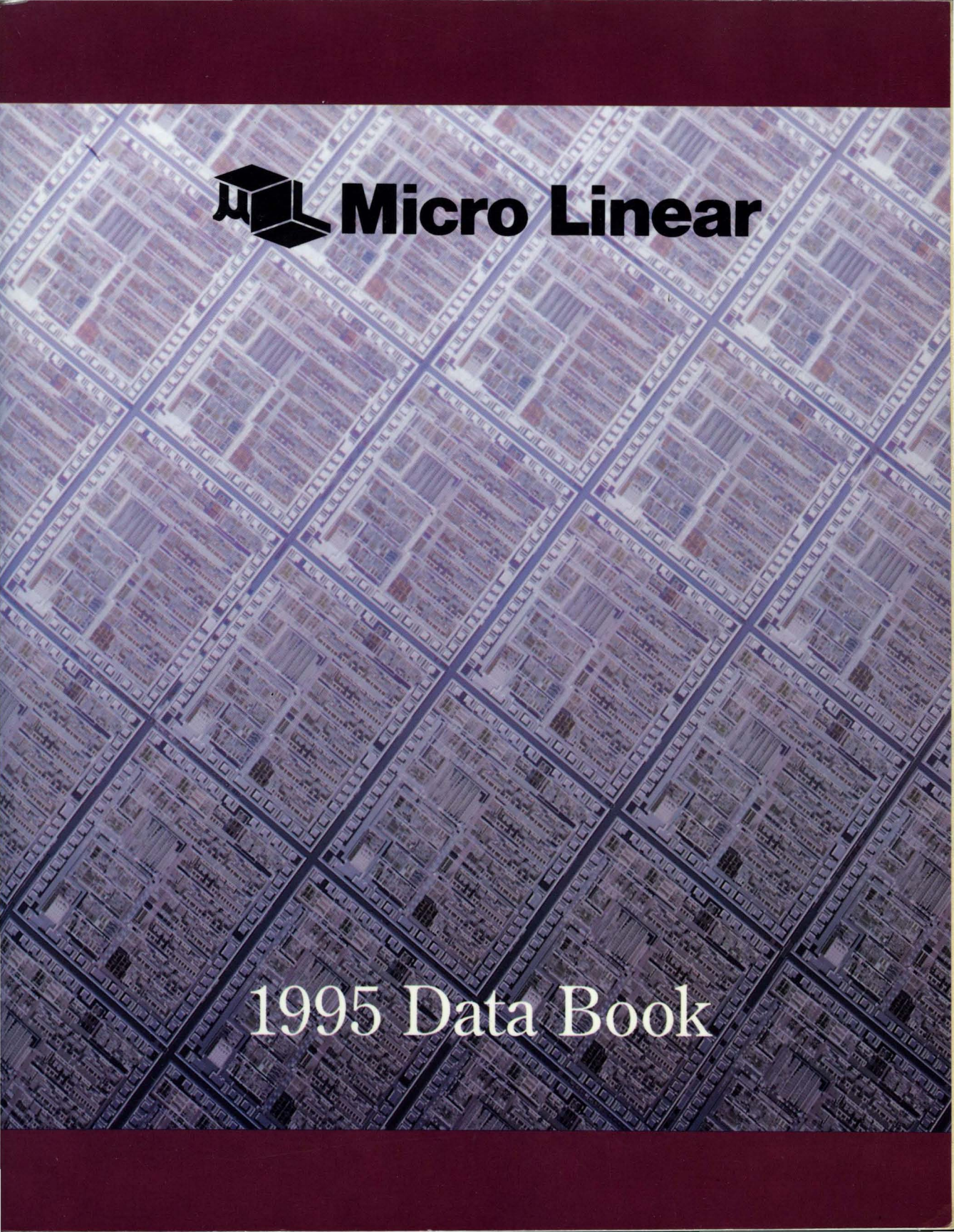
Micro Linear
1995 Data Book

INTRODUCTION

Micro Linear Corporation, headquartered in San Jose, California, designs, develops and markets high performance analog and mixed signal integrated circuits for a broad range of applications within the communications, computer and industrial markets. By combining its analog expertise with a unique development methodology, Micro Linear offers to its customers highly-integrated system-level solutions that add value and reduce systems costs.

This product catalog contains more than 180 standard products many of which are application specific focused on the following areas:

Local Area Networks

Telecommunications

Hard Disk Drives

Magnetic Tape Drives

Magneto-Optical Drives

Motor Controls

Switch Mode Power Supplies

DC to DC Converters

Fluorescent Lamp Ballasts

Data Acquisition Systems

Bus Products

Micro Linear is committed to supplying analog and mixed signal system level solutions to our customers with the highest quality and best service possible.

Micro Linear Corporation
Data Book
1995

LIFE SUPPORT POLICY

MICRO LINEAR'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF MICRO LINEAR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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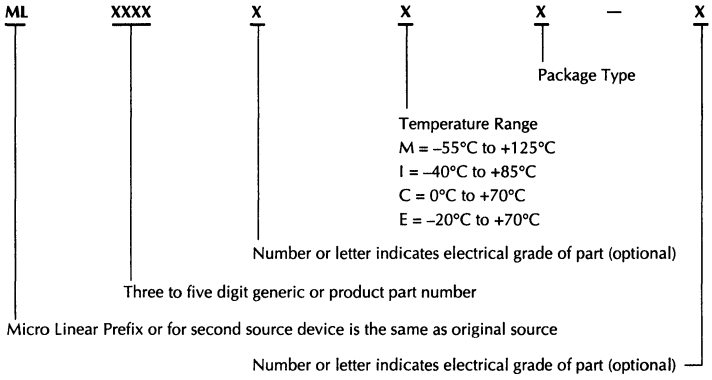
SECTION 9 — PACKAGING INFORMATION (continued)

General Information

Section 1

Part Number and Package Type Explanation

PART NUMBER



PACKAGE TYPE

Letter Suffix	Description
D	Side Brazed Hermetic DIP
F	Flat Pack
G	(PQFP) Plastic Quad Flat Pack
H	Thin Quad Flat Pack (TQFP)
J	Ceramic Hermetic DIP (CERDIP)
K	Quarter Size Small Outline Package (QSOP)
L	Ceramic Leadless Chip Carrier (LCC)
P	Plastic DIP
Q	Plastic Chip Carrier (PCC)
R	Shrink Small Outline Package (SSOP)
S	Small Outline (SOIC)
T	Thin Shrink Small Outline Package (TSSOP)

Alternate Source Part Number

Analog Devices

Analog Devices Part Number	Micro Linear Direct Replacement[1]
AD7820BQ	ML2261CIJ
AD7820CQ	ML2261BIJ
AD7820KN	ML2261CCP
AD7820KP	ML2261CCQ
AD7820LN	ML2261BCP
AD7820LP	ML2261BCQ
AD7820TQ	ML2261CMJ
AD7820UQ	ML2261BMJ
AD7824BQ	ML2264CIJ
AD7824CQ	ML2264BIJ
AD7824KN	ML2264CCP
AD7824LN	ML2264BCP
AD7824TQ	ML2264CMJ
AD7824UQ	ML2264BMJ

Linear Technology

Linear Technology Part Number	Micro Linear Direct Replacement[1]
LTC1060ACJ	ML2110BIJ2
LTC1060ACN	ML2110BCP2
LTC1060AMJ	ML2110BMJ2
LTC1060CJ	ML2110CIJ2
LTC1060CN	ML2110CCP2
LTC1060MJ	ML2110CMJ2

National Semiconductor

National Semiconductor Part Number	Micro Linear Direct Replacement[1]
ADC0808CJ	ML2258BMJ
ADC0808CCJ	ML2258BIJ
ADC0808CCV	ML2258BIQ
ADC0809CCN	ML2258CIP
ADC0809CCV	ML2258CIQ
ADC0820BCJ	ML2261BIJ
ADC0820BCN	ML2261BCP
ADC0820BCV	ML2261BCQ
ADC0820CCJ	ML2261CIJ
ADC0820CCN	ML2261CCP
ADC0820CCV	ML2261CCQ
ADC0820CJ	ML2261CMJ

National Semiconductor

National Semiconductor Part Number	Micro Linear Direct Replacement[1]
ADC0831BCJ	ML2281BIJ
ADC0831BCN	ML2281BCP
ADC0831CCJ	ML2281CIJ
ADC0831CCN	ML2281CCP
ADC0832BCJ	ML2282BIJ
ADC0832BCN	ML2282BCP
ADC0832CCJ	ML2282CIJ
ADC0832CCN	ML2282CCP
ADC0833BCJ	ML2283BIJ
ADC0833BCN	ML2283BCP
ADC0833CCJ	ML2283CIJ
ADC0833CCN	ML2283CCP
ADC0834BCJ	ML2284BIJ
ADC0834BCN	ML2284BCP
ADC0834CCJ	ML2284CIJ
ADC0834CCN	ML2284CCP
ADC0838BCJ	ML2288BIJ
ADC0838BCN	ML2288BCP
ADC0838BCV	ML2288BCQ
ADC0838CCJ	ML2288CIJ
ADC0838CCN	ML2288CCP
ADC0838CCV	ML2288CCQ
ADC08061BCN	ML2261BCP
ADC08061BCV	ML2261BCQ
ADC08061BCWM	ML2261BCS
ADC08061BCJ	ML2261BCJ
ADC08061BMJ	ML2261BMJ
ADC08061CCN	ML2261CCP
ADC08061CCV	ML2261CCQ
ADC08061CCWM	ML2261CCS
ADC08061CCJ	ML2261CCJ
ADC08061CMJ	ML2261CMJ
ADC08061BIN	ML2261BIP
ADC08061BIV	ML2261BIQ
ADC08061BIWM	ML2261BIS
ADC08061BIJ	ML2261BIJ
ADC08061CIN	ML2261CIP
ADC08061CIV	ML2261CIQ
ADC08061CIWM	ML2261CIS
ADC08061CIJ	ML2261CIJ
ADC08064BCN	ML2264BCP
ADC08064BCV	ML2264BCQ
ADC08064BCWM	ML2264BCS
ADC08064BCJ	ML2264BCJ

Note 1. 100% pin-for-pin compatible with improved electrical specifications.
Note 2. Consult data sheet for electrical specifications that may vary from limit or conditions of alternate source.
Note 3. Alternate source ships –40°C to +85°C product as molded; Micro Linear does this on a customer need basis.

National Semiconductor

National Semiconductor Part Number	Micro Linear Direct Replacement[1]
ADC08064BMJ	ML2264BMJ
ADC08064CCN	ML2264CCP
ADC08064CCV	ML2264CCQ
ADC08064CCWM	ML2264CCS
ADC08064CCJ	ML2264CCJ
ADC08064CMJ	ML2264CMJ
ADC08064BIN	ML2264BIP
ADC08064BIV	ML2264BIQ
ADC08064BIWM	ML2264BIS
ADC08064BIJ	ML2264BIJ
ADC08064CIN	ML2264CIP
ADC1061	ML2271
ADC08064CIV	ML2264CIQ
ADC08064CIWM	ML2264CIS
ADC08064CIJ	ML2264CIJ
ADC1061CIJ	ML2271CIJ
ADC1061CIN	ML2271CCP3
ADC1061CIWM	ML2271CCS3
ADC1061CMJ	ML2271CMJ
DP5016QC	ML501-6CQ
DP5016RQC	ML501R-6CQ
DP5018QC	ML501-8CQ
DP5018RQC	ML501R-8CQ
µA5016QC	ML501-6CQ
µA5016RQC	ML501R-6CQ
µA5018QC	ML501-8CQ
µA5018RQC	ML501R-8CQ
DP8464BN-3	ML8464B-3CP2
DP8464BV-3	ML8464B-3CQ2
DP8464BN-2	ML8464B-2CP2
DP8464BV-2	ML8464B-2CQ2
DP8464BN-2	ML8464B-2CP2
DP8464BN-3	ML8464B-3CP2
DP8464BV-2	ML8464B-2CQ2
DP8464BV-3	ML8464B-3CQ2
DP8468BTP-3	ML4568-3CQ2
DP8468BTP-2	ML4568-2CQ2
LMF100CCN	ML2111CCP
LMF100CCWM	ML2111CCS
MF10AJ	ML2110CMJ2
MF10ACN	ML2110BCP2
MF10CCJ	ML2110CIJ2
MF10CCWM	ML2110CCS2
MF10CCN	ML2110CCP2

Silicon Systems, Inc.

Silicon Systems, Inc. Part Number	Micro Linear Direct Replacement[1]
SSI 32P541-CH	ML541CQ
SSI 32P541-P	ML541CP
SSI 32P541A-CH	ML4042CQ
SSI 32P541A-P	ML4042CP
SSI 32P541B-CH	ML4042CQ
SSI 32P541B-P	ML4042CP
SSI 32R4610A	ML6320CS-5
SSI 32R2020R	ML6320CS-5
SSI 32R2024R	ML6320CS-5
SSI 32R2030A	ML6320CS-5
SSI 32R2201R	ML6320CS-5
SSI 32R2300R	ML6320CS-5
SSI 32R2310R	ML6320CS-5
SSI 32R2300R	ML6320CR-3
SSI 32R2310R	ML6320CR-3
SSI 32R501R-6H	ML501R-6CQ
SSI 32R501R-8F	ML501R-8CF
SSI 32R501R-8H	ML501R-8CQ
SSI 32R501R-8P	ML501R-8CP
SSI 32R501-6H	ML501-6CQ
SSI 32R501-8F	ML501-8CF
SSI 32R501-8H	ML501-8CQ
SSI 32R501-8P	ML501-8CP
SSI 32R511R-4S	ML511R-4CS
SSI 32R511R-6H	ML511R-6CQ
SSI 32R511R-6P	ML511R-6CP
SSI 32R511R-6S	ML511R-6CS
SSI 32R511R-8H	ML511R-8CQ
SSI 32R511R-8P	ML511R-8CP
SSI 32R511R-8S	ML511R-8CS
SSI 32R511-4S	ML511-4CS
SSI 32R511-6H	ML511-6CQ
SSI 32R511-6P	ML511-6CP
SSI 32R511-6S	ML511-6CS
SSI 32R511-8H	ML511-8CQ
SSI 32R511-8P	ML511-8CP
SSI 32R511-8S	ML511-8CS

Note 1. 100% pin-for-pin compatible with improved electrical specifications.
Note 2. Consult data sheet for electrical specifications that may vary from limit or conditions of alternate source.
Note 3. Alternate source ships –40°C to +85°C product as molded; Micro Linear does this on a customer need basis.

Texas Instruments

Texas Instruments Part Number	Micro Linear Direct Replacement[1]
ADC0808MJ	ML2258BMJ
ADC0808FN	ML2258BCQ
ADC0808N	ML2258BIP
ADC0809FN	ML2258CCQ
ADC0809N	ML2258CIP
TLC0820ACN	ML2261CCP
TLC0820ACFN	ML2261CCQ
TLC0820BCN	ML2261BCP
TLC0820BCFN	ML2261BCQ
ADC0831ACP	ML2281CCP
ADC0831AIP	ML2281CIJ3
ADC0831BCP	ML2281BCP
ADC0831BIP	ML2281BIJ3
ADC0832ACP	ML2282CCP
ADC0832AIP	ML2282CIJ3
ADC0832BCP	ML2282BCP
ADC0832BIP	ML2282BIJ3
ADC0834ACN	ML2284CCP
ADC0834AIN	ML2284CIJ3
ADC0834BCN	ML2284BCP
ADC0834BIN	ML2284BIJ3
ADC0838ACN	ML2288CCP
ADC0838AIN	ML2288CIJ3
ADC0838CCN	ML2288BCP
ADC0838BIN	ML2288BIJ3

Unitrode

Unitrode Part Number	Micro Linear Direct Replacement[1]
UC1823J	ML4823MJ
UC1825J	ML4825MJ
UC2823N	ML4823IP
UC2823Q	ML4823IQ
UC2825N	ML4825IP
UC2825Q	ML4825IQ
UC3823N	ML4823IP
UC3823Q	ML4823CQ
UC3825N	ML4825IP
UC3825Q	ML4825CQ

VTC

VTC Part Number	Micro Linear Direct Replacement[1]
VM117-2DK	ML117-2CJ
VM117-2PK	ML117-2CP
VM117-4FK	ML117-4CF
VM117-4PK	ML117-4CP
VM117-4DK	ML117-4CJ
VM117-6PK	ML117-6CP
VM117-6DK	ML117-6CJ
VM117-6PK	ML117-6CP
VM117-6PLK	ML117-6CQ
VM117R-2DK	ML117R-2CJ
VM117R-2PK	ML117R-2CP
VM117R-4FK	ML117R-4CF
VM117R-4PK	ML117R-4CP
VM117R-4DK	ML117R-4CJ
VM117R-6DK	ML117R-6CJ
VM117R-6PK	ML117R-6CP
VM117-6PLK	ML117R-6CQ
VM217-6PK	ML501-6CP
VM217-6PLK	ML501-6CQ
VM217-8PK	ML501-8CP
VM217-8PLK	ML501-8CQ
VM7204	ML6320CR-5
VM720H4	ML6320CR-5
VM720L4	ML6320CR-5
VM3204	ML6320CR-3
VM320H4	ML6320CR-3
VM320L4	ML6320CR-3

Note 1. 100% pin-for-pin compatible with improved electrical specifications
Note 2. Consult data sheet for electrical specifications that may vary from limit or conditions of alternate source.
Note 3. Alternate source ships –40°C to +85°C product as molded; Micro Linear does this on a customer need basis.

Alpha Numeric Index

Section 2

8-Bit A/D

PART NUMBER	CONV. TIME	MAX FREQ OF V_{IN}	SAMPLE TIME	INPUTS (MUX)	NON LINEARITY (MAX)	BUS INTERFACE, BITS	SUPPLY VOLTAGE	SUPPLY CURRENT	PIN COUNT	ALTERNATE SOURCES	FEATURES
ML2252	6.6µs	51KHz	0.39µs	2	±1/2, ±1LSB	Parallel	5V	3mA	20		Ratiometric output
ML2258	6.6µs	51KHz	0.39µs	8	±1/2, ±1LSB	Parallel	5V	3mA	20	ADC0808, ADC0809	Superior alternative Superior alternative
ML2259	6.6µs	51KHz	0.39µs	8	±1LSB	Parallel	5V	3mA	28		Ratiometric output
ML2261	0.7µs	500KHz	0.30µs	1	±1/2, ±1LSB	Parallel	5V	15.5mA	20	AD7820, ADC0820, ADC08061 TLC0820	Superior alternative Superior alternative
ML2264	0.7µs	500KHz		4	±1/2, ±1LSB	Parallel	5V	20mA	24	ADC08064	T & H or S & H modes
ML2280	6.6µs	51KHz	0.38µs	1	±1/2, ±1LSB	Serial	5V	2.5mA	8		No zero or full-scale adjustment required
ML2281	6.6µs	51KHz	0.38µs	1	±1/2, ±1LSB	Serial	5V	2.5mA	8	ADC0831	Superior alternative
ML2282	6.6µs	51KHz	0.38µs	2	±1/2, ±1LSB	Serial	5V	3.5mA	8	ADC0832	Superior alternative
ML2283	6.6µs	51KHz	0.38µs	4	±1/2, ±1LSB	Serial	5V	2.5mA	14	ADC0833	Superior alternative
ML2284	6.6µs	51KHz	0.38.µs	4	±1/2, ±1LSB	Serial	5V	2.5mA	14	ADC0834	Superior alternative
ML2288	6.6µs	51KHz	0.38.µs	8	±1/2, ±1LSB	Serial	5V	2.5mA	20	ADC0830	Superior alternative

10-Bit A/D

PART NUMBER	CONV. TIME	MAX FREQ OF V_{IN}	SAMPLE TIME	INPUTS (MUX)	NON LINEARITY (MAX)	BUS INTERFACE, BITS	SUPPLY VOLTAGE	SUPPLY CURRENT	PIN COUNT	ALTERNATE SOURCES	FEATURES
ML2271	1.5µs	150KHz		1	±1/2, ±1LSB	Parallel	5V	35mA	20	ADC1061	Latched 3-state output
ML2375	2µs			4	±1 to ±1LSB	Parallel	5V, 12V	11mA	28		Two channel simultaneous S & H
ML2377	2µs			6	±1 to ±1LSB	Parallel	5V, 12V	11mA	44		Two channel simultaneous S & H

12-Bit A/D + Sign

PART NUMBER	CONV. TIME	MAX FREQ OF V_{IN}	SAMPLE TIME	INPUTS (MUX)	NON LINEARITY (MAX)	BUS INTERFACE, BITS	SUPPLY VOLTAGE	SUPPLY CURRENT	PIN COUNT	ALTERNATE SOURCES	FEATURES
ML2200	31.5µs	12KHz	2.3µs	4	±3/4, ±1LSB	Parallel	±5V	50mA	40		Differential inputs. 16 bit timer & clock. Limit alarm.
ML2208	31.5µs	12KHz	2.3µs	8	±3/4, ±1LSB	Parallel	±5V	50mA	40		16 bit timer & clock. Limit alarm.
ML2221	44µs	8.5KHz	3.2µs	1	±3/4, ±1LSB	Serial	±5V	50mA	16, 20		4-wire interface to µP
ML2223	44µs	8.5KHz	3.2µs	1	±3/4, ±1LSB	Serial	±5V	50mA	16, 20		Async. RS 232 interface
ML2230	31.5µs	12KHz	2.3µs	1	±3/4, ±1LSB	Parallel	±5V	50mA	24		Outputs two 8-bit bytes
ML2233	31.5µs	12KHz	2.3µs	1	±3/4, ±1LSB	Parallel	±5V	50mA	28		Self calibrating. Differential Inputs.

8-Bit D/A

8-BIT D/A	SETTLING TIME	SET-UP TIME	OUTPUT CURRENT	OUTPUT VOLTAGE	NON LINEARITY (MAX)	BUS INTERFACE, BITS	SUPPLY VOLTAGE	SUPPLY CURRENT	PIN COUNT	FEATURES
ML2330	10µs	1.3ns	2mA	20mV-4V 20mV-2V	±1 LSB	Serial	3V, 3.3V, 5V	4mA	8	Dual DAC. Low power.
ML2340	5µs	45ns	–10mA +10mA	V_{CC} – 0.05V	±1/4, ±1/2 LSB	8, µP	5V, ±5V 12V	9.3mA	18	Internal 2.50V reference. 11 bit resolution. Programmable voltage gain: 1/4, 1/2, 1, 2
ML2341	5µs	50ns	5mA	V_{CC} – 0.05V	±1/4, ±1/2 LSB	8, µP	5V, ±5V 12V	5mA	20	Internal 2.50V reference. 11 bit resolution. Programmable voltage gain: 1/4, 1/2, 1, 2
ML2350	5µs	45ns	5mA	V_{CC} – 0.05V	±1/4, ±1/2 LSB	8, µP	5V, ±5V 12V	9.3mA	18	Internal 2.50V reference. 11 bit resolution. Programmable voltage gain: 1/4, 1/2, 1, 2
ML2351	5µs	50ns	5mA	V_{CC} – 0.05V	±1/4, ±1/2 LSB	8, µP	5V, ±5V 12V	5mA	20	Internal 2.50V reference. 11 bit resolution. Programmable voltage gain: 1/4, 1/2, 1, 2
ML2375	2µs	60ns		V_{CC} – 0.25V	±1/4, ±1/2 LSB	16, µP	5V	11mA	28	16 bit timer & clock. Limit alarm.
ML2377	2µs	60ns		V_{CC} – 0.25V	±1/4, ±1/2 LSB	16, µP	5V	11mA	44	16 bit timer & clock. Limit alarm.

10-Bit D/A

8-BIT D/A	SETTLING TIME	SET-UP TIME	OUTPUT CURRENT	OUTPUT VOLTAGE	NON LINEARITY (MAX)	BUS INTERFACE, BITS	SUPPLY VOLTAGE	SUPPLY CURRENT	PIN COUNT	FEATURES
ML2375	2µs	60ns		V_{CC} – 0.25V	±1/4, ±1/2 LSB	16, µP	5V	11mA	28	16 bit timer & clock. Limit alarm.
ML2377	2µs	60ns		V_{CC} – 0.25V	±1/4, ±1/2 LSB	16, µP	5V	11mA	44	16 bit timer & clock. Limit alarm.

ML2200, ML2208

12-Bit Plus Sign Data Acquisition Peripheral

GENERAL DESCRIPTION

The ML2200 and ML2208 Data Acquisition Peripherals (DAP) are monolithic CMOS data acquisition subsystems. These data acquisition peripherals feature an input multiplexer, a programmable gain instrumentation amplifier, a 2.5V bandgap reference, and a 12-bit plus sign A/D converter with built-in sample-and-hold. In addition to a general purpose 8-bit microprocessor interface, the ML2200 and ML2208 include a programmable processor, data buffering, a 16-bit timer, and limit alarms.

The ML2200B and ML2208B self-calibrating algorithmic A/D converters have a maximum non-linearity error over temperature of 0.018% of full-scale, while the ML2200C, ML2200D, ML2208C, and ML2208D have a maximum non-linearity error over temperature of 0.024%.

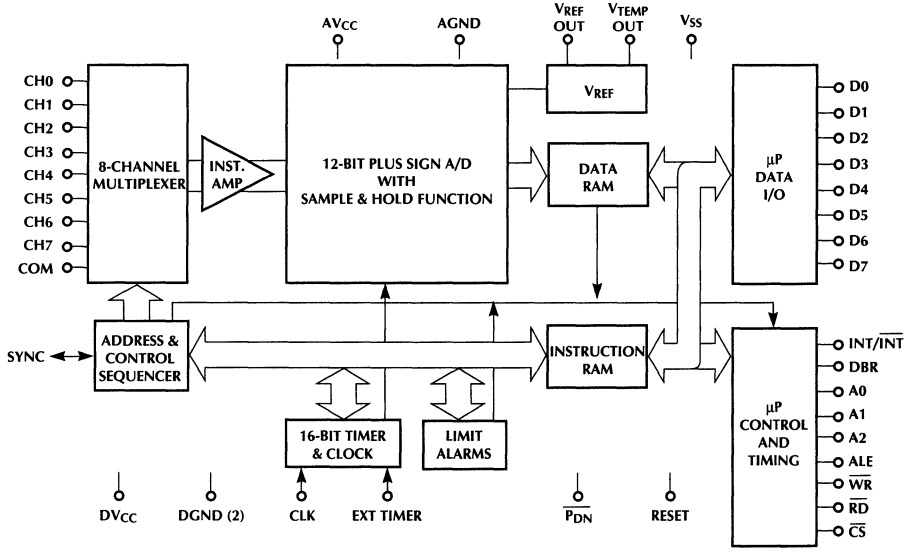
The ML2200 has a four channel differential input multiplexer and the ML2208 has an eight channel single ended input multiplexer.

The digital interface, with software-alterable configurations, is designed to off-load the microprocessor. Control of the DAP is autonomously handled through the control sequencer which receives its instructions from the instruction RAM.

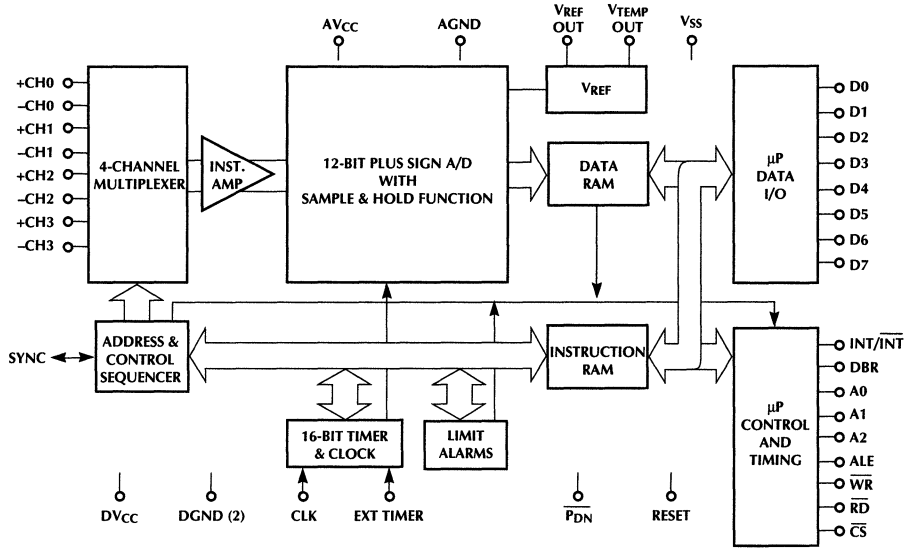
FEATURES

- Resolution 12-bits + sign
- Conversion time (including S/H acquisition) 31.5µs max
- Sample-and-hold acquisition 2.3µs max
- Non-linearity error ±3/4 LSB and ±1 LSB max
- Low harmonic distortion 0.01%
- No missing codes
- Self-calibrating — maintains accuracy over time and temperature
- Inputs withstand |7V| beyond supplies
- Internal voltage reference 2.5V ± 2%
- Four differential or eight single-ended input channels
- Data buffering (8 word data RAM)
- Programmable limit alarm
- 8-Bit microprocessor interface — interrupt, DMA, or polling
- 16-Bit timer for programmable conversion rates
- Standard hermetic 40-pin DIP

BLOCK DIAGRAM



ML2200 BLOCK DIAGRAM



BLOCK SCHEMATIC DIAGRAM

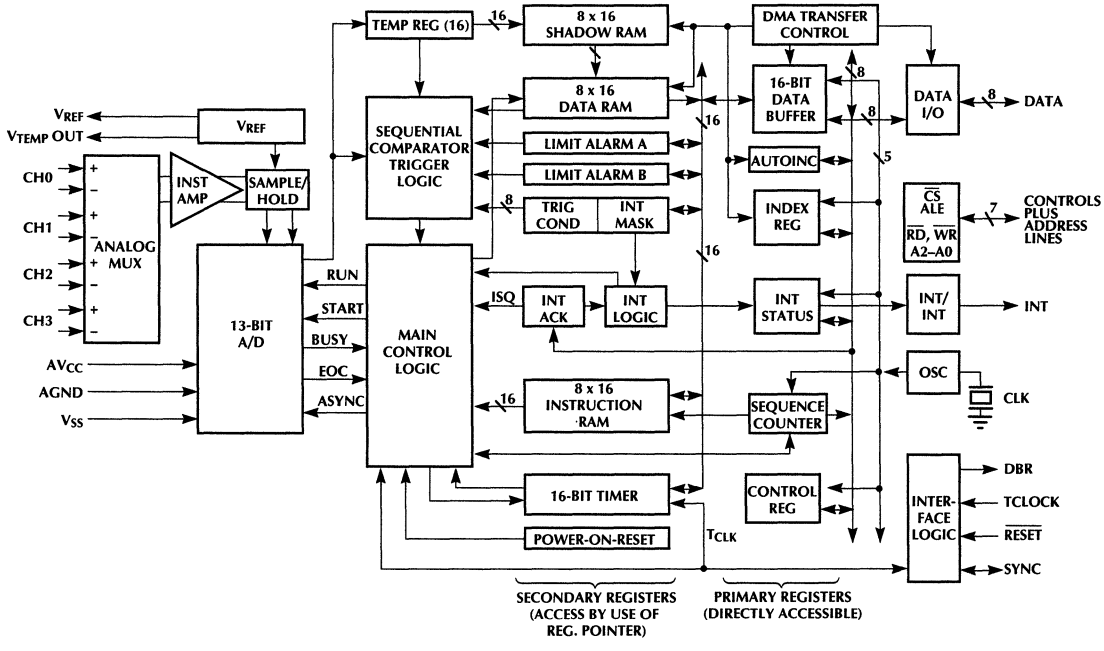


Figure 1. Block Schematic Diagram.

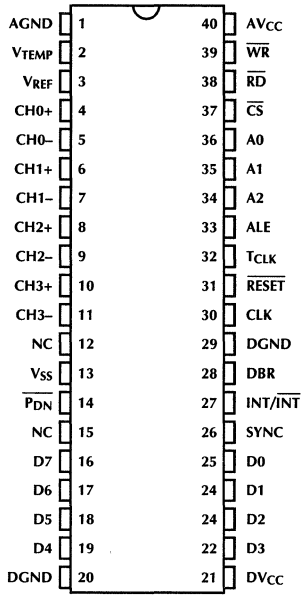
PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	AGND	Analog Ground.
2	V_{TEMP}	Voltage output proportional to the die temperature.
3	V_{REF}	Internal voltage reference output
4-11	CH	Analog Inputs. ML2200 — Positive or negative input of four differential inputs ML2208 — Eight single ended inputs referenced to common pin. Digitally selected by control sequencer.
12	NC COM	ML2200 — No connection. ML2208 — Negative common input for the eight input channels. Tie to analog ground or (V_{SS} +2.5)to (AV_{CC} – 2.5 V)
13	V_{SS}	Negative power supply; decouple to AGND.
14	$\overline{P_{DN}}$	Power-Down Input When $\overline{P_{DN}}$ = 0, device in power-down mode with register contents retained if AV_{CC} >2.0V.
15	NC	No Connection.
16-19	D7, D6, D5, D4	Bidirectional data bits.
20	DGND	Digital Ground.
21	DV_{CC}	Digital power supply. Tie to AV_{CC} from same power supply.
22-25	D3, D2, D1, D0	Bidirectional data bits.
26	SYNC	In the slave mode, SYNC is a positive edge triggered input used to start a conversion. In master mode, SYNC is an output and indicates a conversion has occurred .
27	INT	Interrupt output. A maskable interrupt programmable to be active high or low or will default to active high. INT will not clear until acknowledged in halt mode; not affected by the run or halt state. INT = 0 during reset and inactive during P_{DN}.
28	DBR	Data Buffer Ready output active high indicates that a sequence of operations has completed and data is ready to transfer. DBR is not maskable. It can be used to generate an interrupt in addition to the INT pin when the DBRIE bit in the interrupt mask register has not been enabled. DBR is the DMA request pin when DMA mode is enabled. DBR is not active unless in run mode and at least one sequence of operations has been completed. DBR remains active in the halt mode if not acknowledged; low during reset time and power-down.
29	DGND	Digital Ground.
30	CLK	Clock input. Drive with an external clock or crystal reference to DGND. The crystal must be parallel resonant with minimum capacitive loading (i.e., No bypass caps should be used and leads should be kept short).
31	$\overline{RESET}$	Active low hardware reset with internal pull up resistor of 200K. Tie to system reset line or to grounded capacitor. The capacitor size (usually >6µF) is based on the time the power supplies stabilize, to the time reset voltage reaches 1.4V (>400ms).
32	T_{CLK}	External timer, T_{CLK} is used as external clock input for the 16-bit timer when the T_{CLK} bit in the control register is set to one.
33	ALE	Address latch enable, active low latches information on A0, A1, A2 and $\overline{CS}$. Tie to AV_{CC} to disable use when separate address and data bus are used.
34	A2	Address 2
35	A1	Address 1
36	A0	Address 0
37	$\overline{CS}$	Chip select, active low
38	$\overline{RD}$	Read, active low enables ML2200 or ML2208 to drive data bus.
39	$\overline{WR}$	Write, active low allows writing into the registers.
40	A V_{CC}	Positive analog Power supply. Decouple to AGND. Tie to DV_{CC} from same power supply

PIN CONNECTIONS

ML2200

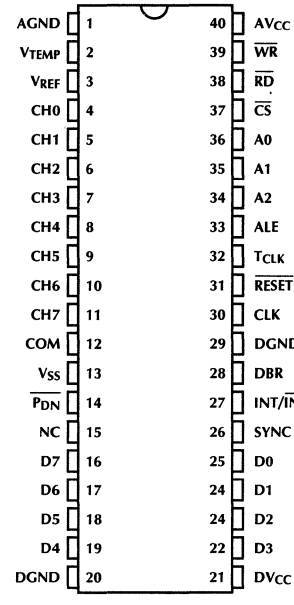
40-PIN DIP



TOP VIEW

ML2208

40-PIN DIP



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages (AV_{CC} and DV_{CC}) 6.0V
Negative Supply Voltage (V_{SS}) ..... – 6.0V
Voltage at Analog Inputs ..... V_{SS} – 7V to AV_{CC} +7V
Voltage at V_{REF} ..... V_{SS} – 7V to AV_{CC} +7V
Input Current per Digital Pin ..... ±10mA
Input Current at Analog Inputs ..... ±20mA
Storage Temperature Range ..... – 65°C to +150°C
Package Dissipation @ 25° C 1W
Lead Temperature (Soldering 10 sec.)
Dual-In-Line Package (Plastic) ..... 260°C

OPERATING CONDITIONS

(Note 2)

Temperature Range ..... $T_{MIN} \le T_A \le T_{MAX}$
ML2200BCP, ML2200CCP, ML2200DCP .....0°C to 70°C
ML2208BCP, ML2208CCP, ML2208DCP .....0°C to 70°C
Supply Voltage (AV_{CC} and DV_{CC}) ..... $4.5V_{DC}$ to $6.0V_{DC}$
Negative Supply Voltage (V_{SS}) ..... $-4.5V_{DC}$ to $-6.0V_{DC}$

ELECTRICAL CHARACTERISTICS

The following specifications apply for AV_{CC} = DV_{CC} = +5V ± 5%, V_{SS} = –5V ± 5%, AGND = DGND = COM = CHX– = 0V, T_A = T_{MIN} to T_{MAX} unless otherwise specified. C_L = 100pF for D0–D7, C_L = 50pF for INT, DBR, and SYNC.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
Converter Characteristics							
	Linearity Error						
	ML2200BCP, ML2208BCP	4	f_{CCLK} = 0.1 ≤ 7MHz			±3/4	LSB
	ML2200CCP, ML2208CCP		f_{CCLK} = 0.1 ≤ 7MHz			±1	LSB
	ML2200DCP, ML2208DCP		f_{CCLK} = 0.1 ≤ 5MHz			±1	LSB
	Unadjusted Zero Error						
	ML2200BCP, ML2208BCP	4				±3/4	LSB
	ML2200CCP, ML2208CCP					±2	LSB
	ML2200DCP, ML2208DCP					±2	LSB
	Unadjusted Positive and Negative Full Scale Error	5				±4	LSB
	Zero Error Temperature Coefficient				0.5		ppm/°C
	Gain Temperature Coefficient		External Reference		3		ppm/°C
	Common-Mode Rejection	13			80		dB
	Analog Input Range	5	All Analog Inputs	V_{SS} – 0.05		AV_{CC} + 0.05	V
	External Source Resistance for Analog Inputs	5	Channel = Analog Input Channel = Voltage Reference			2 0.5	kΩ kΩ
	Differential Analog Input Range		CHX referred to COM for ML2208 CHX+ referred to CHX– for ML2200	$–V_{REF}$		$+V_{REF}$	V
	Off Channel Leakage Current	5, 6	On Chan = 2.5V, Off Chan = –2.5V On Chan =–2.5V Off Chan = 2.5V	–100		 +100	nA
	On Channel Leakage Current	5, 6	On Chan = –2.5V, Off Chan = 2.5V On Chan = 2.5V Off Chan = –2.5V	–100		 +100	nA
	Gain Error		Gain = 2, 4, or 8		0.03		%
Voltage Reference and V_{TEMP} Characteristics							
	V_{REF} Absolute Value	4	Referred to AGND	2.45		2.55	V
	V_{REF} Output Pin						
	Output Resistance	5				300	mΩ
	Minimum Load Resistance	5		1			kΩ
	Maximum Load Resistance	5				50	pF
	Temperature Coefficient				50		ppm/°C
	Line Regulation		4.75 ≤ AV_{CC} ≤ 5.25		1		mV
			–4.75 ≥ V_{SS} ≥ –5.25		1		mV
	Load Regulation		1µA – 2.5mA		1		mV
	Output Noise				100		$µV_{RMS}$
	V_{TEMP} Output Pin				AV_{CC} – 1.5		
	Absolute Value @ 25°C						
	Volts per °C				5		mV/°C

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply for AV_{CC} = DV_{CC} = +5V ± 5%, V_{SS} = –5V ± 5%, AGND = DGND = COM = CHX– = 0V, T_A = T_{MIN} to T_{MAX} unless otherwise specified. C_L = 100pF for D0–D7, C_L = 50pF for INT, DBR, and SYNC.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
DC Characteristics							
	Power Supply Current						
	AI_{CC}, Analog AV_{CC}	4			30	50	mA
	DI_{CC}, Digital DV_{CC}	12	$\overline{RD}$ = $\overline{CS}$ = V_{IH}		10		µA
	I_{SS}, V_{SS}	4			18	30	mA
I_{CC}	Standby Current AI_{CC} + DI_{CC}	4, 9	$\overline{P_{DN}}$ pin = GND		10	1000	µA
I_{SS}	Standby Current				10	1000	µA
	V_{CCPD} Minimum AV_{CC} and DV_{CC} for power-down data retention		$\overline{P_{DN}}$ pin = GND V_{SS} = –5.25 to GND	2			V
	Power Supply Rejection	7					
	AV_{CC}/DV_{CC}		DC		80		dB
			DC to 25kHz, 200mV_{P-P}		50		dB
	V_{SS}		DC		80		dB
			DC to 25kHz, 200mV_{P-P}		50		dB
V_{IL}	Input Low Voltage (except CLK, t_{CLK})	4				0.8	V
V_{IL1}	Input Low Voltage (CLK, t_{CLK})	4				0.8	V
V_{IH}	Input High Voltage (except CLK, t_{CLK})	4		2.0			V
V_{IH1}	Input High Voltage (CLK, t_{CLK})	4		3.5			V
V_{OL}	Output Low Voltage	4	I_{OL} = 2.0mA			0.45	V
V_{OH}	Output High Voltage	5	I_{OH} = –1mA	4.0			V
I_L	Input Leakage Current (except CLK and RESET)	4	GND < V_{IN} < V_{CC}			±10	µA
I_{L1}	Input Leakage Current (CLK)	4	GND < V_{IN} < V_{CC}			±200	µA
I_{L0}	Output Leakage Current (D0 – D7)	4	$\overline{RD}$ = $\overline{CS}$ = V_{IH}			±10	µA
I_{RST}	RESET Pin Source Current	4	$\overline{RESET}$ = 0V	15	50	100	µA
C_I	Input Capacitance (All Digital Inputs)				10		pF
C_O	Output Capacitance (All Outputs and D0 – D7)				20		pF
AC Electrical Characteristics (Note 8)							
t_C	Conversion Time	4, 9	CLK Mode = 0, f_{CLK} = 7.0MHz	31.5			µs
			CLK Mode = 0, f_{CLK} = 5.0MHz	44.0			µs
	Sample and Hold Acquisition	4, 9	CLK Mode = 0, f_{CLK} = 7.0MHz			2.3	µs
			CLK Mode = 0, f_{CLK} = 5.0MHz			3.2	µs
SNR	Signal-to-Noise Ratio		V = 10kHz, 2.5V Sine. f_{CLK} = 7MHz ($f_{SAMPLING}$ = 31.8kHz). Noise is sum of all nonfundamental components up to 1/2 of $f_{SAMPLING}$.		73		dB
THD	Total Harmonic Distortion		V = 10kHz, 2.5V Sine. f_{CLK} = 7MHz ($f_{SAMPLING}$ = 31.8kHz). THD is sum of 2, 3, 4, 5 harmonics relative to fundamental.		–75		dB

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply for AV_{CC} = DV_{CC} = +5V ± 5%, V_{SS} = –5V ± 5%, AGND = DGND = COM = CHX– = 0V, T_A = T_{MIN} to T_{MAX} unless otherwise specified. C_L = 100pF for D0–D7, C_L = 50pF for INT, DBR, and SYNC.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
AC Electrical Characteristics (Note 8) (Continued)							
IMD	Intermodulation Distortion		V_{IN} = f_A + f_B. f_A = 9kHz 1.25V sine. f_B = 10kHz, 1.25 sine. f_{CLK} = 7MHz ($f_{SAMPLING}$ = 31.8kHz). IMD is (f_A + f_B), (f_A – f_B), ($2f_A$ – f_B), ($2f_A$ + f_B), (f_A + $2f_B$), (f_A – $2f_B$) relative to fundamental.		–75		dB
FR	Frequency Response		V_{IN} = 0 to 10kHz, 2.5V sine relative to 1kHz		0.01		dB
f_{CLK}	CLK Frequency	4	(No crystal)	0.1		7	MHz
f_{CLKX}	CLK Frequency	4	(Crystal)	3		7	MHz
f_{CLKI}	Internal CLK Frequency				1/2		f_{CLK} or f_{CLKX}
f_{CLKT}	CLK Frequency (t_{CLK} only)	4				f_{CLKI}	MHz
f_{CLKW}	Minimum Clock High/Low Width (CLK)	5		50			ns
f_{CLKWT}	Minimum Clock High/Low Width (t_{CLK})	5		75			ns
t_{RF}	Maximum Rise/Fall Times, All Inputs	5				25	ns
t_{RESET}	Minimum Reset Active Time	4, 10		10			f_{CLK} Periods
t_{PDN}	Power-Up Time		Time After P_{DN} = V_{IH}		1		ms
Non-Multiplexed Data Bus Timing							
t_{AL}	Address to ALE Setup Time	4		20			ns
t_{LA}	Address Hold Time After ALE	4		20			ns
t_{LC}	Latch to RD or WR Control	4		20			ns
t_{RD}	Valid Data Delay from Read	4				150	ns
t_{AD}	Address Stable to Valid Data	5		150			ns
t_{LL}	ALE Width	4		80			ns
t_{DF}	Data Bus Float After Read	4		10		50	ns
t_{CL}	Read or Write Control to ALE	4		20			ns
t_{CC}	Read or Write Control Width	4		150			ns
t_{DW}	Data Setup Time for Write	4		100			ns
t_{WD}	Data Hold Time for Write	4		0			ns
t_{RV}	Recovery Time Between Two Reads or Writes	4		250			ns
t_{AD}	Address Stable to Valid Data	5		150			ns
t_{AR}	Address Stable Before Read	4		0			ns
t_{RA}	Address Hold Time for Read	4		0			ns
t_{RR}	Read Pulse Width	4		150			ns
t_{RD}	Data Delay from Read	4				150	ns
t_{DF}	Read to Data Float	4		10		50	ns

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply for AV_{CC} = DV_{CC} = +5V ± 5%, V_{SS} = –5V ± 5%, AGND = DGND = COM = CHX– = 0V, T_A = T_{MIN} to T_{MAX} unless otherwise specified. C_L = 100pF for D0–D7, C_L = 50pF for INT, DBR, and SYNC.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
Non-Multiplexed Data Bus Timing							
t_{RV}	Recovery Time Between Two Reads or Writes	4		250			ns
t_{AW}	Address Stable Before Write	4		0			ns
t_{WA}	Address Hold Time for Write	4		0			ns
t_{WW}	Write Pulse Width	4		150			ns
t_{DW}	Data Setup Time for Write	4		100			ns
t_{WD}	Data Hold Time for Write	4		0			ns
DMA Interrupt and SYNC Timings							
t_{CKDBR}	Clock to DBR Assert	11, 4	DMA		120	190	ns
t_{RDD}	Read to DBR Negation on Last Byte	4			110	170	ns
t_{CKDBR}	Clock to DBR or t_{CKINT}, INT Assert	11, 4	Non-DMA		100	180	ns
t_{WRDBR}	Write to DBR or t_{WRINT} INT Negation	11, 4			70	120	ns
t_{CKSYNC}	Clock to SYNC Delay	11, 4	Master Mode		150	220	ns
t_{SYNCN}	SYNC Input Width	5		3			f_{CLKI}
t_{SYNCCK}	SYNC to Clock Setup	4	Slave: Mode 4 Only	50			ns
t_{SYNCO}	Minimum SYNC Output Width	4		4		4	f_{CLKI}

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: 0°C to +70°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 6: Leakage current is measured with the clock not switching.

Note 7: Power supply rejection is the ratio of the change in zero error to the change in power supply voltage.

Note 8: All parameters measured from 0.8V to 2.0V.

Note 9: Power-down current is with power-down pin at GND potential only. Any other level will dissipate more power. Other digital input pins may float but cannot be above VDD or below GND.

Note 10: RESET should be held active for at least 10 internal clocks after power supplies have stabilized to within 5% of 5V

Note 11: Since the internal master clock is the input clock divided by 2, this number can be either the maximum listed or the maximum listed plus 1/2 the input clock period.

Note 12: When RD = CS = V_{IL}, the current into the DV_{CC} pin depends on the data bus pins D0 – D7.

Note 13: Common-Mode rejection is the ratio of the change in zero error to the change in common-mode input voltage.

TIMING DIAGRAMS

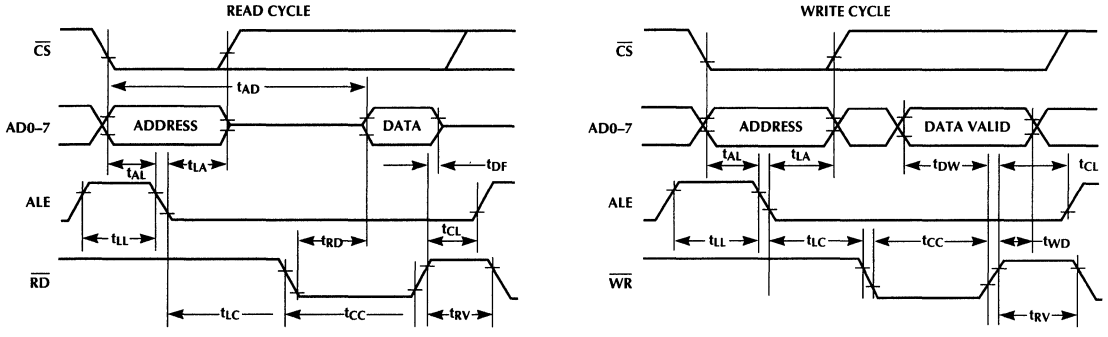


Figure 2. Multiplexed Bus.

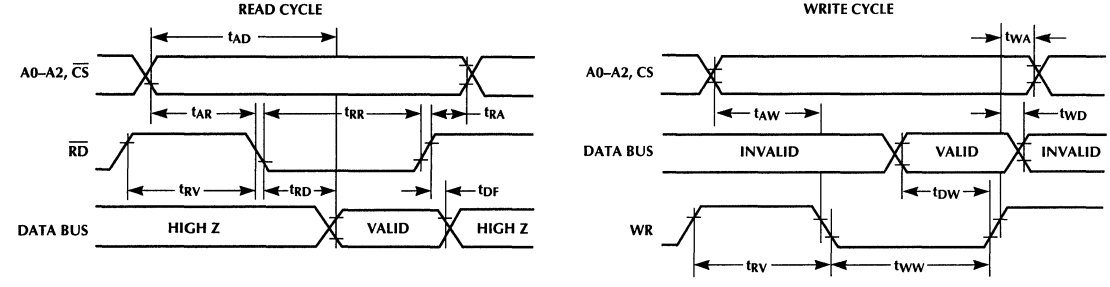
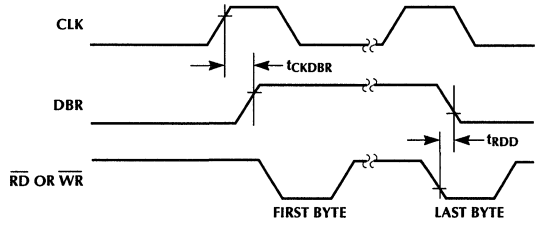


Figure 3. Non-Multiplexed Bus.

TIMING DIAGRAMS (Continued)



Note: There are 2*n Read Operations where n is the number of words to be transferred DBR is set and cleared by internal circuitry. DMA bit in the control register must be set for this operation.

Figure 4. DMA Mode.

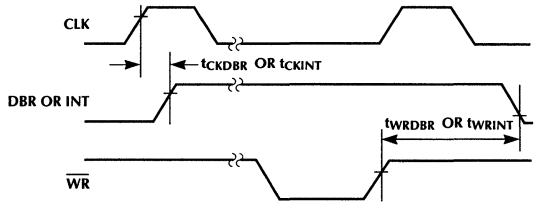


Figure 5. DBR and INT (Non-DMA Mode).

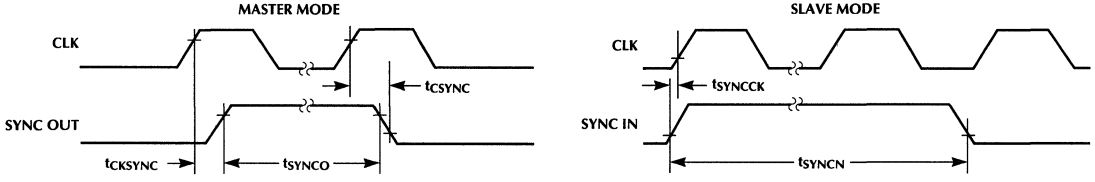


Figure 6. SYNC

1.0 FUNCTIONAL DESCRIPTION

1.1 ALGORITHMIC A/D CONVERTER

Micro Linear's algorithmic converter uses a successive approximation technique. Most of today's successive approximation converters use a DAC to feed back the approximated signal, however this technique requires more circuitry than algorithmic converters. In addition the values of all of the resistors or capacitors in the DAC must be matched to within the accuracy of the converter. This is difficult to do in silicon beyond 10 bits unless trimming is used. An algorithmic converter uses less circuitry and is more easily trimmed. Micro Linear's algorithmic converter is implemented using a 2x amplifier, a sample/hold amp, and a comparator as shown in Figure 7.

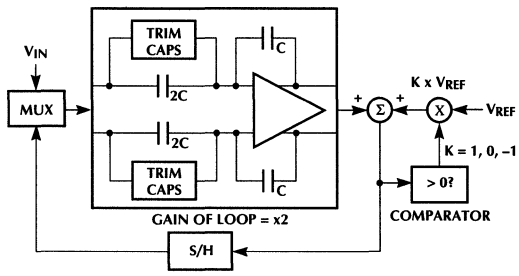


Figure 7. Self Calibrating A/D Converter.

The input sample is first multiplied by two then compared to the reference voltage. If the 2x input voltage is greater than the reference, the MSB is a 1 and the reference voltage is subtracted from the 2x input voltage. The remainder is stored in the sample-and-hold. If the 2x input voltage is less than the reference, the MSB is a 0 and the 2x input voltage is stored in the sample-and-hold. This process repeats again, however now the sample-and-hold voltage is multiplied by 2.

Self-Calibration

In order to maintain integral and differential linearity to the ½ LSB level in an algorithmic converter, two critical parameters need to be controlled, loop offsets and the gain of the loop. Loop offsets are automatically nulled before each conversion using auto-zeroing circuitry on both the sampling amp and the 2x amp. The gain of the loop is adjusted using self-calibration .

Self-calibrating the algorithmic converter, once the offsets have been nulled, is performed by measuring the 2x gain of the loop and adjusting it. The gain can be measured by converting the reference voltage as the input as well as the reference (V_{REF}/V_{REF}), and examining the output code. Converting V_{REF} should yield plus full-scale, since V_{REF}/V_{REF} should equal 1. If the gain of the loop is slightly less than 2, the resulting LSB of the conversion will be "0" . If the magnitude bits of the resulting conversion are all "1s",

the gain may be too great, therefore the gain is reduced to the point where the threshold of the LSB is reached.

Adjustment of the 2x gain is done with the binary weighted trim capacitor arrays connected to each of the 2C input capacitors. A small value of capacitance is either added to or subtracted from the 2C input caps until the gain of the loop is within 13-bit accuracy of 2.

1.2 MULTIPLEXER INPUT

The input voltage is ±2.5V relative to COM of the ML2208 or a CH– of the ML2200. The input voltages under normal operation must not exceed supply voltages by 0.05V. Each channel is selected by the programmable sequencer.

1.3 INTERNAL VOLTAGE REFERENCE AND V_{TEMP}

The internal bandgap voltage reference with a temperature coefficient of 50 ppm /°C has an external use current of 2.5mA.

The voltage reference V_{TEMP} output is directly proportional to the chip temperature.

1.4 CONVERSION TIMES

The following table lists the conversion times which include the sample-and-hold acquisition time. For a CALRD and CALWR no A/D conversion actually takes place.

Operation	Number of Internal Clocks*
8-bit A/ D	80
13-bit A/ D	110
CALWR	52
CALRD	80

*Internal clock is the external clock divided by two.

1.5 SAMPLE-AND-HOLD TIMING

Figure 8 shows the internal timing for the sample-and-hold circuitry. The relationship between the "Start of Conversion" and the input channel going into sample mode is fixed at 6 internal clocks, regardless of the Start Mode. Six internal clocks after the Start of Conversion, the Sample-and-Hold is switched into the sample mode, placing two 9pF capacitors in parallel with the input pins; one on CH+ and one on CH– for the ML2200, and CH and COM for the ML2208. The sample switch is kept in the sample mode for 8 internal clocks (2.3µs at a 7MHz external clock), then placed in the hold mode. During the next 2 internal clocks the charge on the sample-and-hold is transferred into the A/D, after which the V_{REF} pin is sampled for 8 internal clocks.

Figure 8 also illustrates the timing of the SYNC pin in Master Mode during a conversion. SYNC is activated one internal clock cycle before the Start of Conversion and lasts for four internal clocks.

1.6 ANALOG INPUTS DIFFERENTIAL INPUTS AND COMMON-MODE REJECTION

The differential inputs of the ML2200 eliminate the effects of common-mode input noise (60Hz, for example), as CH+ and CH– are sampled at the same time.

Noise

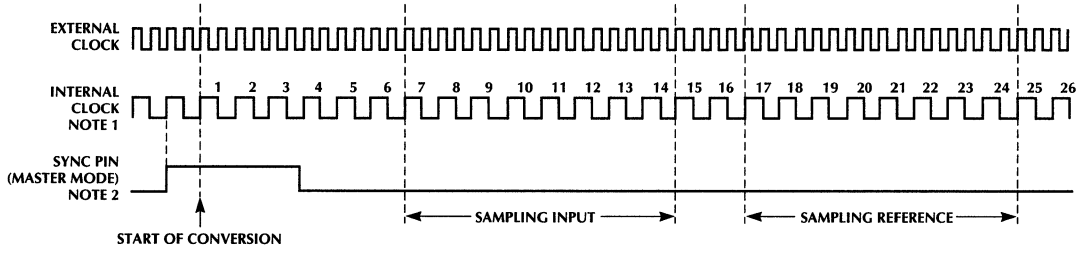
The leads to the analog inputs should be kept as short as possible to minimize output noise. Noise as well as digital clocks can couple into the inputs and cause errors. Input filters can be used to reduce the effects of these sources.

Power Supply Decoupling

Low inductance tantalum capacitors of 1µF or greater and 0.01µF disc ceramic capacitors are recommended for bypassing AV_{CC} as well as V_{SS} to AGND. These capacitors should be placed close to the AV_{CC} and V_{SS} pins.

2.0 µP HARDWARE INTERFACE

The microprocessor interface is a byte-oriented structure which occupies eight memory or I/O locations in the microprocessor's address space. Each register is readable and writable via the chip select, read and write pins, three address lines, and 8-bit data bus.



Note 1: External clock in phase with internal clock using RESET.
Note 2: Immediate execute mode where start of conversion and start of operation occur at the same time

Figure 8. Sample-and-Hold Timing.

Interfaces are shown for multiplexed address data bus in Figure 9 and Figure 10. When non-multiplexed interfaces are used, ALE can be tied high. All internal address and chip select latches are transparent.

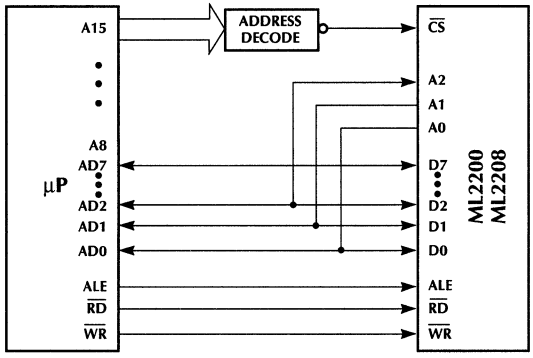


Figure 9. 8-Bit Multiplexed Bus Interface.

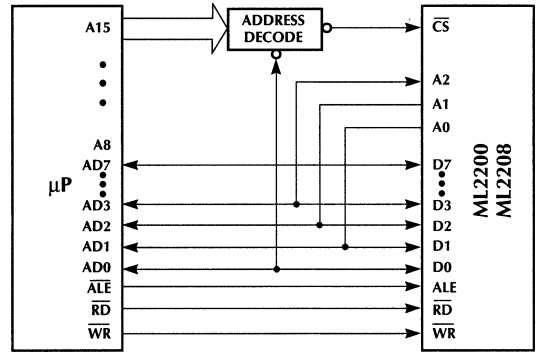


Figure 10. 16-Bit Multiplexed Bus Interface.

2.1 INTERRUPTS

The ML2200 and ML2208 provide two interrupt pins, one for control/status interrupts (INT), and one for data interrupts (DBR). The standard INT pin is maskable via an interrupt mask register while the DBR pin is always enabled to signify that data is available. DBR can be mapped into the INT pin if only one interrupt pin is desired.

The interrupt pin (INT) can be programmed, via the Interrupt Bit Mask register, to be active high, or active low. When programmed for active high, it is driven in both directions. When INT is programmed for active low, it is an open drain output, therefore an external pull-up resistor of 2.5 kΩ or more should be used. The DAP's Status register can be read to determine whether its interrupt is active or not.

2.2 DMA

The separate DBR pin can also serve as a DMA request signal when DMA operation is enabled in the Control register. DBR goes active high when the data buffer is full and ready to be read. DBR remains high until the last byte in the data buffer has been read. This allows back-to-back DMA cycles or single cycle transfers depending on how the DMA controller is programmed. The data for the DMA cycle is transferred over the 8-bit data bus at address 0 (A0 – A2 =0). The ML2200 or ML2208 automatically places both high and low bytes of the 16-bit wide data buffer at address 0 or 1 for the DMA controller to read. The LOBYT bit in the Control register specifies whether the high or low byte is placed on the bus first. Figure 11 shows a block diagram interfacing to the 8237 DMA controller.

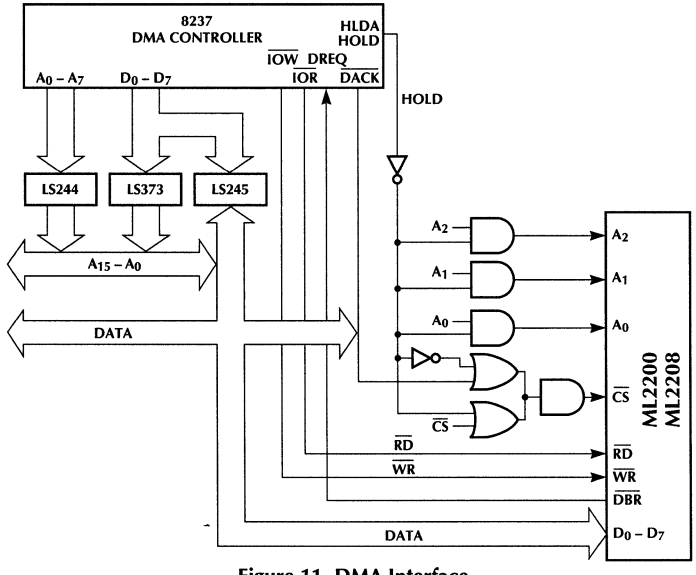


Figure 11. DMA Interface.

3.0 REGISTER DEFINITIONS

These data acquisition peripherals contain six directly addressable 8-bit registers, and twenty indirectly addressable 16-bit registers. Figure 12 illustrates the register architecture while Figures 13, 14 & 15 illustrate the bit maps and addresses. The first three primary registers (Window Low, Window High, and Index) are used to access the 20 secondary registers. Window Low and Window High provide read /write access to the low and high bytes of the secondary register pointed to by Index.

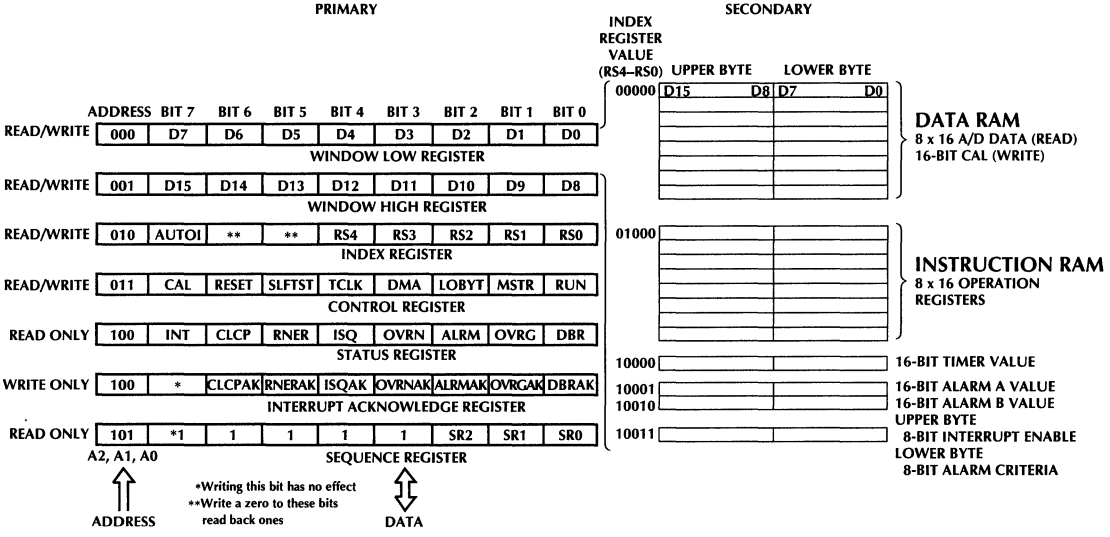


Figure 12. Register Architecture.

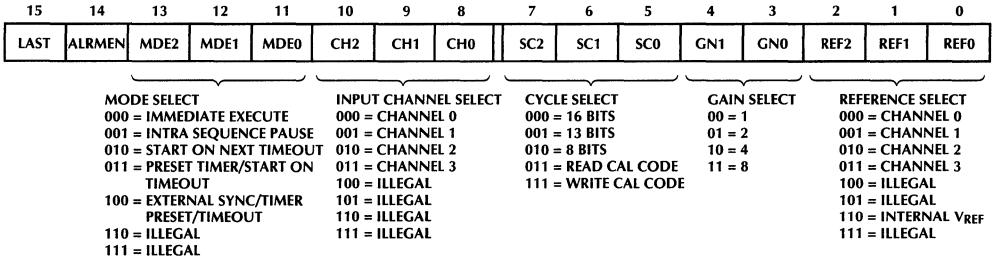


Figure 13. ML2200 Bit Map of Instruction RAM.

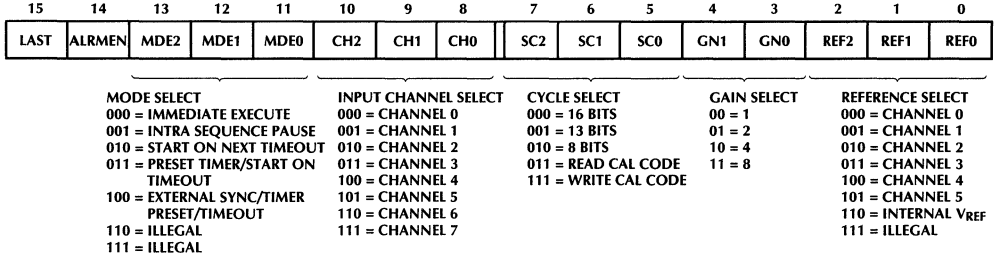


Figure 14. ML2208 Bit Map of Instruction RAM.

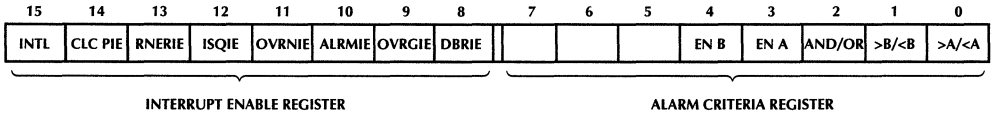


Figure 15. Interrupt Enable and Alarm Criteria Registers.

3.1 Primary Registers

READ/ WRITE

D7	D6	D5	D4	D3	D2	D1	D0

Window Low Register

READ/ WRITE

D15	D14	D13	D12	D11	D10	D9	D8

Window High Register

Window Registers— Registers 0 and 1

These registers form a two-byte window into the secondary registers. Window Low is the low byte of the secondary 16-bit word, and Window High is the high byte. Any one of the 20 words in the secondary register set can be accessed by first setting a 5-bit address in the Index register, then reading from or writing to the Window registers. Sequential access of the secondary registers is also available without writing to the Index register via the AUTOI bit in the Index register.

Index Register — Register 2

READ/ WRITE

AUTOI			RS4	RS3	RS2	RS1	RS0

Index Register

RSX = Secondary Register Address (Bits 0 to 4): The lower five bits of this register (RSO – RS4) define the location within the secondary register set that the window registers are positioned at.

Bits 5 and 6: Undefined. Writing to these bits have no effect, however a zero should be written; always read as ones.

AUTOI = autoincrement (Bit 7): Setting AUTOI signifies that the lower five addressing bits in the Index register are automatically incremented after either the Window Low or Window High register is accessed. Whether the autoincrement occurs when accessing Window Low or Window High register, is based on the LOBYT bit in the Control register.

Interrupt Operation Caution!!! — Using the autoincrement feature with interrupt driven software deserves special attention. A problem can arise when an interrupt service routine accessing the secondary registers, interrupts another routine accessing secondary registers. This problem can be avoided one of two ways: disable the interrupt in the main routine while accessing secondary registers, or reload the index register to its entry value when exiting the interrupt routine.

Note: The Index register is automatically cleared only under two conditions, one is a RESET, the other is when mode is used. This register is reset to 0 in DMA mode just prior to the DMA request (DBR going active). DMA mode uses the index register for operation, so the index register should never be written to when RUN and DMA are set.

Control Register — Register 3

READ/ WRITE

CAL	RESET	SLFTST	t_{CLK}	DMA	LOBYT	MSTR	RUN

Control Register

RUN (Bit 0): Setting this bit to a one will cause the chip to start executing the operations defined in the Instruction RAM, beginning with location 0. This is referred to as the Run mode. Clearing this bit will place the ML2200 in the Halt mode. The run bit is initially cleared on power up or after a hardware or software reset. In order to properly start the chip operation, the RUN bit should be set after setting all other applicable bits in the control register. The act of halting the chip will always reset the sequence pointer to operation 0. Thus, the next time RUN is asserted, the chip starts from operation 0 again. Placing the chip in the Run or Halt mode has no effect on the Interrupt pins (INT and DBR), nor the status bits in the status register. It is recommended that secondary registers only be written to in the Halt mode. Writing to secondary registers in the Run mode will cause the RNER status bit to be set, indicating a run error. All of the status bits in the Status register should be acknowledged (cleared) before entering the Run mode.

MSTR = master (Bit 1): Indicates whether the SYNC pin will be an input or an output. If set the chip will enter the master mode of operation and the SYNC pin will become an output pin which puts out a sync pulse at the beginning of each operation. This serves as a signal for other slave chips that are used in a synchronous operating method. While in master mode, any operation requiring a sync input will not proceed, and the chip will "hang", waiting for a sync that will never come. The chip default is slave mode with the SYNC pin as an input.

LOBYT = low byte first (Bit 2): This bit is used to indicate which byte is accessed first in AUTOI or DMA operation. When this bit is set, the index register is incremented on the read or write of the Window High register. When this bit is clear, the index register is incremented on the read or write of the Window Low register. If DMA operation is specified, then setting this bit will make the low byte be output first, then the high byte, after which the index register is incremented. Conversely, clearing this bit will output the high byte first, then the low byte, then increment the index register. The default is low.

DMA = DMA Mode (Bit 3): When set enables DMA operation. DMA operation proceeds as follows:

1) The DMA bit must be set after defining all other registers (Instruction RAM, Alarm etc.) but prior to setting the RUN bit. The RUN bit is then set.

2) The sequence of operations in the Instruction RAM is executed.

3) At the end of the sequence, the DBR pin goes true, requesting DMA service, and the Index register is automatically cleared, pointing to the first location of the data buffer.

4) Each read of either Window Low or Window High register outputs a byte from the data registers. The DMA controller can read Window Low register, or Window High register, or alternate between Window Low and Window High. The same data is placed in both Window Low and Window High registers, and updated in both of them when either one is read. The data is placed in the Window registers beginning with data word 0 and incrementing on up. The placement of the low byte/ high byte order is based on the LOBYT bit in the Control register. The number of bytes transmitted equals twice the number of operations defined, since the words are 16-bits going over an 8-bit bus. DBR remains asserted until all of the bytes have been transmitted. It is negated on the leading edge of the last byte read pulse. DBR acknowledge (setting the DBRAK bit in the Status register) is not required when transferring bytes via DMA.

The AUTOI bit does not have to be set when in the DMA mode. Setting the DMA bit forces the Index register to be auto-incremented in the Run mode. However if AUTOI is not set, then when in Halt mode autoincrement will not be enabled. If the AUTOI bit and DMA bit are both set, the autoincrement will occur in both the Run mode and the Halt mode.

t_{CLK} = enable external timer clock (Bit 4): When set, will divert the clock input for the internal sixteen bit timer to the t_{CLK} pin. When reset to 0, the timer runs at the internal chip clock frequency, which is ½ of that generated at the CLK pin.

SLFTST = self test (Bit 5): When set, the function of the input multiplexer is modified to enable self test operations. This bit also redefines the Instruction Word, specifically the CHAN field of the instruction word (See Figure 16 for the redefinition of the Instruction Word when SLFTST = 1). With SLFTST set the CHAN bits now specify which of four self tests is to be performed as shown below.

Instruction Word CHAN Field	Function	Description
000	System Offset	Inputs shorted together and shorted to ground
001	Internal Reference	Convert internal V_{REF}, plus side tied to V_{REF}, minus side tied to AGND
010	Minus Internal	Convert internal V_{REF}, Reference minus side tied to V_{REF}, plus side tied to AGND
011	Common Mode	Both inputs of the converter are tied to V_{REF}
100-111	Illegal	

These self-test results are useful for user confidence at power on. The default on reset is 0, normal mode of operation.

RESET = soft reset (Bit 6): Is a software reset of the chip. This bit does not have to be cleared once set. The microprocessor should read this bit back to determine if the reset operation has completed, especially if a slow clock rate is being used. It takes at least 4 internal clocks for the reset bit to clear. Microprocessor communication with the chip should be held off until this bit is read back as cleared. When issuing a hardware reset, communication with the chip should be held off until the $\overline{RESET}$ pin goes inactive. The chip will be in the Halt mode (RUN bit cleared) after a reset. See RESET/Power-On Conditions (Section 4.2) for chip register conditions after a reset.

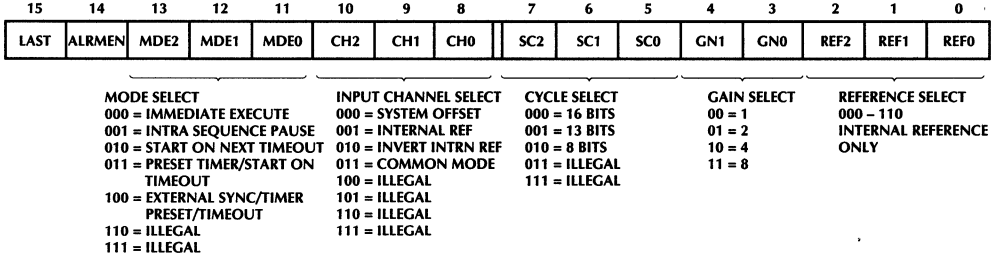


Figure 16. Bit Map of Instruction Word When SLFTST = 1.

CAL = calibration start (Bit 7): When set, a self-calibration of the A/D converter will begin. Reading the CAL bit indicates whether the chip has been calibrated since the last reset or power-on condition. If CAL is a 1, then a calibration of the A/D converter has been performed since the last reset or power-up. When setting CAL, the user should not write a 0 back to clear it. ***Writing a 0 to the CAL bit has no effect;*** this will not clear it if it was previously set. Attempting to set the RUN bit without this bit being set will result in a run error condition, in which the RNER status bit will be set, and an interrupt being generated if it was enabled in the mask register. The amount of time required for calibration is 8,260 internal clocks, or 16,520 external clocks. To determine when a calibration is complete, the microprocessor should enable the calibration complete interrupt (CLCPIE) in the interrupt mask register, and wait for the interrupt to occur. Interrupt servicing of the calibration complete interrupt is done in a normal manner, in which the interrupt is acknowledged by setting the CLCPAK bit in the interrupt acknowledge register. All I /O to the ML2200 should be avoided during calibration (i.e., 16,520 external clocks after the CAL bit is set), because accessing the chip during calibration could adversely affect the calibration. If an interrupt is not desired, the microprocessor can read the Status register to verify completion 16,520 external clocks after the CAL bit is set. When the CAL bit is set, all other bits in the Control register should be cleared. DO NOT set the CAL and RUN bits simultaneously.

Status Register — Register 4

READ ONLY

INT	CLCP	RNER	ISQ	OVRN	ALRM	OVRG	DBR

Status Register

Register 4 serves as the status register of the various conditions that can occur. The bits in the Status register will be updated regardless of the Mask register. The status bits are updated any time within or at the end of a sequence of operations. The bits in the Status register are cleared by setting the corresponding bits in the Interrupt Acknowledge register. The status register can be polled at any time without fear of clearing the status bits. This register is not cleared at HALT time. When entering the Run mode, all of the old status bits should be cleared (acknowledged).

DBR = Data Buffer Ready (Bit 0): Is set when the chip has gone through one complete sequence of operations and has filled the data registers with the converted results. This bit signifies that the microprocessor should read all locations in the data registers that have relevant data. Reading all loaded data locations will clear DBR. If all loaded data locations are not read, DBRAK in the Interrupt Acknowledge register should be set to clear DBR, else OVRN will be set. The DBR pin is logically the same as the DBR status bit. The DBR pin is ALWAYS enabled and cannot be masked out. The DBR status bit is the only condition that can cause the DBR pin to be asserted. The DBR status bit can be enabled to assert the INT pin through the Interrupt Mask register.

OVRG = overrange interrupt (Bit1): Is set at the end of an operation when an underflow or overflow of the A/D converter has occurred (underflow and overflow are the most negative and most positive number, respectively, that is representable in the chip according to the specified cycle length). The overflow and underflow conditions apply to ALL incoming A/D converted data.

ALRM = limit alarm (Bit 2): Is the limit alarm status bit. It is set whenever the alarm criteria specified in the alarm registers is satisfied by a conversion from an operation where the ALRMEN bit is enabled. The limit alarm test only applies to an operation in which the ALRMEN bit is set.

Note that OVRG and ALRM can be enabled without enabling the DBR interrupt so that the microprocessor can be left alone until an overflow/underflow or limit alarm occurs. This is done to search for a limit condition first without taking any data into the microprocessor. Doing this, however, will set the OVRN (overrun error) bit in the status register, indicating that the microprocessor has not read any data from previous sequences.

OVRN = overrun error (Bit 3): The OVRN bit indicates that the microprocessor has missed from one byte to several blocks of data. Even if an overrun error occurs, the ML2200 or ML2208 continues converting the inputs and updating the data registers with the new conversions.

This bit may intentionally become set as a result of searching for the overflow/underflow or limit alarm criteria without reading the data.

The setting of the OVRN bit also occurs in DMA mode if all data has not been read by the completion of the next sequence. (Note: DBRAK should not be set in DMA mode, since DBR is automatically cleared by the chip.) If OVRN occurs in DMA mode, DBR will not be reactivated once all of the data from the sequence which was overrun is read; OVRN automatically disables DBR reactivation. Acknowledging OVRN (setting OVRNAK in the Interrupt Acknowledge register) will re-enable the DBR pin, however the OVRN bit may immediately be set again before the DMA controller can read the entire buffer. Therefore, it is recommended that in DMA mode if OVRN gets set, put the ML2200 or ML2208 in the Halt state, acknowledge the overrun and the DBR, then place the chip back in the Run mode.

ISQ = intra-sequence pause (Bit 4): Indicates that the chip has halted operation within a sequence as a result of choosing the ISQ op code in the mode field of the Instruction word. Setting the ISQAK bit in the interrupt acknowledge register will then restart the operation within the sequence. This lets the microprocessor achieve timing control of individual operations within a sequence.

RNER= run error (Bit 5): Indicates that an error occurred either entering or operating in the Run state. The following operational errors cause the RNER bit to get set

1. Entering the Run state without having performed a self-calibration after the most recent Reset or power-up. The status of whether a calibration was executed or not is indicated by the CAL bit in the control register. If the CAL bit in the Control register is a one, the chip has already been calibrated.
2. Writing to any secondary registers other than the data registers during Run mode. All secondary register locations are readable during Run time.

CLCP = calibration complete (Bit 6): Is set at the end of a calibration sequence. The purpose of this bit is to notify the microprocessor that a self-calibration has completed.

INT = interrupt (Bit 7): Is identical to the state of the INT pin. The INT status bit and pin is an OR of the status bits enabled in the Interrupt Mask register. While the polarity of the INT pin can be defined in the interrupt mask register, this bit is positive true only.

Interrupt Acknowledge Register — Register 4

WRITE ONLY

	CLCPAK	RNERAK	ISQAK	OVRNAK	ALRAK	OVRGAK	DBRAK

Interrupt Acknowledge Register

The status bits in the status register can only be cleared by setting the appropriate bit in this register; writing a zero has no effect. The relative bit positions in the Interrupt Acknowledge register are identical to the Status register except for bit 7, which is valid for reads (see explanation in Status Register) and undefined for writes (user must write a zero to this bit to be software-compatible for possible future redefinitions).

Sequence Register — Register 5

READ ONLY

1	1	1	1	1	SR2	SR1	SR0

Sequence Register

During the RUN mode, this register can be read back to indicate the current operation in progress. This is especially useful for examining interrupts when multiple intra-sequence pauses are specified. Bits 3–7 always reads 1s.

Registers 6 and 7— these registers are reserved for future use.

3.2 SECONDARY REGISTERS

There are twenty 16-bit wide secondary registers containing the Data RAM, Instruction RAM, Timer, Alarms, Alarm Criteria Register, and Interrupt Mask. Except for the Data RAM, the secondary registers should only be accessed on initialization, or when the chip is placed in the Halt mode.

Secondary Registers 0 to 7

Data RAM (read only)
Calibration Holding Register (write only)

	UPPER BYTE		LOWER BYTE		
	D15	D8	D7	D0	
0					8 x 16 A/D DATA REGISTERS
1					
2					
3					
4					16-BIT CAL REGISTERS
5					
6					
7					

The Data RAM consists of eight 16-bit wide registers that hold the output results from the latest conversion sequence. Each word in the Data RAM has a one-for-one correspondence with a word in the Instruction RAM. The Data RAM is also referred to as the data output registers.

The data output registers are double buffered and readable by the microprocessor at any time. The A/ D converter fills a "shadow" bank of registers during conversions, while the microprocessor is free to read the output registers. When the sequence is done, the "shadow" bank information is transferred to the output registers for the microprocessor to read, after which time DBR is asserted. Therefore, the microprocessor has essentially one sequence time to drain the data buffer. This time varies according to the number of operations defined, the system clock frequency, the mode field for each operation, and the cycle length (number of bits to be converted). Refer to Conversion Times for more information.

Data Format

All data is returned from the converter in 16-bit two's complement format, right hand justified, with the sign bit extended across the most significant unused bits.

Cycle	+Max	–Max	Mid-Range
16	7FFF	8000	0000
13	0FFF	F000	0000
8	007F	FF80	0000

Calibration Holding Register —

This register is for diagnostic purposes only. It is one 16-bit wide register mapped into the write only secondary address space 0 to 7 (i.e., a write to any of the secondary addresses 0-7 will load the Calibration Holding register). This register is write only and cannot be read back directly. It is used when the mode field in the Instruction Word is set to CAL Write, and the Instruction is executed. This command takes the contents of the Calibration Holding register and loads it into the Calibration register of the A/D converter. Note that this will change the calibration of the A/D converter, and a calibration of the A/D converter should be done after a CAL Write command is issued.

Instruction RAM — Secondary Registers 8 to 15 (Read/Write)

OP	0	8
OP	1	9
OP	2	10
OP	3	11
OP	4	12
OP	5	13
OP	6	14
OP	7	15

8 x 16 OPERATION REGISTERS

The Instruction RAM, sometimes referred to as the Operation registers, consists of eight 16-bit wide registers broken up into seven different fields (see Figures 10 and 10A). Each Instruction or Operation defines a single conversion, where the converted data result is stored in the corresponding data output register. Note that when the SLFTST bit in the Control register is set, the Instruction Word is redefined for diagnostic mode. Figure 12 illustrates the redefinition when SLFTST is set. The following section defines the seven different fields making up the Instruction word when SLFTST = 0.

D15	D14	D13 – 11	D10 – 8	D7 – 5	D4, 3	D2 – 0
LAST	ALRMEN	MODE	CHAN	CYCLE	GAIN	REF

REF (Bits 2,1, 0 — Voltage Reference Selection) REF specifies the source of the voltage reference used for the A/ D conversion.

GAIN (Bits 4 and 3 — Gain Settings) GAIN defines the gain of the precision instrumentation amplifier. The gain can be either 1, 2, 4, or 8. Each gain factor of 2 adds an additional 4 internal clock cycles (1 /f_{CLKI}) to the conversion time. Therefore a gain of 8 adds an additional 12 internal clock cycles to the conversion time.

CYCLE (Bits 7, 6, 5 — Cycle Select) CYCLE defines one of five different cycles: 8-, 13-, or 16-bit conversions, and READ or WRITE CAL CODE. Choosing 8-, 13- or 16-bit cycles determines how many bits the A/ D converter will convert. However, even though the converter has a 16-bit cycle, it may not have 16-bits of useful resolution. The useful resolution of the converter can be determined from the linearity specs.

Since the algorithmic converter is a successive approximation type of converter, an 8-bit cycle requires the least amount of time to convert, and the 16-bit cycle requires the most. Refer to Sampling Rates and Conversion Times for the exact number of clocks each cycle takes.

READ CAL CODE and WRITE CAL CODE cycles are for diagnostic purposes only. READ CAL CODE reads the Calibration register in the A/D converter and loads it into the corresponding data output register. WRITE CAL CODE transfers the contents of the Calibration Holding register into the A/D converter's Calibration register. The transfer is complete after the operation is executed. Refer to Diagnostics for more information on READ and WRITE CAL CODE.

CHAN (Bits 10, 9, 8 — Input Channel Number) defines the input channel to be converted.

ALRMEN (Bit 14 — Alarm Enable) When this bit is set the alarm criteria for the operation is enabled, otherwise the alarm is disabled for this operation. If ALRMEN is set and the alarm condition is met, the ALRM bit in the Status register will be set at the end of the operation.

LAST (Bit 15 — Last Operation) signifies that this operation is the last operation of the sequence. The chip will return to and begin the first operation of the sequence after execution of the current operation. If all eight operations are specified, the last one MUST have this bit set.

MODE (Bits 13,12,11—Mode Selection) defines the condition that must be met for the operation to proceed. The mode field also has an effect on the Operation Execution Time.

000	Immediate Execute
001	Intra-Sequence Pause
010	Start on Next Time out
011	Preset Timer/Start on Time out
100	External Sync Start
101	External Sync/Timer Preset/Time out
110	ILLEGAL
111	ILLEGAL

Events That Occur Within an Operation

To better understand six modes of the ML2200 or ML2208 one must first understand the events that occur during an operation. This can be aided by referring to Figure 17.

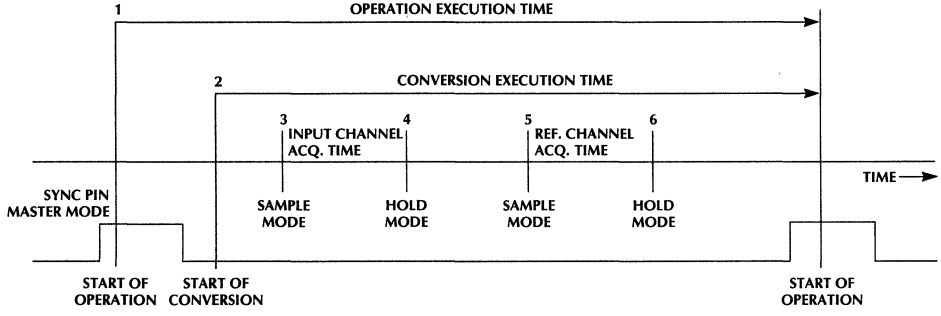


Figure 17. Events Within an Operation.

The first event that occurs in the Operation is the Start of Operation. This may or may not be the beginning of the conversion, depending on the mode selected. The time between the Start of Operation and Start of Conversion is variable. When the conditions of the mode have been met, the Start of Conversion occurs.

The Conversion Execution time includes the input and reference acquisition times, the gain time, and the successive approximation conversion time. Shortly after the Start of Conversion the S/H goes into sample mode acquiring the input channel for eight internal clocks. After the input has been acquired the S/H goes into hold mode, disconnecting the S/H from the input channel, and transferring the charge into the A/D converter. A couple of clocks later the same S/H goes into sample mode on the reference voltage, either the internal V_{REF} or one of the input channels. The reference acquisition time for all six modes is the same; eight internal clocks. After the S/H goes into hold mode the successive approximation A/D conversion begins. When the conversion is complete the next operation begins.

Immediate Execute (000) — The Start of Conversion begins at the Start of Operation. In other words, the conversion begins the instant the operation begins. There is no gating item delaying the conversion. This mode allows the chip to convert at its maximum rate with no unnecessary delays. As an example of calculating the sequence time, if all eight operations used Immediate Execute with a gain of 1 and a 13-bit conversion, the time to execute one sequence (all eight operations) would be 8 x 110 = 880 internal clocks.

Intra-Sequence Pause (001) — This mode provides a way for the microprocessor to initiate conversions, rather than the other modes which either initiate conversions from internal timings or an external pulse. At the Start of Operation the ISQ status bit is set. The microprocessor will recognize the setting of the ISQ status bit either by polling the Status register, or having enabled the ISQ interrupt. The Start of Conversion is delayed until the ISQAK bit in the Interrupt Acknowledge register is set.

Start on Next Time out (010) — After the Start of Operation occurs the Start of Conversion is delayed until the internal timer decrements from 1 to 0. When using this mode the timer will be free-running. This means that the timer is initialized in the Halt mode and left alone to decrement and reload automatically when in the Run mode. This mode can be used to establish a specific sampling rate. Note that the timer value must be greater than the conversion time, therefore this mode can only slow the sampling rate down from its maximum rate. In the case where several operations are used, and only one of them uses this mode, the timer value must be greater than all the other Operation Execution times plus the current operation conversion time.

Preset Timer/Start on Time out (011) — At the Start of Operation the timer is loaded with its pre-programmed count. The delay between the Start of Operation and the Start of Conversion is the pre-programmed count. Execution time of the operation is the pre-programmed timer count plus the conversion time. As opposed to mode 2, the timer can be any value between 2 and 2^{16}; i.e., there is no restriction on the timer value being greater than the conversion time. One application of this mode would be when an external analog event is triggered by the SYNC pulse, and the conversion needs to be delayed by a programmable amount of time.

Using the External SYNC Input — The following description applies to modes 4 and 5, since these two modes use the external SYNC input. These modes should only be used when the SYNC pin is programmed as an input (MSTR bit in Control register is 0). If the external SYNC signal arrives before the Start of Operation, it may be latched depending upon the arrival time. If it arrives 22 clocks after the previous operation's Start of Conversion, external SYNC will be latched; any time before will miss the pulse. Therefore the external SYNC pulse rate should not be any faster than the frequency of the operations which use this mode, otherwise there will be more external SYNC pulses than conversions.

External SYNC Start (100) — After the Start of Operation, the Start of Conversion is delayed until the rising edge of the SYNC pulse and the next rising edge of the internal clock. Unless the rising edge of the external SYNC is synchronized with the internal clock (See t_{SYNCCK} Spec), the aperture uncertainty is one internal clock.

External SYNC/Timer Preset/Time out (101) — For this mode, the external SYNC pulse presets the timer, and when the timer times out the Start of Conversion begins. The timer is preset after the rising edge of the external SYNC and the next rising edge of the internal clock. When the timer transitions from 1 to 0, the Start of Conversion begins. As in the previous mode, unless the rising edge of the external SYNC is synchronized with the internal clock, the aperture uncertainty is one internal clock.

Timer Functions of the Different Modes — The on-chip timer is started when RUN is asserted. It then free-runs, pre-loads and restarts itself at the pre-programmed count unless one of the modes in an operation word specifies a timer preset. If "Start on Next Timeout" mode is selected for all operations, the timer free-runs and subsequently starts conversions on regular intervals, without the inclusion of any variable overhead timing requirements of any specific operation. The "preset timer" function that can be specified in any operation, functions as a "one-shot" time out feature; however it can upset the regularity of conversions. The use of the external SYNC start allows flexibility with asynchronous conditions outside the chip. In addition, the use of time out with external SYNC allows synchronous operation of multiple Micro Linear chips with interleaved operation. If a different rate is desired other than increments of one master clock cycle (1/2 the CLK pin frequency) or if external events need to be counted before starting an operation, then setting the t_{CLK} bit in the control register will divert the timer to the t_{CLK} pin for all operations.

Timer Holding Register — Secondary Register 16 — This register holds the pre-programmed value of the timer. The value is in 1 internal clock increments, or the period of t_{CLK} if this input is used. The timer is a countdown timer, therefore the realized delay will be the number loaded into the Timer Holding register multiplied by the clock period. The value is written as a 16-bit binary word, and

either high or low bytes can be written first. These registers are both writable and readable, with register writes executed only when the chip is in the Halt mode (RUN bit cleared in the control register). Reading the Timer Holding register will return the preprogrammed value for the timer, it will not provide the actual timer value. Timer Holding register values of 1 or 0 are illegal and will "hang up" the timer when placed in Run mode. Therefore the minimum value that can be loaded into the Timer holding register is 2. The timer is decrementing when in Run mode and idle when in Halt mode. When the chip is placed in Run mode, the timer is automatically loaded with the value in the Timer Holding Register, and begins to count down.

Alarm Registers — Secondary Registers 17, 18 (Read /Write) — These registers specify the alarm criteria against which the converted data of a current operation is compared. The comparison occurs only when the ALRMEN bit is set within the operation. Secondary register 17 is Alarm A and secondary register 18 is Alarm B. These values are written in two's complement format, right justified and sign extended (refer to Data Format for more information).

Alarm Criteria Register— Secondary Register 19 lower byte (Read/Write) — Specifies the compare criteria to be used with alarm registers A and B. Bit 0 specifies whether the comparison of alarm word A is to be greater than (setting the bit) or less than equal to (clearing the bit). Similarly, bit I specifies the same criteria for alarm word B. The criteria of the two groups can be "ANDed" or "ORed" together by clearing (OR) or setting (AND) bit 2. Bits 3 and 4 enable the alarm comparison for words A and B, respectively. Bits 5, 6, and 7 are unused and be can be any value when written, always read as ones. The following table illustrates all of the possible combinations, X signifies don't care.

Bit Number					
4	3	2	1	0	
ENB	ENA	AND	GB	GA	Test Done:
0	0	X	X	X	No Test
0	1	X	X	0	≤ A
0	1	X	X	1	> A
1	0	X	0	X	≤ B
1	0	X	1	X	> B
1	1	0	0	0	≤ B or ≤ A
1	1	0	0	I	≤ B or >A
1	1	0	1	0	> B or ≤ A
1	1	0	1	1	> B or > A
1	1	1	0	0	≤ B and ≤ A
1	1	1	0	1	≤ B and > A
1	1	1	1	0	> B and ≤ A
1	1	1	1	1	> B and > A

Using the various criteria, the chip can discern whether a certain channel is inside or outside a band, or greater than or less than a value. Notifying the microprocessor can be done through an interrupt or by polling the status register.

Interrupt Mask— Secondary Register 19 Upper Byte (Read/Write)

D15	D14	D13	D12	D11	D10	D9	D8
INTL	CLCPIE	RNERIE	ISQIE	IVRNIE	ALRMIE	OVRGIE	DBRIE

This register is used to define which interrupt conditions are capable of setting the hardware interrupt pin and the INT bit of the Status register. The bits in the Interrupt Mask register are interrupt enable bits, meaning when the bits are set they enable the corresponding status bit to activate the hardware interrupt pin as well as the INT bit in the Status register. The INTL bit determines the polarity of the INT pin. If set, the INT pin becomes active low, with an open drain output. If clear, the INT pin becomes active high, with driving capability in both directions.

Secondary Registers 20 to 31 — Undefined
These registers are undefined and will cause unpredictable results if read or written to.

4.0 SAMPLING RATES AND CONVERSION TIMES

To determine the sampling rate, one must first determine the sequence execution time. A sequence is defined as the number of operations or instructions used. Therefore the sequence execution time equals the sum of the individual operation execution times. The simplest case for determining the sampling rate is when only one operation is used in the sequence. Then the sampling period is the operation execution time. If all eight instructions are used in the sequence, the sampling rate would be the sequence rate multiplied by the number of times the channel was sampled in the sequence.

It is possible to sample one channel more frequently than another. For example, if every other operation sampled channel 0, while the remaining operations sampled channels 1, 2, and 3, the sampling rate for channel 0 would be four times the sampling rate of the other channels. If periodic sampling is important, one must be careful when sampling a channel multiple times in a sequence since different operations can have different execution times.

EXAMPLE: SAMPLING FOUR CHANNELS IN A BURST EVERY 10 MS

Using Mode 2 "Start on Next Time out" for Instruction 0 will establish the 10ms sampling rate, once the clock is initialized properly. Instructions 1, 2, and 3 can each use Mode 0 "Immediate Execution." For the ML2200, each instruction can sample a different channel, thus covering all four channels in a burst. For the ML2208, the same holds true except all eight channels can be sampled in a burst, periodically.

Assuming the external clock is 7MHz and each conversion is 13 bits with a gain of 1, the conversion time for each operation will be 110 x 286 ns = 31.4µs. Therefore four instructions will require 4 x 31.4µs = 125.7µs. The execution time is much less than the sampling rate, thus the timer can be used to set the sampling rate. The timer value for a 10 ms sample rate is: 10 ms/286 ns = 35,000 decimal or 88B8H.

OPERATION OR INSTRUCTION EXECUTION TIME

Figure 17 illustrates the Operation Execution Time. The time between the Start of Operation and Start of Conversion is variable and depends on the Mode chosen. For more information on how to determine the time between Start of Operation and Start of Conversion refer to the Secondary registers Mode field description in the Instruction RAM.

The Conversion Execution time depends on the Cycle, the Gain, and the Mode chosen in the instruction word. Modes 0–5 all behave the same way when it comes to Conversion Execution Time. To help determine the Conversion Execution Time the following table gives the number of internal clocks used for Modes 0–5 based on the Cycle chosen.

Cycle	Number of Internal System Clocks Needed ($1/f_{CLKI}$)
16-Bit	128
13-Bit	110
8-Bit	80
Read CAL	80
Write CAL	52

Add 4 extra clocks to the Cycle time for each gain of 2 (including Read CAL and Write CAL). For a gain of 2 add 4 extra clocks, for gain of 4 add 8 extra clocks, for gain of 8 add 12 extra clocks. Example: Modes 0–5, Cycle = 13-bit conversion with a gain of 8. Conversion Execution time is 122 internal clocks.

5.0 MICROPROCESSOR INITIALIZATION PROCEDURE

The following sequence of steps is recommended when initializing the ML2200 from the microprocessor:

1) Keep reset active for at least 10 internal clock cycles after power supplies have stabilized. If a software reset is issued, hold off microprocessor communications with the chip until the RESET bit in the control register is read back as cleared, which takes 4 internal clock cycles.

2) If desired, check the data register path by performing a write and read of the calibration register for all 8 operations. (This step is optional, but does provide user assurance of the integrity of the on-chip data paths.) The calibration register is a full 16-bit data path.

3) Perform a calibration by first enabling the CLCP interrupt in the Interrupt Mask register, then start the calibration by asserting the CAL bit i n the Control register. Alternately, if an interrupt driven system is not desired, the interrupt status register can be polled 8260 internal clocks after the CAL bit has been set. The chip should not be polled during calibration.

4) Upon receiving the CLCP interrupt, acknowledge it. If desired, read back the calibration code to verify a successful calibration. Other diagnostics may be run at this time, however diagnostics are optional and not required.

5) Load the Instruction RAM, alarm criteria, interrupt conditions, and timer. Set the proper data transfer mode up (DMA, interrupt driven or polled mode.) Clear all status bits before setting the RUN bit.

6) Start the chip running by setting the RUN bit in the Control register. This may be done by ORing the RUN bit with the other bits already configured in the Control register; however do not set the CAL bit again or another calibration will take place. Writing a 0 to the CAL bit has no effect; it will still read 1.

5.1 RESET/ POWER-ON CONDITIONS

When applying power to the ML2200, DV_{CC} and AV_{CC} should never be powered-on at different times.

It is OK to assert both $\overline{RD}$ and $\overline{WR}$ during RESET time, but not legal to do so otherwise; this may damage the chip internally.

The following list specifies the affected registers on the chip after a reset is performed. Note that both hardware and software reset of the chip have identical effects.

All registers shown below are cleared (all bits 0):

Primary Registers:
Index register (register 2)
Control register (register 3)
Status register (register 4)
Sequence status (register 5)

Secondary Registers:
Interrupt bit mask (upper half, register 19)
Alarm criteria register (lower half, register 19)

All other registers will have random data in them after power on. If a hardware or software reset is performed later, registers which are not listed above will be unchanged. Re-calibration after a hardware or software reset is not necessary, since the calibration register remains the same after a reset. Only after a power-up is a calibration necessary. However the CAL bit in the Control Register will be cleared after a reset. Setting the RUN bit while the CAL bit is clear will cause the RNER bit to be set. But, if a calibration had been done before the reset, the RNER may be ignored.

5.2 TIMER

If any of the operations require a timer function, (either a one-shot or regular conversion interval) then the timer value must be written. This is done by writing the index register value to 10 hexadecimal and writing the proper 16-bit time value to the window registers. The timer value must be greater than 1. If using mode 2 "Start on Next Time out" the timer value must be greater than the conversion time.

5.3 LIMIT ALARM OPERATION

The chip may be set up to watch for certain data conditions by enabling the proper interrupt bits in the Interrupt Mask register. These conditions include A/D overrange/ underrange and user-defined alarm criteria. In order to use the alarms, the A and B alarm values must be defined. Note that since alarm registers A and B are 16 bits wide, 13-bit two's complement sign extended values must be loaded. (Refer to Data Format for more information). In order to further qualify alarm registers A and B, the Alarm Criteria register must be initialized.

5.4 DEFINING INTERRUPT CONDITIONS

If the chip is used in polled situations, the interrupt mask bits need not be set unless the "OR" of the interrupt conditions, bit 7 in the Status register is used.

If the chip is used in interrupt mode rather than polled mode, the desired interrupt conditions should be considered. In addition to the interrupts specified for data comparison operations, several other interrupts can be defined in the Interrupt Mask register. The DBR bit can be set if the DBR pin is not used. This enables interrupts at the end of sequences for data transfer via the INT pin. The intra-sequence interrupt bit should be enabled if intra-sequence pauses are desired in any of the operations. Overrun error and run-time error bits should be enabled if trapping of these errors is desired.

Note that alarm A and B and overrange interrupts occur at any time within the sequence of operations. Due to the interrupt latency time of the microprocessor, multiple interrupts of this type within a sequence may be indistinguishable from each other. The A and B alarms should generally be used on only one operation so that its source can be determined with no ambiguity. Overrange interrupts can be handled by examining the data in the chip at the end of the sequence.

The INT pin polarity can be defined to be active high (bit 15 cleared in the Interrupt Mask register) or active low (bit 15 set). When active low is chosen, the INT pin is open drain without a pull-up. When active high, the INT pin is driven actively in both directions. The default condition is active high, and the INT pin is actively driven low during reset time.

6.0 METHODS OF DATA TRANSFER TO THE MICROPROCESSOR

There are several ways to handle the data output; polling, interrupt, or DMA. If interrupts are the method chosen, method 5) may be preferable. Method 5) DMA/Interrupt mode, does not require a DMA controller. It simply uses the DMA mode of the ML2200 or ML2208 which can be interfaced to an interrupt controller.

1) Intra-Sequence pause instruction is used when the microprocessor is not going to periodically/continuously read the data, but it will read the data at arbitrary times. The Table 1 below shows the op codes to sample all eight channels.

   Using these instructions the program begins when the RUN bit is set in the control register. Immediately after RUN is set, before the first conversion takes place, the ISQ bit in the status register is set. This indicates that the sequencer has paused. When the microprocessor wants to read a value on one or more of the channels it sets the ISQAK bit in the Interrupt Acknowledge register. The ML2208 then performs eight conversions back-to-back, jumps back to sequence 0, and sets the ISQ and DBR bits in the status register. The data from all eight channels is now available in the Data RAM. The next time a conversion is desired, once again the microprocessor sets ISQAK in the interrupt acknowledge register.

2) Polled mode transfer is done simply by polling the status register and examining the DBR bit to see if a sequence has been completed. The DBRIE interrupt mask bit need not be set, but an acknowledge should be done by setting DBRAK in the Interrupt Acknowledge register, otherwise an overrun error will occur. The CPU can just poll the INT bit in the Status register. Only the bits which are enabled in the Interrupt Mask register will set the INT status bit. When the INT bit is set, the CPU can examine the other status bits to determine which requests are active.

3) Interrupt mode can be implemented using the INT pin and enabling the desired interrupt conditions in the Interrupt Mask register. The polarity of the INT pin can be selected at the same time. If desired, DBR can be used as a second interrupt pin to signify the transfer of data only. This may be useful in systems with multiple and prioritized interrupt structures. If DBR is used, the DBR mask bit in the interrupt mask register should be disabled or cleared.

4) DMA mode can be implemented by setting the DMA enable bit in the control register and selecting high byte or low byte first by setting or clearing the LOBYT bit. The DBR pin is utilized as the DMA request, and will remain asserted until all data from the sequence is read.

5) DMA/Interrupt mode. DMA mode can also be used in non-DMA applications. Although this appears to be unconventional, it may actually be preferred over the interrupt mode because of its convenience and speed. One way to do this would be to use the DBR pin as an interrupt request but enable DMA mode in the DAP. When data is ready DBR interrupts the microprocessor. The microprocessor then reads either window register the required number of times to drain the Data RAM.

TABLE 1. CHANNELS IN AN ML2208 AT ARBITRARY TIMES

	LAST	ALRMEN	MODE	CHAN	CYCLE	GAIN	REF
SEQ0	0	0	Intra Sequence Pause	CH0	13	1	Internal
SEQI	0	0	Immed Execute	CHI	13	1	Internal
SEQ2	0	0	Immed Execute	CH2	13	I	Internal
SEQ3	0	0	Immed Execute	CH3	13	I	Internal
SEQ4	0	0	Immed Execute	CH4	13	I	Internal
SEQ5	0	0	Immed Execute	CH5	13	I	Internal
SEQ6	0	0	Immed Execute	CH6	13	I	Internal
SEQ7	I	0	Immed Execute	CH7	13	I	Internal

Using the DMA mode interrupt method over non-DMA mode interrupt method saves a lot of overhead. For example in non-DMA mode interrupt method (assuming AUTOI is set), the index register would have to be set on entry, and the DBRAK bit would have to be set each service routine. In DMA interrupt mode, neither the Index register nor the DBRAK bit would have to be set. These are handled automatically in DMA mode.

7.0 POWER-DOWN MODE

The chip can be powered-down by asserting the P_{DN} pin. It is advisable to place the chip in HALT mode first by clearing the RUN bit in the control register, however the chip will automatically go into Halt mode when powered-down. All analog circuits are powered-off; digital circuits are left in an idle state. All registers within the chip will retain their values down to a level of 2V between V_{CC} and GND.

Powering-up the chip is done by bringing P_{DN} high. The chip will be in Halt mode upon power-up. Note, however, that the first 10ms of chip operation after a power-up will not be valid due to the settling of quiescent bias conditions within the on-chip's analog circuits. Any data that is returned for this period after power-up should be considered invalid. The user has the choice of either throwing away the first 10ms of data or waiting for 10ms and then setting the chip in RUN mode. The on-chip timer can be used for this purpose, if desired, by defining a sequence of dummy operations that last for the required delay, then rewriting the required operations for normal use.

Acknowledge register. D_{BRAK} should also be set sometime before the next sequence to prevent the OVRN bit from being set, however this is not necessary.

Note that the microprocessor cannot let the ML2200 sequencer run continuously, i.e., SEQ 0 would be changed to Immediate Execute and asynchronously read the Data RAM. The problem in this case would be that the microprocessor may read the data at the same time that the chip is updating it. That is why either polling, interrupt, or DMA transfer is required in a continuous run mode of operation.

APPENDIX A

DIAGNOSTICS

The ML2200 and ML2208 may be run through a diagnostic routine after power-up. The DAP provides software programmable diagnostics so that no external hardware is necessary. Diagnostics are not necessary. They are provided as an option to the user.

SELF-TEST MODE

Setting the SLFTST bit in the Control register redefines the CHAN field in the Instruction Word. This in effect changes the input to the Sample-and-Hold from the multiplexer input channels to internal points within the chip; such as V_{REF} and AGND. Conversions in the Self-Test Mode allow the user to determine how the Sample-and-Hold and A/D converter behave with known input signals. This can be useful as a diagnostic routine for a product in the field, or as a debugging feature during product development. Figure 16 illustrates the redefinition of the instruction word when SLFTST= 1.

1. **System Offset** — The positive and negative inputs to the Sample-and-Hold are tied to analog ground. With this setting, converted data will give the offset of the A/D converter and Sample-and-Hold combination.
2. **Internal Reference** — Connects the positive input of the Sample-and-Hold to V_{REF} and the negative input of the Sample-and-Hold to analog ground. The result of converting in this test mode is a value near positive full scale.
3. **Invert Internal Reference** — Connects the negative input of the Sample-and-Hold to V_{REF} and the positive input of the Sample-and-Hold to analog ground. The result of converting in this test mode is a value near negative full scale.
4. **Common Mode** — Both the positive and negative inputs of the Sample-and-Hold are tied to the internal V_{REF}. The result of a conversion in this test mode indicates how well the converter is rejecting a common mode signal.

Since setting the SLFTST bit merely changes the input to the Sample-and-Hold, conversions must be executed in order to read the results. This means placing the chip in the RUN mode and reading the results from the Data RAM. It is possible to run one sequence then halt the sequencer and read the results. The sequencer can be put in a "pause" via the Intra Sequence Pause Mode instruction. The following instructions accomplish this:

	LAST	ALRMEN	MODE	CHAN	CYCLE	GAIN	REF
SEQ 0	0	0	Intra SEQ Pause	System Offset	13	1	0
SEQ 1	0	0	Immed Execute	INT REF	13	1	0
SEQ 2	0	0	Immed Execute	Minus INT REF	13	1	0
SEQ 3	1	0	Immed Execute	Common Mode	13	1	0

After the RUN bit is set, the ISQ bit in the status register is immediately set. Setting the ISQAK bit in the Interrupt Acknowledge register will allow the sequencer to continue. The next time the ISQ bit is set, the results may be read from the Data RAM.

Reading and Writing to the Calibration Register The ML2200 and ML2208 architecture provides a way for the microprocessor to indirectly read and write to the A/D converter; specifically the Calibration register and the A/D's Data register. Figure 18 illustrates this architecture.

The instructions that cause these transfers are READ CAL CODE and WRITE CAL CODE; selected in the Cycle field of the instruction word when SLFTST = 0. WRITE CAL CODE transfers the contents of the Calibration Holding register into the A/D converter's Calibration register. READ CAL CODE transfers the contents of the Calibration Holding register through the A/D's Data register, into the Data Output register with the same location as the operation.

As a result of providing READ and WRITE CAL, it is possible to execute digital loopbacks through the Calibration register, A/D registers, and all 8 Data Output registers. These loopbacks provides user assurance that all of the paths are clear and there are no stuck bits.

Writing to the Calibration register changes the calibration of the A/D converter. Therefore a self calibration should be performed after executing a WRITE CAL CODE to ensure the A/D is properly calibrated.

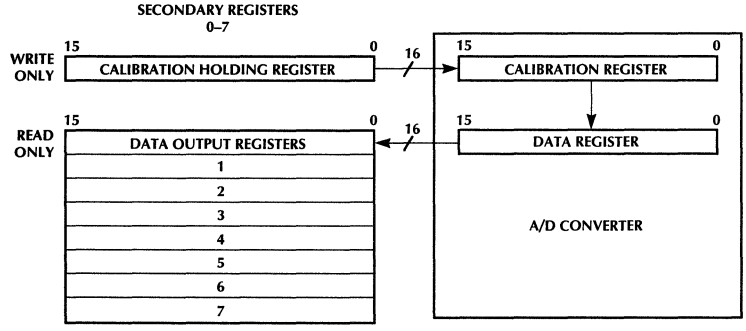


Figure 18. Digital Loopback Architecture.

DIGITAL LOOPBACK ARCHITECTURE

Reading the calibration register provides a way for the microprocessor to determine that the self calibration was successful. The microprocessor configures the DAP to execute a READ CAL CODE after a self calibration has been performed. If the lower byte of data from the READ CAL CODE is anything other than all 1s, then the calibration was successful.

Even though the calibration register itself is a 16-bit register, and is capable of holding a 16-bit result, only the lower 9 bits are significant in determining the calibration code. These 9 bits have a sign magnitude format, in other words the 9th bit (MSB of the 9-bit word) is the sign bit, and the other eight bits are magnitude bits. An easy way to determine whether the calibration has passed or failed is to read the lower data byte after a READ CAL is executed. If it's not all 1s then the calibration was a success.

APPLICATIONS

Utilizing instruction RAM bits 0, 1, and 2, any of the differential input channels of the ML2200 can be programmed to sense the external reference (See Figure 13.) Only single ended channels 0 thru 5 can be used on the ML2208 (See Figure 14.)

Figure 19. Using a 2.5V External Reference.

The system gain errors can be nulled by applying 2.4991 V (the full-scale voltage minus 1.5LSB) to one of the input channels and adjusting R1 until the digital output toggles between 01111 1111 1110 and 01111 1111 1111. If offset is not adjusted the full-scale voltage will be shifted by the amount of this unadjusted offset voltage.

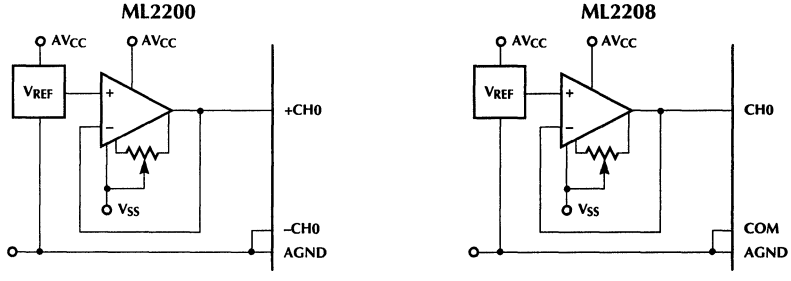


Figure 20. Adjusting Full-Scale Error.

APPLICATIONS (Continued)

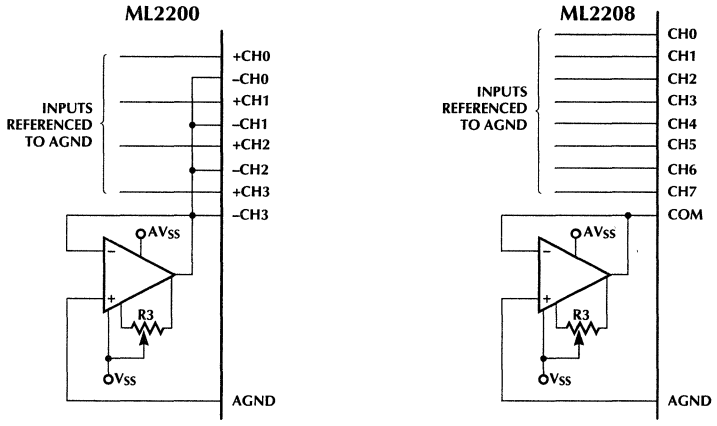


Figure 21. Adjusting Zero Error.

An op amp with an offset adjustment with a range of at least + 1.3 mV is required, like an OP – 27. The Zero Error can be nulled by first applying 305µV to one of the input channels (referenced to AGND.) 305µV is equivalent to ½ LSB which is the ideal input voltage which should cause the digital output to toggle from 0 0000 0000 0000 to 0 0000 0000 0001. Adjust R3 until this occurs.

If an external reference is also being used, it should be referenced to AGND, while the COM or negative inputs are tied to the offset op amp as shown above. In this configuration, the offset adjustment will effect the gain setting and so should be set first.

The Channel to Channel Zero Error and Full-Scale Error are very low and do not need to be adjusted separately. If, however, the input signal sources have their own different offsets, a separate op amp, with an offset adjustment, can be placed at each channel input.

APPLICATIONS (Continued)

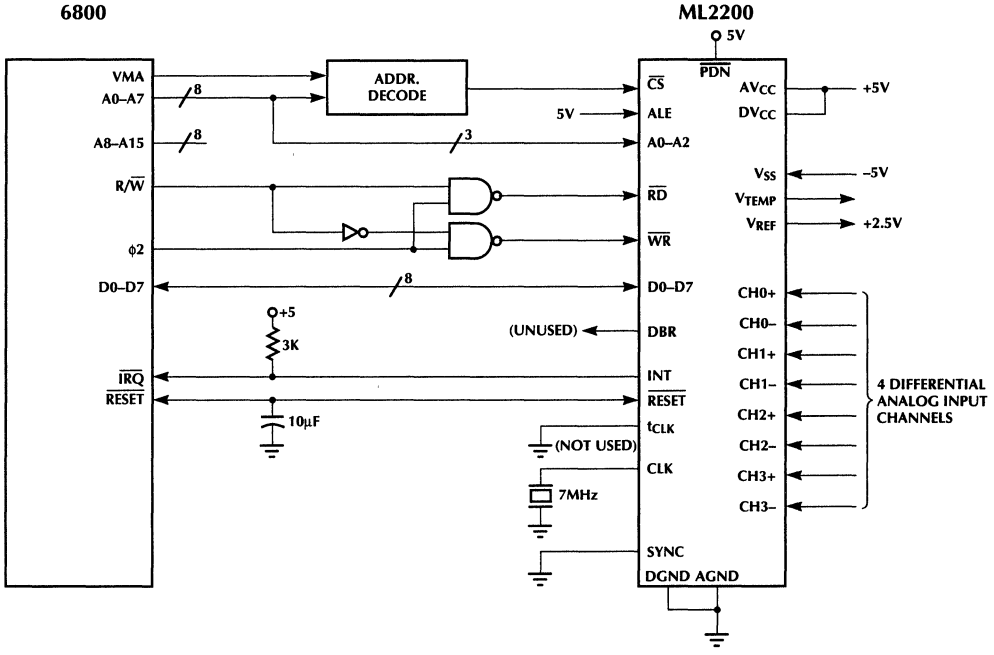


Figure 22. Interfacing ML2200 to 6800 Type Microprocessors.

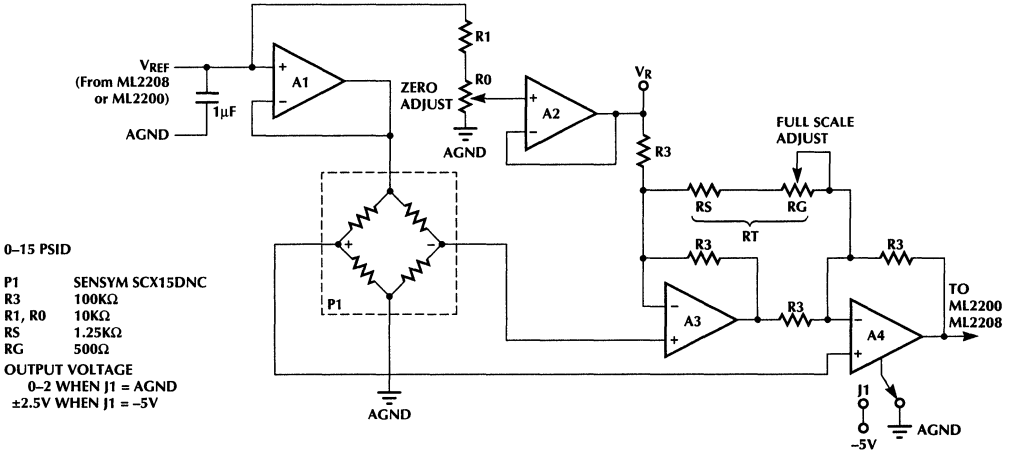


Figure 23. Pressure Sensor Application.

ORDERING INFORMATION

PART NUMBER	LINEARITY ERROR	MINIMUM CONVERSION	PACKAGE	TEMPERATURE RANGE
Four Differential Analog Inputs				
ML2200BCP	±3/4 LSB	31.5µs	Plastic DIP (P40)	0°C to +70°C
ML2200CCP	±1 LSB	31.5µs		
ML2200DCP	± LSB	44.0µs		
Eight Single Ended Analog Inputs				
ML2208BCP	±3/4 LSB	31.5µs	Plastic DIP (P40)	0°C to +70°C
ML2208CCP	±1 LSB	31.5µs		

Micro Linear

ML2221

Serial Peripheral Interface (SPI) 12-Bit Plus Sign A/D Converter with S/H

GENERAL DESCRIPTION

The ML2221 is a member of Micro Linear's 12-bit plus sign CMOS A/D converter family utilizing a self calibrating algorithmic SAR technique. All errors of the sample-and-hold are accounted for in the analog-to-digital converter's accuracy specification.

These A/D converters have a maximum nonlinearity error over temperature of ±0.009% or ±0.012% of minus full scale to plus full scale.

The serial interface is compatible with industry standard serial interfaces. The ML2221 has 4 modes of operation: gated serial data clock, gated chip select, chip select to initiate conversion with serial out data controlled by ML2221, and free run mode.

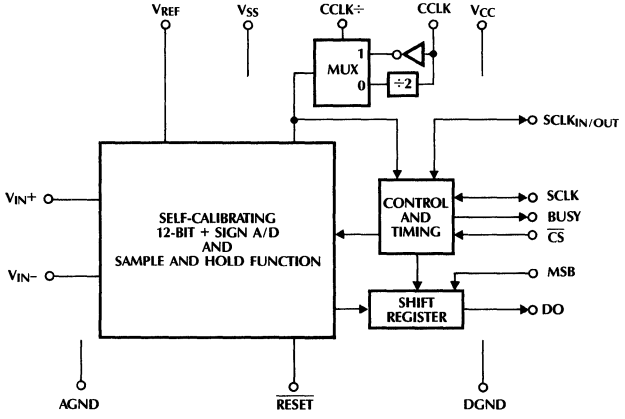
The serial interface allows either MSB or LSB first data with 2's complement output coding. For easy interface to microprocessors and shift registers the output data word is 16 bits.

FEATURES

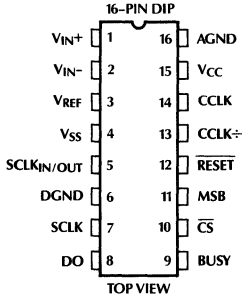
- Nonlinearity error ±¾ LSB and ±1 LSB max
- Conversion time (including S/H acquisition) 44μs max
- Harmonic distortion 0.01%
- No missing codes
- Inputs withstand |7V| beyond supplies
- Bipolar –5V to +5V analog input range
- Controlled or free run operation
- Direct 4-wire interface to μP (MPU) with synchronous serial formats
- 0°C to +70°C, –40°C to +85°C temperature range
- 16-pin DIP

2

BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	$V_{IN}+$	Positive Differential Analog Input; range = $V_{SS} \leq V_{IN}+ \leq V_{CC}$, $\lvert(V_{IN}+) - (V_{IN}-)\rvert \leq V_{REF}$.
2	$V_{IN}-$	Negative Differential Analog Input; range = $V_{SS} \leq V_{IN}- \leq V_{CC}$, $\lvert(V_{IN}+) - (V_{IN}-)\rvert \leq V_{REF}$.
3	V_{REF}	Voltage Reference Input; referenced to analog ground.
4	V_{SS}	Negative Supply -5V ± 5%; decouple to AGND.
5	$SCLK_{IN/OUT}$	SCLK mode select $SCLK_{IN/OUT}$ = 5V; SCLK is an input serial CLK. $SCLK_{IN/OUT}$ = 0V; SCLK is an output serial CLK.
6	DGND	Digital Ground.
7	SCLK	Bi-Directional Serial Data Clock. Serial data is transmitted by the clock present at SCLK.
8	DO	Data Out. Digital output which contains result of A/D conversion. The serial data is clocked out on falling edges of SCLK.
9	BUSY	Three-state active high BUSY status output. Normally low. Goes high to indicate that a conversion is in progress; de-asserted when conversion is complete and data is available from the conversion just completed. A pulldown resistor is recommended on this pin.
10	$\overline{CS}$	Active Low Chip Select, starts a conversion and brings the BUSY and DO out of the three-state mode. $\overline{CS}$ is used in modes where conversion or transmission timing is controlled; held low in gated SCLK and FREERUN modes.
11	MSB	Most Significant Bit is transmitted first if MSB is tied to V_{CC}; Least Significant Bit transmitted first if MSB is tied to DGND.
12	$\overline{RESET}$	Active Low Reset. The RESET period is set by the time constant of the internal 50K pull up resistor and an external capacitor. After the RESET period the converter will be ready for accepting requests or will automatically start conversions/transmissions based upon the mode.
13	CCLK÷	Sets CCLK equal to internal clock if tied to 5V. If tied to 0V the internal clock equals CCLK/2. With CCLK equal to the internal CLK the user can synchronize to all internal timing events, although CCLK duty cycle must be controlled to meet the minimum clock high and low times specified.
14	CCLK	Clock Input. Internal clock can be generated by tying a crystal from this pin to DGND or applying a clock directly to the pin.
15	V_{CC}	Positive Supply. +5V ± 5% decouple to AGND.
16	AGND	Analog Ground 0 Volts. Common mode reference point of the internal differential circuitry.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage (V_{CC}) 6.0V
Negative Supply Voltage (V_{SS}) ..... -6.0V
Voltage at Analog Inputs ..... V_{SS} - 7V to V_{CC} + 7V
Voltage at V_{REF} ..... V_{SS} - 7V to V_{CC} + 7V
Input Current per Digital Pin ..... ±10mA
Input Current at Analog Inputs ..... ±20mA
Storage Temperature Range ..... -65°C to +150°C
Package Dissipation at 25°C (Board Mount) 875mW
Lead Temperature (soldering 10 seconds)
Dual-In-Line Package (Molded) ..... 260°C
Dual-In-Line Package (Ceramic) ..... 300°C

OPERATING CONDITIONS
(Note 2)

Temperature Range ..... $T_{MIN} \leq T_A \leq T_{MAX}$
ML2221BIJ, ML2221CIJ ..... -40°C to +85°C
ML2221BCP, ML2221CCP ..... 0°C to +70°C
Supply Voltage (V_{CC}) ..... $4.5V_{DC}$ to $6.0V_{DC}$
Negative Supply Voltage (V_{SS}) ..... $-4.5V_{DC}$ to $-6.0V_{DC}$
Reference Voltage (V_{REF}) ..... V_{CC}

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC} = +5V ± 5%, V_{SS} = -5V ± 5%, V_{REF} = +4.75V, $V_{IN}-$ = AGND, $V_{IN}+$ = -4.75V to +4.75V, T_A = T_{MIN} to T_{MAX} unless otherwise specified.

			ML2221BIJ, ML2221CIJ			ML2221BCP, ML2221CCP			
PARAMETER	NOTES	CONDITIONS	MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX	UNITS
Converter Characteristics									
Linearity Error ML2221BXX ML2221CXX	4	f_{CCLK} = 0.1 to 5MHz			±¾ ±1			±¾ ±1	LSB LSB
Unadjusted Zero Error ML2221BXX ML2221CXX	4				±¾ ±2			±¾ ±2	LSB LSB
Unadjusted Positive and Negative Full-Scale Error	4				±5			±4	LSB
Zero Error Temperature Coefficient				0.5			0.5		ppmFS/°C
Gain Temperature Coefficient				10			10		ppmFS/°C
Common Mode Rejection	5, 6		80			80			dB
Analog Input Source Resistance	4				2			2	kΩ
Analog Input Range	4	$V_{IN}+$ Referred to $V_{IN}-$	$-V_{REF}$		$+V_{REF}$	$-V_{REF}$		$+V_{REF}$	V
Analog Input Leakage Current	4				100			100	nA
Voltage Reference Input Source Impedance	4				0.5			0.5	kΩ
Reference Input Leakage Current	4				100			100	nA
Digital and DC Characteristics									
Power Supply Current I_{CC}, V_{CC} I_{SS}, V_{SS}	4			30 18	50 30		30 18	50 30	mA mA
Power Supply Rejection V_{CC} V_{SS} 	7	 DC DC to 25kHz DC DC to 25kHz		 80 50 80 50			 80 50 80 50		 dB dB dB dB
V_{ILCLK}, Clock Input Low Voltage	4				0.8			0.8	V
V_{IHCLK}, Clock Input High Voltage	4		3.5		V_{CC}	3.5		V_{CC}	V
I_{L1}, Input Leakage Current (CCLK)	4	AGND ≤ V_{IN} ≤ V_{CC}			±200			±200	μA
V_{IL}, Input Low Voltage	4				0.8			0.8	V
V_{IH}, Input High Voltage	4		2.0		V_{CC}	2.0		V_{CC}	V
V_{OL}, Output Low Voltage	4	I_{OL} = 2.0mA			0.45			0.45	V
V_{OH}, Output High Voltage	4	I_{OH} = -400μA	2.4			2.4			V
I_L, Input Leakage Current (except CCLK)	4	DGND ≤ V_{IN} ≤ V_{CC}			±10			±10	μA
I_{HI-Z}, Output Leakage Current	4	$\overline{CS}$ ≥ V_{IH}			±10			±10	μA
C_I, Input Capacitance (all digital inputs)	5			10			10		pF
C_O, Output Capacitance (all digital outputs)	5			10			10		pF

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	NOTES	CONDITIONS		MIN	TYP (Note 3)	MAX	UNITS
AC Electrical Characteristics (Note 8)								
t_C	Conversion Time	4, 9	f_{CCLK} = 5MHz (CCLK÷ = "0")		44			μs
	Sample and Hold Acquisition	4, 9	f_{CCLK} = 5MHz (CCLK÷ = "0")		3.2			μs
f_{CCLK0}	Clock Frequency	5, 9	Crystal (CCLK÷ = "0")		3		5	MHz
			Driven (CCLK÷ = "0")		0.1		5	MHz
f_{CCLK}	Clock Duty Cycle	5, 9	Driven		40		60	%
f_{CCLK0}	Clock Width	5, 9	Driven (CCLK÷ = "0")	High	50			ns
				Low	50			ns
f_{CCLK1}	Clock Frequency	5,9	Driven (CCLK÷ = "1")		0.05		2.5	MHz
f_{CCLK1}	Clock Width	5	Driven (CCLK÷ = "1")	High	150			ns
				Low	150			ns
t_{CSB}	$\overline{CS}$ Low to BUSY Driven	4					85	ns
$t_{CSB}HZ$	$\overline{CS}$ High to BUSY, Hi-Z	4					85	ns
$t_{SCLKB}A$	SCLK High to BUSY	5	Gated SCLK				270	ns
$t_{CCLKB}D$	CCLK Low to BUSY, Deassert	5					160	ns
$t_{SCLK, DO}$	Serial Clock Low to DO Valid/Hold	4					190	ns
$t_{CS, DO}$	$\overline{CS}$ Low to DO Driven	4					85	ns
$t_{CS, DO}HZ$	$\overline{CS}$ High to DO Hi-Z	4					85	ns
$t_{CS, CCLK}$	$\overline{CS}$ Low Setup Time to CCLK	4	Immediate Conversion Start		0			ns
$t_{CS, SCLK}$	$\overline{CS}$ Low Setup to SCLK Low for No-Delay Data Transmit	5					75	ns
$t_{CCLK, SCLK}$	CCLK to SCLK Output Delay	5	$SCLK_{IN/OUT}$ = "0"				225	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: 0°C to +70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 6: Common mode rejection is the ratio of the change in zero error to the change in common mode input voltage.

Note 7: Power supply rejection is the ratio of the change in zero error to the change in power supply voltage.

Note 8: All parameters measured from 0.8V to 2.0V, C_L = 50pF.

Note 9: Maximum frequency is $1/t_{CLK1}$ (high) + t_{CLK1} (low) + rise + fall times, which must be ≤ 2.5 MHz.

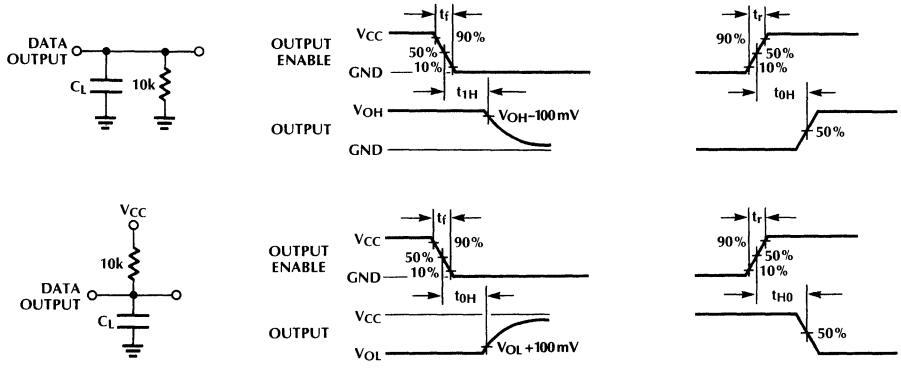


Figure 1. High Impedance Test Circuits and Waveforms

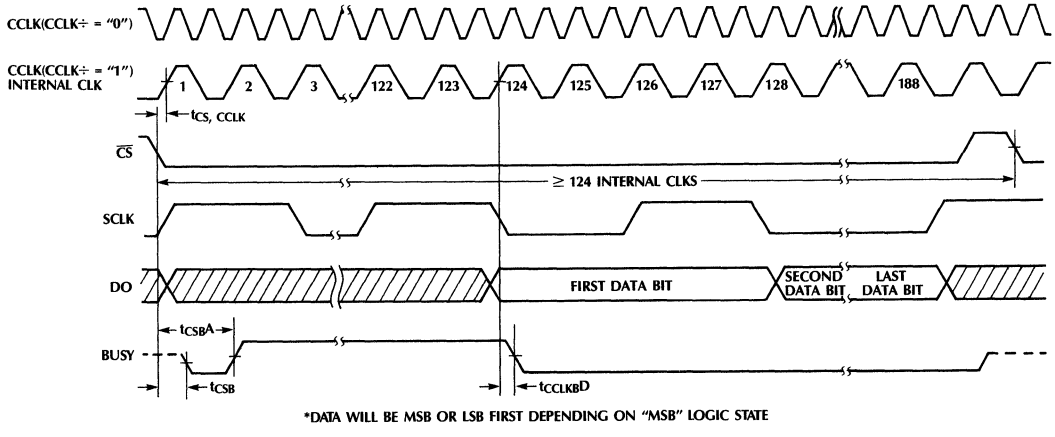


Figure 2. $\overline{CS}$, SCLK Sourced Mode

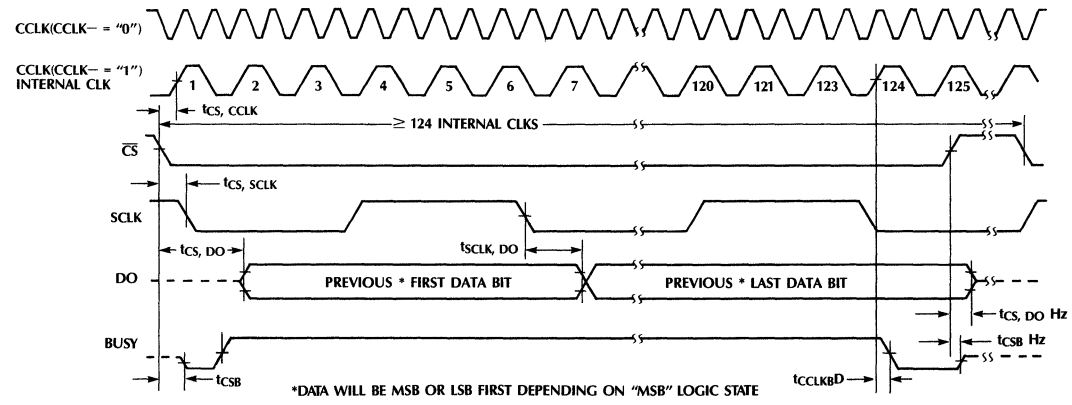


Figure 3. $\overline{CS}$, SCLK External Mode

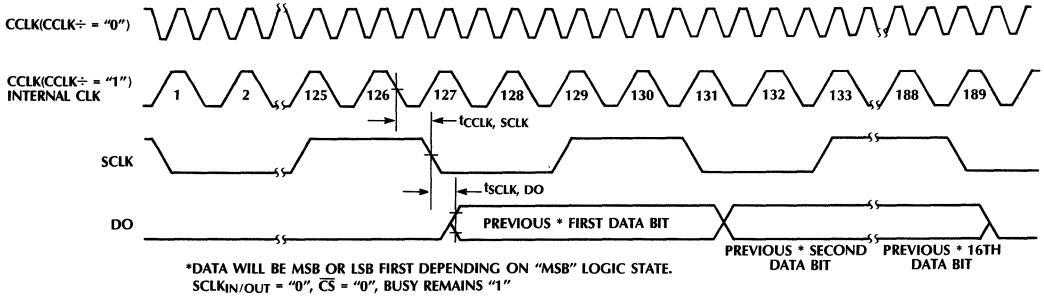


Figure 4. FREERUN Mode

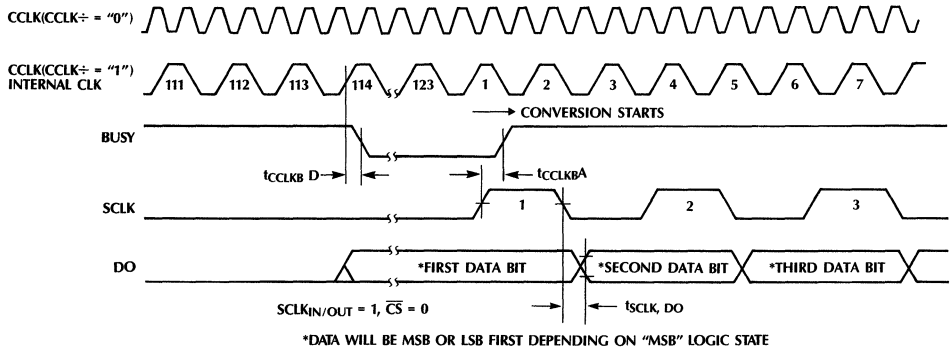


Figure 5. Gated SCLK Mode

1.0 FUNCTIONAL DESCRIPTION

1.1 ALGORITHMIC A/D CONVERTER

Micro Linear's algorithmic converter uses a successive approximation technique. Most of today's successive approximation converters use a DAC to feedback the approximated signal, however this technique requires more circuitry than algorithmic converters. In addition the values of all of the resistors or capacitors in the DAC must be matched to within the accuracy of the converter. This is difficult beyond 10 bits unless trimming is used. An algorithmic converter uses less circuitry and is more easily trimmed. Micro Linear's algorithmic converter is implemented using a 2x amplifier, a sample/hold amplifier and a comparator as shown in Figure 6.

The input sample is first multiplied by two then compared to the reference voltage. If the 2x input voltage is greater than the reference, the MSB is a 1 and the reference voltage is subtracted from the 2x input voltage. The remainder is stored in the sample and hold. If the 2x input voltage is less than the reference, the MSB is a 0 and the 2x input voltage is stored in the sample and hold. This process repeats again, however now the sample and hold voltage is multiplied by 2.

The algorithm involves multiplication by 2, comparison, and possibly subtraction. Referring to Figure 6, the algorithm for the circuit can be described as follows:

Step 1 If $(2 \times V_{IN}) - V_{REF} \geq 0$
then MSB = 1
$(2 \times V_{IN}) - V_{REF} \rightarrow S/H$
else MSB = 0
$(2 \times V_{IN}) \rightarrow S/H$

Step 2 If $(2 \times S/H) - V_{REF} \geq 0$
then next bit = 1
$(2 \times S/H) - V_{REF} \rightarrow S/H$
else next bit = 0
$(2 \times S/H) \rightarrow S/H$

Step 3 Repeat Step 2 until conversion complete.

Since the A/D converter handles bipolar inputs, negative inputs are handled slightly differently using the same principle.

1.1.1 Self Calibration

In order to maintain integral and differential linearity in an algorithmic converter, two critical parameters need to be controlled, loop offsets and the gain of the loop. Loop offsets are automatically nulled before each conversion using auto-zeroing circuitry on both the sampling amplifier and the 2x amplifier. The gain of the loop is adjusted using self calibration.

Self calibrating the algorithmic converter, once the offsets have been nulled, is performed by measuring the 2x gain of the loop and adjusting it. The gain can be measured by converting the reference voltage at the input as well as the reference (V_{REF}/V_{REF}), and examining the output code. Converting V_{REF} should yield plus full scale, since V_{REF}/V_{REF} should equal 1. If the gain of the loop is slightly less than 2, the resulting LSB of the conversion will be "0". If the magnitude bits of the resulting conversion are all "1s", the gain may be too great, therefore the gain is reduced to the point where the threshold of the LSB is reached.

Adjustment of the 2x gain is done with the binary weighted trim capacitor arrays connected to each of the 2C input capacitors. A small value of capacitance is either added to or subtracted from the 2C input caps until the gain of the loop is within 13-bit accuracy.

Self calibration is done at the factory. The calibration process is not available at the finished product level.

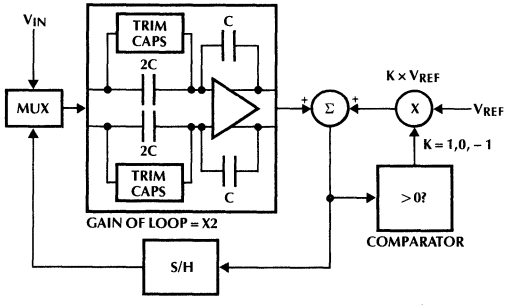


Figure 6. Self Calibrating A/D Converter

1.1.2 Conversion Times

The following table lists the conversion times which include the sample and hold acquisition time.

OPERATION MODE	INTERNAL CLOCKS*
$\overline{CS}$, SCLK External	124
$\overline{CS}$, SCLK Sourced	124
FREERUN	110
Gated SCLK	124

1.1.3 Sample and Hold Timing

Figure 7 shows the internal timing for the sample and hold circuitry. The relationship between the start of conversion and the input channel going into sample mode is fixed at 6 internal clocks*, regardless of the start mode. Six internal clocks after the start of conversion the sample and hold is switched into the sample mode, placing two 9pF capacitors in parallel with the input pins; one on $V_{IN}+$ and one on $V_{IN}-$. The sample switch is kept in the sample mode for 8 internal clocks (3.2μs at a 5MHz external clock, if CLK÷ = 0), then placed in the hold mode. During the next 2 internal clocks the charge on the sample and hold is transferred into the A/D, after which the V_{REF} pin is sampled for 8 internal clocks.

1.2 ANALOG INPUTS

1.2.1 Differential Inputs and Common Mode Rejection

The differential inputs of the ML2221 eliminate the effects of common mode input noise (60Hz for example), as $V_{IN}+$ and $V_{IN}-$ are sampled at the same time.

* For a description of internal clocks see Clock section.

1.2.2 Noise

The leads to the analog inputs should be kept as short as possible to minimize input noise. Noise as well as digital clocks can couple into the inputs and cause errors. Input filters can be used to reduce the effects of these sources.

1.2.3 Power Supply Decoupling

Low inductance tantalum capacitors of 1μF or greater and 0.01μF disc ceramic capacitors are recommended for bypassing V_{CC} as well as V_{SS} to AGND. These capacitors should be placed close to the V_{CC} and V_{SS} pins.

1.3 CONVERTER CLOCK

The CCLK input can be driven with an external clock or a crystal referenced to DGND. The crystal must be parallel resonant with minimum capacitive loading. (i.e., no bypass caps should be used and leads should be kept short)

If driven with external clock and if the CCLK÷ pin is tied to V_{CC}, the frequency must be between 50KHz to 2.5MHz with the requirement that clock LOW (t_{CCLKL}) and clock HIGH (t_{CCLKH}) durations must be more than 150ns. If the CCLK÷ pin is tied to ground then the frequency can be from 100KHz to 5.0MHz.

For crystal operation with the divide by two flip flop bypassed, and there is a 30 to 70% variation in duty cycle of the oscillator, the maximum crystal frequency is 2.0MHz to insure that the minimum clock high and low times are greater than 150 nsec.

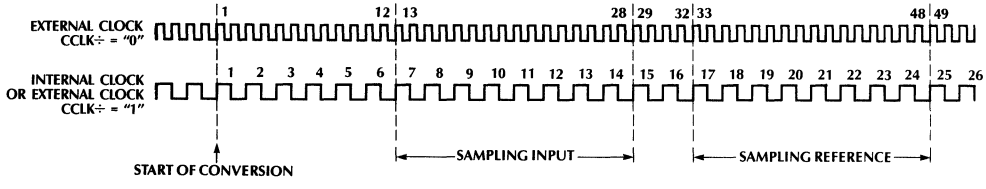


Figure 7. Sample and Hold Timing

1.4 RESET

The $\overline{\text{RESET}}$ pin has an internal 100K pullup resistor. Power supplies must be stable to within a ±5% tolerance before the reset condition is removed.

The active low hardware reset can be performed by a capacitor value (usually >6μF) tied to the $\overline{\text{RESET}}$ pin or by driving it with the system reset signal.

1.5 DIGITAL INTERFACE

All four synchronous interface modes of operation are determined by $\overline{\text{CS}}$ during reset period as follows:

Logic Level of $\overline{\text{CS}}$ During Reset	SCLK Mode Select ($SCLK_{IN/OUT}$)	Serial Interface Mode
0	0	FREERUN
0	1	Gated SCLK
1	0	$\overline{\text{CS}}$, SCLK Sourced
1	1	$\overline{\text{CS}}$, SCLK External

After the reset time, the $SCLK_{IN/OUT}$ pin can be changed to switch between either (FREERUN and Gated SCLK) or ($\overline{\text{CS}}$, SCLK Sourced and $\overline{\text{CS}}$, SCLK External).

The logic level of $\overline{\text{CS}}$ will not change the mode of operation of the ML2221 once the mode of operation is programmed during the RESET period.

1.5.1 $\overline{\text{CS}}$, SCLK External Mode

$\overline{\text{CS}}$ starts a conversion. The SCLK is continuously driven into the ML2221 and data from the previous conversion is shifted out at the SCLK rate starting at the first SCLK falling edge from the $\overline{\text{CS}}$ assertion. $\overline{\text{CS}}$ is normally kept low for all 16 bits of data, but can be brought back high after the desired number of bits have been shifted out. $\overline{\text{CS}}$ should be held low for a minimum of 124 internal clocks (see Figure 8) for the conversion to complete.

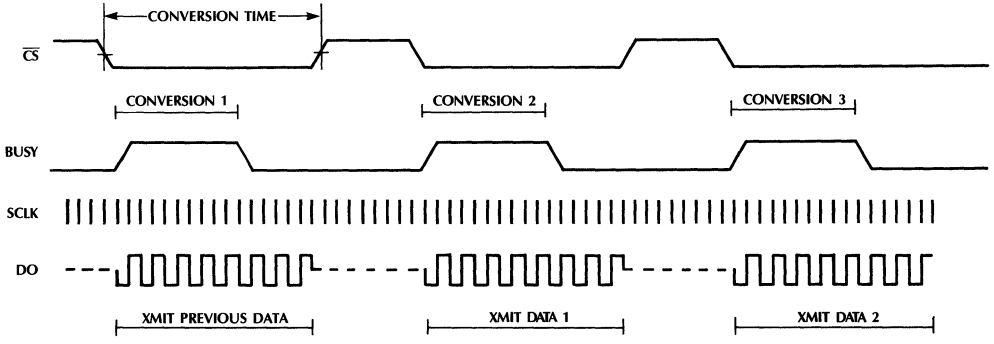
It takes 110 internal clocks to convert an analog signal into 13 bits of data plus 13 more clock periods to make data available. At a 5.0MHz clock and CCLK÷ = 0V, the maximum conversion rate is 49.6 microseconds or 124 internal converter clocks.

When $\overline{\text{CS}}$ is asserted (LOW) a conversion begins and the DO output becomes active. The ML2221 is ready to shift out the data serially.

The BUSY output is in the high impedance state when the ML2221 is not selected. When $\overline{\text{CS}}$ input goes low, the BUSY output is driven high or low depending on if a conversion is in progress. Once a conversion begins, BUSY is held active for 123 internal converter clocks.

The DO output is high impedance when the ML2221 is not selected. When $\overline{\text{CS}}$ input goes low, it is driven with the first bit of data initially, and then begins to put out all subsequent data bits on each FALLING edges of the serial clock (SCLK). Data is always output in 16 bit format: if the LSB is output first, the data is sign extended after 13 bits; if the MSB is output first, the data is zero-filled after 13 bits. DO remains driven as long as $\overline{\text{CS}}$ remains low.

a. Serial Transmission < Conversion Time



NOTE: CONVERSION TIME EQUALS 124 INTERNAL CLOCK OR CCLK'S IF CCLK÷ = "1"

Notes:
1. Use 10k pulldown resistor on BUSY pin to get "true" convert busy.
2. If $\overline{\text{CS}}$ is brought high in the middle of a serial data transmission, the data transmission is aborted and the data is reloaded into the output shifter.

Figure 8. $\overline{\text{CS}}$, SCLK External Mode

1.5.2 $\overline{CS}$, SCLK Sourced Mode

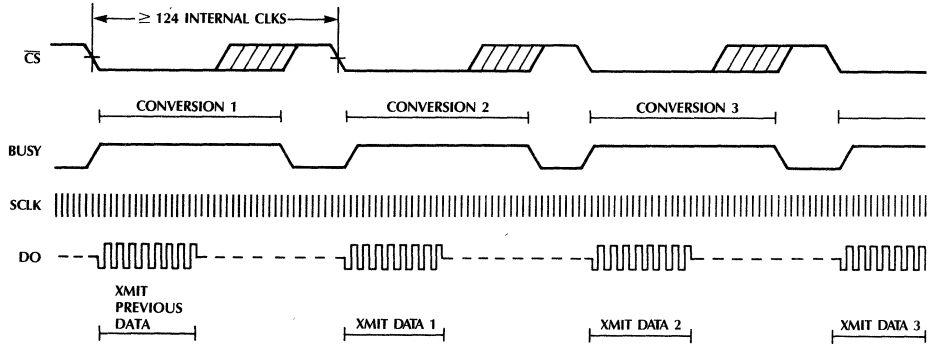
Conversion is initiated by $\overline{CS}$. In this mode, SCLK is sourced by the ML2221. At the end of the conversion, the device will provide a packet of 16 SCLKs to transmit the 16 bits data stream (see Figure 9). The data rate at which the data is being transmitted is (internal clock)/4. For example, when CCLK÷ = 1, CCLK = 256kHz, the data rate is 64Kbps.

$\overline{CS}$ should be held low during the entire conversion and the transmission sequence. The time required to convert an analog signal is 110 clocks, with additional 13 clocks to shift out the data. The total conversion time is therefore 123 clocks plus one bit delay. Data transmission will need 64 (16-bit x 4) internal clocks. Hence, the total clock cycles to complete one operation in this mode is 188 clocks. $\overline{CS}$ therefore should be held low for a minimum of 188 clocks.

Example: If CCLK = 5 Mhz, CCLK÷ = 0, the maximum conversion time will be 75.2μs. Therefore, the maximum frequency for $\overline{CS}$ is 13.3kHz.

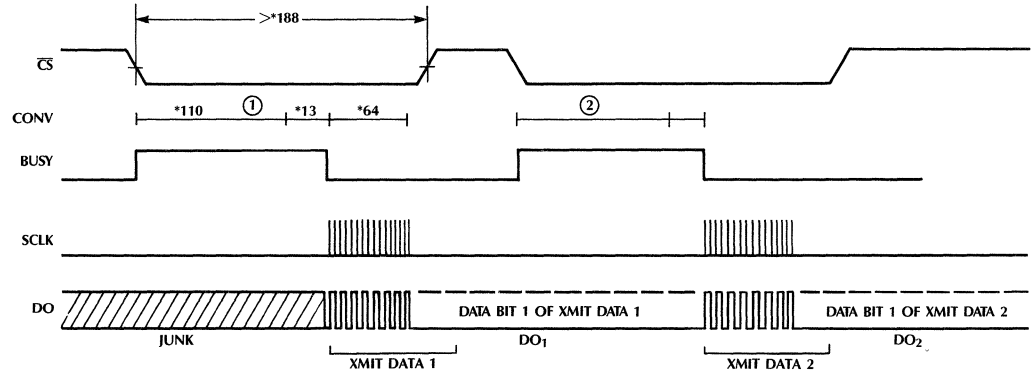
In this mode, the data transmitted is always the current data.

b. Serial Transmission > Conversion Time



Notes:
1. Use 10K pulldown resistor on BUSY pin to get "TRUE" convert BUSY status.
2. If $\overline{CS}$ is brought HIGH in the middle of a serial data transmission, the data transmission is aborted and the data is reloaded into the output shifter.

Figure 8. $\overline{CS}$, SCLK External Mode



*NUMBER OF INTERNAL CONVERTER CLOCKS OR C CLKS WITH C CLK÷ = "1"

Notes:
1. Use 10K pulldown resistor on BUSY pin to get "TRUE" convert BUSY status.
2. If $\overline{CS}$ is brought HIGH in the middle of a serial data transmission, the data transmission is aborted and the data is reloaded into the output shifter.

Figure 9. $\overline{CS}$, SCLK Sourced Mode

1.5.3 FREERUN Mode

The FREERUN mode executes continuous back-to-back conversions at the rate of 110 internal converter clocks per conversion, and outputs 16 bits of data and 16 corresponding SCLKS at the rate of 4 internal converter clocks per bit (see Figure 10). The ML2221 immediately begins converting after reset and starts outputting data after the first conversion. A conversion rate of 44 microseconds can be achieved by using the maximum CCLK frequency.

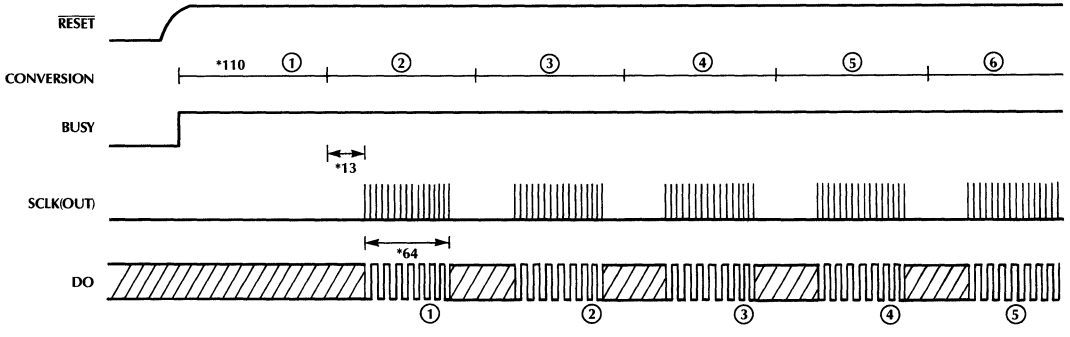
In the FREERUN mode, SCLK can not be sourced externally. The SCLK provided internally by the device is equal to (internal clock)/4. Since the converter is performing continuous conversion, BUSY is therefore always asserted.

1.5.4 Gated SCLK Mode

In this mode of operation, an external SCLK source must be used. This external SCLK should be a 16 clock packet which will be used by the converter to send out the data and initiate the conversion simultaneously (see Figure 11).

The data transmitted by ML2221 is the data from the previous conversion (see Figure 11). Therefore, in order to ensure integrity of the first data byte, the first SCLK signal should be initiated after a minimum of 124 internal clocks after reset. After the reception of the first SCLK signal, the converter will start the conversion process which is 124 clock as mentioned. Therefore the minimum time required between initiation of conversion by the SCLK should be no less than 124 clocks. In the case of maximum CCLK at 5MHz, the miniumum time interval between two packets of SCLK should be 49.6μs.

The BUSY output never floats and is asserted at the first SCLK and deasserted after 123 internal converter clocks. DO is always driven.

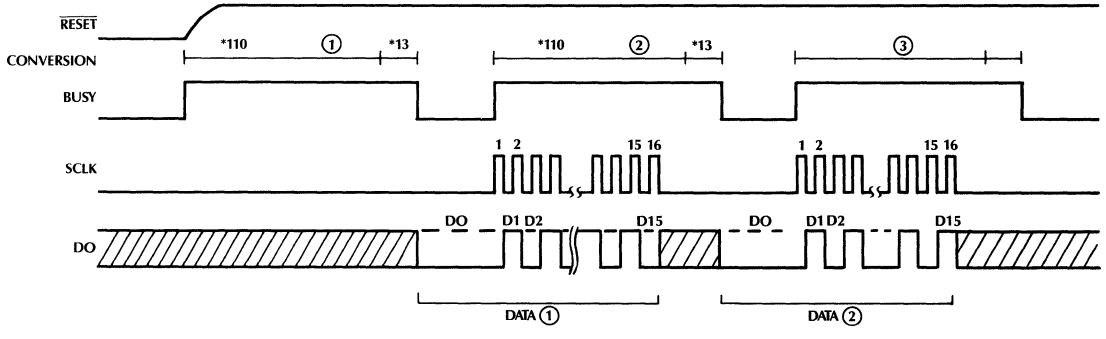


*NUMBER OF INTERNAL CONVERTER CLOCKS OR CCLKS WITH CCLK÷ = "1"

Note: DO is always driven.

Figure 10. FREERUN Mode

a. Serial Data Transmission < Conversion Time



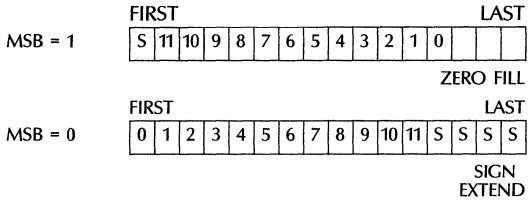
*NUMBER OF INTERNAL CONVERTER CLOCKS OR CCLKS WITH CCLK÷ = "1"

Note: Time from first SCLK↑ to seventeenth SCLK↑ must be greater than 124 internal converter clocks.

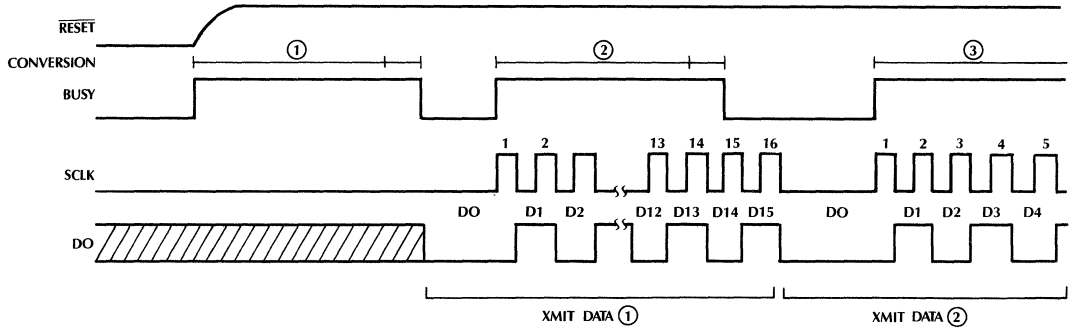
Figure 11. Gated SCLK Mode

1.6 DATA FORMAT

The MSB pin determines if the MSB or LSB data is transmitted first and in the following format. If more than 13 SCLK's occur.



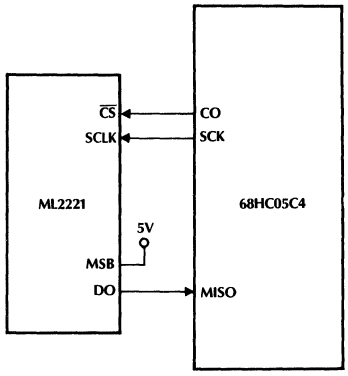
b. Serial Data Transmission > Conversion Time



Note: Time from first SCLK↑ to seventeenth SCLK↑ must be greater than 124 internal converter clocks.

Figure 11. Gated SCLK Mode

APPLICATIONS



START	MNEMONIC	INSTRUCTION
START	BCLRn	Bit 0 Port C goes low ($\overline{CS}$ goes low)
	LDA	Load contents of SPI data register into Acc. (D_{OUT} MSBs)
	STA	Start next SPI cycle
	AND	Clear 3 MSBs of first D_{OUT} word
	STA	Store in memory location A (MSBs)
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	BSETn	Set B0 of Port C ($\overline{CS}$ goes high)
	LDA	Load contents of SPI data register into Acc. (D_{OUT} LSBs)
	STA	Store in memory location A + 1 (LSBs)

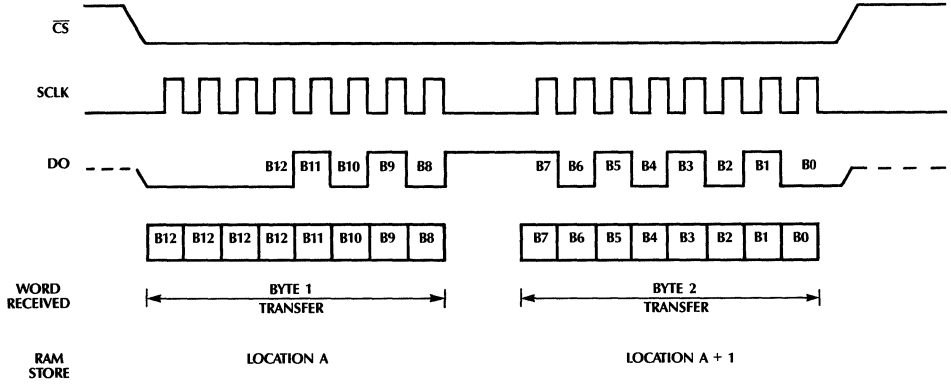


Figure 12. Interfacing to 68HC05C4 with a Dedicated Serial Port

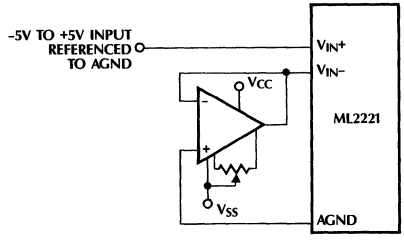


Figure 13. Adjusting Zero Error

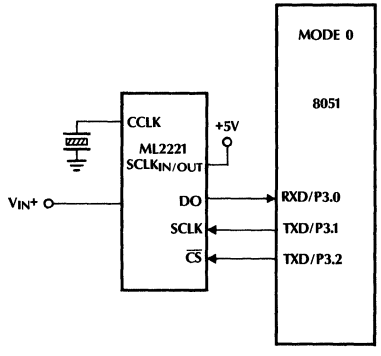


Figure 14. 1 Mbps 8051 Interface

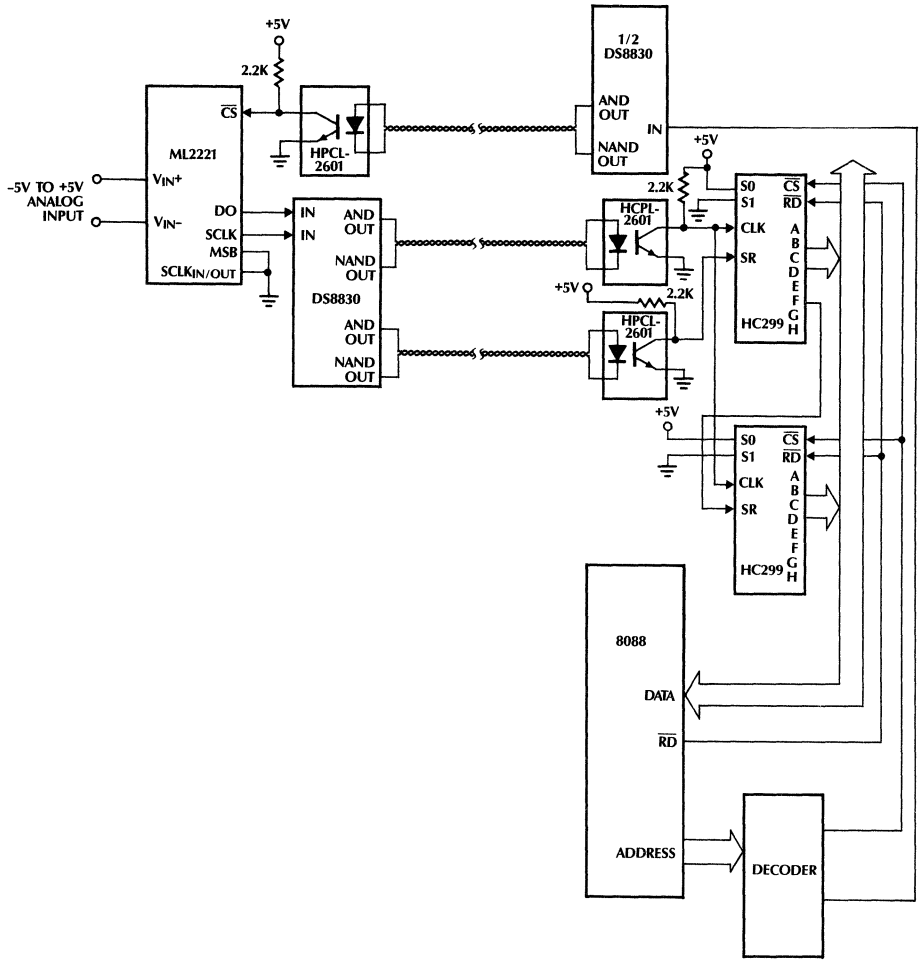


Figure 15. Optical Isolated 8088 Interface

ORDERING INFORMATION

PART NUMBER	LINEARITY ERROR	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
ML2221BCP	±¾ LSB	±1½	0°C to +70°C	MOLDED DIP (P16)
ML2221BIJ			-40°C to +85°C	HERMETIC DIP (J16)
ML2221CCP	±1 LSB	±2½	0°C to +70°C	MOLDED DIP (P16)
ML2221CIJ			-40°C to +85°C	HERMETIC DIP (J16)

Asynchronous Serial Interface 12-Bit Plus Sign A/D Converter with S/H

GENERAL DESCRIPTION

The ML2223 is a member of Micro Linear's 12-bit plus sign CMOS A/D converter family utilizing a self calibrating algorithmic SAR technique. All errors of the sample-and-hold are accounted for in the analog-to-digital converter's accuracy specification.

These A/D converters have a maximum nonlinearity error over temperature of ±0.009% or ±0.012% of full scale.

For easy interface to microprocessors, the ML2223 is designed to transmit data into RS-232 type ports.

The ML2223 operates in an asynchronous mode of operation. In this mode, the A/D continuously transmits 2 bytes in a 24-bit stream, inserting 8 idle bits between transmissions. When $\overline{\text{CURR}}$ input pin is tied high, transmission of the previous data begins immediately upon receiving a conversion start request. When CURR is low, transmission is started after a new conversion is completed.

The serial data clock can be generated by the ML2223 or it can be provided by an external source.

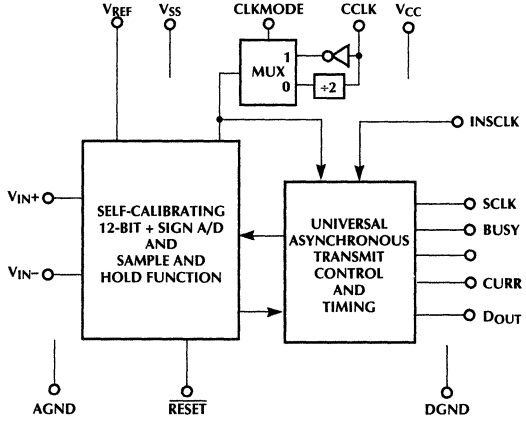
The serial interface provides LSB first data with 2's complement output coding.

FEATURES

- RS-232 compatible asynchronous interface
- One-wire data transmission
- Continuous conversions
- Nonlinearity error ±3/4 LSB and ±1 LSB max
- Conversion time (including S/H acquisition) 45.6µs max
- Bipolar –5V to +5V analog input range with ±5V power supplies
- Harmonic distortion 0.01%
- No missing codes
- Self calibrating — maintains accuracy over time and temperature
- Inputs withstand |7V| beyond supplies
- 0°C to +70°C, –40°C to +85°C temperature range
- Standard 0.3" 16-pin DIP or 20-pin SOIC (wide)

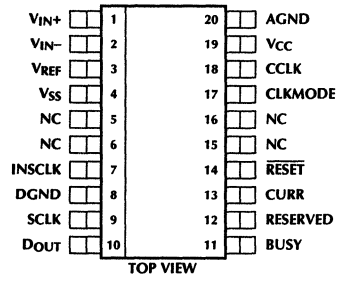
2

BLOCK DIAGRAM



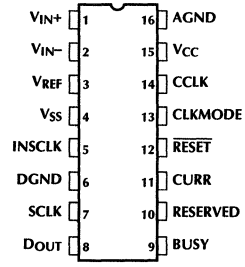
PIN CONFIGURATION

ML2223
20-Pin SOIC (S20W)



TOP VIEW

ML2223
16-Pin DIP (P16)



TOP VIEW

PIN DESCRIPTION

20 PIN	16 PIN	NAME	FUNCTION
1	1	$V_{IN}+$	Positive differential analog input; range = $V_{SS} \le V_{IN} + \le V_{CC}$, $\lvert(V_{IN}+) - (V_{IN}-)\rvert \le V_{REF}$.
2	2	$V_{IN}-$	Negative differential analog input; range = $V_{SS} \le V_{IN} - \le V_{CC}$, $\lvert(V_{IN}+) - (V_{IN}-)\rvert \le V_{REF}$.
3	3	V_{REF}	Voltage reference input; referenced to analog ground.
4	4	V_{SS}	Negative supply –5V ± 5%; decouple to AGND.
7	5	INSCLK	SCLK mode select. This pin is used to select SCLK pin as an input or an output. When INSCLK is high, SCLK is an input. When INSCLK is low, SCLK becomes an output pin. SCLK will then provide a clock at 1/128 or 1/256 depending on how the CLKMODE pin is set-up.
8	6	DGND	Digital ground.
9	7	SCLK	Serial data transmit clock. The serial data will always be transmitted at the frequency of the clock present at this pin. The SCLK pin can be programmed as an input or an output by using the INSCLK pin (pin 5). When the SCLK is used as an output pin. The data rate will be the internal converter clock divided by 128. When CLKMODE = 1, SCLK = CCLK/128. When CLKMODE = 0, SCLK = CCLK/256.
10	8	D_{OUT}	Data out. Digital output which contains result of A/D conversion. The serial data is clocked out on falling edges of SCLK.
11	9	BUSY	Three-state active high BUSY status output. Normally low. Goes high to indicate that a conversion is in progress; de-asserted when conversion is complete and data is available from the conversion just completed. A pulldown resistor is recommended on this pin.
12	10	RESERVED	This pin should be tied to ground.
13	11	CURR	Current or previous data mode pin. When this pin is tied high, the data will be transmitted at the start of a conversion (previous data mode). When CURR is tied low, the data will then be transmitted at the completion of the conversion.
14	12	$\overline{\text{RESET}}$	Active low reset. The RESET period is set by the time constant of the internal 100K pull up resistor and an external capacitor. After the RESET period the converter will be ready for accepting requests or will automatically start conversions/ transmissions based upon the mode.
17	13	CLKMODE	Clock mode pin. When CLKMODE pin = 1, the internal converter clock = CCLK. When CLKMODE pin is tied low, the internal converter clock = CCLK/2.
18	14	CCLK	Clock input. Internal clock can be generated by tying a crystal from this pin to DGND or applying a clock directly to the pin.
19	15	V_{CC}	Positive supply. +5V ± 5% decouple to AGND.
20	16	AGND	Analog ground 0 volts. Common mode reference point of the internal differential circuitry.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6.0V
Negative Supply Voltage (V_{SS}) ..... –6.0V
Voltage at Analog Inputs ..... V_{SS} – 7V to V_{CC} + 7V
Voltage at V_{REF} ..... V_{SS} – 7V to V_{CC} + 7V
Input Current per Digital Pin ..... ±10mA
Input Current at Analog Inputs ..... ±20mA
Storage Temperature Range ..... –65°C to +150°C
Package Dissipation at 25°C (Board Mount) 875mW
Lead Temperature (soldering 10 seconds)
Dual-In-Line Package (Molded) ..... 260°C
Dual-In-Line Package (Ceramic) ..... 300°C

OPERATING CONDITIONS

(Note 2)

Temperature Range ..... $T_{MIN} \le T_A \le T_{MAX}$
ML2223BIJ, ML2223CIJ ..... –40°C to +85°C
ML2223BCP, ML2223CCP ..... 0°C to +70°C
Supply Voltage (V_{CC}) ..... $4.5V_{DC}$ to $6.0V_{DC}$
Negative Supply Voltage (V_{SS}) ..... $-4.5V_{DC}$ to $-6.0V_{DC}$
Reference Voltage (V_{REF}) ..... V_{CC}

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC} = +5V ± 5%, V_{SS} = –5V ± 5%, V_{REF} = +4.75V, V_{IN}– = AGND, V_{IN}+ = –4.75V to +4.75V, $T_A = T_{MIN}$ to T_{MAX} unless otherwise specified.

			ML2223BIJ, ML2223CIJ			ML2223BCP, ML2223CCP			
PARAMETER	**NOTES**	**CONDITIONS**	**MIN**	**TYP (NOTE 3)**	**MAX**	**MIN**	**TYP (NOTE 3)**	**MAX**	**UNITS**
Converter Characteristics									
Linearity Error ML2223BXX ML2223CXX	4	f_{CCLK} = 0.1 ≤ 5MHz			±3/4 ±1			±3/4 ±1	LSB LSB
Unadjusted Zero Error ML2223BXX ML2223CXX	4				±3/4 ±2			±3/4 ±2	LSB LSB
Unadjusted Positive and Negative Full-Scale Error	4				±5			±4	LSB
Zero Error Temperature Coefficient				0.5			0.5		ppmFS/°C
Gain Temperature Coefficient				10			10		ppmFS/°C
Common Mode Rejection	5, 6		80			80			dB
Analog Input Source Resistance	4				2			2	kΩ
Analog Input Range	4	V_{IN}+ Referred to V_{IN}–	$-V_{REF}$		$+V_{REF}$	$-V_{REF}$		$+V_{REF}$	V
Analog Input Leakage Current	4				100			100	nA
Voltage Reference Input Source Impedance	4				0.5			0.5	kΩ
Reference Input Leakage Current	4				100			100	nA
Digital and DC Characteristics									
Power Supply Current I_{CC}, V_{CC} I_{SS}, V_{SS}	4			30 18	50 30		30 18	50 30	mA mA
Power Supply Rejection V_{CC} V_{SS} 	7	 DC DC to 25kHz DC DC to 25kHz		 80 50 80 50			 80 50 80 50		 dB dB dB dB
V_{ILCLK}, Clock Input Low Voltage	4				0.8			0.8	V
V_{IHCLK}, Clock Input High Voltage	4		3.5		V_{CC}	3.5		VCC	V
I_{L1}, Input Leakage Current (CCLK)	4	DGND ≤ V_{IN} ≤ V_{CC}			±200			±200	µA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	NOTES	CONDITIONS	ML2223BIJ, ML2223CIJ MIN	ML2223BIJ, ML2223CIJ TYP (NOTE 3)	ML2223BIJ, ML2223CIJ MAX	ML2223BCP, ML2223CCP MIN	ML2223BCP, ML2223CCP TYP (NOTE 3)	ML2223BCP, ML2223CCP MAX	UNITS
Digital and DC Characteristics (Continued)									
V_{IL}, Input Low Voltage	4				0.8			0.8	V
V_{IH}, Input High Voltage	4		2.0		V_{CC}	2.0		V_{CC}	V
V_{OL}, Output Low Voltage	4	I_{OL} = 2.0mA			0.45			0.45	V
V_{OH}, Output High Voltage	4	I_{OH} = –400µA	2.4			2.4			V
I_L, Input Leakage Current (except CLK)	4	DGND ≤ V_{IN} ≤ V_{CC}			±10			±10	µA
I_{HI-Z}, Output Leakage Current	4	$\overline{CS}$ ≥ V_{IH}			±10			±10	µA
C_I, Input Capacitance (all digital outputs)	5			10			10		pF
C_O, Output Capacitance (all digital outputs)	5			10			10		pF

SYMBOL	PARAMETER	NOTES	CONDITIONS		MIN	TYP (NOTE 3)	MAX	UNITS
AC Electrical Characteristics (Note 8)								
t_C	Conversion Time	4, 9	f_{CCLK} = 5MHz (CCLKMODE = "0")		45.6			µs
f_{CCLK0}	Clock Frequency	5, 9	Crystal (CCLKMODE = "0")		0.3		5	MHz
			Driven (CCLKMODE = "0")		0.1		5	MHz
f_{CCLK0}	Clock Width	5, 9	Driven (CCLKMODE = "0")	High	50			ns
				Low	50			ns
f_{CCLK1}	Clock Frequency	5	Driven (CCLKMODE = "1")		0.05		2.5	MHz
f_{CCLK1}	Clock Width	5	Driven (CCLKMODE = "1")	High	150			ns
				Low	150			ns
$t_{SCLK, DO}$	Serial Clock Low to DO Valid/Hold	4					190	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground

Note 2: 0°C to +70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions

Note 3: Typicals are parametric norm at 25°C

Note 4: Parameter guaranteed and 100% production tested.

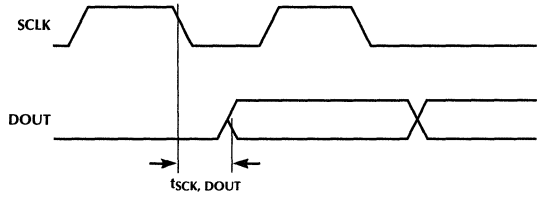
Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 6: Common mode rejection is the ratio of the change in zero error to the change in common mode input range.

Note 7: Power supply rejection is the ratio of the change in zero error to the change in power supply voltage.

Note 8: All parameters measured from 0.8V to 2.0V, CL = 50pF.

Note 9: Maximum frequency is $1/t_{CLK1}$ (high) + t_{CLK1} (low) + rise + fall times, which must be ≤ 2.5MHz.



Serial Clock to Data Out Delay

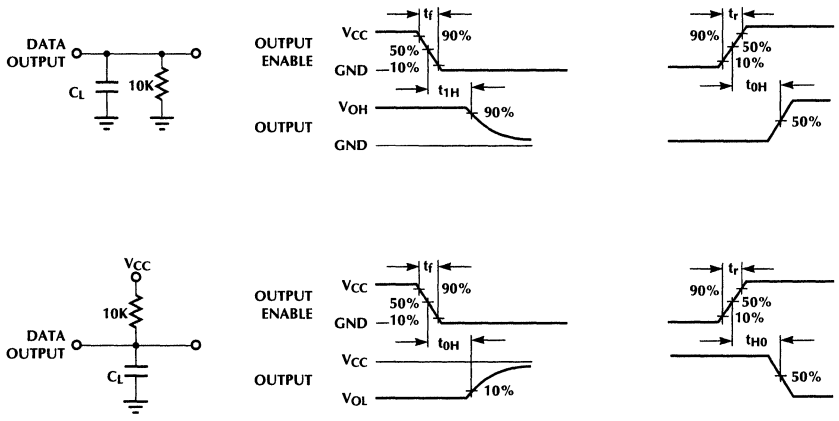


Figure 1. High Impedance Test Circuits and Waveforms

1.0 FUNCTIONAL DESCRIPTION

2

1.1 ALGORITHMIC A/D CONVERTER

Micro Linear's algorithmic converter uses a successive approximation technique. Most of today's successive approximation converters use a DAC to feedback the approximated signal, however this technique requires more circuitry than algorithmic converters. In addition the values of all of the resistors or capacitors in the DAC must be matched to within the accuracy of the converter. This is difficult beyond 10 bits unless trimming is used. An algorithmic converter uses less circuitry and is more easily trimmed. Micro Linear's algorithmic converter is implemented using a 2x amplifier, a sample/hold amplifier and a comparator as shown in Figure 2.

The input sample is first multiplied by two then compared to the reference voltage. If the 2x input voltage is greater than the reference, the MSB is a 1 and the reference voltage is subtracted from the 2x input voltage. The remainder is stored in the sample and hold. If the 2x input voltage is less than the reference, the MSB is a 0 and the 2x input voltage is stored in the sample and hold. This process repeats again, however now the sample and hold voltage is multiplied by 2.

The algorithm involves multiplication by 2, comparison, and possibly subtraction. Referring to Figure 2, the algorithm for the circuit can be described as follows:

Step 1 If $(2 \times V_{IN}) - V_{REF} \geq 0$
then MSB = 1
$(2 \times V_{IN}) - V_{REF} \rightarrow S/H$
else MSB = 0
$(2 \times V_{IN}) \rightarrow S/H$

Step 2 If $(2 \times S/H) - V_{REF} \geq 0$
then next bit = 1
$(2 \times S/H) - V_{REF} \rightarrow S/H$
else next bit = 0
$(2 \times S/H) \rightarrow S/H$

Step 3 Repeat Step 2 until conversion complete.

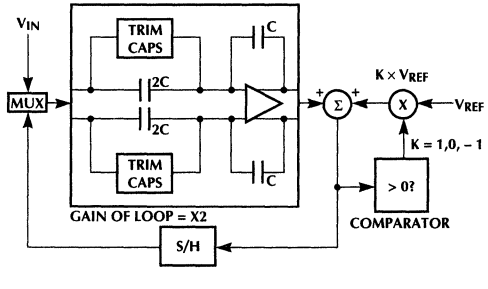


Figure 2. Self Calibrating A/D Converter

Since the A/D converter handles bipolar inputs negative inputs are handled slightly differently using the same principle.

1.1.1 Self Calibration

In order to maintain integral and differential linearity in an algorithmic converter, two critical parameters need to be controlled, loop offsets and the gain of the loop. Loop offsets are automatically nulled before each conversion using auto-zeroing circuitry on both the sampling amplifier and the 2x amplifier. The gain of the loop is adjusted using self calibration.

Self calibrating the algorithmic converter, once the offsets have been nulled, is performed by measuring the 2x gain of the loop and adjusting it. The gain can be measured by converting the reference voltage at the input as well as the reference (V_{REF}/V_{REF}), and examining the output code. Converting V_{REF} should yield plus full scale, since V_{REF}/V_{REF} should equal 1. If the gain of the loop is slightly less than 2, the resulting LSB of the conversion will be "0". If the magnitude bits of the resulting conversion are all "1s", the gain may be too great, therefore the gain is reduced to the point where the threshold of the LSB is reached.

Adjustment of the 2x gain is done with binary weighted trim capacitor arrays connected to each of the 2C input capacitors. A small value of capacitance is either added to or subtracted from the 2C input caps until the gain of the loop is within 13-bit accuracy.

The self calibration and trimming is performed in the factory at wafer sort. This procedure is not available as a finished product.

1.1.2 Conversion Times

The following table lists the conversion times which include the sample and hold acquisition time.

OPERATION MODE	INTERNAL CLOCKS*
FREERUN	113

1.1.3 Sample and Hold Timing

Figure 3 shows the internal timing for the sample and hold circuitry. The relationship between the start of conversion and the input channel going into sample mode is fixed at 6 internal clocks*. Six internal clocks after the start of conversion the sample and hold is switched into the sample mode, placing two 9pF capacitors in parallel with the input pins; one on $V_{IN}+$ and one on $V_{IN}-$. The sample switch is kept in the sample mode for 8 internal clocks (3.2µs at a 5MHz external clock), then placed in the hold mode. During the next 2 internal clocks the charge on the sample and hold is transferred into the A/D, after which the V_{REF} pin is sampled for 8 internal clocks.

*For a description of internal clocks see Clock section.

1.2 ANALOG INPUTS

1.2.1 Differential Inputs and Common Mode Rejection

The differential inputs of the ML2223 eliminate the effects of common mode input noise (60Hz for example), as $V_{IN}+$ and $V_{IN}-$ are sampled at the same time.

1.2.2 Noise

The leads to the analog inputs should be kept as short as possible to minimize output noise. Noise as well as digital clocks can couple into the inputs and cause errors. Input filters can be used to reduce the effects of these sources.

1.2.3 Power Supply Decoupling

Low inductance tantalum capacitors of 1µF or greater and 0.01µF disc ceramic capacitors are recommended for bypassing V_{CC} as well as V_{SS} to AGND. These capacitors should be placed close to the V_{CC} and V_{SS} pins.

1.3 CONVERTER CLOCK

The CCLK input can be driven with an external clock or a crystal referenced to DGND. The crystal must be parallel resonant with minimum capacitive loading. (i.e., no bypass caps should be used and leads should be kept short).

If driven with external clock and if the CLKMODE pin is tied to V_{CC}, the frequency must be between 50KHz to 2.5MHz with the requirement that clock LOW (t_{CCLKL}) and clock HIGH (t_{CCLKH}) durations must be more than 150ns. If the CCLKMODE pin is tied to ground then the frequency can be from 100KHz to 5.0MHz.

For crystal operation with the divide by two flip flop bypassed, and there is a 40 to 60% variation in duty cycle of the oscillator, the maximum crystal frequency is 2.5MHz to insure that the minimum clock high and low times are greater than 150 nsec.

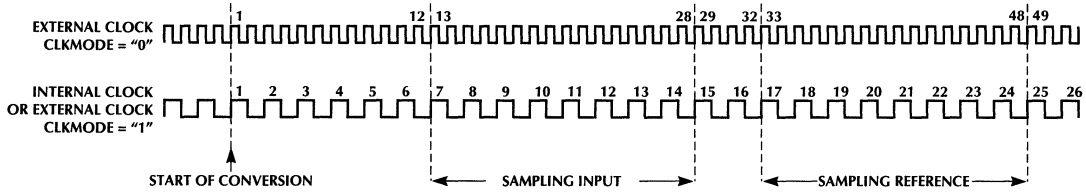


Figure 3. Sample and Hold Timing

1.4 RESET

The $\overline{\text{RESET}}$ pin has an internal 100K pullup resistor. Power supplies must be stable to within a ±5% tolerance before the reset condition is removed.

The active low hardware reset can be performed by a capacitor value (usually >6µF) tied to the $\overline{\text{RESET}}$ pin or by driving it with the system reset signal.

1.5 SCLK

The SCLK is used to clock out the data to the transmission line via the D_{OUT} pin. The SCLK can be supplied either externally or internally through the use of the INSCLK pin. Maximum SCLK frequency is 625kHz.

In applications where the internal SCLK is used, the SCLK is generated by dividing the internal clock by 128. For example, when 2.4576MHz crystal is used to generate CCLK, this will result in a 19.2Kbps data transmission rate (CLKMODE = 1). In the case where CLKMODE = 0, then the transmission rate will be 9.6Kbps.

1.6 CONVERTER OPERATION

There are two basic types of operation. By programming the CURR pin to "1", the device will be operating in the "Previous Data Mode" and when CURR pin = "0", the device is in the "Current Data Mode."

The ML2223 performs continuous conversion. The conversion takes 110 clock periods and an additional 13 clock periods are required for the device to shift out the data. In the Current Data Mode, the data are transmitted after the conversion is completed. 24-bit time of the SCLK (transmit clock) is required to transmit the full data frame and an additional 8-bit time of idle is needed before the next conversion begins. A total of 32-bit time delay of the SCLK is therefore needed between conversions (see Figure 4).

In the Previous Data Mode, the data is transmitted at the start of the conversion (see Figure 5).

1.7 DATA FORMAT

The converter data is output in two data byte frame. Each frame has one start bit and two stop bits and each data byte consists of 8 bits of data and one parity bit. The data is transmitted LSB first (see Figure 6).

The first data byte transmitted is the least significant byte with even parity and the second byte is the most significant byte with odd parity. Thus, the UART can identify the lower byte or the upper byte by observing the parity error flag in accordance to the parity check it has set-up.

2

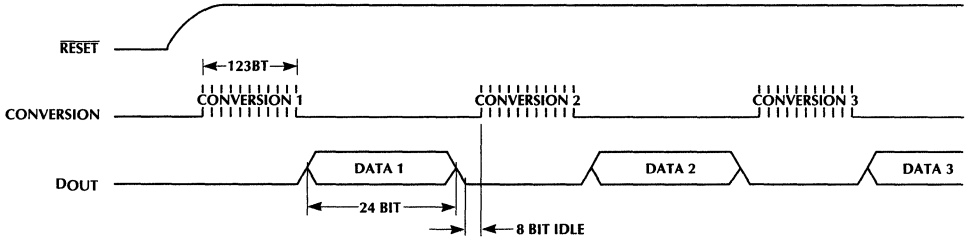


Figure 4. Current Data Mode.

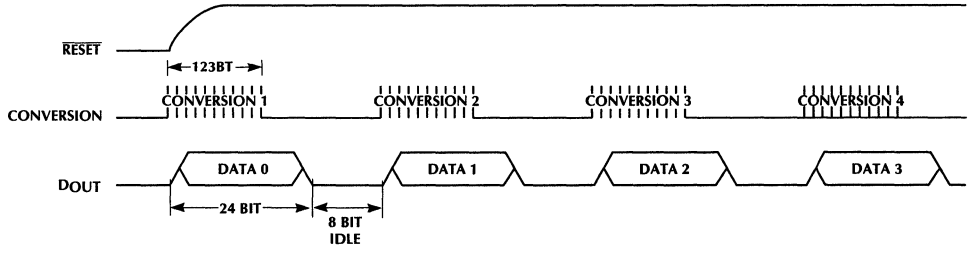


Figure 5. Previous Data Mode.

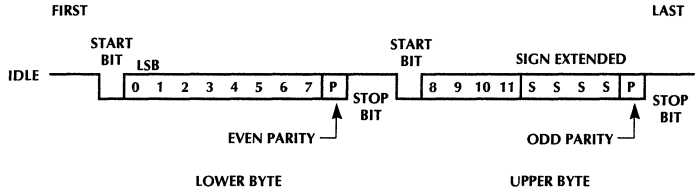


Figure 6. Data Format.

APPLICATIONS (For detailed applications information, see Application Note 41)

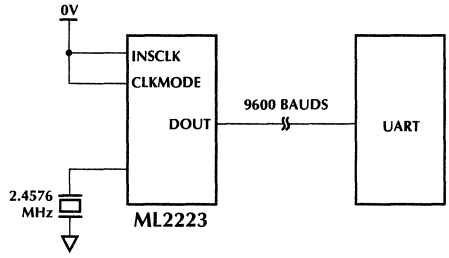


Figure 7. Remote Monitor System.

ORDERING INFORMATION

PART NUMBER	LINEARITY ERROR	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
ML2223BCP ML2223BIJ	±3/4 LSB	±1 1/2	0°C to +70°C –40°C to +85°C	Molded DIP (P16) Hermetic DIP (J16)
ML2224CCP ML2223CCS	±1 LSB	±2 1/2	0°C to +70°C 0°C to +70°C	Molded DIP (P16) Molded SOIC (S20W)

ML2223EVAL

12-BIT A/D Converter with PC Compatible Serial Interface Evaluation Kit

GENERAL DESCRIPTION

The ML2223 12-bit plus sign A/D Converter has an Asynchronous serial output designed specifically for the communications port (COM1 or COM2 etc.) of IBM PC-compatible computers. This is the same port used by the mouse or any other external serial port device such as modems and printers. The ML2223 evaluation kit is a combination of hardware and software to ease the interface between the PC and device without spending considerable time writing software or prototyping the circuit board. The board contains optional functions to set baud rate, reference voltage and analog multiplexing to allow user customization. The software provided ranges from a simple Assembly/C routine to a sophisticated GUI (Graphical User Interface) that furnishes software control over the hardware and an "oscilloscope" type display of the analog input.

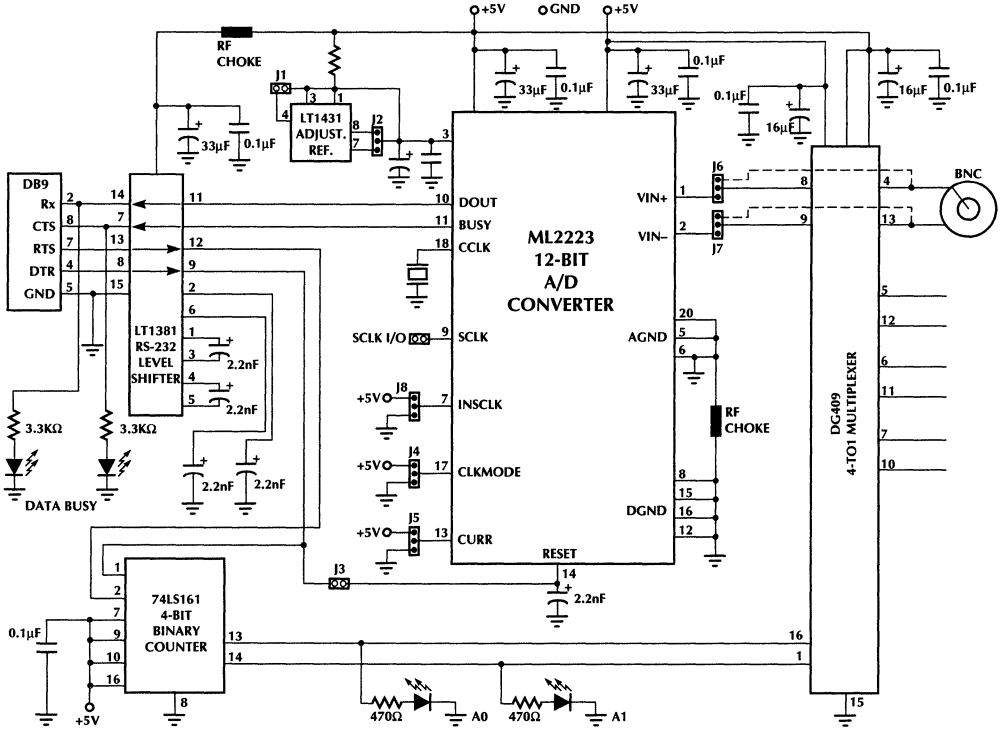
FEATURES

- RS-232 compatible asynchronous interface
- One or two-wire data transmission
- Assembly, C and LabWindows™ software provided
- 9600 or 19200 on-board baud rate generator
- 256Kbaud available with external generator
- DB9 connector for direct connection to COM port

KIT CONTENTS

- ML2223EVAL Users guide
- ML2223 data sheet
- Fully populated, assembled and tested Evaluation board
- 3.5" Disk with PC-compatible software
- Gerber File

2



µP Compatible 12-Bit Plus Sign A/D Converter with Sample and Hold

GENERAL DESCRIPTION

The ML2230 is a member of Micro Linear's 12-bit plus sign CMOS A/D converter family utilizing a self calibrating algorithmic technique. The sample-and-hold, incorporated on the ML2230, has a differential input for noise immunity and power supply rejection. All errors of the sample-and-hold are accounted for in the analog-to-digital converter's accuracy specification.

The ML2230B has a maximum non-linearity error over temperature of 0.018% of full-scale, and the ML2230C and ML2230D have a maximum non-linearity error over temperature of 0.024% of full scale.

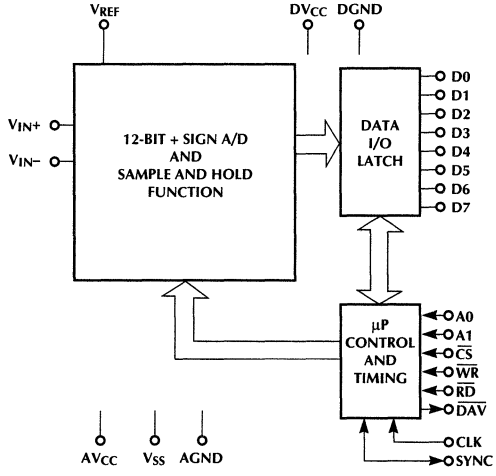
Designed to interface to an 8-bit microprocessor bus without additional components, the ML2230 outputs the 13-bit data result two 8-bit bytes. Data format is 2's complement. All digital signals are fully TTL and CMOS compatible.

For interfacing to a 16-bit microprocessor bus the ML2233 provides a 13-bit data result.

FEATURES

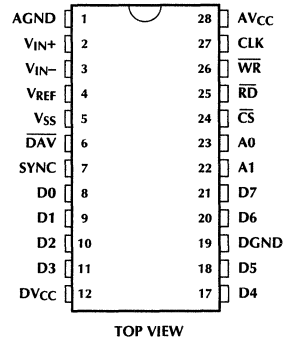
- Resolution 12-bits + sign
- Conversion time (including S/H acquisition) 31.5µs max
- Sample and hold acquisition 2.3µs max
- Non-linearity error ±¾LSB and ±1LSB max
- Low harmonic distortion 0.01%
- No missing codes
- Self calibrating — maintains accuracy over time and temperature
- Inputs withstand |7V| beyond supplies
- Data transfer options — interrupt, DMA, or polling
- Outputs data in two 8-bit bytes
- Standard 24-pin DIP

BLOCK DIAGRAM



PIN CONNECTIONS

ML2230
24-Pin DIP (P24)



TOP VIEW

PIN DESCRIPTION

DIP	PCC	NAME	FUNCTION
1	1	AGND	Analog ground.
2	2	$V_{IN}+$	Positive differential analog input; range = $V_{SS} \le V_{IN}+ \le AV_{CC}$, $\lvert(V_{IN}+) - (V_{IN}-)\rvert \le V_{REF}$.
3	3	$V_{IN}-$	Negative differential analog input; range = $V_{SS} \le V_{IN}- \le AV_{CC}$, $\lvert(V_{IN}+) - (V_{IN}-)\rvert \le V_{REF}$.
4	4	V_{REF}	Voltage reference input; referenced to analog ground.
5	5	V_{SS}	Negative power supply; decouple to AGND.
6	8	$\overline{DAV}$	Data available; indicates a conversion has completed and data is available or calibration completed.
7	9	SYNC	In the slave mode, SYNC is a positive edge triggered input used to start a conversion. In master mode, SYNC is an output and indicates a conversion has occurred.
8	10	D0	Bidirectional data bit.
9	11	D1	Bidirectional data bit.
10	13	D2	Bidirectional data bit.
11	14	D3	Bidirectional data bit.
12	15	DV_{CC}	Digital power supply. Tie to AV_{CC} from same power supply.
13	16	D4	Bidirectional data bit.
14	17	D5	Bidirectional data bit.
15	18,19	DGND	Digital ground.
16	20	D6	Bidirectional data bit.
17	21	D7	Bidirectional data bit.
18	22	A1	Address for the microprocessor interface to access any one of the four registers.
19	23	A0	Address for the microprocessor interface to access any one of the four registers.
20	24	$\overline{CS}$	Chip select; enables writing to or reading from.
21	25	$\overline{RD}$	Read; enables ML2230 to drive data bus.
22	26	$\overline{WR}$	Write; allows writing into the registers.
23	27	CLK	Clock input. Driven with an external clock or crystal referenced to DGND. The crystal must be parallel resonant with minimum capacitive loading. (i.e., no bypass caps should be used and leads should be kept short.)
24	28	AV_{CC}	Positive analog power supply. Decouple to AGND. Tie to DV_{CC} from same power supply.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages (AV_{CC} and DV_{CC}) 6.0V
Negative Supply Voltage (V_{SS}) ..... –6.0V
Voltage at Analog
Inputs ..... V_{SS} – 7V to AV_{CC} + 7V
Voltage at V_{REF} ..... V_{SS} – 7V to AV_{CC} + 7V
Input Current per Digital Pin ..... ±10mA
Input Current at Analog Inputs ..... ±20mA
Storage Temperature Range ..... –65°C to +150°C
Package Dissipation @ 25°C 875mW
Lead Temperature soldering,
Dual-In-Line Package (Plastic) ..... 260°C

OPERATING CONDITIONS

(Note 2)

Temperature Range ..... 0°C to 70°C
Supply Voltage (AV_{CC} and DV_{CC}) ..... $4.5V_{DC}$ to $6.0V_{DC}$
Negative Supply Voltage (V_{SS}) ..... $-4.5V_{DC}$ to $-6.0V_{DC}$
Reference Voltage (V_{REF}) 2.60V

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC} = +5V ± 5%, V_{SS} = –5V ± 5%, V_{REF} = 2.500V, V_{IN}– = AGND, V_{IN}+ = –2.5V to +2.5V, T_A = T_{MIN} to T_{MAX} unless otherwise specified.

PARAMETER	NOTES	CONDITIONS	TYP MIN	(NOTE 3)	MAX	UNITS
Converter Characteristics						
Linearity Error						
ML2230BXX	4	f_{CCLK} = 0.1 ≤ 7MHz			±3/4	LSB
ML2230CXX		f_{CCLK} = 0.1 ≤ 7MHz			±1	LSB
ML2230DXX		f_{CCLK} = 0.1 ≤ 5MHz			±1	LSB
Unadjusted Zero Error						
ML2230BXX	4				±3/4	LSB
ML2230CXX					±2	LSB
ML2230DXX					±2	LSB
Unadjusted Positive and Negative Full Scale Error	5				±4	LSB
Zero Error Temperature Coefficient				0.5		ppm/°C
Gain Temperature Coefficient				10		ppm/°C
Common-Mode Rejection	5, 6		80			dB
Analog Input Source Resistance	5				2	kΩ
Analog Input Range	4	V_{IN}+ Refer to V_{IN}–	–V_{REF}		+V_{REF}	V
Analog Input Leakage Current	4				100	nA
Voltage Reference Input Source Impedance	5				0.5	kΩ
Reference Input Leakage Current	4				100	nA
Digital and DC Characteristics						
Power Supply Current						
AI_{CC}, Analog V_{CC}	4			30	50	mA
DI_{CC}, Digital V_{CC}				10		µA
I_{SS}, V_{SS}				18	30	mA
Power Supply Rejection	7					
AV_{CC}		DC		80		dB
		DC to 25kHz		50		dB
V_{SS}		DC		80		dB
		DC to 25kHz		50		dB
V_{ILCLK}, Clock Input Low Voltage	4				0.8	V
V_{IHCLK}, Clock Input High Voltage	4		3.5		AV_{CC}	V
I_{L1}, Input Leakage Current (CLK)	4	AGND ≤ V_{IN} ≤ AV_{CC}			±200	µA
V_{IL}, Input Low Voltage	4				0.8	V
V_{IH}, Input High Voltage	4		2.0		DV_{CC}	V
V_{OL}, Output Low Voltage	4	I_{OL} = 2.0mA			0.45	V
V_{OH}, Output High Voltage	4	I_{OH} = –400µA	2.4			V
I_L, Input Leakage Current (except CLK)	4	AGND ≤ V_{IN} ≤ AV_{CC}			±10	µA
I_{HI-Z}, Output Leakage Current (D0–D7)	4	$\overline{RD}$ = $\overline{CS}$ = V_{IH}			±10	µA
C_I, Input Capacitance (all digital inputs)				10		pF
C_O, Output Capacitance (outputs D0 to D7, and $\overline{DAV}$)				10		pF

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	NOTES	CONDITIONS		MIN	TYP (NOTE 3)	MAX	UNITS
AC Electrical Characteristics (Note 8)								
t_C	Conversion Time	4, 9	CLK Mode = 0	f_{CLK} = 7.0MHz f_{CLK} = 5.0MHz	31.5 44.0			µs µs
	Sample and Hold Acquisition	4, 9	CLK Mode = 0	f_{CLK} = 7.0MHz f_{CLK} = 5.0MHz			2.3 3.2	µs µs
f_{CLK0}	Clock Frequency	5, 9	Crystal (CLK Mode = 0) Crystal (CLK Mode = 0)		3 1		7 7	MHz MHz
t_{CLK0}	Clock Width	5, 9	Driven (CLK Mode = 0)	High Low	50 50			ns ns
f_{CLK1}	Clock Frequency	5, 10	Driven (CLK Mode = 1)		0.5		(Note 11)	MHz
t_{CLK1}	Clock Width	5, 10	Driven (CLK Mode = 1)	High Low	125 125			ns ns
t_{AD}	Address Stable to Valid Data	4			150			ns
t_{AR}	Address Stable Before Read	4			0			ns
t_{RA}	Address Hold After Read	4			0			ns
t_{RR}	Read Pulse Width	4			150			ns
t_{RD}	Read Access	4					150	ns
t_{1Z}, t_{0Z}	Data Read to Hi-Z	4			0		50	ns
t_{RV}	Recovery Between Two Reads or Writes	5			250			ns
t_{RDCK}	Read to Clock Setup Time	5, 12			40			ns
t_{AW}	Address Stable Before Write	4			0			ns
t_{WA}	Address Hold After Write	4			0			ns
t_{WW}	Write Pulse Width	4			150			ns
t_{DW}	Data Setup Before Write Trailing Edge	4			100			ns
t_{WD}	Data Hold After Write Trailing Edge	4			0			ns
t_{WRCK}	Write to Clock Setup Time	5, 12			40			ns
t_{CKDAV}	Clock to $\overline{DAV}$ Assert	4, 13	C_L = 50pF			120	220	ns
t_{SYNCCK}	SYNC Input to Clock Setup	5, 12			40			ns
t_{SYNCN}	SYNC Input Width	5	(CLK Mode = 0) (CLK Mode = 1)		6 3			$1/f_{CLK0}$ $1/f_{CLK1}$

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP (NOTE 3)	MAX	UNITS
AC Electrical Characteristics (Note 8) (Continued)							
t_{CKSYNC}	External Clock to SYNC Output Delay	5, 13	C_L = 50pF		150	200	ns
t_{SYNCO}	SYNC Output Pulse Width	5, 13	(CLK Mode = 0) (CLK Mode = 1)			8 4	$1/f_{CLK0}$ $1/f_{CLK1}$
t_{WRDAV}	Write Reg2 to $\overline{DAV}$ Rising Edge	4, 14	C_L = 50pF			170	ns
t_{RDDAV}	Read Reg0 to $\overline{DAV}$ Rising Edge	4, 15	C_L = 50pF			170	ns
t_r, t_f	Rise and Fall		All Inputs			25	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Devices are 100% tested with temperature limits guaranteed by 100% testing, sampling or by correlation with worst-case test conditions.
Note 3: Typicals are parametric norm at 25°C.
Note 4: Parameter guaranteed and 100% production tested.
Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.
Note 6: Common mode rejection is the ratio of the change in zero error to the change in common mode input range.
Note 7: Power supply rejection is the ratio of the change in zero error to the change in power supply voltage.
Note 8: All parameters measured from 0.8V to 2.0V, C_L = 100pF
Note 9: CK1X bit in control register = 0.
Note 10: CK1X bit in control register = 1.
Note 11: Maximum frequency is $1/t_{CLK1}$ (high) + t_{CLK1} (low) + rise + fall times and ≤ 3.5MHz.
Note 12: Setup time required for synchronous start of conversion.
Note 13: In CLK mode = 0 (CK1X bit in control register = 0) start of conversion will occur at specified time, or time plus one t_{CLK0} period (see Figure 5).
Note 14: Writing a control register bit 0 with a one will acknowledge the $\overline{DAV}$ condition and de-assert DAV output.
Note 15: In start mode = 1, a read from location "0" will start the next conversion and de-assert the DAV output.

TIMING DIAGRAMS

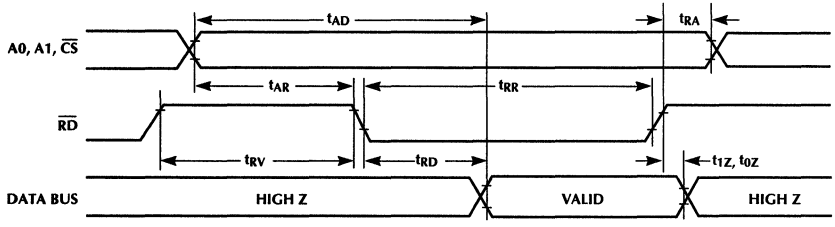


Figure 1. Read Cycle

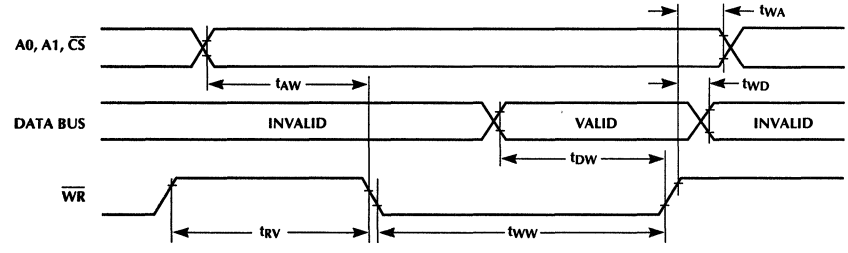
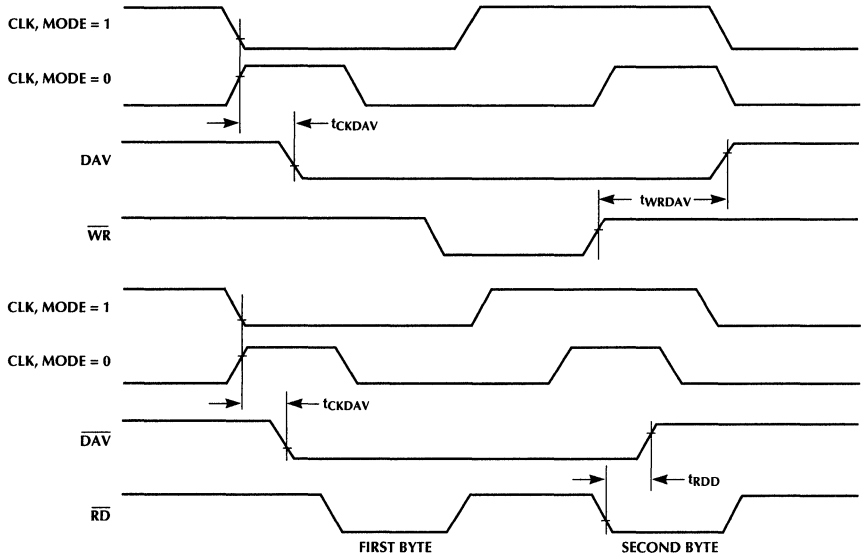


Figure 2. Write Cycle

TIMING DIAGRAMS (Continued)



DAV IS SET AND CLEARED BY INTERNAL CIRCUITRY.
NOTE: DMA BIT IN THE CONTROL REGISTER MUST BE SET FOR THIS OPERATION.

Figure 3. Data Available

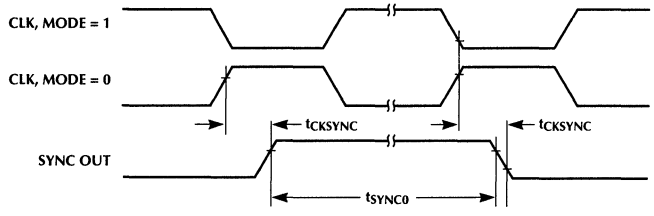
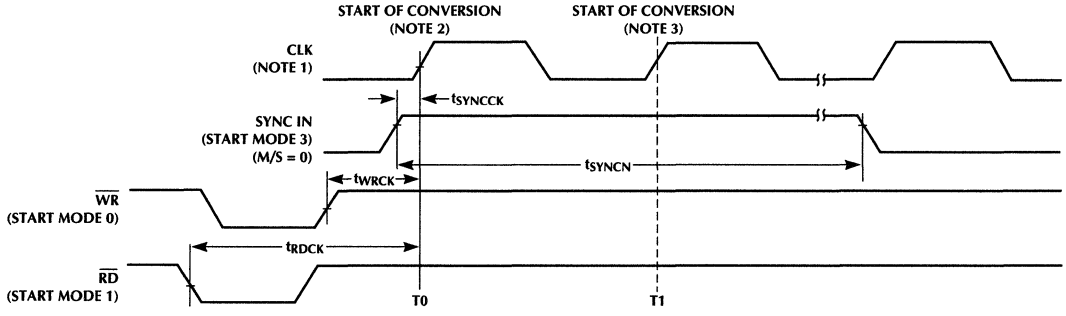


Figure 4. SYNC Output

TIMING DIAGRAMS (Continued)



NOTES:
1. CLK IS THE CLOCK DRIVEN AT THE CLOCK PIN.
2. IN CLK MODE 1, WILL ALWAYS OCCUR AT T0 IF SETUP TIMES ARE MET.
3. IN CLK MODE 0, WILL OCCUR EITHER AT T0 OR T1 IF SETUP TIMES ARE MET.

Figure 5. Start of Conversion (Start Mode 0, 1, 3)

BLOCK DIAGRAM

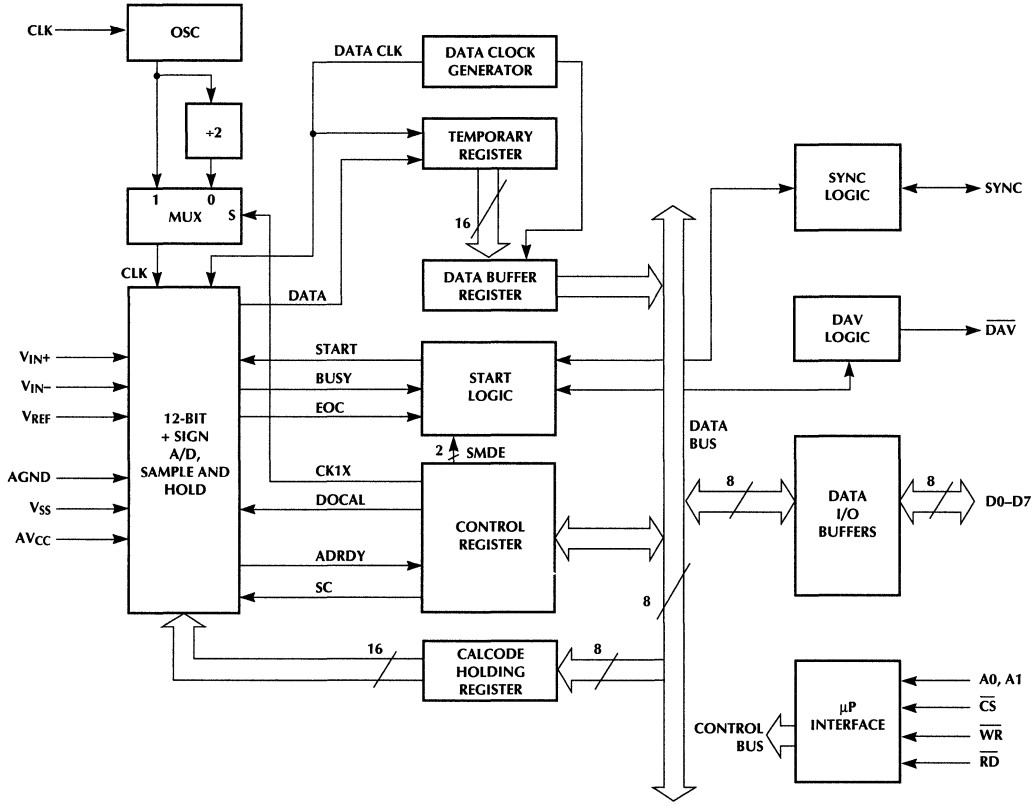


Figure 6. Block Schematic Diagram

FUNCTIONAL DESCRIPTION

ALGORITHMIC A/D CONVERTER

Micro Linear's algorithmic converter uses a successive approximation technique. Most of today's successive approximation converters use a DAC to feedback the approximated signal, however this technique requires more circuitry than algorithmic converters. In addition the values of all of the resistors or capacitors in the DAC must be matched to within the accuracy of the converter. This is difficult to do in silicon beyond 10 bits unless trimming is used. An algorithmic converter uses less circuitry and is more easily trimmed. Micro Linear's algorithmic converter is implemented using a 2x amplifier, a sample/hold amp, and a comparator as shown in Figure 7.

The input sample is first multiplied by two then compared to the reference voltage. If the 2x input voltage is greater than the reference, the MSB is a 1 and the reference voltage is subtracted from the 2x input voltage. The remainder is stored in the sample and hold. If the 2x input voltage is less than the reference, the MSB is a 0 and the 2x input voltage is stored in the sample and hold. This process repeats again, however now the sample and hold voltage is multiplied by 2.

The algorithm involves multiplication by 2, comparison, and possibly subtraction. Referring to Figure 6, the algorithm for the circuit can be described as follows:

Step 1 If $(2 \times V_{IN}) - V_{REF} \geq 0$
then MSB = 1
$(2 \times V_{IN}) - V_{REF} \rightarrow S/H$
else MSB = 0
$(2 \times V_{IN}) \rightarrow S/H$

Step 2 If $(2 \times S/H) - V_{REF} \geq 0$
then next bit = 1
$(2 \times S/H) - V_{REF} \rightarrow S/H$
else next bit = 0
$(2 \times S/H) \rightarrow S/H$

Step 3 Repeat Step 2 until conversion complete.

Since the A/D converter handles bipolar inputs, negative inputs are handled slightly differently using the same principle.

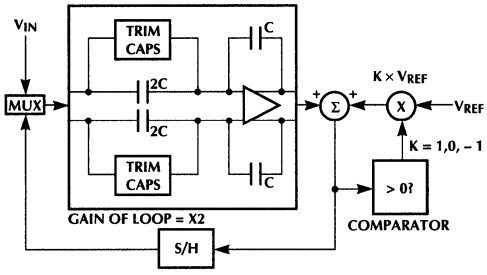


Figure 7. Self Calibrating A/D Converter

SELF CALIBRATION

In order to maintain integral and differential linearity to the 1/2 LSB level in an algorithmic converter, two critical parameters need to be controlled, loop offsets and the gain of the loop. Loop offsets are automatically nulled before each conversion using auto-zeroing circuitry on both the sampling amp and the 2x amp. The gain of the loop is adjusted using self calibration.

Self calibrating the algorithmic converter, once the offsets have been nulled, is performed by measuring the 2x gain of the loop and adjusting it. The gain can be measured by converting the reference voltage as the input as well as the reference (V_{REF}/V_{REF}), and examining the output code. Converting V_{REF} should yield plus full scale, since V_{REF}/V_{REF} should equal 1. If the gain of the loop is slightly less than 2, the resulting LSB of the conversion will be "0". If the magnitude bits of the resulting conversion are all "1s", the gain may be too great, therefore the gain is reduced to the point where the threshold of the LSB is reached.

Adjustment of the 2x gain is done with the binary weighted trim capacitor arrays connected to each of the 2C input capacitors. A small value of capacitance is either added to or subtracted from the 2C input caps until the gain of the loop is within 13 bit accuracy of 2.

CONVERSION TIMES

The following table lists the conversion times which include the sample and hold acquisition time. For a CALRD and CALWR no A/D conversion actually takes place.

OPERATION	# OF INTERNAL CLOCKS*
8 bit A/D	80
13 bit A/D	110
CALWR	52
CALRD	80

SAMPLE AND HOLD TIMING

Figure 8 shows the internal timing for the sample and hold circuitry. The relationship between the "Start of Conversion" and the input channel going into sample mode is fixed at 6 internal clocks*, regardless of the Start Mode. Six internal clocks after the Start of Conversion the Sample and Hold is switched into the sample mode, placing two 9pF capacitors in parallel with the inputs pins; one on $V_{IN}+$ and one on $V_{IN}-$. The sample switch is kept in the sample mode for 8 internal clocks (2.3µs at a 7MHz external clock), then placed in the hold mode. During the next 2 internal clocks the charge on the sample and hold is transferred into the A/D, after which the V_{REF} pin is sampled for 8 internal clocks.

Figure 8 also illustrates the timing of the SYNC pin in Master Mode during a conversion (M/S = 1 Control High Byte register) and Start Mode 0, 1, or 2. SYNC is activated one internal clock cycle after the Start of Conversion and lasts for four internal clocks.

*For a description of internal clocks see Clock section.

ANALOG INPUTS

Differential Inputs and Common Mode Rejection

The differential inputs of the ML2230 eliminate the effects of common mode input noise (60Hz for example), as $V_{IN}+$ and $V_{IN}-$ are sampled at the same time.

Noise

The leads to the analog inputs should be kept as short as possible to minimize output noise. Noise as well as digital clocks can couple into the inputs and cause errors. Input filters can be used to reduce the effects of these sources.

Power Supply Decoupling

Low inductance tantalum capacitors of 1µF or greater and 0.01µF disc ceramic capacitors are recommended for bypassing AV_{CC} as well as V_{SS} to AGND. These capacitors should be placed close to the AV_{CC} and V_{SS} pins.

MICROPROCESSOR INTERFACE

There are four 8-bit directly addressable registers; two Data Buffer registers and two Control registers. The data buffer registers provide the conversion results. The data registers are double buffered, allowing one result to be read while the next sample is being converted. The data registers also allow access to the algorithmic converter's calibration code. Normally the ML2230 is operated without ever accessing these registers. (Refer to Diagnostics for more information). The two Control registers provide complete control and status information. These four registers are addressed by pins A0 and A1.

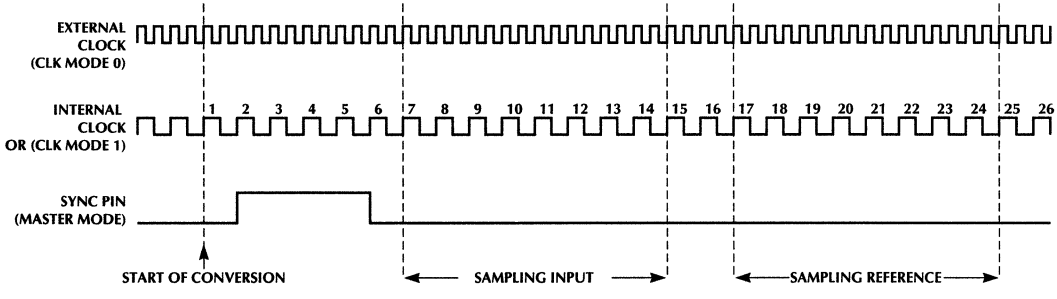


Figure 8. Sample and Hold Timing

All data is returned from the converter in sixteen bit two's complement format, right hand justified, with the sign bit extended across the most significant bits

Cycle	+Max	–Min	Zero
13	0FFF	F000	0000
8	007F	FF80	0000

REGISTER DESCRIPTION

REGISTER 0 — DATA BUFFER LOW BYTE:

Register 0 contains the low byte result of the latest conversion when read. Depending on the Start Mode selected, reading or writing to this register may start the next conversion.

REGISTER 1 — DATA BUFFER HIGH BYTE:

Register 1 contains the high byte result of the latest conversion when read.

REGISTER 2 — CONTROL REGISTER LOW BYTE:

Bit 0 (DAV status when READ/DAVACK acknowledge when a ONE is written):
Reading DAV = 1 indicates that new data is available or a calibration is complete. If both data bytes have been read, DAV will be cleared automatically. This bit can be explicitly acknowledged by writing a ONE to it; writing a zero has no effect. The $\overline{DAV}$ output pin always reflects the DAV status bit.

Bit 1 (BUSY status when READ/RESET when a ONE is written):
Reading BUSY = 1 indicates that a conversion or calibration is in progress. Writing a ONE will force a chip reset. Writing a zero has no effect.

RESET DEFAULT CONDITIONS:

Both Control registers will automatically be cleared. Both Data Buffer registers will be unchanged. The Calibration register is not cleared after a reset, however the ADRDY bit is cleared. Since the DAV status bit is cleared, the DAVB output is inactivated (high). The SYNC pin is forced to be an input as a result of clearing the M/S bit in the Control High Byte register.

Bit 2 (ADRDY status when READ/DOCAL request when a ONE is written):
Reading ADRDY = 0 indicates that the converter has not been calibrated since the last reset, and ADRDY = 1 indicates that is has been calibrated since the last reset. Writing a ONE will force the converter to do a calibration; writing a zero has no effect.

Bit 3 (SC: Short cycle select):
Selects 8 or 13 bit conversions.

SC = 0: 13-bit conversion (default)
SC = 1: 8-bit conversion (short cycle)

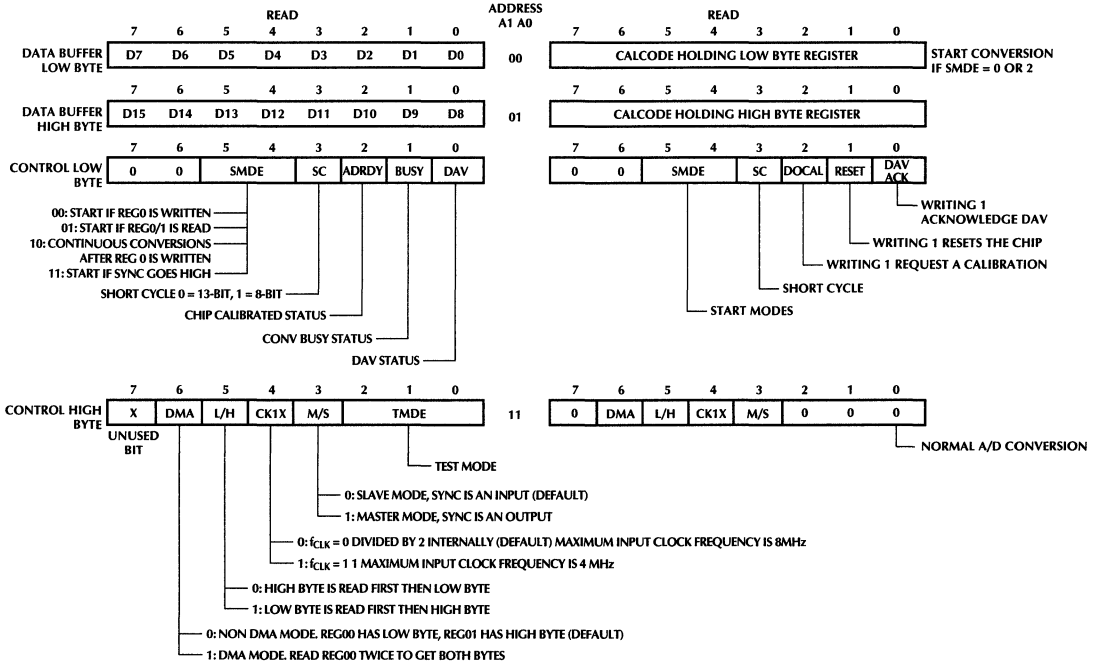


Figure 9. Register Description

Note: For 8-bit conversions in non-DMA mode, only one byte needs to be read. This can be accomplished by setting L/H = 0, DMA = 0 and reading the Data Low Byte register. In DMA mode both bytes need to be read.

Bits 4,5 (SMDE: Start Mode):
Defines Start Conversion mode.

Bits 5,4

00	Start Conversion upon writing to register 0 (default)
01	Start Conversion upon reading register 0 if L/H = 0, or Start Conversion upon reading register 1 if L/H = 1. In DMA mode both bytes need to be read. The second byte read will Start Conversion.
10	Start Continuous Conversions upon writing to register 0.
11	Start on external SYNC input going high (Requires Slave mode: M/S = 0)

Bits 7,6 (reserved):
These bits are reserved by Micro Linear and must be written as zero.

Register 3 (Control Register High Byte):

Bits 2,1,0 (TMDE: test mode select bits)
These bits are used for diagnostic purposes only and normally not accessed during operation. The default value of TMDE is 000 which selects a normal A/D conversion. See Diagnostics for more information.

TMDE	Description
000	Normal A/D Conversion
001	Reserved by Micro Linear (Do Not Use)
010	CALWR Operation
011	CALRD Operation
100	System Offset
101	Common-mode
110	Plus Full Scale
111	Minus Full Scale

Bit 3 (M/S: Master/Slave bit):
Dictates whether the SYNC pin is an input or an output. Upon RESET, this bit is cleared.

M/S = 0: Slave Mode	SYNC is an input which is used to trigger a conversion if SMDE = 11.
M/S = 1: Master Mode	SYNC is an output. At the beginning of every conversion, SYNC is high for 4 internal clocks.

Bit 12 (CK1X: clock select bit):
Selects whether the external clock will be divided by two or used directly as the internal clock. See Clock section for a detailed explanation.

CK1X = 0:	the external clock is divided by two and used as the internal clock. This is referred to as CLK Mode = 0.
CK1X = 1:	the external clock input is used directly as the internal clock. This is referred to as CLK Mode = 1.

Bit 5 (L/H: Low Byte/High Byte):
In non-DMA mode the L/H bit defines whether DAVB is deactivated by reading the Data Low Byte or Data High Byte. In DMA mode, the L/H bit defines the order in which the Low/High Data Bytes are presented to the data bus. DMA mode automatically deactivates DAVB after both bytes are read.

*non-DMA mode: DMA = 0

L/H = 0:	reading register 0 (Low Byte) will de-assert DAVB
L/H = 1:	reading register 1 (High Byte) will de-assert DAVB

*DMA mode: DMA = 1

L/H = 0:	the first read is the Data High Byte, and the second read is the Data Low Byte, then DAVB output is de-asserted
L/H = 1:	the first read is the Data Low Byte, and the second read is the Data High Byte, then DAVB output is de-asserted.

Bit 6 (DMA: DMA mode bit):
This bit allows both high and low bytes from the 13 bit conversion to be read from one address; either Data Buffer Low Byte or Data Buffer High Byte registers.

DMA = 0	The high byte of the conversion will always be read from the Data Buffer High Byte register and the low byte of the conversion will always be read from the Data Buffer Low Byte Register.
DMA = 1:	Both high and low bytes of the conversion can be read from either the Data Buffer High or Low Byte Registers. A DMA controller, microprocessor, or other I/O device can use a single I/O address to read both the low and high bytes of the conversion. The order in which the high and low data bytes are presented is defined by the L/H control bit.

Note: This feature is not restricted to DMA controllers. It is an I/O option which may be used by a DMA controller, microprocessor, or any other type of I/O device.

Bit 7 (Reserved by Micro Linear)
This bit is not used. When written use zero.

GENERAL OPERATING INFORMATION

CONVERSION-START PROTOCOL

There are four different ways to start a conversion. They are defined by SMDE bits 4 and 5 in the Control Low Byte Register.

SMDE
Bits 5,4

00: A write to register 0 will start a conversion. During a conversion, if another write is issued to register 0, the "Start Conversion" command will be latched and another conversion will immediately follow the current one. To insure that the second write will be latched, it must occur at least 3 internal clocks after the first write. Only one additional write will be latched; multiple writes within a conversion will only yield one more conversion.

01: Reading the data from the previous conversion starts the next conversion. Start Conversion upon reading register 0 if L/H = 0, or Start Conversion upon reading register if L/H = 1. In DMA mode both bytes need to be read. The second byte read will Start the Conversion.

10: This mode causes continuous conversions; the next conversion begins immediately after the previous conversion ends. Writing to register 0 will start the first conversion; thereafter the converter runs continuously. This mode yields the maximum conversion rate.

11: The SYNC input triggers the start of a conversion. The M/S bit in the Control High Byte Register must be cleared, placing the chip in the slave mode.

Note: the external activation for Start Modes 0, 1, and 3 are synchronized internally to the system clock. If periodic sampling is required using these Start Modes, the SYNC, $\overline{RD}$, or $\overline{WR}$ pulses must be synchronized to the system clock. Start Mode 2 guarantees periodic sampling.

DOUBLE-BUFFERED DATA REGISTER

The A/D conversion result is double-buffered using the Data Buffer registers and the A/D Data register. The actual End-Of-Conversion (EOC) does not correspond with the DAVB output going low. The DAVB output goes low 16 internal clocks after the EOC. From the time DAVB output goes LOW, the user has one full conversion time (80 or 110 internal clocks) minus 16 internal clocks to read two data bytes as shown in Figure 10.

SELF CALIBRATION

Setting the DOCAL bit issues a calibration request to the chip. When calibration is done, the DAV status bit is set and the DAVB output goes low.

A calibration requires 8,260 internal clocks. Using a 7MHz clock (CLK Mode = 0), this approximately 2 ms. Power supplies and external voltage reference must be stable before issuing a request for calibration.

The ML2230 should be calibrated before any conversions are attempted. Calibrations must not be performed simultaneously with conversions. Before requesting a calibration, the user may want to read the Busy status bit to make sure that the converter is idle. Polling the chip while the calibration is in progress is not recommended.

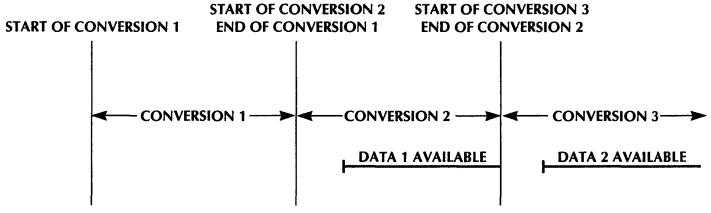


Figure 10.

CLOCK

The ML2230 has the option of dividing the clock at the CLK pin by 2, or using it directly to drive the internal logic. This option is selected through the CK1X bit in the Control register. When CK1X = 0 the clock is divided by 2. This is referred to as CLK Mode = 0. The clock at the CLK pin is referred to as the External clock, and the Internal Clock is the External clock divided by 2. When CK1X = 1, the clock at the CLK pin drives the internal logic directly, therefore this clock is referred to as the Internal clock. This is also known as CLK Mode = 1. All internally clocked logic is positive edge triggered.

CLK Mode = 0:

There are two advantages to CLK Mode 0. This is the only Mode that allows an external crystal to be used. CLK Mode 1 cannot operate with an external crystal, the CLK pin must be driven. The second advantage of CLK Mode 0 is that the duty cycle for a driven clock is less stringent than in CLK Mode 1. (Refer to t_{CLK0} and t_{CLK1} in AC Electrical Characteristics for CLK Mode 0 and 1 timing requirements, respectively.)

On power up the state of the divide by two flip-flop is indeterminate. Therefore the relationship between the internal clock and the external clock at the CLK pin can have one of two possibilities as shown in Figure 11. As a result the following should be considered.

t_{WRCK}, t_{RDCK}, and t_{SYNCCK} specs, ($\overline{RD}$, $\overline{WR}$, and SYNC setup times to Start of Conversion), will be as shown in the data sheet, or the data sheet specs plus one external clock period. Since these specifications are with respect to the rising edge of the external clock, it is not known whether this rising edge corresponds to the rising edge or falling edge of the internal clock. Therefore there is an uncertainty of one external clock period.

If periodic sampling is necessary and Start Mode 0, 1 or 3 is used, the external start pulse (either $\overline{RD}$, $\overline{WR}$, or SYNC) must be synchronous to the external clock, meet the setup time, and be an even number of external clock periods. If the start pulse were an odd number of external periods, half the pulses would correspond with the rising edge of the internal clock, and the other half would correspond with the falling edge of the internal clock. Therefore the sampling period would change by one external clock period every sample. Start Mode 2 guarantees periodic sampling regardless of the CLK mode.

CLK Mode = 1:

This mode eliminates the requirement that external start pulses must be an even number of external clock periods. However periodic sampling still requires that the start pulse be synchronous to the external clock, and the setup time must be met. CLK Mode 1 also eliminates the uncertainty of the t_{WRCK}, t_{RDCK} and t_{SYNCCK} requirements.

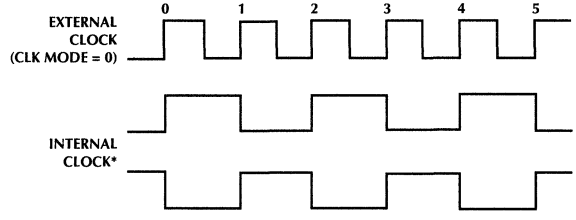


Figure 11.

DIAGNOSTICS

Diagnostics routines may be run after power up or any other time to ensure proper operation. The diagnostic features, which are software selectable, don't require external hardware. Both the analog and digital sections can be tested.

The ML2230 is placed in the diagnostic mode via the TMDE field in the Control High Byte Register. Once the ML2230 is placed in one of the diagnostic modes, a conversion must be executed before the results can be read. As with all conversions, DAVB will be activated upon completion.

ANALOG CONVERSION DIAGNOSTICS

TMDE = 000: Normal Operation
Selects normal A/D conversion. Default condition after a software reset.

TMDE = 001: Reserved by Micro Linear.

TMDE = 0101: CALWR operation
The data in Write register 0 and 1 (CALCODE Holding Register), are transferred into the converter's Calibration register when a "Start Conversion" is issued. A dummy conversion occurs and the DAVB output goes LOW to indicate that the operation is complete.

TMDE = 011: CALRD operation
The contents of the Calibration register are transferred through the A/D Data register and loaded into the Data Buffer register. A dummy 8-bit conversion occurs and DAVB output goes LOW to indicate that the CALRD operation is complete.

TMDE = 100: System Offset
The positive and negative inputs to the Sample and Hold are tied to analog ground. With this setting, converted data will give the offset of the A/D converter and Sample/Hold combination. The $V_{IN}+$ and $V_{IN}-$ pins will remain in a high impedance state while in this mode.

TMDE = 101: Common-mode
Both the positive and negative inputs of the Sample and Hold are tied to V_{REF}. The results of a conversion in this test mode indicates how well the converter is rejecting a common mode signal.

TMDE = 110: Positive Full Scale
This test mode connects the positive input of the Sample and Hold to V_{REF} and the negative input of the Sample and Hold to analog ground. The result of converting in this test mode is a value near positive full scale.

TMDE = 111: Negative Full Scale
This test mode connects the positive input of the Sample and Hold to analog ground and the negative input to V_{REF}. The result of converting in this test mode is a value near negative full scale.

DIGITAL LOOPBACK

The ML2230's architecture provides a way for the microprocessor to indirectly read and write to the A/D converter's calibration register and data register via a CALRD and CALWR. Figure 12 illustrates this architecture. This in effect allows a digital loopback.

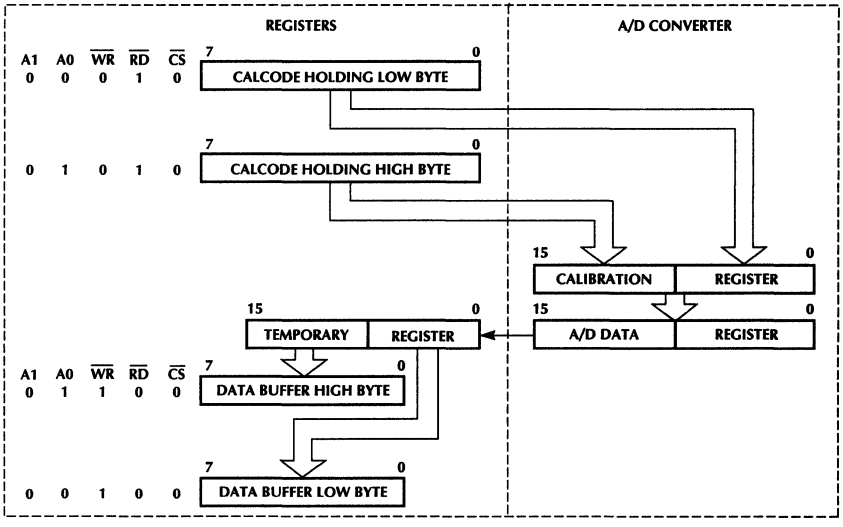


Figure 12. Digital Loopback

When the TMDE bits are set to 010 CAL WRITE (CALWR), and a Start Conversion is issued in any one of the four modes, the contents of the CALCODE Holding Low Byte and High Byte registers are transferred into the A/D converter's Calibration register. When the TMDE bits are set to 011 CAL READ (CALRD), and a Start Conversion is issued, the contents of the Calibration register are transferred through the A/D's Data register into the Data Buffer Low Byte and Data Buffer High Byte registers. The result of these two operations is a complete loopback from the CALCODE Holding registers through the A/D converter and back into the Data buffer registers. This loopback provides user assurance that all the paths are clear and there are no stuck bits.

Note: When a CALWR is done, the previous calibration value is lost. The correct calibration value must be restored before the converter is used to convert data.

CALIBRATION PASS/FAIL TEST

The CALRD can be used as a way to verify a successful calibration. After a calibration is completed, the CALRD may be issued in order to read the contents of the Calibration register. If the Low Byte of the data buffer register is all ones after executing a CALRD, the calibration failed; otherwise the calibration is successful.

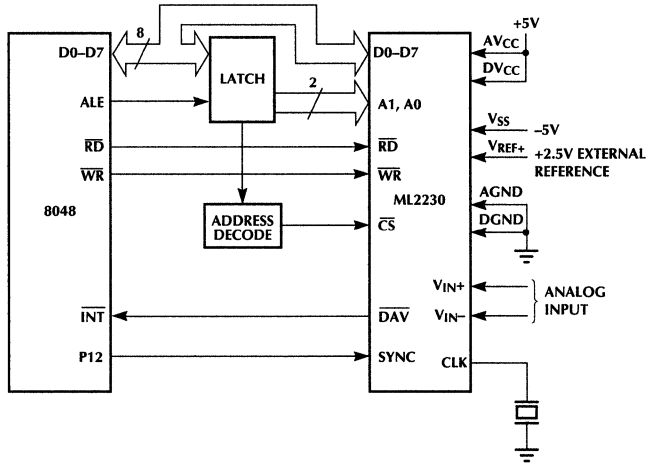


Figure 13. Interfacing to 8048 Microcontroller

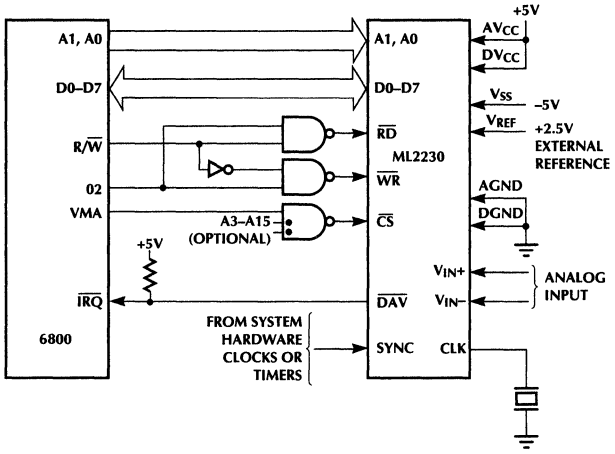


Figure 14. Interfacing to 6800 Microprocessor

2

ORDERING INFORMATION

PART NUMBER	LINEARITY ERROR	MINIMUM CONVERSION	TEMPERATURE RANGE	PACKAGE
ML2230BCP	±3/4 LSB	31.5µs	0°C to +70°C	Plastic DIP (P24)
ML2230CCP	±1 LSB	31.5µs	0°C to +70°C	Plastic DIP (P24)
ML2230DCP	±1 LSB	44.0µs	0°C to +70°C	Plastic DIP (P24)

µP Compatible 12-Bit Plus Sign A/D Converter with Sample and Hold

GENERAL DESCRIPTION

The ML2233 is a member of Micro Linear's 12-bit plus sign CMOS A/D converter family utilizing a self calibrating algorithmic technique. The sample-and-hold, incorporated on the ML2233, has a differential input for noise immunity and power supply rejection. All errors of the sample-and-hold are accounted for in the analog-to-digital converter's accuracy specification.

The ML2233B has a maximum non-linearity error over temperature of 0.018% of full-scale, and the ML2233C and ML2233D have a maximum non-linearity error over temperature of 0.024% of full scale.

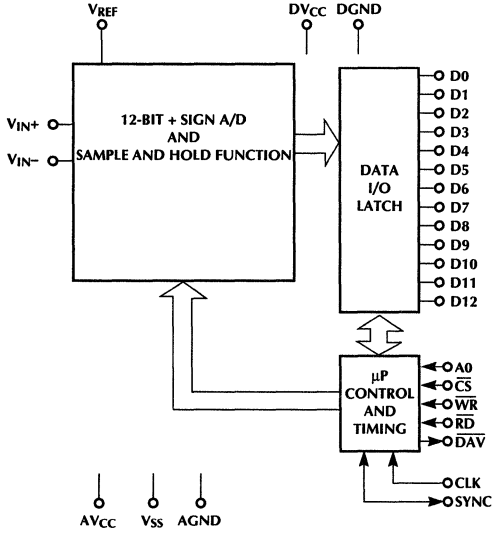
Designed to interface to a 16-bit microprocessor bus without additional components, the ML2233 outputs the 13-bit data result in one word. Data format is 2's complement. All digital signals are fully TTL and CMOS compatible.

For interfacing to an 8-bit microprocessor bus the ML2230 provides a 13-bit data result in two 8-bit bytes.

FEATURES

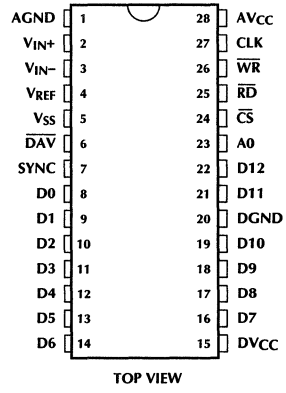
- Resolution 12-bits + sign
- Conversion time (including S/H acquisition) 31.5µs max
- Sample and hold acquisition 2.3µs max
- Non-linearity error ±3/4LSB and ±1LSB max
- Low harmonic distortion 0.01%
- No missing codes
- Self calibrating — maintains accuracy over time and temperature
- Inputs withstand |7V| beyond supplies
- Data transfer options — interrupt, DMA, or polling
- 13-bit result for 16-bit bus interface
- Standard 28-pin DIP

BLOCK DIAGRAM



PIN CONNECTIONS

ML2233
28-Pin DIP (P28)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	AGND	Analog ground.
2	$V_{IN}+$	Positive differential analog input; range = $V_{SS} \le V_{IN}+ \le AV_{CC}$, $\lvert(V_{IN}+) - (V_{IN}-)\rvert \le V_{REF}$.
3	$V_{IN}-$	Negative differential analog input; range = $V_{SS} \le V_{IN}- \le AV_{CC}$, $\lvert(V_{IN}+) - (V_{IN}-)\rvert \le V_{REF}$.
4	V_{REF}	Voltage reference input; referenced to analog ground.
5	V_{SS}	Negative power supply; decouple to AGND.
6	$\overline{DAV}$	Data available; indicates a conversion has completed and data is available or calibration completed.
7	SYNC	In the slave mode, SYNC is a positive edge triggered input used to start a conversion. In master mode, SYNC is an output and indicates conversion start.
8	D0	Bidirectional data bit.
9	D1	Bidirectional data bit.
10	D2	Bidirectional data bit.
11	D3	Bidirectional data bit.
12	D4	Bidirectional data bit.
13	D5	Bidirectional data bit.
14	D6	Bidirectional data bit.
15	DV_{CC}	Digital power supply.
16	D7	Bidirectional data bit.
17	D8	Bidirectional data bit.
18	D9	Bidirectional data bit.
19	D10	Bidirectional data bit.
20	DGND	Digital ground.
21	D11	Bidirectional data bit.
22	D12	Bidirectional data bit.
23	A0	Address for the microprocessor interface to access registers.
24	$\overline{CS}$	Chip select; enables writing to or reading from.
25	$\overline{RD}$	Read; enables ML2233 to drive data bus.
26	$\overline{WR}$	Write; allows writing into the registers.
27	CLK	Clock input. Driven with an external clock or crystal referenced to DGND. The crystal must be parallel resonant with minimum capacitive loading. (i.e., no bypass caps should be used and leads should be kept short.)
28	AV_{CC}	Positive analog power supply. Decouple to AGND. Tie to DV_{CC} from same power supply.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages (AV_{CC} and DV_{CC}) 6.0V
Negative Supply Voltage (V_{SS}) ..... –6.0V
Voltage at Analog
Inputs ..... V_{SS} – 7V to AV_{CC} + 7V
Voltage at V_{REF} ..... V_{SS} – 7V to AV_{CC} + 7V
Input Current per Digital Pin ..... ±10mA
Input Current at Analog Inputs ..... ±20mA
Storage Temperature Range ..... –65°C to +150°C
Package Dissipation @ 25°C 875mW
Lead Temperature (soldering, 10 seconds)
Dual-In-Line Package (Plastic) ..... 260°C

OPERATING CONDITIONS

(Note 2)

Temperature Range ..... 0°C to 70°C
Supply Voltage (AV_{CC} and DV_{CC}) ..... $4.5V_{DC}$ to $6.0V_{DC}$
Negative Supply Voltage (V_{SS}) ..... $-4.5V_{DC}$ to $-6.0V_{DC}$
Reference Voltage (V_{REF}) 2.60V

ELECTRICAL CHARACTERISTICS

The following specifications apply for AV_{CC} = DV_{CC} = 5V ± 5%, V_{SS} = –5V ± 5%, V_{REF} = 2.500V, V_{IN}– = AGND, V_{IN}+ = –2.5V to +2.5V, T_A = T_{MIN} to T_{MAX} unless otherwise specified.

PARAMETER	NOTES	CONDITIONS	TYP MIN	(NOTE 3)	MAX	UNITS
Converter Characteristics						
Linearity Error						
ML2233BCJ	4	f_{CCLK} = 0.1 ≤ 7MHz			±3/4	LSB
ML2233CCJ		f_{CCLK} = 0.1 ≤ 7MHz			±1	LSB
ML2233DCJ		f_{CCLK} = 0.1 ≤ 5MHz			±1	LSB
Unadjusted Zero Error						
ML2233BCJ	4				±3/4	LSB
ML2233CCJ					±2	LSB
ML2233DCJ					±2	LSB
Unadjusted Positive and Negative Full Scale Error	5				±4	LSB
Zero Error Temperature Coefficient				0.5		ppm/°C
Gain Temperature Coefficient				10		ppm/°C
Common-Mode Rejection	5, 6		80			dB
Analog Input Source Resistance	5				2	kΩ
Analog Input Range	4	V_{IN}+ Referred to V_{IN}–	–V_{REF}		+V_{REF}	V
Analog Input Leakage Current	4				100	nA
Voltage Reference Input Source Impedance	5				0.5	kΩ
Reference Input Leakage Current	4				100	nA
Digital and DC Characteristics						
Power Supply Current						
AI_{CC}, Analog V_{CC}	4			30	50	mA
DI_{CC}, Digital V_{CC}				10		µA
I_{SS}, V_{SS}				18	30	mA
Power Supply Rejection	7					
AV_{CC}		DC		80		dB
		DC to 25kHz		50		dB
V_{SS}		DC		80		dB
		DC to 25kHz		50		dB
V_{ILCLK}, Clock Input Low Voltage	4				0.8	V
V_{IHCLK}, Clock Input High Voltage	4		3.5		AV_{CC}	V
I_{L1}, Input Leakage Current (CLK)	4	AGND ≤ V_{IN} ≤ AV_{CC}			±200	µA
V_{IL}, Input Low Voltage	4				0.8	V
V_{IH}, Input High Voltage	4		2.0		DV_{CC}	V
V_{OL}, Output Low Voltage	4	I_{OL} = 2.0mA			0.45	V
V_{OH}, Output High Voltage	4	I_{OH} = –400µA	2.4			V
I_L, Input Leakage Current (except CLK)	4	AGND ≤ V_{IN} ≤ AV_{CC}			±10	µA
I_{HI-Z}, Output Leakage Current (D0–D12)	4	$\overline{RD}$ = $\overline{CS}$ = V_{IH}			±10	µA
C_I, Input Capacitance (all digital inputs)				10		pF
C_O, Output Capacitance (outputs D0 to D12, SYNC and $\overline{DAV}$)				10		pF

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	NOTES	CONDITIONS		MIN	TYP (NOTE 3)	MAX	UNITS
AC Electrical Characteristics (Note 8)								
t_C	Conversion Time	4, 9	CLK Mode = 0	f_{CLK} = 7.0MHz f_{CLK} = 5.0MHz	31.5 44.0			µs µs
	Sample and Hold Acquisition	4, 9	CLK Mode = 0	f_{CLK} = 7.0MHz f_{CLK} = 5.0MHz			2.3 3.2	µs µs
f_{CLK0}	Clock Frequency	5, 9	CLK Mode = 0	Crystal Driven	3 1		7 7	MHz MHz
f_{CLK0}	Clock Width	5, 9	Driven (CLK Mode = 0)	High Low	50 50			ns ns
f_{CLK1}	Clock Frequency	5, 10	Driven (CLK Mode = 1)		0.5		(Note 11)	MHz
t_{CLK1}	Clock Width	5, 10	Driven (CLK Mode = 1)	High Low	125 125			ns ns
t_{AD}	Address Stable to Valid Data	4			150			ns
t_{AR}	Address Stable Before Read	4			0			ns
t_{RA}	Address Hold After Read	4			0			ns
t_{RR}	Read Pulse Width	4			150			ns
t_{RD}	Read Access	4					150	ns
t_{1Z}, t_{0Z}	Data Read to Hi-Z	4			0		50	ns
t_{RV}	Recovery Between Two Reads or Writes	5			250			ns
t_{RDCK}	Read to Clock Setup Time	5, 12			40			ns
t_{AW}	Address Stable Before Write	4			0			ns
t_{WA}	Address Hold After Write	4			0			ns
t_{WW}	Write Pulse Width	4			150			ns
t_{DW}	Data Setup Before Write Trailing Edge	4			100			ns
t_{WD}	Data Hold After Write Trailing Edge	4			0			ns
t_{WRCK}	Write to Clock Setup Time	5, 12			40			ns
t_{CKDAV}	Clock to $\overline{DAV}$ Assert	4, 13	C_L = 50pF			120	220	ns
t_{SYNCCK}	SYNC Input to Clock Setup	5, 12			40			ns
t_{SYNCN}	SYNC Input Width	5	(CLK Mode = 0) (CLK Mode = 1)		6 3			$1/f_{CLK0}$ $1/f_{CLK1}$

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP (NOTE 3)	MAX	UNITS
AC Electrical Characteristics (Note 8)							
t_{CKSYNC}	External Clock to SYNC Output Delay	5, 13	C_L = 50pF		150	200	ns
t_{SYNCO}	SYNC Output Pulse Width	5, 13	(CLK Mode = 0) (CLK Mode = 1)			8 4	$1/f_{CLK0}$ $1/f_{CLK1}$
t_{WRDAV}	Write Reg2 to $\overline{DAV}$ Rising Edge	4, 14	C_L = 50pF			170	ns
t_{RDDAV}	Read Reg0 to $\overline{DAV}$ Rising Edge	4, 15	C_L = 50pF			170	ns
t_r, t_f	Rise and Fall		All Inputs			25	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Devices are 100% tested with temperature limits guaranteed by 100% testing, sampling or by correlation with worst-case test conditions.
Note 3: Typicals are parametric norm at 25°C
Note 4: Parameter guaranteed and 100% production tested.
Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.
Note 6: Common mode rejection is the ratio of the change in zero error to the change in common mode input range
Note 7: Power supply rejection is the ratio of the change in zero error to the change in power supply voltage.
Note 8: All parameters measured from 0.8V to 2.0V, C_L = 100pF.
Note 9: CK1X bit in control register = 0.
Note 10: CK1X bit in control register = 1.
Note 11: Maximum frequency is $1/t_{CLK1}$ (high) + t_{CLK1} (low) + rise + fall times and ≤ 3.5MHz.
Note 12: Setup time required for synchronous start of conversion.
Note 13: In CLK mode = 0 (CK1X bit in control register = 0) start of conversion will occur at specified time; or time plus one f_{CLK0} period (see Figure 5)
Note 14: Writing a control register bit 0 with a one will acknowledge the $\overline{DAV}$ condition and de-assert DAV output
Note 15: In start mode = 1, a read from location "0" will start the next conversion and de-assert the DAV output

TIMING DIAGRAMS

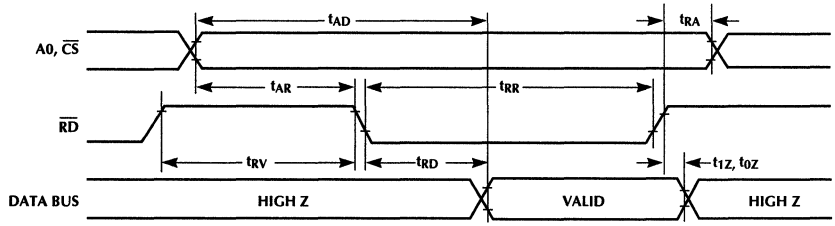


Figure 1. Read Cycle

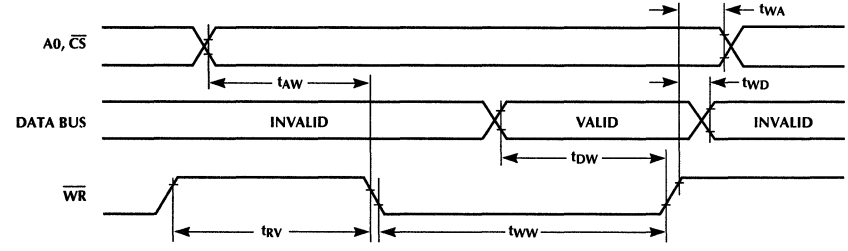
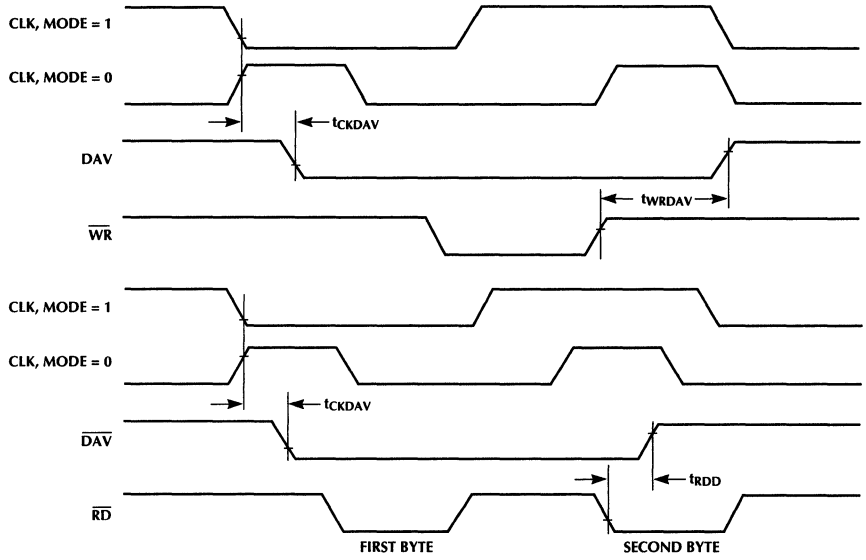


Figure 2. Write Cycle

TIMING DIAGRAMS (Continued)



DAV IS SET AND CLEARED BY INTERNAL CIRCUITRY.
NOTE: DMA BIT IN THE CONTROL REGISTER MUST BE SET FOR THIS OPERATION.

Figure 3. Data Available

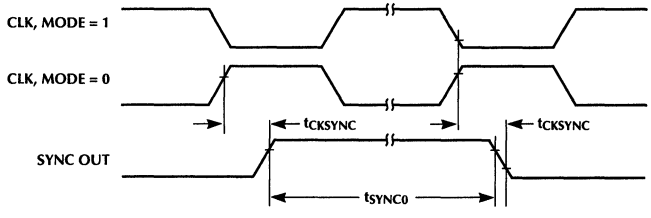
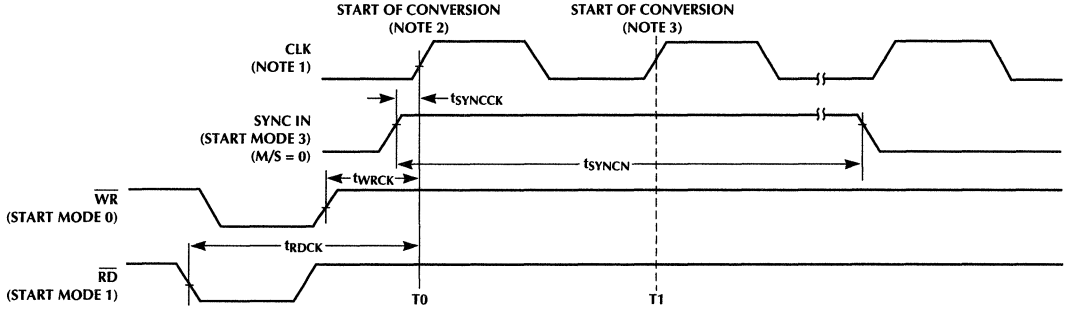


Figure 4. SYNC Output

TIMING DIAGRAMS (Continued)



NOTES:
1. CLK IS THE CLOCK DRIVEN AT THE CLOCK PIN.
2. IN CLK MODE 1, WILL ALWAYS OCCUR AT T0 IF SETUP TIMES ARE MET.
3. IN CLK MODE0, WILL OCCUR EITHER AT T0 OR T1 IF SETUP TIMES ARE MET.

Figure 5. Synchronous Start of Conversion (Start Mode 0, 1, 3)

BLOCK DIAGRAM

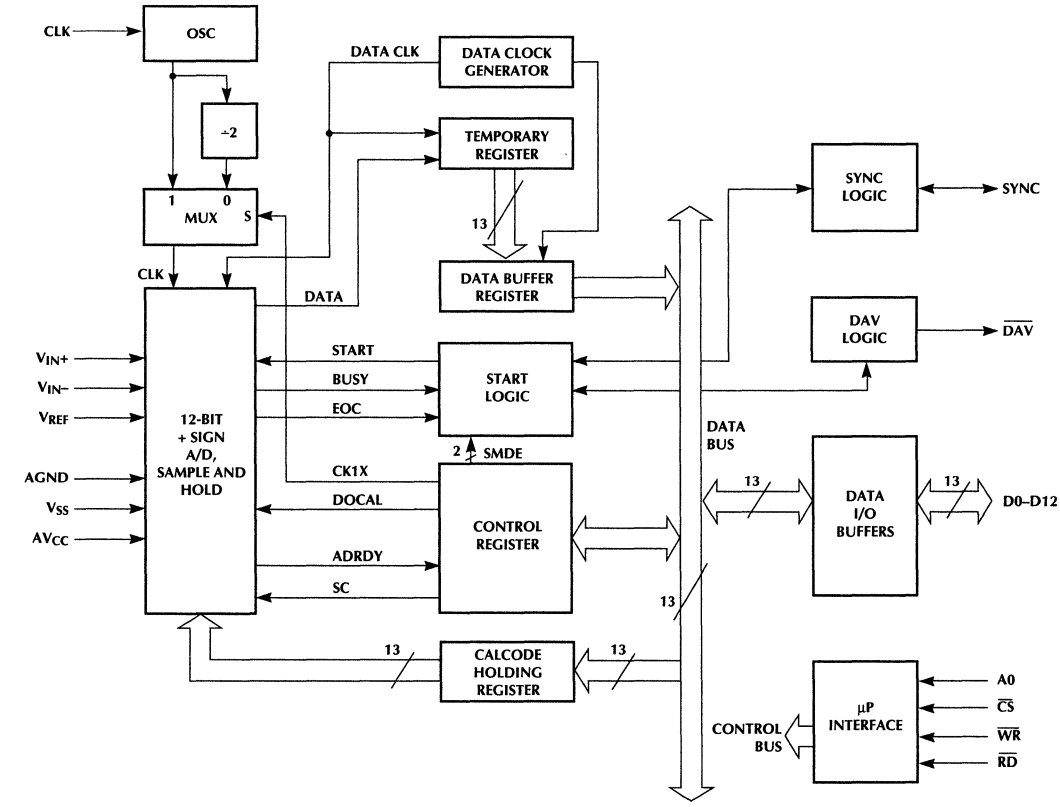


Figure 6. Block Schematic Diagram

FUNCTIONAL DESCRIPTION

ALGORITHMIC A/D CONVERTER

Micro Linear's algorithmic converter uses a successive approximation technique. Most of today's successive approximation converters use a DAC to feedback the approximated signal, however this technique requires more circuitry than algorithmic converters. In addition the values of all of the resistors or capacitors in the DAC must be matched to within the accuracy of the converter. This is difficult to do in silicon beyond 10 bits unless trimming is used. An algorithmic converter uses less circuitry and is more easily trimmed. Micro Linear's algorithmic converter is implemented using a 2x amplifier, a sample/hold amp, and a comparator as shown in Figure 7.

The input sample is first multiplied by two then compared to the reference voltage. If the 2x input voltage is greater than the reference, the MSB is a 1 and the reference voltage is subtracted from the 2x input voltage. The remainder is stored in the sample and hold. If the 2x input voltage is less than the reference, the MSB is a 0 and the 2x input voltage is stored in the sample and hold. This process repeats again, however now the sample and hold voltage is multiplied by 2.

The algorithm involves multiplication by 2, comparison, and possibly subtraction. Referring to Figure 6, the algorithm for the circuit can be described as follows:

Step 1 If $(2 \times V_{IN}) - V_{REF} \geq 0$
then MSB = 1
$(2 \times V_{IN}) - V_{REF} \rightarrow S/H$
else MSB = 0
$(2 \times V_{IN}) \rightarrow S/H$

Step 2 If $(2 \times S/H) - V_{REF} \geq 0$
then next bit = 1
$(2 \times S/H) - V_{REF} \rightarrow S/H$
else next bit = 0
$(2 \times S/H) \rightarrow S/H$

Step 3 Repeat Step 2 until conversion complete.

Since the A/D converter handles bipolar inputs, negative inputs are handled slightly differently using the same principle.

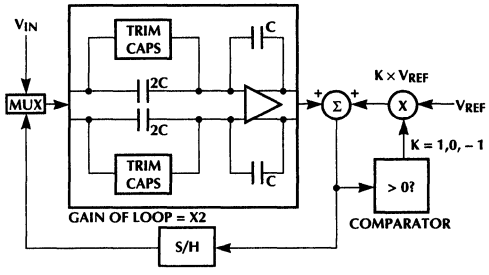


Figure 7. Self Calibrating A/D Converter

SELF CALIBRATION

In order to maintain integral and differential linearity to the 1/2 LSB level in an algorithmic converter, two critical parameters need to be controlled, loop offsets and the gain of the loop. Loop offsets are automatically nulled before each conversion using auto-zeroing circuitry on both the sampling amp and the 2x amp. The gain of the loop is adjusted using self calibration.

Self calibrating the algorithmic converter, once the offsets have been nulled, is performed by measuring the 2x gain of the loop and adjusting it. The gain can be measured by converting the reference voltage as the input as well as the reference (V_{REF}/V_{REF}), and examining the output code. Converting V_{REF} should yield plus full scale, since V_{REF}/V_{REF} should equal 1. If the gain of the loop is slightly less than 2, the resulting LSB of the conversion will be "0". If the magnitude bits of the resulting conversion are all "1s", the gain may be too great, therefore the gain is reduced to the point where the threshold of the LSB is reached.

Adjustment of the 2x gain is done with the binary weighted trim capacitor arrays connected to each of the 2C input capacitors. A small value of capacitance is either added to or subtracted from the 2C input caps until the gain of the loop is within 13 bit accuracy of 2.

CONVERSION TIMES

The following table lists the conversion times which include the sample and hold acquisition time. For a CALRD and CALWR no A/D conversion actually takes place.

OPERATION	# OF INTERNAL CLOCKS*
8 bit A/D	80
13 bit A/D	110
CALWR	52
CALRD	80

SAMPLE AND HOLD TIMING

Figure 8 shows the internal timing for the sample and hold circuitry. The relationship between the "Start of Conversion" and the input channel going into sample mode is fixed at 6 internal clocks*, regardless of the Start Mode. Six internal clocks after the Start of Conversion the Sample and Hold is switched into the sample mode, placing two 9pF capacitors in parallel with the inputs pins; one on $V_{IN}+$ and one on $V_{IN}-$. The sample switch is kept in the sample mode for 8 internal clocks (2.3µs at a 7MHz external clock), then placed in the hold mode. During the next 2 internal clocks the charge on the sample and hold is transferred into the A/D, after which the V_{REF} pin is sampled for 8 internal clocks.

Figure 8 also illustrates the timing of the SYNC pin in Master Mode during a conversion (M/S = 1 Control register) and Start Mode 0, 1, or 2. SYNC is activated one internal clock cycle after the Start of Conversion and lasts for four internal clocks.

*For a description of internal clocks see Clock section.

ANALOG INPUTS

Differential Inputs and Common Mode Rejection

The differential inputs of the ML2233 eliminate the effects of common mode input noise (60Hz for example), as $V_{IN}+$ and $V_{IN}-$ are sampled at the same time.

Noise

The leads to the analog inputs should be kept as short as possible to minimize output noise. Noise as well as digital clocks can couple into the inputs and cause errors. Input filters can be used to reduce the effects of these sources.

Power Supply Decoupling

Low inductance tantalum capacitors of 1µF or greater and 0.01µF disc ceramic capacitors are recommended for bypassing AV_{CC} as well as V_{SS} to AGND. These capacitors should be placed close to the AV_{CC} and V_{SS} pins.

MICROPROCESSOR INTERFACE

There are two 13-bit directly addressable registers; a Data Buffer register and a Control register. The data buffer register provides the conversion results. The data register is double buffered, allowing one result to be read while the next sample is being converted. The data register also allows access to the algorithmic converter's calibration code. Normally the ML2233 is operated without ever accessing these registers. (Refer to Diagnostics for more information). The Control register provides complete control and status information. The two registers are addressed by pin A0.

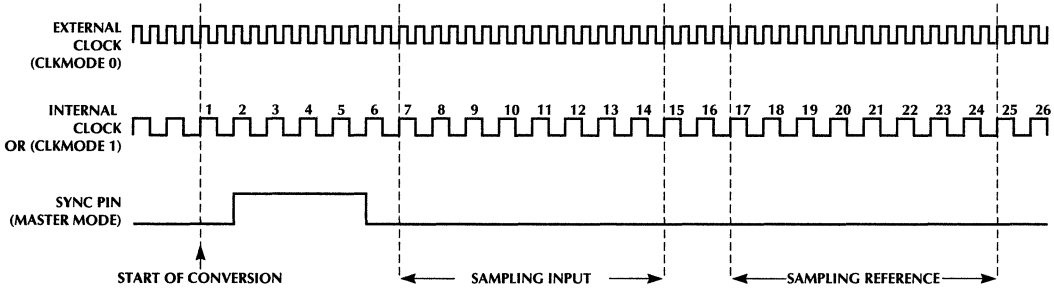


Figure 8. Sample and Hold Timing

All data is returned from the converter in two's complement format.

Cycle	+Max	–Min	Zero
13	0FFF	1000	0000
8	007F	1F80	0000

REGISTER DESCRIPTION

REGISTER 0 — DATA BUFFER:

Register 0 contains the results of the latest conversion when read. Depending on the Start Mode selected, reading or writing to this register may start the next conversion.

REGISTER 1 — CONTROL REGISTER

Bit 0 (DAV status when READ/DAVACK acknowledge when a ONE is written):
Reading DAV = 1 indicates that new data is available or a calibration is complete. DAV will be cleared automatically when the data is read. This bit can be explicitly acknowledged by writing a ONE to it; writing a zero has no effect. The $\overline{DAV}$ output pin always reflects the DAV status bit.

Bit 1 (BUSY status when READ/RESET when a ONE is written):
Reading BUSY = 1 indicates that a conversion or calibration is in progress. Writing a ONE will force a chip reset. Writing a zero has no effect.

RESET DEFAULT CONDITIONS:

The Control register will automatically be cleared. The Data Buffer register will be unchanged. The Calibration register is not cleared after a reset, however the ADRDY bit is cleared. Since the DAV status bit is cleared, the $\overline{DAV}$ output is inactivated (high). The SYNC pin is forced to be an input as a result of clearing the M/S bit in the Control register.

Bit 2 (ADRDY status when READ/DOCAL request when a ONE is written):

Reading ADRDY = 0 indicates that the converter has not been calibrated since the last reset, and ADRDY = 1 indicates that is has been calibrated since the last reset. Writing a ONE will force the converter to do a calibration; writing a zero has no effect.

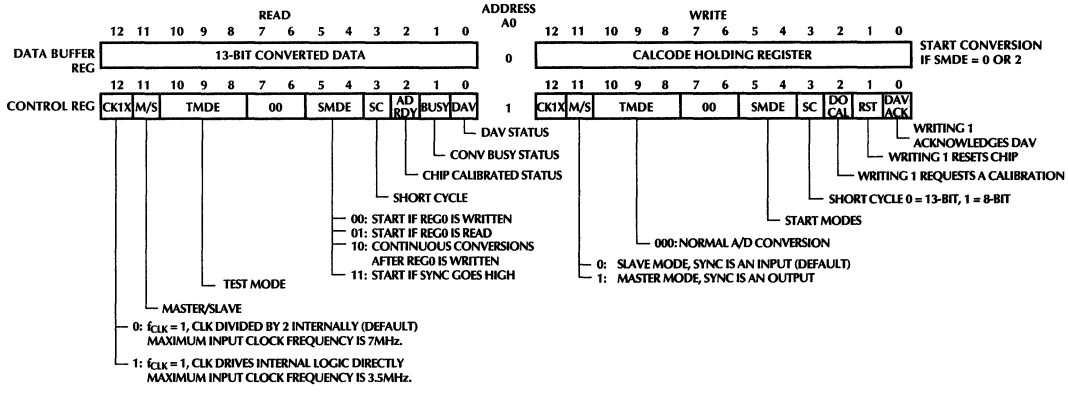


Figure 9. Register Description

Bit 3 (SC: Short cycle select):
Selects 8 or 13 bit conversions.

SC = 0: 13-bit conversion (default)
SC = 1: 8-bit conversion (short cycle)

Bits 4,5 (SMDE: Start Mode):
Defines Start Conversion mode.

Bits 5,4

00	Start Conversion upon writing to register 0 (default)
01	Start Conversion upon reading register 0
10	Start Continuous Conversions upon writing to register 0.
11	Start on external SYNC input going high (Requires Slave mode: M/S = 0)

Bits 7,6 (reserved):
These bits are reserved by Micro Linear and must be written as zero.

Bits 10,9,8 (TMDE: test mode select bits)
These bits are used for diagnostic purposes only and normally not accessed during operation. The default value of TMDE is 000 which selects a normal A/D conversion. See Diagnostics for more information.

TMDE	Description
000	Normal A/D Conversion
001	Reserved by Micro Linear (Do Not Use)
010	CALWR Operation
011	CALRD Operation
100	System Offset
101	Common-mode
110	Plus Full Scale
111	Minus Full Scale

Bit 11 (M/S: Master/Slave bit):
Dictates whether the SYNC pin is an input or an output. Upon RESET, this bit is cleared.

M/S = 0: Slave Mode	SYNC is an input which is used to trigger a conversion if SMDE = 11.
M/S = 1: Master Mode	SYNC is an output. At the beginning of every conversion, SYNC is high for 4 internal clocks.

Bit 12 (CK1X: clock select bit):
Selects whether the external clock will be divided by two or used directly as the internal clock. See Clock section for a detailed explanation.

CK1X = 0:	the external clock is divided by two and used as the internal clock. This is referred to as CLK Mode = 0.
CK1X = 1:	the external clock input is used directly as the internal clock. This is referred to as CLK Mode = 1.

GENERAL OPERATING INFORMATION

CONVERSION-START PROTOCOL

There are four different ways to start a conversion. They are defined by SMDE bits 4 and 5 in the Control Register.

SMDE
Bits 5,4

00: A write to register 0 will start a conversion. During a conversion, if another write is issued to register 0, the "Start Conversion" command will be latched and another conversion will immediately follow the current one. To insure that the second write will be latched, it must occur at least 3 internal clocks after the first write. Only one additional write will be latched; multiple writes within a conversion will only yield one more conversion.

01: Reading the data from the previous conversion starts the next conversion.

10: This mode causes continuous conversions; the next conversion begins immediately after the previous conversion ends. Writing to register 0 will start the first conversion; thereafter the converter runs continuously. This mode yields the maximum conversion rate.

11: The SYNC input triggers the start of a conversion. The M/S bit in the Control Register must be cleared, placing the chip in the slave mode.

Note: the external activation for Start Modes 0, 1, and 3 are synchronized internally to the system clock. If periodic sampling is required using these Start Modes, the SYNC, $\overline{RD}$, or $\overline{WR}$ pulses must be synchronized to the system clock. Start Mode 2 guarantees periodic sampling.

DOUBLE-BUFFERED DATA REGISTER

The A/D conversion result is double-buffered using the Data Buffer register and the A/D Data register. The actual End-Of-Conversion (EOC) does not correspond with the $\overline{DAV}$ output going low. The $\overline{DAV}$ output goes low 16 internal clocks after the EOC. From the time $\overline{DAV}$ output goes LOW, the user has one full conversion time (80 or 110 internal clocks) minus 16 internal clocks to read the data as shown in Figure 10.

SELF CALIBRATION

Setting the DOCAL bit issues a calibration request to the chip. When calibration is done, the DAV status bit is set and the $\overline{DAV}$ output goes low.

A calibration requires 8,260 internal clocks. Using a 7MHz clock (CLK Mode = 0), this approximately 2 ms. Power supplies and external voltage reference must be stable before issuing a request for calibration.

The ML2233 should be calibrated before any conversions are attempted. Calibrations must not be performed simultaneously with conversions. Before requesting a calibration, the user may want to read the Busy status bit to make sure that the converter is idle. Polling the chip while the calibration is in progress is not recommended.

2

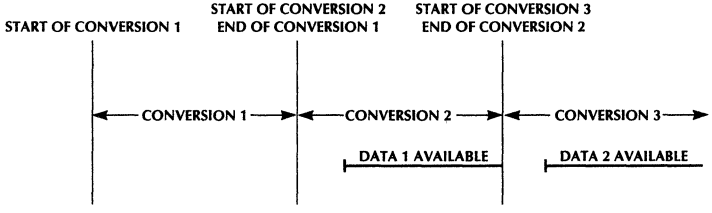


Figure 10.

CLOCK

The ML2233 has the option of dividing the clock at the CLK pin by 2, or using it directly to drive the internal logic. This option is selected through the CK1X bit in the Control register. When CK1X = 0 the clock is divided by 2. This is referred to as CLK Mode = 0. The clock at the CLK pin is referred to as the External clock, and the Internal Clock is the External clock divided by 2. When CK1X = 1, the clock at the CLK pin drives the internal logic directly, therefore this clock is referred to as the internal clock. This is also known as CLK Mode = 1. All internally clocked logic is positive edge triggered.

CLK Mode = 0:

There are two advantages to CLK Mode 0. This is the only Mode that allows an external crystal to be used. CLK Mode 1 cannot operate with an external crystal, the CLK pin must be driven. The second advantage of CLK Mode 0 is that the duty cycle for a driven clock is less stringent than in CLK Mode 1. (Refer to t_{CLK0} and t_{CLK1} in AC Electrical Characteristics for CLK Mode 0 and 1 timing requirements, respectively.)

On power up the state of the divide by two flip-flop is indeterminate. Therefore the relationship between the internal clock and the external clock at the CLK pin can have one of two possibilities as shown in Figure 11. As a result the following should be considered.

t_{WRCK}, t_{RDCK}, and t_{SYNCCK} specs, ($\overline{RD}$, $\overline{WR}$, and SYNC setup times to Start of Conversion), will be as shown in the data sheet, or the data sheet specs plus one external clock period. Since these specifications are with respect to the rising edge of the external clock, it is not known whether this rising edge corresponds to the rising edge or falling edge of the internal clock. Therefore there is an uncertainty of one external clock period.

If periodic sampling is necessary and Start Mode 0, 1 or 3 is used, the external start pulse (either $\overline{RD}$, $\overline{WR}$, or SYNC) must be synchronous to the external clock, meet the setup time, and be an even number of external clock periods. If the start pulse were an odd number of external periods, half the pulses would correspond with the rising edge of the internal clock, and the other half would correspond with the falling edge of the internal clock. Therefore the sampling period would change by one external clock period every sample. Start Mode 2 guarantees periodic sampling regardless of the CLK mode.

CLK Mode = 1:

This mode eliminates the requirement that external start pulses must be an even number of external clock periods. However periodic sampling still requires that the start pulse be synchronous to the external clock, and the setup time must be met. CLK Mode 1 also eliminates the uncertainty of the t_{WRCK}, t_{RDCK} and t_{SYNCCK} requirements.

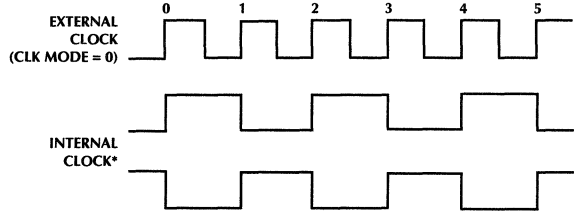


Figure 11.

DIAGNOSTICS

Diagnostics routines may be run after power up or any other time to ensure proper operation. The diagnostic features, which are software selectable, don't require external hardware. Both the analog and digital sections can be tested.

The ML2233 is placed in the diagnostic mode via the TMDE field in the Control Register. Once the ML2233 is placed in one of the diagnostic modes, a conversion must be executed before the results can be read. As with all conversions, $\overline{DAV}$ will be activated upon completion.

ANALOG CONVERSION DIAGNOSTICS

TMDE = 000: Normal Operation
Selects normal A/D conversion. Default condition after a software reset.

TMDE = 001: Reserved by Micro Linear.

TMDE = 0101: CALWR operation
The data in Write register 0 (CALCODE Holding Register), is transferred into the converter's Calibration register when a "Start Conversion" is issued. A dummy conversion occurs and the $\overline{DAV}$ output goes LOW to indicate that the operation is complete.

TMDE = 011: CALRD operation
The contents of the Calibration register are transferred through the A/D Data register and loaded into the Data Buffer register. A dummy 8-bit conversion occurs and $\overline{DAV}$ output goes LOW to indicate that the CALRD operation is complete.

TMDE = 100: System Offset
The positive and negative inputs to the Sample and Hold are tied to analog ground. With this setting, converted data will give the offset of the A/D converter and Sample/Hold combination. The $V_{IN}+$ and $V_{IN}-$ pins will remain in a high impedance state while in this mode.

TMDE = 101: Common-mode
Both the positive and negative inputs of the Sample and Hold are tied to V_{REF}. The results of a conversion in this test mode indicates how well the converter is rejecting a common mode signal.

TMDE = 110: Positive Full Scale
This test mode connects the positive input of the Sample and Hold to V_{REF} and the negative input of the Sample and Hold to analog ground. The result of converting in this test mode is a value near positive full scale.

TMDE = 111: Negative Full Scale
This test mode connects the positive input of the Sample and Hold to analog ground and the negative input to V_{REF}. The result of converting in this test mode is a value near negative full scale.

DIGITAL LOOPBACK

The ML2233's architecture provides a way for the microprocessor to indirectly read and write to the A/D converter's calibration register and data register via a CALRD and CALWR. Figure 12 illustrates this architecture. This in effect allows a digital loopback.

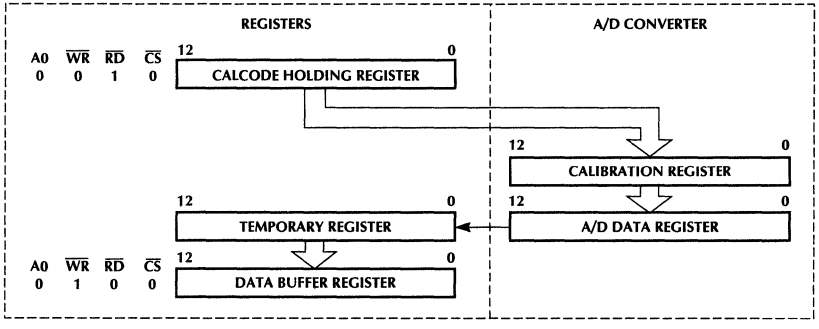


Figure 12. Digital Loopback

When the TMDE bits are set to 010 CAL WRITE (CALWR), and a Start Conversion is issued in any one of the four modes, the contents of the CALCODE Holding register is transferred into the A/D converter's Calibration register. When the TMDE bits are set to 011 CAL READ (CALRD), and a Start Conversion is issued, the contents of the Calibration register are transferred through the A/D's Data register into the Data Buffer register. The result of these two operations is a complete loopback from the CALCODE Holding register through the A/D converter and back into the Data buffer register. This loopback provides user assurance that all the paths are clear and there are no stuck bits.

Note: When a CALWR is done, the previous calibration value is lost. The correct calibration value must be restored before the converter is used to convert data.

CALIBRATION PASS/FAIL TEST

The CALRD can be used as a way to verify a successful calibration. After a calibration is completed, the CALRD may be issued in order to read the contents of the Calibration register. If the Low Byte (lower 8 bits) of the data buffer register are ones after executing a CALRD, the calibration failed; otherwise the calibration is successful.

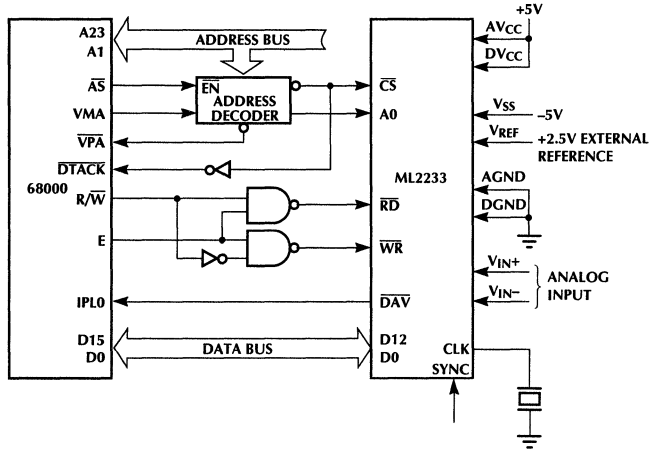


Figure 13. Interfacing to 68000 Microprocessor

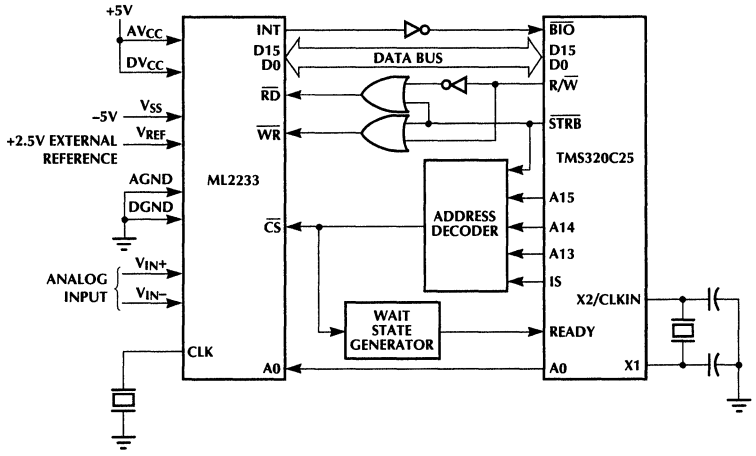


Figure 14. Interfacing to TMS320C25 Digital Signal Processor

2

ORDERING INFORMATION

PART NUMBER	MAXIMUM LINEARITY ERROR	MAXIMUM TOTAL UNADJUSTED ERROR	MINIMUM CONVERSION	PACKAGE
ML2233BCP	±3/4 LSB	±11/2 LSB	31.5µs	Plastic DIP (P28)
ML2233CCP	±1 LSB	±21/2 LSB	31.5µs	Plastic DIP (P28)
ML2233DCP	±1 LSB	±21/2 LSB	44.0µs	Plastic DIP (P28)

ML2252, ML2259

µP Compatible 8-Bit A/D Converters with 2- or 8-Channel Multiplexer

GENERAL DESCRIPTION

The ML2252 and ML2259 combine an 8-bit A/D converter, 2- or 8-channel analog multiplexer, and a microprocessor compatible 8-bit parallel interface and control logic in a single monolithic CMOS device.

Easy interface to microprocessors is provided by the latched and decoded multiplexer address inputs and a double buffered three-state data bus. These analog-to-digital converters allow the microprocessor to operate completely asynchronous to the converter clock.

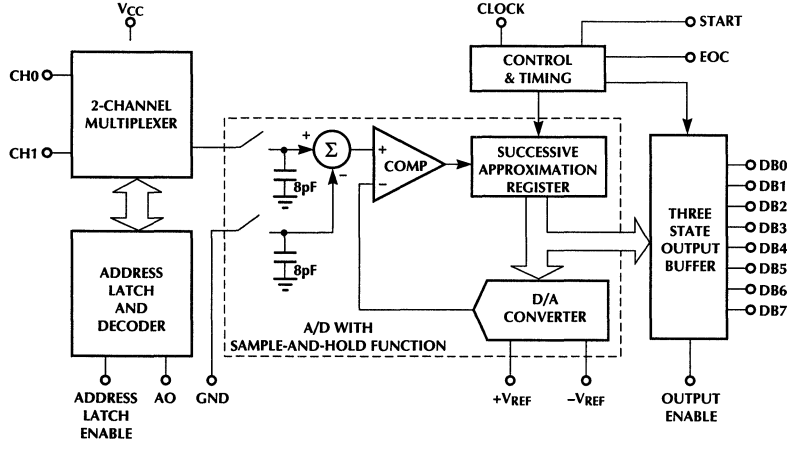
The built in sample and hold function provides the ability to digitize a 5V, 50KHz sine wave to 8-bit accuracy. The differential comparator design provides low power supply sensitiveity to DC and AC variations. The voltage reference can be externally set to any value between ground and V_{CC}, thus allowing a full conversion over a relatively small span if desired. All parameters are guaranteed over temperature with a power supply voltage of 5V ±10%.

The device is suitable for a wide range of applications from process and machine control to consumer, automotive, and telecommunication applications.

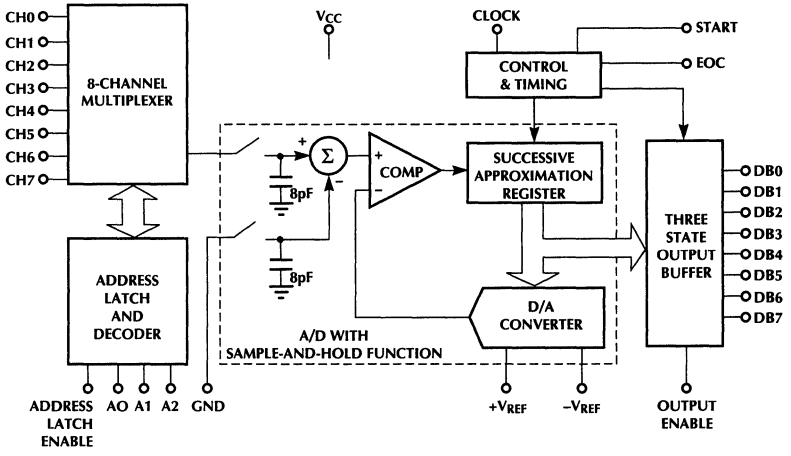
FEATURES

- Conversion time (f_{CLK} = 1.46MHz) 6.6µs
- Total unadjusted error ±1/2LSB or ±1LSB
- No missing codes
- Sample and hold 390ns acquisition
- Capable of digitizing a 5V, 50KHz sine wave
- 2- or 8-channel input multiplexer
- 0V to 5V analog input range with single 5V power supply
- Operates ratiometrically or with up to 5V voltage reference
- No zero or full scale adjust required
- Analog input protection 25mA per input min
- Continuous conversion mode
- Low power dissipation 15mW MAX
- TTL and CMOS compatible digital inputs and outputs
- Standard 20-pin or 28-pin DIP or PCC
- Temperature range 0°C to +70°C, or –40°C to +85°C, or –55°C to +125°C

ML2252 BLOCK DIAGRAM



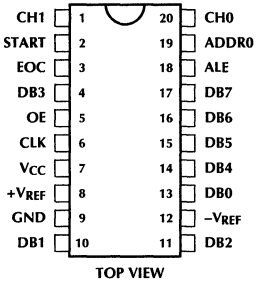
ML2259 BLOCK DIAGRAM



PIN CONFIGURATION

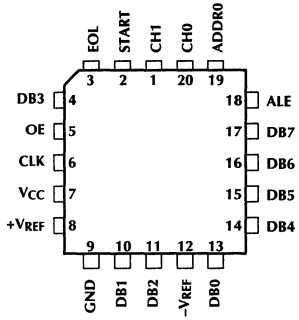
2

ML2252
20-Pin DIP (P20)



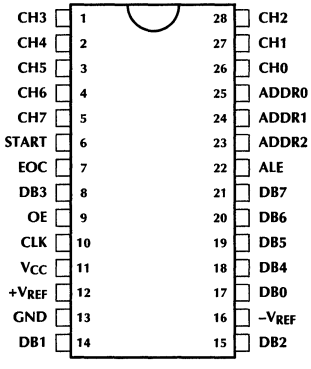
TOP VIEW

ML2252
20-Pin PCC (Q20)



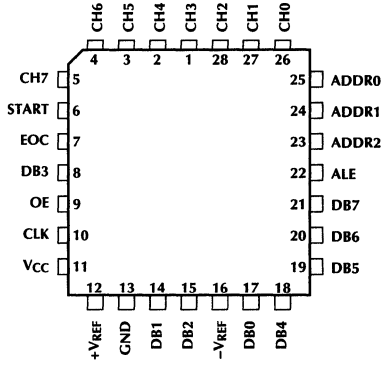
TOP VIEW

ML2259
28-Pin DIP(P28)



TOP VIEW

ML2259
28-Pin PCC (Q28)



TOP VIEW

PIN DESCRIPTION

Pin Number ML2252	Pin Number ML2259	Name	Function
	1	CH3	Analog input 3.
	2	CH4	Analog input 4.
	3	CH5	Analog input 5.
	4	CH6	Analog input 6.
	5	CH7	Analog input 7.
2	6	START	Start of conversion. Active high digital input pulse initiates conversion.
3	7	EOC	End of conversion. This output goes low after a START pulse occurs, stays low for the entire A/D conversion, and goes high after conversion is completed. Data on DB0–DB7 is valid on rising edge of EOC and stays valid until next EOC rising edge.
4	8	DB3	Data output 3.
5	9	OE	Output enable input. When OE = 0, DB0–DB7 are in high impedance state; OE = 1, DB0–DB7 are active outputs.
6	10	CLK	Clock. Clock input provides timing for A/D converter, S/H, and digital interface.
7	11	V_{CC}	Positive supply. 5V ±10%.
8	12	$+V_{REF}$	Positive reference voltage.
9	13	GND	Ground. 0V, all analog and digital inputs or outputs are referenced to this point.
10	14	DB1	Data output 1.
11	15	DB2	Data output 2.
12	16	$-V_{REF}$	Negative reference voltage.
13	17	DB0	Data output 0.
14	18	DB4	Data output 4.
15	19	DB5	Data output 5.
16	20	DB6	Data output 6.
17	21	DB7	Data output 7.
18	22	ALE	Address latch enable. Input to latch in the digital address (ADDR2-0) on the rising edge of the multiplexer.
	23	ADDR2	Address input 2 to multiplexer. Digital input for selecting analog input.
	24	ADDR1	Address input 1 to multiplexer. Digital input for selecting analog input.
19	25	ADDR0	Address input 0 to multiplexer. Digital input for selecting analog input.
20	26	CH0	Analog input 0.
1	27	CH1	Analog input 1.
	28	CH2	Analog input 2.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage, V_{CC} 6.5V
Voltage
  Logic Inputs ..... –0.3V to V_{CC} +0.3V
  Analog Inputs ..... –0.3V to V_{CC} +0.3V
Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Package Dissipation
  at T_A = 25°C (Board Mount) 875mW
Lead Temperature (Soldering 10 sec.)
  Dual-In-Line Package (Plastic) ..... 260°C
  Dual-In-Line Package (Ceramic) ..... 300°C
Molded Chip Carrier Package
  Vapor Phase (60 sec.) ..... 215°C
  Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... $4.5V_{DC}$ to $6.3V_{DC}$
Temperature Range (Note 3) ..... $T_{MIN} \le T_A \le T_{MAX}$
  ML2252/59BMJ, ML2252/59CMJ ..... –55°C to +125°C
  ML2252/59BIJ, ML2252/59CIJ ..... –40°C TO +85°C
  ML2252/59BCP, ML2252/59BCQ, ML2252/59CCP, ML2252/59CCQ ..... 0°C TO +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 10\%$, $-V_{REF} = GND$ and $f_{CLK} = 1.46MHz$

PARAMETER	NOTES	CONDITIONS	ML2252B, ML2259B MIN	ML2252B, ML2259B TYP (NOTE 4)	ML2252B, ML2259B MAX	ML2252C, ML2259C MIN	ML2252C, ML2259C TYP (NOTE 4)	ML2252C, ML2259C MAX	UNITS
Converter and Multiplexer Characteristics									
Total Unadjusted Error	5, 7	$V_{REF} = V_{CC}$			±1/2			±1	LSB
$+V_{REF}$ Voltage Range	6		$-V_{REF}$		$V_{CC} + 0.1$	$-V_{REF}$		$V_{CC} + 0.1$	V
$-V_{REF}$ Voltage Range	6		GND – 0.1		$+V_{REF}$	GND – 0.1		$+V_{REF}$	V
Reference Input Resistance	5		14	20	35	14	20	28	KΩ
Analog Input Range	5, 8		GND – 0.1		$V_{CC} + 0.1$	GND – 0.1		$V_{CC} + 0.1$	V
Power Supply Sensitivity	6	DC, $V_{CC} = 5V \pm 10\%$		±1/32	±1/4		±1/32	±1/4	LSB
		100mVp-p, 100KHz Sine on V_{CC}, $V_{IN} = 0$		±1/16			±1/16		LSB
I_{OFF}, Off Channel Leakage Current (Note 9)	5, 9	On Channel = V_{CC} Off Channel = 0V	–1			–1			µA
		On Channel = 0V Off Channel = V_{CC}			1			1	µA
I_{ON}, On Channel Leakage Current (Note 9)	5, 9	On Channel = 0V Off Channel = V_{CC}	–1			–1			µA
		On Channel = V_{CC} Off Channel = 0V			1			1	µA

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNITS
Digital and DC							
$V_{IN(1)}$	Logical "1" Input Voltage	5		2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	5				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	5	$V_{IN} = V_{CC}$			1	µA
$I_{IN(0)}$	Logical "0" Input Current	5	$V_{IN} = 0V$	–1			µA
$V_{OUT(1)}$	Logical "1" Output Voltage	5	$I_{OUT} = -2mA$	4.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	5	$I_{OUT} = 2mA$			0.4	V
I_{OUT}	Three-State Output Current	5	$V_{OUT} = 0V$	–1			µA
			$V_{OUT} = V_{CC}$			1	µA
I_{CC}	Supply Current	5			1.5	3	mA
AC and Dynamic Performance Characteristics (Note 10)							
t_{ACQ}	Sample and Hold Acquisition				1/2		$1/f_{CLK}$
f_{CLK}	Clock Frequency	5		10		1460	KHz
t_C	Conversion Time				8.5	8.5 + 250ns	$1/f_{CLK}$
SNR	Signal to Noise Ratio		$V_{IN} = 51KHz$, 5V Sine. $f_{CLK} = 1.46MHz$ ($f_{SAMPLING} \cong 150KHz$). Noise is Sum of All Nonfundamental Components up to 1/2 of $f_{SAMPLING}$		47		dB

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNITS
AC and Dynamic Performance Characteristics (Note 10) (Continued)							
THD	Total Harmonic Distortion		V_{IN} = 51KHz, 5V Sine. f_{CLK} = 1.46MHz ($f_{SAMPLING} \cong$ 150KHz). THD is Sum 2, 3, 4, 5 Harmonics Relative to Fundamental		–60		dB
IMD	Intermodulation Distortion		$V_{IN} = f_A + f_B$. f_A = 49KHz, 2.5V Sine. f_B = 47.8KHz, 2.5V Sine, f_{CLK} = 1.46MHz ($f_{SAMPLING} \cong$ 150KHz). IMD is $(f_A + f_B)$, $(f_A - f_B)$, $(2f_A + f_B)$, $(2f_A - f_B)$, $(f_A + 2f_B)$, $(f_A - 2f_B)$ Relative to Fundamental		–60		dB
FR	Frequency Response		V_{IN} = 0 to 50KHz. 5V Sine Relative to 1KHz		0.1		dB
t_{DC}	Clock Duty Cycle	6, 11		40		60	%
t_{EOC}	End of Conversion Delay	5			1/2	1/2 + 250ns	$1/f_{CLK}$
t_{WS}	Start Pulse Width	5		50			ns
t_{SS}	Start Pulse Setup Time	6, 12	Synchronous Only	40			ns
t_{WALE}	Address Latch Enable Pulse Width	5		50			ns
t_S	Address Setup	5		0			ns
t_H	Address Hold	5		50			ns
$t_{H1, H0}$	Output Enable for DB0–DB7	6	Figure 1, C_L = 50pF			100	ns
		6	Figure 1, C_L = 10pF			50	ns
$t_{1H, 0H}$	Output Disable for DB0–DB7	6	Figure 1, C_L = 50pF			100	ns
		6	Figure 1, C_L = 10pF			50	ns
C_{IN}	Capacitance of Logic Input				5		pF
C_{OUT}	Capacitance of Logic Outputs				10		pF

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < GND –0 1V or V_{CC} + 0.1) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: –55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation

Note 7: Total unadjusted error includes offset, full scale, linearity, multiplexer and sample and hold errors

Note 8: For $-V_{REF} \geq V_{IN}$ (+) the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4 5V), as high level analog inputs (5V) can cause this input diode to conduct — especially at elevated temperatures, and cause errors for analog inputs near full scale. The spec allow 100mV forward bias of either diode This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of $4.900V_{DC}$ over temperature variations, initial tolerance and loading

Note 9: Leakage current is measured with the clock not switching.

Note 10: C_L = 50pF, timing measured at 50% point.

Note 11: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum time the clock is high or the minimum time the clock is low must be at least 40ns. The maximum time the clock can be high or low is 60µs.

Note 12: The conversion start setup time requirement only needs to be satisfied if a conversion must be synchronized to a given clock rising edge. If the setup time is not met, start conversion will have an uncertainty of one clock pulse.

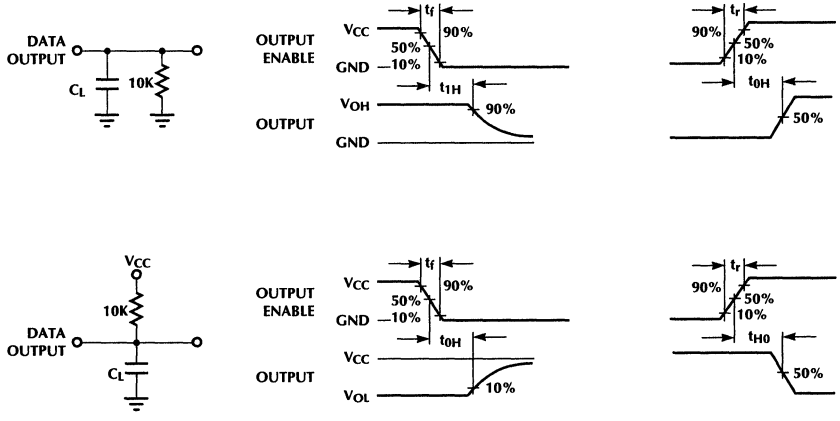


Figure 1. High Impedance Test Circuits and Waveforms

2

TYPICAL PERFORMANCE CURVES

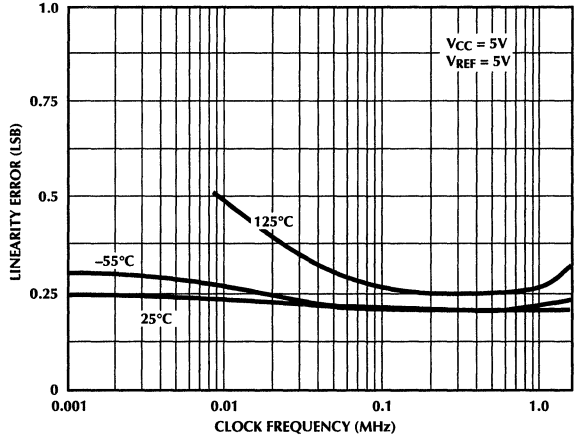


Figure 2. Linearity Error vs f_{CLK}

TYPICAL PERFORMANCE CURVES (Continued)

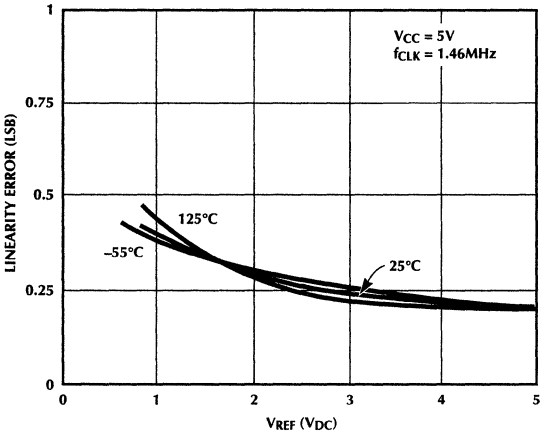


Figure 3. Linearity Error vs V_{REF} Voltage

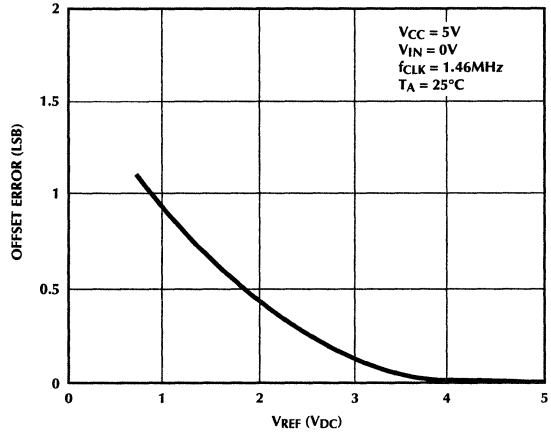


Figure 4. Unadjusted Offset Error vs V_{REF} Voltage

1.0 FUNCTIONAL DESCRIPTION

1.1 MULTIPLEXER ADDRESSING

The ML2252 and ML2259 contain a single ended analog multiplexer. A particular input channel is selected by using the address decoder. The relationship between the address inputs, ADDR0–ADDR2, and the analog input selected is shown in Table 1. The address inputs are latched into the decoder on the rising edge of the address latch signal ALE.

ML2252

SELECTED ANALOG CHANNEL	ADDRESS INPUT
CH0	0
CH1	1

ML2259

SELECTED ANALOG CHANNEL	ADDRESS INPUT ADDR2	ADDR1	ADDR0
CH0	0	0	0
CH1	0	0	1
CH2	0	1	0
CH3	0	1	1
CH4	1	0	0
CH5	1	0	1
CH6	1	1	0
CH7	1	1	1

Table 1. Multiplexer Address Decoding

1.2 A/D CONVERTER

The A/D converter uses successive approximation to perform the conversion. The converter is composed of the successive approximation register, the DAC and the comparator.

The DAC generates the precise levels that determine the linearity and accuracy of the conversion. The DAC is composed of a capacitor upper array and a resistor lower array. The capacitor upper array generates the 4 MSB decision levels while the series resistor lower array generates the 4 LSB decision levels. A switch decoder tree is used to decode the proper level from both arrays.

The capacitor/resistor array offers fast conversion, superior linearity and accuracy since matching is only required between $2^4 = 16$ elements (as opposed to $2^8 = 256$ elements in conventional designs). And since the levels are based on the ratio of capacitors to capacitors and resistors to resistors, the accuracy and long term stability of the converter is improved. This also guarantees monotonicity and no missing codes, as well as eliminating any linearity temperature or power supply dependence.

The successive approximation register is a digital block used to store the bit decisions from the conversion.

The comparator design is unique in that it is fully differential and auto zeroed. The fully differential architecture provides excellent noise immunity, excellent power supply rejection, and wide common mode range. The comparator is auto zeroed at the start of each conversion in order to remove any DC offset and full scale gain error, thus improving accuracy and linearity.

Another advantage of the capacitor array approach used in the ML2252 and ML2259 is the inherent sample-and-hold function. This true S/H allows an accurate conversion to be done on the input even if the analog signal is not stable. Linearity and accuracy are maintained for analog signals up to 1/2 the sampling frequency. As a result, input signals up to 50KHz can be converted without degradation in linearity or accuracy.

The sequence of events during a conversion is shown in figure 5. The rising edge of a START pulse resets the internal registers and initiates a conversion on the next rising edge of CLK providing that (t_{SS}) start pulse setup time is satisfied. If this setup time is not met, start conversion will have an uncertainty of one clock pulse. The input is then sampled for the next half CLK period until EOC goes low. EOC goes low on the falling edge of the next CLK pulse indicating that the conversion is now beginning. The actual conversion now takes place for the next eight CLK pulses, one bit for each CLK pulse. After the conversion is done, the data is updated on DB0–DB7 and EOC goes high on the rising edge of the 9th CLK pulse, indicating that the conversion has been completed and data is valid on DB0–DB7. The data will stay valid on DB0–DB7 until the next conversion updates the data word on the next rising edge of EOC.

A conversion can be interrupted and restarted at any time by a new START pulse.

1.3 ANALOG INPUTS AND SAMPLE/HOLD

The ML2252 and ML2259 have a true sample-and-hold circuit which samples both the selected input and ground simultaneously. These analog to digital converters can reject AC common mode signals from DC–50KHz as well as maintain linearity for signals from DC–50KHz.

The plot in figure 6 shows a 2048 point FFT of the ML2259 converting a 50KHz, 0 to 5V, low distortion sine wave input. The ML2252 and ML2259 sample and digitize, at their specified accuracy, dynamic input signals with frequency components up to the Nyquist frequency (one-half the sampling rate). The output spectra yields precise measurements of input signal level, harmonic components, and signal to noise ratio up to the 8-bit level. The near ideal signal to noise ratio is maintained independent of increasing analog input frequencies to 50KHz.

The signal at the analog input is sampled during the interval when the sampling switch is open prior to conversion start. The sampling window (S/H acquisition time) is one half CLK period long and occurs one half CLK period after START goes low. When the sampling switch closes at the start of the S/H acquisition time, 8pF of capacitance is thrown onto the analog input. One half CLK period later, the sampling switch opens, the signal present at analog input is stored and conversion starts. Since any error on the analog input at the end of the S/H acquisition time will cause additional conversion error, care should be taken to insure adequate settling and charging time from the source. If more charging or settling time is needed to reduce these analog input errors, a longer CLK period can be used.

Each analog input has dual diodes to the supply rails, and a minimum of ±25mA (±100mA typically) can be injected into each analog input without causing latchup.

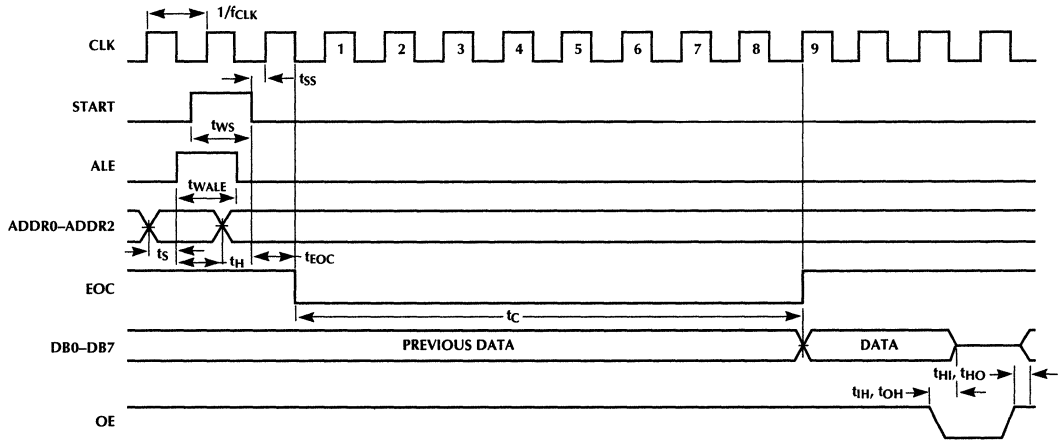


Figure 5. Timing Diagram

1.4 REFERENCE

The voltage applied to the $+V_{REF}$ and $-V_{REF}$ inputs defines the voltage span of the analog input (the difference between V_{INMAX} and V_{INMIN}) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pins must be connected to a voltage source capable of driving the reference input resistance, typically 20K.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the $+V_{REF}$ pin can be tied to V_{CC} and $-V_{REF}$ tied to GND. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between specific voltage limits, the reference pins can be biased with a time and temperature stable voltage source.

$+V_{REF}$ and $-V_{REF}$ can be at any voltage between V_{CC} and GND. In addition, the difference between $+V_{REF}$ and $-V_{REF}$ can be set to small values for conversions over smaller voltage ranges. Particular care must be taken with regard to noise pickup, circuit layout ond system error voltage sources when operating with a reduced span due to the increased sensitivity converter.

1.5 POWER SUPPLY AND REFERENCE DECOUPLING

A 10µF electrolytic capacitor is recommended to bypass V_{CC} to GND, using as short a lead length as possible. In addition, with clock frequencies above 1MHz, a 0.1µF ceramic disc capacitor should be used to bypass V_{CC} to GND.

If REF+ and REF– inputs are driven by long lines, they should be bypassed by 0.1µF ceramic disc capacitors at the reference input pins (pins 12, 16).

1.6 DYNAMIC PERFORMANCE

Signal-to-Noise Ratio

Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)dB$$

where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92dB.

Harmonic Distortion

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2252 and ML2259 are defined as

$$20\log = \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

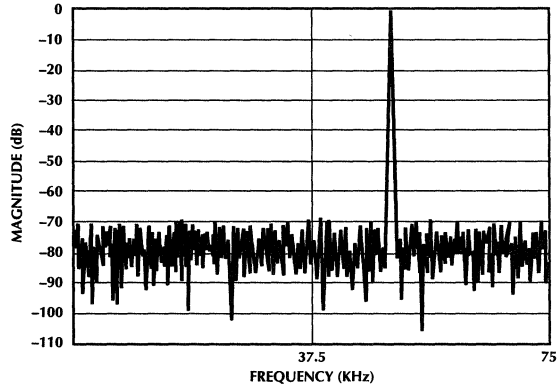


Figure 6. Output Spectrum

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of $mf_A + nf_B$, where m, n = 0, 1, 2, 3,... . Intermodulation terms are those for which m or n is not equal to zero. The (IMD) intermodulation distortion specification includes the second order terms ($f_A + f_B$) and ($f_A - f_B$) and the third order terms ($2f_A + f_B$), ($2f_A - f_B$), ($f_A + 2f_B$) and ($f_A - 2f_B$) only.

1.7 DIGITAL INTERFACE

The analog inputs are selected by the digital addresses, ADDR0–ADDR2, and latched on the rising edge of ALE. This is described in the Multiplexer Addressing section.

A conversion is initiated by the rising edge of a START pulse. As long as this pulse is high, the internal logic is reset.

The sampling interval starts with the following CLK rising edge after a START falling edge and ends on the falling edge of CLK. The conversion starts and EOC goes low. The sampling clock is at least one half CLK period wide. Each bit conversion in the successive approximation process takes 1 CLK period. On the rising edge of the ninth CLK pulse, the digital output of the conversion is updated on the outputs DB0–DB7 and EOC goes high indicating the conversion is done and data on DB0–DB7 is valid.

One feature of the ML2252 and ML2259 is that the data is double buffered. This means that the outputs DB0–DB7 will stay valid until updated at the end of the next conversion and will not become invalid when the next conversion starts. This facilitates interfacing with external logic of µP.

The signal OE drives the data bus, DB0–DB7, into the high impedance state when held low. This allows the ML2252 and ML2259 to be tied directly to a µP system bus without any latches or buffers.

1.7.1 Restart During Conversion

If the A/D is restarted (start goes low and returns high) during a convesion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed. EOC will remain low and the output data latch is not updated.

1.7.2 Continuous Conversions

In the free-running, continuous conversion mode, the start input is tied to the (figure 7) EOC output. An initialization pulse, following power-up, of mementarily forcing a logic high level is required to guarantee operation.

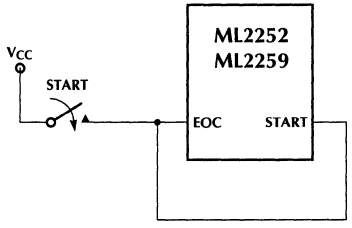


Figure 7. Continuous Conversion Mode

2.0 TYPICAL APPLICATIONS

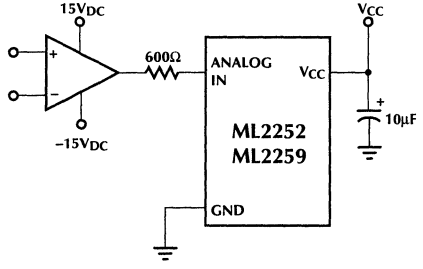


Figure 8. Protecting the Input

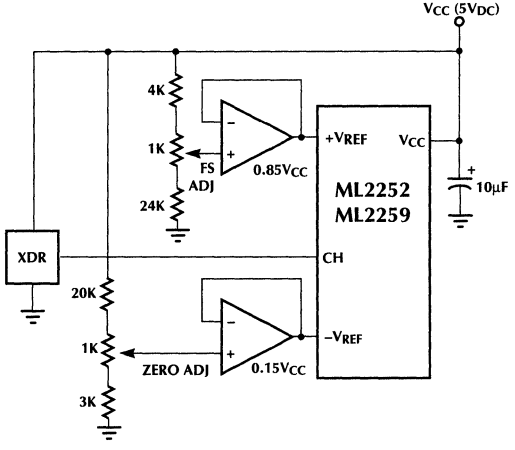


Figure 9. Operating with Ratiometric Transducers 15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

ORDERING INFORMATION

PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
Two Analog Inputs, 20-Pin Package			
ML2252BMJ	±1/2 LSB	–55°C to +125°C	Hermetic DIP (J20)
ML2252BIJ		–40°C to +85°C	Hermetic DIP (J20)
ML2252BCP		0°C to +70°C	Molded DIP (P20)
ML2252BCQ		0°C to +70°C	Molded PCC (Q20)
ML2252CIJ	±1 LSB	–40°C to +85°C	Hermetic DIP (J20)
ML2252CCP		0°C to +70°C	Molded DIP (P20)
ML2252CCQ		0°C to +70°C	Molded PCC (Q20)
Eight Analog Inputs, 28-Pin Package			
ML2259BMJ	±1/2 LSB	–55°C to +125°C	Hermetic DIP (J28)
ML2259BIJ		–40°C to +85°C	Hermetic DIP (J28)
ML2259BIP		–40°C to +85°C	Molded DIP (P28)
ML2259BCP		0°C to +70°C	Molded DIP (P28)
ML2259BCQ		0°C to +70°C	Molded PCC (Q28)
ML2259CIP		–40°C to +85°C	Molded DIP (P28)
ML2259CIJ	±1 LSB	–40°C to +85°C	Hermetic DIP (J28)
ML2259CCP		0°C to +70°C	Molded DIP (P28)
ML2259CCQ		0°C to +70°C	Molded PCC (Q28)

ML2258

µP Compatible 8-Bit A/D Converter with 8-Channel Multiplexer

GENERAL DESCRIPTION

The ML2258 combines an 8-bit A/D converter, 8-channel analog multiplexer, and a microprocessor compatible 8-bit parallel interface and control logic in a single monolithic CMOS device.

Easy interface to microprocessors is provided by the latched and decoded multiplexer address inputs and latched three-state outputs.

The device is suitable for a wide range of applications from process and machine control to consumer, automotive, and telecommunication applications.

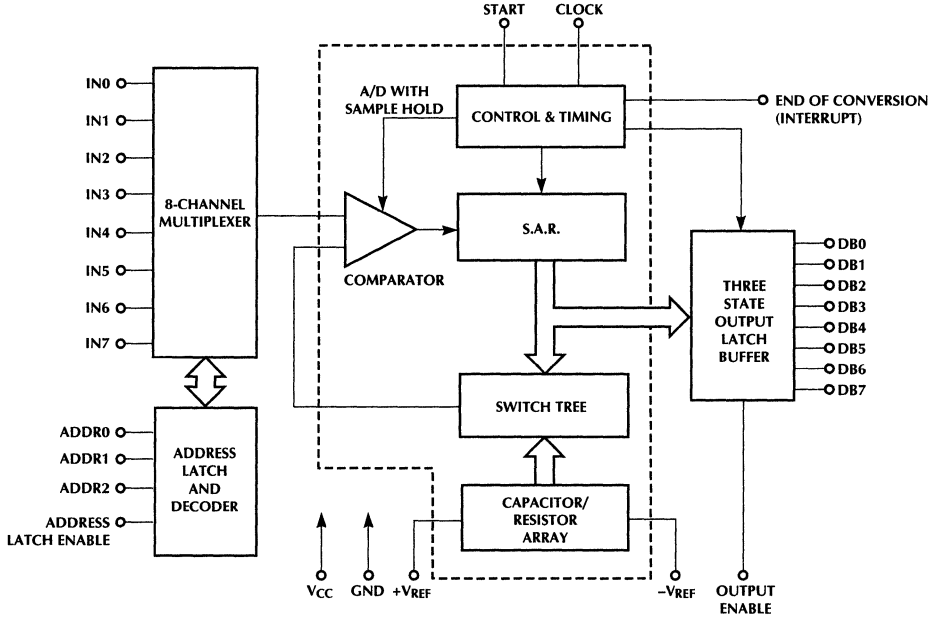
The ML2258 is an enhanced pin compatible second source for the industry standard ADC0808/ADC0809. The ML2258 enhancements are faster conversion time, true sample and hold function, superior power supply rejection, wider reference range, and a double buffered data bus as well as faster digital timing. All parameters are guaranteed over temperature with a power supply voltage of 5V ±10%.

FEATURES

- Conversion time 6.6µs
- Total unadjusted error ±1/2LSB or ±1LSB
- No missing codes
- Sample and hold 390ns acquisition
- Capable of digitizing a 5V, 50KHz sine wave
- 8-input multiplexer
- 0V to 5V analog input range with single 5V power supply
- Operates ratiometrically or with up to 5V voltage reference
- No zero or full scale adjust required
- Analog input protection 25mA per input min
- Low power dissipation 3mA max
- TTL and CMOS compatible digital inputs and outputs
- Standard 28-pin DIP or surface mount PCC
- Superior pin compatible replacement for ADC0808 and ADC0809

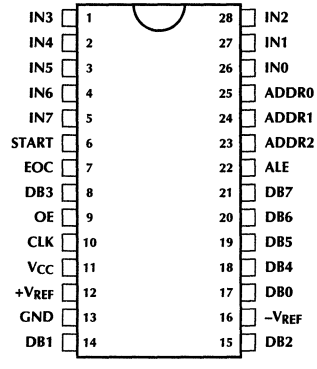
2

BLOCK DIAGRAM



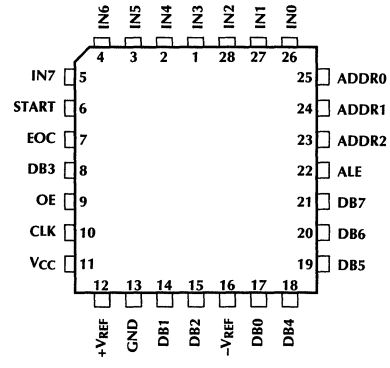
PIN CONFIGURATION

ML2258
28-Pin DIP (P28)



TOP VIEW

ML2258
28-Pin PCC (Q28)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	IN3	Analog input 3.
2	IN4	Analog input 4.
3	IN5	Analog input 5.
4	IN6	Analog input 6.
5	IN7	Analog input 7.
6	START	Start of conversion. Active high digital input pulse initiates conversion.
7	EOC	End of conversion. This output goes low after a START pulse occurs, stays low for the entire A/D conversion, and goes high after conversion is completed. Data on DB0–DB7 is valid on rising edge of EOC and stays valid until next EOC rising edge.
8	DB3	Data output 3.
9	OE	Output enable input. When OE = 0, DB0–DB7 are in high impedance state; OE = 1, DB0–DB7 are active outputs.
10	CLK	Clock. Clock input provides timing for A/D converter, S/H, and digital interface.
11	V_{CC}	Positive supply. 5V ± 10%.
12	$+V_{REF}$	Positive reference voltage.
13	GND	Ground. 0V, all analog and digital inputs or outputs are reference to this point.
14	DB1	Data output 1.
15	DB2	Data output 2.
16	$-V_{REF}$	Negative reference voltage.
17	DB0	Data output 0.
18	DB4	Data output 4.
19	DB5	Data output 5.
20	DB6	Data output 6.
21	DB7	Data output 7.
22	ALE	Address latch enable. Input to latch in the digital address (ADDR2–0) on the rising edge of the multiplexer.
23	ADDR0	Address input 0 to multiplexer. Digital input for selecting analog input.
24	ADDR1	Address input 1 to multiplexer. Digital input for selecting analog input.
25	ADDR2	Address input 2 to multiplexer. Digital input for selecting analog input.
26	IN0	Analog input 0.
27	IN1	Analog input 1.
28	IN2	Analog input 2.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage, V_{CC} 6.5V
Voltage
  Logic Inputs ..... –0.3V to V_{CC} +0.3V
  Analog Inputs ..... –0.3V to V_{CC} +0.3V
Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Package Dissipation
  at T_A = 25°C (Board Mount) 875mW
Lead Temperature (Soldering 10 sec.)
  Dual-In-Line Package (Plastic) ..... 260°C
  Dual-In-Line Package (Ceramic) ..... 300°C
  Molded Chip Carrier Package
    Vapor Phase (60 sec.) ..... 215°C
    Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... 4.5V_{DC} to 6.3V_{DC}
Temperature Range (Note 3) ..... $T_{MIN} \le T_A \le T_{MAX}$
  ML2258BMJ, ML2258CMJ ..... –55°C to +125°C
  ML2258BIJ, ML2258BIP, ML2258BIQ, ML2258CIJ
  ML2258CIP, ML2258CIQ ..... –40°C to +85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 10\%$, $-V_{REF}$ = GND and f_{CLK} = 10.24MHz

			ML2258B			ML2258C			
PARAMETER	NOTES	CONDITIONS	MIN	TYP (NOTE 4)	MAX	MIN	TYP (NOTE 4)	MAX	UNITS
Converter and Multiplexer									
Total Unadjusted Error	5, 7	$V_{REF} = V_{CC}$			±1/2			±1	LSB
$+V_{REF}$ Voltage Range	6		$-V_{REF}$		V_{CC} + 0.1	$-V_{REF}$		V_{CC} + 0.1	V
$-V_{REF}$ Voltage Range	6		GND – 0.1		$+V_{REF}$	GND – 0.1		$+V_{REF}$	V
Reference Input Resistance	5		14	20	35	14	20	28	KΩ
Analog Input Range	5, 8		GND – 0.1		V_{CC} + 0.1	GND – 0.1		V_{CC} + 0.1	V
Power Supply Sensitivity	6	DC, V_{CC} = 5V ± 10%		±1/32	±1/4		±1/32	±1/4	LSB
		100mVp-p, 100KHz Sine on V_{CC}, V_{IN} = 0		±1/16			±1/16		LSB
I_{OFF}, Off Channel Leakage Current (Note 9)	5, 9	On Channel = V_{CC} Off Channel = 0V	–1			–1			µA
		On Channel = 0V Off Channel = V_{CC}			1			1	µA
I_{ON}, On Channel Leakage Current (Note 9)	5, 9	On Channel = 0V Off Channel = V_{CC}	–1			–1			µA
		On Channel = V_{CC} Off Channel = 0V			1			1	µA
Digital and DC									
$V_{IN(1)}$, Logical "1" Input Voltage	5		2.0			2.0			V
$V_{IN(0)}$, Logical "0" Input Voltage	5				0.8			0.8	V
$I_{IN(1)}$, Logical "1" Input Current	5	$V_{IN} = V_{CC}$			1			1	µA
$I_{IN(0)}$, Logical "0" Input Current	5	V_{IN} = 0V	–1			–1			µA
$V_{OUT(1)}$, Logical "1" Output Voltage	5	I_{OUT} = –2mA	4.0			4.0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	5	I_{OUT} = 2mA			0.4			0.4	V
I_{OUT}, Three-State Output Current	5	V_{OUT} = 0V	–1			–1			µA
		$V_{OUT} = V_{CC}$			1			1	µA
I_{CC}, Supply Current	5			1.5	3		1.5	3	mA

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNITS
AC and Dynamic Performance Characteristics (Note 10)							
t_{ACQ}	Sample and Hold Acquisition				4		$1/f_{CLK}$
f_{CLK}	Clock Frequency	5		100		10240	KHz
t_C	Conversion Time	5			67	67 + 250ns	$1/f_{CLK}$
SNR	Signal to Noise Ratio		V_{IN} = 51KHz, 5V Sine. f_{CLK} = 10.24MHz ($f_{SAMPLING} \cong$ 150KHz). Noise is Sum of All Nonfundamental Components up to 1/2 of $f_{SAMPLING}$		47		dB
THD	Total Harmonic Distortion		V_{IN} = 51KHz, 5V Sine. f_{CLK} = 10.24MHz ($f_{SAMPLING} \cong$ 150KHz). THD is Sum of 2, 3, 4, 5 Harmonics Relative to Fundamental		–60		dB
IMD	Intermodulation Distortion		$V_{IN} = f_A + f_B$. f_A = 49KHz, 2.5V Sine. f_B = 47.8KHz, 2.5V Sine, f_{CLK} = 10.24MHz ($f_{SAMPLING} \cong$ 150KHz). IMD is $(f_A + f_B)$, $(f_A - f_B)$, $(2f_A + f_B)$, $(2f_A - f_B)$, $(f_A + 2f_B)$, $(f_A - 2f_B)$ Relative to Fundamental		–60		dB
FR	Frequency Response		V_{IN} = 0 to 50KHz. 5V Sine Relative to 1KHz		0.1		dB
t_{DC}	Clock Duty Cycle	6, 11		40		60	%
t_{EOC}	End of Conversion Delay	5			8	8 + 250ns	$1/f_{CLK}$
t_{WS}	Start Pulse Width	5		50			ns
t_{SS}	Start Pulse Setup Time	6, 12	Synchronous Only	40			ns
t_{WALE}	Address Latch Enable Pulse Width	5		50			ns
t_S	Address Setup	5		0			ns
t_H	Address Hold	5		50			ns
$t_{H1, H0}$	Output Enable for DB0–DB7	6	Figure 1, C_L = 50pF			100	ns
		6	Figure 1, C_L = 10pF			50	ns
$t_{1H, 0H}$	Output Disable for DB0–DB7	6	Figure 1, C_L = 50pF			200	ns
		6	Figure 1, C_L = 10pF			100	ns
C_{IN}	Capacitance of Logic Input				5		pF
C_{OUT}	Capacitance of Logic Outputs				10		pF

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired All voltages unless otherwise specified are measured with respect to ground

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < V– or V_{IN} > V+) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: –55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Total unadjusted error includes offset, full scale, linearity, multiplexer and sample and hold errors.

Note 8: For $-V_{REF} \geq V_{IN}$ (+) the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct — especially at elevated temperatures, and cause errors for analog inputs near full scale. The spec allow 100mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 100mV, the output code will be correct To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of 4 $900V_{DC}$ over temperature variations, initial tolerance and loading

Note 9: Leakage current is measured with the clock not switching.

Note 10: C_L = 50pF, timing measured at 50% point.

Note 11: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum time the clock is high or the minimum time the clock is low must be at least 40ns. The maximum time the clock can be high or low is 60µs.

Note 12: The conversion start setup time requirement only needs to be satisfied if a conversion must be synchronized to a given clock rising edge. If the setup time is not met, start conversion will have an uncertainty of one clock pulse.

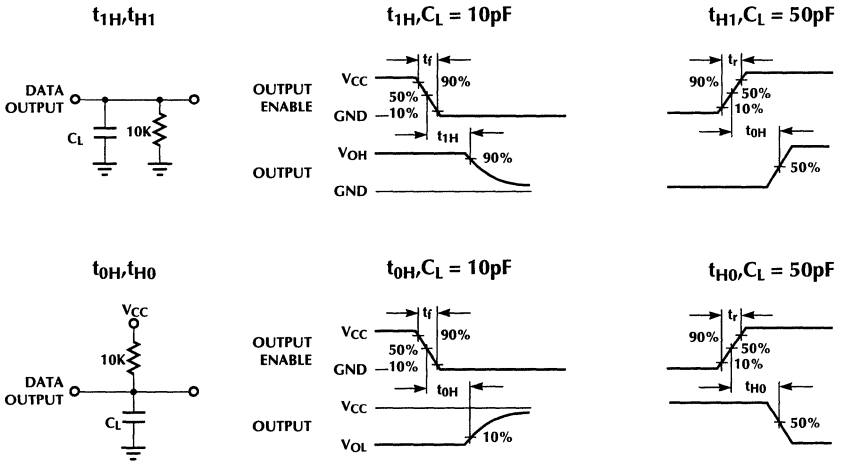


Figure 1. High Impedance Test Circuits and Waveforms

2

TYPICAL PERFORMANCE CURVES

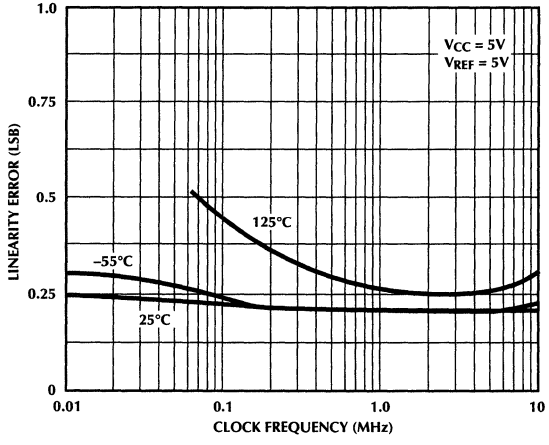


Figure 2. Linearity Error vs f_{CLK}

TYPICAL PERFORMANCE CURVES (Continued)

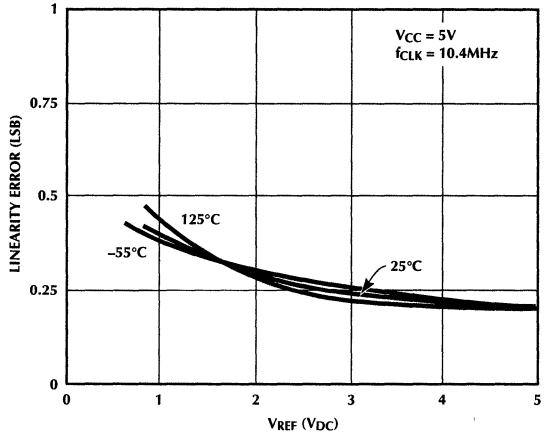


Figure 3. Linearity Error vs V_{REF} Voltage

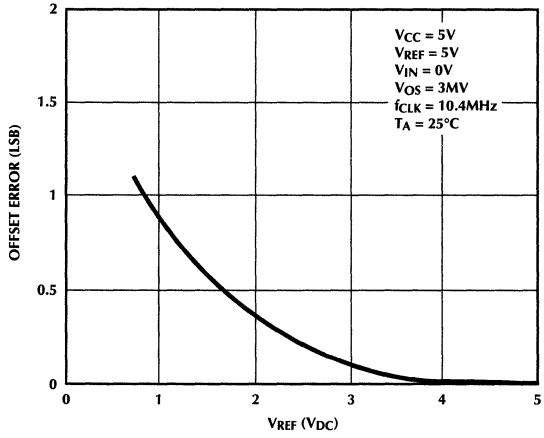


Figure 4. Unadjusted Offset Error vs V_{REF} Voltage

1.0 FUNCTIONAL DESCRIPTION

1.1 MULTIPLEXER ADDRESSING

The ML2258 contains an 8-channel single ended analog multiplexer. A particular input channel is selected by using the address decoder. The relationship between the address inputs, ADDR0–ADDR2, and the analog input selected is shown in Table 1. The address inputs are latched into the decoder on the rising edge of the address latch signal ALE.

SELECTED ANALOG CHANNEL	ADDRESS INPUT ADDR2	ADDR1	ADDR0
IN0	0	0	0
IN1	0	0	1
IN2	0	1	0
IN3	0	1	1
IN4	1	0	0
IN5	1	0	1
IN6	1	1	0
IN7	1	1	1

Table 1. Multiplexer Address Decoding

1.2 A/D CONVERTER

The A/D converter uses successive approximation to perform the conversion. The converter is composed of the successive approximation register, the DAC and the comparator.

The DAC generates the precise levels that determine the linearity and accuracy of the conversion. The DAC is composed of a capacitor upper array and a resistor lower array. The capacitor upper array generates the 4 MSB decision levels while the series resistor lower array generates the 4 LSB decision levels. A switch decoder tree is used to decode the proper level from both arrays.

The capacitor/resistor array offers fast conversion, superior linearity and accuracy since matching is only required between $2^4 = 16$ elements (as opposed to $2^8 = 256$ elements in conventional designs). And since the levels are based on the ratio of capacitors to capacitors and resistors to resistors, the accuracy and long term stability of the converter is improved. This also guarantees monotonicity and no missing codes, as well as eliminating any linearity temperature or power supply dependence.

The successive approximation register is a digital block used to store the bit decisions from the conversion.

The comparator design is unique in that it is fully differential and auto zeroed. The fully differential architecture provides excellent noise immunity, excellent power supply rejection, and wide common mode range. The comparator is auto zeroed at the start of each conversion in order to remove any DC offset and full scale gain error, thus improving accuracy and linearity.

Another advantage of the capacitor array approach used in the ML2258 over conventional designs is the inherent sample and hold function. This true S/H allows an accurate conversion to be done on the input even if the analog signal is not stable. Linearity and accuracy are maintained for analog signals up to 1/2 the sampling frequency. As a result, input signals up to 75KHz can be converted without degradation in linearity or accuracy.

The sequence of events during a conversion is shown in figure 5. The rising edge of a START pulse resets the internal registers and the falling edge initiates a conversion on the next rising edge of CLK. Four CLK pulses later, sampling of the analog input begins. The input is then sampled for the next four CLK periods until EOC goes low. EOC goes low on the rising edge of the 8th CLK pulse indicating that the conversion is now beginning. The actual conversion now takes place for the next 56 CLK pulses, one bit for each 7 CLK pulses. After the conversion is done, the data is updated on DB0–DB7 and EOC goes high on the rising edge of the 67th CLK pulse, indicating that the conversion has been completed and data is valid on DB0–DB7. The data will stay

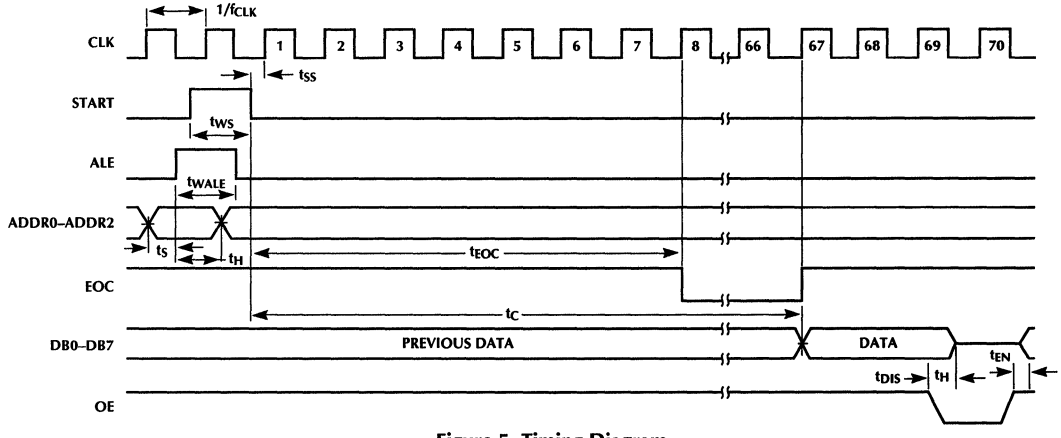


Figure 5. Timing Diagram

valid on DB0–DB7 until the next conversion updates the data word on the next rising edge of EOC.

A conversion can be interrupted and restarted at any time by a new START pulse.

1.3 ANALOG INPUTS AND SAMPLE/HOLD

The ML2258 has a true sample and hold circuit which samples both the selected input and ground simultaneously. This simultaneous sampling with a true S/H will give common mode rejection and AC linearity performance that is superior to devices where the two input terminals are not sampled at the same instant and where true sample and hold capability does not exist. Thus, the ML2258 can reject AC common mode signals from DC–50KHz as well as maintain linearity for signals from DC–50KHz.

The plot below (figure 6) shows a 2048 point FFT of the ML2258 converting a 50KHz, 0 to 5V, low distortion sine wave input. The ML2258 samples and digitizes, at its specified accuracy, dynamic input signals with frequency components up to the Nyquist frequency (one-half the sampling rate). The output spectra yields precise measurements of input signal level, harmonic components, and signal to noise ratio up to the 8-bit level. The near ideal signal to noise ratio is maintained independent of increasing analog input frequencies to 50KHz.

The signal at the analog input is sampled during the interval when the sampling switch is open prior to conversion start. The sampling window (S/H acquisition time) is 4 CLK periods long and occurs 4 CLK periods after START goes low. When the sampling switch closes at the start of the S/H acquisition time, 8pF of capacitance is thrown onto the analog input. 4 CLK periods later, the sampling switch opens, the signal present at analog input is stored and conversion starts. Since any error on the analog input at the end of the S/H acquisition time will cause additional conversion error, care should be taken to insure adequate settling and charging time from the source. If more charging or settling time is needed to reduce these analog input errors, a longer CLK period can be used.

The ML2258 has improved latchup immunity. Each analog input has dual diodes to the supply rails, and a minimum of ±25mA (±100mA typically) can be injected into each analog input without causing latchup.

1.4 REFERENCE

The voltage applied to the $+V_{REF}$ and $-V_{REF}$ inputs defines the voltage span of the analog input (the difference between V_{INMAX} and V_{INMIN}) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pins must be connected to a voltage source capable of driving the reference input resistance, typically 20K.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the $+V_{REF}$ pin can be tied to V_{CC} and $-V_{REF}$ tied to GND. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between specific voltage limits, the reference pins can be biased with a time and temperature stable voltage source.

In contrast to the ADC0808 and ADC0809, the ML2258 $-V_{REF}$ and $+V_{REF}$ reference values do not have to be symmetric around one half of the supply. $+V_{REF}$ and $-V_{REF}$ can be at any voltage between V_{CC} and GND. In addition, the difference between $+V_{REF}$ and $-V_{REF}$ can be set to small values for conversions over smaller voltage ranges. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter.

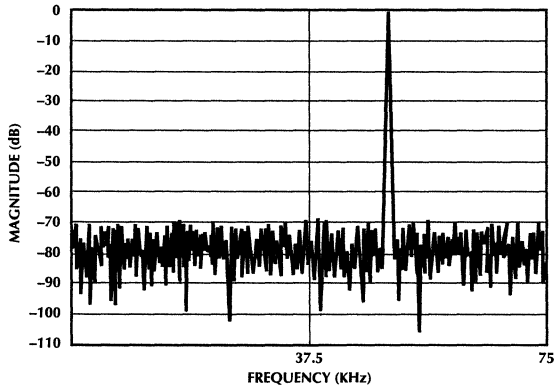


Figure 6. Output Spectrum

1.5 POWER SUPPLY AND REFERENCE DECOUPLING

A 10µF electrolytic capacitor is recommended to bypass V_{CC} to GND, using as short a lead length as possible. In addition, with clock frequencies above 1MHz, a 0.1µF ceramic disc capacitor should be used to bypass V_{CC} to GND.

If REF+ and REF– inputs are driven by long lines, they should be bypassed by 0.1µF Ceramic disc capacitors at the reference pins (pins 12, 16).

1.6 DYNAMIC PERFORMANCE

Signal-to-Noise Ratio

Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)dB$$

where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92dB.

Harmonic Distortion

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2258 is defined as

$$20\log = \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of $mf_A + nf_B$, where m, n = 0, 1, 2, 3,... . Intermodulation terms are those for which m or n is not equal to zero. The ML2258 (IMD) intermodulation distortion specification includes the second order terms $(f_A + f_B)$ and $(f_A - f_B)$ and the third order terms $(2f_A + f_B)$, $(2f_A - f_B)$, $(f_A + 2f_B)$ and $(f_A - 2f_B)$ only.

1.7 DIGITAL INTERFACE

The analog inputs are selected by the digital addresses, ADDR0–ADDR2, and latched on the rising edge of ALE. This is described in the Multiplexer Addressing section.

A conversion is initiated by the rising edge of a START pulse. As long as this pulse is high, the internal logic is reset.

The sampling interval starts with the 4th CLK rising edge after a START falling edge and ends on the 8th rising edge of CLK, 4 CLK periods later. On the rising edge of the 8th CLK pulse, the conversion starts and EOC goes low.

Each bit conversion in the successive approximation process takes 7 CLK periods. On the rising edge of the 64 CLK pulse, the digital output of the conversion is updated on the outputs DB0–DB7. On the rising edge of the 65th CLK pulse, EOC goes high indicating the conversion is done and data on DB0–DB7 is valid.

One feature of the ML2258 over conventional devices is that the data is double buffered. This means that the outputs DB0–DB7 will stay valid until updated at the end of the next conversion and will not become invalid when the next conversion starts. This facilitates interfacing with external logic of µP.

The signal OE drives the data bus, DB0–DB7, into the high impedance state when held low. This allows the ML2258 to be tied directly to a µP system bus without any latches or buffers.

2.0 TYPICAL APPLICATIONS

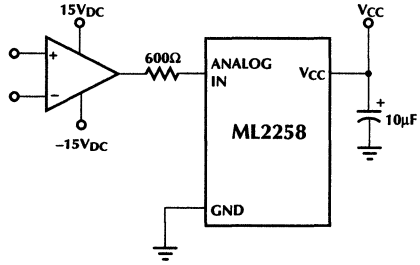


Figure 7. Protecting the Input

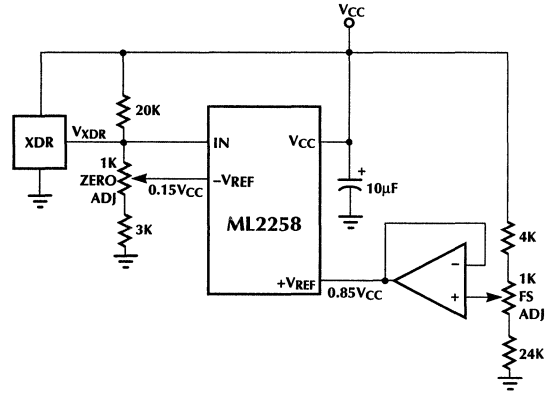


Figure 8. Operating with Ratiometric Transducers 15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

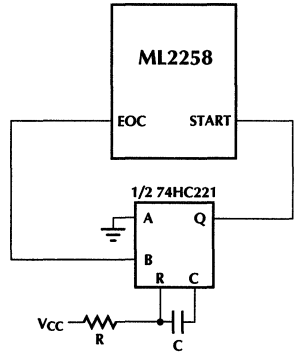


Figure 9. Continuous Conversion Mode

ORDERING INFORMATION

PART NUMBER	ALTERNATE PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
ML2258BMJ	ADC0808CJ	±1/2LSB	–55°C to +125°C	Hermetic DIP (J28)
ML2258BIJ	ADC0808CCJ		–40°C to +85°C	Hermetic DIP (J28)
ML2258BIP	ADC0808CCN		–40°C to +85°C	Molded DIP (P28)
ML2258BIQ	ADC0808CCV		–40°C to +85°C	Molded PCC (Q28)
ML2258CIJ		±1LSB	–40°C to +85°C	Hermetic DIP (J28)
ML2258CIP	ADC0809CCN		–40°C to +85°C	Molded DIP (P28)
ML2258CIQ	ADC0809CCV		–40°C to +85°C	Molded PCC (Q28)

Micro Linear

ML2261

μP Compatible High-Speed 8-Bit A/D Converter with T/H (S/H)

GENERAL DESCRIPTION

The ML2261 is a high-speed, μP compatible 8-bit A/D converter with a conversion time of 670ns over the operating temperature range and supply voltage tolerance. The ML2261 operates from a single 5V supply and has an analog input range from GND to V_{CC}.

The ML2261 has two different pin selectable modes. The T/H mode has an internal track and hold. The S/H mode has a true internal sample and hold and can digitize 0 to 5V sinusoidal signals as high as 500kHz. Timing is compatible with the AD7821.

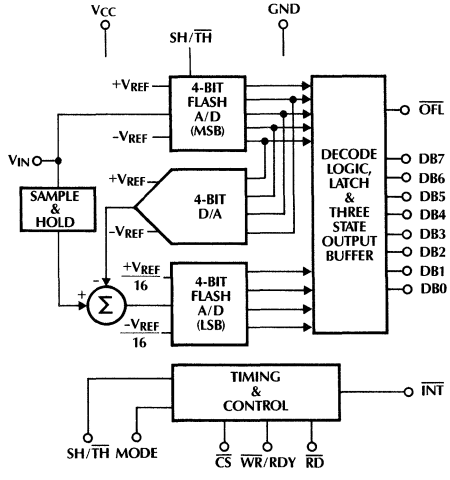
The ML2261 digital interface has been designed so that the device appears as a memory location or I/O port to a μP.

The ML2261 is an enhanced, pin compatible second source for the industry standard ADC0820 and AD7820. The ML2261 enhancements are faster conversion time, parameters guaranteed over the supply tolerance and temperature range, improved digital interface timing, superior power supply rejection, and better latchup immunity on analog inputs.

FEATURES

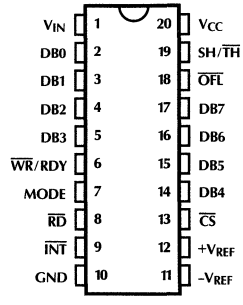
- Conversion time, WR-RD mode over temperature and supply voltage tolerance
  - Track & Hold Mode ..... 850ns max
  - Sample & Hold Mode ..... 700ns max
- Total unadjusted error ..... ±1/2 LSB or ±1 LSB
- Digitizes a 5V, 250kHz sine wave to 8-bit accuracy
- No missing codes
- 0V to 5V analog input range with single 5V power supply
- No zero or full scale adjust required
- Analog input protection ..... 25mA min
- Operates ratiometrically or with up to 5V voltage reference
- No external clock required
- Easy interface to μP, or operates stand alone
- Power-on reset circuitry
- Low power 75mW
- Standard 20-pin DIP or surface mount PCC
- Superior pin compatible replacement for ADC0820 and AD7820

BLOCK DIAGRAM



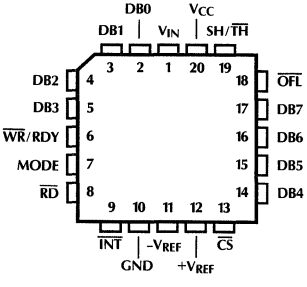
PIN CONNECTIONS

20-Pin DIP



TOP VIEW

20-Pin PCC



TOP VIEW

Micro Linear

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	V_{IN}	Analog input.
2	DB0	Data output — bit 0 (LSB).
3	DB1	Data output — bit 1.
4	DB2	Data output — bit 2.
5	DB3	Data output — bit 3.
6	$\overline{WR}$/RDY	Write input or ready output. In WR-RD mode, this pin is WR input. In RD mode, this pin is RDY open drain output. See Digital Interface section.
7	MODE	Mode select input. MODE = GND: RD mode MODE = V_{CC}: WR-RD mode Pin has internal current source pulldown to GND.
8	$\overline{RD}$	Read input. In RD mode, this pin initiates a conversion. In WR-RD mode, this pin latches data into output latches. See Digital Interface section.
9	$\overline{INT}$	Interrupt output. This output signals the end of a conversion and indicates that data is valid on the data outputs. See Digital Interface section.
10	GND	Ground.
11	$-V_{REF}$	Negative reference voltage for A/D converter.
12	$+V_{REF}$	Positive reference voltage for A/D converter.
13	$\overline{CS}$	Chip select input. This pin must be held low for the device to perform a conversion.
14	DB4	Data output — bit 4.
15	DB5	Data output — bit 5.
16	DB6	Data output — bit 6.
17	DB7	Data output — bit 7 (MSB).
18	$\overline{OFL}$	Overflow output. This output goes low at end of conversion if V_{IN} is greater than $+V_{REF}$ – ½LSB.
19	SH/$\overline{TH}$	S/H, T/H mode select. When SH/$\overline{TH}$ = V_{CC}, the device is in sample and hold mode. When SH/$\overline{TH}$ = GND, the device is in track and hold mode. Pin has internal pulldown current source to GND.
20	V_{CC}	Positive supply. +5 volts ± 5%.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage, V_{CC} 6.5V
Voltage
- Logic Inputs ..... –0.3V to V_{CC} + 0.3V
- Analog Inputs ..... –0.3V to V_{CC} + 0.3V

Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Package Dissipation
- at T_A = 25°C (Board Mount) 875mW

Lead Temperature (Soldering 10 sec.)
- Dual-In-Line Package (Plastic) ..... 260°C
- Dual-In-Line Package (Ceramic) ..... 300°C
- Molded Chip Carrier Package
  - Vapor Phase (60 sec.) ..... 215°C
  - Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... $4.5V_{DC}$ to $6.0V_{DC}$
Temperature Range (Note 3) ..... $T_{MIN} \leq T_A \leq T_{MAX}$
- ML2261BIJ, ML2261CIJ ..... –40°C to +85°C
- ML2261BCQ, ML2261CCQ
- ML2261BCP, ML2261CCP ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, and $-V_{REF} = GND$

PARAMETER	NOTES	CONDITIONS	ML2261XCX MIN	ML2261XCX TYP (Note 4)	ML2261XCX MAX	ML2261XIX MIN	ML2261XIX TYP (Note 4)	ML2261XIX MAX	UNITS
Converter									
Total Unadjusted Error ML2261BXX ML2261CXX	5, 7	$V_{REF} = V_{CC}$			±1/2 ±1			±1/2 ±1	LSB LSB
$+V_{REF}$ Voltage Range	6		$-V_{REF}$		$V_{CC}+0.1$	$-V_{REF}$		$V_{CC}+0.1$	V
$-V_{REF}$ Voltage Range	6		GND–0.1		$+V_{REF}$	GND–0.1		$+V_{REF}$	V
Reference Input Resistance	5		1	2	3	1	2	3	kΩ
Analog Input Range	5, 8		GND–0.1		$V_{CC}+0.1$	GND–0.1		$V_{CC}+0.1$	V
Power Supply Sensitivity	5	DC $V_{CC} = 5V \pm 5\%$, $V_{REF} = 4.75V$		±1/32	±1/4		±1/32	±1/4	LSB
		100mVp-p 100kHz sine on V_{CC}, $V_{IN} = 0$		±1/16			±1/16		LSB
Analog Input Leakage Current	5, 9	Converter Idle	–1		+1	–1		+1	µA
Analog Input Capacitance		During Acquisition Period		45			45		pF
Digital and DC									
$V_{IN(1)}$, Logical "1" Input Voltage	5	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$	2.0			2.0			V
		MODE, SH/$\overline{TH}$	V_{CC}–0.5			V_{CC}–0.5			V
$V_{IN(0)}$, Logical "0" Input Voltage	5	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$			0.8			0.8	V
		MODE, SH/$\overline{TH}$			0.5			0.5	V
$I_{IN(1)}$, Logical "1" Input Current	5	$V_{IH} = V_{CC}$; $\overline{WR}$, $\overline{RD}$, $\overline{CS}$			1			1	µA
		$V_{IH} = V_{CC}$; MODE, SH/$\overline{TH}$	15	50	150	15	50	150	µA
$I_{IN(0)}$, Logical "0" Input Current	5	$V_{IL} = GND$; $\overline{WR}$, $\overline{RD}$, $\overline{CS}$	–1			–1			µA
		$V_{IL} = GND$; MODE, SH/$\overline{TH}$	–20			–20			µA
$V_{OUT(1)}$, Logical "1" Output Voltage	5	$I_{OUT} = -2mA$	4.0			4.0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	5	$I_{OUT} = 2mA$			0.4			0.4	V
I_{OUT}, Three-State Output Current	5	$V_{OUT} = 0V$	–1			–1			µA
		$V_{OUT} = V_{CC}$			1			1	µA
C_{OUT}, Logic Output Capacitance				5			5		pF
C_{IN}, Logic Input Capacitance				5			5		pF
I_{CC}, Supply Current	5	$\overline{CS} = \overline{WR} = \overline{RD}$ = "1" No Output Load		8	14		8	15.5	mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, $-V_{REF}$ = GND, and timing measured at 1.4V, C_L = 100pF.

PARAMETER	NOTES	CONDITIONS	ML2261XCX MIN	ML2261XCX TYP (Note 4)	ML2261XCX MAX	ML2261XIX MIN	ML2261XIX TYP (Note 4)	ML2261XIX MAX	UNITS
AC and Dynamic Performance (Note 9)									
t_{CRD}, Conversion Time, Read Mode	5	$\overline{RD}$ to $\overline{INT}$, MODE = 0V			1060			1100	ns
t_{CWR-RD}, Conversion Time, Write-Read Mode	5, 9	$\overline{WR}$ Falling Edge to $\overline{INT}$, $t_{RD} < t_{INT}$, MODE = V_{CC}; SH/$\overline{TH}$=V_{CC}		650	700		690	740	ns
		$\overline{WR}$ Falling Edge to $\overline{INT}$, $t_{RD} < t_{INT}$, MODE = V_{CC}; SH/$\overline{TH}$=GND			850			920	ns
SNR, Signal to Noise Ratio		V_{IN} = 5V, 250kHz Noise is sum of all nonfundamental components from 0–500kHz. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1 MHz		48			48		dB
HD, Harmonic Distortion		V_{IN} = 5V, 250kHz THD is sum of 2–5th harmonics relative to fundamental. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1 MHz		–63			–63		dB
IMD, Intermodulation Distortion		fa = 2.5V, 250kHz fb = 2.5V, 248kHz IMB is (fa + fb), (fa – fb), (2fa + fb), (2fa – fb), (fa + 2fb), or (fa – 2fb) relative to fundamental. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1 MHz		–60			–60		dB
FR, Frequency Response		V_{IN} = 5V, 0–250kHz Relative to 1kHz SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1 MHz		±0.1			±0.1		dB
SR, Slew Rate Tracking	6	SH/$\overline{TH}$ = V_{CC}			4.0			4.0	V/μs
		SH/$\overline{TH}$ = GND			.25			.25	V/μs
AC Performance Read Mode (Pin 7 = 0V), Figure 2									
t_{RDY}, $\overline{CS}$ to RDY Delay	5		0		65	0		70	ns
t_{RDD}, $\overline{RD}$ Low to RDY Delay	5, 10	Figure 1			1060			1100	ns
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	5		0			0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	5		0			0			ns
t_{CRD}, Conversion Time — $\overline{RD}$ Low to $\overline{INT}$ Low	5, 10				1060			1100	ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, $-V_{REF}$ = GND, and timing measured at 1.4V, C_L = 100pF

PARAMETER	NOTES	CONDITIONS	ML2261XCX			ML2261XIX			UNITS
			MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
AC Performance Read Mode (Pin 7 = 0V), Figure 2 (Continued)									
t_{ACC0}, Data Access Time $\overline{RD}$ to Data Valid	5		t_{CRD}		t_{CRD}+30	t_{CRD}		t_{CRD}+30	ns
t_{RDPW}, $\overline{RD}$ Pulse Width	5		t_{CRD}+30			t_{CRD}+30			ns
t_{INTH}, $\overline{RD}$ to $\overline{INT}$ Delay	5, 10		0		65	0		70	ns
t_{DH}, Data Hold Time — $\overline{RD}$ Rising Edge to Data High Impedance State	6, 10	Figure 1	0		50	0		60	ns
t_P, Delay Time Between Conversions — $\overline{INT}$ Low to $\overline{RD}$ Low	5, 10	Sample & Hold Mode, SH/$\overline{TH}$ = V_{CC}	300			325			ns
		Track & Hold Mode, SH/$\overline{TH}$ = GND	240			260			ns
AC Performance Write-Read Mode (Pin 7 = 5V), Figures 3 and 4									
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	5		0			0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	5		0			0			ns
t_{WR}, $\overline{WR}$ Pulse Width	5	SH/$\overline{TH}$ = V_{CC}	170		50K	180		50K	ns
	6	SH/$\overline{TH}$ = GND	320		50K	360		50K	ns
t_{RD}, Read Time — $\overline{WR}$ High to $\overline{RD}$ Low Delay	5	$t_{RD} < t_{INTL}$	275			290			ns
t_{RI}, $\overline{RD}$ to $\overline{INT}$ Delay	5, 10	$t_{RD} < t_{INTL}$	0		255	0		270	ns
t_{ACC1}, Data Access Time — $\overline{RD}$ Low to Data Valid	5	$t_{RD} < t_{INTL}$	0		260	0		280	ns
t_{CWR-RD}, Conversion Time — $\overline{WR}$ Falling Edge to $\overline{INT}$ Low	5,9,10	$t_{RD} < t_{INTL}$, SH/$\overline{TH}$ = V_{CC}		650	700		690	740	ns
	6,9,10	$t_{RD} < t_{INTL}$, SH/$\overline{TH}$ = GND			850			920	ns
t_{INTL}, Internal Comparison Time — $\overline{WR}$ Rising Edge to $\overline{INT}$ Low	5, 10	$t_{RD} > t_{INTL}$			650			670	ns
t_{ACC2}, Data Access Time — $\overline{RD}$ to Data Valid	5	$t_{RD} > t_{INTL}$	0		50	0		60	ns
t_{DH}, Data Hold Time — $\overline{RD}$ Rising Edge to Data High Impedance State	6, 10	Figure 1	0		50	0		60	ns
t_{INTH}, $\overline{RD}$↑ to $\overline{INT}$↑ Delay	5, 10		0		65	0		70	ns
t_P, Delay Time Between Conversions — $\overline{INT}$ Low to $\overline{WR}$ Low	5, 10	Sample & Hold Mode, SH/$\overline{TH}$ = V_{CC}	300			325			ns
		Track & Hold Mode, SH/$\overline{TH}$ = GND	240			260			ns
t_{IHWR}, $\overline{WR}$↑ to $\overline{INT}$↑ Delay	5, 10	Standalone Mode	0		100	0		110	ns
t_{ID}, $\overline{INT}$↓ to Data Valid Delay	5, 10	Standalone Mode	0		20	0		30	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: When the voltage at any pin exceeds the power supply rails (V_{IN} < GND or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: 0°C to +70°C and -40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Total unadjusted error includes offset, full scale, linearity, and sample and hold errors. Total unadjusted error is tested at the minimum specified times for $\overline{WR}$, $\overline{RD}$, t_{RI}, and t_P. For example, for the ML2261XCX in the sample and hold mode, $\overline{WR}/\overline{RD}$ mode: t_{WR} = 170ns, t_{RD} = 275ns with a frequency of 1.00MHz (cycle time of 1000ns).

Note 8: For $-V_{REF} \geq V_{IN}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to the analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct — especially at elevated temperatures, and cause errors for analog inputs near full scale. The spec allows 100mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of $4.900V_{DC}$ over temperature variations, initial tolerance and loading.

Note 9: Conversion time, write-read mode = t_{WR} + t_{RD} + t_{RI}.

Note 10: Defined from the time an output crosses 0.8V or 2.4V.

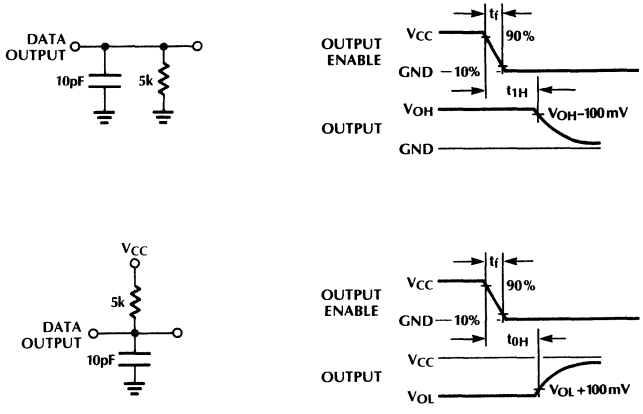


Figure 1. High Impedance Test Circuits and Waveforms

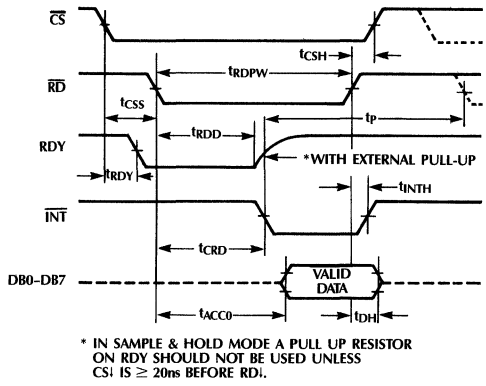


Figure 2. RD Mode Timing

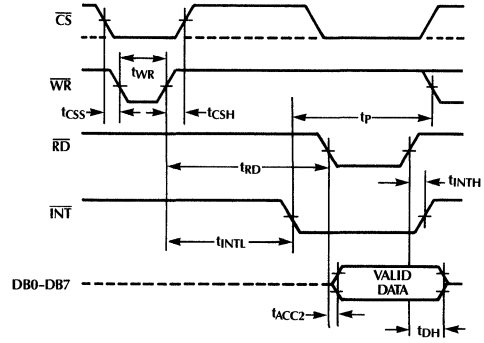


Figure 3. WR-RD Mode Timing ($t_{RD} > t_{INTL}$)

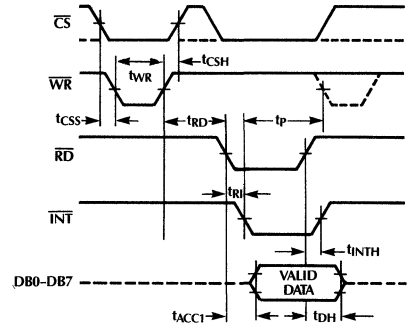


Figure 4. WR-RD Mode Timing ($t_{RD} < t_{INTL}$)

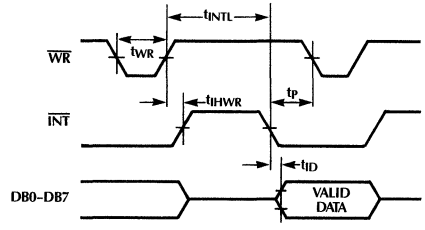


Figure 5. WR-RD Mode Stand-Alone Timing $\overline{CS}$ = $\overline{RD}$ = 0

1.0 FUNCTIONAL DESCRIPTION

The ML2261 uses a two stage flash technique for A/D conversion. This technique first performs a 4 bit flash conversion on V_{IN} to determine the 4 MSB's. These 4 MSB's are then cycled through an internal DAC to recreate the analog input. This reconstructed analog input signal from the DAC is then subtracted from the input, and the difference voltage is converted by a second 4 bit flash conversion, providing the 4 LSB's of the output data word. An additional overrange function detects if V_{IN} is greater than $+V_{REF}$ – ½LSB.

1.1 ANALOG INPUT

The analog input on the ML2261 behaves differently than inputs on conventional converters. The analog input current requirements change while the conversion is in progress, and the amount of input current depends on what cycle the converter is in.

The equivalent input circuit for the converter is shown in Figure 6. When the conversion starts in the T/H mode ($\overline{WR}\downarrow$ in the WR-RD mode or $\overline{RD}\downarrow$ in the RD mode) S1, S4 and S6 close and S3 opens. This period is known as the acquisition period where the MSB flash converter tracks the input signal and the LSB flash converter samples it. During this period, V_{IN} is connected to the 16 MSB and 15 LSB comparators. Thus 38 pF of input capacitance must be charged up through the combined R_{ON} resistance of the internal analog switches plus any external source resistance, R_S. In addition, there is a stray capacitance of approximately 11 pF that needs to be charged through the external source resistance R_S. This period ends in the WR-RD mode when $\overline{WR}\uparrow$ or by an internal timer in the RD mode. At this point S1 and S4 open and the analog input at V_{IN} is no longer being sampled; thus during this time the analog voltage on V_{IN} does not affect converter performance.

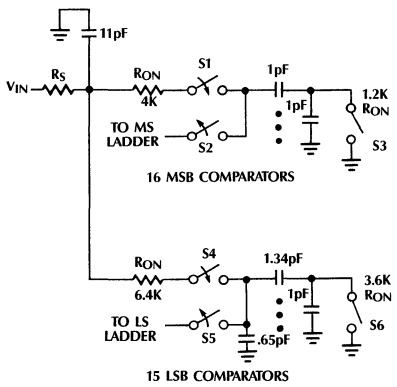


Figure 6. Converter Equivalent Input Circuit

As shown above, the critical period for charging up the analog input occurs when the MSB and LSB comparators are sampling the input, known as the acquisition period. The source of the external signal on V_{IN} must adequately charge up the analog voltage during the acquisition period. To do this, the input must settle within the required analog accuracy tolerance at least 50ns before the end of the acquisition period so that the MSB comparators have adequate time to make the correct decision. If more time is needed due to finite charging or settling time of the external source, the $\overline{WR}$ low period can be extended in WR-RD mode. In RD mode, since the acquisition time is fixed by internal delays, the burden is on the external source to charge up and settle the input adequately.

When the ML2261 operates in the S/H mode (pin 19 = V_{CC}) both the MSB and the LSB flash converter perform a true sample and hold operation during the acquisition or sampling period. This period starts after the falling edge of $\overline{INT}$ and ends with the falling edge of $\overline{WR}$ in the WR-RD mode or the falling edge of $\overline{RD}$ in the RD mode. The duration of this period is user controlled and must satisfy a minimum of t_P.

During this period S1, S3, S4 and S6 close, therefore 46 pF of input capacitance must be charged up in addition to the 11 pF of stray capacitance.

1.2 TRACK AND HOLD vs. SAMPLE AND HOLD

The MSB Flash Converter of the ML2261 in T/H mode has a track and hold mechanism for sampling the input. The input is attached to the MSB comparators directly in the MSB compare cycle, or acquisition period. When the MSB compare cycle ends, the state of the MSB comparators is latched. The LSB Flash Converter always performs a S/H operation. Thus, the analog input signal can be changing during the MSB compare cycle, or acquisition period, and the MSB comparators will be tracking it as long as the slew rate of the analog input is slow enough so that the MSB comparators can respond. The ML2261 can track and hold signals with slew rates as high as .25V/μs (16kHz @ 5 volts) without sacrificing conversion accuracy.

The ML2261 in S/H mode does not have the slew rate limitation of the T/H mode since an internal sample and hold acquires the analog signal, holds it internally, and then performs a conversion. Since this is a true sample and hold function, the S/H mode can theoretically digitize signals of frequencies much higher than the T/H mode. The ML2261 in S/H mode can digitize signals of frequencies as high as 250kHz @ 5V (slew rates as high as 4V/μs) without sacrificing conversion accuracy. In most applications, the S/H mode is more desirable than T/H mode because of the better dynamic performance.

1.2.1 CONVERTER — T/H MODE

The operating sequence for the WR-RD mode is illustrated in Figure 7a. Initially, the internal comparators are auto-zeroed while WR is high. A conversion is initiated by the falling edge of WR. While WR is low, the MSB comparators are tracking the analog input and comparing this voltage against voltages from the internal resistor ladder. At the same time, the input is being acquired or sampled by LSB comparators. On the rising edge of WR, the MSB comparator results are latched, and the LSB acquisition time is ended by closing the sampling switch to the LSB comparators. While WR is high, the LSB comparators then compare the residual input voltage against internal voltages from the resistor ladder to determine the 4 LSB's. When the LSB comparison or conversion is complete, INT goes low and latches the conversion result into the output latches. Then, the comparators are auto-zeroed while WR is high before another conversion can start.

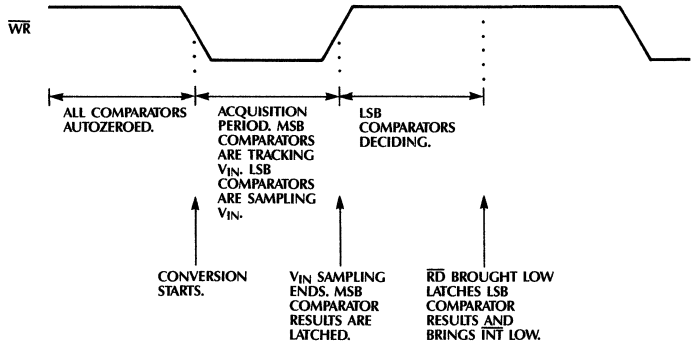
The operating sequence for RD mode, is similar to that described above for the WR-RD mode, except the conversion is initiated by the falling edge of RD, and the MSB and LSB conversions are generated by internal clock edges that are generated while RD is low.

1.2.2 CONVERTER — S/H MODE

The operating sequence for S/H mode is illustrated in Figure 7b. Notice that it is similar to T/H mode described above except this mode has a true sample and hold function. The falling edge of INT closes the sampling switch and starts the acquisition period where the analog input is sampled at the same time all comparators are auto-zeroed. The falling edge of WR opens the internal sampling switch, ends the acquisition period, and starts the conversion on the internally sample and held signal. The MSB comparators make their decisions while WR is low. On the rising edge of WR, the MSB comparator results are latched. The LSB comparators make their decision when WR is high. When the LSB comparison or conversion is complete, INT goes low and latches the conversion result into the output buffers. Then, the acquisition period begins again and the converter is ready for the next conversion.

The operating sequence for the RD mode is the same as the WR-RD mode, except the conversion is initiated by the falling edge of RD, and the MSB and LSB conversions are generated by internal clock edges that are generated while RD is low.

a). T/H Mode



b). S/H Mode

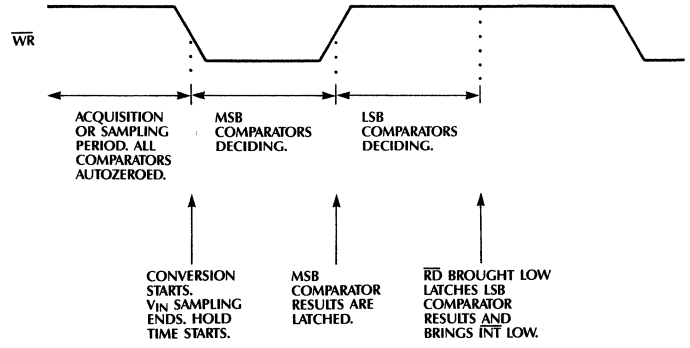


Figure 7. Operating Sequence (WR-RD Mode)

1.3 REFERENCE

The $+V_{REF}$ and $-V_{REF}$ inputs are the reference voltages that determine the full scale and zero input voltages, respectively, for the A/D converter. Thus, $+V_{REF}$ defines the analog input which produces a full scale output and $-V_{REF}$ defines the analog input which produces an output code of all zeroes. The transfer function for the A/D converter is shown in Figure 8.

$+V_{REF}$ and $-V_{REF}$ can be set to any voltage between GND and V_{CC}. This means that the reference voltages can be offset from GND and the difference between $+V_{REF}+$ and $-V_{REF}-$ can be made small to increase the resolution of the conversion. Note that the total unadjusted error increases when $[+V_{REF} - (-V_{REF})]$ decreases.

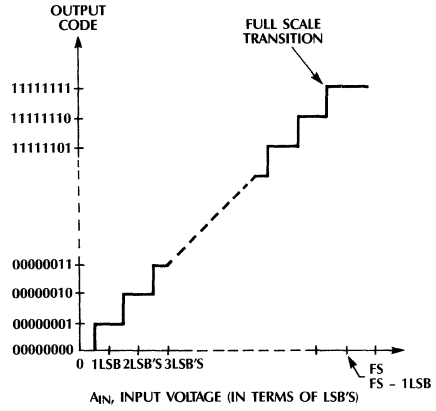


Figure 8. A/D Transfer Characteristic

1.4 POWER SUPPLY AND REFERENCE DECOUPLING

A 0.1μF ceramic disc capacitor is recommended to bypass V_{CC} to GND, using as short a lead length as possible.

If REF+ and REF– inputs are driven by long lines, they should be bypassed by 0.1μF ceramic disc capacitors at the reference input pins.

1.5 DYNAMIC PERFORMANCE

1.5.1 SINUSOIDAL INPUTS

Since the ML2261 has an internal sample and hold, the device can digitize high frequency sinusoids with little or no signal degradations. Using the Nyquist criteria, the highest frequency input to the converter could theoretically be 1/2 the sampling rate (f_s). Any frequency components above $f_s/2$ will be aliased below $f_s/2$. In most applications, these aliased components cause unacceptable distortion and must be filtered out of the input. If the input frequency is too close to $f_s/2$, then the requirements on the anti-alias filter become difficult to impossible to realize with standard component and tolerances. In most practical applications, the highest input frequency has to be limited to 1/3 to 1/4 of f_{max} in order to relax the filtering requirements enough to make a realizable anti-alias filter.

The maximum sampling rate (f_{max}) for the ML2261 in the WR-RD mode, ($t_{RD} < t_{INTL}$) can be calculated as follows:

$$f_{max} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_P}$$

$$f_{max} = \frac{1}{170ns + 275ns + 255ns + 300ns}$$

f_{max} = 1.00 MHz

t_{WR} = Write Pulse Width

t_{RD} = Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses

t_{RI} = $\overline{RD}$ to $\overline{INT}$ Delay

t_P = Delay Time between Conversions

This permits a maximum sampling rate of 1MHz for the ML2261. The dynamic performance specifications (SNR, HD, IMD, and FR) for the ML2261 are all specified at 250kHz, which is approximately 1/4 of the sampling rate, f_s.

In applications where aliased frequency components are acceptable and filtering of the input signal is not needed or where a filter with a steep amplitude response is available, the user can apply an input sinusoid higher than 250kHz to the device. Note, however, that as the input frequency increases above 500kHz, dynamic performance degradation will occur due to the finite bandwidth of the internal sample and hold.

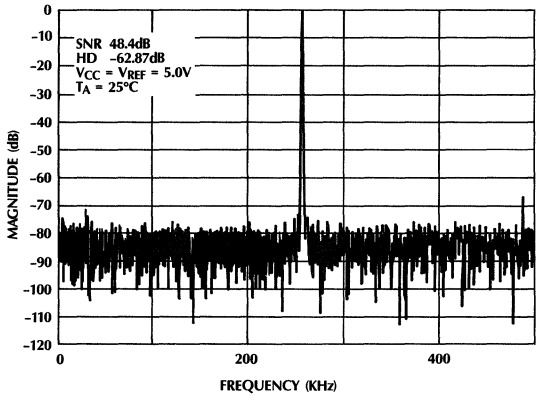
The Figure 9 plots are 4096 point FFT's of the ML2261 converting a 257kHz and a 491kHz, 0 to 4.5V, low distortion sine wave input. The ML2261 samples and digitizes at its specified accuracy, dynamic input signals with frequency components up to the Nyquist frequency (one-half the sampling rate). The output spectra yields precise measurements of the input signal level, harmonic components, and signal to noise ratio up to the 8-bit level. The near ideal signal to noise ratio is maintained independent of increasing analog input frequencies to 500kHz.

1.5.2 SIGNAL-TO-NOISE RATIO

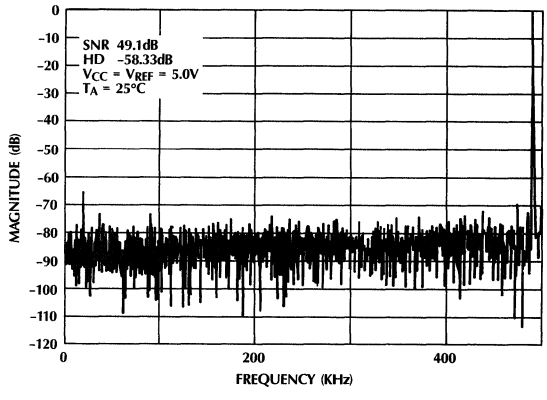
Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more the levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92 dB.



a) Ouput Spectrum with f_{IN} = 257kHz, f_S = 1MHz



b) Output Spectrum with f_{IN} = 491kHz, f_S = 1MHz

Figure 9. Dynamic Performance, Sample and Hold Mode

1.5.3 HARMONIC DISTORTION

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2261 is defined as

$$20 \log = \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

1.5.4 INTERMODULATION DISTORTION

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of $mf_A + nf_B$, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. The (IMD) intermodulation distortion specification includes the second order terms ($f_A + f_B$) and ($f_A - f_B$) and the third order terms ($2f_A + f_B$), ($2f_A - f_B$), ($f_A + 2f_B$), and ($f_A - 2f_B$) only.

1.6 DIGITAL INTERFACE

The ML2261 has two basic interface modes, RD and WR-RD, which are selected by the MODE input pin.

1.6.1 RD MODE

In the RD mode, the $\overline{WR}$/RDY pin is configured as the RDY output. The read mode performs a conversion with a single $\overline{RD}$ pulse. This allows the μP to start a conversion, wait, and then read data with a single read instruction.

The timing for the $\overline{RD}$ mode is shown in Figure 2. To do a conversion, $\overline{CS}$ must be low to select the device. After $\overline{CS}$ goes low, the RDY output goes low indicating that the device is ready to do a conversion. The conversion starts on the falling edge of $\overline{RD}$. While $\overline{RD}$ is low, the MSB and LSB decisions are made with internally generated clock edges. When the conversion is complete, RDY goes high and $\overline{INT}$ goes low signaling the end of the conversion. After $\overline{INT}$ goes low, the data outputs go from high impedance to active state with valid output data. Data stays valid until either $\overline{RD}$ or $\overline{CS}$ goes high. When either signal goes high, the output data lines return to the high impedance state and $\overline{INT}$ returns high. A pull up resistor on RDY in the sample and hold mode will cause clock injection, degrading the total unadjusted error, unless $\overline{CS}\downarrow$ is $\geq$ 20ns before $\overline{RD}\downarrow$.

1.6.2 WR-RD MODE

In the WR-RD mode, the $\overline{WR}$/RDY pin is configured as the $\overline{WR}$ input. In this mode, $\overline{WR}$ initiates the conversion and $\overline{RD}$ controls reading the output data. This can be done in several ways, described below.

1.6.3 WR-RD MODE — USING INTERNAL DELAY ($t_{RD} > t_{INTL}$)

The timing is shown in Figure 3. To do a conversion, $\overline{CS}$ must be low to select the device. Then, $\overline{WR}$ falling edge triggers the conversion. While $\overline{WR}$ is low, the MSB comparison is made. When $\overline{WR}$ returns high the LSB decision is made. After some internal delay, $\overline{INT}$ goes low indicating end of conversion. Valid data will appear on DB0–7 when $\overline{RD}$ is pulled low. $\overline{INT}$ is then reset by the rising edge of either $\overline{CS}$ or $\overline{RD}$.

1.6.4 WR-RD MODE — READING BEFORE DELAY ($t_{RD} < t_{INTL}$)

The internally generated delay for the LSB decision when $t_{RD} > t_{INTL}$ is longer than necessary due to circuit design tolerances of t_{INTL} delay. If desired, a faster conversion will result without loss of accuracy by bringing $\overline{RD}$ low within the minimum time specified for t_{RD}. The timing diagram for this mode is shown in Figure 4. $\overline{WR}$ is the same as when $t_{RD} > t_{INTL}$. But in this case, $\overline{RD}$ is brought low t_{RD} ns after $\overline{WR}$ rising edge and before $\overline{INT}$. $\overline{INT}$ goes low indicating an end of conversion after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. When $\overline{RD}$ is brought low before $\overline{INT}$ goes low the data bus always remains in the high-impedance state until $\overline{INT}\downarrow$.

1.6.5 WR-RD MODE — STAND ALONE OPERATION

Stand alone operation can be implemented by tying $\overline{CS}$ and $\overline{RD}$ low as shown in Figure 5. $\overline{WR}$ initiates a conversion as before. When $\overline{WR}$ is low, the MSB comparison is made. When $\overline{WR}$ goes high, the LSB comparison is made. Since $\overline{RD}$ is already low, the output data will appear automatically at end of conversion. Since $\overline{RD}$ is always low, $\overline{INT}$ is reset on rising edge of $\overline{WR}$ and goes low at end of conversion.

1.6.6 POWER-ON RESET

When power is first applied, an internal power-on reset and timer circuit inhibits the $\overline{CS}$ input and resets the internal circuitry to prevent the ML2261 from starting in an unknown state. During this period of approximately 3μs, $\overline{INT}$ remains high and the data bus is in the high-impedance state.

2.0 TYPICAL APPLICATIONS

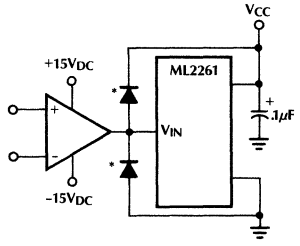


Figure 10. Protecting the Input

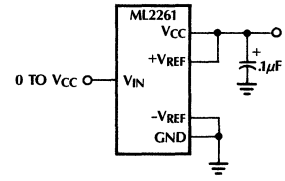


Figure 11. Using V_{CC} as Reference for Ratiometric Operation

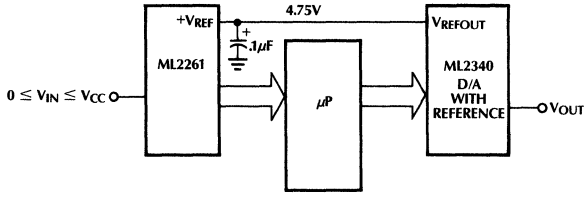


Figure 12. Using External Reference of D/A

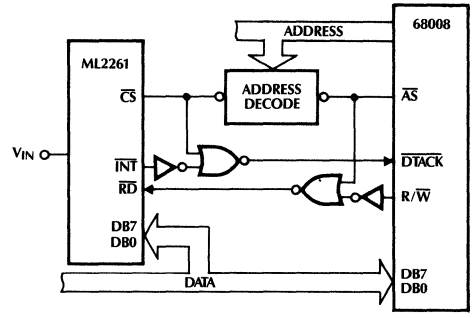


Figure 13. 68000 Type Interface to ML2261

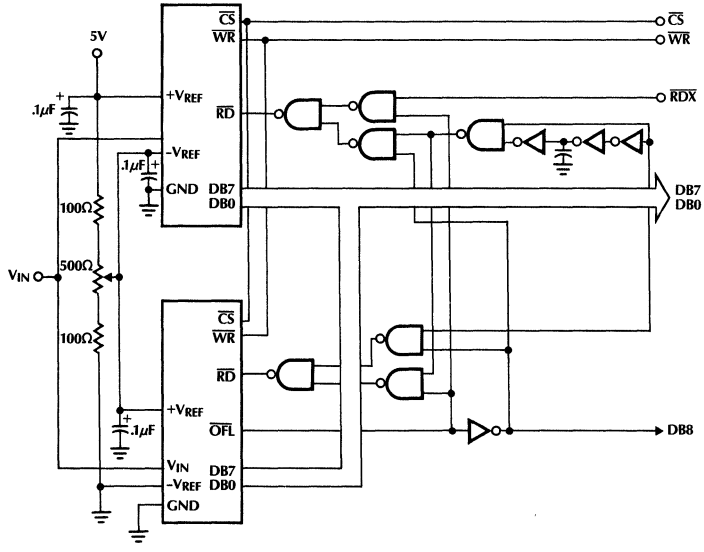


Figure 14. 9-Bit Resolution

2.0 TYPICAL APPLICATIONS (Continued)

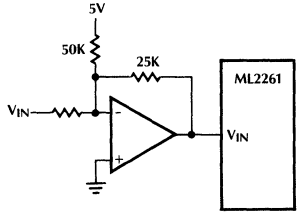


Figure 15. ±2.5V Analog Input Range

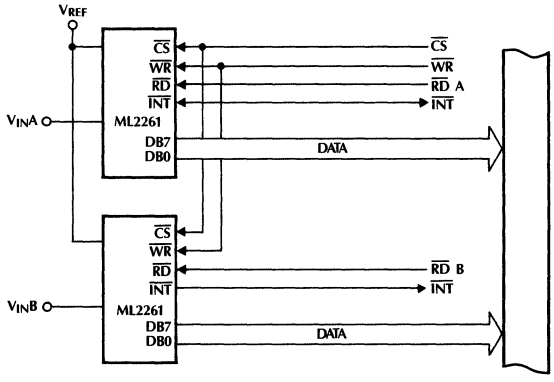


Figure 16. Simultaneous Sampling of Two Variables

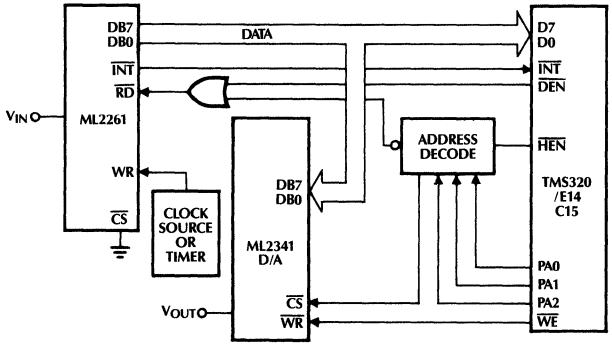


Figure 17. TMS320 Interface with D/A Output

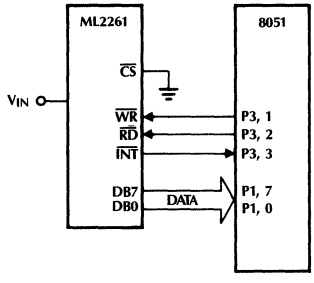


Figure 18. 8051 Interface to ML2261

TYPICAL APPLICATIONS (Continued)

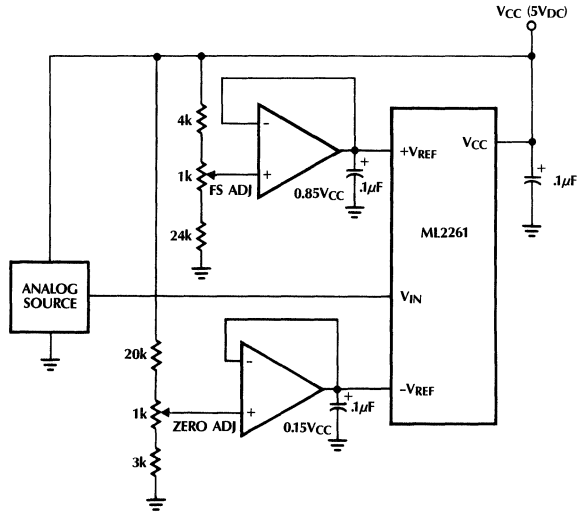


Figure 19. Operating with a Ratiometric Analog Signal of 15% of V_{CC} to 85% of V_{CC}

ORDERING INFORMATION

PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
ML2261BIJ	±½ LSB	–40°C to +85°C	HERMETIC DIP (J20)
ML2261BCP		0°C to +70°C	MOLDED DIP (P20)
ML2261BCQ		0°C to +70°C	MOLDED PCC (Q20)
ML2261CIJ	±1 LSB	–40°C to +85°C	HERMETIC DIP (J20)
ML2261CCP		0°C to +70°C	MOLDED DIP (P20)
ML2261CCQ		0°C to +70°C	MOLDED PCC (Q20)

ML2264

4-Channel High-Speed 8-Bit A/D Converter with T/H (S/H)

GENERAL DESCRIPTION

The ML2264 is a high-speed, µP compatible, 4-channel 8-bit A/D converter with a conversion time of 680ns over the operating temperature range and supply voltage tolerance. The ML2264 operates from a single 5V supply and has an analog input range from GND to V_{CC}.

The ML2264 has two different pin selectable modes. The T/H mode has an internal track and hold. The S/H mode has a true internal sample and hold and can digitize 0 to 5V sinusoidal signals as high as 500kHz.

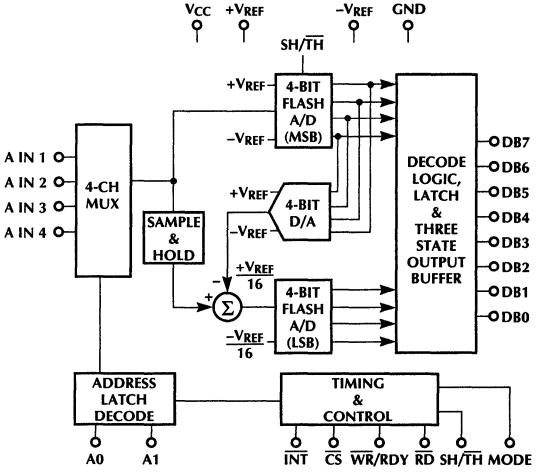
The ML2264 digital interface has been designed so that the device appears as a memory location or I/O port to a µP. Analog input channels are selected by the latched and decoded multiplexer address inputs.

The ML2264 is an enhanced, pin compatible second source for the industry standard AD7824. The ML2264 enhancements are faster conversion time, parameters guaranteed over the supply tolerance and temperature range, improved digital interface timing, superior power supply rejection, and better latchup immunity on analog inputs.

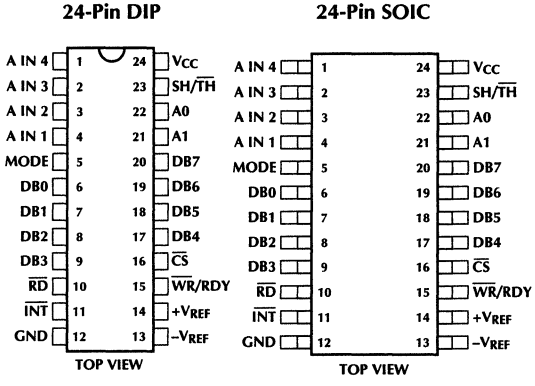
FEATURES

- Conversion time, WR-RD mode over temperature and supply voltage tolerance
  - Track & Hold Mode ..... 830ns max
  - Sample & Hold Mode ..... 700ns max
- Total unadjusted error ..... ±1/2 LSB or ±1 LSB
- Capable of digitizing a 5V, 250kHz sine wave
- 4-analog input channels
- No missing codes
- 0V to 5V analog input range with single 5V power supply
- No zero or full scale adjust required
- Analog input protection ..... 25mA min
- Operates ratiometrically or with up to 5V voltage reference
- No external clock required
- Power-on reset circuitry
- Low power 100mW
- Narrow 24-pin DIP or surface mount SOIC
- Superior pin compatible replacement for AD7824

BLOCK DIAGRAM



PIN CONNECTIONS



PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	A IN 4	Analog input 4.
2	A IN 3	Analog input 3.
3	A IN 2	Analog input 2.
4	A IN 1	Analog input 1.
5	MODE	Mode select input. MODE = GND: RD mode MODE = V_{CC}: WR-RD mode Pin has internal current source pulldown to GND.
6	DB0	Data output — bit 0 (LSB).
7	DB1	Data output — bit 1.
8	DB2	Data output — bit 2.
8	DB3	Data output — bit 3.
10	$\overline{RD}$	Read input. In RD mode, this pin initiates a conversion. In WR-RD mode, this pin latches data into output latches. See Digital Interface section.
11	$\overline{INT}$	Interrupt output. This output signals the end of a conversion and indicates that data is valid on the data outputs. See Digital Interface section.
12	GND	Ground.
13	$-V_{REF}$	Negative reference voltage for A/D converter.
14	$+V_{REF}$	Positive reference voltage for A/D converter.
15	$\overline{WR}$/RDY	Write input or ready output. In WR-RD mode, this pin is $\overline{WR}$ input. In RD mode, this pin is RDY open drain output. See Digital Interface section.
16	$\overline{CS}$	Chip select input. This pin must be held low for the device to perform a conversion.
17	DB4	Data output — bit 4.
18	DB5	Data output — bit 5.
19	DB6	Data output — bit 6.
20	DB7	Data output — bit 7 (MSB).
21	A1	Digital address input 1 that selects analog input channel. See multiplexer addressing section.
22	A0	Digital address input 0 that selects analog input channel. See multiplexer addressing section.
23	SH/$\overline{TH}$	S/H, T/H mode select. When SH/$\overline{TH}$ = V_{CC}, the device is in sample and hold mode. When SH/$\overline{TH}$ = GND, the device is in track and hold mode. Pin has internal pulldown current source to GND.
24	V_{CC}	Positive supply. +5 volts ± 5%.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage, V_{CC} 6.5V
Voltage
  Logic Inputs ..... –0.3V to V_{CC} + 0.3V
  Analog Inputs ..... –0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Package Dissipation
  at T_A = 25°C (Board Mount) 875mW
Lead Temperature (Soldering 10 sec.)
  Dual-In-Line Package (Plastic) ..... 260°C
  Dual-In-Line Package (Ceramic) ..... 300°C
  SOIC
    Vapor Phase (60 sec.) ..... 215°C
    Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... $4.5V_{DC}$ to $6.0V_{DC}$
Temperature Range (Note 3) ..... $T_{MIN} \le T_A \le T_{MAX}$
  ML2264BMJ, ML2264CMJ ..... –55°C to +125°C
  ML2264BIJ, ML2264CIJ ..... 40°C to +85°C
  ML2264BCS, ML2264CCS
  ML2264BCP, ML2264CCP ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, and $-V_{REF} = GND$

PARAMETER	NOTES	CONDITIONS	ML2264XCX			ML2264XIX, ML2264XMX			UNITS
			MIN	TYP (NOTE 4)	MAX	MIN	TYP (NOTE 4)	MAX	
Converter									
Total Unadjusted Error ML2264BXX ML2264CXX	5, 7	$V_{REF} = V_{CC}$			±1/2 ±1			±1/2 ±1	LSB LSB
Integral Linearity Error ML2264BXX ML2264CXX	5, 7	$V_{REF} = V_{CC}$			±1/2 ±1			±1/2 ±1	LSB LSB
Differential Linearity Error ML2264BXX ML2264CXX	5	$V_{REF} = V_{CC}$			±1/2 ±1			±1/2 ±1	LSB LSB
Full Scale Error ML2264BXX ML2264CXX	5				±1/2 ±1			±1/2 ±1	LSB LSB
Zero Scale Error ML2264BXX ML2264CXX	5				±1/2 ±1			±1/2 ±1	LSB LSB
Channel to Channel Mismatch	5				±1/4			±1/4	LSB
$+V_{REF}$ Voltage Range	6		$-V_{REF}$		$V_{CC}+0.1$	$-V_{REF}$		$V_{CC}+0.1$	V
$-V_{REF}$ Voltage Range	6		GND–0.1		$+V_{REF}$	GND–0.1		$+V_{REF}$	V
Reference Input Resistance	5		1	2.5	4	1	2.5	4	kΩ
Analog Input Range	5, 8		GND–0.1		$V_{CC}+0.1$	GND–0.1		$V_{CC}+0.1$	V
Power Supply Sensitivity	5	DC V_{CC} =5V ± 5%, V_{REF} = 4.50V		±1/32	±1/4		±1/32	±1/4	LSB
		100mVp-p 100kHz sine on V_{CC}, V_{IN} = 0		±1/16			±1/16		LSB
Analog Input Leakage Current, OFF Channel	5	ON Channel = V_{CC} OFF Channel = 0V	–1			–1			µA
		ON Channel = 0V OFF Channel = V_{CC}			1			1	µA
Analog Input Leakage Current, ON Channel	5	ON Channel = 0V OFF Channel = V_{CC}	–1			–1			µA
		ON Channel = V_{CC} OFF Channel = 0V			1			1	µA
Analog Input Capacitance		During Acquisition Period		45			45		pF
Digital and DC									
$V_{IN(1)}$, Logical "1" Input Voltage	5	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0, A1	2.0			2.0			V
		MODE, SH/$\overline{TH}$	V_{CC}–0.5			V_{CC}–0.5			V
$V_{IN(0)}$, Logical "0" Input Voltage	5	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0, A1			0.8			0.8	V
		MODE, SH/$\overline{TH}$			0.5			0.5	V

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, and $-V_{REF} = GND$, and timing measured at 1.4V, $C_L = 100pF$.

PARAMETER	NOTES	CONDITIONS		ML2264XCX MIN	ML2264XCX TYP (NOTE 4)	ML2264XCX MAX	ML2264XIX, ML2264XMX MIN	ML2264XIX, ML2264XMX TYP (NOTE 4)	ML2264XIX, ML2264XMX MAX	UNITS
Digital and DC (Continued)										
$I_{IN(1)}$, Logical "1" Input Current	5	$V_{IH} = V_{CC}$	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0, A1			1			1	µA
			MODE, SH/$\overline{TH}$	15	50	150	15	50	150	µA
$I_{IN(0)}$, Logical "0" Input Current	5	$V_{IL} = GND$	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$	–1			–1			µA
			MODE, SH/$\overline{TH}$	–20			–20			µA
$V_{OUT(1)}$, Logical "1" Output Voltage	5	$I_{OUT} = -2mA$		4.0			4.0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	5	$I_{OUT} = 2mA$				0.4			0.4	V
I_{OUT}, Three-State Output Current	5	$V_{OUT} = 0V$		–1			–1			µA
		$V_{OUT} = V_{CC}$				1			1	µA
C_{OUT}, Logic Output Capacitance					5			5		pF
C_{IN}, Logic Input Capacitance					5			5		pF
I_{CC}, Supply Current	5	$\overline{CS} = \overline{WR} = \overline{RD} = $ "1" No Output Load				18			20	mA
AC and Dynamic Performance (Note 9)										
t_{CRD}, Conversion Time, Read Mode	5	$\overline{RD}$ to $\overline{INT}$, MODE = 0V				1020			1100	ns
t_{CWR-RD}, Conversion Time, Write-Read Mode	5, 9	$\overline{WR}$ Falling Edge to $\overline{INT}$, $t_{RD} < t_{INT}$, MODE = V_{CC}	SH/$\overline{TH}$ = V_{CC}			700			775	ns
			SH/$\overline{TH}$ = GND			830			930	ns
SNR, Signal to Noise Ratio		V_{IN} = 5V, 250kHz Noise is sum of all nonfundamental components from 0–500kHz. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1.0 MHz			48			48		dB
HD, Harmonic Distortion		V_{IN} = 5V, 250kHz THD is sum of 2–5th harmonics relative to fundamental. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1.0 MHz			–63			–63		dB
IMD, Intermodulation Distortion		fa = 2.5V, 250kHz fb = 2.5V, 248kHz IMB is (fa + fb), (fa – fb), (2fa + fb), (2fa – fb), (fa + 2fb), or (fa – 2fb) relative to fundamental. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1.0 MHz			–60			–60		dB

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, and $-V_{REF} = GND$, and timing measured at 1.4V, $C_L = 100pF$.

PARAMETER	NOTES	CONDITIONS	ML2264XCX			ML2264XIX, ML2264XMX			UNITS
			MIN	TYP (NOTE 4)	MAX	MIN	TYP (NOTE 4)	MAX	
AC and Dynamic Performance (Note 9) (Continued)									
FR, Frequency Response		V_{IN} = 5V, 0–250kHz Relative to 1kHz $SH/\overline{TH} = V_{CC}$, MODE = V_{CC} $f_{SAMPLING}$ = 1.0 MHz		±0.1			±0.1		dB
SR, Slew Rate Tracking	6	$SH/\overline{TH} = V_{CC}$			4.0			4.0	V/µs
		$SH/\overline{TH}$ = GND			0.25			0.25	V/µs
t_{AS}, Multiplexer Address Setup Time	5	$SH/\overline{TH}$ = GND, Figure 1 (Track & Hold Operation)	0			0			ns
t_{AH}, Multiplexer Address Hold Time	5	$SH/\overline{TH}$ = GND, Figure 1 (Track & Hold Operation)	60			70			ns
t_{AS}, Multiplexer Address Setup Time	5	$SH/\overline{TH} = V_{CC}$, Figure 2 (Sample & Hold Operation)	225			245			ns
t_{AH}, Multiplexer Address Hold Time	5	$SH/\overline{TH} = V_{CC}$, Figure 2 (Sample & Hold Operation)	60			70			ns
AC Performance Read Mode (Pin 5 = 0V), Figure 4									
t_{RDY}, $\overline{CS}$ to RDY Delay	5		0		60	0		65	ns
t_{RDD}, $\overline{RD}$ Low to RDY Delay	5, 10	Figure 3			1020			1100	ns
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	5		0			0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	5		0			0			ns
t_{CRD}, Conversion Time — $\overline{RD}$ Low to $\overline{INT}$ low	5, 10				1020			1100	ns
t_{ACC0}, Data Access Time $\overline{RD}$ to Data Valid	5		t_{CRD}–10		t_{CRD}+20	t_{CRD}–10		t_{CRD}+20	ns
t_{RDPW}, $\overline{RD}$ Pulse Width	5		t_{CRD}+30			t_{CRD}+30			ns
t_{INTH}, $\overline{RD}$ to $\overline{INT}$ Delay	5, 10		0		65	0		75	ns
t_{DH}, Data Hold Time — $\overline{RD}$ Rising Edge to Data High Impedance State	6, 10	Figure 3	0		50	0		60	ns
t_P, Delay Time Between Conversions — $\overline{INT}$ Low to $\overline{RD}$ Low	5, 10	Sample & Hold Mode, $SH/\overline{TH} = V_{CC}$	300			325			ns
		Track & Hold Mode, $SH/\overline{TH}$ = GND	240			260			ns
AC Performance Write-Read Mode (Pin 5 = 5V), Figures 5 and 6									
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	5		0			0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	5		0			0			ns
t_{WR}, $\overline{WR}$ Pulse Width	5	$SH/\overline{TH} = V_{CC}$	190		50K	205		50K	ns
	6	$SH/\overline{TH}$ = GND	320		50K	360		50K	ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, and $-V_{REF} = GND$, and timing measured at 1.4V, $C_L = 100pF$.

PARAMETER	NOTES	CONDITIONS	ML2264XCX			ML2264XIX, ML2264XMX			UNITS
			MIN	TYP (NOTE 4)	MAX	MIN	TYP (NOTE 4)	MAX	
AC Performance Write-Read Mode (Pin 5 = 5V) Figures 5 and 6 (Continued)									
t_{RD}, Read Time — $\overline{WR}$ High to $\overline{RD}$ Low Delay	5	$t_{RD} < t_{INTL}$	275			300			ns
t_{RI}, $\overline{RD}$ to $\overline{INT}$ Delay	5, 10	$t_{RD} < t_{INTL}$	0		235	0		270	ns
t_{ACC1}, Data Access Time — $\overline{RD}$ Low to Data Valid	5	$t_{RD} < t_{INTL}$	0		240	0		300	ns
t_{CWR-RD}, Conversion Time — $\overline{WR}$ Falling Edge to $\overline{INT}$ Low	5, 9, 10	$t_{RD} < t_{INTL}$, SH/$\overline{TH}$ = V_{CC}			700			775	ns
	6, 9, 10	$t_{RD} < t_{INTL}$, SH/$\overline{TH}$ = GND			830			930	ns
t_{INTL}, Internal Comparison Time — $\overline{WR}$ Rising Edge to $\overline{INT}$ Low	5, 10	$t_{RD} > t_{INTL}$			620			670	ns
t_{ACC2}, Data Access Time — $\overline{RD}$ to Data Valid	5	$t_{RD} > t_{INTL}$	0		50	0		60	ns
t_{DH}, Data Hold Time — $\overline{RD}$ Rising Edge to Data High Impedance State	6, 10	Figure 3	0		50	0		60	ns
t_{INTH}, $\overline{RD}\uparrow$ to $\overline{INT}\uparrow$ Delay	5, 10		0		65	0		75	ns
t_P, Delay Time Between Conversions — $\overline{INT}$ Low to $\overline{WR}$ Low	5, 10	Sample & Hold Mode, SH/$\overline{TH}$ = V_{CC}	300			325			ns
		Track & Hold Mode, SH/$\overline{TH}$ = GND	240			260			ns
t_{IHWR}, $\overline{WR}\uparrow$ to $\overline{INT}\uparrow$ Delay	5, 10	Standalone Mode	0		90	0		100	ns
t_{ID}, $\overline{INT}\downarrow$ to Data Valid Delay	5, 10	Standalone Mode	0		20	0		30	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired All voltages unless otherwise specified are measured with respect to ground.

Note 2: When the voltage at any pin exceeds the power supply rails ($V_{IN} < GND$ or $V_{IN} > V_{CC}$) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: –55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-cast test conditions. 0°C to +70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

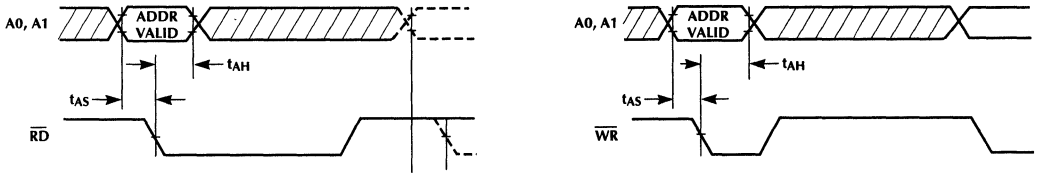
Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Total unadjusted error includes offset, full scale, linearity, sample and hold, and multiplexer errors. Total unadjusted error is tested at the minimum specified times for $\overline{WR}$, $\overline{RD}$, t_{R1}, and t_P. For example, for the ML2264XCX in the sample and hold mode, $\overline{WR}/\overline{RD}$ mode t_{WR} = 190ns, t_{RD} = 275ns with a frequency of 1.000MHz (cycle time of 1000ns).

Note 8: For $-V_{REF} \geq V_{IN}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to the analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct — especially at elevated temperatures, and cause errors for analog inputs near full scale The spec allows 100mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of $4.900V_{DC}$ over temperature variations, initial tolerance and loading

Note 9: Conversion time, write-read mode = $t_{WR} + t_{RD} + t_{RI}$.

Note 10: Defined from the time an output crosses 0.8V or 2 4V



a) RD Mode (Pin 5 = GND)

b) WR-RD Mode (Pin 5 = V_{CC})

Figure 1. Analog Multiplexer Address Timing for Track & Hold Mode (Pin 23 = GND)

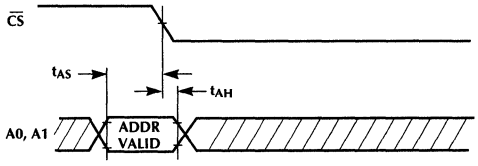


Figure 2. Analog Multiplexer Address Timing for Sample & Hold Mode (Pin 23 = V_{CC})

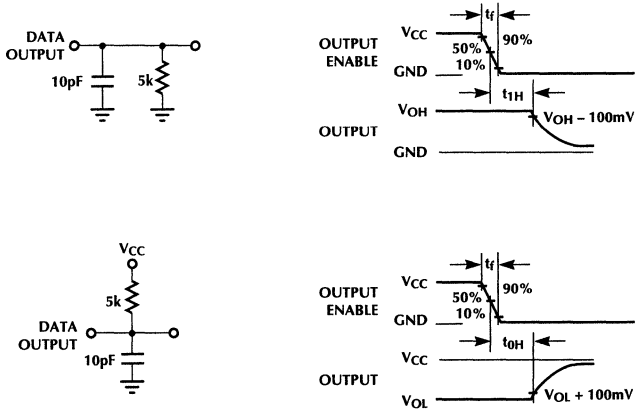
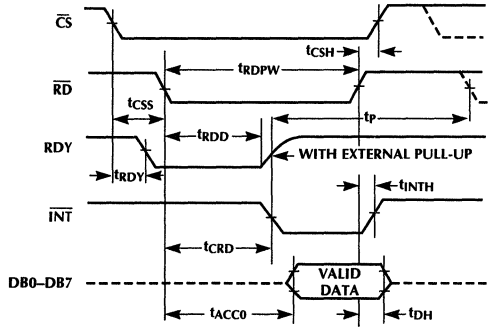


Figure 3. High Impedance Test Circuits and Waveforms



*In SAMPLE & HOLD mode a pull up resistor on RDY should not be used unless CS↓ is ≥ 20ns before RD↓.

Figure 4. RD Mode Timing

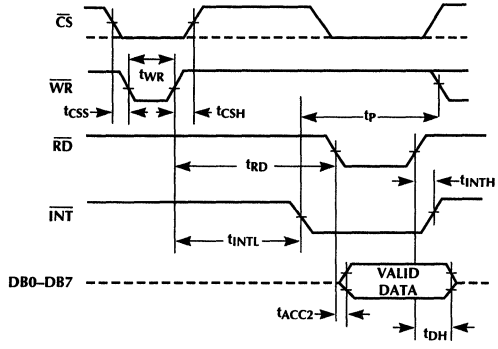


Figure 5. WR-RD Mode Timing ($t_{RD} > t_{INTL}$)

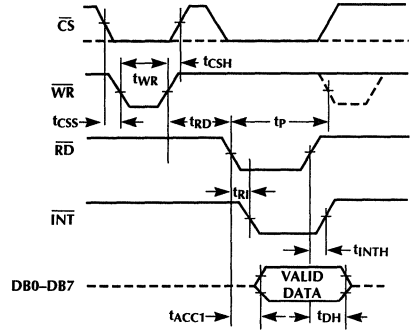


Figure 6. WR-RD Mode Timing ($t_{RD} < t_{INTL}$)

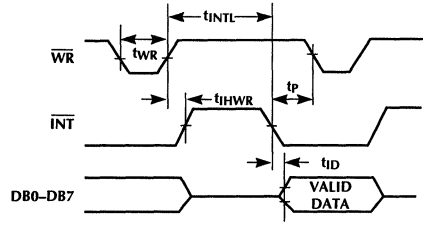


Figure 7. WR-RD Mode Stand-Alone Timing $\overline{CS} = \overline{RD} = 0$

1.0 FUNCTIONAL DESCRIPTION

The ML2264 uses a two stage flash technique for A/D conversion. This technique first performs a 4 bit flash conversion on V_{IN} to determine the 4 MSB's. These 4 MSB's are then cycled through an internal DAC to recreate the analog input. This reconstructed analog input signal from the DAC is then subtracted from the input, and the difference voltage is converted by a second 4 bit flash conversion, providing the 4 LSB's of the output data word.

1.1 MULTIPLEXER ADDRESSING

The ML2264 contains a 4-channel single ended analog multiplexer. A particular input channel is selected by using the address inputs A0 and A1. The relationship between the address inputs, A0 and A1, and the analog input selected is shown in Table 1.

Selected Analog Channel	Address Input	
	A0	A1
A IN 1	0	0
A IN 2	1	0
A IN 3	0	1
A IN 4	1	1

Table 1. Multiplexer Address Decoding

The address inputs are latched into the ML2264 on the falling edge of the $\overline{RD}$, $\overline{WR}$, or $\overline{CS}$ depending on the state of pins SH/$\overline{TH}$ and mode as shown in Table 2.

Address Latching Signal	Mode	Operation Mode
$\overline{RD}\downarrow$	GND	GND
$\overline{WR}\downarrow$	V_{CC}	GND
$\overline{CS}\downarrow$	GND	V_{CC}
$\overline{CS}\downarrow$	V_{CC}	V_{CC}

Table 2.

In the Sample & Hold mode of operation $\overline{CS}$ is used as the address latch enable, allowing for continuous conversions without addressing a given analog input for each conversion.

The Track & Hold mode of operation requires an analog input to be addressed and latched for each conversion that the ML2264 performs.

1.2 ANALOG INPUTS

The analog input on the ML2264 behaves differently than inputs on conventional converters. The analog input current requirements change while the conversion is in progress, and the amount of input current depends on what cycle the converter is in.

The equivalent input circuit for the converter is shown in Figure 8. When the conversion starts in the T/H mode ($\overline{WR}\downarrow$ in the WR-RD mode or $\overline{RD}\downarrow$ in the RD mode) S1, S4 and S6 close and S3 opens. This period is known as the acquisition period where the MSB flash converter tracks the input signal and the LSB flash converter samples it. During this period, V_{IN} is connected to the 16 MSB and 15 LSB comparators. Thus 38pF of input capacitance must be charged up through the combined R_{ON} resistance of the internal analog switches plus any external source resistance, R_S. In addition, there is a stray capacitance of approximately 11pF that needs to be charged through the external source resistance R_S. This period ends in the WR-RD mode when $\overline{WR}\uparrow$ or by an internal timer in the RD mode. At this point S1 and S4 open and the analog input at V_{IN} is no longer being sampled; thus during this time the analog voltage on V_{IN} does not affect converter performance.

As shown above, the critical period for charging up the analog input occurs when the MSB and LSB comparators are sampling the input, known as the acquisition period. The source of the external signal on V_{IN} must adequately charge up the analog voltage during the acquisition period. To do this, the input must settle within the required analog accuracy tolerance at least 50ns before the end of the acquisition period so that the MSB comparators have adequate time to make the correct decision. If more time is needed due to finite charging or settling time of the external source, the $\overline{WR}$ low period can be extended in WR-RD mode. In RD mode, since the acquisition time is fixed by internal delays, the burden is on the external source to charge up and settle the input adequately.

When the ML2264 operates in the S/H mode (pin 23 = V_{CC}) both the MSB and the LSB flash converter perform a true sample and hold operation during the acquisition or sampling period. This period starts after the falling edge of $\overline{INT}$ and ends with the falling edge of $\overline{WR}$ in the WR-RD mode or the falling edge of $\overline{RD}$ in the RD mode. The duration of this period is user controlled and must satisfy a minimum of t_P.

During this period S1, S3, S4 and S6 close, therefore 46pF of input capacitance must be charged up in addition to the 11pF of stray capacitance.

1.3 TRACK AND HOLD vs. SAMPLE AND HOLD

The MSB Flash Converter of the ML2264 in T/H mode has a track and hold mechanism for sampling the input. The input is attached to the MSB comparators directly in the MSB compare cycle, or acquisition period. When the MSB compare cycle ends, the state of the MSB comparators is latched. The LSB Flash Converter always performs a S/H operation. Thus, the analog input signal can be changing during the MSB compare cycle, or acquisition period, and

the MSB comparators will be tracking it as long as the slew rate of the analog input is slow enough so that the MSB comparators can respond. The ML2264 can track and hold signals with slew rates as high as 0.25V/µs (16kHz @ 5 volts) without sacrificing conversion accuracy.

The ML2264 in S/H mode does not have the slew rate limitation of the T/H mode since an internal sample and hold acquires the analog signal, holds it internally, and then performs a conversion. Since this is a true sample and hold function, the S/H mode can theoretically digitize signals of frequencies much higher than the T/H mode. The ML2264 in S/H mode can digitize signals of frequencies as high as 250kHz @ 5V (slew rates as high as 4V/µs) without sacrificing conversion accuracy. In most applications, the S/H mode is more desirable than T/H mode because of the better dynamic performance.

1.3.1 Converter — T/H Mode

The operating sequence for the WR-RD mode is illustrated in Figure 9a. Initially, the internal comparators are auto-zeroed while $\overline{WR}$ is high. A conversion is initiated by the falling edge of $\overline{WR}$. While $\overline{WR}$ is low, the MSB comparators are tracking the analog input and comparing this voltage against voltages from the internal resistor ladder. At the same time, the input is being acquired or sampled by LSB comparators. On the rising edge of $\overline{WR}$, the MSB comparator results are latched, and the LSB acquisition time is ended by closing the sampling switch to the LSB comparators. While $\overline{WR}$ is high, the LSB comparators then compare the residual input voltage against internal voltages from the resistor ladder to determine the 4 LSB's. When the LSB comparison or conversion is complete, $\overline{INT}$ goes low and latches the conversion result into the output latches. Then, the comparators are auto-zeroed while $\overline{WR}$ is high before another conversion can start.

The operating sequence for RD mode, is similar to that described above for the WR-RD mode, except the conversion is initiated by the falling edge of $\overline{RD}$, and the MSB and LSB conversions are generated by internal clock edges that are generated while $\overline{RD}$ is low.

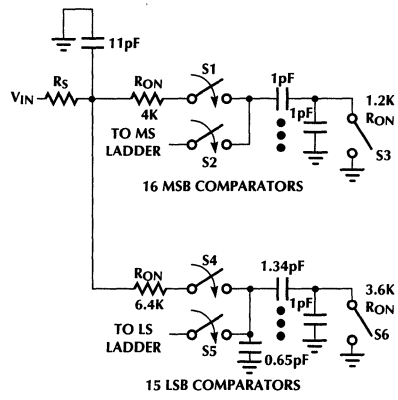


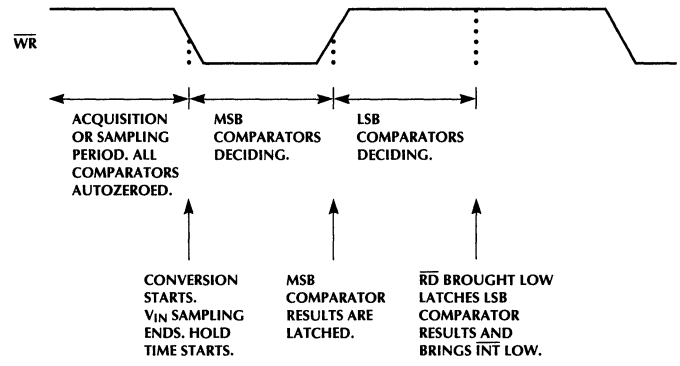
Figure 8. Converter Equivalent Input Circuit

1.3.2 Converter — S/H Mode

The operating sequence for S/H mode is illustrated in Figure 9b. Notice that it is similar to T/H mode described above except this mode has a true sample and hold function. The falling edge of $\overline{INT}$ closes the sampling switch and starts the acquisition period where the analog input is sampled at the same time all comparators are auto-zeroed. The falling edge of $\overline{WR}$ opens the internal sampling switch, ends the acquisition period, and starts the conversion on the internally sample and held signal. The MSB comparators make their decisions while $\overline{WR}$ is low. On the rising edge of $\overline{WR}$, the MSB comparator results are latched. The LSB comparators make their decision when $\overline{WR}$ is high. When the LSB comparison or conversion is complete, $\overline{INT}$ goes low and latches the conversion result into the output buffers. Then, the acquisition period begins again and the converter is ready for the next conversion.

The operating sequence for the RD mode is the same as the WR-RD mode, except the conversion is initiated by the falling edge of $\overline{RD}$, and the MSB and LSB conversions are generated by internal clock edges that are generated while $\overline{RD}$ is low.

(a) T/H Mode



(a) S/H Mode

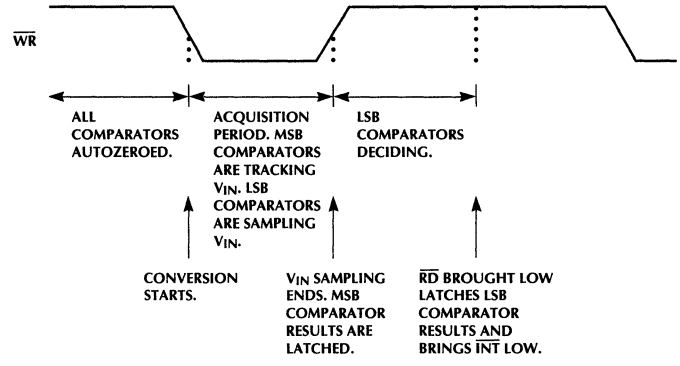


Figure 9. Operating Sequence (WR-RD Mode)

1.4 REFERENCE

The $+V_{REF}$ and $-V_{REF}$ inputs are the reference voltages that determine the full scale and zero input voltages, respectively, for the A/D converter. Thus, $+V_{REF}$ defines the analog input which produces a full scale output and $-V_{REF}$ defines the analog input which produces an output code of all zeroes. The transfer function for the A/D converter is shown in Figure 10.

$+V_{REF}$ and $-V_{REF}$ can be set to any voltage between GND and V_{CC}. This means that the reference voltages can be offset from GND and the difference between $+V_{REF}$+ and $-V_{REF}$– can be made small to increase the resolution of the conversion. Note that the total unadjusted error increases when $[+V_{REF} - (-V_{REF})]$ decreases.

1.5 POWER SUPPLY AND REFERENCE DECOUPLING

A 0.1µF ceramic disc capacitor is recommended to bypass V_{CC} to GND, using as short a lead length as possible.

If REF+ and REF– inputs are driven by long lines, they should be bypassed by 0.1µF ceramic disc capacitors at the reference input pins.

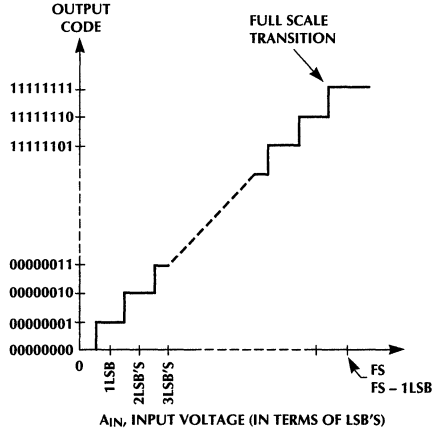


Figure 10. A/D Transfer Characteristic

1.6 DYNAMIC PERFORMANCE

1.6.1 Sinusoidal Inputs

Since the ML2264 has an internal sample and hold, the device can digitize high frequency sinusoids with little or no signal degradations. Using the Nyquist criteria, the highest frequency input to the converter could theoretically be 1/2 the sampling rate (f_S). Any frequency components above $f_S/2$ will be aliased below $f_S/2$. In most applications, these aliased components cause unacceptable distortion and must be filtered out of the input. If the input frequency is too close to $f_S/2$, then the requirements on the anti-alias filter become difficult to impossible to realize with standard component and tolerances. In most practical applications, the highest input frequency has to be limited to 1/3 to 1/4 of f_{MAX} in order to relax the filtering requirements enough to make a realizable anti-alias filter.

The maximum sampling rate (f_{max}) for the ML2264 in the WR-RD mode, ($t_{RD} < t_{INTL}$) can be calculated as follows:

$$f_{max} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_P}$$

$$f_{max} = \frac{1}{190ns + 275ns + 235ns + 300ns}$$

f_{max} = 1.000 MHz

t_{WR} = Write Pulse Width

t_{RD} = Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses

t_{RI} = $\overline{RD}$ to $\overline{INT}$ Delay

t_P = Delay Time between Conversions

This permits a maximum sampling rate of 1MHz for the ML2264. The dynamic performance specifications (SNR, HD, IMD, and FR) for the ML2264 are all specified at 250kHz, which is approximately 1/4 of the sampling rate, f_S.

In applications where aliased frequency components are acceptable and filtering of the input signal is not needed, or where a filter with a steep amplitude response is available, the user can apply an input sinusoid higher than 250kHz to the device. Note, however, that as the input frequency increases above 500kHz, dynamic performance degradation will occur due to the finite bandwidth of the internal sample and hold.

The Figure 11 plots are 4096 point FFT's of the ML2264 converting a 257kHz and a 491kHz, 0 to 4.5V, low distortion sine wave input. The ML2264 samples and digitizes at its specified accuracy, dynamic input signals with frequency components up to the Nyquist frequency (one-half the sampling rate). The output spectra yields precise measure-ments of the input signal level, harmonic components, and signal to noise ratio up to the 8-bit level. The near ideal signal to noise ratio is maintained independent of increasing analog input frequencies to 500kHz.

1.6.2 Signal-To-Noise Ratio

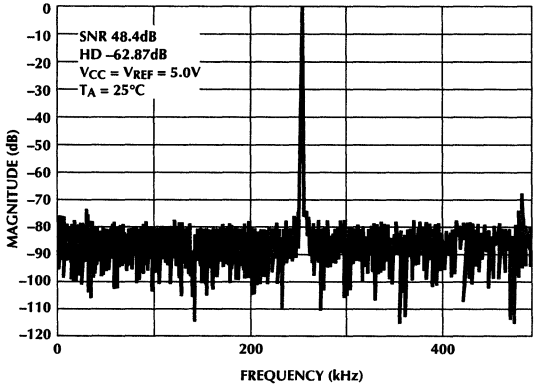
Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more the levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\ dB$$

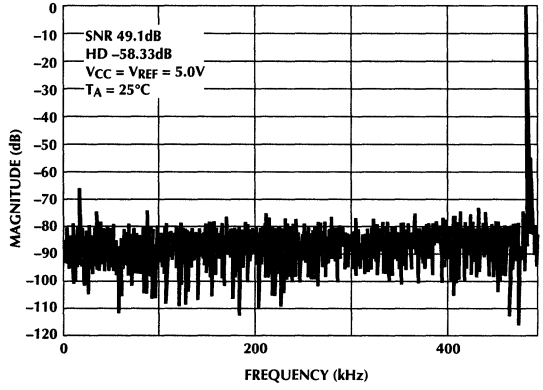
where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92 dB.

1.6.3 HARMONIC DISTORTION

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2264 is defined as



a) Output Spectrum with f_{IN} = 257kHz, f_S = 1MHz



b) Output Spectrum with f_{IN} = 491kHz, f_S = 1MHz

Figure 11. Dynamic Performance, Sample and Hold Mode

$$20\log = \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

1.6.2 Signal-To-Noise Ratio

Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more the levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

SNR = (6.02N + 1.76) dB

where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92 dB.

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where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

1.6.4 Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of $mf_A + nf_B$, where m, n = 0, 1, 2, 3 ... Intermodulation terms are those for which m or n is not equal to zero. The (IMD) intermodulation distortion specification includes the second order terms ($f_A + f_B$) and $f_A - f_B$) and the third order terms ($2f_A + f_B$), ($2f_A - f_B$), ($f_A + 2f_B$), and ($f_A - 2f_B$) only.

1.7 DIGITAL INTERFACE

The ML2264 has two basic interface modes, RD and WR-RD, which are selected by the MODE input pin.

1.7.1 RD Mode

In the RD mode, $\overline{WR}$/RDY pin is configured as the RDY output. The read mode performs a conversion with a single $\overline{RD}$ pulse. This allows the µP to start a conversion, wait, and then read data with a single read instruction.

The timing for the RD mode is shown in Figure 4. To do a conversion, $\overline{CS}$ must be low to select the device. After $\overline{CS}$ goes low, the RDY output goes low indicating that the device is ready to do a conversion. The conversion starts on the falling edge of $\overline{RD}$. While $\overline{RD}$ is low, the MSB and LSB decisions are made with internally generated clock edges. When the conversion is complete, RDY goes high and $\overline{INT}$ goes low signaling the end of the conversion. After $\overline{INT}$ goes low, the data outputs go from high impedance to active state with valid output data. Data stays valid until either $\overline{RD}$ or $\overline{CS}$ goes high. When either signal goes high, the output data lines return to the high impedance state and $\overline{INT}$ returns high.

1.7.2 WR-RD Mode

In the WR-RD mode, the $\overline{WR}$/RDY pin is configured as the $\overline{WR}$ input. In this mode, $\overline{WR}$ initiates the conversion and $\overline{RD}$ controls reading the output data. This can be done in several ways, described below.

1.7.3 WR-RD Mode — Using Internal Delay ($t_{RD} > t_{INTL}$)

The timing is shown in Figure 5. To do a conversion, $\overline{CS}$ must be low to select the device. Then, $\overline{WR}$ falling edge triggers the conversion. While $\overline{WR}$ is low, the MSB comparison is made. When $\overline{WR}$ returns high the LSB decision is made. After some internal delay, $\overline{INT}$ goes low indicating end of conversion. Valid data will appear on DB0–7 when $\overline{RD}$ is pulled low. $\overline{INT}$ is then reset by the rising edge of either $\overline{CS}$ or $\overline{RD}$.

1.7.4 WR-RD Mode — Reading Before Delay ($t_{RD} < t_{INTL}$)

The internally generated delay for the LSB decision when $t_{RD} > t_{INTL}$ is longer than necessary due to circuit design tolerances of t_{INTL} delay. If desired, a faster conversion will result without loss of accuracy by bringing $\overline{RD}$ low within the minimum time specified for t_{RD}. The timing diagram for this mode is shown in Figure 6. $\overline{WR}$ is the same as when $t_{RD} > t_{INTL}$. But in this case, $\overline{RD}$ is brought low t_{RD} ns after WR rising edge and before $\overline{INT}$. $\overline{INT}$ goes low indicating an end of conversion after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. When $\overline{RD}$ is brought low before $\overline{INT}$ goes low the data bus always remains in the high-impedance state until $\overline{INT}\downarrow$.

1.7.5 WR-RD Mode — Stand Alone Operation

Stand alone operation can be implemented by tying $\overline{CS}$ and $\overline{RD}$ low as shown in Figure 7. $\overline{WR}$ initiates a conversion as before. When $\overline{WR}$ is low, the MSB comparison is made. When, $\overline{WR}$ goes high, the LSB comparison is made. Since $\overline{RD}$ is already low, the output data will appear automatically at end of conversion. Since $\overline{RD}$ is always low, $\overline{INT}$ is reset on rising edge of $\overline{WR}$ and goes low at end of conversion.

1.7.6 Power-On Reset

When power is first applied, an internal power-on reset and timer circuit inhibits the $\overline{CS}$ input and resets the internal circuitry to prevent the ML2264 from starting in an unknown state. During this period of approximately 3µs, $\overline{INT}$ remains high and the data bus is in the high-impedance state.

2.0 TYPICAL APPLICATIONS

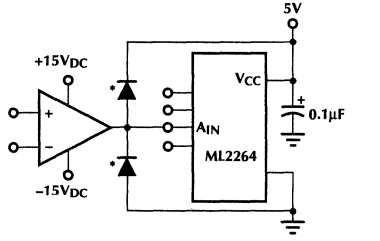


Figure 12. Protecting the Input

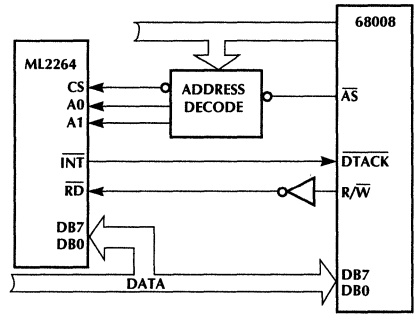


Figure 15. 68000 Type Interface to ML2264

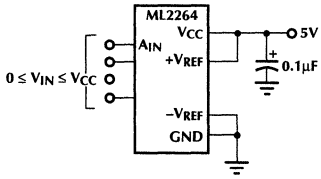


Figure 13. Using V_{CC} as Reference for Ratiometric Operation

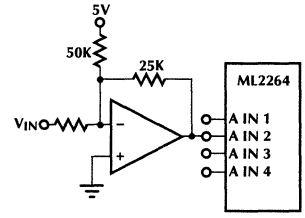


Figure 16. ±2.5V Analog Input Range

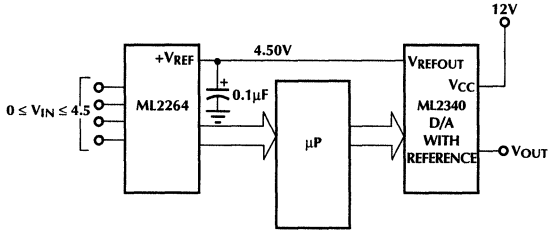


Figure 14. Using External Reference of D/A

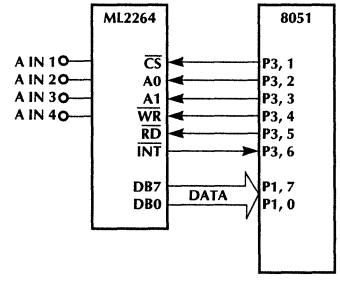


Figure 17. 8051 Interface to ML2264

2.0 TYPICAL APPLICATIONS (Continued)

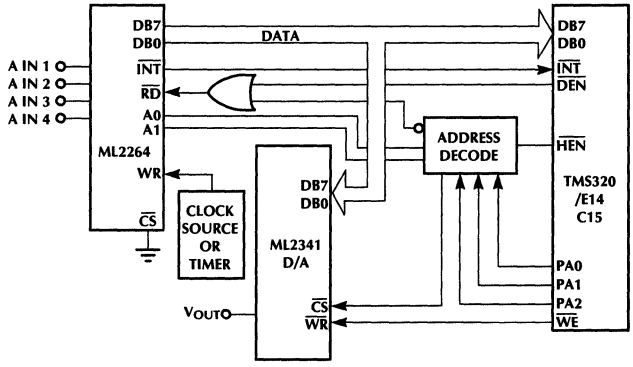


Figure 18. TMS320 Interface with D/A Output

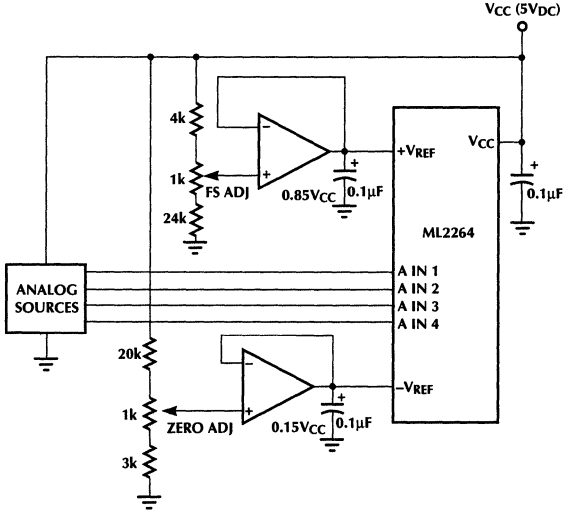


Figure 19. Operating with a Ratiometric Analog Signal of 15% of V_{CC} to 85% of V_{CC}

ORDERING INFORMATION

PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
ML2264BMJ	±1/2 LSB	–55°C to +125°C	Hermetic DIP (J24)
ML2264BIJ		–40°C to +85°C	Hermetic DIP (J24)
ML2264BCP		0°C to +70°C	Molded DIP (P24)
ML2264BCS		0°C to +70°C	Molded SOIC (S24)
ML2264CMJ	±1 LSB	–55°C to +125°C	Hermetic DIP (J24)
ML2264CIJ		–40°C to 85°C	Hermetic DIP (J24)
ML2264CCP		0°C to +70°C	Molded DIP (P24)
ML2264CCS		0°C to +70°C	Molded SOIC (S24)

ML2271

µP Compatible High-Speed 10-Bit A/D Converter with S/H

GENERAL DESCRIPTION

The ML2271 is a high speed, µP compatible 10-bit A/D converter. A three step flash technique is used to achieve a conversion time of 1.65µs. The ML2271 operates from a single 5V supply and has an analog input range from GND to V_{CC}.

The ML2271 has a true internal sample and hold and can digitize sinusoid signals as high as 150kHz without conversion errors.

The ML2271 digital interface has been designed so that the device appears as a memory location or I/O port to a µP, eliminating the need for external interfacing logic. The data outputs are latched and have three state control, allowing direct connection to a µP bus or I/O port. The addition of an internal timing generator also allows the device to easily operate in stand alone applications.

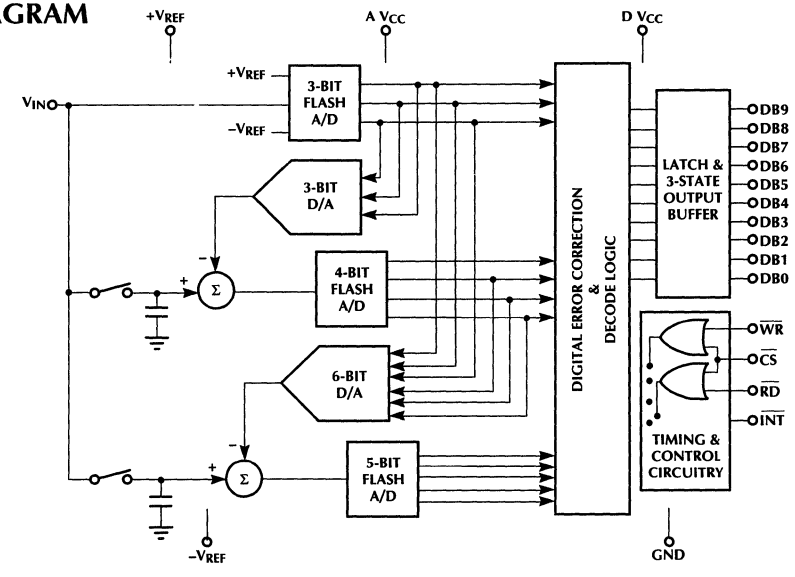
The ML2271 is pin and function compatible with the ADC1061.

FEATURES

- Conversion time over temperature and supply voltage tolerance 1.8µs
- Linearity error ±1LSB
- Full scale error ±1LSB
- Zero error ±1LSB
- Capable of digitizing a 5V, 150kHz sine wave
- No missing codes
- 0V to 5V analog input range with single 5V power supply
- Analog input protection — 25mA min
- Operates ratiometrically or with up to 5V voltage reference
- No external clock required
- Easy interface to µP, or operates stand-alone
- Latched, 3-state data outputs
- Power-on reset circuitry
- Low power — 175mW max
- Standard 20-pin DIP or surface mount SOIC
- 0°C to 70°C, –40°C to +85°C operating temperature range

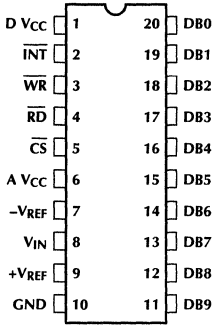
2

BLOCK DIAGRAM



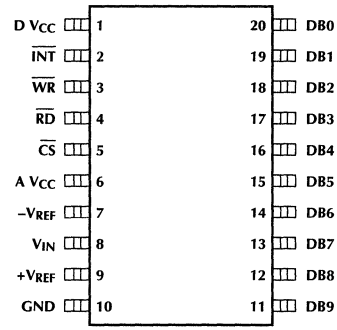
PIN CONFIGURATION

20-Pin DIP



TOP VIEW

20-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	D V_{CC}	Digital supply. +5V ±5%. Connect to A V_{CC}.
2	$\overline{INT}$	Interrupt output. This output signals the end of a conversion and indicates that data is valid on the data outputs. See Digital Interface section.
3	$\overline{WR}$	Write input. Input which initiates a conversion. See Digital Interface section.
4	$\overline{RD}$	Read input. This input latches data into the output latches. See Digital Interface section.
5	$\overline{CS}$	Chip select input. This input must be held low during $\overline{WR}$ and $\overline{RD}$ for the device to perform a conversion.
6	A V_{CC}	Analog supply. +5V ±5%. Connect to D V_{CC}.
7	$-V_{REF}$	Negative reference input voltage for A/D converter.
8	V_{IN}	Analog input.
9	$+V_{REF}$	Positive reference input voltage for A/D converter.
10	GND	Ground.
11	DB9	Data output — bit 9 (MSB)
12	DB8	Data output — bit 8
13	DB7	Data output — bit 7
14	DB6	Data output — bit 6
15	DB5	Data output — bit 5
16	DB4	Data output — bit 4
17	DB3	Data output — bit 3
18	DB2	Data output — bit 2
19	DB1	Data output — bit 1
20	DB0	Data output — bit 0 (LSB)

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage, A V_{CC}, D V_{CC} 6.5V
Voltage
  Logic Inputs ..... –0.3V to V_{CC} + 0.3V
  Analog Inputs ..... –0.3V to V_{CC} + 0.3
Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Package Dissipation
  at T_A = 25°C (Board Mount) 875mW
Lead Temperature (Soldering 10 sec.)
  Dual-In-Line Package (Molded) ..... 260°C
  Molded Small Outline IC Package
    Vapor Phase (60 sec.) ..... 215°C
    Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Temperature Range (Note 3) ..... $T_{MIN} \le T_A \le T_{MAX}$
  ML2271CCS ..... 0°C to +70°C
  ML2271CCP ..... 0°C to +70°C
  ML2271CIS ..... –40°C to +85°C
  ML2271CIP ..... –40°C to +85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, D V_{CC} = A V_{CC} = $+V_{REF}$ = 5V ±5%, and $-V_{REF}$ = GND

PARAMETER	CONDITIONS	ML2271CCX			ML2271CIX			UNITS
		MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
Converter								
Integral Linearity Error ML2271CXX	$V_{REF} = V_{CC}$ (Notes 5,7)			±1			±1.5	LSB
Differential Linearity Error ML2271CXX	$V_{REF} = V_{CC}$ (Note 5)			±1			±1	LSB
Full Scale Error ML2271CXX	(Note 5)			±1			±1	LSB
Zero Scale Error ML2271CXX	(Note 5)			±1			±1	LSB
Total Unadjusted Error ML2271CXX	(Note 5)			±1.5			±2.0	LSB
$+V_{REF}$ Voltage Range	(Note 6)	$-V_{REF}$		V_{CC}+0.1	$-V_{REF}$		V_{CC}+0.1	V
$-V_{REF}$ Voltage Range	(Note 6)	GND–0.1		$+V_{REF}$	GND–0.1		$+V_{REF}$	V
Reference Input Resistance	(Note 5)	0.9	1.3	1.7	0.9	1.3	1.7	kΩ
Analog Input Range	(Notes 5,8)	$-V_{REF}$		$+V_{REF}$	$-V_{REF}$		$+V_{REF}$	V
Power Supply Sensitivity	DC V_{CC} = 5V ± 5%, V_{REF} = 4.75V (Note 5)		±1/32	±1/4		±1/32	±1/4	LSB
	100mV_{P-P}, 100kHz sine on V_{CC}, V_{IN} = 0 (Note 5)		±1/16			±1/16		LSB
Analog Input Leakage Current	Converter Idle (Notes 5,9)	–2		+2	–2		+2	µA
Analog Input Capacitance	During Acquisition Period		25			25		pF

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, D $V_{CC} = A\ V_{CC} = +V_{REF} = 5V \pm 5\%$, and $-V_{REF} = GND$

PARAMETER	CONDITIONS	ML2271CCX			ML2271CIX			UNITS
		MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
Digital and DC								
$V_{IN(1)}$, Logical "1" Input Voltage	(Note 5)	2.0			2.0			V
$V_{IN(0)}$, Logical "0" Input Voltage	(Note 5)			0.8			0.8	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN} = V_{CC}$ (Note 5)			1			1	µA
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN} = 0V$ (Note 5)	–1			–1			µA
$V_{OUT(1)}$, Logical "1" Output Voltage	$I_{OUT} = -2mA$ (Note 5)	4.0			4.0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	$I_{OUT} = 2mA$ (Note 5)			0.4			0.4	V
I_{OUT}, Three-State	$V_{OUT} = 0V$ (Note 5)	–1			–1			µA
Output Current	$V_{OUT} = V_{CC}$ (Note 5)			1			1	µA
C_{OUT}, Logic Output Capacitance			5			5		pF
C_{IN}, Logic Input Capacitance			5			5		pF
I_{CC}, Supply Current, Analog Plus Digital	$\overline{CS} = \overline{WR} = \overline{RD} = 0$ No Output Load (Note 5)			32			35	mA
AC and Dynamic Performance (Note 9)								
t_{CONV}, Conversion Time, Interrupt Mode	Figure 2 t_{WR} = 250ns (Note 6)			1.65			1.8	µs
t_{CWRD}, Conversion Time, Write-Read Mode	Figure 3 (Note 5)			1.9			2.0	µs
t_{CRD}, Conversion Time, Write-Read Mode	Figure 4 (Note 6)			1.9			2.0	µs
SNR, Signal to Noise Ratio	V_{IN} = 5V, 150kHz Noise is sum of all nonfundamental components from 0–300kHz. $f_{SAMPLING}$ = 600kHz		60			60		dB
HD, Harmonic Distortion	V_{IN} = 5V, 150kHz THD is sum of 2–5th harmonics or aliases relative to fundamental. $f_{SAMPLING}$ = 600kHz		–60			–60		dB
IMD, Intermodulation Distortion	fa = 2.5V, 150kHz fb = 2.5V, 148kHz IMB is (fa + fb), (fa – fb), (2fa + fb), (2fa – fb), relative to fundamental. $f_{SAMPLING}$ = 600kHz		–60			–60		dB
FR, Frequency Response	V_{IN} = 5V, 0–150kHz Relative to 1kHz $f_{SAMPLING}$ = 600kHz		±0.1			±0.1		dB
SR, Slew Rate Tracking			2.36			2.36		V/µs

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, D V_{CC} = A V_{CC} = $+V_{REF}$ = 5V ±5%, and $-V_{REF}$ = GND

PARAMETER	CONDITIONS	ML2271CCX			ML2271CIX			UNITS
		MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
AC Performance, Figures 2, 3, 4, and 5								
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	(Note 5)	0			0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	(Note 5)	0			0			ns
t_{WR}, $\overline{WR}$ Pulse Width	(Note 5)	250		50K	250		50K	ns
t_{ACC2}, $\overline{WR}$ to Data Valid	(Note 5)			2.05			2.05	µs
t_{RD}, Read Pulse Width	(Note 5)	100			100			ns
t_{WRL}, $\overline{WR}\uparrow$ to $\overline{RD}\downarrow$	(Note 6)	0			0			ns
t_{INTH}, $\overline{RD}\uparrow$ to $\overline{INT}\uparrow$	(Note 5)	10		55	10		55	ns
t_{ACC1}, Data Access Time, $\overline{RD}\downarrow$ to Data Valid	(Note 5)	0		55	0		55	ns
t_{ID}, Data Access Time, $\overline{INT}\downarrow$ to Data Valid	(Note 5)	0		50	0		50	ns
t_{1H}, t_{0H}, $\overline{RD}\uparrow$ to Data High Impedance State	Figure 1 (Note 5)	10		50	10		60	ns
t_P, Delay From End of Conversion to Next Conversion	(Note 6)			20			20	ns
t_{IC}, $\overline{INT}\downarrow$ to Start of Next Conversion	(Note 5)	500			500			ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground

Note 2: When the voltage at any pin exceeds the power supply rails (V_{IN} < or GND or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: 0°C to +70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Total unadjusted error includes offset, full scale, linearity, and sample and hold errors.

Note 8: For $-V_{REF} \geq V_{IN}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to the analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct — especially at elevated temperatures, and cause errors for analog inputs near full scale The spec allows 100mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 100mV, the output code will be correct To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of 4 $900V_{DC}$ over temperature variations, initial tolerance and loading.

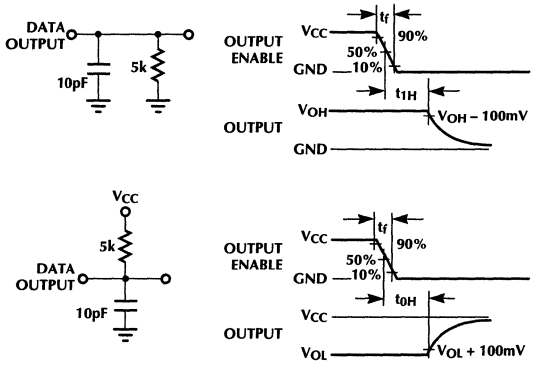


Figure 1. High Impedance Test Circuits and Waveforms

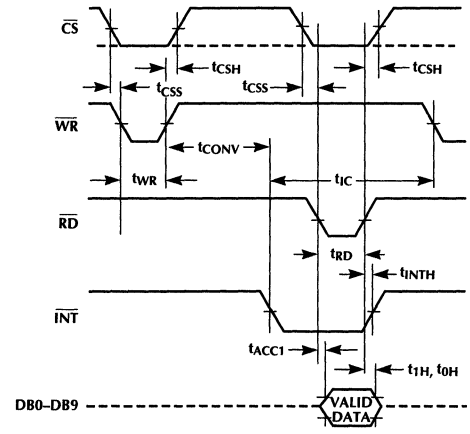


Figure 2. Interrupt Mode Timing

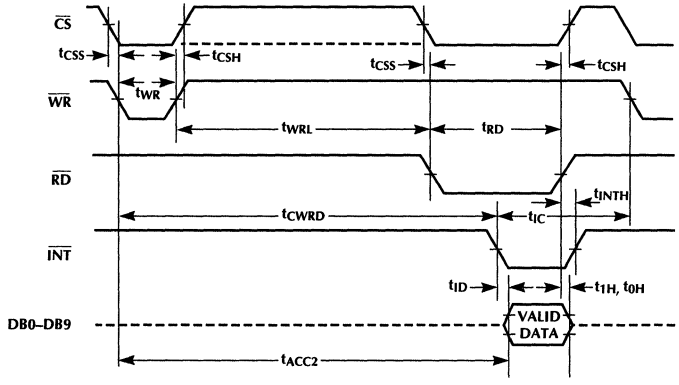


Figure 3. WR-RD Mode Timing

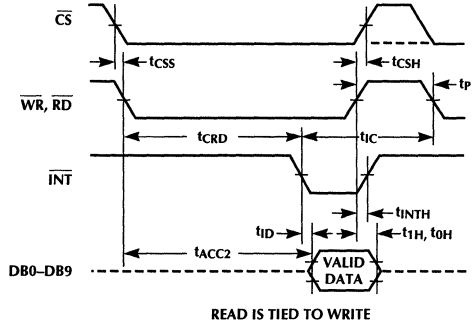


Figure 4. RD Mode Timing

1.0 FUNCTIONAL DESCRIPTION

The ML2271 uses a three step flash technique for A/D conversion. This technique first performs a 3 bit flash conversion on V_{IN} to determine the 3 most significant bits (MSB decision). These 3 MSB's are then cycled through an internal DAC to recreate the analog input. This reconstructed analog input signal from the DAC is then subtracted from the input, and the difference voltage is converted by a second 3 bit flash conversion providing the next 3 significant bits, called intermediate significant bits (ISB decision). This procedure is then performed again to provide the final 4 least significant bits (LSB decision).

The ML2271 has a true internal sample and hold. The internal operating sequence is shown in Figure 5. The falling edge of $\overline{WR}$ opens the S/H sampling switch, ends the acquisition time for the analog input, and starts the conversion on the internally sample and held signal. Then the MSB, ISB, and LSB decisions are made. $\overline{INT}$ goes low at end of conversion and $\overline{RD}$ controls the data outputs. This falling edge of $\overline{INT}$ also closes the sampling switch and starts the acquisition period for the next conversion.

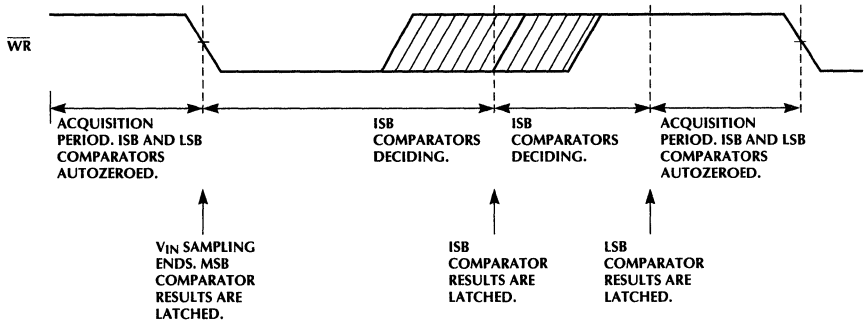


Figure 5. Operating Sequence

1.1 ANALOG INPUT

The analog input on the ML2271 behaves differently than inputs on conventional converters. The analog input current requirements change while the conversion is in progress, and the amount of input current depends on what cycle the converter is in.

The input circuit for the converter is shown in Figure 6A with the equivalent input circuit shown in Figure 6B. The acquisition period for the S/H starts on $\overline{INT}$ falling edge and ends on $\overline{WR}$ falling edge.

The critical period for charging up the analog input occurs during the acquisition period and the source of the external signal on V_{IN} must adequately charge up the analog voltage during this time. To do this, the input must settle within the required analog accuracy tolerance 100ns before the end of the acquisition period so that the sampling capacitors have adequate time to store the input signal. If more time is needed due to finite charging or settling time of the external source, the $\overline{WR}$ high period can be extended as long as is required.

1.2 SAMPLE AND HOLD

The ML2271 does not have the limitation of an equivalent circuit implemented with a track/hold. An internal sample and hold acquires the analog signal, holds it internally, and then a conversion is performed on the sample and held signal. Since this is a true sample and hold function, the ML2271 can sample and hold signals with frequencies as high as 150kHz @ 5V (slew rates as high as 2.36V/µs) without sacrificing conversion accuracy.

1.3 REFERENCE

The $+V_{REF}$ and $-V_{REF}$ inputs are the reference voltages that determine the full scale and zero input voltages, respectively, for the A/D converter. Thus, $+V_{REF}$ defines the analog input which produces a full scale output and $-V_{REF}$ defines the analog input which produces an output code of all zeroes. The transfer function for the A/D converter is shown in Figure 7.

$+V_{REF}$ and $-V_{REF}$ can be set to any voltage between GND and V_{CC}. This means that the reference voltages can be offset from GND and the difference between $+V_{REF}$ and $-V_{REF}$ can be made small to increase the resolution of the conversion. Note that the linearity error increases when $[+V_{REF} - (-V_{REF})]$ decreases.

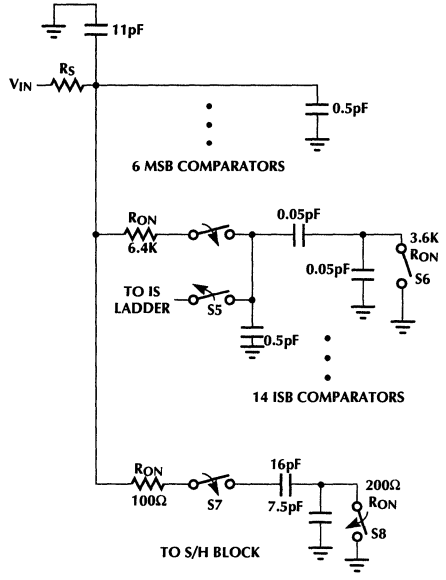


Figure 6A. Converter Input Circuit

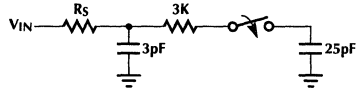


Figure 6B. Converter Equivalent Input Circuit

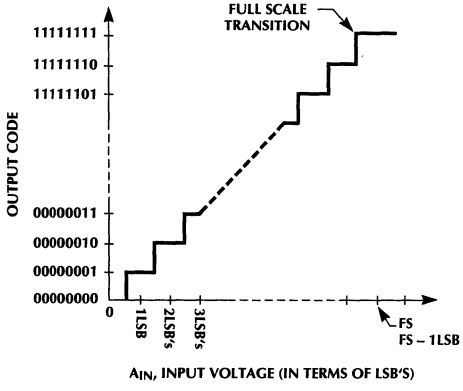


Figure 7. A/D Transfer Characteristic

1.4 POWER SUPPLY AND REFERENCE DECOUPLING

0.1µF in parallel with 0.01µF ceramic disc capacitors are recommended to bypass A V_{CC} to GND, as well as D V_{CC} to GND, using the shortest lead lengths possible.

If $+V_{REF}$ and $-V_{REF}$ inputs are driven by long lines, they should be bypassed by 0.1µF in parallel with 0.01µF ceramic disc capacitors at the reference input pins.

1.5 DYNAMIC PERFORMANCE

1.5.1 Sinusoidal Inputs

Since the ML2271 has an internal sample and hold, the device can digitize high frequency sinusoids with little or no signal degradations. Using the Nyquist criteria, the highest frequency input to the converter could theoretically by 1/2 the sampling rate (f_S). Any frequency components above $f_S/2$ will be aliased below $f_S/2$. In most applications, these aliased components cause unacceptable distortion and must be filtered out of the input. If the input frequency is too close to $f_S/2$, then the requirements on the antialias filter become difficult or impossible to realize with standard component and tolerances. In most practical applications, the highest input frequency has to be limited to 1/3 to 1/4 of f_S in order to relax the filtering requirements enough to make a realizable antialias filter.

The maximum sampling rate (f_{MAX}) for the ML2271 can be calculated as follows:

$$f_{MAX} = \frac{1}{t_{CONT} + t_P}$$

$$f_{MAX} = \frac{1}{1.45\mu s + 0.300\mu s}$$

f_{MAX} = 570kHz

t_{WR} = Write Pulse Width

t_{WRD} = Write to Data Delay

t_P = Delay Time Between Conversions

Note that the dynamic performance specifications (SNR, HD, IMD and FR) for the ML2271 are all specified at 150kHz, which is less than 1/3 of the sampling rate, f_S. This allows adequate margin between the input frequency and the aliased components to allow antialias filtering if needed.

In applications where aliased frequency components are acceptable and filtering of the input signal is not needed, the user can apply an input sinusoid higher than 150kHz to the device. Note, however, that as the input frequency increases above 150kHz, dynamic performance degradation will occur due to the finite bandwidth of the internal sample and hold.

1.5.2 Signal-to-Noise Ratio

Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling

frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more the levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus for ideal 10-bit converter, SNR = 61.96 dB.

1.5.3 Harmonic Distortion

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2271 is defined as

$$20\ \log = \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

1.5.4 Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of $mf_A + nf_B$, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. The (IMD) intermodulation distortion specification includes the second order terms ($f_A + f_B$) and ($f_A - f_B$) and the third order terms ($2f_A + f_B$), ($2f_A - f_B$), and ($f_A - 2f_B$) only.

1.6 DIGITAL INTERFACE

Depending on the way the external signals are applied to the ML2271, the timing of the conversion and resultant digital interface can be configured in three different modes.

While the operation for each mode is described below, there are some general rules that dictate the general relationships between $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{INT}$, and DB0–DB9. The falling edge of $\overline{WR}$ terminates the acquisition period and initiates a conversion. $\overline{INT}$ is forced low when a conversion is internally completed. $\overline{INT}$ is reset high by the $\overline{RD}$ rising edge. DB0–DB9 is in the high impedance state except when both $\overline{RD}$ and $\overline{INT}$ are low. $\overline{RD}$ low period does not affect the internal conversion but only determines when the digital signals DB0–DB9 are active; thus, $\overline{RD}$ can occur anytime. $\overline{CS}$ is used to select the device and needs to be low only while $\overline{WR}$ is low or when $\overline{RD}$ is low.

1.6.1 Interrupt Mode

Timing for the Interrupt Mode is shown in Figure 2. To do a conversion, $\overline{CS}$ must be low to select the device. $\overline{INT}$ falling edge starts the acquisition period. The falling edge of $\overline{WR}$ ends the acquisition period and the MSB comparison is made. Then, the (Intermediate Significant Bits) ISB and LSB decisions are made with internal timing signals. After the conversion is complete, $\overline{INT}$ goes low indicating end of conversion. When $\overline{RD}$ goes low, DB0–DB9 goes from high impedance to the active state with the digital result of the conversion. $\overline{INT}$ is rest high and DB0–DB9 is reset to high impedance on the rising edge of $\overline{RD}$.

Interrupt Operation is intended to be used in interrupt driven systems or applications where $\overline{INT}$ signals the transfer of data.

1.6.2 Write-Read Mode

Write-Read Operation is the same as Interrupt Operation except that $\overline{RD}$ is brought low before the internal conversion is completed (before $\overline{INT}$ goes low).

Timing for Write-Read Operation is shown in Figure 3. To perform a conversion, $\overline{CS}$ must be low to select the device. $\overline{INT}$ falling edge starts the acquisition period. The falling edge of $\overline{WR}$ ends the acquisition period and the MSB decision is made. Then, the ISB and LSB decisions are made by internal timing signals. In this mode, $\overline{RD}$ is brought low before the internal conversion is completed. When the internal conversion is completed, $\overline{INT}$ will be forced low and data will appear on DB0–DB9 as long as $\overline{RD}$ is still low. $\overline{INT}$ is reset high and DB0–DB9 is reset to high impedance on the rising edge of $\overline{RD}$.

Write-Read Operation is intended for applications where $\overline{RD}$ controls the transfer of data to a microprocessor.

1.6.3 Read Mode

Read Mode Operation is implemented by tying $\overline{RD}$ to $\overline{WR}$ and keeping $\overline{RD}$ and $\overline{WR}$ low long enough so that the conversion time is totally determined by the internal timing signals.

Timing for the Read Mode is shown in Figure 4. To do a conversion, $\overline{CS}$ must be low to select the device. The $\overline{RD}$ and $\overline{WR}$ falling edge starts the conversion. $\overline{RD}$ and $\overline{WR}$ is held low for the entire internal conversion. Thus, the MSB, ISB, and LSB comparisons along with the end of the acquisition period are made by internally generated timing signals. After the conversion is complete, $\overline{INT}$ goes low. Since $\overline{RD}$ is fixed low, DB0–DB9 will go from high impedance to active state as soon as $\overline{INT}$ goes low. $\overline{INT}$ is reset high and DB0–DB9 is reset to high impedance on rising edge of $\overline{WR}$ and $\overline{RD}$.

Read Mode Operation allows a conversion to be done with the device's own internal timing and thus, no eternal timing is needed.

1.6.4 Power-On Reset

When power is first applied, an internal power-on reset and timer circuit inhibits the $\overline{CS}$ input and resets the internal circuitry to prevent the ML2271 from starting in an unknown state. During this period of approximately 50µs, $\overline{INT}$ remains high and the data bus is in the high-impedance state.

2.0 TYPICAL APPLICATIONS

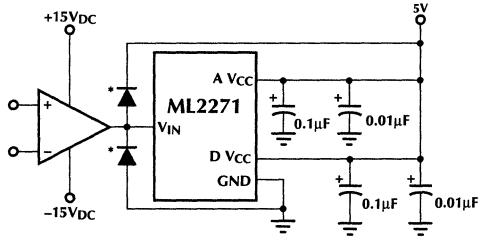


Figure 8. Protecting the Input

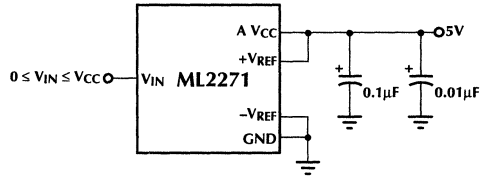


Figure 9. Using V_{CC} as Reference for Ratiometric Operation

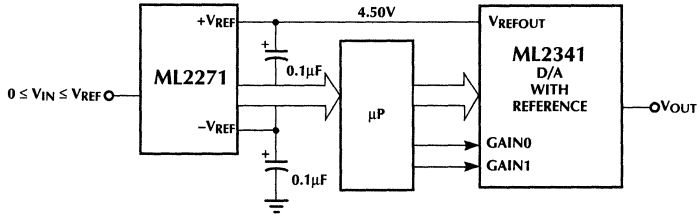


Figure 10. Using External Reference of D/A

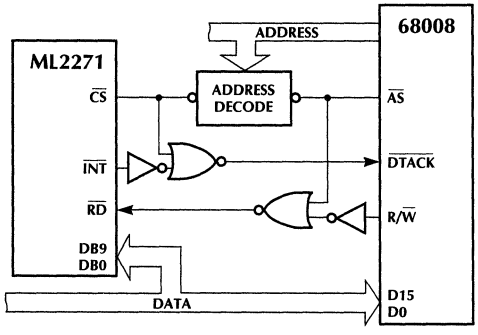


Figure 11. 68000 Type Interface to ML2271

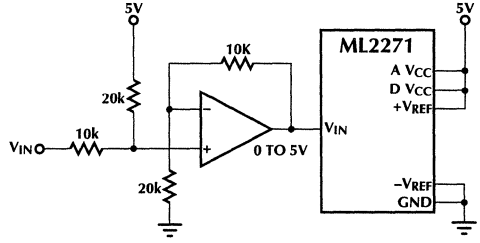


Figure 12. ±2.5V Analog Input Range

2.0 TYPICAL APPLICATIONS (Continued)

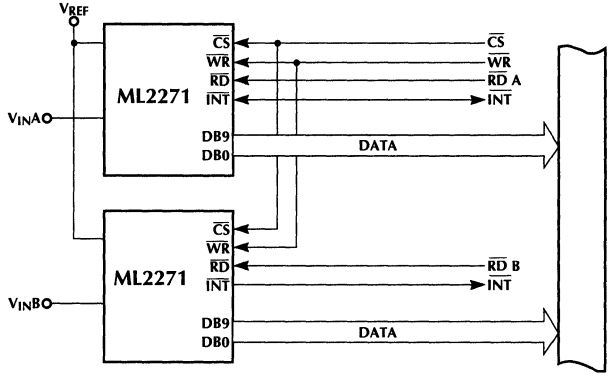


Figure 13. Simultaneous Sampling of Two Variables

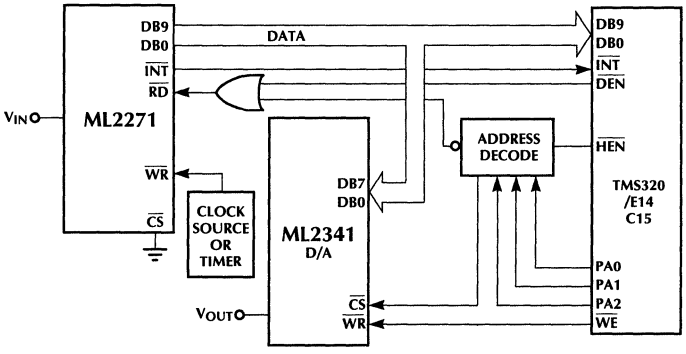


Figure 14. TMS320 Interface with D/A Output

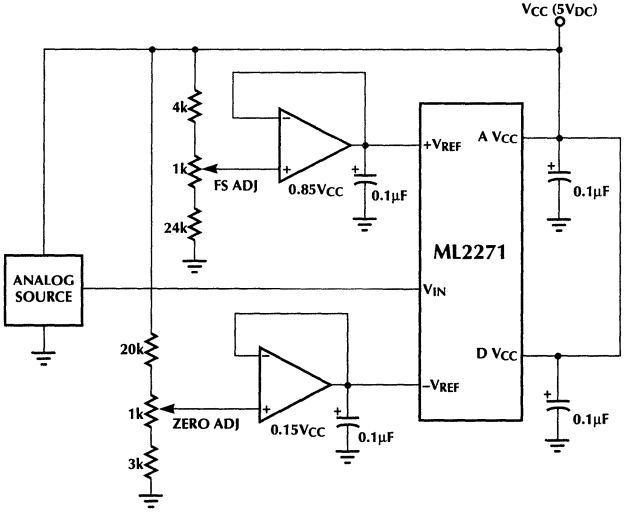


Figure 15. Operating with a Ratiometric Analog Signal of 15% of V_{CC} to 85% of V_{CC}

ORDERING INFORMATION

PART NUMBER	LINEARITY ERROR	TEMPERATURE RANGE	PACKAGE
ML2271CIP	±1 LSB	–40°C TO +85°C	MOLDED DIP (P20)
ML2271CIS		–40°C TO +85°C	MOLDED SOIC (S20)
ML2271CCP	±1 LSB	0°C TO +70°C	MOLDED DIP (P20)
ML2271CCS		0°C TO +70°C	MOLDED SOIC (S20)

ML2280, ML2283

Serial I/O 8-Bit A/D Converters

GENERAL DESCRIPTION

The ML2280 and ML2283 are 8-bit successive approximation A/D converters with serial I/O and configurable input multiplexers with up to 4 input channels.

All errors of the sample-and-hold incorporated on the ML2280 and ML2283, are accounted for in the analog-to-digital converters accuracy specification.

The voltage reference can be externally set to any value between GND and V_{CC}, thus allowing a full conversion over a relatively small voltage span if desired.

The ML2283 is an enhanced double polysilicon CMOS pin compatible second source for the ADC0833 A/D converter. All parameters are guaranteed over temperature with a power supply voltage of 5V ±10%.

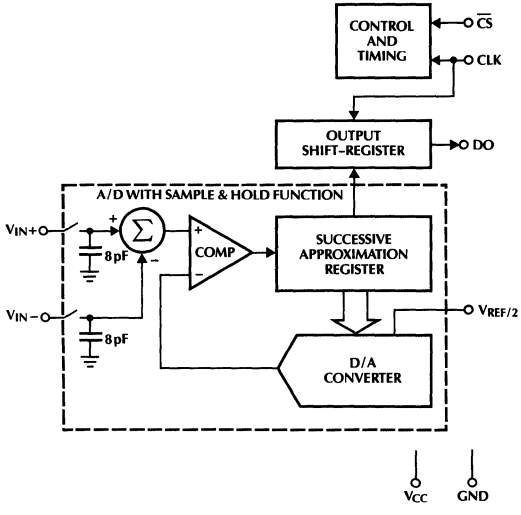
FEATURES

- Conversion time 6μs
- ML2280 capable of digitizing a 5V, 40kHz sine wave
- Total unadjusted error with external reference ±½LSB or ±1LSB
- Sample-and-hold 375ns acquisition
- 0 to 5V analog input range with single 5V power supply
- 2.5V reference provides 0 to 5V analog input range
- No zero or full-scale adjust required
- Low power 12.5mW MAX
- Analog input protection 25mA (min) per input
- Differential analog voltage inputs
- 0.3" width 8- or 14-pin DIP
- 4-channel input MUX option
- Superior pin compatible replacement for ADC0833

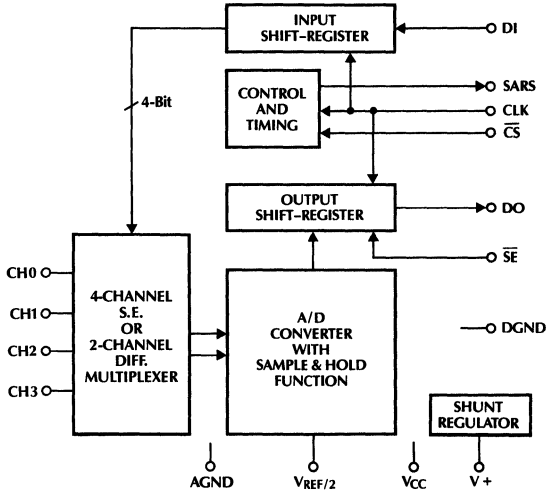
2

BLOCK DIAGRAMS

ML2280



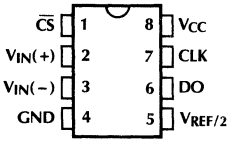
ML2283



PIN CONNECTIONS

ML2280 Single Differential Input

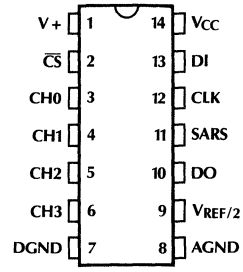
8-PIN DIP



TOP VIEW

ML2283 4-Channel MUX

14-PIN DIP



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
V_{CC}	Positive supply. 5 volts ± 10%
DGND	Digital ground. 0 volts. All digital inputs and outputs are referenced to this point.
AGND	Analog ground. The negative reference voltage for A/D converter.
GND	Combined analog and digital ground.
CH0, $V_{IN}+$, $V_{IN}-$	Analog inputs. Digitally selected to be single ended (V_{IN}) or; $V_{IN}+$ or $V_{IN}-$ of a differential input. Analog range = GND ≤ V_{IN} ≤ V_{CC}
$V_{REF/2}$	Reference. The analog input range is twice the positive reference voltage value applied to this pin.
V+	Input to the Shunt Regulator.
DO	Data out. Digital output which contains result of A/D conversion. The serial data is clocked out on falling edges of CLK.

NAME	FUNCTION
SARS	Successive approximation register status. Digital output which indicates that a conversion is in progress. When SARS goes to 1, the sampling window is closed and conversion begins. When SARS goes to 0, conversion is completed. When $\overline{CS}$ = 1, SARS is in high impedance state.
CLK	Clock. Digital input which clocks data in on DI on rising edges and out on DO on falling edges. Also used to generate clocks for A/D conversion.
DI	Data input. Digital input which contains serial data to program the MUX and channel assignments.
$\overline{CS}$	Chip select. Selects the chip for multiplexer and channel assignment and A/D converison. When $\overline{CS}$ = 1, all digital outputs are in high impedance state. When $\overline{CS}$ = 0, normal A/D conversion takes place.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Current into V+ 15mA
Supply Voltage, V_{CC} 6.5V
Voltage
  Logic Inputs ..... −7V to V_{CC} +7V
  Analog Inputs ..... −0.3V to V_{CC} +0.3V
Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... −65°C to +150°C
Package Dissipation
  at T_A = 25°C (Board Mount) 800mW
Lead Temperature (Soldering 10 sec.)
  Dual-In-Line Package (Molded) ..... 260°C
  Dual-In-Line Package (Ceramic) ..... 300°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... 4.5V_{DC} to 6.3V_{DC}
Temperature Range (Note 3) ..... $T_{MIN} \leq T_A \leq T_{MAX}$
  ML2280BMJ, ML2283BMJ ..... −55°C to +125°C
  ML2280BIJ, ML2283BIJ ..... −40°C to +85°C
  ML2280CIJ, ML2283CIJ
  ML2280BCP, ML2283BCP ..... 0°C to +70°C
  ML2280CCP, ML2283CCP

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $f_{CLK} = 1.333MHz$, and $V_{REF/2} = 2.5V$.

PARAMETER	NOTES	CONDITIONS	ML2280B, ML2283B			ML2280C, ML2283C			UNITS
			MIN	TYP NOTE 4	MAX	MIN	TYP NOTE 4	MAX	
CONVERTER AND MULTIPLEXER CHARACTERISTICS									
Total Unadjusted Error	5, 7	$V_{REF/2}$ = 2.5V $V_{REF/2}$ not Connected			±1/2 ±2			±1 ±2	LSB LSB
Reference Input Resistance, $V_{REF/2}$	5		3	5	7.5	3	5	7.5	kΩ
Common-Mode Input Range	5,8		GND −0.05		V_{CC} +0.05	GND −0.05		V_{CC} +0.05	V
DC Common-Mode Error	6	Common Mode Voltage GND to $V_{CC/2}$		±1/16	±1/4		±1/16	±1/4	LSB
AC Common-Mode Error	6	Comon Mode Voltage GND to V_{CC}, 0 to 50kHz			±1/4			±1/4	LSB
DC Power Supply Sensitivity	6	$V_{CC} = 5V \pm 10\%$ $V_{REF} \leq V_{CC}$ +0.1V		±1/32	±1/4		±1/32	±1/4	LSB
AC Power Supply Sensitivity	6	100mV_{P-P}, 25kHz Sine on V_{CC}			±1/4			±1/4	LSB
Change in Zero Error from V_{CC} = 5V to Internal Zener Operation	6	15mA into V+ V_{CC} = N.C. $V_{REF/2}$ = 2.5V		±1/2			±1/2		LSB
V_Z, Internal Diode Regulated Breakdown (at V+)		15mA into V+		6.9			6.9		V
V+ Input Resistance	5		20	35		20	35		kΩ
I_{Off}, Off Channel Leakage Current	5, 9	On Channel = V_{CC} Off Channel = 0V	−1			−1			µA
		On Channel = 0V Off Channel = V_{CC}			+1			+1	µA
I_{On}, On Channel Leakage Current	5, 9	On Channel = 0V Off Channel = V_{CC}	−1			−1			µA
		On Channel = V_{CC} Off Channel = 0V			+1			+1	µA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $f_{CLK} = 1.333\,MHz$, and $V_{REF/2} = 2.5V$.

PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 4	MAX	LIMIT UNITS
DIGITAL AND DC CHARACTERISTICS						
$V_{IN(1)}$, Logical "1" Input Voltage	5		2.0			V
$V_{IN(0)}$, Logical "0" Input Voltage	5				0.8	V
$I_{IN(1)}$, Logical "1" Input Current	5	$V_{IN} = V_{CC}$			1	μA
$I_{IN(0)}$, Logical "0" Input Current	5	$V_{IN} = 0V$	−1			μA
$V_{OUT(1)}$, Logical "1" Output Voltage	5	$I_{OUT} = -2\,mA$	4.0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	5	$I_{OUT} = 2\,mA$			0.4	V
I_{OUT}, Hi-Z Output Current	5	$V_{OUT} = 0V$ $V_{OUT} = V_{CC}$	−1		 1	μA μA
I_{SOURCE}, Output Source Current	5	$V_{OUT} = 0V$	−6.5			mA
I_{SINK}, Output Sink Current	5	$V_{OUT} = V_{CC}$			8.0	mA
I_{CC}, Supply Current	5			1.3	2.5	mA
AC ELECTRICAL CHARACTERISTICS						
f_{CLK}, Clock Frequency	5		10		1333	kHz
t_{ACQ}, Sample-and-Hold Acquistion				1/2		$1/f_{CLK}$
t_C, Conversion Time		Not including MUX Addressing Time		8		$1/f_{CLK}$
SNR, Signal to Noise Ratio ML2280	12	$V_{IN} = 40\,kHz$, 5V Sine. $f_{CLK} = 1.333\,MHz$ ($f_{SAMPLING} \cong 120\,kHz$). Noise is Sum of All Nonfundamental Components up to 1/2 of $f_{SAMPLING}$		47		dB
THD, Total Harmonic Distortion ML2280	12	$V_{IN} = 40\,kHz$, 5V Sine. $f_{CLK} = 1.333\,MHz$ ($f_{SAMPLING} \cong 120\,kHz$). THD is Sum of 2, 3, 4, 5 Harmonics Relative to Fundamental		−60		dB
IMD, Intermodulation Distortion ML2280	12	$V_{IN} = f_A + f_B$. $f_A = 40\,kHz$, 2.5V Sine. $f_B = 39.8\,kHz$, 2.5V Sine, $f_{CLK} = 1.333\,MHz$ ($f_{SAMPLING} \cong 120\,kHz$). IMD is $(f_A + f_B)$, $(f_A - f_B)$, $(2f_A + f_B)$, $(2f_A - f_B)$, $(f_A + 2f_B)$, $(f_A - 2f_B)$ Relative to Fundamental		−60		dB
Clock Duty Cycle	5, 10		40		60	%
t_{SET-UP} CS Falling Edge or Data Input Valid to CLK Rising Edge	5		130			ns
t_{HOLD}, Data Input Valid after CLK Rising Edge	5		80			ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $f_{CLK} = 1.333MHz$, and $V_{REF/2} = 2.5V$

PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 4	MAX	LIMIT UNITS
AC ELECTRICAL CHARACTERISTICS						
t_{pd1}, t_{pd0}—CLK Falling Edge to Output Data Valid	5, 11	$C_L = 100pF$ Data MSB First Data LSB First		 90 50	 200 110	 ns ns
t_{1H}, t_{0H}, —Rising Edge of CS to Data Output and SARS Hi-Z	6	$C_L = 10pF$, $R_L = 10k$ (see High Impedance Test Circuits)		40	90	ns
	6	$C_L = 100pF$, $R_L = 2k$		80	160	ns
C_{IN}, Capacitance of Logic Input				5		pF
C_{OUT}, Capacitance of Logic Outputs				5		pF

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < GND$ or $V_{IN} > V_{CC}$) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: −55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. 0°C to 70°C and −40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Total unadjusted error includes offset, full-scale, linearity, multiplexer and sample-and-hold errors.

Note 8: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (See Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater then the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct-especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 9: Leakage current is measured with the clock not switching.

Note 10: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum, time the clock is high or the minimum time the clock is low must be at least 300ns. The maximum time the clock can be high or low is 60μs.

Note 11: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (See Block Diagram) to allow for comparator response time.

Note 12: Because of multiplexer addressing, test conditions for the ML2283 is $V_{IN} = 30kHz$, 5V sine ($f_{SAMPLING} \approx 89kHz$).

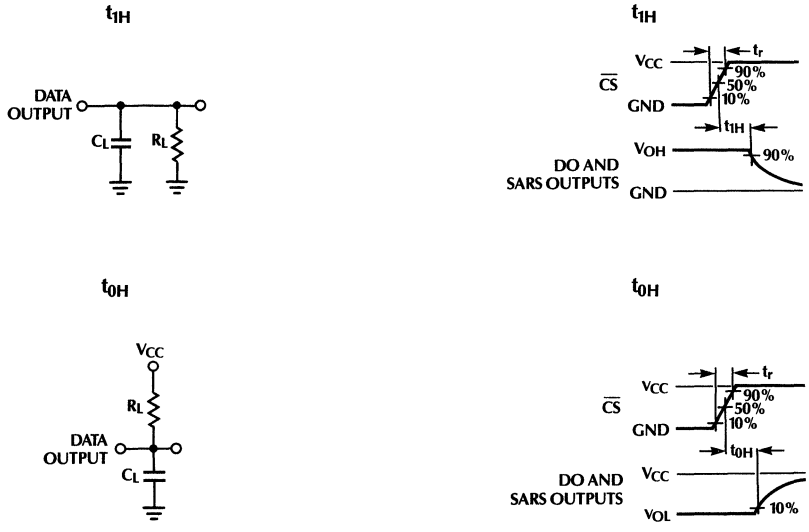


Figure 1. High Impedance Test Circuits and Waveforms

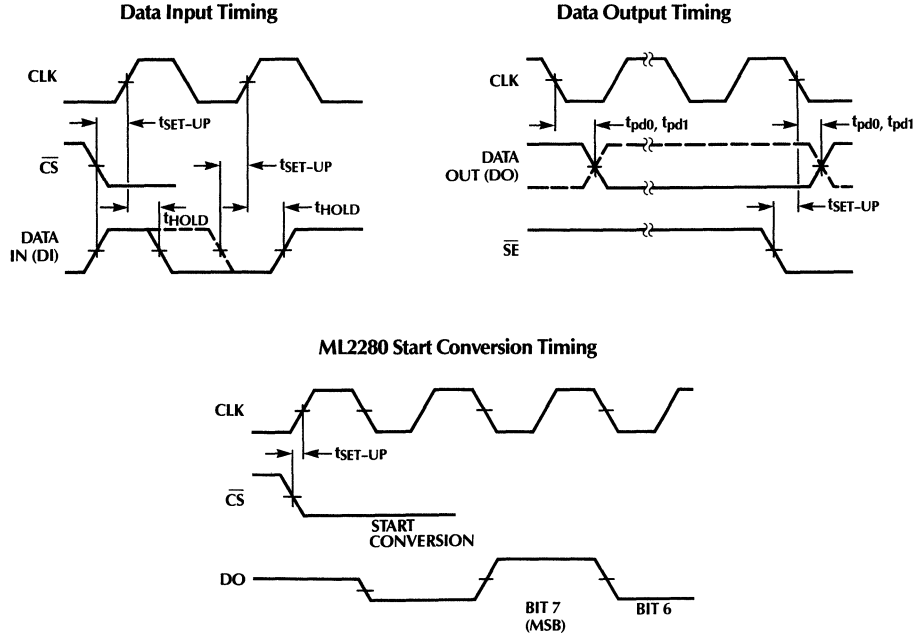
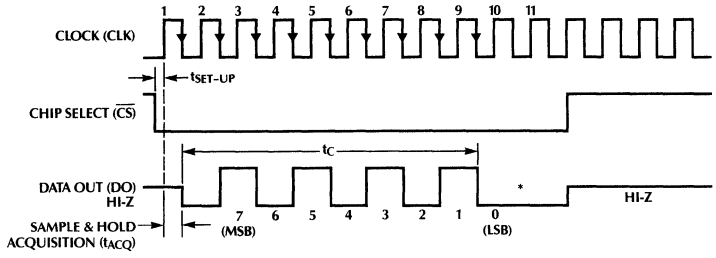


Figure 2. Timing Diagrams

ML2280 Timing



*LSB FIRST OUTPUT NOT AVAILABLE ON ML2280

2

ML2283 Timing

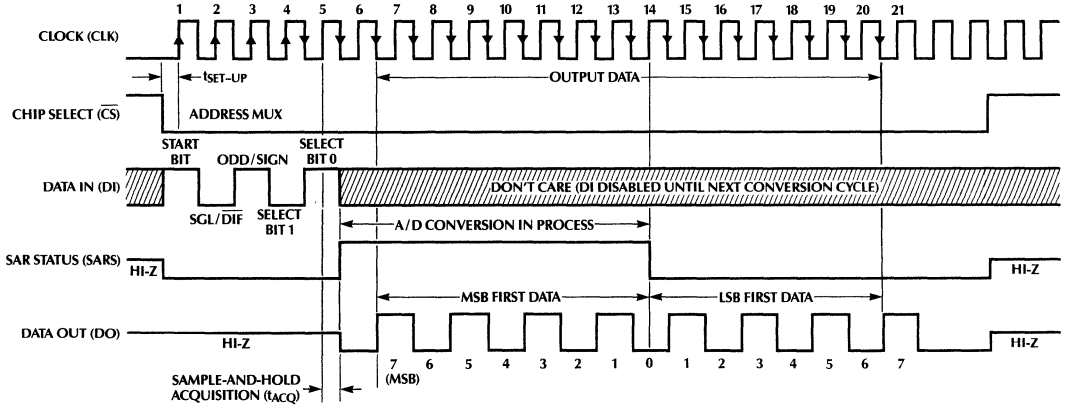


Figure 2. Timing Diagrams (Continued)

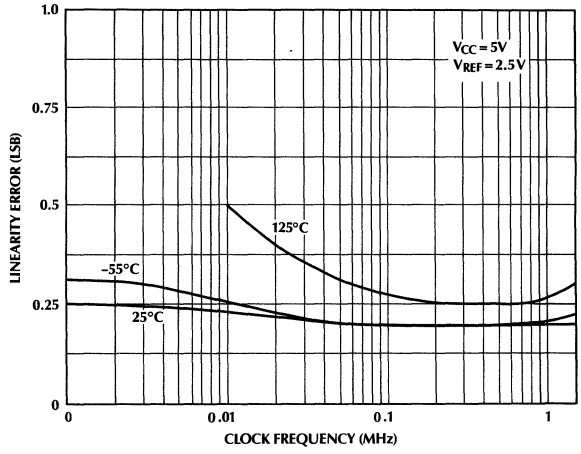


Figure 3. Linearity Error vs f_{CLK}

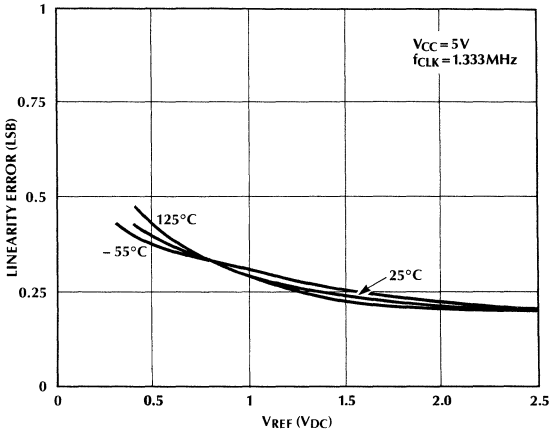


Figure 4. Linearity Error vs V_{REF} Voltage

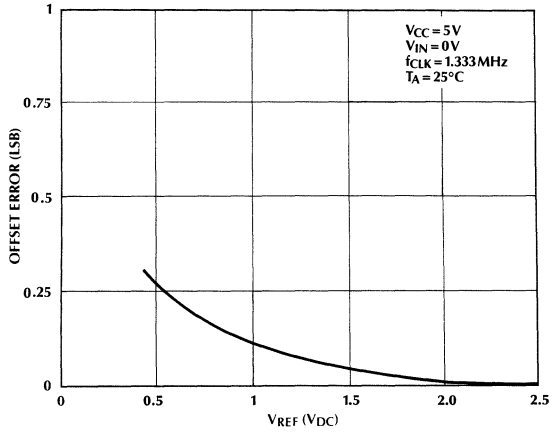
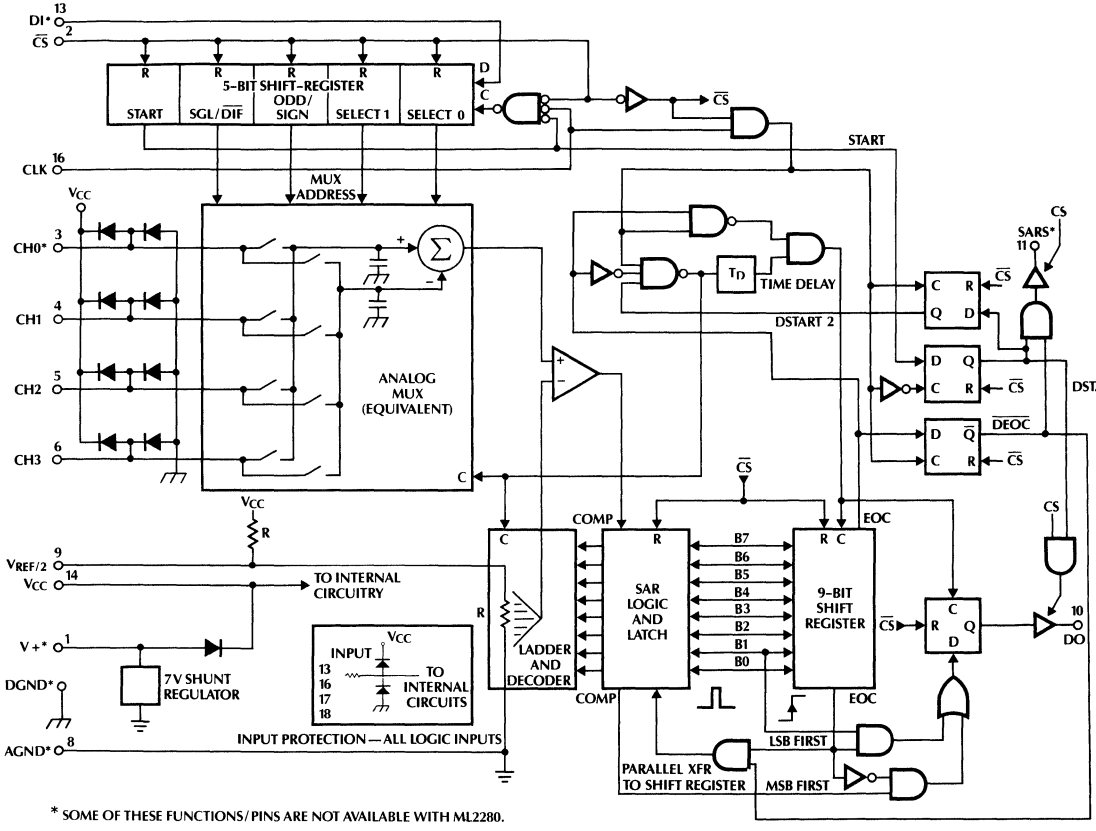


Figure 5. Unadjusted Offset Error vs V_{REF} Voltage



* SOME OF THESE FUNCTIONS/PINS ARE NOT AVAILABLE WITH ML2280.

Figure 6. ML2283 Functional Block Diagram

1.0 FUNCTIONAL DESCRIPTION

1.1 Multiplexer Addressing

The design of these converters utilizes a sample data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input, the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software configurable single ended, or differential options.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single ended or differential. In the differential case, it also assigns the polarity of the analog channels. Differential inputs are restricted to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a different pair but channel 0 or channel 1 cannot act differentially with any other channel. In addition to selecting the differential mode, the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is illustrated by the MUX addressing codes shown in *Table 1.*

The MUX address is shifted into the converter via the DI input. Since the ML2280 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 7* illustrates these different input modes.

Table 1. ML2283 MUX Addressing 4 Single-Ended or 2 Differential Channel

Single-Ended MUX Mode

MUX Address				Channel #			
SGL/ DIF	ODD/ SIGN	SELECT 1	SELECT 0	0	1	2	3
1	0	0	1	+			
1	0	1	1			+	
1	1	0	1		+		
1	1	1	1				+

Differential MUX Mode

MUX Address				Channel #			
SGL/ DIF	ODD/ SIGN	SELECT 1	SELECT 0	0	1	2	3
0	0	0	1	+	−		
0	0	1	1			+	−
0	1	0	1	−	+		
0	1	1	1			−	+

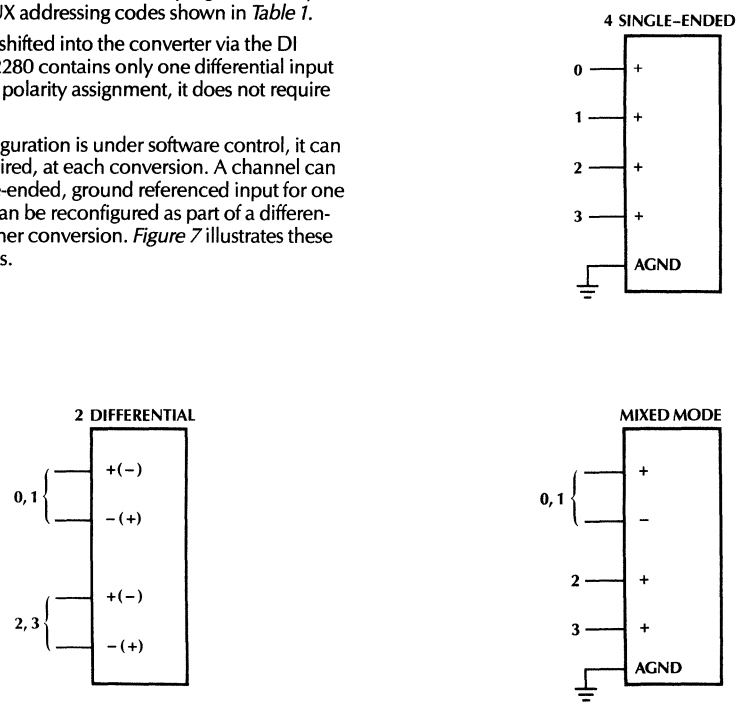


Figure 7. Analog Input Multiplexer Functional Options for ML2283

1.2 Digital Interface

The block diagram and timing diagrams in *Figures 2-5* illustrate how a conversion sequence is performed.

A conversion is initiated when $\overline{CS}$ is pulsed low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

A clock is applied to the CLK input. On each rising edge of the clock, the data on DI is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on the DI input (all leading edge zeros are ignored). After the start bit, the device clocks in the next 2 to 4 bits for the MUX assignment word.

When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of 1/2 clock period is used for sample-and-hold settling through the selected MUX channels. The SAR status output goes high at this time to signal that a conversion is now in progress and the DI input is ignored.

The DO output comes out of high impedance and provides a leading zero for this one clock period.

When the conversion begins, the output of the comparator, which indicates whether the analog input is greater than or less than each successive voltage from the internal DAC, appears at the DO output on each falling edge of the clock. This data is the result of the conversion being shifted out (with MSB coming first) and can be read by external logic or μP immediately.

After 8 clock periods, the conversion is completed. The SAR status line returns low to indicate this 1/2 clock cycle later.

The serial data is always shifted out MSB first during the conversion. After the conversion has been completed, the data is shifted out a second time with LSB first. The ML2280 data is shifted out only once, MSB first.

All internal registers are cleared when the $\overline{CS}$ input is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI input and DO output can be tied together and controlled through a bidirectional μP I/O bit with one connection. This is possible because the DI input is only latched in during the MUX addressing interval while the DO output is still in the high impedance state.

1.3 Reference

The ML2280 and ML2283 are intended primarily for use in circuits requiring absolute accuracy. In this type of system, the analog inputs vary between very specific voltage limits and the reference voltage for the A/D converter must remain stable with time and temperature. For ratiometric applications, see the ML2281 and ML2284 which have a V_{REF} input that can be tied to V_{CC}.

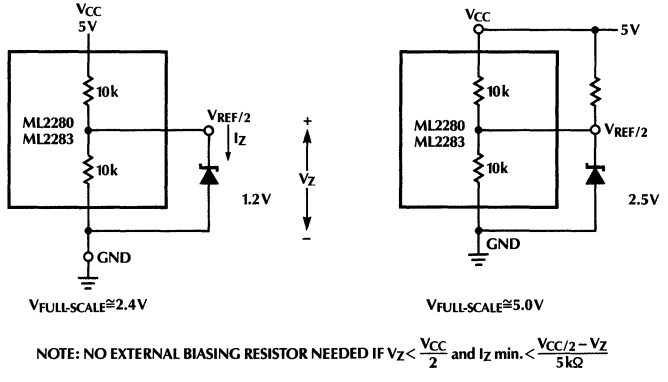
The voltage applied to the $V_{REF/2}$ pin defines the voltage span of the analog input (the difference between VIN+ and $V_{IN}-$) over which the 256 possible output codes apply. A full-scale conversion (an all 1s output code) will result when the voltage difference between a selected "+" input and "−" input is approximately *twice* the voltage at the $V_{REF/2}$ pin. This internal gain of 2 from the applied reference to the full-scale input voltage allows biasing a low voltage reference diode from the $5V_{DC}$ converter supply. To accommodate a 5V input span, only a 2.5V reference is required. The output code changes in accordance with the following equation:

$$\text{Output Code} = 256\left(\frac{V_{IN}(+) - V_{IN}(-)}{2(V_{REF}/2)}\right)$$

where the output code is the decimal equivalent of the 8-bit binary output (ranging from 0 to 255) and the term $V_{REF/2}$ is the voltage to ground.

The $V_{REF/2}$ pin is the center point of a two resistor divider (each resistor is 10kΩ) connected from V_{CC} to ground. Total ladder input resistance is the parallel combination of these two equal resistors. As shown in *Figure 8*, a reference diode with a voltage less than $V_{CC/2}$ can be connected without requiring an external biasing resistor if its current requirements meet the indicated level.

The minimum value of $V_{REF/2}$ can be quite small (See Typical Performance Curves) to allow direct conversions of transducer outputs providing less than a 5V output span. Particu-



NOTE: NO EXTERNAL BIASING RESISTOR NEEDED IF $V_Z < \frac{V_{CC}}{2}$ and I_Z min. $< \frac{V_{CC/2} - V_Z}{5k\Omega}$

Figure 8. Reference Biasing

lar care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF/256}$).

1.4 Analog Inputs and Sample/Hold

An important feature of the ML2280 and ML2283 is that they can be located at the source of the analog signal and then communicate with a controlling μP with just a few wires. This avoids bussing the analog inputs long distances and thus reduces noise pickup on these analog lines. However, in some cases, the analog inputs have a large common mode voltage or even some noise present along with the valid analog signal.

The differential input of these converters reduces the effects of common mode input noise. Thus, if a common mode voltage is present on both "+" and "−" inputs, such as 60 Hz, the converter will reject this common mode voltage since it only converts the difference between "+" and "−" inputs.

The ML2280 and ML2283 have a true sample-and-hold circuit which samples both "+" and "−" inputs simultaneously. This simultaneous sampling with a true S/H will give common mode rejection and AC linearity performance that is superior to devices where the two input terminals are not sampled at the same instant and where true sample-and-hold capability does not exist. Thus, these A/D converters can reject AC common mode signals from DC-50 kHz as well as maintain linearity for signals from DC-50kHz.

The signal at the analog input is sampled during the interval when the sampling switch is closed prior to conversion start. The sampling window (S/H acquisition time) is 1/2 CLK period wide and occurs 1/2 CLK period before DO goes from high impedance to active low state. When the sampling switch closes at the start of the S/H acquisition time, 8 pF of capacitance is thrown onto the analog input. 1/2 CLK period later, the sampling switch is opened and the signal present at the analog input is stored. Any error on the analog input at the end of the S/H acquisition time will cause additional conversion error. Care should be taken to allow adequate charging or settling time from the source. If more charging or settling time is needed to reduce these analog input errors, a longer CLK period can be used.

For latch-up immunity each analog input has dual diodes to the supply rails, and a minimum of ±25 mA (±100 mA typically) can be injected into each analog input without causing latch-up.

1.5 Zero Error Adjustment

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, V_{INMIN} is not ground, a zero offset can be done. The converter can be made to output 00000000 digital code for this minimum input voltage by biasing any $V_{IN}-$ input at this V_{INMIN} value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}-$ input and applying a small magnitude positive voltage to the $V_{IN}+$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 00000000 to 00000001 and the ideal 1/2 LSB value (1/2 LSB = 9.8 mV for $V_{REF/2} = 2.500 V_{DC}$).

1.6 Full-Scale Adjustment

The full-scale adjustment can be made by applying a differential input voltage which is 1 1/2 LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF/2}$ input for a digital output code which is just changing from 11111110 to 11111111.

1.7 Adjustment for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A $V_{IN}+$ voltage which equals this desired zero reference plus 1/2 LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00000000 to 00000001 code transition.

The full-scale adjustment should be made by forcing a voltage to the $V_{IN}+$ input which is given by:

$$V_{IN}+ \text{ fs adjust} = V_{MAX} - 1.5*[(V_{MAX} - V_{MIN})/256]$$

where V_{MAX} = high end of the analog input range

V_{MIN} = low end (offset zero) of the analog range

The V_{REF} or V_{CC} voltage is then adjusted to provide a code change from 11111110 to 11111111.

1.8 Shunt Regulator

A unique feature of the ML2283 is the inclusion of a shunt regulator connected from V+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode as shown in *Figure 9*. When the regulator is turned on, the V+ voltage is clamped at 11 V_{BE} set by the internal resistor ratio. The typical I-V curve of the shunt regulator is shown in *Figure 10*. It should be noted that before V+ voltage is high enough to turn on the shunt regulator (which occurs at about 5.5 V), 35 kΩ of resistance is observed between V+ and GND. When the shunt regulator is not used, V+ pin should be either left floating or tied to GND. The temperature coefficient of the regulator is −22 mV/°C.

2.0 APPLICATIONS

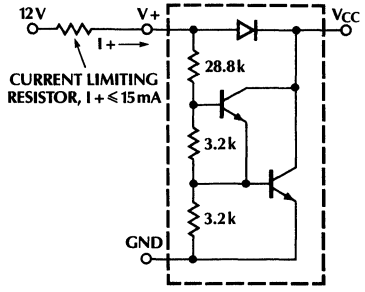


Figure 9. Shunt Regulator

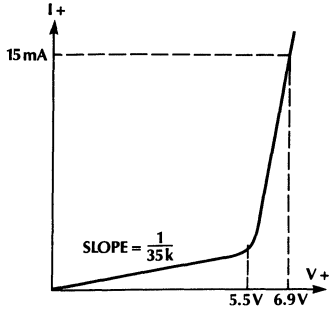
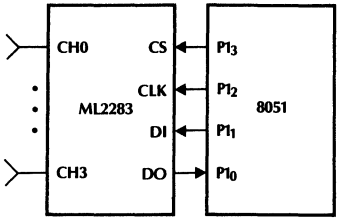


Figure 10. I–V Characteristic of the Shunt Regulator

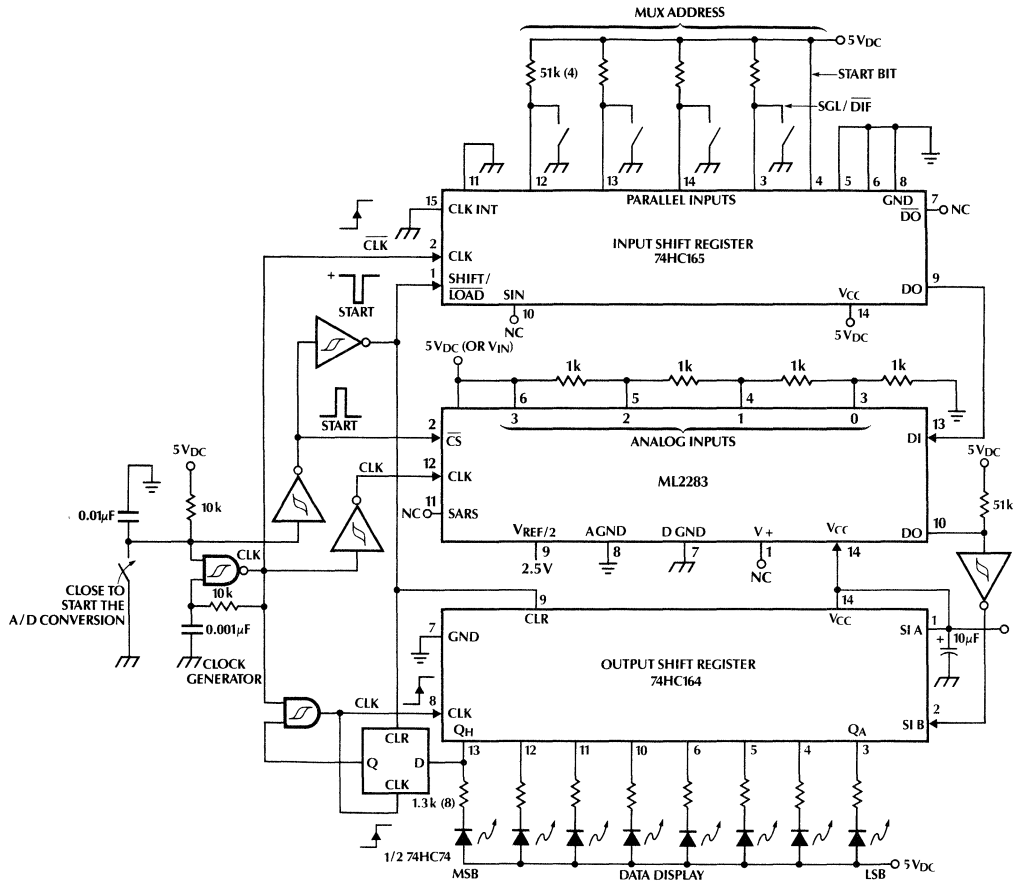
8051 Interface and Controlling Software



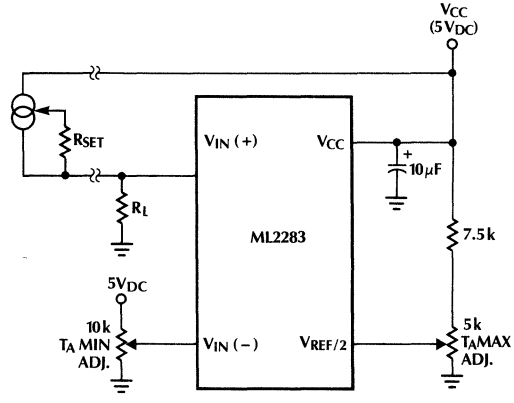
Mnemonic			Instruction
START	ANL	P1, #0F7H	;SELECT A/D (CS = 0)
	MOV	B, #5	;BIT COUNTER ← 5
	MOV	A, #ADDR	;A ← MUX BIT
LOOP 1:	RRC	A	;CY ← ADDRESS BIT
	JC	ONE	;TEST BIT ;BIT = 0
ZERO:	ANL	P1, #0FEH	;DI ← 0
	SJMP	CONT	;CONTINUE ;BIT = 1
ONE:	ORL	P1, #1	;D1 ← 1
CONT:	ACALL	PULSE	;PULSE SK 0 → 1 → 0
	DJNZ	B, LOOP 1	;CONTINUE UNTIL DONE
	ACALL	PULSE	;EXTRA CLOCK FOR SYNC
	MOV	B, #8	;BIT COUNTER ← 8
LOOP 2:	ACALL	PULSE	;PULSE SK 0 → 1 → 0
	MOV	A, P1	;CY ← DO
	RRC	A	
	RRC	A	
	MOV	A, C	;A ← RESULT
	RLC	A	;A(0) ← BIT AND SHIFT
	MOV	C, A	;C ← RESULT
	DJNZ	B, LOOP 2	;CONTINUE UNTIL DONE
RETI			
			;PULSE SUBROUTINE
PULSE:	ORL	P1, #04	;SK ← 1
	NOP		;DELAY
	ANL	P1, #0FBH	;SK ← 0
	RET		

APPLICATIONS (Continued)

ML2283 "Stand-Alone" or Evaluation Circuit

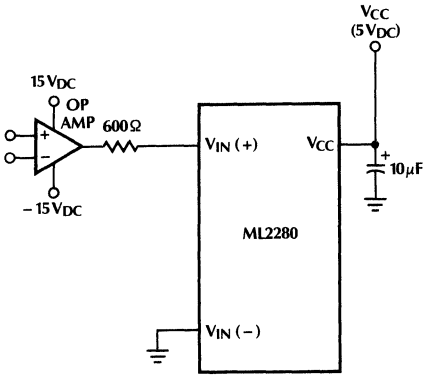


Low-Cost Remote Temperature Sensor



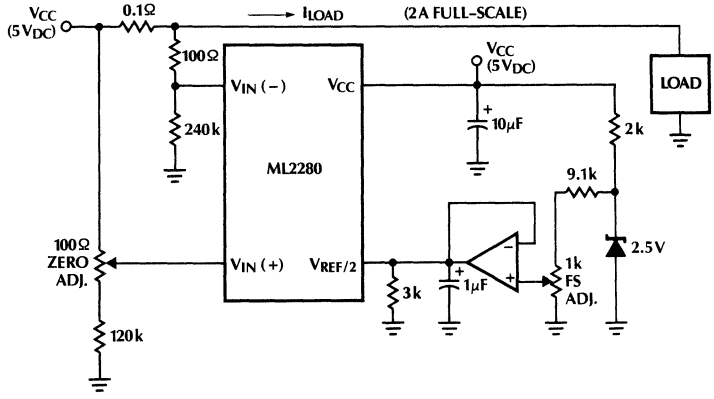
APPLICATIONS (Continued)

Protecting the Input

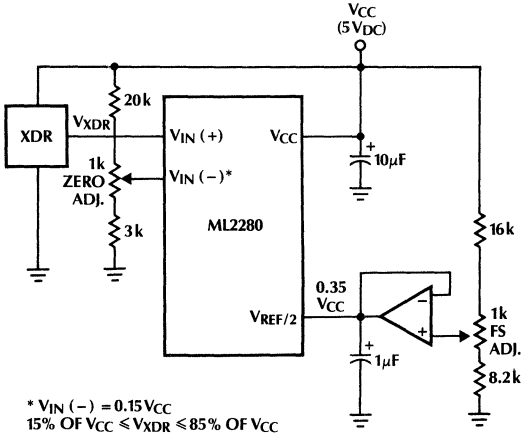


DIODE CLAMPING IS NOT NEEDED
IF CURRENT IS LIMITED TO 25 mA

Digitizing a Current Flow

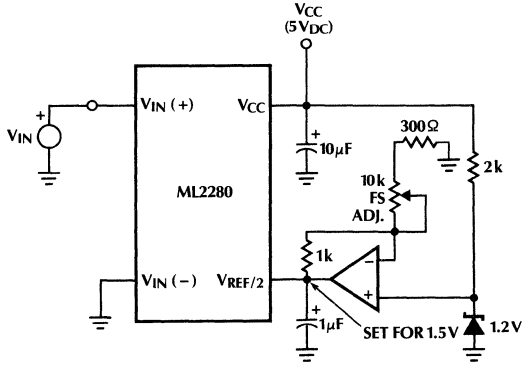


Operating with Ratiometric Transducers



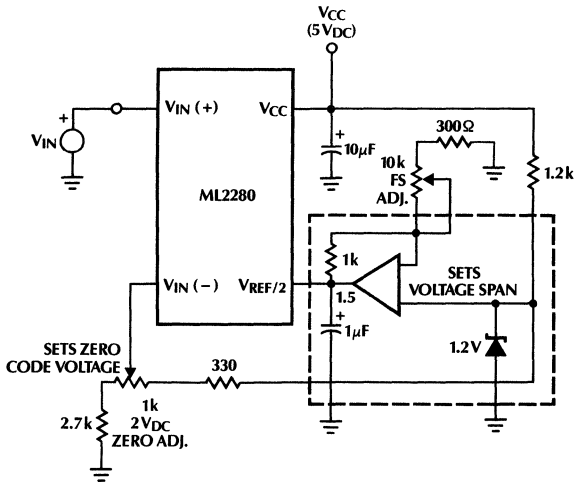
* $V_{IN}(-) = 0.15 V_{CC}$
15% OF $V_{CC} \leq V_{XDR} \leq 85\%$ OF V_{CC}

Span Adjust: $0V \leq V_{IN} \leq 3V$

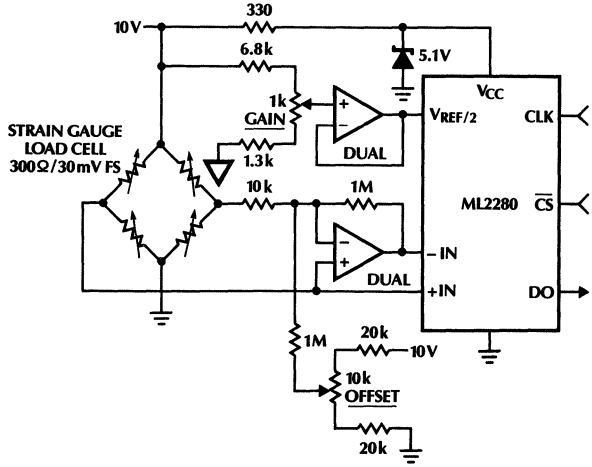


APPLICATIONS (Continued)

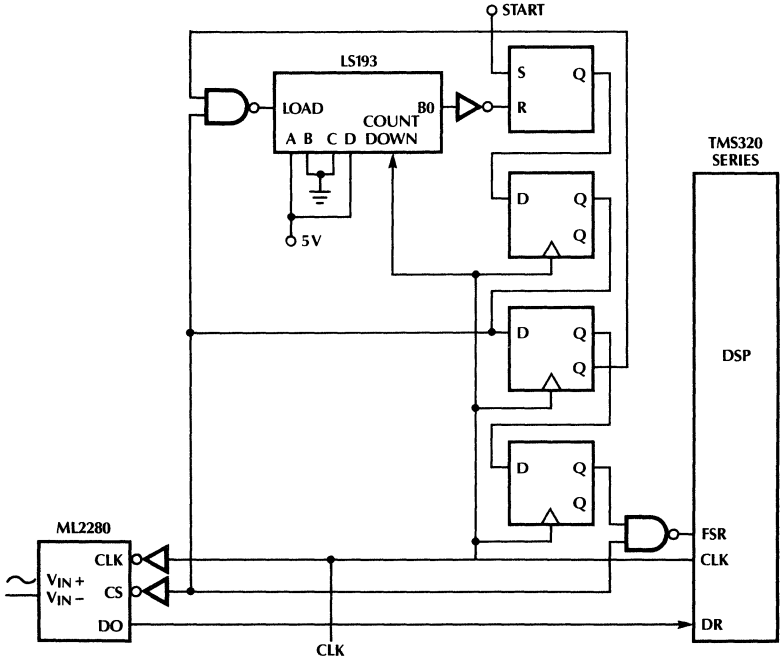
Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



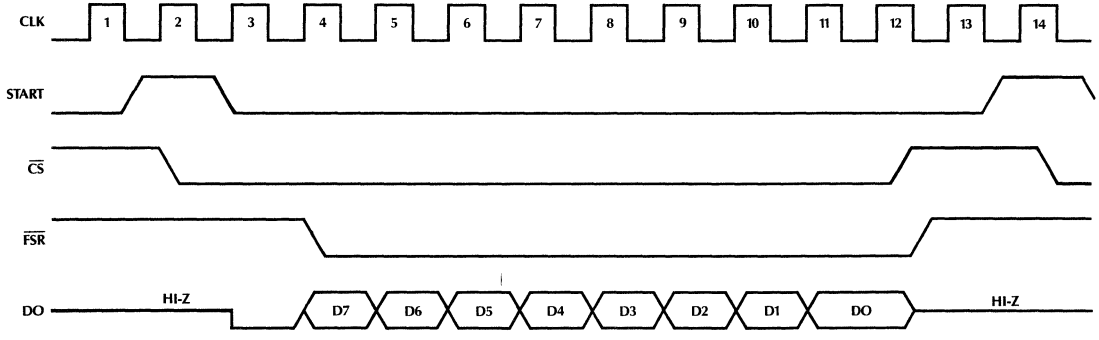
Digital Load Cell



- USES ONE MORE WIRE THAN LOAD CELL ITSELF
- TWO MINI-DIPs COULD BE MOUNTED INSIDE LOAD CELL FOR DIGITAL OUTPUT TRANSDUCER
- ELECTRONIC OFFSET AND GAIN TRIMS RELAX MECHANICAL SPECS FOR GAUGE FACTOR AND OFFSET
- LOW LEVEL CELL OUTPUT IS CONVERTED IMMEDIATELY FOR HIGH NOISE IMMUNITY



Sampling Rate 111KHz, Data Rate 1.33MHz



Interfacing ML2280 to TMS320 Series

ORDERING INFORMATION

PART NUMBER	ALTERNATE PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
SINGLE ANALOG INPUT, 8-PIN PACKAGE				
ML2280BMJ		±½LSB	−55°C to +125°C	HERMETIC DIP (J08)
ML2280BIJ			−40°C to +85°C	HERMETIC DIP (J08)
ML2280BCP			0° to +70°C	MOLDED DIP (P08)
ML2280CIJ		±1LSB	−40°C to +85°C	HERMETIC DIP (J08)
ML2280CCP			0°C to +70°C	MOLDED DIP (P08)
FOUR ANALOG INPUTS, 14-PIN PACKAGE				
ML2283BMJ	ADC0833BJ	±½LSB	−55°C to +125°C	HERMETIC DIP (J14)
ML2283BIJ	ADC0833BCJ		−40°C to +85°C	HERMETIC DIP (J14)
ML2283BCP	ADC0833BCN		0° to +70°C	MOLDED DIP (P14)
ML2283CIJ	ADC0833CCJ	±1LSB	−40°C to +85°C	HERMETIC DIP (J14)
ML2283CCP	ADC0833CCN		0°C to +70°C	MOLDED DIP (P14)

ML2281, ML2282 ML2284, ML2288

Serial I/O 8-Bit A/D Converters with Multiplexer Options

GENERAL DESCRIPTION

The ML2281 family are 8-bit successive approximation A/D converters with serial I/O and configurable input multiplexers with up to 8 input channels.

All errors of the sample-and-hold, incorporated on the ML2281 family are accounted for in the analog-to-digital converters accuracy specification.

The voltage reference can be externally set to any value between GND and V_{CC}, thus allowing a full conversion over a relatively small voltage span if desired.

The ML2281 family is an enhanced double polysilicon CMOS pin compatible second source for the ADC0831, ADC0832, ADC0834, and ADC0838 A/D converters. The ML2281 series enhancements are faster conversion time, true sample-and-hold function, superior power supply rejection, improved AC common mode rejection, faster digital timing, and lower power dissipation. All parameters are guaranteed over temperature with a power supply voltage of 5V ±10%.

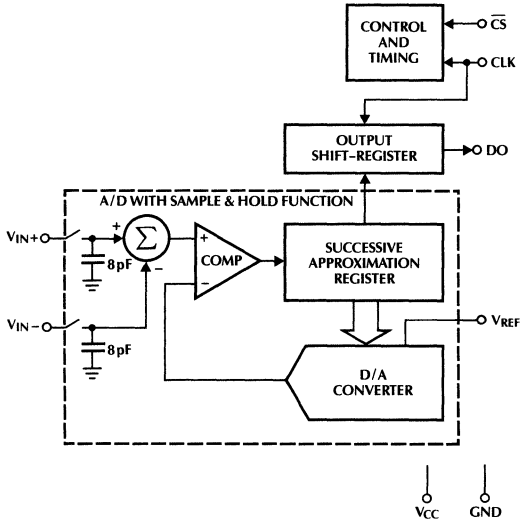
FEATURES

- Conversion time 6μs
- Total unadjusted error ±½LSB or ±1LSB
- Sample-and-hold 375 ns acquisition
- 2, 4, or 8-input multiplexer options
- 0 to 5V analog input range with single 5V power supply
- Operates ratiometrically or with up to 5V voltage reference
- No zero or full-scale adjust required
- ML2281 capable of digitizing a 5V, 40kHz sine wave
- Low power 12.5mW MAX
- 0.3" width 8-, 14-, or 20-pin DIP
- 20-pin surface mount PCC ML2288
- Superior pin compatible replacement for ADC0831, ADC0832, ADC0834, and ADC0838
- Analog input protection 25mA (min) per input

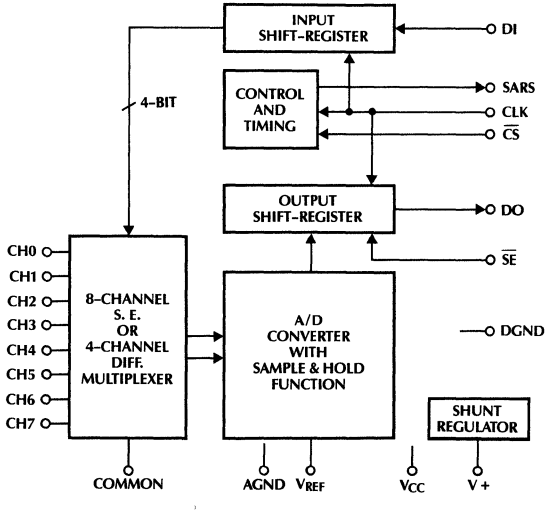
2

BLOCK DIAGRAMS

ML2281



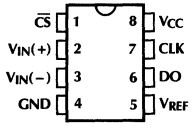
ML2288



PIN CONNECTIONS

ML2281 Single Differential Input

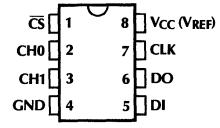
8-PIN DIP



TOP VIEW

ML2282 2-Channel MUX

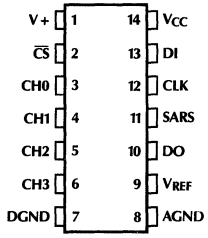
8-PIN DIP



TOP VIEW

ML2284 4-Channel MUX

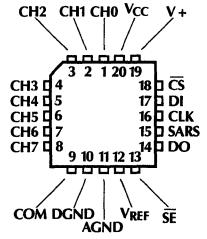
14-PIN DIP



TOP VIEW

ML2288 8-Channel MUX

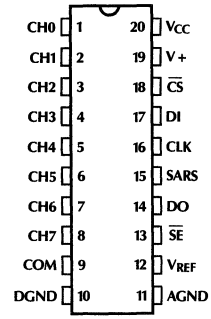
20-PIN PCC



TOP VIEW

ML2288 8-Channel MUX

20-PIN DIP



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
V_{CC}	Positive supply. 5 volts ± 10%
DGND	Digital ground. 0 volts. All digital inputs and outputs are referenced to this point.
AGND	Analog ground. The negative reference voltage for A/D converter.
CH0-7, $V_{IN}+$, $V_{IN}-$	Analog inputs. Digitally selected to be single ended (V_{IN}) or; $V_{IN}+$ or $V_{IN}-$ of a differential input. Analog range = GND ≤ V_{IN} ≤ V_{CC}
COM	Common reference point for analog inputs. A/D conversion is performed on voltage difference between analog input and this common reference point if single-end conversion is specified.
V_{REF}	Reference. The positive reference voltage for A/D converter.
$\overline{SE}$	Shift enable. Input controls whether LSB first bit stream is shifted out on serial output DO. If $\overline{SE}$ = 1, MSB first is shifted out only. If $\overline{SE}$ = 0, an MSB first bit stream is shifted out, then a second bit stream with LSB first is shifted out after end of conversion.
V+	Input to the Shunt Regulator.

NAME	FUNCTION
DO	Data out. Digital output which contains result of A/D conversion. The serial data is clocked out on falling edges of CLK.
SARS	Successive approximation register status. Digital output which indicates that a conversion is in progress. When SARS goes to 1, the sampling window is closed and conversion begins. When SARS goes to 0, conversion is completed. When $\overline{CS}$ = 1, SARS is in high impedance state.
CLK	Clock. Digital input which clocks data in on DI on rising edges and out on DO on falling edges. Also used to generate clocks for A/D conversion.
DI	Data input. Digital input which contains serial data to program the MUX and channel assignments.
$\overline{CS}$	Chip select. Selects the chip for multiplexer and channel assignment and A/D converison. When $\overline{CS}$ = 1, all digital outputs are in high impedance state. When $\overline{CS}$ = 0, normal A/D conversion takes place.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Current into V+ 15mA
Supply Voltage, V_{CC} 6.5V
Voltage
  Logic Inputs ..... $-7V$ to V_{CC} $+7V$
  Analog Inputs ..... $-0.3V$ to V_{CC} $+0.3V$
Input Current per Pin (Note 2) ..... $\pm 25mA$
Storage Temperature ..... $-65°C$ to $+150°C$
Package Dissipation
  at $T_A = 25°C$ (Board Mount) 800mW
Lead Temperature (Soldering 10 sec.)
  Dual-In-Line Package (Molded) ..... 260°C
  Dual-In-Line Package (Ceramic) ..... 300°C
  Molded Chip Carrier Package
    Vapor Phase (60 sec.) ..... 215°C
    Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... $4.5V_{DC}$ to $6.3V_{DC}$
Temperature Range (Note 3) ..... $T_{MIN} \leq T_A \leq T_{MAX}$
  ML2281/2/4/8 BMJ ..... $-55°C$ to $+125°C$
  ML2281/2/4/8 CMJ
  ML2281/2/4/8 BIJ ..... $-40°C$ to $+85°C$
  ML2281/2/4/8 CIJ
  ML2281/2/4/8 BCP ..... 0°C to +70°C
  ML2281/2/4/8 CCP

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{REF} = 5V \pm 10\%$, and $f_{CLK} = 1.333MHz$

PARAMETER	NOTES	CONDITIONS	ML2281B, ML2282B ML2284B, ML2288B MIN	TYP NOTE 4	MAX	ML2281C, ML2282C ML2284C, ML2288C MIN	TYP NOTE 4	MAX	UNITS
CONVERTER AND MULTIPLEXER CHARACTERISTICS									
Total Unadjusted Error	5, 7	$V_{REF} = V_{CC}$			$\pm 1/2$			± 1	LSB
Reference Input Resistance	5,8		6	10	15	6	10	15	kΩ
Common-Mode Input Range	5,9		GND -0.05		V_{CC} $+0.05$	GND -0.05		V_{CC} $+0.05$	V
DC Common-Mode Error	6	Common Mode Voltage GND to $V_{CC/2}$		$\pm 1/16$	$\pm 1/4$		$\pm 1/16$	$\pm 1/4$	LSB
AC Common-Mode Error	6	Comon Mode Voltage GND to $V_{CC/2}$, 0 to 50kHz			$\pm 1/4$			$\pm 1/4$	LSB
DC Power Supply Sensitivity	6	$V_{CC} = 5V \pm 10\%$ - $V_{REF} \leq V_{CC} + 0.1V$		$\pm 1/32$	$\pm 1/4$		$\pm 1/32$	$\pm 1/4$	LSB
AC Power Supply Sensitivity	6	$100mV_{P-P}$, 25kHz sine on V_{CC}			$\pm 1/4$			$\pm 1/4$	LSB
Change in Zero Error from $V_{CC} = 5V$ to Internal Zener Operation	6	15mA into V+ V_{CC} = N.C. $V_{REF} = 5V$		$\pm 1/2$			$\pm 1/2$		LSB
V_Z, Internal Diode Regulated Breakdown (at V+)		15mA into V+		6.9			6.9		V
V+ Input Resistance	5		20	35		20	35		kΩ
I_{Off}, Off Channel Leakage Current	5, 10	On Channel = V_{CC} Off Channel = 0V	-1			-1			µA
		On Channel = 0V Off Channel = V_{CC}			+1			+1	µA
I_{On}, On Channel Leakage Current	5, 10	On Channel = 0V Off Channel = V_{CC}	-1			-1			µA
		On Channel = V_{CC} Off Channel = 0V			+1			+1	µA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{REF} = 5V \pm 10\%$, and $f_{CLK} = 1.333MHz$

PARAMETER	NOTES	CONDITIONS	ML2281B, ML2282B ML2284B, ML2288B			ML2281C, ML2282C ML2284C, ML2288C			UNITS
			MIN	TYP NOTE 4	MAX	MIN	TYP NOTE 4	MAX	
DIGITAL AND DC CHARACTERISTICS									
$V_{IN(1)}$, Logical "1" Input Voltage	5		2.0			2.0			V
$V_{IN(0)}$, Logical "0" Input Voltage	5				0.8			0.8	V
$I_{IN(1)}$, Logical "1" Input Current	5	$V_{IN} = V_{CC}$			1			1	μA
$I_{IN(0)}$, Logical "0" Input Current	5	$V_{IN} = 0V$	−1			−1			μA
$V_{OUT(1)}$, Logical "1" Output Voltage	5	$I_{OUT} = -2mA$	4.0			4 0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	5	$I_{OUT} = 2mA$			0.4			0.4	V
I_{OUT}, Hi-Z Output Current	5	$V_{OUT} = 0V$ $V_{OUT} = V_{CC}$	−1		 1	−1		 1	μA μA
I_{SOURCE}, Output Source Current	5	$V_{OUT} = 0V$	−6.5			−6.5			mA
I_{SINK}, Output Sink Current	5	$V_{OUT} = V_{CC}$			8.0			8.0	mA
I_{CC}, Supply Current ML2281, ML2284, ML2288	5			1.3	2.5		1.3	2.5	mA
ML2282	5	Includes Ladder Current		1.8	3 5		1.8	3.5	mA

PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 4	MAX	LIMIT UNITS
AC ELECTRICAL CHARACTERISTICS						
f_{CLK}, Clock Frequency	5		10		1333	kHz
t_{ACQ}, Sample-and-Hold Acquistion				1/2		$1/f_{CLK}$
t_C, Conversion Time		Not including MUX Addressing Time		8		$1/f_{CLK}$
SNR, Signal to Noise Ratio ML2281	12	$V_{IN} = 40kHz$, 5V Sine. $f_{CLK} = 1.333MHz$ ($f_{SAMPLING} \cong 120kHz$). Noise is Sum of All Nonfundamental Components up to 1/2 of $f_{SAMPLING}$		47		dB
THD, Total Harmonic Distortion ML2281	12	$V_{IN} = 40kHz$, 5V Sine. $f_{CLK} = 1.333MHz$ ($f_{SAMPLING} \cong 120kHz$). THD is Sum of 2, 3, 4, 5 Harmonics Relative to Fundamental		−60		dB

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{REF} = 5V \pm 10\%$, and $f_{CLK} = 1.333MHz$

PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 4	MAX	LIMIT UNITS
AC ELECTRICAL CHARACTERISTICS (Continued)						
IMD, Intermodulation Distortion ML2281	12	$V_{IN} = f_A + f_B$. $f_A = 40kHz$, 2.5V Sine. $f_B = 39.8kHz$, 2.5V Sine, $f_{CLK} = 1.333MHz$ ($f_{SAMPLING} \cong 120kHz$). IMD is $(f_A + f_B)$, $(f_A - f_B)$, $(2f_A + f_B)$, $(2f_A - f_B)$, $(f_A + 2f_B)$, $(f_A - 2f_B)$ Relative to Fundamental		−60		dB
Clock Duty Cycle	5, 11		40		60	%
t_{SET-UP}, $\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge	5		130			ns
t_{HOLD}, Data Input Valid after CLK Rising Edge	5		80			ns
t_{pd1}, t_{pd0} — CLK Falling Edge to Output Data Valid	5, 13	$C_L = 100pF$ Data MSB First Data LSB First		90 50	200 110	ns ns
t_{1H}, t_{0H}, — Rising Edge of $\overline{CS}$ to Data Output and SARS Hi-Z	6	$C_L = 10pF$, $R_L = 10k$ (see High Impedance Test Circuits)		40	90	ns
	5	$C_L = 100pF$, $R_L = 2k$		80	160	ns
C_{IN}, Capacitance of Logic Input				5		pF
C_{OUT}, Capacitance of Logic Outputs				5		pF

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < GND$ or $V_{IN} > V_{CC}$) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: −55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. 0°C to 70°C and −40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Total unadjusted error includes offset, full-scale, linearity, multiplexer and sample-and-hold errors.

Note 8: Cannot be tested for ML2282.

Note 9: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater then the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct-especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 10: Leakage current is measured with the clock not switching.

Note 11: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum, time the clock is high or the minimum time the clock is low must be at least 300ns. The maximum time the clock can be high or low is 60μs.

Note 12: Because of multiplexer addressing, test conditions for the ML2282 would be $V_{IN} = 34kHz$, 5V sine ($f_{SAMPLING} \approx 102kHz$); ML2284 $V_{IN} = 32kHz$, 5V sine ($f_{SAMPLING} \approx 95kHz$); ML2288 $V_{IN} = 30kHz$, 5V sine ($f_{SAMPLING} \approx 89kHz$).

Note 13: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

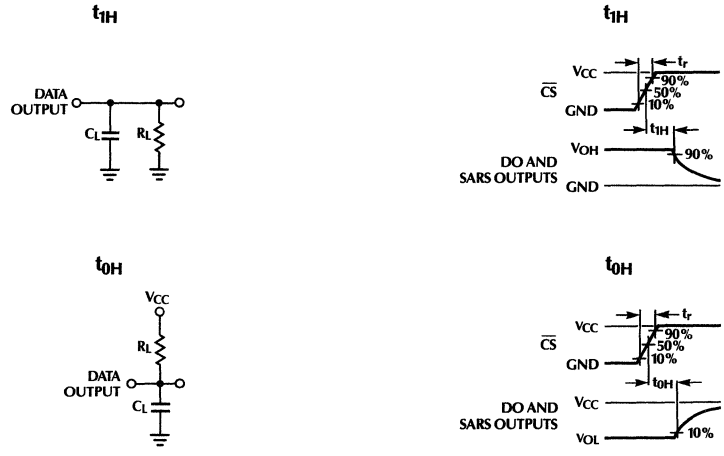


Figure 1. High Impedance Test Circuits and Waveforms

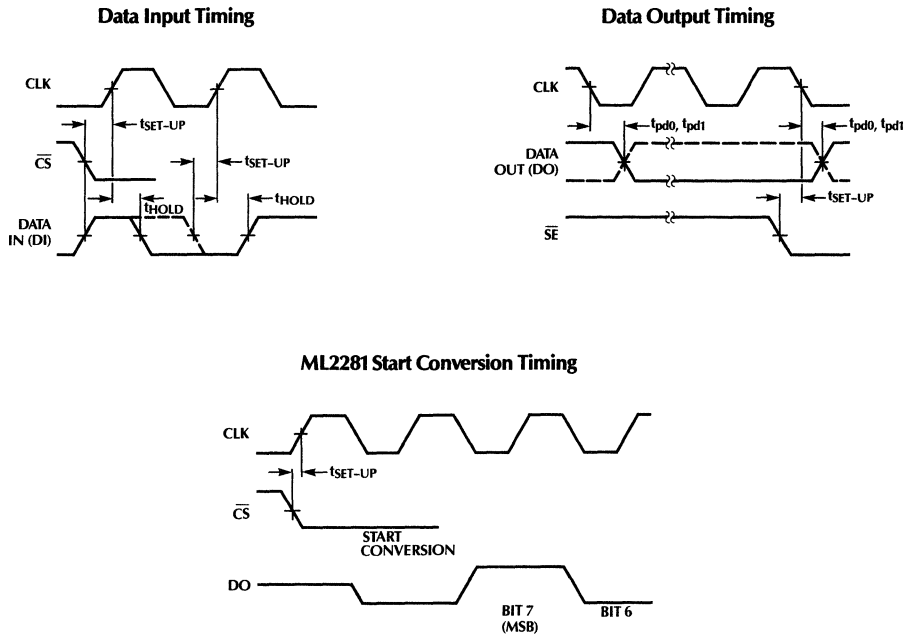
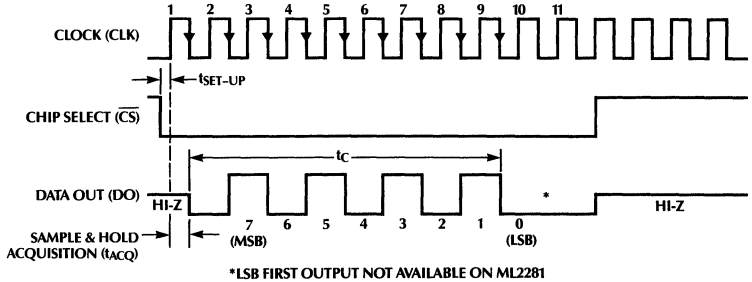


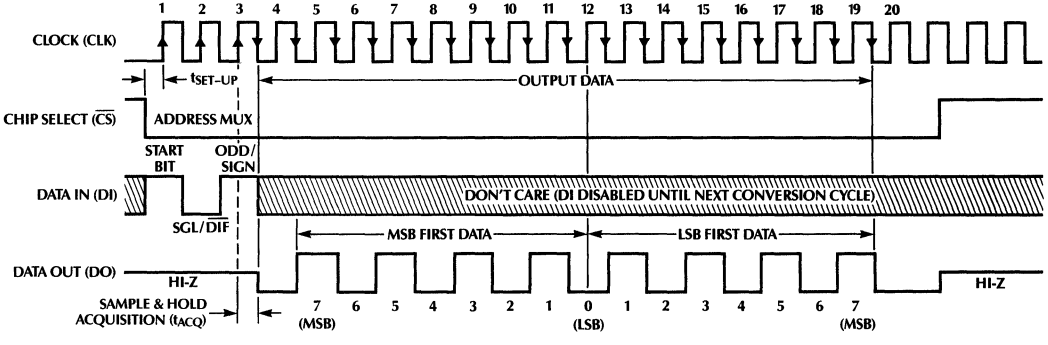
Figure 2. Timing Diagrams

ML2281 Timing



*LSB FIRST OUTPUT NOT AVAILABLE ON ML2281

ML2282 Timing



ML2284 Timing

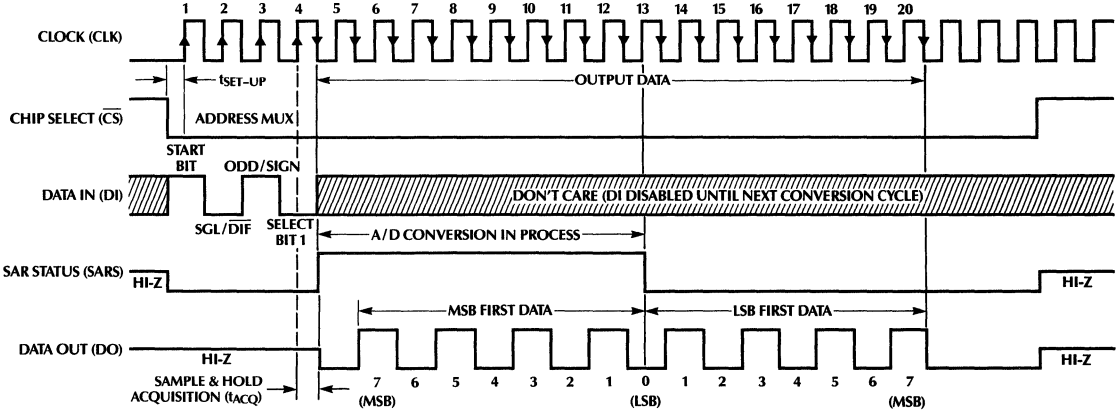


Figure 2. Timing Diagrams (Continued)

ML2288 Timing

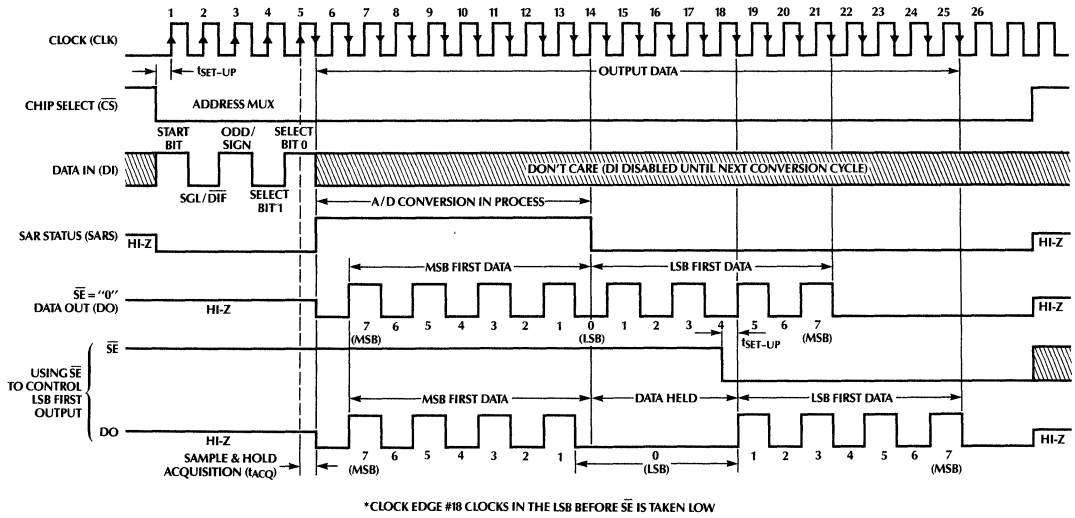


Figure 2. Timing Diagrams (Continued)

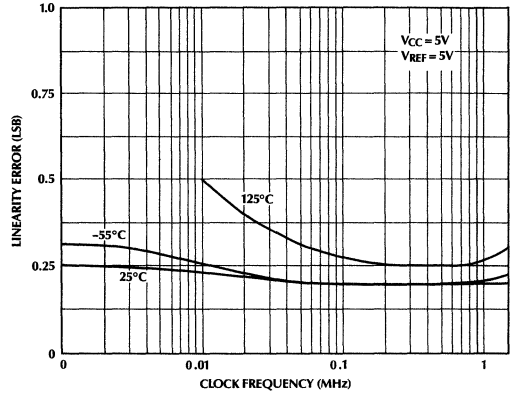


Figure 3. Linearity Error vs f_{CLK}

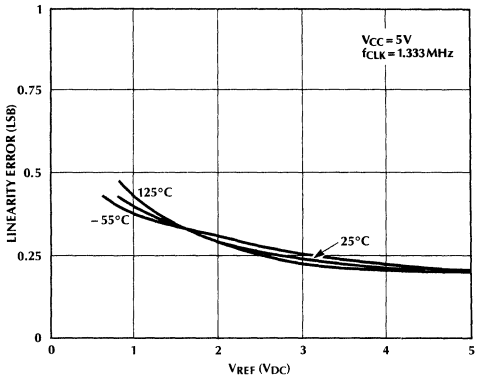


Figure 4. Linearity Error vs V_{REF} Voltage

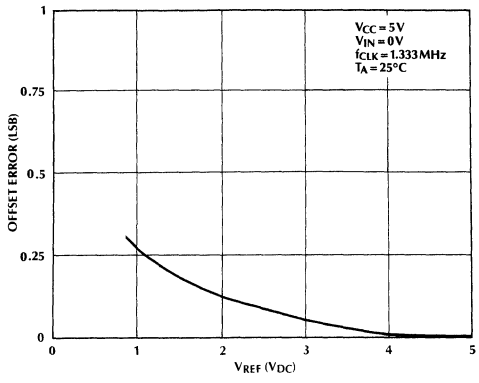
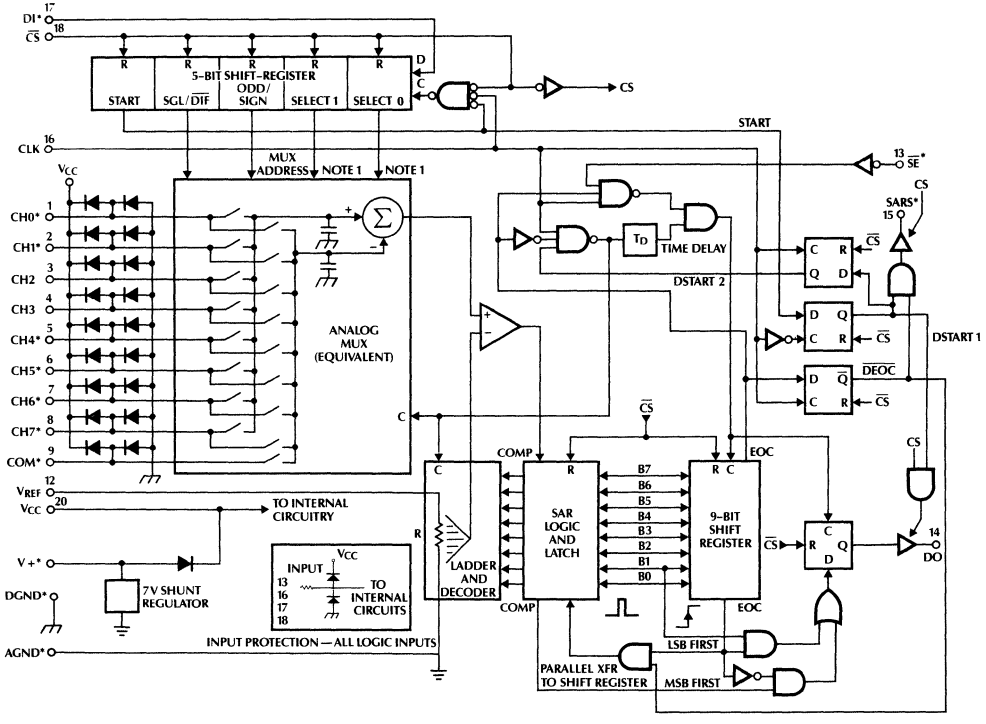


Figure 5. Unadjusted Offset Error vs V_{REF} Voltage

2



*SOME OF THESE FUNCTIONS/PINS ARE NOT AVAILABLE WITH OTHER OPTIONS.
NOTE 1: FOR THE ML2284 DI IS INPUT DIRECTLY TO THE D INPUT OF SELECT 1. SELECT 0 IS FORCED TO A "1". FOR THE ML2282, DI IS INPUT DIRECTLY TO THE D INPUT OF ODD/SIGN. SELECT 0 IS FORCED TO A "1" AND SELECT 1 IS FORCED TO A "0".

Figure 6. ML2288 Functional Block Diagram

1.0 FUNCTIONAL DESCRIPTION

1.1 Multiplexer Addressing

The design of these converters utilizes a sample data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input, the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software configurable single ended, differential, or pseudo differential options. The pseudo differential option will convert the difference between the voltage at any analog input and a common terminal. One converter package can now accomodate ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single ended or differential. In the differential case, it also assigns the polarity of the analog channels. Differential inputs are restricted to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a different pair but channel 0 or channel 1 cannot act differentially with any other channel. In addition to selecting the differential mode, the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is illustrated by the MUX addressing codes shown in *Tables 1, 2, and 3*.

The MUX address is shifted into the converter via the DI input. Since the ML2281 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

The common input line on the ML2288 can be used as a pseudo differential input. In this mode, the voltage on the COM pin is treated as the "−" input for any of the other input channels. This voltage does not have to be analog ground; it can be any reference potential which is common to all of the inputs. This feature is most useful in single supply applications where the analog circuitry may be biased at a potential other than ground and the output signals are all referred to this potential.

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 7* illustrates these different input modes.

Table 1. ML2288 MUX Addressing 8 Single-Ended or 4 Differential Channels

Single-Ended MUX Mode

MUX Address				Analog Single-Ended Channel #								
SGL/ DIF	ODD/ SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7	COM
1	0	0	0	+								−
1	0	0	1			+						−
1	0	1	0					+				−
1	0	1	1							+		−
1	1	0	0		+							−
1	1	0	1				+					−
1	1	1	0						+			−
1	1	1	1								+	−

Differential MUX Mode

MUX Address				Analog Differential Channel-Pair #							
				0		1		2		3	
SGL/ DIF	ODD/ SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7
0	0	0	0	+	−						
0	0	0	1			+	−				
0	0	1	0					+	−		
0	0	1	1							+	−
0	1	0	0	−	+						
0	1	0	1			−	+				
0	1	1	0					−	+		
0	1	1	1							−	+

Table 2. ML2284 MUX Addressing 4 Single-Ended or 2 Differential Channel

Single-Ended MUX Mode

MUX Address			Channel #			
SGL/ DIF	ODD/ SIGN	SELECT 1	0	1	2	3
1	0	0	+			
1	0	1			+	
1	1	0		+		
1	1	1				+

COM is internally tied to A GND

Differential MUX Mode

MUX Address			Channel #			
SGL/ DIF	ODD/ SIGN	SELECT 1	0	1	2	3
0	0	0	+	−		
0	0	1			+	−
0	1	0	−	+		
0	1	1			−	+

Table 3. ML2282 MUX Addressing 2 Single-Ended or 1 Differential Channel

Single-Ended MUX Mode

MUX Address		Channel #	
SGL/$\overline{DIF}$	ODD/SIGN	0	1
1	0	+	
1	1		+

COM is internally tied to GND

Differential MUX Mode

MUX Address		Channel #	
SGL/$\overline{DIF}$	ODD/SIGN	0	1
0	0	+	−
0	1	−	+

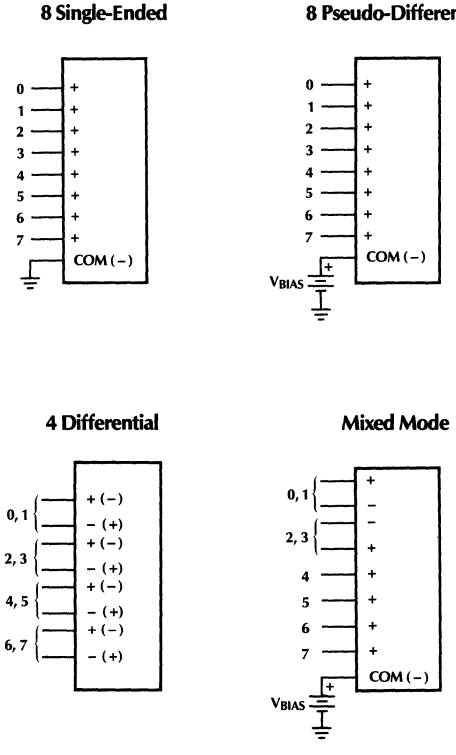


Figure 7. Analog Input Multiplexer Functional Options for ML2288

1.2 Digital Interface

The block diagram and timing diagrams in *Figures 2-5* illustrate how a conversion sequence is performed.

A conversion is initiated when $\overline{CS}$ is pulsed low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

A clock is applied to the CLK input. On each rising edge of the clock, the data on DI is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on the DI input (all leading edge zeros are ignored). After the start bit, the device clocks in the next 2 to 4 bits for the MUX assignment word.

When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of ½ clock period is used for sample & hold settling through the selected MUX channels. The SAR status output goes high at this time to signal that a conversion is now in progress and the DI input is ignored.

The DO output comes out of High impedance and provides a leading zero for this one clock period.

When the conversion begins, the output of the comparator, which indicates whether the analog input is greater than or less than each successive voltage from the internal DAC, appears at the DO output on each falling edge of the clock. This data is the result of the conversion being shifted out (with MSB coming first) and can be read by external logic or μP immediately.

After 8 clock periods, the conversion is completed. The SAR status line returns low to indicate this ½ clock cycle later.

The serial data is always shifted out MSB first during the conversion. After the conversion has been completed, the data can be shifted out a second time with LSB first, depending on level of $\overline{SE}$ input. For the case of ML2288, if $\overline{SE}$=1, the data is shifted out MSB first during the conversion only. If $\overline{SE}$ is brought low before the end of conversion (which is signalled by the high to low transition of SARS), the data is shifted out again immediately after the end of conversion; this time LSB first. If $\overline{SE}$ is brought low after end of conversion, the LSB first data is shifted out on falling edges of clock after $\overline{SE}$ goes low. For ML2282 and 2284, $\overline{SE}$ is internally tied low, so data is shifted out MSB first, then shifted out a second time LSB first at end of conversion. For ML2281, $\overline{SE}$ is internally tied high, so data is shifted out only once MSB first.

All internal registers are cleared when the $\overline{CS}$ input is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI input and DO output can be tied together and controlled through a bidirectional μP I/O bit with one connection. This is possible because the DI input is only latched in during the MUX addressing interval while the DO output is still in the high impedance state.

1.3 Reference

The voltage applied to the reference input to these converters defines the voltage span of the analog input (the difference between V_{IN}max and V_{IN}min) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance, typically 10k. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small to allow direct conversion of inputs with less than 5 volts of voltage span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter.

1.4 Analog Inputs and Sample/Hold

An important feature of the ML2281 family of devices is that they can be located at the source of the analog signal and then communicate with a controlling µP with just a few wires. This avoids bussing the analog inputs long distances and thus reduces noise pickup on these analog lines. However, in some cases, the analog inputs have a large common mode voltage or even some noise present along with the valid analog signal.

The differential input of these converters reduces the effects of common mode input noise. Thus, if a common mode voltage is present on both "+" and "−" inputs, such as 60Hz, the converter will reject this common mode voltage since it only converts the difference between "+" and "−" inputs.

The ML2281 family have a true sample and hold circuit which samples both "+" and "−" inputs simultaneously. This simultaneous sampling with a true S/H will give common mode rejection and AC linearity performance that is superior to devices where the two input terminals are not sampled at the same instant and where true sample and hold capability does not exist. Thus, the ML2281 family of devices can reject AC common mode signals from DC-50kHz as well as maintain linearity for signals from DC-50kHz.

The signal at the analog input is sampled during the interval when the sampling switch is closed prior to conversion start. The sampling window (S/H acquisition time) is 1/2 CLK period wide and occurs 1/2 CLK period before DO goes from high impedance to active low state. When the sampling switch closes at the start of the S/H acquisition time, 8pF of capacitance is thrown onto the analog input. 1/2 CLK period later, the sampling switch is opened and the signal present at the analog input is stored. Any error on the analog input at the end of the S/H acquisition time will cause additional conversion error. Care should be taken to allow adequate charging or settling time from the source. If more charging or settling time is needed to reduce these analog input errors, a longer CLK period can be used.

The ML2281X family has improved latchup immunity. Each analog input has dual diodes to the supply rails, and a minimum of +/− 25mA (+/−100mA typically) can be injected into each analog input without causing latchup.

1.5 Dynamic Performance

Signal-to-Noise-Ratio

Signal-to-noise ratio (SNR) is the measured signal-to-noise at the output of the converter. The signal is the RMS magnitude of the fundamental. Noise is the RMS sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\,dB$$

where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92dB.

Harmonic Distortion

Harmonic distortion is the ratio of the RMS sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2281 Series is defined as

$$20 \log \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental and V_2, V_3, V_4, V_5 are the RMS amplitudes of the individual harmonics.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of $mf_A + nf_B$, where m, n = 0, 1, 2, 3,... . Intermodulation terms are those for which m or n is not equal to zero. The (IMD) intermodulation distortion specification includes the second order terms ($f_A + f_B$) and ($f_A - f_B$) and the third order terms ($2f_A + f_B$), ($2f_A - f_B$), ($f_A + 2f_B$) and ($f_A - 2f_B$) only.

1.6 Zero Error Adjustment

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, V_{IN}min is not ground, a zero offset can be done. The converter can be made to output 00000000 digital code for this minimum input voltage by biasing any $V_{IN}-$ input at this V_{IN} min value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}-$ input and applying a small magnitude positive voltage to the $V_{IN}+$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 00000000 to 00000001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF} = 5.000 V_{DC}$).

1.7 Full-Scale Adjustment

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input or V_{CC} for a digital output code which is just changing from 11111110 to 11111111.

1.8 Adjustment for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A $V_{IN}+$ voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00000000 to 00000001 code transition.

The full-scale adjustment should be made by forcing a voltage to the $V_{IN}+$ input which is given by:

$V_{IN}+$ fs adjust = Vmax − 1.5*[(Vmax-Vmin)/256]
where Vmax = high end of the analog input range
Vmin = low end (offset zero) of the analog range

The V_{REF} or V_{CC} voltage is then adjusted to provide a code change from 11111110 to 11111111.

1.9 Shunt Regulator

A unique feature of ML2288 and ML2284 is the inclusion of a shunt regulator connected from V+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode as shown in *Figure 8*. When the regulator is turned on, the V+ voltage is clamped at 11 V_{BE} set by the internal resistor ratio. The typical I-V curve of the shunt regulator is shown in *Figure 9*. It should be noted that before V+ voltage is high enough to turn on the shunt regulator (which occurs at about 5.5 V), 35 kΩ of resistance is observed between V+ and GND. When the shunt regulator is not used, V+ pin should be either left floating or tied to GND. The temperature coefficient of the regulator is −22 mV/°C.

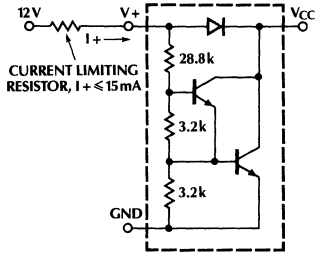


Figure 8. Shunt Regulator

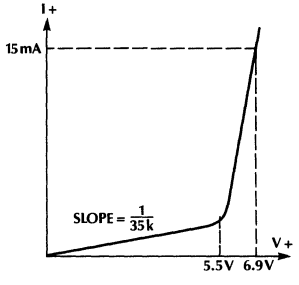
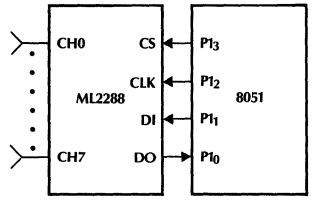


Figure 9. I-V Characteristic of the Shunt Regulator

2.0 APPLICATIONS

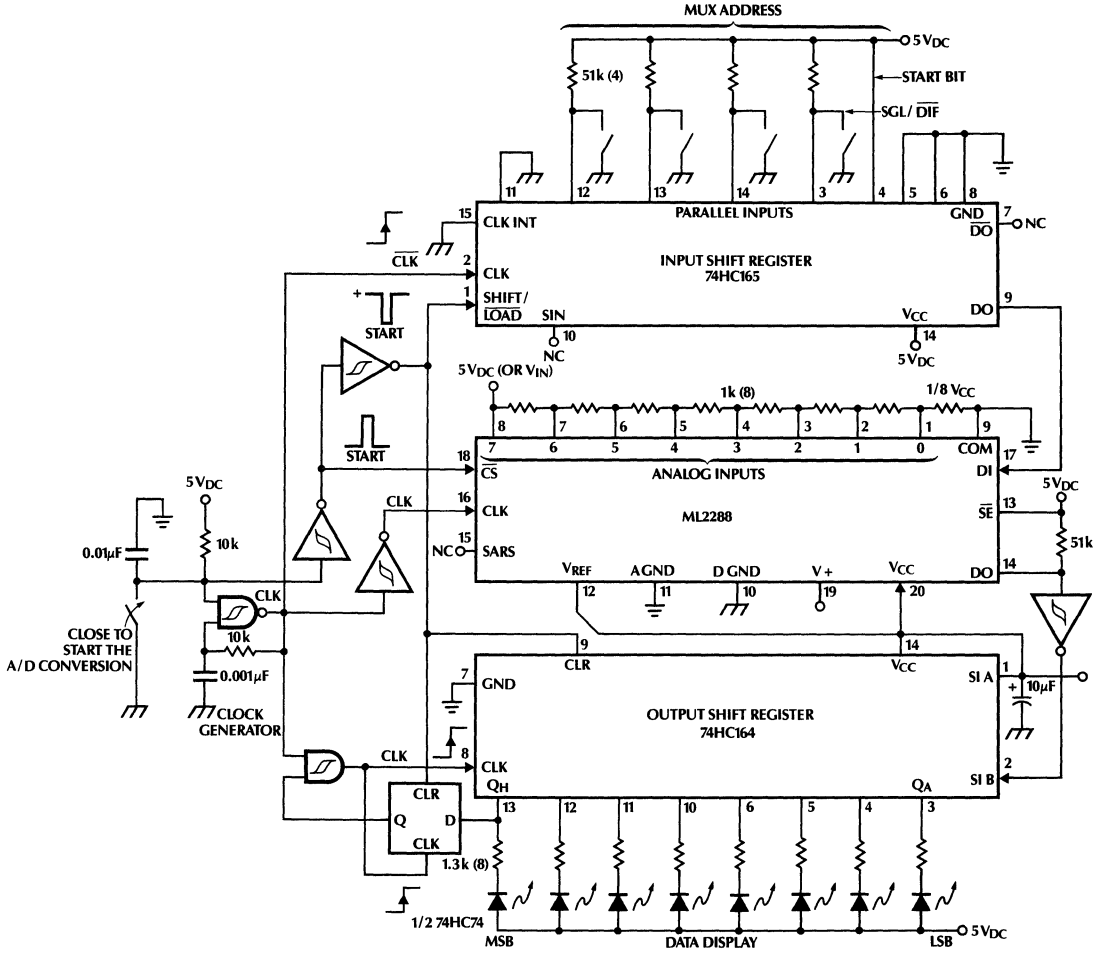
8051 Interface and Controlling Software



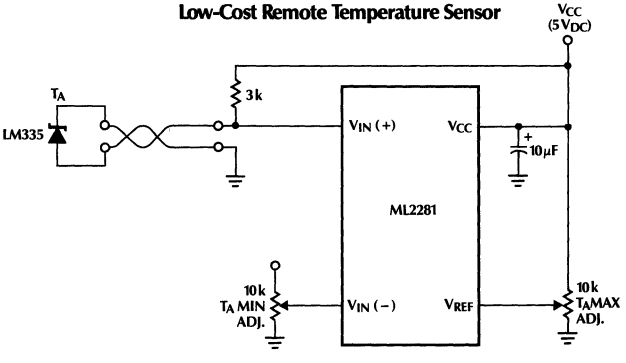
Mnemonic			Instruction
START	ANL	P1, #0F7H	;SELECT A/D (CS = 0)
	MOV	B, #5	;BIT COUNTER ← 5
	MOV	A, #ADDR	;A ← MUX BIT
LOOP 1:	RRC	A	;CY ← ADDRESS BIT
	JC	ONE	;TEST BIT ;BIT = 0
ZERO:	ANL	P1, #0FEH	;DI ← 0
	SJMP	CONT	;CONTINUE ;BIT = 1
ONE:	ORL	P1, #1	;D1 ← 1
CONT:	ACALL	PULSE	;PULSE SK 0 → 1 → 0
	DJNZ	B, LOOP 1	;CONTINUE UNTIL DONE
	ACALL	PULSE	;EXTRA CLOCK FOR SYNC
	MOV	B, #8	;BIT COUNTER ← 8
LOOP 2:	ACALL	PULSE	;PULSE SK 0 → 1 → 0
	MOV	A, P1	;CY ← DO
	RRC	A	
	RRC	A	
	MOV	A, C	;A ← RESULT
	RLC	A	;A(0) ← BIT AND SHIFT
	MOV	C, A	;C ← RESULT
	DJNZ	B, LOOP 2	;CONTINUE UNTIL DONE
RETI			
			;PULSE SUBROUTINE
PULSE:	ORL	P1, #04	;SK ← 1
	NOP		;DELAY
	ANL	P1, #0FBH	;SK ← 0
	RET		

APPLICATIONS (Continued)

ML2288 "Stand-Alone" or Evaluation Circuit

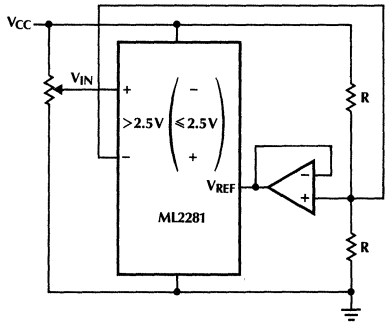


Low-Cost Remote Temperature Sensor



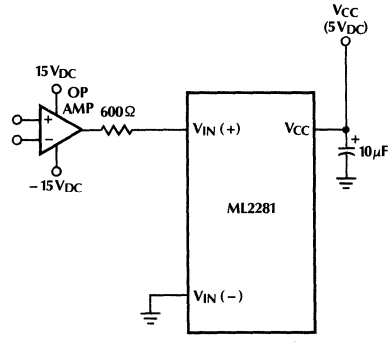
APPLICATIONS (Continued)

Obtaining 9-Bit Resolution



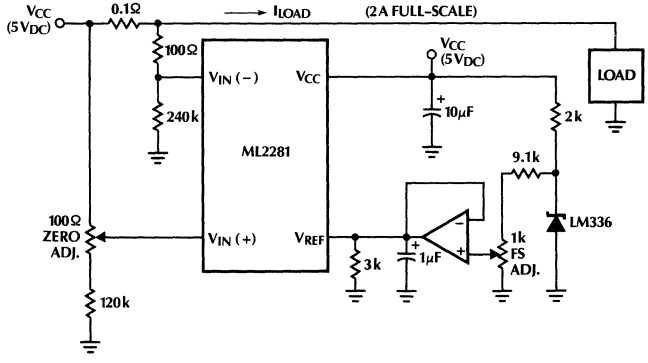
CONTROLLER PERFORMS A ROUTINE TO DETERMINE WHICH INPUT POLARITY PROVIDES A NON-ZERO OUTPUT CODE. THIS INFORMATION PROVIDES THE EXTRA BITS.

Protecting the Input

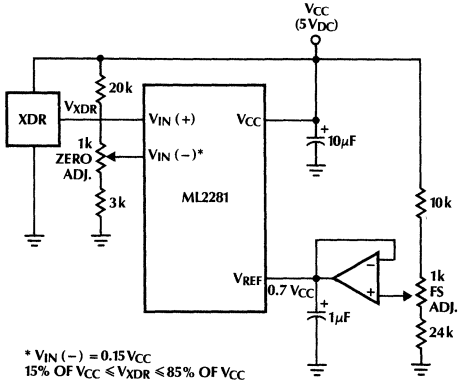


DIODE CLAMPING IS NOT NEEDED IF CURRENT IS LIMITED TO 25mA

Digitizing a Current Flow

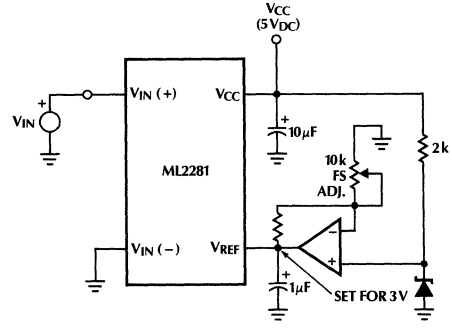


Operating with Ratiometric Transducers



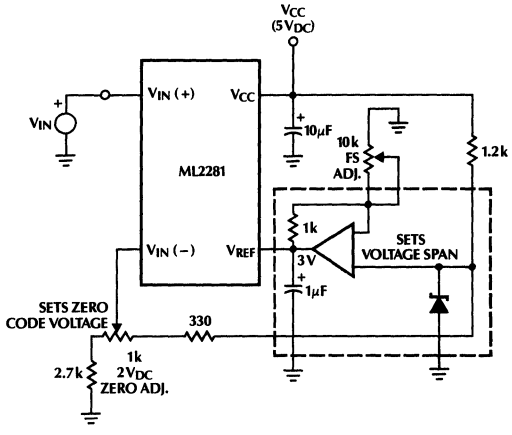
* $V_{IN}(-) = 0.15V_{CC}$
15% OF $V_{CC} \leq V_{XDR} \leq 85\%$ OF V_{CC}

Span Adjust: $0V \leq V_{IN} \leq 3V$

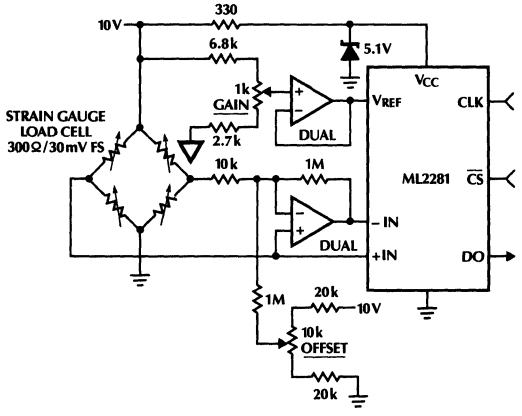


APPLICATIONS (Continued)

Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$

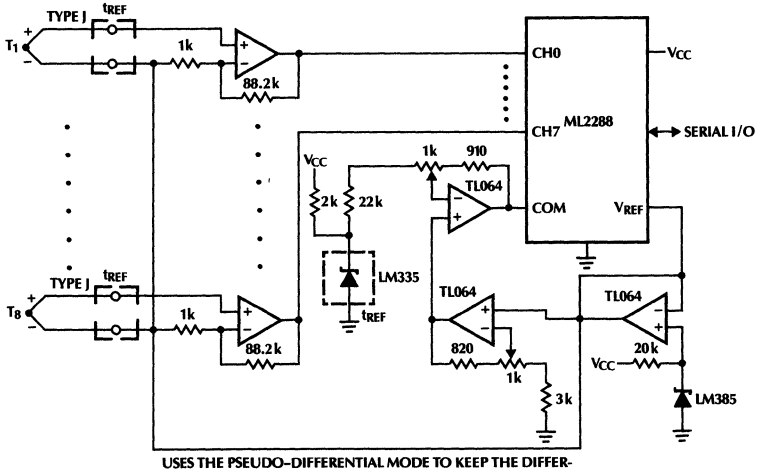


Digital Load Cell



- USES ONE MORE WIRE THAN LOAD CELL ITSELF
- TWO MINI-DIPs COULD BE MOUNTED INSIDE LOAD CELL FOR DIGITAL OUTPUT TRANSDUCER
- ELECTRONIC OFFSET AND GAIN TRIMS RELAX MECHANICAL SPECS FOR GAUGE FACTOR AND OFFSET
- LOW LEVEL CELL OUTPUT IS CONVERTED IMMEDIATELY FOR HIGH NOISE IMMUNITY

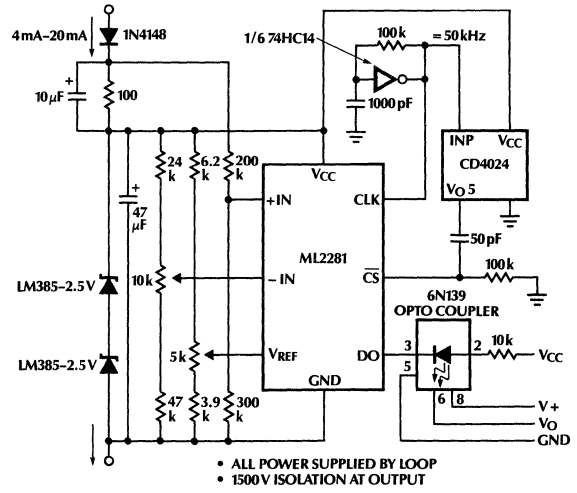
Convert 8 Thermocouples with only One Cold-Junction Compensator



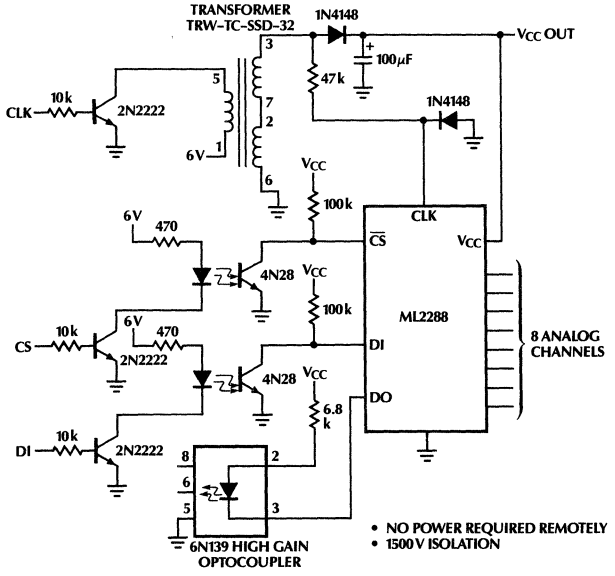
USES THE PSEUDO-DIFFERENTIAL MODE TO KEEP THE DIFFERENTIAL INPUTS CONSTANT WITH CHANGES IN REFERENCE TEMPERATURE (T_{REF}).

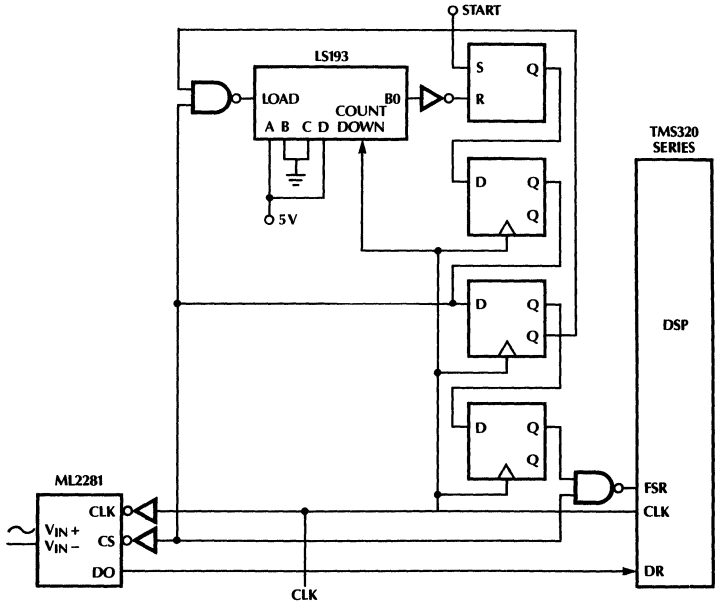
APPLICATIONS (Continued)

4mA–20mA Current Loop Converter

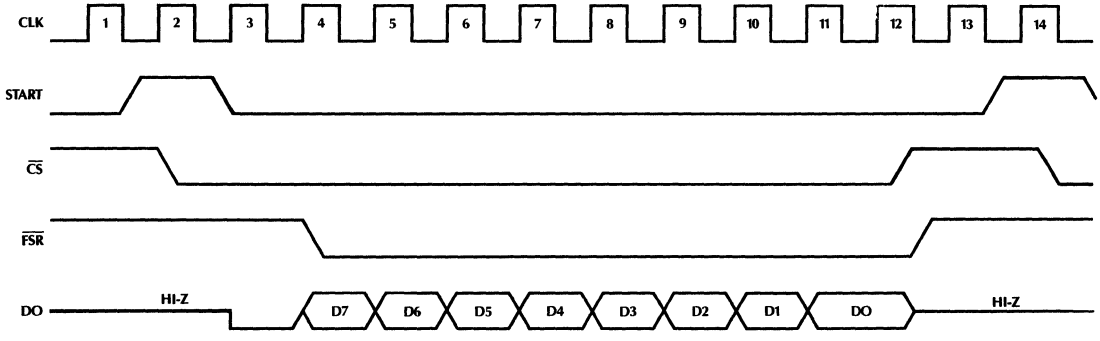


Isolated Data Converter





SAMPLING RATE 111kHz, DATA RATE 1.33MHz



Interfacing ML2281 to TMS320 Series

ORDERING INFORMATION

PART NUMBER	ALTERNATE PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
SINGLE ANALOG INPUT, 8-PIN PACKAGE				
ML2281BMJ	ADC0831BJ	±1/2 LSB	−55°C to +125°C	HERMETIC DIP (J08)
ML2281BIJ	ADC0831BCJ		−40°C to +85°C	HERMETIC DIP (J08)
ML2281BCP	ADC0831BCN		0° to +70°C	MOLDED DIP (P08)
ML2281CIJ	ADC0831CCJ	±1LSB	−40°C to +85°C	HERMETIC DIP (J08)
ML2281CCP	ADC0831CCN		0°C to +70°C	MOLDED DIP (P08)
TWO ANALOG INPUTS, 8-PIN PACKAGE				
ML2282BMJ	ADC0832BJ	±1/2 LSB	−55°C to +125°C	HERMETIC DIP (J08)
ML2282BIJ	ADC0832BCJ		−40°C to +85°C	HERMETIC DIP (J08)
ML2282BCP	ADC0832BCN		0°C to +70°C	MOLDED DIP (P08)
ML2282CIJ	ADC0832CCJ	±1LSB	−40°C to +85°C	HERMETIC DIP (J08)
ML2282CCP	ADC0832CCN		0°C to +70°C	MOLDED DIP (P08)
FOUR ANALOG INPUTS, 14-PIN PACKAGE				
ML2284BMJ	ADC0834BJ	±1/2 LSB	−55°C to +125°C	HERMETIC DIP (J14)
ML2284BIJ	ADC0834BCJ		−40°C to +85°C	HERMETIC DIP (J14)
ML2284BCP	ADC0834BCN		0° to +70°C	MOLDED DIP (P14)
ML2284CIJ	ADC0834CCJ	±1LSB	−40°C to +85°C	HERMETIC DIP (J14)
ML2284CCP	ADC0834CCN		0°C to +70°C	MOLDED DIP (P14)
EIGHT ANALOG INPUTS, 20-PIN PACKAGE				
ML2288BMJ	ADC0838BJ	±1/2 LSB	−55°C to +85°C	HERMETIC DIP (J20)
ML2288BIJ	ADC0838BCJ		−40°C to +85°C	HERMETIC DIP (J20)
ML2288BCP	ADC0838BCN		0°C to +70°C	MOLDED DIP (P20)
ML2288BCQ	ADC0838BCV		0°C to +70°C	MOLDED PCC (Q20)
ML2288CIJ	ADC0838CCJ	±1LSB	−40°C to +85°C	HERMETIC DIP (J20)
ML2288CCP	ADC0838CCN		0°C to +70°C	MOLDED DIP (P20)
ML2288CCQ	ADC0838CCV		0°C to +70°C	MOLDED PCC (Q20)

Selectable Dual 3V/3.3V/5V 8-Bit DACs

GENERAL DESCRIPTION

The ML2330 Selectable Dual 3V/3.3V/5V 8-bit DACs are dual voltage-output digital-to-analog converters which can be independently programmed or powered down to conserve power. The devices are intended for use in portable or low power 3V systems where space is critical.

Programming access to the DACs is provided over a high speed (10Mb/s), 3-wire serial interface which is compatible to the SPI™ and Microwire™ In addition to independent programming of the DAC output voltages, each device may be powered down independent of the other DAC to conserve power. Each DAC draws 2mA of maximum quiescent current when operating, and typically less than 1µA when powered down.

The device comes in an 8-pin SOIC package and in a special Extended Commercial temperature range (–20°C to 70°C).

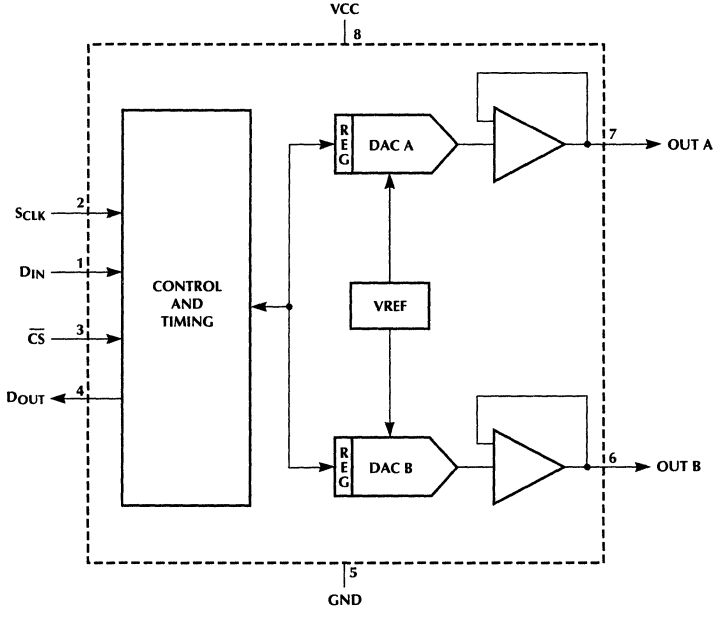
FEATURES

- 3V ±10%, 3.3 ±10% or 5V ±10% operation
- Low supply current (4mA max)
- Individual and full power down (down to 1µA)
- 10Mb/s three-wire serial interface, compatible to SPI and Microwire
- 8-pin SOIC packages
- Available in Extended Commercial Temperature range (–20°C to 70°C)

SPI is a trademark of Motorola.
Microwire is a trademark of National Semiconductor.

2

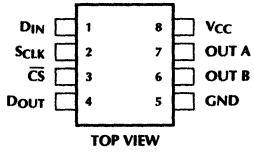
BLOCK DIAGRAM



PIN CONFIGURATION

ML2330

8-Pin SOIC (S08N)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	D_{IN}	Data In
2	S_{CLK}	Serial Clock
3	$\overline{CS}$	Chip Select
4	D_{OUT}	Data Out
5	GND	Ground
6	OUT B	Output of DAC B
7	OUT A	Output of DAC A
8	V_{CC}	Positive Supply

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6.0V
GND ..... –0.3V to V_{CC} + 0.3V
Logic Inputs ..... –0.3V to V_{CC} + 0.3V
Input Current per Pin ..... ±25mA
Storage Temperature ..... –65°C to 150°C
Package Dissipation at T_A = 25°C 750mW
Lead Temperature (Soldering 10 sec.)
SOIC ..... 150°C

OPERATING CONDITIONS

Supply Voltage (V_{CC}) ..... 2.7V to 5.5V
Temperature Range ..... –20°C < T_A < 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 3.3V ±10%, F_{CLK} = 10MHz R_L = 1K, C_L = 100pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Converter						
Resolution			8			bits
Integral Linearity Error	ILE				±1	LSB
Differential Linearity Error	DLE				±1	LSB
Offset Error			15	20	25	mV
Gain Error					±3	%FS
Analog Output						
Output Drive Current	I_{OUTPP}	@00 & FF	2			mA
Power Supply Rejection Ratio	PSRR	@00 & FF	–40			dB
Digital and DC						
Logic Input Low	V_{IL}				0.5	V
Logic Input High	V_{IH}		2.0			V
Logic Input Low Current	I_{IL}	V_{IN} = GND	–1			µA
Logic Input High Current	I_{IH}	V_{IN} = VCC			1	µA
Logic Output Low	V_{OL}	I = 3.2mA			0.4	V
Logic Output High	V_{OH}	I = 0.4mA	2.4			V
Supply Current	I_{CC}	R_L = ∞		2.5	4	mA
Power Down Current		V_{CC} = 3V			1	µA
		V_{CC} = 5V			5	µA
AC Performance						
Settling Time	t_s	±1/2 LSB		5	10	µs
Slew Rate				1.4		V/µs
Crosstalk			60			dB

TIMING CHARACTERISTICS

VCC = 3.3V ±10%, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Converter						
$\overline{CS}$ Fall to S_{CLK} Setup Time	t_{CSS}		20			ns
S_{CLK} Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		50			ns
D_{IN} to S_{CLK} Rise Setup Time	t_{DS}		20			ns
D_{IN} to S_{CLK} Rise Hold Time	t_{DH}		20			ns
S_{CLK} Frequency	f_{CLK}			10		MHz
S_{CLK} Duty Cycle			40		60	%
S_{CLK} to D_{OUT} Valid	t_{DO}			30		ns

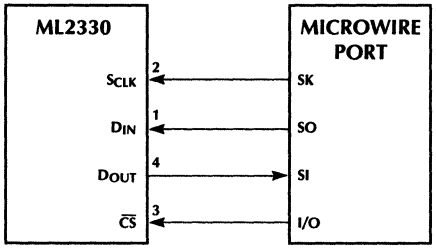


Figure 1A. Connections for Microwire.

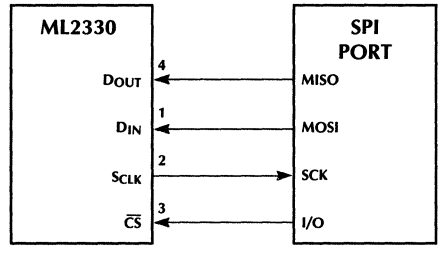
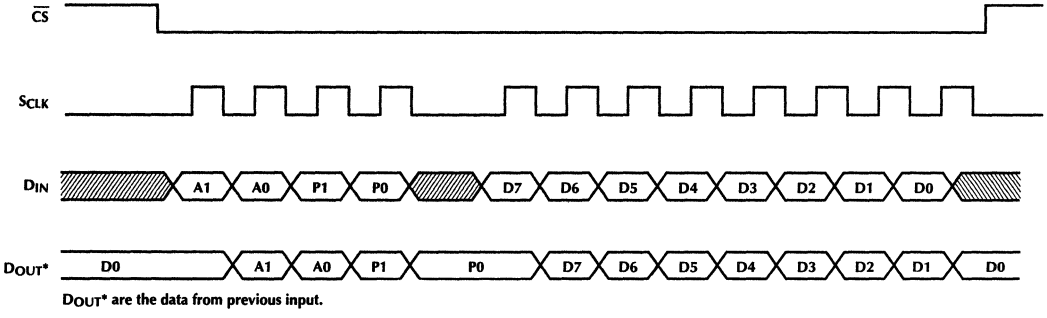


Figure 1B. Connections for SPI.



DOUT* are the data from previous input.

Figure 1C. Interface Timing

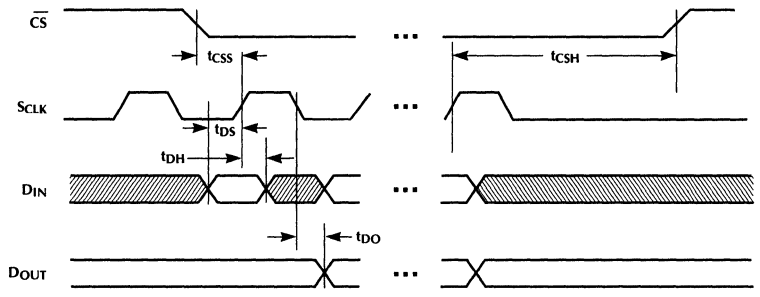


Figure 2. Detail Interface Timing

FUNCTIONAL DESCRIPTION

SERIAL INTERFACE

The ML2330 communicates with microprocessors through a synchronous, full-duplex, 3-wire interface (figure 1A & B). At power on, the control registers are cleared and both DACs have high impedance outputs. Data timing shown in figure 1C is sent MSB first and can be transmitted in one 4-bit and one 8-bit packet or in one 12-bit word. If a 16-bit control word is used, the first four bits are ignored. The serial clock (S_{CLK}) synchronizes the data transfer. Data is transmitted and received simultaneously. Figure 2 shows detailed serial interface timing. Note that the clock should be low between updates. D_{OUT} does not go into a high impedance state if the clock idles or $\overline{CS}$ is high.

Serial data is clocked into the data registers in MSB-first format, with the address and configuration information preceding the actual DAC data. Data is sampled on the S_{CLK}'s rising edge while $\overline{CS}$ is low. Data at D_{OUT} is clocked out 12.5 clock cycles later, on the S_{CLK}'s falling edge.

Chip select ($\overline{CS}$) must be low to enable the read or write operation. If $\overline{CS}$ is high, the interface is disabled and D_{OUT} remains unchanged. $\overline{CS}$ must go low at least 10ns before the first clock pulse to properly clock in the first bit. With $\overline{CS}$ low, data is clocked into the ML2330's internal shift register on the rising edge of the external serial clock. S_{CLK} can be driven at rates up to 10MHz.

SERIAL INPUT DATA FORMAT AND CONFIGURATION CODES

The 12-bit serial input format shown in Figure 3 comprises two DAC address bits (A1, A0), two power down control bits (P1, P0) and eight bits of data (D7 . . . D0).

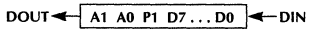


Figure 3. Serial Input Format

The 4-bit address/control code configures the DAC as shown in Table 3.

A1	A0	Function
0	0	No operation
0	1	Select control bits and DAC A
1	0	Select control bits and DAC B
1	1	Select control bits and both DACs

Table 3.1 Address Selection

P1	P0	Function
0	0	Normal
0	1	Power down DAC A
1	0	Power down DAC B
1	1	Power down entire chip

Table 3.2 Power Down Selection

DAC OPERATION

The DACs are implemented using an array of equal current sources that are decoded linearly for the four most significant bits to improve differential linearity and to reduce output glitch around major carries. A voltage difference between on-board bandgap reference voltage and GND is converted to a reference current using an internal resistor to set up the appropriate current level in the DACs. The DACs output current is then converted to a voltage output by an output buffer and a resistive network. The matching among the on-chip resistors preserves the gain accuracy between these conversions.

VOLTAGE REFERENCE

A bandgap voltage reference is incorporated on the ML2330. It is trimmed for Zero Temperature Coefficient at 25°C to minimize output voltage drift over the specified operating temperature range.

OUTPUT BUFFER AND GAIN SETTING

The output buffer converts the DAC output current to a voltage output using a resistive network. The outputs can swing from GND +0.02V to either 2.02V (3V) or 4.02V (5V). The DAC transfer function is:

$$V_{OUT} = \frac{K \times DATA}{256} + 0.02$$

where K = 2 if V_{CC} = 3V and K = 4 if V_{CC} = 5V

In the 3V operation, the amplifier outputs will settle to 1/2LSB in 10µs when loads are greater than 1KΩ (2KΩ for 5V operation) and capacitive loads smaller than 100pF.

VCC SUPPLY RANGE

ML2330 can be operated at 3V ±10% (ML2330-2), 3.3V ±10% (ML2330-3) or 5V ±10% (ML2330-5).

POWER DOWN MODE

There are three power down modes in the ML2330. By clearing the control bits P1-P0 (Table 3.2), the entire chip will be powered down with a supply current less than 5µA. Individual DACs can also be powered down to save power.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2330ES	–20°C to +70°C	8-PIN SOIC (S08N)

ML2340, ML2350

Single Supply, Programmable 8-Bit D/A Converters

GENERAL DESCRIPTION

The ML2340 and ML2350 are CMOS voltage output, 8-bit D/A converters with an internal voltage reference and a µP interface. These devices are designed to be powered by a single supply, although they can be powered from dual power supplies. The output voltage swings above zero scale (V_{ZS}) in the unipolar mode or around zero scale (V_{ZS}) in the bipolar mode, both with programmable gain. V_{ZS} can be set to any voltage from AGND to 2.25V below V_{CC}. The digital and analog grounds, DGND and AGND, are totally independent of each other. DGND can be set to any voltage from AGND to 4.5V below V_{CC} for easy interfacing to standard TTL and CMOS logic families.

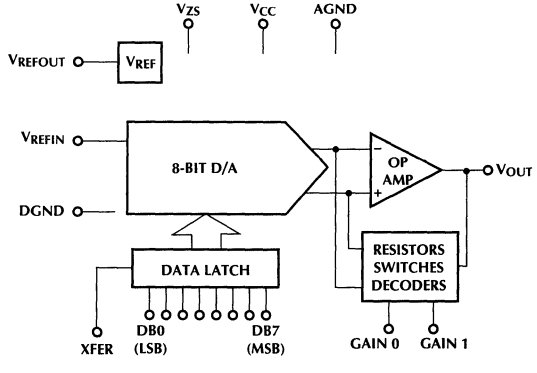
The high level of integration and versatility of the ML2340 and ML2350 makes them ideal for a wide range of applications in hard disk drives, automotive, telecom, and a variety of general purpose industrial. One specific intended application is controlling a hard disk voice coil.

The internal reference of the ML2340 provides a 2.25V or 4.50V output for use with A/D converters that use a single 5V ±10% power supply, while the ML2350 provide a 2.50V or 5.00V reference output.

FEATURES

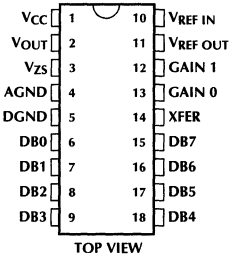
- Programmable output voltage gain settings of 2, 1, ½, ¼ provide 8-, 9-, 10-, or 11-bit effective resolution around zero
- AGND to V_{CC} output voltage swing
- Bipolar or unipolar output voltage
- 4.5V to 13.2V single supply or ±2.25V to ±6.5V dual-supply operation
- Transparent latch allows microprocessor interface with 30ns setup time
- Data flow through mode
- Voltage reference output
  - ML2340 ..... 2.25V or 4.50V
  - ML2350 ..... 2.50V or 5.00V
- Nonlinearity ..... ±¼ LSB or ±½ LSB
- Output voltage settling time over temperature and supply voltage tolerance
  - Within 1V of V_{CC} and AGND ..... 2.5µs max
  - Within 100mV of V_{CC} and AGND ..... 5µs max
- TTL and CMOS compatible digital inputs
- Low supply current (5V supply) ..... 5mA max
- 18-pin DIP or surface mount SOIC
- Operating temperature range of 0°C to +70°C, –40°C to +85°C, and –55°C to +125°C

BLOCK DIAGRAM



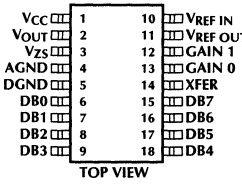
PIN CONNECTIONS

ML2340
ML2350
18-Pin DIP (P18)



TOP VIEW

ML2340
ML2350
18-Pin SOIC (S18W)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	V_{CC}	Positive supply.
2	V_{OUT}	Voltage output of the D/A converter. V_{OUT} is referenced to V_{ZS}.
3	V_{ZS}	Zero Scale Voltage. V_{OUT} is referenced to V_{ZS}. V_{ZS} is normally tied to AGND in the unipolar mode or to mid-supply in the bipolar mode. When the device is operated from a single power supply, V_{ZS} has a maximum current requirement of –300µA in the bipolar mode.
4	AGND	Analog ground.
5	DGND	Digital ground. This is the ground reference level for all digital inputs. The range is AGND < (V_{CC} – 4.5V). DGND is normally tied to system ground.
6	DB0	Data input — Bit 0 (LSB).
7	DB1	Data input — Bit 1.
8	DB2	Data input — Bit 2.
9	DB3	Data input — Bit 3.
10	DB4	Data input — Bit 4.
11	DB5	Data input — Bit 5.
12	DB6	Data input — Bit 6.
13	DB7	Data input — Bit 7 (MSB).
14	XFER	Transfer enable input. The data is transferred into the transparent latch at the high level of XFER.
15	GAIN 0	Digital gain setting input 0.
16	GAIN 1	Digital gain setting input 1.
17	$V_{REF\ OUT}$	Voltage reference output. $V_{REF\ OUT}$ is referenced to AGND. $V_{REF\ OUT}$ is set to 2.5V and 5.0V in a low-voltage and high-voltage operation, respectively for the ML2350; 2.25V and 4.5V for the ML2340.
18	$V_{REF\ IN}$	Voltage reference input. $V_{REF\ IN}$ is referenced to AGND.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage V_{CC} with Respect to AGND 14.2V
DGND ..... –0.3V to V_{CC} + 0.3V
V_{ZS}, $V_{REF\ IN}$ ..... –0.3V to V_{CC} + 0.3V
Logic Inputs ..... –0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Package Dissipation at T_A = 25°C (Board Mount) ... 875mW
Lead Temperature (Soldering 10 sec.)
Dual-In-Line Package (Molded) ..... 260°C
Dual-In-Line Package (Ceramic) ..... 300°C
Molded Small Outline IC Package
Vapor Phase (60 sec.) ..... 215°C
Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

(Note 1)

Supply Voltage, V_{CC} ..... 4.5V_{DC} to 13.2V_{DC}
Temperature Range (Note 3) ..... $T_{MIN} \le T_A \le T_{MAX}$
ML2340BMJ, ML2340CMJ
ML2350BMJ, ML2350CMJ ..... –55°C to +125°C
ML2340BIJ, ML2350BIJ ..... –40°C to +85°C
ML2340BCP, ML2340CCP
ML2350BCP, ML2350CCP
ML2340BCS, ML2340CCS
ML2350BCS, ML2350CCS ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} – AGND = 5V ±10% and 12V ±10%, $V_{REF\ IN}$ for ML2340 = 2.25V and 4.50V, for ML2350 $V_{REF\ IN}$ = 2.50V and 5.00V, V_{OUT} load is R_L = 1K and C_L = 100pF, V_{REF} load is R_L = 1K and C_L = 100pF and input control signals with $t_R = t_F \leq 20$ns.

PARAMETER	NOTES	CONDITIONS	ML2340XCX, ML2350XCX MIN	ML2340XCX, ML2350XCX TYP (NOTE 4)	ML2340XCX, ML2350XCX MAX	ML2340XIX, ML2350XMX ML2350XIX, ML2350XMX MIN	ML2340XIX, ML2350XMX ML2350XIX, ML2350XMX TYP (NOTE 4)	ML2340XIX, ML2350XMX ML2350XIX, ML2350XMX MAX	UNITS
Converter and Programmable Gain Amplifier									
Converter Resolution	5		8			8			Bits
Integral Linearity Error	5	GAIN = 2, 1, ½, or ¼							
ML2340BXX, ML2350BXX					±¼			±¼	LSB
ML2340CXX, ML2350CXX					±½			±½	LSB
Differential Linearity Error	5	GAIN = 2, 1, ½, or ¼							
ML2340BXX, ML2350BXX					±¼			±¼	LSB
ML2340CXX, ML2350CXX					±½			±½	LSB
Mode Select	5	V_{ZS} with respect to AGND							
Unipolar Output			0		1.0	0		1.0	V
Bipolar Output			1.50		V_{CC}–2.25	1.50		V_{CC}–2.25	V
Offset Error	5	Figure 1							
Unipolar Mode		GAIN = ¼, ½, 1			±10			±12	mV
		GAIN = 2			±20			±24	mV
Bipolar Mode	5	Figure 1							
		GAIN = ¼, ½, 1, 2			±10 plus ±2½ LSB			±10 plus ±2½ LSB	mV
Gain Error	5	Figure 1							
Unipolar Mode		GAIN = ¼, ½, 1, 2		±0.5	±2		±0.5	±2.5	%FS
Bipolar Mode		GAIN = ¼, ½, 1, 2		±0.5	±2		±0.5	±2.5	%FS
Reference									
$V_{REF\ OUT}$ Voltage	5								
ML2340BXX		$V_{CC} \leq 7.0V$ T_A = 25°C	2.23	2.25	2.27	2.23	2.25	2.27	V
		T_{MIN} to T_{MAX}	2.22		2.28	2.18		2.32	V
		$V_{CC} \geq 8.0V$ T_A = 25°C	4.48	4.50	4.52	4.48	4.50	4.52	V
		T_{MIN} to T_{MAX}	4.46		4.54	4.43		4.57	V
ML2340CXX		$V_{CC} \leq 7.0V$ T_A = 25°C	2.22	2.25	2.29	2.22	2.25	2.28	V
		T_{MIN} to T_{MAX}	2.20		2.30	2.18		2.32	V
		$V_{CC} \geq 8.0V$ T_A = 25°C	4.45	4.50	4.55	4.45	4.50	4.55	V
		T_{MIN} to T_{MAX}	4.40		4.60	4.35		4.65	V
ML2350BXX	5	$V_{CC} \leq 7.0V$ T_A = 25°C	2.48	2.50	2.52	2.48	2.50	2.52	V
		T_{MIN} to T_{MAX}	2.47		2.53	2.43		2.57	V
		$V_{CC} \geq 8.0V$ T_A = 25°C	4.98	5.00	5.02	4.98	5.00	5.02	V
		T_{MIN} to T_{MAX}	4.96		5.04	4.90		5.10	V
ML2350CXX		$V_{CC} \leq 7.0V$ T_A = 25°C	2.45	2.50	2.55	2.46	2.50	2.55	V
		T_{MIN} to T_{MAX}	2.44		2.58	2.42		2.59	V
		$V_{CC} \geq 8.0V$ T_A = 25°C	4.95	5.00	5.05	4.95	5.00	5.05	V
		T_{MIN} to T_{MAX}	4.90		5.10	4.85		5.15	V
Temperature Coefficient $V_{REF\ OUT}$				50			50		ppm/°C
V_{REF} Output Current	5		0.75		5	0.75		5	mA
$V_{REF\ OUT}$ Power Supply Rejection Ratio	5	100mV_{P-P}, 1kHz Sinewave on V_{CC}	–40	–60		–40	–60		dB

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	NOTES	CONDITIONS	ML2340XCX, ML2350XCX			ML2340XIX, ML2350XMX ML2350XIX, ML2350XMX			UNITS
			MIN	TYP (NOTE 4)	MAX	MIN	TYP (NOTE 4)	MAX	
$V_{REF\ IN}$ and V_{ZS}									
$V_{REF\ IN}$ Input Range	5	$V_{CC} \le 8.75V$ $V_{CC} \ge 8.75V$	AGND+2 AGND+2		V_{CC}–1.75 AGND+7	AGND+2 AGND+2		V_{CC}–1.75 AGND+7	V V
$V_{REF\ IN}$ DC Input Resistance	5		10			10			MΩ
V_{ZS} Voltage Range	5, 8	$V_{CC} \le 7.0V$	AGND		V_{CC}–2.25	AGND		V_{CC}–2.25	V
Analog Output									
V_{OUT} Output Swing Unipolar Mode	5, 8	R_L = 100K	AGND+ 0.01		V_{CC}–0.5	AGND+ 0.01		V_{CC}–0.5	V
		R_L = 1K	AGND+ 1.0		V_{CC}–1.0	AGND+ 1.0		V_{CC}–1.0	V
Bipolar Mode	5	R_L = 100K	AGND+ 0.1		V_{CC}–0.1	AGND+ 0.1		V_{CC}–0.1	V
		R_L = 1K	AGND + 1.0		V_{CC}–1.0	AGND + 1.0		V_{CC}–1.0	V
V_{OUT} Output Current	5	AGND+1V<V_{OUT}<V_{CC}–1V	–10		+10	–10		+10	mA
Power Supply Rejection Ratio		100mV_{P-P}, 1kHz sinewave on V_{CC}		–60			–60		dB
Digital and DC									
$V_{IN(0)}$ Logical "0" Input Voltage	5				0.8			0.8	V
$V_{IN(1)}$ Logical "1" Input Voltage	5		2.0			2.0			V
$I_{IN(0)}$ Logical "0" Input Current	5	V_{IN} = DGND	–1			–1			µA
$I_{IN(1)}$ Logical "1" Input Current	5	$V_{IN} = V_{CC}$			1			1	µA
Supply Current, Bipolar Mode									
I_{CC}, V_{CC} Current	5	V_{CC} = 5V ± 10%			5.3			5.3	mA
I_{AGND}, Analog Ground Current					–5.0			–5.0	mA
I_{VZS}, V_{ZS} Current				–90	–300		–90	–300	µA
I_{CC}, V_{CC} Current	5	V_{CC} = 12V ± 10%			9.3			9.3	mA
I_{AGND}, Analog Ground Current					–9.0			–9.0	mA
I_{VZS}, V_{ZS} Current				–90	–300		–90	–300	µA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	NOTES	CONDITIONS	ML2340XCX, ML2350XCX MIN	ML2340XCX, ML2350XCX TYP (NOTE 4)	ML2340XCX, ML2350XCX MAX	ML2340XIX, ML2350XMX ML2350XIX, ML2350XMX MIN	ML2340XIX, ML2350XMX ML2350XIX, ML2350XMX TYP (NOTE 4)	ML2340XIX, ML2350XMX ML2350XIX, ML2350XMX MAX	UNITS
Digital and DC (Continued)									
Supply Current, Unipolar Mode									
I_{CC}, V_{CC} Current	5	V_{CC} = 5V ± 10%			6.0			6.0	mA
I_{AGND}, Analog Ground Current					–4.3			–4.3	mA
I_{VZS}, V_{ZS} Current					–1.7			–1.7	mA
I_{CC}, V_{CC} Current	5	V_{CC} = 12V ±10%			11.0			11.0	mA
I_{AGND}, Analog Ground Current					–7.3			–7.3	mA
I_{VZS}, V_{ZS} Current					–3.7			–3.7	mA
AC Performance									
Settling Time t_{S1}	5	Figure 2, Output Step of AGND + 1V to V_{CC} – 1V, R_L = 1K		1.2	2.5		1.2	3.0	µs
t_{S2}		Output Step of AGND + 100mV to V_{CC} – 100mV, R_L = 100K		2.5	5		2.5	6	µs
t_{S3}		Output Step of ±1LSB			1			1	µs
t_{S4}, Gain Change		Change of Any Gain Setting		1.1	2.5		1.1		µs
t_{XFER}, XFER Pulse Width	5	Figure 3	60			60			ns
t_{DBS}, DB0–DB7 Setup Time	5	Figure 3	40			45			ns
t_{DBH}, DB0–DB7 Hold Time	5	Figure 3	0			0			ns
t_{RESET}, Power-On Reset Time	6				16			16	µs

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to analog ground

Note 2: When the voltage at any pin exceeds the power supply rails (V_{IN} < AGND or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: –55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

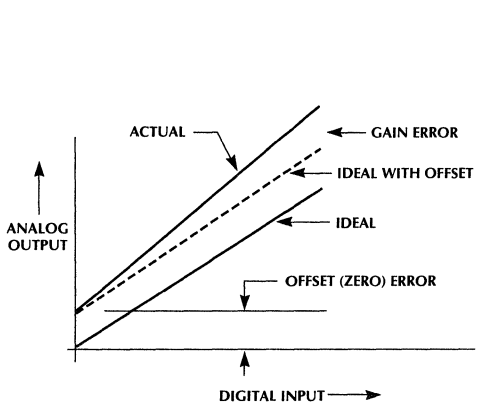
Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

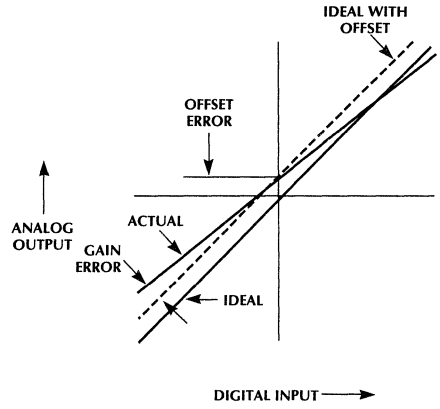
Note 6: Parameter guaranteed Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Supply current and analog ground current are specified with the digital inputs stable and no load on V_{OUT}.

Note 8: In unipolar operation with V_{ZS} and AGND tied together, digital codes that represent an analog value of less than 100mV from AGND should be avoided.



Unipolar Mode



Unipolar Mode

Figure 1. Gain and Offset Error

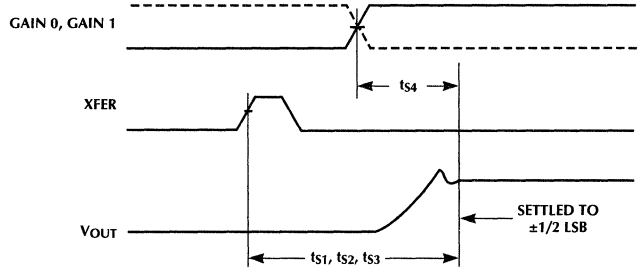


Figure 2. Settling Time

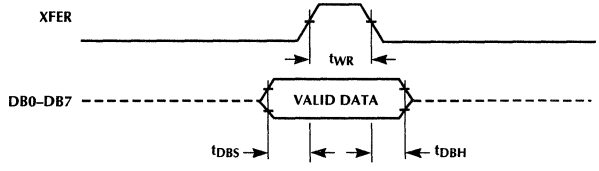


Figure 3. Single Buffered Mode

1.0 FUNCTIONAL DESCRIPTION

1.1 D/A CONVERTER

The D/A converter is implemented using an array of equal current sources that are decoded semi linearly for the four most significant bits to improve differential linearity and to reduce output glitch around major carries. See Figure 4.

The input voltage reference of the D/A converter is the difference between $V_{REF\ IN}$ and AGND. This difference voltage is converted to a reference current using an internal resistor to set up the appropriate current level in the D/A converter. The D/A converter output current is then converted to a voltage output by an output buffer and a resistive network. The matching among the on-chip resistors preserves the gain accuracy between these conversions.

The D/A converter can be used in a multiplying mode by modulating the reference input within the specified $V_{REF\ IN}$ range.

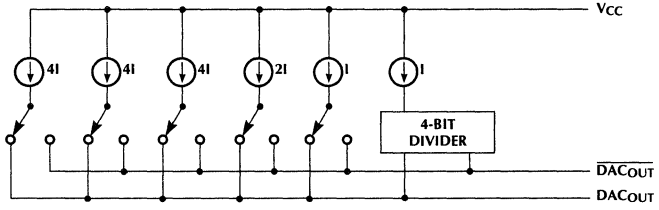


Figure 4. D/A Converter Implementation

1.2 SINGLE-SUPPLY vs. DUAL-SUPPLY OPERATION

ML2340 and ML2350 can be powered from a single supply ranging from 4.5V to 13.2V or dual supplies ranging from ±2.25V to ±6.6V.

The internal digital and analog circuitry is powered between V_{CC} and AGND. The range of DGND is AGND ≤ DGND ≤ V_{CC} – 4.5V with the logic thresholds set between 0.8V and 2.0V above DGND (standard TTL logic level). The range of V_{ZS} is AGND ≤ V_{ZS} ≤ (V_{CC} – 2.25V).

1.3 UNIPOLAR AND BIPOLAR OUTPUT VOLTAGE SWING

ML2340 and ML2350 can operate in either unipolar bipolar output voltage mode. Unipolar/bipolar mode selection is determined by comparing the zero scale voltage (V_{ZS}) of these devices to a precise internal reference that is referred to AGND. V_{ZS} is ideally the voltage that will be produced at the DAC voltage output when the digital input data is set to all "0's" Unipolar mode is selected when V_{ZS} is lower than 1.00 volt, and bipolar mode is selected when V_{ZS} is greater than 1.50 volts.

1.3.1 Unipolar Output Mode

In the unipolar mode, V_{OUT} swings above V_{ZS}. Ideally the 00000000 code results in an output voltage of V_{ZS}, and the 11111111 code results in an output voltage of V_{FS} x 255/256, where V_{FS} is the full-scale voltage determined by $V_{REF\ IN}$ and the gain setting.

1.3.2 Bipolar Output Mode

In the bipolar mode, V_{OUT} swings around V_{ZS}. The input data is in 2's complement binary format. Ideally, the 00000000 code results in an output voltage of V_{ZS}; the 10000000 code results in an output voltage of (V_{ZS} – V_{FS}); and the 01111111 results in an output voltage of (V_{ZS} + V_{FS} 127/128), where V_{FS} is the full scale output voltage determined by $V_{REF\ IN}$ and the gain setting.

1.4 OUTPUT BUFFER AND GAIN SETTING

The output buffer converts the D/A output current to a voltage output using a resistive network with proper gain setting determined by the GAIN 0 and GAIN 1 inputs. There are four possible gain settings for unipolar output voltage mode and bipolar output voltage mode as listed below:

Unipolar Output Voltage Mode

GAIN 1	GAIN 0	GAIN	Voltage Output Swing Relative to V_{ZS}
0	0	1/4	$V_{REF\ IN}$ × 1/4
0	1	1/2	$V_{REF\ IN}$ × 1/2
1	0	1	$V_{REF\ IN}$ × 1
1	1	2	$V_{REF\ IN}$ × 2

Bipolar Output Voltage Mode

GAIN 1	GAIN 0	GAIN	Voltage Output$_{P-P}$
0	0	1/4	$V_{REF\ IN} \times 1/8$
0	1	1/2	$V_{REF\ IN} \times 1/4$
1	0	1	$V_{REF\ IN} \times 1/2$
1	1	2	$V_{REF\ IN} \times 1$

The output buffer can source or sink as much as 10mA of current with an output voltage of at least 1V from either V_{CC} or AGND. As the output voltage approaches V_{CC} or AGND the current sourcing/sinking capability of the output buffer is reduced. The output buffer can still swing down to within 10mV of AGND and up to within 40mV of V_{CC} with a 100K load at V_{OUT} to AGND in the unipolar operation. In the bipolar operation, the output buffer swing is limited to about 100mV from either rails.

1.5 VOLTAGE REFERENCE

A bandgap voltage reference is incorporated on the ML2340 and ML2350. Two reference voltages can be produced by each device. An internal comparator monitors the power supply voltage to determine the selection of the reference voltage. A reference voltage of 2.25 volts on the ML2340 and 2.50 volts on the ML2350 is selected when the supply voltage is less than approximately 7.50 volts. Otherwise, a reference voltage of 4.50 volts and 5.00 volts is selected. To prevent the comparator from oscillating between the two selections, avoid operation with a power supply between 70 and 8.0 volts.

The bandgap reference is trimmed for zero Temperature Coefficient (TC) at 35°C to minimize output voltage drift over the specified operating temperature range.

The internal reference is buffered for use by the DAC and external circuits. The reference buffer will source more than 5mA of current and sink more than 1mA of current. With $V_{REF\ IN}$ connected to $V_{REF\ OUT}$, the following output voltage ranges of the DAC are obtained:

ML2340

Gain Setting	V_{REF} = 2.25V with $V_{CC} \le$ 7.0V		V_{REF} = 4.5V with $V_{CC} \ge$ 8.0V	
	Unipolar	Bipolar	Unipolar	Bipolar
1/4	0 to 0.562V	–0.281V to +0.281V	0 to 1.125V	–0.562V to +0.562V
1/2	0 to 1.125V	–0.562V to +0.562V	0 to 2.250V	–1.125V to +1.125V
1	0 to 2.250V	–1.125V to +1.125V	0 to 4.500V	–2.250V to +2.250V
2	0 to 4.500V	–2.250V to +2.250V	0 to 9.000V	–4.500V to +4.500V

ML2350

Gain Setting	V_{REF} = 2.50V with $V_{CC} \le$ 7.0V		V_{REF} = 5.0V with $V_{CC} \ge$ 8.0V	
	Unipolar	Bipolar	Unipolar	Bipolar
1/4	0 to 0.625V	–0.3125V to +0.3125V	0 to 1.25V	–0.625V to +0.625V
1/2	0 to 1.250V	–0.6250V to +0.6250V	0 to 2.50V	–1.250V to +1.250V
1	0 to 2.500V	–1.2500V to +1.2500V	0 to 5.00V	–2.500V to +2.500V
2	0 to 5.000V	–2.5000V to +2.5000V	0 to 10.00V	–5.000V to +5.000V

An external reference can alternatively be used on $V_{REF\ IN}$ to set the desired full scale voltage. The linearity of the D/A converter depends on the reference used, however. To insure integral linearity at an 8-bit level, a reference voltage of no less than 2V and no more than 7V (2.75V for operation with a low-voltage power supply) should be used.

1.6 DIGITAL INTERFACE

The digital interface of the ML2340 and ML2350 consist of a transfer input (XFER) and eight data inputs, DB0 through DB7. The digital interface operates in one of the two modes:

1.6.1 Single-Buffered Mode

Digital input data on DB0–DB7 is passed through an 8-bit transparent input latch on the rising edge of XFER. Because the outputs of the latch are connected directly to the inputs of the internal DAC, changes on the digital data while the XFER input is still active will cause an immediate change in the DAC output voltage. To hold the input data on the latch, the XFER input needs deactivated while the data is still stable.

1.6.2 Flow-Through Mode

In the flow-through mode, the input latch is bypassed. When XFER is set to logic "1", a change of data inputs, DB0–DB7, results in an immediate update of the output voltage.

1.7 POWER-ON-RESET

The ML2340 and ML2350 have an internal power-on-reset circuit to initialize the device when power is first applied to the device. The power-on-reset interval of typically 8µs begins when the supply voltage, V_{CC} reaches approximately 2.0V. During the power-on-reset interval, the transparent latch is reset to all "0's".

2.0 TYPICAL APPLICATIONS

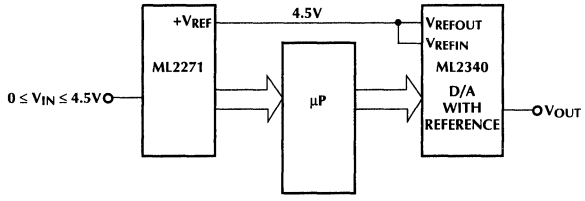


Figure 5. Using 4.50V Reference of D/A for Reference of A/D Using Single 5V V_{CC} ± 10%

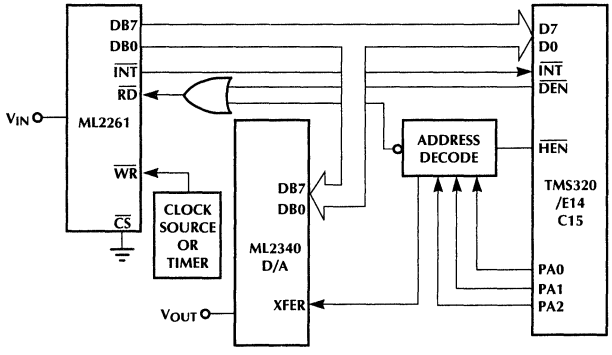


Figure 6. TMS320 Interface

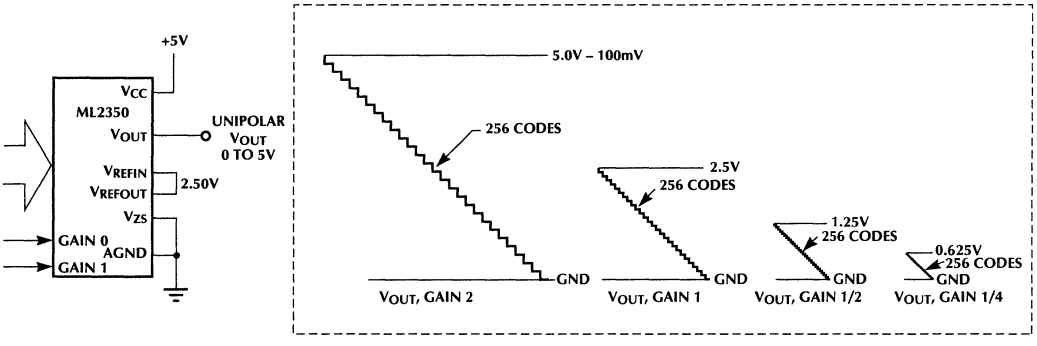


Figure 7. Single 5V Supply Unipolar V_{OUT}

TYPICAL APPLICATIONS (Continued)

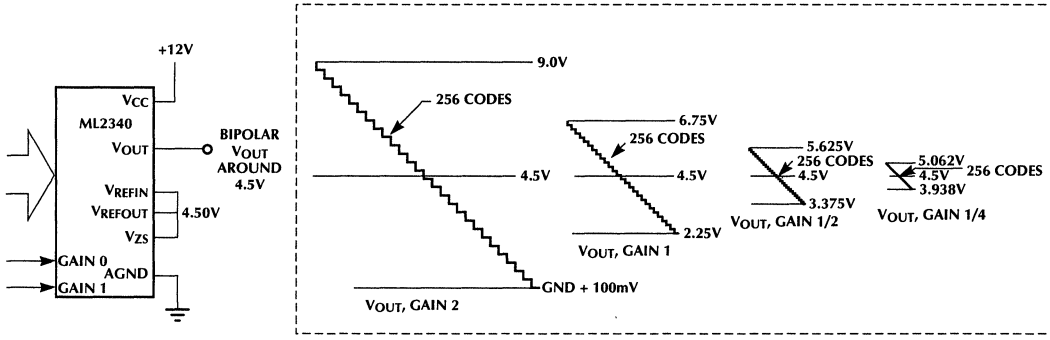


Figure 8. Single 12V Supply, Bipolar V_{OUT} with 11-Bits Resolution Around Zero

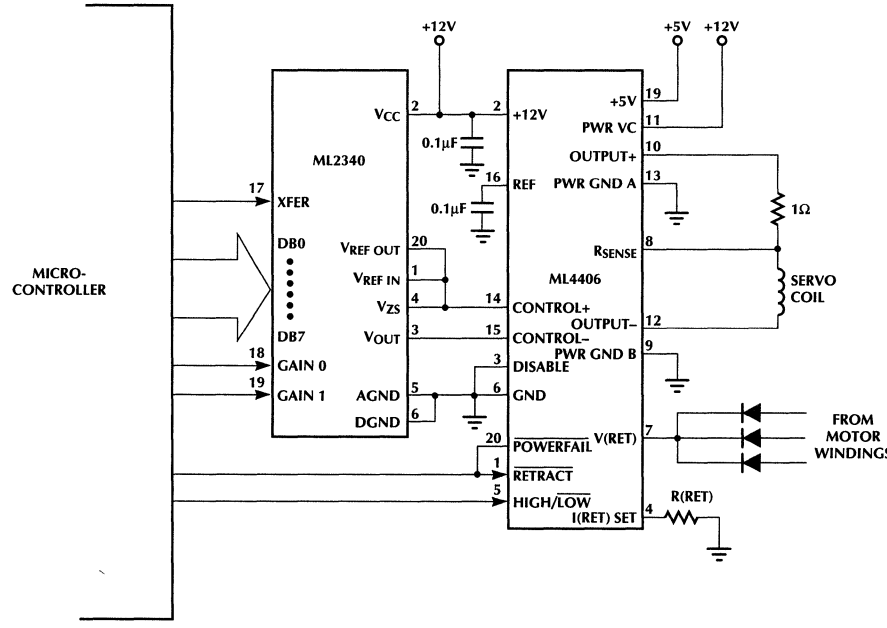


Figure 9. Hard Disc Drive Servo Coil Driver Providing 13-Bit Effective Resolution

ORDERING INFORMATION

PART NUMBER	INTEGRAL & DIFFERENTIAL NON-LINEARITY	TEMPERATURE RANGE	PACKAGE
$V_{REF\ OUT}$ = 2.25V with V_{CC} = 5V			
ML2340BMJ/5	±¼ LSB	–55°C to +125°C	Hermetic DIP (J18)
ML2340BIJ/5		–40°C to +85°C	Hermetic DIP (J18)
ML2340BCP/5		0°C to +70°C	Molded DIP (P18)
ML2340BCQ/5		0°C to +70°C	Molded PCC (Q18)
ML2340CMJ/5	±½ LSB	–55°C to +125°C	Hermetic DIP (J18)
ML2340CCP/5		0°C to +70°C	Molded DIP (P18)
ML2340CCQ/5		0°C to +70°C	Molded PCC (Q18)
$V_{REF\ OUT}$ = 2.50V with V_{CC} = 5V			
ML2350BMJ/5	±¼ LSB	–55°C to +125°C	Hermetic DIP (J18)
ML2350BIJ/5		–40°C to +85°C	Hermetic DIP (J18)
ML2350BCP/5		0°C to +70°C	Molded DIP (P18)
ML2350BCQ/5		0°C to +70°C	Molded PCC (Q18)
ML2350CMJ/5	±½ LSB	–55°C to +125°C	Hermetic DIP (J18)
ML2350CCP/5		0°C to +70°C	Molded DIP (P18)
ML2350CCQ/5		0°C to +70°C	Molded PCC (Q18)
$V_{REF\ OUT}$ = 4.50V with V_{CC} = 12V			
ML2340BMJ/12	±¼ LSB	–55°C to +125°C	Hermetic DIP (J18)
ML2340BIJ/12		–40°C to +85°C	Hermetic DIP (J18)
ML2340BCP/12		0°C to +70°C	Molded DIP (P18)
ML2340BCQ/12		0°C to +70°C	Molded PCC (Q18)
ML2340CMJ/12	±½ LSB	–55°C to +125°C	Hermetic DIP (J18)
ML2340CCP/12		0°C to +70°C	Molded DIP (P18)
ML2340CCQ/12		0°C to +70°C	Molded PCC (Q18)
$V_{REF\ OUT}$ = 5.00V with V_{CC} = 12V			
ML2350BMJ/12	±1/4 LSB	–55°C to +125°C	Hermetic DIP (J18)
ML2350BIJ/12		–40°C to +85°C	Hermetic DIP (J18)
ML2350BCP/12		0°C to +70°C	Molded DIP (P18)
ML2350BCQ/12		0°C to +70°C	Molded PCC (Q18)
ML2350CMJ/12	±1/2 LSB	–55°C to +125°C	Hermetic DIP (J18)
ML2350CCP/12		0°C to +70°C	Molded DIP (P18)
ML2350CCQ/12		0°C to +70°C	Molded PCC (Q18)

Micro Linear

ML2341, ML2351

Single Supply, Programmable 8-Bit D/A Converters

GENERAL DESCRIPTION

The ML2341 and ML2351 are CMOS voltage output, 8-bit D/A converters with an internal voltage reference and a μP interface. These devices are designed to be powered by a single supply, although they can be powered from dual power supplies. The output voltage swings above zero scale (V_{ZS}) in the unipolar mode or around zero scale (V_{ZS}) in the bipolar mode, both with programmable gain. V_{ZS} can be set to any voltage from AGND to 2.25V below V_{CC}. The digital and analog grounds, DGND and AGND, are totally independent of each other. DGND can be set to any voltage from AGND to 4.5V below V_{CC} for easy interfacing to standard TTL and CMOS logic families.

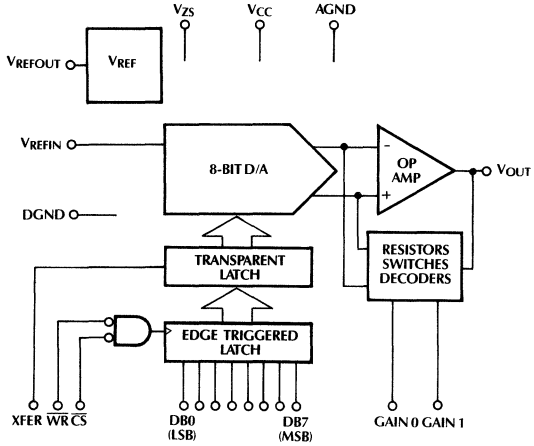
The high level of integration and versatility of the ML2341 and ML2351 makes them ideal for a wide range of applications in hard disk drives, automotive, telecom, and a variety of general purpose industrial. One specific intended application is controlling a hard disk voice coil.

The ML2341 provides a 2.25V or 4.50V reference output for use with A/D converters that use a single 5V ± 10% power supply, while the ML2351 provides a 2.50V or 5.00V reference output.

FEATURES

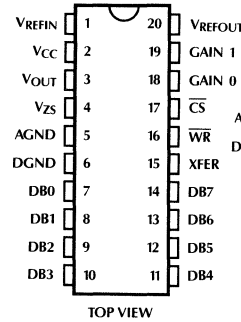
- Programmable output voltage gain settings of 2, 1, ½, ¼ provide 8-, 9-, 10-, or 11-bit effective resolution around zero
- AGND to V_{CC} output voltage swing
- Bipolar or unipolar output voltage
- 4.5V to 13.2V single supply or ±2.25V to ±6.5V dual-supply operation
- Single- and double-buffered, edge-triggered interface with 30ns write time, 0ns hold time
- Voltage reference output
  - ML2341 ..... 2.25V or 4.50V
  - ML2351 ..... 2.50V or 5.00V
- Nonlinearity ..... ±¼ LSB or ±½ LSB
- Output voltage settling time over temperature and supply voltage tolerance
  - Within 1V of V_{CC} and AGND ..... 2.5μs max
  - Within 100mV of V_{CC} and AGND ..... 5μs max
- TTL and CMOS compatible digital inputs
- Low supply current ($V_{REF} \leq 2.5V$) ..... 5mA max
- 20-pin DIP or PCC
- Operating temperature range of 0°C to +70°C, –40°C to +85°C, and –55°C to +125°C

BLOCK DIAGRAM



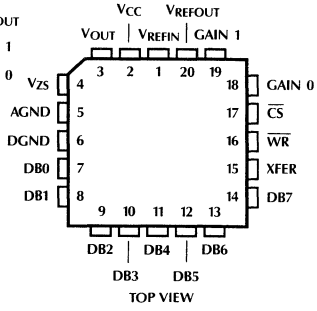
PIN CONNECTIONS

ML2341
ML2351
20-Pin DIP



TOP VIEW

ML2341
ML2351
20-Pin PCC



TOP VIEW

Micro Linear

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	$V_{REF\ IN}$	Voltage reference input. $V_{REF\ IN}$ is referenced to AGND.
2	V_{CC}	Positive supply.
3	V_{OUT}	Voltage output of the D/A converter. V_{OUT} is referenced to V_{ZS}.
4	V_{ZS}	Zero Scale Voltage. V_{OUT} is referenced to V_{ZS}. V_{ZS} is normally tied to AGND in the unipolar mode or to mid-supply in the bipolar mode. When the device is operated from a single power supply, V_{ZS} has a maximum current requirement of –300μA in the bipolar mode.
5	AGND	Analog ground.
6	DGND	Digital ground. This is the ground reference level for all digital inputs. The range is AGND < (V_{CC} – 4.5V). DGND is normally tied to system ground.
7	DB0	Data input — Bit 0 (LSB).
8	DB1	Data input — Bit 1.
9	DB2	Data input — Bit 2.
10	DB3	Data input — Bit 3.
11	DB4	Data input — Bit 4.
12	DB5	Data input — Bit 5.
13	DB6	Data input — Bit 6.
14	DB7	Data input — Bit 7 (MSB).
15	XFER	Transfer enable input. In the double buffered mode of operation, the data in the input latch is transferred to the D/A converter at the high level of XFER.
16	$\overline{WR}$	Write enable input. While $\overline{CS}$ is low, data inputs are latched into the input latch on the rising edge of $\overline{WR}$.
17	$\overline{CS}$	Chip select input. Active low input which enables latching in the data on the rising edge of $\overline{WR}$.
18	GAIN 0	Digital gain setting input 0.
19	GAIN 1	Digital gain setting input 1.
20	$V_{REF\ OUT}$	Voltage reference output. $V_{REF\ OUT}$ is referenced to AGND. $V_{REF\ OUT}$ is set to 2.5V and 5.0V in a low-voltage and high-voltage operation, respectively for the ML2351; 2.25V and 4.5V for the ML2341.

2

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage V_{CC} with Respect to AGND 14.2V
DGND ..... –0.3V to V_{CC} + 0.3V
V_{ZS}, $V_{REF\ IN}$ ..... –0.3V to V_{CC} + 0.3V
Logic Inputs ..... –0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Package Dissipation at T_A = 25°C (Board Mount) 875mW
Lead Temperature (Soldering 10 sec.)
Dual-In-Line Package (Plastic) ..... 260°C
Dual-In-Line Package (Ceramic) ..... 300°C
Molded Chip Carrier Package
Vapor Phase (60 sec.) ..... 215°C
Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS
(Note 1)

Supply Voltage, V_{CC} ..... 4.5V_{DC} to 13.2V_{DC}
Temperature Range (Note 3) ..... $T_{MIN} \leq T_A \leq T_{MAX}$
ML2341BMJ, ML2341CMJ
ML2351BMJ, ML2351CMJ ..... –55°C to +125°C
ML2341BIJ, ML2341CIJ
ML2351BIJ, ML2351CIJ ..... –40°C to +85°C
ML2341BCQ, ML2341CCQ
ML2351BCQ, ML2351CCQ
ML2341BCP, ML2341CCP
ML2351BCP, ML2351CCP ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} – AGND = 5V ± 10% and 12V ± 10% (Note 9), $V_{REF\ IN}$ for ML2341 = 2.25V and 4.50V, for ML2351 $V_{REF\ IN}$ = 2.50V and 5.00V, V_{OUT} load is R_L = 1K and C_L = 100pF, V_{REF} load is R_L = 1K and C_L = 100pF and input control signals with $t_R = t_F \leq 20$ns.

			ML2341XCX, ML2351XCX			ML2341XIX, ML2341XMX ML2351XIX, ML2351XMX			
PARAMETER	NOTES	CONDITIONS	MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	UNITS
Converter and Programmable Gain Amplifier									
Converter Resolution	5		8			8			Bits
Integral Linearity Error ML2341BXX, ML2351BXX ML2341CXX, ML2351CXX	5	GAIN = 2, 1, ½, or ¼			 ±¼ ±½			 ±¼ ±½	 LSB LSB
Differential Linearity Error ML2341BXX, ML2351BXX ML2341CXX, ML2351CXX	5	GAIN = 2, 1, ½, or ¼			 ±¼ ±½			 ±¼ ±½	 LSB LSB
Mode Select Unipolar Output Bipolar Output	5	V_{ZS} with respect to AGND	 0 1.50		 1.0 V_{CC}–2.25	 0 1.50		 1.0 V_{CC}–2.25	 V V
Offset Error Unipolar Mode	5	Figure 1 GAIN = ¼, ½, 1 GAIN = 2			 ±10 ±20			 ±12 ±24	 mV mV
Bipolar Mode	5	Figure 1 GAIN = ¼, ½, 1, 2			±10 plus ±2½ LSB			±10 plus ±2½ LSB	mV
Gain Error Unipolar Mode Bipolar Mode	5	Figure 1 GAIN = ¼, ½, 1, 2 GAIN = ¼, ½, 1, 2		 ±.5 ±.5	 ±2 ±2		 ±.5 ±.5	 ±2.5 ±2.5	 %FS %FS
Reference									
$V_{REF\ OUT}$ Voltage ML2341BXX/5	5	V_{CC} = 5.0V T_A = 25°C T_{MIN} to T_{MAX}	2.23 2.22	2.25	2.27 2.28	2.23 2.18	2.25	2.27 2.32	V V
ML2341CXX/5		V_{CC} = 5.0V T_A = 25°C T_{MIN} to T_{MAX}	2.22 2.20	2.25	2.29 2.30	2.22 2.18	2.25	2.28 2.32	V V
ML2351BXX/5	5	V_{CC} = 5.0V T_A = 25°C T_{MIN} to T_{MAX}	2.48 2.47	2.50	2.52 2.53	2.48 2.43	2.50	2.52 2.57	V V
ML2351CXX/5		V_{CC} = 5.0V T_A = 25°C T_{MIN} to T_{MAX}	2.45 2.44	2.50	2.55 2.58	2.46 2.42	2.50	2.55 2.59	V V
ML2341BXX/12	5	V_{CC} = 12.0V T_A = 25°C T_{MIN} to T_{MAX}	4.48 4.46	4.50	4.52 4.54	4.48 4.43	4.50	4.52 4.57	V V
ML2341CXX/12		V_{CC} = 12.0V T_A = 25°C T_{MIN} to T_{MAX}	4.45 4.40	4.50	4.55 4.60	4.45 4.35	4.50	4.55 4.65	V V
ML2351BXX/12	5	V_{CC} = 12.0V T_A = 25°C T_{MIN} to T_{MAX}	4.98 4.96	5.00	5.02 5.04	4.98 4.90	5.00	5.02 5.10	V V
ML2351CXX/12		V_{CC} = 12.0V T_A = 25°C T_{MIN} to T_{MAX}	4.95 4.90	5.00	5.05 5.10	4.95 4.85	5.00	5.05 5.15	V V
Temperature Coefficient $V_{REF\ OUT}$				50			50		ppm/°C
V_{REF} Output Current	5		0.75		5	0.75		5	mA
$V_{REF\ OUT}$ Power Supply Rejection Ratio	5	100mV_{P-P}, 1kHz Sinewave on V_{CC}	–40	–60		–40	–60		dB

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} – AGND = 5V ± 10% and 12V ± 10% (Note 9), $V_{REF\ IN}$ for ML2341 = 2.25V and 4.50V; for ML2351 $V_{REF\ IN}$ = 2.50V and 5.00V, V_{OUT} load is R_L = 1K and C_L = 100pF, V_{REF} load is R_L = 1K and C_L = 100pF and input control signals with $t_R = t_F \leq 20$ns.

PARAMETER	NOTES	CONDITIONS	ML2341XCX, ML2351XCX			ML2341XIX, ML2341XMX ML2351XIX, ML2351XMX			UNITS
			MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
$V_{REF\ IN}$ and V_{ZS}									
$V_{REF\ IN}$ Input Range	5	$V_{CC} \leq 8.75V$ $V_{CC} \geq 8.75V$	AGND+2 AGND+2		V_{CC}–1.75 AGND+7	AGND+2 AGND+2		V_{CC}–1.75 AGND+7	V V
$V_{REF\ IN}$ DC Input Resistance	5		10			10			MΩ
V_{ZS} Voltage Range	5, 8	$V_{CC} \leq 7.0V$	AGND		V_{CC}– 2.25	AGND		V_{CC}– 2.25	V
	5, 8	$V_{CC} \geq 8.0V$	AGND		V_{CC}–3.0	AGND		V_{CC}–3.0	V
Analog Output									
V_{OUT} Output Swing Unipolar Mode	5, 8	R_L = 100K	AGND+ 0.01		V_{CC}–.05	AGND+ 0.01		V_{CC}–.05	V
		R_L = 1K	AGND+ 1.0		V_{CC}–1.0	AGND+ 1.0		V_{CC}–1.0	V
Bipolar Mode	5	R_L = 100K	AGND+ 0.1		V_{CC}–0.1	AGND+ 0.1		V_{CC}–0.1	V
		R_L = 1K	AGND+ 1.0		V_{CC}–1.0	AGND+ 1.0		V_{CC}–1.0	V
V_{OUT} Output Current	5	AGND+1V<V_{OUT}<V_{CC}–1V	–10		+10	–10		+10	mA
Power Supply Rejection Ratio		100mV_{P-P}, 1kHz sinewave on V_{CC}		–60			–60		dB
Digital and DC									
$V_{IN(0)}$ Logical "0" Input Voltage	5				0.8			0.8	V
$V_{IN(1)}$ Logical "1" Input Voltage	5		2.0			2.0			V
$I_{IN(0)}$ Logical "0" Input Current	5	V_{IN} = DGND	–1			–1			μA
$I_{IN(1)}$ Logical "1" Input Current	5	V_{IN} = V_{CC}			1			1	μA
Supply Current, Bipolar Mode									
I_{CC}, V_{CC} Current	5	V_{CC} = 5V ± 10%			5.3			5.3	mA
I_{AGND}, Analog Ground Current					–5.0			–5.0	mA
I_{VZS}, V_{ZS} Current				–90	–300		–90	–300	μA
I_{CC}, V_{CC} Current	5	V_{CC} = 12V ± 10%			9.3			9.3	mA
I_{AGND}, Analog Ground Current					–9.0			–9.0	mA
I_{VZS}, V_{ZS} Current				–90	–300		–90	–300	μA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} – AGND = 5V ± 10% and 12V ± 10% (Note 9), $V_{REF\ IN}$ for ML2341 = 2.25V and 4.50V; for ML2351 $V_{REF\ IN}$ = 2.50V and 5.00V, V_{OUT} load is R_L = 1k and C_L = 100pF, V_{REF} load is R_L = 1K and C_L = 100pF and input control signals with $t_R = t_F \leq$ 20ns.

PARAMETER	NOTES	CONDITIONS	ML2341XCX, ML2351XCX			ML2341XIX, ML2341XMX ML2351XIX, ML2351XMX			UNITS
			MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
Digital and DC (Continued)									
Supply Current, Unipolar Mode									
I_{CC}, V_{CC} Current	5	V_{CC} = 5V ± 10%			6.0			6.0	mA
I_{AGND}, Analog Ground Current					–4.3			–4.3	mA
I_{VZS}, V_{ZS} Current					–1.7			–1.7	mA
I_{CC}, V_{CC} Current	5	V_{CC} = 12V ± 10%			11.0			11.0	mA
I_{AGND}, Analog Ground Current					–7.3			–7.3	mA
I_{VZS}, V_{ZS} Current					–3.7			–3.7	mA
AC Performance									
Settling Time	5	Figure 2,							
t_{S1}		Output Step of AGND + 1V to V_{CC} – 1V, R_L = 1K		1.2	2.5		1.2	3.0	µs
t_{S2}		Output Step of AGND + 100mV to V_{CC}–100mV, R_L = 100K		2.5	5		2.5	6	µs
t_{S3}		Output Step of ±1LSB			1			1	µs
t_{S4}, Gain Change		Change of Any Gain Setting		1.1	2.5		1.1	3	µs
t_{WR}, $\overline{WR}$ Pulse Width	5	Figure 3	40			40			ns
t_{XFER}, XFER Pulse Width	5	Figure 3	60			60			ns
t_{XW}, $\overline{WR}$↑ to XFER↓	6	Figure 3	30			30			ns
t_{DBS}, DB0–DB7 Setup Time	5	Figure 3	40			45			ns
t_{DBH}, DB0–DB7 Hold Time	5	Figure 3	0			0			ns
t_{CSS}, $\overline{CS}$ Setup Time	5	Figure 3	50			50			ns
t_{CSH}, $\overline{CS}$ Hold Time	5	Figure 3	0			0			ns
t_{RESET}, Power-On Reset Time	6				16			16	µs

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to analog ground.

Note 2: When the voltage at any pin exceeds the power supply rails (V_{IN} < AGND or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: –55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

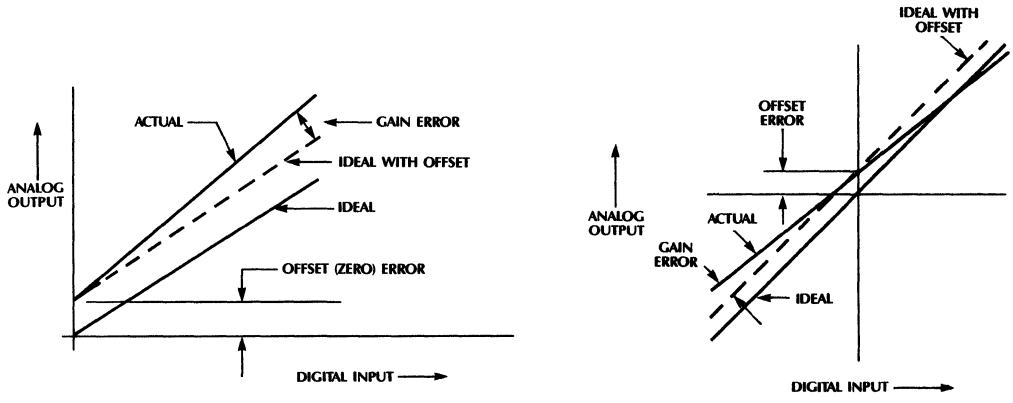
Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Supply current and analog ground current are specified with the digital inputs stable and no load on V_{OUT}.

Note 8: In unipolar operation with V_{ZS} and AGND tied together, digital codes that represent an analog value of less than 100mV from AGND should be avoided.

Note 9: ML2341XXX/5 and ML2351XXX/5 are tested for 5V operation only and ML2341XXX/12 and ML2351XXX/12 are tested for 12V operation.



Unipolar Mode

Bipolar Mode

Figure 1. Gain and Offset Error

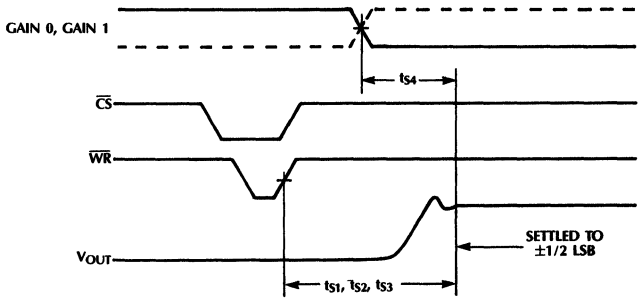


Figure 2. Settling Time

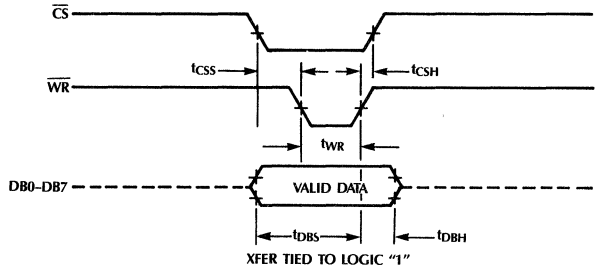


Figure 3a. Single Buffered Mode

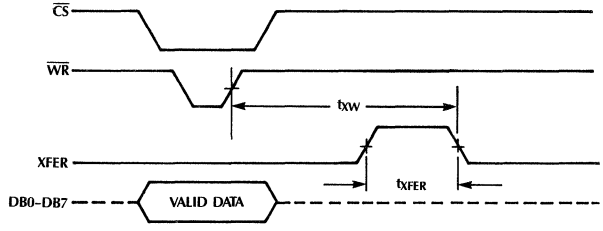


Figure 3b. Double Buffered Mode

1.0 FUNCTIONAL DESCRIPTION

1.1 D/A CONVERTER

The D/A converter is implemented using an array of equal current sources that are decoded semi linearly for the four most significant bits to improve differential linearity and to reduce output glitch around major carries. See Figure 4.

The input voltage reference of the D/A converter is the difference between $V_{REF\ IN}$ and AGND. This difference voltage is converted to a reference current using an internal resistor to set up the appropriate current level in the D/A converter. The D/A converter output current is then converted to a voltage output by an output buffer and a resistive network. The matching among the on-chip resistors preserves the gain accuracy between these conversions.

The D/A converter can be used in a multiplying mode by modulating the reference input within the specified $V_{REF\ IN}$ range.

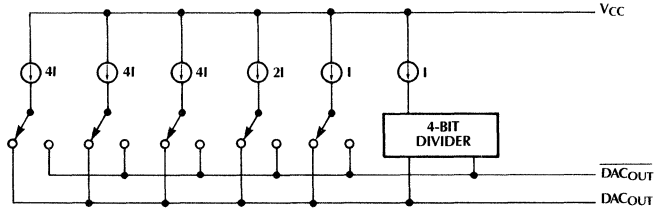


Figure 4. D/A Converter Implementation

1.2 SINGLE-SUPPLY vs. DUAL-SUPPLY OPERATION

ML2341 and ML2351 can be powered from a single supply ranging from 4.5V to 13.2V or dual supplies ranging from ±2.25V to ±6.6V.

The internal digital and analog circuitry is powered between V_{CC} and AGND. The range of DGND is AGND ≤ DGND ≤ V_{CC} - 4.5V with the logic thresholds set between .8V and 2.0V above DGND (standard TTL logic level). The range of V_{ZS} is AGND ≤ V_{ZS} ≤ (V_{CC} - 2.25V).

1.3 UNIPOLAR AND BIPOLAR OUTPUT VOLTAGE SWING

The ML2341 and ML2351 can operate in either unipolar and bipolar output voltage mode. Unipolar/bipolar mode selection is determined by comparing the zero scale voltage (V_{ZS}) of these devices to a precise internal reference that is referred to AGND. V_{ZS} is ideally the voltage that will be produced at the DAC voltage output when the digital input data is set to all "0's". Unipolar mode is selected when V_{ZS} is lower than 1.00 volt, and bipolar mode is selected when V_{ZS} is greater than 1.50 volts.

1.3.1 Unipolar Output Mode

In the unipolar mode, V_{OUT} swings above V_{ZS}. Ideally the 00000000 code results in an output voltage of V_{ZS}, and the 11111111 code results in an output voltage of V_{FS} × 255/256, where V_{FS} is the full-scale voltage determined by $V_{REF\ IN}$ and the gain setting.

1.3.2 Bipolar Output Mode

In the bipolar mode, V_{OUT} swings around V_{ZS}. The input data is in 2's complement binary format. Ideally, the 00000000 code results in an output voltage of V_{ZS}; the 10000000 code results in an output voltage of (V_{ZS} - V_{FS}); and the 01111111 results in an output voltage of (V_{ZS} + V_{FS} 127/128), where V_{FS} is the full scale output voltage determined by $V_{REF\ IN}$ and the gain setting.

1.4 OUTPUT BUFFER AND GAIN SETTING

The output buffer converts the D/A output current to a voltage output using a resistive network with proper gain setting determined by the GAIN 0 and GAIN 1 inputs. There are four possible gain settings for unipolar output voltage mode and bipolar output voltage mode as listed below:

Unipolar Output Voltage Mode

GAIN 1	GAIN 0	GAIN	Voltage Output Swing Relative to V_{ZS}
0	0	¼	$V_{REF\ IN}$ × ¼
0	1	½	$V_{REF\ IN}$ × ½
1	0	1	$V_{REF\ IN}$ × 1
1	1	2	$V_{REF\ IN}$ × 2

Bipolar Output Voltage Mode

GAIN 1	GAIN 0	GAIN	Voltage $Output_{P-P}$
0	0	¼	±$V_{REF\ IN}$ × ⅛
0	1	½	±$V_{REF\ IN}$ × ¼
1	0	1	±$V_{REF\ IN}$ × ½
1	1	2	±$V_{REF\ IN}$ × 1

The output buffer can source or sink as much as 10mA of current with an output voltage of at least 1V from either V_{CC} or AGND. As the output voltage approaches V_{CC} or AGND the current sourcing/sinking capability of the output buffer is reduced. The output buffer can still swing down to within 10mV of AGND and up to within 40mV of V_{CC} with a 100K load at V_{OUT} to AGND in the unipolar operation. In the bipolar operation, the output buffer swing is limited to about 100mV from either rails.

1.5 VOLTAGE REFERENCE

A bandgap voltage reference is incorporated on the ML2341 and ML2351. Two reference voltages can be produced by each device. An internal comparator monitors the power supply voltage to determine the selection of the reference voltage. A reference voltage of 2.25 volts on the ML2341 and 2.50 volts on the ML2351 is selected when the supply voltage is less than approximately 7.50 volts. Otherwise, a reference voltage of 4.50 volts and 5.00 volts is selected. To prevent the comparator from oscillating between the two selections, avoid operation with a power supply between 7.0 and 8.0 volts.

The bandgap reference is trimmed for zero Temperature Coefficient (TC) at 35°C to minimize output voltage drift over the specified operating temperature range.

The internal reference is buffered for use by the DAC and external circuits. The reference buffer will source more than 5mA of current and sink more than 1mA of current. With $V_{REF\ IN}$ connected to $V_{REF\ OUT}$, the following output voltage ranges of the DAC are obtained:

ML2341

Gain Setting	V_{REF} = 2.25V with V_{CC} ≤ 7.0V		V_{REF} = 4.5V with V_{CC} ≥ 8.0V	
	Unipolar	Bipolar	Unipolar	Bipolar
¼	0 to 0.562V	-0.281V to +0.281V	0 to 1.125V	-0.562V to +0.562V
½	0 to 1.125V	-0.562V to +0.562V	0 to 2.250V	-1.125V to +1.125V
1	0 to 2.250V	-1.125V to +1.125V	0 to 4.500V	-2.250V to +2.250V
2	0 to 4.500V	-2.250V to +2.250V	0 to 9.000V	-4.500V to +4.500V

ML2351

Gain Setting	V_{REF} = 2.50V with $V_{CC} \leq$ 7.0V		V_{REF} = 5.00V with $V_{CC} \geq$ 8.0V	
	Unipolar	Bipolar	Unipolar	Bipolar
¼	0 to 0.625V	-0.3125V to +0.3125V	0 to 1.25V	-0.625V to +0.625V
½	0 to 1.250V	-0.6250V to +0.6250V	0 to 2.50V	-1.250V to +1.250V
1	0 to 2.500V	-1.2500V to +1.2500V	0 to 5.00V	-2.500V to +2.500V
2	0 to 5.000V	-2.5000V to +2.5000V	0 to 10.00V	-5.000V to +5.000V

An external reference can alternatively be used on $V_{REF\ IN}$ to set the desired full scale voltage. The linearity of the D/A converter depends on the reference used, however. To insure integral linearity at an 8-bit level, a reference voltage of no less than 2V and no more than 7V (2.75V for operation with a low-voltage power supply) should be used.

1.6 DIGITAL INTERFACE

The digital interface of the device consists of a chip select input, $\overline{CS}$, a write input, $\overline{WR}$, a transfer input, XFER and eight data inputs, DB0 through DB7. The digital interface operates in one of the two modes:

1.6.1 Single-Buffered Mode

To use the ML2341 and ML2351 in the single-buffered mode, tie XFER to logic "1". This will put the D/A latch in the transparent mode and the rising edge of $\overline{WR}$ at low level of $\overline{CS}$ will latch the data on DB0–DB7 into the input latch as well as update the D/A output voltage.

1.6.2 Double-Buffered Mode

To use the devices in the double-buffered mode, timing information is applied to $\overline{WR}$ as well as XFER inputs. The rising edge of $\overline{WR}$ at low level of $\overline{CS}$ will latch the data on DB0–DB7 into the input latch. The D/A output voltage will not be updated, however, until XFER is brought to a high level, which transfers the data from input latch to D/A latch. Note that the D/A latch is a transparent latch controlled by the level, not edge, of the XFER input, any write operation to the input latch while XFER is still at a high level results in the immediate update of the D/A output voltage.

1.7 POWER-ON-RESET

The ML2341 and ML2351 have an internal power-on-reset circuit to initialize the device when power is first applied to the device. The power-on-reset interval of typically 8μs begins when the supply voltage, V_{CC} reaches approximately 2.0V. During the power-on-reset interval, both the input and data latch are reset to all "0's".

2.0 TYPICAL APPLICATIONS

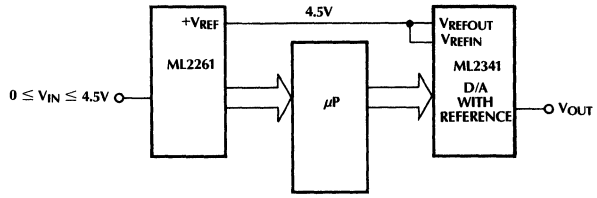


Figure 5. Using 4.50V Reference of D/A for Reference of A/D Using Single 5V V_{CC} ± 10%

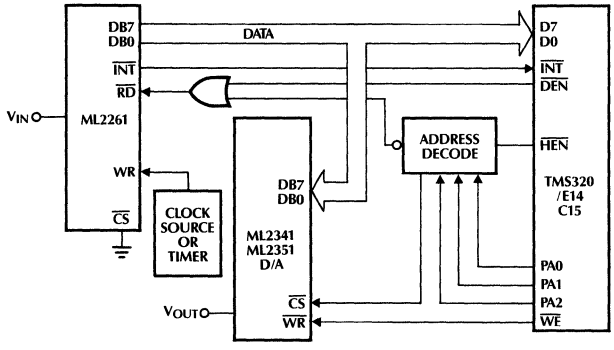


Figure 6. TMS320 Interface with D/A Output

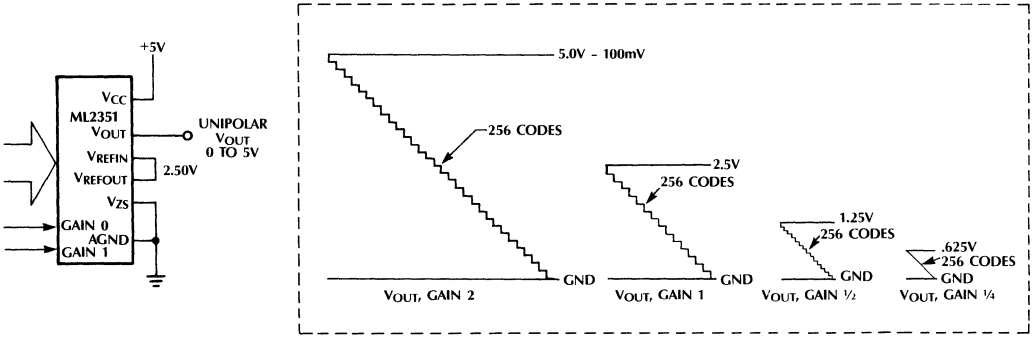


Figure 7. Single 5V Supply Unipolar V_{OUT}

2.0 TYPICAL APPLICATIONS (Continued)

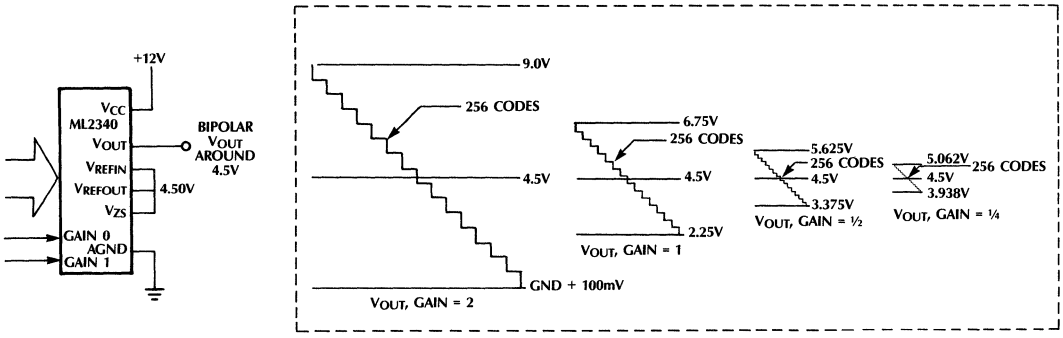


Figure 8. Single 12V Supply, Bipolar V_{OUT} with 11-Bits Resolution Around Zero

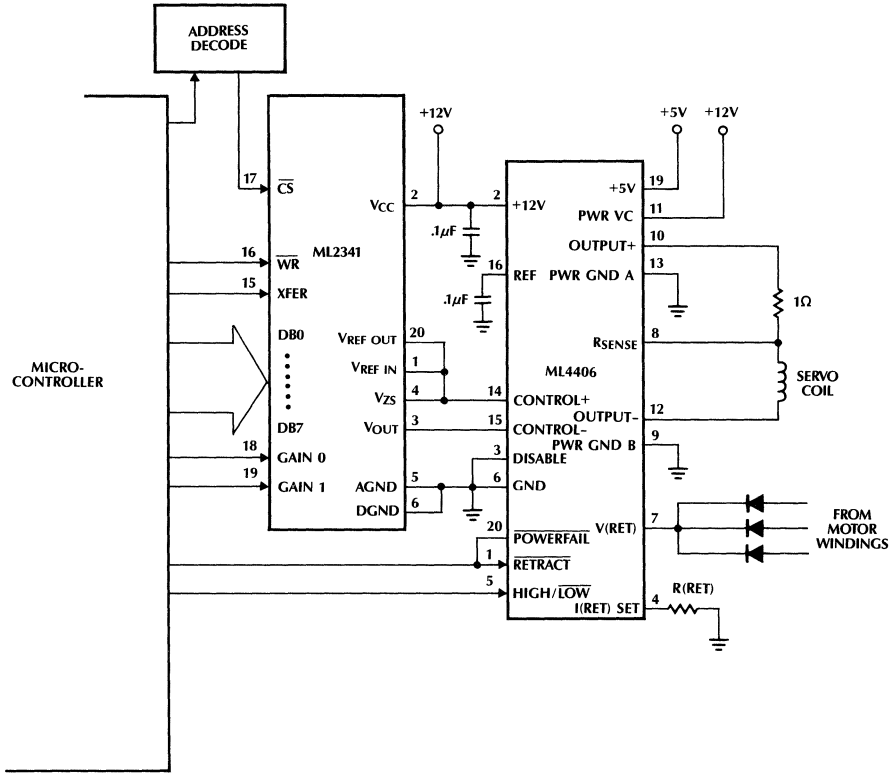


Figure 9. Hard Disc Drive Servo Coil Driver Providing 13-Bit Effective Resolution

ORDERING INFORMATION

PART NUMBER	INTEGRAL & DIFFERENTIAL NON-LINEARITY	TEMPERATURE RANGE	PACKAGE
$V_{REF\ OUT}$ = 2.25V with V_{CC} = 5V			
ML2341BMJ/5	±¼ LSB	–55°C to +125°C	HERMETIC DIP (J20)
ML2341BIJ/5		–40°C to +85°C	HERMETIC DIP (J20)
ML2341BCP/5		0°C to +70°C	MOLDED DIP (P20)
ML2341BCQ/5		0°C to +70°C	MOLDED PCC (Q20)
ML2341CMJ/5	±½ LSB	–55°C to +125°C	HERMETIC DIP (J20)
ML2341CIJ/5		–40°C to +85°C	HERMETIC DIP (J20)
ML2341CCP/5		0°C to +70°C	MOLDED DIP (P20)
ML2341CCQ/5		0°C to +70°C	MOLDED PCC (Q20)
$V_{REF\ OUT}$ = 2.50V with V_{CC} = 5V			
ML2351BMJ/5	±¼ LSB	–55°C to +125°C	HERMETIC DIP (J20)
ML2351BIJ/5		–40°C to +85°C	HERMETIC DIP (J20)
ML2351BCP/5		0°C to +70°C	MOLDED DIP (P20)
ML2351BCQ/5		0°C to +70°C	MOLDED PCC (Q20)
ML2351CMJ/5	±½ LSB	–55°C to +125°C	HERMETIC DIP (J20)
ML2351CIJ/5		–40°C to +85°C	HERMETIC DIP (J20)
ML2351CCP/5		0°C to +70°C	MOLDED DIP (P20)
ML2351CCQ/5		0°C to +70°C	MOLDED PCC (Q20)
$V_{REF\ OUT}$ = 4.50V with V_{CC} = 12V			
ML2341BMJ/12	±¼ LSB	–55°C to +125°C	HERMETIC DIP (J20)
ML2341BIJ/12		–40°C to +85°C	HERMETIC DIP (J20)
ML2341BCP/12		0°C to +70°C	MOLDED DIP (P20)
ML2341BCQ/12		0°C to +70°C	MOLDED PCC (Q20)
ML2341CMJ/12	±½ LSB	–55°C to +125°C	HERMETIC DIP (J20)
ML2341CIJ/12		–40°C to +85°C	HERMETIC DIP (J20)
ML2341CCP/12		0°C to +70°C	MOLDED DIP (P20)
ML2341CCQ/12		0°C to +70°C	MOLDED PCC (Q20)
$V_{REF\ OUT}$ = 5.00V with V_{CC} = 12V			
ML2351BMJ/12	±¼ LSB	–55°C to +125°C	HERMETIC DIP (J20)
ML2351BIJ/12		–40°C to +85°C	HERMETIC DIP (J20)
ML2351BCP/12		0°C to +70°C	MOLDED DIP (P20)
ML2351BCQ/12		0°C to +70°C	MOLDED PCC (Q20)
ML2351CMJ/12	±½ LSB	–55°C to +125°C	HERMETIC DIP (J20)
ML2351CIJ/12		–40°C to +85°C	HERMETIC DIP (J20)
ML2351CCP/12		0°C to +70°C	MOLDED DIP (P20)
ML2351CCQ/12		0°C to +70°C	MOLDED PCC (Q20)

ML2375, ML2377

DSP Analog I/O Peripheral

GENERAL DESCRIPTION

The ML2377 is a complete analog I/O peripheral front-end for DSP based control system. It contains a high-speed 10-bit A/D converter, a two channel simultaneous sample/hold circuit, a 6 channel input multiplexer, a 10-bit D/A converter and a 8-bit D/A converter.

The two channel simultaneous sample/hold in conjunction with the multiple channel multiplexer provided on-chip is especially well suited for disk drive applications, where minimum skew positional channel conversion and flexible calibration sensing functions are desirable.

Both input and output channel voltages are referenced to floating common points provided by the device. An additional common point is also available in the A/D input for flexibility. Bipolar conversion of ±2 volts around the floating point is provided by the chip.

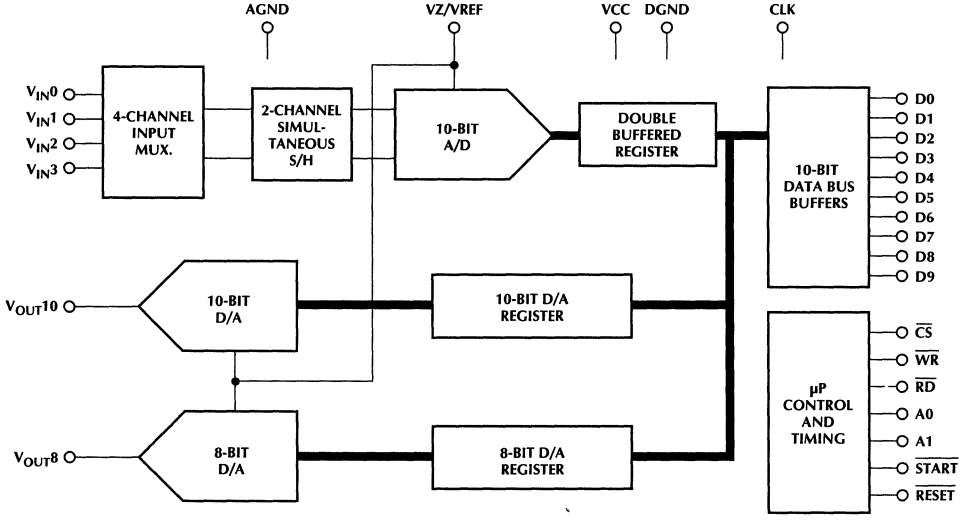
Channel multiplexing and common referencing control are provide on-chip via its easy to use microprocessing port. In addition, external control of the conversion start and MUX addressing is also available for the ML2377.

The ML2375 is a 4 channel version of the ML2377.

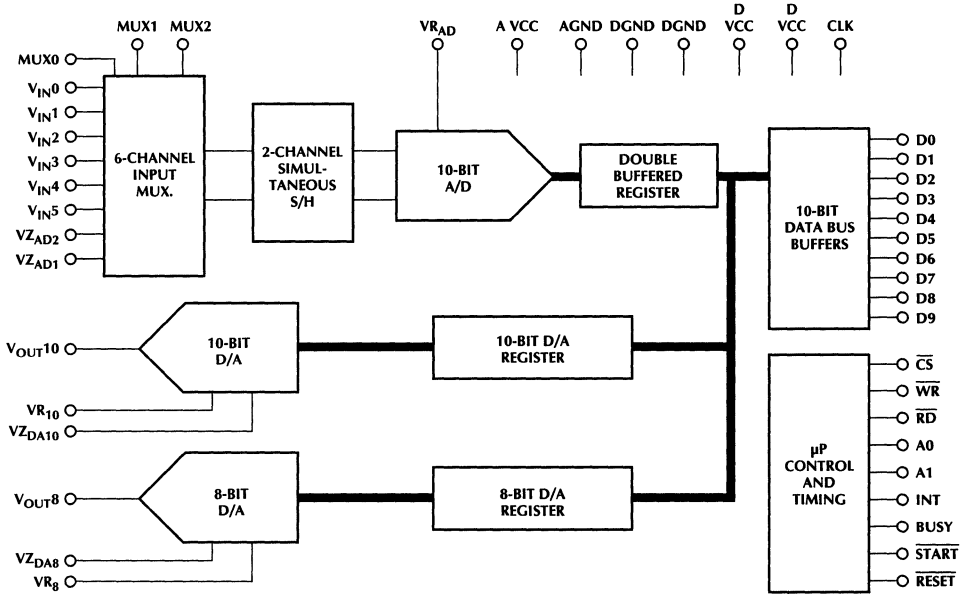
FEATURES

- 10-bit bipolar A/D resolution
- 10-bit bipolar and 8-bit bipolar D/A resolution
- 2µs A/D conversion time
- 2µs D/A settling time (ILSB, 4µs full scale)
- 2 channel simultaneous S/H
- 6 bipolar input channels
- A/D and D/A converters have no missing codes
- Inputs and outputs have floating commons
- ±2 volt input/output range with 2.5V reference
- Extra floating common input for A/D
- Programmable input MUX and common
- TMS320C14 compatible microprocessor interface
- Single 5 volt power supply
- External conversion start and MUX control (ML2377)
- Additional package and bond-out options available

BLOCK DIAGRAM ML2375

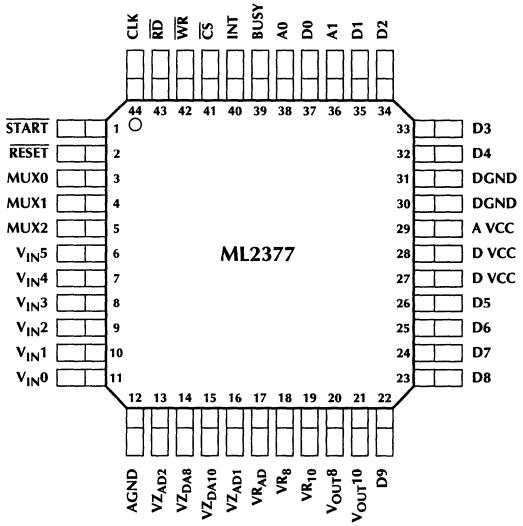


BLOCK DIAGRAM ML2377

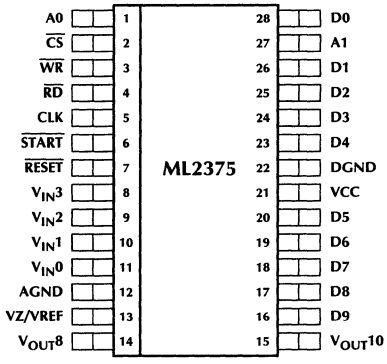


PIN CONNECTION

ML2377
44-Pin QFP (G44)



ML2375
28-Pin SSOP (R28)



2

PIN DESCRIPTION

NAME	FUNCTION
VZ_{AD2}	Programmable input common
VZ_{AD1}	Default A/D input common.
VZ_{DA10}	10-bit D/A common.
VZ_{DA8}	8-bit D/A common.
$\overline{START}$	Active low input starts A/D converter.
$\overline{RESET}$	Active low resets the IC.
MUX0	Multiplexer address bit 0.
MUX1	Multiplexer address bit 1.
MUX2	Multiplexer address bit 2.
$V_{IN}5$-0	Analog input channels 5 through 0.
AGND	Analog ground.
VR_{AD}	Voltage reference input for establishing ± full scale for the A/D converter. ± full scale value is 0.8 of the voltage on VR_{AD}, referenced to AGND.
VR_8	± full scale value for the 8-bit D/A converter is 0.8 of the voltage reference input on VR_8, referenced to AGND.
VR_{10}	± full scale value for the 10-bit D/A converter is 0.8 of the voltage reference input on VR_{10}, referenced to AGND.

NAME	FUNCTION
$V_{OUT}8$	Voltage output of the 8-bit D/A converter.
$V_{OUT}10$	Voltage output of the 10-bit D/A converter.
D9-D0	Data I/O bit 9 through 0.
DVCC	Digital power supply. +5 volts ±5%.
AVCC	Analog power supply. +5 volts ±5%.
DGND	Digital ground.
A1	Register address 1.
A0	Register address 0.
BUSY	Active high output indicates that an A/D conversion is in progress.
INT	Active high output indicating A/D conversion complete.
$\overline{CS}$	Active low chip select input.
$\overline{WR}$	Write input, active low.
$\overline{RD}$	Read input, active low
CLK	Clock input. Clock can be generated by tying a crystal from this pin to DGND or applying a clock directly to pin.

Note: ALE (Address Latch Enable) for demultiplexing address and data information can be made available on request. Consult Micro Linear for more information
Other pin-out options of the ML2377 are available on request.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages (AV_{CC} and DV_{CC}) 6.0V
Maximum Voltage Between AGND and DGND 1V
Maximum Voltage Between AV_{CC} and DV_{CC} 0.3V
Input Current per Pin ..... ±25mA
Package Dissipation @ 25°C 1W
Lead Temperature (Soldering, 10 sec) ..... 300°C

OPERATING CONDITIONS

Temperature Range ..... 0°C to +70°C
Supply Voltage (AV_{CC} and DV_{CC}) ..... $4.5V_{DC}$ to $6.0V_{DC}$

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation in not implied.

ELECTRICAL CHARACTERISTICS

The following specifications apply for $AV_{CC} = DV_{CC} = +5V \pm 5\%$, AGND = DGND = 0V, T_A = Operating Temperature Range $VZ_{AD1} = VZ_{AD2} = VZ_{DA10} = VZ_{DA8} = VR_{AD} = VR_8 = VR_{10} = 2.5V$, $T_A = T_{MIN}$ to T_{MAX} unless otherwise specified, C_L= 50pF for all digital outputs, $V_{OUT}8$ and $V_{OUT}10$ load is R_L = 1K and C_L = 100pF, and input control signals with $t_R = t_F$ 20ns, f_{CLK} = 11MHz.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
A/D Converter, S/H and Multiplexer Performance						
	Integral Linearity Error	C Grade			±3	LSB
		B Grade			±1	LSB
	Differential Linearity Error				±1	LSB
	Converter Resolution	V_{REF} = 2.5V	10			Bits
	Zero Error	VZ = 2.5V			±3	LSB
	Positive and Negative Full Scale Error	V_{REF} = 2.5V			±3	LSB
	Input Voltage Range		0		V_{CC}	V
	V_{REF} Input Resistance		1.5		3.5	kΩ
	Maximum V_{REF} Input Voltage	Referred to AGND			2.6	V
I_{ON}	On Channel Leakage Current	$0V < V_{IN} < V_{CC}$	–1		1	µA
I_{OFF}	Off Channel Leakage Current	$0V < V_{IN} < V_{CC}$	–1		1	µA
C_{ON}	On Channel Input Capacitance	$0V < V_{IN} < V_{CC}$		20		pF
C_{OFF}	Off Channel Input Capacitance	$0V < V_{IN} < V_{CC}$		10		pF
	Clock Duty Cycle		30		70	%
f_{CLK}	Input Clock Frequency		1		11	MHz
t_C	Conversion Time	Including S/H Acquisition Time		22		$1/f_{CLK}$
t_{ACQ}	Acquisition Time	Included in Conversion Time		2		$1/f_{CLK}$

2

ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
10-Bit D/A Converter Performance						
	Integral Linearity Error	V_{REF} = 2.5V			±3	LSB
	Differential Linearity Error	V_{REF} = 2.5V			±1	LSB
	Settling Time	V_{REF} = 2V, Settling to ±1/2LSB, ±1LSB Step 4V Step (Note 1)			2 4	µs µs
	Resolution	V_{REF} = 2.5V	10			Bits
	Zero Error				±5	LSB
	+ and – Full Scale Error	Full Scale = 4V			±10	LSB
	Output Voltage Swing	V_{REF} = 2.5V	0.25		V_{CC} – 0.25	V
	V_{REF} Input Resistance	(ML2377 only)		1		MΩ
8-Bit D/A Converter Performance						
	Integral Linearity Error	V_{REF} = 2.5V			±1	LSB
	Differential Linearity Error	V_{REF} = 2.5V			±1	LSB
	Settling Time	V_{REF} = 2V, Settling to ± 1/2LSB, ±1LSB Step 4V Step (Note 1)			2 4	µs µs
	Resolution	V_{REF} = 2.5V	8			Bits
	Zero Error				±3	LSB
	+ and – Full Scale Error				±3	LSB
	Output Voltage Range	V_{REF} = 2.5V	0.25		V_{CC} – 0.25	V
	V_{REF} Input Resistance	(ML2377 only)		1		MΩ
DC Characteristics						
I_{IL}	Logic Input Current	0 < V_{IN} < V_{CC}, MUX0-2, $\overline{START}$, $\overline{RESET}$, ALE			±100	µA
I_{IN}	Logic Input Current	0 < V_{IN} < V_{CC}			±1	µA
I_{INC}	Clock Input Current	0 < V_{IN} < V_{CC}			±200	µA
V_{IH}	Logic High		2			V
V_{IL}	Logic Low				0.8	V
$V_{(CLK)H}$	Clock High	(CLK Pin)	3.7			V
$V_{(CLK)L}$	Clock LOW	(CLK Pin)			1.8	V
I_{OFF}	Output Leakage Current	$\overline{CS}$ = V_{IH}, 0 < V_{OUT} < V_{CC}			±1	µA
V_{OL}	Output Low	I_{OL} = 2mA			0.4	V
V_{OH}	Output High	I_{OH} = –1mA	2.4			V

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (V_{REF} = 2.5V, No Output Load)						
	No Input Switching			10	20	mA
	Analog Ground Current	V_{REF} = 2.5V			10	mA
Microprocessor Interface Read Cycle Timing						
t_{ST}	$\overline{START}$ Pulse Width		100			ns
t_{AD}	Address Stable to Data Valid				55	ns
t_{AR}	Address Stable Before Read		5			ns
t_{RA}	Address Hold After Read		5			ns
t_{RR}	Read Pulse Width		50			ns
t_{RD}	Data Valid from Read				55	ns
t_{DF}	Read to Data Float	(Note 1)			20	ns
t_{RV}	Recovery Time Between Reads		25			ns
Microprocessor Interface Write Cycle Timing						
t_{AW}	Address Stable Before Write		5			ns
t_{WA}	Address Hold After Write		5			ns
t_{WW}	Write Pulse Width		50			ns
t_{DS}	Data Valid Before Write		30			ns
t_{DH}	Data Hold After Write		15			ns
t_{RV}	Recovery Time Between Writes		25			ns
Microprocessor Interface Interrupt and Busy Timing						
t_{CI}	Clock to Interrupt Active				100	ns
t_{RI}	Read to Interrupt Inactive				100	ns
t_{CB}	Clock to Busy Active	(ML2377 Only)			100	ns
t_{CB}	Clock to Busy Inactive	(ML2377 Only)			100	ns

Note 1: Guaranteed by characterization and/or correlation to other test.

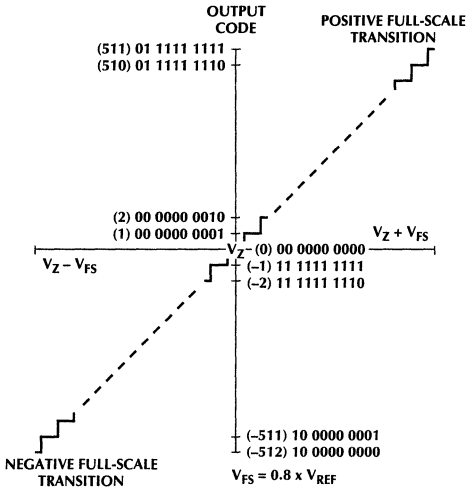


Figure 1. Transfer Characteristics

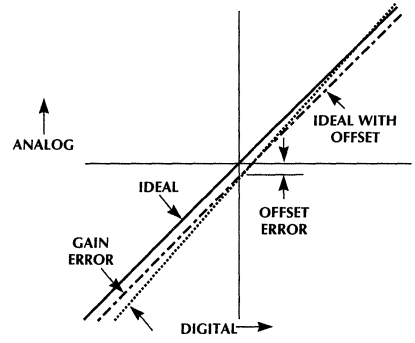


Figure 2. Gain and Offset Error

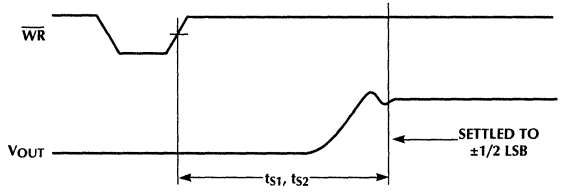


Figure 3. Settling Time

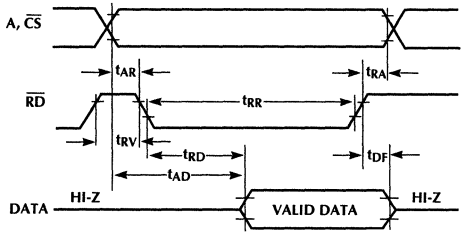


Figure 4. Read Cycle Timing

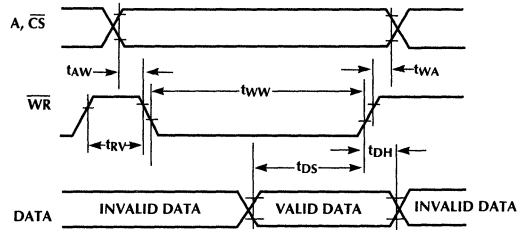


Figure 5. Write Cycle Timing

FUNCTIONAL DESCRIPTION

DEVICE TYPES

The family consists of two different devices:

1) The ML2375
   It is a 28 pin device that contains the basic 10-bit A/D converier, 10-bit D/A converter, 8-bit D/A converter and a 4 channel multiplexer.

2) The ML2377
   It is a 6 channel version of ML2375. In addition, the BUSY, INT and multiplexer control pins are also available to the user.

ANALOG INPUT AND OUTPUT VOLTAGES

The ML2375 and ML2377 allow the analog input and output voltages to be referenced to a common point. Thus, the input voltage swing and the offset of the ADC and the output voltage swing and the offset of the DAC can be defined by the voltage applied at the commons, VZ_{AD1}, VZ_{AD2}, VZ_{DA10} and VZ_{DA8}.

The voltage at the common for the 10-bit D/A converter and the 8-bit D/A converter are defined by VZ_{DA10} and VZ_{DA8} respectively. For the A/D inputs, channel 0 and 1 common are defined by VZ_{AD1}. The common of the other channels (2 to 5) may be programmed to VZ_{AD2} by setting the on-chip control register (see Table 3).

The peak full scale voltage is defined by the reference voltages.

$$V_{FS} = 0.8 \times V_{REF}$$

Figure 1 shows the transfer function of the ML2375 and ML2377 and the relationship between VZ and V_{FS}.

A/D CONVERTER OPERATION

Input Multiplexer Addressing

The input multiplexer is addressed with either the MUX0 to MUX2 pins or the internal multiplexer address register. The MUX0 to MUX2 pins are not latched, and control the addressing of the multiplexer directly. If control of the multiplexer is to be done from the microprocessor addressable mux control register, then all MUX pins should be tied to a logic high. This condition, which is an illegal mux address, will then route control of the multiplexer addressing to the internal register, which is under microprocessor control.

ML2375 multiplexer can only be addressed via its on-chip multiplexer register.

Simultaneous Sample/Hold Function

The simultaneous sample/hold function is only available on channels 0 and 1. When addressing channel 0 or 1 with the external MUX pins or the internal register bits and starting a conversion, both channels will be sampled and held simultaneously. Two conversions will then proceed back to back, with the BUSY pin and status bit going active for two conversion times. The INT pin and status bit will go active after the completion of the first conversion. A read of the data register will then clear the INT pin and status bit. After the second conversion is completed, the INT pin and status bit will go active again, indicating the need for a read of the second result from the data register. If, however, the results of the first register are not read after the first conversion and before the second conversion, the INT pin and status bit remain active until the completion of the second conversion. The results of the first conversion remain in the data register, with the results of the second conversion stored in a holding register. After completion of the second conversion, which is indicated by the BUSY status bit or pin going inactive, both results can be obtained by successive reads of the data register. The INT pin and status bit are then cleared by the act of the second data register read.

D/A CONVERTER OPERATION

The D/A converters are updated beginning on the rising edge of the $\overline{WR}$ pin. Settling time is measured from this point.

Microprocessor Interface

The ML2375 is presented as four 10-bit registers to the microprocessor. These registers are addressed via the address pins A0 and A1. The register map below describes the four registers.

Converter Registers

Table 1. A/D Converter Register

ADDRESS 00

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data Bit	9	8	7	6	5	4	3	2	1	0
	Sign	MSB								LSB

Table 2. D/A Converter Register

ADDRESS 01

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/A 10	9	8	7	6	5	4	3	2	1	0
	Sign	MSB								LSB

ADDRESS 10

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/A 8	7	6	5	4	3	2	1	0		
	Sign	MSB						LSB	0	0

REGISTER DESCRIPTIONS

Register Address 00

This register holds the results of the 10-bit A/D conversion results when read. The converted results are in 2's complement form, where 0 is the potential at the common pin. Reading of this register also clears the INT status bit and the deasserts the INT pin on the falling edge of the $\overline{RD}$ pin.

Register Address 01

When written, it receives the 10-bit digital value for the 10-bit D/A converter. All codes are in 2's complement form, where the 0 code indicates the potential at the VZ_{DA10} or VZ/V_{REF} pin. This register can also be read, which returns the previously written value.

Register Address 10

This register receives the 8-bit digital value for the 8-bit D/A converter. This value is also in 2's complement format. When read, it returns the previously written value. 8-bit data in this 10-bit register is left justified.

Control Register

This is the control register. Functions such as A/D conversion start, multiplexer control, and A/D converter status are included.

D9 When VZ_5 = 1, Channel 5 common = VZ_{AD2}

D8 When VZ_4 = 1, Channel 4 common = VZ_{AD2}

D7 When VZ_3 = 1, Channel 3 common = VZ_{AD2}

D6 When VZ_2 = 1, Channel 2 common = VZ_{AD2}

D5 INT. It is equivalent to the INT pin. It provides indication that a conversion is completed.

D4 BUSY. This bit is A/D converter status bit which provides indication that a conversion is in progress. It is equivalent to the BUSY pin of the ML2377.

D3 $\overline{START}$. This bit has the same function as the $\overline{START}$ pin. When this bit receives a 1, it will start a conversion. After the conversion has started, this bit is cleared after 4 clock cycles.

D2 MUX2. MUX address bit 2.

D1 MUX1. MUX address bit 1.

D0 MUX0. MUX address bit 0.

CHIP RESET

The chip is reset when a 0 is presented to the $\overline{RESET}$ pin. All registers are reset to 0. Therefore, the D/A and the A/D converters are all at zero scale and the multiplexer select is addressed to channel 0. Additionally, VZ_2–VZ_5 are cleared in the control register.

Table 3. Control Register

ADDRESS 11

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ML2375	0	0	0	0	INT	BUSY	START	0	MUX1	MUX0
ML2377	VZ_5	VZ_4	VZ_3	VZ_2	INT	BUSY	START	MUX2	MUX1	MUX0

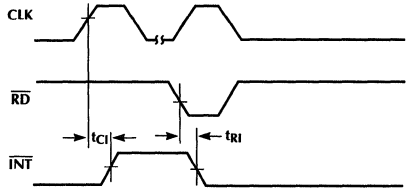


Figure 6. Interrupt Timing, ML2375, and ML2377

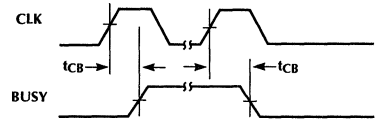


Figure 7. BUSY Timing, ML2377

ORDERING INFORMATION

PART NUMBER	PACKAGE	GRADE	COMMENTS
ML2375BCP	28-Pin DIP (P28)	B	Multiplex Address and Data Bus
ML2375CCP	28-Pin DIP (P28)	C	
ML2375BCQ	28-Pin PLCC (Q28)	B	
ML2375CCQ	28-Pin PLCC (Q28)	C	
ML2375BCR	28-Pin SSOP (R28)	B	
ML2375CCR	28-Pin SSOP (R28)	C	
ML2377BCQ	44-Pin PLCC (Q44)	B	Additional Analog Inputs, Individual V_{REF} and V_{ZS}
ML2377CCQ	44-Pin PLCC (Q44)	C	
ML2377BCH	44-Pin TQFP (H44)	B	
ML2377CCH	44-Pin TQFP (H44)	C	
ML2377BCG	44-Pin QFP (G44)	B	
ML2377CCG	44-Pin QFP (G44)	C	

Telecommunications

Section 3

Gain/Attenuators

Part Number	Gain Range (dB)	Resolution (dB Steps)	Noise (dBrnc @ Max Gain)	Harmonic Distortion (dB)	Digital Interface	Power Supplies (V)	Temperature Range C	Temperature Range I	Package
ML2003	–24 to +24	0.1	0	–60	Serial, Hard Wire	±5	X	X	18-Pin DIP 20-Pin PLCC
ML2004	–24 to +24	0.1	0	–60	Serial	±5	X	X	14-Pin DIP
ML2008	–24 to +24	0.1	0	–60	8-Bit µP	±5	X	X	18-Pin DIP 20-Pin PLCC
ML2009	–24 to +24	0.1	0	–60	16-Bit µP	±5	X	X	18-Pin DIP 20-Pin PLCC

Equalizers

Part Number	Frequency Response Adjustable	Idle Channel Noise (dBrnc)	Harmonic Distortion (dB)	Comment	Interface Interface	Power Supplies (V)	Temperature Range C	Temperature Range I	Package
ML2020	Slope, Height Bandwidth	8	–48	60Hz Rejection	Serial	±5	X	X	16-Pin DIP 18-Pin SOIC
ML2021	Slope, Height Bandwidth	8	–48	Group Delay Optimized	Serial	±5	X	X	16-Pin DIP 18-Pin SOIC

Tone Detectors

Part Number	Detect Frequency (Hz)	Dynamic Range Detect (dBm)	Frequency Template (Hz)	Comment	Power Supplies (V)	Temperature Range C	Temperature Range I	Package
ML2031	1K to 4K	–34 to +6	Detect ±10 No Detect ±36	Exceed Bell Pub 43004 Clock Outputs of CLK_{IN} ÷2, ÷8	±5	X	X	8-Pin DIP
ML2032	1K to 4K	–34 to +6	Detect ±10 No Detect ±36	Exceed Bell Pub 43004 Uncommitted Op Amp	±5	X	X	8-Pin DIP

Programmable Sinewave Generators

Part Number	Frequency Range (Hz)	Min Resolution (Hz)	Gain Error (dB)	Harmonic Distortion (dB)	Comment	Digital Interface	Power Supplies (V)	Temperature Range C	Temperature Range I	Package
ML2035	DC to 25K	±0.75	±0.1	–45	Voltage Amplitude $V_{CC}/2$	Serial	±5	X	X	8-Pin DIP
ML2036	DC to 50K	±0.75	±0.1	–45	Adj. Voltage Amplitude, Clock Outputs of CLK_{IN} ÷2, ÷8	Serial	±5	X	X	14-Pin DIP 16-Pin SOIC

Switched Capacitor Filters

Part Number	No. of Sections	f_O Range (Hz)	f_O/f_{CLK} Ratio	f_O Tempco (ppm/°C)	Power Supplies (V)	Temp. Range C	Temp. Range I	Package
ML2110	2	25 to 30K	100, 50:1	20	±2.5 to ±5	X	X	20-Pin DIP 20-Pin SOIC
ML2111	2	25 to 150K	100, 50:1	20	±2.5 to ±5	X	X	20-Pin DIP 20-Pin SOIC

Logarithmic Gain/Attenuator

GENERAL DESCRIPTION

The ML2003 and ML2004 are digitally controlled logarithmic gain/attenuators with a range of -24 to +24dB in 0.1dB steps.

The gain settings are selected by a 9-bit digital word. The ML2003 digital interface is either parallel or serial. The ML2004 is packaged in a 14-pin DIP with a serial interface only.

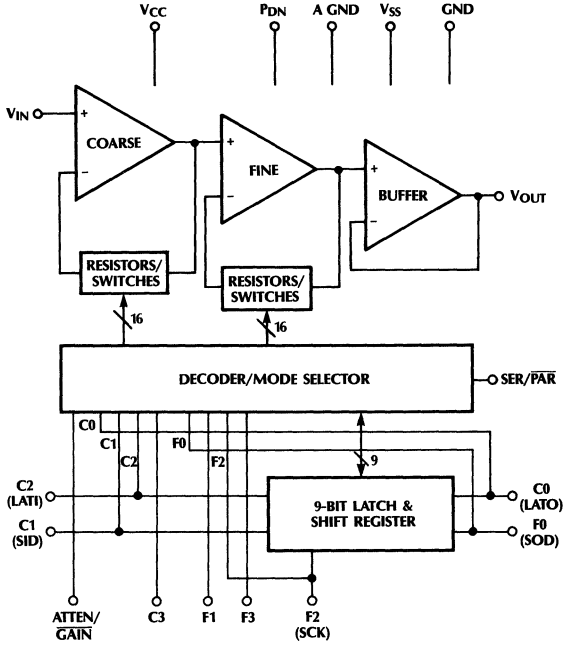
Absolute gain accuracy is 0.05dB max over supply tolerance of ±10% and temperature range.

These CMOS logarithmic gain/attenuators are designed for a wide variety of applications in telecom, audio, sonar, or general purpose function generation. One specific intended application is analog telephone lines.

FEATURES

- Low noise 0 dBrnc max with +24dB gain
- Low harmonic distortion -60dB max
- Gain range -24 to +24dB
- Resolution 0.1dB steps
- Flat frequency response ±.05dB from .3-4kHz
  ±.10dB from .1-20kHz
- Low supply current 4mA max from ±5V supplies
- TTL/CMOS compatible digital interface
- ML2003 has pin selectable serial or parallel interface; ML2004 serial interface only
- Standard 14-pin or 18-pin 0.3" center DIP or 20-pin molded chip carrier package

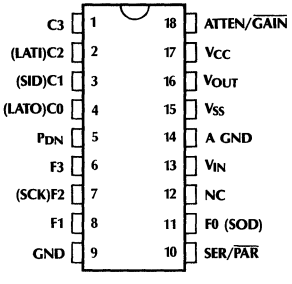
BLOCK DIAGRAM



NOTE: SERIAL MODE FUNCTIONS INDICATED BY PARENTHESES.

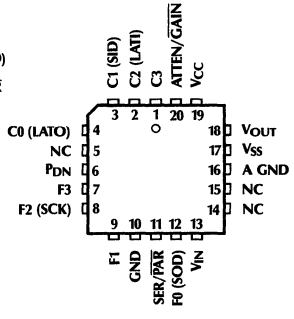
PIN CONNECTIONS

ML2003 18-PIN DIP



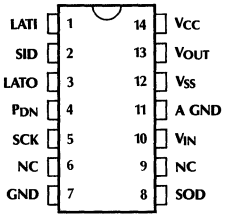
TOP VIEW

ML2003 20-PIN PCC



TOP VIEW

ML2004 14-PIN DIP



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
C3	In serial mode, pin is unused. In parallel mode, coarse gain select bit. Pin has internal pulldown resistor to GND.
(LATI) C2	In serial mode, input latch clock which loads the data from the shift register into the latch. In parallel mode, coarse gain select bit. Pin has internal pulldown resistor to GND.
(SID) C1	In serial mode, serial data input that contains serial 9 bit data word which controls the gain setting. In parallel mode, coarse gain select bit. Pin has internal pulldown resistor to GND.
(LATO) C0	In serial mode, output latch clock which loads the 9 bit data word back into the shift register from the latch. In parallel mode, coarse gain select bit. Pin has internal pulldown resistor to GND.
P_{DN}	Powerdown input. When P_{DN} = 1, device is in powerdown mode. When P_{DN} = 0, device is in normal operation. Pin has internal pulldown resistor to GND.
F3	In serial mode, pin is unused. In parallel mode, fine gain select bit. Pin has internal pulldown resistor to GND.
(SCK) F2	In serial mode, shift register clock which shifts the serial data on SID into the shift register on rising edges and out on SOD on falling edges. In parallel mode, fine gain select bit. Pin has internal pulldown resistor to GND.

NAME	FUNCTION
F1	In serial mode, pin is unused. In parallel mode, fine gain select bit. Pin has internal pulldown resistor to GND.
GND	Digital ground. 0 volts. All digital inputs and output are referenced to this ground.
SER/$\overline{PAR}$	Serial or parallel select input. When SER/$\overline{PAR}$ = 1, device is in serial mode. When SER/$\overline{PAR}$ = 0, device is in parallel mode. Pin has internal pullup resistor to V_{CC}.
(SOD) F0	In serial mode, serial output data which is the output of the shift register. In parallel mode, fine gain select bit. Pin has internal pulldown resistor to GND.
V_{IN}	Analog input.
AGND	Analog ground. 0 volts. Analog input and output are referenced to this ground.
V_{SS}	Negative supply. -5 volts ±10%.
V_{OUT}	Analog output.
V_{CC}	Positive supply. +5 volts ±10%.
ATTEN/$\overline{GAIN}$	In serial mode, pin is unused. In parallel mode, attenuation/gain select bit. Pin has internal pulldown resistor to GND.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage
- V_{CC} ..... +6.5V
- V_{SS} ..... -6.5V

AGND with respect to GND ..... ±.5V
Analog Input and Output ..... V_{SS} - 0.3V to V_{CC} + 0.3V
Digital Inputs and Outputs ..... GND - 0.3V to V_{CC} + 0.3V
Input Current Per Pin ..... ±25mA
Power Dissipation 750mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2003CP, ML2004CP, ML2004CQ ..... 0°C to +70°C
- ML2003IJ, ML2004IJ ..... -40°C to +85°C

Supply Voltage
- V_{CC} ..... 4V to 6V
- V_{SS} ..... -4V to -6V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ±10%, V_{SS} = -5V ±10%, Data Word: ATTEN/$\overline{GAIN}$ = 1, Other Bits = 0 (0dB Ideal Gain), C_L = 100pF, R_L = 600Ω, SCK = LATI = LATO = 0, dBm measurements use 600Ω as reference load, digital timing measured at 1.4V.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
Analog							
AG	Absolute gain accuracy	4	V_{IN} = 8dBm, 1kHz	-0.05		+0.05	dB
RG	Relative gain accuracy	4	100000001 000000000 000000001 All other gain settings All values referenced to 100000000 gain when ATTEN/$\overline{GAIN}$ = 1, V_{IN} = 8dBm when ATTEN/$\overline{GAIN}$ = 0, V_{IN} = (8dBm - Ideal Gain) in dB	-.05 -.05 -.05 -0.1		+.05 +.05 +.05 +0.1	dB dB dB dB
FR	Frequency response	4	300–4000Hz 100–20,000 Hz Relative to 1kHz	-0.05 -0.1		+0.05 +0.1	dB dB
VOS	Output Offset Voltage	4	V_{IN} = 0, +24dB gain			±100	mV
ICN	Idle Channel Noise	4 5	V_{IN} = 0, +24dB gain, C msg. Weighted V_{IN} = 0, +24dB gain, 1kHz		-6 450	0 900	dBrnc nv/√Hz
HD	Harmonic Distortion	4	V_{IN} = 8dBm, 1kHz Measure 2nd, 3rd harmonic relative to fundamental			-60	dB
SD	Signal to Distortion	4	V_{IN} = 8dBm, 1kHz. C msg. weighted	+60			dB
PSRR	Power Supply Rejection	4	200mV_{p-p}, 1kHz sine, V_{IN} = 0 on V_{CC} on V_{SS}		 -60 -60	 -40 -40	 dB dB
Z_{IN}	Input Impedance, V_{IN}	4		1			Meg
V_{INR}	Input Voltage Range	4		±3.0			V
V_{OSW}	Output Voltage Swing	4		±3.0			V
Digital and DC							
V_{IL}	Digital Input Low Voltage	4				.8	V
V_{IH}	Digital Input High Voltage	4		2.0			V
V_{OL}	Digital Output Low Voltage	4	I_{OL} = 2mA			.4	V
V_{OH}	Digital Output High Voltage	4	I_{OH} = -1mA	4.0			V
I_{NS}	Input Current, SER/$\overline{PAR}$	4	V_{IH} = GND	-5		-100	μA
I_{ND}	Input Current, All Digital Inputs Except SER/$\overline{PAR}$	4	V_{IH} = V_{CC}	5		100	μA
I_{CC}	V_{CC} Supply Current	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}, V_{IN} = 0			4	mA
I_{SS}	V_{SS} Supply Current	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}, V_{IN} = 0			-4	mA
I_{CCP}	V_{CC} Supply Current, Powerdown Mode	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}			.5	mA
I_{SSP}	V_{SS} Supply Current Powerdown Mode	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}			-.1	mA

3

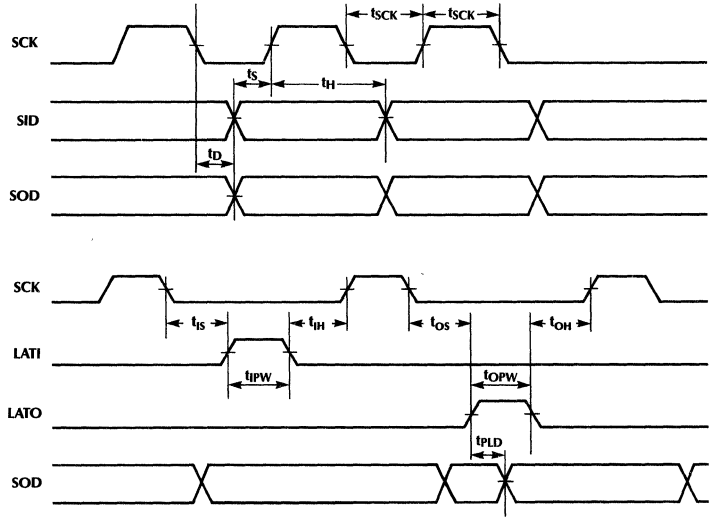
ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ±10%, V_{SS} = -5V ±10%, Data Word: ATTEN/$\overline{GAIN}$ = 1, Other Bits = 0 (0dB Ideal Gain), C_L = 100pF, R_L = 600Ω, SCK = LATI = LATO = 0, dBm measurements use 600Ω as reference load, digital timing measured at 1.4V. C_L = 100pF or SOD.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
AC Characteristics							
t_{SET}	V_{OUT} Settling Time	4	V_{IN} = 0.185V. Change gain from -24 to +24dB. Measure from LATI rising edge to when V_{OUT} settles to within 0.05dB of final value.			20	µs
t_{STEP}	V_{OUT} Step Response	4	Gain = +24dB. V_{IN} = -0.185V to +0.185V step. Measured when V_{OUT} settles to within 0.05dB of final value.			20	µs
t_{SCK}	SCK On/Off Period	4		250			ns
t_S	SID Data Setup Time	4		50			ns
t_H	SID Data Hold Time	4		50			ns
t_D	SOD Data Delay	4		0		125	ns
t_{IPW}	LATI Pulse Width	4		50			ns
t_{OPW}	LATO Pulse Width	4		50			ns
t_{IS}, t_{OS}	LATI, LATO Setup Time	4		50			ns
t_{IH}, t_{OH}	LATI, LATO Hold Time	5		50			ns
t_{PLD}	SOD Parallel Load Delay	4		0		125	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: 0°C to 70°C and -40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.
Note 3: Typicals are parametric norm at 25°C.
Note 4: Parameter guaranteed and 100% production tested.
Note 5: Parameter guaranteed. parameters not 100% tested are not in outgoing quality level calculation.

TIMING DIAGRAM



TIMING PARAMETERS ARE REFERENCED TO THE 1.4 VOLT MIDPOINT.

Figure 1. Serial Mode Timing Diagram

TYPICAL PERFORMANCE CURVES

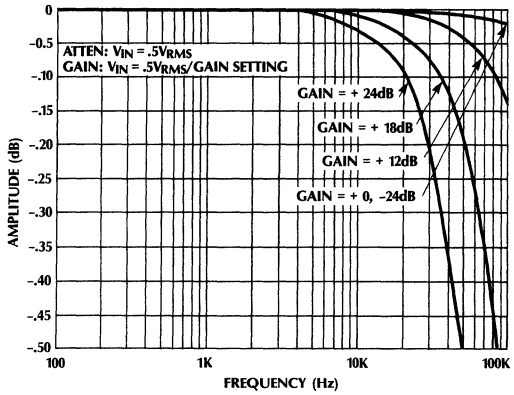


Figure 2. Amplitude vs Frequency (V_{IN}/V_{OUT} = .5V_{RMS})

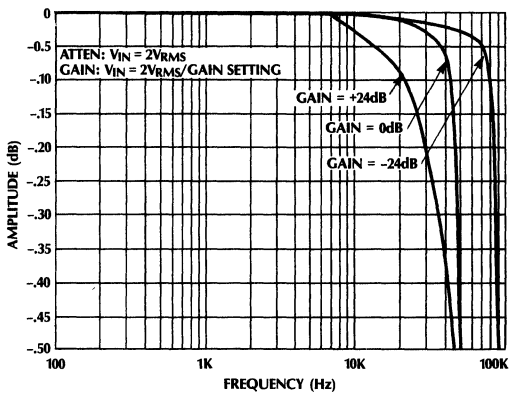


Figure 3. Amplitude vs Frequency (V_{IN}/V_{OUT} = 2V_{RMS})

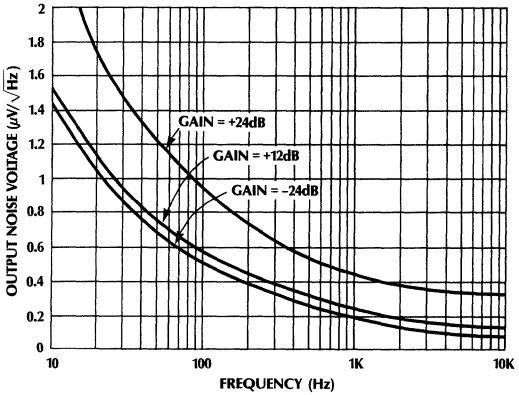


Figure 4. Output Noise Voltage vs Frequency

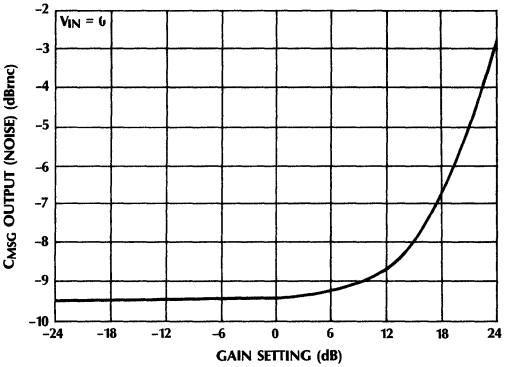


Figure 5. C_{MSG} Output Noise vs Gain Setting

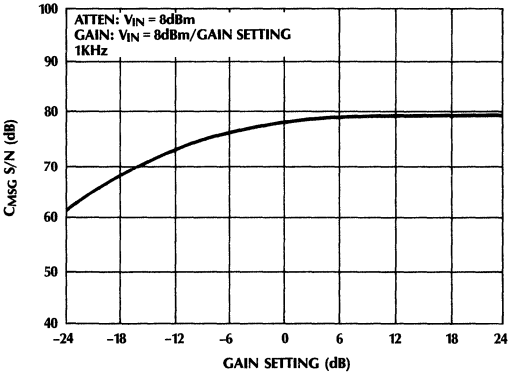


Figure 6. C_{MSG} S/N vs Gain Setting

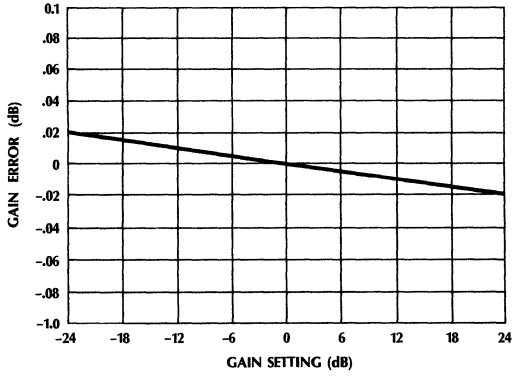


Figure 7. Gain Error vs Gain Setting

TYPICAL PERFORMANCE CURVES (Continued)

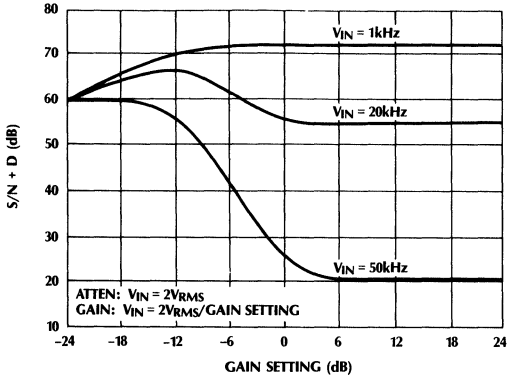


Figure 8. S/N + D vs Gain Setting (V_{IN}/V_{OUT} = $2V_{RMS}$)

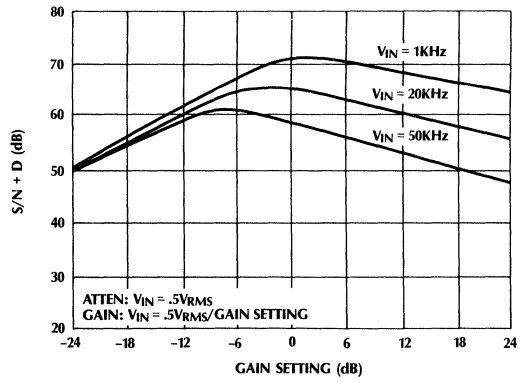


Figure 9. S/N + D vs Gain Setting (V_{IN}/V_{OUT} = $.5V_{RMS}$)

1.0 FUNCTIONAL DESCRIPTION

The ML2003 consists of a coarse gain stage, a fine gain stage, an output buffer, and a serial/parallel digital interface.

1.1 Gain Stages

The analog input, V_{IN}, goes directly into the op amp input in the coarse gain stage. The coarse gain stage has a gain range of 0 to 22.5dB in 1.5dB steps.

The fine gain stage is cascaded onto the coarse section. The fine gain stage has a gain range of 0 to 1.5dB in 0.1dB steps.

In addition, both sections can be programmed for either gain or attenuation, thus doubling the effective gain range.

The logarithmic steps in each gain stage are generated by placing the input signal across a resistor string of 16 series resistors. Analog switches allow the voltage to be tapped from the resistor string at 16 points. The resistors are sized such that each output voltage is at the proper logarithmic ratio relative to the input signal at the top of the string. Attenuation is implemented by using the resistor string as a simple voltage divider, and gain is implemented by using the resistor string as a feedback resistor around an internal op amp.

1.2 Gain Settings

Since the coarse and fine gain stages are cascaded, their gains can be summed logarithmically. Thus, any gain from -24dB to +24dB in 0.1dB steps can be obtained by combining the coarse and fine gain settings to yield the desired gain setting. The relationship between the digital select bits and the corresponding analog gain values is shown in Tables 1 and 2. Note that C3-C0 selects the coarse gain, F3-F0 selects the fine gain, and ATTEN/GAIN selects either attenuation or gain.

1.3 Output Buffer

The final analog stage is the output buffer. This amplifier has internal gain of 1 and is designed to drive 600 ohms and 100pF loads. Thus, it is suitable for driving a telephone hybrid circuit directly without any external amplifier.

1.4 Power Supplies

The digital section is powered between V_{CC} and GND, or 5 volts. The analog section is powered between V_{CC} and V_{SS} and uses AGND as the reference point, or ±5 volts.

GND and AGND are totally isolated inside the device to minimize coupling from the digital section into the analog section. However, AGND and GND should be tied together physically near the device and ideally close to the common power supply ground connection.

Typically, the power supply rejection of V_{CC} and V_{SS} to the analog output is greater than -60dB at 1kHz. If decoupling of the power supplies is still necessary in a system, V_{CC} and V_{SS} should be decoupled with respect to AGND.

FUNCTIONAL DESCRIPTION (Continued)

Table 1. Fine Gain Settings (C3–C0 = 0)

F3	F2	F1	F0	Ideal Gain (dB) ATTEN/GAIN = 1	Ideal Gain (dB) ATTEN/GAIN = 0
0	0	0	0	.0	.0
0	0	0	1	–.1	.1
0	0	1	0	–.2	.2
0	0	1	1	–.3	.3
0	1	0	0	–.4	.4
0	1	0	1	–.5	.5
0	1	1	0	–.6	.6
0	1	1	1	–.7	.7
1	0	0	0	–.8	.8
1	0	0	1	–.9	.9
1	0	1	0	–1.0	1.0
1	0	1	1	–1.1	1.1
1	1	0	0	–1.2	1.2
1	1	0	1	–1.3	1.3
1	1	1	0	–1.4	1.4
1	1	1	1	–1.5	1.5

Table 2. Coarse Gain Settings (F3–F0 = 0)

C3	C2	C1	C0	Ideal Gain (dB) ATTEN/GAIN = 1	Ideal Gain (dB) ATTEN/GAIN = 0
0	0	0	0	.0	.0
0	0	0	1	–1.5	1.5
0	0	1	0	–3.0	3.0
0	0	1	1	–4.5	4.5
0	1	0	0	–6.0	6.0
0	1	0	1	–7.5	7.5
0	1	1	0	–9.0	9.0
0	1	1	1	–10.5	10.5
1	0	0	0	–12.0	12.0
1	0	0	1	–13.5	13.5
1	0	1	0	–15.0	15.0
1	0	1	1	–16.5	16.5
1	1	0	0	–18.0	18.0
1	1	0	1	–19.5	19.5
1	1	1	0	–21.0	21.0
1	1	1	1	–22.5	22.5

1.5 Powerdown Mode

A powerdown mode can be selected with pin P_{DN}. When P_{DN} = 1, the device is powered down. In this state, the power consumption is reduced by removing power from the analog section and forcing the analog output, V_{OUT}, to a high impedance state. While the device is in powerdown mode, the digital section is still functional and the current data word remains stored in the latch when in serial mode. When P_{DN} = 0, the device is in normal operation.

1.6 Digital Section

The ML2003 can be operated with a serial or parallel interface. The SER/PAR pin selects the desired interface. When SER/PAR = 1, the serial mode is selected. When SER/PAR = 0, the parallel mode is selected. The ML2004 digital interface is serial only.

1.6.1 Serial Mode

Serial mode is selected by setting SER/$\overline{\text{PAR}}$ pin high. The serial interface allows the gain settings to be set from a serial data word.

The timing for the serial mode is shown in Figure 10. The serial input data, SID, is loaded into a shift register on rising edges of the shift clock, SCK. The data can be parallel loaded into a latch when the input latch signal, LATI, is high. The LATI pulse must occur when SCK is low. In this way, a new data word can be loaded into the shift register without disturbing the existing data word in the latch.

The parallel outputs of the latch control the attenuation/gain setting. The order of the data word bits in the latch is shown in Figure 11. Note that bit 0 is the first bit of the data word clocked into the shift register. Tables 1 and 2 describe how the data word programs the gain.

The device also has the capability to read out the data word stored in the latch. This can be done by parallel loading the data from the latch back into the shift register when the latch signal, LATO, is high. The LATO pulse must occur when SCK is low. Then, the data word can be shifted out of the shift register serially to the output, SOD, on falling edges of the shift clock, SCK.

The loading and reading of the data word can be done continuously or in bursts. Since the shift register and latch circuitry inside the device is static, there are no minimum frequency requirements on the clocks or data pulses. However, there is coupling (typically less than 100μV) of the digital signals into the analog section. This coupling can be minimized by clocking the data bursts in during noncritical intervals or at a frequency outside the analog frequency range.

1.6.2 Parallel Mode

The parallel mode is selected by setting SER/$\overline{\text{PAR}}$ pin low. The parallel interface allows the gain settings to be set with external switches or from a parallel microprocessor interface.

In parallel mode, the shift register and latch are bypassed and connections are made directly to the gain select bits with external pins ATTEN/GAIN, C3–C0, and F3–F0. Tables 1 and 2 describe how these pins program the gain. The pins ATTEN/GAIN, C3–C0, and F3–F0 have internal pulldown resistors to GND. The typical value of these pulldown resistors is 100kΩ.

FUNCTIONAL DESCRIPTION (Continued)

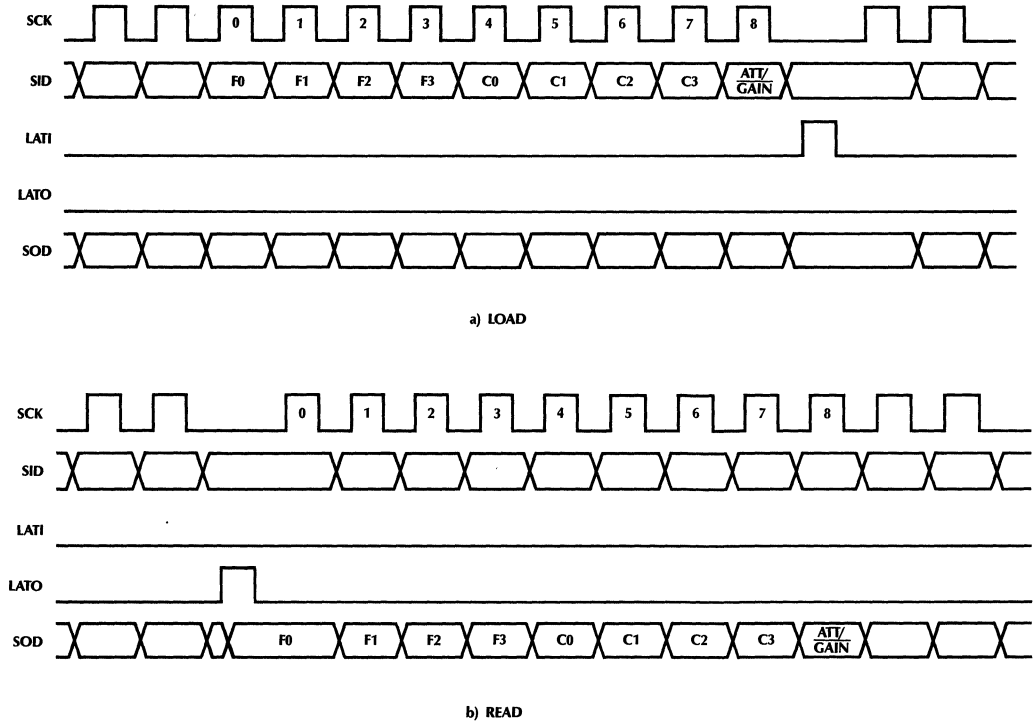


Figure 10. Serial Mode Timing

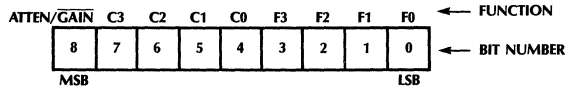


Figure 11. 9-Bit Latch

APPLICATIONS

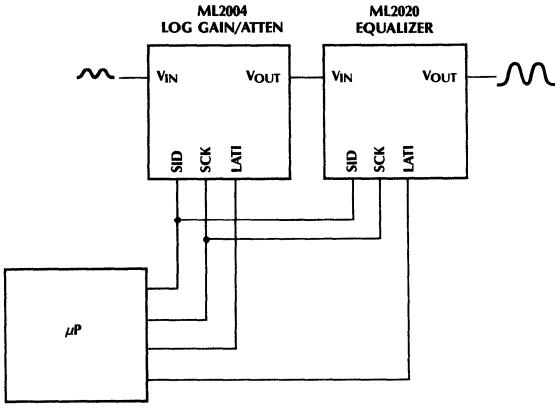


Figure 12. Typical Serial Interface

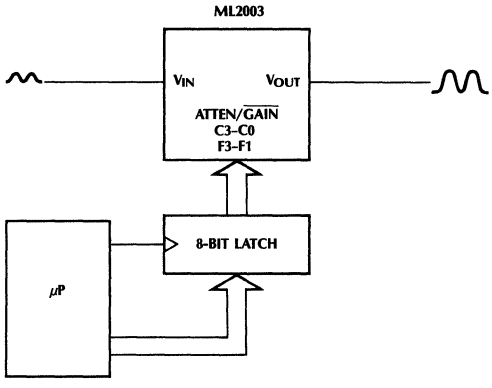


Figure 13. Typical μP Parallel Interface

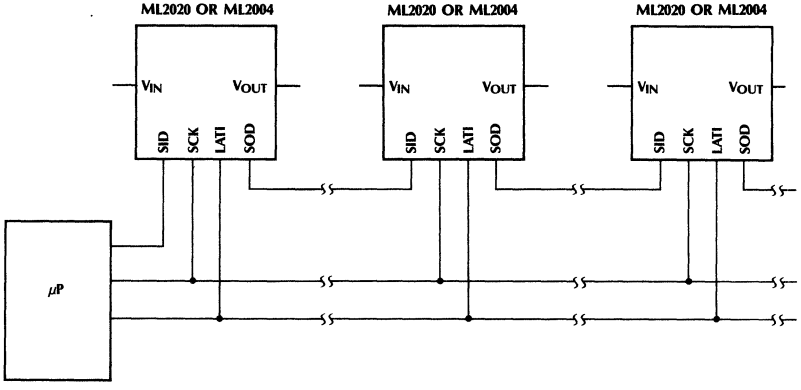


Figure 14. Controlling Multiple ML2020 and ML2004 With Only 3 Digital Lines Using One Long Data Word

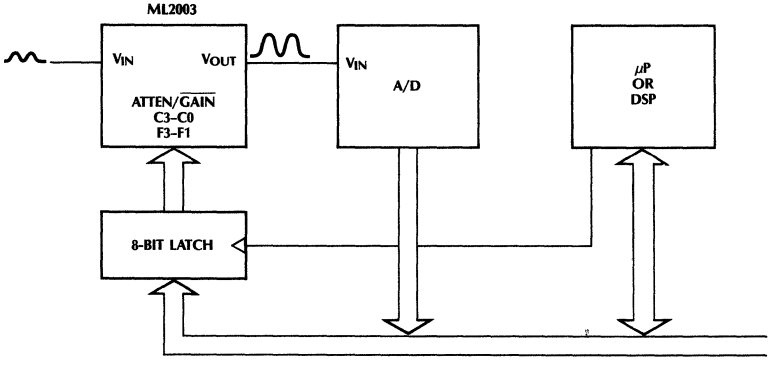


Figure 15. AGC For DSP Or Modem Front End

APPLICATIONS (Continued)

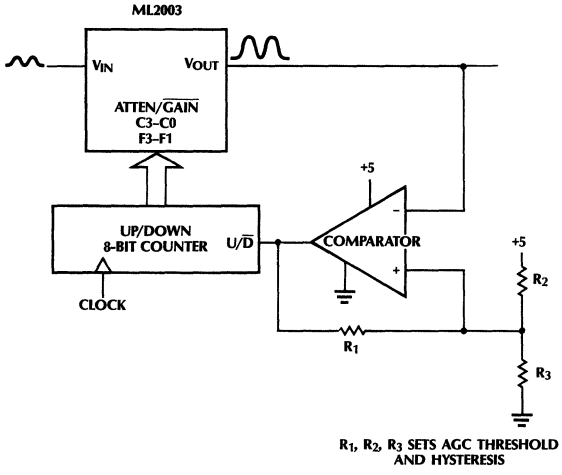


Figure 16. Analog AGC

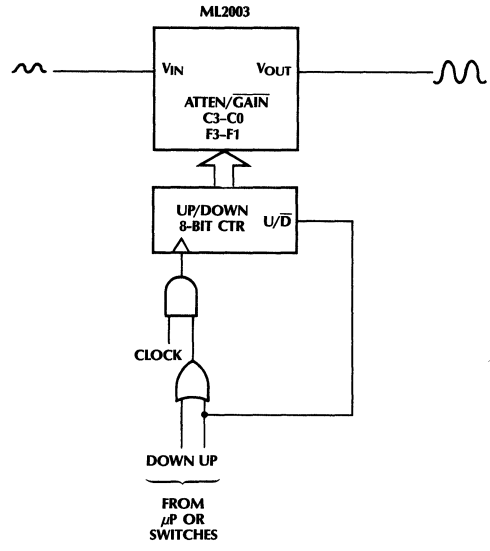


Figure 17. Digitally Controlled Volume Control

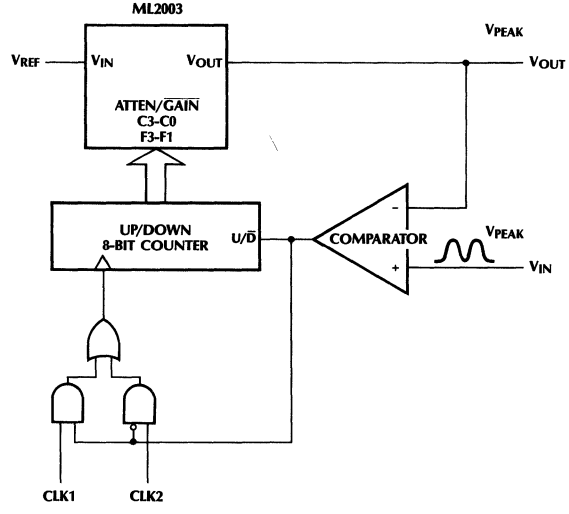


Figure 18. Precision Peak Detector (±1%) with Controllable Acquire and Hold Times

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML2003IJ	–40°C to +85°C	HERMETIC DIP (J18)
ML2003IP	–40°C to +85°C	MOLDED DIP (P18)
ML2003IQ	–40°C to +85°C	MOLDED PCC (Q20)
ML2003CP	0°C to +70°C	MOLDED DIP (P18)
ML2003CQ	–40°C to +85°C	MOLDED PCC (Q20)
ML2004IJ	–40°C to +85°C	HERMETIC DIP (J14)
ML2004IP	–40°C to +85°C	MOLDED DIP (P14)
ML2004CP	0°C to +70°C	MOLDED DIP (P14)

Micro Linear

ML2008, ML2009

µP Compatible Logarithmic Gain/Attenuator

GENERAL DESCRIPTION

The ML2008 and ML2009 are digitally controlled logarithmic gain/attenuators with a range of –24 to +24dB in 0.1dB steps.

Easy interface to microprocessors is provided by an input latch and control signals consisting of chip select and write.

The interface for gain setting of the ML2008 is by an 8-bit data word, while the ML2009 is designed to interface to a 16-bit data bus with a single write operation by hard-wiring the gain/attenuation pin or LSB pin. The ML2008 can be power downed by the microprocessor utilizing a bit in the second write operation.

Absolute gain accuracy is 0.05dB max over supply tolerance of ±10% and temperature range.

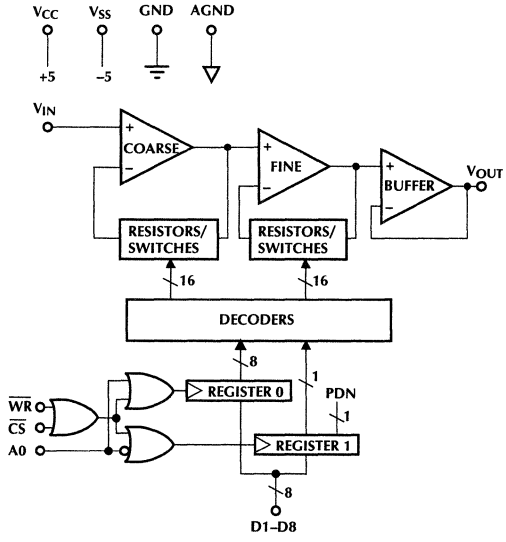
These CMOS logarithmic gain/attenuators are designed for a wide variety of applications in telecom, audio, sonar or general purpose function generation.

FEATURES

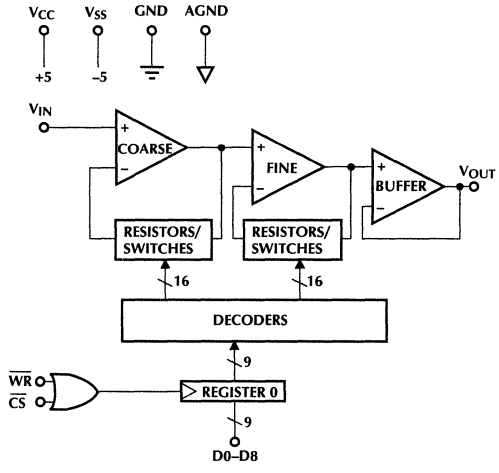
- Low noise 0dBrnc max with +24dB gain
- Low harmonic distortion –60dB max
- Gain range –24 to +24dB
- Resolution 0.1dB steps
- Flat frequency response ±0.05dB from 0.3-4kHz
±0.10dB from 0.1-20kHz
- Low supply current 4mA max from ±5V supplies
- TTL/CMOS compatible digital interface
- ML2008 is designed to interface to an 8-bit data bus; ML2009 to 16-bit data bus
- Standard 18-pin 0.3" center DIP or 20-pin molded chip carrier package

BLOCK DIAGRAM

ML2008

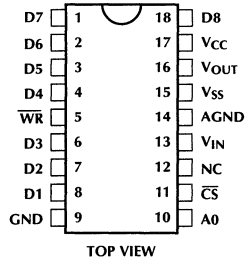


ML2009



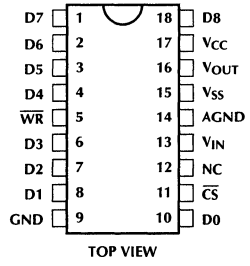
PIN CONFIGURATION

ML2008
18-Pin DIP (P18)



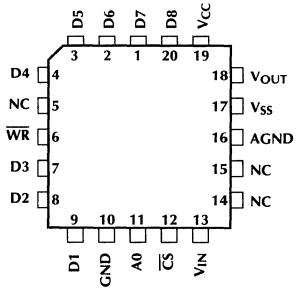
TOP VIEW

ML2009
18-Pin DIP (P18)



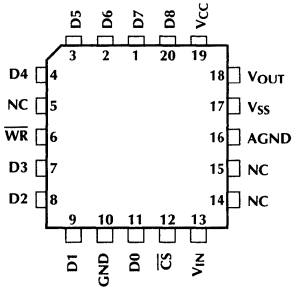
TOP VIEW

20-Pin PLCC (Q20)



TOP VIEW

20-Pin PLCC (Q20)



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
V_{SS}	Negative supply. –5Volts ±10%
V_{CC}	Positive supply. 5Volts ±10%
GND	Digital ground. 0Volts. All digital inputs are referenced to this ground.
AGND	Analog ground. 0Volts. Analog input and output are referenced to this ground.
V_{IN}	Analog input
V_{OUT}	Analog output
D8	Data bit, ATTEN/$\overline{GAIN}$
D7	Data bit, C3
D6	Data bit, C2
D5	Data bit, C1
D4	Data bit, C0
D3	Data bit, F3
D2	Data bit, P_{DN}, F2 ML2008; F2 ML2009
D1	Data bit, F0, F1 ML2008; F1 ML2009
D0	Data bit, F0 ML2009 only
$\overline{WR}$	Write enable. This input latches the data bits into the registers on rising edges of $\overline{WR}$.
$\overline{CS}$	Chip select. This input selects the device by only allowing the $\overline{WR}$ signal to latch in data when $\overline{CS}$ is low.
A0 (ML2008 only)	Address select. This input determines which data word is being written into the registers.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} ..... +6.5V
- V_{SS} ..... –6.5V
- AGND with Respect to GND ..... V_{CC} to V_{SS}
- Analog Inputs and Outputs ..... V_{SS} –0.3V to V_{CC} +0.3V
- Digital Inputs and Outputs ... GND –0.3V to V_{CC} +0.3V
- Input Current Per Pin ..... ±25mA
- Power Dissipation 750mW
- Storage Temperature Range ..... –65°C to +150°C
- Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2008CP, ML2009CP ..... 0°C to +70°C
- ML2008CQ, ML2009CQ ..... 0°C to +70°C
- ML2008IJ, ML2009IJ ..... –40°C to +85°C

Supply Voltage
- V_{CC} ..... 4V to 6V
- V_{SS} ..... –4V to –6V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ±10%, V_{SS} = –5V ±10%, Data Word: D8 (ATTEN/$\overline{GAIN}$) = 1, Other Bits = 0, (0dB Ideal Gain), C_L = 100pF, R_L = 600Ω, dBm measurements use 600Ω as reference load, digital timing measured at 1.4V.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
Analog							
AG	Absolute Gain Accuracy	4	V_{IN} = 8dBm, 1kHz	–0.05		+0.05	dB
RG	Relative Gain Accuracy	4	100000001 000000000 000000001 All other gain settings All values referenced to 100000000 gain when D8 (ATTEN/$\overline{GAIN}$) = 1, V_{IN} = 8dBm when D8 (ATTEN/$\overline{GAIN}$) = 0, V_{IN} = (8dBm – Ideal Gain) in dB	–0.05 –0.05 –0.05 –0.1		+0.05 +0.05 +0.05 +0.1	dB dB dB dB
FR	Frequency Response	4	300-4000Hz 100-20,000Hz Relative to 1kHz	–0.05 –0.1		+0.05 +0.1	dB dB
V_{OS}	Output Offset Voltage	4	V_{IN} = 0, +24dB gain			±100	mV
I_{CN}	Idle Channel Noise	4 5	V_{IN} = 0, +24dB, C msg weighted V_{IN} = 0, +24dB, 1kHz		–6 450	0 900	dBrnc nv/$\sqrt{Hz}$
HD	Harmonic Distortion	4	V_{IN} = 8dBm, 1kHz Measure 2nd, 3rd, harmonic relative to fundamental			–60	dB
SD	Signal to Distortion	4	V_{IN} = 8dBm, 1kHz C msg weighted	+60			dB
PSRR	Power Supply Rejection	4	200mV_{P-P}, 1kHz sine, V_{IN} = 0 on V_{CC} on V_{SS}		 –60 –60	 –40 –40	 dB dB
Z_{IN}	Input Impedance, V_{IN}	4		1			Meg
V_{INR}	Input Voltage Range	4		±3.0			V
V_{OSW}	Output Voltage Swing	4		±3.0			V

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
Digital and DC							
V_{IL}	Digital Input Low Voltage	4				0.8	V
V_{IH}	Digital Input High Voltage	4		2.0			V
I_{IN}	Input Current, Low	4	V_{IH} = GND			–10	µA
I_{IN}	Input Current, High	4	V_{IH} = V_{CC}			10	µA
I_{CC}	V_{CC} Supply Current	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}, V_{IN} = 0			4	mA
I_{SS}	V_{SS} Supply Current	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}, V_{IN} = 0			–4	mA
I_{CCP}	V_{CC} Supply Current, ML2008 Powerdown Mode Only	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}			0.5	mA
I_{SSP}	V_{SS} Supply Current, ML2008 Powerdown Mode Only	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}			–0.1	mA
AC Characteristics							
t_{SET}	V_{OUT} Settling Time	4	V_{IN} = 0.185V. Change gain from –24 to +24dB. Measure from $\overline{WR}$ rising edge to when V_{OUT} settles to within 0.05dB of final value.			20	µs
t_{STEP}	V_{OUT} Step Response	4	Gain = +24dB. V_{IN} = –3V to +3V step. Measure from V_{IN} = –3V to when V_{OUT} settles to within 0.05dB of final value.			20	µs
t_{DS}	Data Setup Time	4		50			ns
t_{DH}	Data Hold Time	4		50			ns
t_{AS}	A0 Setup Time	4		0			ns
t_{AH}	A0 Hold Time	4		0			ns
t_{CSS}	$\overline{CS}$* Setup Time	4		0			ns
t_{CSH}	$\overline{CS}$* Hold Time	4		0			ns
t_{PW}	$\overline{WR}$* Pulse Width	4		50			ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground

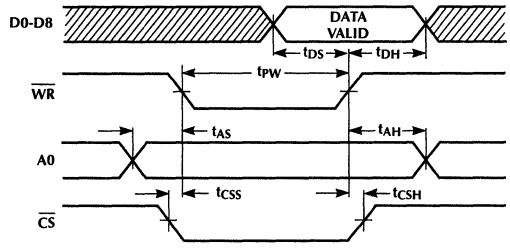
Note 2: 0°C to +70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed Parameters not 100% tested are not in outgoing quality level calculation.

TIMING DIAGRAM



TYPICAL PERFORMANCE CURVES

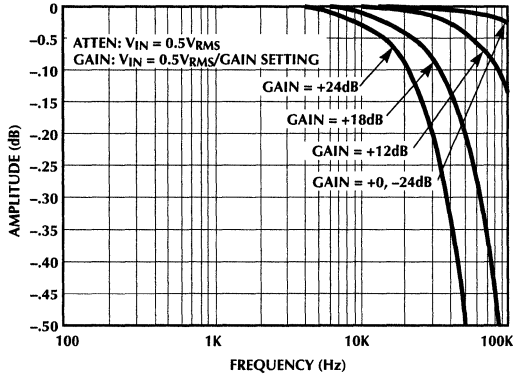


Figure 2. Amplitude vs Frequency (V_{IN}/V_{OUT} = 0.5V_{RMS})

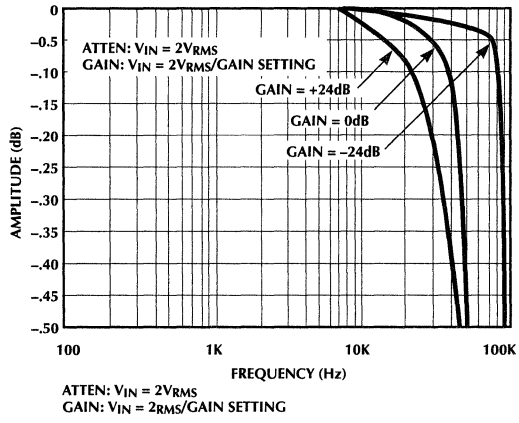


Figure 3. Amplitude vs Frequency (V_{IN}/V_{OUT} = 2V_{RMS})

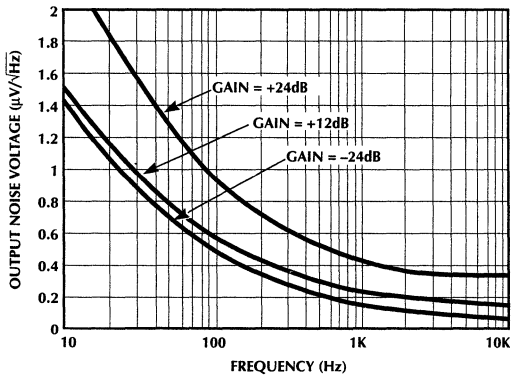


Figure 4. Output Noise Voltage vs Frequency

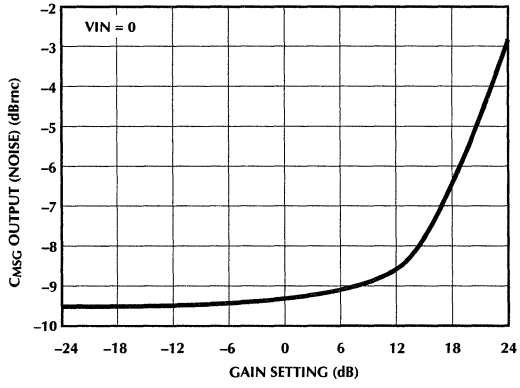


Figure 5. C_{MSG} Output Noise vs Gain Setting

TYPICAL PERFORMANCE CURVES (Continued)

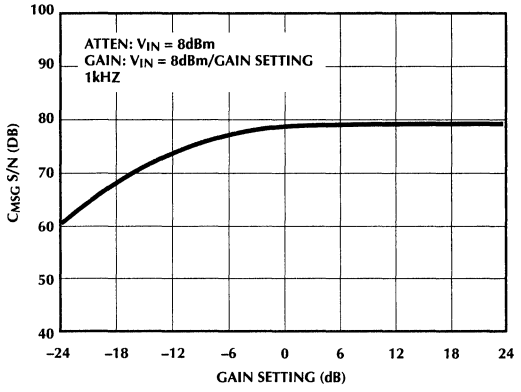


Figure 6. C_{MSG} S/N vs Gain Setting

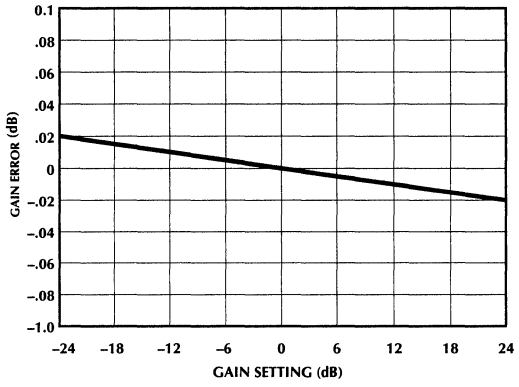


Figure 7. Gain Error vs Gain Setting

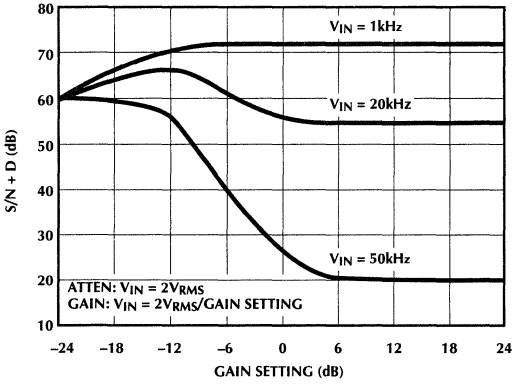


Figure 8. S/N +D vs Gain Setting (V_{IN}/V_{OUT} = $2V_{RMS}$)

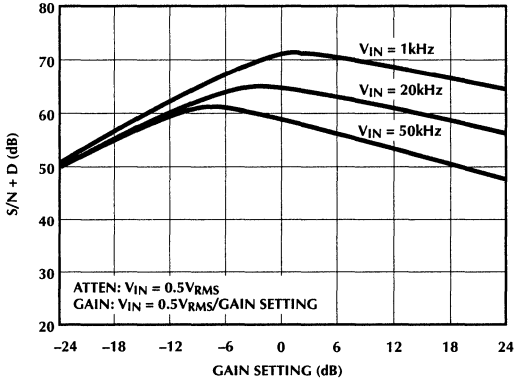


Figure 9. S/N +D vs Gain Setting (V_{IN}/V_{OUT} = $0.5V_{RMS}$)

3

1.0 FUNCTIONAL DESCRIPTION

The ML2008, ML2009 consists of a coarse gain stage, a fine gain stage, an output buffer, and a µP compatible parallel digital interface.

1.1 Gain Stages

The analog input, V_{IN}, goes directly into the op amp input in the coarse gain stage. The coarse gain stage has a gain range of 0 to 22.5dB in 1.5dB steps.

The fine gain stage is cascaded onto the coarse section. The fine gain stage has a gain range of 0 to 1.5dB in 0.1dB steps.

Both stages can be programmed for either gain or attenuation, thus doubling the effective gain range.

The logarithmic steps in each gains stage are generated by placing the input signal across a resistor string of 16 series resistors. Analog switches allow the voltage to be tapped from the resistor string at 16 points. The resistors are sized such that each output voltage is at the proper logarithmic ratio relative to the input signal at the top of the string. Attenuation is implemented by using the resistor string as a simple voltage divider, and gain is implemented by using the resistor string as a feedback resistor around an internal op amp.

1.2 Gain Settings

Since the coarse and fine gain stages are cascaded, their gains can be summed logarithmically. Thus, any gain from –24dB to +24dB in 0.1dB steps can be obtained by combining the coarse and fine gain setting to yield the

desired gain setting. The relationship between the register 0 and 1 bits and the corresponding analog gain values is shown in Tables 1 and 2. Note that C3-C0 select the coarse gain, F3-F0 select the fine gain, and ATTEN/$\overline{\text{GAIN}}$ selects either gain or attenuation.

1.3 Output Buffer

The final analog stage is the output buffer. This amplifier has internal gain of 1 and is designed to drive 600Ω, 100pF loads. Thus, it is suitable for driving a telephone hybrid circuit directly without any external amplifier.

1.4 Power Supplies

The digital section is powered between V_{CC} and GND, or 5V. The analog section is powered between V_{CC} and V_{SS} and uses AGND as the reference point, or ±5V.

GND and AGND are totally isolated inside the device to minimize coupling from the digital section into the analog section. Typically this is less than 100µV. However, AGND and GND should be tied together physically near the device and ideally close to the common power supply ground connection.

Typically, the power supply rejection of V_{CC} and V_{SS} to the analog output is greater than –60dB at 1KHz. If decoupling of the power supplies is still necessary in a system, V_{CC} and V_{SS} should be decoupled with respect to AGND.

Table 1. Fine Gain Settings (C3 – C0 = 0)

				Ideal Gain (dB)	
F3	F2	F1	F0	ATTEN/GAIN = 1	ATTEN/GAIN = 0
0	0	0	0	0.0	0.0
0	0	0	1	–0.1	0.1
0	0	1	0	–0.2	0.2
0	0	1	1	–0.3	0.3
0	1	0	0	–0.4	0.4
0	1	0	1	–0.5	0.5
0	1	1	0	–0.6	0.6
0	1	1	1	–0.7	0.7
1	0	0	0	–0.8	0.8
1	0	0	1	–0.9	0.9
1	0	1	0	–1.0	1.0
1	0	1	1	–1.1	1.1
1	1	0	0	–1.2	1.2
1	1	0	1	–1.3	1.3
1	1	1	0	–1.4	1.4
1	1	1	1	–1.5	1.5

Table 2. Coarse Gain Settings (F3 – F0 = 0)

				Ideal Gain (dB)	
C3	C2	C1	C0	ATTEN/GAIN = 1	ATTEN/GAIN = 0
0	0	0	0	0.0	0.0
0	0	0	1	–1.5	1.5
0	0	1	0	–3.0	3.0
0	0	1	1	–4.5	4.5
0	1	0	0	–6.0	6.0
0	1	0	1	–7.5	7.5
0	1	1	0	–9.0	9.0
0	1	1	1	–10.5	10.5
1	0	0	0	–12.0	12.0
1	0	0	1	–13.5	13.5
1	0	1	0	–15.0	15.0
1	0	1	1	–16.5	16.5
1	1	0	0	–18.0	18.0
1	1	0	1	–19.5	19.5
1	1	1	0	–21.0	21.0
1	1	1	1	–22.5	22.5

2.0 DIGITAL INTERFACE

The architecture of the digital section is shown in the preceding black diagram.

The structure of the data registers or latches is shown in Figures 10 and 11 for the ML2008 and ML2009, respectively. The registers control the attenuation/gain setting bits and with the ML2008 the power down bit.

Tables 1 and 2 describe how the data word programs the gain.

The difference between the ML2008 and ML2009 is in the register structure. The ML2008 is an 8-bit data bus version. This device has one 8-bit register and one 2-bit register to store the 9 gain setting bits and 1 powerdown bit. Two write operations are necessary to program the full 10 data bits from eight external data pins. The address pin A0 controls which register is being written into. The powerdown bit, PDN, causes the device to be placed in powerdown. When PDN = 1, the device is powered down. In this state, the power consumption is reduced by removing power from the analog section and forcing the analog output, V_{OUT}, to a high impedance state. While the device is in powerdown, the digital section is still functional and the current data word remains stored in the registers. When PDN = 0, device is in normal operation.

The ML2009 is a 9-bit data bus version. This device has one 9-bit register to store the 9 gain setting bits. The full 9 data bits can be programmed with one write operation from nine external data pins.

The internal registers or latches are edge triggered. The data is transferred from the external pins to the register output on the rising edge of $\overline{\text{WR}}$. The address pin, A0, controls which register the data will be written into as shown in Figures 1 and 2. The $\overline{\text{CS}}$ control signal selects the device by allowing the $\overline{\text{WR}}$ signal to latch in the data only when $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is high, $\overline{\text{WR}}$ is inhibited from latching in new data into the registers.

	D8	D7	D6	D5	D4	D3	D2	D1	BIT
A0 = 0	ATTEN/$\overline{\text{GAIN}}$	C3	C2	C1	C0	F3	F2	F1	REG 0
A0 = 1							P_{DN}	F0	REG 1

Figure 10. ML2008 Register Structure

D8	D7	D6	D5	D4	D3	D2	D1	D0	BIT
ATTEN/$\overline{\text{GAIN}}$	C3	C2	C1	C0	F3	F2	F1	F0	REG 0

Figure 11. ML2009 Register Structure

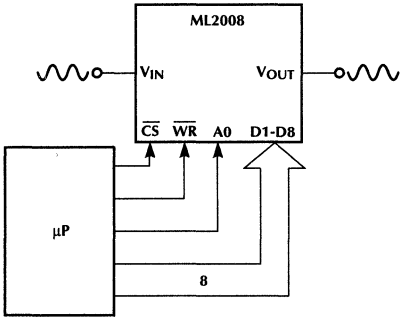


Figure 12. Typical 8-Bit µP Interface, Double Write

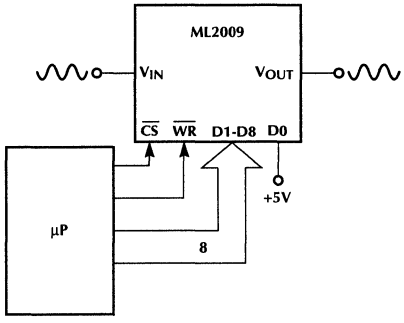


Figure 13. Typical 8-Bit µP Interface, Single Write

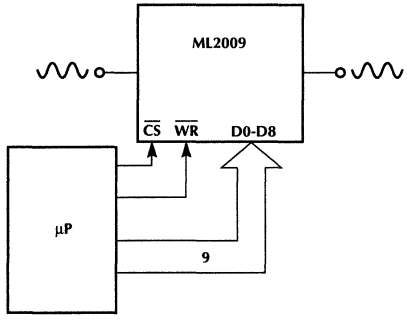


Figure 14. Typical 16-Bit µP Interface

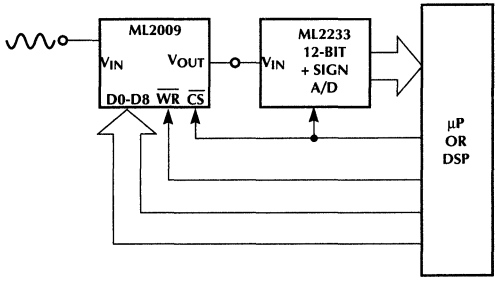


Figure 15. AGC for DSP or Modem Front End

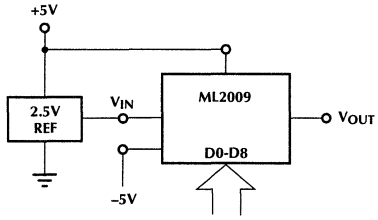


Figure 16. Operation as Logarithmic D/A Converter

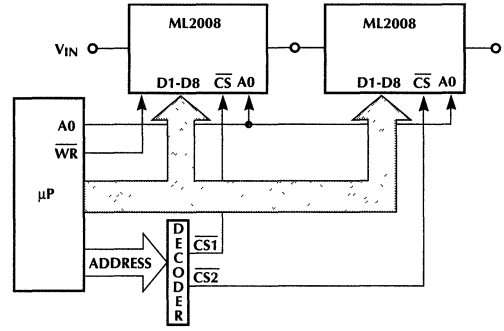


Figure 17. Controlling Multiple Gain/Attenuators

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2008IJ	–40°C to 85°C	Hermetic Dip (J18)
ML2008IP	–40°C to 85°C	Molded Dip (P18)
ML2008IQ	–40°C to 85°C	Molded PCC (Q20)
ML2008CP	0°C to +70°C	Molded Dip (P18)
ML2008CQ	0°C to +70°C	Molded PCC (Q20)
ML2009IJ	–40°C to 85°C	Hermetic Dip (J18)
ML2009IP	–40°C to 85°C	Molded Dip (P18)
ML2009IQ	–40°C to 85°C	Molded PCC (Q20)
ML2009CP	0°C to +70°C	Molded Dip (P18)
ML2009CQ	0°C to +70°C	Molded PCC (Q20)

Telephone Line Equalizer

GENERAL DESCRIPTION

The ML2020 is a monolithic analog line equalizer for telephone applications. The ML2020 consists of a switched capacitor filter that realizes a family of frequency response curves optimized for telephone line equalization.

The ML2020 consists of a continuous anti-aliasing filter, a 60Hz rejection highpass filter section, three programmable switched capacitor equalization filters, an output smoothing filter, a 600Ω driver, and a digital section for the serial interface.

The equalization filters adjust the slope, height, and bandwidth of the frequency response. The desired frequency response is programmed by a digital 14-bit serial input data stream.

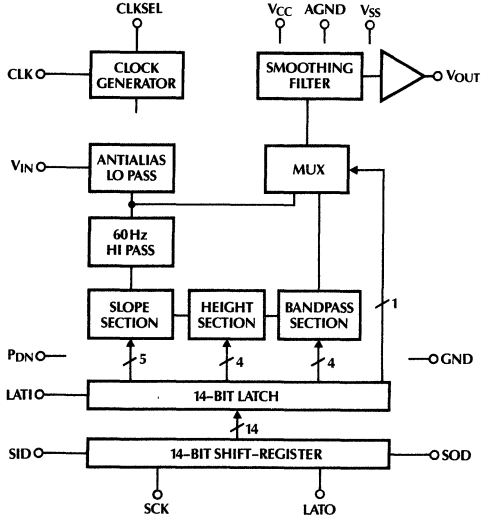
The ML2020 is implemented in a double polysilicon CMOS technology.

FEATURES

- Slope, height, and bandwidth adjustable
- 60Hz rejection filter
- On chip anti-alias filter
- Bypass mode
- Low supply current 6mA typical from ±5V supplies
- TTL/CMOS compatible interface
- Double buffered data latch
- Selectable master clock 1.544 or 1.536MHz
- Synchronous or asynchronous data loading capability
- Compatible with ML2003 and ML2004 logarithmic gain/attenuator
- Standard 16-pin 0.3" center molded or hermetic dip and 18-pin SOIC
- 0°C to +70°C and -40°C to +85°C operating temperature range

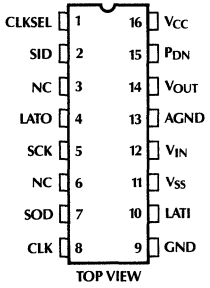
3

BLOCK DIAGRAM



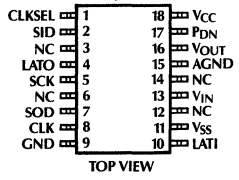
PIN CONNECTIONS

ML2020
16-PIN DIP



TOP VIEW

ML2020
18-PIN SOIC



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
CLKSEL	Clock select input. This pin selects the frequency of the CLK input. If CLK is 1.536MHz, set CLKSEL=1. If CLK is 1.544MHz, set CLKSEL=0. Pin has an internal pullup resistor to V_{CC}.
SID	Serial input data. Digital input that contains serial data word which controls the filter frequency response setting.
LATO	Output latch clock. Digital input which loads the data word back into the shift register from the latch.
SCK	Shift clock. Digital input which shifts the serial data on SID into the shift register on rising edges and out onto SOD on falling edges.
SOD	Serial output data. Digital output of the shift register.
CLK	Master clock input. Digital input which generates clocks for the switched capacitor filters. Frequency can be either 1.544MHz or 1.536MHz.
GND	Digital ground. 0volts. All digital inputs and output are referenced to this ground.
LATI	Input latch clock. Digital input which loads data from the shift register into the latch.
V_{SS}	Negative supply. −5volts ±10%.
V_{IN}	Analog input.
AGND	Analog ground. 0volts. Analog input and output are referenced to this ground.
V_{OUT}	Analog output.
P_{DN}	Powerdown input. When $P_{DN}=1$, device is in powerdown mode. When $P_{DN}=0$, device is in normal operation. This pin has an internal pulldown resistor to GND.
V_{CC}	Positive supply. 5volts ±10%

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} ..... +6.5V
- V_{SS} ..... −6.5V
- AGND with Respect to GND ..... ±0.5V
- Analog Input and Output ..... V_{SS} −0.3V to V_{CC} +0.3V
- Digital Input and Outputs ..... GND −0.3V to V_{CC} +0.3V
- Input Current Per Pin ..... ±25mA
- Power Dissipation 750mW
- Storage Temperature Range ..... −65°C to +150°C
- Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2020CP, ML2020CS ..... 0°C to +70°C
- ML2020IJ ..... −40°C to +85°C

Supply Voltage
- V_{CC} ..... 4V to 6V
- V_{SS} ..... −4V to −6V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, Data Word: $\overline{BP} = 1$, Other Bits = 0, $C_L = 100pF$, $R_L = 600\Omega$, dBm measurements use 600Ω as reference load, $V_{IN} = -7$ dBm, 1kHz sinusoid CLK = 1.544MHz ±300Hz and digital time measured at 1.4V

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
ANALOG							
SR	Response, Slope Section	4	1kHz response				
			NL/L S3 S2 S1 S0				
			0 0 0 0 1			1.4±0.1	dB
			0 0 0 1 0			2.6±0.2	dB
			0 0 1 0 0			4.7±0.2	dB
			0 1 0 0 0			7.8±0.2	dB
			0 1 1 1 1			11.4±0.25	dB
			1 0 0 0 0			0±0.1	dB
			1 0 0 0 1			0.4±0.1	dB
			1 0 0 1 0			0.9±0.2	dB
			1 0 1 0 0			1.8±0.2	dB
			1 1 0 0 0			3.7±0.2	dB
			1 1 1 1 1			6.6±0.25	dB
			Referenced to				
			0 0 0 0 0				
HR	Response, Height Section	4	3250Hz response referenced to 1kHz response with $\overline{BP} = 1$, other bits = 0				
			NL/L H3 H2 H1 H0				
			0 0 0 0 0			0±0.1	dB
			0 0 0 0 1			0.6±0.2	dB
			0 0 0 1 0			1.2±0.2	dB
			0 0 1 0 0			2.4±0.2	dB
			0 1 0 0 0			5.8±0.3	dB
			0 1 1 1 1			11.2±0.3	dB
BR	Response, Bandwidth Section (Q)	4	NL/L B3 B2 B1 B0 H3 H2 H1 H0				
			0 0 0 0 0 1 1 1 1			16.1±2.0	
			0 0 0 0 1 1 1 1 1			14.2±1.5	
			0 0 0 1 0 1 1 1 1			12.6±1.5	
			0 0 1 0 0 1 1 1 1			9.1±1.0	
			0 1 0 0 0 1 1 1 1			3.6±0.5	
			0 1 1 1 1 1 1 1 1			1.2±0.35	
PK	BW Peak Frequency	4	H3 thru H0 = 1	3230	3250	3270	Hz
AG	Absolute Gain, Flat Response	4	1 to 4kHz	−0.1	+0.1	+0.3	dB
AGB	Absolute Gain, Bypass Mode	4	0.3 to 4kHz, $\overline{BP} = 0$	−0.1	+0.1	+0.3	dB
ICN	Idle Channel Noise	4	$V_{IN} = 0$		3	8	dBrnc
			V_{IN} = 0, All Data Bits = 1		9		dBrnc

3

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, Data Word: $\overline{BP} = 1$, Other Bits = 0, $C_L = 100pF$, $R_L = 600\Omega$, dBm measurements use 600Ω as reference load, $V_{IN} = -7dBm$, 1kHz sinusoid CLK = 1.544MHz ±300Hz and digital time measured at 1.4V

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 4	MAX	LIMIT UNITS
ANALOG							
HD	Harmonic Distortion	4	$V_{IN} = 5dBm$, 1kHz Measure 2nd, 3rd, harmonic relative to fundamental			−48	dB
SD	Signal to Distortion	4	$V_{IN} = -12dBm$, 1kHz C msg weighted	+48			dB
SFN	Single Frequency Noise	5	$V_{IN} = 0$, 4kHz ≤ frequency ≤ 150kHz			−50	dBm
PSRR	Power Supply Rejection	4	$200mV_{p-p}$, 1kHz sine, $V_{IN} = 0$ on V_{CC} on V_{SS}			−40 −40	dB dB
Z_{IN}	Input Impedance, V_{IN}	4		100			kΩ
V_{OS}	Output Offset Voltage	4	$V_{IN} = 0$			±50	mV
V_{INR}	Input Voltage Range	4		±2.0			V
V_{OSW}	Output Voltage Swing	4	$R_L = 600\Omega$	±2.0			V
DIGITAL AND DC							
V_{IL}	Digital Input Low Voltage	4				0.8	V
V_{IH}	Digital Input High Voltage	4		2.0			V
V_{OL}	Digital Output Low Voltage	4	$I_{OL} = 2mA$			0.4	V
V_{OH}	Digital Output High Voltage	4	$I_{OH} = -1mA$	4.0			V
I_{LCLK}	Input Current, CLK SEL	4	$V_{IN} = 0$	5		100	μA
I_{LPDN}	Input Current, PDN	4	$V_{IN} = V_{CC}$	−5		−100	μA
I_L	Input Current, All Other Inputs	4	$V_{IN} = 0 - V_{CC}$			±10	μA
I_{CC}	V_{CC} Supply Current	4	No output load, $V_{IL} = GND$, $V_{IH} = V_{CC}$, $V_{IN} = 0$			10	mA
I_{SS}	V_{SS} Supply Current	4	No output load, $V_{IL} = GND$, $V_{IH} = V_{CC}$, $V_{IN} = 0$			−10	mA
I_{CCP}	V_{CC} Supply Current, Powerdown Mode	4	No output load, $V_{IL} = GND$, $V_{IH} = V_{CC}$			1.2	mA
I_{SSP}	V_{SS} Supply Current, Powerdown Mode	4	No output load, $V_{IL} = GND$, $V_{IH} = V_{CC}$			−1.2	mA
AC CHARACTERISTICS							
t_{DC}	Clock Duty Cycle	5		40		60	%
t_{SCK}	SCK On/Off Period	4		250			ns
t_S	SID Data Setup Time	4		50			ns
t_H	SID Data Hold Time	4		50			ns
t_D	SOD Data Delay	4		0		125	ns
t_{IPW}	LATI Pulse Width	4		50			ns
t_{OPW}	LATO Pulse Width	4		50			ns
t_{IS}, t_{OS}	LATI, LATO Setup Time	4		50			ns
t_{IH}, t_{OH}	LATI, LATO Hold Time	5		50			ns
t_{PLD}	SOD Parallel Load Delay	4		0		125	ns

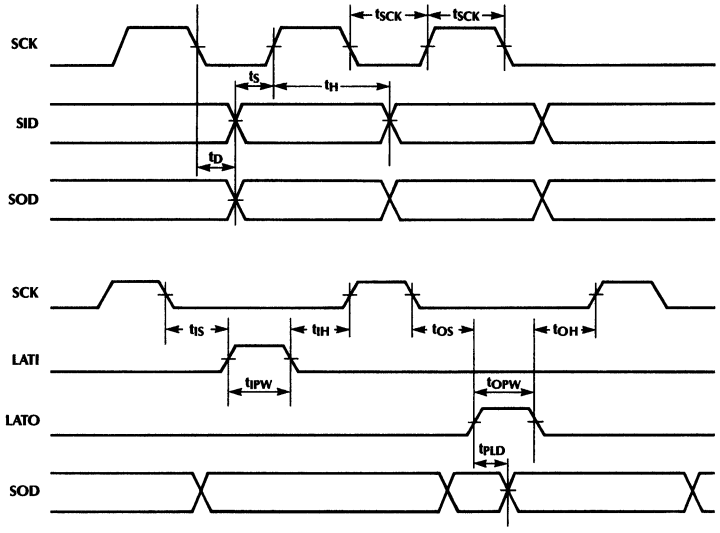
Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: 0°C to +70°C and −40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.



TIMING PARAMETERS ARE REFERENCED TO THE 1.4 VOLT MIDPOINT.

Figure 1. Serial Timing Diagram

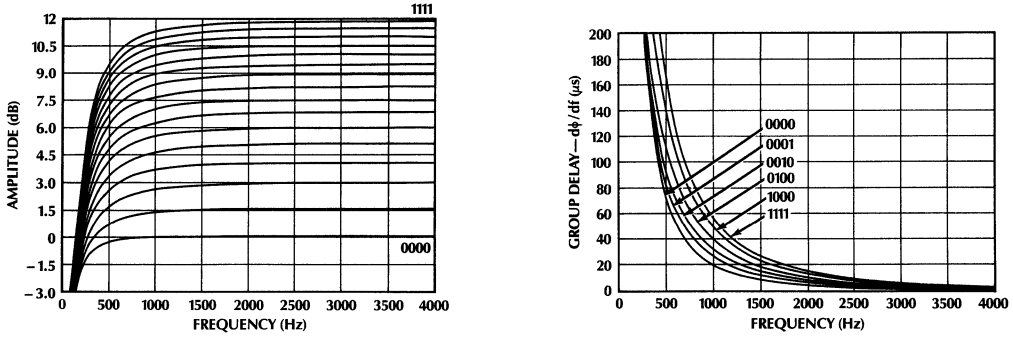


Figure 2. Typical Slope Filter Response — NL/L = 0

B3–B0, H3–H0 = 0000, S3–S0 = 0000 to 1111.

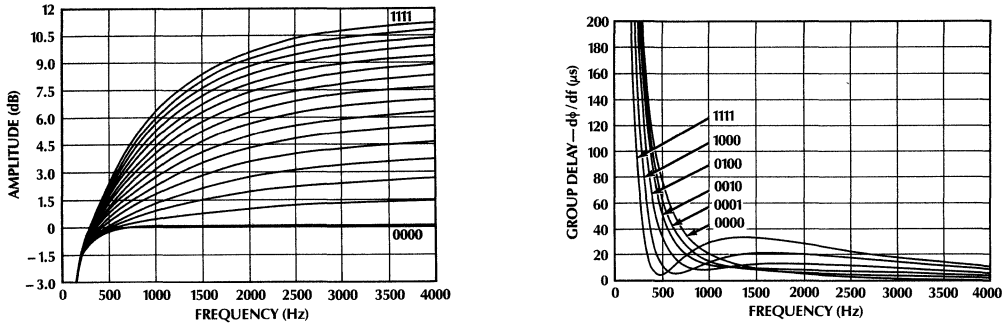


Figure 3. Typical Slope Filter Response — NL/L = 1
B3–B0, H3–H0 = 0000, S3–S0 = 0000 to 1111.

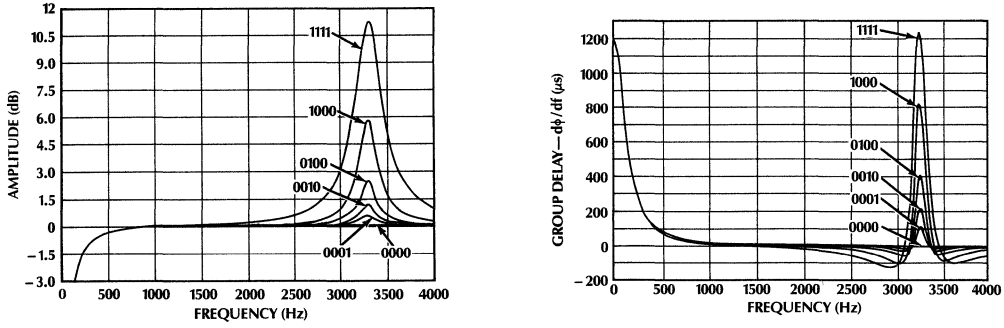


Figure 4. Typical Height Filter Response — NL/L = 0
B3–B0, S3–S0 = 0000; H3–H0 = 0000 to 1111.

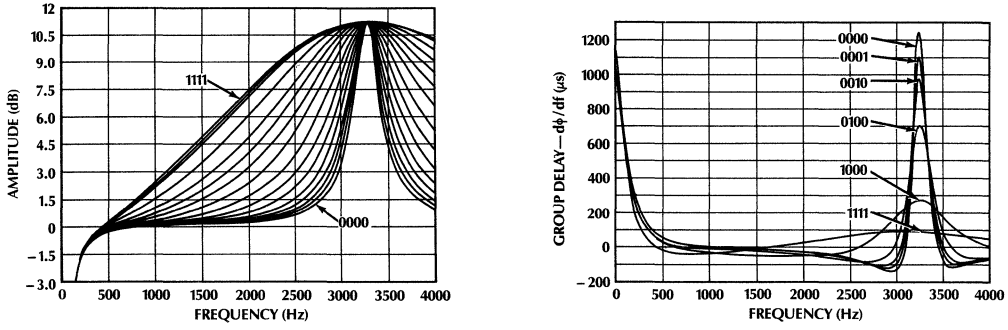


Figure 5. Typical Bandwidth Filter Response — NL/L = 0
H3–H0 = 1111; S3–S0 = 0000; B3–B0 = 0000 to 1111.

1.0 FUNCTIONAL DESCRIPTION

The ML2020 consists of a continuous anti-alias filter, a 60Hz reject highpass filter section, three programmable switched capacitor equalization filters, an output smoothing filter, an output driver, and a digital section for the serial interface.

1.1 Anti-Alias Filter

The first section is a continuous anti-alias filter. This filter is needed to prevent aliasing of high frequency signals present on the input into the passband by the sampling action of the switched capacitor filters. This section is a continuous second order lowpass filter with a typical 3dB frequency at 20kHz and 30dB of rejection at 124kHz.

1.2 60Hz Rejection Filter

The 60Hz section is a highpass switched capacitor filter designed to reject DC offsets and low frequency signals present on the input. This filter is a first order section with a typical 3dB frequency at 135Hz.

1.3 Equalization Filters

The equalizer filters follow the 60Hz highpass section. These programmable filters implement a family of frequency response curves intended to compensate for the response of telephone lines.

This filter is composed of three distinct sections: slope, height, and bandwidth.

1.3.1 Response of Slope, Height, and Bandwidth

The family of response curves generated by the slope section are shown in Figures 2 and 3. There are 4 slope select bits, S3-S0. These bits alter the slope of the highpass response under 1000Hz, and as a result, the absolute gain above 1000Hz will be unique for each setting. Table 1 gives typical 1kHz gain values for all slope settings.

Table 1. Typ. 1kHz Gain for Slope Settings

Slope Setting	Rel 1kHz Gain (dB)	
	NL/L=1	NL/L=0
0	0.0	Rel
1	0.4	1.4
2	0.9	2.6
3	1.4	3.7
4	1.8	4.7
5	2.3	5.5
6	2.8	6.3
7	3.4	7.2
8	3.7	7.8
9	4.2	8.4
10	4.6	9.0
11	5.0	9.5
12	5.4	10.0
13	5.8	10.5
14	6.2	11.0
15	6.6	11.4

HT, BW Bits=0

There is an additional bit, NL/L, that also affects the highpass response of the slope filter. The slope response curves in Figure 2 are with NL/L=0. These same response curves are shown in Figure 3 with NL/L=1. Notice that the NL/L bit adds more droop in the highpass response below 2500Hz.

The family of response curves generated by the height section are shown in Figure 4. There are 4 height select bits, H3-H0. This section creates a peak in the response at 3250Hz and this filter controls the amount of peaking. Table 2 gives typical 1kHz gain values for all height and bandwidth settings.

Table 2. Typ. 1kHz Gain for HT and BW Settings

	Relative 1kHz Gain (dB)															
	HT Setting															
BW Setting	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Rel	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0.1
5	0	0	0	0	0	0	0	0	0	0	0	0	0.1	0.1	0.1	0.1
6	0	0	0	0	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.1
7	0	0	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.2	0.2	0.2
8	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.2	0.2	0.3	0.3	0.4
9	0	0	0	0	0	0.1	0.1	0.1	0.1	0.2	0.2	0.3	0.3	0.4	0.5	0.6
10	0	0	0	0	0.1	0.1	0.1	0.1	0.2	0.3	0.3	0.4	0.5	0.6	0.7	0.8
11	0	0	0	0.1	0.1	0.1	0.2	0.2	0.3	0.4	0.4	0.5	0.7	0.8	0.9	1.1
12	0	0	0.1	0.1	0.1	0.2	0.2	0.3	0.4	0.5	0.7	0.8	1.0	1.1	1.4	1.6
13	0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.6	0.8	0.9	1.1	1.4	1.6	1.9	2.3
14	0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.7	0.8	1.0	1.2	1.5	1.7	2.0	2.4
15	0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.7	0.9	1.1	1.3	1.6	1.8	2.1	2.5

Slope Bits=0

The family of response curves generated by the bandwidth section is shown in Figure 5 There are 4 bandwidth select bits, B3-B0. This section causes the response of the 3250Hz peak to be widened, and as a result, this filter controls the bandwidth of the 3250Hz peaked region.

1.3.2 Transfer Function

The transfer function for the ML2020 is shown below. This transfer function is valid for magnitude response only. The actual magnitude response from an individual device may deviate from the computed response from the transfer function by typically 0–0.2dB.

$$H(s) = \frac{-s}{s+a} \times \frac{c(s+b)}{b(s+c)} \times \frac{\left[s^2 + h(\omega_o/Q)s + \omega_o^2\right]}{\left[s^2 + (\omega_o/Q)s + \omega_o^2\right]} \times \frac{\left[\sin(\pi f/fc)\right]}{(\pi f/fc)}$$

$s = j \times 256000 \times \tan(\pi f/128000)$
$a = 848.230$
$\omega_o = 20463.77$
$fc = 128000$
b,c : See Table 3. (slope)
Q : See Table 4. (bandwidth)
h : See Table 5. (height)

Table 3. Slope Response Factors (b, c)

S3–0	b NL/L = 0	b NL/L = 1
0000	2.371759E+03	1.116280E+04
0001	1.985920E+03	9.345141E+03
0010	1.701779E+03	8.007156E+03
0011	1.493571E+03	7.026999E+03
0100	1.326721E+03	6.241681E+03
0101	1.196668E+03	5.629636E+03
0110	1.087277E+03	5.114881E+03
0111	9.983588E+02	4.696487E+03
1000	9.179889E+02	4.318339E+03
1001	8.537864E+02	4.016273E+03
1010	7.966049E+02	3.747249E+03
1011	7.478074E+02	3.517676E+03
1100	7.035099E+02	3.309279E+03
1101	6.651771E+02	3.128945E+03
1110	6.299477E+02	2.963214E+03
1111	5.990361E+02	2.817797E+03

S3–0	c NL/L = 0	c NL/L = 1
XXXX	2.371759E+03	1.116280E+04

Table 4. Slope Response Factors (b, c)

B3–0	Q
0000	17.444906
0001	15.386148
0010	13.652451
0011	11.593677
0100	9.859960
0101	8.017864
0110	6.392453
0111	5.092080
1000	3.900003
1001	3.141338
1010	2.599369
1011	2.165724
1100	1.731965
1101	1.406509
1110	1.352248
1111	1.297981

Table 5. Height Response Factors (h)

Code	h
0000	1.000000
0001	1.071519
0010	1.148154
0011	1.230269
0100	1.318257
0101	1.445438
0110	1.603245
0111	1.757924
1000	1.949845
1001	2.137962
1010	2.317395
1011	2.540973
1100	2.786121
1101	3.019951
1110	3.311311
1111	3.672823

1.4 Smoothing Filter

The equalizer filters are followed by a continuous second order smoothing filter that removes the high frequency sample information generated by the action of the switched capacitor filters. This filter provides a continuous analog signal at the output, V_{OUT} .

1.5 Output Buffer

The final stage in the ML2020 is the output buffer. This amplifier has internal gain of 1 and is capable of driving 600Ω, 100pF loads. Thus, it is suitable for driving telephone hybrids directly without any external amplifier.

1.6 Bypass Mode

The filter sections can be bypassed by setting the bypass data bit, $\overline{BP}$, to 0. Since the switched capacitor filters are bypassed in this mode, frequency response effects of the switched capacitor filters are eliminated. Thus, this mode offers very flat response and low noise over the 300–4000Hz frequency range.

1.7 Filter Clock

The master clock, CLK, is used to generate the internal clocks for the switched capacitor filters. The frequency of CLK can be either 1.544MHz or 1.536MHz. However, the internal clock frequency must be kept at 1.536MHz to guarantee accurate frequency response. The CLKSEL pin enables a bit swallower circuit to keep the internal clock frequency set to 1.536MHz. When 1.544MHz clock is used, CLKSEL should be set to logic level 0, and one bit out of every 193 bits is removed (swallowed) to reduce the internal frequency to 1.536MHz. When 1.536MHz clock is used, CLKSEL should be set to logic level 1, and the internal clock rate is the same as the external clock rate.

1.8 Serial Interface

The architecture of the digital section is shown in the preceding block diagram.

A timing diagram for the serial interface is shown in Figure 6. The serial input data, SID, is loaded into a shift register on rising edges of the shift clock, SCK. The data word is parallel loaded into a latch when the input latch signal, LATI, is high. The LATI pulse must occur when SCK is low. A new data word can be loaded into the shift register without disturbing the existing data word in the latch.

The parallel outputs of the latch control the filter response curves. The order of the data word bits in the latch is shown in Figure 7.

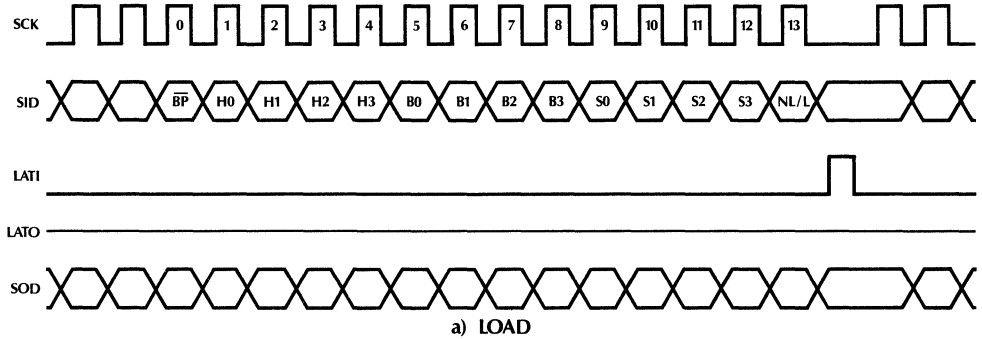
Note that bit 0 is the first bit of the data word clocked into the shift register.

The device has the capability to read out the data word stored in the latch. This is done by parallel loading the data from the latch back into the shift register when the latch signal, LATO, is high. The LATO pulse must occur when SCK is low. Then, the data word can be shifted out of the register serially to the output, SOD, on falling edges of the shift clock, SCK.

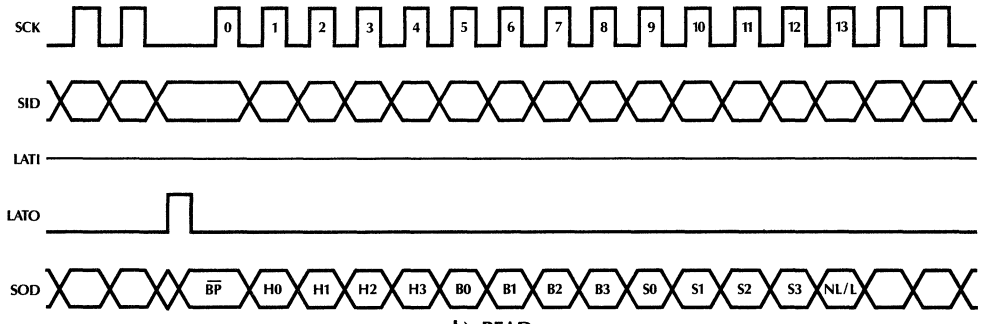
The loading and reading of the data word can be done continuously or in bursts. Since the shift register and latch

circuitry inside the device is static, there are no minimum frequency requirements on the clocks or data pulses. However, there is some coupling of the digital signals into the analog section. If this coupling is undesirable, the data can be clocked in bursts during non critical intervals, or the data rate can be done at a frequency outside the analog frequency range.

The clocks used to shift and latch data (SCK, LATI, LATO) are not related internally to the master clock and can occur asynchronous to CLK.



a) LOAD



b) READ

Figure 6. Serial Timing

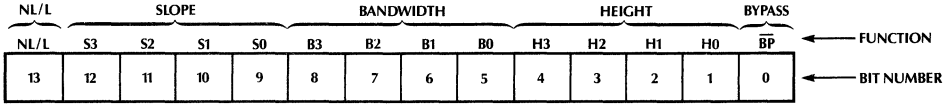


Figure 7. 14-Bit Latch

POWERDOWN MODE

A powerdown mode can be selected with pin P_{DN}. When $P_{DN}=1$, the device is powered down. In this state, the power consumption is reduced by removing power from the analog section and forcing the analog output, V_{OUT}, to a high impedance state. While the device is in power down mode, the digital section is still functional and the current data word remains stored in the latch. The master clock, CLK, can be left active or removed during powerdown mode. When $P_{DN}=0$, the device is in normal operation.

POWER SUPPLIES

The digital section inside the device is powered between V_{CC} and GND, or 5 volts. The analog section is powered between V_{CC} and V_{SS}, or ±5 volts. The analog section uses AGND as the reference point.

GND and AGND are totally isolated inside the device to minimize coupling from the digital section into the analog section. Typically this is less than 100μV. However, AGND and GND should be tied together physically near the device and close to the common power supply ground connection.

The power supply rejection of V_{CC} and V_{SS} to the analog output is greater than −60dB at 1kHz, typically. If decoupling of the power supplies is still necessary in a system, V_{CC} and V_{SS} should be decoupled with respect to AGND.

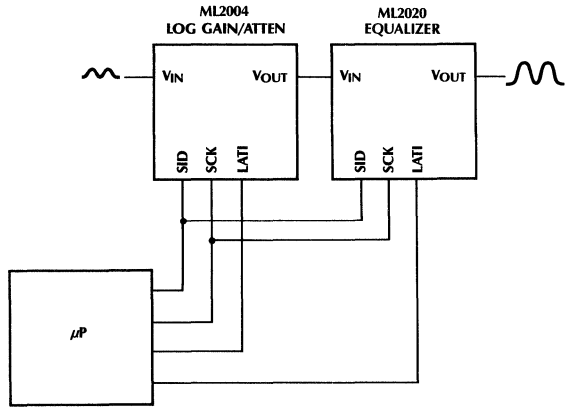


Figure 8. Typical Serial Interface

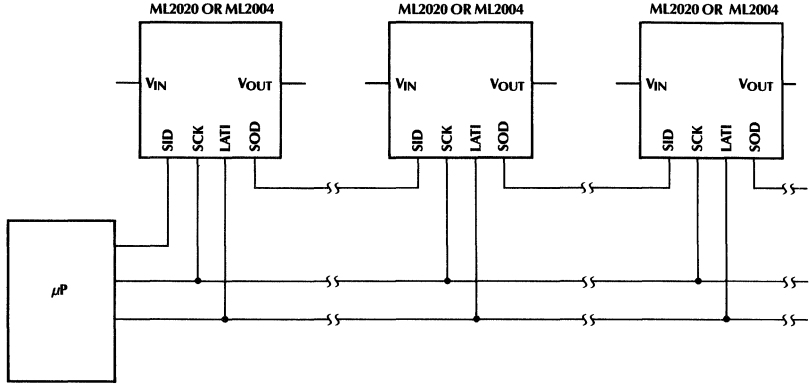


Figure 9. Controlling Multiple ML2020 and ML2004 With Only 3 Digital Lines Using One Long Data Word

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML2020CP	0°C to +70°C	MOLDED DIP (P16)
ML2020CS	0°C to +70°C	MOLDED SOIC (S18W)
ML2020IJ	–40°C to +85°C	HERMETIC DIP (J16)
ML2020IP	–40°C to +85°C	MOLDED DIP (P16)
ML2020IS	–40°C to +85°C	MOLDED SOIC (S18W)

Micro Linear

ML2021

Telephone Line Equalizer

GENERAL DESCRIPTION

The ML2021 is a monolithic analog line equalizer for telephone applications. The ML2021 consists of a switched capacitor filter that realizes a family of frequency response curves optimized for telephone line amplitude equalization while minimizing group delay. This ML2021 is the same function as the ML2020 telephone equalizer without the 60Hz rejection filter.

The ML2021 consists of a continuous anti-aliasing filter, three programmable switched capacitor equalization filters, an output smoothing filter, a 600Ω driver, and a digital section for the serial interface.

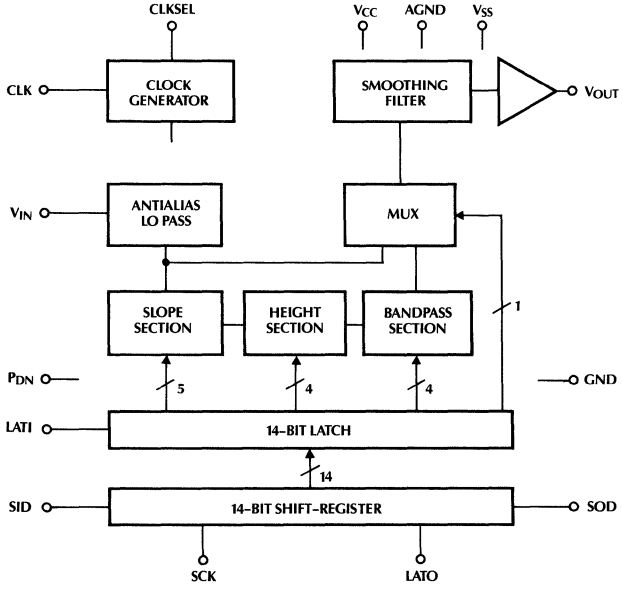
The equalization filters adjust the slope, height, and band-width of the frequency response. The desired frequency response is programmed by a digital 14-bit serial input data stream.

The ML2021 is implemented in a double polysilicon CMOS technology.

FEATURES

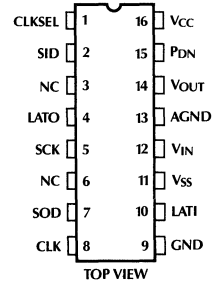
- Slope, height, and bandwidth adjustable
- Optimized group delays (500 Hz to 6.4 kHz)
- On chip anti-alias filter
- Bypass mode
- Low supply current 6mA typical from ±5V supplies
- TTL/CMOS compatible interface
- Double buffered data latch
- Selectable master clock 1.544 or 1.536 MHz
- Synchronous or asynchronous data loading capability
- Compatible with ML2003 and ML2004 logarithmic gain/attenuator
- Standard 16-pin 0.3" center molded or hermetic DIP and 18-pin SOIC
- 0°C to +70°C and -40°C to +85°C operating temperature range

BLOCK DIAGRAM



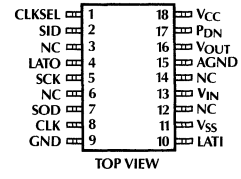
PIN CONNECTIONS

ML2021
16-pin DIP



TOP VIEW

ML2021
18-pin SOIC



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
CLKSEL	Clock select input. This pin selects the frequency of the CLK input. If CLK is 1.536MHz, set CLKSEL = 1. If CLK is 1.544MHz, set CLKSEL = 0. Pin has an internal pullup resistor to V_{CC}.
SID	Serial input data. Digital input that contains serial data word which controls the filter frequency response setting.
LATO	Output latch clock. Digital input which loads the data word back into the shift register from the latch.
SCK	Shift clock. Digital input which shifts the serial data on SID into the shift register on rising edges and out onto SOD on falling edges.
SOD	Serial output data. Digital output of the shift register.
CLK	Master clock input. Digital input which generates clocks for the switched capacitor filters. Frequency can be either 1.544MHz or 1.536MHz.
GND	Digital ground. 0 volts. All digital inputs and output are referenced to this ground.
LATI	Input latch clock. Digital input which loads data from the shift register into the latch.
V_{SS}	Negative supply. −5 volts ±10%.
V_{IN}	Analog input.
AGND	Analog ground. 0 volts. Analog input and output are referenced to this ground.
V_{OUT}	Analog output.
P_{DN}	Powerdown input. When P_{DN} = 1, device is in powerdown mode. When P_{DN} = 0, device is in normal operation. This pin has an internal pulldown resistor to GND.
V_{CC}	Positive supply. 5 volts ±10%

3

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} ..... +6.5V
- V_{SS} ..... −6.5V
- AGND with Respect to GND ..... ±0.5V
- Analog Input and Output ..... V_{SS} −0.3V to V_{CC} +0.3V
- Digital Input and Outputs ..... GND −0.3V to V_{CC} +0.3V
- Input Current Per Pin ..... ±25mA
- Power Dissipation 750mW
- Storage Temperature Range ..... −65°C to +150°C
- Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2021CP, ML2021CS ..... 0°C to +70°C
- ML2021IJ ..... −40°C to +85°C

Supply Voltage
- V_{CC} ..... 4V to 6V
- V_{SS} ..... −4V to −6V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, Data Word: $\overline{BP} = 1$, Other Bits = 0, $C_L = 100pF$, $R_L = 600\Omega$, dBm measurements use 600Ω as reference load, $V_{IN} = -7$dBm, 1kHz sinusoid CLK = 1.544MHz ±300Hz and digital time measured at 1.4V

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
ANALOG							
SR	Response, Slope Section	4	1kHz response NL/L S3 S2 S1 S0 0 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0 1 1 1 1 1 0 0 0 0 1 0 0 0 1 1 0 0 1 0 1 0 1 0 0 1 1 0 0 0 1 1 1 1 1 Referenced to 0 0 0 0 0			 1.4 ±0.1 2.6 ±0.2 4.7 ±0.2 7.8 ±0.2 11.4 ±0.25 0 ±0.1 0.4 ±0.1 0.9 ±0.2 1.8 ±0.2 3.7 ±0.2 6.6 ±0.25	 dB dB dB dB dB dB dB dB dB dB dB
HR	Response, Height Section	4	3250Hz response referenced to 1kHz response with $\overline{BP} = 1$, other bits = 0 NL/L H3 H2 H1 H0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0 1 1 1 1			 0 ± 0.15 0.5 ± 0.2 1.1 ± 0.2 2.3 ± 0.2 5.7 ± 0.3 11.1 ± 0.3	 dB dB dB dB dB dB
BR	Response, Bandwidth Section (Q)	4	NL/L B3 B2 B1 B0 H3 H2 H1 H0 0 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 1 0 0 0 1 0 1 1 1 1 0 0 1 0 0 1 1 1 1 0 1 0 0 0 1 1 1 1 0 1 1 1 1 1 1 1 1			 16.1 ±2.0 14.2 ±1.5 12.6 ±1.5 9.1 ±1.0 3.6 ±0.5 1.2 ±0.35	
PK	BW Peak Frequency	4	H3 thru H0 = 1	3230	3250	3270	Hz
AG	Absolute Gain, Flat Response	4	.5 to 4kHz	−0.1	+0.1	+0.3	dB
AGB	Absolute Gain, Bypass Mode	4	0.3 to 4kHz, $\overline{BP} = 0$	−0.1	+0.1	+0.3	dB
ICN	Idle Channel Noise	4	$V_{IN} = 0$		3	8	dBrnc
			$V_{IN} = 0$, all data bits = 1		9		dBrnc

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, Data Word: $\overline{BP} = 1$, Other Bits = 0, $C_L = 100pF$, $R_L = 600\Omega$, dBm measurements use 600Ω as reference load, $V_{IN} = -7$dBm, 1kHz sinusoid CLK = 1.544MHz ±300Hz and digital time measured at 1.4V

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	LIMIT UNITS
ANALOG							
HD	Harmonic Distortion	4	$V_{IN} = 5$dBm, 1kHz Measure 2nd, 3rd, harmonic relative to fundamental			−48	dB
SD	Signal to Distortion	4	$V_{IN} = -12$dBm, 1kHz C msg weighted	+48			dB
SFN	Single Frequency Noise	5	$V_{IN} = 0$, 4kHz ≤ frequency ≤ 150kHz			−50	dBm
PSRR	Power Supply Rejection	4	200mV$_{P-P}$, 1kHz sine, $V_{IN} = 0$ on V_{CC} on V_{SS}			−40 −40	dB dB
Z_{IN}	Input Impedance, V_{IN}	4		100			kΩ
V_{OS}	Output Offset Voltage	4	$V_{IN} = 0$			±50	mV
V_{INR}	Input Voltage Range	4		±2.0			V
V_{OSW}	Output Voltage Swing	4	$R_L = 600\Omega$	±2.0			V
DIGITAL AND DC							
V_{IL}	Digital Input Low Voltage	4				0.8	V
V_{IH}	Digital Input High Voltage	4		2.0			V
V_{OL}	Digital Output Low Voltage	4	$I_{OL} = 2$mA			0.4	V
V_{OH}	Digital Output High Voltage	4	$I_{OH} = -1$mA	4.0			V
I_{LCLK}	Input Current, CLK SEL	4	$V_{IN} = 0$	5		100	μA
I_{LPDN}	Input Current, PDN	4	$V_{IN} = V_{CC}$	−5		−100	μA
I_L	Input Current, All Other Inputs	4	V_{IN} = 0 to V_{CC}			±10	μA
I_{CC}	V_{CC} Supply Current	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$, $V_{IN} = 0$			10	mA
I_{SS}	V_{SS} Supply Current	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$, $V_{IN} = 0$			−10	mA
I_{CCP}	V_{CC} Supply Current, Powerdown Mode	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$			1.2	mA
I_{SSP}	V_{SS} Supply Current, Powerdown Mode	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$			−1.2	mA
AC CHARACTERISTICS							
t_{DC}	Clock Duty Cycle	5		40		60	%
t_{SCK}	SCK On/Off Period	4		250			ns
t_S	SID Data Setup Time	4		50			ns
t_H	SID Data Hold Time	4		50			ns
t_D	SOD Data Delay	4		0		125	ns
t_{IPW}	LATI Pulse Width	4		50			ns
t_{OPW}	LATO Pulse Width	4		50			ns
t_{IS},t_{OS}	LATI, LATO Setup Time	4		50			ns
t_{IH},t_{OH}	LATI, LATO Hold Time	5		50			ns
t_{PLD}	SOD Parallel Load Delay	4		0		125	ns

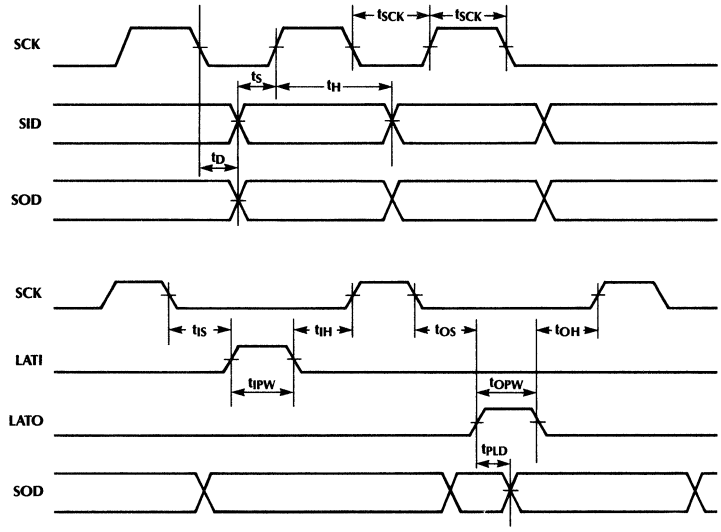
Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: 0°C to +70°C and −40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.



TIMING PARAMETERS ARE REFERENCED TO THE 1.4 VOLT MIDPOINT.

Figure 1. Serial Timing Diagram

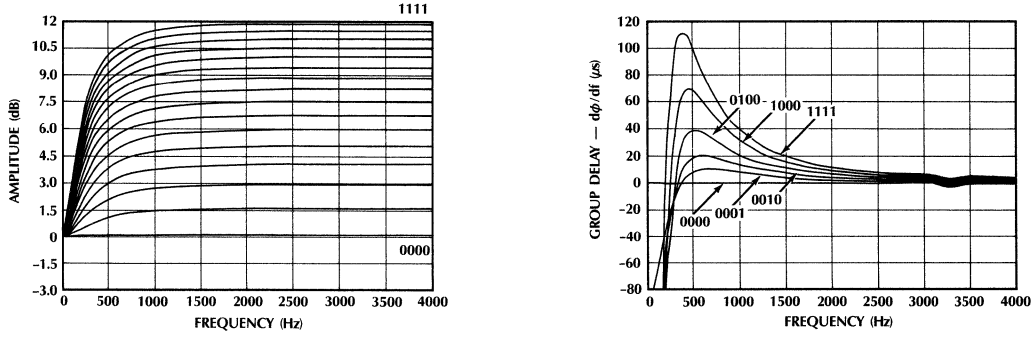


Figure 2. Typical Slope Filter Response — NL/L = 0

B3–B0, H3–H0 = 0000, S3–S0 = 0000 to 1111.

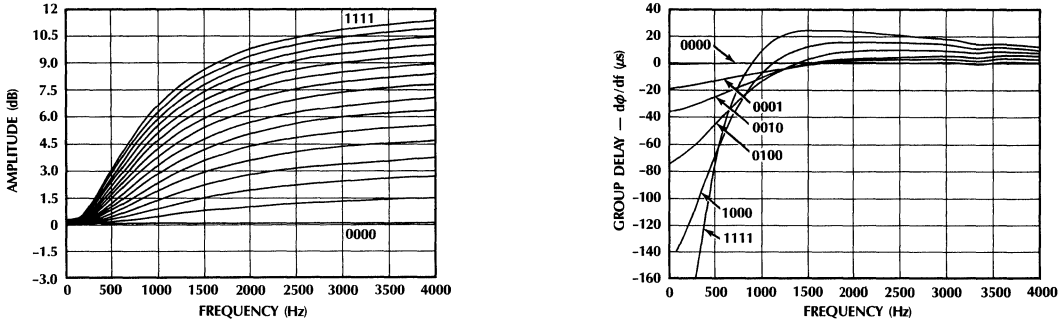


Figure 3. Typical Slope Filter Response — NL/L = 1

B3–B0, H3–H0 = 0000, S3–S0 = 0000 to 1111.

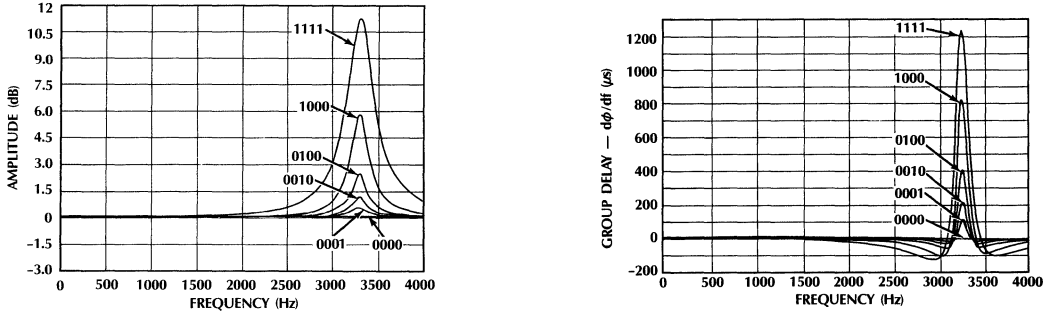


Figure 4. Typical Height Filter Response — NL/L = 0

B3–B0, S3–S0 = 0000; H3–H0 = 0000 to 1111.

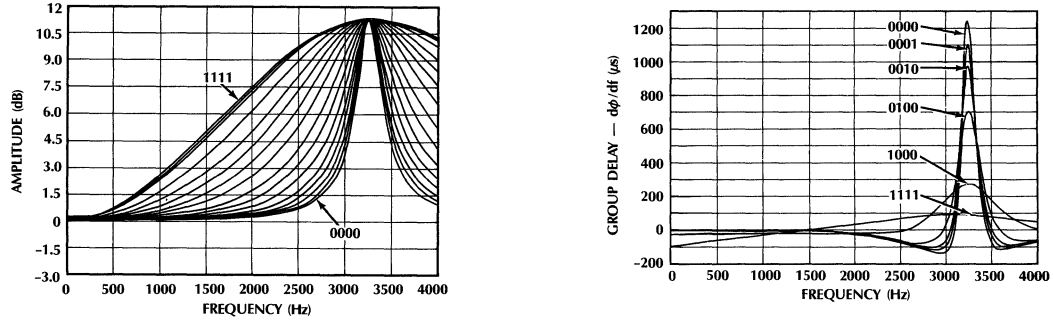


Figure 5. Typical Bandwidth Filter Response — NL/L = 0

H3–H0 = 1111; S3–S0 = 0000; B3–B0 = 0000 to 1111.

1.0 FUNCTIONAL DESCRIPTION

The ML2021 consists of a continuous anti-alias filter, three programmable switched capacitor equalization filters, an output smoothing filter, an output driver, and a digital section for the serial interface.

1.1 ANTI-ALIAS FILTER

The first section is a continuous anti-alias filter. This filter is needed to prevent aliasing of high frequency signals present on the input into the passband by the sampling action of the switched capacitor filters. This section is a continuous second order lowpass filter with a typical 3dB frequency at 20kHz and 30dB of rejection at 124kHz.

1.2 EQUALIZATION FILTERS

The programmable filters implement a family of frequency response curves intended to compensate for the response of telephone lines.

This filter is composed of three distinct sections: slope, height, and bandwidth.

1.2.1 RESPONSE OF SLOPE, HEIGHT, AND BANDWIDTH

The family of response curves generated by the slope section are shown in Figures 2 and 3. There are 4 slope select bits, S3-S0. These bits alter the slope of the highpass response under 1000Hz, and as a result, the absolute gain above 1000Hz will be unique for each setting. Table 1 gives typical 1kHz gain values for all slope settings.

Table 1. Typ. 1kHz Gain for Slope Settings

Slope Setting	Rel 1kHz Gain (dB)	
	NL/L=1	NL/L=0
0	0.0	Rel
1	0.4	1.4
2	0.9	2.6
3	1.4	3.7
4	1.8	4.7
5	2.3	5.5
6	2.8	6.3
7	3.4	7.2
8	3.7	7.8
9	4.2	8.4
10	4.6	9.0
11	5.0	9.5
12	5.4	10.0
13	5.8	10.5
14	6.2	11.0
15	6.6	11.4

HT, BW Bits=0

There is an additional bit, NL/L, that also affects the highpass response of the slope filter. The slope response curves in Figure 2 are with NL/L=0. These same response curves are shown in Figure 3 with NL/L=1. Notice that the NL/L bit adds more droop in the highpass response below 2500Hz.

The family of response curves generated by the height section are shown in Figure 4. There are 4 height select bits, H3-H0. This section creates a peak in the response at 3250Hz and this filter controls the amount of peaking. Table 2 gives typical 1kHz gain values for all height and bandwidth settings.

Table 2. Typ. 1kHz Gain for HT and BW Settings

	Relative 1kHz Gain (dB)															
	HT Setting															
BW Setting	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Rel	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0.1
5	0	0	0	0	0	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1
6	0	0	0	0	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.1
7	0	0	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.2	0.2	0.2
8	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.2	0.2	0.3	0.3	0.4
9	0	0	0	0	0	0.1	0.1	0.1	0.1	0.2	0.2	0.3	0.3	0.4	0.5	0.6
10	0	0	0	0	0.1	0.1	0.1	0.1	0.2	0.3	0.3	0.4	0.5	0.6	0.7	0.8
11	0	0	0	0.1	0.1	0.1	0.2	0.2	0.3	0.4	0.4	0.5	0.7	0.8	0.9	1.1
12	0	0	0.1	0.1	0.1	0.2	0.2	0.3	0.4	0.5	0.7	0.8	1.0	1.1	1.4	1.6
13	0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.6	0.8	0.9	1.1	1.4	1.6	1.9	2.3
14	0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.7	0.8	1.0	1.2	1.5	1.7	2.0	2.4
15	0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.7	0.9	1.1	1.3	1.6	1.8	2.1	2.5

Slope Bits=0

The family of response curves generated by the bandwidth section is shown in Figure 5 There are 4 bandwidth select bits, B3-B0. This section causes the response of the 3250Hz peak to be widened, and as a result, this filter controls the bandwidth of the 3250Hz peaked region.

1.2.2 TRANSFER FUNCTION

The transfer function for the ML2021 is shown below. This transfer function is valid for magnitude response only. The actual magnitude response from an individual device may deviate from the computed response from the transfer function by typically 0–0.2dB.

$$H(s) = \frac{c(s+b)}{b(s+c)} \times \frac{\left[s^2 + h(\omega_o/Q)s + \omega_o^2\right]}{\left[s^2 + (\omega_o/Q)s + \omega_o^2\right]} \times \frac{\left[\sin(\pi f/fc)\right]}{(\pi f/fc)}$$

$s = j \times 256000 \times \tan(\pi f/128000)$

$\omega_o = 20463.77$

$fc = 128000$

b,c : See Table 3. (slope)

Q : See Table 4. (bandwidth)

h : See Table 5. (height)

Table 3. Slope Response Factors (b, c)

S3–0	b NL/L = 0	b NL/L = 1
0000	2.371759E+03	1.116280E+04
0001	1.985920E+03	9.345141E+03
0010	1.701779E+03	8.007156E+03
0011	1.493571E+03	7.026999E+03
0100	1.326721E+03	6.241681E+03
0101	1.196668E+03	5.629636E+03
0110	1.087277E+03	5.114881E+03
0111	9.983588E+02	4.696487E+03
1000	9.179889E+02	4.318339E+03
1001	8.537864E+02	4.016273E+03
1010	7.966049E+02	3.747249E+03
1011	7.478074E+02	3.517676E+03
1100	7.035099E+02	3.309279E+03
1101	6.651771E+02	3.128945E+03
1110	6.299477E+02	2.963214E+03
1111	5.990361E+02	2.817797E+03

S3–0	c NL/L = 0	c NL/L = 1
XXXX	2.371759E+03	1.116280E+04

Table 4. Slope Response Factors (b, c)

B3–0	Q
0000	17.444906
0001	15.386148
0010	13.652451
0011	11.593677
0100	9.859960
0101	8.017864
0110	6.392453
0111	5.092080
1000	3.900003
1001	3.141338
1010	2.599369
1011	2.165724
1100	1.731965
1101	1.406509
1110	1.352248
1111	1.297981

Table 5. Height Response Factors (h)

Code	h
0000	1.000000
0001	1.071519
0010	1.148154
0011	1.230269
0100	1.318257
0101	1.445438
0110	1.603245
0111	1.757924
1000	1.949845
1001	2.137962
1010	2.317395
1011	2.540973
1100	2.786121
1101	3.019951
1110	3.311311
1111	3.672823

1.2.3 GROUP DELAY

The difference between the ML2020 and ML2021 is the elimination of a 60Hz highpass filter in order to eliminate positive group delay at low frequency.

The group delay through the ML2021 can be minimized such that less than 50μs of group delay can be achieved in both unloaded and cable loaded conditions relative to 1804Hz in the frequency range of 504 to 3004Hz. Minimum group delays are dependent upon using the proper setting for slope, height, and bandwidth for a give equalization requirement.

1.3 SMOOTHING FILTER

The equalizer filters are followed by a continuous second order smoothing filter that removes the high frequency sample information generated by the action of the switched capacitor filters. This filter provides a continuous analog signal at the output, V_{OUT} .

1.4 OUTPUT BUFFER

The final stage in the ML2020 is the output buffer. This amplifier has internal gain of 1 and is capable of driving 600Ω, 100pF loads. Thus, it is suitable for driving telephone hybrids directly without any external amplifier.

1.5 BYPASS MODE

The filter sections can be bypassed by setting the bypass data bit, $\overline{BP}$, to 0. Since the switched capacitor filters are bypassed in this mode, frequency response effects of the switched capacitor filters are eliminated. Thus, this mode offers very flat response and low noise over the 300–4000Hz frequency range.

1.6 FILTER CLOCK

The master clock, CLK, is used to generate the internal clocks for the switched capacitor filters. The frequency of CLK can be either 1.544MHz or 1.536MHz. However, the internal clock frequency must be kept at 1.536MHz to guarantee accurate frequency response. The CLKSEL pin enables a bit swallower circuit to keep the internal clock frequency set to 1.536MHz. When 1.544MHz clock is used, CLKSEL should be set to logic level 0, and one bit out of every 193 bits is removed (swallowed) to reduce the internal frequency to 1.536MHz. When 1.536MHz clock is used, CLKSEL should be set to logic level 1, and the internal clock rate is the same as the external clock rate.

1.7 SERIAL INTERFACE

The architecture of the digital section is shown in the preceding block diagram.

A timing diagram for the serial interface is shown in Figure 6. The serial input data, SID, is loaded into a shift register on rising edges of the shift clock, SCK. The data word is parallel loaded into a latch when the input latch signal, LATI, is high. The LATI pulse must occur when SCK is low. A new data word can be loaded into the shift register without disturbing the existing data word in the latch.

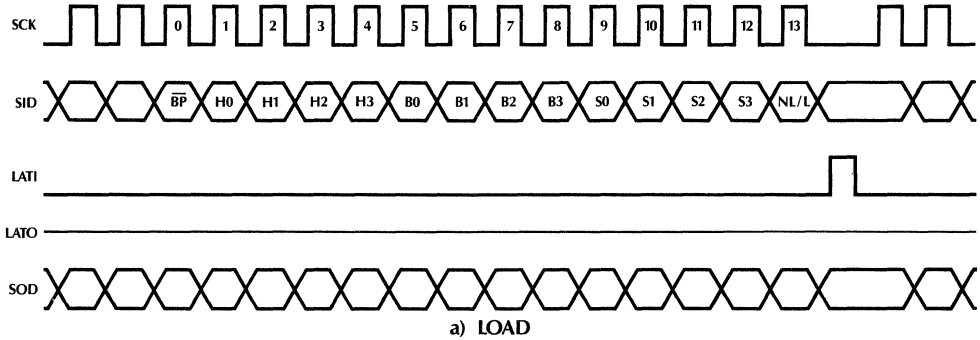
The parallel outputs of the latch control the filter response curves. The order of the data word bits in the latch is shown in Figure 7.

Note that bit 0 is the first bit of the data word clocked into the shift register.

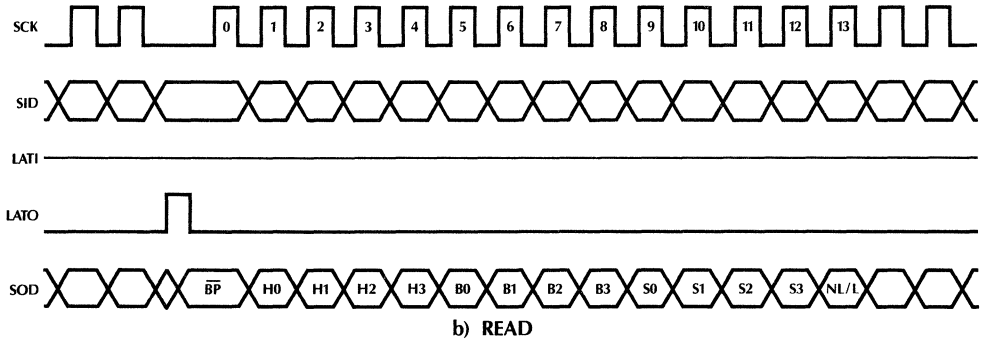
The device has the capability to read out the data word stored in the latch. This is done by parallel loading the data from the latch back into the shift register when the latch signal, LATO, is high. The LATO pulse must occur when SCK is low. Then, the data word can be shifted out of the register serially to the output, SOD, on falling edges of the shift clock, SCK.

The loading and reading of the data word can be done continuously or in bursts. Since the shift register and latch circuitry inside the device is static, there are no minimum frequency requirements on the clocks or data pulses. However, there is some coupling of the digital signals into the analog section. If this coupling is undesirable, the data can be clocked in bursts during non critical intervals, or the data rate can be done at a frequency outside the analog frequency range.

The clocks used to shift and latch data (SCK, LATI, LATO) are not related internally to the master clock and can occur asynchronous to CLK.



a) LOAD



b) READ

Figure 6. Serial Timing

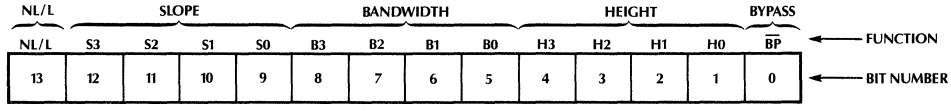


Figure 7. 14-Bit Latch

1.8 POWERDOWN MODE

A powerdown mode can be selected with pin P_{DN}. When $P_{DN}=1$, the device is powered down. In this state, the power consumption is reduced by removing power from the analog section and forcing the analog output, V_{OUT}, to a high impedance state. While the device is in power down mode, the digital section is still functional and the current data word remains stored in the latch. The master clock, CLK, can be left active or removed during powerdown mode. When $P_{DN}=0$, the device is in normal operation.

1.9 POWER SUPPLIES

The digital section inside the device is powered between V_{CC} and GND, or 5 volts. The analog section is powered between V_{CC} and V_{SS}, or ±5 volts. The analog section uses AGND as the reference point.

GND and AGND are totally isolated inside the device to minimize coupling from the digital section into the analog section. Typically this is less than 100μV. However, AGND and GND should be tied together physically near the device and close to the common power supply ground connection.

The power supply rejection of V_{CC} and V_{SS} to the analog output is greater than −60dB at 1kHz, typically. If decoupling of the power supplies is still necessary in a system, V_{CC} and V_{SS} should be decoupled with respect to AGND.

2.0 APPLICATIONS

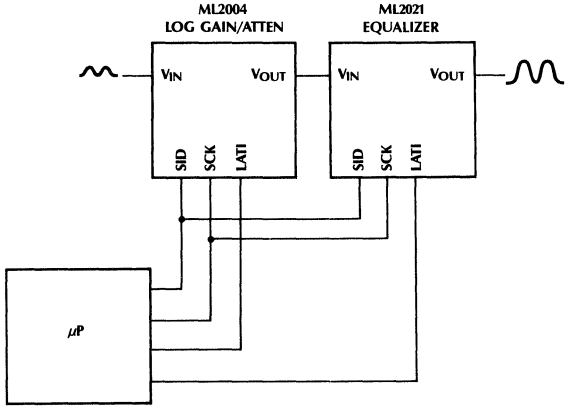


Figure 8. Typical Serial Interface

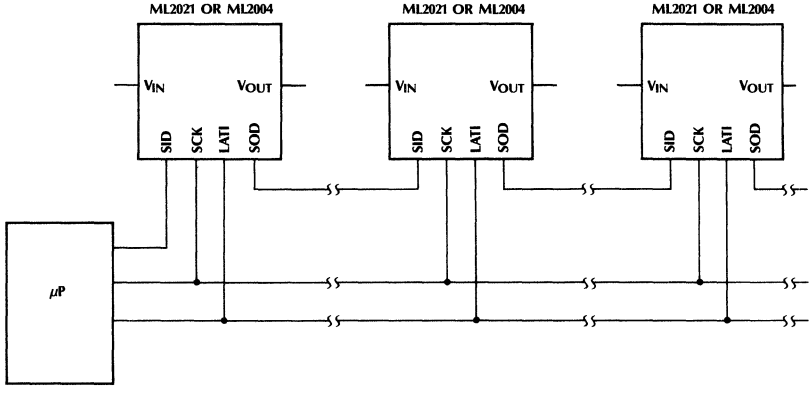


Figure 9. Controlling Multiple ML2021 and ML2004 With Only 3 Digital Lines Using One Long Data Word

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML2021CP	0°C to +70°C	MOLDED DIP (P16)
ML2021CS	0°C to +70°C	MOLDED SOIC (S18W)
ML2021IJ	–40°C to +85°C	HERMETIC DIP (J16)
ML2021IP	–40°C to +85°C	MOLDED DIP (P16)
ML2021IS	–40°C to +85°C	MOLDED SOIC (S18W)

ML2031, ML2032

Tone Detector

GENERAL DESCRIPTION

The ML2031 and ML2032 are monolithic tone detectors intended for telecommunication applications utilizing 4-wire loopback capability. The device meets or exceeds the 4-wire Maintenance Terminating Unit (MTU) requirements outlined in BELL PUB 43004.

These devices incorporate a 2713 Hz tone detector, clock oscillator, and uncommitted op amp in an 8-pin DIP. No external components are required.

The ML2031 or ML2032 can be used to detect frequencies of 1004 Hz or 2600 Hz, as the tone detector frequency template from 1000 Hz to 4000 Hz is proportional to the frequency of the external clock.

The ML2031 has two clock outputs. $CLK_{OUT}1$ is one half the frequency of CLK_{IN}, while $CLK_{OUT}2$ is one eighth of the frequency of CLK_{IN}. The ML2032 has an uncommitted op amp instead of the clock outputs.

The ML2031 and ML2032 are implemented in a double polysilicon CMOS technology.

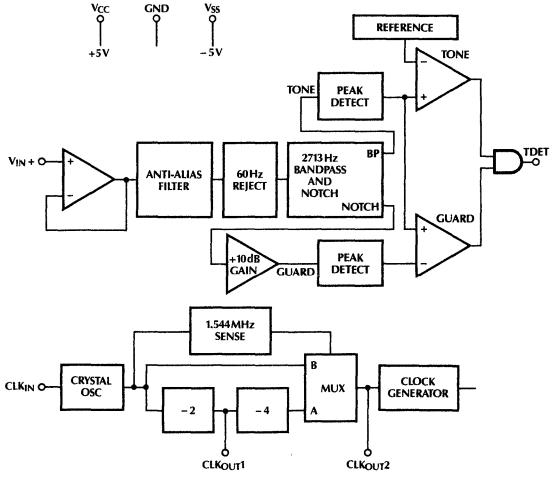
FEATURES

- Meets or exceeds BELL PUB 43004 requirements
- Extended dynamic range detect −34 dBm to +6 dBm
  no detect ≤ −40 dBm
- Frequency template ($f_{CLK\ IN}$ = 12MHz)
  detect 2713 ± 10Hz
  no detect 2713 ± 36Hz
- General purpose tone detect range of 1000Hz to 4000Hz
- Signal-to-guard ratio 8dB to 13dB
- No external components required
- Continuous anti-alias filter
- 60 Hz reject filter
- ±5 V supplies
- Clock input 12.352 MHz, 1.544 MHz, or a 12.352 MHz crystal
- ML2031 has clock outputs of 1.544 MHz and 6.176 MHz
- Tone detection of 1000 Hz to 4000 Hz proportional to external clock
- ML2032 has uncommitted op amp
- 8-pin dual-in-line package

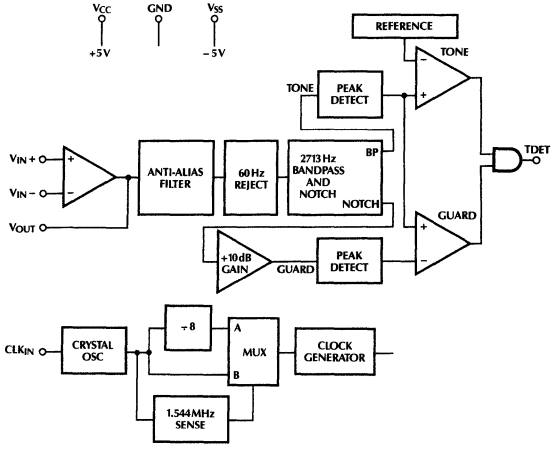
3

BLOCK DIAGRAMS

ML2031

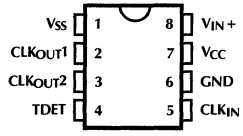


ML2032



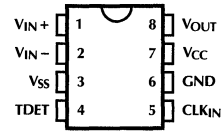
PIN CONNECTIONS

ML2031



TOP VIEW

ML2032



TOP VIEW

PIN DESCRIPTIONS

ML2031

PIN NO.	NAME	FUNCTION
1	V_{SS}	Negative supply. −5V ± 10%
2	$CLK_{OUT}1$	Clock output. Digital output from oscillator divided by 2.
3	$CLK_{OUT}2$	Clock output. Digital output from oscillator divided by 8.
4	TDET	Tone detect output. Digital output which indicates when valid 2713 Hz tone is present on analog input.
5	CLK_{IN}	Clock input. Internal clock can be generated by tying a 12.352 MHz crystal between this pin and GND, or by applying a 12.352 MHz or 1.544 MHz clock to this pin.
6	GND	Ground. Analog and digital inputs and outputs are referenced to this point.
7	V_{CC}	Positive supply. +5V ± 10%
8	$V_{IN}+$	Analog input.

ML2032

PIN NO.	NAME	FUNCTION
1	$V_{IN}+$	Positive Analog input. Positive input to the uncommitted op amp.
2	$V_{IN}-$	Negative Analog input. Negative input to the uncommitted op amp.
3	V_{SS}	Negative supply. −5V ± 10%
4	TDET	Tone detect output. Digital output which indicates when valid 2713 Hz tone is present on analog input.
5	CLK_{IN}	Clock input. Internal clock can be generated by tying a 12.352 MHz crystal between this pin and GND, or by applying a 12.352 MHz or 1.544 MHz clock to this pin.
6	GND	Ground. Analog and digital inputs and outputs are referenced to this point.
7	V_{CC}	Positive supply. +5V ± 10%
8	V_{OUT}	Analog output. Output of the uncommitted op amp.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} ..... +6.5V
- V_{SS} ..... −6.5V
- Analog Input and Output ..... V_{SS} −0.3V to V_{CC} +0.3V
- Digital Input and Outputs ..... −0.3V to V_{CC} +0.3V
- Input Current Per Pin ..... ±25mA
- Power Dissipation 750mW
- Storage Temperature Range ..... −65°C to +150°C
- Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2031CP, ML2032CP ..... 0°C to +70°C
- ML2031IJ, ML2032IJ ..... −40°C to +85°C

Supply Voltage
- V_{CC} ..... 4V to 6V
- V_{SS} ..... −4V to −6V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, $CLK_{IN} = 12.352MHz \pm 1200Hz$, or $CLK_{IN} = 1.544MHz \pm 150Hz$, $C_L = 100pF$, dBm measurements use 600Ω as reference load, uncommitted op amp in unity gain configuration.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
TONE DETECT							
f_{TD}	Tone Detection Frequency	4	V_{IN} = +6dBm to −34dBm	2703		2723	Hz
f_{TR}	Tone Rejection Frequency	4		2679		2747	Hz
A_{TD}	Tone Detection Amplitude	4	V_{IN} = 2703 Hz to 2723 Hz	−34		+6	dBm
A_{TR}	Tone Rejection Amplitude	4		−40			dBm
SGM	Signal to Guard Margin	4	800 Hz 1400 Hz 2000 Hz 2450 Hz Signal = −13 dBm, 2713 Hz. See BELL PUB 43004 sec. 2.4 for test method	8 8 8 8		13 13 13 13	dB dB dB dB
SFI	SF Tone Immunity	5	V_{IN} + = 2600 Hz No tone detect			+6	dBm
t_{TD}	Tone Detect Delay	4	V_{IN}+ = −8dBm, 2713 Hz Figure 1	0	10	30	ms
t_{TR}	Tone Removal Delay	4	V_{IN}+ = −8dBm, 2713 Hz Figure 1	0	4	30	ms
OP AMP							
V_{INR}	Input Voltage Range	5		±3			V
V_{OSW}	Output Voltage Swing	4	ML2032 Only	±3			V
V_{OS}	Input Offset Voltage	4	ML2032 Only			±20	mV
Z_{IN}	Input Impedance	4		1			MΩ
A_{VOL}	DC Open Loop Gain	4		1k	5k		V/V
f_{UG}	Unity Gain Frequency	5		0.5	1		MHz
I_{CN}	Noise- Input Referred	5	C msg weighted 1kHz		−9	−3 375	dBrnc nv/√Hz

3

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, $CLK_{IN} = 12.352MHz \pm 1200Hz$, or $CLK_{IN} = 1.544MHz \pm 150Hz$, $C_L = 100pF$, dBm measurements use 600Ω as reference load, uncommitted op amp in unity gain configuration.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
DIGITAL AND DC							
V_{IL}	Input Low Voltage, CLK_{IN}	4				1.5	V
V_{IH}	Input High Voltage, CLK_{IN}	4		3.5			V
I_{IN}	Input Current, CLK_{IN}	4	CLK_{IN} = 1.5V to 3.5V		10	60	μA
			CLK_{IN} = 0 to 1.5V; 3.5V to V_{CC}		150	500	μA
C_{IN}	Input Capacitance, CLK_{IN}	5			11		pF
V_{OL}	Output Low Voltage	4	I_{OL} = –2mA			0.4	V
V_{OH}	Output High Voltage	4	I_{OH} = 2mA	4.0			V
I_{CC}	V_{CC} Supply Current	4	No output load			7.5	mA
I_{SS}	V_{SS} Supply Current	4	No output load			–4.5	mA
CLOCK OUTPUT							
$f_{CLK}1$	$CLK_{OUT}1$ Output Frequency	4	Figure 2	½		½	$f_{CLK}1$
$f_{CLK}2$	$CLK_{OUT}2$ Output Frequency	4	Figure 2	⅛		⅛	$f_{CLK}1$
t_{1R}	$CLK_{OUT}1$ Output Rise Time	4	Figure 2, C_L = 50pF	0		20	ns
t_{1F}	$CLK_{OUT}1$ Output Fall Time	4	Figure 2, C_L = 50pF	0		20	ns
t_{2R}	$CLK_{OUT}2$ Output Rise Time	4	Figure 2, C_L = 50pF	0		20	ns
t_{2F}	$CLK_{OUT}2$ Output Fall Time	4	Figure 2, C_L = 50pF	0		20	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

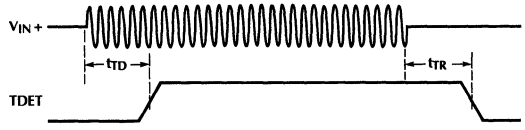
Note 2: 0°C to +70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

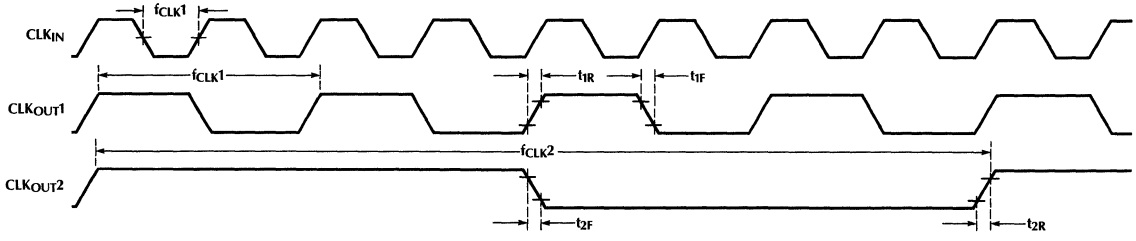
Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

TIMING DIAGRAMS



t_{TD} MEASURED FROM V_{IN} + ZERO CROSSING TO 1.4V MIDPOINT ON TDET
t_{TR} MEASURED FROM 1.4V MIDPOINT ON TDET TO ZERO CROSSING ON V_{IN} +

Figure 1. Tone Detect Timing



t_{1F}, t_{1R}, t_{2F}, t_{2R} MEASURED BETWEEN 0.8 and 2.0 VOLT TRANSITION POINTS
ALL OTHER PARAMETERS REFERRED TO 1.4V MIDPOINT

Figure 2. Digital Clock Output Timing

TYPICAL PERFORMANCE CURVE

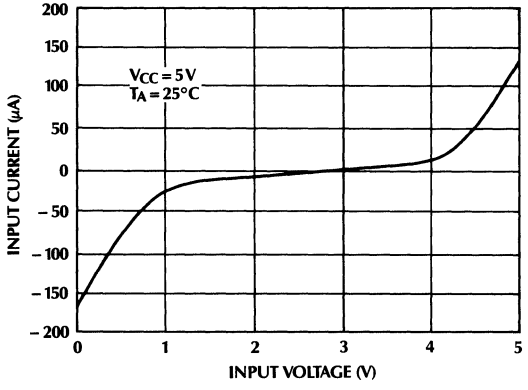


Figure 3. CLK_{IN} Input Current vs. Input Voltage

1.0 FUNCTIONAL DESCRIPTION

The ML2031 has a divide by 2 and divide by 8 clock output to drive external devices. The ML2032 has an uncommitted op amp. Refer to the block diagram.

1.1 Uncommitted Op Amp

The ML2032 features an uncommitted op amp. The ML2031 has the op amp connected in the unity gain configuration ($V_{IN}-$ internally tied to V_{OUT}).

The uncommitted op amp is a general purpose amplifier that can be used to interface the device with the analog telephone line. It has a high impedance input, a 0.5 MHz unity gain bandwidth, will drive a 1k, 100 pF load, and the input and output can swing within 1.5 V of the supplies.

1.2 Anti-Alias Filter

The anti-alias filter is a continuous second order low pass designed to prevent high frequency signals at the input from being aliased into the passband by the sampling action of the switched capacitor filters. The typical 3 dB corner frequency is 25 kHz and the typical rejection at 124 kHz is −30 dB.

1.3 60 Hz Reject Filter

The 60 Hz reject filter is a switched capacitor second order high pass designed to reject 60 Hz line interference on the analog input. The typical 3 dB corner frequency is 300 Hz and the typical rejection at 60 Hz is −24 dB.

1.4 Tone Detector

The tone detector is a monolithic block designed to indicate when a valid 2713 Hz tone is present on the analog input. A tone is valid if the following criteria are met:

1. 2713 Hz tone satisfies amplitude vs. frequency tone detector template shown in *Figure 4*.
2. The non-2713 Hz out of band energy present on the input is sufficiently small enough compared to the 2713 Hz tone (signal to guard margin).

The tone detector consists of 2713 Hz bandpass and notch filters, tone and guard peak detectors, tone and guard comparators, reference, and digital output buffer.

The analog signal first goes through the 2713 Hz bandpass and notch switched capacitor filters. The bandpass filter outputs any 2713 Hz signal (tone), and the notch filter outputs any non-2713 Hz signals (guard) in the range of 300–4500 Hz, respectively.

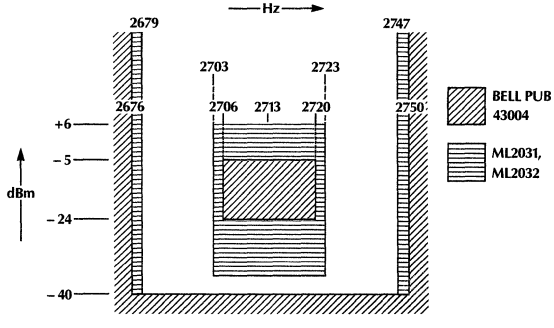


Figure 4. Tone Detector Template

The tone and guard signals then go to peak detectors which output a DC voltage proportional to the 2713 Hz and non-2713 Hz energy present on the analog input.

The tone comparator compares the tone energy to a fixed reference value to determine if it meets the amplitude requirements for tone detection shown in *Figure 4*.

The guard comparator compares the tone energy to the guard energy to determine if the signal to guard margin is met.

If both comparators indicate that a 2713 Hz tone and no out of band energy exists, the TDET output goes high indicating valid tone detection. If the signal comparator indicates insufficient signal energy or the guard comparator indicates too much out of band energy, then the TDET output stays low indicating invalid tone output.

1.5 Crystal Oscillator/Clock Generator

The crystal oscillator/clock generator generates the necessary internal clocks from either an external clock or an external crystal.

If an external clock input is used to drive CLK_{IN}, the input frequency can either be 12.352 MHz or 1.544 MHz in order to meet the frequency template. The device has an internal frequency sense circuit that can sense the difference between 12.352 MHz and 1.544 MHz and makes the necessary changes in the clock generator to accomodate either frequency at the input.

If a crystal is used, a 12.352 MHz crystal must be connected between CLK_{IN} and GND. This unique 1-pin crystal oscillator does not generally require any external capacitors or other external components to meet the frequency template. The crystal should be physically placed as close as possible to the CLK_{IN} pin to minimize stray inductances and capacitances.

The crystal must have the following characteristics:

1. Parallel resonant type
2. Frequency: 12.352000 MHz
3. Tolerance: ±0.005% @ 25°C
4. Less than 0.005% variation over desired temperature range
5. Maximum equivalent series resistance of 15 Ω at a drive level of 1 μW to 200 μW
6. Maximum equivalent series resistance of 30 Ω at drive levels of 10 nW to 1 μW
7. Typical load capacitance: 18 pF
8. Maximum case capacitance: 5 pF

The frequency of oscillation will be a function of the crystal parameters and board capacitance. If the final oscillation frequency is different than the ideal 12.352 MHz, the template frequencies will change according to the formulas outlined in section 1.6. If the crystal meets the above recommended parameters and typical PC board capacitance from CLK_{IN} to GND is 2 pF, then the device will meet the template specifications. Crystals that meet these requirements are M-tron 3709-010 12.352 for 0°C to +70°C and 3709-020 12.352 for −40°C to +85°C operation.

1.0 FUNCTIONAL DESCRIPTION (Continued)

The ML2031 has two clock outputs that can be used to drive other external devices. The $CLK_{OUT}1$ output is a buffered output from the oscillator divided by 2. The $CLK_{OUT}2$ output is a buffered output from the oscillator divided by 8. If a 12.352MHz clock or crystal is used, $CLK_{OUT}1 = 6.176$MHz and $CLK_{OUT}2 = 1.544$MHz.

1.6 Detecting Tones from 1000 Hz to 4000 Hz

The tone detector frequency template shown in *Figure 5* is proportional to the frequency of CLK_{IN}. Thus, the device can be set to a center frequency (other than 2713 Hz) by adjusting CLK_{IN} frequency.

The external clock frequency, $fCLK_{IN}$, needed to produce a given center frequency, can be calculated by:

$$fCLK_{IN} = f_C \times 4552.893$$

once $fCLK_{IN}$ has been determined, the other template frequency points shown in *Figure 5* can be calculated by:

$$f_{DL} = fCLK_{IN} \times 2.18831 \times 10^{-4}$$

$$f_{DU} = fCLK_{IN} \times 2.20450 \times 10^{-4}$$

$$f_{RL} = fCLK_{IN} \times 2.16888 \times 10^{-4}$$

$$f_{RU} = fCLK_{IN} \times 2.22393 \times 10^{-4}$$

The above formulas are valid for center frequencies with the range of 1000 Hz to 4000 Hz. The internal divide by 8 circuitry may be bypassed by applying a clock that is one eighth of the above calculated values.

When the required CLK_{IN} frequency calculated above is less than 6MHz, the internal frequency sense circuit may become enabled causing the detection of an erroneous center frequency. In this case, the divide by 8 function cannot be used and only the lower clock frequency may be used. For example, for a 1004 Hz tone detector, the clock frequency applied must be 571kHz.

1.7 Power Supplies

The analog circuits in the device run from +5 to −5 (V_{CC} to V_{SS}) and are referenced to GND.

The digital circuits in the device run from +5 to 0 (V_{CC} to GND).

It is recommended that the power supplies to the device be bypassed by placing decoupling capacitors from V_{CC} to GND and V_{SS} to GND as physically close to the device as possible.

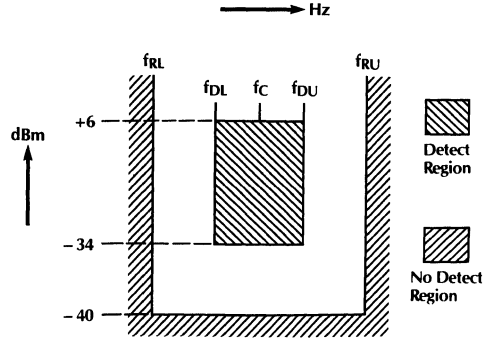


Figure 5. Tone Detector Template

2.0 APPLICATIONS

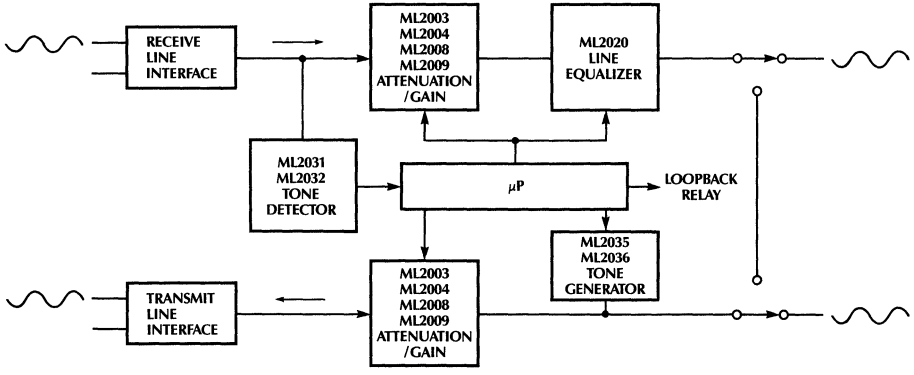


Figure 6. 4-Wire Termination Equipment

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML2031CP	0°C to +70°C	MOLDED DIP (P08)
ML2031IP	–40°C to +85°C	MOLDED DIP (P08)
ML2032CP	0°C to +70°C	MOLDED DIP (P08)
ML2032IP	–40°C to +85°C	MOLDED DIP (P08)

ML2035, ML2036

Programmable Sinewave Generator

GENERAL DESCRIPTION

The frequency of these monolithic sinewave generators is programmable for the ML2035 from DC to 25kHz and for the ML2036 from DC to 50kHz. No external components are required.

The frequency of the sinewave output is derived from either an external crystal or clock input, thus providing a stable and accurate frequency reference. The frequency is programmed by a 16-bit serial data word.

The ML2035 is packaged in an 8-pin DIP and has a V_{OUT} amplitude of $\pm V_{CC}/2$.

The ML2036 provides for a V_{OUT} amplitude of either $\pm V_{REF}$ or $\pm V_{REF}/2$. Also included with the ML2036 is an inhibit input which allows the sinewave output to be held at zero volts after completing the last half cycle of the sinewave preventing steps in voltage. Two pins of the ML2036 are clock outputs designed to drive other devices with one half or one eighth of the clock input frequency.

The ML2035 and ML2036 are intended for telecommunications and modem applications that need low cost and accurate generation of precise test tones, call progress tones, and signaling tones.

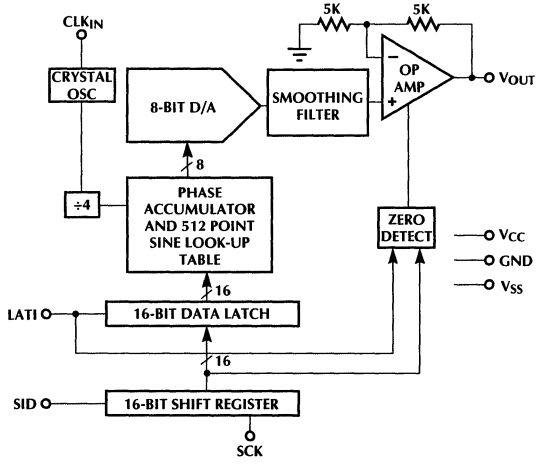
FEATURES

- Programmable frequency DC to 50kHz
- Frequency resolution with f_{CLKIN} = 12MHz (±0.75Hz) 1.5Hz
- Absolute gain error ±0.1dB max
- Harmonic distortion –45dB max
- Output voltage amplitude of $\pm V_{REF}$ or $\pm V_{REF}/2$
- On chip crystal oscillator 3 to 12MHz
- ML2036 has clock outputs of 1/2 or 1/8 of the input clock frequency
- No external components required
- µP compatible serial interface
- Double buffered data latch
- Synchronous or asynchronous data loading capability
- Power dissipation 50mW max from ±5 supplies
- Compatible with ML2031 and ML2032 tone detector, and ML2004 logarithmic gain/attenuator
- TTL/CMOS compatible inputs
- ML2035 package 8-pin DIP; ML2036 14-pin DIP or 16-pin SOIC
- 0°C to +70°C or –40°C to +85°C operating temperature range

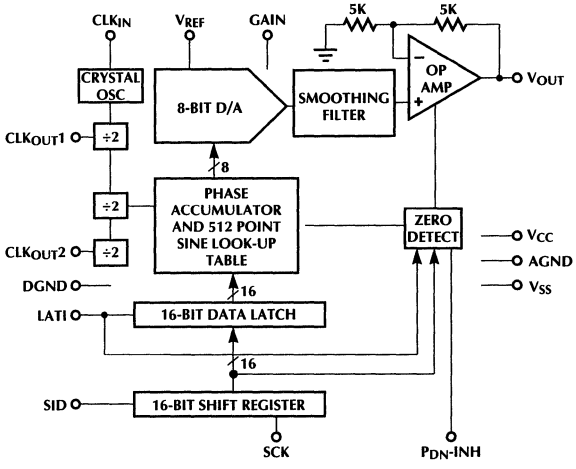
3

BLOCK DIAGRAMS

ML2035

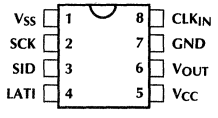


ML2036



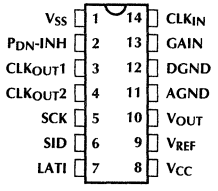
PIN CONFIGURATIONS

ML2035
8-Pin DIP (P08)



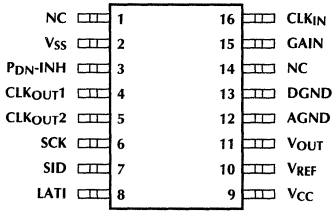
TOP VIEW

ML2036
14-Pin DIP (P14)



TOP VIEW

ML2036
16-Pin SOIC (S16W)



TOP VIEW

PIN DESCRIPTIONS

ML2035

PIN#	NAME	FUNCTION
1	V_{SS}	Negative supply. –5V ± 10%.
2	SCK	Serial clock. Digital input which clocks in serial data on rising edges.
3	SID	Serial data. Serial input data which programs the frequency of V_{OUT}.
4	LATI	Serial latch. Digital input which latches serial data into the internal data latch on falling edges.
5	V_{CC}	Positive supply. +5V ± 10%.
6	V_{OUT}	Analog output. V_{OUT} swing is $\pm V_{CC}/2$.
7	GND	Ground. 0 volts. All inputs and outputs referenced to this point.
8	CLK_{IN}	Clock input. Internal clock can be generated by tying a 3 to 12MHz crystal from this pin to GND or applying a clock directly to the pin.

ML2036

PIN# DIP	PIN# SOIC	NAME	FUNCTION
1	2	V_{SS}	Negative supply. –5V ± 10%.
2	3	P_{DN}-INH	Three level input. Controls inhibit mode and power down mode. Current source pull up to V_{CC}.
3	4	CLK_{OUT1}	Clock output. Digital output from internal clock generator that can drive other devices. $f_{CLKOUT1} = f_{CLKIN/2}$.
4	5	CLK_{OUT2}	Clock output. Digital output form internal generator that can drive other devices. $f_{CLKOUT2} = f_{CLKIN/8}$.
5	6	SCK	Serial clock. Digital input which clocks in serial data on rising edges.
6	7	SID	Serial data. Serial input data which programs the frequency of V_{OUT}.
7	8	LATI	Serial latch. Digital input which latches serial data into the internal data latch on falling edges.
8	9	V_{CC}	Positive supply. +5V ± 10%.
9	10	V_{REF}	Reference input. The voltage on this pin determines the peak-peak swing on V_{OUT}. V_{REF} can be tied to V_{CC}.
10	11	V_{OUT}	Analog output.
11	12	AGND	Analog ground. 0 volts. Analog inputs and outputs referenced to this point.
12	13	DGND	Digital ground. 0 volts. Analog inputs and outputs referenced to this point.
13	15	GAIN	Sets V_{OUT} peak amplitude to V_{REF} or $V_{REF}/2$. Current source pull down to DGND.
14	16	CLK_{IN}	Clock input. Internal clock can be generated by tying a 3 to 12MHz crystal from this pin to DGND or applying a clock directly to the pin.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} ..... +6.5V
- V_{SS} ..... –6.5V
- Analog Input and Output ..... V_{SS} – 0.3V to V_{CC} + 0.3V
- AGND Voltage ..... V_{SS} to V_{CC}
- Digital Inputs and Outputs ..... –0.3V to V_{CC} + 0.3V
- Input Current per Pin ..... ±25mA
- Power Dissipation 750mW
- Storage Temperature Range ..... –65°C to +150°C

Lead Temperature (soldering 10 sec)
- Dual-In-Line Package (Molded) ..... 260°C
- Dual-In-Line Package (Ceramic) ..... 300°C
- Molded Small Outline IC Package
  - Vapor Phase (60 sec) ..... 215°C
  - Infrared (15 sec) ..... 220°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2035CP, ML2036CP, ML2036CS ..... 0°C to +70°C
- ML2035IJ, ML2036IJ ..... –40°C to +85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ± 10%, V_{SS} = –5V ± 10%, CLK_{IN} = 12.352MHz, V_{OUT} load C_L = 100pF and R_L = 1k, all digital timing measured at 1.4V midpoint, and input control signals from 10% to 90% of V_{CC} with $t_R = t_F$ = 20ns.

SYMBOL	PARAMETER	NOTES	CONDITIONS		MIN	TYP	MAX	UNITS
Sinewave Generator								
HD	Harmonic Distortion	4	2nd or 3rd harmonic relative to fundamental	f_{OUT} = 20Hz to 5kHz			–45	dB
				f_{OUT} = 5kHz to 25kHz			–40	dB
SND	Signal to Noise + Distortion	4	200Hz ≤ f_{OUT} ≤ 3400Hz, noise measured 200Hz to 4kHz				–45	dB
			20Hz ≤ f_{OUT} ≤ 25kHz, noise measured 20Hz to 75kHz				–40	dB
ICN	Output Idle Channel Noise	4	Power Down Mode, Cmsg weighted			–20	0	dBrnc
			Power Down Mode, 1kHz			50		$nV/\sqrt{Hz}$
PSRR	Power Supply Rejection Ratio	5	200mV_{P-P}, 0–10kHz sine, measured on V_{OUT}	V_{CC}			–40	dB
				V_{SS}			–40	dB
V_{OS}	V_{OUT} Offset Voltage	4					±75	mV
V_{PK}	V_{OUT} Peak Voltage					±V_{CC}/2		V
V_{GN}	V_{OUT} Gain Error	4	Relative to V_{CC}	f_{OUT} = 20Hz to 5kHz			±0.1	dB
				f_{OUT} = 5kHz to 25kHz			±0.3	dB
Digital and DC								
V_{IL}, CLK	Input Low Voltage, CLK_{IN}	4					1.5	V
V_{IH}, CLK	Input High Voltage, CLK_{IN}	4			3.5			V
I_{IN}, CLK	Input Current, CLK_{IN}	4	CLK_{IN} = 1.5V to 3.5V			10	60	µA
			CLK_{IN} = 0 to 1.5V; 3.5V to V_{CC}				250	µA
C_{IN}, CLK	Input Capacitance, CLK_{IN}	5				12		pF
V_{IL}	Input Low Voltage	4					0.8	V
V_{IH}	Input High Voltage	4			2.0			V
I_{IL}	Input Low Current	4	V_{IN} = 0V		–1			µA
I_{IH}	Input High Current	4	V_{IN} = V_{CC}				1	µA
C_{IN}	Digital Input Capacitance					5		pF
V_{OL}	Output Low Voltage	4	I_{OL} = –2mA				0.4	V
V_{OH}	Output High Voltage	4	I_{OH} = 2mA		4.0			V

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP	MAX	UNITS
Digital and DC (Continued)							
I_{CC}	V_{CC} Supply Current	4	No output load, V_{CC} = 5.5V			5.5	mA
I_{SS}	V_{SS} Supply Current	4	No output load, V_{SS} = –5.5V, V_{CC} = 5.5V			–3.5	mA
I_{CCI}	V_{CC} Supply Current, Power Down Mode	4	No output load, Power Down Mode			2.0	µA
I_{SSI}	V_{SS} Supply Current, Power Down Mode	4	No output load, Power Down Mode			–100	µA
Digital Timing							
t_{CKI}	CLK_{IN} On/Off Period	4	$t_R = t_F$ = 10ns, 2.5V midpoint	30			ns
t_{SCK}	SCK On/Off Period	4		100			ns
t_{DS}	SID DATA Setup Time	4		50			ns
t_{DH}	SID DATA Hold Time	4		50			ns
t_{LPW}	LATI Pulse Width	4		50			ns
t_{LH}	LATI Hold Time	4		50			ns
t_{LS}	LATI Setup Time	5		50			ns

ML2036 ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ± 10%, V_{SS} = –5V ± 10%, AGND = DGND = 0V, V_{REF} = 2.5V to V_{CC}, and CLK_{IN} = 12.352MHz, V_{OUT} load C_L = 100pF and R_L = 1k, all digital timing measured at 1.4V midpoint, and input control signals from 10% to 90% of V_{CC} with $t_R = t_F$ = 20ns.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP	MAX	UNITS
Sinewave Generator							
HD	Harmonic Distortion	4, 6	2nd or 3rd harmonic relative to fundamental; f_{OUT} = 20Hz to 5kHz			–45	dB
			2nd or 3rd harmonic relative to fundamental; f_{OUT} = 5kHz to 50kHz			–40	dB
SND	Signal to Noise + Distortion	4, 6	200Hz ≤ f_{OUT} ≤ 3400Hz, noise measured 200Hz to 4kHz			–45	dB
			20Hz ≤ f_{OUT} ≤ 50kHz, noise measured 20Hz to 150kHz			–40	dB
ICN	Output Idle Channel Noise	4	Power Down Mode, Cmsg weighted		–20	0	dBrnc
			Power Down Mode, 1kHz		50		$nV/\sqrt{Hz}$
			Inhibit mode, 1kHz		500		$nV/\sqrt{Hz}$
PSRR	Power Supply Rejection Ratio	5	200mV$_{P-P}$, 0–10kHz sine, measured on V_{OUT}; V_{CC}			–40	dB
			200mV$_{P-P}$, 0–10kHz sine, measured on V_{OUT}; V_{SS}			–40	dB
V_{OS}	V_{OUT} Offset Voltage	4, 7				±(0.025 + V_{OUTP-P}/100)	V
V_{PK}	V_{OUT} Peak Voltage	6	GAIN = V_{CC}		±V_{REF}		V
			GAIN = DGND		±V_{REF}/2		V
V_{SW}	V_{OUT} Swing	5	GAIN = V_{CC}	V_{SS} + 1.5V		V_{CC} – 1.5V	V
V_{GN}	V_{OUT} Gain Error	4, 6	f_{OUT} = 20Hz to 5kHz			±0.1	dB
			f_{OUT} = 5kHz to 50kHz			±0.3	dB
R_{REF}	Reference Input Resistance	4		2.5	12		MΩ
Digital and DC							
V_{IL}, CLK	Input Low Voltage, CLK_{IN}	4				1.5	V
V_{IH}, CLK	Input High Voltage, CLK_{IN}	4		3.5			V
I_{IN}, CLK	Input Current, CLK_{IN}	4	CLK_{IN} = 1.5V to 3.5V		10	60	µA
			CLK_{IN} = 0 to 1.5V; 3.5V to V_{CC}			250	µA
C_{IN}, CLK	Input Capacitance, CLK_{IN}	5			12		pF
V_{IL}	Input Low Voltage	4	LATI, SID, GAIN, SCK			0.8	V
V_{IH}	Input High Voltage	4	LATI, SID, GAIN, SCL	2.0			V
I_{IL}	Input Low Current	4	V_{IN} = 0V, LATI, SID, GAIN, SCK	–1			µA
I_{IH}	Input High Current	4	V_{IN} = V_{CC}, LATI, SID, P_{DN}–INH, SCK			1	µA
I_{IL}, P_{DN}	Input Low Current	4	P_{DN}–INH, V_{IN} = 0V	–70	–20	–5	µA
I_{IH}, G	Input High Current	4	GAIN, V_{IN} = V_{CC}	5	20	70	µA
V_{I1}	Input Logic Low P_{DN}–INH	4		DGND–0.5		0.8	V
V_{I2}	Inhibit State Voltage P_{DN}–INH	4				V_{SS} + 0.5	V
V_{I3}	Input Logic High P_{DN}–INH	4		2.0			V
C_{IN}	Digital Input Capacitance				5		pF
V_{OL}	Output Low Voltage	4	I_{OL} = –2mA			0.4	V
V_{OH}	Output High Voltage	4	I_{OH} = 2mA	4.0			V

ML2036 ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP	MAX	UNITS
Digital and DC (Continued)							
I_{CC}	V_{CC} Supply Current	4	No output load, $V_{CC} = V_{REF} = 5.5V$			5.5	mA
I_{SS}	V_{SS} Supply Current	4	No output load, $V_{SS} = -5.5V$, $V_{CC} = V_{REF} = 5.5V$			–3.5	mA
I_{CCI}	V_{CC} Supply Current, Power Down Mode		No output load, power down mode			2.0	mA
I_{SSI}	V_{SS} Supply Current, Power Down Mode		No output load, power down mode			–100	µA
Digital Timing							
t_{CK1}	CLK_{IN} On/Off Period	4	$t_R = t_F = 10ns$, 2.5V midpoint	30			ns
t_{SCK}	SCK On/Off Period	4		100			ns
t_{DS}	SID DATA Setup Time	4		50			ns
t_{DH}	SID DATA Hold Time	4		50			ns
t_{LPW}	LATI Pulse Width	4		50			ns
t_{LH}	LATI Hold Time	4		50			ns
t_{LS}	LATI Setup Time	5		50			ns
Clock Output							
f_{CLK1}	CLK_{OUT1} Output Frequency	4	Figure 2	1/2		1/2	f_{CLKIN}
f_{CLK2}	CLK_{OUT2} Output Frequency	4	Figure 2	1/8		1/8	f_{CLKIN}
t_{1R}, t_{2R}	CLK_{OUT1}, CLK_{OUT2}, Output Rise Time	5	$C_L = 40pF$, 10% and 90% transition point	0		20	ns
		4	$C_L = 100pF$, 0.8V and 2.0V transition point	0		20	ns
t_{1F}, t_{2F}	CLK_{OUT1}, CLK_{OUT2}, Output Fall Time	5	$C_L = 40pF$, 10% and 90% transition point	0		20	ns
		4	$C_L = 100pF$, 0.8V and 2.0V transition point	0		20	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: 0°C to +70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 6: Maximum peak-to-peak voltage for output sinewave is $V_{OUTP-P} \leq (125kV \times Hz)/f_{OUT}$. For example at 50kHz output the maximum guaranteed voltage swing is $2.5V_{P-P}$.

Note 7: Offset voltage is a function of the peak-to-peak output voltage, for example if $V_{OUTP-P} = 2.5V$, $V_{OS} = \pm 50mV$ max.

TIMING DIAGRAMS

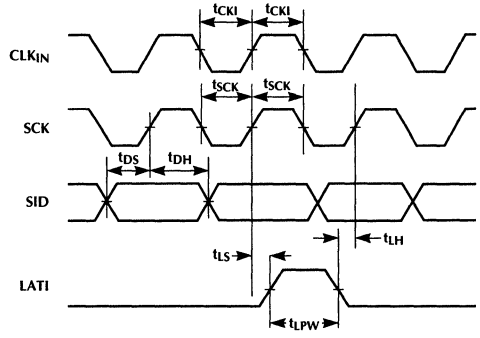
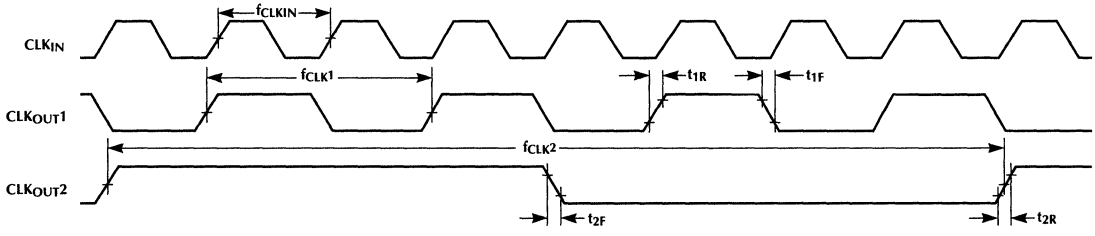


Figure 1. Serial Interface Timing.



fCLK PARAMETERS REFERRED TO 1.4V MIDPOINT

Figure 2. ML2036 Digital Clock Output Timing.

TYPICAL PERFORMANCE

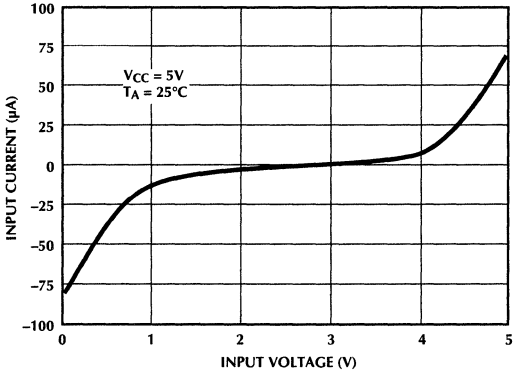


Figure 3. CLK_{IN} Input Current vs. Input Voltage.

1.0 FUNCTIONAL DESCRIPTION

The ML2035 and ML2036 are composed of a programmable frequency generator, sinewave generator crystal oscillator, and serial digital interface. The ML2035 and ML2036 frequency and sinewave generator functional block diagram is shown in figure 4.

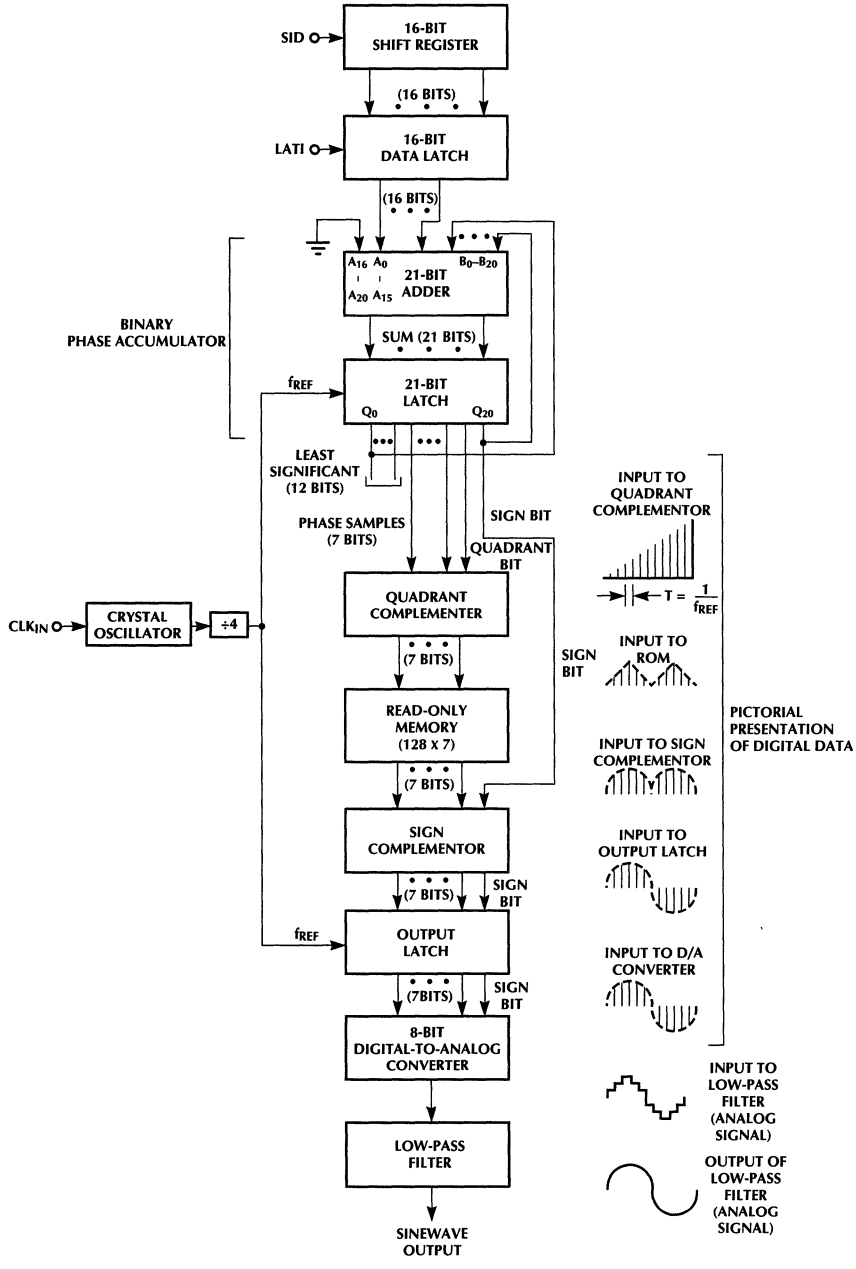


Figure 4. Frequency and Sinewave Generator Functional Block Diagram.

1.1 PROGRAMMABLE FREQUENCY GENERATOR

The programmable frequency generator produces a digital output whose frequency is determined by a 16-bit digital word.

The frequency generator is composed of a phase accumulator which is clocked at $f_{CLKIN/4}$. The value stored in the data latch is added to the phase accumulator every 4 cycles of CLK_{IN}. The frequency of the analog output is equal to the rate at which the accumulator overflows and is given by the following equation:

$$f_{OUT} = \frac{f_{CLKIN} \times (D15 - D0)_{DEC}}{2^{23}}$$

The frequency resolution and the minimum frequency are the same and is given by the following equation:

$$\Delta f_{MIN} = \frac{f_{CLKIN}}{2^{23}}$$

When f_{CLKIN} = 12.352MHz, Δf_{MIN} = 1.5Hz (±0.75Hz). Lower frequencies are obtained by using a lower clock.

Due to the phase quantization nature of the frequency generator spurious tones can be present in the output range of –55dB relative to fundamental. The energy from these tones is included in the signal to noise + distortion specification. The frequency of these tones can be very close to the fundamental, therefore it is not practical to filter them out.

1.2 SINEWAVE GENERATOR

The sinewave generator is composed of a sine look-up table, a DAC, and an output smoothing filter. The sine look-up table is addressed by the phase accumulator. The DAC is driven by the output of the look-up table and generates a staircase representation of a sinewave.

The output smoothing filter "smooths" the analog output by removing the high frequency sampling components. The resultant voltage on V_{OUT} is a sinusoid with all distortion components at least 45dB below the fundamental.

The ML2035 provides a peak sinewave voltage of $\pm V_{CC}/2$. The ML2036 has a V_{REF} input that can be tied to V_{CC} or generated from an external voltage. With the gain input equal to a logic "1" the sinewave peak voltage is equal to $\pm V_{REF}$; with the gain input equal to a logic "0" the peak voltage is $\pm V_{REF}/2$. The sinewave output is referenced to AGND for the ML2036 and GND for the ML2035.

The analog section is designed to operate over a range from DC to 50kHz. Due to slew rate limitations, the peak-to-peak output voltage must be limited to $V_{OUTP-P} \leq (125kV \times Hz)/f_{OUT}$. For example on the ML2036 an output at 50kH must be limited to $2.5V_{P-P}$. Since the ML2035 peak-to-peak output voltage is equal to V_{CC}, the maximum output frequency must be limited to 25kHz for V_{CC} = 5V. V_{OUT} can drive 1kΩ, 100pF loads and swing to within 1.5V of V_{CC} and V_{SS}, provided the slew rate limitations mentioned above are not exceeded.

The output offset voltage, V_{OS}, is a function of the peak-to-peak output voltage and is specified as

$$\pm\left(0.025 + \frac{V_{OUTP-P}}{100}\right)V_{MAX}.$$

For example, if V_{OUTP-P} = 2.5V

then $V_{OS} = \pm\left(0.025 + \frac{2.5}{100}\right)V_{MAX}$.

So, V_{OS} = ±0.050 V_{MAX}, or ± 50mV max.

1.3 CRYSTAL OSCILLATOR

The crystal oscillator generates an accurate reference clock for the programmable frequency generator.

The internal clock can be generated with a crystal or external clock.

If a crystal is used, it must be placed between CLK_{IN} and DGND of the ML2036 or GND of the ML2035. An on chip crystal oscillator will then generate the internal clock. No other external capacitors or components are required. The crystal should be a parallel resonant type with a frequency between 3MHz to 12.4MHz. It should be placed physically as close as possible to the CLK_{IN} and DGND (GND).

An external clock can drive CLK_{IN} directly if desired. The frequency of this clock can be anything from 0 to 12MHz.

The crystal must have the following characteristics:

1. Parallel resonant type
2. Frequency: 3MHz to 12.4MHz
3. Maximum equivalent series resistance of 15Ω at a drive level of 1µW to 200µW
4. Maximum equivalent series resistance of 30Ω at drive levels of 10nW to 1µW
5. Typical load capacitance: 18pF
6. Maximum case capacitance: 7pF

The frequency of oscillation will be a function of the crystal parameters and board capacitance. Crystals that meet these requirements at 12.352000MHz are M-tron 3709-010 12.352 for 0°C to +70°C and 3709-020 12.352 for –40°C to +85°C operation.

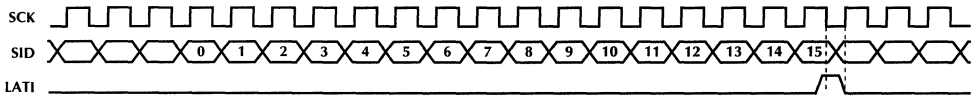


Figure 5. Serial Interface Timing

The ML2036 has two clock outputs that can be used to drive other external devices. The CLK_{OUT1} output is a buffered output from the oscillator divided by 2. The CLK_{OUT2} output is a buffered output from the oscillator divided by 8.

1.4 SERIAL DIGITAL INTERFACE

The digital interface consists of a shift register and data latch. The serial 16-bit data word on SID is clocked into a 16-bit shift register on rising edges of the serial shift clock, SCK. The LSB should be shifted in first and the MSB last as shown in figure 5. The data that has been shifted into the shift register is loaded into a 16-bit data latch on the falling edge of LATI. To insure that true data is loaded into the data latch from the shift register, LATI falling edge should occur when SCK is low, as shown in figure 1. LATI should be low while shifting data into the shift register to avoid inadvertently entering the power down mode as described in paragraph 1.5. Note that all data is entered and latched on edges, not levels, of SCK and LATI.

1.5 INHIBIT AND POWER DOWN MODES

1.5.1 ML2035 Power Down Mode

The power down mode of the ML2035 can be selected by entering all zeros in the shift register and applying a logic "1" to LATI and holding it high. A zero data detect circuit detects when all bits in the shift register are zero's. In this state, the power consumption is reduced to 11.5mW max, and V_{OUT} goes to 0V as shown in figure 6 and appears as 10k to analog ground. The master clock, CLK_{IN}, can be left active or removed during power down mode.

1.5.2 ML2036 Inhibit and Power Down Modes

The ML2036 has an inhibit mode and a power down mode which are controlled by the three-level P_{DN}–INH input as described in table 1. When a logic "1", V_{I3}, is applied to the P_{DN}–INH pin, the power down mode is entered in the same way as described for the ML2035. Also, the ML2036 will be placed in the power down mode by applying a logic "0" to the P_{DN}–INH pin.

If V_{SS} to V_{SS} + 0.5V, V_{I2}, is applied to the P_{DN}–INH pin, the inhibit mode is entered by shifting all zero's into the shift register and applying a logic "1" to the LATI pin. Once the inhibit mode is entered V_{OUT} will complete the last half cycle of the sinewave and then be held at approximately V_{OS}, such that no voltage step occurs, as shown in figure 6.

PART NUMBER	P_{DN}–INH MODE	P_{DN}–INH PIN	DATA IN SHIFT REG.	LATI	SINEWAVE OUTPUT
ML2036	P_{DN}(1)	V_{I1}, Logic "0"	X	X	V_{OUT} = 0V (10K to AGND)
ML2036	Inhibit	V_{I2}, Inhibit State Voltage, V_{SS} to V_{SS} + 0.5V	All 0's	Logic "1"	V_{OUT} goes to approximately V_{OS} at the next V_{OS} crossing. See figure 6.
ML2035 & ML2036	P_{DN}(1)	V_{I3}, Logic "1"	All 0's	Logic "1"	V_{OUT} = 0V (10K to AGND)

Note 1: In the power down mode, the oscillator, CLK_{OUT1} and CLK_{OUT2}, shift register, and data latch are all functional

Table 1. Three Level P_{DN}–INH Function.

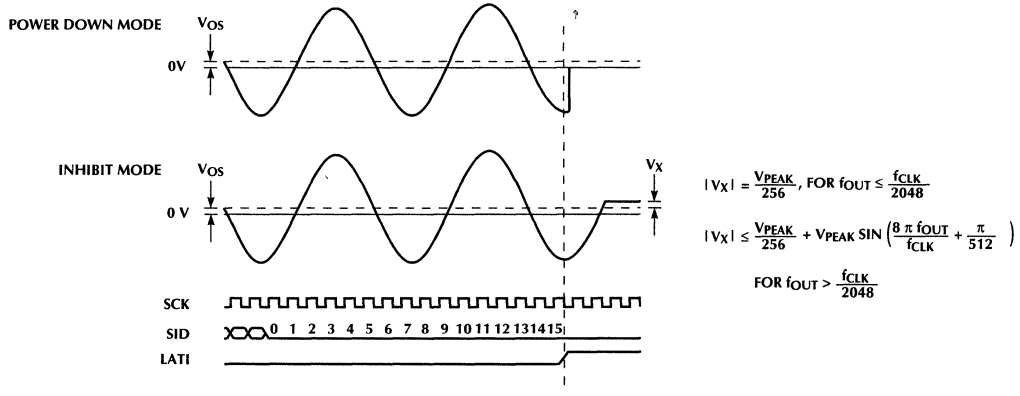


Figure 6. Power Down and Inhibit Mode.

1.6 POWER SUPPLIES

The analog circuitry in the device are powered from +5V to –5V (V_{CC} to V_{SS}) and are referenced to AGND.

The digital circuits in the device are powered from +5V to 0V (V_{CC} to DGND).

For the ML2036, it is recommended that AGND and DGND be connected together close to the device and have a good connection back to the power source.

It is recommended that the power supplies to the device should be bypassed by placing decoupling capacitors from V_{CC} to AGND (GND for ML2035) and V_{SS} to AGND (GND for ML2035) as physically close to the device as possible.

2.0 TYPICAL APPLICATIONS

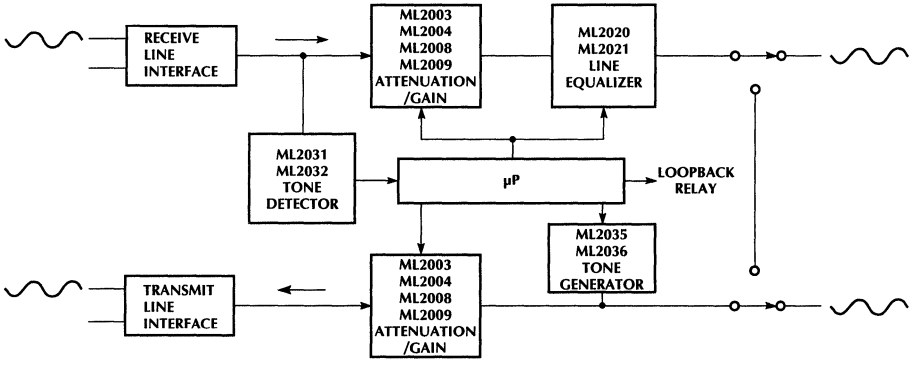


Figure 7. 4-Wire Termination Equipment.

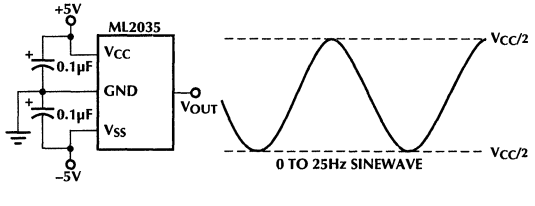


Figure 8. Sinewave Ratiometric to $\pm V_{CC}/2$.

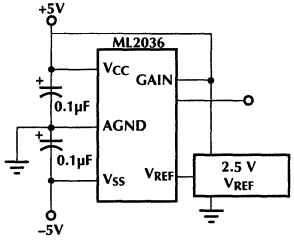


Figure 9. Sinewave with $\pm 2.5V_{P-P}$ ($5V_{P-P}$).

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2035IJ	–40°C to +85°C	Hermetic DIP (J08)
ML2035IP	–40°C to +85°C	Molded DIP (P08)
ML2036IJ	–40°C to +85°C	Hermetic DIP (J14)
ML2036IP	–40°C to +85°C	Molded DIP (P14)
ML2036IS	–40°C to +85°C	Molded SOIC (S16W)
ML2035CP	0°C to +70°C	Molded DIP (P08)
ML2036CP	0°C to +70°C	Molded DIP (P14)
ML2036CS	0°C to +70°C	Molded SOIC (S16W)

Micro Linear

ML2110

Universal Dual Filter

GENERAL DESCRIPTION

The ML2110 consists of two independent switched capacitor filters that perform second order filter functions such as lowpass, bandpass, highpass, notch and allpass. All filter configurations including Butterworth, Bessel, Cauer, and Chebyshev can be formed.

The center frequency of these filters is tuned by an external clock or the external clock and resistor ratio.

The ML2110 frequency range is specified to 30kHz with ±2.25V (single 5V operation) to ±5.5V power supplies.

For higher frequency operation the ML2111 is specified up to 150kHz operation.

These filters are ideal where center frequency accuracy and high Qs are needed.

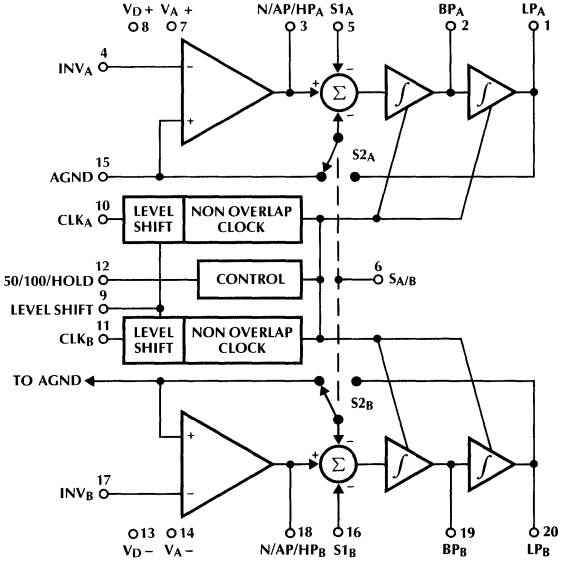
The ML2110 is a pin compatible superior replacement for MF10, LMF100, and LTC1060 filters.

FEATURES

- Specified to 30kHz
- Center frequency×Q product ≤2MHz
- Separate highpass, notch, allpass, bandpass, and lowpass outputs
- Center frequency accuracy ±0.3% or ±0.8% max
- Q accuracy ±3% or ±6% max
- Clock inputs TTL or CMOS compatible with duty cycle 40% to 60%
- Single 5V (±2.25V) or ±5V supply operation
- 0°C to 70°C, −40°C to +85°C, −55°C to +125°C operating temperature range
- Standard 0.3" 20-pin DIP or 20-pin small outline (SOIC) package

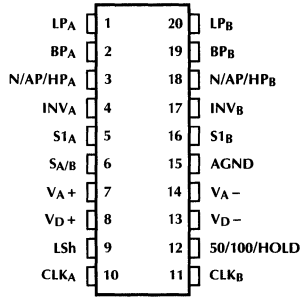
3

BLOCK DIAGRAM



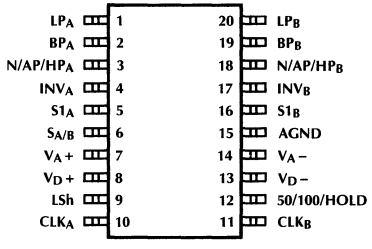
PIN CONNECTIONS

ML2110
20-PIN DIP



TOP VIEW

ML2110
20-PIN SOIC



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	LP_A	Lowpass output for biquad A.
2	BP_A	Bandpass output for biquad A.
3	$N/AP/HP_A$	Notch/allpass/highpass output for biquad A.
4	INV_A	Inverting input of the summing op amp for biquad A.
5	$S1_A$	Auxiliary signal input pin used in modes 1a, 1d, 4, 5, and 6b.
6	$S_{A/B}$	Controls S2 input function.
7	V_A+	Positive analog supply.
8	V_D+	Positive digital supply.
9	LSh	Reference point for clock input levels. Logic threshold typically 1.4V above LSh voltage.
10	CLK_A	Clock input for biquad A.
11	CLK_B	Clock input for biquad B.
12	50/100/HOLD	Input pin to control the clock to center frequency ratio of 50:1 or 100:1, or stops the clock to hold the last sample of the band-pass or lowpass outputs.
13	V_D-	Negative digital supply.
14	V_A-	Negative analog supply.
15	AGND	Analog ground.
16	$S1_B$	Auxiliary signal input used in modes 1a, 1d, 4, 5, and 6b.
17	INV_B	Inverting input of the summing op amp for biquad B.
18	$N/AP/HP_B$	Notch/allpass/highpass output for biquad B.
19	BP_B	Bandpass output for biquad B.
20	LP_B	Lowpass output for biquad B.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage
- $|V_A+|, |V_D+|-|V_A-|, |V_D-|$ 13V
- V_A+, V_D+ to LSh 13V

Inputs ..... $|V_A+, V_D+|+0.3V$ to $|V_A-, V_D-|-0.3V$
Outputs ..... $|V_A+, V_D+|+0.3V$ to $|V_A-, V_D-|-0.3V$
$|V_A+|$ to $|V_D+|$ ..... ±0.3V
Power Dissipation 750mW
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (soldering, 10 sec) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2110BCP, ML2110CCP, ML2110BCS, ML2110CCS ..... 0°C to 70°C
- ML2110BIJ, ML2110CIJ ..... −40°C to +85°C
- ML2110BMJ, ML2110CMJ ..... −55°C to +125°C

Supply Voltage Range ..... ±2.25V to ±6.0V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_A+ = V_D+ = 5V \pm 10\%$, $V_A- = V_D- = -5V \pm 10\%$, $C_L = 25pF$, $V_{IN} = 2.5V_{PK}$ (1.767 V_{RMS}) Clock Duty Cycle 40% to 60%.

			ML2110B			ML2110C			
PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	MIN	TYP NOTE 3	MAX	UNITS
Filter									
f_o, Center Frequency Maximum	5, 6	Figure 16 (Mode 1) $Q \le 50$, Q Accuracy $\le \pm 20\%$ $Q \le 20$, Q Accuracy $\le \pm 10\%$			20 30			20 30	kHz kHz
f_o, Center Frequency Minimum	5, 6	Figure 16 (Mode 1) $Q \le 50$, Q Accuracy $\le \pm 30\%$ $Q \le 20$, Q Accuracy $\le \pm 15\%$	25 25			25 25			Hz Hz
f_o, Temperature Coefficient		$f_{CLK} < 1MHz$		−10			−10	*	ppm/°C
Clock to Center Frequency Ratio	 4 4	Q = 10 Figure 16 (Mode 1) 50:1, $f_{CLK} = 250kHz$ 100:1, $f_{CLK} = 500kHz$	 49.85 100.0	 50.0 100.3	 50.15 100.6	 49.60 99.50	 50.0 100.3	 50.40 101.1	

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_A+ = V_D+ = 5V \pm 10\%$, $V_A- = V_D- = -5V \pm 10\%$, $C_L = 25pF$, $V_{IN} = 2.5V_{PK}$ (1.767 V_{RMS}) Clock Duty Cycle 40% to 60%.

PARAMETER	NOTES	CONDITIONS	ML2110B MIN	ML2110B TYP NOTE 3	ML2110B MAX	ML2110C MIN	ML2110C TYP NOTE 3	ML2110C MAX	UNITS
Filter (Continued)									
Clock Frequency	5	Q ≤ 20, Q Accuracy ≤ ±15%	2.5k		1.5M	2.5k		1.5M	Hz
Clock Feedthrough	5	$f_{CLK} \leq 1MHz$		10	20		10	20	mV(p-p)
Q Accuracy	4	f_o = 5kHz, Q = 10, Figure 16 (Mode 1) 50:1			±3			±6	%
		100:1			±4			±8	%
Q Temperature Coefficient		f_{CLK} < 500kHz, Q = 10		20			20		ppm/°C
DC Offset		50:1, f_{CLK} = 250kHz							
V_{OS} 2, 3	4	$S_{A/B}$ High		7	40		7	60	mV
V_{OS} 2, 3	4	$S_{A/B}$ Low		7	40		7	60	mV
DC Offset		100:1, f_{CLK} = 500kHz							
V_{OS} 2, 3	4	$S_{A/B}$ High		14	60		14	100	mV
V_{OS} 2, 3	4	$S_{A/B}$ Low		14	60		14	100	mV
Gain Accuracy									
DC Lowpass	4	R1 = 20k, R2 = 2k, R3 = 20k		0.01	2		0.01	2	%
Bandpass at f_o	4	100:1, f_o = 5kHz, Q = 10		1	4		1	8	%
DC Notch Output	5			0.02	2		0.02	2	%
Noise	7	Figure 16 (Mode 1) Q = 1, R1 = R2 = R3 = 2k							
		Bandpass, 5kHz, 50:1		80			80		μV_{RMS}
		5kHz, 100:1		100			100		μV_{RMS}
		Lowpass, 5kHz, 50:1		105			105		μV_{RMS}
		5kHz, 100:1		130			130		μV_{RMS}
		Notch, 5kHz, 50:1		80			80		μV_{RMS}
		5kHz, 100:1		100			100		μV_{RMS}
		Figure 16 (Mode 1) Q = 10, R1 = R3 = 20k, R2 = 2k							
		Bandpass, 5kHz, 50:1		256			256		μV_{RMS}
		5kHz, 100:1		315			315		μV_{RMS}
		Lowpass, 5kHz, 50:1		262			262		μV_{RMS}
		(R1 = 2k) 5kHz, 100:1		320			320		μV_{RMS}
		Notch, 5kHz, 50:1		33			33		μV_{RMS}
		(R1 = 2k) 5kHz, 100:1		38			38		μV_{RMS}
Crosstalk		f_{CLK} = 250kHz, f_o = 5kHz		−70			−70		dB
Filter, $V_A+ = V_D+ = 2.25V$, $V_A- = V_D- = -2.25V$, $V_{IN} = 0.707\ V_{PK}$ ($0.5V_{RMS}$) (NOTE 8)									
f_o, Center Frequency Maximum	5	Figure 16 (Mode 1) Q ≤ 50, Q Accuracy ≤ ±25%			20			20	kHz
		Q ≤ 20, Q Accuracy ≤ ±12%			30			30	kHz
f_o, Center Frequency Minimum	5	Figure 16 (Mode 1) Q ≤ 50, Q Accuracy ≤ ±30%	25			25			Hz
		Q ≤ 20, Q Accuracy ≤ ±15%	25			25			Hz
Clock to Center Frequency Ratio		Q = 10, Figure 16 (Mode 1)							
	4	50:1, f_{CLK} = 250kHz	49.85	50.0	50.15	49.60	50.0	50.40	
	5	100:1, f_{CLK} = 500kHz	100.0	100.3	100.6	99.50	100.3	101.1	
Clock Frequency	5	Q ≤ 20, Q Accuracy ≤ ±15%	2.5k		1.5M	2.5k		1.5M	Hz
Q Accuracy	4	f_{CLK} = 250kHz, Q = 10 50:1			±4			±8	%
		Figure 16 (Mode 1) 100:1		±3			±6		%

3

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_A+ = V_D+ = 5V \pm 10\%$, $V_A- = V_D- = -5V \pm 10\%$, $C_L = 25pF$, $V_{IN} = 2.5V_{PK}$ (1.767 V_{RMS}) Clock Duty Cycle 40% to 60%.

PARAMETER	NOTES	CONDITIONS	ML2110B MIN	ML2110B TYP NOTE 3	ML2110B MAX	ML2110C MIN	ML2110C TYP NOTE 3	ML2110C MAX	UNITS
Filter, $V_A+ = V_D+ = 2.25V$, $V_A- = V_D- = -2.25V$, $V_{IN} = 0.707\ V_{PK}$ (0.5 V_{RMS}) (Continued)									
Noise	7	Figure 16 (Mode 1)							
		Q = 1, R1 = R2 = R3 = 2k							
		Bandpass, 5kHz, 50:1		80			80		μV_{RMS}
		5kHz, 100:1		100			100		μV_{RMS}
		Lowpass, 5kHz, 50:1		105			105		μV_{RMS}
		5kHz, 100:1		130			130		μV_{RMS}
		Notch, 5kHz, 50:1		80			80		μV_{RMS}
		5kHz, 100:1		100			100		μV_{RMS}
		Figure 16 (Mode 1)							
		Q = 10, R1 = R3 = 20k, R2 = 2k							
		Bandpass, 5kHz, 50:1		256			256		μV_{RMS}
		5kHz, 100·1		315			315		μV_{RMS}
		Lowpass, 5kHz, 50:1		262			262		μV_{RMS}
		(R1 = 2k) 5kHz, 100:1		320			320		μV_{RMS}
		Notch, 5kHz, 50:1		33			33		μV_{RMS}
		(R1 = 2k) 5kHz, 100:1		38			38		μV_{RMS}
Operational Amplifiers and Power Supply									
V_{OS} DC Offset	4			2	15		2	15	mV
DC Open Loop Gain		$R_L = 1k$		95			95		dB
Gain Bandwidth Product				2.4			2.4		MHz
Slew Rate				2.0			2.0		V/μs
Output Voltage Swing (Clipping Level)	5	$R_L = 2k$, |V| from V_{A+} or V_{A-}		.5	1.2		.5	1.2	V
Output Short Circuit Current		Source		50			50		mA
		Sink		25			25		mA
Power Supply And Clock									
Supply Current	4	$f_{CLK} = 250kHz$							
$(I_A+) + (I_D+)$				13	22		13	22	mA
$(I_A-) + (I_D-)$				12	21		12	21	mA
I_{LSH}				0.5	1		0.5	1	mA
V_{CLK} Input Threshold	4	Low			0.8			0.8	V
		High	2.0			2.0			V
CLKA, CLKB Pulse Width	5	CLK High or CLK Low	250			250			ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: −55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. 0°C to 70°C and −40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.
Note 3: Typicals are parametric norm at 25°C.
Note 4: Parameter guaranteed and 100% production tested.
Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.
Note 6: Center frequency is defined as the peak of the bandpass output.
Note 7: The noise is measured with the HP8903A audio analyzer with a bandwidth of 30kHz which is 6 times the f_o at 50:1 or at 100:1.
Note 8: For T_A = -55°C to +125°C; $V_A+ = V_D+ = 2.375V$, $V_A- = V_D- = -2.375V$

TYPICAL PERFORMANCE CURVES

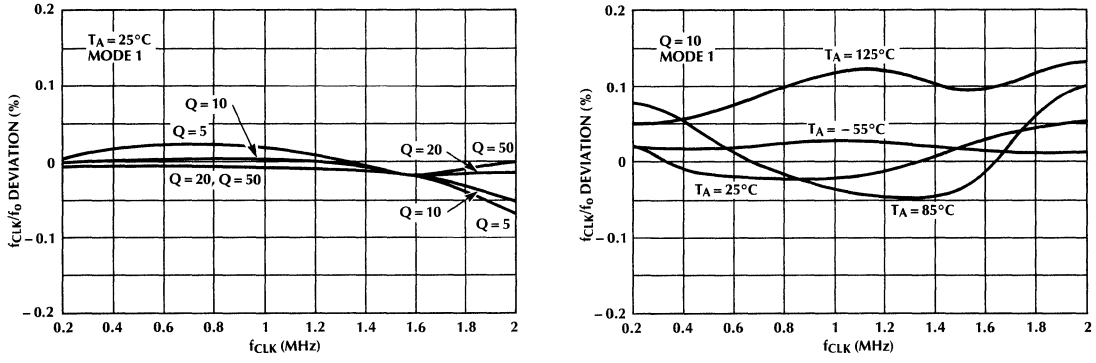


Figure 1. f_{CLK}/f_o vs. f_{CLK} (100:1, 50:1 at $V_S = \pm 2.5V$ or $V_S = \pm 5V$)

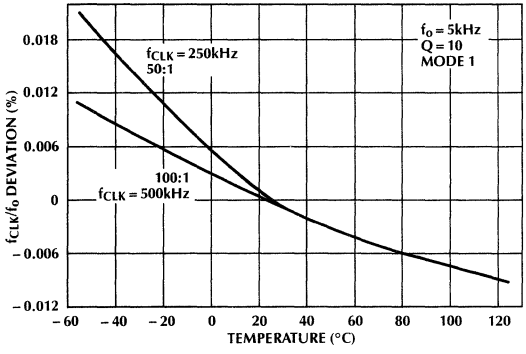


Figure 2A. f_{CLK}/f_o Deviation vs. Temperature ($V_S = \pm 5V$)

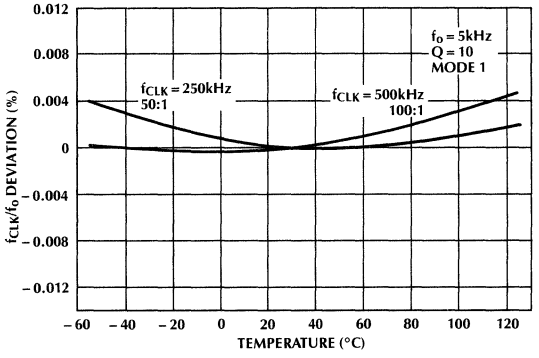
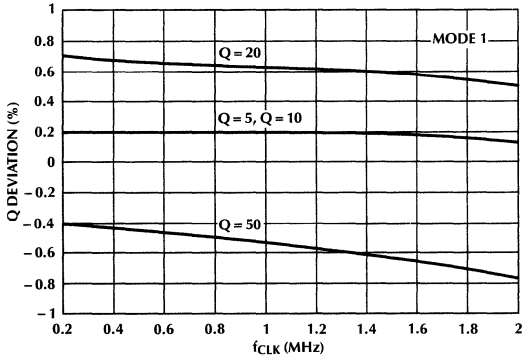


Figure 2B. f_{CLK}/f_o Deviation vs. Temperature ($V_S = \pm 2.5V$)



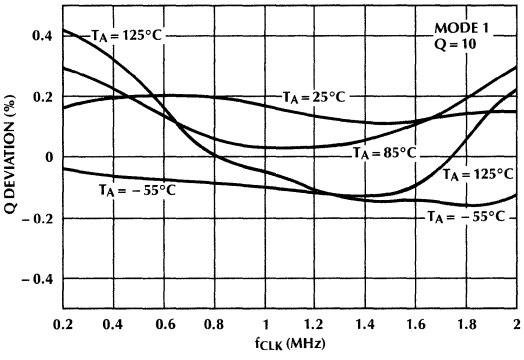


Figure 3. Q Error vs. f_{CLK} (100:1, 50:1 at $V_S = \pm 2.5V$ or $V_S = \pm 5V$)

TYPICAL PERFORMANCE CURVES (Continued)

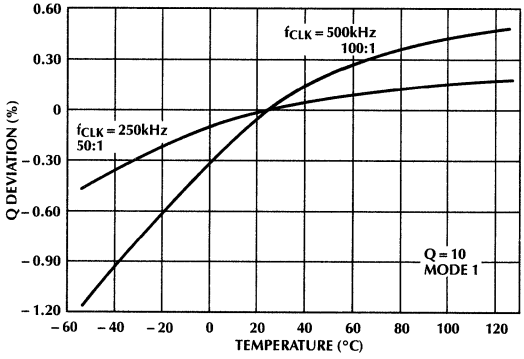


Figure 4A. Q Deviation vs. Temperature ($V_S = \pm 5V$)

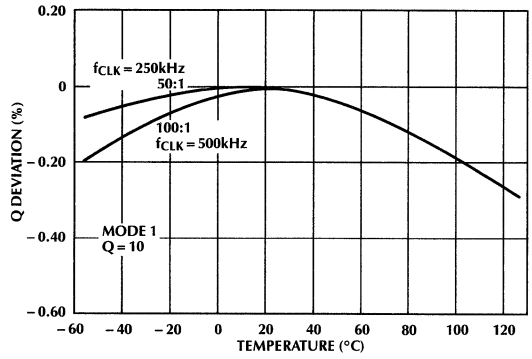


Figure 4B. Q Deviation vs. Temperature ($V_S = \pm 2.5V$)

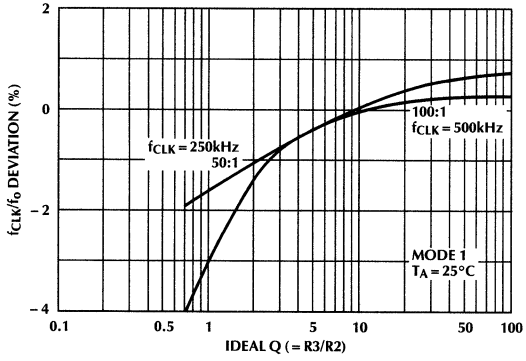


Figure 5A. f_{CLK}/f_o Deviation vs. Q ($V_S = \pm 5V$)

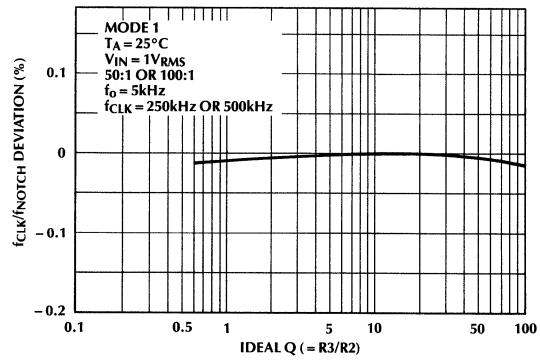


Figure 5B. f_{CLK}/f_{NOTCH} Deviation vs. Q ($V_S = \pm 5V$)

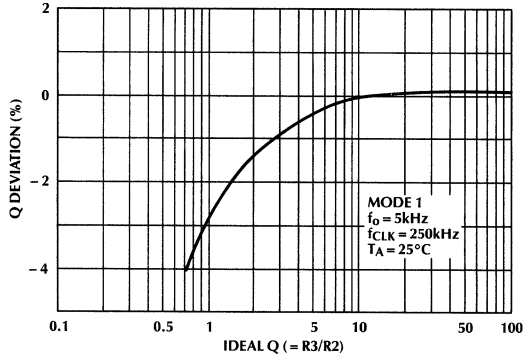


Figure 6A. Q Deviation vs. Q (50:1, $V_S = \pm 5V$)

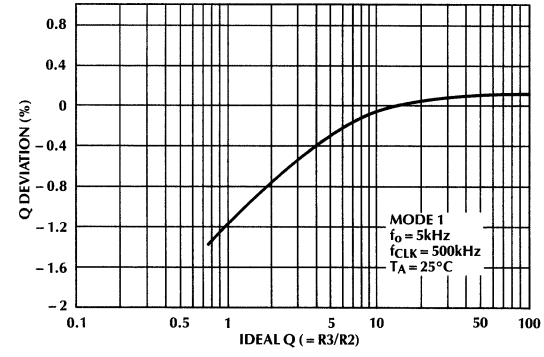


Figure 6B. Q Deviation vs. Q (100:1, $V_S = \pm 5V$)

TYPICAL PERFORMANCE CURVES (Continued)

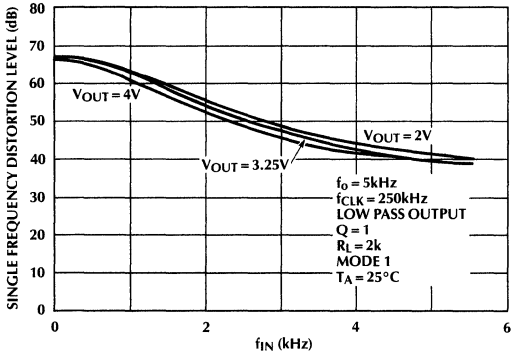


Figure 7A. Distortion vs. f_{IN} (50:1, $V_S = \pm 5V$)

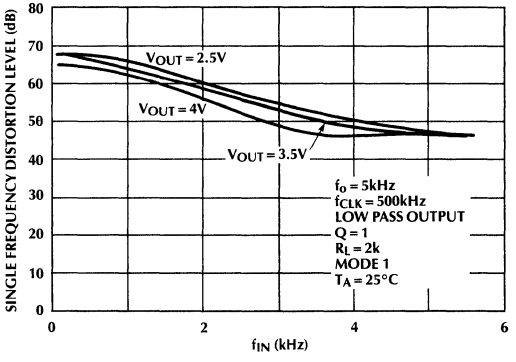


Figure 7B. Distortion vs. f_{IN} (100:1, $V_S = \pm 5V$)

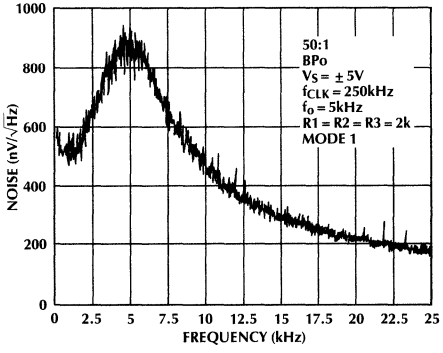


Figure 8A. Noise Spectrum Density (Q = 1)

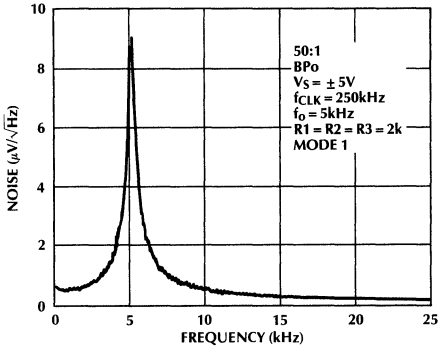


Figure 8B. Noise Spectrum Density (Q = 10)

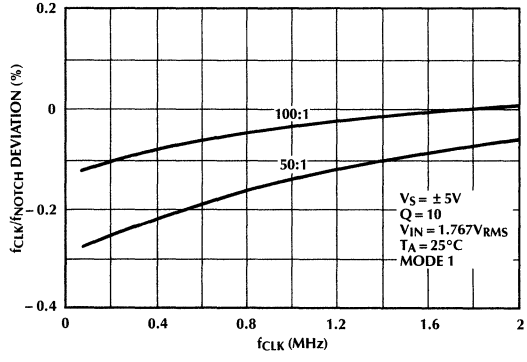


Figure 9. f_{CLK}/f_{NOTCH} vs. f_{CLK}

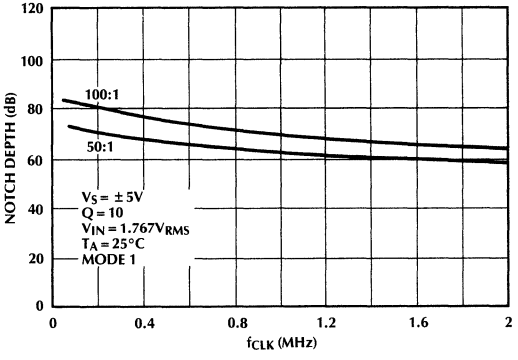


Figure 10. Notch Depth vs f_{CLK}

TYPICAL PERFORMANCE CURVES (Continued)

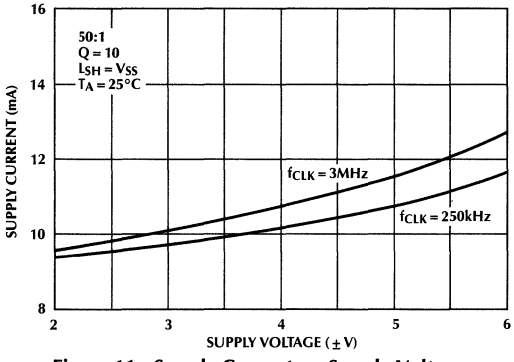


Figure 11. Supply Current vs. Supply Voltage

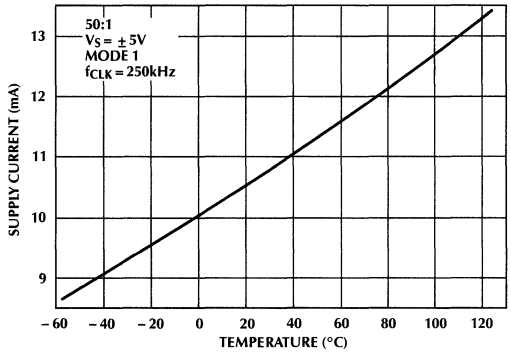


Figure 12. Supply Current vs. Temperature

FUNCTIONAL DESCRIPTION

POWER SUPPLIES

The analog (V_A+) and digital (V_D+) supply voltage pins, in most cases, are tied together and bypassed to AGND with a 0.1μF and a 0.01μF disc ceramic capacitor. If high digital noise exists, the supply pins can be bypassed separately. The ML2110 positive analog and positive digital supply pins are internally connected by the IC substrate and should be biased from the same DC source.

The ML2110 operates with a single supply from 5V ± 10% and with split supplies from ±4.5V to ±6V supplies.

CLOCK INPUT PINS AND LEVEL SHIFT

With dual supplies equal to or higher than ±4.0V, the level shift (LSh) pin 9 can be connected to the same potential as the AGND or V_A- pin. With single supply operation, the negative supply pins and the LSh pin should be tied to the system ground. The AGND, pin 15, should be biased at 1/2 supplies. Under these conditions, the clock levels are TTL or CMOS. The input clock pins (10, 11) share the same level shift pin.

50/100/HOLD (Pin 12)

By tying pin 12 to (V_A+, V_D+) the filter operates in the 50:1 mode. By tying pin 12 to 1/2 of the voltage supplies (AGND potential), the ML2110 operates in the 100:1 mode. The range of pin 12 with total supply voltage of +5V is 2.5 ± 0.5V; +10V is 5V ± 0.5V. When pin 12 is tied to the negative supply pin, the filter operation is stopped and the bandpass and lowpass outputs act as an S/H circuit holding the last sample.

$S1_A$, $S1_B$, (Pins 5 and 16)

These are voltage signal input pins and should be driven with a source impedance below 5k. The $S1_A$, $S1_B$ pins can be used to alter the clock to center frequency ratio (f_{CLK}/f_o) of the filter (see modes 1b, 1c, 2a, 2b) or to feedforward the input signal for allpass filter configurations (see modes 4 and 5). When these pins are not used, they should be tied to the AGND pin.

$S_{A/B}$ (Pin 6)

When $S_{A/B}$ is high, the S2 negative input of the voltage summer is tied to the lowpass output. When the $S_{A/B}$ pin is connected to the negative supply, the S2 input switches to ground.

AGND (Pin 15)

AGND is connected to the system ground for dual supply operation. When operating with a single positive supply, the analog ground pin should be tied to 1/2 of the supply and bypassed with a 0.1μF capacitor. The positive inputs of the internal op amps and the reference point of the internal switches are connected to the AGND pin.

f_{CLK}/f_o RATIO

The ML2110 is a sampled data filter and approximates continuous time filters. The filter deviates from its ideal continuous filter model when the (f_{CLK}/f_o) ratio decreases and when the Qs are low.

$f_o \times Q$ PRODUCT RATIO

The $f_o \times Q$ product of the ML2110 depends on the clock frequency and the mode of operation. For clock frequencies below 1MHz, in mode 1 and its derivatives, the $f_o \times Q$ product is mainly limited by the desired f_o and Q accuracy. For the same clock frequency and for the same Q value the $f_o \times Q$ product can be further increased if the clock to center frequency ratio is lowered below 50:1.

Mode 3, Figure 24, and the modes of operation where R4 is finite, are "slower" than the basic mode 1. The resistor R4 places the input op amp inside the resonant loop. The finite GBW of this op amp creates an additional phase shift and enhances the Q value at high clock frequencies.

OUTPUT NOISE

The wideband RMS noise of the ML2110 outputs is nearly independent from the clock frequency provided that the clock itself does not become part of the noise. The noise at the BP and LP outputs increases for high Qs.

FILTER FUNCTION DEFINITIONS

Each filter of the ML2110 with an external clock and resistors approximates 2nd order filter functions. These are tabulated below in the frequency domain.

1. **Bandpass function:** available at the bandpass output pins (2, 19), Figure 13.

$$G(s) = H_{OBP}\frac{s\omega_o/Q}{s^2 + (s\omega_o/Q) + \omega_o^2}$$

H_{OBP} = Gain at $\omega = \omega_o$

$f_o = \omega_o/2\pi$; f_o is the center frequency of the complex pole pair. f_o is measured as the peak frequency of the bandpass output.

Q = Quality factor of the complex pole pair. It is the ratio of f_o to the −3dB bandwidth of the 2nd order bandpass function. The Q is always measured at the filter BP output.

2. **Lowpass function:** available at the LP output pins (1, 20), Figure 14.

$$G(s) = H_{OLP}\frac{\omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OLP} = DC gain of the LP output.

3. **Highpass function:** available only in mode 3 at the output pins (3, 18), Figure 15.

$$G(s) = H_{OHP}\frac{s^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OHP} = gain of the HP output for $f \rightarrow \frac{f_{CLK}}{2}$

4. **Notch function:** available at pins 3 (18) for several modes of operation.

$$G(s) = (H_{ON2})\frac{(s^2 + \omega^2{}_n)}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{ON2} = gain of the notch output for $f \rightarrow \frac{f_{CLK}}{2}$

H_{ON1} = gain of the notch output for $f \rightarrow 0$

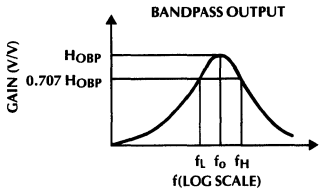
$f_n = \omega_n/2\pi$; f_n is the frequency of the notch occurrence.

5. **Allpass function:** available at pins 3(18) for mode 4, 4a.

$$G(s) = H_{OAP}\frac{[s^2 - s(\omega_o/Q) + \omega_o^2]}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OAP} = gain of the allpass output for $0 < f < \frac{f_{CLK}}{2}$

For allpass functions, the center frequency and the Q of the numerator complex zero pair is the same as the denominator. Under these conditions, the magnitude response is a straight line. In mode 5, the center frequency f_Z, of the numerator complex zero pair, is different than f_o. For high numerator Q's, the magnitude response will have a notch at f_Z.

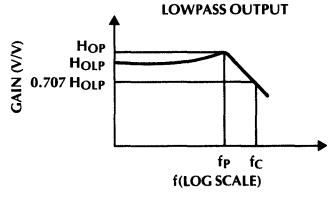


$$Q = \frac{f_o}{f_H - f_L};\ f_o = \sqrt{f_L f_H}$$

$$f_L = f_o\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_o\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

Figure 13

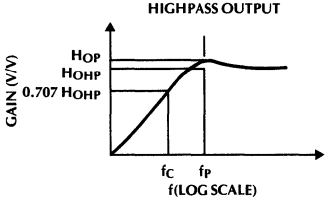


$$f_C = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_P = f_o\sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 14



$$f_C = f_o \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_P = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 15

OPERATION MODES

Table 1. 1st Order Functions

MODE	PIN 2 (19)	PIN 3 (18)	f_C	f_Z
6a	LP	HP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	
6b	LP	LP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	
7	LP	AP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$

Table 2. 2nd Order Functions

MODE	PIN 1 (20)	PIN 2 (19)	PIN 3 (18)	f_o	f_N
1	LP	BP	Notch	$\frac{f_{CLK}}{100(50)}$	f_o
1a	LP	BP	BP	$\frac{f_{CLK}}{100(50)}$	
1b	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5+R6}}$
1c	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$
1d	LP	BP		$\frac{f_{CLK}}{100(50)}$	
2	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)}$
2a	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4} + \frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5+R6}}$
2b	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4} + \frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$
3	LP	BP	HP	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	
3a	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R_h}{R_l}}$
4	LP	BP	AP	$\frac{f_{CLK}}{100(50)}$	
4a	LP	BP	AP	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	
5	LP	BP	C.Z	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 - \frac{R1}{R4}}$

OPERATION MODES (Continued)

There are basically three modes of operation: mode 1, mode 2, mode 3. In the mode 1, Figure 16, the input amplifier is outside the resonant loop. Because of this, mode 1 and its derivatives (mode 1a, 1b, 1c, 1d) are faster than modes 2 and 3.

Mode 1a, Figure 17, represents the most simple hook-up of the ML2110. Mode 1a is useful when voltage gain at the bandpass output is required. The bandpass voltage gain, however, is equal to the value of Q, and a second order, clock tunable, BP resonator can be achieved with only 2 resistors. The filter center frequency directly depends on the external clock frequency. For high order filters, mode 1a is not practical as it requires several clock frequencies to tune the overall filter response.

Mode 1, Figure 16, provides a clock tunable notch. Mode 1 is a practical configuration for second order clock tunable bandpass/notch filters. In mode 1, a bandpass output with a very high Q, together with unity gain, can be obtained with the dynamics of the remaining notch and lowpass outputs.

Modes 1b and 1c, Figures 18, 19 are similar. They both produce a notch with a frequency which is always equal to the filter center frequency. The notch and the center frequency can be adjusted with an external resistor ratio.

The clock to center frequency ratio range is:

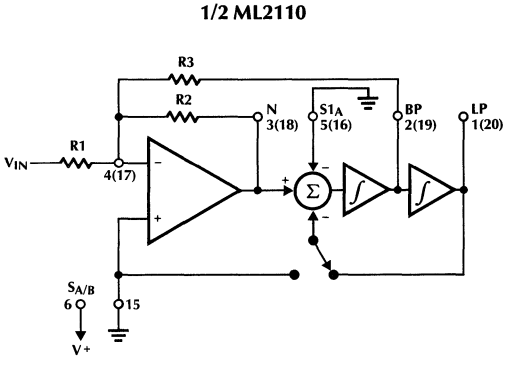
$$\frac{500}{1} \geq \frac{f_{CLK}}{f_o} \geq \frac{100}{1} \text{ or } \frac{50}{1}; \text{ mode 1b}$$

$$\frac{100}{1} \text{ or } \frac{50}{1} \geq \frac{f_{CLK}}{f_o} \geq \frac{100}{\sqrt{2}} \text{ or } \frac{50}{\sqrt{2}}; \text{ mode 1c}$$

The input impedance of the S1 pin is clock dependent, and in general R5 should not be larger than 5k. Mode 1b can be used to increase the clock to center frequency ratio beyond 100:1. For this mode, the limit for the (f_{CLK}/f_o) ratio is 500:1. Beyond this, the filter will exhibit large output offsets. Mode 1d, Figure 20, is the fastest mode of operation: In the 50:1 mode center frequencies beyond 20kHz can easily be achieved.

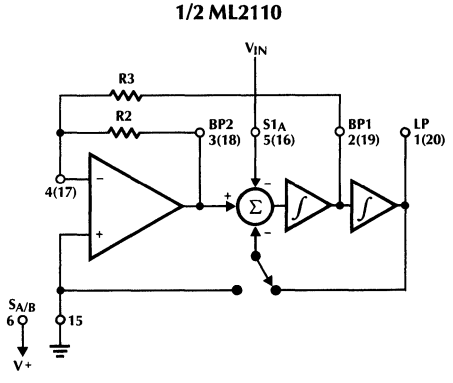
Modes 2, 2a, and 2b have a notch output which frequency, f_n, can be tuned independently from the center frequency, f_o. For all cases, however, $f_n < f_o$. These modes are useful when cascading second order functions to create an overall elliptic highpass, bandpass or notch response. The input amplifier and its feedback resistors (R2/R4) are now part of the resonant loop. Because of this, mode 2 and its derivatives are slower than mode 1's.

3



$f_o = \frac{f_{CLK}}{100(50)}$; $f_n = f_o$; $H_{OLP} = -\frac{R2}{R1}$; $H_{OBP} = -\frac{R3}{R1}$; $H_{ON1} = -\frac{R2}{R1}$; $Q = \frac{R3}{R2}$

Figure 16. Mode 1: 2nd Order Filter Providing Notch, Bandpass, Lowpass

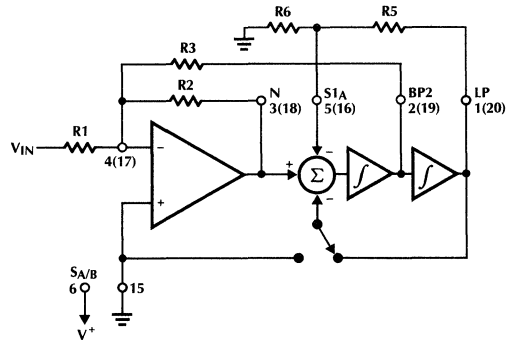


$f_o = \frac{f_{CLK}}{100(50)}$; $Q = \frac{R3}{R2}$; $H_{OBP1} = -\frac{R3}{R2}$; $H_{OBP2} = 1$(NONINVERTING); $H_{OLP} = -1$

Figure 17. Mode 1a: 2nd Order Filter Providing Bandpass, Lowpass

OPERATION MODES (Continued)

1/2 ML2110

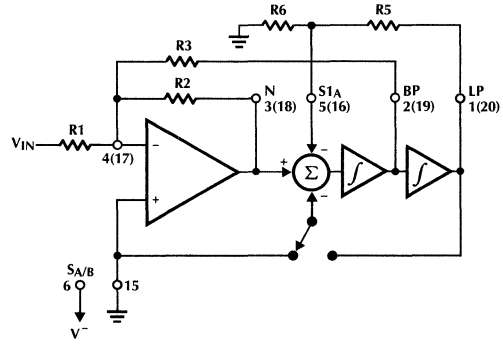


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R6}{R5+R6}};\ f_n = f_o;\ Q = \frac{R3}{R2}\sqrt{1+\frac{R6}{R5+R6}};$$

$$H_{ON1}(f\rightarrow 0) = H_{ON2}\left(f-\frac{f_{CLK}}{2}\right) = -\frac{R2}{R1};\ H_{OBP} = -\frac{R3}{R1};\ H_{OLP} = \frac{-R2/R1}{1+R6/(R5+R6)};\ R5 < 5k\Omega$$

Figure 18. Mode 1b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2110

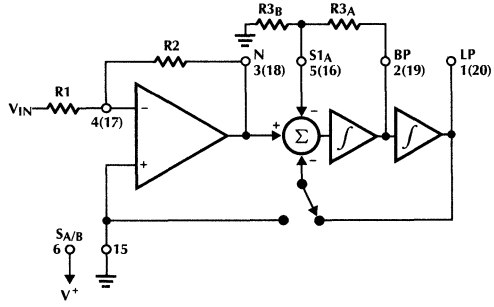


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R6}{R5+R6}};\ f_n = f_o;\ Q = \frac{R3}{R2}\sqrt{\frac{R6}{R5+R6}};$$

$$H_{ON1}(f\rightarrow 0) = H_{ON2}\left(f-\frac{f_{CLK}}{2}\right) = -\frac{R2}{R1};\ H_{OLP} = \frac{-R2/R1}{R6/(R5+R6)};\ H_{OBP} = -\frac{R3}{R1};\ R5 < 5k\Omega$$

Figure 19. Mode 1c: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2110



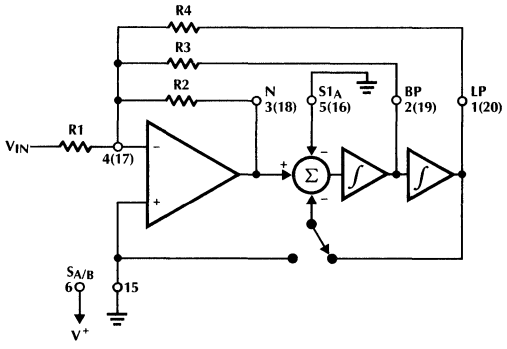
$$f_o = \frac{f_{CLK}}{100(50)};\ Q = 1+\frac{R3_A}{R3_B};\ H_{OBP} = -\frac{R2}{R1}\times Q$$

$$H_{OLP} = -\frac{R2}{R1};\ V_N = -\frac{R2}{R1}V_{IN}$$

Figure 20. Mode 1d: 2nd Order Filter Providing Bandpass and Lowpass for Qs Greater Than or Equal to 1.

OPERATION MODES (Continued)

1/2 ML2110

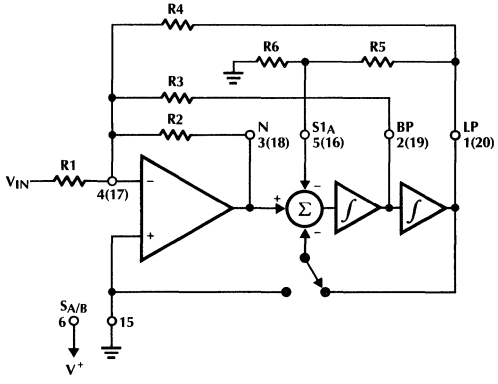


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}};\ f_n = \frac{f_{CLK}}{100(50)};\ Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}};\ H_{OLP} = \frac{-R2/R1}{1+(R2/R4)}$$

$$H_{OBP} = -R3/R1;\ H_{ON1(f\to 0)} = \frac{-R2/R1}{1+(R2/R4)};\ H_{ON2}\left(f\to\frac{f_{CLK}}{2}\right) = -R2/R1$$

Figure 21. Mode 2: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2110



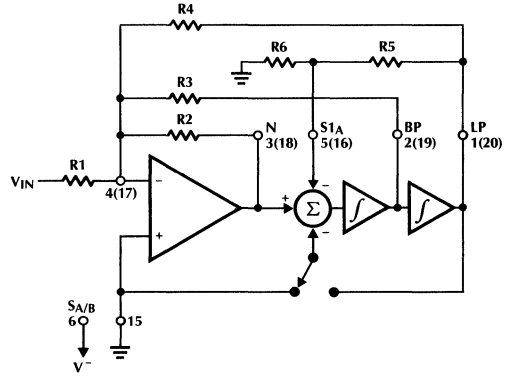
$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}+\frac{R6}{R5+R6}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R6}{R5+R6}};\ Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}+\frac{R6}{R5+R6}}$$

$$H_{ON1(f\to 0)} = -\frac{R2}{R1}\left|\frac{1+R6/(R5+R6)}{1+(R2/R4)+[R6/(R5+R6)]}\right|;\ H_{ON2}\left(f\to\frac{f_{CLK}}{2}\right) = -R2/R1$$

$$H_{OBP} = -R3/R1;\ H_{OLP} = \frac{-R2/R1}{1+(R2/R4)+[R6/(R5+R6)]}$$

Figure 22. Mode 2a: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2110



$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}+\frac{R6}{R5+R6}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R6}{R5+R6}};\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}+\frac{R6}{R5+R6}}$$

$$H_{ON1(f\to 0)} = -\frac{R2}{R1}\left|\frac{R6/(R5+R6)}{(R2/R4)+[R6/(R5+R6)]}\right|;\ H_{ON2}\left(f\to\frac{f_{CLK}}{2}\right) = -R2/R1$$

$$H_{OBP} = -R3/R1;\ H_{OLP} = \frac{-R2/R1}{(R2/R4)+[R6/(R5+R6)]}$$

Figure 23. Mode 2b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

OPERATION MODES (Continued)

In mode 3, Figure 24, a single resistor ratio (R2/R4) can tune the center frequency below or above the $f_{CLK}/100$ (or $f_{CLK}/50$) ratio. Mode 3 is a state variable configuration since it provides a highpass, bandpass, lowpass output through progressive integration; notches are obtained by summing the highpass and lowpass outputs (mode 3a, Figure 25). The notch frequency can be tuned below or above the center frequency through the resistor ratio (R_h/R_l). Because of this, modes 3 and 3a are the most versatile and useful modes for cascading second order sections to obtain high order elliptic filters. Figure 33, shows the 2 sections connected in mode 3a to obtain a clock tunable 4th order sharp elliptic bandpass filter. The first notch is created by summing directly the HP and LP outputs of the first section into the inverting input of the second section op amp. The individual Q's are 29.6 and the filter maintains its shape and performance up to 20kHz center frequency, as shown in Figure 34. For this circuit an external op amp is required to obtain the 2nd notch. The dynamics of Figure 34 show that the amplitude response at each output pin does not exceed 0dB. The gain in the passband depends on the ratio of $(R_g/R_{h2}) \times (R22/R_{h1}) \times (R21/R11)$. Any gain value can be obtained by acting on the (R_g/R_{h2}) ratio of the external op amp, the remaining ratios are adjusted for optimum dynamics of the output nodes. The external op amp of Figure 33 is not always required. In Figure 35, one section in mode 3a is cascaded with the other section in mode 2b to obtain a 4th order, 1dB ripple, elliptic bandreject filter. The clock to center frequency ratio is adjusted to 200:1; this is done in order to better approximate a linear R,C notch filter. The amplitude response of the filter is shown in Figure 36 with up to 1MHz clock frequency. The 0dB bandwidth to the stop bandwidth ratio is 8/1. When the filter is centered at 1kHz, it should theoretically have a 44dB rejection with a 50Hz stop bandwidth. For a more narrow filter than the above, the unused BP output of the mode 2b section, Figure 35, has a gain exceeding unity which limits the dynamic range of the overall filter. For very selective bandpass/bandreject filters, the mode 3a approach as in Figure 25, yields better dynamic range since the external op amp helps to optimize the dynamics of the output nodes of the ML2110.

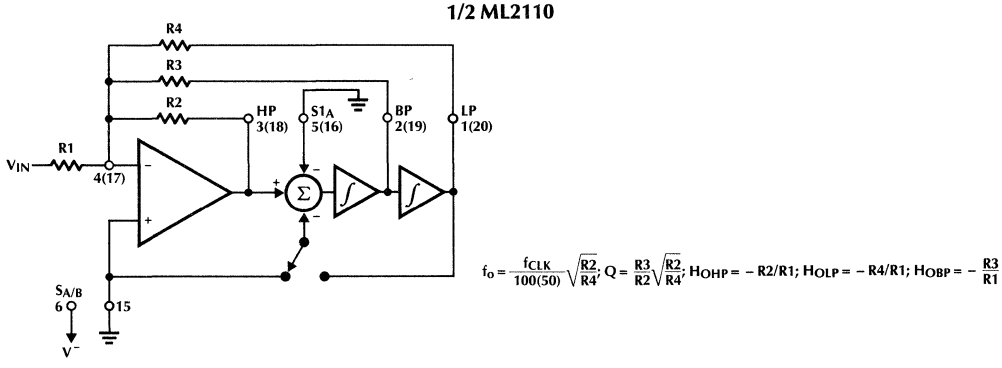


Figure 24. Mode 3: 2nd Order Filter Providing Highpass, Bandpass, Lowpass

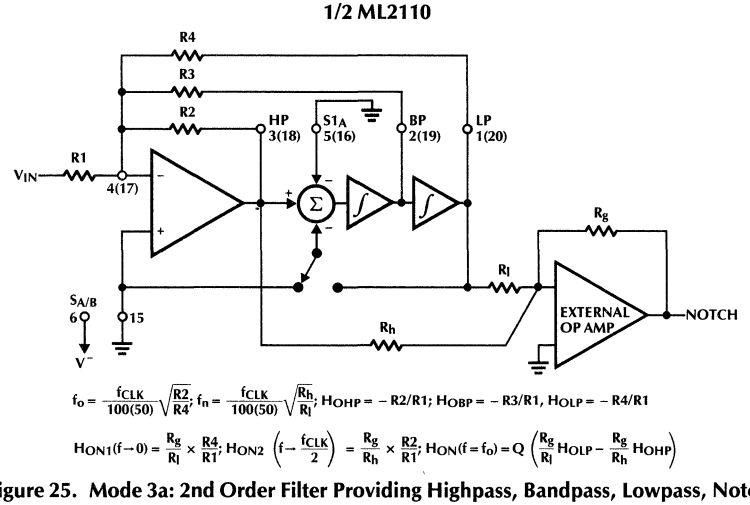
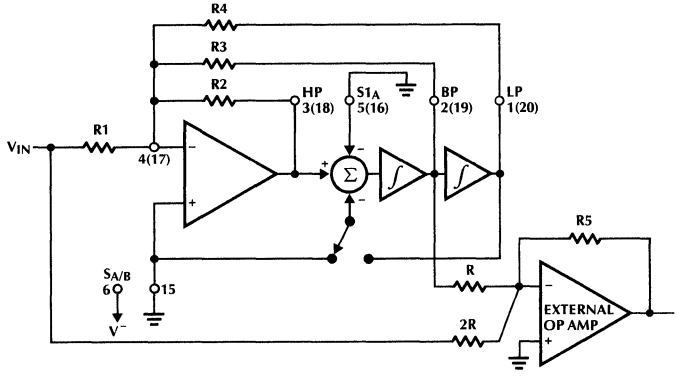


Figure 25. Mode 3a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Notch

OPERATION MODES (Continued)

1/2 ML2110

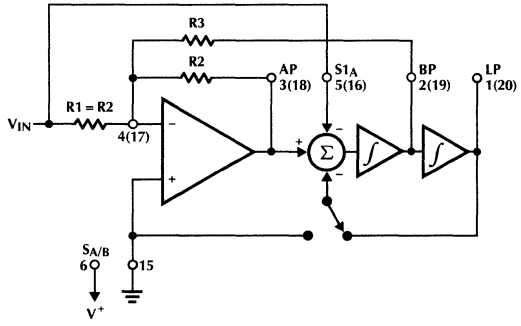


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}};\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}};\ H_{OAP} = \frac{R5}{2R};\ H_{OHP} = -\frac{R2}{R1};\ H_{OBP} = -\frac{R3}{R1};\ H_{OLP} = -\frac{R4}{R1}$$

Figure 26. Mode 4a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Allpass

3

1/2 ML2110

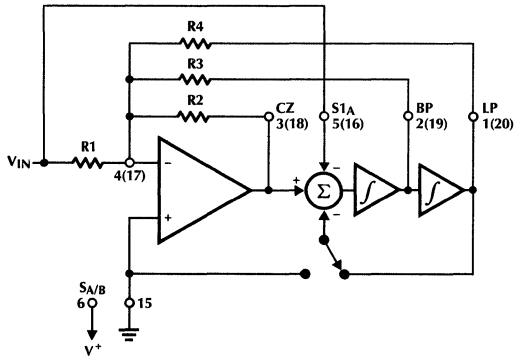


$$f_o = \frac{f_{CLK}}{100(50)};\ Q = \frac{R3}{R2};\ H_{OAP} = -\frac{R2}{R1};\ H_{OLP} = -2;\ H_{OBP} = -2\left(\frac{R3}{R2}\right)$$

Figure 27. Mode 4: 2nd Order Filter Providing Allpass, Bandpass, Lowpass

OPERATION MODES (Continued)

1/2 ML2110



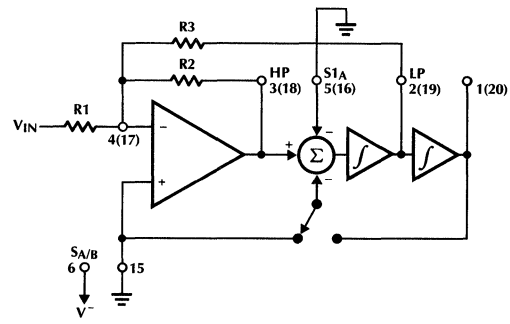
$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}};\ f_z = \frac{f_{CLK}}{100(50)}\sqrt{1-\frac{R1}{R4}};\ Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}}$$

$$Q_Z = \frac{R3}{R1}\sqrt{1-\frac{R1}{R4}};\ H_{OZ(f\to 0)} = \frac{(R4/R1)-1}{(R4/R2)+1};\ H_{OZ}\left(f=\frac{f_{CLK}}{2}\right) = \frac{R2}{R1};$$

$$H_{OBP} = \frac{R3}{R2}\left(1+\frac{R2}{R1}\right);\ H_{OLP} = \frac{1+(R2/R1)}{1+(R2/R4)}$$

Figure 28. Mode 5: 2nd Order Filter Providing Numerator Complex Zeros, Bandpass, Lowpass

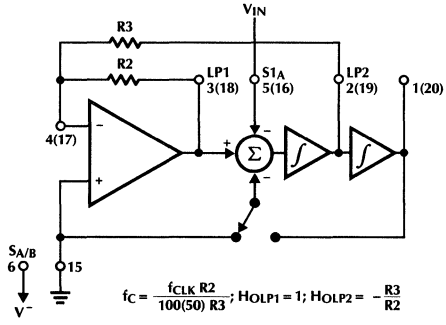
1/2 ML2110



$$f_C = \frac{f_{CLK}\,R2}{100(50)\,R3};\ H_{OLP} = -R3/R1;\ H_{OHP} = -R2/R1$$

Figure 29. Mode 6a: 1st Order Filter Providing Highpass, Lowpass

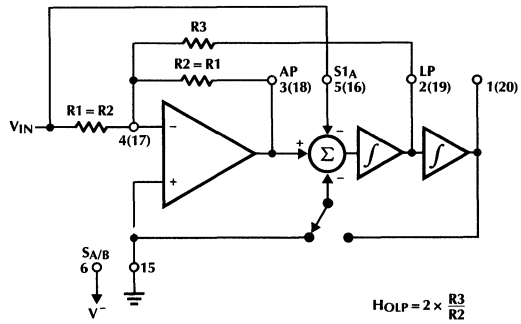
1/2 ML2110



$$f_C = \frac{f_{CLK}\,R2}{100(50)\,R3};\ H_{OLP1} = 1;\ H_{OLP2} = -\frac{R3}{R2}$$

Figure 30. Mode 6b: 1st Order Filter Providing Lowpass

1/2 ML2110

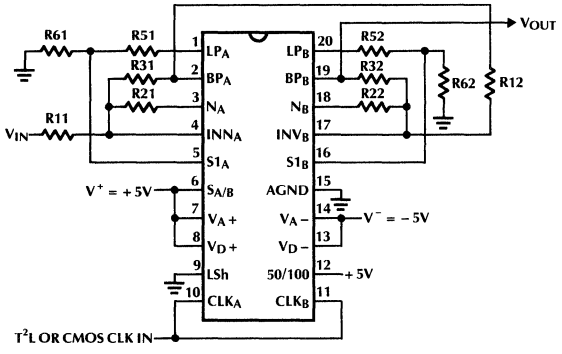


$$H_{OLP} = 2 \times \frac{R3}{R2}$$

$$f_p = \frac{f_{CLK}\,R2}{100(50)\,R3};\ f_z = \frac{f_{CLK}\,R2}{100(50)\,R3};\ \text{GAIN AT OUTPUT} = 1\ \text{FOR}\ 0 \le f \le \frac{f_{CLK}}{2}$$

Figure 31. Mode 7: 1st Order Filter Providing Allpass, Lowpass

OPERATION MODES (Continued)



PRECISE RESISTOR VALUES

R11 = 149.55k	R12 = 44.1k
R21 = 4.988k	R22 = 4.999k
R31 = 149.73k	R32 = 143.5k
R51 = 2.538k	R52 = 2.498k
R61 = 2.495k	R62 = 4.331k

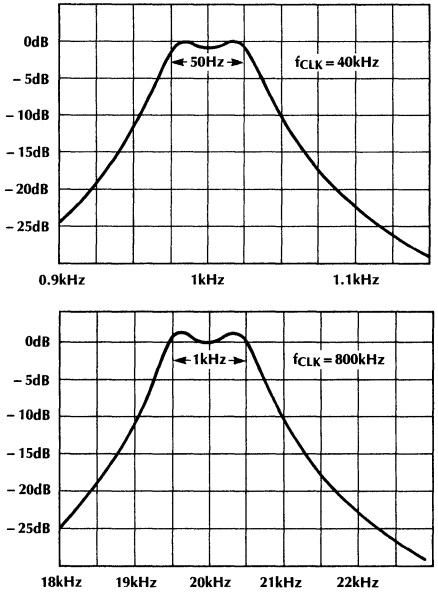
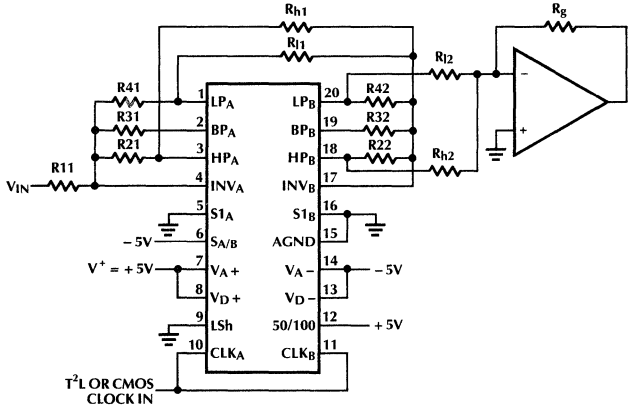


Figure 32. Cascading the 2 sections connected in mode 1b to obtain a clock tunable 4th order 1dB ripple bandpass Chebyshev filter with (center frequency)/(Ripple Bw) = 20/1.



RESISTOR VALUES

R11 = 155.93k	R21 = 5k	R31 = 152k	R41 = 5.27k
R_{h1} = 13.2k	R_{I1} = 10.74k	R22 = 5.26k	R32 = 151.8k
R42 = 5k	R_{I2} = 6.11k	R_{h2} = 5k	R_g = 37.3k

NOTE: FOR CLOCK FREQUENCIES ABOVE 700kHz A 12pF CAPACITOR ACROSS R41 AND A 20pF CAPACITOR ACROSS R42 WERE USED TO PREVENT THE PASSBAND RIPPLE FROM ANY ADDITIONAL PEAKING.

Figure 33. Combining mode 3 with mode 3a to make the 4th order BP filter of Figure 34 with improved dynamics. The gain at each node is ≤0dB for all input frequencies.

OPERATION MODES (Continued)

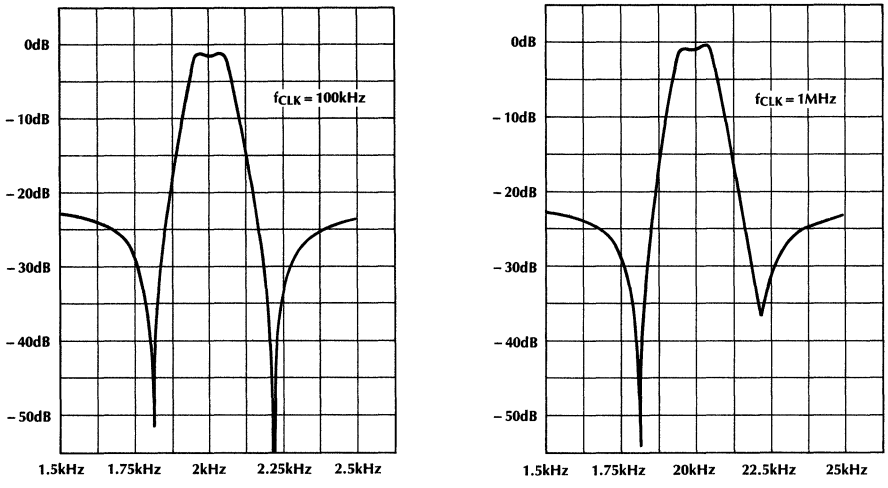


Figure 34. The BP filter of Figure 33, when swept from a 2kHz to 20kHz center frequency.

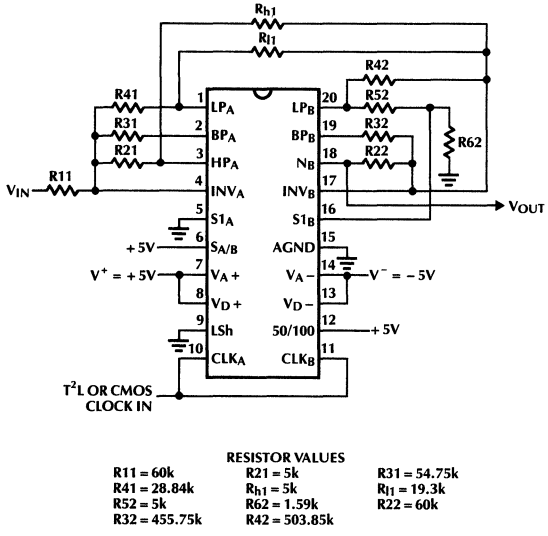


Figure 35. Combining mode 3 with mode 2b to create a 4th order BP elliptic filter with 1dB ripple and a ratio of 0db to stop bandwidth equal to 8/1.

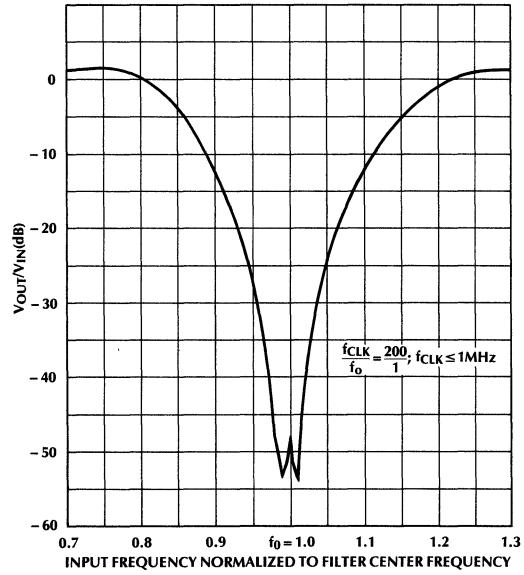


Figure 36. Amplitude Response of the Notch Filter of Figure 35.

OFFSETS

Switched capacitor integrators generally exhibit higher input offsets than discrete R,C integrators.

These offsets are mainly the charge injection of the CMOS switches into the integrating capacitors. The internal op amp offsets also add to the overall offset budget.

Figure 37 shows half of the ML2110 filter with its equivalent input offsets V_{OS1}, V_{OS2}, V_{OS3}.

The DC offset at the filter bandpass output is always equal to V_{OS3}. The DC offsets at the remaining two outputs (Notch and LP) depend on the mode of operation and external resistor ratios. Table 3 illustrates this.

It is important to know the value of the DC output offsets, especially when the filter handles input signals with large dynamic range. As a rule of thumb, the output DC offsets increase when:

1. The Q's decrease
2. The ratio (f_{CLK}/f_o) increases beyond 100:1. This is done by decreasing either the (R2/R4) or the R6/(R5 + R6) resistor ratios.

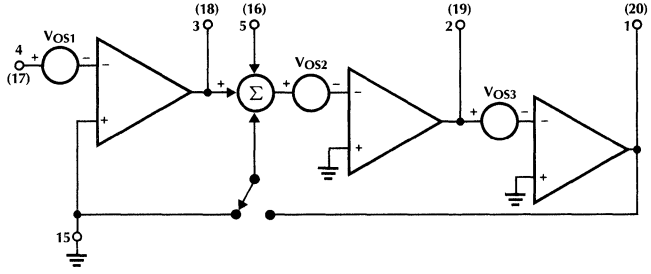


Figure 37. Equivalent Input Offsets of 1/2 ML2110 Filter

Table 3

MODE	V_{OSN} PIN 3 (18)	V_{OSBP} PIN 2 (19)	V_{OSLP} PIN 1 (20)
1,4	$V_{OS1}[(1/Q)+1+\lVert H_{OLP}\rVert]-V_{OS3}/Q$	V_{OS3}	$V_{OSN}-V_{OS2}$
1a	$V_{OS1}[1+(1/Q)]-V_{OS3}/Q$	V_{OS3}	$V_{OSN}-V_{OS2}$
1b	$V_{OS1}[(1/Q)+1+R2/R1]-V_{OS3}/Q$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})(1+R5/R6)$
1c	$V_{OS1}[(1/Q)+1+R2/R1]-V_{OS3}/Q$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})\frac{(R5+R6)}{(R5+2R6)}$
1d	$V_{OS1}[1+R2/R1]$	V_{OS3}	$V_{OSN}-V_{OS2}-V_{OS3}/Q$
2, 5	$[V_{OS1}(1+R2/R1+R2/R3+R2/R4)-V_{OS3}(R2/R3)]\times[R4/(R2+R4)]+V_{OS2}[R2/(R2+R4)]$	V_{OS3}	$V_{OSN}-V_{OS2}$
2a	$[V_{OS1}(1+R2/R1+R2/R3+R2/R4)-V_{OS3}(R2/R3)]\times\left[\frac{R4(1+k)}{R2+R4(1+k)}\right]+V_{OS2}\left[\frac{R2}{R2+R4(1+k)}\right];k=\frac{R6}{R5+R6}$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})\frac{(R5+R6)}{(R5+2R6)}$
2b	$[V_{OS1}(1+R2/R1+R2/R3+R2/R4)-V_{OS3}(R2/R3)]\times\left[\frac{R4k}{R2+R4k}\right]+V_{OS2}\left[\frac{R2}{R2+R4k}\right];k=\frac{R6}{R5+R6}$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})(1+R5/R6)$
3, 4a	V_{OS2}	V_{OS3}	$V_{OS1}\left[1+\frac{R4}{R1}+\frac{R4}{R2}+\frac{R4}{R3}\right]-V_{OS2}\left(\frac{R4}{R2}\right)-V_{OS3}\left(\frac{R4}{R3}\right)$

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML2110BCP	0°C to +70°C	MOLDED DIP (P20)
ML2110CCP	0°C to +70°C	MOLDED DIP (P20)
ML2110BCS	0°C to +70°C	MOLDED SOIC (S20W)
ML2110CCS	0°C to +70°C	MOLDED SOIC (S20W)
ML2110BIJ	–40°C to +85°C	HERMETIC DIP (J20)
ML2110CIJ	–40°C to +85°C	HERMETIC DIP (J20)

PART NUMBER	TEMP. RANGE	PACKAGE
ML2110BMJ	–55°C to +125°C	HERMETIC DIP (J20)
ML2110CMJ	–55°C to +125°C	HERMETIC DIP (J20)
ML2110BIP	–40°C to +85°C	MOLDED DIP (P20)
ML2110CIP	–40°C to +85°C	MOLDED DIP (P20)
ML2110BIS	–40°C to +85°C	MOLDED SOIC (S20W)
ML2110CIS	–40°C to +85°C	MOLDED SOIC (S20W)

Micro Linear

ML2111

Universal Hi-Frequency Dual Filter

GENERAL DESCRIPTION

The ML2111 consists of two independent switched capacitor filters that operate up to 150kHz. These filters perform second order functions, such as lowpass, bandpass, highpass, notch and allpass. All filter configurations, including Butterworth, Bessel, Cauer and Chebyshev can be formed.

The center frequency of these filters are tuned by an external clock or the external clock and a resistor ratio.

The ML2111 frequency range up to 150kHz is specified with ±5.0V±10% power supplies. Using a single 5.0V±10% power supply the frequency range is up to 100kHz.

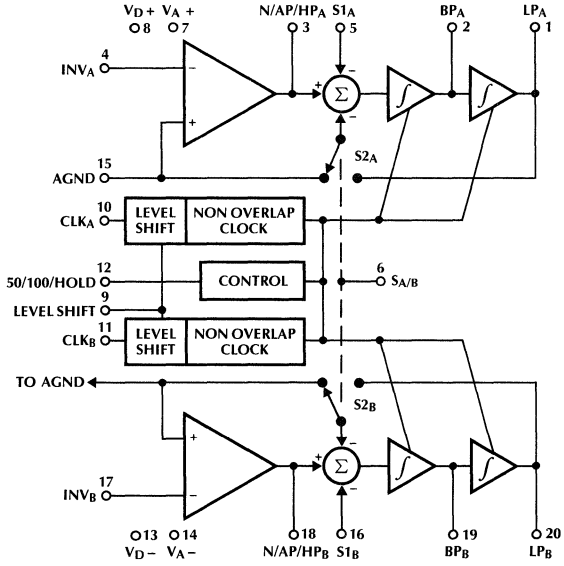
These filters are ideal where center frequency accuracy and high Qs are needed.

The ML2111 is a pin compatible superior replacement for MF10, LMF100, and LTC1060 filters.

FEATURES

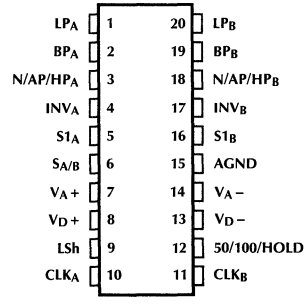
- Guaranteed frequency range to 150kHz
- Center frequency × Q product ⩽5MHz
- Separate highpass, notch, allpass, bandpass, and lowpass outputs
- Center frequency accuracy ±0.4% or ±0.8% max
- Q accuracy ±4%, or ±8% max
- Clock inputs TTL or CMOS compatible
- Single 5V (±2.25V) or ±5V ±10% supply operation guaranteed
- 0°C to +70°C, −40°C to +85°C, −55°C to +125°C operating temperature range
- Standard 0.3" 20-pin DIP or 20-pin small outline (SOIC) package

BLOCK DIAGRAM



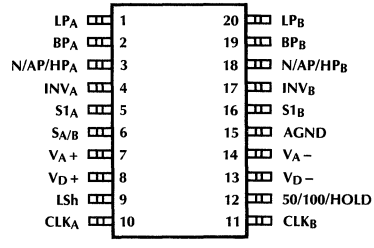
PIN CONNECTIONS

ML2111
20-PIN DIP



TOP VIEW

ML2111
20-PIN SOIC



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	LP_A	Lowpass output for biquad A.
2	BP_A	Bandpass output for biquad A.
3	$N/AP/HP_A$	Notch/allpass/highpass output for biquad A.
4	INV_A	Inverting input of the summing op amp for biquad A.
5	$S1_A$	Auxiliary signal input pin used in modes 1a, 1d, 4, 5, and 6b.
6	$S_{A/B}$	Controls S2 input function.
7	V_A+	Positive analog supply.
8	V_D+	Positive digital supply.
9	LSh	Reference point for clock input levels. Logic threshold typically 1.4V above LSh voltage.
10	CLK_A	Clock input for biquad A.
11	CLK_B	Clock input for biquad B.
12	50/100/HOLD	Input pin to control the clock to center frequency ratio of 50:1 or 100:1, or stops the clock to hold the last sample of the bandpass or lowpass outputs.
13	V_D-	Negative digital supply.
14	V_A-	Negative analog supply.
15	AGND	Analog ground.
16	$S1_B$	Auxiliary signal input used in modes 1a, 1d, 4, 5, and 6b.
17	INV_B	Inverting input of the summing op amp for biquad B.
18	$N/AP/HP_B$	Notch/allpass/highpass output for biquad B.
19	BP_B	Bandpass output for biquad B.
20	LP_B	Lowpass output for biquad B.

3

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage
$|V_A+|, |V_D+| - |V_A-|, |V_D-|$ 13V
V_A+, V_D+ to LSh 13V
Inputs ..... $|V_A+, V_D+| + 0.3V$ to $|V_A-, V_D-| - 0.3V$
Outputs ..... $|V_A+, V_D+| + 0.3V$ to $|V_A-, V_D-| - 0.3V$
$|V_A+|$ to $|V_D+|$ ..... ±0.3V
Power Dissipation 750mW
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (soldering, 10 sec) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
ML2111BCP, ML2111CCP,
ML2111BCS, ML2111CCS ..... 0°C to 70°C
ML2111BIJ, ML2111CIJ ..... −40°C to +85°C
ML2111BMJ, ML2111CMJ ..... −55°C to +125°C
Supply Voltage Range ..... ±2.25V to ±6.0V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_A+ = V_D+ = 5V \pm 10\%$, $V_A- = V_D- = -5V \pm 10\%$, $C_L = 25pF$, $V_{IN} = 1.41V_{PK}$ (1.00 V_{RMS}), Clock Duty Cycle 45% to 55%.

PARAMETER	NOTES	CONDITIONS	ML2111B MIN	ML2111B TYP NOTE 3	ML2111B MAX	ML2111C MIN	ML2111C TYP NOTE 3	ML2111C MAX	UNITS
Filter									
f_o, Center Frequency Maximum	5, 6	Figure 15 (Mode 1) $V_{IN} = 1V_{PK}$ (.707 V_{RMS}) $Q \leq 50$, Q Accuracy $\leq \pm 25\%$ $Q \leq 20$, Q Accuracy $\leq \pm 15\%$			 100 150			 100 150	 kHz kHz
f_o, Center Frequency Minimum	5, 6	Figure 15 (Mode 1) $Q \leq 50$, Q Accuracy $\leq \pm 30\%$ $Q \leq 20$, Q Accuracy $\leq \pm 15\%$	 25 25			 25 25			 Hz Hz
f_o, Temperature Coefficient		$f_{CLK} < 5MHz$		−10			−10		ppm/°C
Clock to Center Frequency Ratio	 4 4	$Q = 10$ Figure 15 (Mode 1) 50:1, $f_{CLK} = 5MHz$ 100:1, $f_{CLK} = 5MHz$	 49.65 99.60	 49.85 100	 50.05 100.40	 49.45 99.20	 49.85 100	 50.25 100.80	

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_A+ = V_D+ = 5V \pm 10\%$, $V_A- = V_D- = -5V \pm 10\%$, $C_L = 25pF$, $V_{IN} = 1.41V_{PK}$ (1.00 V_{RMS}), Clock Duty Cycle 50% (Note 8).

PARAMETER	NOTES	CONDITIONS	ML2111B MIN	ML2111B TYP NOTE 3	ML2111B MAX	ML2111C MIN	ML2111C TYP NOTE 3	ML2111C MAX	UNITS
Filter (Continued)									
Clock Frequency	5	Q ≤ 20, Q Accuracy ≤ ±15%	2.5k		7.5M	2.5k		7.5M	Hz
Clock Feedthrough	5	$f_{CLK} \leq 5MHz$		10	20		10	20	mV(p-p)
Q Accuracy	4	$f_{CLK} = 5MHz$, Q = 10, Figure 15 (Mode 1) 50:1			±3			±5	%
		100:1			±4			±8	%
Q Temperature Coefficient	5	$f_{CLK} < 5MHz$, Q = 10		20			20		ppm/°C
DC Offset		50:1, $f_{CLK} = 5MHz$							
$V_{OS\ 2,3}$	4	$S_{A/B}$ High		7	40		7	60	mV
$V_{OS\ 2,3}$	4	$S_{A/B}$ Low		7	40		7	60	mV
DC Offset		100:1, $f_{CLK} = 5MHz$							
$V_{OS\ 2,3}$	4	$S_{A/B}$ High		14	60		14	100	mV
$V_{OS\ 2,3}$	4	$S_{A/B}$ Low		14	60		14	100	mV
Gain Accuracy									
DC Lowpass	4	R1 = 20k, R2 = 2k, R3 = 20k		0.01	2		0.01	2	%
Bandpass at f_o	4	100:1, f_o = 50kHz, Q = 10		1	4		1	6	%
DC Notch Output	5			0.02	2		0.02	2	%
Noise	7	Figure 15 (Mode 1) Q = 1, R1 = R2 = R3 = 2k							
		Bandpass, 100kHz, 50:1		103			103		μV_{RMS}
		50kHz, 100:1		121			121		μV_{RMS}
		Lowpass, 100kHz, 50:1		120			120		μV_{RMS}
		50kHz, 100:1		150			150		μV_{RMS}
		Notch, 100kHz, 50:1		115			115		μV_{RMS}
		50kHz, 100:1		135			135		μV_{RMS}
		Figure 15 (Mode 1) Q = 10, R1 = R3 = 20k, R2 = 2k							
		Bandpass, 100kHz, 50:1		262			262		μV_{RMS}
		50kHz, 100:1		333			333		μV_{RMS}
		Lowpass, 100kHz, 50:1		268			268		μV_{RMS}
		(R1 = 2k) 50kHz, 100:1		342			342		μV_{RMS}
		Notch, 100kHz, 50:1		64			64		μV_{RMS}
		(R1 = 2k) 50kHz, 100:1		72			72		μV_{RMS}
Crosstalk		$f_{CLK} = 5MHz$, $f_o = 100kHz$		−50			−50		dB
Filter, $V_A+ = V_D+ = 2.25V$, $V_A- = V_D- = -2.25V$, $V_{IN} = 0.707\ V_{PK}$ (0.5V_{RMS}) (NOTE 9)									
f_o, Center Frequency Maximum	5	Figure 15 (Mode 1)							
		Q ≤ 50, Q Accuracy ≤ ±30%			75			75	kHz
		Q ≤ 20, Q Accuracy ≤ ±15%			100			100	kHz
f_o, Center Frequency Minimum	5	Figure 15 (Mode 1)							
		Q ≤ 50, Q Accuracy ≤ ±30%	25			25			Hz
		Q ≤ 20, Q Accuracy ≤ ±15%	25			25			Hz
Clock to Center Frequency Ratio		Q = 10, Figure 15 (Mode 1)							
	4	50:1, $f_{CLK} = 2.5MHz$	49.65	49.85	50.05	49.45	49.85	50.25	
	5	100:1, $f_{CLK} = 2.5MHz$	99.60	100	100.40	99.20	100	100.80	
Clock Frequency	5	Q ≤ 20, Q Accuracy ≤ ±15%	2.5k		5M	2.5k		5M	Hz
Q Accuracy	4	$f_{CLK} = 2.5MHz$, Q = 10, 50:1			±4			±8	%
		Figure 15 (Mode 1) 100:1		±3			±6		%

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_A+ = V_D+ = 5V \pm 10\%$, $V_A- = V_D- = -5V \pm 10\%$, $C_L = 25pF$, $V_{IN} = 1.41V_{PK}$ (1.00 V_{RMS}), Clock Duty Cycle 50% (Note 8).

PARAMETER	NOTES	CONDITIONS	ML2111B MIN	ML2111B TYP NOTE 3	ML2111B MAX	ML2111C MIN	ML2111C TYP NOTE 3	ML2111C MAX	UNITS
Filter, $V_A+ = V_D+ = 2.25V$, $V_A- = V_D- = -2.25V$, $V_{IN} = 0.707\ V_{PK}$ (0.5 V_{RMS}) (Continued)									
Noise	7	Figure 15 (Mode 1)							
		Q = 1, R1 = R2 = R3 = 2k							
		Bandpass, 100kHz, 50:1		105			105		μV_{RMS}
		50kHz, 100:1		123			123		μV_{RMS}
		Lowpass, 100kHz, 50:1		122			122		μV_{RMS}
		50kHz, 100:1		152			152		μV_{RMS}
		Notch, 100kHz, 50:1		117			117		μV_{RMS}
		50kHz, 100:1		138			138		μV_{RMS}
		Figure 15 (Mode 1)							
		Q = 10, R1 = R3 = 20k, R2 = 2k							
		Bandpass, 100kHz, 50:1		265			265		μV_{RMS}
		50kHz, 100:1		335			335		μV_{RMS}
		Lowpass, 100kHz, 50:1		270			270		μV_{RMS}
		(R1 = 2k) 50kHz, 100:1		245			245		μV_{RMS}
		Notch, 100kHz, 50:1		65			65		μV_{RMS}
		(R1 = 2k) 50kHz, 100:1		73			73		μV_{RMS}
Operational Amplifiers and Power Supply									
V_{OS} DC Offset	4			2	15		2	15	mV
DC Open Loop Gain		$R_L = 1k$		95			95		dB
Gain Bandwidth Product				2.4			2.4		MHz
Slew Rate				2.0			2.0		V/μs
Output Voltage Swing (Clipping Level)	5	$R_L = 2k$, $\|V\|$ from V_{A+} or V_{A-}		0.5	1.2		0.5	1.2	V
Output Short Circuit Current		Source		50			50		mA
		Sink		25			25		mA
Power Supply And Clock									
Supply Current	4	$f_{CLK} = 5MHz$							
$(I_A+) + (I_D+)$				13	22		13	22	mA
$(I_A-) + (I_D-)$				12	21		12	21	mA
I_{LSH}				0.5	1		0.5	1	mA
V_{CLK} Input Threshold	4	$f_{CLK} = 5MHz$ Low			0.6			0.6	V
		High	3.0			3.0			V
	5	$f_{CLK} < 2.5MHz$ Low			0.8			0.8	V
		High	2.0			2.0			V
CLKA, CLKB Pulse Width	5, 8	CLK High or $\|V_D+\| - \|V_D-\| \geq 4.5V$	100			100			ns
		CLK Low $\|V_D+\| - \|V_D-\| \geq 9.0V$	66			66			ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: -55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. 0°C to 70°C and -40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 6: Center frequency is defined as the peak of the bandpass output.

Note 7: The noise is measured with the HP8903A audio analyzer with a bandwidth of 750kHz which is 7.5 times the f_O at 50:1 and 15 times the f_O at 100:1.

Note 8: For best performance with $f_{CLK} > 2.5MHz$ use a 50% duty cycle.

Note 9: For $T_A = -55°C$ to +125°C; $V_A+ = V_D+ = 2.375V$, $V_A- = V_D- = -2.375V$

FUNCTIONAL DESCRIPTION

POWER SUPPLIES

The analog (V_A+) and digital (V_D+) supply voltage pins should be tied together and bypassed to AGND with at least a 0.1μF and a 0.01μF disc ceramic capacitor. If high digital noise exists, the supply pins can be bypassed separately. The ML2111 positive analog and positive digital supply pins are internally connected by the IC substrate and should be biased from the same DC source. The ML2111 negative analog and negative digital supply are not connected internally, however they should be biased from the same DC source and bypassed with at least a 0.1μF and a 0.01μF disc ceramic capacitor.

The ML2111 operates with a single supply from 4V to 12V and with split supplies from ±2.0V to ±6V.

CLOCK INPUT PINS AND LEVEL SHIFT

With dual supplies equal to or higher than ±4.0V, the level shift (LSh) pin 9 can be connected to the same potential as the AGND or V_A- pin. With single supply operation, the negative supply pins and the LSh pin should be tied to the system ground. The AGND, pin 15, should be biased at 1/2 supplies. Under these conditions, the clock levels are TTL or CMOS. The input clock pins (10, 11) share the same level shift pin.

50/100/HOLD (Pin 12)

By tying pin 12 to (V_A+, V_D+) the filter operates in the 50:1 mode. By tying pin 12 to 1/2 of the voltage supplies (AGND potential), the ML2111 operates in the 100:1 mode. The range of pin 12 without affecting the 100:1 filter operation with total supply voltage of +5V is 2.5±0.5V; +10V is 5V±0.5V. When pin 12 is tied to the negative supply pin, the filter operation is stopped and the bandpass and lowpass outputs act as an S/H circuit holding the last sample.

$S1_A$, $S1_B$, (Pins 5 and 16)

These are the auxiliary voltage signal input pins always connected to one of the negative inputs of the voltage summer (the other negative input switches between LPo and AGND according to control pin $S_{A/B}$ (pin 6). The positive input of the voltage summer is always connected to N/AP/HP pin of the corresponding section. They should be driven with a source impedance below 5k for $f_{CLK} < 2.5$MHz and 1k to 2k for $f_{CLK} > 2.5$MHz. The $S1_A$, $S1_B$ pins can be used to alter the clock to center frequency ratio (f_{CLK}/f_o) of the filter (see modes 1b, 1c, 2a, 2b) or to feedforward the input signal for allpass filter configurations (see modes 4 and 5). They can also be used, as in mode 1d to avoid the finite phase shift through the input amplifier, hence allowing higher operating frequencies. When these pins are not used, they should be tied to the AGND pin.

$S_{A/B}$ (Pin 6)

When $S_{A/B}$ is high, the S2 negative input of the voltage summer is tied to the lowpass output. When the $S_{A/B}$ pin is connected to the negative supply, the S2 input switches to ground.

AGND (Pin 15)

AGND is connected to the system ground for dual supply operation. When operating with a single positive supply, the analog ground pin should be tied to 1/2 of the supply and bypassed with a 0.1μF and a 0.01μF disc ceramic capacitor. The positive inputs of the internal op amps and the reference point of the internal switches are connected to the AGND pin.

f_{CLK}/f_o RATIO

The ML2111 is a sampled data filter and approximates continuous time filters. The filter deviates from its ideal continuous filter model when the (f_{CLK}/f_o) ratio decreases and when the Qs are low.

$f_o \times Q$ PRODUCT RATIO

The $f_o \times Q$ product of the ML2111 depends on the clock frequency and the mode of operation. For clock frequencies below 5MHz, in mode 1 and its derivatives, the $f_o \times Q$ product is mainly limited by the desired f_o and Q accuracy. For the same clock frequency and for the same Q value the $f_o \times Q$ product can be further increased if the clock to center frequency ratio is lowered below 50:1.

Mode 3, Figure 23, and the modes of operation where R4 is finite, are "slower" than the basic mode 1. The resistor R4 places the input op amp inside the resonant loop. The finite GBW of this op amp creates an additional phase shift and enhances the Q value at high clock frequencies.

OUTPUT NOISE

The wideband RMS noise of the ML2111 outputs is nearly independent from the clock frequency provided that the clock itself does not become part of the noise. The noise at the BP and LP outputs increases for high Qs.

TYPICAL PERFORMANCE CURVES

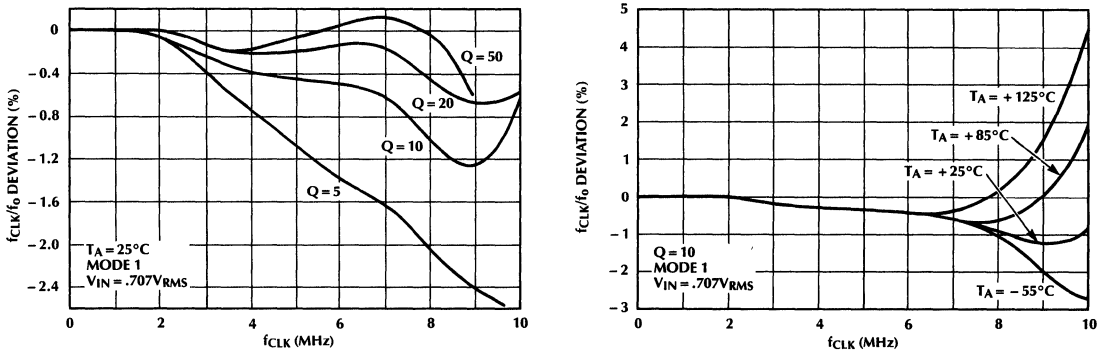


Figure 1A. f_{CLK}/f_o vs. f_{CLK} (50:1, $V_S = \pm 5V$)

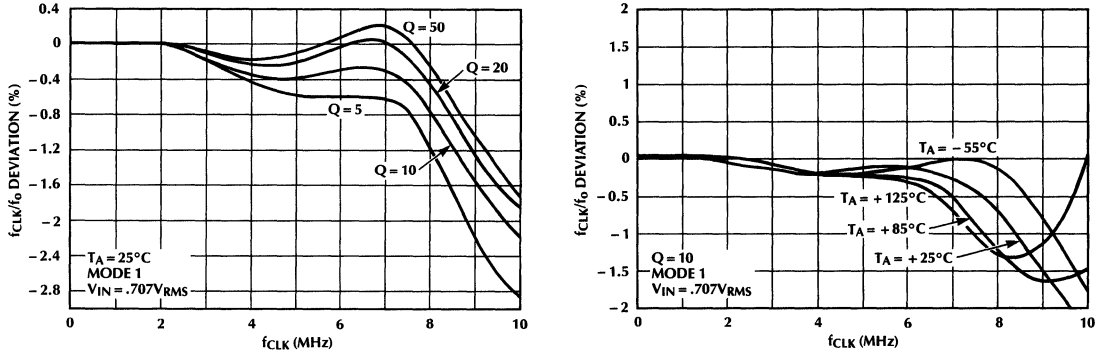


Figure 1B. f_{CLK}/f_o vs. f_{CLK} (100:1, $V_S = \pm 5V$)

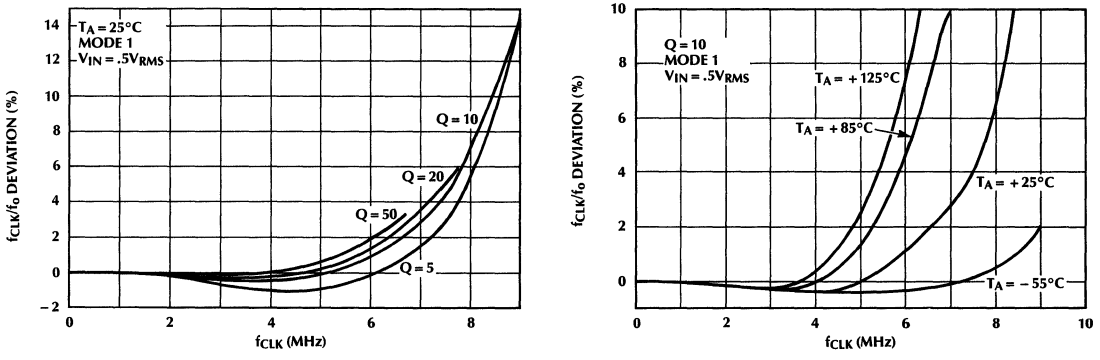
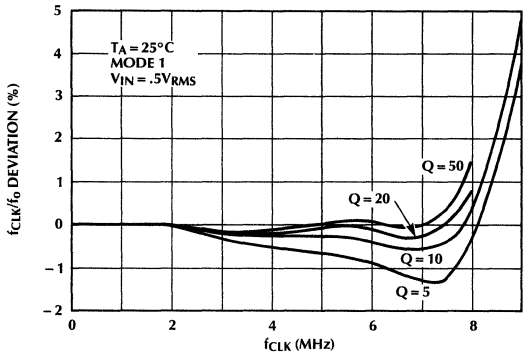


Figure 1C. f_{CLK}/f_o vs. f_{CLK} (50:1, $V_S = \pm 2.5V$)

TYPICAL PERFORMANCE CURVES (Continued)



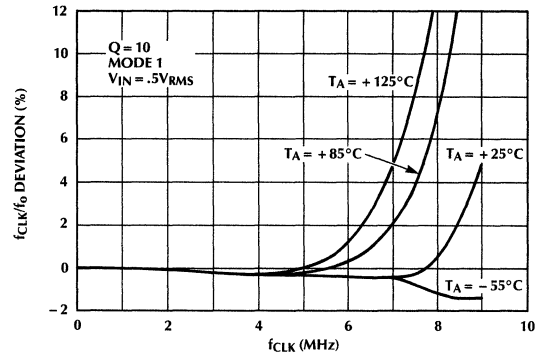


Figure 1D. f_{CLK}/f_o vs. f_{CLK} (100:1, V_S = ±2.5V)

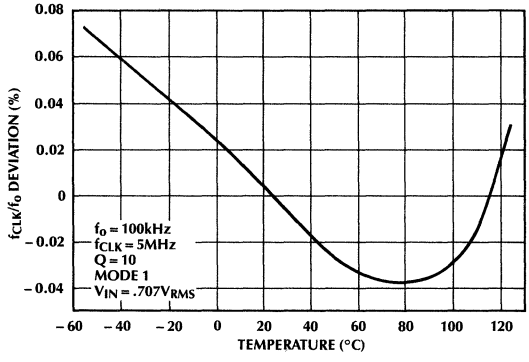


Figure 2A. f_{CLK}/f_o Deviation vs. Temperature (50:1, V_S = ±5V)

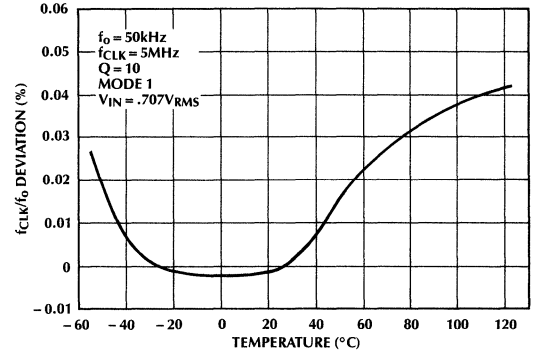


Figure 2B. f_{CLK}/f_o Deviation vs. Temperature (100:1, V_S = ±5V)

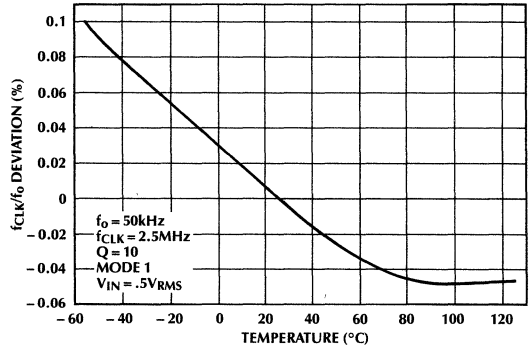


Figure 2C. f_{CLK}/f_o Deviation vs. Temperature (50:1, V_S = ±2.5V)

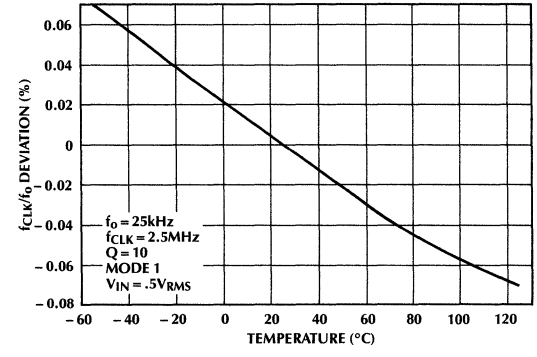


Figure 2D. f_{CLK}/f_o Deviation vs. Temperature (100:1, V_S = ±2.5V)

TYPICAL PERFORMANCE CURVES (Continued)

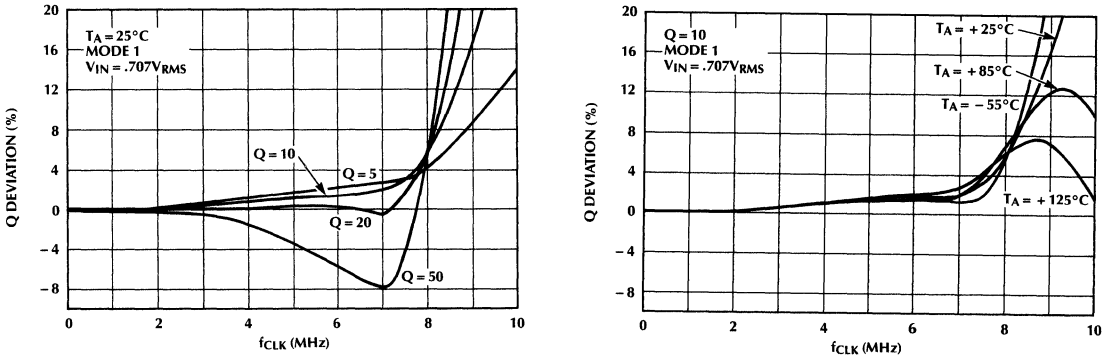


Figure 2E. Q Error vs. f_{CLK} (50:1, $V_S = \pm 5V$)

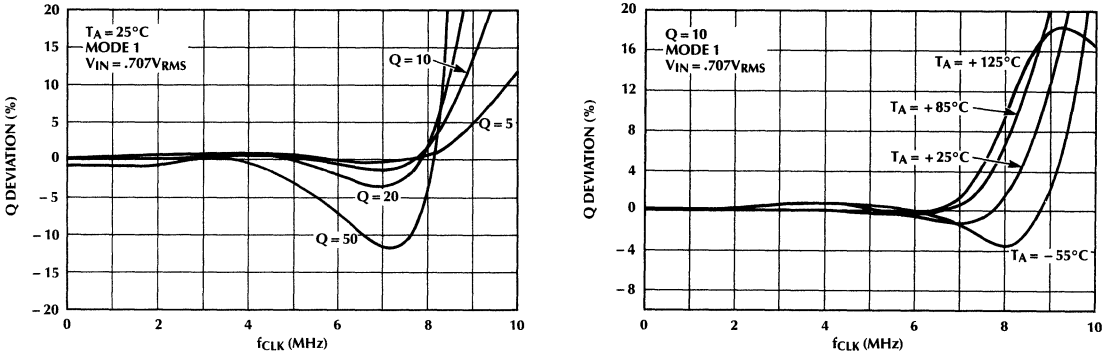


Figure 2F. Q Error vs. f_{CLK} (100:1, $V_S = \pm 5V$)

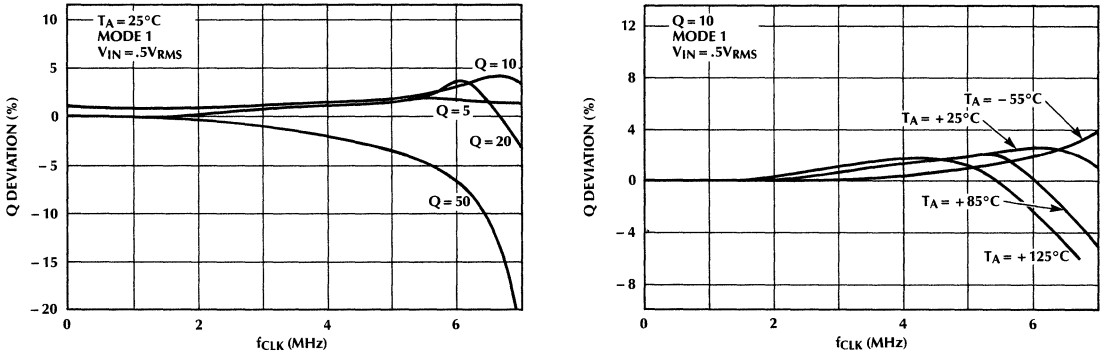
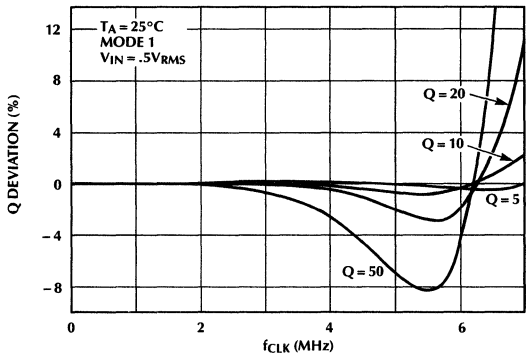


Figure 2G. Q Error vs. f_{CLK} (50:1, $V_S = \pm 2.5V$)

TYPICAL PERFORMANCE CURVES (Continued)



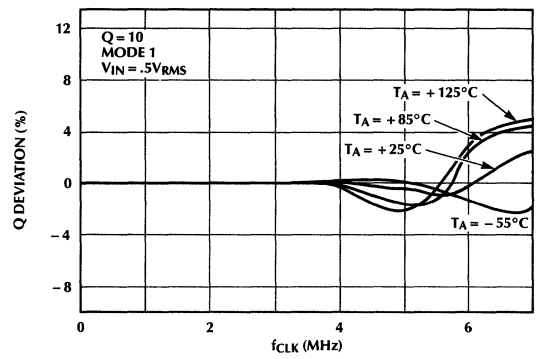


Figure 2H. Q Error vs. f_{CLK} (100:1, V_S = ±2.5V)

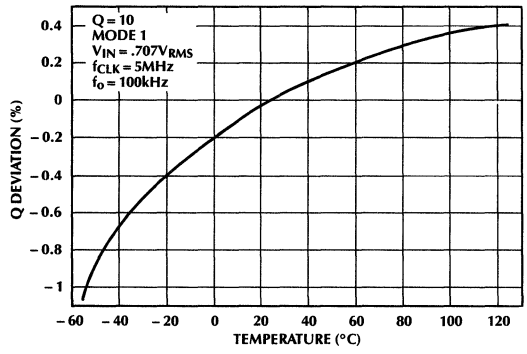


Figure 3A. Q Deviation vs. Temperature (50:1, V_S = ±5V)

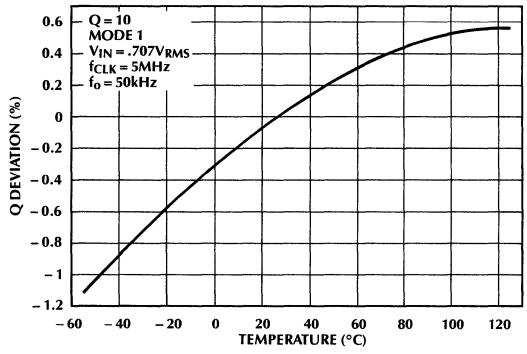


Figure 3B. Q Deviation vs. Temperature (100:1, V_S = ±5V)

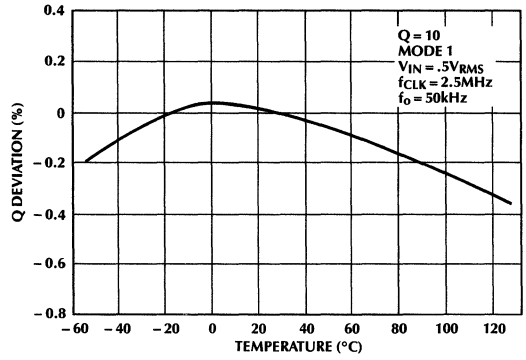


Figure 3C. Q Deviation vs. Temperature (50:1, V_S = ±2.5V)

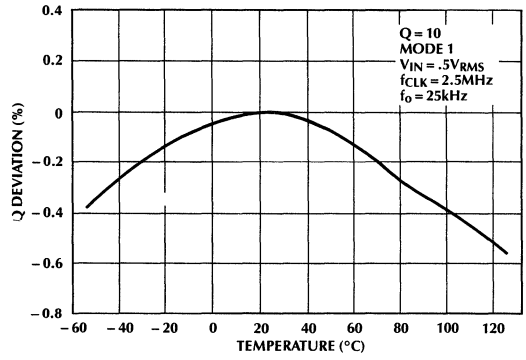


Figure 3D. Q Deviation vs. Temperature (100:1, V_S = ±2.5V)

TYPICAL PERFORMANCE CURVES (Continued)

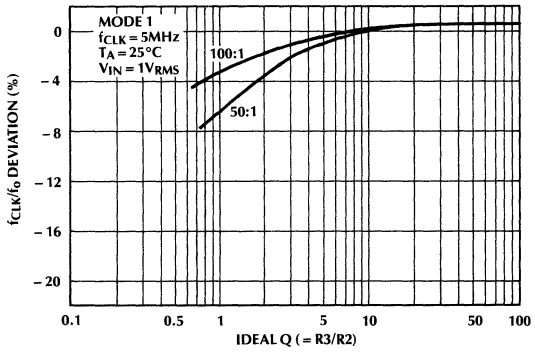


Figure 4A. f_{CLK}/f_o Deviation vs. Q (V_S = ±5V)

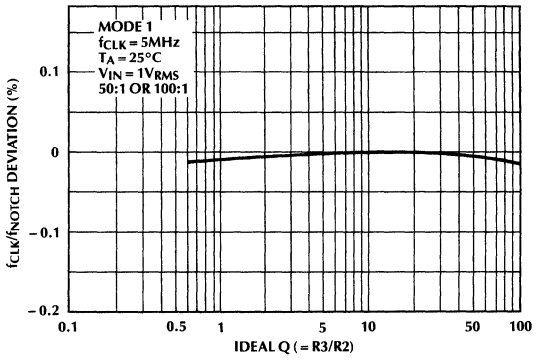


Figure 4B. f_{CLK}/f_{NOTCH} Deviation vs. Q (V_S = ±5V)

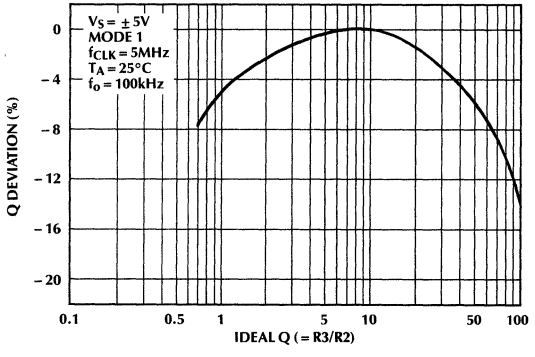


Figure 5A. Q Deviation vs. Q (50:1, V_S = ±5V)

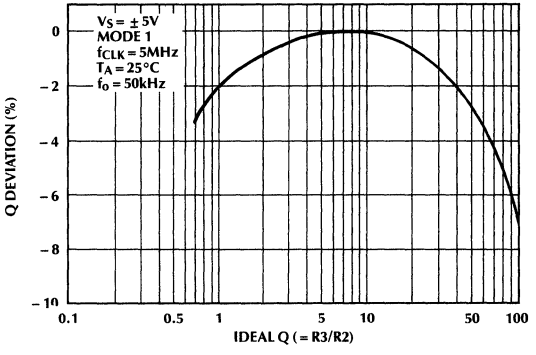


Figure 5B. Q Deviation vs. Q (100:1, V_S = ±5V)

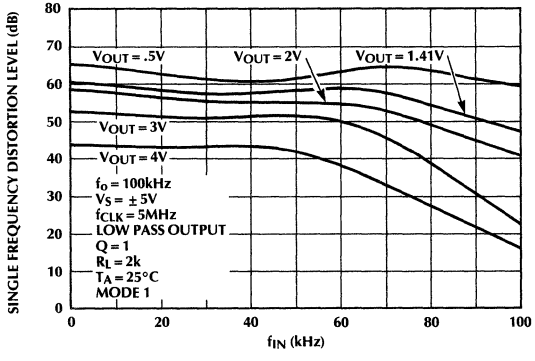


Figure 6A. Distortion vs. f_{IN} (50:1, V_S = ±5V)

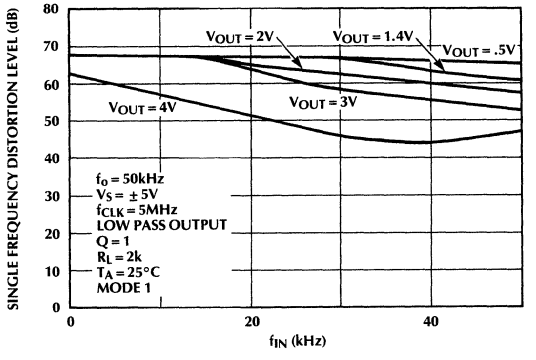


Figure 6B. Distortion vs. f_{IN} (100:1, V_S = ±5V)

TYPICAL PERFORMANCE CURVES (Continued)

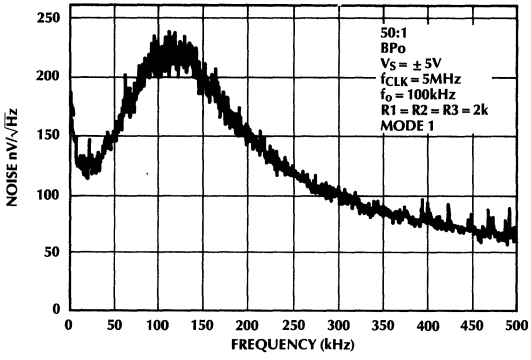


Figure 7A. Noise Spectrum Density (Q = 1)

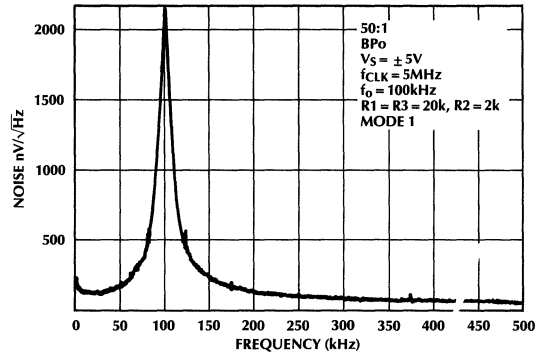


Figure 7B. Noise Spectrum Density (Q = 10)

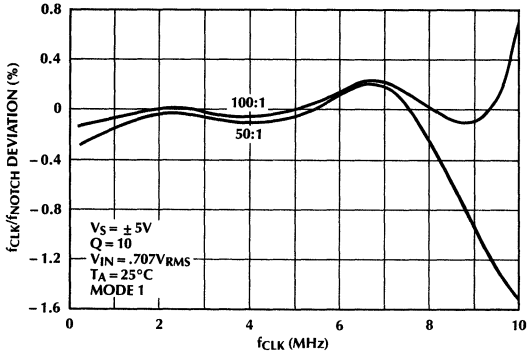


Figure 8. f_{CLK}/f_{NOTCH} vs. f_{CLK}

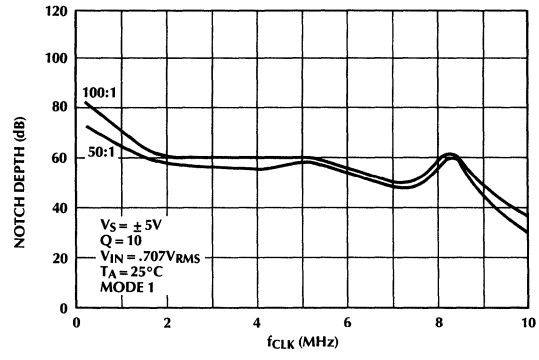


Figure 9. Notch Depth vs. f_{CLK}

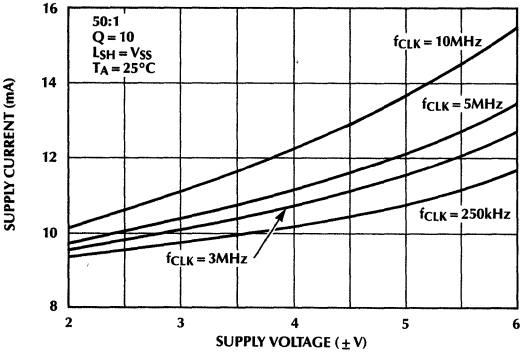


Figure 10. Supply Current vs. Supply Voltage

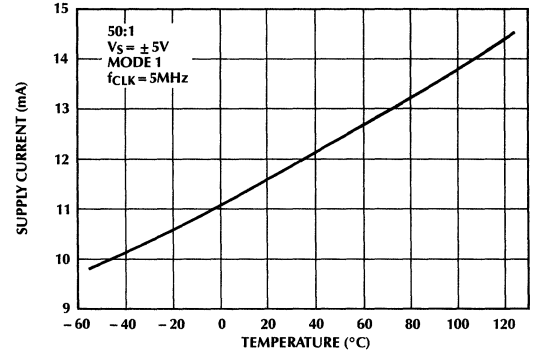


Figure 11. Supply Current vs. Temperature

FILTER FUNCTION DEFINITIONS

Each filter of the ML2111 with an external clock and resistors approximates 2nd order filter functions. These are tabulated below in the frequency domain.

1. **Bandpass function:** available at the bandpass output pins (2, 19), Figure 12.

$$G(s) = H_{OBP}\frac{s\omega_o/Q}{s^2 + (s\omega_o/Q) + \omega_o^2}$$

H_{OBP} = Gain at $\omega = \omega_o$

$f_o = \omega_o/2\pi$; f_o is the center frequency of the complex pole pair. f_o is measured as the peak frequency of the bandpass output.

Q = Quality factor of the complex pole pair. It is the ratio of f_o to the −3dB bandwidth of the 2nd order bandpass function. The Q is always measured at the filter BP output.

2. **Lowpass function:** available at the LP output pins (1, 20), Figure 13.

$$G(s) = H_{OLP}\frac{\omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OLP} = DC gain of the LP output.

3. **Highpass function:** available only in mode 3 at the output pins (3, 18), Figure 14.

$$G(s) = H_{OHP}\frac{s^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OHP} = gain of the HP output for $f \rightarrow \frac{f_{CLK}}{2}$

4. **Notch function:** available at pins 3 (18) for several modes of operation.

$$G(s) = (H_{ON2})\frac{(s^2 + \omega_n^2)}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{ON2} = gain of the notch output for $f \rightarrow \frac{f_{CLK}}{2}$

H_{ON1} = gain of the notch output for $f \rightarrow 0$

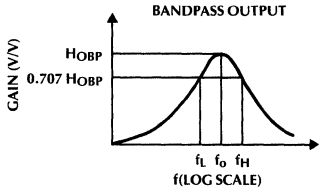
$f_n = \omega_n/2\pi$; f_n is the frequency of the notch occurrence.

5. **Allpass function:** available at pins 3(18) for mode 4, 4a.

$$G(s) = H_{OAP}\frac{[s^2 - s(\omega_o/Q) + \omega_o^2]}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OAP} = gain of the allpass output for $0 < f < \frac{f_{CLK}}{2}$

For allpass functions, the center frequency and the Q of the numerator complex zero pair is the same as the denominator. Under these conditions, the magnitude response is a straight line. In mode 5, the center frequency f_Z, of the numerator complex zero pair, is different than f_o. For high numerator Q's, the magnitude response will have a notch at f_Z.

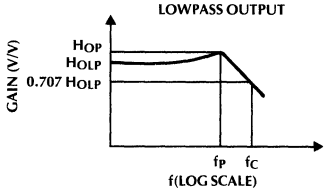


$$Q = \frac{f_o}{f_H - f_L};\ f_o = \sqrt{f_L f_H}$$

$$f_L = f_o\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_o\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

Figure 12

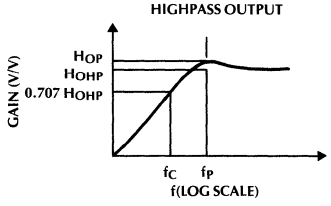


$$f_C = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_P = f_o\sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 13



$$f_C = f_o \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_P = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 14

OPERATION MODES

Table 1. 1st Order Functions

MODE	PIN 2 (19)	PIN 3 (18)	f_C	f_Z
6a	LP	HP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	
6b	LP	LP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	
7	LP	AP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$

Table 2. 2nd Order Functions

MODE	PIN 1 (20)	PIN 2 (19)	PIN 3 (18)	f_o	f_N
1	LP	BP	Notch	$\frac{f_{CLK}}{100(50)}$	f_o
1a	LP	BP	BP	$\frac{f_{CLK}}{100(50)}$	
1b	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5+R6}}$
1c	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$
1d	LP	BP		$\frac{f_{CLK}}{100(50)}$	
2	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)}$
2a	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4} + \frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5+R6}}$
2b	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4} + \frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$
3	LP	BP	HP	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	
3a	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R_h}{R_l}}$
4	LP	BP	AP	$\frac{f_{CLK}}{100(50)}$	
4a	LP	BP	AP	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	
5	LP	BP	C.Z	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 - \frac{R1}{R4}}$

OPERATION MODES (Continued)

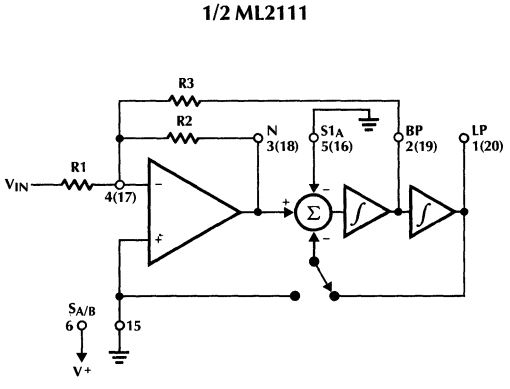
There are basically three modes of operation: mode 1, mode 2, mode 3. In the mode 1, Figure 15, the input amplifier is outside the resonant loop. Because of this, mode 1 and its derivatives (mode 1a, 1b, 1c, 1d) are faster than modes 2 and 3. The table below gives an approximation of the frequency range for each mode.

Mode 1*	High Frequency Mode
1, 1a, 1d	f_0 up to 150kHz; Q up to 20**
1b, 1c	f_0 up to 100kHz; Q up to 30
Mode 2	**Flexible for Notches**
2, 2a, 2b	f_0 up to 30kHz; Q up to 30
Mode 3	**Most Flexible/Low Component Count**
3, 3a	f_0 up to 30kHz; Q up to 30

* Q and f_0 have an inverse relationship. This table is only an approximation. Actual performance depends on board layout and stray capacitance.

** 15% of less Q deviation Higher Q's can be realized with greater deviation

Mode 1a, Figure 16, represents the most simple hook-up of the ML2111. Mode 1a is useful when voltage gain at the bandpass output is required. The bandpass voltage gain, however, is equal to the value of Q, and a second order, clock tunable, BP resonator can be achieved with only 2 resistors. The filter center frequency directly depends on the external clock frequency. For high order filters, mode 1a is not practical as it requires several clock frequencies to tune the overall filter response.



$$f_0 = \frac{f_{CLK}}{100(50)};\ f_n = f_0;\ H_{OLP} = -\frac{R2}{R1};\ H_{OBP} = -\frac{R3}{R1};\ H_{ON1} = -\frac{R2}{R1};\ Q = \frac{R3}{R2}$$

NOTE: ELECTRICAL TESTING IS PERFORMED WITH FOLLOWING RESISTOR VALUES:
Q = 1 WITH R1 = R2 = R3 = 2k
Q = 10 WITH R1 = R3 = 20k, R2 = 2k

Figure 15. Mode 1: 2nd Order Filter Providing Notch, Bandpass, Lowpass

Mode 1a is a good choice when Butterworth filters are desired since they have poles in a circle with the same f_0. Figure 31 shows an example of a 4th order 100kHz lowpass Butterworth filter clocked at 5MHz.

A monotonic passband response with a smooth transition band results, showing the circuit's low sensitivity, even though 1% resistors are used which result in an approximate value of Q.

Mode 1, Figure 15, provides a clock tunable notch. Mode 1 is a practical configuration for second order clock tunable bandpass/notch filters. In mode 1, a bandpass output with a very high Q, together with unity gain, can be obtained with the dynamics of the remaining notch and lowpass outputs. Figure 32 is an example of a 4th order bandpass filter implemented by cascading 2 sections each with a Q of 10. This figure shows the amplitude response when $f_{CLK} = 7.5$MHz resulting in a center frequency of 150kHz and a Q of 15.5.

Modes 1b and 1c, Figures 17, 18 are similar. They both produce a notch with a frequency which is always equal to the filter center frequency. The notch and the center frequency can be adjusted with an external resistor ratio.

The clock to center frequency ratio range is:

$$\frac{500}{1} \geq \frac{f_{CLK}}{f_0} \geq \frac{100}{1} \text{ or } \frac{50}{1};\ \text{mode 1c}$$

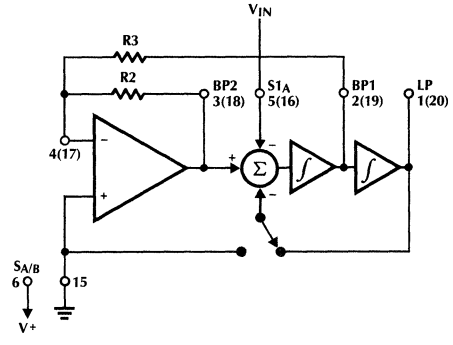
$$\frac{100}{1} \text{ or } \frac{50}{1} \geq \frac{f_{CLK}}{f_0} \geq \frac{100}{\sqrt{2}} \text{ or } \frac{50}{\sqrt{2}};\ \text{mode 1b}$$

The input impedance of the S1 pin is clock dependent, and in general R5 should not be larger than 5k for $f_{CLK} < 2.5$MHz and 1k to 2k for $f_{CLK} > 2.5$MHz. Mode 1b can be used to increase the clock to center frequency ratio beyond 100:1. For this mode, the limit for the (f_{CLK}/f_0) ratio is 500:1. Beyond this, the filter will exhibit large output offsets. Mode 1d, Figure 19, is the fastest mode of operation: In the 50:1 mode center frequencies beyond 150kHz can easily be achieved. Figure 33 is an example using mode 1d of a 4th order filter where each section has a Q of 1 independent of resistor ratios. In this mode the input amplifier is outside the damping (Q) loop. Therefore, its finite bandwidth does not degrade the response at high frequency. This allows the amplifier to be used as an anti-aliasing and continuous smoothing filter by placing a capacitor across R2.

Modes 2, 2a, and 2b have a notch output which frequency, f_n, can be tuned independently from the center frequency, f_0. For all cases, however, $f_n < f_0$. These modes are useful when cascading second order functions to create an overall elliptic highpass, bandpass or notch response. The input amplifier and its feedback resistors (R2/R4) are now part of the resonant loop. Because of this, mode 2 and its derivatives are slower than mode 1's.

OPERATION MODES (Continued)

1/2 ML2111

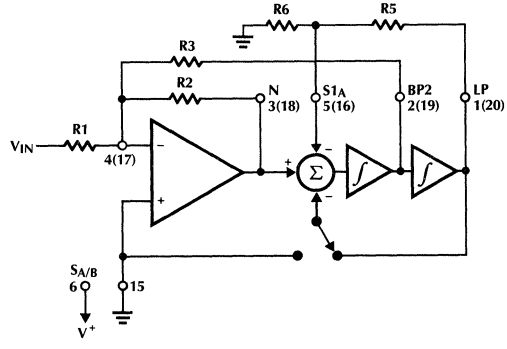


$$f_o = \frac{f_{CLK}}{100(50)}; Q = \frac{R3}{R2}; H_{OBP1} = -\frac{R3}{R2};$$

$$H_{OBP2} = 1(\text{NONINVERTING}); H_{OLP} = -1$$

Figure 16. Mode 1a: 2nd Order Filter Providing Bandpass, Lowpass

1/2 ML2111

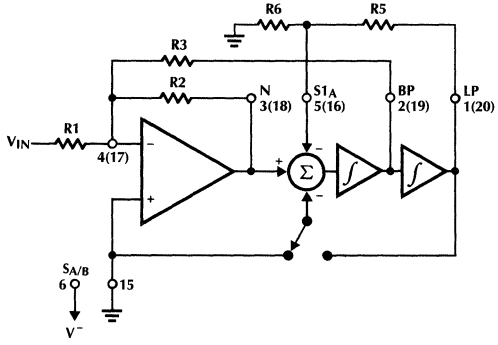


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R6}{R5+R6}}; f_n = f_o; Q = \frac{R3}{R2}\sqrt{1+\frac{R6}{R5+R6}};$$

$$H_{ON1}(f\rightarrow 0) = H_{ON2}\left(f-\frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}; H_{OBP} = -\frac{R3}{R1}; H_{OLP} = \frac{-R2/R1}{1+R6/(R5+R6)}; R5 < 5k\Omega$$

Figure 17. Mode 1b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2111

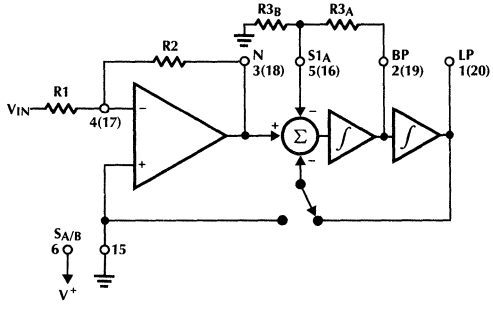


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R6}{R5+R6}}; f_n = f_o; Q = \frac{R3}{R2}\sqrt{\frac{R6}{R5+R6}};$$

$$H_{ON1}(f\rightarrow 0) = H_{ON2}\left(f\rightarrow\frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}; H_{OLP} = \frac{-R2/R1}{R6/(R5+R6)}; H_{OBP} = -\frac{R3}{R1}; R5 < 5k\Omega$$

Figure 18. Mode 1c: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2111



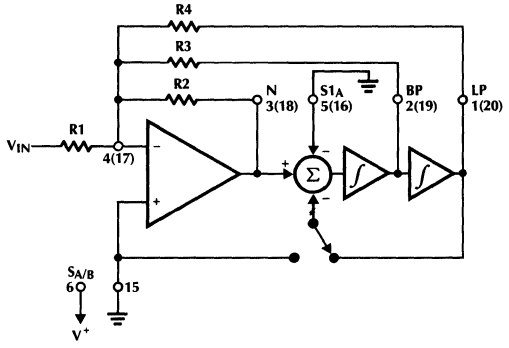
$$f_o = \frac{f_{CLK}}{100(50)}; Q = 1+\frac{R3_A}{R3_B}; H_{OBP} = -\frac{R2}{R1}\times Q$$

$$H_{OLP} = -\frac{R2}{R1}; V_N = -\frac{R2}{R1}V_{IN}$$

Figure 19. Mode 1d: 2nd Order Filter Providing Bandpass and Lowpass for Qs Greater or Equal to 1

OPERATION MODES (Continued)

1/2 ML2111

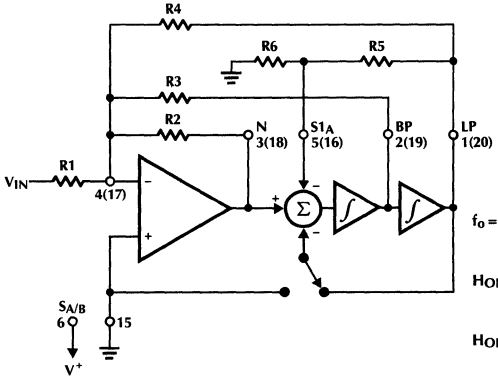


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}};\ f_n = \frac{f_{CLK}}{100(50)};\ Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}};\ H_{OLP} = \frac{-R2/R1}{1+(R2/R4)}$$

$$H_{OBP} = -R3/R1;\ H_{ON1}(f\rightarrow 0) = \frac{-R2/R1}{1+(R2/R4)};\ H_{ON2}\left(f\rightarrow\frac{f_{CLK}}{2}\right) = -R2/R1$$

Figure 20. Mode 2: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2111



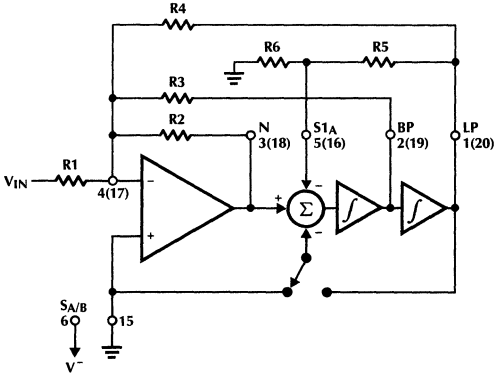
$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}+\frac{R6}{R5+R6}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R6}{R5+R6}};\ Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}+\frac{R6}{R5+R6}}$$

$$H_{ON1}(f\rightarrow 0) = -\frac{R2}{R1}\left\{\frac{1+R6/(R5+R6)}{1+(R2/R4)+[R6/(R5+R6)]}\right\};\ H_{ON2}\left(f\rightarrow\frac{f_{CLK}}{2}\right) = -R2/R1$$

$$H_{OBP} = -R3/R1;\ H_{OLP} = \frac{-R2/R1}{1+(R2/R4)+[R6/(R5+R6)]}$$

Figure 21. Mode 2a: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2111



$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}+\frac{R6}{R5+R6}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R6}{R5+R6}};\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}+\frac{R6}{R5+R6}}$$

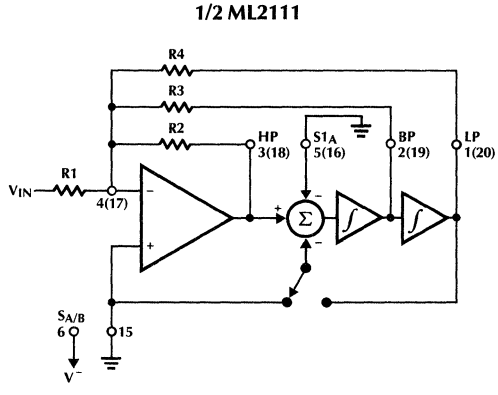
$$H_{ON1}(f\rightarrow 0) = -\frac{R2}{R1}\left\{\frac{R6/(R5+R6)}{(R2/R4)+[R6/(R5+R6)]}\right\};\ H_{ON2}\left(f\rightarrow\frac{f_{CLK}}{2}\right) = -R2/R1$$

$$H_{OBP} = -R3/R1;\ H_{OLP} = \frac{-R2/R1}{(R2/R4)+[R6/(R5+R6)]}$$

Figure 22. Mode 2b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

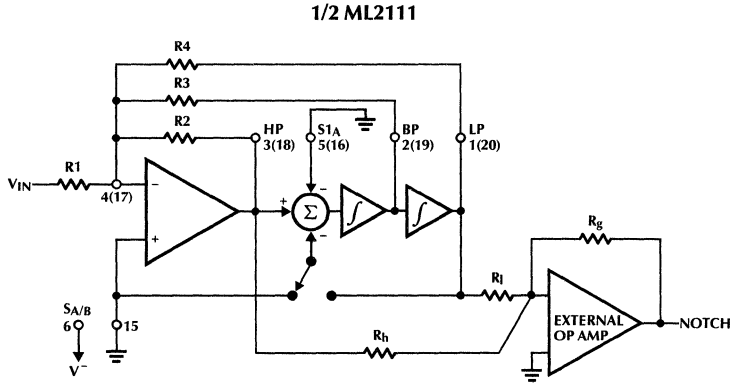
OPERATION MODES (Continued)

In mode 3, Figure 23, a single resistor ratio (R2/R4) can tune the center frequency below or above the $f_{CLK}/100$ (or $f_{CLK}/50$) ratio. Mode 3 is a state variable configuration since it provides a highpass, bandpass, lowpass output through progressive integration; notches are obtained by summing the highpass and lowpass outputs (modes 3a, Figure 24). The notch frequency can be tuned below or above the center frequency through the resistor ratio (R_h/R_l). Because of this, modes 3 and 3a are the most versatile and useful modes for cascading second order sections to obtain high order elliptic filters with frequencies up to 30 kHz.



$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}};\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}};\ H_{OHP} = -R2/R1;\ H_{OLP} = -R4/R1;\ H_{OBP} = -\frac{R3}{R1}$$

Figure 23. Mode 3: 2nd Order Filter Providing Highpass, Bandpass, Lowpass



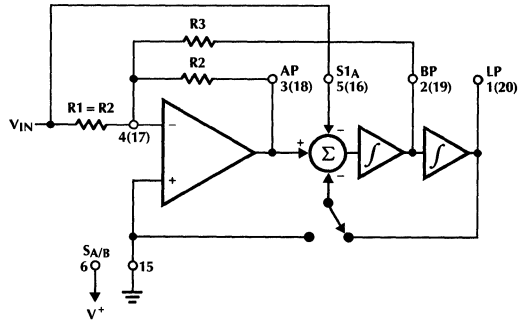
$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{\frac{Rh}{Rl}};\ H_{OHP} = -R2/R1;\ H_{OBP} = -R3/R1,\ H_{OLP} = -R4/R1$$

$$H_{ON1(f\to 0)} = \frac{Rg}{Rl} \times \frac{R4}{R1};\ H_{ON2}\left(f \to \frac{f_{CLK}}{2}\right) = \frac{Rg}{Rh} \times \frac{R2}{R1};\ H_{ON(f=f_o)} = Q\left(\frac{Rg}{Rl}H_{OLP} - \frac{Rg}{Rh}H_{OHP}\right)$$

Figure 24. Mode 3a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Notch

OPERATION MODES (Continued)

1/2 ML2111

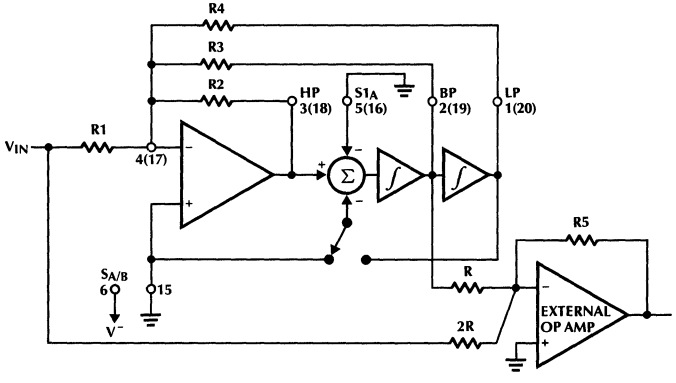


$$f_o = \frac{f_{CLK}}{100(50)}; Q = \frac{R3}{R2}; H_{OAP} = -\frac{R2}{R1}; H_{OLP} = -2; H_{OBP} = -2\left(\frac{R3}{R2}\right)$$

Figure 25. Mode 4: 2nd Order Filter Providing Allpass, Bandpass, Lowpass

3

1/2 ML2111

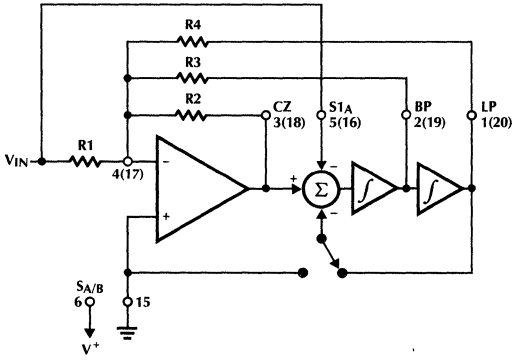


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}}; Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}}; H_{OAP} = \frac{R5}{2R}; H_{OHP} = -\frac{R2}{R1}; H_{OBP} = -\frac{R3}{R1}; H_{OLP} = -\frac{R4}{R1}$$

Figure 26. Mode 4a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Allpass

OPERATION MODES (Continued)

1/2 ML2111



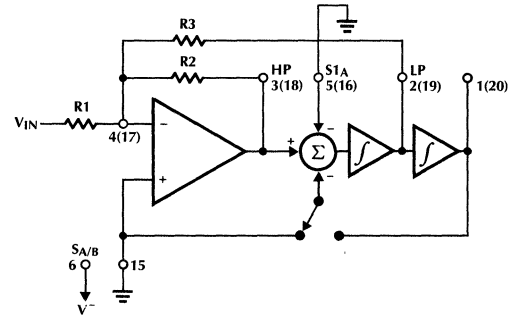
$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}};\ f_z = \frac{f_{CLK}}{100(50)}\sqrt{1-\frac{R1}{R4}};\ Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}}$$

$$Q_Z = \frac{R3}{R1}\sqrt{1-\frac{R1}{R4}};\ H_{OZ}(f\rightarrow 0) = \frac{(R4/R1)-1}{(R4/R2)+1};\ H_{OZ}\left(f\rightarrow\frac{f_{CLK}}{2}\right) = \frac{R2}{R1};$$

$$H_{OBP} = \frac{R3}{R2}\left(1+\frac{R2}{R1}\right);\ H_{OLP} = \frac{1+(R2/R1)}{1+(R2/R4)}$$

Figure 27. Mode 5: 2nd Order Filter Providing Numerator Complex Zeros, Bandpass, Lowpass

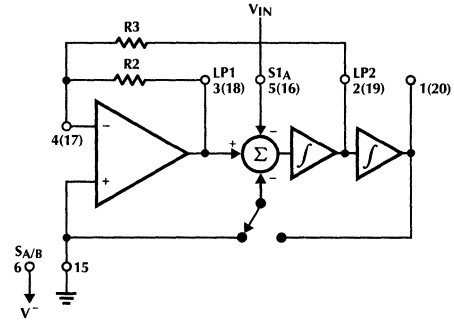
1/2 ML2111



$$f_C = \frac{f_{CLK}\ R2}{100(50)\ R3};\ H_{OLP} = -R3/R1;\ H_{OHP} = -R2/R1$$

Figure 28. Mode 6a: 1st Order Filter Providing Highpass, Lowpass

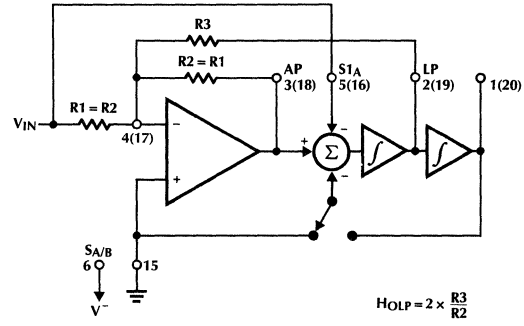
1/2 ML2111



$$f_C = \frac{f_{CLK}\ R2}{100(50)\ R3};\ H_{OLP1} = 1;\ H_{OLP2} = -\frac{R3}{R2}$$

Figure 29. Mode 6b: 1st Order Filter Providing Lowpass

1/2 ML2111



$$f_p = \frac{f_{CLK}\ R2}{100(50)\ R3};\ f_Z = \frac{f_{CLK}\ R2}{100(50)\ R3};\ \text{GAIN AT OUTPUT} = 1\ \text{FOR}\ 0 \le f \le \frac{f_{CLK}}{2}$$

Figure 30. Mode 7: 1st Order Filter Providing Allpass, Lowpass

OPERATION MODES (Continued)

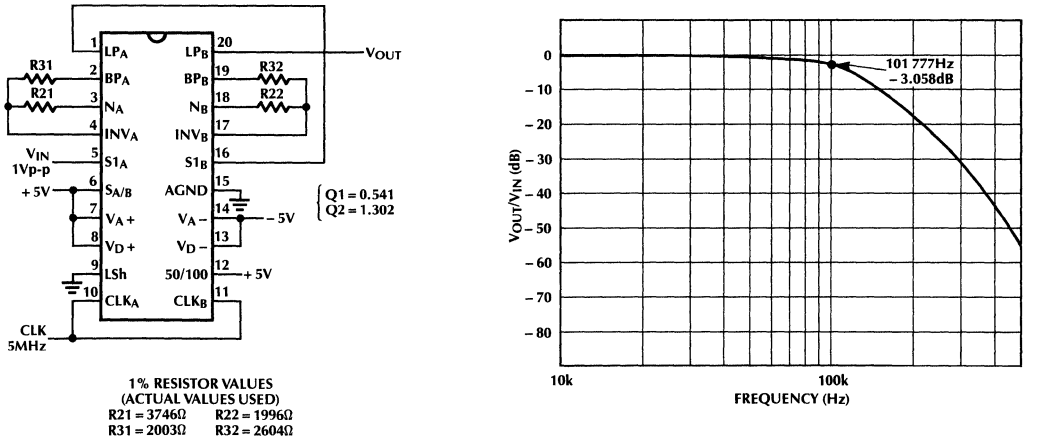


Figure 31. 4th Order, 100kHz Lowpass Butterworth Filter Obtained by Cascading 2 Sections in Mode 1a

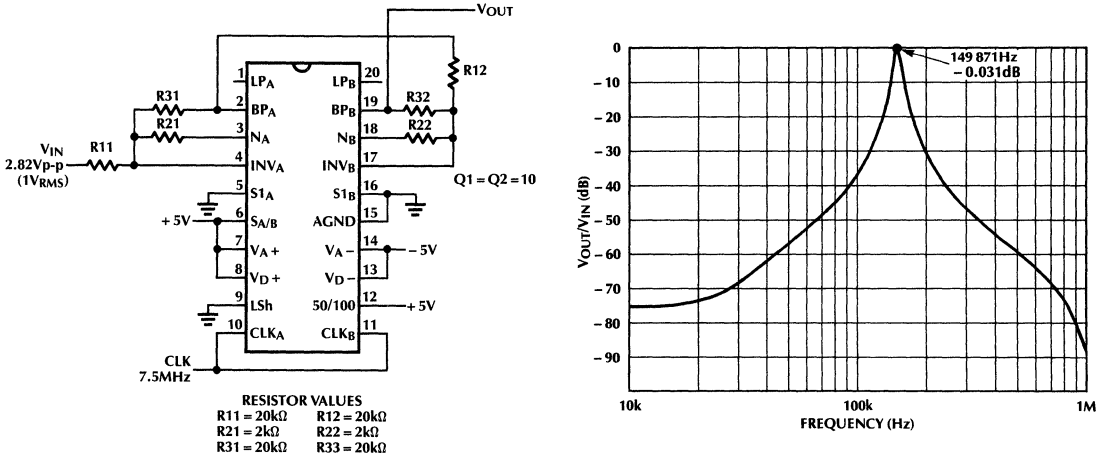


Figure 32. Cascading Two Sections in Mode 1, Each With Q = 10 Results in a Bandpass Filter with Q = 15.5 and f_o = 150kHz (f_{CLK} = 7.5MHz)

OPERATION MODES (Continued)

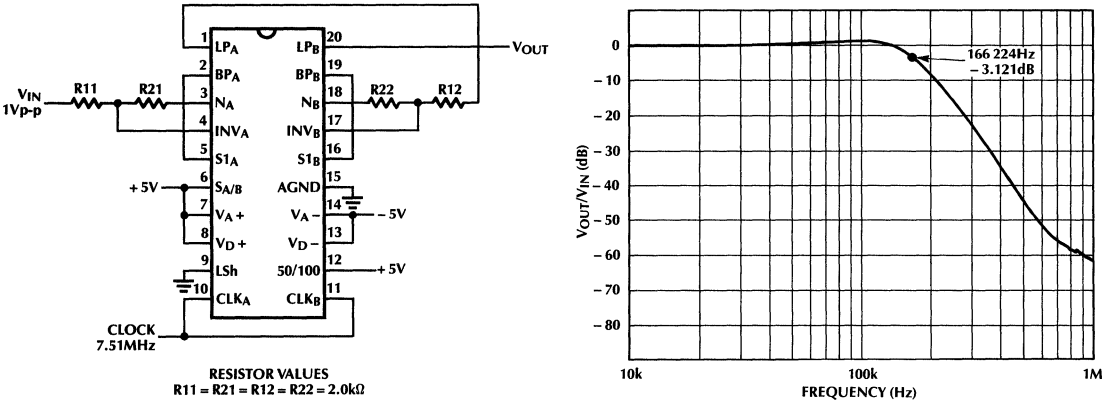


Figure 33. Cascading Two Sections in Mode 1d, Each With Q = 1 (Independent of Resistor Ratios) Creates a Sharper 4th Order Lowpass Filter

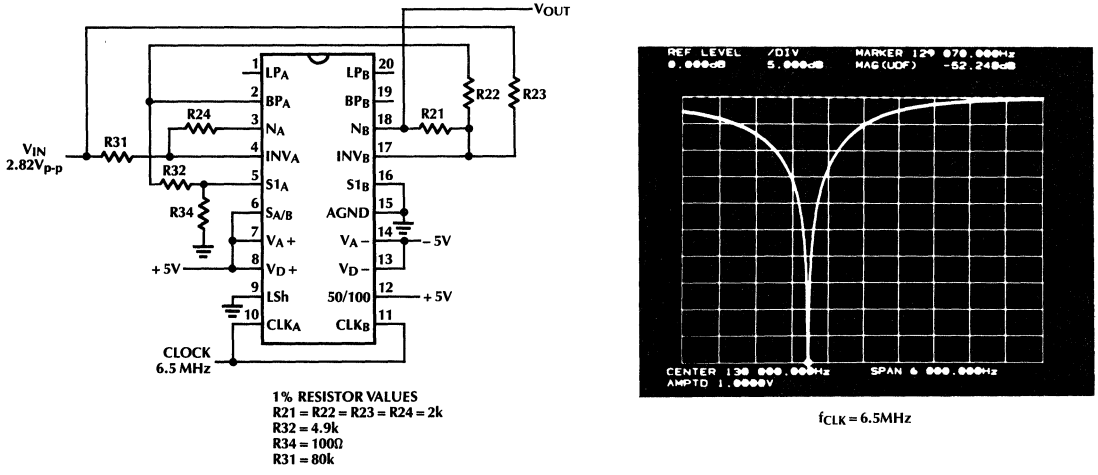


Figure 34. Notch Filter with Q = 50 and f_0 = 130kHz. This Circuit Uses Side A's Biquad in Mode 1d and the Side B Op Amp to Create a Notch Whose Depth is Controlled by R31. The Notch is Created by Subtracting the Bandpass from V_{IN}. The Bandpass of Side A is Subtracted Using the Op Amp of Side B.

OFFSETS

Switched capacitor integrators generally exhibit higher input offsets than discrete R, C integrators.

These offsets are mainly the charge injection of the CMOS switches into the integrating capacitors. The internal op amp offsets also add to the overall budget.

Figure 35 shows half of the ML2111 filter with its equivalent input offsets V_{OS1}, V_{OS2}, V_{OS3}.

The DC offset at the filter bandpass output is always equal to V_{OS3}. The DC offsets at the remaining two outputs (Notch and LP) depend on the mode of operation and external resistor ratios. Table 3 illustrates this.

It is important to know the value of the DC output offsets, especially when the filter handles input signals with large dynamic range. As a rule of thumb, the output DC offsets increase when:

1. The Q's decrease
2. The ratio (f_{CLK}/f_o) increases beyond 100:1. This is done by decreasing either the (R2/R4) or the R6/(R5 + R6) resistor ratios.

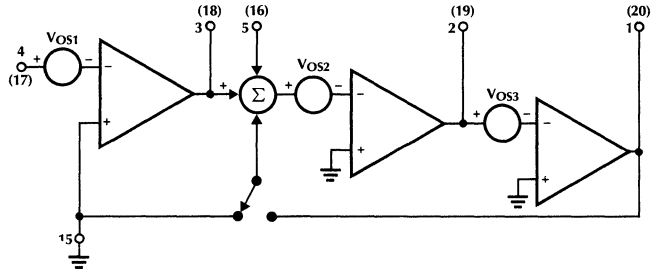


Figure 35. Equivalent Input Offsets of 1/2 ML2111 Filter

Table 3

MODE	V_{OSN} PIN 3 (18)	V_{OSBP} PIN 2 (19)	V_{OSLP} PIN 1 (20)
1,4	$V_{OS1}[(1/Q)+1+\lVert H_{OLP}\rVert]-V_{OS3}/Q$	V_{OS3}	$V_{OSN}-V_{OS2}$
1a	$V_{OS1}[1+(1/Q)]-V_{OS3}/Q$	V_{OS3}	$V_{OSN}-V_{OS2}$
1b	$V_{OS1}[(1/Q)+1+R2/R1]-V_{OS3}/Q$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})(1+R5/R6)$
1c	$V_{OS1}[(1/Q)+1+R2/R1]-V_{OS3}/Q$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})\frac{(R5+R6)}{(R5+2R6)}$
1d	$V_{OS1}[1+R2/R1]$	V_{OS3}	$V_{OSN}-V_{OS2}-V_{OS3}/Q$
2, 5	$[V_{OS1}(1+R2/R1+R2/R3+R2/R4)-V_{OS3}(R2/R3)]\times[R4/(R2+R4)]+V_{OS2}[R2/(R2+R4)]$	V_{OS3}	$V_{OSN}-V_{OS2}$
2a	$[V_{OS1}(1+R2/R1+R2/R3+R2/R4)-V_{OS3}(R2/R3)]\times\left[\frac{R4(1+k)}{R2+R4(1+k)}\right]+V_{OS2}\left[\frac{R2}{R2+R4(1+k)}\right];k=\frac{R6}{R5+R6}$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})\frac{(R5+R6)}{(R5+2R6)}$
2b	$[V_{OS1}(1+R2/R1+R2/R3+R2/R4)-V_{OS3}(R2/R3)]\times\left[\frac{R4k}{R2+R4k}\right]+V_{OS2}\left[\frac{R2}{R2+R4k}\right];k=\frac{R6}{R5+R6}$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})(1+R5/R6)$
3, 4a	V_{OS2}	V_{OS3}	$V_{OS1}\left[1+\frac{R4}{R1}+\frac{R4}{R2}+\frac{R4}{R3}\right]-V_{OS2}\left(\frac{R4}{R2}\right)-V_{OS3}\left(\frac{R4}{R3}\right)$

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML2111BCP	0°C to +70°C	MOLDED DIP (P20)
ML2111CCP	0°C to +70°C	MOLDED DIP (P20)
ML2111BCS	0°C to +70°C	MOLDED SOIC (S20W)
ML2111CCS	0°C to +70°C	MOLDED SOIC (S20W)
ML2111BIJ	-40°C to +85°C	HERMETIC DIP (J20)
ML2111CIJ	-40°C to +85°C	HERMETIC DIP (J20)

PART NUMBER	TEMP. RANGE	PACKAGE
ML2111BMJ	-55°C to +125°C	HERMETIC DIP (J20)
ML2111CMJ	-55°C to +125°C	HERMETIC DIP (J20)
ML2111BIP	-40°C to +85°C	MOLDED DIP (P20)
ML2111CIP	-40°C to +85°C	MOLDED DIP (P20)
ML2111BIS	-40°C to +85°C	MOLDED SOIC (S20W)
ML2111CIS	-40°C to +85°C	MOLDED SOIC (S20W)

Section 4

ETHERNET

Part Number	Description	LED Outputs	Autopolarity	Package Types
ML2652	10BASE-T Physical Layer with AUI Port	6	Yes	44 Pin PLCC
ML2653	10BASE-T Physical Layer	2	Yes	28 Pin PLCC
ML2653EVAL	Evaluation Kit for ML2653			
ML4642	AUI Multiplexer (2-port)	6	N/A	28 Pin SSOP
ML4644	AUI Multiplexer (4-port)	10	N/A	68 Pin PLCC
ML4652	10BASE-T MAU	6	No	24 Pin Skinny DIP 28 Pin PLCC
ML4658	10BASE-T MAU	6	Yes	24 Pin Skinny DIP 28 Pin PLCC
ML4662	10BASE-FL MAU (without Quantizer)	5	N/A	28 Pin PLCC
ML4662EVAL	Evaluation Kit for ML4662			
ML4663	10BASE-FL MAU (includes Quantizer)	5	N/A	28 Pin PLCC
ML4663EVAL	Evaluation Kit for ML4663			

High-Speed Networking

Part Number	Applications	Data Rate	Media Interface	Adaptive Equilization	Base Line Wander	Package Types
ML6671	FDDI over Copper (TP-PMD) Fast Ethernet (100BASE-TX)	125MHz	MLT-3	Yes	No	32 Pin PLCC 32 Pin TQFP
ML6671-22EVAL	Evaluation Kit for ML6671					
ML6672	ATM over Copper	155Mbps	NRZ	Yes	No	32 Pin PLCC 32 Pin TQFP
ML6672-9EVAL	Evaluation Kit for ML6672					
ML6673	FDDI over Copper (TP-PMD) Fast Ethernet (100BASE-TX)	125MHz	MLT-3	Yes	Yes	32 Pin PLCC 32 Pin TQFP

Token Ring Physical Interface

Part Number	Application	Data Rates	Cable Type	Package Type
ML6682	Station Concentrator	4 Mbps 16 Mbps	UTP STP	44 Pin TQFP

Fiber Optic Components

Part Number	Decription	Bandwidth	I/O Types	Package Types
ML4621	Quantizer	50 MHz	TTL, ECL	24 Pin Skinny DIP 28 Pin PLCC
ML4622	Quantizer	40 MHz	TTL, ECL	16 Pin Skinny DIP 16 Pin Narrow SOIC
ML4624	Quantizer	40 MHz	TTL, ECL	24 Pin Skinny DIP 28 Pin PLCC
ML4632	LED Driver	20 MHz	TTL, ECL	14 Pin DIP 16 Pin SOIC
ML6622	Quantizer	150 MHz	ECL	16 Pin DIP 16 Pin Narrow SOIC
ML6633	LED Driver	200 MHz	ECL	8 Pin DIP 8 Pin SOIC
ML6633/22EVAL	Evalutation Kit for ML6633 and ML6622			

Networking Interface Products

Part Number	Decription	Protocols	Data Rate	Package Types
ML4670	Multiple Protocol Physical Interface	RS-449, RS-232 V.35, X.21	10Mbps	84 Pin PLCC

ML2652/ML2653

10Base-T Physical Interface Chip

GENERAL DESCRIPTION

The ML2652, 10BASE-T Physical Interface Chip, is a complete physical interface for twisted pair and AUI Ethernet applications. It combines a 10BASE-T MAU, Manchester Encoder/Decoder, and Twisted Pair Interface filters in one monolithic IC. A complete DTE interface for twisted pair Ethernet can be implemented by combining the ML2652, an Ethernet controller, and transformers.

The ML2652 can automatically select between an AUI and twisted pair interface based on Link Pulses. Six LED outputs provide complete status at the physical link. Link and Test can be enabled or disabled through the LED outputs.

The unique transmitter design uses a waveform generator and low pass filter to meet the 10BASE-T transmitter requirements without the need for an external filter. The differential current driven output reduces common mode which in turn results in very low EMI and RFI noise.

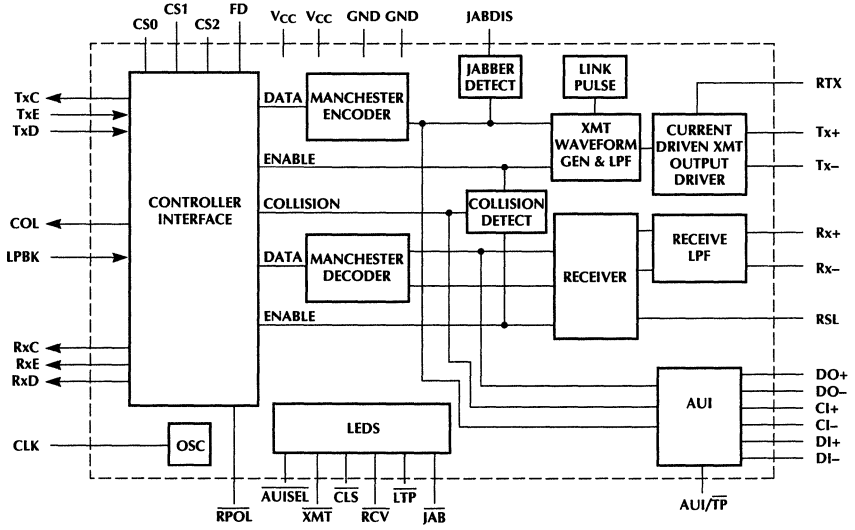
The ML2652 and ML2653 (28 pin version) is implemented in a low power double polysilicon CMOS technology. The ML2653 does not include the AUI interface.

FEATURES

- Complete physical interface solution
- Conforms to IEEE 802.3i–1990 (10Base-T)
- On-chip transmit and receive filters
- Automatic AUI/Twisted Pair selection (ML2652 only)
- Power down mode
- Pins selectable controller interface-(CS0 – CS2)
  - Intel 82586, 82596
  - NSC DP8390
  - Seeq 8003, 8005
  - AMD 7990
- Automatic polarity correction
- Pin selectable receive squelch levels
- Status pins for: link detect, receive & transmit activity, collision, jabber, AUI selection
- Single supply 5V ±5%
- ML2653 — 28 pin PLCC package
- ML2652 — 44 pin PLCC package (see page 2)

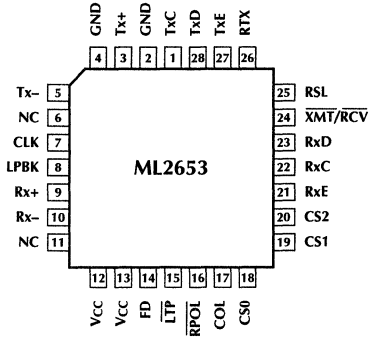
4

ML2652 BLOCK DIAGRAM

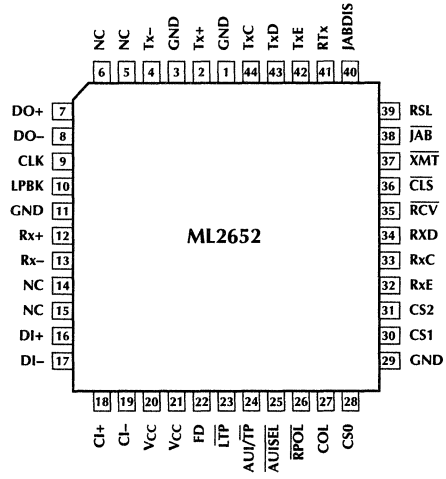


PIN CONNECTIONS

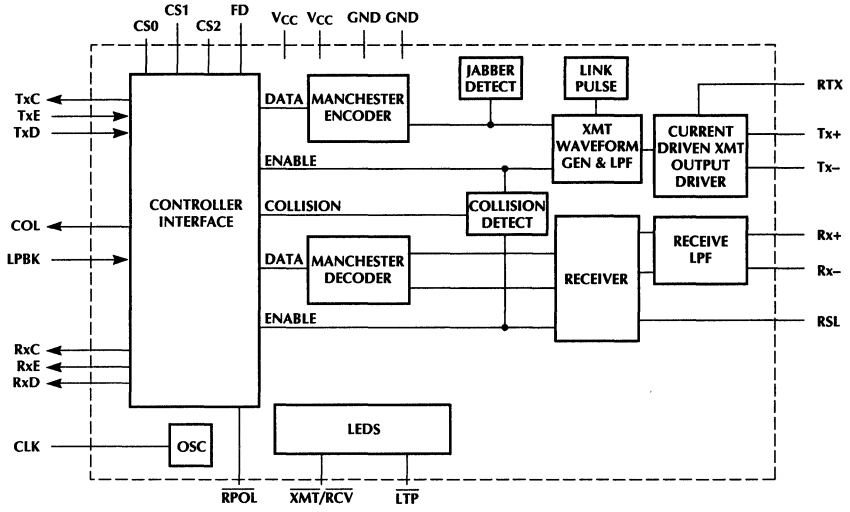
ML2652
44-Pin PLCC (Q44)



ML2653
28-Pin PLCC (Q28)



ML2653 BLOCK DIAGRAM



PIN DESCRIPTION

NAME	FUNCTION
VCC	Positive supply. +5V
GND	Ground. 0 volts. All inputs and outputs referenced to this point.
CLK	Clock input. There must be either a 20 MHz crystal or a 20 MHz clock between this pin and GND.
Tx+	Transmit positive twisted pair output. This output is a current source that drives the twisted pair cable through a pulse transformer.
Tx–	Transmit negative twisted pair output. This output is a current source that drives the twisted pair cable through a pulse transformer.
Rx+	Receive positive twisted pair input. This input receives data from the twisted pair cable through a pulse transformer.
Rx–	Receive negative twisted pair input. This input receives data from the twisted pair cable through a pulse transformer.
DO+	AUI positive transmit output. AUI transmit data output to optional external transceiver.
DO–	AUI negative transmit output. AUI transmit data output to optional external transceiver.
DI+	AUI positive receive data input from optional external transceiver.

NAME	FUNCTION
DI–	AUI negative receive data input from optional external transceiver.
CI+	AUI positive collision input from optional external transceiver.
CI–	AUI negative collision input from optional external transceiver.
RTX	Transmit current set. An external resistor between this pin and GND programs the absolute value of output current on Tx±.
TxC	Transmit clock output. Digital output which clocks the transmit data (TxD) into the device from the controller.
TxD	Transmit data input. Digital input which contains transmit data from the controller.
TxE	Transmit enable input. Digital input from the controller that indicates when the transmit data (TxD) is valid.
COL	Collision output Digital output to the controller which indicates when a collision condition is present.
RxC	Receive clock output. Digital output which clocks receive data (RxD) from the device into the controller.

PIN DESCRIPTION (Continued)

NAME	FUNCTION
RxD	Receive data output. Digital output which contains receive data sent to the controller.
RxE	Receive data valid. Digital output to the controller that indicates when the receive data (RxD) is valid.
LPBK	Local loopback. Digital input from the controller which forces the device to loopback transmit data without sending it on the media.
FD	Full Duplex Enable. When enabled the 10BASE-T MAU loopback and collision detect are disabled. LPBK must be disabled when using this function.
CS0	Controller selection input. Digital input which selects one of four standard controller timing interfaces. This pin has an internal pulldown resistor to GND.
CS1	Controller select input. Digital input which selects one of four standard controller timing interfaces. This pin has an internal pulldown resistor to GND.
CS2	Controller select input. Digital input which selects one of four standard controller timing interfaces. This pin has an internal pulldown resistor to GND.
RSL	Receive squelch level select input. Pin has internal pullup resistor to VCC. RSL = High Receive squelch level = 10Base-T RSL = Low Receive squelch level = extended distance
$\overline{XMT}$	Transmit status output. Digital output which indicates data transmission on Tx+ and Tx–. Pin is open drain output with resistor pullup and is capable of driving an LED. $\overline{XMT}$ pin and $\overline{RCV}$ pin are the same pin for ML4653.
$\overline{RCV}$	Receive status output. Digital output which indicates unsquelched data reception on Rx+ and Rx–. Pin is an open drain output with resistor pullup and is capable of driving an LED.
$\overline{CLS}$	Collision status output. Digital output which indicates that collision condition has been detected. Pin is an open drain output with resistor pullup and is capable of driving an LED.
$\overline{LTP}$	Link test pass output/input. This pin consists of an open drain output transistor with a resistor pullup that serves both as a link test pass output and a link test disable input. When used as an output, this pin is capable of driving an LED. $\overline{LTP}$ = High, link test failed $\overline{LTP}$ = Low, link test pass $\overline{LTP}$ = GND, link test disabled
AUI/$\overline{TP}$	AUI/twisted pair interface select input. AUI/$\overline{TP}$ = High, AUI selected AUI/$\overline{TP}$ = Low, TP selected
$\overline{RPOL}$	This pin must be grounded at all times.
$\overline{JAB}$	Jabber detect output. Digital output which indicates that the jabber condition has been detected. Pin is an open drain output with resister pullup and is capable of driving a LED. $\overline{JAB}$ = High, normal $\overline{JAB}$ = Low, jabber detected
$\overline{AUISEL}$	AUI/$\overline{TP}$ port output status $\overline{AUISEL}$ = High, TP port selected $\overline{AUISEL}$ = Low, AUI port selected
JABDIS	Jabber disable input JABDIS = High, jabber disabled JABDIS = Low, normal operation
NC	No connect. Leave this pin open circuit.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to GND. (Note 1)

VCC supply voltage ..... +6.5 volts
All inputs and outputs ..... –0.3v to VCC + .3v
Input current per pin ..... ±25 mA
Power dissipation ..... 0.75 Watt
Storage temperature range ..... –65°C to +150°C
Lead temperature (soldering, 10 sec) ..... 300°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified T_A = 0°C to 70°C, V_{CC} = 5V +5%. Note 2 & 3.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VIL	Digital input low voltage	All except CLK CLK			.8 1.5	V V
VIH	Digital input high voltage	All except CLK CLK	2.0 3.5			V V
IIL	Digital input low current	VIN=GND TxD, TxE, AUI/$\overline{TP}$ VIN=GND LPBK, CS2–0, LBDIS,JABDIS VIN=GND RSL VIN=GND $\overline{LTP}$, RPOL, VIN=GND CLK	 –10 –15	 –25 –250	–5 –5 –50 –500 –300	µA µA µA µA µA
IIH	Digital input high current	VIN=VCC TxD, TxE, AUI/$\overline{TP}$ VIN=VCC LPBK, CS2–0, LBDIS, JABDIS VIN=VCC RSL VIN=VCC $\overline{LTP}$, RPOL VIN=VCC CLK	 10	 25	1 50 1 1 250	µA µA µA µA µA
CIN	Digital input capacitance	All except CLK CLK		5 10		pF pF
VOL	Digital output low voltage	IOL=–2mA TxC, COL, RxC, RxD, RxE IOL=–10mA $\overline{XMT}$, $\overline{RCV}$, $\overline{CLS}$, $\overline{LTP}$, RPOL, $\overline{JAB}$			.4 .6	V V
VOH	Digital output high voltage	IOH=2mA TxC, COL, RxC, RxD, RxE IOL=10uA $\overline{XMT}$, $\overline{RCV}$, $\overline{CLS}$, $\overline{LTP}$, RPOL, $\overline{JAB}$	 4.0 2.4			 V V
ICC	VCC supply current	TX transmission No transmission Powerdown mode		 2	140 105	mA mA mA
TOV	Tx± differential output voltage	RTX = 10K	2.2	2.5	2.8	Vp
THD	Tx± harmonic distortion	TxD=all ones	–27			dB
TCM	Tx± common mode output voltage				± 50	mVp
TCMR	Tx± common mode rejection	VCM=15vp, 10.1 MHz sine		± 100		mVp
TOVI	Tx± differential output voltage during idle				± 50	mVp
TOIA	Tx± output current accuracy	RTX=10K		50		mA
TRO	Tx± output resistance			1		Mohm
TCO	Tx± output capacitance			10		pF
RRI	Receive input resistance		2.5K	10K		ohms
RCI	Receive input capacitance			10		pF
RSON	Receive squelch on level	RSL=1 RSL=0	275 150		520 325	mVp mVp

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RSOF	Receive squelch off level	RSL=1 RSL=0	150 100		325 225	mVp mVp
DOV	DO± differential output voltage		± 550		± 1170	mV
DOVI	DO± differential output voltage during idle				± 40	mV
DOUS	DO±differential output voltage return to 0 undershoot				–100	mV
DOCMA	DO± common mode AC output voltage				± 40	mV
DOCMA	DO± common mode DC output voltage			VCC *.5		V
DIRI	DI/CI input resistance		2.5K	10K		ohms
DICI	DI/CI input capacitance			10		pF
DIBV	DI/CI input bias voltage	DI/CI floating		VCC *.5		V
DISON	DI/CI squelch on level		–175		–325	mVp
t1	TxC on time		45		55	ns
t2	TxC off time		45		55	ns
t3	TxC period			100		ns
t4	TxE setup time		25			ns
t5	TxE hold time		0			ns
t6	TxD setup time		25			ns
t7	TxD hold time		0			ns
t8	Transmit propagation delay	Tx± DO±		60	200 200	ns ns
t9	Start of Idle Pulse Width	Tx± DO±	200		350	ns
t10	SOI pulse width to within 40mV of final value	Tx± DO±			4500 8000	ns ns
t11	Transmit output jitter	Tx± DO±			± 8.0 ± .5	ns ns
t12	Transmit output rise and fall time	Tx± , 10–90%		5		ns
t13	TxE to $\overline{\text{XMT}}$ assert				250	ms
t14	$\overline{\text{XMT}}$ blinker pulse period		95		115	ms

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t15	$\overline{XMT}$ duty cycle		45		55	%
t20	Start of receive packet to RxE assert	Rx± DI±			600 200	ns ns
t21	Start of receive packet to RxC active	Rx+ DI+			1600 1300	ns ns
t22	RxC on time		45		900	ns
t23	RxC off time		45		55	ns
t24	RxD valid before RxC		45			ns
t25	RxD valid after RxC		35			ns
t26	RxE assert to $\overline{RCV}$ assert				250	ms
t27	$\overline{RCV}$ blinker pulse period		95		115	ms
t28	$\overline{RCV}$ duty cycle		45		55	%
t29	Receive input jitter	Preamble Data			± 12 ± 18	ns ns
t30	Receive propagation delay	Tx± DI±			160 160	ns ns
t31	RxC to RxE assert		30		60	ns
t32	RxC to RxE deassert		20		45	ns
t33	RxE deassert to RxC switchover		100		200	ns
t34	Minimum SOI pulse width required for receive detection	Tx± DI±	180 180			ns ns
t40	Jabber activation delay- TxE assert to Tx± disable		20		150	ms
t41	Tx± disable to $\overline{JAB}$ assert			200		ms
t42	Jabber reset time – TxE deassert to $\overline{JAB}$ deassert		250		750	ms
t43	Tx± disable to COL assert			50		ns
t44	Tx± disable to $\overline{CLS}$ assert			50		ns
t45	$\overline{JAB}$ deassert to COL deassert				50	ns
t46	$\overline{JAB}$ deassert to $\overline{CLS}$ deassert				50	ns
t51	Transmit link pulse period		8		24	ms
t52	Minimum link pulse period required for receive detection		2		7	ms
t52	Maximum link pulse period required for receive detection		25		150	ms
t53	Receive link pulse no detect to $\overline{LTP}$ deassert		50		150	ms

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t54	Receive link pulse detect to $\overline{LTP}$ assert		2			Link Pulse
t55	AUI/$\overline{TP}$ to $\overline{AUISEL}$ delay				200	ns
t60	TxE deassert to COL assert		.9	1.0	1.1	µs
t61	COL pulse Width		.9	1.0	1.1	µs
t70	Start of $\overline{RCV}$ packet during transmission to COL assert	Rx±			500	ns
t71	Start of $\overline{RCV}$ packet during transmission to $\overline{CLS}$ assert	Rx±			500	ns
t72	End of $\overline{RCV}$ packet during transmission to COL deassert	Rx±			300	ns
t73	$\overline{CLS}$ blinker pulse period		95		115	ms
t74	$\overline{CLS}$ duty cycle		45		55	%
t75	Transmission start during reception to COL assert	Tx±			300	ns
t76	Transmission start during reception to $\overline{CLS}$ assert	Tx±			250	ms
t77	CI± period		80		120	ns
t78	CI± duty cycle		40		60	%
t79	First valid negative CI± data transition to COL assert				100	ns
t80	First valid negative CI± data transition to $\overline{CLS}$ assert				100	ns
t81	Last CI± positive data transition to COL deassert		160		250	ns
t82	External clock input jitter				50	ps

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 3: Low Duty cycle pulse testing is performed at T_A.

TIMING DIAGRAMS

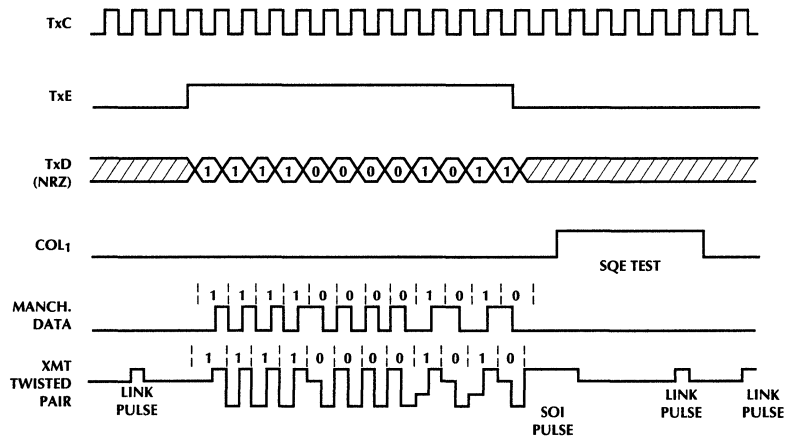


Figure 1. Transmit System Timing

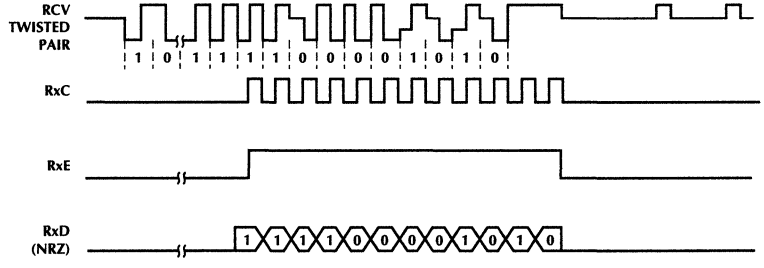


Figure 2. Receive Timing

TIMING DIAGRAMS

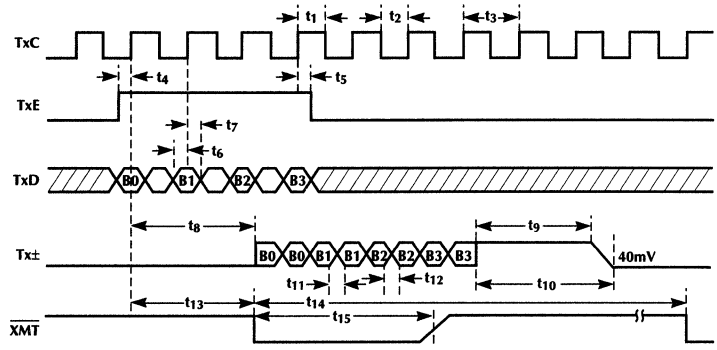
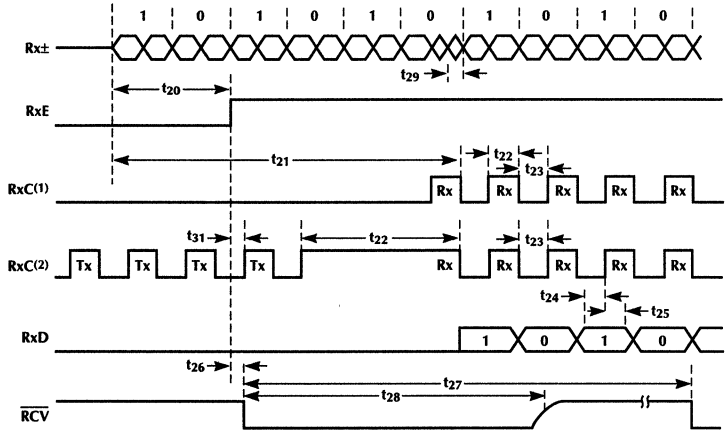


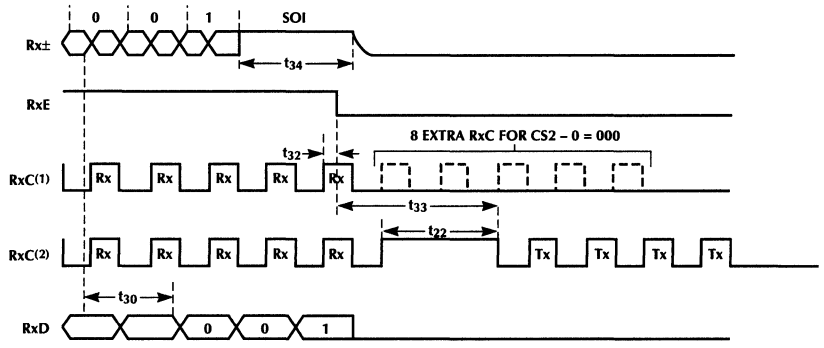
Figure 3. Transmit Timing



NOTE:
1. RxC IS NOT CONTINUOUS DURING IDLE
2. RxC IS CONTINUOUS DURING IDLE

Figure 4. Receive Timing – Start of Frame

TIMING DIAGRAMS



NOTE:
1. RxC IS NOT CONTINUOUS DURING IDLE — 8 EXTRA CLOCKS ADDED FOR CS2 – 0 = 000
2. RxC IS CONTINUOUS DURING IDLE

Figure 5. Receive Timing – End of Frame

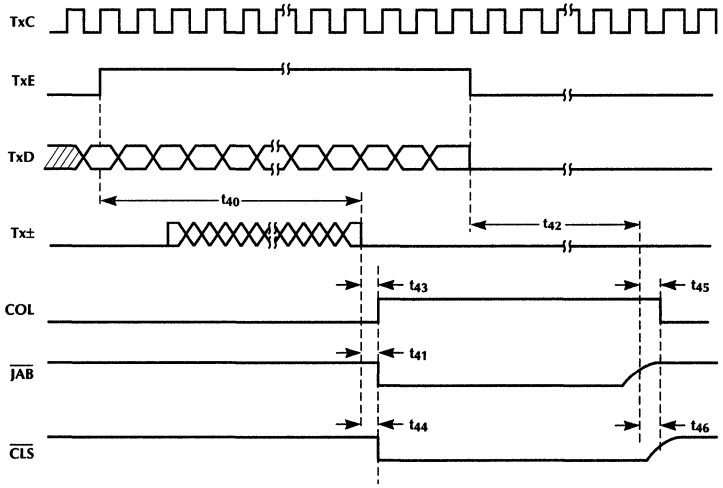


Figure 6. Jabber Timing (ML2652 only.)

TIMING DIAGRAMS

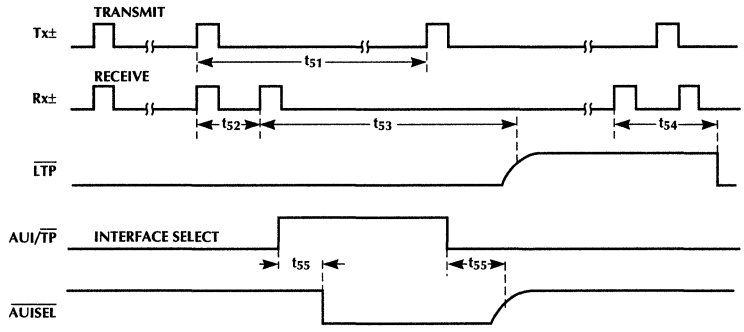


Figure 7. Link Pulse Timing

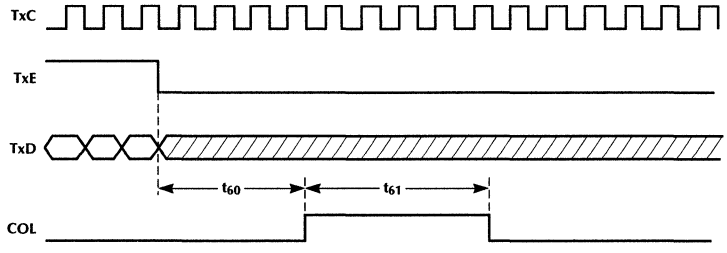


Figure 8. SQE Test Timing

TIMING DIAGRAMS

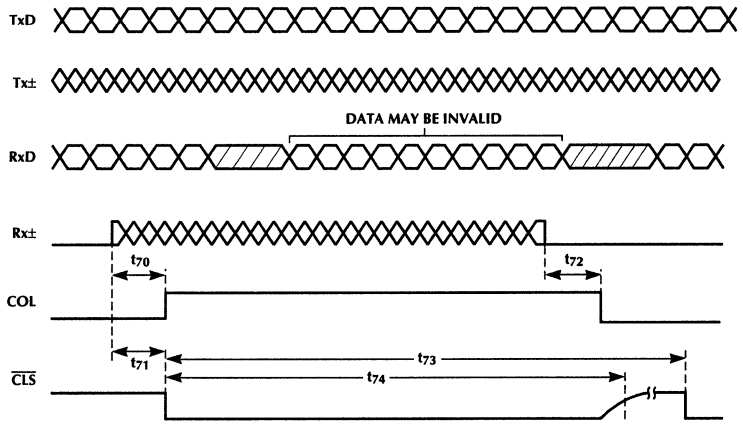


Figure 9. Collision Timing Reception During Transmission

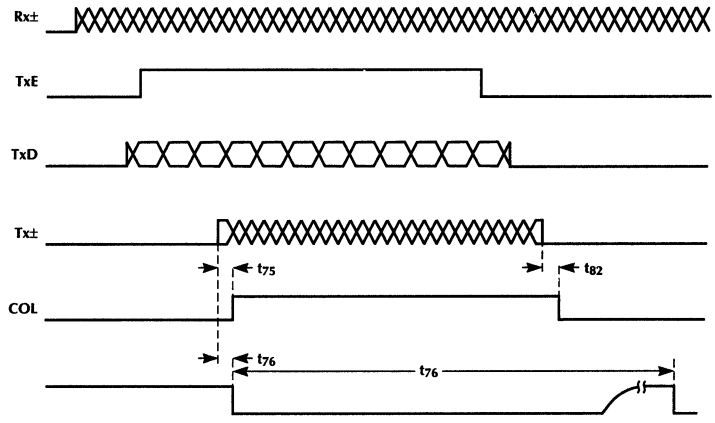


Figure 10. Collision Timing Transmission During Reception

TIMING DIAGRAMS

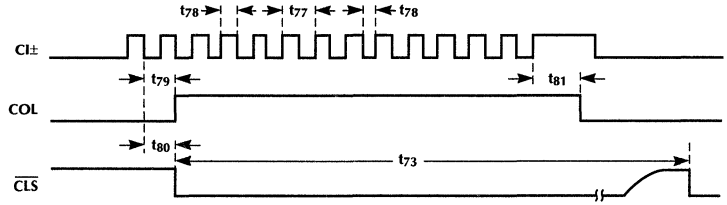


Figure 11. CI± Collision

APPLICATION CIRCUIT — ML2652

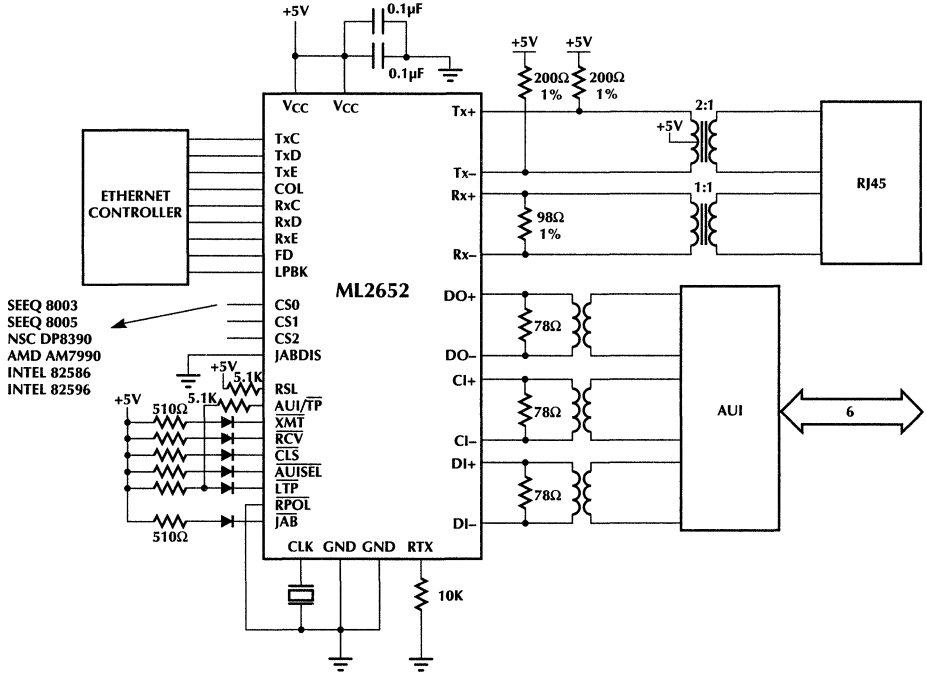


Figure 12

FUNCTIONAL DESCRIPTION

GENERAL

The ML2652 and ML2653 are composed of a transmitter section, receive section and some miscellaneous functions.

The transmit section consists of the manchester encoder, AUI, jabber detect, link pulse generator, start of idle (SOI) pulse generator, waveform generator, and line driver. The purpose of the transmit section is to take data from the controller, encode it, and transmit it over either the AUI or twisted pair interface. In addition, the transmit section generates link pulses, start of idle pulses, and checks for jabber condition. The transmitter keeps the data jitter to a maximum of ±8.0ns, and the maximum delay through the transmission section is less than 2 bits, or 200ns.

The receive section consists of the manchester decoder, collision detect, AUI, receive LPF, receive comparators, receive squelch, automatic polarity correct, start of idle (SOI) detect, and link pulse detect. The purpose of the receive section is to take data from either the twisted pair cable or AUI, decode it, then send the data to the controller via the controller interface. In addition, the receive section detects and automatically corrects for reverse polarity, detects link pulses, detects start of idle pulses, and implements an intelligent receive squelch algorithm. The receive section can successfully lock onto an incoming data that contains ±18ns of jitter in less than 1.6µs.

APPLICATION CIRCUIT — ML2653

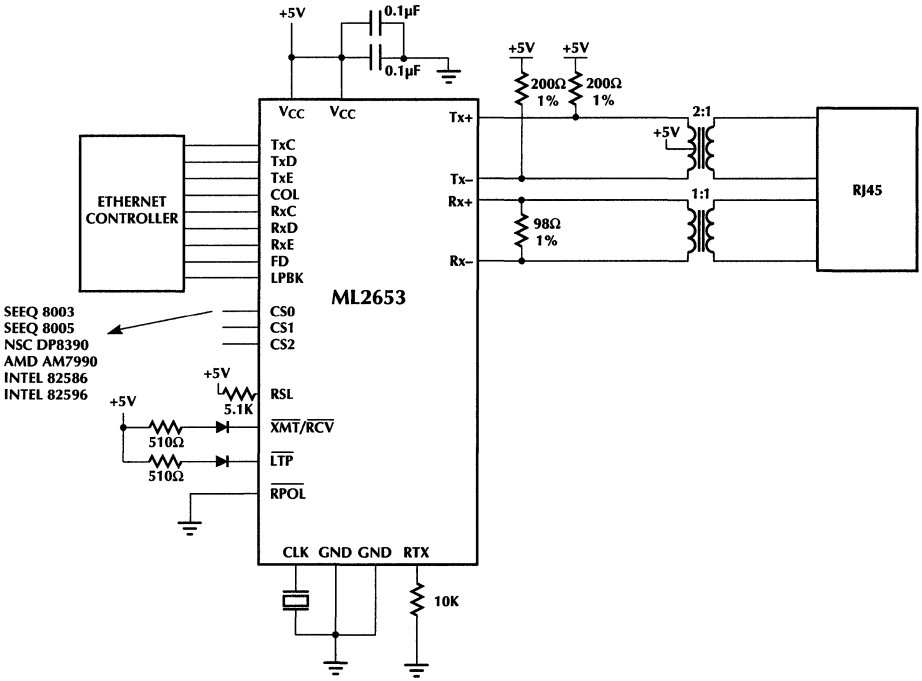


Figure 13

The miscellaneous functions are the controller interface, single pin crystal oscillator, AUI, loopback modes, test mode, and powerdown mode. The ML2653 has no AUI interface output.

The following text describes each of these blocks and functions in more detail. Refer to the block diagram.

TRANSMISSION

The transmit data (NRZ) is first clocked into the device through the controller interface. The device can be digitally programmed to accommodate any one of four standard Ethernet controllers as described in Controller section.

Then the NRZ data is encoded by the manchester encoder as shown in transmit timing diagram in Figure 1.

The manchester encoded data then goes to either the AUI or twisted pair interface. The selection of the appropriate interface is automatic. If the AUI is selected, the manchester encoded data is transmitted out differentially on the DO+ and DO– pins, and the twisted pair line driver is disabled. If the twisted pair interface is selected, the manchester encoded data is transmitted out differentially on Tx+ and Tx– pins, and the transmit AUI is disabled.

Refer to the AUI section for details on how the AUI and automatic interface selection is accomplished.

Assuming that the twisted pair interface is selected, the Manchester encoded data then goes to the transmit waveform generator. The transmit waveform generator takes the digital Manchester encoded data and generates a waveform. When this waveform is passed through the cable model in the 10BASE-T standard (figure 14–7 IEEE Std 802.3i–1990) it meets the voltage template (figure 14–9 IEEE Std 802.3i–1990).

The transmit waveform generator is composed of a 16 x 4 bit ROM, 4 bit DAC, 3rd order LPF, and clock generator. The DAC is used to synthesize a stair-step representation of a signal that will meet the required output template. The ROM stores the digital representation of the output signal and provides a digital input to the DAC. The ROM is addressed by a 16 phase clock generator that is locked to the transmit clock TxC. The high frequency content present in the output of the DAC is removed by a 3rd order continuous LPF which smooths the output.

The transmit line driver takes the output of the waveform generator and converts this voltage to a differential output current on Tx+ and Tx– pins. When one transmit output (either Tx+ or Tx–) is sinking current, the other output is high impedance, and vice versa. In this way, a differential output voltage is developed by sinking this output current through two external 200 ohm terminating resistor and a 2:1 transformer as shown in Figure 12.

Setting the external terminating resistors to 200 ohms as shown in Figure 12 will implement a 100 ohm terminating impedance when looking back through the transformer. If other terminating impedances are required (such as 150 ohm), the terminating resistor values can be adjusted accordingly as long as the output current stays within the minimum and maximum limits (30–70mA).

The absolute value of the output current, and subsequently the output voltage level, is set by an external resistor between RTX and GND. If RTX = 10k ohms and Tx± is terminated as shown in Figure 12, the output level is ±2.5V which meets 802.3i–1990 differential output voltage requirements. If a different output current/voltage level is desired, the level can be changed by changing the value of RTX according to the following formula:

$$RTX = K*Vb/Iout$$

$$= 125*4v/50mA$$

$$RTX = 10k\Omega$$

When data is being transmitted (and there is no collision or link pulse fail condition), the transmit data is looped back to the receive path, and the Manchester decoder will lock onto the transmit data stream.

After data transmission is completed, the transmitter sends a start of idle (SOI) pulse to signal the end of a packet. During the idle period, Tx+ and Tx– are held low. Occasionally, link pulses are transmitted during the idle period.

The $\overline{XMT}$ pin is an output that indicates transmit activity. The pin consists of an open drain output with an internal pull-up resistor and can drive an LED from VCC or another digital input. In order to make an LED visible, $\overline{XMT}$ has an internal blinker circuit that generates a 100ms blink (50ms high, 50ms low) that is triggered when a trans-mission starts. At the completion of the 100ms blink period, if a transmission is in progress, another 100ms blink is generated.

RECEPTION

The twisted pair receive data is typically transformer coupled and terminated with an external resistor as shown in Figure 12.

The output of the transformer is then applied to the device input pins Rx+ and Rx–. The input is differential, and the common mode input voltage is biased to VCC/2 by two internal 10K bias resistors from Rx+, Rx– to VCC/2.

The Rx+ and Rx– inputs then go to the receive filter. The receive filter is a continuous 3rd order LPF and has the following characteristics:

1. 3 dB cut-off frequency	15 MHz
2. Insertion Loss (5–10 MHz)	≤ 1.0 dB
3. 30 MHz attenuation	17.5 dB min.

The output of the filter goes to the receive comparators. There are two receive comparators inside the chip, threshold and zero crossing. The threshold comparator determines if the receive data is valid by checking the input signal level against a predetermined positive and negative squelch level. Once the threshold comparator determines that valid data is being received, the zero crossing comparator senses zero crossings to determine data transitions. Both comparators are fast enough to respond to 12ns pulse widths with minimum squelch overdrive.

The receive squelch circuit determines when data on incoming Rx+, Rx– is valid. The receive squelch is considered "on" when the data is deemed to be invalid, and the receive squelch is considered "off" when data is determined to be valid.

The input signal must meet the following criteria in order to turn receive squelch off and be recognized as valid data:

1. The input signal must exceed the receive squelch on level. When this occurs, a 400ns squelch interval timer is started.

2. During the 400ns squelch interval, the input signal must go from one squelch threshold to the opposite polarity squelch threshold in less than 127ns.

3. During the 400ns squelch interval, the input signal has to make less than 9 squelch threshold to opposite polarity squelch threshold crossings.

When the receive squelch is turned off, the receive squelch off level is reduced to 2/3 of receive squelch on level.

The receive squelch will be turned back on if either the incoming data peaks go below the receive squelch off level for 400ns or the start of idle (SOI) pulse is detected.

The receive squelch on level can be digitally programmed for one of two possible levels by using the RSL pin. When RSL = 1, the squelch on level complies with the IEEE 802.3i–1990 specification. When RSL = 0, the receive squelch on level is lowered in order to accommodate greater receive attenuation and consequently longer twisted pair cable lengths. The receive squelch on level can be programmed as follows:

	Receive Squelch On Level			
RSL	**Application**	**Min**	**Typ**	**Max**
1	10BASE-T	300		585mV
0	Long Distance	200		390mV

The $\overline{RCV}$ pin is an output that indicates receive activity. The pin consists of an open drain output with an internal pull-up resistor and can drive an LED from VCC or another digital input. In order to make an LED visible, $\overline{RCV}$ has an internal blinker circuit that generates a 100ms blink (50ms high, 50ms low) that is triggered when reception starts. At the completion of the 100ms blink period, if reception is in progress, another 100ms blink is generated.

The manchester decoder receives data from either the twisted pair interface (as described above) or the AUI (described in AUI section).

The manchester decoder is responsible for recovering clock and data from the incoming receive bit stream. Clock and data recovery is accomplished by a digital PLL which can lock on the incoming bit stream in less than 1.6µs.

The clock (RxC) and NRZ data (RxD) are then output to the external world via the controller interface.

SOI

A start of idle (SOI) pulse is sent at the end of transmission in order to signal to all receivers that transmission has ended and the idle period begins. Thus, the transmit section has an SOI generator and the receive section has an SOI detector.

The transmit SOI pulse generator inserts an SOI pulse at the end of each transmission. The SOI pulse is typically a 250ns positive pulse inserted after the last positive data transition. Depending on the data pattern, the positive data transition could occur either in the middle or at the end of the last bit cell. So the actual width of the transmitted SOI pulse can vary from 250–300ns, typically.

The receive SOI detector senses the SOI pulse using the zero crossing comparator. When the SOI pulse is detected, the receiver signals to the controller that receive data is no longer valid and turns the receive squelch on.

LINK PULSE

During the idle period, link pulses are sent by the transmitter and detected by the receiver so that the integrity of the twisted pair link can be continuously monitored. Thus, the transmit section has a link pulse generator, and the receiver has a link pulse detector.

The transmit link pulse generator transmits a 100ns wide positive pulse (Tx+ high, Tx– low) every 16 ±8ms.

IEEE 802.3i–1990 Section 14 requires the link pulse to be shaped to meet a template when passed or not passed through the twisted pair line model. The transmit waveform generator takes the link pulse and generates the waveform on TX± when passed or not passed through the twisted pair line model.

The receiver monitors the receive input to determine if the link pulses are present. When the device is in the link pulse pass state, normal packet transmission and reception can occur. All link pulses less than 2–7ms apart are ignored while in the link pass state. If no link pulses or receive packets are detected for a period of 50–150ms, the device goes into the link pulse fail state.

When the device is in the link pulse fail state, reception is inhibited and the transmitter is placed in the idle state (no data transmission but link pulses are still transmitted). In order for the device to exit the link pulse fail state, one complete packet or 4 consecutive link pulses must be detected, and transmit and receive must be idle. Consecutive link pulses are defined as pulses that occur within 25–150ms of each other. If the link pulses occur 2–7ms apart in the link fail state, the device ignores the link pulses and resets the number of consecutive link pulses to zero. After the link pulse fail state is exited, transmission and reception can be resumed.

Link pulse status is indicated by the $\overline{LTP}$ pin. $\overline{LTP}$ is a dual function input/output pin that acts both as an active low link test pass output and a link test disable input. The pin consists of an open drain output with an internal pull-up resistor. If the pin is tied to GND, the pin acts as an input and the link test function is disabled. If the pin is not tied to GND, the pin acts as an active low link test pass output and can drive an LED from VCC or another digital output. Thus, the LED is lit when the link test is passing.

JABBER

The transmit section contains a jabber detect circuit. Jabber is a fault condition characterized by a babbling transmitter. The ML2652 and ML2653 detect jabber when a transmission packet exceeds 20–150ms in length. If jabber detect occurs, the transmit output is disabled, the collision signal COL is sent over the controller interface, and the $\overline{JAB}$ pin is pulled low. The device remains in the jabber detect state until there is at least 250–750ms of continuous non-transmission. Note that link pulses continue to be transmitted even when the device is in the jabber condition.

The jabber detection circuitry can be disabled (only on the ML2652) with the JABDIS pin for testing and diagnostic purposes. Disabling jabber means that a jabber condition is never recognized, even when it occurs. JABDIS is an active high jabber disable input and has an internal pull-down resistor to GND.

COLLISION

Collision occurs whenever the DTE card is transmitting and receiving data simultaneously. However, the collision circuit on the ML2652 operates differently depending on whether twisted pair interface or AUI is being used.

When the twisted pair interface is used, collision occurs whenever the device is transmitting and receiving data simultaneously, that is when both RxE and TxE are active. The collision state is indicated by COL and $\overline{CLS}$ pins. COL is used to signal collision to the controller. $\overline{CLS}$ is an active low open drain output. $\overline{CLS}$ is activated during Jabber, but not during SQE test while COL is activated during both.

When the AUI is used (ML2652 only), collision is no longer detected from simultaneous transmission and reception, but the collision state is determined when a collision signal is present on the AUI collision inputs, CI+ and CI–. A 10 MHz square wave has to be applied to this input in order for the device to signal the collision state on COL and $\overline{CLS}$.

The $\overline{CLS}$ pin is an output that indicates collision activity. The pin consists of an open drain output with an internal pull-up resistor and can drive an LED from VCC or another digital input. In order to make an LED visible, $\overline{CLS}$ has an internal blinker circuit that generates a 100ms blink (50ms high, 50ms low) that is triggered when a collision starts. At the completion of the 100ms blink period, if collision is in progress, another 100ms blink is generated.

SQE TEST

When the twisted pair interface is used, the device tests the collision circuitry at the end of each transmission by sending a 1µs collision pulse over the COL pin. This is known as SQE (signal quality error) test and is shown in the transmit timing diagram in Figure 1. The SQE test is disabled if the device is in jabber detect state or link pulse fail condition.

When AUI is used (ML2652), the SQE test pulse is generated by an external MAU and the external MAU sends the SQE test pulse to the ML2652 via the collision inputs , CI+ and CI–. The ML2652 then relays the collision signal to the controller via the COL and $\overline{CLS}$ output pins.

RECEIVE POLARITY DETECT AND AUTO CORRECTION

The ML2652 and ML2653 contain an auto-polarity circuit that detects the polarity of the receive twisted pair leads, Rx+ and RX-and internally reverses the leads if their polarity is incorrect.

When the device is powered up, it is assumed that the polarity is correct and no polarity correction occurs. Then receive polarity is continuously monitored by checking the polarity of the SOI and link pulses since they are always positive pulses. If either 2 consecutive SOI or 4 consecutive link pulses have incorrect RX± polarity, then the auto-polarity circuit internally reverses the Rx+ and Rx– connections.

AUI (APPLIES ONLY TO ML2652)

The ML2652 can be used with an external MAU via the Attachment Unit Interface (AUI). When the AUI is used, the internal MAU functions and twisted pair interface are disabled, and the device only uses the manchester encoder and decoder functions, as shown in the block diagram. The AUI consists of three differential signal pairs: DI, DO, and CI. The function of each pair is described below.

The DO+ and DO– are differential outputs to the external MAU which contain the transmit data output from the Manchester encoder. The DO+ and DO– output drivers are capable of driving 50 meters of 78 ohm cable with less than 5ns rise and fall time and less than ±0.5ns of jitter. In addition, at the end of transmission, the AUI output driver inserts a 200ns minimum pulse and meets the turnoff and idle characteristics specified in IEEE 802.3–1988. An external 78 ohm resistor across DO+ and DO– is required as shown in Figure 12 to develop the proper output levels from the internal current sources. The DO+ and DO– outputs can be coupled to an external MAU with either capacitors or a transformer. The ML2652 meets all AUI transmitter specifications outlined in IEEE 802.3–1988 Section 7.

DI+ and DI– are inputs from the external MAU which contain the receive data that goes to the manchester decoder.

The DI+ and DI– inputs contain an AUI DI squelch circuit which determines when incoming data on DI+ and DI– is valid. The DI squelch is considered "on" when the data is deemed to be invalid, and the DI squelch is considered "off" when data is determined to be valid.

The input signal on DI+ and DI– must meet the following criteria in order to turn receive squelch off and be recognized as valid data:

1. The input signal must exceed the negative AUI DI squelch on level.

2. The input signal must exceed the negative AUI DI squelch on level for more than 20ns.

When the DI squelch is turned off, the DI squelch off level is reduced to 2/3 of the DI squelch on level.

The DI squelch circuit will be turned back on if the idle period is detected by no DI squelch level transitions for more than 180ns.

An external 78 ohm termination resistor is needed across DI+ and DI– as shown in Figure 12. The DI+ and DI– inputs can be coupled from an external MAU into the ML2652 with either capacitors or a transformer. The ML2652 meets all AUI receiver specifications outlined in IEEE 802.3–1988 Section 7.

CI+ and CI– are inputs from the external MAU which contain the 10 MHz ± 15% collision signal as defined in IEEE 802.3–1988 Section 7. The CI+ and CI– inputs contain the same squelch circuit used on the DI inputs described in previous paragraphs in this section.

An external 78 ohm termination resistor is needed across CI+ and CI– as shown in Figure 12. The CI+ and CI– inputs can be coupled from an external MAU into the ML2652 with either capacitors (shown in Figure 12) or a transformer. The ML2652 meets all AUI receiver specifications outlined in IEEE 802.3–1988 Section 7.

The ML2652 contains an AUI/$\overline{\text{TP}}$ select input pin which controls whether the AUI or twisted pair interface is to be used for data transmission and reception. When AUI/Twisted Pair Switching = High, the AUI is used for data transmission and reception. When AUI/Twisted Pair Switching = Low, the twisted pair interface is used for data transmission and reception.

The $\overline{\text{AUISEL}}$ pin is a digital status output that indicates which interface has been selected for data transfer, either twisted pair or AUI. The pin consists of an open drain output with an internal pull-up resistor and can drive an LED from VCC or another digital input. $\overline{\text{AUISEL}}$ = High indicates that the twisted pair interface has been selected. $\overline{\text{AUISEL}}$ = Low indicates that the AUI interface has been selected.

The ML2652 has the capability to automatically select between the twisted pair interface and AUI. This automatic interface selection is accomplished by tying the $\overline{\text{LTP}}$ output pin to the AUI/$\overline{\text{TP}}$ input pin. When these two pins are connected together, if valid link pulses are detected, it is assumed that the twisted pair interface is being used. This causes $\overline{\text{LTP}}$ output to go low, thus forcing AUI/$\overline{\text{TP}}$ low, and thus enabling the twisted pair interface. If no valid link pulses are detected, it is assumed that the twisted pair interface is not being used, thus causing $\overline{\text{LTP}}$ to go high, thus forcing AUI/$\overline{\text{TP}}$ high, thus enabling the AUI interface. If valid link pulses reappear, the device will automatically disable the AUI and enable the twisted pair interface. The algorithm for determining valid link pulses is described in the Link Pulse section.

LOOPBACK

LPBK provides a loopback through the manchester encoder/decoder, but not through the on-chip 10BASE-T MAU. No data will go out on either the AUI port or the twisted pair port in this mode. This same function is found on many discrete manchester encoder/decoders.

IEEE 802.3 MAUs normally loop the transmit data (DO+) when transmitting with no collisions. When using an external transceiver through the ML2652's AUI port, the controller can first check the local loopback by setting LPBK. If it passes this test it can then check the AUI cable and external MAU by doing the normal MAU loopback.

FULL DUPLEX OPERATION

The ML2652 and ML2653 are capable of operating in the full duplex mode which transmits and receives data simultaneously. In the full duplex mode the collision circuitry is disabled just as it is in the loopback mode. To achieve full duplex operation the full duplex pin FD is enabled and the loopback pin LPBK must be disabled. Both of these conditions must be present to operate in the full duplex mode.

CONTROLLER INTERFACE

The ML2652 and ML2653 has a flexible and programmable digital interface which enables it to directly interface to Ethernet controllers manufactured by Intel, AMD, National and Seeq.

The controller interface consists of seven pins. TxC, TxD, and TxE are the transmit clock output, transmit data input, and transmit data enable input, respectively. RxC, RxD, and RxE are the receive clock output, receive data output, and receive data enable output, respectively. COL is the collision detect output.

All the standard Ethernet controllers use a similar controller interface but differ in the polarity of COL, LPBK, TxE and RxE, and in what edge of TxC and RxC that clocks in the data. They also differ on whether the RxC clock needs to be continuous or not during idle, and on the polarity of RxD during idle. In order to accommodate the different controller interface definitions, the controller select pins, CS2–0, modify these signals according to Table 1.

POWERDOWN

The device can be placed in the power down mode with the controller select pins CS2–0 as described in Table 1. When in powerdown mode, the current consumption is reduced to less than 100µA and all device functions are disabled.

CRYSTAL OSCILLATOR

The ML2652 requires an accurate 20 MHz reference for internal clock generation. This can be achieved by connecting an external crystal or an external clock between the CLK and GND pins.

If an external clock is used, it must have a frequency of 20 MHz ±0.01% and have high and low levels of 3.5 and 1.5 volts.

If a crystal is used, the crystal should be placed physically as close as possible to the CLK and GND pins, especially CLK. No other external capacitors or components are required. The crystal should have the following characteristics:

1. Parallel resonant type
2. Frequency: 20 MHz
3. Tolerance: ±0.005% @ 25°C
4. Less than 0.005% frequency drift across temperature.
5. Maximum equiv. series resistance:
   15 ohms @ 1–200µW
   30 ohms @ 0.01–1µW
6. Typical load capacitance: 20pF
7. Maximum case capacitance: 5pF

Table 1. Controller Select Pin Definitions

CS2–0	TxC	TxE	RxC	RxE	COL	LPBK	Idl RxC	Idl RxD	Controller	
0 0 0	r	h	r	h	h	h	m	l	NSC	DP8390
0 0 1	f	l	f	l	l	l	n	hi	Intel	82586/96
0 1 0	r	h	r	h	h	h	n	hi	AMD	AM7990
0 1 1	f	h	r	h	h	l	c	lo	Seeq	8003/5
1 0 0	—	—	—	—	—	—	—	—	—	
1 0 1	—	—	—	—	—	—	—	—	—	
1 1 0	—	—	—	—	—	—	—	—	—	
1 1 1	—	—	—	—	—	—	—	—	PDN mode	

r = rising edge clocks data
f = falling edge clocks data
h = active high
l = active low
c = RxC required continuously
n = RxC only during RxD transmission
m = RxC only during RxD transmission + 5 extra RxC cycles

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2652CQ	0°C TO +70°C	44-Pin Molded Leaded PCC (Q44)
ML2653CQ	0°C TO +70°C	28-Pin Molded Leaded PCC (Q28)

ML2653EVAL

10BASE-T Transceiver Evaluation Kit

GENERAL DESCRIPTION

The ML2653EVAL evaluation board is an internal 10BASE-T transceiver which can interface to either National or AMD's Ethernet controller. The ML2653 contains an encoder/decoder (ENDEC), media access unit (MAU), and filter. The ML2653 interfaces to the twisted pair media through an isolation transformer. This evaluation board can interface to the Ethernet LAN controller by plugging it's 24-pin socket into the manchester encoder/decoder (ENDEC) socket.

FEATURES

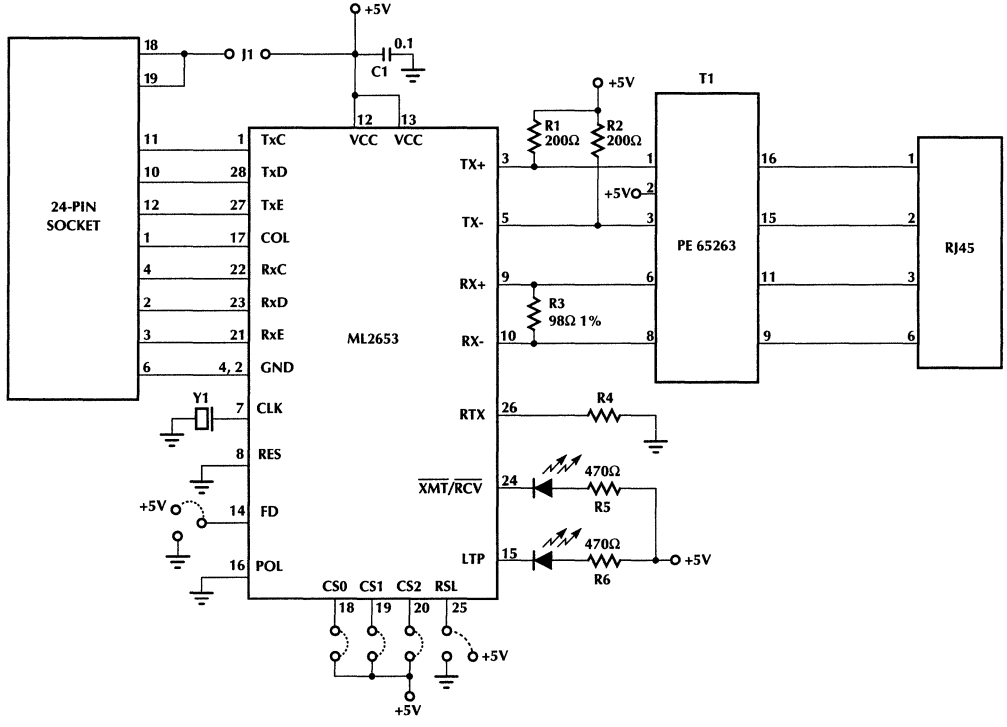
- LED status for; link detect, receive and transmit activity
- Selectable receive squelch level
- Selectable full duplex mode
- Single supply 5V ±5%

KIT COMPONENTS

- ML2653 user guide
- ML2653 data sheet
- ML2653 assembled Eval board

The user guide includes performance data, lay out recommendation, lay out, schematic, parts list and a tutorial on how to use the demo board.

BLOCK DIAGRAM



ML4621

Data Quantizer

GENERAL DESCRIPTION

The ML4621 Data Quantizers is a low noise, wideband, bipolar monolithic ICs designed specifically for signal recovery applications in fiberoptic receiver systems. It contains a two stage wideband limiting amplifier which is capable of accepting an input signal as low as 2mV with a 55dB dynamic range. This high level of sensitivity is achieved by using a DC restoration feedback loop which nulls any offset voltage produced in the limiting amplifier.

The output stage is a high speed comparator circuit with both TTL and ECL outputs. An enable pin is included for added control.

The Minimum Signal Discriminator circuit provides a Link Monitor function with a user selectable reference voltage. This circuit monitors the peaks of the input signal and provides a logic level output indicating when the input falls below an acceptable level. This output can be used to disable the Quantizer and/or drive an LED, providing a visible link status.

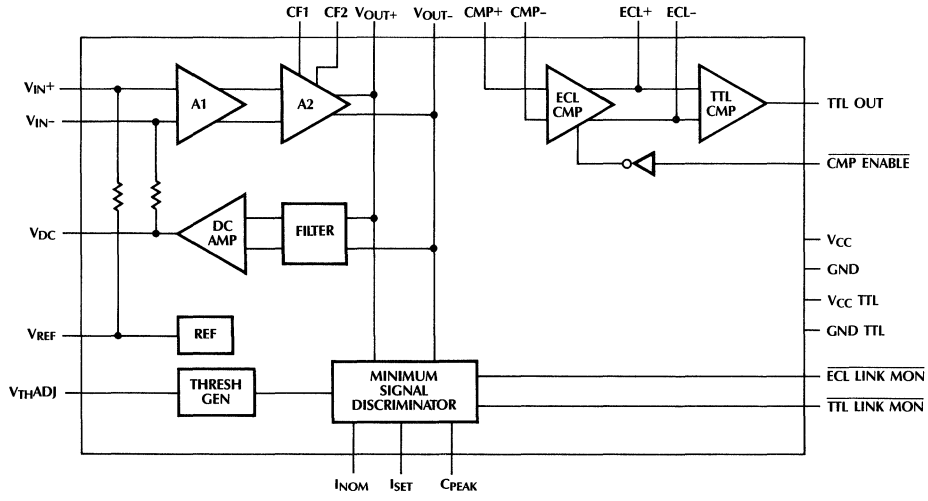
FEATURES

- 50MHz minimum bandwidth for data rates of up to 100MBd
- Can be powered by either +5V providing TTL level outputs or –5.2V providing ECL levels
- Low noise design:
  25μV RMS over 50MHz noise bandwidth
- Adjustable Link Monitor function
- Wide 55dB input dynamic range
- 10ns minimum input pulse
- Available in a 24-pin Skinny DIP and 28-pin PLCC

APPLICATIONS

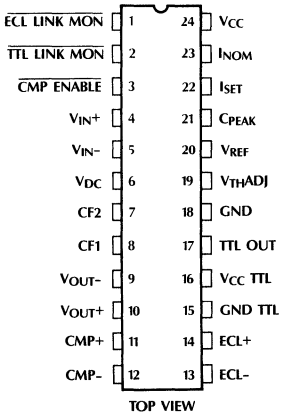
- IEEE 802.3 FOIRL Receiver
- IEEE 802.5 4 and 16 Mbps Fiber Optic Token Ring
- IEEE 802.4 Fiber Optic Token Bus
- Fiber Optic Data Communications and Telecommunications Receivers

BLOCK DIAGRAM



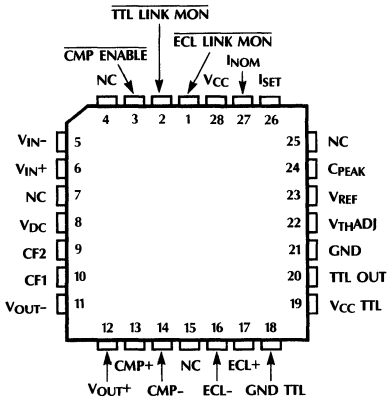
PIN CONNECTIONS

ML4621
24-Pin Skinny DIP



TOP VIEW

ML4621
28-Pin PCC



TOP VIEW

4

PIN DESCRIPTION

NAME	FUNCTION
$\overline{\text{ECL LINK MON}}$	ECL Link Monitor output. Signal is low when the V_{IN}+, V_{IN}– inputs exceed the minimum threshold, which is set by a voltage on the V_{TH}ADJ pin. Signal is high when the input signal level is below the threshold.
$\overline{\text{TTL LINK MON}}$	TTL Link Monitor output. Same logic function as $\overline{\text{ECL LINK MON}}$. Capable of driving a 10mA LED indicator. This pin normally tied to $\overline{\text{CMP ENABLE}}$.
$\overline{\text{CMP ENABLE}}$	A low voltage at this TTL input pin enables both the ECL and the TTL outputs. A high TTL voltage disables the comparator output with ECL+ high, ECL– low, and TTL OUT high.
V_{IN}–	This input pin should be capacitively coupled to the input source or to ground. (The input resistance is approximately 8kΩ.)
V_{IN}+	This input pin should be capacitively coupled to the input source or to ground. (The input resistance is approximately 8kΩ.)
CMP–	This comparator input pin is an open base configuration which relies on the DC bias of the amplifier output to establish the proper DC operating voltage. This voltage should be reestablished if filtering is implemented between V_{OUT}– and CMP–.
ECL–	The ECL comparator negative output.
ECL+	The ECL comparator positive output.
GND TTL	The negative supply for the TTL comparator stage. If the TTL output is not necessary, connect GND TTL and V_{CC} TTL to V_{CC}.
V_{CC} TTL	The positive supply for the TTL comparator stage. If the TTL output is not necessary, connect GND TTL and V_{CC} TTL to V_{CC}.
TTL OUT	TTL data output. (Totem pole type output stage.)

NAME	FUNCTION
V_{DC}	An external capacitor on this pin integrates an error signal which nulls the offset of the input amplifier. If the DC feedback loop is not being used, this pin should be connected to V_{REF}.
CF2	A capacitor from this pin to ground controls the maximum bandwidth of the amplifier to accommodate lower operating frequencies.
CF1	The capacitor on this pin should match the one on CF2.
V_{OUT}–	The negative output of the amplifier, which is normally tied to CMP–.
V_{OUT}+	The positive output of the amplifier, which is normally tied to CMP+.
CMP+	This comparator input pin is an open base configuration which relies on the DC bias of the amplifier output to establish the proper DC operating voltage. This voltage should be reestablished if filtering is implemented between V_{OUT}+ and CMP+.
GND	Negative supply. Connect to –5.2V for ECL operation, or to ground for TTL operation.
V_{TH}ADJ	This input pin sets the minimum amplitude of the input signal required to cause the link monitors to go low.
V_{REF}	A 2.5V reference with respect to GND.
C_{PEAK}	A capacitor from this pin to ground determines the Link Monitor response time.
I_{SET}	Current into an internal diode connected between this pin and GND is turned around and pulled from C_{PEAK}. This pin is normally connected to I_{NOM}.
I_{NOM}	Sets a current of approx. 125μA when connected to I_{SET}.
V_{CC}	Positive supply. Connect to ground for ECL operation, or to 5V for TTL operation.

ABSOLUTE MAXIMUM RATINGS

V_{CC} - GND ..... –0.3 to +7.0
V_{CC} TTL - GND TTL ..... –0.3 to +7.0
Inputs/Output GND ..... –0.3 to V_{CC} +0.3
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ML4621 ELECTRICAL CHARACTERISTICS

Over recommended operating conditions of T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, GND = 0V unless otherwise noted.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{CC1}	V_{CC} Supply Current		65	100	mA	V_{CC} TTL = GND TTL = V_{CC}
I_{CC2}	V_{CC} Supply Current (TTL Out Enabled)		70	110	mA	V_{CC} TTL = V_{CC} GND TTL = GND
$I_{V_{REF}}$	V_{REF} Output Current	–5.0		0.5	mA	
V_{REF}	Reference Voltage	2.40	2.55	2.65	V	
A_V	Amplifier Gain A1 A2		75		V/V	V_{IN} = 5mV
V_{IN}	Input Signal Range	2		1400	mV_{P-P}	
V_{TH}ADJ Range	External Voltage at V_{TH}ADJ to set V_{TH}	1		2.5	V	
V_{OS}	Input Offset		3		mV	V_{DC} = V_{REF} (DC loop inactive)
E_N	Input Referred Noise		25		μV	50MHz BW
BW	3dB Bandwidth	50	65		MHz	
V_{IN} PW	Min Input Pulsewidth		10		ns	
R_{IN}	Input Resistance		8		kΩ	V_{IN}+, V_{IN}–
t_{PD} AMP	Amplifier Propagation Delay	4		8	ns	From V_{IN}+, V_{IN}– to V_{OUT}+, V_{OUT}– V_{IN} = $10mV_{P-P}$
t_{PD} ECL	ECL Comparator Propagation Delay	4		8	ns	From CMP+, CMP– to ECL+, ECL– V_{IN} = $10mV_{P-P}$
t_{PD} TTL	TTL Comparator Propagation Delay	4		8	ns	From ECL+, ECL– to TTL OUT V_{IN} = $10mV_{P-P}$
$R_{V_{TH}ADJ}$	Input Resistance of V_{TH}ADJ		6.8		kΩ	
$I_{V_{OUT}}$	Output Current of V_{OUT}+ and V_{OUT}–			3	mA	
I_{CMP}	Leakage Current of CMP+ and CMP–		25		μA	
VCM_{CMP}	Common Mode Range of CMP+ and CMP–	GND + 2.0		V_{CC} – 1.0	V	
ECL V_{OH}	Output High Voltage at ECL+, ECL–	3.90		4.30	V	With 200Ω load tied to V_{CC} – 2V T_A = 25°C
ECL V_{OL}	Output Low Voltage at ECL+, ECL–	3.11		3.38	V	With 200Ω load tied to V_{CC} – 2V T_A = 25°C
A_V ECL	ECL CMP Gain		100		V/V	
TTL V_{OH}		2.4			V	V_{CC} TTL = 5V, I_{OH} = –50μA
TTL V_{OL}				0.4	V	V_{CC} TTL = 5V, I_{OL} = 2mA
TTL V_{IH}		2.0			V	
TTL V_{IL}				0.8	V	
TTL I_{IH}		–50		50	μA	V_{IH} = 2.4V
TTL I_{IL}		–1.6		0	mA	V_{IH} = 0.4V
I_{NOM}			125		μA	I_{NOM} = I_{SET}

FUNCTIONAL DESCRIPTION

AMPLIFIER

The Quantizer has a two stage limiting amplifier with an input common mode range of (GND + 1.8V) to (V_{CC} - 1.5V). Maximum sensitivity is achieved through the use of a DC restoration feedback loop and AC coupling the input. When AC coupled, the input DC bias voltage is set by an on-chip network at about 1.9V. These coupling capacitors, in conjunction with the input impedance of the amplifier, establish a high pass filter with a 3dB corner frequency, f_L, at

$$f_L = \frac{1}{2\pi\ 8000\ C} \quad (1)$$

Since the amplifier has a differential input, two capacitors of equal value are required. If the signal driving the input is single ended, one of the coupling capacitors can be tied to V_{CC} as shown in figure 1. The high corner frequency can also be adjusted by attaching capacitors to CF1 and CF2. The equation for adjusting this corner is

$$f_H = \frac{1}{2\pi\ 425\ C} \quad (2)$$

Although the input is AC coupled, the offset voltage *within* the amplifier will be present at the amplifier's output. This is represented by V_{OS} in figure 2. In order to reduce this error a DC feedback loop is incorporated. This negative feedback loop nulls the offset voltage, forcing V_{OS} to be zero. An external capacitor at V_{DC} is used to store the offset voltage. Although the value of this capacitor is non-critical, the pole it creates can effect the stability of the feedback loop. To avoid stability problems using the ML4621, the

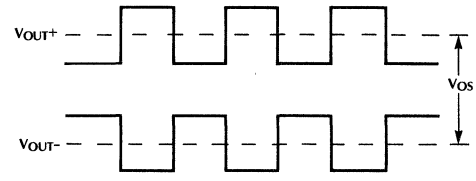


Figure 2.

value of this capacitor should be at least 100 times smaller than the input coupling capacitors.

On the ML4621, the output of the amplifier is isolated from the comparator and made available to the user. This allows the user to add circuitry between the amplifier and the comparator for wave shaping and other signal conditioning as desired.

COMPARATOR

Two types of comparators are employed in the output section of these Quantizers. The high speed ECL comparator is used to provide the ECL level outputs and in turn drives the TTL comparator. The enable pin, CMP ENABLE, is provided to control the ECL comparator. When CMP ENABLE is low the comparators function normally. When it's high, it forces ECL+ high, ECL- low, and TTL OUT high. The CMP ENABLE pin can be controlled with TTL level signals when the Quantizer is powered by 5V and ground.

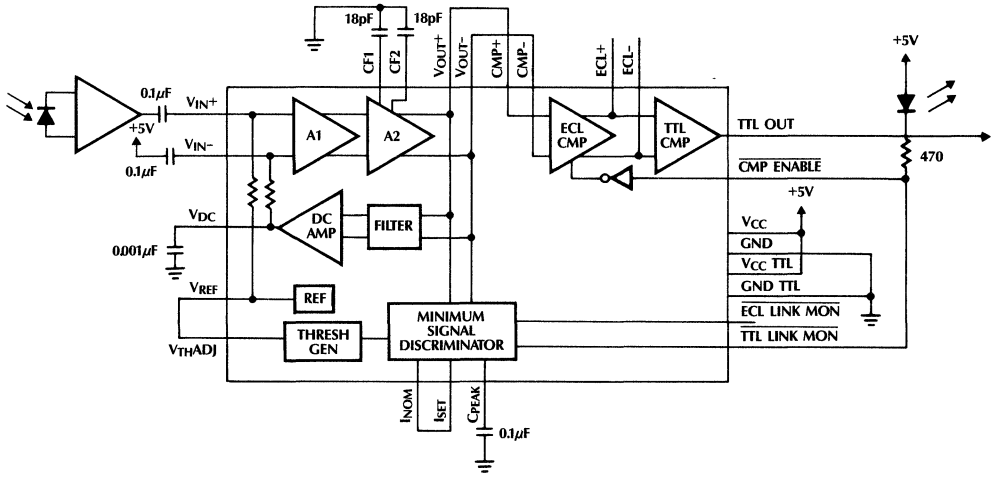


Figure 1. The ML4621 Configured for 20MHz Bandwidth with TTL Output

LINK MONITOR

This function is implemented by the Minimum Signal Discriminator and the Threshold Generator circuits. The purpose of this function is to monitor the input signal and provide a status signal indicating when the input falls below a preset voltage level. This is done by peak detecting the output of the amplifier section and comparing this level with the voltage at $V_{TH}ADJ$.

The equation which determines the droop rate of the peak detector is

$$\frac{dV}{dt} = \frac{I_{SET}}{C} \quad (3)$$

In this equation C is the peak capacitor at C_{PEAK}. On the ML4621 the droop rate of the peak detector can be adjusted two ways:

1) By adjusting the value of the peak capacitor at C_{PEAK}.
2) By adjusting the charge current into the peak capacitor at I_{SET}.

The charge current, I_{SET}, can be controlled externally by connecting a resistor, R_{EXT}, between I_{SET} and V_{CC}. I_{SET} will then be

$$I_{SET} = \frac{V_{CC} - 0.7}{R_{EXT} + 1700} \quad (4)$$

For convenience, an on-chip current source of 125μA is available by connecting I_{NOM} to I_{SET}.

The Threshold Generator level shifts the reference voltage at $V_{TH}ADJ$ through a circuit which has a temperature coefficient matching that of the limiting amplifier. The relationship between $V_{TH}ADJ$ and V_{TH} (the minimum *peak* voltage at the input which will trigger the Link Monitor) is:

$$V_{TH}ADJ = 600V_{TH} + 0.7 \quad (5)$$

The on-chip reference voltage, V_{REF}, can be tied directly to $V_{TH}ADJ$ to set the threshold level. This will set the minimum input signal on the ML4621 at about 3mV (peak).

A lower threshold level can be set by dividing down V_{REF} with a resistor string, as in figure 3.

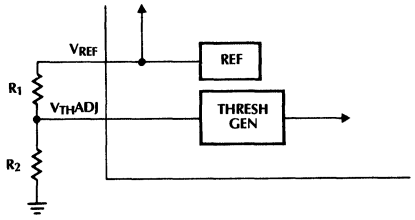


Figure 3.

Since the ML4621 has a relatively low input impedance of 6.8K and is offset by one diode drop, the equation which accounts for the load and offset is:

$$V_{TH}ADJ = \frac{R_2(6800V_{REF} + 0.7R_1)}{6800(R_1 + R_2) + R_1R_2} \quad (8)$$

THRESHOLD ADJUSTMENT EXAMPLE

If you are using the ML4621 and you want the Link Monitor to trigger when the received optical power goes below 1μW (-30dBm), you first need to calculate the resultant voltage at $V_{IN}+$ and $V_{IN}-$. If you are using the Hewlett-Packard HFBR-24X6 Fiberoptic Receiver with a responsitivity of 8mV/μW, the peak-to-peak voltage would be:

$$1\mu W \times 8mV/\mu W = 8mV_{P-P} \quad (9)$$

So the Link Monitor should trigger at some point slightly lower than 4mV peak, say 3mV. Setting V_{TH} in equation 5 to 3mV and solving for $V_{TH}ADJ$ yields:

$$V_{TH}ADJ = 600(.003) + 0.7 = 2.5V$$

This is a convenient value since the reference voltage supplied by the Quantizer, V_{REF}, is 2.5V.

The Link Monitor has about 0.4mV (peak) hysteresis built-in. More hysteresis can be induced by connecting a resistor between $\overline{\text{TTL LINK MON}}$ and $V_{TH}ADJ$ creating a positive feedback loop.

Refer to Micro Linear's Application Note 6 for more detail.

4

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4621CP	0°C to +70°C	Molded DIP (P24N)
ML4621CQ	0°C to +70°C	MOLDED PCC (Q28)

Micro Linear

ML4622, ML4624

Fiber Optic Data Quantizer

GENERAL DESCRIPTION

The ML4622 and ML4624 Data Quantizers are low noise, wideband, bipolar monolithic ICs designed specifically for signal recovery applications in fiberoptic receiver systems. They contain a wideband limiting amplifier which is capable of accepting an input signal as low as $2mV_{P-P}$ with a 55dB dynamic range. This high level of sensitivity is achieved by using a DC restoration feedback loop which nulls any offset voltage produced in the limiting amplifier.

The output stage is a high speed comparator circuit with both TTL and ECL outputs. An enable pin is included for added control.

The Link Detect circuit provides a Link Monitor function with a user selectable reference voltage. This circuit monitors the peaks of the input signal and provides a logic level output indicating when the input falls below an acceptable level. This output can be used to disable the Quantizer and/or drive an LED, providing a visible link status.

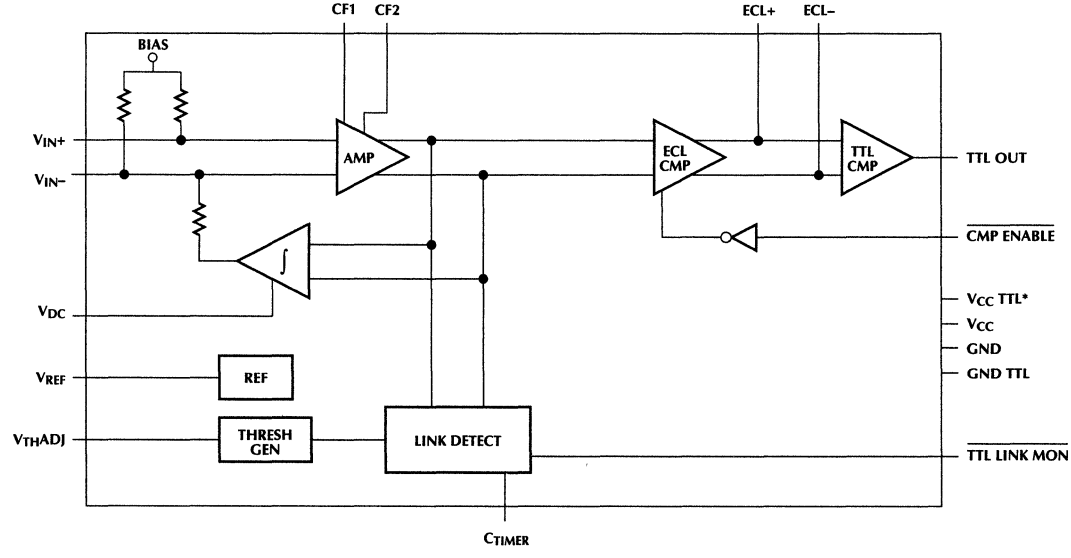
FEATURES

- Data rates up to 40MHz or 80MBd
- Can be powered by either +5V providing TTL or raised ECL level outputs or –5.2V providing ECL levels
- Low noise design: 25µV RMS over bandwidth
- Adjustable Link Monitor function with hystersis
- Wide 55dB input dynamic range
- Low power design
- Available in 16-pin SOIC (Narrow) or DIP (ML4622), 24-pin Skinny DIP (ML4624) and 28-pin PCC (ML4624)
- ML4624 is pin compatible with the ML4621

APPLICATIONS

- IEEE 802.3 FOIRL, 10BASE-F Receiver
- IEEE 802.5 4 and 16 Mbps Fiber Optic Token Ring
- Fiber Optic Data Communications and Telecommunications Receivers

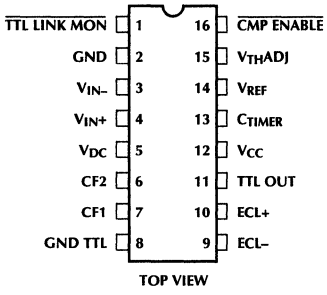
ML4622/ML4624 BLOCK DIAGRAM



*ML4624 ONLY

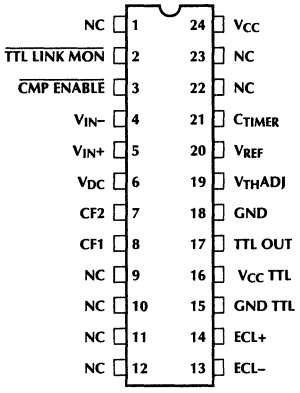
PIN CONNECTIONS

ML4622
16-Pin DIP or
SOIC (Narrow)



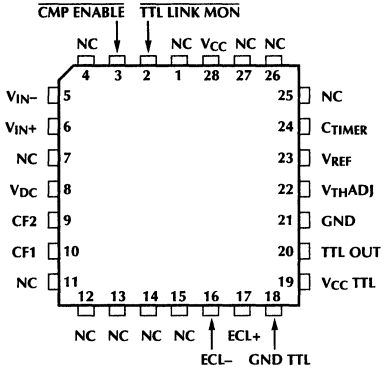
TOP VIEW

ML4624
24-Pin Skinny DIP



TOP VIEW

ML4624
28-Pin PCC



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PIN DESCRIPTION

NAME	FUNCTION
$\overline{\text{TTL LINK MON}}$	TTL Link Monitor output. Signal is low when the V_{IN}+, V_{IN}– inputs exceed the minimum threshold, which is set by a voltage on the V_{TH}ADJ pin. Signal is high when the input signal level is below the threshold. Capable of driving a 10mA LED indicator. This pin can be tied to $\overline{\text{CMP ENABLE}}$.
$\overline{\text{CMP ENABLE}}$	A low voltage at this TTL input pin enables both the ECL and the TTL outputs. A high TTL voltage disables the comparator output with ECL+ high, ECL– low, and TTL OUT high.
V_{IN}–	This input pin should be capacitively coupled to the input source or to filtered ground (note 5). (The input resistance is approximately 1.6KΩ.)
V_{IN}+	This input pin should be capacitively coupled to the input source or to filtered ground (note 5). (The input resistance is approximately 1.6KΩ.)
ECL–	The ECL comparator negative output. Has internal pull down resistor. External pull downs are not required unless driving a large capacitive load.
ECL+	The ECL comparator positive output. Has internal pull down resistor. External pull downs are not required unless driving a large capacitive load.
GND TTL	The negative supply for the TTL comparator stage. If the TTL output is not necessary, connect GND TTL to V_{CC}.
V_{CC} TTL	The positive supply for the TTL comparator stage. If the TTL output is not necessary, connect V_{CC} TTL to V_{CC}. (ML4624 only)
TTL OUT	TTL data output.
V_{DC}	An external capacitor on this pin integrates an error signal which nulls the offset of the input amplifier. If the DC feedback loop is not being used, this pin should be connected to V_{REF}.
CF2	A capacitor from this pin to CF1 controls the maximum bandwidth of the amplifier.
CF1	Connect to CF2 through a capacitor.
GND	Negative supply. Connect to –5.2V for ECL operation, or to ground for TTL or raised ECL operation.
V_{TH}ADJ	This input pin sets the link monitor threshold.
V_{REF}	A 2.5V reference with respect to GND.
C_{Timer}	A capacitor from this pin to V_{CC} determines the Link Monitor response time.
V_{CC}	Positive supply. Connect to ground for negative ECL operation, or to 5V for TTL or raised ECL operation.

ABSOLUTE MAXIMUM RATINGS

(Note 1)
V_{CC} – GND ..... –0.3 to +7.0
V_{CC} TTL – GND TTL ..... –0.3 to +7.0
Inputs/Outputs GND ..... –0.3 to V_{CC} +0.3
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C

ML4622, ML4624 ELECTRICAL CHARACTERISTICS (Note 2 and 3)

Over recommended operating conditions of T_A = 0°C to 70°C for commercial temperature range, T_A = –40°C to +85°C for industrial temperature range, V_{CC} = 5V ± 10%, GND = 0V unless otherwise noted.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{CC1}	V_{CC} Supply Current (TTL Output Disabled)		35	45	mA	GND TTL = V_{CC}
I_{CC2}	V_{CC} Supply Current (TTL Output Enabled)		55	70	mA	GND TTL = GND
V_{REF}	Reference Voltage	2.40	2.50	2.60	V	
I_{VREF}	V_{REF} Output Source Current			5	mA	
A_V	Amplifier Gain		100		V/V	
V_{IN}	Input Signal Range	2		1600	mV_{P-P}	
V_{TH}ADJ Range	External Voltage at V_{TH}ADJ to set V_{TH}	0.5		2.6	V	
V_{OS}	Input Offset		3		mV	V_{DC} = V_{REF} (DC loop inactive)
E_N	Input Referred Noise		25		µV	50MHz BW
BW	3dB Bandwidth		45		MHz	
R_{IN}	Input Resistance	1	1.6	2.5	kΩ	V_{IN}+, V_{IN}–
I_{VTHADJ}	Input Bias Current of V_{TH}ADJ	–200	10	+200	µA	
t_{PDTTL}	Propagation Delay		15		ns	From V_{IN}+, V_{IN}– to TTL Out V_{IN} = $10mV_{P-P}$
t_{PDECL}	Propagation Delay		11		ns	From V_{IN}+, V_{IN}– to ECL+, ECL– V_{IN} = $10mV_{P-P}$
TTL V_{OH}		2.4			V	V_{CC} TTL = 5V, I_{OH} = –50µA
TTL V_{OL}				0.55	V	V_{CC} TTL = 5V, I_{OL} = 2mA
TTL V_{IH}		2.0			V	
TTL V_{IL}				0.8	V	
TTL I_{IH}		–50		50	µA	V_{IH} = 2.4V
TTL I_{IL}		–1.6		0	mA	V_{IH} = 0.4V

ML4622, ML4624 ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions of T_A = 0°C to 70°C for commercial temperature range, T_A = –40°C to +85°C for industrial temperature range, V_{CC} = 5V ± 10%, GND = 0V unless otherwise noted.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{TH}	Input Threshold Voltage ML4622 ML4624	 4 5	 5 6	 6 7	 mV_{P-P} mV_{P-P}	 $V_{TH}ADJ = V_{REF}$ (note 4) $V_{TH}ADJ = V_{REF}$ (note 4)
Hystersis			20		%	
V_{CM}	Common mode voltage on VIN+, VIN–		1.65		V	
ECL_{VOH}	Output High Voltage at ECL+, ECL–	V_{CC} – 1.06		V_{CC} – 0.7 V_{CC} – 0.6	 (note 5)	With 200Ω load tied to V_{CC} – 2V
ECL_{VOL}	Output Low Voltage at ECL+, ECL–	V_{CC} – 1.89		V_{CC} – 1.62 V_{CC} – 1.56	 (note 5)	With 200Ω load tied to V_{CC} – 2V

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Low Duty Cycle pulse testing is performed at T_A.

Note 4: DC Tested — Threshold for switching $\overline{\text{TTL LINK MON}}$ from High (off) to Low (on).

Note 5: Industrial temperature range specification..

FUNCTIONAL DESCRIPTION

AMPLIFIER

The ML4622, ML4624 have an adjustable Bandwidth limiting amplifier. Maximum sensitivity is achieved through the use of a DC restoration feedback loop and AC coupling the input. When AC coupled, the input DC bias voltage is set by an on-chip network at about 1.7V. These coupling capacitors, in conjunction with the input impedance of the amplifier, establish a high pass filter with a 3dB corner frequency, f_L, at

$$f_L = \frac{1}{2\pi 1600\,C} \qquad (1)$$

Since the amplifier has a differential input, two capacitors of equal value are required. If the signal driving the input is single ended, one of the coupling capacitors can be tied to V_{CC} as shown in figure 1.

CF1 and CF2 create a low pass filter with the corner frequency determined by the following equation

$$f_H = \frac{1}{2\pi 800(C+4pF)} \qquad (2)$$

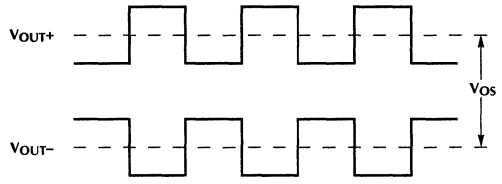
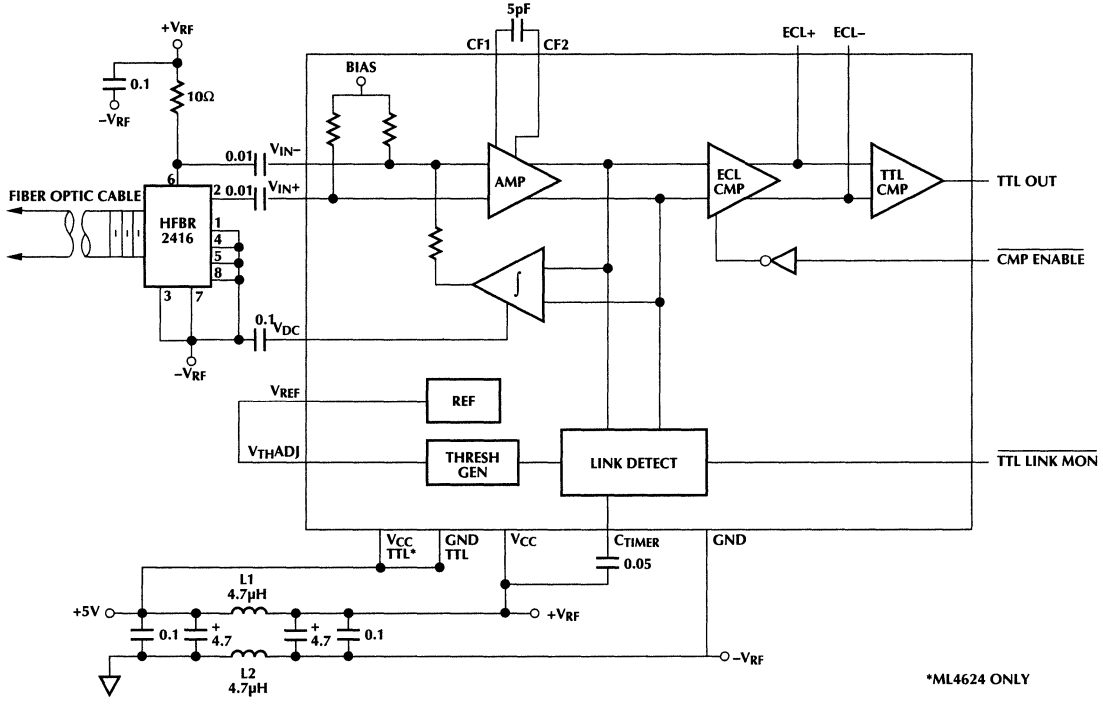


Figure 2.

The above equation applies when a single capacitor is tied between CF1 and CF2. When using two capacitors of equal value (Cap1 from CF1 to V_{CC}, Cap2 from CF2 to V_{CC}) the value derived for C should be doubled.

Although the input is AC coupled, the offset voltage *within* the amplifier will be present at the amplifier's output. This is represented by V_{OS} in figure 2. In order to reduce this error a DC feedback loop is incorporated. This negative feedback loop nulls the offset voltage, forcing V_{OS} to be zero. Although the capacitor on V_{DC} is non-



Note: If TTL OUT is used, tie GND TTL to unfiltered ground and remove L1. If TTL OUT and ECL outputs are both used, add 3K pulldown resistors at ECL outputs.

Figure 1. The ML4622, ML4624 Configured for 20MHz Bandwidth

critical, the pole it creates can effect the stability of the feedback loop. To avoid stability problems, the value of this capacitor should be at least 10 times larger than the input coupling capacitors.

COMPARATOR

Two types of comparators are employed in the output section of these Quantizers. The high speed ECL comparator is used to provide the ECL level outputs and in turn drives the TTL comparator. The enable pin, CMP ENABLE, is provided to control the ECL comparator. When CMP ENABLE is low the comparators function normally. When it's high, it forces ECL+ high, ECL– low, and TTL OUT high. The CMP ENABLE pin can be controlled with TTL level signals when the Quantizer is powered by 5V and ground.

LINK DETECT CIRCUIT

The Link Detect circuit monitors the input signal and provides a status signal indicating when the input falls below a preset voltage level. When the input falls below the preset voltage level, the TTL LINK MON output changes from active (low) to inactive (high). This signal can be fed to the ML4662 10BASE-FL transceiver or a similar type of function to indicate a Low Light Condition. This output can also be used to disable the output data by tying it to the CMP ENABLE input.

In many fiber optic systems, including Ethernet and Token Ring, a bit error rate is given at a minimum power level. For example, in a 10Base-FL receiver there must be less than 1×10^{-9} bit errors at a receive power level of –32.5dBm average. Designers of these systems must insure that the bit error rate is lower than the specification at the given minimum power level. One procedure to determine the sensitivity of a receiver is to start at the lowest optical power level and gradually increase the optical power until the BER is met. In this case the Link Detect circuit must not disable the receiver (i.e. CMP ENABLE should be tied to Ground). Once the sensitivity of the receiver is determined, the Link Detector circuit can be set just above the power level that meets the BER specification. This way the receiver will shut off before the BER is exceeded.

The ML4622 and ML4624 quantizers have greater Link Detect sensitivity, noise immunity, and accuracy than their predecessor the ML4621.

The threshold generator shifts the reference voltage at $V_{TH}ADJ$ through a circuit which has a temperature coefficient matching that of the limiting amplifier. The relationship between the $V_{TH}ADJ$ and the V_{TH} (the peak to peak input threshold) is:

$$V_{TH}ADJ = 417\ V_{TH} \text{ (ML4624)} \quad (3)$$

$$V_{TH}ADJ = 500\ V_{TH} \text{ (ML4622)}$$

In most cases, including 10Base-FL, 10Base-FB and Token-Ring, $V_{TH}ADJ$ can be tied directly to V_{REF}. However if greater sensitivity is required the circuit in figure 3 can be used to adjust the $V_{TH}ADJ$ voltage. Even if V_{REF} is tied to $V_{TH}ADJ$, it is a good idea to layout a board with these two resistors available. This will allow potential future adjustments without board revisions.

The response time of the Link Detect circuit is set by the C_{Timer} pin. Starting from the link off state (i.e., TTL LINK MON is high), the link can be switched on if the input exceeds the set threshold for a time given by:

$$T = \frac{C_{TIMER} \times 0.7V}{700\mu A} \quad (4)$$

To switch the link from on to off, the above time will be doubled.

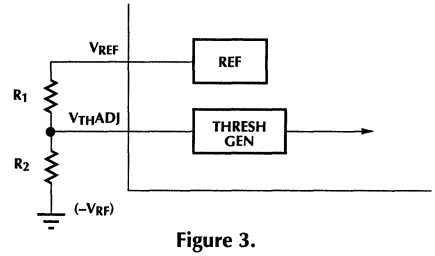


Figure 3.

BURST MODE

In some fiber optic links, the idle signal is DC, or of a frequency that is substantially different from the data. For these links, a faster response time of the DC loop and the Link Monitor is required.

The ML4622 and ML4624 has been designed to accommodate these two requirements. The input coupling capacitors can be relatively small and still maintain stability. With smaller input coupling capacitors and V_{DC} capacitor a faster DC loop response time can be achieved. The Link Monitor is also enhanced to have a faster response time.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4622CP	0°C to +70°C	Molded DIP (P16)
ML4622CS	0°C to +70°C	Molded SOIC (Narrow) (S16N)
ML4622IS	–40°C to +85°C	Molded SOIC (Narrow) (S16N)
ML4624CP	0°C to +70°C	Molded DIP (P24N)
ML4624CQ	0°C to +70°C	Molded PCC (Q28)

ML4632

Fiber Optic LED Driver

GENERAL DESCRIPTION

The ML4632 is a fiber optic LED driver suited for network applications up to 20Mbps. The part is capable of driving up to 100mA of current through a Fiber Optic LED from an ECL or TTL level input signal. Its efficient output stage provides a high current that can be programmed for accurate absolute output level as well as automatic temperature compensation. The combination of automatic temperature compensation and a highly accurate current driven design insures precise launch power.

The LED driver's output stage provides fast, well matched rise and fall times through a unique class B output stage that burns supply current only when the LED is on. A positive temperature coefficient of up to 3300ppm/°C can be programmed into the output current to compensate for the negative temperature coefficient of the LED optical output power. An optional peaking circuit may also be employed.

The ECL and TTL inputs are ANDed so one can be used for data and the other for an enable input. An ECL compatible BIAS voltage is also provided for single ended ECL applications.

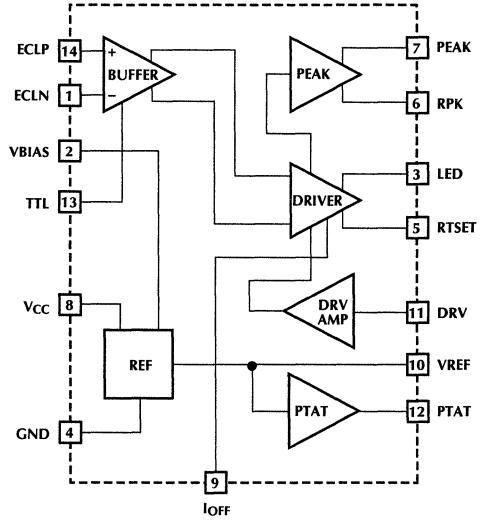
FEATURES

- Current Driven Output for accurate Launch Power
- Programmable output current from 20mA to 100mA
- Programmable temperature coefficient, 0 to 3300ppm/°C
- High Efficiency Output Stage
- Programmable LED pre-bias current
- Low EMI/RFI Noise
- ECL or TTL inputs
- Optional Peaking circuit

APPLICATIONS

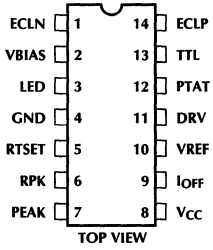
- IEEE 802.3, 10BASE-F
- IEEE 802.5 Fiber Optic Token Ring
- IEEE 802.4 Fiber Optic Token Bus
- Fiber Optic Data Communications and Telecommunications

BLOCK DIAGRAM

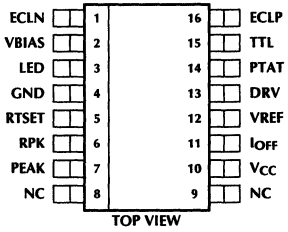


PIN CONFIGURATION

ML4632
14-Pin DIP (P14)



ML4632
16-Pin SOIC (S16W)



PIN DESCRIPTION

NAME	FUNCTION
ECLN	Negative ECL data input. Tie to VBIAS for single ended ECL operation or when ECLP is used as an enable. Tie to ground during TTL only operation.
VBIAS	BIAS voltage for single ended ECL operation.
LED	Fiber optic LED drive pin. Connect the LED between this pin and V_{CC}.
GND	Negative power supply. The pin should be tied to the grounded side of RTSET to improve output accuracy and avoid a ground loop.
RTSET	Output current programming pin. Connect a resistor of value V_{DRV}/I_{LED} from this pin to ground to set the high LED output current.
RPK	Peaking circuit bias pin. Connect a resistor of value V_{DRV}/I_{PEAK} from this pin to ground when using the peaking circuit. Leave open circuited when peaking is not used.
PEAK	Peaking circuit output pin. When using peaking, connect this pin to V_{CC} through a resistor of value RRPK. Then connect a capacitor from this pin to the LED cathode. When peaking is not used, open circuit RPK.

NAME	FUNCTION
V_{CC}	Positive power supply. +5 volts.
I_{OFF}	Connect a resistor from this pin to V_{CC} to increase the off current to the LED, i.e. 4.3KΩ for 1mA. With this pin open, the default I_{OFF} current is between 0.5–1.0mA.
VREF	A constant 1.2V reference output used to set up DRV.
DRV	A DC input that sets the positive swing on RTSET and the high level output current to the LED.
PTAT	Proportional to Absolute Temperature. A 1.0V reference at 25°C that moves proportional to absolute temperature, also used to set up DRV. (See figure 1)
TTL	TTL data input. Can also be used as an enable during ECL operation. TTL = High (enabled), TTL = Low (disabled).
ECLP	Positive ECL data input controls signal to the LED. Tie to VBIAS during TTL only operation or use as an enable.

4

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... –0.3V to 6V
Input Pin Voltages ..... –0.3V to V_{CC} +0.3V
LED Output Current 120mA
PEAK DC Output Current 120mA
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... 260°C

ELECTRICAL CHARACTERISTICS

Over the recommended operating conditions of T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Supply Current	LED off		25	35	mA
VREF	VREF Voltage	No Load	1.14	1.20	1.26	V
V_{PTAT}	PTAT Voltage	No Load, T_A = 25°C T_A = 85°C	0.9 1.08	1.0 1.2	1.1 1.32	V V
V_{OS}	Driver Offset	VDRV = 1.2V, RTSET = 20Ω			50	mV
 I_{LEDH} I_{LEDL}	LED Current Accuracy High Low	VDRV = VREF, RTSET = 20Ω I_{OFF} = open	 54 0.5	 60 0.7	 66 1.0	 mA mA
t_R	Rise Time	VDRV = VREF, RTSET = 20Ω		4.5		ns
t_F	Fall Time	VDRV = VREF, RTSET = 20Ω		4.5		ns
 t_{PLH} t_{PHL}	Propagation Delay Low to High High to Low	VDRV = VREF, RTSET = 20Ω TTL and ECL		 10.0 10.0		 ns ns
t_{PWD}	Pulse Width Distortion	VDRV = VREF, RTSET = 20Ω		1.0	2.0	ns
V_{PK}	Peaking Voltage	R_{RPK} = 20Ω, C_{PK} = 100pF, R_{PEAK} = 20Ω	1.08	1.2	1.32	V
V_{PKTR}	Peaking Rise Time	R_{RPK} = 20Ω, C_{PK} = 100pF, R_{PEAK} = 20Ω		4.5		ns
V_{PKTF}	Peaking Fall Time	R_{RPK} = 20Ω, C_{PK} = 100pF, R_{PEAK} = 20Ω		4.5		ns
I_{ECL}	ECL Input Current				20	µA
I_{TTL}	TTL Input Current				100	µA
V_{DO}	Dropout Voltage between pin 5 and 3		1.5			V
I_{OFF}	Additional LED Off Current	V_{CC} = 5V, R_{IOFF} = 4.3KΩ	0.8	1.0	1.2	mA
VBIAS	ECL BIAS Voltage	V_{CC} = 5V, T_A = 25°C		3.8		V

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Limits are guaranteed by 100% testing, sampling or correlation with worst-case test conditions.
Note 3: Low Duty cycle pulse testing is performed at T_A.

FUNCTIONAL DESCRIPTION

The ML4632 accepts ECL and TTL input signals and generates a high speed, high accuracy output current which is independent of supply voltage variations. The output current is programmable from 20mA to 100mA. A temperature coefficient can be programmed into the output current and a peaking circuit can be added with a few external components.

The input of the LED driver accepts both ECL and TTL signals. The ECL input stage is a standard NPN differential pair with a common mode range of between 3V and 4.5V with a +5V supply. A bias voltage VBIAS is available for biasing either ECL input for single-ended operation. The TTL input has a standard switching range of between 0.8V and 2.0V. These inputs are ANDed so that the extra input can be used as an enable.

Output current to the LED is set by connecting the appropriate resistance from RTSET to ground. With the VREF and DRV pins tied together, the high level output voltage at RTSET will be 1.2V. The current through the LED. The output current with RTSET set to 20Ω will be

$$I_{LED}\,(HIGH) = 1.2V/R_{TSET} = 1.2V/20\Omega = 60mA.$$

The low level output current is set internally by a resistor at approximately 0.7mA. This current prebiases the LED and results in faster optical rise times. The value of this current can be increased by connecting a resistor from the I_{OFF} pin to V_{CC}. The additional current will be equal to $(V_{CC} - 0.7V)/R_{IOFF}$.

The voltage input at the DRV pin appears across the RTSET pin when the LED is turned on. The current in RTSET is directed through the LED. Therefore the voltage set at DRV along with the RTSET resistor sets current through the LED.

A temperature coefficient of between 0ppm/°C and 3300ppm/°C can be programmed into the high level output current to compensate for the drop in LED optical output power at high temperatures. This is accomplished by driving the DRV pin from a resistor divider between the VREF and PTAT pins.

When DRV is tied directly to PTAT, the peak voltage at RTSET will be 1.0V at 25°C and have a 3300ppm/°C temperature coefficient. At 85°C, PTAT is 1.2V and equal to VREF. An arbitrary temperature coefficient less than 3300 ppm/°C can be set by using a resistor divider between PTAT and VREF to set the voltage at DRV, as shown in figure 1.

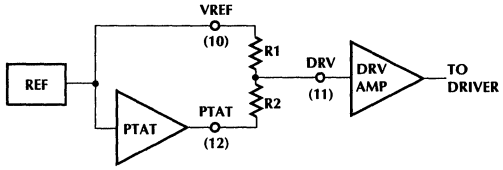


Figure 1. Current for Programming Output Temperature Coefficient

In this configuration the temperature coefficient is

$$TC_{ILED} = (3300ppm/°C)\frac{R1}{R1+R2}, \text{ and}$$

$$I_{LED\,(HIGH)} = \frac{1V + 0.2V\left(\frac{R2}{R1+R2}\right)}{RTSET}$$

The output current will be a linear function of temperature. A plot of I_{LED} versus temperature for several values of the programming resistance, R1 and R2, in figure 2.

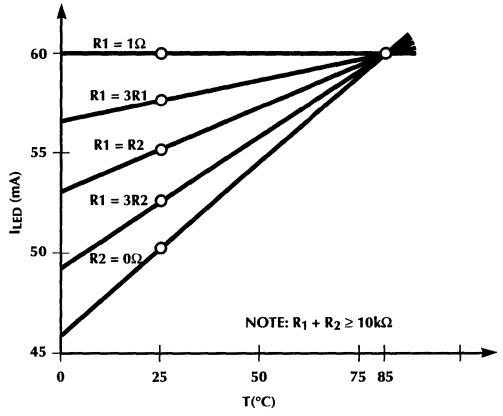


Figure 2. I_{LED} vs T, R_{TSET} = 20Ω

The ML4632 output stage conducts full load current only when the LED is on, and even then power dissipation in the part is low because most of the +5V supply voltage is dropped across the LED and external resistor R_{TSET}. Even with a low power design, the LED driver junction temperature will rise above ambient due to quiescent power dissipation and won't exactly match the LED junction temperature since it is also self-heating. Therefore, the effectiveness of a temperature compensated design will be related to component power dissipations, thermal conductance of the PC board and packaging, and the proximity of the LED driver to the LED.

The ML4632 also provides for peaking of the LED output current. Peaking is used to counteract the effects of the LED junction capacitance. By creating a controlled overshoot and undershoot in the output current waveform, charge is transferred to and from the LED capacitance on the rising and falling edges of the output, speeding up rise and fall times.

To provide peaking current, a second output stage is biased up with a resistor from RPK to ground and another from PEAK to V_{CC}. When these bias resistors are set equal to each other, a pulse will be generated across the R_{PEAK} resistor with a magnitude equal to the voltage on the DVR pin. A coupling capacitor transfers the rising and falling edges of the output current waveform.

A typical application is shown in figure 3. When the resistors R_{RPK} and R_{PEAK} are both set to 20Ω, a pulse will be generated at the PEAK pin of magnitude 1.2V and equivalent resistance 20Ω (assuming V_{DRV} = 1.2V).

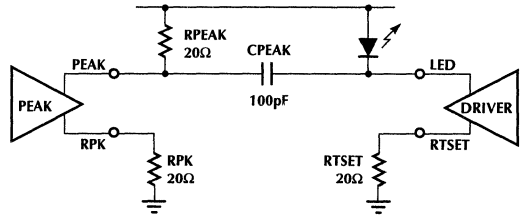
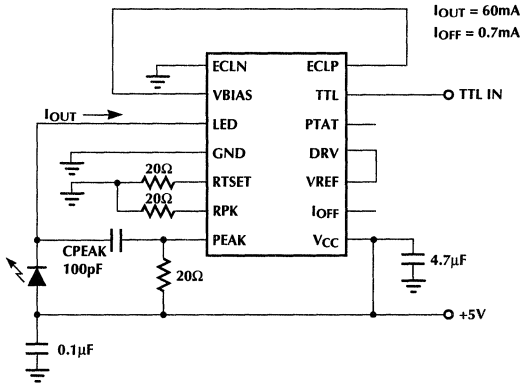


Figure 3. Application of the Peaking Circuit

The peaking current is coupled through the 100pF capacitor, C_{PEAK}, which will transfer 120pC of charge to and from the LED on each cycle of output current. The peaking circuit shown provides approximately a 70% overshoot current into a 0Ω LED impedance. Peaking currents will be slightly lower for real LED's.



Note: The LED, PEAK and V_{CC} traces should be very short and shielded with a GND plane to reduce ringing and overshoot at the LED.

TTL Driven Implementation
(No Temp. Comp)

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4632CP	0°C to +70°C	14-Pin Molded DIP (P14)
ML4632CS	0°C to +70°C	16-Pin SOIC (S16W)

ML4642

AUI Multiplexer

GENERAL DESCRIPTION

The ML4642 AUI Multiplexer contains all the necessary drivers/receivers and control logic to implement a 2 port MAU when used in conjuction with a transceiver chip which has a standard 802.3 AUI interface. In addition, the ML4642 is capable of operating in stand-alone mode where it interconnects two DTEs in the absence of a network MAU. Several ML4642s can be cascaded together to implement a 4 or 8 port MAU or stand-alone device.

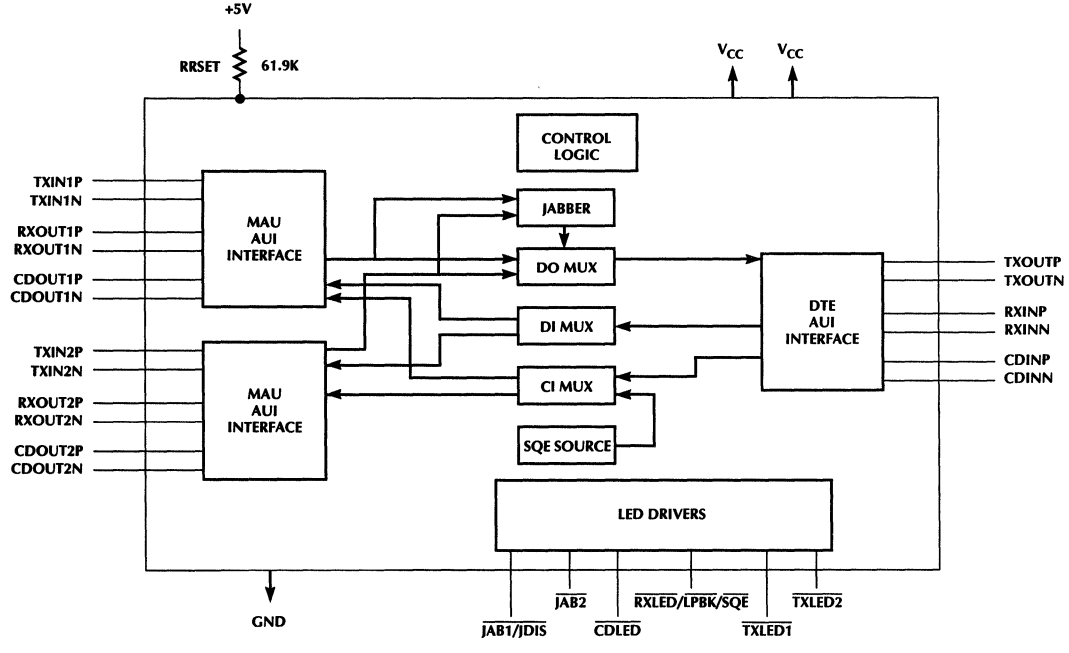
Logic within the ML4642 detects collisions resulting from multiple DTEs transmitting simultaneously. In addition, collision signals received from a transceiver attached at the MAU port are propagated to both of the DTE ports. Jabbering DTEs are prevented from loading down the network by internal jabber timers which disable babbling ports.

Squelch circuitry on port receivers prevent noise on the cables from being erroneously interpreted as valid data. Transmit, receive, collision, and jabber LED drivers indicate network activity and faults. The ML4642 is available in a 28 pin SSOP package.

FEATURES

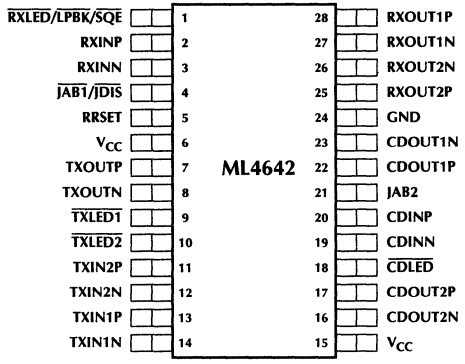
- IEEE 802.3 compliant AUI interfaces assure compatibility with any AUI ready devices.
- No crystal or clock input.
- On-chip Jabber logic, Collision Detection, and SQE test with enable/disable option.
- Selectable Loopback, Jabber, and SQE Test allows cascading of multiple chips to increase DTE port fan-out.
- Six network status LED outputs.
- 28 pin SSOP packaging
- Semi-standard options available

BLOCK DIAGRAM



PIN CONNECTIONS

ML4642
28-PIN SSOP (R28)



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION	DESCRIPTION
1	$\overline{\text{RXLED}}/\overline{\text{LPBK}}/\overline{\text{SQE}}$	I/O	Active low receive LED driver for MAU port. If tied to ground, this pin enables internal loopback of the active TXIN pair to the RXOUT pairs and enables SQE test. If tied to 0.6 volts internal loopback is enable but SQE test is disabled. SQE and loopback are disabled when this pin is pulled high.
2	RXINP	Input	Receive signal pair for MAU port.
3	RXINN	Onput	Receive signal pair for MAU port.
4	$\overline{\text{JAB1}}/\overline{\text{JDIS}}$	I/O	Active low jabber LED driver for DTE port 1. If tied to ground, the jabber function is disabled at TXIN1 and TXIN2.
5	RRSET	Input	Bias setting external resistor, 61.9KΩ.
6	V_{CC}	Power	+5 volt power supply
7	TXOUTP	Output	Transmit signal pair for MAU port.
8	TXOUTN	Output	Transmit signal pair for MAU port.
9	$\overline{\text{TXLED1}}$	Output	Open collector, active low transmit LED driver for DTE AUI port 1.
10	$\overline{\text{TXLED2}}$	Output	Open collector, active low transmit LED driver for DTE AUI port 2.
11	TXIN2P	Input	Transmit signal pair for DTE port 2.
12	TXIN2N	Input	Transmit signal pair for DTE port 2.
13	TXIN1P	Input	Transmit signal pair for DTE port 1.
14	TXIN1N	Input	Transmit signal pair for DTE port 1.
15	V_{CC}	Power	+5 volt power supply
16	CDOUT2N	Output	Collision signal pair for DTE port 2.
17	CDOUT2P	Output	Collision signal pair for DTE port 2.
18	$\overline{\text{CDLED}}$	Output	Open collector, active low collision LED driver.
19	CDINN	Input	Collision signal pair for MAU port.
20	CDINP	Input	Collision signal pair for MAU port.
21	JAB2	Output	Open collector, active low jabber LED driver for DTE port 2.
22	CDOUT1P	Output	Collision signal pair for DTE port 1.
23	CDOUT1N	Output	Collision signal pair for DTE port 1.
24	GND	Ground	GND.
25	RXOUT2P	Output	Receive signal pair for DTE port 2.
26	RXOUT2N	Output	Receive signal pair for DTE port 2.
27	RXOUT1N	Output	Receive signal pair for DTE port 1.
28	RXOUT1P	Output	Receive signal pair for DTE port 1.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Power Supply Voltage Range V_{CC} ..... −0.3 to +6.0V
Input Current RRSET, $\overline{JAB1}/\overline{JABD}$, $\overline{JAB2}$, $\overline{CDLED}$, $\overline{RxLED}/\overline{LPBK}/\overline{SQE}$, $\overline{TxLED1}$, $\overline{TxLED2}$ 60mA
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering 10 seconds)..... 260°C

OPERATING CONDITIONS (Note 2)

Supply Voltage (V_{CC}) ..... 5V ± 10%
LED on Current 10mA
RRSET ..... 61.9KΩ ± 1%

ML4642 ELECTRICAL CHARACTERISTICS

Unless otherwise specified T_A = 0°C to 70°C (Note 3), V_{CC} = 5V ± 10%.

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Power Supply Current I_{CC} (Note 4)	V_{CC} = 5V		60	120	mA
LED Drivers: V_{OL}	R_L=510Ω for $\overline{CDLED}$, $\overline{TXLED1}$,2, $\overline{JAB2}$ R_L=270Ω for $\overline{JAB1}/\overline{JDIS}$, $\overline{RxLED}/\overline{LPBK}/\overline{SQE}$ (Note 5)			0.8	V
Transmit Squelch Voltage Level (Tx+, Tx−)		−300	−250	−200	mV
Differential Output Voltage		±550		±1200	mV
Common Mode Output Voltage			4.0		V
Differential Output Voltage Imbalance			2	±40	mV
$\overline{RxLED}/\overline{LPBK}/\overline{SQE}$	$\overline{SQE}$ Enabled/Loopback Enabled $\overline{SQE}$ Disabled/Loopback Enabled	 0.4	 0.6	0.3 0.8	V

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Limits are guaranteed by 100% testing , sampling, or correlation with worst-case test conditions.
Note 3: Low Duty cycle pulse testing is performed at T_A.
Note 4: This does not include the current from the AUI pull down resistors or the LED output pins
Note 5: LED drivers can sink up to 20mA, but V_{OL} will be higher

ML4642 ELECTRICAL CHARACTERISTICS (Continued)

AC ELECTRICAL CHARACTERISTICS

SYMBOLS	PARAMETER	MIN	TYP.	MAX	UNITS
TRANSMIT					
t_{TXNPW}	Transmit Turn-On Pulse Width		20		ns
t_{TXFPW}	Transmit Turn-Off Pulse Width		180		ns
t_{XODY}	Transmitter Turn-On Delay		30		ns
t_{TXLP}	Transmit Loopback Startup Delay		40		ns
t_{TXSDY}	Transmit Steady State Prop. Delay		15		ns
t_{TXJ}	Transmitter Jitter		1		ns
RECEIVE					
t_{RXODY}	Receive Turn-On Delay		20		ns
t_{RXSDY}	Receive Steady State Prop. Delay		15		ns
t_{RXJ}	Receiver Jitter		1		ns
t_{AR}	Differential Output Rise Time 20% to 80% (Rx+/–, COL+/–)		3		ns
t_{AF}	Differential Output Fall Time 20% to 80% (Rx+/–, COL+/–)		3		ns
COLLISION					
t_{CPSQE}	Collision Present to SQE Assert	0		200	ns
t_{SQEXR}	Time for SQE to Deactivate after a collision	100		900	ns
t_{CLF}	Collision Frequency	8.5	10	11.5	MHz
t_{CLPDC}	Collision Pulse Duty Cycle	40	50	60	%
t_{SQEDY}	SQE Test Delay (Tx Inactive to SQE)	0.6	1.1	1.6	µs
t_{SQETD}	SQE Test Duration	0.5	1.0	1.5	µs
t_{SQEB}	SQE Blank Period	4		7	µsec
JABBER, LINK TEST AND LED TIMING					
t_{JAD}	Jabber Activation Delay	7	13.5	20	ms
t_{JRT}	Jabber Reset Unjab Time	250	450	750	ms
t_{JSQE}	Delay from Outputs Disabled to Collision Oscillator On		100		ns
t_{LEDT}	$\overline{\text{CDLED}}$, $\overline{\text{RxLED}}$, $\overline{\text{TxLED1}}$, $\overline{\text{TxLED2}}$ On Time	20	50	300	ms

TIMING DIAGRAMS

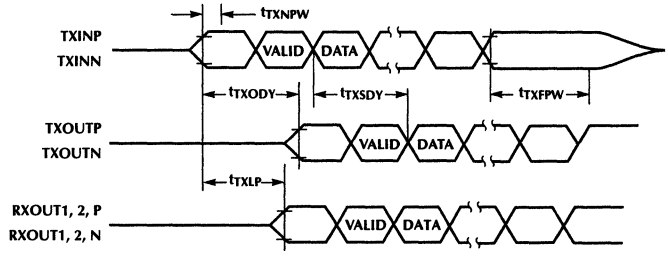


Figure 1. Transmit and Loopback Timing

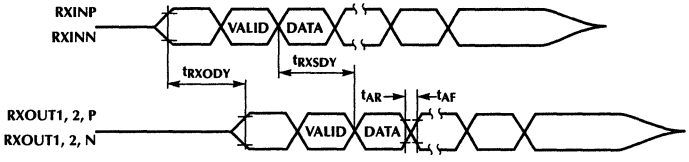


Figure 2. Receive Timing

TIMING DIAGRAMS (Continued)

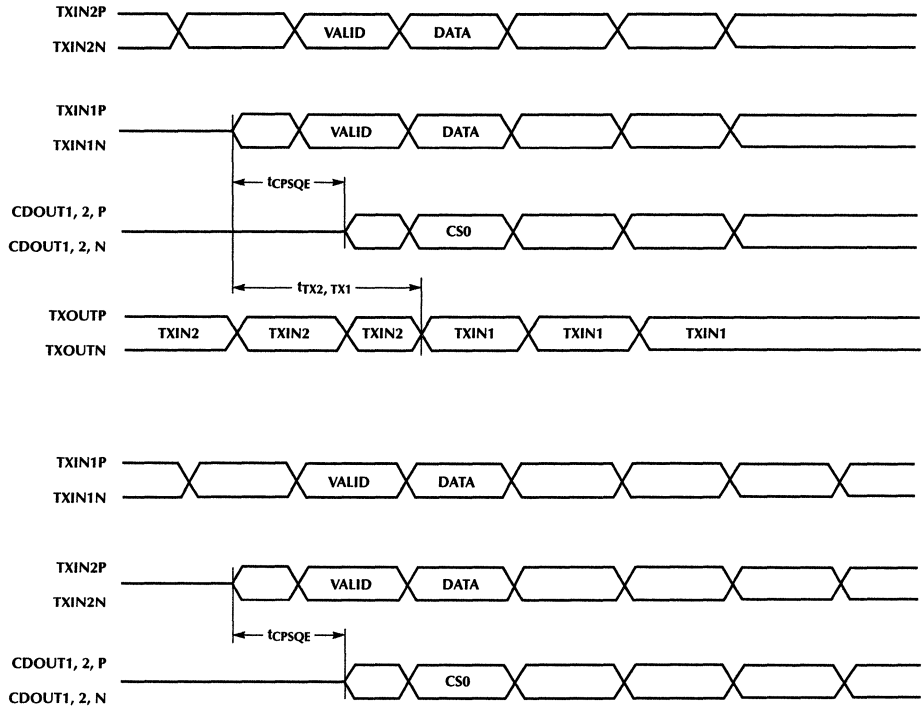


Figure 3. Collision Timing

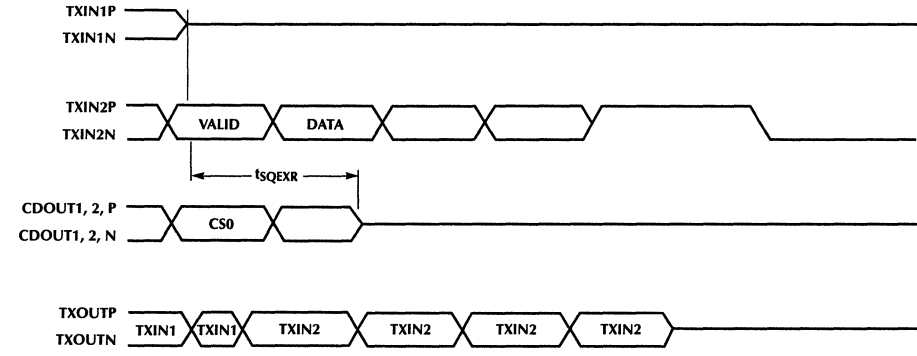


Figure 4. Collision Timing

TIMING DIAGRAMS (Continued)

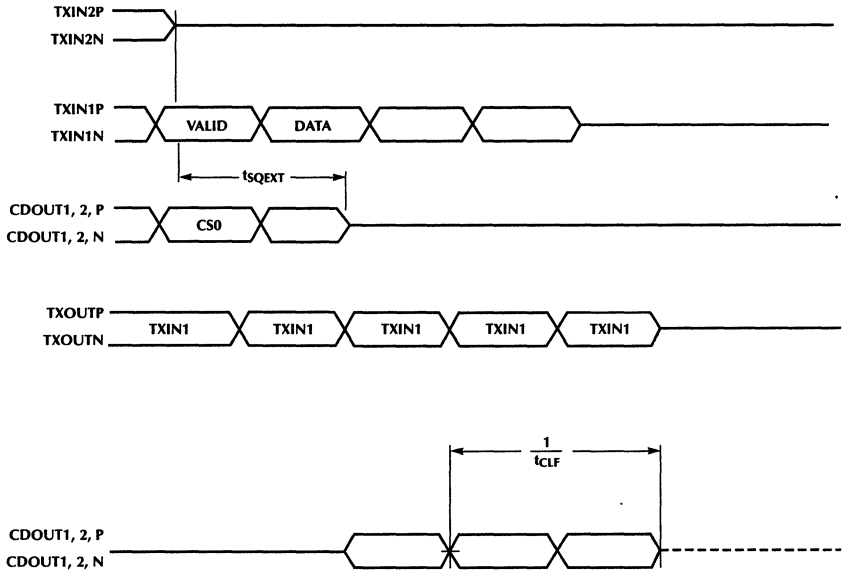


Figure 5. Collision Timing

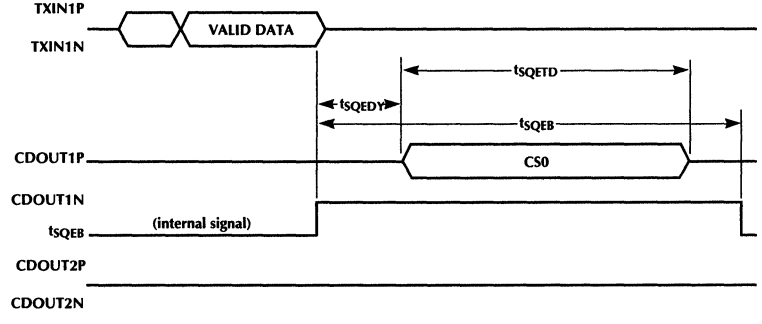


Figure 6. SQE Timing

TIMING DIAGRAMS (Continued)

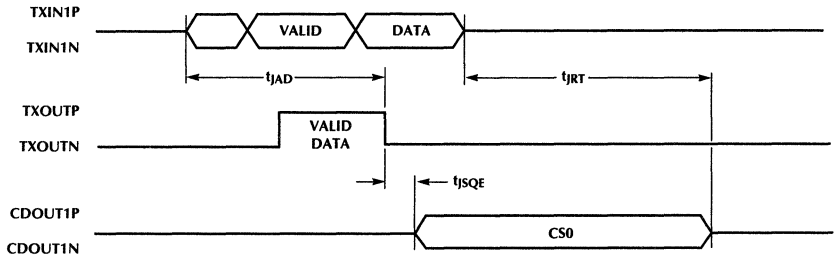


Figure 7. Jabber Timing

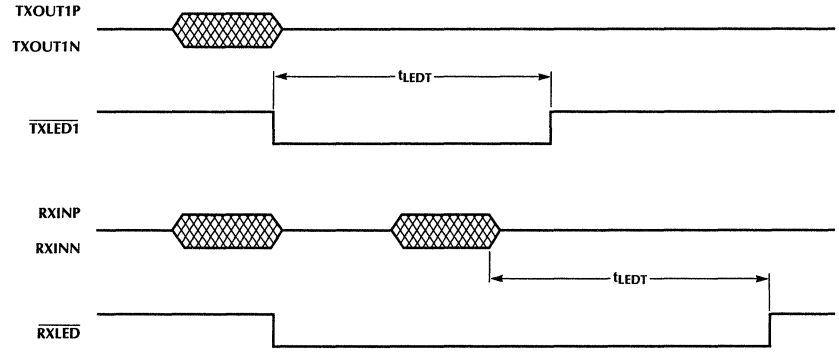


Figure 8. LED Timing

FUNCTIONAL DESCRIPTION

Figure 9 is a block diagram of a Two Port Multiplexer using the ML4642 chip. All AUI interfaces are shown AC coupled as they would be in an AUI multiplexer which does not include the MAU circuitry on the same board.

TRANSMISSION

The transmit function consists of detecting data on either of the TXIN differential receivers (TXIN1 or TXIN2) and transmitting this data out the TXOUT differential driver at the MAU port as well as both RXOUT1 and RXOUT2 drivers of the DTE ports. (Note: the looping back of data received at a TXIN pair to the RXOUT pairs is discussed in the Loopback section.)

Before data will be transmitted to the TXOUT and RXOUT pins from the TXIN pins it must meet the unsquelch requirements of the TXIN receiver circuitry. The squelch circuitry prevents any noise on the TXIN wires from being misinterpreted as data and transmitted to the TXOUT and RXOUT pins. The squelch circuit rejects signals with pulse widths less than typically 20ns and voltage levels more positive than –250mV. Once the TXIN receiver is unsquelched it remains so until reception of the input idle signal, which is detected when the TXIN signal is more positive than –170mV for longer than 180ns.

RECEPTION

The receive function consists of detecting data at the RXIN differential receiver of the MAU port transmitting this data to both DTE port RXOUT pairs.

Before data will be transmitted to the RXOUT pins of the DTE ports it must meet the unsquelch requirements for the RXIN receiver circuitry. The squelch circuitry at the RXIN differential receiver input performs the same function as that of the TXIN squelch circuitry using the same noise rejection criteria.

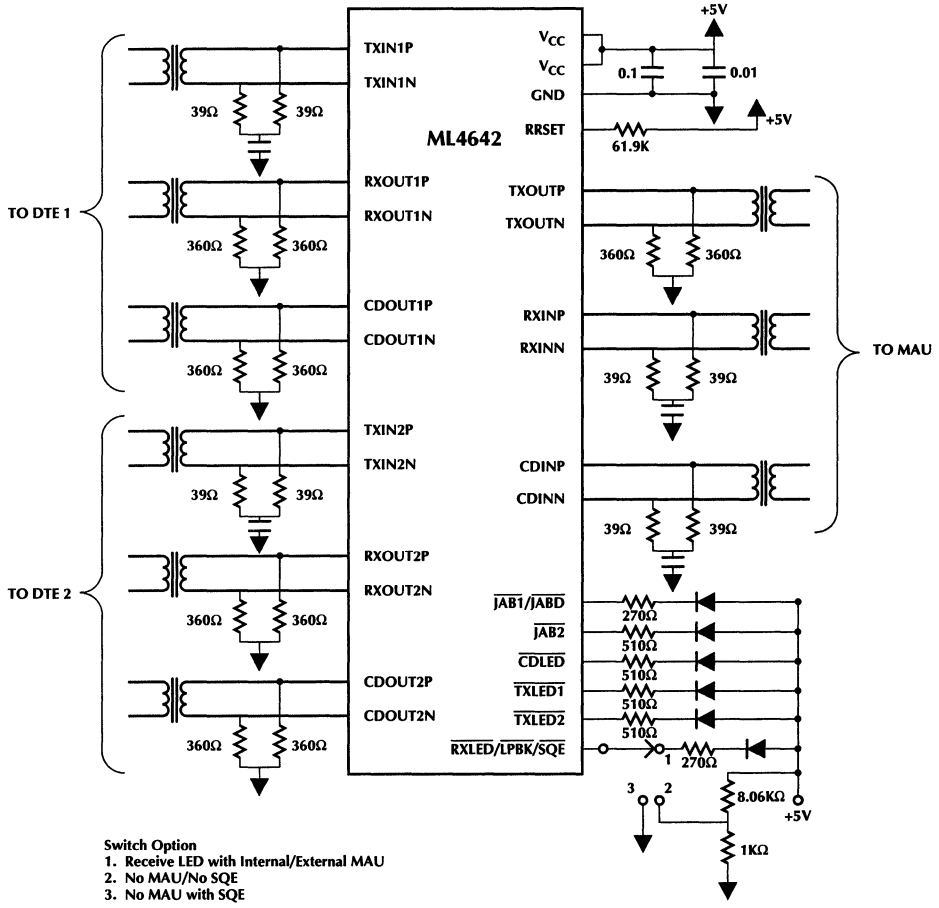


Figure 9. Two Port AUI Multiplexer

COLLISION

There are two conditions that constitute a collision from the point of view of the ML4642:

a) If data is received at the TXIN inputs of both DTE ports simultaneously a **local collision** occurs within the ML4642.

b) If the CDIN input is active at any time other than the inter-packet gap window allowed for the SQE Test function described below.

In either of the above circumstances it is necessary for the ML4642 to drive the CDOUT pairs on both DTE ports with the collision signal. The collision signal consists of a 10 MHz +/– 15% square wave matching the AUI specifications and capable of driving a 78Ω load. The collision signal shall turn on within 2 bit times of the origination of the collision condition and shall turn off within 2–5 bit times after the collision condition subsides.

During a collision condition there are two sources for data to be transmitted to TXOUT, TXIN1 and TXIN2. The highest priority source for data to be transmitted to TXOUT is the TXIN1 receiver.

For example if TXIN2 begins transmission then TXIN1 turns on, the collision oscillator will turn on and TXOUT will switch from TXIN2 to TXIN1. If the collision ends by TXIN1 turning off first, TXOUT will switch from TXIN1 to TXIN2, and 2–5 bit times later the collision oscillator will turn off.

The MAU port's CDIN receiver contains squelch circuitry to prevent noise from causing the erroneous detection of a collision signal. A signal on the CDIN pair will not be considered active until it exceeds the same squelch requirements as those of the TXIN receivers.

LOOPBACK

The loopback function allows the ML4642 to emulate a coaxial transceiver by propagating the TXIN data back out the RXOUT pair of the same DTE port that is sourcing the data as well as the RXOUT pair of the idle DTE port. This allows the Ethernet controller sending the data to monitor its transmit packets and detect network faults.

The loopback function is enabled at both DTE ports when the $\overline{\text{RXLED}}$ pin is tied to ground, or 0.6 volts.

SQE TEST FUNCTION

The Signal Quality Error (SQE) Test function allows the DTE to determine whether or not the collision detection circuitry is functional. After each transmission, during the inter-packet gap time, the collision signal will be activated on the CDOUT pair of the same port as the TXIN pair which received the packet, for typically 1 µs. The SQE function will not be activated on DTE ports of the ML4642 which are in the Jabber state. The SQE function is enabled on both DTE ports when the RXLED/LPBK/SQE pin is grounded.

JABBER

The jabber function prevents a babbling transmitter from loading down the network. Within the ML4642 is a jabber timer on each TXIN receiver. Each timer starts at the beginning of a received packet and resets at the end of each packet. If a packet lasts longer than 7 to 20ms the jabber logic disables its corresponding TXIN receiver (thus preventing its data from being retransmitted) and generates a collision signal on the babbling port's CDOUT pair. When the TXIN pair finally goes idle, a second timer measures 0.5 seconds of idle on TXIN prior to re-enabling the receiver and turning off the collision signal. If the TXIN pair becomes active again before the 0.5 seconds has expired, the timer is reset and measures another 0.5 seconds of idle time.

The jabber function can be disabled on both ports by tying the JAB1/JABD pin to ground.

LED DRIVERS

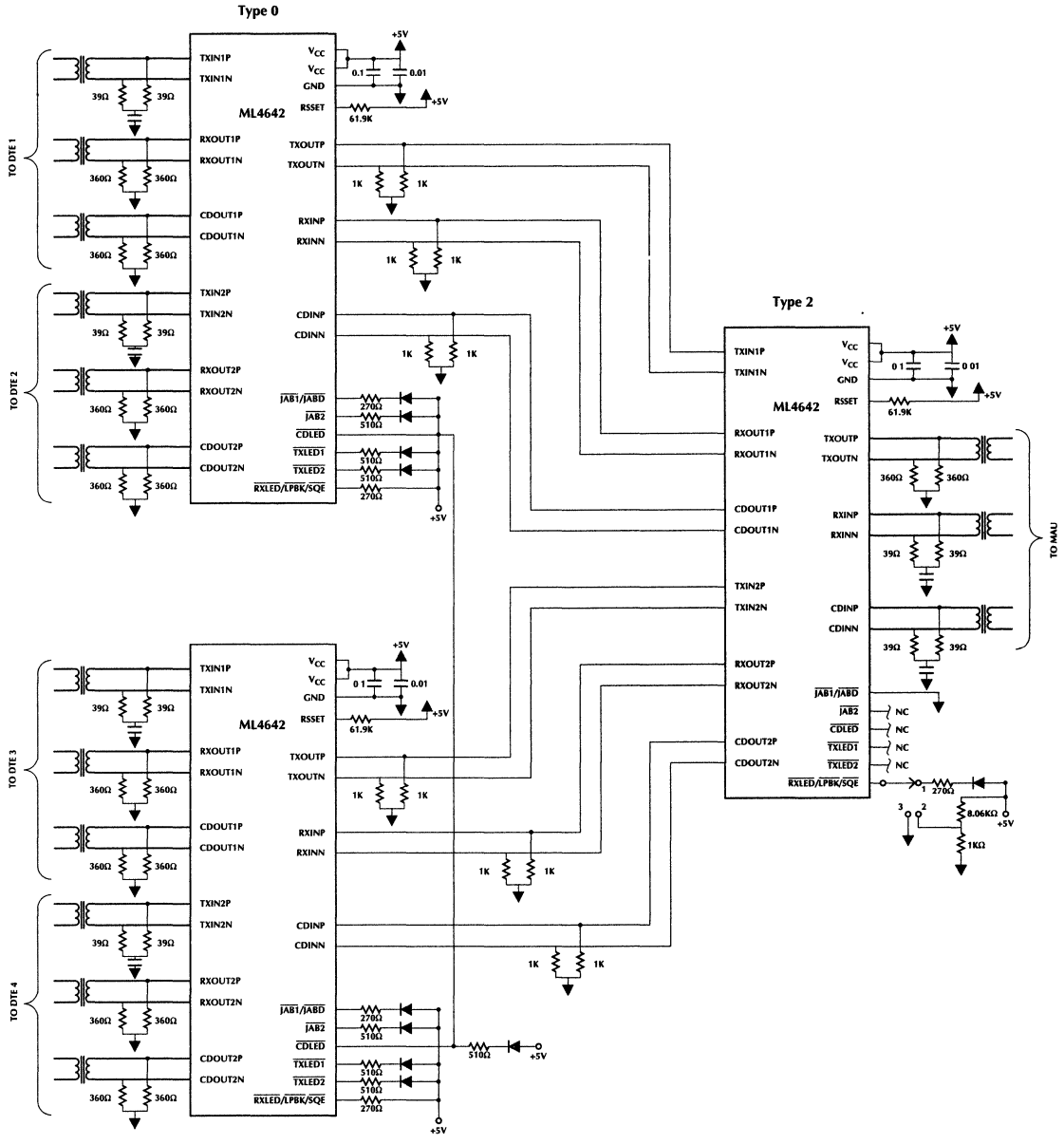
The ML4642 has six LED driver pins. Each DTE port has a transmit LED and a jabber LED and the MAU port has a receive LED. Additionally, there is a collision LED which indicates the presence of a collision condition. All LED drivers are active low 10mA current sources.

The $\overline{\text{TXLED}}$, $\overline{\text{RXLED}}$, and $\overline{\text{CDLED}}$ outputs have 50ms pulse stretchers on them to enable the LEDs to be visible. The $\overline{\text{JLED}}$ outputs do not have pulse stretchers on them because their conditions occur long enough for the LEDs to be visible.

Two of the ML4642 LED outputs serve as configuration pins as well. $\overline{\text{RXLED}}$/LPBK/$\overline{\text{SQE}}$ and JAB1/$\overline{\text{JDIS}}$ may be tied through a resistor to V_{CC}, tied through a resistor and a LED to V_{CC} or grounded. Additionally $\overline{\text{RXLED}}$/LPBK/$\overline{\text{SQE}}$ may be tied to a specific voltage. When these pins are grounded or tied to a 0.6 Volts they become configuration inputs. Otherwise when tied high they become status outputs.

CASCADING THE ML4642 FOR 4 AND 8 PORT DESIGNS

The configurability of such functions as loopback, jabber, and SQE allows ease of cascading multiple ML4642 chips for larger fan-out designs. Figure 10 shows a four port AUI Multiplexer design. For a type 0 configuration both jabber and transmit LEDs are available on a per port basis for status. The $\overline{\text{RXLED}}$/LPBK/$\overline{\text{SQE}}$ pins are tied through a resistor to 5 volts, and $\overline{\text{CDLED}}$ is wire OR'ED with the other chip for one collision detect status LED per system. There is also only one receive LED status output which is displayed in a type 2 configuration. This particular pin in a type 2 configuration offers three options. In option 1, when tied to +5 volts through a resistor and an LED, an internal or external MAU will be connected. For stand-alone operation without an internal or external MAU a loopback is required. Option 2 allows loopback with no SQE test while option 3 provides loopback with an SQE test.



Switch Options
1 Receive LED with Internal/External MAU
2 No MAU/No SQE
3. No MAU with SQE

Figure 10. Four Port AUI Multiplexer

An eight port design is accomplished in the same way as shown in the block diagram in Figure 11. In an eight port design Type 0 and Type 2 configuration remain the same as in a four port design. Type 1 however only differs from Type 2 by tying $\overline{\text{RXLED}}/\text{LPBK}/\overline{\text{SQE}}$ through a resistor to +5 volts. Table 1 summerizes all of the different LED configurations.

SQE TEST WHEN CASCADING

As mentioned before, after each transmission during the interpacket gap time the collision signal will be activated on the CDOUT pair of the same port as the TXIN pair which received the packet. When cascading ML4642s to implement 4 or 8 port designs, the path is remembered and followed to acheive this function. The paths that did not carry the transmit data blocks CDOUT for 4-7 µsec after transmission to guarantee that only the port that transmitted will see SQE test.

TABLE 1. LED Configurations for 2, 4, and 8 Port Designs

	JAB1/JABD	RXLED/LPBK/SQE	JAB2	CDLED	TXLED1	TXLED2
Two Port AUI Mux	LED	GND, 0.6V, LED	LED	LED	LED	LED
Type 0	LED	270Ω to +5V	LED	WIRE'ORED	LED	LED
Type 1	GND	270Ω to +5V	NC	NC	NC	NC
Type 2	GND	GND, 0.6V, LED	NC	NC	NC	NC

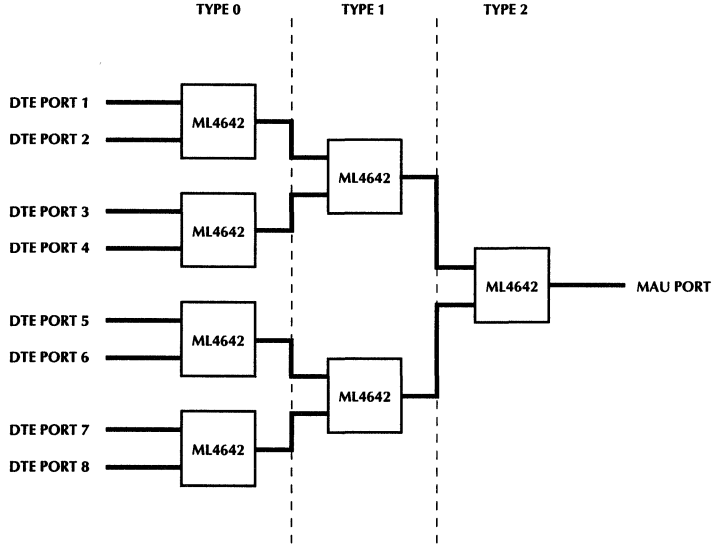


Figure 11. Eight Port AUI Multiplexer

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4642CR	0°C to 70°C	28-Pin SSOP (R28)

ML4644

4 Port AUI Multiplexer

GENERAL DESCRIPTION

The ML4644 AUI Multiplexer contains all the necessary drivers/receivers and control logic to implement a 4 port MAU when used in conjuction with a transceiver chip which has a standard 802.3 AUI interface. Two ML4644s together with a ML4642 can be used to implement an 8 port MAU.

Logic within the ML4644 detects collisions resulting from multiple DTEs transmitting simultaneously. In addition, collision signals received from a transceiver attached at the MAU port are propagated to all of the DTE ports. Jabbering DTEs are prevented from loading down the network by an internal jabber timer which disables babbling ports.

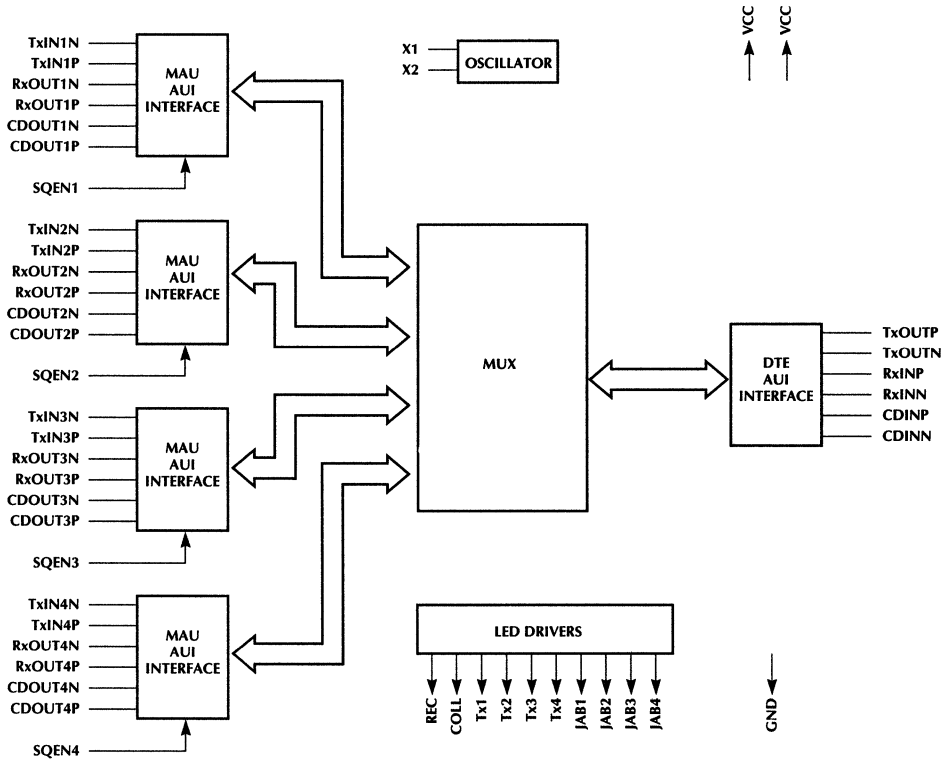
Squelch circuitry on port receivers prevent noise on the cables from being erroneously interpreted as valid data.

Transmit, receive, collision, and jabber LED drivers indicate network activity and faults. The ML4644 is available in a 68 pin PLCC package.

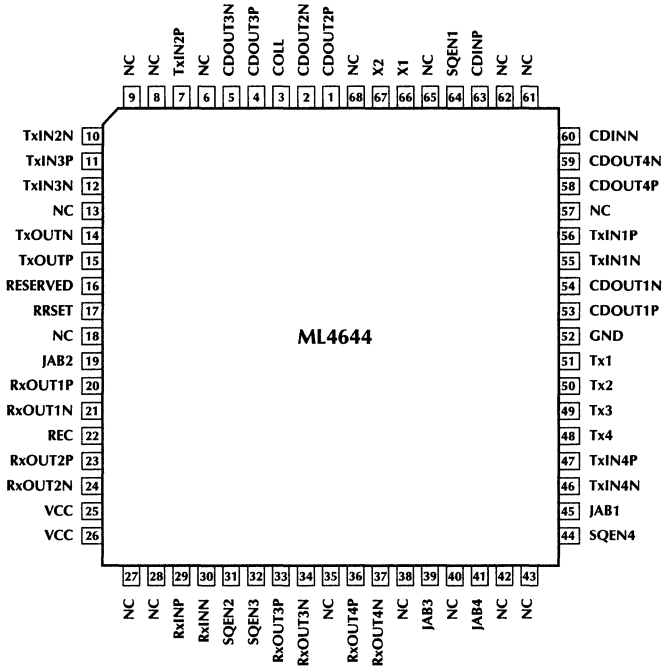
FEATURES

- IEEE 802.3 compliant AUI interfaces assure compatibility with any AUI ready devices.
- On-chip Jabber logic, Collision Detection, and SQE test with enable/disable option.
- Selectable SQE Test
- Ten network status LED outputs.
- 68 pin PLCC packaging
- Semi-standard options available

BLOCK DIAGRAM



PIN CONNECTIONS



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PIN DESCRIPTION

PIN #	NAME	FUNC.	DESCRIPTION
1	CDOUT2P	Output	Collision signal pair for DTE port 2.
2	CDOUT2N	Output	Collision signal pair for DTE port 2.
3	COLL	Output	Open collector LED driver for collision.
4	CDOUT3P	Output	Collision signal pair for DTE port 3.
5	CDOUT3N	Output	Collision signal pair for DTE port 3.
6	NC		No connection.
7	TxIN2P	Input	Transmit signal pair for DTE port 2.
8	NC		No connection.
9	NC		No connection.
10	TxIN2N	Input	Transmit signal pair for DTE port 2.
11	TxIN3P	Input	Transmit signal pair for DTE port 3.
12	TxIN3N	Input	Transmit signal pair for DTE port 3.
13	NC		No connection.
14	TxOUTN	Output	Transmit signal pair for MAU port.
15	TxOUTP	Output	Transmit signal pair for MAU port.
16	Reserved		This pin should be tied to VCC.
17	RRSET	Input	Bias setting external resistor, 61.9KΩ, connected to VCC
18	NC		No connection.
19	JAB2	Output	Open collector jabber LED driver for Jabber of DTE port 2.
20	RxOUT1P	Output	Receive signal pair for DTE port 1.
21	RxOUT1N	Output	Receive signal pair for DTE port 1.

PIN DESCRIPTION (continued)

PIN #	NAME	FUNC.	DESCRIPTION
22	REC	Output	Open collector LED driver for receive
23	RxOUT2P	Output	Receive signal pair for DTE port 2.
24	RxOUT2N	Output	Receive signal pair for DTE port 2.
25	VCC	Power	+5V power supply.
26	VCC	Power	+5V power supply.
27	NC		No connection.
28	NC		No connection.
29	RxINP	Input	Receive signal pair for MAU port.
30	RxINN	Input	Receive signal pair for MAU port.
31	SQEN2	Input	Active High. This pin is used to enable the SQE function of DTE port 2.
32	SQEN3	Input	Active High. This pin is used to enable the SQE function of DTE port 3.
33	RxOUT3P	Output	Receive signal pair for DTE port 3.
34	RxOUT3N	Output	Receive signal pair for DTE port 3.
35	NC		No connection.
36	RxOUT4P	Output	Receive signal pair for DTE port 4.
37	RxOUT4N	Output	Receive signal pair for DTE port 4.
38	NC		No connection.
39	JAB3	Output	Open collector jabber LED driver for Jabber of DTE port 3.
40	NC		No connection.
41	JAB4	Output	Open collector jabber LED driver for Jabber of DTE port 4.
42	NC		No connection.
43	NC		No connection.
44	SQEN4	Input	Active High. This pin is used to enable the SQE function of DTE port 4.
45	JAB1	Output	Open collector jabber LED driver for Jabber of DTE port 1.
46	TxIN4N	Input	Transmit signal pair for DTE port 4.
47	TxIN4P	Input	Transmit signal pair for DTE port 4.
48	Tx4	Output	Open collector transmit LED driver for Jabber of DTE port 4.
49	Tx3	Output	Open collector transmit LED driver for Jabber of DTE port 3.
50	Tx2	Output	Open collector transmit LED driver for Jabber of DTE port 2.
51	Tx1	Output	Open collector transmit LED driver for Jabber of DTE port 1.
52	GND	Ground	Ground.
53	CDOUT1P	Output	Collision signal pair for DTE port 1.
54	CDOUT1N	Output	Collision signal pair for DTE port 1.
55	TxIN1N	Input	Transmit signal pair for DTE port 1.
56	TxIN1P	Input	Transmit signal pair for DTE port 1.
57	NC		No connection.
58	CDOUT4P	Output	Collision signal pair for DTE port 4.
59	CDOUT4N	Output	Collision signal pair for DTE port 4.
60	CDINN	Input	Collision signal pair for MAU port.
61	NC		No connection.
62	NC		No connection.
63	CDINP	Input	Collision signal pair for MAU port.
64	SQEN1	Input	Active High. This pin is used to enable the SQE function of DTE port 1.
65	NC		No connection.
66	X1	Input	10MHz Crystal input pin. This pin can also be used as a 10MHz clock input pin.
67	X2	Input	10 MHz Crystal input pin.
68	NC		No connection.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Power Supply Voltage Range V_{CC} ..... –0.3 to +6.0V
Input Current RRSET, All LED Driver Pins 60mA
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering 10 seconds)..... 260°C

OPERATING CONDITIONS (Note 2)

Supply Voltage (V_{CC}) ..... 5V ± 10%
RRSET..... 61.9KΩ ± 1%

ELECTRICAL CHARACTERISTICS

Unless otherwise specified T_A = 0°C to 70°C (Note 3), V_{CC} = 5V ± 10%.

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Power Supply Current I_{CC} (Note 4)	V_{CC} = 5V	50	150	190	mA
LED Drivers: V_{OL}	R_L=510Ω (Note 5)			0.8	V
Transmit Squelch Voltage Level (Tx+, Tx–)		–300	–250	–200	mV
Differential Output Voltage		±550		±1200	mV
Common Mode Output Voltage			4.0		V
Differential Output Voltage Imbalance			2	±40	mV

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Limits are guaranteed by 100% testing , sampling, or correlation with worst-case test conditions.
Note 3: Low Duty cycle pulse testing is performed at T_A.
Note 4: This does not include the current from the AUI pull down resistors or the LED output pins.
Note 5: LED drivers can sink up to 20mA, but V_{OL} will be higher.

ELECTRICAL CHARACTERISTICS (Continued)

AC ELECTRICAL CHARACTERISTICS

SYMBOLS	PARAMETER		MIN	TYP.	MAX	UNITS
TRANSMIT						
t_{TXNPW}	Transmit Turn-On Pulse Width			20		ns
t_{TXFPW}	Transmit Turn-Off Pulse Width			180		ns
t_{XODY}	Transmitter Turn-On Delay			50		ns
t_{TXSDY}	Transmit Steady State Prop. Delay			15		ns
RECEIVE						
t_{RXODY}	Receive Turn-On Delay			20		ns
t_{RXSDY}	Receive Steady State Prop. Delay			15		ns
t_{AR}	Differential Output Rise Time 20% to 80% (Rx±, COL±)			3		ns
t_{AF}	Differential Output Fall Time 20% to 80% (Rx±, COL±)			3		ns
COLLISION						
t_{CPSQE}	Collision Present to SQE Assert		0		200	ns
t_{SQEXR}	Time for SQE to Deactivate after a collision		0		500	ns
F_{CLF}	Collision Frequency	XTAL Controlled	8.5	10	11.5	MHz
	Collision Pulse Duty Cycle	XTAL Controlled	40	50	60	%
t_{SQEDY}	SQE Test Delay (Tx Inactive to SQE)		0.6	1.1	1.6	µs
t_{SQETD}	SQE Test Duration		0.5	1.0	1.5	µs
JABBER, LINK TEST AND LED TIMING						
t_{JAD}	Jabber Activation Delay		7	13.5	20	ms
t_{JSQE}	Delay from Outputs Disabled to Collision Oscillator On			100		ns
t_{LEDT}	REC, COLL, Tx1, Tx2, Tx3, Tx4 On Time		0.3	1.0	3.0	ms

TIMING DIAGRAMS

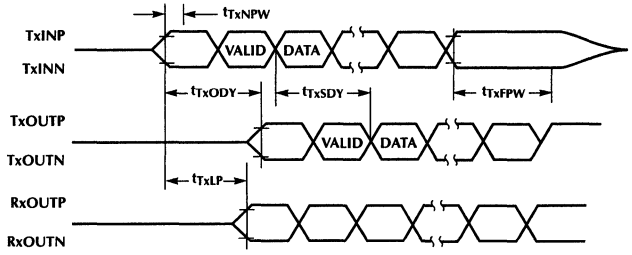


Figure 3. Transmit Timing

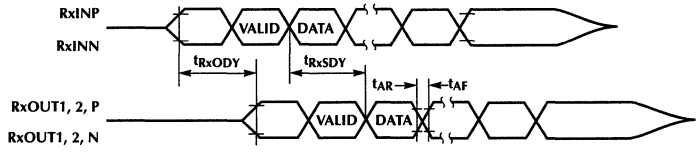


Figure 4. Receive Timing

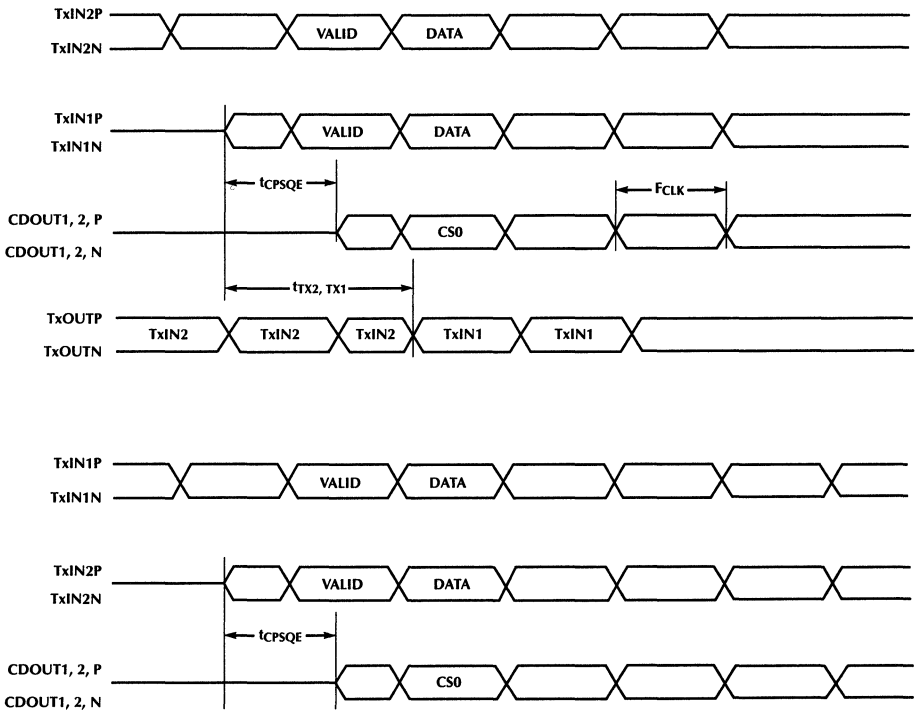


Figure 5. Collision Timing

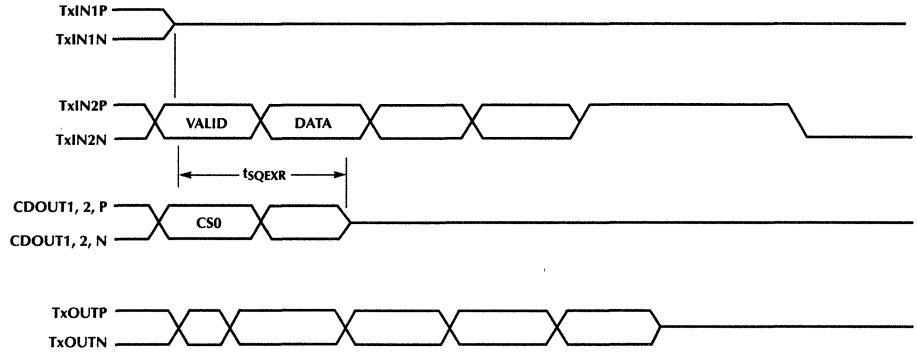


Figure 6. Collision Timing

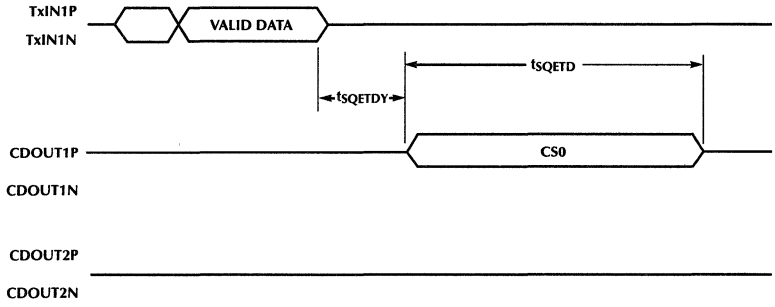


Figure 7. SQE Timing

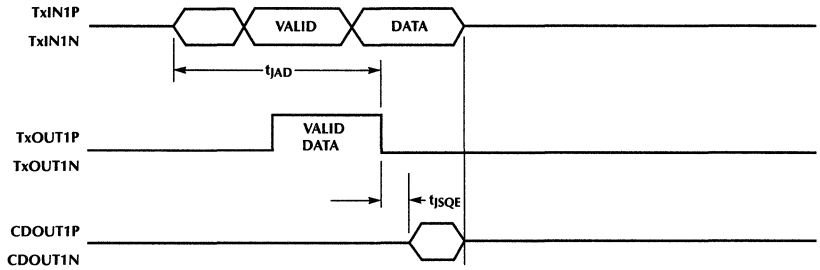


Figure 8. Jabber Timing

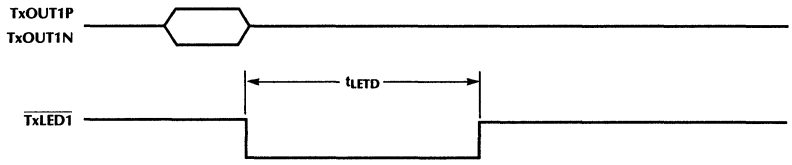


Figure 9. LED Timing

FUNCTIONAL DESCRIPTION

Figure 1 is a block diagram of a Four Port Multiplexer using the ML4644. All AUI interfaces are transformer coupled as required in an AUI connection.

RECEPTION

The receive function consists of detecting data on receive differential data input pair of the MAU port (RxIN) and transmitting this data out of the RxOUT ports of all the DTE port. This data will only be passed onto the DTE port if it meets the unsquelch criteria of the AUI receiver circuit. This provision prevents any noise on the AUI cable from being misinterpreted as data and transmitted to the RxOUT pins.

The receiver squelch circuit rejects signal typically with pulse width less than 20ns or a voltage level more positive than –250mV. Once the receiver is unsquelched, it remains so until reception of the idle signal which is more positive than –170mV for longer than 180ns.

TRANSMISSION

The transmit function consists of detecting data on any of the four differential data input pairs (TxIN1, TxIN2, TxIN3, and TxIN4) and transmitting this data out of the TxOUT pair of the MAU port. The loopback function of the MAU will loop the data back to the RxOUT port. The RxOUT port will treat the data as a received data and passes it on to all the DTE ports.

Only data that meets the unsquelch criteria of the AUI receiver circuit will be passed onto the TxOUT port.

COLLISION

There are two possible collision scenarios.

1. Collision from the network connected to the MAU.
2. Collision between two or more DTEs attached to the multiplexer.

In the case of a network collision, the MAU will send a collision presence signal to the multiplexer. The ML4644 will propagate this signal to the CDOUT pins of each of the DTE ports. The collision signal is a 10MHz ±0.01% signal.

When a collision event occurs between two or more DTE ports, the ML4644 will send the collision presence signal to each of the DTEs via the collision ports. At the same time a 5MHz JAM signal is sent to the network.

SQE TEST FUNCTION

The Signal Quality Error (SQE) test function allows the DTE to determine whether or not the collision port is functional. After each transmission, during the interpacket gap time, the collision signal will be activated on the CDOUT port of the same DTE port data has been transmitted, for typically 1 µs. The SQE function is not activated at the DTE ports that are in jabber state. The SQE function of each port can be disabled by tying the SQEN pin low.

JABBER FUNCTION

The jabber function prevents a malfunction transmitter from continuous transmission and thus loaded down the network. Within the ML4644, there is a jabber timer. The timer starts at the beginning of a received packet and resets at the end of each packet. If the packet lasts longer than 7 to 20ms the jabber circuit will disable the offending TxIN receiver (the transmission of excessively long packet is thus terminated) and generates a collision signal to the collision port of the offending DTE port. The DTE port will exit the jabber state when the transmission goes idle.

LED DRIVERS

The ML4644 has ten LED drivers. Each DTE port has a transmit LED and a jabber LED and the MAU port has a receive LED. Additionally there is a collision LED which indicates the presence of a collision condition. All LED drivers are active low open collector driver.

All LED drivers except the jabber have pulse 1ms pulse stretchers. The pulse stretchers provide adequate on time for the LED to be visible.

CASCADING THE ML4644 FOR EIGHT PORT MULTIPLEXER APPLICATION

An 8 port multiplexer can be realized by using two ML4644s and one ML4642. In this configuration (see fig. 2), the SQE function of the ML4642 should be disabled to prevent false collision signalling. The SQE function in this configuration is performed by each DTE port of the ML4644 independently.

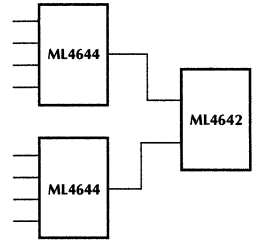


Figure 2. Block Diagram of an Eight port Multiplexer.

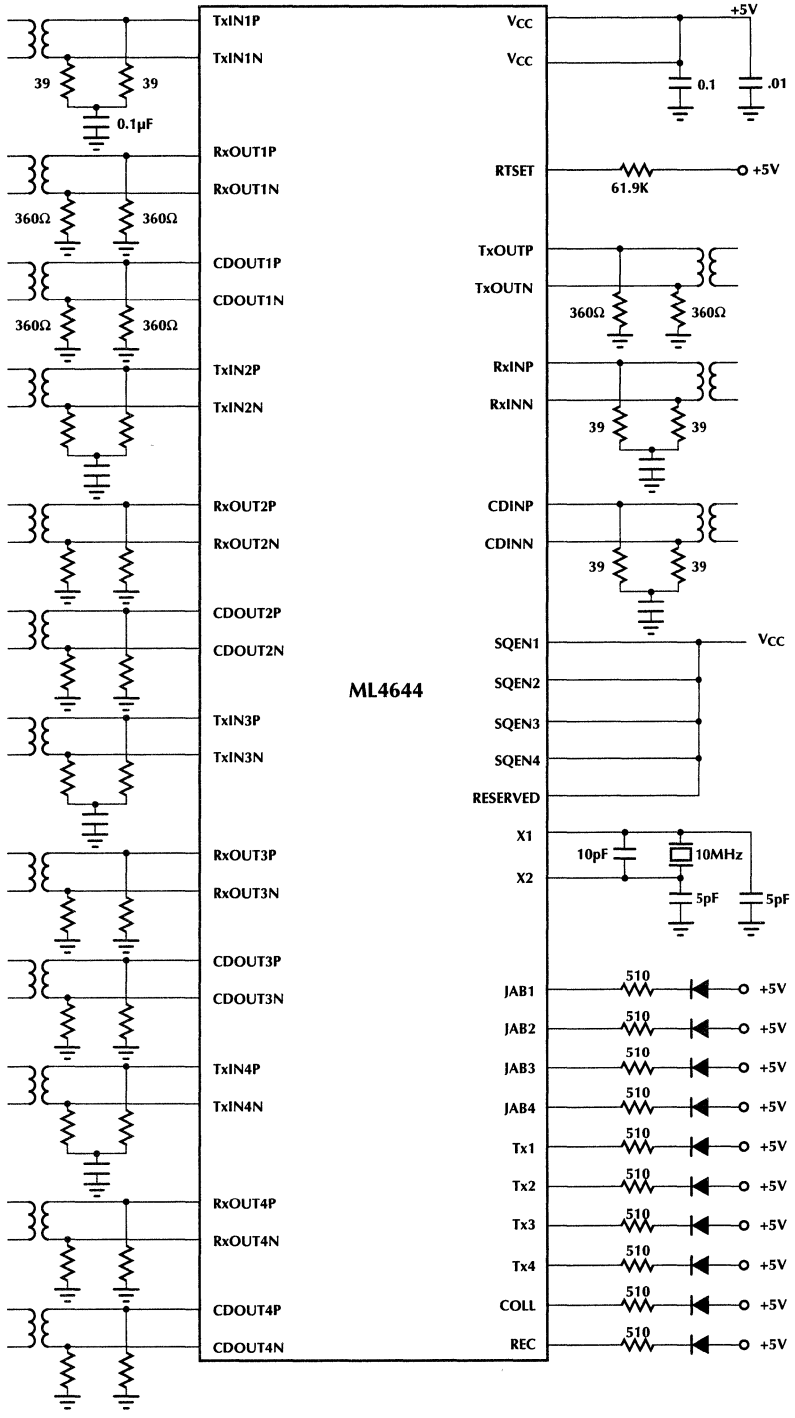


Figure 1. Four Port AUI Multiplexer.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4644CQ	0°C to 70°C	68-Pin PLCC (Q68)

ML4652, ML4658

10BASE-T Transceiver

GENERAL DESCRIPTION

The ML4652/ML4658 10BASE-T Transceivers are single chip cable line driver/receivers that provides all of the functionality required to implement both an internal and external IEEE 802.3 10BASE-T MAU. These parts offer a standard IEEE 802.3 AU interface that allows them to directly connect to industry standard manchester encoder/decoder chips or an AUI cable.

These parts require a minimal number of external components, and are compliant to the IEEE 802.3 10BASE-T standard. The differential current driven transmitter offers superior performance because of its highly symetrical switching. This results in low RFI noise and low jitter.

The Transceiver easily interfaces to 100Ω unshielded twisted pair cable, 150Ω shielded twisted pair cable, or a range of other characteristic impedances by simply changing one external resistor. Jabber, Link Test, and SQE Test are fully integrated onto the chip with enable/disable options. A polarity detection status pin, which can drive an LED, is provided for receive data, and the ML4658 offers automatic polarity correction.

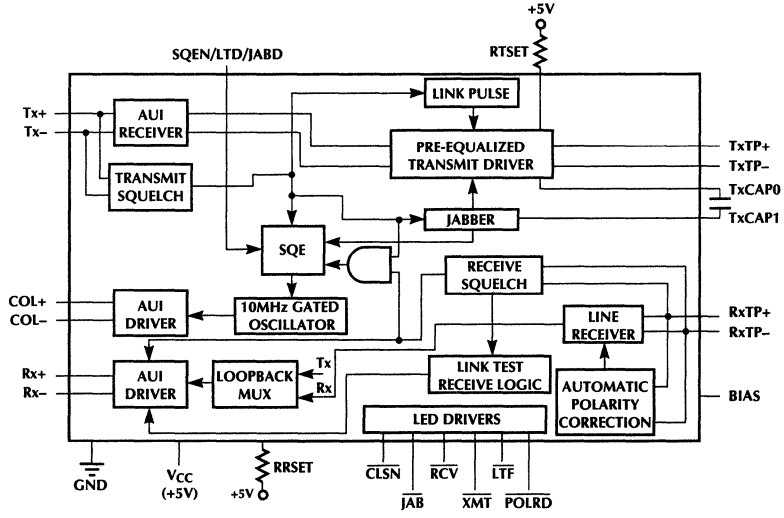
The ML4652 and ML4658 are available in 24 pin skinny DIP as well as a 28 pin PLCC.

FEATURES

- Complete implementation of IEEE 802.3 10BASE-T Medium Attachment Unit (MAU)
- Incorporates an AU interface for use in an external MAU or internal MAU
- Single +5 volt supply ±10%
- No crystal or clock input
- Current Driven Output for low RFI noise and low jitter
- Capable of driving 100Ω unshielded twisted pair cable or 150Ω shielded twisted pair cable
- Polarity detect status pin capable of driving an LED
- Automatic Polarity Correction on the ML4658
- On-chip Jabber logic, Link Test, and SQE test with enable/disable option
- ML4652 and ML4658 provide six network status LED ouput pins
- ML4652 and ML4658 are available in a 24-pin skinny DIP or 28-pin PLCC
- Semi-standard option using Micro Linear's FB3651 LAN Transceiver Tile Array

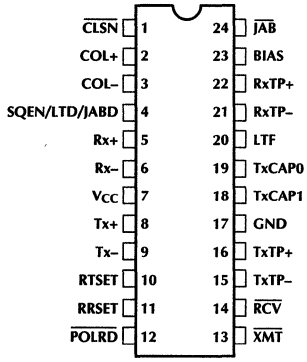
4

BLOCK DIAGRAM



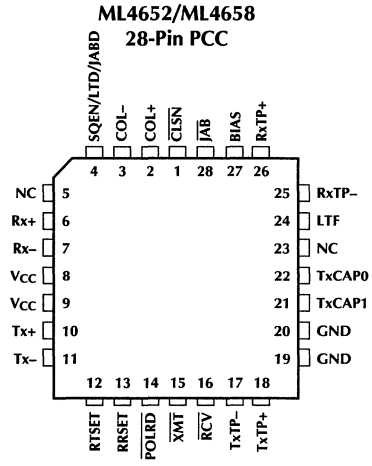
PIN CONFIGURATION

ML4652/ML4658
24-Pin DIP



TOP VIEW

ML4652/ML4658
28-Pin PCC



TOP VIEW

PIN DESCRIPTION (DIP)

PIN#	NAME	FUNCTION
1	$\overline{\text{CLSN}}$	Indicates that a collision is taking place. Active low LED driver, open collector. Event is extended 100ms for visibility.
2 3	COL+ COL–	Gated 10MHz signal used to indicate a collision, SQE test, or jabber. Balanced differential line driver outputs that meet AU interface specifications. AC or DC coupled.
4	SQEN/LTD/ JABD	SQE Test Enable, Link Test Disabled, Jabber Disabled. This input uses four voltage levels to configure the chip as shown in Table 1.

Table 1. SQEN/LTD/JABD Pin Configuration

Pin	SQE Test	Link Test	Jabber
0V (GND)	Disabled	Enabled	Enabled
1.2V	Disabled	Disabled	Disabled
BIAS	Enabled	Disabled	Enabled
5V (V_{CC})	Enabled	Enabled	Enabled

When link test is disabled, no link pulses are transmitted, and the transmitter and receiver will not be disabled as a result of a loss of receive link pulses. When Jabber is disabled the transmitter can transmit continuously without interruption, and the collision oscillator will not be activated.

5 6	Rx+ Rx–	Manchester encoded receive data output to the local device. Balanced differential line driver outputs that meet AU interface specifications. AC or DC coupled.
7	V_{CC}	+5 Volt power input.
8 9	Tx+ Tx–	Balanced differential line receiver inputs that meet AU interface specifications. These inputs may be AC or DC coupled. When AC coupled, the BIAS pin is used to set the common mode voltage. Signals meeting the transmitter squelch input requirements are pre-equalized and output on TxTP+ and TxTP–.
10	RTSET	When using 100Ω unshielded twisted pair, a 220Ω resistor is tied between this pin and V_{CC}. When using 150Ω shielded twisted pair, a 330Ω resistor is tied between this pin and V_{CC}.
11	RRSET	A 1% 61.9KΩ resistor tied from this pin to V_{CC} is used for internal biasing.

PIN DESCRIPTION (DIP) (Continued)

PIN#	NAME	FUNCTION
12	$\overline{\text{POLRD}}$	Receive Polarity status. Active low LED Driver, open collector output. Indicates the polarity of the receive twisted pair regardless of auto polarity correction. When this pin is high, the receive polarity is correct, and when this pin is low the receive polarity is reversed.
13	$\overline{\text{XMT}}$	Indicates that transmission is taking place on the TxTP+, TxTP– pair. Active low LED driver, open collector. It is extended 100ms for visibility.
14	$\overline{\text{RCV}}$	Indicates that the transceiver has unsquelched and is receiving data from the twisted pair. Active low LED driver, open collector. It is extended 100ms for visibility.
15	TxTP–	Pre-equalized differential balanced current driven output. These ouputs are connected to a balanced transmit output filter which drives the twisted pair cable through pulse transformers. The output current is set with an external resistor connected to RTSET allowing the chip to drive 100Ω unshielded twisted pair, 150Ω shielded twisted pair cables or a range of other characteristic impedances.
16	TxTP+	
17	GND	Ground reference.
18	TxCAP1	An external capacitor of 330pF is tied between these two pins to set the pulse width for the pre-equalization on the transmitter. If these two pins are shorted together, no pre-equalization occurs.
19	TxCAP0	
20	LTF	Link Test Fail. Active high. Normally this pin is low, indicating that the link is operational. If the link goes down resulting from the absence of link pulses or frames being received, the chip will go into the Link Test Fail state and bring LTF high. In the Link Test Fail state, both the transmitter and receiver are disabled, however link pulses are still sent. A station that only has access to the AUI can detect a Link Test Fail by the absence of loopback. This pin is low when the Link Test is disabled. Open collector LED output.
21	RxTP–	Twisted Pair receive data input. When this signal exceeds the receive squelch requirements the receive data is buffered and sent to the Rx± outputs.
22	RxTP+	
23	BIAS	Bias voltage, output. Used to bias the receive twisted pair inputs as well as the Tx± inputs when they are AC coupled.
24	$\overline{\text{JAB}}$	Open collector TTL output capable of driving an LED. When in the Jabber state, this pin will be low and the transmitter will be disabled. In the Jabber "OK" state this pin will be high.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- V_{CC} ..... –0.3 to 6V

Input Voltage Range
- Digital Inputs (SQEN, LTD) ..... –0.3 to V_{CC}
- Tx+, Tx–, RxTP+, RxTP– ..... –0.3 to V_{CC}

Input Current
- RRSET, RTSET, $\overline{JAB}$, $\overline{CLSN}$, $\overline{XMT}$, $\overline{RCV}$, LTF 60mA

Output Current
- TxTP+, TxTP– 80mA

Storage Temperature ..... –65°C to +150°C

Lead Temperature (Soldering 10 sec.) ..... 260°C

OPERATING CONDITIONS

(Note 2)

Supply Voltage (V_{CC}) ..... 5V ±10%

LED on Current 10mA

RRSET ..... 61.9KΩ ±1%

RTSET ..... 220Ω ±1%

TxCAP 330pF

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 0°C to 70°C (Note 3), VCC = 5V ±10%

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current I_{CC} (Note 4)	V_{CC} = 5V			140	mA
LED Drivers: V_{OL}	R_L = 510Ω (Note 5)			0.8	V
Transmit Peak Output Current	RTSET = 220Ω		42 (Note 6)		mA
Transmit Squelch Voltage Level (Tx+, Tx–)			–170		mV
Differential Input Voltage (RxTP+, RxTP–)		±0.300		±3.1	V
Receiver Input Resistance		10			KΩ
SQEN/LTD/JABD Input Resistance			12		KΩ
Receive Squelch Voltage Level (RxTP+, RxTP–)		300	450	585	mV-p
Differential Output Voltage (Rx±, COL±)		±550		±1200	mV
Common Mode Output Voltage (Rx±, COL±)			4.0		V
Differential Output Voltage Imbalance (Rx±, COL±)			2	±40	mV
BIAS Voltage			3.2		V
SQEN/LTD/JABD	SQE TEST disabled All disabled Link Test Disabled All Enabled	 1.1 BIAS – 0.15 V_{CC} – 0.05V		0.3 1.4 BIAS + 0.15	V

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Low Duty cycle pulse testing is performed at T_A.

Note 4: This does not include the current from the AUI pull down resistors, the transmit pins TxTP+ and TxTP– or the LED output pins.

Note 5: LED drivers can sink up to 20mA, but VOL will be higher.

Note 6: This current will result in a 2.5V peak output voltage on unshielded twisted pair cable when connected through an external filter and transformer as shown in Figure 12.

ELECTRICAL CHARACTERISTICS (Continued)

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Transmit					
t_{TXNPW}	Transmit Turn-On Pulse Width	20		ns	
t_{TXFPW}	Transmit Turn-Off Pulse Width	180		ns	
t_{TXLP}	Transmit Loopback Startup Delay			200	ns
t_{TXODY}	Tranmitter Turn-On Delay			200	ns
t_{TXSDY}	Transmit Steady State Prop. Delay		15	100	ns
t_{TXJ}	Transmitter Jitter		±2	±3.5	ns
Receive					
t_{RXODY}	Receive Turn-On Delay if Transmit is Idle		420	500	ns
t_{RXTDY}	Receive Turn-On Delay if Tranmit is Active		650	800	ns
t_{RXFX}	Last Bit Received to Start Slow Decay Output	230	800		ns
t_{RXSDY}	Receive Steady State Prop. Delay		15	100	ns
t_{RXJ}	Receiver Jitter		±0.7	±1.5	ns
t_{AR}	Differential Output Rise Time 20% to 80% (Rx±, COL±)		3		ns
t_{AF}	Differential Output Fall Time 20% to 80% (Rx±, COL±)		3		ns
Collision					
t_{CPSQE}	Collision Present to SQE Assert 0		900	ns	
t_{TXRX}	Time for Loopback to swtich from Tx to RxTP during a collision	0		900	ns
t_{SQEXR}	Time for SQE to deactivate given that RxTP goes idle and TxTP continues	0		900	ns
t_{SQEXT}	Time for SQE to deactivate given thata TxTP goes idle and RxTP continues	0		900	ns
t_{CLF}	Collision Frequency	8.5	10	11.5	MHz
t_{CLPDC}	Collision Pulse Duty Cycle	40	50	60	%
t_{SQEDY}	SQE Test Delay (Tx Inactive to SQE)	0.6	1.1	1.6	µs
t_{SQETD}	SQE Test Duration	0.5	1.0	1.5	µs
Jabber, Link Test and LED Timing					
t_{JAD}	Jabber Activation Delay	20	70	150	ms
t_{JRT}	Jabber Reset Unjab Time	250	450	750	ms
t_{JSQE}	Delay from Outputs Disabled to Collision Oscillator On		100		ns
t_{LLT}	Link Loss Time	50	95	150	ms
t_{LTN}	Link Test Pulse Receive Minimum Time	2	4.2	7	ms
t_{LTX}	Link Test Pulse Receive Maximum Time	25	70	150	ms
t_{TLP}	Link Test Pulse Repetition Rate 8	16	24	ms	
t_{LTPW}	Link Test Pulse Width	85	100	200	ns
t_{LEDT}	$\overline{XMT}$, $\overline{RCV}$, $\overline{CLSN}$ On Time	30	100	300	ms

TIMING DIAGRAMS

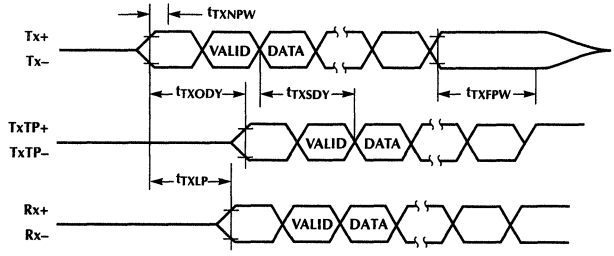


Figure 1. Transmit and Loopback Timing

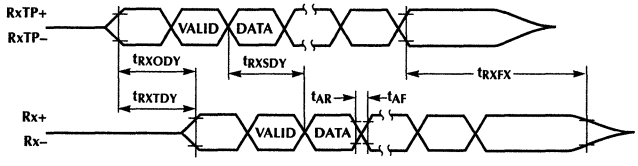


Figure 2. Receive Timing

TIMING DIAGRAMS (Continued)

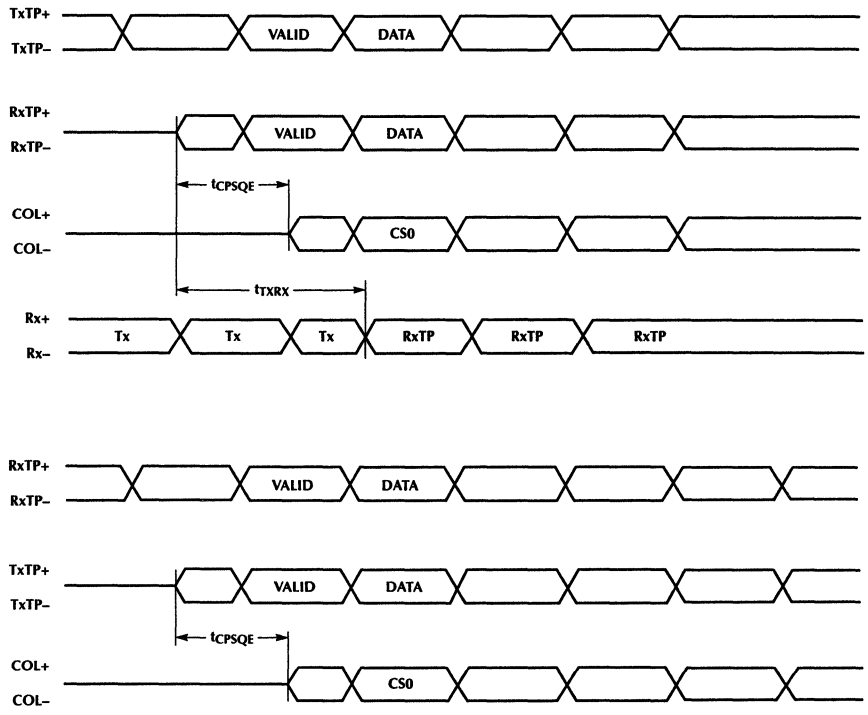


Figure 3. Collision Timing

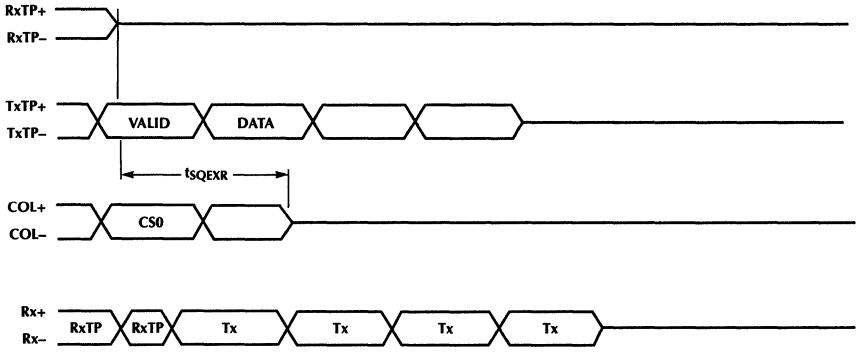


Figure 4. Collision Timing

TIMING DIAGRAMS (Continued)

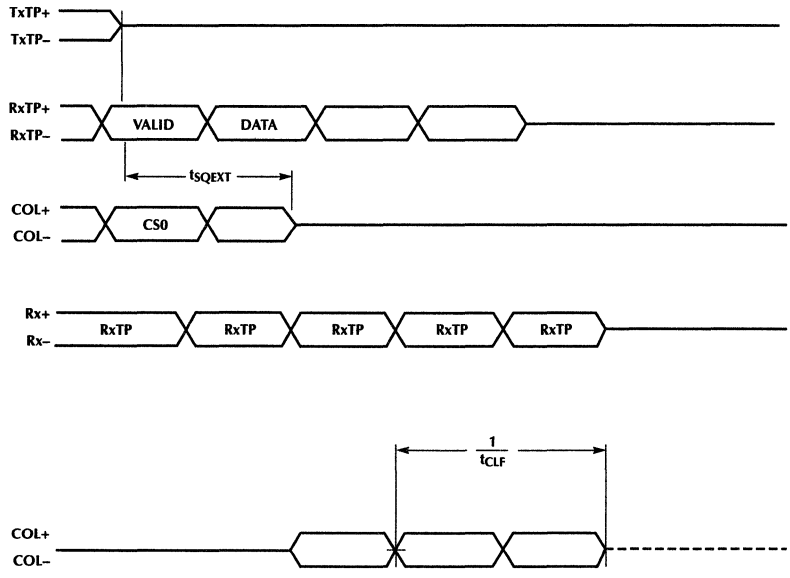


Figure 5. Collision Timing

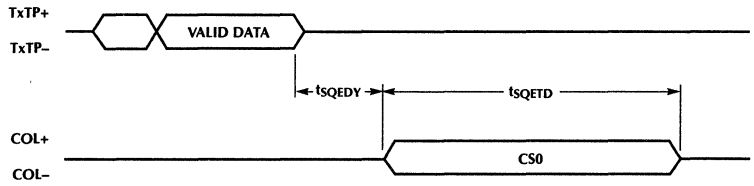


Figure 6. SQE Timing

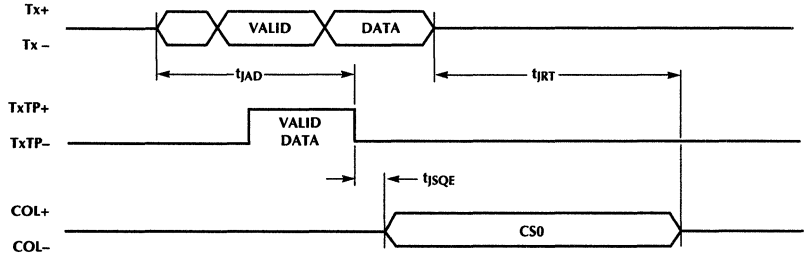


Figure 7. Jabber Timing

TIMING DIAGRAMS (Continued)

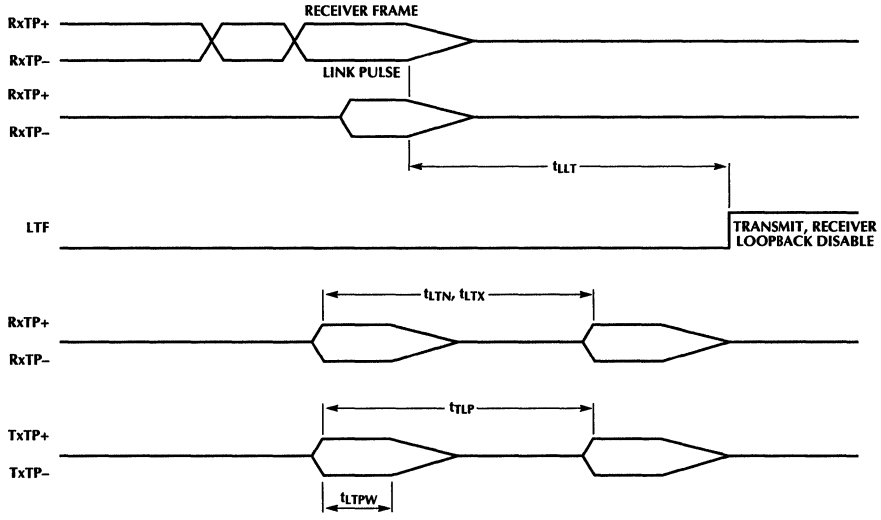


Figure 8. Link Pulse Timing

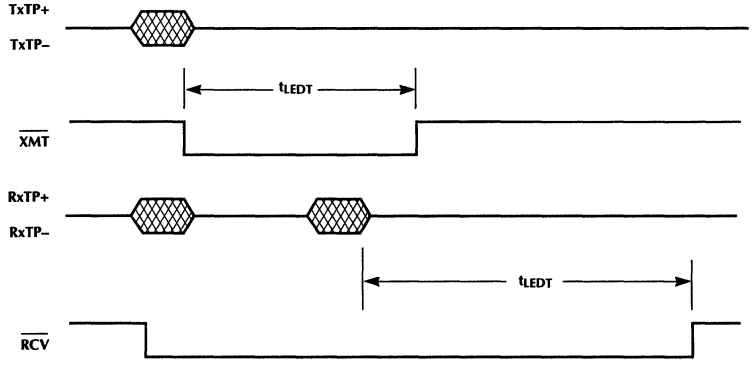


Figure 9. LED Timing

SYSTEM DESCRIPTION

Figure 10 shows a typical block diagram of an external 10BASE-T transceiver interface. On one side of the transceiver is the AU interface and the other is the twisted pair. The AU interface is AC coupled when used in an external transceiver or can be AC or DC coupled when used in an internal transceiver. The AU interface for an external transceiver includes isolation transformers, some biasing resistors, and a voltage converter for power.

The twisted pair side of the transceiver requires external transmit and receive filters, isolation transformers, and terminating resistors. These components can be obtained in a single hybrid package from suppliers listed in figure 12. The transmitter sends pre-equalized data through the transmit filters onto the twisted pair. The pre-equalized data uses a standard two step output waveform that lowers the amplitude of the 5MHz component so that at the receiving end both the 5MHz and 10MHz components have the same amplitude. The external transmit filter smooths the edges of the signal before passing it onto the twisted pair.

The receive pair side of the transceiver accepts the data after it passes through the isolation transformer and the receive low pass filter. Since this is an AC coupled input, the Bias pin is used to set the proper common mode voltage for the receive inputs. A pair of 50Ω resistors correctly terminate the receive pair and provide a common mode for the Bias voltage connection point.

AU INTERFACE

The AU interface consists of 3 pair of signals, DO, CI and DI as shown in Figure 10. The DO pair contains transmit data from the DTE which is received by the transceiver and sent out onto the twisted pair. The DI pair contains valid data that has been either received from the twisted pair or looped back from the DO and output through the DI pair to the DTE. The CI pair indicates whether a transmit based collision has occurred. It is an output that oscillates at 10MHz. CI pair is also used for Jabber and SQE Test.

The transceiver may be AC or DC coupled depending on the application. For the AC coupled interface, the DO input must be DC biased (shifted up in voltage) for the proper common mode input voltage. The BIAS pin serves this purpose. When DC coupled, the manchester encoder/decoder transmit output pair provides this common mode voltage and the Bias pin is not connected.

The two 39Ω 1% resistors tied to the Tx+ and Tx– pins serve two purposes. They provide a point to connect the common mode bias voltage, and they provide the proper matching termination for the AUI cable. The CI and DI pair, which are output drivers from the transceiver to the AUI cable, require 360Ω pull down resistors when terminated with a 78Ω load. However on a DTE card, CI and DI do not need 78Ω terminating resistors. This also means that the pull down resistors on CI and DI can be 1KΩ or greater depending upon the particular manchester encoder/decoder chip used.

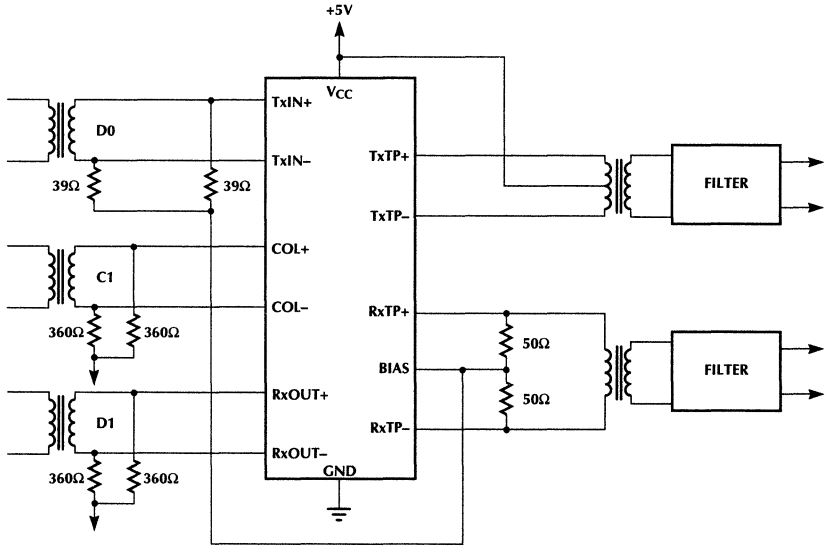


Figure 10. System Block Diagram

The AUI drivers are capable of driving the full 50 meters of cable length and have a rise and fall time of typically 3ns. The rise and fall times match to within 1ns. In the idle state, the outputs go to the same voltage to prevent DC standing current in the isolation transformers.

TRANSMISSION

The transmit function consists of detecting the presence of data from the AUI DO input (Tx+, Tx–) and driving that data onto the transmit twisted pair (TxTP+, TxTP–). A positive signal on the Tx+ lead relative to the Tx– lead of the DO circuit will result in a positive signal on the TxTP+ lead of the chip with respect to the TxTP– lead.

Before data will be transmitted onto the twisted pair from the AU interface, it must exceed the squelch requirements for the DO pair. The Tx squelch circuit serves the function of preventing any noise from being transmitted onto the twisted pair. This circuit rejects signals with pulse widths less than typically 20ns and voltage levels more positive than –175mV. Once the Tx squelch circuit has unsquelched, it looks for the start of idle signal to turn on the squelch circuit again. The transmitter turns on the squelch again when it receives an input signal at Tx± that is more positive than –175mV for more than approximately 180ns.

At the start of a packet transmission, no more than 2 bits are received from the DO circuit and not transmitted onto the twisted pair. The difference between start-up delays (bit loss plus steady-state propagation delay) for any two packets that are separated by 9.6µs or less will not exceed 200ns.

The output stage of the transmitter is a current mode switch which develops the output voltage by driving current through the terminating resistor and the output filter. The transmitter employs a center tap 2:1 transformer where the center tap is tied to V_{CC} (+5V). While one pin of the transmit pair (TxTP+, TxTP–) is pulled low, the other pin floats. The output pins to the twisted pair wires, TxTP+ and TxTP–, can drive a 100Ω, 150Ω load, or a variety of impedances that are characteristic of the twisted pair wire. RTSET selects the current into the TxTP+, TxTP– pins. This current along with the characteristic impedance of the cable determines the output voltage.

Once the characteristic impedance of the twisted pair is determined, one must select the appropriate RTSET resistor as well as match the terminating impedances of the transmit and receive filter. The RTSET resistor can be selected as follows:

$$RTSET = (R_L/100) \times 220\Omega$$

where R_L is the characteristic impedance of the twisted pair cable.

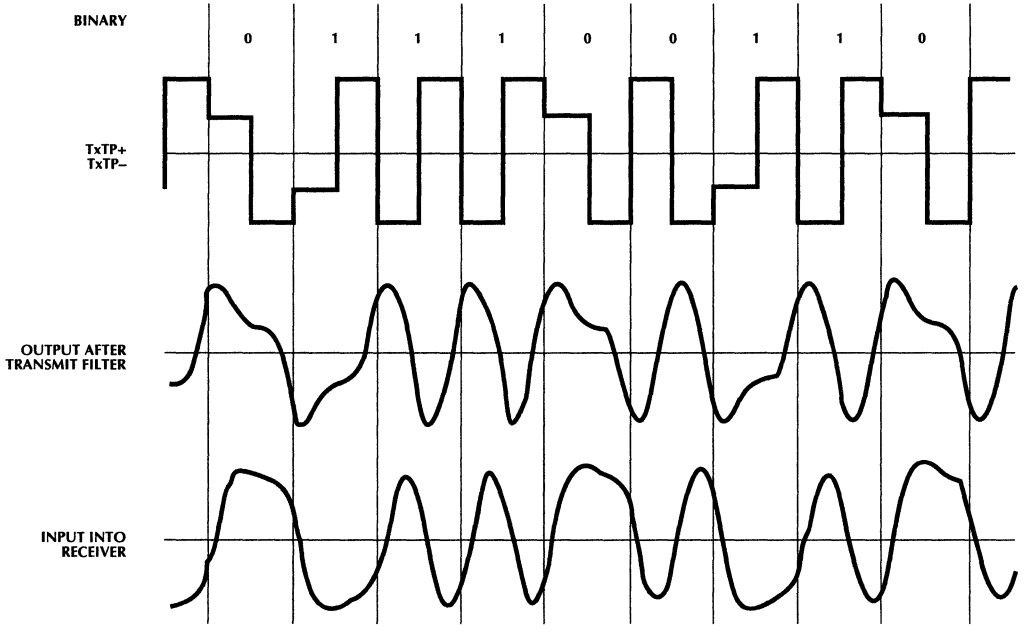


Figure 11. Transmit Pre-Equalization Waveform

The transmitter incorporates a pre-equalization circuit for driving the twisted pair line. Pre-equalization compensates for the amplitude and phase distortion introduced by the twisted pair cable. The twisted pair line will attenuate the 10MHz signal more than the 5MHz signal. Therefore pre-equalization insures that both the 5 and 10MHz components will be roughly the same amplitude at the far end receiver.

The pre-equalization circuit reduces the current output when a 5MHz bit is being transmitted. After 50ns of a 5MHz bit, the current level is reduced to approximately 2/3 of its peak for the remaining 50ns. Figure 11 illustrates the pre-equalization.

An on-chip one-shot determines the pulse width of the pre-equalized transmit signal. This requires an external capacitor connected to pins TxCAP0 and TxCAP1. The proper value for this one-shot is 330pF. Pre-equalization can be disabled by shorting TxCAP0 and TxCAP1 together.

The transmitter enters the idle state when it detects start of idle on Tx+ and Tx– input pins. The transmitter maintains a minimum differential output voltage of at least 450mV for 250ns after the last low to high transition. The driver differential output voltage will then be within 50mV of 0V within 45 bit times.

RECEPTION

The twisted pair receive data is transformer coupled and low pass filtered before it is fed into the input pins RxTP±. The input is differential with the common mode voltage set by the chip's Bias pin. At the start of packet reception from the twisted pair link, no more than 5 bits are received from the twisted pair cable and not transmitted onto the DI circuit. The first bit sent on the DI circuit may contain phase violations or invalid data, but all subsequent bits are valid.

The receive squelch will reject the following signals on the RxTP+ and RxTP– inputs:

1. All signals that produce a peak magnitude less than 300mV.
2. All continuous sinusoidal signals of amplitude less than $6.2V_{P\_P}$ and frequency less than 2MHz.
3. All single sinusoidal cycles of amplitude less than $6.2V_{P\_P}$ and either polarity, where the frequency is between 2MHz and 15MHz. For a period of 4 BT before and after this single cycle, the signal will conform to (1) above.
4. All sinusoidal cycles gated by a 100ns pulse gate of amplitude less than $6.2V_{P\_P}$ and either polarity, where the sinusoidal frequency is between 2MHz and 30MHz. The off time of the pulse gate on the sinusoidal signal shall be at least 400ns.

The first three receive squelch criteria are required to conform to the 10BASE-T standard. The fourth receive squelch criteria exceeds the 10BASE-T requirements and enhances the performance of the receiver. The fourth squelch criteria prevents a false unsquelch caused by cross talk or noise typically found coupling from the phone lines onto the receive twisted pair.

When the receive squelch is on during idle, the input voltage must exceed approximately ±450mV peak several times before unsquelch occurs. If the transmitter is inactive, the receiver has up to 5 bit times to unsquelch and output the receive data on the Rx+, Rx– pair. If the transmitter is active, the receive squelch extends the time it takes to determine whether to unsquelch. If the receiver unsquelches while the transmitter is active, a collision will result. Therefore the receive squelch uses the additional time to insure that a collision will not be reported as a result of a false receive squelch.

After the receiver is unsquelched, the detection threshold is lowered to 275mV. Upon passing the receive squelch requirements the receive data propagates into the multiplexer and eventually passes to the Rx+ and Rx– outputs of the AU interface. The addition of jitter through the receive section is no more than ±1.5ns.

While in the unsquelch state, the receive squelch circuit looks for the start of idle signal at the end of the packet. When start of idle is detected, receive squelch is turned on again. The proper start of idle occurs when the input signal remains above 300mV for 160ns. Nevertheless, if no transitions occur for 160ns, receive squelch is still turned on.

COLLISION

Whenever the receiver and the transmitter are active at the same time the chip will activate the collision output. The collision output is a differential square wave matching the AUI specifications and capable of driving a 78Ω load. The frequency of the square wave is 10MHz ±15% with a 60/40 to 40/60 duty cycle. The collision oscillation turns on no more than 9 bit times after the collision condition begins, and turns off no more than 9 bit times after the collision condition is removed. The collision oscillator also is activated during SQE Test and Jabber.

LOOPBACK

The loopback function emulates a coax Ethernet transceiver where the transmit data sent by the DTE is looped back over the AUI receive pair. Many LAN controllers report the status of the carrier sense for each packet transmitted. The software can use this loopback information to determine whether a MAU is connected to the DTE by checking the status of carrier sense after each packet transmission.

When data is received by the chip while transmitting, a collision condition exits. This will cause the collision oscillator to turn on within 9 bit times. The data on the DI AUI pair (Rx+, Rx–) changes from Tx+, Tx– to RxTP+, RxTP–, when entering the collision state. During a collision, if the receive data (RxTP+, RxTP–) drops out before the transmit data (Tx+, Tx–), Rx+, Rx– will switch back to Tx+, Tx–.

SQE TEST FUNCTION (SIGNAL QUALITY ERROR)

The SQE test function allows the DTE to determine whether the collision detect circuitry is functional. After each transmission, during the inter-packet gap time, the collision oscillator will be activated for typically 1µs. The SQE test will not be activated if the chip is in the link fail state, or the Jabber state.

For SQE to operate, the SQEN pin must be tied to V_{CC} or BIAS. The SQE test can be disabled by tying the SQEN pin to 1.2V or ground. This allows the chip to be interfaced to a repeater.

JABBER FUNCTION

The Jabber function prevents a babbling transmitter from bringing down the network. Within the transceiver is a Jabber timer that starts at the beginning of each transmission and resets at the end of each transmission. If the transmission lasts longer than 20ms the jabber logic disables the transmitter, and turns on the collision oscillator COL+, COL–. When Tx+ and Tx– finally go idle, a second timer measures 0.5 seconds of idle on Tx+ and Tx– before re-enabling the transmitter and turning off the collision oscillator. If transmission starts up again before 0.5 seconds has expired, the timer is reset and measures another 0.5 seconds of idle time.

Even though the transmitter is disabled during jabber, Link Pulses are still transmitted if the, Link Test is enabled.

Jabber can be disabled by placing 1.2V on the SQEN/LTD/JABD pin. This is useful for measuring jitter performance on the transmitter.

LINK TEST FUNCTION

Transmission — Whenever data is not being delivered to the twisted pair link, the idle signal is applied. The idle signal is a sequence of Link Pulses separated by a 16ms period of silence. The idle signal starts with a period of silence after a packet transmission ends. The link test pulse is a single high pulse with the same amplitude requirements as the data signal.

Reception — The transceiver monitors the receive twisted pair input for packet and link pulse activity. If neither a packet nor a link test pulse is received for 50 to 150ms, the transceiver enters the Link Test Fail state and inhibits transmission and reception. Link pulses received with the wrong polarity will be ignored and cause the chip to go into link test fail.

A DTE can determine that the transceiver is in Link Test Fail one of two ways: it can monitor the LTF pin if the transceiver is internal, or it can monitor loopback. If the MAU is on-board the LTF pin can be sampled to determine that the transceiver is in the link fail state. If the MAU is external the DTE can monitor carrier sense during transmission. A loss of carrier sense is an indication of Link Test Fail State, since in Link Test Fail, loopback is disabled. Note that jabber also disables loopback but with Jabber the collision signal will be on.

When a packet, or two consecutive link test pulses is received from the twisted pair input, the transceiver will exit the Link Test Fail state upon transmit and receive data being idle, and re-enable transmission and reception.

Link test pulses that do not occur within at most 25 to 150ms of each other are not considered consecutive. In addition, detected pulses that occur within a time between 2 to 7ms of a previous pulse will be considered as noise by the link test circuitry.

POLARLITY CIRCUITRY

The ML4652 offers polarity detection, while the ML4658 offers automatic polarity correction. The ML4652 and ML4658 are pin for pin compatible. The $\overline{\text{POLRD}}$ pin is used to report the status of the receive pair polarity. This pin reflects the true status of the receive polarity regardless of whether the part has autopolarity correction or not.

Polarity Detection — ML4652 — The internal circuitry uses the start of idle signal to determine the receive polarity. With the correct receive polarity, the Start of Idle signal (the end of the frame) will remain above 300mV for more than 160ns. If the polarity is reversed, the Start of Idle signal will end with a negative voltage.

The $\overline{\text{POLRD}}$ status pin is updated only when two consecutive frames are received with the same Start of Idle polarity. In the case where the part is powered up with the receive polarity reversed and no frames are received, the part will go into link test fail without reflecting a reverse polarity condition. Without autopolarity correction, the part will remain in link test fail unless a frame is received or the correct polarity link pulses are received.

Automatic Polarity Correction — ML4658 — In the link OK state, receive polarity is updated when two consecutive frames are received with the same Start of Idle polarity. In the Link Test Fail state the part will use either the Start of Idle signal or link pulses to correct the receive polarity.

In the case where the part is powered up with the receive polarity reversed and no frames are received, the part will go into Link Test Fail. After two link pulses are received with the same polarity, the part will exit Link Test Fail and correct the receive polarity. The $\overline{\text{POLRD}}$ pin will continue to reflect the true polarity of the receive pair.

LED DRIVERS

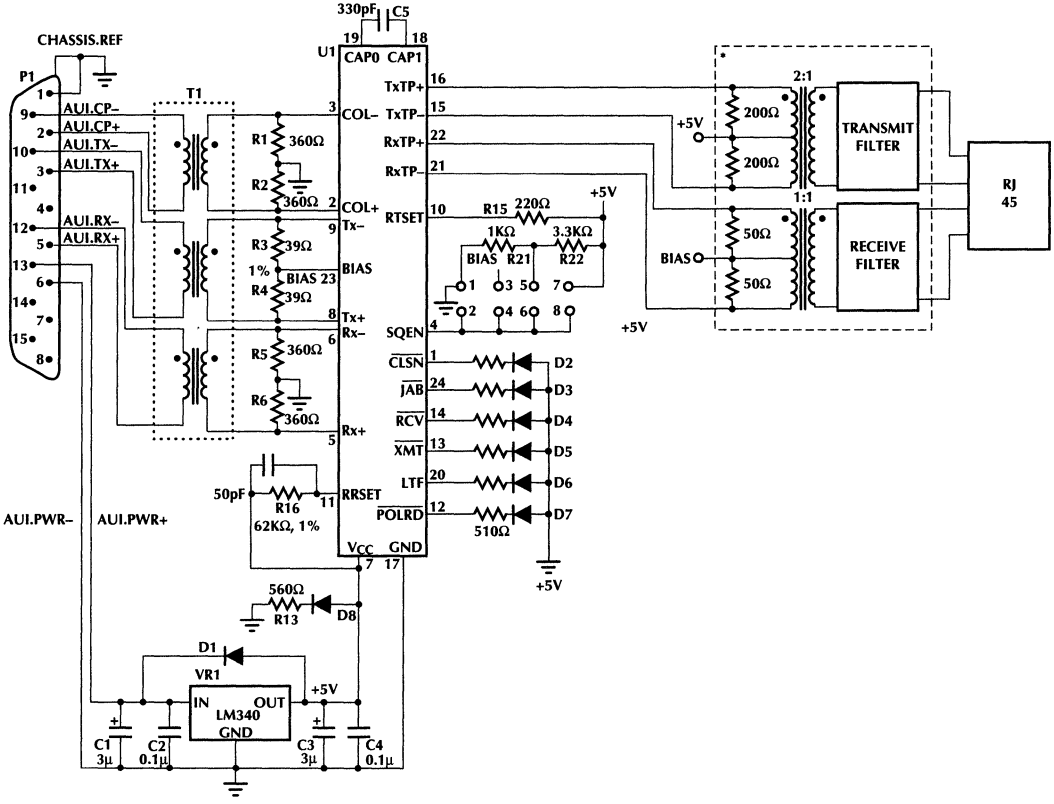
The ML4652, ML4658 have six LED drivers for transmit, receive, collision, Link Test Fail, reverse polarity, and jabber. The LEDs are normally off except for LTF which is normally on and active high. The LEDs are tied to their respective pins through a 510Ω resistor to 5 Volts.

The $\overline{\text{XMT}}$, $\overline{\text{RCV}}$ and $\overline{\text{CLSN}}$ pins have pulse stretchers on them which enables the LEDs to be visible. When transmission or reception occurs, the LED $\overline{\text{XMT}}$, $\overline{\text{RCV}}$ or $\overline{\text{CLSN}}$ status pins will activate low for 100ms. If another transmit, receive or collision condition occurs during the first 100ms, the LED timer will reset and begin timing again for 100ms. The LEDs will remain on for consecutive frames. The $\overline{\text{JAB}}$, $\overline{\text{POLRD}}$, and LTF LEDs do not have pulse stretchers on them since their conditions occur long enough for the eye to see.

SEMI-STANDARD OPTION

The ML4652 and ML4658 are designed using Micro Linear's Bipolar Tile Array technology. They use a special Tile Array, the FB3651, that was designed for Data Communications applications. As a result these parts are customizable, and can be modified to suit a specific customer application. Please contact your local representative or Micro Linear for more information on semi-standard options.

APPLICATION: EXTERNAL MAU



* Single Chip Solutions are Available from Magnetic Suppliers.

Magnetics and Filter Suppliers·
Pulse Engineering, Inc (San Diego)
Valor Electronics, Inc. (San Diego)
Fil-Mag (San Diego)

Figure 12. External MAU

4

APPLICATION: INTERNAL MAU

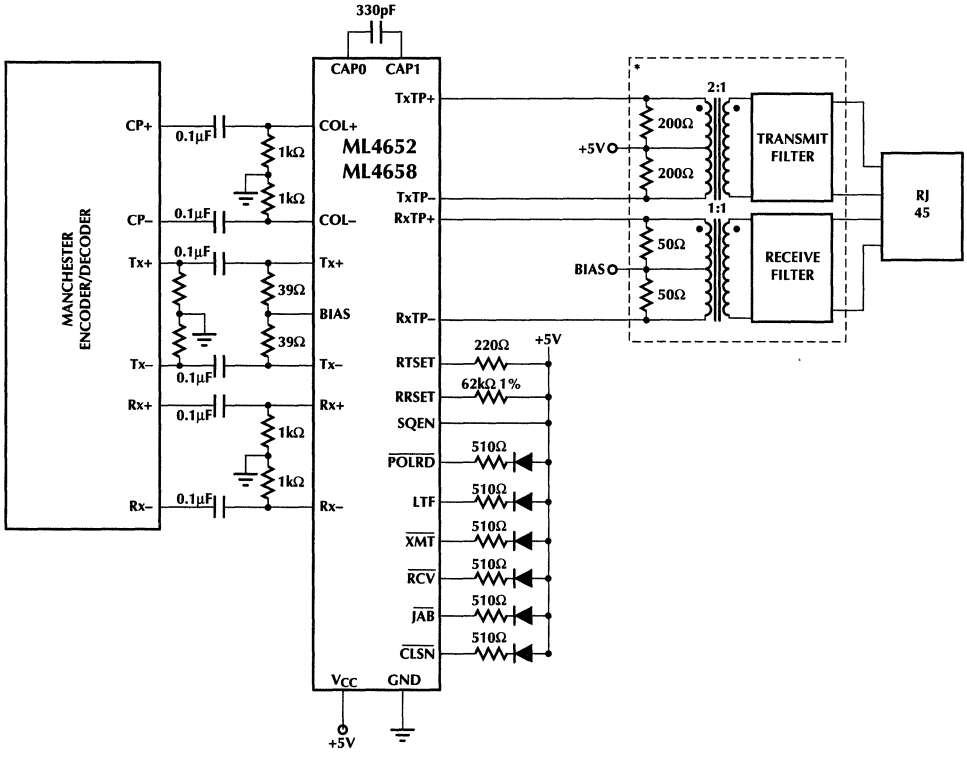


Figure 13. Internal MAU

ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	PIN COUNT	AUTO-POLARITY
ML4652CP	Skinny DIP (P24N)	24 pins	No
ML4658CP	Skinny DIP (P24N)	24 pins	Yes
ML4652CQ	PLCC (Q28)	28 pins	No
ML4658CQ	PLCC (Q28)	28 pins	Yes

Micro Linear

ML4654

10BASE-T Transceiver for Multi-Port Repeaters

GENERAL DESCRIPTION

The ML4654 10BASE-T Transceiver is a single chip cable line driver/receiver that provides all of the functionality required to implement an internal 10BASE-T Transceiver for a Multi-Port Repeater. The ML4654 provides a TTL interface well suited for Multi-Port Repeater control logic.

The ML4654 uses a minimal number of external components, and fully conforms to the IEEE 802.3 10BASE-T standard. The transmitter offers a current driven output that is less sensitive to power supply variation and noise. It offers superior performance because of its highly symetrical switching which results in low RFI noise and low jitter.

The Transceiver easily interfaces to 100Ω unshielded twisted pair cable, 150Ω shielded twisted pair cable, or a range of other characteristic impedances by changing one external resistor. Jabber and Link Test Function are fully integrated into the chip with enable/disable options. An autopolarity circuit detects the polarity of the receive pair and automatically corrects it if necessary. A polarity status pin that can drive an LED reflects the true polarity of the receive pair.

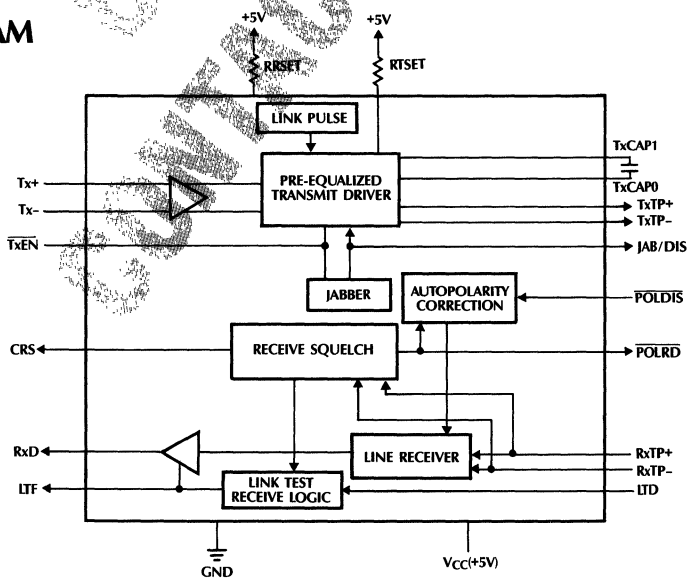
The ML4654 is available in a 20 pin skinny DIP as well as a surface mount 28 pin PLCC. The ML4654 is designed using Micro Linear's Bipolar Tile Array technology. It uses a special Tile Array designed for Data Communications applications. Semi-Standard options are available to suit a particular customer application.

FEATURES

- Complete implementation of IEEE 802.3 10BASE-T internal Medium Attachment Unit (MAU)
- TTL interface for direct connection to Multi-Port Repeater control logic
- Automatic polarity correction with a status pin to reflect the true receive polarity
- Single +5 volt supply ± 10%
- No clock or crystal required
- Capable of driving 100Ω unshielded twisted pair cable or 150Ω shielded twisted pair cable
- Fully integrated Link Test logic, with Link Test Fail Status pin and enable/disable option
- On-chip Jabber logic, with enable/disable option
- Available in a 20 pin skinny DIP or 28 pin PLCC
- Semi-standard option using Micro Linear's FB3651 LAN Transceiver Tile Array

4

BLOCK DIAGRAM



Micro Linear

ML4661

FOIRL Transceiver

GENERAL DESCRIPTION

The ML4661 FOIRL transceiver combined with the ML4621 or ML4622 fiber optic quantizers provides all of the functionality required to implement both an internal and external IEEE 802.3 FOIRL MAU. The ML4661 offers a standard IEEE 802.3 AU interface that allows it to be directly connected to industry standard manchester encoder/decoder chips or an AUI cable.

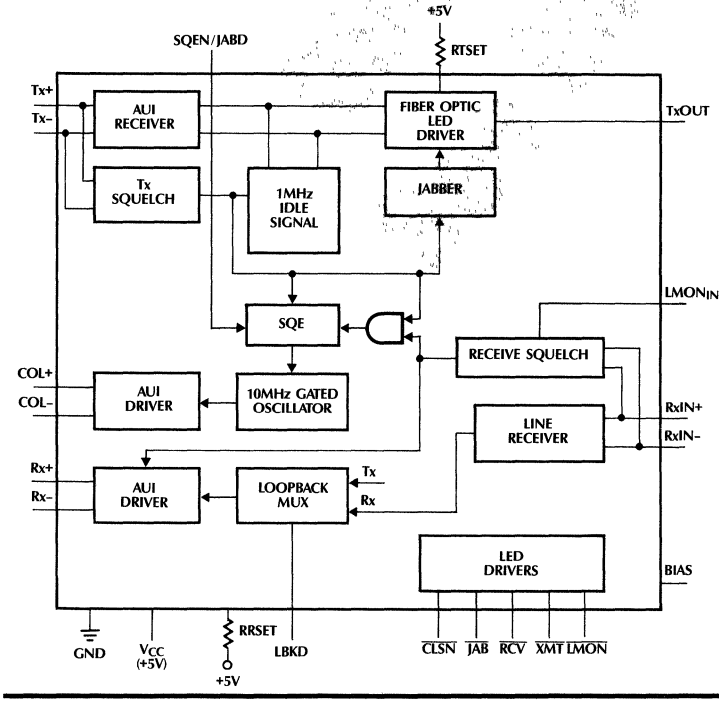
The ML4661 provides a highly integrated solution that requires a minimal number of external components, and is compliant to the IEEE 802.3 FOIRL standard. The transmitter offers a current driven output that directly drives a fiber optic LED transmitter. Jabber, 1MHz idle signal, and SQE Test are fully integrated onto the chip.

The receiver accepts an ECL level input coming from the ML4621 or ML4622 fiber optic quantizers. The 1MHz idle signal is removed and the AUI output is activated when the receive squelch criteria is exceeded. A Link Monitor function is also provided for low light detection.

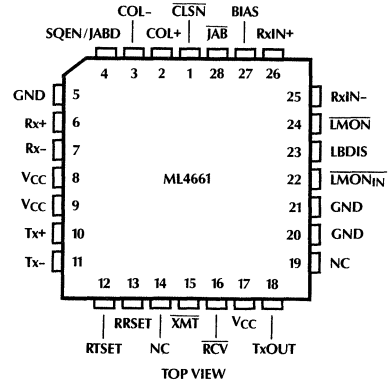
FEATURES

- Combined with the ML4621 or ML4622, offers a complete implementation of an FOIRL Medium Attachment Unit (MAU)
- Incorporates an AU interface for use in an external MAU or an internal MAU
- Single +5 volt supply ± 10%
- No crystal or clock required
- On-chip Jabber, 1MHz idle, and SQE Test with enable/disable option
- Five network status LED outputs
- Available in a 28-pin PLCC package
- Semi-standard option using Micro Linear's FB3651 LAN Transceiver Tile Array

BLOCK DIAGRAM



PIN CONNECTION



Micro Linear

ML4662

10BASE-FL Transceiver

GENERAL DESCRIPTION

The ML4662 10Base-FL transceiver combined with the ML4622 or ML4624 fiber optic quantizers provides all of the functionality required to implement both an internal and external IEEE 802.3 10Base-FL MAU. The ML4662 offers a standard IEEE 802.3 AU interface that allows it to be directly connected to industry standard manchester encoder/decoder chips or an AUI cable.

The ML4662 provides a highly integrated solution that requires a minimal number of external components, and is compliant to the IEEE 802.3 10Base-FL standard. The transmitter offers a current driven output that directly drives a fiber optic LED transmitter. Jabber, 1MHz idle signal, and SQE Test are fully integrated onto the chip.

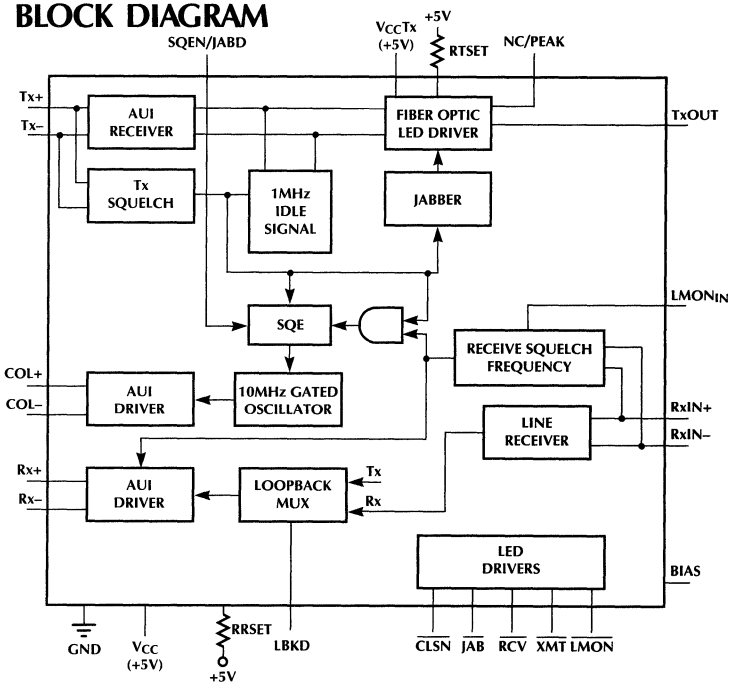
The receiver accepts an ECL level input coming from the ML4622 or ML4624 fiber optic quantizers. The 1MHz idle signal is removed and the AUI output is activated when the receive squelch criteria is exceeded. A Link Monitor function is also provided for low light detection.

FEATURES

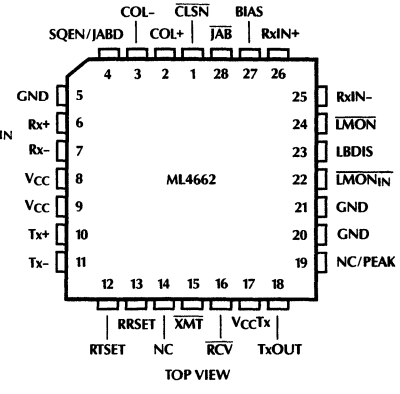
- Combined with the ML4622 or ML4624, offers a complete implementation of an 10Base-FL Medium Attachment Unit (MAU)
- Pin compatible with the ML4661 FOIRL Transceiver
- Incorporates an AU interface for use in an external MAU or an internal MAU
- Single +5 volt supply ± 10%
- No crystal or clock required
- On-chip Jabber, 1MHz idle, and SQE Test with enable/disable option
- Five network status LED outputs
- Available in a 28-pin PCC package
- Semi-standard option available

4

BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	$\overline{\text{CLSN}}$	Indicates that a collision is taking place. Active low LED driver, open collector. Event is extended with internal timer for visibility.
2	COL+	Gated 10MHz oscillation used to indicate a collision, SQE test, or jabber. Balanced differential line driver outputs that meet AUI specifications.
3	COL–	
4	SQEN/JABD	SQE Test Enable, Jabber Disable. When tied low, SQE test is disabled, when tied high SQE test is enabled. When tied to BIAS both SQE test and Jabber are disabled.
5	GND	Ground Reference.
6	Rx+	Manchester encoded receive data output to the local device. Balanced differential line driver outputs that meet AUI specifications.
7	Rx–	
8	V_{CC}	+5 Volt power input.
9	V_{CC}	
10	Tx+	Balanced differential line receiver inputs that meet AUI specifications. These inputs may be transformer, AC or DC coupled. When transformer or AC coupled, the BIAS pin is used to set the common mode voltage.
11	Tx–	
12	RTSET	Sets the current driven out of the transmitter.
13	RRSET	A 1% 61.9 KΩ resistor tied from this pin to V_{CC} sets the biasing currents for internal nodes.
14	NC	No Connection.
15	$\overline{\text{XMT}}$	Indicates that transmission is taking place. Active low LED driver, open collector. Event is extended with internal timer for visibility.
16	$\overline{\text{RCV}}$	Indicates that the transceiver is receiving a frame from the optical input. Active low LED driver, open collector. Event is extended with internal timer for visibility.
17	V_{CC}Tx	+5 volt supply for LED driver.
18	TxOUT	Fiber optic LED driver output.
19	NC/PEAK	Normally this pin can be left floating. (tying it to GND or V_{CC} is OK too.) Some fiber optic LEDs may need an additional peaking circuit to speed-up the rise and fall times. For this case, tie pin 19 (NC/PEAK) to pin 18 (TxOUT). When using the HP HFBR 1414, let pin 19 float. Using the peaking circuit may deteriorate optical overshoot and undershoot.
20	GND	Ground Reference.
21	GND	Ground Reference.
22	$\overline{\text{LMON}}_{\text{IN}}$	Link Monitor Input from the ML4622 or ML4624. This input must be low (active) for the receiver to unsquelch.
23	LBDIS	Loopback Disable. When this pin is tied to V_{CC}, the AUI transmit pair data is not looped back to the AUI receive pair, and collision is disabled. When this pin is tied to GND (normal operation), the AUI transmit pair data is looped back to the AUI receiver pair.
24	$\overline{\text{LMON}}$	Link Monitor LED status output. This pin is pulled low when $\overline{\text{LMON}}_{\text{IN}}$ input is low and there are transitions on RxIN± indicating an idle signal or active data. If either LMON_{IN} goes high or transitions cease on RxIN±, $\overline{\text{LMON}}$ will go high. Active low LED driver, open collector.
25	RxIN–	Fiber Optic receive pair. This ECL level signal is received from the ML4622 or ML4624 fiber optic quantizer. When this signal exceeds the receive squelch requirements, and the $\overline{\text{LMON}}_{\text{IN}}$ input is low, the receive data is buffered and sent to the AUI receive outputs.
26	RxIN+	
27	BIAS	BIAS output voltage for the AUI Tx+, Tx– inputs when they are AC coupled.
28	$\overline{\text{JAB}}$	Jabber network status LED. When in the Jabber state, this pin will be low and the transmitter will be disabled. In the Jabber "OK" state this pin will be high. Open collector TTL output.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Power Supply Voltage Range
  V_{CC} ..... -0.3 to 6V
Input Voltage Range
  Digital Inputs (SQEN, $LMON_{IN}$, LBDIS) ..... -0.3 to V_{CC}
  Tx+, Tx–, RxIN+, RxIN– ..... -0.3 to V_{CC}
Input Current
  RRSET, RTSET, $\overline{JAB}$, $\overline{CLSN}$, $\overline{XMT}$, $\overline{RCV}$, $\overline{LMON}$ 60mA
Output Current
  TxOUT 70mA
Storage Temperature ..... -65° C to +150°C
Lead Temperature (Soldering 10 seconds) ..... 260°C

OPERATING CONDITIONS
(Note 2)

Supply Voltage (V_{CC}) ..... 5V ± 10%
LED on Current 10mA
RRSET ..... 61.9KΩ ± 1%
RTSET ..... 162Ω ± 1%

ELECTRICAL CHARACTERISTICS
Unless otherwise specified, T_A = 0°C to 70°C, V_{CC} = 5V ± 10% (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current I_{CC}: While Transmitting	V_{CC} = 5V, RTSET = 162Ω (Note 4)			200	mA
LED Drivers: V_{OL}	I_{OL} = 10mA (Note 5)			0.8	V
Transmit Peak Output Current (Note 6)	RTSET = 162Ω, V_{CC} = V_{CC}Tx = 5V ± 5%	47	52	60	mA
Transmit Squelch Voltage Level (Tx+, Tx–)		-300	-250	-200	mV
Common Mode Input Voltage (Tx±, RxIN±)		2		V_{CC} - 0.5	V
Differential Output Voltage (Rx±, COL±)		±550		±1200	mV
Common Mode Output Voltage (Rx±, COL±)			4.0		V
Differential Output Voltage Imbalance (Rx±, COL±)				±40	mV
BIAS Voltage			3.2		V
SQE/JABD	SQE Test Disable Jabber Disable Both Enabled	 1.5 V_{CC} - 0.5		.3 V_{CC} - 2	V
LBDIS Threshold	Disabled Enabled	V_{CC} -0.10		 1	V

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Transmit					
t_{TXNPW}	Transmit Turn-On Pulse Width		20		ns
t_{TXFPW}	Transmit Turn-Off Pulse Width from Data to Idle	400		2100	ns
t_{TXLP}	Transmit Loopback Startup Delay			500	ns
t_{TXODY}	Transmitter Turn-On Delay			100	ns
t_{TXIDF}	Transmit Idle Frequency	0.85		1.25	MHz
t_{TXDC}	Transmit Idle Duty Cycle	45		55	%
t_{TXSDY}	Transmit Steady State Propagation Delay		15	50	ns
t_{TXJ}	Transmitter Jitter into 31Ω Load			±1.5	ns
Receive					
t_{RXSFT}	Receive Squelch Frequency Threshold	2.51		4.5	MHz
t_{RXODY}	Receive Turn-On Delay			250	ns
t_{RXFX}	Last Bit Received to Slow Decay Output	230	300		ns
t_{RXSDY}	Receive Steady State Propagation Delay		15	50	ns
t_{RXJ}	Receiver Jitter			±1.5	ns
t_{AR}	Differential Output Rise Time 20% to 80% (Rx±, COL±)		4		ns
t_{AF}	Differential Output Fall Time 20% to 80% (Rx±, COL±)		4		ns
Collision					
t_{CPSQE}	Collision Present to SQE Assert	0		350	ns
t_{SQEXR}	Time for SQE to Deactivate After Collision	0		700	ns
t_{CLF}	Collision Frequency	8.5		11.5	MHz
t_{CLPDC}	Collision Pulse Duty Cycle	40	50	60	%
t_{SQEDY}	SQE Test Delay (Tx Inactive to SQE)	0.6		1.6	μs
t_{SQETD}	SQE Test Duration	0.5	1.0	1.5	μs
Jabber and LED Timing					
t_{JAD}	Jabber Activation Delay	20	70	150	ms
t_{JRT}	Jabber Reset Unjab Time	250	450	750	ms
t_{JSQE}	Delay from Outputs Disabled to Collision Oscillator On		100		ns
t_{LED}	$\overline{RCV}$, $\overline{CLSN}$, $\overline{XMIT}$ On Time	8	16	32	ms
t_{LLPH}	Low Light Present to LMON High	3	5	10	μs
t_{LLCL}	Low Light Clear to LMON Low	250		750	ms

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 3: Low Duty Cycle pulse testing is performed at T_A.
Note 4: This does not include the current from the AUI pull down resistors, or LED status outputs.
Note 5: LED drivers can sink up to 20mA, but V_{OL} will be higher.
Note 6: Does not include prebias current for fiber optic LED which would typically be 3mA.

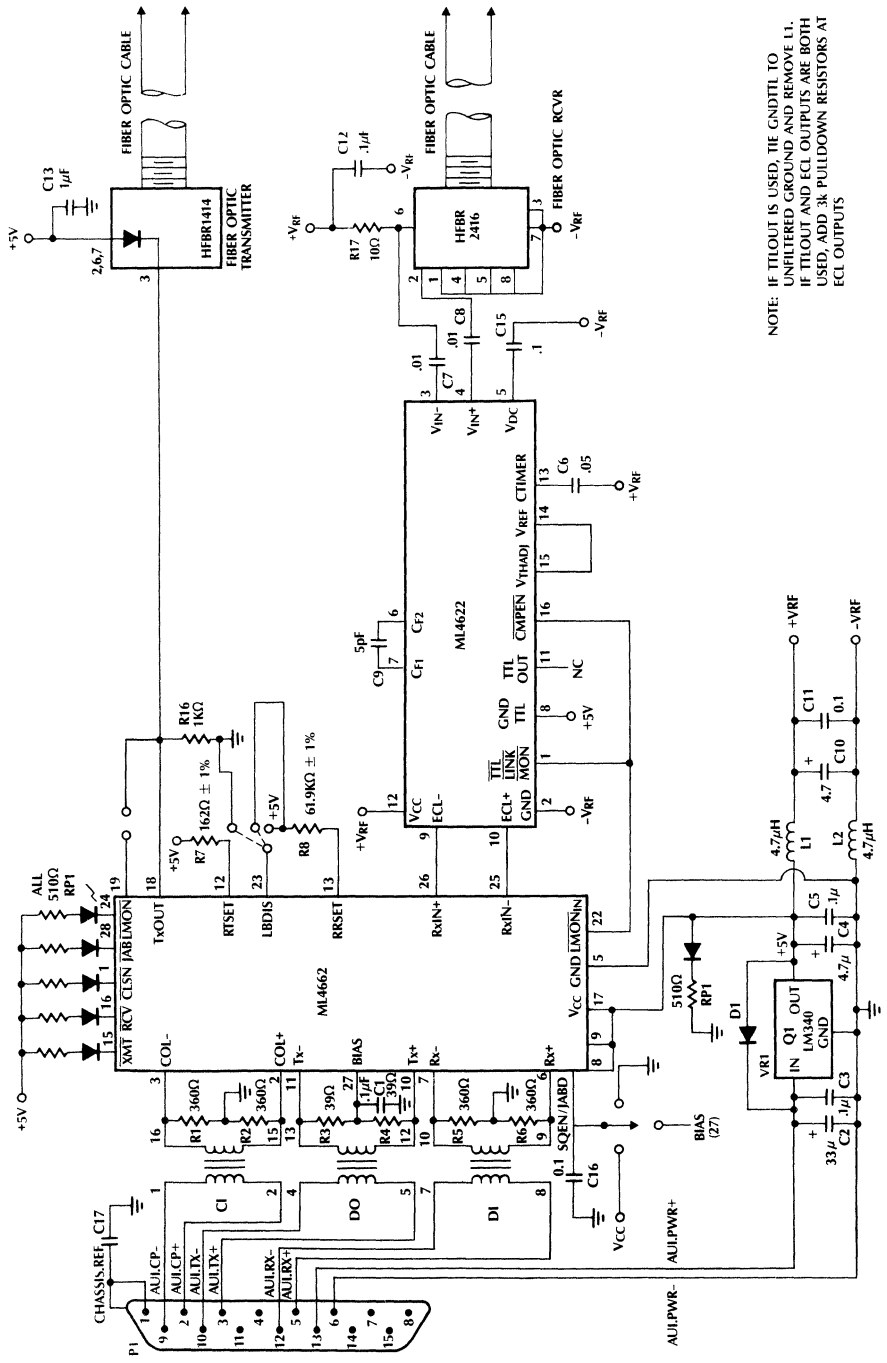


Figure 1. ML4662 Schematic Diagram

SYSTEM DESCRIPTION

Figure 1 shows a schematic diagram of the ML4662 in an internal or external 10Base-FL MAU. On one side of the transceiver is the AU interface and the other is the fiber optic interface. The AU interface is AC coupled when used in an external transceiver or can be AC or DC coupled when used in an internal transceiver. The AU interface for an external transceiver includes isolation transformers, some biasing resistors, and a voltage regulator for power.

The fiber optic side of the transceiver requires an external fiber optic transmitter, fiber optic receiver, and the ML4622 or ML4624 fiber optic quantizers. The transmitter uses a current driven output that directly drives the fiber optic transmitter. The receive side of the transceiver accepts the data after passing through the fiber optic receiver and the ML4622/ML4624 fiber optic quantizer.

AU INTERFACE

The AUI interface consist of 3 pair of signals, DO, CI and DI as shown in figure 1. The DO pair contains transmit data from the DTE which is received by the transceiver and sent out onto the fiber optic cable. The DI pair contains valid data that has been either received from the fiber optic cable or looped back from the DO and output through the DI pair to the DTE. The CI pair indicates whether a collision has occurred. It is an output that oscillates at 10MHz if a collision Jabber or SQE Test has taken place, otherwise it remains idle.
When the transceiver is external, these three pair are AC coupled through isolation transformers, while an internal transceiver may be AC or DC coupled. For the AC coupled interface, DO which is an input must be DC biased (shifted up in voltage) for the proper common mode input voltage. The BIAS pin serves this purpose. When DC coupled, transmit output pair coming from the serial interface provides this common mode voltage and the BIAS pin is not connected.

The two 39Ω 1% resistors tied to the Tx+ and Tx– pins serve two purposes. First they provide a point to connect the common mode bias voltage as discussed above, and they provide the proper matching termination for the AUI cable. The CI and DI pair, which are output from the transceiver to the AUI cable, require 360Ω pull down resistors when terminated with a 78Ω load. However on a DTE card, CI and DI do not need 78Ω terminating resistors. This also means that the pull down resistors on CI and DI can be 1KΩ or greater depending upon the particular manchester encoder/decoder chip used. Using higher value pull down resistors as in a DTE card will save power.

The AUI drivers are capable of driving the full 50 meters of cable length and have a rise and fall time of typically 4ns. In the idle state, the outputs go to the same voltage to prevent DC standing current in the isolation transformers.

TRANSMISSION

The transmit function consists of detecting the presence of data from the AUI DO input (Tx+, Tx–) and driving that data onto the fiber optic LED transmitter. A positive signal on the Tx+ lead relative to the Tx– lead of the DO circuit will result in no current, hence the fiber optic LED is in a low light condition. When Tx+ is more negative than Tx–, the ML4662 will sink current into the chip and the LED will light up.

Before data will be transmitted onto the fiber optic cable from the AUI interface, it must exceed the squelch requirements for the DO pair. The Tx squelch circuit serves the function of preventing any noise from being transmitted onto the fiber. This circuit rejects signals with pulse widths less than typically 20ns (negative going), or with levels less than –250mV. Once Tx squelch circuit has unsquelched, it looks for the start of idle signal to turn on the squelch circuit again. The transmitter turns on the squelch again when it receives an input signal at TxIN± that is more positive than –250mV for more than approximately 180ns.

At the start of a packet transmission, no more than 1 bit is received from the DO circuit and not transmitted onto the fiber optic cable. The difference between start-up delays (bit loss plus steady-state propagation delay) for any two packets that are separated by 9.6μs or less will not exceed 200ns.

FIBER OPTIC LED DRIVER

The output stage of the transmitter is a current mode switch which develops the output light by sinking current through the LED into the TxOUT pin. Once the current requirement for the LED is determined, the RTSET resistor is selected. The following equation is used to select the correct RTSET resistor:

$$RTSET = \left(\frac{52mA}{I_{OUT}}\right)162\Omega$$

The transmitter enters the idle state when it detects start of idle on Tx+ and Tx– input pins. After detecting the start of idle the transmitter switches to a 1MHz output idle signal.

The output current is switched through the TxOUT pin during the on cycle and the V_{CC}Tx pin during the off cycle as shown in figure 2. Since the sum of the current in these two pins is constant, V_{CC}Tx should be connected as close as possible to the V_{CC} connection for the LED.

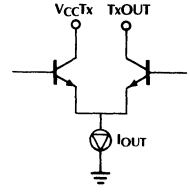


Figure 2. Fiber Optic LED Driver Structure.

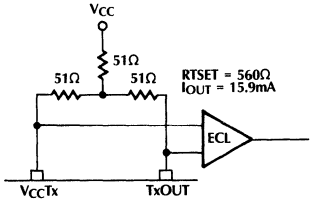


Figure 3. Converting Optical LED Driver Output to Differential ECL.

If not driving an optical LED directly, a differential output can be generated by tying resistors from V_{CC}Tx and TxOUT to V_{CC} as shown in figure 3. The minimum voltage on these two pins should not be less than V_{CC} - 2V.

RECEPTION

The input to the transceiver comes from the ECL outputs of the ML4622 or ML4624. At this point it is a clean digital ECL signal. At the start of packet reception no more than 2.5 bits are received from the fiber cable and not transmitted onto the DI circuit. The receive squelch will reject frequencies lower than 2.51MHz and any receive input if the $\overline{LMON}_{IN}$ pin is high.

While in the unsquelch state, the receive squelch circuit looks for the start of idle signal at the end of the packet. Start of idle occurs when the input signal remains idle for more than 160ns. When start of idle is detected, the receive squelch circuit returns to the squelch state and the start of idle signal is output on the DI circuit (Rx+, Rx–).

COLLISION

Whenever the receiver and the transmitter are active at the same time the chip will activate the collision output, except when loopback is disabled (LBDIS = V_{CC}). The collision output is a differential square wave matching the AUI specifications and capable of driving a 78Ω load. The frequency of the square wave is 10MHz ± 15% with a 60/40 to 40/60 duty cycle. The collision oscillator also is activated during SQE Test and Jabber.

LOOPBACK

The loopback function emulates a 10Base-T transceiver whereby the transmit data sent by the DTE is looped back over the AUI receive pair. Some LAN controllers use this loopback information to determine whether a MAU is connected by monitoring the carrier sense while transmitting. The software can use this loopback information to determine whether a MAU is connected to the DTE by checking the status of carrier sense after each packet transmission.

When data is received by the chip while transmitting, a collision condition exits. This will cause the collision oscillator to turn on and the data on the DI pair will follow RxIN±. After a collision is detected, the collision oscillator will remain on until either DO or RxIN go idle.

Loopback can be disabled by strapping LBDIS to V_{CC}. In this mode the chip operates as a full duplex transmitter and receiver, and collision detection is disabled. A loopback through the transceiver can be accomplished by tying the fiber transmitter to the receiver.

SQE TEST FUNCTION (SIGNAL QUALITY ERROR)

The SQE test function allows the DTE to determine whether the collision detect circuitry is functional. After each transmission, during the inter packet gap time, the collision oscillator will be activated for typically 1μs. The SQE test will not be activated if the chip is in the low light state, or the jabber on state.

For SQE to operate, the SQEN pin must be tied to V_{CC}. This allows the MAU to be interfaced to a DTE. The SQE test can be disabled by tying the SQEN pin to ground, for a repeater interface.

JABBER FUNCTION REQUIREMENTS

The Jabber function prevents a babbling transmitter from bringing down the network. Within the transceiver is a Jabber timer that starts at the beginning of each transmission and resets at the end of each transmission. If the transmission last longer than 20ms the jabber logic disables the transmitter, and turns on the collision signal COL+, COL–. When Tx+ and Tx– finally go idle, a second timer measures 0.5 seconds of idle time before the transmitter is enabled and collision is turned off. Even though the transmitter is disabled during jabber, the 1MHz idle signal is still transmitted.

LED DRIVERS

The ML4662 has five LED drivers. The LED driver pins are active low, and the LEDs are normally off. The LEDs are tied to their respective pins through a 500Ω resistor to 5 Volts.

The $\overline{XMT}$, $\overline{RCV}$ and $\overline{CLSN}$ pins have pulse stretchers on them which enables the LEDs to be visible. When transmission or reception occurs, the LED $\overline{XMT}$, $\overline{RCV}$ or $\overline{CLSN}$ status pins will activate low for several milliseconds. If another transmit, receive or collision conditions occurs before the timer expires, the LED timer will reset and restart the timing. Therefore rapid events will leave the LEDs continuously on. The $\overline{JAB}$ and $\overline{LMON}$ LEDs do not have pulse stretchers on them since their conditions occur long enough for the eye to see.

LOW LIGHT CONDITION

The $\overline{\text{LMON}}$ LED output is used to indicate a low light condition. LMON is activated low when both LMON_{IN} is low and there are transitions on RxIN± less than 3μs apart. If either one of these conditions do not exist, LMON will go high.

DIFFERENCES BETWEEN 10BASE-FL AND FOIRL

10Base-FL is an improved version of the original FOIRL standard. The 10Base-FL standard allows backward compatibility of a 10Base-FL transceiver with a FOIRL transceiver. The main improvements incorporated into 10Base-FL are that it can attach to a DTE by adding the SQE test, and the distance has been increased from 1Km to 2Km. The other differences are much more subtle.

1. SQE Test: The FOIRL standard did not include the option of attaching a fiber transceiver to a DTE. Adding the SQE test to 10Base-FL enables a 10Base-FL transceiver to attach to a DTE. Micro Linear's ML4661 FOIRL transceiver has a SQE test, but this is beyond the scope of the FOIRL standard.

2. 0 to at Least 2Km Distance: The FOIRL standard specifies a 1Km distance while 10Base-FL specifies 2Km. The additional 1Km distance for 10Base-FL comes from an increased flux budget for the cable of 3.5dB. This 3.5dB increase came from an increase of 2.5dB sensitivity for the receiver and a 1dB improvement for the transmitter. The following table illustrates the transmit and receive power requirements for the two standards. Note: FOIRL specifies optical power in peak and 10Base-FL specifies it in average. Subtracting 3dB from peak will give the average. In the table below the FOIRL specifications were converted from peak to average power.

Transmit/Receive Average Power	MIN	MAX	Conditions
FOIRL			
Transmitter	-12dBm	-21dBm	
Receiver	-12dBm	-30dBm	BER < 10^{-10}
10Base-FL			
Transmitter	-12dBm	-20dBm	
Receiver	-12dBm	-32.5dBm	BER < 10^{-9}

3. MAU State Diagrams are Different: The state diagrams for 10Base-FL are similar to 10Base-T, while the state diagrams for FOIRL are slightly different. The differences are in the AUI loopback, and in the link integrity function.

AUI Loopback — In 10Base-FL, the DO to DI loopback is always disabled during a collision, and optical receive data is passed through to DI. For FOIRL there are some cases where loopback continues (i.e. DO looped to DI) during a collision, and others where loopback is disabled during a collision. 10Base-FL is identical to 10Base-T in this case. Please refer to the IEEE standards for greater detail.

Link Integrity — 10Base-FL adds an additional state to the Link Integrity Test function that will not allow an exit from the Low Light State until both the transmitter and receiver are idle. In FOIRL it is possible to exit from the Low Light State while still receiving data.

MAU Timing Differences — The timing differences between 10Base-FL and FOIRL relate to propagation delays, start-up delays, and collision deassert delays. The following table provides the details of these parameters.

Timing Parameter Differences	FOIRL (bit times)	10Base-FL (bit times)
ORD_input to input on DI		
Steady State Prop Delay	0.5	2
Start-up Delay	3.5	5
output on DO to OTD_output		
Steady State Prop Delay	0.5	2
Start-up Delay	3.5	5
Collision Deassert to SQE Deassert minimum	4.5	0

OTD — Optical Transmit Data
ORD — Optical Receive Data
DI, DO, CI — AUI Interface Signals

TIMING DIAGRAMS

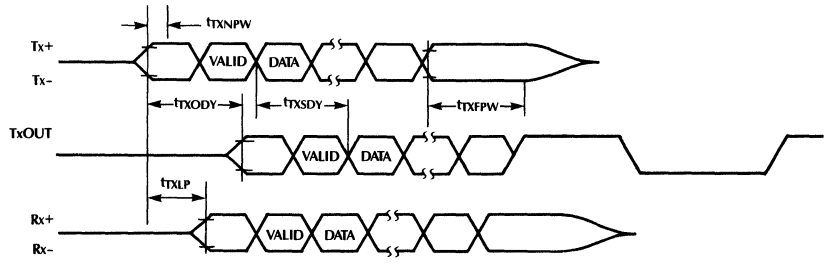


Figure 4. Transmit and Loopback Timing

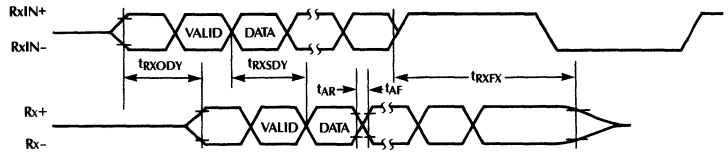


Figure 5. Receive Timing

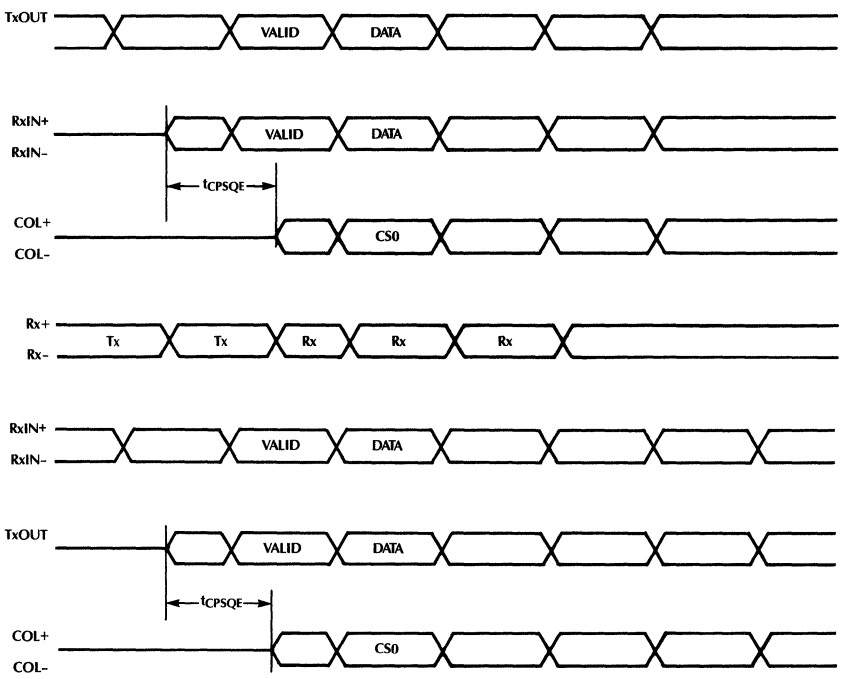


Figure 6. Collision Timing

TIMING DIAGRAMS (Continued)

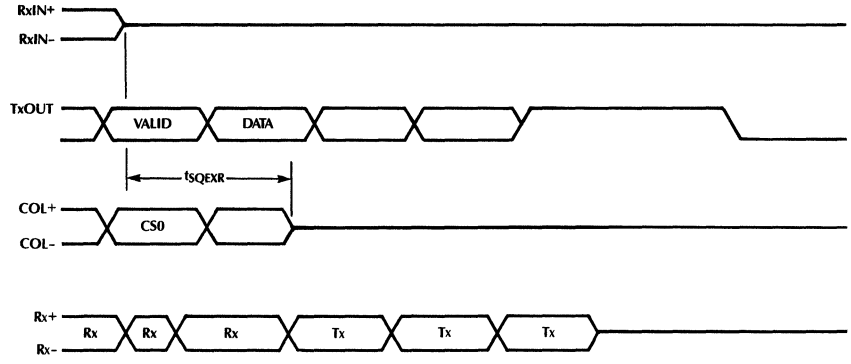


Figure 7. Collision Timing

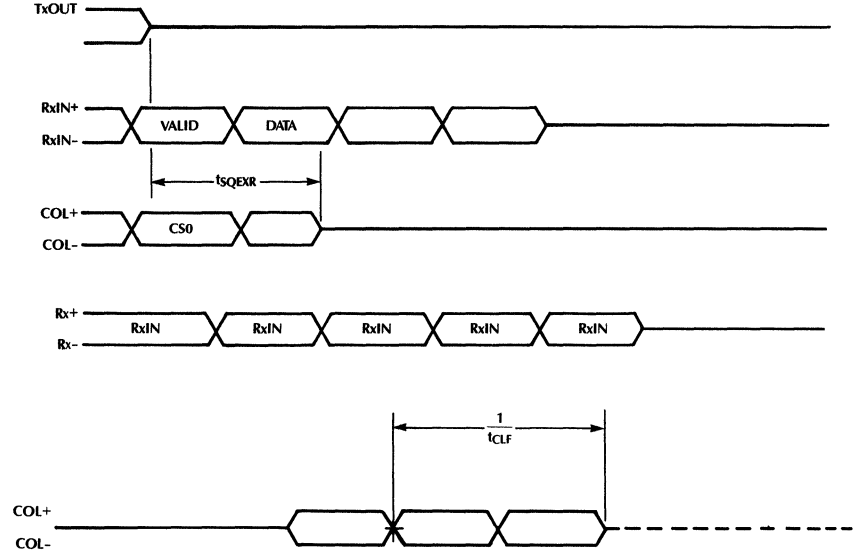


Figure 8. Collision Timing

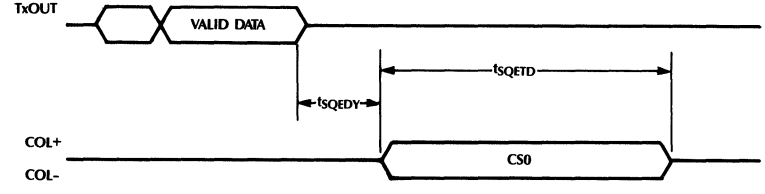


Figure 9. SQE Timing

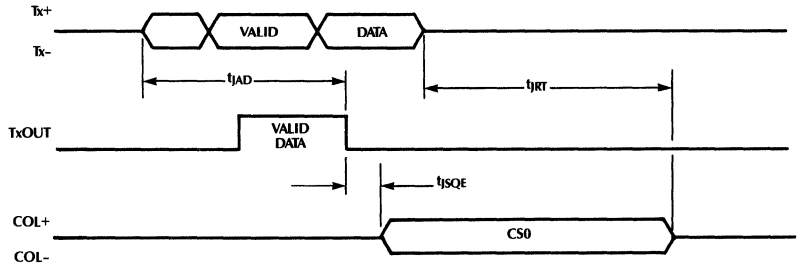


Figure 10. Jabber Timing

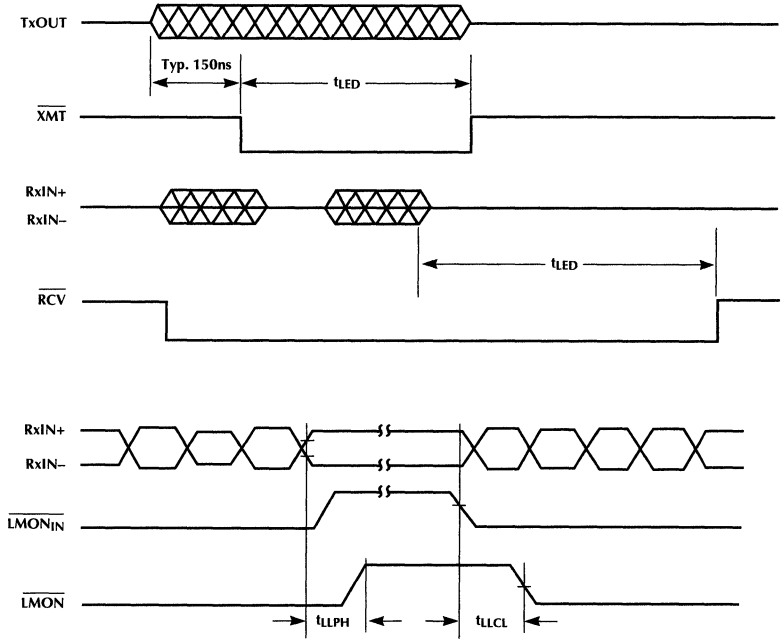


Figure 11. LED Timing

ORDERING INFORMATION

PART NUMBER	PIN COUNT	PACKAGE
ML4662CQ	28 Pins	Molded PCC (Q28)

ML4662EVAL

10BASE-FL Evaluation Kit

GENERAL DESCRIPTION

The ML4662EVAL is an external MAU designed to evaluate the ML4662 FOIRL/10BASE-FL transceiver and the ML4622 fiber optic quantizer. The board interfaces to the AUI port through the transformer and to the fiber optic cable through the HP fiber optic transmitter and receiver.

FEATURES

- Jumper switches to enable or disable Loop Back.
- Jumper switches to enable or disable SQE and Jabber functions.
- Capable of adjusting the receive sensitivity.
- 6 status LEDs.
- Current consumption: 260-290mA Typically

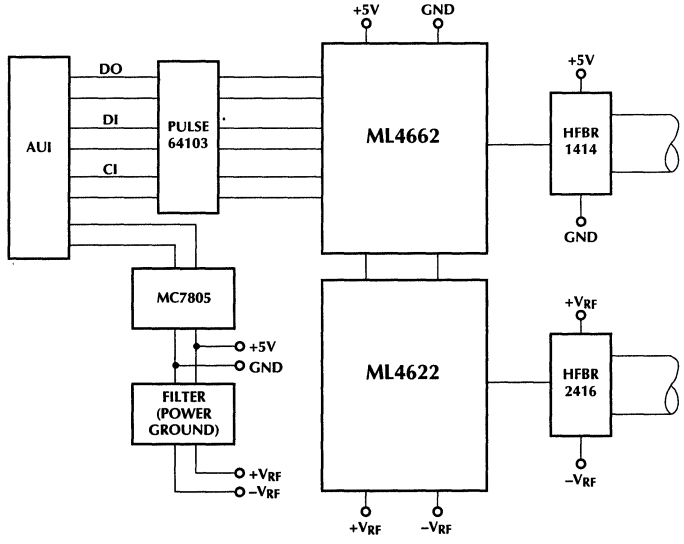
KIT COMPONENTS

The ML4662EVAL kit includes the following items to help the customer speed their design, layout and debug process.

1) BLANK PCB: 4 layer board with separate power and ground plane (inner layers).
2) COMPONENT KIT: Includes the key components as listed below. The rest of the components should be provided by the customer based on the parts list of the ML4662EVAL.
   - HFBR1414: HP fiber Optic LED transmitter.
   - HFBR2416: HP fiber optic pin diode receiver.
   - One 28 pind sockets for the ML4662.
   - ML4662CQ: 10BASE-FL transceiver.
   - ML4622CP: Fiber Optic quantizer.
   - PE64103: PULSE AUI coupling transformer.
   - AUI CONNECTOR: 15 pins D SUB connector.
3) DOCUMENTATION: Includes the following items:
   - Demo board description.
   - Block Diagram of the DEMO board.
   - Schematic of the demo board.
   - Lay out of the demo board.
   - Parts list of the ML4662EVAL.

4

BLOCK DIAGRAM



Micro Linear

ML4663

Single Chip 10BASE-FL Transceiver

GENERAL DESCRIPTION

The ML4663 Single Chip 10BASE-FL Transceiver integrates both a ML4662 10BASE-FL Transceiver with a ML4622 Fiber Optic Data Quantizer to implement a highly integrated solution for 10BASE-FL transceivers. ML4663 offers a standard IEEE 802.3 AU interface that allows it to be directly connected to industry standard manchester encoder/decoder chips or an AUI connector.

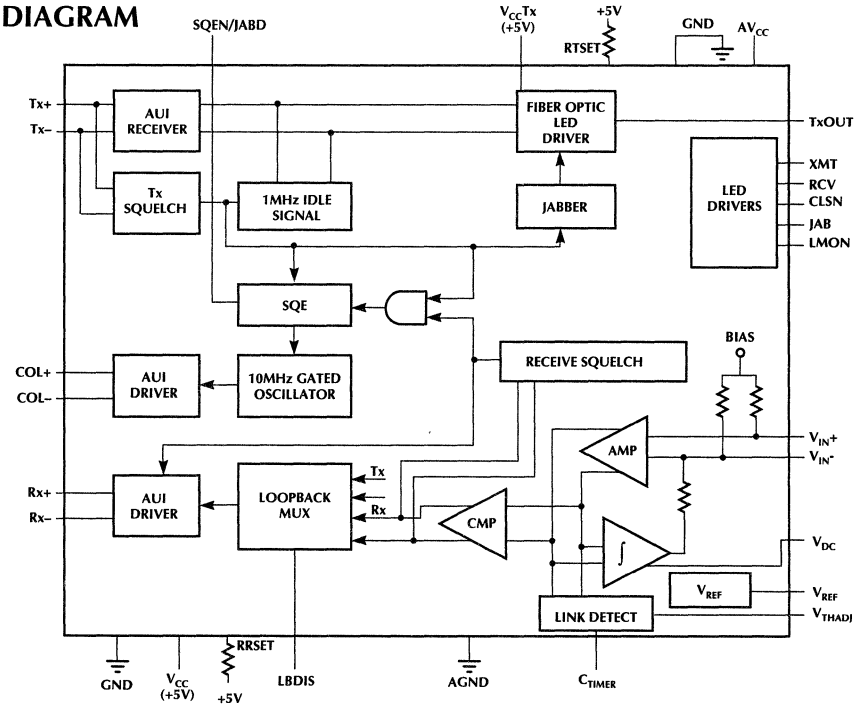
The ML4663 provides a highly integrated solution that requires a minimal number of external components, and is compliant to the IEEE 802.3 10BASE-FL standard. The transmitter offers a current drive output that directly drives a fiber optic LED transmitter. The receiver offers a highly stable fiber optic data quantizer capable of accepting input signals as low as $2mV_{P-P}$ with a 55dB dynamic range.

The transmitter automatically inserts 1MHz signal during idle time and removes this signal on reception. Low Light is continuously monitored for both activity as well as power level. Five LED status indicators monitor error conditions as well as transmissions, receptions and collisions.

FEATURES

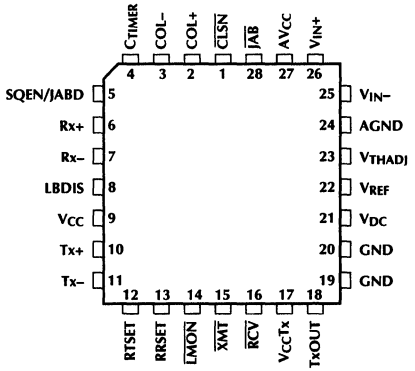
- Single chip solution for 10BASE-FL internal or external Medium Attachment Units (MAUs)
- Incorporates an AU interface
- Highly stable data quantizer with 55dB input dynamic range
- Input sensitivity as low as $2mV_{P-P}$
- Current driven fiber optic LED driver for accurate launch power
- Single +5 volt supply
- No crystal or clock required
- Five network status LED outputs
- Available in 28 pin PCC package
- Semi-Standard option available

BLOCK DIAGRAM



PIN CONNECTION

28-Pin PCC Q-28



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	$\overline{\text{CLSN}}$	Indicates that a collision is taking place. Active low LED driver, open collector. Event is extended with internal timer for visibility.
2 3	COL+ COL–	Gated 10MHz oscillation used to indicate a collision, SQE test, or jabber. Balanced differential line driver outputs that meet AUI specifications.
4	C_{TIMER}	A capacitor from this pin to V_{CC} determines the Link Monitor response time.
5	SQEN/JABD	SQE Test Enable, Jabber Disable. When tied low, SQE test is disabled, when tied high SQE test is enabled. When tied to 2.0V both SQE test and Jabber are disabled.
6 7	Rx+ Rx–	Manchester encoded receive data output to the local device. Balanced differential line driver outputs that meet AUI specifications.
8	LBDIS	Loopback Disable. When this pin is tied to V_{CC}, the AUI transmit pair data is not looped back to the AUI receive pair, and collision is disabled. When this pin is tied to GND (normal operation) or left floating, the AUI transmit pair data is looped back to the AUI receiver pair, except during collision.
9	V_{CC}	+5 volt power input.
10 11	Tx+ Tx–	Balanced differential line receiver inputs that meet AUI specifications. These inputs may be transformer or capacitively coupled. The Tx input pins are internally DC biased for AC coupling.
12	RTSET	Sets the current driven output of the transmitter.
13	RRSET	A 1% 61.9kΩ resistor tied from this pin to V_{CC} sets the biasing currents for internal nodes.
14	$\overline{\text{LMON}}$	Link Monitor "Low Light" LED status output. This pin is pulled low when the voltage on the V_{IN}+, V_{IN}– inputs exceed the minimum threshold set by the V_{THADJ} pin, and there are transitions on V_{IN}+, V_{IN}– indicating an idle signal or active data. If either the voltage on the V_{IN}+, V_{IN}– inputs fall below the minimum threshold or transitions cease on V_{IN}+, V_{IN}–, $\overline{\text{LMON}}$ will go high. Active low LED driver, open collector.
15	$\overline{\text{XMT}}$	Indicates that transmission is taking place. Active low LED driver, open collector. Event is extended with internal timer for visibility.
16	$\overline{\text{RCV}}$	Indicates that the transceiver is receiving a frame from the optical input. Active low LED driver, open collector. Event is extended with internal timer for visibility.
17	V_{CC}Tx	+5 volt supply for fiber optic LED driver.
18	TxOUT	Fiber optic LED driver output.
19	GND	Ground Reference.
20	GND	Ground Reference.
21	V_{DC}	An external capacitor on this pin integrates an error signal which nulls the offset of the input amplifier. If the DC feedback loop is not being used, this pin should be connected to V_{REF}.
22	V_{REF}	A 2.5V reference with respect to GND.
23	V_{THADJ}	This input pin sets the link monitor threshold.
24	AGND	Analog Filtered Ground.
25	V_{IN}–	This input pin should be capacitively coupled to the input source or to filtered AV_{CC}. (The input resistance is approximately 1.3kΩ.)
26	V_{IN}+	This input pin should be capacitively coupled to the input source or to filtered AV_{CC}. (The input resistance is approximately 1.3kΩ.)
27	AV_{CC}	Analog Filtered +5 volts.
28	$\overline{\text{JAB}}$	Jabber network status LED. When in the Jabber state, this pin will be low and the transmitter will be disabled. In the Jabber "OK" state this pin will be high. Active low LED, open collector.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- V_{CC} ..... –0.3 to 6V

Input Voltage Range
- Digital Inputs (SQEN, LBDIS) ..... –0.3 to V_{CC}
- Tx+, Tx–, V_{IN}+, V_{IN}– ..... –0.3 to V_{CC}

Input Current
- RRSET, RTSET, $\overline{JAB}$, $\overline{CLSN}$, $\overline{XMT}$, $\overline{RCV}$, $\overline{LMON}$ 60mA

Output Current
- TxOUT 70mA

Storage Temperature Range ..... –65°C to +150°C

Lead Temperature (soldering 10 sec) ..... 260°C

OPERATING CONDITIONS

Supply Voltage (V_{CC}) ..... 5V ± 5%

LED on Current 10mA

RRSET ..... 61.9kΩ ± 1%

RTSET ..... 115Ω ± 1%

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 0°C to 70°C, V_{CC} = V_{CC}Tx = 5V ± 5% (Note 2 and 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current I_{CC}: While Transmitting	V_{CC} = 5V, RTSET = 115Ω (Note 4)			220	mA
LED Drivers: V_{CC}	I_{OL} = 10mA (Note 5)			0.8	V
Transmit Peak Output Current (Note 6)	RTSET = 115Ω	47	52	57	mA
Transmit Squelch Voltage Level (Tx+, Tx–)		–300	–250	–200	mV
Differential Output Voltage (Rx±, COL±)		±550		±1200	mV
Common Mode Output Voltage (Rx±, COL±)			4.0		V
Differential Output Voltage Imbalance (Rx±, COL±)				±40	mV
SQE/JABD	SQE Test Disable Both Disabled Both Enabled	 1.5 V_{CC} – 0.5		0.3 V_{CC} – 2	V V V
LBDIS Threshold	Disabled Enabled	V_{CC} – 0.1		 1	V V
Common Mode Voltage (Tx+, Tx–)			3.5		V
Common Mode Voltage (V_{IN}+, V_{IN}–)			1.65		V
Reference Voltage		2.30	2.45	2.60	V
V_{REF} Output Source Current				5	mA
Amplifier Gain			100		V/V
Input Signal Range		2		1600	mV_{P-P}
External Voltage at V_{THADJ} to Set V_{TH}		0.5		2.7	V
Input Offset	V_{DC} = V_{REF} (DC loop active)		3		mV
Input Referred Noise	50MHz BW		25		µV
Input Resistance	V_{IN}+, V_{IN}–	0.8	1.3	2.0	kΩ
Input Bias Current of V_{THADJ}		–200	10	+200	µA
Input Threshold Voltage	V_{THADJ} = V_{REF} (Note 7)	5	6	7	mV_{P-P}
Hysteresis			20		%

4

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Transmit					
t_{TXNPW}	Transmit Turn-On Pulse Width		20		ns
t_{TXFPW}	Transmit Turn-Off Pulse Width from Data to Idle	400		2100	ns
t_{TXLP}	Transmit loopback Start-up Delay			500	ns
t_{TXODY}	Transmit Turn-On Delay			100	ns
t_{TXIDF}	Transmit Idle Frequency	0.85		1.25	MHz
t_{TXDC}	Transmit Idle duty Cycle	45		55	%
t_{TXSDY}	Transmit Steady State Propagation Delay		15	50	ns
t_{TXJ}	Transmit Jitter into 31Ω Load			±1.5	ns
Receive					
t_{RXSFT}	Receive Squelch Frequency Threshold	2.51		4.5	MHz
t_{RXODY}	Receive Turn-On Delay			270	ns
t_{RXFX}	Last Bit Received to Slow Decay Output	230	300		ns
t_{RXSDY}	Receive Steady State Propagation Delay		15	50	ns
t_{RXJ}	Receive Jitter			±1.5	ns
t_{AR}	Differential Output Rise Time 20% to 80% (Rx±, COL±)		4		ns
t_{AF}	Differential Output Fall Time 20% to 80% (Rx±, COL±)		4		ns
Collision					
t_{CPSQE}	Collision Present to SQE Assert	0		350	ns
t_{SQEXR}	Time for SQE to Deactivate After Collision	0		700	ns
t_{CLF}	Collision Frequency	8.5		11.5	MHz
t_{CLPDC}	Collision Pulse Duty Cycle	40	50	60	%
t_{SQEDY}	SQE Test Delay (Tx Inactive to SQE)	0.6		1.6	µs
t_{SQETD}	SQE Test Duration	0.5	1.0	1.5	µs
Jabber and LED Timing					
t_{JAD}	Jabber Activation Delay	20	70	150	ms
t_{JRT}	Jabber Reset Unjab Time	250	450	750	ms
t_{JSQE}	Delay from Outputs Disabled to Collision Oscillator On		100		ns
t_{LED}	$\overline{RCV}$, $\overline{CLSN}$, $\overline{XMT}$ On Time	8	16	32	ms
t_{LLPH}	Low Light Present to $\overline{LMON}$ High	3	5	10	µs
t_{LLCL}	Low Light Present to $\overline{LMON}$ Low	250		750	ms

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 3: Low Duty Cycle pulse testing is performed at T_A.
Note 4: This dose not include the current from the AUI pull-down resistors, or LED status outputs.
Note 5: LED drivers can sink up to 20mA, but V_{OL} will be higher.
Note 6: Does not include pre-bias current for fiber optic LED which would typically be 3mA.
Note 7: Threshold for switching from Link Fail to Link Pass (Low Light).

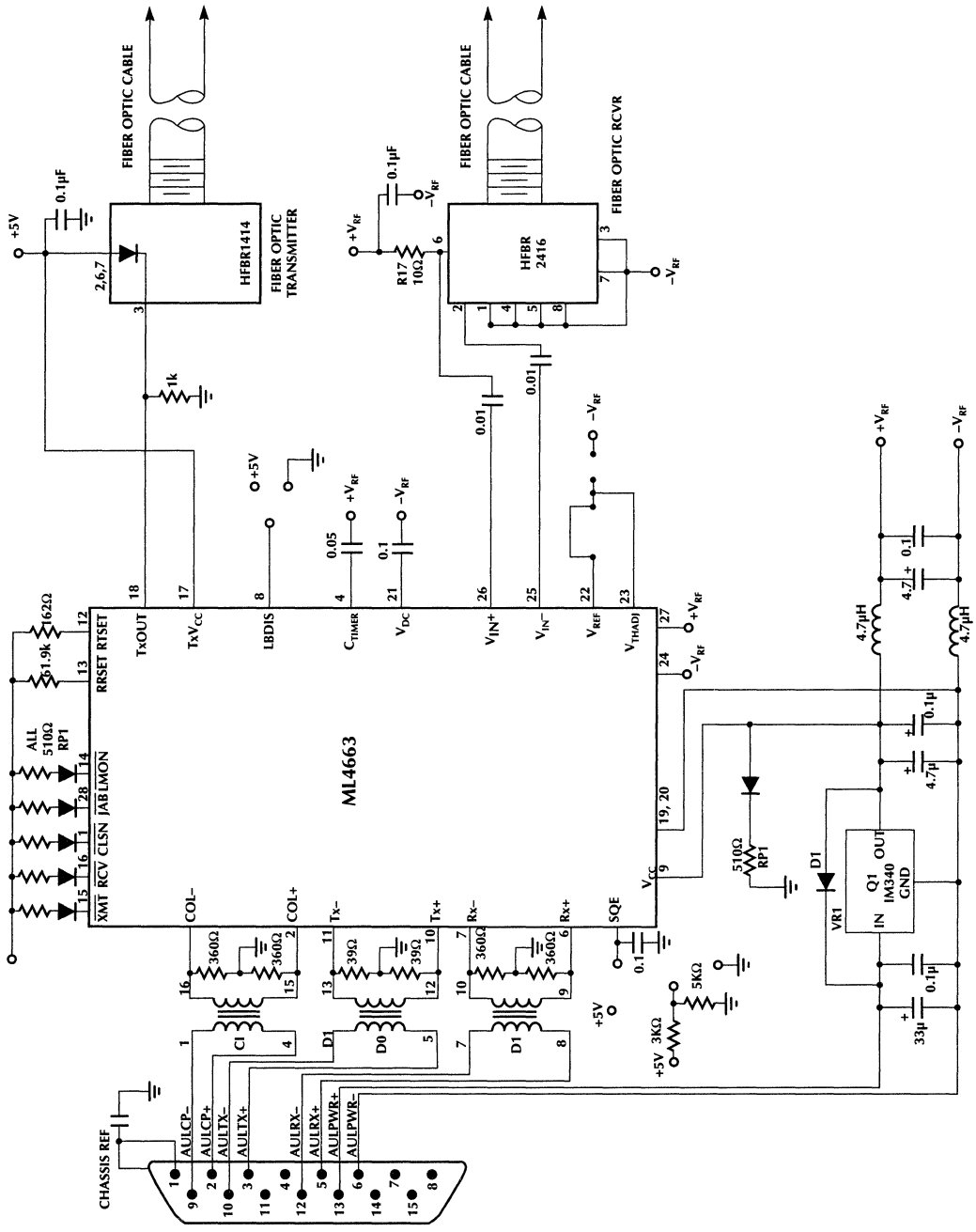


Figure 1. ML4663 Schematic Diagram

SYSTEM DESCRIPTION

Figure 1 shows a schematic diagram of the ML4663 in an internal or external 10BASE-FL MAU. On one side of the transceiver is the AU interface and the other is the fiber optic interface. The AU interface is AC coupled when used in an external transceiver or an internal transceiver. The AU interface for an external transceiver includes isolation transformers, some biasing resistors, and a voltage regulator for power.

The fiber optic side of the transceiver requires an external fiber optic transmitter and fiber optic receiver. The transmitter uses a current driven output that directly drives the fiber optic transmitter. The receive side of the transceiver accepts the data after passing through a fiber optic receiver, which consists of a module containing a pin diode and a transimpedance amplifier.

AU INTERFACE

The AU interface consist of 3 pair of signals, DO, CI and DI as shown in figure 1. The DO pair contains transmit data from the DTE which is received by the transceiver and sent out onto the fiber optic cable. The DI pair contains valid data that has been either received from the fiber optic cable or looped back from the DO and output through the DI pair to the DTE. The CI pair indicates whether a collision has occurred. It is an output that oscillates at 10MHz if a collision, Jabber or SQE Test has taken place, otherwise it remains idle.

When the transceiver is external, these three pairs are AC coupled through isolation transformers, while an internal transceiver may be capacitively coupled. Tx+, Tx– is internally DC biased (shifted up in voltage) for the proper common mode input voltage.

The two 39Ω 1% resistors (or one 78Ω 1% resistor) tied to the Tx+ and Tx– pins will provide the proper termination. The CI and DI pair, which are output from the transceiver to the AUI cable, require 360Ω pull down resistors when terminated with a 78Ω load. However on a DTE card, CI and DI do not need 78Ω terminating resistors. This also means that the pull down resistors on CI and DI can be 1kΩ or greater depending upon the particular Manchester encoder/decoder chip used. Using higher value pull down resistors as in a DTE card will save power. Refer to Application Note 13 for a more detailed explanation of the AUI pull-down resistors.

The AUI drivers are capable of driving the full 50 meters of cable length and have a rise and fall time of typically 4ns. In the idle state, the outputs go to the same voltage to prevent DC standing current in the isolation transformers.

TRANSMISSION

The transmit function consists of detecting the presence of data from the AUI DO input (Tx+, Tx–) and driving that data onto the fiber optic LED transmitter. A positive signal on the Tx+ lead relative to the Tx– lead of the DO circuit will result in no current, hence the fiber optic LED is in a low light condition. When Tx+ is more negative than Tx–, the ML4663 will sink current into the chip and the fiber optic LED will light up.

Before data will be transmitted onto the fiber optic cable from the AUI interface, it must exceed the squelch requirements for the DO pair. The Tx squelch circuit serves the function of preventing any noise from being transmitted onto the fiber. This circuit rejects signals with pulse widths less than typically 20ns (negative going), or with levels less than –250mV. Once Tx squelch circuit has unsquelched, it looks for the start of idle signal to turn on the squelch circuit again. The transmitter turns on the squelch again when it receives an input signal at Tx+, Tx– that is more positive than –250mV for more than approximately 180ns.

At the start of a packet transmission, no more than 2 bits are received from the DO circuit and not transmitted onto the fiber optic cable. The difference between start-up delays (bit loss plus steady-state propagation delay) for any two packets that are separated by 9.6µs or less will not exceed 200ns.

FIBER OPTIC LED DRIVER

The output stage of the transmitter is a current mode switch which develops the output light by sinking current through the LED into the TxOUT pin. Once the current requirement for the LED is determined, the RTSET resistor is selected. The following equation is used to select the correct RTSET resistor:

$$RTSET = \left(\frac{52mA}{I_{OUT}}\right) 115\Omega$$

The transmitter enters the idle state when it detects start of idle on Tx+ and Tx– input pins. After detecting the start of idle the transmitter switches to a 1MHz output idle signal.

The output current is switched through the TxOUT pin during the on cycle and the V_{CC}Tx pin during the off cycle as shown in figure 2. Since the sum of the current in these two pins is constant, V_{CC}Tx should be connected as close as possible to the V_{CC} connection for the LED.

If not driving an optical LED directly, a differential output can be generated by tying resistors from V_{CC}Tx and TxOUT to V_{CC} as shown in figure 3. The minimum voltage on these two pins should not be less than V_{CC} – 2V.

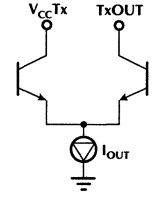


Figure 2. Fiber Optic LED Driver Structure.

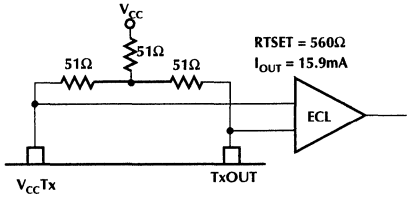


Figure 3. Converting Optical LED Driver Output to Differential ECL.

RECEPTION

The input to the transceiver comes from a fiber optic receiver as shown in figure 1. At the start of packet reception no more than 2.7 bits are received from the fiber cable and not transmitted onto the DI circuit. The receive squelch will reject frequencies lower than 2.51MHz.

While in the unsquelch state, the receive squelch circuit looks for the start of idle signal at the end of the packet. Start of idle occurs when the input signal remains idle for more than 160ns. When start of idle is detected, the receive squelch circuit returns to the squelch state and the start of idle signal is output on the DI circuit (Rx+, Rx–).

COLLISION

Whenever the receiver and the transmitter are active at the same time the chip will activate the collision output, except when loopback is disabled (LBDIS = V_{CC}). The collision output is a differential square wave matching the AUI specifications and capable of driving a 78Ω load. The frequency of the square wave is 10MHz ± 15% with a 60/40 to 40/60 duty cycle. The collision oscillator also is activated during SQE Test and Jabber.

LOOPBACK

The loopback function emulates a 10BASE-T transceiver whereby the transmit data sent by the DTE is looped back over the AUI receive pair. Some LAN controllers use this loopback information to determine whether a MAU is connected by monitoring the carrier sense while transmitting. The software can use this loopback information to determine whether a MAU is connected to the DTE by checking the status of carrier sense after each packet transmission.

When data is received by the chip while transmitting, a collision condition exits. This will cause the collision oscillator to turn on and the data on the DI pair will follow V_{IN}+, V_{IN}–. After a collision is detected, the collision oscillator will remain on until either DO or V_{IN}+, V_{IN}– go idle.

Loopback can be disabled by strapping LBDIS to V_{CC}. In this mode the chip operates as a full duplex transmitter and receiver, and collision detection is disabled. A loopback through the transceiver can be accomplished by tying the fiber transmitter to the receiver.

SQE TEST FUNCTION (SIGNAL QUALITY ERROR)

The SQE test function allows the DTE to determine whether the collision detect circuitry is functional. After each transmission, during the inter packet gap time, the collision oscillator will be activated for typically 1µs. The SQE test will not be activated if the chip is in the low light state, or the jabber on state.

For SQE to operate, the SQEN pin must be tied to V_{CC}. This allows the MAU to be interfaced to a DTE. The SQE test can be disabled by tying the SQEN pin to ground, for a repeater interface.

JABBER FUNCTION REQUIREMENTS

The Jabber function prevents a babbling transmitter from bringing down the network. Within the transceiver is a Jabber timer that starts at the beginning of each transmission and resets at the end of each transmission. If the transmission last longer than 20ms the jabber logic disables the transmitter, and turns on the collision signal COL+, COL–. When Tx+ and Tx– finally go idle, a second timer measures 0.5 seconds of idle time before the transmitter is enabled and collision is turned off. Even though the transmitter is disabled during jabber, the 1MHz idle signal is still transmitted.

LED DRIVERS

The ML4663 has five LED drivers. The LED driver pins are active low, and the LEDs are normally off (except for $\overline{\text{LMON}}$). The LEDs are tied to their respective pins through a 500Ω resistor to 5 Volts.

The $\overline{\text{XMT}}$, $\overline{\text{RCV}}$ and $\overline{\text{CLSN}}$ pins have pulse stretchers on them which enables the LEDs to be visible. When transmission or reception occurs, the LED $\overline{\text{XMT}}$, $\overline{\text{RCV}}$ or $\overline{\text{CLSN}}$ status pins will activate low for several milliseconds. If another transmit, receive or collision conditions occurs before the timer expires, the LED timer will reset and restart the timing. Therefore rapid events will leave the LEDs continuously on. The $\overline{\text{JAB}}$ and $\overline{\text{LMON}}$ LEDs do not have pulse stretchers on them since their conditions occur long enough for the eye to see.

LOW LIGHT CONDITION

The $\overline{\text{LMON}}$ LED output is used to indicate a low light condition. $\overline{\text{LMON}}$ is activated low when both the receive power exceeds the Link Monitor threshold and there are transitions on V_{IN}+, V_{IN}– less than 3µs apart. If either one of these conditions do not exist, $\overline{\text{LMON}}$ will go high.

INPUT AMPLIFIER

The V_{IN}+, V_{IN}– input signal is fed into a limiting amplifier with a gain of about 100 and input resistance of 1.3kΩ. Maximum sensitivity is achieved through the use of a DC restoration feedback loop and AC coupling the input. When AC coupled, the input DC bias voltage is set by an on-chip network at about 1.7V. These coupling capacitors, in conjunction with the input impedance of the amplifier, establish a high pass filter with 3dB corner frequency, f_L, at

$$f_L = \frac{1}{2\pi 1300C} \quad (1)$$

Since the amplifier has a differential input, two capacitors of equal value are required. If the signal driving the input is single ended, one of the coupling capacitors can be tied to AV_{CC} as shown in figure 1.

The internal amplifier has a lowpass filter built-in to band limit the input signal which in turn will improve the signal to noise ratio.

Although the input is AC coupled, the offset voltage *within* the amplifier will be present at the amplifier's output. This is represented by V_{OS} in figure 4. Inorder to reduce this error a DC feedback loop is incorporated. This negative feedback loop nulls the offset voltage, forcing V_{OS} to be zero. Although the capacitor on V_{DC} is non-critical, the pole it creates can effect the stability of the feedback loop. To avoid stability problems, the value of this capacitor should be at least 10 times larger than the input coupling capacitors.

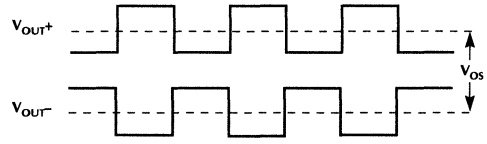


Figure 4.

The comparator is a high-speed differential zero crossing detector that slices and accurately digitizes the receive signal. The output of the comparator is fed in parallel into both the receive squelch circuit and the loopback MUX.

LINK DETECT CIRCUIT AND LOW LIGHT

The link detect circuit monitors the input signal and determines when the input falls below a preset voltage level. When the input falls below a preset voltage, the ML4663 goes into the Low Light state. In the Low Light state the transmitter is disabled, but continues sending the 1MHz idle signal, the loopback is disabled, the receiver is disabled, and the $\overline{\text{LMON}}$ LED pin goes to high shutting off the $\overline{\text{LMON}}$ LED. To return to the Link Pass state, the optical receiver power must be 20% higher than the shut-off state. This built-in hysteresis adds stability to the Link Monitor circuit. Once the receiver power threshold is exceeded, the ML4663 waits 250ms to 750ms, then checks to see that Tx+. Tx– is idle and no data is being received before re-enabling the transmitter, receiver, loopback circuit, and lighting up the $\overline{\text{LMON}}$ LED.

The V_{THADJ} pin is used to adjust the sensitivity of the receiver. The ML4663 is capable of exceeding the 10BASE-FL specifications for sensitivity. The sensitivity is dependent on the layout of the PC board. A good low noise layout will exceed the 10BASE-FL specifications, while a poor layout will fail to meet the sensitivity and BER spec.

The threshold generator shifts the reference voltage at V_{THADJ} through a circuit which has a temperature coefficient matching that of the limiting amplifier. The relationship between the V_{THADJ} and the V_{TH} (the peak to peak input threshold) is:

$$V_{THADJ} = 408V_{TH} \quad (2)$$

In a 10BASE-FL receiver there must be less than 1×10^{-9} bit errors at a receive power level of –32.5dBm average. One procedure to determine the sensitivity of a receiver is to start at the lowest optical power level and gradually increase the optical power until the BER is met. In this case the Link Detect circuit must not disable the receiver (i.e. V_{THADJ} should be tied to Ground). Once the sensitivity of the receiver is determined, V_{THADJ} can be set just above the power level that meets the BER specification. This way the receiver will shut-off before the BER is exceeded.

For 10BASE-FL V_{THADJ} can be tied directly to V_{REF}. However if greater sensitivity is required the circuit in figure 5 can be used to adjust the V_{THADJ} voltage. Even if V_{REF} is tied to V_{THADJ}, it is a good idea to layout a board with these two resistors available. This will allow potential future adjustments without board revisions.

The response time of the Link Detect circuit is set by the C_{TIMER} pin. Starting from the link off state the link can be switched on if the input exceeds the set threshold for a time given by:

$$T = \frac{C_{TIMER} \times 0.7V}{700\mu A} \quad (3)$$

To switch the link from on to off, the above time will be doubled. A value of 0.05µF will meet to 10BASE-FL specifications.

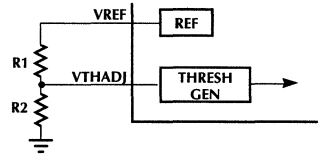


Figure 5.

DIFFERENCES BETWEEN 10BASE-FL AND FOIRL

10BASE-FL is an improved version of the original FOIRL standard. The 10BASE-FL standard allows backward compatibility of a 10BASE-FL transceiver with a FOIRL transceiver. The main improvements incorporated into 10BASE-FL are that it can attach to a DTE by adding the SQE test, and the distance has been increased from 1Km to 2Km. The other differences are much more subtle.

1. SQE Test: The FOIRL standard did not include the option of attaching a fiber transceiver to a DTE. Adding the SQE test to 10BASE-FL enables a 10BASE-FL transceiver to attach to a DTE.

2. 0 to at Least 2Km Distance: The FOIRL standard specifies a 1Km distance while 10BASE-FL specifies 2Km. The additional 1Km distance for 10BASE-FL comes from an increased flux budget for the cable of 3.5dB. This 3.5dB increase came from an increase of 2.5dB sensitivity for the receiver and a 1dB improvement for the transmitter. The following table illustrates the transmit and receive power requirements for the two standards. Note: FOIRL specifies optical power in peak and 10BASE-FL specifies it in average. Subtracting 3dB from peak will give the average. In the table below the FOIRL specifications were converted from peak to average power.

TRANSMIT/RECEIVE AVERAGE POWER	MIN	MAX	CONDITIONS
FOIRL			
Transmitter	–12dBm	–21dBm	
Receiver	–12dBm	–30dBm	BER < 10^{-10}
10BASE-FL			
Transmitter	–12dBm	–20dBm	
Receiver	–12dBm	–32.5dBm	BER < 10^{-9}

3. MAU State Diagrams are Different: The state diagrams for 10BASE-FL are similar to 10BASE-T, while the state diagrams for FOIRL are slightly different. The differences are in the AUI loopback, and in the link integrity function.

AUI Loopback — In 10BASE-FL, the DO to DI loopback is always disabled during a collision, and optical receive data is passed through to DI. For FOIRL there are some cases where loopback continues (i.e. DO looped to DI) during a collision, and others where loopback is disabled during a collision. 10BASE-FL is identical to 10BASE-T in this case. Please refer to the IEEE standards for greater detail.

Link Integrity — 10BASE-FL adds an additional state to the Link Integrity Test function that will not allow an exit from the Low Light State until both the transmitter and receiver are idle. In FOIRL it is possible to exit from the Low Light State while still receiving data.

MAU Timing Differences — The timing differences between 10BASE-FL and FOIRL relate to propagation delays, start-up delays, and collision deassert delays. The following table provides the details of these parameters.

TIMING PARAMETER DIFFERENCES	FOIRL (BIT TIMES)	10BASE-FL (BIT TIMES)
ORD_input to input on DI		
Steady State Prop Delay	0.5	2
Start-Up Delay	3.5	5
output on DO to OTD_output		
Steady State Prop Delay	0.5	2
Start-Up Delay	3.5	5
Collision Deassert to SQE Deassert minimum	4.5	0

OTD — Optical Transmit Data
ORD — Optical Receive Data
DI, DO, CI — AUI Interface Signals

TIMING DIAGRAMS

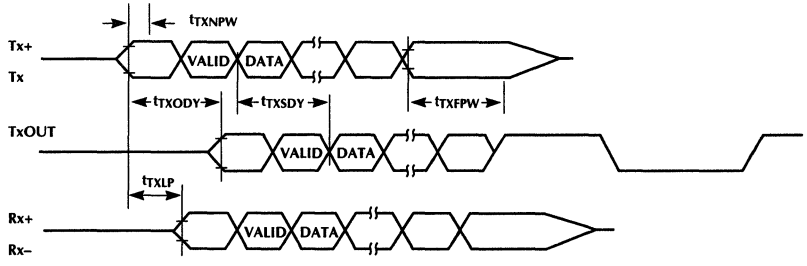


Figure 6. Transmit and Loopback Timing

TIMING DIAGRAMS

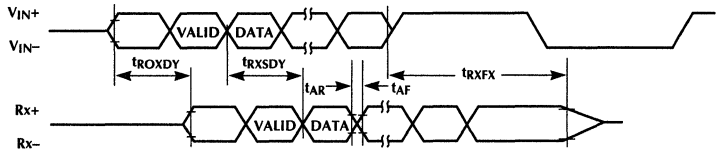


Figure 7. Receive Timing

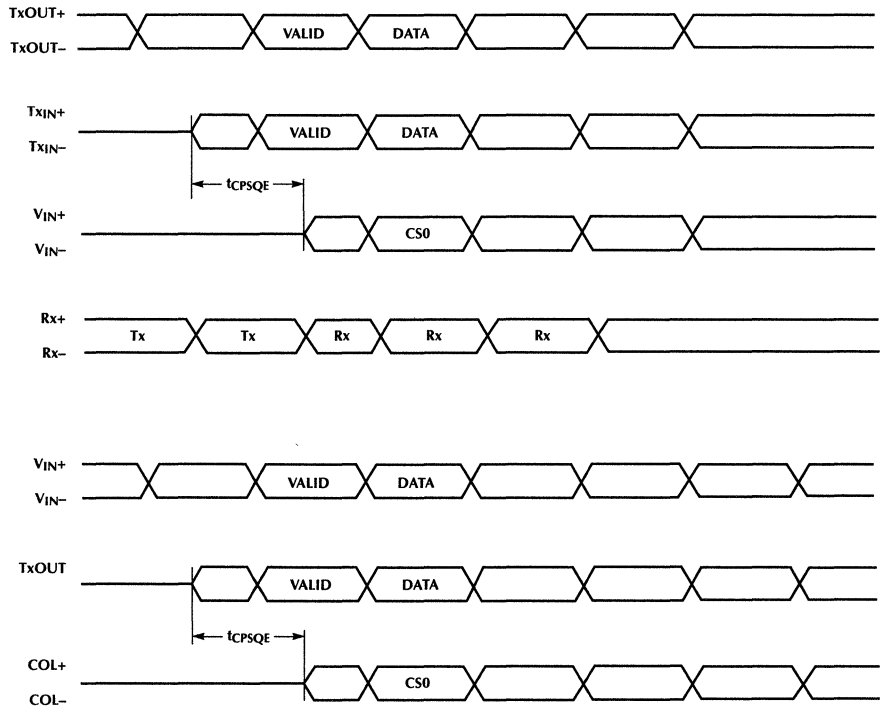


Figure 8. Collision Timing

TIMING DIAGRAMS

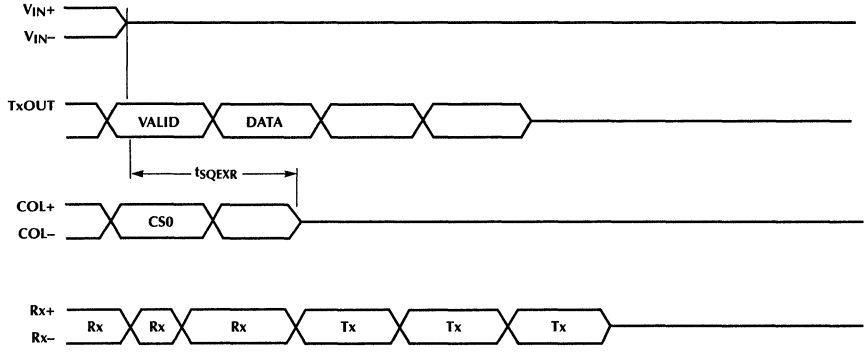


Figure 9. Collision Timing

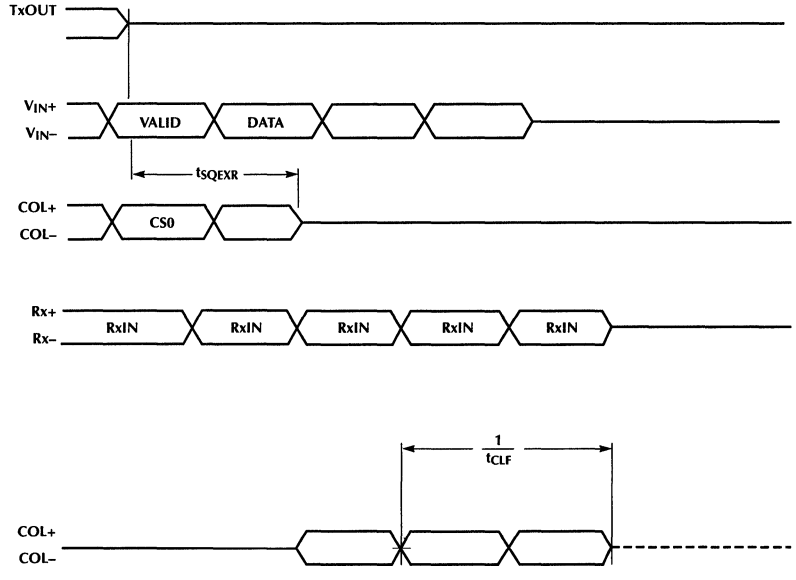


Figure 10. Collision Timing

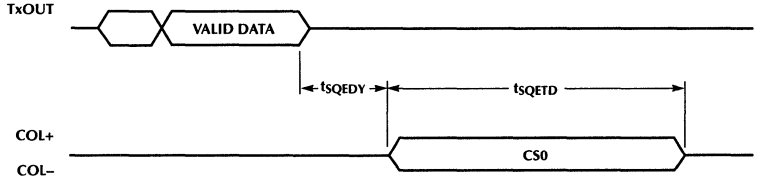


Figure 11. SQE Timing

TIMING DIAGRAMS

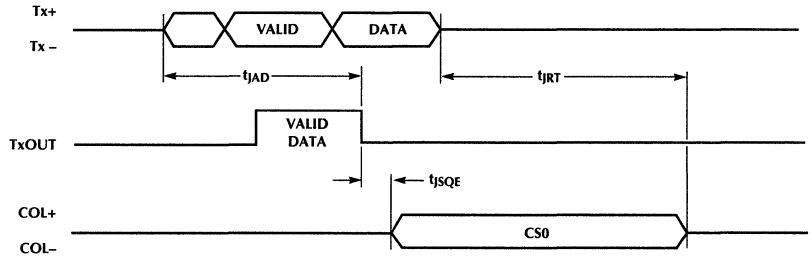


Figure 12. Jabber Timing

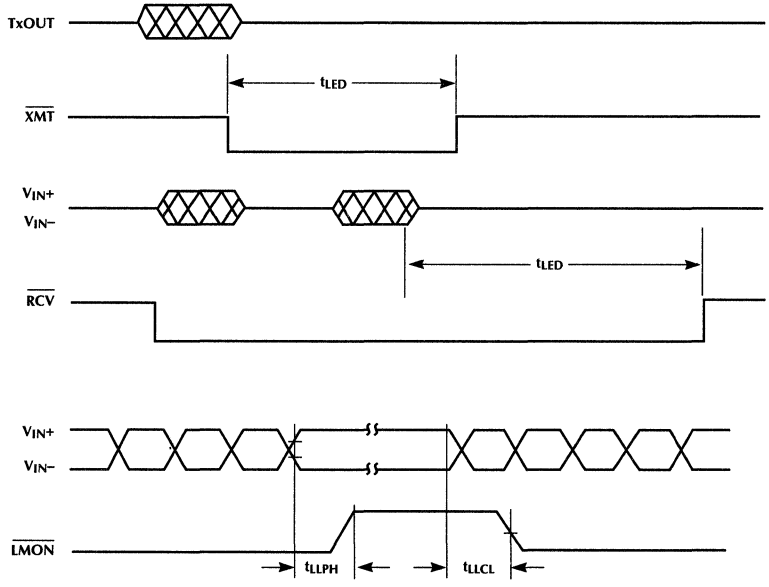


Figure 13. LED Timing

ORDERING INFORMATION

PART NUMBER	PIN COUNT	PACKAGE
ML4663CQ	28 Pins	Molded PCC (Q28)

ML4663EVAL

10BASE-FL Evaluation Kit

GENERAL DESCRIPTION

The ML4663EVAL is an external MAU designed to evaluate the ML4663 10BASE-FL PMD chip. The board interfaces to the AUI port through the transformer and to the fiber optic cable through the HP fiber optic transmitter and receiver.

FEATURES

- Jumper switches to enable or disable Loop Back.
- Jumper switches to enable or disable SQE and Jabber functions.
- Capable of adjusting the receive sensitivity.
- 6 status LEDs.
- Current consumption 260-280mA typically

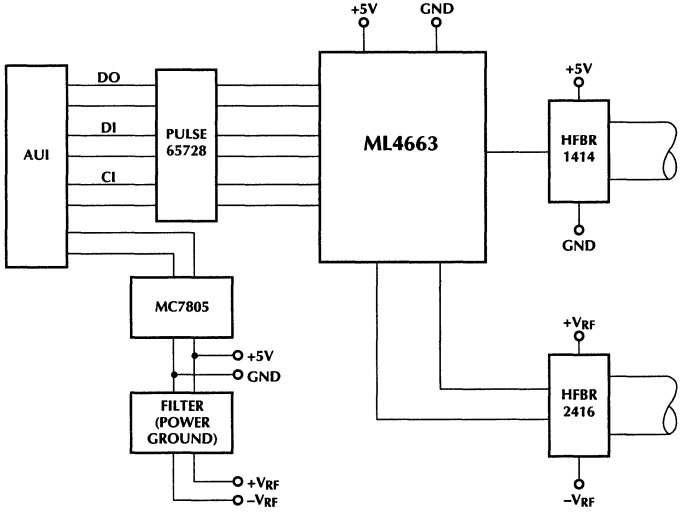
KIT COMPONENTS

The ML4663EVAL kit includes the following items to help the customer speed their design, layout and debug process.

1) BLANK PCB: 4 layer board with separate power and ground plane (inner layers).
2) COMPONENT KIT: Includes the key components as listed below. The rest of the components should be provided by the customer based on the parts list of the ML4663EVAL.
   - HFBR1414: HP fiber Optic LED transmitter.
   - HFBR2416: HP fiber optic pin diode receiver.
   - One 28 pin sockets for the ML4663.
   - ML4663CQ: 10BASE-FL combo transceiver and quantizer.
   - PE65728: PULSE AUI coupling transformer.
   - AUI CONNECTOR: 15 pins D SUB connector.
3) DOCUMENTATION: includes the following items:
   - Demo board description.
   - Block Diagram of the DEMO board.
   - Schematic of the demo board.
   - Lay out of the demo board.
   - Parts list of the ML4663EVAL.

4

BLOCK DIAGRAM



ML4670

Multi-Protocol Physical Interface

GENERAL DESCRIPTION

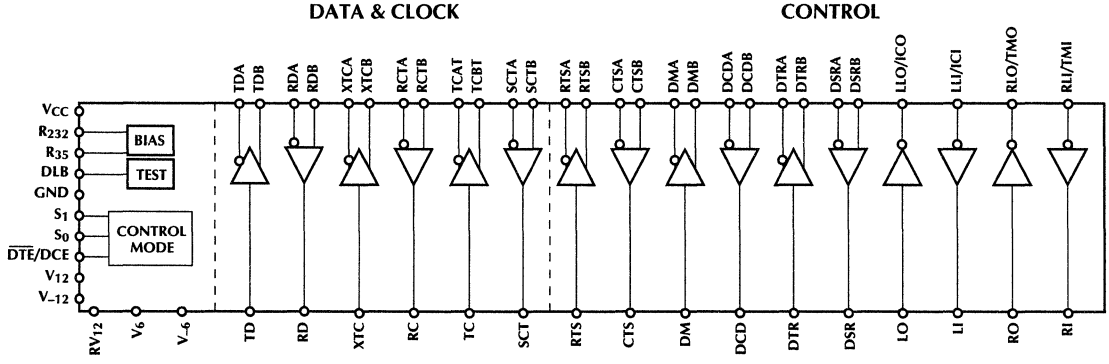
The ML4670 Multi-Protocol Interface Device is designed primarily for use in and with bridge, router and frame relay equipment. The device provides the serial communications interface for DCE or DTE applications that require RS-232, RS-449, X.21/V.36 or V.35 protocols.

The ML4670 offers system designers a single chip that provides the physical electrical interface for the four most commonly used serial protocols. The device is programmable with standard, static TTL levels that select the desired electrical interface for clock, data and diagnostic local loopback control. The selection of the desired interface alters the characteristics of the line drivers and receivers such that the proper interface is available for transmit and receive of clock, data, and control signals for the above listed protocols. The flexibility of the ML4670 allows the implementation of a single device that can be configured to interface with any one of the four desired protocols.

FEATURES

- Programmable physical interfaces for RS-232, RS-449, X.21/V.36, V.35
- Supports DCE/DTE transmit and receive clocks as well as data and control signals
- 200mV hysteresis on all receive inputs for noise immunity
- 10Mb/s data and clock rates for high-speed V.35, X.21, and RS-449 protocols
- DTE/DCE function selectable by single pin
- Resistor programmable slew rate for RS-232 transmitters
- Pin selectable diagnostic loopback mode
- ±12V or ±6V power supply flexibility for RS-232 implementation
- 84-pin PLCC package

BLOCK DIAGRAM



ML6622

High-Speed Data Quantizer

GENERAL DESCRIPTION

The ML6622 High-Speed Data Quantizer is a low noise, wide-band, BiCMOS monolithic IC designed specifically for signal recovery applications in FDDI and SONET fiber-optic receiver systems. An internal DC restoration feedback loop nulls any offset voltage produced in the input stage. The limiting amplifier contributes to a high level of sensitivity and a minimum of duty cycle distortion.

The output of the data path is a high-speed comparator with ECL outputs. An enable pin gates the comparator on or off in response to the input signal level or a system control signal.

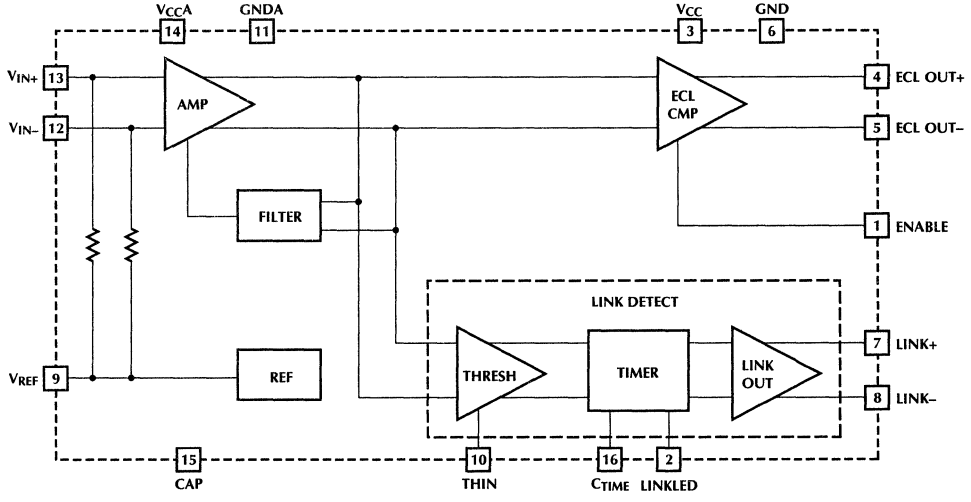
The Link Detect circuit provides an Assert-Deassert function with a user-selectable threshold voltage. This circuit monitors the input signal and provides an ECL High output within 100ms of signal acquisition and an ECL Low output within 350ms of signal loss. The ECL discriminator output can be used to disable the comparator when the signal is below the user-selected threshold. LINKLED drives an LED for a visible indication of the link status.

FEATURES

- 150 MHz bandwidth
- Low noise design
- Adjustable Link Detect function
- Low power design: 35mA typical
- Available in 16-pin DIP and 16-pin Skinny SOIC

4

BLOCK DIAGRAM



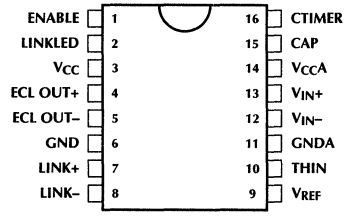
PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	ENABLE	ECL input active low. When this input is tied to LINKLED the ECL comparator output is automatically enabled and disabled by the Link Detect circuit. This input can be tied to GND for continuous enable. When the ECL Comparator is disabled, ECL OUT– goes low and ECL OUT+ goes high.
2	LINKLED	Link Detect Status output. LINKLED is an open collector active low signal. It will be active low when the input signal applied to V_{IN+},V_{IN-} exceeds the programmed threshold level at the THIN pin. Capable of driving a 20mA LED indicator.
3	V_{CC}	Positive Power Supply. +5 volts
4 5	ECL OUT– ECL OUT+	Positive and Negative ECL Comparator outputs. 1mA internal pull downs are incorporated so that external pull downs aren't required for light loads.
6	GND	Ground connection. Used for less noise sensitive nodes.
7	LINK+	Positive ECL Link Detect output. Active high when the input signal exceeds the programmed Link Detect threshold. 1mA internal pull down current sources.
8	LINK –	Negative ECL Link Detect output. Active low when the input signal exceeds the programmed Link Detect threshold. 1mA internal pull down current sources.
9	V_{REF}	A 2.5V reference with respect to GND.

NAME	PIN #	FUNCTION
10	THIN	Threshold Input. A voltage applied to this input pin sets the minimum amplitude of the input signal required to cause the link detect to activate. In most cases this can be tied to V_{REF}.
11	GNDA	Ground connection for noise sensitive circuits in the chip; the input amplifier, DC restoration loop, part of the Comparator and part of the link detect circuit. In some system designs, it may be advantageous to separate GND and GNDA.
12	V_{IN-}	This input pin should be capacitively coupled to the input source or to V_{CC}.
13	V_{IN+}	This input pin should be capacitively coupled to the input source or to V_{CC}.
14	$V_{CC}A$	Positive power supply V_{CC} for noise sensitive circuits as mentioned in GNDA. +5 volts.
15	CAP	A capacitor is tied from this pin to V_{REF}. This capacitor sets the lower frequency rejection and helps remove internal DC offset. This capacitor should be 10 times larger than the input capacitors.
16	C_{TIMER}	A capacitor from this pin to ground determines the Link Detect response time. To Meet FDDI specifications this capacitor should be 2,000pF. This capacitor can be removed for faster response time.

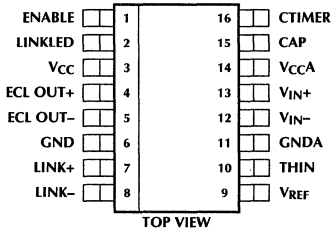
PIN CONNECTION

ML6622
16-Pin DIP (P16)



TOP VIEW

ML6622
16-Pin Narrow SOIC (S16N)



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} – GND ..... –0.3 to +7.0
$V_{CC}A$ – GNDA ..... –0.3 to +7.0
Inputs/Outputs GND ..... –0.3 to V_{CC} +0.3
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C

ELECTRICAL CHARACTERISTICS

Over recommended operating conditions of T_A = 0°C to 70°C, V_{CC} = 5V ±5%, GND = 0V, unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	V_{CC} Supply Current (No load on ECL outputs)			35	50	mA
V_{REF}	Reference Voltage		2.37	2.47	2.57	V
IV_{REF}	V_{REF} Output Current		–1	3	+5	mA
V_{IN}	Input Signal Range		3.5		1600	mV_{P-P}
V_{TH} ADJ Range	External Voltage at THIN to set V_{TH}		0.5		V_{REF}	V
EN	Input-referred Voltage Noise	100 MHz BW		25		μV_{RMS}
R_{IN}	Input Resistance	V_{IN}+, V_{IN}–	500	770	1000	Ω
I_{THIN}	Input Bias Current of THIN		–100		+100	µA
V_{OL}-V_{CC}	ECL Output Voltage-Low	Through 50Ω to V_{CC} –2V, T_A = 25° C	–1.840	–1.730	–1.620	V
V_{OH}-V_{CC}	ECL Output Voltage-High	Through 50Ω to V_{CC} –2V, T_A = 25° C	–1.045	–0.963	–0.880	V
t_r	Data Output Rise Time					ns
t_f	Data Output Fall Time		0.35		1.3	ns
Link Detect						
AS_Max	Assert Time (off to on)	C_{TIME} = 2000pF	0		100	µs
ANS_Max	Deassert Time (on to off)	C_{TIME} = 2000pF	0		350	µs
V_{TH}	Input threshold Hysteresis	THIN = V_{REF} Assert	8 1.5	10 1.7	12 2	mV dB
BW	Bandwidth 1-3dB			200		MHz
VIPW	Minimum Input Pulse Width			5		ns
DCD	Duty Cycle Distortion Peak-to-peak	Data rate = 155Mb/s 50% duty cycle input		0.5		ns
DDJ	Data Dependent Jitter Peak-to-peak	FDDI – 56 Data Pattern V_{IN} = 60mV, Data rate = 125Mb/s		1.2		ns

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case conditions.

FUNCTIONAL DESCRIPTION

The ML6622 High Speed Data Quantizer accepts a low level analog signal from a pin diode and transimpedance amp front end and converts it into digital ECL levels for subsequent digital processing. The input signal, from a transimpedance amplifier, is immediately amplified by a two-stage video amplifier. The output of this amplifier feeds two parallel paths.

The data path is comprised of a high speed comparator that outputs PECL differential data on the ECL OUT± pins. The Link Detection path monitors the magnitude of the amplified input signal, compares it to a user-settable threshold, and provides the result of the comparison as a PECL differential output on the Link± pins. The timer following the threshold block is used to set the Link Detect output acquire and deacquire time using a capacitor.

AMPLIFIER

The amplifier is a two stage video amplifier with a gain of approximately 55V/V. Maximum sensitivity is achieved through the use of the DC restoration feedback loop and AC coupling the input. The AC coupling input capacitors, in conjunction with the input impedance of the amplifier, establishes a high pass filter with the lower 3dB point determined by the input resistance and the input coupling capacitors.

Since the amplifier has a differential input, two AC capacitors of equal value are required. If the signal driving the input is single ended, the other coupling capacitor should be tied to V_{CC}.

Another low-pass filter is created with the CAP capacitor. The lower 3dB point controlled by a capacitor tied from the CAP pin to V_{REF} as shown in the application circuit. For stability reasons the value of the capacitor on the CAP pin should be 10 times larger than the input coupling capacitors. The 3dB point is given by the following equation:

$$F_{3dB} = \frac{1}{2\pi 100C}$$

Although the input is AC coupled, the offset voltage within the amplifier will be present at the amplifier's output. The removal of the dc offset in the amplifier helps the circuit respond to small input voltages, and reduces duty-cycle distortion. In order to reduce this error, a negative feedback loop nulls the offset voltage. An external capacitor connected to the CAP pin is used to store the offset voltage. This voltage is compared to V_{REF} and a difference current proportional to the result is applied to the negative side of the input stage of the AMP circuit block thereby nulling the DC offset.

COMPARATOR

A high speed ECL comparator with PECL outputs is used for the quantization function. The comparator has an Enable input pin which takes an ECL level. This Enable pin is normally driven by LINKLED, which causes the output to be enabled when the link is up and disabled when the link is down. When ENABLE is low the comparator is operational. When ENABLE is high the comparator is disabled causing ECL OUT– to go low and ECL OUT+ to go high. The ENABLE pin can be tied to ground to keep the comparator permanently enabled.

LINK DETECT CIRCUIT

The Link Detection Circuit is used to accurately measure the input amplitude to determine whether it is large enough to reliably recover the input signal. Once the Bit Error Rate (BER) for the ML6622 receive circuit is determined, the link detect threshold can be set so that the Link Detect Circuit will shut off before the error rate exceeds the link requirement.

The Link Detection Circuit consists of three functional blocks; Thresh, Timer, and Link Out. Thresh detects the output of Amp and compares it to a programmable threshold input THIN. As long as the input amptitude is greater than the programmable threshold input, the Link Detect output remains active.

When the peak input drops below THIN, Thresh's output changes state and Timer delays the Link Out state change for a programmable amount of time. When using the default C_{TIME} capacitance of 2000pF, the deassert time and the assert time values conform to the ANSI X3.166-1990 PMD standard for FDDI.

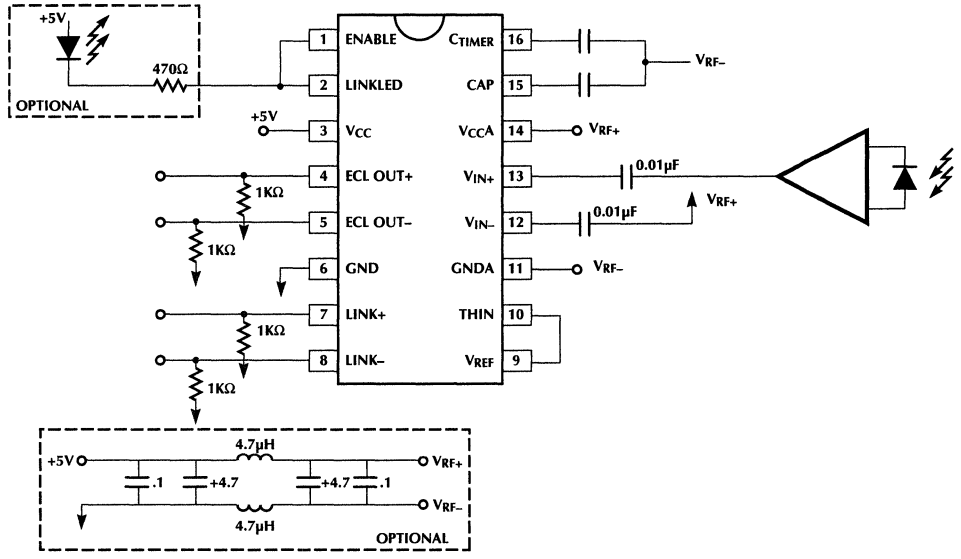
To improve stability, the Link Detect circuit includes 1.7dB of hysteresis.

The V_{REF} output can be tied directly to THIN to set the Link Detect threshold. For greater sensitivities, V_{REF} can be divided down before applied to THIN. The formula for the threshold on the thin pin is as follows:

$$\text{Threshold(Assert)} = \frac{V_{THIN}}{500}$$

$$\text{Threshold(Deassert)} = \frac{V_{THIN}}{750}$$

APPLICATION CIRCUIT



4

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6622CP	0° to +70°C	16-Pin MOLDED DIP (P16)
ML6622CS	0° to +70°C	16-Pin MOLDED SOIC (S16N)

ML6633

High Speed Fiber Optic LED Driver

GENERAL DESCRIPTION

The ML6633 is a high speed fiber optic LED driver suited for networking applications up to 200 Mbps. The part is capable of driving up to 75 mA of current through a fiber optic LED from an ECL level input signal. Its efficient output stage provides a high current that can be programmed for accurate absolute output level which insures precise launch power.

The LED driver's output stage provides a fast well matched rise and fall time through a unique differential output stage.

The ML6633 high speed fiber optic LED driver is implemented in BiCMOS process and is available in an 8-pin SOIC or PDIP package.

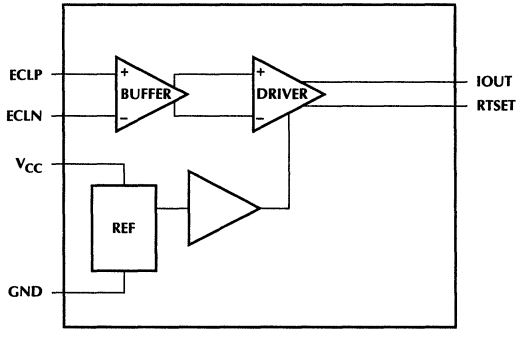
FEATURES

- Data rates up to 200 Mbps
- Current driven output for accurate launch power
- Programmable output current from 20 mA to 75 mA
- High Efficiency Output Stage
- Low EMI/RFI Noise
- ECL inputs

APPLICATIONS

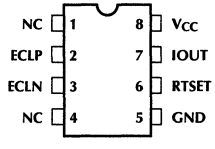
- Fiber Optic Token Ring
- FDDI
- SONET OC1 and OC3
- Fiber Optic Data Communications and Telecommunications

BLOCK DIAGRAM



PIN CONNECTION

8-Pin SOIC or PDIP



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	NC	
2	ECLP	Positive ECL data input controls signal to the LED.
3	ECLN	Negative ECL data input.
4	NC	
5	GND	Negative power supply ground.
6	RTSET	Output current programming pin. Connect a resistor of value $2/I_{LED}$ from this pin to ground to set the high LED output current.
7	IOUT	Fiber optic LED drive pin. Connect the LED between this pin and V_{CC}.
8	V_{CC}	Positive power supply. +5 volts.

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC} ..... –0.3V to 6V
Input Pin Voltages ..... –0.3V to V_{CC} +0.3V
LED Output Current (IOUT) 75mA
Peak DC Output Current (IOUT) 75mA
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... 260°C

4

ELECTRICAL CHARACTERISTICS

Over the recommended operating conditions of T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, RTSET = 26.1Ω ± 1%, unless otherwise specified. (Notes 2 and 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
I_{CC}	Supply Current				40mA+I_{OUT}	mA
	LED Current Accuracy (IOUT)					
I_{LEDH}	High		70	75	80	mA
I_{LEDL}	Low				0.1	mA
t_R	Rise Time (IOUT)				2	ns
t_F	Fall Time (IOUT)				2	ns
	Propagation Delay (IOUT)					
t_{PLH}	Low to High				10	ns
t_{PHL}	High to Low				10	ns
t_{PWD}	Pulse Width Distortion (IOUT)				1.0	ns
I_{ECL}	ECL Input Current				20	µA

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground
Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions
Note 3: Low Duty Cycle pulse testing is performed at T_A.

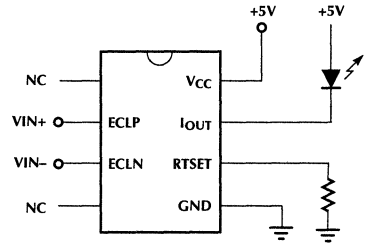
FUNCTIONAL DESCRIPTION

The ML6633 accepts ECL input signals and generates a high speed, high accuracy output current which is independent of supply voltage variations. The output current is programmable from 75mA.

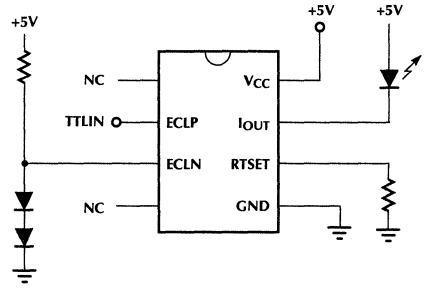
The ECL input stage is a standard NPN differential pair with a common mode range of between 1V and 4.5V with a +5V supply. With this common mode range it is possible to convert the ECL inputs into TTL. If the ECLN input is biased up to the TTL switching level, the ECLP pin can be driven by a TTL or CMOS output. Figure 1b shows a circuit implementing this technique. This circuit may degrade pulse width distortion and should be checked for acceptable performance in this configuration.

Output current to the LED is set by connecting the appropriate resistance from RTSET to ground. The high level output voltage at RTSET will be 2.0V. The current in the external resistor will be equal to the current through the LED. The output current with RTSET set to 26.1Ω will be:

$$I_{LED}(HIGH) = 2.0V/R_{TSET} = 2.0V/26.1\Omega = 75mA.$$



a) I_{OUT} = 75mA



b)

Figure 1. Typical Applications

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6633CP	0°C to +70°C	8-Pin Molded DIP (P08)
ML6633CS	0°C to +70°C	8-Pin SOIC (S08N)

ML6633/22EVAL

High Speed Fiber Optic Evaluation Kit

GENERAL DESCRIPTION

The ML6633/22 evaluation kit is designed for high speed fiber optic applications such as 125Mbaud FDDI (Fiber Data Distributed Interface), OC1 and OC3 SONET (Optical Carrier-level 1 and 3 for Synchronous Optical Network), and Fiber Channel.

Data inputs and outputs of the ML6633/22EVAL board are designed for high speed ECL lines. 50/125µm or 62.5/125µm fiber optic cable with an ST connector at each end plugged into a 1300nm fiber optic LED and a pin detector in the demo board.

FEATURES

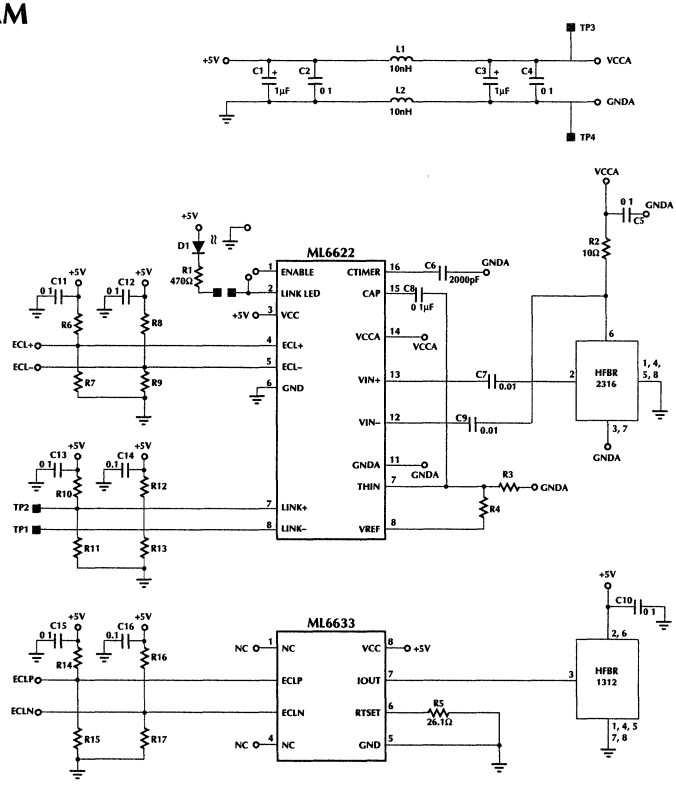
- Adjustable link detect function through R3 and R4
- Fast rise and fall time at the transmitter
- Link LED status
- Low noise design

KIT COMPONENTS

- ML6633/22 user guide
- ML6633 data sheet
- ML6622 data sheet
- ML6633/22 assembled Eval board
- 3.5" disk with Gerber Files

The user guide includes performance data, layout recommendation, layout, schematic, parts list and a tutorial on how to use the demo board.

BLOCK DIAGRAM



ML6671

TP-PMD Transceiver

GENERAL DESCRIPTION

The ML6671 is a complete monolithic transceiver for 125 Mbaud MLT-3 encoded data transmission over Category 5 Unshielded Twisted Pair and Shielded Twisted Pair cables. The adaptive equalizer in the ML6671 will accurately compensate for line losses of up to 100m of UTP. The part requires only external 1% resistors for accurate equalization.

The ML6671 receive section consists of an equalizing filter with a feedback loop for controlling effective line compensation. The feedback loop contains a filter and detection block for determining the proper control signal. The ML6671 also contains data comparators with precisely controlled slicing thresholds and an MLT-3 to NRZI translator. An ECL 100K compatible buffer at the output interfaces directly with existing FDDI PHY silicon from various manufacturers.

The ML6671 transmit section accepts ECL 100K compatible NRZI inputs and converts them to differential current mode MLT-3 signals. Transmit amplitude is controlled by a single external resistor.

Several additional functions are provided by the ML6671 to simplify applications. A common-mode reference is provided to set the input DC level for the equalizer and the near-end transformer winding. This terminal may be used as an AC ground for the transformer center-tap or termination resistors. The transmitter can be disabled to provide true quiet line.

The ML6671 is implemented in a BiCMOS process. A differential signal path throughout minimizes the effects of power supply transients and noise.

FEATURES

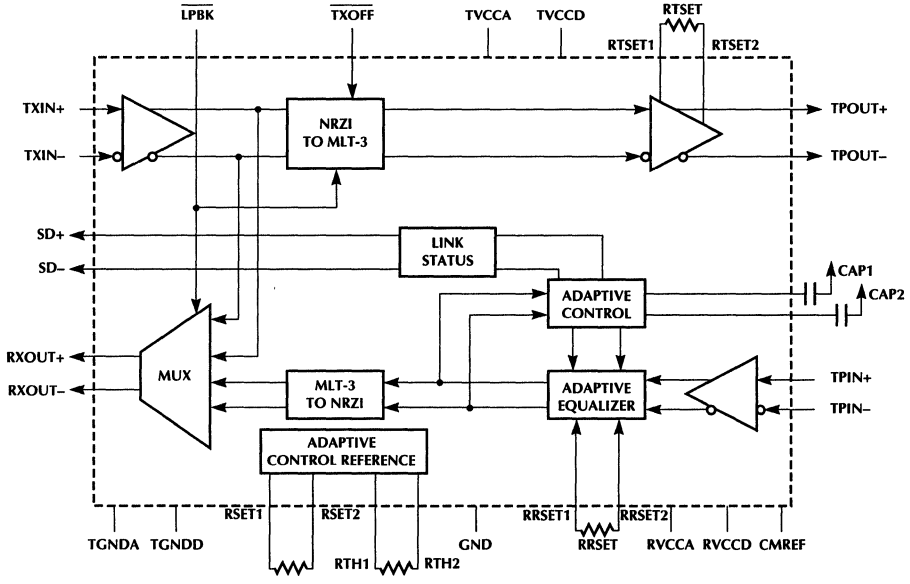
- Transmitter converts NRZI ECL signals to MLT-3 current driven outputs
- Transmitter can be externally turned off for true quiet line
- Receiver includes adaptive equalizer and MLT-3 to NRZI decoder
- Operates over 100 meters of STP or category 5 UTP Twisted Pair Cable
- 32-pin surface mount package

APPLICATIONS

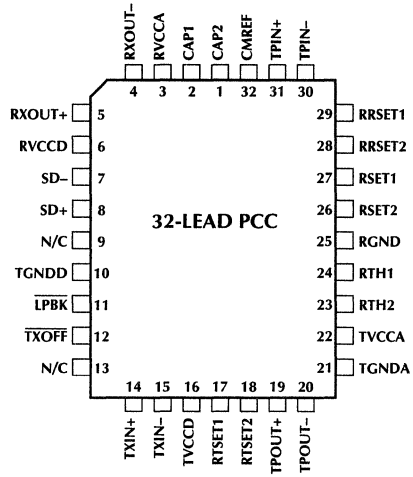
- FDDI over copper (TP-PMD)
- Fast Ethernet (100BASE-TX)

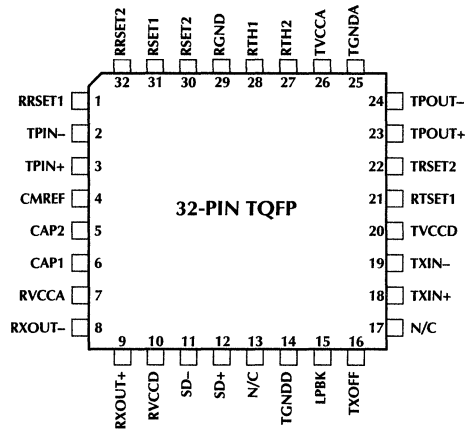
4

BLOCK DIAGRAM



PIN CONFIGURATION





PIN DESCRIPTION

NAME	FUNCTION
TXIN+, TXIN–	These differential ECL100K compatible inputs receive NRZI data from the PHY for transmission.
TPOUT+, TPOUT–	Outputs from the NRZI-MLT3 state machine drive these differential current outputs. The transmitter filter/transformer module connects the media to these pins.
$\overline{\text{LPBK}}$	This TTL input enables transmitter-receiver loopback internally when asserted low.
$\overline{\text{TXOFF}}$	This TTL input forces the NRZI-MLT3 state machine to a quiet state when asserted low.
RTSET1, RTSET2	An external 1% resistor connected between these pins controls the transmitter output current amplitude. I_{OUT} = 64 x 1.25V/RTSET
TVCCA, TVCCD	Separate analog and digital transmitter power supply pins help to isolate sensitive circuitry from noise generating digital functions. Both supplies are nominally +5 volts.
TGNDA, TGNDD	Analog and digital transmitter grounds provide separate return paths for clean and noisy signals.
SD+, SD–	These differential ECL100K compatible outputs indicate the presence of a data signal with an amplitude exceeding a preset threshold.
TPIN+, TPIN–	MLT-3 encoded data from the receiver filter/ transformer module enters the receiver through these pins.

NAME	FUNCTION
RXOUT+, RXOUT–	Differential ECL100K compatible outputs provide NRZI encoded data to the PHY.
CAP1, CAP2	Two external capacitors connected to these pins sets the time constant for the adaptation in the equalizer loop as well as for signal detect response.
RRSET1, RRSET2	Internal time constants controlling the equalizer's transfer function are set by an external resistor connected across these pins.
CMREF	This pin provides a DC common mode reference point for the receiver inputs.
RVCCA, RVCCD	Analog and digital supply pins are separated to isolate clean and noisy circuit functions. Both supplies are nominally +5 volts.
RGND	Receiver ground.
RSET1, RSET2	An external 5KΩ resistor across these pins sets up an internal reference current.
RTH1, RTH2	An external resistor connected across these pins sets the internal levels for equalization as well as signal detect. This resistor allows compensation for transmit and magnetics variations. RTH should be set to match the peak-to-peak transmit amplitude. V_{AMP} = 16 x 1.25 x RTH/RSET where V_{AMP} is the peak-to-peak amplitude of the transmit output with zero length cable.

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage Range ..... –0.3V to 6V
Input Voltage Range
  Digital Inputs ..... –0.3V to V_{CC}
Output Current
  TPOUT±, SD±, RXOUT± 50mA
  All other outputs 10mA
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

V_{CC} Supply Voltage ..... 5V ± 5%
T_A, Ambient Temperature ..... 0°C to +70°C
RTSET ..... 2KΩ ±1%
RRSET ..... 8KΩ ±1%
RSET ..... 5KΩ ±1%
RTH ..... 500Ω ±1%
CAP1, CAP2 ..... 0.33µF ±5%

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ±5%, RTSET = 2.0KΩ, RTH = 500Ω.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics					
Supply Current					
RVCCD			67		mA
RVCCA			52		mA
TVCCD			25		mA
TVCCA			6		mA
RVCCD + RVCCA + TVCCD + TVCCA				170	mA
TTL Inputs ($\overline{TXOFF}$, $\overline{LPBK}$)					
V_{IL} Input Low Voltage				0.8	V
V_{IH} Input High Voltage		2.0			V
Differential Inputs (TPIN±, TXIN±)					
TPIN+, TPIN– Common Mode Input Voltage		2.2		V_{CC}	V
TPIN+, TPIN– Differential Input Voltage				1.5	V
TPIN+, TPIN– Differential Input Resistance		10.0K			Ω
TPIN+, TPIN– Common Mode Input Current				+10	µA
TXIN+, TXIN– Input Voltage HIGH (V_{IH})		V_{CC}–1.165		V_{CC}–0.88	V
TXIN+, TXIN– Input Voltage LOW (V_{IL})		V_{CC}–1.810		V_{CC}–1.475	V
TXIN+, TXIN– Input Current LOW (I_{IL})		0.5			µA
TXIN+, TXIN– Input Current HIGH (I_{IH})				50	µA
Differential Outputs (SD±, RXOUT±, TPOUT±)					
SD+, SD–, RXOUT+, RXOUT– Output Voltage HIGH (V_{OH})	Note 5	V_{CC}–1.025		V_{CC}–0.88	V
SD+, SD–, RXOUT+, RXOUT– Output Voltage LOW (V_{OL})	Note 5	V_{CC}–1.81		V_{CC}–1.62	V
TPOUT+, TPOUT– Output Current HIGH	$V_{OUT} = V_{CC} \pm 0.5$, Note 4	38.0		42.0	mA
TPOUT+, TPOUT– Output Current LOW	$V_{OUT} = V_{CC} \pm 0.5$, Note 4	0		0.5	mA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Outputs (SD±, RXOUT±, TPOUT±) (Continued)					
TPOUT+, TPOUT– Output Current Offset	Note 3			0.5	mA
TPOUT+, TPOUT– $V_{OUT} = V_{CC}$ Output Amplitude Error	Note 3, 4	–5.0		5.0	%
TPOUT+, TPOUT– $V_{OUT} = V_{CC} \pm 1.1V$ Output Voltage Compliance		–2.0		+2.0	%
AC Characteristics					
TPOUT+, TPOUT– Rise/Fall Time	Note 2		2.0		ns
TPOUT+, TPOUT– Output Jitter	Note 2		0.8		ns
RXOUT+, RXOUT– Rise/Fall Time	Note 2			5	ns
RXOUT+, RXOUT– Output Jitter	Note 2		2.0		ns

Note 1. Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2. Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3. Low Duty cycle pulse testing is performed at T_A.

Note 4. Output current amplitude is determined by I_{OUT} = 64 x 1 25V/RTSET.

Note 5. Output voltage levels are specified when terminated by 50Ω to V_{CC} – 2V or equivalent load.

FUNCTIONAL DESCRIPTION

The ML6671 MLT-3 transceiver is a physical media dependent transceiver that allows the transmission and reception of 125 Mbaud data up to 100 meters over shielded twisted pair cable or category 5 unshielded twisted pair cable. It provides a standard Physical Media Dependent (PMD) interface compatible with many FDDI chip sets.

The transmit section accepts NRZI data, converting it to a three level MLT-3 code and sending the information on a two pin current driven transmitter. The transmitted output passes through an external low pass filter and transformer before entering the connectors to the STP or UTP cable. The output amplitude of the transmitted signal is programmable through the external RTSET resistor.

The receive section accepts MLT-3 coded data after passing through an isolation transformer and band limiting filter. Before the data con be converted from MLT-3 back to NRZI, the adaptive equalizer is used to compensate for the amplitude and phase distortion incurred from the cable. The adaptive control section determines the cable length and adjusts the equalizer accordingly.

The adaptive control block governs both the equalization level as well as the link detection status. The link detection threshold has a fixed relationship to the overall equalization level which is currently 25% of the transmitted amplitude. For the link status to be true, a minimum level signal must be received. When the input signal is small, the equalization will be at its maximum.

After the signal has been equalized, it passes into the MLT-3 to NRZI converter where it is converted back to NRZI and fed through the loopback multiplexer onto the RXOUT± pins.

Figure 1 shows a timing diagram of NRZI data and the equivalent MLT-3 data. The MLT-3 data shows the output current I_{OUT} for one side of the transmitter, either TPOUT+ or TPOUT–. The other transmit output pin will be the complement. Whenever there is a change in level in NRZI, MLT-3 will change levels too. The maximum fundamental frequency of MLT-3 is half of the maximum fundamental of NRZI.

Figure 2 shows a typical gain vs frequency plot of the adaptive equalizer for 0, 25, 50, 75 and 100 meter category 5 cable lengths.

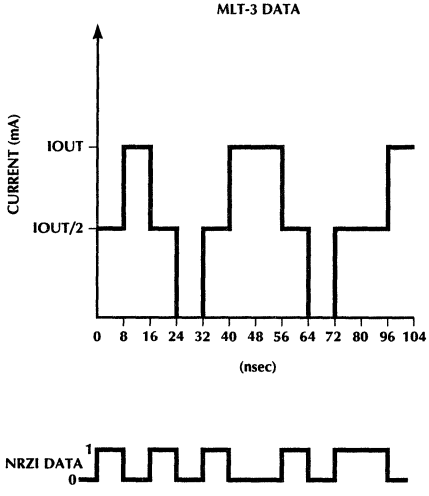


Figure 1. MLT-3 Encoding

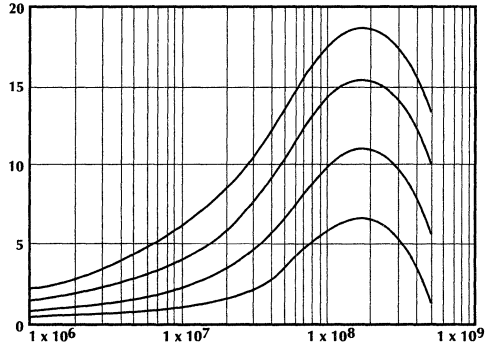
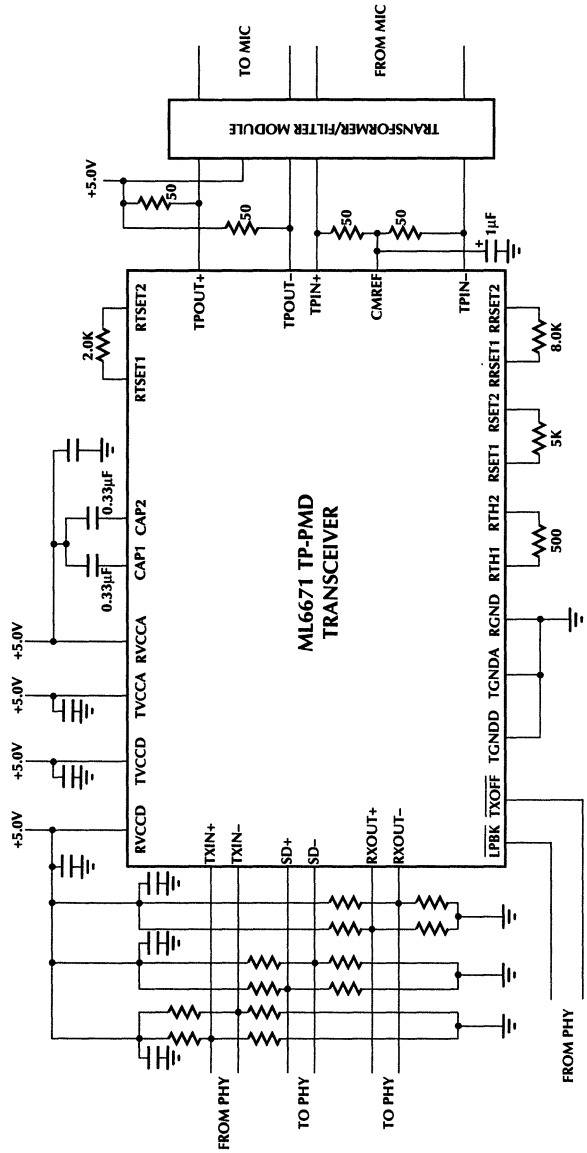


Figure 2. Equalization Range



Application Example of ML6671 Configured for 2.0V_{P-P} Transmit Amplitude on C5 UTP.

Note 1. Split 100K ECL terminations are 82Ω and 130Ω to VCC and GND respectively.
Note 2. Recommended power supply bypass capacitors are 0.1µF with optional 10µF tantalum in parallel.
Note 3. Transformer turns ratio is 1:1.
Note 4. LPBK and TXOFF inputs are active LOW.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6671CQ	0°C to +70°C	32-Pin Molded Leaded PCC (Q32)
ML6671CH	0°C to +70°C	32-Pin TQFP (H32)

ML6671-22EVAL

TP-PMD Transceiver Evaluation Kit

GENERAL DESCRIPTION

The ML6671-22EVAL board is a TP-PMD transceiver designed to replace an existing 1402U ODL FDDI transceiver (22-pin). This permits the conversion of an existing fiber-based FDDI adapter card or concentrator to a copper-based FDDI design.

At one end, the ML6671 demo board interfaces to an RJ45 connector through a transformer and common mode choke. The other end of the evaluation board interfaces to a 22-pin ODL footprint.

FEATURES

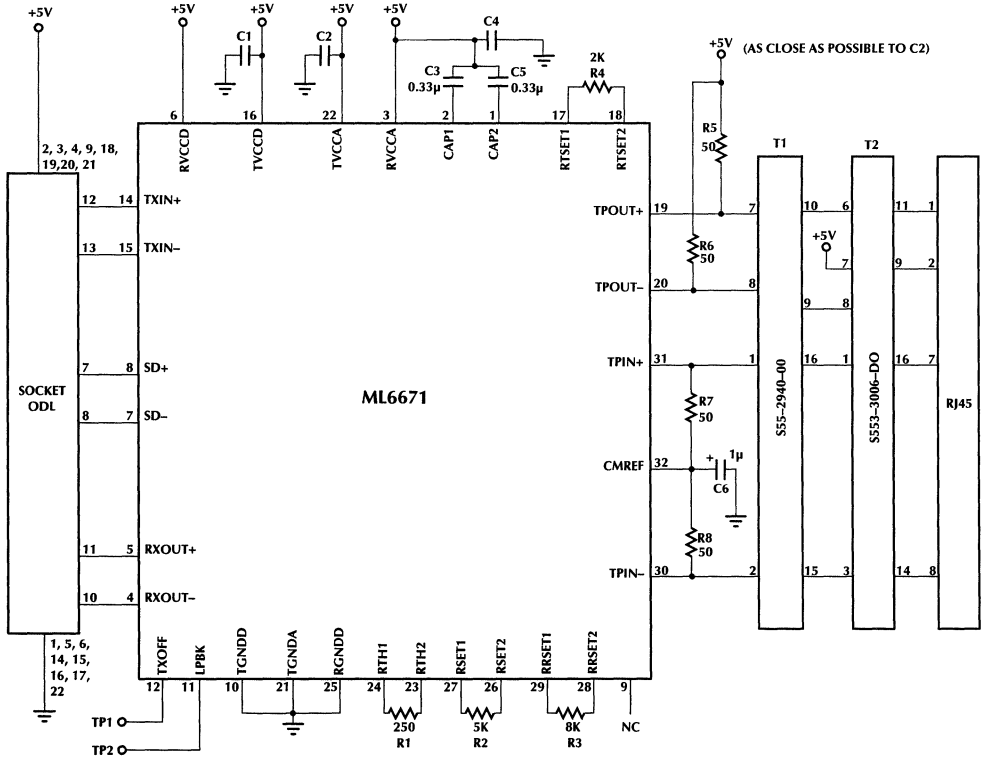
- Loop back capability
- Quiet line by turning the transmitter off
- Low jitter
- Fast rise and fall times at the transmitter

KIT COMPONENTS

- ML6671-22EVAL user guide
- Application Note 28
- ML6671 data sheet
- Assembled evaluation board
- 3.5" disk with Gerber Files

The user guide includes performance data, layout recommendations, layout, schematic, parts list and a tutorial on how to use the demo board.

BLOCK DIAGRAM



ML6672

ATM UTP Transceiver

GENERAL DESCRIPTION

The ML6672 is a complete monolithic transceiver for 155Mbps NRZ encoded data transmission over Category 5 Unshielded Twisted Pair and Shielded Twisted Pair cables. The ML6672 is compliant with the ATM Forum 155Mbps Twisted Pair Specification. The adaptive equalizer in the ML6672 will accurately compensate for line losses of up to 100m of UTP. The part requires only external 1% resistors for accurate equalization.

The ML6672 receive section consists of an equalizing filter with a feedback loop for controlling effective line compensation. The feedback loop contains a filter and detection block for determining the proper control signal. An ECL 100K compatible buffer at the output interfaces directly with ATM physical interface chips.

The ML6672 transmit section accepts ECL 100K compatible NRZ inputs.

Several additional functions are provided by the ML6672 to simplify applications. A common-mode reference is provided to set the input DC level for the equalizer and the near-end transformer winding. This terminal may be used as an AC ground for the transformer center-tap or termination resistors. A link status circuit monitors line integrity and provides a proper logic level output signal to interface with the host system.

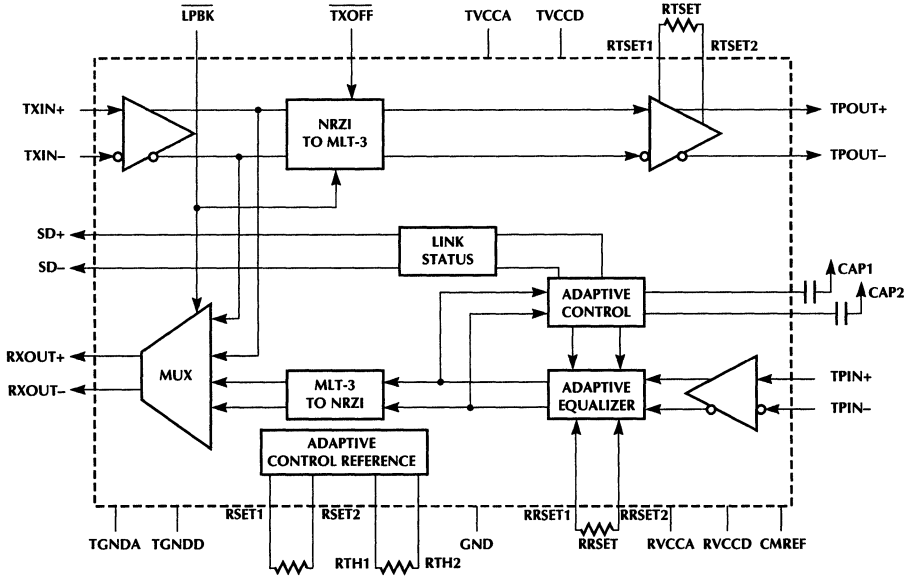
The ML6672 is implemented in a BiCMOS process. A differential signal path throughout minimizes the effects of power supply transients and noise.

FEATURES

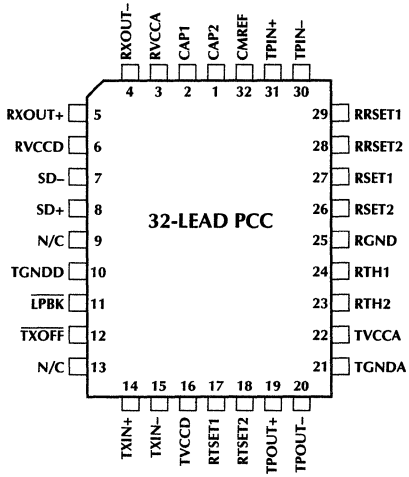
- Complies with ATM Forum 155Mbps Twisted Pair Specification
- Transmitter can be externally turned off for true quiet line
- Receiver includes adaptive equalizer
- Operates over 100 meters of STP or category 5 UTP Twisted Pair Cable
- 32-pin surface mount package
- Semi-standard options available

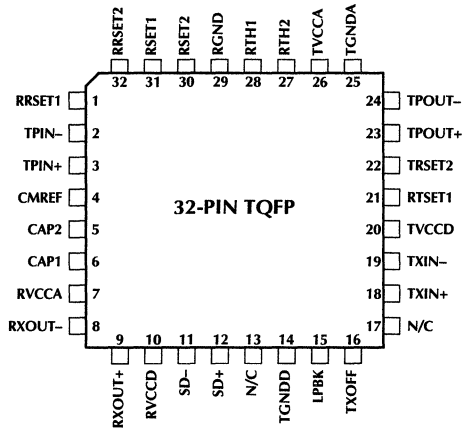
4

BLOCK DIAGRAM



PIN CONFIGURATION





PIN DESCRIPTION

NAME	FUNCTION
TX_{IN}+, TX_{IN}–	These differential ECL100K compatible inputs receive NRZ data from the PHY for transmission.
TPOUT+, TPOUT–	Outputs from the NRZ buffer drive these differential current outputs. The transmitter filter/transformer module connects the media to these pins.
$\overline{\text{LPBK}}$	This TTL input enables transmitter-Receiver loopback internally when asserted low.
$\overline{\text{TXOFF}}$	This TTL input forces the NRZ buffer to a quiet state when asserted low.
RTSET1, RTSET2	An external 1% resistor connected between these pins controls the transmitter output current amplitude. I_{OUT} = 64 x 1.25V/RTSET
TVCCA, TVCCD	Separate analog and digital transmitter power supply pins help to isolate sensitive circuitry from noise generating digital functions. Both supplies are nominally +5 volts.
TGNDA, TGNDD	Analog and digital transmitter grounds provide separate return paths for clean and noisy signals.
SD+, SD–	These differential ECL100K compatible outputs indicate the presence of a data signal with an amplitude exceeding a preset threshold.
TPIN+, TPIN–	NRZ encoded data from the receiver filter/ transformer module enters the Receiver through these pins.

NAME	FUNCTION
RXOUT+, RXOUT–	Differential ECL100K compatible outputs provide NRZ encoded data to the PHY.
CAP1, CAP2	Two external capacitors connected to these pins sets the time constant for the adaptation in the equalizer loop as well as for signal detect response.
RRSET1, RRSET2	Internal time constants controlling the equalizer's transfer function are set by an external resistor connected across these pins.
CMREF	This pin provides a DC common mode reference point for the receiver inputs.
RVCCA, RVCCD	Analog and digital supply pins are separated to isolate clean and noisy circuit functions. Both supplies are nominally +5 volts.
RGND	Receiver ground.
RSET1, RSET2	An external 5KΩ resistor across these pins sets up an internal reference current.
RTH1, RTH2	An external resistor connected across these pins sets the internal levels for equalization as well as signal detect. This resistor allows compensation for transmit and magnetics variations. RTH should be set to match the peak-to-peak transmit amplitude. V_{AMP} = 16 x 1.25 x RTH/RSET where V_{AMP} is the peak-to-peak amplitude of the transmit output with zero length cable.

ABSOLUTE MAXIMUM RATINGS

VCC Supply Voltage Range ..... –0.3V to 6V
Input Voltage Range
  Digital Inputs ..... –0.3V to VCC
Output Current
  TPOUT+/TPOUT–, SD±, RXOUT± 50mA
  All other outputs 10mA
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

VCC Supply Voltage ..... 5V ± 5%
T_A, Ambient Temperature ..... 0°C to +70°C
RTSET ..... 4KΩ + 1%
RRSET ..... 8KΩ + 1%
RSET ..... 5KΩ + 1%
RTH ..... 250Ω + 1%
CAP1, CAP2 ..... 1.0µF + 5%

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, VCC = 5V ±5%, RTSET = 4.0KΩ, RTH = 250Ω.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics					
Supply Current					
RVCCD			67		mA
RVCCA			52		mA
TVCCD			25		mA
TVCCA			6		mA
RVCCD + RVCCA + TVCCD + TVCCA				170	mA
TTL Inputs ($\overline{TXOFF}$, $\overline{LPBK}$)					
V_{IL} Input Low Voltage				0.8	V
V_{IH} Input High Voltage		2.0			V
Differential Inputs (TPIN±, TXIN±)					
TPIN+, TPIN– Common Mode Input Voltage		2.2		V_{CC}	V
TPIN+, TPIN– Differential Input Voltage				1.5	V
TPIN+, TPIN– Differential Input Resistance		10.0K			Ω
TPIN+, TPIN– Common Mode Input Current				+10	uA
TXIN+, TXIN– Input Voltage HIGH (V_{IH})		V_{CC}–1.165		V_{CC}–0.88	V
TXIN+, TXIN– Input Voltage LOW (V_{IL})		V_{CC}–1.810		V_{CC}–1.475	V
TXIN+, TXIN– Input Current LOW (I_{IL})		0.5			uA
TXIN+, TXIN– Input Current HIGH (I_{IH})				50	uA
Differential Outputs (SD±, RXOUT±, TPOUT±)					
SD+, SD–, RXOUT+, RXOUT– Output Voltage HIGH (V_{OH})	Note 5	V_{CC}–1.025		V_{CC}–0.88	V
SD+, SD–, RXOUT+, RXOUT– Output Voltage LOW (V_{OL})	Note 5	V_{CC}–1.81		V_{CC}–1.62	V
TPOUT+, TPOUT– Differential Output Current HIGH	$V_{OUT} = V_{CC} \pm 0.5$, Note 4	19.0		21.0	mA
TPOUT+, TPOUT– DifferentialOutput Current LOW	$V_{OUT} = V_{CC} \pm 0.5$, Note 4	0		0.1	mA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Outputs (SD±, RXOUT±, TPOUT±) (Continued)					
TPOUT+, TPOUT– Output Current Offset	Note 3			0.5	mA
TPOUT+, TPOUT– $V_{OUT} = V_{CC}$ Output Amplitude Error	Note 3, 4	–5.0		5.0	%
TPOUT+, TPOUT– $V_{OUT} = V_{CC} \pm 1.1V$ Output Voltage Compliance		–2.0		+2.0	%
AC Characteristics					
TPOUT+, TPOUT– Rise/Fall Time	Note 2	1.5	2.0	2.5	ns
TPOUT+, TPOUT– Output Jitter	Note 2		0.5		ns
RXOUT+, RXOUT– Rise/Fall Time	Note 2			5	ns
RXOUT+, RXOUT– Output Jitter	Note 2		2.0		ns

Note 1. Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2. Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 3. Low Duty cycle pulse testing is performed at T_A.
Note 4. Output current amplitude is determined by $I_{OUT} = 64 \times 1.25V/RTSET$.
Note 5. Output voltage levels are specified when terminated by 50Ω to V_{CC}-2V or equivalent load.

FUNCTIONAL DESCRIPTION

The ML6672 transceiver is a physical media dependent transceiver that allows the transmission and reception of 155 Mbps data up to 100 meters over shielded twisted pair cable or category 5 unshielded twisted pair cable.

The transmit section accepts NRZ data, sending the information on a two pin current driven transmitter. The transmitted output passes through an external low pass filter and transformer before entering the connectors to the STP or UTP cable. The output amplitude of the transmitted signal is programmable through the external RTSET resistor.

The receive section accepts NRZ coded data after it passes through an isolation transformer and band limiting filter. The adaptive equalizer is used to compensate for the amplitude and phase distortion incurred from the cable. The adaptive control section determines the cable length and adjusts the equalizer accordingly. As the input signal amplitude diminishes, the amount of equalization increases until it reaches its maximum of an equivalent 100 meters of category 5 cable.

The adaptive control block governs both the equalization level as well as the link detection status. The link detection threshold has a fixed relationship to the overall equalization level which is currently 25% of the transmitted amplitude. For the link status to be true, a minimum level signal must be received. When the input signal is small, the equalization will be at its maximum.

After the signal has been equalized, it is fed through the loopback multiplexer onto the RXOUT± pins.

Figure 1 shows a typical gain vs frequency plot of the adaptive equalizer for 0, 25, 50, 75 and 100 meter category 5 cable lengths.

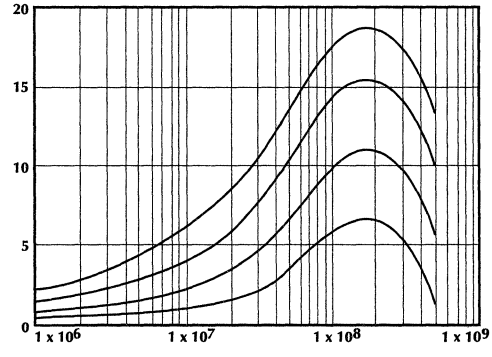


Figure 1. Equalization Range

TRANSMISSION

PECL level scrambled NRZ data is received by the ML6672 and the current driven transmitter then sent the data to the filter/transformer module. The transmit amplitude is controlled by one external resistor, RTSET.

$$I_{OUT} = \frac{64 \times 1.25V}{RTSET}$$

For ATM UTP applications the transmit amplitude is 1V peak to peak. The termination at the transmitter output is 50Ω. Therefore the transmit current I_{OUT} = 1/50 = 20 mA.

Therefore, RTSET = 64 x 1.25/40KΩ = 4KΩ

The transmitter may be disabled via the TXOFF pin. When this pin is pulled low, the transmitter's output goes to its center value ($I_{OUT}/2$) with no differential current flowing through the transformer.

ADAPTIVE EQUALIZATION

During transmission of data over UTP (unshielded twisted pair), distortion and ISI are caused by dispersion in the cable. Equalization is used to overcome this signal corruption. However, the distortion is frequency dependent and loop length dependent. Therefore, in most practical cases, the TP port characteristic is unknown and it is impractical to tune the equalizer specifically to each individual port. Hence, adaptive equalizer is used in the TP-PMD to ensue proper compensation of the received signal.

By using adaptive equalizer, the receiver automatically compensate different length of cable without over equalizing or under equalizing the line. The ML6672 monitors the energy of the received signal to determine the cable length and adjust the equalizer accordingly. The input signal level is inversely proportional to the cable length. Therefore, as the signal level decreases, the amount of equalization is increased to compensate for the line loss.

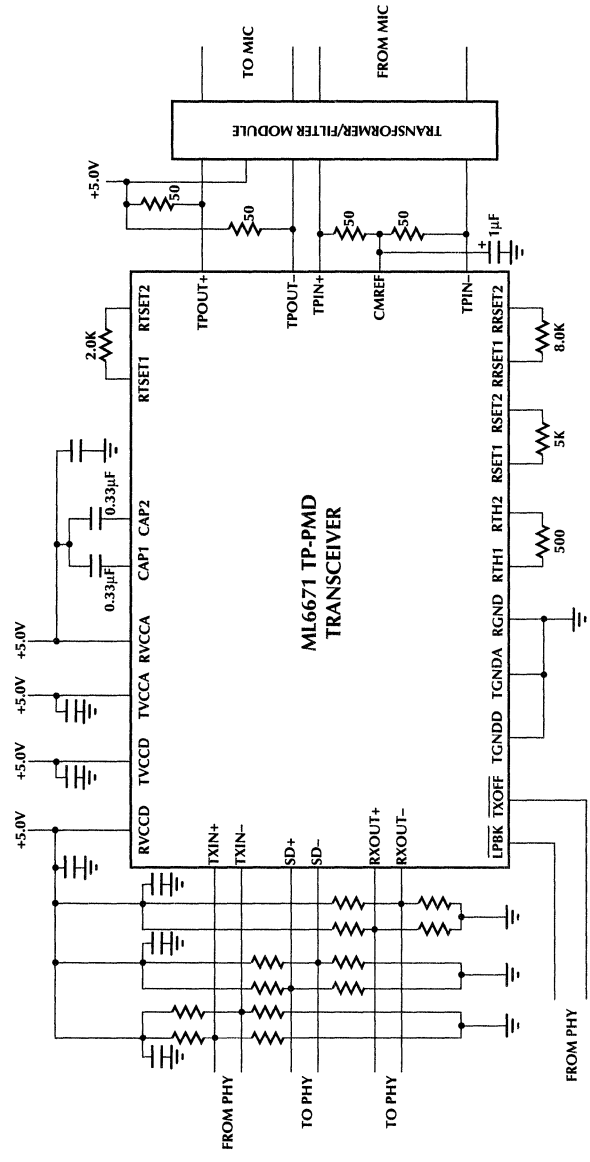
RECEIVE CIRCUIT

After the data is received and equalized, it is then sent to the clock recovery circuit via the RXOUT pins. A resistor RTH is used to control the internal level of equalization.

$$V_{AMP} = \frac{16 \times 1.25 \times RTH}{RSET}$$

VAMP is the transmit voltage amplitude and is equal to 1V and RSET = 5KΩ. Therefore, RTH = 1 x 5/(16 x 1.25) KΩ = 250Ω.

CAP1 and CAP2 are capacitors used to set the time constant for adaptation of the equalizer loop and should be 0.33µF.



Application Example of ML6672 Configured for 1.0V_{P-P} Transmit Amplitude on C5 UTP.

Note 1. Split 100K ECL terminations are 82Ω and 130Ω to VCC and GND respectively.
Note 2. Recommended power supply bypass capacitors are 0.1µF with optional 10µF tantalum in parallel
Note 3. Transformer turns ratio is 1:1.
Note 4. LPBK and TXOFF inputs are active LOW.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6672CQ	0°C to +70°C	32-Pin Molded Leaded PCC (Q32)
ML6672CH	0°C to +70°C	32-Pin TQFP (H32)

ML6672-9EVAL

155Mbps ATM Transceiver Evaluation Kit

GENERAL DESCRIPTION

The ML6672-9EVAL board is a 155Mbps ATM transceiver for transmission over UTP (Unshielded Twisted Pair) Category 5 cable. At one end, the ML6672-9EVAL board interfaces to an RJ45 connector, through a transformer and common mode choke module (T1 and T2). The other end of the evaluation board interfaces to a 9-pin ODL (1408U) footprint socket. This permits the conversion of an existing fiber-based ATM design to a copper-based design.

FEATURES

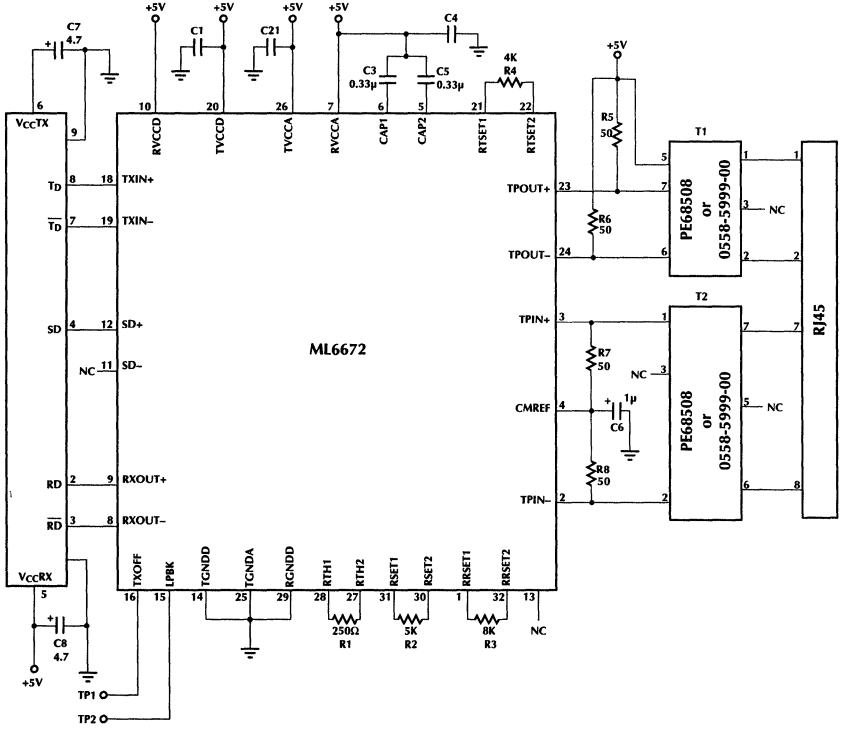
- Loop back capability
- Quiet line by turning transmitter off
- Low jitter
- Fast rise and fall times at the transmitter

KIT COMPONENTS

- ML6672-9EVAL user guide
- Application Note 30
- ML6672 data sheet
- Assembled evaluation board
- 3.5" disk with Gerber Files

The user guide includes performance data, layout recommendation, layout, schematic, parts list and tutorial on how to use the demo board.

BLOCK DIAGRAM



ML6673

TP-PMD Transceiver

GENERAL DESCRIPTION

The ML6673 is a complete monolithic transceiver for 125 Mbaud MLT-3 encoded data transmission over Category 5 Unshielded Twisted Pair and Shielded Twisted Pair cables. The ML6673 integrates the baseline restoration function defined in the TP-PMD standard. The adaptive equalizer in the ML6673 will accurately compensate for line losses of up to 100m of UTP. The part requires only external 1% resistors for accurate equalization.

The ML6673 receive section consists of an equalizing filter with a feedback loop for controlling effective line compensation. The feedback loop contains a filter and detection block for determining the proper control signal. The ML6673 also contains data comparators with precisely controlled slicing thresholds and an MLT-3 to NRZI translator. An ECL 100K compatible buffer at the output interfaces directly with existing FDDI PHY silicon from various manufacturers.

The ML6673 transmit section accepts ECL 100K compatible NRZ inputs and converts them to differential current mode MLT-3 signals. Transmit amplitude is controlled by a single external resistor.

Several additional functions are provided by the ML6673 to simplify applications. A common-mode reference is provided to set the input DC level for the equalizer and the near-end transformer winding. This terminal may be used as an AC ground for the transformer center-tap or termination resistors. The transmitter can be disabled to provide true quiet line.

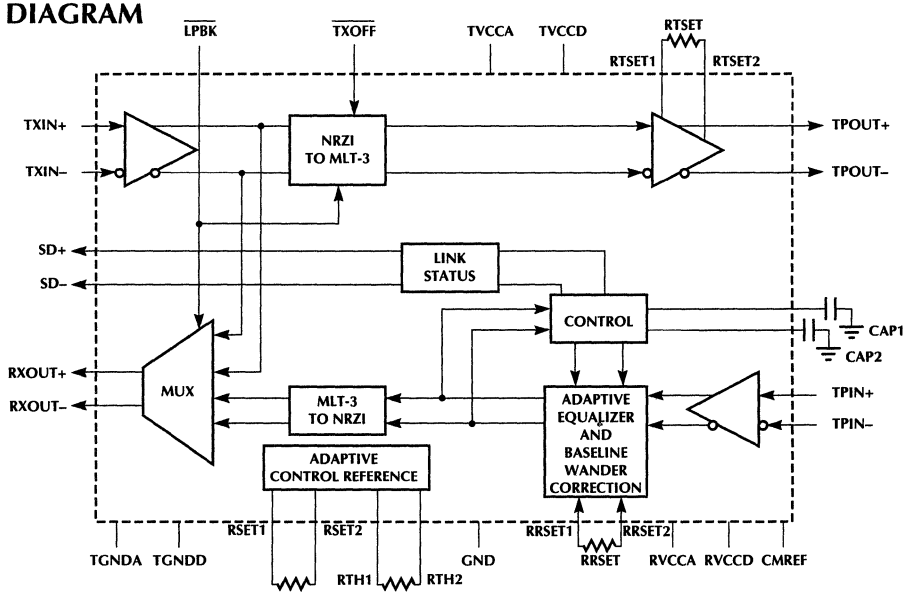
The ML6673 is implemented in a BiCMOS process. A differential signal path throughout minimizes the effects of power supply transients and noise.

FEATURES

- Compliant with ANSI X3T12 FDDI over copper (TP-PMD) standard
- Compliant with IEEE 802.3 Fast Ethernet (100BASE-TX) standard
- Integrated baseline wander correction circuit
- Transmitter converts NRZI ECL signals to MLT-3 current driven outputs
- Transmitter can be externally turned off for true quiet line
- Receiver includes adaptive equalizer and MLT-3 to NRZI decoder
- Operates over 100 meters of STP or category 5 UTP Twisted Pair Cable
- 32-pin PLCC and TQFP

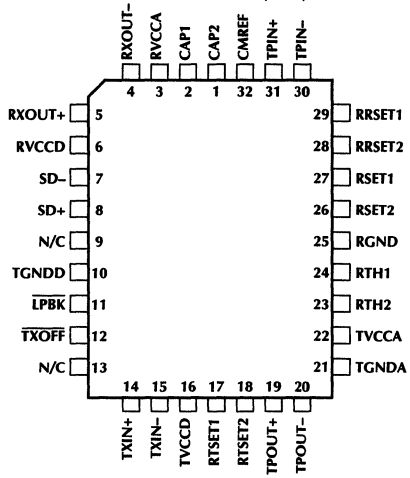
4

BLOCK DIAGRAM

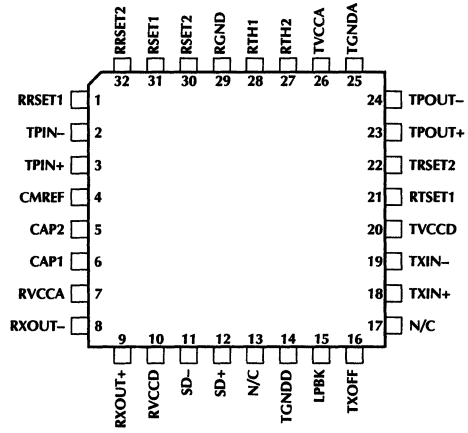


PIN CONFIGURATION

ML6673
32-Pin PLCC (P38)



ML6673
32-Pin TQFP (H38)



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6673CQ	0°C to 70°C	32-Pin Molded PCC
ML6673CH	0°C to 70°C	32-Pin TQFP

ML6682

Token Ring Physical Interface

GENERAL DESCRIPTION

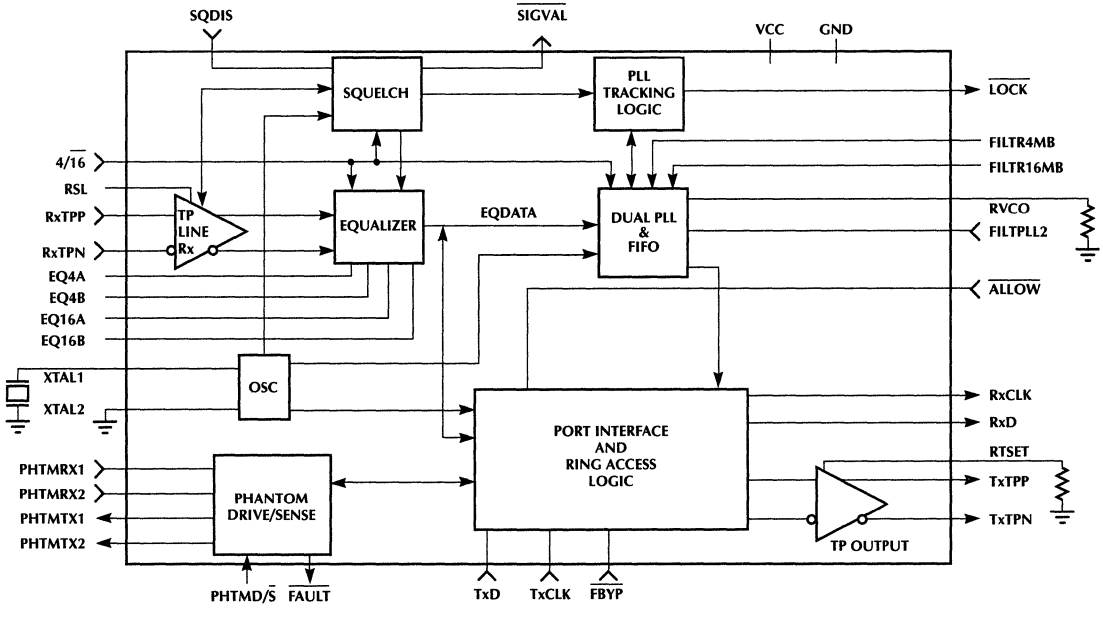
The ML6682 Token Ring Physical Interface Circuit is designed for use as a token ring concentrator port interface in 4Mb/s and 16Mb/s IEEE 802.5 networks using category 4 and 5 unshielded twisted pair (UTP) and type 1 shielded twisted pair (STP) cable. It can also be configured as a Ring-In or Ring-Out port for concentrator interface to the main network trunk. It includes a receiver equalizer for suppression of inter-symbol distortion, a narrow-bandwidth master PLL with a constant-gain phase/frequency detector for enhanced clock tracking and low VCO phase distortion, an 8 UI FIFO and slave PLL for additional jitter attenuation, internal frequency/phase tracking select logic, and a waveshaping twisted pair transmit driver which requires only a very simple external filter to meet the 802.5 standard. The circuit also includes phantom wire fault detection and output drivers for use with an external phantom switching mechanism in a concentrator-to-trunk interface application. The part has an on-chip single-pin crystal oscillator designed for a 16MHz crystal. It can also be used with an external clock of either 16MHz or 32MHz frequency. The part uses a frequency squelch circuit at the twisted pair receiver to allow detection of incorrect network speed.

FEATURES

- Supports the complete interface for a concentrator.
- Supports dual PLL jitter attenuator and clock regeneration for each lobe port and Ring In/Ring Out ports for UTP/STP extended distance concentrators.
- Compatible with IEEE 802.5-1989 Standard for Token Ring
- Pin selectable 16 and 4Mb/s data rates
- Supports dual ring fault tolerant Ring In/ Ring Out trunks
- Fault isolation capability at each concentrator port available for network management.
- Provides Dual Phase-Locked Loop with single edge constant gain phase detector and 8 UI FIFO for clock regeneration, jitter attenuation and data recovery.
- Phantom voltage drive/sense for both transmit and receive cable pairs.
- On-chip crystal oscillator can also be driven by external clock.
- On-chip receiver channel equalization switchable for both 4 and 16 Mbps
- Advanced BiCMOS technology

4

BLOCK DIAGRAM

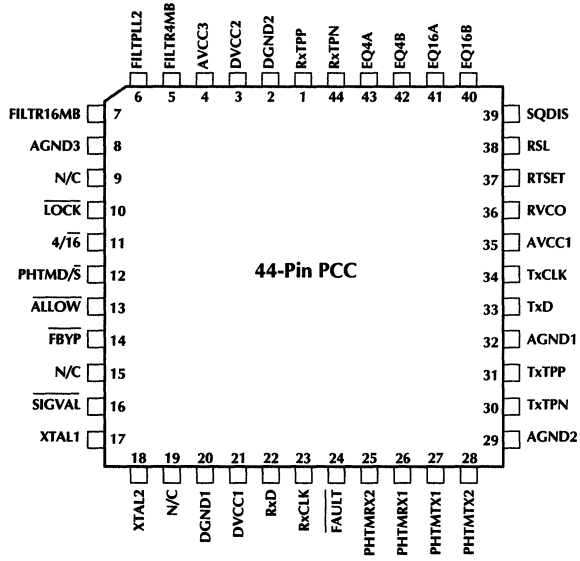


GENERAL DESCRIPTION (Continued)

External components are minimized by the use of internally-controlled station fault, receiver pulse width squelch, on-chip crystal oscillator, and internal 4/16 Mbps switching logic. The ML6682 performs the hybrid switching functions, eliminating the need for relays. Isolation can be achieved optically. The circuit requires a single +5V power supply, and is fabricated in BiCMOS technology.

PIN CONFIGURATION

ML6682
44-Pin PCC (Q44)



PIN DESCRIPTION

PIN #	NAME	FUNCTION
1 44	RxTPP RxTPN	Receive wire pair inputs. These inputs receive data from the twisted pair media through the receive isolation transformer. These pins are DC biased internally for proper receive data biasing.
2 20	DGND2 DGND1	Digital ground pins.
3 21	DVCC2 DVCC1	Positive power supply pins (+5V) for digital part of the chip.
4 35	AVCC3 AVCC1	Positive power supply pins (+5V) for analog part of the chip.
5	FILTR4MB	4Mbps PLL filter input. Connection point for external PLL filter components for 4 Mbps data rate.
6	FILTPLL2	Second PLL filter input. Connection point for external PLL filter components for second (slave) PLL.
7	FILTR16MB	16 Mbps PLL filter input. Connection point for external PLL filter components for 16 Mbps data rate.
8 29 32	AGND3 AGND2 AGND1	Analog ground pins.
9	N/C	
10	$\overline{\text{LOCK}}$	PLL phase lock indicator output. This output goes low when both PLLs achieve lock. May be externally gated with $\overline{\text{FBYP}}$ for zero delay lockout. (Prevent a 4 Mbps station from entering a 16 Mbps Ring).
11	4/$\overline{16}$	Data rate selection input. A logic one selects 4 Mbps operation. A logic zero selects 16 Mbps operation. The pin automatically switches the receive equalizer and the PLL loop filter for the appropriate data rate.
12	PHTMD/$\overline{S}$	"Phantom drive/sense" select input. When set low, the chip is configured for "phantom sense". In the "phantom sense" state PHTMRX1 pin serves as an input coming from an opto-isolator to sense phantom current and PHTMTX1 is an output. When PHTMD/$\overline{S}$ is set high, the chip is configured for "phantom drive". In the "phantom drive" state PHTMTX1 and PHTMTX2 provide the phantom drive and fault detect for the transmit pair of wires, and PHTMRX1 and PHTMRX2 sense fault detect for the receive pair of wires.
13	$\overline{\text{ALLOW}}$	$\overline{\text{ALLOW}}$ is a digital input that allows the port to control INSERT/BYPASS through phantom current, or allows the port to be forced into INSERT mode using $\overline{\text{FBYP}}$.
14	$\overline{\text{FBYP}}$	Force Bypass input. This digital input provides network management control to force the ML6682 into BYPASS mode.
15	N/C	
16	$\overline{\text{SIGVAL}}$	Valid signal indicator output. This output goes low when the signal at RxTPP/N meets frequency and amplitude squelch requirements.
17	XTAL1	Crystal/external clock input. Connecting a 16MHz crystal between this pin and ground provides the required reference frequency. This pin may also be driven by an external 16MHz clock. XTAL2 must be connected to ground when XTAL1 is used.
18	XTAL2	Clock input pin. Connecting a 32MHz external clock between this pin and ground provides the required reference frequency. When XTAL2 is used, XTAL1 must be grounded.
19	N/C	
22	RxD	Receive data output. When the ML6682 is in INSERT mode, RxD is sourced by the PLL reclocked data from receive twisted pair inputs RxTPP, RxTPN. When the ML6682 is in the BYPASS mode, RxD is sourced by the TxD input.
23	RxCLK	Synchronized data clock output. When the ML6682 is in INSERT mode, RxCLK is sourced by the PLL. When the ML6682 is in BYPASS mode, RxCLK is sourced by the TxCLK input.
24	$\overline{\text{FAULT}}$	Phantom wire fault detection output. When this output is low, the phantom current test has failed. In the "phantom drive" mode this will be detected as an open or a short by the PHTMTX1, PHTMTX2, PHTMRX1, PHTMRX2 pins. In the "phantom sense" mode, $\overline{\text{FAULT}}$ is an output that simply buffers the PHTMRX1 input.
25 26	PHTMRX2 PHTMRX1	Receive pair phantom sense inputs. In the "phantom drive" mode (PHTMD/$\overline{S}$ pin is tied to V_{CC}) these inputs sense phantom current on the receive pair wires to detect a phantom circuit fault condition. In "phantom sense" configuration (PHTMD/$\overline{S}$ pin is tied to GND) PHTMRX1 is the sense input for phantom current coming from an opto isolator and PHTMRX2 should be grounded.

PIN DESCRIPTION (Continued)

PIN #	NAME	FUNCTION
27 28	PHTMTX1 PHTMTX2	Transmit pair phantom drive/sense pair. In the "phantom drive" mode, these pins output a +5 volt phantom signal and sense opens and shorts as a phantom circuit fault condition. In the "phantom sense" mode, PHTMTX1 is an open collector pin that can be used to drive an LED to reflect the INSERT/BYPASS state. In the INSERT state, PHTMTX1 is low to light the LED and in the BYPASS state PHTMTX1 is high. PHTMTX2 should be left floating in the "phantom sense" mode.
30 31	TxTPN TxTPP	Transmitter wire pair outputs. These pins are the differential current driver outputs to the lobe fed through an isolation transformer out on to the ring.
33	TxD	Data input from the previous lobe or Ring In/Ring Out port. In INSERT mode TxD is clocked by TxCLK out onto the transmit twisted pair cable TxTPP, TxTPN. In BYPASS mode the TxD input is internally connected to the RxD output.
34	TxCLK	Synchronized data clock input from the previous lobe or Ring In/Ring Out port. In INSERT mode TxCLK clocks TxD out onto the transmit twisted pair at TxTPP, TxTPN. In BYPASS mode the TxCLK input is internally connected to the RxCLK output.
36	RVCO	External resistor input. A precision resistor of the appropriate value connected to this input sets the phase detector gain.
37	RTSET	External resistor input. A precision resistor of the appropriate value connected to this input sets the twisted pair transmitter output level.
38	RSL	Receive squelch low select input. When this pin is tied to V_{CC} the receive squelch level will be lower; more sensitive. When this pin is tied to GND, the receive squelch level will be higher; less sensitive.
39	SQDIS	Squelch disable input. Normally wired to ground. A high level input disables the RX wire pair squelch function.
40 41	EQ16B EQ16A	Differential connection for external equalization components for 16 Mbps operation. The equalizer is disabled when these two pins are tied together.
42 43	EQ4B EQ4A	Differential connection for external equalization components for 4 Mbps operation. The equalizer is disabled when these two pins are tied together.

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage Range ..... –0.3V to 6V
Input Voltage Range
  Digital Inputs ..... –0.3 to V_{CC}
  TxD, TxCLK, RxTPP,
  RxTPN, XTAL1, XTAL2 ..... –0.3V to V_{CC}
Output Current
  TxTPP, TxTPN 50mA
  PHTMRX1, PHTMRX2, PHTMTX1, PHTMTX2 .... 25mA
  All other outputs 10mA
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

V_{CC} Supply Voltage ..... 5V ± 5%
All V_{CC} supply pins must be within 0.1V of each other.
All GND pins must be within 0.1V of each other.
T_A, Ambient Temperature ..... 0°C to +70°C
T_J, Junction Temperature ..... 0°C to +125°C
REXT1 ..... 1.66K ohms ± 1%
REXT2 ..... 2.42K ohms ± 1%

ELECTRICAL CHARACTERISTICS

Over full range of operating conditions unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TTL Inputs (4/$\overline{16}$, $\overline{NSERT}$, PHTMD/$\overline{S}$, SQDIS, $\overline{ALLOW}$, TxD, TxCLK, $\overline{FBYP}$)						
V_{IL}	Input Low Voltage	I_{IL} = 400µA	–0.3		0.8	V
V_{IH}	Input High Voltage	I_{IH} = 100µA	2.0		V_{CC} +0.3V	V
I_{IL}	Input Low Current	All except TxD, TxCLK; V_{IN} = 0.4V	–400			µA
		TxD, TxCLK; V_{IN} = 0.4V	–1600			µA
I_{IH}	Input High Current	V_{IN} = 2.7V			100	µA
TTL Outputs ($\overline{FAULT}$, $\overline{LOCK}$, RxCLK, RxD, RxCLK, RxD):						
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.40	V
V_{OH}	Output High Voltage	I_{OH} = –0.1mA	2.4			V
Receiver						
V_{OSR}	RxTPP–RxTPN Differential Offset Voltage	$V_{SQDIS} = V_{IH}$	–35		35	mV
V_{DSO}	RxTPP–RxTPN Differential Squelch Threshold	RSL = V_{IL}	335		565	mVp-p
		RSL = V_{IH}	35		70	mVp-p
V_{PSO}	RxTPP–RxTPN Post-Squelch Differential Input Threshold	RSL = V_{IL}	167		282	mVp-p
		RSL = V_{IH}	23		47	mVp-p
V_{IBR}	RxTPP–RxTPN Open-Circuit Common-Mode Bias Voltage		2.2		2.8	V
R_{IDR}	RxTPP–RxTPN Differential Input Resistance	Input differential voltage = 2V, centered at V_{IBR}	3.0		6.7	KΩ
V_{STX}	XTAL1 Input Switching Threshold Voltage		2.2		3.4	V
I_{RXT1}	RExT1 Input Current	RExT1 = 1.66KΩ	575		625	µA
I_{RXT2}	RExT2 Input Current	RExT2 = 2.42KΩ	387		438	µA
Transmitter						
I_{TOUT}	TxTPP Differential Output Current	R_L = 100 or 150Ω	28		33	mA
I_{TOFF}	TxTPP–TxTPN Off-state Output Current	$V_{\overline{FBYP}} = V_{IL}$; R_L = 200Ω			1.5	mA
I_{TXI}	TxTPP–TxTPN Differential Current Imbalance	R_L = 200Ω	–900		+900	µA

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Phantom Output Driver (PHTMD/$\overline{S}$ = V_{IH}, except as noted)						
V_{OHP}	PHTMTX1/PHTMTX2 Output High Voltage	I_{OHP} = –1mA	4.1			V
		I_{OHP} = –2mA	3.8			V
I_{OHP}	PHTMTX1/PHTMTX2 Output Short Circuit Current	V_{OHP} = 0V	–20		–4	mA
I_{OZP}	PHTMTX1/Tx2/Rx1/Rx2 Output Off Current	PHTMD/$\overline{S}$ = V_{IL} 0V ≤ V_{OHP} ≤ V_{CC}	–100		+100	µA
Phantom Output Fault Sensing (PHTMD/$\overline{S}$ = V_{IH})						
V_{OPN}	$\overline{FAULT}$ Output Voltage, Normal Condition	Notes 2, 3	2.4			V
V_{OPF}	$\overline{FAULT}$ Output Voltage, Fault Condition	Notes 2, 4			0.45	V
Power Supply Current						
I_{CC1}	Supply Current, Transmitting	Note 1			205	mA
I_{CC2}	Supply Current, Idle	Current into all V_{CC} pins, V_{CC} = 5.25V			165	mA

AC CHARACTERISTICS (Over full range of operating conditions unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Transmitter (Note 8)						
t_{DF01}	TxTPP–TxTPN Output Delay Mismatch, Zeros and Ones	16Mb/s, Note 5A	0.3		1.0	ns
		4Mb/s	–0.5		0.5	ns
t_{DFMX}	TxTPP–TxTPN Output Delay Mismatch, Random Data	4Mb/s & 16Mb/s, Note 5B	–2.0		2.0	ns
t_{DCD}	TxTPP–TxTPN Output Duty Cycle Distortion	16Mb/s, Note 6	–1.5		1.5	ns
		4Mb/s, Note 6	–6.0		6.0	ns
Receiver, General						
t_{RPWL}	Maximum RxTPP-RxTPN Period To Turn On	16Mb/s, RxTP V_{DIFP-P} = 1V	166		244	ns
		4Mb/s, RxTP V_{DIFP-P} = 1V	667		2000	ns
t_{RPWS}	Minimum RxTPP-RxTPN Period To Turn On	16Mb/s, RxTP V_{DIFP-P} = 1V	40		59	ns
		4Mb/s, RxTP V_{DIFP-P} = 1V	166		244	ns
t_{PL}	PLL Phase-Lock After Freq. Lock	Figure 1			1.5	ms
t_{FL}	PLL Frequency-Lock After Power-Up	Power-up to 2BR ± 1% Hz frequency at RxCLK; Note 7			500	ms
t_{DL}	PLL Phase Unlock Time	Figure 1			100	µs
t_{PVC1}	RxCLK Period, $V_{FILTR4MB}$ = 2.2V	$V_{4/\overline{16}} = V_{OH}$ (4Mb/s), Note 9	225		150	ns
t_{PVC2}	RxCLK Period, $V_{FILTR4MB}$ = 2.8V	$V_{4/\overline{16}} = V_{OH}$ (4Mb/s), Note 9	75		112	ns
t_{PVC3}	RxCLK Period, V_{FILTSL} = 2.2V	$V_{4/\overline{16}} = V_{OL}$ (16Mb/s), Note 9	56.3		37.5	ns
t_{PVC4}	RxCLK Period, V_{FILTSL} = 2.8V	$V_{4/\overline{16}} = V_{OL}$ (16Mb/s), Note 9	18.8		28	ns
K_d	Phase Detector Gain	4Mb/s; Note 10 and Figure 2	0.25		0.35	µA/ns
		16Mb/s; Note 10 and Figure 2	1.0		1.4	µA/ns
t_{RSTE}	PLL Static Phase Error	Note 11	–2		+2	ns
t_{RDC}	RxD to RxCLK Delay		–2		2	ns
t_{RTD}	RxTP to RxD Delay		1		4	BT
t_{RCFS}	RxCLK 90-10% Fall Time	RxCLK t_{PER} = 31.25ns			5	ns
t_{PTRD}	TxD to RxD Propagation Delay	$V_{\overline{FBYP}} = V_{OL}$, Figure 4	TBD		TBD	ns
t_{PTRC}	TxCK to RxCK Propagation Delay	$V_{\overline{FBYP}} = V_{OL}$, Figure 4	TBD		TBD	ns
t_{SRM}	Setup Time, RxD Valid to RxCLK Rising Edge (1.5V point)	RxCLK t_{PER} = 31.25ns, Figure 4	10			ns
t_{HRM}	Hold Time, RxD Valid After RxCLK Rising Edge (1.5V)	RxCLK t_{PER} = 31.25ns, Figure 4	2			ns
t_{RCRM}	RxCLK 10-90% Rise Time	RxCLK t_{PER} = 31.25ns, C_L = 15pF; Figure 4			5	ns
t_{RCFM}	RxCLK 90-10% Fall Time	RxCLK t_{PER} = 31.25ns, C_L = 15pF; Figure 4			5	ns

Note 1: Current into all V_{CC} pins, V_{CC} = 5.25V, transmitting and receiving 16MHz data.

Note 2: Use a 2K ohm load at $\overline{FAULT}$ for these tests.

Note 3: 2.9K < RL1 < 5.5K, 2.9K < RL2 < 5.5K. RL1 connected between PHTMTX1 and PHTMRX1; RL2 connected between PHTMTX2 and PHTMRX2.

Note 4: Tested under the following conditions:

A. RL1 > 9.9K and 2.9K < RL2 < 5.5K, or RL2 > 9.9K and 2.9K < RL1 < 5 5K.

B. RL1 < 100Ω and 2.9K < RL2 < 5.5K, or RL2 < 100Ω and 2.9K < RL1 < 5.5K.

Note 5: A. Difference between the delay from the nearest TxCLK rising edge to the TxTPPN differential BR edge and the delay from the nearest TxCLK rising edge to the TxTPPN differential BR/2 edge. Measured for either rising output edges or falling output edges only, with measurements made for each. Measurements are to be made at the output of both test circuits shown in Figure 3. (See waveforms in Figure 7 –4 of draft IEEE 802.5q/D4).

B. Difference between the delay from the nearest TxCLK rising edge to the TxTPPN differential edge and the delay from the nearest TxCLK rising edge to the TxTPPN differential edge. Measured for either rising output edges or falling output edges only, with measurements made for each using random data (JKs, 0s, 1s) Measurements are to be made at the output of both test circuits shown in Figure 3. (See waveforms in Figure 7 –4 of draft IEEE 802.5q/D4)

Note 6: One-half the difference between the positive-going differential output pulsewidth and the negative-going differential output pulsewidth. Measured at the output of both test circuits in Figure 3 with a constant stream of all zeros or all ones. Measurements are to be averaged over 128 data pulses Measured with input drive to TxD/TxCLK.

Note 7: Not tested in production Guaranteed by characterization measurements.

Note 8: The transmitter TxTPP-TxTPN output waveform must also meet the waveform templates shown in section 7.2.2.2 of IEEE 802.5q

Note 9: Disconnect the filter components at the FILT4MB or FILT16MB pins and apply the indicated voltage to that pin. Measure the output period at RxCLK. Disconnect RxTPPN from all input.

Note 10: See Figure 2 for timing. With the circuit in phase-lock, inject I1 = +5µA and measure the propagation delay t_{PD1} between an RxTPP rising edge and the corresponding RxCLK falling edge. Make a second delay measurement t_{PD2} while injecting I2 = –5µA. Phase detector gain is given by $K_d = (I2\text{-}I1)/(t_{PD1}\text{-}t_{PD2})$.

Note 11: The ML6682 is phase-locked to the RxTPP waveform with RxTPN biased to 2.5V (see Figure 5). Monitor RxD to observe correct data being latched For one pulse, shorten the positive pulse at RxTPP by moving the rising edge, and check to see if the short pulse was latched Continue to shorten the pulse in this manner until incorrect data appears at RxCLK. The time between the rising edge and the unshortened positive pulse midpoint is t_{RSTE}. Repeat this procedure for the other 3 cases shown in Figure 5.

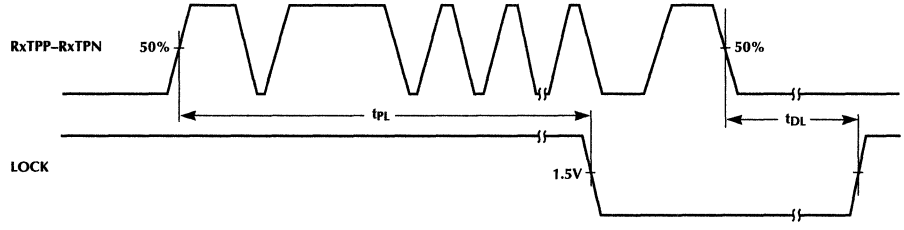


Figure 1. PLL Phase Lock Timing.

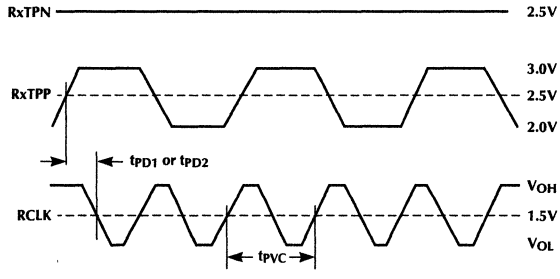


Figure 2. Phase Detector Gain Test.

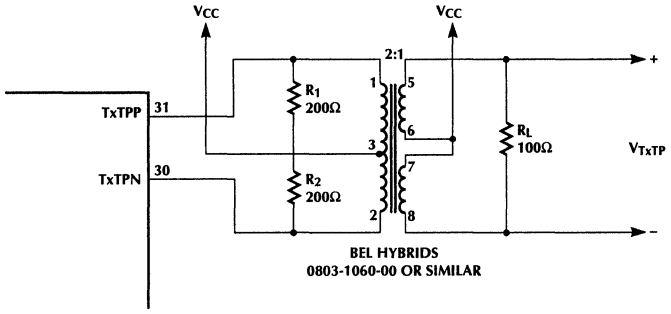


Figure 3A. Transmitter AC Test Circuit, 100 Ohms (UTP).

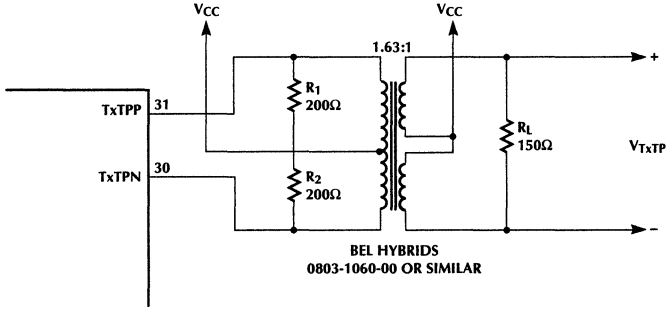


Figure 3B. Transmitter AC Test Circuit, 150 Ohms (STP).

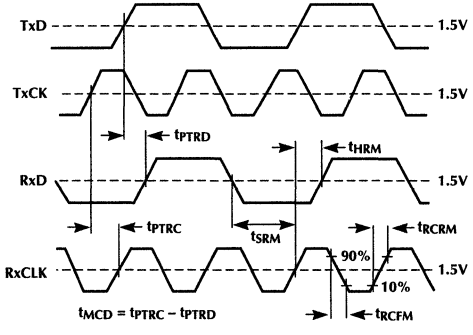


Figure 4. Receiver Timing.

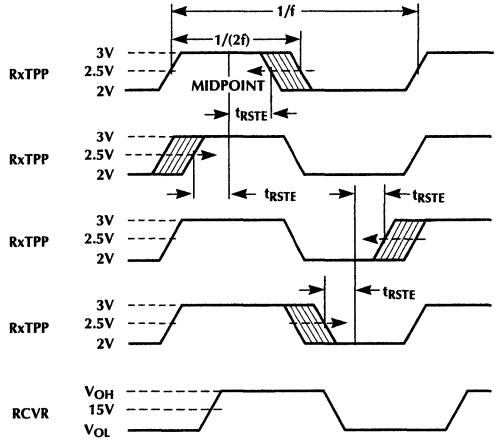


Figure 5. Receiver Static Timing Error Test.

FUNCTIONAL DESCRIPTION

Page 1 shows the functional block diagram of the ML6682. The device contains four major functional blocks; twisted pair line interface, port interface, PLL retiming circuit and crystal oscillator. In normal operation, the data is retransmitted from the previous port on to the transmit TP wire pair (to the station) by the use of TxD and TxCLK. The data from the station via the receive wire pair is retimed through the use of a dual PLL/FIFO. The retimed data at RxD is then clocked out to the next port by RxCLK.

PORT INTERFACE

The ML6682 can be used for implementing Lobe, Ring In and Ring Out ports in a concentrator. The device can be placed into either the INSERT state or the BYPASS state. Figure 6 is a functional illustration of the INSERT and BYPASS states.

When ML6682 is in the BYPASS state, the station is bypassed. The data input from the previous port is retimed and fed directly through to the next port (see figure 6). Signal from the receive twisted pair is retimed via the PLL and looped back to the transmit twisted pair. However, if the signal does not meet the receive frequency squelch criteria, the signal will not be fed to the PLL. The PLL will transmit the local clock signal onto the transmit twisted pair.

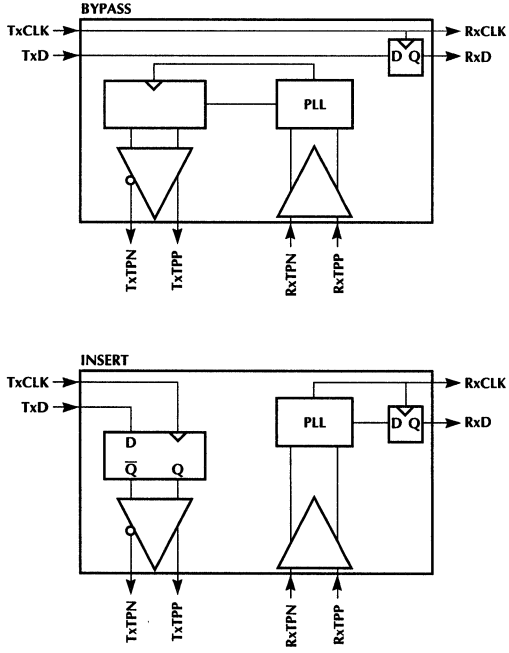


Figure 6. Bypass and Insert States.

When the port is INSERTed into the network, the transmit data TxD from the previous port is clocked by transmit clock TxCLK, and fed out on the twisted pair lines. The data from the receive twisted pair input is passed through the PLL and output on RxD and RxCLK pins.

Through various input pins, the ML6682 may be selected for one of three options:

1. Forced into the INSERT state
2. Forced into the BYPASS state
3. Allow the remote station to place the ML6682 into INSERT or BYPASS state with phantom control.

The logic equation to implement these options is as follows:

$$\overline{FBYP} \times (\overline{ALLOW} + \overline{FAULT}) = INSERT$$

When INSERT is a logic 1, the ML6682 is placed into the INSERT state as shown in Figure 6. When INSERT is a logic 0, the ML6682 is placed into the BYPASS state. Truth table 1 illustrates how the three above options can be achieved.

	$\overline{FBYP}$	$\overline{ALLOW}$	$\overline{FAULT}$	INSERT State
Forced Bypass Mode	0	X	X	0
Phantom Controlled Bypass	1	0	0	0
Phantom Controlled Insert	1	0	1	1
Forced Insert	1	1	X	1

X = Don't Care

Table 1. Logic for INSERT/BYPASS.

TP LINE INTERFACE

TP Line Receiver consists of a line equalizer, receive squelch circuit and a resistive attenuator.

RECEIVE EQUALIZER

This receive equalizer compensates for twisted-pair cable dispersion, which otherwise would give rise to inter-symbol interference (ISI). The amount of equalization varies with the average amplitude of the received signal. The received signal amplitude gives a rough value for the length of the attached cable. The filter/equalizer characteristic is the inverse of the cable's dispersion characteristic. Both UTP and STP cables approximate a low-pass filter, so the filter/equalizer approximates an inverse root equalizer. There are two sets of equalizers, one for 4 Mbps operation and one for 16 Mbps operation. This is switched automatically when the 4/$\overline{16}$ pin is toggled. Each equalizer has its own external components which consist of two resistors and a capacitor.

RECEIVE SQUELCH CIRCUIT

The TP line receiver consists of a resistive attenuator with common-mode bias set circuit and voltage offset comparators to set the amplitude squelch threshold. When the RxTP input signal meets amplitude and pulsewidth requirements, the SQUELCH circuit reduces the offset voltage of the TP Line Receive comparators, decreasing the amplitude squelch threshold. This hysteresis allows the receiver to stay on in the presence of a fading input signal.

The receive squelch circuit qualifies the incoming signal to determine whether the signal contains valid data. The circuit qualifies the signal on the basis of both the amplitude and frequency of the signal. This prevents the PLL from trying to lock onto the wrong frequency when using 4 or 16 Mbps data rates, as well as preventing the PLL from locking onto noise. Once the signal has been qualified, the circuit will then unsquelch. The RSL pin selects one of two amplitude levels for the amplitude squelch criteria, while the 4/$\overline{16}$ pin selects one of two frequency squelch criteria.

The level of the amplitude squelch circuit can be selected by using the RSL pin. The squelch threshold range is as follows:

	MIN Threshold	MAX Threshold
RSL = 1	35 mV_{P-P}	70 mV_{P-P}
RSL = 0	335 mV_{P-P}	565 mV_{P-P}

Frequency Squelch Criteria

4 Mbps max limit	4.1MHz to 6MHz
4 Mbps min limit	0.5MHz to 1.5MHz
16 Mbps max limit	17MHz to 25MHz
16 Mbps min limit	4.1MHz to 6MHz

When squelch is on, the PLL is tracking the internal clock frequency coming from an external clock or the internal oscillator. When the part unsquelches the PLL switches into phase acquisition mode, attempting to phase lock onto the incoming data.

PHASE LOCK LOOP

The PLLs are third-order, type II charge pump loops (see F.M. Gardner, "Charge-Pump Phase-Lock Loops", IEEE Trans Comm, Vol. COM-28, No. 11, pp. 1849-1858, November 1980). They have high damping factor and low loop bandwidth to minimize accumulated jitter. The loop filter is externally connected. The third pole is at a very high frequency, since the ratio of the second and third order pole capacitors C1/C3 is about 20,000:1. This, too, is done to minimize accumulated jitter.

The 16 Mbps loop filter, slave loop filter, and 4 Mbps loop filter are external to the chip. Each filter consists of two capacitors and a resistor. The switching between the 16Mbps and 4Mbps loop filters is automatic when the 4/$\overline{16}$ pin is toggled. Each data rate uses a different charge pump.

The VCO uses a MOS voltage-to-current converter at its input to give a very high input impedance and low static phase error. The high VCO input impedance also allows the elimination of a loop filter buffer and the parasitic poles a buffer would add to the loop. The oscillator itself is a bipolar ring type oscillator with temperature and voltage-compensated output frequency for low jitter.

The first PLL will achieve lock after several microseconds of a static phase error of less than ± 4 nsec. Hysteresis is built into the lock circuit so that it is more difficult to achieve lock than it is to lose lock. This will also prevent any oscillation of the $\overline{LOCK}$ pin. Lock will be lost if the phase error exceeds ±4 nsec for several micro-seconds. Once lock is lost, the PLL will try to achieve phase lock for several milli-seconds. If it is unsuccessful, the ML6682 will switch to internal frequency acquisition mode and re-center the VCO. Once it has achieved frequency lock with its internal oscillator, it will automatically switch to phase acquisition mode and try again to phase lock onto the data.

The frequency squelch circuit will limit the frequency range allowed to pass into the PLL. This limited frequency range in addition to the stringent lock criteria will insure that the PLL will not lock onto harmonics or sidebands of the fundamental data rate.

The first PLL clocks the data into an 8 UI FIFO. Each flip-flop in the FIFO stores one UI which is one half bit. The second (slave) PLL has a much narrower bandwidth set by the external filter connected to pin FILTPLL2. The second PLL is fed the first PLL's clock so that it can remove more of the jitter. The clock out of the second PLL is used to clock the data out of the FIFO and onto the RxD pin. The second PLL's clock output appears at RxCLK. This dual PLL architecture is the most effective way to reduce jitter and insure optimal performance from a token ring network.

TP LINE DRIVER

The TP OUTPUT driver uses a current mode switch which develops the output voltage by driving current through the terminating resistor and the output filter. Both TxTPP and TxTPN outputs are open collector, intended to drive a center-tapped transformer, with the center tap connected to V_{CC}. The driver is capable of driving 150Ω doubly-terminated transmission lines to a minimum 4.1V_{P-P} level or 100Ω doubly-terminated transmission lines to a minimum 2.7V_{P-P} level. The driver's output is waveshaped, allowing the use of a simple external transmit filter.

PHANTOM CURRENT DETECTION

The ML6682 provides a phantom current detection function. With PHTMD/$\overline{S}$ driven high, the phantom voltage and wire fault detection circuit provides correct phantom DC output voltage under normal conditions. It also senses short-circuit and open-circuit fault conditions, and removes phantom voltage when appropriate.

In the LOBE port application with PHTMD/$\overline{S}$ tied low ($\overline{FBYP}$ is tied high and $\overline{ALLOW}$ is tied low), driving PHTMRX1 high places the device into the INSERT mode. Driving PHTMRX1 low places the device in the BYPASS mode, in which data from the previous port will be passed on to the next port.

CLOCK OSCILLATOR

The ML6682 provides an on-chip clock oscillator by connecting a crystal to the XTAL1 pin. The ML6682 can also be driven by an external 16MHz clock at the XTAL1 pin, or by an external 32MHz clock at the XTAL2 pin. In either case, the unused XTAL pin should be grounded.

APPLICATIONS

Figure 7 shows a block diagram of an intelligent UTP Hub implementation with active retiming on each port. The architecture shown has a back up ring for fault tolerant operation. The Ring In and Ring Out ports use phantom current to detect wire faults. When a fault is detected, the Ring-In and Ring-Out port go into the bypass state and perform an automatic loopback onto the Back-up Ring. This feature is especially useful in stackable hub designs.

A micro processor can be used to manage each individual port. All the ports including the Ring In and Ring Out ports can be individually programmed into "Force INSERT", "Force BYPASS" or "Allow phantom control".

LOBE PORT

Figure 8 shows a typical implementation of a lobe port. Lobe ports are configured as phantom sense ports using opto isolators for sensing phantom current. Phantom current is sensed with an opto isolated output signal fed into pin PHTMRX1. PHTMTX1 will go low with an open collector output when the ML6682 goes into the INSERT state. PHTMTX1 may either be used to drive an LED indicator or another opto isolator to signal the remote station whether it is inserted or not.

By connecting the signal from the $\overline{LOCK}$ pin to the $\overline{FBYP}$ pin, the ML6682 is forced into bypass mode until the PLL achieves lock. When a station with a frequency different than the ring frequency attempts to insert into the ring, the PLL will not achieve lock and thus the station will not be inserted.

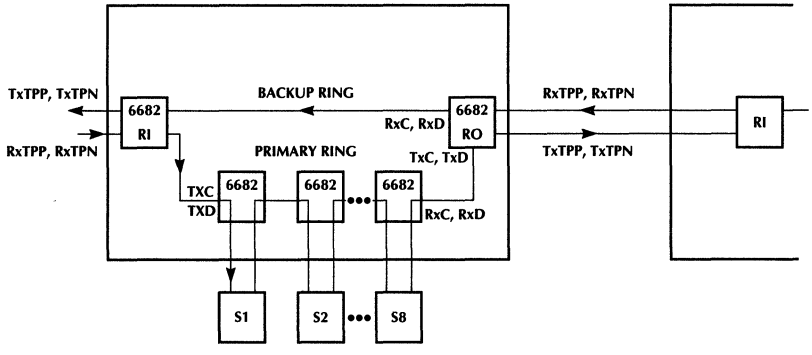


Figure 7. Intelligent UTP Hub.

RING-IN PORT

The Ring In port may also be configured for phantom sense with automatic loopback fault detection. When Phantom current is detected the part is in the INSERT state. If phantom current is lost, the ML6682 will automatically switch to the BYPASS state. Using the $\overline{FBYP}$ and $\overline{ALLOW}$ pins the part can also be forced into INSERT state, for compatibility with older standard type hubs, or forced into BYPASS for diagnostic purposes.

The configuration of a fault tolerant Ring In port is implemented exactly like a lobe port. The TxD and TxCLK pins are connected to the RxD and the RxCLK pins of the ring out port to create a "back up" ring. When the fault tolerant feature is not needed for compatibility with the older hubs, the phantom current sense capability of the ML6682 should be disabled and the device should be placed in the forced insert state by using $\overline{FBYP}$ and $\overline{ALLOW}$. The $\overline{LOCK}$ pin should still be used to ensure that the proper ring speed is maintained.

RING OUT PORT

Tie the PHTMD/$\overline{S}$ pin high to configure the ML6682 as a Ring Out port. In this mode the Ring Out port looks like a station; however, when a FAULT is detected on the transmit or receive twisted pair wires, the ML6682 will automatically go into BYPASS state. The PHTMRX1 and PHTMRX2 pins drive the receive pair transformer center taps, and the PHTMX1 and PHTMTX2 pins drive the transmit pair transformer center taps on the cable side of the transformers in this mode.

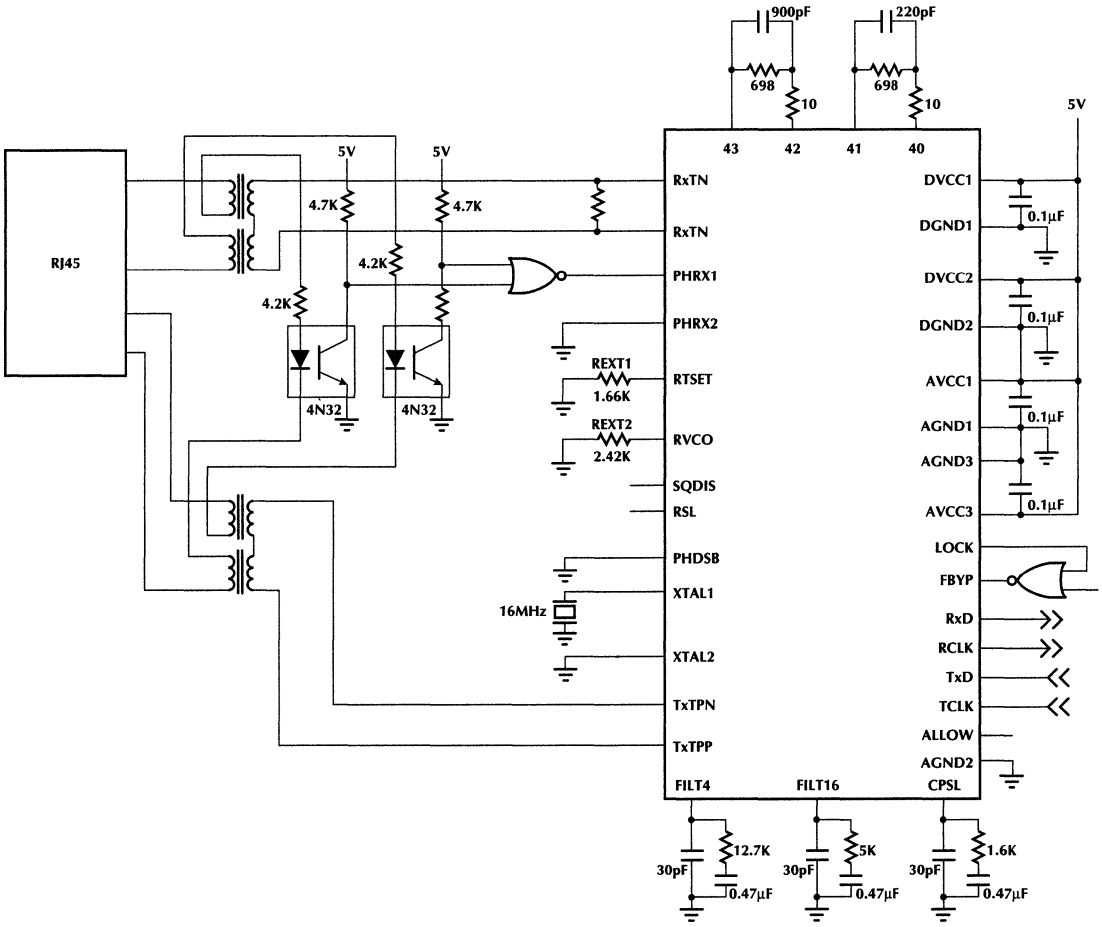


Figure 8. Typical Circuit for a Lobe Port.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6682CS	0°C to +70°C	44-Pin PLCC (Q44)

Section 5

Read/Write Signal Processing (Continued)

Servo Control ICs

Motor Control ICs

Tape Drive

Magneto Optical Drive

READ/WRITE AMPLIFIERS

Part Number	Numbers of Channels	Head Type	Max Input Noise (nV/VHz)	Write Current Range (mA)	Key Features	Package Options
ML117	2, 4 or 6	Ferrite	2.1	10 to 50	Write Current Disable Function	PDIP-18, 22, 28; SO-18, 24; PCC-28
ML117R	2, 4 or 6	Ferrite	2.1	10 to 50	Internal Damping Resistors	PDIP-18, 22, 28; SO-18, 24; PCC-28
ML501	6 or 8	Ferrite	1.5	10 to 50	Enchanced Write Stability	PDIP-28, 40; SO-32; PCC-28, 44
ML501R	6 or 8	Ferrite	1.5	10 to 50	ML501 with Internal Damping Resistors	PDIP-28, 40; SO-28, 32; PCC-28, 44
ML502	6 or 8	Thin Film	1.5	10 to 50	Enchanced Write Stability	PDIP-28, 40; SO-32; PCC-28, 44
ML502R	6, 7 or 8	Thin Film	1.5	10 to 50	ML502 with Internal Damping Resistors	PDIP-28, 40; SO-32; PCC-28, 44
ML502S	6 or 8	Thin Film	1.5	10 to 50	ML502 with Internal 750Ω Damping Resistor	PCC-28, 44
ML511	4, 6 or 8	Ferrite	1.5	10 to 40	Improved Write Stability	SO-24; PCC-28, 44
ML511R	4, 6, 7 or 8	Ferrite	1.5	10 to 40	ML511 with Internal Damping Resistor	SO-24; PCC-28, 44
ML4415	15	Ferrite	1.5	10 to 40	Improved Write Current Stability	PCC-44
ML4415R	15	Ferrite	1.5	10 to 40	ML4415 with Internal Damping Resistor	PCC-44
ML4416	14	Ferrite	1.5	10 to 40	Chip Select Input	PCC-44
ML4416S	14	Ferrite	1.5	10 to 40	ML4416 with Internal Damping Resistor	PCC-44
*ML4610R	2 or 4	Thin Film	0.85	5 to 35	Switchable Damping Res. (700Ω)	SO-16, 20
*ML4611R	4	Thin Film	0.85	5 to 35	Switchable Damping Res. (700Ω) and Write Current Adjust	SO-24
ML6320-3	4	Thin Film	0.6	3 to 30	2.7V to 3.6V Operating Supply	SSOP-20
ML6320-5	4	Thin Film	0.6	3 to 30	5V, SSI/VTC Alternate Source	SOIC-20

Note: * Possible uses in Tape Drive Applications.

READ/WRITE SIGNAL PROCESSING

Part Number	Function	Key Features	Package Options
ML4041	Read Data Processor	Fast AGC Recovery, 1ns Pulse Pairing	PDIP-24, SO-24, PCC-28
ML4042	ML4041 with Undervoltage Detector	Fast AGC Recovery, 1ns Pulse Pairing	PDIP-28, SO-28, PCC-28
ML4417 ML4427	Zone Bit Recording IC	100 MHz VCO	SO-16, PDIP-16
ML4568	Pulse Detector with Embedded Servo	5V Only; 1ns Pulse Pairing	PCC-28
*ML541	Read Data Processor	15 MBits/sec Data Rate	PDIP-24, CERDIP-24, PCC-28, SO-24
ML6005	24 Mbps HDD Filter/Equalizer	Low Power/High Performance	SSOP-20
ML6006	36 Mbps HDD Filter/Equalizer	Low Power/High Performance	SSOP-20
ML6010	36 Mbps Read Channel Combo	Low Cost/High Integration Configurable Array	QFP-52
ML6024	16Mbps Tape Filter/Equalizer	Parasitic Insensitive Gm/C Filter, Programmable f_C 2-9MHz, 10dB Boost	SSOP-20
ML6025	24Mbps HDD Filter/Equalizer	Parasitic Insensitive Gm/CFilter, Programmable f_C 3-13MHz, 10dB Boost	SSOP-20
ML6026	36Mbps Tape Filter/Equalizer	Parasitic Insensitive Gm/C Filter, Programmable f_C 4-20MHz, 10dB Boost	SSOP-20
ML6310	3V/5V HDD Read Channel Front-end Processor	Low Profile Package, High Integration, Low Power, 3V/5V Supplies	TQFP-32
ML6311	3V/5V HDD Read Channel Back-end Processor	Low Profile Package, High Integration, Low Power, 3V/5V Supplies	TQFP-32
ML8464B	Pulse Detector	DP8464B Second Source	PDIP-24, PCC-28
ML8464C	Pulse Detector	1ns Pulse Pairing	PDIP-24, PCC-28

Note: * Possible uses in Tape Drive Applications.

SERVO CONTROL ICs

Part Number	Function	Key Features	Package Options
ML4401	Servo Demodulator	ECL Output VCO	PDIP-28, PCC-28
ML4402	Servo Driver, External Power Drive	Low Offset (±5mV)	PDIP-20, PCC-20
ML4403	Servo Controller	On-Chip Interpolation Function	PDIP-20, PCC-20
ML4404	Analog Trajectory Generator	User-Defined Trajectory, 2 DACs	PDIP-28, PCC-28
ML4406	Servo Driver, Internal Power Drive	Internal Threshold Reference	PCC-20
ML4407	Servo Driver, Internal Power Drive	External Threshold Reference	PCC-20
ML4408	Low Voltage Drop Servo Driver	5V Only or 12V Operation	SOIC-24
ML4413	Servo Controller	ML4403 with Ext. Amp. Nulling	PDIP-24, PCC-28
ML4418	Low Saturation Voice Coil Servo Driver	On-Chip Precision Power Fail Detect Circuitry	SOIC-20
ML4431	Servo Demodulator	Enhanced ML4401; TTL Output	PCC-32
ML4506	Servo Driver, Internal Power Drive	5V Operation, Internal Threshold Reference	SOIC-20, SSOP-20
ML4508	Low Voltage Drop Servo Driver	5V Operation	SOIC-20
ML4532	Servo Burst Area Detector	Includes PWM DAC	SSOP-20, PCC-20
ML4533	Servo Burst Area Detector	No PWM DAC, Reference Levels Compatible to ML A/D Converters	SOIC-16
ML4536	Servo Burst Area Detector	No PWM DAC, Reference Levels Compatible to Zilog µC with ADC	SOIC-16
ML4534	SUM/DIFF Area Detector	For Hybrid Servo	PCC-20
ML4535	Hybrid Servo Demodulator	Integration/Area Detection	PCC-32

MOTOR CONTROLLER ICs

Part Number	Function	Key Features	Package Options
ML4510	Sensorless Spindle Motor Controller	Linear or PWM, PNP Drivers, 5V Operation	SOIC-28
ML4410	Sensorless Spindle Motor Controller	Linear or PWM, FET Drivers	SOIC-28, PCC-28
ML4411	Sensorless Spindle Motor Controller	Linear or PWM, FET Drivers	SOIC-28, PCC-28
ML4412	Sensorless Spindle Motor Controller	Linear or PWM, FET Drivers, 200mW	SOIC-28
ML4420	Sensorless Spindle Motor Controller	µP Controlled PWM, FET Drivers, 200mW	SOIC-28
ML4425	Sensorless Motor Controller	On Board PWM Generator and Speed Controller, FET Drivers	PDIP-28N, SOIC-28
ML4426	Sensorless Motor Controller with Reverse	On Board PWM Generator and Speed Controller, FET Drivers	PDIP-28N, SOIC-28
ML6035	Sensorless Spindle Motor Controller	µP Controlled, 1A FET Drivers, 5V Operation, Phase Advance	TQFP-32

TAPE DRIVE

Part Number	Function	Key Features	Package Options
ML6042	Tape Drive Data Channel Processor	Complete Read/Write Data Channel for QIC40/80/3010/3020 Tape Drives	SOIC-32
ML4451	Tape Drive Read/Write Preamplifier	Isolated 2R & 2W Channels, Ferrite Heads	SOIC-24
ML4452	MR Head Preamplifier for Tape Drives	2 Channel Read and 1 Channel Write with Readback	SSOP-20

MAGNETO OPTICAL DRIVE

Part Number	Function	Key Features	Package Options
ML6012	3.5" R/W MOD Read Channel Front-end Processor	Supports 128M and 230M ISO standards for R/W Magneto-Optical Drives, implements complete read channel with ML6013	TQFP-32
ML6013	3.5" R/W MOD Read Channel Back-end Processor	Supports 128M and 230M ISO standards for R/W Magneto-Optical Drives, implements complete read channel with ML6012	TQFP-32

ML117, ML117R

2, 4, or 6-Channel Read/Write Circuits

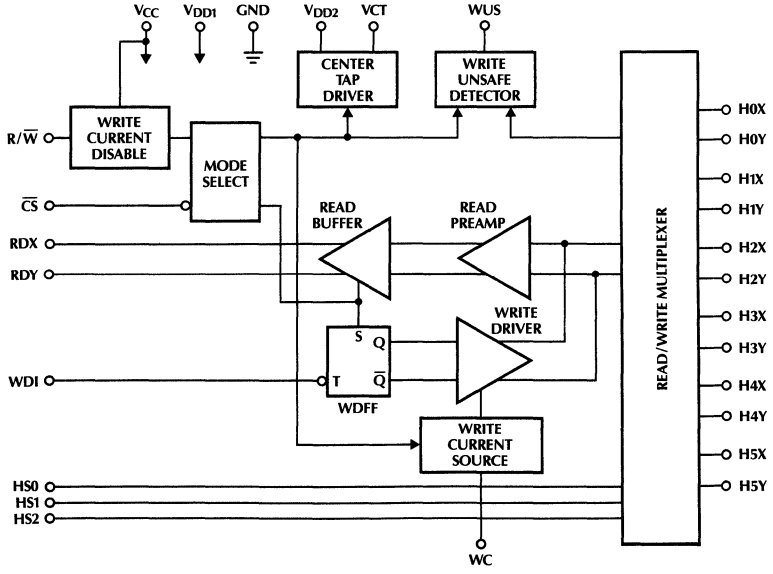
GENERAL DESCRIPTION

The ML117 devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read path, write current control, and data protection circuitry for as many as six channels. The ML117 requires +5V and +12V power supplies and is available in 2, 4, or 6-channel versions with a variety of packages. The ML117 contains exclusive circuitry that inhibits write current during device power-up, thereby eliminating power-up "glitches" common to similar read/write circuits. The ML117R differs from the ML117 by having internal damping resistors.

FEATURES

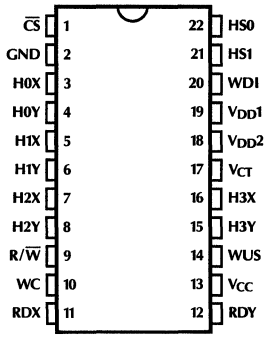
- Exclusive write current disable during power-up
- Replacement for SSI 32R117/117R
- +5V, +12V power supplies
- Single or multi-platter Winchester drives
- Designed for center-tapped ferrite heads
- Programmable write current source
- Available in 2, 4, or 6 channels
- Easily multiplexed for larger systems
- Includes write unsafe detection
- TTL compatible control signals

BLOCK DIAGRAM



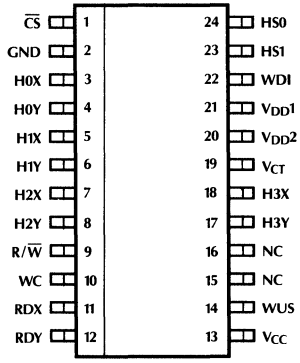
PIN CONNECTIONS

ML117-4 OR ML117R-4
4 Channels
22-PIN DIP



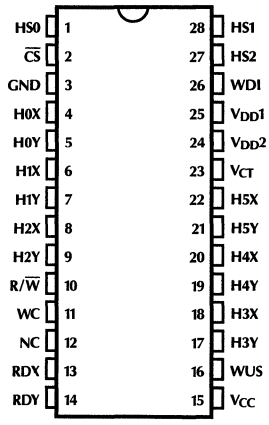
TOP VIEW

ML117-4 OR ML117R-4
4 Channels
24-PIN SOIC



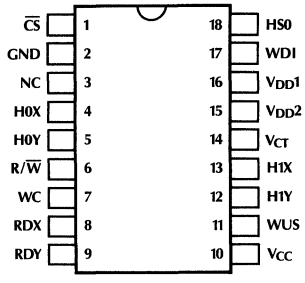
TOP VIEW

ML117-6 OR ML117R-6
6 Channels
28-PIN DIP



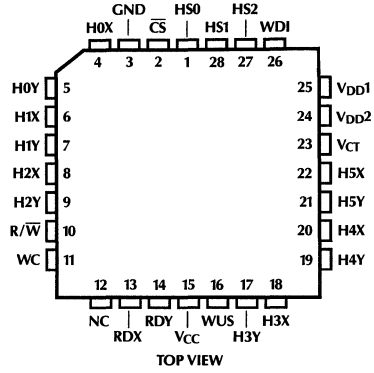
TOP VIEW

ML117-2 OR ML117R-2
2 Channels
18-PIN SOIC AND DIP



TOP VIEW

ML117-6 OR ML117R-6
6 Channels
28-PIN PCC



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
HS0–HS2	Head Select (six heads)
$\overline{CS}$	Chip Select (low level enables chip)
R/$\overline{W}$	Read/Write (high level selects Read mode)
WUS	Write Unsafe, open collecter output (high level indicates alarm)
WDI	Write Data In (negative transition toggles head current direction)
H0X–H5X	X head connections
H0Y–H5Y	Y head connections

NAME	FUNCTION
RDX, RDY	X, Y Read Data (differential read signal out)
WC	Write Current (used to set the write current magnitude)
V_{CT}	Voltage Center Tap (center tap voltage source)
V_{CC}	+5 volts
$V_{DD}1$	+12 volts
$V_{DD}2$	Positive supply for center tap
GND	Ground

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- $V_{DD}1$ ..... −0.3 to 14 V_{DC}
- $V_{DD}2$ ..... −0.3 to 14 V_{DC}
- V_{CC} ..... −0.3 to 6 V_{DC}

Input Voltage Range
- Digital Inputs ($\overline{CS}$, R/$\overline{W}$, HS, WDI) ..... −0.3 to V_{CC} +0.3 V_{DC}
- Head Ports (H0X–H5X, H0Y–H5Y) .... −0.3 to $V_{DD}1$ +0.3 V_{DC}
- Write Unsafe (WUS) ..... −0.3 to 14 V_{DC}

Write Current (I_W) ..... 60 mA

Output Current
- Read Data (RDX, RDY) ..... −10 mA
- Center Tap Current (I_{CT}) ..... −60 mA
- Write Unsafe (WUS) ..... 12 mA

Storage Temperature ..... −65°C to 150°C

Junction Temperature (T_J) ..... 125°C

Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Supply Voltage
- $V_{DD}1$ ..... 12 V ± 10%
- V_{CC} ..... 5 V ± 10%
- $V_{DD}2$ ..... 6.5 to $V_{DD}1$

Head Inductance (L_H) ..... 5 to 15 µH

Damping Resistor (R_D, ML117 only) ..... 500 to 2000 Ω

RCT Resistor (1/2 Watt) ..... 130 Ω ± 5%

Write Current (I_W) ..... 25 to 50 mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $V_{DD}1 = 12\,V \pm 10\%$, $V_{CC} = 5\,V \pm 10\%$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC OPERATING CHARACTERISTICS						
POWER SUPPLY						
I_{CC}	V_{CC} Supply Current	Read or Idle Mode			25	mA
		Write Mode			30	mA
I_{DD}	V_{DD} Supply Current	Read Mode			50	mA
		Write Mode			30+I_W	mA
		Idle Mode			25	mA
P_D	Power Dissipation	Read Mode			600	mW
		Write Mode I_W = 50 mA, R_{CT} = 130 Ω			700	mW
		Write Mode I_W = 50 mA, R_{CT} = 0 Ω			1050	mW
		Idle Mode			400	mW
DIGITAL INPUTS ($\overline{CS}$, R/$\overline{W}$, HS, WDI)						
V_{IH}	High Voltage		2		V_{CC}+0.3	V_{DC}
V_{IL}	Low Voltage		−0.3		0.8	V_{DC}
I_{IH}	High Current	V_{IH} = 2.0 V			100	µA
I_{IL}	Low Current	V_{IL} = 0.8 V	−0.4			mA
WUS OUTPUT						
V_{OL}	Output Low Voltage	I_{OL} = 8 mA (Safe)			0.5	V_{DC}
I_{OH}	Output High Current	V_{OH} = 5 V (Unsafe)			100	µA
CENTER TAP VOLTAGES						
V_{CT}	Read Mode	Read Mode		4		V_{DC}
V_{CT}	Write Mode	Write Mode		6		V_{DC}

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ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $I_W = 45mA$, $L_H = 10\mu H$, $R_D = 750\Omega$, $f_{DATA} = 5MHz$, C_L (RDX, RDY) $\leq 20pF$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE CHARACTERISTICS						
I_{WR}	Write Current Range	$I_W = K/R_{WC}$	10		50	mA
K	Write Current Constant		133		147	V
V_{HD}	Differential Head Voltage Swing		8			V_{PK}
I_{HU}	Unselected Head Transient Current				2	mA_{PK}
C_{OD}	Differential Output Capacitance				15	pF
R_{OD}	Differential Output Resistance	ML117	10k			Ω
		ML117R	562		938	Ω
f_{WDI}	WDI Transition Frequency	WUS = Low	250			kHz
A_I	I_{WS} to Head Current Gain			20		A/A
I_L	Unselected Head Leakage	Sum of X & Y Side Leakage Current			85	μA
READ MODE CHARACTERISTICS						
A_V	Differential Voltage Gain	$V_{IN} = 1mV_{P-P}$ @ 300kHz, R_L (RDX, RDY) = 1kΩ	80		120	V/V
DR	Dynamic Range	DC Input Voltage (V_i) Where Gain Falls 10%, $V_{IN} = V_i + 0.5mV_{P-P}$ @ 300kHz	−3		+3	mV
BW	Bandwidth (−3dB)	$\|Z_S\| < 5\Omega$, $V_{IN} = 1mV_{RMS}$	30			MHz
e_{IN}	Input Noise Voltage	BW = 15MHz, $L_H = 0$, $R_H = 0$			2.1	$nV/\sqrt{Hz}$
C_{IN}	Differential Input Capacitance				20	pF
R_{IN}	Differential Input Resistance	ML117	2k			Ω
		ML117R	390		810	Ω
I_{IN}	Input Bias Current				45	μA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V_{CT} + 100mV_{P-P}$ @ f = 5MHz	50			dB
PSRR	Power Supply Rejection Ratio	$100mV_{P-P}$ @ 5MHz on $V_{DD}1$, $V_{DD}2$, or V_{CC}	45			dB
CS	Channel Separation	Unselected Channels: $V_{IN} = 100mV_{P-P}$ @ 5MHz and Selected Channel: $V_{IN} = 0mV_{P-P}$	45			dB
V_{OS}	Output Offset Voltage		−480		+480	mV
V_{OCM}	Common-Mode Output Voltage	Read Mode	5		7	V
		Write or Idle Mode		4.3		V
R_{OUT}	Single-Ended Output Resistance	f = 5MHz			30	Ω
I_L	Leakage Current, RDX, RDY	RDX, RDY = 6V Write or Idle Mode	−100		+100	μA
I_O	Output Current	AC Coupled Load, RDX to RDY	2			mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $I_W = 45mA$, $L_H = 10\mu H$, $R_D = 750\Omega$, $f_{DATA} = 5MHz$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_{RW}	R/$\overline{W}$ to Write Switching Delay	To 90% of Write Current Output			1	µS
t_{WR}	R/$\overline{W}$ to Read Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	µS
t_{IW} or t_{IR}	$\overline{CS}$ to Select Switching Delay	To 90% of Write Current or to 90% of 100mV, 10MHz Read Signal Envelope			1	µS
t_{WI} or t_{RI}	$\overline{CS}$ to Select Switching Delay	To 90% Decay of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	µS
t_{HS}	Head Select Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope			1	µS
tD1	Safe to Unsafe Write Unsafe Delay	$I_W = 50mA$	1.6		8	µS
tD2	Unsafe to Safe Write Unsafe Delay	$I_W = 50mA$			1	µS
tD3	Head Current Prop. Delay	$L_H = 0$, $R_H = 0$ From 50% points			25	nS
tD3	Head Current Asymmetry	WDI has 50% Duty Cycle and 1nS Rise/Fall Time			2	nS
	Time Head Current Rise/Fall	10% and 90% Points			20	nS

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Maximum junction temperature (T_J) should not exceed 125°C.

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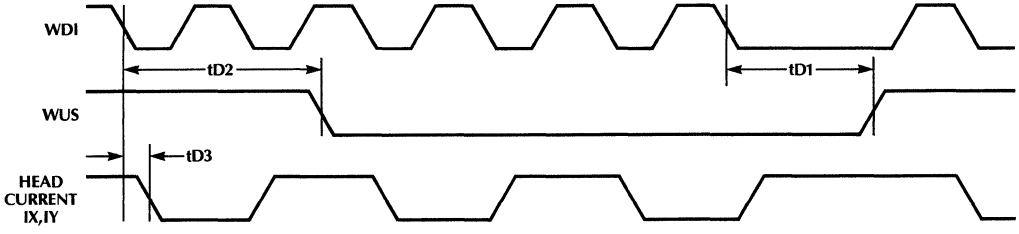
TIMING DIAGRAMS



Write Mode Timing Diagram

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

The ML117, ML117R functions as a write driver or as a read amplifier for the selected head. Head selection and mode control are described in *Tables 1 & 2*. Both R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors for the prevention of an accidential write condition.

READ MODE

In the Read Mode the ML117, ML117R is configured as a low noise differential amplifier, the write current source and the write unsafe detector are deactivated, and the write data flip-flop is set. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports.

The internal write current source is deactivated for both the Read and the Chip Deselect modes which eliminates the need for external gating of the write current source.

WRITE MODE

The Write mode configures the ML117, ML117R as a current switch and activates the Write Unsafe Detector. The head current is toggled between the X- and Y-side of the recording head on the falling edges of WDI, Write Data Input. A preceding read operation initializes the Write Data Flip-Flop, WDFF, to pass current through the X-side of the head. The magnitude of the write current, given by:

$I_W = K/R_{WC}$, where K = Write Current Constant

is set by the external resistor, R_{WC}, connected from pin WC to GND.

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- Head open
- Head center tap open
- WDI frequency too low
- Device in Read mode
- Device not selected
- No write current

Two negative transitions on WDI are required to clear WUS after the fault condition is removed.

Table 1.

Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	NONE

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

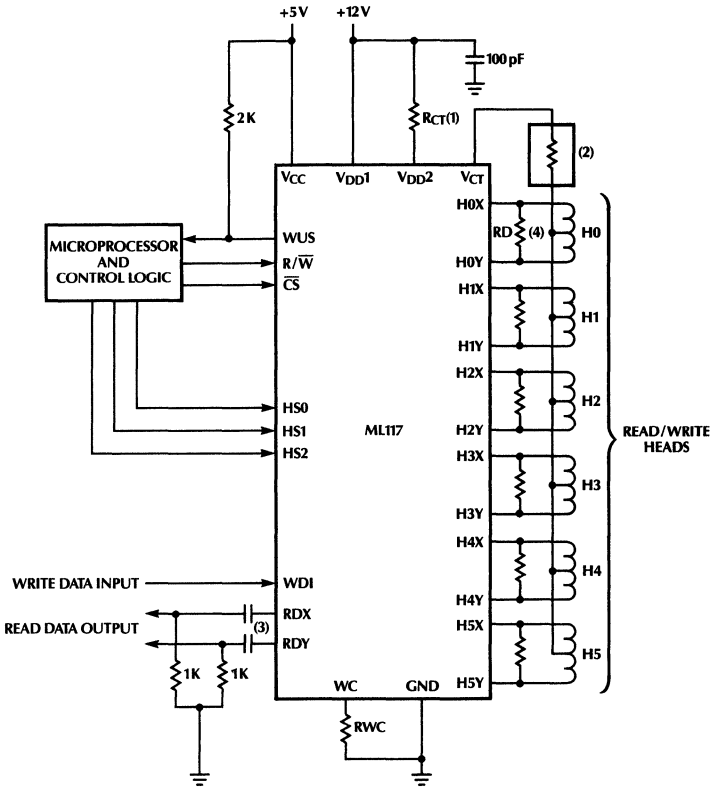
Table 2.

Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

TYPICAL APPLICATION



NOTES:

1. RCT is optional and is used to limit internal power dissipation (Otherwise connect $V_{DD}1$ to $V_{DD}2$).
   RCT (1/2 Watt) = 130 (55/I_W) ohms
   where I_W = Write Current, in mA
2. Ferrite bead optional: used to suppress write current overshoot and ringing. Recommend Ferroxcube 3659065/4A6.
3. RDX and RDY load capacitance 20 pF maximum. RDX and RDY output current must be limited to 100 μA.
4. Damping resistors not required on ML117R.

THERMAL CHARACTERISTICS

28-Lead	
PDIP	80°C/W
PCC	60°C/W
24-Lead	
SOIC	60°C/W
22-Lead	
PDIP	100°C/W
18-Lead	
PDIP	115°C/W
SOIC	85°C/W

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ORDERING INFORMATION

PART NUMBER	PACKAGE	NUMBER OF CHANNELS
ML117-2CP	18-Lead Molded DIP (P18)	2
ML117R-2CP	18-Lead Molded DIP (P18)	2
ML117-2CS	18-Lead Molded SOIC (S18)	2
ML117R-2CS	18-Lead Molded SOIC (S18)	2
ML117-4CP	22-Lead Molded DIP (P22)	4
ML117R-4CP	22-Lead Molded DIP (P22)	4
ML117-4CS	24-Lead Molded SOIC (S24)	4
ML117R-4CS	24-Lead Molded SOIC (S24)	4
ML117-6CP	28-Lead Molded DIP (P28)	6
ML117R-6CP	28-Lead Molded DIP (P28)	6
ML117-6CQ	28-Lead PCC (Q28)	6
ML117R-6CQ	28-Lead PCC (Q28)	6

ML501, ML501R, ML502, ML502R, ML502S–Series

6, 7, or 8-Channel Read/Write Circuits

GENERAL DESCRIPTION

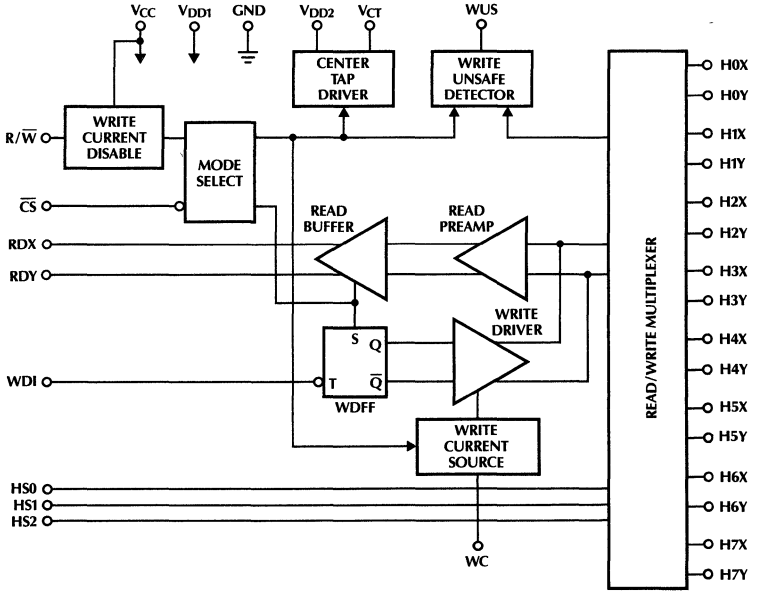
The ML501, ML502 family of devices are bipolar monolithic read/write circuits designed for use with fixed disk center-tapped recording heads. The ML501 and ML501R are designed for use with ferrite recording heads while the ML502, ML502R and ML502S are designed for thin film or composite heads. The R and S designation in the part number indicate that these parts have internal head damping resistors.

The ML501, ML502 family provides up to eight multiplexed read/write data channels. These circuits exhibit features not found in similar read/write circuits such as improved write current stability and the elimination of write current "glitches" during power-up. The exclusive ML502 is identical to the ML501 except that the write unsafe detect circuitry is designed to operate with lower head inductance.

FEATURES

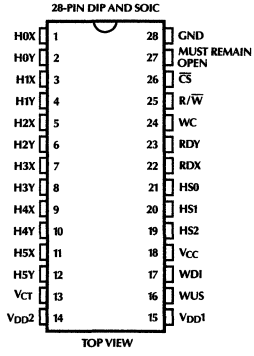
- Exclusive write current disable during power-up
- Enhanced write current stability
- ML501, ML501R is replacement for SSI 32R501/501R and is designed for center-tapped ferrite heads
- ML502, ML502R, and ML502S are designed for center-tapped thin film or composite heads
- Single or multi-platter Winchester drives
- Easily multiplexed for larger systems
- Available in 6, 7 or 8 channels
- TTL compatible control signals
- Programmable write current source
- Includes write unsafe detection
- Available in a selection of packages
- +5V, +12V power supplies

BLOCK DIAGRAM

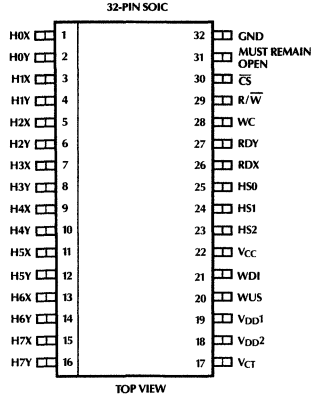


PIN CONNECTIONS

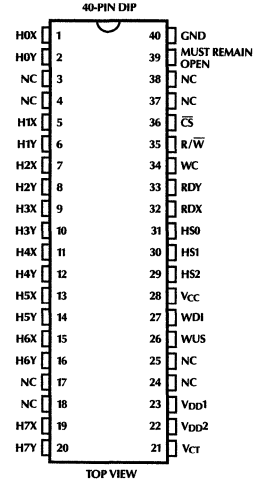
ML501-6 OR ML501R-6 OR ML502-6 OR ML502R-6 6 Channels



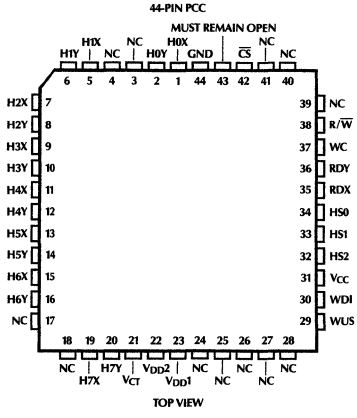
ML501-8 OR ML501R-8 OR ML502-8 OR ML502R-8 8 Channels



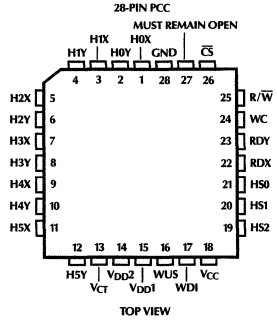
ML501-8 OR ML501R-8 OR ML502-8 OR ML502R-8 8 Channels



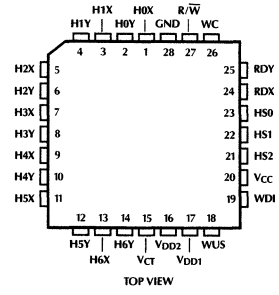
ML501-8 OR ML501R-8 OR ML502-8 OR ML502R-8 OR ML502S-8 8 Channels



ML501-6 OR ML501R-6 OR ML502-6 OR ML502R-6 OR ML502S-6 6 Channels



ML502S-7CQ ML502R-7CQ



PIN DESCRIPTION

NAME	FUNCTION
HS0–HS2	Head Select (eight heads)
$\overline{CS}$	Chip Select (low level enables chip)
R/$\overline{W}$	Read/Write (high level selects Read mode)
WUS	Write Unsafe, open collecter output (high level indicates an unsafe writing condition)
WDI	Write Data In (negative transition toggles head current direction)
H0X–H7X	X head connections
H0Y–H7Y	Y head connections

NAME	FUNCTION
RDX, RDY	X, Y Read Data (differential read signal out)
WC	Write Current (used to set the write current magnitude)
V_{CT}	Voltage Center Tap (center tap voltage source)
V_{CC}	+5 volts
$V_{DD}1$	+12 volts
$V_{DD}2$	Positive supply for center tap
GND	Ground

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- $V_{DD}1$ ..... −0.3 to 14 V_{DC}
- $V_{DD}2$ ..... −0.3 to 14 V_{DC}
- V_{CC} ..... −0.3 to 6 V_{DC}

Input Voltage Range
- Digital Inputs ($\overline{CS}$, R/$\overline{W}$, HS, WDI) ..... −0.3 to V_{CC} +0.3 V_{DC}
- Head Ports (H0X–H7X, H0Y–H7Y .... −0.3 to $V_{DD}1$ +0.3 V_{DC}
- Write Unsafe (WUS) ..... −0.3 to 14 V_{DC}

Write Current (I_W) ..... 60 mA

Output Current
- Read Data (RDX, RDY) ..... −10 mA
- Center Tap Current (I_{CT}) ..... −60 mA
- Write Unsafe (WUS) ..... 12 mA

Storage Temperature ..... −65°C to 150°C

Junction Temperature (T_J) ..... 135°C

Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Supply Voltage
- $V_{DD}1$ ..... 12 V ± 10%
- V_{CC} ..... 5 V ± 10%

Head Inductance
- L_H, ML501 or ML501R only ..... 5 to 15 µH
- L_H, ML502, ML502R, ML502S only ..... 400 to 1000 nH

Damping Resistor (R_D, ML501 only) ..... 500 to 2000 Ω

RCT Resistor (1/2 Watt) ..... 120 Ω ± 5%

Write Current (I_W) ..... 22 to 50 mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $V_{DD}1 = 12\,V \pm 10\%$, $V_{CC} = 5\,V \pm 10\%$, $R_{CT} = 120\,\Omega \pm 5\%$, $I_W = 45\,mA$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC OPERATING CHARACTERISTICS						
POWER SUPPLY						
I_{CC}	V_{CC} Supply Current	Read or Idle Mode			25	mA
		Write Mode			25	mA
I_{DD}	V_{DD} Supply Current	Read Mode			48	mA
		Write Mode			$25 + I_W$	mA
		Idle Mode			20	mA
P_D	Power Dissipation	Read Mode			770	mW
		Write Mode $I_W = 50\,mA$			830	mW
		Write Mode $I_W = 50\,mA$, $R_{CT} = 0\,\Omega$			1125	mW
		Idle Mode			400	mW
DIGITAL INPUTS ($\overline{CS}$, R/$\overline{W}$, HS, WDI)						
V_{IH}	High Voltage		2			V_{DC}
V_{IL}	Low Voltage				0.8	V_{DC}
I_{IH}	High Current	$V_{IH} = 2.0\,V$			100	µA
I_{IL}	Low Current	$V_{IL} = 0.8\,V$	−0.4			mA
WUS OUTPUT						
V_{OL}	Output Low Voltage	$I_{OL} = 8\,mA$ (Safe)			0.5	V_{DC}
I_{OH}	Output High Current	$V_{OH} = 5\,V$ (Unsafe)			100	µA
CENTER TAP VOLTAGES						
V_{CT}	Read Mode	Read Mode		4		V_{DC}
V_{CT}	Write Mode	Write Mode		6		V_{DC}

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 45mA$, $L_H = 10\mu H$ (ML501, ML501R), $L_H = 600nH$ (ML502, ML502R, ML502S), $R_D = 750\Omega$ (ML501), $f_{DATA} = 5MHz$, C_L (RDX, RDY) $\leq 20pF$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE CHARACTERISTICS						
I_{WR}	Write Current Range	$I_W = K/R_{WC}$	10		50	mA
K	Write Current Constant		129		151	V
V_{HD}	Differential Head Voltage Swing		7.5			V_{PK}
I_{HU}	Unselected Head Transient Current				2	mA_{PK}
C_{OD}	Differential Output Capacitance				15	pF
R_{OD}	Differential Output Resistance	ML501, ML502	10k			Ω
		$T_J = 25°C$ ML501R, ML502S/ML502R	560/180		940/300	Ω
f_{WDI}	WDI Transition Frequency	WUS = Low	250			kHz
A_I	I_{WC} to Head Current Gain			20		A/A
I_L	Unselected Head Leakage	Sum of X & Y Side Leakage Current			85	μA
READ MODE CHARACTERISTICS						
A_V	Differential Voltage Gain	$V_{IN} = 1mV_{P-P}$ @ 300kHz, R_L (RDX, RDY) = 1kΩ	90		120	V/V
DR	Dynamic Range	DC Input Voltage (V_I) Where Gain Falls 10%, $V_{IN} = V_I + 0.5mV_{P-P}$ @ 300kHz	−3		+3	mV
BW	Bandwidth (−3dB)	$\|Z_S\| < 5\Omega$, $V_{IN} = 1mV_{P-P}$	30			MHz
e_{IN}	Input Noise Voltage	BW = 15MHz, $L_H = 0$, $R_H = 0$			1.5	$nV/\sqrt{Hz}$
C_{IN}	Differential Input Capacitance	f = 5MHz			23	pF
R_{IN}	Differential Input Resistance	f = 5MHz, $T_J = 25°C$ ML501, ML502	2k			Ω
		$V_{IN} = 6mV_{P-P}$ ML501R, ML502S/ML502R	530/180		790/300	Ω
I_{IN}	Input Bias Current (1 side)				100	μA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V_{CT} + 100mV_{P-P}$ @ f = 5MHz	50			dB
PSRR	Power Supply Rejection Ratio	$100mV_{P-P}$ @ 5MHz on $V_{DD}1$, $V_{DD}2$, or V_{CC}	45			dB
CS	Channel Separation	Unselected Channels: $V_{IN} = 100mV_{P-P}$ @ 5MHz and Selected Channel: $V_{IN} = 0mV_{P-P}$	45			dB
V_{OS}	Output Offset Voltage		−480		+480	mV
V_{OCM}	Common-Mode Output Voltage	Read Mode	5		7	V
		Write or Idle Mode		4.3		V
R_{OUT}	Single-Ended Output Resistance	f = 5MHz			30	Ω
R_L	External Resistive Load (AC Coupled to Output)	Per Side to GND	100			Ω
I_L	Leakage Current, RDX, RDY	3V < (RDX, RDY) < 8V Write or Idle Mode	−50		50	μA
Z_O	Center Tap Output Impedance	0MHz ≤ f ≤ 5MHz			150	Ω
I_O	Output Current	AC Coupled Load, RDX to RDY	2			mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 45mA$, $L_H = 10\mu H$ (ML501, ML501R), $L_H = 600nH$ (ML502, ML502R, ML502S), $R_D = 750\Omega$ (ML501), $f_{DATA} = 5MHz$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_{RW}	R/$\overline{W}$ to Write Switching Delay	To 90% of Write Current Output			600	ns
t_{WR}	R/$\overline{W}$ to Read Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			600	ns
t_{IW} or t_{IR}	$\overline{CS}$ to Select Switching Delay	To 90% of Write Current or to 90% of 100mV, 10MHz Read Signal Envelope			600	ns
t_{WI} or t_{RI}	$\overline{CS}$ to Unselect Switching Delay	To 90% Decay of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			600	ns
t_{HS}	Head Select Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope			600	ns
tD1	Safe to Unsafe Write Unsafe Delay	$I_W = 50mA$	1.6		8	us
tD2	Unsafe to Safe Write Unsafe Delay	$I_W = 20mA$			1	us
tD3	Prop. Delay Head Current	$L_H = 0$, $R_H = 0$ From 50% points		25	40	ns
tD3	Asymmetry Head Current	WDI has 50% Duty Cycle and 1nS Rise/Fall Time			2	ns
	Rise/Fall Head Current	10% and 90% Points			20	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Maximum junction temperature (T_J) should not exceed 135°C.

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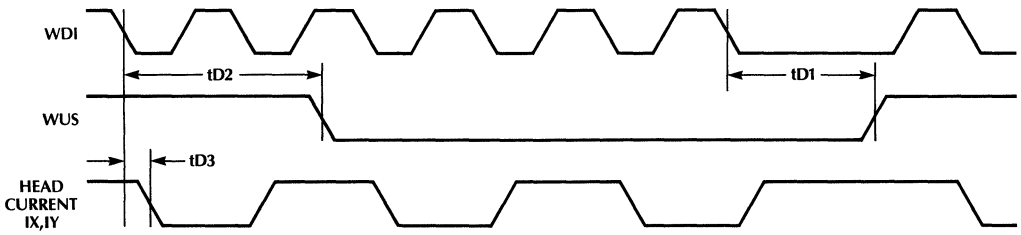
TIMING DIAGRAM



Write Mode Timing Diagram

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

For any selected head, the ML501, ML502 functions as a read amplifier when in the Read mode, or as a write current switch when in the Write mode. Pins $\overline{HS0}$, HS1 and HS2 determine head selection while pin R/$\overline{W}$ controls the Read/Write mode. A detected "write-unsafe" condition is indicated by pin WUS.

READ MODE

When the ML501, ML502 is in the Read Mode, it operates as a low-noise differential amplifier on the selected channel. In Read mode the write data flip-flop is set and both the write unsafe detector and the write current source are deactivated. The center tap voltage is also lowered. Pins RDX and RDY provide differential emitter follower outputs which are in phase with the X and Y head input pins.

Note that during the Read or Chip Deselect mode the internal write current is deactivated, thus making external write current gating unnecessary.

WRITE MODE

The ML501, ML502 operates as a write-current switch when in the Write mode. Write current magnitude is determined by the following relationship:

$I_W = K/R_{WC}$

Where: K = Write Current Constant

R_{WC} = Resistance connected between pin WC and GND.

The head current is toggled between the X and Y side of the selected head by a negative transition on WDI (Write Data Input). When switching the ML501, ML502 to write mode, the WDFF (Write Data Flip-Flop) is initialized to pass write current through the X-side of the head.

The ML501, ML502 exhibit enhanced write current stability, compared to similar read/write circuits, which reduces the problem of oscillation. This is a result of increased internal write current compensation. Also, write current "glitches" during power-up, common in similar read/write circuits, are eliminated with an exclusive write current disabling function.

The WUS (Write Unsafe) pin is an open collector output that gives a logic high level for any of the following unsafe write conditions:

- Open head
- Open head center-tap
- Too low WDI frequency
- Read mode selected
- Device not selected
- No write current

Two negative transitions on WDI are required to clear WUS after the fault condition is removed.

The ML502, ML502R, ML502S differ from the ML501, ML501R by having write unsafe detect circuitry that is designed to operate with lower amplitude write pulse voltages, which result from the lower head inductance of thin film or composite heads.

Table 1.

Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

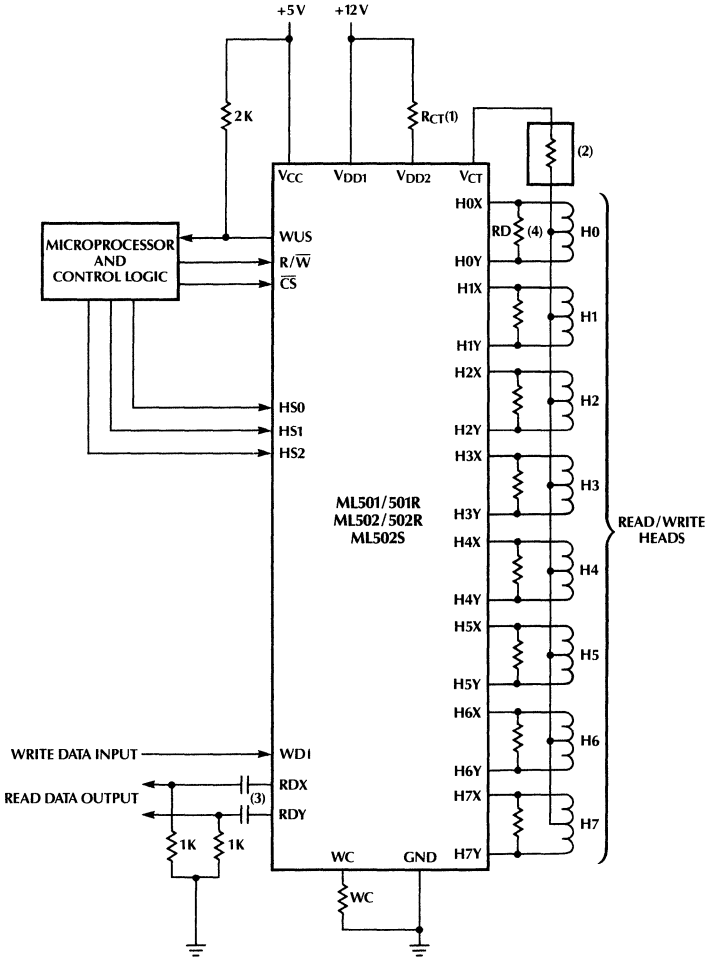
Table 2.

Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

TYPICAL APPLICATION



NOTES:

1. RCT is optional and is used to limit internal power dissipation (Otherwise connect $V_{DD}1$ to $V_{DD}2$).
   RCT (1/2 Watt) = 120 (50/I_W) ohms
   where I_W = Write Current, in mA
2. Ferrite bead optional: used to suppress write current overshoot and ringing. Recommend Ferroxcube 3659065/4A6.
3. RDX and RDY load capacitance 20 pF maximum. RDX and RDY output current must be limited to 100 μA.
4. Damping resistors not required on ML501R or ML502R.

ORDERING INFORMATION

PART NUMBER	PACKAGE	NUMBER OF CHANNELS	TRANSDUCER HEAD TYPE
ML501-6CP	28-Lead Molded DIP (P28)	6	Ferrite Heads
ML501-6CQ	28-Lead PCC (Q28)	6	
ML501-6CS	28-Lead SOIC (S28)	6	
ML501-8CP	40-Lead Molded DIP (P40)	8	
ML501-8CQ	44-Lead PCC (Q44)	8	
ML501-8CS*	32-Lead SOIC (S32)	8	
ML501R-6CP	28-Lead Molded DIP (P28)	6	Ferrite Heads
ML501R-6CQ	28-Lead PCC (Q28)	6	
ML501R-6CS	28-Lead SOIC (S28)	6	
ML501R-8CP	40-Lead Molded DIP (P40)	8	
ML501R-8CQ	44-Lead PCC (Q44)	8	
ML501R-8CS*	32-Lead SOIC (S32)	8	
ML502-6CP	28-Lead Molded DIP (P28)	6	Thin Film or Composite Heads
ML502-6CQ	28-Lead PCC (Q28)	6	
ML502-6CS	28-Lead SOIC (S28)	6	
ML502-8CP	40-Lead Molded DIP (P40)	8	
ML502-8CQ	44-Lead PCC (Q44)	8	
ML502-8CS*	32-Lead SOIC (S32)	8	
ML502R-6CP	28-Lead Molded DIP (P28)	6	Thin Film or Composite Heads
ML502R-6CQ	28-Lead PCC (Q28)	6	
ML502R-6CS	28-Lead SOIC (S28)	6	
ML502R-7CQ	28-Lead PCC (Q28)	7	
ML502R-8CP	40-Lead Molded DIP (P40)	8	
ML502R-8CQ	44-Lead PCC (Q44)	8	
ML502R-8CS*	32-Lead SOIC (S32)	8	
ML502S-6CQ	28-Lead PCC (Q28)	6	Thin Film or Composite Heads
ML502S-7CQ	28-Lead PCC (Q28)	7	
ML502S-8CQ	44-Lead PCC (Q44)	8	

* This package is available as a special order only.

Micro Linear

ML511, ML511R-Series

4, 6, 7, or 8-Channel Ferrite Read/Write Circuits

GENERAL DESCRIPTION

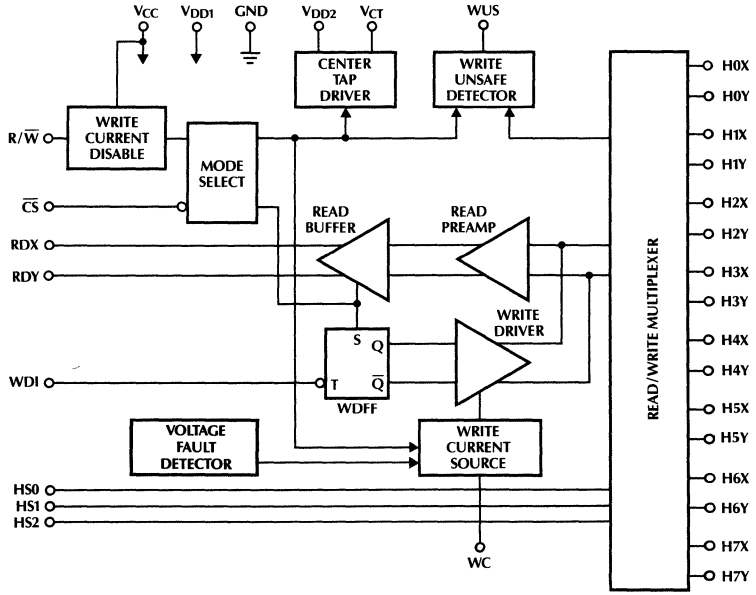
The ML511 is a bipolar monolithic read/write circuit designed for use with center-tapped ferrite recording heads. The ML511 and ML511R are performance upgrades from the ML501 and ML501R. The R designation in the part number indicates that this part has internal head damping resistors.

The ML511 provides up to eight multiplexed read/write data channels. These circuits exhibit features not found in similar read/write circuits such as improved write current stability and the elimination of write current "glitches" during power-up. The ML511 also provides a low noise read data path, and data protection circuitry for all of the channels.

FEATURES

- Enhanced write current stability
- ML511, ML511R is replacement for SSI 32R511/511R and is designed for center-tapped ferrite heads
- Single or multi-platter Winchester drives
- Easily multiplexed for larger systems
- Power supply fault protection
- 1.5 nV/ $\sqrt{Hz}$ maximum input noise voltage
- TTL compatible control signals
- Programmable write current source
- Includes write unsafe detection
- Available in a selection of packages
- +5V, +12V power supplies

BLOCK DIAGRAM



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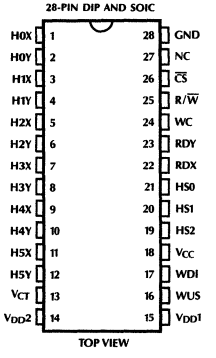
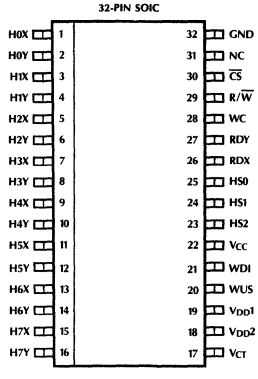
PIN CONNECTIONS

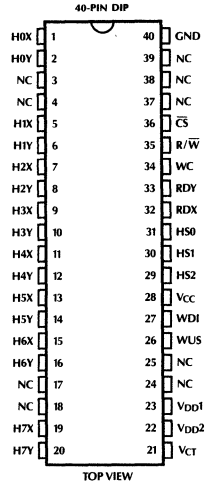
ML511-6 OR ML511R-6
6 Channels



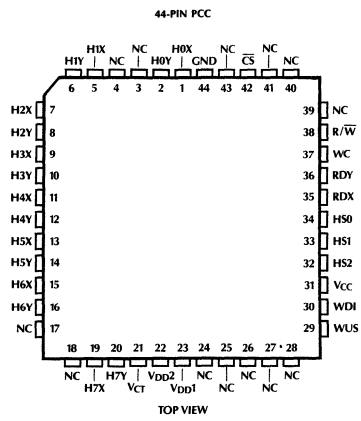
ML511-8 OR ML511R-8
8 Channels



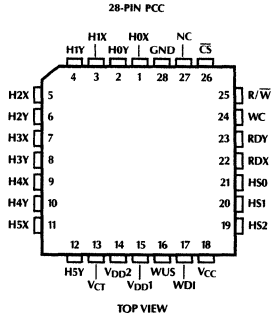
ML511-8 OR ML511R-8
8 Channels



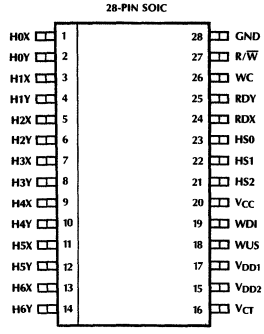
ML511-8 OR ML511R-8
8 Channels



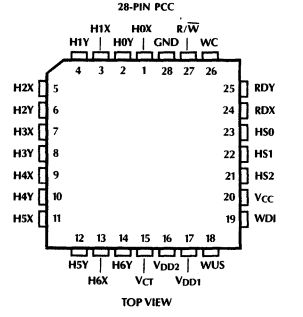
ML511-6 OR ML511R-6
6 Channels



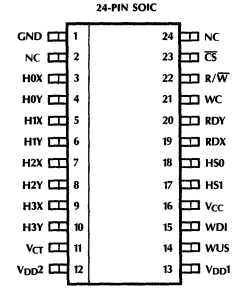
ML511R-7CS
28-Lead SOIC



ML511R-7CQ
28-Lead PCC



ML511-4 OR ML511R-4
4 Channels



PIN DESCRIPTION

NAME	FUNCTION
HS0–HS2	Head Select (eight heads)
$\overline{CS}$	$\overline{\text{Chip Select}}$ (low level enables chip)
R/$\overline{W}$	Read/$\overline{\text{Write}}$ (high level selects Read mode)
WUS	Write Unsafe, open collecter output (high level indicates an unsafe writing condition)
WDI	Write Data In (negative transition toggles head current direction)
H0X–H7X	X head connections
H0Y–H7Y	Y head connections

NAME	FUNCTION
RDX, RDY	X, Y Read Data (differential read signal out)
WC	Write Current (used to set the write current magnitude)
V_{CT}	Voltage Center Tap (center tap voltage source)
V_{CC}	+5 volts
$V_{DD}1$	+12 volts
$V_{DD}2$	Positive supply for center tap
GND	Ground

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- $V_{DD}1$ ..... −0.3 to 14 V_{DC}
- $V_{DD}2$ ..... −0.3 to 14 V_{DC}
- V_{CC} ..... −0.3 to 6 V_{DC}

Input Voltage Range
- Digital Inputs ($\overline{CS}$, R/$\overline{W}$, HS, WDI) ..... −0.3 to V_{CC} +0.3 V_{DC}
- Head Ports (H0X–H7X, H0Y–H7Y .... −0.3 to $V_{DD}1$ +0.3 V_{DC}
- Write Unsafe (WUS) ..... −0.3 to 14 V_{DC}

Write Current (I_W) ..... 60 mA

Output Current
- Read Data (RDX, RDY) ..... −10 mA
- Center Tap Current (I_{CT}) ..... −60 mA
- Write Unsafe (WUS) ..... 12 mA

Storage Temperature ..... −65°C to 150°C

Junction Temperature (T_J) ..... 135°C

Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Supply Voltage
- $V_{DD}1$ ..... 12 V ± 10%
- V_{CC} ..... 5 V ± 10%

Head Inductance
- L_H, ML511 or ML511R ..... 5 to 15 µH

Damping Resistor (R_D, ML511 only) ..... 500 to 2000 Ω

RCT Resistor (1/4 Watt) ..... 120 Ω ± 5%

Write Current (I_W) ..... 10 to 40 mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $V_{DD}1 = V_{DD}2 = 12\,V \pm 10\%$, $V_{CC} = 5\,V \pm 10\%$, $R_{CT} = 120\,\Omega \pm 5\%$, $I_W = 40\,mA$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC OPERATING CHARACTERISTICS						
POWER SUPPLY						
I_{CC}	V_{CC} Supply Current	Read or Idle Mode			35	mA
		Write Mode			30	mA
I_{DD}	V_{DD} Supply Current	Read Mode			35	mA
		Write Mode			$20+I_W$	mA
		Idle Mode			20	mA
P_D	Power Dissipation	Read Mode			655	mW
		Write Mode $I_W = 40\,mA$, $R_{CT} = 0\,\Omega$			960	mW
		Idle Mode			455	mW
DIGITAL INPUTS ($\overline{CS}$, R/$\overline{W}$, HS, WDI)						
V_{IH}	High Voltage		2			V_{DC}
V_{IL}	Low Voltage				0.8	V_{DC}
I_{IH}	High Current	$V_{IH} = 2.0\,V$			100	µA
I_{IL}	Low Current	$V_{IL} = 0.8\,V$	−0.4			mA
WUS OUTPUT						
V_{OL}	Output Low Voltage	$I_{OL} = 8\,mA$ (Safe)			0.5	V_{DC}
I_{OH}	Output High Current	$V_{OH} = 5\,V$ (Unsafe)			100	µA
CENTER TAP VOLTAGES						
V_{CT}	Read Mode	Read Mode		4		V_{DC}
V_{CT}	Write Mode	Write Mode		6		V_{DC}

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ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 35mA$, $L_H = 10\mu H$, $R_D = 750\Omega$ (ML511), $f_{DATA} = 5MHz$, C_L (RDX, RDY) $\leq 20pF$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE CHARACTERISTICS						
I_{HCW}	Head Current (per side)	Write Mode $0 \leq V_{CC} \leq 3.7V$ $0 \leq V_{DD}1 \leq 8.7V$	−200		200	μA
I_{WR}	Write Current Range	$I_W = K/R_{WC}$	10		40	mA
K	Write Current Constant		2.375		2.625	
V_{HD}	Differential Head Voltage Swing		7.0			V_{PK}
I_{HU}	Unselected Head Transient Current				2	mA_{PK}
C_{OD}	Differential Output Capacitance				15	pF
R_{OD}	Differential Output Resistance	ML511	10k			Ω
		$T_J = 25°C$ ML511R	600		960	Ω
f_{WDI}	WDI Transition Frequency	WUS = Low	250			kHz
A_I	I_{WC} to Head Current Gain			0.99		mA/mA
I_L	Unselected Head Leakage	Sum of X & Y Side Leakage Current			85	μA
READ MODE CHARACTERISTICS						
A_V	Differential Voltage Gain	$V_{IN} = 1mV_{P-P}$ @ 300kHz, R_L (RDX, RDY) = 1kΩ	85		115	V/V
DR	Dynamic Range	DC Input Voltage (V_I) Where Gain Falls 10%, $V_{IN} = V_I + 0.5mV_{P-P}$ @ 300kHz	−3		+3	mV
BW	Bandwidth (−3dB)	$\|Z_S\| < 5\Omega$, $V_{IN} = 1mV_{P-P}$	30			MHz
e_{IN}	Input Noise Voltage	BW = 15MHz, $L_H = 0$, $R_H = 0$			1.5	nV/ $\sqrt{Hz}$
C_{IN}	Differential Input Capacitance	f = 5MHz			20	pF
R_{IN}	Differential Input Resistance	f = 5MHz, $T_J = 25°C$ ML511	2k			Ω
		$V_{IN} = 6mV_{P-P}$ ML511R	460		860	Ω
I_{HCR}	Head Current (per side)	Read or Idle Mode $0 \leq V_{CC} \leq 5.5V$ $0 \leq V_{DD}1 \leq 13.2V$	−200		200	μA
I_{IN}	Input Bias Current (1 side)				45	μA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V_{CT} + 100mV_{P-P}$ @ f = 5MHz	50			dB
PSRR	Power Supply Rejection Ratio	$100mV_{P-P}$ @ 5MHz on $V_{DD}1$, $V_{DD}2$, or V_{CC}	45			dB
CS	Channel Separation	Unselected Channels: $V_{IN} = 100mV_{P-P}$ @ 5MHz and Selected Channel: $V_{IN} = 0mV_{P-P}$	45			dB
V_{OS}	Output Offset Voltage	Read Mode	−460		+460	mV
		Write or Idle Mode	−20		+20	mV
V_{OCM}	Common-Mode Output Voltage	Read Mode	4.5		6.5	V
		Write or Idle Mode		5.3		V
R_{OUT}	Single-Ended Output Resistance	f = 5MHz			30	Ω
I_L	Leakage Current, RDX, RDY	(RDX, RDY) = 6V Write or Idle Mode	−100		100	μA
I_O	Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 35mA$, $L_H = 10\mu H$, $R_D = 750\Omega$ (ML511), $f_{DATA} = 5MHz$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_{RW}	R/$\overline{W}$ to Write Switching Delay	To 90% of Write Current Output			1	µs
t_{WR}	R/$\overline{W}$ to Read Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	µs
t_{IW} or t_{IR}	$\overline{CS}$ to Select Switching Delay	To 90% of Write Current or to 90% of 100mV, 10MHz Read Signal Envelope			1	µs
t_{WI} or t_{RI}	$\overline{CS}$ to Unselect Switching Delay	To 90% Decay of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	µs
t_{HS}	Head Select Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope			1	µs
tD1	Safe to Unsafe Write Unsafe Delay	$I_W = 35mA$	1.6		8	us
tD2	Unsafe to Safe Write Unsafe Delay	$I_W = 35mA$			1	us
tD3	Prop. Delay Head Current	$L_H = 0$, $R_H = 0$ From 50% points			25	ns
	Asymmetry Head Current	WDI has 50% Duty Cycle and 1nS Rise/Fall Time			2	ns
	Rise/Fall Head Current	10% and 90% Points			20	ns

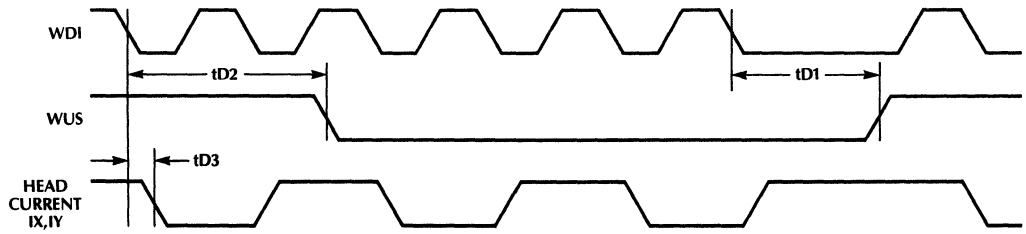
Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Maximum junction temperature (T_j) should not exceed 135°C.

5

TIMING DIAGRAM



Write Mode Timing Diagram

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

For any selected head, the ML511 functions as a read amplifier when in the Read mode, or as a write current switch when in the Write mode. Pins HS0, HS1 and HS2 determine head selection while pin R/$\overline{W}$ controls the Read/Write mode. A detected "write-unsafe" condition is indicated by pin WUS.

READ MODE

When the ML511 is in the Read Mode, it operates as a low-noise differential amplifier on the selected channel. In Read mode the write data flip-flop is set and both the write unsafe detector and the write current source are deactivated. The center tap voltage is also lowered. Pins RDX and RDY provide differential emitter follower outputs which are in phase with the X and Y head input pins.

Note that during the Read or Chip Deselect mode the internal write current is deactivated, thus making external write current gating unnecessary.

WRITE MODE

The ML511 operates as a write-current switch when in the Write mode. Write current magnitude is determined by the following relationship:

$I_W = K/R_{WC}$

Where: K = Write Current Constant

R_{WC} = Resistance connected between pin WC and GND.

The head current is toggled between the X and Y side of the selected head by a negative transition on WDI (Write Data Input). When switching the ML511 to write mode, the WDFF (Write Data Flip-Flop) is initialized to pass write current through the X-side of the head.

The ML511, ML511R exhibit enhanced write current stability, compared to similar read/write circuits, which reduces the problem of oscillation. This is a result of increased internal write current compensation. Also, write current "glitches" during power-up, common in similar read/write circuits, are eliminated with an exclusive write current disabling function.

The WUS (Write Unsafe) pin is an open collector output that gives a logic high level for any of the following unsafe write conditions:

- Open head
- Open head center-tap
- Too low WDI frequency
- Read mode selected
- Device not selected
- No write current

Two negative transitions on WDI are required to clear WUS after the fault condition is removed.

The ML511 also offers a voltage fault detection circuit that prevents write current during power-loss or power-up.

Table 1.

Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

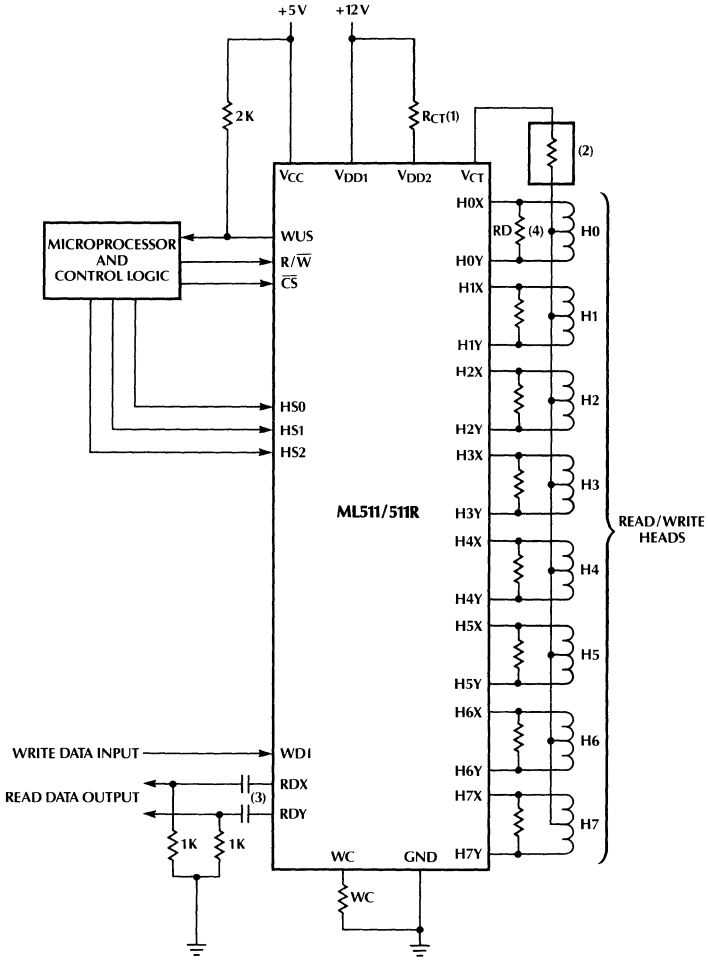
Table 2.

Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

TYPICAL APPLICATION



NOTES:

1. RCT is optional and is used to limit internal power dissipation (Otherwise connect $V_{DD}1$ to $V_{DD}2$).
   RCT (1/2 Watt) = 120 (40/I_W) ohms
   where I_W = Write Current, in mA
2. Ferrite bead optional: used to suppress write current overshoot and ringing. Recommend Ferroxcube 3659065/4A6.
3. RDX and RDY load capacitance 20 pF maximum. RDX and RDY output current must be limited to 100 μA.
4. Damping resistors not required on ML511R.

ORDERING INFORMATION

PART NUMBER	PACKAGE	NUMBER OF CHANNELS
ML511-4CS	24-Lead SOIC (S24)	4
ML511R-4CS	24-Lead SOIC (S24)	4
ML511-6CP	28-Lead Molded DIP (P28)	6
ML511R-6CP	28-Lead Molded DIP (P28)	6
ML511-6CQ	28-Lead PCC (Q28)	6
ML511R-6CQ	28-Lead PCC (Q28)	6
ML511-6CS	28-Lead SOIC (S28)	6
ML511R-6CS	28-Lead SOIC (S28)	6
ML511R-7CS	28-Lead SOIC (S28)	7
ML511R-7CQ	28-Lead PCC (Q28)	7
ML511-8CP	40-Lead Molded DIP (P40)	8
ML511R-8CP	40-Lead Molded DIP (P40)	8
ML511-8CQ	44-Lead PCC (Q44)	8
ML511R-8CQ	44-Lead PCC (Q44)	8
ML511-8CS	32-Lead SOIC (S32)	8
ML511R-8CS	32-Lead SOIC (S32)	8

THERMAL CHARACTERISTICS

PIN COUNT	PACKAGE	θja
24-Lead	SOIC	75°C/W
28-Lead	PDIP	55°C/W
28-Lead	PCC	65°C/W
28-Lead	SOIC	70°C/W
32-Lead	SOIC	60°C/W
44-Lead	PCC	60°C/W
40-Lead	PDIP	45°C/W

Read Data Processor

GENERAL DESCRIPTION

The ML541 is a monolithic bipolar integrated circuit for use in a disk drive system to detect analog pulse peaks generated by the recording head during a Read operation. Connected to the read/write amplifier output, it detects valid data and provides a TTL output to the data separator for further processing. It contains both analog and digital circuitry and supports the reading of MFM and RLL encoded data at rates up to 15 megabits/second.

The primary functional blocks within the device include an AGC amplifier, a level detector, a slope detector, and output logic. Operating modes Read, Write, and Hold are selectable with input logic signals. Read mode is used for pulse peak detection during a Read operation. Write mode disables the device's ouput during a Write operation, while Hold mode holds the AGC gain constant during recovery of embedded servo information.

By using both level and slope detection, accurate pulse validation and peak time detection is acheived. The ML541 performance can be adjusted to fit particular needs through external component selection.

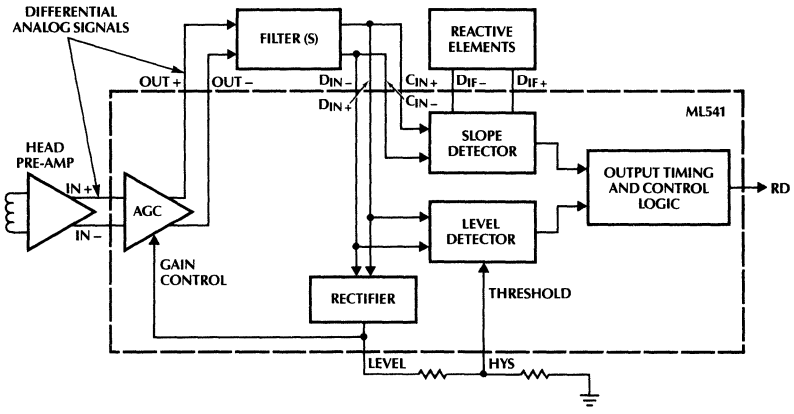
The ML541 is available both in a 24-pin PDIP and 28-pin PCC.

FEATURES

- Second source for SSI 541
- Data rates up to 15 megabits/second
- Supports MFM and RLL encoded read data
- 25 MHz wide-bandwidth AGC amplifier
- Fast AGC region for fast transient recover
- Slow AGC region for minimum zero crossing distortion
- Write to read transient suppression
- Supports embedded servo decoding
- +5V, +12V power supplies

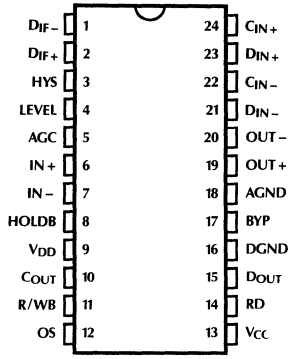
5

SIMPLIFIED BLOCK DIAGRAM

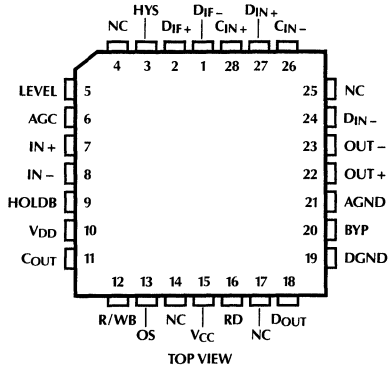


PIN CONNECTIONS

24-Pin DIP and SOIC Package



28-Pin PCC Package



PIN DESCRIPTION

NAME	FUNCTION
V_{CC}	+5V
V_{DD}	+12V
AGND	Analog Ground.
DGND	Digital Ground.
R/WB	TTL compatible Read/Write Control pin.
IN+, IN–	Analog Signal Input pins
OUT+, OUT–	AGC Amplifier Output pins
BYP	The AGC timing capacitor C_{AGC} is tied between this pin and AGND.
HOLDB	TTL compatible pin that holds the AGC gain when pulled low.
AGC	Reference input voltage level for the AGC circuit.
D_{IN+}, D_{IN-}	Analog input to the hysteresis comparator.

NAME	FUNCTION
HYS	Input for setting hysteresis level of the hysteresis comparator.
LEVEL	Provides rectified signal level for input to the hysteresis comparator.
D_{OUT}	Buffered test point for monitoring D input of the flip-flop.
C_{IN+}, C_{IN-}	Analog input to the differentiator.
D_{IF+}, D_{IF-}	External differentiating network connection pins.
C_{OUT}	Buffered test point for monitoring the clock input to the flip-flop.
OS	Connection for read output pulse width setting capacitor C_{OS}.
RD	TTL compatible read output.

TABLE 1 MODE SELECT

R/WB	HOLDB	MODE	DESCRIPTION
1	1	READ	AGC amp section active, Digital section active.
1	0	HOLD	AGC gain constant, Digital section active.
0	X	WRITE	AGC gain maximum, Digital section inactive, Input common mode resistance reduced.

0 = Logic level low
1 = Logic level high
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- V_{CC} ..... −0.3 to 6 V_{DC}
- V_{DD} ..... −0.3 to 14 V_{DC}

Terminal Voltage Range
- R/WB, IN+, IN−, HOLDB ..... −0.3 V to V_{CC} +0.3 V
- RD ..... −0.3 V to V_{CC} +0.3 V or +12 mA
- All others ..... −0.3 V to V_{DD} +0.3 V

Storage Temperature Range ..... −65°C to +150°C
Junction Temperature (T_J) ..... +135°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

Supply Voltage
- V_{CC} ..... 5 V ± 10%
- V_{DD} ..... 12 V ± 10%

$V_{(C_{IN+}-C_{IN-})}$, $V_{(D_{IN+}-D_{IN-})}$ ..... 1 V_{P-P}
V_{HYS} ..... 1.0 V
C_{OS} ..... 50 to 200 pF

Typical Component Values (Refer to Typical Applications)
- C_{IN} ..... 0.001 µF
- C_S ..... 0.01 µF
- C_{OUT} ..... 0.0047 µF
- R_{OUT} ..... 400 Ω
- C_{AGC1} ..... 220 pF
- C_{AGC2} ..... 2000 pF
- R_{AGC} ..... 2.21 kΩ
- C_{LEVEL} ..... 150 pF
- R_{LEVEL1} ..... 1.54 kΩ
- R_{LEVEL2} ..... 6.49 kΩ
- C_{OS} ..... 50 pF

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of V_{CC} = 5 V ± 10%, V_{DD} = 12 V ± 10%, 0°C < T_A < 70°C and external components as specified under recommended operating conditions unless otherwise specified. (See Note 2.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 5	MAX	UNITS
DC Characteristics						
I_{CC}	V_{CC} Supply Current	Outputs unloaded			14	mA
I_{DD}	V_{DD} Supply Current	Outputs unloaded			70	mA
P_D	Power Dissipation	Outputs unloaded, T_A = 70°C			930	mW
Digital Inputs Characteristics (HOLDB, R/WB)						
V_{IH}	High Voltage		2			V
V_{IL}	Low Voltage				0.8	V
I_{IH}	High Current	V_{IH} = 2.4 V			100	µA
I_{IL}	Low Current	V_{IL} = 0.4 V	−0.4			mA
Digital Outputs Characteristics (C_{OUT}, RD)						
V_{OL}	Output Low Voltage	I_{OL} = 4 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 400 µA	2.4			V
WRITE AND HOLD MODE CHARACTERISTICS						
Mode Control						
t_{RW}	Read to Write Transition Time				1	µs
t_{WR}	Write to Read Transition Time	AGC settling not included, time to high input resistance	1.2		3	µs
t_{RH}	Read to Hold Transition Time				1	µs
Write Mode						
Z_{IC}	Common Mode Input Impedance (both sides)	R/WB pin = low		250		Ω

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ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of V_{CC} = 5V ± 10%, V_{DD} = 12V ± 10%, 0°C ≤ T_A ≤ 70°C, IN+ and IN− AC coupled, OUT+ and OUT− differentially loaded with >600Ω and each side loaded with <10pF to GND, C_{BYP} = 2000pF, OUT+ and OUT− AC coupled to D_{IN+} and D_{IN-} respectively, V_{AGC} = 2.2V unless otherwise specified. (See Note 2.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 5	MAX	UNITS
READ MODE CHARACTERISICS						
AGC Amplifier						
R_{ID}	Differential Input Resistance	$V_{(IN+-IN-)}$ = 100mV$_{P-P}$ @ 2.5MHz		5		kΩ
C_{ID}	Differential Input Capacitance	$V_{(IN+-IN-)}$ = 100mV$_{P-P}$ @ 2.5MHz			10	pF
Z_{IC}	Common Mode Input Impedance (both sides)	R/WB pin high		1.8		kΩ
		R/WB pin low		0.25		kΩ
A_{VR}	Gain Range	1V$_{P-P}$ ≤ $V_{OUT\,diff}$ < 2.5V$_{P-P}$	4		83	V/V
e_N	Input Noise Voltage	Gain set to maximum			30	nV/ $\sqrt{Hz}$
BW	Bandwidth	Gain set to maximum, −3dB point	25			MHz
V_{OP}	Maximum Output Voltage Swing	Set by V_{AGC}	3			V_{P-P}
I_{OD}	OUT+ to OUT− Pin Current	No DC path to GND, See Note 3	±3.2			mA
R_O	Output Resistance			20	30	Ω
C_O	Output Capacitance			12		pF
V_{IP} / V_{AGC}	($D_{IN+} - D_{IN-}$) Input Voltage Swing VS AGC Input Level	30mV$_{P-P}$ ≤ $V_{(IN+-IN-)}$ ≤ 550mV$_{P-P}$, 1.5V ≤ V_{AGC} ≤ 3.75V		0.48		V_{P-P}/V
V_{IP}	($D_{IN+} - D_{IN-}$) Input Voltage Swing Variation	30mV$_{P-P}$ < $V_{(IN+-IN-)}$ < 550mV$_{P-P}$, AGC Fixed, over supply and temp.			+8	%
t_D	Gain Decay Time	See Figure 1a; V_{IN} = 300mV$_{P-P}$ then >150mV$_{P-P}$ at 2.5MHz, V_{OUT} to 90% of final value.		50		µs
t_A	Gain Attack Time	See Figure 1b; from Write to Read transition to V_{OUT} at 110% of final value, V_{IN} = 400mV$_{P-P}$ @ 2.5MHz		4		µs
I_{AGCfc}	Fast AGC Capacitor Charge Current	$V_{(D_{IN+}-D_{IN-})}$ = 1.6V, V_{AGC} = 3.0V		1.5		mA
I_{AGCsc}	Slow AGC Capacitor Charge Current	$V_{(D_{IN+}-D_{IN-})}$ = 1.6V, Vary V_{AGC} until slow discharge begins		0.17		mA
	Fast to Slow Attack Switchover Point	$V_{(D_{IN+}-D_{IN-})}$		1.25		-
		$V_{(D_{IN+}-D_{IN-})}$ Final				
I_{AGCD}	AGC Capacitor Discharge Current	$V_{(D_{IN+}-D_{IN-})}$ = 0.0V Read Mode		4.5		µA
		Hold Mode	−0.2		+0.2	µA
CMRR	CMRR (Input Referred)	$V_{IN+} = V_{IN-}$ = 100mV$_{P-P}$ @ 5MHz, gain at max.	40			dB
PSRR	PSRR (Input Referred)	V_{CC} or V_{DD} = 100mV$_{P-P}$ @ 5MHz, gain at max.	30			dB
Hysteresis Comparator						
V_{IP}	Input Signal Range				1.5	V_{P-P}
R_{ID}	Differential Input Resistance	$V_{(D_{IN+}-D_{IN-})}$ = 100mV$_{P-P}$ @ 2.5MHz	5		15	kΩ
C_{ID}	Differential Input Capacitance	$V_{(D_{IN+}-D_{IN-})}$ = 100mV$_{P-P}$ @ 2.5MHz			6.0	pF
Z_{IC}	Common Mode Input Impedance	(both sides)		2.0		kΩ
V_{IO}	Comparator Offset Voltage	HYS pin at −0.5V, ≤1.5kΩ across D_{IN+}, D_{IN-}		5		mV

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of $V_{CC}=5V\pm10\%$, $V_{DD}=12V\pm10\%$, $0°C\leq T_A\leq 70°C$, IN+ and IN− AC coupled, OUT+ and OUT− differentially loaded with >600Ω and each side loaded with <10pF to GND, $C_{BYP}=2000pF$, OUT+ and OUT− AC coupled to D_{IN+} and D_{IN-} respectively, $V_{AGC}=2.2V$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ MODE CHARACTERISICS (Continued)						
Hysteresis Comparator (Continued)						
V_{HYSP} V_{HYS}	Peak Hysteresis Voltage vs HYS pin voltage (input referred)	$1V<V_{HYS}<3V$		0.21		V/V
I_I	HYS Pin Input Current	$1V<V_{HYS}<3V$	0		−20	μA
I_O	LEVEL Pin Max Output Current		3			mA
R_O	LEVEL Pin Output Resistance	$I_{LEVEL}=0.5mA$		180		Ω
V_{OL}	D_{OUT} Pin Output Low Voltage	$T_A=70°C$	$V_{DD}-4.0$		$V_{DD}-2.5$	V
V_{OH}	D_{OUT} Pin Output High Voltage	$T_A=70°C$	$V_{DD}-2.2$		$V_{DD}-1.5$	V
V_{OL}	D_{OUT} Pin Output Low Voltage	$T_A=25°C$	$V_{DD}-4.0$		$V_{DD}-2.8$	V
V_{OH}	D_{OUT} Pin Output High Voltage	$T_A=25°C$	$V_{DD}-2.5$		$V_{DD}-1.6$	V
Active Differentiator						
V_{IP}	Input Signal Range				1.5	V_{P-P}
R_{ID}	Differential Input Resistance	$V_{(C_{IN+}-C_{IN-})}=100mV_{P-P}$ @ 2.5MHz	5		15	kΩ
C_{ID}	Differential Input Capacitance	$V_{(C_{IN+}-C_{IN-})}=100mV_{P-P}$ @ 2.5MHz			6	pF
Z_{IC}	Common Mode Input Impedance	(both sides)		2.0		kΩ
I_{OD}	D_{IF+} to D_{IF-} Pin Current	Differentiator Imped must be set so as not to clip signal at this current level	±1.3			mA
V_{IO}	Comparator Offset Voltage	D_{IF+}, D_{IF-} AC Coupled		5		mV
V_{OL}	C_{OUT} Pin Output Low Voltage	$0\leq I_{OH}\leq 0.5mA$		$V_{DD}-3$		V
V_{PO}	C_{OUT} Pin Output Pulse Voltage	$0\leq I_{OH}\leq 0.5mA$		0.4		V
PW_0	C_{OUT} Pin Output Pulse Width	$0\leq I_{OH}\leq 0.5mA$		30		ns

The following specifications apply over the recommended operating conditions of $V_{CC}=5V\pm10\%$, $V_{DD}=12V\pm10\%$, $0°C\leq T_A\leq 70°C$, $V_{(C_{IN+}-C_{IN-})}=V_{(D_{IN+}-D_{IN-})}=1.0V_{P-P}$ AC coupled sine wave at 2.5MHz, $R_{D_{IF}}=100Ω$, $C_{D_{IF}}=65pF$, $V_{HYS}=1.8V$, $C_{OS}=60pF$, 4kΩ to V_{CC} and 10pF to GND on pin RD unless otherwise specified.

Output Data Characteristics (Refer to Figure 2)						
t_{D1}	D-Flip-Flop Set Up Time	Min delay from $V_{(D_{IN+}-D_{IN-})}$ exceeding threshold to $V_{(D_{IF+}-D_{IF-})}$ reaching a peak	0			ns
t_{D3}	Propagation Delay				110	ns
t_{D5}	Output Data Pulse Width	$T_A=25°C$, $V_{CC}=5V$, $V_{DD}=12V$		±15%		
t_{D5}	Output Data Pulse Width Variation	$C_{OS}=60pF$, See Note 4	30		80	ns
t_{D3}-t_{D4}	Logic Skew (Pulse Pairing)				3	ns
t_R	Output Rise Time	$V_{OH}=2.4V$			18	ns
t_F	Output Fall Time	$V_{OL}=0.4V$			14	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: AGC amplifier output current may be increased as in Figure 4.

Note 4: $t_{D5}\cong 770\ (C_{OS})$, $50pF < C_{OS} < 150pF$.

Note 5: Typicals are parametric norm at 25°C

FUNCTIONAL DESCRIPTION

Operating Modes

The ML541 has three definitive operation modes which are: Read mode, Write mode and Hold mode. These modes are defined by input pins HOLDB and R/WB as shown in Table 1. Read mode, the mode used normally for pulse detection, is assumed in the following sections unless otherwise noted.

AGC Amplifier Section

The purpose of the AGC amplifier is to provide a constant read signal level for both the level and slope detectors. Full differential processing of the read signal is used to minimize noise and distortion in the analog signal. A wide gain range is required due to large signal variation when moving the recording head from an inside to outside data track or variations in media.

The differential output voltage level V_{OUT} from the AGC amp is determined by voltage V_{AGC} present at pin AGC. V_{OUT} is full wave rectified and compared against V_{AGC} to create charge/discharge current for capacitor C_{BYP} connected at pin BYP. Voltage V_{BYP} across C_{BYP} controls the gain in the AGC amplifier.

Two distinct values of I_{BYP} are possible which determine a fast and slow AGC gain response attack rate. When V_{OUT} is more than 125% of the set level a high value of I_{BYP} is sourced which provides a fast AGC attack rate. When V_{OUT} is within 100% to 125% of the set level a reduced value of I_{BYP} is sourced which provides a slower attack rate. The fast-slow gain response attack rates provides for an initial quick system response and then minimum zero crossing distortion of the analog signal once the gain is within working range. V_{AGC} should be set so that the differential input voltage V_{DIN} into the level comparator is $1V_{P-P}$ at nominal Read signal conditions. The AGC amp section gain is given by:

$$\frac{A_{V2}}{A_{V1}} = \exp \frac{V_{BYP2} - V_{BYP1}}{5.8 \times V_T}$$

Where: A_{V1}, A_{V2} are initial and final amplifier gain values corresponding to initial and final V_{BYP} values.

$V_T = (KT)/Q = 26\,mV$ at room temperature.

The AGC amp's differential inputs must be AC coupled to the read amplifier (ML117, ML501, etc.) differential outputs. Similarly, AC coupling must be used at the AGC amp outputs.

AGC Amp During Write Mode— When the ML541 is put into write mode, the AGC amp's input impedance is lowered to allow a faster dampening of the Write to Read transient from the head pre-amp. The AGC gain is also set to maximum gain so that fast AGC attack will occur when changing back to the Read mode. Internal device timing is controlled so that settling occurs prior to Read mode activation. Minimal value input coupling capacitors should be chosen to reduce settling time, however, bandwidth requirements also need to be considered.

AGC Amp During Hold Mode— During the Hold mode, the charge/discharge current driving pin BYP is internally disconnected. AGC compensation capacitor C_{AGC} will then hold the present gain setting. The amplitude of V_{OUT} will therefore not affect the AGC gain and gain will remain constant.

Hold mode is used so that AGC gain will not be adjusted when embedded servo information is read. This prevents loosing the pulse peak amplitude information needed during position decoding, or creating additional gain settling time when again reading data. Embedded servo pulses are normally taken at outputs D_{IF-} and D_{IF+}, as shown in the typical application.

External Filter Network

Filtering for the level and slope detectors can be performed with a single filter or two separate filters. If separate filters are used, care must be used to insure that time delays are matched. A multi-pole Bessell filter is recommended due to the group delay and linear phase characteristics.

Level Detector

The full wave rectified V_{OUT} is buffered and available at pin LEVEL. The level detector uses a hysteresis comparator to compare the processed read signal amplitude against a reference voltage derived from voltage V_{LEVEL} output from pin LEVEL. Using V_{LEVEL} provides a feed-forward function that allows valid level detection to be performed prior to AGC amp gain settling. The level detector hysteresis value is set in a way that will only allow relatively large read pulse peaks (negative or positive) to be detected.

Slope Detector

The slope detector uses an external reactive component network to produce a voltage signal proportional to the differential of the read signal. By using a hysteresis comparator to detect zero slope of the read signal, the time occurrence of positive or negative read pulse peak values can be determined.

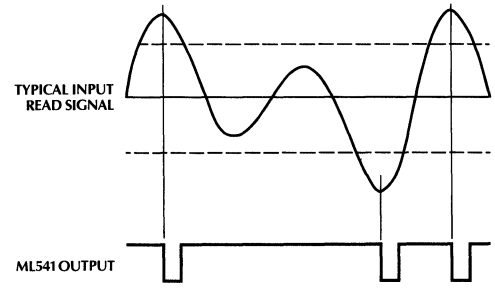
An external reactive network, shown in the Typical Application, is used between the D_{IF+} and D_{IF-} pins to provide the differential function given by:

$$A_V = \frac{-2000Cs}{LCs^2 + (R + 92)\,Cs + 1}$$

Where: C = External capacitor (20 pF to 150 pF)
L = External inductor
R = External resistor
$s = j\omega = j2\pi f$

Output Logic

The output logic provides a negative TTL pulse at pin RD which begins at the peak of a valid read pulse, as shown below.

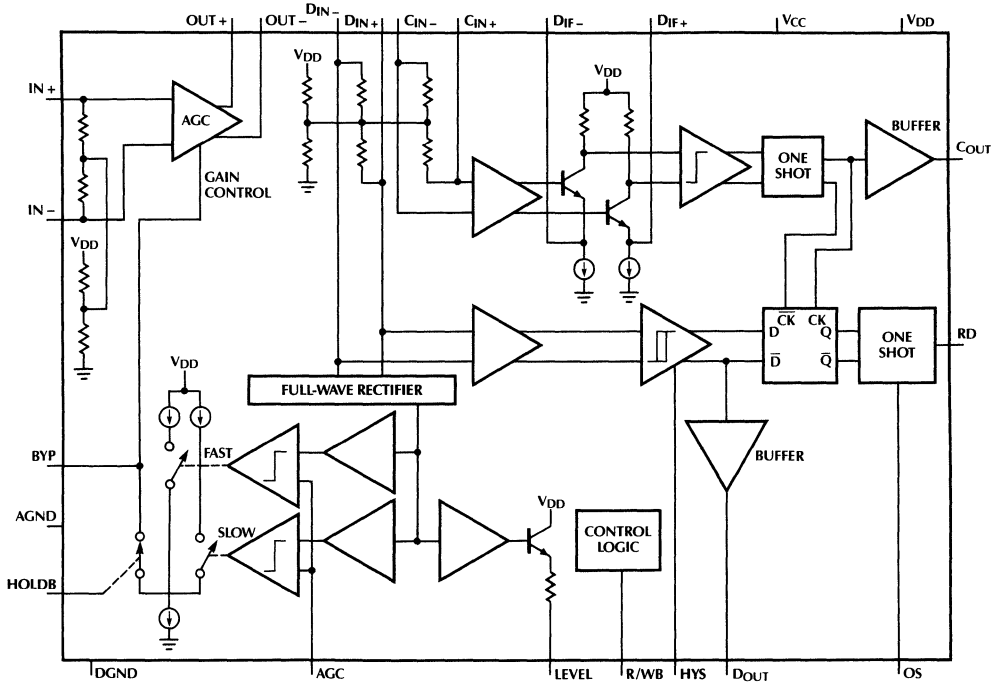


Pin R/WB must be high for the output logic to be active. The key element in the output logic is the D flip-flop. The flip-flop is clocked by the slope detector at the time of a zero crossing, which loads data from level detector. The flip-flop inputs only change state when the level detector detects a peak amplitude of a polarity opposite to the previous valid peak. Thus, through the output logic the slope detector determines output timing and the level detector determines pulse validity.

Layout Considerations

As with any high gain, wide bandwidth analog circuitry, care needs to be exercised in PC layout. Power supply and ground lines should be bypassed and well isolated from other circuitry. A ground plane is recommended, as is keeping analog lines short and well balanced to prevent interaction with nearby circuitry in the disk drive.

BLOCK DIAGRAM



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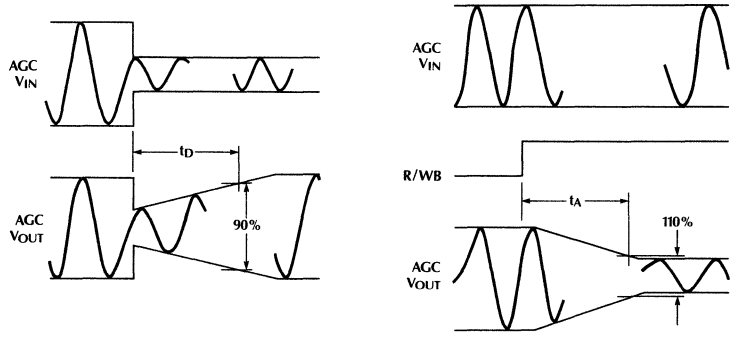

Figure 1. AGC Timing Diagram

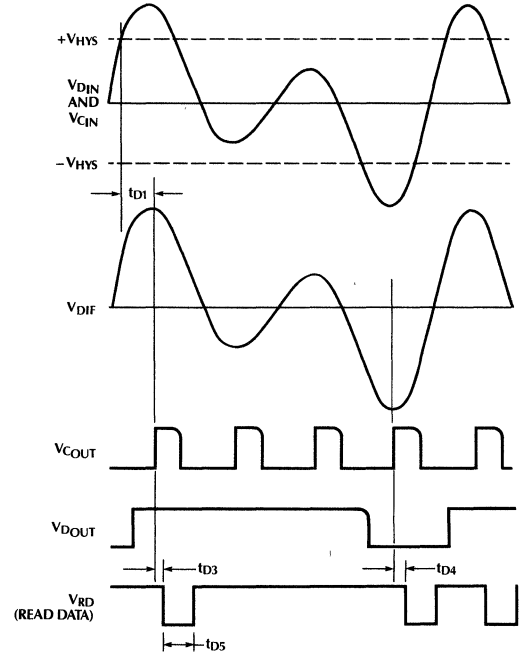

Figure 2. Output Logic Timing Diagram

TYPICAL APPLICATIONS

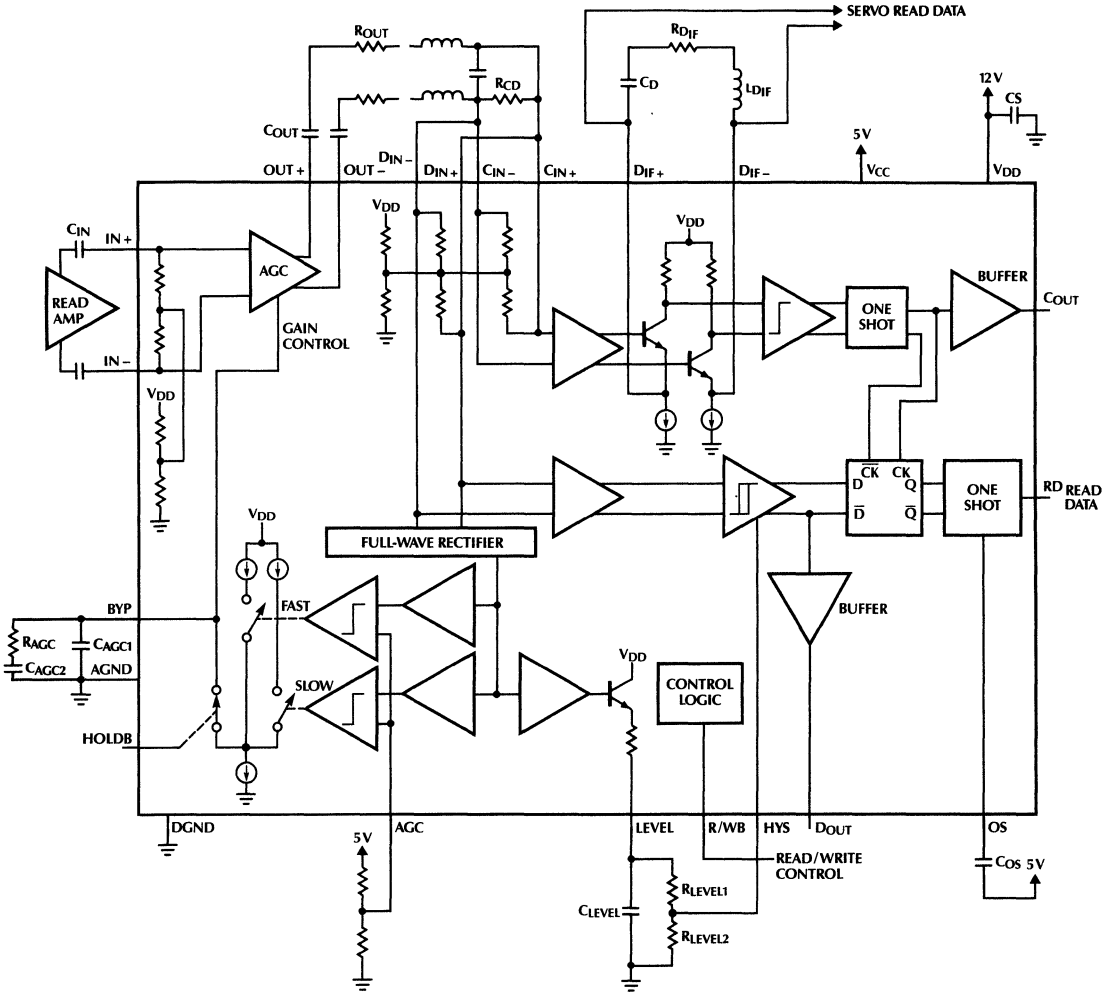

Figure 3. Typical Application Diagram

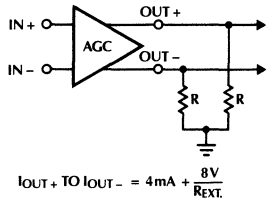

Figure 4. Modification of AGC Amplifier Output to Drive Low Impedance Filters

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML541CP	0°C to +70°C	MOLDED DIP (P24)
ML541CJ	0°C to +70°C	HERMETIC DIP (J24)
ML541CQ	0°C to +70°C	MOLDED PCC (Q28)
ML541CS	0°C to +70°C	MOLDED SOIC (S24)

ML4041, ML4042

Read Data Processor

GENERAL DESCRIPTION

The ML4041, ML4042 is a monolithic bipolar integrated circuit used in disk drive systems to detect amplitude peaks generated by the recording heads during a Read operation. Connected to the read/write amplifier output, it detects valid data and provides a TTL output to the data separator. Containing both analog and digital circuitry, it supports the reading of MFM and RLL encoded data at rates up to 24 megabits/second.

Operating modes Read, Write, and Hold are selectable with input logic signals. Read mode is used for pulse peak detection during a Read operation. Write mode disables the device's output during a Write operation, while Hold mode holds the AGC gain constant during recovery of embedded servo information.

By using both level and slope detection, accurate pulse validation and peak time detection is achieved. The ML4041, ML4042 characteristics can be modified to fit particular needs through external component selection. The ML4041, ML4042 has a swift Write to Read recovery time of 2μs (10μs max) allowing for better format efficiency with faster access times. Pulse pairing of 1ns max reduces data decoding errors by allowing tighter specs for the clock recovery circuit.

FEATURES

- Fully compatible with industry standard read data processor
- Write to Read recovery time — 2μs typical, 10μs max
- Pulse pairing — 1ns max
- Data rates up to 24 megabits/second
- Supports MFM and RLL encoded read data
- 30MHz wide-bandwidth AGC amplifier
- Fast AGC region for fast transient recover
- Slow AGC region for minimum zero crossing distortion
- +5V and +12V undervoltage fault detection (ML4042 only)
- Write to read transient suppression
- Hold pin supports embedded servo decoding

The ML4042 is identical to the ML4041 but in addition it includes a +5V and +12V undervoltage detector. The ML4041 is available in a 24-pin PDIP, 24-pin SOIC, or a 28-pin PCC, while the ML4042 is available in a 28-pin PDIP, 28-pin SOIC, or a 28-pin PCC.

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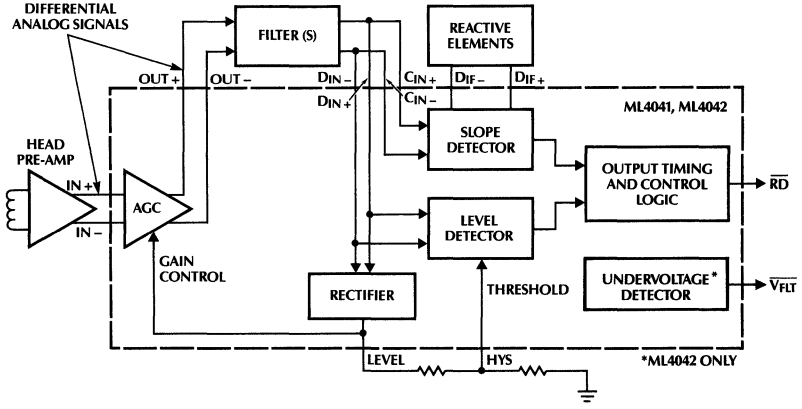
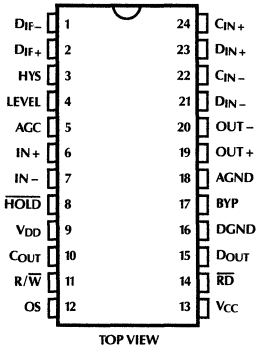
SIMPLIFIED BLOCK DIAGRAM

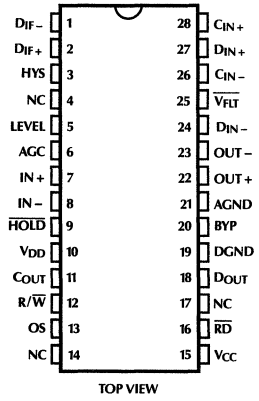


PIN CONNECTIONS

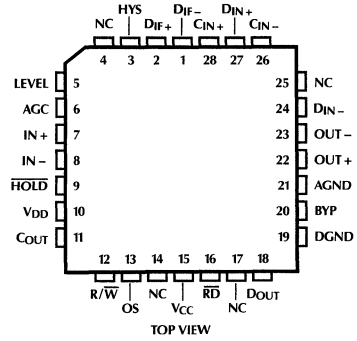
ML4041
24-Pin DIP and SOIC Package



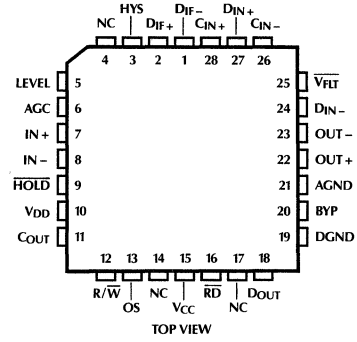
ML4042
28-Pin DIP and SOIC Package



ML4041
28-Pin PCC Package



ML4042
28-Pin PCC Package



PIN DESCRIPTION

NAME	FUNCTION
V_{CC}	+5V
V_{DD}	+12V
AGND	Analog Ground.
DGND	Digital Ground.
R/$\overline{W}$	TTL compatible Read/Write Control pin.
IN+, IN–	Analog Signal Input pins
OUT+, OUT–	AGC Amplifier Output pins
BYP	The AGC timing capacitor C_{AGC} is tied between this pin and AGND.
$\overline{HOLD}$	TTL compatible pin that holds the AGC gain when pulled low.
AGC	Reference input voltage level for the AGC circuit.
D_{IN+}, D_{IN-}	Analog input to the hysteresis comparator.

NAME	FUNCTION
HYS	Input for setting hysteresis level of the hysteresis comparator.
LEVEL	Provides rectified signal level for input to the hysteresis comparator.
D_{OUT}	Buffered test point for monitoring D input of the flip-flop.
C_{IN+}, C_{IN-}	Analog input to the differentiator.
D_{IF+}, D_{IF-}	External differentiating network connection pins.
C_{OUT}	Buffered test point for monitoring the clock input to the flip-flop.
OS	Connection for read output pulse width setting capacitor C_{OS}.
$\overline{RD}$	TTL compatible read output.
$\overline{V_{FLT}}$	Undervoltage detector output, active low; ML4042 only.

TABLE 1 MODE SELECT

R/$\overline{W}$	$\overline{HOLD}$	MODE	DESCRIPTION
1	1	READ	AGC amp section active, Digital section active.
1	0	HOLD	AGC gain constant, Digital section active.
0	X	WRITE	AGC gain maximum, Digital section inactive, Input common mode resistance reduced.

0 = Logic level low
1 = Logic level high
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- V_{CC} ..... −0.3 to 6 V_{DC}
- V_{DD} ..... −0.3 to 14 V_{DC}

Terminal Voltage Range
- R/W, IN+, IN−, HOLD ..... −0.3V to V_{CC} +0.3V
- RD ..... −0.3V to V_{CC} +0.3V or +12mA
- All others ..... −0.3V to V_{DD} +0.3V

Storage Temperature Range ..... −65°C to +150°C
Junction Temperature (T_J) ..... +135°C
Lead Temperature (Soldering, 10sec) ..... 260°C

OPERATING CONDITIONS

Supply Voltage
- V_{CC} ..... 5V ± 10%
- V_{DD} ..... 12V ± 10%

$V_{(C_{IN+}-C_{IN-})}$, $V_{(D_{IN+}-D_{IN-})}$ ..... $1V_{P-P}$
V_{HYS} 1.0V
C_{OS} ..... 50 to 200pF

Typical Component Values (Refer to Typical Applications)
- C_{IN} 0.001μF
- C_S 0.01μF
- C_{OUT} 0.0047μF
- R_{OUT} 400Ω
- C_{AGC1} 220pF
- C_{AGC2} 2000pF
- R_{AGC} 2.21kΩ
- C_{LEVEL} 150pF
- R_{LEVEL1} 1.54kΩ
- R_{LEVEL2} 6.49kΩ
- C_{OS} 50pF

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of V_{CC} = 5V ± 10%, V_{DD} = 12V ± 10%, 0°C < T_A < 70°C and external components as specified under operating conditions unless otherwise specified. (See Note 2.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 4	MAX	UNITS
DC Characteristics						
I_{CC}	V_{CC} Supply Current	Outputs unloaded			14	mA
I_{DD}	V_{DD} Supply Current	Outputs unloaded			70	mA
P_D	Power Dissipation	Outputs unloaded, T_A = 70°C			930	mW
Digital Inputs Characteristics ($\overline{HOLD}$, R/$\overline{W}$)						
V_{IH}	High Voltage		2			V
V_{IL}	Low Voltage		−0.3		0.8	V
I_{IH}	High Current	V_{IH} = 2.4V			100	μA
I_{IL}	Low Current	V_{IL} = 0.4V	−0.4			mA
Digital Outputs Characteristics (C_{OUT}, $\overline{RD}$)						
V_{OL}	Output Low Voltage	I_{OL} = 4mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 400μA	2.4			V
WRITE AND HOLD MODE CHARACTERISTICS						
Mode Control						
t_{RW}	Read to Write Transition Time				1	μs
t_{WR}	Write to Read Transition Time	AGC settling not included, time to high input resistance	1.2		3	μs
t_{RH}	Read to Hold Transition Time				1	μs
Write Mode						
Z_{IC}	Common Mode Input Impedance (both sides)	R/$\overline{W}$ pin = low		250		Ω

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ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of $V_{CC} = 5V \pm 10\%$, $V_{DD} = 12V \pm 10\%$, $0°C \leq T_A \leq 70°C$, IN+ and IN− AC coupled, OUT+ and OUT− differentially loaded with >600Ω and each side loaded with <10pF to GND, $C_{BYP} = 2000pF$, OUT+ and OUT− AC coupled to D_{IN+} and D_{IN-} respectively, $V_{AGC} = 2.2V$ unless otherwise specified. (See Note 2.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 4	MAX	UNITS
READ MODE CHARACTERISICS						
AGC Amplifier						
R_{ID}	Differential Input Resistance	$V_{(IN+-IN-)} = 100mV_{P-P}$ @ 2.5MHz		5		kΩ
C_{ID}	Differential Input Capacitance	$V_{(IN+-IN-)} = 100mV_{P-P}$ @ 2.5MHz			10	pF
Z_{IC}	Common Mode Input Impedance (both sides)	$R/\overline{W}$ pin high		1.8		kΩ
		$R/\overline{W}$ pin low		0.25		kΩ
$A_{V_{MAX}}$	Maximum Gain	$V_{BYP} = 2.6V$	83			V/V
$A_{V_{MIN}}$	Minimum Gain	$V_{BYP} = 6V$	2		4	V/V
e_N	Input Noise Voltage	Gain set to maximum			30	nV/ $\sqrt{Hz}$
BW	Bandwidth	Gain set to maximum, −3dB point	30			MHz
ΔV_{OS}	Maximum Gain and Minimum Gain AGC Amp Output Offset Voltage Difference	$V_{BYP} = 2.6V$ for maximum gain $V_{BYP} = 5.0V$ for minimum gain			700	mV
$V_{BYP_{MAX}}$	Max Voltage at BYP Pin at Minimum Gain	$V_{(D_{IN+}-D_{IN-})} = 1.6V$, $V_{AGC} = 3.0V$		6.0	6.7	V
V_{OP}	Maximum Output Voltage Swing	Set by V_{AGC}	3			V_{P-P}
I_{OD}	OUT+ to OUT− Pin Current	No DC path to GND, See Note 3	±3.2			mA
R_O	Output Resistance			18	32	Ω
C_O	Output Capacitance			12		pF
V_{IP} V_{AGC}	$(D_{IN+} - D_{IN-})$ Input Voltage Swing VS AGC Input Level	$30mV_{P-P} \leq V_{(IN+-IN-)} \leq 550mV_{P-P}$, $0.5V_{P-P} \leq V_{(D_{IN+}-D_{IN-})} \leq 1.5V_{P-P}$	0.37	0.48	0.56	V_{P-P}/V
V_{IP}	$(D_{IN+} - D_{IN-})$ Input Voltage Swing Variation	$30mV_{P-P} < V_{(IN+-IN-)} < 550mV_{P-P}$, AGC Fixed, over supply and temp.			+8	%
t_D	Gain Decay Time	See Figure 1a; $V_{IN} = 300mV_{P-P}$ then >150mV$_{P-P}$ at 2.5MHz, V_{OUT} to 90% of final value.		50		µs
t_A	Gain Attack Time	See Figure 1b; from Write to Read transition to V_{OUT} at 110% of final value, $V_{IN} = 400mV_{P-P}$ @ 2.5MHz		4		µs
I_{AGCfc}	Fast AGC Capacitor Charge Current	$V_{(D_{IN+}-D_{IN-})} = 1.6V$, $V_{AGC} = 3.0V$	1.3	1.5	2.0	mA
I_{AGCsc}	Slow AGC Capacitor Charge Current	$V_{(D_{IN+}-D_{IN-})} = 1.6V$, Vary V_{AGC} until slow discharge begins	0.14	0.17	0.22	mA
	Fast to Slow Attack Switchover Point	$\frac{V_{(D_{IN+}-D_{IN-})}}{V_{(D_{IN+}-D_{IN-})}\ \text{Final}}$		1.25		-
I_{AGCD}	AGC Capacitor Discharge Current	$V_{(D_{IN+}-D_{IN-})} = 0.0V$ Read Mode		4.5		µA
		Hold Mode	−0.2		+0.2	µA
CMRR	CMRR (Input Referred)	$V_{IN+} = V_{IN-} = 100mV_{P-P}$ @ 5MHz, gain at maximum	40			dB
PSRR	PSRR (Input Referred)	V_{CC} or $V_{DD} = 100mV_{P-P}$ @ 5MHz, gain at maximum	30			dB
TREC	Write to Read Recovery Time. Includes AGC Settling	$V_{(IN+-IN-)} = 100mV_{P-P}$ @ 2.5MHz	1.2	2	10	µs

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of $V_{CC}=5V\pm10\%$, $V_{DD}=12V\pm10\%$, $0°C\leq T_A\leq 70°C$, IN+ and IN− AC coupled, OUT+ and OUT− differentially loaded with >600Ω and each side loaded with <10pF to GND, $C_{BYP}=2000pF$, OUT+ and OUT− AC coupled to D_{IN+} and D_{IN-} respectively, $V_{AGC}=2.2V$ unless otherwise specified. (See Note 2.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 4	MAX	UNITS
READ MODE CHARACTERISICS (Continued)						
Hysteresis Comparator						
V_{IP}	Input Signal Range				1.5	V_{P-P}
R_{ID}	Differential Input Resistance	$V_{(D_{IN+}-D_{IN-})}=100mV_{P-P}$ @ 2.5MHz	5		15	kΩ
C_{ID}	Differential Input Capacitance	$V_{(D_{IN+}-D_{IN-})}=100mV_{P-P}$ @ 2.5MHz			6.0	pF
Z_{IC}	Common Mode Input Impedance	(both sides)		2.0		kΩ
V_{IO}	Comparator Offset Voltage	HYS pin at −0.5V, ≤1.5kΩ across D_{IN+}, D_{IN-}		5		mV
V_{HYSP} V_{HYS}	Peak Hysteresis Voltage vs HYS pin voltage (input referred)	$1V<V_{HYS}<3V$	0.16	0.21	0.25	V/V
I_I	HYS Pin Input Current	$1V<V_{HYS}<3V$	0		−20	μA
I_O	LEVEL Pin Max Output Current		3			mA
R_O	LEVEL Pin Output Resistance	$I_{LEVEL}=0.5mA$		180		Ω
V_{OL}	D_{OUT} Pin Output Low Voltage	$T_A=70°C$	$V_{DD}-4.0$		$V_{DD}-2.5$	V
V_{OH}	D_{OUT} Pin Output High Voltage	$T_A=70°C$	$V_{DD}-2.2$		$V_{DD}-1.5$	V
V_{LEVEL} $V_{D_{IN}}$	Level Pin Output Voltage vs $V_{(D_{IN+}-D_{IN-})}$	$0.6<\lvert V_{(D_{IN+}-D_{IN-})}\rvert<1.3V_{P-P}$ 10kΩ from level pin to GND	1.5		2.5	V/V_{P-P}
Active Differentiator						
V_{IP}	Input Signal Range				1.5	V_{P-P}
R_{ID}	Differential Input Resistance	$V_{(C_{IN+}-C_{IN-})}=100mV_{P-P}$ @ 2.5MHz	5		11	kΩ
C_{ID}	Differential Input Capacitance	$V_{(C_{IN+}-C_{IN-})}=100mV_{P-P}$ @ 2.5MHz			6	pF
Z_{IC}	Common Mode Input Impedance	(both sides)		2.0		kΩ
I_{OD}	D_{IF+} to D_{IF-} Pin Current	Differentiator Imped must be set so as not to clip signal at this current level	±1.3			mA
V_{IO}	Comparator Offset Voltage	D_{IF+}, D_{IF-} AC Coupled		5		mV
V_{OL}	C_{OUT} Pin Output Low Voltage	$0\leq I_{OH}\leq 0.5mA$		$V_{DD}-3$		V
V_{PO}	C_{OUT} Pin Output Pulse Voltage	$0\leq I_{OH}\leq 0.5mA$		0.4		V
PW_0	C_{OUT} Pin Output Pulse Width	$0\leq I_{OH}\leq 0.5mA$		30		ns
A_V	Voltage Gain From $C_{IN\pm}$ to $D_{IF\pm}$	$R_{(D_{IF+}\text{ to }D_{IF-})}=2k\Omega$	1.7		2.2	V/V
Undervoltage Detector (ML4042 Only)						
$V_{CC\,TH+}$	V_{CC} Fault Threshold +	$\overline{V_{FLT}}$ transition from low to high	3.8	4.2	4.5	V
$V_{CC\,TH-}$	V_{CC} Fault Threshold −	$\overline{V_{FLT}}$ transition from high to low	3.8	4.1	4.5	V
$V_{DD\,TH+}$	V_{DD} Fault Threshold +	$\overline{V_{FLT}}$ transition from low to high	9.6	10.2	10.8	V
$V_{DD\,TH-}$	V_{DD} Fault Threshold −	$\overline{V_{FLT}}$ transition from high to low	9.6	10.0	10.8	V
V_{OL}	Output Low Voltage ($\overline{V_{FLT}}$)	$I_{OL}=1.6mA$			0.4	V
V_{OH}	Output High Voltage ($\overline{V_{FLT}}$)	$I_{OH}=-400\mu A$	2.7			V

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ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of $V_{CC} = 5V \pm 10\%$, $V_{DD} = 12V \pm 10\%$, $0°C \leq T_A \leq 70°C$, $V_{(C_{IN+}-C_{IN-})} = V_{(D_{IN+}-D_{IN-})} = 1.0V_{P-P}$ AC coupled sine wave at 2.5MHz, $R_{D_{IF}} = 100\Omega$, $C_{D_{IF}} = 65pF$, $V_{HYS} = 1.8V$, $C_{OS} = 60pF$, 4kΩ to V_{CC} and 10pF to GND on pin $\overline{RD}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 4	MAX	UNITS
Output Data Characteristics (Refer to Figure 2)						
t_{D1}	D-Flip-Flop Set Up Time	Min delay from $V_{(D_{IN+}-D_{IN-})}$ exceeding threshold to $V_{(D_{IF+}-D_{IF-})}$ reaching a peak	0			ns
t_{D3}	Propagation Delay				110	ns
t_{D5}	Output Data Pulse Width Variation	(See Note 5) C_{OS} = 60pF, T_A = 25°C	40	50	65	ns
t_{D3}-t_{D4}	Logic Skew (Pulse Pairing)				1	ns
t_R	Output Rise Time	$V_{OH} = 2.4V$			18	ns
t_F	Output Fall Time	$V_{OL} = 0.4V$			14	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: AGC amplifier output current may be increased as in Figure 4.

Note 4: Typicals are parametric norm at 25°C.

Note 5: t_{D5} = 830 (C_{OS}), 50pF < C_{OS} < 150pF

FUNCTIONAL DESCRIPTION

Operating Modes

The ML4041, ML4042 has three definitive operation modes which are: Read mode, Write mode and Hold mode. These modes are defined by input pins $\overline{HOLD}$ and R/$\overline{W}$ as shown in Table 1. Read mode, the mode used normally for pulse detection, is assumed in the following sections unless otherwise noted.

AGC Amplifier Section

The purpose of the AGC amplifier is to provide a constant read signal level for both the level and slope detectors. Full differential processing of the read signal is used to minimize noise and distortion in the analog signal. A wide gain range is required due to large signal variation when moving the recording head from an inside to outside data track or variations in media.

The differential output voltage level V_{OUT} from the AGC amp is determined by voltage V_{AGC} present at pin AGC. V_{OUT} is full wave rectified and compared against V_{AGC} to create charge/discharge current for capacitor C_{BYP} connected at pin BYP. Voltage V_{BYP} across C_{BYP} controls the gain in the AGC amplifier.

Two distinct values of I_{BYP} are possible which determine a fast and slow AGC gain response attack rate. When V_{OUT} is more than 125% of the set level a high value of I_{BYP} is sourced which provides a fast AGC attack rate. When V_{OUT} is within 100% to 125% of the set level a reduced value of I_{BYP} is sourced which provides a slower attack rate. The fast-slow gain response attack rates provides for an initial quick system response and then minimum zero crossing distortion of the analog signal once the gain is within working range. V_{AGC} should be set so that the differential input voltage $V_{D_{IN}}$ into the level comparator is $1V_{P-P}$ at nominal Read signal conditions. The AGC amp section gain is given by:

$$\frac{A_{V2}}{A_{V1}} = \exp \frac{V_{BYP2} - V_{BYP1}}{5.8 \times V_T}$$

Where: A_{V1}, A_{V2} are initial and final amplifier gain values corresponding to initial and final V_{BYP} values.

$V_T = (KT)/Q = 26mV$ at room temperature.

The AGC amp's differential inputs must be AC coupled to the read amplifier (ML117, ML501, etc.) differential outputs. Similarly, AC coupling must be used at the AGC amp outputs.

AGC Amp During Write Mode — When the ML4041, ML4042 is put into write mode, the AGC amp's input impedance is lowered to allow a faster dampening of the Write to Read transient from the head pre-amp. The AGC gain is also set to maximum gain so that fast AGC attack will occur when changing back to the Read mode. Internal device timing is controlled so that settling occurs prior to Read mode activation. Minimal value input coupling capacitors should be chosen to reduce settling time, however, bandwidth requirements also need to be considered.

AGC Amp During Hold Mode— During the Hold mode, the charge/discharge current driving pin BYP is internally disconnected. AGC compensation capacitor C_{AGC} will then hold the present gain setting. The amplitude of V_{OUT} will therefore not affect the AGC gain and gain will remain constant.

Hold mode is used so that AGC gain will not be adjusted when embedded servo information is read. This prevents loosing the pulse peak amplitude information needed during position decoding, or creating additional gain settling time when again reading data. Embedded servo pulses are normally taken at outputs D_{IF-} and D_{IF+}, as shown in the typical application.

External Filter Network
Filtering for the level and slope detectors can be performed with a single filter or two separate filters. If separate filters are used, care must be used to insure that time delays are matched. A multi-pole Bessell filter is recommended due to the group delay and linear phase characteristics.

Level Detector
The full wave rectified V_{OUT} is buffered and available at pin LEVEL. The level detector uses a hysteresis comparator to compare the processed read signal amplitude against a reference voltage derived from voltage V_{LEVEL} output from pin LEVEL. Using V_{LEVEL} provides a feed-forward function that allows valid level detection to be performed prior to AGC amp gain settling. The level detector hysteresis value is set in a way that will only allow relatively large read pulse peaks (negative or positive) to be detected.

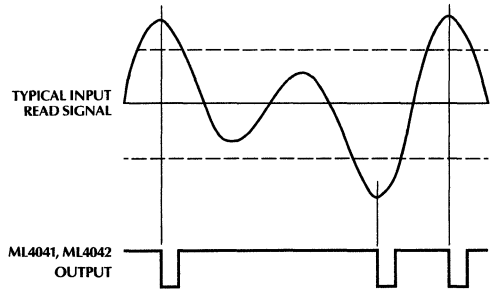
Slope Detector
The slope detector uses an external reactive component network to produce a voltage signal proportional to the differential of the read signal. By using a hysteresis comparator to detect zero slope of the read signal, the time occurrence of positive or negative read pulse peak values can be determined.

An external reactive network, shown in the Typical Application, is used between the D_{IF+} and D_{IF-} pins to provide the differential function given by:

$$A_V = \frac{-2000Cs}{LCs^2 + (R + 92)Cs + 1}$$

Where: C = External capacitor (20pF to 150pF)
L = External inductor
R = External resistor
$s = j\omega = j2\pi f$

Output Logic
The output logic provides a negative TTL pulse at pin $\overline{RD}$ which begins at the peak of a valid read pulse, as shown below.

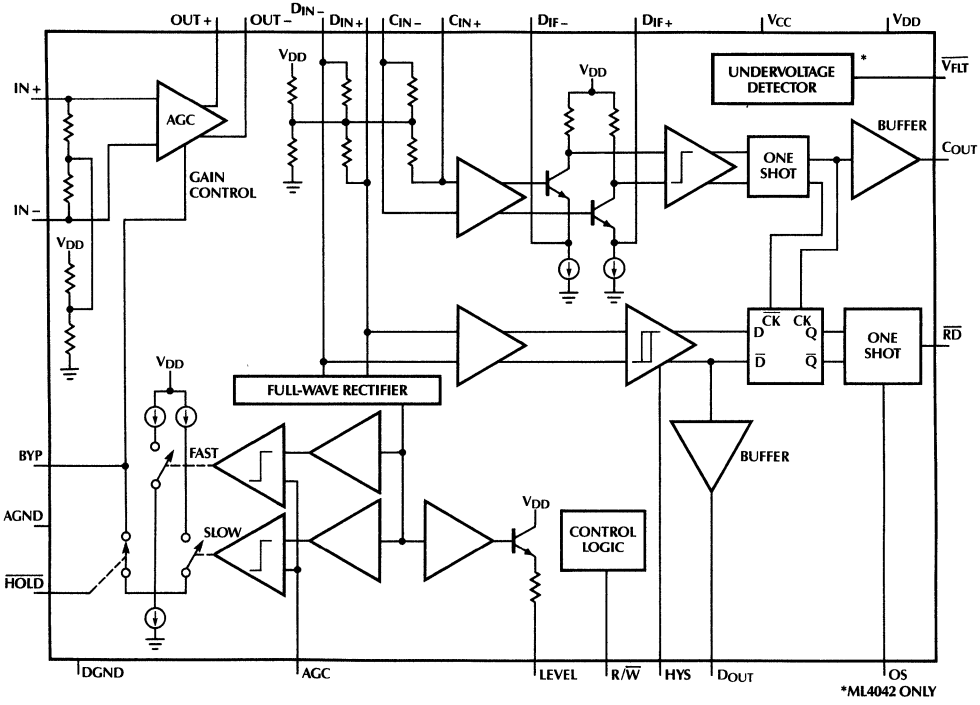


Pin R/$\overline{W}$ must be high for the output logic to be active. The key element in the output logic is the D flip-flop. The flip-flop is clocked by the slope detector at the time of a zero crossing, which loads data from level detector. The flip-flop inputs only change state when the level detector detects a peak amplitude of a polarity opposite to the previous valid peak. Thus, through the output logic the slope detector determines output timing and the level detector determines pulse validity.

Layout Considerations
As with any high gain, wide bandwidth analog circuitry, care needs to be exercised in PC layout. Power supply and ground lines should be bypassed and well isolated from other circuitry. A ground plane is recommended, as is keeping analog lines short and well balanced to prevent interaction with nearby circuitry in the disk drive.

5

BLOCK DIAGRAM



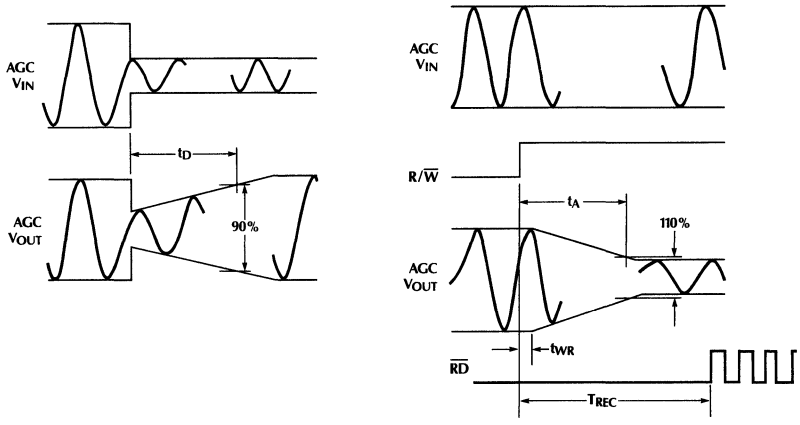


Figure 1. AGC Timing Diagram

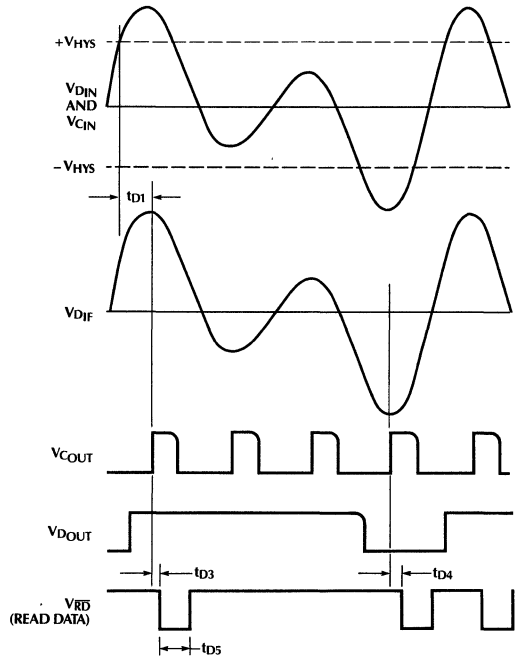


Figure 2. Output Logic Timing Diagram

TYPICAL APPLICATIONS

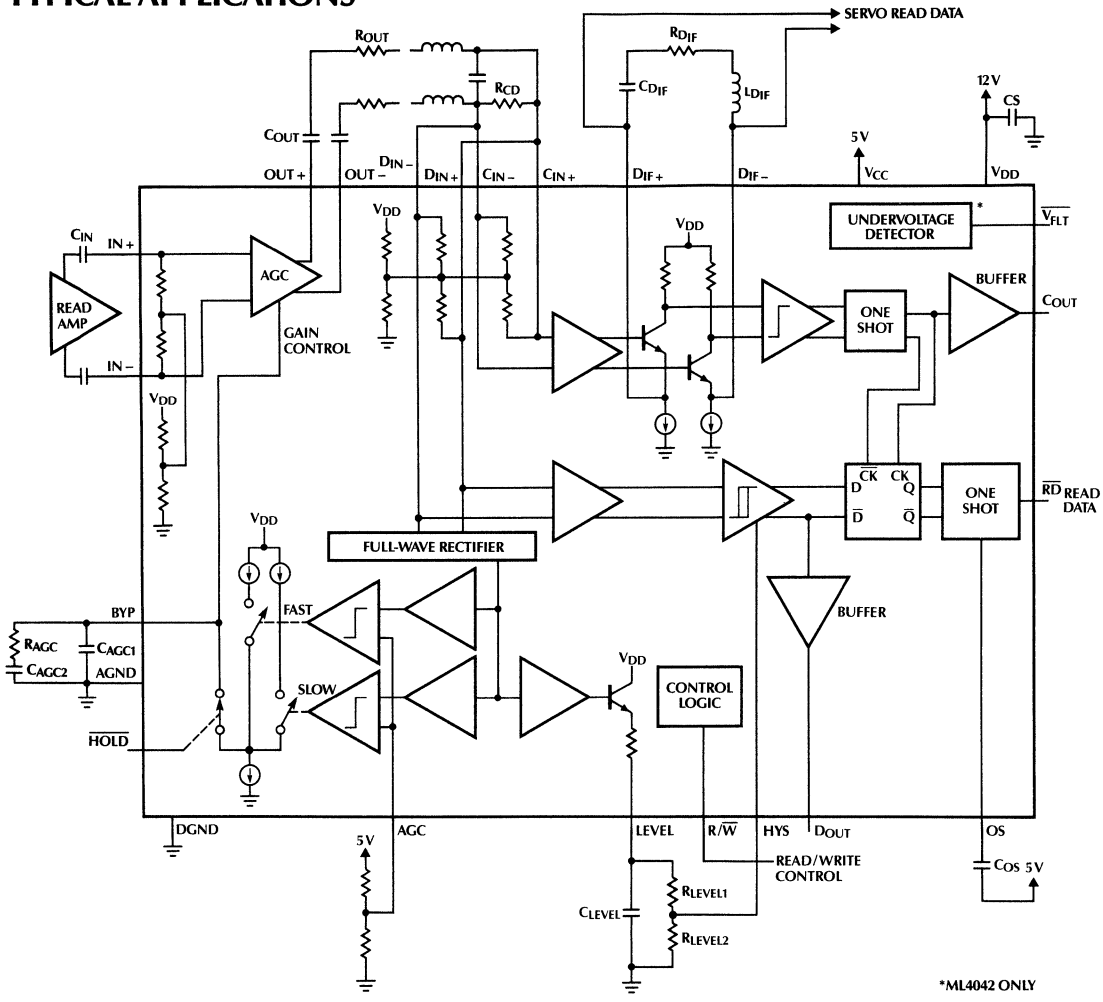


Figure 3. Typical Application Diagram

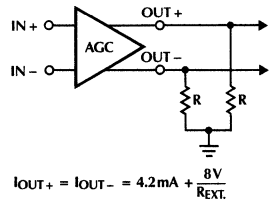


Figure 4. Modification of AGC Amplifier Output to Drive Low Impedance Filters

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML4041CP	0°C to +70°C	MOLDED DIP (P24)
ML4041CQ	0°C to +70°C	MOLDED PCC (Q28)
ML4041CS	0°C to +70°C	MOLDED SOIC (S24)
ML4042CP	0°C to +70°C	MOLDED DIP (P28)
ML4042CQ	0°C to +70°C	MOLDED PCC (Q28)
ML4042CS	0°C to +70°C	MOLDED SOIC (S28)

Micro Linear

ML4401

Servo Demodulator

GENERAL DESCRIPTION

The ML4401 provides all of the analog circuitry necessary for the demodulation of di-bit servo signal information in Winchester disk drives. It interfaces to the servo head preamp and provides quadrature position signal outputs for the servo controller circuitry.

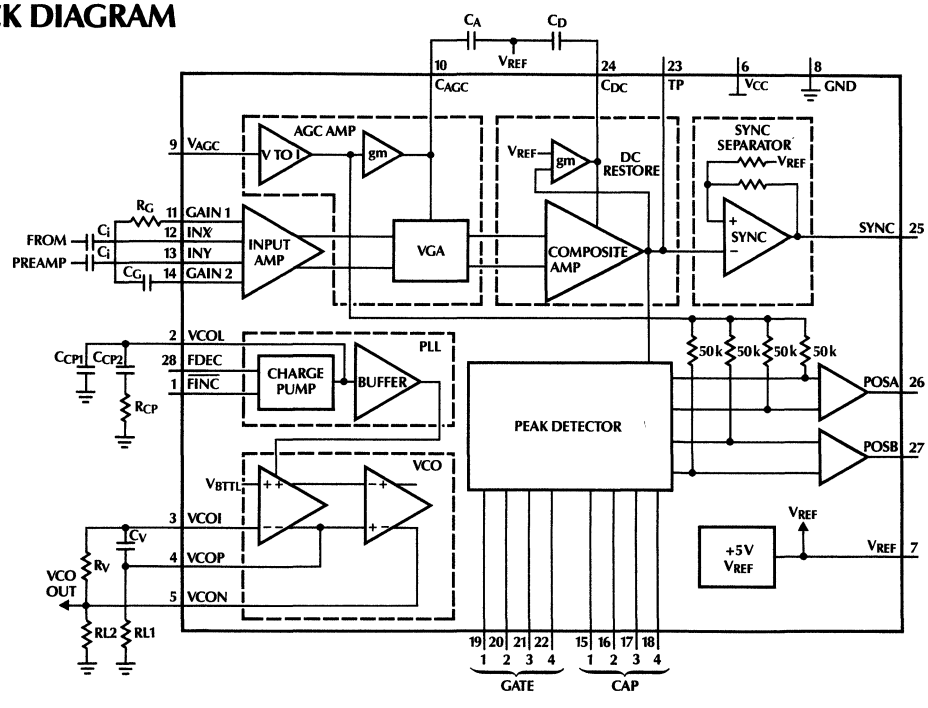
The ML4401 includes a high-performance 592-type input amplifier and differential AGC circuit. External logic is designed to meet the needs of the particular servo system utilizing the VCO and Charge Pump to create a PLL time base for Peak Detector gating. The SYNC output provides servo channel timing information for the logic.

The ML4401 when combined with the ML4402, ML4406/07/08 Servo Driver, the ML4403, ML4413 Servo Controller and the ML4404 Trajectory Generator, provides a flexible closed-loop servo control system.

FEATURES

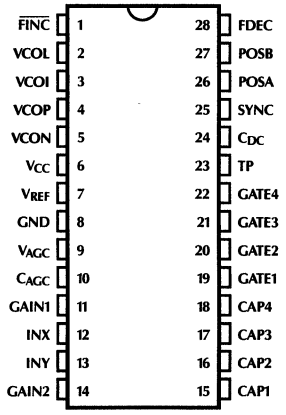
- Combines all analog di-bit demodulation circuitry
- Logic track-type switching can be used to minimize demodulator offset
- Exponential AGC characteristics makes AGC settling independent of input step size
- External loop compensation of analog blocks
- External digital circuitry allows flexible pattern format
- On-chip band gap voltage reference eliminates external referencing
- Operates from 12V power supply
- Compatible with Micro Linear's ML4403, ML4413 Servo Controller, ML4402, ML4406/07/08 Servo Driver and ML4404 Trajectory Generator

BLOCK DIAGRAM



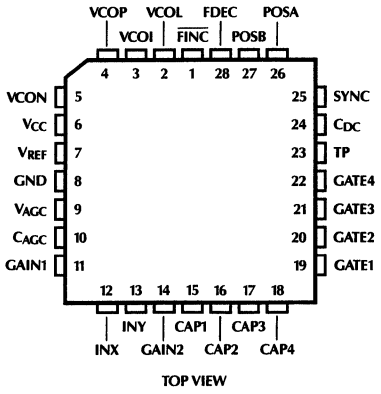
PIN CONNECTIONS

ML4401 28-Pin DIP
(Prototypes Only)



TOP VIEW

ML4401 28-Pin PCC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	$\overline{\text{FINC}}$	Charge pump frequency increment input (TTL).
2	VCOL	PLL loop compensation terminal.
3	VCOI	VCO high impedance input.
4	VCOP	VCO positive output, for capacitive feedback to VCOI.
5	VCON	VCO negative output, drives resistance feedback to VCOI, also provides ECL output on ML4401 and TTL output on ML4411.
6	V_{CC}	+12 V supply.
7	V_{REF}	Voltage reference output (+5 V).
8	GND	Ground.
9	V_{AGC}	AGC gain reference voltage input.
10	C_{AGC}	External capacitor terminal to set AGC response.
11	GAIN1	Input amplifier gain adjusting RC terminal 1.
12	INX	X input into input amplifier.
13	INY	Y input into input amplifier.
14	GAIN2	Input amplifier gain adjusting RC terminal 2.
15	CAP1	Peak detector 1 capacitor terminal.
16	CAP2	Peak detector 2 capacitor terminal.
17	CAP3	Peak detector 3 capacitor terminal.
18	CAP4	Peak detector 4 capacitor terminal.
19	GATE1	Peak detector 1 gate input (TTL) high enabled, low disabled.
20	GATE2	Peak detector 2 gate input (TTL) high enabled, low disabled.
21	GATE3	Peak detector 3 gate input (TTL) high enabled, low disabled.
22	GATE4	Peak detector 4 gate input (TTL) high enabled, low disabled.
23	TP	Composite test point, normally left unconnected.
24	C_{DC}	External capacitor terminal to set DC restore response.
25	SYNC	SYNC pulse output (TTL).
26	POSA	Position output A.
27	POSB	Position output B.
28	FDEC	Charge pump frequency decrement input (TTL).

5

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Power Supply Voltage, V_{CC} 14V
Input Voltages:
GAIN1, GAIN2 ..... -0.3 to 8V
C_{AGC} ..... -0.3 to 7.0V
V_{AGC} ..... -0.3 to 5.3V
CAP1, CAP2, CAP3, CAP4 ..... 3.0 to 10V
GATE1, GATE2, GATE3, GATE4, VCOP ..... -0.3 to 7.5V
INX, INY, VCON, VCOI, $\overline{FINC}$, FDEC, C_{DC} ..... -0.3 to V_{CC} +0.3V
Θ_{JA} for 28-Pin Plastic Dip ..... ≤60°C/Watt
Θ_{JA} for 28-Pin PLCC ..... 60°C/Watt
Storage Temperature Range ..... -65°C to 150°C
Junction Tempearture (T_{JMAX}) ..... 150°C
Lead Temperature (Soldering, 10sec) ..... 260°C

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
Supply Voltage (V_{CC}) ..... 12 V_{DC} ±10%
Input Coupling Capacitance (Ci) 0.01μF
Input Amp Gain Capacitance (C_G) 0.047μF
Input Amp Gain Resistance (R_G) 1kΩ
AGC Response Compensation Capacitance (C_A) 0.082μF
Composite DC Restore Capacitance (C_D) 0.01μF
PLL Compensation Components:
C_{CP1} 0.1μF
C_{CP2} 1μF
R_{CP} 910Ω
PLL Gain Components:
R_V 1000Ω
RL1, RL2 ..... 1000Ω
Peak Detector Capacitance (CAP1 thru CAP4) 270pF
SYNC Output Pull-Up Resistor (to 5V) 3.3k
On track Base-to-Peak Voltage at pin TP 1.75V
V_{GA} Gain Control Voltage (at pin C_{AGC}) 0.65

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of T_A = 0 to 70° C, V_{CC} = 10.8 to 13.2 V, V_{VAGC} = 5.0 V, and external components as recommended above, unless otherwise specified (See Note 1.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
Power Supply						
I_{CC}	Supply Current	V_{CC} = 12V		81	110	mA
TTL Inputs $\overline{FINC}$, FDEC, GATE1, GATE2, GATE3, GATE4						
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	V_{IH} = 2.4V	-1		30	μA
I_{IL}	Low Level Input Current	V_{IL} = 0.4V	-20		1	μA
SYNC Output (TTL Open Collector) See Note 3						
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6mA	0	0.3	0.5	V
V_{THR}	Positive going input threshold			V_{REF} +0.9		V
V_{THF}	Negative going input threshold			V_{REF}		V
t_{PD} ±	Propagation Delay Rising, Falling	RL = 2k, C_L = 15pF		50		ns
VCOP Output ML4401 (T_A = 25° C)						
V_{OH}	High Level Output Voltage	RL = 1kΩ	4.0	4.3	4.6	V
V_{OL}	Low Level Output Voltage	RL = 1kΩ	2.9	3.2	3.5	V
VCOP Output ML4411						
V_{OH}	High Level Output Voltage	I_{OH} = 50μA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6mA	0		0.5	V
VCO and Charge Pump Section						
I_{BIAS}	V_{COI} Input Bias Current		0	25	50	μA
I_{CH}, I_{DIS}	V_{COL} Charge and Discharge Current		495	660	825	μA
I_{CH}/I_{DIS}	V_{COL} Charge/Discharge Ratio		0.95	1.00	1.05	μA/μA
I_{OFF}	V_{COL} OFF State Current	$\overline{FINC}$ = 2.0 FDEC = 0.8	0	25	50	nA

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of $T_A = 0$ to 70° C, $V_{CC} = 10.8$ to 13.2 V, $V_{AGC} = 5.0$ V, and external components as recommended above, unless specified (See Note 1.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
VCO and Charge Pump Section (Continued)						
F_{MAX}	MAX VCO Frequency to Maintain + and − 5% Control Range Note 4		30			MHz
F_{VCO}	VCO Frequency Range Note 4	T_A = 25°C, V_{CC} = 12, V_{COL} = 6V C_V = 1000pF, R_V = 604Ω	9.7	10.0	10.3	MHz
K_{VCO}	VCO Voltage to Frequency Factor			2		%/V
Input AMP, AGC AMP, and DC Restore						
R_{IN}	INX, INY Differential Input Resistance		7.5	10	20	kΩ
$I_{GAIN1, 2}$	GAIN1, GAIN2 Bias Current		0.66	1.0	1.20	mA
I_{BIAS}	V_{AGC} Input Bias Current		0	5	20	μA
G_{MAGC}	AGC Transconductance at C_{AGC}			370		μMHOS
R_{AGC}	Control Range of AGC Loop to Regulate Composite Amplitude to within 2% of Nominal			7/1		V/V
BW	Bandwidth from INX, INY to Composite Note 4		10	15		MHz
GMDCR	DC Restore Transconductance			200		μMHOS
Peak Detectors						
I_{CH}	Charge Current		12.7			mA
I_{DIS}	Discharge Current	T_A = 25° C	25	45	60	μA
T_{CDIS}	Tempco of I_{DIS}			−0.17		μA/° C
Voltage Reference						
V_{REF}	Reference Voltage	T_A = 25° C	4.85	5.10	5.35	V
TC	Tempco			50		ppm/° C
R_{OUT}	Load Regulation			2		mV/mA
PSRR	Line Regulation			10		mV/V
I_{SINK}	Maximum SINK Current		0.8			mA
Output Amplifiers (POSA, POSB)						
V_{OS}	Input Offset	V_{CAP}1-4 = 6V	−10	0	10	mV
A_V	Gain		1.23	1.28	1.33	V/V
A_{VA}/A_{VB}	Gain Tracking		−3	0	+3	%
V_{OUT}	Output Voltage Range		1.0		9.5	V
I_{SRC}	Output Source Current		5			mA
I_{SNK}	Output Sink Current		2			mA
SR	Slew Rate			2.5		V/μs
BW	3 dB Gain Bandwidth			3		MHz

Note 1: 0° C to 70° C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Typicals are parametric norm at 25° C.

Note 3: Pin 25 is an open collector output which should not exceed 7 volts in the high state.

Note 4: This parameter is guaranteed but not 100% tested and is not used in outgoing quality level calculations.

APPLICATION HINTS

Using a nominal on-track servo signal, amplitude adjustment should be made as follows:

1. Set composite signal amplitude, measured at pin TP, by adjusting voltage at pin V_{AGC} (approximately 4.7 volts). The composite signal should be set to 1.75 volts base to peak of an on-track position pulse (an off-track position pulse will be about 3.5 volts maximum).
2. Adjust Rg so that the VGA is in mid-range. This is determined by measuring the voltage at pin C_{AGC}; it should be approximately 0.9 volts. C_{AGC} voltage will vary approximately ±0.5 volts over the AGC range.

FUNCTIONAL DESCRIPTION

Input Amplifier

The input amplifier is equivalent to a wide-band 592 type video amplifier and provides amplification and buffering to the AGC circuitry. The Inputs INX and INY, which must be AC coupled, accept the composite analog signal from the servo head differential preamplifier. Internal input termination resistors eliminate the need for external bias resistors. Prefiltering of the signal is normaly desired to eliminate unwanted components. External components R_G and C_G determine the input amplifier's low frequency cutoff and gain as follows:

$$FC = \frac{1}{2\pi\ (R_G + 60\Omega)\ C_G} \qquad A_V = \frac{1700}{R_G + 60\Omega}$$

Where: C_G = External series capacitance between pins GAIN1 and GAIN2

R_G = External series resistance between pins GAIN1 and GAIN2

Automatic Gain Control (AGC)

The purpose of the AGC loop is to maintain a constant peak output voltage level at outputs POSA and POSB. This peak level is established by the reference voltage applied to pin V_{AGC}.

$$V_{P\text{-}P\ (Composite)} = K1 \times V_{AGC} + K2$$

Where: K1 = 0.65

K2 = 0.41V

In this closed-loop system, the peak detector output voltages are fed back and combined with the V_{AGC} voltage to provide a gain control current. The current controls the variable gain amplifier (VGA) and is compensated at pin C_{AGC} to provide control of AGC bandwidth. The bandwidth of the entire AGC loop is determined by:

$$BW = \frac{K\ V_{VAGC}}{2\pi\ C_A}$$

Where: K = 4.3×10^{-4}

V_{VAGC} = External reference voltage at pin V_{AGC}

C_A = External capacitance at pin C_{AGC}

Optimum system stability is achieved by deriving V_{VAGC} from the V_{REF} output using a resistive divider.

Composite Amplifier

The input amplifier and AGC circuit of the ML4401 operate in a differential signal mode to provide good common mode and power supply rejection. The composite amplifier converts the differential signal into a buffered single-ended signal for the peak detector circuitry. The DC base line of the composite signal is equal to V_{REF} . The bandwidth of the DC restore function is controlled by capacitor C_D at pin C_{DC} with the following relationship:

$$BW = \frac{gm}{2\pi\ C_D}$$

Where: gm = 1/5 kΩ

C_D = External capacitance at pin C_{DC}

The composite signal is available at pin TP and is normally left unconnected. For short circuit protection a 425Ω resistor is connected in series with pin TP internally.

Synchronization Pulse Separator

The SYNC pulse separator is a threshold comparator with hysteresis which passes pulses from the composite amplifier above a set threshold. It provides a buffered open collector TTL output. The SYNC output, when gated through an external one-shot, is used to control the external gate timing and PLL logic.

Peak Detector

The peak detector circuit captures the peak signal amplitude of the di-bit pulses. The gates are controlled by inputs GATE1 through GATE4. Timing is established by the external logic circuitry. The external peak detector capacitors are connected from pins CAP1 through CAP4 to ground. The peak detector discharge rate (set by CAP1-CAP4) determines the maximum track crossing rate during an access operation. The performance of this block can be enhanced by using the velocity output of the ML4403, ML4413 to create a velocity proportional discharge. The peak detector outputs are fed into internal differential amplifiers that calculate the track error signals and provide buffered outputs POSA and POSB as follows:

POSA = 1.25 (CAP1 – CAP2) + V_{REF}

POSB = 1.25 (CAP3 – CAP4) + V_{REF}

Voltage Controlled Oscillator and Charge Pump

The VCO and external phase compare logic provide a time base for peak detector gate sychronization. Inputs $\overline{FINC}$ and FDEC provide increment and decrement signals to the charge pump for changing the oscillator frequency. The $\overline{FINC}$ and FDEC inputs gate the charge pump for the duration of the pulse width. The RC timing network formed by C_V and R_V at pins VCOI, VCON, and VCOP control the oscillators center frequency. (See Typical Performance Characteristics)

R_V should be greater than 330Ω. Too low of a value will result in excessive power dissipation. RL1, RL2 and R_V should be approximately equal, although the values of RL1 and RL2 do not require accuracy.

The VCO output should only be taken from pin VCON. Charge pump capacitor C_{CP1} is connected from pin VCOL to ground. Components R_{CP} and C_{CP2} are also connected in series from pin VCOL to ground to provide VCO loop compensation.

Internal Voltage Reference

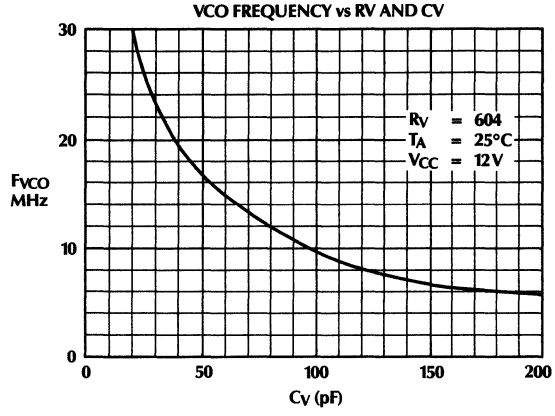
V_{REF} is an internal band-gap voltage reference. It is buffered and available at pin V_{REF} and is used by the ML4402, ML4403, ML4404 and other chips requiring a 5 volt reference.

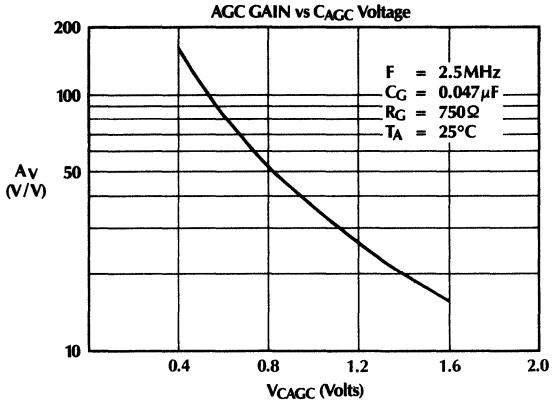
External Logic

The external logic provided by the user typically has a complexity of about 150 to 300 equivalent gates. Complexity and architecture depends on the users di-bit pattern and control function.

Note: Stray capacitance should be considered in applying the above relationships when low capacitor values are used. Stray capacitance of the integrated circuit terminal is typically about 2 to 3 pF.

TYPICAL PERFORMANCE CHARACTERISTICS





ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML4401CP	0°C to +70°C	MOLDED DIP (P28)
ML4401YCQ	0°C to +70°C	MOLDED PCC (Q28)

Servo Driver

GENERAL DESCRIPTION

The ML4402 Servo Driver contains all of the control circuitry necessary to drive the head positioning actuator of a hard or rigid disk drive system. It receives the error signal generated from a servo controller circuit, such as the ML4403, ML4413, and drives an external transistor bridge which controls the head positioning voice coil actuator. The ML4402 output control circuitry includes current sense inputs to provide closed-loop control of actual actuator current. By using an external power transistor bridge, flexible thermal and space management is allowed as well as transistor selection which enables a wide application range.

Included in the device is a unique disable function which permits interruption of actuator current. During a disable, the output control amplifiers are shut down which cuts off all current to the external transistor bridge. Disable can be activated by a logic high into pin DIS or by the on-board low-voltage detector. Use of the low-voltage disable function prevents actuator response to a false error signal during a power failure. The low voltage detector can monitor up to two power supplies and has user definable low voltage trigger levels.

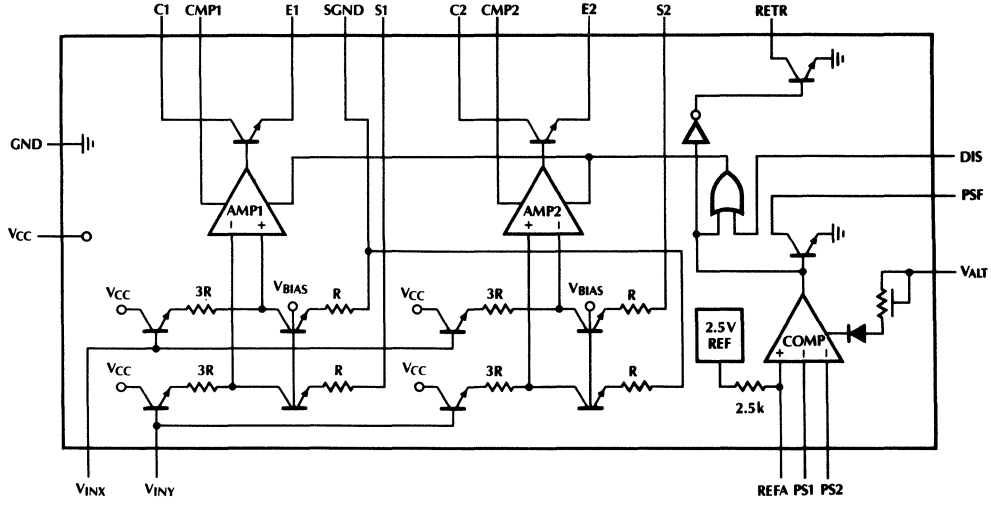
The ML4402, when combined with the ML4401/4431 Servo Demodulator, the ML4403, ML4413 Analog Servo Controller and the ML4404 Trajectory Generator, provides a flexible high-performance head positioning servo system.

FEATURES

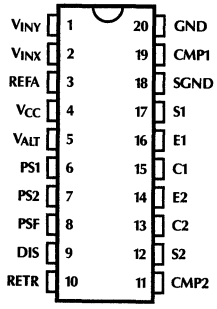
- Low differential input offset voltage
- Contains all control circuitry necessary to drive an external transistor bridge
- Differential amplifiers internally compensated
- Unique disable function interrupts actuator current
- Programmable dual supply low voltage detector
- Single +12V power supply
- Compatible with Micro Linear's ML4401/4431 Servo Demodulator, ML4403, ML4413 Servo Controller and ML4404 Trajectory Generator chips

The ML4402-1 and ML4402-2 differ in offset voltage at the differential error signal inputs which is a result of the manufacturing trim process.

BLOCK DIAGRAM

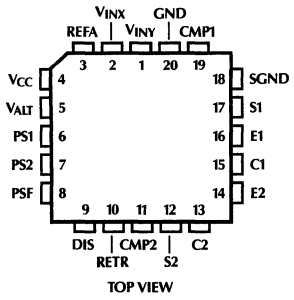


PIN CONNECTIONS



20-PIN DIP (Prototypes Only)

20-PIN PLCC Package



PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	V_{INY}	Inverting input for error voltage signal. Used as a reference voltage (analog ground) input when using a single ended output from the ML4403 Servo Controller. Obtained from the V_{REF} output of the ML4401 Servo Demodulator.
2	V_{INX}	Non-inverting input for error voltage signal. Used as the signal input pin when using a single ended output from the ML4403.
3	REFA	Reference pin for low voltage comparator.
4	V_{CC}	+12V power supply pin.
5	V_{ALT}	Optional +5V power supply pin to keep the PSF pin operating if V_{CC} fails. With V_{ALT} at +5V, the PSF pin will go low if V_{CC} goes to zero, or too low to operate the comparator.
6	PS1	Voltage input for low voltage comparator.
7	PS2	Voltage input for low voltage comparator.
8	PSF	Power supply failure indication, is an open collector output of comparator. Logic low indicates PS1 and/or PS2 voltage has gone below REFA.
9	DIS	Amplifier Disable pin. TTL input that disables both amplifiers with a logic high.
10	RETR	Return spring output, clamped open collector output, opposite logic polarity as pin PSF. Used to drive optional safety circuitry.
11	CMP2	Compensation node of AMP2 used to add additional compensation; the device is manufactured with approximately 27pF of internal compensation. Bandwidth Effects: $f = \frac{gm}{2\pi (C + 27\,pF)}$ Slew Rate Effects: $SR = \frac{20\mu A}{C + 27\,pF}$ Where: gm = 150μmhos C = External Compensation Capacitor C_{CMP1} or C_{CMP2}
12	S2	Current sense input for AMP2.
13	C2	Collector of output transistor of AMP2.
14	E2	Emitter of output transistor of AMP2.
15	C1	Collector of output transistor of AMP1.
16	E1	Emitter of output transistor of AMP1.
17	S1	Current sense input for AMP1.
18	SGND	Reference ground for S1, S2 feedback.
19	CMP1	Compensation node of AMP1, used to add additional compensation. The device is manufactured with approximately 27pF of internal compensation. Bandwidth and Slew Rate effects are the same as the CMP2 pin.
20	GND	Ground.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Power Supply Voltage (V_{CC}) 14V
Terminal Voltage Range
(V_{INX}, V_{INY}, V_{ALT}, PS1, PS2, REFA, DIS) ..... −0.3 to V_{CC} +0.3V
S1, S2 ..... 7V
Terminal Input Current (CMP1, CMP2) 0.1mA
Storage Temperature Range ..... −65°C to +150°C
Junction Temperature (T_J) ..... 125°C
Lead Temperature (Soldering, 10sec) ..... 260°C

OPERATING CONDITIONS

Supply Voltage
V_{CC} ..... 12V ± 10%
V_{ALT} ..... 5V ± 10%
Typical Component Values (Refer to Typical Application)
R_{OA} 470Ω
R_{OB} 240Ω
R_{OC} 150Ω
R_{OD} 0.5Ω

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of V_{CC} = 10.8V to 13.2V, V_{INY} = 5V, T_A = 0 to 70° C, and external components as shown above unless otherwise specified (See Note 1).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP NOTE 2	MAX	UNITS
Power Supply							
I_{CC}	V_{CC} Supply Current	Outputs unloaded, Pin REFA open			10	20	mA
I_{DD}	V_{ALT} Supply Current	V_{CC} = GND			150	500	µA
Amplifier Characteristics							
A_{V1}	Voltage Gain at Pin S1, $V_{S1}/(V_{INX}-V_{INY})$; Applies when $V_{INX} > V_{INY}$	V_{INX} = 5.1 and 6V V_{INY} = 5.0V		0.342	0.352	0.362	V/V
A_{V2}	Voltage Gain at Pin S2, $V_{S2}/(V_{INY}-V_{INX})$; Applies when $V_{INY} > V_{INX}$	V_{INX} = 4.9 and 4V V_{INY} = 5.0V		0.342	0.352	0.362	V/V
e_{AV}	Gain Linearity Error	$(A_{V1}-A_{V2}/0.5(A_{V1}+A_{V2})$		−2	0	2	%
V_{OS}	V_{INX}, V_{INY} Input Offset Voltage with Respect to Either Pin S1 or Pin S2	V_{OS} defined where A_{V1} or $A_{V2} > 0.16$ T_A = 25° C		−10		+10	mV
$V_{OS\ DIFF}$	Differential Input Offset	$V_{OS1}-V_{OS2}$ T_A = 25° C	ML4402-1 ML4402-2	−5 −10		+5 +10	mV
T_{CVOS}	Offset Voltage Tempco				15		µV/° C
V_S	Voltage Swing Range of Pin S1, S2 Above Ground	V_{S1}; V_{INX} = 6.7V V_{S2}; V_{INX} = 3.3V			0.5	0.65	V
I_{VR}	Input Voltage Range into V_{INX} and V_{INY}			3.3		10	V
I_{IB1}	Input Bias Current, V_{INX} and V_{INY}			0	10	75	µA
I_{IB2}	Input Bias Current, Pin S1 or S2 (sourcing)	V_{S1}, V_{S2} = GND		−1.6	−1.2	−0.8	mA
PSRR	Power Supply Rejection				60		dB
CMRR	Common Mode Rejection Ratio				80		dB
GBP	Gain Bandwidth Product	$C_{CMP1,\ 2}$ = 0			0.83		MHz
SR	Slew Rate	$C_{CMP1,\ 2}$ = 0			0.74		V/µS
Output Transistor Characteristics							
I_{OUT}	Output Current; I_{C1}, I_{E1}, I_{C2}, I_{E2}	$V_{INX}-V_{INY}$ = +1V V_{C1}, V_{C2} = 3V; V_{E1}, V_{E2} = 0.7V		50	100		mA

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of V_{CC} = 10.8V to 13.2V, V_{INY} = 5V, T_A = 0 to 70° C, and external components as shown unless otherwise specified (See Note 1).

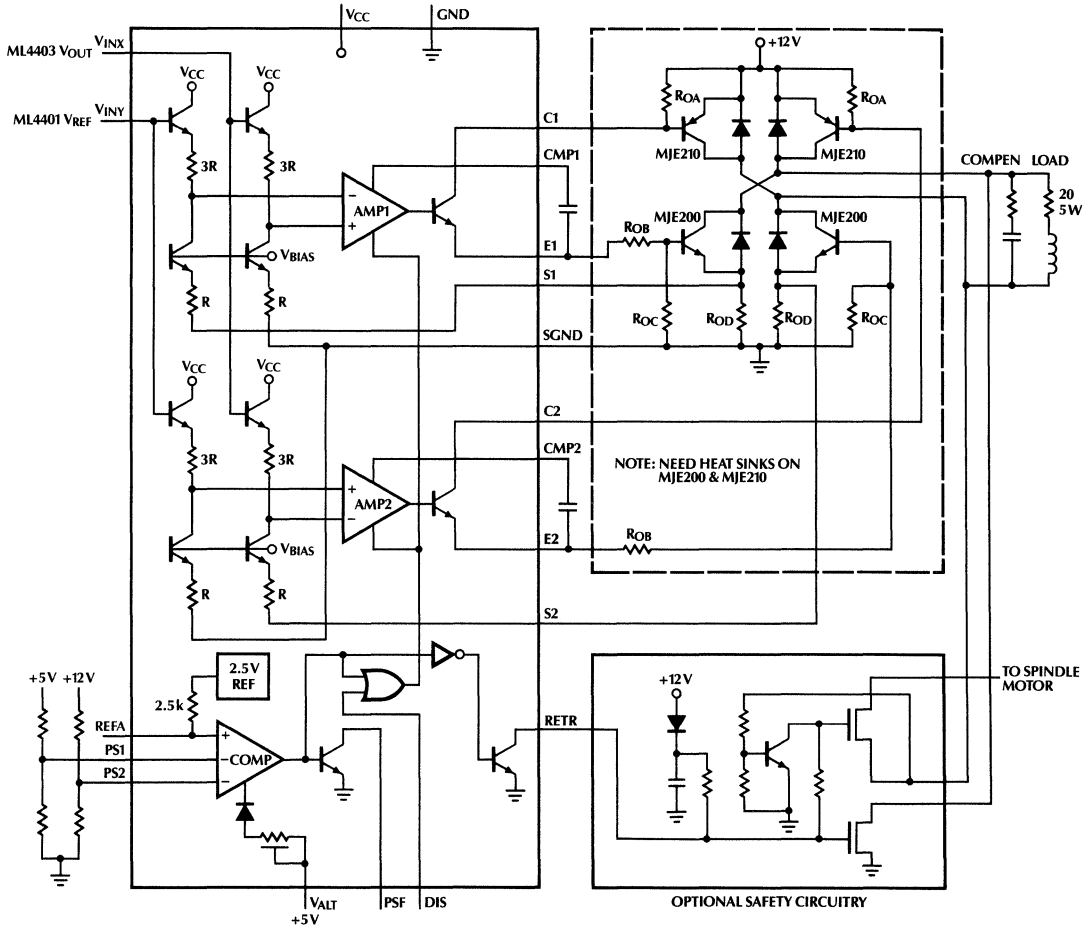
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
Internal Voltage Reference (V_{REF})						
PS_{MIN}	Minimum Allowable V_{CC} Voltage	Where V_{REF} > 2.48V	4.75			V
V_{REF}	V_{REF} Voltage	T_J = 25° C	2.44	2.55	2.66	V
T_{REG}	V_{REF} Thermal Stability	Over Specified Range		50		ppm/° C
R_{REF}	R_{REF} Resistance	(Internal Resistor from V_{REF} to Pin REFA)		2.55		kΩ
Comparator						
V_{OS}	Input Offset Voltage, any Two Inputs		−30	5	30	mV
I_{IN}	Input Bias Current		−0.5	−0.1	0	µA
V_{OL}	PSF Logic 0 Voltage	I_{OL} = 1.6mA	0	0.2	0.4	V
V_{OL}	RETR Logic 0 Voltage	I_{SINK} = 3mA	0	0.5	1	V
I_{OH}	PSF Logic 1 Leakage Current	V_{PSF} = 5V	−10	0.2	10	µA
I_{OH}	RETR Logic 1 Leakage Current	V_{RETR} = 2V	−20	0.05	20	µA
Amplifier Disable Section						
V_{IH}	DIS Logic High Voltage		2.0			V
I_{IH}	DIS Logic High Current	V_{IH} = 2.4V	−20		20	µA
V_{IL}	DIS Logic Low Voltage				0.8	V
I_{IL}	DIS Logic Low Current	V_{IL} = 0.4V	−20		20	µA

Note 1: 0° C to 70° C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 2: Typicals are parametric norm at 25° C.

5

TYPICAL APPLICATION DIAGRAM



ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE	COMMENTS
ML4402-1CP	0°C to +70°C	MOLDED DIP (P20)	Input Offset = ±5mV
ML4402-1CQ	0°C to +70°C	MOLDED PCC (Q20)	Input Offset = ±5mV
ML4402-2CP	0°C to +70°C	MOLDED DIP (P20)	Input Offset = ±10mV
ML4402-2CQ	0°C to +70°C	MOLDED PCC (Q20)	Input Offset = ±10mV

Micro Linear

ML4403, ML4413

Servo Controller

GENERAL DESCRIPTION

The ML4403/4413 Servo Controller provides analog circuitry used in high performance trajectory and position control system for disk drive transducer heads. As a part of a head positioning servo system, this bipolar monolithic chip is designed to accept quadrature position signals and generate a servo error signal. While designed for minimum track access time, the ML4403/4413 supports a wide range of system designs.

Trajectory control functions include a track crossing detector, a velocity signal generator, and a velocity event detector. System stability and short settling time is insured by the interpolator function, which generates a ramp signal used to smooth the external position DAC output.

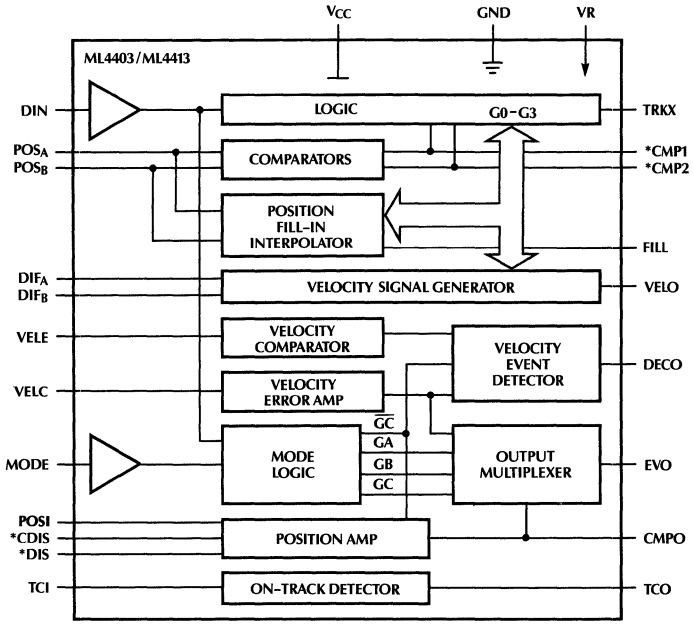
Position control is provided by a signal error amplifier within the device. When used with the ML4401/4431 Servo Position Demodulator, the track selection is performed by ML4401/4431 peak detector timing. This selection method eliminates track to track voltage offset problems and allows minimum track spacing. The ML4413 has a discharge function that enables zeroing of the external error amplifier compensation. This feature further reduces position settling time. An on-board on-track detector is provided which is used as a safety alarm by the controller for an off-track condition.

The ML4403/4413 Servo Controller, when combined with the ML4401 Servo Demodulator, the ML4402, ML4406/07/08 Servo Driver and the ML4404 Trajectory Generator provides a flexible closed-loop servo control system.

FEATURES

- Interpolate function smooths trajectory curve
- Flexible architecture allows user defined loop response
- Provides minimum track access time and maximum track density
- Single +12V power supply
- Compatible with ML4401 Servo Demodulator, ML4402, ML4406/07/08 Servo Driver and ML4404 Trajectory Generator

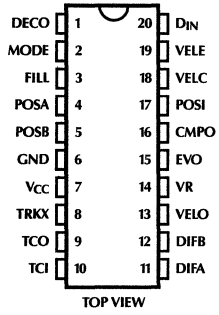
BLOCK DIAGRAM



* PINS WITH THE * IN FRONT ARE USED ON THE ML4413 ONLY.

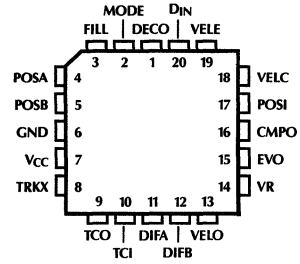
PIN CONNECTIONS

ML4403 20-PIN DIP (Prototypes only)



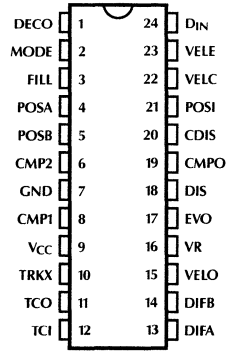
TOP VIEW

ML4403 20-PIN PLCC



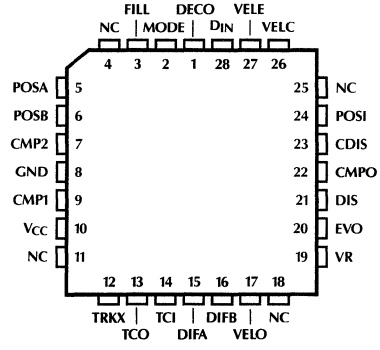
TOP VIEW

ML4413 24-PIN SKINNY DIP (Prototypes only)



TOP VIEW

ML4413 28-PIN PLCC



TOP VIEW

NC = NO CONNECTION

PIN DESCRIPTION

ML4403 DIP and PLCC	ML4413 DIP	ML4413 PLCC	NAME	FUNCTION
1	1	1	DECO	Digital output from the velocity event detector. In application, this output goes to a logic high when the actual actuator velocity reaches the trajectory curve. It remains high through the "braking" or negative acceleration. This pin goes low when velocity is zero and remains low during actuator acceleration. This pin is only allowed to go high during access mode. This output is open collector and requires an external pull-up resistor.
2	2	2	MODE	Digital input used to select Hold mode (low level) or Access mode (high level).
3	3	3	FILL	Analog output that provides a sawtooth waveform that, when summed with stair-step output of the external DAC, provides a smooth trajectory curve. Refer to Figure 3.
4	4	5	POSA	Analog input for quadrature position signals from demodulator (ML4401/
5	5	6	POSB	4431). Low pass prefiltering is recommended to eliminate peak detector ripple and external noise.
6	7	8	GND	Device ground connection.
	8	9	CMP1	Digital outputs that can be used for various control and count schemes. These
	6	7	CMP2	pins are only available on the ML4413. Timing is shown in Figure 3. These outputs are open collector outputs with an internal pull-up resistor tied to +5V.
7	9	10	V_{CC}	+12V power supply connection.
8	10	12	TRKX	Digital output that provides a logic transition at each track crossing which is defined as the point midway between two tracks. Refer to Figure 3. This output is open collector with an internal pull-up resistor tied to +5V.
9	11	13	TCO	Digital output from the on-track detector. Used in Hold mode, this pin goes to logic high when the position signal exceeds an established window. This output is open collector with an internal pull-up resistor tied to +5V.
10	12	14	TCI	Analog input into the on-track detector. The input is normally derived from the position signal.
11	13	15	DIFA	Analog inputs for differentiated quadrature position signals. These inputs are
12	14	16	DIFB	used to generate the velocity signal at output VELO.
13	15	17	VELO	Analog output that provides a continuous velocity (tachometer) signal by time multiplexing/inverting the DIFA, DIFB input signals.
14	16	19	VR	Reference voltage input. This value should typically be +5V, which is obtainable from the V_{REF} output of ML4401/4431.
15	17	20	E_{VO}	Multiplexed analog output of both velocity error and position error signals. This output is used as the input for the servo actuator driving circuity such as the ML4402.
	18	21	DIS	Digital input that, upon a logic high, electrically shorts pins CDIS and CMPO in order to keep the compensator capacitor discharged after entering hold mode. This pin and function is only available on ML4413. This function is used to reduce settling time when entering the Hold mode. Unlike pins MODE and DIN which float to logic high, this pin floats to logic low when left unconnected.
16	19	22	CMPO	Analog connection point for position compensation circuitry that is connected between this pin and POSI.
	20	23	C_{DIS}	Used to discharge external position compensation as shown in Figure 5. This pin is only available on ML4413. On the ML4403 this pin is internally connected to pin POSI.
17	21	24	POSI	Analog input for position control amplifier.
18	22	26	VELC	Analog input into velocity comparator. The velocity comparator trigger level is VR and is used for velocity event detection as described below.
19	23	27	VELE	Analog input for velocity error signal generated off-chip, referenced to VR.
20	24	28	D_{IN}	Digital input that controls actuator direction during Seek mode. This input affects the waveforms of outputs F_{ILL}, V_{ELO}, and E_{VO}. Refer to Figure 3.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied. (All voltages referenced to GND.)

Power Supply Voltage, V_{CC} 14V
Terminal Voltage Range
VR ..... −0.3 to 7.0V
POSI ..... −0.3 to V_R +0.3V
DIN, POSA, POSB, DIFA, DIFB, VELE, VELC, MODE, DIS, TCI ..... −0.3 to V_{CC} +0.3V
Storage Temperature Range ..... −65°C to +150°C
Junction Temperature ..... +125°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
Supply Voltage (V_{CC}) ..... 12V ± 10%

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of V_{CC} = 10.8 to 13.2V, and V_R = 5.0V, unless otherwise specified. (See Note 1.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
Power Supply						
I_{CC}	V_{CC} Supply Current	Outputs unloaded		38	60	mA
DIGITAL INPUT/OUTPUT CHARACTERISTICS						
Inputs D_{IN} and Mode						
V_{IH}	Logic High Voltage		2.0			V
I_{IH}	Logic High Current	V_{IH} = 2.4V	−40	1	40	µA
V_{IL}	Logic Low Voltage				0.8	V
I_{IL}	Logic Low Current	V_{IL} = 0.4V	−100	−50	0	µA
Input DIS (ML4413 Only)						
V_{IH}	Logic High Voltage		2.0			V
I_{IH}	Logic High Current	V_{IH} = 2.4V	0	180	250	µA
V_{IL}	Logic Low Voltage				0.65	V
Outputs TCO and TRKX						
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA	0		0.4	V
V_{OH}	Output High Voltage	I_{OH} − 50µA	2.4			V
t_{PD}	Propagation Delay	C_L = 15pF		200		ns
V_{TH}	Track Comparator Window	+ and − relative to VR	235	257	270	mV
Outputs CMP1 and CMP2 (ML4413 Only)						
V_{OL}	Output Low Voltage	I_{OL} = 0.4mA	0		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −50µA	2.4			V
Output DECO						
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA	0		0.5	V

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of V_{CC} = 10.8 to 13.2 V, and V_R = 5.0 V, unless otherwise specified. (See Note 1.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
ANALOG INPUT/OUTPUT CHARACTERISTICS						
Outputs Fill, VELO, COMPO, and EVO						
V_{OS1}	Input Offset Voltage EVO, FILL			2		mV
V_{OS2}	Input Offset Voltage COMPO		−5		5	mV
V_{OS3}	VELO Input Offset Voltage Tracking Between 4 Multiplex States	Variation in output level in 4 multiplex states with DIFA = DIFB = 5 V	−10		10	mV
SR_1	Slew Rate FILL			4		V/μs
SR_2	Slew Rate COMPO, VELO, EVO			1		V/μs
V_{OUT}	Output Range All		1.0		9.0	V
I_{SRC1}	Source Current COMP, VELO, FILL		3			mA
I_{SRC2}	Source Current EVO		1.5			mA
I_{SNK1}	Sink Current FILL		0.25			mA
I_{SNK2}	Sink Current EVO, VELE		2			mA
I_{SNK3}	Sink Current COMPO		4			mA
Operational Amplifiers						
V_{OS}	Input Offset Voltage			2		mV
t_C	Average Temperature Coeff of Input Offset Voltage			20		μV/°C
I_{OS}	Input Offset Current			10		nA
I_B	Input Bias Current			100		nA
AV_{OL}	Open Loop Gain			200		V/mV
GBW	Gain Bandwidth Product			1		MHz
POSA, POSB Comparators						
V_{OS}	Input Offset Voltage			2		mV
V_{HYS}	Hysteresis			±500		mV
t_C	Average Temp Coeff of Input Offset Voltage			20		μV/°C
I_{OS}	Input Offset Current			50		nA
I_B	Input Bias Current			500		nA
A_V	Voltage Gain			200		V/mV
Pd	Response Time			500		ns

Note 1: 0°C to +70°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 2: Typicals are parametric norm at 25°C.

FUNCTIONAL DESCRIPTION

Power Supply and Reference Requirements

The ML4403/4413 operates from a single 12V ± 10% power supply, a 5.0V reference is required at pin VR which is available from pin V_{REF} on the ML4401/4431. VR serves as a system reference or "analog ground".

Modes of Operation

The device has two modes of operation, Access and Hold mode, which are controlled by pin MODE. To accomplish this, pin MODE controls the output multiplexer that selects either the velocity or position error signal.

Access Mode

The head actuator servo system uses Access mode to move the recording head(s) from one data track to another. Access mode circuitry within the ML4403/4413 includes analog functions necessary to measure and control head actuator velocity. The head velocity is controlled in a fashion that provides for a fast track-to-track movement and minimum settling time, which results in minimum track access time.

Actuator Trajectory

Similar to racing to the next stop sign, the fastest way to move from one data track to the next is through maximum acceleration and maximum braking (negative acceleration). In a disk drive the acceleration, either positive or negative, is governed by maximum available actuator current. To do this in a controllable manner and land on the target track, an achievable "braking curve" or trajectory function is first defined. At the beginning of Access mode, maximum acceleration is applied until the head velocity reaches this defined braking curve. Following the velocity profile of the trajectory curve, controlled braking stops the head on the target track.

Unlike acceleration, velocity and distance are accurately measurable and therefore controllable parameters. The trajectory function, as shown in Figure 2, is therefore expressed as velocity (track crossing rate) vs. distance (tracks to go). The desirable constant positive and negative acceleration will result in the expression of velocity as a function of the square root of distance. Therefore generation of the trajectory curve, velocity vs. distance, requires a non-linear function.

Actuator Trajectory Generation

At the start of a track access cycle, initial tracks-to-go count is supplied by the microprocessor. As the head moves, the count is decremented by the ML4403/4413 track crossing detector. To generate the analog "desired velocity" signal required for braking control, the tracks-to-go count (distance variable) is converted through a DAC (Digital to Analog Converter) with a non-linear square function included either before or after the conversion. One common approach used to obtain this non-linear function is to pre-process the tracks-to-go count (or multiple thereof) in the microprocessor. This can be performed algorithmically by the use of a look up table.

An alternate method, as shown in the typical application of Figure 5 places the non-linear function after the DAC conversion. The tracks-to-go count is maintained by a simple discrete down-counter that is initialized by the microprocessor. To eliminate the DAC steps and provide a smooth distance signal, the DAC output is summed with the ML4403/4413's FILL output in the external summing amplifier shown. The FILL output generates a sawtooth wave, as shown in Figure 3. This distance signal is then passed through the non-linear trajectory generator which generates the "desired velocity" signal used during braking. Generating a smooth trajectory curve reduces electrical/mechanical system oscillation and target track settling time.

Inductance-caused actuator lag can also create a target track overshoot problem. The trajectory curve generator, as indicated, can be designed to allow the microprocessor to modify the non-linear function in a way to account for this lag. Refer to Figure 2. The amount of lag will depend on duration of braking. Braking duration can be correlated against acceleration duration which is indicated by the timing of pin DECO.

The track crossing detector, which drives the trajectory position counter (see Figure 5), is generated with external logic. The input comparators have a fixed amount of internal hysteresis to provide noise immunity and media dropouts. The CMP1 and CMP2 outputs on the ML4413 can be used to perform more sophisticated sequential track crossing detection schemes. This can further reduce the detector's susceptability to media dropouts.

Hold Mode

At the end of an Access cycle, the head is stopped, or nearly so, on the target track. Hold mode is then selected to maintain accurate head positioning on that track. In this mode, the compensator output (CMPO) is multiplexed into the error amplifier output (EVO).

Track Selection

Track position is held by maintaining a zero value of the position input signal, with respect to VR. However, to allow selection of one of four track types and maintain error signal polarity, selection of POSA, POSB, or their inverse needs to be possible. Commonly this selection process is accomplished with an analog multiplexer-inverter matrix. The problem inherent with this approach is the track-to-track offset differences, caused by the amplifier input offset differences within the matrix.

The track selection scheme adopted by the ML4401/4431 and ML4403/4413 combination performs the multiplexing within the ML4401/4431. The selection/inversion operation is performed with the external support logic of the ML4401/4431 by changing the peak detector sample timing. This method eliminates the offset problems and allows a higher track density.

Position Amplifier and Compensator Zeroing

During track following mode (mode low), the compensator amplifier acts as an integrator which nulls out the position error. The timing of the transition between access mode and track follow is critical to minimize settling time. The velocity at which this transition occurs can be externally set by resistor RCMP (see Figure 5). During seek mode, the large compensator capacitor (CCMP) is discharged through an internal switch, so that the integrating loop sees no initial charge at the beginning of track follow mode. This can reduce settling time by several milliseconds.

The ML4413 provides a further enhancement of this feature. The switch can remain closed after the beginning of the seek-to-track follow transition by holding pin DIS high. In this way, the time at which the logic switches modes, and the time that integration begins can be controlled independently, and further settling time reduction can be acheived.

On-Track Detector

The on board on-track detector is a window comparator that provides a digital alarm of an off-track condition. This feature is useful as a safety to prevent data transfer during an off-track condition that may occur during track settling or mechanical jarring.

Velocity Control

As a necessary element of velocity control, a velocity signal is generated and is output at pin VELO. To accomplish this, the quadrature position signals are first differentiated through external RC networks and then input into pins DIFA and DIFB. The ML4403/4413 then time multiplexes these differentiated signals to obtain a continous velocity signal that is output at pin VELO. It is important to note that the trajectory generator shown in Figure 5 generates a "desired velocity" signal positive with respect to VR, and that VELO creates a negative signal with respect VR. This allows the use of a simple external resistor bridge to create the velocity error signal.

The summing function can be modified, as illustrated, by the action of pin DECO when the actual velocity reaches the trajectory curve. Modification can also be made just prior to that time with the "optional trajectory overshoot compensation" circuit, shown in Figure 5, that prevents overshoot due to actuator motor inductance.

Inductance-caused actuator lag can also create a track overshoot problem. The trajectory curve generator, as indicated, can be designed to allow the microprocessor to modify the non-linear function in a way to account for this lag as shown in Figure 2. The amount of lag will depend on duration of braking. Braking duration can be correlated against acceleration duration which is indicated by the timing of pin DECO.

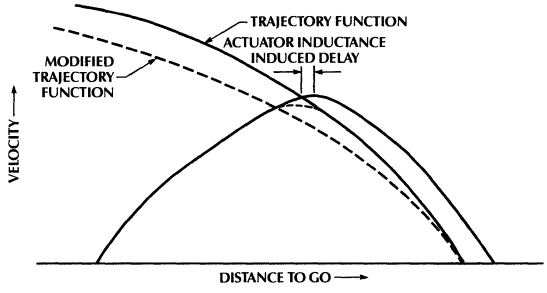


Figure 2.

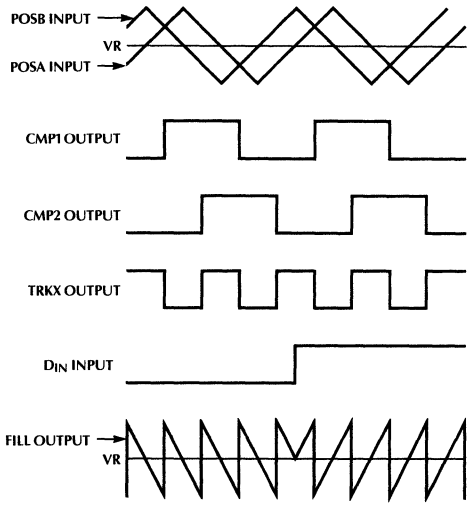
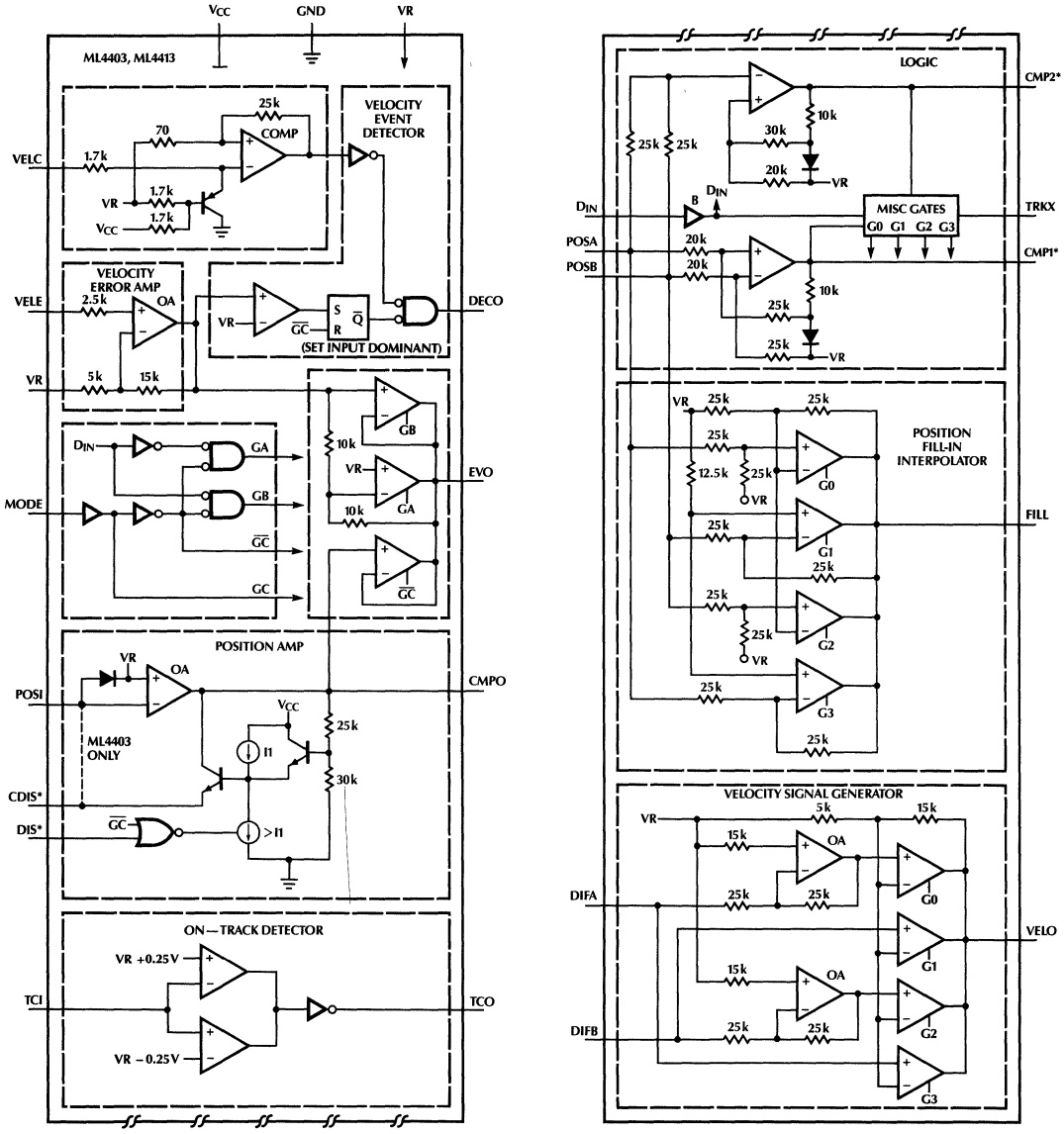


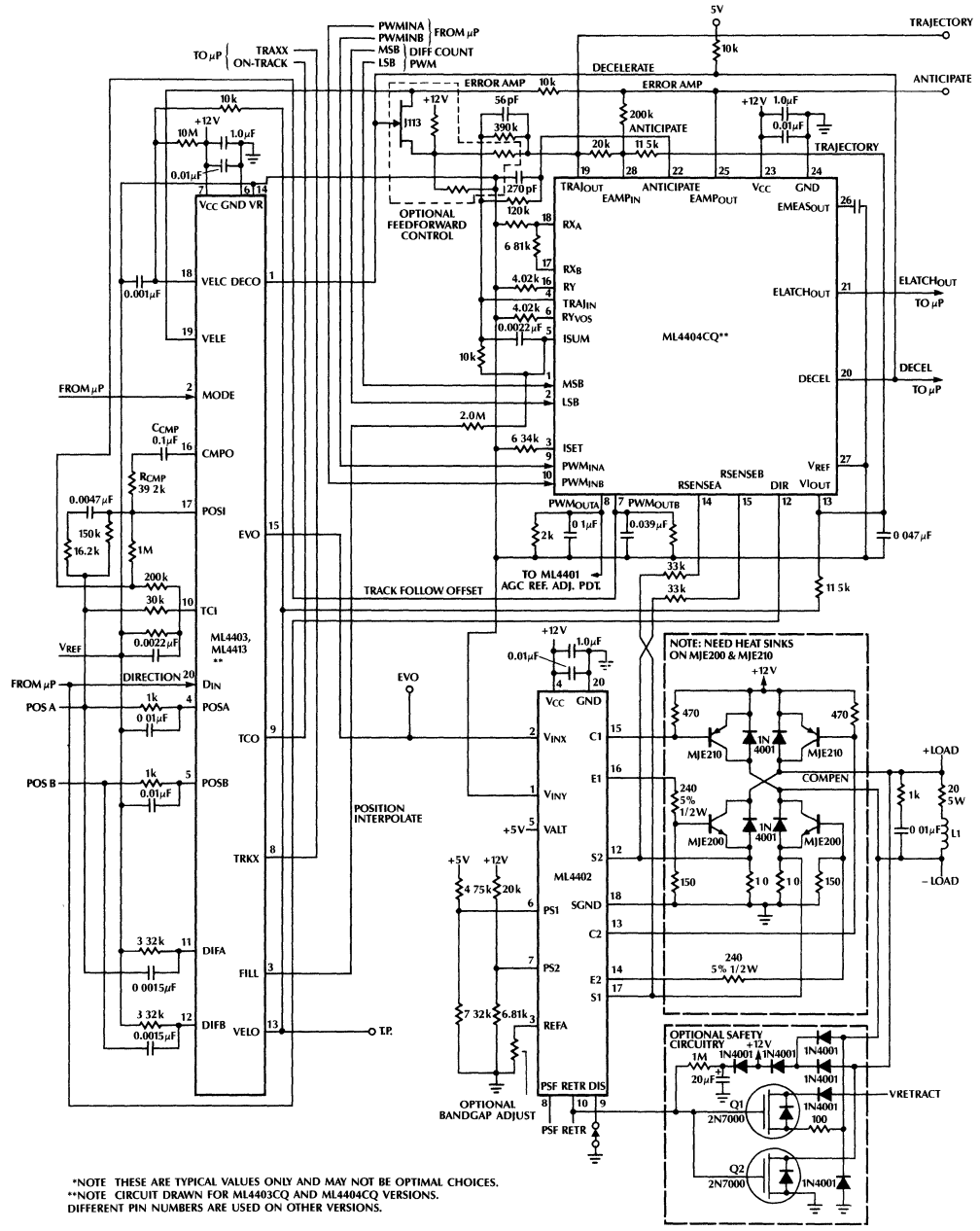
Figure 3.



*NOTE: THESE PINS ONLY AVAILABLE ON ML4413

Detailed Function of Block Diagram of the ML4403/13

Figure 4.



*NOTE THESE ARE TYPICAL VALUES ONLY AND MAY NOT BE OPTIMAL CHOICES.
**NOTE CIRCUIT DRAWN FOR ML4403CQ AND ML4404CQ VERSIONS.
DIFFERENT PIN NUMBERS ARE USED ON OTHER VERSIONS.

Figure 5. Connecting the ML4403 to the ML4404 Trajectory Generator and the ML4402 Servo Driver

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML4403CP	0°C to +70°C	MOLDED DIP (P20)
ML4403CQ	0°C to +70°C	MOLDED PCC (Q20)
ML4413CP	0°C to +70°C	MOLDED DIP (P24)
ML4413CQ	0°C to +70°C	MOLDED PCC (Q28)

Micro Linear

ML4404

Trajectory Generator

GENERAL DESCRIPTION

The ML4404 Trajectory Generator provides the trajectory function for time optimal head positioning systems. The ML4404 receives position and velocity information from a servo controller, such as the ML4403, and generates the desired time optimal velocity trajectory. Desired Velocity is then compared with the actual velocity to create the error signal used by the servo controller.

An anticipate function is included to compensate for phase shift error caused by actuator inductance. Another feature on the ML4404 is an error measure output which averages the velocity error during deceleration, so that the control system can monitor and adjust the necessary transducer gain for minimum access time.

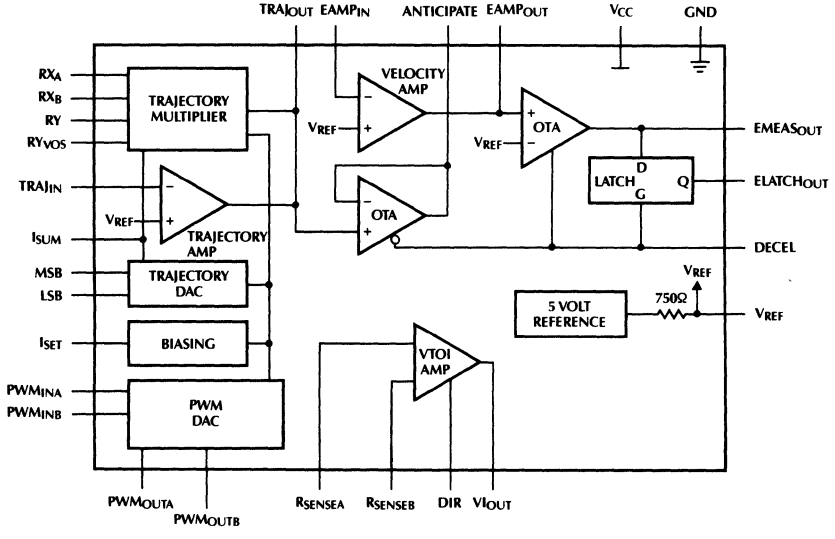
The servo system usually requires accurate analog voltages to be set through software control. This is easily accomplished with a duty cycle to current translator function on the ML4404. By controlling the duty cycle of a TTL line, a processor can set an analog voltage on the translator output. These translators are fully independent blocks which can be used anywhere in the control system.

FEATURES

- Flexible architecture allows a user defined trajectory function
- Anticipate function compensates for phase delay caused by actuator inductance
- Feed forward function improves system stability
- Uncommitted PWM to current translators allow an analog voltage to be set with microprocessor control
- Single +12V power supply
- Compatible with Micro Linear's ML4401, ML4431 Demodulator, ML4402, ML4406/07/08 Driver, and ML4403, ML4413 Controller

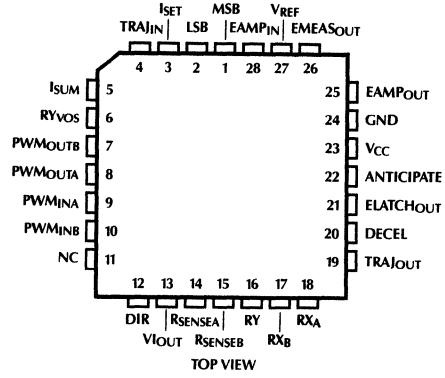
5

BLOCK DIAGRAM



PIN CONNECTIONS

ML4404 28-Pin PLCC



PIN DESCRIPTION

PIN # ML4404	NAME	FUNCTION
1	MSB	Pulse width modulated (PWM) DAC TTL input (active low). The DAC output current is the position input to the trajectory generator. The MSB/LSB ratio is 8/1. The duty cycle of these two TTL inputs are controlled by a processor to form an 8-bit PWM DAC. The 3 higher order bits are modulated into the MSB.
2	LSB	Pulse width modulated (PWM) DAC TTL input (active low). The 5 lower order bits are modulated into the LSB input.
3	I_{SET}	A resistor (R_{SET}) from this pin to V_{REF} sets the internal bias levels. $I_{BIAS} = 3V/R_{SET}$. The nominal value should be between 0.25 and 0.5 mA.
4	$TRAJ_{IN}$	The trajectory generator input. This node is connected through an external filter to the sum of the PWM DAC output and the multiplier output.
5	I_{SUM}	The trajectory DAC output which is summed with the multiplier output feedback. An external RC filter network from this pin to $TRAJ_{IN}$ smooths out PWM DAC ripple.
6	RY_{VOS}	Nulls out the offset of the trajectory curve at the origin. A resistor equal to RY is connected from this pin to V_{REF}. This pin is available only on the ML4404.
7	PWM_{OUTB}	PWM to current translator output.
8	PWM_{OUTA}	PWM to current translator output.
9	PWM_{INA}	TTL input for the PWM to current translator. This converter translates a signal's duty cycle to an analog voltage.
10	PWM_{INB}	TTL input for the PWM to current translator. This converter translates a signal's duty cycle to an analog voltage.
11	NC	No Connection.
12	DIR	TTL direction input from the processor. Controls the polarity of the V/I converter output.

PIN DESCRIPTION (Continued)

PIN # ML4404	NAME	FUNCTION
13	VI_{OUT}	The V/I converter output. This circuit block monitors the differential voltage across the sense resistors of an actuator driver (such as the ML4402) and converts it to a bidirectional current whose scale factor is set by two external resistors. This current can be used to compensate for a noise reducing low pass filter in the output of the velocity transducer so that there is no net phase shift in the velocity signal.
14	R_{SENSEA}	A gain setting resistor is connected from this input to the sense resistor on the bridge driver.
15	R_{SENSEB}	A gain setting resistor is connected from this input to the sense resistor on the bridge driver.
16	RY	A resistor (RY) is connected from this pin to V_{REF}. RY and RX set the second order term of the trajectory curve.
17	RX_B	A resistor (RX) is connected between RX_A AND RX_B to set the second order term in the trajectory curve.
18	RX_A	A resistor (RX) is connected between RX_A and RX_B to set the second order term in the trajectory curve. An additional resistor (RK3) can be connected from RX_A to either the trajectory output ($TRAJ_{OUT}$) or to V_{REF} to set the third order term.
19	$TRAJ_{OUT}$	The trajectory output. This voltage relative to V_{REF} is proportional to the desired velocity. A resistor and capacitor from this pin to $TRAJ_{IN}$ sets the first order term and the loop compensation.
20	DECEL	Decelerate mode TTL input from the servo controller (such as the ML4403). When low (during accelerate) the anticipate output becomes a voltage follower, the error measure output is a high impedance, and the error sign is latched. When high (during deceleration) anticipate goes to high impedance, error measure integrates the velocity error, and the error sign latch is transparent.
21	$ELATCH_{OUT}$	The latched sign of the access loop error during deceleration. This TTL output can be used by the processor to adjust the velocity transducer gain to match that required by the mechanical system.
22	ANTICIPATE	Modifies the trajectory curve during acceleration and the accelerate to decelerate transition. This accounts for the time delay error caused by the actuator inductance.
23	V_{CC}	+12V power supply.
24	GND	Ground.
25	$EAMP_{OUT}$	Error amplifier output. The positive trajectory output (desired velocity) is summed with the negative velocity input (actual velocity) to form a difference output. The velocity input comes from the servo controller (such as the ML4403).
26	$EMEAS_{OUT}$	Error measure output. This output averages the value of the access loop error during deceleration.
27	V_{REF}	The analog zero reference point. This pin is intended to be driven with the ML4401 V_{REF} output. The ML4404 has an internal 5V reference connected through a current limiting resistor to this pin so that standalone operation/evaluation is available.
28	$EAMP_{IN}$	Error amplifier input. The INPUT summing node for the trajectory and velocity signals.

5

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied. (All voltages referenced to GND.)

Power Supply Voltage, V_{CC} 14V
V_{REF}, R_{SENSEA}, R_{SENSEB} ..... −0.3 to +7V
TTL Inputs, I_{BIAS}, $ELATCH_{OUT}$ ..... −0.3 to +7V
PWM_{OUTA}, PWM_{OUTB}, PWM_{OUTC} ..... −0.3 to V_{CC} +0.3V
Anticipate, V_{IOUT}, $EAMP_{OUT}$ ..... −0.3 to V_{CC} +0.3V
$EAMP_{IN}$, $TRAJ_{IN}$ ..... −0.3 to V_{CC} +0.3V
I_{SUM} ..... V_{REF} −1 to V_{REF} +1V
$TRAJ_{OUT}$, RX_A, RX_B, RY, RY_{VOS} ..... V_{REF} −1 to V_{CC} +0.3V
Storage Temperature Range ..... −65°C to +150°C
Junction Temperature (T_J) ..... +125°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

(See Figure 7)

Temperature Range ..... 0°C to 70°C
Supply Voltage (V_{CC}) ..... 12V ± 10%
R_{SET} 6.2K
RK1 ..... 110K
RY 3K
RY_{VOS} 3K
RX 6.8K
RK3 ..... 12K to V_{REF}
CCOMP 56pF
CF1 ..... 0.0022µF
CF2 ..... Open
RF 10K
R_{LOAD} ..... 20K to V_{REF}

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of V_{CC} = 10.8 to 13.2V, V_{REF} = 5V, TA = 0 to 70°C, R_{FILT} = 10K, RY = RY_{VOS} = 3K, RK1 = 100K, RX = 6.8K, R_{SET} = 6.2K and RK3 = 12K to V_{REF} unless otherwise specified. (See Note 1.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
DC CHARACTERISTICS						
I_{CC}	Power Supply Current			23	35	mA
DIGITAL INPUT/OUTPUT CHARACTERISTICS						
(Inputs PWM_{INA}, B, C, MSB, LSB, DIR)						
V_{IH}	Logic High Voltage		2.0			V
I_{IH}	Logic High Current	V_{IH} = 2.4V	−40	10	40	µA
V_{IL}	Logic Low Voltage				0.8	V
I_{IL}	Logic Low Current	V_{IL} = 0.4V	−40	1	40	µA
Inputs (DECEL)						
V_{IH}	Logic High Voltage		2.0			V
I_{IH}	Logic High Current	V_{IH} = 2.4V	−250	5	40	µA
V_{IL}	Logic Low Voltage				0.8	V
I_{IL}	Logic Low Current	V_{IL} = 0.4V	−1600	−850	0	µA
Outputs ($ELATCH_{OUT}$)						
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA	0	0.3	0.4	V
V_{OH}	Output High Voltage	R_L = 5K to V_{REF}	2.4	5.0	5.5	V
Trajectory Amplifier (See Note 3)						
I_B	Input Bias Current		0	7	20	nA
A_V	Open Loop Gain			75k		V/V
BW	Unity Gain Bandwidth			1		MHz
PHIM	Phase Margin			75		DEG
Velocity Error Amplifier						
V_{OS}	Input Offset Voltage		−10		10	mV
I_B	Input Bias Current		0	50	300	nA
A_V	Open Loop Gain			120k		V/V
I_{SOURCE}	Source Current		4	8		mA
I_{SINK}	Sink Current		1	2		mA
BW	Unity Gain Bandwidth			1		MHz
PHIM	Phase Margin			75		DEG
V_{OUT}	Output Voltage Range		0.5		V_{CC} −3	V

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of V_{CC} = 10.8 to 13.2V, V_{REF} = 5V, T_A = 0 to 70°C, R_{FILT} = 10K, RY = RY_{VOS} = 3K, RK1 = 100K, RX = 6.8K, R_{SET} = 6.2K and RK3 = 12K to V_{REF} unless otherwise specified. (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
Biasing						
V_{IS}	I_{SET} Voltage		2.00	2.02	2.06	V
PWM to Current Translators						
	I_{CHARGE}/I_{SET}, I_{DIS}/I_{SET}	PWM_{OUT} = 5.0V		0.98		mA/mA
	I_{CHARGE}/I_{DIS}	PWM_{OUT} = 5.0V	0.910	0.99	1.10	mA/mA
V_{OUT}	Output Voltage Range		1.5		9	V
Transconductance Amps						
V_{OS}	Input Offset Voltage		-10		10	mV
gm	Transconductance			1700		μMhos
I_{OUTMAX}	Max Output Current			90		μA
I_B	Input Bias Current			4.5		μA
Latch/Comparator						
I_B	Input Bias Current		0	2	10	μA
V_{OS}	Input Offset Voltage	$V_{TRAJOUT}$ @ 5V	-10		10	mV
A_V	Open Loop Gain			15k		V/V
t_{pd}	Propagation Delay	C_L = 10pF, R_L = 2K to V_{REF}		60		ns
V/I Amp						
I_{OS}/I_{SENSE} *100	Sense Current Offset	$I_{SENSEA} = I_{SENSEB}$ 0.1mA < I_{SENSE} < 1mA V_{IOUT} = 5V	-2	0	2	%
V_{SMAX}	Max R_{SENSE} Voltage		0.5	0.64		V
V_{OUT}	Output Range		1.8		9	V
Trajectory DAC						
I_{MSB}/I_{SET}	MSB Current			0.98		mA/mA
I_{MSB}/I_{LSB}	MSB to LSB Ratio		7.8	8.00	8.5	mA/mA
Trajectory Multiplier (Note 4)						
V_{OS}	V_{OUT} - V_{REF} at Origin	V_{OUT} at I_{SUM} = 0	-5		5	mV
	V_{TRACK1} : $V_{TRACK32}$	(V_{OUT} at I_{LSB}/32)/(V_{OUT} at I_{LSB})	0.090		0.140	mV/mV
	V_{TRACK2} : $V_{TRACK32}$	(V_{OUT} at I_{LSB}/16)/(V_{OUT} at I_{LSB})	0.165		0.205	mV/mV
	V_{TRACK4} : $V_{TRACK32}$	(V_{OUT} at I_{LSB}/8)/(V_{OUT} at I_{LSB})	0.270		0.320	mV/mV
	V_{TRACK8} : $V_{TRACK32}$	(V_{OUT} at I_{LSB}/4)/(V_{OUT} at I_{LSB})	0.430		0.470	mV/mV
	$V_{TRACK16}$: $V_{TRACK32}$	(V_{OUT} at I_{LSB}/2)/(V_{OUT} at I_{LSB})	0.660		0.695	mV/mV
V_{LSB}	$V_{TRACK32}$	V_{OUT} at I_{SUM} = I_{LSB}	0.935		1.035	V
V_{CROSS}	Crossover Error	(V_{OUT} at I_{SUM} = I_{LSB}) - (V_{OUT} at I_{SUM} = I_{MSB}/8)	-25		+10	mV
	$V_{TRACK32}$: $V_{TRACK256}$	(V_{OUT} at I_{MSB}/8)/(V_{OUT} at I_{MSB})	0.305		0.325	mV/mV
	$V_{TRACK64}$: $V_{TRACK256}$	(V_{OUT} at I_{MSB}/4)/(V_{OUT} at I_{MSB})	0.450		0.470	mV/mV
	$V_{TRACK128}$: $V_{TRACK256}$	(V_{OUT} at I_{MSB}/2)/(V_{OUT} at I_{MSB})	0.670		0.685	mV/mV
	$V_{TRACK192}$: $V_{TRACK256}$	(V_{OUT} at I_{MSB}*3/4)/(V_{OUT} at I_{MSB})	0.840		0.860	mV/mV
V_{MSB}	$V_{TRACK256}$	V_{OUT} at I_{SUM} = I_{MSB} (Full Scale + 1)	3.070		3.225	V
PSRR	Supply Rejection	at Origin at Full Scale		0.2 2		mV/V mV/V

Note 1: 0°C to +70°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.
Note 2: Typicals are parametric norm at 25°C.
Note 3: Minimum recommended load resistor is 10kΩ from the trajectory output to V_{REF}.

FUNCTIONAL DESCRIPTION

Power Supply and Reference Requirements

The ML4404 operates from a single 12V power supply. In addition, a 5.0V reference is required at pin V_{REF} which is available from the ML4401, ML4431. V_{REF} serves as a system reference or "analog ground".

Biasing

All of the critical internal biasing on the ML4404 is set as a function of an external resistor, R_{SET}. An internal feed-back loop forces the voltage on I_{SET} (pin 3) to be 2.0V. R_{SET} is connected from this pin to V_{REF} (5.0V) and the resulting current is used in the multiplier and duty cycle-to-current translators.

$$I_{BIAS} = (V_{REF} - 2)/R_{SET} = 3V/R_{SET}$$

The nominal value of I_{BIAS} should be between 0.25 and 0.50mA.

Trajectory Multiplier/Amplifier

The Trajectory Multiplier/Amplifier generates the optimal velocity output from the position-to-go input. The optimal velocity is the $TRAJ_{OUT}$ voltage relative to V_{REF}. The input position is set by the duty cycle of the MSB and LSB-inputs.

During an access operation, the actuator is first driven to maximum acceleration, and then into braking or deceleration. To minimize access times the trajectory curve (velocity vs position) during deceleration must be accurately controlled so that the head stops exactly on the desired track (without overshooting or undershooting). The head is driven to maximum acceleration until this braking curve is reached. Then the velocity is controlled to follow this optimal trajectory during deceleration.

According to the theory for a second order system, time optimal access is achieved if the position is proportional to the square of velocity ($P = KV^2$, or $V = KP^{1/2}$). However, in the real system environment, this theory needs modification in two important areas. First, as shown in Figure 1, the slope of the trajectory at the origin (final position) is infinite for a pure square root function. This infinite slope would result in an infinite bandwidth servo loop. As a result, a first order linear term needs to be included which will reduce the slope of this curve near the origin. Second, at large velocity, the square root function is not quite optimal, due to non-zero actuator inductance. A higher order term to modify the curve in this region needs to be included.

This trajectory curve, with its first, second, and third order terms is implemented with a multiplier in the feedback loop of an opamp (see Figure 2). The position input is a current which is a fraction of I_{BIAS}, as discussed in the trajectory DAC section below. The first order term is implemented with a feedback resistor (RK1) directly in the feedback path of the op amp. This transfer function of this I/V converter is expressed by $V_{OUT} = RK1 * I_{IN}$. The second order term comes from the multiplier.

$$I_{IN} = (V_{OUT}^2/(2.25\, I_{BIAS} * RX * RY))$$

With both terms together,

$$I_{IN} = \frac{V_{OUT}}{RK1} + \frac{V_{OUT}^2}{2.25\, I_{BIAS} * RX * RY}$$

The first order term dominates near the origin, and the second order term dominates, at higher velocities.

The multiplier is modified by the addition of a resistor (RK3) which results in the third order term. This resistor is connected from RXA (pin 18) to either $TRAJ_{OUT}$ or V_{REF}. As shown in Figure 3, the shape of the trajectory curve for large velocities can be adjusted in either direction from nominal, depending on which pins RK3 is connected between. It should be noted that the above equations are only approximate. The actual multiplier transfer function is not a pure second order function, even with RK3 unconnected. The multiplier is designed to approximate the required trajectory for most typical servo systems. For most applications, very little correction with RK3 will be required. On the ML4404, an additional resistor (RY_{VOS}) equal to RY can be included which nulls the offset of the curve near the origin.

Since the resistors R_{SET}, RK1, RX, RY, RK3, and RY_{VOS} are all external, any desired trajectory can be set. The constraints on these values are as of follows:

$V_{OUTMAX} < 1.5 * RX * I_{BIAS}$
$V_{OUTMAX} > 1.5 * RY * I_{BIAS}$
$V_{OUTMAX} < 3.5V$
$6k < R_{SET} < 12k$ for $V_{REF} = 5V$
$R_{FILT} < RK1/10$
$R_{FILT} * C_{FILT2} < RK1 * C_{COMP}$
$R_{LOAD} > 10k$ to V_{REF}

V_{OUTMAX} is the maximum trajectory output voltage (relative to V_{REF}).

Trajectory DAC

The trajectory DAC creates, a position input for the trajectory multiplier. The position input is controlled by the duty cycle of the TTL inputs MSB and LSB. For most applications the position information will be digitally encoded to 8-bit resolution — each code representing one track. Therefore, the full scale input of the trajectory curve is 255 tracks. The input current corresponding to this full scale is I_{BIAS}.

Since the duty cycle of a single line is difficult to control to 0.4% (1/256), the duty cycle to input current translator section is divided into 2 signals (MSB and LSB). As shown in Figure 4, the ratio between these two currents is 8/1. The 5 lower order bits of code are modulated into the LSB input, and the 3 higher order bits into the MSB input. For example, a position input of 32 tracks would correspond to the MSB line always inactive, and the LSB line always active. 256 tracks would be MSB always active, and the LSB always inactive. 1 track would be MSB always inactive, and LSB 1/32 of the period active.

In general for an 8-bit binary code D7 D6 D5 D4 D3 D2 D1 D0 where D7 is the high order bit, the active duty cycle for the MSB input is D7 D6 D5/8 and the active duty cycle for the LSB input is D4 D3 D2 D1 D0 /32. For example 10100011 (163 tracks) would be active 5/8 of a period on the MSB, and 3/32 of a period on the LSB.

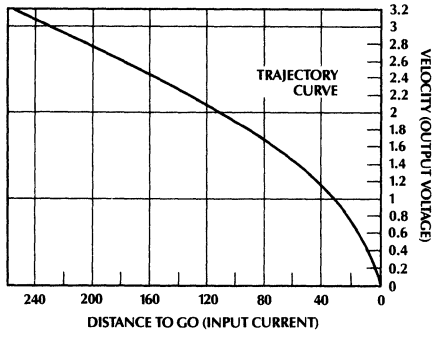


Figure 1.

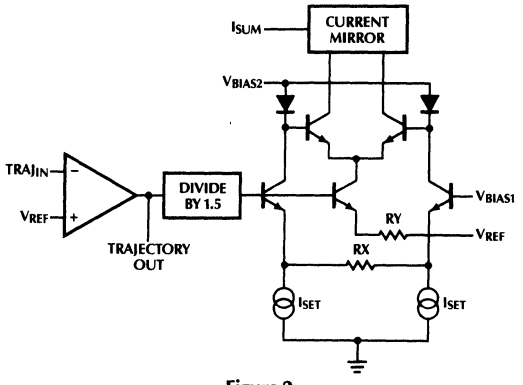


Figure 2.

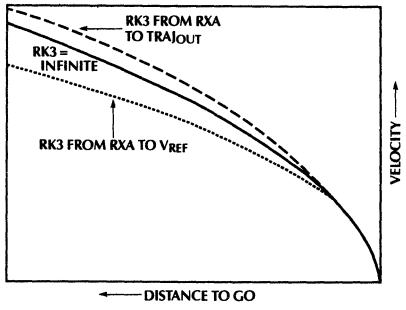


Figure 3.

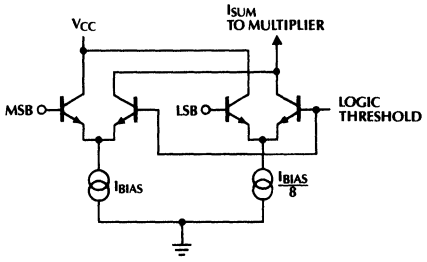


Figure 4.

AC Considerations — Trajectory Amp/Multiplier

The AC response of the trajectory output is primarily controlled by the external components C_{FILT1}, C_{FILT2}, R_{FILT}, RK1, and C_{COMP}. Four parameters must be considered to determine the values of these components.

First, the value of RK1 is set based on the bandwidth of the servo loop. RK1 sets the gain of the trajectory function at the origin. As the system bandwidth increases, more gain is required near the origin, and the value of RK1 increases.

Second, the exponential decay rate of the trajectory output during deceleration must be fast enough for the mechanical system to dominate the loop response. As the head approaches the target track, the multiplier (2nd and 3rd order terms) becomes less significant, and the first order term dominates. In this region, the exponential decay is dominated by the RK1 * C_{COMP} product. This product should be set at a frequency which is a few times higher than that of the position loop bandwidth, so that the overall phase margin is not significantly degraded.

Third, the filter components should be set such that the ripple from the trajectory DAC is minimized. Once the values for C_{COMP} and RK1 have been set, then the values of the remaining components, C_{FILT1}, C_{FILT2}, and R_{FILT}, can be determined. As the capacitance and resistance of these components increase the PWM ripple from the trajectory DAC is reduced. Due to the nonlinear nature of this circuit block, a mathematical analysis of the ripple is quite cumbersome, so the values of these components are best chosen empirically. The PWM ripple is dependent on R_{FILT}, C_{FILT1}, C_{FILT2}, as well as the duty cycle (50% duty cycle on the MSB will result in the largest ripple), and the frequency of modulation (the ripple is proportional to the square of the period).

Fourth, the R_{FILT}-C_{FILT} combination must be set such that the dynamic response of the trajectory output does not overshoot during deceleration. Ideally, the RC combination should be set such that the system is critically damped to a maximum deceleration input.

Note that a tradeoff exists between the ripple amplitude and the transient response. Too large a value of R_{FILT}-C_{FILT} will cause an overshoot in the transient response, and a low ripple level. Too small a value will provide acceptable transient response, but a large ripple amplitude. A range of values exists for most applications which results in acceptable performance for both ripple and transient response.

Anticipate

The function of the anticipate block is to modify the trajectory curve during acceleration. This compensates for the actuator inductance delay during the accelerate-to-decelerate transition.

At the start of a access operation, the actuator is driven into acceleration. The actuator velocity increases until either the maximum velocity is reached, or the trajectory deceleration curve is reached. As shown in Figure 5, if the trajectory curve is reached first, then the actuator needs to be driven into deceleration so that the trajectory curve can be followed. This accelerate-to-decelerate transition requires that the

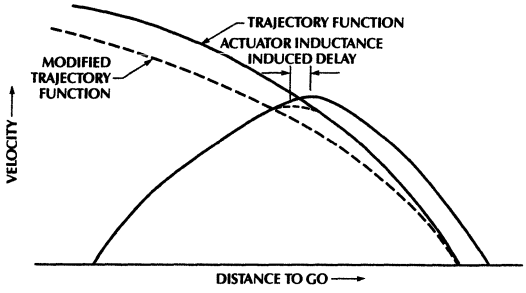


Figure 5.

current in the actuator be reversed. Since this cannot happen instantaneously (due to actuator inductance), a phase shift results. The actuator will then overshoot the desired trajectory, and miss the target track. However, if the curve can be modified (see Figure 5) such that the accelerate-to-decelerate transition begins before the nominal trajectory is reached, this overshoot problem can be eliminated. This function is implemented with a switched transconductance amp. During acceleration (DECEL input low), the anticipate output becomes a voltage follower-the anticipate signal is identical to the $TRAJ_{OUT}$ signal. An external resistor from anticipate to $TRAJ_{IN}$ will modify the trajectory curve as required. During deceleration, the anticipate output becomes a high impedance and the normal trajectory curve is followed.

In addition to the external resistor, an external capacitor to V_{REF} sets the anticipate decay time constant equal to the current reversal time for the actuator.

Velocity Error Amplifier

The function of this block is to subtract the desired velocity (from the trajectory output) with the actual velocity (from the servo controller) to create a velocity error output. This error output is multiplexed through the servo controller into the servo driver during access mode (see ML4403, ML4413 data sheet).

Since the polarity of the velocity input from the ML4403, ML4413 is the opposite of the trajectory output polarity, the difference function is accomplished with a summing amplifier, as shown in the application diagram. The summing resistors and the feedback resistor are external.

V/I Amp—Velocity Filter

The function of this block is to create a low noise velocity input. The velocity error amp requires that a clean, noise-free velocity input be compared with the desired velocity (from the trajectory output) to create a velocity error signal.

One way to create this velocity signal is to differentiate position. However, the differentiated signal will be noisy, and this noise can excite the mechanical resonances in the system. Another way to create velocity is to integrate acceleration. This eliminates the noise problem, however, the integrator DC accuracy will be poor due to the drift.

The ML4404 uses both of these techniques to achieve a low noise tachometer function which will operate at low frequencies noise from the mechanical resonances is attenuated by the RC filter. The filter output is then summed with a current proportional to acceleration.

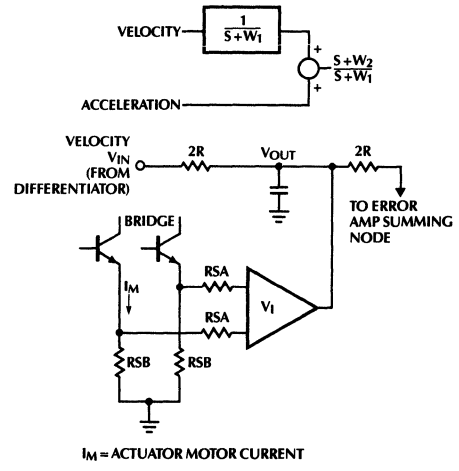


Figure 6.

The V/I amp creates this current by monitoring the sense resistors in the bridge driver. The resulting transfer function has both a pole and a zero, and can be expressed by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R*(M*RSB/(KF*KT*RSA))*S + 1}{R*C*S + 1}$$

Where KT = The velocity transducer gain (from differentiator)

KF = Motor force constant

M = Total moving mass

The above equation is a first order approximation which assumes that the, frictional components of the system (such as windage) are negligible. If the pole and zero are set to identical frequencies, then an all pass function is achieved. To do this, first, set the pole (W = 1/RC) at a frequency much lower than the mechanical resonances. Then set the scaling resistors, RSA, such that:

$$RSA = M*RSB/(KF*KT*C)$$

Note that setting a lower corner frequency results in increased dependence on the actuator current being an accurate representation of true acceleration. Some frictional terms and bias forces (such as flex cable force), as well as variations in KF, will distort this relationship. The lower limit on this corner frequency will be determined by these non ideal effects.

Error Averaging

The velocity error output should ideally be within a few millivolts of V_{REF} (near zero error) through the deceleration region. However, due to manufacturing tolerances, this error will not be identical for each drive. The $EMAS_{OUT}$ and $ELATCH_{OUT}$ pins, allow this error to be nulled out for each individual system.

During deceleration (DECEL input high) a transconductance amplifier is switched on (see Block Diagram) and the velocity error output is integrated through an external capacitor. This average velocity error is then compared with V_{REF} and sent to $ELATCH_{OUT}$ (TTL output).

During acceleration (DECEL input low) the amplifier is switched off (high impedance output) and the external capacitor is discharged to V_{REF} through an external resistor. In this condition, the TTL output, $ELATCH_{OUT}$, is held in its previous state. Since the velocity error during acceleration is not of interest, the $ELATCH_{OUT}$ during acceleration is the sign of the average velocity error output at the end of the previous deceleration cycle.

The processor can modify the velocity transducer gain based on the state of the $ELATCH_{OUT}$ signal. During a power-up sequence, this transducer gain can be iteratively adjusted through several seek operations until the velocity error is minimized. As described below, one of the PWM to current translators on the ML4404 could be used to adjust this transducer gain.

PWM To Current Translators

The function of this block is to convert the duty cycle of a TTL input line to an analog output voltage. To optimize a complex servo control system, the manufacturing tolerances of some components must be accounted for. Traditionally, the manufacturing process included an expensive sequence of measurement and adjustment to bring each individual unit within specification. A more cost effective solution is to perform these tasks through software control.

The ML4404 implements this function with TTL to current translators. The external components R_{PWM} and C_{PWM} set the desired characteristics. The operation of these translators can be expressed by:

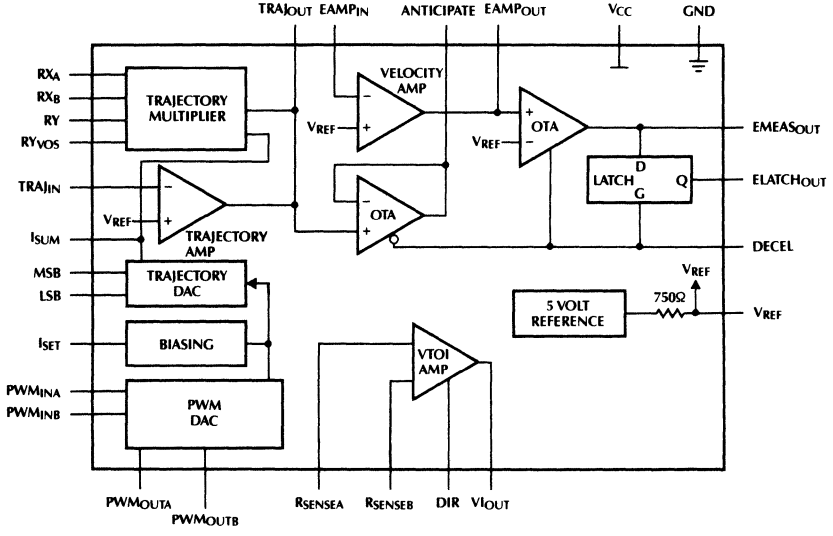
$$VO = V_{REF} + I_{BIAS} * R_{PWM} * (2 * DUTY\ CYCLE/100 - 1)$$

Thus for a 50% duty cycle, the output voltage equals the reference voltage. The output voltage increases linearly with the input duty cycle.

The external capacitor (C_{PWM}) should be made sufficiently large to smooth out the PWM ripple.

The ML4404 has two translators. These stand-alone converters can be used for any purpose, but their intended functions are:

1. To set the AGC reference voltage on the ML4401, ML4431 servo demodulator.
2. To offset the position loop null location for data recovery (compensator inputs on the ML4403, ML4413 servo controller).
3. To offset the access arrival point for the trajectory (I_{SUM} node on the ML4404).



* Not available on the ML4404
** Not available on the ML4414

Figure 7. Block Diagram of Trajectory Generator.

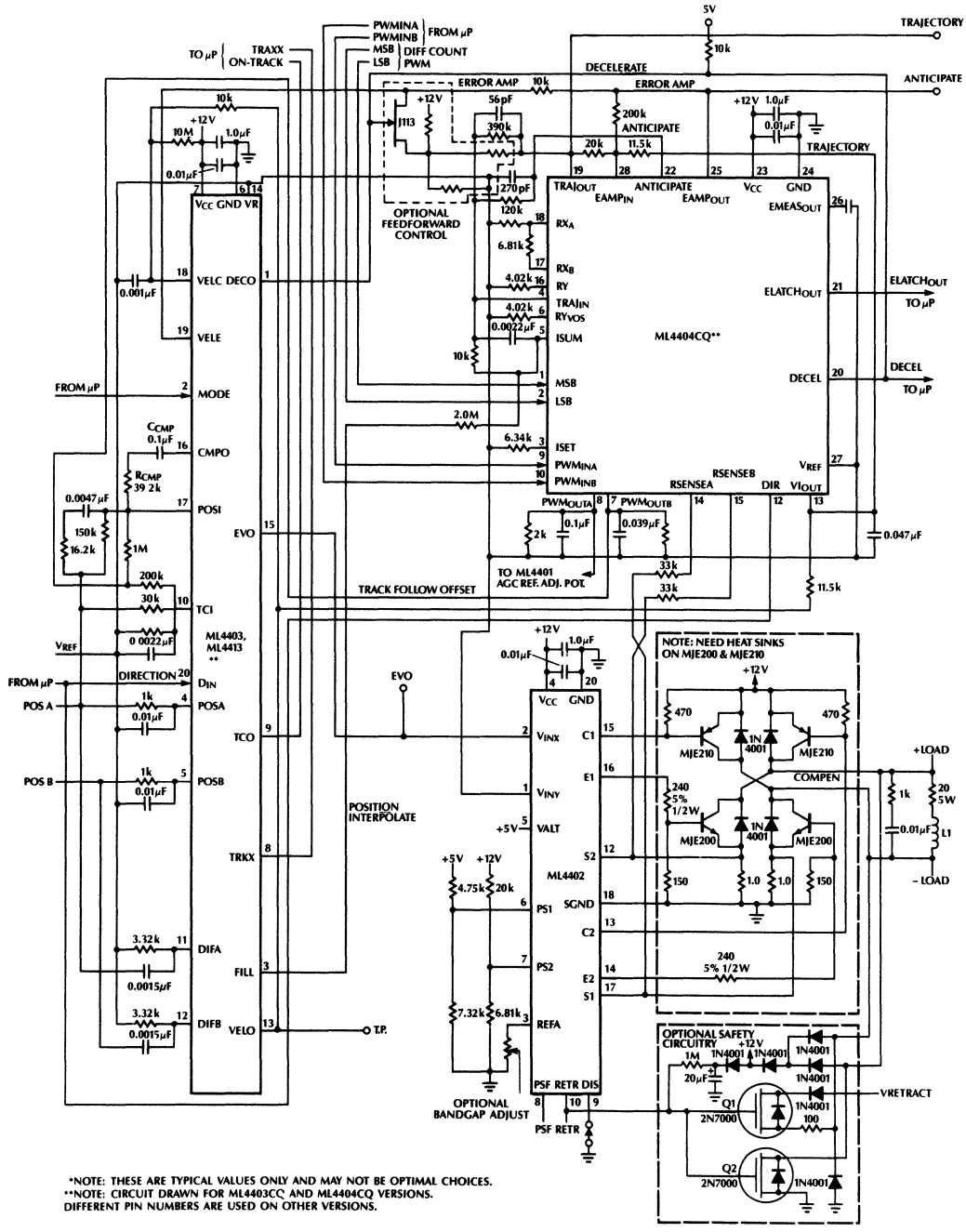


Figure 8. Connecting the ML4403 to the ML4404 Trajectory Generator and the ML4402 Servo Driver

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML4404YCQ	0°C to +70°C	MOLDED PCC (Q28)

Micro Linear

ML4406, ML4407

Disk Voice Coil Servo Driver

GENERAL DESCRIPTION

The ML4406 is a voice coil power driver intended for use in Hard Disk servo systems. The ML4406 contains all power and control circuitry necessary to drive the voice coils of most 3.5" drives. In addition, power fail detection and head retraction functions are provided for orderly shut-down of the drive.

The transconductance is programmed by a logic input at 1/4 A/V and 1/24 A/V respectively, using a 1Ω sense resistor. This allows for greater DAC resolution in digitally controlled servos during track follow without compromising dynamic range during seek.

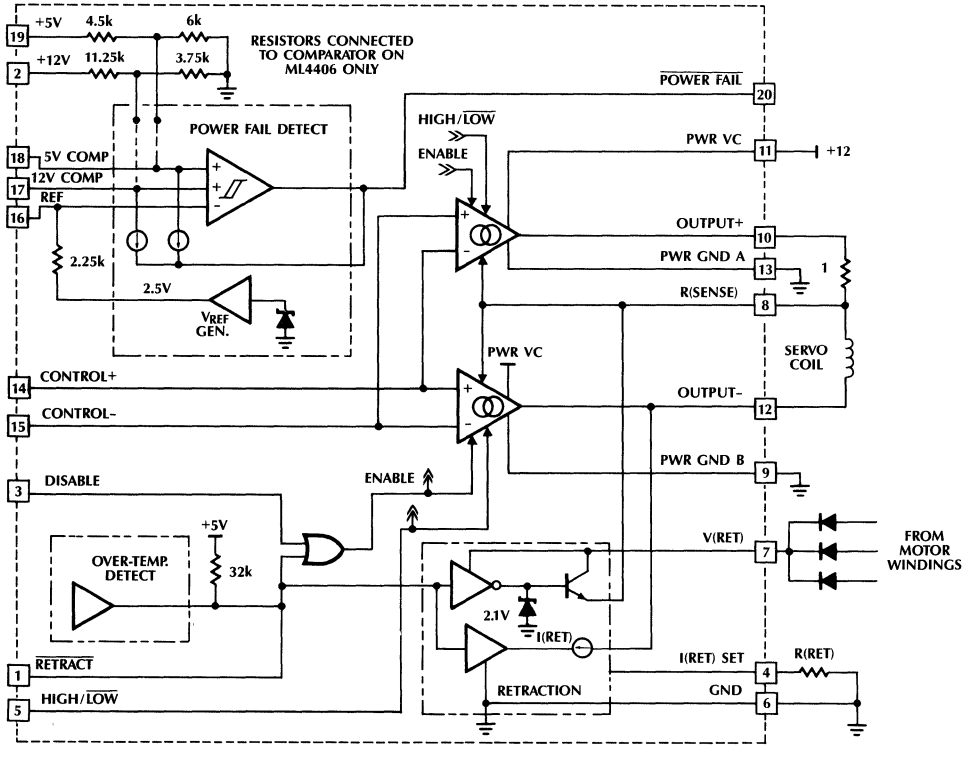
The retraction circuit, main drive cicruit, and control circuits are each powered from their own supplies. This allows maximum flexibility and provides for the lowest forward drop.

The power fail detection circuit includes a precision 2.5V bandgap reference with the option of either internally generated power-fail thresholds (ML4406) or open comparator inputs for adjustable thresholds (ML4407).

The ML4406 is implemented using Micro Linear's bipolar array technology. This allows for easy customization of the IC for a user's specific application.

FEATURES

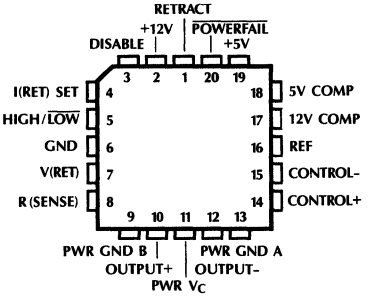
- 500mA power output with 1.5V total forward drop
- Low offsets, cross-over distortion and quiescent current
- Pin-programmable transconductance settings
- Retraction circuitry with programmable retract current, voltage limiting, and separate supply pin
- On-chip precision power fail detect circuitry
- Over-temperature protection with flag output
- Logic input available for disabling outputs



Micro Linear

PIN CONFIGURATION

ML4406/ML4407
20-Pin PCC



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	$\overline{\text{RETRACT}}$	A logic "0" input causes the main outputs to tri-state and the retraction circuit to activate. This input also functions as a flag output and will go low in the event of an over-temperature condition.
2	+12V	12V power to the circuit and input to the power fail detection circuit.
3	DISABLE	A logic "1" turns off the main outputs.
4	I(RET) SET	A resistor to ground sets the retract current.
5	HIGH/$\overline{\text{LOW}}$	A logic "1" sets the trans-conductance gain to 1/4 while a logic "0" sets the gain to 1/24. Transconductance gain is voltage across R_{SENSE} ÷ the input voltage.
6	GND	Analog Signal Ground.
7	V(RET)	Power supply for the retract circuit.
8	R(SENSE)	Current sensing resistor terminal.
9	PWR GND B	Ground Terminal for power amplifier.
10	OUTPUT+	Output terminal for bridge amplifier.
11	PWR VC	Power supply for bridge amplifier.
12	OUTPUT–	Output terminal for bridge amplifier.
13	PWR GND A	Ground Terminal for power amplifier.
14	CONTROL+	Positive input for current command.
15	CONTROL–	Negative input for current command.
16	REF	Reference input to the Power Fail comparator. Leave open to use internal 2.5V reference.
17	12V COMP	Input to the Power Fail Comparator. Connect to an external resistor divider for the ML4407. Internally connected to a resistor divider from 12V in the ML4406.
18	5V COMP	Input to the Power Fail Comparator. Connect to an external resistor divider for the ML4407. Internally connected to a resistor divider from 5V in the ML4406.
19	+5V	5V power supply terminal.
20	$\overline{\text{POWER FAIL}}$	Open collector output drives low if pin 17 or pin 18 are below pin 16. Normally tied to pin 1.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 11, 13, 7, 2) 14V
Voltage Pins 19, 18, 17, 16, 1, 3, 5 ..... –.3V to +7V
Pins 14, 15 ..... –.3 to +V_{CC}
Output Current ..... ±750mA
Retraction Current 80mA
Retract Set Current (Pin 4) 3mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (soldering 10 sec.) ..... 260°C
Thermal Resistance (θ_{JA}) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
Supply Voltage (PWR VC, +12V) ..... 12V ± 10%
+5V (Pin 19) ..... 5V ± 10%
V(RET) (Pin 7) ..... 2.5V to 16V
Control + Voltage Range (Pin 15 = 5V) ..... 0V to V_{CC}
Control – Voltage Range ..... –1V to V_{CC} – 1V

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, V_{CC} = 12V, R_{SENSE} = 1Ω, R_{LOAD} = 15Ω, CONTROL– (Pin 15) = 5V, R_{SET} (Pin 4) = 1.2KΩ.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Amplifier						
Offset					±10	mA
Gain	Pin 5 = 2V		238	250	263	mA/V
	Pin 5 = 0.8V		39.6	41.7	43.8	mA/V
Bandwidth				100		KHz
Sinking Saturation	I_{OUT} = 100mA				.6	V
	I_{OUT} = 300mA				.8	
	I_{OUT} = 500mA				1.0	
Sourcing Saturation	I_{OUT} = 100mA				1.2	V
	I_{OUT} = 300mA				1.3	
	I_{OUT} = 500mA				1.5	
Retraction Circuit						
I(RET)SET				.75		V
Turn On Time				300		ns
Turn Off Time				2		ms
I(RET) Current	Pin 1 = 0.8V		34	50	65	mA
Power Fail Detection Circuit						
Reference Voltage			2.35	2.50	2.65	V
Reference Source Impedance				2.25		kΩ
Comparator Bias Current	ML4407 only, Pin 20 high			50	250	nA
Hysteresis Current	Pin 20 low, ML4407 only			10		μA
Offset Voltage	ML4407 only				10	mV
12V Threshold Hysteresis	ML4406 only ML4406 only		9.5	10 120	10.5	V mV
5V Threshold Hysteresis	ML4406 only ML4406 only		4.40	4.575 30	4.75	V mV
Logic Inputs						
Voltage High (V_{IH})			2	1.4		V
Voltage Low (V_{IL})				1.4	.8	V
Current High (I_{IH})	V_{IN} = 5V				±10	μA
Current Low (I_{IL})	V_{IN} = 0V	Except Pin 1	–40	–10		μA
		Pin 1 Only	–250	–160		μA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, T_A = Operating Temperature Range, V_{CC} = 12V, R_{SENSE} = 1Ω, R_{LOAD} = 15Ω, CONTROL– (Pin 15) = 5V, R_{SET} (Pin 4) = 1.2kΩ.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current Consumption					
Pin 19	I_{LOAD} = 0		1	2	mA
Pin 7	I_{RET} = 0		1	2	mA
Pin 2 + Pin 11	I_{LOAD} = 0		10	15	mA

FUNCTIONAL DESCRIPTION

POWER AMPLIFIER

The ML4406 power amplifier circuit is set up as a Howland current source with a fixed gain of 1/4 or 1/24 (set by driving pin 5 high or low respectively). This architecture yields minimal cross-over distortion while maintaining low output cross conduction currents. The gain figure refers to the ratio of input voltage to the output voltage seen across R_{SENSE}. For example, at a 1/4 gain setting with V– input at 2.5 and the V+ input at 4.5V, +500mA would flow through the coil using a 1Ω sense resistor. Under the same conditions with pin 5 low, the current would be 83mA. The ability to change from low to high gain allows more complete utilization of DAC resolution when in the track follow mode.

The output stage (Figure 2) is designed to provide minimal saturation losses and employs a "composite PNP" for the sourcing drive and a saturable NPN to sink current. Sourcing saturation drop is typically .9V while sinking saturation drop is typically < 0.4V.

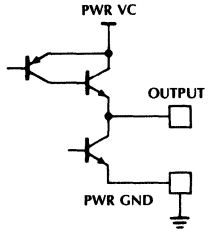


Figure 2. Main Power Output Stage

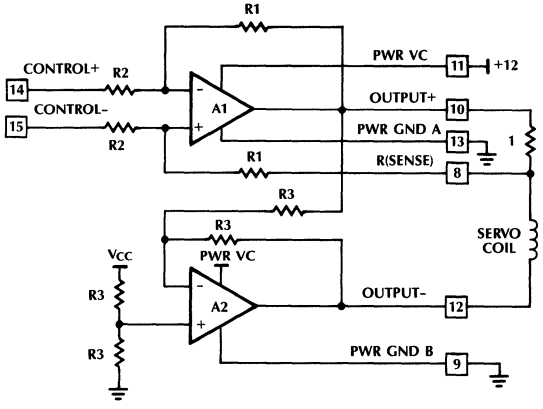


Figure 1. Power Amplifier Topology

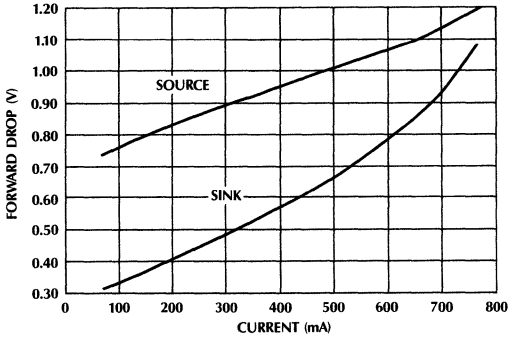


Figure 3. Output Saturation Voltage vs. Output Current (Power V_C = 12V)

Power Fail Detect

The ML4406 power fail detection circuit consists of a precision trimmed reference, resistor dividers, and an "or-function" comparator with hysteresis. The 10μA current sink on the comparator input lowers the comparator's positive input by 15mV when the output of the comparator is high. This creates an effective hysteresis of 30mV at the 5V input (on the ML4406). The amount of hysteresis and threshold levels can be programmed by external resistor dividers on the ML4407. The impedance of the external divider sets the amount of hysteresis while the division ratio sets the power fail threshold. The output at pin 20 is open-collector and is normally tied to pin 1 which is internally pulled-up to 5V.

Retract

The retract circuit features a current sink which is programmed via external resistor from pin 4 to ground (R_{RET}). The output of the retract circuit is voltage limited to 1.4V. The current sink provides an acceleration limit during retract while the voltage limited source provides a velocity limit. Pin 1 (Retract Input) also serves as a flag to indicate an over-temperature condition on the die. Pin 1 goes low in the event of over-temperature, which occurs when the die temperature exceeds a safe operating limit (about 160°C).

The retraction current is set by programming R_{RET} (figure 4). The retract circuit works down to 3V on $V_{RETRACT}$ (Pin 7).

Compensation

Figure 6 shows the equivalent AC circuit for the transconductance amplifier.

The amplifier's current bandwidth is limited by C_{OUT} which varies with the value chosen for R_{SENSE}

$$C_{OUT} = \frac{25nF}{R_{SENSE}}$$

With no snubber (RS and CS) the bandwidth is limited to

$$F_{-3dB} = \frac{1}{2\pi}\sqrt{\frac{2.414}{L(M)\ C(OUT)}}$$

Since this is a second order system with L(M) and C(OUT) forming a resonant circuit, some damping is desirable to reduce ringing in the step response. This is accomplished with a resistive snubber. The optimum value of R(S) occurs when the following condition is met:

$$R(S) = \sqrt{\frac{L(VCM)}{C(OUT)}}$$

For a given C(S), setting R(S) to this value will minimize the ringing in the transient response. Larger values of R(S) will result in more ringing and more bandwidth. Smaller values of R(S) will result in more ringing and less bandwidth. R(S) should not exceed 300Ω.

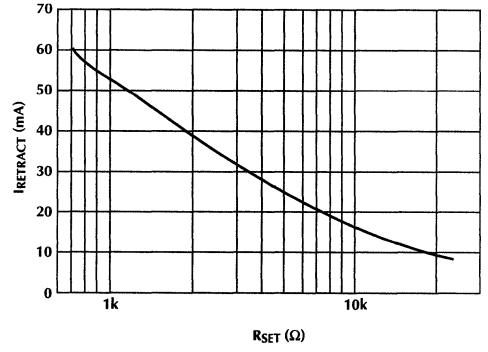


Figure 4. Retract Current vs. R_{SET}

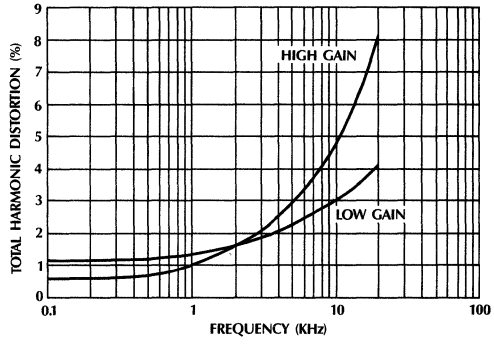


Figure 5. Total Harmonic distortion vs Frequency
Low Gain Setting ($V_{PIN\ 5}$ = 0), R_{SENSE} = 1Ω, V_{IN} = 2.4V_{P-P}
High Gain Setting ($V_{PIN\ 5}$ = 0), R_{SENSE} = 1Ω, V_{IN} = 0.4V_{P-P}

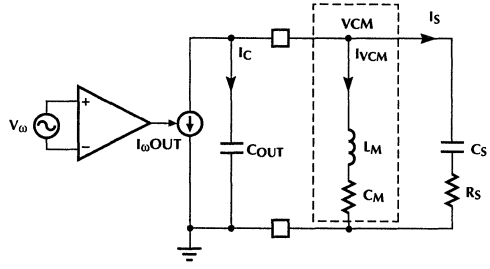


Figure 6. AC Equivalent Circuit for Current Amplifier, Voice Coil Motor (VCM) and Snubber.

C(S) (snubber capacitor) values of between 200nF and 1μF are usually necessary to achieve the desired reduction of ringing in the step response. At the optimum value of R(S) larger values of C(S) further reduce the ringing but do not affect the bandwidth.

Tuning the current loop response can be easily done simulating the network in figure 6 with a computer simulator (such as SPICE).

APPLICATIONS

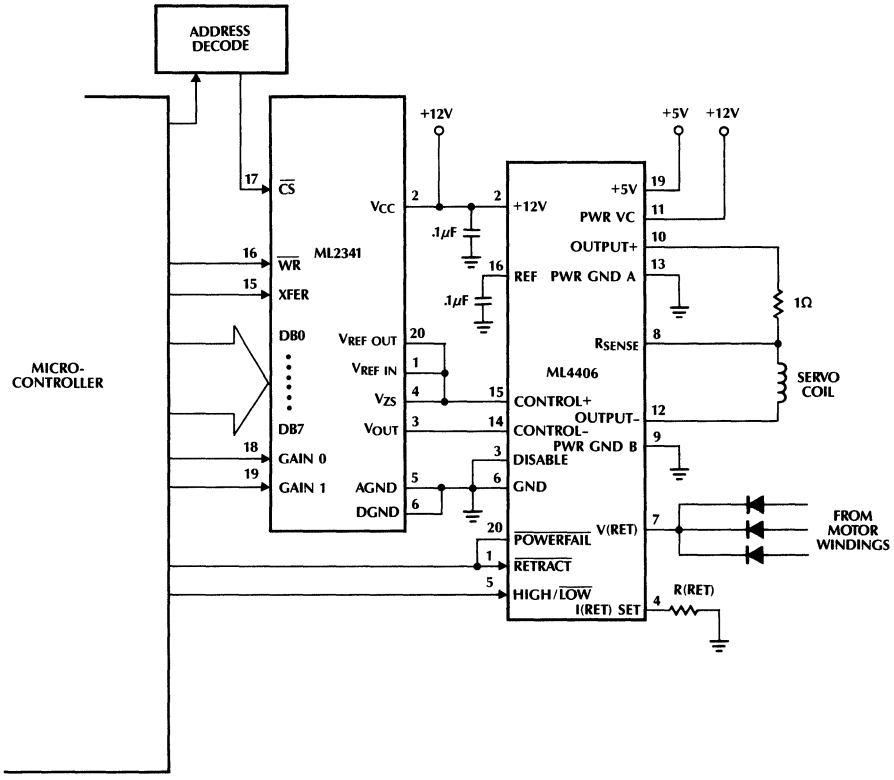


Figure 7. Typical Application: ML4406 used with ML2341 8-bit DAC provides up to 12-bit effective resolution

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML4406CQ	0°C to +70°C	MOLDED PCC (Q20)
ML4407CQ	0°C to +70°C	MOLDED PCC (Q20)

Micro Linear

ML4408

Low Voltage Drop Voice Coil Servo Driver

GENERAL DESCRIPTION

The ML4408 is a voice coil power driver intended for use in High Performance 12V Hard Disk servo systems. The ML4408 contains all control circuitry necessary to drive the voice coils of most small drives. To maximize compliance voltage, the ML4408 includes two 1-Amp NPN drivers and provides drivers for external PNP transistors. In addition, power fail detection and a low voltage head retraction functions are provided for orderly shut-down of the drive.

The transconductance is programmed by a logic input at 1/4 A/V and 1/24 A/V respectively, when using a 1Ω sense resistor. This allows for greater DAC resolution in digitally controlled servos during track follow without compromising dynamic range during seek.

The retraction circuit, main drive circuit, and control circuits are each powered from their own supplies. Retract is self-contained for 12V systems but allows the use of an external PNP retraction with as little as 1V of back EMF from the spindle.

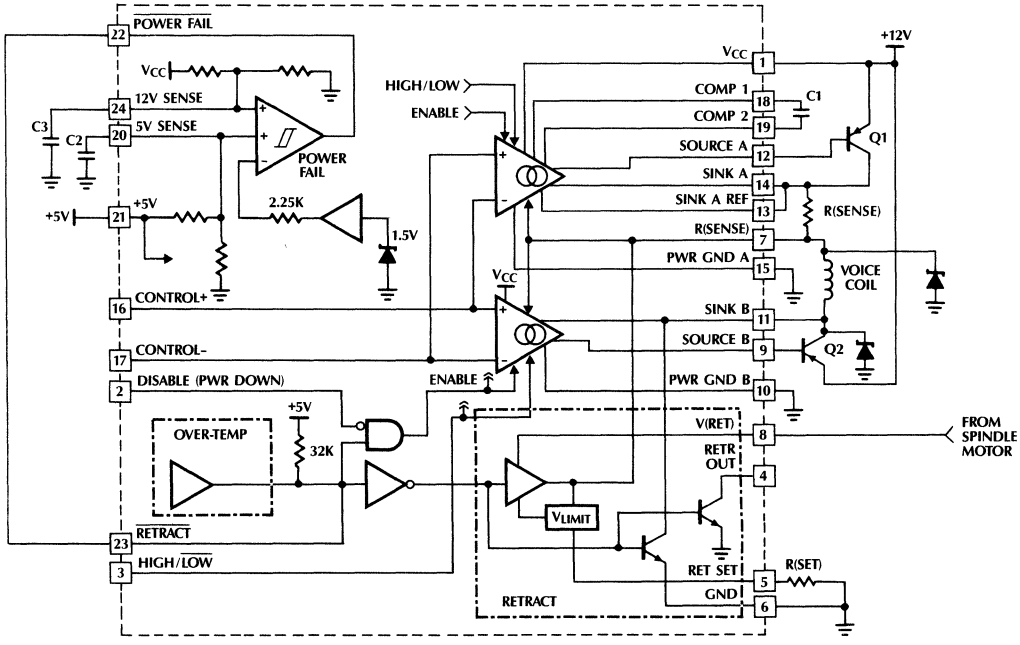
The power fail detection circuit includes a precision 1.5V bandgap reference and a power fail comparator.

The ML4408 is implemented using Micro Linear's bipolar array technology. This allows for customization of the IC for a user's specific application.

FEATURES

- Low saturation voltage (<1V at 1A)
- No cross-over distortion with low quiescent current
- Pin-programmable transconductance settings
- Retraction circuitry with programmable retract voltage and separate power pin
- On-chip precision power fail detect circuitry
- Over-temperature protection with flag output

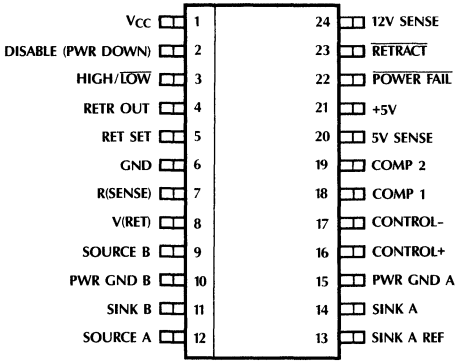
BLOCK DIAGRAM



Micro Linear

PIN CONFIGURATION

ML4408
24-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	V_{CC}	Supply input to power amplifiers.
2	DISABLE (PWR DOWN)	A Logic "1" puts the IC into a low power state and disables the power amplifiers.
3	HIGH/$\overline{\text{LOW}}$	A logic "1" sets the transconductance gain to 1/4 while a logic "0" sets the gain to 1/24. Transconductance gain is the $V_{RSENSE} \div V_{CONTROL}$.
4	RETR OUT	Open collector output which pulls low during retract. Used to drive external power transistor to source retract current to the coil and can provide a braking signal to spindle.
5	RET SET	External set resistor to establish a voltage limit for the internal retract driver.
6	GND	Analog signal ground.
7	R(SENSE)	Current sense resistor terminal.
8	V(RET)	Supply pin for retract circuits.
9	SOURCE B	PNP Base drive output for inverting power amplifier.
10	PWR GND B	Power return pin for inverting power amplifier. Normally used for current sensing.
11	SINK B	Current sinking output for inverting power amplifier. Connects to voice coil (–) terminal.
12	SOURCE A	PNP Base drive output for non-inverting power amplifier.
13	SINK A REF	Kelvin sensing point for power amplifier. Connect to SINK A.
14	SINK A	Current sinking output for non-inverting power amplifier. Connects to voice coil (+) terminal.
15	PWR GND A	Power return pin for non-inverting power amplifier. Normally used for current sensing.
16	CONTROL+	Positive input for current command.
17	CONTROL–	Negative input for current command.
18	COMP 1	Pin for external compensation capacitor.
19	COMP 2	Pin for external compensation capacitor.
20	5V SENSE	Center node of a resistor divider from +5V.
21	+5V	Input for +5V for power fail detection and logic power supply.
22	$\overline{\text{POWER FAIL}}$	Open Collector output drives low for low voltage conditions.
23	$\overline{\text{RETRACT}}$	A logic "0" initiates retract. Also used as an open-collector over-temperature output flag.
24	12V SENSE	Input to the power fail comparator from a resistor divider from V_{CC}.

5

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (pins 1, 8) 14V
Voltage pins 2, 3, 23 ..... –.3V to +7V
pins 4, 7, 9, 11, 12, 13, 14, 16, 17, 22 ..... –.3V to V_{CC}
Output Sink Current ..... ±1A
Retraction Current 80mA
Retract Set Current (pin 5) 3mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... 150°C
Thermal Resistance (θ_{JA}) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to +70°C
V_{CC} Supply Voltage
12V operation ..... 10.8V to 13.2V
+5V (pin 21) Supply Voltage ..... 4.5V to 5.5V
V(RET) (pin 8) Supply Voltage
12V operation ..... 2.5V to 13.2V
Control + Voltage Range (pin 15 = 5V) ..... 0V to V_{CC}
Control – Voltage Range ..... 2V to V_{CC} – 1.5V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, V_{CC} = Operating Range, R_{SENSE} = 1Ω, R_{COIL} = 15Ω, CONTROL– (pin 17) = $V_{CC/2}$, C1 = 30pF, Q1, Q2 = MJE210, R_{SET} = 3.7KΩ.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Amplifier					
Offset				±10	mA
Gain	Pin 5 = 2V	238	250	263	mA/V
	Pin 5 = 0.8V	39.6	41.7	43.8	mA/V
Bandwidth			100		KHz
Sinking Saturation	I_{OUT} = 100mA		.3		V
	I_{OUT} = 300mA		.4		V
	I_{OUT} = 500mA		.5		V
Sourcing Saturation	I_{OUT} = 100mA		.1		V
	I_{OUT} = 300mA		.2		V
	I_{OUT} = 500mA		.3		V
Source A/B Base Drive		20			mA
Q1/Q2 Standby Current	$V_{PIN\ 16}$ = 5V		4		mA
Retraction Circuit					
I(RET) SET			.75		V
Turn On Time			800		ns
Turn Off Time			8		µs
Source Voltage	$V_{PIN\ 23}$ = 0.8V, $V_{PIN\ 8}$ = 3V, $I_{PIN\ 7}$ = 50mA	0.95	1.2	1.5	V
Sink Current	$V_{PIN\ 23}$ = 0.8V, $V_{PIN\ 8}$ = 1.2V, $V_{PIN\ 11}$ = 0.5V	36	48	60	mA
RETR OUT V_{OL}	$V_{PIN\ 23}$ = 0.8V, $I_{PIN\ 4}$ = 1mA		0.1	0.4	V
Power Fail Detection Circuit					
12V Threshold		9.5	10	10.5	V
Hysteresis — 12V Sense			120		mV
5V Threshold		4.40	4.575	4.75	V
Hysteresis — 5V Sense			30		mV

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, T_A = Operating Temperature Range, V_{CC} = Operating Range, R_{SENSE} = 1Ω, R_{COIL} = 15Ω, CONTROL- (pin 17) = $V_{CC/2}$, C1 = 30pF, Q1, Q2 = MJE210, R_{SET} = 3.7KΩ.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Inputs and Outputs					
Voltage High (V_{IH})		2	1.4		V
Voltage Low (V_{IL})			1.4	.8	V
Current High (I_{IH})	V_{IN} = 5V			±10	μA
Current Low (I_{IL})	V_{IN} = 0V, except pin 23	-40	-10		μA
	V_{IN} = 0V, pin 23 only	-250	-160		μA
Voltage Low (pins 22, 23)	I_{OL} = 1mA			.4	V
Over-Temperature Detection					
T_J Threshold			160		°C
Hysteresis			30		°C
Current Consumption					
Pin 21	Pin 21 = 5.5V		5	7	mA
Pin 1	V_{CC} = 13.2V, $V_{PIN\ 16}$ = $V_{CC/2}$		5	10	mA
Pin 8	$V_{PIN\ 8}$ = 13.2V, $V_{PIN\ 23}$ = 5V		3.5	5	mA

FUNCTIONAL DESCRIPTION

POWER AMPLIFIER

The ML4408 power amplifier circuit (figure 1) is set up as a Howland Current source with a fixed gain of 1/4 or 1/24 (set by driving pin 3 high or low respectively). This architecture yields minimal cross-over distortion while maintaining low output cross conduction currents. The gain figure refers to the ratio of input voltage to the output voltage seen across R_{SENSE}. For example, at a 1/4 gain setting, with V(–) input at 2.5V and the V(+) input at 4.5V, +500mA would flow through the coil using a 1Ω sense resistor. Under the same conditions with pin 3 low, the current would be 83mA. If lower input voltage swings and higher currents are desired, the overall transconductance gain may be increased by using a lower value of sense resistor, however offset current will increase proportionally. The ability to change from low to high gain allows more complete utilization of DAC resolution when in the track follow mode.

The output stage is designed to provide minimal saturation losses and employs an external PNP transistor for the sourcing drive and an internal saturable NPN to sink current. Sinking saturation drop is typically under 0.4V. Sourcing saturation drop depends on the external transistors used.

Care should be taken to avoid drawing substrate currents due to negative excursions on any pin of the ML4408. Schoktty diodes should be included on both sides of the VCM to prevent negative excursions from forward biasing the substrate diodes on the IC.

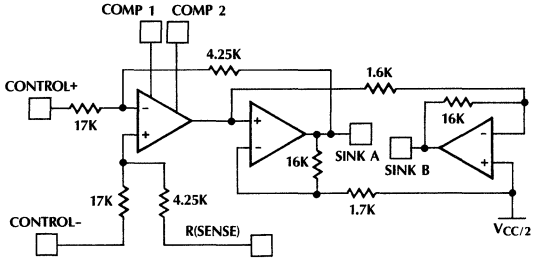


Figure 1. Simplified Power Amplifier Schematic (High Gain Mode)

Two areas should be considered to avoid high frequency oscillation in the output stage:

1. Choose external PNP transistors with a F_T of at least 50MHz.
2. An RC compensation network should be used to cancel the zero presented to the output by the L/R of the voice coil motor as shown in figure 2.

COMPENSATION

Figure 2 shows the equivalent AC circuit for the current amplifier.

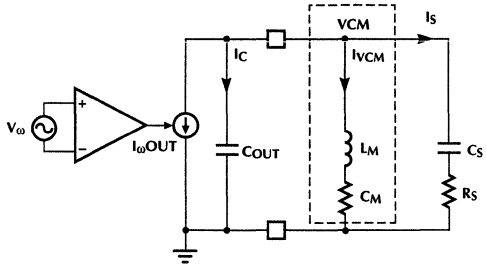


Figure 2. AC Equivalent Circuit for Current Amplifier, Voice Coil Motor (VCM) and Snubber.

The amplifier's current bandwidth is limited by C_{OUT} which varies with the value chosen for R_{SENSE}

$$C_{OUT} \approx \frac{1200\times(C_{COMP} + 12.8pF)}{R_{SENSE}}$$

Where C_{COMP} is C1 between pins 18 and 19. With no snubber (R_S and C_S) the bandwidth is limited to

$$F_{-3dB} = \frac{1}{2\pi}\sqrt{\frac{2.414}{L(M)\ C(OUT)}}$$

Since this is a second order system with L(M) and C(OUT) forming a resonant circuit, some damping is desirable to reduce ringing in the step response. This is accomplished with a resistive snubber. The optimum value of R(S) occurs when the following condition is met:

$$R(S) = \sqrt{\frac{L(VCM)}{C(OUT)}}$$

For a given C(S), setting R(S) to this value will minimize the ringing in the transient response. Larger values of R(S) will result in more ringing and more bandwidth. Smaller values of R(S) will result in more ringing and less bandwidth. C(S) (snubber capacitor) values of between 200nF and 1μF are usually necessary to achieve the desired reduction of ringing in the step response. At the optimum value of R(S) larger values of C(S) further reduce the ringing but do not affect the bandwidth.

Tuning the current loop response can be easily done simulating the network in figure 2 with a computer simulator (such as SPICE).

POWER FAIL DETECT CIRCUIT

The ML4408 circuit consists of a precision trimmed reference, resistor dividers and an "or function" comparator with hysteresis. The output (open collector) of this circuit appears on pin 22. When either comparator input (pins 20 and 24) falls below the 1.5V reference, pin 22 pulls low.

RETRACT CIRCUITS

When pin 23 goes low, pin 4 will pull low. The internal NPN transistor will saturate, pulling SINK B (pin 11) low. This portion of the circuit will function with less than 1V on V(RET). An internal voltage limited pull-up transistor is provided which sources current on pin 7 to the VCM. This circuit will operated reliably down to a V(RET) voltage of around 2.5V, making the ML4408 retract circuit adequate for 12V systems where the spindle motor EMF provided is adequate.

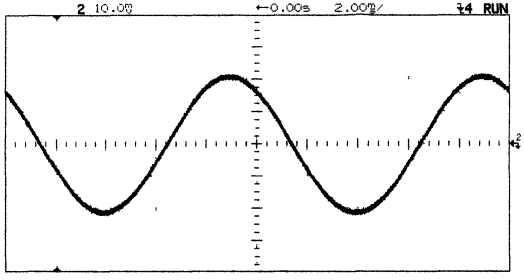


Figure 3. Output Current: V_{IN} = 100 Hz Sine Wave, $1V_{P-P}$ Low Gain Mode ($V_{PIN\ 3}$ = 0), R_{SENSE} = 1Ω

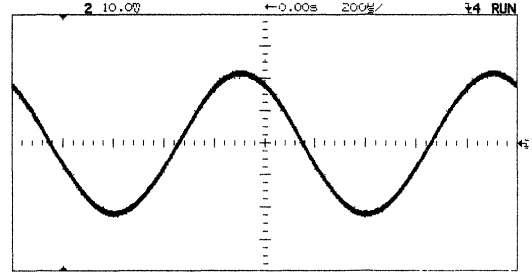


Figure 4. Output Current: V_{IN} = 1 KHz Sine Wave, $1V_{P-P}$ Low Gain Mode ($V_{PIN\ 3}$ = 0), R_{SENSE} = 1Ω

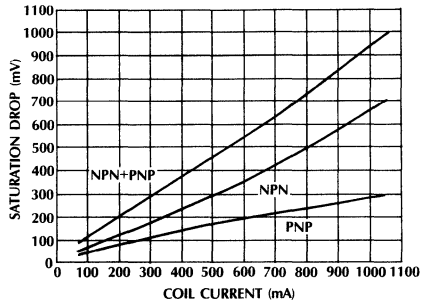


Figure 5. Output Saturation Voltage vs Output Current (Q_1 = Q_2 = MJE210)

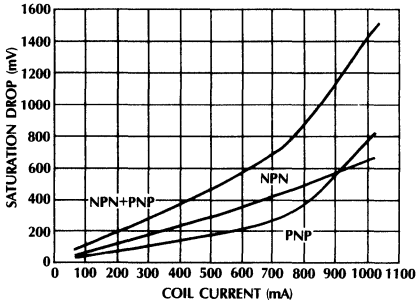


Figure 6. Output Saturation Voltage vs Output Current with BSR31 (Q_1 = Q_2 = BSR31)

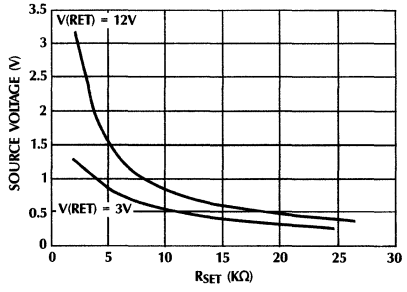


Figure 7. Retract Source Voltage Limit

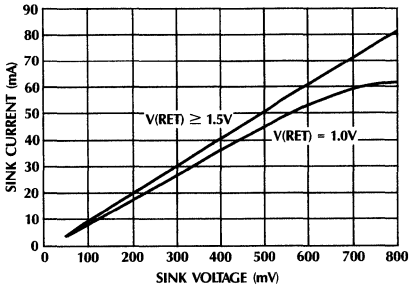


Figure 8. Retract Sink Voltage vs Current

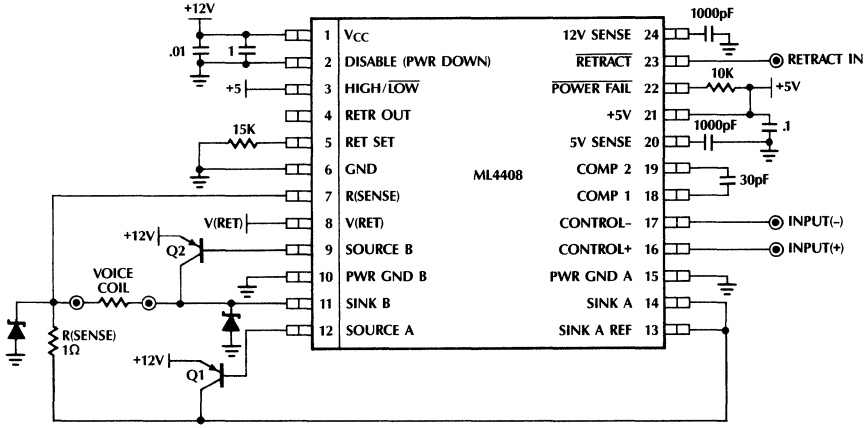


Figure 9. Typical 12V Application

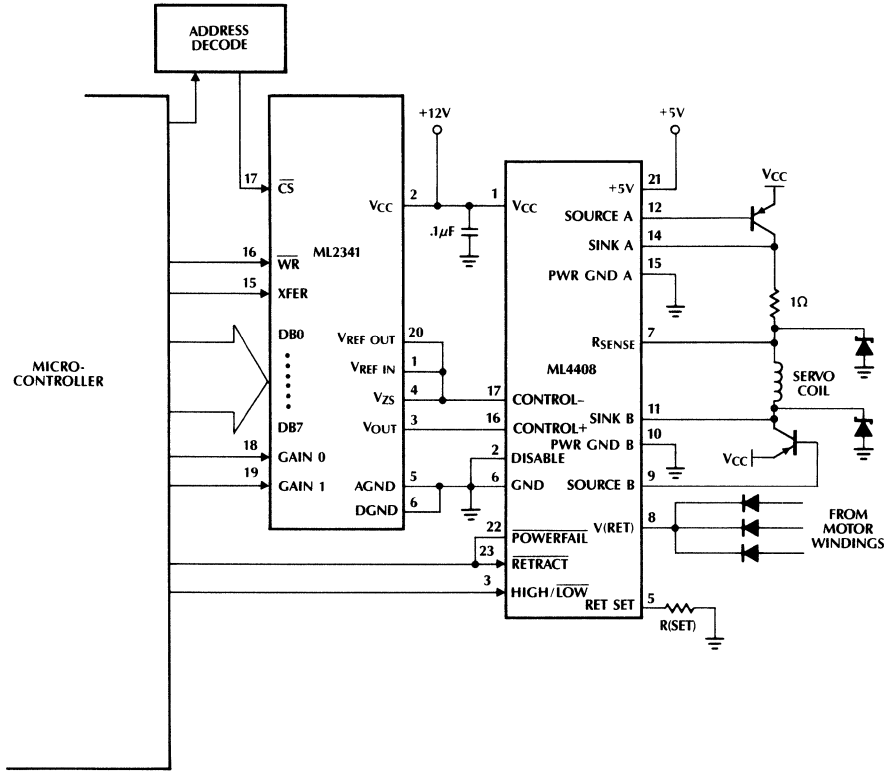


Figure 10. ML4408 Used with ML2341 8-Bit DAC Provides up to 13-Bit Effective Resolution

ML4410

Sensorless Spindle Motor Controller

GENERAL DESCRIPTION

The ML4410 provides complete commutation for delta or wye wound Brushless DC (BLDC) motors without the need for signals from Hall Effect sensors. This IC senses the back EMF of the 3 motor windings (no neutral required) to determine the proper commutation phase angle using phase lock loop techniques. This technique will commutate virtually any 3-phase BLDC motor and is insensitive to PWM noise and motor snubbing.

Included in the ML4410 is the circuitry necessary for a Hard Disk Drive microcontroller driven control loop. The ML4410 controls motor current with either a constant off-time PWM or linear current control driven by the microcontroller. Speed feedback for the micro is a stable digital frequency equal to the commutation frequency of the motor. All commutation is performed by the ML4410. Braking and Power Fail are also included in the ML4410.

Two different start-up sequencing (minimum start-up time or minimum reverse rotation at start up) algorithms are supported by the ML4410. Since the timing of the start-up sequencing is determined by the micro, the system can be optimized for a wide range of motors and inertial loads.

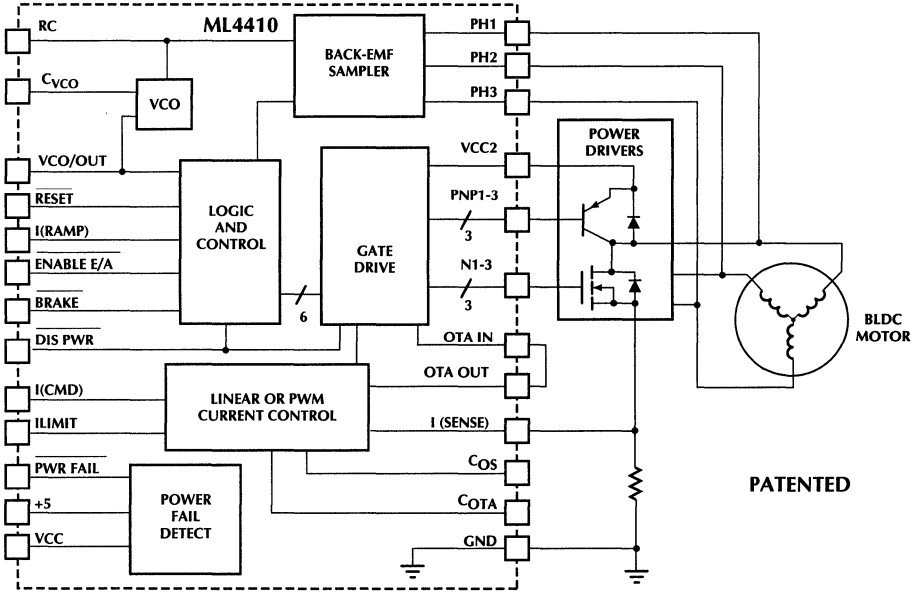
The ML4410 modulates the gates of external N-channel power MOSFETs to regulate the motor current. The IC drives external PNP transistors or P-channel MOSFETs directly. Special circuits are used to save base drive power at low load currents.

FEATURES

- Back-EMF Commutation Provides Maximum Torque for Minimum "Spin-Up" Time for Spindle Motors
- Accurate, Jitter-Free Phase Locked Motor Speed Feedback Output
- Linear or PWM Motor Current Control
- Easy Microcontroller Interface for Optimized Start-Up Sequencing and Speed Control
- Power Fail Detect Circuit with Delayed Braking
- Drives External N-Channel FETs and PNP's or P-Channel FETs

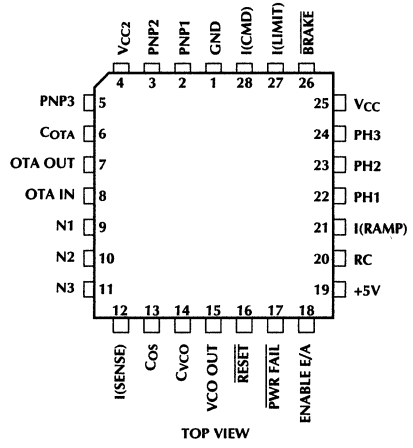
5

BLOCK DIAGRAM



PIN CONNECTION

ML4410
28-Pin PCC (Q28)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	GND	Signal and Power Ground
2	PNP1	Drives the external PNP transistor driving motor PH1.
3	PNP2	Drives the external PNP transistor driving motor PH2.
4	V_{CC2}	12V power and power for the braking fucntion.
5	PNP3	Drives the external PNP power transistor driving motor PH3.
6	C_{OTA}	Compensation capacitor for linear motor current amplifier loop.
7	OTA OUT	Output of motor current error amplifier, normally connected to OTA IN or to external MOSFET gate.
8	OTA IN	Driving voltage for N1-N3. Normally tied to OTA OUT.
9-11	N1, N2 N3	Drives the external N-channel MOSFETs for PH1, PH2, PH3
12	I(SENSE)	Motor current sense input.
13	C_{OS}	Timing capacitor for fixed off-time PWM current control.
14	C_{VCO}	Timing capacitor for VCO
15	VCO OUT	Open Collector Logic Output from VCO.
16	$\overline{\text{RESET}}$	Input which holds VCO off and sets the ML4410 to the RESET condition.
17	$\overline{\text{PWR FAIL}}$	A "0" output indicates 5V or 12V is under-voltage.
18	ENABLE E/A	A "1" logic input enables the error amplifier and closes the back-EMF feedback loop.
19	+5V	5V power supply input.
20	RC	VCO loop filter components.
21	I(RAMP)	Current into this pin sets the initial acceleration rate of the VCO during start-up.
22	PH1	Motor Terminal 1
23	PH2	Motor Terminal 2
24	PH3	Motor Terminal 3
25	V_{CC}	12V power supply. Terminal which is sensed for power fail.
26	$\overline{\text{BRAKE}}$	A "0" activates the braking circuit.
27	I(LIMIT)	Sets the threshold for the PWM comparator.
28	I(CMD)	Current Command for Linear Current amplifier.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (pins 4, 25) 14V
Output Current (pins 2, 3, 5, 9,10,11) ..... ±150mA
Logic Inputs (pins 16, 17, 18, 26) ..... –0.3 to 7V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... 150°C
Thermal Resistance (θ_{JA}) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to =70°C
V_{CC} Voltage +12V (Pin 25) ..... 12V ± 10%
+5V (pin 19) ..... 5V ± 10%
I(RAMP) Current (Pin 21) ..... 0 to 100µA
Control Voltage Range (Pins 27, 28) ..... 0V to 7V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, $V_{CC} = V_{CC2}$ = 12V, R_{SENSE} = 1Ω, $C_{OTA} = C_{VCO}$ = 0.01µF, C_{OS} = 0.02µF

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator (VCO) Section (Mode 1 or 2 unless otherwise specified)					
Frequency vs. $V_{PIN\ 20}$	$1V \le V_{PIN20} \le 10V$		300		Hz/V
Frequency	V_{VCO} = 6V	1450	1800	2150	Hz
	V_{VCO} = 0.5V	70	140	210	Hz
Reset Voltage at C_{VCO}	Mode = 0		125	250	mV
Sampling Amplifier					
V_{RC}	Mode 0		125	250	mV
I_{RC}	Mode 1, R_{RAMP} = 39KΩ	70	100	130	µA
	Mode 2A, V_{PH2} = 4V	13	50	70	µA
	Mode 2A, V_{PH2} = 6V	–15	2	+15	µA
	Mode 2A, V_{PH2} = 8V	–30	–50	–70	µA
Motor Current Control Section					
I(SENSE) Gain	V_{PIN27} = 5V, $0V \le V_{PIN28} \le 2.5V$	4.5	5	5.5	V/V
One Shot Off Time		12	25	33	µs
I(CMD) Transconductance Gain			0.19		mmho
Power Fail Detection Circuit					
12V Threshold		9.1	9.8	10.5	V
Hysteresis			150		mV
5V Threshold		3.8	4.25	4.5	V
Hysteresis			70		mV
Logic Inputs					
Voltage High (V_{IH})		2			V
Voltage Low (V_{IL})				0.8	V
Current High (I_{IH})	V_{IN} = 2.7V	–10	1	10	µA
Current Low (I_{IL})	V_{IN} = 0.4V	–500	–350	–200	µA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Outputs I(CMD) = I(LIMIT) = 2.5V					
I_{PNP} low		50	75	100	mA
I_{PNP} high	Off State	–100		100	µV
V_N high	V_{PIN8} = 10V	9.7	10	10.3	V
V_N low			0.2	0.7	V
A_V PIN 8 to V_N	V_{PIN8} = 6V	0.95	1	1.05	V/V
LOGIC low	I_{OUT} = 0.5mA			0.4	V
LOGIC I_{OUT} High			5		µA
Supply Currents (N and PNP Outputs Open)					
5V Current			2	4	mA
V_{CC} Current			38	50	mA
V_{CC2} Current			4	10	mA

Note 1. For explanation of states, see Figure 5 and Table 1.

FUNCTIONAL DESCRIPTION

The ML4410 provides closed-loop commutation for 3-phase brushless motors. To accomplish this task, a VCO, integrating Back-EMF Sampling error amplifier and sequencer form a phase-locked loop, locking the VCO to the back-EMF of the motor. The IC also contains circuitry to control motor current with either linear or constant off-time PWM modes. Braking and power fail detection functions are also provided on chip. The ML4410 is designed to drive external power transistors (N-channel MOSFET sinking transistors and PNP sourcing transistors) directly, and contains a special circuit to reduce PNP base currents when output current demand is reduced.

Start-up sequencing and motor speed control are accomplished by a microcontroller. Speed sensing is accomplished by monitoring the output of the VCO, which will be a signal which is phased-locked to the commutation frequency of the motor.

BACK-EMF SENSING AND COMMUTATOR

The ML4410 contains a patented back-EMF sensing circuit which samples the phase which is not energized (Shaded area in figure 2) to determine whether to increase or decrease the commutator (VCO) frequency. A late commutation causes the error amplifier to charge the filter (RC) on pin 20, increasing the VCO input while early commutation causes pin 20 discharge. Analog speed control loops can use pin 20 as a speed feedback voltage.

The input impedance of the three PH inputs is about 8KΩ to GND. When operating with a higher voltage motor, the PH inputs should be divided down in voltage so that the maximum voltage at any PH input does not exceed VCC. See ML4410 data sheet for applications.

VCO AND PHASE DETECTOR CALCULATIONS

The VCO should be set so that at the maximum frequency of operation (the running speed of the motor) the VCO

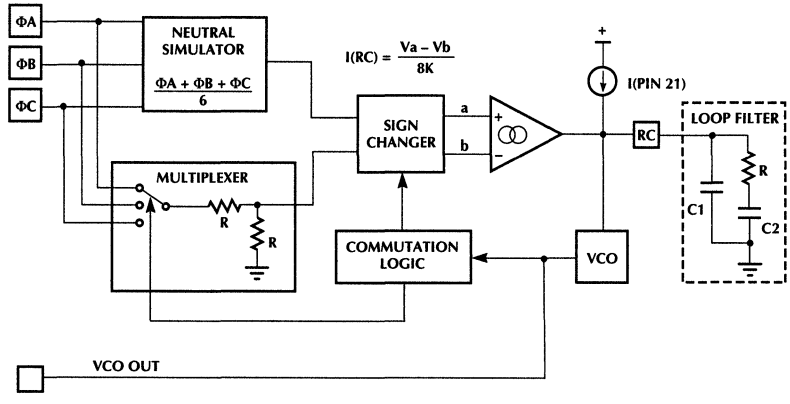


Figure 1. Back EMF Sensing Block Diagram.

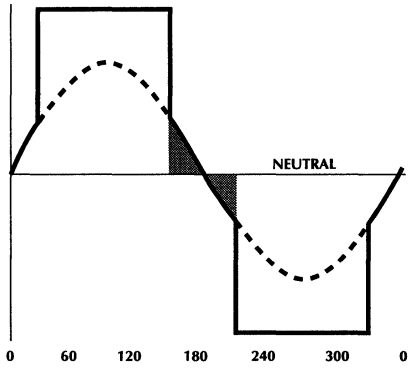


Figure 2. Typical Motor Phase Waveform with Back-EMF Superimposed (Ideal Commutation).

control voltage will be no higher than VCC_{MIN} – 1V. The VCO maximum frequency will be:

$$F_{MAX} = 0.05 \times POLES \times RPM$$

where POLES is the number of poles on the motor and RPM is the maximum motor speed in Revolutions Per Minute.

The minimum VCO gain derived from the specification table (using the minimum F_{VCO} at V_{VCO} = 6V) is:

$$K_{VCO(MIN)} = \frac{2.42 \times 10^{-6}}{C_{VCO}}$$

Assuming that the $V_{VCO(MAX)}$ = 9.5V, then

$$C_{VCO} = \frac{9.5 \times 2.42 \times 10^{-6}}{F_{MAX}}$$

or

$$C_{VCO} = \frac{460}{POLES \times RPM}\ \mu F$$

Figure 4 shows the transfer function of the Phase Lock Loop with the phase detector formed from the sampled phase through the Gm amplifier with the loop filtered formed by R, C1, and C2.

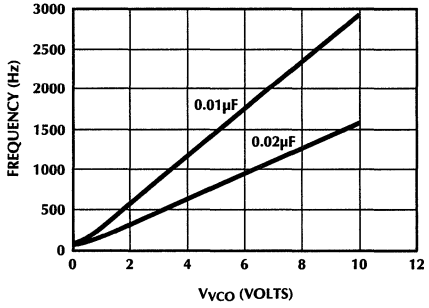


Figure 3. VCO Output Frequency vs. V_{VCO} (Pin 20)

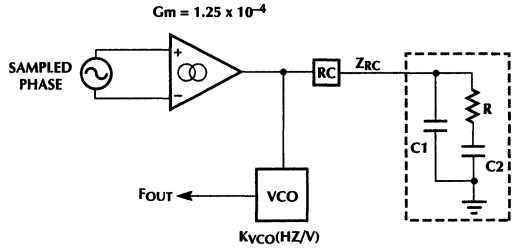


Figure 4. Back EMF Phase Lock Loop Components.

The impedance of the loop filter is

$$Z_{RC}(s) = \frac{1}{C_1 s} \frac{(s + \omega_{LEAD})}{(s + \omega_{LAG})}$$

Where the lead and lag frequencies are set by:

$$\omega_{LEAD} = \frac{1}{RC_2}$$

$$\omega_{LAG} = \frac{C_1 + C_2}{RC_1C_2}$$

START-UP SEQUENCING

When the motor is initially at rest, it is generating no back-EMF. Because a back-EMF signal is required for closed loop commutation, the motor must be started "open-loop" until a velocity sufficient to generate some back-EMF is attained (around 100 RPM). The following steps are a typical procedure for starting a motor which is at rest.

Step 1: The IC is held in reset (state R) with full power applied to the windings (see figure 6). This aligns the rotor to a position which is 30° (electrical) before the center of the first commutation state.

Step 2: Reset is released, and a fixed current is input to pin 21 and appears as a current on pin 20, and will ramp the VCO input voltage, accelerating the motor at a fixed rate.

Step 3: When the motor speed reaches about 100 RPM, the back EMF loop can be closed by pulling pin 18 high.

5

Table 1 Commutation, Braking and PLL States

STATE	OUTPUTS						INPUT SAMPLING
	N1	N2	N3	P1	P2	P3	
R OR 0	OFF	ON	OFF	ON	OFF	ON	N/A
A	OFF	OFF	ON	ON	OFF	OFF	PH2
B	OFF	OFF	ON	OFF	ON	OFF	PH1
C	ON	OFF	OFF	OFF	ON	OFF	PH3
D	ON	OFF	OFF	OFF	OFF	ON	PH2
E	OFF	ON	OFF	OFF	OFF	ON	PH1
F	OFF	ON	OFF	ON	OFF	OFF	PH3

Table 1. Commutation States.

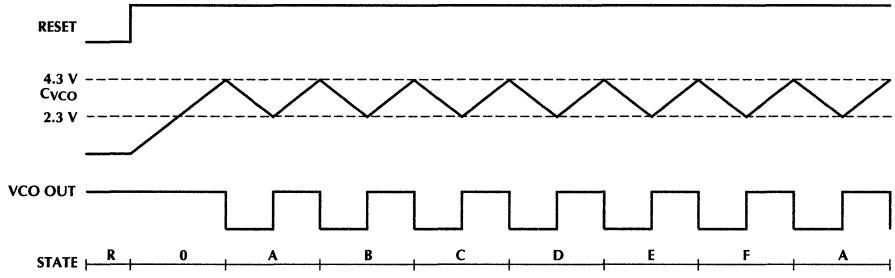


Figure 5. Commutation Timing and Sequencing.

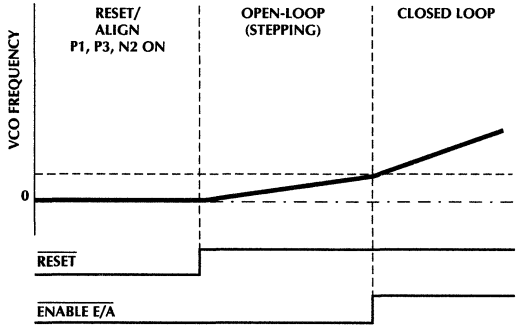


Figure 6. Typical Start-up Sequence.

Using this technique, some reverse rotation is possible. The maximum amount of reverse rotation is 360/N, where N is the number of poles. For an 8 pole motor, 45° reverse rotation is possible.

STEP	PIN 16	PIN 18	PIN 21	I(LIMIT) I(CMD)
1	0	0	FIXED	I_{MAX}
2	1	0	FIXED	I_{MAX}
3	1	1	0	I_{MAX}

Table 2. Start-up Sequence.

ADJUSTING OPEN LOOP STEP RATE

I_{RAMP} should be set so that the VCO's frequency ramp during "open loop stepping" phase of motor starting is less than the motor's acceleration rate. In other words, the motor must be able to keep up with the VCO's ramp rate in open loop stepping mode. The VCO's input voltage ($V_{PIN\ 20}$) ramp rate is given by:

$$\frac{dV_{VCO}}{dt} = \frac{I_{RAMP}}{C_1 + C_2}$$

since

$$F_{VCO} = K_{VCO} \times V_{VCO}$$

$$K_{VCO(MAX)} \approx \frac{4 \times 10^{-6}}{C_{VCO}}$$

then combining the 3 equations I_{RAMP} can be calculated from the desired maximum open loop stepping rate the motor can follow.

$$I_{RAMP} < \frac{dF_{VCO}}{dt} \frac{C_{VCO} \times (C_1 + C_2)}{4 \times 10^{-6}}$$

The motor will start more consistently and tolerate a wider variation in open loop step rate if there is some damping on the motor (such as head drag) during the open loop modes.

The tolerance of the open loop step VCO acceleration $\left(\frac{dF_{VCO}}{dt}\right)$ depends on the tolerances of K_{VCO}, I_{RAMP}, C1, C2, and C_{VCO}. For more optimum spin up times, these variables can be digitally "calibrated" out by the microprocessor using the following procedure:

1. Reset the IC by holding pin 16 low for at least 5µs.
2. Go into open loop step mode with no current on the motor and measure the difference between the first two complete VCO periods with the PWM signal at 50% duty cycle:

   ENABLE E/A = (see below)
   I(CMD) = 0V
   PWM OUT = 50%

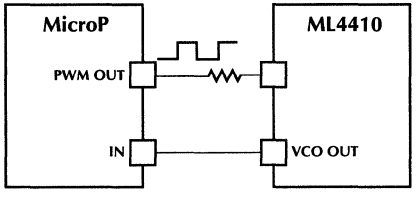


Figure 7. Auto-Calibration of Open-Loop Step Rate.

3. Compute a correction factor to adjust I_{RAMP} current by changing the PWM duty cycle from the Micro (D.C.)

$$D.C.(NEW) = 50\% \times \frac{\Delta F_{VCO}(DESIRED)}{\Delta F_{VCO}(MEASURED)}$$

4. Use new computed duty cycle for open loop stepping mode and proceed with a normal start-up sequence.

If this auto calibration is used ENABLE E/A can be tied permanently high, eliminating a line from the Micro. Since there is offset associated with the Phase Detector Error Amp (E/A), more current than is being injected by I_{RAMP} may be taken out of pin 20 if the offset is positive (into pin 20) if the error amp were enabled during the open loop stepping mode. In that case, V_{VCO} would not rise and the motor would not step properly. The effect of E/A offset can also be canceled out by the auto calibration algorithm described above allowing the E/A to be permanently enabled.

PWM AND LINEAR CURRENT CONTROL

To facilitate speed control, the ML4410 includes two current control loops — linear and PWM (figure 9). The linear control loop senses the motor current on the I(SENSE) terminal through R_{SENSE}. An internal current sense amplifier's (A2) output modulates the gates of the 3 N-channel MOSFET's when OTA OUT is tied to OTA IN, or can modulate a single MOSFET gate tied to OTA OUT. When operated in this mode, OTA IN is tied to 12V, and N1-N3 are saturated switches. This method produces the lowest current ripple at the expense of an extra MOSFET.

The linear current control modulates the gates of the external MOSFET drivers. Amplifier A2 is a transconductance amplifier which amplifies the difference between I(CMD) and I(SENSE). The transconductance gain of A2 is:

$$g_m = 1.875 \times 10^{-4} \mho$$

The current loop is compensated by C_{OTA} which forms a pole given by

$$\omega_P = \frac{9.375 \times 10^{-4}}{C_{OTA}}$$

This time constant should be fast enough so that the current loop settles in less than 10% of T_{VCO} at the highest motor speed to avoid torque ripple to V_{TH} mismatch of the N-Channel MOSFETs, or use a separate MOSFET in series with N1-N3 with a lower time constant.

The ML4410 also includes a current mode constant off-time PWM circuit. When motor current builds to the threshold set on I(LIMIT) input (pin 27), a one-shot is fired whose timing is set by C_{OS}. The current in the motor will be controlled by the lower of pin 27 and pin 28.

The I(SENSE) input pin should be kept below 1V. If I(SENSE) goes above 1V, a bias current of about –300µA will flow out of pin 12 and the N outputs will be inhibited. Bringing I(SENSE) below .7V removes the bias current to its normal level. For this reason, the noise filter resistor on the I(SENSE) pin (1KΩ on Figure 11) should be less than 1.5KΩ.

The noise filter time constant should be less than 1µs to avoid excessive phase shift in the I(SENSE) signal.

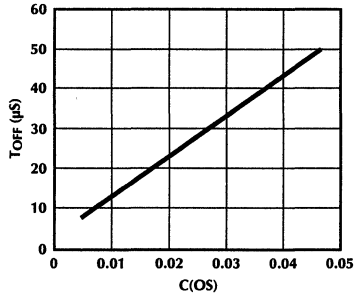


Figure 8. I(LIMIT) Output Off-Time vs. C_{OS}.

OUTPUT DRIVERS

The motor's source transistor drivers are open-collector NPN's with internal 50KΩ pull-up resistors, whose current is controlled according to the current demanded through the motor. To conserve power, the ML4410 sets the current to PNP1, PNP2, and PNP3, proportional to the lower of pin 27 and pin 28.

Drivers N1 through N3 are totem-pole outputs capable of sourcing and sinking 10mA. Switching noise in the external MOSFETs can be reduced by adding resistance in series with the gates.

BRAKING

Applying a 0 on pin 26 activates the braking circuit. The brake circuit turns on PNP1 through PNP3 and turns off NPN1 and NPN3.

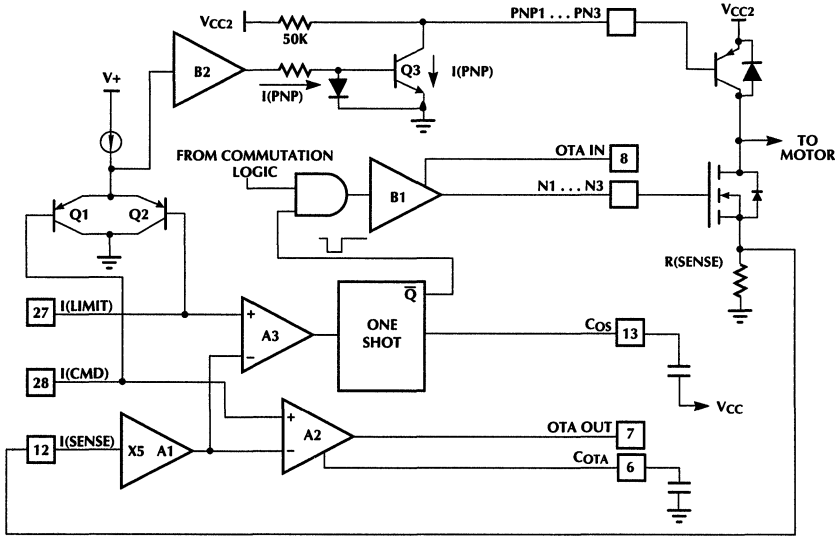


Figure 9. Current Control, Output Drive and Braking Circuits.

APPLICATIONS

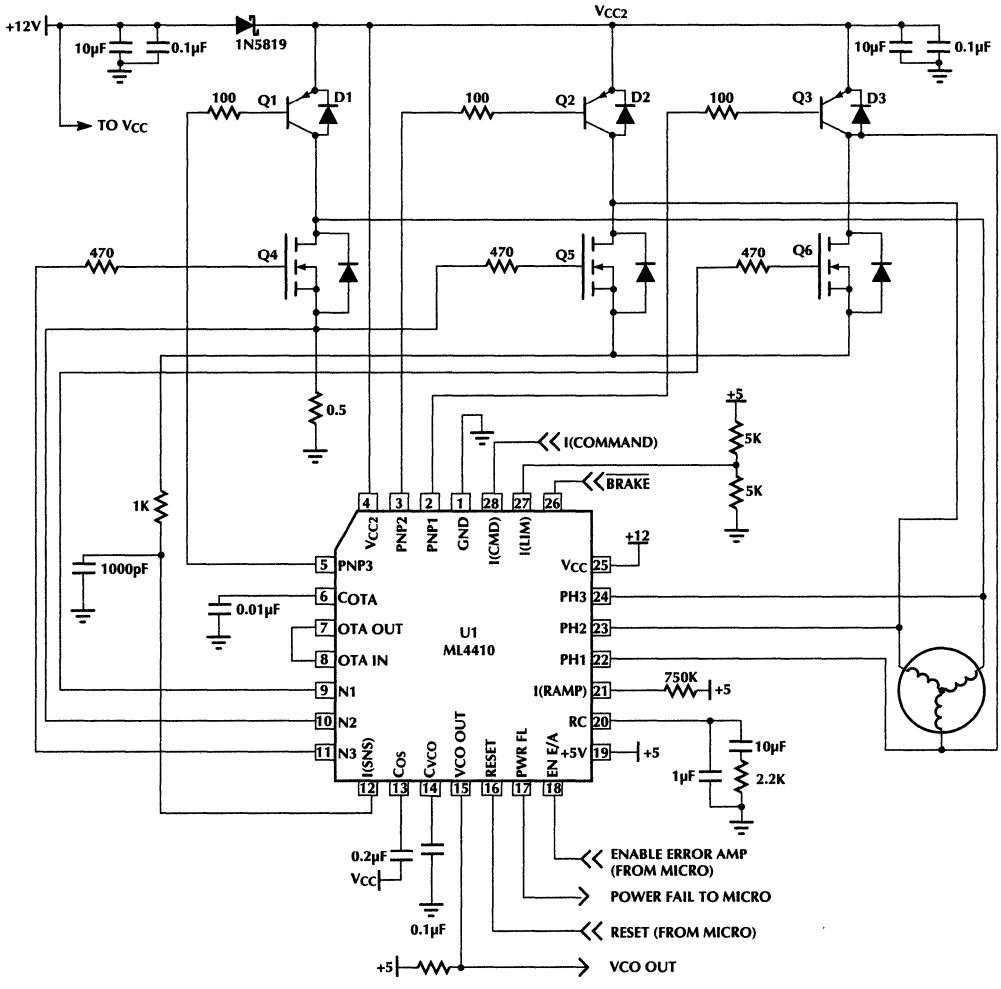


Figure 11. ML4410 Typical Application.

APPLICATIONS (Continued)

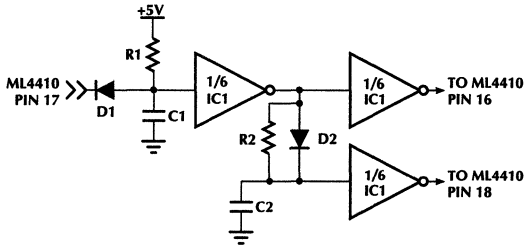
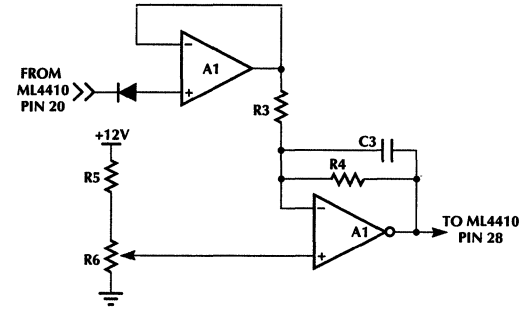


Figure 12. Analog Start-up Circuit.



SYMBOL	VALUE
A1	LM358
Q1	74HC14
D1, D2	1N4148
R1	1MΩ
R2	1MΩ
R3	100KΩ

SYMBOL	VALUE
R4	100KΩ
R5	50KΩ
R6	50KΩ
C1	3.3µF
C2	3.3µF
C3	0.47µF

Figure 13. Analog Speed Control.

Figure 11 shows a typical application of the ML4410 in a hard disk drive spindle control. Although the timing necessary to start the motor in most applications would be generated by a microcontroller, Figure 12 shows a simple "one-shot" start-up timing approach.

Speed control can be accomplished either by:

1. Sensing the VCO OUT frequency with a Microcontroller and adjusting I(CMD) via an analog output from the Micro (PWM DAC).
2. Using analog circuitry for speed control (Figure 13).

OUTPUT STAGE HINTS

Q1, Q2, and Q3 are MJE210 or equivalent. Q4, Q5, and Q6 are IRFU010 or equivalent. Base resistors (100Ω) are included to reduce power dissipation in the IC during start-up. If requested currents are low, these can be eliminated. Switching transients due to commutation can be reduced by increasing the 470Ω gate resistors on Q4-Q6.

Since the output section in a full bridge application consists of three half-H switches, cross-conduction can occur. Cross-conduction is the condition where an N-FET and PNP in the same phase of the bridge conduct simultaneously. This could happen under two conditions (see figure 14):

1. When transitioning from mode 0 to mode A (see table 1) or from braking to mode R, a PNP goes from on to off at the same time N goes from off to on in the same phase. If the PNP turns off slowly and N turns on quickly, cross-conduction may occur. This condition has been prevented inside the IC on later revisions of the ML4410. Consult your Micro Linear representative for date code information. On earlier revision parts, forcing the PNP to turn off more quickly than the NPN turns on will minimize the cross-conduction current.
2. When the MOSFET (or PNP) in the same phase switches on gate current flows due to capacative coupling of current through the FET's drain to gate capacitance (or PNP's Miller Capacitance). This could cause the device that was off to be turned on.

In Condition 2 above, the PNP is pulled up inside the ML4410 with a 50KΩ resistor. If the current through C(CB) is greater than 0.7V ÷ 50K when the N-FET turns on, the PNP could turn on simultaneously, causing cross-conduction. Adding R1 as shown in figure 14 eliminates this. The size of R1 will depend on the fall time of the phase voltage, and the size of the C(CB).

APPLICATIONS (Continued)

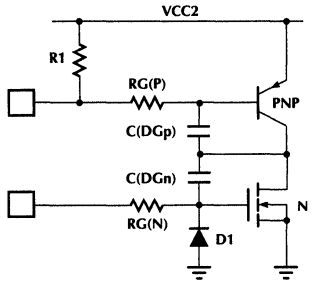


Figure 14. Causes of Cross-conduction.

Adding a series damping resistor to the N-FET gate (RGn) will slow the fall time. The damping resistor should be low enough to:

Avoid turning on the N-Channel gate when the PNP turns on via the same mechanism outlined in condition 2 above

Not severely increase the switching losses in the N-FET

In higher power applications, when large MOSFETs are used, the N-Output can be pulled below GND, causing the internal substrate diode (Dint) to conduct. The negative substrate current should be limited to less than 2mA, which can be done by adding D1 as shown in figure 14. D1 prevents the gate from going below 0.7V, limiting the substrate current to:

$$\frac{V_{BE(D1)} - V_{BE(Dint)}}{RG(N)}$$

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4410CQ	0°C to +70°C	28-Pin Molded PCC (Q28)

ML4411

Sensorless Spindle Motor Controller

GENERAL DESCRIPTION

The 4411 provides complete commutation for delta or wye wound Brushless DC (BLDC) motors without the need for signals from Hall Effect Sensors. This IC senses the back EMF of the 3 motor windings (no neutral required) to determine the proper commutation phase angle using Phase Lock Loop techniques. This technique will commutate virtually any 3-phase BLDC motor and is insensitive to PWM noise and motor snubbing. The ML4411 is architecturally similar to the ML4410 but with improved braking and brown-out recovery circuitry.

Included in the ML4411 is the circuitry necessary for a Hard Disk Drive microcontroller driven control loop. The 4411 controls motor current with either a constant off-time PWM or linear current control driven by the microcontroller. All commutation is performed by the ML4411. Braking and Power Fail are also included in the ML4411.

The timing of the start-up sequencing is determined by the micro, allowing the system to be optimized for a wide range of motors and inertial loads.

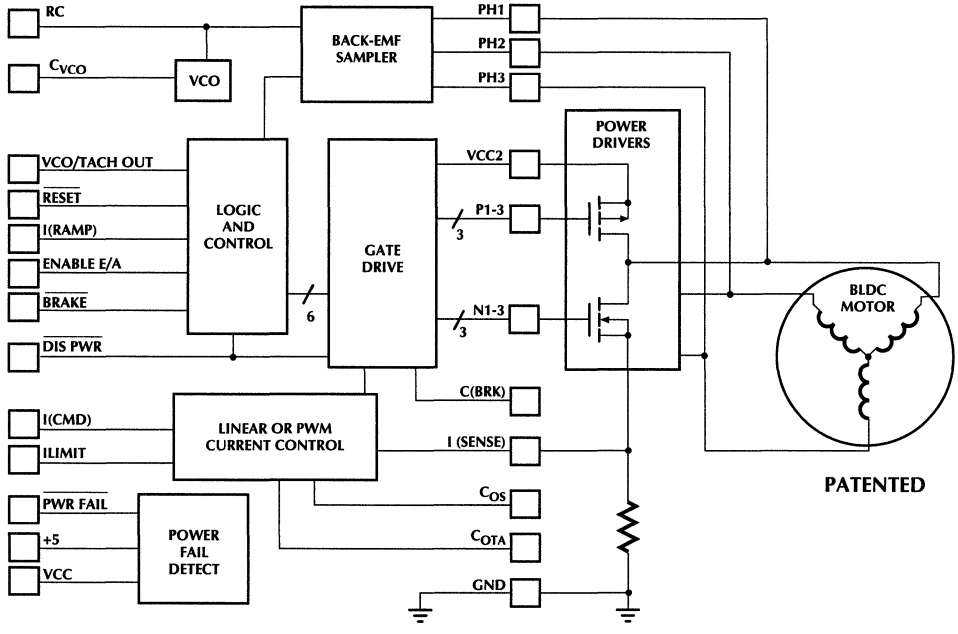
The ML4411 modulates the gates of external N-Channel power MOSFETs to regulate the motor current. The IC drives P-Channel MOSFETs directly.

The ML4411A includes a comparator on the P3 output to prevent cross-conduction.

FEATURES

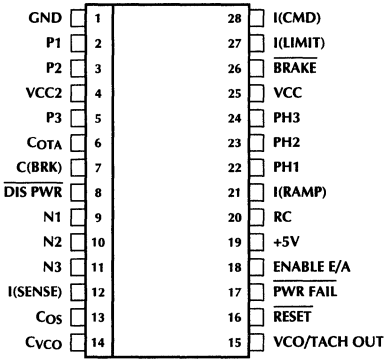
- Back-EMF Commutation Provides Maximum Torque for Minimum "Spin-Up" Time for Spindle Motors
- Accurate, Jitter-Free Phase Locked Motor Speed Feedback Output
- Linear or PWM Motor Current Control
- Easy Microcontroller Interface for Optimized Start-Up Sequencing and Speed Control
- Power Fail Detect Circuit with Delayed Braking
- Drives External N-Channel FETs and P-Channel FETs
- Back-EMF comparator detects motor rotation after power fail for fast re-lock after brownout
- Improved version of ML4411

BLOCK DIAGRAM



PIN CONFIGURATION

ML4411
28-Pin SOIC (S28W)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	GND	Signal and Power Ground
2	P1	Drives the external P-channel transistor driving motor PH1
3	P2	Drives the external P-channel transistor driving motor PH2
4	V_{CC2}	12V power and power for the braking function
5	P3	Drives the external P-channel transistor driving motor PH3
6	C_{OTA}	Compensation capacitor for linear motor current amplifier loop
7	C(BRK)	Capacitor which stores energy to charge N-channel MOSFETs for braking with power off.
8	$\overline{\text{DIS PWR}}$	A logic 0 on this pin turns off the N and P outputs and causes the TACH comparator output to appear on TACH OUT
9-11	N1, N2 N3	Drives the external N-channel MOSFETs for PH1, PH2, PH3
12	I(SENSE)	Motor current sense input
13	C_{OS}	Timing capacitor for fixed off-time PWM current control
14	C_{VCO}	Timing capacitor for VCO
15	VCO/TACH OUT	Logic Output from VCO or TACH comparator
16	$\overline{\text{RESET}}$	Input which holds VCO off and sets the IC to the RESET condition
17	$\overline{\text{PWR FAIL}}$	A "0" output indicates 5V or 12V is under-voltage. This is an open collector output with a 4.5KΩ pull-up to +5V
18	ENABLE E/A	A "1" logic input enables the error amplifier and closes the back-EMF feedback loop
19	+5V	5V power supply input
20	RC	VCO loop filter components
21	I(RAMP)	Current into this pin sets the initial acceleration rate of the VCO during start-up
22	PH1	Motor Terminal 1
23	PH2	Motor Terminal 2
24	PH3	Motor Terminal 3
25	V_{CC}	12V power supply. Terminal which is sensed for power fail
26	$\overline{\text{BRAKE}}$	A "0" activates the braking circuit
27	I(LIMIT)	Sets the threshold for the PWM comparator
28	I(CMD)	Current Command for Linear Current amplifier

5

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (pins 4, 25) 14V
Output Current (pins 2, 3, 5, 9,10,11) ..... ±150mA
Logic Inputs (pins 16, 17, 18, 25) ..... –0.3 to 7V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 150°C
Thermal Resistance (θ_{JA}) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
VCC Voltage +12V (pin 25) ..... 12V ± 10%
+5V (pin 19) ..... 5V ± 10%
I(RAMP) current (Pin 21) ..... 0 to 100µA
I Control Voltage Range (pins 27, 28) ..... 0V to 7V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, $V_{CC} = V_{CC2}$ = 12V, R_{SENSE} = 1Ω, $C_{OTA} = C_{VCO}$ = 0.01µF, C_{OS} = 0.02µF

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator (VCO) Section (V_{PIN16} = 5V)					
Frequency vs. $V_{PIN\ 20}$	$1V \le V_{PIN20} \le 10V$		300		Hz/V
Frequency	V_{VCO} = 6V	1450	1800	2150	Hz
	V_{VCO} = 0.5V	70	140	210	Hz
Reset Voltage at C_{VCO}	Mode = 0		125	250	mV
Sampling Amplifier (Note 1)					
V_{RC}	State R		125	250	mV
I_{RC}	V_{PIN18} = 0V, R_{RAMP} = 39KΩ	70	100	130	µA
	V_{PIN18} = 5V, State A, V_{PH2} = 4V	30	50	90	µA
	V_{PIN18} = 5V, State A, V_{PH2} = 6V	–13	2	13	µA
	V_{PIN18} = 5V, State A, V_{PH2} = 8V	–30	–50	–90	µA
V_{PIN21}	R_{PIN21} = 39KΩ to +5V	1.0	1.1	1.20	V
Motor Current Control Section					
I(SENSE) Gain	V_{PIN27} = 5V, $0V \le V_{PIN28} \le 2.5V$	4.5	5	5.5	V/V
One Shot Off Time		12	25	33	µs
I(CMD) Transconductance Gain			0.19		mmho
I(CMD), I(LIM) Bias Current	V_{IN} = 0	0	–100	–400	nA
Power Fail Detection Circuit					
12V Threshold		9.1	9.8	10.5	V
Hysteresis			150		mV
5V Threshold		3.8	4.25	4.5	V
Hysteresis			70		mV
Logic Inputs					
Voltage High (V_{IH})		2			V
Voltage Low (V_{IL})				0.8	V
Current High (I_{IH})	V_{IN} = 2.7V	–10	1	10	µA
Current Low (I_{IL})	V_{IN} = 0.4V	–500	–350	–200	µA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Braking Circuit (V_{PIN17} = 0V)					
Brake Active Threshold		0.8	1.2	1.6	V
PIN 26 Bias Current	V_{PIN26} = 0V		0.3	1	µA
N-Channel Leakage	V_{CC}, V_{CC2} = 0V V_{PIN17} = 0V, V_N = 4V	0	0.06	10	nA
C(BRK) Current	V_{CC}, V_{CC2} = 0V, V_{PIN26} = 3V V_{PIN7} = 6V		20	85	µA
Outputs (I_{CMD} = I_{LIMIT} = 2.5V)					
I_P Low	V_P = 0.8V	5	7	19.5	mA
	V_P = 0.4V	2	4		mA
V_P High	I_P = –10µA	V_{CC} – 0.4			V
P3 Comparator Threshold		V_{CC2} – 1.6		V_{CC2} – 0.8	V
V_N High	V_{PIN12} = 0V	V_{CC2} – 3.2	10	V_{CC} – 1.2	V
V_N Low	I_N = 1mA		0.2	0.7	V
LOGIC Low (V_{OL})	I_{OUT} = 0.4mA			0.5	V
VCO/TACH V_{OH}	I_{OUT} = –100µA	2.4			V
POWER FAIL V_{OH}	I_{OUT} = –10µA	V_{PIN19} – 0.2	V_{PIN19} – 0.1	V_{PIN19}	V
Supply Currents (N and P Outputs Open)					
5V Current			3	4	mA
V_{CC} Current			38	50	mA
V_{CC2} Current	ML4411		2	3	mA
V_{CC2} Current	ML4411A		2.6	3.75	mA

Note 1. For explanation of states, see Figure 5 and Table 1

FUNCTIONAL DESCRIPTION

The ML4411 provides closed-loop commutation for 3-phase brushless motors. To accomplish this task, a VCO, integrating Back-EMF Sampling error amplifier and sequencer form a phase-locked loop, locking the VCO to the back-EMF of the motor. The IC also contains circuitry to control motor current with either linear or constant off-time PWM modes. Braking and power fail detection functions are also provided on chip. The ML4411 is designed to drive external power transistors (N-channel sinking transistors and PNP sourcing transistors) directly.

Start-up sequencing and motor speed control are accomplished by a microcontroller. Speed sensing is accomplished by monitoring the output of the VCO, which will be a signal which is phased-locked to the commutation frequency of the motor.

BACK-EMF SENSING AND COMMUTATOR

The ML4411 contains a patented back-EMF sensing circuit which samples the phase which is not energized (Shaded area in figure 2) to determine whether to increase or decrease the commutator (VCO) frequency. A late commutation causes the error amplifier to charge the filter (RC) on pin 20, increasing the VCO input while early commutation causes pin 20 discharge. Analog speed control loops can use pin 20 as a speed feedback voltage.

The input impedance of the three PH inputs is about 8KΩ to GND. When operating with a higher voltage motor, the PH inputs should be divided down in voltage so that the maximum voltage at any PH input does not exceed VCC.

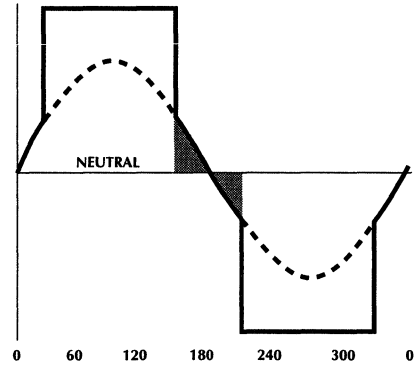


Figure 2. Typical motor phase waveform with Back-EMF superimposed (Ideal Commutation)

VCO AND PHASE DETECTOR CALCULATIONS

The VCO should be set so that at the maximum frequency of operation (the running speed of the motor) the VCO control voltage will be no higher than VCC_{MIN} – 1V. The VCO maximum frequency will be:

$$F_{MAX} = 0.05 \times POLES \times RPM$$

where POLES is the number of poles on the motor and RPM is the maximum motor speed in Revolutions Per Minute.

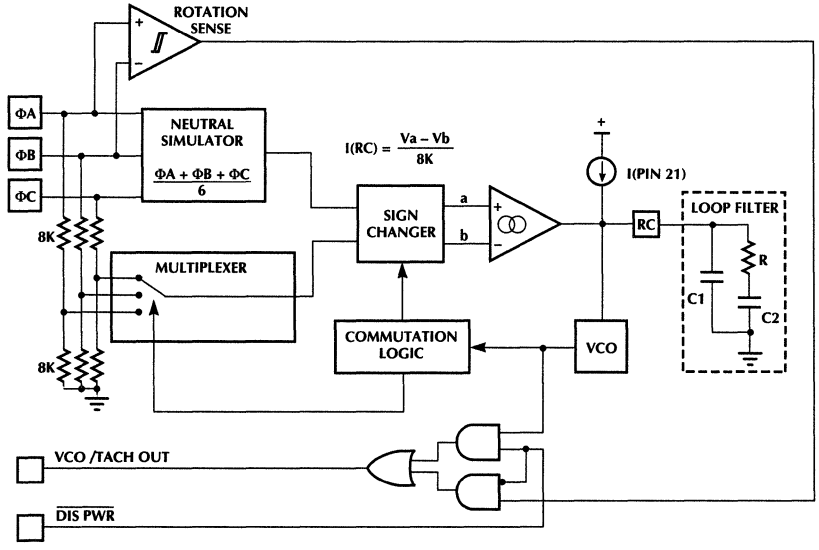


FIGURE 1. BACK EMKF sensing block diagram

The minimum VCO gain derived from the specification table (using the minimum Fvco at V_{VCO} = 6V) is:

$$K_{VCO(MIN)} = \frac{2.42 \times 10^{-6}}{C_{VCO}}$$

Assuming that the $V_{VCO(MAX)}$ = 9.5V, then

$$C_{VCO} = \frac{9.5 \times 2.42 \times 10^{-6}}{F_{MAX}}$$

or

$$C_{VCO} = \frac{460}{POLES \times RPM}\ \mu F$$

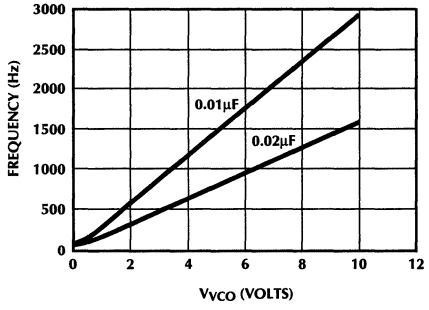


Figure 3. VCO Output Frequency vs. V_{VCO} (Pin 20)

Figure 4 shows the transfer function of the Phase Lock Loop with the phase detector formed from the sampled phase through the Gm amplifier with the loop filtered formed by R, C1, and C2.

The impedance of the loop filter is

$$Z_{RC}(s) = \frac{1}{C_1 s} \frac{(s + \omega_{LEAD})}{(s + \omega_{LAG})}$$

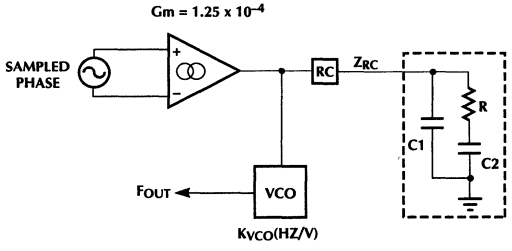


Figure 4. Back EMF Phase Lock Loop Components

Where the lead and lag frequencies are set by:

$$\omega_{LEAD} = \frac{1}{RC_2}$$

$$\omega_{LAG} = \frac{C_1 + C_2}{RC_1C_2}$$

START-UP SEQUENCING

When the motor is initially at rest, it is generating no back-EMF. Because a back-EMF signal is required for closed loop commutation, the motor must be started "open-loop" until a velocity sufficient to generate some back-EMF is attained (around 100 RPM). The following steps are a typical procedure for starting a motor which is at rest.

Step 1: The IC is held in reset (state R) with full power applied to the windings (see figure 6). This aligns the rotor to a position which is 30° (electrical) before the center of the first commutation state.

Step 2: Reset is released, and a fixed current is input to pin 21 and appears as a current on pin 20, and will ramp the VCO input voltage, accelerating the motor at a fixed rate.

Step 3: When the motor speed reaches about 100 RPM, the back EMF loop can be closed by pulling pin 18 high.

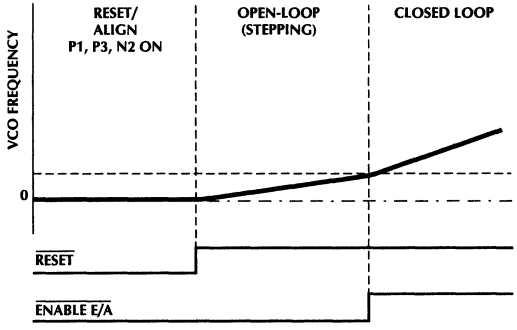


Figure 6. Typical Start-up Sequence.

Using this technique, some reverse rotation is possible. The maximum amount of reverse rotation is 360/N, where N is the number of poles. For an 8 pole motor, 45° reverse rotation is possible.

For quick recovery following a momentary power failure, the following steps can be taken:

STEP	PIN 16	PIN 18	PIN 21	I(LIMIT) I(CMD)
1	0	0	FIXED	I_{MAX}
2	1	0	FIXED	I_{MAX}
3	1	1	0	I_{MAX}

Table 2. Start-up Sequence.

5

STATE	OUTPUTS						INPUT SAMPLING
	N1	N2	N3	P1	P2	P3	
R OR 0	OFF	ON	OFF	ON	OFF	ON	N/A
A	OFF	OFF	ON	ON	OFF	OFF	PH2
B	OFF	OFF	ON	OFF	ON	OFF	PH1
C	ON	OFF	OFF	OFF	ON	OFF	PH3
D	ON	OFF	OFF	OFF	OFF	ON	PH2
E	OFF	ON	OFF	OFF	OFF	ON	PH1
F	OFF	ON	OFF	ON	OFF	OFF	PH3

Table 1. Commutation States.

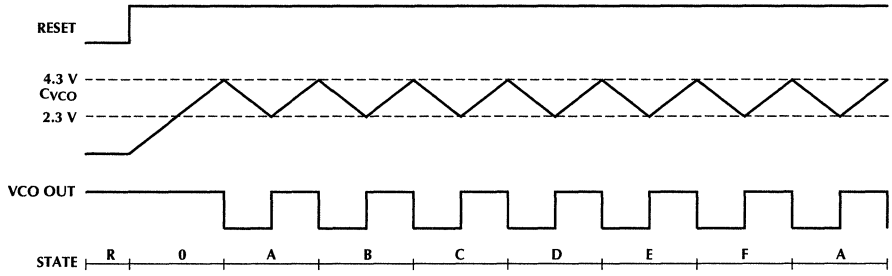


Figure 5. Commutation Timing and Sequencing.

Step 1a: The IC is held in reset (state R) with I(CMD) low and DIS PWR low. The Micro Processor monitors the VCO/TACH OUT pin to determine if a signal is present. If a signal is present, the frequency is determined (by measuring the period). If a signal is not present, proceed to the routine described above for starting a motor which is a rest.

Step 2a: Release RESET and DIS PWR. Apply a current to pin 21 and monitor the VCO/TACH OUT pin for VCO frequency.

Step 3a: When the VCO frequency approaches 6 X the motor frequency (or where the motor frequency has decelerated to by coasting during the time the VCO frequency was ramping up) the back EMF loop can be closed by pulling pin 18 high and motor current brought up with I(CMD) or I(LIMIT).

ADJUSTING OPEN LOOP STEP RATE

I_{RAMP} should be set so that the VCO's frequency ramp during "open loop stepping" phase of motor starting is less than the motor's acceleration rate. In other words, the motor must be able to keep up with the VCO's ramp rate in open loop stepping mode. The VCO's input voltage ($V_{PIN\ 20}$) ramp rate is given by:

$$\frac{dV_{VCO}}{dt} \approx \frac{I_{RAMP}}{C_1 + C_2}$$

since

$$F_{VCO} = K_{VCO} \times V_{VCO}$$

$$K_{VCO(MAX)} = \frac{4 \times 10^{-6}}{C_{VCO}}$$

then combining the 3 equations I_{RAMP} can be calculated from the desired maximum open loop stepping rate the motor can follow.

$$I_{RAMP} < \frac{dF_{VCO}}{dt} \frac{C_{VCO} \times (C_1 + C_2)}{4 \times 10^{-6}}$$

The motor will start more consistently and tolerate a wider variation in open loop step rate if there is some damping on the motor (such as head drag) during the open loop modes.

The tolerance of the open loop step VCO acceleration $\left(\frac{dF_{VCO}}{dt}\right)$ depends on the tolerances of K_{VCO}, I_{RAMP}, C1, C2, and C_{VCO}. For more optimum spin up times, these variables can be digitally "calibrated" out by the microprocessor using the following procedure:

1. Reset the IC by holding pin 16 low for at least 5µs.
2. Go into open loop step mode with no current on the motor and measure the difference between the first two complete VCO periods with the PWM signal at 50% duty cycle:

   ENABLE E/A = (see below)
   I(CMD) = 0V
   PWM OUT = 50%

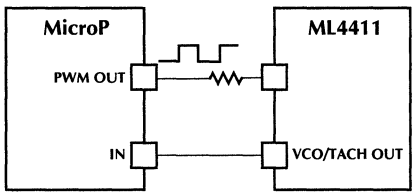


Figure 7. Auto-Calibration of Open-Loop Step Rate.

3. Compute a correction factor to adjust I_{RAMP} current by changing the PWM duty cycle from the Micro (D.C.)

$$D.C.(NEW) = 50\% \times \frac{\Delta F_{VCO}(DESIRED)}{\Delta F_{VCO}(MEASURED)}$$

4. Use new computed duty cycle for open loop stepping mode and proceed with a normal start-up sequence.

If this auto calibration is used ENABLE E/A can be tied permanently high, eliminating a line from the Micro. Since there is offset associated with the Phase Detector Error Amp (E/A), more current than is being injected by I_{RAMP} may be taken out of pin 20 if the offset is positive (into pin 20) if the error amp were enabled during the open loop stepping mode. In that case, V_{VCO} would not rise and the motor would not step properly. The effect of E/A offset can also be canceled out by the auto calibration algorithm described above allowing the E/A to be permanently enabled.

$$A_V = \frac{1.875 \times 10^{-4}}{sC_{OTA}}$$

PWM AND LINEAR CURRENT CONTROL

To facilitate speed control, the ML4411 includes two current control loops — linear and PWM (figure 9). The linear control loop senses the motor current on the I(SENSE) terminal through R_{SENSE}. An internal current sense amplifier's (A2) output modulates the gates of the 3 N-channel MOSFET's when OTA OUT is tied to OTA IN, or can modulate a single MOSFET gate tied to OTA OUT. When operated in this mode, OTA IN is tied to 12V, and N1-N3 are saturated switches. This method produces the lowest current ripple at the expense of an extra MOSFET.

The linear current control modulates the gates of the external MOSFET drivers. Amplifier A2 is a transconductance amplifier which amplifies the difference between I(CMD) and I(SENSE). The transconductance gain of A2 is:

$$g_m = 1.875 \times 10^{-4}\ \mho$$

The current loop is compensated by C_{OTA} which forms a pole given by

$$\omega_P = \frac{9.375 \times 10^{-4}}{C_{OTA}}$$

This time constant should be fast enough so that the current loop settles in less than 10% of T_{VCO} at the highest motor speed to avoid torque ripple to V_{TH} mismatch of the N-Channel MOSFETs.

The I(SENSE) input pin should be kept below 1V. If I(SENSE) goes above 1V, a bias current of about –300µA will flow out of pin 12 and the N outputs will be inhibited. Bringing I(SENSE) below 0.7V removes the bias current to its normal level. For this reason, the noise filter resistor on the I(SENSE) pin (1KΩ on Figure 10) should be less than 1.5KΩ.

The noise filter time constant should be great enough to filter the leading edge current spike when the N-FETs turn on but small enough to avoid excessive phase shift in the I(SENSE) signal.

OUTPUT DRIVERS

The motor's source drivers (P1 thru P3) are open-collector NPN's with internal 16KΩ pull-up resistors. N3is inhibited until P3 is within 1.4V (typ) of V_{CC2} on the ML4411A.

Drivers N1 through N3 are totem-pole outputs capable of sourcing and sinking 10mA. Switching noise in the external MOSFETs can be reduced by adding resistance in series with the gates.

BRAKING

As shown in figure 9, the braking circuit pulls the N-Channel MOSFET gates high when BRAKE falls below a 1.4V threshold. After a power failure, C(DLY) is discharged slowly through R(DLY) providing a delay for retract to occur before the braking circuit is activated. The N-Channel buffer (B1) tri-states when the BRAKE pin reaches 2.1V to ensure that no charge from C(BRK) is lost through the pull-down transistor in B1. To brake the motor with external signals, first disable power by pulling pin 8 low, then pull pin 26 below 1.4V using an open drain (or diode isolated) output.

The bias current for the Braking circuits comes from VCC2. When the N-Channel MOSFETs turn on, no additional power is generated for VCC2 (motor back-EMF rectified through out the MOSFET body diodes). After VCC2 drops below 4V, Q2 turns off. Continued braking relies on the C_{GS} of the N-Channel MOSFETs to sustain the MOSFET gate enhancement voltage.

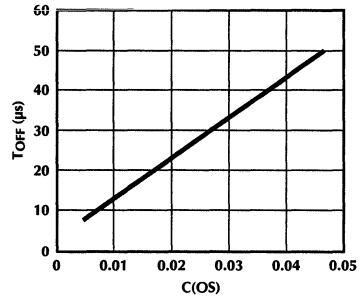


Figure 8. I(LIMIT) Output Off-Time vs. C_{OS}.

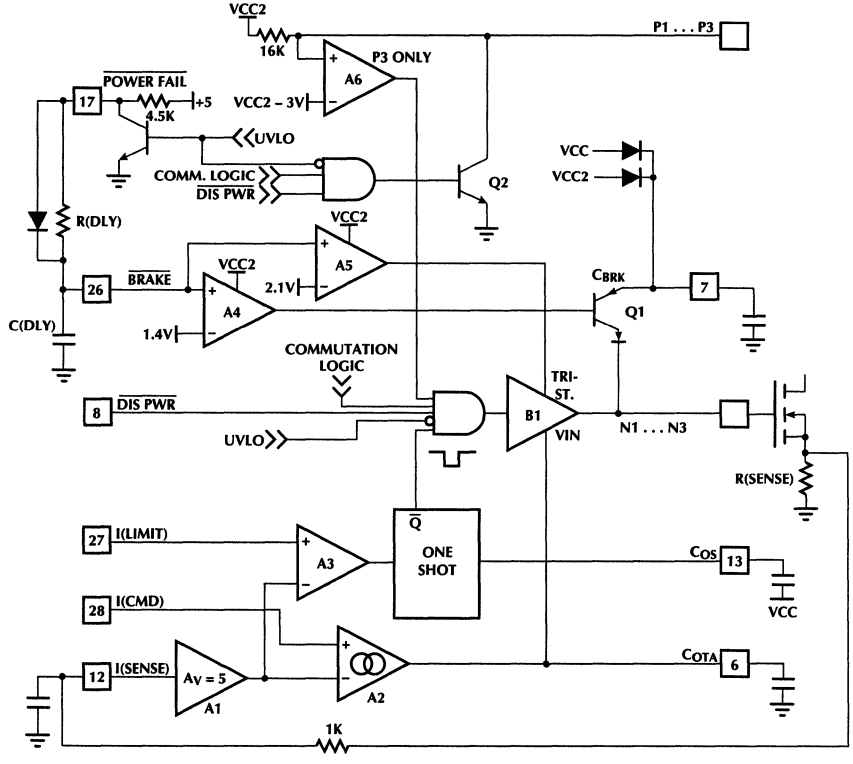


Figure 9. Current Control, Output Drive and Braking Circuits.

APPLICATIONS

Figure 10 shows a typical application of the ML4411 in a hard disk drive spindle control. Although the timing necessary to start the motor in most applications would be generated by a microcontroller, Fig. 11 shows a simple "one shot" start-up timing approach.

Speed control can be accomplished either by:

1. Sensing the VCO OUT frequency with a Microcontroller and adjusting I(CMD) via an analog output form the Micro (PWM DAC).
2. Using analog circuitry for speed control. (Fig. 12).

OUTPUT STAGE HINTS

In the circuit in Figure 10, Q1, Q2, and Q3 are IRFR9024 or equivalent. Q4, Q5, and Q6 are IRFR024 or equivalent. New MOSFET packaging technology such as the Little Foot® series may decrease the PC board space. These packages, however have much lower thermal inertia and dissipation capabilities than the larger packages, and care should be taken not to exceed their rated current and junction temperature.

Since the output section in a full bridge application consists of three half-H switches, cross-conduction can occur. Cross-conduction is the condition where an N-FET and P-FET in the same phase of the bridge conduct simultaneously. This could happen under two conditions (see figure 13):

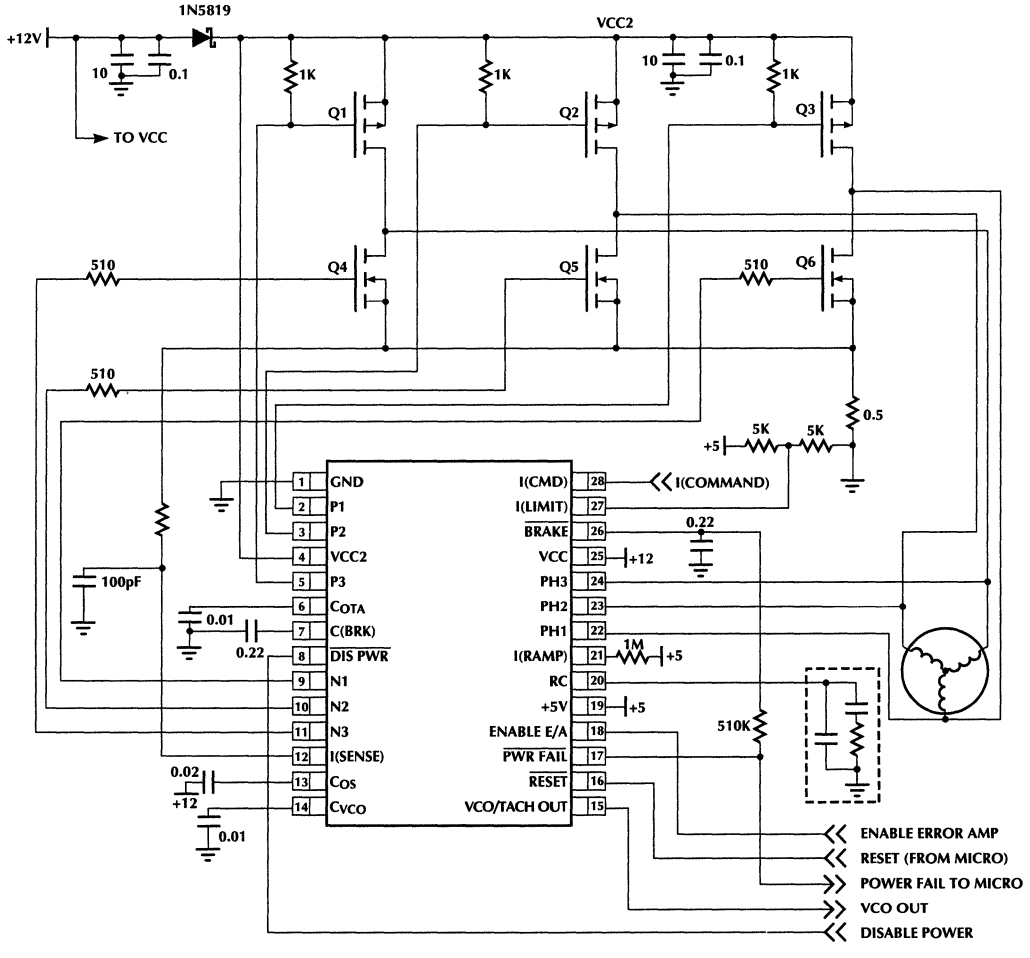


Figure 10. ML4411 Typical Application

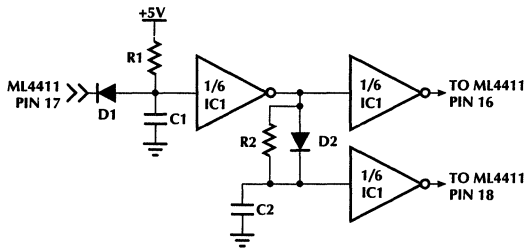
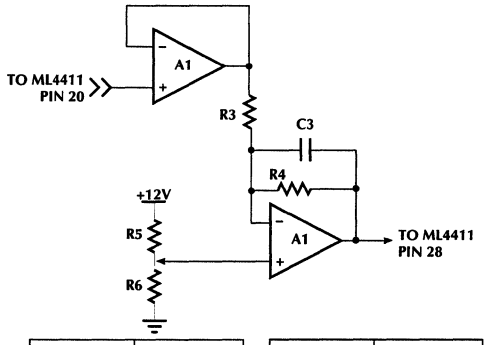


Figure 11. Analog Start-up Circuit



SYMBOL	VALUE
A1	LM358
IC1	74HC14
D1, D2	IN4148
R1	1MΩ
R2	1MΩ
R3	100KΩ

SYMBOL	VALUE
R4	100KΩ
R5	50KΩ
R6	50KΩ
C1	3.3µF
C2	3.3µF
C3	0.47µF

Figure 12. Analog Speed Control

1. When transitioning from mode 0 to mode A (see table 1) P3 goes from on to off at the same time N3 goes from off to on. If the P3 turns off slowly and N3 turns on quickly, cross-conduction may occur. This condition has been prevented inside the IC on the ML4411A through the addition of comparator A6 on the P3 output (Figure 9). This comparator may cause an oscillation when the N3 switches on due to the capacitive coupling effect described below pulling the P3 pin below VCC2-1.4V. To avoid this, use the circuit in Figure 13.
2. When the MOSFET in the same phase switches on gate current flows due to capacitive coupling of current through the MOSFET's drain to gate capacitance. This could cause the device that was off to be turned on.

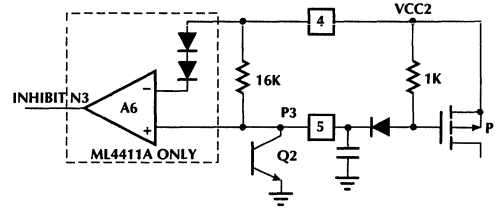


Figure 13. Alternate cross-conduction prevention for ML4411A

In Condition 2 above, the P-Channel MOSFET is pulled up inside the ML4411 with a 16KΩ resistor. If the current through C(CGp) is greater than V_{TH} ÷ 16K when the N-FET turns on, the P-FET could turn on simultaneously, causing cross-conduction. Adding R1 as shown in Figure 14 eliminates this. The size of R1 will depend on the fall time of the phase voltage, and the size of the C(DGp). D1 may be needed for high power applications to limit the negative current pulled (through C(DGn)) out of the substrate diode in the ML4411 when P-FET turns off.

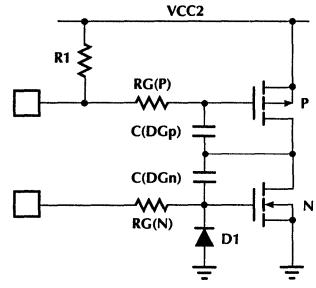


Figure 14. Causes of Cross-conduction

Adding a series damping resistor to the N-FET gate (RGn) will slow the fall time. The damping resistor should be low enough to:

Avoid turning on the N-Channel gate when the PNP turns on via the same mechanism outlined in condition 2 above

Not severely increase the switching losses in the N-FET

UNIPOLAR OPERATION

Unipolar mode offers the potential advantage of lower motor drive cost by only requiring the use of 3 transistors to drive the motor. The ML4411 will operate in unipolar mode (Figure 15) provided the following precautions are taken:

1. The IC supplies should not exceed 12V + 10%.
2. The phase pins on the IC should not exceed the supply voltage.

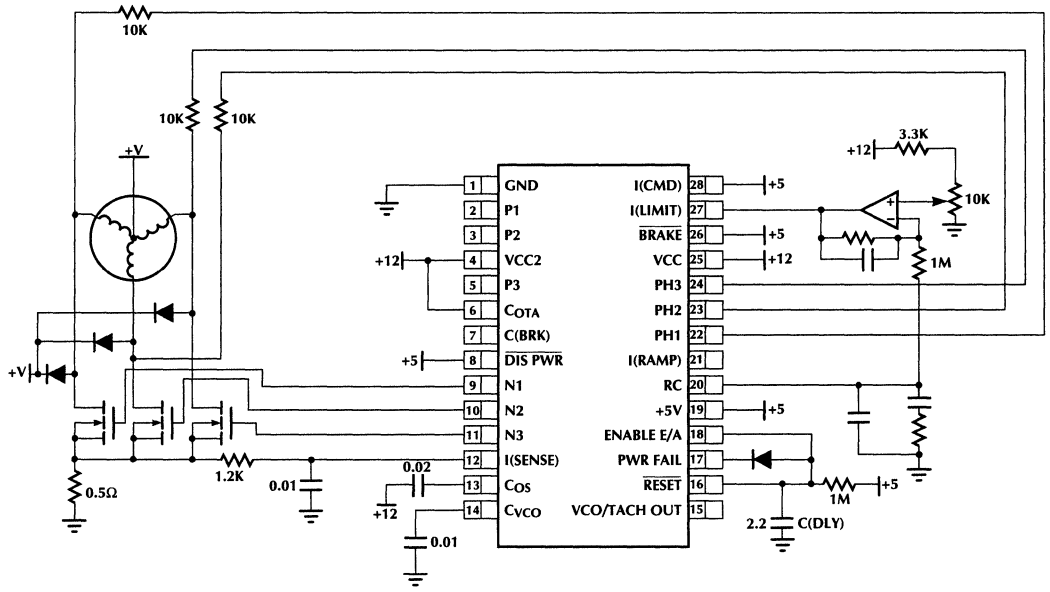


Figure 15. ML4411 Unipolar Drive Application

In unipolar operation, the motor's windings must be allowed to drive freely to:

$$V_{\Phi(MAX)} = V_{SUPPLY\ (MAX)} + V_{EMF\ (MAX)}$$

Therefore, there can be no diodes to clamp the inductive energy to V_{SUPPLY}. This energy must be clamped, however, to avoid an over-voltage condition on the MOSFETs and other components. Typically, a V_{CLAMP} voltage is created to provide the clamping voltage. The inductive energy may either be dissipated (Figure 16) or alternately efficiently regenerated back to the system supply (Figure 17).

The circuit in Figure 15 is designed to minimize the external components necessary, at some compromise to performance. The 3 resistors from the motor phase windings to the PH inputs work with the ML4411's 8KΩ internal resistance to ground to divide the motor's phase voltage down, providing input signals that do not exceed 12V.

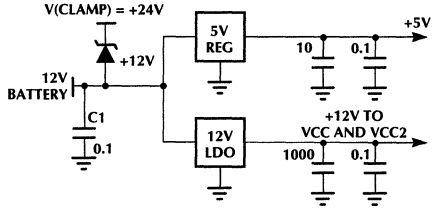


Figure 16. Dissipative Clamping Technique

This circuit uses analog speed regulation. The 1MμΩ resistor from Pin 20 to the speed regulation op amp provides the function of injecting current into the VCO loop filter for the open loop stepping phase of start-up operation. The "one shot" circuitry to time the reset is replaced by a diode and RC delay from the rising edge or the POWERFAIL signal. The error amplifier is left enabled continuously since at low speeds its current contribution is negligible. The current injected into the loop filter must be greater than the leakage current from the phase detector amplifier for the motor to start reliably.

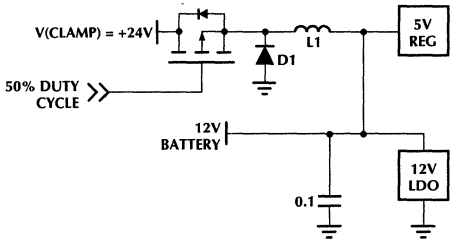


Figure 17. Non-Dissipative Clamping Technique

HIGHER VOLTAGE MOTOR DRIVE

To drive a higher voltage motor, the same precautions regarding ML4411 voltage limitations as were outlined for Unipolar drive above should be followed. Figures 14–16 provide several methods of translating the ML4411's P outputs to drive a higher voltage.

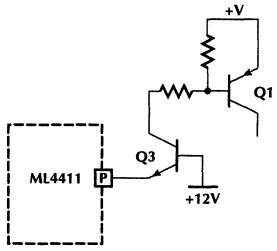


Figure 18. High Voltage Translation using PNP Power Transistor

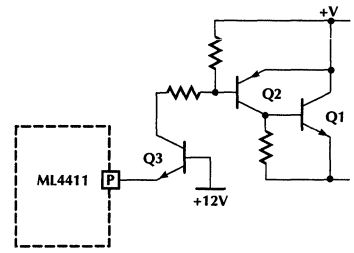


Figure 19. High Voltage Translation using "Composite" PNP Power Transistor

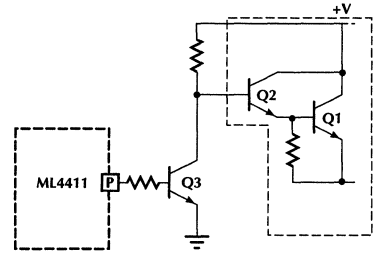


Figure 20. High Voltage Translation with NPN Darlington

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4411CS	0°C to +70°C	28-Pin SOIC (S28W)

Enhanced Sensorless BLDC Motor Controller

GENERAL DESCRIPTION

The ML4412 motor controller provides complete commutation for delta or wye wound Brushless DC (BLDC) motors without the need for signals from Hall Effect Sensors to indicate rotor position. It senses the back EMF of the motor windings (no neutral required) to determine the proper commutation phase sequence using PLL techniques. The ML4412 uses a patented Back-EMF sensing technique which will commutate virtually any 3-phase BLDC motor and is insensitive to PWM noise and motor snubbing circuitry.

The ML4412 controls the motor current with a constant off-time PWM or with a microprocessor controlled linear current. The velocity loop can be controlled with an external microprocessor or through an analog feedback loop. An accurate, jitter-free, VCO output is provided, equal to the commutation frequency of the motor. The ML4412 modulates the gates of external N-channel power MOSFETs to regulate the motor current and directly drives the P-channel MOSFETs. The ML4412 supports enhancements like a blanker circuit to prevent false retriggering of the one shot during a motor current spike and circuitry to ensure that there is no shoot through in any state.

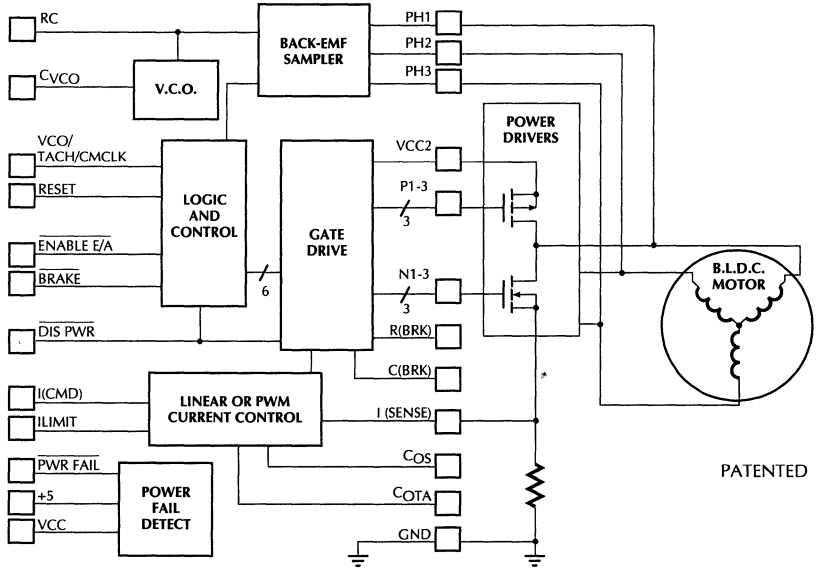
The start-up algorithm consists of measuring a fixed VCO frequency and externally ramping the commutation clock until it is equal to the VCO frequency. The timing of the start-up sequencing is determined by the microprocessor thus allowing the optimization for a wide range of motors and inertial loads.

FEATURES

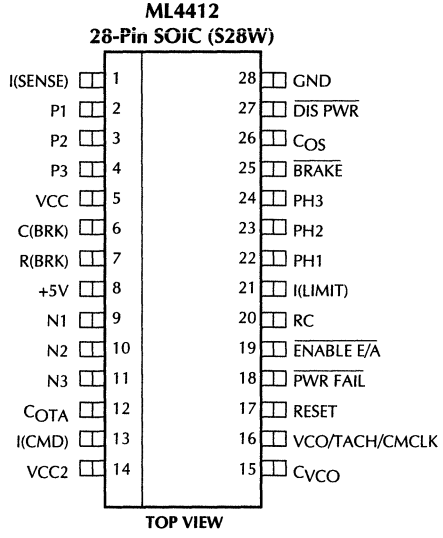
- Less than 200mW power dissipation
- Patented Back-EMF commutation technique provides jitterless torque for minimum "spin-up" time
- Linear or PWM motor current control
- Microprocessor based start-up algorithm allows for optimized start-up sequencing, speed control and support for variable motor loads
- Back-EMF comparator output senses motor rotation after power fail for fast re-lock after brownout
- Onboard power fail detect monitor
- Onboard motor braking circuit allows 'life' braking on command
- Drives external N-ch & P-ch FETs
- Enhanced version of the ML4410 & ML4411

5

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	I(SENSE)	Motor current sense input
2	P1	Drives the external P-Channel transistor driving motor PH1
3	P2	Drives the external P-Channel transistor driving motor PH2
4	P3	Drives the external P-Channel transistor driving motor PH3
5	VCC	12V power supply. Terminal which is sensed for power fail
6	C(BRK)	Capacitor which stores energy to charge N-Channel MOSFETs for braking with power off
7	R(BRK)	External resistor to C(BRK) to drive NMOS during braking
8	+5V	5V power supply input
9-11	N1, N2 N3	Drives the external N-channel MOSFETs for PH1, PH2, PH3
12	C_{OTA}	Compensation capacitor for linear motor current amplifier loop
13	I(CMD)	Current Command for Linear Current amplifier
14	VCC2	12V power and power for the braking function
15	C_{VCO}	Timing capacitor for VCO
16	VCO/TACH/ CMCLK	Logic Output from VCO or TACH comparator, or serves as an input pin for the commutation clock used in start-up sequencing
17	RESET	Input which holds the VCO off and sets the IC to the RESET condition (refer table 1)
18	$\overline{\text{PWR FAIL}}$	A "0" output indicates 5V or 12V is under-voltage. This is an open collector output with a 4.5kΩ pull-up to +5V
19	$\overline{\text{ENABLE E/A}}$	A "0" logic input enables the error amplifier and closes the Back-EMF feedback loop (refer table 1)
20	RC	VCO loop filter components
21	I(LIMIT)	Sets the threshold for the PWM comparator
22	PH1	Motor Terminal 1
23	PH2	Motor Terminal 2
24	PH3	Motor Terminal 3
25	$\overline{\text{BRAKE}}$	A "0" activates the braking circuit
26	C_{OS}	Timing capacitor to GND and resistor to +5V, for fixed off-time PWM current control
27	$\overline{\text{DIS PWR}}$	A logic 0 on this pin turns off the N and P outputs and causes the TACH comparator output to appear on TACH OUT
28	GND	Signal and Power Ground

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (pins 5, 14) 14V
Output Current (pins 2, 3, 4, 9,10,11) ..... ±150mA
Logic Inputs (pins 14, 17, 18, 25) ..... –0.3 to 7V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 150°C
Thermal Resistance (θ_{JA}) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
VCC Voltage +12V (pin 14) ..... 12V ± 10%
+5V (pin 8) ..... 5V ± 10%
I Control Voltage Range (pins 13, 21) ..... 0V to 7V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, VCC = VCC2 = 12V, R_{SENSE} = 1Ω, C_{OTA} = C_{VCO} = 0.01µF, C_{OS} = 0.001µF, R_{OS} = 10kΩ

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator (VCO) Section					
Frequency vs. V_{PIN20}	$1V \le V_{PIN20} \le 10V$		300		Hz/V
Frequency	V_{VCO} = 6V	1450	1800	2150	Hz
	Reset mode	70	140	210	Hz
Sampling Amplifier (note 1)					
V_{RC}	State R	400	500	600	mV
I_{RC}	State A, V_{PH2} = 4V	30	50	70	µA
	State A, V_{PH2} = 6V	–13	2	13	µA
	State A, V_{PH2} = 8V	–30	–50	–70	µA
Motor Current Control Section					
I(SENSE) Gain	V_{PIN21} = 2.5V	4.5	5	5.5	V/V
One Shot off time		5	10	15	µS
I(CMD) Transconductance Gain			0.19		mmho
I(CMD), I(LIM) Bias Current	V_{IN} = 0	0	–100	–400	nA
Power Fail Detection Circuit					
12V Threshold		9.1	9.8	10.5	V
Hysteresis			150		mV
5V Threshold		3.8	4.25	4.5	V
Hysteresis			70		mV
Logic Inputs					
Voltage High (V_{IH})		2			V
Voltage Low (V_{IL})				0.8	V
Current High (I_{IH})	V_{IN} = 2.7V	–10	1	10	µA
Current Low (I_{IL})	V_{IN} = 0.4V	–500	–350	–200	µA
Braking Circuit					
Brake Active Threshold		1.0	1.4	1.8	V
PIN 25 Bias Current	V_{PIN25} = 0V		0.3	1	µA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, T_A = Operating Temperature Range, VCC = VCC2 = 12V, R_{SENSE} = 1Ω, C_{0TA} = C_{VCO} = 0.01µF, C_{OS} = 0.001µF, R_{OS} = 10kΩ

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Outputs I(CMD) = I(LIMIT) = 2.5V					
I_P low	V_P = 2V	0.5		1.2	mA
V_P high	I_P = –10µA	VCC2 – 1V			V
P3 Comparator Threshold		VCC2 – 3.6V		VCC2 – 2.4V	V
V_N high	V_{PIN1} = 0V	VCC – 3.2	10	VCC – 1.2	V
V_N low	I_N = 1mA		0.2	0.7	V
LOGIC low (V_{OL})	I_{OUT} = 0.4mA			0.5	V
VCO/TACH V_{OH}	I_{OUT} = 100µA	2.4			V
POWER FAIL V_{OH}	I_{OUT} = 10µA	V_{PIN8} – 0.2	V_{PIN8} – 0.1	V_{PIN8}	V
Supply Currents (N and P outputs open)					
5V Current			8	25	mA
VCC Current			1	1.5	mA
VCC2 Current			8	16	mA

Note 1. For explanation of states, see Figure 5 and Table 1.

SUMMARY OF ENHANCEMENTS IN ML4412 OVER THE ML4411

1. Lower power dissipation, 200mW versus 450mW in the ML4411.
2. Accurate and customized start-up by using commutation clock provided by the microprocessor instead of relying on I_{RAMP} as in the ML4411.
3. True braking function which is biased by TOB, to allow braking block to work under a power loss situation.
4. ML4412 adds hysteresis into braking comparator to accelerate the transition as soon as the (Vth) threshold is reached.
5. ML4412 adds comparator to prevent the PMOS from coming "ON" when the braking is active.
6. ML4412 adds active pull-up to the P output to replace the resistor pull-up in ML4411.
7. ML4412 enhances pull-down capability to the N output to prevent injected shoot through (only 3 mA in the ML4411).
8. ML4412 adds comparator to prevent P3 N3 shoot through during reset to state A transition.
9. The one-shot accuracy in the ML4412 is improved over the ML4411's.
10. ML4412 adds a blanker circuit to one-shot to prevent it from false triggering which occurrs when large starting currents cause noise coupling to the chip.

FUNCTIONAL DESCRIPTION

The ML4412 provides closed-loop commutation for 3-phase brushless motors. To accomplish this task, a VCO, Integrating Back-EMF Sampling error amplifier and sequencer form a phase-locked loop, locking the VCO to the back-EMF of the motor. The IC also contains circuitry to control motor current with either linear or constant off-time PWM modes. Braking and power fail detection functions are also provided on chip. The ML4412 is designed to drive external power transistors (N-channel sinking transistors and P-Channel sourcing transistors) directly.

Start-up sequencing and motor speed control are accomplished by a microcontroller. Speed sensing is accomplished by monitoring the output of the VCO, which will be a signal, phased-locked to the commutation frequency of the monitor.

BACK-EMF SENSING AND COMMUTATOR

The ML4412 contains a patented back-EMF sensing circuit which samples the phase which is not energized (Shaded area in figure 2 below) to determine whether to increase or decrease the commutator (VCO) frequency. A late commutation causes the error amplifier to charge the filter (RC) on pin 20, increasing the VCO input while early commutation causes pin 20 to discharge. Analog speed control loops can use Pin 20 as a speed feedback voltage.

The input impedance of the three PH inputs is about 5kΩ to GND. When operating with a higher voltage motor, the PH inputs should be divided down in voltage so that the maximum voltage at any PH input does not exceed VCC.

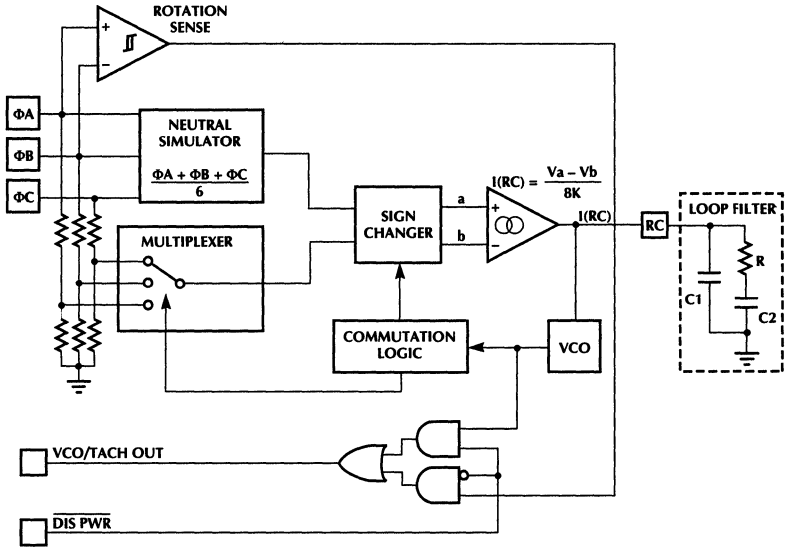


Figure 1. Back-EMF sensing block diagram

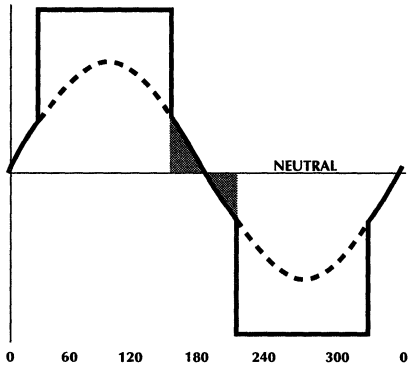


Figure 2. Typical motor phase waveform with Back-EMF superimposed (Ideal Commutation)

VCO AND PHASE DETECTOR CALCULATIONS

The VCO should be set so that at the maximum frequency of operation (the running speed of the motor) the VCO control voltage will be no higher than VCC_{MIN} – 1V. The VCO maximum frequency will be:

$$F_{MAX} = 0.05 \times POLES \times RPM$$

where POLES is the number of poles on the motor and RPM is the maximum motor speed in Revolutions Per Minute.

The minimum VCO gain derived from the specification table (using the minimum F_{VCO} at V_{VCO} = 6V) is:

$$K_{VCO(MIN)} = \frac{2.42 \times 10^{-6}}{C_{VCO}}$$

Assuming that the $V_{VCO(MAX)}$ = 9.5V, then

$$C_{VCO} = \frac{9.5 \times 2.42 \times 10^{-6}}{F_{MAX}}$$

or

$$C_{VCO} = \frac{460}{POLES \times RPM} \mu F$$

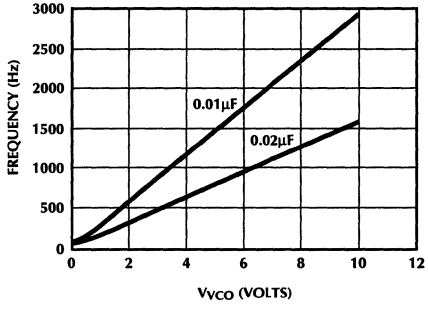


Figure 3. VCO Output Frequency vs. V_{VCO} (pin 20)

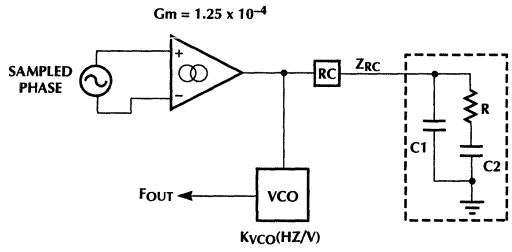


Figure 4. Back EMF Phase Lock Loop Components

Figure 4 above shows the transfer function of the Phase Lock Loop with the phase detector formed from the sampled phase through the Gm amplifier with the loop filtered formed by R, C_1, and C_2.

The impedance of the loop filter is

$$Z_{RC}(s) = \frac{1}{C_1 s} \frac{(s + \omega_{LEAD})}{(s + \omega_{LAG})}$$

Where the lead and lag frequencies are set by:

$$\omega_{LEAD} = \frac{1}{RC_2}$$

$$\omega_{LAG} = \frac{C_1 + C_2}{RC_1C_2}$$

Requiring the loop to settle in 20 PLL cycles with a spread of 10 between $\omega_{LEAD} = 10 \times \omega_{LAG}$ produces the following calculations for R, C_1, and C_2:

$$C_1 \approx \frac{4.66 \times 10^{-9}}{C_{VCO} \times F_{VCO}^{\ 2}}$$

$$C_2 = 9 \times C_1$$

$$R = \frac{12.54}{C_2 \times F_{VCO}}$$

START-UP SEQUENCING

When the motor is initially at rest, it is generating no back-EMF. Because a back-EMF signal is required for closed loop commutation, the motor must be started "open-loop" until a velocity sufficient to generate some back-EMF is attained. The following steps are a typical procedure for starting a motor which is at rest. It is possible to determine if the motor is running by polling the VCO/TACH OUT pin with power disabled (Pin 27 = low).

STEP 1 The IC is held in reset state until the platters are steady by setting pin 17 and pin 19 to a '1', with full power applied to the winding (see figure 5). This aligns the rotor to a position which is 30° (electrical) before the center of the first commutation state. Pin 20 is held at 0.5V internally. Microprocessor needs to measure VCO frequency by setting pin 27 to a '1' and then store it.

STEP 2 Setting pin 17 to a '0' and pin 19 to a '1' holds the IC in a ramping state. Microprocessor sends starting commutation clock to pin 16 which is an input pin in this state. This clock frequency is gradually increasing until it reaches the VCO frequency previously stored in Step 1.

STEP 3 As soon as commutation clock reaches the VCO frequency of Step 1, pin 19 is switched to "0" while pin 17 remains '0'. Now the PLL is closed and the VCO is locked to the Back EMF. Pin 16 becomes an output pin. Thus the commutation clock from the microprocessor should be held in tri-state.

Table 1 Commutation, Braking and PLL States

STATE	OUTPUTS						INPUT SAMPLING
	N1	N2	N3	P1	P2	P3	
R OR 0	OFF	ON	OFF	ON	OFF	ON	N/A
A	OFF	OFF	ON	ON	OFF	OFF	PH2
B	OFF	OFF	ON	OFF	ON	OFF	PH1
C	ON	OFF	OFF	OFF	ON	OFF	PH3
D	ON	OFF	OFF	OFF	OFF	ON	PH2
E	OFF	ON	OFF	OFF	OFF	ON	PH1
F	OFF	ON	OFF	ON	OFF	OFF	PH3

STATE	ENABLE E/A	RESET	PIN20 (RC)	VCO	COMMUTATOR
RESET	1	1	0.5V	RUNNING PER V_{PIN20}	IN RESET STATE
RAMP	1	0	0.5V	PRESET	CLOCKED FROM COMMUTATION CLOCK
RUN	0	0	DRIVEN BY PLL	RUNNING PER V_{PIN20}	SEQUENCED BY VCO
BRAKE	0	1	X	X	X

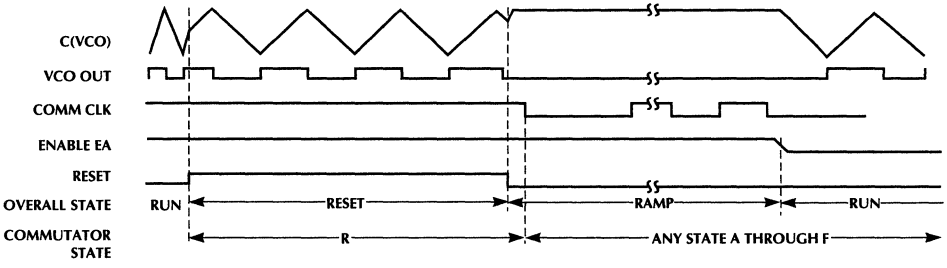


Figure 5. Start up sequencing (from stop)

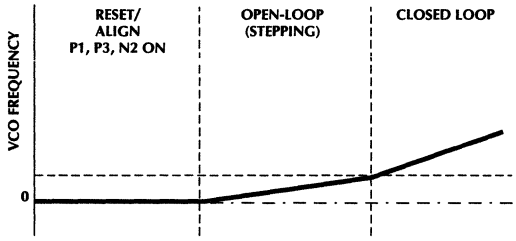


Figure 6. Typical Start-up Sequence

Using this technique, some reverse rotation is possible. The maximum amount of reverse rotation is 360/N, where N is the number of poles. For an 8 pole motor, 45° reverse rotation is possible.

TABLE 2. START-UP SEQUENCE

STEP	PIN 17	PIN 19	PIN 21	I(LIMIT) I(CMD)
1	1	1	FIXED	I_{MAX}
2	0	1	FIXED	I_{MAX}
3	0	0	0	I_{MAX}

PWM AND LINEAR CURRENT CONTROL

To facilitate speed control, the ML4412 includes two current control loops — linear and PWM (fig. 7). The linear control loop senses the motor current on the I(SENSE) terminal through R_{SENSE}. An internal current sense amplifier's (A2) output modulates the gates of the 3 N-channel MOSFET's.

The ML4412 also includes a current mode constant off-time PWM circuit. When motor current builds to the threshold set on I(LIMIT) input (pin 21), a one-shot is fired whose timing is set by C_{OS} and R_{OS} where

$$t_{OFF} = 1.3 \times R_{OS} \times C_{OS}$$

The current in the motor will be controlled by the lower of pin 13 and pin 21.

The linear current control modulates the gates of the external MOSFET drivers. Amplifier A2 is a transconductance amplifier which amplifies the difference between I(CMD) and I(SENSE). The transconductance gain of A2 is:

$$g_m = 1.875 \times 10^{-4} \mho$$

The current loop is compensated by C_{OTA} which forms a pole given by

$$\omega_P = \frac{9.375 \times 10^{-4}}{C_{OTA}}$$

This time constant should be fast enough so that the current loop settles in less than 10% of T_{VCO} at the highest motor speed to avoid torque ripple to V_{TH} mismatch of the N-Channel MOSFET's.

The I(SENSE) input pin should be kept below 1V. If I(SENSE) goes above 1V, a bias current of about –300µA will flow out of pin 1 and the N outputs will be inhibited. Bringing I(SENSE) below 0.7V returns the bias current to its normal level For this reason, the noise filter resistor on the I(SENSE) pin (1kΩ on Figure 8) should be less than 1.5kΩ.

The noise filter time constant should be great enough to filter the leading edge current spike when the N-FETs turn on but small enough to avoid excessive phase shift in the I(SENSE) signal.

OUTPUT DRIVERS

The motor's source drivers (P1 thru P3) are NPN emitter followers. N3 is inhibited until P3 is within 3V (typ) of VCC2. Drivers N1 through N3 are totem-pole outputs capable of sinking 10mA. Switching noise in the external MOSFETs is reduced by an internal 4KΩ resistor in series with the sourcing NPN to form an RC time constant with the N-Channel gate capacitance.

BRAKING

As shown in Figure 7 the braking circuit pulls the N-channel MOSFET Gates high when the BRAKE pin falls below a 2 x Vbe threshold (Vth). After a power failure, C(DLY) is discharged slowly through R(DLY) providing a delay for retract to occur before the braking circuit is activated. The P-channel MOSFETs are turned off well before braking occurs. As soon as the Vth threshold is reached, the braking comparator with hysteresis will accelerate the transition and tri-state the N-channel buffer (B1, refer figure 7) before C(BRK) dump charges into the N-channel Gates. This is to ensure that no charge from C(BRK) is lost through the pull-down transistors in B1, (figure 7). The C(BRK) will continue charging the N-channel Gates, to ensure braking, even when VCC2 (motor BEMF rectified through the MOSFET body diode), drops due to the braking process. An external signal could be used to brake the motor. To accomplish this set pin 17 = '1', pin 19 = '0'. This will pull pin 26 below the threshold to activate the braking circuit.

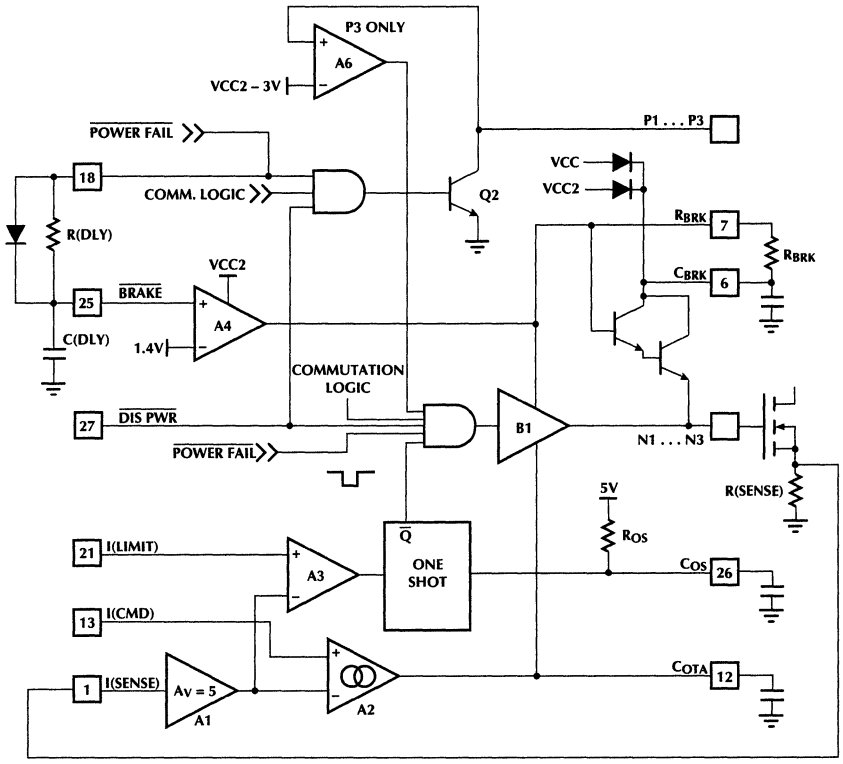


Figure 7. PWM and Linear Current Control, Gate Drive and Braking Circuits

APPLICATIONS

Figure 8 shows a typical application of the ML4412 in a hard disk drive spindle control. The timing needed to start the motor in most applications would be generated by a microcontroller.

Speed control can be accomplished either by:

1. Sensing the VCO OUT frequency with a Microcontroller and adjusting I(CMD) via an analog output from the Micro (PWM DAC).
2. Using analog circuitry for speed control. (Fig. 9)

OUTPUT STAGE HINTS

In the circuit in Figure 8, Q1, Q2 and Q3 are IRFR9024 or equivalent. Q4, Q5 and Q6 are IRFR024 or equivalent. New MOSFET packaging technology such as the Little Foot® series may decrease the PC board space. These packages, however have much lower thermal inertia and dissipation capabilities than the larger packages, and care should be taken not to exceed their rated current and junction temperature.

Since the output section in a full bridge application consists of three half-H switches, cross-conduction can occur. Cross conduction is the condition where an N-FET and P-FET in the same phase of the bridge conduct simultaneously. This could happen under two conditions (see Figure 10):

1. When transitioning from mode 0 to mode A (see table 1) P3 goes from on to off at the same time N3 goes from off to on. If P3 turns off slowly and N3 turns on quickly, cross conduction may occur. This condition has been prevented inside the IC on the ML4412 through the addition of comparator A6 on the P3 output (Fig. 7).

2. When the MOSFET in the same phase switches on gate current flows due to capacative coupling of current through the MOSFET's drain to gate capacitance. This could cause the MOSFET that was off to be turned on.

3. In condition 2 above, the P-channel MOSFET is pulled up inside the ML4412 by a NPN follower with base pulled up to VCC2 via 16KΩ. If the current through Cdgp is greater than the Vth_{PMOS}/16KΩ/Beta NPN, when the N-FET turns ON, the P-FET could be turned ON simultaneously, causing cross-conduction. The same mechanism can be applied to N-FET when P-FET is turned ON. The ML4412 is designed to take care of both the cases through slow turn-on, fast turn-off schemes ie P-FET Gate is pulled down by an 800µA current source and the N-FET Gate is charged up by an emitter follower in series with 4KΩ.

Figure 10 shows the output stages and the potential causes of cross-conduction. The diode D1 shown, may be needed for high power applications to limit the negative current pulled (through Cdgn) out of the substrate diode in the ML4412 when P-FET turns off.

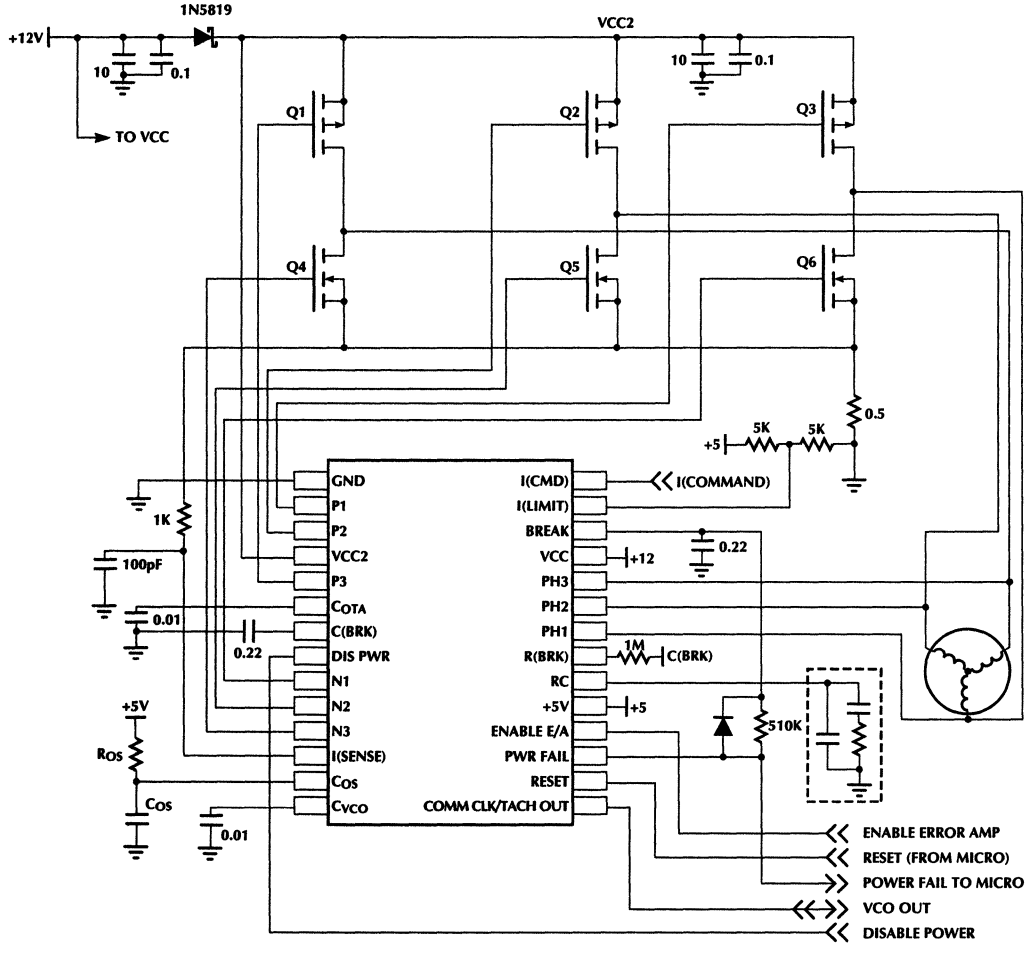
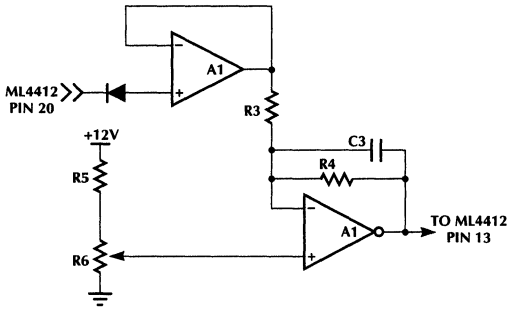


Figure 8. ML4412 Typical Application



SYMBOL	VALUE
A1	LM358
IC1	74HC14
D1, D2	IN4148
R1	1MΩ
R2	1MΩ
R3	100KΩ

SYMBOL	VALUE
R4	100KΩ
R5	50KΩ
R6	50KΩ
C1	3.3µF
C2	3.3µF
C3	0.47µF

Figure 9. Analog Speed Control

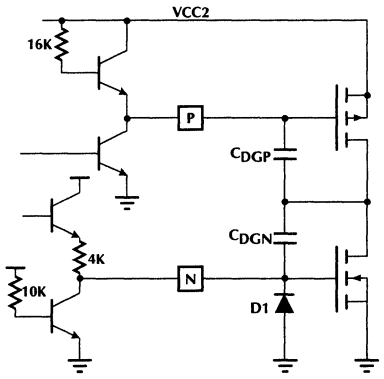


Figure 10. Causes of Cross-conduction

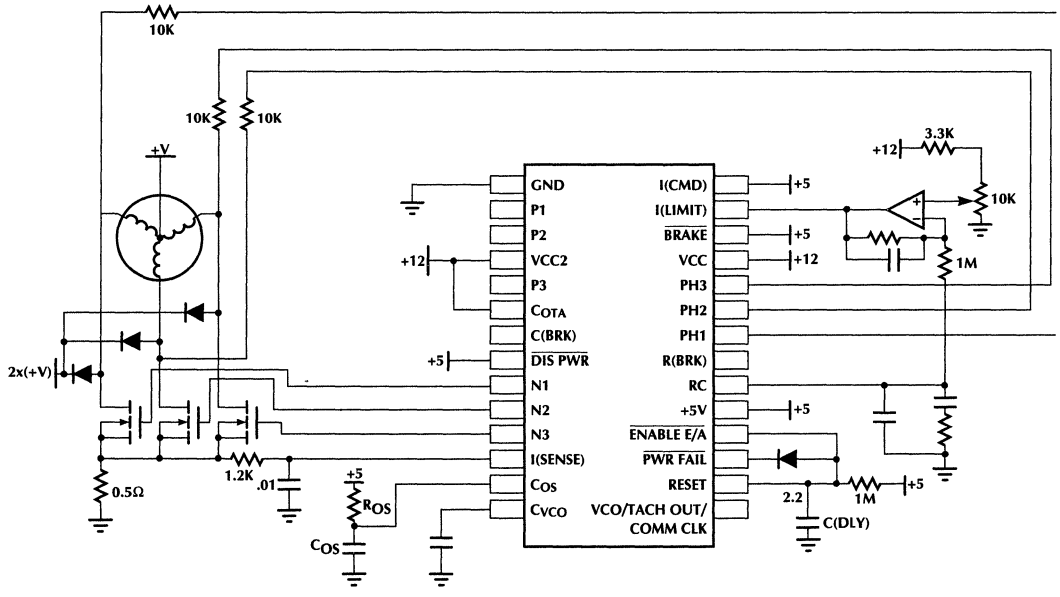


Figure 11. ML4412 Unipolar Drive Application

UNIPOLAR OPERATION

Unipolar mode offers the potential advantage of lower motor drive cost by only requiring the use of 3 transistors to drive the motor. The ML4412 will operate in unipolar mode (Figure 11) provided the following precautions are taken:

1. The IC supplies should not exceed 12V + 10%.
2. The phase pins on the IC should not exceed the supply voltage.

In unipolar operation, the motor's windings must be allowed to drive freely to:

$$V_{\Phi(MAX)} = V_{SUPPLY\ (MAX)} + V_{EMF\ (MAX)}$$

Therefore, there can be no diodes to clamp the inductive energy to V_{SUPPLY}. This energy must be clamped, however, to avoid an over-voltage condition on the MOSFETs and other components. Typically, a V(CLAMP) voltage is created to provide the clamping voltage. The inductive energy may either be dissipated (Figure 12) or alternately efficiently regenerated back to the system supply (Figure 13).

The circuit in Figure 11 is designed to minimize the external components necessary, at some compromise to performance. The 3 resistors from the motor phase windings to the PH inputs work with the ML4412's 5KΩ internal resistance to ground to divide the motor's phase voltage down, providing input signals that do not exceed 12V. This circuit uses analog speed regulation. The "one shot" circuitry to time the reset is replaced by a diode and RC delay from the rising edge or the $\overline{\text{POWERFAIL}}$ signal. The error amplifier is left enabled continuously since at low speeds its current contribution is negligible. The current injected into the loop filter must be greater than the leakage current from the phase detector amplifier for the motor to start reliably.

HIGHER VOLTAGE MOTOR DRIVE

To drive a higher voltage motor, the same precautions regarding ML4412 voltage limitations as were outlined for Unipolar drive above should be followed. Figures 14–16 provide several methods of translating the ML4412's P outputs to drive a higher voltage.

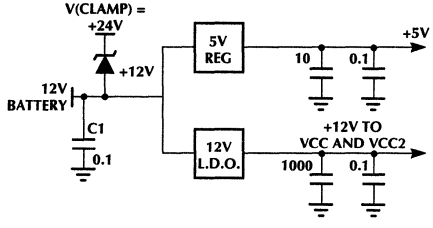


Figure 12. Dissipative Clamping Technique

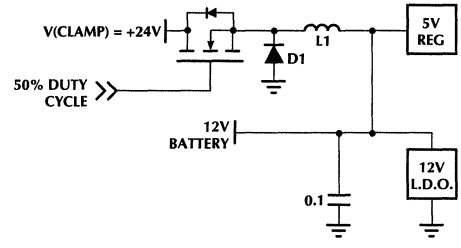


Figure 13. Non-Dissipative Clamping Technique

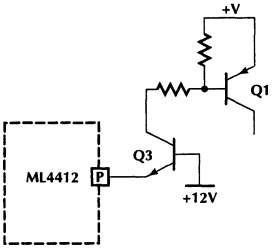


Figure 14. High Voltage Translation using PNP Power Transistor

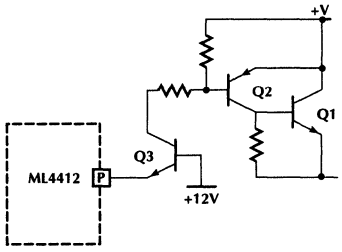


Figure 15. High Voltage Translation using "Composite" PNP Power Transistor

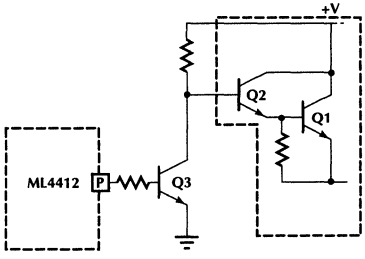


Figure 16. High Voltage Translation with NPN Darlingtion

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4412CS	0°C to +70°C	28-PIN SOIC (S28W)

November 1990
PRELIMINARY

Micro Linear

ML4415, ML4415R
ML4416, ML4416R

15 Channel Read/Write Circuit

GENERAL DESCRIPTION

The ML4415, ML4416 devices are bipolar monolithic read/write circuits designed for use with fixed disk ferrite center-tapped recording heads. They provide a low noise read path, write current control, and data protection circuitry for all channels.

These multiplexed read/write data channels exhibit features not found in similar read/write circuits such as improved write current stability and elimination of write current "glitches" during power up.

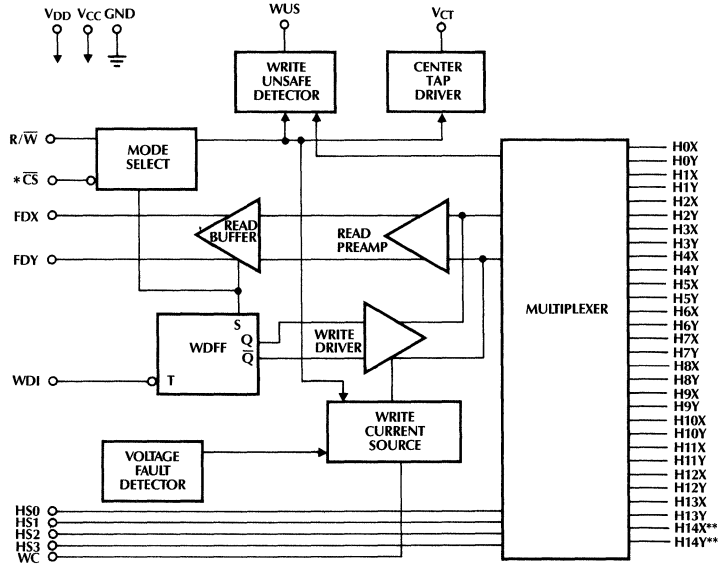
The ML4416 has fourteen read/write data channels and a chip select pin. The chip select pin allows additional read/write circuits in the system by enabling or disabling a particular chip. The ML4415 has fifteen read/write data channels and no chip select pin.

The ML4415R and ML4416R versions include on-chip damping resistors.

FEATURES

- Write current disable during power up
- Enhanced write current stability
- Designed for center-tapped ferrite heads
- ML4415 provides 15 read/write channels
- ML4416 — easily multiplexed for larger systems
- Includes write unsafe detection
- TTL compatible control signals
- Programmable write current source
- +5V, +12V power supplies

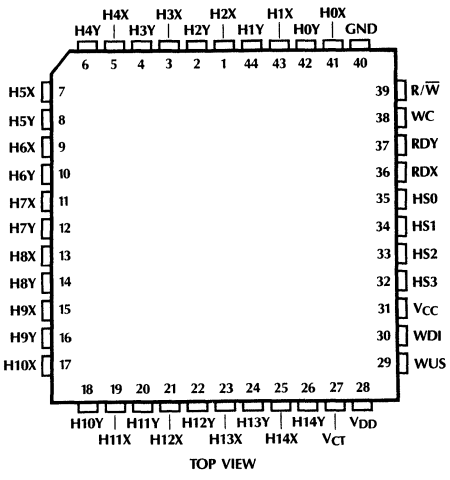
BLOCK DIAGRAM



* ML4416 ONLY
** ML4415 ONLY

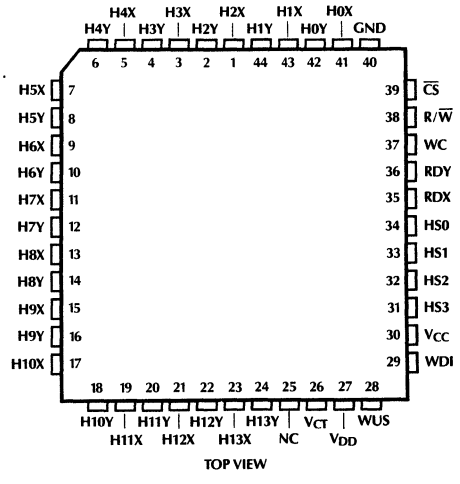
PIN CONNECTIONS

ML4415CQ, ML4415RCQ
44-Pin PCC



TOP VIEW

ML4416CQ, ML4416RCQ
44-Pin PCC



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
HS0–HS3	Head Select (14 heads for the ML4416, and 15 heads for ML4415).
$\overline{CS}$	Chip Select (low level enables, ML4416 only)
R/W	Read/Write (high level select Read Mode)
WUS	Write Unsafe, open collector output (high level indicates an unsafe writing condition)
WDI	Write Data In (negative transition toggles head current direction)

NAME	FUNCTION
H0X–H14X	X head connections
H0Y–H14Y	Y head connections
RDX, RDY	X, Y Read Data (differential read signal out)
WC	Write Current (used to set the write current magnitude)
V_{CT}	Voltage Center Tap (center tap voltage source)
V_{CC}	+5 volts
V_{DD}	+12 volts
GND	Ground

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- $V_{DD}1$ ..... -0.3 to $14V_{DC}$
- $V_{DD}2$ ..... -0.3 to $14V_{DC}$
- V_{CC} ..... -0.3 to $6V_{DC}$

Input Voltage Range
- Digital Inputs ($\overline{CS}$, R/$\overline{W}$, HS, WDI) ... -0.3 to V_{CC} $+0.3V_{DC}$
- Head Ports ..... -0.3 to $V_{DD}1$ $+0.3V_{DC}$
- Write Unsafe (WUS) ..... -0.3 to $14V_{DC}$

Write Current (I_W) 60mA

Output Current
- Read Data (RDX, RDY) ..... -10mA
- Center Tap Current (I_{CT}) ..... -60mA
- Write Unsafe (WUS) 12mA

Storage Temperature ..... $-65°C$ to $150°C$

Junction Temperature (T_J) ..... 135°C

Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Supply Voltage
- $V_{DD}1$ ..... $12V \pm 10\%$
- V_{CC} ..... $5V \pm 10\%$

Head Inductance
- L_H ..... 5 to 15μH

Damping Resistor (R_D, ML4415R or ML4416R) .. 500 to 2000Ω

RCT Resistor (1/4 Watt) ..... $120\Omega \pm 5\%$

Write Current (I_W) ..... 10 to 40mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $V_{DD}1 = V_{DD}2 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 40$mA, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC OPERATING CHARACTERISTICS						
POWER SUPPLY						
I_{CC}	V_{CC} Supply Current	Read or Idle Mode		31	35	mA
		Write Mode		26	30	mA
I_{DD}	V_{DD} Supply Current	Read Mode		29	35	mA
		Write Mode		$17+I_W$	$20+I_W$	mA
		Idle Mode		17	20	mA
P_D	Power Dissipation	Read Mode		550	655	mW
		Write Mode $I_W = 40$mA, $R_{CT} = 0\Omega$		890	960	mW
		Idle Mode		378	455	mW
DIGITAL INPUTS ($\overline{CS}$, R/$\overline{W}$, HS, WDI)						
V_{IH}	High Voltage		2			V_{DC}
V_{IL}	Low Voltage				0.8	V_{DC}
I_{IH}	High Current	$V_{IH} = 2.0V$			100	μA
I_{IL}	Low Current	$V_{IL} = 0.8V$	-0.4			mA
WUS OUTPUT						
V_{OL}	Output Low Voltage	$I_{OL} = 8$mA (Safe)			0.5	V_{DC}
I_{OH}	Output High Current	$V_{OH} = 5V$ (Unsafe)			100	μA
CENTER TAP VOLTAGES						
V_{CT}	Read Mode	Read Mode		4		V_{DC}
V_{CT}	Write Mode	Write Mode		6		V_{DC}

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1$ = 12V ± 10%, V_{CC} = 5V ± 10%, R_{CT} = 120Ω ± 5%, I_W = 35mA, L_H = 10μH, R_D = 750Ω (ML4415, ML4416), f_{DATA} = 5MHz, C_L (RDX, RDY) ≤ 20pF, 0°C ≤ T_A ≤ 70°C (Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE CHARACTERISTICS						
I_{HCW}	Head Current (per side)	Write Mode $0 \leq V_{CC} \leq 3.7V$ $0 \leq V_{DD}1 \leq 8.7V$	−200	0.15	200	μA
I_{WR}	Write Current Range	$I_W = K/R_{WC}$	10		40	mA
K	Write Current Constant		2.375	2.5	2.625	
V_{HD}	Differential Head Voltage Swing		7.0	10.2		V_{PK}
I_{HU}	Unselected Head Transient Current				2	mA_{PK}
C_{OD}	Differential Output Capacitance			8.8	15	pF
R_{OD}	Differential Output Resistance	ML4415, 4416	10k			Ω
		T_J = 25°C ML4415R, 4416R	600		960	Ω
f_{WDI}	WDI Transition Frequency	WUS = Low	250	490		kHz
A_I	I_{WC} to Head Current Gain			0.99		mA/mA
I_L	Unselected Head Leakage	Sum of X & Y Side Leakage Current			85	μA
READ MODE CHARACTERISTICS						
A_V	Differential Voltage Gain	$V_{IN} = 1mV_{P-P}$ @ 300kHz, R_L (RDX, RDY) = 1kΩ	85	106	115	V/V
DR	Dynamic Range	DC Input Voltage (V_I) Where Gain Falls 10%, $V_{IN} = V_I + 0.5mV_{P-P}$ @ 300kHz	−3	±7	+3	mV
BW	Bandwidth (−3dB)	$\|Z_S\| < 5Ω, V_{IN} = 1mV_{P-P}$	30	40		MHz
e_{IN}	Input Noise Voltage	BW = 15MHz, L_H = 0, R_H = 0		1.2	1.5	nV/ $\sqrt{Hz}$
C_{IN}	Differential Input Capacitance	f = 5MHz		14	20	pF
R_{IN}	Differential Input Resistance	f = 5MHz, T_J = 25°C ML4415, 4416	2k	15K		Ω
		V_{IN} = $6mV_{P-P}$ ML4415R, 4416R	460		860	Ω
I_{HCR}	Head Current (per side)	Read or Idle Mode $0 \leq V_{CC} \leq 5.5V$ $0 \leq V_{DD}1 \leq 13.2V$	−200		200	μA
I_{IN}	Input Bias Current (1 side)			8.5	45	μA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V_{CT} + 100mV_{P-P}$ @ f = 5MHz	50	77		dB
PSRR	Power Supply Rejection Ratio	$100mV_{P-P}$ @ 5MHz on $V_{DD}1$, $V_{DD}2$, or V_{CC}	45			dB
CS	Channel Separation	Unselected Channels: $V_{IN} = 100mV_{P-P}$ @ 5MHz and Selected Channel: $V_{IN} = 0mV_{P-P}$	45	57		dB
V_{OS}	Output Offset Voltage	Read Mode	−460	±29	+460	mV
		Write or Idle Mode	−20	±1	+20	mV
V_{OCM}	Common-Mode Output Voltage	Read Mode	4.5	5.5	6.5	V
		Write or Idle Mode		5.6		V
R_{OUT}	Single-Ended Output Resistance	f = 5MHz			30	Ω
I_L	Leakage Current, RDX, RDY	(RDX, RDY) = 6V Write or Idle Mode	−100	±15	100	μA
I_O	Output Current	AC Coupled Load, RDX to RDY	±2.1	±2.7		mA

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ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1$ = 12V ± 10%, V_{CC} = 5V ± 10%, R_{CT} = 120Ω ± 5%, I_W = 35mA, L_H = 10μH, R_D = 750Ω (ML4415, ML4416), f_{DATA} = 5MHz, 0°C ≤ T_A ≤ 70°C (Notes 2 and 3)

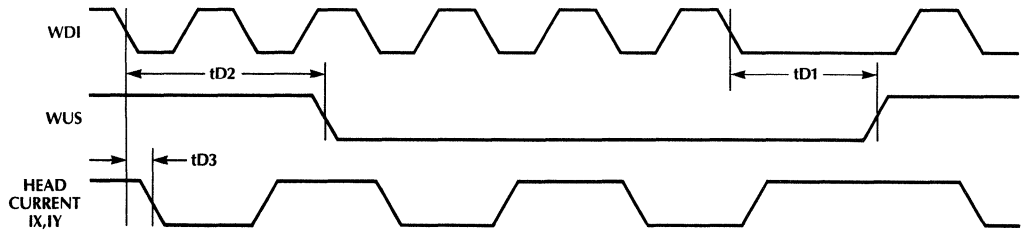
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_{RW}	R/$\overline{W}$ to Write Switching Delay	To 90% of Write Current Output		.105	1	μs
t_{WR}	R/$\overline{W}$ to Read Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current		.036	1	μs
t_{IW} or t_{IR}	$\overline{CS}$ to Select Switching Delay	To 90% of Write Current or to 90% of 100mV, 10MHz Read Signal Envelope		.165	1	μs
t_{WI} or t_{RI}	$\overline{CS}$ to Unselect Switching Delay	To 90% Decay of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current		.084	1	μs
t_{HS}	Head Select Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope		.045	1	μs
tD1	Safe to Unsafe Write Unsafe Delay	I_W = 35mA	1.6	3.9	8	us
tD2	Unsafe to Safe Write Unsafe Delay	I_W = 35mA		.387	1	us
tD3	Prop. Delay Head Current	L_H = 0, R_H = 0 From 50% points		23	25	ns
	Asymmetry Head Current	WDI has 50% Duty Cycle and 1nS Rise/Fall Time		0.9	2	ns
	Rise/Fall Head Current	10% and 90% Points		5	20	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Maximum junction temperature (T_J) should not exceed 135°C.

TIMING DIAGRAM



Write Mode Timing Diagram

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

For any selected head, the ML4415/4416 functions as a read amplifier when in the Read mode, or as a write current switch when in the Write mode. Pins HS0, HS1 and HS2 determine head selection while pin R/W controls the Read/Write mode. A detected "write-unsafe" condition is indicated by pin WUS.

READ MODE

When the ML4415, 4416 is in the Read Mode, it operates as a low-noise differential amplifier on the selected channel. In Read mode the write data flip-flop is set and both the write unsafe detector and the write current source are deactivated. The center tap voltage is also lowered. Pins RDX and RDY provide differential emitter follower outputs which are in phase with the X and Y head input pins.

Note that during the Read or Chip Deselect mode the internal write current is deactivated, thus making external write current gating unnecessary.

WRITE MODE

The ML4415, 4416 operates as a write-current switch when in the Write mode. Write current magnitude is determined by the following relationship:

$I_W = K/R_{WC}$

Where: K = Write Current Constant

R_{WC} = Resistance connected between pin WC and GND.

The head current is toggled between the X and Y side of the selected head by a negative transition WDI (Write Data Input). When switching the ML4415, 4416 to write mode, the WDFF (Write Data Flip-Flop) is initialized to pass write current through the X-side of the head.

The ML4415, 4416 exhibit enhanced write current stability, compared to similar read/write circuits, which reduces the problem of oscillation. This is a result of increased internal write current compensation. Also, write current "glitches" during power-up, common in similar read/write circuits, are eliminated with an exclusive write current disabling function.

The WUS (Write Unsafe) pin is an open collector output that gives a logic high level for any of the following unsafe write conditions:

- Open head
- Open head center-tap
- Too low WDI frequency
- Read mode selected
- Device not selected
- No write current

Two negative transitions on WDI are required to clear WUS after the fault condition is removed.

The ML4415, 4416 also offers a voltage fault detection circuit that prevents write current during power-loss or power-up.

Table 1.

Head Select

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	H0
0	0	0	1	H1
0	0	1	0	H2
0	0	1	1	H3
0	1	0	0	H4
0	1	0	1	H5
0	1	1	0	H6
0	1	1	1	H7
1	0	0	0	H8
1	0	0	1	H9
1	0	1	0	H10
1	0	1	1	H11
1	1	0	0	H12
1	1	0	1	H13
1	1	1	0	H14*

* ML4415 only
0 = Logic Level Low
1 = Logic Level High
X = Don't Care

Table 2.

Mode Select

$\overline{CS}$**	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

** ML4416 only
0 = Logic Level Low
1 = Logic Level High
X = Don't Care

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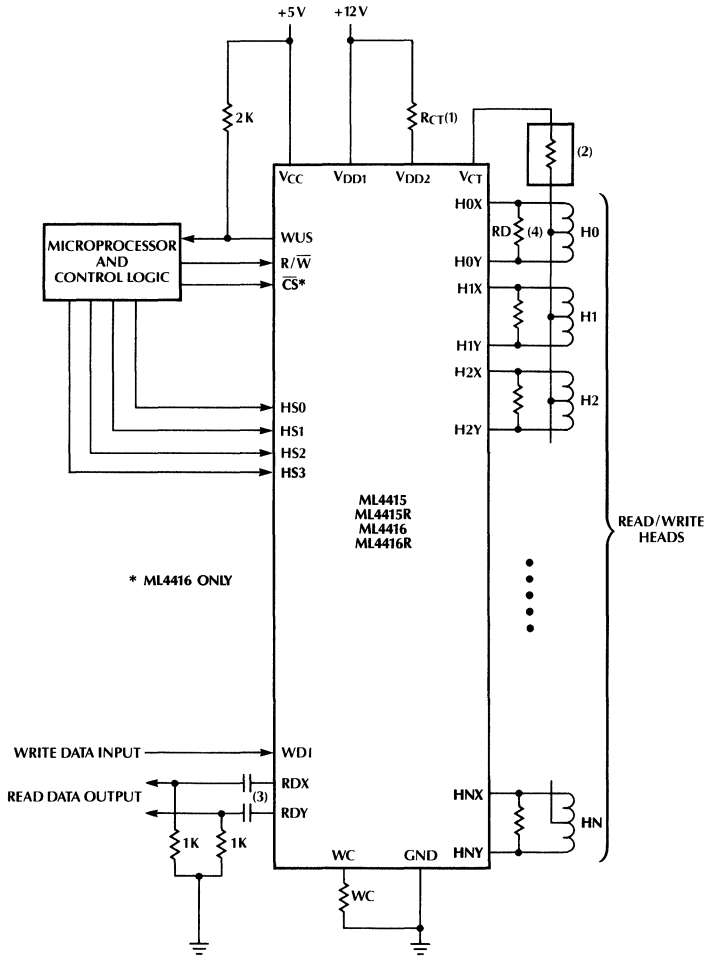
TYPICAL APPLICATION



NOTES:

1. RCT is optional and is used to limit internal power dissipation (Otherwise connect $V_{DD}1$ to $V_{DD}2$).
   RCT (1/2 Watt) = 120 (40/I_W) ohms
   where I_W = Write Current, in mA
2. Ferrite head optional: used to suppress write current overshoot and ringing. Recommend Ferroxcube 3659065/4A6.
3. RDX and RDY load capacitance 20pF maximum. RDX and RDY output current must be limited to 100μA.
4. Damping resistors not required on ML4415R, 4416R.

ORDERING INFORMATION

PART NUMBER	PACKAGE	NUMBER OF CHANNELS
ML4415CQ	MOLDED PCC (Q44)	15
ML4415RCQ	MOLDED PCC (Q44)	15
ML4416CQ	MOLDED PCC (Q44)	14 with $\overline{CS}$
ML4416RCQ	MOLDED PCC (Q44)	14 with $\overline{CS}$

May 1992
PRELIMINARY

Micro Linear

ML4417/ML4427

Zoned Bit Recording Circuit

GENERAL DESCRIPTION

The ML4417/27 is a bipolar monolithic integrated circuit that simplifies the design of zoned bit recording systems in hard disk drives. It contains a VCO capable of operating at frequencies up to 95 MHz, a charge pump, and the active electronics required for a loop filter to form a variable rate data encoding and decoding system.

The ML4417/27 also includes a code clock output and the dividers required for an interface clock output whose frequency is equal to the code clock output frequency divided by 1.5. This feature simplifies the use of RLL (1, 7) coding for improved storage density.

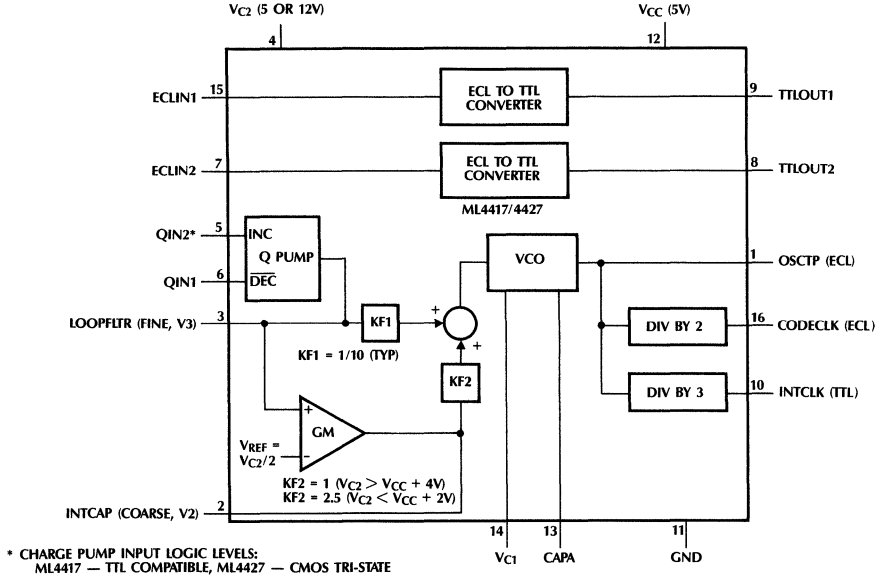
In addition, the ML4417/27 includes two uncommitted ECL to TTL level translators to simplify interfacing with TTL-based systems. The ML4417/27 is designed for operation from 12V and 5V supplies, but may be operated from a single 5V supply if desired.

The ML4417 has TTL-compatible logic input levels on the charge pump, and the ML4427 has a charge pump control input, which, when driven by a CMOS tri-state output, eliminates one logic interface line to the circuit.

FEATURES

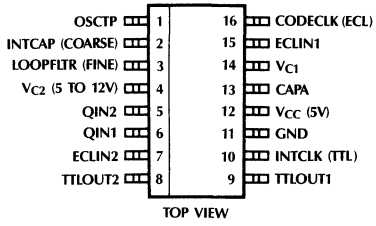
- Wide VCO Range (3:1 Range to 95 MHz)
- Allows RLL (1, 7) or (2, 7) Encoding
- SO-16 (Narrow) Packaging
- Coarse and Fine VCO Control Inputs
- Two Uncommitted ECL to TTL Converters
- 12V, 5V or Single 5V Operation

BLOCK DIAGRAM

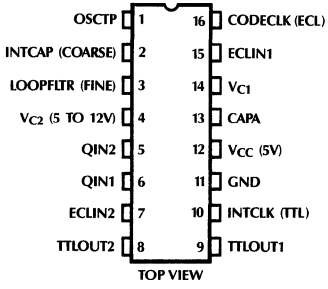


PIN CONNECTIONS

ML4417, ML4427
SOIC-16 (Narrow) Package



ML4417, ML4427
PDIP-16 Package
(Prototypes Only)



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	OSCTP (ECL)	Oscillator Test Point. An ECL output of the VCO that is useful for direct evaluation of the VCO output.
2	INTCAP (COARSE)	The coarse input for the loop filter time constant setting.
3	LOOPFLTR (FINE)	The fine input for loop filter time constant setting.
4	V_{C2}	Analog power supply input, nominal 5V or 12V.
5	QIN2	Increment input on the charge pump. This input is TTL-compatible on the ML4417. On the ML4427, it can be connected, along with pin 6, to a single CMOS tri-state output, eliminating one pin on the controlling gate array. (Active high)
6	QIN1	Decrement input on the charge pump. (Active low)
15, 7	ECLIN1, 2	ECL inputs for ECL to TTL level translators.
9, 8	TTLOUT1, 2	TTL outputs for ECL to TTL level translators.
10	INTCLK (TTL)	Interface clock output. This output is a TTL output at one third of the VCO frequency.
11	GND	Ground.
12	V_{CC} (5V)	Logic power supply input, nominally 5V.
13	CAPA	VCO capacitor connection. This capacitor determines the nominal VCO frequency.
14	V_{C1}	V_{C1} should be connected to a well-regulated 5V ± 5% supply.
16	CODECLK (ECL)	The code clock output. This is an ECL output at half the VCO frequency.

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ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range
- V_{C1} ..... –0.3 to V_{CC} + .3 VDC
- V_{C2} ..... –0.3 to 14 VDC
- V_{CC} ..... –0.3 to 6 VDC

Digital Inputs
- ECLIN1, 2 ..... –0.3 to V_{CC} + 0.3V
- QIN1, 2 ..... –0.3 to V_{CC} + 0.3V

Analog Inputs
- LOOPFLTR, INTCAP ..... –0.3 to V_{C2} + 0.3V
- CAPA ..... –0.3 to V_{C1} + 0.3V

Digital Outputs
- TTLOUT1, 2, OSCTP, CODECLK, INTCLK ..... –0.3 to V_{CC} + 0.3V

TYPICAL OPERATING CONDITIONS

Temperature Range ..... 0°C to +70°C
Analog Supply Voltage (V_{C2})* ..... 5 or 12V
Digital Supply Voltage (V_{CC}) 5V
V_{C1} 5V

* This supply voltage is designed for 5V or 12V operation. This data sheet specifies the ML4417/4427 for 12V operation. For 5V specification, please contact Micro Linear.

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied. (All voltages are referenced to GND.)

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{C2} = 12V ± 10%, V_{CC} = 5V ± 5%, V_{C1} = 5V ± 5%, T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
I_{CC}	V_{CC} Supply Current (1)	Pin 12			90.0		mA
I_{C1}	V_{C1} Supply Current	Pin 14			11.0		mA
I_{C2}	V_{C2} Supply Current	Pin 4			4.5		mA
Digital Inputs							
$V_{IH\ (ECL)}$	High Voltage ECL Input	Pin 15, V_{CC} = 5V		4.0			V
$V_{IL\ (ECL)}$	Low Voltage ECL Input	Pin 15, V_{CC} = 5V				3.6	V
$I_{IH\ (ECL)}$	High Current ECL Input	Pin 15, V_{CC} = 5V				1250	µA
$I_{IL\ (ECL)}$	Low Current ECL Input	Pin 15, V_{CC} = 5V		625		1000	µA
Digital Outputs (ECL are Open Emitter)							
$V_{OH\ (TTL)}$	High Voltage TTL Output	I_{OH} = –0.4mA	TTL $OUT_{1, 2, 3}$ Pins 8, 9, 10, V_{CC} = 5V	3.75			V
$V_{OL\ (TTL)}$	Low Voltage TTL Output	I_{OL} = 1.6mA				0.50	V
$V_{OH\ (ECL)}$	High Voltage ECL Output	I_{OH} = –4mA	ECL Code CLK Pin 16, V_{CC} = 5V	4.05	4.22	4.30	V
$V_{OL\ (ECL)}$	Low Voltage ECL Output	I_{OL} = –4mA		2.80	3.22	3.55	V
Voltage Controlled Oscillator (VCO) (Transfer Function Pin 2 to Pin 1 = 7.5MHz/Volt @ 10pF)							
f_{VCO}	VCO Range	C_{OSC} = 10pF Pin 14 to Pin 13 (Pin 2 = 1V to 11V, Pin 3 = 6V) (Pin 14 = V_{CC})			20–95		MHz
Charge Pump							
I_Q	Charge Pump Current	Pin 3			±125		µA
V_{QH}	Charge Pump Maximum Voltage	Pin 3			V_{C2}–1V		V
V_{QL}	Charge Pump Minimum Voltage	Pin 3			1.0		V
INC, $\overline{DEC}$ Inputs							
V_{IH}	High Voltage Input	Pin 6, V_{CC} = 5V		1.9		V_{CC}	V
V_{IL}	Low Voltage Input	Pin 6		0		0.8	V
V_{IH}	High Voltage Input	Pin 5 (ML4417), V_{CC} = 5V		1.9		V_{CC}	V
V_{IL}	Low Voltage Input	Pin 5 (ML4417)		0		0.8	V

Note 1: This value includes current consumed in 1KΩ terminating resistors from pins 1 and 16 to ground.

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, V_{C2} = 12V ± 10%, V_{CC} = 5V ± 5%, V_{C1} = 5V ± 5%, T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INC, $\overline{DEC}$ Inputs (Continued)						
V_{IH}	High Voltage Input	Pin 5 (ML4427) see figure 2, V_{CC} = 5V	4.2		5.0	V
V_{IL}	Low Voltage Input	Pin 5 (ML4427) see figure 2, V_{CC} = 5V	0		3.1	V
I_{IH}	High Current Input	Pin 6, V_{IN} = 1.9V	–5.0		+1.0	µA
I_{IL}	Low Current Input	Pin 6, V_{IN} = 0V	–25		–1,9	µA
I_{IH}	High Current Input	Pin 5 (ML4417), V_{IN} = 5V	+30		+200	µA
I_{IL}	Low Current Input	Pin 5 (ML4417), V_{IN} = 0 → 0.9V	–25		+40	µA
I_{IH}	High Current Input	Pin 5 (ML4427), V_{IN} = 5V	+1.0		+20	µA
I_{IL}	Low Current Input	Pin 5 (ML4427), V_{IN} = 3.1V	–0.1		+7.0	µA
ECL Input 2 (Pin 7) at 25°C, 5MHz < f_{IN} < 35MHz, 40% < Duty Cycle < 60% (If Unused, Pin 7 = V_{CC})						
V_{IH}	High Voltage Input	V_{CC} = 5V	3.0	4.2	5.1	V
V_{IL}	Low Voltage Input	V_{CC} = 5V	2.5	3.4	4.6	V
V_A	Voltage Swing	V_{IH} – V_{IL}, V_{CC} = 5V	.5		2.0	V
I_{IN}	Input Current	DC Bias Value		35		µA
Transconductance Amplifier						
V_{REFI}	Inverting Input of Amplifier			$V_{C2}/2$		V
G_M	Transconductance	ΔI (Pin 2) ÷ ΔV (Pin 3)		27.5		µmho
I_{SAT}	Limiting Value of Output Current	Pin 2		±120		µA

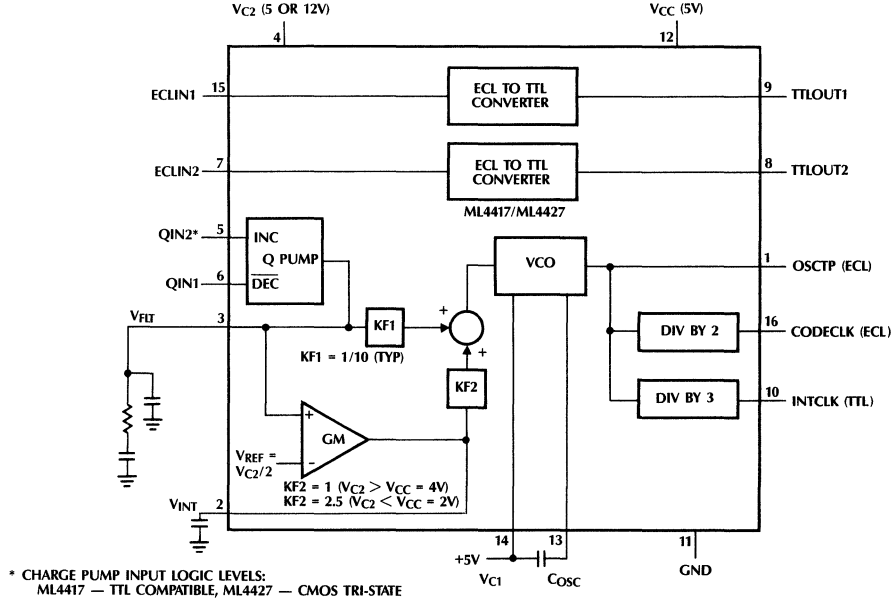


Figure 1. Typical Passive Component Connections

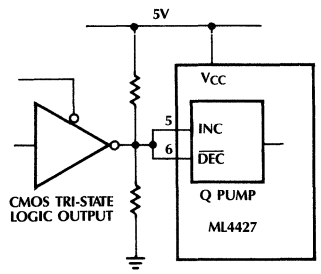
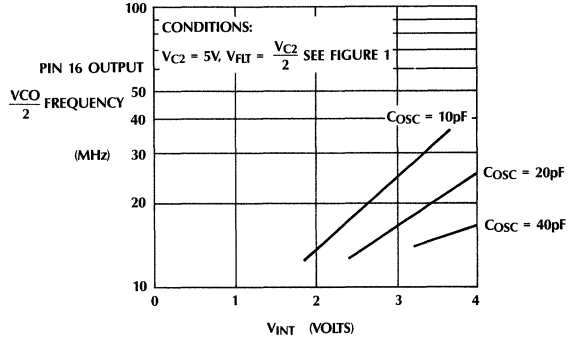


Figure 2.

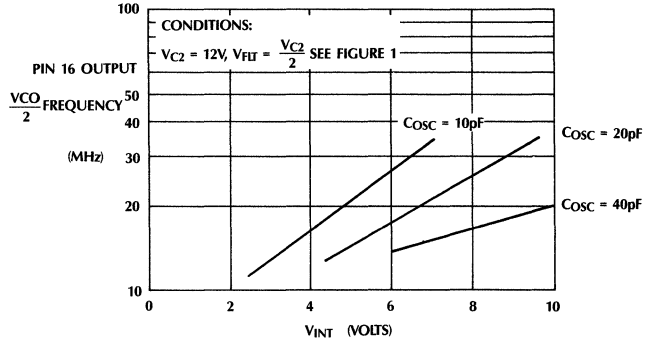
The ML4427 version has an input on pin 5 that allows a single-line control interface on the charge pump. By connecting pins 5 and 6 together, the charge pump can be controlled from a single CMOS tri-state output as follows: HI = increment, LO = decrement, tri-state = coast. The benefit is a savings of one output pin on a control gate array. A resistive termination to $V_{CC}/2$ is required to establish the logic level during tri-state, as shown.

TYPICAL PERFORMANCE CHARACTERISTICS

$\frac{VCO}{2}$ (MHz) vs. V_{INT}
V_{C2} = 5V
(5V-Only Operation)



$\frac{VCO}{2}$ (MHz) vs. V_{INT}
V_{C2} = 12V



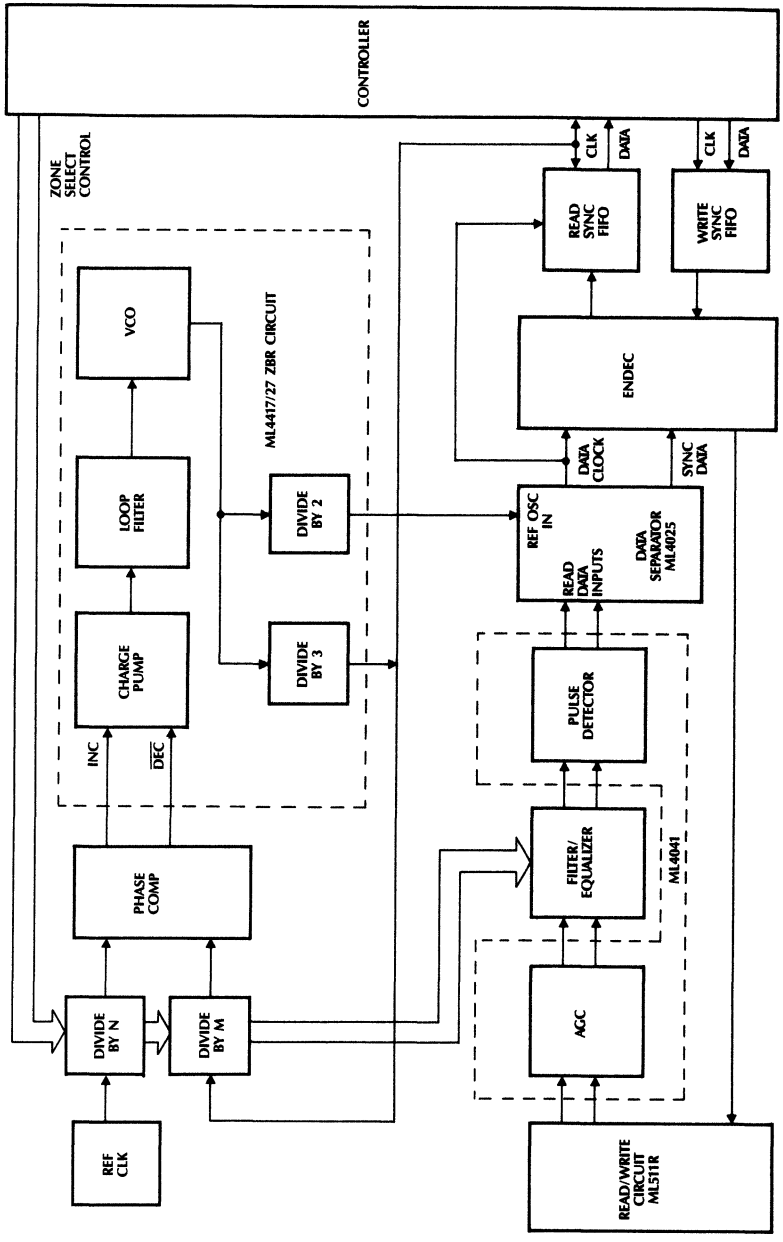


Figure 3. Read Channel Using ML4417/27 ZBR Circuit with RLL (1, 7) Encoding

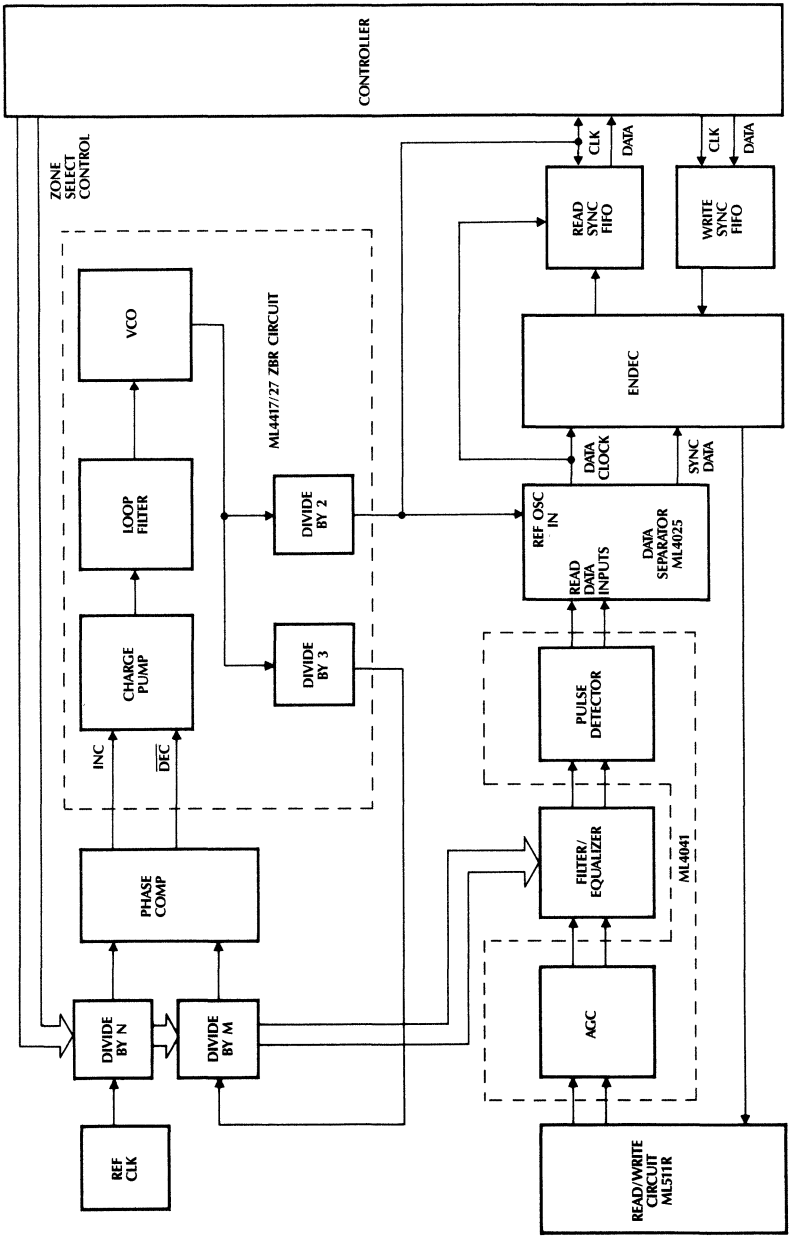
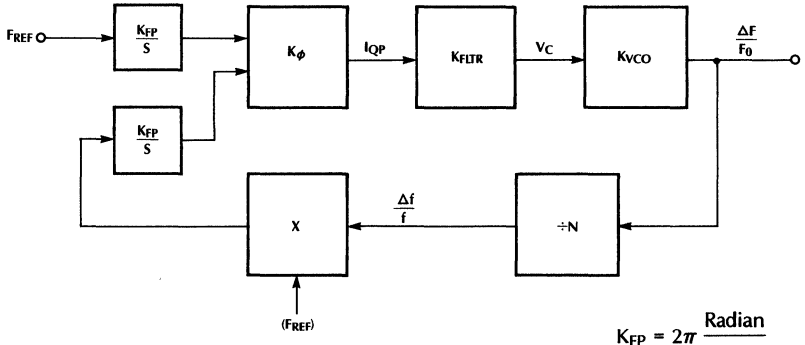


Figure 4. Read Channel Using ML4417/27 ZBR Circuit with RLL (2, 7) Encoding

4417/4427 LOOP RESPONSE

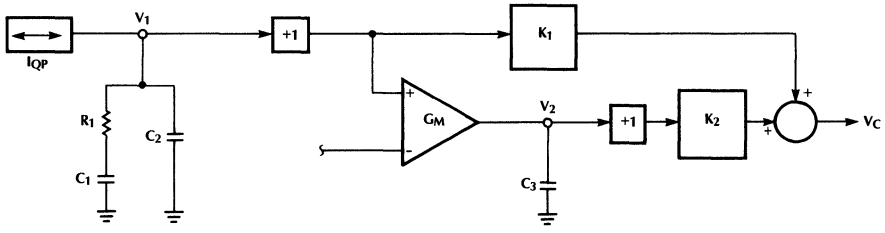


$$K_{FP} = 2\pi \frac{\text{Radian}}{\text{Hertz}}$$

$$K_{\phi} = \frac{.125\text{mA}}{2\pi} \frac{\text{Amp}}{\text{Radian}}$$

K_{FLTR} — To Be Derived, Units = $\frac{\text{Volts}}{\text{Amp}}$

$$K_{VCO} = \frac{100\%}{2.5\text{V}} \frac{\%}{\text{Volt}} \quad (C_{OSC} = 10\text{pF})$$



$$V_1 = I_{QP} * \frac{\left(R_1 + \frac{1}{SC_1}\right)\frac{1}{SC_2}}{R_1 + \frac{1}{SC_1} + \frac{1}{SC_2}} = I_{QP} * \frac{SR_1C_1 + 1}{S(C_1 + C_2)\left(SR_1\frac{C_1C_2}{C_1 + C_2} + 1\right)}$$

$$V_2 = V_1 * \frac{G_M}{SC_3},\ V_C = V_1K_1 + V_2K_2 = V_1\left(K_1 + \frac{G_MK_2}{SC_3}\right) = V_1\frac{S\frac{K_1}{K_2G_M}C_3 + 1}{S\frac{1}{G_MK_2}C_3}$$

$$\therefore \frac{V_C}{I_{QP}} = \frac{G_MK_2\,(SR_1C_1 + 1)\left(S\frac{K_1}{K_2G_M}C_3 + 1\right)}{S^2(C_1 + C_2)C_3\left(SR_1\frac{C_1C_2}{C_1 + C_2} + 1\right)}$$

$$= \frac{(SR_1C_1 + 1)\,(S * 3.6 * 10^3\,C_3 + 1)}{36 * 10^3\,S^2(C_1 + C_2)C_3\left(SR_1\frac{C_1C_2}{C_1 + C_2} + 1\right)} = K_{FLTR}$$

$$K_1 = .1\frac{V}{V}$$

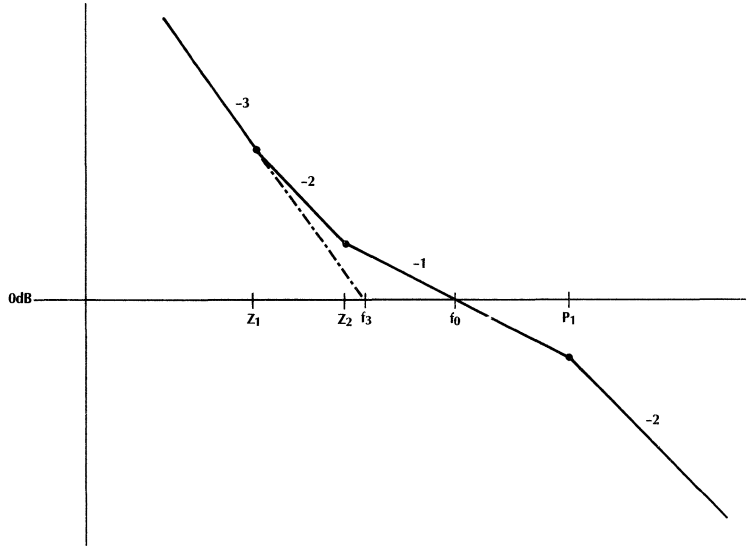
$$K_2 = 1\frac{V}{V}$$

$$G_M = 27.5 * 10^{-6}\frac{\text{Amp}}{\text{Volt}}$$

Thus complete open loop transfer function T_{OL}:

$$T_{OL} = \frac{K_{FP}}{S} * K_{\phi} * K_{FLTR} * K_{VCO} * F_{REF} = \frac{2\pi}{S} * \frac{.125 * 10^{-3}}{2\pi} * K_{FLTR} * \frac{1}{2.5} * F_{REF}$$

$$= \frac{K_{FLTR}}{S} * \frac{F_{REF}}{20 * 10^3} = \frac{(SR_1C_1 + 1)(S * 3.6 * 10^3 C_3 + 1) * F_{REF}}{S^3(C_1 + C_2)C_3\left(SR_1\frac{C_1C_2}{C_1 + C_2} + 1\right) * 720 * 10^6}$$



Must define desired F_{REF}, f_0, Z_2, P_1, Z_1; then can proceed with component value determination.

If $F_{OUT} = 36 * 10^6$, N = 50 (typical numbers), then $F_{REF} = 720 * 10^3$
Assume: f_0 = 1000Hz, Z_2 = 250Hz, P_1 = 3000Hz, Z_1 = 45Hz

1. Set Z_1 with C_3:

$$3.6 * 10^3 * C_3 = \frac{1}{2\pi Z_1} \longrightarrow C_3 = \frac{1}{2\pi * 45 * 3.6 * 10^3} = .982 * 10^{-6} \sim 1\mu F$$

2. Set –3 intercept frequency f_3 with $(C_1 + C_2)$: $f_3 = (Z_1Z_2f_0)^{1/3} = (11.25 * 10^6)^{1/3}$

$$\longrightarrow C_1 + C_2 = \frac{720 * 10^3}{(2\pi)^3 * 11.25 * 10^6 * 10^{-6} * 720 * 10^6} = .358 * 10^{-6}$$

3. Ratio $\frac{Z_2}{P_1} = \frac{R_1\left(\frac{C_1C_2}{C_1 + C_2}\right)}{R_1C_1} = \frac{C_2}{C_1 + C_2} \longrightarrow C_2 = (C_1 + C_2)\frac{Z_2}{P_1} = .358 * 10^{-6} * \frac{250}{3000} = .0298 * 10^{-6} \sim .030\mu F$

4. $C_1 = (C_1 + C_2) - C_2 = .358 * 10^{-6} - .030 * 10^{-6} = .328 * 10^{-6} \sim .33\mu F$

5. Set Z_2 with R_1: $R_1C_1 = \frac{1}{2\pi Z_2} \longrightarrow R_1 = \frac{1}{2\pi * 250 * .33 * 10^{-6}} = 1.929 * 10^3 \sim 1.91K$

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML4417CP	0°C to +70°C	MOLDED DIP (P16)
ML4417CS	0°C to +70°C	MOLDED SOIC (S16N)
ML4427CP	0°C to +70°C	MOLDED DIP (P16)
ML4427CS	0°C to +70°C	MOLDED SOIC (S16N)

Low Saturation Voice Coil Servo Driver

GENERAL DESCRIPTION

The ML4418 is a voice coil power driver intended for use in High Performance 12V Hard Disk servo systems. The ML4418 contains all control circuitry necessary to drive the voice coils of most drives. To maximize compliance voltage, the ML4418 includes two 1-Amp NPN drivers and provides base drive for external PNP transistors. In addition, power fail detection and a low voltage head retraction functions are provided for orderly shut-down of the drive. A current sense amplifier is included to enable voice coil current feedback for velocity calculations. Special care has also been taken to maximize system loop bandwidth.

The transconductance programmed by a logic input at 1/2 A/V and 1/7 A/V respectively, when using a 1Ω sense resistor. This allows for greater DAC resolution in digitally controlled servos during track follow without compromising dynamic range during seek.

The retraction circuit, main drive circuit, and control circuits are each powered from their own supplies. Retract is self-contained for 12V systems but allows the use of an external PNP to allow retraction with as little as 1V of back EMF from the spindle.

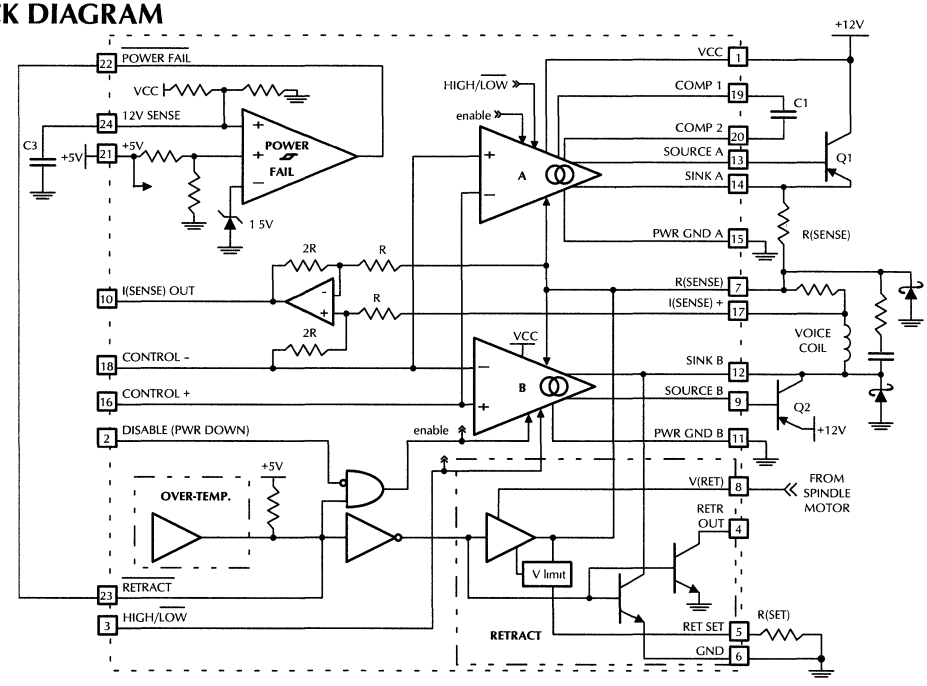
The power fail detection circuit includes a precision 1.5V bandgap reference and a power fail comparator.

The ML4418 is implemented using Micro Linear's bipolar array technology. This allows for customization of the IC for a user's specific application.

FEATURES

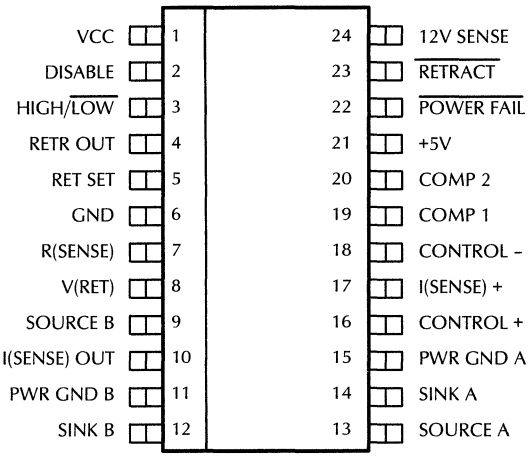
- Low saturation voltage (<1V at 1A.)
- No cross-over distortion with low quiescent current
- VCM coil current output referenced to V_{REF}
- Pin-programmable transconductance settings
- Retraction circuitry with programmable retract voltage and separate power pin operates to 1V
- On-chip precision power fail detect circuitry
- Over-temperature protection with flag output
- Operates from +12 supplies

BLOCK DIAGRAM



PIN CONFIGURATION

ML4418
24-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	VCC	Supply input to power amplifiers
2	DISABLE	A Logic "1" puts the IC into a low power state and disables the power amplifiers.
3	HIGH/$\overline{\text{LOW}}$	A logic "1" sets the transconductance gain to 1/2 while a logic "0" sets the gain to 1/7. Transconductance gain is the $V_{R(SENSE)} \div V_{CONTROL}$.
4	RETR OUT	Open collector output which pulls low during retract. Used to provide a braking signal to spindle.
5	RET SET	External set resistor to establish a voltage limit for the internal retract driver.
6	GND	Analog signal ground.
7	R(SENSE)	Current sense resistor terminal.
8	V(RET)	Supply pin for retract circuits.
9	SOURCE B	PNP Base drive output for inverting power amplifier.
10	I(SENSE) OUT	Output of the Current Sense amplifier
11	PWR GND B	Power return pin for inverting power amplifier B.
12	SINK B	Current sinking output for inverting power amplifier. Connects to voice coil (-) terminal.
13	SOURCE A	PNP Base drive output for non-inverting power amplifier.
14	SINK A	Current sinking output for non-inverting power amplifier. Connects to voice coil (+) terminal.
15	PWR GND A	Power return pin for non-inverting power amplifier A.
16	CONTROL +	Positive input for current command.
17	I(SENSE) +	Positive input for current sense amplifier.
18	CONTROL -	Negative input for current command.
19	COMP 1	Pin for external compensation capacitor.
20	COMP 2	Pin for external compensation capacitor.
21	+5V	Input for +5V for power fail detection and logic power supply.
22	$\overline{\text{POWER FAIL}}$	Open Collector output drives low for low voltage conditions.
23	$\overline{\text{RETRACT}}$	A logic "0" initiates retract. Also used as an open-collector over-temperature output flag.
24	12V SENSE	Input to the power fail comparator from a resistor divider from VCC.

5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pins 1,8) 14V
Voltage pins 2, 3, 23, 22 ..... -0.3V to +7V
pins 4,7,8,9,12,13,14,17 ..... -0.3V to VCC
Output Sink Current ..... ± 1A
Retraction Current 80mA
Retract set current (pin 5) ..... 3 mA
Junction temperature ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 260°C
Thermal Resistance (θ_{JA}) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
VCC Supply Voltage ..... 10.8V to 13.2V
+5V (pin 21) Supply Voltage ..... 4.5V to 5.5V
V(RET) (pin 8) Supply Voltage ..... 2.5V to 13.2V
CONTROL + Voltage Range (pins 16) ..... 0V to VCC
CONTROL - Voltage Range (pins 18) ..... 2.4V to 6.0V

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A=Operating Temperature Range, VCC=operating range, R_{SENSE}=1Ω, R_{COIL}=15Ω CONTROL - (pin 18) = VCC/2, R_{SET} (pin 5) = 7.5KΩ, C1=30pF, Q1=Q2= MJE210.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Amplifier					
Offset				±12	mA
Common Mode Transconductance	$2V \le V_{PIN18} \le 6V$		0.5	1	mA/V
Gain	pin 3 = 2V	475	500	525	mA/V
	pin 3 = 0.8V	136	143	150	mA/V
Maximum Bandwidth			100		Khz
Sinking saturation	I_{OUT} = 100mA		0.3	0.6	V
	I_{OUT} = 300mA		0.4	0.8	V
	I_{OUT} = 500mA		0.5	1	V
Sourcing saturation	I_{OUT} = 100mA		0.1		V
	I_{OUT} = 300mA		0.2		V
	I_{OUT} = 500mA		0.3		V
Source A/B Base Drive		20	30	50	mA
Q1/Q2 Standby Current	β_{PNP} = 200, V_{PIN16} = 5V	1	4	7	mA
Retraction Circuit					
Turn on time			800		nS
Turn off time			8		µS
Source Voltage	V_{PIN23}=0.8V, V_{PIN8}= 3V, I_{PIN7}= –50mA	0.53	0.75	0.97	V
Sink Current	V_{PIN23}=0.8V, V_{PIN8}= 1.2V, V_{PIN12}= 0.6V	36	48	150	mA
RETR OUT V_{OL}	V_{PIN23}=0.8V, I_{PIN4}=1mA			0.4	V
Power Fail Detection Circuit					
12V Threshold		9.5	10	10.5	V
Hysteresis - 12V Sense		5	120	190	mV
5V Threshold		4.35	4.525	4.70	V
Hysteresis - 5V Sense		5	30	80	mV
Logic Inputs and Outputs					
Voltage High (V_{IH})		2	1.4		V
Voltage Low (V_{IL})			1.4	0.8	V
Current High (I_{IH})	V_{IN}=5V			±10	µA
Current Low (I_{IL})	V_{IN}=0V, except pin 23	–40	–10		µA
	V_{IN}=0V, pin 23 only	–250	–160		µA
Voltage Low (pins 22, 4)	I_{OL}=1mA			0.4	V

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, T_A=Operating Temperature Range, VCC=operating range, R_{SENSE}=1Ω, R_{COIL}=15Ω CONTROL - (pin 18) = VCC/2, R_{SET} (pin 5) = 7.5KΩ, C1=30pF, Q1=Q2= MJE210.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Over-Temperature Detection					
T_j Threshold		150	160		°C
Hysteresis			30		°C
Current Sense Amplifier					
Voltage Offset				±50	mV
Differential Mode Gain		1.95	2	2.05	V/V
Common Mode Gain		-44			dB
Current Consumption					
Pin 21	Pin 21 = 5.5V		5	8	mA
Pin 1	VCC=13.2V, V_{PIN16} = VCC/2		8	13	mA
Pin 8	V_{PIN8} = 13.2V, V_{PIN23} = 5V		3.5	5	mA

FUNCTIONAL DESCRIPTION

POWER AMPLIFIER

The ML4418 power amplifier circuit is set up as a Howland Current source with a fixed gain of 1/2 or 1/7 (set by driving pin 3 high or low respectively). This architecture yields minimal cross-over distortion while maintaining low output cross conduction currents.

The gain figure refers to the ratio of input voltage to the output voltage seen across R_{SENSE}. For example, at a 1/2 gain setting, with V(-) input at 2.5V and the V(+) input at 3V, +500mA would flow through the coil using a 0.5Ω sense resistor. Under the same conditions with pin 3 low, the current would be 143mA. The ability to change from low to high gain allows more complete utilization of DAC resolution when in the track follow mode.

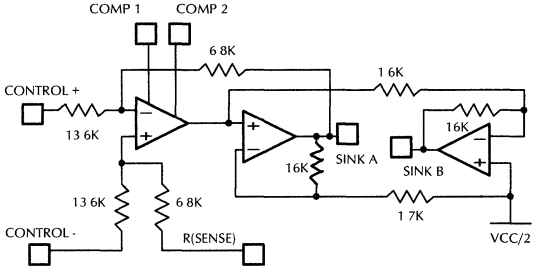


Figure 1. Power Amplifier Topology

The output stage is designed to provide minimal saturation losses and employs an external PNP transistor for the sourcing drive and an internal saturable NPN to sink current. Sinking saturation drop is typically under 0.4V. Sourcing saturation drop depends on the external transistors used. To avoid oscillation in the output stage, PNP transistors with $F_\tau \geq 50$Mhz. should be used.

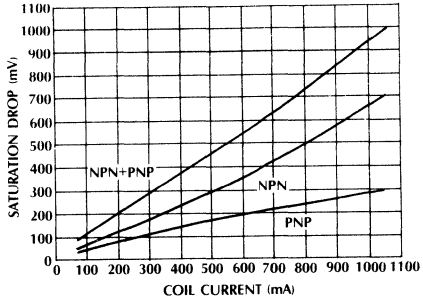


Figure 5. Output Saturation Voltage vs. Output Current (Q1 = Q2 = MJE210)

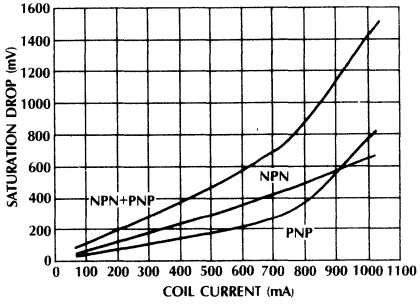


Figure 6. Output Saturation Voltage vs. Output Current (Q1 = Q2 = BSR31)

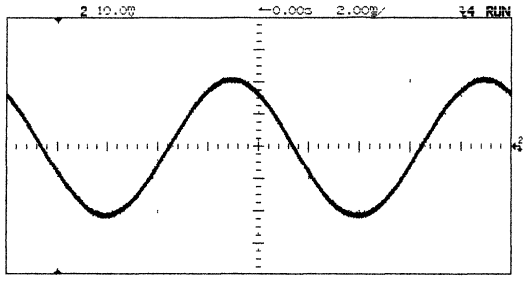


Figure 4. Output Current : V_{IN} = 100 Hz Sine Wave, 2.4V_{P-P}, Low Gain Mode (V_{PIN3}=0), R(SENSE) = 1Ω

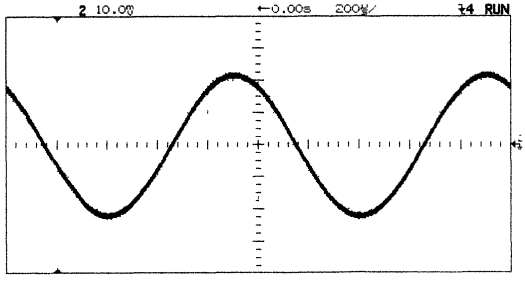


Figure 5. Output Current: V_{IN} = 1 KHz Sine Wave, 2.4V_{P-P} Low Gain Mode (V_{PIN3} = 0), R(SENSE) = 1Ω

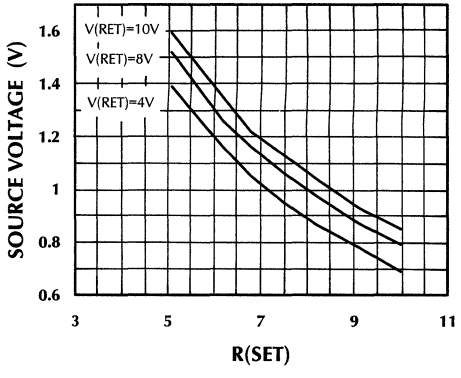


Figure 6. Retract Source Voltage at Pin 7 vs. R(SET) I_{VCM}=50mA

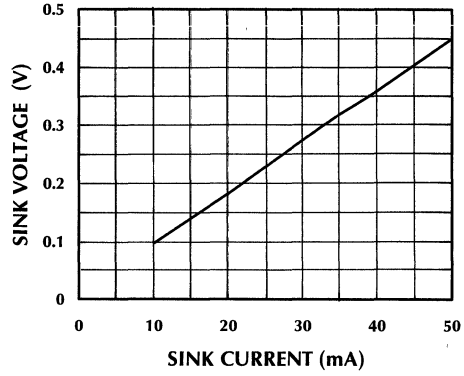


Figure 7. Retract Sink Voltage at Pin 12 vs. I_{VCM}=50mA

POWER FAIL DETECT CIRCUIT

The ML4418 circuit consists of a precision trimmed reference, resistor dividers and an "or function" comparator with hysteresis. The output (open collector) of this circuit appears on pin 22. When either comparator input falls below the 1.5V reference, pin 22 pulls low.

RETRACT CIRCUITS

The ML4418 retract circuit provides for spindle EMF energized power fail retraction of the VCM. When pin 23 goes low, pin 4 will pull low, providing a signal which can be delayed for spindle braking. The internal NPN transistor will saturate, pulling SINK B (pin 12) low. This portion of the circuit will function with less than 1V on V(RET). An internal voltage limited pull-up transistor is provided which sources current on pin 7 to the VCM. This circuit will operate reliably down to a V(RET) voltage of around 2.5V, making the ML4418 retract circuit adequate for 12V systems where the spindle motor EMF provided is adequate.

Figure 6 shows the saturation characteristics of the SINK B output ($R_{SAT} \approx 9\Omega$) The R_{SAT} of the pull down transistor does not vary appreciably with V(RET) voltage. Figure 7 shows the voltage sourced at R(SENSE) during Retract vs. R(SET) at various V(RET) input voltages.

CURRENT SENSE AMPLIFIER

The current sense amplifier in the ML4418 creates a signal referenced to CONTROL - (normally the Vref pin of the system's DAC and ADC) appearing accross a resistor in series with the VCM. Its output is twice the voltage that appears between pins 17 and 7.

APPLICATIONS

POWER AMPLIFIER COMPENSATION

Figure 8 below shows the equivalent AC circuit for the current amplifier.

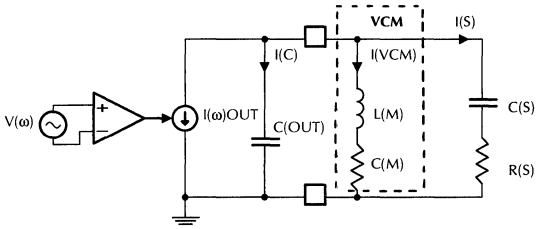


Figure 8. AC Equivalent Circuit for Current Amplifier, Voice Coil Motor (VCM) and Snubber

The amplifier's current bandwidth is limited by C_{OUT} which varies with the value chosen for R_{SENSE}

$$C_{OUT} \approx \frac{1197 \times (C_{COMP} + 3.5pF)}{R_{SENSE}}$$

Where C_{COMP} is C1 between pins 19 and 20. With no snubber (RS and CS) the bandwidth is limited to.

$$F_{-3dB} = \frac{1}{2\pi}\sqrt{\frac{2.414}{L(M)\ C(OUT)}}$$

Since this is a second order system with L(M) and C(OUT) forming a resonant circuit, some damping is desirable to reduce ringing in the step response. This is accomplished with a resistive snubber. The optimum value of R(S) occurs when the following condition is met:

$$R(S) = \sqrt{\frac{L(VCM)}{C(OUT)}}$$

For a given C(S), setting R(S) to this value will minimize the ringing in the transient response. Larger values of R(S) will result in more ringing and more bandwidth. Smaller values of R(S) will result in more ringing and less bandwidth.

C(S) (snubber capacitor) values of between 200nF and 1 µF are usually necessary to achieve the desired reduction of ringing in the step resonse. At the optimum value of R(S) larger values of C(S) further reduce the ringing but do not affect the bandwidth.

Tuning the current loop response can be easily done simulating the network in figure 8 with a computer simulator (such as SPICE).

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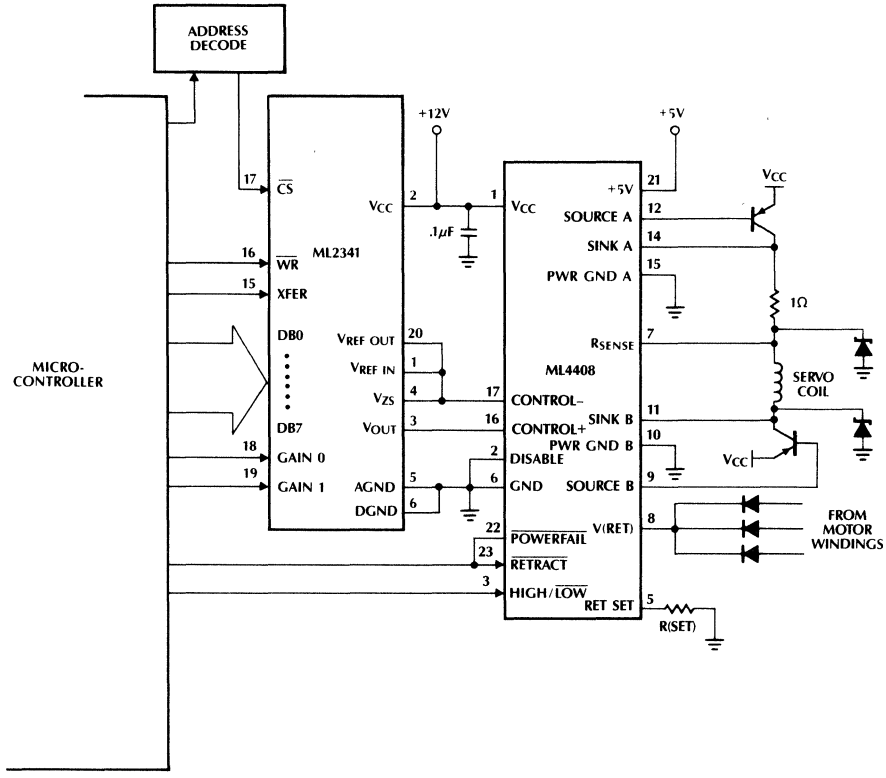

Figure 9. ML4418 Used with ML2341 8-Bit Gain Ranging DAC Provides up to 13-Bit Effective Resolution

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4418CS	0°C to +70°C	S20W

ML4420

Enhanced Sensorless BLDC Motor Controller

GENERAL DESCRIPTION

The ML4420 motor controller provides complete commutation for delta or wye wound Brushless DC (BLDC) motors without the need for signals from Hall Effect Sensors to indicate rotor position. It senses the back EMF of the motor windings (no neutral required) to determine the proper commutation phase sequence using PLL techniques. The ML4420 uses a patented Back-EMF sensing technique which will commutate virtually any 3-phase BLDC motor and is insensitive to PWM noise and motor snubbing circuitry.

The ML4420 controls the motor current with a constant off-time PWM or with a microprocessor controlled constant frequency PWM input. The velocity loop can be controlled with an external microprocessor or through an analog feedback loop. An accurate, jitter-free, VCO output is provided, equal to the commutation frequency of the motor. The ML4420 modulates the gates of external N-channel power MOSFETs to regulate the motor current and directly drives the P-channel MOSFETs. The ML4420 supports enhancements like a blanker circuit to prevent false retriggering of the one shot during a motor current spike and circuitry to ensure that there is no shoot through in any state.

The start-up algorithm consists of measuring a fixed VCO frequency and externally ramping the commutation clock until it is equal to the VCO frequency. The timing of the start-up sequencing is determined by the microprocessor thus allowing the optimization for a wide range of motors and inertial loads.

FEATURES

- Less than 200mW power dissipation
- Patented Back-EMF commutation technique provides jitterless torque for minimum "spin-up" time
- PWM motor current control
- Microprocessor based start-up algorithm allows for optimized start-up sequencing, speed control and support for variable motor loads
- Back-EMF comparator output senses motor rotation after power fail for fast re-lock after brownout
- Onboard power fail detect monitor
- Onboard motor braking circuit allows 'life' braking on command
- Drives external N-ch & P-ch FETs
- Enhanced version of the ML4410 & ML4411

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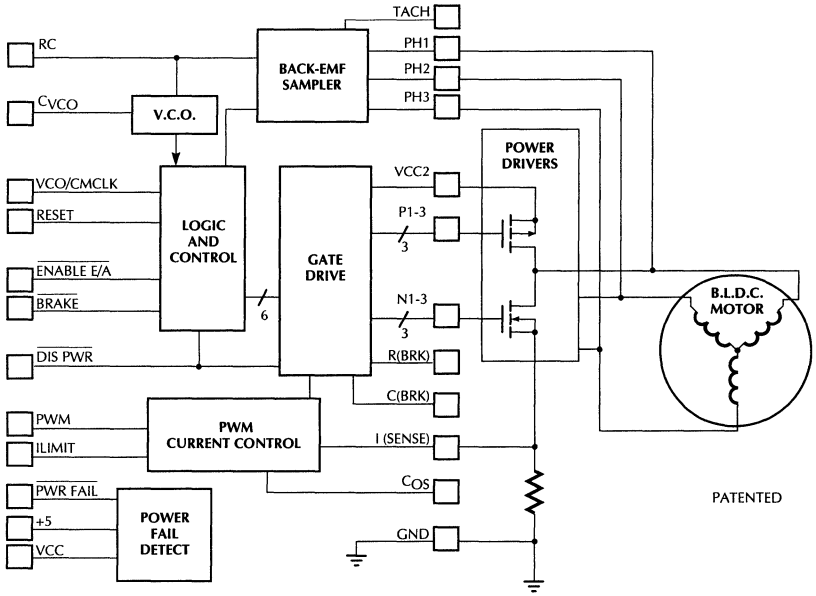
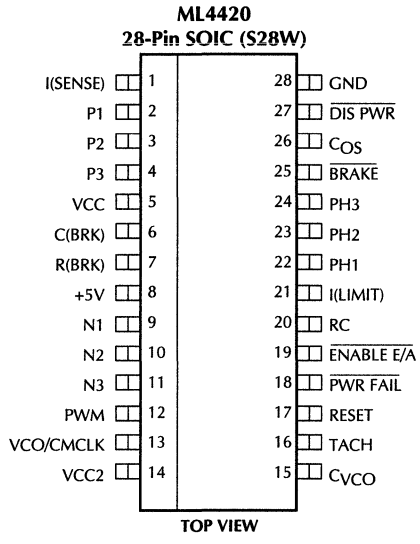
BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	I(SENSE)	Motor current sense input
2	P1	Drives the external P-Channel transistor driving motor PH1
3	P2	Drives the external P-Channel transistor driving motor PH2
4	P3	Drives the external P-Channel transistor driving motor PH3
5	VCC	12V power supply. Terminal which is sensed for power fail
6	C(BRK)	Capacitor which stores energy to charge N-Channel MOSFETs for braking with power off
7	R(BRK)	External resistor to C(BRK) to drive NMOS during braking
8	+5V	5V power supply input
9-11	N1, N2 N3	Drives the external N-channel MOSFETs for PH1, PH2, PH3
12	PWM	TTL input of PMW signal
13	VCO/CMCLK	Logic Output from VCO serves as an input pin for the commutation clock used in start-up sequencing
14	VCC2	12V power and power for the braking function
15	C_{VCO}	Timing capacitor for VCO
16	TACH	Logic Output from TACH comparator
17	RESET	Input which holds the VCO off and sets the IC to the RESET condition (refer table 1)
18	$\overline{\text{PWR FAIL}}$	A "0" output indicates 5V or 12V is under-voltage. This is an open collector output with a 4.5kΩ pull-up to +5V
19	$\overline{\text{ENABLE E/A}}$	A "0" logic input enables the error amplifier and closes the Back-EMF feedback loop (refer table 1)
20	RC	VCO loop filter components
21	I(LIMIT)	Sets the threshold for the PWM comparator
22	PH1	Motor Terminal 1
23	PH2	Motor Terminal 2
24	PH3	Motor Terminal 3
25	$\overline{\text{BRAKE}}$	A "0" activates the braking circuit
26	C_{OS}	Timing capacitor to GND and resistor to +5V, for fixed off-time PWM current control
27	$\overline{\text{DIS PWR}}$	A logic 0 on this pin turns off the N and P outputs and causes the TACH comparator output to appear on TACH OUT
28	GND	Signal and Power Ground

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (pins 5, 14) 14V
Output Current (pins 2, 3, 4, 9,10,11) ..... ±150mA
Logic Inputs (pins 14, 17, 18, 25) ..... –0.3 to 7V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 150°C
Thermal Resistance (θ_{JA}) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
VCC Voltage +12V (pin 14) ..... 12V ± 10%
+5V (pin 8) ..... 5V ± 10%
I Control Voltage Range (pins 13, 21) ..... 0V to 7V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, VCC = VCC2 = 12V, R_{SENSE} = 1Ω, C_{VCO} = 0.01µF, C_{OS} = 0.001µF, R_{OS} = 10kΩ

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator (VCO) Section					
Frequency vs. V_{PIN20}	$1V \le V_{PIN20} \le 10V$		300		Hz/V
Frequency	V_{VCO} = 6V	1450	1800	2150	Hz
	Reset mode	70	140	210	Hz
Sampling Amplifier (note 1)					
V_{RC}	State R	400	500	600	mV
I_{RC}	State A, V_{PH2} = 4V	30	50	70	µA
	State A, V_{PH2} = 6V	–13	2	13	µA
	State A, V_{PH2} = 8V	–30	–50	–70	µA
Motor Current Control Section					
I(SENSE) Gain	V_{PIN21} = 2.5V	4.5	5	5.5	V/V
One Shot off time		8	12	16	µS
Power Fail Detection Circuit					
12V Threshold		9.1	9.8	10.5	V
Hysteresis			150		mV
5V Threshold		3.8	4.25	4.5	V
Hysteresis			70		mV
Logic Inputs					
Voltage High (V_{IH})		2			V
Voltage Low (V_{IL})				0.8	V
Current High (I_{IH})	V_{IN} = 2.7V	–300	1	300	µA
Current Low (I_{IL})	V_{IN} = 0.4V	–150	0	150	µA
Braking Circuit					
Brake Active Threshold		1.0	1.4	1.8	V
PIN 25 Bias Current	V_{PIN25} = 0V	–10	0.3	10	µA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, T_A = Operating Temperature Range, VCC = VCC2 = 12V, R_{SENSE} = 1Ω, C_{VCO} = 0.01µF, C_{OS} = 0.001µF, R_{OS} = 10kΩ

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Outputs I(LIMIT) = 2.5V					
I_P low	V_P = 2V	0.5		1.2	mA
V_P high	I_P = –10µA	VCC2 – 1V			V
P3 Comparator Threshold		VCC2 – 3.6V		VCC2 – 2.4V	V
V_N high	V_{PIN1} = 0V	VCC – 3.2	10	VCC – 1.2	V
V_N low	I_N = 1mA		0.2	0.7	V
LOGIC low (V_{OL})	I_{OUT} = 0.4mA			0.5	V
VCO/TACH V_{OH}	I_{OUT} = 100µA	2.4			V
POWER FAIL V_{OH}	I_{OUT} = 10µA	V_{PIN8} – 0.2	V_{PIN8} – 0.1	V_{PIN8}	V
Supply Currents (N and P outputs open)					
5V Current			16	25	mA
VCC Current			1	2	mA
VCC2 Current			8	16	mA

Note 1. For explanation of states, see Figure 5 and Table 1.

SUMMARY OF ENHANCEMENTS IN ML4420 OVER THE ML4411

1. Lower power dissipation, 200mW versus 450mW in the ML4411.
2. Accurate and customized start-up by using commutation clock provided by the microprocessor instead of relying on I_{RAMP} as in the ML4411.
3. True braking function which is biased by TOB, to allow braking block to work under a power loss situation.
4. ML4420 adds hysteresis into braking comparator to accelerate the transition as soon as the (Vth) threshold is reached.
5. ML4420 adds comparator to prevent the PMOS from coming "ON" when the braking is active.
6. ML4420 adds active pull-up to the P output to replace the resistor pull-up in ML4411.
7. ML4420 enhances pull-down capability to the N output to prevent injected shoot through (only 3 mA in the ML4411).
8. ML4420 adds comparator to prevent P3 N3 shoot through during reset to state A transition.
9. The one-shot accuracy in the ML4420 is improved over the ML4411's.
10. ML4420 adds a blanker circuit to one-shot to prevent it from false triggering which occurrs when large starting currents cause noise coupling to the chip.
11. Directly controls speed through external PWM input.

FUNCTIONAL DESCRIPTION

The ML4420 provides closed-loop commutation for 3-phase brushless motors. To accomplish this task, a VCO, Integrating Back-EMF Sampling error amplifier and sequencer form a phase-locked loop, locking the VCO to the back-EMF of the motor. The IC also contains circuitry to control motor current with either constant frequency or constant off-time PWM modes. Braking and power fail detection functions are also provided on chip. The ML4420 is designed to drive external power transistors (N-channel sinking transistors and P-Channel sourcing transistors) directly.

Start-up sequencing and motor speed control are accomplished by a microcontroller. Speed sensing is accomplished by monitoring the output of the VCO, which will be a signal, phased-locked to the commutation frequency of the monitor.

BACK-EMF SENSING AND COMMUTATOR

The ML4420 contains a patented back-EMF sensing circuit which samples the phase which is not energized (Shaded area in figure 2 below) to determine whether to increase or decrease the commutator (VCO) frequency. A late commutation causes the error amplifier to charge the filter (RC) on pin 20, increasing the VCO input while early commutation causes pin 20 to discharge. Analog speed control loops can use Pin 20 as a speed feedback voltage.

The input impedance of the three PH inputs is about 5kΩ to GND. When operating with a higher voltage motor, the PH inputs should be divided down in voltage so that the maximum voltage at any PH input does not exceed VCC.

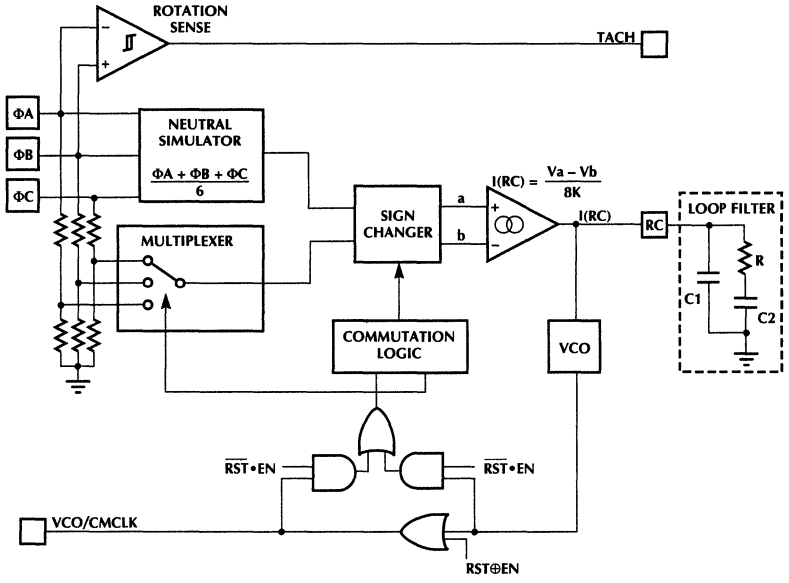


Figure 1. Back-EMF sensing block diagram

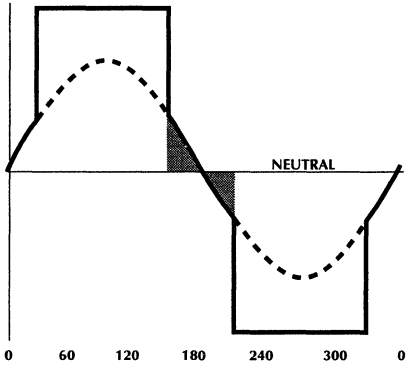


Figure 2. Typical motor phase waveform with Back-EMF superimposed (Ideal Commutation)

VCO AND PHASE DETECTOR CALCULATIONS

The VCO should be set so that at the maximum frequency of operation (the running speed of the motor) the VCO control voltage will be no higher than VCC_{MIN} – 1V. The VCO maximum frequency will be:

$$F_{MAX} = 0.05 \times POLES \times RPM$$

where POLES is the number of poles on the motor and RPM is the maximum motor speed in Revolutions Per Minute.

The minimum VCO gain derived from the specification table (using the minimum F_{VCO} at V_{VCO} = 6V) is:

$$K_{VCO(MIN)} = \frac{2.42 \times 10^{-6}}{C_{VCO}}$$

Assuming that the $V_{VCO(MAX)}$ = 8.0V, then

$$C_{VCO} = \frac{8.0 \times 2.42 \times 10^{-6}}{F_{MAX}}$$

or

$$C_{VCO} = \frac{436}{POLES \times RPM}\,\mu F$$

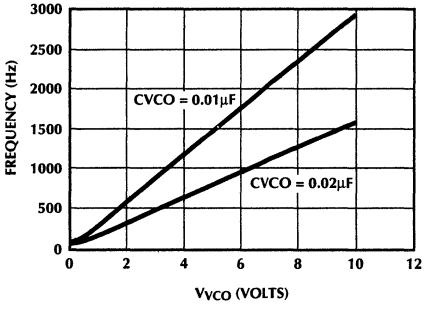


Figure 3. VCO Output Frequency vs. V_{VCO} (pin 20)

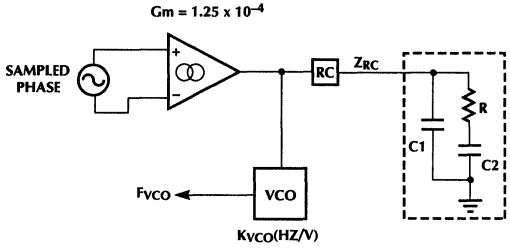


Figure 4. Back EMF Phase Lock Loop Components

Figure 4 above shows the transfer function of the Phase Lock Loop with the phase detector formed from the sampled phase through the Gm amplifier with the loop filtered formed by R, C_1, and C_2.

The impedance of the loop filter is

$$Z_{RC}(s) = \frac{1}{C_1 s} \frac{(s+\omega_{LEAD})}{(s+\omega_{LAG})}$$

Where the lead and lag frequencies are set by:

$$\omega_{LEAD} = \frac{1}{RC_2}$$

$$\omega_{LAG} = \frac{C_1 + C_2}{RC_1C_2}$$

START-UP SEQUENCING

When the motor is initially at rest, it is generating no back-EMF. Because a back-EMF signal is required for closed loop commutation, the motor must be started "open-loop" until a velocity sufficient to generate some back-EMF is attained. The following steps are a typical procedure for starting a motor which is at rest. It is possible to determine if the motor is running by polling the TACH OUT pin 16 with power disabled (Pin 27 = low).

STEP 1 The IC is held in reset state until the platters are steady by setting pin 17 and pin 19 to a '1', with full power applied to the winding (see figure 5). This aligns the rotor to a position which is 30° (electrical) before the center of the first commutation state. Pin 20 is held at 0.5V internally. Microprocessor needs to measure VCO frequency by setting pin 27 to a '1' and then store it.

STEP 2 Setting pin 17 to a '0' and pin 19 to a '1' holds the IC in a ramping state. Microprocessor sends starting commutation clock to pin 13 which is an input pin in this state. This clock frequency is gradually increasing until it reaches the VCO frequency previously stored in Step 1.

STEP 3 As soon as commutation clock reaches the VCO frequency of Step 1, pin 19 is switched to "0" while pin 17 remains '0'. Now the PLL is closed and the VCO is locked to the Back EMF. Pin 13 becomes an output pin. Thus the commutation clock from the microprocessor should be held in tri-state.

Table 1 Commutation, Braking and PLL States

STATE	OUTPUTS						INPUT SAMPLING
	N1	N2	N3	P1	P2	P3	
R OR 0	OFF	ON	OFF	ON	OFF	ON	N/A
A	OFF	OFF	ON	ON	OFF	OFF	PH2
B	OFF	OFF	ON	OFF	ON	OFF	PH1
C	ON	OFF	OFF	OFF	ON	OFF	PH3
D	ON	OFF	OFF	OFF	OFF	ON	PH2
E	OFF	ON	OFF	OFF	OFF	ON	PH1
F	OFF	ON	OFF	ON	OFF	OFF	PH3

Table 2 Start-up Sequence

STATE	$\overline{\text{ENABLE}}$ PIN 19	RESET PIN 17	PIN20 (RC)	VCO	COMMUTATOR
RESET	1	1	0.5V	RUNNING PER V_{PIN20}	IN RESET STATE
RAMP	1	0	0.5V	PRESET	CLOCKED FROM COMMUTATION CLOCK
RUN	0	0	DRIVEN BY PLL	RUNNING PER V_{PIN20}	SEQUENCED BY VCO
BRAKE	0	1	X	X	X

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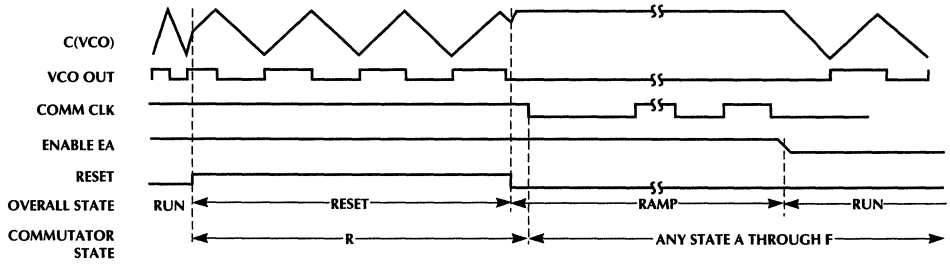


Figure 5. Start up sequencing (from stop)

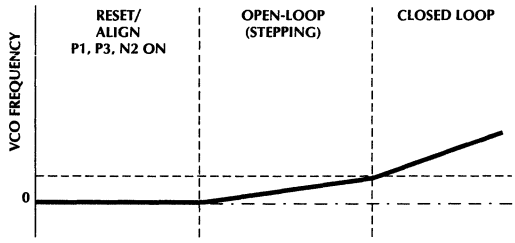


Figure 6. Typical Start-up Sequence

Using this technique, some reverse rotation is possible. The maximum amount of reverse rotation is 360/N, where N is the number of poles. For an 8 pole motor, 45° reverse rotation is possible.

PWM CURRENT CONTROL

To facilitate speed control, the ML4420 has a PWM input pin to receive a constant frequency PWM signal generated from an external speed control loop.

The ML4420 also includes a current mode constant off-time PWM circuit. When motor current builds to the threshold set on I(LIMIT) input (pin 21), a one-shot is fired whose timing is set by C_{OS} and R_{OS} where

$$t_{OFF} = 1.3 \times R_{OS} \times C_{OS}$$

The I(SENSE) input pin should be kept below 1V. If I(SENSE) goes above 1V, a bias current of about –300µA will flow out of pin 1 and the N outputs will be inhibited. Bringing I(SENSE) below 0.7V returns the bias current to its normal level For this reason, the noise filter resistor on the I(SENSE) pin (1kΩ on Figure 8) should be less than 1.5kΩ.

The noise filter time constant should be great enough to filter the leading edge current spike when the N-FETs turn on but small enough to avoid excessive phase shift in the I(SENSE) signal.

OUTPUT DRIVERS

The motor's source drivers (P1 thru P3) are NPN emitter followers. N3 is inhibited until P3 is within 3V (typ) of VCC2. Drivers N1 through N3 are totem-pole outputs capable of sinking 10mA. Switching noise in the external MOSFETs is reduced by an internal 4KΩ resistor in series with the sourcing NPN to form an RC time constant with the N-Channel gate capacitance.

BRAKING

As shown in Figure 7 the braking circuit pulls the N-channel MOSFET Gates high when the BRAKE pin falls below a 2 × Vbe threshold (Vth). After a power failure, C(DLY) is discharged slowly through R(DLY) providing a delay for retract to occur before the braking circuit is activated. The P-channel MOSFETs are turned off well before braking occurs. As soon as the Vth threshold is reached, the braking comparator with hysteresis will accelerate the transition and tri-state the N-channel buffer (B1, refer figure 7) before C(BRK) dump charges into the N-channel Gates. This is to ensure that no charge from C(BRK) is lost through the pull-down transistors in B1, (figure 7). The C(BRK) will continue charging the N-channel Gates, to ensure braking, even when VCC2 (motor BEMF rectified through the MOSFET body diode), drops due to the braking process. An external signal could be used to brake the motor. To accomplish this set pin 17 = '1', pin 19 = '0'. This will pull pin 26 below the threshold to activate the braking circuit.

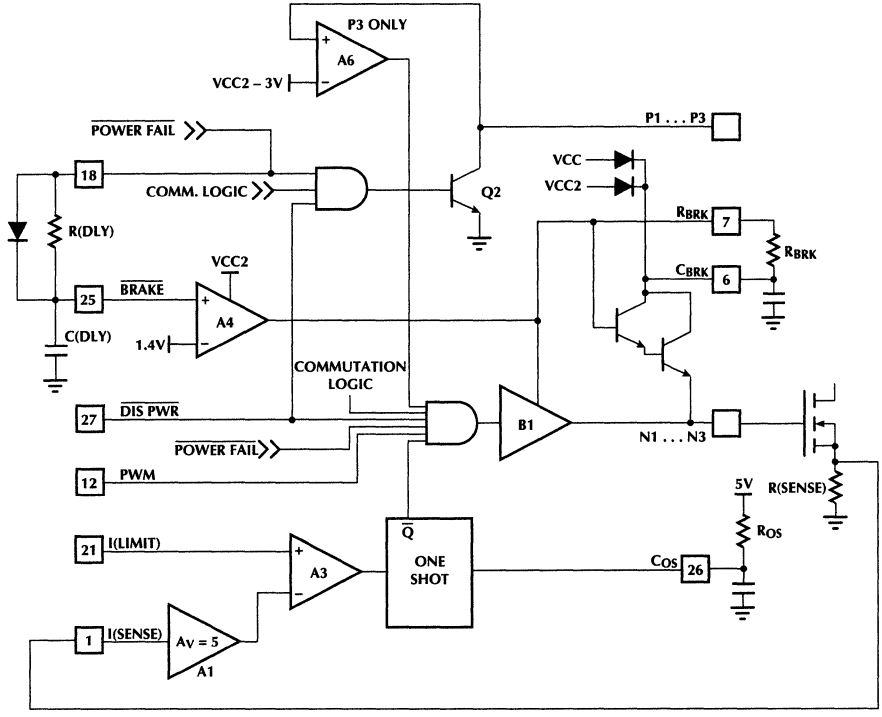


Figure 7. PWM Current Control, Gate Drive and Braking Circuits

APPLICATIONS

Figure 8 shows a typical application of the ML4420 in a hard disk drive spindle control. The timing needed to start the motor in most applications would be generated by a microcontroller.

Speed control can be accomplished either by:

1. Sensing the VCO OUT frequency with a Microcontroller and adjusting the duty cycle of PWM signal sending into PWM pin.
2. Using analog circuitry for speed control. (Fig. 9)

OUTPUT STAGE HINTS

In the circuit in Figure 8, Q1, Q2 and Q3 are IRFR9024 or equivalent. Q4, Q5 and Q6 are IRFR024 or equivalent. New MOSFET packaging technology such as the Little Foot® series may decrease the PC board space. These packages, however have much lower thermal inertia and dissipation capabilities than the larger packages, and care should be taken not to exceed their rated current and junction temperature.

Since the output section in a full bridge application consists of three half-H switches, cross-conduction can occur. Cross conduction is the condition where an N-FET and P-FET in the same phase of the bridge conduct simultaneously. This could happen under two conditions (see Figure 10):

1. When transitioning from mode 0 to mode A (see table 1) P3 goes from on to off at the same time N3 goes from off to on. If P3 turns off slowly and N3 turns on quickly, cross conduction may occur. This condition has been prevented inside the IC on the ML4420 through the addition of comparator A6 on the P3 output (Fig. 7).

2. When the MOSFET in the same phase switches on gate current flows due to capacative coupling of current through the MOSFET's drain to gate capacitance. This could cause the MOSFET that was off to be turned on.

3. In condition 2 above, the P-channel MOSFET is pulled up inside the ML4420 by a NPN follower with base pulled up to VCC2 via 16KΩ. If the current through Cdgp is greater than the Vth_{PMOS}/16KΩ/Beta NPN, when the N-FET turns ON, the P-FET could be turned ON simultaneously, causing cross-conduction. The same mechanism can be applied to N-FET when P-FET is turned ON. The ML4420 is designed to take care of both the cases through slow turn-on, fast turn-off schemes ie P-FET Gate is pulled down by an 800µA current source and the N-FET Gate is charged up by an emitter follower in series with 4KΩ.

Figure 10 shows the output stages and the potential causes of cross-conduction. The diode D1 shown, may be needed for high power applications to limit the negative current pulled (through Cdgn) out of the substrate diode in the ML4420 when P-FET turns off.

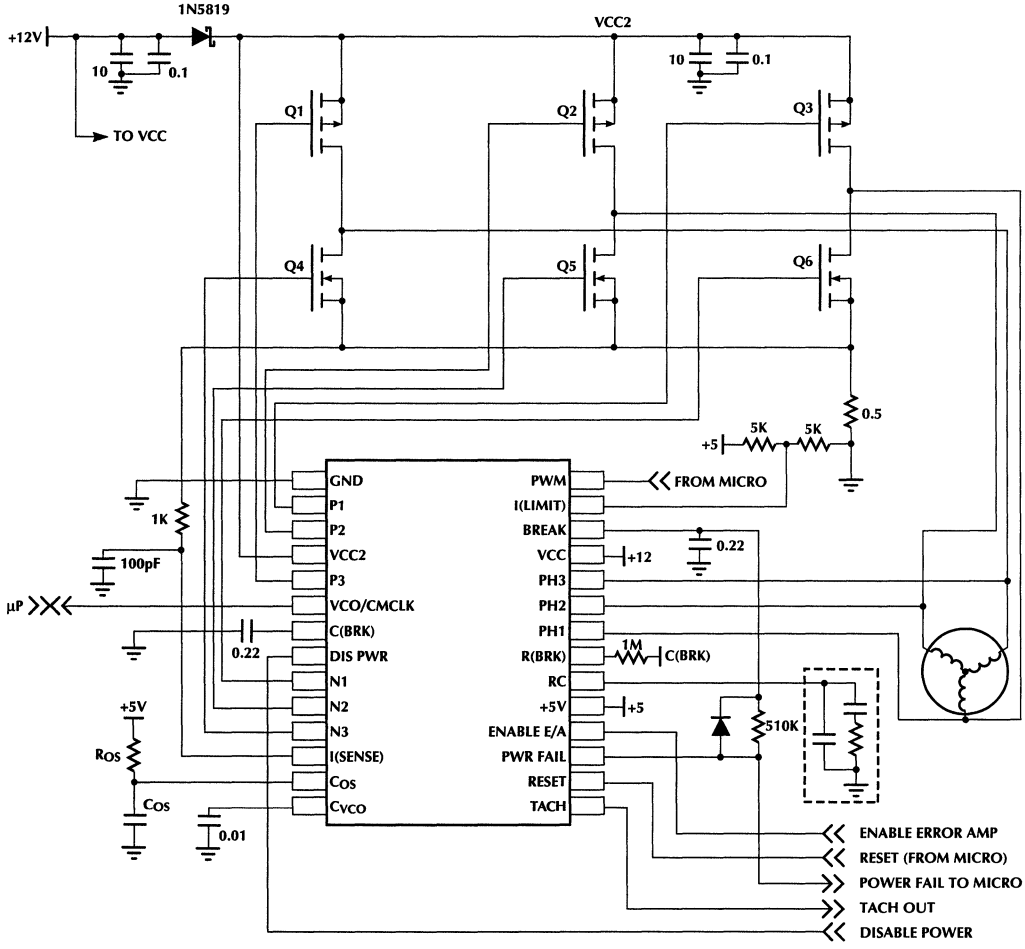


Figure 8. ML4420 Typical Application

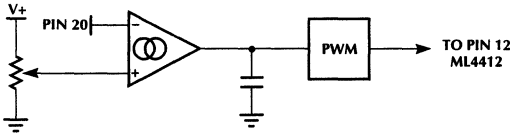


Figure 9. Voltage Controller PWM Generator

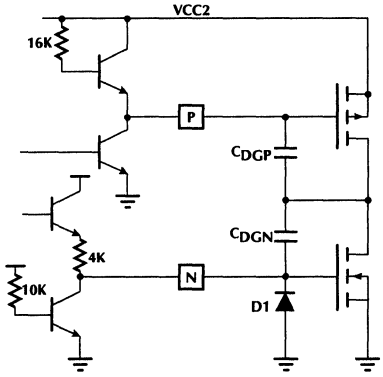


Figure 10. Causes of Cross-conduction

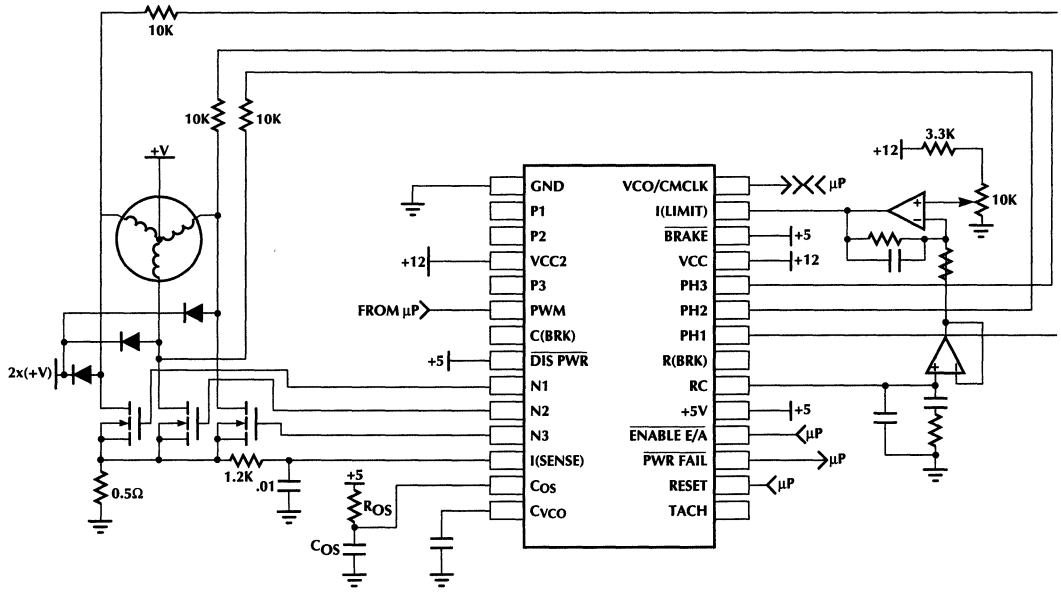


Figure 11. ML4420 Unipolar Drive Application

UNIPOLAR OPERATION

Unipolar mode offers the potential advantage of lower motor drive cost by only requiring the use of 3 transistors to drive the motor. The ML4420 will operate in unipolar mode (Figure 11) provided the following precautions are taken:

1. The IC supplies should not exceed 12V + 10%.
2. The phase pins on the IC should not exceed the supply voltage.

In unipolar operation, the motor's windings must be allowed to drive freely to:

$$V_{\Phi(MAX)} = V_{SUPPLY\ (MAX)} + V_{EMF\ (MAX)}$$

Therefore, there can be no diodes to clamp the inductive energy to V_{SUPPLY}. This energy must be clamped, however, to avoid an over-voltage condition on the MOSFETs and other components. Typically, a V(CLAMP) voltage is created to provide the clamping voltage. The inductive energy may either be dissipated (Figure 12) or alternately efficiently regenerated back to the system supply (Figure 13).

The circuit in Figure 11 is designed to minimize the external components necessary, at some compromise to performance. The 3 resistors from the motor phase windings to the PH inputs work with the ML4420's 5KΩ internal resistance to ground to divide the motor's phase voltage down, providing input signals that do not exceed 12V. This circuit uses analog speed regulation. The "one shot" circuitry to time the reset is replaced by a diode and RC delay from the rising edge or the $\overline{\text{POWERFAIL}}$ signal. The error amplifier is left enabled continuously since at low speeds its current contribution is negligible. The current injected into the loop filter must be greater than the leakage current from the phase detector amplifier for the motor to start reliably.

HIGHER VOLTAGE MOTOR DRIVE

To drive a higher voltage motor, the same precautions regarding ML4420 voltage limitations as were outlined for Unipolar drive above should be followed. Figures 14–16 provide several methods of translating the ML4420's P outputs to drive a higher voltage.

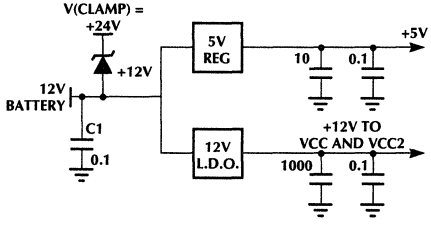


Figure 12. Dissipative Clamping Technique

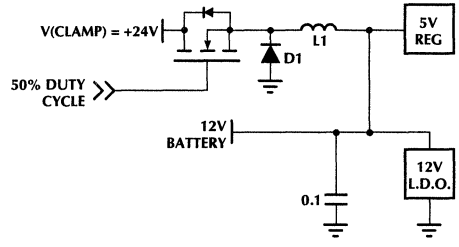


Figure 13. Non-Dissipative Clamping Technique

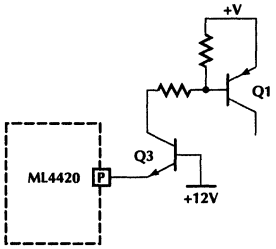


Figure 14. High Voltage Translation using PNP Power Transistor

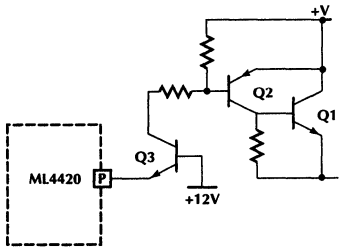


Figure 15. High Voltage Translation using "Composite" PNP Power Transistor

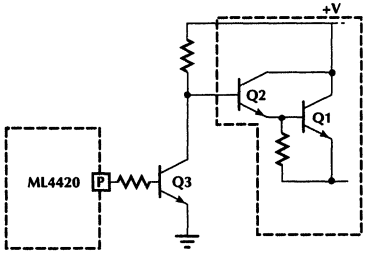


Figure 16. High Voltage Translation with NPN Darlingtion

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4420CS	0°C to +70°C	28-PIN SOIC (S28W)

ML4425/ML4426

Sensorless BLDC PWM Motor Controller

GENERAL DESCRIPTION

The ML4425/ML4426 PWM motor controllers provide all of the functions necessary for starting and controlling the speed of delta or wye wound Brushless DC Motors (BLDC) without Hall Effect Sensors.

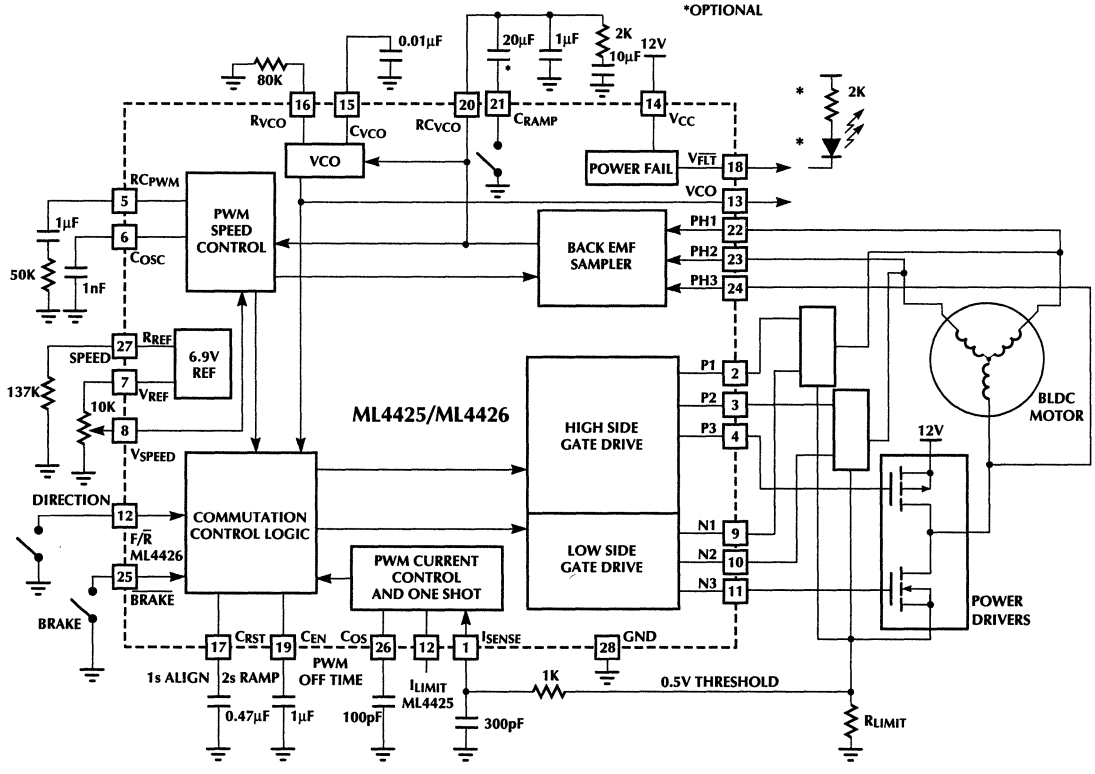
Back EMF voltage is sensed from the motor windings to determine the proper commutation phase sequence using PLL techniques. The patented Back-EMF sensing technique used will commutate virtually any 3-Phase BLDC motor and is insensitive to PWM noise and motor snubbing circuitry.

The ML4425/ML4426 limits the motor current with a constant off-time PWM controlled current. The velocity loop is controlled with an on-board amplifier. An accurate, jitter-free, VCO output is provided equal to the commutation frequency of the motor. The ML4425/ML4426 switches the gates of external N-channel power MOSFETs to regulate the motor current and directly drives

FEATURES

- Stand-alone operation
- Forward and reverse operation: ML4426
- Current limit input: ML4425
- Motor starts and stops with power to IC
- On-board start sequence: Align → Ramp → Set Speed
- Patented Back-EMF commutation technique provides jitterless torque for minimum "spin-up" time
- Simple variable speed control
- On-board voltage reference: 6.9V
- Single External Resistor Sets all Critical Currents
- On-board speed control loop

BLOCK DIAGRAM/TYPICAL APPLICATION



GENERAL DESCRIPTION (Continued)

the P-channel MOSFETs for 12V motors. Higher voltage motors are driven using buffer transistors or standard "High side" drivers.

The ML4425/ML4426 has a blanker circuit to prevent false retriggering of the one shot during a motor current spike and circuitry to ensure that there is no shoot through in any state of the power drive FETs.

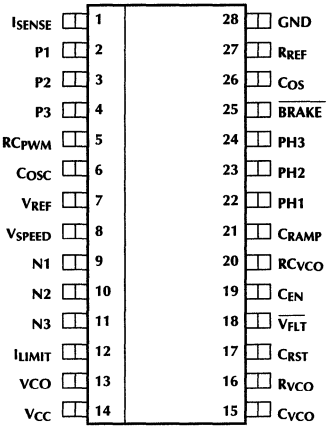
The timing of the start-up sequence is determined with one current setting resistor and two timing capacitors thus allowing for simple optimization for a wide range of motors and loads.

FEATURES (Continued)

- PLL used for commutation provides noise immunity from PWM spikes, compared to noise sensitive zero crossing technique
- PWM control for maximum efficiency
- Under-voltage fault output
- 12 volt operation
- Direct FET drive for 12V motors
- Drives high voltage motors with IC buffers from IR, IXYS, Harris, Power Integration, Holt, Siliconix, etc.
- Industrial temperature range –40°C to +85°C is available
- Available in 28-pin DIP and SOIC packages

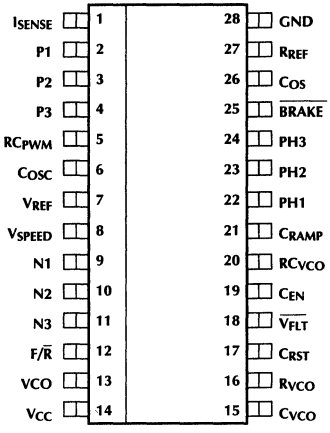
PIN CONFIGURATION

ML4425
28-Pin SOIC (S28W)
28-Pin Molded Narrow DIP (P28N)



TOP VIEW

ML4426
28-Pin SOIC (S28W)
28-Pin Molded Narrow DIP (P28N)



TOP VIEW

5

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	I_{SENSE}	Motor current sense input. I_{LIMIT} occurs when this pin is approximately 0.5V.
2	P1	Drives the external P-channel transistor driving motor PH1.
3	P2	Drives the external P-channel transistor driving motor PH2.
4	P3	Drives the external P-channel transistor driving motor PH3.
5	RC_{PWM}	The resistor/capacitor combination on this gm amplifier sets the pole-zero of the speed loop in conjunction with a gm of 0.385mmho.
6	C_{OSC}	This capacitor sets the PWM oscillator frequency. A 1nF capacitor will set the frequency to approximately 25KHz.
7	V_{REF}	This voltage reference output can be used to set the speed reference voltage.
8	V_{SPEED}	This input to the amplifier in the speed loop controls the speed target of the motor.
9-11	N1, N2, N3	Drives the external N-channel MOSFETs for PH1, PH2, PH3.
12	$F/\overline{R}$	For the ML4426, the forward/reverse pin controls the sequence of the commutation states and thus the direction of motor rotation.
12	I_{LIMIT}	For the ML4425, this pin is internally set to 2.5V which sets the I_{SENSE} threshold to 0.5V. This voltage can be lowered externally to reduce the I_{SENSE} threshold.
13	VCO	This logic output indicates the commutation frequency of the motor.
14	V_{CC}	12V power supply.
15	C_{VCO}	Timing capacitor for VCO
16	R_{VCO}	The resistor on this pin sets a process independent current to generate a repeatable VCO frequency.
17	C_{RST}	A 0.75µA current from this pin will charge a capacitor to 1.5V. This is the time the device will remain in reset mode. Connecting this pin to ground forces the chip to the reset state.
18	V_{FT}	A logic "0" indicates the power supply is under-voltage. A logic "1" is > 3.5V.
19	$\overline{C_{EN}}$	After C_{RST} has timed out a 0.75µA current from this pin will charge a capacitor to 1.5V. This is the time the device will remain in the ramp mode.
20	RC_{VCO}	VCO loop filter components. A 0.5µA current from this pin will ramp the VCO after C_{RST} has timed out.
21	C_{RAMP}	This capacitor can be used if necessary to reduce the ramp speed to enhance start-up in high RPM applications. It is logic low until C_{EN} times out.
22	PH1	Motor Terminal 1
23	PH2	Motor Terminal 2
24	PH3	Motor Terminal 3
25	$\overline{BRAKE}$	A "0" activates the braking circuit
26	C_{OS}	A 30µA current from this pin will charge a timing capacitor to GND for fixed off-time PWM current control
27	R_{REF}	This resistor sets constant currents on the device to reduce process dependence and external components. The 137K resistor sets the previously mentioned current levels.
28	GND	Signal and Power Ground

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (pin 14) 14V
Output Current (pins 2, 3, 4, 9,10,11) ..... ±50mA
Logic Inputs (pins 17, 19, 25) ..... –0.3 to 7V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 150°C
Thermal Resistance (θ_{JA}) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range
ML4425CS/ML4426CS/
ML4425CP/ML4426CP ..... 0°C to 70°C
ML4425IS/ML4426IS/
ML4425IP/ML4426IP ..... –40°C to 85°C
VCC Voltage +12V (pin 14) ..... 12V ± 10%

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, V_{CC} = 12V, R_{SENSE} = 1Ω, C_{VCO} = 0.01µF, C_{OS} = 100pF, R_{REF} = 137kΩ

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator (VCO) Section (V_{PIN16} = 5V)					
Frequency vs. $V_{PIN\ 20}$	$1V \le V_{PIN20} \le 7V$		300		Hz/V
Frequency	V_{VCO} = 6V	1450	1800	2150	Hz
Sampling Amplifier (Note 1)					
V_{RC}	State R		125	250	mV
I_{RC}	Ramp		0.5		µA
	V_{PIN19} = 5V, State A, V_{PH2} = 4V	30	50	70	µA
	V_{PIN19} = 5V, State A, V_{PH2} = 6V	–13	2	13	µA
	V_{PIN19} = 5V, State A, V_{PH2} = 8V	–30	–50	–70	µA
Motor Current Control Section					
I(SENSE) Gain	$V_{PIN12} \le 2.5V$	4.5	5	5.5	V/V
One Shot Off Time		8	12	16	µs
Power Fail Detection Circuit					
12V Threshold		9.1	9.8	10.5	V
Hysteresis			150		mV
Logic Inputs					
Voltage High (V_{IH})		2			V
Voltage Low (V_{IL})				0.8	V
Current High (I_{IH})	V_{IN} = 2.7V	–300	1	300	µA
Current Low (I_{IL})	V_{IN} = 0.4V	–150		150	µA
Braking Circuit					
Pin 25 Bias Current	V_{PIN25} = 0V	–10	0.3	10	µA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Outputs (I_{CMD} = I_{LIMIT} = 2.5V)						
I_P Low	ML4425	V_P = 2V	0.5		1.2	mA
	ML4426	V_P = 2V	4.0		7.0	mA
V_P High		I_P = –10µA	V_{CC} – 1			V
P3 Comparator Threshold			V_{CC} – 3.6		V_{CC} – 2.4	V
V_N High		V_{PIN12} = 0V	V_{CC} – 3.2	10	V_{CC} – 1.2	V
V_N Low		I_N = 1mA		0.2	0.7	V
LOGIC Low (V_{OL})		I_{OUT} = 0.4mA			0.5	V
VCO/V_{OH}		I_{OUT} = –100µA	2.4			V
POWER FAIL V_{OH}		I_{OUT} = –10µA	3.5		6.5	V
Speed Control						
FPWM (Pin 6)		C_{OSC} = 1nF		28		kHz
gm Current (Pin 5)			±10		±15	µA
V_{REF}				6.9		V
Start-Up						
I_{CRST}				0.75		µA
V_{TH} C_{RST}				1.5		V
I_{CEN}				0.75		µA
V_{TH} C_{EN}				1.5		V
Supply Current						
VCC Current				32	50	mA

Note 1. For explanation of states, see Figure 5 and Table 1.

FUNCTIONAL DESCRIPTION

The ML4425/ML4426 provides closed-loop commutation for 3-phase brushless motors. To accomplish this task, a VCO, integrating Back-EMF Sampling error amplifier and sequencer form a phase-locked loop, locking the VCO to the back-EMF of the motor. The IC also contains circuitry to control motor speed in PWM mode. Braking and power fail detection functions are also provided on chip. The ML4425/ML4426 is designed to drive external power transistors (N-channel sinking transistors and P-channel sourcing transistors) directly.

Start-up timing sequence is accomplished by means of 2 timing capacitors charged by currents sources on the device. C_{RST} determines the time the motor stays in align mode and C_{EN} determines the time the motor will ramp before the speed set loop closes. Once the speed loop closes the N-channels are in a PWM mode to control the motor current. The voltage set on V_{SPEED} will force the same voltage on RC_{VCO} to control speed.

Speed sensing is accomplished by monitoring the output of the VCO, which will be a signal which is phased-locked to the commutation frequency of the motor.

BACK-EMF SENSING AND COMMUTATOR

The ML4425/ML4426 contains a patented back-EMF sensing circuit which samples the phase which is not energized (Shaded area in figure 2) to determine whether to increase or decrease the commutator (VCO) frequency. A late commutation causes the error amplifier to charge the filter (RC) on pin 20, increasing the VCO input while early commutation causes pin 20 discharge. The analog speed control loop uses pin 20 as a speed feedback voltage.

The input impedance of the three PH inputs is about 8kΩ to GND. When operating with a higher voltage motor, the PH inputs should be divided down in voltage so that the maximum voltage at any PH input does not exceed V_{CC}.

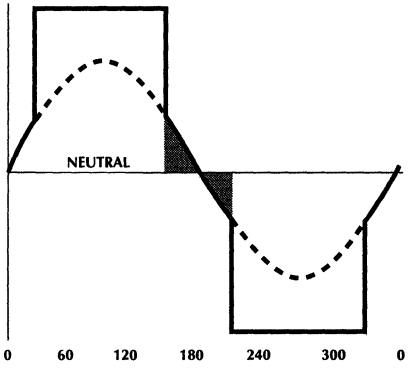


Figure 2. Typical Motor Phase Waveform with Back-EMF Superimposed (Ideal Commutation).

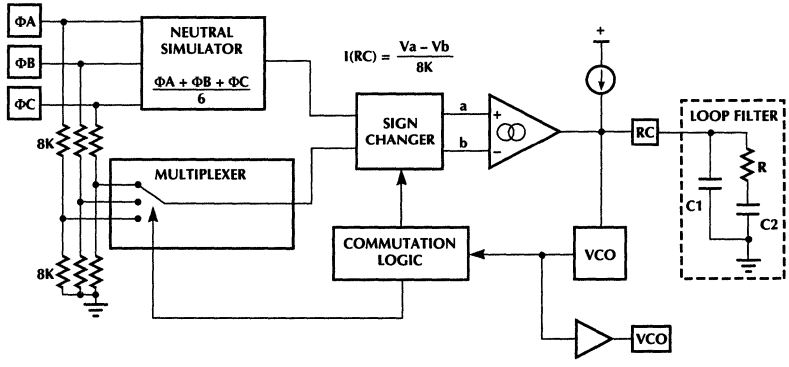


Figure 1. Back EMF Sensing Block Diagram

COMPONENT SELECTION GUIDE

In order to properly select the critical components for the ML4425/ML4426 you should know the following things:

1. The motor operating voltage.
2. The maximum operating current for the motor.
3. The number of poles the motor has.
4. The back EMF constant of the motor.
5. The torque constant of the motor. (This is the same as the back EMF constant, only in different units.)
6. The desired speed of operation.
7. The moment of inertia of the motor and its load.
8. The coefficient of viscous friction.

If you do not know one or more of the above values, it is still possible to pick components for the ML4425/ML4426, but some experimentation may be necessary to determine the optimal value. All quantities are in SI units unless other wise specified. The formulas in the following section are based on linear system models. Since Coulomb friction is not a linear phenomenon, large amounts of friction in a system may require values different from those given below. The following formulas should be considered a starting point from which you can optimize your application.

R_{SENSE}

The function of R_{SENSE} is to provide a voltage proportional to the motor current, for current limit/feedback purposes. The trip voltage across R_{SENSE} is 0.5V so:

$$R_{SENSE} = \frac{0.5}{I_{MAX}}$$

I_{MAX} is the maximum motor current.

The power dissipation is obviously I_{MAX} squared times R_{SENSE}, so the resistor should be sized appropriately. For very high current motors, a smaller resistor can be used, with an op-amp to increase the gain, so that power dissipation in the sense resistor is minimized.

In the ML4425, the trip voltage across R_{SENSE} can be modified with a voltage applied to the I_{LIMIT} pin, pin 12. There is a gain of 5 in the I_{SENSE} path so that 2.5V on pin 12 corresponds to a 0.5V trip voltage across R_{SENSE}. Z_{IN} on the I_{LIMIT} pin is $\approx 6K\Omega$.

I_{SENSE} FILTER

The I_{SENSE} filter consists of an RC lowpass filter in series with the current sense signal. The purpose of this filter is to filter out noise spikes on the current, which may cause false triggering of the one shot circuit. It is important that this filter not slow down the current feedback loop, or destruction of the output stage may result. The recommended values for this circuit are $R = 1K\Omega$ and C= 300pF. This gives a time constant of 300ns, and will filter out spikes of shorter duration. These values should suffice for most applications. If excessive noise is present on the I_{SENSE} pin, the capacitor may be increased at the expense of speed of current loop response. The filter time constant should not exceed 500ns or it will have a significant impact on the response speed of the one shot current limit.

C_{OS}

The one shot capacitor determines the off time after the current limit is activated, i.e. the voltage on the I_{SENSE} pin exceeded 0.5V. The following formula ensures that the motor current is stable in current limit:

$$C_{OS} = \frac{1.11\times10^{-6}\times V_{MOTOR} - 5\times10^{-6}}{947.4}$$

C_{OS} is in Farads

This is the maximum value that C_{OS} should be. Higher average torque during the current limit cycle can be achieved by reducing this value experimentally, while monitoring the motor current carefully, to be sure that a runaway condition does not occur. This runaway condition occurs when the current gained during the on time exceeds the current lost during the off time, causing the motor current to increase until damage occurs. For most motors this will not occur, as it is usually a self limiting phenomenon.

C_{VCO}

As given in the section on the VCO and phase detector:

$$C_{VCO} = \frac{315\times10^{-6}}{N\times RPM}$$

Where N is the number of poles in the motor, and RPM is the motor's maximum operating speed in revolutions per minute.

RESET CAPACITOR

The function of the reset capacitor is to provide a time delay, during which the ML4425/ML4426 will align the rotor to a known position. During this time period the ML4425/ML4426 turns on two of the upper and one of the lower output drivers. This results in a fixed current in the windings, a stationary magnetic field, and a locked rotor. If the position is not at a torque null during the reset period, it will require some time to move to the locked position, and settle. This time period is dependent on the motor, the load, the friction and eddy current losses, and current limit setting. A good starting point for a value for the reset capacitor is:

$$C = \frac{1.5\times10^{-6}}{\delta\times\sqrt{\frac{N\times K\times\tau\times I_{MAX}}{\pi\times J}}}$$

The δ factor is known as the damping factor, and can range from 0.1 in a motor with very little damping to 0.9 in a heavily damped motor. $K\tau$ is the torque constant in N x M/Amp, Imax is the motor current in current limit, and J is the moment of inertia of the motor and the load. If you don't know the damping factor, try a value of 0.3 initially. If you don't know the moment of inertia, start

with a 1µF capacitor. In any case, if the motor has come to a full stop well before the ramp up period, you can decrease this value. If the motor does not stop before ramp up, you must increase this value until it does. Motors with very little friction or damping and a large inertial load tend to require larger values of capacitance here.

ENABLE CAPACITOR

This capacitor provides a time delay after the reset period for the motor to ramp up to speed. The following equation gives an approximate starting value for this capacitor. If starting is not reliable, this capacitor may be increased until it is. If starting is reliable and minimum spin up time is important, this value can be decreased experimentally to find the minimum practical value. Motors with a large amount of friction or a large inertia will tend to need larger capacitors.

$$C_{EN} = \frac{55.85 \times N \times (C1 + C2)}{Kv}$$

Where N is the number of poles in the motor, C 1 and C2 are the VCO loop filter components on pin 20, and Kv is the VCO Pain (See the section on the VCO and phase detector.)

RAMP CAPACITOR

The ML4425/ML4426 outputs a fixed 0.5µA current on pin 20 during ramp up. This is the input to the VCO. Therefore, the rotor's acceleration is a function of the current, VCO gain and the loop filter components only. In some cases, where the VCO capacitor is small due to a high running speed, and the motor inertia is large, the rotor may not be able to follow the VCO during ramp up. In these cases, it is necessary to add a capacitor from pin 21 to ground. This capacitor is switched in during ramp only, and allows the rate of acceleration during ramp up to be lowered. An approximate starting point for this capacitor is given by the equation below:

$$C_{RAMP} = \frac{J \times 0.5 \times 10^{-6}}{I_{MAX} \times Kt} \times \frac{Kv \times 2 \times \pi}{3 \times N} - (C1 + C2)$$

Where J is the inertia of the motor plus load, Kv is the VCO gain, N is the number of poles, Imax is the maximum motor current, Kt is the torque constant, and C1 and C2 are the loop filter components on pin 20. Normally, the result of the preceding equation will be a negative number, meaning that no ramp capacitor is necessary. If the result of this equation is greater than zero, then the ramp capacitor should be included.

C_{OSC}

This capacitor sets the PWM ramp oscillator frequency. This is the PWM "switching frequency". If this value is too low, <20kHz, then magnetostriction effects in the motor may cause audible noise. If this frequency is too high, >30kHz, then the switching losses in the output drivers may become a problem. 25kHz should be a good compromise for this value, which can be obtained by using a 1nF capacitor.

R_{VCO} AND R_{REF}

R_{VCO} should be 80K and R_{REF} should be 137K for normal operation.

RC_{PWM}

This pin is the output of a transconductance amplifier. A resistor and a capacitor in series with this pin and connected to ground form the speed loop compensation. The motor will have a mechanical time constant, given approximately by:

$$\tau_m = \frac{J \times Rw}{Ke^2}$$

Where J is the moment of inertia of the rotor plus the load, Rw is the winding resistance, and Ke is the back-E.M.F. constant This pole occurs at a relatively low frequency, and will limit the frequency of response of the servo loop. In order to get better response, the RC combination on the RC_{PWM} pin can be used to provide phase lead for the speed loop. This combination also sets the open loop gain characteristics, and therefore the accuracy of the speed loop. In order to pick components for this loop, it is necessary to decide on a desired closed loop bandwidth. The chosen closed loop bandwidth should be substantially lower than the bandwidth of the phase locked loop used for commutation, in order to preserve acceptable phase margin. This is usually not a problem, as the mechanical time constant of the motor is necessarily much lower than the commutation loop response. Depending on the motor and its load, a bandwidth in the 1-10Hz range is easily achievable. The frequency of the compensating zero should be set to be a decade below the unity gain crossover frequency, so that its contribution to the phase lead will be maximum at the crossover. The following formula gives the value of C necessary for these conditions:

$$CC = 482.314 \times N \times \frac{V_{CC} \times C_{VCO}}{\left[\text{freq.}\left[Ke\left(\sqrt{2.5 + 98.696 \times \tau_m{}^2 \times \text{freq.}^2}\right)\right]\right]}$$

Where freq. is the desired unity gain crossover frequency, V_{CC} is the supply voltage, C_{VCO} is the VCO capacitor on pin 15, N is the number of poles in the motor, and the other quantities are defined above. Then, the value of R should be

$$R = \frac{10}{2 \times \pi \times CC \times \text{freq.}}$$

If the speed loop is unstable, it is possible that the desired bandwidth is too high, and reducing the value of freq. should solve the problem.

VCO FILTER

See the section on the VCO and Phase detector for information on these components.

VCO AND PHASE DETECTOR CALCULATIONS

The VCO should be set so that at the maximum frequency of operation (the running speed of the motor) the VCO control voltage will be no higher than V_{REF}, or 6.9V. The VCO maximum frequency will be:

$$F_{MAX} = 0.05 \times POLES \times RPM$$

where POLES is the number of poles on the motor and RPM is the maximum motor speed in Revolutions Per Minute.

The minimum VCO gain derived from the specification table (using the minimum F_{VCO} at V_{VCO} = 6V) is:

$$K_{VCO(MIN)} = \frac{2.42 \times 10^{-6}}{C_{VCO}}$$

Assuming that the $V_{VCO(MAX)}$ = 6.5V, then

$$C_{VCO} = \frac{6.5 \times 2.42 \times 10^{-6}}{F_{MAX}}$$

or

$$C_{VCO} = \frac{315}{POLES \times RPM} \mu F$$

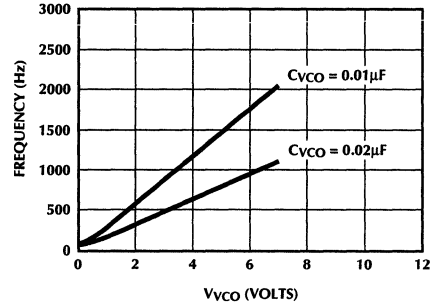


Figure 3. VCO Output Frequency vs. V_{VCO} (Pin 20)

Figure 4 shows the linearized transfer function of the Phase Locked Loop with the phase detector formed from the sampled phase through the Gm amplifier with the loop filtered formed by R, C_1, and C_2. The Phase detector gain is:

$$\frac{Ke \times \omega \times Atten}{2\pi} \times 1.25 \times 10^{-14} A/Radian$$

Where Ke is the motor back-E.M.F. constant in V/Radian/sec, ω is the rotor speed in r/s, and Atten is the back-E.M.F. resistive attenuator, nominally 0.5.

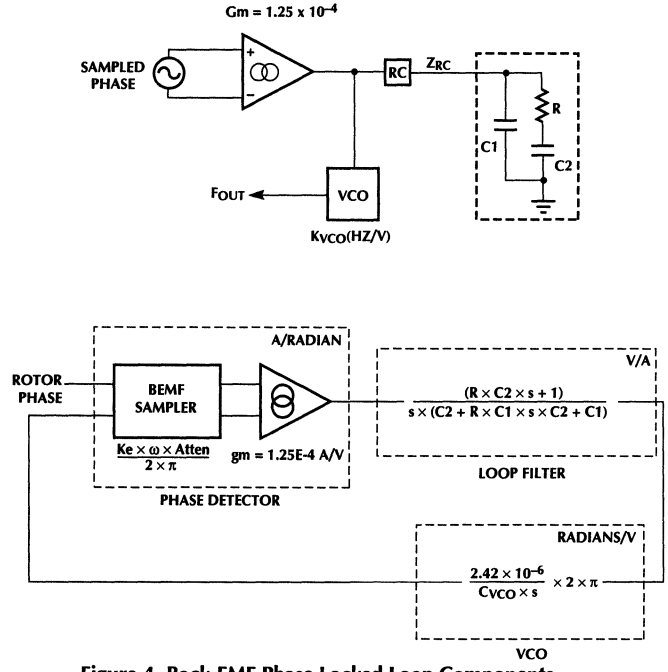


Figure 4. Back-EMF Phase Locked Loop Components.

The simplified impedance of the loop filter is

$$Z_{RC}(s) = \frac{1}{C_1 s} \frac{(s + \omega_{LEAD})}{(s + \omega_{LAG})}$$

Where the lead and lag frequencies are set by:

$$\omega_{LEAD} = \frac{1}{RC_2}$$

$$\omega_{LAG} = \frac{C_1 + C_2}{RC_1C_2}$$

Requiring the loop to settle in 20 PLL cycles with $\omega_{LAG} = 10 \times \omega_{LEAD}$ produces the following calculations for R, C_1 and C_2:

$$C_1 \approx \frac{4.07 \times 10^{-11} \times K_e \times RPM}{C_{VCO} \times F_{VCO}^2}$$

$$C_2 = 9 \times C_1$$

$$R = \frac{9.02}{C_2 \times F_{VCO}}$$

where K_e is the back-EMF constant in volts per radian per second, and RPM is the rotor speed. See Micro Linear application note 35 for derivation of the above formulas.

START-UP SEQUENCING

When the motor is initially at rest, it is generating no back-EMF. Because a back-EMF signal is required for closed loop commutation, the motor must be started "open-loop" until a velocity sufficient to generate some back-EMF is attained (around 100 RPM). The following steps are a typical procedure for starting a motor which is at rest.

Align: The IC is held in reset (state R) with full power applied to the windings (see figure 6). This aligns the rotor to a position which is 30° (electrical) before the center of the first commutation state. This time is

$$t = \frac{(1.5V)\, C_{RST}}{0.75\mu A}$$

Ramp: Align is released, and a fixed 0.5µA current is input to pin 20, and will ramp the VCO input voltage, accelerating the motor at a fixed rate. This time is

$$t = \frac{(1.5V)\, C_{EN}}{0.75\mu A}$$

Run: When the motor speed reaches about 100 RPM, the back-EMF loop can be used in closed loop speed control and the voltage on the RC_{VCO} pin will ramp to the same voltage applied to V_{SPEED}. This allows speed selection referring to figure 3.

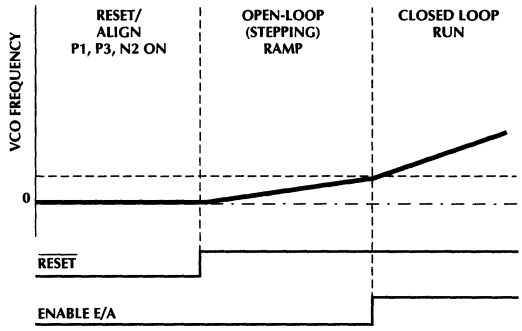


Figure 6. Typical Start-up Sequence.

Using this technique, some reverse rotation is possible. The maximum amount of reverse rotation is 360/N, where N is the number of poles. For an 8 pole motor, 45° reverse rotation is possible.

MODE	PIN 17	PIN 19	I_{LIMIT}
Align	0	0	I_{MAX}
Ramp	1	0	I_{MAX}
Run	1	1	I_{MAX}

Table 2. Start-up Sequence.

ALIGN: The IC is held in reset (state R).

RAMP: After the reset pin has reached 1.5V the C_{EN} pin begins to charge. During this time the RC_{VCO} components are charged with 0.5µA and the VCO begins to ramp up in frequency. This continues until the C_{EN} pin reaches 1.5V and times out. The motor must be able to keep up with the VCO ramp rate.

RUN: After C_{EN} has timed out the device begins closed loop operation using the BEMF of the motor.

DIRECTION: The direction of motor rotation is controlled by the commutation states as given in Table 1. The state sequence is controlled by the F/$\overline{R}$ (pin 12).

5

STATE	DIRECTION	OUTPUTS						INPUT SAMPLES	
	REVERSE	N3	N2	N1	P3	P2	P1		
	FORWARD	N1	N2	N3	P1	P2	P3	FORWARD	REVERSE
R OR 0		OFF	ON	OFF	ON	OFF	ON	N/A	N/A
A		OFF	OFF	ON	ON	OFF	OFF	PH2	PH2
B		OFF	OFF	ON	OFF	ON	OFF	PH1	PH3
C		ON	OFF	OFF	OFF	ON	OFF	PH3	PH1
D		ON	OFF	OFF	OFF	OFF	ON	PH2	PH2
E		OFF	ON	OFF	OFF	OFF	ON	PH1	PH3
F		OFF	ON	OFF	ON	OFF	OFF	PH3	PH1

Table 1. Commutation States.

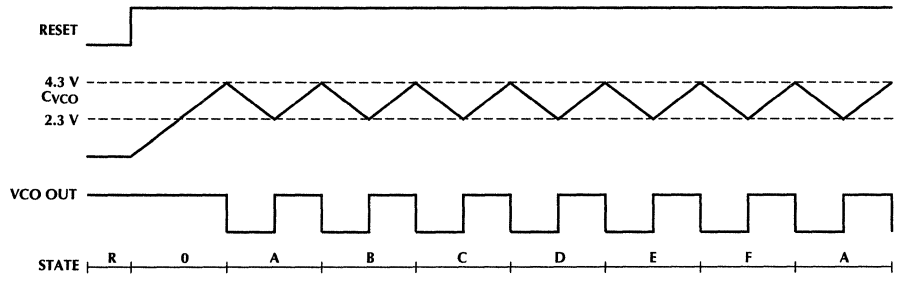


Figure 5. Commutation Timing and Sequencing.

ADJUSTING OPEN LOOP STEP RATE (RAMP)

Align

Motor alignment occurs when power is first applied and C_{RST} (pin 17) and C_{EN} (pin 19) are low. The device will stay in the align mode until the 0.75µA current out of C_{RST} charges the external capacitor to 1.5V at which time ramp mode is enabled.

During align P-channels P1 and P3 will be driven on and N-channel N2 will be on to provide high torque to position rotor on pole.

Motor loads with larger inertia will require longer alignment periods or larger values of C_{RST} for possibly higher currents (I_{LIMIT}).

Maximum current limit can be set by the R_{LIMIT} from the I_{SENSE} pin (1). The threshold on this pin is approximately 0.5V thus

$$I_{LIMIT} = \frac{0.5V}{R_{LIMIT}}$$

I_{LIMIT} is also under PWM control with t_{OFF} set by a capacitor connected to C_{OS} (pin 26) and given by

$$t_{OFF} = C_{OS}\frac{2.5V}{25\mu A}$$

Ramp

Motor ramping begins when C_{RST} has exceeded 1.5V at which time the capacitor connected to C_{EN} (pin 19) which had been held at ground will begin to charge with 0.75µA from the pin. When C_{EN} reaches 1.5V the device will enter run mode.

During ramp mode a 0.5µA current from the RC_{VCO} pin (20) will charge the filter components and begin to ramp the VCO frequency and begin commutating states A through F of the motor in an open loop fashion. C_{RAMP} is shorted to ground during ramp allowing additional flexibility in starting high speed motors.

C_{RAMP} should be set so that the VCO's frequency ramp during "open loop stepping" phase of motor starting is less than the motor's acceleration rate. In other words, the motor must be able to keep up with the VCO's ramp rate in open loop stepping mode. The VCO's input voltage ($V_{PIN\ 20}$) ramp rate is given by:

$$\frac{dV_{VCO}}{dt} \approx \frac{0.5\mu A}{C_1 + C_2 + C_{RAMP}}$$

since

$$F_{VCO} = K_{VCO} \times V_{VCO}$$

$$K_{VCO(MAX)} = \frac{4\times10^{-6}}{C_{VCO}}$$

then combining the 3 equations C_{RAMP} can be calculated from the desired maximum open loop stepping rate the motor can follow.

$$0.5\mu A < \frac{dF_{VCO}}{dt}\frac{C_{VCO}\times(C_1 + C_2 + C_{RAMP})}{4\times10^{-6}}$$

The motor will start more consistently and tolerate a wider variation in open loop step rate if there is some damping on the motor during the open loop modes.

The tolerance of the open loop step VCO acceleration $\left(\frac{dF_{VCO}}{dt}\right)$ depends on the tolerances of K_{VCO}, C_{RAMP}, C_1, C_2, and C_{VCO}.

Larger motors and loads will require longer ramp periods or larger values of C_{EN}.

Run

When the C_{EN} pin exceeds 1.5V the device will enter run mode. At this time the motor speed should be high enough to generate a detectable BEMF and allow closed loop operation to begin. The commutation position compensation has been previously discussed.

The motor will continue to accelerate as long as the voltage on the RC_{VCO} pin (20) is less than the voltage on V_{SPEED} (pin 8). During this time the motor will receive full N-channel drive limited only by I_{LIMIT}. As the voltage on pin 20 approaches that of pin 8 the C_{PWM} capacitor will charge and begin to control the gate drive to the N-channel transistor by setting a level for comparison on the 25kHz PWM saw tooth waveform generated on C_{OSC} (pin 6). The compensation of the speed loop is accomplished on C_{PWM} (pin 5) which is the output of a transconductance amplifier with a gm = 3.85 x 10–4℧.

OUTPUT DRIVERS

The P-channel drivers are emitter follower type with 5mA pull down currents. This allows for fast turn off to prevent cross conduction. The N-channel drivers are totem pole with a 750Ω resistor in series with the pull up device again reducing cross conduction.

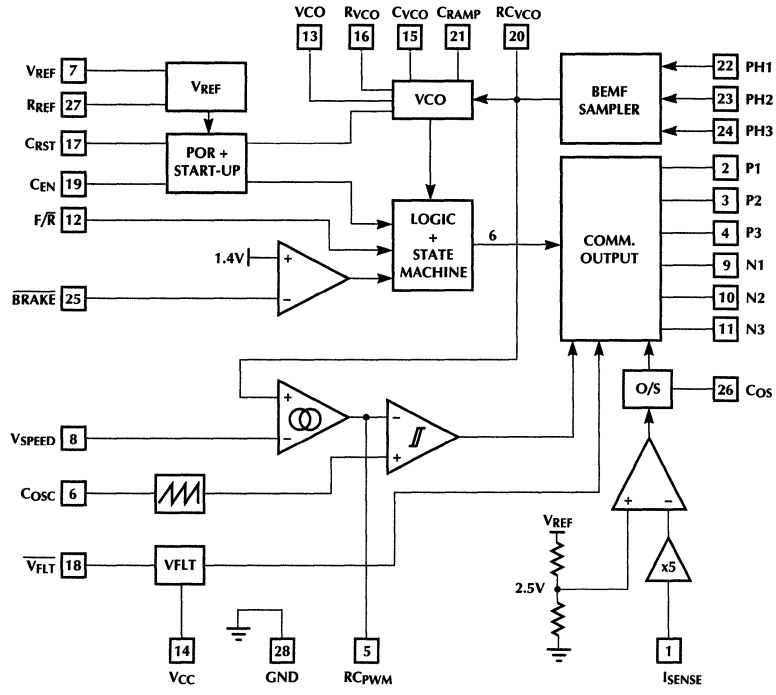


Figure 8. Block Diagram.

BRAKING

When $\overline{\text{BRAKE}}$ pin (25) is pulled low all 3 P-channel drivers will be turned off and all 3 N-channel drivers will be turned on.

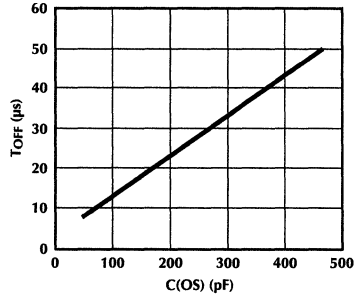


Figure 7. I_{LIMIT} Output Off-Time vs. C_{OS}.

HIGHER VOLTAGE MOTOR DRIVE

The ML4425/ML4426 can be used to drive higher voltage motors by means of level shifters to the high side drive transistors. This can be accomplished by using dedicated high side drivers for applications greater than 60V or a simple NPN level shift as shown in figure 9 for applications below 60V. Figure 10 shows how to interface to the IR2110, a 3-phase bridge driver from I.R. This allows driving motors up to 600V.

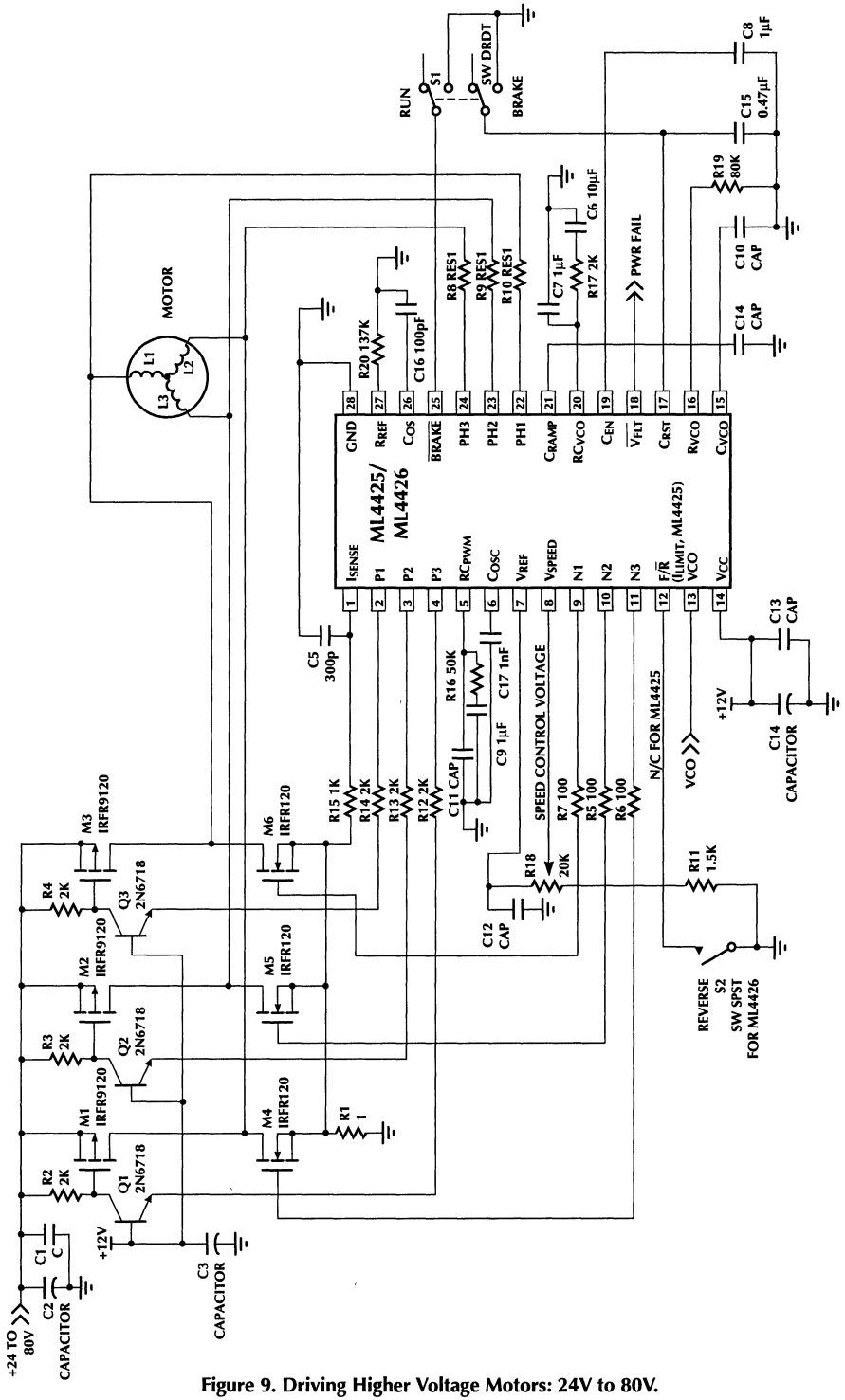


Figure 9. Driving Higher Voltage Motors: 24V to 80V.

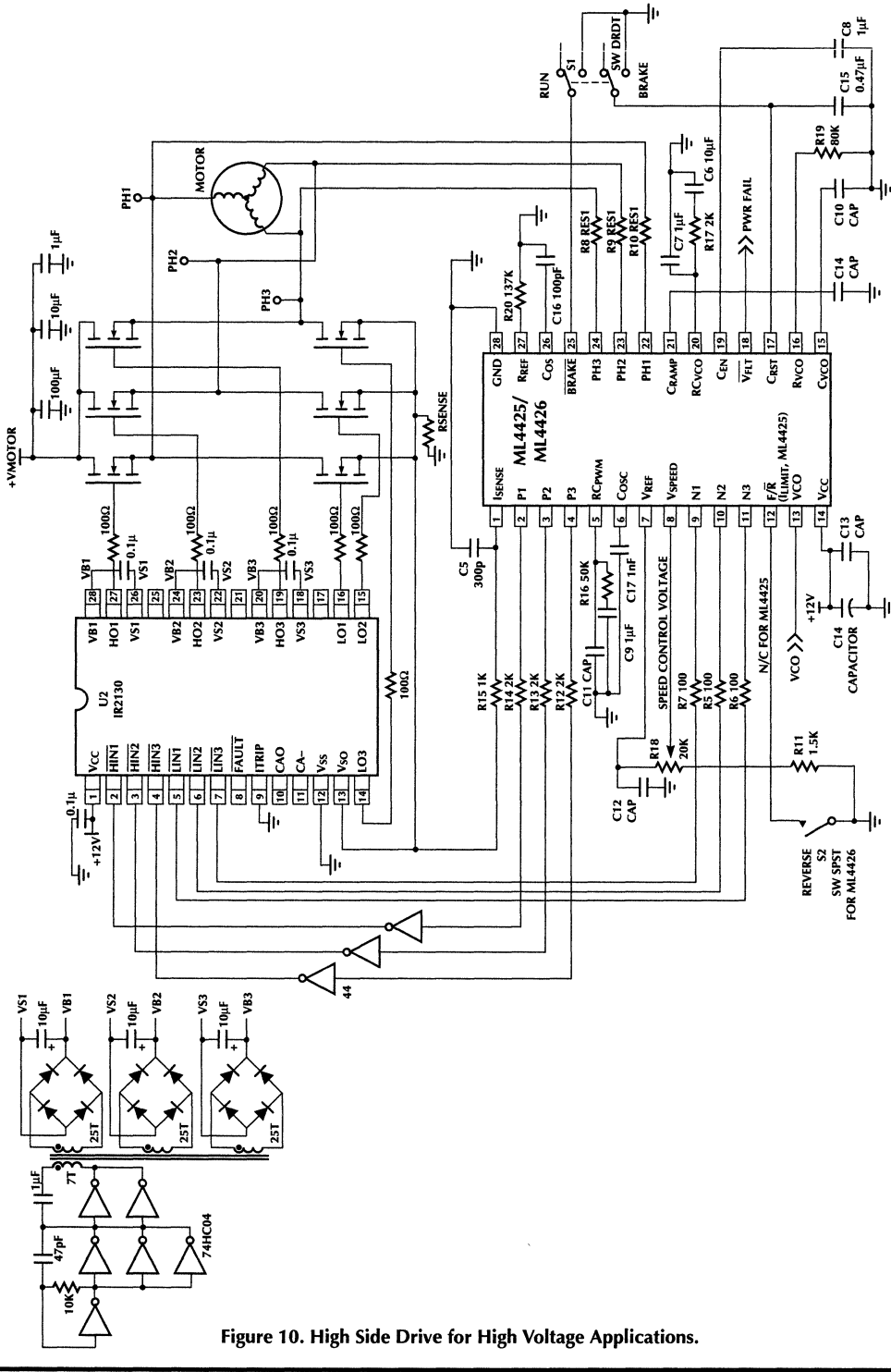


Figure 10. High Side Drive for High Voltage Applications.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4425CS	0°C to +70°C	28-Pin SOIC (S28W)
ML4425CP	0°C to +70°C	28-Pin DIP (P28N)
ML4425IS	–40°C to +85°C	28-Pin SOIC (S28W)
ML4425IP	–40°C to +85°C	28-Pin DIP (P28N
ML4426CS	0°C to +70°C	28-Pin SOIC (S28W)
ML4426CP	0°C to +70°C	28-Pin DIP (P28N)
ML4426IS	–40°C to +85°C	28-Pin SOIC (S28W)
ML4426IP	–40°C to +85°C	28-Pin DIP (P28N)

Micro Linear

ML4431

Servo Demodulator

GENERAL DESCRIPTION

The ML4431 provides all of the analog circuitry necessary for the demodulation of di-bit servo signal information in Winchester disk drives. It interfaces to the servo head preamp and provides quadrature position signal outputs for the servo controller circuitry.

The ML4431 includes a high-performance 592-type input amplifier and differential AGC circuit. External logic is designed to meet the needs of the particular servo system utilizing the VCO and Charge Pump to create a PLL time base for Peak Detector gating. The SYNC output provides servo channel timing information for the logic.

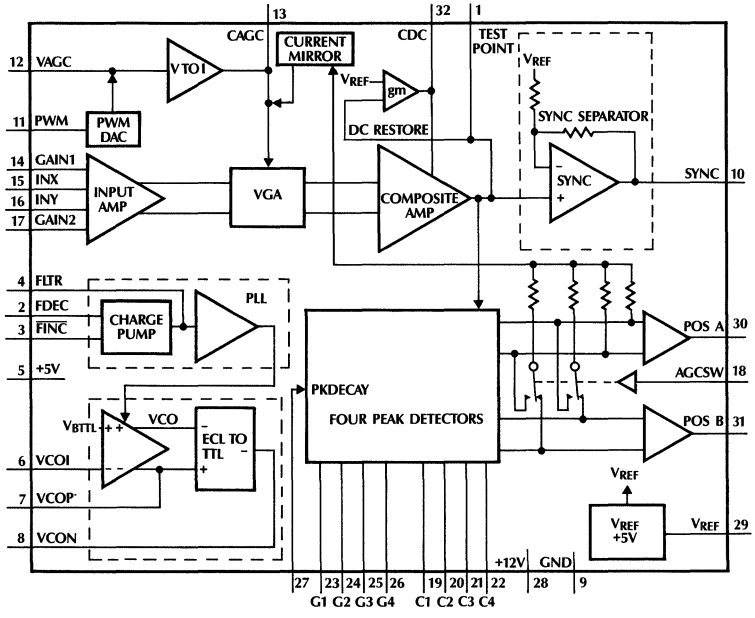
The ML4431 has an ECL-type VCO, with an internal ECL-to-TTL converter for simplified interfacing.

The ML4431, when combined with the ML4402 Servo Driver, the ML4403, ML4413 Servo Controller and the ML4404 Trajectory Generator, provides a flexible closed-loop servo control system.

FEATURES

- Combines all analog di-bit demodulation circuitry
- Logic track-type switching can be used to minimize demodulator offset
- Exponential AGC characteristics makes AGC settling independent of input step size
- External loop compensation of analog blocks
- External digital circuitry allows flexible pattern format
- On-chip band gap voltage reference eliminates external referencing
- Operates from 5V and 12V power supplies
- Programmable Peak Detector Discharge Current
- Digitally-controlled AGC set point
- TTL output VCO
- AGC Sense switchable to "POSA only" or both "POSA and POSB"
- Compatible with Micro Linear's ML4403, ML4413 Servo Controller, ML4402 Servo Driver and ML4404 Trajectory Generator

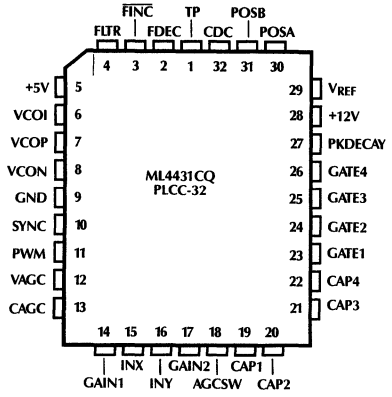
BLOCK DIAGRAM



Micro Linear

PIN CONNECTIONS

ML4431 32-Pin PCC



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	TP	Composite test point, normally left unconnected.
2	FDEC	Charge pump frequency decrement input.
3	$\overline{\text{FINC}}$	Charge pump frequency increment input.
4	FLTR	PLL loop compensation terminal.
5	+5V	+5V supply.
6	VCOI	VCO input.
7	VCOP	VCO positive output, for capacitive feedback to VCOI.
8	VCON	VCO negative output, drives resistive feedback to VCOI.
9	GND	Ground.
10	SYNC	SYNC pulse output.
11	PWM	PWM DAC input to adjust AGC set point.
12	VAGC	AGC gain reference voltage input.
13	CAGC	External capacitor to set AGC response.
14	GAIN1	Input amplifier gain adjusting RC terminal 1
15	INX	X input into input amplifier.
16	INY	Y input into input amplifier.
17	GAIN2	Input amplifier gain adjusting RC terminal 2.
18	AGCSW	Selects between "POSA only" or "POSA and POSB" AGC sense operation. Logic "0" selects "POSA only" operation. Logic "1" selects "POSA and POSB" operation.
19	CAP1	Peak detector 1 capacitor.
20	CAP2	Peak detector 2 capacitor.
21	CAP3	Peak detector 3 capacitor.
22	CAP4	Peak detector 4 capacitor.
23	GATE1	Peak detector 1 gate input (TTL) Logic "1" enabled, "0" disabled.
24	GATE2	Peak detector 2 gate input (TTL) Logic "1" enabled, "0" disabled.
25	GATE3	Peak detector 3 gate input (TTL) Logic "1" enabled, "0" disabled.
26	GATE4	Peak detector 4 gate input (TTL) Logic "1" enabled, "0" disabled.
27	PKDECAY	Sets peak detector discharge current.
28	+12V	+12V supply.
29	V_{REF}	Voltage reference output.
30	POSA	Position output A. POSA = Peak Detector 1 – Peak Detector 2
31	POSB	Position output B. POSA = Peak Detector 3 – Peak Detector 4
32	CDC	External capacitor terminal to set DC restore response.

5

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Power Supply Voltage Range, V_{CC} 14V
Input Voltages:
- GAIN1, GAIN2 ..... –0.3 to 8V
- C_{AGC} ..... –0.3 to 7.0V
- V_{AGC}, PWM, VCOI ..... –0.3 to 5.3V
- CAP1, CAP2, CAP3, CAP4 ..... –0.3 to 10V
- GATE1, GATE2, GATE3, GATE4, VCOP ..... –0.3 to 7.5V
- INX, INY, VCON, FINC, FDEC, C_{DC}, C_{AGC}, FLTR ..... –0.3 to V_{CC} +0.3V

θ_{JA} for PLCC-32 ..... ≈60°C/Watt
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature (T_{JMAX}) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
Supply Voltage $V_{(+12V)}$ ..... $12V_{DC} \pm 10\%$
Supply Voltage $V_{(+5V)}$ ..... $5V_{DC} \pm 10\%$
Input Coupling Capacitance (C_I) 0.01µF
Input Amp Gain Capacitance (C_G) 0.047µF
Input Amp Gain Resistance (R_G) 1kΩ
AGC Response Compensation Capacitance (C_A) 0.018µF
Composite DC Restore Capacitance (C_D) 0.018µF
PLL Compensation Components:
- C_{CP1} 0.1µF
- C_{CP2} 1µF
- R_{CP} 910Ω

VCO Components:
- C_V 39pF
- R_V 1500Ω
- RL 680Ω

Peak Detector Capacitance (CAP1 thru CAP4) 270pF
On track Base-to-Peak Voltage at pin TP 1.75V
V_{GA} Gain Control Voltage (at pin C_{AGC}) ..... ≈2.4V
R_{SET} 330KΩ

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of T_A = 0°C to 70°C, $V_{(+12V)}$ = 10.8 to 13.2V, $V_{(+5V)}$ = 4.5 to 5.5V, V_{VAGC} = 4.0V, and external components as recommended above, unless otherwise specified (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
I_{+12}	Supply Current	V_{+12} = 12V, V_{+5} = 5V		73	51	mA
I_{+5}	Supply Current	V_{+12} = 12V, V_{+5} = 5V		37	47	mA
TTL Inputs FINC, FDEC, GATE1, GATE2, GATE3, GATE4, PWM, AGCSW						
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	V_{IH} = 2.4V	–1		30	µA
I_{IL}	Low Level Input Current	V_{IL} = 0.4V	–20		1	µA
SYNC Output						
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6mA	0	0.35	0.5	V
V_{THR}	Positive going input threshold			V_{REF}+0.9		V
V_{THF}	Negative going input threshold			V_{REF}		V
$t_{PD}\pm$	Propagation Delay Rising, Falling	RL = 2k, C_L = 15pF		50		ns
VCON Output						
V_{OH}	High Level Output Voltage	I_{OH} = 50µA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6mA	0		0.5	V
VCO and Charge Pump Section						
I_{BIAS}	V_{COI} Input Bias Current		0	20	50	µA
I_{CH}, I_{DIS}	FLTR Charge and Discharge Current		330	450	590	µA
I_{CH}/I_{DIS}	FLTR Charge/Discharge Ratio		0.95	1.00	1.05	µA/µA
I_{OFF}	FLTR OFF State Current	FINC = 2.0, FDEC = 0.8	0	25	50	nA
F_{MAX}	MAX VCO Frequency to Maintain + and – 5% Control Range (Note 3)		20			MHz
V_{QH} (FLTR)	Charge Pump Maximum Voltage			$V_{(+12V)}$–1.2V		V
V_{QL} (FLTR)	Charge Pump Minimum Voltage			1.0		V

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of T_A = 0°C to 70°C, $V_{(+12V)}$ = 10.8 to 13.2V, $V_{(+5V)}$ = 4.5 to 5.5V, V_{AGC} = 4.0V, and external components as recommended above, unless otherwise specified (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCO and Charge Pump Section (Continued)						
F_{VCO}	VCO Frequency Range (Note 3)	T_A = 25°C, V_{+5} = 5V, V_{FLTR} = 6V, C_V = 30pF, R_V = 3.74KΩ, see figure 1	9.7	10.0	10.3	MHz
K_{VCO}	VCO Voltage to Frequency Factor			2		%/V
Input AMP, AGC AMP, and DC Restore						
R_{IN}	INX, INY Differential Input Resistance		7	10	14	kΩ
$I_{GAIN1,2}$	GAIN1, GAIN2 Bias Current		0.66	1.0	1.20	mA
R_{INAGC}	V_{AGC} Input Resistance		7	10	13	kΩ
G_{MAGC}	AGC Transconductance at C_{AGC}			370		μMHOS
R_{AGC}	Control Range of AGC Loop to Regulate Composite Amplitude to within 2% of Nominal			7/1		V/V
BW	Bandwidth from INX, INY to Composite (Note 4)		10	15		MHz
GMDCR	DC Restore Transconductance			500		μMHOS
Peak Detectors						
I_{CH}	Charge Current		5			mA
I_{DIS}	Discharge Current	T_A = 25°C, R_{SET} = 330K	10	15	20	μA
Voltage Reference						
V_{REF}	Reference Voltage	T_A = 25°C	4.75	5.00	5.25	V
TC	Tempco			50		ppm/°C
R_{OUT}	Load Regulation			2		mV/mA
PSRR	Line Regulation			10		mV/V
I_{SINK}	Maximum SINK Current		0.8			mA
Output Amplifiers (POSA, POSB)						
V_{OS}	Input Offset	V_{CAP}1–4 = 6V	–10	0	10	mV
A_V	Gain		1.15	1.20	1.25	V/V
A_{VA}/A_{VB}	Gain Tracking		–3	0	+3	%
V_{OUT}	Output Voltage Range		1.0		9.5	V
I_{SRC}	Output Source Current		3			mA
I_{SNK}	Output Sink Current		2			mA
SR	Slew Rate			2.5		V/μs
BW	3dB Gain Bandwidth			3		MHz

Note 1: 0°C to 70°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Typicals are parametric norm at 25°C.

Note 3: This parameter is guaranteed but not 100% tested and is not used in outgoing quality level calculations.

APPLICATION HINTS

Using a nominal on-track servo signal, amplitude adjustment should be made as follows:

1. Set composite signal amplitude, measured at pin TP, by adjusting voltage at pin V_{AGC} (approximately 4.7 volts). The composite signal should be set to 1.75 volts base to peak of an on-track position pulse (an off-track position pulse will be about 3.5 volts maximum).
2. Adjust Rg so that the VGA is in mid-range. This is determined by measuring the voltage at pin C_{AGC}; it should be approximately 0.9 volts. C_{AGC} voltage will vary approximately ±0.5 volts over the AGC range.

FUNCTIONAL DESCRIPTION

INPUT AMPLIFIER

The input amplifier is equivalent to a wide-band 592 type video amplifier and provides amplification and buffering to the AGC circuitry. The Inputs INX and INY, which must be AC coupled, accept the composite analog signal from the servo head differential preamplifier. Internal input termination resistors eliminate the need for external bias resistors. Prefiltering of the signal is normally desired to eliminate unwanted components. External components R_G and C_G determine the input amplifier's low frequency cutoff and gain as follows:

$$FC = \frac{1}{2\pi(R_G + 60\Omega)C_G} \qquad A_V = \frac{1700}{R_G + 60\Omega}$$

Where: C_G = External series capacitance between pins GAIN1 and GAIN2
R_G = External series resistance between pins GAIN1 and GAIN2

AUTOMATIC GAIN CONTROL (AGC)

The purpose of the AGC loop is to maintain a constant peak output voltage level at outputs POSA and POSB. This peak level is established by the reference voltage applied to pin V_{AGC}.

$$V_{P-P\ (Composite\ Position\ Pulses)} = K1 \times V_{AGC} + K2$$

Where: K1 = 0.65
K2 = .13 * V_{REF}

In this closed-loop system, the peak detector output voltages are fed back and combined with the V_{AGC} voltage to provide a gain control current. The current controls the variable gain amplifier (VGA) and is compensated at pin C_{AGC} to provide control of AGC bandwidth. The bandwidth of the entire AGC loop is determined by:

$$BW = \frac{K\ V_{VAGC}}{2\pi\ C_A}$$

Where: K = 2.8×10^{-4}
V_{VAGC} = External reference voltage at pin V_{AGC}
C_A = External capacitance at pin C_{AGC}

PWM CONTROL OF AGC SET POINT

The PWM input (pin 10) accepts a variable duty-cycle input to control the AGC set point. The relationship between duty-cycle and set point is:

100% duty-cycle ..... AGC set point is equal to V_{REF}.

0% duty-cycle ..... AGC set point equal to 0.6 × V_{REF}.

A filter capacitor from pin 11 to ground is required to filter the PWM signal. This capacitor should be sufficiently large relative to the 10KΩ nominal internal termination resistance at pin 11.

The AGC set point may be set manually via direct voltage control of pin 12 if desired. Pin 11 should be grounded in this case.

SWITCHING THE AGC SENSE RESISTORS

The AGCSW input (pin 17) allows selection of the AGC sense. The choices are:

AGCSW low ..... AGC senses POS A peak detector outputs only.

AGCSW high ..... AGC senses POS A and POS B peak detector outputs.

COMPOSITE AMPLIFIER

The input amplifier and AGC circuit of the ML4431 operate in a differential signal mode to provide good common mode and power supply rejection. The composite amplifier converts the differential signal into a buffered single-ended signal for the peak detector circuitry. The DC base line of the composite signal is equal to V_{REF}. The bandwidth of the DC restore function is controlled by capacitor C_D at pin C_{DC} with the following relationship:

$$BW = \frac{gm}{2\pi\ C_D}$$

Where: $gm = \frac{1}{2K\Omega}$
C_D = External capacitance at pin C_{DC}

The composite signal is available at pin TP and is normally left unconnected. For short circuit protection a 750Ω resistor is connected in series with pin TP internally.

SYNCHRONIZATION PULSE SEPARATOR

The SYNC pulse separator is a threshold comparator with hysteresis which passes pulses from the composite amplifier above a set threshold. It provides a buffered TTL output. The SYNC output, when gated through an external one-shot, is used to control the external gate timing and PLL logic. Active pull-up differs from ML4401 SYNC.

PEAK DETECTOR

The peak detector circuit captures the peak signal amplitude of the di-bit pulses. The gates are controlled by inputs GATE1 through GATE4. Timing is established by the external logic circuitry. The external peak detector capacitors are connected from pins CAP1 through CAP4 to ground. The peak detector discharge rate (set by CAP1–CAP4 and current out of PKDECAY) determines the maximum track crossing rate during an access operation. The peak detector outputs are fed into internal differential amplifiers that calculate the track error signals and provide buffered outputs POSA and POSB as follows:

POSA = 1.20 (CAP1 – CAP2) + V_{REF}
POSB = 1.20 (CAP3 – CAP4) + V_{REF}

PEAK DETECTOR DECAY RATE CONTROL

The decay rate of the peak detector can be programmed by changing the external resistor R_{SET} (pin 26, see connection diagram). The decay rate is determined by the discharge current for the hold capacitors C1 – C4. The relationship between the discharge current and R_{SET} is:

$$I_{DISCHARGE} = \frac{V_{REF}}{R_{SET}}$$

VOLTAGE CONTROLLED OSCILLATOR AND CHARGE PUMP

The VCO and external phase compare logic provide a time base for peak detector gate synchronization. Inputs FINC and FDEC provide increment and decrement signals to the charge pump for changing the oscillator frequency. The FINC and FDEC inputs gate the charge pump for the duration of the pulse width. The RC timing network formed by C_V and R_V at pins VCOI, VCON, and VCOP control the oscillators center frequency. (See Typical Performance Characteristics)

R_V should be greater than 1000Ω, Too low of a value will result in excessive power dissipation. RL should be about 680Ω.

The VCO output should only be taken from pin VCON. Charge pump capacitor C_{CP1} is connected from pin FLTR to ground. Components R_{CP} and C_{CP2} are also connected in series from pin FLTR to ground to provide VCO loop compensation.

INTERNAL VOLTAGE REFERENCE

V_{REF} is an internal band-gap voltage reference. It is buffered and available at pin V_{REF} and is used by the ML4402, ML4403, ML4404 and other chips requiring a 5 volt reference.

EXTERNAL LOGIC

The external logic provided by the user typically has a complexity of about 150 to 300 equivalent gates. Complexity and architecture depends on the users di-bit pattern and control function.

Note: Stray capacitance should be considered in applying the above relationships when low capacitor values are used. Stray capacitance of the integrated circuit terminal is typically about 2 to 3pF.

TYPICAL PERFORMANCE CHARACTERISTICS

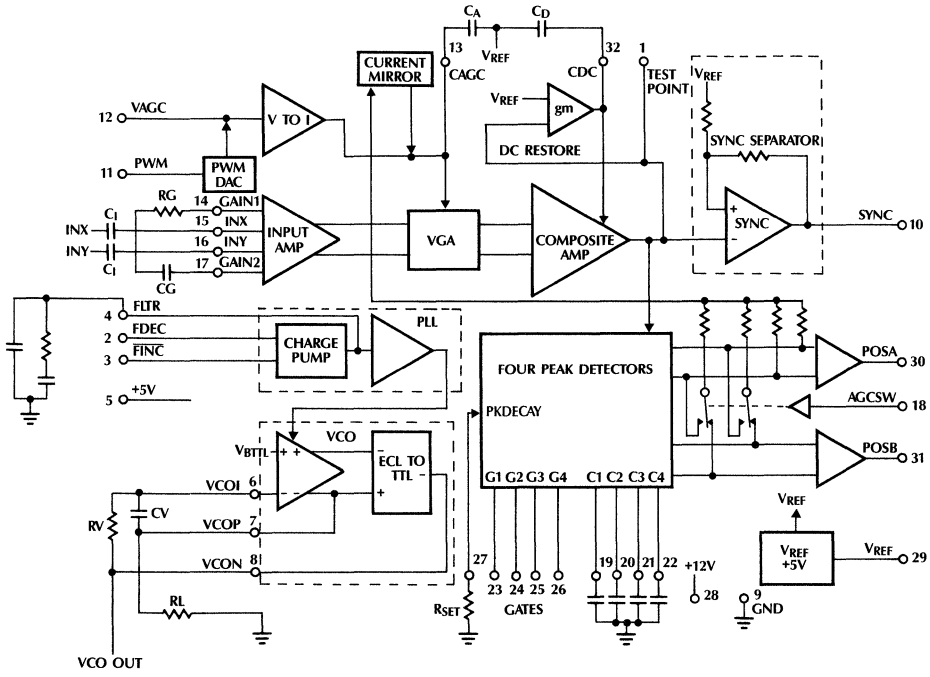
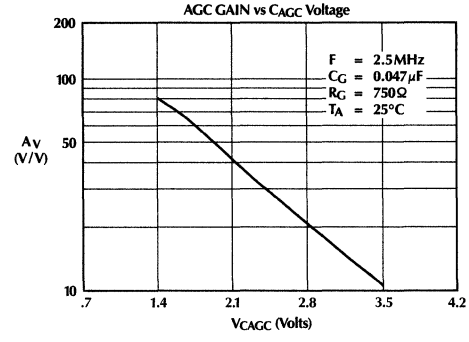


Figure 1. ML4431 Connection Diagram



ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML4431CQ	0°C to +70°C	MOLDED PCC (Q32)

ML4451

2-Channel Preamplifier for Tape Drives

GENERAL DESCRIPTION

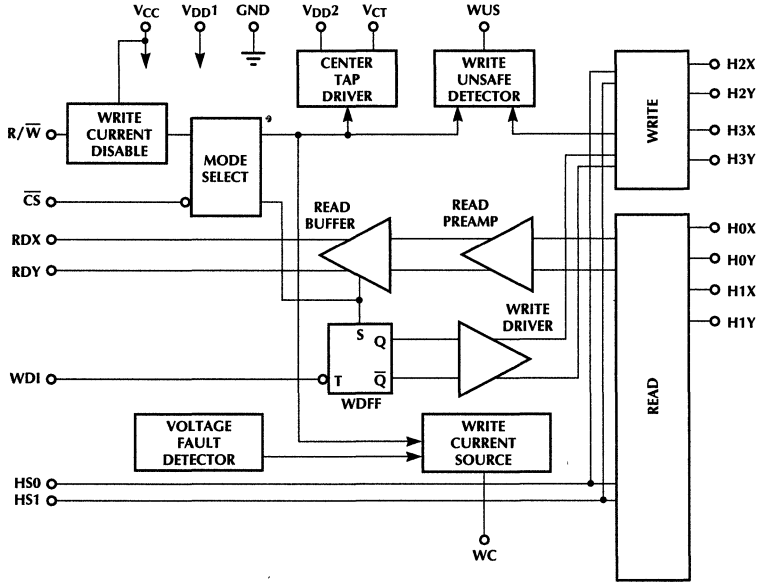
The ML4451 is a bipolar monolithic read/write circuit designed for use with center-tapped ferrite recording heads in tape drive systems. Single ended head drive is also possible by connecting one input to center tap and the other to the head which also returns to center tap.

The ML4451 provides two separate multiplexed read and write data channels. These circuits exhibit features like reduced input bias current and higher read channel voltage gain, which provide a low noise read data path. It also provides improved write current stability and eliminates write current "glitches" during power-up. The control signals to this chip are TTL compatible. The ML4451 is available in a 24-pin SOIC package.

FEATURES

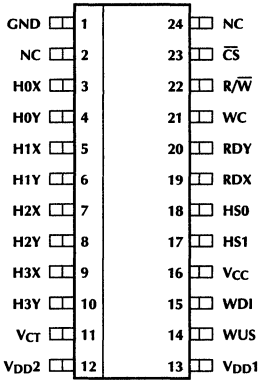
- Enhanced write current stability
- Designed for center-tapped ferrite heads in tape drives
- Provides lower current noise
  Min $A_V > 150$, Max $I_B < 15\mu A$
- Easily multiplexed for larger systems
- Power supply fault protection
- $1.5nV/\sqrt{Hz}$ maximum input noise voltage
- Programmable write current source
- Includes write unsafe detection
- +5V, +12V power supplies

BLOCK DIAGRAM



PIN CONNECTION

ML4451
24-Pin SOIC



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
HS0–HS1	Head Select (four heads)
$\overline{CS}$	$\overline{\text{Chip Select}}$ (low level enables chip)
R/$\overline{W}$	Read/$\overline{\text{Write}}$ (high level selects Read Mode)
WUS	Write Unsafe, open collector output (high level indicates an unsafe writing condition)
WDI	Write Data In (negative transition toggles head current direction)
H0X, H1X	Read head X connections
H2X, H3X	Write head X connections
H0Y, H1Y	Read head Y connections
H2Y, H3Y	Write head Y connections

NAME	FUNCTION
RDX, RDY	X, Y Read Data (differential read signal out)
WC	Write Current (used to set the write current magnitude)
V_{CT}	Voltage Center Tap (center tap voltage source)
VCC	+5 volts
$V_{DD}1$	+12 volts
$V_{DD}2$	Positive supply for center tap
GND	Ground

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ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range
- $V_{DD}1$ ..... –0.3 to 14V_{DC}
- $V_{DD}2$ ..... –0.3 to 14V_{DC}
- V_{CC} ..... –0.3 to 6V_{DC}

Input Voltage Range
- Digital Inputs ($\overline{CS}$, R/$\overline{W}$, HS, WDI) .. –0.3 to V_{CC} +0.3V_{DC}
- Head Ports (H0X-H7X, HOY-H7) . –0.3 to $V_{DD}1$ +0.3V_{DC}
- Write Unsafe (WUS) ..... –0.3 to 14V_{DC}

Write Current (I_W) 60mA

Output Current
- Read Data (RDX, RDY) ..... –10mA
- Center Tap Current (I_{CT}) ..... –60mA
- Write Unsafe (WUS) 12mA

Storage Temperature ..... –65°C to 150°C

Junction Temperature (T_J) ..... 135°C

Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Supply Voltage
- $V_{DD}1$ ..... 12V ±10%
- V_{CC} ..... 5V ±10%

Head Inductance
- L_H ..... 5 to 15µH

Damping Resistor (R_D) ..... 500 to 2000Ω

RCT Resistor (1/4 Watt) ..... 12Ω ±5%

Write Current (I_W) ..... 10 to 40mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $V_{DD}1 = V_{DD}2 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 40mA$, $0°C \le T_A \le 70°C$ (Notes 2 and 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
DC OPERATING CHARACTERISTICS						
I_{CC}	V_{CC} Supply Current	Read or Idle Mode Write Mode			35 30	mA mA
I_{DD}	V_{DD} Supply Current	Read Mode Write Mode Idle Mode			35 20 + I_W 20	mA mA mA
P_D	Power Dissipation	Read Mode Write Mode I_W = 40mA, R_{CT} = 0Ω Idle Mode			655 960 455	mW mW mW
DIGITAL INPUTS ($\overline{CS}$, R/$\overline{W}$, HS, WDI)						
V_{IH}	High Voltage		2			V_{DC}
V_{IL}	Low Voltage				0.8	V_{DC}
I_{IH}	High Current	V_{IH} = 2.0V			100	µA
I_{IL}	Low Current	V_{IL} = 0.8V	–0.4			mA
WUS OUTPUT						
V_{OL}	Output Low Voltage	I_{OL} = 8mA (Safe)			0.5	V_{DC}
I_{OH}	Output High Current	V_{OH} = 5V (Unsafe)			100	µA
CENTER TAP VOLTAGES						
V_{CT}	Read Mode	Read Mode		4		V_{DC}
V_{CT}	Write Mode	Write Mode		6		V_{DC}

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1$ = 12V ±10%, V_{CC} = 5V ±10%, R_{CT} = 120Ω ±5%, I_W = 35mA, L_H = 10µH, R_D = 750Ω f_{DATA} = 5MHz, C_L(RDX, RDY) ≤ 20pF, 0°C ≤ T_A ≤ 70°C
(Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
WRITE MODE CHARACTERISTICS						
I_{HCW}	Head Current (per Side)	Write Mode $0 \le V_{CC} \le 3.7V$ $0 \le V_{DD}1 \le 8.7V$	–200		200	µA
I_{WR}	Write Current Range	$I_W = K/R_{WC}$	10		40	mA
K	Write Current Constant		2.375		2.625	
V_{HD}	Differential Head Voltage Swing		7.0			V_{PK}
I_{HU}	Unselected Head Transient Current				2	mA_{PK}
C_{OD}	Differential Output Capacitance				15	pF
R_{OD}	Differential Output Resistance		10k			Ω
f_{WDI}	WDI Transition Frequency	WUS = Low	250			kHz
A_I	IWC to Head Current Gain			0.99		mA/mA
I_L	Unselected Head Leakage	Sum of X & Y Side Leakage Current			85	µA
READ MODE CHARACTERISTICS						
A_V	Differential Voltage Gain	V_{IN} = 1mV_{P-P} @ 300kHz R_L (RDX, RDY) = 1kΩ	150	180	205	V/V
DR	Dynamic Range	DC Input Voltage (V_I) Where Gain Falls 10% $V_{IN} = V_I$ + 0.5mV_{P-P} @ 300kHz	–3		+3	mV
BW	Bandwidth (–3dB)	$\|Z_S\| < 5Ω$, V_{IN} = 1mV_{P-P}	30			MHz
e_{IN}	Input Noise Voltage	BW = 15MHz, L_H = 0, R_H = 0			1.5	nV/$\sqrt{Hz}$
C_{IN}	Differential Input Capacitance	f = 5MHz			20	pF
R_{IN}	Differential Input Resistance	f = 5MHz, T_J = 25°C	2k			Ω
I_{HCR}	Head Current (per side)	Read or Idle Mode $0 \le V_{CC} \le 5.5V$ $0 \le V_{DD}1 \le 13.2V$	–200		200	µA
I_N	Input Bias Current (1 side)				15	µA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V_{CT}$ + 100mV_{P-P} @ f = 5MHz	50			dB
PSRR	Power Supply Rejection Ratio	100mV_{P-P} @ %MHz on $V_{DD}1$, $V_{DD}1$, $V_{DD}2$, or V_{CC}	45			dB
CS	Channel Separation	Unselected Channels: V_{IN} = 100mV_{P-P} @ 5MHz and Selected Channel: V_{IN} = 0V_{P-P}	45			dB
V_{OS}	Output Offset Voltage	Read Mode Write or Idle Mode	–460 –20		+460 +20	mV mV
R_{OUT}	Single-Ended Output Resistance	f = 5MHz			30	Ω

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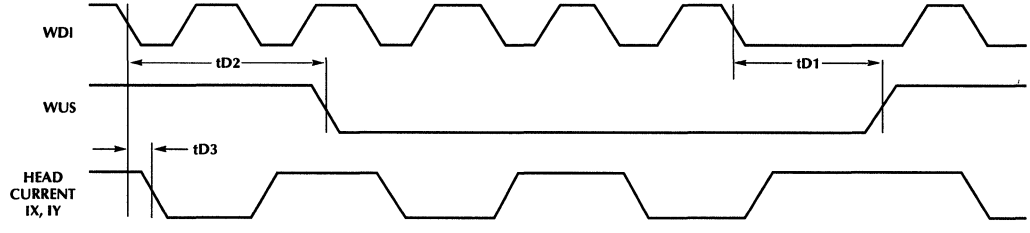
ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1$ = 12V ±10%, V_{CC} = 5V ±10%, R_{CT} = 120Ω ±5%, I_W = 35mA, L_H = 10µH, R_D = 750Ω f_{DATA} = 5MHz, C_L(RDX, RDY) ≤ 20pF, 0°C ≤ T_A ≤ 70°C
(Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
READ MODE CHARACTERISTICS (Continued)						
I_L	Leakage Current, RDX, RDY	(RDX, RDY) = 6V Write or Idle Mode	–100		100	µA
I_O	Output Current	AC Coupled Load, RDX to RDY	±2.1			mA
SWITCHING CHARACTERISTICS						
t_{RW}	R/$\overline{W}$ to Write Switching Delay	To 90% of Write Current Output			1	µs
t_{WR}	R/$\overline{W}$ to Read Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	µs
t_{IW} or t_{RI}	$\overline{CS}$ to Select Switching Delay	To 90% of Write Current or to 90% of 100mV, 10MHz Read Signal Envelope			1	µs
t_{WI} or t_{RI}	$\overline{CS}$ to Unselect Switching Delay	To 90% Decay of 200mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	µs
t_{HS}	Head Select Switching Delay	To 90% of 100MHz Read Signal Envelope			1	µs
tD1	Safe to Unsafe Write Unsafe Delay	I_W = 35mA	1.6		8	µs
tD2	Safe to Unsafe Write Unsafe Delay	I_W = 35mA			1	µs
tD3	Prop. Delay Head Current	L_H = 0, R_H = 0 From 50% points			25	ns
	Asymmetry Head Current	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	ns
	Rise/Fall Head Current	10% and 90% Points			20	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 3: Maximum junction temperature (T_J) should not exceed 135°C.

TIMING DIAGRAM



Write mode Timing Diagram

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

For any selected head, the ML4451 functions as a read amplifier when in Read mode, or as a write amplifier when in the Write mode. Pins HS0 and HS1 determine head selection while pin R/$\overline{W}$ controls the Read/Write mode. A detected "write-unsafe" condition is indicated by pin WUS.

READ MODE

When the ML4451 is in the Read Mode, it operates as a low-noise differential amplifier on the selected channel. In Read mode the write data flip-flop is set and both the write unsafe detector and the write current source are deactivated. The center tap voltage is also lowered. Pins RDX and RDY provide differential emitter follower outputs which are in phase with the X and Y head input pins.

Note that during the Read or Chip Deselect mode the internal write current is deactivated, thus making external write current gating unnecessary.

WRITE MODE

The ML4451 operates as a write-current switch when in the Write mode. Write current magnitude is determined by the following relationship:

$$I_K = K/R_{WC}$$

Where: K = Write Current Constant

R_{WC} = Resistance connected between pin WC and GND

The head current is toggled between the X and Y side of the selected head by a negative transition on WDI (Write Data Input). When switching the ML4451 to write mode, the WDFF (Write Data Flip-Flop) is initialized to pass write current through the X-side of the head.

The ML4451 exhibits enhanced write current stability which reduces the problem of oscillation. This is due to increased internal write current compensation. Also write current "glitches" during power-up are eliminated with an exclusive write current disabling function.

The WUS (Write Unsafe) pin is an open collector output that gives a logic high level for any of the following unsafe write conditions:

— Open head

— Open head center-tap

— Too low WDI frequency

— Read mode selected

— Device not selected

— No write current

Two negative transitions on WDI are required to clear WUS after the fault condition is removed.

The ML4451 also offers a voltage fault detection circuit that prevents write current during power-loss or power-up.

Table 1.

HEAD SELECT

HS1	HS0	HEAD
0	0	0
0	1	1
1	0	2
1	1	3
0	0	4
0	1	5
1	0	6
1	1	7

Notes: 0 = Logic Level Low
1 = Logic Level High
X = Don't Care

Table 2.

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

Notes: 0 = Logic Level Low
1 = Logic Level High
X = Don't Care

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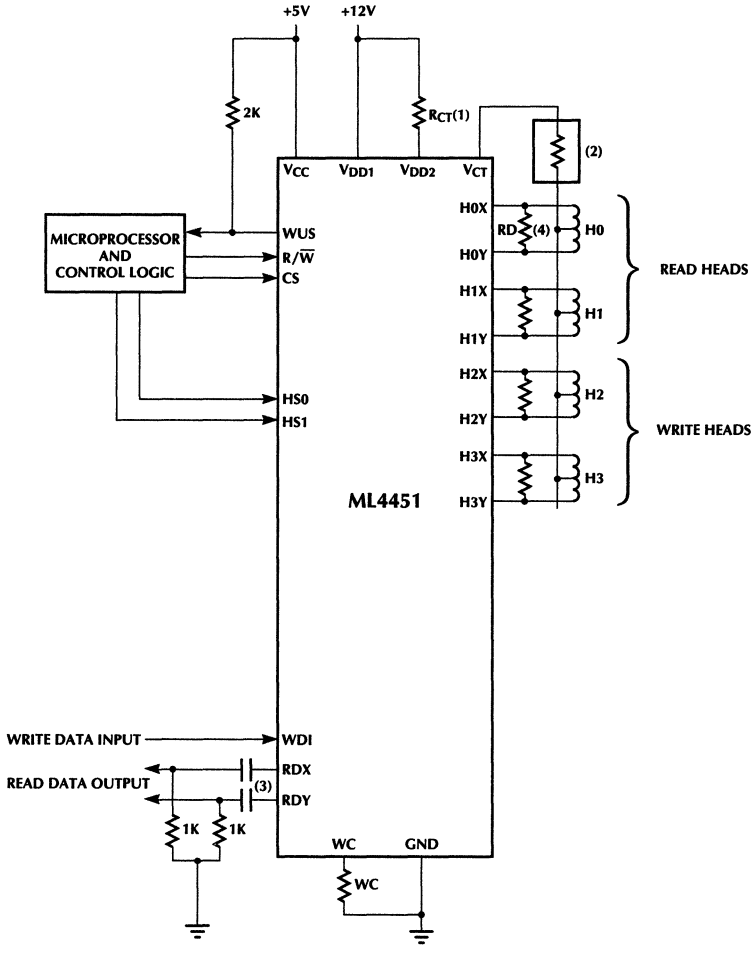
TYPICAL APPLICATION



Note 1: RCT is optional and is used to limit internal power dissipations (Otherwise connect $V_{DD}1$ to $V_{DD}2$).
RCT (1/2 Watt) = 120 (40/I_W) ohms, where I_W = Write Current, in mA.
Note 2: Ferrite bead optional: used to suppress write current overshoot and ringing. Recommend Ferroxcube 3659065/4A6.
Note 3: RDX and RDY load capacitance 20pF maximum. RDX and RDY output current must be limited to 100mA.

ORDERING INFORMATION

PART NUMBER	PACKAGE
ML4451	20-Lead SOIC (S24)

THERMAL CHARACTERISTICS

PIN COUNT	PACKAGE	θ_{ja}
24-Lead	SOIC	75°C/W

MR Head Preamplifier for Tape Drives 2-CH Read and 1-CH Write with Readback

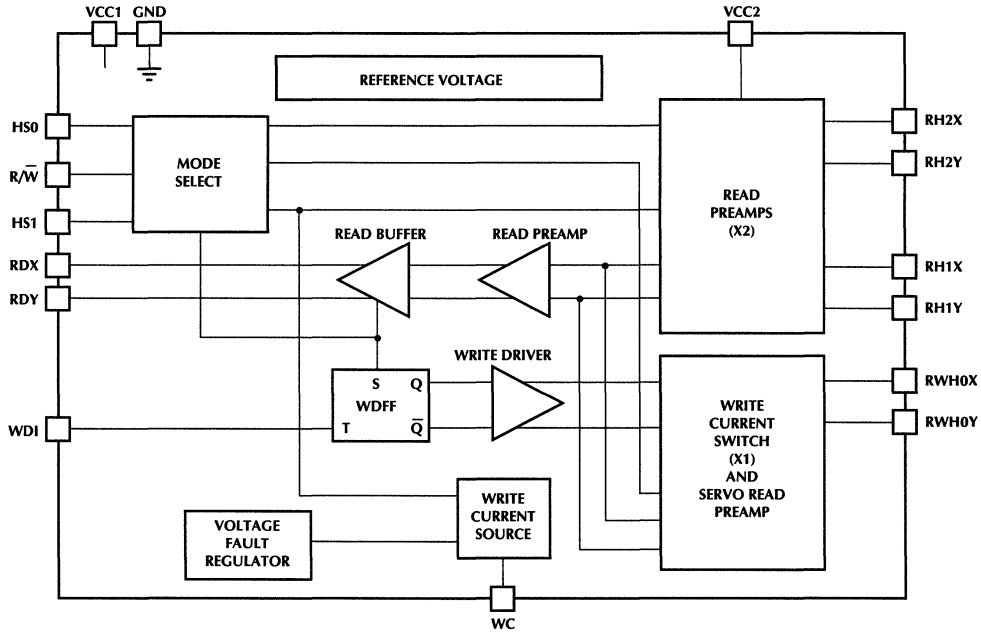
GENERAL DESCRIPTION

The ML4452 is a bipoloar monolithic read preamp circuit designed for use with two-terminal thin-film or MR recording heads for tape drives. It provides two dedicated low noise read channels and a separate write channel with read back capability for use with the servo head. The write channel in the ML4452 incorporates an internal 700Ω damping resistor which dampens the write signals to the head. Additionally write current control and data protection circuitry are also provided. Because the read channels are independent there is no voltage drift, which is a problem with normal preamps when switching from the write to read mode. Power supply fault protection is provided by disabling the write current generator during power sequencing.

FEATURES

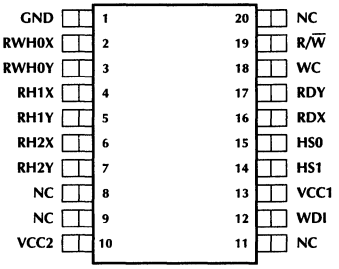
- Architecturally Compatible to SSI's 32R4610AR
- Single +5 Volt Operation, P_{MAX} < 200mW
- Read Mode Gain = 125 V/V
- Dedicated Read Channels for Greater Noise Immunity
- Write Channel also Provides Servo Readback Capability
- 700 Ohm Damping Resistor in the Write Channel
- Input Noise = 0.85nV/$\sqrt{Hz}$ max
- Input Capacitance = 45pF max
- Write Current Range = 10–35mA
- Enhanced System Write to Read Recovery Time
- Power Supply Fault Protection
- No Write Current Glitching on Power-up
- 20-pin SSOP Package

BLOCK DIAGRAM



PIN CONNECTION

ML4452
20-Pin SSOP (R20)



TOP VIEW

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0, HS1	I	Head Select: Selects one of three heads
R/$\overline{W}$	I	Read/Write: A high selects read mode and a low selects write mode
WDI	I	Write Data In: Changes the direction of the current in the head
RH1X, RH2X RH1Y, RH2Y	I	X, Y Head Connectors for MR Read only
RWH0X RWH0Y	I/O	X, Y Head Connectors for Servo MR read and inductive write

NAME	TYPE	FUNCTION
RDX, RDY	O	X, Y Read Data: Differential read data output
WC		Write Current: Used to set the magnitude of the write current
VCC1	I	+5 volt supply
VCC2	I	+5 volt supply for write current drivers
GND	I	Ground

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ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage ($V_{CC}1$) ..... –0.3 to +7VDC
DC Supply Voltage ($V_{CC}2$) ..... –0.3 to +7VDC
Write Current (I_W) 80mA
Digital Input Voltage (V_{IN}) ..... –0.3 to VCC1 + 0.3VDC
Head Port Voltage (V_H) ..... –0.3 to VCC1 + 0.3VDC
Output Current: RDX, RDY (I0) ..... –10mA
Storage Temperature T_{STG} ..... –65 to +150°C

OPERATING CONDITIONS

DC Supply Voltage ($V_{CC}1$) ..... 5 ±5% VDC
DC Supply Voltage ($V_{CC}2$) ..... 5 ±5% VDC
Operating Junction Temperature (T_J) ..... +25° to +110°C

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC1 Supply Current	Read Mode Write Mode			33 27	mA
VCC2 Supply Current	Read Mode Write Mode			11 10 +I_W	mA
Power Dissipation	Read Mode Write Mode			230 190 +4I_W	mW
Digital Inputs					
Input Low Voltage (V_{IL})				0.8	VDC
Input High Voltage (V_{IH})		2.0			VDC
Input Low Current	V_{IL} = 0.8V	–0.4			mA
Input High Current	V_{IH} = 2.0V			100	µA
VCC1 Fault Voltage	I_W < 0.2 mA	3.7	4.0	4.2	VDC
Write Characteristics					
Write Current Constant "K"			0.99		
Write Current Voltage (VWC)		1.15	1.25	1.35	V
Differential Head Voltage Swing		3.4	6		Vpp
Unselected Head Current				1	mA (pk)
Head Differential Load Capacitance				25	pF
Head Differential Load Resistance	R_D	500	700	950	ohms
Write Current Range (Iw)		10		45	mA
Read Characteristics C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1KΩ					
Differential Voltage Gain	V_{IN} = 1mVpp @ 1MHz	100	125	150	V/V
Voltage BW –1dB	|Zs| < 5 ohm, V_{IN} = 1mVpp	20			MHz
–3dB		35			MHz
Input Noise Voltage	BW = 15MHz, L_H = 0, R_H = 0		0.6	0.85	nV/√Hz
Differential Input Capacitance	V_{IN} = 1mVpp, f = 5MHz		27	35	pF
Differential Input Resistance	V_{IN} = 1mVpp, f = 5MHz Read/Write head #0 Read heads #1 & #2	 360 900			 ohms ohms
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value. @ f = 5MHz	3			mVpp

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Read Characteristics C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1KΩ (Continued)					
Common Mode Rejection Ratio	V_{IN} = 0VDC + 100mVpp @ 5MHz	45			dB
Power Supply Rejection Ratio Separation	100mVpp @ 5MHz on V_{CC} Unselected channels driven with V_{IN} = 0VDC + 100mVpp	40 45			dBChannel dB
Output Offset Voltage		–200		+200	mV
Single-ended Output Resistance	f = 5MHz			40	Ohms
Output Current	AC Coupled Load, RDX to RDY	1.4			mA
RDX, RDY Common Mode Output		2.0	2.8	3.5	VDC
Switching Characteristics I_W = 20mA, R_H = 30 Ohm, L_H = 1µH, f_{DATA} = 5MHz					
R/$\overline{W}$ Read to Write	R/W to 90% of write current		0.1	1.0	µs
R/$\overline{W}$ Write to Read	R/W to 90% of 100mV Read signal envelope		0.5	1.0	µs
HS 0, 1 to any head	To 90% of 100 mV 10 MHz Read signal envelope		0.2	1.0	µs
Head Current WDI to I_X-I_Y (TD3) Asymmetry Rise/Fall Time	L_H = 0, R_H = 0 From 50% points WDI has 1ns rise/fall time 10% to 90% points			 32 1.0 12	 ns ns ns

TIMING DIAGRAM

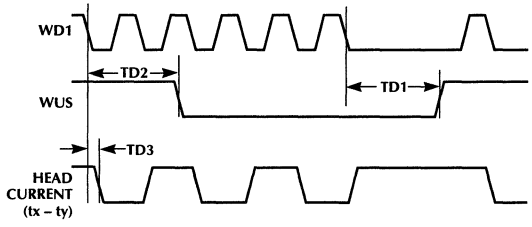


Figure 1. Write Mode.

MODE AND HEAD SELECT

R/$\overline{W}$	HS1	HS0	HEAD	MODE
0	0	0	RWH0	Write
1	0	0	RWH0	Read
1	0	1	RH1	Read
1	1	0	RH2	Read
1	1	1	RESERVED	

Note: The TTL input R/$\overline{W}$ has an internal pull-up resistor to prevent an accidental write condition. The TTL inputs HS0 and HS1 have internal pull-downs.

FUNCTIONAL DESCRIPTION

The ML4452 has the ability to address up to 4 two-terminal thin-film heads and provide write drive or read amplification. Head selection and mode control are described in the tables below. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0 and HS1 have internal pull-downs. Internal clamp circuitry will protect the ML4610R/4611R from a head short to ground condition in any mode. The damping resistors are switched out during read mode, as identified by the R/$\overline{W}$ pin.

WRITE MODE OPERATION

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the ML4610R/4611R as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). A preceding read or idle mode select initializes the Write Data Flip-Flop to pass write current through the "X" side of the head. The current calculations are shown below:

Write current (peak) is given by:

$$I_W = \frac{K \times VWC}{RWC}$$

where

RWC is connected from pin WC to GND

Actual head current is given by:

$$I_{X,Y} = \frac{I_W}{1 + \frac{R_H}{R_D}}$$

where

R_H = head + external wire resistance

R_D = damping resistance

VOLTAGE FAULT DETECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power start-up, regardless of mode. The Write Unsafe (WUS) open collector output goes high under the conditions given below. After the fault condition is removed, a negative transition on WDI is required to clear WUS.

— Write Data Input frequency too low

— Device in Read Mode

— Chip is disabled or head is open

— No write current

READ MODE OPERATION

The Read mode configures the ML4452 as a low noise differential amplifier and deactivates the write current generator. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs. In the Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/$\overline{W}$ applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. The write current source is also deactivated for both the Read and Idle mode. In addition the ML4452 supports the feature by which the internal damping resistors are switched out in the read mode, which allows the full signal to be amplified.

IDLE MODE OPERATION

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum, less than 50mW.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4452CR	0°C to +70°C	20-Pin SSOP (R20)

ML4506

5V Disk Voice Coil Servo Driver

GENERAL DESCRIPTION

The ML4506 is a voice coil power driver intended for use in 5V Hard Disk servo systems. The ML4506 contains all power and control circuitry necessary to drive the voice coils of most small form factor drives. In addition, power fail detection and head retraction functions are provided for orderly shut-down of the drive.

The transconductance is programmed by a logic input at 1/4 A/V and 1/24 A/V respectively, using a 1Ω sense resistor. This allows for greater DAC resolution in digitally controlled servos during track follow without compromising dynamic range during seek.

The retraction circuit, main drive circuit, and control circuits are each powered from their own supplies. This allows maximum flexibility and provides for the lowest forward drop by eliminating the need for a blocking diode.

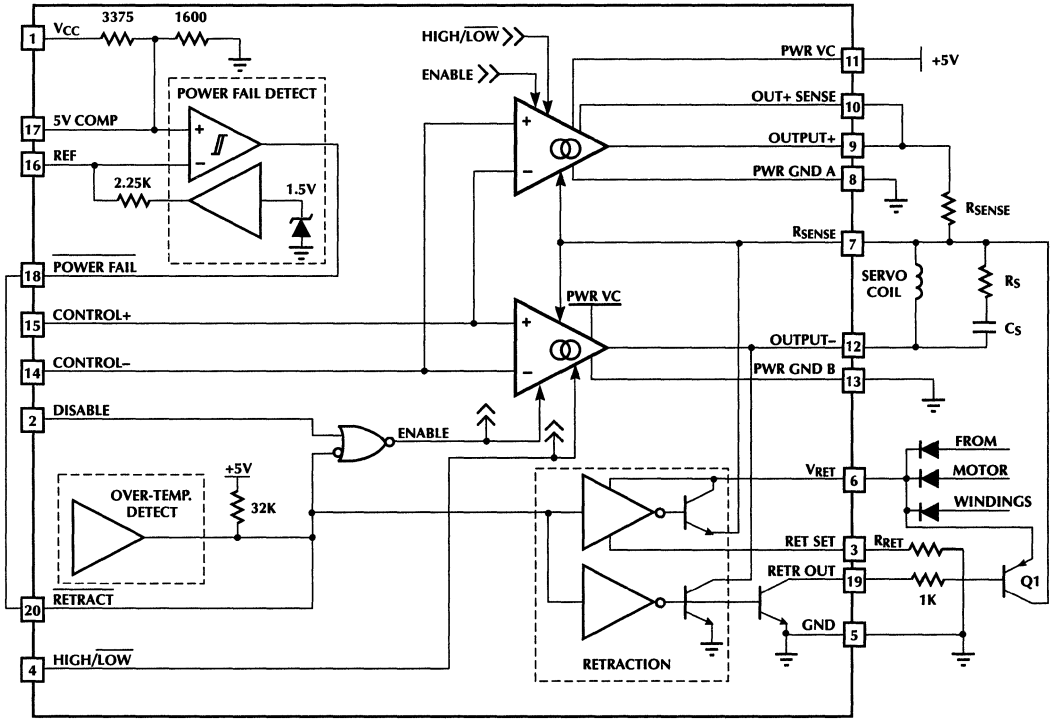
The power fail detection circuit includes a precision 1.5V bandgap reference.

The ML4506 is implemented using Micro Linear's bipolar array technology. This allows for easy customizing of the IC for a user's specific application.

FEATURES

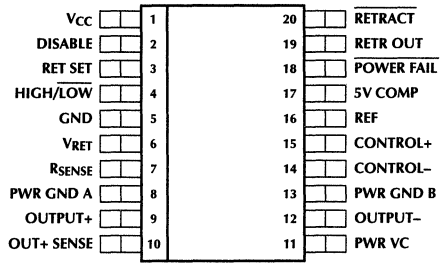
- 500mA power output with 1.3V total forward drop
- Low offsets, cross-over distortion and quiescent current
- Pin-programmable transconductance settings
- Retraction circuitry with programmable retract current, voltage limiting, and separate supply pin.
- On-chip precision power fail detect circuitry
- Over-temperature protection with flag output
- Logic input available for disabling outputs

BLOCK DIAGRAM



PIN CONNECTION

ML4506
20-PIN SOIC (S20W) OR 20-PIN SSOP (R20W)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	V_{CC}	Positive Power supply for the IC. Normally connected to +5V.
2	DISABLE	A logic "1" turns off the main outputs.
3	RET SET	A Current into this sets up the voltage limit for the internal retract sourcing circuit
4	HIGH/$\overline{\text{LOW}}$	A logic "1" sets the transconductance gain to 1/4 while a logic "0" sets the gain to 1/24. Transconductance gain is defined as: $\frac{V_{RSENSE}}{(\text{CONTROL}+)-(\text{CONTROL}-)}$
5	GND	Analog Signal Ground
6	V_{RET}	Power supply for the retract circuit.
7	R_{SENSE}	Current sensing resistor terminal.
8	PWR GND A	Ground Terminal for power amplifier A.
9	OUTPUT+	Positive Output terminal for bridge amplifier.
10	OUT+ SENSE	Positive Amplifier Kelvin sense terminal. Tie to OUTPUT+.
11	PWR VC	+5V supply for bridge amplifier
12	OUTPUT–	Negative Output terminal for bridge amplifier.
13	PWR GND B	Ground Terminal for power amplifier.
14	CONTROL–	Negative input for current command.
15	CONTROL+	Positive input for current command.
16	REF	Reference input to the Power Fail comparator. Leave open to use internal 2.5V reference.
17	5V COMP	Input to the Power Fail Comparator. Can be connected to a bypass capacitor for noise immunity.
18	$\overline{\text{POWER FAIL}}$	Open collector output drives low if pin 17 or pin 18 are below pin 16. Normally tied to pin 20.
19	RETR OUT	Open collector output pulls low to drive external PNP for retract if V_{CC} is less than 3.5V and pin 20 is low.
20	$\overline{\text{RETRACT}}$	A logic "0" input causes the main outputs to tri-state and the retraction circuit to activate. This input also functions as a flag output and will go low in the event of an over-temperature condition.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (pins 1,6,11) 7V
Voltage Pins 2,4,18,19,20 ..... –0.3V to +7V
Pins 14, 15 ..... –0.3 to +V_{CC}
Output Current ..... ±750mA
Retraction Current 80mA
Retract set current (pin 3) 3mA

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 150°C
Thermal Resistance (θ_{JA})
SOIC Package (S) ..... 55°C/W
SSOP Package (R) ..... 65°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
Supply Voltage (pins 1,11) ..... 5V ± 10%
V_{RET} (pin 6) ..... 1V to V_{CC}

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, V_{CC} = 5V ± 10%, R_{SENSE} = 1Ω, CONTROL– (pin 15) = 2.5V, R_{SET} (pin 3) = 3.7kΩ, Load = 10Ω.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
AMPLIFIER					
Control Common Mode Range		0.5		V_{CC} – 1	V
Offset				±10	mV
Transconductance Gain	pin 4 = 2V pin 4 = 0.8V	238 39.6	250 41.7	263 43.8	mA/V mA/V
Bandwidth			100		kHz
Sinking saturation	I_{OUT} = 100mA I_{OUT} = 300mA I_{OUT} = 500mA			0.5 0.6 0.8	V V V
Sourcing saturation	I_{OUT} = 100mA I_{OUT} = 300mA I_{OUT} = 500mA			1.1 1.2 1.3	V V V
RETRACTION CIRCUIT V_{PIN20} = 0.8V, V_{RET} = 2.5V					
I_{RET} SET			0.75		V
Turn on time			300		ns
Turn off time			8		µs
Sink current (I_{PIN12})	V_{PIN12} = 0.4V	34	50	150	mA
Source Voltage (V_{PIN7})	I_{PIN7} = –50mA	0.3	0.5	0.7	V
POWER FAIL DETECTION CIRCUIT					
Reference Voltage		1.35	1.50	1.65	V
Reference Source Impedance			2.25		kΩ
5V Threshold Hysteresis		4.40	4.575 30	4.75	V mV
LOGIC INPUTS					
Voltage High (V_{IH})		2	1.4		V
Voltage Low (V_{IL})			1.4	0.8	V
Current High (I_{IH})	V_{IN} = 5V			±10	mA
Current Low (I_{IL})	V_{IN} = 0V, except pin 20 V_{IN} = 0V, pin 20 only	–40 –250	–10 –160		mA mA
CURRENT CONSUMPTION					
Pin 1 + Pin 11	V_{PIN14} = V_{PIN15} = 2.5V		10	15	mA
Pin 6	V_{PIN14} = 2.5V		2.5	5.0	mA

5

FUNCTIONAL DESCRIPTION

POWER AMPLIFIER

The ML4506 power amplifier circuit is set up as a Howland Current source with a fixed gain of 1/4 or 1/24 (set by driving pin 4 high or low respectively). This architecture yields minimal cross-over distortion while maintaining low output cross conduction currents.

The gain figure refers to the ratio of input voltage to the output voltage seen across R_{SENSE}. For example, at a 1/4 gain setting, with V(–) input at 2.5V and the V(+) input at 3.5V, +500mA would flow through the coil using a 0.5Ω sense resistor. Under the same conditions with pin 4 low, the current would be 83mA. The ability to change from low to high gain allows more complete utilization of DAC resolution when in the track follow mode.

The output stage (figure 2) is designed to provide minimal saturation losses and employs a "composite PNP" for the sourcing drive and a saturable NPN to sink current. Sourcing saturation drop is typically 0.9V while sinking saturation drop is typically 0.4V.

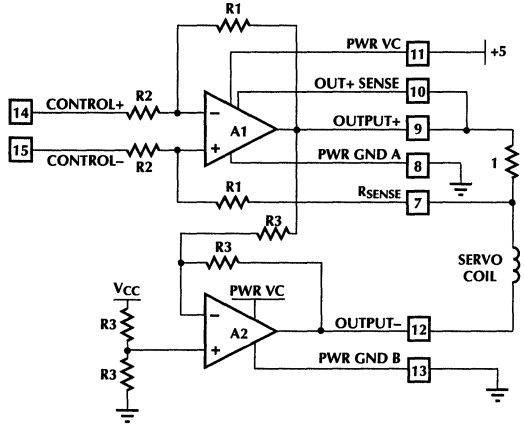


Figure 1. Power Amplifier Topology.

POWER FAIL DETECT

The ML4506 power fail detection circuit consists of a precision trimmed reference, resistor dividers, and a comparator with an effective hysteresis of 30mV. The output at pin 18 is open-collector and is normally tied to pin 1 which is internally pulled-up to 5V.

RETRACT

The retract circuit features provision for very low voltage operation as well as voltage limiting when a "live" retract with 5V on V_{RET} is performed. When pin 20 goes low, the internal NPN transistor will saturate, pulling SINK B (pin 11) low. A RETR OUT signal (open collector) saturates to drive an external PNP source transistor when pin 20 is low and when V_{RET} (pin 6) is below 3.5V. This portion of the circuit will function with less than 1V on V_{RET}.

An internal voltage limited pull-up circuit is provided which sources current on pin 7 to the VCM. This limit is set by an external resistor (see fig. 7) This circuit will operated reliably down to a V_{RET} voltage of around 2.5V. Pin 20 (Retract input) also serves as a flag to indicate an over-temperature condition on the die and goes low when the die temperature exceeds a safe operating limit (about 160°C).

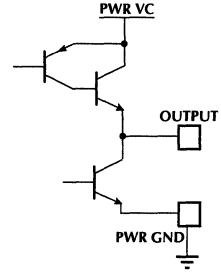


Figure 2. Power Output Stage.

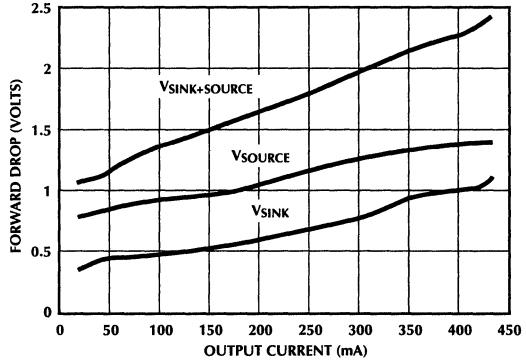


Figure 3. Output Saturation Voltage vs. Output Current. (V_{CC} = PWR VC = 5V)

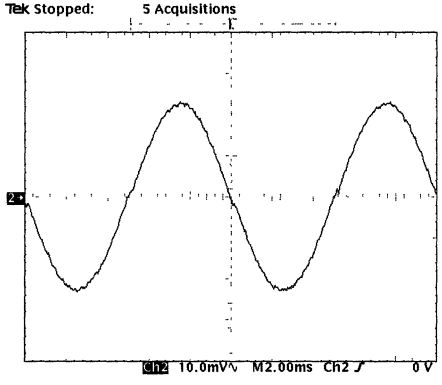


Figure 4. Output Current: V_{IN} = 100Hz Sine Wave, 100mA$_{P-P}$ Low Gain Mode ($V_{PIN\ 5}$ = 0), R_{SENSE} = 0.5Ω, R_L = 10Ω.

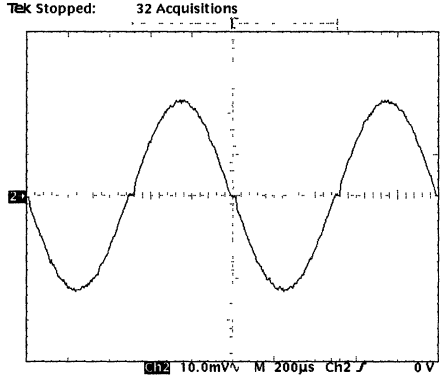


Figure 5. Output Current: V_{IN} = 1kHz Sine Wave, 100mA$_{P-P}$ Low Gain Mode ($V_{PIN\ 5}$ = 0), R_{SENSE} = 0.5Ω, R_L = 10Ω.

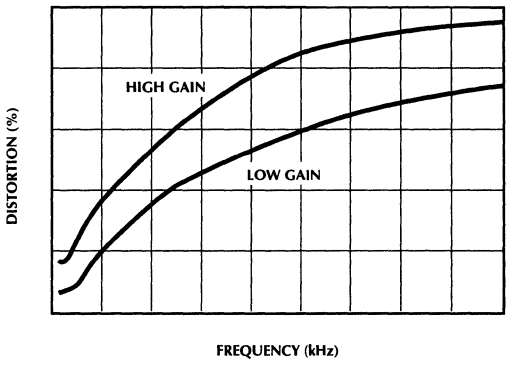


Figure 6. Total Harmonic Distortion vs. Frequency. Low Gain Setting (V_{PIN5} = 0), R_{SENSE} = 1Ω, V_{IN} = 2.4V$_{P-P}$ High Gain Setting (V_{PIN5} = 0), R_{SENSE} = 1Ω, V_{IN} = 0.4V$_{P-P}$

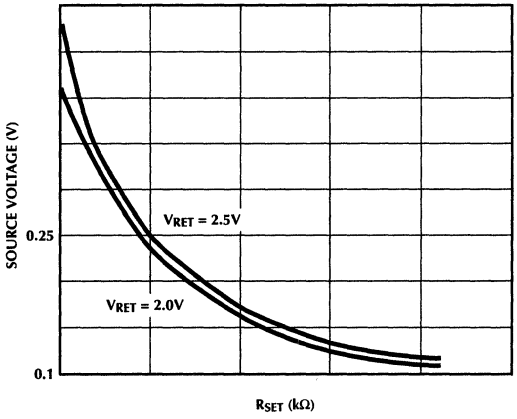


Figure 7. R_{SET} vs. Retract Source Voltage Limit.

APPLICATIONS

COMPENSATION

Figure 8 shows the equivalent AC circuit for the transconductance amplifier.

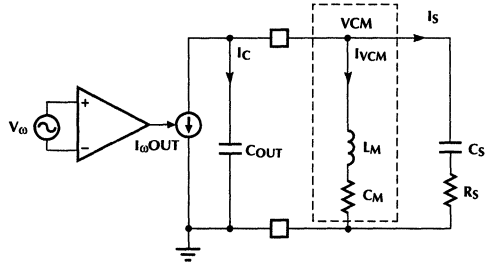


Figure 8. AC Equivalent Circuit for Current Amplifier, Voice Coil Motor (VCM) and Snubber.

The amplifier's current bandwidth is limited by C_{OUT} which varies with the value chosen for R_{SENSE}

$$C_{OUT} = \frac{25nF}{R_{SENSE}}$$

With no snubber (RS and CS) the bandwidth is limited to:

$$F_{-3dB} = \frac{1}{2\pi}\sqrt{\frac{2.414}{L(M)\ C(OUT)}}$$

Since this is a second order system with L(M) and C(OUT) forming a resonant circuit, some damping is desirable to reduce ringing in the step response. This is accomplished with resistive snubber. The optimum value of R(S) occurs when the following condition is met:

$$R(S) = \sqrt{\frac{L(VCM)}{C(OUT)}}$$

For a given C(S), setting R(S) to this value will minimize the ringing in the transient response. Larger values of R(S) will result in more ringing and more bandwidth. Smaller values of R(S) will result in more ringing and less bandwidth. R(S) should not exceed 300Ω.

C(S) (snubber capacitor) values of between 200nF and 1µF are usually necessary to acheive the desired reduction of ringing in the step response. At optimum value of R(S) larger values of C(S) further reduce the ringing but do not affect the bandwidth.

Tuning the current loop response can be best done simulating the network in figure 8 with a computer simulator (such as SPICE).

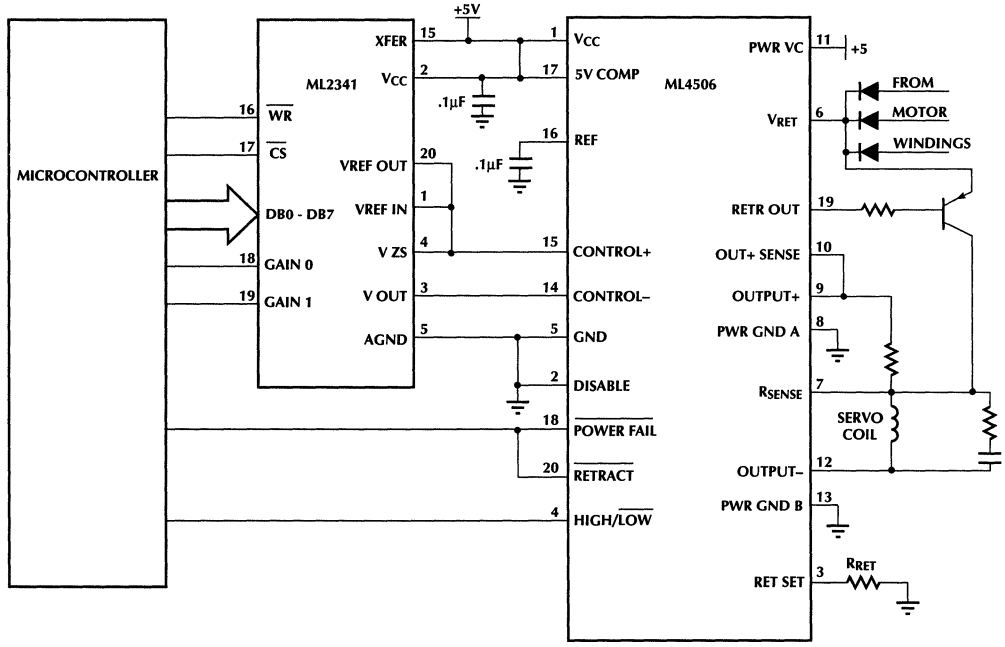


Figure 9. Typical Application: ML4506 used with ML2341 8-bit DAC provides up to 12-bit effective resolution.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4506CS	0°C to 70°C	20-Pin SOIC (S20W)
ML4506CR	0°C to 70°C	20-Pin SSOP (R20)

Low Voltage Drop Voice Coil Servo Driver

GENERAL DESCRIPTION

The ML4508 is a voice coil power driver intended for use in High Performance 5V Hard Disk servo systems. The ML4508 contains all control circuitry necessary to drive the voice coils of most small drives. To maximize compliance voltage, the ML4508 includes two 1-Amp (typical) NPN drivers and provides drivers for external PNP transistors. In addition, power fail detection and a low voltage head retraction functions are provided for orderly shut-down of the drive.

The transconductance is programmed by a logic input at 1/4 A/V and 1/24AV respectively, when using a 1Ω sense resistor. This allows for greater DAC resolution in digitally controlled servos during track follow without compromising dynamic range during seek.

The retraction circuit, main drive circuit, and control circuits are each powered from their own supplies. Retract allows the use of an external PNP retraction with as little as 1V of back EMF from the spindle.

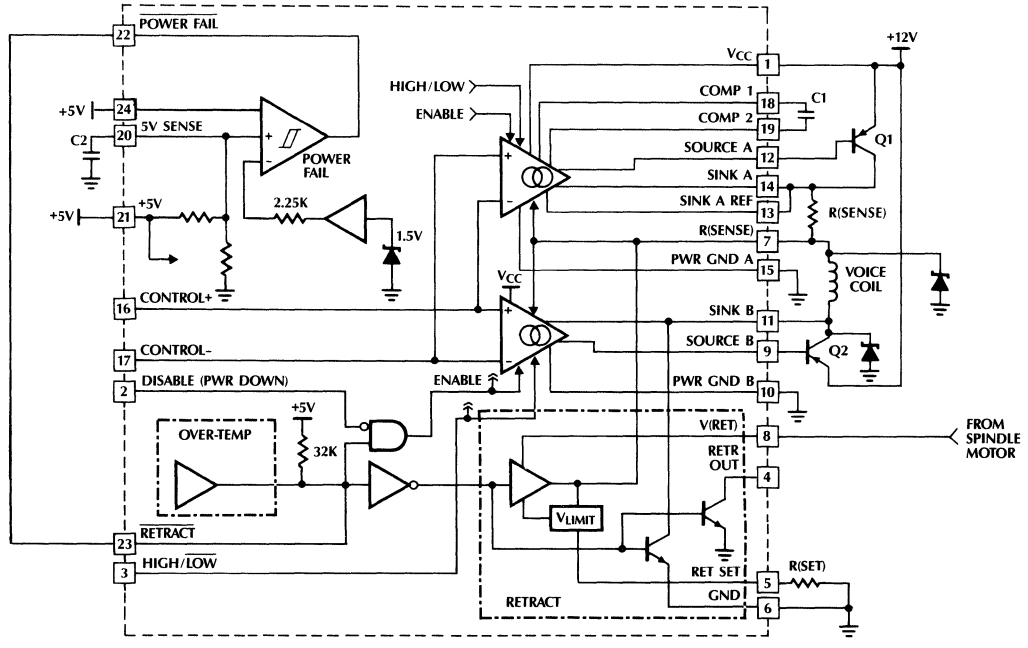
The power fail detection circuit includes a precision 1.5V bandgap reference and a power fail comparator.

The ML4508 is implemented using Micro Linear's bipolar array technology. This allows for customization of the IC for a user's specific application.

FEATURES

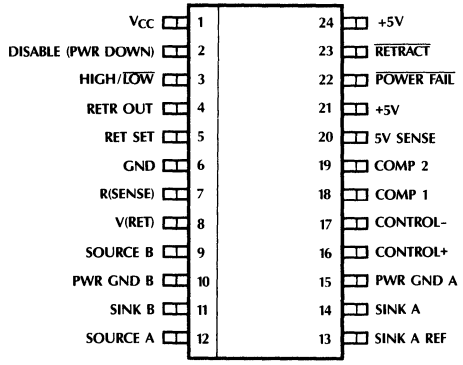
- Low saturation voltage (<1V at 1A typically)
- No cross-over distortion with low quiescent current
- Pin-programmable transconductance settings
- Retraction circuitry with programmable retract voltage and separate power pin
- On-chip precision power fail detect circuitry
- Over-temperature protection with flag output

BLOCK DIAGRAM



PIN CONNECTION

ML4508
24-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	V_{CC}	Supply input to power amplifiers.
2	DISABLE (PWR DOWN)	A Logic "1" puts the IC into a low power state and disables the power amplifiers.
3	HIGH/$\overline{\text{LOW}}$	A logic "1" sets the transconductance gain to 1/4 while a logic "0" sets the gain to 1/24. Transconductance gain is the $V_{RSENSE} \div V_{CONTROL}$.
4	RETR OUT	Open collector ouput which pulls low during retract. Used to drive external power transistor to source retract current to the coil and can provide a braking signal to spindle.
5	RET SET	External set resistor to establish a voltage limit for the internal retract driver.
6	GND	Analog signal ground.
7	R(SENSE)	Current sense resistor terminal.
8	V(RET)	Supply pin for retract circuits.
9	SOURCE B	PNP Base drive ouput for inverting power amplifier.
10	PWR GND B	Power return pin for inverting power amplifier. Normally used for current sensing.
11	SINK B	Current sinking ouput for inverting power amplifier. Connects to voice coil (–) terminal.
12	SOURCE A	PNP Base drive output for non-inverting power amplifier.
13	SINK A REF	Kelvin sensing point for power amplifier. Connect to SINK A.
14	SINK A	Current sinking output for non-inverting power amplifier. Connects to voice coil (+) terminal.
15	PWR GND A	Power return pin for non-inverting power amplifier. Normally used for current sensing.
16	CONTROL+	Positive input for current comand.
17	CONTROL–	Negative input for current command.
18	COMP 1	Pin for external compensation capacitor.
19	COMP 2	Pin for external compensation capacitor.
20	5V SENSE	Center node of a resistor divider from +5V.
21	+5V	Input for +5V for power fail detection and logic power supply.
22	$\overline{\text{POWER FAIL}}$	Open Collector output drives low for low voltage conditions.
23	$\overline{\text{RETRACT}}$	A logic "0" initiates retract. Also used as an open-collector over temperature output flag.
24	+5V	For power fail comparator.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (pins 1,8) 7V
Voltage Pins 2,3,23 ..... –0.3V to +7V
Pins 4, 7, 9, 11, 12, 13, 14, 16, 17, 22 ..... –0.3 to +V_{CC}
Output Sink Current ..... ±1A
Retraction Current 80mA
Retract Set current (pin 5) 3mA

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... 150°C
Thermal Resistance (θ_{JA}) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to +70°C
V_{CC} Supply Voltage ..... 4.5 to 5.5V
+5V (pin 21) Supply Voltage ..... 4.5 to 5.5V
V_{RET} (pin 8) Supply Voltage 2.5V
Control + Voltage Range (pin 15 = 5V) ..... 0V to V_{CC}
Control - Voltage Range ..... 2V to V_{CC} - 1.5V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, V_{CC} = Operating Range, R_{SENSE} = 1Ω, R_{COIL} = 15Ω, CONTROL– (pin 17) = $V_{CC/2}$, C1 = 30pF, Q1, Q2 = MJE210, R_{SET} = 3.7kΩ

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
AMPLIFIER					
Offset				±10	mA
Gain	Pin 5 = 2V	238	250	263	mA/V
	Pin 5 = 0.8V	39.6	41.7	43.8	mA/V
Bandwidth			100		KHz
Sinking Saturation	I_{OUT} = 100mA		0.1	0.6	V
	I_{OUT} = 300mA		0.2	0.8	V
	I_{OUT} = 500mA		0.3	1.0	V
Sourcing Saturation	I_{OUT} = 100mA		.1		V
	I_{OUT} = 300mA		.2		V
	I_{OUT} = 500mA		.3		V
Source A/B Base Drive		10		50	mA
Q1/Q2 Standby Current	$V_{PIN\ 16}$ = 5V		4		mA
RETRACTION CIRCUIT V					
I(RET) SET			.75		V
Turn On Time			800		ns
Turn Off Time			8		µs
Source Voltage	$V_{PIN\ 23}$ = 0.8V, $V_{PIN\ 8}$ = 3V, $I_{PIN\ 7}$ = 50mA	0.95	1.2	1.5	V
Sink Current	$V_{PIN\ 23}$ = 0.8V, $V_{PIN\ 8}$ = 1.2V, force 50mA into pin 11	10	37	1000	mV
RETR OUT V_{OL}	$V_{PIN\ 23}$ = 0.8V, $I_{PIN\ 4}$ = 1mA		0.1	0.4	V
POWER FAIL DETECTION CIRCUIT					
5V Threshold		4.40	4.575	4.75	V
Hysteresis — 5V Sense			30		mV

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, T_A = Operating Temperature Range, V_{CC} = Operating Range, R_{SENSE} = 1Ω, R_{COIL} = 15Ω, CONTROL– (pin 17) = $V_{CC/2}$, C1 = 30pF, Q1, q2 = MJE210, R_{SET} = 3.7kΩ

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
LOGIC INPUTS AND OUTPUTS					
Voltage High (V_{IH})		2	1.4		V
Voltage Low (V_{IL})			1.4	0.8	V
Current High (I_{IH})	V_{IN} = 5V			±10	µA
Current Low (I_{IL})	V_{IN} = 0V, except pin 23 V_{IN} = 0V, pin 23 only	–40 –250	–10 –160		µA µA
Voltage Low (pins 22, 23)	I_{OL} = 1mA			.4	V
OVER-TEMPERATURE DETECTION					
T_J Threshhold			160		°C
Hysteresis			30		°C
CURRENT CONSUMPTION					
Pin 21	Pin 21 = 5.5V		5	7	mA
Pin 1	V_{CC} = 5.5V, $V_{PIN\ 16}$ = $V_{CC/2}$		5	10	mA
Pin 8	$V_{PIN\ 8}$ = 5.5V, $V_{PIN\ 23}$ = 5V		3.5	5	mA

FUNCTIONAL DESCRIPTION

POWER AMPLIFIER

The ML4508 power amplifier circuit (figure 1) is set up as a Howland Current source with a fixed gain of 1/4 or 1/24 (set by driving pin 3 high or low respectively). This architecture yields minimal crossover distortion while maintaining low output cross conduction currents. The gain figure refers to the ratio of input voltage to the output voltage seen across R_{SENSE}. For example, at a 1/4 gain setting, with V(–) input at 2.5V and the V(+) input at 4.5V, +500mA would flow through the coil using a 1Ω sense resistor. Under the same conditions with pin 3 low, the current would be 83mA. If lower input voltage swings and higher currents are desired, the overall transconductance gain may be increased by using a lower value of sense resistor, however offset current will increase proportionally. The ability to change from low to high gain allows more complete utilization of DAC resolution when in the track follow mode.

The output stage is designed to provide minimal saturation losses and employs an external PNP transistor for the sourcing drive and an internal saturable NPN to sink current. Sinking saturation drop is typically under 0.4V. Sourcing saturation drop depends on the external transistors used.

Care should be taken to avoid drawing substrate currents due to negative excursions on any pin of the ML4508. Schoktty diodes should be included on both sides of the VCM to prevent negative excursions from forward biasing the substrate diodes on the IC.

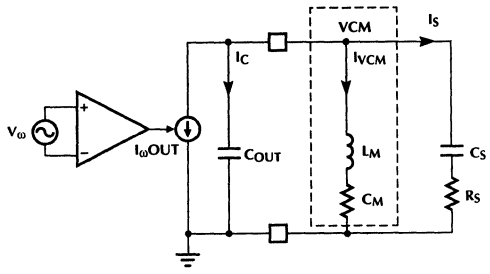


Figure 1. Simplified Power Amplifier Schematic (High Gain Mode)

Two areas should be considered to avoid high frequency oscillation in the output stage:

1. Choose external PNP transistors with a F_T of at least 50MHz.
2. An RC compensation network should be used to cancel the zero presented to the output by the L/R of the voice coil motor as shown in figure 2.

COMPENSATION

Figure 2 shows the equivalent AC circuit for the current amplifier.

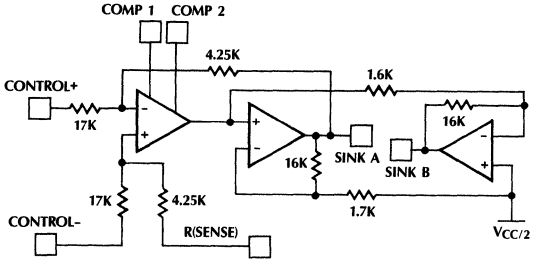


Figure 2. AC Equivalent Circuit for Current Amplifier, Voice Coil Motor (VCM) and Snubber.

The amplifier's current bandwidth is limited by C_{OUT} which varies with the value chosen for R_{SENSE}

$$C_{OUT} \approx \frac{1200 \times (C_{COMP} + 12.8pF)}{R_{SENSE}}$$

Where C_{COMP} is C1 between pins 18 and 19. With no snubber (R_S and C_S) the bandwidth is limited to

$$F_{-3dB} = \frac{1}{2\pi}\sqrt{\frac{1}{LC}}$$

Since this is a second order system with L(M) and C(OUT) forming a resonant circuit, some damping is desirable to reduce ringing in the step response. This is accomplished with a resistive snubber. The optimum value of R(S) occurs when the following condition is met:

$$R(S) = \sqrt{\frac{L(VCM)}{C(OUT)}}$$

For a given C(S), setting R(S) to this value will minimize the ringing in the transient response. Larger values of R(S) will result in more ringing and more bandwidth. Smaller values of R(S) will result in more ringing and less bandwidth. C(S) (snubber capacitor) values of between 200nF and 1mF are usually necessary to achieve the desired reduction of ringing in the step response. At the optimum value of R(S) larger values of C(S) further reduce the ringing but do not affect the bandwidth.

Timing the current loop response can be easily done simulating the network in figure 2 with a computer simulator (such as SPICE).

POWER FAIL DETECT CIRCUIT

The ML4508 circuit consists of a precision trimmed reference, resistor dividers and an "or function" comparator with hysteresis. The output (open collector) of this circuit appears on pin 22. When either comparator input (pins 20 and 24) falls below the 1.5V reference, pin 22 pulls low.

RETRACT CIRCUITS

When pin 23 goes low, pin 4 will pull low. The internal NPN transistor will saturate, pulling SINK B (pin 11) low. This portion of the circuit will function with less than 1V on V(RET). An internal voltage limited pull-up transistor is provided which sources current on pin 7 to the VCM. This circuit will be operated reliably down to a V(RET) voltage of around 2.5V.

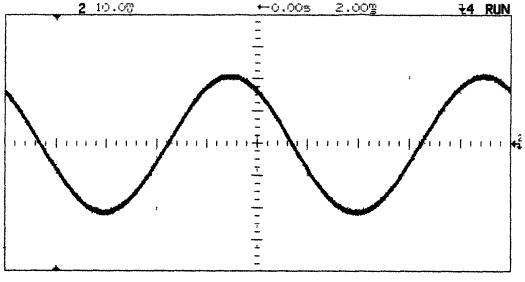


Figure 3. Output Current: V_{IN} = 100 Hz Sine Wave, $1V_{p-p}$ Low Gain Mode ($V_{PIN\ 3}$ = 0), R_{SENSE} = 1Ω

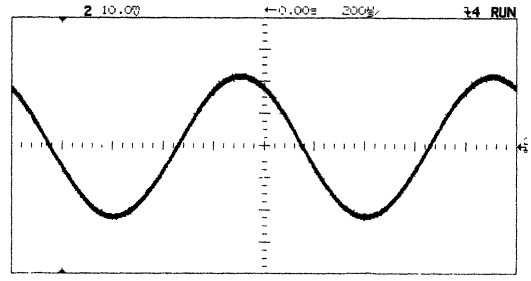


Figure 4. Output Current: V_{IN} = 1KHz Sine Wave, $1V_{P-P}$ Low Gain Mode ($V_{PIN\ 3}$ = 0), R_{SENSE} = 1Ω

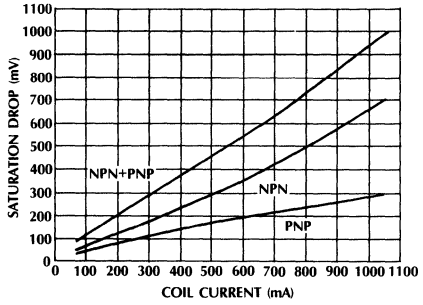


Figure 5. Output Saturation Voltage vs Output Current ($Q_1 = Q_2 = MJE210$)

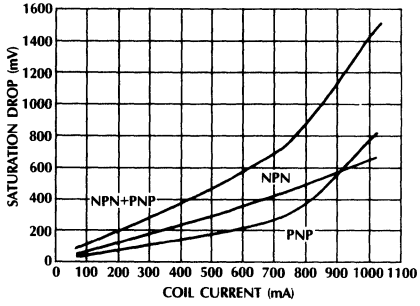


Figure 6. Output Saturation Voltage vs Output Current with BSR31 ($Q_1 = Q_2 = BSR31$)

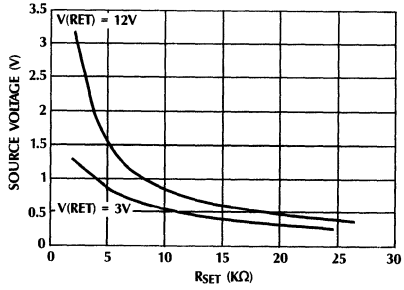


Figure 7. Retract Source Voltage Limit

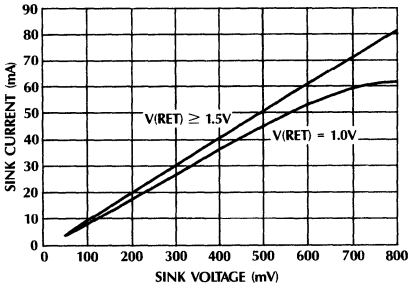


Figure 8. Retract Sink Voltage vs Current

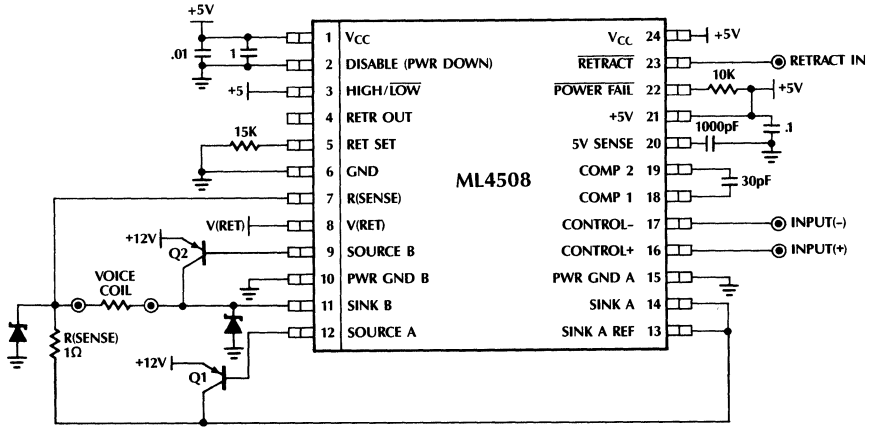


Figure 9. Typical 12V Application

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4508CS	0°C to +70°C	S20W

Micro Linear

ML4510

5V Sensorless Spindle Motor Controller

GENERAL DESCRIPTION

The ML4510 provides complete commutation for delta or wye wound Brushless DC (BLDC) motors without the need for signals from Hall Effect sensors. This IC senses the back EMF of the 3 motor windings (no neutral required) to determine the proper commutation phase angle using phase lock loop techniques. This technique will commutate virtually any 3-phase BLDC motor and is insensitive to PWM noise and motor snubbing.

Included in the ML4510 is the circuitry necessary for a Hard Disk Drive microcontroller driven control loop. The ML4510 controls motor current with either a constant off-time PWM or linear current control driven by the microcontroller. Speed feedback for the micro is a stable digital frequency equal to the commutation frequency of the motor. All commutation is performed by the ML4510. Braking and Power Fail are also included in the ML4510.

Since the timing of the start-up sequencing is determined by external circuitry, the system can be optimized for a wide range of motors and inertial loads.

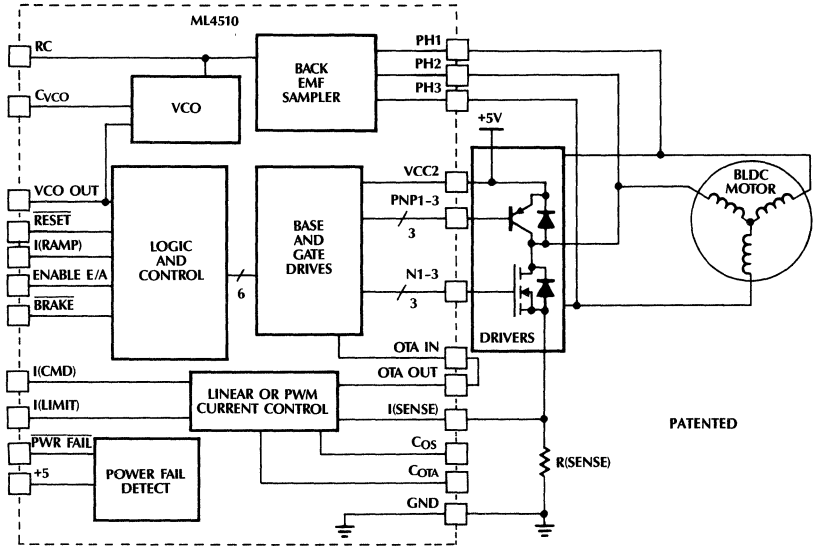
The ML4510 modulates the gates of external N-channel power MOSFETs to regulate the motor current. The IC drives external PNP transistors or P-channel MOSFETs directly. Special circuits are used to save base drive power at low load currents.

FEATURES

- Back-EMF Commutation Provides Maximum Torque for Minimum "Spin-Up" Time for Spindle Motors
- Accurate, Jitter-Free Phase Locked Motor Speed Feedback Output
- Operates on Single 5V Power Supply
- Linear or PWM Motor Current Control
- Easy Microcontroller Interface for Optimized Start-Up Sequencing and Speed Control
- Power Fail Detect Circuit
- Drives External N-Channel FETs and PNP's or P-Channel FETs

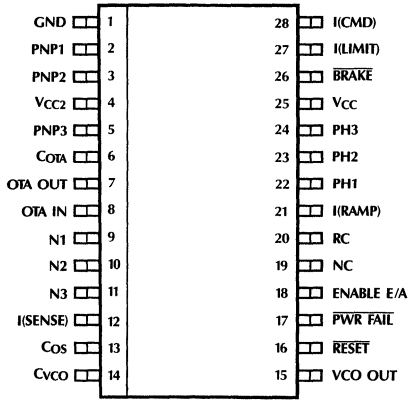
5

BLOCK DIAGRAM



PIN CONFIGURATION

ML4510
28-Pin SOIC (S28W)



PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	GND	Signal and Power Ground.
2	PNP1	Drives the external PNP power transistor driving motor PH1.
3	PNP2	Drives the external PNP power transistor driving motor PH2.
4	VCC2	5V power.
5	PNP3	Drives the external PNP power transistor driving motor PH3.
6	C_{OTA}	Compensation capacitor for linear motor current amplifier loop.
7	OTA OUT	Output of motor current error amplifier, normally connected to OTA IN or to external MOSFET gate.
8	OTA IN	Driving voltage for N1–N3. Normally tied to OTA OUT.
9–11	N1, N2, N3	Drives the external N-channel MOSFETs for PH1, PH2, PH3.
12	I(SENSE)	Motor current sense input.
13	C_{OS}	Timing capacitor for fixed off-time PWM current control.
14	C_{VCO}	Timing capacitor for VCO.
15	VCO OUT	Logic output from VCO.
16	$\overline{\text{RESET}}$	Input which holds the VCO off and sets the ML4510 to the RESET condition.
17	$\overline{\text{PWR FAIL}}$	A "0" output indicates 5V is under-voltage.
18	ENABLE E/A	A "1" logic input enables the error amplifier and closes the back-EMF feedback loop.
19	NC	No Electrical Connection.
20	RC	VCO loop filter components.
21	I(RAMP)	Current into this pin sets the initial acceleration rate of the VCO during start-up.
22	PH1	Motor Terminal 1.
23	PH2	Motor Terminal 2.
24	PH3	Motor Terminal 3.
25	VCC	5V power supply. Terminal which is sensed for power fail.
26	$\overline{\text{BRAKE}}$	A "0" activates the braking circuit.
27	I(LIMIT)	Sets the threshold for the PWM comparator.
28	I(CMD)	Current Command for Linear Current amplifier.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (pins 4, 25) 7V
Output Current (pins 2, 3, 5, 9, 10, 11) ..... ±150mA
Logic Inputs (pins 16, 18, 26) ..... –0.3 to 7V
I(SENSE) Voltage (pin 12) 0.9V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... 150°C
Thermal Resistance (θ_{JA}) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to +70°C
V_{CC} Voltage (pins 4, 25) ..... 5V ± 10%
I(RAMP) Current (pin 21) ..... 0 to 100μA
I Control Voltage Range (pins 27, 28) ..... 0V to 3V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, $V_{CC} = V_{CC2}$ = 5V, R_{SENSE} = 1Ω, $C_{OTA} = C_{VCO}$ = .01μF, C_{OS} = .02μF

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator (VCO) Section (Mode 1 or 2 unless otherwise specified)					
Frequency vs. $V_{PIN\ 20}$	$1V \leq V_{PIN\ 20} \leq 3.5V$		670		Hz/V
Frequency	V_{VCO} = 2.5V	830	1675	2500	Hz
	V_{VCO} = .5V	120	245	350	Hz
Reset Voltage at C_{VCO}	Mode = 0		125	250	mV
Sampling Amplifier					
V_{RC}	Mode 0		125	250	mV
I_{RC}	Mode 1, R_{RAMP} = 39KΩ	16	33	50	μA
	Mode 2A, V_{PH2} = 0.5V	30	60	90	μA
	Mode 2A, V_{PH2} = 2.5V	–6	2	6	μA
	Mode 2A, V_{PH2} = 4.5V	–30	–60	–90	μA
Motor Current Control Section					
I(SENSE) Gain	$V_{PIN\ 27}$ = 5V, $0V \leq V_{PIN\ 28} \leq 2.5V$	4	5	6	V/V
One Shot Off Time		12	25	33	μs
I(CMD) Transconductance Gain			.19		mmho
Power Fail Detection Circuit					
5V Threshold		3.8	4.25	4.5	V
Hysteresis			70		mV
Logic Inputs					
Voltage High (V_{IH})		2			V
Voltage Low (V_{IL})				.8	V
Current High (I_{IH})	V_{IN} = 2.7V	–10	1	10	μA
Current Low (I_{IL})	V_{IN} = 0.4V	–250	–120	–60	μA

5

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, T_A = Operating Temperature Range, V_{CC} = V_{CC2} = 5V, R_{SENSE} = 1Ω, C_{OTA} = C_{VCO} = .01μF, C_{OS} = .02μF

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Outputs	I(CMD) = I(LIMIT) = 2.5V				
I_{PNP} Low		50	75	100	mA
I_{PNP} High	Off State	-100		100	μA
V_N High	$V_{PIN\ 8}$ = 0.5V	2.4	3.1	3.8	V
V_N Low			.2	.7	V
A_V Pin 8 to V_N	$V_{PIN\ 8}$ = 0.5V	-3.0	-3.75	-4.5	V/V
LOGIC Low	I_{OUT} = 0.5mA			.4	V
LOGIC I_{OUT} High			5		μA
Supply Currents	(N and PNP Outputs Open)		I_{LMT} = 2.5V	I_{CMD} = 0V	
V_{CC} Current (Pin 25)			28	40	mA
V_{CC2} Current (Pin 4)			2	5	mA

FUNCTIONAL DESCRIPTION

The ML4510 provides closed-loop commutation for 3-phase brushless motors. To accomplish this task, a VCO, Integrating Back-EMF Sampling error amplifier and sequencer form a phase-locked loop, locking the VCO to the back-EMF of the motor. The IC also contains circuitry to control motor current with either linear or constant off-time PWM modes. Braking and power fail detection functions are also provided on chip. The ML4510 is designed to drive external power transistors (N-channel MOSFET sinking transistors and PNP sourcing transistors) directly, and contains a special circuit to reduce PNP base currents when output current demand is reduced.

Start-up sequencing and motor speed control are accomplished by a microcontroller. Speed sensing is accomplished by monitoring the output of the VCO, which will be a signal which is phased-locked to the commutation frequency of the motor.

BACK-EMF SENSING AND COMMUTATOR

The ML4510 contains a patented back-EMF sensing circuit which samples the phase which is not energized (Shaded area in figure 2) to determine whether to increase or decrease the commutator (VCO) frequency. A late commutation causes the error amplifier to charge the filter (RC) on pin 20, increasing the VCO input while early commutation causes pin 20 discharge. Analog speed control loops can use pin 20 as a speed feedback voltage.

The input impedance of the three PH inputs is about 8KΩ to GND. When operating with a higher voltage motor, the PH inputs should be divided down in voltage so that the maximum voltage at any PH input does not exceed VCC. See ML4411 data sheet for applications.

VCO AND PHASE DETECTOR CALCULATIONS

The VCO should be set so that at the maximum frequency of operation (the running speed of the motor) the VCO

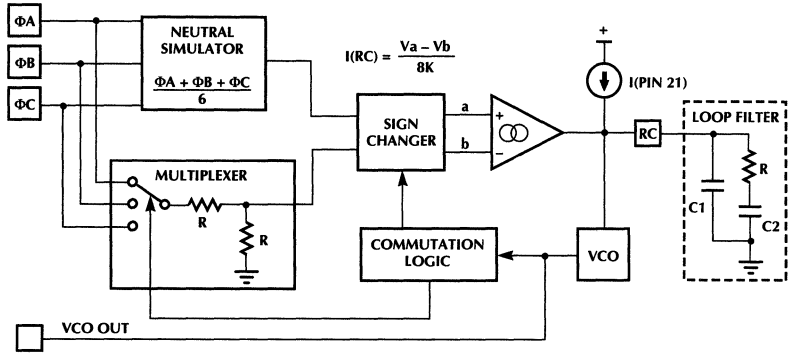


Figure 1. Back EMF Sensing Block Diagram.

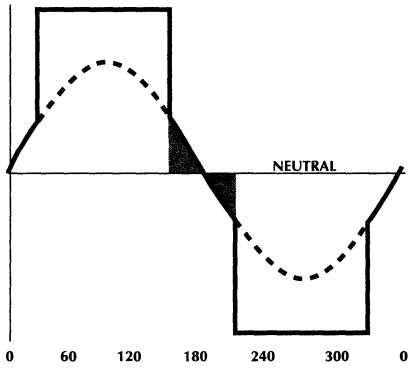


Figure 2. Typical Motor Phase Waveform with Back-EMF Superimposed (Ideal Commutation).

control voltage will be no higher than VCC_{MIN} – 1V. The VCO maximum frequency will be:

$$F_{MAX} = 0.05 \times POLES \times RPM$$

where POLES is the number of poles on the motor and RPM is the maximum motor speed in Revolutions Per Minute.

The minimum VCO gain derived from the specification table (using the minimum F_{VCO} at V_{VCO} = 2.5V) is:

$$K_{VCO(MIN)} = \frac{3.32 \times 10^{-6}}{C_{VCO}}$$

Assuming that the $V_{VCO(MAX)}$ = 3.2V, then

$$C_{VCO} = \frac{3.2 \times 3.32 \times 10^{-6}}{F_{MAX}}$$

or

$$C_{VCO} = \frac{212}{POLES \times RPM}\ \mu F$$

Figure 3 shows the transfer function of the Phase Lock Loop with the phase detector formed from the sampled phase through the Gm amplifier with the loop filtered formed by R, C_1, and C_2.

The impedance of the loop filter is

$$Z_{RC}(s) = \frac{1}{C_1 s} \frac{(s + \omega_{LEAD})}{(s + \omega_{LAG})}$$

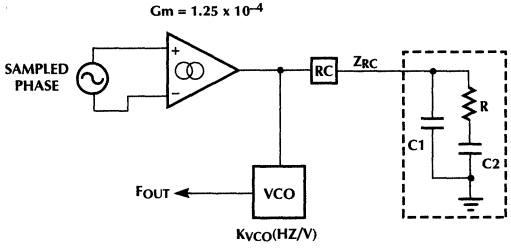


Figure 3. Back EMF Phase Lock Loop Components.

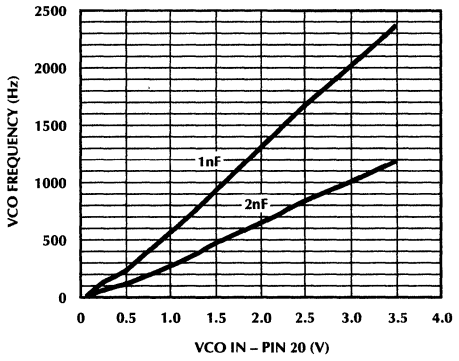


Figure 4. VCO Output Frequency vs. V_{VCO} (Pin 20)

Where the lead and lag frequencies are set by:

$$\omega_{LEAD} = \frac{1}{R C_2}$$

$$\omega_{LAG} = \frac{C_1 + C_2}{R C_1 C_2}$$

Requiring the loop to settle in 20 PLL cycles with a spread of 10 between $\omega_{LEAD} = 10 \times \omega_{LAG}$ produces the following calculations for R, C_1 and C_2:

$$C_1 \approx \frac{1.97 \times 10^{-9}}{C_{VCO} \times F_{VCO}^2}$$

$$C_2 = 9 \times C_1$$

$$R = \frac{12.65}{C_2 \times F_{VCO}}$$

START-UP SEQUENCING

When the motor is intitially at rest, it is generating no back-EMF. Because a back-EMF signal is required for closed loop commutation, the motor must be started "open-loop" until a velocity sufficient to generate some back-EMF is attained (around 100 RPM).

Two modes are possible for starting the motor. For the lowest possible starting time, the chip is held in the reset (mode R) state by holding pin 16 low and providing full current to the motor (figure 5).

Step	Pin 16	Pin 18	Pin 21	I(LIMIT) I(CMD)
1	0	0	Fixed	I_{MAX}
2	1	0	Fixed	I_{MAX}
3	1	1	0	I_{MAX}

Figure 5. Minimum Time Start-Up Sequence.

Step 1: The IC is held in reset (mode R) with full power applied to the windings (see figure 7). This aligns the rotor to a position which is 30° (electrical) before the center of the first commutation state.

Step 2: A fixed current is input to pin 21 and appears as a current on pin 20, and will accelerate the motor at a fixed rate.

Step 3: When the motor speed reaches about 100 RPM, the back-EMF loop can be closed by pulling pin 18 low.

Using this technique, some reverse rotation is possible. The maximum amount of reverse rotation is 360/N, where N is the number of poles. For an 8 pole motor, 45° reverse rotation is possible.

STATE	OUTPUTS						INPUT SAMPLING
	N1	N2	N3	PNP1	PNP2	PNP3	
R or 0	OFF	ON	OFF	ON	OFF	ON	N/A
A	OFF	OFF	ON	ON	OFF	OFF	PH2
B	OFF	OFF	ON	OFF	ON	OFF	PH1
C	ON	OFF	OFF	OFF	ON	OFF	PH3
D	ON	OFF	OFF	OFF	OFF	ON	PH2
E	OFF	ON	OFF	OFF	OFF	ON	PH1
F	OFF	ON	OFF	ON	OFF	OFF	PH3

Figure 6. Commutation State Table.

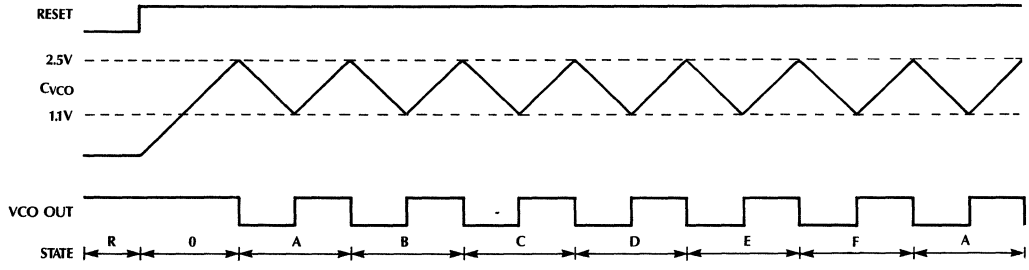


Figure 7. Start-Up Timing and Mode Sequencing.

SPEED CONTROL — CURRENT LOOP

To facilitate speed control, the ML4510 includes two current control loops — linear and PWM (figure 8). The linear control loop senses the motor current on the I(SENSE) terminal through R_{SENSE}. An internal current sense amplifier's output modulates the gates of the 3 N-channel MOSFET's when OTA OUT is tied to OTA IN, or can modulate a single MOSFET gate to control current.

The ML4510 also includes a current mode constant off-time PWM circuit. When motor current builds to the threshold set on I(LIMIT) input (pin 27), a one-shot is fired whose timing is set by C_{OS}. The current in the motor will be controlled by the lower of pin 27 and pin 28.

OUTPUT DRIVERS

The motor's source transistor drivers are open-collector NPN's with internal 8KΩ pull-up resistors, whose current is controlled according to the current demanded through the motor. To conserve power, the ML4510 sets the current to PNP1, PNP2, and PNP3, proportional to the lower of pin 27 and pin 28.

Drivers N1 through N3 are totem-pole outputs capable of sourcing and sinking 10mA. Switching noise in the external MOSFETs can be reduced by adding resistance in series with the gates.

BRAKING

Applying a logic 0 on pin 26 activates the braking circuit. The brake circuit turns on PNP1 through PNP3 and turns off NPN1 through NPN3.

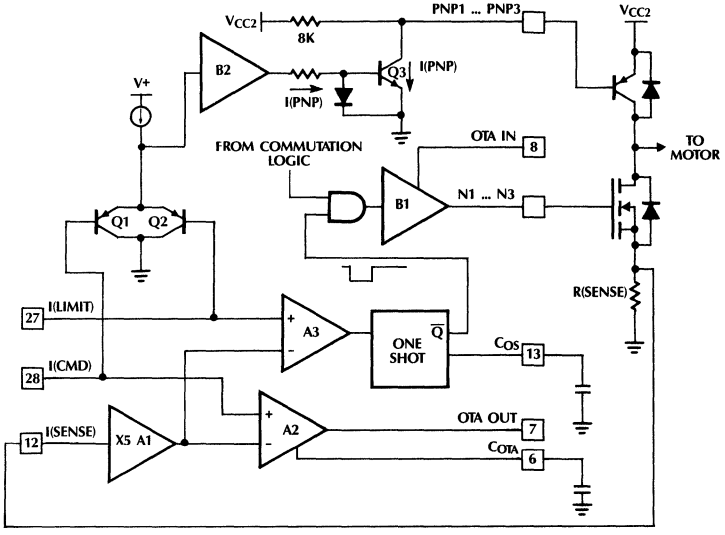


Figure 8. Current Control and Output Drive.

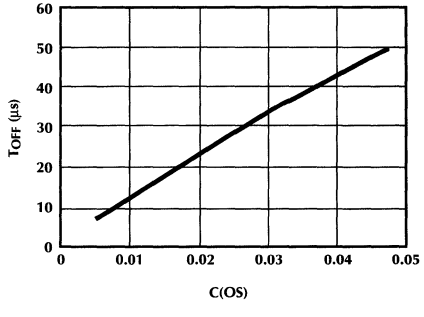


Figure 9. I(LIMIT) Output Off-Time vs. C_{OS}.

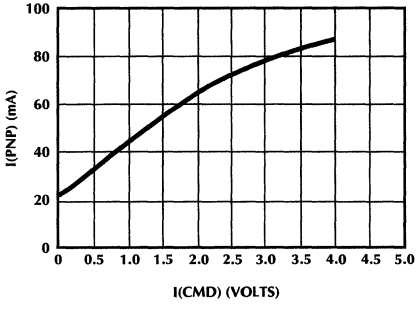


Figure 10. Available PNP Drive Current vs. I(CMD) Input.

APPLICATIONS

Figure 11 shows a typical application of the ML4510 in a hard disk drive spindle control. Although the timing necessary to start the motor in most applications would be generated by a microcontroller, Figure 12 shows a simple "one-shot" start-up timing approach.

Speed control can be accomplished either by:

1. Sensing the VCO OUT frequency with a Microcontroller and adjusting I(CMD) via an analog output from the Micro (PWM DAC).
2. Using analog circuitry for speed control (Figure 13).

Q1, Q2, and Q3 are MJE210 or equivalent. Q4, Q5, and Q6 are IRFU010 or equivalent. Base resistors (50Ω) are included to reduce power dissipation in the IC during start-up. If requested currents are low, these can be eliminated. Switching transients due to commutation can be reduced by increasing the 470Ω gate resistors on Q4-Q6.

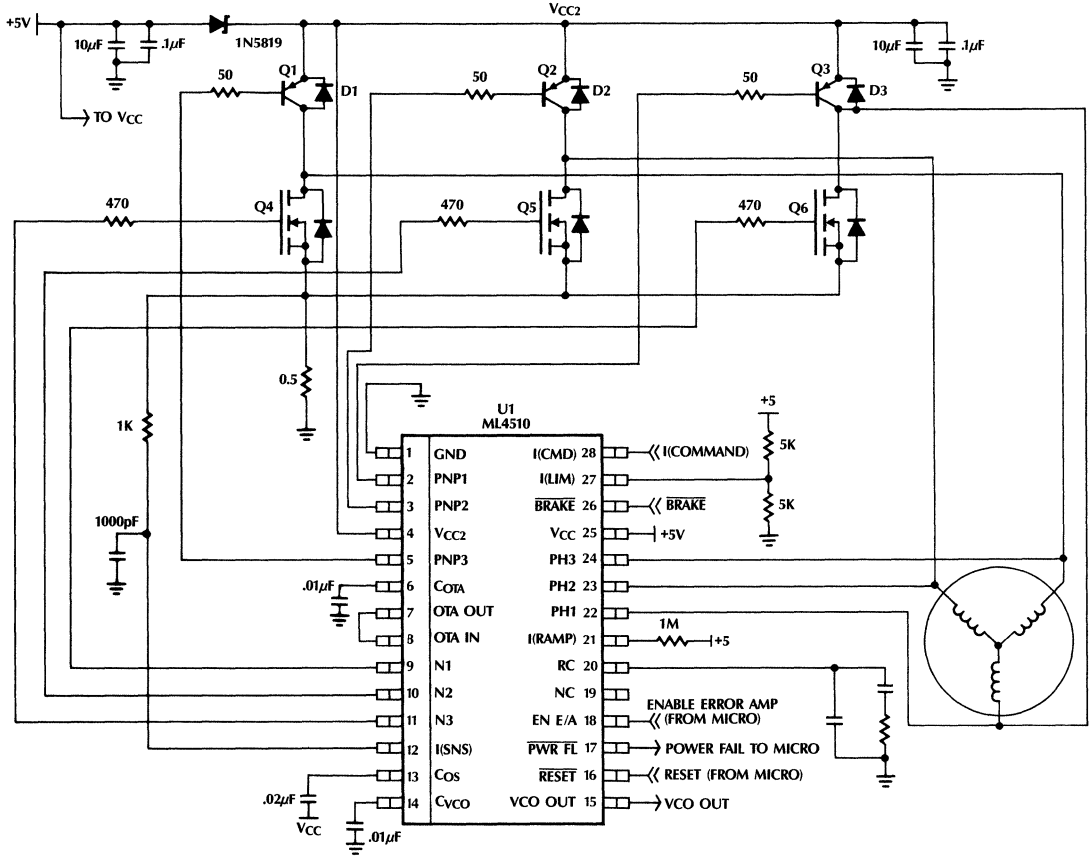


Figure 11. ML4510 Typical Application.

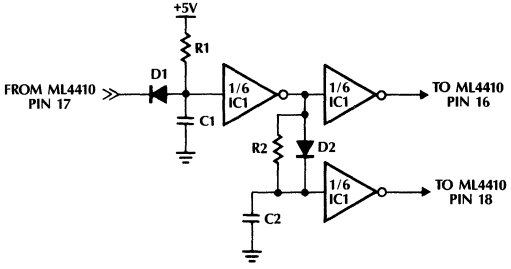


Figure 12. Analog Start-up Circuit.

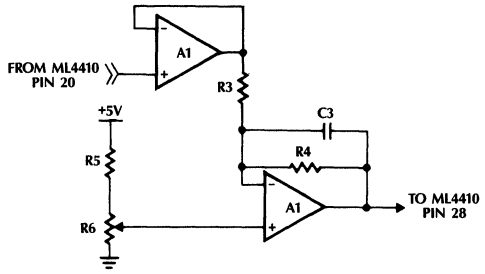


Figure 13. Analog Speed Control.

Symbol	Value
A1	LM358
Q1	74HC14
D1, D2	1N4148
R1	1MΩ
R2	1MΩ
R3	100KΩ

Symbol	Value
R4	100KΩ
R5	50KΩ
R6	50KΩ
C1	3.3μF
C2	3.3μF
C3	.47μF

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ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4510CS	0°C to +70°C	28-Pin SOIC (S28W)

Micro Linear

ML4532, ML4533, ML4536

Servo Burst Area Detector

GENERAL DESCRIPTION

The ML4532 and ML4533 Area Detectors are designed to minimize the pipeline transport delay while accurately quantizing the area of servo bursts in high-speed embedded servo systems. Combined with the ML2261 or ML2264 High Speed A/D Converters, the ML4532 and ML4533 are designed to capture back-to-back servo bursts in a 700ns or larger window. Power dissipation is minimized by the use of a digital power down pin which allows the area detector to be powered down between the servo sectors. The ML4536 is the ML4533 with different reference voltage levels.

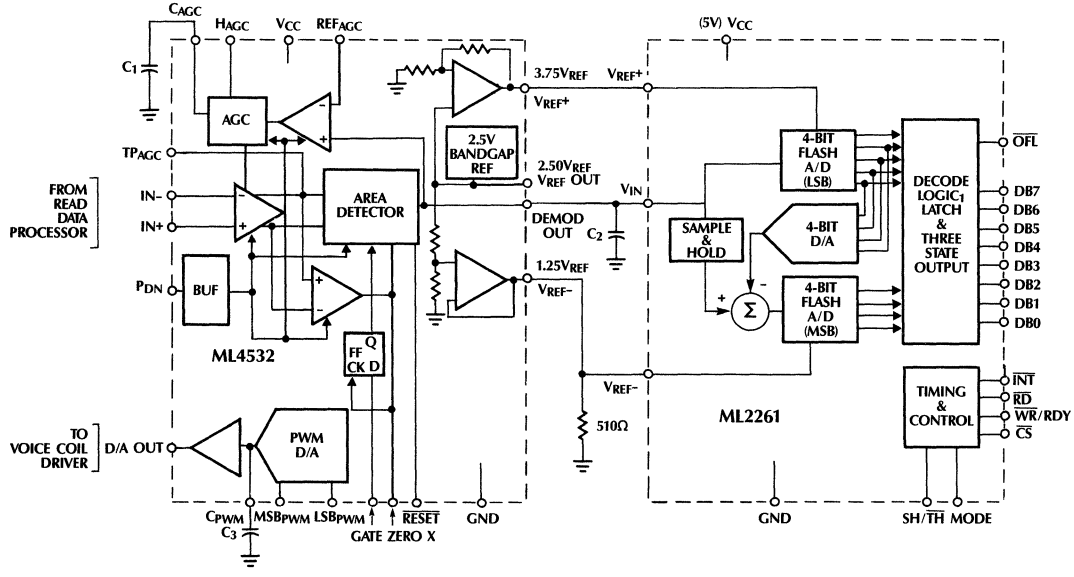
The ML4532 includes a PWM D/A for microprocessor control of the actuator driver, changing the REF_{AGC} pin voltage during head change, or other system control functions.

FEATURES	ML4532	ML4533	ML4536
Package Options	20-Pin PCC or SSOP	16-Pin SOIC	16-Pin SOIC
Zero-Scale Ref. Output Voltage	1.25V	1.25V	1.0V
Full-Scale Ref. Output Voltage	3.75V	3.75V	3.4V
Reference Output Voltage	2.5V	2.5V	2.2V
PWM D/A Onboard	Yes	No	No

FEATURES

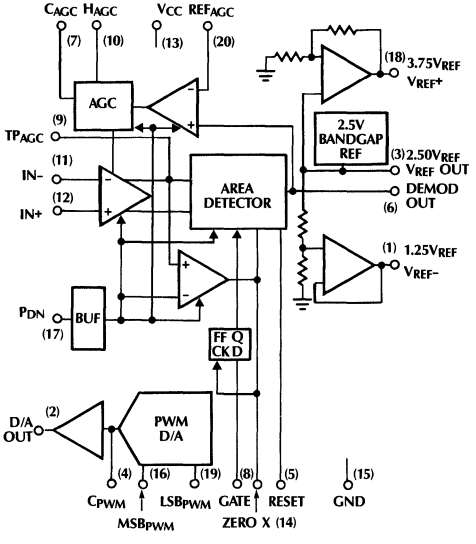
- Allows for Area Detection of 1μs back-to-back bursts
- AGC amplifier for maintaining accuracy
- 0.2% nonlinearity between 25% and 75% of input signal range
- 2% nonlinearity over the input signal range
- Provides zero- and full-scale outputs for A/D converter
- 5V supply, at 29mA for ML4533/ML4536, 35mA for ML4532
- Digitally controlled power down for minimizing power between sectors
- Bandgap Reference output
- ML4532 includes PWM D/A for controlling voice coil driver or AGC during head change
- ML4533/ML4536 available in 16-pin SOIC package ML4532 available in 20-pin PCC or SSOP package
- Reference outputs defining the minimum and maximum demodulation output values

TYPICAL APPLICATION

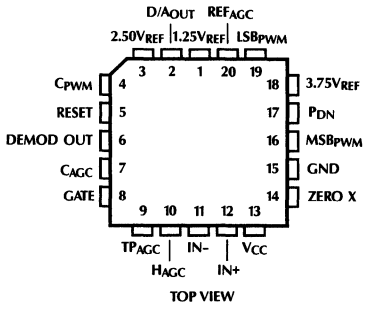


Typical HDD Digital Servo Application

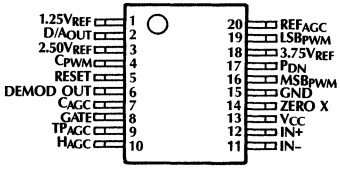
ML4532 BLOCK DIAGRAM AND PIN CONNECTION



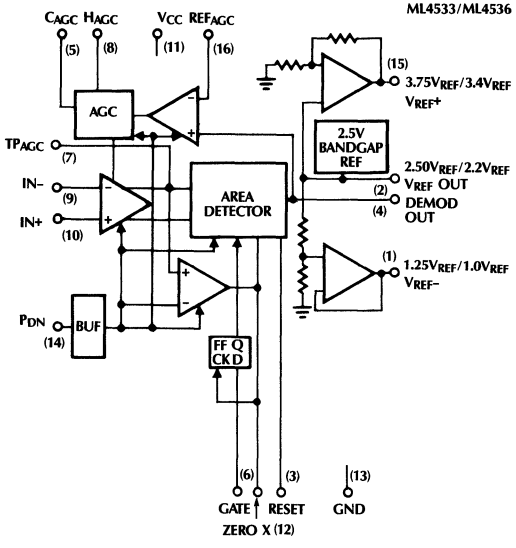
20-Pin PCC



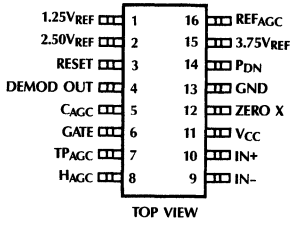
20-Pin SSOP



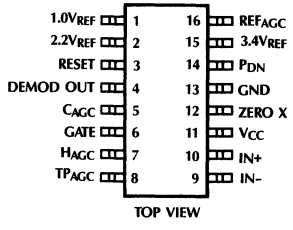
ML4533/ML4536 BLOCK DIAGRAM AND PIN CONNECTION



16-Pin SOIC (ML4533)



16-Pin SOIC (ML4536)



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PIN DESCRIPTION

ML4532 PIN #	ML4533/ ML4536 PIN #	NAME	DESCRIPTION
1	1	$1.25V_{REF}$/ $1.00V_{REF}$	Zero scale reference output.
2		D/A_{OUT}	Analog output of PWM D/A.
3	2	$2.50V_{REF}$ $2.20V_{REF}$	2.50 voltage reference output.
4		C_{PWM}	PWM D/A smoothing capacitor.
5	3	RESET	Reset, active high.
6	4	DEMOD OUT	Area detector output.
7	5	C_{AGC}	AGC capacitor.
8	6	GATE	Defines area detect window, active high.
9	7	TP_{AGC}	Output test point for AGC.
10	8	H_{AGC}	AGC hold input, AGC active when high; AGC constant when low.
11	9	IN–	Negative input.
12	10	IN+	Positive input.
13	11	V_{CC}	5V power supply.
14	12	ZERO X	Zero detector crossing output.
15	13	GND	Ground.
16		MSB_{PWM}	PWM D/A most significant bit input.
17	14	P_{DN}	Power down control, reduces power if logic high.
18	15	$3.75V_{REF}$ $3.40V_{REF}$	Full scale reference output.
19		LSB_{PWM}	PWM D/A least significant bit input.
20	16	REF_{AGC}	AGC voltage reference.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage, V_{CC} 8V
Input Voltage ..... –0.3V to +8V
Storage Temperature ..... –65°C to +150°C
Package Dissipation at T_A = 25°C (Board Mount)
20-Pin PCC 875mW
20-Pin SSOP 750mW
16-Pin SOIC 750mW
Package Lead Temperature
Soldering (10 sec) ..... 260°C
Vapor Phase (60 sec) ..... 215°C
Infrared (15 sec) ..... 220°C

OPERATING CONDITIONS

Temperature Range ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... 5V ± 5%
$(I_{IN+}) - (I_{IN-})$ ..... $1V_{P-P}$
C_{AGC} 100pF
REF_{AGC} 2.5V
C_{PWM} ..... .01µF
C_H at DEMOD OUT 100pF

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, and external component values as recommended above, unless otherwise specified.

PARAMETER	NOTES	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
DEMODULATOR						
Differential Input Range	3	For Full Scale Output	.25		2	V_{P-P}
Differential AGC Range	3		0.8		1.5	V/V
Differential Input Resistance				4		kΩ
Differential Input Capacitance				5		pF
Common Mode Input Resistance				2		kΩ
Power Supply RR				40		dB
Differential Nonlinearity	5, 3 5, 4	25% to 75% of Full Scale Zero to Full Scale		.2 2	2 5	% %
DEMOD OUT Offset Current		V_{IN} = ±500mV			20	µA
Maximum DEMOD OUT Charge Current	3	GATE = High	500			µA
DEMOD OUT Leakage Current	3	GATE = Low			+5	µA
DEMOD OUT Reset Voltage (ML4532/33) (ML4536)			1.15 0.9	1.25 1.0	1.35 1.1	V V
DEMOD OUT Reset Current		Discharge, RESET = High	2.0			mA
AUTOMATIC GAIN CONTROL						
AGC Dynamic Range	3		2.5			V/V
AGC Output Swing	3		1			V
C_{AGC} Charging Current	3		150		250	µA
C_{AGC} Discharging Current	3		150		250	µA
C_{AGC} Leakage Current	3				5	µA
VOLTAGE REFERENCES						
1.25V_{REF} Output Voltage (ML4532/33)	3	T_A = 25°C	1.20	1.25	1.30	V
3.75V_{REF} Output Voltage (ML4532/33)	3	T_A = 25°C	3.60	3.75	3.90	V
2.50V_{REF} Output Voltage (ML4532/33)	3	T_A = 25°C	2.40	2.50	2.60	V
1.0V_{REF} Output Voltage (ML4536)	3	T_A = 25°C	0.95	1.0	1.05	V
3.4V_{REF} Output Voltage (ML4536)	3	T_A = 25°C	3.2	3.4	3.6	V
2.2V_{REF} Output Voltage (ML4536)	3	T_A = 25°C	2.05	2.2	2.35	V
Load Regulation	3	0mA ≤ I_{OUT} ≤ 5mA	–5		+5	mV/mA
Line Regulation			–30		+30	mV/V
DIGITAL AND DC						
Logical "0" Input Voltage	3				.8	V
Logical "1" Input Voltage	3		2.0			V
Logical "0" Input Current	3	V_{IN} = 0.4V			–1.5	mA
Logical "1" Input Current	3	V_{IN} = 2.5V			+100	µA
Logical "0" Output Voltage	3	ZERO X, I_{OUT} = 1mA			.5	V
Logical "1" Output Voltage	3	I_{OUT} = –1mA	3.0			V
Supply Current ML4532 ML4533/ML4536	3 3 3 3	P_{DN} = Low P_{DN} = High P_{DN} = Low P_{DN} = High		 11 5	45 15 38 12	mA mA mA mA
Monotonicity	4		9	10		Bits
LSB to MSB Ratio	3		16.0	16.5	18.0	V/V

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, and external component values as recommended above, unless otherwise specified.

PARAMETER	NOTES	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
D/A CONVERTER (ML4532 Only)						
Output Voltage Swing	3	R_L = 5K	1.25		3.75	V
Logical "0" Input Voltage	3				.8	V
Logical "1" Input Voltage	3		2.0			V
Logical "0" Input Current	3	V_{IL} = .4V			-1	mA
Logical "1" Input Current	3	V_{IH} = 2.5V			300	μA
DYNAMIC AND AC PARAMETERS (Figures 1 and 2)						
f_B, Burst Input Frequency	4		1		10	MHz
t_{GS}, Gate Edge Setup Prior to Burst ↓ Zero Crossing	4, 6				30	ns
t_{RESET}, Reset Pulse Width	4, 6	$C_H \leq$ 200pF	300			ns
t_{BZX}, Burst Zero Crossing to ZERO X Output	4, 6	C_L = 50pF			25	ns
t_{PG}, Power Down ↓ to Gate ↑	4, 5			200	400	ns

Note 1: Absolute Maximum Ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Typicals are parametric norm at 25°C.
Note 3: Parameter guaranteed and 100% production tested.
Note 4: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.
Note 5: Linearity measured as a percentage of the midpoint between 25% to 75% of full scale.
Note 6: Timing measured at 1.4V.

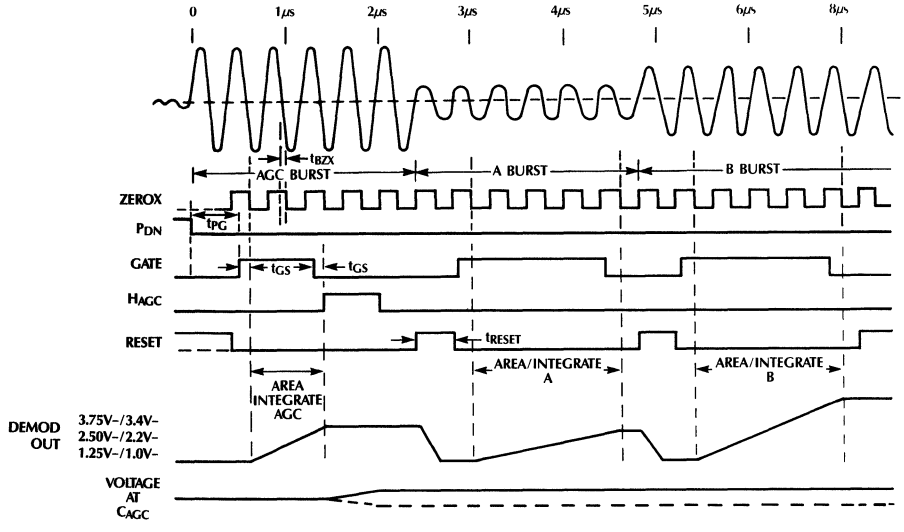

Figure 1. AGC Burst Timing

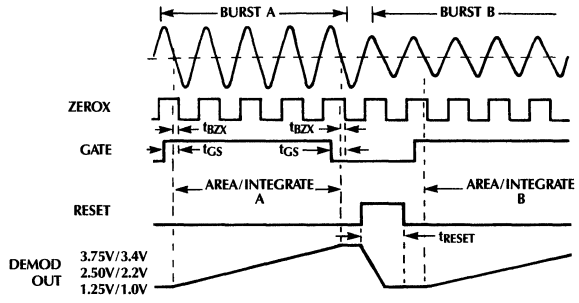

Figure 2. Burst Area Detect Timing

TYPICAL PERFORMANCE CURVES

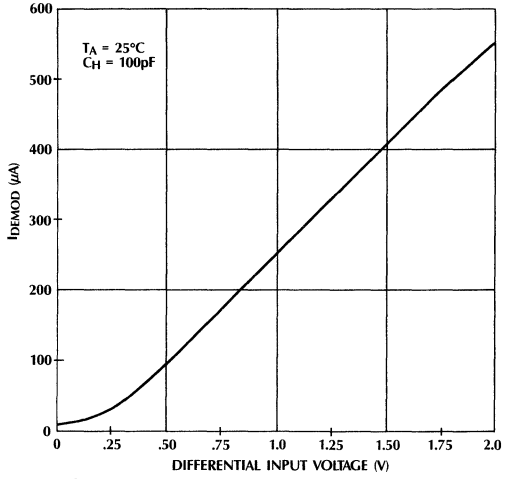

Figure 3. DEMOD Output Current vs. Input

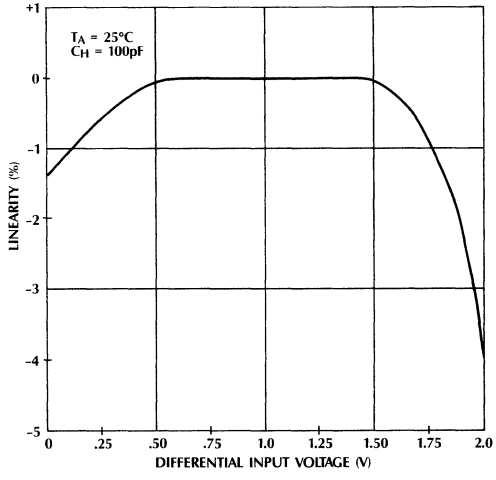

Figure 4. Linearity vs. Input

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1.0 FUNCTIONAL DESCRIPTION

The ML4532, ML4533 and ML4536 are composed of an AGC amplifier, an area detector, and a band-gap reference with three buffered outputs. In addition the ML4532 (see Figure 5) includes a pulse width modulation D/A. The ML4536 is essentially the ML4533 with a different set of reference voltages.

1.1 INPUT AMPLIFIER AND AUTOMATIC GAIN CONTROL

The inputs of the ML4532, ML4533 and ML4536 are intended for use at the output of the read channel filter, accepting a $0.25V_{P-P}$ to $2V_{P-P}$ signal range. The input amplifier and AGC circuit of these area detectors operate in a differential signal mode to provide good common mode and power supply rejection. The purpose of the AGC loop is to maintain a constant area detect value that correlates to the zero scale ($1.25V_{REF}/1.0V_{REF}$) and full scale ($3.75V_{REF}/3.4V_{REF}$) output values based upon the minimum and maximum burst value. The sensing for the AGC is at the output of the area detector, allowing signal ranging based on the area of burst rather than the signal level of the burst. The AGC is intended to be updated at every sector of servo position bursts such that the signal variances due to platter radius and differences in read channel data frequencies can be corrected. The initial gain of the AGC circuit is established by the voltage applied to the REF_{AGC} input.

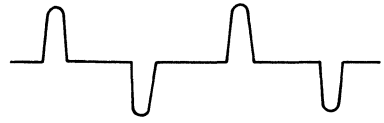
In this closed-loop system, the area detected output voltage is fed back and compared with the REF_{AGC} voltage in the G_M amplifier with a G_M of 1/4000 ohms, to provide a gain control current, charging and discharging C_{AGC}.

The AGC value is held constant by the hold function and is controlled by H_{AGC} pin. When H_{AGC} is at a logic high the level of gain can change up or down and is held at a constant gain with a logic low input.

A capacitor from ground to the C_{AGC} pin holds the gain setting when H_{AGC} is at a logic low level and the area detector output does not affect the gain setting in this mode. See figure 1 for the AGC burst timing.

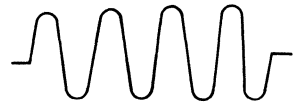
1.2 AREA DETECTOR

The area detector provides a measurement of servo burst area during a time window beginning at the first falling zero crossing edge after the GATE input is placed in a logic high state and ends at the first falling zero crossing edge after the GATE input is placed in a logic low state. The Zero crossing output enables the user to time the gate pulse by counting zero crossings. The analog input should be without open baseline by either keeping burst pulse spacing sufficiently close to avoid it or band limiting the signal. In most cases, both are necessary.



a. May clock anywhere and give multiple transitions, not acceptable.

b. Proper spacing.



c. Band limiting.

The value of the area measurement is held on the output hold capacitor (C_H) until the RESET line is asserted. The RESET pin when placed in a logic high state for at least 300ns resets the area detector output to 1.25V which is the zero scale reference point and equals the voltage value on the $1.25V_{REF}$ pin. See Figure 2 for position area burst detection timing.

ZERO X Detector Output

The output of the zero crossing detector (comparator) is provided for system synchronization. This signal is internally generated in ECL, but an internal ECL to TTL converter is provided to simplify external interfacing to this signal.

1.3 BANDGAP REFERENCE

A 2.5V bandgap reference is included on the ML4532 and ML4533 and a 2.2V one in the ML4536, to set up internal biasing and establish the on-track reference level. This is also a buffered output. Full-scale (V_{REF+}) and zero scale (V_{REF-}) outputs are derived and buffered from the bandgap to simplify the interface to A/D converters, such as the ML2261 or ML2264. The $1.25V_{REF}$ pin is tied directly to the V_{REF-} pin of the A/D converter and with a 510Ω resistor to ground. The $3.75V_{REF}$ pin is tied directly to the V_{REF+} pin of the high speed A/D converter. The ML4536 offers a $1.0V_{REF}$ and $3.4V_{REF}$ for interface with the A/D converter on the Zilog type microcontroller devices.

1.4 PWM D/A OF THE ML4532

A D/A is included on the ML4532 for driving the VCM driver to position the head or for any other desired system error compensation, such as processor-controlled AGC set point during head change. This is a PWM D/A and requires a pulse width modulation logic signal from the microcontroller signal to be applied to the MSB_{PWM} and LSB_{PWM} pins. The buffered and filtered output appears at the (D/A OUT) pin. This output voltage swing is centered around the $2.5V_{REF}$ pin (2.5V). The end-points of the D/A output are defined by:

PWM DAC Output Description:

Range Point	Duty Cycle at MSB_{PWM}	Duty Cycle at LSB_{PWM}	Voltage Output
"Negative" Full-Scale:	0%	0%	1.094V
	0%	100%	1.250V
	100%	0%	3.594V
"Positive" Full Scale:	100%	100%	3.750V

The D/A is designed for 8-bit binary coding with the MSB weighted 16 times the LSB. The MSB_{PWM} and LSB_{PWM} inputs are negative true in that if these inputs are in a low state for 100% of the time the D/A output will be 1.094 volts and if are held in a high state for 100% of the time the output will be at 3.75 volts. The D/A output voltage is 1.25 volts if the MSB_{PWM} input pulse width has a 1/16 or 6.25% positive duty cycle and the LSB_{PWM} is in a constant low state or if the MSB_{PWM} input is held in a low state and the LSB_{PWM} input is held in a high state. The output voltage range that is controlled by the MSB_{PWM} input is 2.5 volts and the LSB_{PWM} input controls 156mV. The time constant for the PWM smoothing filter is approximately $3k\Omega \times C_{PWM}$. The external capacitor (C_{PWM}) should be made sufficiently large to smooth out the PWM ripple.

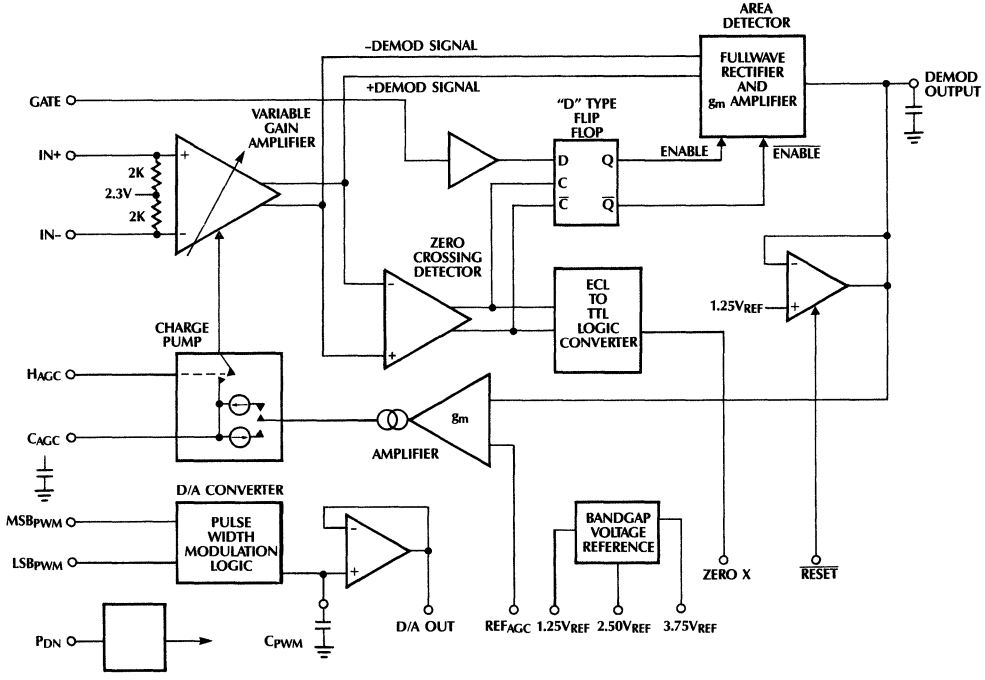


Figure 5. ML4532 Functional Block Diagram

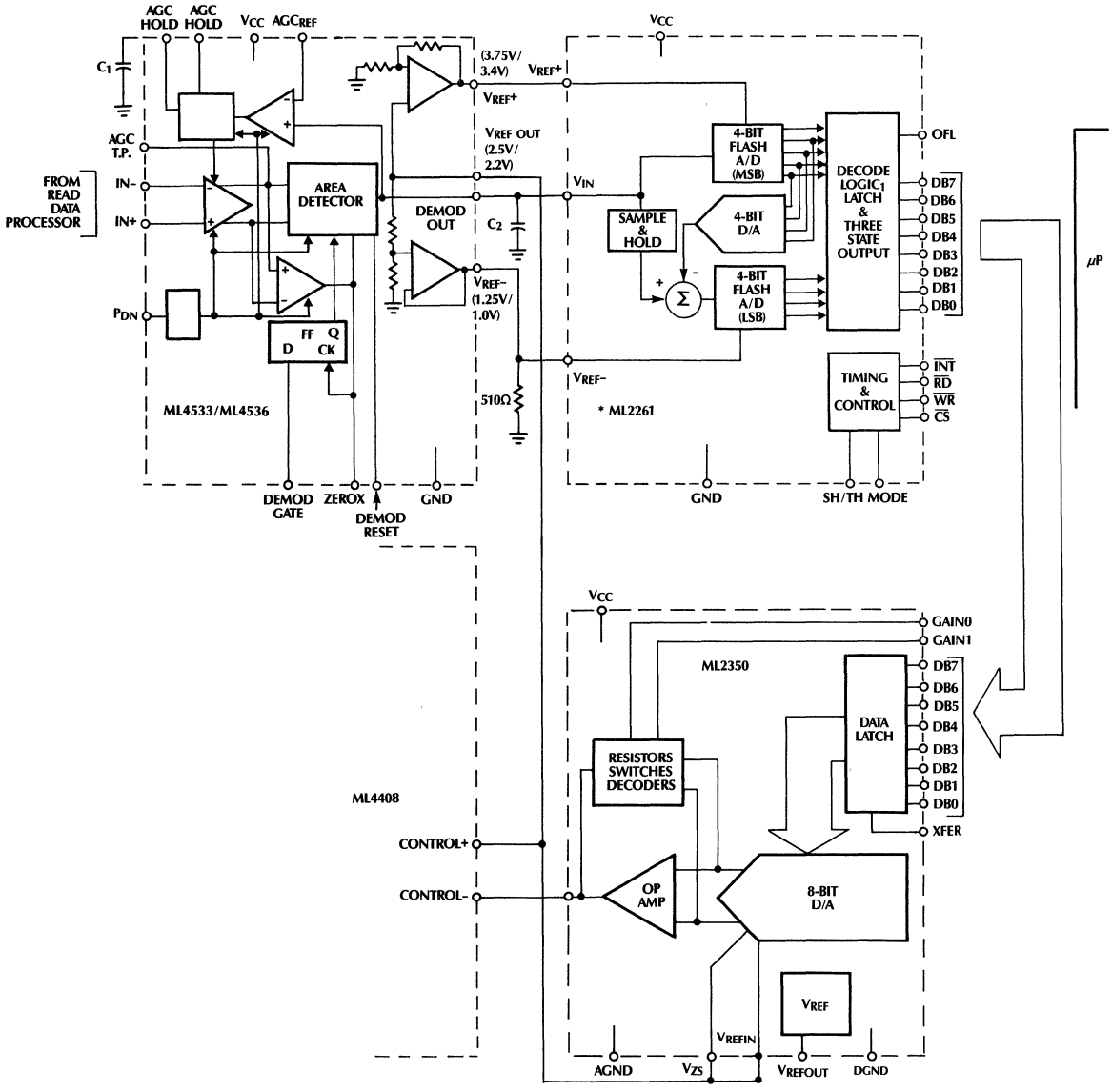


Figure 6. Typical Application ML4533/ML4536

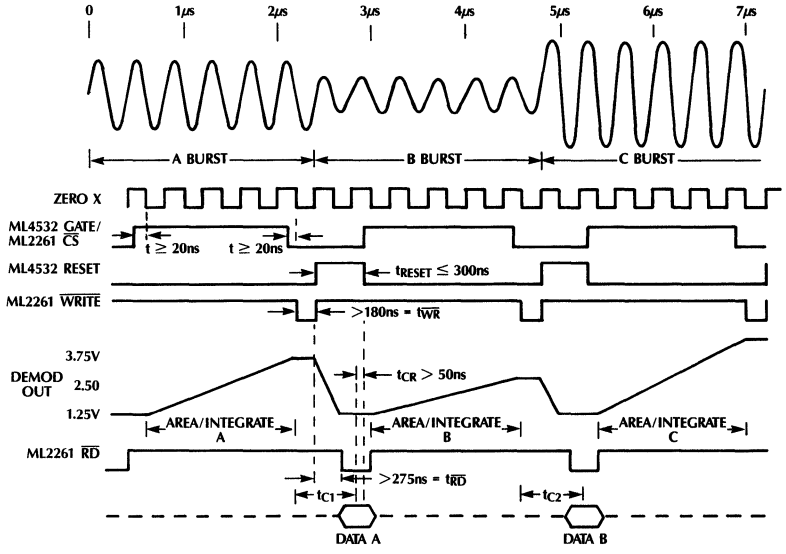


Figure 7. ML4532 Application Timing with ML2261 A/D Converter

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ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML4532CQ	0°C to +70°C	MOLDED PCC (Q20)
ML4532CR	0°C to +70°C	MOLDED SSOP (R20)
ML4533CS	0°C to +70°C	MOLDED SOIC (S16)
ML4536CS	0°C to +70°C	MOLDED SOIC (S16)

Area Detector Based Embedded Servo Demodulator

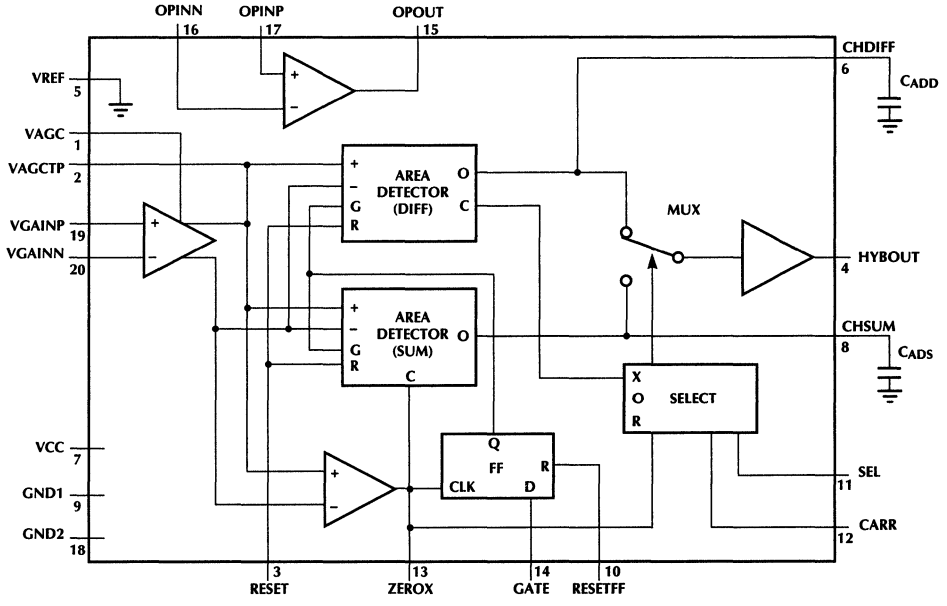
GENERAL DESCRIPTION

The ML4534 Embedded Servo Demodulator IC is designed for use in the hybrid data surface channel of an high-performance disk drive. Hybrid data are interleaved on the data surface with data records and encoded in A/B differential burst format, with a AGC field preceding the burst information. The AGC field is used by the read channel to set AGC gain levels in the burst area, which once established are held fixed for the duration of the servo burst. The demodulator measures burst amplitude using an area detection scheme, for improved noise immunity and provides both (A-B) and (A+B), to permit position error normalization with on-chip synchronization and reset functions. Using the SEL and CARR inputs the on-chip multiplexer allows selection of either (A-B) or (A+B) as the output. The multiplexer and area detection capacitors operate in concert to provide a hold capability for both the (A-B) and (A+B) outputs. Also included is an uncommitted operational amplifier which could be used for voice-coil motor current sensing.

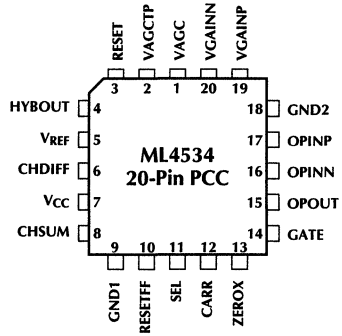
FEATURES

- Allows for Area Detection of back-to-back bursts
- 2% nonlinearity over input signal range
- Reset forces voltage on the Area Detecting capacitors C_{ADD} to V_{REF} & C_{ADS} to $V_{REF}/2$
- Separate Reset provided for Resync Flip-Flop
- Muxed/Selectable (A–B) & (A+B) demodulator output
- General purpose operational amplifier, applicable for use in voice coil motor current sensing
- 5V supply, 20-pin, J-leaded, PLCC package

BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	VAGC	Gain Control input on the VGA
2	VAGCTP	Test point connected through an isolation resistor to the output of the VGA
3	RESET	Asserting this input pin resets the area detector (DIFF) to V_{REF} (+2.5V) and the area detector (SUM) to $V_{REF}/2$
4	HYBOUT	Output of the multiplexing amplifier, with V_{REF}, (A–B) or (A+B) area detector output, depending on the state of the SEL & CARR pins.
5	V_{REF}	+2.5V reference voltage input.
8	CHSUM	The (A+B) area detector integrating capacitor is connected between this pin and the ground.
7	V_{CC}	+5 Volt supply
6	CHDIFF	The (A–B) area detector integrating capacitor is connected between this pin and the ground.
9	GND	Ground
10	RESETFF	Active high signal resets the resynch flip-flop
11	SEL	This pin in conjunction with the CARR pin, governs the multiplexer channel selection as follows : SEL CARR Mux Channel 0 X V_{REF} 1 0 (A–B) 1 1 (A+B)
12	CARR	Asserting this pin high inverts the carrier input of the (A–B) area detector. CARR should be asserted throughout the B burst of the A/B burst pair. While the CARR pin is asserted, the (A–B) area detector integrates the B burst in a direction opposite to that in which the A burst is integrated, thus realizing the (A–B) differencing operation. Carrier polarity in the (A+B) Area Detector is not affected by the state of the CARR pin. CARR pin in conjunction with the SEL pin, selects the multiplexer output.
13	ZEROX	This is the output of the Carrier Comparator. +ZEROX is a nominally square wave having transitions coinciding with zero crossings of the output VGA.
14	GATE	Asserting this line enables the (A+B) and (A–B) area detectors to measure area of the output signal of the VGA. This signal is re-synchronized to the area detector carrier internally before application to the area detectors.
15	OPOUT	Optional operational amplifier (short circuit protected) output.
16	OPINN	Optional operational amplifier inverting input.
17	OPINP	Optional operational amplifier non-inverting input.
18	GND	Ground
19	VGAINP	VGA non-inverting input. Inputs should be AC coupled
20	VGAINN	VGA inverting input. Inputs should be AC coupled

NOTE: The value of the CHSUM capacitor should be roughly twice that of the CHDIFF capacitor. It is also advisable to include a small resistor in series with the capacitor on the CHSUM pin and also the CHDIFF pin, to improve settling time.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (V_{CC}) .....-0.3 to + 7 VDC
Storage Temperature (T_{STG}) .....-65 to +150°C
Package Dissipation
T_A = 25°C (Board Mount) 875mW
Package Lead Temperature:
Soldering (10 sec) .....260°C
Vapor Phase (60 sec) .....215°C
Infrared (15 sec) .....220°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage Range (V_{CC}) .....5 ± 5% VDC
Temperature Range .....0 to +70°C
Operating Junction Temperature (T_J) .....+25 to +125°C

ELECTRICAL CHARCTERISTICS

The following specifications apply over the recommended operating conditions of T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, and external component values as recommended, unless otherwise stated.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	VAGC = 4.0V, V_{REF} = 2.5V		20	40	60	mA
I_{VREF}	V_{REF} = 2.5 V		–50	25	200	µA
GATE, CARR, SEL, RESET, RESETFF	For all signals in test program	V_{IH} V_{IL}	 0.8		2.0	V V
GATE, CARR, SEL, RESET, RESETFF	For V_{IH} = 2.4V and V_{IL} = 0.8V	I_{IH} I_{IL}	–250 –400		–10 40	µA µA
VGAINPDC (VINP)	VGAINP, VGAINN open		2.3	2.5	2.7	V
VGAINNDC (VINN)	VGAINP, VGAINN open		2.3	2.5	2.7	V
V_{OH} ZEROX	VGAINP = 3.5, I_{OH} = –0.4mA VGAINN = 1.5V		2.7		5.0	V
V_{OL} ZEROX	VGAINN = 3.5, I_{OL} = 2.0mA VGAINP = 1.5V		0		0.5	V
OPERATIONAL AMPLIFIER USED FOR MOTOR CURRENT SENSING						
I_{BIAS} Offset	OPINN = OPINP = 1.0V		–200		200	nA
V_{OS} - MCS	A_V = 2.0, V_{IN} = 0		–15		+15	mV
V_{OH} - MCS	A_V = 2.0, V_{IN} =-1.0, I_{SRC} = –1.5mA		3.8		5.0	V
V_{OL} - MCS	A_V = 2.0, V_{IN} =1.0, I_{SINK}= 1.5mA		0		1.0	V
I_{SINK} - MCS	Openloop, OPINP = 0.0V OPINN = 1.0, OPOUT = V_{CC}		1.5		10	mV
I_{BIAS} - MCS	OPINN = 1.0, OPINP = 1.0 (IOPINN + IOPINP)/2		–2.0		0.0	µA
Amplifier Settling Time (t_{SMCS})	R_{OUT} = 604Ω, C_{OUT} = 36pF			0.4	1.0	µs
Amplifier Bandwidth			4	8		MHz
Amplifier Gain (A_V)	Open Loop		58	63		dB
AGC						
A_V - VGAMIN	Minimum Gain of AGC with 400mV input		0		1.1	V/V
A_V - VGAMAX	Maximum Gain of AGC with 100mV input		6.6		20	V/V
VAGCBIAS	VAGC = 1.0		0		200	µA

ELECTRICAL CHARCTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RESET CIRCUITRY					
IRESET SUM, DIFF	RESET = V_{IH}	80		400	µA
IOFF SUM, DIFF	RESET = V_{IL}	–10		10	nA
VCH SUMRESET = V_{IH}	1.245	1.260	1.275	V	
VCH DIFF RESET = V_{IH}	2.490	2.5	2.510	V	
I SUM, DIFF UNBAL	GATE = V_{IH}, CLOCK, 1V swing VAGC 1X, Measure Current with VGAINP = VINP + 0.2 and VGAINN = VINN – 0.2, then do VGAINP = VINP – 0.2 and VGAINN = VINN + 0.2, Subtract	–40		40	µA
I DIFF UNBALXOR	CARR = V_{IH}	–40		+40	µA
I PEAK SUM	VGAINP = VINP + 1.0 VAGC = 1.0	–540	–400	–265	µA
I PEAK DIFF P	VGAINP = VINP + 1.0 VGAINN = VINN – 1.0 VAGC = 1.0, CARR = V_{IL}	–540	–400	–265	µA
I PEAK DIFF ON	VGAINP = VINP + 1.0 VGAINN = VINN – 1.0 VAGC = 1.0, CARR = V_{IH}	265	400	540	µA
VOH SUM	VGAINP = VINP + 1.0 VGAINN = VINN – 1.0	3.9		5.0	V
VOH DIFF	VGAINP = VINP + 1.0 VGAINN = VINN – 1.0 CARR = V_{IL}	3.9		5.0	V
VOL DIFF	VGAINP = VINP + 1.0 VGAINN = VINN - 1.0 CARR = V_{IH}	0.0		1.0	V
IGATE	GATE = V_{IH}, CLOCK, VAGC 1X, V_{SWING} = 1.0	–10		10	nA
IRESETFF	RESETFF = V_{IH}	–10		10	nA

ELECTRICAL CHARCTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
MUX AMPLIFIER					
VHYBOUT	CARR = V_{IL}, SEL = V_{IL}	2.4		2.6	V
VOS MUX SUM	CARR = SEL = V_{IH}, CHSUM = 2.5	–8		8	mV
VOS MUX DIFF	CARR = V_{IL}, SEL = V_{IH}, CHDIFF = 2.5	–8		8	mV
IBIASSUM	CARR = SEL = V_{IH}, CHSUM = 2.5	0		300	nA
IBIASDIFF	CARR = VIL, SEL = V_{IH}, CHSUM = 2.5	0		300	nA
VOHMUX	CARR = SEL = V_{IH} CHSUM = 3.95, I_{SRC} = 1.5mA	3.8		5.0	V
VOLMUX	CARR = V_{IL}, SEL = V_{IH} CHDIFF = 0.95, I_{SINK} = 1.5mA	0		1.0	V
ISINKMUX	CARR = V_{IL}, CHDIFF = 0.95 SEL = V_{IH}, VHYBOUT = V_{CC}	1.5		10	mA
Amplifier settling time (t_{SMUX})	R_{OUT} = 604Ω, C_{OUT} = 36pF		0.4	1	µs
$I_{LEAKAGE}$			10	nA	
Linearity	0 to 1 V_{INPUT}, with VAGC such that A_V VAGC = 1.0	–5		5	%F.S

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FUNCTIONAL DESCRIPTION

The ML4534, +5V Embedded Servo Demodulator IC is designed for use in the hybrid data surface channel of an high-performance disk drive. Hybrid data are interleaved on the data surface with data records and encoded in A/B differential burst format, with an AGC field preceding the burst information. The AGC field is used by the read channel to set AGC gain levels in the burst area, which once established are held fixed for the duration of the servo burst. The demodulator measures burst amplitude using an area detection scheme, for improved noise immunity and provides both (A–B) and (A+B), to permit position error normalization. Using the SEL and CARR inputs, the on-chip multiplexer allows selection of either (A–B) or (A+B) on the output. The multiplexer and area detection capacitors operate in concert to provide a hold capability for both the (A–B) and (A+B) outputs. The area detectors are designed to minimize the pipeline transport delay while accurately quantizing the area of servo bursts in high speed hybrid servo systems. The major functional blocks of the ML4534 are briefly discussed below.

VARIABLE GAIN AMPLIFIER

Hybrid servo burst data from the disk read channel are capacitively coupled into the VGA through the differential input pins (VGAINP, VGAINN). VGA gain is controlled by the voltage on the VAGC pin, and the gain is varied in order to secure constant area of the output signal and counteract the amplitude regulating operation of the read channel AGC loop.

VGABUF COMPARATOR

The VGABUF comparator detects zero crossings of the composite signal delivered by the VGA. The output of this comparator controls the synchronous rectification of the composite VGA output, in the area detectors.

The comparator output is provided at a TTL level on the ZEROX pin. Control logic in the servo channel employs the ZEROX signal to produce an area detector enabling gate, which spans a fixed number of cycles of the composite signal.

AREA DETECTORS (SUM AND DIFF)

The area detectors detect A and B burst levels by area detection. Two area detectors are provided — one to measure the sum of A and B bursts (A+B), and a second one to measure the difference (A–B). Each area detector is implemented as a gated current — output synchronous rectifier driving an external charge accumulating integrating capacitor. Area detection occurs only while the area detector is enabled under control of the GATE pin. When the detector is disabled, the integrating capacitor is effectively floated. An on-chip binary (FF) re-synchronizes the gating signal to remove any phase shifts due to logic delays in the external gate control logic. Initial conditions on the integrating capacitors are established prior to an area detecting operation by a reset circuit controlled by the RESET pin. A reset operation forces the voltage on the area detecting capacitors to equal the 2.5 volts applied on the V_{REF} pin. Determination of the burst difference (A–B) is accomplished under control of the CARR pin, by inverting the phase of the carrier input to the second area detector, while the burst B is being detected. The inversion is performed by an XOR gate. Accordingly (A–B) is bipolar relative to V_{REF}, while (A+B) is unipolar.

MULTIPLEXER AMPLIFIER

The multiplexer amplifier drives the HYBOUT pin and allows sequential interrogation of the (A–B) and (A+B) measurements, the results of which are stored on the external integrating capacitors. The amplifier is implemented as two independently selectable input stages, driving a common output structure, to form a voltage follower. To minimize the droop of the (A–B) and the (A+B) measurements, both input stages are biased off during periods when neither measurement is required to be routed to the HYBOUT pin. The SEL and CARR pins govern multiplexer channel selection through a decoding network.

Figure 1 shows a typical hybrid servo system application diagram for the ML4534 and also illustrates waveforms characteristic of a hybrid demodulator in a typical application

OPERATIONAL AMPLIFIER USED FOR MOTOR CURRENT SENSE

This general purpose operational amplifier is intended for use as a differential to single-ended convertor and level shift stage. It performs voice coil motor current sensing by monitoring the voltage developed differentially across current sense resistors, on the ground side of the voice coil power driver bridge.

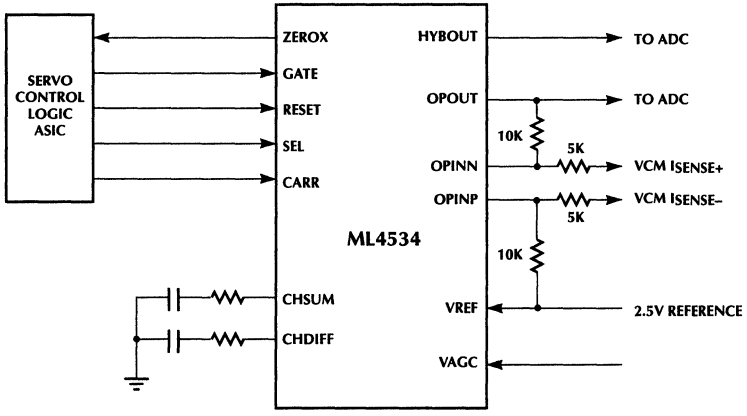


Figure 1. A Typical Servo System Application with the ML4534.

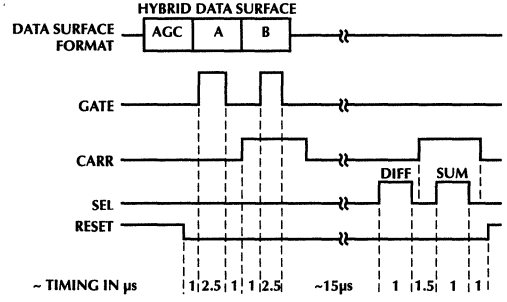


Figure 2. Illustrative Waveforms

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4534CQ	0°C to +70°C	20-Pin Molded PLCC (Q20)

ML4535

Area Detection Based Hybrid Servo Demodulator

GENERAL DESCRIPTION

The ML4535 is a bipolar monolithic hybrid servo circuit that provides area measurement demodulation of both the continuous servo surface (dedicated servo) and the sectored servo data (embedded servo) information in a high end disk drive. It operates on a single +5V supply and is intended to interface to a moderate speed, successive approximation ADC, with multiplexed inputs and sample and holds, like the ML2377 family.

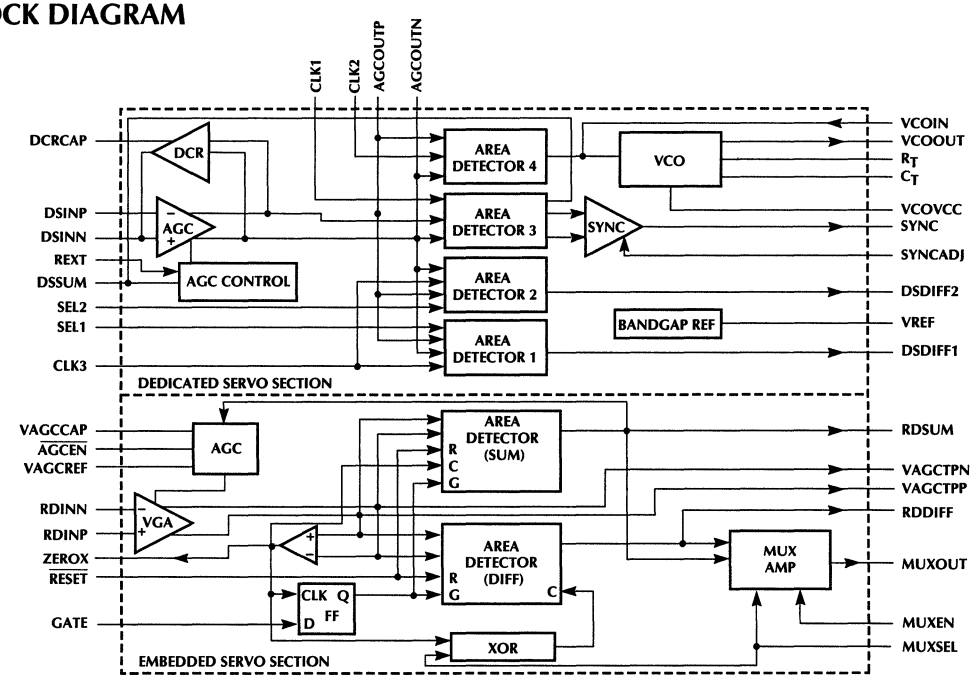
The area detectors are designed to minimize the pipeline transport delay while accurately quantizing the area of servo bursts in high speed servo systems. The data surface (embedded) servo demodulator section consists of Sum and Difference area detectors along with an AGC control loop. The continuous (dedicated) servo demodulator section consists of a variable gain amplifier, variable frequency oscillator and four synchronous area detectors.

The ML4535 provides a high level of integration for designing the complex Hybrid Servo systems becoming popular in disk drives requiring very high bit and track densities, in excess of 3500 TPI.

FEATURES

- Allows for area detection of back-to-back bursts
- 2% non-linearity over the input signal range
- Single +5 volt operation
- Internal 2.5V bandgap reference with reference output
- Separate AGC control loop for data surface and servo surface demodulator sections.
- Data surface amplitude control self contained on chip
- Data surface demodulator has muxed/selectable (A-B) and (A+B) outputs.
- Four synchronous area detectors onboard for implementing the continuous servo demodulator.
- Threshold based Sync detector
- Servo surface area detectors (1 & 2) have current output and can be individually selected using the SEL# pins.
- Available in 44-pin TQFP package

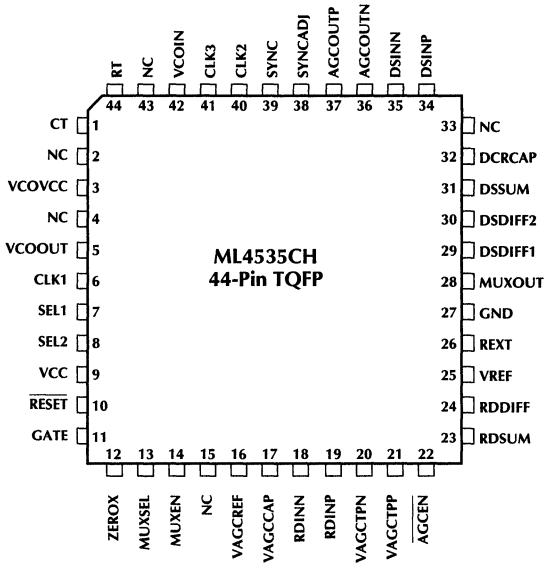
BLOCK DIAGRAM



PIN CONNECTION

ML4535

44-Pin TQFP



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PIN DESCRIPTION

PIN#	NAME	FUNCTION
1 44	CT RT	Pins to connect a resistor/capacitor network for setting the center frequency of the internal VCO; R from RT to CT, C from CT to VCOVCC
2 4 15 43 33	NC	No connects. It is recommended to Connect these to GND
3	VCOVCC	+ 5V supply for PLL
5	VCOOUT	VCO clock output
6	CLK1	Clock for Area Detector 3 (AGC)
7	SEL1	Active high select signal for area detector 1
8	SEL2	Active high select signal for area detector 2
9	VCC	+ 5V supply (± 5%)
10	$\overline{\text{RESET}}$	Asserting this input pin resets the Area Detector (DIFF) to VREF and the Area Detector (SUM) to VREF/2 (active low)
11	GATE	Asserting this pin defines the SUM and DIFF area detect windows, to measure the area under the curve of the VGA output. This signal is resynchronized internally to ZEROX before application to the area detectors.
12	ZEROX	This is the logic signal output of the carrier comparator, nominally a square wave having transitions coinciding with zero crossings of the VGA output.

PIN DESCRIPTION (Continued)

PIN#	NAME	FUNCTION
13	MUXSEL	Asserting this pin inverts the carrier input of the Difference (A-B) area detector. MUXSEL should be asserted throughout the B burst of the A/B burst pair, to implement (A-B). While this pin is asserted, the Difference (A-B) area detector integrates the B burst in a direction opposite to that in which A is integrated, thus realizing the (A-B) operation. Carrier polarity in the (A+B) area detector is not affected by the state of the MUXEN pin. This pin along with the MUXEN pin, also selects the multiplexer output.
14	MUXEN	This pin in conjunction with the MUXSEL pin governs the multiplexer channel selection as follows: MUXSEL MUXEN MUXOUT X 0 VREF 0 1 Difference (A-B) 1 1 Sum (A+B)
16	VAGCREF	AGC voltage reference
17	VAGCCAP	AGC Loop Filter/Hold Capacitor
18 19	RDINN RDINP	Differential input to VGA from Data surface (embedded servo). Inputs must be AC coupled.
20 21	VAGCTPN VAGCTPP	Test points connected through isolation resistors to the output of the VGA. Max $2V_{p-p}$ differential. Typically around 1V.
22	$\overline{\text{AGCEN}}$	AGC enable pin, defines area detect window (active low signal)

PIN#	NAME	FUNCTION
23	RDSUM	The SUM area detector integrating capacitor is connected here.
24	RDDIFF	The DIFF area detector integrating capacitor is connected here.
25	VREF	2.5V Bandgap reference output
26	REXT	A 15.8k (1%) resistor to GND sets the transconductance of all Area Detectors current outputs
27	GND	Ground pin
28	MUXOUT	Output of the multiplexer with DIFF or SUM output
29	DSDIFF1	Area Detector #1 (A,B) or the Normal output
30	DSDIFF2	Area Detector #2 (C,D) or the Quad output
31	DSSUM	Pin for connecting the filter for the AGC loop (Dedicated surface)
32	DCRCAP	DC Restore capacitor
34 35	DSINP DSINN	Differential signal input from Continuous (dedicated) servo surface. Inputs must be AC coupled
36 37	AGCOUTN AGCOUTP	Test points connected through isolation resistors to differential output of servo surface AGC.
38	SYNCADJ	External adjustment of sync threshold below or above the internal setting.
39	SYNC	Servo frame sync signal output
40	CLK2	Clock for Area Detector 4, (PLL)
41	CLK3	Clock for Area Detectors 1 & 2 (POS)
42	VCOIN	Pin for connecting the loop filter for the PLL or external drive

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (VCC) ..... –0.3 to +7 VDC
Package Dimension, TA = 25°C
(board mount) ..... TBD mW
Package Lead Temperature
Soldering (10 sec) ..... 260°C
Vapor Phase (60 sec) ..... 215°C
Infrared (15 sec) ..... 220°C
Storage Temperature (tstg) ..... –65 to +150°C

OPERATING CONDITIONS

DC Supply Voltage (VCC) ..... 5+/–5% VDC
Temperature Range ..... 0 to +70°C
Operating Junction Temperature (Tj) ..... +25 to +125 °C

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
DC CHARACTERISTICS					
ICC Supply Current	VAGCCAP = 4.0V	60	89	110	mA
Bandgap Reference voltage, VREF		2.4	2.52	2.60	V
VIH	For CLK1, CLK2, CLK3 GATE, MUXEN, MUXSEL, AGCEN, SEL1, SEL2			2.0	V
VIL	For CLK1, CLK2, CLK3 GATE, MUXEN, MUXSEL, AGCEN, SEL1, SEL2	0.8			V
IIH	For CLK1, CLK2, CLK3 GATE, MUXEN, RESET MUXSEL, AGCEN, SEL1, SEL2	–40	–0.2	+40	µA
IIL	For CLK1, CLK2, CLK3 GATE, MUXEN, RESET MUXSEL, AGCEN, SEL1, SEL2	–400	–2	10	µA
AGC (for dedicated servo)					
DSINPDC, DSINNDC	open	2.4	2.5	2.6	V
AvAGC min Voltage gain from input to test point	DSSUM = 4.0V, Measure DSDIFF1 DSINP – DSINN = 0.5V		0.2	0.4	V/V
AvAGC max	DSSUM = 1.0V DSINP – DSINN = 20mV	75	120		V/V
DCRHIGH (DCR CAP VOLTAGE)	DSSUM = 1.0V DSINP – DSINN = 20mV	3.0	3.9		V
DCRLOW (DCR CAP VOLTAGE)	DSSUM = 1.0V DSINN – DSINP = 20mV	2.3	2.5	2.7	V
DSOFFSET	DSINP – DSINN = 0	–1	0.0001	+1	V
AREA DETECTOR 1 and 2					
DSDIFF HI 1	SEL1, SEL2 = VIH	VCC – 1.0	VCC – 0.5	VCC	V
DSDIFF LO 2	DSINP – DSINN = 0.1 DSSUM = 1V, CLK3=VIH		0.2	1.0	V
DSDIFF LO 1	CLK3 = VIL		0.2	1.0	V
DSDIFF HI 2		VCC – 1.0	VCC – 0.5	VCC	V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
AREA DETECTOR 1 and 2 (continued)					
DSDIFF HI R1	DSINN – DSINP = 0.1	VCC – 1.0	VCC – 0.5	VCC	V
DSDIFF LO R2	CLK3 = V_{IL}		0.2	1.0	V
DSDIFF LO R1	DSINN – DSINP = 0.1		0.2	1.0	V
DSDIFF HI R2	CLK3 = V_{IH}	VCC – 1.0	VCC – 0.5	VCC	V
IDSDIFF HI IDSDIFF LO	DSINP – DSINN = 0.1 DSINP – DSINN = –0.1	–200 100	–133 133	–100 200	µA µA
IDSDIFF1 IDSOFF2	SEL1 = V_{IL} SEL2 = V_{IL}	–1 1	–0.005 0.001	1 –1	µA µA
AREA DETECTOR 3					
SYNC LO	CLK1 = V_{IH}, I_{IL} = 1.6 mA DSSUM = 1.0V DSINN – DSINP = 0.1		0.35	0.5	V
SYNC HI	CLK1 = V_{IH}, I_{IH}= –0.4 mA DSSUM = 1.0V DSINN – DSINP = 0.1	VCC – 2.1	VCC – 0.8	VCC	V
$V_{SYNCADJ}$	$I_{SYNCADJ}$ = 0	0.1	0.18	0.5	V
I DSSUM OFF	DSINN – DSINP = 0V	15	35	70	µA
I DSSUM HI	CLK1= VIH, DSSUM = 1 V DSINP – DSINN = 0.1	–20	–83	–150	µA
I DSSUM LO	DSINN – DSINP = 0.1	100	186	250	µA
AREA DETECTOR 4, VCO					
I VCOIN HI	CLK2= VIH, DSSUM = 1 V DSINP – DSINN = 0.1V	60	136	200	µA
I VCOIN LO	CLK2 = VIL	–200	–135	–60	µA
VCO HI (V_{OH})	CT = 4.0V, VCOIN = 4.0V, I_{OH} = 0.4mA	2.3	2.6		V
VCO LO (V_{OL})	CT = 1.0V, VCOIN = 1.0V, I_{OL} = 1.6mA		0.25	0.5	V
RDINPDC, RDINNDC	open	2.3	2.5	2.7	V
V_{OH} ZEROX	RDINP – RDINN = 2.0V I_{OH} = –0.4 mA	VCC – 2.1	VCC – 0.7	VCC	V
V_{OL} ZEROX	RDINP – RDINN = 2.0V I_{OL} = 2.0 mA		0.36	0.5	V
V_{REXT}	R_{EXT} = 15.9K	2.2	2.48	2.8	V
AGC (for embedded servo)					
VAGCTP	RDINP – RDINN = 2.0 V VAGC = 1.0V	VCC – 1.5	VCC – 2.1	VCC – 2.7	V
Av VGA MIN	RDINP – RDINN = 1.0 V VAGC = 4.0V		0.3	0.5	V/V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
RESET LOGIC					
Av VGA MAX	RDINP – RDINN = 0.4 V VAGC = 1.0 V	2.0	2.7		V/V
VAGC BIAS	XAGC = 1.0 V	0	40	200	µA
IRESET SUM, DIFF	RESET = V_{IL}	50	100	200	µA
IOFF SUM, DIFF	RESET = V_{IH}	–100		100	nA
VSUM	RESET = V_{IL}	0.9	1.07	1.2	V
VDIFF	RESET = V_{IL}	2.0	2.13	2.3	V
I SUM, DIFF UNBAL	GATE = VIH, CLOCK VAGC 1X, 1 Vp-p swing	–40	0.4	40	µA
IDIFF UNBAL XOR	MUXSEL = VIH	–40		40	µA
I PEAK SUM	RDINP – RDINN = 1.0 V MUXSEL = VIH	–500	–377	–250	µA
I PEAK DIFF P	RDINP – RDINN = 1.0 V MUXSEL = VIH, VAGC = 1V	–500	–377	–250	µA
I PEAK DIFF XOR	RDINP – RDINN = 1.0 V MUXEN = VIH, VAGC = 1.0V	250	377	500	µA
VOHSUM, VOHDIFF	RDINP – RDINN = 1.0V	VCC – 1.0	VCC – 0.5	VCC	V
VOL DIFF, VOLSUM	RDINP – RDINN = 1.0V MUXSEL = VIH	0	0.2	1.0	V
IGATE	GATE = VIH, CLOCK 1X	–100	0	100	nA
MUXAMPLIFIER					
VOS MUXSUM	MUXSEL = MUXEN = VIL	0	5	16	V
VOS MUXDIFF	MUXSEL = VIH, VDIFF = 2.5V,	0	5	16	V
IBIASSUM DIFF	MUXEN = VIL SUM = DIFF = 2.5V	0	200	300	nA
VOHMUX	SUM = 3.9 V	VCC – 1.0	VCC – 0.9	VCC – 0.5	V
VOLMUX	DIFF = 0.95	0	0.9	1.0	V
INSINGMUX	VMUXOUT = VXX	1.5	1.86	2.5	mA
Amplifier settling time - tsmux	Rout = 604 ohms, Cout = 36 pF		0.4	1	µsec
Ileakage				10	nA
Linearity	0 to 1V input with VAGC such that AvVAGC = 1.0V	–5		5	%F.S

5

FUNCTIONAL DESCRIPTION

The ML4535 provides area measurement demodulation of both the continuous (dedicated) servo surface and the sectored (embedded) servo data on each of the data surfaces of a "hybrid" servo disk drive. It operates on a single +5V supply and is intended to interface to a moderate speed, successive approximation ADC with multiplexed inputs and sample and holds, like the ML2377. In a conventional peak detection based servo scheme, the attack rate of the peak detectors are inherently faster than the decay, high crest factor noise sensitivity is high and rectification must have a very low offset for it to be functionally correct. On the other hand area detection has much better noise rejection and is more tolerant of small AGC rectifier offsets. However it requires that the measurement period be an integer number of signal cycles. Hence when the timing requirements are satisfied, area detection is certainly more accurate than peak detection schemes.

DATA SURFACE OR EMBEDDED SERVO DEMODULATOR SECTION

The data surface (embedded) servo demodulator section of the ML4535 consists of a standalone AGC control loop so that the amplitude control function is self contained on the chip and two area detectors providing the sum (A+B) and difference (A–B) which are output through a mux amplifier.

Input Amplifier and AGC

The input amplifier and AGC circuit operate with differential inputs in the range of 0.25Vp–p to 2Vp–p, from the read channel filter's lowpass outputs. The input impedance of the RDIN inputs is approximately 2.3kΩ. The purpose of the AGC loop is to maintain a constant area detect value that correlates to the zero scale and full scale output values based upon the minimum and maximum burst value. The sensing for the AGC is at the output of the SUM area detector, allowing signal ranging based on the area of the burst rather than the peak level of the burst. The AGC is intended to be updated at every sector of servo position bursts such that the signal variances due to the disk radius and differences in the read channel data frequencies can be corrected. In this closed-loop system, the area detected output voltage is compared with the VAGCREF voltage and fed back to provide a gain control current for charging and discharging the VAGCCAP. The VAGCREF voltage should be set to 80% of the full scale value of the RDSUM voltage output. The gain is varied to secure constant area of the output signal and provide amplitude control. The AGC gain value is held constant when the AGCEN is at logic low. When it is logic high, the level of gain can change up or down. The capacitor from VAGCCAP to ground holds the gain setting when AGCEN is at logic low and the area detector output does not affect the gain setting in this mode.

Zero X Detector

The output of the zero crossing detector (comparator) is provided for system synchronization. It detects zero crossings of the composite signal delivered by the Variable Gain Amplifier, VGA. The output of this comparator controls the synchronous rectification of the composite VGA output, in the area detectors. This signal is internally generated in ECL, but an internal ECL to TTL converter presents this output as a TTL level on the ZEROX pin. Control logic in the servo channel employs the ZEROX signal to produce an area detector enabling gate, which spans an integer number of cycles of the composite signal, thus helping to generate accurate timing. If one of the burst signal is very small then the ZEROX signal will not be generated correctly and the Area Detectors (SUM & DIFF) would stay ON. Hence a single radial (always full amplitude) pulse should be located at the beginning and end of each burst. This also minimizes track pairing.

Area Detectors (Sum & Difference)

The area detectors detect the A and B burst levels by area detection. Two area detectors — one to measure the sum of the A and B bursts (A+B), and a second one to measure the difference (A–B). Each area detector is implemented as a gated current — output synchronous rectifier, driving an external charge accumulating integrating capacitor. Area detection occurs only while the area detector is enabled under the control of the GATE pin. The GATE signal turns the SUM & DIFF Area Detectors ON and OFF. Internally it generates a synchronous signal clocked by the AGC output. When GATE is asserted high, the next rising edge of RDINP will turn ON the Area Detectors. When GATE is asserted low, the next rising edge of RDINP will shut OFF the Area Detectors. Thus GATE edges should occur near the falling edges of ZEROX. One point to note is that if the Area Detector is ON and there is no AGC signal then the internal synchronous signal will not change state even if the GATE signal is driven inactive low and the Area Detector continues to remain ON. When the detector is disabled, the integrating capacitor is effectively floated. The on-chip D Flip-Flop resynchronizes the gating signal to remove any timing error due to logic delays in the external gate control logic. It is important that the Area Detectors are shut off when not integrating a desired field, even if there is no AGC signal as the Area Detector offset currents will modify the Area Detector output voltage. Initial conditions on the integrating capacitors are established prior to an area detecting operation by a reset circuit controlled by the $\overline{\text{RESET}}$ pin. The minimum $\overline{\text{RESET}}$ pulse width will depend on the external capacitor used at RDSUM and RDDIFF pins. The pulse width is given by: t_{MIN} = [(CpF x 3V)/80μA] μsecs. $\overline{\text{RESET}}$ is normally held asserted from just after read out until just before the next sample measurement time. A reset operation forces the voltage on the DIFF area detecting capacitor to equal the voltage applied on the VREF pin and the voltage on the sum area detecting capacitor to equal VREF/2. In actuality when $\overline{\text{RESET}}$ is low the voltage observed on the RDDIFF pin will be in the range of 2V to 2.5V and the voltage observed on the RDSUM pin will be in the range of 1V to 1.2V. This is due to internal design constraints. Determination of the burst difference (A-B) or (–A+B) on

alternating tracks, is accomplished under control of the MUXEN pin, by inverting the phase of the carrier input to the DIFF area detector, while one burst is being detected. The inversion is performed by an XOR gate. Accordingly (A-B) is bipolar relative to VREF, while (A+B) is unipolar.

Multiplexer Amplifier

The multiplexed amplifier drives the MUXOUT pin and allows sequential interrogation of the (A-B) DIFF and (A+B) SUM measurements, the results of which are stored on the external integrating capacitors. The amplifier is implemented as two independently selectable input stages, driving a common output structure, to form a voltage follower. To minimize the droop of the (A-B) and the (A+B) measurements, both input stages are biased off during periods when neither measurement is required to be routed to the MUXOUT pin. The MUXSEL and MUXEN pins govern multiplexer channel selection through a decoding network.

CONTINUOUS OR DEDICATED SERVO DEMODULATOR SECTION

The continuous (dedicated) servo demodulator section of the ML4535 consists of its own variable gain amplifier and AGC loop, a variable frequency oscillator and four synchronous detectors. The DSIN input is usually of the order of 20mV–400mV differential peak to peak and the R_{IN} is approximately 4kohms.

The first synchronous detector (AREA DETECTOR #4) is used as a multiplying phase detector to control the variable frequency oscillator and complete the analog portion of the phase locked loop that recovers the clock. A standard PLL loop filter is connected on the VCOIN pin or an external signal could be used to drive this line. The RT and CT components are used to set the VCO frequency range. Figure 1 shows the graphical representation of the VCOOUT frequency vs VCOIN voltage for a fixed value of RT and CT. It is recommended that CT should be kept as large as possible, say around 50pF, otherwise parasitics could begin to dominate. Also it is recommended that CT should connect to the VCOVCC right at the pin and the VCOVCC should be well decoupled at that point. Stability could be further improved by placing another resistor to ground from the RT pin, allowing smaller RT and hence allowing the increase in CT. Recommended range for RT is 200 ohms to 2k ohms. Recommended VCO frequency range is 10 to 30 MHz with the VCO frequency being set at two or four times the servo pattern fundamental frequency. A typical loop filter circuit at VCOIN is shown at the frontend of figure 3. The gain of the VCO is approximately 10% of the center frequency per volt (MHz/volt). The VCOOUT has a V_{OH} of 2.2V to 2.4V and a V_{OL} of 0.5V which improves symmetry around the 1.4V threshold for the VCO (TTL compatible levels). The duty cycle is symmetrical with large enough swings on the RT and CT associated with the VCO.

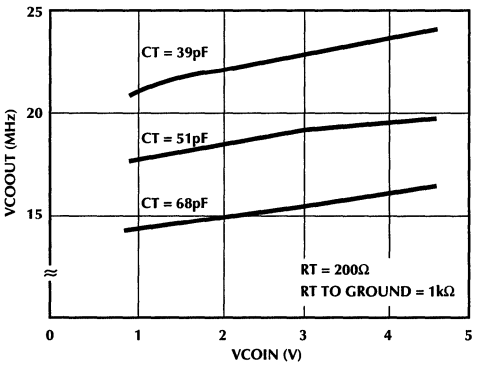


Figure 1. ML4535 VCO Characteristics

The second synchronous detector (AREA DETECTOR #3) is used for measuring the area of the composite signal, to determine its amplitude for comparison with the reference of the AGC loop. The AGC loop consists of the Area Detector 3, external filter capacitor on DSSUM, REXT resistor and internal voltage set reference current on DSSUM and the gain vs. control voltage characteristic of the VGA amplifier. The reference baseline voltage for the AGC output voltage is 2.5V. Area Detector 3 generates a current and when the integral of that current equals a DC current (approx 62µA) set by REXT, the AGC loop is stabilized. The differential output of the servo surface AGC is made available on the AGCOUTP and AGCOUTN pins. An amplitude level comparator is also included on this detector's output to provide the logic level output for Frame sync and Index data. The SYNC detector circuit is threshold based. The threshold level is set internally to 25% of full scale, however this level can be adjusted through the external SYNCADJ pin. Connecting a resistor from the SYNCADJ pin to ground increases the threshold level above 25%, while a resistor to VCC will decrease the threshold level below 25% of full scale. There is a ±20% potential of error on the amount by which the threshold is changed from the internal level using the SYNCADJ pin.

The third and fourth synchronous detectors (AREA DETECTORS #1 & #2) are used to demodulate the normal and quadrature position signals. The Area Detectors 1 & 2 are turned ON by asserting SEL1 and SEL2 lines active high. A logic low on these lines turns them OFF. The normal and quadrature outputs are currents that should be terminated off chip with nominal 19K resistors to VREF or 0.9 VREF. The center value of the nominal output voltage range of DSDIFF1 and DSDIFF2 (the output of Area Detectors 1 & 2) is 2.5V with a range of ±1.5V. The external resistors may be terminated to 2.3V to give maximum swing over supplies (since minimum V_{CC} is 4.5V, hence VCC/2 would be approximately 2.3V). Ripple frequency to slew rate relationship can be improved by adding switches in series with the terminating resistors gated by SEL# in the outputs, although this is usually not required.

The DC requirements of the filter can be reduced by using the configuration where the active filter amplifier does not contribute to the DC offset, for a unity gain configuration. The position detector gain is approximately 1.19. The emitter resistor in the AGC detector is around 16K, giving an I = 62.5µA. This implies that the average voltage out is approximately 1V, which implies that the output ON position with a duty cycle of 3/8 equals (0.375 x 1.19) = 0.466V base to peak based on the resistor ratio of 19K to 15.8K. Making this equal to the half span of the ADC by having a gain in the filter should not have a detrimental effect on the system accuracy because selecting the demodulator clock phase (based on track type) to result in the same polarity of the Position Error Signal (PES) slope and by using the same detector output section for track following results in the cancellation of offsets, with a minimum penalty in the reduction of the PES dynamic range.

Component Selection

The following section outlines the different equations for determining some of the component values associated with the ML4535 design.

VAGCCAP C = {(DC)/(2Kohms x BW)}

where DC = Duty cycle of the AGCEN signal (approx 1/10)
BW = AGC loop bandwidth = 2 x π x f (approx 500Hz)

RDSUM Capacitor C_{SUM} = {(560µA) x (T_{SAMPLE})/(2.8 x M)}

where M = portion of the full scale voltage to be used in nominal condition (suggested value = 0.8)
T_{SAMPLE} = width of the GATE pulse

RDDIFF Capacitor C_{DIFF}= {560µA) x (T_{SAMPLE})/(1.4 x M)}

where M = portion of the full scale voltage to be used in nominal condition (suggested value = 0.8)
T_{SAMPLE} = width of the GATE pulse

DCRCAP C = {(0.04 x 20)/(16Kohms x BW)}

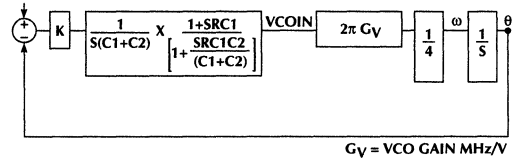
where BW is the AGC restore loop bandwidth = 2 x π x f (range 5 to 10kHz)

DSSUM C = (16/(BW x 8Kohm))

where BW is the bandwidth = 2 x π x f = (range 10 to 50kHz)

EXAMPLE SYSTEM DESCRIPTION

An example continuous servo composite servo encoding and the associated demodulator clock waveforms are shown in figure 2. The VCO operates at twice the frequency of the fundamental of the composite signal and drives two flip flops that generate quadrature and normal phase references. The Clock generation logic circuit and synchronizing circuit for the PLL, to acquire initial lock with type 2 loop, are shown in figure 3. A block diagram of the PLL is shown below with the transfer function based on the loop filter components (refer figure 3).



The value of the constant K is given by:

$$K = \frac{62}{\pi} \times \frac{\text{phase compared cycles in the servo frame}}{\text{total cycles in the servo frame}}$$

A type 2 loop has two poles at the origin of the S-plane or two time domain integrations — one in the frequency to phase conversion and one in the loop filter. In figure 3, the DC level at the non-inverting input of the left comparator should be approximately ($0.1V_{CC}$ plus one diode drop). The current supplied by the output resistors and series diodes should be approximately 62µA/4. Time constant is approximately 2 x (1/PLL BW) and the pullup resistors to V_{CC} are approximately 1 Kohm or much less than the value of the other resistors so as to make the output up level approximately equal to V_{CC} during operation. A state counter divides the servo frame into eight intervals which are:

NAME	LENGTH (IN CLOCK CYCLES)
S	2
X_1, X_2, X_3	1
A, B, C, D	n where n is an integer like 7 or 8

Note that all peaks of the composite signal are on Quad clock phase boundaries, so it contains only one fundamental frequency, which is easily acquired by the phase locked loop. The sync character is 180° out of phase with all others; thus at phase alignment it causes no disturbances to the phase comparator but gives an easily recognizable reverse polarity ripple in the AGC which is detected with a level detector to provide a frame sync logic signal to initialize the state counter.

The inphase clock is used throughout A, B, C, D but inverted 180° as required by the track type to give A–B, C–D, B–A, D–C without additional analog switching in position 1 demodulator for track following.

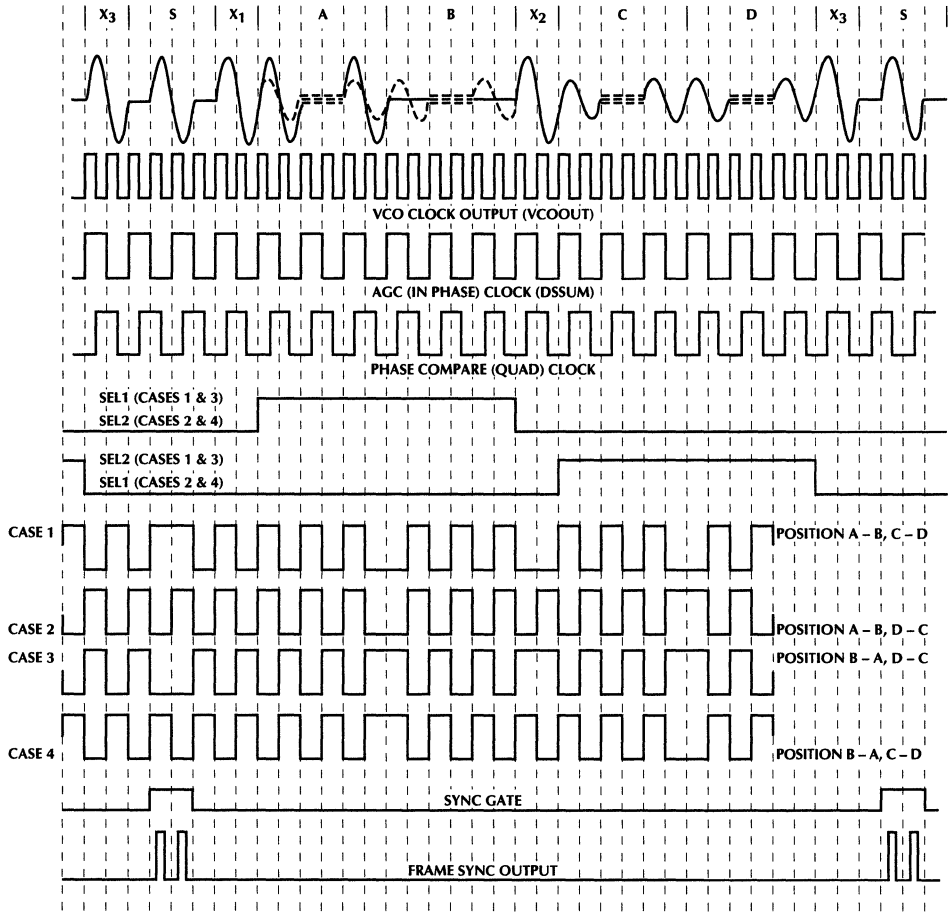


Figure 2. Continuous Servo Encoding and Demodulator Clock Waveforms

Filters are needed on each of the four demodulators for removing the carrier ripple and providing frequency compensation for the gain control and phase locked loop systems. The current output scaling of all four detectors to the AGC output are the same and set by on-chip resistors. The AGC setpoint is a current set by REXT and VREF. Thus a capacitor to ground provides an integrating response for the AGC control loop, as well as ripple filtering. For the phase comparator filter, two capacitors and a resistor provide D.C. integration plus a lead-lag for the PLL control loop compensation. For the position outputs, external 19K nominal resistors to (0.9 x V_{REF}) should be provided and a capacitor to ground is added to form a low pass ripple filter.

The phase compare detector forms phase only (not phase frequency) characteristic, so the loop will not acquire initial lock with an integrating loop filter, which is needed to assure no steady state phase error. Transfer function for the gain of the phase comparator (assuming a sinusoidal servo signal) is given by:

$$\frac{62\mu A}{\pi \text{ rad}} \times \left[\frac{(\text{time of X1, X2, X3}) + (\text{time of A, B, C, D})}{2 \times (\text{time of one frame})} \right]$$

The synchronizing circuit suggested (refer figure 2), senses when the VCO control voltage is near either rail and applies a pulse that ramps it toward the other rail and thus through the operational frequency where it locks. The lock range is much greater than the acquire range, so it retains lock in the presence of the resistor–coupled pulse, with a small phase error, until the pulse goes away and the phase error becomes zero.

It is generally recommended that the servo head magnetic width be equal to two track pitches for best results. In this case for an on-track position one of the four burst patterns becomes almost zero. There is no loss of information on phase when this happens, since then its complement is twice as large so that the sum of the two is constantly independent of position and thus the amount of phase information per frame is also constantly independent of position.

HYBRID SERVO VERSUS ONLY EMBEDDED SERVO

There are a number of merits in using a hybrid servo scheme consisting of a servo surface plus limited data head servo samples over the completely embedded or data head sector servo samples scheme. These are summarized below:

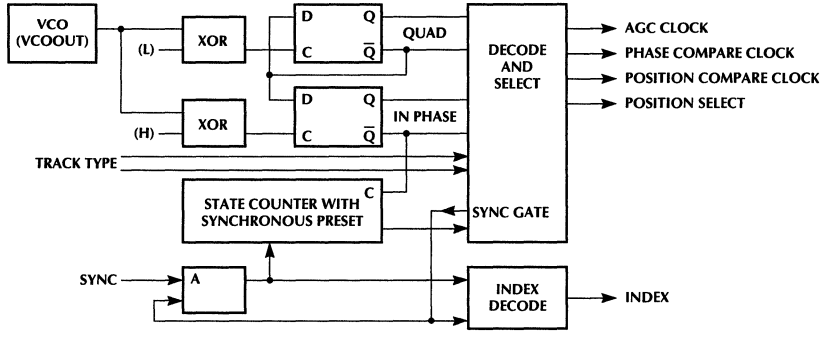
Cost: Lost data surface capacity is less than 1% for a servo surface plus samples compared to 8% for samples only. This suggests that with six or more disks, the servo surface has an advantage. Without a servo surface, it is difficult to generate accurately phase and track center aligned data head (embedded) servo sectors in the drive, requiring them to be done with extra time on an expensive servo writer and moving the cost crossover point nearer to four disks. Drive hardware and costs including assembly and test favour DSP implementations in either case.

Effect on position error sources: These can be very similar for both configurations with optimized control algorithims. The servo surface does have some advantages in being able to obtain higher bandwidths and thus faster settling time and greater reduction of non–repetitive run–out and random disturbances.

Effect on access time: A system with a servo surface has two advantages here. The ability to adjust the control signal at shorter time intervals and a higher small signal bandwidth, both of which reduce settling time. Move times can be equivalent.

Data integrity: Here there is a clear superiority for a servo surface system in preventing writes which destroy existing data. There are at least two ways in which this can happen. Electronic noise in the sector timing causes servo sectors to be over written, so that the head can no longer be positioned to read the track even if the data is intact. This probability can be made acceptably small by redundancy in the electronics. External mechanical shock while writing a data sector can not only cause improper writes of the new data but also overwrite adjacent tracks. Inherently there is no way to prevent this with servo sectors only, as there is no position data measurement available and estimators do no good for random fast disturbances. Dynamically balanced rotary actuators reduce this exposure compared to linear travel positioners but cannot eliminate it completely.

CLOCK GENERATION LOGIC (Implemented in Gate Array)



SYNCHRONIZING CIRCUIT FOR THE PLL (To acquire initial lock with type 2 loop)

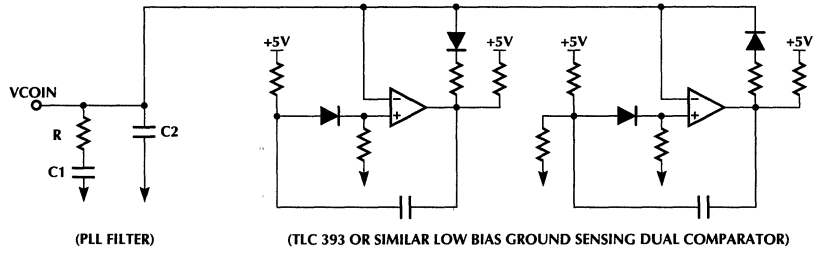


Figure 3. Support Circuitry for the ML4535 Based "Hybrid" Servo Subsystem

SERVO DESIGN SUGGESTIONS FOR A HIGH TRACK DENSITY DISK DRIVE

The best design choices for a high track density disk drive with four or more platters are outlined below and the hybrid servo subsystem based on the ML4535 & ML2377, provides the most optimum solution for implementing these design choices and making track densities greater than 3500 TPI achievable.

1) Continuous servo surface with quadrature signals plus some position samples and/or calibration tracks for each data head.

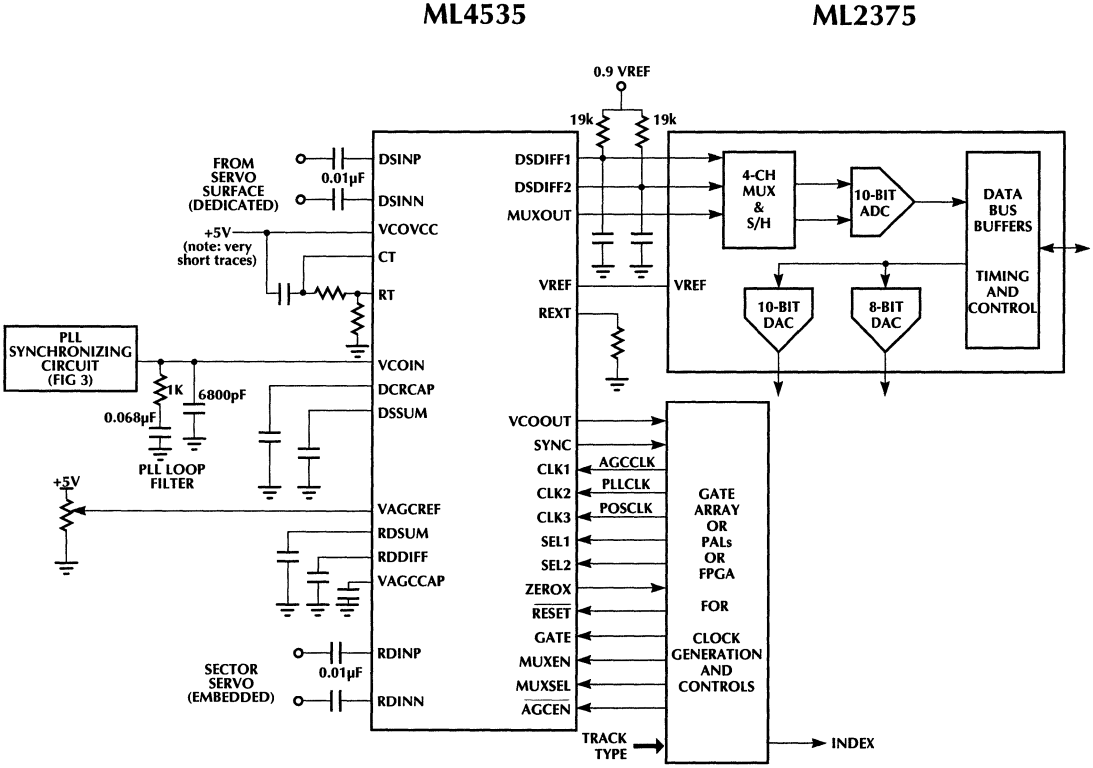
2) DSP implementation of the position control system for best performance of state estimators and adaptive parameter adjustment.

3) Area integration position demodulation on both the servo (dedicated) surface and data head position (embedded) servo samples, for best accuracy and noise rejection.

4) Thin film heads with gap edges aligned and perpendicular to the disk surface.

5) Dynamically balanced rotary actuator for best rejection of external mechanical shock.

ML4535 BASED SYSTEM APPLICATION DIAGRAM



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4535CH	0°C to +70°C	44-Pin TQFP (H44)

Micro Linear

ML4568

Disk Pulse Detector + Embedded Servo Detector

GENERAL DESCRIPTION

The ML4568 is a hard disk pulse detector with two gated peak detectors to demodulate embedded servo information. The pulse detector section includes a wide bandwidth differential amplifier with automatic gain control (AGC), a precision full wave rectifier, time channel and gate channel. The embedded servo peak detector section includes a full-wave rectifier, two gated peak detectors, buffered peak detector outputs, and a difference output. A 2.25V bandgap reference is also included on-chip.

The ML4568 is a 5V-only upgrade for 8468-type devices. Upgraded features include increased data rate operation (to 24 MB/s with RLL(1, 7) coding), improve pulse pairing (1ns), and reduced power consumption (400mW typical) resulting from 5V-only operation.

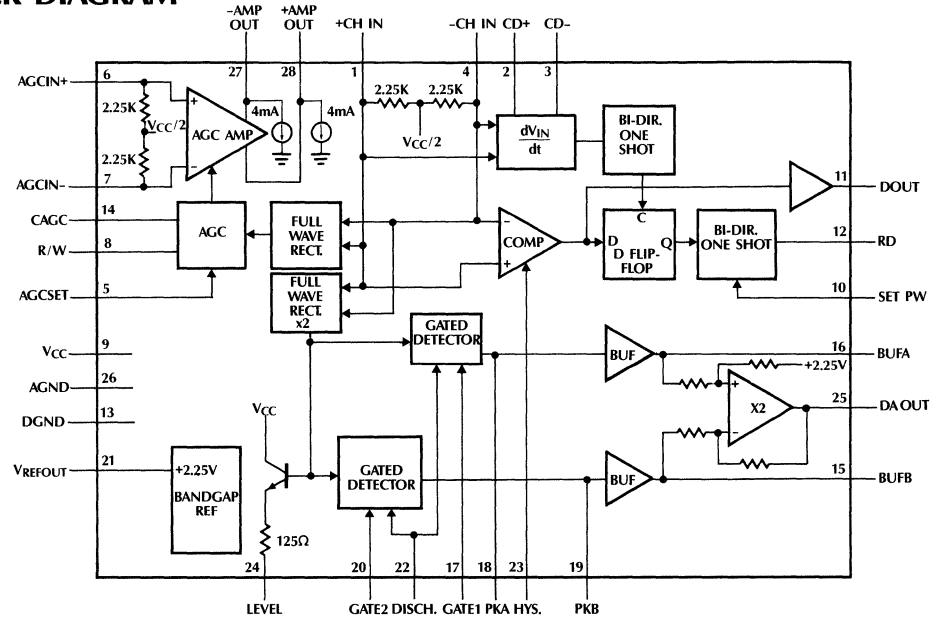
The ML4568 pulse detector section detects amplitude peaks, producing a TTL-compatible output which accurately indicates the time position of signal peaks. In hard disk applications, these signal peaks represent flux reversals in the magnetic medium.

FEATURES

- 5V-only operation
- Low power consumption (400mW typical)
- Supports 24 MB/s RLL(1, 7) coding
- Less than ±1 ns Pulse Pairing
- Wide input signal amplitude range ($10mV_{PP}$ to $100mV_{PP}$)
- On-chip differential gain controlled amplifier, differentiator, comparator gating circuitry, and output pulse generator
- Adjustable comparator hysteresis
- Dynamic hysteresis tracks signal amplitude
- AGC and differentiator time constants set by external components
- TTL compatible digital inputs and outputs
- Built in embedded servo detector
- On chip buffers provide low impedance servo output voltages
- User adjustable servo time constants

5

BLOCK DIAGRAM

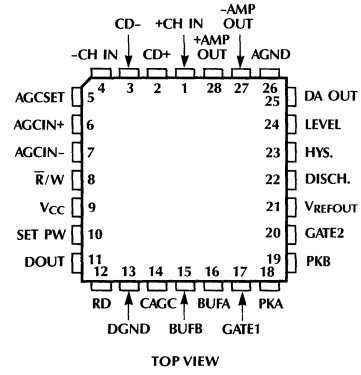


GENERAL DESCRIPTION (Continued)

The ML4568 also incorporates two gated detectors which detect embedded servo information, used for head positioning. The ML4568 provides two buffered low impedance voltage outputs which represent the peak detected level of each servo burst. The ML4568 also provides a buffered output that represents the voltage difference between the two servo channels, centered about V_{REF}.

PIN CONFIGURATION

PLCC-28



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
Power Supply		
9	V_{CC}	+5V ± 10% supply.
21	$V_{REF\ OUT}$	Internal 2.25 V reference voltage output.
26	ANALOG GROUND	Analog signals should be referenced to this pin.
13	DIGITAL GROUND	Digital signals should be referenced to this pin.
Analog Signals		
6 7	AMP IN+ AMP IN–	These are the differential inputs to the Amplifier. The output of the read/write head amplifier should be capacitively coupled to these pins.
28 27	AMP OUT+ AMP OUT–	These are the differential outputs of the Amplifier. These outputs should be capacitively coupled to the channel filter.
4 1	–CH IN +CH IN	These are the differential inputs to the time, gating and servo channels. These inputs must be capacitively coupled to the channel filter at the amp. outputs. The maximum differential peak-to-peak swing at this input is 1.5 V_{P_P}.
2 3	CD+ CD–	The external differentiator network is connected between these two pins.
23	HYS.	The DC voltage on this pin sets the amount of hysteresis on the differential comparator.

PIN #	NAME	FUNCTION
Analog Signals (Continued)		
24	LEVEL	This is a Peak Detector Output signal that is used in conjunction with the set hysteresis pin 23 to provide a dynamic hysteresis function.
5	AGCSET	The AGC circuit adjusts the gain of the gain controlled amplifier to make the differential peak to peak voltage at the Channel inputs equal to four times the DC voltage on this pin. $V_{AGCSET} = \frac{1}{2}V_{CC} + \frac{1}{4}V_{PP}$ where V_{PP} is the peak-peak differential voltage on the channel input.
14	CAGC	The external capacitor for the AGC is connected between this pin and Analog Ground.
18 19	PKA PKB	The peak detected servo signal voltage appears across the RC networks connected from these pins to analog ground.
16 15	BUFA BUFB	These low impedance pins, output the DC level at pins 18 and 19 respectively, level shifted down by two diode drops.
25	DA OUT	This low impedance pin outputs the difference in voltage between pins 16 and 15 about a zero level set by the voltage on pin 21.

PIN DESCRIPTION (Continued)

PIN #	NAME	FUNCTION
Digital Signals		
10	SET PW	An external capacitor to control the pulse width of the Encoded Data Out (RD) is connected between this pin and Digital Ground. See Figure 1.
8	$\overline{R}$/W	If this pin is low, the Pulse Detector is in the read mode and the chip is active. When this pin goes high, the pulse detector is forced into a stand-by mode. This is a standard TTL input.
11	DOUT	This is the buffered, open collector, output of the differential comparator with hysteresis.
12	RD	This is the standard TTL output whose leading edge indicates the time position of the peaks.
Digital Signals (Continued)		
17 20	GATE 1 GATE 2	These inputs accept TTL levels. When a low level is present the embedded servo signal is allowed to charge the RC network at pins 18 and 19 respectively. A high level will force a hold condition of the DC voltage across the RC network and will also disable the servo channel.
22	DISCH.	This input accepts a TTL level. A high level connects a 1.5K internal resistor to ground on pins 18 and 19.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
Pin 9 ..... 14V
TTL Input Voltage
Pins 8, 17, 20, 22 ..... 5.5V
TTL Output Voltage
Pins 12, 11 ..... 5.5V
Input Voltage
Pins 23, 5 ..... 5.5V
Minimum Input Voltage
Pins 23, 5 ..... –0.5V
Differential Input Voltage
Pins 6–7, 4–1 ..... 3V or –3V
ESD susceptibility rating is to be determined
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... 300°C
Maximum Power Dissipation at 25°C:
PLCC Package (derate TBD mW/°C above 25°C) ... 500mW

OPERATING CONDITIONS

V_{CC} ..... 4.5V to 5.5V
Ambient Temperature, T_A ..... 0°C to +70°C

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ELECTRICAL CHARACTERISTICS

Over recommended operating conditions.
Set Hysteresis = 0V, $V_{PIN\ 17}$ = 2V, READ/WRITE = 0.4V, $V_{PIN\ 22}$ = 0.4V, unless otherwise noted.

Symbol	Pins	Parameter	Conditions	Min	Typ	Max	Units
Amplifier							
Z_{INAI}	6, 7	Amp In Impedance (Note 1)	T_A = 25°C	1.8	2.4	3.0	KΩ
A_{VMIN}	28, 27	Minimum Voltage Gain Differential	AC Output 3 V_{PP}		6	15	V/V
A_{VMAX}	28, 27	Maximum Voltage Gain Differential	AC Output 3 V_{PP}	250	300		V/V
Channel							
Z_{INCI}	4, 1	Channel Input Impedance	T_A = 25°C (Note 1)		2.5		KΩ
I_{CAGC^-}	14	Pin 14 Current which Charges C_{AGC}	$V_{PIN\ 14}$ = 2.2V	5.0	5.8		mA
I_{CAGC^+}	14	Pin 14 Current which Discharges C_{AGC}	$V_{PIN\ 14}$ = 2.2V		0.5	2	μA
I_{AGCSET}	5	AGCSET Input Bias Current			8	100	μA
I_{IL}	23	Set Hysteresis Input Bias Current	$V_{PIN\ 23}$ = 0			–20	μA
I_{CD}	2, 3	Current into Pin 2 and 3 that Discharges C_D		0.8	1.0		mA
HYS	23	Peak Hys. vs V_{HYS}	$V_{PIN\ 23}$ = 1V	0.25	0.4	0.55	V_{PK}/ V_{DC}
Write Mode							
Z_{INAI}	6, 7	Amp In Impedance in Write Mode	$V_{PIN\ 8}$ = 2.0V		350	450	Ω
I_{AGC^-}	14	Pin 14 Current in Write Mode	$V_{PIN\ 8}$ = 2.0V, $V_{PIN\ 14}$ = 2.2V		0.2	1.0	μA
Digital Pins							
V_{IH}	8, 17, 20, 22	High Level Input Voltage		2			V
V_{IL}	8, 17, 20, 22	Low Level Input Voltage				0.8	V
I_{IH}	8, 17, 20, 22	High Level Input Current	V_{5V} = Max, V_I = 2.7V			20	μA
I_{IL}	8, 17, 20, 22	Low Level Input Current	V_{5V} = Max, V_I = 0.5V		140	200	μA
V_{OH}	12	High Level Output Voltage	V_{5V} = Min, I_{OH} = –400μA (Note 2)	2.4			V
V_{OL12}	12	Low Level Output Voltage	V_{5V} = Min, I_{OL} = 800μA (Note 2)			0.5	V
I_{LH}	11	High Level Output Leakage Current	$V_{PIN\ 11}$ = V_{CC} Measure Current into Pin 11			50	μA
V_{OL11}	11	Low Level Output Voltage	$I_{PIN\ 11}$ = 800 μA			0.5	V
Servo Channel							
Z_{DIS}	18, 19	Discharge Impedance	$V_{PIN\ 22}$ = 2V (discharge) Force 2.5V on Pins 18 or 19	0.5	1.8	2.5	KΩ
V_{BOQ}	15, 16	Buffer Quiescent Output Level	$V_{PIN\ 17, 20, 22}$ = 0.4V, V_{CI} = 0V Pull 0mA from Pins 15 and 16	1.0	1.6	2.0	V
$V_{LEVEL\ Q}$	24	Level Quiescent Output Level	V_{CI} = 0V Pull 200μA from Pin 24		0.2	0.5	V
I_L	18, 19	Gated Off Leakage Current	$V_{PIN\ 22}$ = 0.4V, $V_{PIN\ 20}$ = $V_{PIN\ 17}$ = 2V Force 3V on Pin 18 or Pin 19	–1		1	μA

ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions.
Set Hysteresis = 0V, $V_{PIN\ 17}$ = 2V, READ/WRITE = 0.4V, $V_{PIN\ 22}$ = 0.4V, unless otherwise noted.

Symbol	Pins	Parameter	Conditions	Min	Typ	Max	Units
Servo Channel (Continued)							
V_{OSBO}	16, 15	Buffer Output Offset Voltage for V_{CI} = $1V_{PK-PK}$	$V_{PIN\ 17, 20, 22}$ = 0.4V, $V_{PIN\ 1}$ = 2.75V Pull 0mA from Pins 15 and 16 $V_{PIN\ 4}$ = 2.25V, V_{OSBO} = $V_{PIN\ 16}$ – $V_{PIN\ 15}$		2	±15	mV
V_{OSYS}	25, 21	System Output Offset Voltage for V_{CI} = $0.75V_{PK-PK}$ Pull 0mA from Pin 25 V_{OSYS} = $V_{PIN\ 25}$ – $V_{PIN\ 21}$	$V_{PIN\ 17, 20, 22}$ = 0.4 $V_{PIN\ 1}$ = 2.688V, $V_{PIN\ 4}$ = 2.313V		±5	±20	mV
A_{VDA} (1V)	25, 21	Difference Amplifier Gain, 1V Differential Input	$V_{PIN\ 17, 20}$ = 2V $V_{PIN\ 19}$ = 1.5V, $V_{PIN\ 18}$ = 2.5V, $V_{PIN\ 22}$ = 0.4V	1.6	2	2.4	V/V
A_{VDA} (.5V)	25, 21	Difference Amplifier Gain, 0.5V Differential Input	$V_{PIN\ 17, 20}$ = 2V $V_{PIN\ 19}$ = 1.75V, $V_{PIN\ 18}$ = 2.25V, $V_{PIN\ 22}$ = 0.4V	1.6	2	2.4	V/V
GL_{DA}	25	Difference Amplifier Gain Linearity			0.2	2.5	%
Z_{LEVEL} SOURCE	24	Level Out Output Impedance	$V_{PIN\ 17, 20, 22}$ = 0.4V, V_{CI} = 0.75V Measure $V_{PIN\ 24}$ with 200μA and 3mA pulled out of the pin. Z_{LEVEL} = change in $V_{PIN\ 24}$ SOURCE 3mA – 0.2mA	100	180	250	Ω
AV_{GD} (1.5V)	15, 16	Gated Detector Gain for V_{CI} = $1.5V_{PK-PK}$	$V_{PIN\ 22, 20, 17}$ = 0.4V $V_{PIN\ 1}$ = 2.875V, $V_{PIN\ 4}$ = 2.125V	1.45	1.8	2.25	V/V
AV_{GD} (0.75V)	15, 16	Gated Detector Gain for V_{CI} = $0.75V_{PK-PK}$	$V_{PIN\ 22, 20, 17}$ = 0.4V $V_{PIN\ 1}$ = 2.688V, $V_{PIN\ 4}$ = 2.313V	1.45	1.7	2.25	V/V
AV_{LEVEL} (1.5V)	24	Level Voltage Gain For V_{CI} = $1.5V_{PK-PK}$	$V_{PIN\ 1}$ = 2.875V, $V_{PIN\ 4}$ = 2.125V	1.45	1.8	2.25	V/V
AV_{LEVEL} (0.75V)	24	Level Voltage Gain For V_{CI} = $0.75V_{PK-PK}$	$V_{PIN\ 1}$ = 2.687V, $V_{PIN\ 4}$ = 2.312V	1.6	1.9	2.4	V/V
GL_{GD}	15, 16	Gated Detector Gain Linearity			±0.1	±2.5	%
I_{CC}	9	V_{CC} Supply Current	V_{CC} = Max	40	90	110	mA
V_{REF}	21	V_{REF} Voltage		2.0	2.25	2.5	V

AC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Temperature and Supply Range refer to AC Test Setup.
f = 2.5MHz unless otherwise indicated. PKA, PKB = 1KΩ + 10nF to GND.

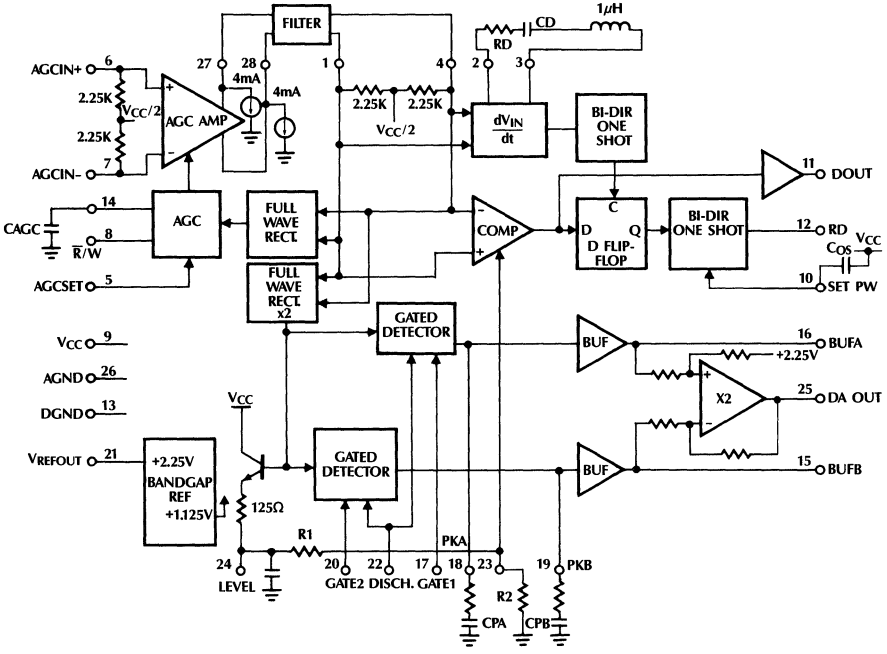
Symbol	Pins	Parameter	Conditions	Min	Typ	Max	Units
t_{CHARGE}	15, 16	Gated Detector Charge Time	V_{CI} = 1.5V_{PP}, $V_{PIN\ 22}$ = 0.3V, With PKA and PKB discharged, measure the time from Pin 17 or 20 going from 2V to 0.3V, to V_{BO1} or V_{BO2} respectively, reaching 90% of their final value		1.0		µs
$t_{DISCHARGE}$	15, 16	Gated Detector Discharge Time	V_{CI} = 1.5V_{PP}. With LP1 charged, measure the time from Pin 22 going from 0.3V to 2V, to the voltage at V_{BO1} or V_{BO2} reaching 90% of their final value		70		µs
t_{ON}	18, 19	Gated Detector Turn ON Time	V_{CI} = 0.35V_{DC}, $V_{PIN\ 22}$ = 0.3V. With LP1 discharged, measure the time from Pin 17 going from 2V to 0.3V, to the voltage on Pin 18 increasing 0.1V. Do a similar measurement with LP2, Pin 20 and Pin 19		0.2		µs
t_{OFF}	18, 19	Gated Detector Turn OFF Time	V_{CI} = 0.35V_{DC}, $V_{PIN\ 22}$ = 2V. Measure the time from Pin 17 going from 0.3V to 2V, to the voltage on Pin 18 decreasing by 0.1V. Do a similar measurement with Pins 20 and 19		0.4		µs
t_{PP}	12	Pulse Pairing ML4568-1	f = 2.5MHz and V_{CI} = 1V_{PP} differential			±1	ns
t_{PP}	12	Pulse Pairing ML4568-2	f = 2.5MHz and V_{CI} = 1V_{PP} differential			±3	ns

Notes:

1. The temperature coefficient of the input impedance is typically 0.05% per °C.
2. To prevent inductive coupling from the digital outputs to Amp In, the TTL outputs should not drive more than one ALS TTL load each. Pin 11 is an open collector output which is tested with an external 1K pullup resistor to the 5V supply.

ML4568 CONNECTION DIAGRAM

PLCC-28 Version



Note 1: K = R1/R2
Note 2: Hysterisis Level = 0.6 x $K/V_{IN\ P-P}$
Note 3: RC on pins PKA and PKB basically tuned to minimize ripple.

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APPLICATION INFORMATION

SETTING THE OUTPUT PULSEWIDTH

The RD output pulsewidth is dependent on the value of C_{OS}, which is connected from pin 10 to V_{CC}. This relationship is shown in figure 1.

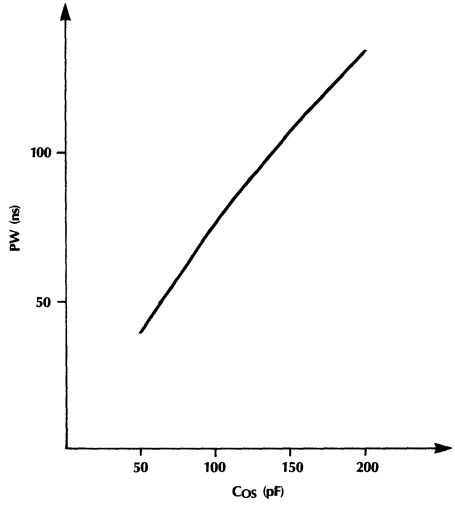


Figure 1. RD Output Pulsewidth as a Function of C_{OS}
$PW \simeq 0.5C_{OS}$

SELECTING C_D

The following table summarizes the maximum C_D value allowed for different data rates. These values are derived using

$$C_D \text{ (max)} = \frac{176}{f_{MAX}}, \; R_D = 0$$

Data Rate	f_{MAX}	C_D (max)
7.5 MB/s	2.81 MHz	62.6 pF
24 MB/s	9 MHz	19.6 pF

Table 1. Maximum C_D Value Allowed for a 1.5 V_{P-P} Differential Signal Using RLL (1, 7) Code

	1, 7 RLL	2, 7 RLL
f_{MAX}	3/8 x Data Rate	1/3 x Data Rate
f_{MAX}	3/32 x Data Rate	1/8 x Data Rate

Table 2.

ORDERING INFORMATION

PART NUMBER	PACKAGE	PULSE PAIRING
ML4568-1CQ	MOLDED PCC (Q28)	±1 ns
ML4568-2CQ	MOLDED PCC (Q28)	±3 ns

ML4610R, ML4611R

5V, 2-, 4-Channel Thin-Film Read/Write Circuit

GENERAL DESCRIPTION

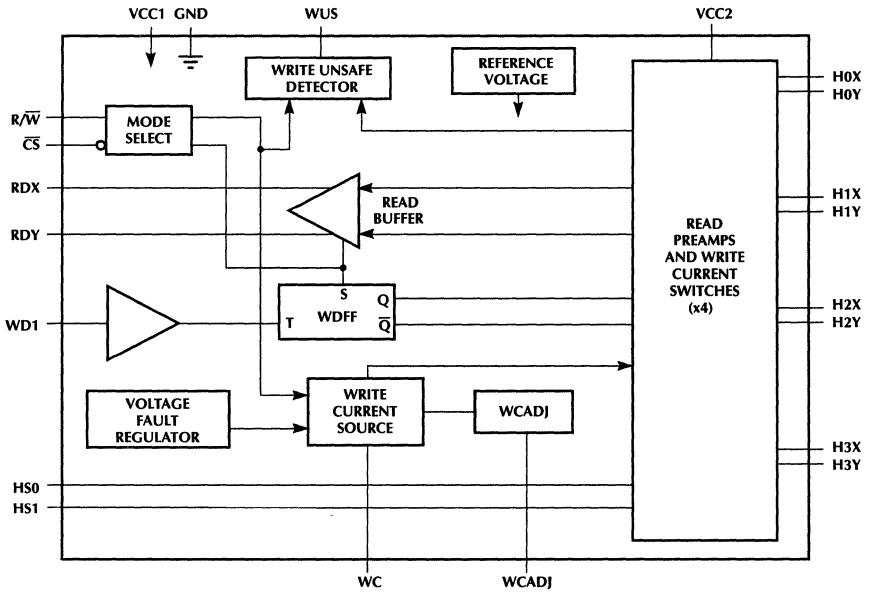
The ML4610R/4611R is a bipolar monolithic read/write circuit designed for use with two-terminal thin-film recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to four channels. The ML4610R/4611R incorporates internal 700 ohm damping resistors which dampen the write signals to the disk. When the device is switched to read mode, the damping resistor is switched out to allow the full signal to be amplified. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The ML4611R option also provides an user controllable write current adjustment capability, available in the 24-Pin package only.

FEATURES

- Compatible to SSIs 32R4610R/4611R
- Can drop into SSIs 32R2020R series sockets
- Single +5 volt operation
- Low Power, P_{IDLE} < 50mW, P_{MAX} < 200mW
- Read Mode gain = 200V/V
- Damping resistors switched out in Read mode
- Input noise = 0.85nV/$\sqrt{Hz}$ max
- Input capacitance = 35pF max
- Write Current range = 10–35mA
- Programmable write current source
- Enhanced system write to read recovery time
- Power supply fault protection
- Head short to ground protection
- 24-pin SOIC (4 channel with WCADJ)
- 20-pin SOIC (4 channel without WCADJ)
- 16-pin SOIC (2 channel without WCADJ)

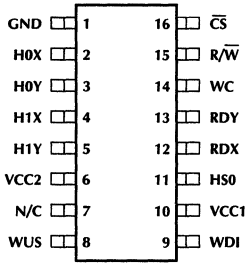
5

BLOCK DIAGRAM



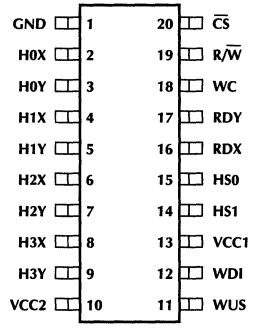
PIN CONNECTION

ML4610R-2CS (S16W)



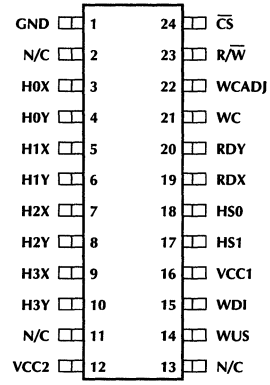
TOP VIEW

ML4610R-4CS (S20W)



TOP VIEW

ML4611R-4CS (S24W)



TOP VIEW

PIN DESCRIPTION

NAME	TYPE	FUNCTION
HS0, HS1	I	Head Select: Selects one of four heads
$\overline{CS}$	I	Chip Select: A high inhibits the chip
R/$\overline{W}$	I	Read/Write: A high selects read mode
WUS	O	Write Unsafe: A high indicates an unsafe writing condition
WDI	I	Write Data In: Changes the direction of the current in the head
H0X - H3X H0Y - H3Y	I/O	X,Y Head Connectors

NAME	TYPE	FUNCTION
RDX, RDY	O	X, Y Read Data: Differential read data output
WC		Write Current: Used to set the magnitude of the write current
WCADJ		Write Current Adjust: Used to decrease the write current
VCC1	I	+5 volt supply
VCC2	I	+5 volt supply for write current drivers
GND	I	Ground

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage ($V_{CC}1$) .....–0.3 to +7VDC
DC Supply Voltage ($V_{CC}2$) .....–0.3 to +7VDC
Write Current (I_W) 80mA
Digital Input Voltage (V_{IN}) .....–0.3 to VCC1 + 0.3VDC
Head Port Voltage (V_H) .....–0.3 to VCC1 + 0.3VDC
Output Current: (RDX, RDY I0) .....–10mA
Output Current: (WUS) .....+12mA
Storage Temperature T_{STG} .....–65 to +150°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage ($V_{CC}1$) .....5 ±5% VDC
DC Supply Voltage ($V_{CC}2$) .....5 ±5% VDC
Operating Junction Temperature (T_J) .....+25° to +110°C

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC}1$	Supply Current	Read Mode Write Mode Idle Mode			33 27 12	mA mA mA
$V_{CC}2$	Supply Current	Read Mode Write Mode Idle Mode			11 10 + I_W 0.4	mA mA mA
	Power Dissipation	Read Mode Write Mode Idle Mode			200 300 65	mW mW mW
DIGITAL INPUTS						
V_{IL}	Input Low Voltage				0.8	VDC
V_{IH}	Input High Voltage		2.0			VDC
	Input Low Current	V_{IL} = 0.8V	–0.4			mA
	Input High Current	V_{IH} = 2.0V			100	µA
V_{OL}	WUS Output Low Voltage	I_{OL} = 2 mA max			0.5	VDC
	VCC1 Fault Voltage	I_W < 0.2 mA	3.8	4.0	4.2	VDC
WRITE CHARACTERISTICS						
	Write Current Constant "K"			0.99		
V_{WC}	Write Current Voltage		1.15	1.25	1.35	V
	WCADJ Voltage	I_{WCADJ} = 0 to 0.5 mA	2.0	$V_{CC}/2$	3.0	VDC
	$I_{HEAD\ (DECREASE)}$ / I_{WCADJ}		26	29	32	mA/mA
	I_{WCADJ} Range		0.0		0.5	mA
	Differential Head Voltage Swing		3.4	6		V_{P-P}
	Unselected Head Current				1	mA (pk)
	Head Differential Load Capacitance				25	pF
	Head Differential Load Resistance	R_D (ML4610R/4611R)	560	700	950	Ω
	WDI Transition Frequency	WUS = low	1.0			MHz
	Write Current Range (Iw)		10		35	mA

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ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ CHARACTERISTICS CL (RDX,RDY) < 20 pF, RL (RDX, RDY) = 1kΩ						
	Differential Voltage Gain	V_{IN} = 1mV_{P-P} @ 1MHz	160	200	240	V/V
	Voltage BW –1dB –3dB	|Zs| < 5Ω, V_{IN} = 1mV_{P-P}	 20 35			 MHz MHz
	Input Noise Voltage	BW = 15MHz, L_H = 0, R_H = 0		0.6	0.85	nV/√Hz
	Differential Input Capacitance	V_{IN} = 1mV_{P-P}, f = 5MHz		27	35	pF
	Differential Input resistance	V_{IN} = 1mV_{P-P}, f = 5MHz	1000			Ω
	Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5MHz	3			mV_{P-P}
	Common Mode Rejection Ratio	V_{IN} = 0 volts DC + 100mV_{P-P} @ 5MHz	45			dB
	Power Supply Rejection Ratio	100mV_{P-P} @ 5MHz on V_{CC}	40			dB
	Channel Separation	Unselected channels driven with V_{IN} = 0 volts DC + 100mV_{P-P}	45			dB
	Output Offset Voltage		–200		+200	mV
	Single-Ended Output Resistance	f = 5MHz			40	Ω
	Output Current	AC coupled load, RDX to RDY	1.4			mA
RDX, RDY	Common Mode Output		2.0	2.8	3.5	VDC
SWITCHING CHARACTERISTICS I_W = 20mA, R_H = 30Ω, L_H = 1µH, f_{DATA} = 5MHz						
R/$\overline{W}$	Read to Write	R/$\overline{W}$ to 90% of write current		0.1	1.0	µs
R/$\overline{W}$	Write to Read	R/$\overline{W}$ to 90% of 100mV Read signal envelope		0.5	1.0	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% of write current or 90% of 100mV, 10MHz		0.4	1.0	µs
$\overline{CS}$	Select to Unselect	$\overline{CS}$ to 10% of write current		0.4	1.0	µs
	HS0-1 to any head	To 90% of 100mV 10MHz Read signal envelope		0.2	1.0	µs
	WUS Safe to Unsafe (TD1) Unsafe to Safe (TD2)		 0.6	 2.0 0.2	 3.6 1.0	 µs µs
	Head Current: WDI to Ix - Iy (TD3) Asymmetry Rise/Fall Time	L_H = 0, R_H = 0 From 50% points WDI has 1ns rise/fall time 10% to 90% points			 32 1.0 12	 ns ns ns

TIMING DIAGRAM

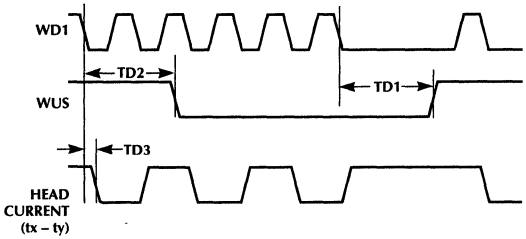

Figure 1. Write Mode.

MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

HEAD SELECT

HS1	HS0	HEAD
0	0	0
0	1	1
1	0	2
1	1	3

FUNCTIONAL DESCRIPTION

The ML4610R/4611R has the ability to address up to 4 two-terminal thin-film heads and provide write drive or read amplification. Head selection and mode control are described in the tables below. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0 and HS1 have internal pull-downs. Internal clamp circuitry will protect the ML4610R/4611R from a head short to ground condition in any mode. The damping resistors are switched out during read mode, as identified by the R/$\overline{W}$ pin.

WRITE MODE OPERATION

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the ML4610R/4611R as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). A preceding read or idle mode select initializes the Write Data Flip-Flop to pass write current through the "X" side of the head. The current calculations are shown below:

Write current (peak) is given by:

$$I_W = \frac{K \times VWC}{RWC}$$

where

RWC is connected from pin WC to GND

Actual head current is given by:

$$I_{X,\,Y} = \frac{I_W}{1 + \frac{R_H}{R_D}}$$

where

R_H = head + external wire resistance

R_D = damping resistance

The ML4610R/4611R adds a feature which allows the user to adjust the Iw current by a finite amount using the WCADJ pin, while writing to the disk. It is used by switching a separate write current adjust resistor in and out on the WCADJ pin or by connecting a DAC to that pin to sink a controllable amount of current. It is nominally biased to $V_{CC}/2$. Sinking current from this pin to ground, will divert a proportional amount of current from the actual head current while maintaining a constant current through the WC resistor and V_{CC}. Allowing WCADJ to float or pulling it high will cut off the circuit and it will have no effect. For example, if the nominal head current is set to 30mA through WC with WCADJ open, then for a

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7.25mA head current decrease, a 10kΩ resistor would be connected from the WCADJ pin to ground. A TTL gate could be used as a switch with a small degradation in accuracy. A DAC could be programmed to sink 0.25mA from the WCADJ pin, for achieving the same function.

$$I_W\ head\ (decrease) = \frac{29 \times V_{WCADJ}}{R_{WCADJ}}$$

where

V_{WCADJ} = Voltage on the WCADJ pin
R_{WCADJ} = Write current adjust setting resistor

VOLTAGE FAULT DETECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power start-up, regardless of mode. The Write Unsafe (WUS) open collector output goes high under the conditions given below. After the fault condition is removed, a negative transition on WDI is required to clear WUS.

— Write Data Input frequency too low

— Device in Read Mode

— Chip is disabled or head is open

— No write current

READ MODE OPERATION

The Read mode configures the ML4610R/4611R as a low noise differential amplifier and deactivates the write current generator. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs. In the Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/$\overline{W}$ applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. The write current source is also deactivated for both the Read and Idle mode. In addition the ML4610R/4611R supports the feature by which the internal damping resistors are switched out in the read mode, which allows the full signal to be amplified.

IDLE MODE OPERATION

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum, less than 50mW.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4610R-2CS	0°C to +70°C	16-Pin SOIC (S16W)
ML4610R-4CS	0°C to +70°C	20-Pin SOIC (S20W)
ML4611R-4CS	0°C to +70°C	24-Pin SOIC (S24W)

24 Mbps Read Channel Filter/Equalizer

GENERAL DESCRIPTION

The ML6005 is a monolithic analog filter/equalizer intended for hard disk drive read channel applications, capable of handling disk data rates upto 24Mbits/s, with an operating power dissipation of less than 300mW. Its architecture consists of a continuous type filter based on a transconductor and a high speed parasitic free active integrator, allowing complete independence of the filter response from interconnect parasitics, thus realizing a family of frequency response curves optimized for disk drive read channel equalization. It consists of a programmable 6-pole 2-zero lowpass filter stage, two pairs of high-speed drivers, and a serial microprocessor interface. The poles of the transfer function approximate a maximally flat group delay (Bessel) response, whereas the symmetric zeros provide the high-frequency boost necessary for pulse slimming. The user can independently adjust both the corner frequency, as well as the slimming level. The desired frequency response is programmed by a 14-bit serial input data stream which includes one bit for power-down, one bit for read/write control, and one bit for auto-zero control. The auto-zero circuitry, if enabled, reduces the output offsets to less than 20mV. The read/write control is also provided by a hardware pin. The ML6005 is well suited for constant density recording systems (Zoned-bit recording) as well as for constant data rate systems. A 36Mbits/s version, ML6006 is also available.

FEATURES

- 6-pole, 2-zero continuous time filter with < -45dB harmonic distortion
- Disk Data rates up to 24Mbit/s
- Programmable filter cutoff frequency
  (4.3:1 range in 64 steps)
  (f_c = 3.13 to 13.5MHz)
- 32 step programmable pulse slimming equalization, 0 to 10dB boost at f_c.
- Power-down, Auto-zero, R/W modes programmable through bits in the Control Register
- Lowpass output and Differentiated Lowpass (Bandpass) output provided.
- Fully I/O balanced architecture with TTL/CMOS compatible interface
- High speed (upto 25MHz clock) three wire serial microprocessor interface
- Double buffered data latch for synchronous or asynchronous data loading.
- Single 5V ± 10% power supply
- 0°C – 70°C operating temperature
- Available in 20-pin SSOP package.
- 4 GHz/1.5µ BiCMOS process
- Power Dissipation — P_{opr} = 300mW, P_{dn} = 7.5mW

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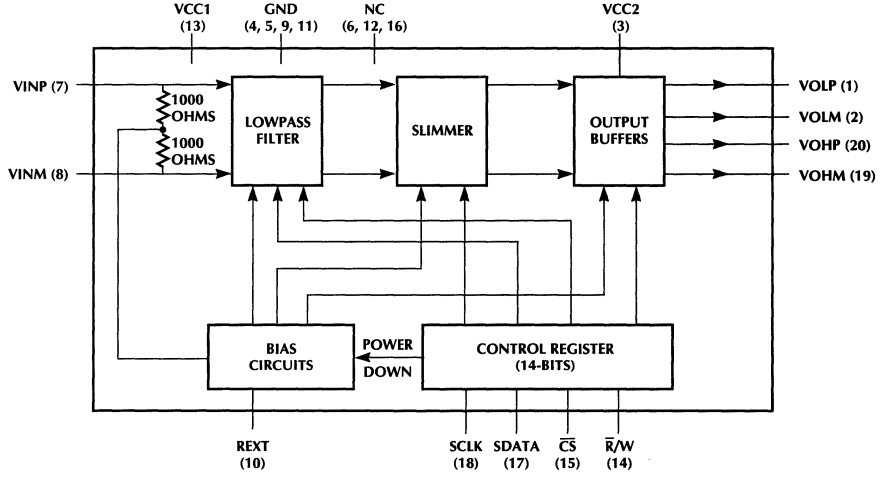
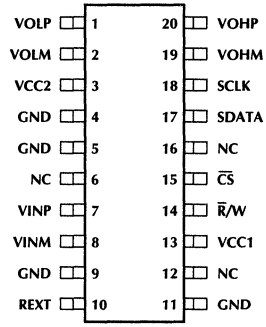
BLOCK DIAGRAM



PIN CONNECTION

20-Pin SSOP



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1 2	VOLP VOLM	Normal Lowpass outputs
3	VCC2	Positive supply for the output drivers, 5V ± 10%
4, 5, 9, 11	GND	Ground
7 8	VINP VINM	Signal Inputs
10	REXT	A 10K resistor between this pin and ground sets the filters corner frequency
13	VCC1	Positive supply, 5V ± 10%
14	$\overline{R}/W$	**Read/Write Control** pin. A low input level allows normal operation of the filter in the read mode. A high level input puts the filter in the write mode, where the input impedance is lowered to prevent the transients generated during write to read transitions from affecting the filter response. A TTL input. Additionally a metal mask option is available to configure this pin as either power down enable or frequency boost disable
15	$\overline{CS}$	**Control Register Enable**. A logical low level allows the SCLK input to clock data into the control register via the SDATA input line. A logical high level latches the control register contents and issues the information to the appropriate circuitry. A TTL input.
17	SDATA	**Control Register Data**. A TTL input
18	SCLK	**Control Register Clock**. Negative edge triggerred control register clock input. A TTL input.
19 20	VOHM VOHP	Differentiated lowpass outputs
6, 12, 16	NC	No Connects, reserved for future use.

ABSOLUTE MAXIMUM RATINGS

VCC1, VCC2 ..... +6.5 volts
VINP, VINM, REXT, $\overline{CS}$, SCLK,
SDATA, R/$\overline{W}$ ..... GND - 0.3V to VCC1 + 0.3V
VOLP, VOLM,
VOHP, VOHM ..... GND - 0.3V to VCC2 + 0.3V
Input Current per pin ..... ± 25 mA
Package Dissipation
at Ta = 25°C (Surface Mount) ..... 1.5 Watts
Junction Temperature ..... +150°C
Storage Temperature ..... -65°C to +150°C

OPERATING CONDITIONS

VCC1 = VCC2 ..... + 5 volts ± 10%
VIN = (VINP-VINM) ..... 1 Vp-p
Rext ..... 10 Kohms
Serial Clock Frequency (SCLK) ..... < 25 MHz
AC Coupling Capacitors ..... > 0.0001 µF

ELECTRICAL CHARACHTERISTICS

The following specifications apply over the recommended operating conditions, unless otherwise stated. Please refer to the application/test setup digram:

VCC1 = VCC2 = 5 volt ± 10%, Ta = 0°C to 70°C, Rext = 10 Kohms
VIN = (VINP - VINM) = 1 Vp-p sinewave input
VOL = (VOLP - VOLM) and VOH = (VOHP - VOHM)
Input and Output coupling capacitors = 0.0047 µF
RB1 = 750 ohms (pins 1 & 2), RB2 = 750 ohms (pins 19 & 20)
RL = 1000 (1000) ohms and CL = 50 (50) pF on pins 1 (19) and 2 (20)
Serial Clock Frequency = 20 MHz, Power Down, Auto Zero, Read/Write bits = 0
Digital timing measured at 1.4V midpoint
Input control signals from 10% - 90% of VCC1 with ($t_r = t_f$) < 5 ns.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
DC CHARACTERISTICS						
I_{CC}	VCC Supply Current	RB1 = RB2 = INF		60	74	mA
Ipd	Standby Current	VIN = 0		1.5	2	mA
DIGITAL INPUT CHARACTERISTICS (SCLK, SDATA, $\overline{CS}$)						
VIL	Low Voltage				0.8	V
VIH	High Voltage		2.0			V
IIH	High Current				1.0	µA
IIL	Low Current				-1.0	µA
CIN	Input Current			5		pF
DIGITAL TIMING CHARACTERISTICS (SCLK, SDATA, $\overline{CS}$)						
t_{PW}-$\overline{CS}$	Width of $\overline{CS}$, High/Low		25			ns
t_{SU}-SDATA	SDATA Setup time to SCLK		15			ns
t_H-SDATA	SDATA Hold Time		5			ns
t_{SU}-$\overline{CS}$	$\overline{CS}$ Setup Time to SCLK		15			ns
t_H-$\overline{CS}$	$\overline{CS}$ Hold Time to SCLK		0			ns
t_{PH}-SCLK	SCLK Pulse Width		20			ns
t_H-SCLK	$\overline{CS}$ Inactive to SCLK Active		125			ns

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ELECTRICAL CHARACHTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
EQUALIZER (NORMAL AND LOWPASS OUTPUT)						
AG	Absolute Gain	S0-S4 = 0, F0-F5 = 0 at 1MHz	-1.5	-0.5	0.5	dB
CF	Cutoff Frequency, -3dB (f_{ref} = 1MHz)	S0-S4 = 0, (-3dB slimming) F5 F4 F3 F2 F1 F0 (f_C)				
		0 0 0 0 0 0	12.15	13.50	14.85	MHz
		0 0 0 0 0 1	11.54	12.82	14.10	MHz
		0 0 0 0 1 0	11.04	12.27	13.50	MHz
		0 0 0 1 0 0	10.13	11.25	12.38	MHz
		0 0 1 0 0 0	8.68	9.64	10.60	MHz
		0 1 0 0 0 0	6.75	7.50	8.25	MHz
		1 0 0 0 0 0	4.67	5.19	5.71	MHz
		1 1 1 1 1 1	2.82	3.13	3.44	MHz
SL	Slimming Level (Gain at CF Referred to AG, Vout = 1Vp-p	F0-F5 = 0; at CF S4 S3 S2 S1 S0				
		0 0 0 0 1	-1.4	-2.4	-3.4	dB
		0 0 0 1 0	-0.9	-1.9	-2.9	dB
		0 0 1 0 0	-0.0	-0.9	-1.9	dB
		0 1 0 0 0	-0.2	0.8	1.8	dB
		1 0 0 0 0	2.4	3.4	4.4	dB
		1 1 1 1 1	5.9	6.9	7.9	dB
GD	Diff Group Delay	Fref = 5.0MHz, F0-F5 = 0	-1		+1	ns
HD	Harmonic Distortion Second and Third related to Fundamental	F0-F5 = 0, Vout = 1.5Vp-p, Fin = 9.0MHz S0-S4 = 0 (no slimming) S0-S4 = 1 (full slimming)			-45 -40	dB dB
ICN	Idle Channel Noise (VIN = 0, DC – 78MHz)	F0-F5 = 0, VOLP S0-S4 = 0 (no slimming) S0-S4 = 1 (full slimming)			2 6	mVrms mVrms
DR	Dynamic Range (Signal/(Noise + Distor)) Signal = 1Vp-p	F0-F5 = 0, Fin = 13.5MHz S0-S4 = 0 (no slimming) S0-S4 = 1 (full slimming)			-41 -35	dB dB
PSRR	Power Supply Rejection	100mVp-p sinewave on Vcc F0-F5 = 0, S0-S4 = 0, Vin = 0 Fin = 1.0MHz Fin = 40MHz		 40 30		 dB dB
DELP HI	Phase Shift between LP and HP Output	All F's and S's = 0 Vin = 1Vp-p, Fin = 9.0MHz	88	90	92	Degree
ANALOG						
VIP	Input Signal Monotonicity	All F's and S's = 0, (VINP - VINM) Fin = 9.0MHz		 1	 2	 Vp-p
RID	Differential Input Resistance	VIN = 100mVp-p at 6.7MHz	1.3	2	3	Kohms
CID	Differential Input Capacitance	VIN = 100mVp-p at 6.7MHz		5		pF
ZIC	Common-mode Input Impedence			1		Kohms
RPD	Recovery from Pwr Dn	Auto Zero function OFF Auto Zero function ON		10 TBD		µs
VOS	Output Offset Voltage	Differential VOLP or VOHP Auto Zero ON (S0-S4 = 0 or 1) Auto Zero OFF (S0-S4 = 0) Auto Zero OFF (S0-S4 = 1)			 20 300 TBD	 mV mV mV

ELECTRICAL CHARACHTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
ANALOG (Continued)						
ROD	Output Resistance	Differential VIN = 0; at 6.7MHz		5		Ohms
COD	Output Capacitance	Differential VIN = 0; at 6.7 MHz		8		pF
ROC	Output Resistance Common Mode	Common mode VIN = 0; at 6.7MHz		5		Ohms
COC	Output Capacitance Common Mode	Common mode VIN = 0; at 6.7MHz		15		pF
CLSE	Load Capacitance	VOLP; RB1 = 750 ohms VOHP; RB2 = 750 ohms			50 50	pF pF
RLSE	Load Resistance	VOLP VOHP	400 400			Ohms Ohms
RLOZ	Input Resistance	Diff; PD and/or RW bit = 1			350	Ohms
I_{OB}	Output Buffer Bias Current	VOLP or VOHP, VOLM or VOHM	1	1.4		mA
I_{OSC}	Short Circuit Output Current	VOLP or VOHP, VOLM or VOHM		50	100	mA
SBA	Stopband Attenuation	S0 = 0 at 2CF	TBD			dB

FUNCTIONAL DESCRIPTION

INTRODUCTION

Many of the high-frequency continuous-time filters have principally utilized a basic integrator consisting of a transconductance stage driving a passive integrating capacitor. These approaches are susceptible to frequency response variations due to the parasitic capacitances associated with the parasitic-sensitive output nodes of the integrator. This type of transconductance stage also often has low open-circuit voltage gain, resulting in limited practical Q range in the filter. The use of an active parasitic-insensitive integrator, has generally been avoided in these filters because of the additional excess phase that the amplifier contributes.

The ML6005 is a continuous-time filter based on a transconductor and a high-speed parasitic free active integrator, allowing complete independence of the filter response from interconnect parasitics and a very wide range of realizable filter Q. A unique approach to cancelling the excess phase contributed by the hi-speed BiCMOS amplifier allows this filter to achieve reproducible responses at 13.5 MHz filter bandwidth in a 1.5µ/4GHz BiCMOS process. This active integrator incorporates a novel technique for setting the transconductance Gm value as a function of an external precision resistor, independent of temperature, supply, in conjunction with a wafer-sort trim technique to adjust capacitor process tolerances, thus eliminating the need for an on-chip PLL for tuning.

The ML6005 filter consists of a 6th order Bessel low-pass and a 2nd order cosine equalizer stage. It is made up of three biquads with lowpass and bandpass outputs. Both outputs of the last stage are available with matched group-delay characteristics. The corner frequency is digitally programmable to 64 values over a 4 to 1 range, through the serial microprocessor interface. This is accomplished internally by changing the integrating capacitor value. Slimming equalization is done by digitally programming two real-symmetric zeroes, through the serial microprocessor interface. This boosts the high frequency response in 32 steps from 0 to 10 dB.

In a typical application, the ML6005 is used together with a pulse detector such as the ML541, ML4041 or the ML8464 , making up a section of the AGC loop. Thus, the output of the AGC amplifier is AC coupled to the ML6005 input and the output of the ML6005 is AC coupled not only to the rectifier input thus closing the AGC loop, but also to the pulse detector input. The ML6005 provides two sets of fully balanced outputs. The lowpass outputs and the differentiated lowpass outputs. The ML6005 input and output common mode voltage biases are generated on-chip. The ML6005 consists of an input common bias circuit, a programmable continuous type equalizer filter with normal and differentiated lowpass outputs, followed by output buffers, and a high speed serial microprocessor interface. The ML6005 processes only differential input signals, common mode inputs are rejected. The output should also be taken differentially in order to obtain the best performance.

INPUT COMMON MODE

The input common mode bias consists of two resistors as shown in the block diagram, and a buffer which biases the center point with a well defined voltage required by the internal circuitry. These resistors are 1000 Ohms each and together with the external coupling capacitor define the lower corner frequency of the transfer function.

EQUALIZER FILTER

The filter transfer function is composed of a second order numerator and a sixth order denominator. The low frequency attenuation is set internally to 0dB. The numerator realizes two zeros symmetrical symmetrical to the imaginary axis, one in the left and the other in the right half plane. The location of the zeros is programmable. This realizes a digitally programmable pulse slimming function in order to overcome intersymbol interference and thus contribute to increasing bit density. The slimming level is controlled by 5 bits in the control register, thus providing 32 different choices between 0 to 10 dB. The denominator approximately realizes a maximally flat group delay (Bessel) function with a digitally programmable corner frequency controlled by 6 bits in the control register, thus providing 64 different cutoff frequencies.

SLIMMING LEVEL

The slimming levels generated by the slimming bits are shown below. There are 5 bits of control, S0 - S4. The typical gain of the equalizer at the cutoff frequency is shown in the table below. The gain at f_c in dB is also given by the formula :

$$\text{Gain (dB)} = 20 \times \text{Log}\,(0.707 \times (1 + 0.06868 \times K))$$

where K = 0, 1, . . . 31

CUTOFF FREQUENCY

There are 6 bits in the control register that controls the position of the cutoff frequency, F0 - F5. The typical values of the cutoff (-3dB) frequency are shown in the table below for the case when S0 - S4=0 (no slimming). There are a total of 64 frequencies available from 13.5MHz down to 3.13MHz. Bits F1 - F5 will select one of 32 frequency settings in a monotonic fashion. Bit F0 is used to shift the whole frequency setting range by 5% lower than each of the 32 settings given by F1 - F5. This offers a scheme to increase the effective resolution of the cutoff frequency programmability. This feature is specially useful in the higher frequency range, where the granularity is coarse.

For example :

By setting F0 = 0,

Cutoff frequency = 13.50 MHz with F5 - F1 = 00000 and

Cutoff frequency = 12.27 MHz with F5 - F1 = 00001, the next consecutive setting.

Frequency delta between consecutive settings = 1.23 MHz or about 9% of 13.50 MHz.

By setting F0 = 1, we can shift the consecutive cutoff frequency settings as follows :

Cutoff frequency = 13.50 MHz with (F5 - F1, F0) = (00000, 0)

Cutoff frequency = 12.82 MHz with (F5 - F1, F0) = (00000, 1) Delta = 0.68 MHz

TABLE 1: TABLE OF SLIMMING LEVEL PROGRAMMING VALUES

S4	S3	S2	S1	S0	K	GAIN AT F_C (dB)	STEPS (dB)
0	0	0	0	0	0	- 3.0	
0	0	0	0	1	1	- 2.4	0.6
0	0	0	1	0	2	- 1.9	0.5
0	0	0	1	1	3	- 1.4	0.5
0	0	1	0	0	4	- 0.9	0.5
0	0	1	0	1	5	- 0.4	0.5
0	0	1	1	0	6	- 0.0	0.4
0	0	1	1	1	7	0.4	0.4
0	1	0	0	0	8	0.8	0.4
0	1	0	0	1	9	1.2	0.4
0	1	0	1	0	10	1.5	0.3
0	1	0	1	1	11	1.9	0.4
0	1	1	0	0	12	2.2	0.3
0	1	1	0	1	13	2.5	0.3
0	1	1	1	0	14	2.8	0.3
0	1	1	1	1	15	3.1	0.3
1	0	0	0	0	16	3.4	0.3
1	0	0	0	1	17	3.7	0.3
1	0	0	1	0	18	4.0	0.3
1	0	0	1	1	19	4.2	0.2
1	0	1	0	0	20	4.5	0.3
1	0	1	0	1	21	4.7	0.2
1	0	1	1	0	22	5.0	0.3
1	0	1	1	1	23	5.2	0.2
1	1	0	0	0	24	5.4	0.2
1	1	0	0	1	25	5.7	0.3
1	1	0	1	0	26	5.9	0.2
1	1	0	1	1	27	6.1	0.2
1	1	1	0	0	28	6.3	0.2
1	1	1	0	1	29	6.5	0.2
1	1	1	1	0	30	6.7	0.2
1	1	1	1	1	31	6.9	0.2

Cutoff frequency = 12.27 MHz with (F5 - F1, F0) = (00001, 0) Delta = 0.55 MHz

Hence frequency delta between consecutive settings is lower, thus higher resolution.

In the table 2 below, the cutoff frequencies are shown as two columns depending on the F0 bit being zero or one. The monotonicity is guaranteed within the individual frequency columns, however because of the limitations of the 5% frequency circuitry, the monotonicity between the two columns cannot be guaranteed. This is especially significant at the lower end of the frequency range, where the difference in frequencies between the two column settings becomes very close (< 1%). Further tuning of the cutoff frequency down to the 1 to 10% range can be achieved by modifying the value of the external resistor

from its ideal 10 Kohms value by 1 to 10%, which shifts the whole response. Larger changes are not recommended for proper operation of the filter. The corner frequency is given by the formula outlined below :

$$f_c = \left(\frac{13.5 \times (1 - F0 \times 0.05)}{[1 + 0.1 \times INT(N/2)]} \times \frac{10Kohms}{Rext} \right) MHz$$

OUTPUT BUFFER

The output buffer is the final stage of the ML6005 for both the normal and differentiated outputs. This is a fully differential buffer with unity gain. Only 1.4 mA of sinking current is provided on chip. More drive can be obtained by connecting external resistors to ground. The common mode output voltage is typically 2V.

SERIAL MICROPROCESSOR INTERFACE

The serial microprocessor interface consists of a simple three-wire serial port. It consists of a fourteen bit serial shift register with a double bufferred latch for synchronous and asynchronous loading. A timing diagram and the control word definition are shown below. The 14-bit data word present on the SDATA line is serially shifted into the register on falling edges of the serial shift clock, SCLK, provided the $\overline{CS}$ pin is active (logical zero). F0 should be shifted in first, and F13 (the power-down bit) shifted in last as shown below. When the $\overline{CS}$ pin is inactive (logical one), SDATA and SCLK are ignored, and the previously shifted information is latched at the rising edge of $\overline{CS}$ becoming inactive (logical one). It is reccommended that the SCLK input be kept inactive low till such time when it is in use. The SCLK input can run upto speeds of 25 MHz. The Autozero function, if enabled, minimizes the offsets at the filter outputs to 20mV.

TABLE 2: TABLE OF CUTOFF FREQUENCY PROGRAMMING VALUES IN MHZ

F5	F4	F3	F2	F1	N	f_c with F0 = 0	N	f_c with F0 = 1
0	0	0	0	0	0	13.5		
0	0	0	0	0			1	12.82
0	0	0	0	1	2	12.27		
0	0	0	0	1			3	11.66
0	0	0	1	0	4	11.25		
0	0	0	1	0			5	10.69
0	0	0	1	1	6	10.38		
0	0	0	1	1			7	9.87
0	0	1	0	0	8	9.64		
0	0	1	0	0			9	9.16
0	0	1	0	1	10	9.0		
0	0	1	0	1			11	8.55
0	0	1	1	0	12	8.44		
0	0	1	1	0			13	8.02
0	0	1	1	1	14	7.94		
0	0	1	1	1			15	7.54
0	1	0	0	0	16	7.50		
0	1	0	0	0			17	7.13
0	1	0	0	1	18	7.11		
0	1	0	0	1			19	6.75
0	1	0	1	0	20	6.75		
0	1	0	1	1	22	6.43		
0	1	0	1	0			21	6.41
0	1	1	0	0	24	6.14		
0	1	0	1	1			23	6.11
0	1	1	0	1	26	5.87		
0	1	1	0	0			25	5.83
0	1	1	1	0	28	5.63		
0	1	1	0	1			27	5.58
0	1	1	1	1	30	5.40		
0	1	1	1	0			29	5.34
1	0	0	0	0	32	5.19		
0	1	1	1	1			31	5.13
1	0	0	0	1	34	5.00		
1	0	0	0	0			33	4.93
1	0	0	1	0	36	4.82		
1	0	0	0	1			35	4.75
1	0	0	1	1	38	4.66		
1	0	0	1	0			37	4.58
1	0	1	0	0	40	4.50		
1	0	0	1	1			39	4.42
1	0	1	0	1	42	4.35		
1	0	1	0	0			41	4.28
1	0	1	1	0	44	4.22		
1	0	1	0	1			43	4.14
1	0	1	1	1	46	4.09		
1	0	1	1	0			45	4.01
1	1	0	0	0	48	3.97		
1	0	1	1	1			47	3.89
1	1	0	0	1	50	3.86		
1	1	0	0	0			49	3.77
1	1	0	1	0	52	3.75		
1	1	0	0	1			51	3.66
1	1	0	1	1	54	3.65		
1	1	0	1	0			53	3.56
1	1	1	0	0	56	3.55		
1	1	1	0	0			55	3.47
1	1	1	0	1	58	3.46		
1	1	1	0	0			57	3.38
1	1	1	1	0	60	3.38		
1	1	1	0	1			59	3.29
1	1	1	1	1	62	3.29		
1	1	1	1	0			61	3.21
1	1	1	1	1			63	3.13

Note: N is the decimal value of the cutoff frequency bits (F5 - F0), in the control register

TIMING DIAGRAM

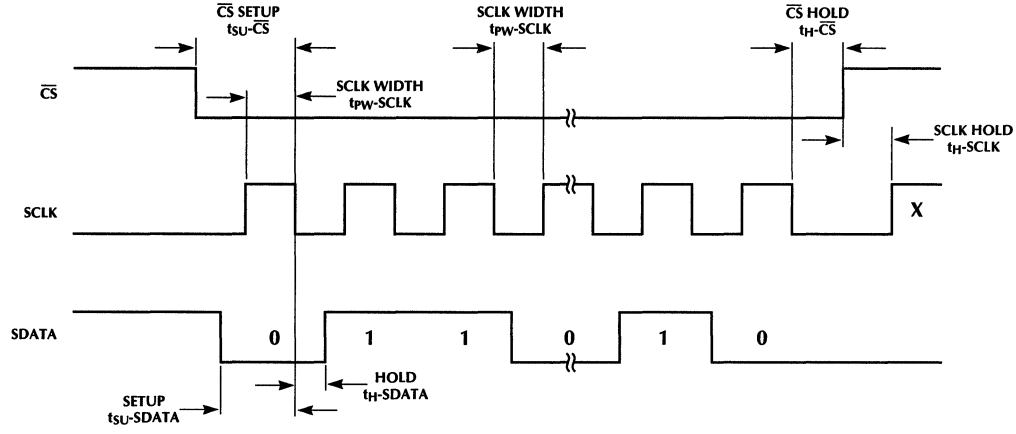


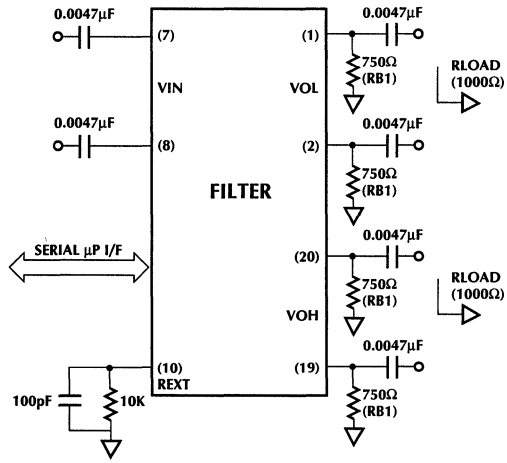
Figure 1.

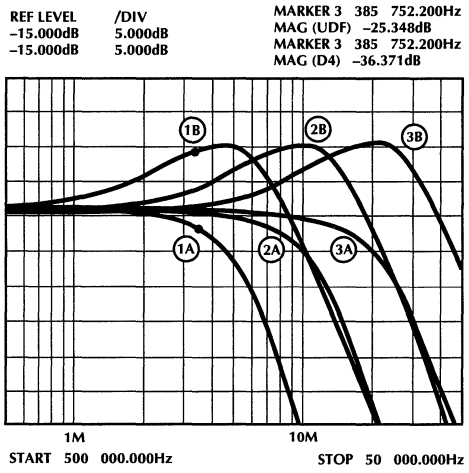
CONTROL REGISTER DEFINITION

F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
AZ	PD	R/W	SLIMMING CONTROL					FREQUENCY CONTROL					

AZ	AutoZero	1 = Autozero circuitry activated 0 = Autozero circuitry inactive
PD	Power Down	1 = Chip is in power down mode 0 = Chip is fully powered up
R/W	Read/Write	1 = Write data mode 0 = Read data mode

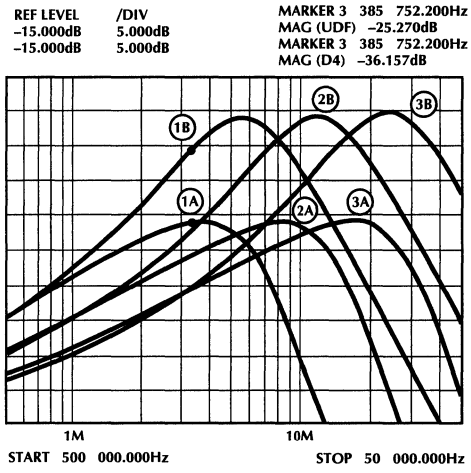
APPLICATIONS CIRCUIT/TEST SETUP





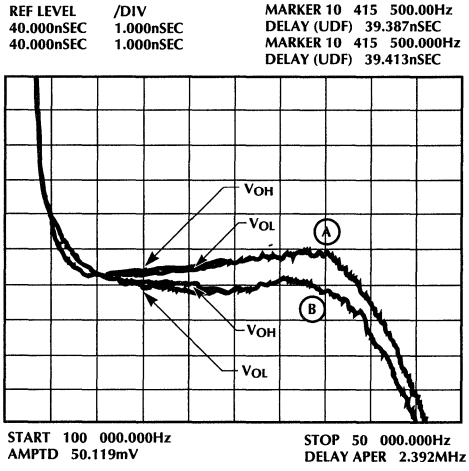
Filter Response (Lowpass Output)

Shown are the ML6005 filter response at three different cutoff frequency (f_C) settings. Setting 1 = 3.13 MHz, 2 = 6.75 MHz and 3 = 13.5 MHz. At each of the f_C settings, the filter response is shown with no slimming (A) and with full slimming (B) activated.



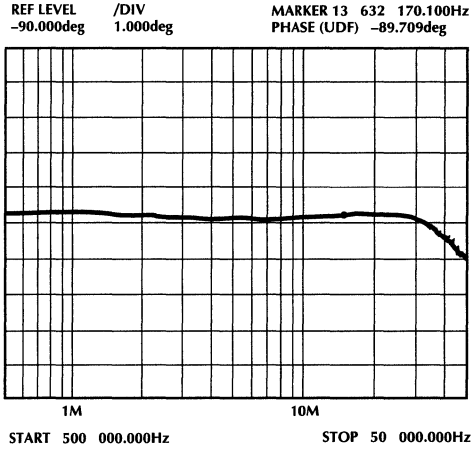
Filter Response (Bandpass Output)

Shown are the ML6005 filter response at three different cutoff frequency (f_C) settings. Setting 1 = 3.13 MHz, 2 = 6.75 MHz and 3 = 13.5 MHz. At each of the f_C settings, the filter response is shown with no slimming (A) and with full slimming (B) activated.



ML6005 Filter/Equalizer group Delay Tracking

Shown are the curves to demonstrate group delay tracking between the lowpass (V_{OL}) and bandpass (V_{OH}) outputs, at an f_C of 13.5 MHz, with on slimming activated (A) and full slimming activated (B). It can be seen that the group delay tracking between the lowpass and bandpass outputs is well within 1 ns.



Phase Difference between Lowpass and Bandpass Outputs

Shown is the delta in the phase between the lowpass and bandpass outputs. Ideally the bandpass output should be -90°. The curve shows that this is within 1° for a frequency range of 50 MHz to 10 MHz.

ML6005 FILTER/EQUALIZER CHARACTERISTICS

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6005CR	0°C to +70°C	20-Pin SSOP (R20)

36 Mbps Read Channel Filter/Equalizer

GENERAL DESCRIPTION

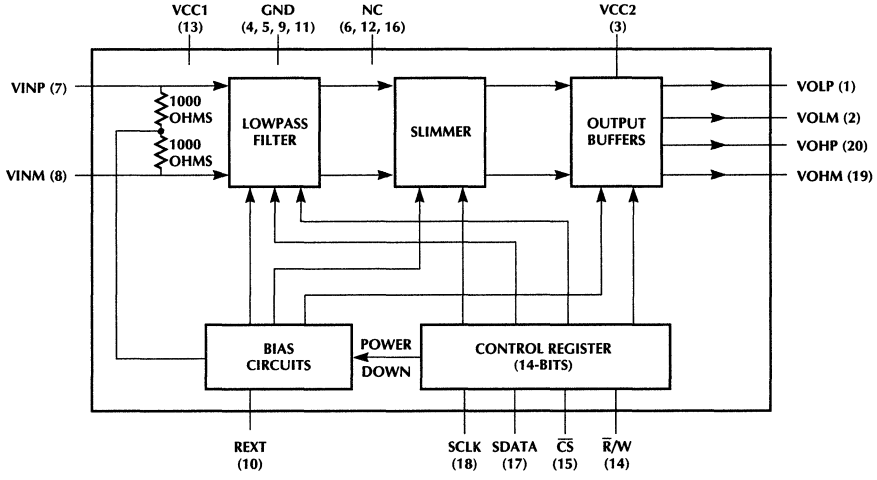
The ML6006 is a monolithic analog filter/equalizer intended for hard disk drive read channel applications, capable of handling disk data rates upto 36Mbits/s, with an operating power dissipation of less than 350mW. Its architecture consists of a continuous type filter based on a transconductor and a high speed parasitic free active integrator, allowing complete independence of the filter response from interconnect parasitics, thus realizing a family of frequency response curves optimized for disk drive read channel equalization. It consists of a programmable 6-pole 2-zero lowpass filter stage, two pairs of high-speed drivers, and a serial microprocessor interface. The poles of the transfer function approximate a maximally flat group delay (Bessel) response, whereas the symmetric zeros provide the high-frequency boost necessary for pulse slimming. The user can independently adjust both the corner frequency, as well as the slimming level. The desired frequency response is programmed by a 14-bit serial input data stream which includes one bit for power-down, one bit for read/write control, and one bit for auto-zero control. The read/write control is also provided by a hardware pin. The ML6006 is well suited for constant density recording systems (Zoned-bit recording) as well as for constant data rate systems. A 24 Mbits/s version, ML6005 is also available.

FEATURES

- 6-pole, 2-zero continuous time filter with < -45dB harmonic distortion
- Disk Data rates up to 36 Mbit/s
- Programmable filter cutoff frequency
  (4.3:1 range in 64 steps)
  (f_C = 4.69 to 20.25 MHz)
- 32 step programmable pulse slimming equalization, 0 to 10dB boost at f_C.
- Power-down, Auto-zero, R/W modes programmable through bits in the Control Register
- Lowpass output and Differentiated Lowpass (Bandpass) output provided.
- Fully I/O balanced architecture with TTL/CMOS compatible interface
- High speed (upto 25MHz clock) three wire serial microprocessor interface
- Double buffered data latch for synchronous or asynchronous data loading.
- Single 5V ± 10% power supply
- 0°C – 70°C operating temperature
- Available in 20-pin SSOP package.
- 4 GHz/1.5µ BiCMOS process
- Power Dissipation: P_{opr} = 350mW, P_{dn} = 7.5mW

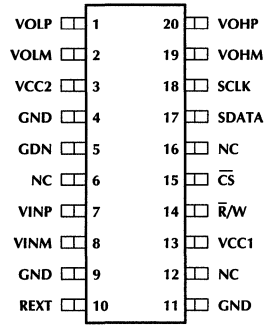
5

BLOCK DIAGRAM



PIN CONNECTION

20-Pin SSOP



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1 2	VOLP VOLM	Normal Lowpass outputs
3	VCC2	Positive supply for the output drivers, 5V ± 10%
4, 5, 9, 11	GND	Ground
7 8	VINP VINM	Signal Inputs
10	REXT	A 10K resistor between this pin and ground sets the filters corner frequency
13	VCC1	Positive supply, 5V ± 10%
14	R/W	**Read/Write Control** pin. A low input level allows normal operation of the filter in the read mode. A high level input puts the filter in the write mode, where the input impedance is lowered to prevent the transients generated during write to read transitions from affecting the filter response. A TTL input. Additionally a metal mask option is available to configure this pin as either power down enable or frequency boost disable
15	CS	**Control Register Enable**. A logical low level allows the SCLK input to clock data into the control register via the SDATA input line. A logical high level latches the control register contents and issues the information to the appropriate circuitry. A TTL input.
17	SDATA	**Control Register Data**. A TTL input
18	SCLK	**Control Register Clock**. Negative edge triggerred control register clock input. A TTL input.
19 20	VOHM VOHP	Differentiated lowpass outputs
6, 12, 16	NC	No Connects, reserved for future use.

ABSOLUTE MAXIMUM RATINGS

VCC1, VCC2 ..... +6.5 volts
VINP, VINM, REXT, ~CS, SCLK,
SDATA, ~R/W ..... GND - 0.3V to VCC1 + 0.3V
VOLP, VOLM,
VOHP, VOHM ..... GND - 0.3V to VCC2 + 0.3V
Input Current per pin ..... ± 25 mA
Package Dissipation
at Ta = 25°C (Surface Mount) ..... 1.5 Watts
Junction Temperature ..... +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... 260°C

OPERATING CONDITIONS

VCC1 = VCC2 ..... + 5 volts ± 10%
VIN = (VINP-VINM) ..... 1 Vp-p
Rext ..... 10 Kohms
Serial Clock Frequency (SCLK) ..... < 25 MHz
AC Coupling Capacitors ..... > 0.0001 µF

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions, unless otherwise stated. Please refer to the application/test setup digram:

VCC1 = VCC2 = 5 volt ± 10%, T_a = 0°C to 70°C, Rext = 10 Kohms
VIN = (VINP - VINM) = 1 Vp-p sinewave input
VOL = (VOLP - VOLM) and VOH = (VOHP - VOHM)
Input and Output coupling capacitors = 0.0047 µF
RB1 = 750 ohms (pins 1 & 2), RB2 = 750 ohms (pins 19 & 20)
RL = 1000 (1000) ohms and CL = 50 (50) pF on pins 1 (19) and 2 (20)
Serial Clock Frequency = 20 MHz, Power Down, Auto Zero, Read/Write bits = 0
Digital timing measured at 1.4V midpoint
Input control signals from 10% - 90% of VCC1 with (t_r = t_f) < 5 ns.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
DC CHARACTERISTICS						
I_{CC}	VCC Supply Current	RB1 = RB2 = INF		70	84	mA
Ipd	Standby Current	VIN = 0		1.5	2	mA
DIGITAL INPUT CHARACTERISTICS (SCLK, SDATA, $\overline{CS}$)						
VIL	Low Voltage				0.8	V
VIH	High Voltage		2.0			V
IIH	High Current				1.0	µA
IIL	Low Current				-1.0	µA
CIN	Input Current			5		pF
DIGITAL TIMING CHARACTERISTICS (SCLK, SDATA, $\overline{CS}$)						
t_{PW}-$\overline{CS}$	Width of $\overline{CS}$, High/Low		25			ns
t_{SU}-SDATA	SDATA Setup time to SCLK		15			ns
t_H-SDATA	SDATA Hold Time		5			ns
t_{SU}-$\overline{CS}$	$\overline{CS}$ Setup Time to SCLK		15			ns
t_H-$\overline{CS}$	$\overline{CS}$ Hold Time to SCLK		0			ns
t_{PH}-SCLK	SCLK Pulse Width		20			ns
t_H-SCLK	$\overline{CS}$ Inactive to SCLK Active		125			ns

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
EQUALIZER (NORMAL AND LOWPASS OUTPUT)						
AG	Absolute Gain	S0-S4 = 0, F0-F5 = 0 at 1MHz	-1.5	-0.5	0.5	dB
CF	Cutoff Frequency, -3dB (f_{ref} = 1MHz)	S0-S4 = 0, (-3dB slimming) F5 F4 F3 F2 F1 F0 (f_C)				
		0 0 0 0 0 0	18.23	20.25	22.28	MHz
		0 0 0 0 0 1	17.32	19.24	21.16	MHz
		0 0 0 0 1 0	16.57	18.41	20.25	MHz
		0 0 0 1 0 0	15.19	16.88	18.57	MHz
		0 0 1 0 0 0	13.01	14.46	15.91	MHz
		0 1 0 0 0 0	10.13	11.25	12.38	MHz
		1 0 0 0 0 0	7.01	7.79	8.57	MHz
		1 1 1 1 1 1	4.22	4.69	5.16	MHz
SL	Slimming Level (Gain at CF Referred to AG, Vout = 1Vp-p	F0-F5 = 0; at CF S4 S3 S2 S1 S0				
		0 0 0 0 1	-1.4	-2.4	-3.4	dB
		0 0 0 1 0	-0.9	-1.9	-2.9	dB
		0 0 1 0 0	-0.0	-0.9	-1.9	dB
		0 1 0 0 0	-0.2	0.8	1.8	dB
		1 0 0 0 0	2.4	3.4	4.4	dB
		1 1 1 1 1	5.9	6.9	7.9	dB
GD	Diff Group Delay	Fref = 7.5MHz, F0-F5 = 0	-1		+1	ns
HD	Harmonic Distortion Second and Third related to Fundamental	F0-F5 = 0, Vout = 1.5Vp-p, Fin = 13.5MHz				
		S0-S4 = 0 (no slimming)			-45	dB
		S0-S4 = 1 (full slimming)			-40	dB
ICN	Idle Channel Noise (VIN = 0, DC – 78MHz)	F0-F5 = 0, VOLP				
		S0-S4 = 0 (no slimming)			2	mVrms
		S0-S4 = 1 (full slimming)			6	mVrms
DR	Dynamic Range (Signal/(Noise + Distor)) (Signal = 1Vp-p)	F0-F5 = 0, Fin = 13.5MHz				
		S0-S4 = 0 (no slimming)			-41	dB
		S0-S4 = 1 (full slimming)			-35	dB
PSRR	Power Supply Rejection	100mVp-p sinewave on Vcc F0-F5 = 0, S0-S4 = 0, Vin = 0				
		Fin = 1.0MHz		40		dB
		Fin = 40MHz		30		dB
DELP HI	Phase Shift between LP and HP Output	All F's and S's = 0 Vin = 1Vp-p, Fin = 13.5MHz	88	90	92	Degree
ANALOG						
VIP	Input Signal Monotonicity	All F's and S's = 0, (VINP - VINM) Fin = 13.5MHz		1	2	Vp-p
RID	Differential Input Resistance	VIN = 100mVp-p at 10MHz	1.3	2	3	Kohms
CID	Differential Input Capacitance	VIN = 100mVp-p at 10MHz		5		pF
ZIC	Common-mode Input Impedence			1		Kohms
RPD	Recovery from Pwr Dn	Auto Zero function OFF		10		µs
		Auto Zero function ON		TBD		
VOS	Output Offset Voltage	Differential VOLP or VOHP				
		Auto Zero ON (S0-S4 = 0 or 1)			20	mV
		Auto Zero OFF (S0-S4 = 0)			300	mV
		Auto Zero OFF (S0-S4 = 1)			TBD	mV

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
ANALOG (Continued)						
ROD	Output Resistance	Differential VIN = 0; at 10MHz		5		Ohms
COD	Output Capacitance	Differential VIN = 0; at 10 MHz		8		pF
ROC	Output Resistance Common Mode	Common mode VIN = 0; at 10MHz		5		Ohms
COC	Output Capacitance Common Mode	Common mode VIN = 0; at 10MHz		15		pF
CLSE	Load Capacitance	VOLP; RB1 = 750 ohms VOHP; RB2 = 750 ohms			50 50	pF pF
RLSE	Load Resistance	VOLP VOHP	400 400			Ohms Ohms
RLOZ	Input Resistance	Diff; PD and/or RW bit = 1			350	Ohms
I_{OB}	Output Buffer Bias Current	VOLP or VOHP, VOLM or VOHM	1	1.4		mA
I_{OSC}	Short Circuit Output Current	VOLP or VOHP, VOLM or VOHM		50	100	mA
SBA	Stopband Attenuation	S0 = 0 at 2CF	TBD			dB

FUNCTIONAL DESCRIPTION

INTRODUCTION

Many of the high-frequency continuous-time filters have principally utilized a basic integrator consisting of a transconductance stage driving a passive integrating capacitor. These approaches are susceptible to frequency response variations due to the parasitic capacitances associated with the parasitic-sensitive output nodes of the integrator. This type of transconductance stage also often has low open-circuit voltage gain, resulting in limited practical Q range in the filter. The use of an active parasitic-insensitive integrator, has generally been avoided in these filters because of the additional excess phase that the amplifier contributes.

The ML6006 is a continuous-time filter based on a transconductor and a high-speed parasitic free active integrator, allowing complete independence of the filter response from interconnect parasitics and a very wide range of realizable filter Q. A unique approach to cancelling the excess phase contributed by the hi-speed BiCMOS amplifier allows this filter to achieve reproducible responses at 20 MHz filter bandwidth in a 1.5µ/4GHz BiCMOS process. This active integrator incorporates a novel technique for setting the transconductance Gm value as a function of an external precision resistor, independent of temperature, supply, in conjunction with a wafer-sort trim technique to adjust capacitor process tolerances, thus eliminating the need for an on-chip PLL for tuning.

The ML6006 filter consists of a 6th order Bessel low-pass and a 2nd order cosine equalizer stage. It is made up of three biquads with lowpass and bandpass outputs. Both outputs of the last stage are available with matched group-delay characteristics. The corner frequency is digitally programmable to 64 values over a 4 to 1 range, through the serial microprocessor interface. This is accomplished internally by changing the integrating capacitor value. Slimming equalization is done by digitally programming two real-symmetric zeroes, through the serial microprocessor interface. This boosts the high frequency response in 32 steps from 0 to 10 dB.

In a typical application, the ML6006 is used together with a pulse detector such as the ML541, ML4041 or the ML8464 , making up a section of the AGC loop. Thus, the output of the AGC amplifier is AC coupled to the ML6006 input and the output of the ML6006 is AC coupled not only to the rectifier input thus closing the AGC loop, but also to the pulse detector input. The ML6006 provides two sets of fully balanced outputs. The lowpass outputs and the differentiated lowpass outputs. The ML6006 input and output common mode voltage biases are generated on-chip. The ML6005 consists of an input common bias circuit, a programmable continuous type equalizer filter with normal and differentiated lowpass outputs, followed by output buffers, and a high speed serial microprocessor interface. The ML6005 processes only differential input signals, common mode inputs are rejected. The output should also be taken differentially in order to obtain the best performance.

INPUT COMMON MODE

The input common mode bias consists of two resistors as shown in the block diagram, and a buffer which biases the center point with a well defined voltage required by the internal circuitry. These resistors are 1000 Ohms each and together with the external coupling capacitor define the lower corner frequency of the transfer function.

EQUALIZER FILTER

The filter transfer function is composed of a second order numerator and a sixth order denominator. The low frequency attenuation is set internally to 0dB. The numerator realizes two zeros symmetrical symmetrical to the imaginary axis, one in the left and the other in the right half plane. The location of the zeros is programmable. This realizes a digitally programmable pulse slimming function in order to overcome intersymbol interference and thus contribute to increasing bit density. The slimming level is controlled by 5 bits in the control register, thus providing 32 different choices between 0 to 10 dB. The denominator approximately realizes a maximally flat group delay (Bessel) function with a digitally programmable corner frequency controlled by 6 bits in the control register, thus providing 64 different cutoff frequencies.

SLIMMING LEVEL

The slimming levels generated by the slimming bits are shown below. There are 5 bits of control, S0 - S4. The typical gain of the equalizer at the cutoff frequency is shown in the table below. The gain at f_c in dB is also given by the formula :

$$\text{Gain (dB)} = 20 \times \text{Log}\,(0.707 \times (1 + 0.06868 \times K))$$

where K = 0, 1, . . . 31

CUTOFF FREQUENCY

There are 6 bits in the control register that controls the position of the cutoff frequency, F0 - F5. The typical values of the cutoff (-3dB) frequency are shown in the table below for the case when S0 - S4=0 (no slimming). There are a total of 64 frequencies available from 20.25MHz down to 4.69MHz. Bits F1 - F5 will select one of 32 frequency settings in a monotonic fashion. Bit F0 is used to shift the whole frequency setting range by 5% lower than each of the 32 settings given by F1 - F5. This offers a scheme to increase the effective resolution of the cutoff frequency programmability. This feature is specially useful in the higher frequency range, where the granularity is coarse.

For example :

By setting F0 = 0,

Cutoff frequency = 20.25 MHz with F5 - F1 = 00000 and

Cutoff frequency = 18.41 MHz with F5 - F1 = 00001, the next consecutive setting.

Frequency delta between consecutive settings = 1.84 MHz or about 9% of 20.25 MHz.

By setting F0 = 1, we can shift the consecutive cutoff frequency settings as follows :

Cutoff frequency = 20.25 MHz with (F5 - F1, F0) = (00000, 0)

Cutoff frequency = 19.24 MHz with (F5 - F1, F0) = (00000, 1) Delta = 1.01 MHz

TABLE 1: TABLE OF SLIMMING LEVEL PROGRAMMING VALUES

S4	S3	S2	S1	S0	K	GAIN AT F_C (DB)	STEPS (DB)
0	0	0	0	0	0	- 3.0	
0	0	0	0	1	1	- 2.4	0.6
0	0	0	1	0	2	- 1.9	0.5
0	0	0	1	1	3	- 1.4	0.5
0	0	1	0	0	4	- 0.9	0.5
0	0	1	0	1	5	- 0.4	0.5
0	0	1	1	0	6	- 0.0	0.4
0	0	1	1	1	7	0.4	0.4
0	1	0	0	0	8	0.8	0.4
0	1	0	0	1	9	1.2	0.4
0	1	0	1	0	10	1.5	0.3
0	1	0	1	1	11	1.9	0.4
0	1	1	0	0	12	2.2	0.3
0	1	1	0	1	13	2.5	0.3
0	1	1	1	0	14	2.8	0.3
0	1	1	1	1	15	3.1	0.3
1	0	0	0	0	16	3.4	0.3
1	0	0	0	1	17	3.7	0.3
1	0	0	1	0	18	4.0	0.3
1	0	0	1	1	19	4.2	0.2
1	0	1	0	0	20	4.5	0.3
1	0	1	0	1	21	4.7	0.2
1	0	1	1	0	22	5.0	0.3
1	0	1	1	1	23	5.2	0.2
1	1	0	0	0	24	5.4	0.2
1	1	0	0	1	25	5.7	0.3
1	1	0	1	0	26	5.9	0.2
1	1	0	1	1	27	6.1	0.2
1	1	1	0	0	28	6.3	0.2
1	1	1	0	1	29	6.5	0.2
1	1	1	1	0	30	6.7	0.2
1	1	1	1	1	31	6.9	0.2

Cutoff frequency = 18.41 MHz with (F5 - F1, F0) = (00001, 0) Delta = 0.83 MHz

Hence frequency delta between consecutive settings is lower, thus higher resolution.

In the table 2 below, the cutoff frequencies are shown as two columns depending on the F0 bit being zero or one. The monotonicity is guaranteed within the individual frequency columns, however because of the limitations of the 5% frequency circuitry, the monotonicity between the two columns cannot be guaranteed. This is especially significant at the lower end of the frequency range, where the difference in frequencies between the two column settings becomes very close (< 1%). Further tuning of the cutoff frequency down to the 1 to 10% range can be achieved by modifying the value of the external resistor

from its ideal 10 Kohms value by 1 to 10%, which shifts the whole response. Larger changes are not recommended for proper operation of the filter. The corner frequency is given by the formula outlined below :

$$f_c = \left(\frac{20.25 \times (1 - F0 \times 0.05)}{[1 + 0.1 \times INT(N/2)]} \times \frac{10Kohms}{Rext} \right) MHz$$

OUTPUT BUFFER

The output buffer is the final stage of the ML6006 for both the normal and differentiated outputs. This is a fully differential buffer with unity gain. Only 1.4 mA of sinking current is provided on chip. More drive can be obtained by connecting external resistors to ground. The common mode output voltage is typically 2V.

SERIAL MICROPROCESSOR INTERFACE

The serial microprocessor interface consists of a simple three-wire serial port. It consists of a fourteen bit serial shift register with a double bufferred latch for synchronous and asynchronous loading. A timing diagram and the control word definition are shown below. The 14-bit data word present on the SDATA line is serially shifted into the register on falling edges of the serial shift clock, SCLK, provided the $\overline{CS}$ pin is active (logical zero). F0 should be shifted in first, and F13 (the power-down bit) shifted in last as shown below. When the $\overline{CS}$ pin is inactive (logical one), SDATA and SCLK are ignored, and the previously shifted information is latched at the rising edge of $\overline{CS}$ becoming inactive (logical one). It is reccommended that the SCLK input be kept inactive low till such time when it is in use. The SCLK input can run upto speeds of 25 MHz. The Autozero function, if enabled, minimizes the offsets at the filter outputs to 20mV.

TABLE 2: TABLE OF CUTOFF FREQUENCY PROGRAMMING VALUES IN MHZ

F5	F4	F3	F2	F1	N	f_c with F0 = 0	N	f_c with F0 = 1
0	0	0	0	0	0	20.25		
0	0	0	0	0			1	19.24
0	0	0	0	1	2	18.41		
0	0	0	0	1			3	17.49
0	0	0	1	0	4	16.88		
0	0	0	1	0			5	16.03
0	0	0	1	1	6	15.58		
0	0	0	1	1			7	14.80
0	0	1	0	0	8	14.46		
0	0	1	0	0			9	13.74
0	0	1	0	1	10	13.50		
0	0	1	0	1			11	12.83
0	0	1	1	0	12	12.66		
0	0	1	1	0			13	12.02
0	0	1	1	1	14	11.91		
0	0	1	1	1			15	11.32
0	1	0	0	0	16	11.25		
0	1	0	0	0			17	10.69
0	1	0	0	1	18	10.66		
0	1	0	0	1			19	10.13
0	1	0	1	0	20	10.13		
0	1	0	1	1	22	9.64		
0	1	0	1	0			21	9.62
0	1	1	0	0	24	9.20		
0	1	0	1	1			23	9.16
0	1	1	0	1	26	8.80		
0	1	1	0	0			25	8.74
0	1	1	1	0	28	8.44		
0	1	1	0	1			27	8.36
0	1	1	1	1	30	8.10		
0	1	1	1	0			29	8.02
1	0	0	0	0	32	7.79		

F5	F4	F3	F2	F1	N	f_c with F0 = 0	N	f_c with F0 = 1
0	1	1	1	1			31	7.70
1	0	0	0	1	34	7.50		
1	0	0	0	0			33	7.40
1	0	0	1	0	36	7.23		
1	0	0	0	1			35	7.12
1	0	0	1	1	38	6.98		
1	0	0	1	0			37	6.87
1	0	1	0	0	40	6.75		
1	0	0	1	1			39	6.63
1	0	1	0	1	42	6.53		
1	0	1	0	0			41	6.41
1	0	1	1	0	44	6.33		
1	0	1	0	1			43	6.21
1	0	1	1	1	46	6.14		
1	0	1	1	0			45	6.01
1	1	0	0	0	48	5.96		
1	0	1	1	1			47	5.83
1	1	0	0	1	50	5.79		
1	1	0	0	0			49	5.66
1	1	0	1	0	52	5.63		
1	1	0	0	1			51	5.50
1	1	0	1	1	54	5.47		
1	1	0	1	0			53	5.34
1	1	1	0	0	56	5.33		
1	1	1	0	0			55	5.20
1	1	1	0	1	58	5.19		
1	1	1	0	0			57	5.06
1	1	1	1	0	60	5.06		
1	1	1	0	1			59	4.93
1	1	1	1	1	62	4.94		
1	1	1	1	0			61	4.81
1	1	1	1	1			63	4.69

Note: N is the decimal value of the cutoff frequency bits (F5 - F0), in the control register

TIMING DIAGRAM

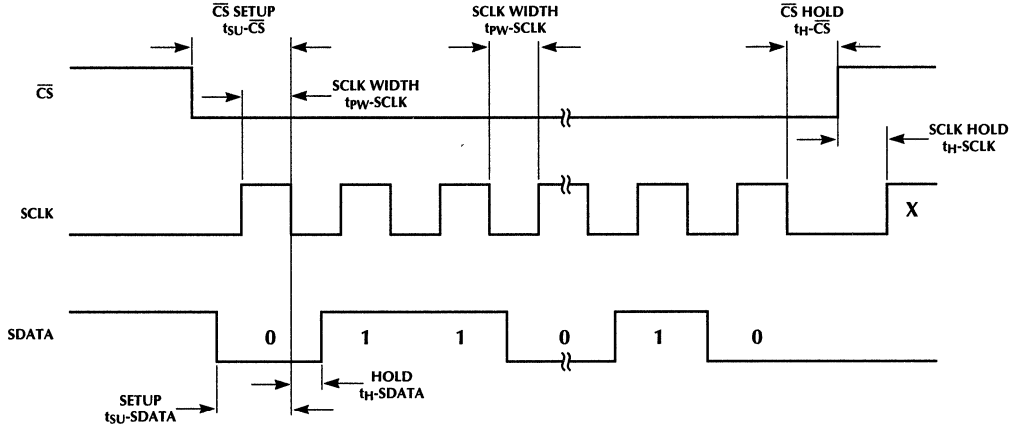


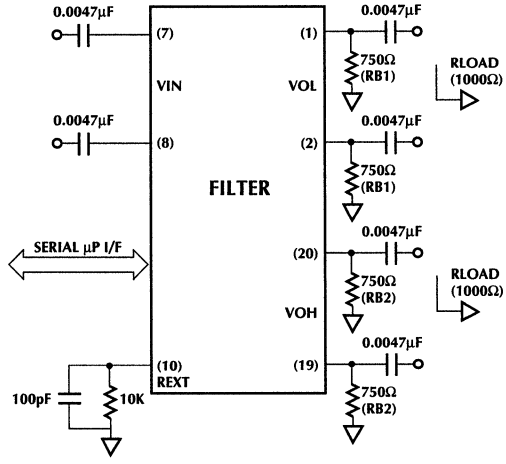
Figure 1.

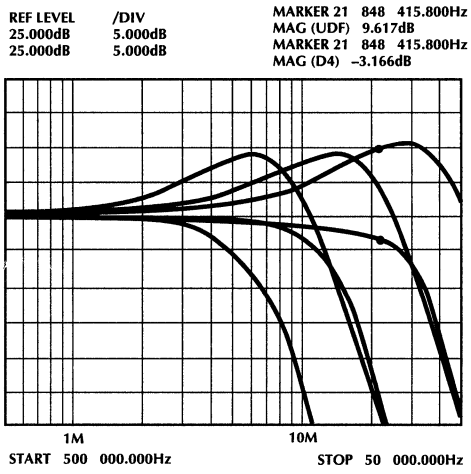
CONTROL REGISTER DEFINITION

F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
AZ	PD	RW	SLIMMING CONTROL					FREQUENCY CONTROL					

AZ	AutoZero	1 = Autozero circuitry activated 0 = Autozero circuitry inactive
PD	Power Down	1 = Chip is in power down mode 0 = Chip is fully powered up
$\overline{RW}$	Read/Write	1 = Write data mode 0 = Read data mode

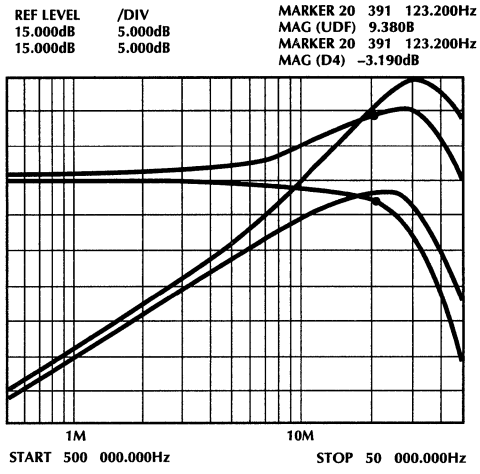
APPLICATIONS





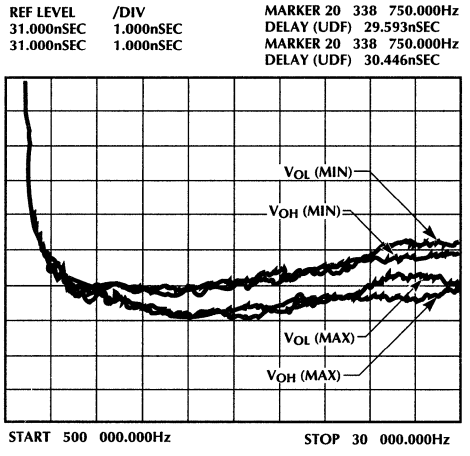
Filter Response (Lowpass Output)

Shown are the ML6006 filter response at three different cutoff frequency (f_c) settings. At each of the f_c settings, the filter response is shown with no slimming and with full slimming activated.



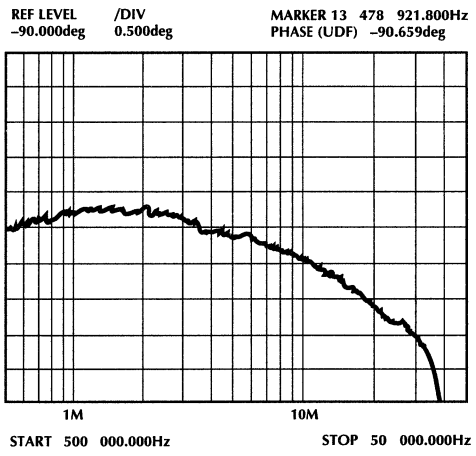
Filter Response (Lowpass and Bandpass Outputs)

Shown are the ML6006 filter characteristic curves for the lowpass and bandpass outputs, with no slimming and full slimming activated.



ML6006 Filter/Equalizer Group Delay Tracking

Shown are the curves to demonstrate group delay tracking between the lowpass (V_{OL}) and bandpass (V_{OH}) outputs, with no slimming activated (min) and full slimming activated (max). It can be seen that the group delay tracking between the lowpass and bandpass outputs is well within 1 ns.



Phase Difference between Lowpass and Bandpass Outputs

Shown is the delta in the phase between the lowpass and bandpass outputs. Ideally the bandpass output should be -90°. The curve shows that this is within 1° for a frequency range of 50 MHz to 10 MHz.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6005CR	0°C to +70°C	20-Pin SSOP (R20)

ML6010

Integrated Disk Read Channel Processor

GENERAL DESCRIPTION

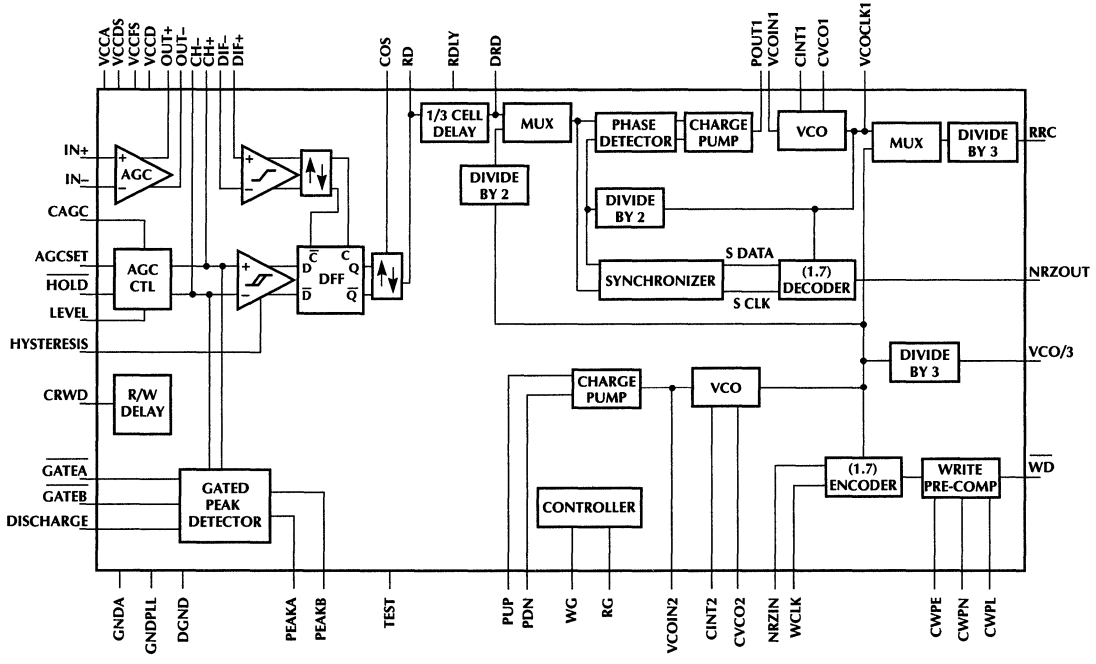
The ML6010 Integrated Disk Read Channel Processor, incorporates a pulse detector, two channel gated servo peak detectors, a data synchronizer, a partial frequency synthesizer, a (1,7) RLL encoder/decoder and write precompensation circuitry onto a single chip, providing a complete read channel solution for hard disk drive subsystems. The chip receives serial NRZ data from the disk controller, encodes the data into (1,7) RLL code with precompensation and writes to the disk. In the read mode it peak detects preamplified read pulses for both data and embedded servo information, resynchronizes the data, and decodes the (1,7) RLL data back to NRZ. The chip operates at data rates up to 36 Mbits/s with three levels of write precompensation, set with an external capacitor and a pulse detector with less than 1ns of pulse pairing. The ML6010 supports constant density recording (CDR) applications with an onboard charge pump and VCO for the frequency synthesizer and requires an external phase detector and M & N dividers to realize a complete frequency synthesizer. It is set to interface directly to ML6005/6 family of BICMOS filter/equalizer chips with programmable cutoff frequency and pulse slimming (equalization) capability.

FEATURES

- NRZ data rates up to 36 Mbits/s
- Single +5 volt power supply +/– 5%
- Operating power dissipation 700mW
- Industry standard pulse detector circuitry with less than 1 ns pulse pairing
- Pattern—insensitive wide bandwidth AGC amplifier
- Two channel gated servo peak detectors for embedded servo recovery
- Industry standard fast acquisition PLL with zero phase start capability
- VCO/Charge pump has greater than 3:1 tuning range
- On-board frequency synthesizer charge pump and VCO for addressing ZBR applications
- Interface to industry standard channel filtering/ equalizer chips like ML6005/6
- Three level Write Data Precompensation support
- (1,7) RLL encoding/decoding support
- Available in a 52 pin QFP package

5

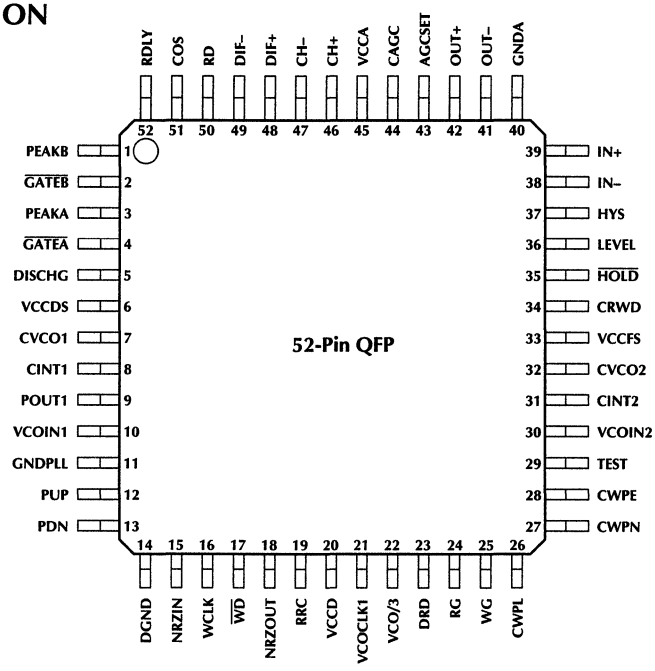
BLOCK DIAGRAM



GENERAL DESCRIPTION (Continued)

The ML6010 is fabricated in a BiCMOS process (4GHz npn f_t; 1.5µ CMOS) and operates off of a single 5 volt supply. The ML6010 is based on a semi-standard tile array (FC3560) with built in uncommitted gain stages for the flexibility of user defined channel pulse detector and/or passive differentiator or matched delay applications and a digital gate array for adding user specific functions, thus allowing for customizable options of this feature set, based on the user requirements. Some examples are the optional servo demod outputs—unbuffered A,B,C,D, or buffered A, B and A-B outputs; a 2,7 RLL Endec instead of the 1,7 RLL Endec or maybe implement the M & N dividers instead of the Endec, digital glue, etc.

PIN CONNECTION



PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	PEAKB	A capacitor or a capacitor in series with a resistor, connected between this pin and GNDA functions as a servo sample and hold for channel B.
2	$\overline{\text{GATEB}}$	TTL input (active low). When this pin is forced TTL low, servo peak detector B is enabled.
3	PEAKA	A capacitor or a capacitor in series with a resistor, connected between this pin and GNDA functions as a servo sample and hold for channel A.
4	$\overline{\text{GATEA}}$	TTL input (active low). When this pin is forced TTL low, servo peak detector A is enabled.
5	DISCHG	TTL input (active high). When this pin is forced to a TTL high, both the servo peak detectors are discharged.
6	VCCDS	Analog + 5 volt supply for data synchronizer related blocks.
7	CVCO1	Capacitor between this pin and VCCDS sets up the VCO center frequency for the data synchronizer.
8	CINT1	Coarse input for data synchronizer loop filter time constant setting.
9	POUT1	Data synchronizer's charge pump output, drives the loop filter input.
10	VCOIN1	Data synchronizer's VCO control input, driven by the loop filter output.

PIN DESCRIPTION (Continued)

PIN#	NAME	FUNCTION
11	GNDPLL	Analog ground for data synchronizer and frequency synthesizer.
12	PUP	Charge pump input for the frequency synthesizer (pump up).
13	PDN	Charge pump input for the frequency synthesizer (pump down).
14	DGND	Digital ground.
15	NRZIN	NRZ write data input from disk controller. This pin can be connected to the NRZOUT pin to form a single bi-directional NRZ port if desired.
16	WCLK	Write clock input synchronous with the NRZ Write data input.
17	$\overline{WD}$	Write precompensated, active low (1,7) RLL encoded write data output to the read/write amplifier.
18	NRZOUT	NRZ read data output to the disk controller. This pin can be connected to the NRZIN pin to form a single bi-directional NRZ port if desired.
19	RRC	Read/Reference clock : a multiplexed clock source used by the disk controller. During mode change there will be no glitches on this line and no more than two lost clock pulses will occur. When Read Gate goes high, RRC synchronized to the NRZ read data will be available after 19 read data pulses.
20	VCCD	Digital VCC +5 volts.
21	VCOCLK1	An open emitter ECL output for testing purposes.
22	VCO/3	Divide by three output of the frequency synthesizer VCO clock output.
23	DRD	1/3 cell delayed read data for testing purposes.
24	RG	Active high read gate input from the disk controller. This signal is used to select the PLL reference input.
25	WG	Active high write gate input from the disk controller. This signal is used to enable the write mode.
26	CWPL	RC network to setup the late delay time constant for write precompensation.
27	CWPN	RC network to setup the normal delay time constant for write precompensation.
28	CWPE	RC network to setup the early delay time constant for write precompensation.
29	TEST	Reserved for test purposes. Must be tied to DGND for normal operation.
30	VCOIN2	Fine input for the frequency synthesizer loop filter time constant setting.
31	CINT2	Coarse input for frequency synthesizer loop filter time constant setting.
32	CVCO2	Capacitor between this pin and VCCA sets up the VCO center frequency for the frequency synthesizer PLL.
33	VCCFS	Analog +5 volt supply for frequency synthesizer.
34	CRWD	Capacitor between this pin and GNDA determines the write to read (input clamp) delay time, e.g. a 1800 pF capacitor gives a delay time of 3 us typ.
35	$\overline{HOLD}$	TTL input pin (active low). When this pin is forced low, all the charging and discharging pathes on the CAGC pin are disabled. The AGC amplifier now acts as a fixed gain amp. with the gain determined by the voltage on the CAGC pin.
36	LEVEL	Emitter follower output, provides rectified signal level, which can be used through a resistor divider network as a dynamic hysteresis control signal to the hysteresis pin.
37	HYS	The voltage applied to this pin determines the threshold level of the qualification channel. In a typical application, the signal on this pin is derived from the LEVEL pin.
38 39	IN- IN+	AGC amplifier differential input, AC coupled from the R/W amplifier. Signal range recommended 15 mV to 150 mVp-p differential.
40	GNDA	Analog ground.

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PIN DESCRIPTION (Continued)

PIN#	NAME	FUNCTION
41 42	OUT- OUT+	AGC amplifier differential outputs, AC coupled to ML6005/ML6006 filter chip. These pins have a current sink capability of 2 mA typical.
43	AGCSET	Voltage on this pin sets up the peak to peak differential voltage at the CH+/CH- pins when the AGC amplifiers are settled. Vp-p diff @CH+/CH- = 4 * (VAGCSET - VCCA/2)
44	CAGC	AGC loop capacitor to GNDA. Lead-Lag network may be used for different loop filter characteristics, if needed.
45	VCCA	Analog +5 volt supply for pulse detector and servo peak detector.
46 47	CH+ CH-	Gating channel differential inputs to hysteresis comparator, AGC fullwave rectifier and two-channel servo peak detector. These are AC coupled from the lowpass output of the ML6005/ML6006 filter/ equalizer chip. Peak to Peak differential signal at these pins are determined by the DC voltage applied to the AGCSET pin.
48 49	DIF+ DIF-	Time Channel zero crossing comparator differential inputs. These are AC coupled from the differentiated (bandpass) outputs of the ML600X filter/equalizer chip.
50	RD	Pulse detector raw read data output. This signal internally goes to the 1/3 cell delay block enroute to the data synchronizer. This is an ECL output.
51	COS	The capacitor between this pin and the VCCA sets up the raw read data pulse width from the pulse detector section to the data synchronizer.
52	RDLY	Resistor between this pin and VCCDS sets the charging current in 1/3 cell delay based on data rate range.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (VCCD) ..... -0.3 to +7 V
TTL Output Voltage (Vout) ..... 5.5 V
TTL Input Voltage (Vin) ..... 5.5 V
Differential Input Voltage (Vdif) ..... 3.0 or -3.0 V
Analog Inputs ..... -0.3 to VCCA + 0.3 V
Storage Temperature (Tstg) ..... -65 to +150 °C
Maximum Junction Temperature ($T_j$max) ..... 125°C

OPERATING CONDITIONS

DC Supply Voltage (VCCD) ..... 5 +/– 5% VDC
DC Supply Voltage (VCCA) ..... 5 +/– 5% VDC
Operating Temperature Range ..... 0 to 70°C

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
AGC Amplifier and I/P Z-Clamp					
AGC 3dB bandwidth (Note 1)	VCAGC = 2V, VIN(Diff) = 15 mVp-p		60		MHz
Maximum AGC gain	VCAGC = 2V, VIN(Diff) = 15 mVp-p	100	150		V/V
Minimum AGC gain	VCAGC = 3.5V, VIN(Diff) = 150 mVp-p		5	10	V/V
AGC Control Range			27		dB
AGC Control Sensitivity			37		dB/V
Input Signal Range (Differential)		15		150	mV
Output Signal Swing (Differential)	VCAGC = 2.0V, VIN(Diff) = +/- 100 mVp-p		1.5	2.5	Vp-p

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
AGC Amplifier and I/P Z-Clamp (continued)					
Input Voltage Noise (Note 1)	VIN = 0 V		20		nV/√Hz
Differential Input Resistance	Read Mode Vin+ = 2.575V Vin- = 2.425	4.5	6.0	7.5	kohm
Differential Input Resistance	Write Mode Vin+ = 2.575V Vin- = 2.425	200	300	400	ohm
Common Mode Rejection Ratio (Note 1)	Vin+ = Vin- = 100 mV VCAGC = 2V		45		dB
AGC offset (I/P referred)	VIN+ = VIN- = VCCA/2 VCAGC = 2 V	-4		4	mV
Power supply Rejection Ratio	VCCA = 5V + 100 mVp-p VCAGC = 2V,		45		dB
AGC output common mode bias	VCCA = 5V, Vin+ = Vin-		2.7	3.0	V
AGC capacitor bias current	VCAGC = 3.5 V		1	20	µA
AGC input offset voltage	VCAGC=2 V, Vin+ = Vin-			400	mV
AGC output sink current	VCCA = 5V	1	2	3	mA
AGC output resistance	Measured on OUT+/OUT-		40		ohms
CAGC voltage range		2.2		3.4	V
Clamp Off time delay (Note 1)	Crwd=1800 pF, VCAGC=2.0V, Vin (diff)=5 mV	2	2.5	3.0	µs
Clamp Propagation Delay R≥W (Note 1)	Crwd=1800 pF, VCAGC=2.0V, Vin (diff)=5 mV		15	100	ns
AGCVOS vs Gain	VCAGC=VCC/2 to VCC/2 + 0.25V	-400		400	mV
AGC Rectifier and Comparator					
Input signal range (Note 1)				2.0	Vp-p
Input Bias voltage		40	50	60	%VCCA
Input resistance (differential)		3.75	5	6.25	Kohms
CAGC Output voltage	@CAGC, Vin > VAGCSET RCAGC = 100K VAGCSET = VCCA/2 + 100mV		VCCA- .8		V
CAGC charge resistance	Vin > VAGCSET VAGCSET = VCCA/2 + 100mV		300		ohms
CAGC clamped voltage (CAGCLMPV)	Vin < VAGCSET VAGCSET = VCCA/2 + 100mV		2.2		V
AGCSET bias current	VAGCSET = 2.5 V		1.5	10	µA
CAGC Decay current	Read , VCAGC=VCCA		4.7		µA
CAGC leak current	Hold Mode VCAGC=CAGCLMPV + 0.4V		0.03	0.5	µA
Hold On & Hold Off time				1	µs

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Zero Crossing Comparator					
Differential input signal range (Note 1)				1.5	Vp-p
Differential input bias current	@ VCCA/2			20	µA
Diff comparator offset voltage	HYS = 0V	-3.0		+ 3.0	mV
Differentail input resistance		4.5	6.0	7.5	kohms
Differential bias voltage		40	50	60	%VCCA
Zero crossing comparator gain (Note 1)			65		dB
Hysteresis Comparator					
HYS input signal range (Note 1)				1.5	Vp-p
Peak Hysterisis vs HYS voltage		0.44	0.5	0.56	V
HYS bias current				20	µA
LEVEL pin max output current		2			mA
LEVEL pin output resistance			130		ohms
Internal and Pulse Qualification One-shot					
Internal one-shot (tpw) (Note 1)			15		ns
Pulse Qualification one-shot (tpw)	Cos = 47 pF		35		ns
Pulse Detector raw data VOH			VCCA-2Vbe		V
Pulse Detector raw data VOL			VOH - 0.73		V
Pulse Pairing Vdiff=1Vp-p diff @ 5 MHz			0.5	1.0	ns
Data Seperator PLL					
Phase Detector range			+/- pi		radians
Charge pump gain	V/I - VCOIN1 @DSVCC/2		125		µA
Data Synch fVCO max	CVCO1 = 10pF ≥ VCCDS RG = 1, WG = 0, VCINT1 = VCCDS - 1 VVCOIN1 = VCCDS/2	108			MHz
Data Synch VCO range	CVCO1 = 10pF ≥ VCCDS RG = 1, WG = 0, VCINT1 = 1V to 4.2V	3:1	4:1		
Data Synch VCO Course Gain	CVCO1 = 10pF ≥ VCCDS RG = 1, WG = 0, VCINT1 = 2V to 2.5V VVCOIN1 = VCCDS/2		300		Mrad/s /V
Data Sync VCO fine Gain	CVCO1 = 10pF ≥ VCCDS RG = 1, WG = 0, VCINT1 = VCCDS/2 VVCOIN1 = 2V to 3V		TBD		Mrad/s /V
PLL jitter specifications			0.7		ns

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Data Seperator PLL (continued)					
Data sync window center offset			1%Tw +/-2		ns
Maximum data rate (1,7 RLL)	CVCO1 = 10pF ≥ VCCDS RG = 1, WG = 0,		28	36	Mbits/s
Frequency Synthesizer PLL					
Charge pump gain	V/I - VCOIN2 @VCCFS/2		125		µA
Freq Synthesizer fVCO max	CVCO2 = 10pF ≥ VCCFS RG = 0, WG = 1, VCINT2 = VCCFS -1 VVCOIN2 = VCCFS/2	108			MHz
Freq Synthesizer VCO range	CVCO2 = 10pF ≥ VCCFS VCINT2 = 1V to 4.2V	3:1	4:1		
Freq Synthesizer fine VCO gain	CVCO2 = 10pF ≥ VCCFS VVCOIN2 = 2V to 3V		TBD		Mrad/s /V
Freq Synthesizer coarse VCO gain	CVCO2 = 10pF ≥ VCCFS VCINT2 = 2V to 2.5V VVCOIN2 = VCCFS/2		300		Mrad/s /V
Servo Peak Detector					
Input signal range (differential) (Note 1)				1.5	Vp-p
Servo demod voltage gain			2		V/V
Offset mismatch between two chnls	Vin = 1.5 Vp-p differential	-20		+20	mV
Output leakage current (ch disabled)	GATE A/B =1, DISCHG=0			10	µA
Servo demod discharge current	R = 750 ohms		650		µA
Miscellaneous					
Operating power dissipation			750	1000	mW
Write Precompensation time	Cwpn=20pF, Cwpl=39pF fWCLK = 36 MHz		2		ns
Write Precompensation time	Cwpn=100pF, Cwpl=200pF fWCLK = 7.2 MHz		20		ns
TTL compatible inputs and outputs					
Input low voltage (VIL)		-0.3		0.8	V
Input high voltage (VIH)		2.0		VCC + 0.3	V
Input low current (IIL)	VIL = 0.4V			0.4	mA
Input high current (IIH)	VIH = 2.7V			100	µA
Output low voltage (VOL)	IOL = 1 mA			0.4	V
Output high voltage (VOH)	IOH = -400 µA	2.4			V

Note 1: These parameters are guaranteed by design. They are not 100% tested and are not in outgoing quality level calculation.

FUNCTIONAL DESCRIPTION

The ML6010 provides the integration of most of the functions associated with the implementation of disk read channel design up to 36 Mbits/s data rates. It incorporates a pulse detector, two gated servo peak detectors, a data seperator with fast acquisition capability, the charge pump and VCO functions for implementing a frequency synthesizer, write precompensation circuitry and a (1,7) RLL Endec. It is targeted at one/two platter 3 1/2" and high capacity 2 1/2" drives, where performance and capacity requirement take priority to power requirements, although the overall power requirements are much lower than earlier discrete block implementations.

The **Pulse Detector** section includes a wide bandwidth differential amplifier with automatic gain control, a precision full wave rectifier, time channel and gate channel. User programmable equalization or pulse slimming, and CDR band selection is supported through an external filter chip (ML6006). The Pulse detector will support pulse pairing specifications less than +/– 1ns.

Two Gated Servo Peak Detectors are incorporated for recovery of embedded servo information. Optionally it can provide buffered (A,B and a position error signal—PES) low impedance outputs which represent the peak detected level of each servo burst. These voltages are suitable for digitizing by an A/D converter and processed by the controlling processor, for head positioning.

The **Data Synchronizer** incorporates a fast acquisition phase lock loop with zero phase start capability and a 3:1 tuning range. Precise decode window control is achievable using external components and the 1/3 cell delay automatically tunes to the synthesized frequency depending on the zone. The settling time is typically less than 2 µs which is well within the requirements, e.g. for 36 Mbps data rate with 8 bytes of 3T preamble, and 1,7RLL code the minimum settling time required equals :

$$1/36 * 2 * 8 * 8 = 3.55\ \mu s$$

The partial **Frequency Synthesizer** generates all necessary clocks for data encoding and synchronizer reference. The synthesizer requires external logic for the input divider (N) and feedback divider (M) programming and also uses an external loop filter, giving the user full control over the PLL's dynamics.

The **Endec** employs the 2/3 (1,7) RLL code type and supports a hard sectored drive implementation. After the index/sector pulse has been detected, an internal counter counts negative transitions of the incoming read data looking for three consecutive "3T" pattern. Once detected the VCO lock process is established. The **Write Precompensation** circuitry, provides control of the normal, early and late settings.

The ML6010 is fabricated in a BiCMOS process (4GHz npn f_t; 1.5µ CMOS) and operates off of a single 5 volt supply and is based on the **FC3560 semi-standard array**. The tile array allows a number of configurable features to realize a ML6010 like read channel combo chip, with customized features and pinout. For more information on the configurable options contact the factory.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6010CG	0°C to +70°C	52-Pin QFP (G52)

3.5" R/W MOD Read Channel Front-end Processor

GENERAL DESCRIPTION

The ML6012 is a BiCMOS Read channel front-end processor IC which is one-half of the read channel chip-set from Micro Linear, intended for 3.5" Magneto-Optical disk drive (MOD) applications. It works in conjunction with the ML6013 MOD read channel back-end processor to form a complete solution to support the ISO standards for the 128M and the 230M rewritable magneto-optical disk drive. The coupling capacitors between AGC/Filter/Pulse detector are implemented on chip and the programmability of various options is achieved with on-board DACs, thus reducing the external component count significantly.

The major functional blocks in this chip are :

- Analog Mux for RO and MO selection
- VGA (variable gain amplifier)
- AGC control loop
- Sector mark detector
- Programmable VGA for sector mark detection
- 6th order Filter/equalizer with 2nd differentiator for sector mark detection
- Two corner frequency registers for changing between sector mark and data
- DC restore and Data detector
- Dropout detector (Retriggerable one-shot)
- Bandgap reference
- Timing and control logic
- 3-Wire Serial Port Interface

The ML6012 will have a typical power dissipation of 300mW in normal operating mode and less than 1mW in the sleep mode.

FEATURES

- Supports ISO Standards for 128M and 230M R/W Magneto-Optical drive (MOD)
- Operating supply range 4.5V to 5.5V
- Typical power dissipation is 300mW
- Sleep mode power dissipation less than 1mW
- Operates up to 24Mb/s NRZ data rate and supports (2, 7) RLL with a 48MHz code rate
- On-chip mux for RO & MO channel selection
- Wide bandwidth VGA amplifier
- Independent programmable level qualification for sector mark detection
- Independent programmable level qualification for Data detection
- On-chip DC restore circuit bandwidth tracks the filter bandwidth for reliable data detection and AGC operation.
- Programmable AGC attack and decay current
- 6 pole, 2 zero equiripple filter with less than 40dB harmonic distortion
- Programmable filter cutoff frequency with separate registers for MO and RO inputs
  MO — Data mode (DSLIM = 0);
  f_C = 4 to 14MHz in 32 steps
  RO — Sector mark mode (DSLIM = 1)
  f_C = 2 to 6.84MHz in 16 steps

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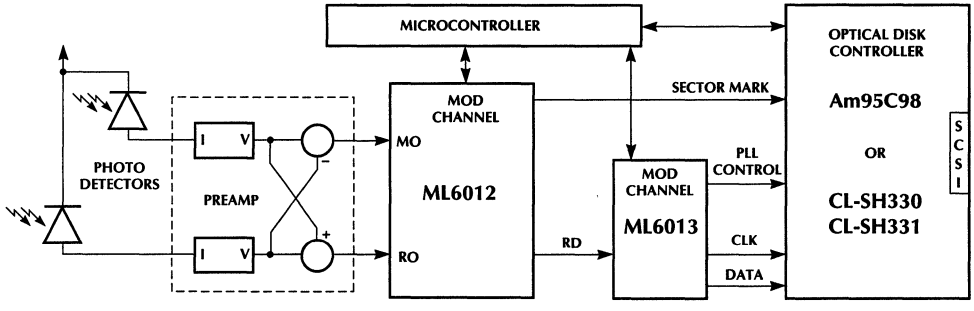
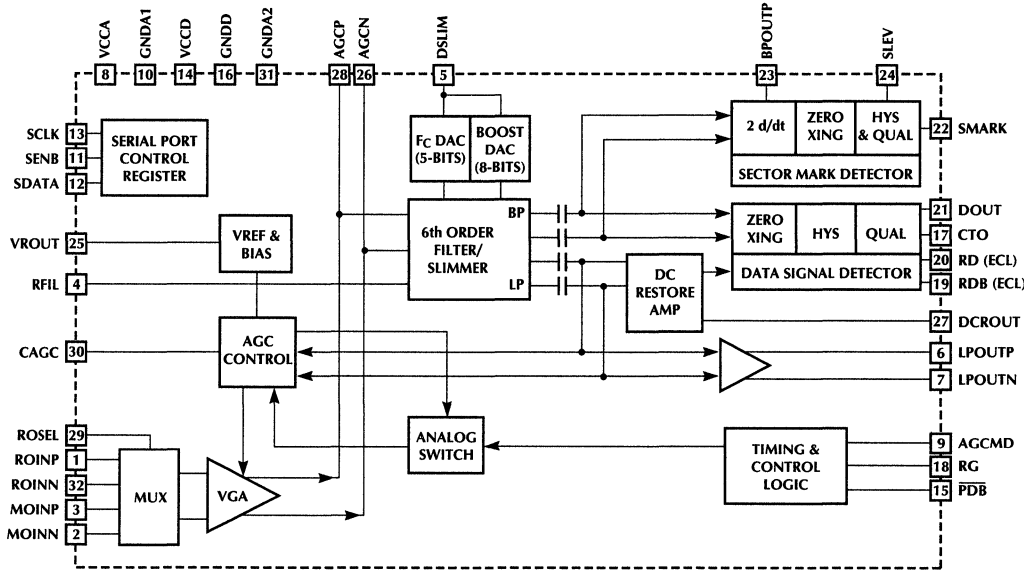
SYSTEM BLOCK DIAGRAM



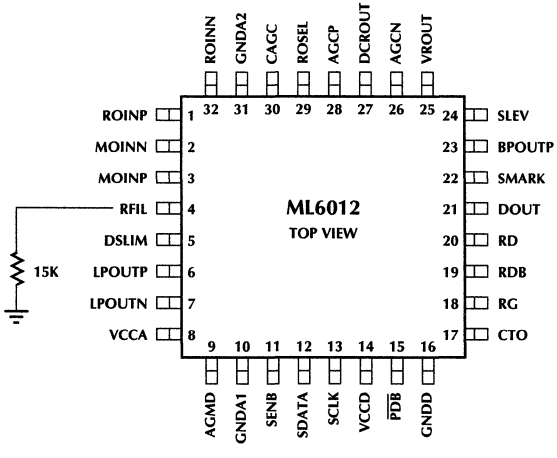
FEATURES (continued)

- Programmable asymmetric equalization with 8-bits (256 combinations of phase/frequency) and 0 to 11dB boost capability at f_C
- High speed (20MHz clock) three wire serial port interface with double buffered data
- External components minimized
- 32-pin TQFP low profile package

BLOCK DIAGRAM



PIN CONNECTION WITH TYPICAL COMPONENT VALUES



PIN DESCRIPTION

PIN	NAME	FUNCTION
1 32	ROINP ROINN	RO channel differential signal inputs. Signal dynamic range: 25mV to 500mV$_{P-P}$ differential. These two pins are internally biased at approximately VCCA – 2.8V. A positive level on ROINP corresponds to the "MARK." A positive peak on ROINP pin corresponds to "1."
3 2	MOINP MOINN	MO channel differential signal inputs. Signal dynamic range: 25mV to 500mV$_{P-P}$ differential. These two pins are internally biased at approximately VCCA – 2.8V. A positive level on MOINP corresponds to the "MARK." A positive level on MOINP pin corresponds to "1."
29	ROSEL	RO channel and MO channel selection control input, CMOS compatible. When this pin goes low, the MO channel is selected as an input to the IC. When this pin goes high, the RO channel is selected.
28 26	AGCP AGCN	Differential VGA amplifier outputs (open emitter). Used as a test point for evaluation purposes. Leave these two pins open to reduce the power dissipation caused by the external bias resistors, or current sources. The output common-mode voltage is set at approximately VCCA – 2.7V. For better noise rejection, the signal should be observed differentially. If the signal is observed single ended, it should be referred to VCCA. 1KΩ resistors to ground may be used to bias these outputs.
4	RFIL	A 15KΩ resistor between this pin and GNDA will set up the cut-off frequency (f_C) of the filter. This resistor may be increased up to 50% to decrease the filter cut-off frequency (f_C).
5	DSLIM	Slimming disable function control pin (CMOS compatible, active high). When this pin is forced to logic high, the equalizer/slimmer function is disabled, the SMARK output is enabled, and the f_C of the filter can be programmed between 2 and 6.8MHz by the content of Register #3. When this pin is forced to logic low, the equalizer function is enabled, and can be programmed with Register #1 and Register #2, the SMARK output is disabled and held to logic low, and the f_C of the filter can be programmed between 4 and 14MHz, by the content of Register #0. It is required to set this pin to logic low during power up and while programing the control registers in order to reset the SMARK output.
6 7	LPOUTP LPOUTN	Differential LPF outputs from the filter (open emitter). Used as a test point for evaluation purposes. Leave these two pins open to reduce the power dissipation caused by the external bias resistors, or current sources. The output common-mode voltage is set at approximately 1.5 volts above ground. For better noise rejection, the signal should be observed differentially. Single ended, it should be referred to GNDA. 750Ω resistors to ground may be used to bias these outputs.
23	BPOUTP	1st differentiator output from the filter (open emitter). Used as a test point for evaluation purposes. Leave this pin open to reduce the power dissipation caused by external bias resistor, or current source. The output DC voltage is set at approx. (VCCA – 3V). For better noise rejection the signal should be observed with respect to VCCA. A 750Ω resistor may be used to bias this output.
27	DCROUT	Buffered DC restore output (open emitter). Used as a test point for evaluation purposes. Leave this pin open to reduce the extra power dissipation caused by the external bias resistor, or current source. The output voltage is set at approx. VCCA – 1.85V. For better noise rejection, the signal should be observed with respect to VCCA. A 1 or 2KΩ resistor to ground may be used to bias the output buffer.
30	CAGC	A capacitor between this pin and GNDA sets the AGC loop time constant. A lead-lag RC network may be used if necessary. For data rates from 12-24Mbps, a 1000pF is recommended. For data rates lower than 12Mbps, the capacitor value should be increased.

PIN DESCRIPTION (Continued)

PIN	NAME	FUNCTION
24	SLEV	A DC voltage applied to this pin sets the qualification level for the qualification comparator in the sector mark detector block. This pin can be tied to VROUT.
17	CTO	A capacitor between this pin and GNDA will set the time out period for the dropout detection circuit. (Recommended values are: 355pF for 3600RPM 230MB, 265pF for 4800RPM 230MB, and 250pF for 5100RPM 230MB drives) The typical time is computed from t = 0.105 x R_{INT} x CTO. R_{INT} is 20K (±25%).
21	DOUT	Dropout detection circuit output (CMOS compatible). This pin goes high when no pulses are detected for a preset time interval (determined by CTO). This pin normally ties to the COAST pin in the ML6013 chip.
20 19	RD RDB	Encoded read data output (ECL outputs). The ML6013 back-end processor recovers the clock by using this data stream and the Data synchronizer Phase Locked Loop (PLL) before sending it to the 1/2 (2, 7) RLL ENDEC for decoding. (Rising edge of RD represents the flux changes on the MO drive). If the ML6013 is not connected, 3.2KΩ resistors to ground are needed to increase the bias current of these outputs. These outputs are reset and not active when RG is low. (Reset mode)
22	SMARK	Sector mark detector output (CMOS compatible). This pin goes high when a qualified "mark" is detected.
25	VROUT	Buffered Bandgap reference output (2.5V typical). The voltage for the SLEV pin can be derived from this reference.

PIN	NAME	FUNCTION
15	PDB	Power down enable (CMOS compatible input, active low). This pin is set low to power down the chip. This pin is internally OR'd with bit 4 of control register #5.
18	RG	Read gate (CMOS compatible input, active high) from controller. This pin combines with the AGCMD pin in the "timing and control logic" section, to generate the different AGC modes of operation. When RG:0; the chip enters reset mode (RD:Low, RDB:High) (VGA mode) and CAGC discharges to $0.56V_{CC}$.
9	AGCMD	AGC mode control input (CMOS compatible, active high). This pin is usually tied to the PLLGS pin in the ML6013. When AGCMD:Low and RG:High the AGC is on; when AGCMD:High and RG:High; the AGC is in HOLD mode.
13	SCLK	This is a CMOS input which clocks the Control Register (falling edge triggered). Internally this pin is gated with the SENB signal.
12	SDATA	Control Register Data, CMOS input, clocked by SCLK.
11	SENB	Active low CMOS input — Control Register enable. A logic low input on this pin allows the SCLK input to clock the SDATA into the control register and the rising edge latches the control register contents internally (double buffered).
8	VCCA	VCC for analog sections
14	VCCD	VCC for digital sections
10	GNDA1	Analog ground
31	GNDA2	Analog ground
16	GNDD	Digital ground

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

DC Supply Voltage (VCCA & VCCD) ..... –0.3 to +7V
Analog & Digital Inputs/Outputs ..... –0.3 to VCCA + 0.3V
Input Current per Pin ..... –25 to +25mA
Storage Temperature ..... –65 to +150°C
Maximum Junction Temperature ..... 125°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage Range ..... 4.5V to 5.5V
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VCCA = VCCD = 4.5 to 5.5 volts and T_A = 0 to 70°C (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Dissipation					
VCCA/VCCD		4.5	5.0	5.5	V
IVCCA	Output unloaded		60	75	mA
IVCCD	Output unloaded		3.0	3.5	mA
Sleep Mode Supply Current	VCCA + VCCD			100	µA
Digital I/O Specifications (Inputs are CMOS compatible while outputs are TTL compatible)					
High level input voltage		VCCD – 0.5		VCCD	V
Low level input voltage				0.5	V
High level input current	V_{IH} = VCCD – 0.1V			10	µA
Low level input current	V_{IL} = 0.1V			10	µA
High level output voltage	I_{OH} = 400µA	VCCD – 0.2			V
Low level output voltage	I_{OL} = 2mA			0.4	V
Analog Mux for RO and MO Channel Selection					
Differential input swing	RO and MO signals	25		500	mV_{P-P}
Differential input resistance		3.75	5.0	6.25	KΩ
Input bias voltage			VCCA – 2.8		V
RO/MO select switching				50	ns
Variable Gain Amplifier (VGA)					
Maximum gain (A Vmax)	AGC mode	1.8	2	2.2	V/V
Minimum gain (A Vmin)	AGC mode		0.04	0.1	V/V
Maximum gain (A Vmax)	Fixed gain mode	5.0	5.6		V/V
Minimum gain (A Vmin)	Fixed gain mode		0.05	0.2	V/V
3dB bandwidth	AGC mode	50	60		MHz
Gain control range	AGC mode	25			dB
AGC control sensitivity			40		dB/V
LP_{OUT} diff output swing	Closed loop @ LPF output (ASL0:0 ASL1:1)	384	480	576	mV_{P-P}
Total harmonic distortion	25mV to 500mV_{P-P}			2	%
Equivalent input noise	Fixed gain mode, minimum gain AGC mode, minimum gain		90 30		$nV\sqrt{Hz}$ $nV\sqrt{Hz}$
CMRR	V_{IN} = 300mV_{P-P} diff @ 5.8MHz, input shorted together		40		dB

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ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Variable Gain Amplifier (VGA) (Continued)					
PSRR	V_{IN} = 300mV_{P-P} diff @ 1MHz, input shorted together		40		dB
AC coupling network	Cutoff frequency		8	12	KHz
DC Restore Section					
Maximum bandwidth	DCR bits 2-0 = 100		620		KHz
Minimum bandwidth	DCR bits 2-0 = 100		177		KHz
Maximum shift	DCR bits 2-0 = 111		1.6		
Minimum shift	DCR bits 2-0 = 000		0.2		
AGC Control Section (AGC Mode)					
CAGC clamp voltage (L)		0.52	0.65	0.78	V
CAGC clamp voltage (H)		2.2	2.8	3.4	V
Min CAGC normal attack current	bits ATK1, ATK0 = 00	230	300	390	µA
Max CAGC normal attack current	bits ATK1, ATK0 = 11	925	1200	1560	µA
Min CAGC normal decay current	bits DKY1, DKY0 = 00	23	30	39	µA
Max CAGC normal decay current	bits DKY1, DKY0 = 11	92	120	156	µA
CAGC leak current	RG = 1, AGCMD = 1 (Hold mode)			50	nA
Sector Mark Detection Section					
SLEV DC voltage range	(V to I converter)		2.5		V
RMS jitter ±1 sigma Note 2	f_{IN} = 4.0MHz, f_C = 5.5MHz DSLIM pin = 1			5	ns
Qualification level comparator range	$V_{DAC} = V_{MAX} \times k/16$ (k = 0-15)			±15 x $V_{MAX}/16$	V
Qualification level comparator step	$V_{MAX} = V_{SLEV}/80$		$V_{MAX}/16$		V
Data Detection Section					
Zero crossing comparator resolution			0.5		mV
RMS jitter ±1 sigma Note 2	f_{IN} = 16MHz, f_C = 11.1MHz full slimming, ASL = 1, 0			365	ps
Qualification level comparator range	V_{DAC} = 750mV/16 x K; K = 0 to 15 (4-bit DAC)	0		703.13	mV
Qualification level comparator step			46.875		mV
Dropout one-shot time	CTO = 355pF, t = 0.105 x R_{INT} x CTO	520	745.5	970	ns
Read pulse one-shot		15	25	40	ns
RD/RDB high (V_{OH})	Diff psuedo ECL output		3.4		V
RD/RDB low (V_{OL})	Diff Psuedo ECL output		3.0		V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Lowpass Filter, First and Second Differentiator					
Data mode cutoff frequency	DSLIM = low, f_C(MHz) = 4 + (10 x n/31) where n = 0, 1, 2, . . . 31	4		14	MHz
Sector mark cutoff frequency	DSLIM = high, f_C(MHz) = 2 + (5 x n/31) where n = 0, 2, 4, . . . 30	2		6.84	MHz
Cutoff frequency accuracy		–10		+10	%
Slimming level accuracy	Symmetric equalization	–1		+1	dB
Differential group delay	4MHz ≤ f_C ≤ 14MHz			±5	%
Second differentiator center frequency (f_O) to main filter cutoff frequency (f_C) ratio	Ratio of (f_O/f_C)		1		
Bandgap Reference					
Reference voltage out	VR_{OUT}	2.375	2.5	2.625	V
Driving capability		2			mA
Serial Microprocessor Interface					
Serial clock (SCLK) frequency		10		20,000	KHz
SCLK duty cycle		40		60	%
SCLK pulse width	t_{PW}	20			ns
SCLK to SDATA hold time	t_{HSD}	10			ns
SDATA to SCLK setup time	t_{SSD}	10			ns
SENB to SCLK setup time	t_{SSEN}	10			ns
SCLK to SENB hold time	t_{SSEN}			10	ns
SENB high time		50			ns

Note 1: Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.
Note 2: The ±1 sigma RMS jitter is one standard deviation of the distribution of the edge transistor time. The peak-to-peak is twice the value shown.

TIMING DIAGRAMS

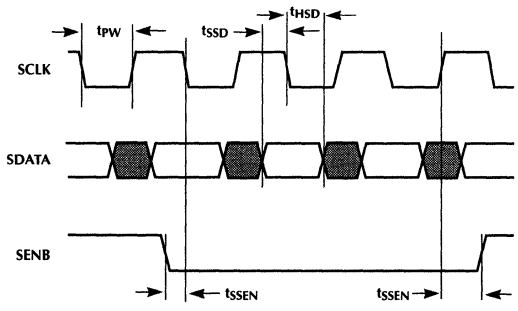


Figure 1. Serial Port Timing Diagram

FUNCTIONAL DESCRIPTION

INTRODUCTION

The ML6012 is a BiCMOS Read channel front-end processor IC which is one half of the read channel chip set from Micro Linear, intended for 3.5" Magneto-Optical disk drive (MOD) applications. It is optimized to handle the front-end channel functions and works in conjunction with the ML6013 MOD read channel back-end processor to form a complete solution to support the ISO standards for the 128M and the 230M rewritable magneto-optical disk drive. The coupling capacitors between AGC/Filter/ Pulse detector are implemented on-chip and the programmability of various options is achieved with on board DACs, thus reducing the external component count significantly.

The pulse detector consists of the AGC amplifier with a full AGC loop, which works in conjunction with the programmable filter/equalizer circuitry. The AGC loop has three operation modes as tabulated below;

MODE CONTROL

RG	AGCMD	MODE
0	X	RESET mode (VGA mode)
1	0	AGC mode (AGC on)
1	1	HOLD mode (CAGC held)

Two different pulse detection schemes are employed to optimize the sector mark signal during RESET mode, and the data detector signal during the AGC and the HOLD modes independently. The entire pulse detector signal path is fully differential to minimize noise pick up from the power supply and external components, thereby increasing the signal-to-noise ratio. Also a design scheme is adopted to guarantee that any baseline noise superimposed on the signal be rejected, thereby preventing false triggering the internal flip-flop that may otherwise occur in the pulse detector.

The ML6012 is designed to offer lower power dissipation, higher level of integration and high level of programmability to minimize the number of external components, thus resulting in an optimized MOD read channel front-end. It outputs ECL a read data signal which is level compatible with the input to the companion chip ML6013, used for data separation and clock synchronization. Please refer to the block diagram of the ML6013 for the details.

SECTOR MARK DETECTOR

Sector mark detector uses the 1st and 2nd differentiated outputs from the filter/equalizer. The 1st differentiated signal is differentially compared in the qualification comparator with the qualification level programmable through control register #4. This ensures that only a data pulse of sufficient amplitude will be qualified as a correct signal and multiplied with the 2nd differentiated signal to generate the clock to the flip-flop and output the sector mark signal.

Control register #3 can be used to program the cutoff frequency of the filter from 2MHz to 6.84MHz to optimize the dynamic range of the sector mark detector channel depending on the input signal amplitude. DSLIM pin can be used to gate the sector mark signal. If DSLIM is set to low, sector mark output is disabled and reset to CMOS logic low. Since the sector mark detector needs to operate only during the RESET mode, it is recommended to set the DSLIM pin to low except during RESET mode to prevent any noise injection due to switching of the CMOS output from the sector mark detector. Also, it is required to set the DSLIM pin to low during power-up to reset the sector mark.

DATA DETECTOR

The inputs to the data detector are the 1st differentiated signal from the filter/equalizer and the DC restored lowpass signal from the AGC control loop. Control register #0 can be used to program the cutoff frequency of the filter from 4MHz to 14MHz to optimize the dynamic range of the data detector channel.

The DC restored signal is first compared differentially in the qualification comparator whose qualification level is programmable using the control register #5. This signal is then multiplied with the output of the zero crossing comparator from the 1st differentiated signal. The multiplier output triggers the oneshot whose ECL output is the encoded read data output from ML6012. This output signal can be directly used as the input to the companion chip ML6013 for data synchronization. This signal is also internally used as an input to the retriggerable oneshot to flag if no pulses are detected for a preset time interval. RG pin can be used to gate the data detector output. If it is set low, the chip is in RESET mode and the data detector output is disabled. (RD:Low, RDB:High)

AGC

The AGC gets its differential input from the RO/MO mux. The input impedance of the mux enters a low impedance state during the intial period of AGC operation in order to avoid transients which may cause erratic AGC operation. The period consists of a 0.4µs fixed blanking portion, during which the CAGC voltage is held constant, and a variable portion that tracks with the inverse of the cutoff frequency of the filter (0.6µs for f_C = 11MHz and 48MHz code rate). From the end of the fixed to the end of the variable portion of this period the super attack and super decay currents are multiplied by a factor of two. The 0.4µs blanking period is necessary to allow the circuit to settle before the CAGC is allowed to change due to the charge pump. The cutoff frequency of the AC coupling network in the mux is set by the external coupling capacitor and the input impedance of the mux. The recommended value of the external capacitor is 8nF. In this case, the cutoff frequency is 12KHz during the RESET mode and approximately 1MHz during the AGC mode. The input signal range is 25mV to 500mV peak-to-peak differential.

The AGC amplifier is a two stage differential amplifier with high bandwidth. The first stage of the amplifier is a variable Gain Amplifier (VGA) whose gain is controlled by the control register #7 during the RESET mode and by the voltage on the CAGC pin during the AGC and the HOLD modes. The output of the AGC amplifier feeds into the filter/equalizer through internal AC coupling network whose time constant is adjusted to get optimal performance in the different modes. In RESET mode, the AC coupling cutoff frequency is set at 12KHz. In AGC mode, the cutoff frequency is set at around 1MHz during the initial 1µs of the AGC to enter the fast mode and at around 120KHz for the rest of the AGC mode.

The lowpass output from the filter/equalizer goes through 12x amplifier and the DC restore circuitry where the DC level is clamped. This signal level is typically 480mV (ASLI = ASL2 = 0) and it is used in the comparator in AGC loop to generate the control voltage on the CAGC pin during AGC mode. The capacitor on the CAGC pin then gets charged or discharged depending on whether the signal is greater than or less than the preset reference voltage. The reference voltage is programmable from 480mV to 840mV in 120mV step through the ASL bits in the control register #6. The charging and discharging current, also referred to as the attack and decay rates, are programmable through the D4 bit in control registers #1-4. Refer to the section Control Register for programming details.

PROGRAMMABLE FILTER/EQUALIZER

The programmable filter/equalizer circuit approximates a sixth-order, 0.05 Equiripple function which achieves a flat group delay up to twice the cutoff frequency ($2f_C$). The filter is implemented by using gm/C integrators, and processes signals in a differential mode for greater noise immunity. Temperature stable cutoff frequencies are obtained. The filter architecture provides for smaller excess phase and power dissipation. It generates both a lowpass and bandpass (differentiated) output. The filter can be operated in two modes controlled by DSLIM pin. If DSLIM is set to high, the filter is operated in the data mode, and the cutoff (corner) frequency of the filter is controlled in the range 4-14MHz range by 5 bits stored in control register #0 (f_Cd4-0) to provide 32 combinations. A low input at the DSLIM pin sets the filter to be operated in the sector mark mode with corner frequency in the range of 2-6.838MHz, which is controlled by 4 bits stored in control register #3 (f_Cs4-1). The corner frequency of the filter is given by the following equations:

$$f_C = 4 + \frac{10}{31} \times (16f_Cd4 + 8f_Cd3 + 4f_Cd2 + 2f_Cd1 + f_Cd0)$$

(data mode)

$$f_C = 2 + \frac{5}{31} \times (16f_Cs4 + 8f_Cs3 + 4f_Cs2 + 2f_Cs1)$$

(sector mark mode)

Two real zeroes of opposite polarity are introduced by two stages inserted between the first/second and the second/third biquads. The zeroes can be adjusted independently so that it is possible to realize asymmetric equalization, if desired. The transfer function of the equalizer and equalization level is given by:

$$Hs = \left(1 - \frac{k_1 s}{\omega_{01}}\right)\left(1 + \frac{k_2 s}{\omega_{02}}\right)$$

Where ω_{01}, and ω_{02} are the corner frequencies of the first and the second biquads. k1 and k2 can be controlled independently by adjusting the bias currents in the slimmers. They are adjusted by changing the slimming control bits in control register #1 (ea3-0) and #2 (eb3-0), and their values are shown below:

$$k_1 = \frac{k_{1MAX}(8ea3 + 4ea2 + 2ea1 + ea0)}{15} = \frac{k_{1MAX}N_1}{15},$$

$$k_2 = \frac{k_{1MAX}(8eb3 + 4eb2 + 2eb1 + eb0)}{15} = \frac{k_{2MAX}N_2}{15}.$$

Then the total slimming level SL(ω) and the group delay G(ω) of the equalizer as a function of frequency are

$$SL(\omega) = 10\log\left[1 + \left(\frac{k_{1MAX}N_1\omega}{15\omega_{01}}\right)^2\right] + 10\log\left[1 + \left(\frac{k_{2MAX}N_2\omega}{15\omega_{02}}\right)^2\right]$$

$$G(\omega) = \frac{k_{1MAX}}{\omega_{01}}\left(\frac{N_1}{1 + \left(\frac{k_1N_1\omega}{\omega_{01}}\right)}\right) - \frac{k_{2MAX}}{\omega_{02}}\left(\frac{N_2}{1 + \left(\frac{k_2N_2\omega}{\omega_{02}}\right)}\right)$$

The maximum slimming level, which is designed to be 11dB at the corner frequency of the filter, is determined by

$$k = k_{1MAX}\frac{\omega_c}{\omega_{01}} = k_{2MAX}\frac{\omega_c}{\omega_{02}}$$

The normalized corner frequencies and the quality factors of the sixth-order equiripple filter are:

$\omega_{01} = 0.981$, $\omega_{02} = 2.074$, $\omega_{03} = 1.47$

$Q_1 = 0.551$, $Q_2 = 1.686$, $Q_3 = 0.893$

k_{1MAX} and k_{2MAX} are designed to be 1.566 and 3.311 to achieve 11dB maximum slimming at the corner frequency of the filter.

The slimming function is disabled in the sector mark mode.

SERIAL MICROPROCESSOR INTERFACE

The serial microprocessor interface consists of a simple three-wire serial port. Data is serially clocked into the ML6012 on the SDATA at the falling edges of the serial shift clock, SCLK, provided the SENB pin is active (low). The data is shifted in blocks of eight bits with MSBit first. The internal registers are organized in blocks of eight bits, with the three most significant bits denoting the address, followed by the five data bits. This addressing scheme allows for a register bank of eight registers. When the chip is physically powered-up, the control registers come up in an undetermined state and hence they need to be initialized to some preset bit configuration so that the behavior of the chip is predictable. The control registers retain their programmed information in any of the power-down modes, until the chip is physically powered-down. When the SENB pin goes inactive (high), the SDATA and SCLK pins are ignored and the previously shifted information is latched on the rising edge of the SENB, into the appropriate register bank based on the address bits. It is recommended that the SCLK input be kept inactive low till such time when it is in use. The SCLK input is capable of handling speeds up to 20MHz.

CONTROL REGISTER DEFINITIONS

The control register bank consists of eight registers with addresses from 0 through 7. On power-up the state of the control register bits is not predictable and hence the desired state needs to be set. It is required that the DSLIM pin be set low during power-up. Outlined below are the detailed bit-by-bit definitions of the control registers.

CONTROL REGISTER #0

Data Filter Cutoff frequency control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	0	0	f_Cd4	f_Cd3	f_Cd2	f_Cd1	f_Cd0

f_Cd4	f_Cd3	f_Cd2	f_Cd1	f_Cd0	f_Cd (MHz)
0	0	0	0	0	4.000
0	0	0	0	1	4.323
0	0	0	1	0	4.645
0	0	0	1	1	4.968
0	0	1	0	0	5.290
0	0	1	0	1	5.613
0	0	1	1	0	5.935
0	0	1	1	1	6.258
0	1	0	0	0	6.581
0	1	0	0	1	6.903
0	1	0	1	0	7.226
0	1	0	1	1	7.548
0	1	1	0	0	7.871
0	1	1	0	1	8.194
0	1	1	1	0	8.516
0	1	1	1	1	8.839
1	0	0	0	0	9.161
1	0	0	0	1	9.484
1	0	0	1	0	9.806
1	0	0	1	1	10.129
1	0	1	0	0	10.452
1	0	1	0	1	10.774
1	0	1	1	0	11.097
1	0	1	1	1	11.419
1	1	0	0	0	11.742
1	1	0	0	1	12.065
1	1	0	1	0	12.387
1	1	0	1	1	12.710
1	1	1	0	0	13.032
1	1	1	0	1	13.355
1	1	1	1	0	13.677
1	1	1	1	1	14.000

Note: DSLIM pin is LOW.

CONTROL REGISTER #1

Asymmetric equalization — Zero A & AGC

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	0	1	atk1	ea3	ea2	ea1	ea0

Note: Refer Asymmetric equalization tables attached.

CONTROL REGISTER #2

Asymmetric equalization — Zero B & AGC

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	1	0	atk0	eb3	eb2	eb1	eb0

		AGC ATTACK CURRENT	
atk1	atk0	NORMAL	SUPER
0	0	300µA	600µA
0	1	600µA	1200µA
1	0	900µA	1800µA
1	1	1200µA	2400µA

CONTROL REGISTER #3

Sector mark Filter Cutoff frequency control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	1	1	dky1	fsm3	fsm2	fsm1	fsm0

fsm3	fsm2	fsm1	fsm0	f_{C}sm (MHz)
0	0	0	0	2.00
0	0	0	1	2.32
0	0	1	0	2.65
0	0	1	1	2.97
0	1	0	0	3.29
0	1	0	1	3.61
0	1	1	0	3.94
0	1	1	1	4.26
1	0	0	0	4.58
1	0	0	1	4.90
1	0	1	0	5.23
1	0	1	1	5.55
1	1	0	0	5.87
1	1	0	1	6.19
1	1	1	0	6.52
1	1	1	1	6.84

Note: DSLIM pin is HIGH.

CONTROL REGISTER #4

AGC & Sector Mark Qualification level control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	0	0	dky0	shy3	shy2	shy1	shy0

		AGC DECAY CURRENT	
dky1	dky0	NORMAL	SUPER
0	0	30µA	60µA
0	1	60µA	120µA
1	0	90µA	180µA
1	1	120µA	240µA

shy3 . . . shy0 — Sector Mark qualification level control. These 4-bits program the sector mark qualification level with a 4-bit DAC whose reference is the voltage at the SLEV pin. DSLIM pin needs to be set low before programming this register in order to avoid false qualification at sector mark detector.

CONTROL REGISTER #5

Data Detector Qualification level control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	0	1	pdwn	dhy3	dhy2	dhy1	dhy0

PDB PIN	PDWN BIT	DESCRIPTION
0	X	Chip powered-down, Pd < 1mW
X	0	Chip powered-down, Pd < 1mW
1	1	Normal operation, Pd < 350mW

dhy3 . . . dhy0 — Data Detection Qualification level control. These 4-bits program the data detector qualification level with a 4-bit DAC.

5

CONTROL REGISTER #6

AGC & DC Restore level control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	1	0	asl1	asl0	dcr2	dcr1	dcr0

asl1, asl0 — AGC set level control bits allow the optimization of the internal dynamic range between 3T and 8T frequency levels, which affects the data detectors performance. The optimum setting depends upon the f_C setting, the slimming level and the input signal resolution (ratio of 3T frequency to 8T frequency). A setting of (00) sets the lowest internal signal amplitude while a setting of (11) sets the largest. For a 20% resolution the (00) setting is recommended with $f_C = 2/3f_{3T}$ and full slimming.

dcr2 . . . dcr1 — DC restore discharge current control to set the bandwidth of the DC restore circuitry. The DC restore discharge current which sets the bandwidth of the DC restore circuit, tracks the filter cutoff frequency set by the f_Cd bits. In addition, the dcr bits provide an extra adjustment around this value, as shown in the table below. The range is from 0.2 to 1.6 times the internally set bandwidth.

dcr2	dcr1	dcr0	dcr BW SHIFT
0	0	0	0.2
0	0	1	0.4
0	1	0	0.6
0	1	1	0.8
1	0	0	1.0
1	0	1	1.2
1	1	0	1.4
1	1	1	1.6

CONTROL REGISTER #7

AGC Fixed Gain Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	1	1	vga4	vga3	vga2	vga1	vga0

Programs the gain of the AGC amplifier in the reset mode (RG = 0)

vga4	vga3	vga2	vga1	vga0	GAIN
0	0	0	0	0	5.86
0	0	0	0	1	5.54
0	0	0	1	0	5.15
0	0	0	1	1	4.78
0	0	1	0	0	4.44
0	0	1	0	1	4.13
0	0	1	1	0	3.85
0	0	1	1	1	3.58
0	1	0	0	0	3.33
0	1	0	0	1	3.10
0	1	0	1	0	2.88
0	1	0	1	1	2.67
0	1	1	0	0	2.48
0	1	1	0	1	2.29
0	1	1	1	0	2.12
0	1	1	1	1	1.95
1	0	0	0	0	1.79
1	0	0	0	1	1.64
1	0	0	1	0	1.50
1	0	0	1	1	1.36
1	0	1	0	0	1.23
1	0	1	0	1	1.10
1	0	1	1	0	0.98
1	0	1	1	1	0.86
1	1	0	0	0	0.75
1	1	0	0	1	0.64
1	1	0	1	0	0.54
1	1	0	1	1	0.43
1	1	1	0	0	0.34
1	1	1	0	1	0.24
1	1	1	1	0	0.15
1	1	1	1	1	0.06

FILTER GROUP DELAY AND SLIMMING LEVEL AS A FUNCTION OF N1 (EAn bits, Reg1) AND N2 (EBn bits, Reg2)

N1	N2	Gdf_C (ns MHz)	SL (dB)
0	0	0.000	0.000
0	1	0.191	0.049
0	2	1.479	0.193
0	3	4.735	0.424
0	4	10.467	0.727
0	5	18.813	1.088
0	6	29.620	1.492
0	7	42.568	1.925
0	8	57.264	2.377
0	9	73.324	2.838
0	10	90.408	3.301
0	11	108.233	3.761
0	12	126.575	4.215
0	13	145.264	4.660
0	14	164.173	5.094
0	15	183.207	5.516
1	0	–0.191	0.049
1	1	0.000	0.098
1	2	1.288	0.243
1	3	4.544	0.473
1	4	10.276	0.776
1	5	18.621	1.137
1	6	29.429	1.541
1	7	42.376	1.974
1	8	57.073	2.426
1	9	73.133	2.887
1	10	90.217	3.350
1	11	108.041	3.811
1	12	126.384	4.264
1	13	145.073	4.709
1	14	163.982	5.143
1	15	183.016	5.566
2	0	–1.479	0.193
2	1	–1.288	0.243
2	2	0.000	0.387
2	3	3.256	0.617
2	4	8.988	0.920
2	5	17.333	1.281
2	6	28.141	1.685
2	7	41.088	2.119
2	8	55.785	2.570
2	9	71.845	3.031
2	10	88.929	3.494
2	11	106.753	3.955
2	12	125.096	4.408
2	13	143.785	4.853
2	14	162.694	5.287
2	15	181.728	5.710
3	0	–4.735	0.424
3	1	–4.544	0.473
3	2	–3.256	0.617
3	3	0.000	0.847
3	4	5.732	1.150
3	5	14.078	1.511
3	6	24.886	1.915
3	7	34.833	2.349
3	8	52.529	2.801
3	9	68.589	3.262
3	10	85.673	3.725
3	11	103.498	4.185
3	12	121.840	4.639
3	13	140.529	5.083
3	14	159.438	5.518
3	15	178.472	5.940
4	0	–10.467	0.727
4	1	–10.276	0.776
4	2	–8.988	0.920
4	3	–5.737	1.150
4	4	0.000	1.454
4	5	8.346	1.815
4	6	19.154	2.219
4	7	32.101	2.652
4	8	46.797	3.104
4	9	62.857	3.565
4	10	79.941	4.028
4	11	97.766	4.488
4	12	116.108	4.942
4	13	134.798	5.387
4	14	153.706	5.821
4	15	172.740	6.243
5	0	–18.813	1.088
5	1	–18.621	1.37
5	2	–17.333	1.281
5	3	–14.078	1.511
5	4	–8.346	1.815
5	5	0.000	2.176
5	6	10.808	2.580
5	7	23.755	3.013
5	8	38.451	3.465
5	9	54.512	3.926
5	10	71.595	4.389
5	11	89.420	4.849
5	12	107.762	5.303
5	13	126.452	5.748
5	14	145.360	6.182
5	15	164.394	6.604
6	0	–29.620	1.492
6	1	–29.429	1.541
6	2	–28.141	1.685
6	3	–24.886	1.915
6	4	–19.154	2.219
6	5	–10.808	2.580
6	6	0.000	2.983
6	7	12.947	3.417
6	8	27.643	3.869
6	9	43.704	4.330
6	10	60.787	4.793
6	11	78.612	5.253
6	12	96.955	5.707
6	13	115.644	6.152
6	14	134.552	6.586
6	15	153.586	7.008
7	0	–42.568	1.925
7	1	–42.376	1.974
7	2	–41.088	2.119
7	3	–37.833	2.349
7	4	–32.101	2.652
7	5	–23.755	3.013
7	6	–12.947	3.417
7	7	0.000	3.851
7	8	14.696	4.302
7	9	30.757	4.763
7	10	47.840	5.226
7	11	65.665	5.687
7	12	84.007	6.140
7	13	102.697	6.585
7	14	121.605	7.019
7	15	140.639	7.442
8	0	–57.264	2.377
8	1	–57.073	2.426
8	2	–55.785	2.570
8	3	–52.529	2.801
8	4	–46.797	3.104
8	5	–38.451	3.465
8	6	–27.643	3.869
8	7	–14.696	4.302
8	8	0.000	4.754
8	9	16.060	5.215
8	10	33.144	5.678
8	11	50.969	6.138
8	12	69.311	6.592
8	13	88.001	7.037
8	14	106.909	7.471
8	15	125.943	7.893

FILTER GROUP DELAY AND SLIMMING LEVEL AS A FUNCTION OF N1 (EAn bits, Reg1) AND N2 (EBn bits, Reg2) (Continued)

N1	N2	Gdf_C (ns MHz)	SL (dB)
9	0	–73.324	2.838
9	1	–73.133	2.887
9	2	–71.845	3.031
9	3	–68.589	3.262
9	4	–62.857	3.565
9	5	–54.512	3.926
9	6	–43.704	4.330
9	7	–30.757	4.763
9	8	–16.060	5.215
9	9	0.000	5.676
9	10	17.084	6.139
9	11	34.908	6.599
9	12	53.251	7.053
9	13	71.940	7.498
9	14	90.849	7.932
9	15	109.883	8.354
10	0	–90.408	3.301
10	1	–90.217	3.350
10	2	–88.929	3.494
10	3	–85.673	3.725
10	4	–79.941	4.028
10	5	–71.595	4.389
10	6	–60.787	4.793
10	7	–47.840	5.226
10	8	–33.144	5.678
10	9	–17.084	6.139
10	10	0.000	6.602
10	11	17.825	7.062
10	12	36.167	7.516
10	13	54.856	7.961
10	14	73.765	8.395
10	15	92.799	8.818
11	0	–108.233	3.761
11	1	–108.041	3.811
11	2	–106.753	3.955
11	3	–103.498	4.185
11	4	–97.766	4.488
11	5	–89.420	4.849
11	6	–78.612	5.253
11	7	–65.665	5.687
11	8	–50.969	6.138
11	9	–34.908	6.599
11	10	–17.825	7.062
11	11	0.000	7.523
11	12	18.342	7.976
11	13	37.032	8.421
11	14	55.940	8.855
11	15	74.974	9.278
12	0	–126.575	4.215
12	1	–126.384	4.264
12	2	–125.096	4.408
12	3	–121.840	4.639
12	4	–116.108	4.942
12	5	–107.762	5.303
12	6	–96.955	5.707
12	7	–84.007	6.140
12	8	–69.311	6.592
12	9	–53.251	7.053
12	10	–36.167	7.516
12	11	–18.342	7.976
12	12	0.000	8.430
12	13	18.689	8.875
12	14	37.598	9.309
12	15	56.632	9.732
13	0	–145.264	4.660
13	1	–145.073	4.709
13	2	–143.785	4.853
13	3	–140.529	5.083
13	4	–134.798	5.387
13	5	–126.452	5.748
13	6	–115.644	6.152
13	7	–102.697	6.585
13	8	–88.001	7.037
13	9	–71.940	7.498
13	10	–54.856	7.961
13	11	–37.032	8.421
13	12	–18.687	8.875
13	13	0.000	9.320
13	14	18.909	9.754
13	15	37.943	10.176
14	0	–164.173	5.094
14	1	–163.982	5.143
14	2	–162.694	5.287
14	3	–159.438	5.518
14	4	–153.706	5.821
14	5	–145.360	6.182
14	6	–134.552	6.586
14	7	–121.605	7.019
14	8	–106.909	7.471
14	9	–90.849	7.932
14	10	–73.765	8.395
14	11	–55.940	8.855
14	12	–37.598	9.309
14	13	–18.909	9.754
14	14	0.000	10.188
14	15	19.034	10.610
15	0	–183.206	5.516
15	1	–183.016	5.566
15	2	–181.728	5.710
15	3	–178.472	5.940
15	4	–172.740	6.243
15	5	–164.394	6.604
15	6	–153.586	7.008
15	7	–140.639	7.442
15	8	–125.943	7.893
15	9	–109.883	8.354
15	10	–92.799	8.818
15	11	–74.974	9.278
15	12	–56.632	9.732
15	13	–37.943	10.176
15	14	–19.034	10.610
15	15	0.000	11.033

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6012CH	0°C to +70°C	32-Pin TQFP (H32)

3.5" R/W MOD Read Channel Back-end Processor

GENERAL DESCRIPTION

The ML6013 is a Read Channel Back-end processor for 3.5" Rewritable Magneto-Optical drives (MOD). It works in conjunction with the ML6012 Read Channel Front-end chip to form a complete integrated Read Channel solution for 128M and 230M MOD drives supporting the ISO standards. It incorporates a full function data synchronizer with a 3:1 operating range, a full function frequency synthesizer with onboard M & N dividers. The most critical blocks on this chip are the three VCOs, one for the data synchronizer PLL, one for the frequency synthesizer PLL and the third VCO is used to generate the tracking 1/4 cell delay for (2, 7) RLL data synchronization. Careful design considerations have been incorporated to minimize the noise coupling and crosstalk among the VCOs. The system noise is highly minimized as the VCO operates at only 2X the data rate.

It provides 40-bits for user programmability of a number of features through a serial microprocessor interface and a bank of internal control registers. The center frequency of the VCO, window centering, M & N dividers and power management options are programmable.

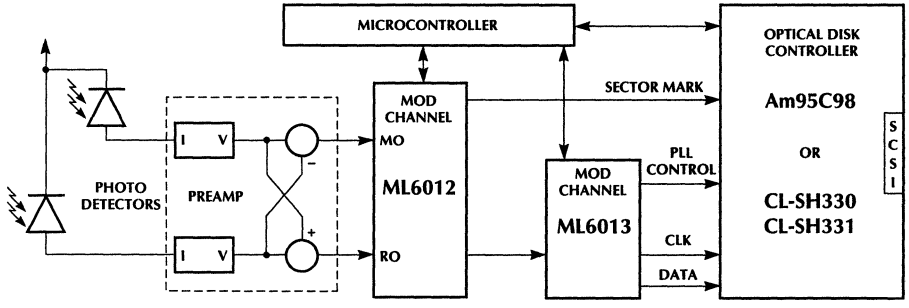
The ML6013 has a typical power dissipation of 350mW in normal mode, and less than 1mW in power down mode. The ML6013 has four levels of power management control for maximum flexibility.

FEATURES

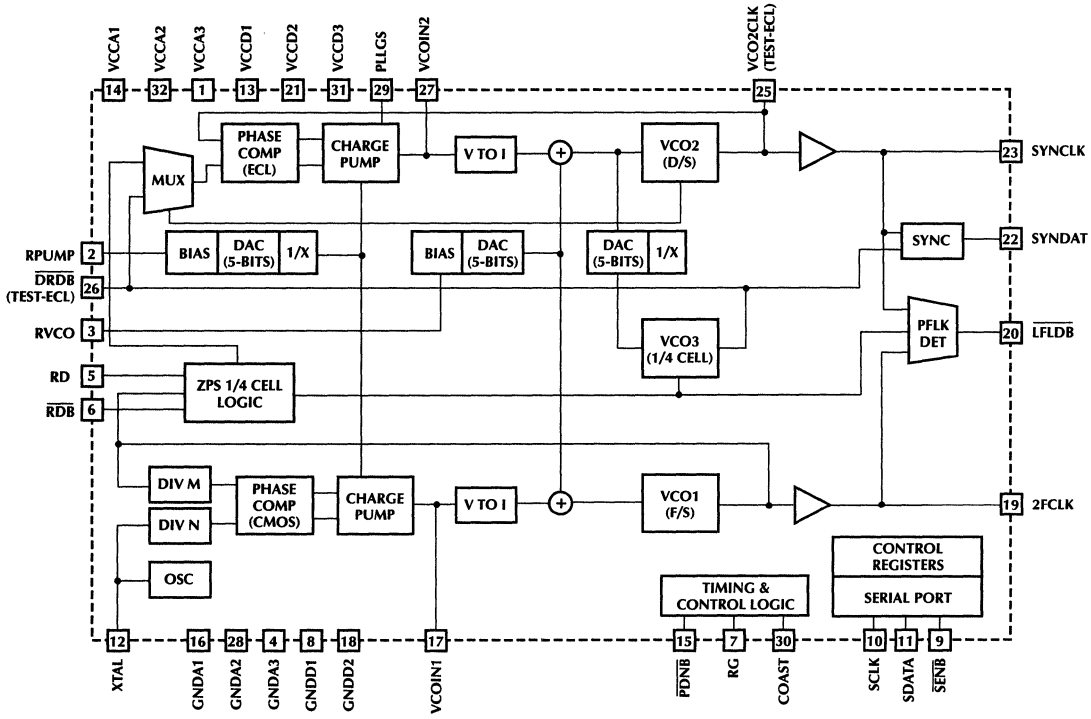
- Supports ISO standards for 128M and 230M R/W Magneto-Optical Drive (MOD)
- Operating supply range 4.5V to 5.5V
- Typical power dissipation is 300mW
- Sleep mode power dissipation less than 1mW
- Low profile, small area, 32-pin TQFP package
- 3:1 NRZ data rate range — 8 to 24 Mbits/s
- Fast acquisition PLL with zero phase start capability
- 3:1 VCO tuning range with 48 Mbits/s 2, 7RLL code rate
- Tracking 1/4 cell delay for handling 2, 7 RLL data
- Programmable VCO center frequency and window centering adjustment (±25% in steps of 1.6%)
- PLL based frequency synthesizer with reference crystal oscillator and M (7-bit) & N (7-bit) dividers
- High speed (20MHz) three wire serial microprocessor interface with double buffered data latches
- Four levels of programmable power management control with external power down pin support
- CMOS, TTL compatible I/O interface for lower power
- Controls provided for manual operation of PLL for recovery from defects

5

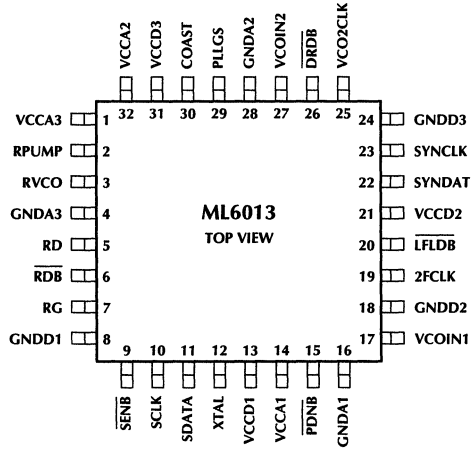
SYSTEM BLOCK DIAGRAM



BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN	NAME	FUNCTION
ECL Level Logic Inputs		
5	RD	Encoded read data from the ML6012 MOD drive read channel front-end processor. The rising edges of RD represent the flux changes on the media. (differential "+" input)
6	$\overline{\text{RDB}}$	Encoded read data from the ML6012 MOD drive read channel front-end processor. The falling edges of RDB represent the flux changes on the media. (differential "–" input)
ECL Level Logic Outputs		
(Note: These are test outputs for characterization purposes. External current sources are necessary to provide driving capability for these signals and the ECL buffer needs to be enabled from Control Register #7)		
25	VCO2CLK	Test point for Data separator VCO clock output.
26	$\overline{\text{DRDB}}$	Delayed read data output after the 1/4 cell delay. This signal is used for 1/4 cell delay characterization and window margin test. The rising edge is phase compared with the rising edge of VCO2CLK.
CMOS Level Logic Inputs		
7	RG	Read Gate signal from the disk controller. Active high signal indicates read mode. This input selects the phase detector input, switches the RRC output, initiates the data separator PLL acquisition.
12	XTAL	A parallel resonant crystal with low parasitic capacitance is connected between this pin and ground as the master clock source. An external clock can be used as an alternative.
15	$\overline{\text{PDNB}}$	Power Down Control. A low level input on this pin puts the chip in the power down (SLEEP) mode.
29	PLLGS	PLL gain select. A high level on this pin places the PLL in low-gain mode. A low places the PLL in high-gain mode.
30	COAST	A high level on this pin disables the phase detector/charge pump of the data separator PLL and allows the VCO to coast.

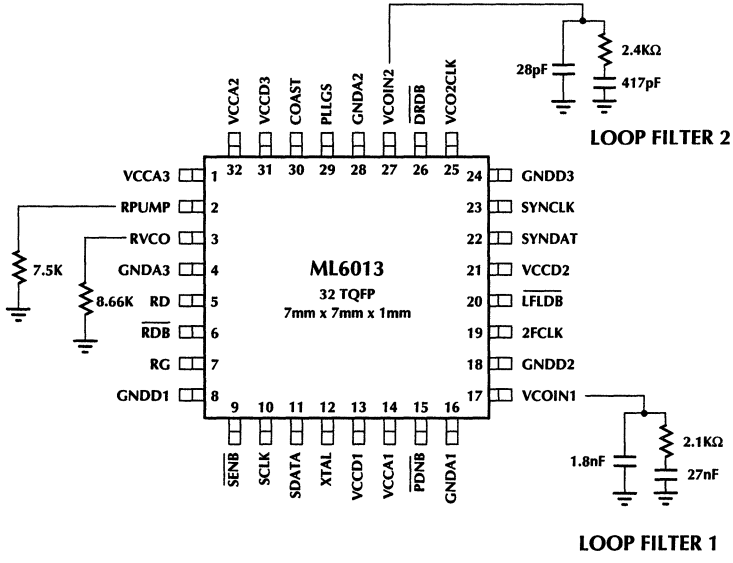
PIN	NAME	FUNCTION
CMOS Level Logic Inputs (continued)		
9	$\overline{\text{SENB}}$	Control Register Enable. Active low CMOS input. A logic low input on this pin allows the SCLK input to clock the SDATA into the control Register and a logic high on this input latches the control register contents.
10	SCLK	This is a CMOS input which clocks the Control Register. Internally this pin is gated with the $\overline{\text{SENB}}$ signal. While $\overline{\text{SENB}}$ is low, address and programming data are clocked in on the falling edges of SCLK.
11	SDATA	Control Register Data, CMOS input, clocked by SCLK.
CMOS Level Logic Outputs		
19	2FCLK	2X clock output from the frequency synthesizer.
20	$\overline{\text{LFLDB}}$	Loss of Phase/Frequency lock detected. This pin outputs a low level signal when the data separator VCO is out of lock or the incoming read data (RD) is missing for a predetermined number of clock (2FCLK) cycles.
22	SYNDAT	This is the synchronized and encoded data from the MOD drive. Data is clocked out on the falling edges of SYNCLK.
23	SYNCLK	Data synchronized clock. This pin outputs 2X (code rate) clock derived from the data separator VCO clock. In the read mode this is the recovered clock from the encoded read data.
Analog Pins		
3	RVCO	A 1% resistor connected between this pin and GNDA3 sets the VCO center frequency which is then programmed via register #3.
2	RPUMP	1% resistor connected between this pin and GNDA3 sets the nominal charge pump current.
17	VCOIN1	Frequency synthesizer PLL charge pump output and VCO input pin. A lowpass filter is connected between this pin and GNDA1.
27	VCOIN2	Data separator PLL charge pump output and VCO input pin. A lowpass filter is connected between this pin and GNDA2.

PIN DESCRIPTION

PIN	NAME	FUNCTION
Power Supplies		
13	VCCD1	5V digital supply
14	VCCA1	5V analog supply for frequency synthesizer.
21	VCCD2	5V digital supply
31	VCCD3	5V digital supply
32	VCCA2	5V analog supply for data separator.

PIN	NAME	FUNCTION
Power Supplies (continued)		
1	VCCA3	5V analog supply for miscellaneous functions.
4	GNDA3	Analog ground for miscellaneous functions
8	GNDD1	Digital Ground
16	GNDA1	Analog ground for frequency synthesizer
18	GNDD2	Digital Ground
28	GNDA2	Analog ground for data separator

TYPICAL EXTERNAL COMPONENTS



ASSUMPTIONS

T_S = 1.5µs @ F_{VCO} = 48MHz

Change pump current = 4X

K_O = 3200A/S/V

$\theta_{e,f} < 20\%$ of $\theta_{e,i}$

$\xi = 0.8$, $\omega_n T = 2.4$

ASSUMPTIONS

F_{XTAL} = 20MHz

N + 1 = 20, M + 1 = 48

K_O = 800A/S/V

$\theta_{e,f} < 1\%$ of $\theta_{e,i}$

T_S = 200µs

$\xi = 0.7$, $\omega_n T = 5$

Note: Loop filter optimized for 24Mbps NRZ operation.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

DC Supply Voltage (VCCA & VCCD) ..... –0.3 to +7V
Analog & Digital Inputs/Outputs ..... –0.3 to VCCA + 0.3V
Input Current per Pin ..... –25 to +25mA
Storage Temperature ..... –65 to +150°C
Maximum Junction Temperature ..... 125°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage Range ..... 4.75V to 5.25V
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VCCA = VCCD = 4.5 to 5.5 volts and T_A = 0 to 70°C, Note 1

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Dissipation					
V_{CC} (VCCA), (VCCD)		4.5		5.5	V
Supply Current	VCCA, VCCD = 4.5V to 5.5V, Data Rate = 24 Mbps, C_L < 15pF				
Read Mode	All circuits operational			80	mA
PLLFS Mode	Data separator, OFF			40	mA
Idle Mode	Only bias circuits & serial interface ON			10	mA
Sleep Mode	All circuits OFF, register contents retained			40	µA
Digital I/O Specifications					
High level input voltage		VCCD – 0.5		VCCD	V
Low level input voltage		GNDD		0.5	V
High level input current	V_{IN} = VCC			0.5	µA
Low level input current	V_{IN} = GND			0.5	µA
High level output voltage	$\|I_{OUT}\|$ = 2mA	VCCD – 0.5		VCCD	V
Low level output voltage	$\|I_{OUT}\|$ = 2mA			0.4	V
High impedance output current	@ V_{IN} = 100mV & VCC – 100mV	–0.5		0.5	µA
DC Characteristics					
Differential Input voltage swing	On ECL input pins RD & $\overline{RDB}$	0.8		1.6	V_{P-P}
Psuedo ECL low level output voltage	@ I_{OUT} = 3mA $\overline{DRDB}$ & VCO2CLK pins	VCCA – 2.05		VCCA – 1.45	V
Psuedo ECL high level output voltage	@ I_{OUT} = 3mA $\overline{DRDB}$ & VCO2CLK pins	VCCA – 1.7		VCCA – 1.3	V
Psuedo ECL output swing		0.15	0.25	0.35	V
Low level input current (Psuedo ECL)	Diff V_{IN} = 0V & VCC – 0.7V (RD & RDB inputs)	0.8	1.0	1.5	mA
High level input current (Psuedo ECL)	Diff V_{IN} = VCC – 0.7V & 0V (RD & RDB inputs)	0.8	1.0	1.5	mA
$V_{RD/RDB}$ common mode	Note 1	1.3	VCCD – 1.4	VCCD – 1.1	V
RPUMP bias voltage	RPUMP = 7.5 KΩ (1%)	0.7	0.75	0.8	V
RVCO bias voltage	RVCO = 7.9KΩ (1%)	0.65	0.79	0.9	V

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Synthesizer					
XTAL or input frequency	Parallel resonant type with minimum capacitance loading	5		20	MHz
M divider register		1		127	Decimal
N divider register		1		127	Decimal
VCO center frequency dynamic range (f_O)	Measure f_H @ VCOIN1 = 0.7V Measure f_L @ VCOIN1 = 2.3V Dynamic range = $(f_H - f_L)/f_1$	±17	±20		%
VCO gain	$\omega_O = 2 \times \pi \times f_O$, $K_{VCO} = \pi \times (f_1 - f_2)/100mV$ f_1 @ VCOIN1 @ f_O + 100 mV f_2 @ VCOIN1 @ f_O – 100 mV	0.25	0.35	0.44	rad/s-V
Pump current resistor	for setting pump current (±1%)		7.5		Kohms
Phase detector gain	$Kd = (I_O \times 48MHz) / (2 \times \pi \times f_O)$ $I_O = 0.75V/(2 \times R_{PUMP})$	0.80Kd	Kd	1.20Kd	A/rad
PLL loop gain	$G_O = 6.3 \times 10^6 / R_{PUMP}$	0.70 G_O	G_O	1.30 G_O	A/s x V
PLLFS RMS jitter ± 1 Sigma	Note 2			600	ps
Read Mode and Data Synchronizer					
VCO center frequency dynamic range (f_O)	Measure f_H @ VCOIN2 = 0.7V Measure f_L @ VCOIN2 = 2.3V Dynamic range = $(f_H - f_L)/f_1$	±10	±20		%
VCO gain	$\omega_O = 2 \times \pi \times f_O$, $K_{VCO} = \pi \times (f_1 - f_2)/100mV$ f_1 @ VCOIN1 @ f_O + 100 mV f_2 @ VCOIN1 @ f_O – 100 mV	0.25	0.35	0.44	rad/s – V
Phase detector gain	$Kd = (I_O \times 48MHz) / (2 \times \pi \times f_O)$ $I_O = (2 \times 0.75V)/R_{PUMP}$	0.80Kd	Kd	1.20Kd	A/rad
PLL loop gain	$G_O = 25.2 \times 10^6/R_{PUMP}$ (during preamble)	0.70G_O	G_O	1.30G_O	A/s x V
VCO ZPS error	(zero phase start)	–0.05T – 2		+0.05T + 2	ns
1/4 cell delay accuracy	relative to T/2			±5	%
Decode window centering accuracy	WC4 = 0 WC0 – 3 = 1, (Code rate = 48MHz)			±14	%
RD input pulse width	t_{WRD}	15		T	ns
RRC duty cycle	WG = 0, RG = 1	35		65	%
PLLDS RMS jitter, ± 1 Sigma	WG = 0, RG = 1, (Code rate = 48Mhz) Note 2			1	ns

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Read Mode and Data Synchronizer (continued)					
RRC to NRZout delay	t_{DNRZ1}			5	ns
RG to valid NRZout delay	t_{DNRZ2}		6TRRC		ns
Serial Microprocessor Interface					
Serial clock (SCLK) frequency		0.01		20	MHz
SCLK pulse width	t_{PW}	20			ns
SCLK to SDATA hold time	t_{HSD}	10			ns
SDATA to SCLK setup time	t_{SSD}	10			ns
SENB to SCLK setup time	t_{SSEN}	10			ns

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 2: The ±1 sigma RMS jitter is one standard deviation of the distribution of the edge transition time. The peak-to-peak is twice the value shown.

TIMING DIAGRAMS

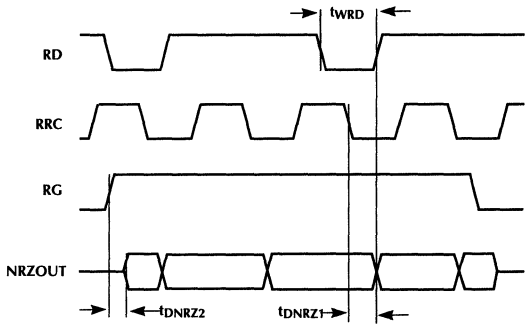


Figure 1. Read Mode Timing

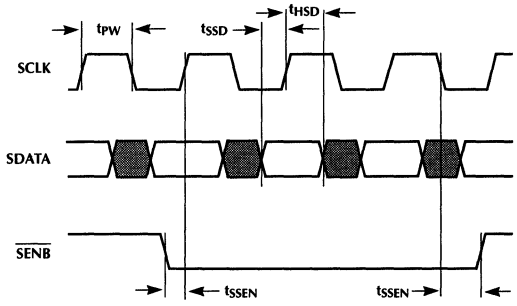


Figure 2. Serial Port Timing

FUNCTIONAL DESCRIPTION

The ML6013 is a BiCMOS MOD Read Channel Back-end Processor IC which works in conjunction with the ML6012 MOD Read Channel Front-end Processor to form a complete solution for the next generation of 3.5" Rewritable Magneto-Optical Drives (MOD). It incorporates a full function data synchronizer with a 3:1 operating range and a full function frequency synthesizer with onboard M & N dividers.

The most critical blocks on this chip are the three VCOs, one for the data synchronizer PLL, one for the frequency synthesizer PLL and the third VCO is used to generate the tracking 1/4 cell delay for (2, 7) RLL data synchronization. Careful design considerations have been incorporated to minimize the noise coupling and crosstalk among the VCOs. The highlights of the ML6013 VCO architecture are that it is a fully differential, high speed circuit with built-in switching. It provides a constant amplitude across the frequency span with on-chip timing capacitors. The system noise is highly minimized as the VCO operates at only 2X the data rate.

It provides 40-bits for user programmability of a number of features through a serial microprocessor interface and a bank of internal control registers. The control registers come up in an undetermined state on physical power-up and hence need to be initialized, to setup the ML6013 in a known state, on power-up. The control registers will retain their contents in all the power down modes, until power is physically switched off to the chip. The center frequency of the frequency synthesizer VCO is programmed with a 5-bit current DAC. The program information can be provided by the user, or it can be derived from the M & N information. The VCO control current results from the summation of this DAC based coarse control and PLL based fine control. The center frequency of the data separator VCO is programmed by duplicating the control current in the frequency synthesizer VCO as the coarse control. This leaves only the data rate variation to be fine tuned by the PLL, hence implying lower sensitivity and better jitter performance. The VCO3 period is programmed from a 5-bit current DAC, which is in turn referenced to the VCO2 control current. This will vary the 1/2 cycle of VCO3 for the required window centering programmability.

The ML6013 supports four power down modes for implementation of intelligent power management schemes. An external hardware pin is also provided to implement real time power management. In the sleep mode all sections are powered down except the serial microprocessor interface.

The ML6013 accepts the raw data in a pseudo ECL voltage level, as generated by the ML6012 and provides the synchronized data and clock outputs for the optical disk controller.

VCO ARCHITECTURE

The most critical circuit blocks in the ML6013 are the three VCOs. The first VCO is used in the frequency synthesizer PLL, the second VCO is used in the data separator PLL and the third VCO is used to generate the tracking 1/4 cell delay for (2, 7)RLL data synchronization.

The VCO architecture is optimized to minimize noise coupling from the digital sections of the chip and also the cross talk among the VCOs. The highlights of the VCO architecture are:

- High speed operation with built-in switching mechanism for optimized performance.
- Fully differential circuit configuration to achieve high level of noise immunity.
- On chip timing capacitors to control accuracy and for better noise immunity.
- Constant amplitude across frequency span.
- Symmetrical waveform (~50% duty cycle).

The operating frequency of the VCO is controlled by the tail current of the VCO which consists of two components — a fixed but programmable current (coarse), generated from a DAC which is controlled by the control register #3 and a variable current generated from the PLL. The coarse setting sets the center frequency of the VCO near the operating frequency and the negative feedback around the PLL is used to tune the VCO into the target operating frequency. To minimize the dependence on process and temperature variations the DAC current is derived using an external 1% resistor R_{VCO}. The center frequency is given by the equation:

$$f_O = \frac{m+17}{(16 \times R_{VCO} \times C)}$$

where m = 0 to 31 from control register #3

C = internal capacitor

R_{VCO} = 7.87 kΩ, 1% (recommended)

The architecture of the VCOs is such that they run at 2X the data rate. This reduces the speed requirements of the circuits and also helps in minimizing crosstalk between the VCOs, thus contributing towards overall system noise immunity. The output of the VCO is sent to a frequency doubler to generate the 4X frequency locally which is then divided by 2 or 4 to generate the synchronized 2X and 1X clocks. Zero phase start of the data separator VCO is supported for initial phase alignment.

PLL ARCHITECTURE

There are two PLLs implemented to realize the data separation (for data and clock recovery) and frequency synthesis function (required to support a zoned bit recording (ZBR) implementation). Shown below is a block diagram of the PLL which requires a first order loop filter.

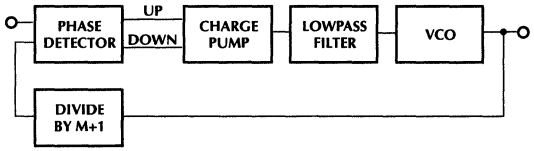


Figure 3. Block Diagram of PLL.

To design the PLL response with a well controlled loop gain value, an external 1% resistor (R_{PUMP}) is used to set the charge pump current according to the bandgap reference voltage generated on chip. The recommended value for Rpump is 7.5kΩ. The capacitor in series with the resistor in the loop filter is chosen so that typically it is 10 times the other capacitor. The resistor is chosen to yield a damping factor between 0.5 and 1 for the acquisition performance of the PLL.

FREQUENCY SYNTHESIZER PLL

In a Zone Bit Recording (ZBR) implementation, the disk is divided into a number of zones and the data rate varies from zone to zone. In order to support a ZBR implementation the appropriate frequencies need to be synthesized. VCO1 is used in the ML6013 frequency synthesizer to generate a clock with frequency f_{VCO1}. This is given by the formula:

$$f_{VCO1} = \frac{(M+1) \times f_{XTAL}}{(N+1)}$$

where M and N are 7-bit dividers, programmable through control registers #6, 5, 4. M and N should be at least 1 so that the divide ratio in both the forward and feedback paths are no less than 2, as that 50% duty cycle is guaranteed for the phase compared clocks. In a typical application the users keeps the N at a fixed value and reprograms M from zone to zone to synthesize the required frequency. A 2.5:1 span is required for most applications. The synthesized VCO1 clock is used to derive the 2FCLK clock. The VCO1 clock is also used to train VCO2 PLL during the non-read mode. The charge pump gain can be controlled through the CPG1 bit in control register #0. The default is always 1X gain. The frequency synthesizer PLL bandwidth is relatively low (~10KHz) for jitter performance.

The coarse center frequency of the frequency synthesizer VCO is programmed with a 5-bit current DAC in conjunction with control register #3. This speeds up the frequency acquisition and also minimizes the VCO sensitivity to V_{VCOIN1} and improves the jitter performance. The synthesized frequency is tuned using the M & N divider information and the crystal frequency, as given by the equation above.

PLL LOOP FILTER DESIGN FOR FREQUENCY SYNTHESIZER

To select the components for the loop filter, two parameters, ξ (damping factor) and ω_n (natural frequency) of the loop characteristic need to be specified.

It is desirable to have the damping factor ξ between 0.5 and 1 to prevent locking to harmonics while maintaining an acceptable lock time. For a high gain, second-order loop this results in minimum noise bandwidth.

The desired natural frequency ω_n of the loop is determined by satisfying the acquisition time (1% maximum phase error after phase acquisition) which is less than the minimum track-to-track seek time. This yields a settling time of approximately $t_S = 5/\omega_n$.

The formula for the filter components are shown in equations (1) and (2).

$$C_1 = \frac{K_O}{(M+1)\,\omega_n^{\,2}} \qquad (1)$$

$$R = \frac{2\xi\omega_n (M+1)}{K_O} \qquad (2)$$

where $K_O = K_D K_{VCO}$ (open loop gain)

The operating frequency F_{VCO} (code rate) is programmed by M&N registers. Equation (3) shows the programming relationship.

$$F_{VCO} = \frac{(M+1)}{(N+1)} \times F_{XTAL} \qquad (3)$$

The value of N should be fixed in the above equation and allow only the M to change for desired operating frequency.

Loop Filter Design Example:

NRZ data rate = 12 to 24 Mbps (1:2 ratio)
Code rate, F_{VCO} = 24 to 48MHz
(assumes (2, 7) RLL code)
F_{XTAL} = 20MHz
Choose N = 19, ⇒ M = 23 to 47
$K_D K_{VCO}$ = 800 A/S/V

Let the loop damping factor, ξ = 0.7 at F_{VCO} = 48MHz to allow ξ to rise at lower frequencies. Let ω_n = 25Krad/s (relatively low frequency, in the order of tens Krad/s for better jitter performance). This value produces a loop settling time = 200μs.

from eqn. (3) M + 1 = 48
from eqn. (1) $C_1 = 27nF \Rightarrow C_2 = C_1/15 = 1.8nF$
from eqn. (2) R = 2.1KΩ

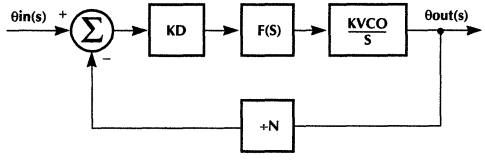
At F_{VCO} = 24MHz, M+1 = 24 which yields ξ = 1.0, and ω_n = 35Krad/s.

DATA SEPARATOR PLL

The center frequency of VCO2 is programmed by duplicating the control current in the VCO1 as the coarse control (control register #3). VCOIN2 thus has to do the fine tuning due to data rate variations (less than several percent), thus implying low sensitivity and good jitter performance. This is an important factor because the data separator PLL has higher bandwidth (of the order of 100KHz) to track the data rate variations and is hence more susceptible to noise induced jitter.

The charge pump has two modes of operation. During the non-read mode, the VCO clock is compared to the frequency synthesizer clock in every cycle, hence the charge pump should operate in the low gain mode (PLLGS = 1). After Read Gate is asserted, VCO clock is compared to the preamble data on every third clock (assuming 3T preamble pattern for (2, 7) RLL code). The charge pump should switch to the high gain mode (PLLGS = 0) to partially compensate for the loss of phase detector gain. This switching is necessary to maintain the damping factor in the PLL during the initial acquisition for guaranteed frequency lock after 24 preamble bytes. After the initial acquisition, the charge pump is switched back into the low gain mode for better jitter and noise performance.

The overall block diagram for the PLL can be described as:



where N = The ratio of the VCO frequency to the input frequency

To select the components for the loop filter, the user needs to consider the following loop requirements:

1. Residual phase error at the end of the preamble should be less than 4% of the total synchronization window (i.e. θ_e < 1ns for F_{VCO} = 48MHz or T_W = 20.8ns). This implies a large loop bandwidth so that it can quickly obtain lock within a predetermined length of the preamble field.
2. The lock-in range $\Delta\omega_L$ must be larger than the expected frequency step change due to variations in disk rotational velocity. In today's technology, the disk rotational velocity can be well controlled within ±1%.
3. The natural frequency ω_n and the damping factor ξ of the loop must be minimized to achieve maximum jitter rejection in the data field. The minimum value for the damping factor ξ will be 0.5 for adequate stability.
4. Re-lock time to the reference clock (frequency synthesizer) must be less than the minimum track-to-track seek time.

It is generally valid to assume the minimum value of ω_n is dominated by the bandwidth needed during preamble from requirement #1. This assumption will be checked in the design example.

The following loop filter design example assumes:

a. (2, 7) RLL code

b. The PLL encounters a phase offset instead of a frequency offset of the incoming data at the initial lock acquisition. The zero phase start function minimizes the initial phase offset to ±(0.2T + 2)ns where T = synchronization window.

Since the highest data rate yields the minimum amount of time that the PLL has to settle before decoding data, the settling time is calculated based on the highest data rate.

Loop Filter Design Example:

NRZ data rate = 24MHz
Code rate, F_{VCO} = 48MHz
N_{MIN} = 3 (during preamble, highest recorded frequency)
N_{MAX} = 8 (lowest recorded frequency)
Preamble length = 24 of 3T (100) pattern
T_S (settling time of PLL) = 3 x 24 ÷ 48MHz = 1.5µs
Initial phase error $\theta_{e,i}$ = 3ns
Final phase error (after T_S) $\theta_{e,f}$ < 20% of $\theta_{e,i}$
K_O = 3200 A/S/V during preamble

It is desirable to have the damping factor ξ between 0.5 and 1 during acquisition. For a high gain, second-order loop this results in minimum noise bandwidth.

Let the loop damping factor ξ = 0.9 to allow ξ to drop at N ≠ 3
As shown in figure 4, with ξ = 0.9, choosing $\omega_n T$ = 2.4 the phase error will be at most 20% of the initial phase error. Since T_S = 1.5µs, ω_n = 1.6Mrad/s.

If the previous assumption is correct, ω_n = 1.6Mrad/s should meet the loop requirements 2 and 4. First, examining requirement #2:

Let the maximum frequency step Δf = ±1% of the preamble frequency
Δf = ± 0.01 x 48MHz ÷ 3 = ±160KHz
Lock-in range is given by
$\Delta\omega_L = 2\xi\omega_n$ = 2 x 0.9 x 1.6Mrad/s = 2.88 Mrad/s

Thu, Δf_L = 458KHz > 160KHz and requirement #2 is met.

User is encouraged to check that ω_n = 1.6Mrad/s during preamble does meet the requirement #4.

Recall the equations for determining the filter components:

$$C_1 = \frac{K_O}{N \times \omega_n^2} \quad (4)$$

$$R = \frac{2\xi\omega_n N}{K_O} \quad (5)$$

from eqn. (4) $C_1 = 417pF \Rightarrow C_2 = C_1/15 = 28pF$
from eqn. (2) $R = 2.7K\Omega$

The above analysis is only shown as an example. The calculated values for filter components are most likely not optimized for all systems using the same data rate, code and preamble.

1/4 CELL DELAY & SYNCHRONIZER

The synchronizer circuit aligns the encoded read data pulses to the data separator VCO clock for the external decoder. Each rising edge of the encoded read data (RD) activates the following events:

1) It enables the 1/4 cell delay (VCO3 for half of a cycle) to generate a $\overline{\text{DRDB}}$ (delayed read data) pulse. The width of the $\overline{\text{DRDB}}$ pulse can be programmed by changing the tail current of VCO3. In normal operation, VCO3 is biased at the same current level as VCO2 so the half cycle pulse width is equivalent to 1/4 of the NRZ data period.

2) The falling edges of $\overline{\text{DRDB}}$ enable the phase detector, which operates in phase only mode during a read operation, so that the rising edges of the $\overline{\text{DRDB}}$ will be phase compared to the rising edges of VCO2 clock. The negative feedback around the PLL eventually aligns the rising edge of the $\overline{\text{DRDB}}$ to the rising edge of the VCO2 clock.

3) The falling edges of $\overline{\text{DRDB}}$ set the output of an internal Data Register (DR) flip-flop to 1, so the following rising edges of the VCO2 clock will clock it into the synchronizer. After the 1 is clocked into the synchronizer, DR is reset to 0 and the following VCO2 clocks will clock in 0's to the synchronizer until the DR is set by another read pulse.

   VCO3 period is programmed from a 5-bit current DAC which is in turn referenced to VCO2 control current. This will vary the 1/2 cycle of VCO3 for the required window centering programmability while performing window margin test.

LOSS OF PHASE/FREQUENCY LOCK DETECTOR

The loss of phase detector will bring the output $\overline{\text{LFLDB}}$ low after the encoded read data (RD) has been missing for a certain number of clock cycles due to surface defects. The internal control registers P1 and P0 determine the number of clock cycles to be used as reference. The loss of frequency detector detects if the VCO2 has locked to the harmonics of the incoming read data (in phase only mode) by comparing the frequency of VCO2 with the frequency of VCO1. The frequency detector guarantees a low output at $\overline{\text{LFLDB}}$ when it sees more than 10.5% difference in the frequency between VCO2 and VCO1 (the closest harmonic frequency that the VCO2 can lock to will be approximately ±12.5% from the operating channel frequency, 2FCLK). To allow margin for frequency offset in the recovery clock (SYNCLK) due to frequency variations, the frequency detector also guarantees no frequency offset detection if the SYNCLK is within ±3.5% of the 2FCLK.

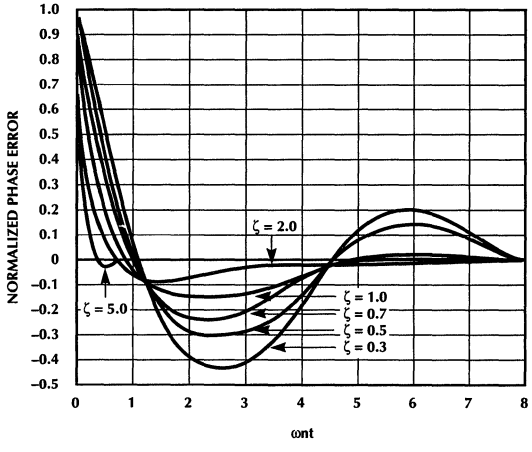


Figure 4. Transient phase error $\theta_e(t)$ due to a step in phase $\Delta\theta$.

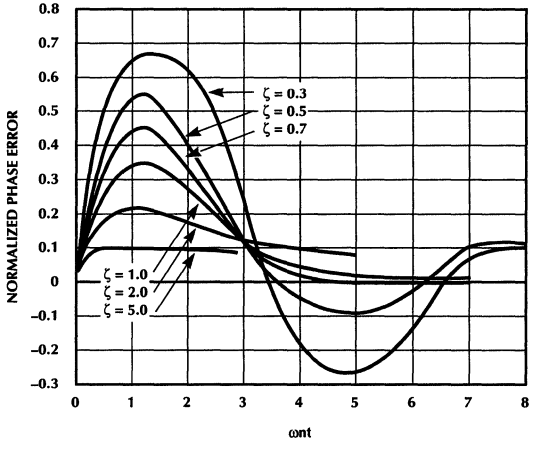


Figure 5. Transient phase error $\theta_e(t)$ due to a step in frequency $\Delta\omega$.

READ MODE OPERATION OF THE ML6013

When Read Gate (RG) is inactive low, the data separator PLL is locked to the VCO1 clock with the phase detector operating in the phase/frequency mode.

When Read Gate (RG) goes active high, (PLLGS should go low as RG goes high) the chip enters the read mode. The internal counter starts counting the number of pulses received on the RD/$\overline{\text{RDB}}$ input. After 8 RD pulses the VCO2 is stopped. VCO2 will restart at the next input transition. The zero phase start circuit eliminates the initial misalignment and speeds up the PLL acquisition. When RG is reasserted (PLLGS should stay high) after VCO2 recovers from the surface defects, zero phase start will be active immediately without counting another 8 RD pulses. When VCO2 restarts, the phase detector is switched to phase only mode with the input connected to DRD (delayed read data). The phase detector gain is also increased by 4X (CPG2 = 1) to ensure that the PLL has enough bandwidth and the right damping factor to lock within 24 preamble bytes. After 24 more RD pulses the PLL acquisition is assumed complete. The phase detector gain is then switched to the low gain mode (1X) for better jitter and noise performance. The phase detector gain will be automatically set when the PLLGS signal is not available from the controller. The 1-bit control "EXT" from the control register determines whether the PLLGS is controlled externally.

The end of the read operation is signalled by Read Gate going inactive low. VCO2 is stopped again and is restarted, synchronized with VCO1. Circuitry is implemented to ensure a glitchless transition of the clock frequencies on the RRC output.

POWER MANAGEMENT

The ML6013 provides a hardware pin ($\overline{\text{PDNB}}$) and two bits in control register #7 for multiple levels of power management control.

The major circuit blocks in the ML6013 are the serial interface, VCO1 and frequency synthesizer PLL, VCO2 and data separator PLL, VCO3, synchronizer, bias circuits and I/O circuits. The PDNB pin in conjunction with the 2 bits in control register #7 can be used to selectively turn off a combination of these blocks depending on the mode of operation. This allows the system designer to turn off sections of the chip that are not in use during a particular sequence of events, thus minimizing power dissipation at a micro management level. Table 1 shows these different power down modes and the circuit blocks affected in these different modes. Total typical power dissipation has two components — analog power dissipation which is more or less constant and digital power dissipation which varies with operating data rate.

SERIAL MICROPROCESSOR INTERFACE

The serial microprocessor interface consists of a simple three-wire serial port. Data is shifted serially into the ML6013 on the SDATA line on the falling edges of the serial shift clock, SCLK, provided the $\overline{\text{SENB}}$ pin is active (low). The data is shifted in blocks of eight bits with MSBit first. The internal registers are organized in blocks of eight bits, with the three most significant bits denoting the address, followed by the five data bits. This addressing scheme allows for a register bank of eight registers. When the chip is physically powered-up, the control registers come up in an undetermined state and hence they need to be initialized to some preset configuration, so that the behavior of the chip is predictable. The control registers retain their programmed information in all the power-down modes, except when the chip is physically powered-down. When the $\overline{\text{SENB}}$ pin goes inactive (high), the SDATA and SCLK pins are ignored and the previously shifted information is latched on the rising edge of the $\overline{\text{SENB}}$, into the appropriate register bank based on the address bits. It is recommended that the SCLK input be kept inactive low when it is in use. The SCLK input is capable of handling speeds up to 20MHz.

Table 1: Power down modes in the ML6013 with typical power dissipation

POWER DOWN MODE	SLEEP	IDLE	PLL	READ	PDWN	MAX WAKE UP TIME (ms)
PDNB pin	high	high	high	high	low	—
PM1, PM0	00	01	10	11	XX	—
VCO1 and PLLFS	off	off	on	on	off	0.5
VCO2, PLLDS VCO3 and Synchronizer	off	off	off	on	off	0.1
Bias and I/O circuits	off	on	on	on	off	0.02
XTAL Oscillator	off	on	on	on	off	100
Serial Interface	on	on	on	on	on	0
Typical analog power dissipation (mA)	<0.1	6	14	37	<0.1	—

CONTROL REGISTER DEFINITIONS

The control register bank consists of eight registers with addresses from 0 through 7. Outlined below are the detailed bit by bit definitions of the control registers 0 through 7.

CONTROL REGISTER #0

Miscellaneous Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	0	0	CPG2	CPG1	K2	K1	EXT

EXT = 0 PLLGS function is controlled internally
EXT = 1 PLLGS function is controlled externally

K1 = 0 Disable VCO1
K1 = 1 VCO1 is enabled

K2 = 0 Disable VCO2
K2 = 1 VCO2 is enabled

CPG1 = 0 Frequency synthesizer Phase detector gain is set to 1X
CPG1 = 1 Frequency synthesizer Phase detector gain is set to 2X

CPG2 = 0 Data separator phase detector gain is set to 2X during preamble acquisition
CPG2 = 1 Data separator phase detector gain is set to 4X during preamble acquisition and remains at 4X during read mode when EXT = 1 and PLLGS = 0

CONTROL REGISTER #1

Loss of Frequency Detection Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	0	1	RSVD	P1	P0	EFB	EPB

EPB = 0 Enable loss of phase lock detection
EPB = 1 Disable loss of phase lock detection

EFB = 0 Enable loss of frequency lock detection
EFB = 1 Disable loss of frequency lock detection

P1, P0 The combination of these two bits programs the number of VCO1 clock cycles that can elapse without RD present, before a loss of phase is detected in the LFLD circuit. This is shown in the table below:

P1	P0	NUMBER OF VCO1 CYCLES
0	0	12
0	1	20
1	0	22
1	1	28

CONTROL REGISTER #2

Data separator PLL window centering control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	1	0	WC4	WC3	WC2	WC1	WC0

WC4	WC3	WC2	WC1	WC0	VALUE
0	0	0	0	0	–24.0 %
0	0	0	0	1	–22.4 %
0	0	0	1	0	–20.8 %
0	0	0	1	1	–19.2 %
0	0	1	0	0	–17.6 %
0	0	1	0	1	–16.0 %
0	0	1	1	0	–14.4 %
0	0	1	1	1	–12.8 %
0	1	0	0	0	–11.2 %
0	1	0	0	1	–9.6 %
0	1	0	1	0	–8.0 %
0	1	0	1	1	–6.4 %
0	1	1	0	0	–4.8 %
0	1	1	0	1	–3.2 %
0	1	1	1	0	–1.6 %
0	1	1	1	1	0 % (center)
1	0	0	0	0	+1.6 %
1	0	0	0	1	+3.2 %
1	0	0	1	0	+4.8 %
1	0	0	1	1	+6.4 %
1	0	1	0	0	+8.0 %
1	0	1	0	1	+9.6 %
1	0	1	1	0	+11.2 %
1	0	1	1	1	+12.8 %
1	1	0	0	0	+14.4 %
1	1	0	0	1	+16.0 %
1	1	0	1	0	+17.6 %
1	1	0	1	1	+19.2 %
1	1	1	0	0	+20.8 %
1	1	1	0	1	+22.4 %
1	1	1	1	0	+24.0 %
1	1	1	1	1	+25.6 %

CONTROL REGISTER #3

VCO Coarse Center Frequency Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	1	1	CF4	CF3	CF2	CF1	CF0

CF4	CF3	CF2	CF1	CF0	F_O MHZ
0	0	0	0	0	17 MHz
0	0	0	0	1	18 MHz
0	0	0	1	0	19 MHz
0	0	0	1	1	20 MHz
0	0	1	0	0	21 MHz
0	0	1	0	1	22 MHz
0	0	1	1	0	23 MHz
0	0	1	1	1	24 MHz
0	1	0	0	0	25 MHz
0	1	0	0	1	26 MHz
0	1	0	1	0	27 MHz
0	1	0	1	1	28 MHz
0	1	1	0	0	29 MHz
0	1	1	0	1	30 MHz
0	1	1	1	0	31 MHz
0	1	1	1	1	31 MHz
1	0	0	0	0	33 MHz
1	0	0	0	1	34 MHz
1	0	0	1	0	35 MHz
1	0	0	1	1	36 MHz
1	0	1	0	0	37 MHz
1	0	1	0	1	38 MHz
1	0	1	1	0	39 MHz
1	0	1	1	1	40 MHz
1	1	0	0	0	41 MHz
1	1	0	0	1	42 MHz
1	1	0	1	0	43 MHz
1	1	0	1	1	44 MHz
1	1	1	0	0	45 MHz
1	1	1	0	1	46 MHz
1	1	1	1	0	47 MHz
1	1	1	1	1	48 MHz

CONTROL REGISTER #4

Divide by N Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	0	0	N6	N5	N4	N3	N2

CONTROL REGISTER #5

Divide by M Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	0	1	M6	M5	M4	M3	M2

CONTROL REGISTER #6

Divide by M & N and endec control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	1	0	RSVD	M1	M0	N1	N0

M & N are given by :

$$M = M6 \times 26 + M5 \times 25 + M4 \times 24 + M3 \times 23 + M2 \times 22 + M1 \times 21 + 1$$

or

$$M = 64 \times M6 + 32 \times M5 + 16 \times M4 + 8 \times M3 + 4 \times M2 + 2 \times M1 + 1$$

and

$$N = N6 \times 26 + N5 \times 25 + N4 \times 24 + N3 \times 23 + N2 \times 22 + N1 \times 21 + 1$$

or

$$N = 64 \times N6 + 32 \times N5 + 16 \times N4 + 8 \times N3 + 4 \times N2 + 2 \times N1 + 1$$

Note: The 7-bit M & N values are updated (latched) internally only when the most significant bit (M6 or N6) is written to, irrespective of changes in any other bits.

CONTROL REGISTER #7

Power Down Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	1	1	RSVD	BUF	0	PM1	PM0

BUF = 1 This bit enables the ECL output buffers so that the test signals $\overline{\text{DRDB}}$ and VCO2CLK are made available to the user.

BUF = 0 This disables the ECL output buffer, thus minimizing power dissipation.

D2 = 0 Reserved, must be programmed as "0" at all times.

Bit configuration for power down modes

PDNB	PM1	PM0	MODE
1	0	0	SLEEP
1	0	1	IDLE
1	1	0	PLL
1	1	1	READ
0	X	X	PDOWN

Note: PDOWN dissipation is the same as SLEEP mode

5

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6013CH	0°C to +70°C	32-Pin TQFP (H32)

ML6024

16 Mbps Filter/Equalizer for Tape Drives

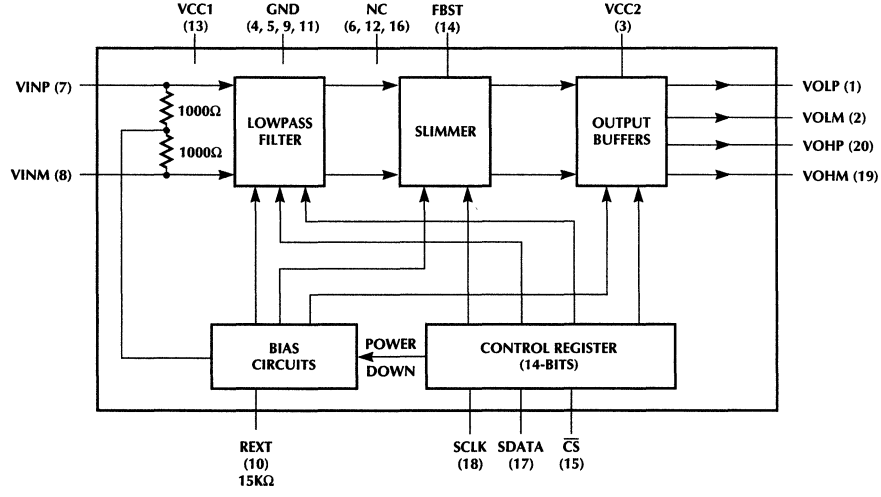
GENERAL DESCRIPTION

The ML6024 is a monolithic analog filter/equalizer intended for tape drive read channel applications, capable of handling disk data rates up to 16 Mbps, with an operating power dissipation less than 300mW. Its architecture consists of a continuous type filter based on a transconductor and a high speed parasitic free active integrator, allowing complete independence of the filter response from interconnect parasitics, thus realizing a family of frequency response curves optimized for tape drive read channel equalization, especially to handle the different format and media types, for ensuring backward compatibility. It consists of a programmable 6-pole 2-zero lowpass filter stage, two pairs high-speed drivers, and a serial microprocessor interface. The poles of the transfer function approximate a maximally flat group delay (modified bessel type) response, whereas the symmetric zeros provide the high-frequency boost necessary for equalization. The user can independently program the corner frequency, as well as the slimming level and individual bits for power-down, read/write control, and auto-zero control.

FEATURES

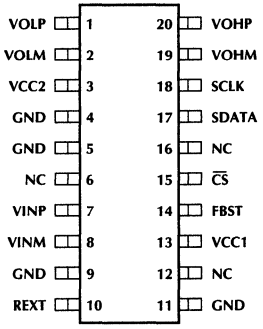
- 6-pole, 2-zero continuous time filter with < –45dB harmonic distortion
- Data transfer rates up to 16 Mbps
- Programmable filter cutoff frequency
  (4.3:1 range in 64 steps)
  (f_C = 2 to 9MHz)
- 32 step programmable pulse slimming equalization, 0 to 10dB boost at f_C.
- Power-down, auto-zero, R/W modes programmable through bits in the control register
- Lowpass output and differentiated lowpass (bandpass) output provided.
- Fully I/O balanced architecture with TTL/CMOS compatible interface
- High speed (up to 20MHz clock) three wire serial microprocessor interface
- Double buffered data latch for synchronous or asynchronous data loading.
- External pin to disable the slimmer
- Single 5V ± 10% power supply
- Available in 20-pin SSOP package.
- 4 GHz/1.5µ BiCMOS process
- Power Dissipation — P_{OPR} = 300mW, P_{DN} = 7.5mW
- Gm set through an external 15KΩ (REXT) resistor

BLOCK DIAGRAM



PIN CONNECTION

20-Pin SSOP



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1 2	VOLP VOLM	Normal Lowpass outputs
3	VCC2	Positive supply for the output drivers, 5V ± 10%
4, 5, 9, 11	GND	Ground
7 8	VINP VINM	Signal Inputs
10	REXT	A 15K resistor between this pin and ground sets corner frequency
13	VCC1	Positive supply, 5V ± 10%
14	FBST	Slimmer Enable pin. A high input level allows normal operation of the filter. A low level input disables the slimmer, resulting in 0dB boost. A TTL input.

PIN#	NAME	FUNCTION
15	$\overline{CS}$	Control Register Enable. A logical low level allows the SCLK input to clock data into the control register via the SDATA input line. A logical high level latches the control register contents and issues the information to the appropriate circuitry. A TTL input.
17	SDATA	Control Register Data. A TTL input
18	SCLK	Control Register Clock. Negative edge triggered control register clock input. A TTL input.
19 20	VOHM VOHP	Differentiated lowpass outputs
6, 12, 16	NC	No Connects, reserved for future use.

5

ML6025

24 Mbps Read Channel Filter/Equalizer

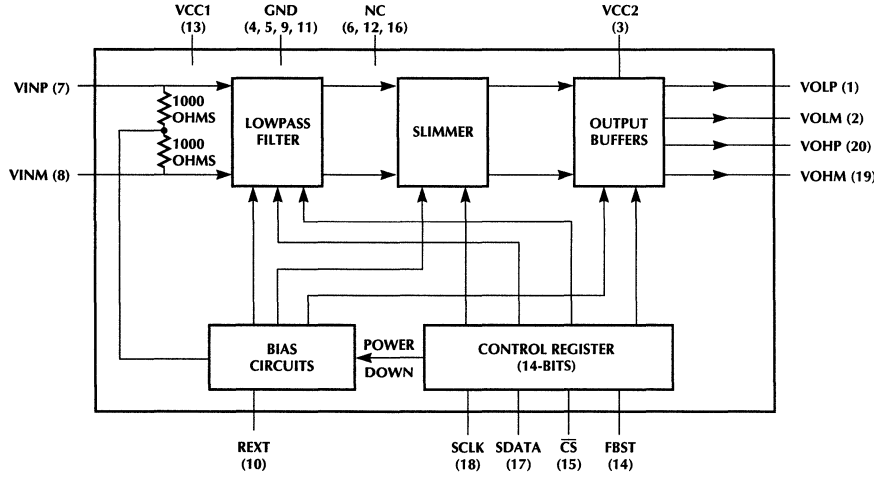
GENERAL DESCRIPTION

The ML6025 is a monolithic analog filter/equalizer intended for hard disk drive read channel applications, capable of handling disk data rates upto 24Mbits/s, with an operating power dissipation of less than 300mW. Its architecture consists of a continuous type filter based on a transconductor and a high speed parasitic free active integrator, allowing complete independence of the filter response from interconnect parasitics, thus realizing a family of frequency response curves optimized for disk drive read channel equalization. It consists of a programmable 6-pole 2-zero lowpass filter stage, two pairs of high-speed drivers, and a serial microprocessor interface. The poles of the transfer function approximate a maximally flat group delay (Bessel) response, whereas the symmetric zeros provide the high-frequency boost necessary for pulse slimming. The cutoff frequency range is determined by Rext, which is inversely proportional to the frequency. The user can independently adjust both the corner frequency, as well as the slimming level. The desired frequency response is programmed by a 14-bit serial input data stream which includes one bit for power-down, one bit for read/write control, and one bit for auto-zero control. The auto-zero circuitry, if enabled, reduces the output offsets to less than 20mV. External control for disabling the slimmer during servo sections is also provided. The ML6025 is well suited for constant density recording systems (Zoned-bit recording) as well as for constant data rate systems. A 36Mbits/s version, ML6026 is also available.

FEATURES

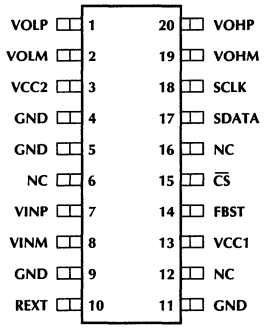
- 6-pole, 2-zero continuous time filter with < -45dB harmonic distortion
- Disk Data rates up to 24Mbit/s
- Programmable filter cutoff frequency
  (4.3:1 range in 64 steps)
  (f_C = 3.13 to 13.5MHz)
- 32 step programmable pulse slimming equalization, 0 to 10dB boost at f_C.
- Power-down, Auto-zero, R/W modes programmable through bits in the Control Register
- Lowpass output and Differentiated Lowpass (Bandpass) output provided.
- Fully I/O balanced architecture with TTL/CMOS compatible interface
- High speed (upto 25MHz clock) three wire serial microprocessor interface
- Double buffered data latch for synchronous or asynchronous data loading.
- Single 5V ± 10% power supply
- 0°C – 70°C operating temperature
- Available in 20-pin SSOP package.
- 4 GHz/1.5µ BiCMOS process
- Power Dissipation — P_{opr} = 300mW, P_{dn} = 7.5mW
- Evaluation board available (ML602XEVAL)

BLOCK DIAGRAM



PIN CONNECTION

20-Pin SSOP



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1 2	VOLP VOLM	Normal Lowpass outputs
3	VCC2	Positive supply for the output drivers, 5V ± 10%
4, 5, 9, 11	GND	Ground
7 8	VINP VINM	Signal Inputs
10	REXT	A 10K resistor between this pin and ground sets the filters corner frequency
13	VCC1	Positive supply, 5V ± 10%
14	FBST	**Slimmer Enable** pin. A high input level allows normal operation of the filter. A low level input disables the slimmer, resulting in 0dB boost. A TTL input.
15	$\overline{CS}$	**Control Register Enable**. A logical low level allows the SCLK input to clock data into the control register via the SDATA input line. A logical high level latches the control register contents and issues the information to the appropriate circuitry. A TTL input.
17	SDATA	**Control Register Data**. A TTL input
18	SCLK	**Control Register Clock**. Negative edge triggerred control register clock input. A TTL input.
19 20	VOHM VOHP	Differentiated lowpass outputs
6, 12, 16	NC	No Connects, reserved for future use.

TRANSFER FUNCTION

The transfer function is: (modified Bessel)

$$\frac{\left(1-\frac{k_{SL}\times s^2}{Q_2^2\times\omega_{02}^2}\right)}{\left(\frac{s^2}{\omega_{01}^2}+\frac{s}{Q_1\times\omega_{01}}+1\right)\left(\frac{s^2}{\omega_{02}^2}+\frac{s}{Q_2\times\omega_{02}}+1\right)\left(\frac{s^2}{\omega_{03}^2}+\frac{s}{Q_3\times\omega_{03}}+1\right)}$$

Where:
$s = j\omega$
k_{SL} = 0 to 7.75
f_{01} = 1.607
Q_1 = 0.51
f_{02} = 1.908
Q_2 = 1.02
f_{03} = 1.692
Q_3 = 0.611
$\omega_{01} = (2\pi f_C) f_{01}$
$\omega_{02} = (2\pi f_C) f_{02}$
$\omega_{03} = (2\pi f_C) f_{03}$
f_C = corner frequency

ABSOLUTE MAXIMUM RATINGS

VCC1, VCC2 ..... +6.5 volts
VINP, VINM, REXT, $\overline{CS}$, SCLK,
SDATA, R/$\overline{W}$ ..... GND - 0.3V to VCC1 + 0.3V
VOLP, VOLM,
VOHP, VOHM ..... GND - 0.3V to VCC2 + 0.3V
Input Current per pin ..... ± 25 mA
Package Dissipation
at Ta = 25°C (Surface Mount) ..... 1.5 Watts
Junction Temperature ..... +150°C
Storage Temperature ..... -65°C to +150°C

OPERATING CONDITIONS

VCC1 = VCC2 ..... + 5 volts ± 10%
VIN = (VINP-VINM) ..... 1 Vp-p
Rext ..... 10 Kohms
Serial Clock Frequency (SCLK) ..... < 25 MHz
AC Coupling Capacitors ..... > 0.0001 µF

ELECTRICAL CHARACHTERISTICS

The following specifications apply over the recommended operating conditions, unless otherwise stated. Please refer to the application/test setup digram:

VCC1 = VCC2 = 5 volt ± 10%, Ta = 0°C to 70°C, Rext = 10 Kohms
VIN = (VINP - VINM) = 1 Vp-p sinewave input
VOL = (VOLP - VOLM) and VOH = (VOHP - VOHM)
Input and Output coupling capacitors = 0.47µF
RB1 = 750 ohms (pins 1 & 2), RB2 = 750 ohms (pins 19 & 20)
RL = 1000 (1000) ohms and CL = 50 (50) pF on pins 1 (19) and 2 (20)
Serial Clock Frequency = 20 MHz, Power Down, Read/Write bits = 0, Auto Zero = 1
Digital timing measured at 1.4V midpoint
Input control signals from 10% - 90% of VCC1 with ($t_r = t_f$) < 5 ns.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
DC CHARACTERISTICS						
I_{CC}	VCC Supply Current	RB1 = RB2 = INF		60	77	mA
Ipd	Standby Current	VIN = 0		1.5	1.75	mA
DIGITAL INPUT CHARACTERISTICS (SCLK, SDATA, $\overline{CS}$)						
VIL	Low Voltage				0.8	V
VIH	High Voltage		2.2			V
IIH	High Current				1.0	µA
IIL	Low Current				-1.0	µA
CIN	Input Capacitance			5		pF
DIGITAL TIMING CHARACTERISTICS (SCLK, SDATA, $\overline{CS}$)						
t_{PW}-$\overline{CS}$	Width of $\overline{CS}$, High/Low		25			ns
t_{SU}-SDATA	SDATA Setup time to SCLK		15			ns
t_H-SDATA	SDATA Hold Time		5			ns
t_{SU}-$\overline{CS}$	$\overline{CS}$ Setup Time to SCLK		15			ns
t_H-$\overline{CS}$	$\overline{CS}$ Hold Time to SCLK		0			ns
t_{PH}-SCLK	SCLK Pulse Width		20			ns
t_H-SCLK	$\overline{CS}$ Inactive to SCLK Active		125			ns

ELECTRICAL CHARACHTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
EQUALIZER (NORMAL AND LOWPASS OUTPUT)						
AG	Absolute Gain	S0-S4 = 0, F0-F5 = 0 at 0.5MHz	-1.5	-0.5	0.5	dB
CF	Cutoff Frequency, -3dB ±1.5 (f_{ref} = 0.5MHz)	S0-S4 = 0, (no slimming) F5 F4 F3 F2 F1 F0 (f_C)				
		0 0 0 0 0 0	12.15	13.50	14.85	MHz
		0 0 0 0 0 1	11.54	12.82	14.10	MHz
		0 0 0 0 1 0	11.04	12.27	13.50	MHz
		0 0 0 1 0 0	10.13	11.25	12.38	MHz
		0 0 1 0 0 0	8.68	9.64	10.60	MHz
		0 1 0 0 0 0	6.75	7.50	8.25	MHz
		1 0 0 0 0 0	4.67	5.19	5.71	MHz
		1 1 1 1 1 1	2.82	3.13	3.44	MHz
SL	Slimming Level (Gain at CF Referred to AG, Vout = 1Vp-p	F0-F5 = 0; at CF S4 S3 S2 S1 S0				
		0 0 0 0 1	-0.4	0.6	1.6	dB
		0 0 0 1 0	0.1	1.1	2.1	dB
		0 0 1 0 0	1.1	2.1	3.1	dB
		0 1 0 0 0	2.8	3.8	4.8	dB
		1 0 0 0 0	5.4	6.4	7.4	dB
		1 1 1 1 1	8.9	9.9	10.9	dB
GD	Diff Group Delay	$0.3f \le f \le f_C$, F0-F5 = 0, Note 2			±5	%
HD	Harmonic Distortion Second and Third related to Fundamental	F0-F5 = 0, Vout = 1.5Vp-p, Fin = 9.0MHz				
		S0-S4 = 0 (no slimming)			-45	dB
		S0-S4 = 1 (full slimming), Note 1			-40	dB
ICN	Idle Channel Noise (VIN = 0, DC – 78MHz)	F0-F5 = 0, VOLP				
		S0-S4 = 0 (no slimming)			2	mVrms
		S0-S4 = 1 (full slimming), Note 1			6	mVrms
DR	Dynamic Range (Signal/(Noise + Distor)) Signal = 1Vp-p	F0-F5 = 0, Fin = 9.0MHz				
		S0-S4 = 0 (no slimming)			-41	dB
		S0-S4 = 1 (full slimming), Note 1			-35	dB
PSRR	Power Supply Rejection	100mVp-p sinewave on Vcc F0-F5 = 0, S0-S4 = 0, Vin = 0				
		Fin = 1.0MHz		40		dB
		Fin = 40MHz		30		dB
DELP HI	Phase Shift between LP and HP Output	All F's and S's = 0 Vin = 1Vp-p, Fin = 9.0MHz	87.5	90	92.5	Degree
ANALOG						
VIP	Input Signal Monotonicity	All F's and S's = 0, (VINP - VINM) Fin = 9.0MHz		1	2	Vp-p
RID	Differential Input Resistance	VIN = 100mVp-p at 6.7MHz	1.6	2	2.5	Kohms
CID	Differential Input Capacitance	VIN = 100mVp-p at 6.7MHz		5		pF
ZIC	Common-mode Input Impedence			1		Kohms
VOS	Output Offset Voltage	Differential VOLP or VOHP				
		Auto Zero ON (S0-S4 = 0 or 1)			±10	mV
		Auto Zero OFF (S0-S4 = 0)			±400	mV
		Auto Zero OFF (S0-S4 = 1)			±400	mV

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ELECTRICAL CHARACHTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
ANALOG (Continued)						
ROD	Output Resistance	Differential VIN = 0; at 6.7MHz		5		Ohms
COD	Output Capacitance	Differential VIN = 0; at 6.7 MHz		8		pF
ROC	Output Resistance Common Mode	Common mode VIN = 0; at 6.7MHz		5		Ohms
COC	Output Capacitance Common Mode	Common mode VIN = 0; at 6.7MHz		15		pF
CLSE	Load Capacitance	VOLP; RB1 = 750 ohms VOHP; RB2 = 750 ohms			50 50	pF pF
RLSE	Load Resistance	VOLP VOHP	400 400			Ohms Ohms
RLOZ	Input Resistance	Diff; PD and/or RW bit = 1			350	Ohms
I_{OB}	Output Buffer Bias Current	VOLP or VOHP, VOLM or VOHM	1	1.4		mA
I_{OSC}	Short Circuit Output Current	VOLP or VOHP, VOLM or VOHM		44	60	mA

Note 1: These parameters are guaranteed by characterization only.
Note 2: Tested only at max f_C setting, however this parameter is guaranteed by characterization over entire range.

FUNCTIONAL DESCRIPTION

INTRODUCTION

Many of the high-frequency continuous-time filters have principally utilized a basic integrator consisting of a transconductance stage driving a passive integrating capacitor. These approaches are susceptible to frequency response variations due to the parasitic capacitances associated with the parasitic-sensitive output nodes of the integrator. This type of transconductance stage also often has low open-circuit voltage gain, resulting in limited practical Q range in the filter. The use of an active parasitic-insensitive integrator, has generally been avoided in these filters because of the additional excess phase that the amplifier contributes.

The ML6025 is a continuous-time filter based on a transconductor and a high-speed parasitic free active integrator, allowing complete independence of the filter response from interconnect parasitics and a very wide range of realizable filter Q. A unique approach to cancelling the excess phase contributed by the hi-speed BiCMOS amplifier allows this filter to achieve reproducible responses at 13.5 MHz filter bandwidth in a 1.5µ/4GHz BiCMOS process. This active integrator incorporates a novel technique for setting the transconductance Gm value as a function of an external precision resistor, independent of temperature, supply, in conjunction with a wafer-sort trim technique to adjust capacitor process tolerances, thus eliminating the need for an on-chip PLL for tuning.

The ML6025 filter consists of a 6th order Bessel low-pass and a 2nd order cosine equalizer stage. It is made up of three biquads with lowpass and bandpass outputs. Both outputs of the last stage are available with matched group-delay characteristics. The corner frequency is digitally programmable to 64 values over a 4 to 1 range, through the serial microprocessor interface. This is accomplished internally by changing the integrating capacitor value. Slimming equalization is done by digitally programming two real-symmetric zeroes, through the serial microprocessor interface. This boosts the high frequency response in 32 steps from 0 to 10 dB. The slimmer can also be instantly disabled through an external pin.

In a typical application, the ML6025 is used together with a pulse detector such as the ML541, ML4041 or the ML8464 , making up a section of the AGC loop. Thus, the output of the AGC amplifier is AC coupled to the ML6025 input and the output of the ML6025 is AC coupled not only to the rectifier input thus closing the AGC loop, but also to the pulse detector input. The ML6025 provides two sets of fully balanced outputs. The lowpass outputs and the differentiated lowpass outputs. The ML6025 input and output common mode voltage biases are generated on-chip. The ML6025 consists of an input common bias circuit, a programmable continuous type equalizer filter with normal and differentiated lowpass outputs, followed by output buffers, and a high speed serial microprocessor interface. The ML6025 processes only differential input signals, common mode inputs are rejected. The output should also be taken differentially in order to obtain the best performance.

INPUT COMMON MODE

The input common mode bias consists of two resistors as shown in the block diagram, and a buffer which biases the center point with a well defined voltage required by the internal circuitry. These resistors are 1000 Ohms each and together with the external coupling capacitor define the lower corner frequency of the transfer function.

EQUALIZER FILTER

The filter transfer function is composed of a second order numerator and a sixth order denominator. The low frequency attenuation is set internally to 0dB. The numerator realizes two zeros symmetrical symmetrical to the imaginary axis, one in the left and the other in the right half plane. The location of the zeros is programmable. This realizes a digitally programmable pulse slimming function in order to overcome intersymbol interference and thus contribute to increasing bit density. The slimming level is controlled by 5 bits in the control register, thus providing 32 different choices between 0 to 10 dB. The denominator approximately realizes a maximally flat group delay (Bessel) function with a digitally programmable corner frequency controlled by 6 bits in the control register, thus providing 64 different cutoff frequencies.

SLIMMING LEVEL

The slimming levels generated by the slimming bits are shown below. There are 5 bits of control, S0 - S4. The typical gain of the equalizer at the cutoff frequency is shown in the table below. The gain at f_C in dB is also given by the formula :

$$\text{Gain (dB)} = 20 \times \text{Log}\,(0.707 \times (1 + 0.06868 \times K))$$

where K = 0, 1, . . . 31

CUTOFF FREQUENCY

There are 6 bits in the control register that controls the position of the cutoff frequency, F0 - F5. The typical values of the cutoff (-3dB) frequency are shown in the table below for the case when S0 - S4=0 (no slimming). There are a total of 64 frequencies available from 13.5MHz down to 3.13MHz. Bits F1 - F5 will select one of 32 frequency settings in a monotonic fashion. Bit F0 is used to shift the whole frequency setting range by 5% lower than each of the 32 settings given by F1 - F5. This offers a scheme to increase the effective resolution of the cutoff frequency programmability. This feature is specially useful in the higher frequency range, where the granularity is coarse.

For example :

By setting F0 = 0,

Cutoff frequency = 13.50 MHz with F5 - F1 = 00000 and

Cutoff frequency = 12.27 MHz with F5 - F1 = 00001, the next consecutive setting.

Frequency delta between consecutive settings = 1.23 MHz or about 9% of 13.50 MHz.

By setting F0 = 1, we can shift the consecutive cutoff frequency settings as follows :

Cutoff frequency = 13.50 MHz with (F5 - F1, F0) = (00000, 0)

Cutoff frequency = 12.82 MHz with (F5 - F1, F0) = (00000, 1) Delta = 0.68 MHz

TABLE 1: TABLE OF SLIMMING LEVEL PROGRAMMING VALUES

S4	S3	S2	S1	S0	K	GAIN AT f_C (dB)	STEPS (dB)
0	0	0	0	0	0	- 3.0	
0	0	0	0	1	1	- 2.4	0.6
0	0	0	1	0	2	- 1.9	0.5
0	0	0	1	1	3	- 1.4	0.5
0	0	1	0	0	4	- 0.9	0.5
0	0	1	0	1	5	- 0.4	0.5
0	0	1	1	0	6	- 0.0	0.4
0	0	1	1	1	7	0.4	0.4
0	1	0	0	0	8	0.8	0.4
0	1	0	0	1	9	1.2	0.4
0	1	0	1	0	10	1.5	0.3
0	1	0	1	1	11	1.9	0.4
0	1	1	0	0	12	2.2	0.3
0	1	1	0	1	13	2.5	0.3
0	1	1	1	0	14	2.8	0.3
0	1	1	1	1	15	3.1	0.3
1	0	0	0	0	16	3.4	0.3
1	0	0	0	1	17	3.7	0.3
1	0	0	1	0	18	4.0	0.3
1	0	0	1	1	19	4.2	0.2
1	0	1	0	0	20	4.5	0.3
1	0	1	0	1	21	4.7	0.2
1	0	1	1	0	22	5.0	0.3
1	0	1	1	1	23	5.2	0.2
1	1	0	0	0	24	5.4	0.2
1	1	0	0	1	25	5.7	0.3
1	1	0	1	0	26	5.9	0.2
1	1	0	1	1	27	6.1	0.2
1	1	1	0	0	28	6.3	0.2
1	1	1	0	1	29	6.5	0.2
1	1	1	1	0	30	6.7	0.2
1	1	1	1	1	31	6.9	0.2

Cutoff frequency = 12.27 MHz with (F5 - F1, F0) = (00001, 0) Delta = 0.55 MHz

Hence frequency delta between consecutive settings is lower, thus higher resolution.

In the table 2 below, the cutoff frequencies are shown as two columns depending on the F0 bit being zero or one. The monotonicity is guaranteed within the individual frequency columns, however because of the limitations of the 5% frequency circuitry, the monotonicity between the two columns cannot be guaranteed. This is especially significant at the lower end of the frequency range, where the difference in frequencies between the two column settings becomes very close (< 1%). Further tuning of the cutoff frequency down to the 1 to 10% range can be

achieved by modifying the value of the external resistor from its ideal 10 Kohms value by 1 to 10%, which shifts the whole response. Larger changes are not recommended for proper operation of the filter. The corner frequency is given by the formula outlined below :

$$f_C = \left(\frac{13.5 \times (1 - F0 \times 0.05)}{[1 + 0.1 \times INT(N/2)]} \times \frac{10Kohms}{Rext} \right) MHz$$

OUTPUT BUFFER

The output buffer is the final stage of the ML6025 for both the normal and differentiated outputs. This is a fully differential buffer with unity gain. Only 1.4 mA of sinking current is provided on chip. More drive can be obtained by connecting external resistors to ground. The common mode output voltage is typically 2V.

SERIAL MICROPROCESSOR INTERFACE

The serial microprocessor interface consists of a simple three-wire serial port. It consists of a fourteen bit serial shift register with a double bufferred latch for synchronous and asynchronous loading. A timing diagram and the control word definition are shown below. The 14-bit data word present on the SDATA line is serially shifted into the register on falling edges of the serial shift clock, SCLK, provided the $\overline{CS}$ pin is active (logical zero). F0 should be shifted in first, and F13 (the power-down bit) shifted in last as shown below. When the $\overline{CS}$ pin is inactive (logical one), SDATA and SCLK are ignored, and the previously shifted information is latched at the rising edge of $\overline{CS}$ becoming inactive (logical one). It is reccommended that the SCLK input be kept inactive low till such time when it is in use. The SCLK input can run upto speeds of 25 MHz. The Autozero function, if enabled, minimizes the offsets at the filter outputs to 20mV.

TABLE 2: TABLE OF CUTOFF FREQUENCY PROGRAMMING VALUES IN MHZ

F5	F4	F3	F2	F1	N	f_C with F0 = 0	N	f_C with F0 = 1
0	0	0	0	0	0	13.5		
0	0	0	0	0			1	12.82
0	0	0	0	1	2	12.27		
0	0	0	0	1			3	11.66
0	0	0	1	0	4	11.25		
0	0	0	1	0			5	10.69
0	0	0	1	1	6	10.38		
0	0	0	1	1			7	9.87
0	0	1	0	0	8	9.64		
0	0	1	0	0			9	9.16
0	0	1	0	1	10	9.0		
0	0	1	0	1			11	8.55
0	0	1	1	0	12	8.44		
0	0	1	1	0			13	8.02
0	0	1	1	1	14	7.94		
0	0	1	1	1			15	7.54
0	1	0	0	0	16	7.50		
0	1	0	0	0			17	7.13
0	1	0	0	1	18	7.11		
0	1	0	0	1			19	6.75
0	1	0	1	0	20	6.75		
0	1	0	1	1	22	6.43		
0	1	0	1	0			21	6.41
0	1	1	0	0	24	6.14		
0	1	0	1	1			23	6.11
0	1	1	0	1	26	5.87		
0	1	1	0	0			25	5.83
0	1	1	1	0	28	5.63		
0	1	1	0	1			27	5.58
0	1	1	1	1	30	5.40		
0	1	1	1	0			29	5.34
1	0	0	0	0	32	5.19		
0	1	1	1	1			31	5.13
1	0	0	0	1	34	5.00		
1	0	0	0	0			33	4.93
1	0	0	1	0	36	4.82		
1	0	0	0	1			35	4.75
1	0	0	1	1	38	4.66		
1	0	0	1	0			37	4.58
1	0	1	0	0	40	4.50		
1	0	0	1	1			39	4.42
1	0	1	0	1	42	4.35		
1	0	1	0	0			41	4.28
1	0	1	1	0	44	4.22		
1	0	1	0	1			43	4.14
1	0	1	1	1	46	4.09		
1	0	1	1	0			45	4.01
1	1	0	0	0	48	3.97		
1	0	1	1	1			47	3.89
1	1	0	0	1	50	3.86		
1	1	0	0	0			49	3.77
1	1	0	1	0	52	3.75		
1	1	0	0	1			51	3.66
1	1	0	1	1	54	3.65		
1	1	0	1	0			53	3.56
1	1	1	0	0	56	3.55		
1	1	1	0	0			55	3.47
1	1	1	0	1	58	3.46		
1	1	1	0	0			57	3.38
1	1	1	1	0	60	3.38		
1	1	1	0	1			59	3.29
1	1	1	1	1	62	3.29		
1	1	1	1	0			61	3.21
1	1	1	1	1			63	3.13

Note: N is the decimal value of the cutoff frequency bits (F5 - F0), in the control register

TIMING DIAGRAM

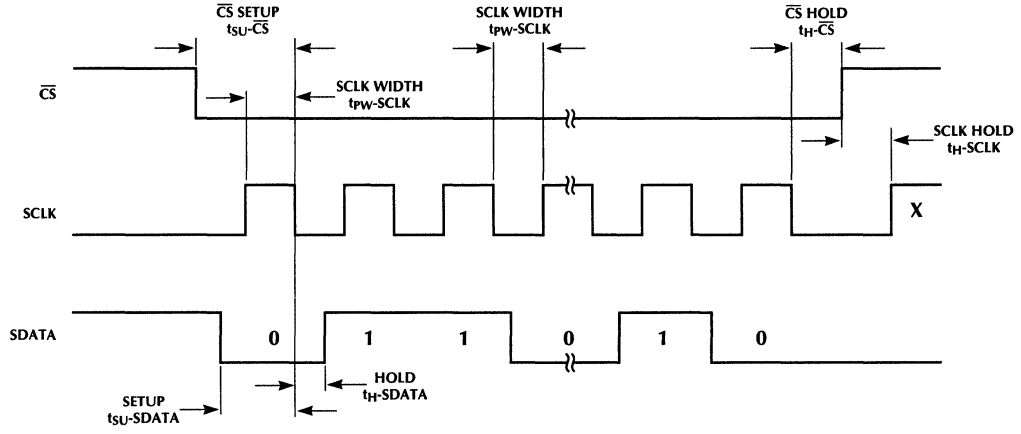


Figure 1.

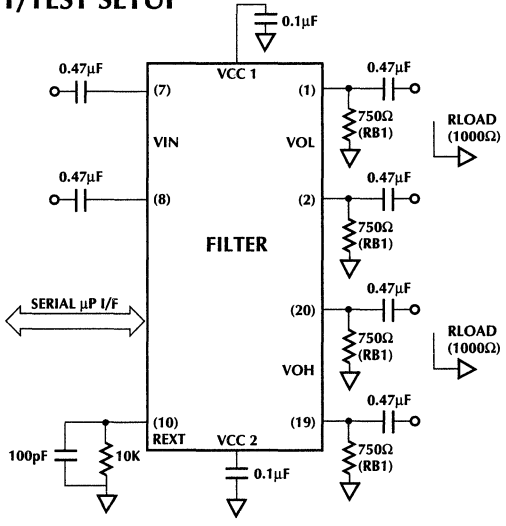
CONTROL REGISTER DEFINITION

F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
AZ	PD	R/W	SLIMMING CONTROL					FREQUENCY CONTROL					

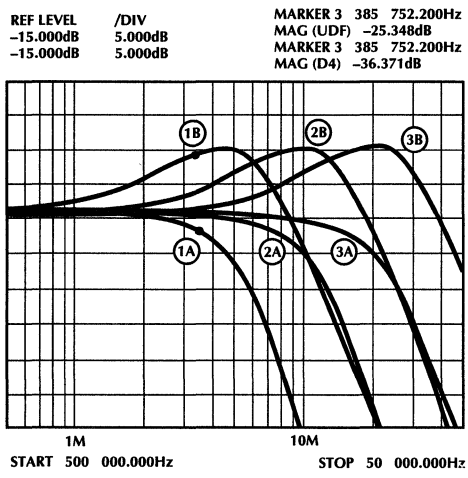
AZ	AutoZero	1 = Autozero circuitry activated 0 = Autozero circuitry inactive
PD	Power Down	1 = Chip is in power down mode 0 = Chip is fully powered up
R/W	Read/Write	1 = Write data mode 0 = Read data mode

5

APPLICATIONS CIRCUIT/TEST SETUP

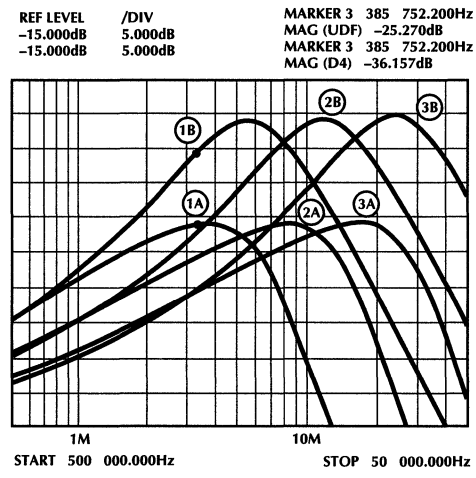


Note: Decoupling capacitors need to be very close to the chip, to prevent oscillations.



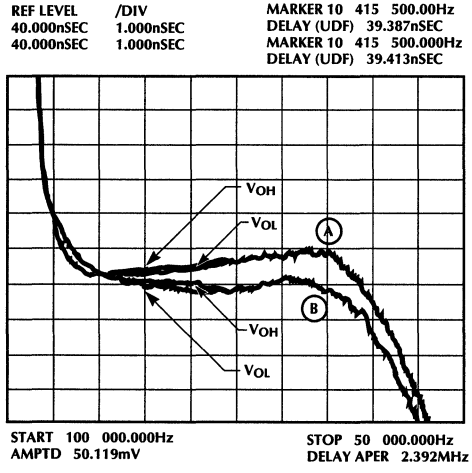
Filter Response (Lowpass Output)

Shown are the ML6025 filter response at three different cutoff frequency (f_c) settings. Setting 1 = 3.13 MHz, 2 = 6.75 MHz and 3 = 13.5 MHz. At each of the f_c settings, the filter response is shown with no slimming (A) and with full slimming (B) activated.



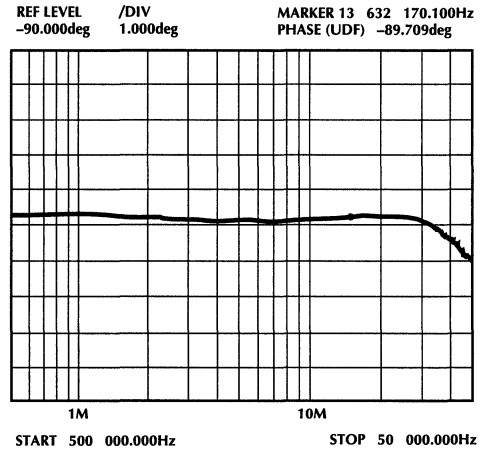
Filter Response (Bandpass Output)

Shown are the ML6025 filter response at three different cutoff frequency (f_c) settings. Setting 1 = 3.13 MHz, 2 = 6.75 MHz and 3 = 13.5 MHz. At each of the f_c settings, the filter response is shown with no slimming (A) and with full slimming (B) activated.



ML6025 Filter/Equalizer group Delay Tracking

Shown are the curves to demonstrate group delay tracking between the lowpass (V_{OL}) and bandpass (V_{OH}) outputs, at an f_c of 13.5 MHz, with no slimming activated (A) and full slimming activated (B). It can be seen that the group delay tracking between the lowpass and bandpass outputs is well within 1 ns.



Phase Difference between Lowpass and Bandpass Outputs

Shown is the delta in the phase between the lowpass and bandpass outputs. Ideally the bandpass output should be -90°. The curve shows that this is within 1° for a frequency range of 50 MHz to 10 MHz.

ML6025 FILTER/EQUALIZER CHARACTERISTICS

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6025CR	0°C to +70°C	20-Pin SSOP (R20)

ML6026

36 Mbps Read Channel Filter/Equalizer

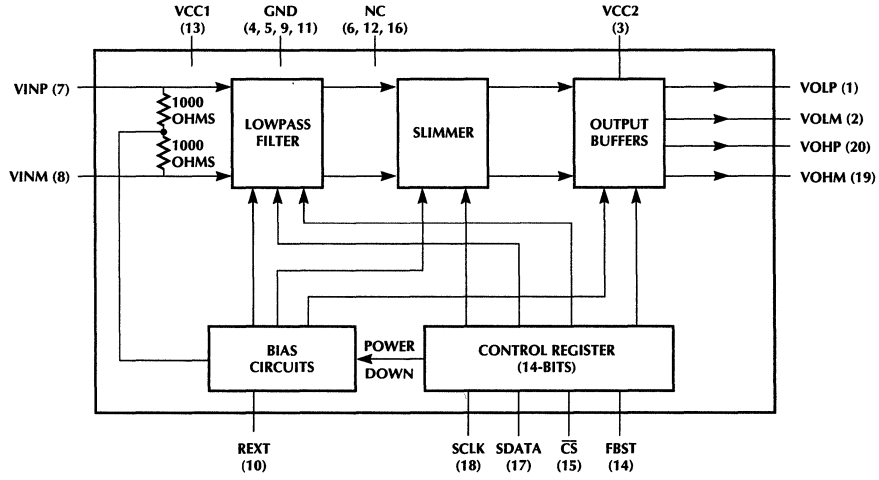
GENERAL DESCRIPTION

The ML6026 is a monolithic analog filter/equalizer intended for hard disk drive read channel applications, capable of handling disk data rates upto 36Mbits/s, with an operating power dissipation of less than 350mW. Its architecture consists of a continuous type filter based on a transconductor and a high speed parasitic free active integrator, allowing complete independence of the filter response from interconnect parasitics, thus realizing a family of frequency response curves optimized for disk drive read channel equalization. It consists of a programmable 6-pole 2-zero lowpass filter stage, two pairs of high-speed drivers, and a serial microprocessor interface. The poles of the transfer function approximate a maximally flat group delay (Bessel) response, whereas the symmetric zeros provide the high-frequency boost necessary for pulse slimming. The cutoff frequency range is determined by Rext, which is inversely proportional to the frequency. The user can independently adjust both the corner frequency, as well as the slimming level. The desired frequency response is programmed by a 14-bit serial input data stream which includes one bit for power-down, one bit for read/write control, and one bit for auto-zero control. External control for disabling the slimmer during servo sections is also provided. The ML6026 is well suited for constant density recording systems (Zoned-bit recording) as well as for constant data rate systems. A 24 Mbits/s version, ML6025 is also available.

FEATURES

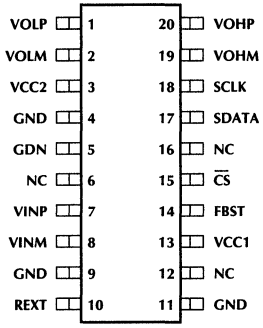
- 6-pole, 2-zero continuous time filter with < -45dB harmonic distortion
- Disk Data rates up to 36 Mbit/s
- Programmable filter cutoff frequency
  (4.3:1 range in 64 steps)
  (f_C = 4.69 to 20.25 MHz)
- 32 step programmable pulse slimming equalization, 0 to 10dB boost at f_C.
- Power-down, Auto-zero, R/W modes programmable through bits in the Control Register
- Lowpass output and Differentiated Lowpass (Bandpass) output provided.
- Fully I/O balanced architecture with TTL/CMOS compatible interface
- High speed (upto 25MHz clock) three wire serial microprocessor interface
- Double buffered data latch for synchronous or asynchronous data loading.
- Single 5V ± 10% power supply
- 0°C – 70°C operating temperature
- Available in 20-pin SSOP package.
- 4 GHz/1.5µ BiCMOS process
- Power Dissipation: P_{opr} = 350mW, P_{dn} = 7.5mW
- Evaluation board available (ML602XEVAL)

BLOCK DIAGRAM



PIN CONNECTION

20-Pin SSOP



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1 2	VOLP VOLM	Normal Lowpass outputs
3	VCC2	Positive supply for the output drivers, 5V ± 10%
4, 5, 9, 11	GND	Ground
7 8	VINP VINM	Signal Inputs
10	REXT	A 10K resistor between this pin and ground sets the filters corner frequency
13	VCC1	Positive supply, 5V ± 10%
14	FBST	**Slimmer Enable** pin. A high input level allows normal operation of the filter. A low level input disables the slimmer, resulting in 0dB boost. A TTL input
15	$\overline{CS}$	**Control Register Enable**. A logical low level allows the SCLK input to clock data into the control register via the SDATA input line. A logical high level latches the control register contents and issues the information to the appropriate circuitry. A TTL input.
17	SDATA	**Control Register Data**. A TTL input
18	SCLK	**Control Register Clock**. Negative edge triggerred control register clock input. A TTL input.
19 20	VOHM VOHP	Differentiated lowpass outputs
6, 12, 16	NC	No Connects, reserved for future use.

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TRANSFER FUNCTION

The transfer function is: (modified Bessel)

$$\frac{\left(1-\frac{k_{SL}\times s^2}{Q_2^2\times\omega_{02}^2}\right)}{\left(\frac{s^2}{\omega_{01}^2}+\frac{s}{Q_1\times\omega_{01}}+1\right)\left(\frac{s^2}{\omega_{02}^2}+\frac{s}{Q_2\times\omega_{02}}+1\right)\left(\frac{s^2}{\omega_{03}^2}+\frac{s}{Q_3\times\omega_{03}}+1\right)}$$

Where: $s = j\omega$
k_{SL} = 0 to 7.75
f_{01} = 1.607
Q_1 = 0.51
f_{02} = 1.908
Q_2 = 1.02
f_{03} = 1.692
Q_3 = 0.611
$\omega_{01} = (2\pi f_C) * f_{01}$
$\omega_{02} = (2\pi f_C) f_{02}$
$\omega_{03} = (2\pi f_C) f_{03}$
f_C = corner frequency

ABSOLUTE MAXIMUM RATINGS

VCC1, VCC2 ..... +6.5 volts
VINP, VINM, REXT, $\overline{CS}$, SCLK,
SDATA, R/$\overline{W}$ ..... GND - 0.3V to VCC1 + 0.3V
VOLP, VOLM,
VOHP, VOHM ..... GND - 0.3V to VCC2 + 0.3V
Input Current per pin ..... ± 25 mA
Package Dissipation
at Ta = 25°C (Surface Mount) ..... 1.5 Watts
Junction Temperature ..... +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... 260°C

OPERATING CONDITIONS

VCC1 = VCC2 ..... + 5 volts ± 10%
VIN = (VINP-VINM) ..... 1 Vp-p
Rext ..... 10 Kohms
Serial Clock Frequency (SCLK) ..... < 25 MHz
AC Coupling Capacitors ..... > 0.0001 µF

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions, unless otherwise stated. Please refer to the application/test setup digram:

VCC1 = VCC2 = 5 volt ± 10%, T_a = 0°C to 70°C, Rext = 10 Kohms
VIN = (VINP - VINM) = 1 Vp-p sinewave input
VOL = (VOLP - VOLM) and VOH = (VOHP - VOHM)
Input and Output coupling capacitors = 0.47 µF
RB1 = 750 ohms (pins 1 & 2), RB2 = 750 ohms (pins 19 & 20)
RL = 1000 (1000) ohms and CL = 50 (50) pF on pins 1 (19) and 2 (20)
Serial Clock Frequency = 20 MHz, Power Down, Read/Write bits = 0, Auto Zero = 1
Digital timing measured at 1.4V midpoint
Input control signals from 10% - 90% of VCC1 with ($t_r = t_f$) < 5 ns.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
DC CHARACTERISTICS						
I_{CC}	VCC Supply Current	RB1 = RB2 = INF		70	87	mA
Ipd	Standby Current	VIN = 0		1.5	1.75	mA
DIGITAL INPUT CHARACTERISTICS (SCLK, SDATA, $\overline{CS}$)						
VIL	Low Voltage				0.8	V
VIH	High Voltage		2.2			V
IIH	High Current				1.0	µA
IIL	Low Current				-1.0	µA
CIN	Input Capacitance			5		pF
DIGITAL TIMING CHARACTERISTICS (SCLK, SDATA, $\overline{CS}$)						
t_{PW}-$\overline{CS}$	Width of $\overline{CS}$, High/Low		25			ns
t_{SU}-SDATA	SDATA Setup time to SCLK		15			ns
t_H-SDATA	SDATA Hold Time		5			ns
t_{SU}-$\overline{CS}$	$\overline{CS}$ Setup Time to SCLK		15			ns
t_H-$\overline{CS}$	$\overline{CS}$ Hold Time to SCLK		0			ns
t_{PH}-SCLK	SCLK Pulse Width		20			ns
t_H-SCLK	$\overline{CS}$ Inactive to SCLK Active		125			ns

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
EQUALIZER (NORMAL AND LOWPASS OUTPUT)						
AG	Absolute Gain	S0-S4 = 0, F0-F5 = 0 at 0.5MHz	-1.5	-0.5	0.5	dB
CF	Cutoff Frequency, -3dB ±1.5 (f_{ref} = 0.5MHz)	S0-S4 = 0, (no slimming) F5 F4 F3 F2 F1 F0 (f_C)				
		0 0 0 0 0 0	18.23	20.25	22.28	MHz
		0 0 0 0 0 1	17.32	19.24	21.16	MHz
		0 0 0 0 1 0	16.57	18.41	20.25	MHz
		0 0 0 1 0 0	15.19	16.88	18.57	MHz
		0 0 1 0 0 0	13.01	14.46	15.91	MHz
		0 1 0 0 0 0	10.13	11.25	12.38	MHz
		1 0 0 0 0 0	7.01	7.79	8.57	MHz
		1 1 1 1 1 1	4.22	4.69	5.16	MHz
SL	Slimming Level (Gain at CF Referred to AG, Vout = 1Vp-p	F0-F5 = 0; at CF S4 S3 S2 S1 S0				
		0 0 0 0 1	0.4	0.6	1.6	dB
		0 0 0 1 0	0.1	1.1	2.1	dB
		0 0 1 0 0	1.1	2.1	3.1	dB
		0 1 0 0 0	2.8	3.8	4.8	dB
		1 0 0 0 0	5.4	6.4	7.4	dB
		1 1 1 1 1	8.9	9.9	10.9	dB
GD	Diff Group Delay	$0.3f_C \le f \le f_C$, F0-F5 = 0, Note 2			±5	%
HD	Harmonic Distortion Second and Third related to Fundamental	F0-F5 = 0, Vout = 1.5Vp-p, Fin = 13.5MHz S0-S4 = 0 (no slimming) S0-S4 = 1 (full slimming), Note 1			 -45 -40	 dB dB
ICN	Idle Channel Noise (VIN = 0, DC – 78MHz)	F0-F5 = 0, VOLP S0-S4 = 0 (no slimming) S0-S4 = 1 (full slimming), Note 1			 2 6	 mVrms mVrms
DR	Dynamic Range (Signal/(Noise + Distor)) (Signal = 1Vp-p)	F0-F5 = 0, Fin = 13.5MHz S0-S4 = 0 (no slimming) S0-S4 = 1 (full slimming), Note 1			 -41 -35	 dB dB
PSRR	Power Supply Rejection	100mVp-p sinewave on Vcc F0-F5 = 0, S0-S4 = 0, Vin = 0 Fin = 1.0MHz Fin = 40MHz		 40 30		 dB dB
DELP HI	Phase Shift between LP and HP Output	All F's and S's = 0 Vin = 1Vp-p, Fin = 13.5MHz	87.5	90	92.5	Degree
ANALOG						
VIP	Input Signal Monotonicity	All F's and S's = 0, (VINP - VINM) Fin = 13.5MHz		 1	 2	 Vp-p
RID	Differential Input Resistance	VIN = 100mVp-p at 10MHz	1.6	2	2.5	Kohms
CID	Differential Input Capacitance	VIN = 100mVp-p at 10MHz		5		pF
ZIC	Common-mode Input Impedence			1		Kohms
VOS	Output Offset Voltage	Differential VOLP or VOHP Auto Zero ON (S0-S4 = 0 or 1) Auto Zero OFF (S0-S4 = 0) Auto Zero OFF (S0-S4 = 1)			 ±10 ±500 ±500	 mV mV mV

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ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
ANALOG (Continued)						
ROD	Output Resistance	Differential VIN = 0; at 10MHz		5		Ohms
COD	Output Capacitance	Differential VIN = 0; at 10 MHz		8		pF
ROC	Output Resistance Common Mode	Common mode VIN = 0; at 10MHz		5		Ohms
COC	Output Capacitance Common Mode	Common mode VIN = 0; at 10MHz		15		pF
CLSE	Load Capacitance	VOLP; RB1 = 750 ohms VOHP; RB2 = 750 ohms			50 50	pF pF
RLSE	Load Resistance	VOLP VOHP	400 400			Ohms Ohms
RLOZ	Input Resistance	Diff; PD and/or RW bit = 1			350	Ohms
I_{OB}	Output Buffer Bias Current	VOLP or VOHP, VOLM or VOHM	1	1.4		mA
I_{OSC}	Short Circuit Output Current	VOLP or VOHP, VOLM or VOHM		44	60	mA

Note 1: These parameters are guaranteed by characterization only.
Note 2: Tested only at max f_C setting, however this parameter is guaranteed by characterization over the entire range

FUNCTIONAL DESCRIPTION

INTRODUCTION

Many of the high-frequency continuous-time filters have principally utilized a basic integrator consisting of a transconductance stage driving a passive integrating capacitor. These approaches are susceptible to frequency response variations due to the parasitic capacitances associated with the parasitic-sensitive output nodes of the integrator. This type of transconductance stage also often has low open-circuit voltage gain, resulting in limited practical Q range in the filter. The use of an active parasitic-insensitive integrator, has generally been avoided in these filters because of the additional excess phase that the amplifier contributes.

The ML6026 is a continuous-time filter based on a transconductor and a high-speed parasitic free active integrator, allowing complete independence of the filter response from interconnect parasitics and a very wide range of realizable filter Q. A unique approach to cancelling the excess phase contributed by the hi-speed BiCMOS amplifier allows this filter to achieve reproducible responses at 20 MHz filter bandwidth in a 1.5µ/4GHz BiCMOS process. This active integrator incorporates a novel technique for setting the transconductance Gm value as a function of an external precision resistor, independent of temperature, supply, in conjunction with a wafer-sort trim technique to adjust capacitor process tolerances, thus eliminating the need for an on-chip PLL for tuning.

The ML6026 filter consists of a 6th order Bessel low-pass and a 2nd order cosine equalizer stage. It is made up of three biquads with lowpass and bandpass outputs. Both outputs of the last stage are available with matched group-delay characteristics. The corner frequency is digitally programmable to 64 values over a 4 to 1 range, through the serial microprocessor interface. This is accomplished internally by changing the integrating capacitor value. Slimming equalization is done by digitally programming two real-symmetric zeroes, through the serial microprocessor interface. This boosts the high frequency response in 32 steps from 0 to 10 dB. The slimmer can also be instantly disabled through an external pin.

In a typical application, the ML6026 is used together with a pulse detector such as the ML541, ML4041 or the ML8464 , making up a section of the AGC loop. Thus, the output of the AGC amplifier is AC coupled to the ML6026 input and the output of the ML6026 is AC coupled not only to the rectifier input thus closing the AGC loop, but also to the pulse detector input. The ML6026 provides two sets of fully balanced outputs. The lowpass outputs and the differentiated lowpass outputs. The ML6026 input and output common mode voltage biases are generated on-chip. The ML6026 consists of an input common bias circuit, a programmable continuous type equalizer filter with normal and differentiated lowpass outputs, followed by output buffers, and a high speed serial microprocessor interface. The ML6026 processes only differential input signals, common mode inputs are rejected. The output should also be taken differentially in order to obtain the best performance.

INPUT COMMON MODE

The input common mode bias consists of two resistors as shown in the block diagram, and a buffer which biases the center point with a well defined voltage required by the internal circuitry. These resistors are 1000 Ohms each and together with the external coupling capacitor define the lower corner frequency of the transfer function.

EQUALIZER FILTER

The filter transfer function is composed of a second order numerator and a sixth order denominator. The low frequency attenuation is set internally to 0dB. The numerator realizes two zeros symmetrical symmetrical to the imaginary axis, one in the left and the other in the right half plane. The location of the zeros is programmable. This realizes a digitally programmable pulse slimming function in order to overcome intersymbol interference and thus contribute to increasing bit density. The slimming level is controlled by 5 bits in the control register, thus providing 32 different choices between 0 to 10 dB. The denominator approximately realizes a maximally flat group delay (Bessel) function with a digitally programmable corner frequency controlled by 6 bits in the control register, thus providing 64 different cutoff frequencies.

SLIMMING LEVEL

The slimming levels generated by the slimming bits are shown below. There are 5 bits of control, S0 - S4. The typical gain of the equalizer at the cutoff frequency is shown in the table below. The gain at f_c in dB is also given by the formula :

$$\text{Gain (dB)} = 20 \times \text{Log}\,(0.707 \times (1 + 0.06868 \times K))$$

where K = 0, 1, . . . 31

CUTOFF FREQUENCY

There are 6 bits in the control register that controls the position of the cutoff frequency, F0 - F5. The typical values of the cutoff (-3dB) frequency are shown in the table below for the case when S0 - S4=0 (no slimming). There are a total of 64 frequencies available from 20.25MHz down to 4.69MHz. Bits F1 - F5 will select one of 32 frequency settings in a monotonic fashion. Bit F0 is used to shift the whole frequency setting range by 5% lower than each of the 32 settings given by F1 - F5. This offers a scheme to increase the effective resolution of the cutoff frequency programmability. This feature is specially useful in the higher frequency range, where the granularity is coarse.

For example :

By setting F0 = 0,

Cutoff frequency = 20.25 MHz with F5 - F1 = 00000 and

Cutoff frequency = 18.41 MHz with F5 - F1 = 00001, the next consecutive setting.

Frequency delta between consecutive settings = 1.84 MHz or about 9% of 20.25 MHz.

By setting F0 = 1, we can shift the consecutive cutoff frequency settings as follows :

Cutoff frequency = 20.25 MHz with (F5 - F1, F0) = (00000, 0)

Cutoff frequency = 19.24 MHz with (F5 - F1, F0) = (00000, 1) Delta = 1.01 MHz

TABLE 1: TABLE OF SLIMMING LEVEL PROGRAMMING VALUES

S4	S3	S2	S1	S0	K	GAIN AT f_C (DB)	STEPS (DB)
0	0	0	0	0	0	- 3.0	
0	0	0	0	1	1	- 2.4	0.6
0	0	0	1	0	2	- 1.9	0.5
0	0	0	1	1	3	- 1.4	0.5
0	0	1	0	0	4	- 0.9	0.5
0	0	1	0	1	5	- 0.4	0.5
0	0	1	1	0	6	- 0.0	0.4
0	0	1	1	1	7	0.4	0.4
0	1	0	0	0	8	0.8	0.4
0	1	0	0	1	9	1.2	0.4
0	1	0	1	0	10	1.5	0.3
0	1	0	1	1	11	1.9	0.4
0	1	1	0	0	12	2.2	0.3
0	1	1	0	1	13	2.5	0.3
0	1	1	1	0	14	2.8	0.3
0	1	1	1	1	15	3.1	0.3
1	0	0	0	0	16	3.4	0.3
1	0	0	0	1	17	3.7	0.3
1	0	0	1	0	18	4.0	0.3
1	0	0	1	1	19	4.2	0.2
1	0	1	0	0	20	4.5	0.3
1	0	1	0	1	21	4.7	0.2
1	0	1	1	0	22	5.0	0.3
1	0	1	1	1	23	5.2	0.2
1	1	0	0	0	24	5.4	0.2
1	1	0	0	1	25	5.7	0.3
1	1	0	1	0	26	5.9	0.2
1	1	0	1	1	27	6.1	0.2
1	1	1	0	0	28	6.3	0.2
1	1	1	0	1	29	6.5	0.2
1	1	1	1	0	30	6.7	0.2
1	1	1	1	1	31	6.9	0.2

Cutoff frequency = 18.41 MHz with (F5 - F1, F0) = (00001, 0) Delta = 0.83 MHz

Hence frequency delta between consecutive settings is lower, thus higher resolution.

In the table 2 below, the cutoff frequencies are shown as two columns depending on the F0 bit being zero or one. The monotonicity is guaranteed within the individual frequency columns, however because of the limitations of the 5% frequency circuitry, the monotonicity between the two columns cannot be guaranteed. This is especially significant at the lower end of the frequency range, where the difference in frequencies between the two column settings becomes very close (< 1%). Further tuning of the cutoff frequency down to the 1 to 10% range can be

achieved by modifying the value of the external resistor from its ideal 10 Kohms value by 1 to 10%, which shifts the whole response. Larger changes are not recommended for proper operation of the filter. The corner frequency is given by the formula outlined below :

$$f_C = \left(\frac{20.25 \times (1 - F0 \times 0.05)}{[1 + 0.1 \times INT(N/2)]} \times \frac{10Kohms}{Rext} \right) MHz$$

OUTPUT BUFFER

The output buffer is the final stage of the ML6026 for both the normal and differentiated outputs. This is a fully differential buffer with unity gain. Only 1.4 mA of sinking current is provided on chip. More drive can be obtained by connecting external resistors to ground. The common mode output voltage is typically 2V.

SERIAL MICROPROCESSOR INTERFACE

The serial microprocessor interface consists of a simple three-wire serial port. It consists of a fourteen bit serial shift register with a double bufferred latch for synchronous and asynchronous loading. A timing diagram and the control word definition are shown below. The 14-bit data word present on the SDATA line is serially shifted into the register on falling edges of the serial shift clock, SCLK, provided the $\overline{CS}$ pin is active (logical zero). F0 should be shifted in first, and F13 (the power-down bit) shifted in last as shown below. When the $\overline{CS}$ pin is inactive (logical one), SDATA and SCLK are ignored, and the previously shifted information is latched at the rising edge of $\overline{CS}$ becoming inactive (logical one). It is reccommended that the SCLK input be kept inactive low till such time when it is in use. The SCLK input can run upto speeds of 25 MHz. The Autozero function, if enabled, minimizes the offsets at the filter outputs to 20mV.

TABLE 2: TABLE OF CUTOFF FREQUENCY PROGRAMMING VALUES IN MHZ

F5	F4	F3	F2	F1	N	f_C with F0 = 0	N	f_C with F0 = 1
0	0	0	0	0	0	20.25		
0	0	0	0	0			1	19.24
0	0	0	0	1	2	18.41		
0	0	0	0	1			3	17.49
0	0	0	1	0	4	16.88		
0	0	0	1	0			5	16.03
0	0	0	1	1	6	15.58		
0	0	0	1	1			7	14.80
0	0	1	0	0	8	14.46		
0	0	1	0	0			9	13.74
0	0	1	0	1	10	13.50		
0	0	1	0	1			11	12.83
0	0	1	1	0	12	12.66		
0	0	1	1	0			13	12.02
0	0	1	1	1	14	11.91		
0	0	1	1	1			15	11.32
0	1	0	0	0	16	11.25		
0	1	0	0	0			17	10.69
0	1	0	0	1	18	10.66		
0	1	0	0	1			19	10.13
0	1	0	1	0	20	10.13		
0	1	0	1	1	22	9.64		
0	1	0	1	0			21	9.62
0	1	1	0	0	24	9.20		
0	1	0	1	1			23	9.16
0	1	1	0	1	26	8.80		
0	1	1	0	0			25	8.74
0	1	1	1	0	28	8.44		
0	1	1	0	1			27	8.36
0	1	1	1	1	30	8.10		
0	1	1	1	0			29	8.02
1	0	0	0	0	32	7.79		

F5	F4	F3	F2	F1	N	f_C with F0 = 0	N	f_C with F0 = 1
0	1	1	1	1			31	7.70
1	0	0	0	1	34	7.50		
1	0	0	0	0			33	7.40
1	0	0	1	0	36	7.23		
1	0	0	0	1			35	7.12
1	0	0	1	1	38	6.98		
1	0	0	1	0			37	6.87
1	0	1	0	0	40	6.75		
1	0	0	1	1			39	6.63
1	0	1	0	1	42	6.53		
1	0	1	0	0			41	6.41
1	0	1	1	0	44	6.33		
1	0	1	0	1			43	6.21
1	0	1	1	1	46	6.14		
1	0	1	1	0			45	6.01
1	1	0	0	0	48	5.96		
1	0	1	1	1			47	5.83
1	1	0	0	1	50	5.79		
1	1	0	0	0			49	5.66
1	1	0	1	0	52	5.63		
1	1	0	0	1			51	5.50
1	1	0	1	1	54	5.47		
1	1	0	1	0			53	5.34
1	1	1	0	0	56	5.33		
1	1	1	0	0			55	5.20
1	1	1	0	1	58	5.19		
1	1	1	0	0			57	5.06
1	1	1	1	0	60	5.06		
1	1	1	0	1			59	4.93
1	1	1	1	1	62	4.94		
1	1	1	1	0			61	4.81
1	1	1	1	1			63	4.69

Note: N is the decimal value of the cutoff frequency bits (F5 - F0), in the control register

TIMING DIAGRAM

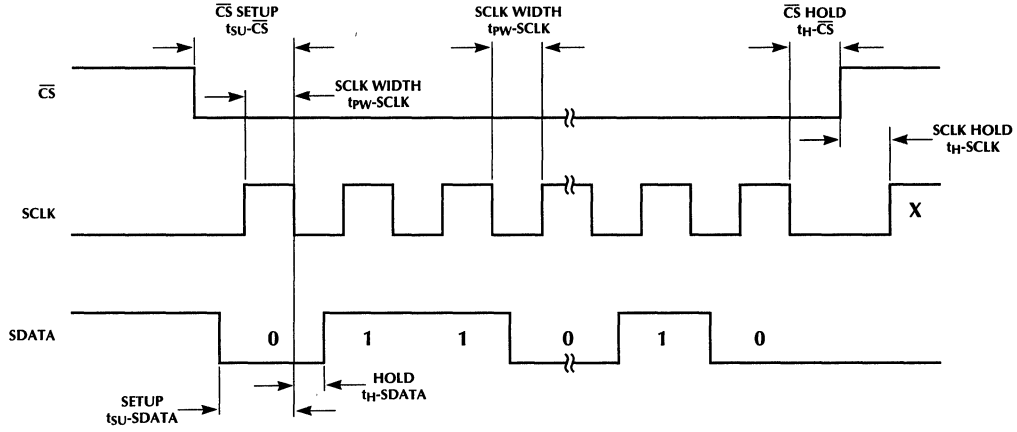


Figure 1.

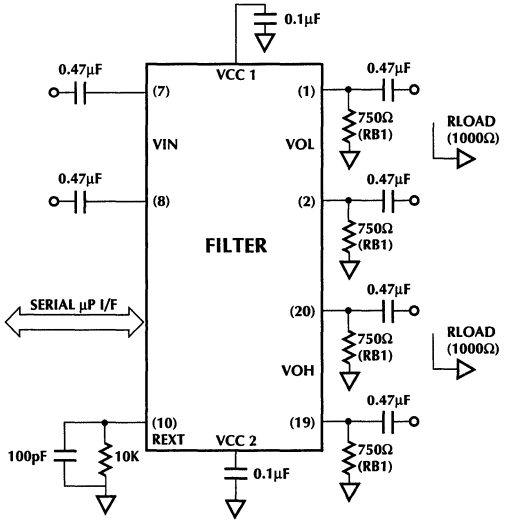
CONTROL REGISTER DEFINITION

F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
AZ	PD	RW	SLIMMING CONTROL					FREQUENCY CONTROL					

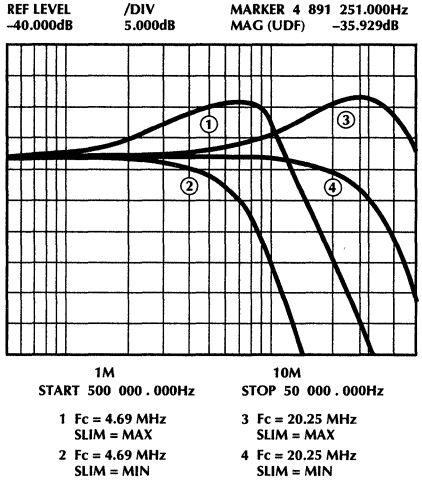
AZ	AutoZero	1 = Autozero circuitry activated 0 = Autozero circuitry inactive
PD	Power Down	1 = Chip is in power down mode 0 = Chip is fully powered up
$\overline{RW}$	Read/Write	1 = Write data mode 0 = Read data mode

5

APPLICATIONS

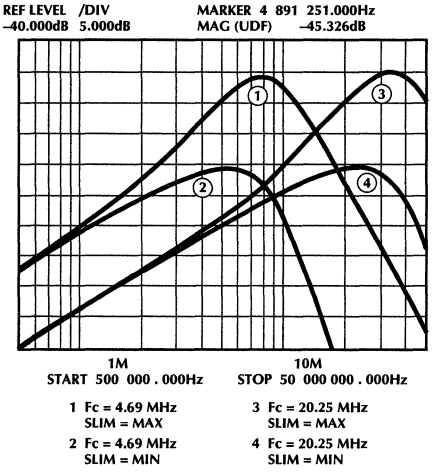


Note: Decoupling capacitors need to be very close th the chip to prevent any oscillations.



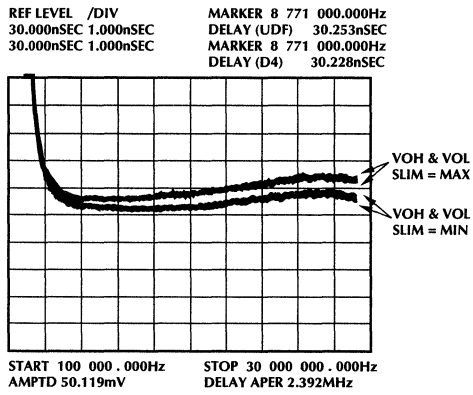
Filter Response (Lowpass Output)

Shown are the ML6026 filter response at the two extreme cutoff frequency (f_C) settings. At each of the f_C settings, the filter response is shown with no slimming and with full slimming activated.



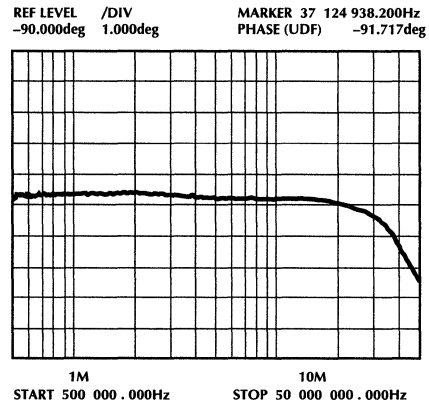
Filter Response (Bandpass Output)

Shown are the ML6026 filter characteristic curves for the bandpass output, with no slimming and full slimming activated.



ML6026 Filter/Equalizer Group Delay Tracking

Shown are the curves to demonstrate group delay tracking between the lowpass (V_{OL}) and bandpass (V_{OH}) outputs, with no slimming activated (min) and full slimming activated (max). It can be seen that the group delay tracking between the lowpass and bandpass outputs is well within 1 ns.



Phase Difference between Lowpass and Bandpass Outputs

Shown is the delta in the phase between the lowpass and bandpass outputs. Ideally the bandpass output should be -90°. The curve shows that this is within 1° for a frequency range of 50 MHz to 10 MHz.

ML6026 FILTER/EQUALIZER CHARACTERISTICS

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6026CR	0°C to +70°C	20-Pin SSOP (R20)

ML6035

5V Spindle Motor Controller and Driver

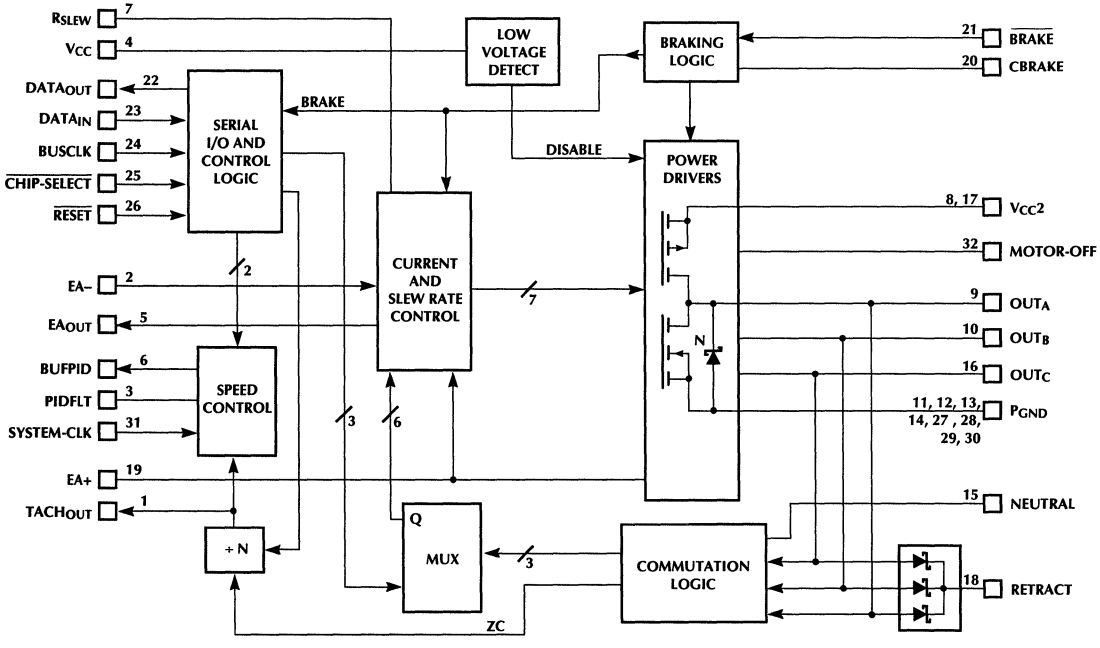
GENERAL DESCRIPTION

The ML6035 is a 5 volt brushless motor controller and driver. The circuit provides three phase sensorless commutation and speed control. A digital commutation circuit including digital delay with adjustable phase advance is included. The circuit also has three 1A complementary output drivers each with a typical on resistance of one half ohm (or one ohm total). An additional P-channel power device is provided to pull up the motor neutral for unipolar operation. Bipolar or unipolar start with either bipolar run or unipolar run is supported with mode switching. A serial bus is provided to minimize the use of dedicated pins and to provide for more command functions. Both internal speed control and external speed control (from sector data) are supported. Sensorless commutation is provided using back EMF zero crossing information. The chip has been designed for maximum flexibility to permit custom start and run algorithms to be used.

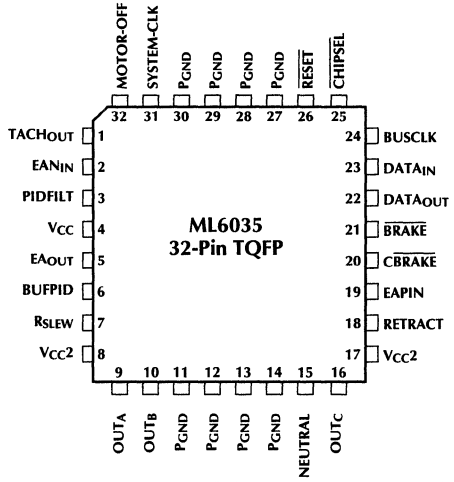
FEATURES

- Power drivers on chip (1A max at 1 ohm)
- V_{CC} decoupling diode not required
- Unipolar and bipolar operation supported
- Digital speed control loop on chip with external PID filter or supports sector data speed control
- Digital commutation circuit including digital delay with adjustable phase advance
- Serial bus for loading necessary motor information, phase advance desired, motor speed, etc.
- Supplies retract voltage with on-chip schottky diodes
- Serial interface compatible with 3V logic
- Supplies tach output
- Sleep mode (I_{CC} = 100µA max)
- Brake pin with adjustable delay to permit back EMF to be used for retract. Brake also accessible from the serial bus
- Output slope or slew rate control to minimize flyback pulses
- Able to recover from momentary power interruptions without stopping the motor for a complete restart

BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	$TACH_{OUT}$	Tach output signal. This pin generates an indication of motor speed. Control bit D3P can be programmed for tach-out = 1 pulse per rev. (divide by N active) or raw zero crossing (divide by N in-active)
2	EAN_{IN}	Error amplifier inverting input
3	PIDFILT	This dual purpose pin is used either for an external PID filter for the internal charge pump speed control circuit or if the charge pump is disabled by serial bus command it is used as an input for sector data.
4	V_{CC}	Main supply pin V = 5V nominal
5	EA_{OUT}	Independent output from the error amplifier
6	BUFPID	Output of the PID buffer amplifier
7	R_{SLEW}	Slew Adjust Resistor
8	$V_{CC}2$	Power V_{CC}
9	OUT_A	Output to drive motor phase A
10	OUT_B	Output to drive motor phase B
11,12 13,14	P_{GND}	Main ground and thermal heat conductor
15	Neutral	In a delta wound motor this pin forms a phantom neutral for the zero crossing comparators. In a Y wound motor the neutral from the motor is connected here.
16	OUT_C	Output to drive motor phase C
17	$V_{CC}2$	Power V_{CC}
18	RETRACT	This pin supplies the raw rectified back-emf voltage from the motor (as it spins down) to retract the heads in a disk drive.
19	EAPIN	Error amp non-inverting input
20	CBRAKE	A capacitor on this pin stores the energy required by the chip to actuate the gates of the output devices and brake the motor during a power fail condition
21	$\overline{BRAKE}$	This pin is normally at 5V. At V_{TH} = 1.2V braking will occur.
22	DATAOUT	Serial data output. $V_{OH} = 2.9 \pm 0.3V$
23	DATAIN	Serial data input. $V_{TH} = 1.4V$
24	BUSCLK	Serial bus clock. F < 20MHz
25	$\overline{CHIPSEL}$	Chip select. A logical low level allows the Bus-Clk to clock data into the shift registers via data-in input; falling edge latches commutation states for read out
26	$\overline{RESET}$	Reset. A logic low level on the reset will set the control registers to zero and force the part into sleep mode
27,28 29,30	P_{GND}	Main ground and thermal heat sink
31	SYSTEM-CLK	System clock. A square wave clock at 2MHz is suggested. An internal prescaler is used to normalize the frequency based on # of poles.
32	MOTOROFF	Bi-directional I/O pin. Upon reset this pin is configured as an input to allow microprocessor to turn the motor on or off. If over temp occurs, the motor will turn off and this pin is pulled low.

ABSOLUTE MAXIMUM RATINGS

V_{CC1}, V_{CC2}, ... +6.5V
OUT_A, OUT_B, OUT_C ..... GND – 0.3V to V_{CC2} + 4.5V
All other pins ..... GND – 0.3V to V_{CC1} + 0.3V
Output Current, OUTA, B, C ..... ±1A
Input Current per pin ..... ±25mA
Package Dissipation at T_A = 25°C (board mount) . 1.5 Watt
Junction Temperature ..... +150°C
Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 sec) ..... +260°C

OPERATING CONDITIONS

$V_{CC1} = V_{CC2}$ ..... +5V ± 10%
Serial Clock Frequency ..... < 20MHz

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions (unless otherwise stated):

1) $V_{CC1} = V_{CC2}$ = 5V ± 10%,
2) T_A = 0°C to 70°C
3) Serial clock frequency = 20MHz (TBD)
4) System clock frequency = 2MHz
5) Digital timing measured at 1.4V threshold.
6) PD = logic zero.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
V_{CC}	Ckt supply voltage	Operating	4.5	5.0	5.5	V
V_{CC2}	Pwr supply voltage	Operating	4.5	5.0	5.5	V
I_{CC}	V_{CC} current	PIN7 = LOW		6	10	mA
I_{PD}	Sleep current				100	µA
V_{CC}	Power fail		3.8	4.0	4.25	V
V_{CC2}	Power fail		3.8	4.0	4.25	V
DIGITAL INPUT CHARACTERISTICS						
V_{IL}	Low voltage				0.8	V
V_{IH}	High voltage		2.0			V
I_{IH}	High current				+1	µA
I_{IL}	Low current				–1	µA
C_{IN}	Input capacitance			5		pF
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	High voltage	I_{OUT} = 1mA		2.9 ± 0.3V		V
V_{OL}	Low voltage	I_{OUT} = 1mA		0.4	0.8	V
DIGITAL TIMING CHARACTERISTICS						
t_{CSS}	Chip-sel set-up time to Bus-clk		10			ns
t_{CSH}	Chip-sel hold time to Bus-clk		10			ns
t_{DIS}	$DATA_{IN}$ set-up time to Bus-clk		10			ns
t_{DIH}	$DATA_{IN}$ hold time to Bus-clk		10			ns
t_{BKL}	Bus-clk off time		25			ns
t_{BKH}	Bus-clk on time		25			ns
t_{PDHL}	$DATA_{OUT}$ high to low delay to Bus-clk		15			ns
t_{PDLH}	$DATA_{OUT}$ low to high delay to Bus-clk		15			ns

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT SECTION (Phase Outputs, A, B, or C) I_{SLEW} = 1µA						
V_{OH}	V_{OUT} high	I = TBD T = TBD		V_{CC} – 0.5V		V
V_{OL}	V_{OUT} sat low	I = TBD T = TBD		0.5		V
V_F	N-channel clamp diode forward V	I_F = 100mA		0.5		V
t_R	Output rise time	w/o slew control		1.0		µs
t_F	Output fall time	w/o slew control		1.0		µs
t_{RS}	Output rise time	R_{SLEW} = 2M		960		µs
t_{FS}	Output fall time	R_{SLEW} = 2M		960		µs
t_{RS}	Output rise time	R_{SLEW} = 250k		120		µs
t_{FS}	Output fall time	R_{SLEW} = 250k		120		µs
BRAKE SECTION						
V_{BR}	Brake trip point		2.4		2.6	V
V_{CBR}	Brake storage clamp voltage	V_{CC} = 5V		4.3		V
RETRACT SECTION						
V_{RET}	Retract diode $V_{FORWARD}$	I_F = 100mA, T = TBD (V_{OUTX} – V_{PIN14})		0.5		V
CHARGE PUMP SECTION						
I_{PID}	Charge pump source current	V_{PID} = 2.5V, TBD		24		µA
I_{PID}	Sink current			–24		µA
I_{RAT}	Current ratio	I_{PID}(chg)/I_{PID}(dchg)	0.9	1.0	1.1	
PID BUFFER AMPLIFIER SECTION						
V_{OS}	Offset voltage	V_{IN} = 2V		20		mV
Slew	Slew rate			1		V/µs
I_B	Input bias current	V_{IN} = 2V		–10		µA
Swing	Input range		0		4	V
CURRENT CONTROL SECTION						
I_{RSEN}	Gain set #1	I_{OUT} = 120mA		125		µA
I_{RSEN}	Gain set #2	I_{OUT} = 120mA		250		µA
I_{RSEN}	Gain set #3	I_{OUT} = 120mA		500		µA
I_{RSEN}	Gain set #4	I_{OUT} = 120mA		1.0		mA
ERROR AMPLIFIER SECTION						
V_{OS}	Offset voltage	V_{CM} = 2V		40		mV
I_B	Input bias current	V_{CM} = 2V		10	1000	pA
A_{VOL}	Open loop gain	V_{CM} = 2V		60		db
B_W	Bandwidth	V_{CM} = 2V, AV = 1		2		MHz
V_{CMR}	Common-mode range		1.5		4.8	V
V_{REF}	Input clamp V	V_{NIN} = V_{REF}		1.25		V
Slew	Slew rate	V_{CM} = 2V, AV = 1		1.5		V/µs

FUNCTIONAL DESCRIPTION

In a typical disk drive application a microprocessor and the ML6035 are used to start a three phase brushless motor. After start-up the chip can provide stand-alone constant speed control or can be used in an external speed control loop. Unipolar run mode is supported to provide for higher motor speeds. Sensorless motor commutation is provided. See Fig. 1 for a typical application.

MOTOR START-UP

By using a microprocessor to send and receive information from the motor control chip almost any desired variation in any desired start-up algorithm can be achieved.

Under µP control, initial open-loop commutation sequence is provided to the commutation logic through the bits A, B and C. The Motor_off pin is used to control the current to the motor. As the motor is advancing and accelerating, the µP can look at the TACHOUT pin to check the speed of the motor and switch to close loop by setting bit ST.

COMMUTATION LOGIC

Commutation is performed by a 12-bit wide digital circuit. It can detect the zero crossing pulses, then evaluate the time needed between pulses and generate a commutation pulse after the half-time delay. Should the interval of zero crossings exceed the effective range of the counter, the delay will be set at the half of the full count automatically. Unwanted flyback pulses can be blanked out by setting bits FB[5:0]. Blanking time from 4µs to 128µs with a step of 2µs can be programmed by µP. Phase delay less than 30° can be achieved by programming bits PA[7:0].

During momentary power interruptions the continuing motor zero crossing information can be used to recover commutation and resume closed loop speed control.

POWER DRIVERS

Three source PMOS devices and three sink NMOS devices, each capable of 1A @ 500mV are used in complementary output stages. When mode switching is used to change from bipolar drive to unipolar drive the upper devices are disabled and an additional PMOS transistor is used to pull the motor neutral to the 5V supply.

By using a small portion of each lower FET a closed loop current mirror can be created to monitor the current in each leg. The currents from the three lower current mirrors are summed to provide a voltage across R_{SENSE} for a local current loop.

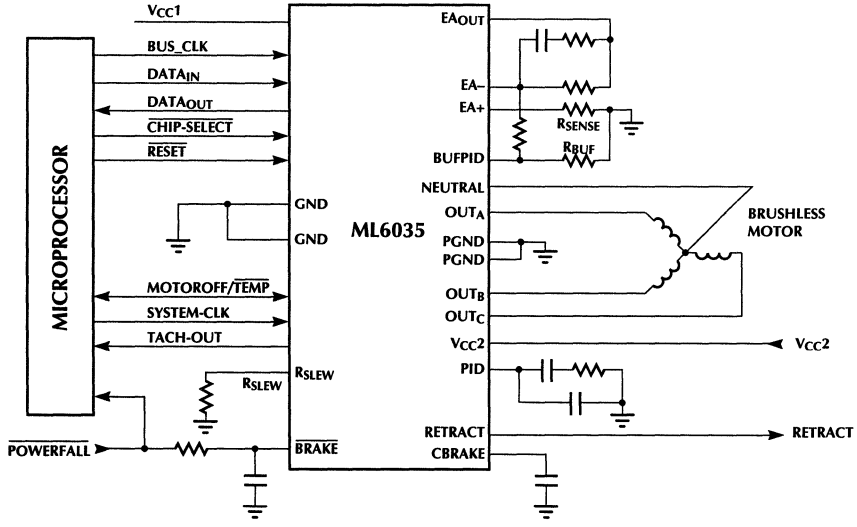


Figure 1. Typical Application Circuit

After a power failure, during the brake delay time period, the outputs are turned off so that the back-EMF energy can be used to retract the heads. Three schottky diodes are connected from the motor output pins to the retract pin to rectify the back EMF from the still spinning motor. The return rectification is provided by three schottky diodes tied in conjunction with the body diodes of each N-channel sinking transistor.

BRAKING LOGIC

This block provides active braking to slow down motor rotation quickly. A signal applied to an R/C network connected to the external brake pin initiates a delay prior to braking (turning off the P-channel devices and turning on all the output N-channel devices). A brake command from the serial bus initiates an immediate braking sequence with no delay. To prevent a momentary high current spike due to simultaneous conduction of a P-Channel and an N-channel power output device, a motor off command should be issued prior to a serial bus brake command.

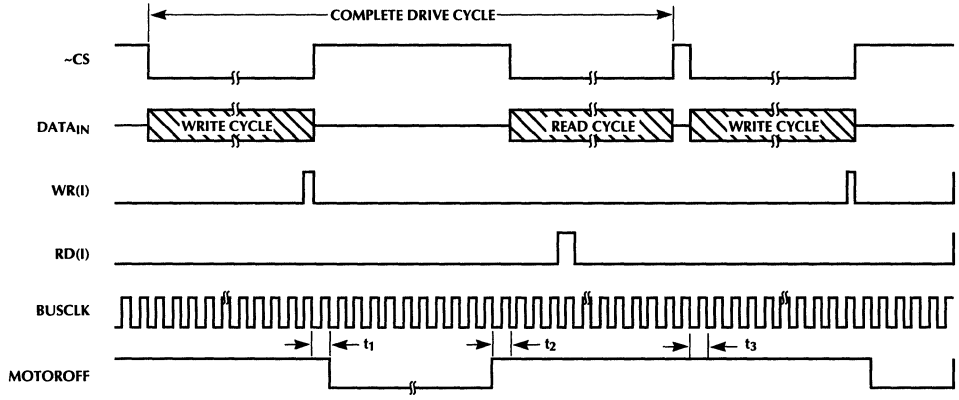
SPEED CONTROL

During motor start a command from the serial bus can select one out of four divide ratios from the sum of the currents in the output sink devices (0.0005, 0.001, 0.002 and 0.004) to be applied to the R_{SENSE} pin. The voltage so formed is used to derive a current loop at the non-inverting input to the error amplifier. By starting with a low ratio 1A drive currents can be achieved. Note that the current loop is active during start-up.

When sufficient speed is reached to close the commutation loop (16% of final speed) the R_{SENSE} ratio can be selected to provide more dynamic range at the R_{SENSE} pin for the normal operating current and internal speed control (velocity loop) can be used. This is done by using a one pulse per revolution signal from the commutation circuit to compare with a preset value for the 14-bit divider, which together with the [external] system clock frequency determine the speed (see Figure 3). A digital frequency comparator compares these two signals and generates a command signal to the charge pump to charge up or discharge the external PID filter. The voltage at the PID pin is internally buffered and applied to the BUFOUT pin. The buffered PID signal is then applied to the inverting input to the error amplifier to provide a reference for the current loop and to complete the velocity loop.

If sector data information is available the charge pump can be disabled by a signal from the serial bus and the sector information can be input to the PID pin to control the current loop (see next section).

5



Notes: t1 = min time required between "end of write" and "motor-activate"
t2 = min time required between "motor inactivate" and "beginning of read"
t3 = min time required between "read" and "write"

Figure 2. Start-up Waveform

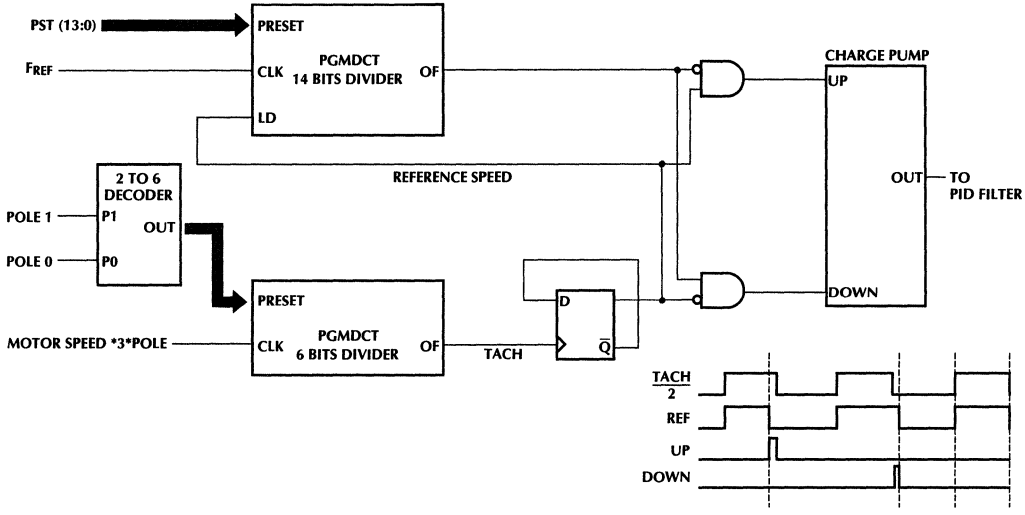


Figure 3. Speed Control

CURRENT AND SLEW RATE CONTROL

This block provides output current wave shaping to minimize very steep current slopes. The elimination of these steep currents helps to reduce magnetostriction noise in the motor windings and helps to eliminate or minimize flyback pulses caused by the motor winding inductance. Slew rate control is provided on both the P-channel devices and the N-channel devices and is active for both rise and fall. The charge and discharge rate for the slew rate control is set by an external resistor, R_{SLEW}. The value of this resistor should be adjusted so that a rise time or fall time of 20% (40% for both) of each "on" time. The range for R_{SLEW} is 250K to 2MΩ. This corresponds to a t_{RS}, t_{FS} range of 120µs to 960µs. For example, an "ON" time of 1ms, 40% corresponds to 400µs which equates to 1.1MΩ.

In addition to slew rate control the chip also supports a linear current loop on the lower (sinking) power drivers. A signal from the external PID filter is buffered and applied as a reference signal to an error amplifier shown in Figure 4. The error signal for this amplifier is derived from the R_{SENSE} signal described in the power driver section above. The error amplifier has both inputs and the output available so compensation for the current loop can be easily done.

The maximum output current limit is used during motor start and is programmed from the serial bus by selecting the current ratio at Isense as mentioned above.

DIVIDE BY N BLOCK

The "divide by N" block shown in the block diagram, supplies a selectable tach output. If selected from the serial bus, one pulse per revolution is provided. This signal is derived from the equivalent of a divider tied to the zero crossing comparator for phase A. This will insure a signal with minimum jitter. A register loaded from the serial bus programs the divider for a 4, 8, 12 or 16 pole motor. During start-up a serial command can disable the divide circuit to provide raw zero crossing information to the tach out pin.

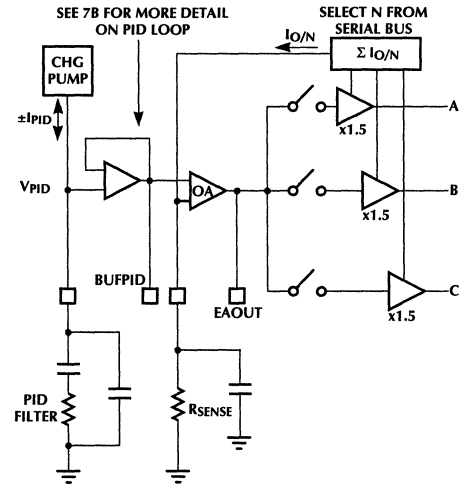


Figure 4. Current Loop Velocity Loop

LOW VOLTAGE DETECT

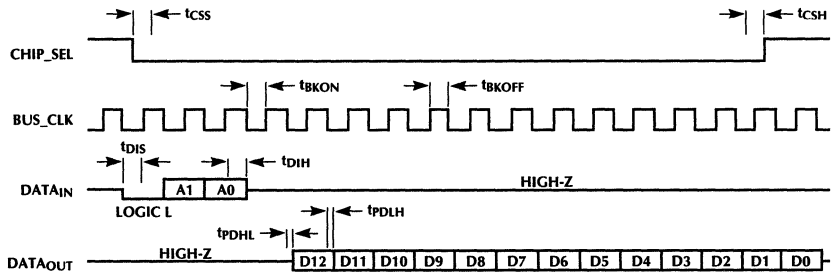
This section provides a fail safe low voltage detect for both V_{CC} and V_{CC2}. In most systems the low voltage detect resides on the Voice coil driver chip and has a threshold voltage of 4.575V with 30mV hysteresis. In the event this external chip fails to detect a low voltage condition or in the event this function is not available in another chip, then an internal low voltage detect (Vth = 4.325V, hysteresis = 30mV) will disable the outputs and initiate a shutdown with retract voltage available.

OVER TEMPERATURE FLAG

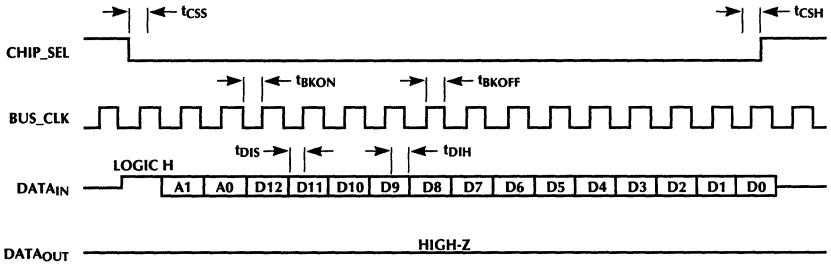
This section is located close to the output drivers and is used to detect an over temperature condition. At a temperature of 150 degree C the following events will occur: the outputs will be turned off and the Motor-off pin will be pulled low to signal the microprocessor that a thermal shutdown has occurred. The motor-off pin is reset to normal operation by the sleep command. When the microprocessor "sees" motor off go low it should initiate a retract so the heads can be parked prior to motor braking.

SERIAL I/O AND CONTROL LOGIC

The digital interface consists of a four-wire serial port. The 16-bit data word present on the $DATA_{IN}$ pin is serially shifted on the rising edges of the serial interface clock when the chip-select pin is active low. The R/WR bit is shifted in first and followed by address bits and data bits. To read stored data word, data will be shifted out from the $DATA_{OUT}$ pin on the falling edge of the serial clock when the chip-select pin is active low. When the chip select pin is high, $DATA_{IN}$ and Bus-Clk are ignored.



Read Waveform



Write Waveform

CONTROL REGISTER 0

R/W	A1	A0	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	A	B	C	REV	Sleep	Brake	ST	D3P	UNI	CP2	CP1	T2	T0

COMMUTATION START POINT

D12 to D10 000 = A+ OFF A– OFF B+ OFF B– OFF C+ OFF C– OFF
001 = A+ OFF A– OFF B+ OFF B– ON C+ ON C– OFF
010 = A+ OFF A– ON B+ ON B– OFF C+ OFF C– OFF
011 = A+ OFF A– ON B+ OFF B– OFF C+ ON C– OFF
100 = A+ ON A– OFF B+ OFF B– OFF C+ OFF C– ON
101 = A+ ON A– OFF B+ OFF B– ON C+ OFF C– OFF
110 = A+ OFF A– OFF B+ ON B– OFF C+ OFF C– ON
111 = A+ OFF A– OFF B+ OFF B– OFF C+ OFF C– OFF

In read mode, these three bits contain the commutation status latched at the falling edge of CS.

D9 0 = forward direction
1 = reverse direction

D8 0 = sleep mode
1 = on

D7 0 = brake off
1 = brake on

D6 0 = commutated by setting D12-D10 of control register 0
1 = commutated by digital delay loop

D5 0 = Tach-out (1 pulse/phase)
1 = Tach-out (1 pulse/rev.)

D4 1 = Unipolar operation
0 = Bipolar operation

D2–D3 Charge pump
00 = normal operation
01 = discharge
10 = charge
11 = high impedance

D1–D0 Debug mode. Enables part to a/p internal signals from the data-out (serial out) pin.
00 = tachout (normal operation)
01 = blanking pulse width
10 = $\overline{UP}$
11 = commutation pulse

Note: a logic "0" refers to a logic low signal
a logic "1" refers to a logic high signal

CONTROL REGISTER 1

R/W	A1	A0	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	0	1	0	P1	P0	CL1	CL0	Tach/DN	—	FB5	FB4	FB3	FB2	FB1	FB0

D11,D10 00 = 4 pole motor
01 = 8 pole motor
10 = 12 pole motor
11 = 16 pole motor

D9, D8 Current limit
11 = I at R_{SENSE} = 0.0005 * Iout Sink (A or B or C)
00 = I at R_{SENSE} = 0.0010 * Iout Sink (A or B or C)
01 = I at R_{SENSE} = 0.0020 * Iout Sink (A or B or C)
10 = I at R_{SENSE} = 0.0040 * Iout Sink (A or B or C)

D7 Tach/DN 0 = DN pulse
1 = Tach out

D6 Unused

D5-D0 Blanking pulse width

Time step = prescale factor*/system clock rate
= 4 /(2 x 106 counts/sec) = 2 usec/count
* the prescale factor is: 4 for a four pole motor
2 for an eight pole motor
1 for a twelve pole motor
1 for a sixteen pole motor

Note: a logic "0" refers to a logic low signal
a logic "1" refers to a logic high signal

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CONTROL REGISTER 2

R/W	A1	A0	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	1	0	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	—	—	—	—	FR0

D0 = Least significant bit for # of counts to preset the frequency down counter (see next page for formula and remaining bits)

D1 to D4 Not used

D12 to D5 Select the desired phase advance

$$\text{Counts needed per electrical degree} = \frac{\text{system} - \text{clock rate}}{\text{prescale factor}} \times \frac{60}{\text{rpm}} \times \frac{1}{(3 * \text{poles})} \times \frac{1}{60}$$

$$= \frac{2E6\ \text{count/sec}}{4} \times \frac{60\ \text{sec/min}}{3600\ \text{rev/min}} \times \frac{1}{3 \times 4\ \text{phase/rev}} \times \frac{1}{60\ \text{deg/ph}}$$

$$= 11.6\ \text{count/el degree}$$

* The prescale factor is: 4 for a 4 pole motor
2 for an 8 pole motor
1 for a 12 pole motor
1 for a 16 pole motor

Note: a logic "0" refers to a logic low signal
a logic "1" refers to a logic high signal

CONTROL REGISTER 3

R/W	A1	A0	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	1	1	FR13	FR12	FR11	FR10	FR9	FR8	FR7	FR6	FR5	FR4	FR3	FR2	FR1

D12 TO D0 equal the # of counts to preset the frequency down counter

$$\text{counts needed} = \frac{\text{system clock rate}}{\text{prescale factor}} \times \frac{60}{\text{rpm}}$$

$$= \frac{2E6\ \text{counts/rev}}{4} \times \frac{60\ \text{sec/min}}{3600\ \text{rev/min}}$$

$$= 8{,}333\ \text{counts/rev}$$

$$= 10, 0000, 1000, 1101$$

* The prescale factor is fixed in all cases.

Note: a logic "0" refers to a logic low signal
a logic "1" refers to a logic high signal

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6035CH	0°C to +70°C	32-Pin TQFP (H32)

ML6042

Tape Drive Data Channel Processor

GENERAL DESCRIPTION

The ML6042 is a single chip Data Channel for high capacity tape drives supporting a floppy like interface. It integrates the head preamplifier, pulse detector, filter/equalizer, and write driver functions. It also contains the gap/hole detector, under-voltage detector, and write driver with MR head bias. All major functions are controlled and their parameters programmed via the serial interface.

This IC is intended for tape drive systems typically utilizing the QIC formats. Specifically the QIC40/80 and the QIC3010/3020 recording formats. The minimal external components combined with the very small package makes the ML6042 ideal for designs with board space and height constraints like the popular 3½" form factor half height drives.

The head preamp is compatible with both thin film and magneto resistive heads with a programmable MR bias. The write driver currents are also programmable.

The filter is a 6 pole, 2 zero, 0.05° equi-ripple continuous time configuration with asymmetric equalization. The cutoff frequency and amount of asymmetric equalization are programmable via the serial interface in 32 steps. The cutoff frequency can range from 200KHz to 1.6MHz in two ranges.

The pulse detector utilizes a high bandwidth AGC and supports both fixed and variable gain modes with programmable attack and decay.

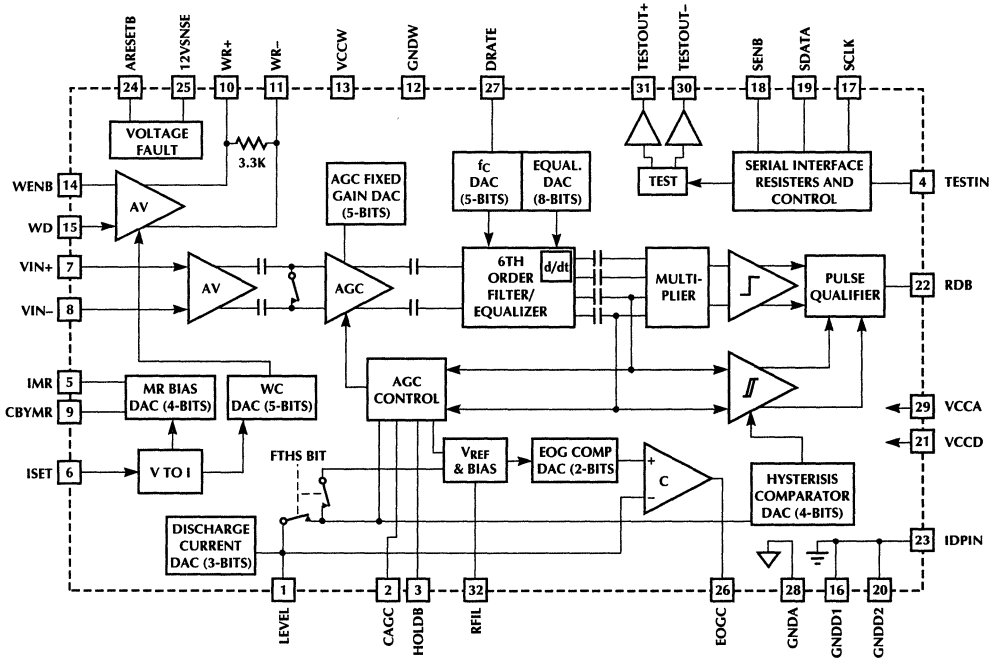
The three wire serial microprocessor interface has a buffered data latch.

The ML6042 is available in a low profile 32 pin SOIC package. (0.3" wide)

FEATURES

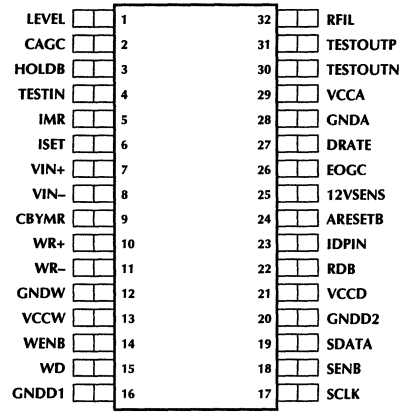
- Complete data channel for tape drives
- Compatible with QIC 40/80/3010/3020 formats
- Data rates — 2 Mbps (MFM) or 5 Mbps (RLL)
- All key parameters are programmable
- Minimal external components
- Continuous time filter with asymmetric equalization
- Less than 500mW operating power dissipation
- Total jitter & pulse pairing < 5% of window

BLOCK DIAGRAM



PIN CONFIGURATION

ML6042
32-pin SOIC (S32)



TOP VIEW

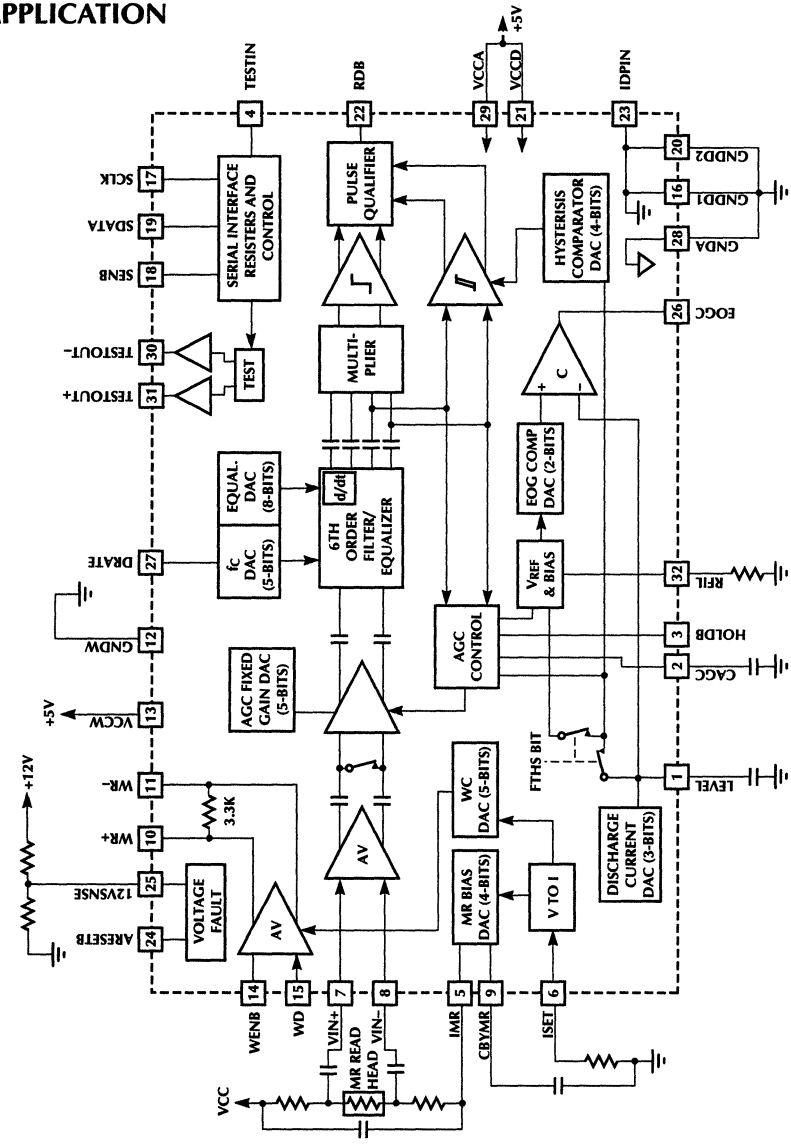
PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	LEVEL	Rectified signal level output, and input to the programmable hysteresis comparator. An external capacitor connects between this pin and GNDA to set the discharge time constant.
2	CAGC	The AGC loop capacitor connects between this pin and GNDA.
3	HOLDB	Logic input for AGC disable. A low on this pin disables the charging and discharging paths to the CAGC pin causing it to float.
4	TESTIN	Control input to select the test signal on the TESTOUT pin. An input voltage of 0–1V selects the AGC output at TESTOUT, 2–3V selects the multiplier output, and 4–5V selects the filter low pass output.
5	IMR	MR bias current sink output pin.
6	ISET	External resistor to GNDA that sets the write driver and MR bias current.
7	VIN+	Differential signal positive input to read channel.
8	VIN–	Differential signal negative input to read channel.
9	CBYMR	MR bias circuit bypass capacitor to GNDA.
10	WR+	Differential positive write driver output. One side of the write head coil and damping resistor connects to this pin.
11	WR–	Differential negative write driver output. One side of the write head coil and damping resistor connects to this pin.
12	GNDW	Ground connection for the write driver.
13	VCCW	Positive power supply (5V) connection for the write driver.
14	WENB	Write enable logic input. A logic low on this pin enables the write driver, switches the AGC amplifier to fixed gain mode, and discharges the CAGC pin to the lower clamp voltage. A logic high disables the write driver and initiates the write to read transition clamp time-out.
15	WD	Write data input, MFM encoded.
16	GNDD1	Digital ground.
17	SLCK	Clock input for serial interface.
18	SENB	Logic input for serial interface enable. Active low.
19	SDATA	Serial data input.
20	GNDD2	Digital ground.
21	VCCD	Positive power supply connection (+5V) for digital circuitry.
22	RDB	Read data output. Encoded data from pulse detector.
23	IDPIN	Used for chip identification. If not used it should be connected to GNDA.
24	ARESETB	Under voltage status logic output. Active low.

PIN DESCRIPTION (Continued)

PIN#	NAME	FUNCTION
25	12VSNSE	Sense input for 12 volt fault detector. An external resistor divider from +12 volts to ground connects to this pin.
26	EOGC	Output of end-of-gap detector.
27	DRATE	Control input for selecting the cutoff frequency of the filter. A logic high sets the filter to the high range and a logic low to the low range. It has an internal pull down.
28	GNDA	Analog ground.
29	VCCA	Positive power connection for the analog circuitry.
30	TESTOUT–	Differential negative test signal output. See TESTIN.
31	TESTOUT+	Differential positive test signal output. See TESTIN.
32	RFIL	External resistor to GNDA sets the center frequency of the filter.

TYPICAL APPLICATION



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6042CS	0°C to +70°C	32-PIN SOIC (S32)

ML6310

3V/5V Read Channel Front-end Processor

GENERAL DESCRIPTION

The ML6310 is a BiCMOS Read Channel Front-end Processor IC which is one half of the disk read channel chipset from Micro Linear, intended for the next generation of small form factor (1.8" & 1.3") disk drives, operating on 3V and/or 5V supplies. It works in conjunction with the ML6311 Read Channel Back-end Processor to form a complete solution for the low-voltage/ low-power disk read/write channel. It incorporates a full function pulse detector, four channel servo demodulator, and a filter/equalizer with switchable response characteristics between data and servo.

The filter architecture consists of a 6-pole, 2-zero, 0.05° Equiripple type, continuous time filter, with asymmetric equalization, realizing a family of frequency response curves optimized for the disk drive read channel. The cutoff frequency and boost (asymmetric equalization) are programmable through the serial interface using internal 5- & 4-bit DACs. The pulse detector is implemented with a high bandwidth AGC whose attack and decay rates are programmable through the serial interface using 2-bit DACs respectively. The Hysteresis level for the pulse detector Gate channel is also programmable through the serial interface using a 4-bit DAC. A four channel servo demodulator is onboard which offers buffered outputs for head positioning with a programmable option to bring out either A, B, C, D or A+B, A–B, C–D, C+D outputs.

The ML6310 supports four power down modes for implementation of real-time power management in an optimal manner. The operating power dissipation is targeted to be less than 300mW at 3V, while the part will dissipate less than 15µW in the sleep mode. The ML6310 requires only three external components.

FEATURES

- Operating supply ranges are 2.7V to 3.3V or 3.0V to 3.6V or 4.5 to 5.5V.
- Very Low Power dissipation at 3V P_{SLEEP} < 15µW, P_{OPR} < 300 mili-watts
- Low profile, 32-pin TQFP package, (7 x 7 x 1) mm^3
- NRZ Disk data rates up to 32 Mbits/s, for 1,7 RLL
- Pulse detector with less than ±500ps pulse pairing
- Wide bandwidth (> 60MHz) AGC amplifier
- Internal stable reference voltage level for AGC
- Programmable hysteresis level in Gate channel (static)
- Four channel servo demodulator with internal capacitors for track & hold capability. Selectable A, B, C, D or A–B, C–D, A+B, C+D demod outputs.
- Onboard coupling capacitors and DC offset cancellation circuitry to minimize internal offsets
- 6-pole, 2-zero continuous time, 0.05° equiripple filter with less than 40dB harmonic distortion
- Programmable filter cutoff frequency (3 :1 range in 32 steps) (f_C = 6.0 to 18 MHz). Also allows a 10% range shift under external resistor control
- Programmable Asymmetric Equalization in 256 steps (256 combinations of Group Delay and Boost), providing 0 to 11.6 dB slimming boost at f_C.
- High speed (20MHz clock) three wire serial microprocessor interface with double buffered data latch for synchronous or asynchronous data loading.
- Four Power-down modes selectable, plus hardware pin
- CMOS / TTL compatible I/O to minimize power

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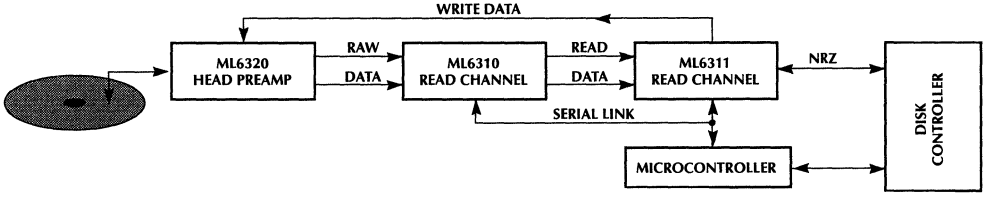
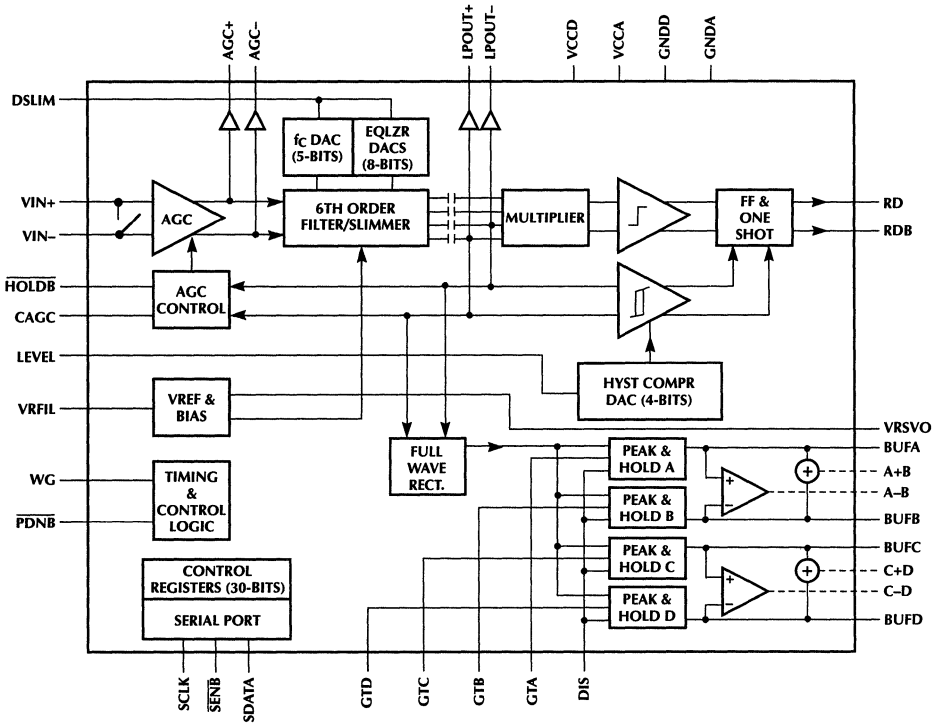
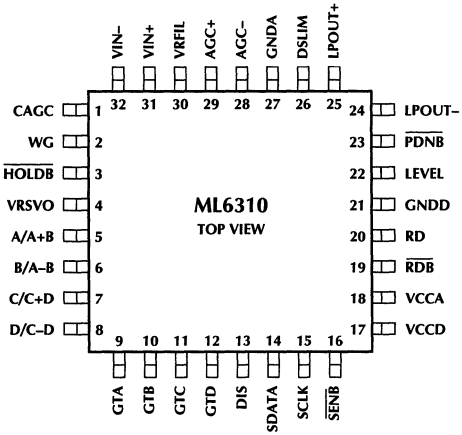
SYSTEM BLOCK DIAGRAM



BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN	NAME	FUNCTION
Pulse Detector		
31 32	VIN+ VIN–	AGC amplifier differential input. This input is AC coupled from the Read/ Write amplifier output. It is recommended that the differential input signal be in the range of $15mV_{P-P}$ to $150mV_{P-P}$.
1	CAGC	The AGC loop capacitor is connected from this pin to GNDA. Lead-Lag network may be used for a differential loop filter characteristic, if desired. The Attack and Decay currents of the AGC can be adjusted through the bits in the control register.
3	$\overline{\text{HOLDB}}$	This is an active low CMOS input pin. When this pin is forced to a logic low, all the charging and discharging paths on the CAGC pin are disabled. The AGC amplifier now acts as a fixed gain amplifier with the gain being determined by the voltage on the CAGC pin.
22	LEVEL	Rectified signal level output and input to the programmable hysteresis comparator. An external capacitor between this pin and GNDA, in conjunction with an internal resistor (8 Kohms typical), sets up the discharge time constant.
20 19	$\overline{\text{RD}}$ $\overline{\text{RDB}}$	These pins provide the differential pulse detector encoded read data output (ECL). These signals form the input to the ML6311 — read channel back-end processor chip which does the data synchronization and clock recovery. (Low voltage ECL O/P's)
29 28	AGC+ AGC–	Buffered AGC outputs used for test and prototyping purposes. These are differential open emitter outputs and hence should be left open in normal operation to minimize power dissipation.
Filter / Equalizer		
30	VRFIL	A resistor between this pin and GNDA sets up the center frequency of the filter.
26	DSLIM	When this pin is high, the slimming function is disabled and the filter cutoff frequency is switched to the servo filter cutoff frequency. When this pin is low the filter data path cutoff frequency is used, with the slimming being programmable.

PIN	NAME	FUNCTION
Filter / Equalizer (continued)		
25 24	LPOUT+ LPOUT–	Buffered lowpass filter outputs used for test and prototyping purposes. These are differential open emitter outputs and hence should be left open in normal operation to minimize power dissipation.
Timing and Control		
23	$\overline{\text{PDNB}}$	Active low CMOS input. In conjunction with the power management bits in the Control Register, this helps setup the ML6310 in one of the four power down modes.
2	WG	Active high CMOS input. This input is used to activate the input clamp for a period of 1µs, to generate the write to read transition delay.
Servo Demodulator		
4	VRSVO	This reference voltage derived from the internal bandgap is used by the A/D converter handling the servo bursts, to define the middle point of the dynamic range. A typical value for this is 1.0V.
9 10 11 12	GTA GTB GTC GTD	Gate control for the four channel servo burst detectors. Active high CMOS inputs. Internal holding capacitors hold the charge corresponding to the peaks of the servo bursts.
13	DIS	Active high CMOS input. When this pin is asserted high, the four servo peak detector capacitors are discharged.
5 6 7 8	A/A+B B/A–B C/C+D D/C–D	Buffered four channel servo demodulator outputs. The four outputs can be optionally selected to be either A, B, C, D or A+B, A–B, C+D, C–D through a bit (SMODE), in the Control Register #6
Serial Interface		
15	SCLK	This is a CMOS input which clocks the Control Register (negative edge trigger). Internally this pin is gated with the $\overline{\text{SENB}}$ signal.
14	SDATA	Control Register Data, CMOS input, clocked by SCLK.
16	$\overline{\text{SENB}}$	Active low CMOS input — Control Register enable. A logic low input on this pin pin allows the SCLK input to clock the SDATA into the control register and a logic high latches the control register contents.

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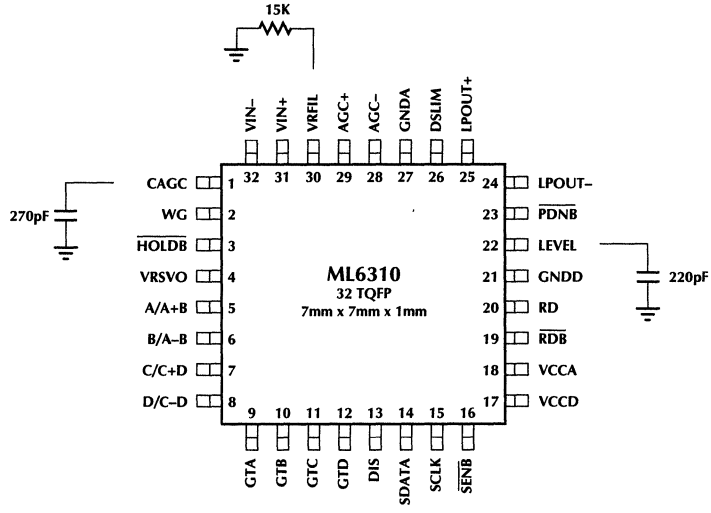
PIN DESCRIPTION (continued)

PIN	NAME	FUNCTION
Power Supply and Ground		
18	VCCA	This is the analog VCC input, used for the pulse detector, filter/equalizer and servo demodulator. In the case of a 5V supply operation this pin needs to be left open, while in the case of a 3V supply operation this pin is tied to VCCD.
17	VCCD	Digital VCC input for serial microprocessor interface and related logic. This can handle the 2.7V to 5.5V supply range.
27	GNDA	Analog ground
21	GNDD	Digital ground

TYPICAL EXTERNAL COMPONENTS



ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (VCCA & VCCD) ..... –0.3 to +7V
Analog & Digital Inputs/Outputs ..... –0.3 to VCCA + 0.3V
Input Current per Pin ..... –25 to +25mA
Storage Temperature ..... –65 to +150°C
Maximum Junction Temperature ..... 125°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage Range ..... 2.7V to 3.6V or 4.5V to 5.5V
For 5V Operation ..... VCCA is left open, VCCD is at 5V
For 3V Operation ..... VCCA and VCCD are tied to 3V
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VCCA = VCCD = 2.7 to 3.6 Volts or 4.5 to 5.5 Volts and T_A = 0 to 70°C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Dissipation					
Analog V_{CC} (VCCA)	Left open for 5V operation	2.7		3.6	V
Digital V_{CC} (VCCD)	Connected for both 3V & 5V	2.7		5.5	V
Supply Current (Analog)	@ VCCA = 3.0V @ Sleep mode (PDNB pin = 0)			80 8	mA µA
Supply Current (Digital)	@ VCCA = 3.0V or 5.0V @ Sleep mode (PDNB pin = 0)			10 2	mA µA
Supply Current (Total)	VCCA = VCCD = 3.0V VCCD = 5.0V, VCCA = open @ sleep mode (PDNB pin = 0)			90 110 10	mA mA µA
Power Down Current (Normal mode)	PDNB pin = 1 Control Reg bits PM1=PM0=0			90	mA
Power Down Current (Servo mode)	Serial Interface + AGC + Filter + Servo demodulator enabled PDNB = 1, PM1= 0, PM0 = 1			65	mA
Power Down Current (Pulse mode)	Serial Interface + AGC + Filter + Pulse Detector enabled PDNB = 1, PM1= 1, PM0 = 0			68	mA
Power Down Current (Idle mode)	Only Serial Interface enabled PDNB = 1, PM1= 1, PM0 = 1				
	VCC = 2.7 to 3.6V		0.45	30	µA
	VCC = 4.5 to 5.5V		0.8	1.5	mA
Power Down Current (Sleep mode)	Control register retains data PDNB = 0, PM1= X, PM0 = X		0.15	5	µA
Digital I/O Specifications					
High level input voltage		VCCD-0.5		VCCD	V
Low level input voltage		GNDD		GNDD+0.5	V
High level input current	@ VCC and GND			1	µA
Low level input current	@ VCC and GND			1	µA
AGC Amplifier and Input Clamp					
Differential Input signal range	Note 2	15		150	mV_{P-P}
Maximum AGC gain	VCAGC = 1.2V @ AGC ± pins	15	22	28	V/V
Minimum AGC gain	VCAGC = 2.2V @ AGC ± pins		0.6	3	V/V
Differential input resistance	Read mode (WG is low)	3.75	5	6.25	Kohms
	Write mode (WG is high)	200	500	700	Ohms

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AGC Amplifier and Input Clamp (continued)					
CMRR	$V_{IN}+ = V_{IN}- = 100$ mV @ 5MHz & VCAGC = 1.2 V	40			dB
PSRR	VCCA = 100 mV @ 5 MHz & VCAGC = 1.2 V		40		dB
CAGC voltage range	@ VCCD = 2.7V Note 1	1		2.2	V
Input Clamp Off time	From WG active to input clamp release	0.7	1	1.3	µs
Clamp propagation delay	From WG inactive to input Z clamped		20	100	ns
AGC Control — Rectifier and Comparator					
CAGC clamp voltage		1.2	1.8	2.5	V
CAGC Output voltage	Maximum possible	1.8	VCCA/0.5	3.0	V
CAGC Attack current	Min — Control register bits = 00 Max — Control register bits = 11	20 70	30 120	45 170	µA µA
CAGC Decay current	Min — Control register bits = 00 Max — Control register bits = 11	1 6	3 9	6 12	µA µA
CAGC leak current	$\overline{HOLDB}$ pin is low			±0.1	µA
HOLD on / off	$\overline{HOLDB}$ pin, ON time and OFF time		0.5		µs
Hysteresis Comparator					
Input signal range	Differential input, Note 1				
Hysteresis range	percent of input signal amplitude	0		93.8	%
Hysteresis resolution	controlled by internal DAC, Note 1		6.25		%
Max output current	LEVEL pin short to gnd (I_{SHORT} > 1 mA)	1			mA
Output resistance	LEVEL pin		400		ohms
Pulse Qualification Section					
Read Data pulse width		20		30	ns
Pulse Pairing	0.2 MHz sinewave @ 15 mV_{P-P} diff, f_C = 9MHz (1 sigma)		±0.5	±1	ns
Jitter on RD (falling edge)	0.2 MHz sinewave @ 15 mV_{P-P} diff, f_C = 9MHz (1 sigma)		±0.1	±1	ns
RD/RDB raw data output	Differential, Psuedo ECL $\lvert V_{RD} - V_{RDB} \rvert$	0.6	0.7	0.8	V
$V_{RD/RDB}$ common mode	Note 1		VCCA – V_{BE}		V
Filter / Equalizer Section					
Differential Group delay	0.3f_C to f_C, f_C0–f_C4 = 1			±5	%
Cutoff Frequency Accuracy		–10		+10	%
Slimming Level Accuracy		–1		+1	dB
Phase shift (LP & BP)	f_C0–f_C4 = 1, Note 2		90 ±2		degree
Response settling time	Due to change in f_C, Note 2		1		µs

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Servo Demodulator Section (All tests @ f = 5 MHz)					
Servo Amplifier voltage gain	@ Input = 50 mV and 150 mV. AGC set to a gain of 1.	3	5	7	V/V
Channel offset matching			±2	±10	mV
Output leakage current			5		nA
Discharge time	Input = 150 mV, discharge to 50% output			5	µs
Droop rate	Input = 150 mV, GATE on to GATE off		0.01	0.1	mV/µs
Acquisition time	Gate enable to 90% of peak detector output		1	1.5	µs
Difference error	Input = 150 mV		±2	±10	mV
VRSVO output voltage		0.9	1.05	1.3	V
Serial Microprocessor Interface					
Serial clock (SCLK) frequency		0.01		20	MHz
SCLK pulse width	t_{PW}	20			ns
SCLK to SDATA hold time	t_{HSD}	5			ns
SDATA to SCLK setup time	t_{SSD}	5			ns
$\overline{SENB}$ to SCLK setup time	t_{SSEN}	10			ns
SCLK to $\overline{SENB}$ hold time	t_{SSEN}			10	ns

Note 1: These specifications are design goals and are not tested They are provided for informational purposes only.
Note 2: These parameters are guaranteed by design and verified by characterization only and are not part of the production test program, hence only the typical values are indicated for system designer's reference.

5

TIMING DIAGRAM

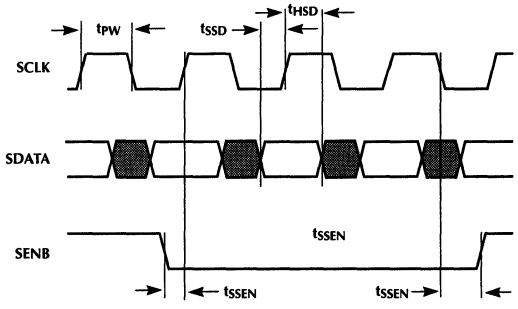


Figure 1. 3-Wire Serial Interface.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The ML6310 is a Read Channel Front-end Processor IC which is one half of the disk read channel chipset from Micro Linear, intended for the next generation of small form factor (1.8" & 1.3") disk drives, operating on 3V and/or 5V supplies. Fabricated in Micro Linear's BiCMOS process (1.5µ CMOS, 4GHz f_t bipolar), it works in conjunction with the ML6311 Read Channel Back-end Processor to form a complete solution for the low voltage/low power disk read/write channel. It incorporates a full function pulse detector, four channel servo demodulator, and a filter/equalizer with switchable response characteristics between data and servo. The ML6310 supports four power down modes for implementation of real-time power management in an optimal manner. The maximum power dissipation is targeted to be less than 350mW, while the part will dissipate less than 1 mW in the sleep mode. In this mode all sections are powered down except the serial microprocessor interface. A high level of digital programmability through this interface and onboard registers contributes to reducing the external component count significantly.

The pulse detector is implemented with a high bandwidth AGC whose attack and decay rates are programmable through the serial interface using 2-bit DACs respectively. The Hysteresis level for the pulse detector Gate channel is also programmable through the serial interface using a 4-bit DAC. Pulse qualification is achieved by using both level and polarity.

A four channel servo demodulator is onboard which offers buffered outputs for head positioning with a programmable option to bring out either A, B, C, D or A+B, A–B, C–D, C+D outputs. The four hold capacitors for the servo peak detectors are implemented on board.

The programmable filter architecture consists of a 6-pole, 2-zero. 0.05° Equiripple type, continuous time filter, with asymmetric equalization, realizing a family of frequency response curves optimized for the disk drive read channel. For embedded servo handling, the servo and the data path filter cutoff frequencies are programmed separately. Using the external DSLIM pin, the filter characteristics can be switched to the servo cutoff frequency with no slimming boost. The switching of the filter frequency response is very fast, thus allowing for real-time embedded servo handling The cutoff frequency and boost (asymmetric equalization) are programmable through the serial interface using internal 5-bit and 4-bit DACs.

The three wire serial interface is also used to program a number of parameters controlling the various sections of the chip. On physical power-up, the control registers will come up in an undetermined state and hence these registers must be initialized to their default values first, so that the chip is put in a defined state. The contents of the control registers are retained in all power down modes, except when the power is physically turned off to the chip.

The ML6310 is designed to offer the lowest power dissipation, a high level of integration and offer a high level of programmability to minimize the number of external components, thus resulting in an optimized read channel front-end. It outputs raw data in an ECL format whose level is compatible with the input to the companion chip ML6311, used for data separation and clock synchronization. Please refer to the block diagram of the ML6310 for the details.

PULSE DETECTOR

The pulse detector consists of the AGC amplifier with a full AGC control loop, on the front-end, which works in conjunction with the programmable filter/equalizer circuitry. The pulse detector consists of the conventional time channel and gate channel to help in pulse qualification, for generating the raw data output which represents the time position of the peaks corresponding to the flux reversals on the disk.

AGC

The AGC amplifier is a two stage differential amplifier design with high bandwidth, typically greater than 100MHz. The first stage of the AGC is a Variable Gain Amplifier (VGA) whose gain is controlled by the voltage on the CAGC pin. The gain of the amplifier decreases as the voltage on the CAGC pin increases. The second stage is essentially a fixed gain amplifier.

The AGC usually gets its differential input from the output of the head preamp circuit. The input signal range is 15mV to 150mV peak-to-peak differential. The AGC's input has a switchable input impedance clamp to enhance the write to read transient recovery. This is indirectly controlled by the Write Gate signal from the disk controller. When Write Gate is active-high (write mode), the input impedance is reduced or clamped to a low impedance state and when Write Gate goes inactive-low, the input impedance switches back to the normal (high impedance state), after a 1µs delay, typically.

The output of the AGC amplifier feeds into the filter/equalizer directly. The lowpass output from the filter/equalizer serves as the input to the AGC control front-end which is a full wave rectifier. The AGCSET comparator compares the full wave rectifier output with an internal settled voltage reference and generates an output to the AGC control circuitry. The AGC control circuitry compares this voltage with the voltage from the CAGC pin, before providing the feedback into the control nodes of the Variable Gain Amplifier. The capacitor on the CAGC pin then gets charged or discharged depending on whether the full wave rectifier output is greater than or less than the preset internal reference voltage. The charging and discharging current, also referred to as the attack and decay rates, are programmable through the bits in control register #5, as shown below. Refer to the section on Control Register for programming details.

1	0	1	REG	DKY1	DKY0	ATK1	ATK0

During the servo capture period, the AGC amplifier functions as a fixed gain amplifier, under control of the HOLDB pin. When the HOLDB pin is forced to a logic low, the AGC control loop is disabled and the charging and discharging of the capacitor on the CAGC pin is stopped. The AGC loop maintains the gain setting prior to the HOLDB pin going low. The impedance and gain of the AGC amplifier are not affected.

Time Channel

The time channel of the pulse detector consists of a multiplier and a zero crossing comparator, the output of which generates the clocking signal to the pulse qualification flip-flop. The input of the multiplier is the differential lowpass and bandpass outputs of the filter/equalizer. The capacitative coupling ensures the removal of any DC offsets in the differentiated outputs of the filter/equalizer. This technique contributes significantly to better pulse pairing by eliminating the need for a matching bidirectional one-shot as used in conventional approaches.

The output of the multiplier goes to the zero-crossing comparator which produces a logic output whose edges correspond to the zero crossing points of the input signal. A positive transient of state at the zero crossing output indicates that a minima and maxima has been detected at the filter/equalizer's differentiated output.

Gate Channel

The Gate Channel consists of a hysteresis comparator which prevents false triggering of the output one-shot due to baseline noise. The lowpass output of the filter/equalizer forms the input of the hysteresis comparator. Only when a data pulse is of sufficient amplitude will the hysteresis comparator allow the output one shot to be triggered. The hysteresis comparator also ensures that the output one-shot is triggered once for each data pulse polarity. The hysteresis level (as a percentage of the hysteresis comparator input signal peak), is programmable through the bits in control register #4, as shown below. Refer to the section on Control Register for programming details.

1	0	0	NC	HYS3	HYS2	HYS1	HYS0

Pulse Qualification

The pulse qualification circuitry consists of a D flip-flop whose data input is the hysteresis comparator output and it is clocked by the zero-crossing comparator output in the time channel. The output of this D flip-flop triggers a one-shot whose pulse width is programmed through an internal RC constant. In order to allow the zero-crossing comparator output to fire the one-shot, every positive transient in the zero-crossing comparator shall correspond to the opposite polarity of the hysteresis comparator output. The output of the one-shot then constitutes the raw data output which represents the time position of the peaks corresponding to the flux transitions on the disk media.

PROGRAMMABLE FILTER/EQUALIZER

The programmable filter/equalizer circuit approximately realizes a sixth-order, 0.05° Equiripple function thus achieving a flat group delay up to twice the cutoff frequency ($2f_C$). The filter processes signals in a differential mode for greater noise immunity. This filter architecture is capable of handling fast transients and provides smaller excess phase and power dissipation. It is made up of three biquads which generate a lowpass and bandpass (differentiated) output. The cutoff (corner) frequency of the filter is controlled by 5 bits in control register which provide 32 combinations in the range of 6MHz to 18MHz. Control register #0 is used to program the data channel corner frequency while the servo channel corner frequency is programmed in control register #1, as shown below. Refer to the section on Control Register for programming details.

DATA PATH CUTOFF FREQUENCY

0	0	0	Df_C4	Df_C3	Df_C2	Df_C1	Df_C0

SERVO PATH CUTOFF FREQUENCY

0	0	1	Sf_C4	Sf_C3	Sf_C2	Sf_C1	Sf_C0

These five bits are used to control a DAC to generate a current which is used to control the frequency of the filter. The cutoff (corner) frequency of the filter is given by the following equation :

$$f_C = 6 + (0.387 \times 16 f_C4 + 8 f_C3 + 4 f_C2 + 2 f_C1 + f_C0)$$

Table 1 lists the corner frequencies and the corresponding control register bit configurations.

Two real zeroes are introduced by two equalizers (slimmers) inserted between the first/second and the second/third biquads. The zeroes can be adjusted independently so that it is possible to realize asymmetric equalization, if desired. The transfer function of the equalizer (slimmer) is given by :

$$H_S = \left[1 - \left(k_1 \times \frac{S}{\omega_{O1}}\right)\right]\left[1 + \left(k_2 \times \frac{S}{\omega_{O2}}\right)\right]$$

Where ω_{O1}, ω_{O2} are the corner frequencies of the first and second biquads and $S = j\omega$ is the complex frequency. The normalized corner frequencies of the first and second biquads are 0.981 and 2.074. The group delay variation at the corner frequency is given by :

$$\Delta G_{\omega C} = \frac{1}{\omega_C}\left[\frac{\left(\frac{k_1}{0.981}\right)^3}{1+\left(\frac{k_1}{0.981}\right)^2} - \frac{\left(\frac{k_2}{2.074}\right)^3}{1+\left(\frac{k_2}{2.074}\right)^2}\right]$$

k_1 and k_2 can be controlled by adjusting the bias currents in the slimmers. They are adjusted by changing the slimming control bits — zeroA (N_A) in control register #2 and zeroB (N_B) in control register #3 as shown below. Refer to Table 2 and the section on Control Register, for details.

MSB

0	1	0	RSVD	EA3	EA2	EA1	EA0

MSB

0	1	1	RSVD	EB3	EB2	EB1	EB0

k_1 & k_2 are expressed by the equations below :

$$k_1 = \frac{k_{1MAX} N_A}{15} \qquad k_{1MAX} = 1.578$$

$$k_2 = \frac{k_{2MAX} N_B}{15} \qquad k_{2MAX} = 3.327$$

N_A and N_B are the decimal expression of the slimming bits EA3 – EA0 and EB3 – EB0, respectively. Hence the group delay and corner frequency product (refer table 2), is given by :

$$\Delta G_{\omega C} f_C = \frac{1}{2\pi}\left[\frac{(0.1078N_A)^3}{1+(0.1078N_A)^2} - \frac{(0.1078N_B)^3}{1+(0.1078N_B)^2}\right]$$

The equalization (slimming) level is given by :

$$SL(dB) = 10\log\left[1+\left(\frac{k_1 \times \omega}{\omega_{O1}}\right)^2\right] + 10\log\left[1+\left(\frac{k_2 \times \omega}{\omega_{O2}}\right)^2\right]$$

At the corner frequency of the filter (18 MHz), the equation is reduced to :

$$SL(dB) = 10\log\left[1+(0.1078N_A)^2\right] + 10\log\left[1+(0.1078N_B)^2\right]$$

TABLE 1: Corner frequency programming values

f_C4	f_C3	f_C2	f_C1	f_C0	f_C (MHz)
0	0	0	0	0	6.000
0	0	0	0	1	6.387
0	0	0	1	0	6.774
0	0	0	1	1	7.161
0	0	1	0	0	7.548
0	0	1	0	1	7.935
0	0	1	1	0	8.323
0	0	1	1	1	8.710
0	1	0	0	0	9.097
0	1	0	0	1	9.484
0	1	0	1	0	9.871
0	1	0	1	1	10.258
0	1	1	0	0	10.645
0	1	1	0	1	11.032
0	1	1	1	0	11.419
0	1	1	1	1	11.806
1	0	0	0	0	12.194
1	0	0	0	1	12.581
1	0	0	1	0	12.968
1	0	0	1	1	13.355
1	0	1	0	0	13.742
1	0	1	0	1	14.129
1	0	1	1	0	14.516
1	0	1	1	1	14.903
1	1	0	0	0	15.290
1	1	0	0	1	15.677
1	1	0	1	0	16.065
1	1	0	1	1	16.452
1	1	1	0	0	16.839
1	1	1	0	1	17.226
1	1	1	1	0	17.613
1	1	1	1	1	18.000

Table 2 shows the Product of Delta Group Delay & f_C , slimming level, zeroA and zeroB programming values with control register bit configurations. The values, Binary (EA3 – EA0) = Decimal N_A and Binary (EB3 – EB0) = Decimal N_B.

FILTER TRANSFER FUNCTION

$$= \left[\frac{\omega_{01}^2}{s^2 + \frac{s \times \omega_{01}}{Q_1} + \omega_{01}^2}\right]\left[\frac{\omega_{02}^2}{s^2 + \frac{s \times \omega_{02}}{Q_2} + \omega_{02}^2}\right]\left[\frac{\omega_{03}^2}{s^2 + \frac{s \times \omega_{03}}{Q_3} + \omega_{03}^2}\right]$$

Where: $\omega_{01} = 0.981\ \omega_C$
$\omega_{02} = 2.074\ \omega_C$
$\omega_{03} = 1.470\ \omega_C$
$Q_1 = 0.551$
$Q_2 = 1.686$
$Q_3 = 0.893$

TABLE 2

N_A	N_B	ΔGf_C(sHz)	SL(dB)
0	0	0	0
0	1	0.0002	0.0502
0	2	0.0015	0.1973
0	3	0.0049	0.432
0	4	0.0108	0.7406
0	5	0.0193	1.1077
0	6	0.0304	1.5178
0	7	0.0436	1.9574
0	8	0.0585	2.4148
0	9	0.0749	2.8809
0	10	0.0922	3.3487
0	11	0.1103	3.8132
0	12	0.1289	4.2706
0	13	0.1478	4.7187
0	14	0.1669	5.1557
0	15	0.1862	5.5807
1	0	–0.0002	0.0502
1	1	0	0.1004
1	2	0.0013	0.2475
1	3	0.0047	0.4822
1	4	0.0106	0.7908
1	5	0.0191	1.1578
1	6	0.0302	1.568
1	7	0.0434	2.0076
1	8	0.0583	2.465
1	9	0.0747	2.9311
1	10	0.092	3.3989
1	11	0.1101	3.8634
1	12	0.1287	4.3208
1	13	0.1476	4.7688
1	14	0.1667	5.2058
1	15	0.186	5.6309
2	0	–0.0015	0.1973
2	1	–0.0013	0.2475
2	2	0	0.3946
2	3	0.0033	0.6293
2	4	0.0092	0.9379
2	5	0.0178	1.305
2	6	0.0288	1.7152
2	7	0.0421	2.1547
2	8	0.057	2.6121
2	9	0.0733	3.0782
2	10	0.0907	3.546
2	11	0.1088	4.0105
2	12	0.1273	4.468
2	13	0.1463	4.916
2	14	0.1654	5.353
2	15	0.1846	5.778
3	0	–0.0049	0.432
3	1	–0.0047	0.4822
3	2	–0.0033	0.6293
3	3	0	0.864
3	4	0.0059	1.1726
3	5	0.0144	1.5397
3	6	0.0255	1.9498
3	7	0.0387	2.3894
3	8	0.0537	2.8468
3	9	0.07	3.3129
3	10	0.0873	3.7807
3	11	0.1054	4.2452
3	12	0.124	4.7026
3	13	0.1429	5.1507
3	14	0.162	5.5877
3	15	0.1813	6.0127

N_A	N_B	ΔGf_C(sHz)	SL(dB)
4	0	–0.0108	0.7406
4	1	–0.0106	0.7908
4	2	–0.0092	0.9379
4	3	–0.0059	1.1726
4	4	0	1.4812
4	5	0.0086	1.8483
4	6	0.0196	2.2584
4	7	0.0328	2.698
4	8	0.0478	3.1554
4	9	0.0641	3.6215
4	10	0.0815	4.0893
4	11	0.0995	4.5538
4	12	0.1181	5.0112
4	13	0.137	5.4593
4	14	0.1562	5.8963
4	15	0.1754	6.3213
5	0	–0.0193	1.1077
5	1	–0.0191	1.1578
5	2	–0.0178	1.305
5	3	–0.0144	1.5397
5	4	–0.0086	1.8483
5	5	0	2.2153
5	6	0.0111	2.6255
5	7	0.0243	3.065
5	8	0.0392	3.5225
5	9	0.0556	3.9886
5	10	0.0729	4.4564
5	11	0.091	4.9208
5	12	0.1096	5.3783
5	13	0.1285	5.8263
5	14	0.1476	6.2633
5	15	0.1668	6.6884
6	0	–0.0304	1.5178
6	1	–0.0302	1.568
6	2	–0.0288	1.7152
6	3	–0.0255	1.9498
6	4	–0.0196	2.2584
6	5	–0.0111	2.6255
6	6	0	3.0357
6	7	0.0132	3.4752
6	8	0.0282	3.9326
6	9	0.0445	4.3987
6	10	0.0619	4.8666
6	11	0.0799	5.331
6	12	0.0985	5.7885
6	13	0.1174	6.2365
6	14	0.1366	6.6735
6	15	0.1558	7.0985
7	0	–0.0436	1.9574
7	1	–0.0434	2.0076
7	2	–0.0421	2.1547
7	3	–0.0387	2.3894
7	4	–0.0328	2.698
7	5	–0.0243	3.065
7	6	–0.0132	3.4752
7	7	0	3.9148
7	8	0.015	4.3722
7	9	0.0313	4.8383
7	10	0.0486	5.3061
7	11	0.0667	5.7706
7	12	0.0853	6.228
7	13	0.1042	6.6761
7	14	0.1233	7.1131
7	15	0.1426	7.5381

TABLE 2 (continued)

N_A	N_B	ΔGf_C(sHz)	SL(dB)
8	0	–0.0585	2.4148
8	1	–0.0583	2.465
8	2	–0.057	2.6121
8	3	–0.0537	2.8468
8	4	–0.0478	3.1554
8	5	–0.0392	3.5225
8	6	–0.0282	3.9326
8	7	–0.015	4.3722
8	8	0	4.8296
8	9	0.0163	5.2957
8	10	0.0337	5.7635
8	11	0.0517	6.228
8	12	0.0703	6.6854
8	13	0.0892	7.1335
8	14	0.1084	7.5705
8	15	0.1276	7.9955
9	0	–0.0749	2.8809
9	1	–0.0747	2.9311
9	2	–0.0733	3.0782
9	3	–0.07	3.3129
9	4	–0.0641	3.6215
9	5	–0.0556	3.9886
9	6	–0.0445	4.3987
9	7	–0.0313	4.8383
9	8	–0.0163	5.2957
9	9	0	5.7618
9	10	0.0173	6.2296
9	11	0.0354	6.6941
9	12	0.054	7.1515
9	13	0.0729	7.5996
9	14	0.092	8.0366
9	15	0.1113	8.4616
10	0	–0.0922	3.3487
10	1	–0.092	3.3989
10	2	–0.0907	3.546
10	3	–0.0873	3.7807
10	4	–0.0815	4.0893
10	5	–0.0729	4.4564
10	6	–0.0619	4.8666
10	7	–0.0486	5.3061
10	8	–0.0337	5.7635
10	9	–0.0173	6.2296
10	10	0	6.6975
10	11	0.0181	7.1619
10	12	0.0367	7.6194
10	13	0.0556	8.0674
10	14	0.0747	8.5044
10	15	0.0939	8.9294
11	0	–0.1103	3.8132
11	1	–0.1101	3.8634
11	2	–0.1088	4.0105
11	3	–0.1054	4.2452
11	4	–0.0995	4.5538
11	5	–0.091	4.9208
11	6	–0.0799	5.331
11	7	–0.0667	5.7706
11	8	–0.0517	6.228
11	9	–0.0354	6.6941
11	10	–0.0181	7.1619
11	11	0	7.6264
11	12	0.0186	8.0838
11	13	0.0375	8.5318
11	14	0.0566	8.9688
11	15	0.0759	9.3939

N_A	N_B	ΔGf_C(sHz)	SL(dB)
12	0	–0.1289	4.2706
12	1	–0.1287	4.3208
12	2	–0.1273	4.468
12	3	–0.124	4.7026
12	4	–0.1181	5.0112
12	5	–0.1096	5.3783
12	6	–0.0985	5.7885
12	7	–0.0853	6.228
12	8	–0.0703	6.6854
12	9	–0.054	7.1515
12	10	–0.0367	7.6194
12	11	–0.0186	8.0838
12	12	0	8.5413
12	13	0.0729	7.5996
12	14	0.092	8.0366
12	15	0.1113	8.4616
13	0	–0.1478	4.7187
13	1	–0.1476	4.7688
13	2	–0.1463	4.916
13	3	–0.1429	5.1507
13	4	–0.137	5.4593
13	5	–0.1285	5.8263
13	6	–0.1174	6.2365
13	7	–0.1042	6.6761
13	8	–0.0892	7.1335
13	9	–0.0729	7.5996
13	10	–0.0556	8.0674
13	11	–0.0375	8.5318
13	12	–0.0189	8.9893
13	13	0	9.4373
13	14	0.0191	9.8743
13	15	0.0384	10.299
14	0	–0.1669	5.1557
14	1	–0.1667	5.2058
14	2	–0.1654	5.353
14	3	–0.162	5.5877
14	4	–0.1562	5.8963
14	5	–0.1476	6.2633
14	6	–0.1366	6.6735
14	7	–0.1233	7.1131
14	8	–0.1084	7.5705
14	9	–0.092	8.0366
14	10	–0.0747	8.5044
14	11	–0.0566	8.9688
14	12	–0.038	9.4263
14	13	–0.0191	9.8743
14	14	0	10.311
14	15	0.0192	10.736
15	0	–0.1862	5.5807
15	1	–0.186	5.6309
15	2	–0.1846	5.778
15	3	–0.1813	6.0127
15	4	–0.1754	6.3213
15	5	–0.1668	6.884
15	6	–0.1558	7.0985
15	7	–0.1426	7.5381
15	8	–0.1276	7.9955
15	9	–0.1113	8.4616
15	10	–0.0939	8.9294
15	11	–0.0759	9.3939
15	12	–0.0573	9.8514
15	13	–0.0384	10.299
15	14	–0.0192	10.736
15	15	0	11.162

SERVO DEMODULATOR

Four gated peak detectors are incorporated for recovery of embedded servo information. The ML6310 provides four buffered low impedance outputs (A, B, C, D), which represent the peak detected level of each servo burst. The voltages on these pins are suitable for digitizing by an external A/D converter and processed by the controlling microprocessor for head positioning. With the help of the SMODE bit in control register #6, these four outputs can be configured to be (A+B, A–B, C+D, C–D) using internal summation and difference amplifiers. The summation outputs (A+B, C+D) are equal to the sum of the peak detected levels divided by 2. The difference outputs (A–B, C–D) are equal to the difference of the peak detected levels divided by 2. The zero-level for the difference outputs (A–B, C–D) is given at the VRSVO pin. The typical value for this reference signal is 1V. There is also a VSET bit in control register #6 which controls the direction of the VRSVO pin. If VSET = 0, the difference zero-level is generated internally (1V). If VSET = 1, an external reference voltage is used to set the difference zero-level.

The zero-level for the buffered servo outputs (A, B, C, D) or the summation outputs (A+B, C+D) is internally generated and has a value of 0.5V.

1	1	0	RSVD	SMODE	VSET	PM1	PM0

The servo peak detectors in the demodulator section receive the servo burst signal from the lowpass output of the filter/equalizer, which are then amplified to the proper amplitude and sent through a full wave rectifier before the sample and hold operation. There are four identical peak and hold circuits, with internal holding capacitors which perform the sample and hold operation. This optimized architecture thus provides for higher integration by not only eliminating the four external holding capacitors but also the pins required for them, thus contributing towards minimizing the external component count and hence cost.

POWER MANAGEMENT

The ML6310 provides a hardware pin ($\overline{PDNB}$) and two bits in the control register #6 for five levels of micro power management control.

1	1	0	RSVD	SMODE	VSET	PM1	PM0

The major circuit blocks in the ML6310 comprise of the regulator, the serial interface, the AGC, the filter/equalizer, the pulse detector, the servo demodulator and the bias circuits. The $\overline{PDNB}$ pin in conjunction with the two bits in the control register #6 can be used to selectively turn of a combination of these blocks depending on the mode of operation viz, read mode, write mode, servo mode, etc. This allows the system designer to turn off the sections of the chip that are not in use during the operation and thus minimize power dissipation at a micro management level. Table 3 below shows these five different power management modes and the circuits that are active in these individual modes.

TABLE 3: Power Management Modes

PIN	PM1	PM0	POWER MANAGEMENT MODE
1	0	0	Normal mode
1	0	1	Servo mode
1	1	0	Data mode
1	1	1	Idle mode
0	X	X	Sleep mode

Normal Mode — All circuits are enabled. Typical Power dissipation @ 2.7V is 175mW.

Servo Mode — Pulse Detector is disabled. Typical Power dissipation @ 2.7V is 150mW.

Data Mode — Servo demodulator is disabled. Typical Power dissipation @ 2.7V is 160mW.

Idle Mode — Only serial interface circuit and regulator are enabled. In 3V mode of operation the regulator is not used and could be powered off using the 'reg' bit in control register #5. Typical Power dissipation @ 4.75V is 4mW. Typical Power dissipation @ 2.7V is 1.2µW.

Sleep Mode — All circuits disabled, however control registers will hold latest programmed data and can be accessed through the serial interface. Typical Power dissipation @ 2.7V is 0.5µW.

SERIAL MICROPROCESSOR INTERFACE

The serial microprocessor interface consists of a simple three-wire serial port. Data is shifted serially into the ML6310 on the SDATA line on the falling edges of the serial shift clock, SCLK, provided the $\overline{SENB}$ pin is active (low). The data is shifted in blocks of eight bits with MSBit first. The internal registers are organized in blocks of eight bits, with the three most significant bits denoting the address, followed by the five data bits. This addressing scheme thus allows for a register bank of eight registers. When the chip is physically powered-up, the control registers come up in an undetermined state and hence they need to be initialized to some preset bit configuration so that the behavior of the chip is predictable. The control registers retain their programmed information in any of the power-down modes, until the chip is physically powered-down. When the $\overline{SENB}$ pin goes inactive (high), the SDATA and SCLK pins are ignored and the previously shifted information is latched on the rising edge of the $\overline{SENB}$, into the appropriate register bank based on the address bits. It is recommended that the SCLK input be kept inactive low till such time when it is in use. The SCLK input is capable of handling speeds up to 20MHz.

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CONTROL REGISTER DEFINITIONS

The control register bank consists of eight registers with addresses from 0 through 7. Control register #7 is not used and some of the bits in control register 0 through 6 are reserved. Outlined below are the detailed bit by bit definitions of the control registers 0 through 6.

CONTROL REGISTER #0

Data Channel filter cutoff frequency control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	0	0	Df_C4	Df_C3	Df_C2	Df_C1	Df_C0

CONTROL REGISTER #1

Servo Channel filter cutoff frequency control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	0	1	Sf_C4	Sf_C3	Sf_C2	Sf_C1	Sf_C0

f_C4	f_C3	f_C2	f_C1	f_C0	f_C (MHz)
0	0	0	0	0	6.000
0	0	0	0	1	6.387
0	0	0	1	0	6.774
0	0	0	1	1	7.161
0	0	1	0	0	7.548
0	0	1	0	1	7.935
0	0	1	1	0	8.323
0	0	1	1	1	8.710
0	1	0	0	0	9.097
0	1	0	0	1	9.484
0	1	0	1	0	9.871
0	1	0	1	1	10.258
0	1	1	0	0	10.645
0	1	1	0	1	11.032
0	1	1	1	0	11.419
0	1	1	1	1	11.806
1	0	0	0	0	12.194
1	0	0	0	1	12.581
1	0	0	1	0	12.968
1	0	0	1	1	13.355
1	0	1	0	0	13.742
1	0	1	0	1	14.129
1	0	1	1	0	14.516
1	0	1	1	1	14.903
1	1	0	0	0	15.290
1	1	0	0	1	15.677
1	1	0	1	0	16.065
1	1	0	1	1	16.452
1	1	1	0	0	16.839
1	1	1	0	1	17.226
1	1	1	1	0	17.613
1	1	1	1	1	18.000

CONTROL REGISTER #2

Asymmetric equalization (slimming) — zero A (N_A)

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	1	0	RSVD	EA3	EA2	EA1	EA0

Refer to Table 2 for programming configurations

CONTROL REGISTER #3

Asymmetric equalization (slimming) — zero B (N_B)

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	1	1	RSVD	EB3	EB2	EB1	EB0

Refer to Table 2 for programming configurations

CONTROL REGISTER #4

Hysteresis Comparator qualification level

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	0	0	RSVD	HYS3	HYS2	HYS1	HYS0

HYS3	HYS2	HYS1	HYS0	% OF SIGNAL PEAK
0	0	0	0	0.00 %
0	0	0	1	6.25 %
0	0	1	0	12.50 %
0	0	1	1	18.75 %
0	1	0	0	25.00 %
0	1	0	1	31.25 %
0	1	1	0	37.50 %
0	1	1	1	43.75 %
1	0	0	0	50.00 %
1	0	0	1	56.25 %
1	0	1	0	62.50 %
1	0	1	1	68.75 %
1	1	0	0	75.00 %
1	1	0	1	81.25 %
1	1	1	0	87.50 %
1	1	1	1	93.75 %

CONTROL REGISTER #5

AGC Attack & Decay rate control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	0	1	REG	DKY1	DKY0	AKY1	AKY0

REG bit = 1 implies regulator is ON

REG bit = 0 implies regulator is OFF

This bit applies only in the 3V operating mode where the regulator could be switched OFF, to minimize power dissipation, as it is not needed. This bit must be set to a "1" in the 5V operating mode.

ATK1	ATK0	AGC ATTACK CURRENT
0	0	30µA
0	1	60µA
1	0	90µA
1	1	120µA

DKY1	DKY0	AGC DECAY CURRENT
0	0	3.0µA
0	1	5.0µA
1	0	7.0µA
1	1	9.0µA

CONTROL REGISTER #6

Miscellaneous functions register

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	1	0	RSVD	SMODE	VSET	PM1	PM0

RSVD implies bit reserved for future use. Can be zero or one.

PM1, PM0 power management mode bits

$\overline{\text{PDNB}}$ PIN	PM1	PM0	POWER MANAGEMENT MODE
1	0	0	Normal mode
1	0	1	Servo mode
1	1	0	Data mode
1	1	1	Idle mode
0	x	x	Sleep mode

SMODE = 1 implies servo demodulator outputs are configured as A+B, A–B, C+D, C—D

SMODE = 0 implies servo demodulator outputs are configured as A, B, C, D

VSET = 1 VRSVO servo reference pin configured as **input**. This allows the use of an external reference to calibrate the servo demodulator outputs for data conversion.

VSET = 0 VRSVO servo reference pin configured as **output**. This implies that the internal reference is used to calibrate the servo demodulator outputs for data conversion purposes.

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ORDERING INFORMATION

PART NUMBER	VCC RANGE	TEMPERATURE RANGE	PACKAGE
ML6310 CH2	2.7V to 3.3V	0°C to 70°C	32-pin TQFP (H32)
ML6310 CH3	3.0V to 3.6	0°C to 70°C	32-pin TQFP (H32)
ML6310 CH5	4.5V to 5.5V	0°C to 70°C	32-pin TQFP (H32)

3V/5V Read Channel Back-end Processor

GENERAL DESCRIPTION

The ML6311 is a BiCMOS Read Channel Back-end Processor IC which is one half of the disk read channel chipset from Micro Linear, intended for the next generation of smaller form factor (1.8" & 1.3") disk drives, operating on 3V and 5V supplies. It works in conjunction with the ML6310 Read Channel Front-end Processor to form a complete solution for the low voltage/low power disk read/write channel. It incorporates a full function data synchronizer with a 3:1 operating range, a full function frequency synthesizer with onboard M&N dividers, (1,7) RLL encoder/decoder and write precompensation circuitry. The most critical blocks on this chip are the three VCOs, one for the data synchronizer PLL, one for the frequency synthesizer PLL and the third VCO is used to generate the tracking 1/3 cell delay for (1,7) RLL data synchronization. Careful design considerations have been incorporated to minimize the noise coupling and crosstalk among the VCOs. The system noise is highly minimized as the VCO operates at only 1.5X the data rate.

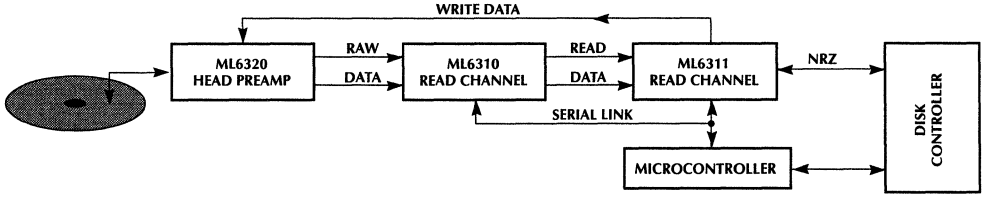
It provides 40-bits for user programmability of a number of features through a serial microprocessor interface and a bank of internal control registers. The center frequency of the VCO, window centering, M & N dividers and power management options are programmable. Independent early and late write precompensation programmability is provided through a 6-bit decoder array. The ML6311 requires two external components besides the two loop filters for the PLL's.

The ML6311 supports six power down modes. An external hardware pin is also provided to implement real time power management. The operating power dissipation is targeted to be less than 170mW, while it will dissipate less than 100µW in the sleep mode.

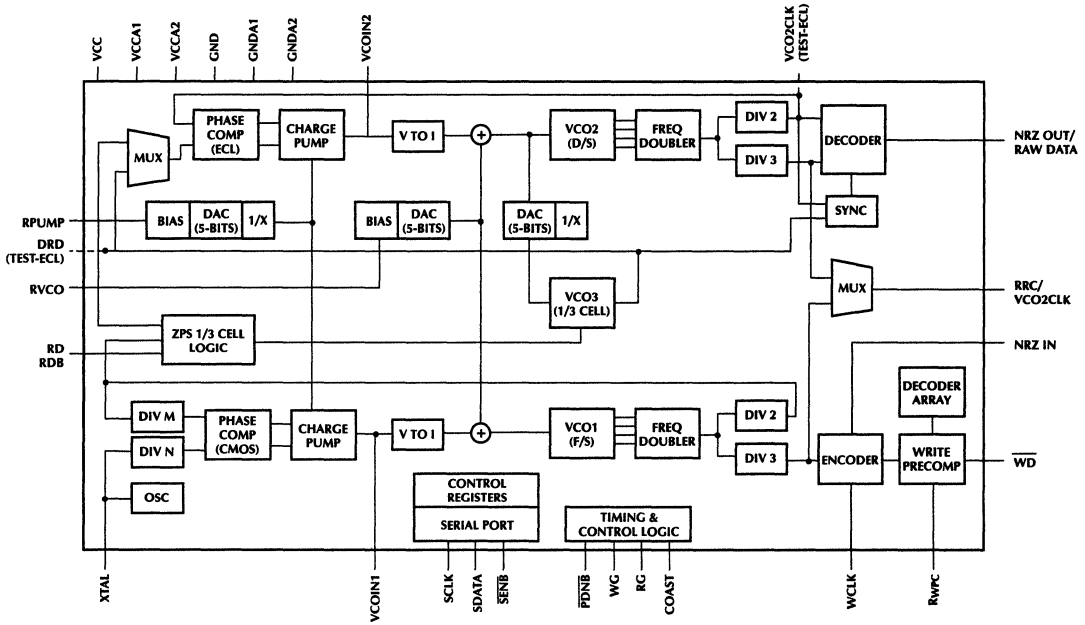
FEATURES

- Operating supply range 2.7V to 3.6V or 4.5V to 5.5V
- Very Low Power dissipation at 3V
  P_{SLEEP} < 100µW, P_{OPR} < 170mW
- Low profile, small area, 32-pin TQFP package
- 3:1 Disk data rate range — 11 to 32 Mbits/s
- Fast acquisition PLL with zero phase start capability
- 3:1 VCO tuning range with 48 Mbits/s 1,7RLL code rate
- Onboard (1, 7) RLL encoder/decoder
- Tracking 1/3 cell delay for internal 1,7 RLL Endec and 1/4 cell delay for external 2, 7 RLL Endec
- Programmable VCO center frequency and window centering adjustment (75% to 125% in steps of 1.6%)
- PLL based frequency synthesizer with reference crystal oscillator and M (7-bit) & N (7-bit) dividers
- Programmable independent early and late write precompensation.
- High speed (20MHz) three wire serial microprocessor interface with double buffered data latches
- Programmable six levels of power management control with external power down pin support
- CMOS, TTL compatible I/O interface for lower power

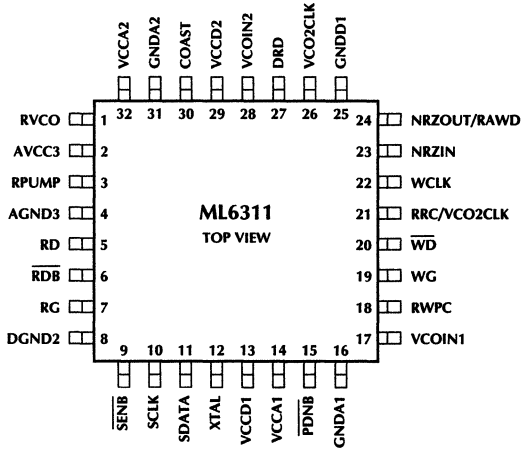
SYSTEM BLOCK DIAGRAM



BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN	NAME	FUNCTION
ECL Level Logic Inputs		
5	RD	Encoded read data from the disk drive read channel front-end chip ML6310. The rising edges of RD represent the flux changes on the disk. (differential "+" input)
6	$\overline{\text{RDB}}$	Encoded read data from the disk drive read channel front-end chip ML6310. The falling edges of RDB represent the flux changes on the disk. (differential "–" input)
ECL Level Logic Outputs		
(Note: These are test outputs for characterization purposes. External current sources are necessary to provide driving capability for these signals and the ECL buffer needs to be enabled from Control Register #7)		
27	DRD	Delayed read data output after the 1/3rd cell delay. This signal is used for 1/3rd cell delay characterization and window margin test.
26	VCO2CLK	Test point for Data seperator VCO clock output.
CMOS Level Logic Inputs		
7	RG	Read Gate signal from the disk controller. Active high signal indicates read mode. This input selects the phase detector input, switches the RRC output, initiates the data separator PLL acquisition and enables the (1, 7) RLL decoder.
19	WG	Write Gate signal from the disk controller. Active high signal indicates write mode. This input enables the (1, 7) RLL encoder and write precompensation circuits.
30	COAST	A high level on this pin disables phase detector/charge pump of the data separator PLL and allows the VCO to coast.
15	$\overline{\text{PDNB}}$	Power Down Control. A low level input on this pin puts the chip in the power down (SLEEP) mode with a power dissipation of less than 100µW.
12	XTAL	A parallel resonant crystal with low parasitic capacitance is connected between this pin and ground as the master clock source. If a crystal oscillator is not desired, an external clock can be forced onto this pin.

PIN	NAME	FUNCTION
CMOS Level Logic Inputs (continued)		
22	WCLK	Write data clock from disk controller. This is the data rate clock synchronized to the RRC. If minimum cable delay is desired, WCLK pin can be shorted to RRC.
23	NRZIN	Non-return to zero write data input from disk controller. In write mode, NRZIN is clocked into the chip on the rising edges of the WCLK.
9	$\overline{\text{SENB}}$	Active low CMOS input — Control Register Enable. A logic low input on this pin allows the SCLK input to clock the SDATA into the control Register and a logic high on this input, latches the control register contents.
10	SCLK	This is a CMOS input which clocks the Control Register. Internally this pin is gated with the $\overline{\text{SENB}}$ signal. While $\overline{\text{SENB}}$ is low, address and programming data are clocked in at the chip on the falling edges of SCLK.
11	SDATA	Control Register Data, CMOS input, clocked by SCLK.
CMOS Level Logic Outputs		
24	NRZOUT	Non-return to zero read data output. This is the synchronized and decoded data from the disk drive. In the read mode, NRZOUT is clocked out of the chip on the falling edges of RRC. In the external Endec mode (selected through the control register #6 RAW bit), this pin provides the synchronized encoded data output.
21	RRC	Read/Reference clock. In the write mode, this pin outputs 1X (data rate) clock derived from the frequency synthesizer VCO clock. In the read mode, it switches to 1X clock derived from the data separator VCO clock after detecting 19 pulses on the RD line. In the external Endec mode (selected through the control register #6 RAW bit), this pin outputs 1.5X clock (1, 7RLL) and 2X clock (2, 7RLL), derived from the data separator VCO2.
20	$\overline{\text{WD}}$	(1, 7) RLL encoded write data output.

PIN DESCRIPTION

PIN	NAME	FUNCTION
Analog Pins		
18	RWPC	A 1% timing resistor for write precompensation delay setting.
4	RVCO	A 1% resistor connected between this pin and GNDA3 sets the current level for data rate programmability.
3	RPUMP	1% resistor connected between this pin and GNDA3 sets the charge pump current for the two PLL's and the bias current for miscellaneous blocks.
17	VCOIN1	Frequency synthesizer PLL charge pump output and VCO input pin. A lowpass filter is connected between this pin and GNDA1.
28	VCOIN2	Data separator PLL charge pump output and VCO input pin. A lowpass filter is connected between this pin and GNDA2.

PIN	NAME	FUNCTION
Power Supplies		
13	VCCD1	2.7V to 5.5V digital supply
29	VCCD2	2.7V to 5.5V digital supply
14	VCCA1	2.7V to 3.6V analog supply for frequency synthesizer. This pin should be left open for 5V operation.
32	VCCA2	2.7V to 3.6V analog supply for data separator. This pin should be left open for 5V operation.
2	VCCA3	2.7V to 3.6V analog supply for miscellaneous functions. This pin should be left open for 5V operation.
25	GNDD1	Digital Ground
8	GNDD2	Digital Ground
16	GNDA1	Analog ground for frequency synthesizer
31	GNDA2	Analog ground for data separator
1	GNDA3	Analog ground for miscellaneous functions

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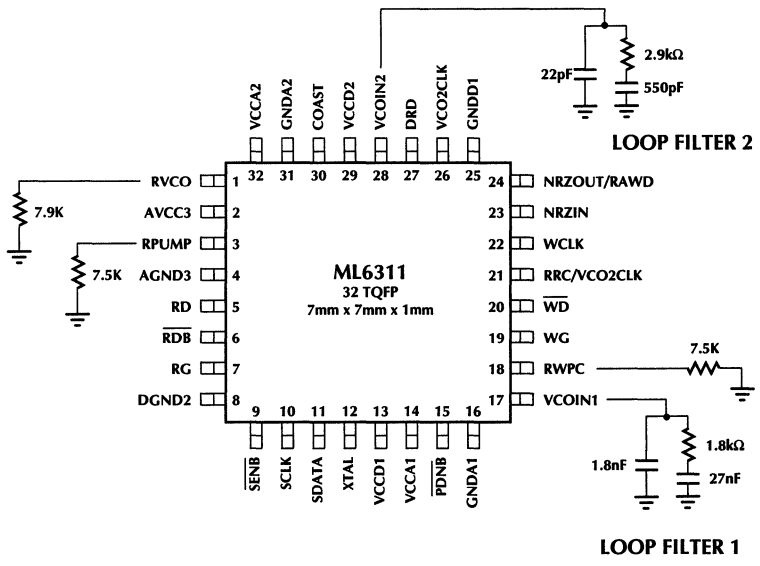
TYPICAL EXTERNAL COMPONENTS



ASSUMPTIONS

$T_S = 1\mu s$ @ $F_{VCO} = 48MHz$

Change pump current = 3X

$K_O = 2400A/S/V$

$\theta_{e,f} = 15\% \theta_{e,i}$

$\xi = 0.95$, $\omega_n T = 1.2$

ASSUMPTIONS

$F_{XTAL} = 20MHz$

$N + 1 = 20$, $M + 1 + 48$

$K_O = 800A/S/V$

$T_S = 200\mu s$

$\omega_n T = 5$

$\theta_{e,f} = 1\%$ of $\theta_{e,i}$

$\xi = 0.6$

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (VCCA & VCCD) ..... –0.3 to +7V
Analog & Digital Inputs/Outputs ..... –0.3 to VCCA + 0.3V
Input Current per Pin ..... –25 to +25mA
Storage Temperature ..... –65 to +150°C
Maximum Junction Temperature ..... 125°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage Range ..... 2.7V to 3.6V or 4.5V to 5.5V
For 5V Operation ..... VCCA is left open, VCCD is at 5V
For 3V Operation ..... VCCA and VCCD are tied to 3V
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VCCA = VCCD = 2.7 to 3.6 volts or 4.5 to 5.5 volts and T_A = 0 to 70°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Dissipation					
Analog Vcc (VCCA)	Left open for 5V operation	2.7		3.6	V
Digital Vcc (VCCD)	Connected for both 3V & 5V	2.7		5.5	V
Analog Supply Current	VCCA = 3.6V, Data Rate = 32 Mbps				
Normal Mode	All circuits operational		37	40	mA
Read Mode	Encoder & WPrecomp OFF		36	39	mA
Write Mode	Data separator and decoder OFF		15	17	mA
PLLFS Mode	Data separator, endec, WPrecomp OFF		14	16	mA
Idle Mode	Only bias circuits & serial interface ON		5	5.5	mA
Sleep Mode	All circuits OFF, register contents retained			10	µA
Digital Supply Current	VCCD = 3.6V, Data Rate = 32 Mbps, C_L < 15pF				
Normal Mode	All circuits operational		16	20	mA
Read Mode	Encoder & WPrecomp OFF		16	20	mA
Write Mode	Data separator and decoder OFF		15	20	mA
PLLFS Mode	Data separator, endec, WPrecomp OFF		9	11	mA
Idle Mode	Only bias circuits & serial interface ON		1.5	2	mA
Sleep Mode	All circuits OFF, register contents retained			10	µA
Digital Supply Current	VCCA = open, VCCD = 4.5V to 5.5V, Data Rate = 32 Mbps, C_L < 15pF				
Normal Mode	All circuits operational			60	mA
Read Mode	Encoder & WPrecomp OFF			59	mA
Write Mode	Data separator and decoder OFF			37	mA
PLLFS Mode	Data separator, endec, WPrecomp OFF			27	mA
Idle Mode	Only bias circuits & serial interface ON			7.5	mA
Sleep Mode	All circuits OFF, register contents retained			20	µA
Digital I/O Specifications					
High level input voltage		VCCD – 0.5		VCCD	V
Low level input voltage		GNDD		0.5	V
High level input current	V_{IN} = VCC			0.1	µA
Low level input current	V_{IN} = GND			0.1	µA
High level output voltage	$\|I_{OUT}\|$ = 2mA	VCCD – 0.5		VCCD	V
Low level output voltage	$\|I_{OUT}\|$ = 2mA			0.4	V
High impedance output current	@ V_{IN} = 100mV & VCC – 100mV	–0.5		0.5	µA

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics					
Differential Input voltage swing	On ECL input pins RD & RDB	0.8		1.6	V_{P-P}
Psuedo ECL low level output voltage	@ I_{OUT} = 3 mA DRD & VCO2CLK pins	VCCA – 2.05		VCCA – 1.45	V
Psuedo ECL high level output voltage	@ I_{OUT} = 3 mA DRD & VCO2CLK pins	VCC – 1.7		VCC – 1.3	V
Psuedo ECL output swing		0.15	0.25	0.35	V
Low level input current (Psuedo ECL)	Diff V_{IN} = 0V & VCC – 0.7V (RD & RDB inputs)	0.8	1.0	1.3	mA
High level input current (Psuedo ECL)	Diff V_{IN} = VCC – 0.7V & 0V (RD & RDB inputs)	0.8	1.0	1.3	mA
$V_{RD/RDB}$ common mode	Note 1		VCCA – V_{BE}		V
RPUMP bias voltage	RPUMP = 7.5 Kohms (1%)		0.75		V
RWPC bias voltage	RWPC = 15 Kohms (1%) RWPC = 7.87 Kohms (1%)	1.25 0.63	1.5 0.78	1.75 0.92	V V
RVCO resistor	7.87KΩ (1%) recommended	0.6	0.78	0.9	KΩ
Frequency Synthesizer					
Xtal or input frequency	Parallel resonant type with minimum capacitance loading	5		20	MHz
M divider register		1		127	Decimal
N divider register		1		127	Decimal
VCO center frequency dynamic range (f_O)	Measure f_H @ VCOIN1 = 0.7V Measure f_L @ VCOIN1 = 2.3V Dynamic range = $(f_H - f_L)/f_O$	±17	±20		%
VCO gain	$\omega_O = 2 \times \pi \times f_O$, $K_{VCO} = \pi \times (f_1 - f_2)/100mV$ f_1 @ VCOIN1 @ f_O + 100 mV f_2 @ VCOIN1 @ f_O – 100 mV	0.3	0.35	0.4	rad/s-V
Pump current resistor	for setting pump current		7.5		Kohms
Pump current	@ f_O = 48MHz, $I_O = 0.75V/(2 \times R_{PUMP})$	$0.85I_O$	I_O	$1.15I_O$	µA
Phase detector gain	$Kd = (I_O \times 48MHz) / (2 \times \pi \times f_O)$	0.85Kd	Kd	1.15Kd	A/rad
PLL loop gain	$G_O = 3.6 \times 106 / R_{PUMP}$	$0.75G_O$	G_O	$1.25G_O$	A/s x V
PLLFS jitter	RG active, 5V mode, Note 1 RG active, 3V mode, Note 1		200 120	TBD TBD	ps ps

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ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Read Mode and Data Synchronizer					
VCO center frequency dynamic range (f_O)	Measure f_H @ VCOIN2 = 0.7V Measure f_L @ VCOIN2 = 2.3V Dynamic range = $(f_H - f_L)/f_O$	±17	±20		%
VCO gain	$\omega_O = 2 \times \pi \times f_O$, $K_{VCO} = \pi \times (f_1 - f_2)/100mV$ f_1 @ VCOIN1 @ f_O + 100 mV f_2 @ VCOIN1 @ f_O – 100 mV	0.3	0.35	0.4	rad/s – V
Read mode pump current during preamble	@ f_O = 48 MHz, $I_O = (2 \times 0.75V)/R_{PUMP}$ if CPG bit = 0	$0.64I_O$	$0.75I_O$	$0.86I_O$	µA
Normal pump current	@ f_O = 48 MHz, $I_O = (2 \times 0.75V)/R_{PUMP}$ if CPG bit = 0	$0.21I_O$	$0.25I_O$	$0.29I_O$	A
Phase detector gain	$Kd = (I_O \times 48MHz) / (2 \times \pi \times f_O)$	0.85Kd	Kd	1.15Kd	A/rad
PLL loop gain	$G_O = 2.9 \times 106/R_{PUMP}$ (during preamble)	$0.75G_O$	G_O	$1.25G_O$	A/s x V
VCO ZPS error	(zero phase start)	–0.02T – 2		+0.02T + 2	ns
1/3 cell delay accuracy	relative to T/2			±5	%
1/4 cell delay accuracy	relative to T/2, RAW bit = 1 (Reg #6)			±5	%
Decode window centering accuracy				±1	ns
RD input pulse width	t_{WRD}	15		30	ns
RRC duty cycle	WG = 0, RG = 1	40		60	%
PLLDS jitter	Input = 8MHz, sine wave $100mV_{P-P}$, 48MHz encoded clock rate (1 sigma) 5V mode 3V mode		 300 200	 TBD TBD	 ps ps
RRC to NRZout delay	t_{DNRZ1}			5	ns
RG to valid NRZout delay	t_{DNRZ2}		6TRRC		ns
Write Mode and Write Precompensation					
Write precomp accuracy	$t_E = (R_{WPC} \times C \times E/10)$ 0 < E < 7 $t_L = (R_{WPC} \times C \times L/10)$ 0 < L < 7 7.5K < R_{WPC} < 15K & C(int) = 0.67pF	$0.8t_E$ $0.8t_L$		$1.2t_E$ $1.2t_L$	ns ns
WD pulse width	$T = 1/f_O$ t_{WWD}	0.6T		1.4T	ns
RRC duty cycle	WG = 1	40		60	%
WCLK to NRZin Hold time	t_{HNRZ}	5			ns
NRZin to WCLK setup time	t_{SNRZ}	5			ns
Serial Microprocessor Interface					
Serial clock (SCLK) frequency		0.01		20	MHz
SCLK pulse width	t_{PW}	40			ns
SCLK to SDATA hold time	t_{HSD}	10			ns
SDATA to SCLK setup time	t_{SSD}	10			ns
SENB to SCLK setup time	t_{SSEN}	10			ns

Note 1. These parameters are guaranteed by design and verified by characterization only and are not part of the production test program, hence only the typical values are indicated for system designer's reference.

TIMING DIAGRAMS

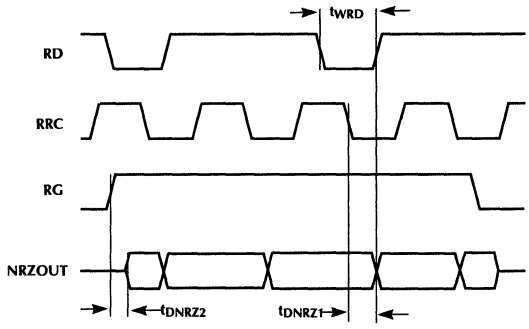


Figure 1. Read Mode Timing

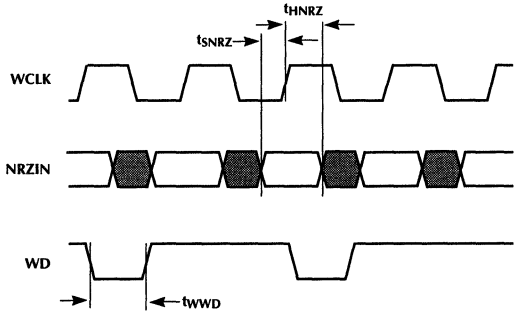


Figure 2. Write Mode Timing

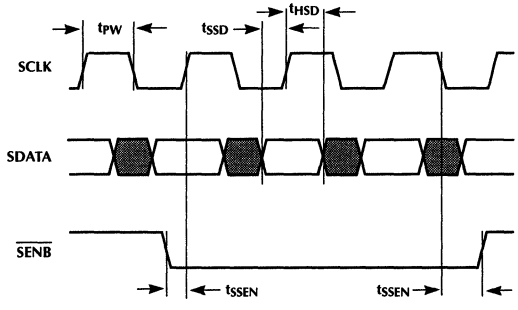


Figure 3. Serial Port Timing

FUNCTIONAL DESCRIPTION

The ML6311 is a BiCMOS Read Channel Back-end Processor IC which is one half of the disk read channel chipset from Micro Linear, intended for the next generation of smaller form factor (1.8" & 1.3") disk drives, operating on 3V and 5V supplies. Fabricated in Micro Linear's BiCMOS process (1.5µ CMOS, 4 GHz ft bipolar), it works in conjunction with the ML6310 Read Channel Front-end Processor to form a complete solution for the low voltage/low power disk read/write channel. It incorporates a full function data synchronizer with a 3:1 operating range, a full function frequency synthesizer with onboard M&N dividers, (1, 7) RLL encoder/decoder and write precompensation circuitry. Bidirectional NRZ I/O can be realized by tying the NRZ Out & NRZ In pins.

The most critical blocks on this chip are the three VCOs, one for the data synchronizer PLL, one for the frequency synthesizer PLL and the third VCO is used to generate the tracking 1/3 cell delay for (1, 7) RLL data synchronization. It also supports a tracking 1/4 cell delay for (2, 7) RLL data synchronization, with an external endec. Careful design considerations have been incorporated to minimize the noise coupling and crosstalk among the VCOs. The highlights of the ML6311 VCO architecture are that it is a fully differential, high speed circuit with built-in switching. It provides a constant amplitude across the frequency span with on-chip timing capacitors. The system noise is highly minimized as the VCO operates at only 1.5X the data rate.

It provides 40-bits for user programmability of a number of features through a serial microprocessor interface and a bank of internal control registers. The control registers come up in an undetermined state on physical power-up and hence need to be initialized, to setup the ML6311 in a known state, on power-up. The control registers will retain their contents in all the power down modes, until power is physically switched off to the chip. The center frequency of the frequency synthesizer VCO is programmed with a 5-bit current DAC. The program information can be provided by the user, or it can be derived from the M & N information. The VCO control current results from the summation of this DAC based coarse control and PLL based fine control. The center frequency of the data separator VCO is programmed by duplicating the control current in the frequency synthesizer VCO as the coarse control. This leaves only the data rate variation to be fine tuned by the PLL, hence implying lower sensitivity and better jitter performance. The VCO3 period is programmed from a 5-bit current DAC, which is in turn referenced to the VCO2 control current. This will vary the 1/2 cycle of VCO3 for the required window centering programmability. Independent early and late write precompensation programmability is provided through a 6-bit decoder array. The external resistor is used to set the time delay for the precompensation.

The ML6311 supports six power down modes for implementation of intelligent power management schemes. An external hardware pin is also provided to implement real time power management. The operating power dissipation is targeted to be less than 170mW, while it will dissipate less than 100µW in the sleep mode. In this mode all sections are powered down except the serial microprocessor interface.

The ML6311 accepts the raw data in a pseudo ECL voltage level, as generated by the ML6310 and provides the synchronized data and clock outputs for the disk controller. Please refer to the block diagram of the ML6311 for the details.

VCO ARCHITECTURE

The most critical circuit blocks in the ML6311 are the three VCOs. The first VCO is used in the frequency synthesizer PLL, the second VCO is used in the data separator PLL and the third VCO is used to generate the tracking 1/3 cell delay for (1, 7) RLL data synchronization or a tracking 1/4 cell delay for (2, 7)RLL data synchronization.

The VCO architecture is optimized to minimize noise coupling from the digital sections of the chip and also the cross talk among the VCOs. The highlights of the VCO architecture are:

- High speed operation with built-in switching mechanism for optimized performance.
- Fully differential circuit configuration to achieve high level of noise immunity.
- On chip timing capacitors to control accuracy and for better noise immunity.
- Constant amplitude across frequency span.
- Symmetrical waveform (~50% duty cycle).

The operating frequency of the VCO is controlled by the tail current of the VCO which consists of two components — a fixed but programmable current (coarse), generated from a DAC which is controlled by the control register #3 and a variable current generated from the PLL. The coarse setting sets the center frequency of the VCO near the operating frequency and the negative feedback around the PLL is used to tune the VCO into the target operating frequency. To minimize the dependence on process and temperature variations the DAC current is derived using an external 1% resistor R_{VCO}. The center frequency is given by the equation:

$$f_O = \frac{m+17}{(16 \times R_{VCO} \times C)}$$

where m = 0 to 31 from control register #3

C = internal capacitor

R_{VCO} = 7.87 kOhms, 1% (recommended)

The architecture of the VCOs is such that they are running at 1.5X the data rate, as opposed to the 3X data rate in the conventional designs used for (1, 7) RLL data streams. This reduces the speed requirements of the circuits and also helps in minimizing crosstalk between the VCOs, thus contributing towards overall system noise immunity. The output of the VCO is sent to a frequency doubler to generate the 3X frequency locally which is then divided

by 2 or 3 to generate the synchronized 1.5X and 1X clocks. Zero phase start of the data separator VCO is supported for initial phase alignment.

PLL ARCHITECTURE

There are two PLLs implemented to realize the data separation (for data and clock recovery) and frequency synthesis function (required to support a zoned bit recording (ZBR) implementation). Shown below is a block diagram of the PLL which requires a first order loop filter.

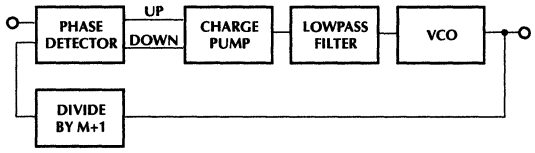


Figure 4. Block Diagram of PLL.

To design the PLL response with a well controlled loop gain value, an external 1% resistor (R_{PUMP}) is used to set the charge pump current according to the bandgap reference voltage generated on chip. The recommended value for Rpump is 7.5kOhms. The capacitor in series with the resistor in the loop filter is chosen so that typically it is 10 times the other capacitor. The resistor is chosen to yield a damping factor between 0.5 and 1 for the acquisition performance of the PLL. The recommended loop filter values are shown in the typical external component diagram.

FREQUENCY SYNTHESIZER PLL

In a ZBR implementation, the disk is divided into a number of zones and the data rate varies from zone to zone. In order to support a ZBR implementation the appropriate frequencies need to be synthesized. VCO1 is used in the ML6311 frequency synthesizer to generate a clock with frequency f_{VCO1}. This is given by the formula:

$$f_{VCO1} = \frac{(M+1) \times f_{XTAL}}{(N+1)}$$

where M and N are 7-bit dividers, programmable through control registers #6, 5, 4. M and N should be at least 1 so that the divide ratio in both the forward and feedback paths are no less than 2, as that 50% duty cycle is guaranteed for the phase compared clocks. In a typical application the users keeps the N at a fixed value and reprograms M from zone to zone to synthesize the required frequency. A 2.5:1 span is required for most applications. The synthesized VCO1 clock is used to derive the encoder clock and the RRC (read/reference clock) for the write operation in ZBR applications. The VCO1 clock is also used to train VCO2 PLL during the non-read mode.

PLL LOOP FILTER DESIGN FOR FREQUENCY SYNTHESIZER

To select the components for the loop filter, two parameters, ξ (damping factor) and ω_n (natural frequency) of the loop characteristic need to be specified.

It is desirable to have the damping factor ξ between 0.5 and 1 to prevent locking to harmonics while maintaining an acceptable lock time. For a high gain, second-order loop this results in minimum noise bandwidth.

The desired natural frequency ω_n of the loop is determined by satisfying the acquisition time (1% maximum phase error after phase acquisition) which is less than the minimum track-to-track seek time. This yields a settling time of approximately $t_S = 5/\omega_n$.

The formulae for the filter components are shown in equations (1) and (2).

$$C_1 = \frac{\frac{K_O}{(M+1)}}{\omega_n^2} \quad (1)$$

$$R = \frac{2\xi\omega_n(M+1)}{K_O} \quad (2)$$

where $K_O = K_D K_{VCO}$ (open loop gain)

The operating frequency F_{VCO} (code rate) is programmed by M&N registers. Equation (3) shows the programming relationship.

$$F_{VCO} = \frac{(M+1)}{(N+1)} F_{XTAL} \quad (3)$$

The value of N should be fixed in the above equation and allow only the M to change for desired operating frequency.

Loop Filter Design Example:

NRZ data rate = 12 to 24 Mbps (1:2 ratio)
Code rate, F_{VCO} = 24 to 48MHz
(assumes (2, 7) RLL code)
F_{XTAL} = 20MHz
Choose N = 19, $\Rightarrow$ M = 23 to 47
$K_D K_{VCO}$ = 800 A/S/V

Let the loop damping factor, ξ = 0.9 at F_{VCO} = 24MHz to allow ξ to drop at higher frequencies. Let ω_n = 50Krad/s (relatively low frequency, in the order of tens Krad/s for better jitter performance). This value produces a loop settling time = 100µs.

from eqn. (3) M + 1 = 24
from eqn. (1) $C_1 = 13.3nF \Rightarrow C_2 = C_1/15 = 880pF$
from eqn. (2) $R = 2.7K\Omega$

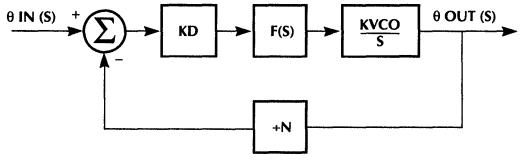
At F_{VCO} = 48MHz, M+1 = 48 which yields ξ = 0.64, and ω_n = 35Krad/s.

DATA SEPARATOR PLL

The center frequency of VCO2 is programmed by duplicating the control current in the VCO1 as the coarse control (control register #3). VCOIN2 thus has to do the fine tuning due to data rate variations (less than several percent), thus implying low sensitivity and good jitter performance. This is an important factor because the data separator PLL has higher bandwidth (of the order of 200KHz) to track the data rate variations and is hence more susceptible to noise induced jitter.

The charge pump has two modes of operation. During the non-read mode, the VCO clock is compared to the frequency synthesizer clock in every cycle, hence the charge pump operates in the low speed mode. After Read Gate is asserted, the charge pump is switched to the high speed mode with (3X CPG = 0) gain and VCO clock is compared to the preamble data on every third clock (assuming 3T preamble pattern for (1, 7) RLL code).

The overall block diagram for the PLL can be described as:



where N = The ratio of the VCO frequency to the input frequency

To select the components for the loop filter, the user needs to consider the following loop requirements:

1. Residual phase error at the end of the preamble should be less than 4% of the total synchronization window (i.e. θ_e < 1ns for F_{VCO} = 48MHz or T_W = 20.8ns). This implies a large loop bandwidth so that it can quickly obtain lock within a predetermined length of the preamble field.
2. The lock-in range $\Delta\omega_L$ must larger than the expected frequency step change due to variations in disk rotational velocity. In today's technology, the disk rotational velocity can be well controlled within ±1%.
3. The natural frequency ω_n and the damp factor ξ of the loop must be minimized to achieve maximum jitter rejection in the data field. The minimum value for the damping factor ξ will be 0.5 for adequate stability.
4. Re-lock time to the reference clock (frequency synthesizer) must be less than the minimum track-to-track seek time.

It is generally valid to assume the minimum value of wn is dominated by the bandwidth needed during preamble from requirement #1. This assumption will be checked in the design example.

The following loop filter design example assumes:

a. (2, 7) RLL code

b. The PLL encounters a phase offset instead of a frequency offset of the incoming data at the initial lock acquisition. The zero phase start function minimizes the initial phase offset to ±(0.2T + 2)ns where T = synchronization window.

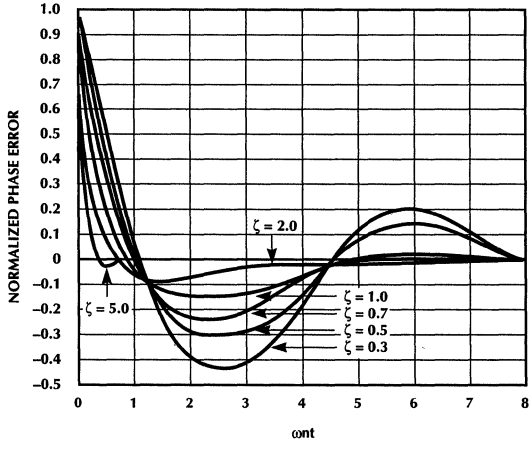


Figure 4. Transient Phase Error $\theta_e(t)$ Due to Step in Phase $\Delta\theta$.

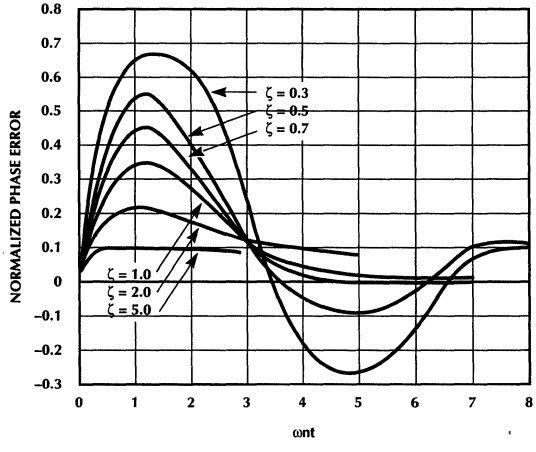


Figure 5. Transient Phase Error $\theta_e(t)$ Due to Step in Frequency $\Delta\omega$.

Since the highest data rate yields the minimum amount of time that the PLL has to settle before decoding data, the settling time is calculated based on the highest data rate.

Loop Filter Design Example:

NRZ data rate = 24MHz
Code rate, F_{VCO} = 48MHz
N_{MIN} = 3 (during preamble, highest recorded frequency)
N_{MAX} = 8 (lowest recorded frequency)
Preamble length = 24 of 3T (100) pattern
TS (settling time of PLL) = 3 x 24 ÷ 48MHz = 1.5µs
Initial phase error $\theta_{e,i}$ = 3ns
Final phase error (after TS) $\theta_{e,f}$ < 20% of $\theta_{e,i}$
K_O = 3200 A/S/V during preamble

It is desirable to have the damping factor ξ between 0.5 and 1 during acquisition. For a high gain, second-order loop this results in minimum noise bandwidth.

Let the loop damping factor ξ = 0.8 to allow ξ to drop at N ≠ 3
As shown in figure 4, with ξ = 0.8, choosing $\omega_n T$ = 2.4 the phase error will be at most 20% of the initial phase error. Since T_S = 1.5µs, ω_n = 1.6Mrad/s.

If the previous assumption is correct, ω_n = 1.6Mrad/s should meet the loop requirements 2 and 4. First, examining requirement #2:

Let the maximum frequency step Δf = ±1% of the preamble frequency
Δf = ± 0.01 x 48MHz ÷ 3 = ±160KHz
Lock-in range is given by
$\Delta\omega_L = 2\xi\omega_n$ = 2 x 0.8 x 1.6Mrad/s = 2.56 Mrad/s

Thu, Δf_L = 407KHz > 160KHz and requirement #2 is met.

User is encouraged to check that ω_n =1.6Mrad/s durnig preamble does meet the requirement #4.

Recall the equations for determining the filter components:

$$C_1 = \frac{\frac{K_O}{N}}{\omega_n^2} \quad (4)$$

$$R = \frac{2\xi\omega_n N}{K_O} \quad (5)$$

from eqn. (4) $C_1 = 417pF \Rightarrow C_2 = C_1/15 = 28pF$
from eqn. (2) $R = 2.4K\Omega$

The above analysis is only shown as an example. The calculated values for filter components are most likely not optimized for all systems using the same data rate, code and preamble.

The coarse center frequency of the frequency synthesizer VCO is programmed with a 5-bit current DAC in conjunction with control register #3. This speeds up the frequency acquisition and also minimizes the VCO sensitivity to V_{VCOIN1} and improves the jitter performance. The synthesized frequency is tuned using the M & N divider information and the crystal frequency, as given by the equation above.

1/3 CELL DELAY & SYNCHRONIZER

The synchronizer circuits align the encoded read data pulses to the data separator VCO clock for the proper decoding of read data. The encoded read data comes in at ECL levels with the timing information embedded in its falling edges. On each rising edge of the encoded read data, the VCO3 is enabled for half of a cycle to generate a DRD (delayed read data) pulse. The falling edges of the DRD pulse enable the phase detector, which operates in phase only mode during read operation, so that the falling edges of the DRD will be phase compared to the rising edges of the VCO2 clock. The falling edges of the DRD are aligned to the rising edges of the VCO2 clock by the negative feedback around the PLL. The rising edges of DRD set the output of the internal data register to a 1, so that the following rising edge of the VCO2 clock will clock it into the synchronizer. After the 1 is clocked into the synchronizer, the internal data register is reset to a 0 and the following VCO2 clocks will clock in 0's to the synchronizer until the data register is set by another read pulse. The VCO3 period is programmed from a 5-bit DAC which is in turn referenced to the VCO2 control current. This will vary the 1/2 cycle of VCO3 for the required window centering programmability (control register #2), while performing a window margin test.

When the RAW bit in control register #6 is set, then this becomes a 1/4 cell delay and the endec is disabled, thus allowing the handling of (2, 7)RLL data. The synchronized data and 2X clock outputs are made available on the NRZOUT and RRC pins.

READ MODE OPERATION OF THE ML6311

When Read Gate (RG) is inactive low, the data separator PLL is locked to the VCO1 clock with the phase detector operating in the phase/frequency mode. The internal multiplexer selects the 1X clock derived from VCO1 clock and outputs it as the RRC (read/reference clock).

When Read Gate (RG) goes active high, the chip enters the read mode. In the read mode the decoder circuits and the NRZOUT signal are enabled. The internal counter starts counting the number of pulses received on the RD/$\overline{\text{RDB}}$ input. After 3 pulses the VCO2 is stopped. VCO2 will restart at the next input transition. The zero phase start circuit eliminates the initial misalignment and speeds up the PLL acquisition. When VCO2 restarts, the phase detector is switched to phase only mode with the input connected to DRD (delayed read data). The phase detector gain is also increased by 3X to ensure that the PLL has enough bandwidth to lock within 16 preamble bytes. After 16 more RD pulses the PLL acquisition is assumed complete. The multiplexer now selects the 1X clock derived from VCO2 clock and outputs it as the RRC (read/reference clock). The decoder then recovers the NRZ data from the RD input and outputs it onto the NRZOUT pin. The data on NRZOUT is clocked out on the falling edges of RRC.

5

The end of the read operation is signalled by Read Gate going inactive low, which then returns the NRZOUT pin to high impedance and also switches the phase detector input to the VCO1 clock with low gain. VCO2 is stopped again and is restarted, synchronized with VCO1. Circuitry is implemented to ensure a glitchless transition of the clock frequencies on the RRC output.

WRITE MODE OPERATION OF THE ML6311 WRITE PRECOMPENSATION CIRCUITRY

When Write Gate (WG) is asserted active high, the chip enters the write mode. During this mode it clocks in the data on the NRZIN input on the rising edges of WCLK and puts out the (1, 7)RLL encoded write data ($\overline{WD}$). The width of the $\overline{WD}$ pulse is made to track the data rate. Write precompensation can be achieved on this write data if desired. Write precompensation can be bypassed by setting the appropriate bit in control register #0. Write precompensation is implemented through a decoder array and the precompensation current is set through an external resistor, R_{WPC}. The recommended values of R_{WPC} are 7.5KOhm or 15KOhm. The early and late shift values are independently programmed through control registers #1 & #0. Table 1 shows the (1, 7) RLL code mapping table used in the ML6311 and Table 2 shows the write precompensation algorithim.

Table 1: (1, 7) RLL Code Mapping table

NRZ DATA				(1, 7) RLL CODE					
X0	X1	X2	X3	Y1	Y2	Y3	Y4	Y5	Y6
0	0	*	*	X	0	1			
0	1	*	*	0	1	0			
1	0	*	*	X	0	0			
1	1	0	0	0	1	0	0	0	1
1	1	0	1	X	0	0	0	0	0
1	1	1	0	X	0	0	0	0	1
1	1	1	1	0	1	0	0	0	0

Note: X is the complement of the previous code bit

Table 2: Write Precompensation Algorithm

BIT	BIT	BIT	BIT	BIT	COMPENSATION
n-1	n-2	n	n+1	n+2	BIT n
1	0	1	0	1	None
0	0	1	0	0	None
1	0	1	0	0	Early
0	0	1	0	1	Late

Late: Bit n is time shited (delayed) from its nominal time position towards the bit n+1 time position.

Early: Bit n is time shited (advanced) from its nominal time position towards the bit n-1 time position.

POWER MANAGEMENT

The ML6311 provides a hardware pin (PDNB) and three bits in control register #7 for seven levels of micro power management control.

1	1	1	CPG	BUF	PM2	PM1	PM0

The major circuit blocks in the ML6311 comprises of the regulator, the serial interface, VCO1 & frequency synthesizer PLL, VCO2 & data separator PLL, VCO3, synchronizer, decoder, encoder, precompensation circuits, bias circuits and I/O circuits. The PDNB pin in conjunction with the 3 bits in control register #7 can be used to selectively turn off a combination of these blocks depending on the mode of operation. This allows the system designer to turn off sections of the chip that are not in use during a particular sequence of events, thus minimizing power dissipation at a micro management level. Table 3 shows these seven different power down modes and the circuit blocks affected in these different modes. Total typical power dissipation has two components — analog power dissipation which is more or less constant and digital power dissipation which varies with operating data rate.

Table 3: Power down modes in the ML6311 with typical power dissipation

POWER DOWN MODE	SLEEP	IDLE	PLLFS	READ	WRITE	NORMAL	PDWN
PDNB pin	high	high	high	high	high	high	low
Bits PM2,PM1,PM0	000	010	011	100	101	110	XXX
VCO1 and PLLFS	off	off	on	on	on	on	off
VCO2 and PLLDS	off	off	off	on	off	on	off
VCO3, Synchronizer and Decoder	off	off	off	on	off	on	off
Encode & WPrecomp	off	off	off	off	on	on	off
Bias and I/O circuits	off	on	on	on	on	on	off
Serial Interface	on	on	on	on	on	on	on
Typical analog power dissipation @ 2.7V	25µW	14mW	40mW	97mW	41mW	100mW	25µW

SERIAL MICROPROCESSOR INTERFACE

The serial microprocessor interface consists of a simple three-wire serial port. Data is shifted serially into the ML6311 on the SDATA line on the falling edges of the serial shift clock, SCLK, provided the $\overline{SENB}$ pin is active (low). The data is shifted in blocks of eight bits with MSBit first. The internal registers are organized in blocks of eight bits, with the three most significant bits denoting the address, followed by the five data bits. This addressing scheme thus allows for a register bank of eight registers. When the chip is physically powered-up, the control registers come up in an undetermined state and hence they need to be initialized to some preset configuration, so that the behavior of the chip is predictable. The control registers retain their programmed information in all the power-down modes, except when the chip is physically powered-down. When the $\overline{SENB}$ pin goes inactive (high), the SDATA and SCLK pins are ignored and the previously shifted information is latched on the rising edge of the $\overline{SENB}$, into the appropriate register bank based on the address bits. It is recommended that the SCLK input be kept inactive low till such time when it is in use. The SCLK input is capable of handling speeds up to 20MHz.

CONTROL REGISTER DEFINITIONS

The control register bank consists of eight registers with addresses from 0 through 7. Outlined below are the detailed bit by bit definitions of the control registers 0 through 7.

CONTROL REGISTER #0

Write Precompensation Late control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	0	0	L2	L1	L0	BYP	REG

BYP = 0 Do not bypass the write precompensation circuitry

BYP = 1 Bypass the write precompensation circuitry

REG = 0 implies regulator is ON (5V Mode)

REG = 1 implies regulator is OFF (3V Mode)

The REG bit applies only in the 3V operating mode, where the regulator should be switched OFF, to minimize power dissipation, as it is not needed. This bit must be set to 0 in the 5V operating mode.

L2	L1	L0	R_{WPC} = 7.5K	R_{WPC} = 15K
0	0	0	0 ns	0 ns
0	0	1	0.5 ns	1.0 ns
0	1	0	1.0 ns	2.0 ns
0	1	1	1.5 ns	3.0 ns
1	0	0	2.0 ns	4.0 ns
1	0	1	2.5 ns	5.0 ns
1	1	0	3.0 ns	6.0 ns
1	1	1	3.5 ns	7.0 ns

CONTROL REGISTER #1

Write Precompensation Early control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	0	1	E2	E1	E0	RSVD	RSVD

RSVD = 1 Reserved, must be programmed as a 1, all the time, to ensure proper operation of the chip.

E2	E1	E0	R_{WPC} = 7.5K	R_{WPC} = 15K
0	0	0	0 ns	0 ns
0	0	1	0.5 ns	1.0 ns
0	1	0	1.0 ns	2.0 ns
0	1	1	1.5 ns	3.0 ns
1	0	0	2.0 ns	4.0 ns
1	0	1	2.5 ns	5.0 ns
1	1	0	3.0 ns	6.0 ns
1	1	1	3.5 ns	7.0 ns

CONTROL REGISTER #2

Data separator PLL window centering control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	1	0	WC4	WC3	WC2	WC1	WC0

WC4	WC3	WC2	WC1	WC0	VALUE
0	0	0	0	0	–24.0 %
0	0	0	0	1	–22.4 %
0	0	0	1	0	–20.8 %
0	0	0	1	1	–19.2 %
0	0	1	0	0	–17.6 %
0	0	1	0	1	–16.0 %
0	0	1	1	0	–14.4 %
0	0	1	1	1	–12.8 %
0	1	0	0	0	–11.2 %
0	1	0	0	1	–9.6 %
0	1	0	1	0	–8.0 %
0	1	0	1	1	–6.4 %
0	1	1	0	0	–4.8 %
0	1	1	0	1	–3.2 %
0	1	1	1	0	–1.6 %
0	1	1	1	1	0 % (center)
1	0	0	0	0	+1.6 %
1	0	0	0	1	+3.2 %
1	0	0	1	0	+4.8 %
1	0	0	1	1	+6.4 %
1	0	1	0	0	+8.0 %
1	0	1	0	1	+9.6 %
1	0	1	1	0	+11.2 %
1	0	1	1	1	+12.8 %
1	1	0	0	0	+14.4 %
1	1	0	0	1	+16.0 %
1	1	0	1	0	+17.6 %
1	1	0	1	1	+19.2 %
1	1	1	0	0	+20.8 %
1	1	1	0	1	+22.4 %
1	1	1	1	0	+24.0 %
1	1	1	1	1	+25.6 %

CONTROL REGISTER #3

VCO Coarse Center Frequency Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	1	1	CF4	CF3	CF2	CF1	CF0

CF4	CF3	CF2	CF1	CF0	F_O MHZ
0	0	0	0	0	17 MHz
0	0	0	0	1	18 MHz
0	0	0	1	0	19 MHz
0	0	0	1	1	20 MHz
0	0	1	0	0	21 MHz
0	0	1	0	1	22 MHz
0	0	1	1	0	23 MHz
0	0	1	1	1	24 MHz
0	1	0	0	0	25 MHz
0	1	0	0	1	26 MHz
0	1	0	1	0	27 MHz
0	1	0	1	1	28 MHz
0	1	1	0	0	29 MHz
0	1	1	0	1	30 MHz
0	1	1	1	0	31 MHz
0	1	1	1	1	31 MHz
1	0	0	0	0	33 MHz
1	0	0	0	1	34 MHz
1	0	0	1	0	35 MHz
1	0	0	1	1	36 MHz
1	0	1	0	0	37 MHz
1	0	1	0	1	38 MHz
1	0	1	1	0	39 MHz
1	0	1	1	1	40 MHz
1	1	0	0	0	41 MHz
1	1	0	0	1	42 MHz
1	1	0	1	0	43 MHz
1	1	0	1	1	44 MHz
1	1	1	0	0	45 MHz
1	1	1	0	1	46 MHz
1	1	1	1	0	47 MHz
1	1	1	1	1	48 MHz

CONTROL REGISTER #4

Divide by N Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	0	0	N6	N5	N4	N3	N2

CONTROL REGISTER #5

Divide by M Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	0	1	M6	M5	M4	M3	M2

CONTROL REGISTER #6

Divide by M & N and endec control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	1	0	RAW	M1	M0	N1	N0

RAW = 0 Onboard (1, 7)RLL endec enabled NRZ data output on NRZOUT and 1X clock output on RRC pins.

RAW = 1 Onboard (1, 7) RLL endec is disabled. Encoded synchronized data on NRZOUT pin and VCO clock output (2X clock) is available on the RRC pin for (2, 7)RLL code.

M & N are given by :

$$M = M6 \times 2^6 + M5 \times 2^5 + M4 \times 2^4 + M3 \times 2^3 + M2 \times 2^2 + M1 \times 2^1 + 1$$

or

$$M = 64 \times M6 + 32 \times M5 + 16 \times M4 + 8 \times M3 + 4 \times M2 + 2 \times M1 + 1$$

and

$$N = N6 \times 2^6 + N5 \times 2^5 + N4 \times 2^4 + N3 \times 2^3 + N2 \times 2^2 + N1 \times 2^1 + 1$$

or

$$N = 64 \times N6 + 32 \times N5 + 16 \times N4 + 8 \times N3 + 4 \times N2 + 2 \times N1 + 1$$

Note: The 7-bit M & N values are updated (latched) internally only when the most significant bit (M6 or N6) is written to, irrespective of changes in any other bits.

CONTROL REGISTER #7

Power Down Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	1	1	CPG	BUF	PM2	PM1	PM0

BUF = 1 This bit enables the ECL output buffers so that the test signals DRD and VCO2CLK are made available to the user.

BUF = 0 This disables the ECL output buffer. The two pins (ECL output buffer) must be left open for zero power consumption.

CPG = 0 Implies PLLDS Charge Pump Gain is 1X in training mode and 3X in the read mode.

CPG = 1 Implies PLLDS (Data Separator) Charge Pump Gain is 2X in training mode and 4X in the read mode.

Bit configuration for power down modes

PDNB	PM2	PM1	PM0	MODE
1	0	0	0	SLEEP
1	0	0	1	Reserved
1	0	1	0	IDLE
1	0	1	1	PLLFS
1	1	0	0	READ
1	1	0	1	WRITE
1	1	1	0	NORMAL
1	1	1	1	Reserved
0	X	X	X	PDOWN

Note: PDOWN dissipation is the same as SLEEP mode

5

ORDERING INFORMATION

PART NUMBER	VCC RANGE	TEMPERATURE RANGE	PACKAGE
ML6311 CH2	2.7V to 3.3V	0°C to 70°C	32-pin TQFP (H32)
ML6311 CH3	3.0V to 3.6	0°C to 70°C	32-pin TQFP (H32)
ML6311 CH5	4.5V to 5.5V	0°C to 70°C	32-pin TQFP (H32)

ML6320

3V/5V 4-Channel Thin-Film Read/Write Circuit

GENERAL DESCRIPTION

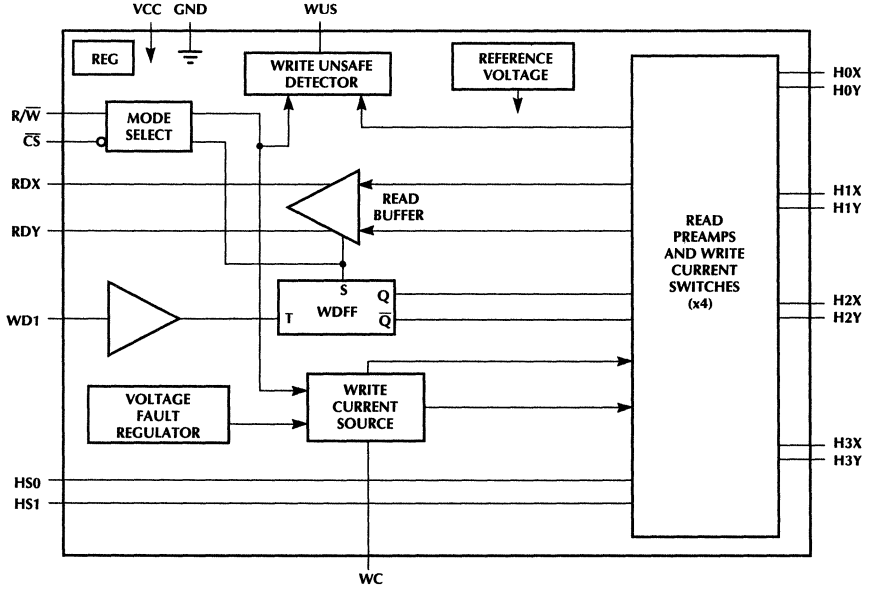
The ML6320 is a BiCMOS monolithic read/write circuit designed for use with two-terminal recording heads, in the next generation disk drives operating on 3V supplies. In addition it can also support a 5V supply, available as a bonding option. They provide a low noise read amplifier, write current control, and data protection circuitry for up to four channels. The ML6320 incorporates internal 400Ω damping resistors which are required for the write operation to the disk. When the device is switched to read mode, the damping resistors are switched out to allow the full signal to be amplified, thus allowing for better noise immunity. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode.

The ML6320CR-3 operates on 2.7V to 3.6V and is available in a 20-pin SSOP package. This is pin compatible with the SSI 32R2300R and VTC VM3200 family of 3V devices. The ML6320CS-5 operates on 4.75V to 5.25V and is available in a 20-pin SOIC package. This is pin compatible with the ML4610R, SSI 32C2020R and VTC VM7200 family of 5V devices.

FEATURES

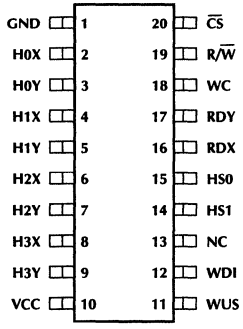
- Operating supply range for the ML6320CR-3 is 2.7V to 3.6V (3V part)
- Operating supply range for the ML6320CS-5 is 4.75V to 5.25V (5V part)
- Low Power Dissipation:
  P_{IDLE} < 3mW,
  P_{READ} < 100mW (Nominal Read) (@ 3.6V)
- Read Mode gain = 250V/V
- Damping resistors switched out in Read mode
- Nominal input noise = 0.6nV/√Hz
- Nominal input capacitance < 15pF typical
- Write Current range = 3–30mA
- Head Inductance range = 0.2 to 5µH
- Enhanced system write to read recovery time
- Power supply fault protection provided
- Supports two terminal thin film heads
- Write Unsafe detection circuitry onboard

BLOCK DIAGRAM



PIN CONNECTION

ML6320
(S20W)



TOP VIEW

PIN DESCRIPTION

NAME	TYPE	FUNCTION
HS0, HS1	I	Head Select: Selects one of four heads
$\overline{CS}$	I	Chip Select: A high inhibits the chip
R/$\overline{W}$	I	Read/Write: A high selects read mode
WUS	O	Write Unsafe: A high indicates an unsafe writing condition
WDI	I	Write Data In: Changes the direction of the current in the head
H0X - H3X H0Y - H3Y	I/O	X,Y Head Connectors

NAME	TYPE	FUNCTION
RDX, RDY	O	X, Y Read Data: Differential read data output
WC		Write Current: Used to set the magnitude of the write current
VCC	I	+3 volt supply (2.7V to 3.6V) — ML6320CR-3
		+5 volt supply (4.75V to 5.25V) — ML6320CS-5
GND	I	Ground

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (V_{CC}) ..... –0.3 to +7VDC
Write Current (I_W) 40mA
Digital Input Voltage (V_{IN}) ..... –0.3 to VCC + 0.3VDC
Head Port Voltage (V_H) ..... –0.3 to VCC + 0.3VDC
Output Current: (RDX, RDY I0) ..... –10mA
Output Current: (WUS) ..... +12mA
Storage Temperature T_{STG} ..... –65 to +150°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage (V_{CC}) ..... 2.7V to 5.25V
Operating Junction Temperature (T_J) ..... +25° to +110°C

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current V_{CC} = 2.7V to 3.6V	Read Mode Write Mode Idle Mode, $\overline{CS}$ and R/$\overline{W}$ = V_{CC}			26 20 + I_W 0.8	mA mA mA
Supply Current V_{CC} = 4.75V to 5.25V	Read Mode Write Mode Idle Mode, $\overline{CS}$ and R/$\overline{W}$ = V_{CC}			26 20 + I_W 1.0	mA mA mA
Power Dissipation V_{CC} = 3.6V	Read Mode Write Mode, I_W = 20mA Idle Mode			93 144 2.9	mW mW mW
Power Dissipation V_{CC} = 5.25V	Read Mode Write Mode, I_W = 20mA Idle Mode			136 210 5.25	mW mW mW
DIGITAL INPUTS					
Input Low Voltage				0.8	VDC
Input High Voltage		2.0			VDC
Input Low Current	V_{IL} = 0.8V	–0.1			mA
Input Low Current, $\overline{CS}$ and R/$\overline{W}$ pins	V_{IL} = 0.8V, V_{CC} = 5.25V	–0.48			mA
Input Low Current, $\overline{CS}$ and R/$\overline{W}$ pins	V_{IL} = 0.8V, V_{CC} = 3.6V	–0.30			mA
Input High Current	V_{IH} = 2.0V			10	µA
WUS Output Low Voltage	I_{OL} = 2 mA max			0.5	VDC
VCC Fault Voltage	I_W < 0.2 mA	2.25	2.45	2.65	VDC
WRITE CHARACTERISTICS					
Write Current Constant "K"		36.8	40	43.2	mA/mA
Write Current Voltage		1.15	1.25	1.35	V
Differential Head Voltage Swing		3.4	6		V_{P-P}
Unselected Head Current				0.6	mA (pk)
Head Differential Load Capacitance				40	pF
Head Differential Load Resistance	R_D	250	350	450	Ω
WDI Transition Frequency	WUS = low	0.75			MHz
Write Current Range (I_W)		3		30	mA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ CHARACTERISTICS CL (RDX,RDY) < 20 pF, RL (RDX, RDY) = 1kΩ					
Differential Voltage Gain	V_{IN} = 1mV_{P-P} @ 1MHz	210	250	285	V/V
Voltage BW –1dB –3dB	|Zsl| < 5Ω, V_{IN} = 1mV_{P-P}	 20 40			 MHz MHz
Input Noise Voltage	BW = 15MHz, L_H = 0, R_H = 0		0.63	0.75	nV/√Hz
Differential Input Capacitance	V_{IN} = 1mV_{P-P}, f = 5MHz			15	pF
Differential Input resistance	V_{IN} = 1mV_{P-P}, f = 5MHz	500			Ω
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5MHz	3			mV_{P-P}
Common Mode Rejection Ratio	V_{IN} = 0 volts DC + 100mV_{P-P} @ 5MHz	45			dB
Power Supply Rejection Ratio	100mV_{P-P} @ 5MHz on V_{CC}	40			dB
Channel Separation	Unselected channels driven with V_{IN} = 0 volts DC + 100mV_{P-P}	45			dB
Output Offset Voltage		–350		+350	mV
Single-Ended Output Resistance	f = 5MHz			40	Ω
Output Current	AC coupled load, RDX to RDY	1.5			mA
Common Mode Output	3V operation	V_{CC} – 1.5	V_{CC} – 1.8	V_{CC} – 2.1	VDC
SWITCHING CHARACTERISTICS I_W = 20mA, R_H = 30Ω, L_H = 1µH, f_{DATA} = 5MHz					
Read to Write	R/$\overline{W}$ to 90% of write current		0.6	1.0	µs
Write to Read	R/$\overline{W}$ to 90% of 100mV Read signal envelope		0.5	1.0	µs
Unselect to Select	$\overline{CS}$ to 90% of write current or 90% of 100mV, 10MHz		0.6	1.0	µs
Select to Unselect	$\overline{CS}$ to 10% of write current		0.4	1.0	µs
HS0-1 to any head	To 90% of 100mV 10MHz Read signal envelope		0.2	1.0	µs
WUS Safe to Unsafe (TD1) Unsafe to Safe (TD2)		 0.6	 2.0 0.2	 3.6 1.0	 µs µs
Head Current: WDI to Ix - Iy (TD3) Asymmetry Rise/Fall Time	L_H = 0, R_H = 0 From 50% points WDI has 1ns rise/fall time 10% to 90% points			 32 1.0 12	 ns ns ns

5

TIMING DIAGRAM

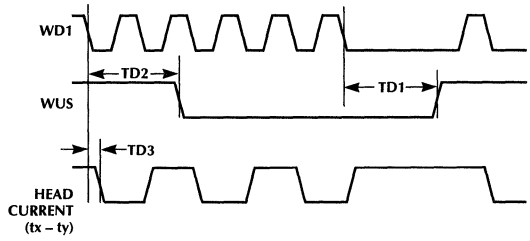


Figure 1. Write Mode.

MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

HEAD SELECT

HS1	HS0	HEAD
0	0	0
0	1	1
1	0	2
1	1	3

FUNCTIONAL DESCRIPTION

The ML6320 has the ability to address up to 4 two-terminal thin-film heads and provide write drive or read amplification. Head selection and mode control are described in the tables below. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0 and HS1 have internal pull-downs. Internal clamp circuitry will protect the ML6320 from a head short to ground condition in any mode. The damping resistors are switched out during read mode, as identified by the R/$\overline{W}$ pin.

WRITE MODE OPERATION

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the ML6320 as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). A preceding read or idle mode select initializes the Write Data Flip-Flop to pass write current through the "X" side of the head. The current calculations are shown below:

Write current (peak) is given by:

$$I_W = \frac{K \times VWC}{RWC}$$

where

RWC is connected from pin WC to GND

Actual head current is given by:

$$I_{X,Y} = \frac{I_W}{1+\frac{R_H}{R_D}}$$

where

R_H = head + external wire resistance

R_D = damping resistance

In the write mode a 400Ω damping resistor is switched in across the Hx, Hy ports.

VOLTAGE FAULT DETECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power start-up, regardless of mode. The Write Unsafe (WUS) open collector output goes high under any of the conditions given below. After the fault condition is removed, two negative transitions on WDI are required to clear WUS.

— Write Data Input frequency too low

— Device in Read or Idle Mode

— No write current

— Chip is disabled or head is open

To ensure proper operation in detecting a head open condition, it is recommended that the product of $I_W \times R_{Dmin}$ should be greater than 2.4V, or in other words:

$$I_W \approx \frac{2.4V}{250\Omega} \cong 10mA$$

READ MODE OPERATION

The Read mode configures the ML6320 as a low noise differential amplifier and deactivates the write current generator. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs. In the Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/$\overline{W}$ applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. The write current source is also deactivated for both the Read and Idle mode. In addition the ML6320 supports the feature by which the internal damping resistors are switched out in the read mode, which allows the full signal to be amplified.

IDLE MODE OPERATION

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum, less than 2mW.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6320CR-3	0°C to +70°C	20-Pin SSOP (R20)
ML6320CS-5	0°C to +70°C	20-Pin SOIC (S20W)

5

Micro Linear

ML8464B, ML8464C

Pulse Detector

GENERAL DESCRIPTION

The ML8464 is a Pulse Detector designed for use in magnetic disk applications to detect the amplitude peaks on the output of the read/write amplifier. These signal peaks are caused by flux reversal on the disk media, which when connected to the read/write amplifier result in an output consisting of a series of pulses of alternating polarity. The relative time position of these signal peaks is indicated by the leading edge of the TTL output pulses. The Pulse Detector accurately represents the time position of these peaks.

The ML8464 contains three major blocks. The amplifier block contains a wide bandwidth differential amplifier with Automatic Gain Control (AGC) and a precision full wave rectifier. The time channel block includes a programmable differentiator followed by a bidirectional one shot multivibrator. The gate channel block includes a differential comparator with programmable hysteresis, a D flip-flop and an output bi-directional one shot multivibrator. The ML8464C internally connects the time channel output to the D flip-flop.

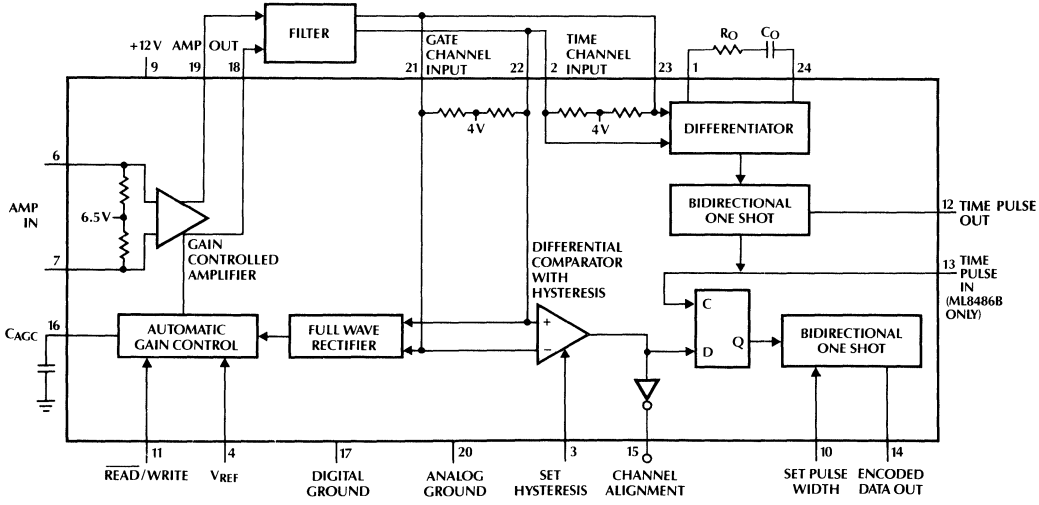
FEATURES

- Wide differential input signal range 20–660 mV_{P-P}
- TTL compatible digital Inputs and Output
- Externally gain controlled input differential amplifier
- Variable hysteresis comparator with gating circuitry
- Differentiator with externally programmable time constants
- Standard 12V power requirement
- Available in 24-pin DIP package, or a 28-pin surface mount PCC
- Improved pulse pairing (±1 ns max.)
- Handles RLL (1, 7) or (2, 7) data to 24 MB/s

ML8464B FEATURES

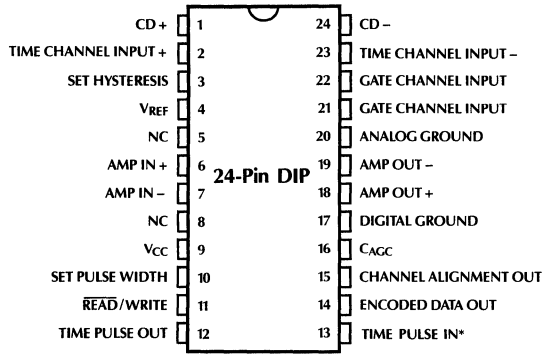
- Direct replacement for DP8464B

BLOCK DIAGRAM

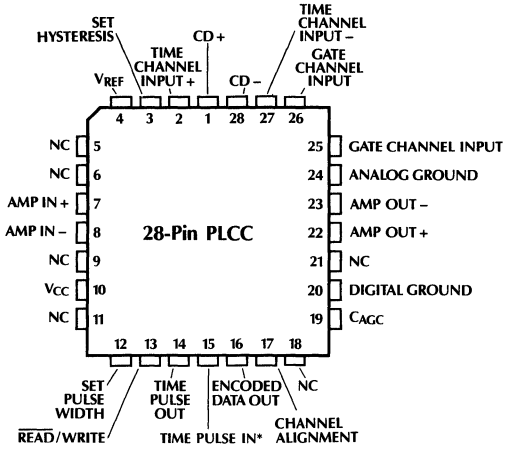


* ML8464C ONLY

PIN CONNECTIONS



NC = No Connect
* THIS PIN IS A NO CONNECT ON THE ML8464C.



PIN DESCRIPTION

NAME	FUNCTION
Amp In+, Amp In–	Differential inputs to the Amplifier. The output of the read/write head amplifier should be capacitively coupled to these pins.
Amp Out+, Amp Out–	Differential outputs of the Amplifier. These outputs should be capacitively coupled to the gating channel filter and to the time channel filter.
Gate Channel Inputs	Differential inputs to the AGC block and the gating channel. Must be capacitively coupled from the Amp Out.
Time Channel Input+, Time Channel Input–	Differential inputs to the time channel differentiator. A filter is required between these pins and Amp Out pins to band limit the noise and to correct for any phase distortion due to read circuitry. Also inputs must be capacitively coupled to prevent disturbing the DC input level.
CD+, CD–	External differentiator network is connected between these two pins.
Set Hysteresis	DC voltage on this pin sets the amount of hysteresis on the differential comparator.
V_{REF}	AGC circuit adjusts the gain of the amplifier to make the differential peak to peak voltage on the Gate Channel. Input is four times the DC voltage on this pin.
C_{AGC}	External capacitor between this pin and Analog ground is connected for the AGC.

NAME	FUNCTION
Set Pulse Width	External capacitor between this pin and Digital ground is connected to control the pulse width of the Encoded Data Out.
$\overline{\text{Read}}$/Write	TTL input. When low, the chip is in read mode and active. When High, the chip is forced into stand by mode.
Channel Alignment	Buffered output of the differential comparator with hysteresis. This output is TTL on the ML8464B, and is open emitter on ML8464C. The ML8464C is specified with a 2KΩ pull-down resistor to ground.
Time Pulse In (ML8464B only)	This is the TTL input to the clock of the D flip-flop. Usually it is connected to the Time Pulse Out pin.
Time Pulse Out	ML8464B: This is the TTL output from the bidirectional one shot following the differentiator. Usually it is connected to the Time Pulse In pin. ML8464C: Open emitter-follower test point.
Encoded Data Out	TTL output. Leading edge of this pin indicates the time position of the peaks.
V_{CC}	12V power supply.
GND	Digital ground. Digital signals should be referenced to this pin.
AGND	Analog ground. Analog signals should be referenced to this pin.

5

FUNCTIONAL DESCRIPTION

The output from the read/write amplifier is AC coupled to the amp input of the ML8464. The amplifier's output voltage is fed back via an external filter to an internal fullwave rectifier and compared against the external voltage on the V_{REF} pin. The AGC circuit adjusts the gain of the amplifier to make the peak to peak differential voltage on the Gate Channel Input four times the DC voltage on the V_{REF}. Typically the signal on the amp out will be set for $4V_{P-P}$ differential. Since the filter usually has a 6dB loss, the signal on the Gate Channel Input will be $2V_{P-P}$ differential. The user should therefore set 0.5V on V_{REF} which can be done with a simple voltage divider from the +12V supply or other suitable reference.

The peak detection is performed by feeding the output of the amplifier through an external filter to the differentiator. The differentiator output changes state when the input pulse changes direction, generally this will be at the peaks. However, if the signal exhibits shouldering, the differentiator will also respond to noise near the baseline. To avoid this problem, the signal is also fed to a gating channel which is used to define a level either side of the baseline. This gating channel is comprised of a differential comparator with hysteresis and a D flip-flop. The hysteresis for this comparator is externally set via the Set Hysteresis pin. In order to have data out, the input amplitude must first cross the hysteresis level which will change the logic level on the D input of the flip-flop. The peak of the input signal will generate a pulse out of the differentiator and bidirectional one shot. This pulse will clock the new data at the D input through to the output. In this way, when the differentiator is responding to noise at the baseline, the output of the D flip-flop is not changing since the logic level into the D input has not been changed. The comparator circuitry is therefore a gating channel which prevents any noise near the baseline from contaminating the data. The amount of hysteresis is twice the DC voltage on the Set Hysteresis pin. For instance, if the voltage on the Set Hysteresis pin is 0.3V, the differential AC signal across the gate channel input must be larger than 0.6V before the comparator will change states. In this case, the hysteresis is 30% of a 2V peak to peak differential signal at the gate channel input.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	14V
TTL Input Voltage	5.5V
TTL Output Voltage	5.5V
Input Voltage	5.5V
Differential Input Voltage	+3V
θ_{JA} for 24-Pin Plastic DIP (Copper Lead Frame)	60°C/Watt
θ_{JA} for 28-Pin PLCC (Copper Lead Frame)	60°C/Watt
Storage Temperature Range	–65°C to +150°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions of T_A = 0 to 70°C, V_{CC} = 12.0V ± 10%, V_{REF} = 0.5V, Set Hysteresis = 0.3V, Read/Write = 0.8V unless otherwise noted. (All pin numbers refer to DIP package.)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
AMPLIFIER						
Z_{INAI}	Amp In Impedance	0.8	1.0	1.5	kΩ	
A_{VMIN}	Min Voltage Gain			6.0	V/V	AC Output $4V_{P-P}$ Differential
A_{VMAX}	Max Voltage Gain	180			V/V	AC Output $4V_{P-P}$ Differential
V_{CAGC}	Voltage on C_{AGC}	 2.8	4.5 3.4	5.5	V V	A_V = 6.0 A_V = 180
GATE CHANNEL						
Z_{INGCI}	Gate Channel Input Impedance	1.75	2.5	3.25	kΩ	
I_{CAGC^-}	Current that charges C_{AGC}	–1.5	–2.5	–3.5	mA	Pin 16 = 3.9V Pin 21 – Pin 22 = 1.3V
I_{CAGC^+}	Current that discharges C_{AGC}		1	5	µA	Pin 16 = 5.0V Pin 21 – Pin 22 = 0.7V
I_{VREF}	V_{REF} Input Bias Current		–0.01	–100	µA	
V_{THAGC}	AGC Threshold	0.88	1.0	1.12	V	Pin 16 = 4.2V See Note 1
I_{SH}	Set Hysteresis Bias Current		–60	–100	µA	
V_{THSH}	Set Hysteresis Threshold	0.48	0.6	0.72	V	See Note 2
TIME CHANNEL						
Z_{INTC}	Time Channel Input Impedance	3.5	5	6.5	kΩ	
I_{CD}	Current into pins 1 & 24 that discharges C_D	2.1	2.7	3.4	mA	
WRITE MODE						
Z_{INAI}	Amplifier Input Impedance in Write Mode	100		500	Ω	Pin 11 = 2V
I_{CAGC}	Pin 16 Current in Write Mode		1.0	5.0	µA	Pin 11 = 2V Pin 16 = 3.9V Pin 21 – Pin 22 = 1.3V
DIGITAL PINS						
V_{IH}	High Level Input Voltage	2.0			V	ML8464B: Pins 11, 13 ML8464C: Pin 11
V_{IL}	Low Level Input Voltage			0.8	V	
V_I	Input Clamp Voltage			–1.5	V	V_{CC} = 10.8V, I_I = –18mA
I_{IH}	High Level Input Current			20	µA	V_{CC} = 13.2V, V_I = 2.7V
I_I	Input Current at Maximum Input Voltage			1	mA	V_{CC} = 13.2V, V_I = 5.5V
I_{IL}	Low Level Input Current			–200	µA	V_{CC} = 13.2V, V_I = 0.5V
V_{OH}	High Level Output Voltage	2.4			V	V_{CC} = 10.8V, V_{IOH} = –40µA See notes 3, 7
V_{OL}	Low Level Output Voltage			0.5	V	V_{CC} = 10.8V, I_{OL} = 800µA, see note 7
I_{OSC}	Output Short Circuit Current			–100	mA	V_{CC} = 13.2V, V_O = 0V
I_{CC}	Supply Current		54	75	mA	V_{CC} = 13.2V

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions of T_A = 0 to 70°C, V_{CC} = 12.0V ± 10%, V_{REF} = 0.5V, Set Hysteresis = 0.3V, Read/Write = 0.8V unless otherwise noted. (All pin numbers refer to DIP package.)

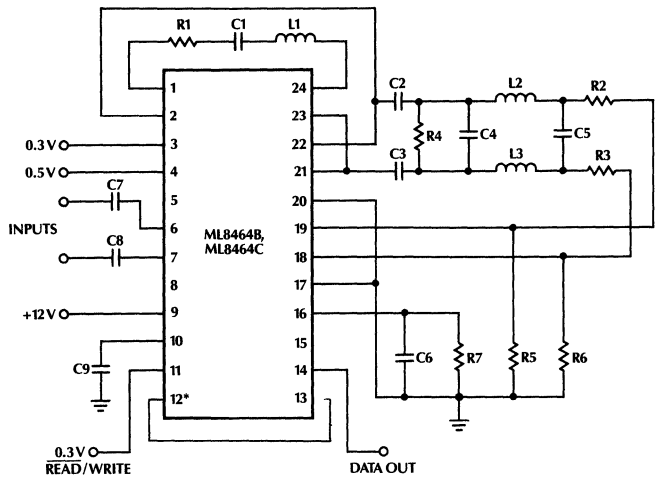
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
DIGITAL PINS (Continued)						
V_{OHCA}	Channel Alignment Pin V_{OH}					(Note 3)
	ML8464B	2.4			V	I_{OH} = –40μA
	ML8464C		7.6		V	10kΩ Load to GND
V_{OLCA}	Channel Alignment Pin V_{OL}					(Note 3)
	ML8464B			0.4	V	I_{OL} = 800μA
	ML8464C		6.9		V	10kΩ Load to GND
V_{OHTP}	Time Pulse Out Pin V_{OH}					
	ML8464B	2.4			V	10kΩ Load to GND
	ML8464C		9.6		V	10kΩ Load to GND
V_{OLTP}	Time Pulse Out Pin V_{OL}					
	ML8464B			0.4	V	10kΩ Load to GND
	ML8464C		8.6		V	10kΩ Load to GND

AC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply range of V_{CC} = 10.8 to 13.2V, T_A = 0 to 70°C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
ML8464-1						
t_{P-P}	Pulse Pairing		±0.5	±1.0	ns	
ML8464-1.5						f = 2.5MHz
t_{P-P}	Pulse Pairing[6]		±0.8	±1.5	ns	V_{IN} = 40mV_{P-P} differential
ML8464-2						See note 4
t_{P-P}	Pulse Pairing		±1.5	±3.0	ns	

Note 1: The AGC threshold is defined as the voltage across the gate channel input when the voltage on C_{AGC} is 4.2V.
Note 2: The Set Hysteresis threshold is defined as the voltage across the gate channel input when the channel alignment output voltage changes state.
Note 3: To prevent inductive coupling from the digital outputs to amplifier inputs, the TTL outputs should not drive more than one ALS TTL load.
Note 4: The filter and differentiator network are described in the pulse pairing set-up.
Note 5: All limits are guaranteed by 100% testing or alternate methods.
Note 6: The 1.5 ns pulse pairing specification is available only on the ML8464C, not the ML8464B.
Note 7: ML8464B: Pins 12, 14, 15
ML8464C: Pins 14 and 15 only.



PULSE PAIRING SET UP

PARTS LIST

R1	220Ω	C1	82pF
R4	680Ω	C2, C3, C6	0.01μF
R2, R3	240Ω	C4	100pF
R5, R6	3.3kΩ	C5	15pF
R7	100kΩ	C7, C8	0.0022μF
L1	1.5μH	C9	47pF
L2, L3	4.7μH		

* The connection between pins 12 and 13 is required only for the ML8464B.

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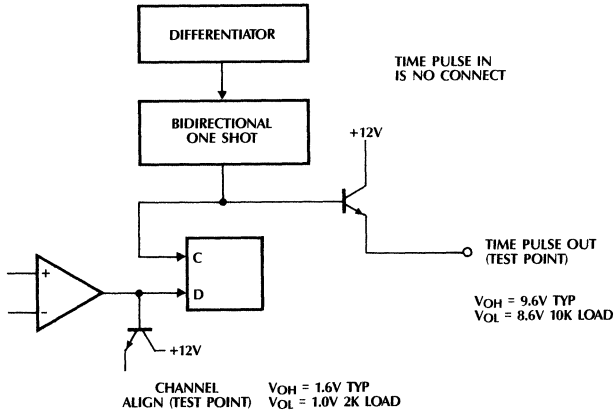
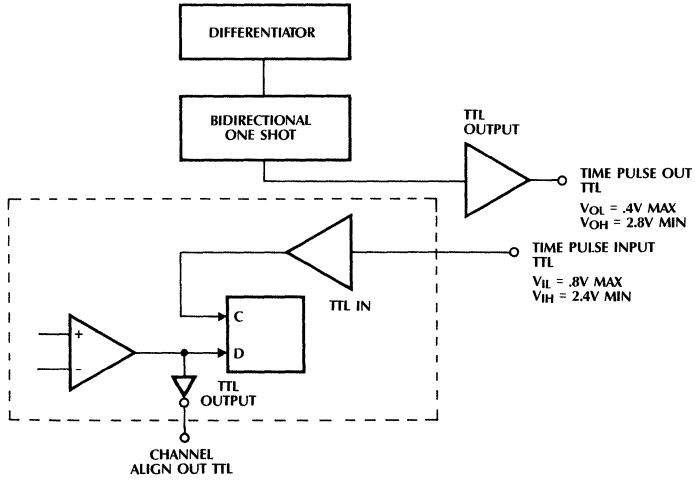
PULSE PAIRING MEASUREMENT

The scope probe is connected to pin 14 (Encoded Data Out) and triggered off of its positive edge. The trigger holdoff is adjusted so that the scope first triggers off the pulse associated with the positive peak and then off the pulse associated with the negative peak. Pulse pairing is displayed on the second pair of pulses on the display. If the second pair of pulses are separated by 6ns, then the pulse pairing for the part is ±3ns.

ML8464C



ML8464B



DIFFERENCES BETWEEN ML8464C AND ML8464B

THE EXTERNAL DELAY

The ML8464B open circuits the digital signal at pins 12 and 13. This allows for the insertion of an external delay filter. The ML8464C has no TTL buffers at these pins and closes the signal path internally bringing out a test point at pin 12. Hence, the ML8464 does not allow for the external delay.

TEST POINTS

The ML8464B has two TTL test points at pins 12 and 15. The ML8464C uses open emitter followers in an ECL configuration. Hence, the voltage levels are not similar at pins 12 and 15 on both devices. The typical voltage level at pins 12 are V_{OH} = 9.6V, V_{OL} = 8.6V and at pin 15 are V_{OH} = 1.6V, V_{OL} = 1.0V.

AGC GAIN CONTROL FACTOR

The AGC reference level is a DC voltage externally set at V_{REF} (pin 4). Increasing this DC voltage will increase the gain of the gain controlled amplifier.

AGC gain control factor =

$$\frac{V_{OUT\ PEAK} = \text{peak of the AGC amp}}{V_{REF}}$$

$$\text{AGC gain control factor} = \frac{2.5V_{PP}}{0.5V_{DC}} = 5 \text{ for ML8464B}$$

$$= \frac{2.0V_{PP}}{0.5V_{DC}} = 4 \text{ for ML8464C}$$

Thus, at V_{REF} = $0.5V_{DC}$, V_{OUT} AGC = 2.5V for ML8464B and 2.0V for ML8464C. This smaller signal amplitude should be taken into consideration at the hysteresis comparator. To set the desired amount of hysteresis, and external DC control voltage is used. The particular settings for V_{REF} and control voltage at pin 3 that optimizes the ML8464B performance may not necessarily optimize the ML8464C performance.

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE	PULSE PAIRING
ML8464C-1CP	0°C to +70°C	MOLDED DIP (P24)	±1 ns
ML8464C-1CQ	0°C to +70°C	MOLDED PCC (Q28)	±1 ns
ML8464C-1.5CP	0°C to +70°C	MOLDED DIP (P24)	±1.5 ns
ML8464C-1.5CQ	0°C to +70°C	MOLDED PCC (Q28)	±1.5 ns
ML8464C-2CP	0°C to +70°C	MOLDED DIP (P24)	±3 ns
ML8464C-2CQ	0°C to +70°C	MOLDED PCC (Q28)	±3 ns
ML8464B-1CP	0°C to +70°C	MOLDED DIP (P24)	±1 ns
ML8464B-1CQ	0°C to +70°C	MOLDED PCC (Q28)	±1 ns
ML8464B-2CP	0°C to +70°C	MOLDED DIP (P24)	±3 ns
ML8464B-2CQ	0°C to +70°C	MOLDED PCC (Q28)	±3 ns

Bus Products

Section 6

Selection Guide

PACMan™ Adaptive Clock Generators

Part Number	No. of Clock Outputs	f_{CLK} Range (MHz)	Maximum Round Trip Delay (ns)	Maximum t_{SKEWR} at the Load (ps)	Clock Source	Package	Feedback Method
ML6500	8	10–80	10	500	Internal or External	44-Pin PLCC	Parallel (2 trace)
ML6508	8	10–80	10	500	External	44-Pin PLCC	Parallel (2 trace)
ML6510	8	10–80 or 10-130	10	500	External	44-Pin PLCC	Series (Single trace)

SCSI Terminators

Part Number	No. of Lines	Disconnect Capacitance (pF)	Package	Features
ML6509	9	<5	16-Pin SOIC 20-Pin TSSOP	Low power mode for laptop internal ternimation Disconnect controlled by hardware or software
ML6599	9	<5	16-Pin SOIC 20-Pin TSSOP	Low insertion current for hot-pluggable applications

High Speed Buffers/Transceivers

Part Number	Function	t_{PLH}, t_{PHL} (ns)	Ground Bounce (mV)	Package	Features
ML65244	Dual Quad Buffer	<1.5	<400	20-Pin SOIC 20-Pin QSOP	TTL compatible Control inputs
ML65245	Octal Transceiver	<1.5	<400	20-Pin SOIC 20-Pin QSOP	TTL compatible Control inputs
ML65541	Octal Buffer	<1.5	<400	20-Pin SOIC 20-Pin QSOP	TTL compatible Control inputs

Programmable Adaptive Clock Manager (PACMan™)

GENERAL DESCRIPTION

The ML6500 (PACMan™) is a Programmable Adaptive Clock Manager which offers an ideal solution for managing high speed synchronous clock distribution in next generation, high speed personal computer and workstation system designs. It provides a PLL clock generator and eight channels of deskew buffers that adaptively compensate for clock skew using a separate feedback trace. Additionally, the ML6500 can also be programmed to be driven by an external clock, thus emulating a SLAVE function, if desired. In the SLAVE mode the ML6500 offers 4X, 2X, 1X and 0.5X clocks, or any ratio realizable between M & N within the maximum frequency limits.

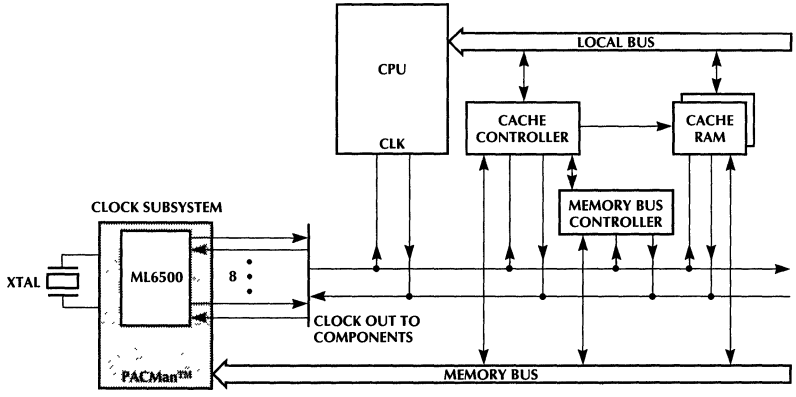
The Programmable clock generator in the PACMan™ is implemented using a low jitter PLL with on-chip loop filter. The PACMan™ deskew buffers adaptively compensate for clock skew on PC boards. An internal skew sense circuit is used to sense the skew caused by the PCB trace and load delays. The sensing is done through a feedback loop from the load and the skew is corrected adaptively via a unique phase control delay circuit to provide low load-to-load skew, at the end of the PCB traces. The chip configuration can be programmed to generate the desired output frequency using the internal ROM or an external serial EEPROM or a standard two-wire serial microprocessor interface. The reference clock can be generated by the internal oscillator (using an external crystal) or it can also be an external clock input.

FEATURES

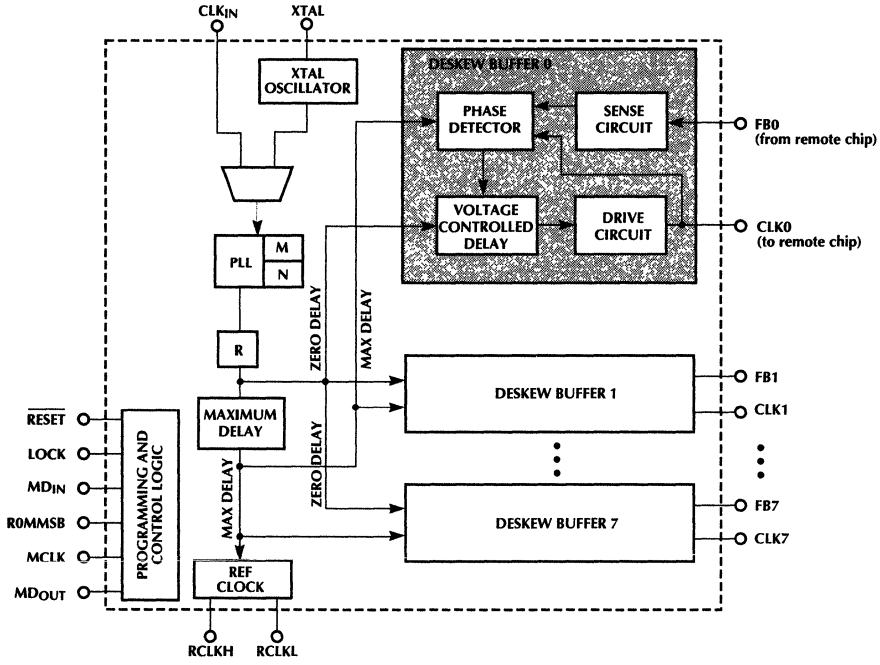
- MASTER mode for clock generation using an on-chip crystal oscillator as a reference
- SLAVE mode for clock generation using a clock input as a reference, providing low input to output clock phase error
- Programmable clock generator PLL with on-chip loop filter and low jitter
- 8 independent, automatically deskewed clock outputs with up to 5ns of on-board deskew range (10ns round trip)
- Controlled edge rate TTL-compatible CMOS clock outputs capable of driving 40Ω PCB traces
- 10 to 80MHz Input and output clock frequency range
- Less than 500ps skew between inputs **at the device loads;** less than 300ps with first order matching
- Frequency multiplication or division
- Lock output indicates PLL and deskew buffer lock
- Test mode operation allows PLL and deskew buffer bypass for board debug
- Supports industry standard processors like Pentium™ Intel80486™ Mips R4000™ SPARC™ 68040™ PowerPC™ Alpha™ etc.

6

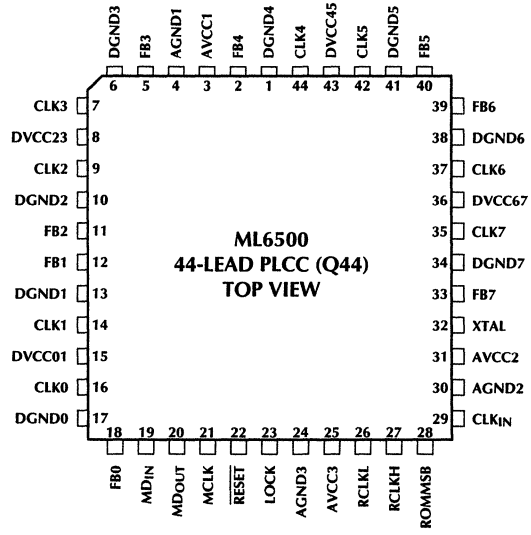
SYSTEM BLOCK DIAGRAM



BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
28	ROMMSB	MSB of the internal ROM address. Tie to GND if not used. See section on Programming the ML6500.
20	MD_{OUT}	Programming pin. See section on Programming the ML6500.
19	MD_{IN}	Programming pin. See section on Programming the ML6500.
21	MCLK	Programming pin. See section on Programming the ML6500.
22	$\overline{RESET}$	Reset all internal circuits. Asserted polarity is low.
23	LOCK	Indicates when the PLL and deskew buffers have locked. Asserted polarity is high.
32	XTAL	Crystal connection for MASTER mode is between this pin and GND. Connect pin to GND if XTAL oscillator is not used.
29	CLK_{IN}	Input reference clock for SLAVE mode. Connect to GND if not used.
16,14,9,7, 44, 42, 37, 35	CLK[0–7]	Clock outputs.
18,12,11,5, 2,40,39,33	FB[0–7]	Clock feedback inputs for the deskew buffers.
3,31 25	AVCC[1–3]	Analog circuitry supply pins, separated from noisy digital supply pins to provide isolation. All supplies are nominally +5V.
4,30,24	AGND[1–3]	Analog circuitry ground pins.
15	DVCC01	Digital supply pin for CLK0 and CLK1 output buffers. Nominally +5V.
8	DVCC23	Digital supply pin for CLK2 and CLK3 output buffers. Nominally +5V.
43	DVCC45	Digital supply pin for CLK4 and CLK5 output buffers. Nominally +5V.
36	DVCC67	Digital supply pin for CLK6 and CLK7 output buffers. Nominally +5V.
17,13,10,6, 1,41,38,34	DGND[0–7]	Digital ground pins for CLK [0–7] output buffers. Each clock output buffer has its own ground pin to avoid crosstalk and ground bounce problems.
26 27	RCLKL RCLKH	Differential reference clock outputs used to minimize part-to-part skew when building clock trees with other PACMan integrated circuits.

ABSOLUTE MAXIMUM RATINGS

VCC Supply Voltage Range ..... –0.3V to 6V
Input Voltage Range ..... –0.3V to VCC
Output Current
  CLK[0–7] 70mA
  All other outputs 10mA
Junction Temperature ..... 150°C
Storage Temperature ..... –65°C to 150°C

ELECTRICAL CHARACTERISTICS

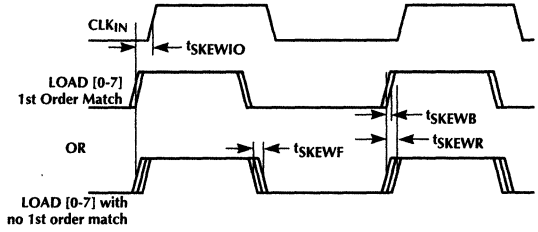
The following specifications apply over the recommended operating conditions of DVCC = AVCC = 5V ± 5% and ambient temperature between 0°C and 70°C. Loading conditions are specified individually.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPY						
IDVCC	Suppy current for each pair of clock outputs	All clock outputs open, f_{CLKX} = 0		50		µA
		C_L = 20pF, Z_O = 50Ω, f_{OUT} = 80MHz		50		mA
IAVCC1	Static supply current, AVCC1 pin			100		mA
IAVCC2	Static supply current, AVCC2 pin			35		mA
IAVCC3	Static supply current, AVCC3 pin			1		mA
LOW FREQUENCY INPUTS AND OUTPUTS (ROMMSB, MD_{OUT}, MD_{IN}, MCLK, $\overline{RESET}$, LOCK)						
V_{IH}	High level input voltage		DVCC – 0.5			V
V_{IL}	Low level input voltage				DGND + 0.5	V
V_{OH}	High level output voltage, MCLK and MDIN	I_{OH} = –100 µA	DVCC – 0.5			V
V_{OL}	Low level output voltage, MCLK and MDIN	I_{OL} = +200 µA			GND + 0.5	V
V_{OH}	High level output voltage, LOCK output	I_{OH} = –100 µA I_{OH} = –10 µA	2.4 DVCC – 0.5			V V
V_{OL}	Low level output voltage, LOCK output	I_{OL} = +1 mA			0.4	V
I_{IN}	Static input current				10	µA
C_{IN}	Input capacitance			5		pF
HIGH FREQUENCY INPUTS AND OUTPUTS (CLK_{IN}, FB [0–7], CLK [0–7])						
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
I_{IH}	High level input current	V_{IH} = 2.4V, MS = 0	–100			µA
I_{IL}	Low level input current	V_{IL} = 0.4V, MS = 0			400	µA
V_{OH}	High level output voltage	I_{OH} = –60mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = +60mA			0.4	V

ELECTRICAL CHARACTERISTICS (Continued)

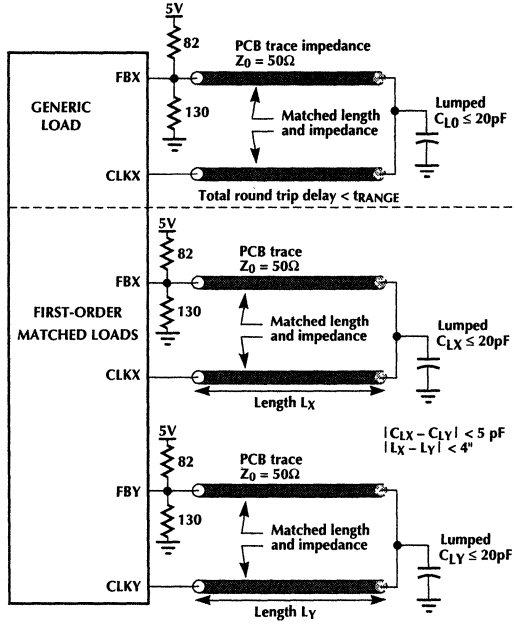
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
AC CHARACTERISTICS rise time, fall time and duty cycle are measured for a generic load; (see Load Conditions section).						
t_R	Rise time, LOAD [0-7] output	0.8 → 2.0V	150		1500	ps
t_F	Fall time, LOAD [0-7] output	2.0 → 0.8V	150		1500	ps
f_{IN}	Input frequency, CLK_{IN} pin		10		80	MHz
f_{OUT}	Output frequency , CLK [0-7] output		10		80	MHz
f_{VCO}	PLL VCO operating frequency		80		160	MHz
f_{XTAL}	Crystal oscillator range		10		20	MHz
DC	Output duty cycle	Measured at device load, at 1.5V	40		60	%
t_{JITTER}	Output jitter	Cycle-to-cycle		75		ps
		Peak-to-peak		150		ps
t_{LOCK}	PLL and deskew lock time	After programming is complete		11		ms
SKEW CHARACTERISTICS All skew measurements are made at the load, at 1.5V threshold each output load can vary independently within the specified range for a generic load (see Load Conditions section).						
t_{SKEWR}	Output-to-output rising edge skew				500	ps
t_{SKEWF}	Output-to-output falling edge skew	Output clock frequency ≥ 50MHz			1.5	ns
t_{SKEWIO}	CLK_{IN} input to any LOAD [0-7] output Maximum rising edge skew	6500 in 1X slave mode, N = M = 0		600		ps
		6500 in slave mode, N ≥ 2, M ≥ 2		1.25		ns
t_{RANGE}	Round trip delay CLKX to FBX pin; output CLK period = t_{CLK}	Output frequency < 50MHz Output frequency ≥ 50MHz	0 0		10 $t_{CLK}/2$	ns
t_{SKEWB}	Output-to-output rising edge skew, between matched loads			250		ps
PROGRAMMING TIMING CHARACTERISTICS						
t_{RESET}	$\overline{RESET}$ assertion pulse width		50			ns
t_{A1}	AUX mode MCLK high time		2000			ns
t_{A2}	AUX mode MCLK low time		2000			ns
t_{A3}	AUX mode MD_{OUT} data hold time		10			ns
t_{A4}	AUX mode MD_{OUT} data setup time		10			ns
t_{A5}	AUX mode MCLK period		5000			ns
t_{M1}	MAIN mode MCLK high time		900			ns
t_{M2}	MAIN mode MCLK low time		900			ns
t_{M3}	MAIN mode MCLK period		1800			ns
t_{M4}	MAIN mode MCLK to MD_{OUT} valid (EEPROM read time)				900	ns

ML6500 configured with M/S = 0 (Slave Mode), (t_{SKEWIO} does not apply for M/S = 1; other skew characteristics are the same):



Note: All skew is measured at the device load input pin, NOT at the ML6500 clock output pin. Skew is always a positive number, regardless of which edge is leading and which is trailing.

AC/SKEW CHARACTERISTICS LOAD CONDITIONS



FUNCTIONAL DESCRIPTION

Micro Linear's ML6500 is the first clock generator chip to use a feedback mechanism to adaptively (on a real time basis), eliminate clock skew in high speed personal computer and workstation system designs. Figure 1 shows a basic configuration of the ML6500 in a system. The skew problem results due to the delaying of clock signals in the system, as shown in Figure 2. Clock skew results from variation in factors like trace length, PCB trace characteristics, load capacitance, parasitic capacitance, temperature and supply variations, etc. Figure 2 shows a representation of the clock skew problem from a timing perspective. It shows a worst case example where the clock signal is delayed so much that its rising edge completely misses the data it is intended to strobe. Using a clock deskew mechanism, this problem can be eliminated and the strobe with the appropriate setup and hold times with respect to the data bus can be generated.

The ML6500 has eight deskew buffers, each with its own independent feedback and error correction circuit. The deskew buffer eliminates skew by using feedback from a remote chip to measure the clock error and then corrects it by generating the appropriate skew to the clock output to compensate. By connecting an external crystal for reference, the onboard low jitter PLL-based clock generator can be used to generate the desired clock output frequency.

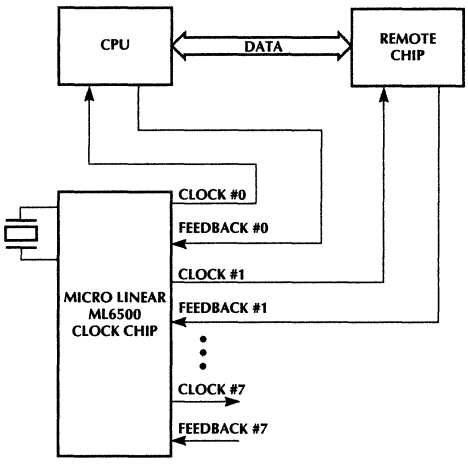


Figure 1. Basic System Configuration Using the ML6500.

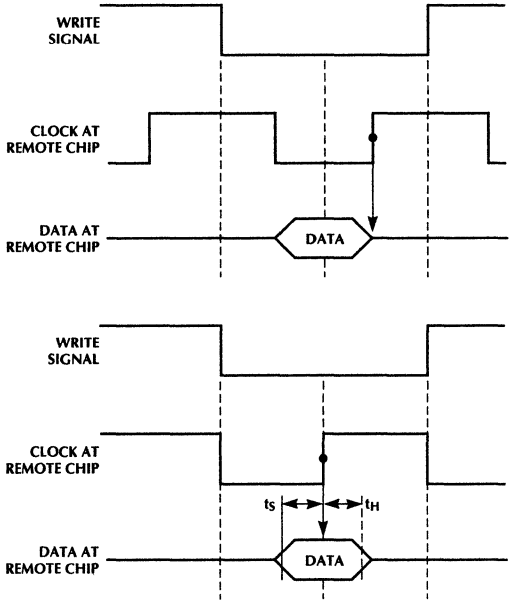


Figure 2. The Skew Problem.

CLOCK GENERATION (MASTER mode) M/S bit = 1

The ML6500 has an integrated clock generator that can be programmed via an external EEPROM, a serial bus, or the on-chip ROM. Shown in Figure 3 is a block diagram of the ML6500 clock generation mechanism. In the MASTER mode (M/S bit set = 1), the full resolution of the PLL frequency synthesizer is available (M register 6 bits, N register 7 bits). The input frequency is defined by the crystal oscillator. The phase relationship between input clock and output clock is not well-defined in the MASTER mode. The VCO frequency is defined by the formula:

$$f_{VCO} = f_{REF} \times \left(\frac{N+1}{M+1}\right)$$

Where F_{REF} is the frequency of the crystal. The VCO frequency must remain in the range 80–160 MHz. The primary output clock is defined by the formula:

$$f_{OUT} = f_{VCO}/2^R$$

R1	R0	INPUT/OUTPUT RANGE
0	0	Not valid: Defaults to R = 01
0	1	40–80 MHz
1	0	20–40 MHz
1	1	10–20 MHz

Note: R implies R1, R0

Example: Using a 14.318 MHz crystal for the input frequency.
Desired output frequency = 66 MHz

Set R = 01 (output range 40–80 MHz)
Set N = 82 (1010010) and M = 8 (001000),
M/S = 1

Then, f_{VCO} = 14.318 x (83/9) = 132.044 MHz
f_{OUT} = 132.044 MHz/2^1 = 66.022 MHz

Eight individually deskewed copies of the clock are provided by the PACMan.

The deskew buffers compensate internally for board-level skew caused by the PCB trace length variations and device load variations. This is accomplished by sensing the round trip delay via the return trace, and then delaying or advancing the clock edge so that all 8 output clocks arrive at their loads in phase. Each of the eight clock lines can have any length PCB trace (up to 5nec each way or 1/4th of the output clock period, whichever is smaller) and the device loads can vary from line to line. The PACMan will automatically compensate for these variations, keeping the device load clocks in phase. (Although PACMan will compensate for skew caused by loading, excessive capacitive loading can cause rise/fall time degradation at the load.) Cascading the ML6500 in slave mode, to the master ML6500 should be done using a deskewed output from master to slave. Alternatively, a ML6508 can be cascaded using the reference clock outputs (RCLKH and RCLKL).

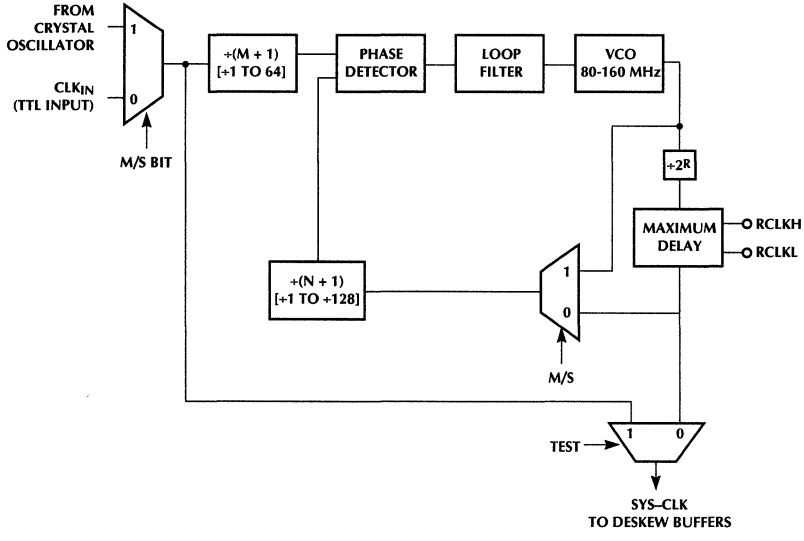


Figure 3. ML6500 Clock Generation Block Diagram.

CLOCK REGENERATION
(ML6500 Slave mode) M/S bit = 0

The ML6500 can also function in a clock regeneration mode (SLAVE mode) to assist in building clock trees or to expand the number of de-skewed clock lines. When the ML6500 functions in the slave mode, it has the ability to do clock multiplication or division as well, while maintaining low skew between the input clock and the device loads. It can generate a 2x or 4x or 0.5x frequency multiplication or division from input to output (e.g. 33 MHz input, 66 MHz output or 66 MHz input, 33 MHz output, etc.). It also can generate a 1x frequency output. To operate the ML6500 in the slave mode, set the M/S bit = 0. Then the VCO frequency is defined by:

$$f_{VCO} = f_{REF} \times \left[\frac{(N+1) \times 2^R}{(M+1)}\right]$$

and the output frequency is still:

$f_{OUT} = f_{VCO}/2^R$ (setting R= 00 defaults to R = 01)

The VCO still must remain in the range 80–160 MHz, and the minimum phase detector input frequency is 625 kHz = (80 MHz/128). Thus the product of (N + 1) and 2^R should be limited to 128:

$(N + 1) \times 2^R \leq 128$ to make sure that the phase detector inputs remain above the minimum frequency.

Example: Generating a 2x clock input frequency = 33 MHz

Set R = 01 (output range 40 – 80 MHz), N = 5 (0000101), M = 2 (000010), M/S = 0

$$f_{VCO} = f_{REF} \times \left[\frac{(N+1) \times 2^R}{(M+1)}\right] = 33MHz \times \left[\frac{6 \times 2^1}{3}\right] = 132MHz$$

$$f_{OUT} = f_{VCO}/2^R = 132\ MHz/2^1 = 66\ MHz$$

Example: Generating a 1x clock Input frequency = 66 MHz

Set R = 01 (output range 40–80 MHz), set M = 0 (000000), N = 0 (0000000), M/S = 0

$$f_{VCO} = 66MHz \times \left[\frac{1 \times 2^1}{1}\right] = 132MHz$$

$$f_{OUT} = f_{VCO}/2^R = 132\ MHz/2^1 = 66\ MHz$$

For doing frequency multiplication and division in slave mode, keep M ≥ 2 and N ≥ 2 for the lowest skew between input clock and output clock.

ADAPTIVE DESKEW BUFFERS

Each copy of the primary clock is driven by an adaptive deskew buffer. The deskew buffer compensates for skew time automatically in accordance to the flight time delay it senses on the feedback line.

Figure 4 shows the simplified functional block diagram of the deskew circuit. The phase of the sense signal and the drive signal is presented to a three-input phase comparator and compared with the reference signal. The phase comparator then controls the voltage controlled delay in the output drive line to match the delay of the fixed reference delay line. Therefore, the sum of the delay of the driver circuit, PCB trace delay, rise time delay at the load and the adjustable delay will always equal the fixed maximum delay.

The sense circuit has an internal level detect such that any skew caused by loading is also accounted for. Since the delay of the circuit is matched for the entire loop, the phase of all the drivers are in close alignment at the inputs of the load.

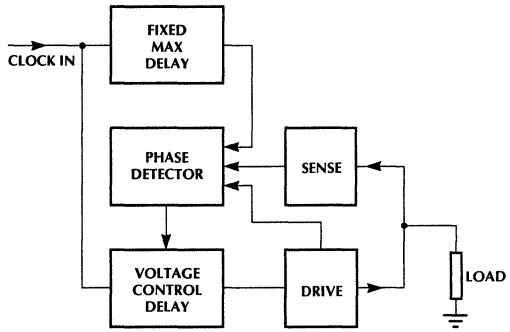
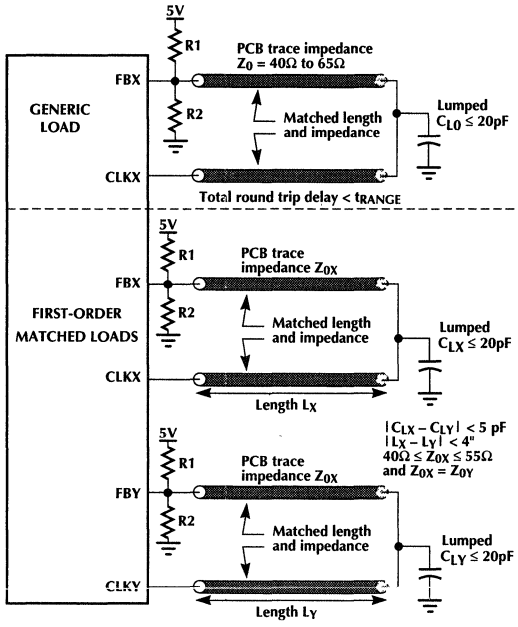


Figure 4. Deskew Circuit Block Diagram.

LOAD CONDITIONS

The ML6500 has been designed to drive the wide range of load conditions that are encountered in a high frequency system. The eight output clock loads can vary individually within a wide range of trace length, impedance and lumped capacitive load, but each load should remain within the designated range for a generic load, to insure the lowest skew and the best signal integrity. The outgoing and return trace should be matched in length and impedance, and the trace should include a termination at the feedback (FB#) pin. All eight output clock traces are generally the same impedance with the same termination resistor values. The clock skew can be further minimized by providing some first order matching between any two loads that require particularly well matched clocks. For the best matching, use adjacent clock outputs with matched loads.



Termination resistors should have a Thevenin voltage of approximately 3V and a Thevenin resistance equal to the impedance of the PCB trace, Z_0:

$$R_1 = \frac{5}{3}(Z_0) \quad \text{then} \quad R_2 = \frac{3}{2}R_1 \quad (\text{for } V_{CC} = 5V)$$

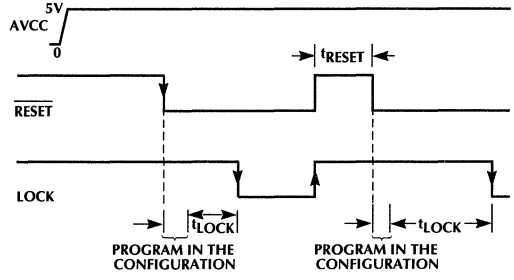
TRACE IMPEDANCE	RECOMMENDED VALUES		MAX. AVG. RESISTOR POWER DISSIPATION W/GENERIC LOAD	
Z0	R1	R2	R1	R2
40Ω	68	100	160 mW	100 mW
50Ω	82	130	150 mW	70 mW
63Ω	110	160	120 mW	70 mW

CRYSTAL OSCILLATOR AND EXTERNAL CLOCKS

If the crystal oscillator is used, the crystal should be placed physically as close as possible to the XTAL and AGND2 pins as possible. No other external components are required. The XTAL pin can also be driven by an external clock signal. There is no well-defined phase difference between input and output clocks in MASTER mode. If a well-defined phase difference is required, the ML6500 should be used in SLAVE mode (M/S = 0), and the CLK_{IN} input used for the external clock (up to 80 MHz).

$\overline{\text{RESET}}$ AND LOCK

When $\overline{\text{RESET}}$ is de-asserted, the internal programming logic will become active and load in the configuration bits (see Programming the ML6500). Once the configuration is loaded, the PLL will lock onto the reference signal, and then the deskew blocks will adapt to the load conditions. When all eight output clocks are stable and deskewed, LOCK will be asserted. The asserted polarity of lock is high. Thus, LOCK can be used to indicate that the system is ready, or it can be used to drive the $\overline{\text{RESET}}$ input of another PACMan in a clock tree.



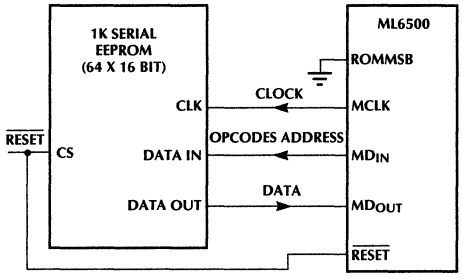
$\overline{\text{RESET}}$ may be reasserted at any time to reset the chip operations. Following a $\overline{\text{RESET}}$ assertion of valid pulse width (see Programming Electrical Characteristics), the ML6500 must again be loaded with a configuration, then it will re-lock and reassert lock when all eight clock outputs are stable and deskewed.

PROGRAMMING THE ML6500

The configuration of the ML6500 is programmed by loading 17 bits into the configuration shift register. To load these bits, the user has 3 options: MAIN, AUX or ROM modes. Which mode is used is determined by the logic level on the MD_{IN} pin when $\overline{RESET}$ is deasserted. If MD_{IN} is tied high, the ML6500 will assume AUX mode; if its tied low, ROM mode. If MD_{IN} is high-impedance (i.e. tied to the input of an EEPROM), it will assume MAIN mode.

1. MAIN Mode

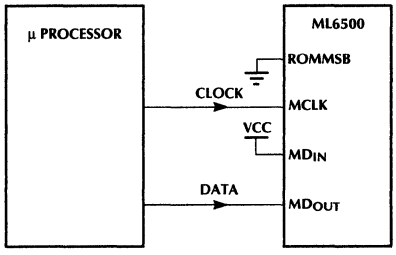
In this mode, the ML6500 will read the 17 configuration bits from an external serial EEPROM, such as the 93C46, using the industry standard 3-wire serial I/O protocol. The serial EEPROM should be a 1K organized in 64 x 16 bits and the PACMan will read the 17 configuration bits out of the two least significant 16-bit words. To use this mode, simply connect the EEPROM serial data input pin to MD_{IN} (ML6500 pin 19), the EEPROM serial data output pin to MD_{OUT} (ML6500 pin 20), and the EEPROM serial data clock pin to MCLK (ML6500 pin 21). After power up, when $\overline{RESET}$ is deasserted, the ML6500 will automatically generate the address and clock to read out the 19 configuration bits. Refer MAIN Mode waveform in Figure 5.



MAIN Mode Configuration.

2. AUX Mode

When MD_{IN} is tied to VCC, programming the PACMan will occur via the AUX Mode. This mode shifts the 17 configuration bits into the shift register directly from the MD_{OUT} pin. The first 17 clock rising edges provided externally on the MCLK pin after $\overline{RESET}$ is deasserted will be used to load the shift register data, which should be provided on the MD_{OUT} pin. See figure 6.



AUX Mode Configuration.

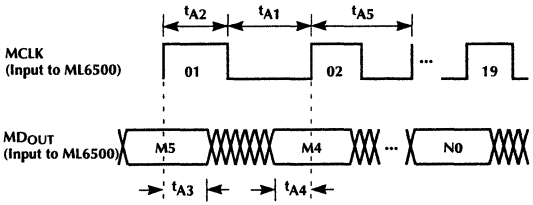


Figure 6. AUX Mode Waveforms

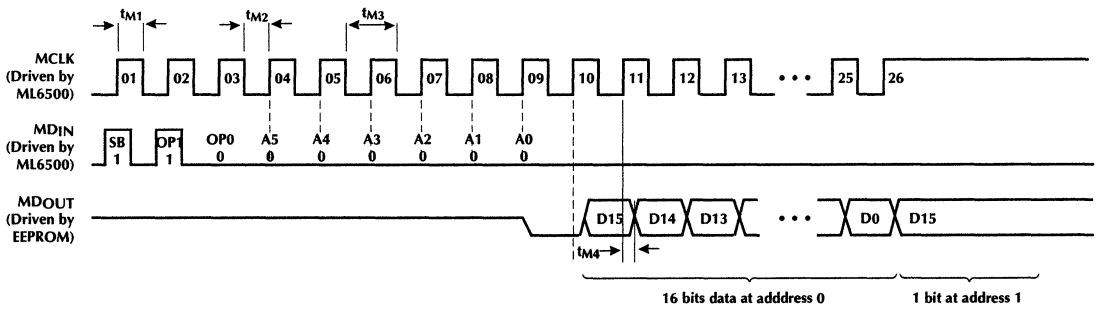
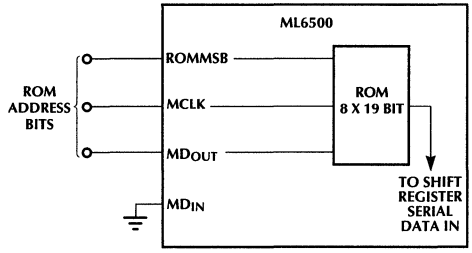


Figure 5. MAIN Mode Waveforms.

3. ROM Mode

When MD_{IN} is tied to GND, programming the PACMan will occur via the ROM Mode. This mode reads the 17 configuration bits directly from an on chip ROM. The selection of one of the eight preset configuration codes is accomplished by means of the pins ROMMSB, MCLK and MD_{OUT} as shown in Table 1. In the table Code 1 is for 1X slave configuration, with output clock in the frequency range of 40-80 MHz. Codes 2-7 assume use of a 14.318 MHz crystal in the master mode to generate some of the common clock frequencies. Code 0 is TEST mode for low frequency testing (PLL is bypassed); the output clocks will follow the CLK_{IN} input.



ROM Mode Configuration.

TABLE 1

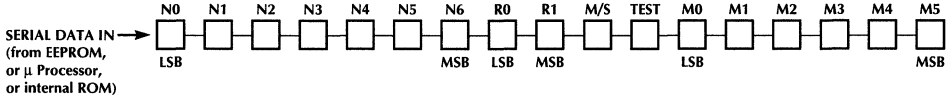
CODE	Selection Bits ROMMSB	MCLK	MD_{OUT}	Input Freq. (MHz)	VCO Freq. (MHz)	Output Freq. (MHz)	Configuration Code M/S	R1, R0	M[1]	N[1]	TEST
0	0	0	0	0–50	—	0–50	0	—	—	—	1
1	0	0	1	40–80	80–160	40–80	0	01	0	0	0
2	0	1	0	14.318	131.73	32.93	1	10	4	45	0
3	0	1	1	14.318	100.23	50.11	1	01	1	13	0
4	1	0	0	14.318	119.91	59.96	1	01	7	66	0
5	1	0	1	14.318	131.73	65.86	1	01	4	45	0
6	1	1	0	14.318	149.32	74.66	1	01	6	72	0
7	1	1	1	14.318	159.88	79.94	1	01	5	66	0

[1]M and N registers are represented in decimal format.

REGISTER DEFINITIONS

BITS	REGISTER	SIZE	FUNCTION
10 – 16	N	7 bit	This register is used to define the ratio for the desired frequency of the primary clock.
8 – 9	R	2 bit	This register defines the frequency of the primary clocks, CLK [0-7].
7	M/S	1 bit	Used to select master/slave operation.
6	TEST	1 bit	If TEST = 1, PLL will be bypassed to allow low frequency testing. Set TEST = 0 for normal operation
0 – 5	M	6 bit	This register is used to define the ratio for the desired frequency of the primary clock.

ML6500 SHIFT REGISTER CHAIN

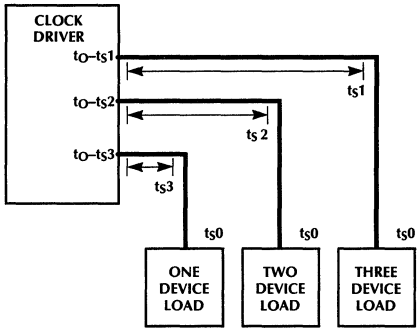


APPLICATIONS

ZERO SKEW CLOCK GENERATION

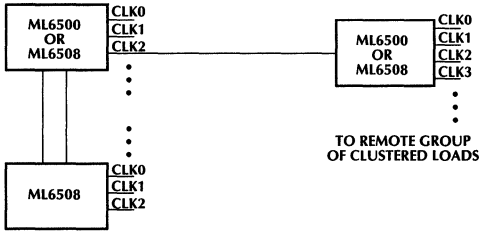
The most advantageous feature of using PACMan is its ability to deliver multiple copies of the clock to the load with very low skew. Because of its unique ability in deskewing, trace length and load consideration are no longer critical in board design and true "zero" deskew can now be realized.

Because of the unique deskewing scheme, neither the trace length nor the device loads need to be equal. This is true for loads, <20pF. Higher loads can be driven if they are placed close to the clock chip, to guarantee signal integrity.



LOW SKEW CLOCK DISTRIBUTION

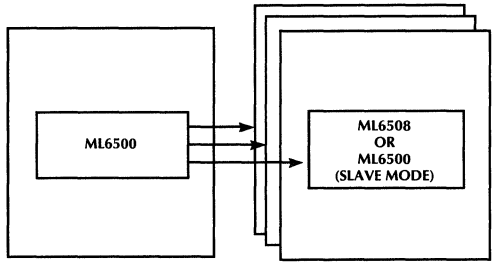
Clock distribution design is usually not a trivial task, especially when multiple clock chips are needed. By using closely grouped PACMans, 16 or more clock lines can be created with low part-to-part skew. Additional groups of clocks can be clustered and driven from de-skewed clock lines, to minimize the number of long-distance clock lines.



BOARD TO BOARD SYNCHRONIZATION

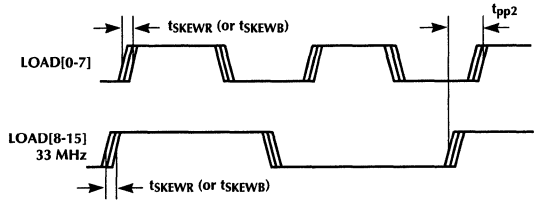
Distribution of the synchronous clock could present significant difficulty at high frequency. With the system clock generated by the ML6500, a zero skew clock delivery to a backplane is now possible. By using the ML6508 slave chip or the ML6500 in slave mode at the receiver end, a near zero delay clock link can be accomplished between the mother board and the satellite boards.

Because the 6500 has frequency doubling capability, a lower frequency signal can be used to route across a back plane.



EXAMPLE CONFIGURATION

Shown in Figure 7 is an example configuration using the ML6500 (Master) and ML6508 (Slave) in tandem to generate eight 66 MHz clocks and eight 33MHz low-skew clocks. This requires only a single crystal and the termination resistors. Configurations are loaded from the internal ROM. PCB traces 0 to 15 are each 50Ω impedance and the load capacitances C_{L0}-C_{L15} are 0 to 20pF each. Outgoing and return trace length for all loads are matched (ie. the load is tapped at the center point of the loop), but no matching is required among separate clock outputs. All traces are shown with a Thevenin termination at the feedback (FB) pin.



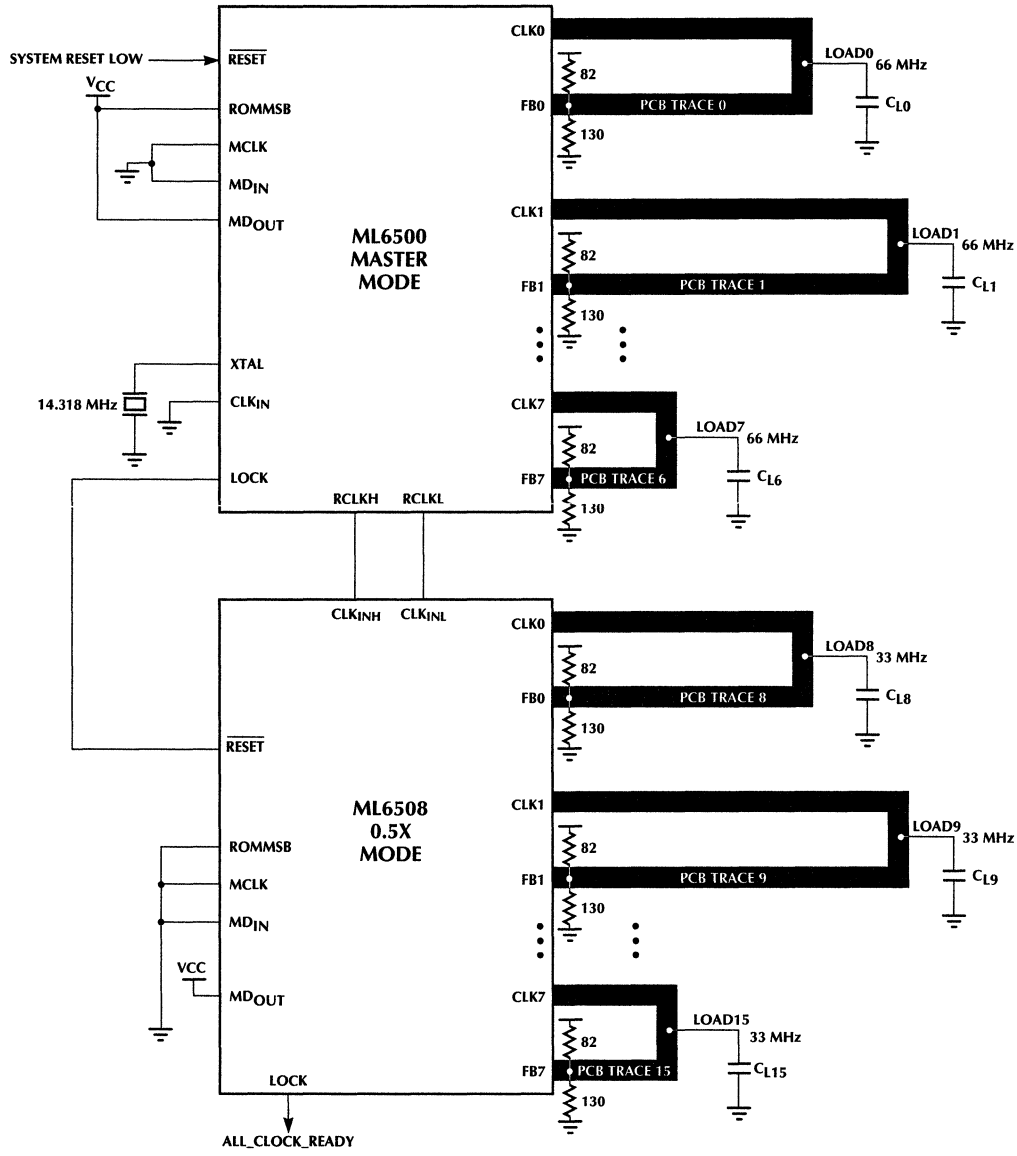


Figure 7. Example use of the ML6500 (Master Mode) in tandem with the ML6500 (Slave Mode) to generate multiple frequency clocks. Master mode ML6500 generates seven 66 MHz clocks while the slave mode ML6500 generates eight 33 MHz clocks.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6500CQ	0°C to +70°C	44-pin PLCC (Q44)

ML6500/08EVAL

Programmable Adaptive Clock Manager (PACMan™) Evaluation Kit

GENERAL DESCRIPTION

The ML6500 and ML6508 are programmable adaptive clock manager masters and slaves capable of automatically adjusting clock skew to within **500ps at the load**. This evaluation kit is designed to exercise the devices with varying PC trace lengths and loading to mimic a "real" system. The board can accommodate either the ML6500 master or the ML6508 slave for evaluation purposes.

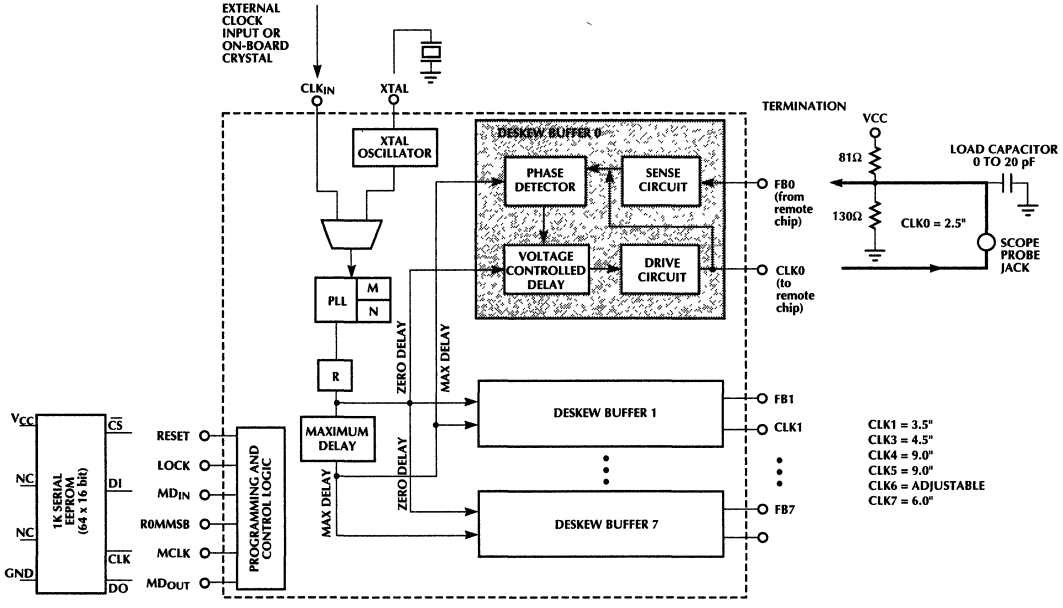
KIT COMPONENTS

- ML6500/08EVAL Users Guide
- ML6500/08 Data Sheet
- Application Note #21
- Gerber file on 3.5" disk
- Complete assembled and tested ML6500EVAL or ML6508EVAL Board

EVAL KIT OPERATION

The EVAL kit is shipped with ML6500 master if the ML6500EVAL is ordered or with the ML6508 slave for the ML6508EVAL. The jumpers are set so that the parts self-program in the "ROM Mode". A 66MHz clock frequency from the on-board 14.318MHz crystal is setup for initial evaluation of the ML6500EVAL. The ML6508EVAL needs an external PECL clock connected to CLK_{INH} and CLK_{INL} for operation. For power, simply provide +5V for V_{CC} into the banana jack marked VCC "+" and Ground connected to GND "–". Ceramic surface mount capacitors in the values of 5 to 20pF are used to emulate a realistic single or multiple IC clock load. There are through hole solder pads for either sockets or capacitors to make it easier to change values. Different clock frequencies from 10 to 80MHz can be chosen by changing the jumper pins.

BLOCK DIAGRAM



The ML6500/08 Evaluation kit. The board can be configured for different clock frequencies and used as a master or slave clock manager.

Programmable Adaptive Clock Manager (PACMan™)

GENERAL DESCRIPTION

The ML6508 is a Programmable Adaptive Clock Manager which offers an ideal solution for managing high speed synchronous clock distribution in next generation, high speed personal computer and workstation system designs. It provides eight channels of deskew buffers that adaptively compensate for clock skew using a separate feedback trace. The input clock can be either TTL or PECL, selected by a bit in the control register. Frequency multiplication or division is possible using the M&N divider ratio, within the maximum frequency limit of 80MHz. 0.5X, 1X, 2X and 4X clocks, or any ratio between M and N can be easily realized.

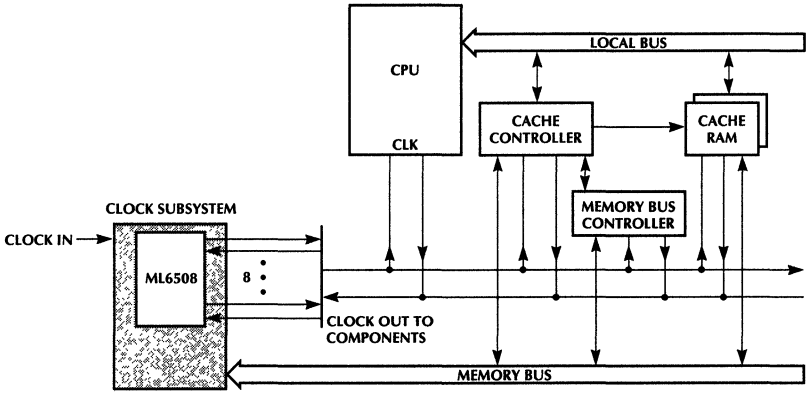
The ML6508 is implemented using a low jitter PLL with on-chip loop filter. The ML6508 deskew buffers adaptively compensate for clock skew on PC boards. An internal skew sense circuit is used to sense the skew caused by the PCB trace and load delays. The sensing is done through a feedback loop from the load and the skew is corrected adaptively via a unique phase control delay circuit to provide low load-to-load skew, at the end of the PCB traces. Additionally, the ML6508 supports PECL reference clock outputs for use in the generation of clock trees with minimal part-to-part skew. The chip configuration can be programmed to generate the desired output frequency using the internal ROM or an external serial EEPROM or a standard two-wire serial microprocessor interface.

FEATURES

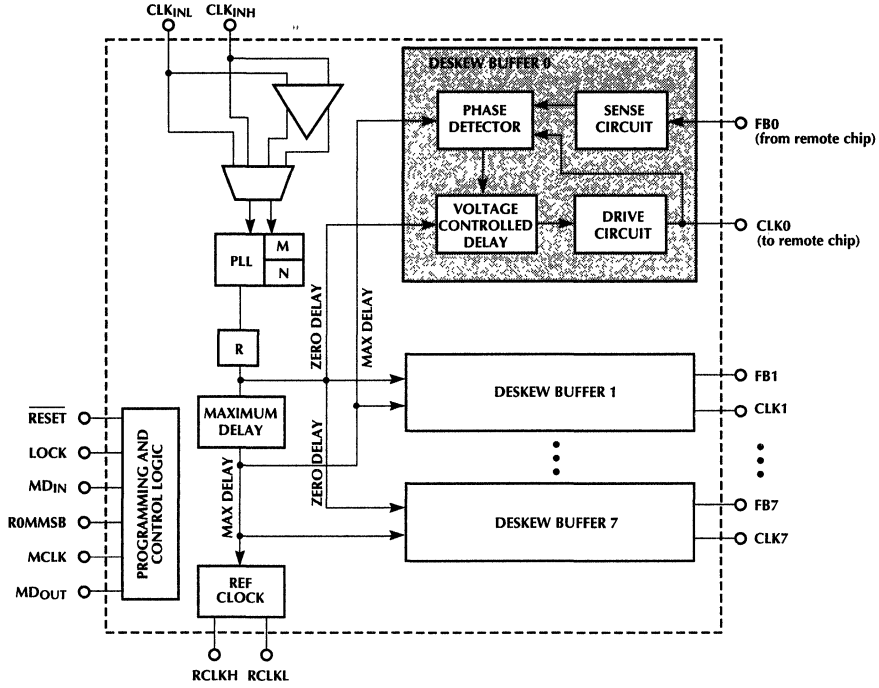
- SLAVE mode for clock generation using a clock input as a reference providing low input to output clock phase error.
- Input clocks can be either TTL or PECL with low input to output clock phase error
- 8 independent, automatically deskewed clock outputs with up to 5ns of on-board deskew range (10ns round trip)
- Controlled edge rate TTL-compatible CMOS clock outputs capable of driving 40Ω PCB traces
- 10 to 80MHz Input and output clock frequency range
- Less than 500ps skew between inputs **at the device loads**; less than 300ps with first-order matching
- Small-swing reference clock outputs for minimizing part-to-part skew
- Frequency multiplication or division
- Lock output indicates PLL and deskew buffer lock
- Test mode operation allows PLL and deskew buffer bypass for board debug
- Supports industry standard processors like Pentium™ Intel80486™ Mips R4000™ SPARC™ 68040™ PowerPC™ Alpha™ etc.

6

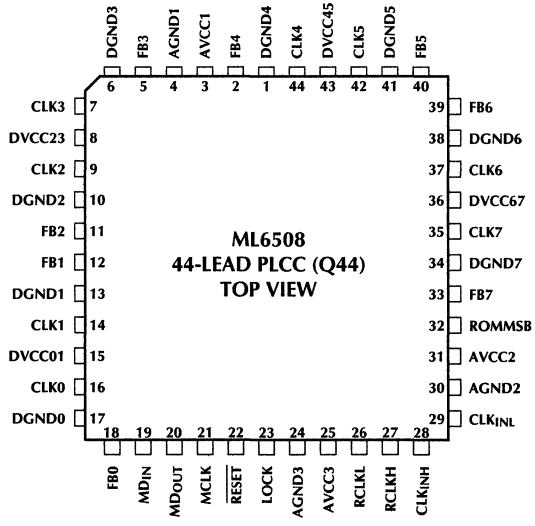
SYSTEM BLOCK DIAGRAM



BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
32	ROMMSB	MSB of the internal ROM address. Tie to GND if not used. See section on Programming the ML6508.
20	MD_{OUT}	Programming pin. See section on Programming the ML6508.
19	MD_{IN}	Programming pin. See section on Programming the ML6508.
21	MCLK	Programming pin. See section on Programming the ML6508.
22	$\overline{RESET}$	Reset all internal circuits. Asserted polarity is low.
23	LOCK	Indicates when the PLL and deskew buffers have locked. Asserted polarity is high.
28 29	CLK_{INH} CLK_{INL}	Input clock pins. For TTL clock reference use CLK_{INH} pin shorted to the CLK_{INL} pin. For PECL clock reference drive pins differentially. Input clock type is selected by the CS bit in the shift register.
16, 14, 9, 7, 44, 42, 37, 35	CLK[0–7]	Clock outputs
18, 12, 11, 5, 2, 40, 39, 33	FB[0–7]	Clock feedback inputs for the deskew buffers
3,31 25	AVCC[1–3]	Analog circuitry supply pins, separated from noisy digital supply pins to provide isolation. All supplies are nominally +5V.
4, 30, 24	AGND[1–3]	Analog circuitry ground pins
15	DVCC01	Digital supply pin for CLK0 and CLK1 output buffers. Nominally +5V.
8	DVCC23	Digital supply pin for CLK2 and CLK3 output buffers. Nominally +5V.
43	DVCC45	Digital supply pin for CLK4 and CLK5 output buffers. Nominally +5V.
36	DVCC67	Digital supply pin for CLK6 and CLK7 output buffers. Nominally +5V.
17, 13, 10, 6, 1, 41, 38, 34	DGND[0–7]	Digital ground pins for CLK [0–7] output buffers. Each clock output buffer has its own ground pin to avoid crosstalk and ground bounce problems.
26 27	RCLKL RCLKH	Differential reference clock output used to minimize part-to-part skew when building clock trees with other PACMan integrated circuits.

ABSOLUTE MAXIMUM RATINGS

VCC Supply Voltage Range ..... –0.3V to 6V
Input Voltage Range ..... –0.3V to VCC
Output Current
CLK[0–7] 70mA
All other outputs 10mA

Junction Temperature ..... 150°C
Storage Temperature ..... –65°C to 150°C

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of VCC = 5V ± 5% and ambient temperature between 0°C and 70°C. Loading conditions are specified individually.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
IDVCC	Supply Current for each pair of clock outputs	All clock outputs open, f_{CLKX} = 0		50		µA
		C_L = 20pF, Z_O = 50Ω f_{OUT} = 80MHz		50		mA
IAVCC1	Static supply current, AVCC1 pin			100		mA
IAVCC2	Static supply current, AVCC2 pin			35		mA
IAVCC3	Static supply current, AVCC3 pin			1		mA
LOW FREQUENCY INPUTS AND OUTPUTS (ROMMSB, MD_{OUT}, MD_{IN}, MCLK, $\overline{RESET}$, LOCK)						
V_{IH}	High level input voltage		DVCC – 0.5			V
V_{IL}	Low level input voltage				DGND + 0.5	V
V_{OH}	High level output voltage, MCLK and MDIN	I_{OH} = –100 µA	DVCC – 0.5			V
V_{OL}	Low level output voltage, MCLK and MDIN	I_{OL} = +200 µA			DGND + 0.5	V
V_{OH}	High level output voltage, LOCK output	I_{OH} = –100 µA I_{OH} = –10 µA	2.4 DVCC – 0.5			V V
V_{OL}	Low level output voltage, LOCK output	I_{OL} = +1 mA			0.4	V
I_{IN}	Static input current				10	µA
C_{IN}	Input capacitance			5		pF
HIGH FREQUENCY INPUTS AND OUTPUTS (CLK_{INH}, CLK_{INL}, FB[0-7], CLK[0-7])						
V_{IH}	High level input voltage	CS = 0 (TTL Input Clock)	2.0			V
		CS = 1 (PECL Input Clock)	AVCC – 1.165		AVCC – 0.88	V
V_{IL}	Low level input voltage	CS = 0 (TTL Input Clock)			0.8	V
		CS = 1 (PECL Input Clock)	AVCC – 1.810		AVCC – 1.475	V
V_{ICM}	Common mode input voltage range for PECL reference clocks	CS = 1 (PECL Input Clock)	2.0		AVCC – 0.4	V
I_{IH}	High level input current	V_{IH} = 2.4V			100	µA
I_{IL}	Low level input current	V_{IL} = 0.4V	–400			µA
V_{OH}	High level output voltage	I_{OH} = –60mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = +60mA			0.4	V

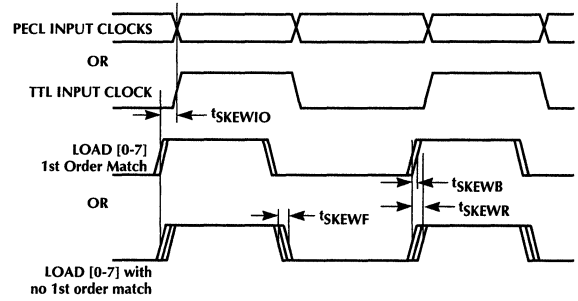
ELECTRICAL CHARACTERISTICS (Continued)

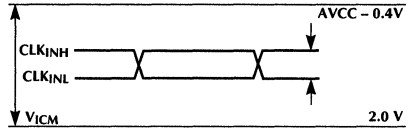
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
AC CHARACTERISTICS rise time, fall time and duty cycle are measured for a generic load; (see Load Conditions section).						
t_R	Rise time, LOAD [0-7] output	0.8 → 2.0V	150		1500	ps
t_F	Fall time, LOAD [0-7] output	2.0 → 0.8V	150		1500	ps
f_{IN}	Input frequency, CLK_{IN} pin		10		80	MHz
f_{OUT}	Output frequency , CLK [0-7] output		10		80	MHz
f_{VCO}	PLL VCO operating frequency		80		160	MHz
DC	Output duty cycle	Measured at device load, at 1.5V	40		60	%
t_{JITTER}	Output jitter	Cycle-to cycle		75		ps
		Peak-to-peak		150		ps
t_{LOCK}	PLL and deskew lock time	After programming is complete		11		ms
SKEW CHARACTERISTICS	All skew measurements are made at the load, at 1.5V threshold each output load can vary independently within the specified range for a generic load (see Load Conditions section).					
t_{SKEWR}	Output to output rising edge skew, all clocks				500	ps
t_{SKEWF}	Output to output falling edge skew	Output clock frequency ≥ 50MHz			1.5	ns
t_{SKEWIO}	CLK_{IN} input to any LOAD [0-7] output Maximum rising edge skew	N = M = 0		600		ps
		N ≥ 2, M ≥ 2		1.25		ns
t_{RANGE}	Round trip delay CLKX to FBX pin; output CLK period = t_{CLK}	Output frequency < 50MHz Output frequency ≥ 50MHz	0 0		10 $t_{CLK}/2$	ns
t_{SKEWB}	Output-to-output rising edge skew, between matched loads	Providing first (see LOAD conditions) order matching order matching between outputs		250		ps
PART-TO-PART SKEW CHARACTERISTICS	Skew measured at the loads, at 1.5V threshold. Reference clock output pins drive clock input pins of another ML6508.					
t_{PP1}	Total load-to-load skew between multiple chips interfaced with reference clock pins.	Slave chip CS = 1, CM = 1 and N = 0, M = 0; RCLK outputs to CLK_{IN} inputs distance less than 2"			TBD	ps
t_{PP2}	Total load-to-load skew between multiple chips interfaced with reference clock pins.	Slave chip CS = 1, CM = 1 and N ≥ 2, M ≥ 2; RCLK outputs to CLK_{IN} inputs distance less than 2"			TBD	ps
PROGRAMMING TIMING CHARACTERISTICS						
t_{RESET}	$\overline{RESET}$ assertion pulse width		50			ns
t_{A1}	AUX mode MCLK high time		2000			ns
t_{A2}	AUX mode MCLK low time		2000			ns
t_{A3}	AUX mode MD_{OUT} data hold time		10			ns
t_{A4}	AUX mode MD_{OUT} data setup time		10			ns

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
PROGRAMMING TIMING CHARACTERISTICS (Continued)						
t_{A5}	AUX mode MCLK period		5000			ns
t_{M1}	MAIN mode MCLK high time		900			ns
t_{M2}	MAIN mode MCLK low time		900			ns
t_{M3}	MAIN mode MCLK period		1800			ns
t_{M4}	MAIN mode MCLK to MD_{OUT} valid (EEPROM read time)				900	ns

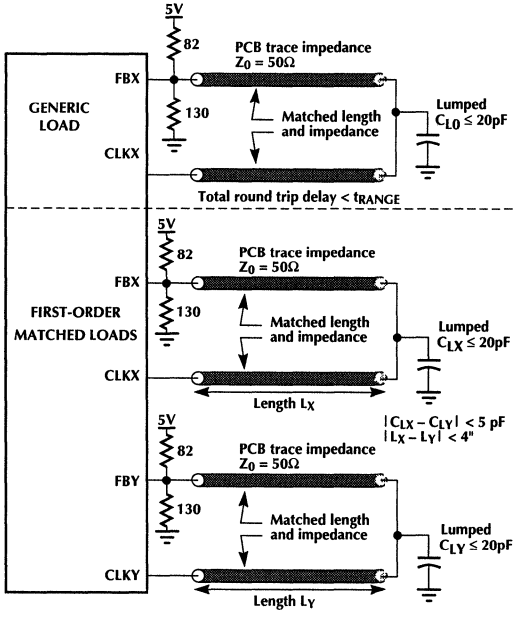
ML6508 configured with bit CM = 0:

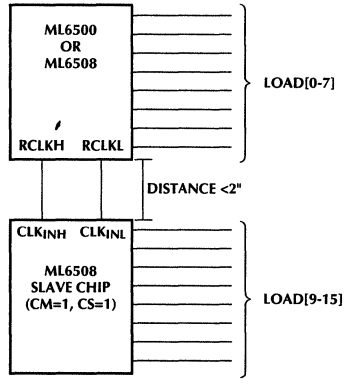


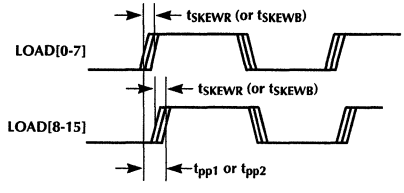


Note: All skew is measured at the device load input pin, NOT at the ML6508 clock output pin. Skew is always a positive number, regardless of which edge is leading and which is trailing.

AC/SKEW CHARACTERISTICS LOAD CONDITIONS







FUNCTIONAL DESCRIPTION

Micro Linear's ML6508 is the first clock chip to use a feedback mechanism to adaptively (on a real time basis), eliminate clock skew in high speed personal computer and workstation system designs. Figure 1 shows a basic configuration of the ML6508 in a system. The skew problem results due to the delaying of clock signals in the system, as shown in Figure 2. Clock skew results from variation in factors like trace length, PCB trace characteristics, load capacitance, parasitic capacitance, temperature and supply variations, etc. Figure 2 shows a representation of the clock skew problem from a timing perspective. It shows a worst case example where the clock signal is delayed so much that its rising edge completely misses the data it is intended to strobe. Using a clock deskew mechanism, this problem can be eliminated and the strobe with the appropriate setup and hold times with respect to the data bus can be generated.

The ML6508 has eight deskew buffers, each with its own independent feedback and error correction circuit. The deskew buffer eliminates skew by using feedback from a remote chip to measure the clock error and then corrects it by generating the appropriate skew to the clock output to compensate.

Eight individually deskewed copies of the clock are provided by the ML6508.

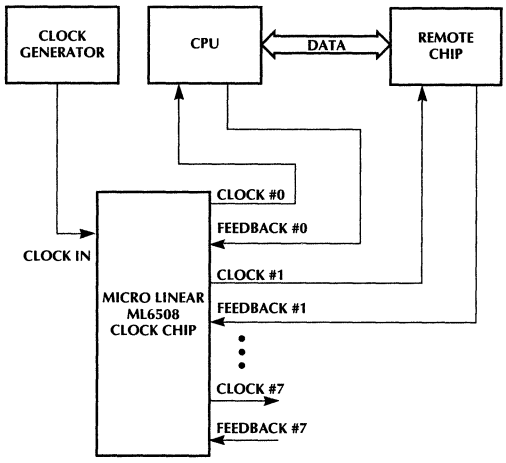


Figure 1. Basic System Configuration Using the ML6508.

The deskew buffers compensate internally for board-level skew caused by the PCB trace length variations and device load variations. This is accomplished by sensing the round trip delay via the return trace, and then delaying or advancing the clock edge so that all 8 output clocks arrive at their loads in phase. Each of the eight clock lines can have any length PCB trace (up to 5ns each way or 1/4th of the output clock period, whichever is smaller) and the device loads can vary from line to line. The ML6508 will automatically compensate for these variations, keeping the device load clocks in phase. Although ML6508 will compensate for skew caused by loading, excessive capacitive loading can cause rise/fall time degradation at the load. Cascading the ML6500 to the ML6508 should be done using the PECL reference clock outputs, to minimize part-to-part skew.

CLOCK REGENERATION

The programmable adaptive clock deskew can function in a clock regeneration mode to assist in building clock trees or to expand the number of de-skewed clock lines. In this mode, it has the ability to do clock multiplication or division as well, while maintaining low skew between

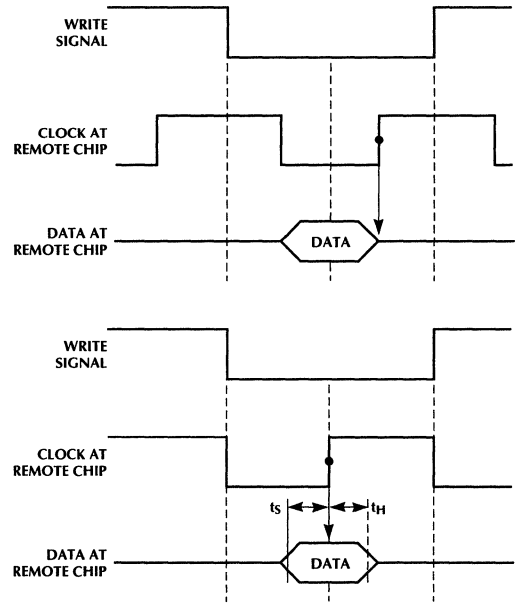


Figure 2. The Skew Problem.

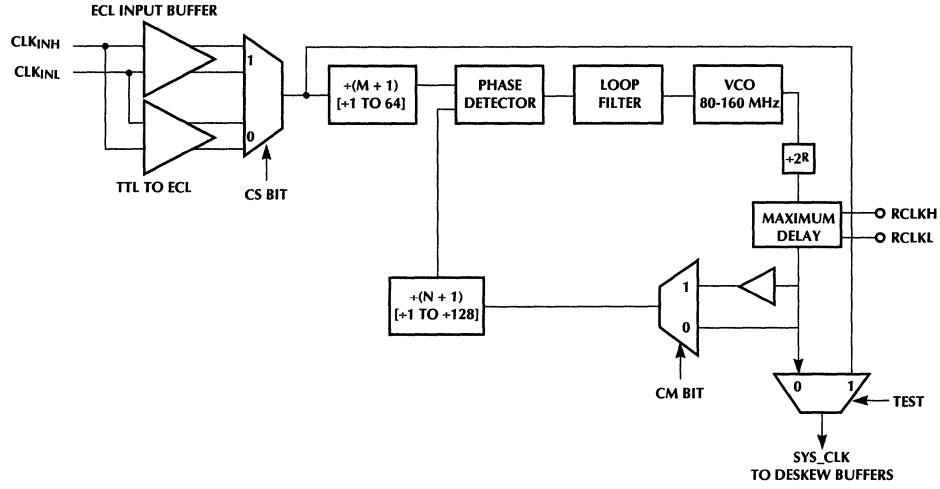


Figure 3. ML6508 Clock Generation Block Diagram.

input clock and output clocks. It can thus generate a 2x or 4x or 0.5x frequency multiplication or division from input to output (e.g. 33 MHz input, 66 MHz output or 66 MHz input, 33 MHz output, etc.). It also can generate a 1x frequency output. The VCO frequency is defined by:

$$f_{VCO} = f_{REF} \times \left[\frac{(N+1)\times 2^R}{(M+1)}\right]$$

and the output frequency is still given by:

$f_{OUT} = f_{VCO}/2^R$ (setting R = 00 defaults to R = 01)

R1	R0	INPUT/OUTPUT RANGE
0	0	Not valid: Defaults to R = 01
0	1	40–80 MHz
1	0	20–40 MHz
1	1	10–20 MHz

Note: R implies R1, R0

The VCO still must remain in the range 80–160 MHz, and the minimum phase detector input frequency is 625kHz = (80 MHz/128). Thus the product of (N + 1) and 2^R should be limited to 128:

$(N + 1) \times 2^R \leq 128$ to make sure that the phase detector inputs remain above the minimum frequency.

Example: Generating a 2x clock input frequency = 33 MHz

Set R = 01 (output range 40 – 80 MHz), N = 5 (0000101), M = 2 (000010), M/S = 0

$$f_{VCO} = f_{REF} \times \left[\frac{(N+1)\times 2^R}{(M+1)}\right] = 33MHz \times \left[\frac{6\times 2^1}{3}\right] = 132MHz$$

$f_{OUT} = f_{VCO}/2^R = 132\ MHz/2^1 = 66\ MHz$

Example: Generating a 1x clock Input frequency = 66 MHz

Set R = 01 (output range 40–80 MHz), set M = 0 (000000), N = 0 (0000000), M/S = 0

$$f_{VCO} = 66MHz \times \left[\frac{1\times 2^1}{1}\right] = 132MHz$$

$F_{OUT} = F_{VCO}/2^R = 132\ MHz/2^1 = 66\ MHz$

For doing frequency multiplication and division, keep $M \geq 2$ and $N \geq 2$ for the lowest skew between input clock and output clock. Several configurations for doing frequency multiplication and division are included in the 8 configurations stored in the on-chip ROM (see PROGRAMMING the ML6508).

ADAPTIVE DESKEW BUFFERS

Each copy of the clock is driven by an adaptive deskew buffer. The deskew buffer compensates for skew time automatically in accordance to the flight time delay it senses on the feedback line.

Figure 4 shows the simplified functional block diagram of the deskew circuit. The phase of the sense signal and the drive signal is presented to a three-input phase comparator and compared with the reference signal. The phase comparator then controls the voltage controlled delay in the output drive line to match the delay of the fixed reference delay line. Therefore, the sum of the delay of the driver circuit, PCB trace delay, rise time delay at the load and the adjustable delay will always equal the fixed maximum delay.

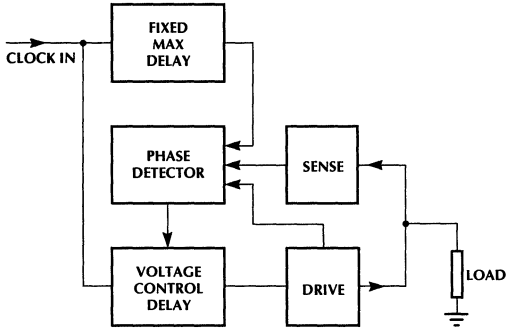
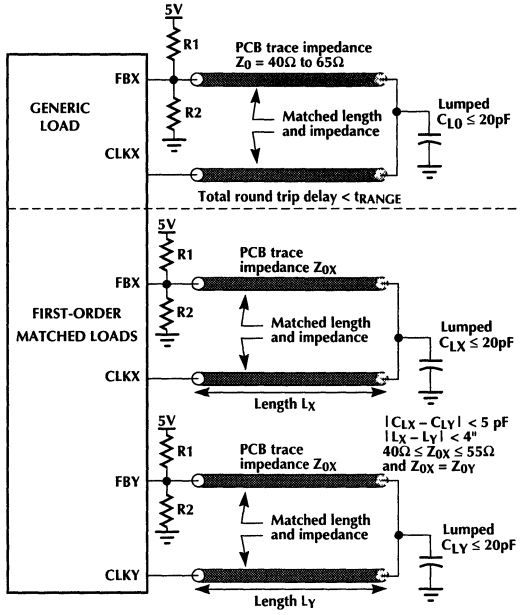


Figure 4. Deskew Circuit Block Diagram.

The sense circuit has an internal level detect such that any skew caused by loading is also accounted for. Since the delay of the circuit is matched for the entire loop, the phase of all the drivers are in close alignment at the inputs of the load.

LOAD CONDITIONS

The ML6508 has been designed to drive the wide range of load conditions that are encountered in a high frequency system. The eight output clock loads can vary individually within a wide range of trace length, impedance and lumped capacitive load, but each load should remain within the designated range for a generic load, to insure the lowest skew and the best signal integrity. The outgoing and return trace should be matched in length and impedance, and the trace should include a termination at the feedback (FB#) pin. All eight output clock traces are generally the same impedance with the same termination resistor values. The clock skew can be further minimized by providing some first order matching between any two loads that require particularly well matched clocks. For best matching use adjacent clock outputs with matched loads.



Termination resistors should have a Thevenin voltage of approximately 3V and a Thevenin resistance equal to the impedance of the PCB trace, Z_0:

$$R_1 = \frac{5}{3}(Z_0) \quad \text{then} \quad R_2 = \frac{3}{2}R_1 \quad (\text{for } V_{CC} = 5V)$$

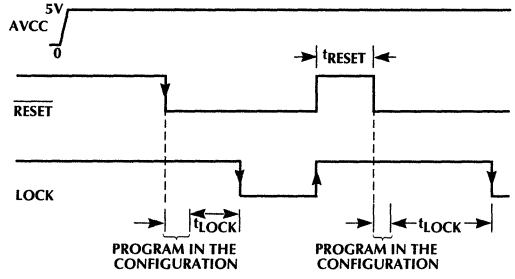
TRACE IMPEDANCE	RECOMMENDED VALUES		MAX. AVG. RESISTOR POWER DISSIPATION W/GENERIC LOAD	
Z0	R1	R2	R1	R2
40Ω	68	100	160 mW	100 mW
50Ω	82	130	150 mW	70 mW
63Ω	110	160	120 mW	70 mW

EXTERNAL INPUT CLOCKS

The external input clock to the ML6508 can be either a differential Pseudo-ECL clock or a single-ended TTL clock. This is selected using the CS bit in the serial shift register. For the single-ended TTL clock tie the CLK_{INH} and CLK_{INL} pins together. The ML6508 ensures that there is a well-defined phase difference between the input and output clocks.

RESET AND LOCK

When RESET is de-asserted, the internal programming logic will become active and load in the configuration bits (see Programming the ML6508). Once the configuration is loaded, the PLL will lock onto the reference signal, and then the deskew blocks will adapt to the load conditions. When all eight output clocks are stable and deskewed, LOCK will be asserted. The asserted polarity of lock is high. Thus, LOCK can be used to indicate that the system is ready, or it can be used to drive the RESET input of another PACMan in a clock tree.



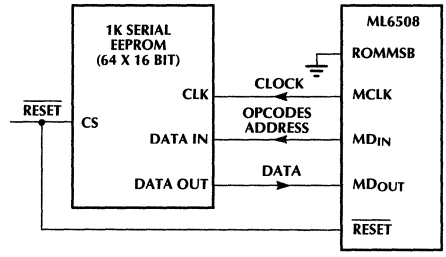
RESET may be reasserted at any time to reset the chip operations. Following a RESET assertion of valid pulse width (see Programming Electrical Characteristics), the ML6508 must again be loaded with a configuration, then it will re-lock and reassert lock when all eight clock outputs are stable and deskewed.

PROGRAMMING THE ML6508

The configuration of the ML6508 is programmed by loading 18 bits into the configuration shift register. To load these bits, the user has 3 options: MAIN, AUX or ROM modes. Which mode is used is determined by the logic level on the MD_{IN} pin when RESET is deasserted. If MD_{IN} is tied high, the ML6508 will assume AUX mode; if its tied low, ROM mode. If MD_{IN} is high-impedance (i.e. tied to the input of an EEPROM), it will assume MAIN mode.

1. MAIN Mode

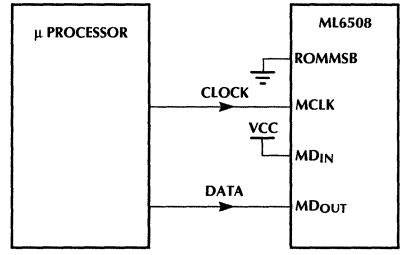
In this mode, the ML6508 will read the 18 configuration bits from an external serial EEPROM, such as the 93C46, using the industry standard 3-wire serial I/O protocol. The serial EEPROM should be a 1K organized in 64 x 16 bits and the PACMan will read the 18 configuration bits out of the two least significant 16-bit words. To use this mode, simply connect the EEPROM serial data input pin to MD_{IN} (ML6508 pin 19), the EEPROM serial data output pin to MD_{OUT} (ML6508 pin 20), and the EEPROM serial data clock pin to MCLK (ML6508 pin 21) and CS pin for the EEPROM should be tied to the RESET signal. After power up, when RESET is deasserted, the ML6508 will automatically generate the address and clock to read out the 18 configuration bits. Refer MAIN Mode waveform in Figure 5.



MAIN Mode Configuration.

2. AUX Mode

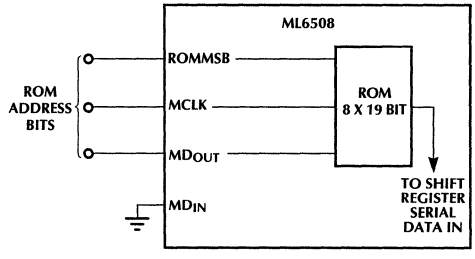
When MD_{IN} is tied to VCC, programming the ML6508 will occur via the AUX Mode. This mode shifts the 18 configuration bits into the shift register directly from the MD_{OUT} pin. The first 18 clock rising edges provided externally on the MCLK pin after RESET is deasserted will be used to load the shift register data, which should be provided on the MD_{OUT} pin. See figure 6.



AUX Mode Configuration.

3. ROM Mode

When MD_{IN} is tied to GND, programming the ML6508 will occur via the ROM Mode. This mode reads the 18 configuration bits directly from an on chip ROM. The selection of one of the eight preset configuration codes is accomplished by means of the pins ROMMSB, MCLK and MD_{OUT} as shown in Table 1. The TEST mode configuration (code 7) is enabled when the TEST bit is set. In this mode the PLL is bypassed for low frequency testing. Codes 0-2 are used when the ML6508 clock inputs are driven from another PACMan's reference clock outputs. Code 3 is used when zero phase error is desired between input and load clocks.



ROM Mode Configuration.

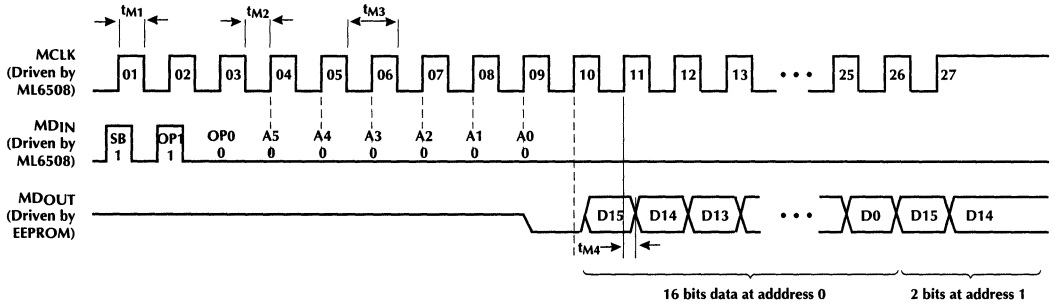


Figure 5. MAIN Mode Waveforms.

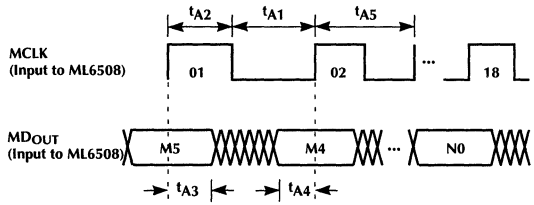


Figure 6. AUX Mode Waveforms.

6

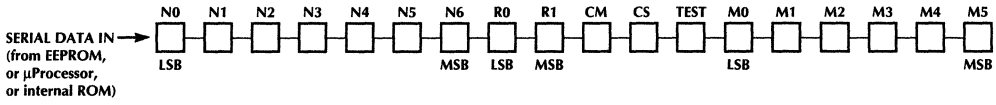
TABLE 1

CODE	DESCRIPTION	SELECTION BITS			INPUT FREQ (MHz)	OUTPUT FREQ (MHz)	CONFIGURATION CODE					
		ROMMSB	MCLK	MD_{OUT}			CS	CM	R1, R0	M	N	TEST
0	PECL Input Clock, 1x mode	0	0	0	40-80	40-80	1	1	01	0	0	0
1	PECL Input Clock, 0.5x mode	0	0	1	40-80	20-40	1	1	10	5	2	0
2	PECL Input Clock, 2x mode	0	1	0	20-40	40-80	1	1	01	2	5	0
3	PECL Input Clock, 1x mode	0	1	1	40-80	40-80	1	0	01	0	0	0
4	TTL Input Clock, 1x mode	1	0	0	40-80	40-80	0	0	01	0	0	0
5	TTL Input Clock, 0.5x mode	1	0	1	40-80	20-40	0	0	10	5	2	0
6	TTL Input Clock, 2x mode	1	1	0	20-40	40-80	0	0	01	2	5	0
7	TEST mode, TTL Input clock	1	1	1	0-50	0-50	0	—	—	—	—	1

REGISTER DEFINITIONS

BITS	REGISTER	SIZE	FUNCTION
11 – 17	N	7 bit	This register is used to define the ratio for the desired frequency of the primary clock.
9 – 10	R	2 bit	This register defines the frequency of the primary clocks, CLK [0-7].
8	CM	1bit	Set CM = 1 when the PECL input reference clock is from another 6500/08 reference clock output. Set CM = 0 if the clock reference is TTL or PECL from an external source and minimum phase error between input and output is desired.
7	CS	1 bit	CS = 0 selects TTL input clock, CS = 1, selects PECL input clock.
6	TEST	1 bit	When set to 1, the PLL is bypassed for low frequency testing.
0 – 5	M	6 bit	This register is used to define the ratio for the desired frequency of the primary clock.

ML6508 SHIFT REGISTER CHAIN

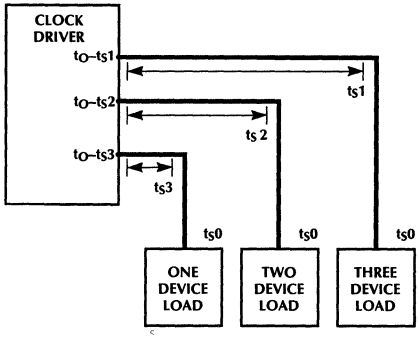


APPLICATIONS

ZERO SKEW CLOCK GENERATION

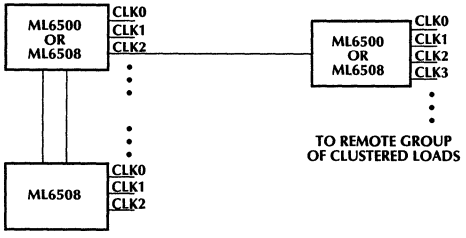
The most advantageous feature of using PACMan is its ability to deliver multiple copies of the clock to the load with very low skew. Because of its unique ability in deskewing, trace length and load consideration are no longer critical in board design.

Because of the unique deskewing scheme, neither the trace length nor the device loads need to be equal. This is true for loads, <20pF. Higher loads can be driven if they are placed close to the clock chip, to guarantee signal integrity.



LOW SKEW CLOCK DISTRIBUTION

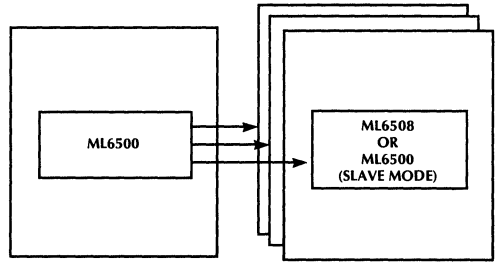
Clock distribution design is usually not a trivial task, especially when multiple clock chips are needed. By using closely grouped PACMans, 16 or more clock lines can be created with low part-to-part skew. Additional groups of clocks can be clustered and driven from de-skewed clock lines, to minimize the number of long-distance clock lines.



BOARD TO BOARD SYNCHRONIZATION

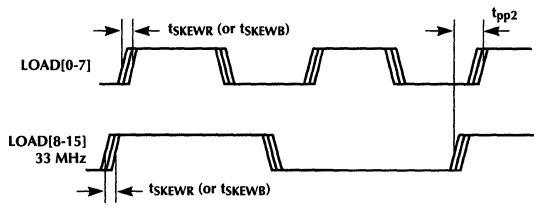
Distribution of the synchronous clock could present significant difficulty at high frequency. With the system clock generated by the ML6508, a zero skew clock delivery to a backplane is now possible. By using the ML6508 slave chip or the ML6500 in slave mode at the receiver end, a near zero delay clock link can be accomplished between the mother board and the satellite boards.

Because the PACMan has frequency doubling capability, a lower frequency signal can be used to route across a back plane.



EXAMPLE CONFIGURATION

Shown in Figure 7 is an example configuration using the ML6500 (Master) and ML6508 (Slave) in tandem to generate eight 66 MHz clocks and eight 33MHz low-skew clocks. This requires only a single crystal and the termination resistors. Configurations are loaded from the internal ROM. PCB traces 0 to 15 are each 50Ω impedance and the load capacitances C_{L0}-C_{L15} are 0 to 20pF each. Outgoing and return trace length for all loads are matched (ie. the load is tapped at the center point of the loop), but no matching is required among separate clock outputs. All traces are shown with a Thevenin termination at the feedback (FB) pin.



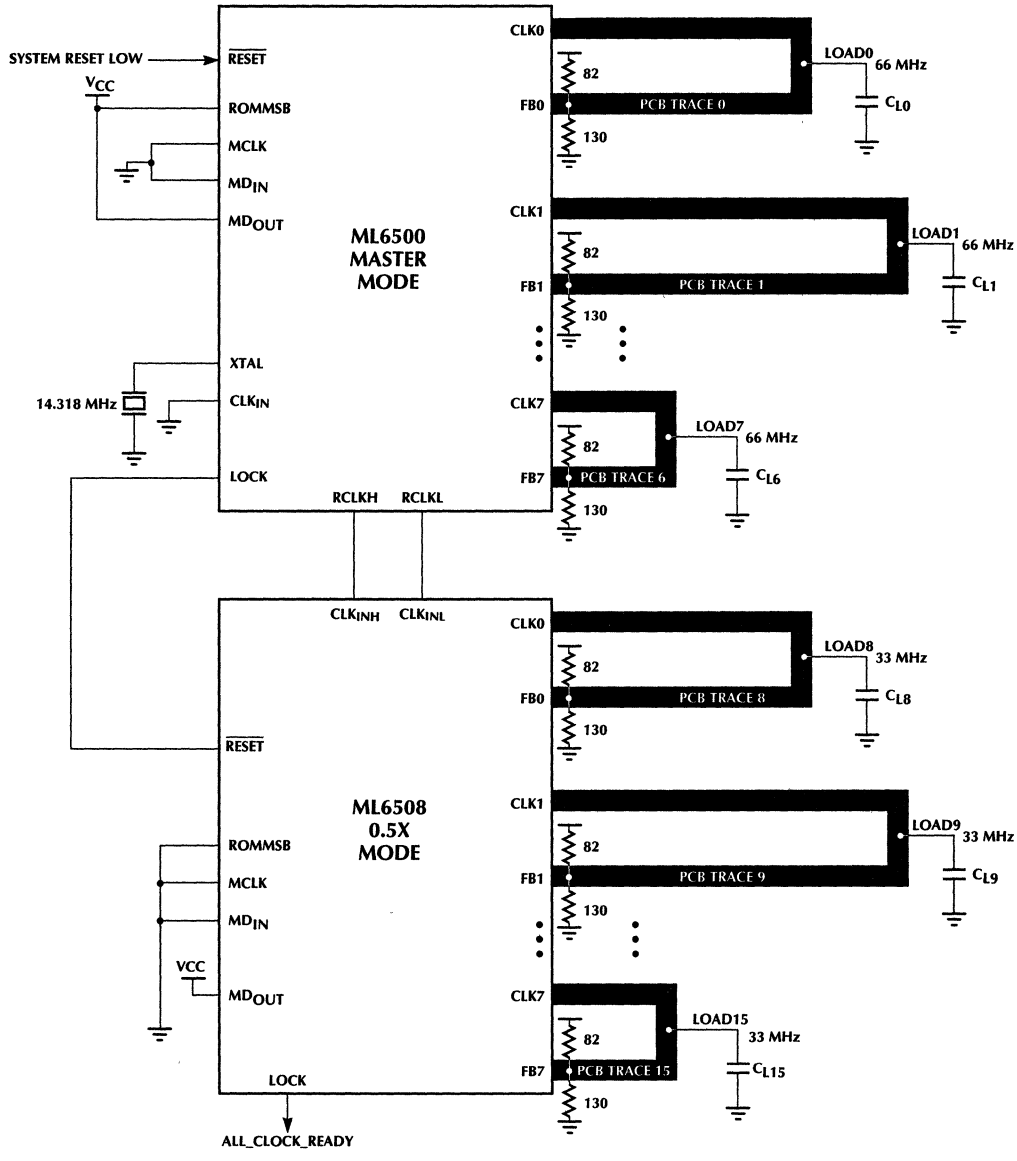


Figure 7. Example use of the ML6500 (Master) in tandem with the ML6508 (Slave) to generate multiple frequency clocks. Master mode ML6500 generates eight 66 MHz clocks while the slave ML6508 generates eight 33 MHz clocks.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6508CQ	0°C to +70°C	44-pin PLCC (Q44)

ML6509

Active SCSI Terminator

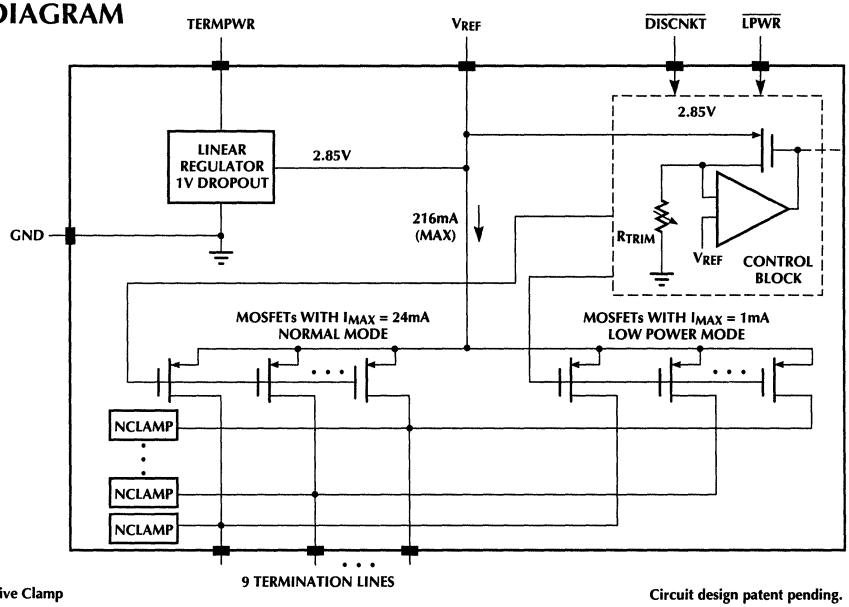
GENERAL DESCRIPTION

The ML6509 BiCMOS SCSI terminator provides active termination in a SCSI system with single-ended drivers and receivers, in full compliance with the SCSI-1, SCSI-2 and SCSI-3 recommendations. It provides a 2.85V reference through an internal 1V dropout linear regulator. Active SCSI termination helps the system designer to effectively control analog transmission line effects like ringing, noise, crosstalk, ground bounce, etc. In addition it provides greater immunity to voltage drops on the TERMPWR line of the SCSI bus. The desired V-I characteristics for signal negation requires that the terminator source 0–24mA while maintaining 2.85V and for signal assertion preferably follow a linear slope of 110Ω. The ML6509 attempts to provide a V-I characteristic optimized to minimize the transmission line effects during both signal assertion and negation, using a MOSFET based architecture. The desired V-I characteristic is achieved by trimming one resistor in the control block. It provides negative clamping for signal assertion transients and current sink capability, to handle active negation driver overshoots above 2.85V, which is currently accomplished with external components in SCSI subsystems today. It provides a disconnect mode, where the terminator is completely disconnected from the SCSI bus and the output capacitance is < 5pF, typically.

FEATURES

- Fully monolithic IC solution providing active termination for 9 lines of the SCSI bus
- Low dropout voltage (1V) linear regulator, trimmed for accurate termination current, with 300mA current source capability
- Output capacitance typically <5pF
- Disconnect mode — Logic pin to disconnect terminator from the SCSI bus, <100µA
- Lowpower mode — For power conscious, portable system & peripheral applications, using less than 6" cables. (Equivalent to a 1mA current drive with a 2.5kΩ termination)
- Current sinking — can sink current >10mA per line to handle active negation driver overshoots above 2.85V
- Negative clamping on all lines to handle signal assertion transients
- Regulator can source 200mA and sink 50mA while maintaining regulation
- Current limit & thermal shutdown protection
- Small and low profile package options; 16-pin SOIC (300 mil), 20-pin TSSOP (1 mil height)

BLOCK DIAGRAM



NCLAMP = Negative Clamp

Circuit design patent pending.

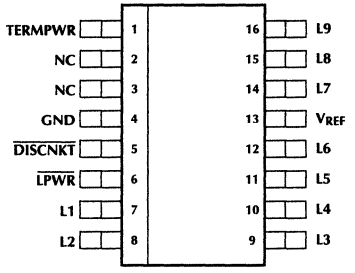
GENERAL DESCRIPTION (Continued)

One unique feature of the ML6509 is its support for a Low Power mode, for use in Notebook and portable computer applications, where it provides a 1mA (approximately 2.5KΩ termination) for less than 6" cable lengths. This minimizes the battery drain significantly in such systems.

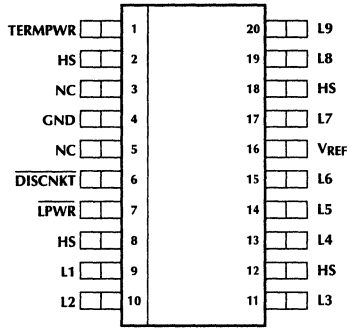
Current limiting and thermal shutdown protection are also provided. The ML6509 provides 9 lines of termination in the industry's smallest package — 20-pin TSSOP. The nine line configuration is optimal for wide SCSI's 18, 27, or 45 line termination needs.

PIN CONFIGURATION

16-Pin SOIC



20-Pin TSSOP



PIN DESCRIPTION

NAME	DESCRIPTION
TERMPWR	Termination Power. Should be connected to the SCSI TERMPWR line. A 10µF tantalum local bypass capacitor is recommended per system, as shown in the application diagram
L1	Signal Termination 1. SCSI Bus line 1
L2	Signal Termination 2. SCSI Bus line 2
L3	Signal Termination 3. SCSI Bus line 3
L4	Signal Termination 4. SCSI Bus line 4
L5	Signal Termination 5. SCSI Bus line 5
L6	Signal Termination 6. SCSI Bus line 6
L7	Signal Termination 7. SCSI Bus line 7
L8	Signal Termination 8. SCSI Bus line 8
L9	Signal Termination 9. SCSI Bus line 9

NAME	DESCRIPTION
V_{REF}	2.85V_{REF} Output. External decoupling with a 10µF tantalum in parallel with a 0.1µF ceramic capacitor is recommended, as shown in the application diagram.
$\overline{\text{DISCNKT}}$	Disconnect Terminator. Logic input to disconnect the terminator from the bus when the SCSI device no longer needs termination due to not being the last device on the bus or otherwise. Active low input.
$\overline{\text{LPWR}}$	Low Power Mode. Logic input to switch the terminator mode to a ~2.5kΩ termination, with a 1mA drive capability, meant for power conscious battery applications which use SCSI devices supporting cable lengths less than six inches. Active low input.
GND	Ground. Signal Ground (0V)
HS	Heat Sink Ground. Should be connected to GND.

NOTE: The $\overline{\text{DISCNKT}}$ and $\overline{\text{LPWR}}$ lines have 200kΩ internal pullup resistors connected to the supply. These pins should be left floating for normal operation and should be connected to ground to enable the function.

ABSOLUTE MAXIMUM RATINGS

Signal Line Voltage ..... –0.3 to TERMPWR +0.3V
Regulator Output Current ..... –100 to 300mA
TERMPWR Voltage ..... –0.3 to +7V
Storage Temperature ..... –65°C to 150°C
Soldering Temperature ..... 260°C for 10 sec
Thermal Impedance (θ_{JA})
SOIC ..... 95°C/W
TSSOP ..... 110°C/W

OPERATING CONDITIONS

TERMPWR Voltage ..... 4V to 5.25V
Operating Temperature ..... 0°C to 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for 4V ≤ TERMPWR ≤ 5.25V, and T_A = 0°C to 70°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY					
TERMPWR Supply Current	L1–L9 = open, $\overline{\text{DISCNKT}}$ = open		3.5	5	mA
	L1–L9 = 0.2 V, $\overline{\text{DISCNKT}}$ = open		225		mA
	$\overline{\text{DISCNKT}}$ = 0 (active)		70	100	µA
INPUT					
Input Low Voltage	$\overline{\text{LPWR}}$, $\overline{\text{DISCNKT}}$			1.0	V
Input High Voltage	$\overline{\text{LPWR}}$, $\overline{\text{DISCNKT}}$	TERMPWR –1.0			V
OUTPUT					
Output High Voltage	Measuring each signal line while other eight are high	2.8	2.85	2.9	V
Maximum Output Current (Normal Mode)	V_{OUT} = 0.2V, Measuring each signal line while the other eight are high			24	mA
Maximum Output Current (Lowpower Mode)	V_{OUT} = 0.2V, $\overline{\text{LPWR}}$ = 0, and measuring each signal line while the other eight are high	0.8	1	1.2	mA
Output Clamp Level	I_{OUT} = –30mA (Note 1)	–0.15	0	0.15	V
Current Sink Capability	V_{OUT} = 3.2V (per line)	7	12		mA
Output Capacitance (ML Method)	L1 thru L9, $\overline{\text{DISCNKT}}$ = 0 $2V_{P-P}$ 100kHz square wave applied biased at 1V D.C. (Note 2)		4	5	pF
Output Capacitance (X3T9.2/855D method)	L1 thru L9, $\overline{\text{DISCNKT}}$ = 0 $0.4V_{P-P}$, 1MHz square wave applied biased at 0.5V D.C. (Note 1)		6	7	pF
REGULATOR					
Output Voltage	Sourcing 0–200mA	2.8	2.85	2.9	V
	Sinking 0–50mA (Note 1)	2.8	2.85	2.95	V
Dropout Voltage	L1–L9 = 0.2V, V_{OUT} = 2.85V		1.0	1.2	V
Short Circuit Current	Regulator output = 0V		100		mA
	Regulator output = 5V		300		mA
Thermal Shutdown			170		°C

Note 1: Parameter guaranteed by characterization only.
Note 2: Only one pin is checked in the production test environment. Otherwise parameter is guaranteed by characterization and correlation.

FUNCTIONAL DESCRIPTION

The SCSI Terminator helps in decreasing the transmission line effects with precise termination. Termination is conventionally provided at the beginning and end of the SCSI bus, however when additional peripherals are added, the termination needs to be disabled from the current device and enabled on the last device on the bus. Existing termination schemes use a SIP (Single-In-Line package) which is plugged into a socket on the PC board of the SCSI peripheral. To remove the termination, the user needs to pull the resistor SIP out of its socket. With the higher levels of system integration, this is no longer a simple task. With the increasing use of higher data rates and cable lengths in SCSI subsystems, the need for active termination is becoming necessary. Active termination also minimizes power dissipation and can be activated or deactivated under software control, thus eliminating the need for end user intervention. The V-I characteristics of popular SCSI termination schemes are shown in Figure 3. Theoretically the desired V-I characteristics are the Boulay type for signal assertion (high to low) and the Ideal type for signal negation. The ML6509 with its MOSFET based nonlinear termination element attempts to provide the most optimum V-I characteristics — optimized for both signal assertion and negation.

The ML6509 provides active termination for nine signal lines, thus accommodating basic SCSI which requires 18 lines to be terminated and wide SCSI which requires 27, 36 or 45 lines to be terminated. The ML6509 integrates an accurate voltage reference (1V dropout voltage) and nine MOSFET based termination lines. A single internal resistor is trimmed to tune the V-I characteristic of the MOSFETs as shown in figure 1. The voltage reference circuit produces a precise 2.85V level and is capable of sourcing at least 24mA into each of the nine terminating lines when low (active). When the signal line is negated (driver turns off), the terminator pulls the signal line to 2.85V (quiescent state). When all signal lines are inactive, the regulator will source about 300mA.

The ML6509 SCSI Terminator provides two control signals, $\overline{\text{DISCNKT}}$ & $\overline{\text{LPWR}}$ which are active low signals and have an internal 200kΩ pull-up resistor. The $\overline{\text{DISCNKT}}$ input when asserted low, isolates the ML6509 from the signal lines and effectively removes the terminator from the SCSI Bus with a disconnect mode current of less than 100µA. The $\overline{\text{LPWR}}$ input, when asserted low, puts the ML6509 in the low power termination mode by providing only a 1mA drive capability with an effective termination impedance of 2.5kΩ. This is intended for power conscious portable system and peripheral applications where the cable lengths are small, thus resulting is fast signal transitions and practically no transmission line effects, while consuming very minimum power (9mA worst case if all lines were active). At the same time, if this portable system were connected with an external SCSI peripheral, over a long cable, the normal terminator mode could be enabled to ensure compliance with the SCSI standard and maintain data integrity. In addition the ML6509 provides for negative clamping of signal transients and also supports current sink capability in excess of 10mA per signal line, to handle active negation driver overshoot above 2.85V, a common occurrence with SCSI transceivers. These functions need to be handled with external components in SCSI subsystems today. Thus the ML6509 helps in eliminating a number of external components.

Disconnect mode capacitance is a very critical parameter in SCSI systems. The ML6509 provides the lowest capacitance contribution of max 5pF and this is guaranteed by production test.

Figure 2 gives an application diagram showing a typical SCSI bus configuration. To ensure proper operation, the TERMPWR pin must be connected to the SCSI TERMPWR line. Each ML6509 requires parallel 0.1µF and 10µF capacitors connected between V_{REF} and GND pins and the TERMPWR line needs a 10µF bypass capacitor per SCSI system.

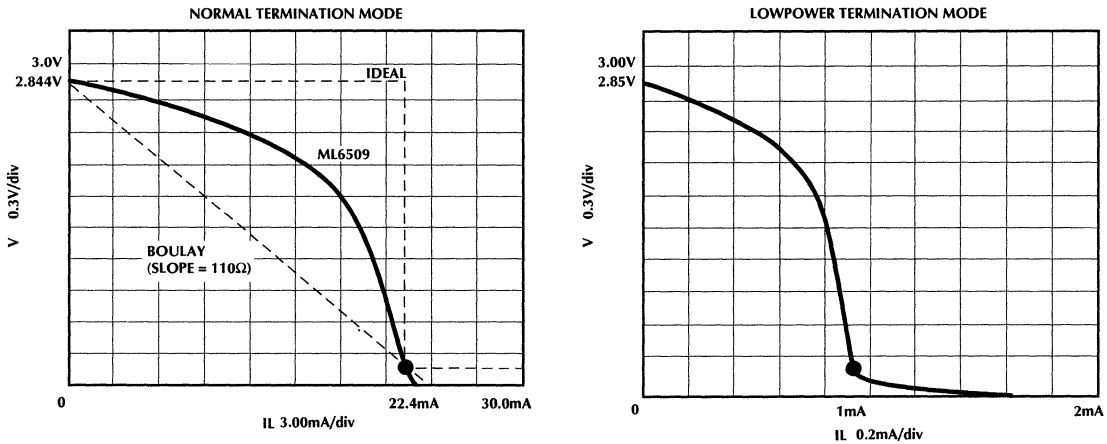


Figure 1. Trimmed V-I Characteristic of the ML6509

Thus in an 8-bit wide SCSI bus arrangement ("A" Cable), two ML6509's would be needed at each end of the SCSI cable in order to terminate the 18 active signal lines. 16-bit wide SCSI would use three ML6509's, while 32-bit wide SCSI bus would require five ML6509's.

In a typical SCSI subsystem, the open collector driver in the SCSI transceiver, when asserted, pulls low and when negated, the termination resistance serves as the pull-up. Also shown in figure 2, is a typical cable response to a pulse. The receiving end of the cable will exhibit a single time delay. When negated, the initial step will reach an intermediate level defined as V_{STEP}. With the higher SCSI data rates, sampling could occur during this step portion. In order to get the most noise margin, the step needs to be as high as possible to prevent false triggering. For this reason the regulator voltage and the resistor defining the MOSFETs characteristic is trimmed to ensure that the I_O is as close as possible to the SCSI max current specification. V_{STEP} is defined as follows :

$$V_{STEP} = V_{OL} + (I_O \times Z_O)$$

where

V_{OL} is the Driver output low voltage,

I_O is current from receiving terminator

Z_O is characteristic impedance of cable.

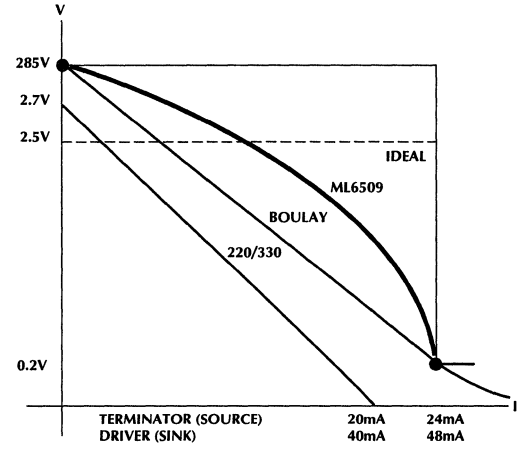


Figure 3. V-I Characteristics of Various SCSI Termination Schemes

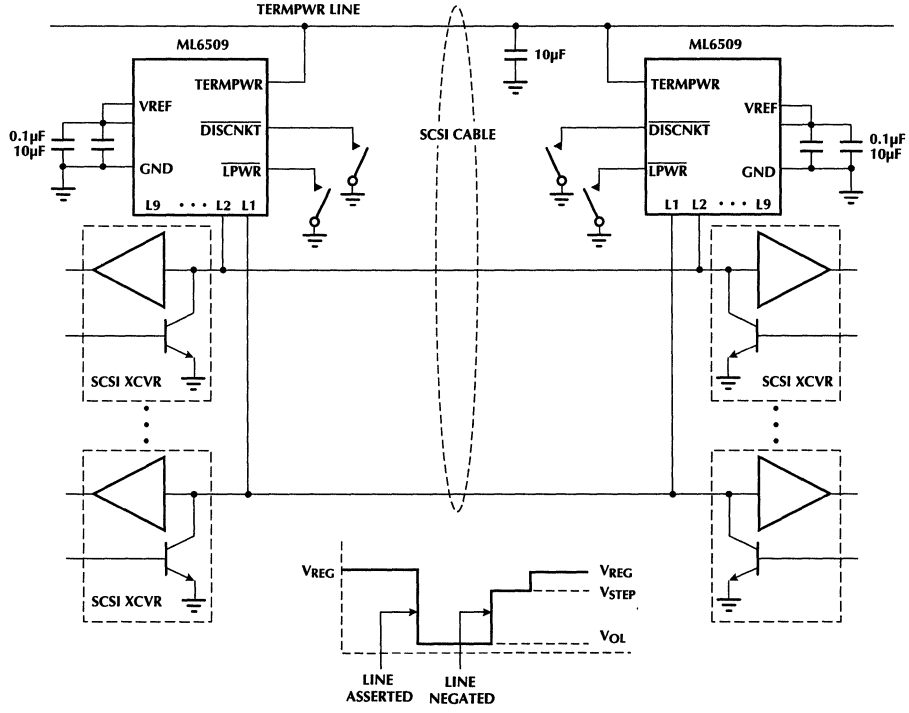


Figure 2. Application Diagram Showing Typical SCSI Bus Configuration with the ML6509

This is a very important characteristic that the terminator helps overcome by increasing the noise margin and boosting the step as high as possible. This capability for the ML6509 implementation is illustrated in the attached simulation graphs which show the terminator performance under different cable impedance situations and a comparison is shown with the standard Boulay terminator, under identical conditions.

APPLICATION INFORMATION

ML6509 EVALUATION BOARD

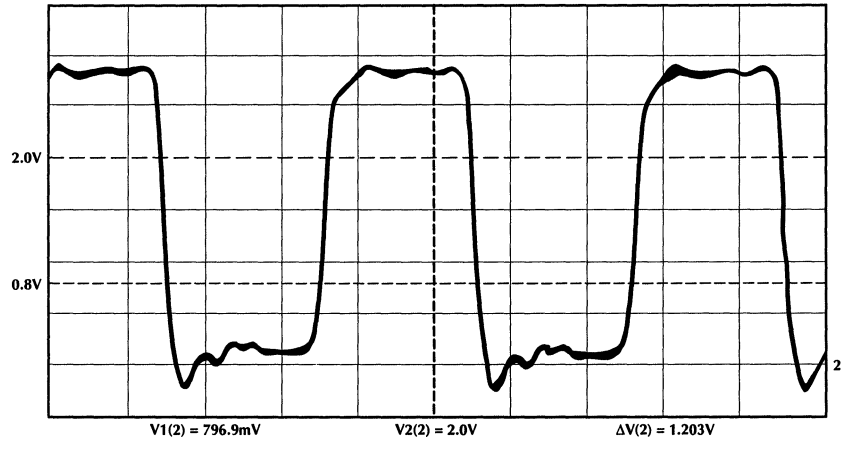
Shown below is the schematic, board component layout, and parts list of the ML6509 SCSI Terminator evaluation board. This evaluation board provides termination for 18 lines of SCSI signals and can be connected as the last device on a standard SCSI Bus system. The SCSI Bus signals can then be monitored to see the impact of the ML6509 Active SCSI Terminator in minimizing the transmission line effects. In addition the disconnect mode and lowpower mode can also be evaluated with respect to power dissipation and output capacitance.

ML6509 EVAL BOARD PARTS LIST

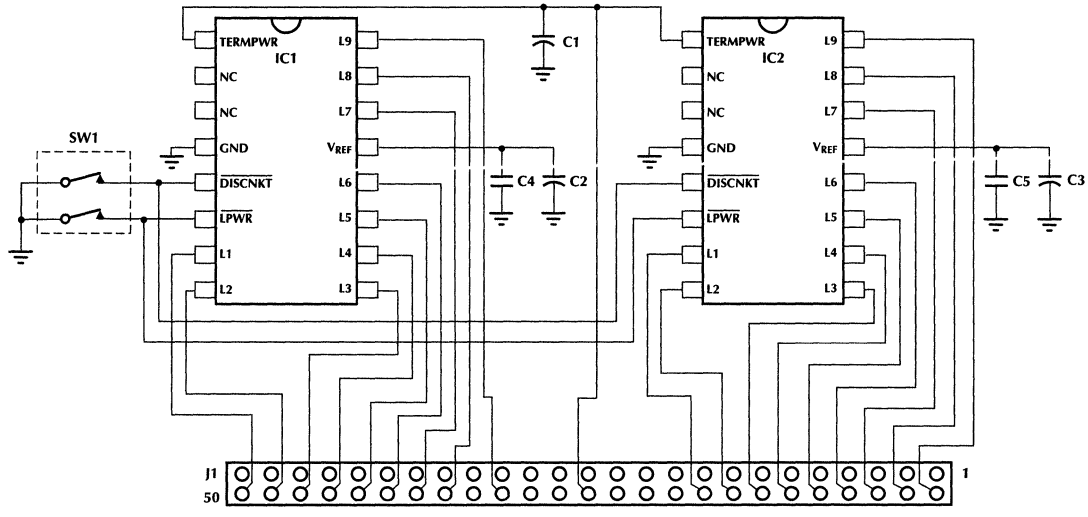
PART#	DESCRIPTION
IC1, IC2	ML6509 Active SCSI Terminator
C1	10µF, 6V Tantalum Chip Capacitor (Philips 49MC106C006K0ASFT)
C2, C3	10µF, 4V Tantalum Chip Capacitor (Philips 49MC106C004K0ASFT)
C4, C5	0.1µF Ceramic Chip Capacitor (Philips C104K1206XFNT)
SW1	Two Position DIP Switch (C&K BD02)
J1	50-pin SCSI Header Connector (AMP 1-103311-0)

TRANSIENT RESPONSE (ACTUAL)

(Approximately 110Ω, 10 feet long, ribbon cable stock)



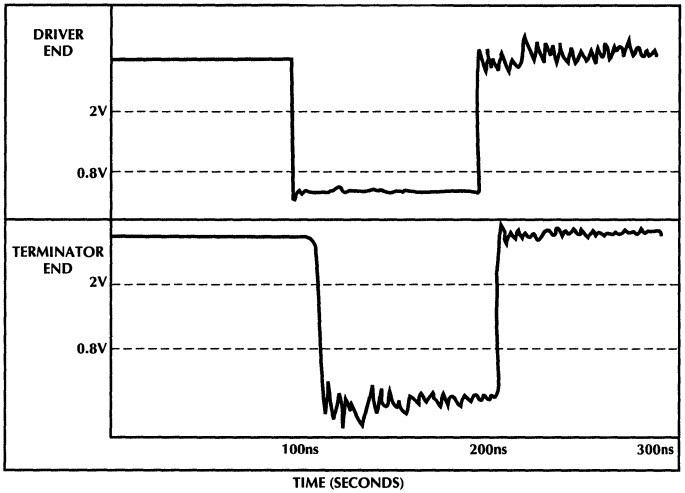
TYPICAL APPLICATION CIRCUIT



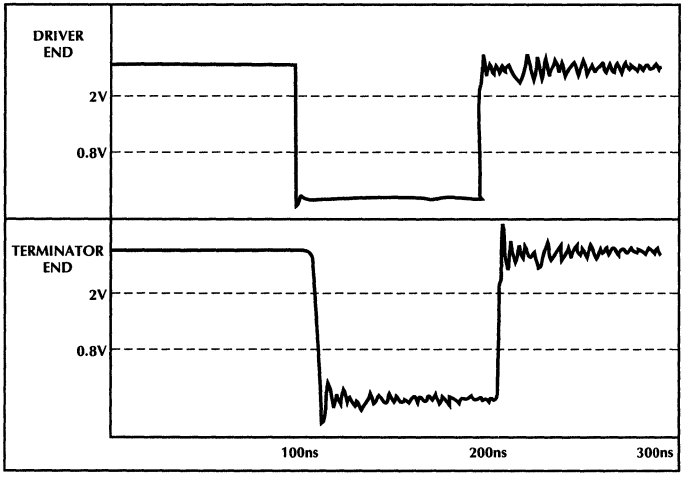
SIGNAL ASSERTION/NEGATION WAVEFORMS (SIMULATED)

Conditions Low Cable impedance of 110Ω (worst case)
t_D = 10ns
10 segment distributed L-C, SCSI Bus Model
Driver end of cable not terminated

ML6509 SCSI TERMINATOR



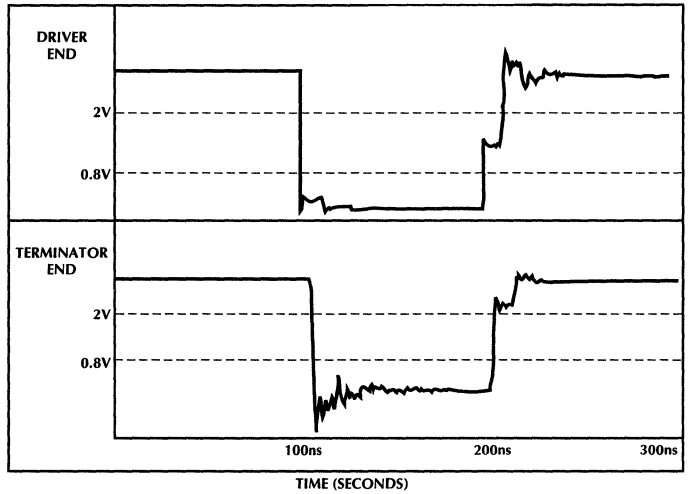
BOULAY TERMINATOR



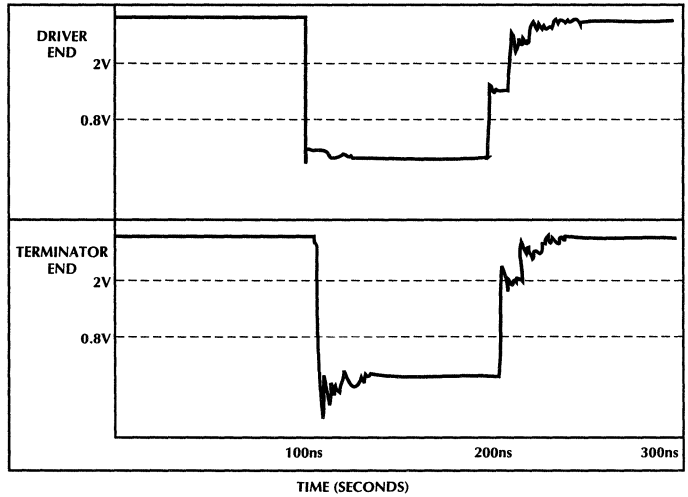
SIGNAL ASSERTION/NEGATION WAVEFORMS(SIMULATED)

Conditions Low Cable impedance of 55Ω (worst case)
t_D = 10ns
10 segment distributed L-C, SCSI Bus Model
Driver end of cable not terminated

ML6509 SCSI TERMINATOR



BOULAY TERMINATOR



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6509CS	0°C to +70°C	16-pin SOIC (S16W)
ML6509CT	0°C to +70°C	20-pin TSSOP (T20)

ML6509EVAL

Active SCSI Terminator Evaluation Kit

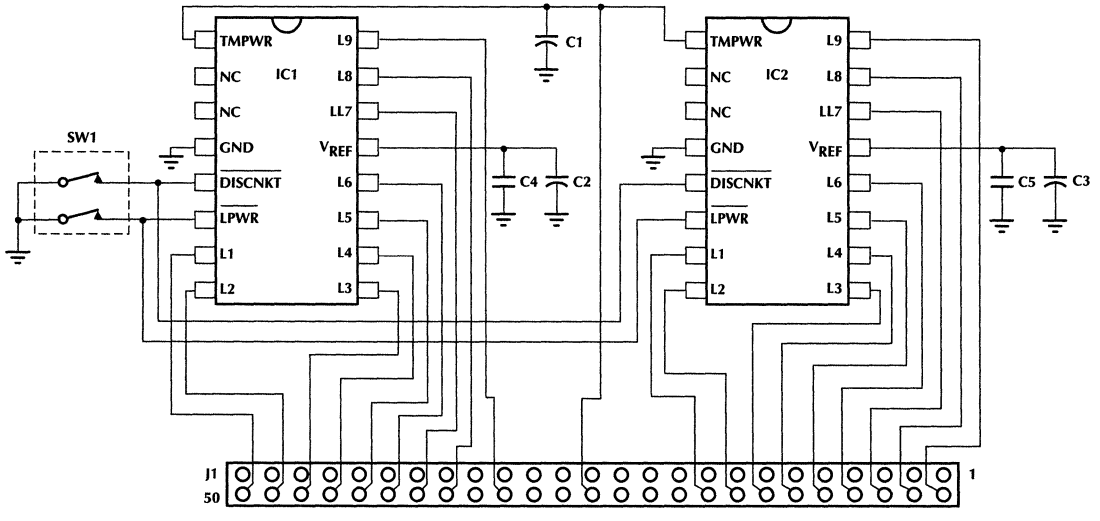
GENERAL DESCRIPTION

The ML6509 BiCMOS SCSI terminator provides active termination in a SCSI system with single-ended drivers and receivers, in full compliance with the SCSI-1, SCSI-2 and SCSI-3 recommendations. It provides a 2.85V reference through an internal 1V dropout linear regulator. Active SCSI termination helps the system designer to effectively control analog transmission line effects like ringing, noise, crosstalk, ground bounce, etc. In addition it provides greater immunity to voltage drops on the TERMPWR line of the SCSI bus. The desired V-I characteristics for signal negation requires that the terminator source 0–24mA while maintaining 2.85V and for signal assertion preferably follow a linear slope of 110Ω. The ML6509 attempts to provide a V-I characteristic optimized to minimize the transmission line effects during both signal assertion and negation, using a MOSFET based architecture. The desired V-I characteristic is achieved by trimming one resistor in the control block. It provides negative clamping for signal assertion transients and current sink capability, to handle active negation driver overshoots above 2.85V, which is currently accomplished with external components in SCSI subsystems today. It provides a disconnect mode, where the terminator is completely disconnected from the SCSI bus and the output capacitance is < 5pF, typically.

FEATURES

- Fully monolithic IC solution providing active termination for 9 lines of the SCSI bus
- Low dropout voltage (1V) linear regulator, trimmed for accurate termination current, with 300mA current source capability
- Output capacitance < 5pF, typically
- Disconnect mode — Logic pin to disconnect terminator from the SCSI bus, <100µA
- Lowpower mode — For power conscious, portable system & peripheral applications, using less than 6" cables. (Equivalent to a 1mA current drive with a 2.5KΩ termination)
- Current sinking — can sink current up to 10mA per line to handle active negation driver overshoots above 2.85V up to 3.2V
- Negative clamping on all lines to handle signal assertion transients
- Regulator can source 200mA and sink 50mA while maintaining regulation
- Current limit & thermal shutdown protection
- Small and low profile package options; 16-pin SOIC (300 mil), 20-pin TSSOP (1 mil height)
- 50 Pin connector for direct connection to SCSI bus ribbon cable
- Dip switches to control the low power and disconnect mode

SCHEMATIC



ML6510

Series Programmable Adaptive Clock Manager (PACMan™)

GENERAL DESCRIPTION

The ML6510 (Super PACMan™) is a Programmable Adaptive Clock Manager which offers an ideal solution for managing high speed synchronous clock distribution in next generation, high speed personal computer and workstation system designs. It provides eight channels of deskew buffers that adaptively compensate for clock skew using only a single trace. The input clock can be either TTL or PECL, selected by a bit in the control register. Frequency multiplication or division is possible using the M&N divider ratio, within the maximum frequency limit. 0.5X, 1X, 2X and 4X clocks can be easily realized.

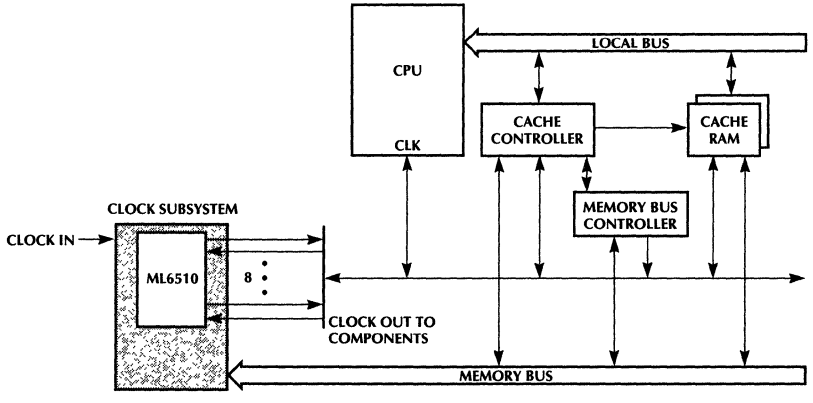
The ML6510 is implemented using a low jitter PLL with on-chip loop filter. The ML6510 deskew buffers adaptively compensate for clock skew on PC boards. An internal skew sense circuit is used to sense the skew caused by the PCB trace and load delays. The sensing is done by detecting a reflection from the load and the skew is corrected adaptively via a unique phase control delay circuit to provide low load-to-load skew, at the end of the PCB traces. Additionally, the ML6510 supports PECL reference clock outputs for use in the generation of clock trees with minimal part-to-part skew. The chip configuration can be programmed to generate the desired output frequency using the internal ROM or an external serial EEPROM or a standard two-wire serial microprocessor interface.

FEATURES

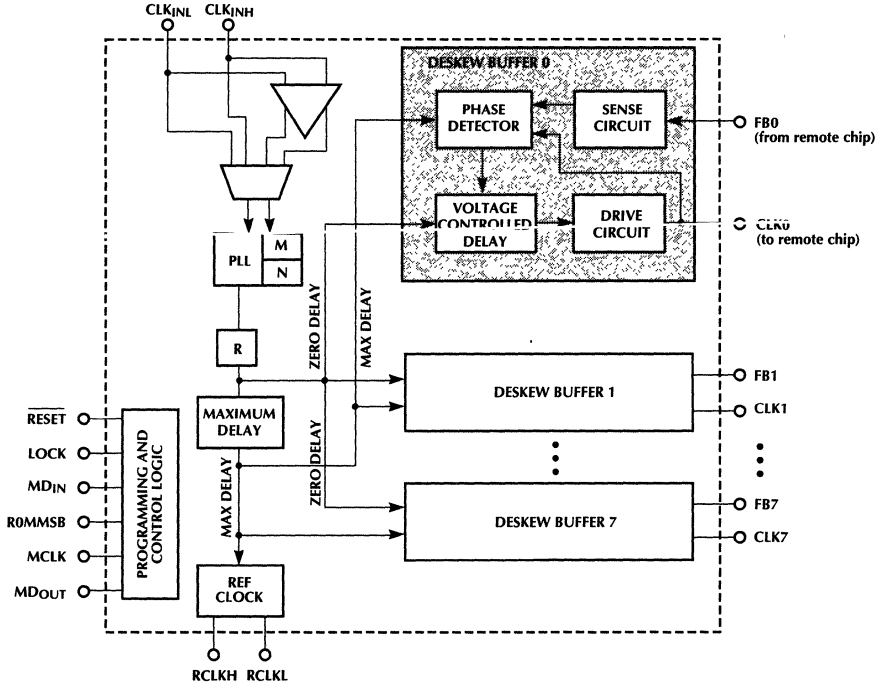
- Input clocks can be either TTL or PECL with low input to output clock phase error
- 8 independent, automatically deskewed clock outputs with up to 5ns of on-board deskew range (10ns round trip)
- Controlled edge rate TTL-compatible CMOS clock outputs capable of driving 40Ω PCB traces
- 10 to 80MHz (6510-80) or 10 to 130MHz (6510-130) input and output clock frequency range
- Less than 500ps skew between inputs **at the device loads**
- Small-swing reference clock outputs for minimizing part-to-part skew
- Frequency multiplication or division is possible using the M&N divider ratio
- Lock output indicates PLL and deskew buffer lock
- Test mode operation allows PLL and deskew buffer bypass for board debug
- Supports industry standard processors like Pentium™ Intel80486™ Mips R4000™ SPARC™ 68040™ PowerPC™ Alpha™ etc.

6

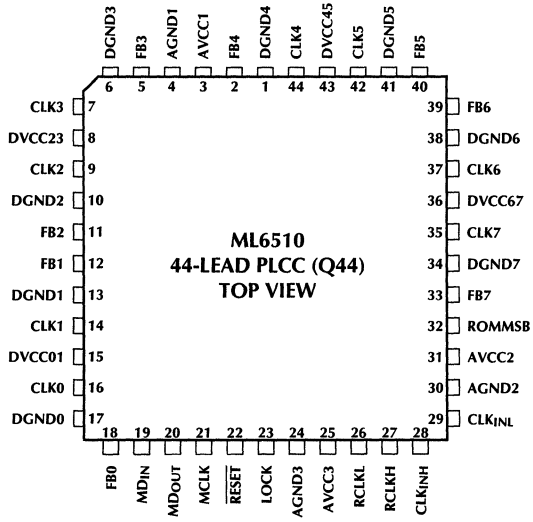
SYSTEM BLOCK DIAGRAM



BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
32	ROMMSB	MSB of the internal ROM address. Tie to GND if not used. See section on Programming the ML6510.
20	MD_{OUT}	Programming pin. See section on Programming the ML6510.
19	MD_{IN}	Programming pin. See section on Programming the ML6510.
21	MCLK	Programming pin. See section on Programming the ML6510.
22	$\overline{RESET}$	Reset all internal circuits. Asserted polarity is low.
23	LOCK	Indicates when the PLL and deskew buffers have locked. Asserted polarity is high.
28 29	CLK_{INH} CLK_{INL}	Input clock pins. For TTL clock reference use CLK_{INH} pin shorted to the CLK_{INL} pin. For PECL clock reference drive pins differentially. Input clock type is selected by the CS bit in the shift register.
16,14,9,7, 44, 42, 37, 35	CLK[0–7]	Clock outputs
18,12,11,5, 2, 40, 39, 33	FB[0–7]	Clock feedback inputs for the deskew buffers
3,31 25	AVCC[1–3]	Analog circuitry supply pins, separated from noisy digital supply pins to provide isolation. All supplies are nominally +5V.
4, 30, 24	AGND[1–3]	Analog circuitry ground pins
15	DVCC01	Digital supply pin for CLK0 and CLK1 output buffers. Nominally +5V.
8	DVCC23	Digital supply pin for CLK2 and CLK3 output buffers. Nominally +5V.
43	DVCC45	Digital supply pin for CLK4 and CLK5 output buffers. Nominally +5V.
36	DVCC67	Digital supply pin for CLK6 and CLK7 output buffers. Nominally +5V.
17, 13, 10, 6, 1, 41, 38, 34	DGND[0–7]	Digital ground pins for CLK [0–7] output buffers. Each clock output buffer has its own ground pin to avoid crosstalk and ground bounce problems.
26 27	RCLKL RCLKH	Differential reference clock output used to minimize part-to-part skew when building clock trees with other PACMan integrated circuits.

ABSOLUTE MAXIMUM RATINGS

VCC Supply Voltage Range ..... –0.3V to 6V
Input Voltage Range ..... –0.3V to VCC
Output Current
CLK[0–7] 70mA
All other outputs 10mA

Junction Temperature ..... 150°C
Storage Temperature ..... –65°C to 150°C

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of DVCC = AVCC = 5V ± 5% and ambient temperature between 0°C and 70°C. Loading conditions are specified individually.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
DVCCXX	Supply Current for each pair of clock outputs	f_{CLKX} = 0		50		µA
		C_L= 20pF, Z_O = 50Ω f_{OUT} = 80MHz		40		mA
IAVCC1	Static supply current, AVCC1 pin			100		mA
IAVCC2	Static supply current, AVCC2 pin			35		mA
IAVCC3	Static supply current, AVCC3 pin			1		mA
LOW FREQUENCY INPUTS AND OUTPUTS (ROMMSB, MD_{OUT}, MD_{IN}, MCLK, $\overline{RESET}$, LOCK)						
V_{IH}	High level input voltage		DVCC – 0.5			V
V_{IL}	Low level input voltage				DGND + 0.5	V
V_{OH}	High level output voltage, MCLK and MDIN	I_{OH} = –100 µA	DVCC – 0.5			V
V_{OL}	Low level output voltage, MCLK and MDIN	I_{OL} = +200 µA			DGND + 0.5	V
V_{OH}	High level output voltage, LOCK output	I_{OH} = –100 µA I_{OH} = –10 µA	2.4 DVCC – 0.5			V V
V_{OL}	Low level output voltage, LOCK output	I_{OL} = +1 mA			0.4	V
I_{IN}	Static input current				10	µA
C_{IN}	Input capacitance			5		pF
HIGH FREQUENCY INPUTS AND OUTPUTS (CLK_{INH}, CLK_{INL}, FB[0-7], CLK[0-7])						
V_{IH}	High level input voltage	CS = 0 (TTL Input Clock)	2.0			V
		CS = 1 (PECL Input Clock)	AVCC – 1.165		AVCC – 0.88	V
V_{IL}	Low level input voltage	CS = 0 (TTL Input Clock)			0.8	V
		CS = 1 (PECL Input Clock)	AVCC – 1.810		AVCC – 1.475	V
V_{ICM}	Common mode input voltage range for PECL reference clocks	CS = 1 (PECL Input Clock)	2.0		AVCC – 0.4	V
I_{IH}	High level input current	V_{IH} = 2.4V			100	µA
I_{IL}	Low level input current	V_{IL} = 0.4V	–400			µA
V_{OH}	High level output voltage	I_{OH} = –60mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = +60mA			0.4	V

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
AC CHARACTERISTICS rise time, fall time and duty cycle are measured for a generic load; (see Load Conditions section).						
t_R	Rise time, LOAD [0-7] output	0.8 → 2.0V	150		1500	ps
t_F	Fall time, LOAD [0-7] output	2.0 → 0.8V	150		1500	ps
f_{IN}	Input frequency, CLK_{IN} pin		10		80	MHz
f_{OUT}	Output frequency , CLK [0-7] output	ML6510-80	10		80	MHz
		ML6510-130	10		130	MHz
f_{VCO}	PLL VCO operating frequency		80		160	MHz
DC	Output duty cycle	Measured at device load, at 1.5V	40		60	%
t_{JITTER}	Output jitter	Cycle-to-cycle		75		ps
		Peak-to-peak		150		ps
t_{LOCK}	PLL and deskew lock time	After programming is complete		11		ms
SKEW CHARACTERISTICS All skew measurements are made at the load, at 1.5V threshold each output load can vary independently within the specified range for a generic load (see Load Conditions section).						
t_{SKEWR}	Output to output rising edge skew, all clocks				500	ps
t_{SKEWF}	Output to output falling edge skew	Output clock frequency ≥ 50MHz			1.5	ns
t_{SKEWIO}	CLK_{IN} input to any LOAD [0-7] output rising edge skew	N = M = 0		600		ps
		N ≥ 2, M ≥ 2		1.25		ns
t_{RANGE}	Round trip delay CLKX to FBX pin; output CLK period = t_{CLK}	Output frequency < 50MHz Output frequency ≥ 50MHz	0 0		10 $t_{CLK}/2$	ns
t_{SKEWB}	Output-to-output rising edge skew, between matched loads	Providing first (see LOAD conditions) order matching order matching between outputs		250		ps
PART-TO-PART SKEW CHARACTERISTICS Skew measured at the loads, at 1.5V threshold. Reference clock output pins drive clock input pins of another ML6510.						
t_{PP1}	Total load-to-load skew between multiple chips interfaced with reference clock pins.	Slave chip CS = 1, CM = 1 and N = 0, M = 0; RCLK outputs to CLK_{IN} inputs distance less than 2"			TBD	ps
t_{PP2}	Total load-to-load skew between multiple chips interfaced with reference clock pins.	Slave chip CS = 1, CM = 1 and N ≥ 2, M ≥ 2; RCLK outputs to CLK_{IN} inputs distance less than 2"			TBD	ps
PROGRAMMING TIMING CHARACTERISTICS						
$t_{\overline{RESET}}$	$\overline{RESET}$ assertion pulse width		50			ns
t_{A1}	AUX mode MCLK high time		2000			ns
t_{A2}	AUX mode MCLK low time		2000			ns
t_{A3}	AUX mode MD_{OUT} data hold time		10			ns
t_{A4}	AUX mode MD_{OUT} data setup time		10			ns
t_{A5}	AUX mode MCLK period		5000			ns

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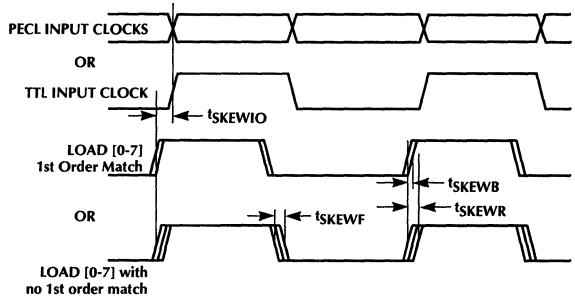
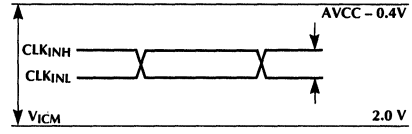
ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
PROGRAMMING TIMING CHARACTERISTICS (continued)						
t_{M1}	MAIN mode MCLK high time		900			ns
t_{M2}	MAIN mode MCLK low time		900			ns
t_{M3}	MAIN mode MCLK period		1800			ns
t_{M4}	MAIN mode MCLK to MD_{OUT} valid (EEPROM read time)				900	ns

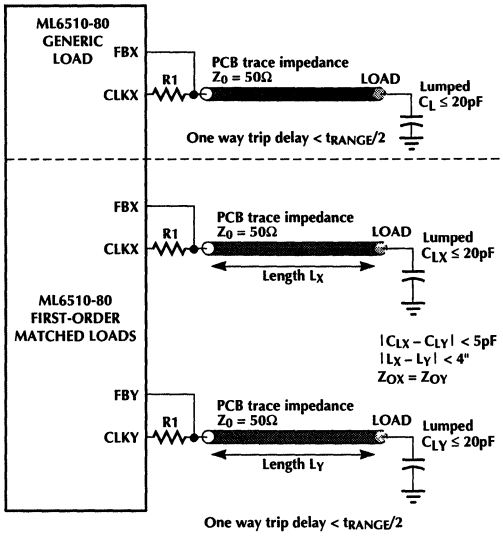
ML6510 configured with bit CM = 0:

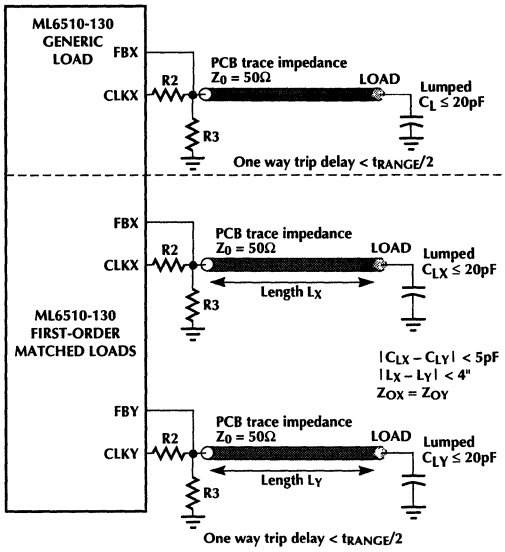


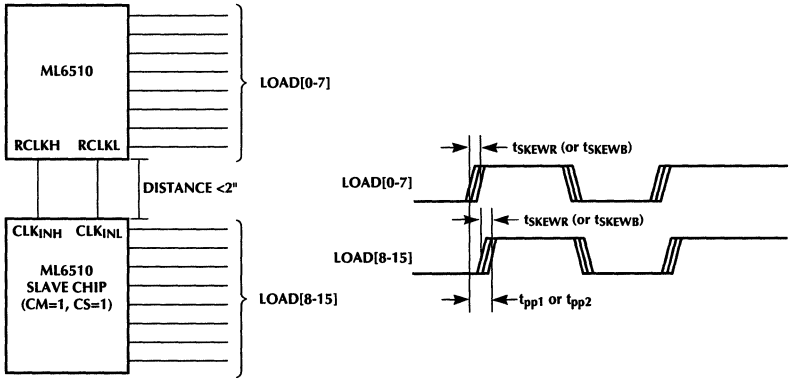


Note: All skew is measured at the device load input pin, NOT at the ML6510 clock output pin. Skew is always a positive number, regardless of which edge is leading and which is trailing.

AC/SKEW CHARACTERISTICS LOAD CONDITIONS







FUNCTIONAL DESCRIPTION

Micro Linear's ML6510 is the first clock chip to use a feedback mechanism to adaptively (on a real time basis), eliminate clock skew in high speed personal computer and workstation system designs. Figure 1 shows a basic configuration of the ML6510 in a system. The skew problem results due to the delaying of clock signals in the system, as shown in Figure 2. Clock skew results from variation in factors like trace length, PCB trace characteristics, load capacitance, parasitic capacitance, temperature and supply variations, etc. Figure 2 shows a representation of the clock skew problem from a timing perspective. It shows a worst case example where the clock signal is delayed so much that its rising edge completely misses the data it is intended to strobe. Using a clock deskew mechanism, this problem can be eliminated and the strobe with the appropriate setup and hold times with respect to the data bus can be generated.

The ML6510 has eight deskew buffers, each with its own independent the reflection and error correction circuit. The deskew buffer eliminates skew by using the reflection from a remote chip to measure the clock error and then corrects it by generating the appropriate skew to the clock output to compensate.

Eight individually deskewed copies of the clock are provided by the ML6510.

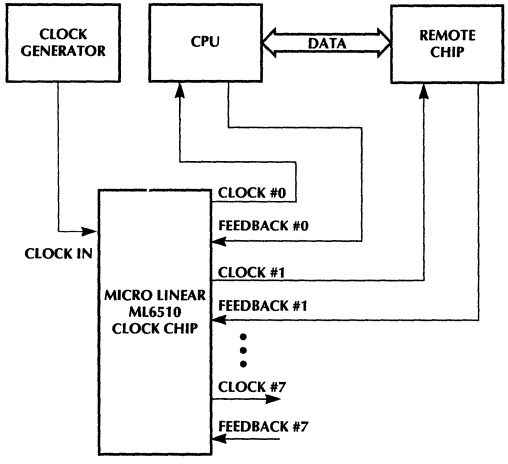


Figure 1. Basic System Configuration Using the ML6510.

The deskew buffers compensate internally for board-level skew caused by the PCB trace length variations and device load variations. This is accomplished by sensing the round trip delay via a reflected signal, and then delaying or advancing the clock edge so that all 8 output clocks arrive at their loads in phase. Each of the eight clock lines can have any length PCB trace (up to 5ns each way or 1/4th of the output clock period, whichever is smaller) and the device loads can vary from line to line. The ML6510 will automatically compensate for these variations, keeping the device load clocks in phase. Although ML6510 will compensate for skew caused by loading, excessive capacitive loading can cause rise/fall time degradation at the load. Cascading one ML6510 to another ML6510 should be done using the PECL reference clock outputs, to minimize part-to-part skew.

CLOCK REGENERATION

The programmable adaptive clock deskew can function in a clock regeneration mode to assist in building clock trees or to expand the number of deskewed clock lines. In this mode, it has the ability to do clock multiplication or division as well, while maintaining low skew between

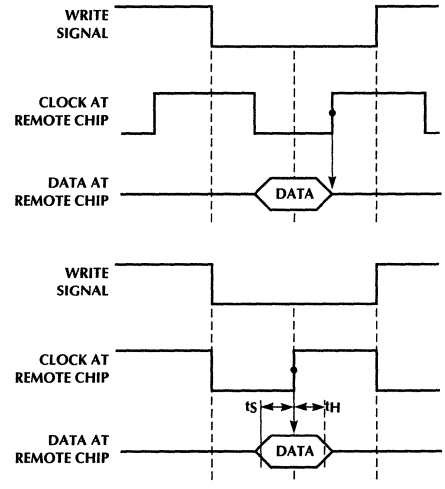


Figure 2. The Skew Problem.

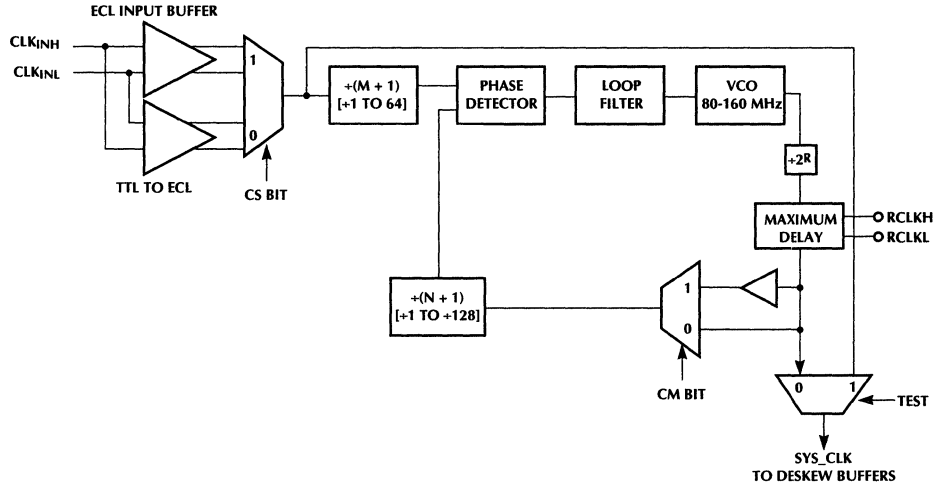


Figure 3. ML6510 Clock Generation Block Diagram.

input clock and output clocks. It can thus generate a 2x or 4x or 0.5x frequency multiplication or division from input to output (e.g. 33 MHz input, 66 MHz output or 66 MHz input, 33 MHz output, etc.). It also can generate a 1x frequency output. The VCO frequency is defined by:

$$f_{VCO} = f_{REF} \times \left[\frac{(N+1)\times 2^R}{(M+1)}\right]$$

and the output frequency is still given by:

$$f_{OUT} = f_{VCO}/2^R$$

R1	R0	INPUT/OUTPUT RANGE
0	0	80-130 MHz
0	1	40–80 MHz
1	0	20–40 MHz
1	1	10–20 MHz

Note: R implies R1, R0; for -80 version, Not valid· Defaults to R = 01

The VCO still must remain in the range 80–160 MHz, and the minimum phase detector input frequency is 625kHz = (80 MHz/128). Thus the product of (N + 1) and 2^R should be limited to 128:

$(N + 1) \times 2^R \leq 128$ to make sure that the phase detector inputs remain above the minimum frequency.

Example: Generating a 2x clock input frequency = 33 MHz

Set R = 01 (output range 40 – 80 MHz), N = 5 (0000101), M = 2 (000010), M/S = 0

$$f_{VCO} = f_{REF} \times \left[\frac{(N+1)\times 2^R}{(M+1)}\right] = 33MHz \times \left[\frac{6\times 2^1}{3}\right] = 132MHz$$

$$f_{OUT} = f_{VCO}/2^R = 132\ MHz/2^1 = 66\ MHz$$

Example: Generating a 1x clock Input frequency = 66 MHz

Set R = 01 (output range 40–80 MHz), set M = 0 (000000), N = 0 (0000000), M/S = 0

$$f_{VCO} = 66MHz \times \left[\frac{1\times 2^1}{1}\right] = 132MHz$$

$$f_{OUT} = f_{VCO}/2^R = 132\ MHz/2^1 = 66\ MHz$$

For doing frequency multiplication and division, keep M ≥ 2 and N ≥ 2 for the lowest skew between input clock and output clock. Several configurations for doing frequency multiplication and division are included in the 8 configurations stored in the on-chip ROM (see PROGRAMMING the ML6510).

ADAPTIVE DESKEW BUFFERS

Each copy of the clock is driven by an adaptive deskew buffer. The deskew buffer compensates for skew time automatically in accordance to the flight time delay it senses from the reflection on the transmission line.

Figure 4 shows the simplified functional block diagram of the deskew circuit. The phase of the sense signal and the driver signal is presented to a three-input phase comparator and compared with the reference signal. The phase comparator then controls the voltage controlled delay in the output drive line to match the delay of the fixed reference delay line. Therefore, the sum of the delay of the driver circuit, PCB trace delay, rise time delay at the load and the adjustable delay will always equal the fixed maximum delay.

The sense circuit has an internal level detect such that any skew caused by loading is also accounted for. Since the delay of the circuit is matched for the entire loop, the phase of all the drivers are in close alignment at the inputs of the load.

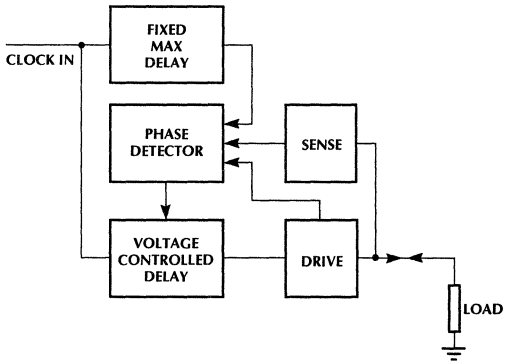


Figure 4. Deskew Circuit Block Diagram.

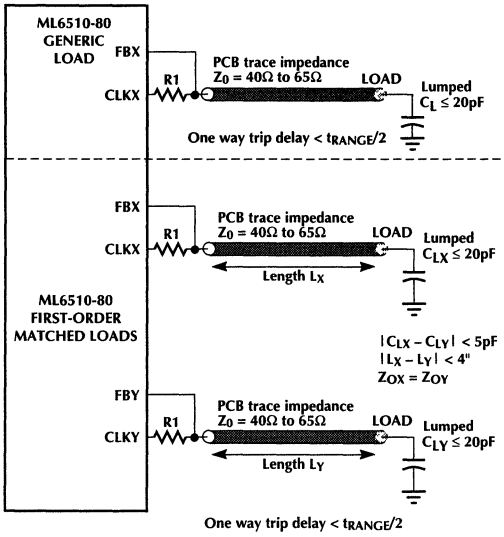
LOAD CONDITIONS

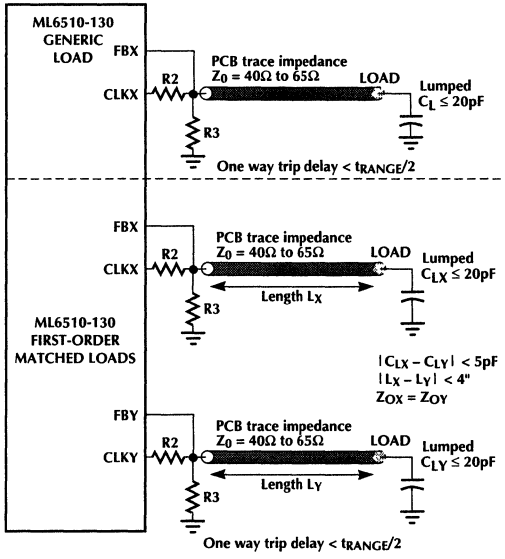
The ML6510 has been designed to drive the wide range of load conditions that are encountered in a high frequency system. The eight output clock loads can each vary within a range of trace length and lumped capacitive load, and the ML6510 will maintain the low skew characteristics specified in Electrical Characteristics. The clock skew can be further minimized by providing some first-order matching between any two loads that require particularly well-matched clocks.

The ML6510-80 produces a 5V swing at the load and requires a single external termination resistor for each output. The ML6510-130 produces a 3V swing at the load and requires two external termination resistors for each output. The FB input pin is connected to the other side of the termination resistor R1 or R2, with a short connection. Termination resistor valves should be chosen as follows:

$R1 = Z_0 \qquad R2 = 1.5 \times Z_0 \qquad R3 = 3 \times Z_0$

TRACE IMPEDANCE	RESISTOR VALUES		
Z0	R1	R2	R3
40Ω	40	60	120
50Ω	50	75	150
63Ω	63	95	189



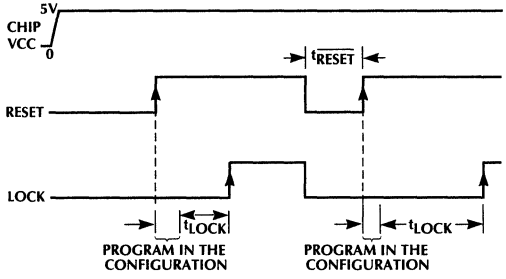


EXTERNAL INPUT CLOCKS

The external input clock to the ML6510 can be either a differential Pseudo-ECL clock or a single-ended TTL clock. This is selected using the CS bit in the serial shift register. For the single-ended TTL clock tie the CLK_{INH} and CLK_{INL} pins together. The ML6510 ensures that there is a well-defined phase difference between the input and output clocks.

$\overline{\text{RESET}}$ AND LOCK

When $\overline{\text{RESET}}$ is de-asserted, the internal programming logic will become active, loading in the configuration bits (see Programming the ML6510). Once the configuration is loaded, the PLL will lock onto the reference signal, and then the deskew blocks will adapt to the load conditions. When all eight output clocks are stable and deskewed, LOCK will be asserted. The asserted polarity of lock is high. Thus, LOCK can be used to indicate that the system is ready, or it can be used to drive the $\overline{\text{RESET}}$ input of another PACMan in a clock tree.



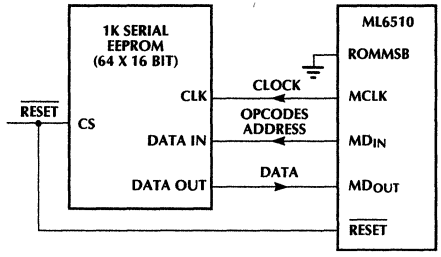
$\overline{\text{RESET}}$ may be reasserted at any time to reset the chip operations. Following a $\overline{\text{RESET}}$ assertion of valid pulse width (see Programming Electrical Characteristics), the ML6510 must again be loaded with a configuration, then it will re-lock and reassert lock when all eight clock outputs are stable and deskewed.

PROGRAMMING THE ML6510

The configuration of the ML6510 is programmed by loading 18 (ML6510-80) or 19 (ML6510-130) bits into the configuration shift register. To load these bits, the user has 3 options: MAIN, AUX or ROM modes. Which mode is used is determined by the logic level on the MD_{IN} pin when $\overline{RESET}$ is deasserted. If MD_{IN} is tied high, the ML6510 will assume AUX mode; if its tied low, ROM mode. If MD_{IN} is high-impedance (i.e. tied to the input of an EEPROM), it will assume MAIN mode.

1. MAIN Mode

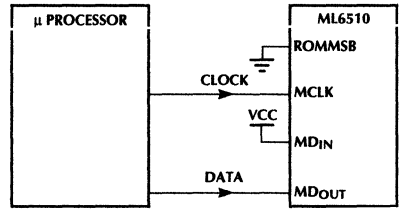
In this mode, the ML6510 will read the configuration bits from an external serial EEPROM, such as the 93C46, using the industry standard 3-wire serial I/O protocol. The serial EEPROM should be a 1K organized in 64 x 16 bits and the PACMan will read the configuration bits out of the two least significant 16-bit words. To use this mode, simply connect the EEPROM serial data input pin to MD_{IN} (ML6510 pin 19), the EEPROM serial data output pin to MD_{OUT} (ML6510 pin 20), and the EEPROM serial data clock pin to MCLK (ML6510 pin 21) and CS pin for the EEPROM should be tied to the $\overline{RESET}$ signal. After power up, when $\overline{RESET}$ is deasserted, the ML6510 will automatically generate the address and clock to read out the configuration bits. Refer MAIN Mode waveform in Figure 5.



MAIN Mode Configuration.

2. AUX Mode

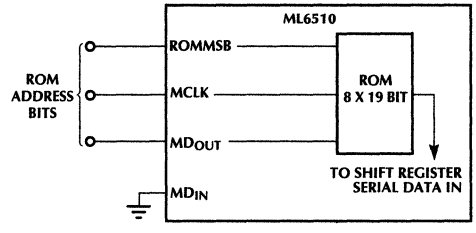
When MD_{IN} is tied to VCC, programming the ML6510 will occur via the AUX Mode. This mode shifts the configuration bits into the shift register directly from the MD_{OUT} pin. The first 18 (ML6510-80) or 19 (ML6510-130) clock rising edges provided externally on the MCLK pin after $\overline{RESET}$ is deasserted will be used to load the shift register data, which should be provided on the MD_{OUT} pin. See figure 6.



AUX Mode Configuration.

3. ROM Mode

When MD_{IN} is tied to GND, programming the ML6510 will occur via the ROM Mode. This mode reads the configuration bits directly from an on chip ROM. The selection of one of the eight preset configuration codes is accomplished by means of the pins ROMMSB, MCLK and MD_{OUT} as shown in Tables 1 and 2. The TEST mode configuration (code 7) is enabled when the TEST bit is set. In this mode the PLL is bypassed for low frequency testing. Codes 0-2 are used when the ML6510 clock inputs are driven from another PACMan's reference clock outputs. Code 3 is used when zero phase error is desired between input and load clocks.



ROM Mode Configuration.

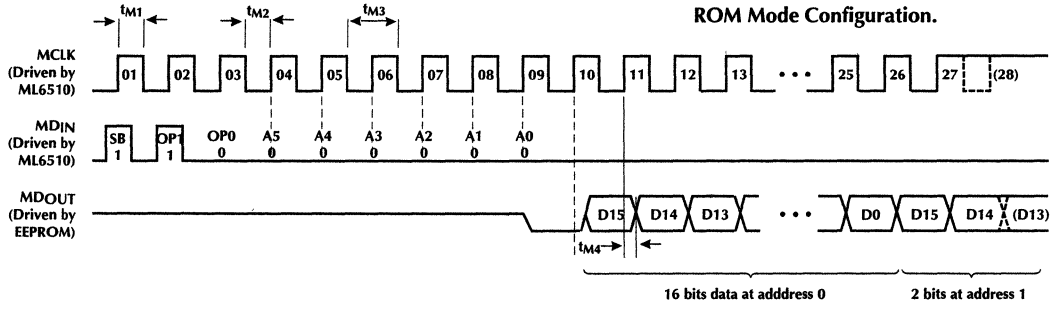


Figure 5. MAIN Mode Waveforms.

TABLE 1: ML6510-80 ROM CODES

CODE	DESCRIPTION	SELECTION BITS			INPUT FREQ (MHz)	OUTPUT FREQ (MHz)	CONFIGURATION CODE					
		ROMMSB	MCLK	MD_{OUT}			CS	CM	R1, R0	M	N	TEST
0	PECL Input Clock, 1x mode	0	0	0	40-80	40-80	1	1	01	0	0	0
1	PECL Input Clock, 0.5x mode	0	0	1	40-80	20-40	1	1	10	5	2	0
2	PECL Input Clock, 2x mode	0	1	0	20-40	40-80	1	1	01	2	5	0
3	PECL Input Clock, 1x mode	0	1	1	40-80	40-80	1	0	01	0	0	0
4	TTL Input Clock, 1x mode	1	0	0	40-80	40-80	0	0	01	0	0	0
5	TTL Input Clock, 0.5x mode	1	0	1	40-80	20-40	0	0	10	5	2	0
6	TTL Input Clock, 2x mode	1	1	0	20-40	40-80	0	0	01	2	5	0
7	TEST mode, TTL Input clock	1	1	1	0-50	0-50	0	—	—	—	—	1

TABLE 2: ML6510-130 ROM CODES

CODE	DESCRIPTION	SELECTION BITS			INPUT FREQ (MHz)	OUTPUT FREQ (MHz)	CONFIGURATION CODE						
		ROMMSB	MCLK	MD_{OUT}			CS	CM	R1, R0	M	N	DDSK	TEST
0	PECL Input Clock, 1x mode	0	0	0	80-130	80-130	1	1	00	0	0	0	0
1	PECL Input Clock, 0.5x mode	0	0	1	80-160	40-80	1	1	01	5	2	0	0
2	PECL Input Clock, 2x mode	0	1	0	40-65	80-130	1	1	00	2	5	0	0
3	PECL Input Clock, 1x mode	0	1	1	80-130	80-130	1	0	00	0	0	0	0
4	TTL Input Clock, 1x mode	1	0	0	80-130	80-130	0	0	00	0	0	0	0
5	TTL Input Clock, 0.5x mode	1	0	1	80-130	40-65	0	0	01	5	2	0	0
6	TTL Input Clock, 2x mode	1	1	0	40-65	80-130	0	0	00	2	5	0	0
7	TEST mode, TTL Input clock	1	1	1	0-50	0-50	0	—	—	—	—	—	1

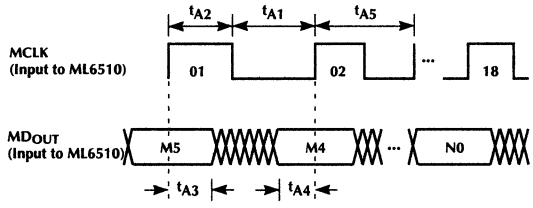
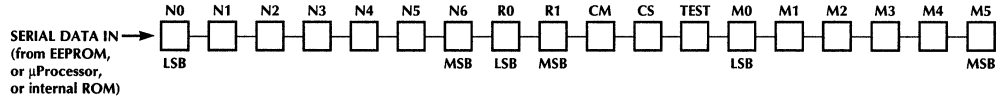


Figure 6. AUX Mode Waveform.

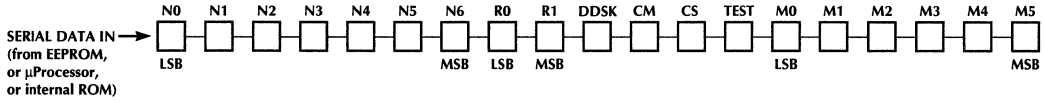
REGISTER DEFINITIONS

REGISTER	SIZE	FUNCTION
N	7 bit	This register is used to define the ratio for the desired frequency of the primary clock.
R	2 bit	This register defines the frequency of the primary clocks, CLK [0-7].
CM	1 bit	Set CM = 1 when the PECL input reference clock is from another 6510 reference clock output. Set CM = 0 if the clock reference is TTL or PECL from an external source and minimum phase error between input and output is desired.
CS	1 bit	CS = 0 selects TTL input clock, CS = 1 selects PECL input clock.
TEST	1 bit	When set to 1, the PLL is bypassed for low frequency testing.
M	6 bit	This register is used to define the ratio for the desired frequency of the primary clock.
DDSK	1 bit	When DDSK is set to 1, deskew is disabled. The chip will provide low skew clocks at the chip output pins, but trace length variations will not be compensated. When DDSK is set to 0, normal deskew will provide low skew clocks at the loads. This bit is only for ML6510-130.

ML6510-80 SHIFT REGISTER CHAIN



ML6510-130 SHIFT REGISTER CHAIN

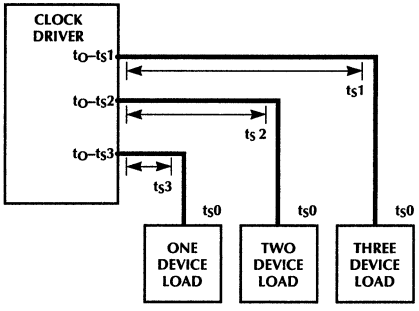


APPLICATIONS

ZERO SKEW CLOCK GENERATION

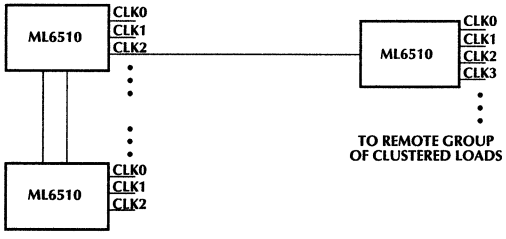
The most advantageous feature of using PACMan is its ability to deliver multiple copies of the clock to the load with very low skew. Because of its unique ability in deskewing, trace length and load consideration are no longer critical in board design.

Because of the unique deskewing scheme, neither the trace length nor the device loads need to be equal. This is true for loads, <20pF. Higher loads can be driven if they are placed close to the clock chip, to guarantee signal integrity.



LOW SKEW CLOCK DISTRIBUTION

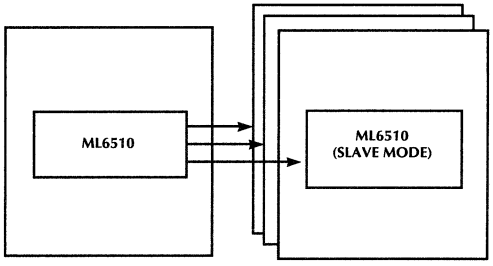
Clock distribution design is usually not a trivial task, especially when multiple clock chips are needed. By using closely grouped PACMans, 16 or more clock lines can be created with low part-to-part skew. Additional groups of clocks can be clustered and driven from deskewed clock lines, to minimize the number of long-distance clock lines.



BOARD TO BOARD SYNCHRONIZATION

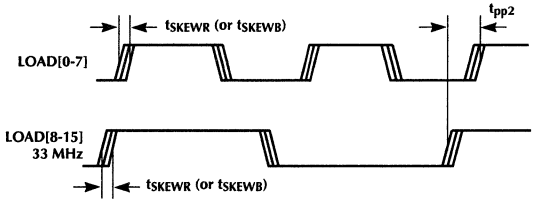
Distribution of the synchronous clock could present significant difficulty at high frequency. With the system clock generated by the ML6510, a zero skew clock delivery to a backplane is now possible. By using the ML6510 slave chip or the ML6510 in slave mode at the receiver end, a near zero delay clock link can be accomplished between the mother board and the satellite boards.

Because the PACMan has frequency doubling capability, a lower frequency signal can be used to route across a back plane.



EXAMPLE CONFIGURATION

Shown in Figure 7 is an example configuration using two ML6510 chips in tandem to generate eight 66 MHz clocks and eight 33MHz low-skew clocks from a 66MHz input reference. This requires only the termination resistors. Configurations are loaded from the internal ROM. PCB traces 0 to 15 are each 50Ω impedance and the load capacitances C_{L0}-C_{L15} are 0 to 20pF each. No trace length matching is required among separate clock outputs. All traces are shown with a series termination at the output.



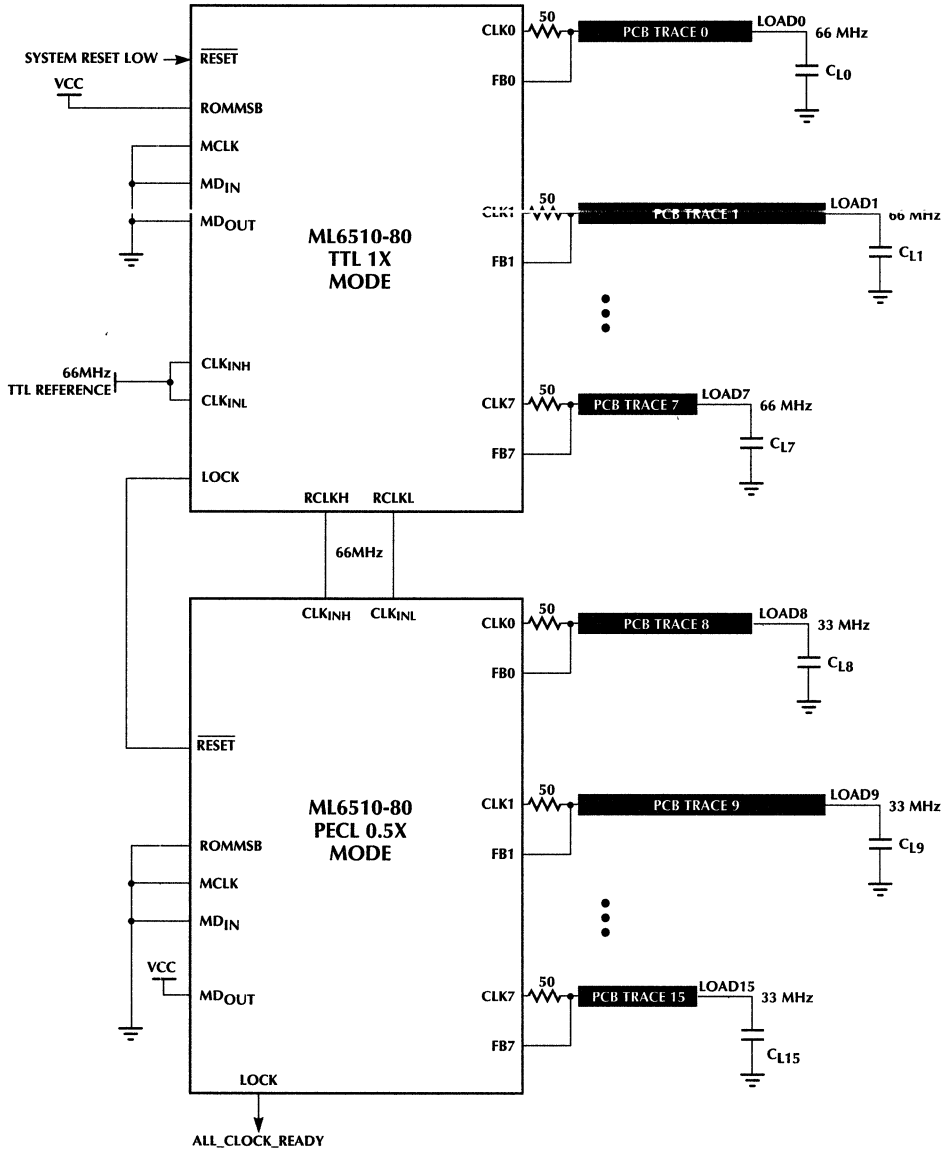


Figure 7. Example use of two ML6510-80 to generate multiple frequency clocks. First ML6510-80 generates eight 66MHz clocks while second ML6510-80 takes 66MHz small-swing reference from the first chip and generates eight 33MHz clocks.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6510CQ-80	0°C to +70°C	44-pin PLCC (Q44)
ML6510CQ-130	0°C to +70°C	44-pin PLCC (Q44)

High Speed Dual Quad Buffer/Line Driver

GENERAL DESCRIPTION

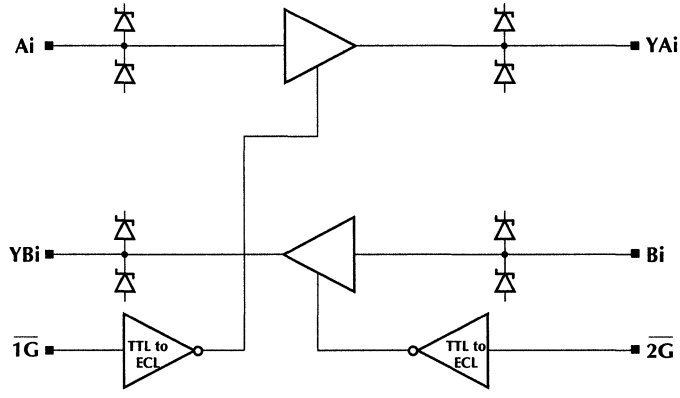
The ML65244 is a BiCMOS, non-inverting dual quad buffer/line driver. Its 8-channels support a propagation delay of 1.5ns, while driving a 50pF load @ 50 MHz switching frequency and have tri-state outputs making them ideal for very high speed bus oriented applications. This increased performance is provided without a significant increase in power dissipation, thus increasing system reliability. The ML65244 high speed buffer uses a unique analog implementation over the conventional inverter approaches and hence does not waste precious nanoseconds waiting for signals to settle. It achieves its low and predictable delay as the output closely follows the input, including the rise and fall times. The ML65244 follows the pinout and functionality of the industry standard FCT244 buffer/line driver and is intended for applications where propagation delay is critical to the system design. The ML65244 is available in SOIC and QSOP packages.

Note: This part was previously numbered ML6582.

FEATURES

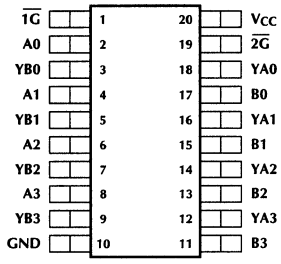
- Fastest buffer/line driver — 1.5ns propagation delay
- Fast 8 bit TTL level buffer/line driver with tri state capability on the output (two 4-bit sections)
- TTL compatible input and output levels
- Schottky diode clamps on all inputs to handle undershoot and overshoot
- Onboard schottky diodes minimizes noise
- Reduced output swing of 0 – 4.1 volts
- Ground bounce controlled outputs, typically less than 400mV (See Figure 1)
- Small area, low profile, 20-pin QSOP and industry standard SOIC packages
- Industry standard FCT244 type pinout
- Applications involve, high speed cache memory, main memory, processor bus buffering and graphics cards

BLOCK DIAGRAM



PIN CONFIGURATION

20-Pin SOIC, QSOP



TOP VIEW

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
Ai	I	Data Bus A
YAi	O	Data Bus A
Bi	I	Data Bus B
YBi	O	Data Bus B
$\overline{1G}$	I	Output Enable for data bus A
$\overline{2G}$	I	Output Enable for data bus B
GND	I	Signal Ground
V_{CC}	I	+ 5V supply

FUNCTION TABLE

$\overline{1G}/\overline{2G}$	Ai/Bi	YAi/YBi
High	X	Tri-state
Low	Low	Low
Low	High	High

6

ABSOLUTE MAXIMUM RATINGS

Supply voltage ..... –0.3 to + 7VDC
DC Output voltage ..... –0.3 to + 7VDC
DC Input voltage ..... –0.3 to + 7VDC
AC Input voltage (PW < 20ns) ..... –3.0V
Storage temperature ..... –65°C to 150°C
Junction temperature ..... 150°C
Max output sink current per pin 120mA
Thermal Impedance (θ_{JA})
SOIC ..... 90°C/W
QSOP ..... 95°C/W

TYPICAL CAPACITANCE

Pins	SOIC	QSOP	Units
1 & 19	4	4	pF
10 & 20	6	6	pF
2–9, 11–18	8	8	pF

Note: Capacitance is based on characterization data only

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for: V_{CC} = 5.0 ± 5%V, T_A = 0°C to 70°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS (C_{LOAD} = 50pF, R_{LOAD} = 500Ω)						
t_{PLH}, t_{PHL}	Propagation delay	Ai to YAi, Bi to YBi (Note 5)		1.3	1.5	ns
t_{OE}	Output enable time $\overline{1G}$, $\overline{2G}$ to YAi/YBi			7	10	ns
t_{OD}	Output disable time $\overline{1G}$, $\overline{2G}$ to YAi/YBi	(Note 3)			10	ns
DC ELECTRICAL CHARACTERISTICS (C_{LOAD} = 50pF, R_{LOAD} = ∞)						
V_{IH}	Input high voltage	Logic HIGH	2.0			V
V_{IL}	Input low voltage	Logic LOW			0.8	V
I_{IH}	Input high current	Per pin, TTL logic high input		0.5	1.5	mA
I_{IL}	Input low current	Per pin, TTL logic low input		2.4	3.5	mA
I_{HI-Z}	Tri-state output current	V_{CC} = 5.25V, 0 < V_{IN} < V_{CC}			5	µA
I_{OS}	Short circuit current	V_{CC} = 5.25V, V_O = GND (Notes 1 & 3)	–60		–225	mA
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IN} = 18mA (Note 3)		–0.7	–1.2	V
V_{OH}	Output high voltage	V_{CC} = 4.75V, I_{OH} = 100µA (Notes 2 & 4)	2.4			V
V_{OL}	Output low voltage	V_{CC} = 4.75V, I_{OL} = 25mA (Notes 2 & 4)			0.55	V
V_{OFF}	V_{IN} – V_{OUT} per buffer	V_{CC} = 4.75V (Note 2)	0	100	200	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = 5.25V, Freq = 0Hz, Inputs/outputs open		55	80	mA

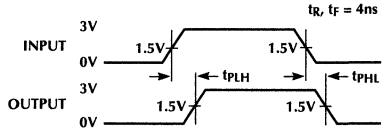
Note 1: Not more than one output should be shorted for more than a second

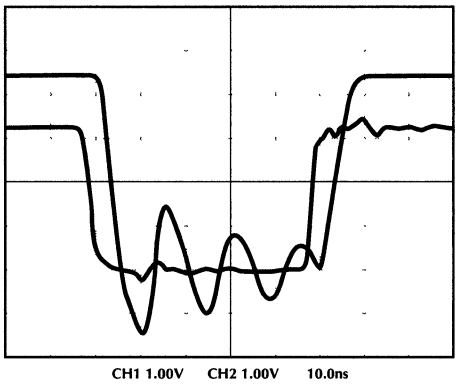
Note 2: This is a true analog buffer. In the linear region, the output tracks the input with an offset (V_{OFF}). For V_{OH}, V_{IN} = 2.6V, $V_{OH\ MIN}$ includes V_{OFF}. For V_{OL}, V_{IN} = 0V, $V_{OL\ MAX}$ includes V_{OFF}.

Note 3: Guaranteed by design only.

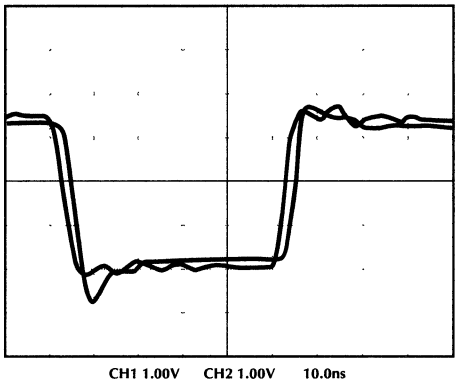
Note 4: See figure 2 for I_{OH} versus V_{OH} and I_{OL} versus V_{OL} data.

Note 5: One line switching, see figure 3, t_{PLH}, t_{PHL} versus C_L.





74FCT244



ML65244

Figure 1. Ground Bounce Comparison, Four Outputs Switching into 50pF Loads.

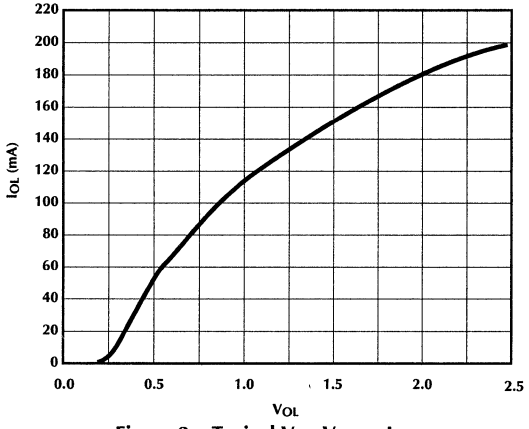


Figure 2a. Typical V_{OL} Versus I_{OL} for One Buffer Output.

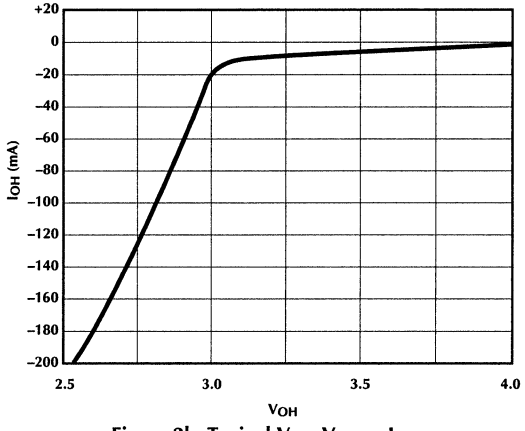


Figure 2b. Typical V_{OH} Versus I_{OH} for One Buffer Output.

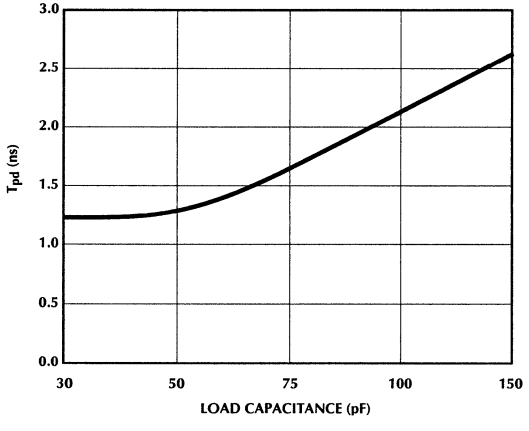


Figure 3. Propagation Delay (t_{PLH}, t_{PHL}) Versus Load Capacitance, One Output Switching.

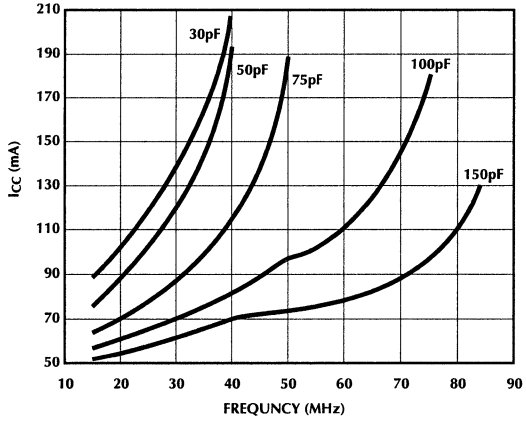


Figure 4. I_{CC} Versus Frequency for Various Load Capacitances, Four Outputs Switching.

6

FUNCTIONAL DESCRIPTION

The ML65244 is a very high speed, 8-bit, non-inverting buffer/line driver with tri-state outputs which are ideally suited for bus-oriented applications. It achieves a 1.5ns propagation delay into a 50pF load at 50 MHz because of the fact that the ML65244 supports an analog design approach (a true unity gain buffer), as compared to the conventional digital inverter type approaches. The ML65244 achieves its low and predictable propagation delay by having its output follow its input with a small offset of a couple of hundred millivolts. The output rise and fall times will closely match those of the input waveform. All inputs and outputs have schottky clamp diodes for handling undershoot or overshoot noise suppression in un-terminated applications. All outputs have ground bounce suppression (which is typically of the order of 400mV), high drive output capability with almost immediate response to the input signal and low output skew. The I_{OL} current drive spec of a buffer/line driver is often interpreted as a measure of the buffer/line drivers ability to sink current in a dynamic sense. This may be true for CMOS buffer/line drivers, but it is not true for the ML65244. This is because the ML65244's sink or source current capability depends on the difference between the output and the input. The ML65244 can sink or source more than 100 milliamps to a load capacitor when the load is switching because in this case, the difference between the input and output is large. I_{OL} is only significant as a DC specification and in the case of the ML65244 it is 25mA. The output enable ($\overline{1G}$ & $\overline{2G}$) inputs enable the selected port for output or tri-state.

The ML65244 follows the pinout and functionality of the industry standard FCT 244 series of buffer/line drivers and is intended to replace them in designs where the propagation delay is a critical part of the system consideration. The user needs to exercise caution in their design as the ML65244 will load an active bus when V_{CC} is removed from the device.

ARCHITECTURAL DESCRIPTION

Dual quad buffer/line drivers are 8 bit logic devices that are capable of driving load capacitances several times larger than their input capacitance. The ML65244 is configured so that the Ai inputs go to the YAi outputs, with the output enable controlled by $\overline{1G}$. Similarly $\overline{2G}$ controls the Bi inputs which go to the YBi outputs.

Until now, these buffer/line drivers were typically implemented in CMOS logic and made to be TTL compatible by sizing the input devices appropriately. In order to buffer large capacitances with CMOS logic, it is necessary to cascade an even number of inverters, each successive inverter larger than the preceding, eventually leading to an inverter that will drive the required load capacitance at the required frequency. Each inverter stage represents an additional delay in the gating process because in order for a single gate to switch, the input must slew more than half of the supply voltage. The best of these CMOS buffers has managed to drive a 50pF load capacitance with a delay of 3.2ns.

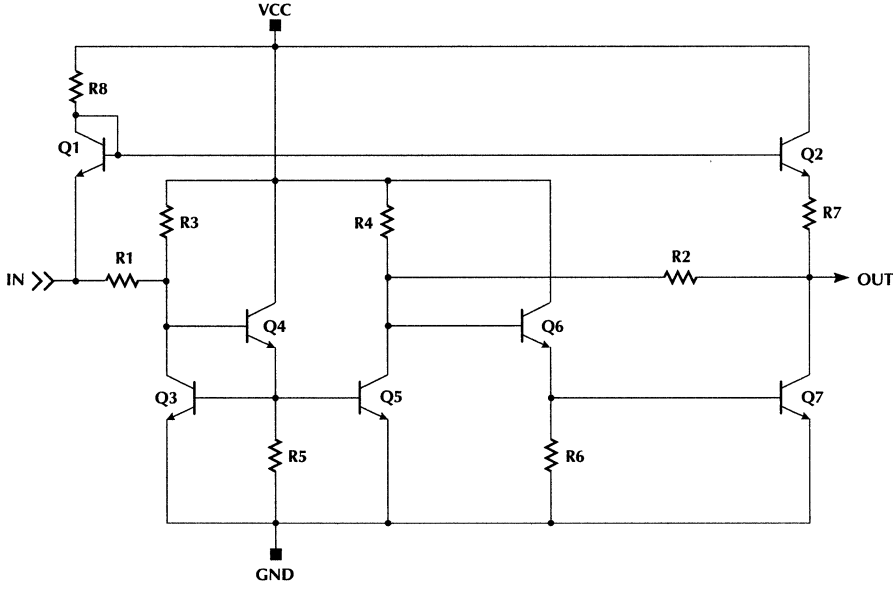


Figure 5. One buffer cell of the ML65244

Micro Linear has produced an dual quad buffer/line driver with a delay less than 1.5ns by using a unique circuit architecture that does not require cascaded logic gates. The ML65244 uses feedback techniques to produce an output that follows the input. If the output voltage is not close to the input then the feedback will source enough current to the load capacitance to correct the discrepancy.

The basic architecture of the ML65244 is shown in Figure 5. It is implemented on a 1.5µm BiCMOS process. However, in this particular circuit, all of the active devices are NPNs — the fastest devices available in the process.

In this circuit, there are two paths to the output. One path sources current to the load capacitance when the signal is asserted and the other path sinks current from the output when the signal is negated.

The assertion path is the emitter follower path consisting of the level shift transistor Q1, the output transistor Q2 and the bias resistor R8. It sources current to the output through the 75Ω resistor R7 which is bypassed by another NPN (not shown) during fast input transients. The negation path is a current differencing opamp connected in a follower configuration. The active components in this amplifier are transistors Q3–Q7. R3–R6 are bias resistors, and R1 and R2 are the feedback resistors. The key to understanding the operation of the current differencing opamp is to know that the current in transistors Q3 and Q5 are the same at all times and that the voltages at the bases of Q4 and Q6 are roughly the same. If the output is higher than the input, then an error current will flow through R2. This error current will flow into the base of Q6 and be multiplied by β squared to the collector of Q7 thus closing the loop. The larger the discrepancy between the output and input, the larger the feedback current, and the harder Q7 sinks current from the load capacitor.

A number of MOSFETs that are not shown in Figure 5 have been used in the ML65244. These MOSFETs were used to tri-state dormant buffers. For instance, the feedback resistors R1 and R2 were implemented as resistive transmission gates to ensure that disabled buffers do not load the lines they are connected to. Similarly, there is a PMOS in series with R8 that is normally on but shuts off for disable. Other MOSFETs have been included to ensure that disabled buffers consume no power.

TERMINATION

R7 in Figure 5 also acts as a termination resistance. This 75Ω resistor is in series with the output and therefore helps suppress noise caused by transmission line effects such as reflections from mismatched impedances. Systems designers using CMOS transceivers commonly have to use external resistors in series with each transceiver output to suppress this noise. Hence, systems designers using the ML65244 may not have to use these external resistors.

APPLICATIONS

There are a wide variety of existing and future needs for an extremely fast buffers in high speed processor system designs like Pentium, PowerPC, Mips, Sparc, Alpha and other RISC processors. The applications are either in the cache memory area or the main memory (DRAM) area. Besides these, the fast buffer could find applications in high speed graphics and multimedia applications. The high capacitive loading due to multiplexed address lines on the system bus demand external buffers to take up the excess drive current. The needed current to skew the transitions between rise and fall times must be done without adding excessive propagation delay. The devices are equipped with schottky diodes to clean up ringing from overshoot and undershoot caused by reflections in un-terminated board traces.

ORDERING INFORMATION

PART NUMBER	SPEED	TEMPERATURE RANGE	PACKAGE
ML65244CS	1.5ns	0°C to +70°C	20-Pin SOIC (S20)
ML65244CK	1.5ns	0°C to +70°C	20-Pin QSOP (K20)

High Speed Octal Buffer Transceiver

GENERAL DESCRIPTION

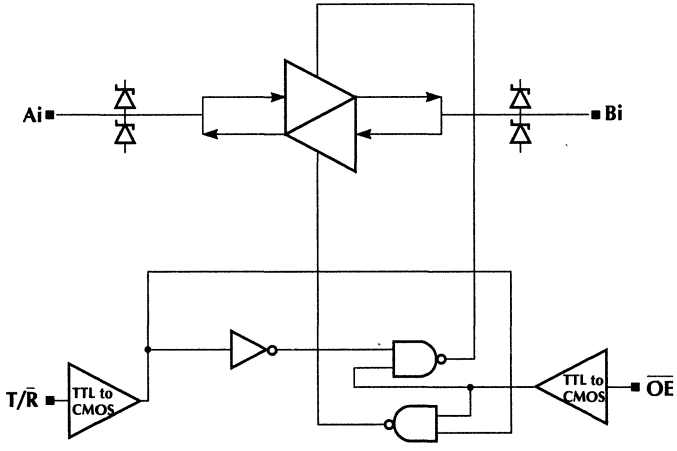
The ML65245 is a BiCMOS, non-inverting octal transceiver. Its 8-channels support a propagation delay of 1.5ns, while driving a 50pF load @ 50 MHz switching frequency and have tri-state outputs making them ideal for very high speed bus oriented applications. This increased performance is provided without a significant increase in power dissipation, thus increasing system reliability. The ML65245 high speed buffer uses a unique analog implementation over the conventional inverter approaches and hence does not waste precious nanoseconds waiting for signals to settle.
It achieves its low and predictable delay as the output closely follows the input, including the rise and fall times. The ML65245 follows the pinout and functionality of the industry standard FCT family of transceivers and is intended for applications where propagation delay is critical to the system design. The ML65245 is available in SOIC and QSOP packages.

Note: This part was previously numbered ML6580.

FEATURES

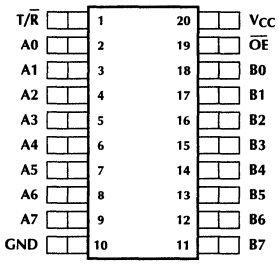
- Fastest transceiver — 1.5ns propagation delay
- Fast 8-bit TTL level transceiver with tri-state capability on the output
- TTL compatible input and output levels
- Schottky diode clamps on all inputs to handle undershoot and overshoot
- Onboard schottky diodes minimizes noise
- Reduced output swing of 0 – 4.1 volts
- Ground bounce controlled outputs, typically less than 400mV (See Figure 1)
- Small area, low profile, 20-pin QSOP and industry standard SOIC packages
- Industry standard FCT245 type pinout
- Applications involve, high speed cache memory, main memory, processor bus buffering and graphics cards

BLOCK DIAGRAM



PIN CONFIGURATION

20-Pin SOIC, QSOP



TOP VIEW

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
Ai	I/O	Data Bus A
Bi	I/O	Data Bus B
T/$\overline{R}$	I	Direction select
$\overline{OE}$	I	Output Enable
GND	I	Signal Ground
V_{CC}	I	+ 5V supply

FUNCTION TABLE

$\overline{OE}$	T/$\overline{R}$	A	B	Function
High	Don't care	Tri-state	Tri-state	Disable
Low	Low	Output	Input	Bus B to Bus A
Low	High	Input	Output	Bus A to Bus B

6

ABSOLUTE MAXIMUM RATINGS

Supply voltage ..... –0.3 to + 7VDC
DC Output voltage ..... –0.3 to + 7VDC
DC Input voltage ..... –0.3 to + 7VDC
AC Input voltage (PW < 20ns) ..... –3.0V
Storage temperature ..... –65°C to 150°C
Junction temperature ..... 150°C
Max output sink current per pin 120mA
Thermal Impedance (θ_{JA})
SOIC ..... 90°C/W
QSOP ..... 95°C/W

TYPICAL CAPACITANCE

Pins	SOIC	QSOP	Units
1 & 19	4	4	pF
10 & 20	6	6	pF
2–9, 11–18	8	8	pF

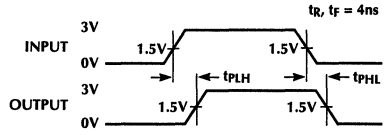
Note: Capacitance is based on characterization data only

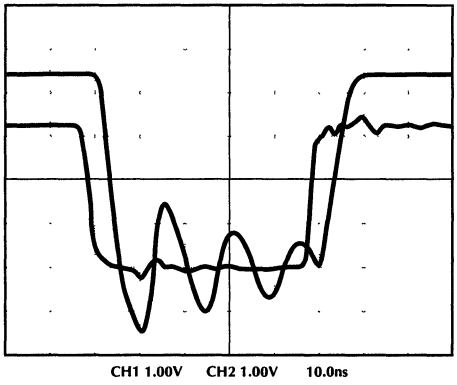
ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for: V_{CC} = 5.0 ± 5%V, T_A = 0°C to 70°C

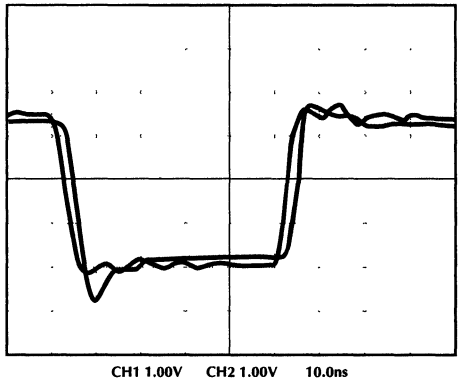
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS (C_{LOAD} = 50pF, R_{LOAD} = 500Ω)						
t_{PLH}, t_{PHL}	Propagation delay	Ai to/from Bi (Note 5)		1.3	1.5	ns
t_{OE}	Output enable time $\overline{OE}$, T/$\overline{R}$ to Ai/Bi			7	10	ns
t_{OD}	Output disable time $\overline{OE}$, T/$\overline{R}$ to Ai/Bi	(Note 3)			10	ns
DC ELECTRICAL CHARACTERISTICS (unless otherwise stated C_{LOAD} = 50pF, R_{LOAD} = ∞)						
V_{IH}	Input high voltage	Logic HIGH	2.0			V
V_{IL}	Input low voltage	Logic LOW			0.8	V
I_{IH}	Input high current	Per pin, TTL logic high input		0.5	1.5	mA
I_{IL}	Input low current	Per pin, TTL logic low input		2.4	3.5	mA
I_{HI-Z}	Tri-state output current	V_{CC} = 5.25V, 0 < V_{IN} < V_{CC}			5	µA
I_{OS}	Short circuit current	V_{CC} = 5.25V, V_O = GND (Notes 1 & 3)	–60		–225	mA
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IN} = 18mA (Note 3)		–0.7	–1.2	V
V_{OH}	Output high voltage	V_{CC} = 4.75V, I_{OH} = 100µA (Notes 2 & 4)	2.4			V
V_{OL}	Output low voltage	V_{CC} = 4.75V, I_{OL} = 25mA (Notes 2 & 4)			0.55	V
V_{OFF}	V_{IN} – V_{OUT} per buffer	V_{CC} = 4.75V (Note 2)	0	100	200	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = 5.25V, f = 0Hz, Inputs/outputs open		55	80	mA

Note 1: Not more than one output should be shorted for more than a second.
Note 2: This is a true analog buffer. In the linear region, the output tracks the input with an offset (V_{OFF}). For V_{OH}, V_{IN} = 2.6V, $V_{OH\ MIN}$ includes V_{OFF}. For V_{OL}, V_{IN} = 0V, $V_{OL\ MAX}$ includes V_{OFF}
Note 3: Guaranteed by design only.
Note 4: See figure 2 for I_{OH} versus V_{OH} and I_{OL} versus V_{OL} data.
Note 5: One line switching, see figure 3, t_{PLH}, t_{PHL} versus C_L.





74FCT245



ML65245

Figure 1. Ground Bounce Comparison, Four Outputs Switching into 50pF Loads.

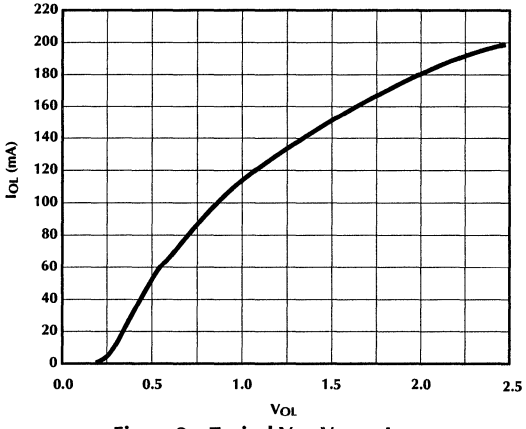


Figure 2a. Typical V_{OL} Versus I_{OL} for One Buffer Output.

Figure 2b. Typical V_{OH} Versus I_{OH} for One Buffer Output.

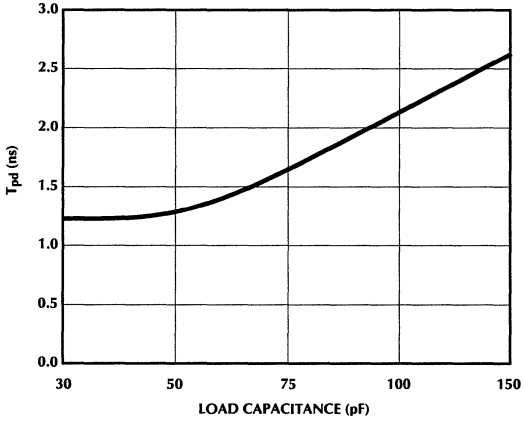


Figure 3. Propagation Delay (t_{PLH}, t_{PHL}) Versus Load Capacitance, One Output Switching.

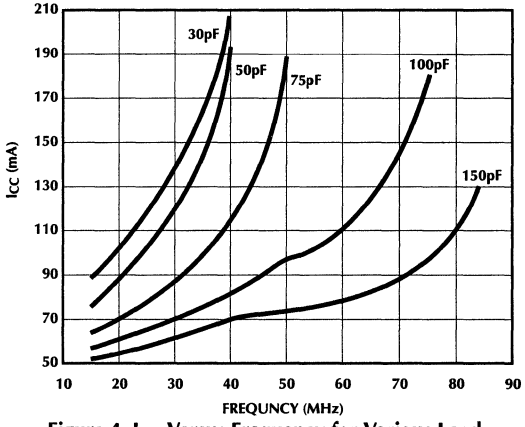


Figure 4. I_{CC} Versus Frequency for Various Load Capacitances, Four Outputs Switching.

FUNCTIONAL DESCRIPTION

The ML65245 is a very high speed, 8-bit, non-inverting transceiver with tri-state outputs which are ideally suited for bus-oriented applications. It achieves a 1.5ns propagation delay into a 50pF load at 50 MHz because of the fact that the ML65245 supports an analog design approach (a true unity gain buffer), as compared to the conventional digital inverter type approaches. The ML65245 achieves its low and predictable propagation delay by having its output follow its input with a small offset of a couple of hundred millivolts. The output rise and fall times will closely match those of the input waveform. All inputs and outputs have schottky clamp diodes for handling undershoot or overshoot noise suppression in un-terminated applications. All outputs have ground bounce suppression (which is typically of the order of 400mV), high drive output capability with almost immediate response to the input signal and low output skew. The I_{OL} current drive spec of a transceiver is often interpreted as a measure of the transceivers ability to sink current in a dynamic sense. This may be true for CMOS transceivers, but it is not true for the ML65245. This is because the ML65245's sink or source current capability depends on the difference between the output and the input. The ML65245 can sink or source more than 100 milliamps to a load capacitor when the load is switching because in this case, the difference between the input and output is large. I_{OL} is only significant as a DC specification and in the case of the ML65245 it is 25mA. The transmit/receive (T/$\overline{R}$) input determines the direction of data flow either from A to B or B to A, while the output enable ($\overline{OE}$) input enables the selected port for output or tri-state. The ML65245 follows the pinout and functionality of the industry standard FCT series of transceivers and is intended to replace them in designs where the propagation delay is a critical part of the system consideration. The user needs to exercise caution in their design as the ML65245 will load an active bus when V_{CC} is removed from the device.

ARCHITECTURAL DESCRIPTION

Octal transceivers are 8 bit logic devices that are capable of driving load capacitances several times larger than their input capacitance. These transceivers have eight inputs labeled A and eight labeled B. They can be programmed to transmit from A to B or from B to A or to go into a disable state in which both A and B are high impedance.

Until now, these transceivers were typically implemented in CMOS logic and made to be TTL compatible by sizing the input devices appropriately. In order to buffer large capacitances with CMOS logic, it is necessary to cascade an even number of inverters, each successive inverter larger than the preceding, eventually leading to an inverter that will drive the required load capacitance at the required frequency. Each inverter stage represents an additional delay in the gating process because in order for a single gate to switch, the input must slew more than half of the supply voltage. The best of these CMOS buffers has managed to drive a 50pF load capacitance with a delay of 3.2ns.

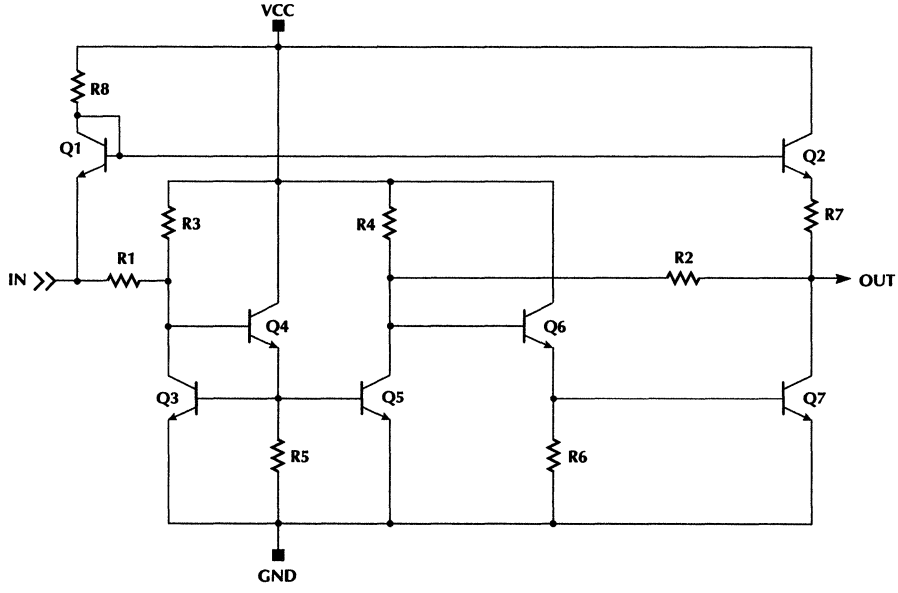


Figure 5. One buffer cell of the ML65245

Micro Linear has produced an octal transceiver with a delay less than 1.5ns by using a unique circuit architecture that does not require cascaded logic gates. The ML65245 uses feedback techniques to produce an output that follows the input. If the output voltage is not close to the input then the feedback will source enough current to the load capacitance to correct the discrepancy.

The basic architecture of the ML65245 is shown in Figure 5. It is implemented on a 1.5µm BiCMOS process. However, in this particular circuit, all of the active devices are NPNs — the fastest devices available in the process.

In this circuit, there are two paths to the output. One path sources current to the load capacitance when the signal is asserted and the other path sinks current from the output when the signal is negated.

The assertion path is the emitter follower path consisting of the level shift transistor Q1, the output transistor Q2 and the bias resistor R8. It sources current to the output through the 75Ω resistor R7 which is bypassed by another NPN (not shown) during fast input transients. The negation path is a current differencing opamp connected in a follower configuration. The active components in this amplifier are transistors Q3–Q7. R3–R6 are bias resistors, and R1 and R2 are the feedback resistors. The key to understanding the operation of the current differencing opamp is to know that the current in transistors Q3 and Q5 are the same at all times and that the voltages at the bases of Q4 and Q6 are roughly the same. If the output is higher than the input, then an error current will flow through R2. This error current will flow into the base of Q6 and be multiplied by β squared to the collector of Q7 thus closing the loop. The larger the discrepancy between the output and input, the larger the feedback current, and the harder Q7 sinks current from the load capacitor.

A number of MOSFETs that are not shown in Figure 5 have been used in the ML65245. These MOSFETs were used to tri-state dormant buffers. For instance, the feedback resistors R1 and R2 were implemented as resistive transmission gates to ensure that disabled buffers do not load the lines they are connected to. Similarly, there is a PMOS in series with R8 that is normally on but shuts off for disable. Other MOSFETs have been included to ensure that disabled buffers consume no power.

TERMINATION

R7 in figure 5 also acts as a termination resistance. This 75Ω resistor is in series with the output and therefore helps suppress noise caused by transmission line effects such as reflections from mismatched impedances. Systems designers using CMOS transceivers commonly have to use external resistors in series with each transceiver output to suppress this noise. Hence, systems designers using the ML65245 may not have to use these external resistors.

APPLICATIONS DESCRIPTION

There are a wide variety of existing and future needs for an extremely fast buffer/transceiver in high speed processor system designs like Pentium, PowerPC, Mips, Sparc, Alpha and other RISC processors. The applications are either in the cache memory area or the main memory (DRAM) area. Besides these, the fast buffer could find applications in high speed graphics and multimedia applications. The high capacitive loading due to multiplexed address lines on the system bus demand external buffers to take up the excess drive current. The needed current to skew the transitions between rise and fall times must be done without adding excessive propagation delay. The devices are equipped with schottky diodes to clean up ringing from overshoot and undershoot caused by reflections in un-terminated board traces.

APPLICATION 1

BUFFERING MAIN MEMORY

An example main memory application is shown in Figure 6 for the Intel PCI chipset with the Pentium processor. This discussion is only intended as a general reference. For details please refer to the appropriate Intel documentation. This system has a 66MHz host processor and a 33MHz main (DRAM) memory bus. The main memory row and column addresses (RAS & CAS) and write enable (WE) signals are provided by the PCMC chip (PCI Cache and Memory Controller) device. The DRAM SIIMs put a heavy load on the PCMC and must be buffered. Three buffered copies of the address signals and write enable are required to drive the six row array. The ML65245 provides the buffered signals and gives extra margin to be able to use slower memory modules instead of the normally required 50/70ns. The burst read (page-hit) performance is typically 7-4-4-4 at 66MHz for 70ns DRAMs or 6-3-3-3 at 66MHz for 50ns DRAMs. This usually translates to significantly higher costs. With the speed improvement offered by the ML65245, a 6-3-3-3 burst with 60ns DRAMs may be achievable. The extra margin comes from the 1.5ns propagation delay of the buffer. External resistor arrays are not necessary. This becomes even more of an issue in future PCI systems which may operate at 80MHz and beyond.

This kind of main memory application for the ML65245 could potentially extend to other kinds of processor systems which do not require latched buffering. Figure 7 shows a main memory design example with the ML65245 for the Mips R4X00 RISC processor based system without secondary cache. The faster propagation delay essentially translates to a faster main memory access.

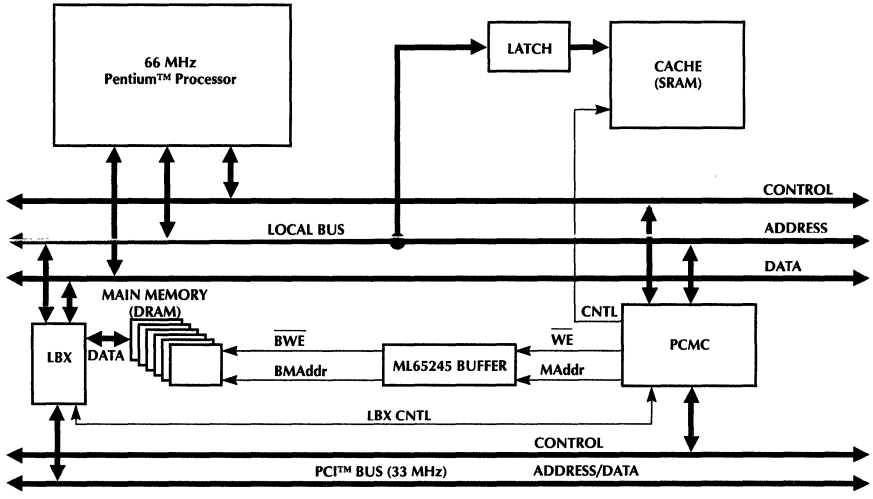


Figure 6. ML65245 in a main memory application for a Pentium based system. The high drive and low propagation delay are essential to buffer the write enable and memory addresses to the main memory SIIMs.

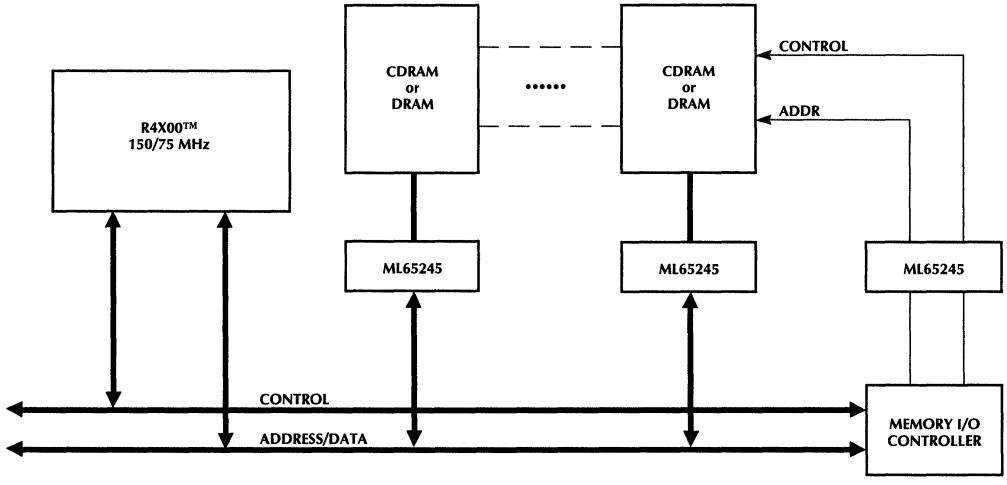


Figure 7. The ML65245 in a non-cache, main memory RISC application. The main memory could be DRAM or CacheDRAM. The ML65245 can be used as a data I/O transceiver as well as an address buffer, as shown above.

APPLICATION 2

BUFFERING CACHE MEMORY

With the advent of higher power operating systems like Windows NT, NeXT Step, Cairo, etc., RISC processor designs are gaining momentum like Mips R4000 series. In these systems the interface to secondary cache has a critical path in the address and bus control pins. As shown in Figure 8, any time (propagation delay) saved in the buffer translates to a slower SRAM access requirement and hence less expensive. Currently the secondary cache bus operates at 75MHz. In order to meet the 13ns cycle time, the SRAM and Buffer must meet a total access time of 12ns. With the ML65245 for a buffer, the required SRAM access time is 10ns at 75MHz and 18ns at 50MHz. With the fastest FCT buffer available (3.2ns), the SRAM access time required in the above scenarios would be 8ns and 15ns respectively. This access time difference could mean the difference between using expensive BiCMOS SRAMs versus less expensive CMOS SRAMs.

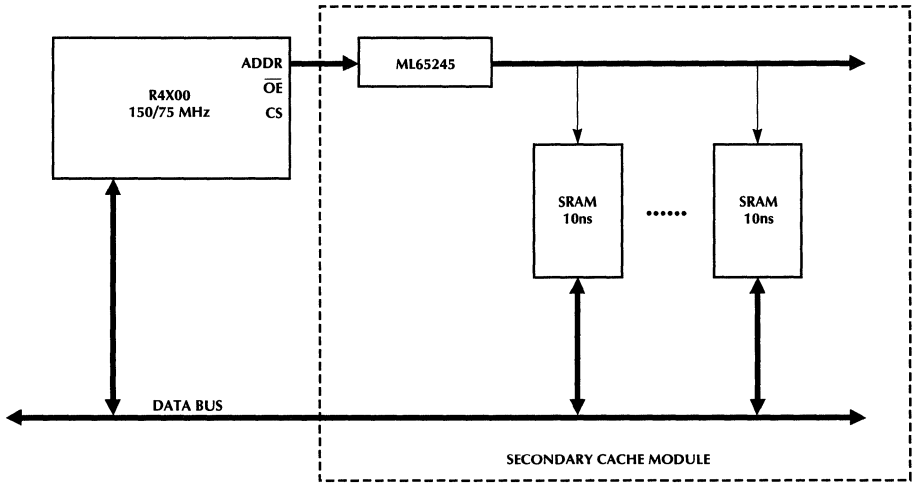


Figure 8. ML65245 in a R4X00 secondary cache application. The address and control signal path is critical and loads the R4X00 output pins. The ML65245 buffer alleviates the load on the R4X00 and because it is fast, slower, less expensive SRAMs can be used.

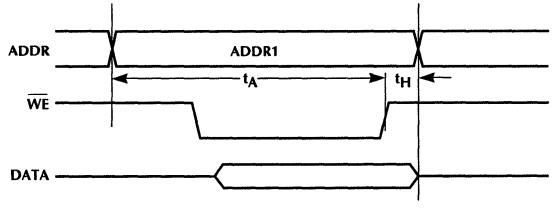


Figure 9. Timing waveform showing address buffer switching rate (t_A + t_H) in a secondary cach module.

ORDERING INFORMATION

PART NUMBER	SPEED	TEMPERATURE RANGE	PACKAGE
ML65245CS	1.5ns	0°C to +70°C	20-Pin SOIC (S20)
ML65245CK	1.5ns	0°C to +70°C	20-Pin QSOP (K20)

ML65541

High Speed Octal Buffer/Line Driver

GENERAL DESCRIPTION

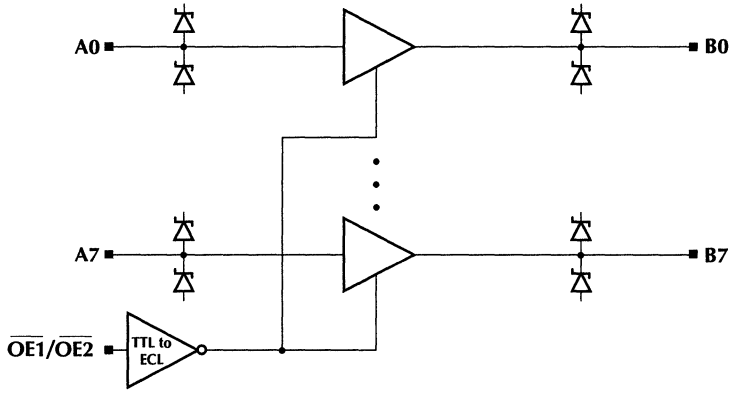
The ML65541 is a BiCMOS, non-inverting octal buffer/line driver. Its 8-channels support a propagation delay of 1.5ns, while driving a 50pF load @ 50 MHz switching frequency and have tri-state outputs making them ideal for very high speed bus oriented applications. This increased performance is provided without a significant increase in power dissipation, thus increasing system reliability. The ML65541 high speed buffer uses a unique analog implementation over the conventional inverter approaches and hence does not waste precious nanoseconds waiting for signals to settle. It achieves its low and predictable delay as the output closely follows the input, including the rise and fall times. The ML65541 follows the pinout and functionality of the industry standard FCT541 family of buffer/line driver and is intended for applications where propagation delay is critical to the system design. The ML65541 is available in SOIC and QSOP packages.

Note: This part was previously numbered ML6581.

FEATURES

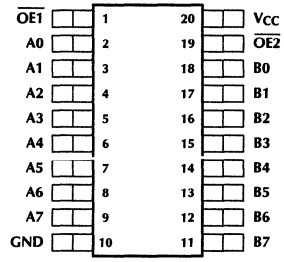
- Fastest buffer/line driver — 1.5ns propagation delay
- Fast 8-bit TTL level buffer/line driver with tri-state capability on the output
- TTL compatible input and output levels
- Schottky diode clamps on all inputs to handle undershoot and overshoot
- Onboard schottky diodes minimizes noise
- Reduced output swing of 0 – 4.1 volts
- Ground bounce controlled outputs, typically less than 400mV (See Figure 1)
- Small area, low profile, 20-pin QSOP and industry standard SOIC packages
- Industry standard FCT541 type pinout
- Applications involve, high speed cache memory, main memory, processor bus buffering and graphics cards

BLOCK DIAGRAM



PIN CONFIGURATION

20-Pin SOIC, QSOP



TOP VIEW

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
Ai	I	Data Bus A
Bi	O	Data Bus B
$\overline{OE1}$ & $\overline{OE2}$	I	Output Enable
GND	I	Signal Ground
V_{CC}	I	+ 5V supply

FUNCTION TABLE

$\overline{OE1}/\overline{OE2}$	A	B
High	X	Tri-state
Low	Low	Low
Low	High	High

ABSOLUTE MAXIMUM RATINGS

Supply voltage ..... –0.3 to + 7VDC
DC Output voltage ..... –0.3 to + 7VDC
DC Input voltage ..... –0.3 to + 7VDC
AC Input voltage (PW < 20ns) ..... –3.0V
Storage temperature ..... –65°C to 150°C
Junction temperature ..... 150°C
Max output sink current per pin 120mA
Thermal Impedance (θ_{JA})
SOIC ..... 90°C/W
QSOP ..... 95°C/W

TYPICAL CAPACITANCE

Pins	SOIC	QSOP	Units
1 & 19	4	4	pF
10 & 20	6	6	pF
2–9, 11–18	8	8	pF

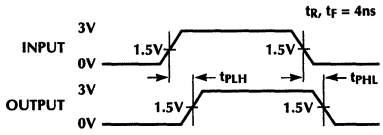
Note: Capacitance is based on characterization data only

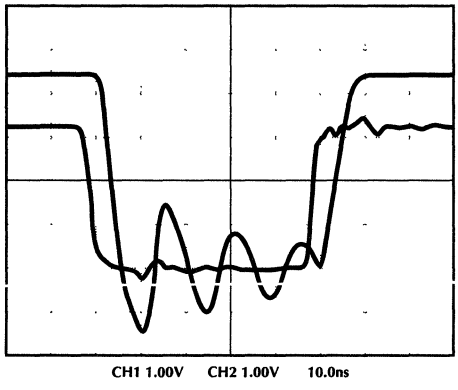
ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for: V_{CC} = 5.0 ± 5%V, T_A = 0°C to 70°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS (C_{LOAD} = 50pF, R_{LOAD} = 500Ω)						
t_{PLH}, t_{PHL}	Propagation delay	Ai to Bi (Note 5)		1.3	1.5	ns
t_{OE}	Output enable time $\overline{OE1}$, $\overline{OE2}$ to Bi			7	10	ns
t_{OD}	Output disable time $\overline{OE1}$, $\overline{OE2}$ to Bi	(Note 3)			10	ns
DC ELECTRICAL CHARACTERISTICS (C_{LOAD} = 50pF, R_{LOAD} = ∞)						
V_{IH}	Input high voltage	Logic HIGH	2.0			V
V_{IL}	Input low voltage	Logic LOW			0.8	V
I_{IH}	Input high current	Per pin, TTL logic high input		0.5	1.5	mA
I_{IL}	Input low current	Per pin, TTL logic low input		2.4	3.5	mA
I_{HI-Z}	Tri-state output current	V_{CC} = 5.25V, 0 < V_{IN} < V_{CC}			5	µA
I_{OS}	Short circuit current	V_{CC} = 5.25V, V_O = GND (Notes 1 & 3)	–60		–225	mA
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IN} = 18mA (Note 3)		–0.7	–1.2	V
V_{OH}	Output high voltage	V_{CC} = 4.75V, I_{OH} = 100µA (Notes 2 & 4)	2.4			V
V_{OL}	Output low voltage	V_{CC} = 4.75V, I_{OL} = 25mA (Notes 2 & 4)			0.55	V
V_{OFF}	V_{IN} – V_{OUT} per buffer	V_{CC} = 4.75V (Note 2)	0	100	200	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = 5.25V, f = 0Hz, Inputs/outputs open		55	80	mA

Note 1: Not more than one output should be shorted for more than a second.
Note 2: This is a true analog buffer. In the linear region, the output tracks the input with an offset (V_{OFF}). For V_{OH}, V_{IN} = 2.6V, $V_{OH\ MIN}$ includes V_{OFF}. For V_{OL}, V_{IN} = 0V, $V_{OL\ MAX}$ includes V_{OFF}
Note 3: Guaranteed by design only.
Note 4: See figure 2 for I_{OH} versus V_{OH} and I_{OL} versus V_{OL} data.
Note 5: One line switching, see figure 3, t_{PLH}, t_{PHL} versus C_L.





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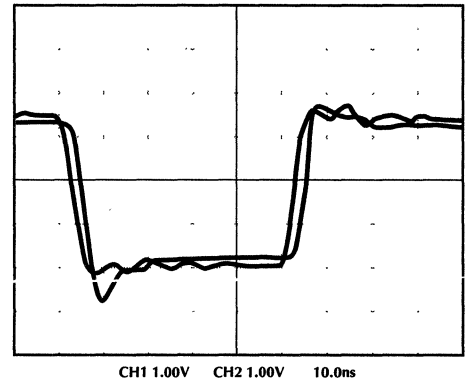

ML65541

Figure 1. Ground Bounce Comparison, Four Outputs Switching into 50pF Loads.

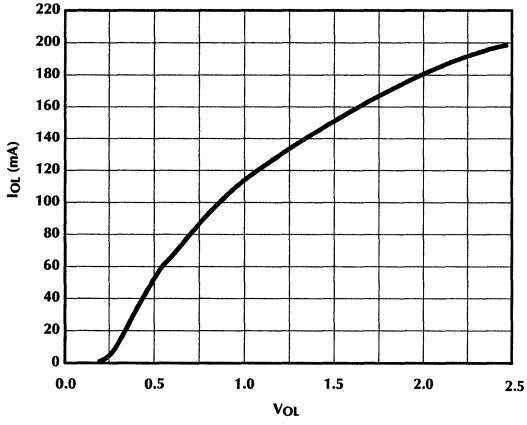

Figure 2a. Typical V_{OL} Versus I_{OL} for One Buffer Output.

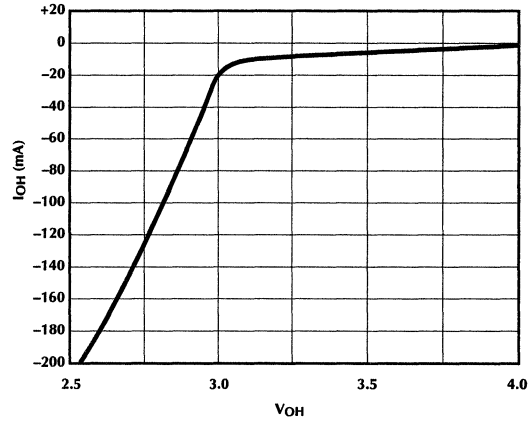

Figure 2b. Typical V_{OH} Versus I_{OH} for One Buffer Output.

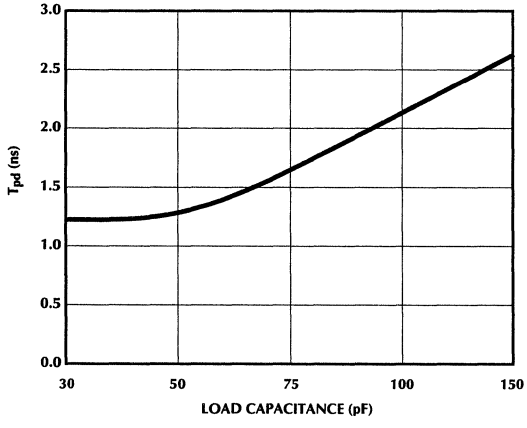

Figure 3. Propagation Delay (t_{PLH}, t_{PHL}) Versus Load Capacitance, One Output Switching.

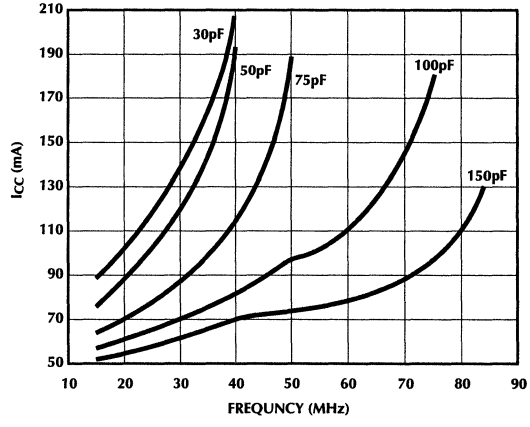

Figure 4. I_{CC} Versus Frequency for Various Load Capacitances, Four Outputs Switching.

FUNCTIONAL DESCRIPTION

The ML65541 is a very high speed, 8-bit, non-inverting buffer/line driver with tri-state outputs which are ideally suited for bus-oriented applications. It achieves a 1.5ns propagation delay into a 50pF load at 50 MHz because of the fact that the ML65541 supports an analog design approach (a true unity gain buffer), as compared to the conventional digital inverter type approaches. The ML65541 achieves its low and predictable propagation delay by having its output follow its input with a small offset of a couple of hundred millivolts. The output rise and fall times will closely match those of the input waveform. All inputs and outputs have schottky clamp diodes for handling undershoot or overshoot noise suppression in un-terminated applications. All outputs have ground bounce suppression (which is typically of the order of 400mV), high drive output capability with almost immediate response to the input signal and low output skew. The I_{OL} current drive spec of a buffer/line driver is often interpreted as a measure of the buffer/line drivers ability to sink current in a dynamic sense. This may be true for CMOS buffer/line drivers, but it is not true for the ML65541. This is because the ML65541's sink or source current capability depends on the difference between the output and the input. The ML65541 can sink or source more than 100 milliamps to a load capacitor when the load is switching because in this case, the difference between the input and output is large. I_{OL} is only significant as a DC specification and in the case of the ML65541 it is 25mA. The output enable ($\overline{OE1}$ & $\overline{OE2}$) inputs enables the selected port for output or tri-state. The ML65541 follows the pinout and functionality of the industry standard FCT 541 series of buffer/line drivers and is intended to replace them in designs where the propagation delay is a critical part of the system consideration. The user needs to exercise caution in their design as the ML65541 will load an active bus when V_{CC} is removed from the device.

ARCHITECTURAL DESCRIPTION

Octal buffer/line drivers are 8 bit logic devices that are capable of driving load capacitances several times larger than their input capacitance. These buffer/line drivers have eight inputs labeled A and eight outputs labeled B.

Until now, these buffer/line drivers were typically implemented in CMOS logic and made to be TTL compatible by sizing the input devices appropriately. In order to buffer large capacitances with CMOS logic, it is necessary to cascade an even number of inverters, each successive inverter larger than the preceding, eventually leading to an inverter that will drive the required load capacitance at the required frequency. Each inverter stage represents an additional delay in the gating process because in order for a single gate to switch, the input must slew more than half of the supply voltage. The best of these CMOS buffers has managed to drive a 50pF load capacitance with a delay of 3.2ns.

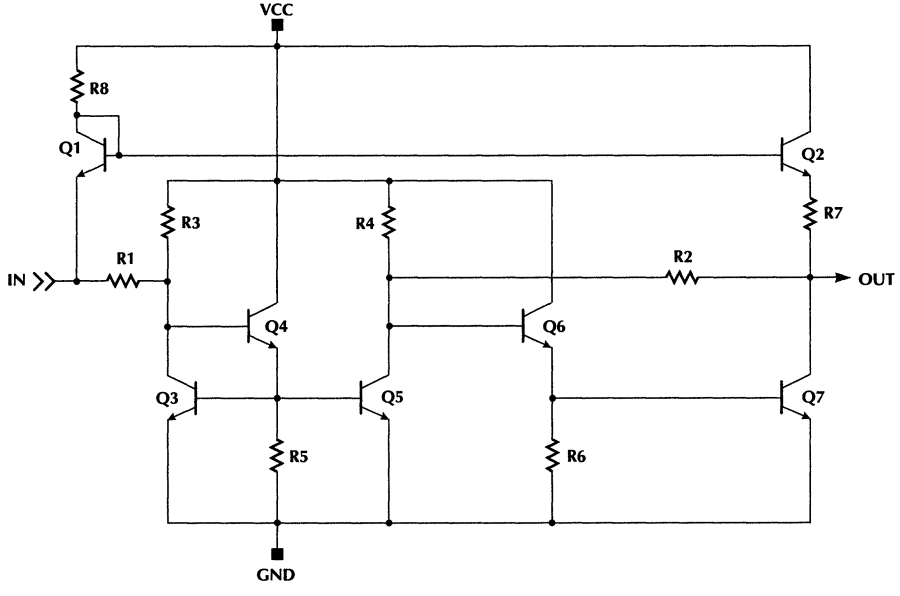

Figure 5. One buffer cell of the ML65541

Micro Linear has produced an octal buffer/line driver with a delay less than 1.5ns by using a unique circuit architecture that does not require cascaded logic gates. The ML65541 uses feedback techniques to produce an output that follows the input. If the output voltage is not close to the input then the feedback will source enough current to the load capacitance to correct the discrepancy.

The basic architecture of the ML65541 is shown in Figure 5. It is implemented on a 1.5µm BiCMOS process. However, in this particular circuit, all of the active devices are NPNs — the fastest devices available in the process.

In this circuit, there are two paths to the output. One path sources current to the load capacitance when the signal is asserted and the other path sinks current from the output when the signal is negated.

The assertion path is the emitter follower path consisting of the level shift transistor Q1, the output transistor Q2 and the bias resistor R8. It sources current to the output through the 75Ω resistor R7 which is bypassed by another NPN (not shown) during fast input transients. The negation path is a current differencing opamp connected in a follower configuration. The active components in this amplifier are transistors Q3–Q7. R3–R6 are bias resistors, and R1 and R2 are the feedback resistors. The key to understanding the operation of the current differencing opamp is to know that the current in transistors Q3 and Q5 are the same at all times and that the voltages at the bases of Q4 and Q6 are roughly the same. If the output is higher than the input, then an error current will flow through R2. This error current will flow into the base of Q6 and be multiplied by β squared to the collector of Q7 thus closing the loop. The larger the discrepancy between the output and input, the larger the feedback current, and the harder Q7 sinks current from the load capacitor.

A number of MOSFETs that are not shown in Figure 5 have been used in the ML65541. These MOSFETs were used to tri-state dormant buffers. For instance, the feedback resistors R1 and R2 were implemented as resistive transmission gates to ensure that disabled buffers do not load the lines they are connected to. Similarly, there is a PMOS in series with R8 that is normally on but shuts off for disable. Other MOSFETs have been included to ensure that disabled buffers consume no power.

TERMINATION

R7 in Figure 5 also acts as a termination resistance. This 75Ω resistor is in series with the output and therefore helps suppress noise caused by transmission line effects such as reflections from mismatched impedances. Systems designers using CMOS transceivers commonly have to use external resistors in series with each transceiver output to suppress this noise. Hence, systems designers using the ML65541 may not have to use these external resistors.

APPLICATIONS

There are a wide variety of existing and future needs for an extremely fast buffers in high speed processor system designs like Pentium, PowerPC, Mips, Sparc, Alpha and other RISC processors. The applications are either in the cache memory area or the main memory (DRAM) area. Besides these, the fast buffer could find applications in high speed graphics and multimedia applications. The high capacitive loading due to multiplexed address lines on the system bus demand external buffers to take up the excess drive current. The needed current to skew the transitions between rise and fall times must be done without adding excessive propagation delay. The devices are equipped with schottky diodes to clean up ringing from overshoot and undershoot caused by reflections in un-terminated board traces.

ORDERING INFORMATION

PART NUMBER	SPEED	TEMPERATURE RANGE	PACKAGE
ML65541CS	1.5ns	0°C to +70°C	20-Pin SOIC (S20)
ML65541CK	1.5ns	0°C to +70°C	20-Pin QSOP (K20)

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Hot-Insertable Active SCSI Terminator

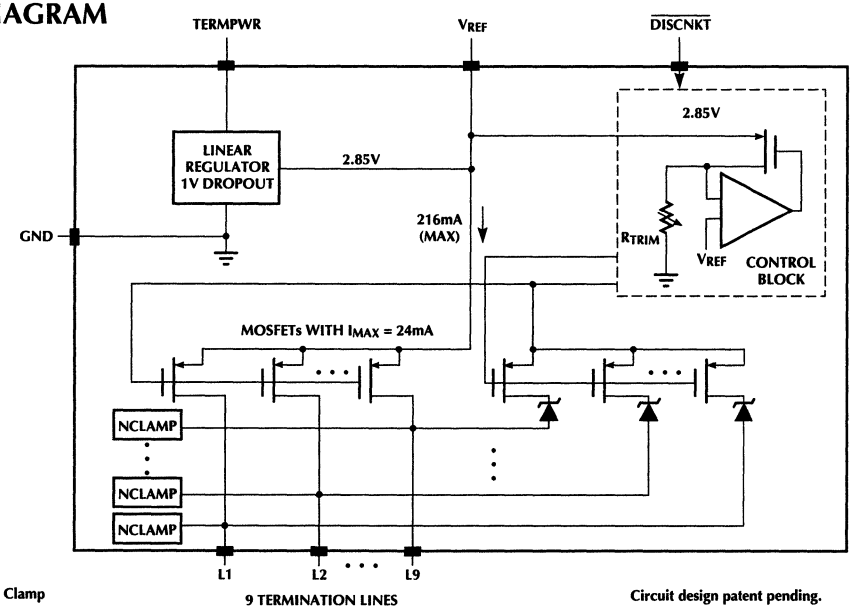
GENERAL DESCRIPTION

The ML6599 BiCMOS SCSI terminator provides active termination in a SCSI system with single-ended drivers and receivers, in full compliance with the SCSI-1, SCSI-2 and SCSI-3 recommendations. It provides a 2.85V reference through an internal 1V dropout linear regulator. Active SCSI termination helps the system designer to effectively control analog transmission line effects like ringing, noise, crosstalk, ground bounce, etc. In addition it provides support for hot insertability on the SCSI bus. The desired V-I characteristics for signal negation requires that the terminator source 0–24mA while maintaining 2.85V and for signal assertion preferably follow a linear slope of 110Ω. The ML6599 provides a V-I characteristic optimized to minimize the transmission line effects during both signal assertion and negation, using a MOSFET based architecture. The desired V-I characteristic is achieved by trimming one resistor in the control block. It provides negative clamping for signal assertion transients and current sink capability, to handle active negation driver overshoots above 2.85V, which is currently accomplished with external components in SCSI subsystems. It provides a disconnect mode, where the terminator is completely disconnected from the SCSI bus and the output capacitance is typically < 5pF.

FEATURES

- Fully monolithic IC solution providing active termination for 9 lines of the SCSI bus
- Provides on board support for hot-insertability on the SCSI bus
- Low dropout voltage (1V) linear regulator, trimmed for accurate termination current
- Output capacitance typically < 5pF
- Disconnect mode — Logic pin to disconnect terminator from the SCSI bus, <100µA
- Current sinking — can sink current in excess of 10mA per line to handle active negation driver overshoots above 2.85V
- Negative clamping on all lines to handle signal assertion transients
- Regulator can source 200mA and sink 50mA while maintaining regulation
- Current limit & thermal shutdown protection
- Small and low profile package options; 16-pin SOIC (300 mil), 20-pin TSSOP (1 mil height)

BLOCK DIAGRAM



NCLAMP = Negative Clamp

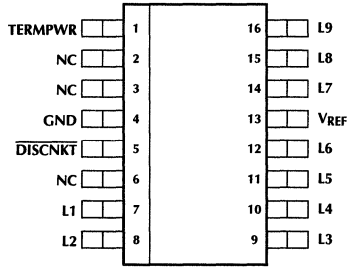
Circuit design patent pending.

GENERAL DESCRIPTION (Continued)

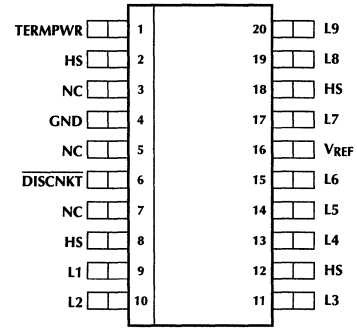
Current limiting and thermal shutdown protection are also provided. The ML6599 provides 9 lines of termination in the industry's smallest package — 20-pin TSSOP. The nine line configuration is optimal for wide SCSI's 18, 27, or 45 line termination needs.

PIN CONFIGURATION

16-Pin SOIC



20-Pin TSSOP



PIN DESCRIPTION

NAME	DESCRIPTION
TERMPWR	Termination Power. Should be connected to the SCSI TERMPWR line. A 10µF tantalum local bypass capacitor is recommended per system, as shown in the application diagram
L1	Signal Termination 1. SCSI Bus line 1
L2	Signal Termination 2. SCSI Bus line 2
L3	Signal Termination 3. SCSI Bus line 3
L4	Signal Termination 4. SCSI Bus line 4
L5	Signal Termination 5. SCSI Bus line 5
L6	Signal Termination 6. SCSI Bus line 6
L7	Signal Termination 7. SCSI Bus line 7
L8	Signal Termination 8. SCSI Bus line 8
L9	Signal Termination 9. SCSI Bus line 9

NAME	DESCRIPTION
V_{REF}	2.85V_{REF} Output. External decoupling with a 10µF tantalum in parallel with a 0.1µF ceramic capacitor is recommended, as shown in the application diagram.
$\overline{\text{DISCNKT}}$	Disconnect Terminator. Logic input to disconnect the terminator from the bus when the SCSI device no longer needs termination due to not being the last device on the bus or otherwise. Active low input.
GND	Ground. Signal Ground (0V)
HS	Heat Sink Ground. Should be connected to GND.

NOTE: The $\overline{\text{DISCNKT}}$ line has a 200kΩ internal pullup resistor connected to the supply. This pin should be left floating for normal operation and should be connected to ground to enable the function

ABSOLUTE MAXIMUM RATINGS

Signal Line Voltage ..... –0.3 to TERMPWR + 0.3V
Regulator Output Current ..... –100 to 300mA
TERMPWR Voltage ..... –0.3 to 7V
Storage Temperature ..... –65°C to 150°C
Soldering Temperature ..... 260°C for 10s
Thermal Impedance (θ_{JA})
SOIC ..... 95°C/W
TSSOP ..... 110°C/W

RECOMMENDED OPERATING CONDITIONS

TERMPWR Voltage ..... 4V to 5.25V
Operating Temperature ..... 0°C to 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for 4V ≤ TERMPWR ≤ 5.25V, and T_A = 0°C to 70°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY					
TERMPWR Supply Current	L1–L9 = open, $\overline{\text{DISCNKT}}$ = open		3.5	5	mA
	L1–L9 = 0.2 V, $\overline{\text{DISCNKT}}$ = open		225		mA
Disconnect Mode Current	$\overline{\text{DISCNKT}}$ = 0 (active)		75	100	µA
INPUT					
Input Low Voltage	$\overline{\text{DISCNKT}}$			1.0	V
Input High Voltage	$\overline{\text{DISCNKT}}$	TERMPWR – 1.0			V
OUTPUT					
Output High Voltage	Measuring each signal line while other eight are high	2.8	2.85	2.9	V
Maximum Output Current (Normal Mode)	V_{OUT} = 0.2V, Measuring each signal line while the other eight are high			24	mA
Hot Insertion Peak Current	TERMPWR = 0V, V_{REF} = 0V Any signal line (L1–L9) at 2.85V		23		µA
Output Clamp Level	I_{OUT} = –30mA (Note 1)	–0.15	0	0.15	V
Current Sink Capability	V_{OUT} = 3.2V (per line)	7	12		mA
Output Capacitance (ML Method)	L1 thru L9, $\overline{\text{DISCNKT}}$ = 0 $2V_{P-P}$ 100kHz square wave applied biased at 1V D.C. (Note 2)			5	pF
Output Capacitance (X3T9.2/855D method)	L1 thru L9, $\overline{\text{DISCNKT}}$ = 0 $0.4V_{P-P}$, 1MHz square wave applied biased at 0.5V D.C. (Note 1)			7	pF
REGULATOR					
Regulator Output Voltage	Sourcing 0-200mA	2.8	2.85	2.9	V
	Sinking 0-50mA (Note 1)	2.8	2.85	2.95	V
Regulator Dropout Voltage	L1–L9 = 0.2V, V_{OUT} = 2.85V		1.0	1.2	V
Regulator Short Circuit Current	Regulator output = 0V		100		mA
	Regulator output = 5V		300		mA
Thermal Shutdown			170		°C

Note 1: Parameter guaranteed by characterization only.
Note 2: Only one pin is checked in the production test environment. Otherwise parameter is guaranteed by characterization and correlation.

FUNCTIONAL DESCRIPTION

The SCSI Terminator helps in decreasing the transmission line effects with precise termination. Termination is conventionally provided at the beginning and end of the SCSI bus, however when additional peripherals are added, the termination needs to be disabled from the current device and enabled on the last device on the bus. Existing termination schemes use a SIP (Single-In-Line package) which is plugged into a socket on the PC board of the SCSI peripheral. To remove the termination, the user needs to pull the resistor SIP out of its socket. With the higher levels of system integration, this is no longer a simple task. With the increasing use of higher data rates and cable lengths in SCSI subsystems, the need for active termination is becoming necessary. Active termination also minimizes power dissipation and can be activated or deactivated under software control, thus eliminating the need for end user intervention. The V-I characteristics of popular SCSI termination schemes are shown in Figure 3. Theoretically the desired V-I characteristics are the Boulay type for signal assertion (high to low) and the Ideal type for signal negation. The ML6599 with its MOSFET based nonlinear termination element attempts to provide the most optimum V-I characteristics — optimized for both signal assertion and negation.

The ML6599 provides active termination for nine signal lines, thus accommodating basic SCSI which requires 18 lines to be terminated and wide SCSI which requires 27, 36 or 45 lines to be terminated. The ML6599 integrates an accurate voltage reference (1V dropout voltage) and nine MOSFET based termination lines. A single internal resistor is trimmed to tune the V-I characteristic of the MOSFETs as shown in figure 1. The voltage reference circuit produces a precise 2.85V level and is capable of sourcing at least 24mA into each of the nine terminating lines when low (active). When the signal line is negated (driver turns off), the terminator pulls the signal line to 2.85V (quiescent state). The regulator will source about 200mA and sink 50mA while maintaining regulation of 2.85V typically.

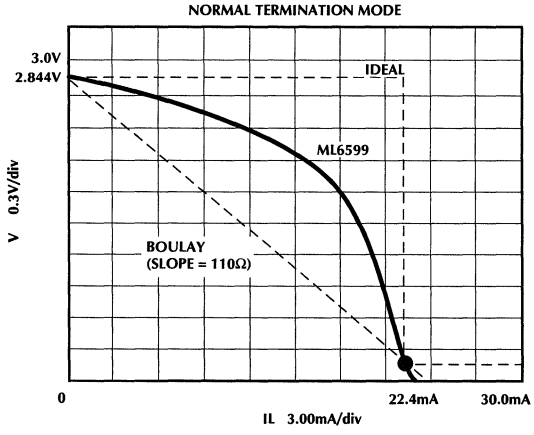


Figure 1. Trimmed V-I Characteristic of the ML6599

The ML6599 SCSI Terminator provides an active low control signal, $\overline{\text{DISCNKT}}$ which has an internal 200KΩ pull-up resistor. The $\overline{\text{DISCNKT}}$ input when asserted low, isolates the ML6599 from the signal lines and effectively removes the terminator from the SCSI Bus with a disconnect mode current of less than 100µA. In addition the ML6599 provides for negative clamping of signal transients and also supports current sink capability in excess of 10mA per signal line, to handle active negation driver overshoot above 2.85V a common occurrence with SCSI transceivers. These functions need to be handled with external components in SCSI subsystems today. Thus the ML6599 helps in eliminating a number of external components.

Disconnect mode capacitance is a very critical parameter in SCSI systems. The ML6599 provides the lowest capacitance contribution of max 5pF and this is guaranteed by production test.

HOT INSERTABILITY

"Hot" insertion of a SCSI device refers to the act of plugging a SCSI device which is initially unpowered into a powered SCSI bus. The SCSI device subsequently draws power from the TERMPWR line during its startup routine and thereafter. "Hot" removal refers to the act of removing a powered SCSI device from a powered SCSI bus. A device which performs both tasks with no physical damage to itself or other devices on the bus, nor which alters the existing state of the bus by drawing excessive currents, is termed "Hot-swappable."

The ML6599 Hot-Insertable SCSI terminator typically draws 23µA from any given output line (L1-L9) during a hot insertion/removal procedure, thereby protecting itself and preserving the state of the bus. The ML6599 design is a slight modification of the ML6509 Low-capacitance SCSI Terminator design. The low current is achieved by effectively shorting the gate to drain of the output PMOS device until the 2.85V reference (V_{REF}) has powered up. A second PMOS in series with a Schottky diode is used as the shorting bypass device. After V_{REF} reaches sufficient level, the bypass device is turned off and the part operates the same as the ML6509. The low-power mode option is not offered on the ML6599.

As outlined in Annex G of the ANSI SCSI-3 Parallel Interface Specification (X3T9.2/855D), "The SCSI bus termination shall be external to the device being inserted or removed." In other words, any terminator connected to a device being hot inserted/removed should be inactive (accomplished by grounding the $\overline{\text{DISCNKT}}$ pin in the case of the ML6599). If the terminator being inserted/removed were in the active state, then at some point in time, the bus would be terminated by either 1 or 3 terminators. In either case, data integrity on the bus is compromised.

Figure 2 gives an application diagram showing a typical SCSI bus configuration. To ensure proper operation, the TERMPWR pin must be connected to the SCSI TERMPOWER line. Each ML6599 requires parallel 0.1µF and 10µF capacitors connected between V_{REF} and GND pins and the TERMPWR line needs a 10µF bypass capacitor per SCSI system.

Thus in an 8-bit wide SCSI bus arrangement ("A" Cable), two ML6599's would be needed at each end of the SCSI cable in order to terminate the 18 active signal lines. Thus 16-bit wide SCSI would use three ML6599's, while 32-bit wide SCSI bus would require five ML6599's.

In a typical SCSI subsystem, the open collector driver in the SCSI transceiver, when asserted, pulls low and when negated, the termination resistance serves as the pull-up. Also shown in Figure 2, is a typical cable response to a pulse. The receiving end of the cable will exhibit a single time delay. When negated, the initial step will reach an intermediate level defined as V_{STEP}. With the higher SCSI data rates, sampling could occur during this step portion. In order to get the most noise margin, the step needs to be as high as possible to prevent false triggering. For this reason the regulator voltage and the resistor defining the MOSFETs characteristic is trimmed to ensure that the I_O is as close as possible to the SCSI max current specification.

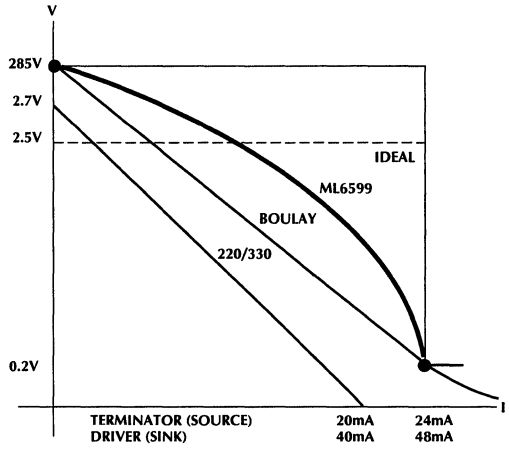


Figure 3. V-1 Characteristics of Various SCSI Termination Schemes

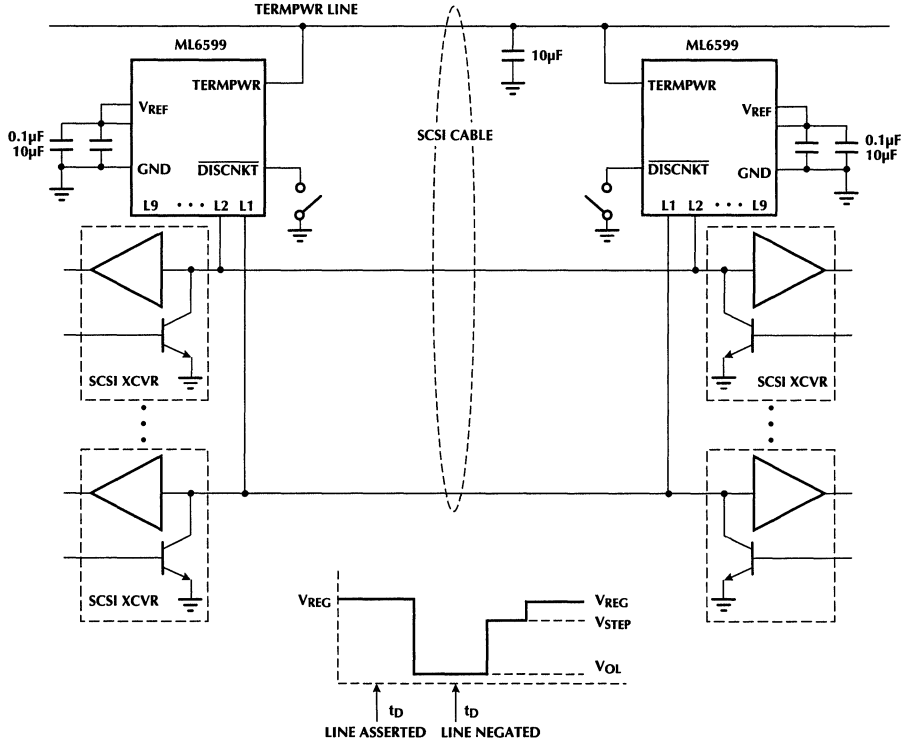


Figure 2. Application Diagram Showing Typical SCSI Bus Configuration with the ML6599

V_{STEP} is defined as follows :

$$V_{STEP} = V_{OL} + (I_O \times Z_O)$$

where

V_{OL} is the Driver output low voltage,

I_O is current from receiving terminator

Z_O is characteristic impedance of cable.

This is a very important characteristic that the terminator helps overcome by increasing the noise margin and boosting the step as high as possible. This capability for the ML6599 implementation is illustrated in the attached simulation graphs which show the terminator performance under different cable impedance situations and a comparison is shown with the standard Boulay terminator, under identical conditions.

APPLICATION INFORMATION

ML6599 EVALUATION BOARD

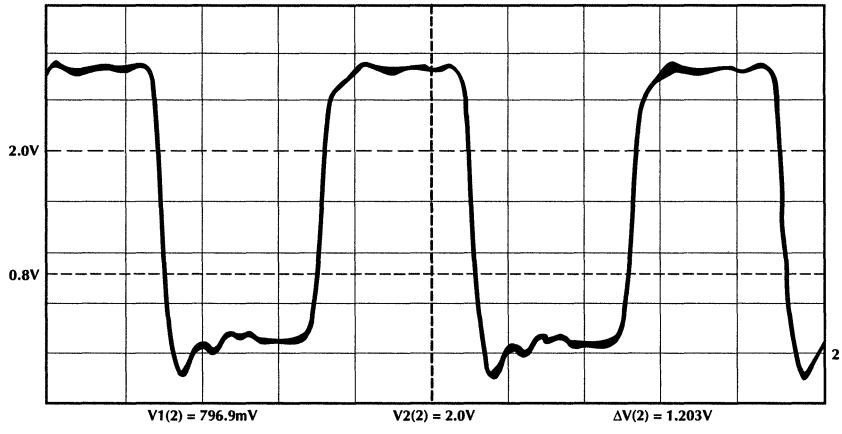
Shown below is the schematic, board component layout, and parts list of the ML6599 SCSI Terminator evaluation board. Actually the ML6509 evaluation board is used for evaluating the ML6599 also. This evaluation board provides termination for 18 lines of SCSI signals and can be connected as the last device on a standard SCSI Bus system. The SCSI Bus signals can then be monitored to see the impact of the ML6599 Active SCSI Terminator in minimizing the transmission line effects. In addition the disconnect mode can be evaluated with respect to power dissipation and output capacitance.

ML6599 EVAL BOARD PARTS LIST

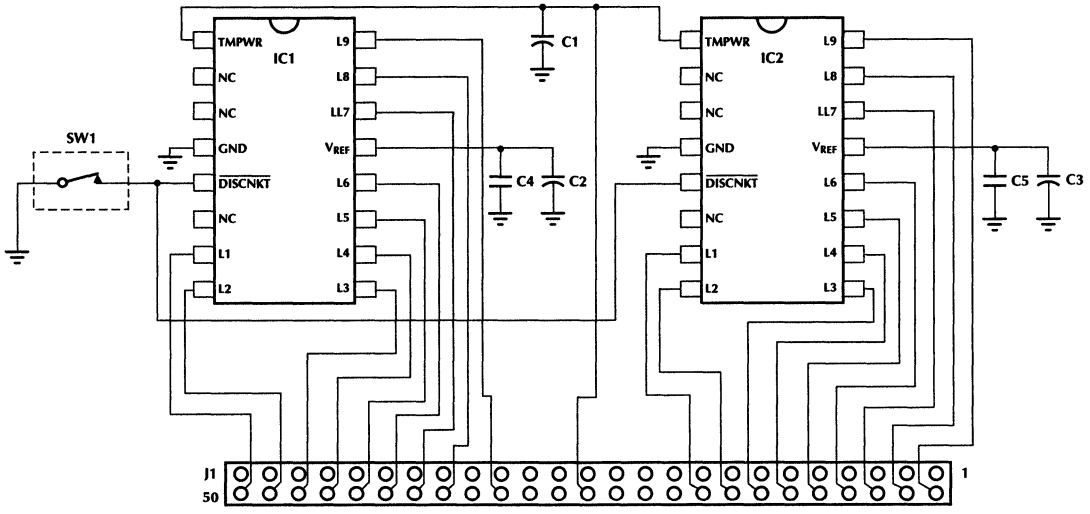
PART#	DESCRIPTION
IC1, IC2	ML6599 Active SCSI Terminator
C1	10µF, 6V Tantalum Chip Capacitor (Philips 49MC106C006K0ASFT)
C2, C3	10µF, 4V Tantalum Chip Capacitor (Philips 49MC106C004K0ASFT)
C4, C5	0.1µF Ceramic Chip Capacitor (Philips C104K1206XFNT)
SW1	Two Position DIP Switch (C&K BD02)
J1	50-pin SCSI Header Connector (AMP 1-103311-0)

TRANSIENT RESPONSE (ACTUAL)

(Approximately 110Ω, 10 feet long, ribbon cable stock)



TYPICAL APPLICATION CIRCUIT



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6599CS	0°C to +70°C	16-pin SOIC (S16W)
ML6599CT	0°C to +70°C	20-pin TSSOP (T20)

Power Management and Control

Section 7

High Frequency PWM Controllers

Resonant and Phase Modulation Controllers

LCD Backlight Lamp Controllers

Electronic Ballast Control

Selection Guide

High Frequency PWM Controllers

Part Number	Reference Accuracy	Max OSC Frequency	Output Driver	Output Current	Soft Start	UV Lockout	Cycle-by-Cycle I_{LIMIT}	Sync Input	Package Type
ML4809	±2%	1 MHz	Push Pull	2A Peak	✓	✓	✓	✓	24-Pin DIP 28-Pin PLCC
ML4810	±2%	1 MHz	Push Pull	2A Peak	✓	✓	✓		16-Pin DIP
ML4811	±2%	1 MHz	Push Pull	2A Peak	✓	✓	✓	✓	20-Pin DIP 20-Pin PLCC
ML4817	±2%	1 MHz	Single Ended	2A Peak	✓	✓	✓		16-Pin DIP 16-Pin SOIC
ML4823	±1%	1 MHz	Single Ended	2A Peak	✓	✓	✓		16-Pin DIP/SOIC 20-Pin PLCC
ML4825	±2%	1 MHz	Push Pull	2A Peak	✓	✓	✓		16-Pin DIP/SOIC 20-Pin PLCC

Power Factor Controllers

Part Number	Reference Accuracy	PFC Topology	Power Factor	Power Range	Output Voltage	Output Current	Soft Start	OV Protection	UV Lockout	Feed Forward	V_{IN} Brownout Protection	Package Type
ML4812	±1%	Peak Current Boost	0.99	>50W	$V_{OUT} > V_{IN}$	1A Peak	✓	✓	✓	✓		16-Pin DIP 20-Pin PLCC
ML4813	±1%	Flyback	0.99	<250W	V_{OUT} Independent of V_{IN}	1A Peak	✓	✓	✓	✓		16-Pin DIP 16-Pin SOIC
ML4821	±2%	Average Current Boost	0.99	>500W	$V_{OUT} > V_{IN}$	1A Peak	✓	✓	✓	✓	✓	18-Pin DIP 20-Pin SOIC

Resonant and Phase Modulation Controllers

Part Number	Reference Accuracy	Max OSC Frequency	Output Driver	Output Current	Soft Start	UV Lockout	Feed Forward	Package Type
ML4815	±2%	2 MHz	Single Ended	2A Peak	✓	✓	✓	16-Pin DIP 20-Pin PLCC
ML4816	±2%	2.5 MHz	Push Pull	1.5A Peak	✓	✓	✓	20-Pin DIP 20-Pin SOIC
ML4818	±1%	500 kHz	Push Pull	1.5A Peak	✓	✓	✓	20-Pin DIP 20-Pin SOIC
ML4828	±1%	1 MHz	Push Pull	500mA Peak	✓	✓	✓	20-Pin DIP 20-Pin SOIC

PFC/PWM Combo Controllers

Part Number	Reference Accuracy	Maximum PFC/PWM Frequency	PFC Topology	PWM Output Driver	PWM Output Current	Soft Start	UV Lockout	Current Limit	Feed Forward	V_{IN} Brownout Protection	Package Type
ML4819	±1%	PFC-500 kHz PWM-500 kHz	Peak Current Boost	Single Ended	1A Peak		✓	✓			20-Pin DIP 20-Pin SOIC
ML4824-1	±1.5%	PFC-500 kHz PWM-500 kHz	Average Current Boost	Single Ended	0.5A Peak	✓	✓	✓	✓	✓	16-Pin DIP 16-Pin SOIC-W
ML4824-2	±1.5%	PFC-250 kHz PWM-500 kHz	Average Current Boost	Single Ended	0.5A Peak	✓	✓	✓	✓	✓	16-Pin DIP 16-Pin SOIC-W
ML4826-1	±1.5%	PFC-500 kHz PWM-500 kHz	Average Current Boost	Push Pull	0.5A Peak	✓	✓	✓	✓	✓	20-Pin DIP 20-Pin SOIC
ML4826-2	±1.5%	PFC-250 kHz PWM-500 kHz	Average Current Boost	Push Pull	0.5A Peak	✓	✓	✓	✓	✓	20-Pin DIP 20-Pin SOIC

Step-Up:

Part Number	Maximum Output Current (mA)	Conversion Efficiency (%)	Quiescent Current (µA)	Input Voltage Range (V)	Output Voltage (V)	Total Regulation (%)	Package Type	Architecture	Features
ML4761	500	90	70	1 to V_{OUT} –0.2	2.5 to 6	3	8-Pin SOIC	PFM	Adjustable Output
ML4851	250	90	80	1 to V_{OUT} –0.2	5, 3.3	3	8-Pin SOIC	PFM	Low Battery Detect
ML4861	500	90	70	1 to V_{OUT} –0.2	6, 5, 3.3	3	8-Pin SOIC	PFM	Low Battery Detect
ML4865	300	90	50	1.8 to V_{OUT} –0.2	12, 15	3	8-Pin SOIC	PFM	Shutdown to Ground, Low Battery Detect
ML4868	500	90	70	1 to V_{OUT} –0.2	5, 3.3	3	8-Pin SOIC	PFM	Low Battery Detect
ML4871	750	90	30	1.8 to V_{OUT} –0.2	5, 3.3	3	8-Pin SOIC	PFM	Low Battery Detect
ML4872	750	90	30	1.8 to V_{OUT} –0.2	5, 3.3	3	8-Pin SOIC	PFM	Shutdown
ML4875	300	90	80	1 to V_{OUT} –0.2	5, 3.3, 3	3	8-Pin SOIC	PFM	Shutdown to Ground, Low Battery Detect
ML4890	100	85	180	1 to 6.5	5, 3.3, 3	3	8-Pin SOIC	PFM/LDO	<5mV Output Ripple, Shutdown to Ground
ML4961	500	90	70	1 to V_{OUT} –0.2	2.5 to 6	3	8-Pin SOIC	PFM	Adjustable Output, Low Battery Detect

Step-Down:

ML4866	1A	90	350	3.5 to 6.5	3.3	3	8-Pin SOIC	PWM	Burst Mode

Flyback (Step-Up/Down):

ML4863	Controller	85	125	3.15 to 15	5 or Multiple	3	8-Pin SOIC	PFM	Shutdown to Ground, Multiple Outputs via Transformer
ML4890	100	85	180	1 to 6.5	5, 3.3, 3	3	8-Pin SOIC	PFM/LDO	<5mV Output Ripple, Shutdown to Ground

Multiple Output Switching Regulator Controllers

Part Number	Output Voltage A	Output Voltage B	Output Voltage C	Quiescent Current Full Load	Quiescent Current No Load	Architecture A	Architecture B	Architecture C	Shut-down	Package	Input Voltage (V)	Power Management FET Drivers	Conversion Efficiency (%)
ML4862	2.5V to $V_{IN}-1$	2.5V to $V_{IN}-1$	12V	10mA	130µA*	PWM	PWM	Linear	Yes	32-Pin SOIC	5.5 to 24	4	93
ML4863	5.0V	Fixed by turns ratio	Fixed by turns ratio	3mA	100µA	Flyback PFM	Flyback PFM	Flyback PFM	Yes	8-Pin SOIC	3.15 to 15	0	85
ML4873	2.5V to $V_{IN}-1$	2.5V to $V_{IN}-1$	12V	10mA	130µA*	PWM	PWM	Linear	Yes	28-Pin SOIC	5.5 to 30	1	93
ML4880	3.0 to 3.5V	4.0 to 5.0V	2.5V to 18V	30mA	300µA*	PFM	PFM	PFM	Yes	24-Pin SOIC	5.5 to 18	0	90

*All outputs shut down.

LCD Backlight Lamp Controllers

Part Number	Function	Key Features	Package Options
ML4864	LCD Backlight Lamp Driver with Contrast	Dimming, 95% efficiency, Positive or Negative Contrast	SSOP-20
ML4874	LCD Backlight Lamp Driver	Differential Drive, Dimming, 95% efficiency	SOIC-16 SSOP-20
ML4876	LCD Backlight Lamp Driver with Contrast	Differential Drive, Dimming, 95% efficiency Positive or Negative Contrast	SSOP-20

Micro Linear

ML1825

High Frequency Power Supply Controller

GENERAL DESCRIPTION

The ML1825 High Frequency PWM Controller is an IC controller optimized for use in Switch Mode Power Supply designs running at frequencies to 1MHz. Propagation delays are minimal through the comparators and logic for reliable high frequency operation while slew rate and bandwidth are maximized on the error amplifier. This controller is designed to work in either voltage or current mode and provides for input voltage feed forward.

A 1V threshold current limit comparator provides cycle-by-cycle current limit while exceeding a 1.4V threshold initiates a soft-start cycle. The soft start pin doubles as a maximum duty cycle clamp. All logic is fully latched to provide jitter-free operation and prohibit multiple pulsing. An under-voltage lockout circuit with 800mV of hysteresis assures low startup current and drives the outputs low.

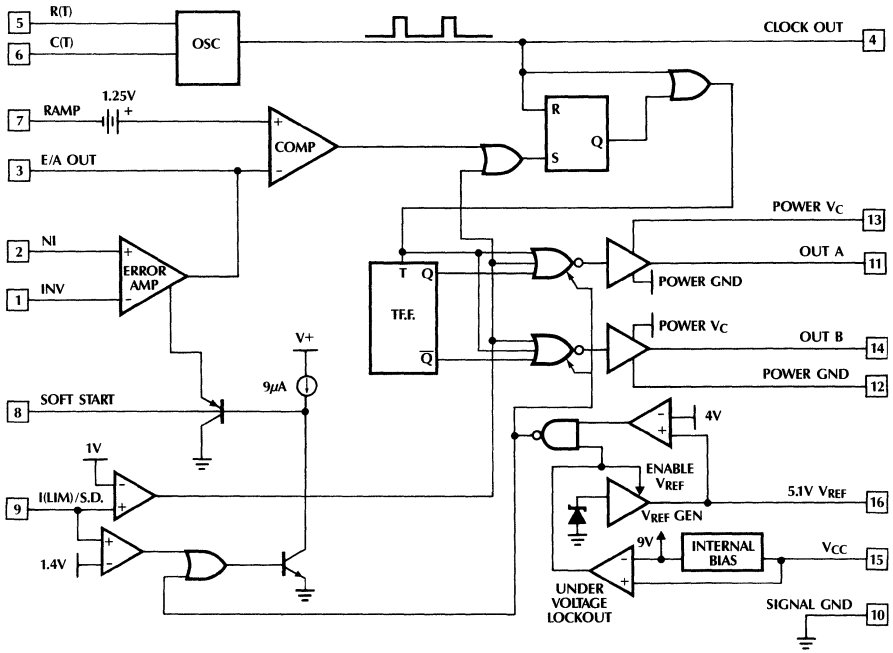
The ML1825 is fabricated on a 40V bipolar process from the FB3480 Power Supply Controller Array. Customized versions of this controller are therefore easily implemented. Please refer to the FB3480 datasheet for more information.

This controller is a pin for pin replacement for the UC1825 controller.

FEATURES

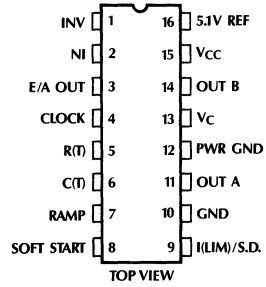
- Practical Operation at Switching Frequencies to 1.0MHz
- High Current (2A peak) Dual Totem Pole Outputs
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start and Max. Duty Cycle Control
- Under Voltage Lockout with Hysteresis
- 5.1V, ±1% Trimmed Bandgap Reference
- Pin Compatible Replacement for UC1825

BLOCK DIAGRAM



PIN CONNECTION

ML1825
16-Pin DIP



PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	INV	Inverting input to error amp.
2	NI	Non-inverting input to error amp.
3	E/A OUT	Output of error amplifier and input to main comparator.
4	CLOCK	Oscillator output.
5	R(T)	Timing Resistor for Oscillator — sets charging current for oscillator timing capacitor (pin 6).
6	C(T)	Timing Capacitor for Oscillator.
7	RAMP	Non-Inverting input to main comparator. Connected to C(T) for Voltage Mode operation or to current sense resistor for current mode.
8	SOFT START	Normally connected to Soft Start Capacitor.
9	I(LIM)/S.D.	Current limit sense pin. Normally connected to current sense resistor.
10	GND	Analog Signal Ground.
11	OUT A	High Current Totem pole output. This output is the first one energized after Power On Reset.
12	PWR GND	Return for the High Current Totem pole outputs.
13	V_C	Positive Supply for the High Current Totem pole outputs.
14	OUT B	High Current Totem pole output.
15	V_{CC}	Positive Supply for the IC.
16	5.1V REF	Buffered output for the 5.1V voltage reference.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13) 30V
Output Current, Source or Sink (Pins 11, 14)
DC 0.5A
Pulse (0.5μs) 2.0A
Analog Inputs
(Pins 1, 2, 7) ..... –0.3V to 7V
(Pins 9, 8) ..... –0.3V to 6V
Clock Output Current (Pin 4) ..... –5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... –5mA
Junction Temperature
ML4825M ..... 150°C
ML4825I, ML4825C ..... 125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Ceramic DIP ..... 65°C/W

OPERATING CONDITIONS

Temperature Range
ML1825M ..... –55°C to +125°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial Accuracy	T_J = 25°C, (note 1)	360	400	440	KHz
Voltage Stability	10V < V_{CC} < 30V, (note 1)		0.2	2	%
Temperature Stability	(note 1)		5		%
Total Variation	line, temp, (note 1)	340		460	KHz
Clock Out High		3.9	4.5		V
Clock Out Low			2.3	2.9	V
Ramp Peak	(note 1)	2.6	2.8	3.0	V
Ramp Valley	(note 1)	0.7	1.0	1.25	V
Ramp Valley to Peak	(note 1)	1.6	1.8	2.0	V
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1mA	5.05	5.10	5.15	V
Line Regulation	10V < V_{CC} < 30V		2	20	mV
Load Regulation	1mA < I_O < 10mA		5	20	mV
Temperature Stability	–55°C < T_J < 150°C, (note 1)		.2	.4	%
Total Variation	line, load, temp (note 1)	5.0		5.20	V
Output Noise Voltage	10Hz to 10KHz		50		μV
Long Term Stability	T_J = 125°C, 1000 hrs, (note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	–15	–50	–100	mA
Error Amplifier Section					
Input Offset Voltage				10	mV
Input Bias Current			.6	3	μA
Input Offset Current			.1	1	μA
Open Loop Gain	1 < V_O < 4V	60	95		dB

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section (Continued)					
CMRR	$1.5 < V_{CM} < 5.5V$	75	95		dB
PSRR	$10 < V_{CC} < 30V$	85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth	(note 1)	3	5.5		MHz
Slew Rate	(note 1)	6	12		V/μs
PWM Comparator Section					
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5	μA
Duty Cycle Range		0		80	%
Pin 3 Zero DC Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		V
Delay to Output	(note 1)		50	80	ns
Soft-Start Section					
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	μA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			mA
Current Limit/Shutdown Section					
Pin 9 Bias Current	$0V < V_{PIN\ 9} < 4V$			+15	μA
Current Limit Threshold		.9	1	1.1	V
Shutdown Threshold		1.25	1.4	1.55	V
Delay to Output	(note 1)		50	80	ns
Output Section					
Output Low Level	I_{OUT} = 20mA		.25	.4	V
	I_{OUT} = 200mA		1.2	2.2	V
Output High Level	I_{OUT} = -20mA	13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		V
Collector Leakage	V_C = 30V		100	500	μA
Rise/Fall Time	C_L = 1000pF, (note 1)		30	60	ns
Under-Voltage Lockout Section					
Start Threshold		8.8	9.2	9.6	V
UVLO Hysteresis		.4	.8	1.2	V
Supply Current					
Start Up Current	V_{CC} = 8V		1.1	2.5	mA
I_{CC}	$V_{PIN\ 1,\ 7,\ 9}$ = 0V, $V_{PIN\ 2}$ = 1V,		22	33	mA

Note 1: This parameter not 100% tested in production but guaranteed by design.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML1825 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $3/R_{SET}$. When the capacitor voltage reaches the upper threshold (Ramp Peak), the comparator changes state and the capacitor discharges to the lower threshold (Ramp Valley) through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where: $T_{RAMP} = C$ (Ramp Valley to Peak)$/I_{SET}$

and: $T_{DEADTIME} = C$ (Ramp Valley to Peak)$/I_{Q1}$

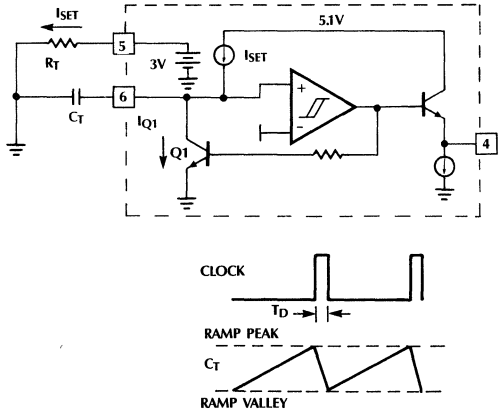


Figure 1. Oscillator Block Diagram

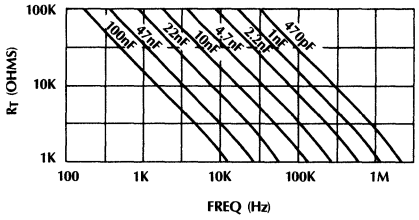


Figure 2. Oscillator Timing Resistance vs Frequency

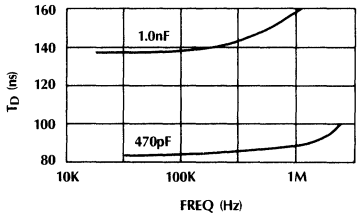


Figure 3. Oscillator Deadtime vs Frequency

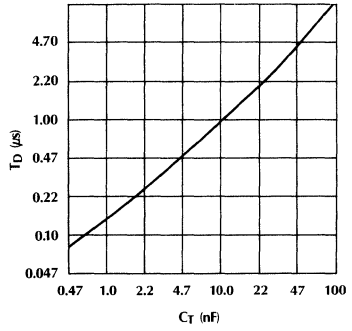


Figure 4. Oscillator Deadtime vs C(T) (3KΩ ≤ R(T) ≤ 100KΩ)

ERROR AMPLIFIER

The ML1825 error amplifier is a 5.5MHz bandwidth 12V/µs slew rate op-amp with provision for limiting the positive output voltage swing (Output Inhibit line) for ease in implementing the soft start function.

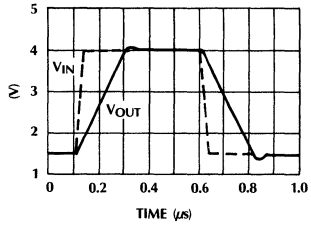


Figure 5. Unity Gain Slew Rate

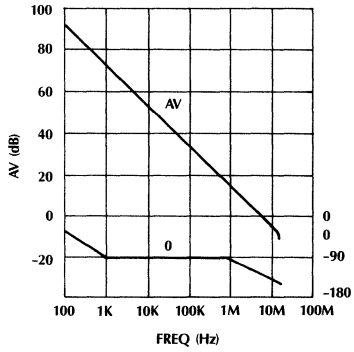


Figure 6. Open Loop Frequency Response

OUTPUT DRIVER STAGE

The ML1825 Output Driver is a 2A peak output high speed totem pole circuit designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors.

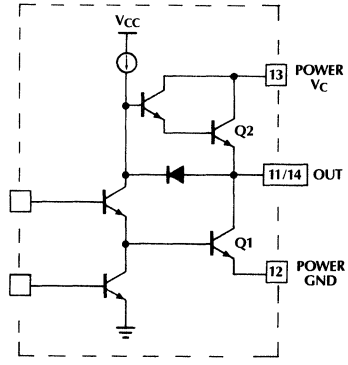


Figure 7. Simplified Schematic

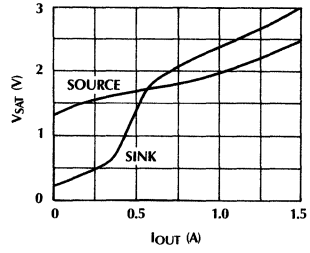


Figure 8. Saturation Curves

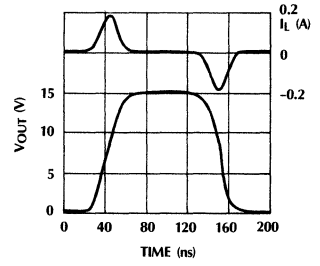


Figure 9. Rise/Fall Time (C_L = 1000pF)

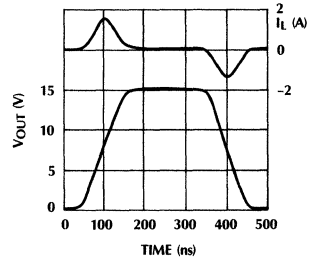


Figure 10. Rise/Fall Time (C_L = 10,000pF)

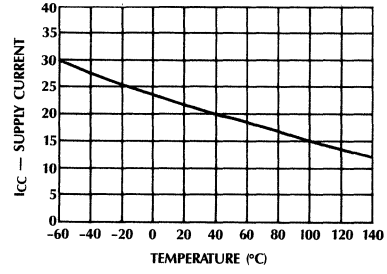


Figure 11. Supply Current vs Temperature

SOFT START AND CURRENT LIMIT

The ML1825 employs two current limits. When the voltage at pin 9 exceeds 1V, the outputs are immediately shut off and the cycle is terminated for the remainder of the oscillator period by resetting the RS flip flop.

If the output current is rising quickly such that the voltage on pin 9 reaches 1.4V before the outputs have turned off, a soft start cycle is initiated and the soft start capacitor (pin 8) is discharged. The duty cycle on start up is limited by limiting the output voltage of the error amplifier voltage to the voltage at pin 8.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML1825MJ	-55°C to +125°C	Hermetic DIP (J16)

ML4761

Adjustable Output Low Voltage Boost Regulator

GENERAL DESCRIPTION

The ML4761 is a boost regulator designed for DC to DC conversion in 1 to 3 cell battery powered systems. The combination of BiCMOS process technology, internal synchronous rectification, variable frequency operation, and low supply current make the ML4761 ideal for 1 cell applications. The ML4761 is capable of start-up with input voltages as low as 1V, and the output voltage can be set anywhere between 2.5V and 6V by an external resistor divider connected to the SENSE pin.

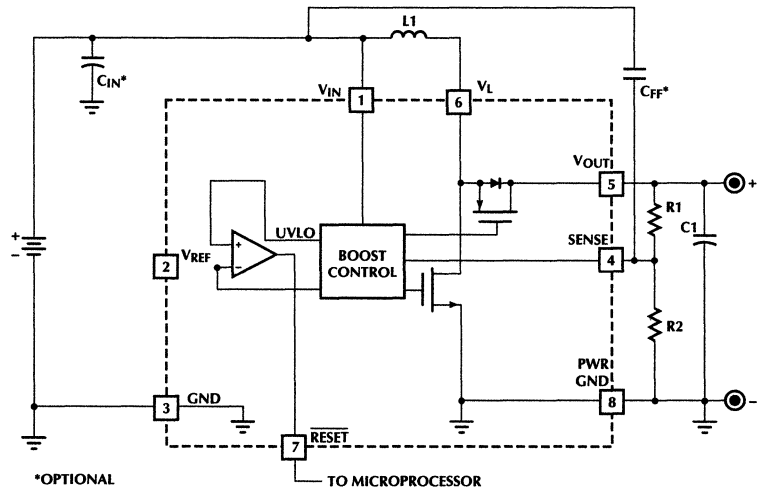
An integrated synchronous rectifier eliminates the need for an external Schottky diode and provides a lower forward voltage drop, resulting in higher conversion efficiency. In addition, low quiescent battery current and variable frequency operation result in high efficiency even at light loads. The ML4761 requires a minimum number of external components to build a very small adjustable regulator circuit capable of achieving conversion efficiencies in excess of 90%.

The circuit also contains a $\overline{\text{RESET}}$ output which goes low when the IC can no longer function due to low input voltage (UVLO).

FEATURES

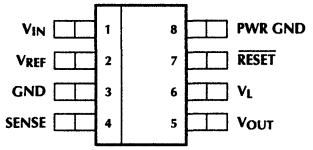
- Guaranteed full load start-up and operation at 1V input
- Pulse Frequency Modulation and Internal Synchronous Rectification for high efficiency
- Minimum external components
- Low ON resistance internal switching FETs
- Micropower operation
- Adjustable output voltage (2.5V to 6V)

BLOCK DIAGRAM



PIN CONNECTION

ML4761
8-Pin SOIC (S08)



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	V_{IN}	Battery input voltage
2	V_{REF}	200mV reference output
3	GND	Analog signal ground
4	SENSE	Programming pin for setting the output voltage
5	V_{OUT}	Boost regulator output
6	V_L	Boost inductor connection
7	$\overline{RESET}$	Output goes low when regulation cannot be achieved
8	PWR GND	Return for the NMOS output transistor.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Voltage on any pin 7V
Peak Switch Current, $I_{(PEAK)}$ 2A
Average Switch Current, $I_{(AVG)}$ 500mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA}) ..... 110°C/W

OPERATING CONDITIONS

Temperature Range
ML4761CS ..... 0°C to +70°C
ML4761ES ..... –20°C to +70°C
ML4761IS ..... –40°C to +85°C
V_{IN} Operating Range
ML4761CS ..... 1.0V to V_{OUT} –0.2V
ML4761ES, ML4761IS ..... 1.1V to V_{OUT} –0.2V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = Operating Voltage Range, T_A = Operating Temperature Range

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Supply					
V_{IN} Current	$V_{IN} = V_{OUT} - 0.2V$		45	55	µA
V_{OUT} Quiescent Current			3	5	µA
V_L Quiescent Current				1	µA
Reference					
Output Voltage (V_{REF})	$0 < I_{PIN2} < -5µA$	194	200	206	mV
PFM Regulator					
Pulse Width (T_{ON})		9	10	11	µs
SENSE Comparator Threshold Voltage (V_{SENSE})		190	200	210	mV
Load Regulation	See Figure 1 V_{IN} = 1.2V, $I_{OUT} \leq$ 25mA V_{IN} = 2.4V, $I_{OUT} \leq$ 135mA	 4.85 4.85	 5.0 5.0	 5.15 5.15	 V V
Undervoltage Lockout Threshold			0.85	0.95	V
$\overline{\text{RESET}}$ Comparator					
$\overline{\text{RESET}}$ Output High Voltage (V_{OH})	I_{OH} = –100µA	V_{OUT} – 0.2			V
$\overline{\text{RESET}}$ Output Low Voltage (V_{OL})	I_{OL} = 100µA			0.2	V

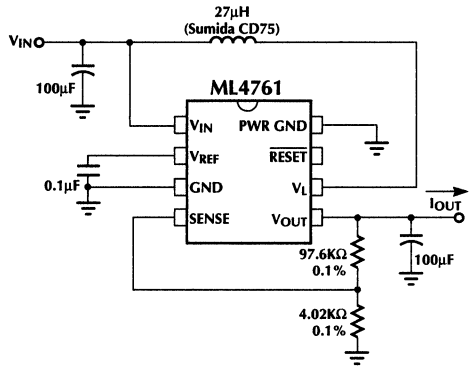


Figure 1. Application Test Circuit.

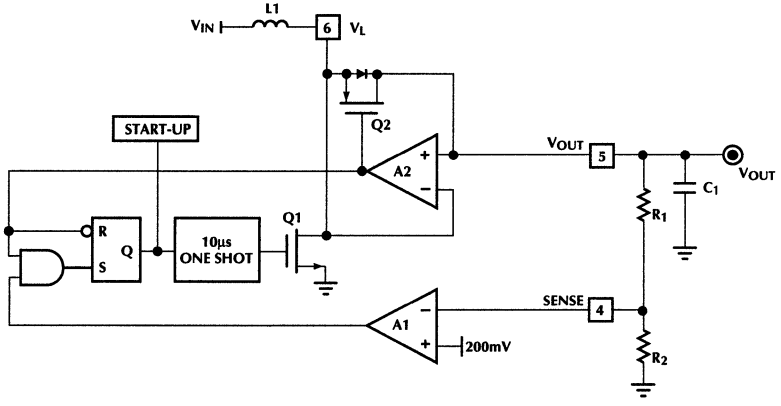


Figure 2. PFM Regulator Block Diagram.

FUNCTIONAL DESCRIPTION

The ML4761 combines Pulse Frequency Modulation (PFM) and synchronous rectification to create a boost converter that is both highly efficient and simple to use. A PFM regulator charges a single inductor for a fixed period of time and then completely discharges before another cycle begins, simplifying the design by eliminating the need for conventional current limiting circuitry. Synchronous rectification is accomplished by replacing an external Schottky diode with an on-chip PMOS device, reducing switching losses and external component count.

REGULATOR OPERATION

A block diagram of the boost converter is shown in Figure 2. The circuit remains idle when V_{OUT} is at or above the desired output voltage, drawing 45µA from V_{IN}, and 8µA from V_{OUT} through the feedback resistors R1 and R2. When V_{OUT} drops below the desired output level, the output of amplifier A1 goes high, signaling the regulator to deliver charge to the output. Since the output of amplifier A2 is normally high, the flip-flop captures the A1 set signal and creates a pulse at the gate of the NMOS transistor Q1. The NMOS transistor will charge the inductor L1 for 10µs, resulting in a peak current given by:

$$I_{L(PEAK)} = \frac{T_{ON} \times V_{IN}}{L1} \approx \frac{10\mu s \times V_{IN}}{L1} \qquad (1)$$

For reliable operation, L1 should be chosen so that $I_{L(PEAK)}$ does not exceed 2A.

When the one-shot times out, the NMOS FET releases the V_L pin, allowing the inductor to fly-back and momentarily charge the output through the body diode of PMOS transistor Q2. But, as the voltage across the PMOS transistor changes polarity, its gate will be driven low by the current sense amplifier A2, causing Q2 to short out its body diode. The inductor then discharges into the load through Q2. The output of A2 also serves to reset the flip-flop and one-shot in preparation for the next charging cycle. A2 releases the gate of Q2 when its current falls to zero. If V_{OUT} is still low, the flip-flop will immediately initiate another pulse. The output capacitor (C1) filters the inductor current, limiting output voltage ripple. Inductor current and one-shot waveforms are shown in Figure 3.

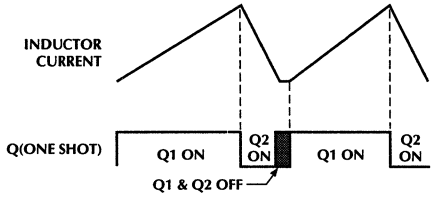


Figure 3. PFM Inductor Current Waveforms and Timing.

$\overline{\text{RESET}}$ COMPARATOR

An additional comparator is provided to detect low V_{IN}. The inverting input of the comparator is internally connected to V_{REF}, while the non-inverting input is connected to the undervoltage lockout circuit. The output of the comparator is the $\overline{\text{RESET}}$ pin, which swings from V_{OUT} to GND when an undervoltage condition is detected.

DESIGN CONSIDERATIONS

INDUCTOR

Selecting the proper inductor for a specific application usually involves a trade-off between efficiency and maximum output current. Choosing too high a value will keep the regulator from delivering the required output current under worst case conditions. Choosing too low a value causes efficiency to suffer. It is necessary to know the maximum required output current and the input voltage range to select the proper inductor value. The maximum inductor value can be estimated using the following formula:

$$L_{MAX} = \frac{V_{IN(MIN)}^{2} \times T_{ON(MIN)} \times \eta}{2 \times V_{OUT} \times I_{OUT(MAX)}} \qquad (2)$$

where η is the efficiency, typically between 0.8 and 0.9. Note that this is the value of inductance that just barely delivers the required output current under worst case conditions. A lower value may be required to cover inductor tolerance, the effect of lower peak inductor currents caused by resistive losses, and minimum dead time between pulses.

Another method of determining the appropriate inductor value is to make an estimate based on the typical performance curves given in Figures 4 and 5. Figure 4 shows maximum output current as a function of input voltage for several inductor values. These are typical performance curves and leave no margin for inductance and ON-time variations. To accommodate worst case conditions, it is necessary to derate these curves by at least 10% in addition to inductor tolerance. Interpolation between the different curves will give a reasonable starting point for an inductor value.

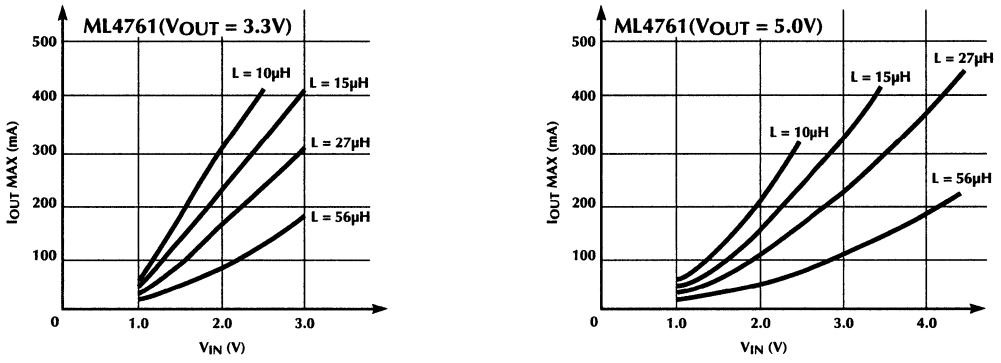


Figure 4. Output Current vs. Input Voltage.

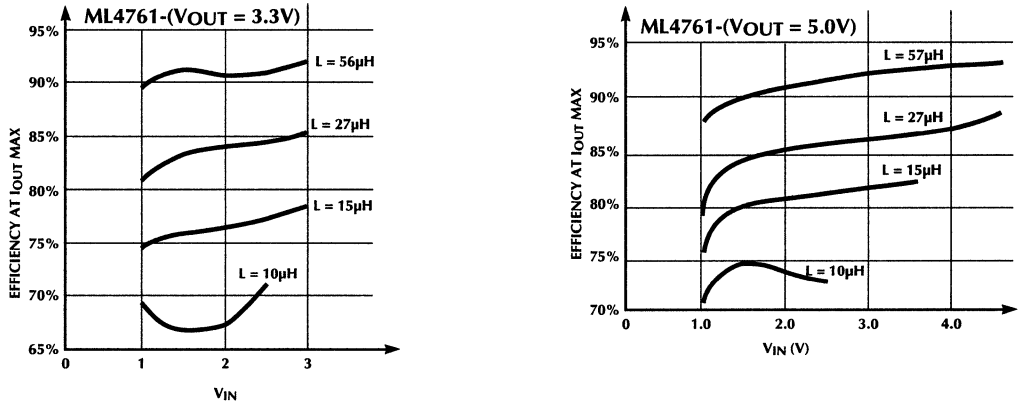


Figure 5. Typical Efficiency as a Function of V_{IN}.

Figure 5 shows efficiency under the conditions used to create Figure 4. It can be seen that efficiency is mostly independent of input voltage and is closely related to inductor value. This illustrates the need to keep the inductor value as high as possible to attain peak system efficiency. As the inductor value goes down to 10µH, the efficiency drops to between 70% and 75%. With 56µH, the efficiency exceeds 90% and there is little room for improvement. At values greater than 100µH, the operation of the synchronous rectifier becomes unreliable because the inductor current is so small that it is difficult for the control circuitry to detect.

After the appropriate inductor value is chosen, it is necessary to find the minimum inductor current rating required. Peak inductor current is determined from the following formula:

$$I_{L(PEAK)} = \frac{T_{ON(MAX)} \times V_{IN(MAX)}}{L_{MIN}} \qquad (3)$$

When comparing various inductors, it is important to keep in mind that suppliers use different criteria to determine their ratings. Many use a conservative current level, where inductance has dropped to 90% of its normal level. In any case, it is a good idea to try inductors of various current ratings with the ML4761 to determine which inductor is the best choice. Check efficiency and maximum output current, and if a current probe is available, look at the inductor current to see if it looks like the waveform shown in Figure 3. For additional information, see Application Note 29.

Suitable inductors can be purchased from the following suppliers:

Coilcraft	(708) 639-6400
Coiltronics	(407) 241-7876
Dale	(605) 665-9301
Sumida	(708) 956-0666

OUTPUT CAPACITOR

The choice of output capacitor is also important, as it controls the output ripple and optimizes the efficiency of the circuit. Output ripple is influenced by three capacitor parameters: capacitance, ESR, and ESL. The contribution due to capacitance can be determined by looking at the change in capacitor voltage required to store the energy delivered by the inductor in a single charge-discharge cycle, as determined by the following formula:

$$\Delta V_{OUT} = \frac{T_{ON}^2 \times V_{IN}^2}{2 \times L \times C \times (V_{OUT} - V_{IN})} \quad (4)$$

For a 2.4V input, and 5V output, a 27µH inductor, and a 47µF capacitor, the expected output ripple due to capacitor value is 87mV.

Capacitor Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL), also contribute to the output ripple due to the inductor discharge current waveform. Just after the NMOS transistor turns off, the output current ramps quickly to match the peak inductor current. This fast change in current through the output capacitor's ESL causes a high frequency (5ns) spike that can be over 1V in magnitude. After the ESL spike settles, the output voltage still has a ripple component equal to the inductor discharge current times the ESR. This component will have a sawtooth shape and a peak value equal to the peak inductor current times the ESR. ESR also has a negative effect on efficiency by contributing I-squared R losses during the discharge cycle.

An output capacitor with a capacitance of 100µF, an ESR of less than 0.1Ω, and an ESL of less than 5nH is a good general purpose choice. Tantalum capacitors which meet these requirements can be obtained from the following suppliers:

Matsuo	(714) 969-2491
Sprague	(603) 224-1961

If ESL spikes are causing output noise problems, an EMI filter can be added in series with the output.

INPUT CAPACITOR

Unless the input source is a very low impedance battery, it will be necessary to decouple the input with a capacitor with a value of between 47µF and 100µF. This provides the benefits of preventing input ripple from affecting the ML4761 control circuitry, and it also improves efficiency by reducing I-squared R losses during the charge and discharge cycles of the inductor. Again, a low ESR capacitor (such as tantalum) is recommended.

SETTING THE OUTPUT VOLTAGE

The adjustable output can be set to any voltage between 2.5V and 6V by connecting a resistor divider to the SENSE pin as shown in the block diagram. The resistor values R_1 and R_2 can be calculated using the following equation:

$$V_{OUT} = 0.2 \times \frac{(R_1 + R_2)}{R_2} \quad (5)$$

The value of R_2 should be 40kΩ or less to minimize bias current errors. R_1 is then found by rearranging the equation:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{0.2} - 1 \right) \quad (6)$$

It is important to note that the accuracy of these resistors directly affects the accuracy of the output voltage. The SENSE pin threshold variation is ±3%, and the tolerances of R_1 and R_2 will add to this to determine the total output variation.

REFERENCE CAPACITOR

Under some circumstances input ripple cannot be reduced effectively. This occurs primarily in applications where inductor currents are high, causing excess output ripple due to "pulse grouping", where the charge-discharge pulses are not evenly spaced in time. In such cases it may be necessary to decouple the reference pin (V_{REF}) with a small 10nF to 100nF ceramic capacitor. This is particularly true if the ripple voltage at V_{IN} is greater than 100mV.

In some applications, input noise may cause output ripple to become excessive due to "pulse grouping", where the charge-discharge pulses are not evenly spaced in time. In such cases it may be necessary to add a small 20pF to 100pF ceramic feedforward capacitor (C_{FF}) from the V_{IN} pin to the SENSE pin.

LAYOUT

Good PC board layout practices will ensure the proper operation of the ML4761. Important layout considerations include:

- Use adequate ground and power traces or planes
- Keep components as close as possible to the ML4761
- Use short trace lengths from the inductor to the V_L pin and from the output capacitor to the V_{OUT} pin
- Use a single point ground for the ML4761 ground pins, and the input and output capacitors

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4761CS	0°C to +70°C	8-Pin SOIC (S08)
ML4761ES	–20°C to +70°C	8-Pin SOIC (S08)
ML4761IS	–40°C to +85°C	8-Pin SOIC (S08)

High Frequency PWM Controller

GENERAL DESCRIPTION

The ML4809 High Frequency PWM Controller is a full-featured IC controller optimized for use in Switch Mode Power Supply designs running at frequencies to 1MHz. Propagation delays are minimized while slew rate and bandwidth are maximized for reliable high frequency operation. This controller is designed to work in either voltage or current mode and provides for input voltage feed forward.

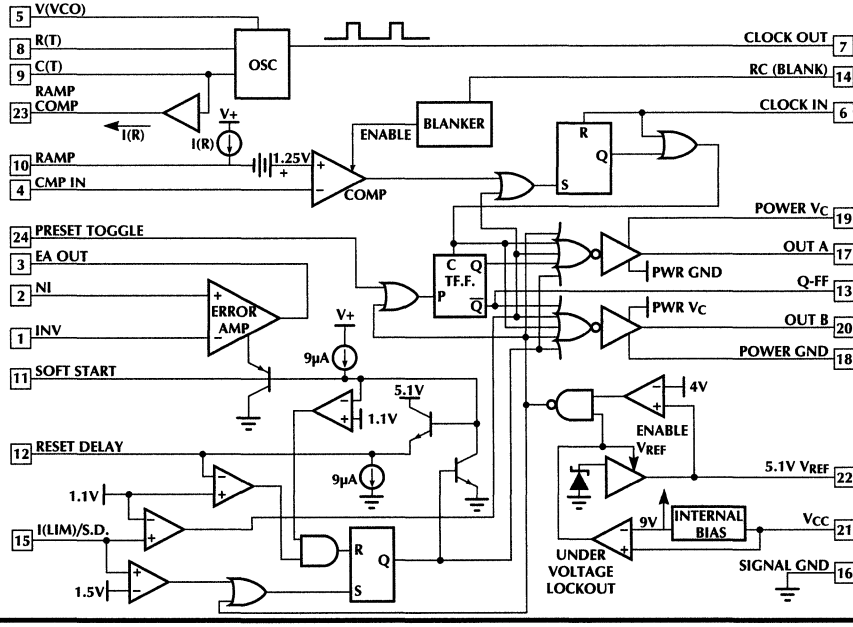
A 1.1V threshold current limit comparator provides cycle-by-cycle current limit while exceeding a 1.5V threshold initiates a soft-start cycle. The soft start pin doubles as a maximum duty cycle clamp. All logic is fully latched to provide jitter-free operation and prohibit multiple pulsing. An under-voltage lockout circuit with 7V of hysteresis assures low startup current and drives the outputs low.

The ML4809 is fabricated on a 40V bipolar process from the FB3480 Power Supply Controller Array. Customized versions of this controller are easily implemented. This controller is similar to the UC1825 controller, however the ML4809 includes many features not found on the 1825. These features are set in *Italics.*

FEATURES

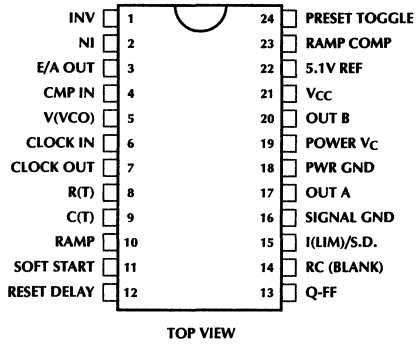
- Practical operation at switching frequencies to 1.0MHz
- High current (2A peak) dual totem pole outputs
- Wide bandwidth error amplifier
- Fully latched logic with double pulse suppression
- Pulse-by-pulse current limiting
- Soft start and max. duty cycle control
- 5.1V ±2% trimmed bandgap reference
- *Under voltage lockout: 16V start with 7V hysteresis*
- *Programmable ramp compensation circuit*
- *VCO input for synchronization or frequency control*
- *External clock input for synchronization*
- *Toggle preset for synchronization*
- *Comparator blanker for better noise immunity/stability*
- *Separate error amplifier output pin for loop filtering versatility*
- *Fast shut down path from current limit to outputs*
- *Outputs preset to known condition after under voltage lockout*
- *Soft start latch ensures full soft start cycle*
- *Programmable soft start delay*

BLOCK DIAGRAM



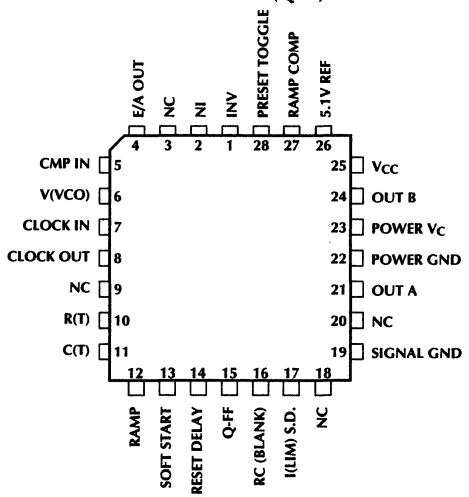
PIN CONFIGURATION

ML4809
24-Pin DIP (P24N)



TOP VIEW

ML4809
28-Pin PCC (Q28)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	INV	Inverting input to error amp.
2	NI	Non-inverting input to error amp.
3	E/A OUT	Output of error amplifier.
4	CMP IN	Main comparator input.
5	V(VCO)	A control voltage input which sets the VCO frequency. May be tied to 5.1V REF (22) for fixed frequency operation.
6	CLOCK IN	A "1" level blanks the outputs and prepares the chip for the next cycle by toggling the T flip flop.
7	CLOCK OUT	Oscillator output. This is an emitter follower output.
8	R(T)	Timing resistor for oscillator — sets charging current for oscillator timing capacitor (pin 9).
9	C(T)	Timing capacitor for oscillator.
10	RAMP	Non-inverting input to main comparator. Connected to C(T) for voltage mode operation or to current sense resistor for current mode.
11	SOFT START	Normally connected to soft start capacitor.
12	RESET DELAY	Connect to capacitor for time delay before new soft-start cycle begins after 1.4V current limit is reached.
13	Q-FF	An emitter follower output which is high for B active.
14	RC (BLANK)	Connect resistor and capacitor to ground for blanker function.
15	I(LIM)/S.D.	Current limit sense pin. Normally connected to sense resistor.
16	GND	Analog signal ground.
17	OUT A	High current totem pole output. This output is the first one energized after power on reset.
18	PWR GND	Return for the high current totem pole outputs.
19	POWER V_C	Positive supply for the high current totem pole outputs.
20	OUT B	High current totem pole output.
21	V_{CC}	Positive supply for the IC.
22	5.1V REF	Buffered output for the 5.1V voltage reference.
23	RAMP COMP	Connect resistor to GND for ramp compensation.
24	PRESET TOGGLE	Presets the toggle flip-flop. Tie to GND to disable.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 21, 19) 36V
Output Current, Source or Sink (Pins 17, 20)
  DC 0.5A
  Pulse (0.5µs) 2.0A
Input Voltage
  (Pins 1, 2, 4, 5, 10) ..... –0.3V to 7V
  (Pins 8, 9, 11, 12, 15, 24) ..... –0.3V to 6V
Logic Output Current (Pins 7, 13) ..... –5mA
Blanker Charge Current (Pin 14) ..... –5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 11) 20mA
Oscillator Charging Current (Pin 8) ..... –5mA
Junction Temperature
  ML4809M ..... 150°C
  ML4809I, ML4809C ..... 125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
  Plastic DIP ..... 50°C/W
  Ceramic DIP ..... 55°C/W
  Plastic Chip Carrier (PCC) ..... 55°C/W

OPERATING CONDITIONS

Temperature Range
  ML4809C ..... 0°C to +70°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 6.2KΩ, C_T = 1000pF, V(VCO) = V_{REF}, R_L (Pins 7, 13) = 5KΩ, T_A = Operating Temperature Range, V_{CC} = 15V. (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial Accuracy	T_J = 25°C, (note 1)	380	430	470	KHz
Voltage Stability	10V < V_{CC} < 30V, (note 1)		0.2	4	%
Temperature Stability	(note 1)		5		%
Total Variation	line, temp, (note 1)	370	430	490	KHz
Clock Out High		3.9	4.5		V
Clock Out Low			2.3	2.9	V
Ramp Peak	(note 1)	2.6	2.8	3.0	V
Ramp Valley	(note 1)	0.7	1.0	1.25	V
Ramp Valley to Peak	(note 1)	1.6	1.8	2.0	V
V(VCO) Control Range		1		5.5	V
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1mA	5.00	5.10	5.20	V
Line Regulation	10V < V_{CC} < 30V		2	20	mV
Load Regulation	1mA < I_O < 10mA		5	20	mV
Temperature Stability	–55°C < T_J < 150°C, (note 1)		0.2	0.4	%
Total Variation	line, load, temp, (note 1)	4.95		5.25	V
Output Noise Voltage	10Hz to 10KHz		50		µV
Long Term Stability	T_J = 125°C, 1000 hrs, (note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V, T_A ≥ 0°C	–15	–50	–100	mA
	T_A < 0°C	–15	–50	–120	mA
Under-Voltage Lockout Section					
Start Threshold		15	16	17	V
UVLO Hysteresis		6.0	7	8.0	V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section					
Input Offset Voltage	T_A = 25°C			±15	mV
				±20	mV
Input Bias Current			0.6	3	µA
Input Offset Current			0.1	1	µA
Open Loop Gain	1 < V_O < 4V	60	96		dB
CMRR	1.5 < V_{CM} < 5.5V, T_A ≥ 0°C	75	95		dB
	1.5 < V_{CM} < 5.5V, T_A < 0°C	65	95		dB
PSRR	10 < V_{CC} < 30V, T_A ≥ 0°C	80	110		dB
	10 < V_{CC} < 30V, T_A < 0°C	70	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	–0.5	–1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = 1mA	3.5	4.3	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth	(note 1)	3	5.5		MHz
Slew Rate	(note 1)	6	12		V/µs
PWM Comparator Section					
Pin 10 Bias Current	$V_{PIN\ 10}$ = 0V, $V_{PIN\ 23}$ = open, $V_{PIN\ 9}$ = 2V		–1	–10	µA
Duty Cycle Range	T_A ≥ 0°C	0		70	%
	T_A < 0°C	0		65	%
Pin 4 Zero DC Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		V
Delay to Output	(note 1)		50	80	ns
Ramp Compensation					
Pin 10 Current	$V_{PIN\ 9}$ = 2V, $R_{PIN\ 23}$ = 6.8KΩ	250	300	350	µA
Soft-Start/Reset Delay Section					
Charge Current (Pin 11)	$V_{PIN\ 11}$ = 0.5V	–3	–9	–20	µA
Discharge Current (Pin 11)	$V_{PIN\ 11}$ = 1V	1			mA
Discharge Current (Pin 12)	$V_{PIN\ 12}$ = 1V	3	9	20	µA
Charge Current (Pin 12)	$V_{PIN\ 12}$ = 0.5V	–0.4			mA
Current Limit/Shutdown Section					
Pin 15 Bias Current	0V < $V_{PIN\ 15}$ < 4V			±20	µA
Current Limit Threshold		1.0	1.1	1.2	V
Shutdown Threshold		1.35	1.50	1.65	V
Delay to Output	(note 1)		40	70	ns
Blanker Section					
T_{BLANK}	(note 1), RC = 5.1KΩ, 68pF	80	100	120	ns

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
Output Low Level	I_{OUT} = 20mA		0.25	0.4	V
	I_{OUT} = 200mA		1.2	2.2	V
Output High Level	I_{OUT} = –20mA	13.0	13.5		V
	I_{OUT} = –200mA	12.0	13.0		V
Collector Leakage	V_C = 30V		100	500	µA
Rise/Fall Time	C_L = 1000pF, (note 1)		30	60	ns
Logic Inputs/Outputs					
Pin 24 Threshold	(note 2)		V_{REF} – 0.98		V
Pin 13 V_{OH}	(note 2)		V_{REF} – 0.65		V
Pin 13 V_{OL}	(note 2)		V_{REF} – 1.3		V
Supply Current					
Start Up Current (note 2)	V_{CC} = 8V, T_A = 25°C		1.1	3.0	mA
	V_{CC} = 8V, T_A < 25°C			3.5	mA
I_{CC}	$V_{PIN\ 1,\ 10,\ 15}$ = 0V, $V_{PIN\ 2}$ = 1V, T_A = 25°C		29	38	mA

Note 1: This parameter not 100% tested in production but guaranteed by design.

Note 2: The thresholds on the logic input pins are set by a reference generator that is: $V_{TH} = V_{REF} - (1.5 \times V_{BE})$. The logic outputs swing from: $V_{OH} = V_{REF} - V_{BE}$ to $V_{OL} = V_{REF} - 2 \times V_{BE}$. V_{BE} is nominally 0.65V and varies with temperature. Logic inputs and outputs will track each other with temperature variation.

Note 3: Since the Under Voltage Lockout start-up threshold is 16V, the supply is first raised to 20V to activate the IC and then lowered to 15V to conduct the electrical testing.

Note 4: Reference short circuit current, Supply current and Start-up ICC decrease with increasing temperature.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4809 Voltage Controlled Oscillator charges the external capacitor (C_T) with a current (I_{CHARGE}) equal to V(VCO)/R_T. When the capacitor voltage reaches the upper threshold (Ramp Peak), the comparator changes state and the capacitor discharges to the lower threshold (Ramp Valley) through Q1. While the capacitor is discharging, Q2 provides a high pulse. For Fixed Frequency Operation, V(VCO) can be tied to V_{REF}.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where: T_{RAMP} = C (Ramp Valley to Peak)/I_{CHARGE}

and: $T_{DEADTIME}$ = C (Ramp Valley to Peak)/I_{DIS}

An approximate expression for the oscillator frequency in fixed frequency operation (where V(VCO) = V_{REF}) is:

$$F_{OSC} \approx \frac{2.48}{R_T C_T}$$

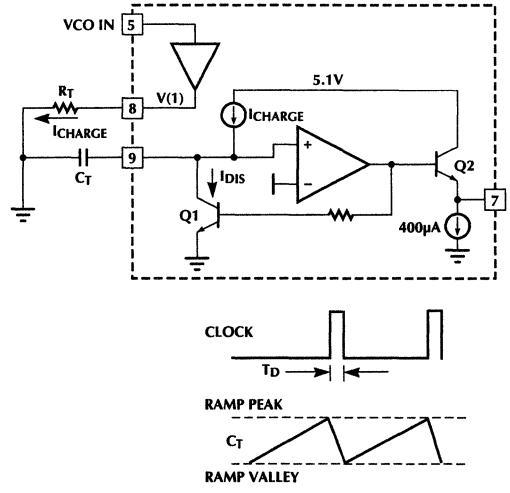


Figure 1. Oscillator Block Diagram.

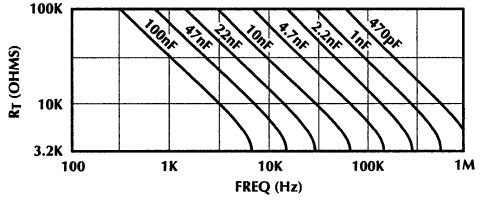


Figure 2. Timing Resistance vs Frequency (V(VCO) = 5.1V).

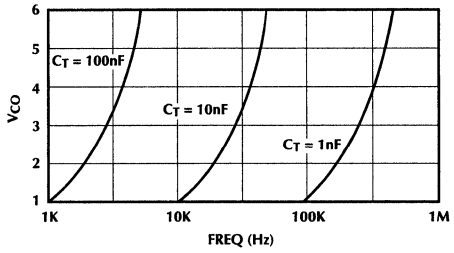


Figure 3. Oscillator Frequency vs V(VCO) (RC = 6.2KΩ, 1000pF).

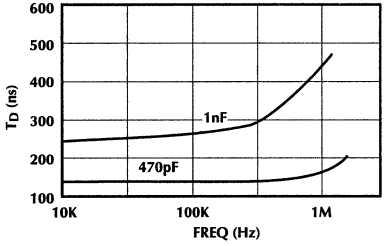


Figure 4. Oscillator Deadtime vs Frequency (V(VCO) = 5.1V).

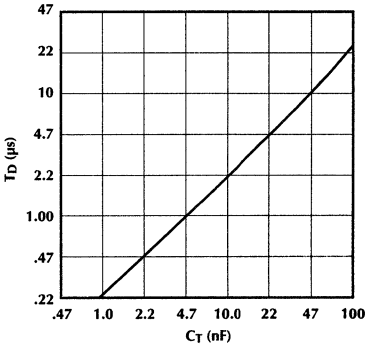


Figure 5. Oscillator Deadtime vs C(T) (3KΩ ≤ R(T) ≤ 100KΩ).

ERROR AMPLIFIER

The ML4809 error amplifier is a 3.5MHz bandwidth 6V/µs slew rate op-amp with provision for limiting the positive output voltage swing (Output Inhibit line) for ease in implementing the soft start function.

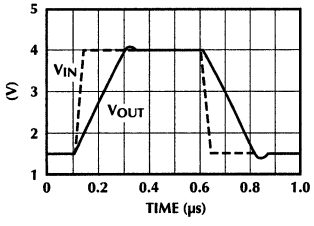


Figure 6. Unity Gain Slew Rate.

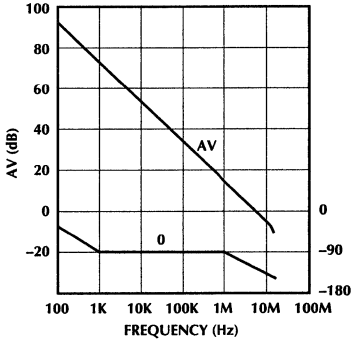


Figure 7. Open Loop Frequency Response.

OUTPUT DRIVER STAGE

The ML4809 Output Driver is a 2A peak output high speed totem pole circuit designed to drive capacitive loads, such as power MOSFET transistors.

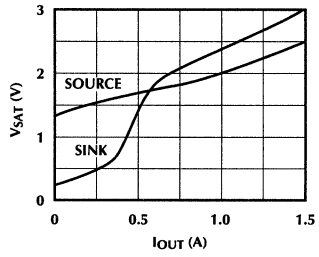


Figure 8. Saturation Curves.

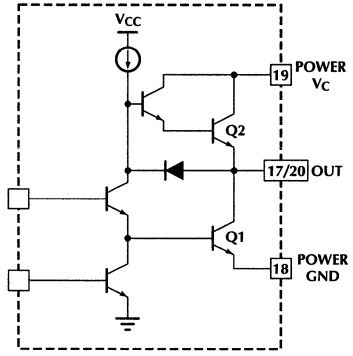


Figure 9. Simplified Schematic.

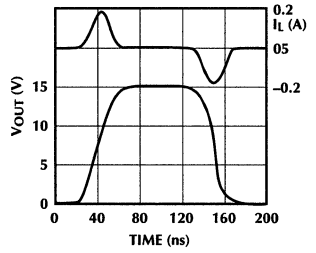


Figure 10a. Rise/Fall Time (C_L = 1000pF).

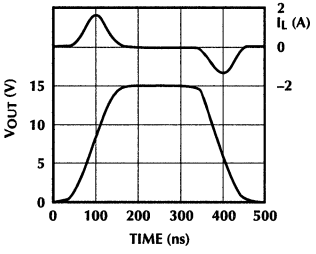


Figure 10b. Rise/Fall Time (CL = 10000pF).

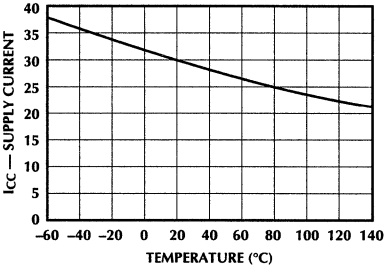


Figure 11. Supply Current vs Temperature.

SOFT START, CURRENT LIMIT, AND RESET DELAY

The ML4809 employs two current limits. When the voltage at pin 15 (I(LIM)/S.D.) exceeds 1.1V, the outputs immediately pull low and the cycle is terminated for the remainder of the oscillator period by resetting the RS flip flop.

If the output current is rising quickly (usually due to transformer saturation) such that the voltage on pin 15 reaches 1.5V before the outputs have turned off, a soft start cycle is initiated. The soft start capacitor (pin 11) is discharged and outputs are held "off" until the voltage at pin 11 reaches 1.1V, ensuring a complete soft start cycle. The duty cycle on start up is limited by limiting the output voltage of the error amplifier voltage to the voltage at pin 11.

The ML4809 also includes a delay circuit which inhibits the outputs from coming on until a time determined by the RESET DELAY capacitor on pin 12. This capacitor is normally charged to a voltage equal to $V_{PIN\ 11}$ – 0.7V and is limited to V_{REF}. After the 1.5V limit is reached, the capacitor is allowed to slowly discharge through the 9µA current sink. When this capacitor and the Soft Start Capacitor both have discharged to 1.1V, the outputs are enabled and the new soft start cycle begins. During Under Voltage Lockout, both capacitors will be discharged to prepare for a new cycle.

Since the emitter follower which drives pin 12 presents a load on Pin 11, the Soft Start Capacitor's effective value will be increased by:

$$C_{EFFECT} = C_{PIN\ 11} + (C_{PIN\ 12}/\beta)$$

where β varies from 50 to 250. Should this cause unacceptable variation on the soft start capacitor value, this effect can be mitigated by connecting a resistor from V_{REF} to pin 11 to charge the Soft Start Cap (select a resistor which keeps the charge current below 2mA).

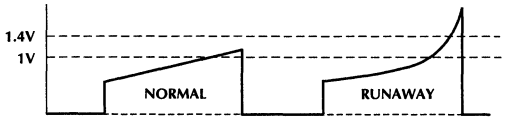


Figure 12. Normal (Cycle by Cycle) and "Runaway" Current Timing.

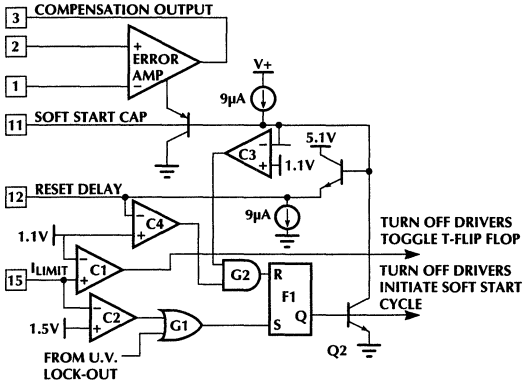


Figure 13. Current Limit, Soft Start and Reset Delay.

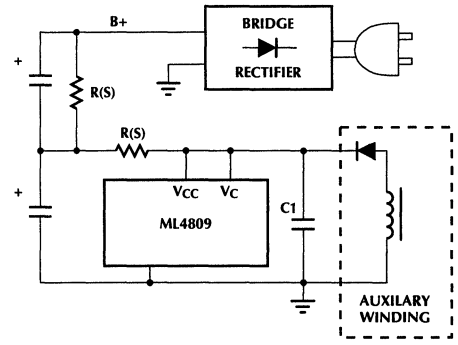
UNDERVOLTAGE LOCKOUT

In the circuit in Figure 14, the ML4809 remains in a low quiescent drain (1.1mA) during T1 while C1 charges through R(S) to 16V. After V_{CC} rises to 16V the ML4809 begins running. C1 provides the energy needed to run the gate drive and ML4809 until the auxilary winding can provide sustaining energy for the control circuit, preventing C1 from draining below the 9V lockout threshold. The 7V of hysteresis in the Undervoltage Lockout circuit allows the ML4809 to start from a bleed resistor/capacitor easily. While the ML4809 is in the standby (Lockout) condition, OUTA and OUTB will be pulled low.

RAMP COMPENSATION

In order to allow stable operation of a current mode regulator above 50% duty cycle, some of the oscillator ramp needs to be added to the current signal.

Notice that the waveform of (1) and the waveform of ramp (2) have different average current values. (1) is an example of a waveform for high line and (2) an example of low line. Since the controllers all regulate based on the peak value of the current in the circuit, and the control variable really wants to be the average current, adding some of the oscillator ramp to comparator input (shown here for clarity as a subtraction of the comparator reference input, which is the output of the error amplifier) allows the peak current control to more closely approximate the average current.



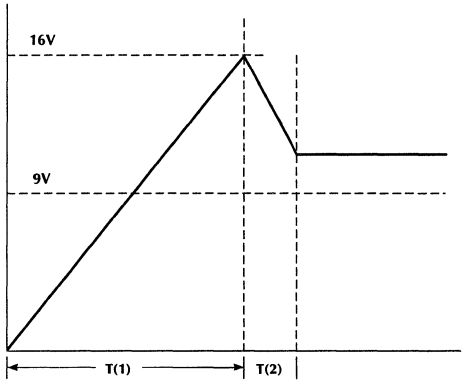


Figure 14. Typical Off-Line Start-Up Circuit and Timing.

In the actual implementation, an external resistor (pin 23) sets a current which will be equal to $V_{RAMP}/R1$ and will appear on the comparator input pin. Since the sense resistor is a low impedance point, putting another resistor (R2) in series with the V_{SENSE} pin (10) causes a voltage to add to the ramp voltage which is equal to V_{RAMP} (R2/R1).

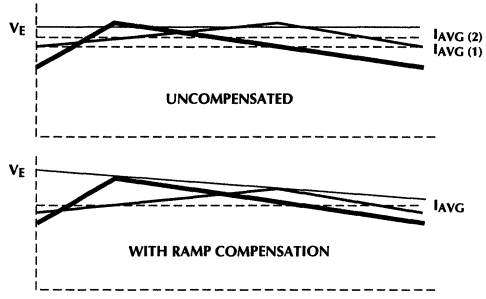


Figure 15. The Effect of Ramp Compensation

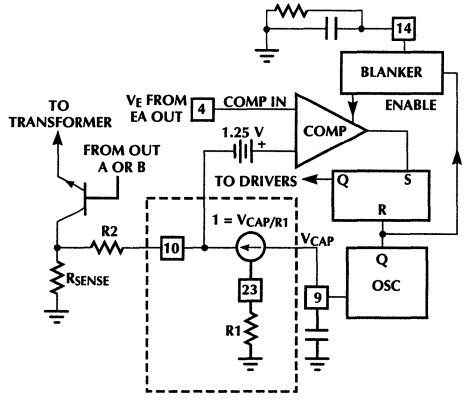


Figure 16. Ramp Compensation and Blanker Block Diagram.

MAIN COMPARATOR BLANKER

When CMP IN (EA OUT) is at a low level, spikes which occur on RAMP (which is connected to a current sense resistor or transformer) when the power MOSFETs first turn on can cause the cycle to terminate early. The result of early termination can cause instabilities. Three problems occur which all contribute to this spike.

1. Inductance in the sense resistor.
2. Inter-winding capacitance in the transformer.
3. Reverse recovery current in the rectifier in the opposite FET intrinsic diode (or from the secondary diodes).

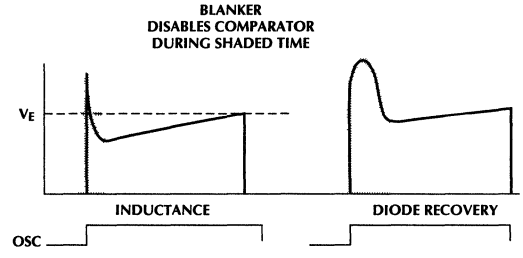


Figure 17. Unintended Early Cycle Termination.

The first two problems usually cause a fairly short spike which is easy to filter out with just a simple RC before the comparator input without causing unacceptable phase delay at the input, since there is not much area underneath the spike. The third problem can have significant energy, and a filter with a low enough pole to reduce the "spike" to a level low enough not to cause early cycle termination would cause excessive phase shift.

The solution is to provide a blanking pulse to the comparator at the beginning of the cycle. The width of this pulse is programmed by an external RC. When CLOCK IN is high, a buffer in the ML4809 charges the capacitor on pin 14 to 4V. When CLOCK goes low, the capacitor discharges through the external resistor. The outputs are held low until the voltage at pin 14 falls below 3.2V. The buffer driving pin 14 is limited to 5mA output current. The Blanking period can be calculated by the expression:

$$T_{BLANK} \approx \frac{R_{BLANK}C_{BLANK}}{2.83}$$

SYNCHRONIZATION INPUTS AND OUTPUTS

When using the Clock (pin 7) or Q (pin 13) outputs, a 5KΩ pull down resistor is recommended. These outputs are open emitters. Clock has an internal (375µA) current sink load while Q is unloaded. Both will exhibit significant timing skew due to PC board capacitance if not loaded.

Clock Output and External Input

Used to synchronize multiple supplies. For synchronized operation of multiple ML4809's, tie the CLOCK OUT from the "master" to the CLOCK IN of the slaves.

Toggle Preset and Q Output

In multiple supply systems, this is important for synchronization. To synchronize multiple chips, connect the Q output from the "master" ML4809 to the Preset Input of the "slave" in a daisy chain". For non-synchronized operation this input would be connected to GND.

OTHER FEATURES

Fast Shut Down Path from Current Limit to Outputs

Provides a 30ns path to the outputs which begins to turn off the outputs while the longer latching path is propagating. In a normal UC1825, it can be as much as 80ns until the over-current condition shuts down the outputs.

Separate Error Amplifier Output Pin for Loop Filtering Versatility

This is especially useful for:

1. Diagnostic purposes, to see what the chip is really doing, it is useful to break the feedback loop.
2. High power supplies — current sharing: In system design with more than one supply running, in order to ensure that the supplies share current equally it is often necessary to have a "master" circuit control the PWM operation of each of the "slaves". This is most easily accomplished by an "or" (where the lowest output dominates) of the Error Amp outputs which is impossible if the output of the amp is internally connected to the input of the comparator.

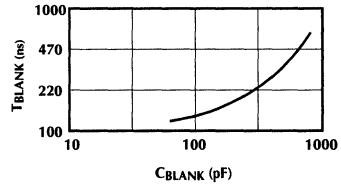


Figure 18. T_{BLANK} vs. C_{BLANK} (R_{BLANK} = 5.1KΩ).

APPLICATIONS

Figure 19 shows the ML4809 in a push-pull non-isolated application. Note the Schottky Diodes on pins 17 and 20. These diodes are necessary in order to prevent transients from driving these pins negative with respect to GND which would cause the IC to malfunction.

Care should be exercised in layout:

1. Avoid Ground Loops. Use "star" grounding.
2. Bypass the V_{CC} line with a high frequency capacitor which is physically close to the IC.
3. Avoid running signal lines near power lines.
4. Employ "ground planing".

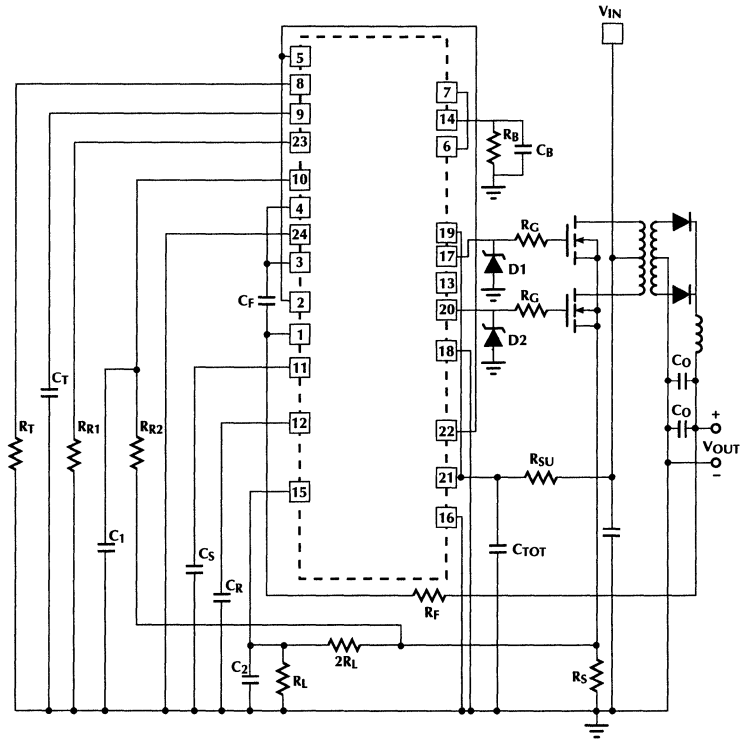


Figure 19. ML4809 Typical Application

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4809CP	0°C to +70°C	Molded DIP (P24N)
ML4809CQ	0°C to +70°C	Molded PCC (Q28)

ML4810, ML4811

High Frequency Power Supply Controller

GENERAL DESCRIPTION

The ML4810 and ML4811 High Frequency PWM Controllers are optimized for use in Switch Mode Power Supply designs running at frequencies to 1MHz. The ML4810/11 contain a unique overload protection circuit which helps to limit stress on the output devices and reliably performs a soft-start reset. Propagation delays are minimal through the comparators and logic for reliable high frequency operation and slew rate and bandwidth are maximized on the error amplifier. These controllers are designed to work in either voltage or current mode and provide for input voltage feed forward.

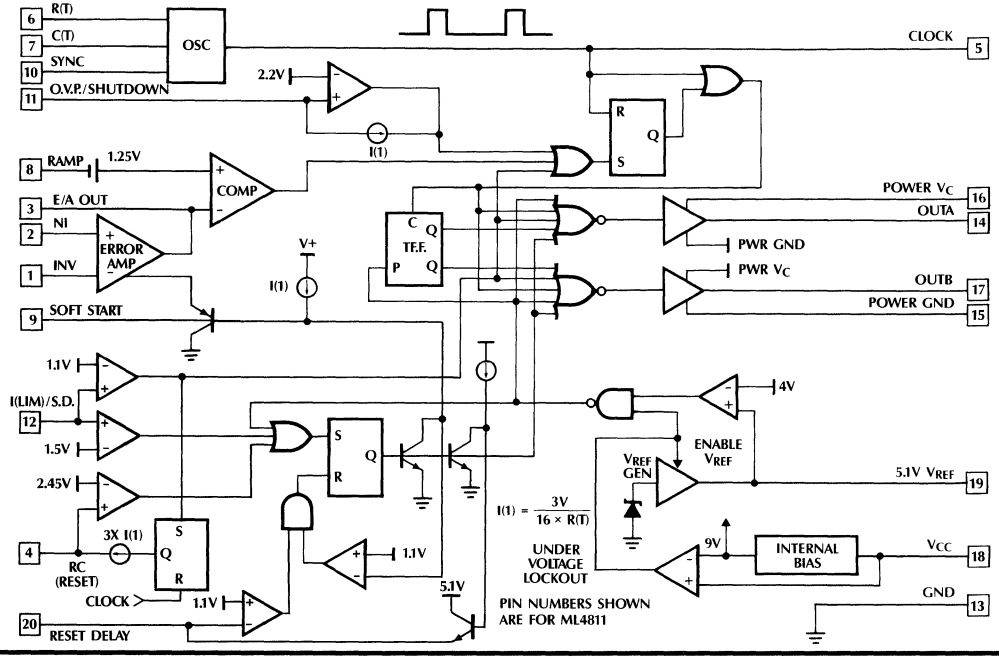
A 1.1V threshold current limit comparator provides a cycle-by-cycle current limit. An integrating circuit "counts" the number of times the 1.1V limit was reached. A soft-start cycle is initiated if the cycle-by-cycle current limit is repeatedly activated. A reset delay function is provided on the ML4811. All logic is fully latched to provide jitter-free operation and prevent multiple pulsing. An under-voltage lockout circuit with 7V of hysteresis assures low startup current and drives the outputs low during fault condition.

The ML4810/11 are fabricated on a 40V bipolar process from the FB3480 Power Supply Controller Array. Customized versions of this controller can therefore be easily implemented. Please refer to the FB3480 data sheet for more information. These controllers are similar to the UC1825 controller, however these controllers include many features not found on the 1825. These features are set in *Italics.*

FEATURES

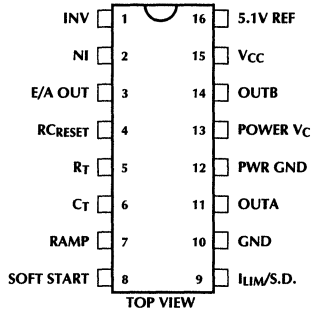
- *Integrating Soft Start Reset*
- High current (2A peak) dual totem pole outputs
- Practical operation to 1MHz (f_{OSC})
- 5.1V ±2% trimmed bandgap reference
- *Under voltage lockout with 7V hysteresis*
- *Soft Start Reset Delay (ML4811)*
- *Oscillator synchronization function (ML4811)*
- *Soft Start latch ensures full soft start cycle*
- *Outputs pull low for undervoltage lockout*
- *Accurately controlled oscillator ramp discharge current*
- *All timing currents "slaved" to R_T for precise control*

BLOCK DIAGRAM



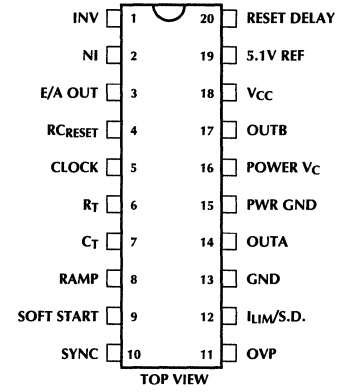
PIN CONFIGURATION

ML4810
16-Pin DIP (P16)



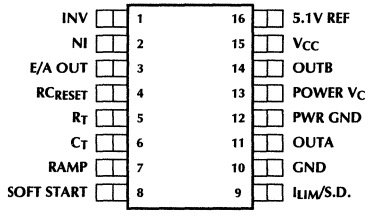
TOP VIEW

ML4811
20-Pin DIP (P20)



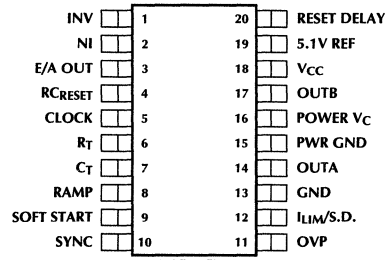
TOP VIEW

ML4810
16-Pin SOIC (S16W)



TOP VIEW

ML4811
20-Pin SOIC (S20W)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	INV	Inverting input to error amp.
2	NI	Non-inverting input to error amp.
3	E/A OUT	Output of error amplifier and input to main comparator.
4	RC_{RESET}	Timing elements for Integrating Soft Start reset.
5	CLOCK	Oscillator output.
6	R_T	Timing resistor for oscillator — sets charging current for oscillator timing capacitor (pin 6).
7	C_T	Timing capacitor for oscillator.
8	RAMP	Non-inverting input to main comparator. Connected to C_T for voltage mode operation or to current sense resistor for current mode.
9	SOFT START	Normally connected to Soft Start capacitor.
10	SYNC	A high going pulse terminates the PWM cycle and discharges C_T.
11	OVP	Exceeding 2.5V terminates the PWM cycle and inhibits the outputs.
12	I_{LIM}/S.D.	Current limit sense pin. Normally connected to current sense resistor.
13	GND	Analog signal ground.
14	OUTA	High current totem pole output. This output is the first one energized after power on reset.
15	PWR GND	Return for the high current totem pole outputs.
16	V_C	Positive supply for the high current totem pole outputs.
17	OUTB	High current totem pole output.
18	V_{CC}	Positive supply for the IC.
19	5.1V REF	Buffered output for the 5.1V voltage reference.
20	RESET DELAY	Timing capacitor to determine the amount of delay between fault.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 18, 16) 25V
Output Current, Source or Sink (Pins 14, 17)
DC 0.5A
Pulse (0.5µs) 2.0A
Analog Inputs
(Pins 1, 2, 8) ..... –0.3V to 7V
(Pins 9, 10, 11, 12, 20) ..... –0.3V to 6V
Clock Output Current (Pins 5) ..... –5mA
Error Amplifier Output Current (Pin 3) 5mA
Junction Temperature
ML4811M ..... 150°C
ML4811I, ML4810C, ML4811C, ML4810I ..... 125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP ..... 65°C/W
Ceramic DIP ..... 65°C/W
Plastic SOIC ..... 65°C/W

OPERATING CONDITIONS

Temperature Range
ML4810C, ML4811C ..... 0°C to +70°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial Accuracy	T_J = 25°C, (note 1)	360	400	440	KHz
Voltage Stability	10V < V_{CC} < 25V, (note 1)		0.2	4	%
Temperature Stability	(note 1)		5		%
Total Variation	line, temp, (note 1)	340		460	KHz
Clock Out High		3.9	4.5		V
Clock Out Low			2.3	2.9	V
Ramp Peak			2.8		V
Ramp Valley			1.0		V
Ramp Valley to Peak		1.6		2.3	V
Sync Input Threshold		0.8	1.0	1.4	V
Sync Input Current	$V_{PIN\ 10}$ = 4V				µA
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1mA	5.00	5.10	5.20	V
Line Regulation	10V < V_{CC} < 25V		2	20	mV
Load Regulation	1mA < I_O < 10mA		5	20	mV
Temperature Stability	–55°C < T_J < 150°C, (note 1)		0.2	0.4	%
Total Variation	line, load, temp, (note 1)	4.95		5.25	V
Output Noise Voltage	10Hz to 10KHz		50		µV
Long Term Stability	T_J = 125°C, 1000 hrs, (note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	–15	–50	–100	mA
Under-Voltage Lockout Section					
Start Threshold		15	16	17	V
UVLO Hysteresis		6.5	7	7.5	V

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current						
Start Up Current	ML4810	V_{CC} = 8V, $T_A \geq 0°C$ V_{CC} = 8V, $T_A < 0°C$		2.0 2.5	3.5 4.0	mA mA
	ML4811	V_{CC} = 8V, $T_A \geq 0°C$ V_{CC} = 8V, $T_A < 0°C$		2.5 3	4.0 4.5	mA mA
I_{CC}	ML4810	$V_{PIN\ 1,\ 7,\ 9}$ = 0V, $V_{PIN\ 2}$ = 1V, T_A = 25°C		32	46	mA
	ML4811	$V_{PIN\ 1,\ 7,\ 9}$ = 0V, $V_{PIN\ 2}$ = 1V, T_A = 25°C		38	55	mA
Error Amplifier Section						
Input Offset Voltage					±20	mV
Input Bias Current				0.6	3	µA
Input Offset Current				0.1	1	µA
Open Loop Gain		1 < V_O < 4V	60	96		dB
CMRR		1.5 < V_{CM} < 5.5V	65	95		dB
PSRR		10 < V_{CC} < 30V	75	90		dB
Output Sink Current		$V_{PIN\ 3}$ = 1V	1	2.5		mA
Output Source Current		$V_{PIN\ 3}$ = 4V	–0.5	–1.3		mA
Output High Voltage		$I_{PIN\ 3}$ = –0.5mA	4.0	4.7	5.0	V
Output Low Voltage		$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth		Note 1	3	5.5		MHz
Slew Rate		Note 1	6	12		V/µs
PWM Comparator Section						
Pin 8 Bias Current		$V_{PIN\ 8}$ = 0V		–1	–5	µA
Duty Cycle Range			0		75	%
Pin 3 Zero DC Threshold			1.1	1.25		V
Delay to Output		Note 1		50	80	ns
Soft-Start Section						
Charge Current (Pin 9)	ML4811	$V_{PIN\ 9}$ = 1V, $V_{PIN\ 4,\ 12}$ = 0	–35	–55	–75	µA
Discharge Current (Pin 9)		$V_{PIN\ 9}$ = 3V, $V_{PIN\ 4}$ > 2.5	1	5		mA
		$V_{PIN\ 9}$ = 3V, $V_{PIN\ 12}$ > 1.65, $V_{PIN\ 4}$ < 2	1	5		mA
Charge Current (Pin 20)		$V_{PIN\ 20}$ = 1V	1	5		mA
Discharge Current (Pin 20)		Requires external discharge resistor		0		µA
Current Limit/Shutdown Section						
Pin 12 Bias Current		0V < $V_{PIN\ 12}$ < 4V			+15	µA
Current Limit Threshold	ML4810		1.2	1.3	1.4	V
	ML4811		0.95	1.1	1.3	V
Reset Threshold (Pin 12)	ML4810	$V_{PIN\ 4}$ < 2V	1.60	1.75	1.90	V
	ML4811	$V_{PIN\ 4}$ < 2V	1.4	1.50	1.8	V
Delay to Output		Note 1		40	70	ns
Pin 4 Charging Current		$V_{PIN\ 12}$ = 2V	120	150	180	µA
Restart Threshold (Pin 4)			2	2.45	3	V
OVP Shutdown Threshold (Pin 11)			2.4	2.7	2.8	V
OVP Input Current		$V_{PIN\ 11}$ = 3V	40	50	60	µA
Charge Current (Pin 8)	ML4810	$V_{PIN\ 8}$ = 1V, $V_{PIN\ 4,\ 9}$ = 0	–40	–50	–60	µA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
Output Low Level	I_{OUT} = 20mA		.25	.4	V
	I_{OUT} = 200mA		1.2	2.2	V
Output High Level	I_{OUT} = -20mA	12.5	13.5		V
	I_{OUT} = -200mA	12.0	13.0		V
Collector Leakage	V_C = 30V		100	500	μA
Rise/Fall Time	C_L = 1000pF, (note 1)		30	80	ns

Note 1: This parameter not 100% tested in production but guaranteed by design.

FUNCTIONAL DESCRIPTION

SOFT START AND CURRENT LIMIT — INTEGRATING SOFT START RESET

The ML4810/11 offers a unique system of fault detection and reset. Most PWM controllers use a two threshold method which relies on the buildup of current in the output inductor during a fault. This buildup occurs because:

1. Inductor di/dt is a small number when the switch is off under load fault (short circuit) conditions, since V_L is small.
2. Some energy is delivered to the inductor since the IC must first detect the over-current because there is a finite delay before the output switch can turn off.

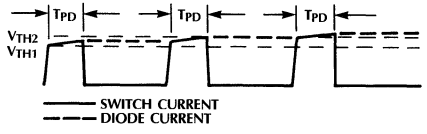


Figure 1. Current Waveforms for Slow Turn-Off System with Load Fault

This scheme was adequate for controllers with longer comparator propagation delays and turn-off delays than is desirable in a high frequency system. For systems with low propagation delays, very little energy will be delivered to the inductor and the current "ratcheting" described above will not occur. This results in the controller never detecting the load fault and continuing to pump full current to the load indefinitely, causing heating in the output rectifiers and inductor.

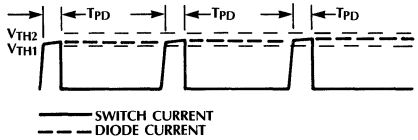


Figure 2. Current Waveforms for High Speed System with Load Fault

A method of circumventing this problem involves "counting" the number of times the controller terminates the PWM cycle due to the cycle by cycle current limit.

When the switch current crosses the 1.1V threshold A1 signals the F1 to terminate the cycle and sets F3, which is reset at the beginning of the PWM cycle. The output of F3 turns on a current source to charge C2. When, after several cycles, C2 has charged to 2.45V, A5 turns on F2 to discharge soft start capacitor C1. Charge is continually bled from C2 by R1. If a current surge is short lived (for instance a disk drive start-up or a board being plugged into a live rack) the control can "ride

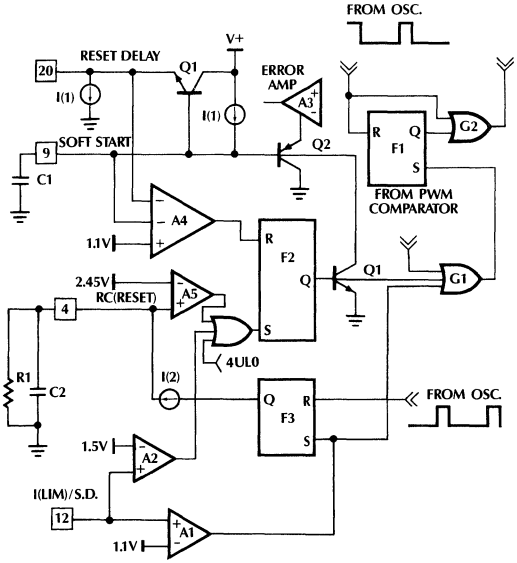


Figure 3. Integrating Soft Start Reset

out" the surge with the switch protected by the cycle by cycle limit. R1 and C1 can be selected to track diode heating, or to ride out various system surge requirements as required.

If the high current demanded is caused by a short circuit, the duty cycle will be short and the output diodes will carry the current for the majority of the PWM cycle. C2 charges fastest for low duty cycles (since F3 will be on for a longer time) providing for quicker shutdown during short-circuit when the output diodes are being maximally stressed.

OSCILLATOR

The ML4811 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $3/R_T$. When the capacitor voltage reaches the upper threshold (Ramp Peak), the comparator changes state and the capacitor discharges to the lower threshold (Ramp Valley) through Q1. While the capacitor is discharging, Q2 provides a high pulse. A discharge of the oscillator can be initiated by applying a high level to the Sync pin. A short pulse of a frequency higher than the oscillator's free running frequency can be used to synchronize the ML4811 to an external clock. The pulse can be equal to the desired deadtime (T_D) or the deadtime can be determined by I_{DIS} and C_T, whichever is greater.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where: $T_{RAMP} = C$ (Ramp Valley to Peak)$/I_{SET}$

and: $T_{DEADTIME} = C$ (Ramp Valley to Peak)$/I_{Q1}$

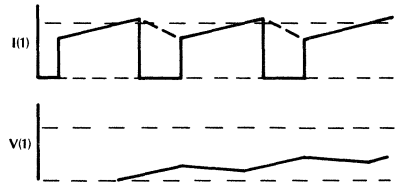


Figure 4. Switching Current and Pin 4 Voltage — Normal

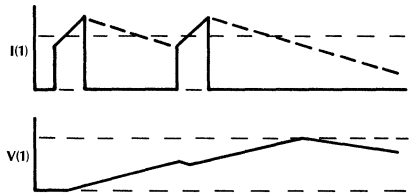


Figure 5. Switching Current and Pin 4 Voltage — Load Fault

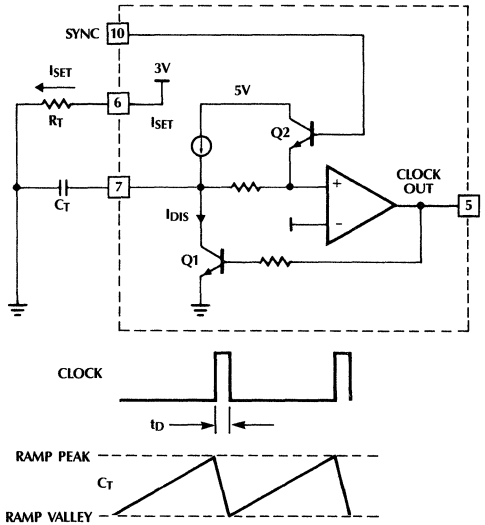


Figure 6. Simplified Oscillator Block Diagram and Timing

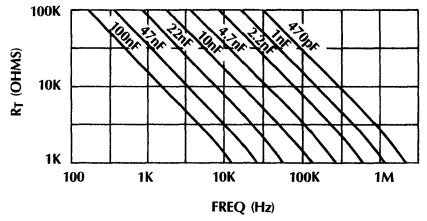


Figure 7. Oscillator Timing Resistance vs. Frequency

ERROR AMPLIFIER

The ML4811 error amplifier is a 5.5MHz bandwidth 12V/μsec slew rate op-amp with provision for limiting the positive output voltage swing (Output Inhibit line) for ease in implementing the soft start function.

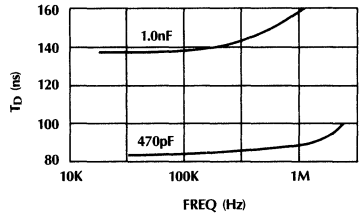


Figure 8. Oscillator Deadtime vs Frequency

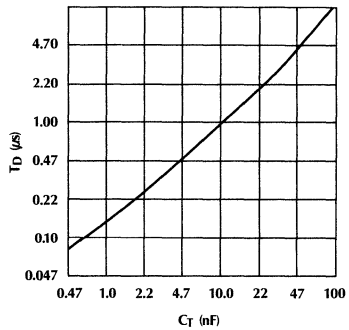


Figure 9. Oscillator Deadtime vs C(T) ($3 \leq R(T) \leq 100K\Omega$)

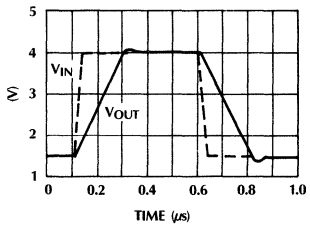


Figure 10. Unity Gain Slew Rate

OUTPUT DRIVER STAGE

The ML4811 Output Driver is a 2A peak output high speed totem pole circuit designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors.

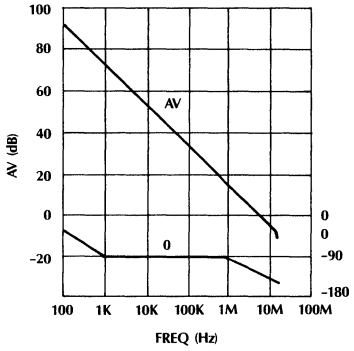


Figure 11. Open Loop Frequency Response

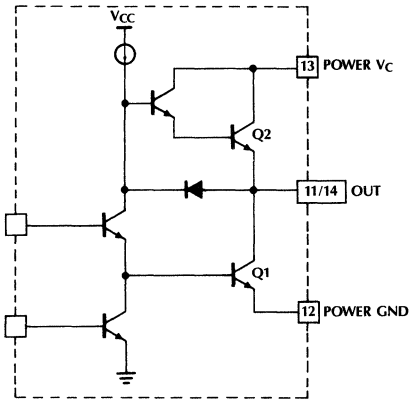


Figure 12. Simplified Schematic

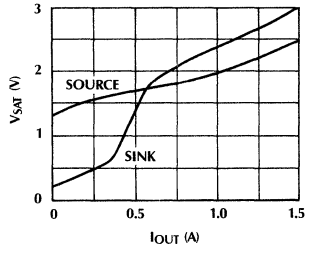


Figure 13. Saturation Curves

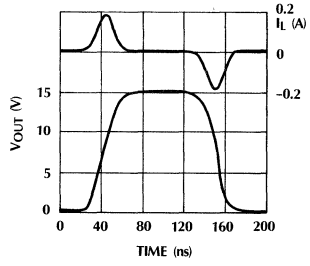


Figure 14. Rise/Fall Time (CL = 1000pF)

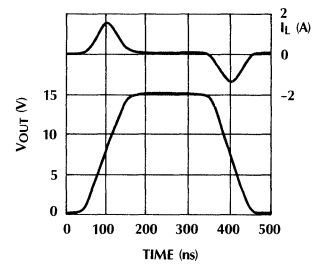


Figure 15. Rise/Fall Time (CL = 10,000pF)

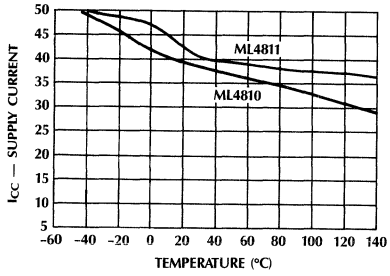


Figure 16. Supply Current vs. Temperature

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4810CP	0°C to +70°C	16-Pin Molded DIP (P16)
ML4810CS	0°C to +70°C	16-Pin Molded SOIC (S16W)
ML4811CP	0°C to +70°C	20-Pin Molded DIP (P20)
ML4811CS	0°C to +70°C	20-Pin Molded SOIC (S20W)

ML4812

Power Factor Controller

GENERAL DESCRIPTION

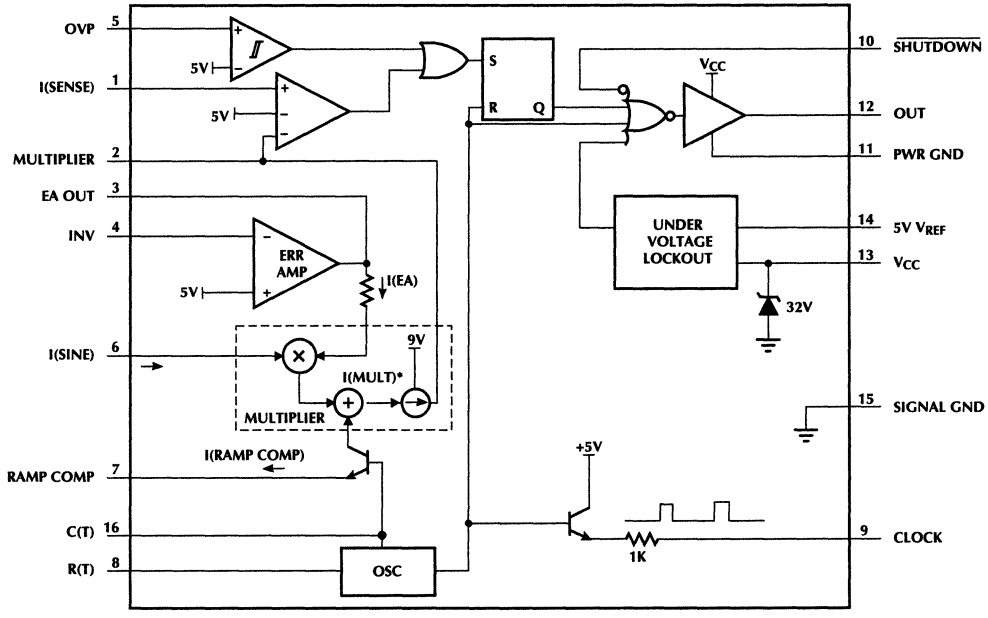
The ML4812 is designed to optimally facilitate a "boost" type power factor correction system. Special care has been taken in the design of the ML4812 to increase system noise immunity. The circuit includes a precision reference, multiplier, error amplifier, over-voltage protection, ramp compensation, as well as a high current output. In addition, start-up is simplified by an under-voltage lockout circuit with 6V hysteresis.

In a typical application, the ML4812 functions as a current mode regulator. The current which is necessary to terminate the cycle is a product of the sinusoidal line voltage times the output of the error amplifier which is regulating the output DC voltage. Ramp compensation is programmable with an external resistor, to provide stable operation when the duty cycle exceeds 50%.

FEATURES

- Precision buffered 5V reference (±0.5%)
- Current input multiplier reduces external components and improves noise immunity
- Programmable ramp compensation circuit
- 1A peak current totem-pole output drive
- Over-voltage comparator eliminates output "runaway" due to load removal
- Wide common mode range in current sense comparators for better noise immunity
- Large oscillator amplitude for better noise immunity

BLOCK DIAGRAM (Pin Out shown is for DIP)

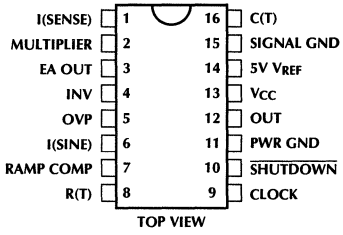


* I(MULT) ∝ I(SINE) x I(EA) – [I(RAMP COMP) ÷ 2]

Patented

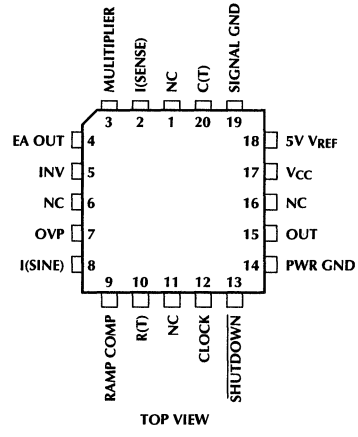
PIN CONFIGURATION

ML4812
16-Pin DIP (P16)



TOP VIEW

ML4812
20-Pin PCC (Q20)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	I(SENSE)	Input from the current sense transformer (T1) to the PWM comparator (+).
2	MULTIPLIER	Output of current multiplier. A resistor to ground on this pin converts the current to a voltage. This pin is clamped to 5V and tied to the PWM comparator (–).
3	EA OUT	Output of error amplifier.
4	INV	Inverting input to error amplifier.
5	OVP	Input to over voltage comparator.
6	I(SINE)	Current multiplier input.
7	RAMP COMP	Buffered output from the oscillator ramp [C(T)]. A resistor to ground sets the current which is internally subtracted from the product of I(SINE) and I(EA) in the multiplier.
8	R(T)	Oscillator timing resistor pin. A 5V source sets a current in the external resistor which is mirrored to charge C(T).
9	CLOCK	Digital clock output.
10	$\overline{\text{SHUTDOWN}}$	A TTL compatible low level on this pin turns off the output.
11	PWR GND	Return for the high current totem pole output.
12	OUT	High current totem pole output.
13	V_{CC}	Positive Supply for the IC.
14	5V V_{REF}	Buffered output for the 5V voltage reference.
15	SIGNAL GND	Analog signal ground.
16	C(T)	Timing capacitor for the oscillator.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 30mA
Output Current Source or Sink (pin 12)
DC 1.0A
Output Energy (capacitive load per cycle) 5µJ
Multiplier I(SINE) Input (pin 6) 1.2mA
Error Amp Sink Current (pin 3) 10mA
Oscillator Charge Current 2mA
Analog Inputs (pins 1, 4, 5) ..... –0.3V to 5.5V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic Chip Carrier (PCC) — Q ..... 60°C/W
Plastic DIP — P ..... 65°C/W
Ceramic DIP — J ..... 65°C/W

OPERATING CONDITIONS

Temperature Range
ML4812C ..... 0°C to +70°C
ML4812I ..... –40°C to +85°C
ML4812M ..... –55°C to +125°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 14KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V (note 2), Pin numbers refer to 16-pin DIP package.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial Accuracy	T_J = 25°C	91	98	105	KHz
Voltage Stability	12V < V_{CC} < 18V		0.3		%
Temperature Stability			2		%
Total Variation	line, temp.	90		108	KHz
Ramp Valley to Peak			3.3		V
R(T) Voltage		4.8	5.0	5.2	V
Discharge Current (pin 8 open)	T_J = 25°C, $V_{PIN\ 16}$ = 2V	7.8	8.4	9.0	mA
	$V_{PIN\ 16}$ = 2V	7.3	8.4	9.3	mA
Clock Out Voltage Low	R_L = 16KΩ		0.2	0.5	V
Clock Out Voltage High	R_L = 16KΩ	3.0	3.5		V
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	V
Line Regulation	12V < V_{CC} < 25V		2	20	mV
Load Regulation	1mA < I_O < 20mA		2	20	mV
Temperature Stability			0.4		%
Total Variation	line, load, temp.	4.9		5.1	V
Output Noise Voltage	10Hz to 10KHz		50		µV
Long Term Stability	T_J = 125°C, 1000 Hrs (note1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	–30	–85	–180	mA
Error Amplifier Section					
Input Offset Voltage				±15	mV
Input Bias Current			–0.1	–1.0	µA
Open Loop Gain	1 < $V_{PIN\ 3}$ < 5V	60	75		dB
PSRR	12V < V_{CC} < 25V	60	75		dB
Output Sink Current	$V_{PIN\ 3}$ = 1.1V, $V_{PIN\ 4}$ = 6.2V	2	12		mA
Output Source Current	$V_{PIN\ 3}$ = 5.0V, $V_{PIN\ 4}$ = 4.8V	–0.5	–1.0		mA
Output High Voltage	$I_{PIN\ 3}$ = –0.5mA, $V_{PIN\ 4}$ = 4.8V	5.3	5.5		V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA, $V_{PIN\ 4}$ = 6.2V		0.5	1.0	V
Unity Gain Bandwidth			1.0		MHz

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Multiplier					
I(SINE) Input Voltage	I(SINE) = 500µA	0.4	0.7	0.9	V
Output Current (pin 2)	I(SINE) = 500µA, Pin 4 = V_{REF} –20mV	460	480	510	µA
	I(SINE) = 500µA, Pin 4 = V_{REF} + 20mV		3	10	µA
	I(SINE) = 1mA, Pin 4 = V_{REF} – 20mV	900	950	1020	µA
	I(SINE) = 500µA, Pin 4 = V_{REF} – 20mV, $I_{PIN\ 7}$ = 50µA		455		µA
Bandwidth			200		KHz
PSRR	12V < V_{CC} < 25V		70		dB
OVP Comparator					
Input Offset Voltage	Output Off	–25		+5	mV
Hysteresis	Output On	95	105	115	mV
Input Bias Current			–0.3	–3	µA
Propagation Delay			150		ns
PWM Comparator: I(SENSE)					
Input Offset Voltage				±15	mV
Input Offset Current				±1	mA
Input Common Mode Range		–0.2		5.5	V
Input Bias Current			–2	–10	µA
Propagation Delay			150		ns
I_{LIMIT} Trip Point	$V_{PIN\ 2}$ = 5.5V	4.8	5	5.2	V
Output Section					
Output Voltage Low	I_{OUT} = –20mA		0.1	0.4	V
	I_{OUT} = –200mA		1.6	2.2	V
Output Voltage High	I_{OUT} = 20mA	13	13.5		V
	I_{OUT} = 200mA	12	13.4		V
Output Voltage Low in UVLO	I_{OUT} = –5mA, V_{CC} = 8V		0.1	0.8	V
Output Rise/Fall Time	C_L = 1000pF		50		ns
Shut Down Input	V_{IH}	2.0			V
	V_{IL}			0.8	V
	I_{IL}, $V_{PIN\ 10}$ = 0V			–1.5	mA
	I_{IH}, $V_{PIN\ 10}$ = 5V			10	µA
Under-Voltage Lockout					
Start-Up Threshold		15	16	17	V
Shut-Down Threshold		9	10	11	V
V_{REF} Good Threshold			4.4		V
Total Device					
Supply Current	Start-Up, V_{CC} = 14V, T_J = 25°C		0.8	1.2	mA
	Operating, T_J = 25°C		20	25	mA
Internal Shunt Zener Voltage	I_{CC} = 30mA	25	30	34	V

Note 1: This parameter not 100% tested in production but guaranteed by design.
Note 2: V_{CC} is raised above the Start-Up Threshold first to activate the IC, then returned to 15V.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4812 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $5/R_{SET}$. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where:

$$T_{RAMP} = \frac{C_T \times V_{RAMP\ VALLEY\ TO\ PEAK}}{I_{SET}}$$

and:

$$T_{DEADTIME} = \frac{C_T \times V_{RAMP\ VALLEY\ TO\ PEAK}}{8.4mA - I_{SET}}$$

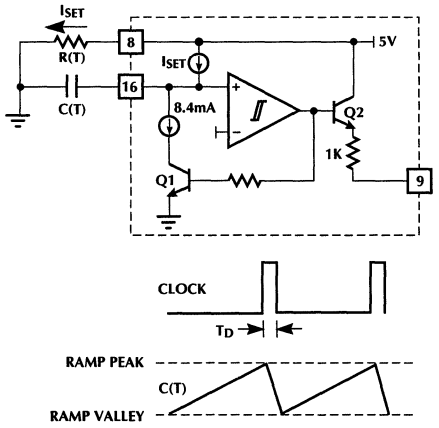


Figure 1. Oscillator Block Diagram

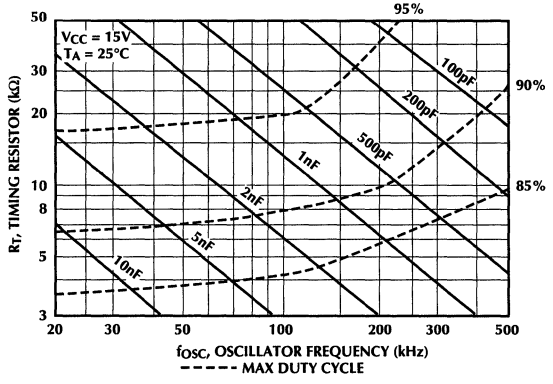


Figure 2. Oscillator Timing Resistance vs. Frequency

OUTPUT DRIVER STAGE

The ML4812 Output Driver is a 1A peak output high speed totem pole circuit designed to quickly drive capacitive loads, such as power MOSFET gates.

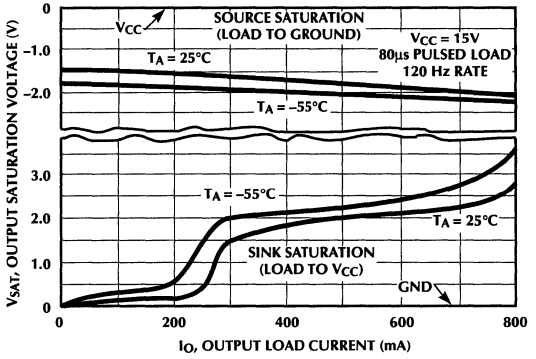


Figure 3. Output Saturation Voltage vs. Output Current

ERROR AMPLIFIER

The ML4812 error amplifier is a high open loop gain, wide bandwidth, amplifier.

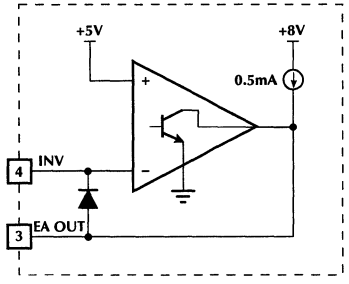


Figure 4. Error Amplifier Configuration

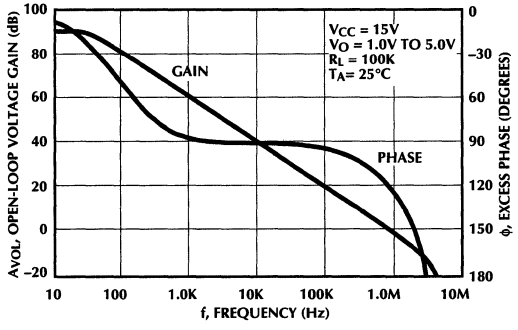


Figure 5. Error Amplifier Open-Loop Gain and Phase vs Frequency

MULTIPLIER

The ML4812 multiplier is a linear current input multiplier to provide high immunity to the disturbances caused by high power switching. The rectified line input sine wave is converted to a current via a dripping resistor. In this way, small amounts of ground noise produce an insignificant effect on the reference to the PWM comparator.

The output of the multiplier is a current proportional to:

$$I_{OUT} \propto I(SINE) \times I(EA)$$

where I(SINE) is the current in the dropping resistor, and I(EA) is a current proportional to the output of the error amplifier. When the error amplifier is saturated high, the output of the multiplier is approximately equal to the I(SINE) input current.

The multiplier output current is converted into the reference voltage for the PWM comparator through a resistor to ground on the multiplier output. The multiplier output is clamped to 5V to provide current limiting.

Ramp compensation is accomplished by subtracting 1/2 of the current flowing out of pin 7 through a buffer transistor driven by C(T) which is set by an external resistor.

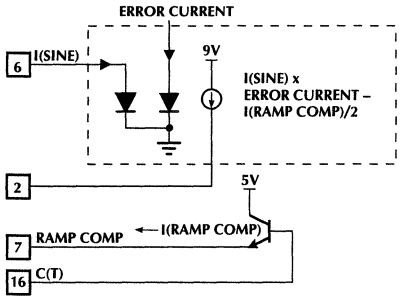


Figure 6. Multiplier Block Diagram

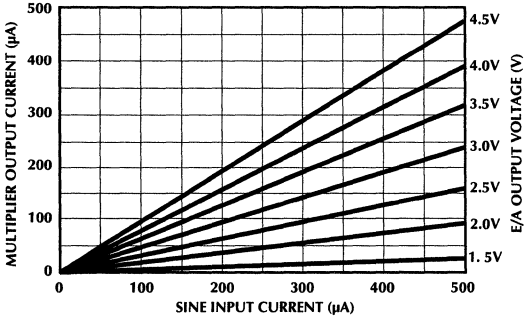


Figure 7. Multiplier Linearity

UNDER VOLTAGE LOCKOUT

On power-up the ML4812 remains in the UVLO condition; output low and quiescent current low. The IC becomes operational when V_{CC} reaches 16V. When V_{CC} drops below 10V, the UVLO condition is imposed. During the UVLO condition, the 5V V_{REF} pin is "off", making it usable as a "flag" for starting up a downstream PWM converter.

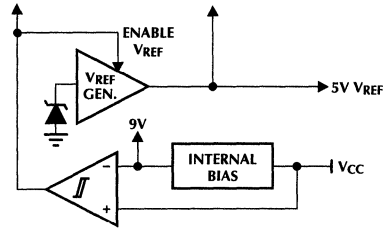


Figure 8. Under-Voltage Lockout Block Diagram

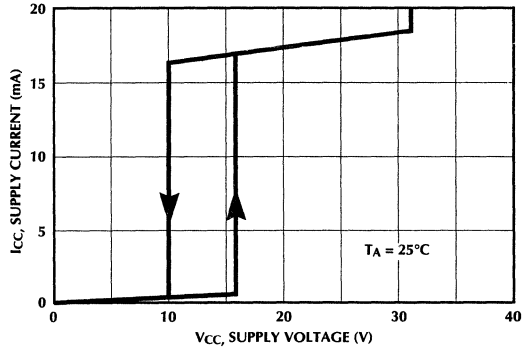


Figure 9a. Total Supply Current vs. Supply Voltage

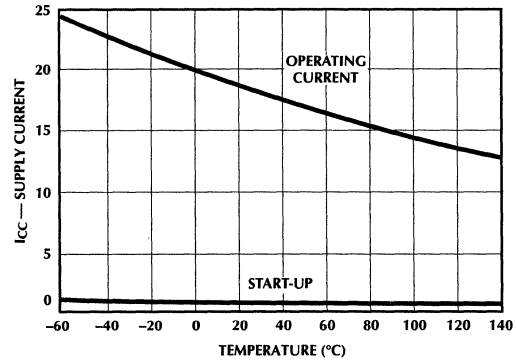


Figure 9b. Supply Current (I_{CC}) vs. Temperature

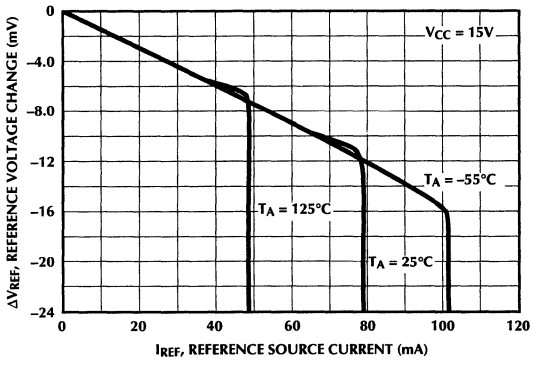


Figure 10. Reference Load Regulation

APPLICATIONS

INPUT INDUCTOR (L1) SELECTION

The central component in the regulator is the input boost inductor. The value of this inductor controls various critical operational aspects of the regulator. If the value is too low, the input current distortion will be high and will result in low power factor and increased noise at the input. This will require more input filtering. In addition, when the value of the inductor is low the inductor dries out (runs out of current) at low currents. Thus the power factor will decrease at lower power levels and/or higher line voltages. If the inductor value is too high, then for a given operating current the required size of the inductor core will be large and/or the required number of turns will be high. So a balance must be reached between distortion and core size.

One more condition where the inductor can dry out is analyzed below where it is shown to be maximum duty cycle dependent.

For the boost converter at steady state:

$$V_{OUT} = \frac{V_{IN}}{1-D_{ON}} \quad (1)$$

Where D_{ON} is the duty cycle $[T_{ON}/(T_{ON} + T_{OFF})]$. The input boost inductor will dry out when the following condition is satisfied:

$$V_{IN}(t) < V_{OUT} \times (1-D_{ON}) \quad (2)$$

or

$$V_{INDRY} = [1-D_{ON}(max)] \times V_{OUT} \quad (3)$$

V_{INDRY}: Voltage where the inductor dries out.
V_{OUT}: Output dc voltage.

Effectively, the above relationship shows that the resetting volt-seconds are more than setting volt-seconds. In energy transfer terms this means that less energy is stored in the inductor during the ON time than it is asked to deliver during the OFF time. The net result is that the inductor dries out.

The recommended maximum duty cycle is 95% at 100KHz to allow time for the input inductor to dump its energy to the output capacitors.

For example:

if: V_{OUT} = 380V and
D_{ON} (max) = 0.95

then substituting in (3) yields V_{INDRY} = 20V. The effect of drying out is an increase in distortion at low voltages.

For a given output power, the instantaneous value of the input current is a function of the input sinusoidal voltage waveform, i.e. as the input voltage sweeps from zero volts to a maximum value equal to its peak so does the current.

The load of the power factor regulator is usually a switching power supply which is essentially a constant power load. As a result, an increase in the input voltage will be offset by a decrease in the input current.

By combining the ideas set forth above, some ground rules can be obtained for the selection and design of the input inductor:

Step 1: Find minimum operating current.

$$I_{IN}(min)_{PEAK} = \frac{1.414 \times P_{IN}(min)}{V_{IN}(max)} \quad (4)$$

$V_{IN}(max)$ = 260V

$P_{IN}(min)$ = 50W

then: $I_{IN}(min)_{PEAK}$ = 0.272A

Step 2: Choose a minimum current at which point the inductor current will be on the verge of drying out. For this example 40% of the peak current found in step 1 was chosen.

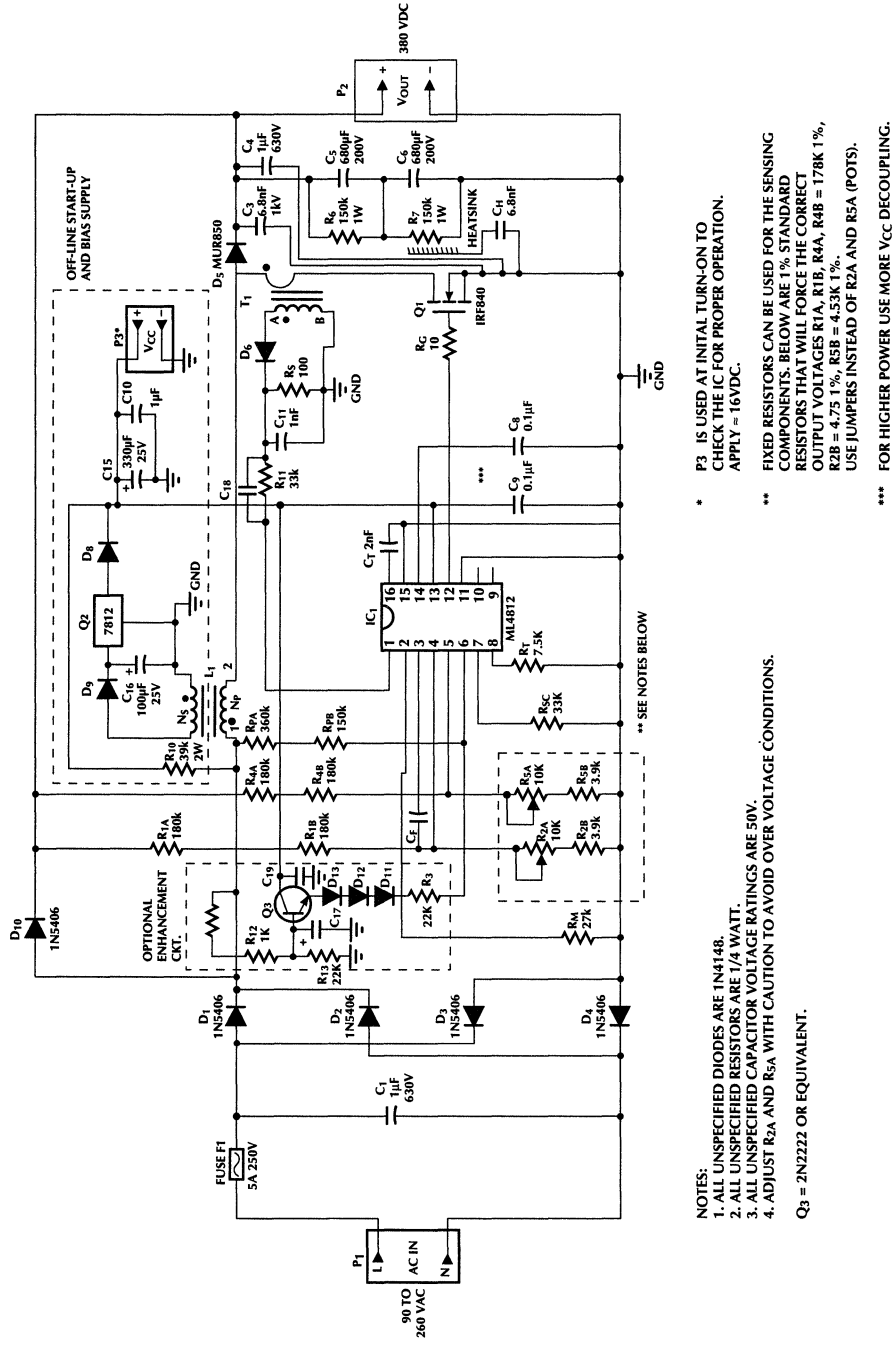
then: I_{LDRY} = 100mA

Step 3: The value of the inductance can now be found using previously calculated data.

$$L1 = \frac{V_{INDRY} \times D_{ON}(max)}{I_{LDRY} \times f_{OSC}} = \frac{20V \times 0.95}{100mA \times 100KHz} = 2mH \quad (5)$$

The inductor can be allowed to decrease in value when the current sweeps from minimum to maximum value. This allows the use of smaller core sizes. The only requirement is that the ramp compensation must be adequate for the lower inductance value of the core so that there is adequate compensation at high current.

7



* P3 IS USED AT INITAL TURN-ON TO CHECK THE IC FOR PROPER OPERATION. APPLY ≈ 16VDC.

** FIXED RESISTORS CAN BE USED FOR THE SENSING COMPONENTS. BELOW ARE 1% STANDARD RESISTORS THAT WILL FORCE THE CORRECT OUTPUT VOLTAGES R1A, R1B, R4A, R4B = 178K 1%, R2B = 4.75 1%, R5B = 4.53K 1%. USE JUMPERS INSTEAD OF R2A AND R5A (POTS).

*** FOR HIGHER POWER USE MORE V_{CC} DECOUPLING. 2µF OR MORE BE REQUIRED AT 1KW LEVELS.

NOTES:
1. ALL UNSPECIFIED DIODES ARE 1N4148.
2. ALL UNSPECIFIED RESISTORS ARE 1/4 WATT.
3. ALL UNSPECIFIED CAPACITOR VOLTAGE RATINGS ARE 50V.
4. ADJUST R_{2A} AND R_{5A} WITH CAUTION TO AVOID OVER VOLTAGE CONDITIONS.

Q_3 = 2N2222 OR EQUIVALENT.

Figure 11. Typical Application, 200W Power Factor Correction Circuit

Step 4: The presence of the ramp compensation will change the dry out point, but the value found above can be considered a good starting point. Based on the amount of power factor correction the above value of L1 can be optimized after a few iterations.

Gapped Ferrites, Molypermalloy, and Powdered Iron cores are typical choices for core material. The core material selected should have a high saturation point and acceptable losses at the operating frequency.

One ferrite core that is suitable at around 200W is the #4119PL00-3C8 made by Ferroxcube. This ungapped core will require a total gap of 0.180" for this application.

OSCILLATOR COMPONENT SELECTION

The oscillator timing components can be calculated by using the following expression:

$$f_{OSC} = \frac{1.36}{R_T \times C_T} \quad (6)$$

For example:

Step 1: At 100KHz with 95% duty cycle T_{OFF} = 500ns calculate C_T using the following formula:

$$C_T = \frac{T_{OFF} \times I_{DIS}}{V_{OSC}} = 1000pF \quad (7)$$

Step 2: Calculate the required value of the timing resistor.

$$R_T = \frac{1.36}{f_{OSC} \times C_T} = \frac{1.36}{100KHz \times 1000pF} \quad (8)$$

$$= 13.6K\Omega \text{ choose } R_T = 14K\Omega.$$

CURRENT SENSE AND SLOPE (RAMP) COMPENSATION COMPONENT SELECTION

Slope compensation in the ML4812 is provided internally. Rather than adding slope to the noninverting input of the PWM comparator it is actually subtracted from the voltage present at the inverting input of the PWM comparator. The amount of slope compensation should be at least 50% of the downslope of the inductor current during off time as reflected to the inverting input of the PWM comparator. Note that slope compensation is required only when the inductor current is continuous and the duty cycle is more than 50%. The downslope of the inductor current at the verge of discontinuity can be found using the expression given below:

$$\frac{di_L}{dt} = \frac{V_{OUT} - V_{IN\,DRY}}{L} = \frac{380V - 20V}{2mH} = 0.18\,A/\mu s \quad (9)$$

The downslope as reflected to the input of the PWM comparator is given by:

$$S_{PWM} = \frac{V_{OUT} - V_{IN\,DRY}}{L} \times \frac{R_S}{N_C} \quad (10)$$

Where R_S is the current sense resistor and N_C is the turns ratio of the current transformer (T1) used. In general, current transformers simplify the sensing of switch currents especially at high power levels where the use of sense resistors is complicated by the amount of power they have to dissipate. Normally the primary side of the transformer consists of a single turn and the secondary consists of several turns of either enameled magnet wire or insulated wire. The diameter of the ferrite core used in this example is 0.5" (SPANG/Magnetics F41206-TC). The rectifying diode at the output of the current transformer can be a 1N4148 for secondary currents up to 75mA average.

Sense FETs or resistive sensing can also be used to sense the switch current, the sensed signal has to be amplified to the proper level before it is applied to the ML4812.

The value of the ramp compensation (SC_{PWM}) as seen at the inverting terminal of the PWM comparator is:

$$SC_{PWM} = \frac{2.5 \times R_M}{R_T \times C_T \times R_{SC}} \quad (11)$$

The required value for R_{SC} can therefore be found by equating:

$$SC_{PWM} = A_{SC} \times S_{PWM}$$

where A_{SC} is the amount of slope compensation and solving for R_{SC}.

The value of R_M (pin 2) depends on the selection of R_P (pin 6)

$$R_P = \frac{V_{IN}(max)_{PEAK}}{I_{SINE}(peak)} = \frac{260 \times 1.414}{0.5mA} = 750K \quad (12)$$

$$R_M = \frac{V_{CLAMP} \times R_P}{V_{IN}(min)_{PEAK}} = \frac{4.9 \times 750K}{90 \times 1.414} = 28.8K \quad (13)$$

The peak of the inductor current can be found approximately by:

$$I_{LPEAK} = \frac{1.414 \times P_{OUT}}{V_{IN}(min)_{RMS}} = \frac{1.414 \times 200}{90} = 3.14A \quad (14)$$

Selection of N_C which depends on the maximum switch current, assume 4A for this example is 80 turns.

$$R_S = \frac{V_{CLAMP} \times N_C}{I_{LPEAK}} = \frac{4.9 \times 80}{4} = 100\Omega \quad (15)$$

Where R_S is the sense resistor, and V_{CLAMP} is the current clamp at the inverting input of the PWM comparator. This clamp is internally set to 5V. In actual application it is a good idea to assume a value less than 5V to avoid unwanted current limiting action due to component tolerances. In this application V_{CLAMP} was chosen as 4.9V.

Having calculated R_S the value S_{PWM} and of R_{SC} can now be calculated:

$$S_{PWM} = \frac{380V - 20}{2mH} \times \frac{100}{80} = 0.225V/\mu s$$

$$R_{SC} = \frac{2.5 \times R_M}{A_{SC} \times S_{PWM} \times R_T \times C_T}$$

$$R_{SC} = \frac{2.5 \times 28.8K}{0.7 \times (0.225 \times 10^6) \times 14K \times 1nF} = 33K \quad (16)$$

The following values were used in the calculation:

$R_M = 28.8K$ $A_{SC} = 0.7$
$R_T = 14K$ $C_T = 1nF$

VOLTAGE REGULATION COMPONENTS

The values of the voltage regulation loop components are calculated based on the operating output voltage. Note that voltage safety regulations require the use of sense resistors that have adequate voltage rating. As a rule of thumb if 1/4W resistors are available, two of them should be used in series. The input bias current of the error amplifier is approximately 0.5µA, therefore the current available from the voltage sense resistors should be significantly higher than this value. Since two 1/4W resistors have to be used the total power rating is 1/2W. The operating power is set to be 0.4W then with 380V output voltage the value can be calculated as follows:

$$R_1 = (380V)^2 / 0.4W = 360K \quad (17)$$

Choose two 178K, 1% connected in series.

Then R2 can be calculated using the formula below:

$$R_2 = \frac{V_{REF} \times R_1}{V_{OUT} - V_{REF}} = \frac{5V \times 356K}{380V - 5V} = 4.747K \quad (18)$$

Choose 4.75K, 1%. One more critical component in the voltage regulation loop is the feedback capacitor for the error amplifier. The voltage loop bandwidth should be set such that it rejects the 120Hz ripple which is present at the output. If this ripple is not adequately attenuated it will cause distortion on the input current waveform. Typical bandwidths range anywhere from a few Hertz to 15Hz. The main compromise is between transient response and distortion. The feedback capacitor can be calculated using the following formula:

$$C_F = \frac{1}{3.142 \times R_1 \times BW}$$

$$C_F = \frac{1}{3.142 \times 356K \times 2Hz} = 0.44\mu F \quad (19)$$

OVERVOLTAGE PROTECTION (OVP) COMPONENTS

The OVP loop should be set so that there is no interaction with the voltage control loop. Typically it should be set to a level where the power components are safe to operate. Ten to fifteen volts above V_{OUT} seems to be adequate. This sets the maximum transient output voltage to about 395V.

By choosing the high voltage side resistor of the OVP circuit the same way as above i.e. R_4 = 356K then R_5 can be calculated as:

$$R_5 = \frac{V_{REF} \times R_4}{V_{OVP} - V_{REF}} = \frac{5V \times 356K}{395V - 5V} = 4.564K \quad (20)$$

Choose 4.53K, 1%.

Note that R_1, R_2, R_4 and R_5 should be tight tolerance resistors such as 1% or better.

CONTROLLER SHUTDOWN

The ML4812 provides a shutdown pin which could be used to shutdown the IC. Care should be taken when this pin is used because power supply sequencing problems could arise if another regulator with its own bootstrapping follows the ML4812. In such a case a special circuit should be used to allow for orderly start up. One way to accomplish this is by using the reference voltage of the ML4812 to inhibit the other controller IC or to shut down its bias supply current.

OFF-LINE START-UP AND BIAS SUPPLY GENERATION

The ML4812 can be started using a "bleed resistor" from the high voltage bus. After the voltage on pin 13 (V_{CC}) exceeds 16V, the IC starts up. The energy stored on the 330µF, C15, capacitor supplies the IC with running power until the supplemental winding on L1 can provide the power to sustain operation.

The values of the start-up resistor R10 and capacitor C15 may need to be optimized depending on the application. The charging waveform for the secondary winding of L1 is an inverted chopped sinusoid which reaches its peak when the line voltage is at its minimum. In this example, C9 = 0.1µF, C15 = 330µF, D8 = 1N4148, R10 = 39K, 2W.

ENHANCEMENT CIRCUIT

The theory of operation of the power factor enhancement circuit (inside the dotted lines) in Figure 11 is described in Application Note 11 in detail. It improves the power factor and lowers the input current harmonics. Note that the circuit meets the proposed IEC 555 specifications (with the enhancement) on the harmonics with a large margin while correcting the input power factor to better than 0.99 under most steady state operating conditions.

CONSTRUCTION AND LAYOUT TIPS

High frequency power circuits require special care during breadboard construction and layout. Double sided printed circuit boards with ground plane on one side are highly recommended. All critical switching leads (power FET, output diode, IC output and ground leads, bypass capacitors) should be kept as small as possible. This is to minimize both the transmission and pick-up of switching noise.

There are two kinds of noise coupling; inductive and capacitive. As the name implies inductive coupling is due to fast changing (high di/dt) circulating switching currents. The main source is the loop formed by Q1, D5, and C3–C4. Therefore this loop should be as small as possible, and the above capacitors should be good high frequency types.

The second form of noise coupling is due to fast changing voltages (high dv/dt). The main source in this case is the drain of the power FET. The radiated noise in this case can be minimized by insulating the drain of the FET from the heatsink and then tying the heatsink to the source of the FET with a high frequency capacitor (C_H in Figure 11).

The IC has two ground pins named PWR GND and Signal GND. These two pins should be connected together with a very short lead at the printed circuit board exit point. In general grounding is very important and ground loops should be avoided. Star grounding schemes are preferred.

Component Values/Bill of Materials for Figure 11

Reference	Description
C1, C4	1µF, 630V FILM (250 VAC)
C3, C_H	6.8nF 1KV Ceramic disk
C5, C6	680µF 200V Electrolytic
C8, C9	0.1µF 50V Ceramic
C10, C19	1µF 50V Ceramic
C11	0.001µF 50V Ceramic
C15	330µF 25V Electrolytic
C16	100µF 25V Electrolytic
C17	10µF 25V Electrolytic
C_F	0.47µF 50V Ceramic
C_T	0.002µF 50V Ceramic
D1, D2, D3, D4, D10	1N5406 (Motorola)
D5	MUR850 (Motorola)
D6, D8, D9 D11, D12, D13	1N4148
F1	5A 250V 3AG with clips
IC1	ML4812CP (Micro Linear)
L1	2mH, 4A I_{PEAK} (see below)
Q1	IRF840 or MTPN8N50

Reference	Description
Q2	LM7815CT
Q3	2N2222 or equivalent
R1A, R1B, R4A, R4B	180KΩ
R2A, R5A	10KΩ TRIMPOT BOURNS 3299 or equivalent
R2B, R5B	3.9KΩ
R3, R13	22KΩ
R6, R7, RPB	150KΩ
R10	39KΩ, 2W
R11	33KΩ
R12	1KΩ
RG	10Ω
RM	27KΩ
RPA, R15	360KΩ
RS	100KΩ
RSC	33KΩ
RT	7.5KΩ
T1	SPANG F41206-TC N_S = 80, N_P = 1 (see attached)

Notes: All resistors 1/4W unless otherwise specified. Some reference designators are skipped (e.g. C2, C12, etc.) and do not appear on the schematic. These designators were used in previous revisions of the board and are not used on this revision. Additional information on key components is included in the attached appendix.

Magnetics Tips (Refer to Figure 11)

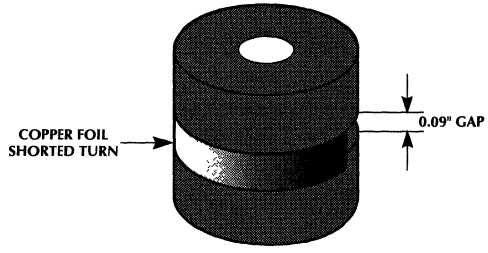
L1 — Main Inductor:

One of several toroidal cores can be used for L1:

Material	Manufacturer	Part #	Turns (#24AWG)
Powdered Iron	Micrometals	T225-8/90	200
Powdered Iron	Micrometals	T184-40	120
Molypermalloy	SPANG (Mag. Inc.)	58076-A2 (high flux)	180

The T184-40 core above is the most economical, but has lower inductance at high current. This would yield higher ripple current and require more line EMI filtering. The value for RSC (slope compensation resistor on Pin 7) was calculated for the T225-8/90 and should be recalculated for other inductor characteristics. Selected pages of the Micrometals iron powder core data sheets are attached for your convenience. The core manufacturer also has additional applications literature available.

A gapped ferrite core can also be used in place of the powdered iron core. One such core is a Ferroxcube core #4229PL00-3C8. This is an un-gapped core. Using 145 turns of #24 AWG wire, a total air gap of 0.180" is required to give a total inductance of about 2mH. Since 1/2 of the gap will be on the outside of the core and 1/2 the gap on the inside, putting a 0.09" spacer in the center will yield a 0.180" total gap. To prevent leakage fields from generating RFI, a shorted turn of copper tape should be wrapped around the gap as shown below:



For production, a gapped center leg can be ordered from most core vendors, eliminating the need for the external shorted copper turn when using a pot core.

T1 — Sense Transformer

In addition to the core type mentioned in the parts list, the following Siemens cores should be suitable for substitution and may be more readily available in Europe.

Material	Size Code	Part #
N27	R16/6.3	B64290-K45-X27
N30	R16/6.3	B64290-K45-X830

The N27 material is for high frequency and will work better above 100KHz but both are adequate. In addition, Ferroxcube/Phillips Magnetics core 768T188-3C8 can be used.

U.S. Core Vendors:

Manufacturer	Phone Number
SPANG/Magnetics Inc.	(412) 282-8282
Micrometals	(800) 356-5977
Ferroxcube/Phillips Magnetics	(818) 998-7311

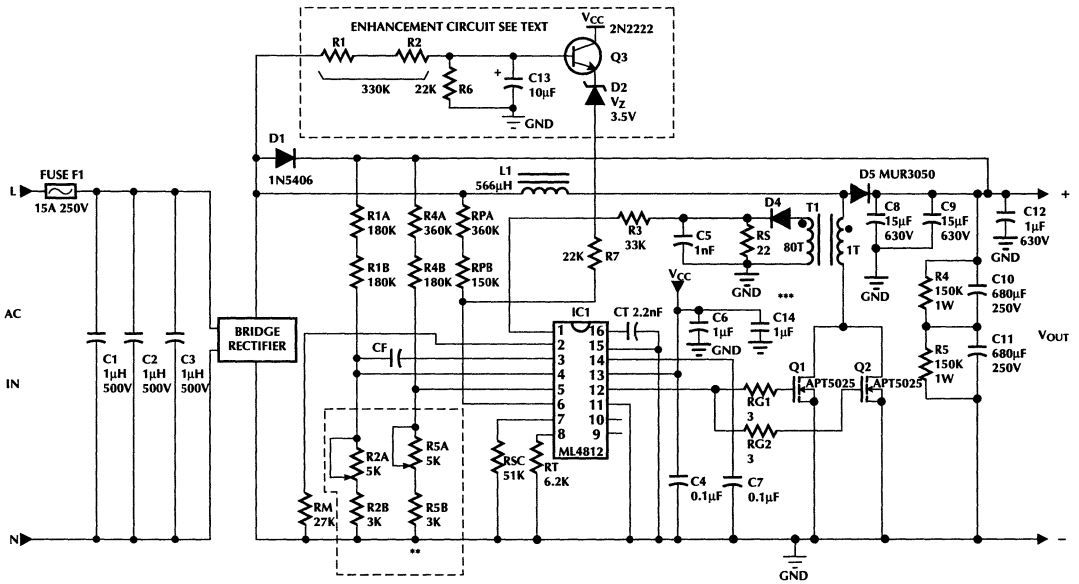


Figure 12. 1KW Input Power, Power Factor Correction Circuit

NOTES:
1. ALL UNSPECIFIED DIODES ARE 1N4148.
2. ALL UNSPECIFIED RESISTORS ARE 1/4 WATT.
3. ALL UNSPECIFIED CAPACITOR VOLTAGE RATINGS ARE 50V.
4. ADJUST R_{2A} AND R_{5A} WITH CAUTION TO AVOID OVER VOLTAGE CONDITIONS.

Q_3 = 2N2222 OR EQUIVALENT.

* AT INITIAL TURN-ON TO CHECK THE IC FOR PROPER OPERATION, APPLY ≈ 16VDC.

** FIXED RESISTORS CAN BE USED FOR THE SENSING COMPONENTS. BELOW ARE 1% STANDARD RESISTORS THAT WILL FORCE THE CORRECT OUTPUT VOLTAGES R1A, R1B, R4A, R4B = 178K 1%, R2B = 4.75 1%, R5B = 4.53K 1%. USE JUMPERS INSTEAD OF R2A AND R5A (POTS).

*** FOR HIGHER POWER USE MORE V_{CC} DECOUPLING.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4812CP	0°C to +70°C	Molded DIP (P16)
ML4812CQ	0°C to +70°C	Molded DIP (Q20)
ML4812IP	–40°C to +85°C	Molded DIP (P16)
ML4812IQ	–40°C to +85°C	Molded DIP (Q20)
ML4812MJ	–55°C to +125°C	Hermetic DIP (J16)

ML4812EVAL

Power Factor Controller Evaluation Kit

GENERAL DESCRIPTION

The ML4812EVAL kit provides a convenient vehicle to evaluate the ML4812 Power Factor Correction circuit. The board implements a 200W "boost" type power factor correction system. Special care has been taken in the layout of this PC board to provide adequate space for probes and a large area for ground plane to increase system noise immunity.

This kit includes a blank PC board, schematic of a complete power factor correction system and specifications for the key external components necessary to build a prototype Power Factor Correction front end. The unit is designed to operate over 90VAC to 256VAC line range and can run from no load to a full 200W. Higher power levels can be achieved using this board by using larger external components.

This boost mode converter is set to run with a 380V output and achieves power factors of better than .99 over a wide range of input line and output load.

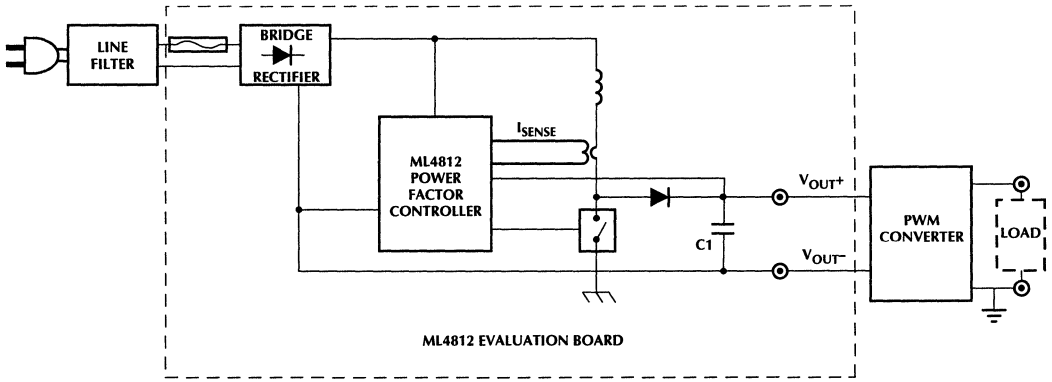
FEATURES

- Power Factor > .99
- Harmonic currents well below proposed IEC555-2 limits.
- 90 to 256VAC input, 380V output to 200W
- 380VDC output to 200W
- Over-Voltage Protection
- Peak Current sense circuit protects Power MOSFET
- PC board and ML4812CP controller included
- Line and Load regulation better than 2%
- Complete documentation and applications information

KIT COMPONENTS

- User's Guide
- ML4812 Datasheet
- ML4812 Sample
- Evaluation Board
- Powder Iron Toroidal Core

BLOCK DIAGRAM



Micro Linear

ML4813

Flyback Power Factor Controller

GENERAL DESCRIPTION

The ML4813 is designed to optimally facilitate a discontinuous "flyback" or "buck-boost" type power factor correction system for low power, low cost applications. Special care has been taken in the design of the ML4813 to reject system noise. The circuit includes a precision reference, oscillator, error amplifier, over-voltage comparator, over-current comparator, and an extra op-amp as well as a high current output. In addition, start-up is simplified by an under-voltage lockout circuit with 6V hysteresis.

In a typical application, the ML4813 functions as a voltage mode regulator. By maintaining a constant duty cycle, the current follows the input voltage, making the impedance of the entire circuit appear purely resistive. With the flyback circuit, power factors of .99 are easily achievable with a small output inductor and a minimum of external components.

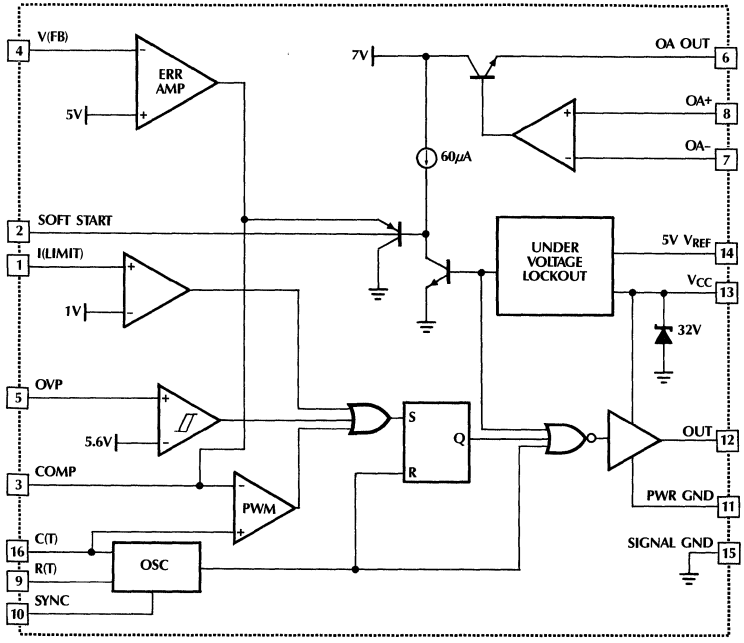
FEATURES

- Precision buffered 5V reference (±1%)
- Extra op-amp for output voltage instrumentation amplifier
- Over Current comparator for switch protection
- Soft Start and 6V hysteresis under-voltage lockout for easy low surge off-line starting
- 1 A Peak Current Totem-Pole Output Drive
- Over-Voltage comparator eliminates output "runaway" due to load removal
- Large oscillator amplitude for better noise immunity

APPLICATIONS

- PC power supplies
- Lamp Ballasts

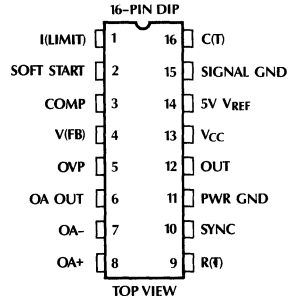
BLOCK DIAGRAM (Pin out shown is for DIP)



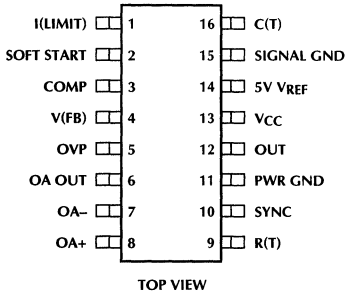
Micro Linear

PIN CONFIGURATION

ML4813
16-Pin DIP



ML4813
16-Pin SOIC



PIN DESCRIPTION (DIP)

PIN #	NAME	FUNCTION
1	I(LIMIT)	Current limit sense pin. Normally connected to sense resistor. When this pin exceeds 1V, the PWM cycle is terminated.
2	SOFT START	Normally connected to a Soft Start capacitor.
3	COMP	Output of error amplifier and input to PWM comparator.
4	V(FB)	Control loop feedback voltage.
5	OVP	Input to over voltage comparator.
6	OA OUT	Output of uncommitted op-amp.
7	OA–	Negative input of uncommitted op-amp.
8	OA+	Positive input of uncommitted op-amp.
9	R(T)	Oscillator timing resistor pin. A 5V source sets a current in the external resistor which is mirrored to charge C(T).
10	SYNC	Input used to synchronize the oscillator to an external source.
11	PWR GND	Return for the High Current Totem pole output.
12	OUT	High Current Totem pole output.
13	V_{CC}	Positive Supply for the IC.
14	5V V_{REF}	Buffered output for the 5V voltage reference.
15	SIGNAL GND	Analog signal ground.
16	C(T)	Timing Capacitor for the Oscillator.

7

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 40mA
Output Current, Source or Sink (Pin 12)
DC 1.0A
Output Energy (capacitive load per cycle) 5μJ
Error Amp Sink Current (pin 3) 10mA
Oscillator Charge Current 5mA
Analog Inputs (pins 1, 3–8) ..... –0.3V to 5.5V

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP or SOIC ..... 65°C/W

OPERATING CONDITIONS

Temperature Range
ML4813C ..... 0°C to 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 14KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial Accuracy	T_J = 25°C	90	97	104	KHz
Voltage Stability	12V < V_{CC} < 18V		0.3		%
Temperature Stability			2		%
Total Variation	line, temp.	88		108	KHz
Ramp Valley			1.0		V
Ramp Peak			4.3		V
R(T) Voltage		4.8	5.0	5.2	V
Discharge Current (pin 8 open)	T_J = 25°C, $V_{PIN\ 16}$ = 2V	7.5	8.4	9.3	mA
	$V_{PIN\ 16}$ = 2V	7.2	8.4	9.5	mA
Sync Pulse Threshold		.8	1.4	2.0	V
Sync Input Bias Current			350	800	μA
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	V
Line Regulation	12V < V_{CC} < 25V		6	20	mV
Load Regulation	1mA < I_O < 20mA		3	20	mV
Temperature Stability			.4		%
Total Variation	line, load, temp.	4.9		5.1	V
Output Noise Voltage	10Hz to 10KHz		50		μV
Long Term Stability	T_J = 125°C, 1000 Hrs, (note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	–30	–85	–180	mA
Error Amplifier Section					
Input Offset Voltage		–15		15	mV
Input Bias Current			–0.1	–1.0	μA
Open Loop Gain	1 < $V_{PIN\ 3}$ < 5V	60	75		dB
PSRR	12V < V_{CC} < 25V	60	70		dB
Output Sink Current	$V_{PIN\ 3}$ = 1.1V, $V_{PIN\ 4}$ = 6.2V	2	12		mA
Output Source Current	$V_{PIN\ 3}$ = 5.0V, $V_{PIN\ 4}$ = 4.8V	–0.5	–1.0		mA
Output High Voltage	$I_{PIN\ 3}$ = –0.5mA, $V_{PIN\ 4}$ = 4.8V	5.3	6.4		V
Output Low Voltage	$I_{PIN\ 3}$ = 2mA, $V_{PIN\ 4}$ = 6.2V		0.5	1.0	V
Unity Gain Bandwidth			1.0		MHz

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 14KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V (note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Un-Committed Op Amp					
Input Offset Voltage		-10		10	mV
Input Bias Current			-0.1	-2.0	μA
Input Offset Current		-0.35		0.35	μA
Open Loop Gain			90		dB
PSRR		80	125		dB
Output High Voltage	$I_{PIN\ 3}$ = -10mA	6.5	8		V
Output Low Voltage	$R_{L(PIN\ 6)}$ = 10KΩ		.2	.5	V
I(LIMIT) Comparator					
Input Trip Point	Output Off	.8	1.0	1.2	V
Input Bias Current			-2	-15	μA
Propagation Delay			150		nS
OVP Comparator					
Input Trip Point	Output Off	5.5	5.6	5.7	V
Hysteresis	Output On		100		mV
Input Bias Current			-0.3	-3	μA
PWM Comparator					
Input Common Mode Range		-0.2		5.5	V
Input Bias Current			-2	-10	μA
Propagation Delay			150		nS
Soft Start Section					
Soft Start Current (pin 2)	$V_{PIN\ 2}$ = 1V	40	60	80	μA
Output Section					
Output Voltage Low	I_{OUT} = 10mA		0.1	0.4	V
	I_{OUT} = 200mA		1.2	2.2	V
Output Voltage High	I_{OUT} = -20mA	13	13.6		V
	I_{OUT} = -200mA	12	13.4		V
Output Voltage Low in UVLO	I_{OUT} = 5mA, V_{CC} = 8V		0.1	0.8	V
Output Rise/Fall Time	C_L = 1000pF		50		nS
Under-Voltage Lockout					
Start-up Threshold		15	16	17	V
Shut-Down Threshold		9	10	11	V
V_{REF} Good Threshold			4.4		V
Total Device					
Supply Current	Start-up, V_{CC} = 14V		.9	1.5	mA
	Operating		20	30	mA
Internal Shunt Zener Voltage	I_{CC} = 30mA	25	30	34	V

Note 1: This parameter not 100% tested in production but guaranteed by design.
Note 2: V_{CC} is raised above the Start-up Threshold first to activate the IC, then returned to 15V.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4813 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $5/R_{SET}$. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where:

$$T_{RAMP} = C \text{ (Ramp Valley to Peak)} \div I_{SET}$$

and:

$$T_{DEADTIME} = C \text{ (Ramp Valley to Peak)} \div (8.4mA - I_{SET})$$

A pulse of a duration shorter than $T_{DEADTIME}$ from an external frequency source set to a higher frequency than f_{OSC} can be applied to pin 10 to synchronize the oscillator. R(SYNC) and C(SYNC) shorten longer pulses.

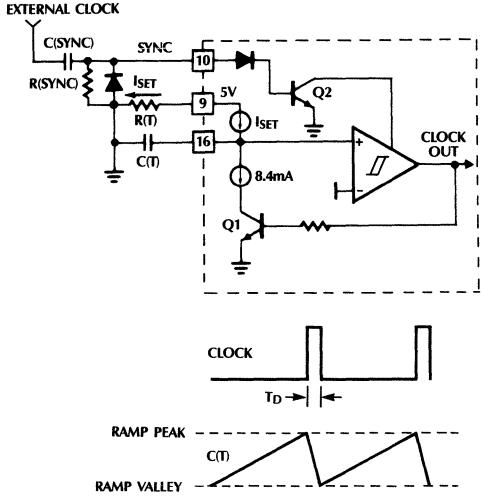


Figure 1. Oscillator Block Diagram

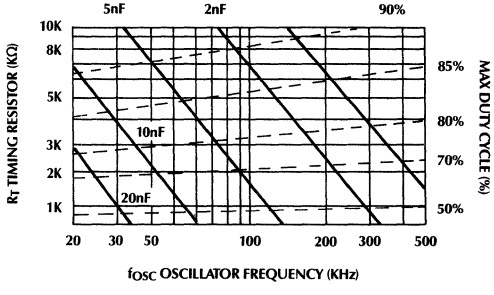


Figure 2. Oscillator Timing Resistance vs. Frequency

OUTPUT DRIVER STAGE

The ML4813 Output Driver is a 1A peak output high speed totem pole circuit designed to quickly drive capacitive loads, such as power MOSFET gates.

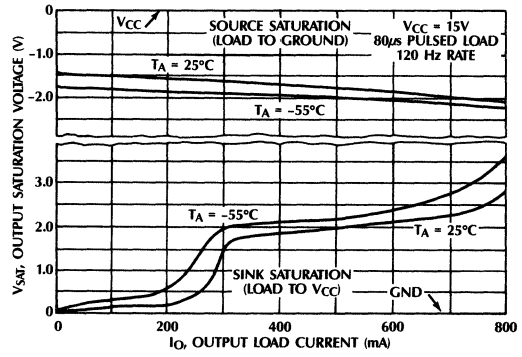


Figure 3. Output Saturation Voltage vs. Output Current

ERROR AMPLIFIER

The ML4813 error amplifier is a high open loop gain, wide bandwidth, amplifier.

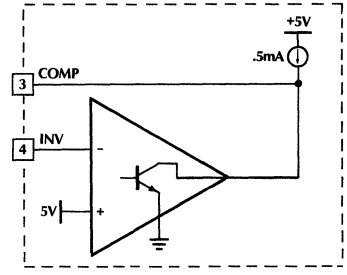


Figure 4. Error Amplifier Configuration

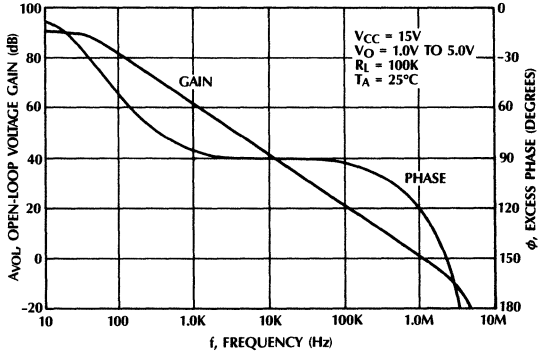


Figure 5. Error Amplifier Open-Loop Gain and Phase vs. Frequency

UN-COMMITTED OP-AMP

The ML4813 contains an un-committed op-amp which is normally configured as a differencing amplifier to sense the output voltage. The output voltage in the flyback configuration is not ground referenced. The op-amp in the ML4813 is a PNP input amplifier similar to the LM324 but with an open emitter output stage (class A).

UNDER VOLTAGE LOCKOUT

On power-up the ML4813 remains in the UVLO condition; output low and quiescent current low. The IC becomes operational when V_{CC} reaches 16V. When V_{CC} drops below 10V, the UVLO condition is imposed. During the UVLO condition, the 5V V_{REF} pin is "off", making it usable as a "flag" for starting up a down-stream PWM converter.

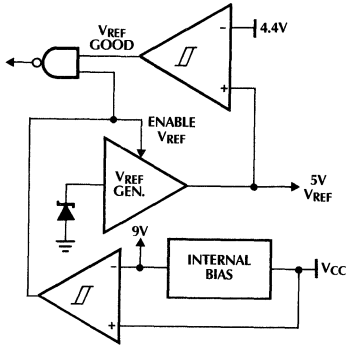


Figure 6. Under-Voltage Lockout Block Diagram

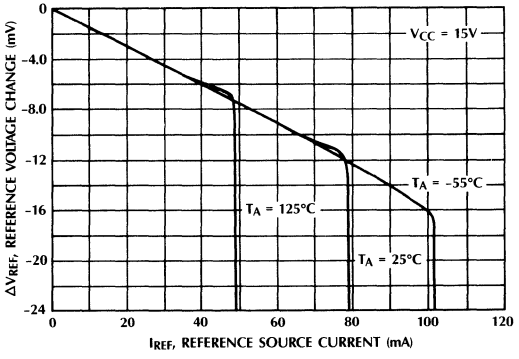


Figure 7. Reference Load Regulation

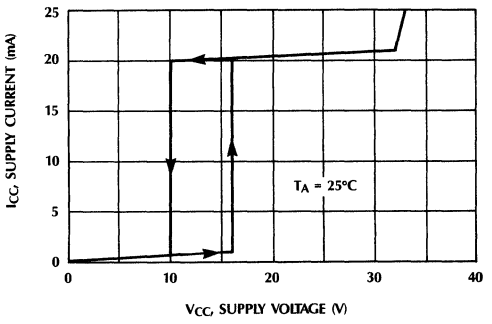


Figure 8. Total Supply Current vs. Supply Voltage

APPLICATIONS

The ML4813 is used to implement a discontinuous mode flyback (buck-boost) power factor regulator. This topology is particularly well suited for low power applications such as: fluorescent ballasts; and low power switching supplies. Also it is a useful topology when there is a requirement for the output voltage to be lower than the peak input voltage, or where an isolated output is required. This is not possible with the boost topology, where the output voltage must always be higher than the maximum peak of the input voltage range. The typical input range for the flyback power factor regulator is from 90 VAC to 260 VAC.

The regulator operates in the discontinuous inductor current conduction mode. The inductor energy stored during the "ON" time of the power switch Q is completely delivered to the output capacitance during the "OFF" time. At steady state conditions, the inductor current at the beginning of the "ON" time starts to ramp-up from 0 Amps to a value that is determined by the instantaneous value of the input full wave rectified voltage; the "ON" time as it is set by the error amplifier and the PWM comparator; and finally by the inductor itself (L).

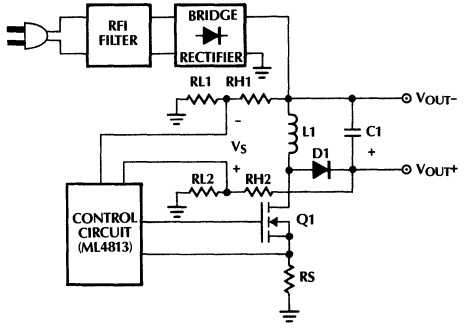


Figure 9. Block Diagram of the Regulator

The expression for the inductor peak current is given by:

$$I_L(\theta) = \frac{V_{IN}(\theta) t_{ON}}{L} \quad (1)$$

Where:

$I_L(\theta)$ = The instantaneous peak inductor current.
t_{ON} = Power switch "on" time.
$V_{IN}(\theta) = V_P \sin \theta$ = Instantaneous Input Voltage.
V_P = Input Peak Voltage.

Figure 10, is a diagram of the relationship between the low frequency envelope and the high frequency inductor current. Note that for clarity the scale between the two waveforms has not been preserved. Normally for 60Hz input line and 100KHz switching frequency, each half of the sine wave contains approximately 833 high frequency triangular waveforms.

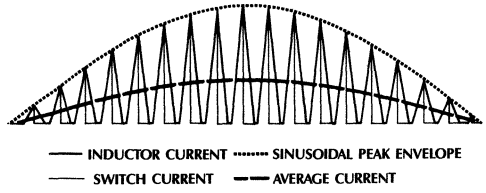


Figure 10. Switch and Line Currents in the Flyback PFC Circuit

The envelope of the peaks of the switch current, which in this case represent the current drawn from the input source, have a sinewave shape. This relationship is shown as:

$$I_L(\theta) = I_P \sin \theta \quad (2)$$

Combining (1) and (2) the following useful relationship is obtained:

$$t_{ON} = \frac{L I_P}{\sqrt{2}\, V_{RMS}} \quad (3)$$

Note that $V_{IN}(\theta) = V_P \sin \theta$, and also $V_P = \sqrt{2}\, V_{RMS}$. The average value of the input triangular current is:

$$I_{AVG}(\theta) = \frac{t_{ON}}{2T} I_P \sin \theta \quad (4)$$

Where:

I_{AVG} = Average value of the switch current. This is the value of the current at the input of the regulator after filtering.
t_{ON} = Switch "on" time.
T = Period of the switch cycle.

Substitution of (3) into (4) yields.

$$I_{AVG}(\theta) = \frac{L I_P^2}{2.828\ T\ V_{RMS}} \sin \theta \quad (5)$$

Equation (5) clearly shows that the average value of the switch current is sinusoidal and in phase with the input voltage. The peak value of the average current is:

$$I_{AVG(PEAK)} = \frac{L I_P^2}{2.828\ T\ V_{RMS}} \sin \theta \quad (6)$$

Also:

$$I_{AVG(PEAK)} = \frac{\sqrt{2}\, P_{IN}}{V_{RMS}} \quad (7)$$

Solving equations (7) and (6) for P_{IN}:

$$P_{IN} = \frac{1}{4} L I_P^2 f \quad (8)$$

For optimum performance and the lowest inductor peak currents, the inductor current should be at the verge of continuity at the lowest operating voltage point and at full load. The above can be satisfied if:

$$I_P \leq \frac{V_{IN}\, V_{OUT}}{f\, L(V_{IN} + V_{OUT})} \quad (9)$$

Where: $V_{IN} = \sqrt{2} \times V_{IN\ MIN\ (RMS)}$

Finally (8) and (9) can be combined to derive an upper bound for the inductor value that will guarantee that the regulator always stays in the discontinuous mode of operation. If the regulator were to operate in the continuous mode the average input current would not be sinusoidal.

$$L \leq \left[\frac{V_{IN}\, V_{OUT}}{2\sqrt{f\, P_{IN}}\, (V_{IN} + V_{OUT})} \right]^2 \quad (10)$$

FLYBACK INDUCTOR CALCULATION

Equation (10) gives the upper bound for the inductor value for any set of specified operating conditions. Normally a few iterations may be required, for finalizing the value. The reason for this is that equation (10) does not contain parameters to correct for second or third order effects. All this means that a good initial value for the inductor is probably 10 to 20% lower than the value calculated by the right hand side expression in (10).

Several core materials are candidates for the inductor, such as: powder iron cores, gapped ferrites, moly permalloy cores, etc. In the application that will be described later, a gapped ferrite core is used.

There are no particular restrictions on the inductor except that the inductance is of correct value and the losses are acceptable.

INPUT BYPASS CAPACITANCE

The triangular high frequency current is bypassed by the input capacitor (C_I) labeled C_7 in Figure 12. This is a high quality film capacitor with low ESR value for minimum losses and heating. A polyester, polypropylene or x-type (for line side) is a good candidate. Typical values, depending on the power level, can range anywhere from 0.33μF to 1.5μF. The

next filtering stage of the RFI filter which has an inductor as input isolates C_7 from the other capacitors which may be present at the input circuit. Note that C_I (C_7) can be on either side of the bridge rectifier. The preferred location for low crossover distortion is at the input side. The voltage ripple across this capacitor is:

$$V_{C(P-P)} = \frac{D}{C_I f}\sqrt{\frac{P_{IN}}{Lf}} - \frac{\sqrt{2}\,P_{IN}}{C_I f\, V_{IN}} \qquad (11)$$

Where:

$V_{C(P-P)}$ = Peak to peak worst case high frequency capacitor voltage.
D = Switch Duty Cycle.

Therefore the RFI filter that follows has to be able to attenuate $V_{C(P-P)}$ to the levels set by the relevant regulatory specifications.

INPUT TRANSIENT OVERVOLTAGE PROTECTION

Careful examination of the power circuits reveals that there is no large capacitance at the input of the regulator. The only capacitances present are the RFI filter capacitors. These capacitors have a combined value in the range of a couple of microfarads. Thus their ability to absorb and minimize any line induced transients is almost non existent. Transients can occur also under sudden load removal. If the line impedance is inductive, hazardous drain source voltages may be generated leading to the destruction of the power switch. To keep this from happening a transient over-voltage protection device should be chosen such that enough safety margin is allowed for the power switch. A good rule of thumb is:

$$B_{VDSS} > V_{ZA} + V_{OUT(OVP)} \qquad (12)$$

Where:

B_{VDSS} = Drain-Source breakdown voltage for the FET.
V_{ZA} = Activation or clamping voltage of the over-voltage transient protector.
$V_{OUT(OVP)}$ = Maximum output voltage. This is set by the OVP function of the controller, and will be covered later.

THE OUTPUT CIRCUIT

The output circuit for this topology, although it is non-isolated, does not share the same ground with the power circuit. Therefore connecting the two grounds with the measuring leads of instruments should be avoided. This is a common mistake especially with the oscilloscope leads.

The output voltage "rides" on the input voltage when the (+) output is measured with respect to PGND (figure 11).

The extra OP-AMP provided in the ML4813 is used to sense the output voltage for regulation and over voltage conditions. This op-amp is connected as a difference amplifier with its output referenced to PGND. Resistors RH1, RH2, RL1, RL2 are used to scale down the voltage.

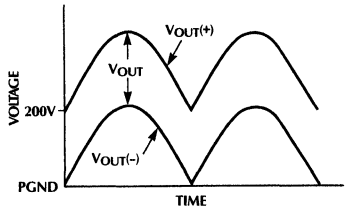


Figure 11. Output Voltage with Respect to PGND

Normally RH1 = RH2 = RH and RL1 = RL2 = RL. Then the voltage designated as V_S in Figure 9 is given by:

$$V_S = V_{OUT}\frac{RL}{RH + RL} \qquad (13)$$

OUTPUT CAPACITANCE

The output capacitance should be calculated such that it has the required output ripple at the worst case operating point. In addition the ESR should be sufficiently low to prevent dissipation due to RMS currents. The first criterion can be met by choosing the value of the output capacitor based on the following:

$$C \geq \frac{P_{IN}}{2\pi f_L\, \Delta V_R\, V_{OUT}} \qquad (14)$$

Where:

C = Total output capacitance.
P_{IN} = Total input power.
ΔV_R = Peak output capacitor ripple voltage.
V_{OUT} = Output Voltage.
f_L = Line Frequency times 2 (120 for 60Hz line).

The second criterion for the selection of the output capacitor can be satisfied by choosing a component with adequately low ESR value, that can safely bypass the RMS currents.

OUTPUT DIODE

The output diode can be a "fast" or ultrafast" type depending on the operating frequency. Reverse recovery losses are low since at steady state and under normal operating conditions the regulator operates in discontinuous current mode. The diode should be rated to handle the output current. The resulting power dissipation will be the forward drop of the diode times the output current.

POWER SWITCH

If a power FET is used, it should be sized for the required efficiency. Lower $R_{DS(ON)}$ devices will yield lower losses, but if they are operated at high frequencies (100KHz) higher charge dumping losses (1/2 $C_{DS}\, V_{DS}^2\, f$) will be experienced. The RMS current value through the power FET and the sensing resistor is:

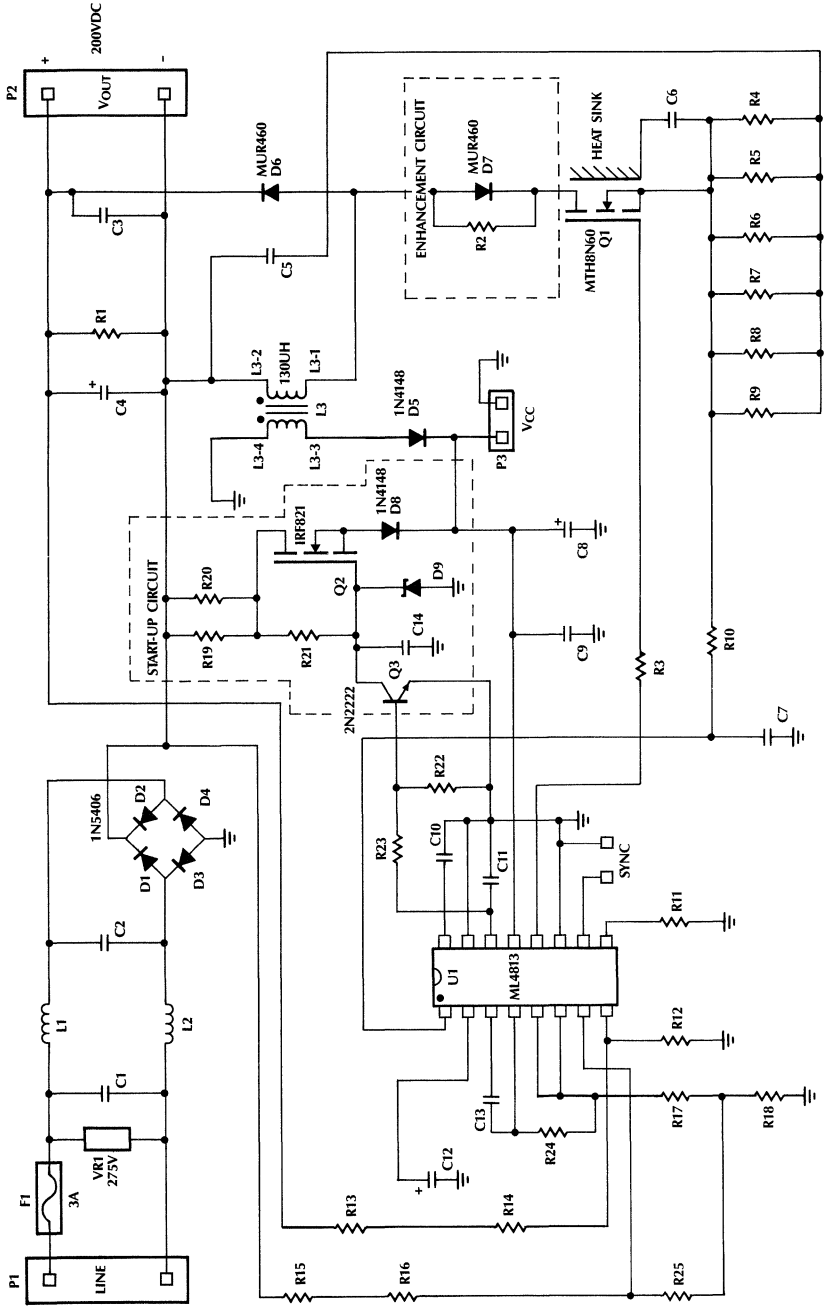


Figure 12. ML4813 Typical Application: 80W Flyback Power Factor Regulator

$$I_{RMS} = \sqrt{\frac{L\ I_P^3\ f_L}{3\sqrt{2}\ V_{RMS}}} \sqrt{\sum_{k=1}^{r} \sin^2 \frac{k\pi}{r}} \qquad (15)$$

Where:

I_{RMS} = Total RMS current through the power FET and sense resistor.
f_L = Line Frequency times 2 (120 for 60Hz line).
$r = f_{SWITCH}/f_L$.

Table 1 is provided to assist in calculating (15) above. When the power switch is a bipolar transistor (constant V_{CE} drop) then the power dissipation produced can be calculated by using (16):

$$P_D = \frac{0.9\ P_{IN}}{V_{RMS}}\ V_{CE} \qquad (16)$$

Where:

P_D = Power dissipation by the transistor (conduction losses).
V_{RMS} = RMS value of the minimum input voltage.
V_{CE} = Collector Emitter forward drop of the power transistor.

OFF-LINE START-UP AND BIAS SUPPLY GENERATION

A fast starting circuit is shown in figure 12. MOSFET Q2 quickly charges the IC's V_{CC} capacitor (C8) when the supply is initially turned on. This allows the supply to come on less than 1 second after AC power is applied. A simpler start-up circuit may be used which replaces the active circuit with a 39KΩ 2W resistor but starts more slowly (up to 15 seconds under low line conditions). Systems which do not require quick starting can reduce cost with the latter start-up method.

f_{SWITCH} (KHz)	r	$\sqrt{\sum_{k=1}^{r} \sin^2 \frac{k\pi}{r}}$
20	167	9.1
30	250	11.2
40	333	12.9
50	417	14.4
60	500	15.8
70	583	17.1
80	667	18.3
90	750	19.4
100	833	20.4
110	917	21.4
120	1000	22.4
130	1083	23.3
140	1167	24.2
150	1250	25.0
160	1333	25.7
170	1417	26.5
180	1500	27.3
190	1583	28.0
200	1667	28.9

Table 1. Figures for Calculating I_{RMS} (eq. 15)

POWER FACTOR ENHANCEMENT

Some combinations of line and load may exhibit distortion of the input current waveform. This distortion is usually caused by the inductor "ringing" with the C_{DS} of the power MOSFET, resulting in a non-zero inductor current at the beginning of the next cycle. This ringing can be dampened by using R2 and D7 in figure 12. Applications which can get by with slightly worse power factor can eliminate these components.

ADJUSTING THE OUTPUT VOLTAGE

The error amplifier creates an error voltage from the difference between the output voltage presented on pin 6 and the 5V internal reference. Since the output voltage is not ground referenced, the ML4813's internal op-amp is connected as an instrumentation amplifier (figure 13).

The output voltage is set by a combination of resistors which determine the relationship between (V_{OUT}+ – V_{OUT}–) and the output of the op-amp (pin 6). For the following discussion, R15' = R15 + R16 and R14' = R14 + R13. The differencing amplifier operation depends on the following relationships:

$$R15' = R14'$$
and
$$R12 = R25 + (R18 \parallel R17)$$

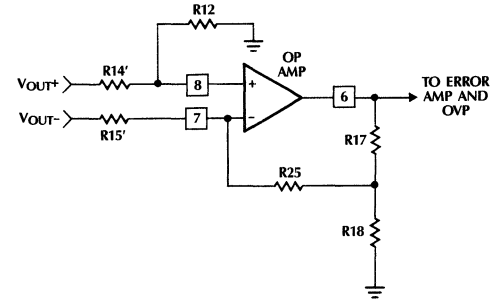


Figure 13. Ground Referencing the Output Voltage

Then:

$$V_{OUT} = \left(\frac{5V \times R18}{R17 + R18}\right)\left(\frac{R15'}{R15' + R25}\right)\left(\frac{R14'}{R12} + 1\right)$$

Since R25 is a low value compared to R15', the second term reduces to approximately 1. The third term is set at approximately 200. Therefore the above equation reduces to:

$$V_{OUT} \cong 1000 \times \left(\frac{R18}{R17 + R18}\right)$$

The over voltage comparator has a threshold that is set for 1.12 × V_{OUT} when pin 5 and pin 6 are connected directly. Figure 14 shows the connection for setting an OVP trip point higher than 1.12 × V_{OUT}, where:

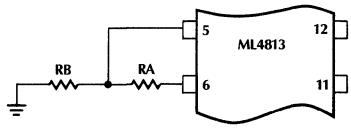


Figure 14. Setting OVP for a $V_{OVP} > 1.12 \times V_{OUT}$

$$V_{OVP} \cong 1.12 \times V_{OUT} \times \left(\frac{RA + RB}{RB} \right)$$

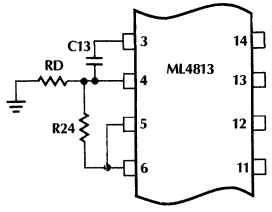


Figure 15. Setting OVP for a $V_{OVP} < 1.12 \times V_{OUT}$

Figure 15 shows OVP set for a voltage lower than 1.12 × V_{OUT} where:

$$V_{OVP} \cong 1.12 \times V_{OUT} \times \left(\frac{RD + R24}{RD} \right)$$

INDUCTOR INFORMATION

L3 is the flyback inductor and also provides the operating power for the control circuitry. A gapped ferrite pot core was chosen for this application for it's modest high frequency losses with high ripple current operation. Some possible choices are:

Manufacturer	Part #	Total Gap	N_P
Magnetics Inc.	F43019	.05"	32
Ferroxcube (Phillips)	3019 PL00-3F3	.05"	32
Ferroxcube (Phillips)	3019 PA125-3C8	.07"	38

The first 2 cores are sold ungapped and require the use of a .025" spacer to gap the center leg to yield a total gap length of .05". If an ungapped core is used, a "shorted turn" should be employed as shown below (figure 16) to prevent radiated EMI. The third core listed is sold with its center leg pre-gapped (.07" total), hence the outside of the core closes completely providing shielding without the shorted turn being required. N_S should be 3 turns. All windings #24AWG wire.

L1 and L2 inductors are constructed using a powdered iron. This is a suitable material for these inductors since the high frequency ripple currents (and resulting flux excursions) are much less severe than for L3. The core selected is:

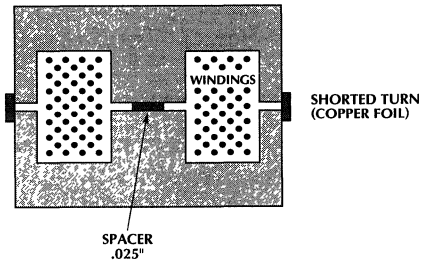


Figure 16. Construction of EMI Shield for Ungapped Cores

Manufacturer	Part #	Turns
MicroMetals	T68-26D	80T #24AWG

COMPONENT	DESCRIPTION
C1, C2	0.68μF, 630V
C3, C5, C6	.01μF, 1KV
C4	330μF, 250V
C7	1000pF, 50V
C8	1000μF, 16V
C9	1μF, 50V
C10	6800pF, 50V
C11, C14	0.1μF, 50V
C12	4.7μF, 50V
C13	0.22μF, 50V
D1 thru D4	1N5406
D5, D8	1N4148
D6, D7	MUR460
D9	22V Zener, 1/4 W
F1	3AG, 3A, 250V
Heat Sink	Thermalloy 6398-U-P3
L1, L2	500μH, 1.5A RMS
L3	160μH, 5A peak
Q1	MTH8N60
Q2	IRF821
Q3	2N2222
R1	220KΩ
R2, R19, R20	4.3KΩ
R3	10Ω
R4 thru R9	1Ω
R10	100Ω
R11	1.8KΩ
R12	4.02KΩ, 1%
R13 thru R16	402KΩ, 1%
R17	806Ω, 1%
R18	200Ω
R21	510KΩ
R22, R23	2KΩ
R24	100KΩ
R25	3.83KΩ, 1%
U1	ML4813CP
VR1	TNR12G431KM

Note: All resistor values 1/4 W ± 5% unless otherwise specified. All capacitor values ±10% unless otherwise specified.

Table 2. Component Values for Figure 8

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4813CP	0°C to +70°C	Molded DIP (P16)
ML4813CS	0°C to +70°C	Molded SOIC (S16W)

Micro Linear

ML4815

Zero Voltage Switching Resonant Controller

GENERAL DESCRIPTION

The ML4815 is designed to facilitate zero-voltage switched (ZVS) resonant converters requiring constant off-time and variable on-time control. Since the power MOSFET is turned on at zero voltage in ZVS resonant converters, power dissipation due to charge-dumping of the MOSFET drain-source capacitance is eliminated, allowing high frequency operation and power density to be maximized. MOSFET parasitic drain-source capacitance can also be used as part of the resonant circuit, minimizing component count.

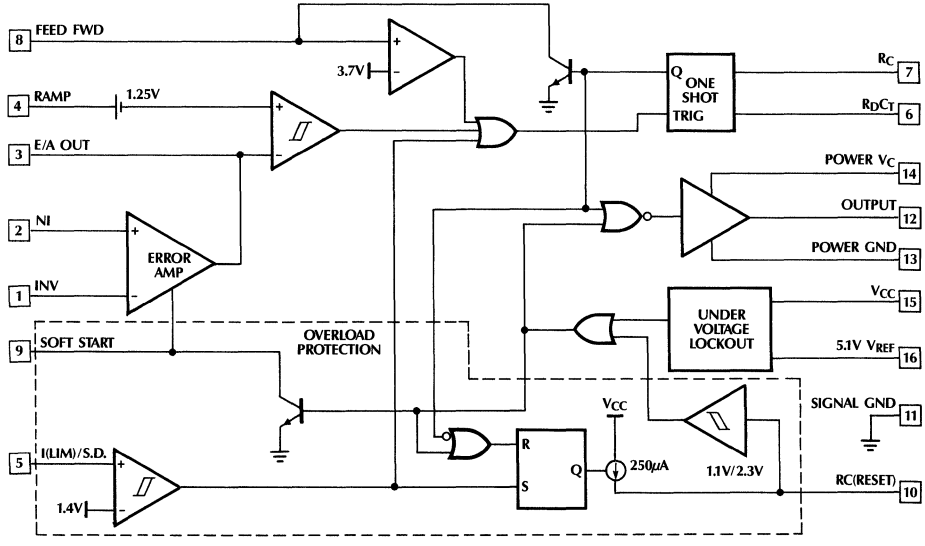
The ML4815 features a monostable multivibrator for precise off-time setting. The on-time is modulated through a ramp comparator in a manner similar to PWM converters. Either current-mode control with maximum on-time clamp or voltage-mode control with input feedforward can be selected.

ML4815 supports pulse-by-pulse (peak) current limiting as well as "hiccup" mode for fault protection. The controller is designed for operation up to 2MHz. ML4815 also includes a wide band error amplifier and a high peak current output driver which minimizes cross-conduction current.

FEATURES

- Supports Single-Switch ZVS Resonant Topology with Minimal External Components
- Ideal for Simple, High Density DC to DC Converters
- Small Converter Frequency Variation from No-Load to Full-Load
- High Current (2A Peak) Totem-Pole Output Drive with Low Cross Conduction
- Precision Buffered 5.1V Reference (±2%)
- Wideband (5.5MHz), High Slew Rate (12V/μS) Error Amp.
- Under-Voltage Lockout with Low Current Start-Up
- Integrating Fault Detection/Soft-Start Reset

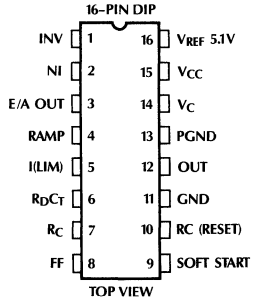
BLOCK DIAGRAM (Pin out shown is for 16-pin DIP)



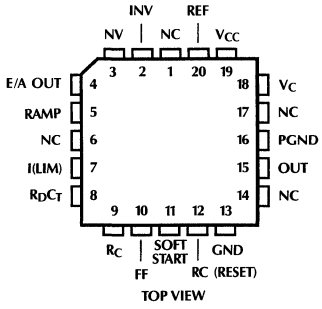
Micro Linear

PIN CONNECTIONS

ML4815
16-Pin DIP



ML4815
20-Pin PCC



PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	INV	Inverting input to error amp.
2	NI	Non-inverting input to error amp.
3	E/A OUT	Output of error amplifier and input to main comparator.
4	RAMP	Non-inverting input to main comparator. Connected to pin 8 for feedforward voltage-mode control or to pin 5 for current-mode control.
5	I(LIM)	Current limit sense pin. Normally connected to current sense resistor.
6	R_DC_T	Off-time setting capacitor and resistor.
7	R_C	Resistor to pin 6 to limit C_T charging rate.
8	FF	Capacitor to generate feedforward ramp.
9	SOFT START	Normally connected to Soft Start Capacitor and charging resistor.
10	RC (RESET)	Timing Capacitor for over-current integration and restart-delay.
11	GND	Analog Signal Ground.
12	OUT	High Current Totem pole output.
13	PGND	Return for the High Current Totem pole output.
14	V_C	Positive Supply for the High Current Totem pole output.
15	V_{CC}	Positive Supply for the IC.
16	5.1V REF	Buffered output for the 5.1V voltage reference.

7

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (Pins 14, 15) 30V
Output Current, Source or Sink (Pin 12)
DC 0.5A
Pulsed (0.5μs) 2A
Analog Inputs (Pins 1, 2, 4, 5, 8, 9, 10) ..... -0.3V to 6V
Error Amplifier Output Current (pin 3) ..... -5mA
Soft Start Sink Current (Pin 9) 100mA
Feedforward Sink Current (Pin 8) 80mA
C_T Charging Current (Pin 7) ..... -50mA

Junction Temperature
ML4815C ..... 125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP ..... 65°C/W
Plastic Chip Carrier (PCC) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range
ML4815C ..... 0°C to 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, these specifications apply for C_T = 330pF, R_C = 100Ω, R_D = 2KΩ, V_{CC} = 15V, T_A = Operating Temperature Range. Pin numbers refer to 16-pin DIP.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1mA	5.00	5.10	5.20	V
Line Regulation	10V < V_{CC} < 30V		2	20	mV
Load Regulation	1mA < I_O < 10mA		5	20	mV
Temperature Stability	-55°C < T_J < 125°C, (note 1)		.2	.4	%
Total Variation	line, load, temp (note 1)	4.95		5.25	V
Output Noise Voltage	10Hz to 10KHz		50		μV
Long Term Stability	T_J = 125°C, 1000 hrs, (note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	-15	-50	-100	mA
Error Amplifier Section					
Input Offset Voltage				20	mV
Input Bias Current			.6	3	μA
Input Offset Current			.1	1	μA
Open Loop Gain	1 < V_O < 4V	60	96		dB
CMRR	1.5 < V_{CM} < 5.5V	75	95		dB
PSRR	12 < V_{CC} < 25V	75	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth	(note 1)	3	5.5		MHz
Slew Rate	(note 1)	6	12		V/μs
RAMP Comparator Section					
Pin 4 Bias Current	$V_{PIN\ 7}$ = 0		-0.7		μA
Pin 3 Zero DC Threshold	$V_{PIN\ 2}$ = 2V, $V_{PIN\ 1}$ = $V_{PIN\ 3}$ $V_{PIN\ 5}$ = 0, $V_{PIN\ 6}$ = 1.5V $V_{PIN\ 8}$ = 2V	1.05	1.20	1.55	V
Delay to Output	C_L = 0, (note 1)		55		ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise noted, these specifications apply for C_T = 330pF, R_C = 100Ω, R_D = 2KΩ, V_{CC} = 15V, T_A = Operating Temperature Range. Pin numbers refer to 16-pin DIP.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit Comparator					
Pin 5 Input Bias Current	$0 < V_{PIN\ 5} < 4V$		2		μA
Current Limit Threshold			1.41		V
Hysteresis			30		mV
Delay to Output	$V_{PIN\ 10}$ = 0, C_L = 0 (note 1)		50		ns
One-Shot Section					
Off-Time Initial Accuracy	C_L = 0, T_A = 25°C		0.45		μs
Off-Time Voltage Stability	C_L = 0, 12V < V_{CC} < 25V		5		%
Off-Time Temperature Stability	C_L = 0 (note 1)		5		%
Off-Time Total Variation	C_L = 0, line, temp (note 1)		6		%
Feedforward/Maximum On-Time Clamp Section					
Discharge Current	$V_{PIN\ 8}$ = 2.5V		30		mA
On-Time Initial Accuracy	C_{FF} = 330pF, R_{FF} = 2.7KΩ to V_{REF}, C_L = 0		1.0		μs
Shutdown/Restart Section					
Pin 10 Charging Current			-250		μA
Overload Shutdown Threshold			2.3		V
Restart Threshold			1.1		V
Soft-Start Section					
Input Bias Current	$V_{PIN\ 9}$ = 4V		1		μA
Discharge Current	$V_{PIN\ 9}$ = 1V		25		mA
Under-Voltage Lockout Section					
Start Threshold			13.4		V
UVLO Hysteresis			3.6		V
Output Section					
Output Low Level	I_{OUT} = 20mA		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2	V
Output High Level	I_{OUT} = -20mA		13.0		V
	I_{OUT} = -200mA		12.7		V
Rise/Fall Time	C_L = 1nF (note 1)		30		ns
Supply Current					
Start Up Current	V_{CC} = 8V, T_J = 25°C V_{CC} = 8V, T_J = -40°C		2.0 2.5	3.0 3.5	mA mA
Operating I_{CC}			28	38	mA

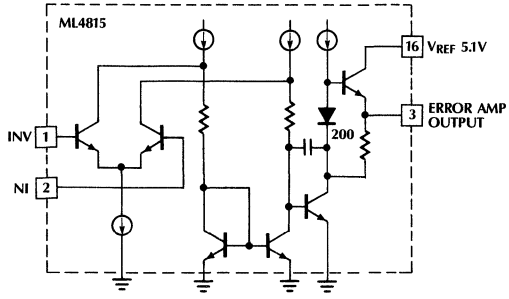
FUNCTIONAL DESCRIPTION

ML4815 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

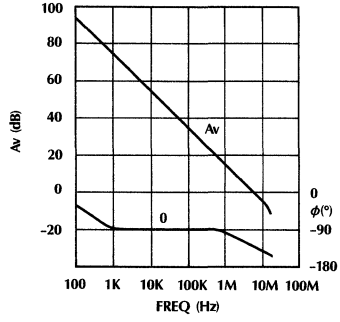
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the ML4815, follow these rules: 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFET. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass V_{CC}, V_C, and V_{REF}. Use 1μF monolithic ceramic capacitors for V_{CC} and V_C with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the off-time setting capacitor, C_T, like a bypass capacitor.

ERROR AMPLIFIER CIRCUIT

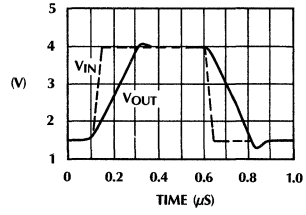
Simplified Schematic



Open-Loop Frequency Response



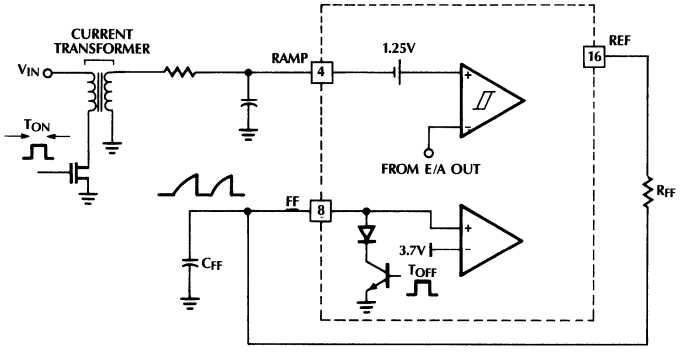
Unity Gain Slew Rate



CONTROL METHODS

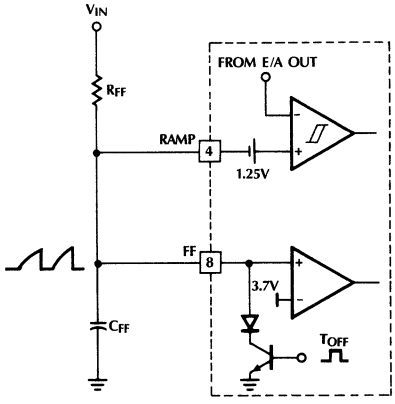
In current-mode control, the current transformer output is fed into the RAMP comparator input. The current-sense waveform is used as the on-time modulating ramp. The on-time can be clamped to a maximum by using R_{FF} and C_{FF} as shown.

Current-Mode Control with Maximum On-Time Clamp



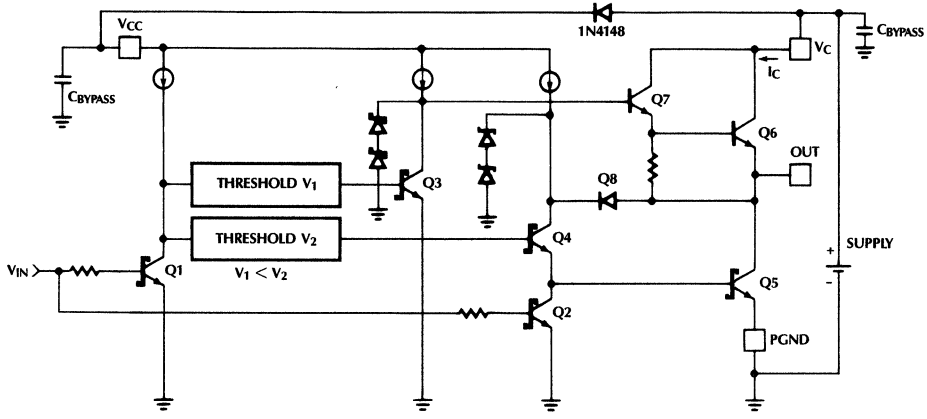
In feedforward voltage-mode control, the on-time modulating ramp is generated with an external capacitor C_{FF} from pin 8 to the ground. C_{FF} is charged through an external resistor R_{FF}. The maximum on-time is the time taken to charge C_{FF} to 3.7V. Since the charging current depends on V_{IN}, the resulting maximum on-time varies with V_{IN}.

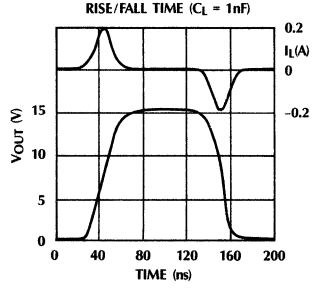
Feedforward Control

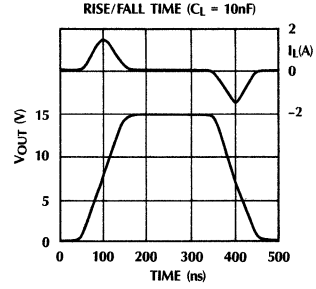


OUTPUT SECTION

Totem-Pole MOSFET Drive with Reduced Cross-Conduction

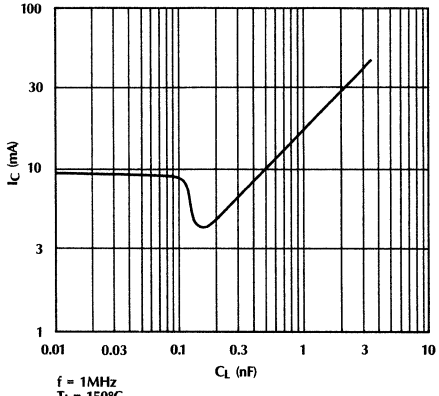






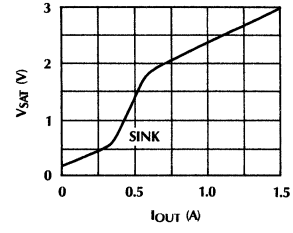
When driving power MOSFET's with high equivalent gate capacitance ($C_G > 3nF$), it is advisable to use an external 1N4148 diode between V_{CC} and V_C pins (figure above) to reduce extra power dissipation caused by slow turn-off of Q_7. In this case both V_{CC} and V_C pins should have bypass capacitors (C = 1μF) as close as possible to the IC pins.

I_C vs C_L

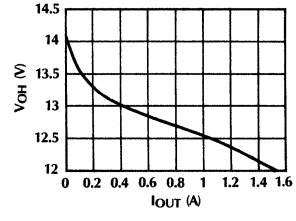


f = 1MHz
T_J = 150°C
I_C = TOTEM-POLE DRIVER CURRENT

V_{OL} Curve



V_{OH} Curve

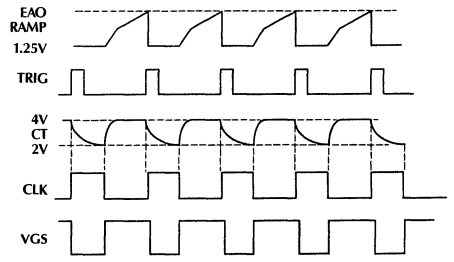


ONE-SHOT

The figure below shows the detailed block diagram of the one-shot. The one-shot is programmed with external resistors R_C, R_D and capacitor C_T. Assuming that CLK is low and Q_2 conducts initially, the timing capacitor C_T is charged to 4V through R_C and Q_3. This corresponds to the switch conduction cycle (on-time). When either the feedforward ramp or the sensed current signal exceeds the error amplifier output voltage, a trigger pulse is sent to the one-shot, setting the R-S latch X_2 and disabling Q_3. C_T is immediately discharged through R_D until C_T voltage reaches the lower threshold (2V) of the Schmitt-trigger X_1. At this point, X_1 output goes high, resetting X_2. Q_1 turns off, allowing Q_3 to recharge C_T to 4V. This time interval corresponds to the switch off-time. Since the off-time is simply the discharge time of C_T, one can express

$$T_{OFF} = 0.69\ R_D C_T$$

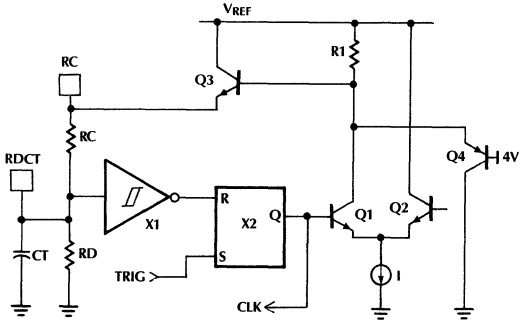
Timing Diagram of the One-Shot



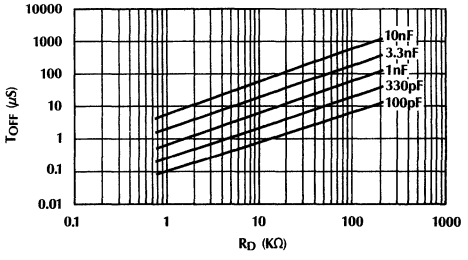
The purpose of R_C is to slow the charging transient of C_T in order to widen the internal reset pulse. R_C is usually chosen such that the following inequality is satisfied.

$$\frac{R_C}{R_C + R_D} < 0.05$$

Block Diagram of the One-Shot



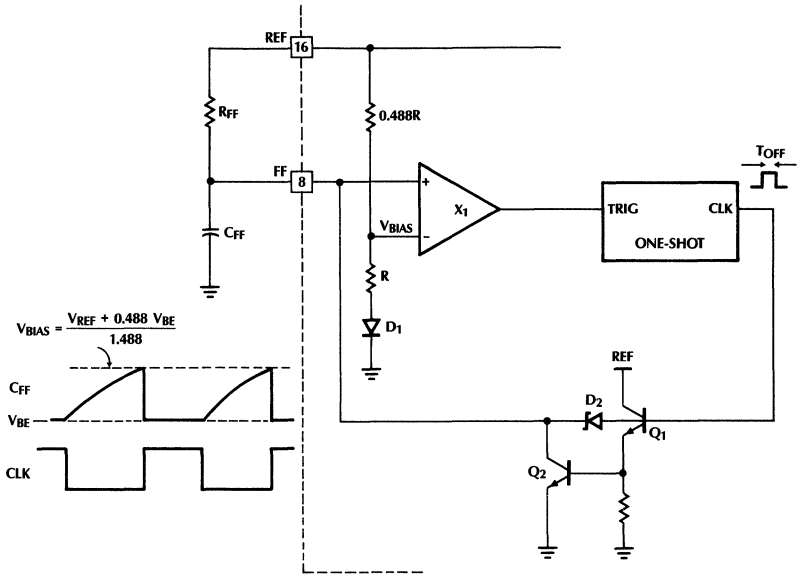
T_{OFF} vs R_D



7

CONSTANT ON-TIME CLAMP (In Current-Mode Only)

Constant On-Time Clamp

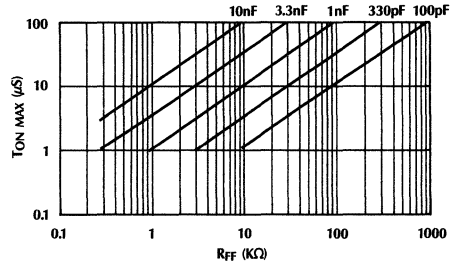


In current-mode control, the maximum on-time can be clamped by using the comparator X_1 (figure above). The internal transistors Q_1, Q_2 and diode D_2 discharges C_{FF} to approximately V_{BE}. The time taken to charge C_{FF} from V_{BE} to V_{BIAS} $\left(= \frac{V_{REF} + 0.488\ V_{BE}}{1.488} \right)$ sets the maximum on-time. The diode D_1 compensates the V_{BE} dependent C_{FF} valley voltage. It can be shown that

$$T_{ON(MAX)} \approx 1.115\ R_{FF}\ C_{FF}$$

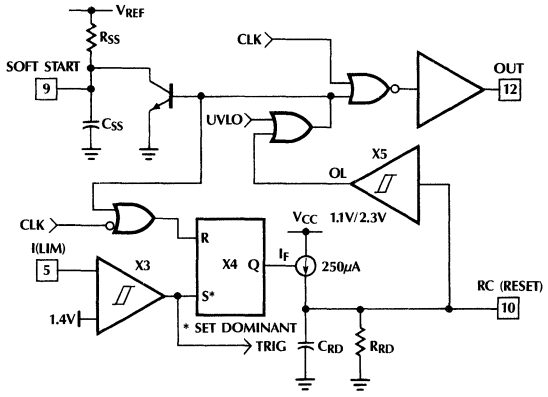
and $T_{ON(MAX)}$ is relatively independent of temperature.

T_{ON} vs R_{FF}



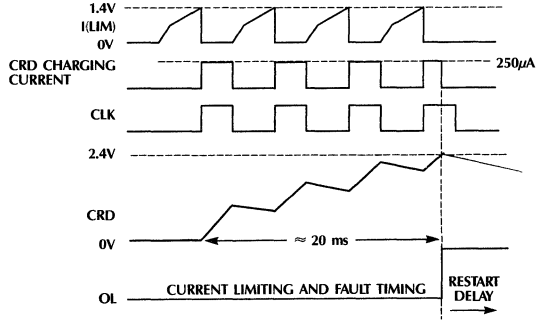
CURRENT-LIMITING, OVERLOAD SHUTDOWN AND FAULT MANAGEMENT

Overload Protection and Fault Management



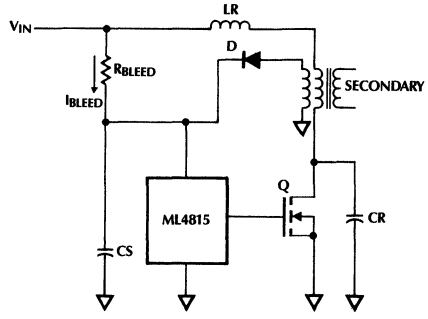
ML4815 features a unique overload protection scheme. The power transistor current is compared with the current-limit threshold (1.4V) of X_3. When the sensed current exceeds this threshold, the one-shot is triggered and the R-S latch X_4 is set. The one-shot blanks the gate drive and X_4 turns on the current source I_F. The external capacitor C_{RD}, which is normally fully discharged, is charged towards an overload threshold of 2.3V. The packet of charge delivered to C_{RD} in each over-current cycle is $I_F \times T_{OFF}$ (figure below). X_4 is reset after the off-time elapses. If output short is removed before C_{RD} reaches the overload threshold, C_{RD} will be discharged through R_{RD} and normal operation will resume. Under persistent output short circuit, C_{RD} is charged until it reaches 2.3V. The gate drive is immediately terminated and the soft-start capacitor is discharged. C_{RD} then discharges through R_{RD} towards the restart threshold (1.1V). Gate drive remains off until C_{RD} is discharged below 1.1V. The time taken for C_{RD} to discharge to the restart threshold is the restart-delay time. This delay reduces the average power delivered to the load during overload, thus protecting both the load and the controller. If overload persists, the controller will continue to hiccup until the cause of overload is removed. The controller undergoes soft-start at each restart. The overload shutdown and restart sequence for a converter with non-bootstrapped power supply V_{CC} is illustrated in figure.

Current Limiting Overload Shutdown and Restart Sequence (Non-Bootstrapped Operation)



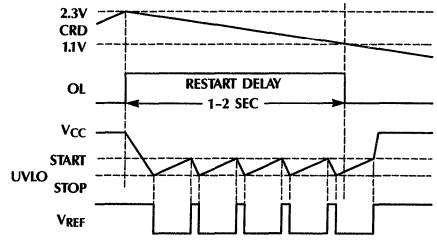
For a bootstrapped converter (where controller V_{CC} is obtained from an auxiliary winding of the main transformer), overload shutdown causes both the converter output and the controller V_{CC} to collapse. Undervoltage lockout (UVLO) is activated and the on-chip bandgap reference is disabled. ML4815 dissipates only 2mA of supply current during shutdown. Since

Simplified V_{CC} Bootstrapping Scheme

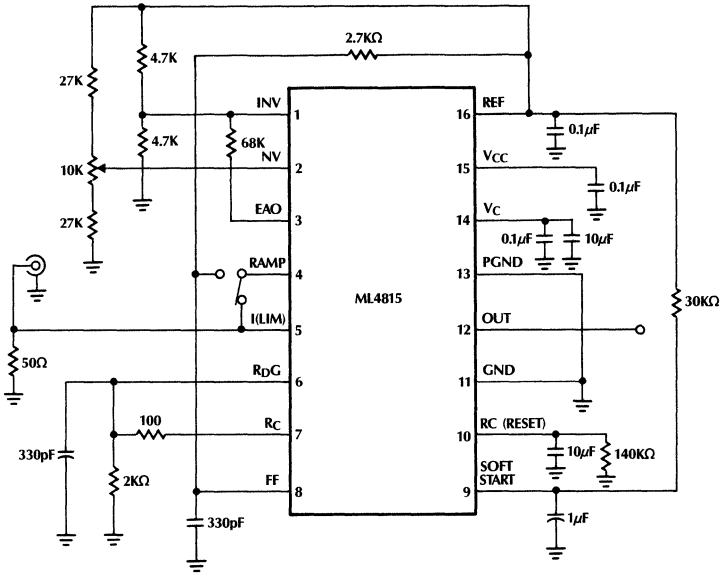


I_{BLEED} is higher than the start-up current, C_S will be charged towards the UVLO start threshold. When this happens, the entire controller becomes operational except that the gate drive remains off. I_{CC} jumps to its full operational value. Since V_{CC} bootstrapping is not yet available, I_{CC} will discharge C_S below the UVLO stop threshold. The on-chip reference will again be disabled with the controller supply current reduced to 2mA. I_{BLEED} will again charge C_S towards the UVLO start threshold. The process repeats until C_{RD} is discharged below the restart threshold. The shutdown and restart sequence is illustrated with the timing diagram below.

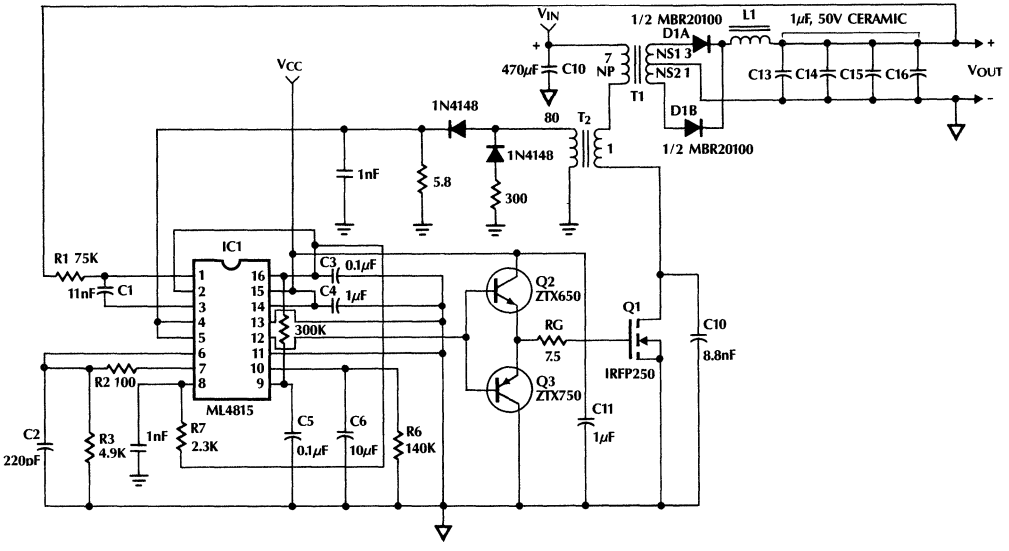
Overload Shutdown UVLO and Restart Sequence (Bootstrapped Operation)



OPEN LOOP LABORATORY TEST FIXTURE



SCHEMATIC OF THE 50W ZVS DC/DC CONVERTER



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4815CP	0°C to +70°C	Molded DIP (P16)
ML4815CQ	0°C to +70°C	Molded PCC (Q20)

Micro Linear

ML4816

High Frequency Multi-Mode Resonant Controller

GENERAL DESCRIPTION

The ML4816 controller IC is suitable for a wide range of resonant converter topologies. This controller can be used with Zero Current Switched (ZCS) Quasi Resonant Converters (QRC) requiring constant on-time and modulated off-time, as well as frequency modulated converters such as Series Resonant Converters operating above resonance.

The ML4816's oscillator features independent control of charging and discharging currents (on-time and off-time). Output frequency can be obtained either proportional or inversely proportional to the controlling voltage. In addition, both upper and lower frequency limits (f_{MIN} and f_{MAX}) can be independently set.

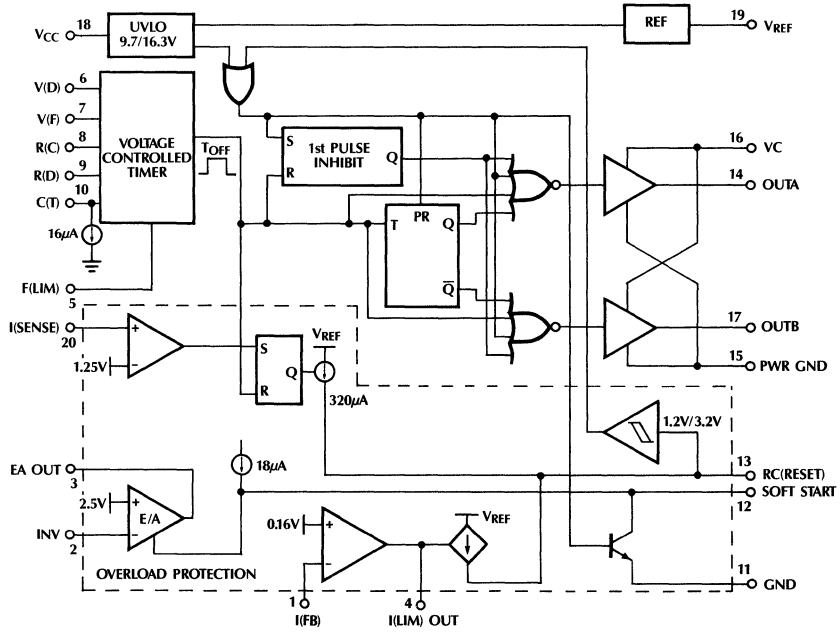
Both pulse-by-pulse and DC current limiting are provided for. Overload protection (shutdown) is triggered after a programmable delay time. Restart after overload shutdown can be delayed by a programmable time. Internal logic disables the gate drive until the oscillator is stable.

The ML4816 includes under-voltage lockout with 6V hysteresis and high current high speed totem pole output drivers for high speed drive of external MOSFETs.

FEATURES

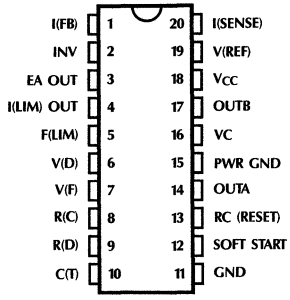
- Supports Zero Current Switched (ZCS) Quasi-Resonant Converters
- Supports Series Resonant (ZVS) converters operating above resonance
- Wide oscillator frequency range
- Programmable f_{MIN} and f_{MAX} limits
- Practical Operation to 2.5MHz (f_{OSC})
- Low Start-up Current and Under-Voltage Lockout Circuits support Off-Line Operation
- Pulse by Pulse or DC Current Limiting
- Integrating Soft Start Reset (Fault Integration) with Programmable Restart Delay
- High current (1.5A peak) totem-pole output drive
- Precision buffered 5V Reference (±1%)

BLOCK DIAGRAM



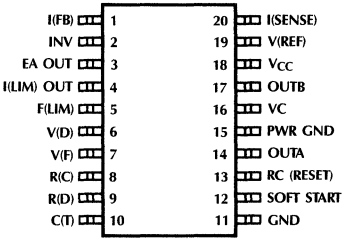
PIN CONFIGURATION

ML4816
20-Pin DIP



TOP VIEW

ML4816
20-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	I(FB)	Input for load current limit.
2	INV	Inverting input to error amp.
3	EA OUT	Output of error amplifier.
4	I(LIM) OUT	Output for load current limit amplifier.
5	F(LIM)	A voltage input sets the maximum on time for the timer.
6	V(D)	Controls the C(T) discharge current and oscillator off time. Connected to error amplifier output for off-time modulation and to V(REF) for constant off time.
7	V(F)	Controls the charging current and oscillator on time. Connected to error amplifier for on time modulation and connected to GND for constant on time.
8	R(C)	External timing resistor to either GND or V(REF) sets the charging current (oscillator on time). This pin can either source or sink current.
9	R(D)	External resistor from this pin to GND sets the oscillator discharge current (off time).
10	C(T)	Timing capacitor for Oscillator.
11	GND	Signal ground.
12	SOFT START	Normally connected to Soft Start capacitor.
13	RC(RESET)	Timing elements for Integrating fault detection and reset delay circuits.
14	OUTA	High Current Totem pole output A.
15	PWR GND	Return for the High Current Totem Pole outputs.
16	VC	Supply for the High Current Totem Pole outputs.
17	OUTB	High Current Totem pole output B.
18	V_{CC}	Positive supply for the IC.
19	V(REF)	Buffered output for the 5.0V voltage reference.
20	I(SENSE)	Primary current sense input for current limit.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (Pins 16, 18) 30V
Output Current, Source or Sink (Pin 12)
DC 0.5A
Pulse (0.5µs) 1.5A
Analog Inputs
(Pins 1, 2, 5, 6, 7, 13) ..... –0.3 to 6.3V
Amplifier Output Currents (Pins 3, 4) 5mA
Soft Start Sink Current (Pin 8) 100mA
R_C Current (Pin 8) ..... –0.5 to +0.5mA
R_D Current (Pin 9) ..... –4mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP or SOIC ..... 65°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, C_T = 470pF, V_{CC} = 15V. V_{CC} is adjusted above the start threshold before settling at 15V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_A = 25°C, I_O = –1mA	4.90	5.00	5.10	V
Line Regulation	12V ≤ V_{CC} ≤ 25V		2	20	mV
Load Regulation	1mA ≤ I_O ≤ 10mA		5	20	mV
Temperature Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (Note 1)		0.2	0.4	mV/°C
Total Variation	line, load, temp.	4.85		5.15	V
Output Noise Voltage	10Hz < f < 10KHz		50		µV
Long Term Stability	T_J = 125°C, 1000 Hrs (Note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0	–40	–70	–100	mA
Error Amplifier Section					
Non-Inverting Input Voltage		2.37	2.47	2.57	V
Input Bias Current				3	µA
Open-Loop Gain	1 ≤ V_O ≤ 4V	60			dB
Unity Gain Bandwidth	(Note 1)	2.5	2.8		MHz
PSRR	12V ≤ V_{CC} ≤ 25V	65			dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7V, $V_{PIN\ 3}$ = 1V	1	2.8		mA
Output Source Current	$V_{PIN\ 2}$ = 2.3V, $V_{PIN\ 3}$ = 4V	–0.5	–2.2		mA
Output High Voltage	$I_{PIN\ 3}$ = –0.5mA	5.0	5.5	6.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA		0.5	1.0	V
Slew Rate			8.5		V/µs
Current-Limit Amplifier Section					
Non-Inverting Input Voltage		0.145	0.17	0.2	V
Input Bias Current				3	µA
Open-Loop Gain	1 ≤ V_O ≤ 4V	65			dB
Unity Gain Bandwidth	(Note 1)	1.0	1.5		MHz
PSRR	12V ≤ V_{CC} ≤ 25V	55			dB
Output Sink Current	$V_{PIN\ 1}$ = 1V, $V_{PIN\ 4}$ = 1V	1	1.6		mA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Amplifier Section (Continued)						
Output Source Current		$V_{PIN\ 1}$ = 0V, $V_{PIN\ 4}$ = 4V	–0.5	–1.1		mA
Output High Voltage		$I_{PIN\ 4}$ = –0.5mA	6.0	7.2	8.0	V
Output Low Voltage		$I_{PIN\ 4}$ = 1mA		0.7	1.0	V
Slew Rate		(Note 1)		0.9		V/µs
Current-Sense Section						
Input Bias Current		$V_{PIN\ 20}$ = 0			–2	µA
Current-Sense Threshold			1.20	1.25	1.30	V
Delay to Pin 13		(Note 1)		80	150	ns
Soft-Start Section						
Discharging Current		$V_{PIN\ 13}$ = 4V, $V_{PIN\ 12}$ = 1V	20	35		mA
Charging Current		$V_{PIN\ 13}$ = 0, $V_{PIN\ 12}$ = 1V	–16	–21	–26	µA
Overload Protection Section						
Overload Threshold			3.0	3.2	3.5	V
Restart Threshold			1.0	1.2	1.4	V
Pulse-by-pulse Charging Current		$V_{PIN\ 20}$ = 1.35V, $V_{PIN\ 13}$ = 2V		–320		µA
Current-Limit Amp. Controlled Current		$V_{PIN\ 1}$ = 0, $V_{PIN\ 13}$ = 2V $V_{PIN\ 4}$ = 1V $V_{PIN\ 4}$ = 2.5V		 –2.2 –0.9		 mA mA
Voltage-Controlled Timer						
C_T Minimum Discharging Current		$V_{PIN\ 6}$ = 0, $V_{PIN\ 10}$ = 3V	14	18.5	22	µA
C_T Peak Voltage				3.75		V
C_T Valley Voltage				2.1		V
R_C Minimum Voltage		$V_{PIN\ 5}$ = $V_{PIN\ 7}$ = 0, 25KΩ from Pin 8 to GND	0.446V_{REF}	0.455V_{REF}	0.464V_{REF}	V
R_C Voltage		$V_{PIN\ 5}$ = 8 ÷ 11 V_{REF}, $V_{PIN\ 7}$ = 5V 25KΩ from Pin 8 to GND	0.713V_{REF}	0.72V_{REF}	0.742V_{REF}	V
R_D Minimum Voltage		$V_{PIN\ 6}$ = 0, 3KΩ from Pin 9 to GND			0	V
R_D Maximum Voltage		$V_{PIN\ 6}$ = 5V, 3KΩ from Pin 9 to GND	0.425V_{REF}	0.45V_{REF}	0.475V_{REF}	V
T_{ON}	T_A = 25°C	$V_{PIN\ 5}$ = $V_{PIN\ 7}$ = 0, $V_{PIN\ 6}$ = 3V, 25KΩ from Pin 8 to GND, 3KΩ from Pin 9 to GND	0.62	0.68	0.75	µs
	Total Variation	12V ≤ V_{CC} ≤ 25V (Note 1) T_{MIN} ≤ T_A ≤ T_{MAX}	0.60	0.71	0.79	µs
Output Dead Time	T_A = 25°C (Note 1)	$V_{PIN\ 5}$ = $V_{PIN\ 7}$ = 0, $V_{PIN\ 6}$ = 5V 25KΩ from Pin 8 to GND, 3KΩ from Pin 9 to GND	100	120	145	ns
	Total Variation	12V ≤ V_{CC} ≤ 25V (Note 1) T_{MIN} ≤ T_A ≤ T_{MAX}	100	120	155	ns

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Voltage-Controlled Timer (Continued)						
Frequency	$f_{MAX(1)}$	$V_{PIN\ 5} = V_{PIN\ 7} = 0$, $V_{PIN\ 6} = 5V$ 25KΩ from Pin 8 to GND 3KΩ from Pin 9 to GND	1.0	1.2	1.4	MHz
	$f_{MIN(1)}$	$V_{PIN\ 5} = V_{PIN\ 7} = 0$, $V_{PIN\ 6} = 1.4V$ 25KΩ from Pin 8 to GND 3KΩ from Pin 9 to GND	17	22	28	KHz
	$f_{MAX(2)}$	$V_{PIN\ 5} = 8 \div 11\ V_{REF}$, $V_{PIN\ 7} = 2V$ $V_{PIN\ 6} = 5V$ 22KΩ from Pin 8 to Pin 19 3KΩ from Pin 9 to GND	1.1	1.33	1.55	MHz
	$f_{MIN(2)}$	$V_{PIN\ 5} = 8 \div 11\ V_{REF}$, $V_{PIN\ 7} = 2V$ $V_{PIN\ 6} = 5V$ 22KΩ from Pin 8 to Pin 19 3KΩ from Pin 9 to GND	650	800	850	KHz
Under Voltage Lockout Section						
Start Threshold			15.0	16.3	16.8	V
Stop Threshold			9.2	9.7	10.2	V
Supply Current						
Start-Up Current		$V_{CC} = 15.5V$	1.2	1.75	2.3	mA
Operating Supply Current		$V_{PIN\ 5} = V_{PIN\ 7} = 0$, $V_{PIN\ 6} = 5V$ 25KΩ from Pin 8 to GND 3KΩ from Pin 9 to GND $C_{LA} = C_{LB} = 0$, $T_A = 25°C$,	26	32	38	mA
		$T_{MIN} \le T_A \le T_{MAX}$			53	mA
Output Section						
Output Low Level		$I_{SINK} = 20mA$		0.1	0.4	V
		$I_{SINK} = 200mA$		0.7	2.2	V
Output High Level		$I_{SOURCE} = 20mA$	12.0	13.5		V
		$I_{SOURCE} = 200mA$	11.5	13.0		V
Rise Time		$C_{LA} = C_{LB} = 1nF$ (Note 1)			60	ns
Fall Time		$C_{LA} = C_{LB} = 1nF$ (Note 1)			60	ns

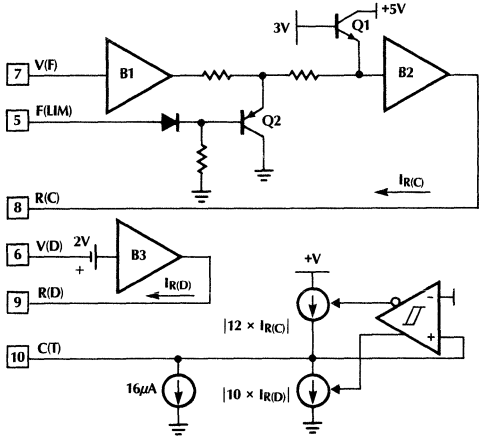
Note 1: This parameter is not 100% tested in production but guaranteed by design.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The oscillator is the core of the ML4816 and is designed to allow the maximum flexibility. This oscillator can be used in two basic modes of operation:

1. On time proportional to V_{IN}, fixed off time with a maximum on time limit (where V_{IN} is the output of the error amplifier).
2. Off time inversely proportional to V_{IN}, fixed on time.



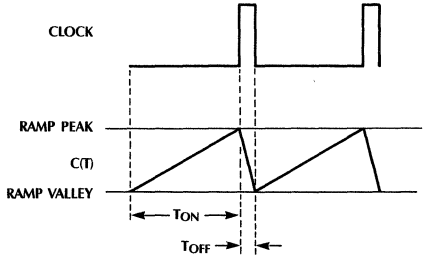


Figure 1. Oscillator Block Diagram

The internal CLOCK signal, shown above, turns the outputs off at its rising edge. Clock remains high and the outputs stay off as long as C(T) is discharging. The discharge time (T_{OFF}) of C(T) is:

$$T_{OFF} = \frac{1.65\ C(T)\ R(D)}{10\ (V(D) - 2V) + 16\mu A\ R(D)} \quad (1)$$

Variable Off-Time, Constant On-Time (Figure 2)

When using a variable off time control, V(D) is tied to the output of the error amplifier. Off time is given by equation (1) while the 16μA current sink prevents the off time from becoming infinite, thereby providing an upper limit to T_{OFF} of:

$$\text{Max } (T_{OFF}) = C(T) \times 1.03 \times 10^5 \quad (2)$$

The on time is given by:

$$T_{ON} = 0.0605\ R(C)\ C(T) \quad (3)$$

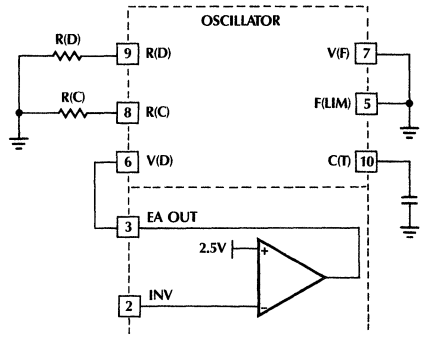


Figure 2. Variable Off Time, Constant On Time Oscillator Connections

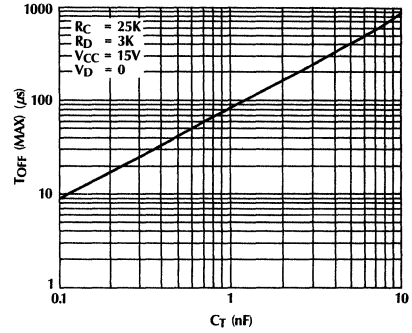


Figure 2a. Max (T_{OFF}) vs. C_T

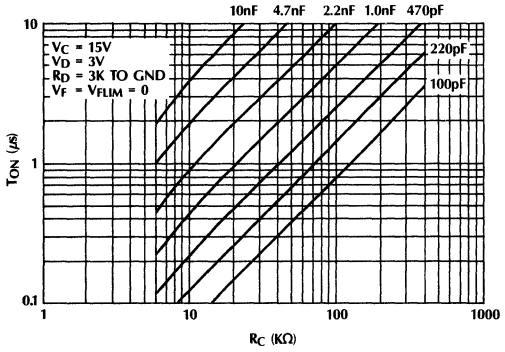


Figure 2b. T_{ON} vs. R(C)

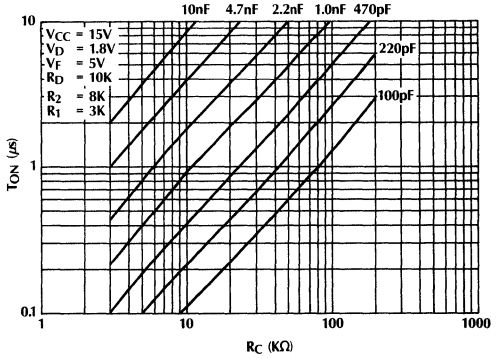


Figure 3a. Minimum T_{ON} for Constant Off-Time Configuration with $V_{FLIM} = \frac{8}{11} \times V_{REF}$

Variable On-Time, Constant Off-Time

The on time (T_{ON}) is controlled by the current flowing from V(REF) through R(C) into B2. The output of B2 is internally limited to be no less than 2.27V and no greater than F(LIM).

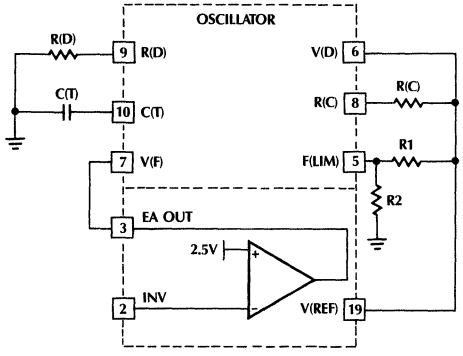


Figure 3. Variable On Time, Constant Off Time Oscillator Connections (T_{ON} Proportional to EA OUT)

The on time for figure 3 is given by:

$$T_{ON} = \frac{0.138\ R(C)\ C(T)}{V(REF) - V(F)} \quad (4)$$

The maximum on time is given by:

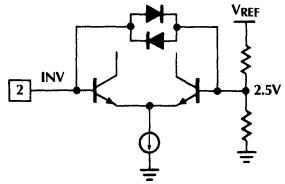
$$T_{ON(MAX)} = \frac{0.138\ R(C)\ C(T)}{V(REF) - F(LIM)} \quad (5)$$

where F(LIM) > 2.27V. The minimum on time is:

$$T_{ON(MIN)} = 0.0506\ R(C)\ C(T) \quad (6)$$

ERROR AMPLIFIER

The ML4816 error amplifier is a 2.5MHz bandwidth, 8.5V/µsec slew rate op-amp with provision for limiting the positive output voltage swing to implement the soft start function.



The Error Amplifier input contains protection diodes as shown above. INV should not be driven lower than 2.5V – V_{BE} or higher than 2.5V + V_{BE}.

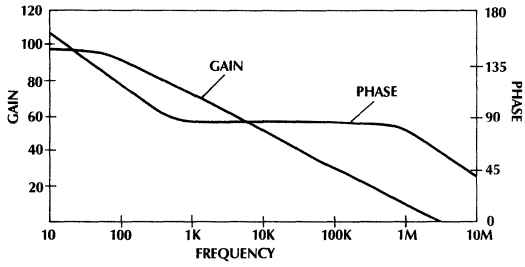


Figure 5. Error Amplifier Open-Loop Gain and Phase vs. Frequency

OUTPUT DRIVER STAGE

The ML4816 has two high current high speed totem pole output drivers each capable of 1.5A peak output, designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors.

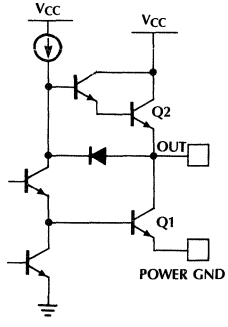


Figure 6. Power Driver Simplified Schematic

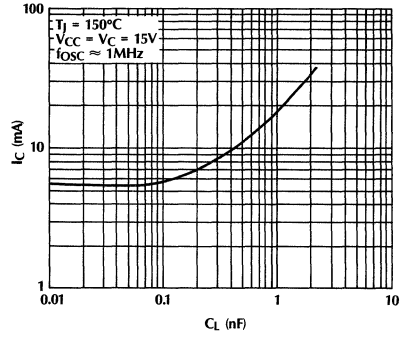


Figure 6a. Output Driver Current Consumption I(C) vs. Output Load Capacitance

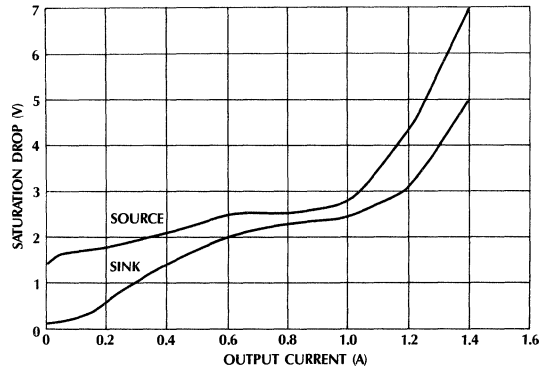


Figure 7. Output Saturation Voltage vs. Output Current

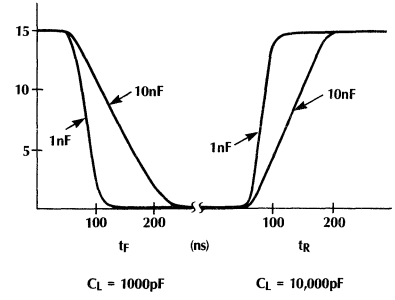


Figure 8. Rise/Fall Time

CURRENT LIMIT, FAULT DETECTION AND SOFT START

The ML4816 has two modes of current limiting: Primary pulse-by-pulse over-current protection and secondary DC average current limiting.

Primary Pulse-by-Pulse Current Limit Circuit

In this mode, the primary current is compared with a 1.25V threshold in comparator X1. When the sensed current exceeds the 1.25V threshold of comparator X1, the R-S latch X2 is set, turning on the 320μA current source to charge C_{RST}. I_{F1} remains on until CLOCK goes high (T_{OFF}). When C_{RST} has charged to 3.2V, a soft start reset occurs. The number of times the outputs reach current limit are "remembered" on C_{RST}. Over time, C_{RST} is discharged by R_{RST} providing a measure of "forgetting" when the over-current condition no longer occurs. If the output fault is removed before C_{RST} reaches 3.2V, C_{RST} discharges slowly through R_{RST} and normal operation resumes.

Over-Current Sensing, Overload Shutdown and Fault Management

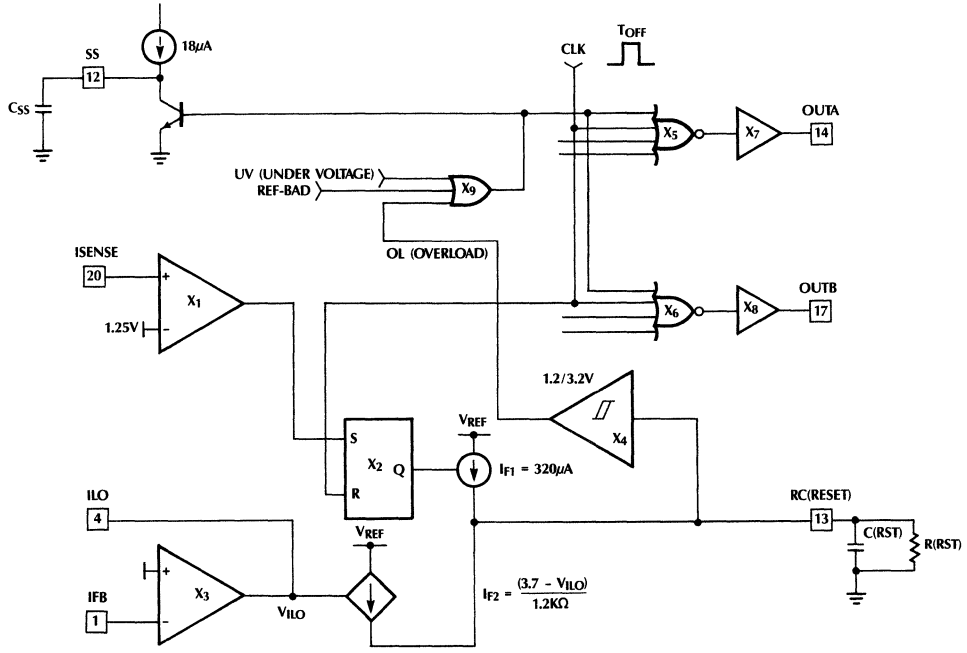


Figure 9. Overload Protection and Fault Management

Secondary dc Current Limit Circuit

In secondary dc current-limiting, the currents in the output rectifiers are sensed, full-wave rectified and smoothed. The smoothed signal is fed into the current-limiting amplifier X_3. If the sensed current is below the 0.16V threshold, the output of X_3 will go above V_{REF} and I_{F2} will be off. As the sensed current exceeds the current-limit threshold, V_{ILO} starts to fall and

I_{F2} ($\approx \frac{V_{REF} - V_{ILO} - 2V_{BE}}{1200\Omega}$) turns on. I_{F2} charges C_{RST} towards the overload threshold (3.2V) of X_4. C_{RST} charging and temporary recovery through R_{RST} here are similar to the pulse-by-pulse over-current sensing case except that I_{F2} is continuous.

Under persistent output short circuit with either form of over-current protection, C_{RST} is charged until it reaches 3.2V. The gate drives are immediately terminated and the soft-start capacitor C_{SS} is discharged. C_{RST} then discharges through R_{RST} toward the restart threshold (1.2V). Gate drives remain off until C_{RST} is discharged below 1.2V. The time taken for C_{RST} to discharge to the restart threshold is the restart-delay time. This delay reduces the average power delivered to the load during overload, thus protecting both the load and the controller. If overload persists, the controller will continue to hiccup until the cause of overload is removed. The controller undergoes soft-start at each restart.

The overload shutdown and restart sequences for both over-current protection schemes with non-bootstrapped V_{CC} are illustrated in Figures 10 and 11.

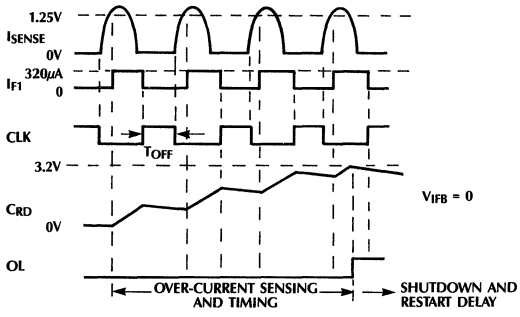


Figure 10. Over-Current Sensing, Overload Shutdown and Restart Sequence (Non-Bootstrapped V_{CC}) (ZCS-QRC Transistor Current Shown)

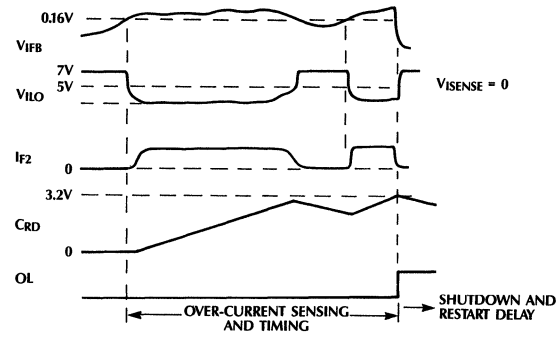


Figure 11. Secondary dc Current Sensing, Overload Shutdown and Restart Sequence (Non-Bootstrapped V_{CC})

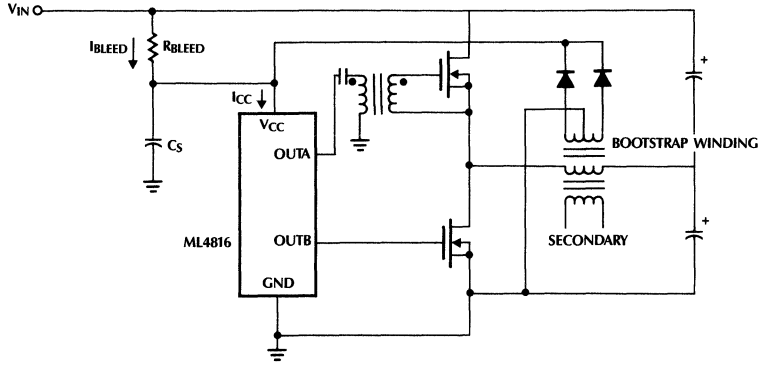


Figure 12. Simplified V_{CC} Bootstrapping Scheme in Half-Bridge Configuration

For a bootstrapped converter, where controller V_{CC} is obtained from an auxiliary winding of the main transformer, (see Figure 12) overload shutdown causes both the converter output and the controller V_{CC} to collapse. Undervoltage lockout (UVLO) is activated and the on-chip bandgap reference is disabled. ML4816 dissipates only 1.5mA during shutdown. Since I_{BLEED} is higher than the start-up current, C_S will be charged towards the UVLO start threshold. When this happens, the entire controller becomes operational except that the gate drives remain off. I_{CC} jumps to its full operational value. Since V_{CC} bootstrapping is not yet available, I_{CC} will discharge C_S below the UVLO stop threshold. The on-chip reference will again be disabled with the controller supply current reduced to 1.5mA. I_{BLEED} will again charge C_S towards the UVLO start threshold. The process repeats until C_{RST} is discharged below the restart threshold. The shutdown and restart sequence is illustrated in Figure 13.

The over-current timing and shutdown sequence can be disabled by grounding pin 13.

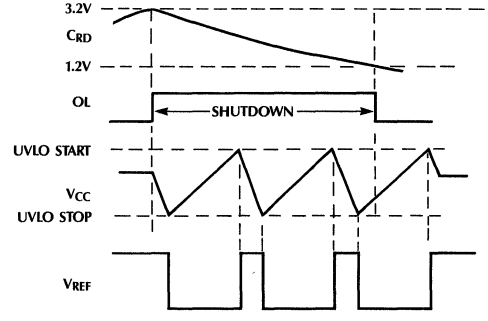


Figure 13. Overload Shutdown, UVLO and Restart Sequence (Bootstrapped Operation)

Auxiliary Output Current-Limiting (RC(RESET) Pin Grounded)

Constant current at power inverter output can be obtained by utilizing the current-limit amplifier with pin 13 shorted to ground. The ILO pin is connected to the EAO pin through two external OR-ing diodes D_1 and D_2 (Figure 14). R_1 is used as a pull-up resistor. The current-limiting loop activates and takes control if the voltage at the inverting input IFB of the current-limit amplifier exceeds the 160mV threshold and ILO is pulled below EAO. The schematic shows that either the main error amplifier or the current-limiting amplifier controls the switching frequency of the converter. The voltage to the IFB pin comes from the output of a current sensor which produces a signal proportional to the output current.

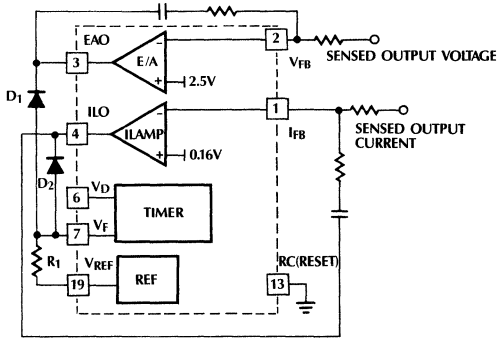


Figure 14. Auxiliary Output Current-Limiting

First-Pulse Inhibit

ML4816 features a unique scheme to prevent input transformer from saturating during initial start-up. Before V_{CC} rises above the undervoltage lockout (UVLO) start threshold, the bandgap reference is disabled. Since the bias circuit of the timer requires a reference output of at least $4V_{BE}$ to operate, the timing capacitor C_T remains fully discharged. As V_{CC} crosses UVLO start threshold at t_0, the reference becomes enabled. The reference output rises at a rate determined by the reference short-circuit current and the external bypass capacitor. C_T remains discharged until V_{REF} exceeds $4V_{BE}$. There is no gate drive until V_{REF} reaches the "reference-good" level (4.4V) (see Figure 16). Once V_{REF} exceeds $4V_{BE}$ (t_1), C_T is charged towards the upper threshold of the oscilllator/timer. Although the gate drives are enabled at t_2, the first-pulse inhibit latch continues to blank the outputs. This latch is reset when C_T voltage crosses the upper oscillator threshold at t_3. OUTA is gated on after the CLK pulse elapses.

Without the first-pulse inhibit circuit, the first OUTA pulse would be on for time T_{ONI} which could be as much as 2 to 3 times longer than the desired T_{ON} time. The first-pulse inhibit latch ensures no abnormally long first gate drive pulse, independent of V_{REF} rise time.

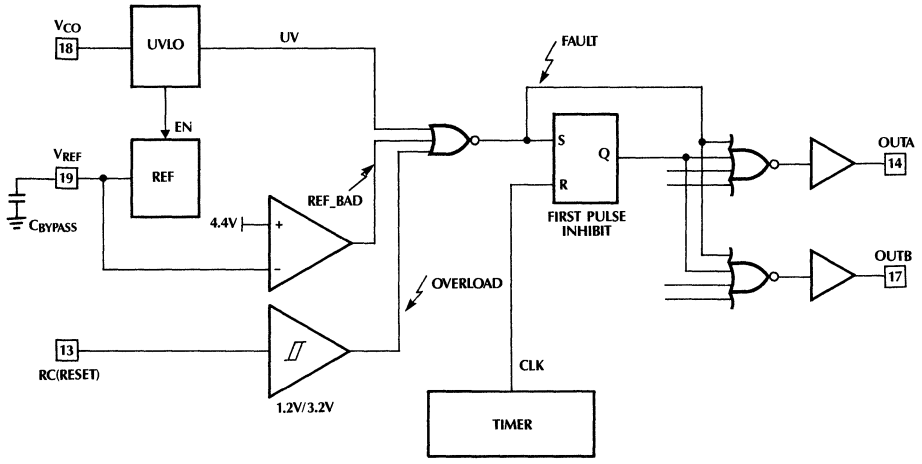


Figure 15. Operation of UVLO and the First-Pulse Inhibit Circuit

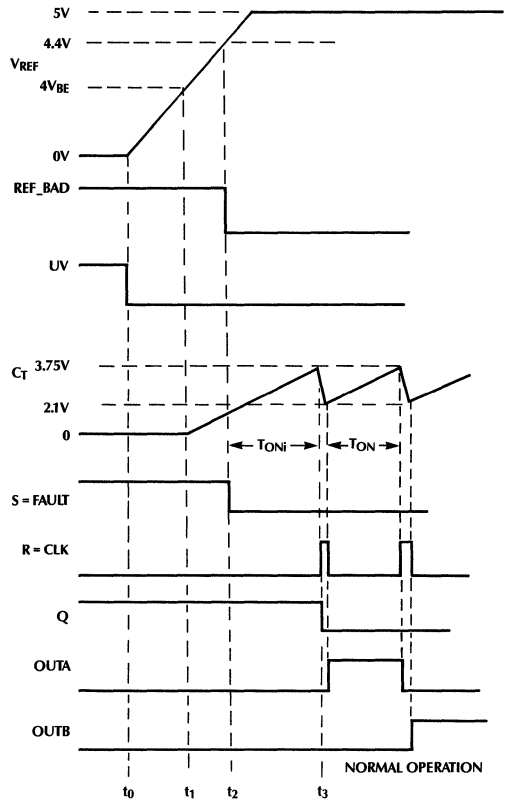
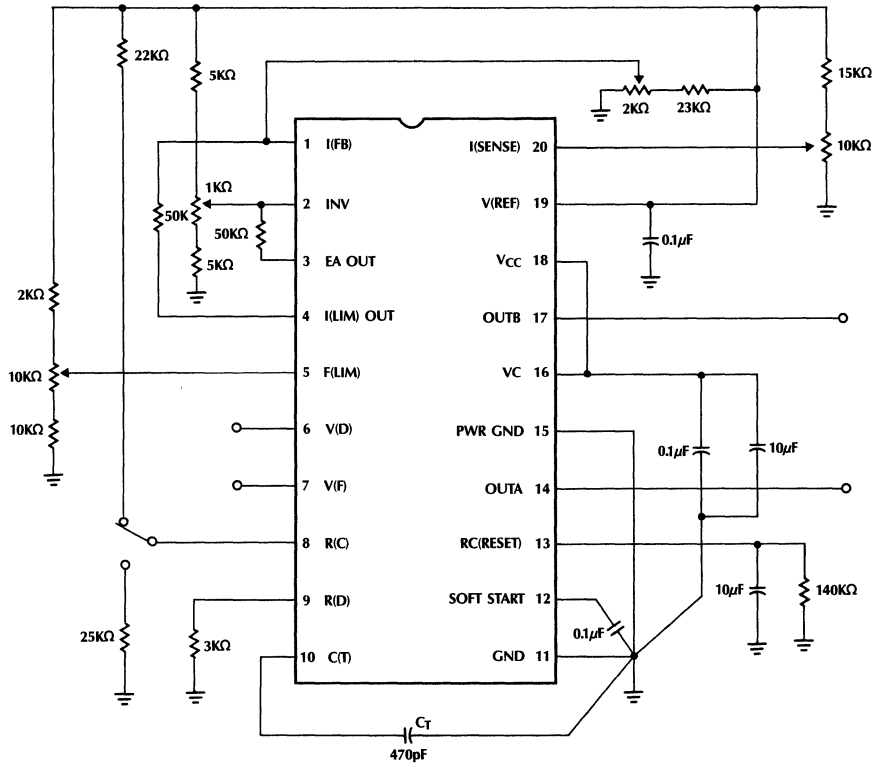


Figure 16. Timing Diagram Illustrating Initial Start-Up and the First-Pulse Inhibit

Open Loop Laboratory Test Fixture



This test fixture is useful for exercising many of the ML4816's functions and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4816CP	0°C to +70°C	Plastic DIP (P20)
ML4816CS	0°C to +70°C	Plastic SOIC (S20W)

Micro Linear

ML4817

Single-Ended High Frequency PWM Controller

GENERAL DESCRIPTION

The ML4817 High Frequency PWM Controller is optimized for use in single-ended Switch Mode Power Supply designs running at frequencies up to 1MHz. Propagation delays are minimal through the comparators and logic for reliable high frequency operation while slew rate and bandwidth are maximized in the error amplifier. This controller is designed to work in either voltage or current mode.

A unique overload protection circuit helps to limit stress on the output devices. This integrating method of fault detection also provides for reset delay before restart. A 1.5V threshold current limit comparator provides cycle-by-cycle current limit.

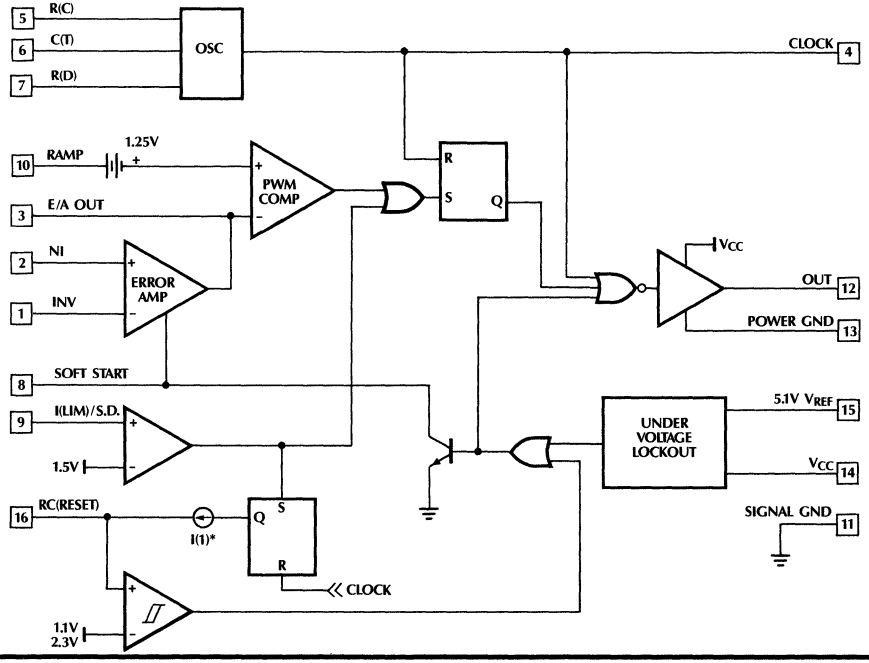
The ML4817 oscillator features accurately programmable dead time control to precisely limit the maximum duty cycle.

The ML4817 is fabricated on a 40V bipolar process from the FB3480 Power Supply Controller Array. Customized versions of this controller are therefore easily implemented. Please refer to the FB3480 datasheet for more information.

FEATURES

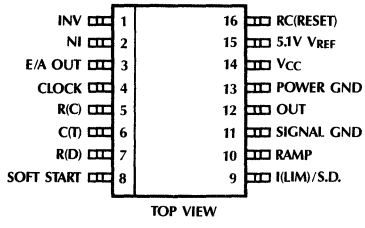
- Practical Operation at Switching Frequencies to 1MHz
- High Current (2A peak) Totem Pole Output
- Temperature Stable Precise Oscillator Frequency and Dead Time
- Precision Maximum Duty Cycle Limit
- Integrating Fault Detection with Reset Delay
- Fast Shut Down Path from Current Limit to Output
- Output Pulls Low for Under-Voltage Lockout

BLOCK DIAGRAM



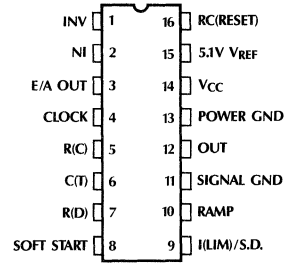
PIN CONFIGURATIION

ML4817
16-Pin SOIC



TOP VIEW

ML4817
16-Pin DIP



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	INV	Inverting input to error amp.
2	NI	Non-inverting input to error amp.
3	E/A OUT	Output of error amplifier and input to main comparator.
4	CLOCK	Oscillator output.
5	R(C)	Timing Resistor for Oscillator — sets charging current for oscillator timing capacitor (Pin 6).
6	C(T)	Timing Capacitor for Oscillator.
7	R(D)	Resistor which sets discharge current for oscillator timing capacitor.
8	SOFT START	Normally connected to Soft Start Capacitor and charging resistor.
9	I(LIM)/S.D.	Current limit sense pin. Normally connected to current sense resistor.
10	RAMP	Non-inverting input to main comparator. Connected to C(T) for Voltage Mode operation or to current sense resistor for current mode.
11	SIGNAL GND	Analog Signal Ground.
12	OUT	High Current Totem pole output.
13	POWER GND	Return for the High Current Totem pole outputs.
14	V_{CC}	Positive Supply for the IC.
15	5.1 V_{REF}	Buffered output for the 5.1V voltage reference.
16	RC(RESET)	Timing elements for integrating fault detection and reset delay circuits.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (Pin 14) 30V
Output Current, Source or Sink (Pin 12)
  DC 0.5A
  Pulsed (0.5μs) 2.0A
Analog Inputs
  (Pins 1, 2, 8, 9, 10, 16) ..... -0.3V to 6V
Clock Output Current (Pin 4) ..... -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 100mA
Oscillator Charging Current (Pin 5) ..... -5mA
Junction Temperature ..... 125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +260°C
Thermal Resistance (θ_{JA})
  Plastic DIP ..... 65°C/W
  Plastic SOIC ..... 65°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R(C) = 2540Ω, R(D) = 2470Ω, C_T = 470pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial Accuracy	T_A = 25°C	500	525	550	KHz
Voltage Stability	12V < V_{CC} < 25V		0.2		%
Temperature Stability	(note 1)			TBD	%
Total Variation	line, temp (note 1)	TBD		TBD	KHz
Maximum Duty Cycle	$V_{PIN\ 1}$ = 2.3V, $V_{PIN\ 2}$ = 2.5V $V_{PIN\ 9}$ = $V_{PIN\ 10}$ = 0V, T_A = 25°C	44	45	46	%
Maximum Duty Cycle	line, temp (note 1)	42		48	%
C(T) Discharge Current	$V_{PIN\ 6}$ = 4V, $V_{PIN\ 7}$ = 3V		4.5		mA
Clock Out High		4.0	4.5		V
Clock Out Low				2.2	V
Ramp Peak			3.75		V
Ramp Valley			2.15		V
Ramp Valley to Peak			1.60		V
Reference Section					
Output Voltage	T_A = 25°C, I_O = 1mA	5.00	5.10	5.20	V
Line Regulation	12V < V_{CC} < 25V		2	20	mV
Load Regulation	1mA < I_O < 10mA		5	20	mV
Temperature Stability	T_{MIN} < T_A < T_{MAX}, (note 1)		.2	.4	mV/°C
Total Variation		4.95		5.25	V
Output Noise Voltage	10Hz to 10KHz		50		μV
Long Term Stability	T_J = 125°C, 1000 hrs, (note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	-15	-50	-100	mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R(C) = 2540Ω, R(D) = 2470Ω, C_T = 470pF, T_A = Operating Temperature Range, V_{CC} = 15V.

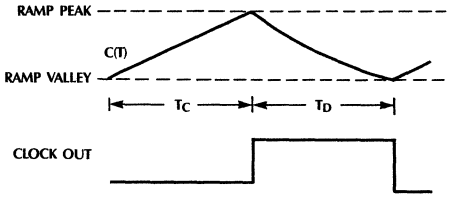
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section					
Input Offset Voltage				15	mV
Input Bias Current			.6	3	μA
Input Offset Current			.1	1	μA
Open Loop Gain	$1 < V_O < 4V$	60	95		dB
CMRR	$1.5 < V_{CM} < 5.5V$	60	95		dB
PSRR	$12 < V_{CC} < 25V$	80	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4.0V	–.5	–1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = –0.5mA	5.3			V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth	(note 1)	3	5.5		MHz
Slew Rate	(note 1)	6	12		V/μs
PWM Comparator Section					
Pin 10 Bias Current	$V_{PIN\ 10}$ = 0V		–1	–5	μA
Pin 3 Zero D.C. Threshold	$V_{PIN\ 10}$ = 0V	1.08	1.25	1.45	V
Delay to Output	(note 1)		50	80	ns
Soft Start Section					
Pin 8 Bias Current	$V_{PIN\ 8}$ = 4V			10	μA
Discharge Current	$V_{PIN\ 8}$ = 1V	10			mA
Current Limit/Shutdown Section					
Pin 9 Bias Current	$0V < V_{PIN\ 9} < 4V$			+10	μA
Current Limit Threshold	$V_{PIN\ 16}$ = 0V	1.35		1.65	V
Delay to Output	(note 1)		40	70	ns
Pin 16 Shutdown Threshold		2.05		2.55	V
Pin 16 Restart Threshold		0.9		1.3	V
Pin 16 Charging Current	$V_{PIN\ 9}$ = 2V, $V_{PIN\ 16}$ = 1.5V	–150	–210	–275	μA
Output Section					
Output Low Level	I_{OUT} = 20mA		.25	.4	V
	I_{OUT} = 200mA		1.2	2.2	V
Output High Level	I_{OUT} = –20mA	12.0	13.5		V
	I_{OUT} = –200mA	11.5	13.0		V
Rise/Fall Time	C_L = 1000pF, (note 1)		30	60	ns
Under-Voltage Lockout Section					
Start Threshold		12.0	13.8	15.0	V
UVLO Hysteresis		3.0	3.6	4.2	V
Supply Current					
Start Up Current			1.8	2.5	mA
I_{CC}	$V_{PIN\ 1}$ = 2.3V, $V_{PIN\ 2}$ = 2.5V $V_{PIN\ 9,\ 10}$ = 0V, C_L = 0, T_A = 25°C		34	42	mA

Note 1. This parameter is not 100% tested in production but guaranteed by design.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4817 oscillator charges the external capacitor, C_T, with a current (I_{SET}) equal to $2/R_C$. When the C_T voltage reaches the upper threshold (Ramp Peak), the comparator changes state, turning off the current source and turning on the 4.5mA current sink which is voltage clamped to 1.05V by Q1. The capacitor then discharges to the lower threshold (Ramp Valley) with a time constant determined by R_D and C_T.



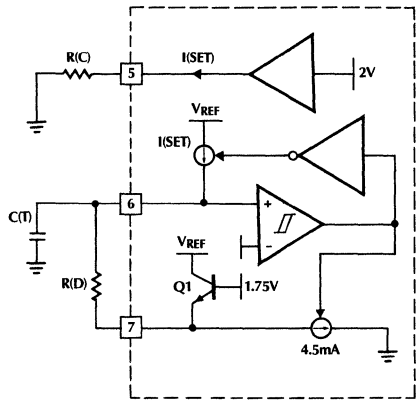


Figure 1. Oscillator Block Diagram

Oscillator period can be determined by the following formula:

$$T_{OSC} = T_C + T_D \quad (1)$$

$$T_C = \frac{(\text{RAMP PEAK} - \text{VALLEY})\, C_T\, R_C}{2} \quad \text{or}$$

$$T_C = 0.8\,(C_T\, R_C) \quad (2)$$

$$T_D = R_D C_T \ln\left(\frac{\text{RAMP PEAK} - 1.05}{\text{RAMP VALLEY} - 1.05}\right) \quad \text{or}$$

$$T_D = 0.90\,(R_D C_T) \quad (3)$$

since: $f_{OSC} = \frac{1}{T_C + T_D}$

then: $f_{OSC} = \frac{1}{C_T\,(.8R_C + .90R_D)}$ (4)

since: $\text{Duty Cycle} = \frac{T_C}{T_C + T_D}$

then: $\text{Duty Cycle} = \frac{1}{1 + 1.12\left(\frac{R_D}{R_C}\right)}$ (5)

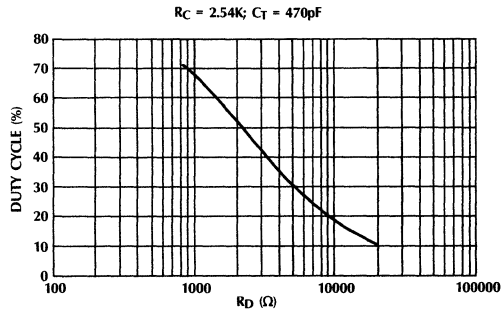


Figure 2. Duty Cycle vs R(D)

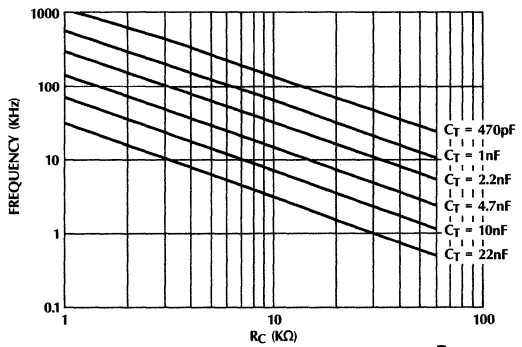


Figure 3. Oscillator Frequency vs $R_D = \frac{R_C}{1.03}$ R(C) for 50% Duty Cycle

7

ERROR AMPLIFIER

The ML4817 error amplifier is a 5.5MHz bandwidth, 12V/μs slew rate op-amp with provision for limiting the positive output voltage swing for ease in implementing the soft start function.

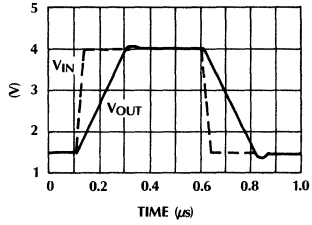


Figure 4. Unity Gain Slew Rate

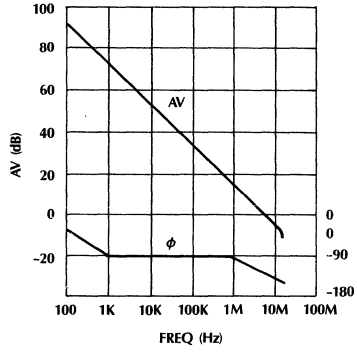


Figure 5. Open Loop Frequency Response

OUTPUT DRIVER STAGE

The ML4817 Output Driver is a 2A peak output high speed totem pole circuit designed to quickly switch capacitive loads, such as power MOSFET transistors.

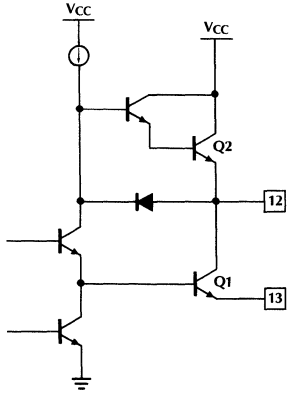
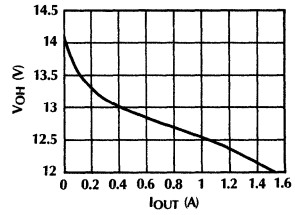


Figure 6. Power Driver Simplified Schematic

V_{OH} Curve



V_{OL} Curve

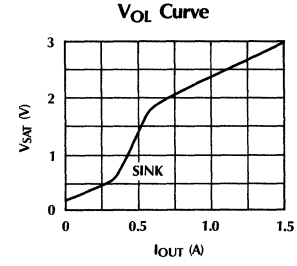


Figure 7. Saturation Curves

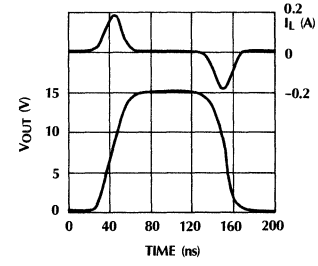


Figure 8. Rise/Fall Time (C_L = 1000pF)

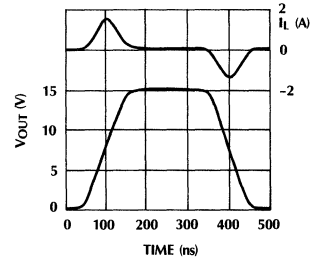


Figure 9. Rise/Fall Time (C_L = 10,000pF)

UNDER-VOLTAGE LOCKOUT

When V_{CC} is below 13.8V, the IC draws very little current (1.8mA typ.) and V_{REF} is disabled. When V_{CC} rises above 13.8V, the IC becomes active and V_{REF} is enabled and will stay in that condition until V_{CC} falls below 10.2V.

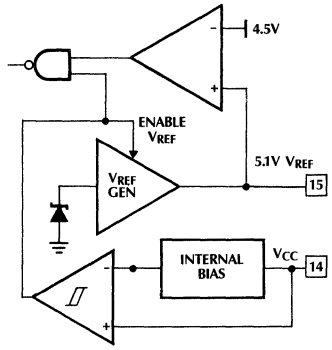


Figure 10. Under-Voltage Lockout Circuit

CURRENT LIMIT, FAULT DETECTION AND SOFT START

When the current (sensed on pin 9) reaches the 1.5V limit, the PWM cycle is terminated. The flip flop (figure 10) turns on current source I(1) to charge C_{RST} and remains on until CLOCK goes high. The magnitude of current source I(1) is .25 × I_{SET} where I_{SET} is the oscillator charging current. When C_{RST} has charged to 2.3V, a soft start reset occurs. The number of times the PWM cycle is terminated due to over-current is "remembered" on C(RST). Over time, C(RST) is discharged by R(RST) providing a measure of "forgetting" when the over-current condition no longer occurs.

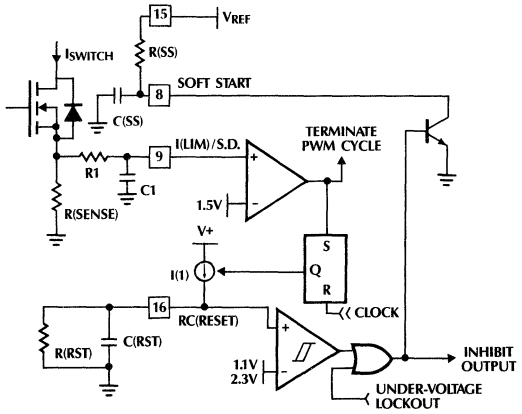


Figure 11. Over-Current, Soft Start, and Integrating Fault Detect Circuits

Since the per cycle charge on RC(RESET) is proportional to how early in the PWM cycle the reset occurs, a reset will occur more quickly under output short circuit conditions (figures 12c and 12d) than during a load surge (figures 12a and 12b).

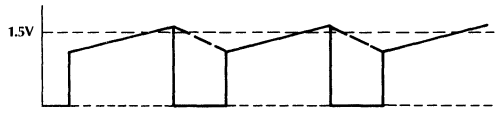


Figure 12a. Pin 9 (I_{LIMIT}) Waveform During Load Surge

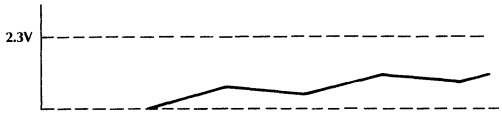


Figure 12b. Corresponding Waveform on Pin 16 (RC_{RESET})

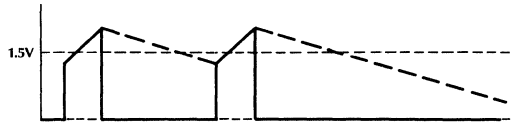


Figure 12c. Current Waveform During Short Circuit (Pin 9)

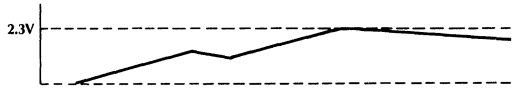


Figure 12d. RC(RESET) (Pin 16) Increases More Quickly During Short Circuit Condition

When the soft start reset occurs, the output is inhibited and the soft start capacitor is discharged. The output will remain off until C(RST) discharges to 1.1V through R(RST), providing a reset delay. When the IC restarts, the error amplifier output voltage is limited to the voltage at pin 8, thus limiting the duty cycle.

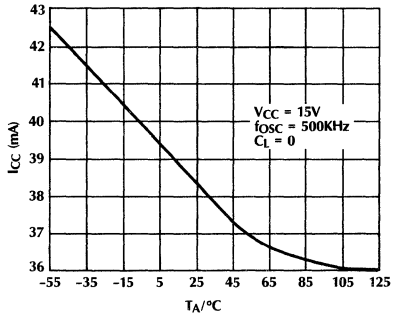


Figure 13. Supply Current vs. Temperature

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4817CP	0°C to +70°C	DIP (P16)
ML4817CS	0°C to +70°C	SOIC (S16W)

Micro Linear

ML4818

Phase Modulation/Soft Switching Controller

GENERAL DESCRIPTION

The ML4818 is a complete phase modulation control IC suitable for full bridge soft switching converters. Unlike conventional PWM circuits, the phase modulation technique allows for zero voltage switching transitions and square wave drive across the transformer. The IC modulates the phases of the two sides of the bridge to control output power.

The ML4818 can be operated in current mode. The delay times for the outputs are externally programmable to allow the zero voltage switching transitions to take place.

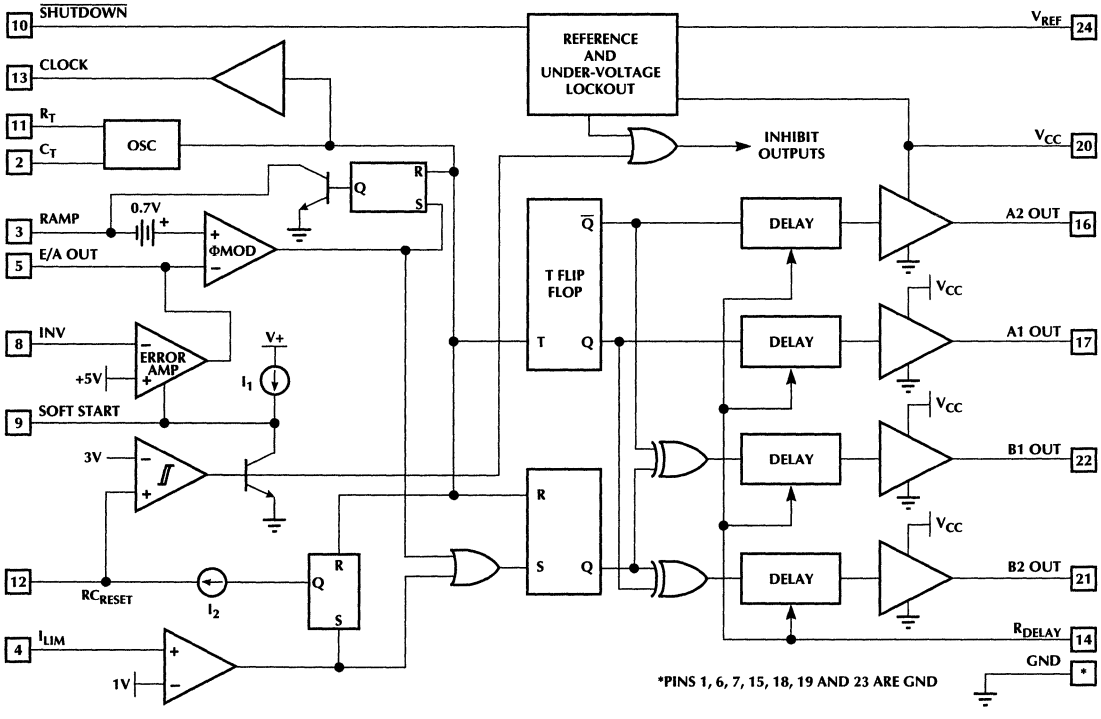
Pulse-by-pulse current limit, integrating fault detection, and soft start reset are provided. The under-voltage lockout circuit features a 6V hysteresis with a low starting current to allow off-line start up with a low power bleed resistor. A shutdown function powers down the IC, putting it into a low quiescent state.

High frequency phase modulation (>500KHz) can be implemented using the ML4828 BiCMOS phase modulator. The ML4818 contains four high current totem pole outputs which feature high slew rate with low cross conduction.

FEATURES

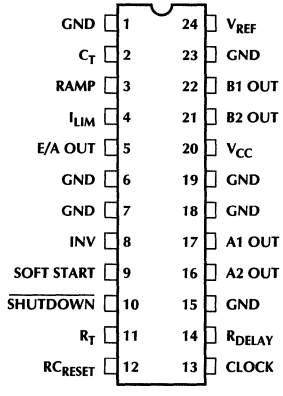
- Full Bridge Phase Modulation **Zero Voltage Switching** Circuit with Programmable ZV transition times
- Constant Frequency Operation to 500KHz
- Current Mode Operation
- Cycle-by-Cycle Current Limiting with Integrating Fault Detection and Restart Delay
- Precision buffered 5V Reference (+ 1%)
- Four 1.5 A Peak Current Totem-Pole Output Drivers
- Under-Voltage Lockout circuit with 6V Hysteresis.
- Power DIP package allows higher dissipation

BLOCK DIAGRAM



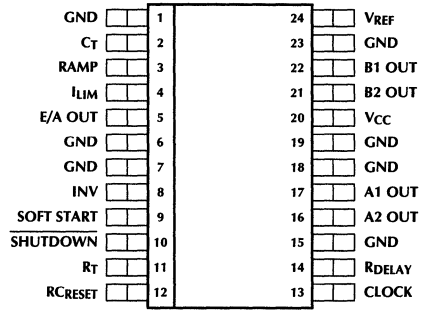
PIN CONNECTION

24-Pin Power DIP



TOP VIEW

24-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	GND	Ground
2	C_T	Timing Capacitor for Oscillator
3	RAMP	Non-Inverting input to main comparator. Connected to current sense resistor for current mode
4	I_{LIM}	Current limit sense pin. Normally connected to current sense resistor
5	E/A OUT	Output of error amplifier and input to PWM comparator
6,7	GND	Ground and Substrate
8	INV	Inverting input to error amp
9	SOFT START	Normally connected to Soft Start Capacitor
10	$\overline{\text{SHUTDOWN}}$	Pulling this pin low puts the IC into a power down mode and turns off all outputs. This pin is internally pulled up to Vref.
11	R_T	Resistor which sets discharge current for oscillator timing capacitor
12	RC_{RESET}	Timing elements for Integrating fault detection and reset delay circuits
13	CLOCK	Oscillator output
14	R_{DELAY}	Resistor to ground on this pin programs the amount of delay from the time an output turns off until its complementary output turns on
15	GND	Ground
16	A2 OUT	High Current Totem pole output A1
17	A1 OUT	High Current Totem pole output A2
18,19	GND	Ground and Substrate
20	V_{CC}	Positive Supply for the IC
21	B2 OUT	High Current Totem pole output B1
22	B1 OUT	High Current Totem pole output B2
23	GND	Ground
24	V_{REF}	Buffered output for the 5.0 V voltage reference

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pin 20) 30V
Output Current, Source or Sink (Pins 16,17,21,22)
DC 0.5A
Pulse (0.5 µs) ..... 1.5 A
Analog Inputs
(Pins 2 thru 5, 8 thru 10, 12) ..... –0.3V to 6V
Clock Output Current (Pin 11) ..... –5mA
Error Amplifier Output Current (Pin 5) 5mA
Soft Start Sink Current (Pin 9) ..... 50 mA
Oscillator Charging Current (Pin 2) ..... –5mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 Sec.) ..... +260°C
Thermal Resistance (θ_{JA}) (see fig 13,14)
Plastic Power DIP ..... 40°C/W

OPERATING CONDITIONS

Operating Temperature Range ..... 0°C to +70°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 12.7KΩ, C_T = 250pF, R_{CLK} = 3KΩ, R_{DELAY} = 5KΩ, T_A = Operating Temperature Range, V_{CC} = 15V. (Note 2)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
OSCILLATOR					
Initial accuracy	T_A = 25°C	410	450	510	KHz
Voltage stability	12V < V_{CC} < 25V		–0.3		%/V
Temperature stability	(note 1)		0.2		%
Total Variation	line, temp.	375		525	KHz
C_T Discharge Current	V_{PIN2} = 2V	4.7	5.5	6.3	mA
Clock out High		2.4	3.1		V
Clock out Low			0	0.4	V
Ramp Peak			4.1		V
Ramp Valley			1.5		V
Ramp Valley to Peak			2.6		V
REFERENCE SECTION					
Output Voltage	T_A = 25°C, I_O = 1mA	4.95	5.0	5.05	V
Line regulation	12V < V_{CC} < 25V		2	20	mV
Load regulation	1mA < I_O < 10 mA		3	20	mV
Temperature stability	(note 1)		.2		mV/°C
Total Variation		4.85		5.15	V
Output Noise Voltage	10Hz to 10 KHz		50		mV
Long Term Stability	T_J = 125°C, 1000 hrs, (note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	–20	–50		mA
ERROR AMPLIFIER SECTION					
Input Offset Voltage		–40		+30	mV
Input Bias Current			0.6	3	µA
Input Offset Current			0.1	1	µA
Open Loop Gain	1 < V_O < 4V	65	75		dB
PSRR	12 < V_{CC} < 25V	70	80		dB
Output Sink Current	$V_{PIN\ 5}$ = 1V	1	3.2		mA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
ERROR AMPLIFIER SECTION (Continued)					
Output Source Current	$V_{PIN\ 5}$ = 5.1V	–0.5	–2.2		mA
Output High Voltage	$I_{PIN\ 5}$ = –0.5mA	5.0	5.5	6.0	V
Output Low Voltage	$I_{PIN\ 5}$ = 1mA			0.8	V
Unity Gain Bandwidth	(note 1)	2.0	2.8		MHz
Slew Rate (note 1)			8.5		V/µs
PHASE MODULATOR SECTION					
Pin 3 Bias Current	$V_{PIN\ 3}$ = 2.5V		–1	–10	µA
Pin 5 Zero D.C. Threshold	$V_{PIN\ 3}$ = 0V		0.6	0.9	V
T_{PD1}, pin 3 to Output	(note 1)		50	80	ns
T_{DELAY}	C_L = 1nF		200	250	ns
V_{PIN14}			4.3		V
SOFT-START SECTION					
Pin 9 Charge Current	$V_{PIN\ 9}$ = 4V	–15	–25	–30	µA
Discharge Current	$V_{PIN\ 9}$ = 1V	10	20	30	mA
CURRENT LIMIT/SHUTDOWN SECTION					
Pin 4 Bias Current	0 V < $V_{PIN\ 4}$ < 4V		–1	–10	µA
Current Limit Threshold	$V_{PIN\ 10}$ = 0V	0.92	1.02	1.12	V
T_{PD1}, pin 4	(note 1)		50		ns
Pin 12 Shutdown Threshold		3.15	3.4	3.65	V
Pin 12 Restart Threshold		1.0	1.3	1.6	V
Pin 12 Charging Current	$V_{PIN\ 4}$ =2V, $V_{PIN\ 12}$ = 1.5V	–400	–523		µA
Pin 10 Shutdown Threshold		2.0	2.4	2.8	V
Pin 10 Input Bias Current	$V_{PIN\ 10}$ = 0		–25	–100	µA
OUTPUT SECTION					
Output Low Level	I_{OUT} = 20 mA I_{OUT} = 200 mA, T_A = 25°C		0.1 0.7	0.4 2.8	V V
Output High Level	I_{OUT} = –20 mA I_{OUT} = –200 mA, T_A = 25°C	12.0 11.0	13.5 13.0		V V
Rise/Fall Time	C_L = 1000pF, (note 1)		50	75	ns
UNDER-VOLTAGE LOCKOUT SECTION					
Start Threshold		15.5	16.5	17.2	V
Stop Threshold		9.25	10.2	10.7	V
SUPPLY CURRENT					
Start Up Current	V_{CC} < 15.8V		3	4	mA
I_{CC}	$V_{PIN\ 8}$ = 4V, $V_{PIN\ 3,4}$ = 0V, C_L = 1nF T_A = 25°C		60	70	mA

Note 1: This parameter not 100% tested in production but guaranteed by design.
Note 2: V_{CC} must be brought above the UVLO start voltage (17.2V) before dropping to V_{CC} = 15V to ensure start-up.

FUNCTIONAL DESCRIPTION

PHASE MODULATOR

Power is controlled by modulating the switching phase on sides A and B of the full H-bridge converter (Figure 1). Power is delivered to the output through the transformer secondary. The power conversion process is described by the following sequence and illustrated by the timing diagram of Figure 2:

1. A2 and B1 are high (Q1 and Q2 are on), beginning the power conversion cycle.
2. After the Φ MOD comparator trips, B1 goes low turning off Q2. The parasitic drain-to-source capacitances of Q2 and Q4 charge to +VIN. This forces the drain-to-source voltage across Q3 to 0V.
3. B2 now goes high after t_{DELAY} (set by R_{DELAY}). Since the voltage across Q3 is now 0V, B2 turns Q3 on at zero voltage.
4. The CLOCK now goes high turning A2 off. During this period, Q1 and Q2 and Q4 are off. The transformer leakage current discharges the drain-to-source capacitance on Q4 until there is 0V across it.
5. A1 will remain low for a period defined by t_{DELAY}, then it goes high. The voltage across Q4 is now 0V as A1 turns it on at zero voltage.
6. The previous sequence is now repeated with the opposite polarity on all outputs (see Figure 2).

The above sequence is then repeated but with the opposite polarity on all outputs.

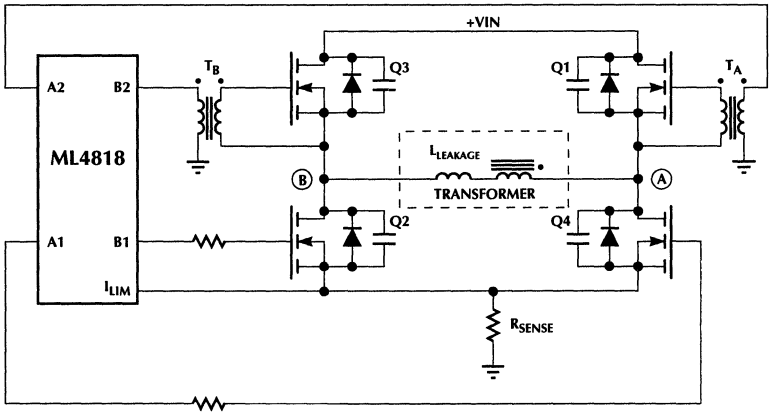


Figure 1. Simplified diagram of Phase Modulated power Outputs.

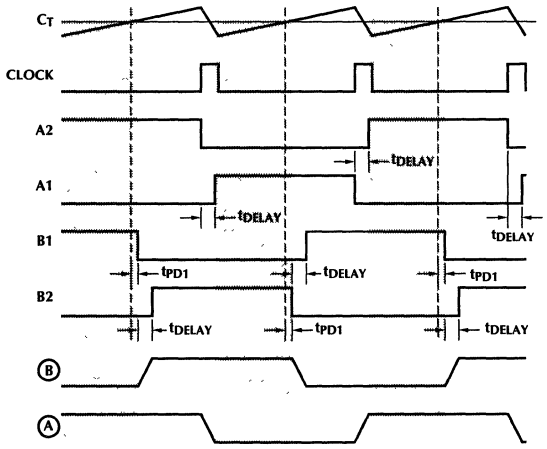


Figure 2. Phase Modulation control waveforms (Shaded areas indicate a power cycle).

The ML4818 can also be used in current mode by sensing load current on the RAMP input (pin 3).

The four output delay timers are programmed via an external R_{DELAY} resistor as shown below. This resistor value should be no less than 1KΩ. Expressing R_{DELAY} in KΩ the delay, in ns is:

$$T_{DELAY} = 33 \times R_{DELAY} + 45 \quad (1)$$

The ML4818 contains special logic circuits to provide for voltage mode feed-forward and lock out long pulses into the internal logic. This prevents instability from occuring when the Φ Comparator trips in voltage mode.

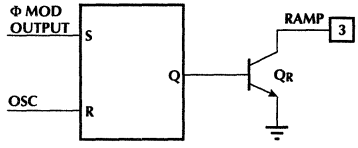


Figure 3. Voltage Feed-Forward Circuit.

The collector of Q_R in figure 3 is high only during a power cycle. When the power cycle terminates, pin 3 is pulled low. In voltage mode operation, a capacitor is connected from pin 3 to GND with a resistor from pin 3 to V_{IN} to provide input voltage feed forward.

OSCILLATOR

The ML4818 oscillator charges the external capacitor, C_T, with a current (I_{SET}) equal to $5/R_T$. When the C_T voltage reaches the upper threshold (Ramp Peak), the comparator changes state, turning on the current sink which discharges C_T to the lower threshold (Ramp Valley). The C_T pin is clamped to Ramp Valley by Q1 (figure 5) to prevent inaccuracy due to undershoot on C_T.

To use the Clock Output for driving external synchronization circuitry, a pull-down resistor is required from CLOCK to GND.

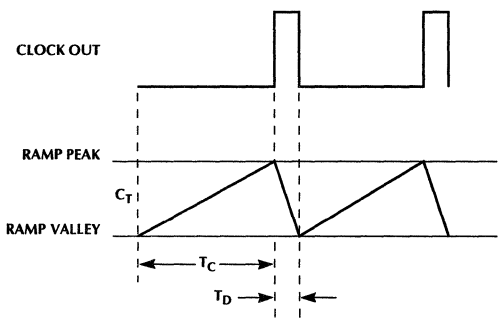


Figure 4. Oscillator Timing Diagram

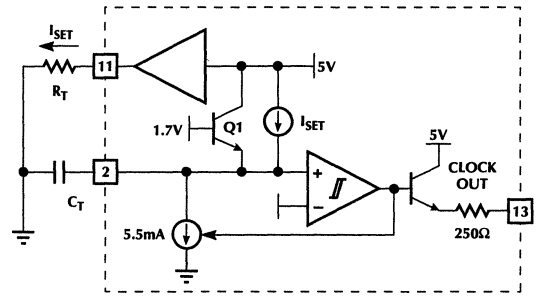


Figure 5. Oscillator Block Diagram.

For frequencies of less than 500KHz, oscillator frequency can be set by using the following formulae:

$$f_{OSC} = \frac{1}{0.52 C_T R_T + 500 C_T} \quad (2)$$

ERROR AMPLIFIER

The ML4818 error amplifier is a 2.5 MHz, bandwidth, 8.5V/μs slew rate op-amp with provision for limiting the positive output voltage swing (Output Inhibit line) to implement the soft start function. The error amplifier output source current is limited to 4.5mA.

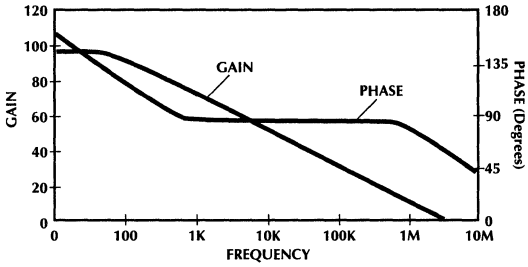


Figure 6. Error Amplifier Open-Loop Gain and Phase vs. Frequency.

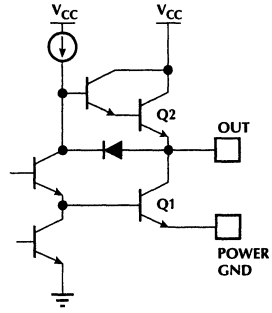


Figure 7. Power Driver Simplified Schematic.

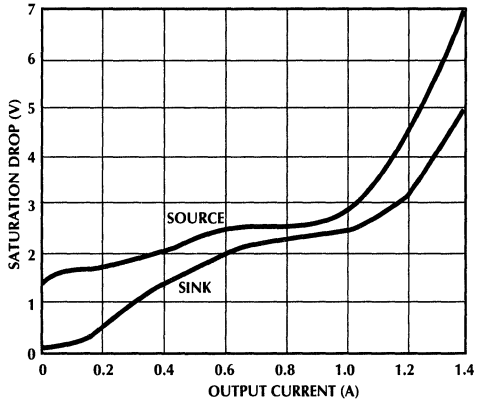


Figure 8. Output Drive Saturation Voltage vs. Output Current.

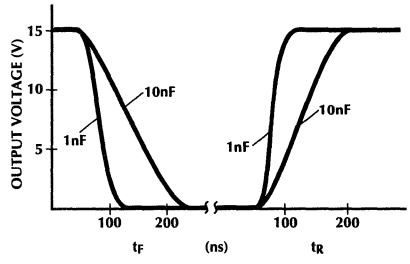


Figure 9. Output Rise/Fall Time.

7

OUTPUT DRIVER STAGE

The ML4818 has four high current high speed totem pole output drivers each capable of 1.5A peak output, designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors. Figure 8 illustrates the saturation characteristics of the ouput drive transistors shown in Figure 7. Typical rise and fall time characteristics of the output drivers are illustrated with capacitive loads of 1nF and 10nF in Figure 9.

CURRENT LIMIT, FAULT DETECTION AND SOFT START

Current limit is implemented when the current sensed on pin 4 reaches the 1V limit. At this point, the PWM cycle is terminated. The flip flop (Figure 10) turns on the current source to charge C_{RST} and remains on for the duration of the clock period. When C_{RST} has charged to 3.4V, a soft start reset occurs. The number of times the PWM cycle is terminated due to over-current is "remembered" on C_{RST}. Over time, C_{RST} is discharged by R_{RST} providing a measure of "forgetting" when the over-current condition no longer occurs. This integrating fault detection is useful in differentiation between short circuit and load surge conditions.

Since the per cycle charge on RC_{RESET} is proportional to how early in the power cycle the over-current occurs, a reset will occur more quickly under output short circuit conditions (Figures 11a and 11b) than during a load surge (Figures 11c and 11d).

When the soft start reset occurs, the output is inhibited and the soft start capacitor is discharged. The output will remain off until C_{RST} discharges to 1.3V through R_{RST}, providing a reset delay. When the IC restarts, the error amplifier output voltage is limited to the voltage at pin 9, thus limiting the duty cycle.

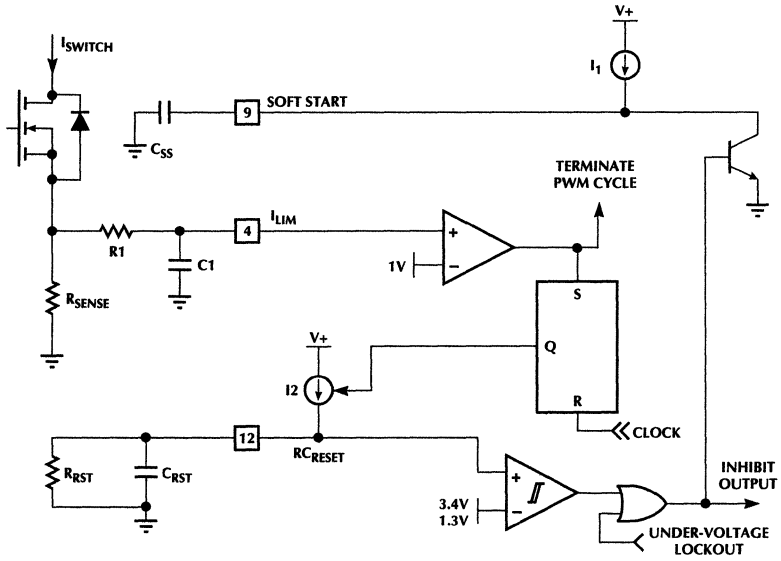


Figure 10. Over-Current, Soft-Start, and Integrating Fault Detect Circuits.

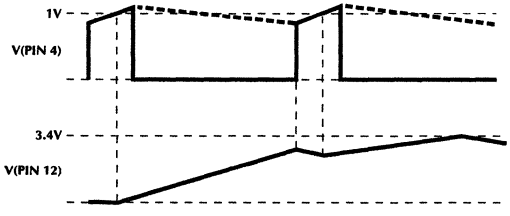


Figure 11a, 11b. I(LIMIT) and Resulting RC(RESET) Waveforms During Short Circuit.

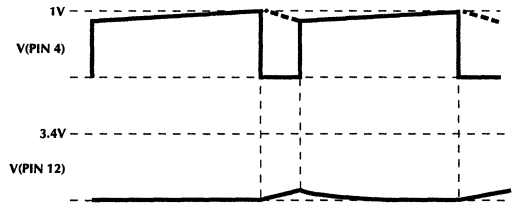


Figure 11c, 11d. I(LIMIT) and Resulting RC(RESET) Waveforms During Load Surge.

UNDER-VOLTAGE LOCKOUT

On power up, when V_{CC} is below 16V, the IC draws very little current (1.1mA typ.) and V_{REF} is disabled. When V_{CC} rises above 16V, the IC becomes active and V_{REF} is enabled and will stay in that condition until V_{CC} falls below 10.2V. (see Figure 12).

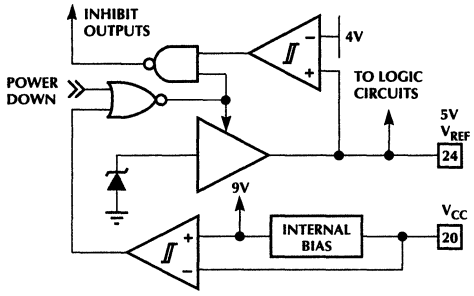


Figure 12. Under-Voltage Lockout and Reference Circuits.

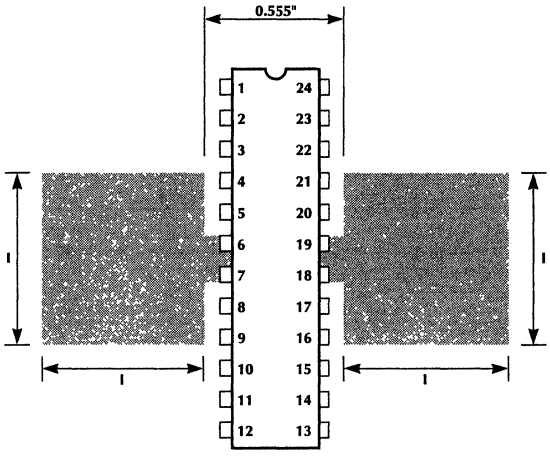


Figure 14. PC Board Copper Area Used as a Heat Sink.

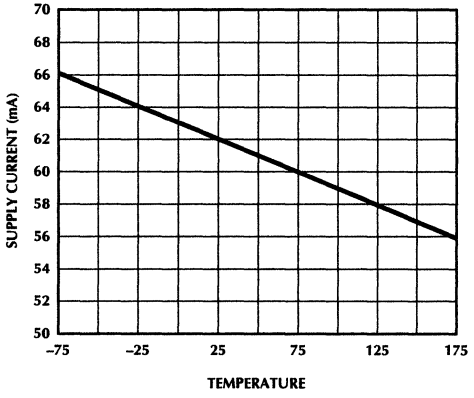


Figure 13. Supply Current vs. Temperature (°C).

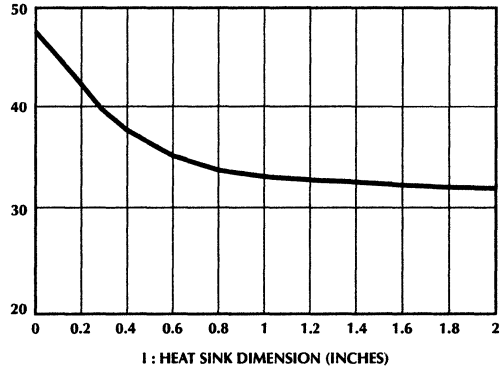


Figure 15. θ_{JA} as a Function of l (see figure 15).

THERMAL INFORMATION

The ML4818 is offered in a Power DIP package. This package features improved thermal conduction through the leadframe. Much of the heat is conducted through the center 4 grounded leads. Thermal dissipation can be improved with this package by using copper area on the board to function as a heat sink. Increasing this area can reduce the θ_{JA} (see figures 14 and 15), increasing the power handling capability of the package. Additional improvement may be obtained by using an external heat sink (available from Staver).

APPLICATIONS

The application, in Figure 16, features the ML4818 in a primary-side controlled voltage mode application with voltage feed-forward. Input voltage is rectified 120VAC (nominal). Feed-forward is provided by the ramp on pin 3 via the resistor connected to the high voltage input. Current is sensed through sense transformer T4.

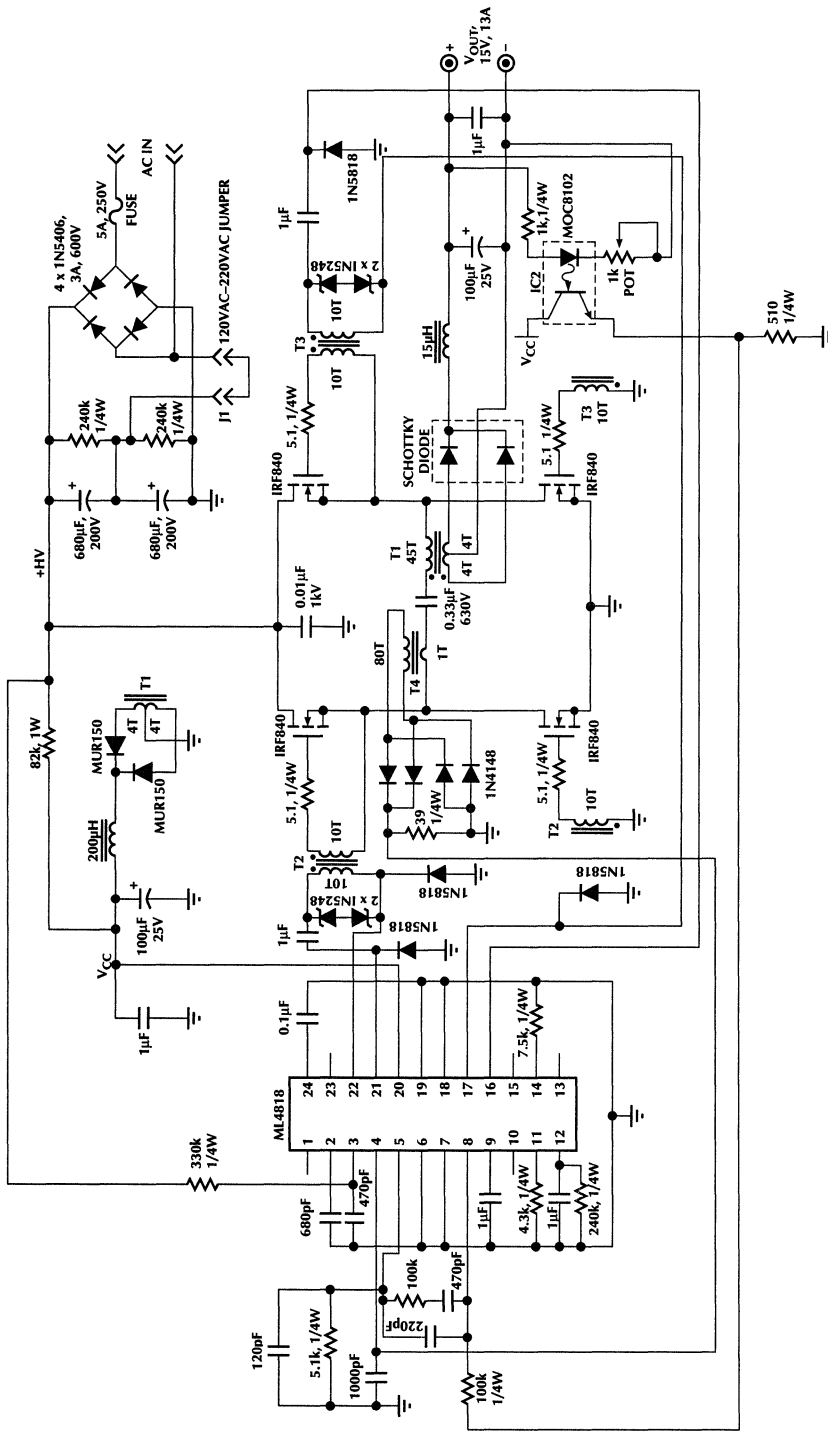


Figure 16. Offline Full Bridge Converter.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4818CP	0°C to +70°C	Power DIP (P24P)*
ML4818CS	0°C to +70°C	SOIC (S24W)

*Same dimensional outline as (P24N)

ML4818EVAL

Phase Modulation Controller Evaluation Kit

GENERAL DESCRIPTION

The ML4818EVAL kit provides a convenient vehicle to evaluate the ML4818 Phase Modulation Control IC. The board implements a 200W Phase Modulated Power Supply.

The application circuit is designed to show the performance of a 200W isolated AC to DC converter circuit. The circuit topology is a full bridge type, suitable for high power and very high frequency operation with zero voltage switching for high efficiency. The oscillator frequency of the circuit is 500KHz.

The PC board is designed around a 200W single output application circuit, however the circuit can be modified for other power levels and operating conditions.

KIT COMPONENTS

- User's Guide - Includes operating specification, procedure, kit component list, a complete parts list, performance data, and a detailed schematic.
- ML4818 Datasheet.
- Application Note #19: Phase Modulated PWM Topology with the ML4818
- Blank PC Board
- Kit Components - A sample of the ML4818 and additional components which may be difficult to procure in small quantities.

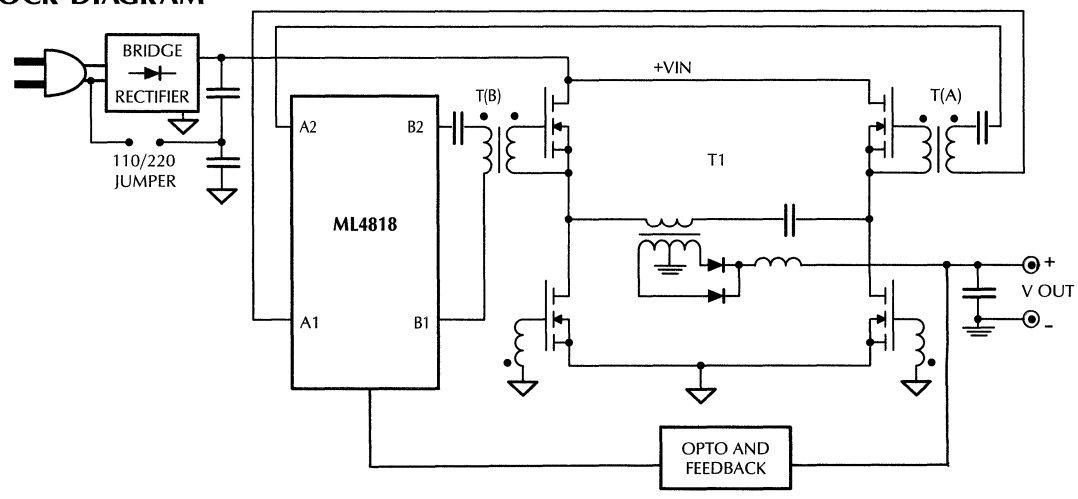
FEATURES

- Zero Voltage Switching (ZVS), high efficiency AC to DC power converter circuit
- High frequency operation resulting in smaller reactive components
- Lower conducted and radiated noise due to slower rise and fall times
- Switching and CV^2 losses greatly minimized
- Feed-forward compensated voltage mode control enables automatic compensation against instantaneous line changes
- Complete documentation and applications information

OPERATING SPECIFICATIONS

Input Voltage Range (switchable)	90 to 260V
Output Voltage	15V
Output Power	200W
Output Current	13A
Switching Frequency	250Khz.
Efficiency (V_{IN}=120V, P_{OUT}=200W)	85%

BLOCK DIAGRAM



Micro Linear

ML4819

Power Factor and PWM Controller "Combo"

GENERAL DESCRIPTION

The ML4819 is a complete boost mode Power Factor Control (PFC) which also contains a PWM controller. The PFC circuit is similar to the ML4812 while the PWM controller can be used for current or voltage mode control for a second stage converter. Since the PWM and PFC circuits share the same oscillator, synchronization of the two stages is inherent. The outputs of the controller IC provide high current (>1A peak) and high slew rate to quickly charge and discharge MOSFET gates. Special care has been taken in the design of the ML4819 to increase system noise immunity.

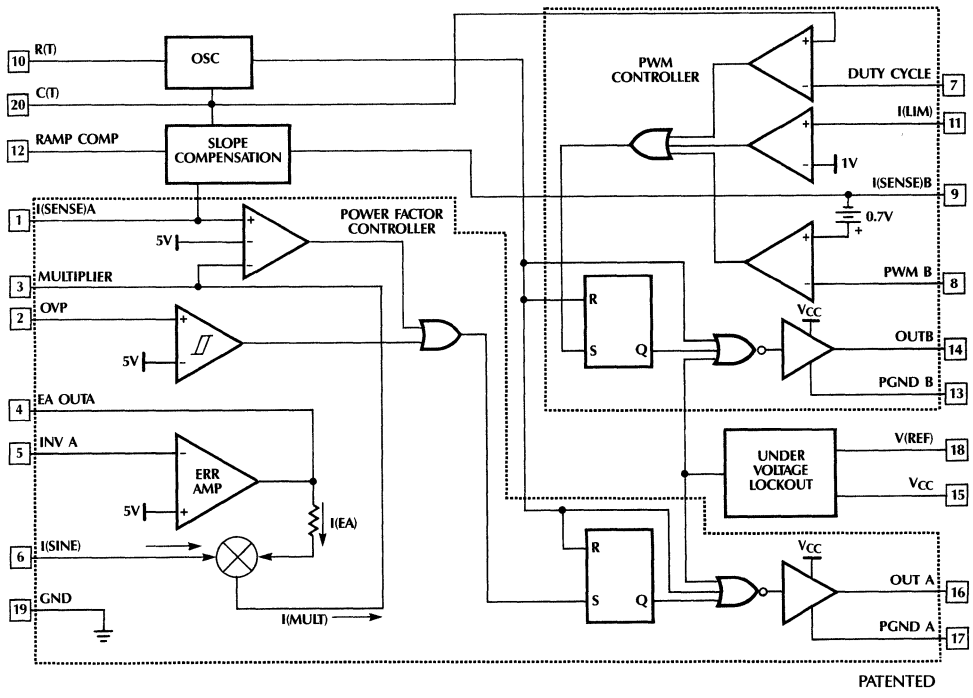
The PFC section is a peak current sensing control which uses a current sense transformer or SENSE FET to non-dissipatively sense switch current, giving the system improved overall efficiency over the average current sensing control method.

The PWM section includes cycle by cycle current limiting, precise duty cycle limiting for single ended converters, and slope compensation.

FEATURES

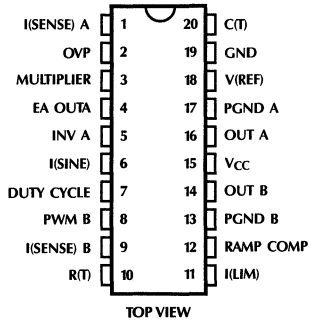
- Two 1A Peak Current Totem-Pole Output Drivers
- Precision buffered 5V Reference (±1%)
- Large oscillator amplitude for better noise immunity
- Precision duty cycle limit for PWM section
- Current input multiplier reduces external components and improves noise immunity
- Programmable Ramp Compensation circuit
- Over-Voltage comparator eliminates output "runaway" due to load removal
- Wide common mode range in current sense comparators for better noise immunity
- Under-Voltage Lockout circuit with 6V hysteresis

BLOCK DIAGRAM (Pin out shown is for DIP)



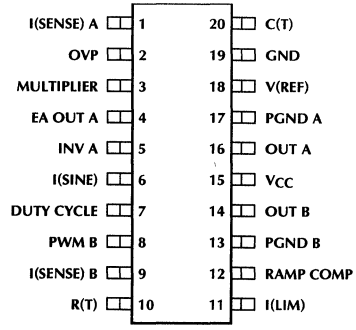
PIN CONFIGURATIONS

ML4819
20-Pin DIP



TOP VIEW

ML4819
20-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	I(SENSE) A	Input from the PFC Current Sense Transformer to the PWM comparator (+). Current Limit occurs when this point reaches 5V.
2	OVP	Input to over voltage comparator.
3	MULTIPLIER	Output of Current Multiplier. A resistor to ground on this pin converts the current to a voltage.
4	EA OUT A	Output of error amplifier.
5	INV A	Inverting input to error amplifier.
6	I(SINE)	Current Multiplier input.
7	DUTY CYCLE	PWM controller duty cycle is limited by setting this pin to a fixed voltage.
8	PWM B	Error voltage feedback input.
9	I(SENSE) B	Input for Current Sense resistor for current mode operation or for Oscillator ramp for voltage mode operation.
10	R(T)	Oscillator timing resistor pin. A 5V source across this resistor sets the charging current for C(T).
11	I(LIM)	Cycle by cycle PWM current limit. Exceeding 1V threshold on this pin terminates the PWM cycle.
12	RAMP COMP	Buffered output from the Oscillator Ramp (C(T)). A resistor to ground sets a current 1/2 of which is sourced on pins 9 and 11.
13	GND B	Return for the high current totem pole output of the PWM controller.
14	OUT B	PWM controller totem pole output.
15	V_{CC}	Positive Supply for the IC.
16	OUT A	PFC controller totem pole output.
17	GND A	Return for the high current totem pole output of the PFC controller.
18	V(REF)	Buffered output for the 5V voltage reference.
19	GND	Analog signal ground.
20	C(T)	Timing Capacitor for the Oscillator.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (V_{CC}) 35V
Output Current, Source or Sink (Pin 12)
DC 1.0A
Output Energy (capacitive load per cycle) 5μJ
Multiplier I(SINE) Input (Pin 6) 1.2mA
Error Amp Sink Current (Pin 3) 10mA
Oscillator Charge Current 2mA
Analog Inputs (Pins 1, 4, 5) ..... –0.3V to 5.5V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP or SOIC ..... 65°C/W

OPERATING CONDITIONS

Temperature Range
ML4819C ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 14KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V (note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial Accuracy	T_J = 25°C	90	97	104	KHz
Voltage Stability	12V < V_{CC} < 25V		0.2		%
Temperature Stability			2		%
Total Variation	line, temp	88		106	KHz
Ramp Valley			0.9		V
Ramp Peak			4.3		V
R(T) Voltage		4.8	5.0	5.2	V
Discharge Current (pin 8 open)	T_J = 25°C, $V_{PIN\ 16}$ = 2V	7.5	8.4	9.3	mA
	$V_{PIN\ 16}$ = 2V	7.2	8.4	9.5	mA
Duty Cycle Limit Comparator					
Input Offset Voltage		–15		15	mV
Input Bias Current			–2	–10	μA
Duty Cycle	$V_{PIN\ 7}$ = $V_{REF/2}$	43	45	49	%
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	V
Line Regulation	12V < V_{CC} < 25V		2	20	mV
Load Regulation	1mA < I_O < 20mA		8	25	mV
Temperature Stability			.4		%
Total Variation	line, load, temp	4.9		5.1	V
Output Noise Voltage	10Hz to 10KHz		50		μV
Long Term Stability	T_J = 125°C, 1000 hrs, (note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	–30	–85	–180	mA
Error Amplifier Section					
Input Offset Voltage		–15		15	mV
Input Bias Current			–0.1	–1.0	μA
Open Loop Gain	1 < $V_{PIN\ 4}$ < 5V	60	75		dB
PSRR	12V < V_{CC} < 25V	60	90		dB
Output Sink Current	$V_{PIN\ 4}$ = 1.1V, $V_{PIN\ 5}$ = 5.2V	2	12		mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 14KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V (note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section (Continued)					
Output Source Current	$V_{PIN\ 4}$ = 5.0V, $V_{PIN\ 5}$ = 4.8V	–0.5	–1.0		mA
Output High Voltage	$I_{PIN\ 4}$ = –0.5mA, $V_{PIN\ 5}$ = 4.8V	6.5	7.0		V
Output Low Voltage	$I_{PIN\ 4}$ = 2mA, $V_{PIN\ 5}$ = 5.2V		0.7	1.0	V
Unity Gain Bandwidth			1.0		MHz
Multiplier					
I(SINE) Input Voltage	I(SINE) = 500μA	.4	.7	.9	V
Output Current (pin 2)	I(SINE) = 500μA, Pin 5 = V_{REF} – 20mV	460	495	505	μA
	I(SINE) = 500μA, Pin 5 = V_{REF} + 20mV		0	10	μA
	I(SINE) = 1mA, Pin 5 = V_{REF} – 20mV	900	990	1005	μA
Bandwidth			200		KHz
PSRR	12V < V_{CC} < 25V		70		dB
Slope Compensation Circuit					
RAMP COMP Voltage (pin 12)			$V_{PIN\ 20}$ – 1		V
I_{OUT} (pin 1 or pin 9)	$I_{PIN\ 12}$ = 100μA (note 3)	45	48	51	μA
OVP Comparator					
Input Offset Voltage	Output Off	–15		15	mV
Hysteresis	Output On	100	120	140	mV
Input Bias Current			–0.3	–3	μA
Propagation Delay			150		ns
I(SENSE) Comparators A and B					
Input Common Mode Range		–0.2		5.5	V
Input Offset Voltage	I(SENSE) A	–15		15	mV
	I(SENSE) B	+0.4	0.7	+0.9	V
Input Bias Current			–3	–10	μA
Input Offset Current		–3	0	+3	μA
Propagation Delay			150		ns
I_{LIMIT} (A) Trip Point	$V_{PIN\ 3}$ = 5.5V	4.8	5	5.2	V
I(LIM) Comparator					
I_{LIMIT} Trip Point		.95	1.0	1.05	V
Input Bias Current			–2	–10	μA
Propagation Delay			150		ns
Output Section (A and B)					
Output Voltage Low	I_{OUT} = –20mA		0.1	0.4	V
	I_{OUT} = –200mA		1.6	2.2	V
Output Voltage High	I_{OUT} = 20mA	13	13.5		V
	I_{OUT} = 200mA	12	13.4		V
Output Voltage Low in UVLO	I_{OUT} = –1mA, V_{CC} = 8V		0.1	0.8	V
Output Rise/Fall Time	C_L = 1000pF		50		ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 14KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V (note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Under Voltage Lockout					
Start-Up Threshold		15	16	17	V
Shut-Down Threshold		9	10	11	V
V_{REF} Good Threshold			4.4		V
Total Device					
Supply Current	Start-Up, V_{CC} = 14V		.6	1.2	mA
	Operating, T_J = 25°C		25	35	mA

Note 1: This parameter not 100% tested in production but guaranteed by design.
Note 2: V_{CC} is raised above the Start-up Threshold first to activate the IC, then returned to 15V.
Note 3: PWM comparator bias currents are subtracted from this reading.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4819 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $5/R_{SET}$. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where:

$$T_{RAMP} = \frac{C\ (\text{Ramp Valley to Peak})}{I_{SET}}$$

and:

$$T_{DEADTIME} = \frac{C\ (\text{Ramp Valley to Peak})}{(8.4\text{mA} - I_{SET})}$$

The maximum duty cycle of the PWM section can be limited by setting a threshold on pin 7. When the C(T) ramp is above the threshold at pin 7, the PWM output is held off and the PWM flip-flop is set:

$$D_{LIMIT} \cong \frac{D_{OSC} \times (V_{PIN\ 7} - 0.9)}{3.4}$$

Where:

D_{LIMIT} = Desired duty cycle limit
D_{OSC} = Oscillator duty cycle

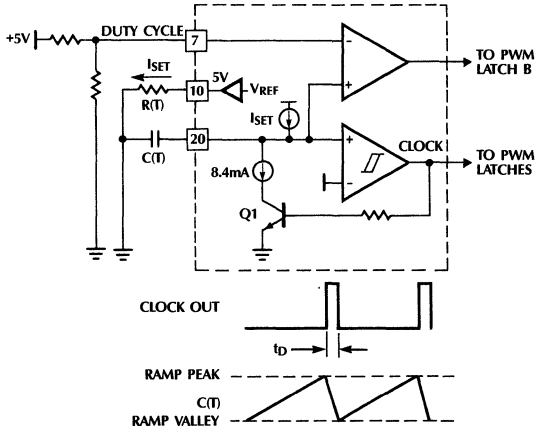


Figure 1. Oscillator Block Diagram

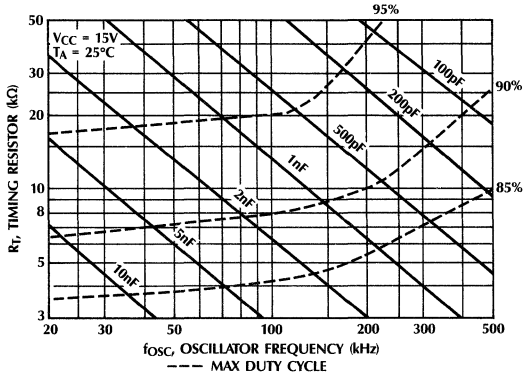


Figure 2. Oscillator Timing Resistance vs. Frequency

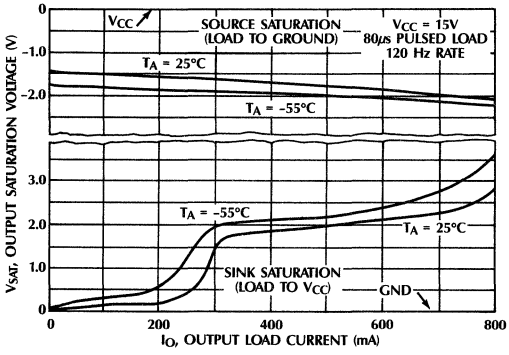


Figure 3. Output Saturation Voltage vs. Output Current

ERROR AMPLIFIER

The ML4819 error amplifier is a high open loop gain, wide bandwidth, amplifier.

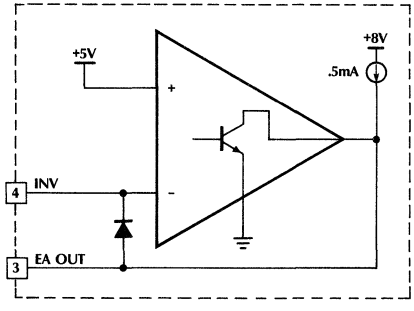


Figure 4. Error Amplifier Configuration

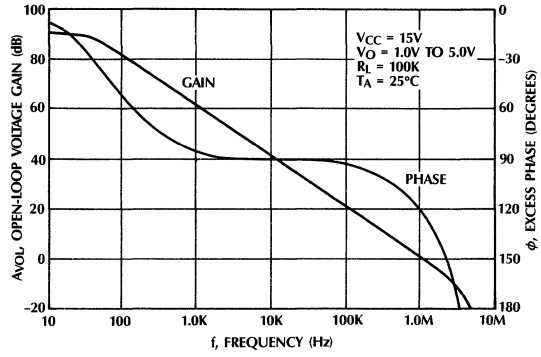


Figure 5. Error Amplifier Open-Loop Gain and Phase vs. Frequency

MULTIPLIER

The ML4819 multiplier is a linear current input multiplier to provide high immunity to the disturbances caused by high power switching. The rectified line input sine wave is converted to a current via a dropping resistor. In this way, small amounts of ground noise produce an insignificant effect on the reference to the PWM comparator.

The output of the multiplier is a current proportional to:

$$I_{OUT} \propto I(SINE) \times I(EA)$$

where I(SINE) is the current in the dropping resistor, and I(EA) is a factor which varies from 0 to 1 proportional to the output of the error amplifier. When the error amplifier is saturated high, the output of the multiplier is approximately equal to the I(SINE) input current.

The multiplier output current is converted into the reference voltage for the PWM comparator through a resistor to ground on the multiplier output (pin 3).

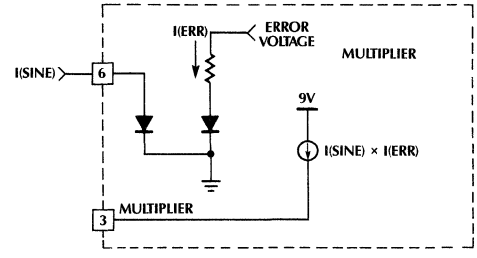


Figure 6. Multiplier Block Diagram

SLOPE COMPENSATION

Slope compensation is accomplished by adding 1/2 of the current flowing out of pin 12 to pin 1 (for the PFC section) and pin 9 (for the PWM section). The amount of slope compensation is equal to ($I_{PIN\ 12}/2$) × R_L where R_L is the impedance to GND on pin 1 or pin 9. Since most of the PWM applications will be limited to 50% duty cycle, slope compensation should not be needed for the PWM section. This can be defeated by using a low impedance load to the current sense on pin 9.

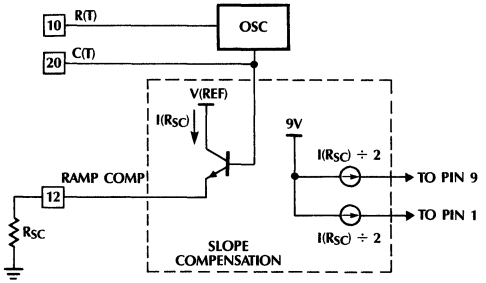


Figure 7. Slope Compensation Circuit

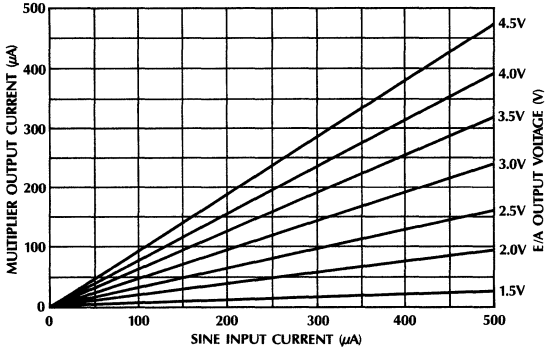


Figure 8. Multiplier Linearity

UNDER VOLTAGE LOCKOUT

On power-up the ML4819 remains in the UVLO condition; output low and quiescent current low. The IC becomes operational when V_{CC} reaches 16V. When V_{CC} drops below 10V, the UVLO condition is imposed. During the UVLO condition, the 5V V_{REF} pin is "off", making it usable as a "flag".

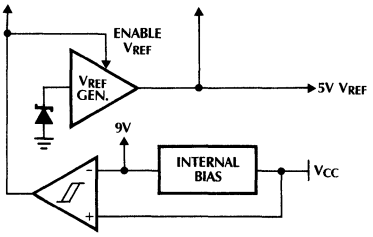


Figure 9. Under-Voltage Lockout Block Diagram

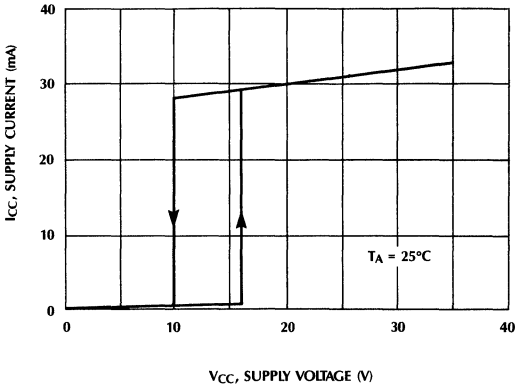


Figure 10a. Total Supply Current vs. Supply Voltage

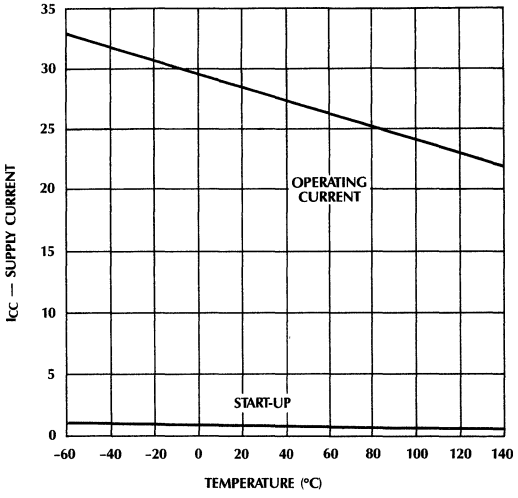


Figure 10b. Total Supply Current (I_{CC}) vs. Temperature

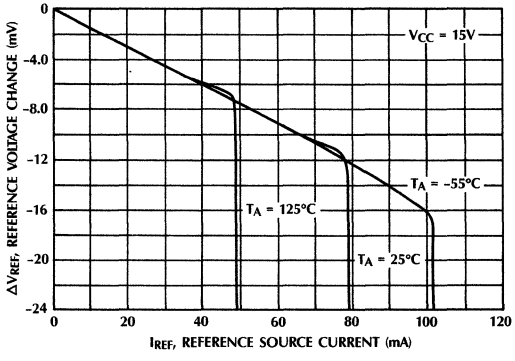


Figure 11. Reference Load Regulation

APPLICATIONS

POWER FACTOR SECTION

The power factor section in the ML4819 is similar to the power factor section in the ML4812 with the exception of the operation of the slope compensation circuit. Please refer to the ML4812 data sheet for more information.

The following calculations refer to figure 12. The component designators in the equations below refer to the following components in figure 12:

R_T = R16, C_T = C6.

INPUT INDUCTOR (L1) SELECTION

The central component in the regulator is the input boost inductor. The value of this inductor controls various critical operational aspects of the regulator. If the value is too low, the input current distortion will be high and will result in low power factor and increased noise at the input. This will require more input filtering. In addition, when the value of the inductor is low the inductor dries out (runs out of current) at low currents. Thus the power factor will decrease at lower power levels and/or higher line voltages. If the inductor value is too high, then for a given operating current the required size of the inductor core will be large and/or the required number of turns will be high. So a balance must be reached between distortion and core size.

One more condition where the inductor can dry out is analyzed below where it is shown to be maximum duty cycle dependent.

For the boost converter at steady state:

$$V_{OUT} = \frac{V_{IN}}{1 - D_{ON}} \quad (1)$$

Where D_{ON} is the duty cycle $[T_{ON}/(T_{ON} + T_{OFF})]$. The input boost inductor will dry out when the following condition is satisfied:

$$V_{IN}(t) < V_{OUT} \times (1 - D_{ON}) \quad (2)$$

or

$$V_{INDRY} = [1 - D_{ON}\,(max)] \times V_{OUT} \quad (3)$$

V_{INDRY}: Voltage where the inductor dries out.
V_{OUT}: Output dc voltage.

Effectively, the above relationship shows that the resetting volt-seconds are more than setting volt-seconds. In energy transfer terms this means that less energy is stored in the inductor during the ON time than it is asked to deliver during the OFF time. The net result is that the inductor dries out.

The recommended maximum duty cycle is 95% at 100KHz to allow time for the input inductor to dump its energy to the output capacitors.

For example:

if: V_{OUT} = 380V and
D_{ON} (max) = 0.95

then substituting in (3) yields V_{INDRY} = 20V. The effect of drying out is an increase in distortion at low voltages.

For a given output power, the instantaneous value of the input current is a function of the input sinusoidal voltage waveform, i.e. as the input voltage sweeps from zero volts to a maximum value equal to its peak so does the current.

The load of the power factor regulator is usually a switching power supply which is essentially a constant power load. As a result, an increase in the input voltage will be offset by a decrease in the input current.

By combining the ideas set forth above, some ground rules can be obtained for the selection and design of the input inductor:

Step 1: Find minimum operating current.

$$I_{IN}(min)_{PEAK} = \frac{1.414 \times P_{IN}(min)}{V_{IN}(max)} \quad (4)$$

V_{IN}(max) = 260V
P_{IN}(min) = 50W
then: $I_{IN}(min)_{PEAK}$ = 0.272A

Step 2: Choose a minimum current at which point the inductor current will be on the verge of drying out. For this example 40% of the peak current found in step 1 was chosen.

then: I_{LDRY} = 100mA

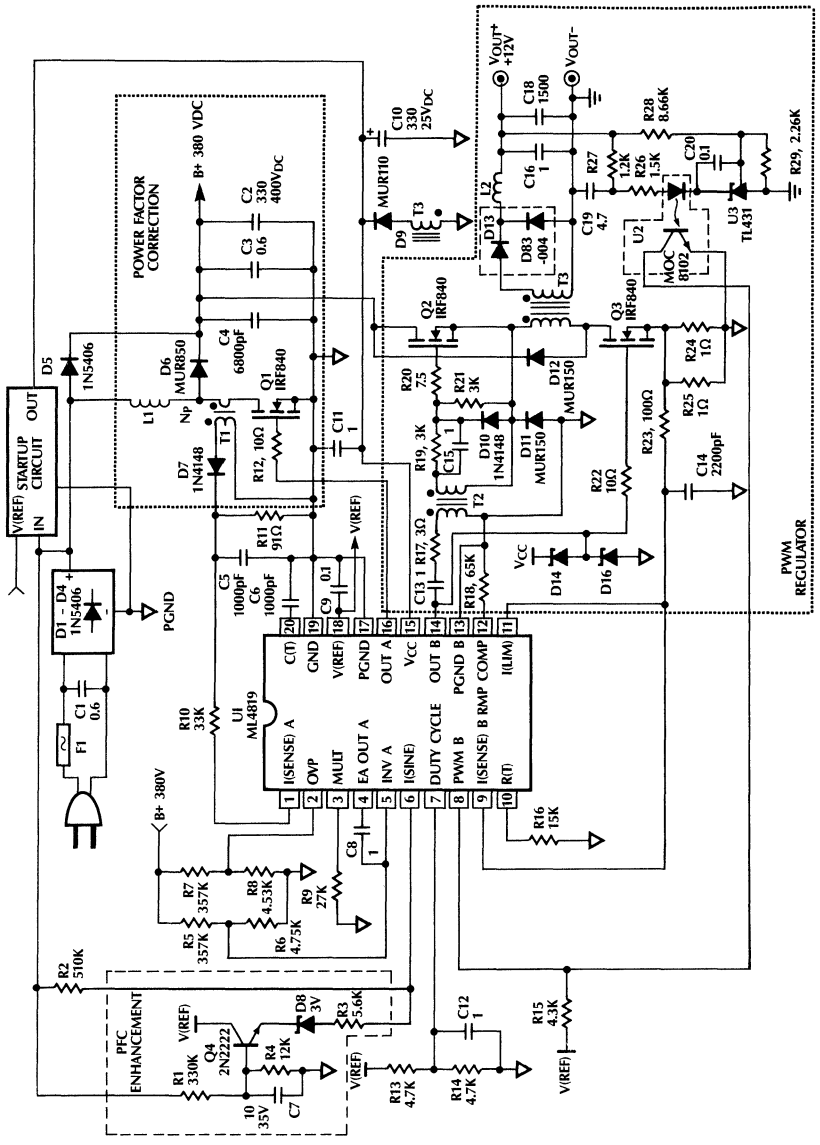


Figure 12. Typical Application, 180W Power Factor Corrected 12V Output Power Supply

Step 3: The value of the inductance can now be found using previously calculated data.

$$L1 = \frac{V_{INDRY} \times D_{ON(max)}}{I_{LDRY} \times f_{OSC}} \quad (5)$$

$$= \frac{20V \times 0.95}{100mA \times 100KHz} = 2mH$$

The inductor can be allowed to decrease in value when the current sweeps from minimum to maximum value. This allows the use of smaller core sizes. The only requirement is that the ramp compensation must be adequate for the lower inductance value of the core so that there is adequate compensation at high current.

Step 4: The presence of the ramp compensation will change the dry out point, but the value found above can be considered a good starting point. Based on the amount of power factor correction the above value of L1 can be optimized after a few iterations.

Gapped Ferrites, Molypermalloy, and Powdered Iron cores are typical choices for core material. The core material selected should have a high saturation point and acceptable losses at the operating frequency.

One ferrite core that is suitable at around 200W is the #4229PL00-3C8 made by Ferroxcube. This ungapped core will require a total gap of 0.180" for this application.

OSCILLATOR COMPONENT SELECTION

The oscillator timing components can be calculated by using the following expression:

$$f_{OSC} = \frac{1.36}{R_T \times C_T} \quad (6)$$

For example:

Step 1: At 100KHz with 95% duty cycle T_{OFF} = 500ns calculate C_T using the following formula:

$$C_T = \frac{T_{OFF} \times I_{DIS}}{V_{OSC}} = 1000pF \quad (7)$$

Step 2: Calculate the required value of the timing resistor.

$$R_T = \frac{1.36}{f_{OSC} \times C_T} = \frac{1.36}{100KHz \times 1000pF} \quad (8)$$

$$= 13.6K\Omega \text{ choose } R_T = 14K\Omega.$$

CURRENT SENSE AND SLOPE (RAMP) COMPENSATION COMPONENT SELECTION

Slope compensation in the ML4819 is provided internally. A current equal to $V_{C(T)}/2(R18)$ is added to I(SENSE) A (pin 1). This is converted to a voltage by R10, adding slope to the sensed current through T1. The amount of slope compensation should be at least 50% of the downslope of the inductor current during the off time as reflected on pin 1. Note that slope compensation is a requirement only if the inductor current is continuous and the duty cycle is more than 50%. The highest inductor downslope is found at the point of inductor discontinuity:

$$\frac{di_L}{dt} = \frac{V_B - V_{IN\ DRY}}{L} = \frac{380V - 20V}{2mH} \quad (9)$$

$$= 0.18\ A/\mu s$$

The downslope as reflected to the input of the PWM comparator is given by:

$$S_{PWM} = \frac{V_B - V_{IN\ DRY}}{L1} \times \frac{R_{11}}{N_C} \quad (10)$$

Where N_C is the turns ratio of the current transformer (T1) used. In general, current transformers simplify the sensing of switch currents especially at high power levels where the use of sense resistors is complicated by the amount of power they have to dissipate. Normally the primary side of the transformer consists of a single turn and the secondary consists of several turns of either enameled magnet wire or insulated wire. The diameter of the ferrite core used in this example is 0.5" (SPANG/Magnetics F41206-TC). The rectifying diode at the output of the current transformer can be a 1N4148 for secondary currents up to 75mA average.

Sense FETs or resistive sensing can also be used to sense the switch current, the sensed signal has to be amplified to the proper level before it is applied to the ML4819.

The value of the ramp compensation (SC_{PWM}) as seen at pin 1 is:

$$SC_{PWM} = \frac{2.5 \times R_9}{R_{16} \times C_6 \times R_{18}} \quad (11)$$

The required value for R_{18} can therefore be found by equating:

$$SC_{PWM} = A_{SC} \times S_{PWM}$$

where A_{SC} is the amount of slope compensation and solving for R_{18}.

The value of R_9 (pin 2) depends on the selection of R_2 (pin 6)

$$R_2 = \frac{V_{IN(max)PEAK}}{I_{SINE(peak)}} = \frac{260 \times 1.414}{0.72mA} = 510K \quad (12)$$

$$R_9 > \frac{V_{CLAMP} \times R_2}{V_{IN(min)PEAK}} = \frac{4.8 \times 510K}{80 \times 1.414} \cong 22K \quad (13)$$

Choose R9 = 27K

The peak of the inductor current can be found approximately by:

$$I_{LPEAK} = \frac{1.414 \times P_{OUT}}{V_{IN(min)RMS}} = \frac{1.414 \times 200}{90} = 3.14A \quad (14)$$

Selection of N_C which depends on the maximum switch current, assume 4A for this example is 80 turns.

$$R_{11} = \frac{V_{CLAMP} \times N_C}{I_{LPEAK}} = \frac{4.8 \times 80}{4} \cong 100\Omega \quad (15)$$

Where R_{11} is the sense resistor, and V_{CLAMP} is the current clamp at the inverting input of the PWM comparator. This clamp is internally set to 5V. In actual application it is a good idea to assume a value less than 5V to avoid unwanted current limiting action due to component tolerances. In this application V_{CLAMP} was chosen as 4.8V.

Having calculated R_{11} the value S_{PWM} and of R_{18} can now be calculated:

$$S_{PWM} = \frac{380V - 20}{2mH} \times \frac{100}{80} = 0.225V/\mu s$$

$$R_{18} = \frac{2.5 \times R_9}{A_{SC} \times S_{PWM} \times R_T \times C_T} \quad (16)$$

$$R_{18} = \frac{2.5 \times 27K}{0.7 \times (.225 \times 10^6) \times 14K \times 1nF} \cong 30K$$

Choose R18 = 33K

The following values were used in the calculation:

R_9 = 27K A_{SC} = 0.7
R_T = 14K C_T = 1nF

VOLTAGE REGULATION COMPONENTS

The values of the voltage regulation loop components are calculated based on the operating output voltage. Note that voltage safety regulations require the use of sense resistors that have adequate voltage rating. As a rule of thumb if 1/4W resistors are available, two of them should be used in series. The input bias current of the error amplifier is approximately 0.5μA, therefore the current available from the voltage sense resistors should be significantly higher than this value. Since two 1/4W resistors have to be used the total power rating is 1/2W. The operating power is set to be 0.4W then with 380V output voltage the value can be calculated as follows:

$$R_5 = (380V)^2/0.4W = 360K \quad (17)$$

Choose two 178K, 1% connected in series.

Then R_6 can be calculated using the formula below:

$$R_6 = \frac{V_{REF} \times R_5}{V_B - V_{REF}} = \frac{5V \times 356K}{380V - 5V} = 4.747K \quad (18)$$

Choose 4.75K, 1%. One more critical component in the voltage regulation loop is the feedback capacitor for the error amplifier. The voltage loop bandwidth should be set such that it rejects the 120Hz ripple which is present at the output. If this ripple is not adequately attenuated it will cause distortion on the input current waveform. Typical bandwidths range anywhere from a few Hertz to 15Hz. The main compromise is between transient response and distortion. The feedback capacitor can be calculated using the following formula:

$$C_8 = \frac{1}{3.142 \times R_5 \times BW} \quad (19)$$

$$C_8 = \frac{1}{3.142 \times 356K \times 2Hz} = 0.44\mu F$$

OVERVOLTAGE PROTECTION (OVP) COMPONENTS

The OVP loop should be set so that there is no interaction with the voltage control loop. Typically it should be set to a level where the power components are safe to operate. Ten to fifteen volts above V_{OUT} seems to be adequate. This sets the maximum transient output voltage to about 395V.

By choosing the high voltage side resistor of the OVP circuit the same way as above i.e. R_7 = 356K then R_8 can be calculated as:

$$R_8 = \frac{V_{REF} \times R_7}{V_{OVP} - V_{REF}} = \frac{5V \times 356K}{395V - 5V} = 4.564K \quad (20)$$

Choose 4.53K, 1%.

Note that R_5, R_6, R_7 and R_8 should be tight tolerance resistors such as 1% or better.

OFF-LINE START-UP AND BIAS SUPPLY GENERATION

The Start-Up Circuit in figure 12 can be either a "bleed resistor" (39KΩ, 2W) or the circuit shown in figure 13. The bleed resistor method offers the advantage of simplicity and lowest cost, but may yield excessive turn-on delay at low line.

When the voltage on pin 15 (V_{CC}) exceeds 16V, the IC starts up. The energy stored on the C10 supplies the IC with running power until the supplemental winding on T3 can provide the power to sustain operation.

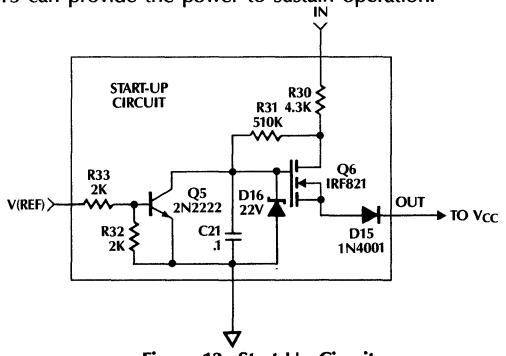


Figure 13. Start-Up Circuit

ENHANCEMENT CIRCUIT

The theory of operation of the power factor enhancement circuit (inside the dotted lines) in Figure 11 is described in APPLICATION NOTE 11 in detail. It improves the power factor and lowers the input current harmonics. Note that the circuit meets the proposed IEC 555 specifications (with the enhancement) on the harmonics with a large margin while correcting the input power factor to better than 0.99 under most steady state operating conditions.

PWM SECTION

The PWM section in figure 12 is a two switch forward converter, shown in figure 14 below for clarity. This fully clamped circuit eliminates the need for very high voltage MOSFETs. Flyback topology is also possible with the ML4819.

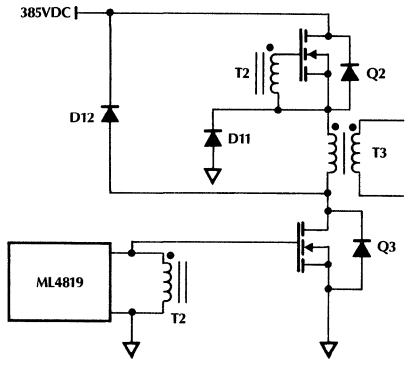


Figure 14. Two-Switch Forward Converter

This regulator (figure 12) uses current mode control. Current is sensed through R24 and filtered for high frequency noise and leading edge transient through R23 and C14. The main regulation loop is through PWM B. The TL431 (U3) in the secondary serves as both the voltage reference and error amplifier, with isolation provided by an opto coupler (U2) providing a current command signal on pin 8. Loop compensation is provided by R29 and C20. The output voltage is set by:

$$V_{OUT} = 2.5 \left(1 + \frac{R_{29}}{R_{28}} \right) \quad (21)$$

The control loop is compensated using standard compensation techniques.

Current is limited to a threshold of 2A (1V on R24). The duty cycle is limited in this circuit to below 50% to prevent transformer (T3) core saturation. The maximum duty cycle limit of 45% is set using a threshold of $V_{REF}/2$ on pin 7.

The circuit in figure 12 can be modified for voltage mode operation by utilizing the slope current which appears on pin 9 as shown in figure 15 below.

The ramp amplitude appearing on pin 9 will be

$$V_R = \frac{I_{R18}}{2} \times R(V) \quad (22)$$

where R_{18} is the slope compensation resistor. Since this circuit operates with a constant input voltage (as supplied by the PFC section) voltage feed-forward is unnecessary.

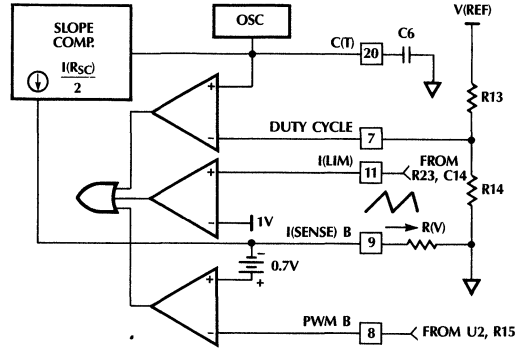


Figure 15. Voltage Mode Configuration

CONSTRUCTION AND LAYOUT TIPS

High frequency power circuits require special care during breadboard construction and layout. Double sided printed circuit boards with ground plane on one side are highly recommended. All critical switching leads (power FET, output diode, IC output and ground leads, bypass capacitors) should be kept as small as possible. This is to minimize both the transmission and pick-up of switching noise.

There are two kinds of noise coupling; inductive and capacitive. As the name implies inductive coupling is due to fast changing (high di/dt) circulating switching currents. The main source is the loop formed by Q1, D6, and C3–C4. Therefore this loop should be as small as possible, and the above capacitors should be good high frequency types.

The second form of noise coupling is due to fast changing voltages (high dv/dt). The main source in this case is the drain of the power FET. The radiated noise in this case can be minimized by insulating the drain of the FET from the heatsink and then tying the heatsink to the source of the FET with a high frequency capacitor.

The IC has two ground pins named PWR GND and Signal GND. These two pins should be connected together with a very short lead at the printed circuit board exit point. In general grounding is very important and ground loops should be avoided. Star grounding schemes are preferred.

Component Values/Bill of Materials for Figure 12

Component	Description
C1, C3	0.6μF, 630V Film (250 VAC)
C2	330μF, 400V Electrolytic
C4	6800pF, 1KV Ceramic
C5, C6	1000pF
C7	10μF, 35V
C8, C11, C13, C15, C16	1μF, Ceramic
C9, C20, C21	0.1μF, Ceramic
C10	1500μF, 25V Electrolytic
C12, C17	1μF, Ceramic
C14	2200pF
C18	1500μF, 16V Electrolytic
C19	4.7μF
D1–D5	1N5406
D6	MUR850
D7, D10	1N4148
D8	3V Zener diode or 4 × 1N4148 in series
D9	MUR110
D11, D12	MUR150
D13	D83-004K
D15	1N4001
D16, D14	1N5818 or 1N5819
F1	5A, 250V, 3AG
L1	2mH, 4A I_{PEAK} Core: Ferroxcube 4229-3C8 150 Turns #24 AWG 0.150" gap
L2	10μH Core: Spang OF 43019 UG00 8 Turns #15AWG gap 0.05"
Q1–Q3	IRF840
Q4, Q5	2N2222
Q6	IRF821
R1	330K
R2, R31	510K
R3	5.6K

Component	Description
R4	12K
R5, R7	357K, 1%
R6	4.75K, 1%
R8	4.53K, 1%
R9	27K
R10, R18	33K
R11	91Ω
R12, R22	10Ω
R13, R14	4.7K
R15	4.3K
R16	15K
R17	3Ω
R20	7.5Ω
R21, R19	3K
R23	100Ω
R24, R25	1Ω
R26	1.5K
R27	1.2K
R28	8.66K, 1%
R29	2.26K, 1%
R30	2K, 1W
R32, R33	2K
T1	Spang F41206-TC or Siemens B64290-K45-X27 or X830 or Ferroxcube 768T188-3C8 N_S = 80, N_P = 1
T2	Same core as T1 $N_S = N_P$ = 15 bifilar
T3	Core: Ferroxcube 4229-3C8 Pri. 44 Turns #18 Litz wire Sec. 4 Turns of copper strip Aux. 2 Turns #24 AWG
U2	MOC8102
U3	TL431

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4819CP	0°C to +70°C	Molded DIP (P20)
ML4819CS	0°C to +70°C	Molded PCC (S20W)

ML4821

Power Factor Controller

GENERAL DESCRIPTION

The ML4821 provides the complete control for a "boost" type power factor correction system using the average current sensing method. Special care has been taken in the design of the ML4821 to increase system noise immunity. The circuit includes a precision reference, multiplier, average current error amplifier, output error amplifier, over-voltage protection comparator, shutdown logic, as well as a high current output. In addition, start-up is simplified by an under-voltage lockout circuit with 7V hysteresis.

In a typical application, the ML4821 controls the average current, adjusting the pulse width of the output to modulate the current so that its shape conforms to the shape of the input voltage. The reference for the current regulator is a product of the sinusoidal line voltage times the output of the error amplifier which is regulating the output DC voltage. Average line voltage compensation is provided in the multiplier to ensure constant loop gain over a wide input voltage range. This compensation includes a special "brown-out" control which reduces output power below 90V RMS input.

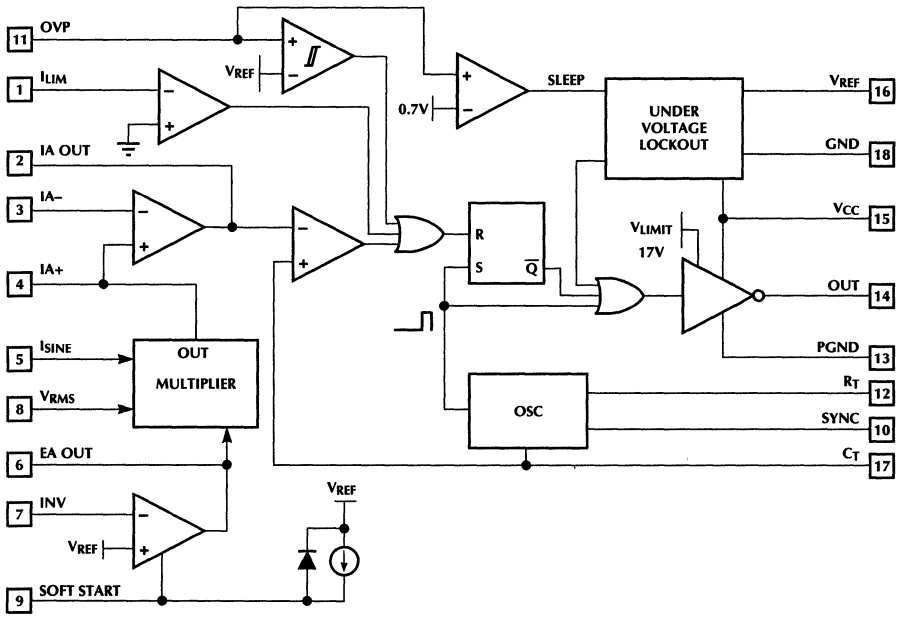
For applications information, Please see Applications Note 16.

The ML4821 uses Micro Linears bipolar array technology which allows for customization of the IC for a user's specific application. Please consult Micro Linear for semi-standard options.

FEATURES

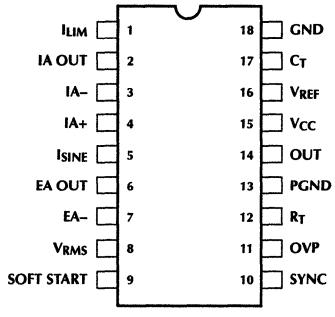
- Average current sensing for lowest possible harmonic distortion
- Average Line compensation with Brown-out control
- Precision buffered 5V Reference (±1%)
- Current Input Multiplier reduces external components and improves noise immunity
- 1A Peak Current Totem-Pole Output Drive
- Over-Voltage comparator eliminates output "runaway" due to load removal
- Wide common mode range in current sense comparators for better noise immunity
- Large oscillator amplitude for better noise immunity
- Output Driver internally limited to 17V
- "Sleep mode" shutdown input

BLOCK DIAGRAM



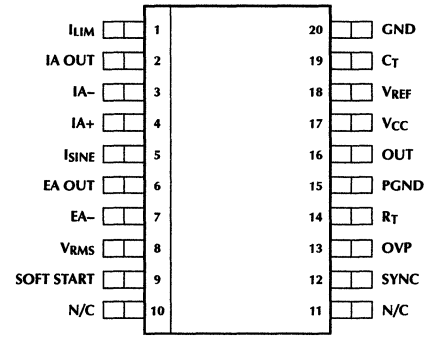
PIN CONNECTION

ML4821
18-Pin DIP



TOP VIEW

ML4821
20-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	I_{LIM}	Peak cycle-by-cycle Current limit input.
2	IA OUT	Output and compensation node of the average current error amplifier.
3	IA–	Inverting input of the average current error amplifier.
4	IA+	Non-Inverting input of the average current error amplifier and output of the multiplier.
5	I_{SINE}	Current Multiplier input.
6	EA OUT	Output of output voltage error amplifier.
7	INV	Inverting input to error amplifier.
8	V_{RMS}	Input for Average Line Voltage compensation
9	SOFT START	Normally connected to Soft Start Capacitor
10	SYNC	Oscillator synchronization input
11	OVP	Inhibits output pulses when the voltage at this pin exceeds 5V. Also, when the voltage at this pin is less than 0.7V, the IC goes into low current shut-down mode.
12	R_T	Timing Resistor for the Oscillator
13	PWR GND	Return for the High Current Totem pole output.
14	OUT	High Current Totem pole output.
15	V_{CC}	Positive Supply for the IC.
16	V_{REF}	Buffered output for the 5V voltage reference.
17	C_T	Timing Capacitor for the Oscillator.
18	GND	Analog signal ground.

ABSOLUTE MAXIMUM RATINGS

Supply Current (I_{CC}) 35mA
Output Current, Source or Sink (pin 14)
DC 1.0A
Output Energy (capacitive load per cycle) 5µJ
Multiplier I_{SINE} Input (pin 5) 1.2mA
Error Amp Source Current (pin 6) 50mA
Oscillator Charge Current 2mA
Analog Inputs (pins 1,3,4, 7,8,9,10,11) ..... –0.3V to 5.5V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP ..... 65°C/W
Plastic SOIC ..... 65°C/W

OPERATING CONDITIONS

Temperature Range
ML4821C ..... 0°C to +70°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 6.2KΩ, C_T = 720pF, T_A = Operating Temperature Range, V_{CC} = 15V (Note 2).

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
OSCILLATOR					
Initial accuracy	T_A = 25°C	90	100	110	KHz
Voltage stability	12V < V_{CC} < 18V		1		%
Temperature stability			2		%
Total Variation	Line, Temperature	85		115	KHz
Ramp Valley to Peak		4.7	5.2	5.6	V
R_T Voltage		4.8	5.0	5.2	V
Discharge Current (pin 12 open)	V_{PIN17} = 2V	7.8	8.4	9.3	mA
Sync Input Threshold		1.5	2.0	3.0	V
REFERENCE SECTION					
Output Voltage	T_A = 25°C, I_O = 1mA	4.95	5.00	5.05	V
Line regulation	12V < V_{CC} < 24V		2	10	mV
Load regulation	1mA < I_O < 20mA		2	15	mV
Temperature stability			.4		%
Total Variation	line, load, temp	4.9		5.1	V
Output Noise Voltage	10Hz to 10KHz		50		µV
Long Term Stability	T_A = 125°C, 1000 hrs, (Note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	–30	–85	–180	mA
VOLTAGE ERROR AMPLIFIER (EA)					
Input Offset Voltage		0		–15	mV
Input Bias Current			–50	–800	nA
Open Loop Gain	2 < V_{PIN6} < 6V	60	75		dB
PSRR	12V < V_{CC} < 24V	70	100		dB
Output Sink Current	V_{PIN6} = 4V, V_{PIN7} = 5.5V	300	500		µA
Output Source Current	V_{PIN6} = 4.0 V, V_{PIN7} = 4.8V	–10	–30		mA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE ERROR AMPLIFIER (EA) (Continued)					
Output High Voltage	I_{PIN6} = –5mA, V_{PIN7} = 4.8V	7.0	7.5		V
Output Low Voltage	I_{PIN6} = 0, V_{PIN7} = 5.5V		0	0.5	V
Unity Gain Bandwidth			1.0		MHz
Soft Start Charge Current	V_{PIN9} = 4V	–22	–38	–50	µA
CURRENT AMPLIFIER (IA)					
Input Offset Voltage		–1.5	0	+3.5	mV
Input Bias Current			–0.15	–1	µA
Input Offset Current				+400	nA
Open Loop Gain	2 < V_{PIN6} < 7V	80	100		dB
PSRR	12V < V_{CC} < 24V	65	85		dB
Output Voltage Low	I_{OL} = 300µA		0	0.5	V
Output Voltage High	I_{OH} = –10mA	7.0	7.5		V
Input Common Mode Range		–0.3		2.5	V
MULTIPLIER					
Gain	V_{PIN7} = 4.8V, V_{PIN8} = 0V V_{PIN7} = 4.8V, V_{PIN8} = 1.75V V_{PIN7} = 4.8V, V_{PIN8} = 2.6V V_{PIN7} = 4.8V, V_{PIN8} = 5.2V	0.75 3.1 1.25 0.22	1.2 3.88 1.75 0.38	1.3 4.45 2.15 0.50	
Output Current	V_{PIN7} = 5.2V, V_{PIN8} = 5.2V		–2	–4	µA
Output Current Limit	V_{PIN7} = 4.8V, I_{PIN5} = 500mA, V_{PIN8} = 1.75V	360	395	420	µA
I_{LIM} COMPARATOR					
Input Offset Voltage				+15	mV
Input Bias Current			–100	–200	µA
OVP COMPARATOR					
Input Offset Voltage	Output Off	–25		5	mV
Hysteresis	Output On	85	105	130	mV
Input Bias Current			–0.3	–3	µA
Propagation Delay			150		ns
Shutdown Threshold		0.4	0.7	1.0	V
PWM COMPARATOR: I_{SENSE}					
Input Common Mode Range		0		8	V
Propagation Delay			150		ns

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
OUTPUT SECTION					
Output Voltage Low	I_{OUT} = 20mA I_{OUT} = 200mA		0.1 1.6	0.4 2.4	V V
Output Voltage High	I_{OUT} = –20mA I_{OUT} = –200mA	13 12	13.5 13.4		V V
Output Voltage Low in UVLO	I_{OUT} = –5mA, V_{CC} = 8V		0.1	0.8	V
Output Rise/Fall Time	C_L = 1000pF		50		ns
UNDER-VOLTAGE LOCKOUT					
Start-up Threshold		14.5		16.5	V
Shut-Down Threshold		8.5		10.5	V
V_{REF} Good Threshold			4.4		V
TOTAL DEVICE					
Supply Current	Start-up, V_{CC} = 14V, T_A = 25°C Operating, T_A = 25°C		0.6 26	1.2 32	mA mA
Internal Shunt Zener Voltage	I_{CC} = 35mA	25	27	35	V

Note 1. This parameter not 100% tested in production but guaranteed by design.
Note 2: V_{CC} is raised above the Start-up Threshold first to activate the IC, then returned to 15V

Note 3: Multiplier gain is defined as: $\frac{I_{OUT\,PIN4}}{I_{INPIN6}}$

7

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4821 oscillator charges the external capacitor (C_T) with a current equal to $2.5/R_T$. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold through Q1.

The Oscillator period can be described by the following relationship:

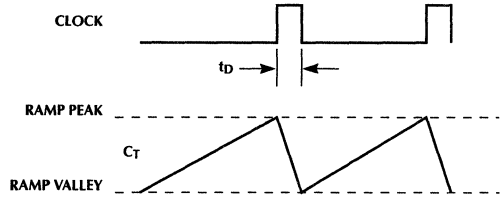
$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where:

$$T_{RAMP} = C(\text{Ramp Valley to Peak}) \div (I_{RT}/2)$$

and:

$$T_{DEADTIME} = C(\text{Ramp Valley to Pk}) \div (8.4mA - I_{RT}/2)$$



The ML4821 oscillator includes a SYNC input for synchronizing to an external frequency source. A positive pulse on this pin of 2V (typ) resets the oscillators comparator and initiates a discharge cycle for C_T. The R_T and C_T component values which set the ML4821 oscillator frequency should be selected to produce a lower frequency than the external frequency source.

ERROR AND CURRENT AMPLIFIERS

The ML4821 error amplifier is a high open loop gain, wide bandwidth, amplifier with a class A output. The soft start circuit controls the input to the error amplifier for closed loop soft start operation.

The current amplifier (IA) is similar to the error amplifier but is designed for very low offsets to allow the selection of a low value resistor for R_{SENSE}.

OUTPUT DRIVER STAGE

The ML4821 Output Driver is a 1A peak output high speed totem pole circuit designed to quickly drive capacitive loads, such as power MOSFET gates. The driver circuit's output voltage is internally limited to 17V.

MULTIPLIER

The ML4821 multiplier is a linear current input multiplier which provides high immunity to the disturbances caused by high power switching. The rectified line input sine wave is converted to a current via a dropping resistor. In this way, small amounts of ground noise produce an insignificant effect on the reference to the PWM comparator.

The output of the multiplier is a current which appears on pin 4 to form the reference for the current error amplifier and is given as:

$$I_{MUL} = K \times I_{SINE} \times (V_{EA} - 0.8)$$

where:

I_{SINE} is the current in the dropping resistor, V_{EA} is the output of the error amplifier and K is a constant determined by the V(RMS) input on pin 8. K assumes a higher value for the range from 90 to 170V than in the range above 170V.

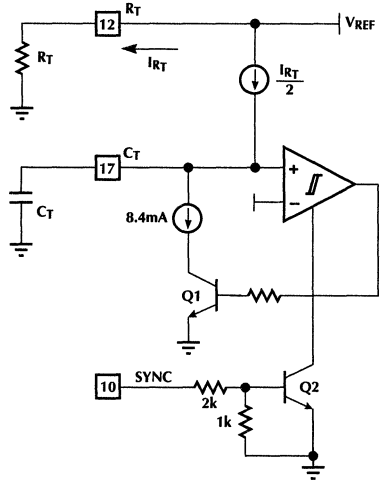


Figure 1. Osccillator Block Diagram.

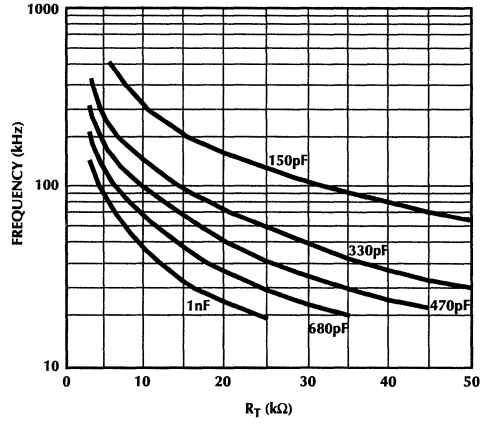


Figure 2. Oscillator Timing Resistance vs. Frequency.

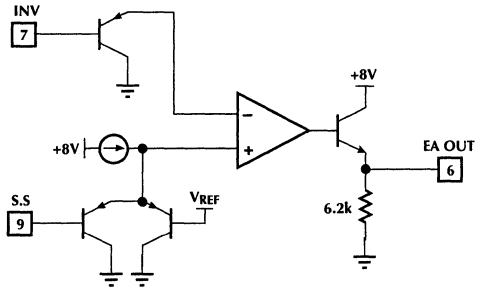


Figure 3. Error and Current Amplifier Configuration

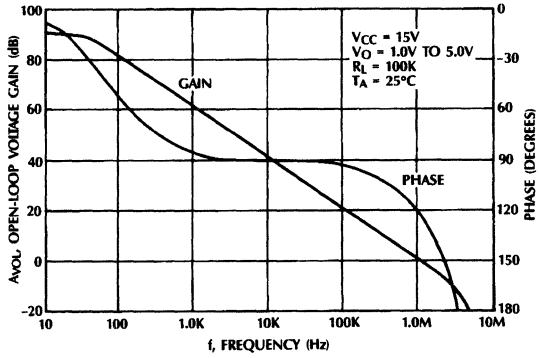


Figure 4. Error Amplifier Open-loop Gain and Phase vs. Frequency.

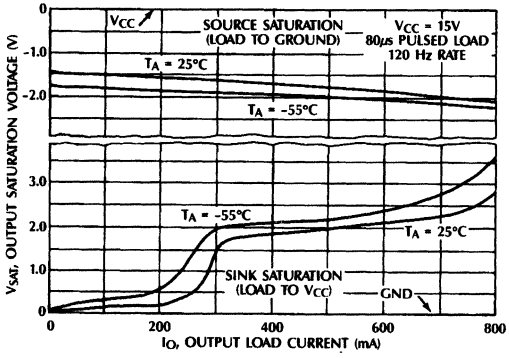


Figure 5. Output Saturation Voltage vs. Output Current.

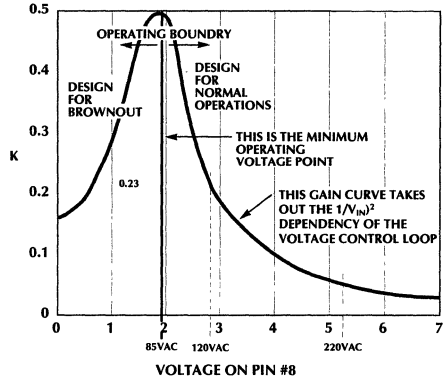


Figure 6. K-factor. Gain adjustor gain with respect to the voltage at pin #8.

The output current of the multiplier is limited to:

$$I_{MUL(MAX)} = \frac{2.5}{R_T}$$

This sets the system current limit.The multiplier output current is converted into the reference voltage for the current (IA) amplifier through a resistor to ground on pin 4, the multiplier output.

Figure 6 shows the gain adjustor (K) with respect to the voltage at pin #8. The curve has been separated in two parts. The right hand part is for operation under normal conditions in the voltage range from minimum line voltage to maximum line voltage (90VAC to 260VAC). 85VAC on the curve has been chosen to account for tolerances. Under normal operating conditions as input voltage decreases the gain increases compensating for the drop in the loop gain.

Under brownout conditions (below 85VAC) the gain decreases to limit the amount of current that is drawn from the line thus preventing an overload condition. This is a very useful feature since in many cases the load for a PFC is a constant power load. The input current has to go high to compensate for a drop in the input voltage.

UNDER VOLTAGE LOCKOUT, OVP AND CURRENT LIMIT

On power-up the ML4821 remains in the UVLO condition; output low and quiescent current low. The IC becomes operational when Vcc reaches 16V. When VCC drops below 9V, the UVLO condition is imposed. During the UVLO condition, the 5V Vref pin is "off", making it usable as a "flag" for starting up a down-stream PWM converter.

OVP, SHUTDOWN, AND IC BIAS

When the input to the OVP comparator exceeds V_{REF}, the output of the ML4821 is inhibited. The OVP input also functions as a "sleep" input, putting the IC into the low quiescent UVLO state when the OVP pin is pulled below 0.7V.

OFF-LINE START-UP AND BIAS SUPPLY GENERATION

The circuit in Figure 11 below supplies V_{CC} power to the ML4821. Start-up current is delivered via R10. The IC starts when pin 15 reaches 15.5V. After that time running power is delivered through the tap on L1. The configuration shown delivers a voltage proportional to VOUT.

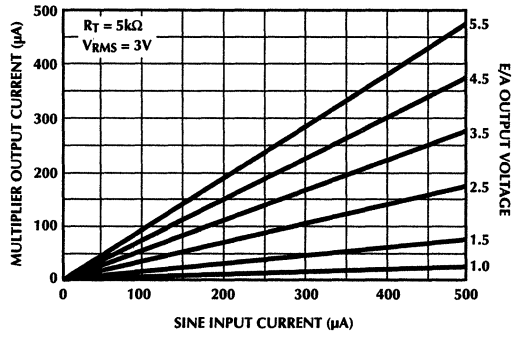


Figure 7. Multiplier Linearity.

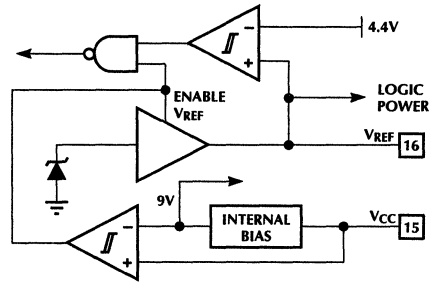


Figure 8. Under-Voltage Lockout Block Diagram.

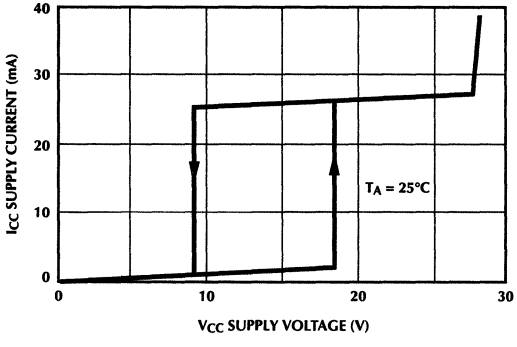


Figure 9. Total Supply Current vs. Supply Voltage.

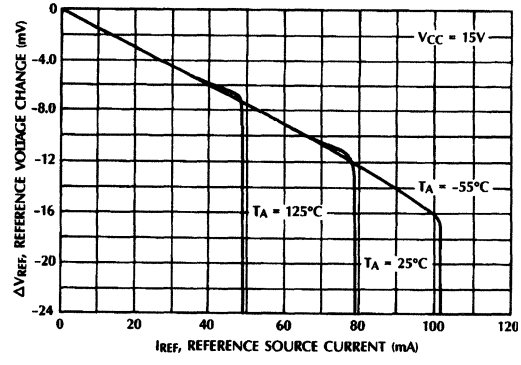


Figure 10. Reference Load Regulation.

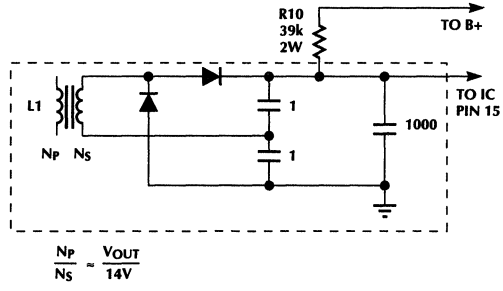


Figure 11. Bias and Start-up Circuit.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4821CP	0°C to +70°C	18-Pin Molded DIP (P18)
ML4821CS	0°C to +70°C	18-Pin Molded SOIC (S18W)

Note: Other packages and temperature ranges can be made available on request. Contact your local Micro Linear Representative for more information.

ML4821EVAL

Average Current PFC Controller Evaluation Kit

GENERAL DESCRIPTION

The ML4821EVAL kit provides a convenient vehicle to evaluate the ML4821 average current sense power factor correction control IC. It contains all of the necessary documentation with the evaluation board and key components to quickly evaluate the application circuit. The board is designed for a 200W universal input PFC circuit. However power components can be replaced for higher or lower power applications.

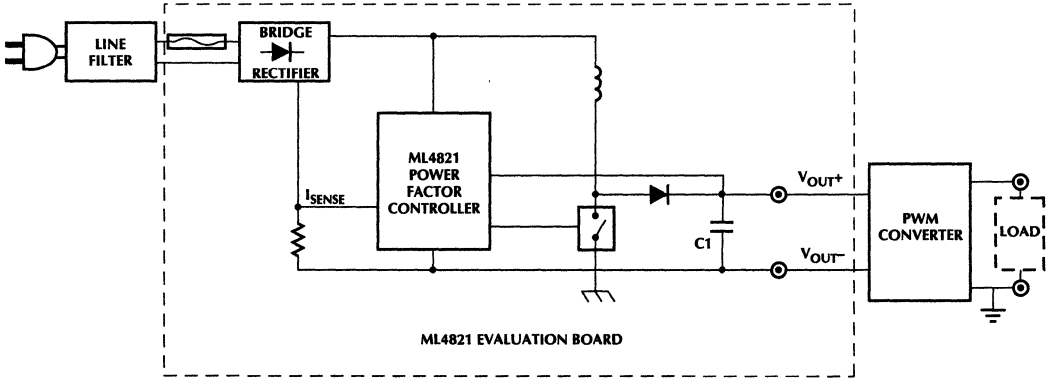
KIT COMPONENTS

- User's Guide
- ML4821 Datasheet
- Application Note 16
- ML4861 Sample
- Evaluation Board
- Key Power Semiconductor Components
- Powder Iron Toroidal Inductor
- Input and output filter capacitors
- Heatsinks

FEATURES

- Harmonic currents well below proposed IEC555-2 limits.
- Power Factor >> .99
- THD < 5%
- Universal Input Range (85Vac to 256Vac)
- 380V output at 200W.
- Efficiency as high as 94%.
- Auxiliary supply from additional inductor winding.
- OVP protection.

BLOCK DIAGRAM



High Frequency Power Supply Controller

GENERAL DESCRIPTION

The ML4823 High Frequency PWM Controller is an IC controller optimized for use in Switch Mode Power Supply designs running at frequencies to 1MHz. Propagation delays are minimal through the comparators and logic for reliable high frequency operation while slew rate and bandwidth are maximized on the error amplifier. This controller is designed for single-ended applications using voltage or current mode and provides for input voltage feed forward.

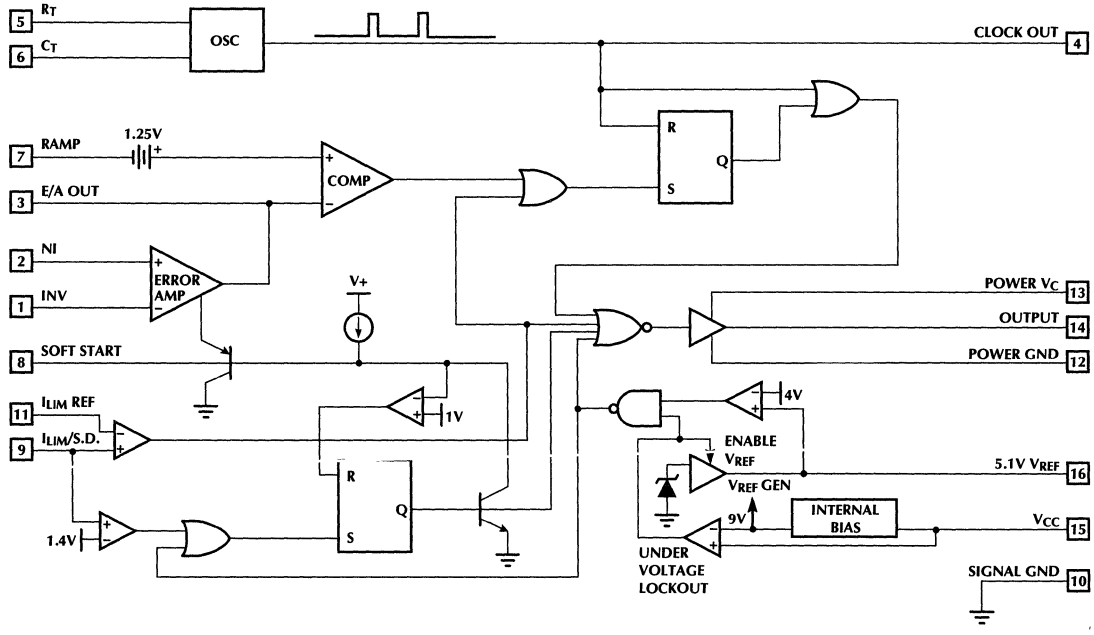
A 1V threshold current limit comparator provides cycle-by-cycle current limit and exceeding a 1.4V threshold initiates a soft-start cycle. The soft start pin doubles as a maximum duty cycle clamp. All logic is fully latched to provide jitter-free operation and prevent multiple pulsing. An under-voltage lockout circuit with 800mV of hysteresis assures low startup current and drives the outputs low during fault conditions.

This controller is an improved second source for the UC1823 controller, however the ML4823 includes features not found on the 1823. These features are set in *Italics.*

FEATURES

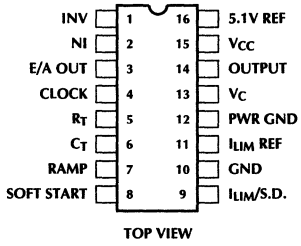
- Practical Operation at Switching Frequencies to 1.0MHz
- High Current (2A peak) Totem Pole Output
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start and Max. Duty Cycle Control
- Under Voltage Lockout with Hysteresis
- 5.1V, ±1% Trimmed Bandgap Reference
- Low Start-up Current (1.1mA)
- Pin Compatible Improved Replacement for UC1823
- *Fast Shut Down Path from Current Limit to Output*
- *Soft Start Latch Ensures Full Soft Start Cycle*
- *Outputs Pull Low for Undervoltage Lockout*

BLOCK DIAGRAM



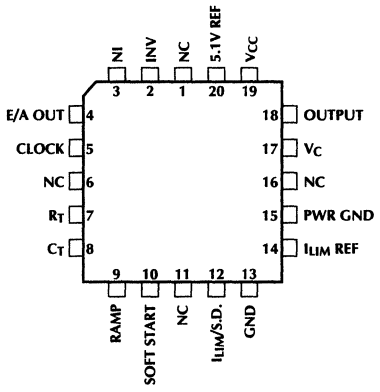
PIN CONFIGURATION

ML4823
16-PIN DIP



TOP VIEW

ML4823
20-PIN PCC



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	INV	Inverting input to error amp.
2	NI	Non-inverting input to error amp.
3	E/A OUT	Output of error amplifier and input to main comparator.
4	CLOCK	Oscillator output.
5	R_T	Timing Resistor for Oscillator — sets charging current for oscillator timing capacitor (pin 6).
6	C_T	Timing Capacitor for Oscillator.
7	RAMP	Non-inverting input to main comparator. Connected to C_T for Voltage Mode operation or to current sense resistor for current mode.
8	SOFT START	Normally connected to Soft Start Capacitor.
9	I_{LIM}/S.D.	Current limit sense pin. Normally connected to current sense resistor.
10	GND	Analog Signal Ground.
11	I_{LIM} REF	Reference input for cycle-by-cycle current limit comparator.
12	PWR GND	Return for the High Current Totem pole outputs.
13	V_C	Positive Supply for the High Current Totem pole outputs.
14	OUT B	High Current Totem pole output.
15	V_{CC}	Positive Supply for the IC.
16	5.1V REF	Buffered output for the 5.1V voltage reference.

7

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pins 15, 13) 30V
Output Current, Source or Sink (pins 11, 14)
DC 0.5A
Pulse (0.5µs) 2.0A
Analog Inputs
(Pins 1, 2, 7, 8, 9) ..... –0.3V to 6V
Clock Output Current (Pin 4) ..... –5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... –5mA
Junction Temperature
ML4823M ..... 150°C
ML4823I, ML4823C ..... 125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C

Thermal Resistance (θ_{JA})
Plastic DIP ..... 65°C/W
Ceramic DIP ..... 65°C/W
Plastic Chip Carrier (PCC) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range
ML4823M ..... –55°C to +125°C
ML4823I ..... –40°C to +85°C
ML4823C ..... 0°C to +70°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial Accuracy	T_J = 25°C, (Note 1)	360	400	440	KHz
Voltage Stability	10V < V_{CC} < 30V, (Note 1)		0.2	2	%
Temperature Stability	(Note 1)		5		%
Total Variation	Line, Temp, (Note 1)	340		460	KHz
Clock Out High		3.9	4.5		V
Clock Out Low			2.3	2.9	V
Ramp Peak	(Note 1)	2.6	2.8	3.0	V
Ramp Valley	(Note 1)	0.7	1.0	1.25	V
Ramp Valley to Peak	(Note 1)	1.6	1.8	2.0	V
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1mA	5.05	5.10	5.15	V
Line Regulation	10V < V_{CC} < 30V		2	20	mV
Load Regulation	1mA < I_O < 10mA		5	20	mV
Temperature Stability	–55°C < T_J < 150°C, (Note 1)		0.2	0.4	%
Total Variation	Line, load, temp. (Note 1)	5.00		5.20	V
Output Noise Voltage	10Hz to 10KHz (Note 1)		50		µV
Long Term Stability	T_J = 125°C, 1000 hrs, (Note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	–15	–50	–100	mA
Error Amplifier Section					
Input Offset Voltage	Operating Temperature Range			±15	mV
Input Bias Current			0.6	3	µA
Input Offset Current			0.1	1	µA
Open Loop Gain	1 < V_O < 4V	60	95		dB

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1nF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section (Continued)					
CMRR	1.5 < V_{CC} < 5.5V Operating Temperature Range	75	95		dB
PSRR	10 < V_{CC} <30V Operting Temperature Range	85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	–0.5	–1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = –0.5mA	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth	(Note 1)	3	5.5		MHz
Slew Rate	(Note 1)	6	12		V/µs
PWM Comparator Section					
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		–1	–5	µA
Duty Cycle Range		0		80	%
Pin 3 Zero DC Threshold	V_{PIN7} = 0V	1.1	1.25		V
Delay to Output	(Note 1)		50	80	ns
Soft-Start Section					
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			mA
Current Limit/Shutdown Section					
Pin 9 Bias Current	0V < V_{PIN9} < 4V			±10	µA
Current Limit Offset	$V_{PIN\ 11}$ = 1.1V	0		15	mV
Pin 11 Common Mode Range		1.0		1.25	V
Shutdown Threshold		1.25	1.40	1.55	V
Delay to Output	(Note 1)		50	80	ns
Output Section					
Output Low Level	I_{OUT} = 20mA		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2	V
Output High Level	I_{OUT} = –20mA	13.0	13.5		V
	I_{OUT} = –200mA	12.0	13.0		V
Collector Leakage	V_C = 30V		100	500	µA
Rise/Fall Time	C_L = 1000PF, (Note 1)		30	60	ns
Under-Voltage Lockout Section					
Start Threshold		8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	V
Supply Current					
Start Up Current	V_{CC} = 8V		1.1	2.5	mA
I_{CC}	$V_{PIN\ 1, 7, 9}$ = 0V $V_{PIN\ 2}$ = 1V		22	33	mA

Note 1: This parameter not 100% tested in production but guaranteed by design.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4823 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $3/R_{SET}$. When the capacitor voltage reaches the upper threshold (Ramp Peak), the comparator changes state and the capacitor discharges to the lower threshold (Ramp Valley) through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where: $T_{RAMP} = C$ (Ramp Valley to Peak)$/I_{SET}$

and: $T_{DEADTIME} = C$ (Ramp Valley to Peak)$/I_{Q1}$

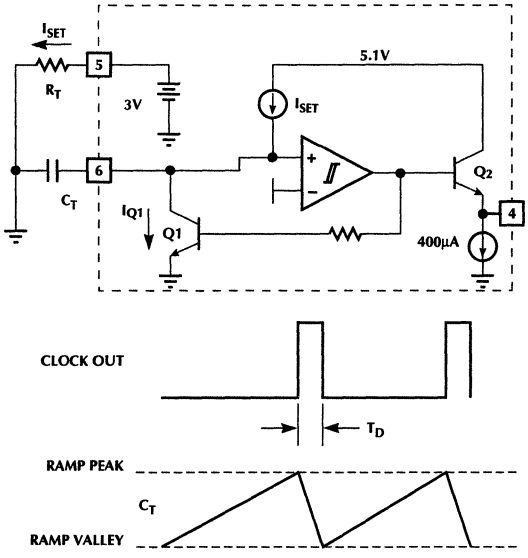


Figure 1. Oscillator Block Diagram

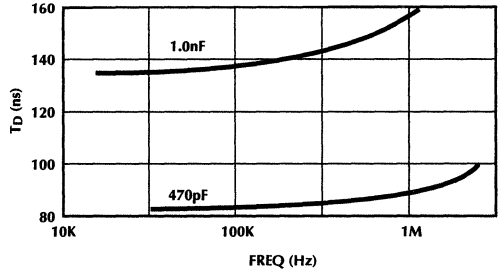


Figure 3. Oscillator Deadtime vs Frequency

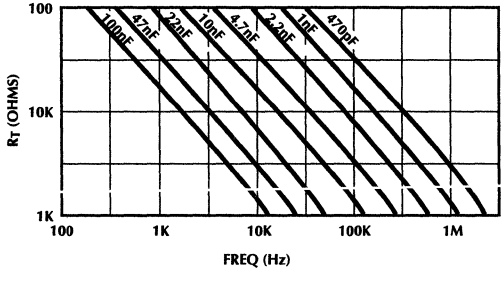


Figure 2. Oscillator Timing Resistance vs Frequency

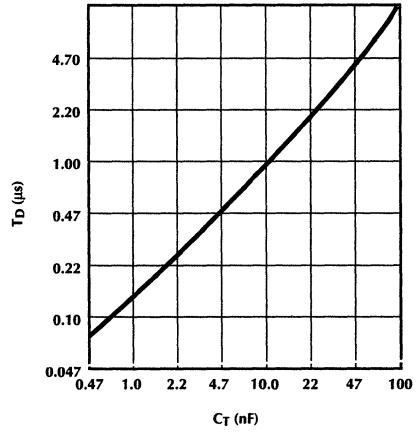


Figure 4. Oscillator Deadtime vs C_T ($3K\Omega \leq R_T \leq 100K\Omega$)

ERROR AMPLIFIER

The ML4823 error amplifier is a 5.5MHz bandwidth 12V/µs slew rate op-amp with provision for limiting the positive output voltage swing (Output Inhibit line) for ease in implementing the soft start function.

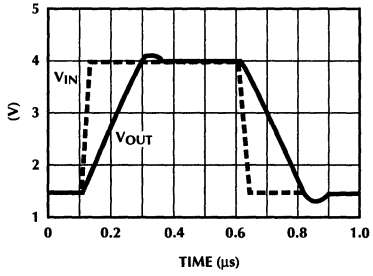


Figure 5. Unity Gain Slew Rate

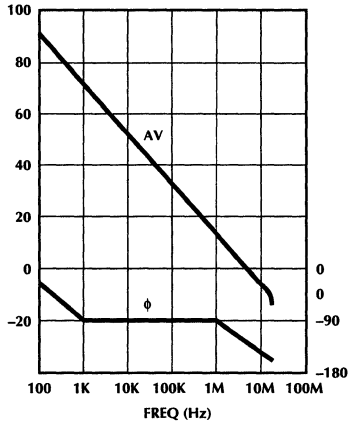


Figure 6. Open Loop Frequency Response

OUTPUT DRIVER STAGE

The ML4823 Output Driver is a 2A peak output high speed totem pole circuit designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors.

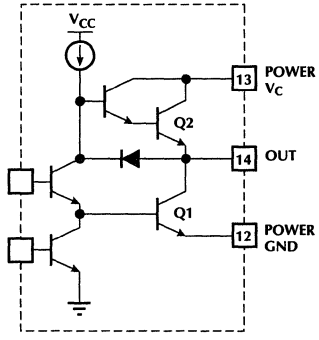


Figure 7. Simplified Schematic

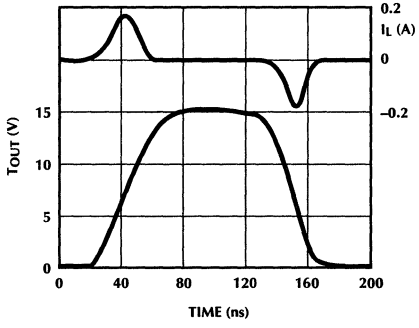


Figure 9. Rise/Fall Time (C_L = 1000pF)

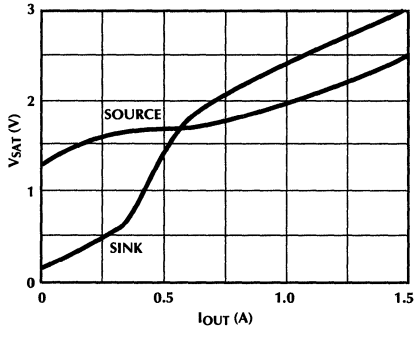


Figure 8. Saturation Curves

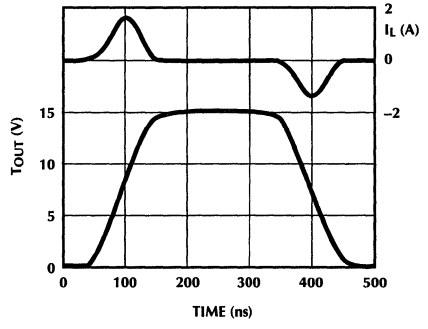


Figure 10 Rise/Fall Time (C_L = 10,000pF)

SOFT START AND CURRENT LIMIT

The ML4823 employs two current limits. When the voltage at pin 9 exceeds the I_{LIM} REF threshold on pin 11, the outputs are immediately shut off and the cycle is terminated for the remainder of the oscillator period by resetting the RS flip flop.

If the output current is rising quickly (usually due to transformer saturation) such that the voltage on pin 9 reaches 1.4V before the outputs have turned off, a soft start cycle is initiated. The soft start capacitor (pin 8) is discharged and outputs are held "off" until the voltage at pin 8 reaches 1V, ensuring a complete soft start cycle. The duty cycle on start up is limited by limiting the output voltage of the error amplifier voltage to the voltage at pin 8.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4823CP	0°C to +70°C	Molded DIP (P16)
ML4823CQ	0°C to +70°C	Molded PCC (Q20)
ML4823CS	0°C to +70°C	Molded SOIC (S16W)
ML4823IP	–40°C to +85°C	Molded DIP (P16)
ML4823IQ	–40°C to +85°C	Molded PCC (Q20)
ML4823IS	–40°C to +85°C	Molded SOIC (S16W)
ML4823MJ	–55°C to +125°C	Hermetic DIP (J16)

ML4824

Power Factor and PWM Combo

GENERAL DESCRIPTION

The ML4824 is a complete controller for a power factor corrected, switched mode power supply. Power Factor Correction results in smaller, lower cost bulk capacitors, reduces power line loading and the stress on switching FETs, and results in a power supply that fully complies with IEC555-2 specifications. Contained in the ML4824 are circuits for the implementation of a leading edge, average current mode "boost" type power factor correction and a trailing edge, synchronized current or voltage mode pulse width modulator (PWM).

The ML4824 comes in two versions; the ML4824XP-1 ($f_{PWM} = f_{PFC}$) and the ML4824XP-2 ($f_{PWM} = 2f_{PFC}$). Doubling the switching frequency of the PWM allows the user to design with a smaller output inductor and capacitor.

An over-voltage comparator is configured to shut-down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting and input voltage brown-out protection.

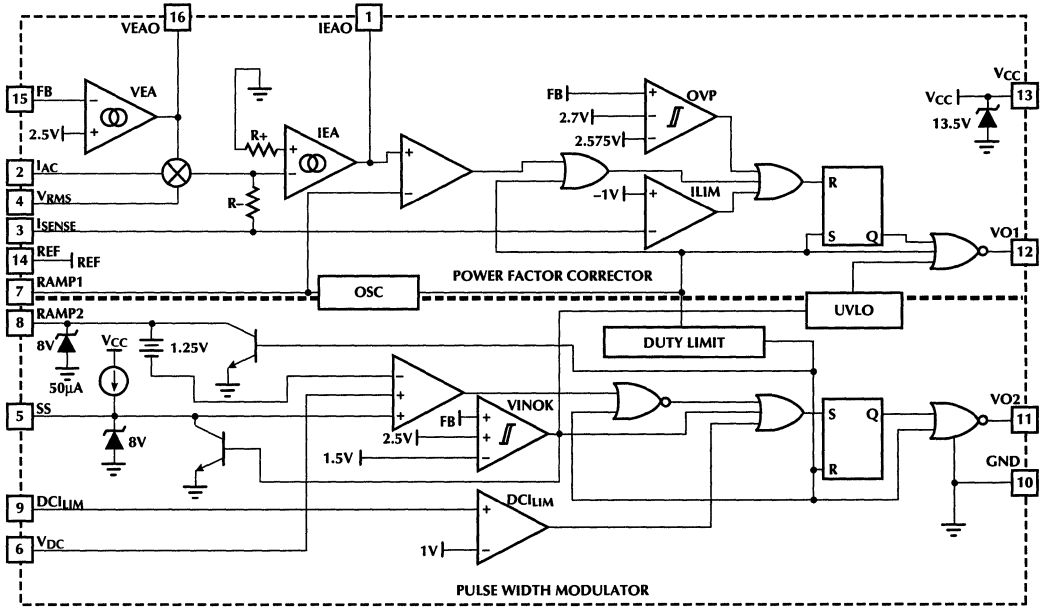
The PWM section can be operated in current mode or voltage mode and includes a precision duty cycle limit to prevent transformer saturation.

When a brown-out occurs, the VINOK comparator shuts down both the PFC and the PWM. A soft-start of the PWM follows with the return of normal line power.

FEATURES

- Internally Synchronized PFC and PWM in one IC
- Low Total Harmonic Distortion
- Average Current Sensing, Continuous Boost, Leading Edge PFC
- High Efficiency, Trailing Edge PWM
- Current Mode or Voltage Mode PWM
- Average Line Voltage Compensation with Brown-Out Control (Universal Input)
- PFC Over-Voltage Comparator Eliminates Output "Runaway" Due to Load Removal
- Current Fed Multiplier to Improve Noise Immunity
- Simplified Compensation Scheme
- Overvoltage Protection, UVLO, and Soft Start

BLOCK DIAGRAM



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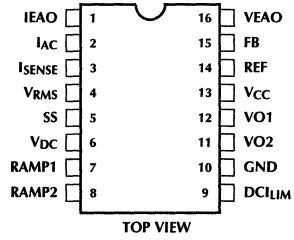
PIN CONFIGURATION

ML4824
16-Pin DIP (P16)
16-Pin SOIC (S16W)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	IEAO	PFC transconductance current error amplifier output.
2	I_{AC}	PFC multiplier reference input.
3	I_{SENSE}	Current sense input to the PFC current limit comparator.
4	V_{RMS}	Input for PFC RMS line voltage compensation.
5	SS	PWM soft start (capacitor).
6	V_{DC}	PWM voltage feedback input.
7	RAMP1	Oscillator timing node; timing set by R_TC_T.
8	RAMP2	Current mode; current sense input. Voltage mode; input for PFC output (feed forward ramp).
9	DCI_{LIM}	PWM current limit.
10	GND	Ground.
11	VO2	PWM driver output.
12	VO1	PFC driver output.
13	V_{CC}	Positive supply (with shunt regulator).
14	REF	Buffered output for the 7.5V voltage reference.
15	FB	PFC transconductance voltage error amplifier input.
16	VEAO	PFC transconductance voltage error amplifier output.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 55mA
Peak Output Current, Source or Sink
(pins 11 & 12) 0.5A
Output Energy (capacitive load per cycle) 1.5mJ
Multiplier I_{AC} Input (pin 2) 10mA
Analog Inputs (pins 4, 6, 9 & 15) ..... –0.3V to V_{CC} – 2V
Pin 3 input voltage ..... –3V to +5V

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP ..... 80°C/W
Plastic SOIC ..... 105°C/W

OPERATING CONDITIONS

Temperature Range
ML4824C ..... 0°C to 70°C
ML4824I ..... –40°C to +85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 52.3kΩ, C_T = 470pF, T_J = Junction Operating Temperature Range, I_{CC} = 25mA

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Amplifiers (pins 1, 3, 15, 16)					
Transconductance, gm_V	$V_{NON-INV} = V_{INV}$ (Note 1)	30	85	140	μ℧
Transconductance, gm_I	$V_{NON-INV} = V_{INV}$ (Note 1)	130	195	335	μ℧
Input Offset Voltage$_V$			±3.0	±15.0	mV
Input Offset Voltage$_I$			±3.0	±15.0	mV
Input Bias Current			–0.3	–1.0	μA
Open Loop Gain		60	75		dB
PSRR	$V_{CCZ} – 3V < V_{CC} < V_{CCZ} – 0.5V$	60	75		dB
Input Voltage Range	Pin 15 (Note 3)	0		7	V
	Pin 3 (Note 3)	–1.5		2	V
Output Low			0.65	1	V
Output High		6.0	6.7		V
Source Current	$\Delta V_{IN} = ±0.5V$, $V_{OUT} = 6V$		–80	–40	μA
Sink Current	$\Delta V_{IN} = ±0.5V$, $V_{OUT} = 1.5V$	40	80		μA
Comparators (pins 1, 3, 5, 6, 15)					
OVP Threshold		2.6	2.7	2.8	V
OVP Hysteresis		80	115	150	mV
ILIM Threshold		–0.80	–1.0	–1.15	V
ILIM Delay to Output	(Note 3)		150	300	ns
DCI_{LIM} Threshold		0.90	1.0	1.10	V
DCI_{LIM} Delay to Output	(Note 3)		150	300	ns
VINOK Threshold		2.4	2.5	2.6	V
VINOK Hysteresis		0.8	1.0	1.2	V
Input Bias Current			±0.3	±1	μA

7

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Multiplier					
Gain (Note 2)	I_{PIN2} = 100µA, V_{PIN4} = 0V, V_{PIN15} = 0V	0.36	0.51	0.66	
	I_{PIN2} = 50µA, V_{PIN4} = 1.2V, V_{PIN15} = 0V	1.20	1.72	2.24	
	I_{PIN2} = 50µA, V_{PIN4} = 1.8V, V_{PIN15} = 0V	0.55	0.78	1.01	
	I_{PIN2} = 100µA, V_{PIN4} = 3.3V, V_{PIN15} = 0V	0.14	0.20	0.26	
Bandwidth	I_{AC} = 250µA		10		MHz
Multiplier Output Voltage	V_{PIN15} = 0V, V_{PIN5} = 1.15V I_{PIN2} = 250µA	0.72	0.8	0.88	V
Oscillator					
Initial Accuracy	T_A = 25°C	71	76	81	kHz
Voltage Stability	V_{CCZ} – 3V < V_{CC} < V_{CCZ} – 0.5V		1		%
Temperature Stability	Over operating temp. range		2		%
Total Variation	Line, temp.	68		84	kHz
Ramp Valley to Peak Voltage			2.5		V
Dead Time	PFC only	270	370	470	ns
C_T Discharge Current	V_{PIN8} = 0V, V_{PIN7} = 2.5V	4.5	7.5	9.5	mA
Reference					
Output Voltage	T_A = 25°C, I_O = 1mA	7.4	7.5	7.6	V
Line Regulation	V_{CCZ} – 3V < V_{CC} < V_{CCZ} – 0.5V		2	10	mV
Load Regulation	1mA < I_O < 20mA		2	15	mV
Temperature Stability			0.4		%
Total Variation	Line, load, temp.	7.25		7.65	V
Long Term Stability	T_J = 125°C, 1000 hrs (Note 3)		5	25	mV
Short Circuit Current	V_{CC} < V_{CCZ} – 0.5V, V_{REF} = 0V	–15	–40	–100	mA
PWM					
Start Period Duty Cycle	ML4824-1	0-44	0-47	0-50	%
	ML4824-2	0-37	0-40	0-45	%
PFC					
Minimum Duty Cycle	V_{IEAO} > 3.8V			0	%
Maximum Duty Cycle	V_{IEAO} < 1.2V	90	95		%
Outputs					
Output Voltage Low	I_{OUT} = –20mA		0.3	0.8	V
	I_{OUT} = –50mA		0.5	3.0	V
Output Voltage High	I_{OUT} = 20mA	9.5	10		V
	I_{OUT} = 50mA	9	9.5		V
Output Voltage Low in UVLO	I_{OUT} = 10mA, V_{CC} = 8V		0.7	1.5	V
Output Rise/Fall Time	C_L = 1000pF		50		ns

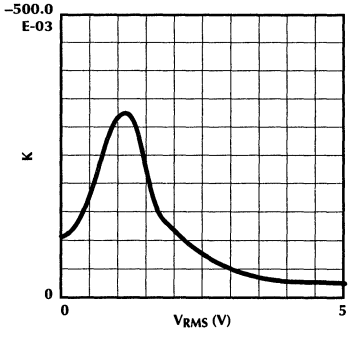
ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Under-Voltage Lockout and Bias Circuits					
I_C Shunt Voltage (V_{CCZ})	I_{CC} = 25mA	12.8	13.5	14.2	V
V_{CCZ} Load Regulation	25mA < I_{CC} < 55mA		±150	±300	mV
V_{CCZ} Total Variation	Load, temp.	12.4		14.6	V
Start-up Current	$V_{CC} \leq$ 12.3V		0.7	1.1	mA
Operating Current	$V_{CC} = V_{CCZ} - 0.5V$		16	19	mA
Undervoltage Lockout Threshold		12	13	14	V
Undervoltage Lockout Hysteresis		2.7	3.05	3.4	V

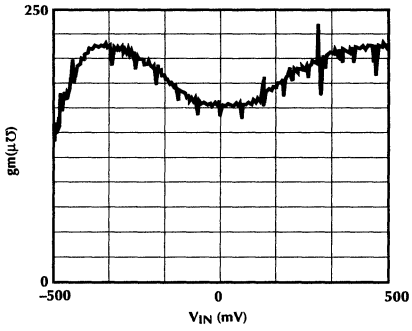
Note 1: gmV is the feedback amplifier transconductance and gmI is the sense amplifier transconductance.
Note 2: Gain = K x 5 3V; $K = (I_{MULO} - I_{OFFSET})(I_{AC} \times V_{EAO} - 1.5)^{-1}$
Note 3: This parameter not 100% tested but guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

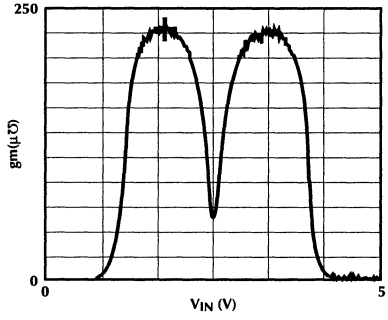
Multiplier Gain (K) vs. VRMS



IEAO Transconductance (gm)



VEAO Transconductance (gm)



7

FUNCTIONAL DESCRIPTION

OVERVIEW

The ML4824 consists of an average current controlled, continuous boost Power Factor (PFC) front-end section with a synchronized Pulse Width Modulator (PWM) back-end. The PWM can be used in either current mode or voltage feed-forward mode.

Synchronizing the PWM with the PFC simplifies the PWM compensation due to the controlled ripple on the PFC output capacitor (the PWM input capacitor). The ML4824XP-1 runs at the same frequency as the PFC. The ML4824XP-2 runs at twice the frequency of the PFC; resulting in a smaller output capacitor and inductor.

In addition to power factor correction, a number of hazard protection features have been built into the ML4824 including soft-start, over-voltage, peak current limiting, brown-out protection, duty cycle limit, and under-voltage lockout.

PFC SECTION

Multiplier

Figure 1 shows the PFC multiplier section. The ML4824 multiplier is a linear current input multiplier which provides the high noise immunity required in high power switching power conversion. The rectified input sine wave is converted to a proportional current via a resistor and is then fed into the multiplier at pin 2, I_{AC}. Sampling current in this way reduces ground noise to an insignificant level.

The output of the multiplier is a 120Hz current sine wave which appears on the negative terminal of the IEA amplifier to form the reference for the current error amplifier. The quality of this waveform is dependent on the quality of the line voltage. The output voltage of the multiplier is given by:

$$V_{MUL} \approx (K)(I_{AC})(VEAO - 1.5V)(3.5k\Omega)$$

where:

I_{AC} is the current in the dropping resistor

VEAO is the output of the error amplifier

K is the gain of the multiplier

The output of the multiplier is limited to around 0.8V and its typical gain characteristics are illustrated in the typical performance characteristics.

AVERAGE CURRENT AND OUTPUT VOLTAGE REGULATION

The modulator in the PFC section will act to offset the positive voltage caused by the multiplier output by producing an offsetting negative voltage on the current sense resistor at pin 3. A cycle-by-cycle current limit is included to protect the MOSFET from high frequency current transients. When the voltage at pin 3 goes negative by more than one volt (–1V), the PFC modulation cycle is terminated.

For more information on compensating the average current and boost voltage error amplifier loops, see Application Notes 16, 33, and 34.

OVER-VOLTAGE PROTECTION

The over-voltage scheme is shown in Figure 2. The OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load should change suddenly.

A resistor divider from the high voltage DC output of the PFC is fed to FB at pin 15. When the voltage on pin 15 exceeds 2.7V, the PFC output driver is shut down. The PWM section will continue to operate. The OVP comparator has 125mV of hysteresis, and the PFC will not restart until the voltage at FB drops below 2.58V. The OVP feedback voltage, FB, should be set at a level where the active and passive external power components are safe to operate and within the safe operating voltage of the I_C, but not so low as to interfere with the boost voltage regulation loop.

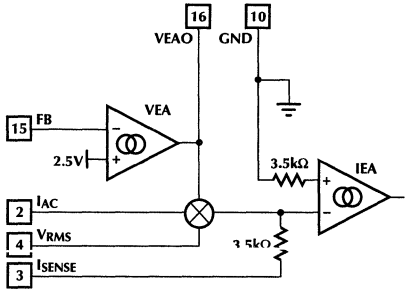


Figure 1. Multiplier Block Diagram

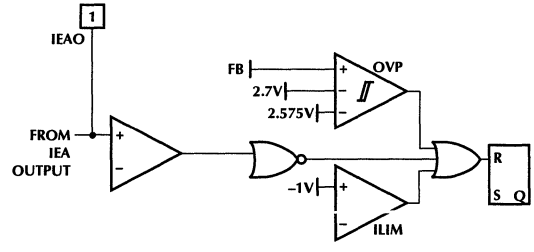


Figure 2. PFC Over-Voltage Comparator

Error Amplifier Compensation

The PWM loading of the PFC can be modelled as a negative resistor; an increase in input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers.

The PFC has two error amplifiers in the control loop. Figure 3 illustrates compensation for the amplifiers.

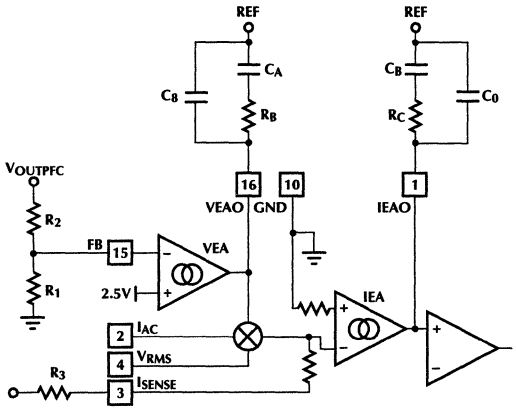


Figure 3. Compensation

There are two major concerns in compensating the voltage loop error amplifier; stability and transient response. Optimizing interaction between transient response and stability requires that the closed loop error amplifier bandwidth be 1/2 that of the line frequency or 30Hz for a 60Hz line.

Current Amplifier Compensation

The current amplifier compensation is similar to that of the error amplifier with the exception of the choice of cut-off frequency. The cut-off frequency of the current amplifier must be 10 times that of the voltage amplifier to prevent interaction with the voltage loop. It should also be limited to less than 1/6th that of the switching frequency; 16.7kHz for a 100kHz switching frequency.

For more information on calculating the values of compensation networks, see appication note 33 and appication note 34.

OSCILLATOR (RAMP1)

The oscillator frequency is determined by the values Of R_T and C_T, which determine the ramp and off-time of the

oscillator output clock $f_{OSC} = \frac{1}{(t_{RAMP} + t_{DEADTIME})}$

The deadtime of the oscillator is derived from the following equation:

$$t_{RAMP} = (C_T)(R_T)(\ln)\left[\frac{V_{REF} - 1.25}{V_{REF} - 3.75}\right] = 0.51[(R_T)(C_T)]$$

$@V_{REF} = 7.5V$

The ramp of the oscillator may be determined using the following:

$$t_{DEADTIME} = (C_T)\frac{2.5V}{5.1mA} = (490)(C_T)$$

The deadtime is so small ($t_{RAMP} >> t_{DEADTIME}$) that the operating frequency can typically be approximated by

$$f_{OSC} = \frac{1}{t_{RAMP}}$$

EXAMPLE:

For the application circuit shown in the data sheet, with the oscillator running at

$$f_{OSC} = (100kHz)(f_{OSC}) = \frac{1}{T} = \frac{1}{\text{oscillation period}} = \frac{1}{t_{RAMP}}$$

$$t_{RAMP} = (0.51)(R_T)(C_T) = 10 \times 10^{-6}$$

So

$$(R_T)(C_T) = 20 \times 10^{-5}$$

Choosing standard components values

$$C_T = 470pF$$

and

$$R_T = 41.2K\Omega$$

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PWM SECTION

Soft Start

Start-up of the PWM is controlled by the selection of the external capacitor on pin 5, SS. A current source of 50µA supplys the charging current for the capacitor, and start-up of the PWM begins at 1.25V. Start up delay can be programmed by the following equation:

$$C_{SS} = (t_d)\frac{50\mu A}{1.25V}$$

where C_{SS} is the required capacitance, and t_d is the desired start-up delay.

It is important that the time constant of the PWM soft-start allow the PFC time to generate sufficient output power for the PWM. The PWM start-up delay should be at least 5mS.

Thus, we get;

$$C_{SS} = (5\times10^{-3})\frac{50\mu A}{1.25V}$$

Where C_{SS} is the required capacitance.

VINOK Comparator

The VINOK comparator monitors the DC output of the PFC and inhibits the PWM if this voltage is lower than 380V. Once this voltage reaches 380V, the soft-start commences.

PWM CONTROL (RAMP2)

RAMP2 can be used as the PWM feedback or as a feed-forward ramp from the PFC with a peak voltage of 5V.

PWM CURRENT LIMIT

A current limit comparator is included with the non-inverting input on pin 9, DCI_{LIM}. The trigger level is set at 1V on the inverting input.

TYPICAL APPLICATION CIRCUIT

Figure 4 is the application circuit for a complete 200W power factor corrected power supply. Full design details are covered in Application Note 33, ML4824 Combo Controller Applications.

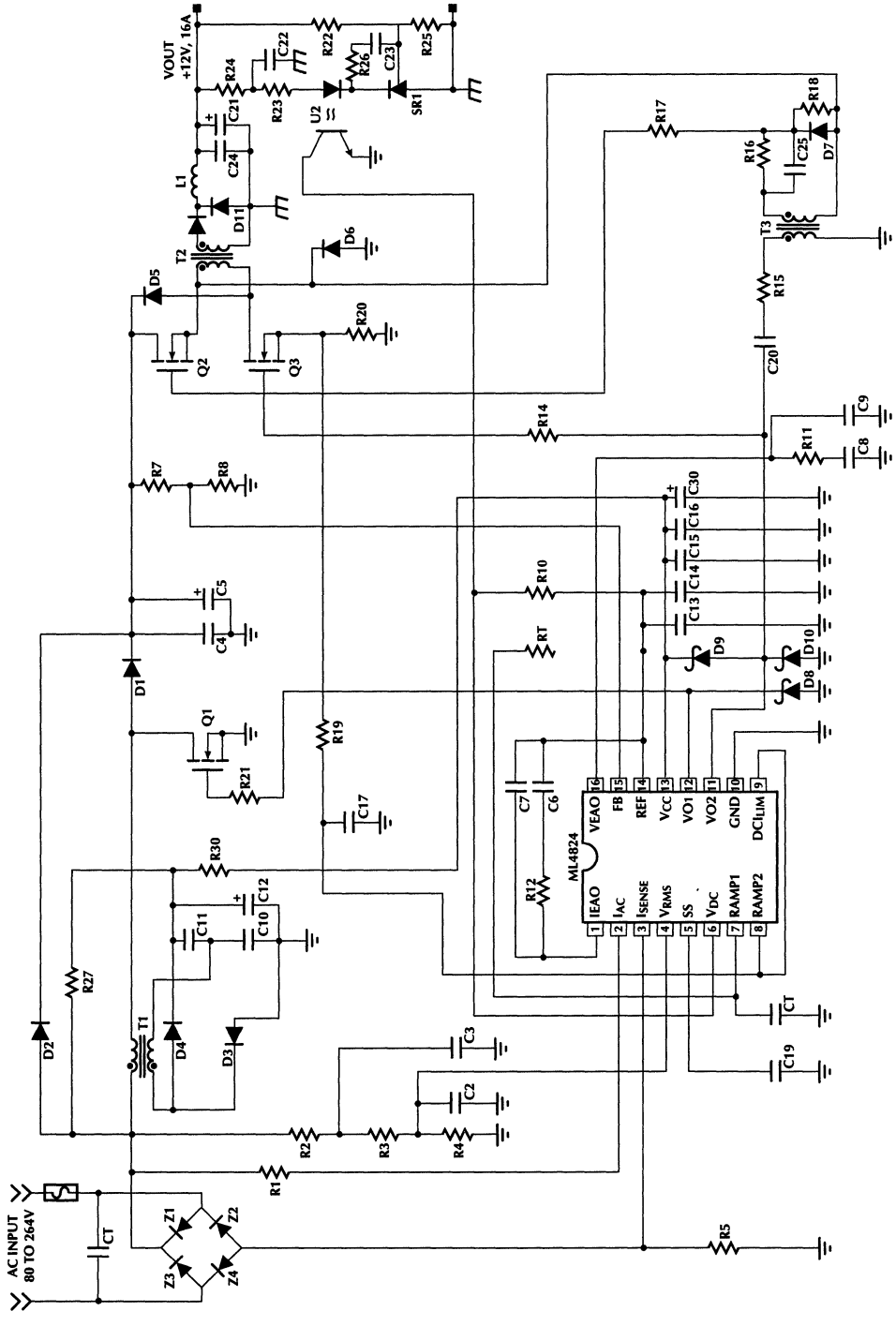


Figure 4. 200W PFC Corrected Power Supply

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4824CP-1	0°C to +70°C	Molded DIP (P16)
ML4824CS-1	0°C to +70°C	Wide SOIC (S16W)
ML4824CP-2	0°C to +70°C	Molded DIP (P16)
ML4824CS-2	0°C to +70°C	Wide SOIC (S16W)
ML4824IP-1	–40°C to +85°C	Molded DIP (P16)
ML4824IS-1	–40°C to +85°C	Wide SOIC (S16W)
ML4824IP-2	–40°C to +85°C	Molded DIP (P16)
ML4824IS-2	–40°C to +85°C	Wide SOIC (S16W)

Micro Linear

ML4825

High Frequency Power Supply Controller

GENERAL DESCRIPTION

The ML4825 High Frequency PWM Controller is an IC controller optimized for use in Switch Mode Power Supply designs running at frequencies to 1MHz. Propagation delays are minimal through the comparators and logic for reliable high frequency operation while slew rate and bandwidth are maximized on the error amplifier. This controller is designed to work in either voltage or current mode and provides for input voltage feed forward.

A 1V threshold current limit comparator provides cycle-by-cycle current limit while exceeding a 1.4V threshold initiates a soft-start cycle. The soft start pin doubles as a maximum duty cycle clamp. All logic is fully latched to provide jitter-free operation and prohibit multiple pulsing. An under-voltage lockout circuit with 800mV of hysteresis assures low startup current and drives the outputs low.

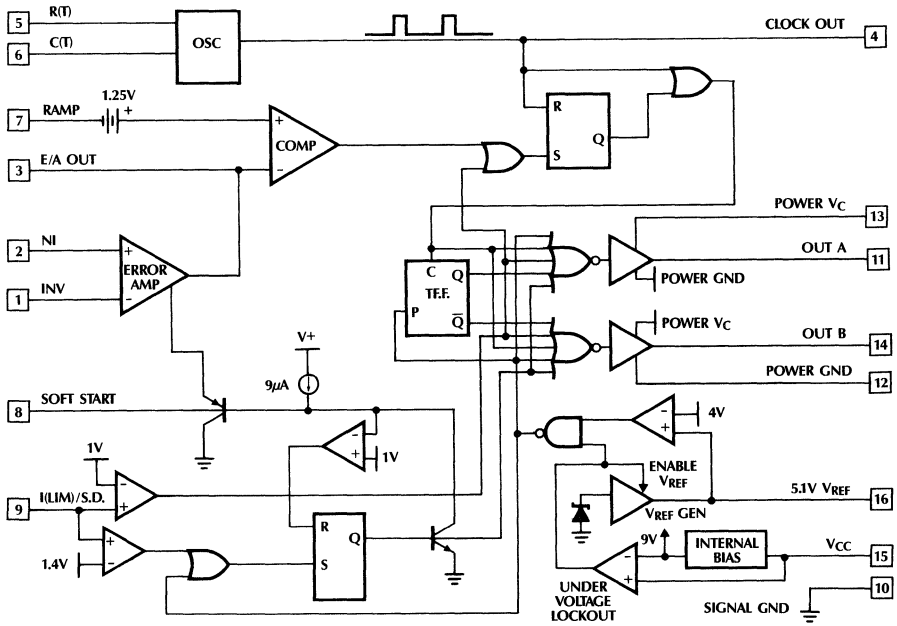
The ML4825 is fabricated on a 40V bipolar process from the FB3480 Power Supply Controller Array. Customized versions of this controller are therefore easily implemented. Please refer to the FB3480 datasheet for more information.

This controller is similar in architecture and performance to the UC1825 controller, however the ML4825 includes many features not found on the 1825. These features are set in *Italics*.

FEATURES

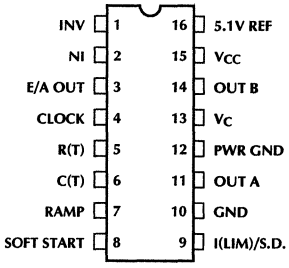
- Practical Operation at Switching Frequencies to 1.0MHz
- High Current (2A peak) Dual Totem Pole Outputs
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start and Max. Duty Cycle Control
- Under Voltage Lockout with Hysteresis
- 5.1V, ±1% Trimmed Bandgap Reference
- Pin Compatible Improved Replacement for UC1825
- *Fast Shut Down Path from Current Limit to Outputs*
- *Outputs Preset to Known Condition After Under Voltage Lockout*
- *Soft Start Latch Ensures Full Soft Start Cycle*
- *Outputs Pull Low for Undervoltage Lockout*

BLOCK DIAGRAM



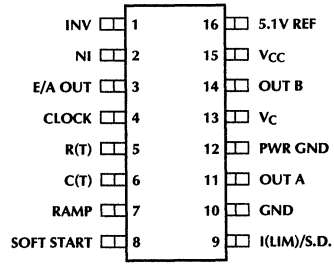
PIN CONNECTIONS

ML4825
16-Pin DIP



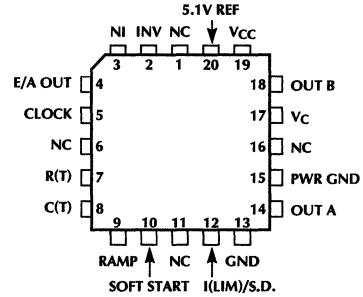
TOP VIEW

ML4825
16-Pin SOIC



TOP VIEW

ML4825
20-Pin PCC



PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	INV	Inverting input to error amp.
2	NI	Non-inverting input to error amp.
3	E/A OUT	Output of error amplifier and input to main comparator.
4	CLOCK	Oscillator output.
5	R(T)	Timing Resistor for Oscillator — sets charging current for oscillator timing capacitor (pin 6).
6	C(T)	Timing Capacitor for Oscillator.
7	RAMP	Non-Inverting input to main comparator. Connected to C(T) for Voltage Mode operation or to current sense resistor for current mode.
8	SOFT START	Normally connected to Soft Start Capacitor.
9	I(LIM)/S.D.	Current limit sense pin. Normally connected to current sense resistor.
10	GND	Analog Signal Ground.
11	OUT A	High Current Totem pole output. This output is the first one energized after Power On Reset.
12	PWR GND	Return for the High Current Totem pole outputs.
13	V_C	Positive Supply for the High Current Totem pole outputs.
14	OUT B	High Current Totem pole output.
15	V_{CC}	Positive Supply for the IC.
16	5.1V REF	Buffered output for the 5.1V voltage reference.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13) 30V
Output Current, Source or Sink (Pins 11, 14)
DC 0.5A
Pulse (0.5μs) 2.0A
Analog Inputs
(Pins 1, 2, 7) ..... –0.3V to 7V
(Pins 9, 8) ..... –0.3V to 6V
Clock Output Current (Pin 4) ..... –5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... –5mA
Junction Temperature
ML4825I, ML4825C ..... 125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C

Thermal Resistance (θ_{JA})
Plastic DIP or SOIC ..... 65°C/W
Plastic Chip Carrier (PCC) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range
ML4825I ..... –40°C to +85°C
ML4825C ..... 0°C to +70°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator						
Initial Accuracy		T_J = 25°C, (note 1)	360	400	440	KHz
Voltage Stability		10V < V_{CC} < 30V, T_A=25°C (note 1)		0.2	2	%
Temperature Stability		(note 1)			5	%
Total Variation		line, temp, (note 1)	340		460	KHz
Clock Out High			3.9	4.5		V
Clock Out Low				2.3	2.9	V
Ramp Peak		(note 1)	2.6	2.8	3.0	V
Ramp Valley		(note 1)	0.7	1.0	1.25	V
Ramp Valley to Peak		(note 1)	1.6	1.8	2.0	V
Reference Section						
Output Voltage	ML4825C	T_J = 25°C, I_O = 1mA	5.00	5.10	5.20	V
	ML4825I		5.05	5.10	5.15	V
Line Regulation		10V < V_{CC} < 30V		2	20	mV
Load Regulation		1mA < I_O < 10mA		5	20	mV
Temperature Stability		–55°C < T_J < 150°C, (note 1)		.2	.4	%
Total Variation	ML4825C	line, load, temp (note 1)	4.95		5.25	V
	ML4825I	line, load, temp T_A > 0°C, (note 1)	5.00		5.20	V
	ML4825I	line, load, temp T_A < 0°C, (note 1)	4.95		5.25	V
Output Noise Voltage		10Hz to 10KHz		50		μV
Long Term Stability		T_J = 125°C, 1000 hrs, (note 1)		5	25	mV
Short Circuit Current		V_{REF} = 0V	–15	–50	–100	mA
Error Amplifier Section						
Input Offset Voltage	ML4825I,C	T_A > 0°C			15	mV
	ML4825I	T_A < 0°C			20	mV
Input Bias Current				.6	3	μA
Input Offset Current				.1	1	μA
Open Loop Gain		1 < V_O < 4V	60	96		dB

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ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section (Continued)						
CMRR	ML4825I,C	$1.5V < V_{CM} < 5.5V$, $T_A > 0°C$	75	95		dB
	ML4825I	$1.5V < V_{CM} < 5.5V$, $T_A < 0°C$	65	95		dB
PSRR	ML4825I,C	$10V < V_{CC} < 30V$, $T_A > 0°C$	80	110		dB
	ML4825I	$10V < V_{CC} < 30V$, $T_A < 0°C$	75	110		dB
Output Sink Current		$V_{PIN\ 3}$ = 1V	1	2.5		mA
Output Source Current		$V_{PIN\ 3}$ = 4V	-.5	-1.3		mA
Output High Voltage		$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	V
Output Low Voltage		$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth		(note 1)	3	5.5		MHz
Slew Rate		(note 1)	6	12		V/μs
PWM Comparator Section						
Pin 7 Bias Current	ML4825I,C	$V_{PIN\ 7}$ = 0V, $T_A > 0°C$		-1	-5	μA
	ML4825I	$V_{PIN\ 7}$ = 0V, $T_A < 0°C$			-10	μA
Duty Cycle Range	ML4825C		0		85	%
	ML4825I	$T_A > 0°C$	0		80	%
	ML4825I	$T_A < 0°C$	0		70	%
Pin 3 Zero DC Threshold		$V_{PIN\ 7}$ = 0V	1.1	1.25		V
Delay to Output		(note 1)		50	80	ns
Soft-Start Section						
Charge Current		$V_{PIN\ 8}$ = 0.5V	3	9	20	μA
Discharge Current		$V_{PIN\ 8}$ = 1V	1			mA
Current Limit/Shutdown Section						
Pin 9 Bias Current	ML4825C	$0V < V_{PIN\ 9} < 4V$			+10	μA
	ML4825I	$0V < V_{PIN\ 9} < 4V$			+15	μA
Current Limit Threshold			.9	1	1.1	V
Shutdown Threshold		$T_A > 0°C$	1.25	1.4	1.55	V
		$T_A < 0°C$	1.25	1.4	1.60	V
Delay to Output		(note 1)		40	70	ns
Output Section						
Output Low Level		I_{OUT} = 20mA		.25	.4	V
		I_{OUT} = 200mA		1.2	2.2	V
Output High Level		I_{OUT} = -20mA	13.0	13.5		V
		I_{OUT} = -200mA	12.0	13.0		V
Collector Leakage		V_C = 30V		100	500	μA
Rise/Fall Time		C_L = 1000pF, (note 1)		30	60	ns
Under-Voltage Lockout Section						
Start Threshold			8.7	9.2	9.6	V
UVLO Hysteresis			0.3	0.8	1.2	V
Supply Current						
Start Up Current	ML4825I,C	V_{CC} = 8V, $T_A > 0°C$		1.1	2.5	mA
	ML4825I	V_{CC} = 8V, $T_A < 0°C$			3.5	mA
I_{CC}		$V_{PIN\ 1,\ 7,\ 9}$ = 0V, $V_{PIN\ 2}$ = 1V, T_A=25°C		26	33	mA

Note 1: This parameter not 100% tested in production but guaranteed by design.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4825 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $3/R_{SET}$. When the capacitor voltage reaches the upper threshold (Ramp Peak), the comparator changes state and the capacitor discharges to the lower threshold (Ramp Valley) through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where: T_{RAMP} = C (Ramp Valley to Peak)/I_{SET}

and: $T_{DEADTIME}$ = C (Ramp Valley to Peak)/I_{Q1}

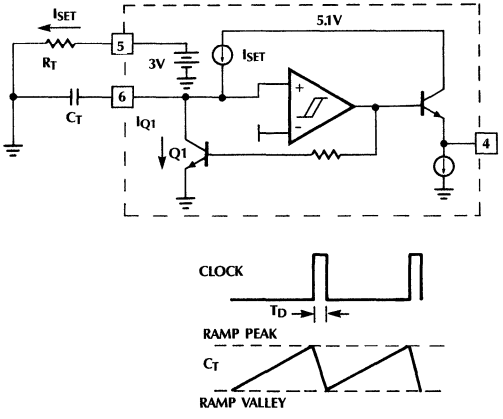


Figure 1. Oscillator Block Diagram

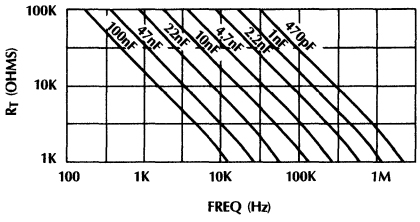


Figure 2. Oscillator Timing Resistance vs Frequency

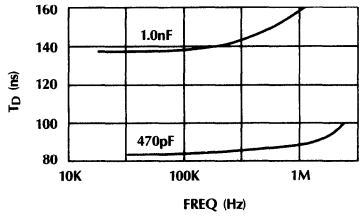


Figure 3. Oscillator Deadtime vs Frequency

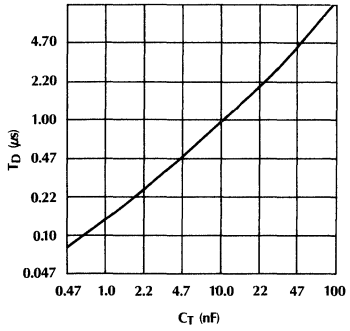


Figure 4. Oscillator Deadtime vs C(T) (3KΩ ≤ R(T) ≤ 100KΩ)

ERROR AMPLIFIER

The ML4825 error amplifier is a 5.5MHz bandwidth 12V/µs slew rate op-amp with provision for limiting the positive output voltage swing (Output Inhibit line) for ease in implementing the soft start function.

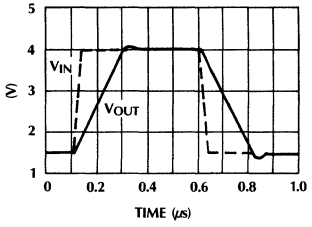


Figure 5. Unity Gain Slew Rate

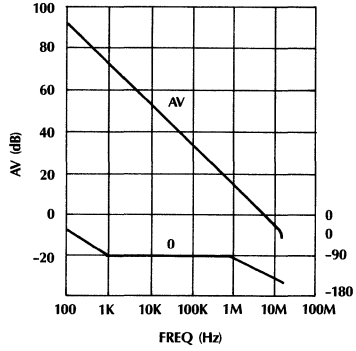


Figure 6. Open Loop Frequency Response

OUTPUT DRIVER STAGE

The ML4825 Output Driver is a 2A peak output high speed totem pole circuit designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors.

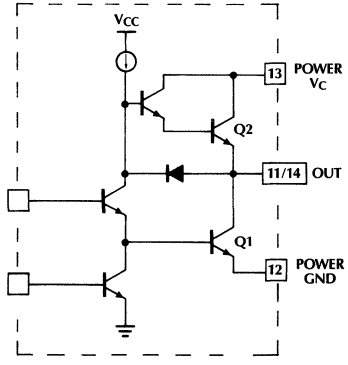


Figure 7. Simplified Schematic

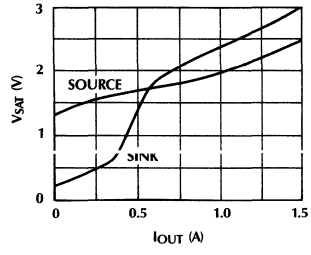


Figure 8. Saturation Curves

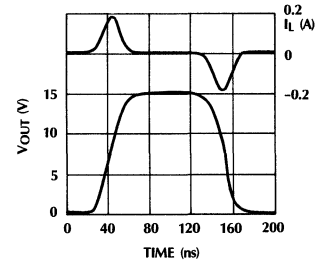


Figure 9. Rise/Fall Time (C_L = 1000pF)

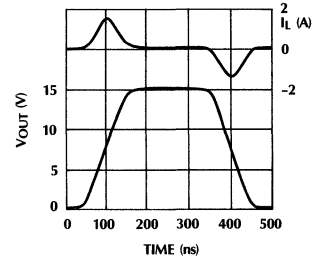


Figure 10. Rise/Fall Time (C_L = 10,000pF)

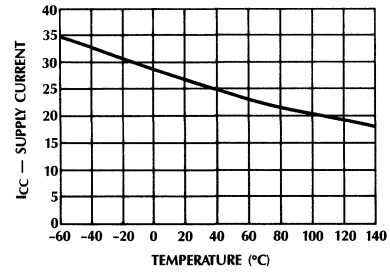


Figure 11. Supply Current vs Temperature

SOFT START AND CURRENT LIMIT

The ML4825 employs two current limits. When the voltage at pin 9 exceeds 1V, the outputs are immediately shut off and the cycle is terminated for the remainder of the oscillator period by resetting the RS flip flop.

If the output current is rising quickly such that the voltage on pin 9 reaches 1.4V before the outputs have turned off, a soft start cycle is initiated. The soft start capacitor (pin 8) is discharged and outputs are held "off" until the voltage at pin 8 reaches 1V, ensuring a complete soft start cycle. The duty cycle on start up is limited by limiting the output voltage of the error amplifier voltage to the voltage at pin 8.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4825CP	0°C to +70°C	Molded DIP (P16)
ML4825CS	0°C to +70°C	Molded SOIC (S16W)
ML4825CQ	0°C to +70°C	Molded PCC (Q20)
ML4825IP	–40°C to +85°C	Molded DIP (P16)
ML4825IS	–40°C to +85°C	Molded SOIC (S16W)
ML4825IQ	–40°C to +85°C	Molded PCC (Q20)

ML4826

Power Factor and Dual PWM Combo

GENERAL DESCRIPTION

The ML4826 is a complete high power controller for a power factor corrected, switched mode power supply. Power factor correction results in smaller, lower cost bulk capacitors, reduces power line loading and the stress on switching FETs, and results in a power supply that fully complies with IEC555-2 specifications. Contained in the ML4826 are circuits for the implementation of a leading edge, average current mode "boost" type power factor correction and a trailing edge, synchronized current or voltage mode Pulse Width Modulator (PWM) with dual totem pole outputs.

The ML4826 comes in two versions: the ML4826XP-1 ($f_{PWM} = f_{PFC}$) and the ML4826XP-2 ($f_{PWM} = 2f_{PFC}$).

An over-voltage comparator is configured to shut down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting and input voltage brown-out protection.

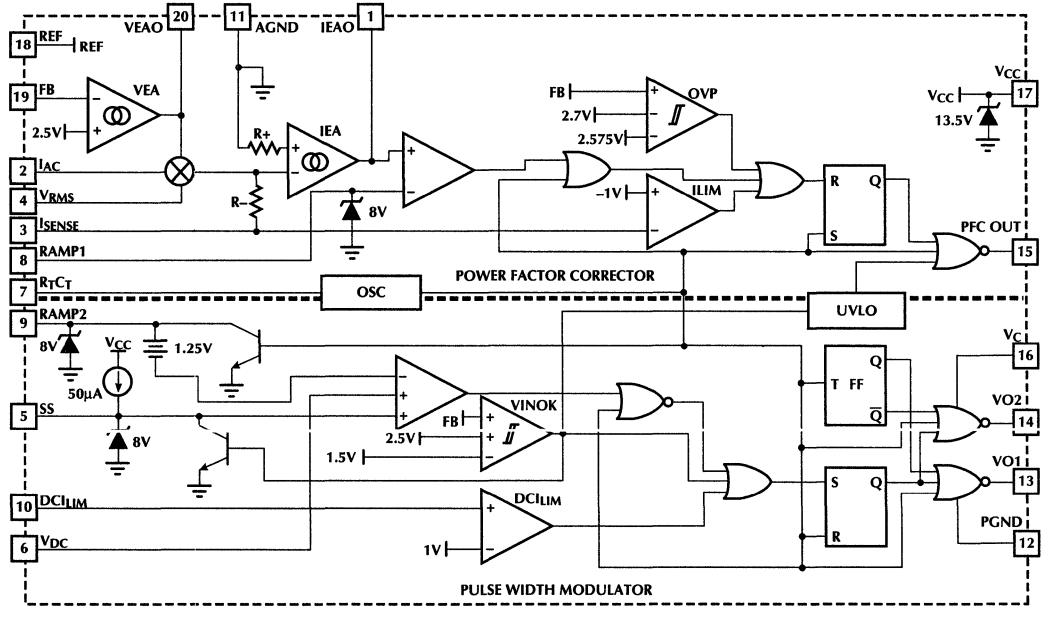
The PWM section can be operated in current mode or voltage mode and includes a precision duty cycle limit to prevent transformer saturation.

When a brown-out occurs, the VINOK comparator shuts down both the PFC and the PWM. A soft-start of the PWM follows with the return of normal line power.

FEATURES

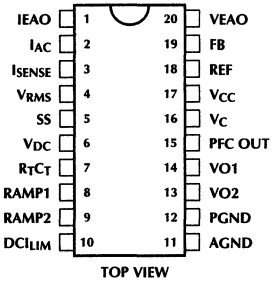
- Internally synchronized PFC and PWM in one IC
- Low total harmonic distortion
- Average current sensing, continuous boost, leading edge PFC
- High efficiency, trailing edge PWM with dual totem pole outputs
- Current mode or voltage mode operation
- Average line voltage compensation with brown-out control (Universal Input)
- PFC over-voltage comparator eliminates output "runaway" due to load removal
- Current fed multiplier to improve noise immunity
- Simplified compensation scheme
- Over-voltage protection, UVLO, and soft-start

BLOCK DIAGRAM



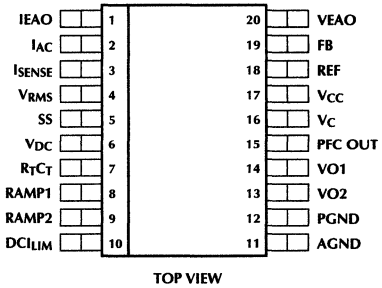
PIN CONFIGURATION

ML4826
20-Pin DIP (P20)



TOP VIEW

ML4826
20-Pin SOIC (S20)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	IEAO	PFC transconductance current error amplifier output.
2	I_{AC}	PFC multiplier reference input.
3	I_{SENSE}	Current sense input to the PFC current limit comparator.
4	V_{RMS}	Input for PFC RMS line voltage compensation.
5	SS	PWM soft start (capacitor).
6	V_{DC}	PWM output voltage feedback.
7	R_TC_T	Connection for oscillator frequency setting components.
8	RAMP1	PFC ramp input. Can be used for voltage feed forward.
9	RAMP2	PWM ramp input. Current mode; current sense input. Voltage mode; input for PFC output (feed forward ramp).
10	DCI_{LIM}	PWM current limit.
11	AGND	Analog signal ground.
12	PGND	Return for the PWM to' ,ole outputs.
13	VO2	PWM totem pole driver 2 output.
14	VO1	PWM totem pole driver 1 output.
15	PFC OUT	PFC driver output.
16	V_C	Positive supply for the PWM totem pole outputs.
17	V_{CC}	Positive supply (with shunt regulator).
18	REF	Buffered output for the 7.5V voltage reference.
19	FB	PFC transconductance voltage error amplifier input.
20	VEAO	PFC transconductance voltage error amplifier output.

7

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 55mA
Peak Output Current, Source or Sink
(pins 13, 14 & 15) 0.5A
Output Energy (capacitive load per cycle) 1.5mJ
Multiplier I_{AC} Input (pin 2) 10mA
Analog Inputs (pins 4, 6, 9 & 15) ..... –0.3V to V_{CC} – 2V
Pin 3 input voltage ..... –3V to +5V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP ..... 80°C/W
Plastic SOIC ..... 100°C/W

OPERATING CONDITIONS

Temperature Range
ML4826C ..... 0°C to 70°C
ML4826I ..... –40°C to +85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $R_{RAMP1} = R_T = 52.3k\Omega$, $C_{RAMP1} = C_T = 180pF$, T_A = Operating Temperature Range, I_{CC} = 25mA

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Amplifiers (pins 1, 3, 15, 16)					
Transconductance, gm_V	$V_{NON-INV} = V_{INV}$ (Note 1)	30	70	140	µ℧
Transconductance, gm_I	$V_{NON-INV} = V_{INV}$ (Note 1)	130	195	335	µ℧
Input Offset Voltage$_V$			±3.0	±15.0	mV
Input Offset Voltage$_I$			±3.0	±15.0	mV
Input Bias Current			–0.5	–1.0	µA
Open Loop Gain		60	75		dB
PSRR	$V_{CCZ} – 3V < V_{CC} < V_{CCZ} – 0.5V$	60	75		dB
Input Voltage Range	Pin 19 (Note 3)	0		7	V
	Pin 3 (Note 3)	–1.5		2	V
Output Low			0.65	1	V
Output High		6.0	6.7		V
Source Current	$\Delta V_{IN} = \pm 0.5V$, $V_{OUT} = 6V$	–40	–90		µA
Sink Current	$\Delta V_{IN} = \pm 0.5V$, $V_{OUT} = 1.5V$	40	90		µA
Comparators (pins 1, 3, 5, 6, 15)					
OVP Threshold		2.6	2.7	2.8	V
OVP Hysteresis		70	95	125	mV
ILIM Threshold		–0.80	–1.0	–1.15	V
ILIM Delay to Output	(Note 3)		150	300	ns
DCI_{LIM} Threshold		0.90	1.0	1.10	V
DCI_{LIM} Delay to Output	(Note 3)		150	300	ns
VINOK Threshold		2.4	2.5	2.6	V
VINOK Hysteresis		0.7	1.0	1.2	V
Input Bias Current			±0.45	±1	µA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Multiplier					
Gain (Note 2)	I_{PIN2} = 100µA, V_{PIN4} = 0V, V_{PIN15} = 0V	0.36	0.51	0.66	
	I_{PIN2} = 50µA, V_{PIN4} = 1.2V, V_{PIN15} = 0V	1.20	1.72	2.24	
	I_{PIN2} = 50µA, V_{PIN4} = 1.8V, V_{PIN15} = 0V	0.55	0.78	1.01	
	I_{PIN2} = 100µA, V_{PIN4} = 3.3V, V_{PIN15} = 0V	0.14	0.20	0.26	
Bandwidth	I_{AC} = 250µA		10		MHz
Multiplier Output Voltage	V_{PIN15} = 0V, V_{PIN5} = 1.15V I_{PIN2} = 250µA	0.72	0.8	0.88	V
Oscillator					
Initial Accuracy	T_A = 25°C	180	190	200	kHz
Voltage Stability	V_{CCZ} – 3V < V_{CC} < V_{CCZ} – 0.5V		1		%
Temperature Stability			2		%
Total Variation	Line, temp.	175		205	kHz
Ramp Valley to Peak Voltage			2.5		V
Dead Time	PFC only, ML4826-1 ML4826-2	100 200	310 440	450 550	ns ns
C_T Discharge Current	V_{PIN8} = 0V, V_{PIN7} = 2.5V	4.5	7.5	9.5	mA
Reference					
Output Voltage	T_A = 25°C, I_O = 1mA	7.4	7.5	7.6	V
Line Regulation	V_{CCZ} – 3V < V_{CC} < V_{CCZ} – 0.5V		2	10	mV
Load Regulation	1mA < I_O < 20mA		2	15	mV
Temperature Stability			0.4		%
Total Variation	Line, load, temp.	7.25		7.65	V
Long Term Stability	T_J = 125°C, 1000 hrs (Note 3)		5	25	mV
Short Circuit Current	V_{CC} < V_{CCZ} – 0.5V, V_{REF} = 0V	–15	–40	–100	mA
PWM					
Duty Cycle Range	ML4826-1	0-47	0-48	0-50	%
	ML4826-2	0-47	0-48	0-50	%
PFC					
Minimum Duty Cycle	ML4826-1, V_{IEAO} > 3.8V			0	%
	ML4826-2, V_{IEAO} > 5.7V			0	%
Maximum Duty Cycle	V_{IEAO} < 1.2V	90	95		%

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Outputs					
Output Voltage Low	I_{OUT} = –20mA		0.3	0.8	V
	I_{OUT} = –50mA		0.6	3.0	V
Output Voltage High	I_{OUT} = 20mA	9.5	10		V
	I_{OUT} = 50mA	9	10		V
Output Voltage Low in UVLO	I_{OUT} = 10mA, V_{CC} = 8V		0.8	1.5	V
Output Rise/Fall Time	C_L = 1000pF		50		ns
Under-Voltage Lockout and Bias Circuits					
Shunt Voltage (V_{CCZ})	I_{CC} = 25mA	12.8	13.5	14.2	V
V_{CCZ} Load Regulation	25mA < I_{CC} < 55mA		±150	±300	mV
V_{CCZ} Total Variation	Load, temp.	12.4		14.6	V
Start-up Current	$V_{CC} \leq$ 12.3V		0.7	1.1	mA
Operating Current	$V_{CC} = V_{CCZ} - 0.5V$		22	28	mA
Undervoltage Lockout Threshold		12	12.9	14	V
Undervoltage Lockout Hysteresis		2.7	3.05	3.4	V

Note 1: gmV is the feedback amplifier transconductance and gmI is the sense amplifier transconductance.
Note 2: Gain = K x 5.3V; $K = (I_{MULO} - I_{OFFSET}) \times I_{AC} \times (V_{EAO} - 1.5)^{-1}$
Note 3: This parameter not 100% tested but guaranteed by design.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4826CP-1	0°C to +70°C	Molded DIP (P20)
ML4826CS-1	0°C to +70°C	Molded SOIC (S20)
ML4826CP-2	0°C to +70°C	Molded DIP (P20)
ML4826CS-2	0°C to +70°C	Molded SOIC (S16)
ML4826IP-1	–40°C to +85°C	Molded DIP (P20)
ML4826IS-1	–40°C to +85°C	Molded SOIC (S20)
ML4826IP-2	–40°C to +85°C	Molded DIP (P20)
ML4826IS-2	–40°C to +85°C	Molded SOIC (S16)

BiCMOS Phase Modulation/Soft Switching Controller

GENERAL DESCRIPTION

The ML4828 is a complete BiCMOS phase modulation control IC suitable for full bridge soft switching converters. Unlike conventional PWM circuits, the phase modulation technique allows for zero voltage switching (ZVS) transitions and square wave drive across the transformer. The IC modulates the phases of the two sides of the bridge to control output power.

The ML4828 can be operated in either voltage or current mode. The delay times for the side A and B outputs are individually programmable to allow zero voltage switching transitions to take place.

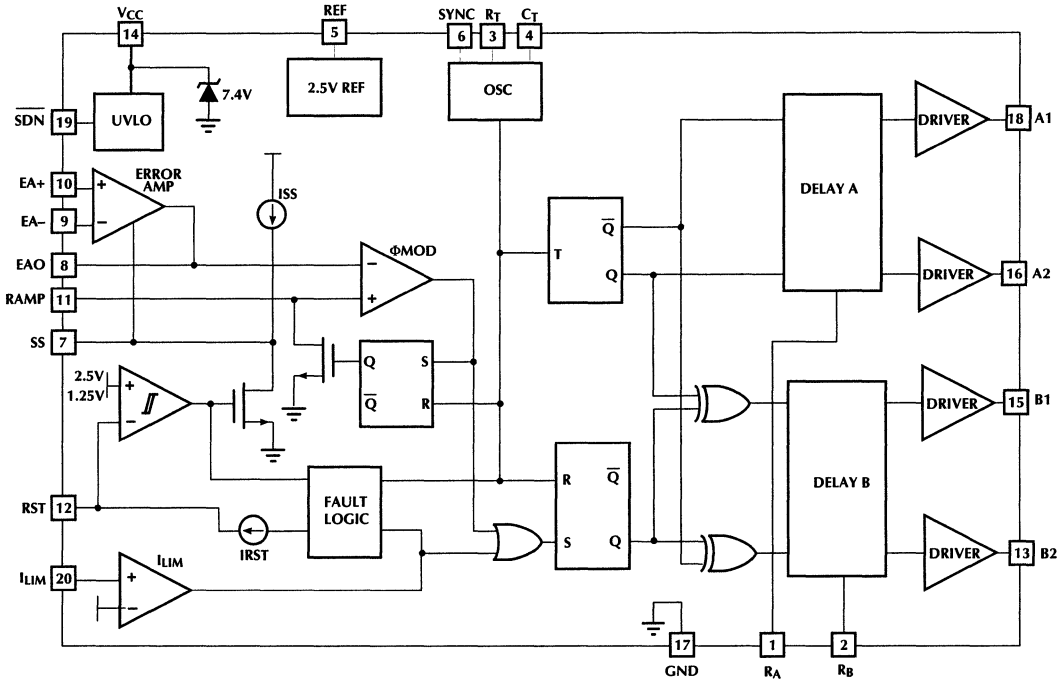
Both cycle-by-cycle current limit, integrating fault detection, and soft start reset are provided. The under-voltage lockout circuit features a 1.5V hysteresis with a low starting current to allow off-line start up with a bleed resistor. A shutdown function powers down the IC, putting it into a low quiescent state.

The circuit can be operated at frequencies up to 1MHz. The ML4828 contains four high current CMOS outputs which feature high slew rate with low cross conduction.

FEATURES

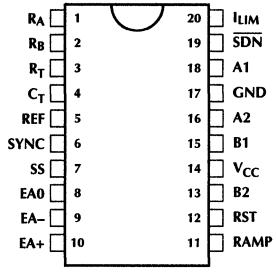
- 5V BiCMOS for low power and high frequency (1MHz) operation
- Full bridge phase modulation **Zero Voltage Switching** circuit with independent programmable delay times
- Current mode operation capability
- Cycle-by-cycle current limiting with integrating fault detection and restart delay
- Can be externally synchronized
- Four 3Ω CMOS output drivers
- Under-voltage lockout circuit with 1.5V hysteresis

BLOCK DIAGRAM



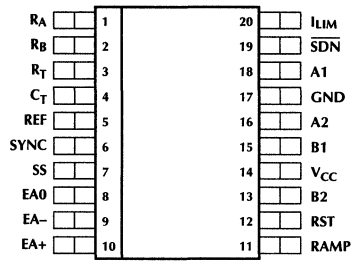
PIN CONNECTION

ML4828
20-Pin DIP (P20)



TOP VIEW

ML4828
20-Pin SOIC (S20)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	DESCRIPTION
1	R_A	A1 and A2 delay programming resistor.
2	R_B	B1 and B2 delay programming resistor .
3	R_T	Oscillator charge current programming resistor.
4	C_T	Oscillator timing capacitor.
5	REF	2.5V reference voltage.
6	SYNC	Synchronization input to oscillator.
7	SS	Soft start capacitor connection.
8	EAO	Error amplifier output.
9	EA-	Error amplifier inverting input.
10	EA+	Error amplifier non-inverting input.

PIN#	NAME	DESCRIPTION
11	RAMP	RC network for phase modulator ramp input.
12	RST	RC network for reset and integrating fault detect.
13	B2	B2 driver output.
14	V_{CC}	Power supply (≤6.5V)
15	B1	B1 driver output.
16	A2	A2 driver output.
17	GND	Ground.
18	A1	A1 driver output.
19	$\overline{SDN}$	Active low device shutdown.
20	I_{LIM}	Current limit.

ABSOLUTE MAXIMUM RATINGS

I_{CC} Current 25mA
Output Current, Source or Sink (Pins 13,15,16,18)
Pulse (0.5 µs) 1.0A
Analog Inputs
(Pins 8 thru 12, and 20) ..... –0.3V to V_{CC} + 0.3V
R_T Current Source (Pin 3) ..... –1mA
Error Amplifier Output Current (Pin 8) ..... ±2mA
Soft Start Discharge Current (Pin 7) 5mA
Oscillator Charging Current (Pin 4) ..... –1mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP ..... 40°C/W
Plastic SOIC ..... 100°C/W

OPERATING CONDITIONS

Commercial Temperature ..... 0°C to +70°C
Industrial Temperature ..... –40°C to +85°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $R_A = R_B = 33.3k\Omega$, $R_T = 16k\Omega$, $C_T = 270pF$, $V_{CC} = 5V$, T_A = Operation Temperature Range

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Oscillator					
Initial Accuracy	$T_A = 25°C$	340	360	380	kHz
Voltage Stability	$4.5V < V_{CC} < 5.5V$		4	5.3	%/V
Temperature Stability	(Note 1)		2		%
Total Variation	Line, temp.	325		400	kHz
C_T Discharge Current	$V_{PIN4} = 2V$	1.3	1.5		mA
Ramp Peak			2.6		V
Ramp Valley			1.12		V
Reference					
Initial Accuracy	$T_A = 25°C$, $I_O = 250µA$	2.48	2.5	2.52	V
Line Regulation	$4.5V < V_{CC} < 6.5V$		±0.2	±1	%/V
Load Regulation	100µA to 1mA		±0.5	±6	mV
Temperature Stability			0.45		%
Total Variation	Line, Load, & Temp	2.44		2.54	V
Long Term Stability	$T_J = 125°C$, 1000 hrs, (Note 1)		5	25	mV
Short Circuit Current	$V_{REF} = 0V$	–10	–23	–35	mA
Error Amplifier					
Input Offset Voltage		–20		20	mV
Open Loop Gain	$1V < V_O < 3V$	60	80		dB
PSRR	$4.5V < V_{CC} < 6.5V$	60	80		dB
Output Sink Current	$V_O = 0.5V$	1.2	1.9		mA
Output Source Current	$V_O = 3V$	–0.9	–1.1		mA
Output High Voltage	$I_{SOURCE} = –500µA$	2.8	2.85		V
Output Low Voltage	$I_{SINK} = 500µA$		0.1	0.2	V
Unity Gain Bandwidth	(Note 1)	7	10		MHz
Slew Rate	(Note 1)	0.5	1		V/µs

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Phase Modulator					
Pin 8 Zero Duty Cycle Threshold	$V_{PIN\ 3}$ = OV	0	0.5	0.9	V
Pin 11 Delay to Output	(Note 1)		50	80	ns
Pin 11 Discharge Current		48		85	mA
Soft-Start					
Pin 7 Charge Current	$V_{PIN\ 7}$ = 4V		–25	–50	µA
Pin 7 Discharge Current	$V_{PIN\ 7}$ = 1V	6	10	11.2	mA
Current Limit/Shutdown					
Current Limit Threshold		0.9	1.0	1.1	V
Pin 20 Delay to Output	(Note 1)		50		ns
Pin 12 Shutdown Threshold		1.0	1.1	1.5	V
Pin 12 Restart Threshold		2.2	2.4	2.6	V
Pin 12 Charging Current		–400	–460	–550	µA
$\overline{SDN}$ Shutdown Threshold			2.0		V
Output					
Output Low Level	I_{OUT} = 20 mA I_{OUT} = 100 mA		0.01 0.1	0.1 0.3	V V
Output High Level	I_{OUT} = –20 mA I_{OUT} = –100 mA	4.9 4.6	4.95 4.7		V V
Rise/Fall Time	C_L = 1000pF, (Note 1)		5	7	ns
ZVS Programmable Delay		240	280	300	ns
Delay Mismatch			0		ns
R_A/R_B Reference Voltage			2.5		V
Under-Voltage Lockout					
Start Threshold		5.1	5.85	6.6	V
Stop Threshold		4.1	4.2	4.3	V
Supply					
Shunt Voltage (V_{CCZ})	I_{CC} < mA		7.4		V
Start Up Current	V_{CC} < 6V			1	mA
Shutdown Current			100	170	µA
I_{CC}	V_{CC} = 5V, C_L = 1µF, T_A = 25°C		5		mA

Note 1: This parameter not 100% tested in production but guaranteed by design.
Note 2: V_{CC} must be brought above the UVLO start voltage (6V) before dropping to V_{CC} = 5V to ensure start-up.

FUNCTIONAL DESCRIPTION

PHASE MODULATOR

The ML4828 controls the power of a full bridge power section by modulating the phases of the switches of the A and B sides (Figure 1). The power cycle starts with A2 and B1 high, as shown in the timing diagram (Figure 2).

1. With A2 and B1 high, Q1 and Q2 are ON. Current flows through the primary of the transformer, and power is delivered to the output through the secondary winding (not shown).
2. After either the ΦMOD or I_{LIM} comparator trips, B1 goes low, turning off Q2. Energy in the primary winding charges the parasitic capacitances of Q2 and Q3 to +VIN during t_{DB}.
3. B2 goes high after time t_{DB}, which is set by the resistor connected from RB (pin 2) to GND. t_{DB} should be set large enough such that the source of Q3 has been charged to +VIN. At this time, Q3 turns on at zero voltage. The transformer is now effectively shorted through Q1 and Q3, with the primary magnetizing current circulating in the loop formed by the transformer primary, Q1, and Q3.
4. CLOCK then goes high and A2 goes low, while A1 remains low for time t_{DA}, which is set by the resistor connected from RA (pin 1) to GND. During this time, both Q1 and Q4 are OFF. The primary magnetizing current discharges the parasitic capacitances of Q1 and Q4 to GND.
5. A1 goes high after time t_{DA}. At this point, the drain of Q4 is discharged to GND, and Q4 turns on at zero voltage. With both Q3 and Q4 ON, a new power cycle starts, and power is delivered to the output.

The above sequence is then repeated with the roles of side A and B interchanged.

The ML4828 can also be used in current mode by sensing the load current on the RAMP input (pin 11).

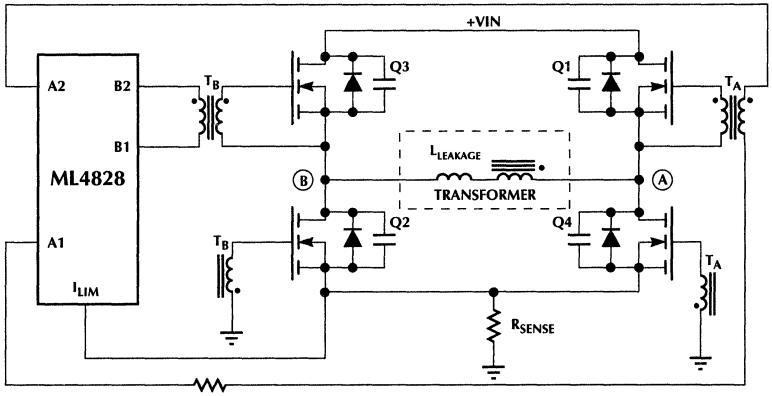


Figure 1. Simplified diagram of Phase Modulated power Outputs.

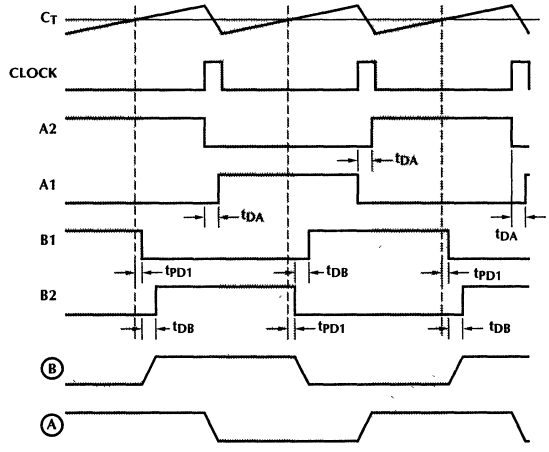


Figure 2. Phase Modulation control waveforms (Shaded areas indicate a power cycle).

SETTING THE OSCILLATOR FREQUENCY

The ML4828 switching frequency is determined by the charge and discharge times of the network connected to the R_T and C_T pins. Figure 3 shows the relationships between the internal clock and the charge and discharge times.

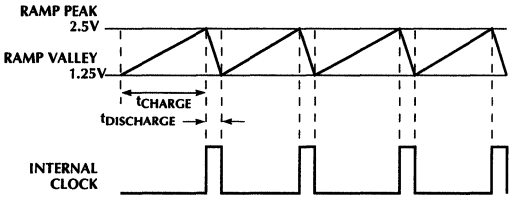


Figure 3. Internal Oscillator Timing.

The frequency of the oscillator is:

$$f_{OSC} = \frac{1}{t_{CHARGE} + t_{DISCHARGE}} \quad (1)$$

The ramp peak is 2.5V and the ramp valley is 1.25V, giving a ramp range of 1.25V. The charging current is set externally through the resistor R_T:

$$I_{CHARGE} = \frac{2.5V}{R_T} \quad (2)$$

while the discharging current is fixed at 1.4 mA. The charge and discharge times can be determined by:

$$t_{CHARGE} = \frac{C_T \times 1.25V}{I_{CHARGE}} = \frac{C_T \times R_T}{2} \quad (3)$$

$$t_{DISCHARGE} = \frac{C_T \times 1.25V}{I_{DISCHARGE}} = \frac{C_T \times 1.25V}{1.4mA} \quad (4)$$

The oscillator frequency can then be found by substituting the results of equations 3 and 4 into equation 1. This frequency activates a T flip-flop which generates the output pulses. The T flip-flop acts as a frequency divider (÷2), so the output frequency will be:

$$f_{OUT} = \frac{f_{OSC}}{2} \quad (5)$$

ERROR AMPLIFIER

The ML4828 error amplifier has a 10MHz bandwidth and a 1V/µs slew rate. Figure 4 gives the Bode plot of the error amplifier.

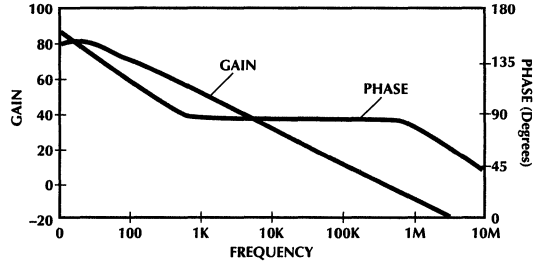


Figure 4. Error Amplifier Open-Loop Gain and Phase vs. Frequency.

OUTPUT DRIVERS

The ML4828 has four high-current CMOS output drivers, each capable of 1A peak output current. These outputs have been designed to quickly switch the gates of power MOSFET transistors via a gate drive transformer. For higher power applications, the outputs can be connected to external MOSFET drivers.

The output phase delay times are set by charging an internal 6.7pF capacitor up to the REF voltage (2.5V) via a current that is externally programmed through R_A and R_B, for the side A and side B drivers, respectively. The charging current and delay time for side A are given by:

$$I_A = \frac{2.5V}{R_A} \quad (6)$$

$$t_{DA} = 6.7pF \times R_A \quad (7)$$

The same equations can be applied to R_B. For example, with $R_A = 33k\Omega$:

$$t_{DA} = 6.7pF \times 33k\Omega = 220ns \quad (8)$$

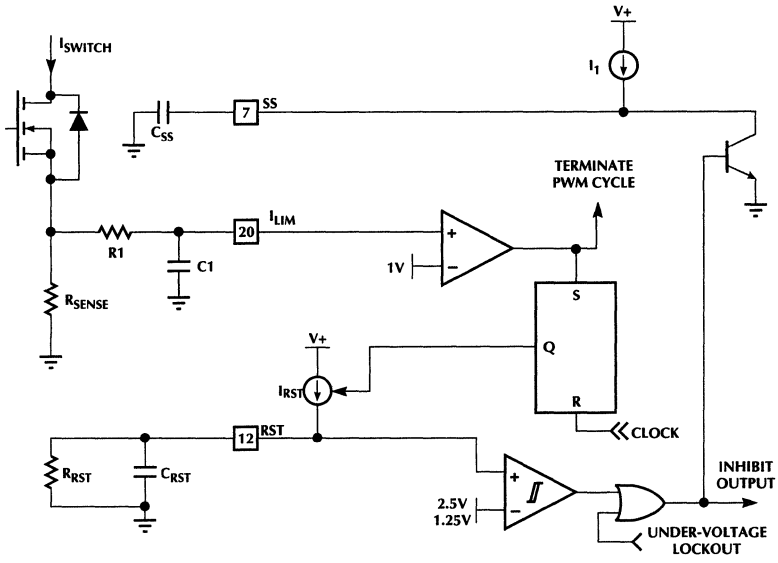


Figure 5. Over-Current, Soft-Start, and Integrating Fault Detect Circuits.

SOFT START TIME CONSTANT

During start up, the output voltage is much lower than the steady state value. Without soft start circuitry, the error amplifier output (EAO) would swing all the way to the upper limit and the phase modulator would issue pulses with full duty cycle, possibly causing output overshoot. To ensure smooth start up, EAO (pin 8) is pulled low and then gradually released through the charging of an external soft start capacitor connected to SS (pin 7). The soft start charging current is internally set at 25µA. Hence, EAO will rise with a time constant of:

$$\frac{dv}{dt} = \frac{25\mu A}{C_{SS}} \qquad (9)$$

For example, with C_{SS} = 25µF, the soft start rate of change will be:

$$\frac{dv}{dt} = \frac{25\mu A}{25\mu F} = 1\frac{V}{s} \qquad (10)$$

FAULT TIME CONSTANT AND RESTART DELAY

Figure 5 shows the internal circuitry and external components involved in fault detection. During normal operation, RST (pin 12) is discharged to ground through the external resistor R_{RST}. The I_{LIM} comparator has a threshold of 1V. R_{SENSE} is selected so that the voltage across it will be equal to the I_{LIM} threshold at the maximum desired I_{SWITCH} current. When the voltage across R_{SENSE} exceeds 1V, the I_{LIM} comparator trips, terminating the present power cycle, and at the same time activating the fault logic to turn on the 500µA current source I_{RST}. This current charges the reset capacitor C_{RST}. For proper design, R_{RST} should be very large (in the order of 100kΩ). This will cause nearly all of the I_{RST} current (approximately 500µA) to go into charging C_{RST} at a rate of:

$$\frac{dv}{dt} = \frac{500\mu A}{C_{RST}} \qquad (11)$$

in volts per second. I_{RST} will be turned off at the beginning of the next clock cycle. If the current limit condition is removed, RST will be gradually discharged to ground, and normal operation resumes as shown in Figure 6.

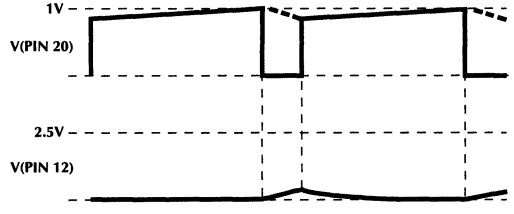


Figure 6. I_{LIM} and Resulting RC_{RST} Waveforms During Load Surge.

If the current limit condition persists, then I_{RST} will be reactivated, thus charging C_{RST} to a higher level as shown in Figure 7. Eventually, the voltage at RST will exceed 2.5V, and the soft start comparator will trip, shutting down all power drivers and inhibiting any further delivery of power. At the same time, the soft start capacitor C_{SS} is discharged to prepare for the next start up cycle.

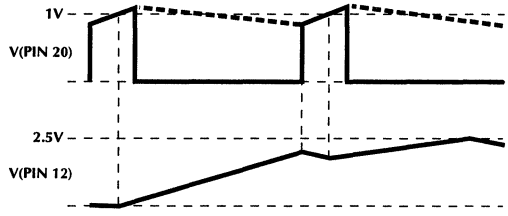


Figure 7. I_{LIM} and Resulting RC_{RST} Waveforms During Short Circuit.

During the I_{LIM} shutdown, I_{RST} is turned off, and C_{RST} is discharged through R_{RST} with a time constant of:

$$t_{RST} = R_{RST} \times C_{RST} \quad (12)$$

When the condition causing the current limit is removed, R_{RST} will discharge C_{RST} with a time constant of t_{RST}. When the voltage at RST (pin 12) drops to 1.25V, the soft start comparator and the converter will undergo a start up cycle. The restart delay ($t_{D(RST)}$) is given by:

$$t_{D(RST)} = t_{RST} \times 1.39 \quad (13)$$

For example, with C_{RST} = 25µF and R_{RST} = 240kΩ:

$$\frac{dv}{dt} = \frac{500\mu A}{25\mu F} = 20\frac{V}{s} \quad (14)$$

and:

$$t_{D(RST)} = (240k\Omega \times 25\mu F) \times 1.39 = 8.3s \quad (15)$$

Since the threshold for shutdown is 2.5V, the controller will shut down after approximately 125ms. After the converter recovers from the current limit condition, the controller will reactivate after 8.3s.

UNDERVOLTAGE LOCKOUT

During start-up, the ML4828 draws very little current (typically 150µA) and V_{REF} is disabled. When V_{CC} rises above 6.0V, the internal circuitry and V_{REF} are enabled, and will stay enabled until V_{CC} falls below the 4.5V UV lockout threshold.

SHUTDOWN FUNCTION

The ML4828 can be externally shut down by bringing SDN (pin 19) low. The shutdown threshold (V_{SD}) is given by:

$$V_{SD} = 0.33 \times V_{CC} \quad (16)$$

For example, if V_{CC} = 5V, then V_{SD} = 1.67V. As long as 2.4V < V_{CC} < 6.0V, the SDN pin will be TTL compatible.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4828CP	0°C to +70°C	20-Pin DIP (P20)
ML4828CS	0°C to +70°C	20-Pin DIP (S20)
ML4828IP	–40°C to +85°C	20- Pin DIP (P20)
ML4828IS	–40°C to +85°C	20- Pin SOIC (S20)

ML4830

Electronic Ballast Controller

GENERAL DESCRIPTION

The ML4830 is a complete solution for a dimmable, high power factor, high efficiency electronic ballast. Contained in the ML4830 are controllers for "boost" type power factor correction as well as for a dimming ballast.

The Power factor circuit uses the average current sensing method with a current fed multiplier and over-voltage protection. This system produces power factors of better than 0.99 with low input current THD at > 95% efficiency. Special care has been taken in the design of the ML4830 to increase system noise immunity by using a high amplitude oscillator, and a current fed multiplier. An over-voltage protection comparator stops the PFC section in the event of sudden load decrease.

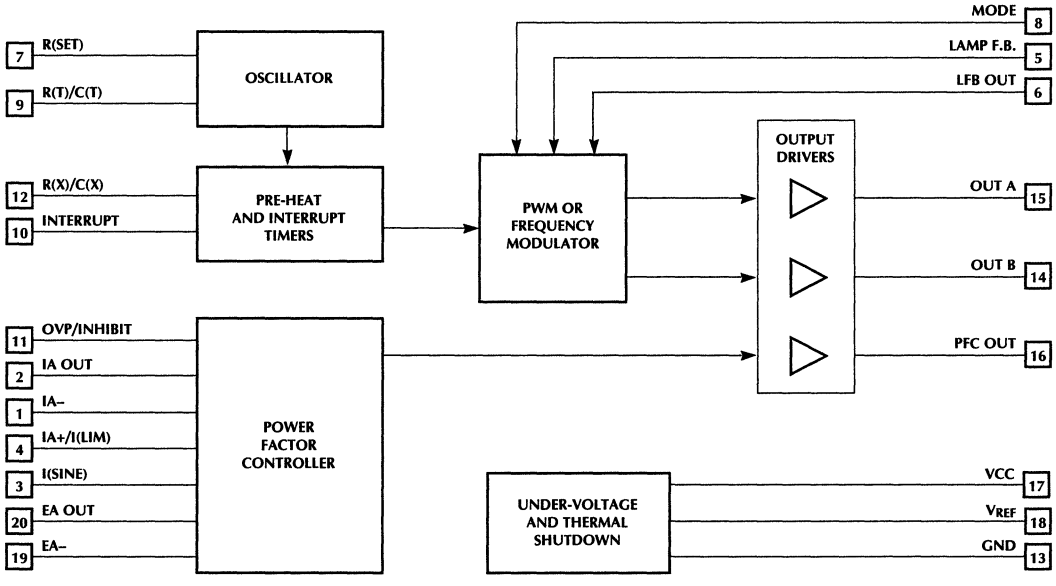
The ballast section provides for programmable starting scenarios with programmable preheat and lamp out-of-socket interrupt times. The IC controls lamp output through either frequency or Pulse Width control using lamp current feedback.

The ML4830 is designed using Micro Linear's Semi-Standard tile array methodology. Customized versions of this IC, optimized to specific ballast architectures can be made available. Contact Micro Linear or an authorized representative for more information.

FEATURES

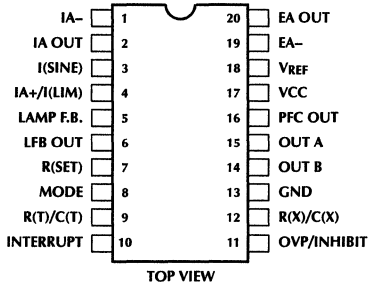
- Complete Power Factor Correction and Dimming Ballast Control on one IC
- Low Distortion, High Efficiency Continuous Boost, Average Current sensing PFC section
- Programmable Start Scenario for Rapid or Instant Start Lamps
- Selectable Variable Frequency dimming and starting
- Programmable Restart for lamp out condition to reduce ballast heating
- Over-Temperature Shutdown replaces external heat sensor for safety
- PFC Over-Voltage comparator eliminates output "runaway" due to load removal
- Large oscillator amplitude and current fed multiplier improves noise immunity

BLOCK DIAGRAM



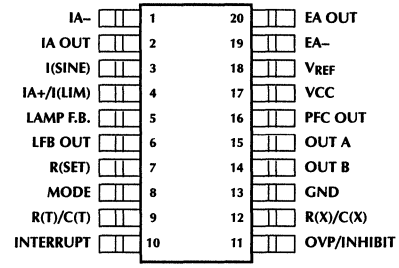
PIN CONFIGURATION

ML4830
20-PIN DIP (P20)



TOP VIEW

ML4830
20-PIN SOIC (S20)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	IA–	Inverting input of the PFC average current error amplifier
2	IA OUT	Output and compensation node of the PFC average current error amplifier
3	I(SINE)	PFC Current Multiplier input
4	IA+/I(LIM)	Non-Inverting input of the PFC average current error amplifier and input of peak current limit comparator
5	LAMP F.B.	Inverting input of an Error Amplifier used to sense (and regulate) lamp arc current. Also the input node for dimming control
6	LFB OUT	Output from the Lamp Current Error Amplifier used for lamp current loop compensation
7	R(SET)	External resistor which sets oscillator FMAX, and R(X)/C(X) charging current
8	MODE	Controls how the Lamp Current Error Amp and preheat timers modulate the ballast outputs. Two Variable Frequency and 1 PWM mode are available through this pin
9	R(T)/C(T)	Oscillator timing components
10	INTERRUPT	A voltage of greater than V_{REF} resets the chip and causes a restart after a delay of 3 times the start interval. Used for lamp-out detection and restart
11	OVP/ INHIBIT	When the voltage of this pin exceeds 5V, the PFC output is inhibited. When the voltage exceeds 6.7V, the IC function is inhibited and the IC is reset. This pin can be used for a remote ballast shutdown.
12	R(X)/C(X)	Sets the timing for the preheat, dimming lockout and interrupt
13	GND	IC Ground
14	OUT B	Ballast MOSFET drive output
15	OUT A	Ballast MOSFET drive output
16	PFC OUT	Power Factor MOSFET drive output
17	VCC	Positive Supply for the IC
18	V_{REF}	Buffered output for the 7.5V voltage reference
19	EA–	Inverting input to PFC error amplifier
20	EA OUT	PFC Error Amplifier output and compensation node

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 75mA
Output Current, Source or Sink (Pins 14)
DC 250mA
Output Energy (capacitive load per cycle)..... 1.5 mJ
Multiplier I(SINE) Input (Pin 3) ..... 10 mA
Amplifier Source Current (Pin 6, 20) ..... 50 mA
Analog Inputs (Pins 1, 5, 10, 11, 19) ....–0.3V to VCC –2V
Pin 4 input voltage .....–3V to +5V

Junction Temperature .....150°C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature (Soldering 10 Sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP–P ..... 65°C/W
Plastic SOIC..... 80°C/W

OPERATING CONDITIONS

Temperature Range
ML4830C ..... 0°C to 85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R(SET) = 26K, R(T) = 52.3K, C(T) = 470pF, T_J = Junction Operating Temperature Range, I_{CC} = 25mA

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Amplifiers (Pins 1, 2, 5, 6, 19, 20)					
Input Offset Voltage			±3.0	±10.0	mV
Input Bias Current			–0.3	–1.0	µA
Open Loop Gain		65	90		dB
PSRR	$V_{CCZ} - 3V < V_{CC} < V_{CCZ} - 0.5V$	70	100		dB
Output Low		0		0.5	V
Output High		7.2	7.5		V
Source Current	V_{OUT} = 7V	–4	–7		mA
Sink Current	V_{OUT} = 1.5V	5	10		mA
	V_{OUT} = 0.2V	10			µA
Slew Rate			1.5		V/µs
Unity Gain Bandwidth			3.0		MHz
Multiplier					
Output Voltage (Note 1)	I_{SINE} = 100µA, V_{PIN20} = 3V		80		mV
	I_{SINE} = 300µA, V_{PIN20} = 3V		255		mV
	I_{SINE} =100µA, V_{PIN20} = 6V		220		mV
	I_{SINE} = 300µA, V_{PIN20} = 6V		660		mV
Output Voltage Limit	I_{SINE} = 600µA, V_{PIN19} = 0V		0.88		V
Offset Voltage	I_{SINE} = 0, V_{PIN19} = 0V			15	mV
	I_{SINE} = 150µA, V_{PIN19} = 8V			15	mV
I(SINE) Input Voltage	I_{SINE} = 200µA	0.8	1.4	1.8	V

Note 1: Measured at Pin 1 with Pins 1 and 2 shorted together and Pin 4 at GND.

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial accuracy	T_A = 25°C, PWM or Dimming Lockout	72	80	88	KHz
Voltage stability	V_{CCZ} – 3V < V_{CC} < V_{CCZ} – 0.5V		1		%
Temperature stability			2		%
Total Variation	Line, temperature	68		92	KHz
Ramp Valley to Peak			2.5		V
C(T) Charging Current (FM Modes)	V_{PIN8} = 0V, V_{PIN9} = 2.5V, V_{PIN12} = 0.9V, Preheat		–94		µA
	V_{PIN8} = 0V, V_{PIN9} = 2.5V, Max. dimming		–188		µA
C(T) Discharge Current	V_{PIN8} = 0V, V_{PIN9} = 2.5V		5		mA
Output Drive Deadtime			0.2		µs
R(SET) Voltage			2.5		V
Reference Section					
Output Voltage	T_A = 25°C, I_O = 1mA	7.4	7.5	7.6	V
Line regulation	V_{CCZ} – 3V < V_{CC} , V_{CCZ} – 0.5V		2	10	mV
Load regulation	1mA < I_O < 20mA		2	15	mV
Temperature stability			0.4		%
Total Variation	Line, load, temp	7.35		7.65	V
Output Noise Voltage	10Hz to 10KHz		50		µV
Long Term Stability	T_J = 125°C, 1000 hrs		5		mV
Short Circuit Current	V_{CC} < V_{CCZ} – 0.5V, V_{REF} = 0V		–40		mA
Preheat and Interrupt Timer (Pin 10) (R(X) = 590KΩ, C(X) = 5.6µF)					
Initial Preheat Period			0.8		s
Subsequent Preheat Period			0.7		s
Start Period			2.1		s
Interrupt Period			6.3		s
Pin 12 Charging Current			–23		µA
Pin 12 Open Circuit Voltage	V_{CC} = 12.3V in UVLO	0.4	0.9	1.1	V
Pin 12 Maximum Voltage		7.0	7.3	7.7	V
Input Bias Current	V_{PIN12} = 1.2V		–0.1		µA
Preheat Lower Threshold			1.18		V
Preheat Upper Threshold			3.36		V
Interrupt Recovery Threshold			1.18		V
Start Period End Threshold			6.6		V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OVP/Inhibit Comparator (Pin 11)					
OVP Threshold		4.87	5.0	5.13	V
Hysteresis			0.5		V
Input Bias Current			-0.3	-2	µA
Propagation Delay			500		ns
Shutdown Threshold		6.36	6.7	7.04	V
Shutdown Hysteresis		0.7	1.2	1.7	V
PWM Comparator (PWM Mode)					
Start Period Duty Cycle		40	50	60	%
Outputs					
Output Voltage Low	I_{OUT} = 20mA		0.4	0.8	V
	I_{OUT} = 200mA		2.1	3.0	V
Output Voltage High	I_{OUT} = -20mA	V_{CC} - 2.5	V_{CC} - 1.9		V
	I_{OUT} = -200mA	V_{CC} - 3.0	V_{CC} - 2.2		V
Output Voltage Low in UVLO	I_{OUT} = 10mA, V_{CC} = 8V		0.8	1.5	V
Output Rise/Fall Time	C_L = 1000pF		50		ns
Under-Voltage Lockout and Bias Circuits					
IC Shunt Voltage (V_{CCZ})	I_{CC} = 25mA	12.8	13.5	14.2	V
V_{CCZ} Load Regulation	25mA < I_{CC} < 68mA		150	300	mV
V_{CCZ} Total Variation	Load, Temp	12.4		14.6	V
Start-up Current	$V_{CC} \leq$ 12.3V		1.3	1.7	mA
Operating Current	V_{CC} = V_{CCZ} - 0.5V		15	19	mA
Start-up Threshold			V_{CCZ} - 0.5		V
Shutdown Threshold			V_{CCZ} - 3.5		V
Shutdown Temperature (T_J)			120		°C
Hysteresis (T_J)			30		°C

FUNCTIONAL DESCRIPTION

OVERVIEW

The ML4830 consists of an Average Current controlled continuous boost Power Factor front end section with a flexible ballast control section. Start-up and lamp-out retry timing are controlled by the selection of external timing components, allowing for control of a wide variety of different lamp types. The ballast control section can be set up to adjust lamp power using either Pulse Width (PWM) or frequency modulation (FM). Either non-overlapping or overlapping conduction can be selected for the FM mode. This allows for the IC to be used with a variety of different ouput networks.

POWER FACTOR SECTION

The ML4830 Power Factor section is an average current sensing boost mode PFC control circuit which is architecturally similar to that found in the ML4821. For detailed information on this control architecture, please refer to Application Note 16 and the ML4821 data sheet.

MULTIPLIER

The ML4830 multiplier is a linear current input multiplier which provides high immunity to the disturbances caused by high power switching. The rectified line input sine wave is converted to a current via a dropping resistor. In this way, small amounts of ground noise produce an insignificant effect on the reference to the PWM comparator.

The output of the multiplier appears as a voltage across the 14K resistor (Figure 1) on the positive terminal of IA to form the reference for the current error amplifier. When the loop is in regulation, the negative voltage on IA+/I(LIM) (Pin 4) keeps the positive terminal of IA at 0V.

$$V_{MUL} \approx 0.034 \times I(SINE) \times (VEA - 1.1) \times (14K\Omega) \quad (1)$$

where: I(SINE) is the current in the dropping resistor,
V(EA) is the output of the error amplifier (Pin 20).

The output of the multiplier is limited to 0.88V.

AVERAGE CURRENT AND OUTPUT VOLTAGE REGULATION

The PWM regulator in the PFC Control section will act to offset the positive voltage caused by the multiplier output by producing an offsetting negative voltage on the current sense resistor at Pin 4. A cycle-by-cycle current limit is included to protect the MOSFET from high speed current transients. When the voltage at Pin 4 goes negative by more than 1V, the PFC cycle is terminated.

For more information on compensating the average current and boost voltage error amplifier loops, see Application Note 16 .

OVERVOLTAGE PROTECTION AND INHIBIT

The OVP/INHIBIT pin serves to protect the power circuit from being subjected to excessive voltages if the load should change suddenly (lamp removal). A divider from the high voltage DC bus (Figure 8: R14, R24) sets the OVP trip level. When the voltage on Pin 11 exceeds 5V, the PFC transistor is inhibited. The ballast section will continue to operate. If Pin 11 is driven above 6.8V, the IC is inhibited and goes into the low quiescent mode. The OVP threshold should be set to a level where the power components are safe to operate, but not so low as to interfere with the boost voltage regulation loop (R11, R12, R23).

BALLAST OUTPUT SECTION

The IC controls output power to the lamps in one of three different modes. The Mode pin (Pin 8) sets the operating mode of the IC. With Pin 8 at GND, the output section is in the Frequency Modulation mode with non-overlapping conduction, which means that both ballast output drivers will be low during t_{DIS} (Figure 2). In the overlapping mode (VCO-O), Pin 8 is left open and the transition from OUT A high to OUT B high occurs with no dead time. This mode is typically used in current fed ballast topologies.

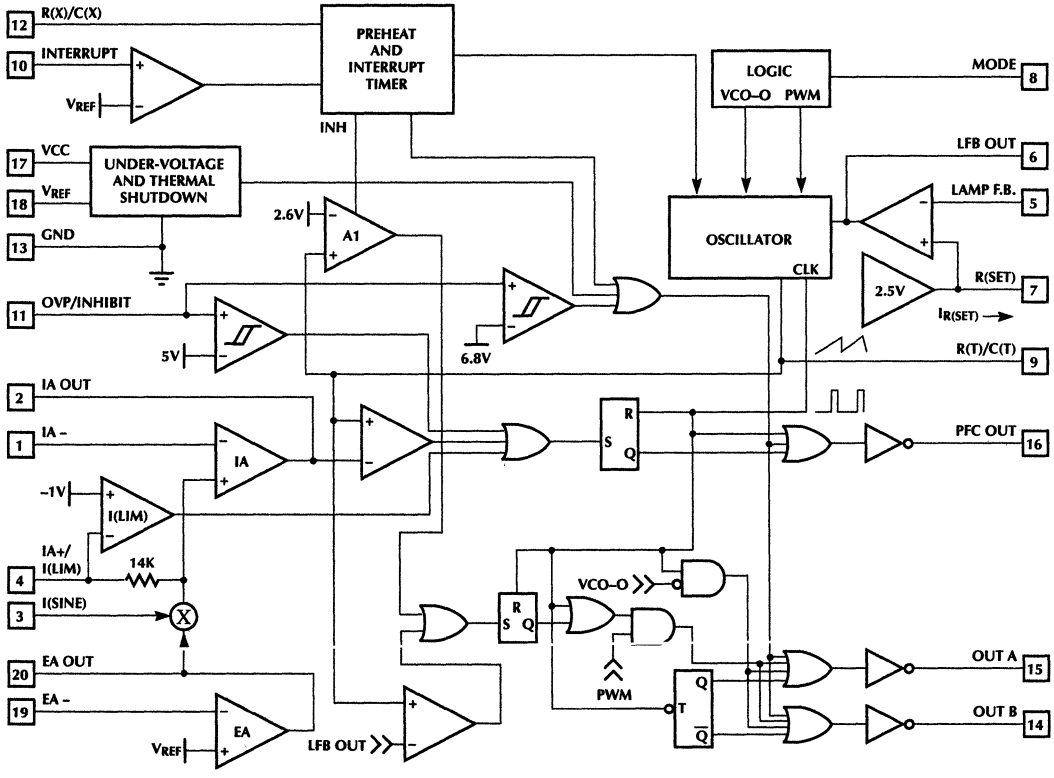


Figure 1. ML4830 Block Diagram

Mode	Pin 8	Definition
VCO	GND	Frequency Modulation
VCO-O	OPEN	Overlapping VCO F.M.
PWM	VREF	Pulse Width Modulation

Table 1. ML4830 Operating Modes

OSCILLATOR

In Table 1 above, the two VCO frequency ranges are controlled by the output of the LFB amplifier (Pin 6). As lamp current decreases, Pin 6 rises in voltage, causing the C(T) charging current to decrease, thereby causing the oscillator frequency to decrease. Since the ballast output network attenuates high frequencies, the power to the lamp will be increased.

In PWM Mode, I_{CHG} is 0 so the oscillator's frequency is set per (1) below.

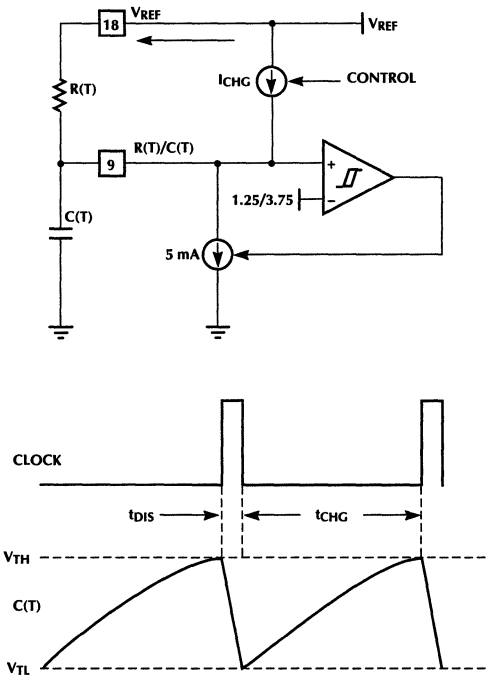


Figure 2. Oscillator Block Diagram and Timing

Also, in both VCO modes, the when LFB OUT is high, I_{CHG} = 0 and the minimum frequency occurs. The charging current varies according to two control inputs to the oscillator:

1. The output of the preheat timer
2. The voltage at Pin 6 (lamp current output)

In preheat condition, charging current is fixed at

$$I_{CHG(PREHEAT)} = \frac{2.5}{R(SET)} \quad (1)$$

In running mode, charging current decreases as the V_{PIN7} rises from 0V to V_{OH} of trhe LAMP FB amplifier. The highest frequency will be attained when I_{CHG} is highest, which is attained when V_{PIN6} is at 0V:

$$I_{CHG(0)} = \frac{5}{R(SET)} \quad (2)$$

The oscillator frequency is determined by the following equations:

$$F_{OSC} = \frac{1}{t_{CHG} + t_{DIS}} \quad (3)$$

and

$$t_{CHG} = R_T C_T \ln\left(\frac{6.25 + I_{CHG} R_T}{3.75 + I_{CHG} R_T}\right) \quad (4)$$

The oscillator's minimum frequency is set when I_{CHG} = 0 where:

$$F_{OSC} \cong \frac{1}{0.51 \times R_T C_T} \quad (5)$$

This assumes that $t_{CHG} >> t_{DIS}$.

Highest lamp power, and lowest output frequency are attained when V_{PIN6} is at its maximum output voltage (V_{OH}).

In this condition, the minimum operating frequency of the ballast is set per (5) above.

For the IC to be used effectively in dimming ballasts with higher Q output networks a larger C_T value and lower R_T value can be used, to yield a smaller frequency excursion over the control range (V_{PIN6}). The discharge current is set to 5mA. Assuming that $I_{DIS} >> I_{RT}$:

$$t_{DIS(VCO)} \cong 490 \times C_T \quad (6)$$

IC BIAS, UNDER-VOLTAGE LOCKOUT AND THERMAL SHUTDOWN

The IC includes a shunt regulator which will limit the voltage at VCC to 13.5 (V_{CCZ}). The IC should be fed with a current limited source, typically derived from the ballast transformer auxiliary winding. When VCC is below V_{CCZ} – 0.7V, the IC draws less than 1.7mA of quiescent current and the outputs are off. This allows the IC to start using a "bleed resistor" from the rectified AC line.

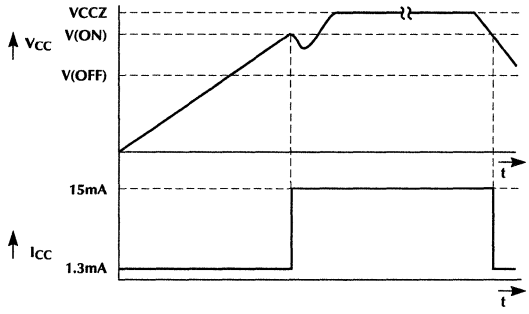


Figure 3. Typical V_{CC} and I_{CC} waveforms when ML4830 is started with a bleed resistor from the rectified AC line and bootstrapped from the ballast transformer.

To help reduce ballast cost, the ML4830 includes a temperature sensor which will inhibit ballast operation if the IC's junction temperature exceeds 120°C. In order to use this sensor in lieu of an external sensor, care should be taken when placing the IC to ensure that it is sensing temperature at the physically appropriate point in the ballast. The ML4830's die temperature can be estimated with the following equation:

$$T_J \cong T_A \times P_D \times 65°C/W \qquad (7)$$

STARTING, RE-START, PREHEAT AND INTERRUPT

The lamp starting scenario implemented in the ML4830 is designed to maximize lamp life and minimize ballast heating during lamp out conditions.

The circuit in Figure 4 controls the lamp starting scenarios: Filament preheat and Lamp Out interrupt. C(X) is charged with a current of $\frac{I_{R(SET)}}{4}$ or $\frac{0.625}{R(SET)}$ and discharged through R(X). The voltage at C(X) is initialized to 0.7V (V_{BE}) at power up. The time for C(X) to rise to 3.4V is the filament preheat time. During that time, the oscillator charging current (I_{CHG}) is $\frac{2.5}{R(SET)}$ in both VCO modes.

This will produce a high frequency (or low duty cycle) for filament preheat, but will not produce sufficient voltage to ignite the lamp.

After cathode heating, the inverter frequency drops to F_{MIN} causing a high voltage to appear to ignite the lamp. If the voltage does not drop when the lamp is supposed to have ignited, the lamp voltage feedback coming into Pin 10 rises to above V_{REF}, the C(X) charging current is shut off and the inverter is inhibited until C(X) is discharged by R(X) to the 1.2V threshold. Shutting off the inverter in this manner prevents the inverter from generating excessive heat when the lamp fails to strike or is out of socket. Typically this time is set to be fairly long by choosing a large value of R(X).

LFB OUT is ignored until C(X) reaches 6.8V threshold. The lamps are therefore driven to full power and then dimmed. The C(X) pin is clamped to about 7.5V.

A timing diagram of lamp ignition and restart sequences provided by the circuit of Figure 4 is given in Figure 7.

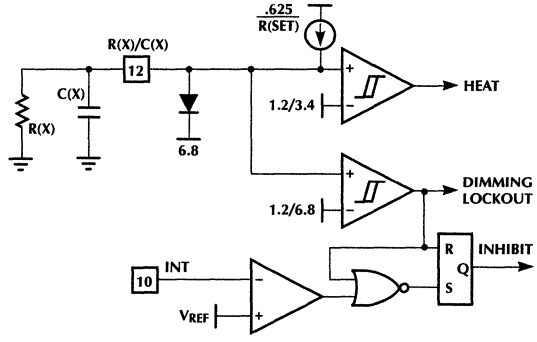


Figure 4. Lamp Preheat and Interrupt Timers

Mode	PWM	FM
Preheat	50%	$\frac{[F(MAX) \text{ to } F(MIN)]}{2}$
Dimming Lock-out	D(MAX)%	F(MIN)
Dimming Control	0 to D(MAX)%	F(MIN) to F(MAX)

Figure 5. Lamp Starting Summary

A summary of the lamp starting scenarios are given in figure 5 for both PWM and Frequency Modulation modes. The PWM duty cycle is defined as:

$$\text{Duty Cycle} = \frac{t_{ON}}{t_{CLK}}$$

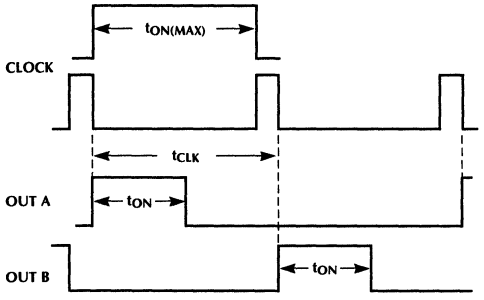


Figure 6. Definition of Duty Cycles

SEMI-STANDARD CAPABILITIES

The ML4830 is designed to work in a wide variety of electronic ballast applications. For high volume, cost sensitive applications, a ballast design can be implemented and debugged using the ML4830. From that design, Micro Linear can produce a reduced feature set, optimized ballast IC design quickly and easily with low risk.

Contact your Micro Linear representative or call Micro Linear for more information on Semi-Standard options.

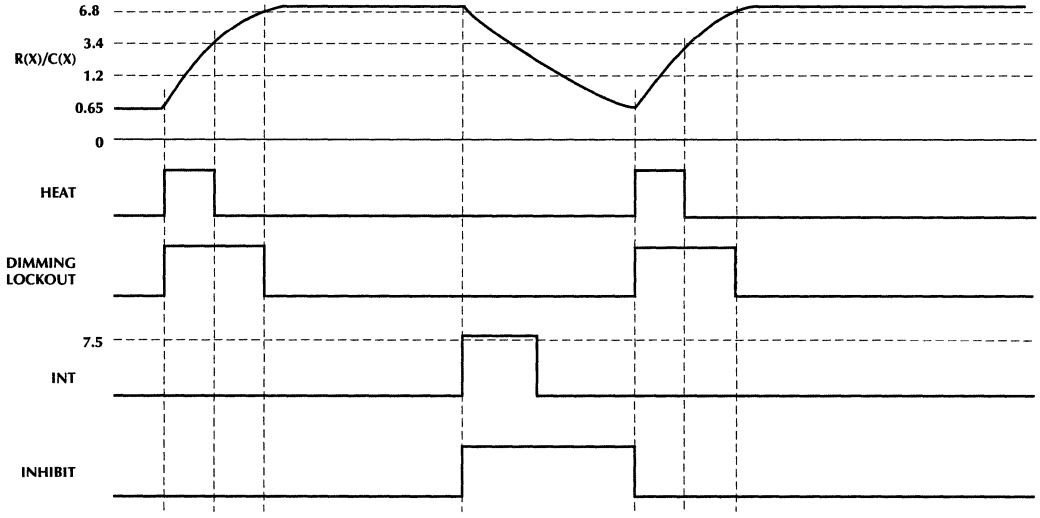


Figure 7. Lamp Starting and Restart Timing

APPLICATIONS

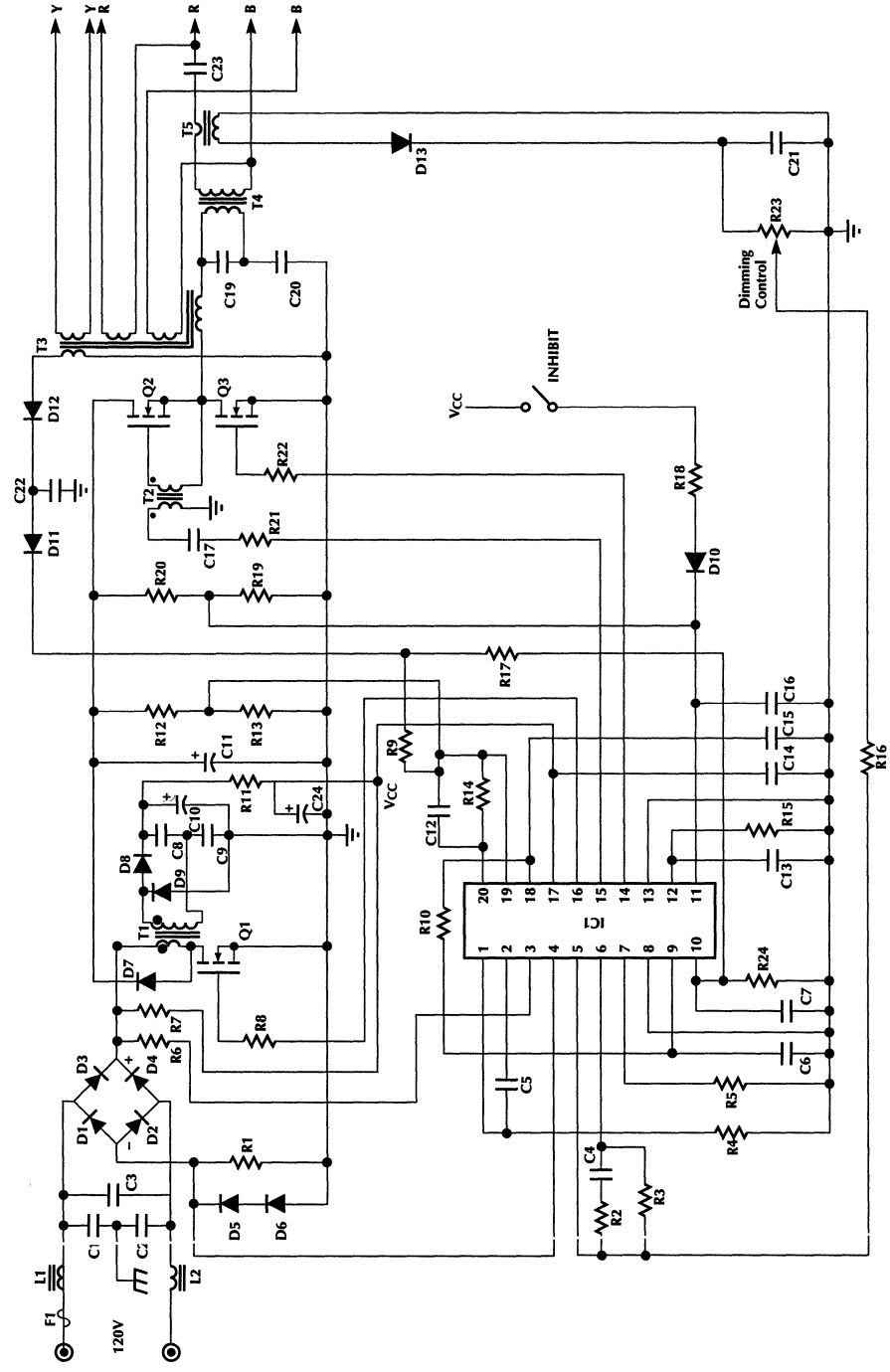


Figure. 8 Typical Application: 2-Lamp Isolated Dimming Ballast with Active Power Factor Correction for 120VAC Input

APPLICATIONS (continued)

The schematic (Figure 8) and the bill of materials on the following pages represents a complete parts list for the schematic (Figure 8). Designators refer to Micro Linear's "rev B" PCB.

TABLE 1: PARTS LIST FOR THE ML4830 TYPICAL APPLICATION

QTY.	REF.	DESCRIPTION	MFR.	PART NUMBER
CAPACITORS				
2	C1, 2	3.3nF, 125VAC, 10%, ceramic, "Y" capacitor	Panasonic	ECK-DNS332ME
1	C3	0.33µF, 250VAC, "X", capacitor	Panasonic	ECQ-U2A334MV
4	C4, 8, 9, 12, 22	0.1µF, 50V, 10%, ceramic capacitor	AVX	SR215C104KAA
1	C5	47nF, 50V, 10%, ceramic capacitor	AVX	SR211C472KAA
1	C6	1.5µF, 50V, 2.5%, NPO ceramic capacitor	AVX	RPE121COG152
2	C7	1µF, 50V, 20%, ceramic capacitor	AVX	SR305E105MAA
1	C10	100µF, 25V, 20%, electrolytic capacitor	Panasonic	ECE-A1EFS101
1	C11	100µF, 250V, 20%, electrolytic capacitor	Panasonic	ECE-S2EG101E
1	C13	4.7µF, 50V, 20%, electrolytic capacitor	Panasonic	ECE-A50Z4R7
3	C14, 15, 17	0.22µF, 50V, 10%, ceramic capacitor	AVX	SR305C224KAA
1	C16	1.5µF, 50V, 10%, ceramic capacitor	AVX	SR151V152KAA
1	C19	22nF, 630V, 5%, polypropylene capacitor	WIMA	MKP10, 22nF, 630V, 5%
1	C20	0.1µF, 250V, 5%, polypropylene capacitor	WIMA	MKP10, 0.1µF, 250V, 5%
1	C21	0.01µF, 50V, 10%, ceramic capacitor	AVX	SR211C103KAA
1	C24	220µF, 16V, 20%, electrolytic capacitor	Panasonic	ECE-A16Z220
RESISTORS:				
1	R1	0.5Ω, 5%, 1/2W, metal film resistor	NTE	
1	R2	4.3K, 1/4W, 5%, carbon film resistor	Yageo	4.3K-Q
1	R3	47K, 1/4W, 5%, carbon film resistor	Yageo	47K-Q
1	R4	12K, 1/4W, 5%, carbon film resistor	Yageo	12K-Q
1	R5	20K, 1/4W, 1%, metal film resistor	Dale	SMA4-20K-1
1	R6	360K, 1/4W, 5%, carbon film resistor	Yageo	360K-Q
1	R7	36K, 1W, 5%, carbon film resistor	Yageo	36KW-1-ND
3	R8, 22, 11	22Ω, 1/4W, 5%, carbon film resistor	Yageo	22-Q
1	R9	402K, 1/4W, 1%, metal film resistor	Dale	SMA4-402K-1
1	R10, 13	17.8K, 1/4W, 1%, metal film resistor	Dale	SMA4-17.8K-1
1	R12, 20	475K, 1/4W, 1%, metal film resistor	Dale	SMA4-475K-1

TABLE 1: PARTS LIST FOR ML4830 TYPICAL APPLICATION (Continued)

RESISTORS: (Continued)

QTY.	REF.	DESCRIPTION	MFR.	PART NUMBER
4	R14	100K, 1/4W, 5%, carbon film resistor	Yageo	100K-Q
1	R15	681K, 1/4W, 5%, carbon film resistor	Yageo	681K-Q
1	R16, 19	10K, 1/4W, 1%, metal film resistor	Dale	SMA4-10K-1
1	R18	4.7K, 1/4W, 5%, carbon film resistor	Tageo	681K-Q
1	R21	33Ω, 1/4W, 5%, carbon film resistor	Yageo	33-Q
1	R23	25K, pot (for dimming adjustment)	Bourns	3386P-253-ND
DIODES:				
4	D1, 2, 3, 4	1A, 600V, 1N4007 diode (or 1N5061 as a substitute)	Motorola	1N4007TR
2	D5, 6	1A, 50V (or more), 1N4001 diodes	Motorola	1N4001TR
1	D7	3A, 400V, BYV26C or BYT03 400 fast recovery or MUR440 Motorola ultra Fast diode	GI	BYV26C
6	D8, 9, 10, 11 12, 13	0.1A, 75V, 1N4148 signal diode	Motorola	1N4148TR
IC's:				
1	IC1	ML4830, Electronic Ballast Controller IC	Micro Linear	ML4830CP
TRANSISTORS:				
3	Q1, 2, 3	3.3A, 400V, IRF720 power MOSFET	IR	IR720
MAGNETICS:				
1	T1	T1 Boost Inductor, E24/25, 1mH, Custom Coils P/N 5039 or Coiltronics P/N CTX05-12538-1 E24/25 core set, TDK PC40 material 8-pin vertical bobbin (Cosmo #4564-3-419), Wind as follows: 195 turns 25AWG magnet wire, start pin #1, end pin #4 1 layer mylar tape 14 turns 26AWG magnet wire, start pin #3, end pin #2 NOTE: Gap for 1mH ±5%		
1	T2	T2 Gate Drive Xfmr, L_{PRI} = 3mH, Custom Coils P/N 5037 or Coiltronics P/N CTX05-12539-1 Toroid Magnetics YW-41305-TC Wind as follows: Primary = 25 turns 30AWG magnet wire, start pin #1, end pin #4 Secondary = 50 turns 30AWG magnet wire, start pin #5, end pin #8		

TABLE 1: PARTS LIST FOR ML4830 TYPICAL APPLICATION (Continued)

QTY.	REF.	DESCRIPTION	MFR.	PART NUMBER
MAGNETICS: (Continued)				
1	T3	T3 Inductor, L_{PRI} = 1.66mH, Custom Ciols P/N 5041 or Coiltronics P/N CTX05-12547-1 E24/25 core set, TDK PC40 material 10 pin horizontal bobbin (Plastron #0722B-31-80) Wind as follows: 1st: 170T of 25AWG magnet wire; start pin #10, end pin #9. 1 layer of mylar tape 2nd: 5T of #32 magnet wire; start pin #2, end pin #1 1 layer of mylar tape 3rd: 3T of #30 Kynar coated wire; start pin #4, end pin #5 4th: 3T of #30 Kynar coated wire; start pin #3, end pin #6 5th: 3T of #30 Kynar coated wire; start pin #7, end pin #8 NOTE: Gap for 1.66mH ±5% (pins 9 to 10)		
1	T4	T4 Power Xfmr, L_{PRI} = 3.87mH, Custom Ciols P/N 5038 or Coiltronics P/N CTX05-12545-1 E24/25 core set, TDK PC40 material 8 pin vertical bobbin (Cosmo #4564-3-419) Wind as follows: 1st: 200T of 30AWG magnet wire; start pin #1, end pin #4. 1 layer of mylar tape 2nd: 300T of 32AWG magnet wire; start pin #5, end pin #8 NOTE: Gap for inductance primary: (pins 1 to 4) @ 3.87mH ±5%		
1	T5	T5 Current Sense Inductor, Custom Coils P/N 5040 or Coiltronics P/N CTX05-12546-1 Toroid Magnetics YW-41305-TC Wind as follows: Primary = 3T 30AWG magnet coated wire, start pin #1, end pin #4 Secondary = 400T 35AWG magnet wire, start pin #5, end pin #8		
INDUCTORS:				
2	L1, 2	EMI/RFI Inductor, 600µH, DC resistance = 0.45Ω	Prem. Magnetics	SPE116A
FUSES:				
1	F1	2A fuse, 5 x 20mm miniature	Littlefuse	F948-ND
2		Fuse Clips, 5 x 20mm, PC Mount		F058-ND
HARDWARE:				
1		Single TO-220 Heatsink	Aavid Eng.	PB1ST-69
2		Double TO-220 Heatsink	IERC	PSE1-2TC
3		MICA Insulators	Keystone	4673K-ND

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4830CP	0°C to + 85°C	Molded DIP (P20)
ML4830CS	0°C to +85°C	Molded SOIC (S20)

ML4831

Electronic Ballast Controller

GENERAL DESCRIPTION

The ML4831 is a complete solution for a dimmable, high power factor, high efficiency electronic ballast. Contained in the ML4831 are controllers for "boost" type power factor correction as well as for a dimming ballast.

The Power factor circuit uses the average current sensing method with a current fed multiplier and over-voltage protection. This system produces power factors of better than 0.99 with low input current THD at > 95% efficiency. Special care has been taken in the design of the ML4831 to increase system noise immunity by using a high amplitude oscillator, and a current fed multiplier. An over-voltage protection comparator inhibits the PFC section in the event of a lamp out or lamp failure condition.

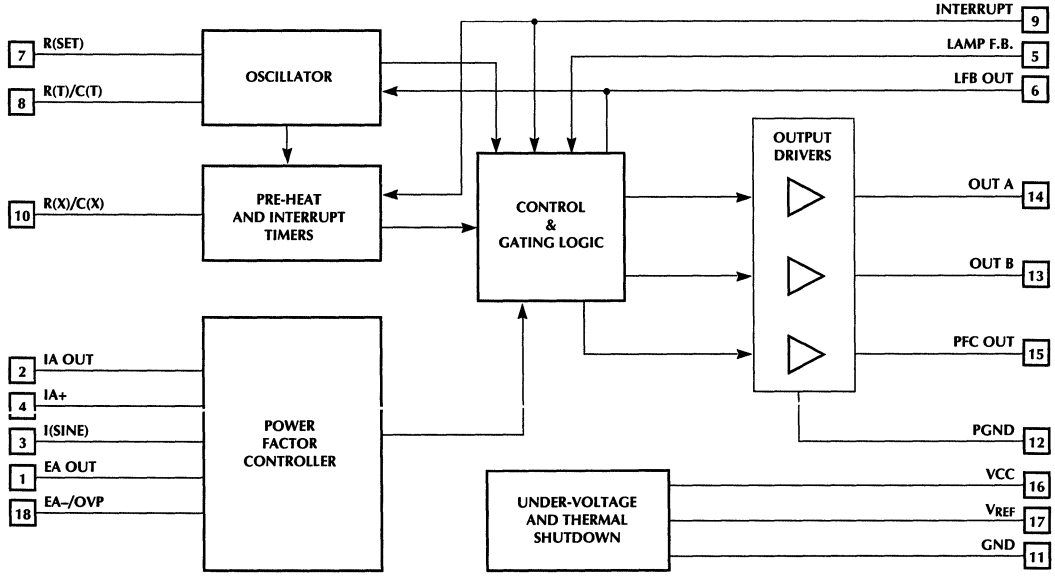
The ballast section provides for programmable starting scenarios with programmable preheat and lamp out-of-socket interrupt times. The IC controls lamp output through either frequency modulation using lamp current feedback.

The ML4831 is designed using Micro Linear's Semi-Standard tile array technology. Customized versions of this IC, optimized to specific ballast architectures can be made available. Contact Micro Linear or an authorized representative for more information.

FEATURES

- Complete Power Factor Correction and Dimming Ballast Control on one IC
- Low Distortion, High Efficiency Continuous Boost, Average Current sensing PFC section
- Programmable Start Scenario for Rapid or Instant Start Lamps
- Lamp Current feedback for Dimming Control
- Variable Frequency dimming and starting
- Programmable Restart for lamp out condition to reduce ballast heating
- Over-Temperature Shutdown replaces external heat sensor for safety
- PFC Over-Voltage comparator eliminates output "runaway" due to load removal
- Large oscillator amplitude and current fed multiplier improves noise immunity

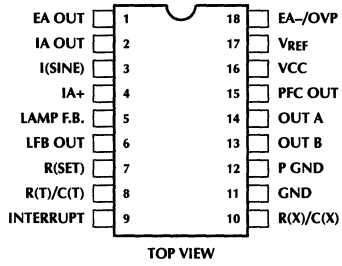
BLOCK DIAGRAM



PIN CONFIGURATION

ML4831

18-Pin DIP (P18)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	EA OUT	PFC Error Amplifier output and compensation node
2	IA OUT	Output and compensation node of the PFC average current transconductance amplifier.
3	I(SINE)	PFC Current Multiplier input.
4	IA+	Non-inverting input of the PFC average current transconductance amplifier and peak current sense point of the PFC cycle by cycle current limit comparator.
5	LAMP F.B.	Inverting input of an Error Amplifier used to sense (and regulate) lamp arc current. Also the input node for dimming control.
6	LFB OUT	Output from the Lamp Current Error Transconductance Amplifier used for lamp current loop compensation
7	R(SET)	External resistor which sets oscillator F_{MAX}, and R(X)/C(X) charging current
8	R(T)C(T)	Oscillator timing components
9	INTERRUPT	Input used for lamp-out detection and restart. A voltage greater than 7.5 volts resets the chip and causes a restart after a programmable interval.
10	R(X)/C(X)	Sets the timing for the preheat, dimming lockout, and interrupt
11	GND	Ground
12	P GND	Power ground for the IC
13	OUT B	Ballast MOSFET drive output
14	OUT A	Ballast MOSFET drive output
15	PFC OUT	Power Factor MOSFET drive output
16	VCC	Positive Supply for the IC
17	V_{REF}	Buffered output for the 7.5V voltage reference
18	EA–/OVP	Inverting input to PFC error amplifier and OVP comparator input

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 75mA
Output Current, Source or Sink (Pins 13, 14, 15)
DC 250mA
Output Energy (capacitive load per cycle)..... 1.5 mJ
Multiplier I(SINE) Input (Pin 3) ..... 10 mA
Analog Inputs (Pins 5, 9, 18) ..... –0.3V to VCC –2V
Pin 4 input voltage ..... –3V to +2V
Maximum Forced Voltage (Pins 1, 6) ..... –0.3V to 7.7V
Maximum Forced Current (Pins 1, 2, 6) ..... ±20mA
Maximum Forced Voltage (Pin 2) ..... –0.3V to 6V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 Sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP–P ..... 70°C/W

OPERATING CONDITIONS

Temperature Range
ML4831C ..... 0°C to 85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R(SET) = 31.6K, R(T) = 16.2K, C(T) = 1.5nF, T_J = Junction Operating Temperature Range, I_{CC} = 25mA

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PFC Current Sense Amplifier (Pins 2, 4)					
Small Signal Transconductance		130	200	270	µmhos
Input Voltage Range		–0.3		3.5	V
Output Low	I_{SINE} = 0mA, V_{PIN1} = 0V, V_{PIN4} = –0.3V, R_L = ∞		0.2	0.4	V
Output High	I_{SINE} = 1.5mA, $V_{PIN18/4}$ = 0V, R_L = ∞	5.2	5.6	6	V
Source Current	I_{SINE} = 1.5mA, $V_{PIN18/4}$ = 0V, V_{PIN2} = 5V		–0.3		mA
Sink Current	I_{SINE} = 0mA, V_{PIN2} = 0.3V, V_{PIN4} = –0.3V, V_{PIN1} = 0V		0.3		mA
PFC Voltage Feedback Amplifier (Pins 1, 18)/Lamp Current Amplifier (Pins 5, 6)					
Input Offset Voltage			±3.0	±10.0	mV
Input Bias Current			–0.3	–1.0	µA
Small Signal Transconductance		50	80	110	µmhos
Input Voltage Range		–0.3		3.5	V
Output Low	$V_{PIN5/18}$ = 3V, R_L = ∞		0.2	0.4	V
Output High	$V_{PIN5/18}$ = 2V, R_L = ∞	7.2	7.5		V
Source Current	$V_{PIN5/18}$ = 0V, $V_{PIN1/6}$ = 7V		–0.2		mA
Sink Current	$V_{PIN5/18}$ = 5V, $V_{PIN1/6}$ = 0.3V		0.2		mA
Multiplier					
Output Voltage	I_{SINE} = 100µA, V_{PIN1} = 3V		40		mV
	I_{SINE} = 300µA, V_{PIN1} = 3V		130		mV
	I_{SINE} =100µA, V_{PIN1} = 6V		112		mV
	I_{SINE} = 300µA, V_{PIN1} = 6V		350		mV
Output Voltage Limit	I_{SINE} = 1.5mA, V_{PIN18} = 0V		865		mV
Offset Voltage	I_{SINE} = 0, V_{PIN18} = 0V			15	mV
	I_{SINE} = 150µA, V_{PIN18} = 3V			15	mV
I(SINE) Input Voltage	I_{SINE} = 200µA	0.8	1.4	1.8	V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial accuracy	T_A = 25°C	72	76	80	KHz
Voltage stability	V_{CCZ} – 3V < V_{CC} <V_{CCZ} – 0.5V		1		%
Temperature stability			2		%
Total Variation	Line, temperature	69		83	KHz
Ramp Valley to Peak			2.5		V
C(T) Charging Current (FM Modes)	V_{PIN5} = 3V, V_{PIN8} = 2.5V, V_{PIN10} = 0.9V (Preheat)		–78		µA
	V_{PIN5} = 3V, V_{PIN8} = 2.5V, V_{PIN10} = Open		–156		µA
C(T) Discharge Current	V_{PIN8} = 2.5V		5		mA
Output Drive Deadtime			0.75		µs
Reference Section					
Output Voltage	T_A = 25°C, I_O = 1mA	7.4	7.5	7.6	V
Line regulation	V_{CCZ} – 3V < V_{CC} < V_{CCZ} – 0.5V		2	10	mV
Load regulation	1mA < I_O < 20mA		2	15	mV
Temperature stability			0.4		%
Total Variation	Line, load, temp	7.35		7.65	V
Output Noise Voltage	10Hz to 10KHz		50		µV
Long Term Stability	T_J = 125°C, 1000 hrs		5		mV
Short Circuit Current	V_{CC} < V_{CCZ} – 0.5V, V_{REF} = 0V		–40		mA
Preheat and Interrupt Timer (Pin 10) (R(X) = 590KΩ, C(X) = 5.6µF)					
Initial Preheat Period			0.8		s
Subsequent Preheat Period			0.7		s
Start Period			2.1		s
Interrupt Period			6.3		s
Pin 10 Charging Current			–19		µA
Pin 10 Open Circuit Voltage	V_{CC} = 12.3V in UVLO	0.4	0.9	1.1	V
Pin 10 Maximum Voltage		7.0	7.3	7.7	V
Input Bias Current	V_{PIN10} = 1.2V		–0.2		µA
Preheat Lower Threshold			1.18		V
Preheat Upper Threshold			3.36		V
Interrupt Recovery Threshold			1.18		V
Start Period End Threshold			6.7		V
Interrupt Input (Pin 9)					
Interrupt Threshold		7.35	7.5	7.65	V
Input Bias Current			–0.3	–1	µA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OVP Comparator (Pin 18)					
OVP Threshold		2.6	2.7	2.8	V
Hysteresis			0.25		V
Propagation Delay			500		ns
Outputs					
Output Voltage Low	I_{OUT} = 20mA		0.4	0.8	V
	I_{OUT} = 200mA		2.1	3.0	V
Output Voltage High	I_{OUT} = –20mA	V_{CC} – 2.5	V_{CC} – 1.9		V
	I_{OUT} = –200mA	V_{CC} – 3.0	V_{CC} – 2.2		V
Output Voltage Low in UVLO	I_{OUT} = 10mA, V_{CC} = 8V		0.8	1.5	V
Output Rise/Fall Time	C_L = 1000pF		50		ns
Under-Voltage Lockout and Bias Circuits					
IC Shunt Voltage (V_{CCZ})	I_{CC} = 25mA	12.8	13.5	14.2	V
V_{CCZ} Load Regulation	25mA < I_{CC} < 68mA		150	300	mV
V_{CCZ} Total Variation	Load, Temp	12.4		14.6	V
Start-up Current	$V_{CC} \leq$ 12.3V		1.3	1.7	mA
Operating Current	$V_{CC} = V_{CCZ}$ – 0.5V		15	19	mA
Start-up Threshold			V_{CCZ} – 0.5		V
Shutdown Threshold			V_{CCZ} – 3.5		V
Shutdown Temperature (T_J)			120		°C
Hysteresis (T_J)			30		°C

FUNCTIONAL DESCRIPTION

OVERVIEW

The ML4831 consists of an Average Current controlled continuous boost Power Factor front end section with a flexible ballast control section. Start-up and lamp-out retry timing are controlled by the selection of external timing components, allowing for control of a wide variety of different lamp types. The ballast section controls the lamp power using frequency modulation (FM) with additional programmability provided to adjust the VCO frequency range. This allows for the IC to be used with a variety of different output networks.

POWER FACTOR SECTION

The ML4831 Power Factor section is an average current sensing boost mode PFC control circuit which is architecturally similar to that found in the ML4821. For detailed information on this control architecture, please refer to Application Note 16 and the ML4821 data sheet.

MULTIPLIER

The ML4831 multiplier is a linear current input multiplier which provides high immunity to the disturbances caused by high power switching. The rectified line input sine wave is converted to a current via a dropping resistor. In this way, small amounts of ground noise produce an insignificant effect on the reference to the PWM comparator.

The output of the multiplier appears on the positive terminal of the IA amplifier to form the reference for the current error amplifier. Please refer to Figure 1.

$$V_{MUL} \approx \frac{[I(SINE) \times (VEA - 1.1V)]}{4.17mA} \quad (1)$$

where: I(SINE) is the current in the dropping resistor,
V(EA) is the output of the error amplifier (Pin 1).

The output of the multiplier is limited to 1.0V.

AVERAGE CURRENT AND OUTPUT VOLTAGE REGULATION

The PWM regulator in the PFC Control section will act to offset the positive voltage caused by the multiplier output by producing an offsetting negative voltage on the current sense resistor at Pin 4. A cycle-by-cycle current limit is included to protect the MOSFET from high speed current transients. When the voltage at Pin 4 goes negative by more than 1V, the PWM cycle is terminated.

For more information on compensating the average current and boost voltage error amplifier loops, see ML4821 data sheet.

OVERVOLTAGE PROTECTION AND INHIBIT

The OVP pin serves to protect the power circuit from being subjected to excessive voltages if the load should change suddenly (lamp removal). A divider from the high voltage DC bus sets the OVP trip level. When the voltage on Pin 18 exceeds 2.75V, the PFC transistors are inhibited. The ballast section will continue to operate. The OVP threshold should be set to a level where the power components are safe to operate, but not so low as to interfere with the boost voltage regulation loop.

TRANSCONDUCTANCE AMPLIFIERS

The PFC voltage feedback, PFC current sense, and the loop current amplifiers are all implemented as operational transconductance amplifiers. They are designed to have low small signal forward transconductance such that a large value of load resistor (R1) and a low value ceramic capacitor (<1µF) can be used for AC coupling (C1) in the frequency compensation network. The compensation network shown in Figure 2 will introduce a zero and a pole at:

$$f_Z = \frac{1}{2\pi R_1 C_1} \qquad f_P = \frac{1}{2\pi R_1 C_2} \qquad (2)$$

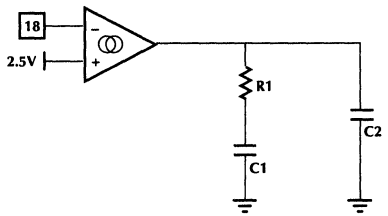


Figure 2. Compensation Network

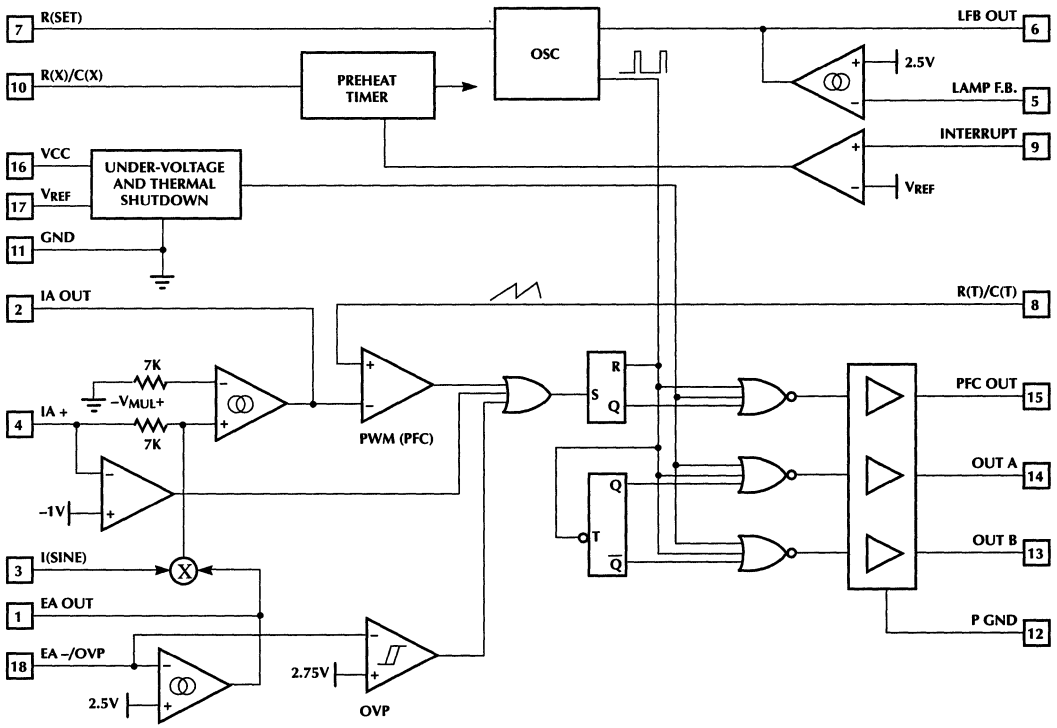


Figure 1. ML4831 Block Diagram

Figure 3 shows the output configuration for the operational transconductance amplifiers.

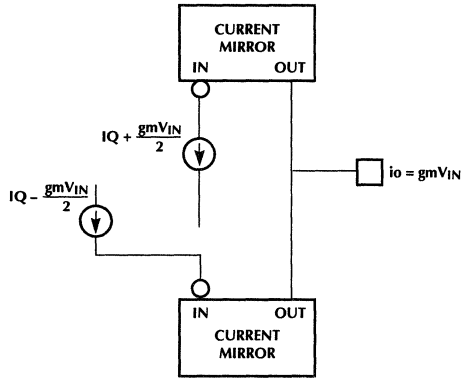


Figure 3. Output Configuration

A DC path to ground or VCC at the output of the transconductance amplifiers will introduce an offset error. The magnitude of the offset voltage that will appear at the input is given by V_{OS} = io/gm. For a io of 1uA and a gm of 0.08 µmhos the input referred offset will be 12.5mV. Capacitor C1 as shown in Figure 2 is used to block the DC current to minimize the adverse effect of offsets.

Slew rate enhancement is incorporated into all of the operational transconductance amplifiers in the ML4831. This improves the recovery of the circuit in response to power up and transient conditions. The response to large signals will be somewhat non-linear as the transconductance amplifiers change from their low to high transconductance mode. This is illustrated in Figure 4.

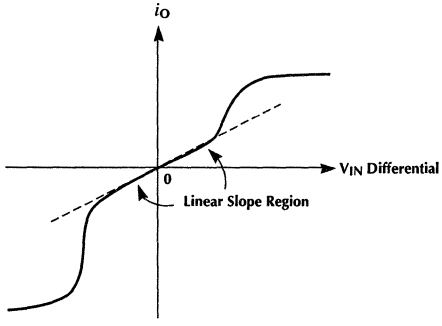


Figure 4. Transconductance Amplifier Characteristics

BALLAST OUTPUT SECTION

The IC controls output power to the lamps via frequency modulation with non-overlapping conduction. This means that both ballast output drivers will be low during the discharging time t_{DIS} of the oscillator capacitor C_T.

OSCILLATOR

The VCO frequency ranges are controlled by the output of the LFB amplifier (Pin 6). As lamp current decreases, Pin 6 rises in voltage, causing the C(T) charging current to decrease, thereby causing the oscillator frequency to decrease. Since the ballast output network attenuates high frequencies, the power to the lamp will be increased.

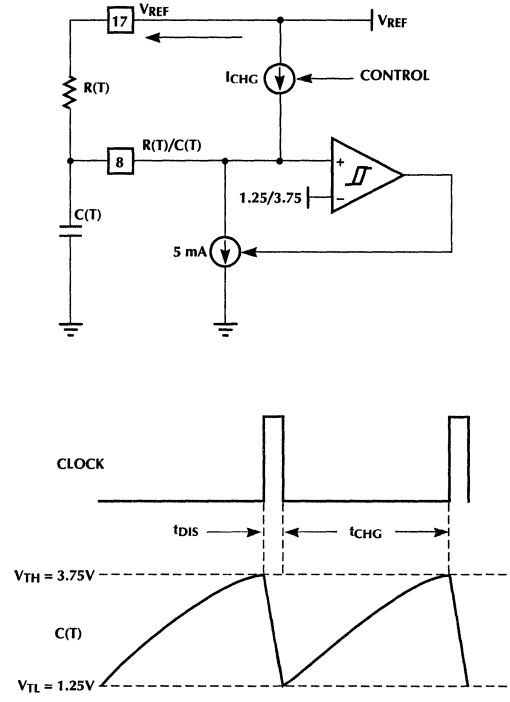


Figure 5. Oscillator Block Diagram and Timing

The oscillator frequency is determined by the following equations:

$$F_{OSC} = \frac{1}{t_{CHG} + t_{DIS}} \qquad (3)$$

and

$$t_{CHG} = R_T C_T \ln\left(\frac{V_{REF} + I_{CH} R_T - V_{TL}}{V_{REF} + I_{CH} R_T - V_{TH}}\right) \qquad (4)$$

The oscillator's minimum frequency is set when $I_{CH} = 0$ where:

$$F_{OSC} \cong \frac{1}{0.51 \times R_T C_T} \quad (5)$$

This assumes that $t_{CHG} >> t_{DIS}$.

When LFB OUT is high, $I_{CH} = 0$ and the minimum frequency occurs. The charging current varies according to two control inputs to the oscillator:

1. The output of the preheat timer
2. The voltage at Pin 6 (lamp feedback amplifier output)

In preheat condition, charging current is fixed at

$$I_{CHG(PREHEAT)} = \frac{2.5}{R(SET)} \quad (6)$$

In running mode, charging current decreases as the V_{PIN6} rises from 0V to V_{OH} of the LAMP FB amplifier. The highest frequency will be attained when I_{CHG} is highest, which is attained when V_{PIN6} is at 0V:

$$I_{CHG(0)} = \frac{5}{R(SET)} \quad (7)$$

Highest lamp power, and lowest output frequency are attained when V_{PIN6} is at its maximum output voltage (V_{OH}).

In this condition, the minimum operating frequency of the ballast is set per (5) above.

For the IC to be used effectively in dimming ballasts with higher Q output networks a larger C_T value and lower R_T value can be used, to yield a smaller frequency excursion over the control range (V_{PIN6}). The discharge current is set to 5mA. Assuming that $I_{DIS} >> I_{RT}$:

$$t_{DIS(VCO)} \cong 490 \times C_T \quad (8)$$

IC BIAS, UNDER-VOLTAGE LOCKOUT AND THERMAL SHUTDOWN

The IC includes a shunt regulator which will limit the voltage at V_{CC} to 13.5 (V_{CCZ}). The IC should be fed with a current limited source, typically derived from the ballast transformer auxiliary winding. When V_{CC} is below V_{CCZ} – 0.7V, the IC draws less than 1.7mA of quiescent current and the outputs are off. This allows the IC to start using a "bleed resistor" from the rectified AC line.

To help reduce ballast cost, the ML4831 includes a temperature sensor which will inhibit ballast operation if the IC's junction temperature exceeds 120°C. In order to use this sensor in lieu of an external sensor, care should be taken when placing the IC to ensure that it is sensing temperature at the physically appropriate point in the ballast. The ML4831's die temperature can be estimated with the following equation:

$$T_J \cong T_A \times P_D \times 65°C/W \quad (9)$$

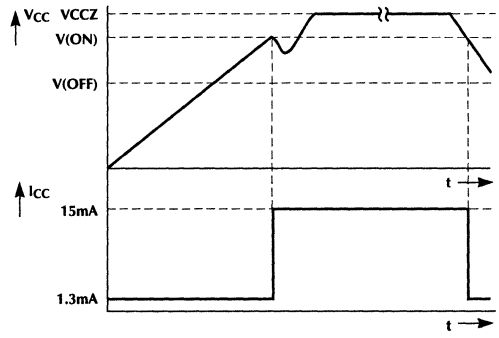


Figure 6. Typical V_{CC} and I_{CC} Waveforms when the ML4831 is Started with a Bleed Resistor from the Rectified AC Line and Bootstrapped from an Auxiliary Winding.

STARTING, RE-START, PREHEAT AND INTERRUPT

The lamp starting scenario implemented in the ML4831 is designed to maximize lamp life and minimize ballast heating during lamp out conditions.

The circuit in Figure 7 controls the lamp starting scenarios: Filament preheat and Lamp Out interrupt. C(X) is charged with a current of $I_{R(SET)}/4$ and discharged through R(X). The voltage at C(X) is initialized to 0.7V (V_{BE}) at power up. The time for C(X) to rise to 3.4V is the filament preheat time. During that time, the oscillator charging current (I_{CHG}) is 2.5/R(SET). This will produce a high frequency for filament preheat, but will not produce sufficient voltage to ignite the lamp.

After cathode heating, the inverter frequency drops to F_{MIN} causing a high voltage to appear to ignite the lamp. If the voltage does not drop when the lamp is supposed to have ignited, the lamp voltage feedback coming into Pin 9 rises to above V_{REF}, the C(X) charging current is shut off and the inverter is inhibited until C(X) is discharged by R(X) to the 1.2V threshold. Shutting off the inverter in this manner prevents the inverter from generating excessive heat when the lamp fails to strike or is out of socket. Typically this time is set to be fairly long by choosing a large value of R(X).

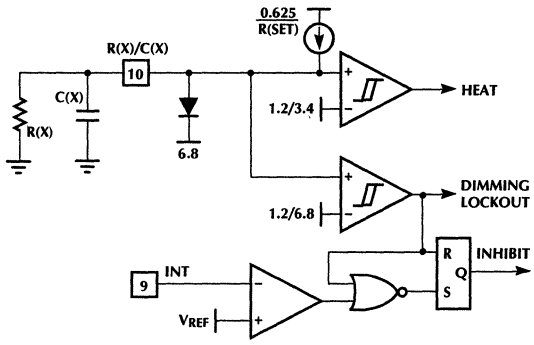


Figure 7. Lamp Preheat and Interrupt Timers

LFB OUT is ignored by the oscillator until C(X) reaches 6.8V threshold. The lamps are therefore driven to full power and then dimmed. The C(X) pin is clamped to about 7.5V.

A summary of the operating frequencies in the various operating modes is shown below.

Operating Mode	Operating Frequency
Preheat	$\frac{[F(MAX) \text{ to } F(MIN)]}{2}$
Dimming Lock-out	F(MIN)
Dimming Control	F(MIN) to F(MAX)

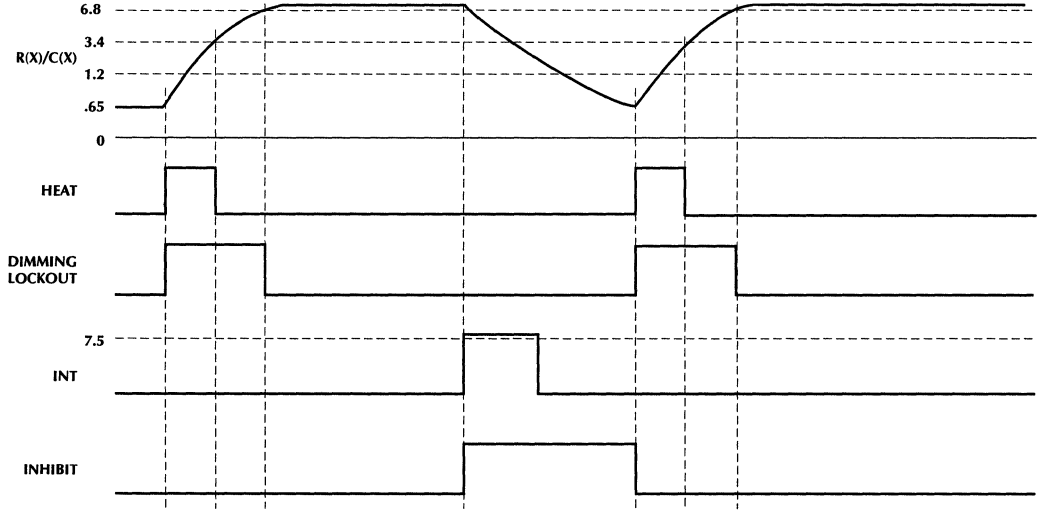


Figure 8. Lamp Starting and Restart Timing

APPLICATIONS POWER FACTOR CORRECTED FLUORESCENT DIMMING LAMP BALLAST

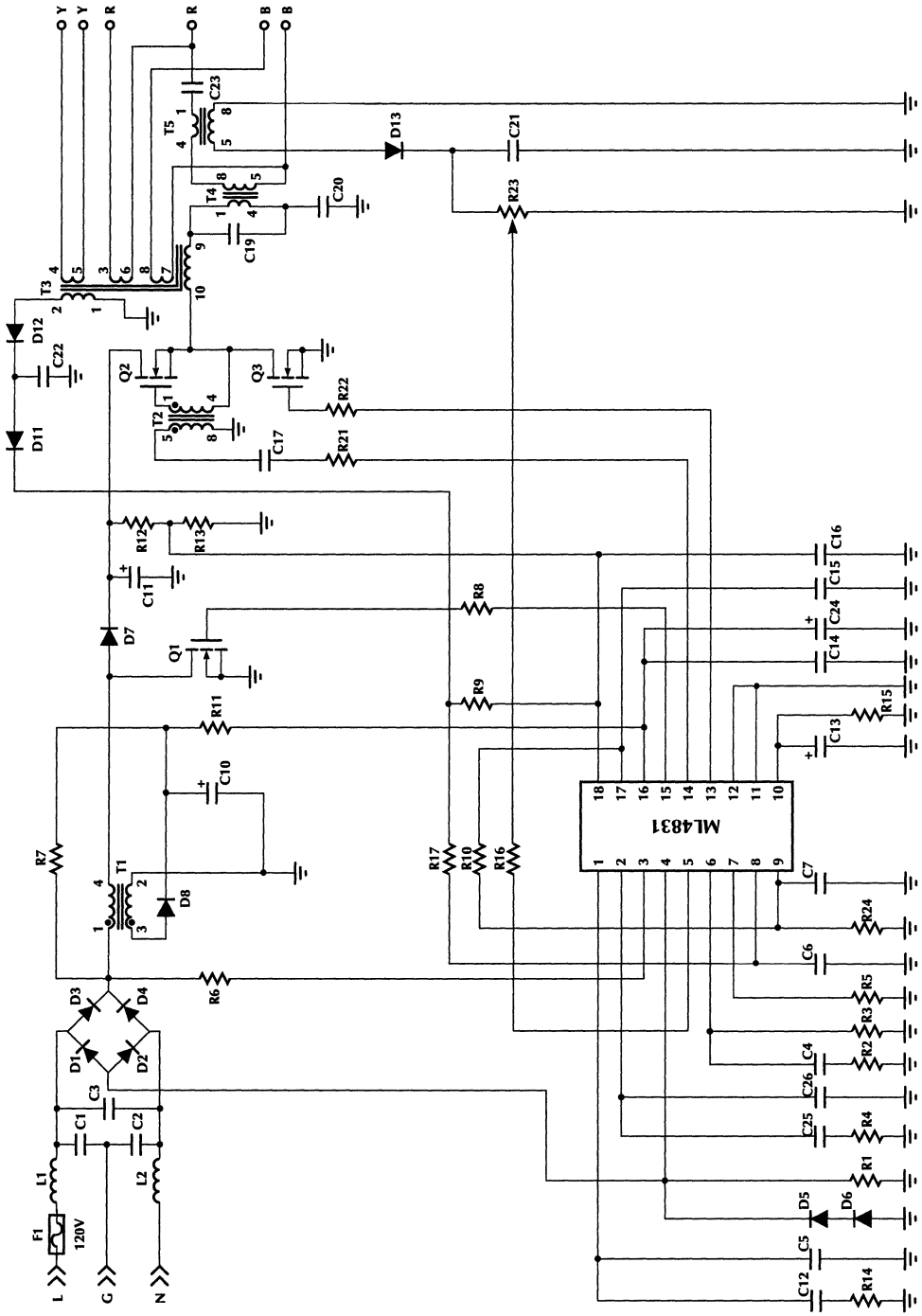


Figure 9. Typical Application: 2-Lamp Isolated Dimming Ballast with Active Power Factor Correction for 120VAC Input

TABLE 1: PARTS LIST FOR THE ML4831EVAL EVALUATION KIT

CAPACITORS

QTY.	REF.	DESCRIPTION	MFR.	PART NUMBER
2	C1, 2	3.3nF, 125VAC, 10%, ceramic, "Y" capacitor	Panasonic	ECK-DNS332ME
1	C3	0.33µF, 250VAC, "X", capacitor	Panasonic	ECQ-U2A334MV
4	C4, 8, 9, 22	0.1µF, 50V, 10%, ceramic capacitor	AVX	SR215C104KAA
2	C5, 21	0.01µF, 50V, 10%, ceramic capacitor	AVX	SR211C103KAA
1	C6	1.5µF, 50V, 2.5%, NPO ceramic capacitor	AVX	RPE121COG152
2	C7, 12	1µF, 50V, 20%, ceramic capacitor	AVX	SR305E105MAA
1	C10	100µF, 25V, 20%, electrolytic capacitor	Panasonic	ECE-A1EFS101
1	C11	100µF, 250V, 20%, electrolytic capacitor	Panasonic	ECE-S2EG101E
1	C13	4.7µF, 50V, 20%, electrolytic capacitor	Panasonic	ECE-A50Z4R7
3	C14, 15, 17	0.22µF, 50V, 10%, ceramic capacitor	AVX	SR305C224KAA
1	C16	1.5µF, 50V, 10%, ceramic capacitor	AVX	SR151V152KAA
1	C19	22nF, 630V, 5%, polypropylene capacitor	WIMA	MKP10, 22nF, 630V, 5%
1	C20	0.1µF, 250V, 5%, polypropylene capacitor	WIMA	MKP10, 0.1µF, 250V, 5%
1	C23	0.068µF, 160V, 5%, polypropylene capacitor	WIMA	MKP4, 68nF, 160V, 5%
1	C24	220µF, 16V, 20%, electrolytic capacitor	Panasonic	ECE-A16Z220
1	C25	47nF, 50V, 10%, ceramic capacitor	AVX	SR211C472KAA
1	C26	330pF, 50V, 10%, ceramic capacitor	AVX	SR151A331JAA
RESISTORS:				
1	R1	0.33Ω, 5%, 1/2W, metal film resistor	NTE	HWD33
1	R2	4.3K, 1/4W, 5%, carbon film resistor	Yageo	4.3K-Q
1	R3	47K, 1/4W, 5%, carbon film resistor	Yageo	47K-Q
1	R4	12K, 1/4W, 5%, carbon film resistor	Yageo	12K-Q
1	R5	20K, 1/4W, 1%, metal film resistor	Dale	SMA4-20K-1
1	R6	360K, 1/4W, 5%, carbon film resistor	Yageo	360K-Q
1	R7	36K, 1W, 5%, carbon film resistor	Yageo	36KW-1-ND
3	R8, 22, 11	22Ω, 1/4W, 5%, carbon film resistor	Yageo	22-Q
1	R9	402K, 1/4W, 1%, metal film resistor	Dale	SMA4-402K-1
1	R10	17.8K, 1/4W, 1%, metal film resistor	Dale	SMA4-17.8K-1
1	R12	475K, 1/4W, 1%, metal film resistor	Dale	SMA4-475K-1
1	R13	5.49K, 1/4W, 1%, metal film resistor	Dale	SMA4-5.49K-1

TABLE 1: PARTS LIST FOR ML4831EVAL EVALUATION KIT (Continued)

QTY.	REF.	DESCRIPTION	MFR.	PART NUMBER
RESISTORS: (Continued)				
4	R14, 17, 24, 25	100K, 1/4W, 5%, carbon film resistor	Yageo	100K-Q
1	R15	681K, 1/4W, 5%, carbon film resistor	Yageo	681K-Q
1	R16	10K, 1/4W, 1%, metal film resistor	Dale	SMA4-10K-1
1	R21	33Ω, 1/4W, 5%, carbon film resistor	Yageo	33-Q
1	R23	25K, pot (for dimming adjustment)	Bourns	3386P-253-ND
DIODES:				
4	D1, 2, 3, 4	1A, 600V, 1N4007 diode (or 1N5061 as a substitute)	Motorola	1N4007TR
2	D5, 6	1A, 50V (or more), 1N4001 diodes	Motorola	1N4001TR
1	D7	3A, 400V, BYV26C or BYT03 400 fast recovery or MUR440 Motorola ultra Fast diode	GI	BYV26C
5	D8, 9, 11, 12, 13	0.1A, 75V, 1N4148 signal diode	Motorola	1N4148TR
IC's:				
1	IC1	ML4831, Electronic Ballast Controller IC	Micro Linear	ML4831CP
TRANSISTORS:				
3	Q1, 2, 3	3.3A, 400V, IRF720 power MOSFET	IR	IR720
MAGNETICS:				
1	T1	T1 Boost Inductor, E24/25, 1mH, Custom Coils P/N 5039 or Coiltronics P/N CTX05-12538-1 E24/25 core set, TDK PC40 material 8-pin vertical bobbin (Cosmo #4564-3-419), Wind as follows: 195 turns 25AWG magnet wire, start pin #1, end pin #4 1 layer mylar tape 14 turns 26AWG magnet wire, start pin #3, end pin #2 NOTE: Gap for 1mH ±5%		
1	T2	T2 Gate Drive Xfmr, L_{PRI} = 3mH, Custom Coils P/N 5037 or Coiltronics P/N CTX05-12539-1 Toroid Magnetics YW-41305-TC Wind as follows: Primary = 25 turns 30AWG magnet wire, start pin #1, end pin #4 Secondary = 50 turns 30AWG magnet wire, start pin #5, end pin #8		

TABLE 1: PARTS LIST FOR ML4831EVAL EVALUATION KIT (Continued)

QTY.	REF.	DESCRIPTION	MFR.	PART NUMBER
MAGNETICS: (Continued)				
1	T3	T3 Inductor, L_{PRI} = 1.66mH, Custom Ciols P/N 5041 or Coiltronics P/N CTX05-12547-1 E24/25 core set, TDK PC40 material 10 pin horizontal bobbin (Plastron #0722B-31-80) Wind as follows: 1st: 170T of 25AWG magnet wire; start pin #10, end pin #9. 1 layer of mylar tape 2nd: 5T of #32 magnet wire; start pin #2, end pin #1 1 layer of mylar tape 3rd: 3T of #30 Kynar coated wire; start pin #4, end pin #5 4th: 3T of #30 Kynar coated wire; start pin #3, end pin #6 5th: 3T of #30 Kynar coated wire; start pin #7, end pin #8 NOTE: Gap for 1.66mH ±5% (pins 9 to 10)		
1	T4	T4 Power Xfmr, L_{PRI} = 3.87mH, Custom Ciols P/N 5038 or Coiltronics P/N CTX05-12545-1 E24/25 core set, TDK PC40 material 8 pin vertical bobbin (Cosmo #4564-3-419) Wind as follows: 1st: 200T of 30AWG magnet wire; start pin #1, end pin #4. 1 layer of mylar tape 2nd: 300T of 32AWG magnet wire; start pin #5, end pin #8 NOTE: Gap for inductance primary: (pins 1 to 4) @ 3.87mH ±5%		
1	T5	T5 Current Sense Inductor, Custom Coils P/N 5040 or Coiltronics P/N CTX05-12546-1 Toroid Magnetics YW-41305-TC Wind as follows: Primary = 3T 30AWG magnet coated wire, start pin #1, end pin #4 Secondary = 400T 35AWG magnet wire, start pin #5, end pin #8		
INDUCTORS:				
2	L1, 2	EMI/RFI Inductor, 600µH, DC resistance = 0.45Ω	Prem. Magnetics	SPE116A
FUSES:				
1	F1	2A fuse, 5 x 20mm miniature	Littlefuse	F948-ND
2		Fuse Clips, 5 x 20mm, PC Mount		F058-ND
HARDWARE:				
1		Single TO-220 Heatsink	Aavid Eng.	PB1ST-69
2		Double TO-220 Heatsink	IERC	PSE1-2TC
3		MICA Insulators	Keystone	4673K-ND

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4831CP	0°C to + 85°C	Molded DIP (P18)

ML4831EVAL

120VAC Dimmable Electronic Ballast Evaluation Kit

GENERAL DESCRIPTION

The ML4831 evaluation board is a low cost, improved version of Micro Linear's ML4830 dimmable ballast EVAL board. Careful attention was given to reducing the magnetics cost of the eval board as well as other costly components. In addition, the design was improved to both increase and linearize the dimming range, eliminate lamp shut-off at low intensities, reduce visible standing waves and simplify the lamp-out protection circuitry. All components used are inexpensive and easy to obtain.

Operating from 85 to 135VAC line, the ML4831 evaluation board is a power factor corrected 60W electronic ballast with a dimming range capable of a 20:1 intensity change. Optimized to power two series connected T8 fluorescent bulbs, the ML4831 EVAL board displays all the features of Micro Linear's latest ballast controller IC. The mode of operation used for pre-heat, striking and dimming of the bulbs is the widely accepted variable frequency, non-overlapping inverter topology. This eval board may be used with various bulbs other than T8's (such as T12's).

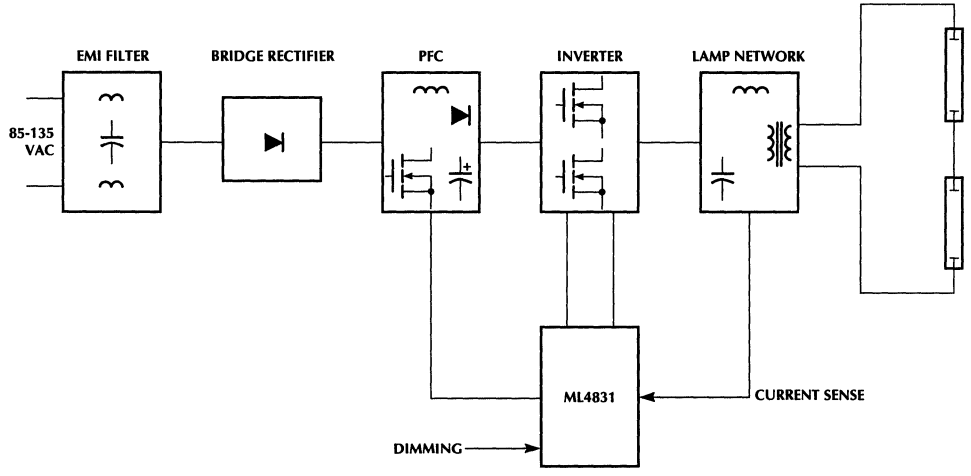
FEATURES

- Drives 2 Series Connected T8 or T12 Lamps (60W) (Will Drive a Single Lamp)
- Power Factor Corrected Front-End
- 85 to 135VAC Operation
- 20 to 1 Dimming Range Capability
- Uses Low Cost External Components

KIT COMPONENTS

- ML4831EVAL User's Guide
- ML4831 Data Sheet
- Fully Functional ML4831 Evaluation Board
- PCB Layout Gerber File

BLOCK DIAGRAM



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FEATURING
Extended Commercial Temperature Range
-20°C to 70°C
for Portable Handheld Equipment

December 1994
ADVANCED INFORMATION

ML4851

Low Voltage Boost Regulator

GENERAL DESCRIPTION

The ML4851 is a low power boost regulator designed for DC to DC conversion in 1 to 3 cell battery powered systems. The maximum switching frequency can exceed 100kHz, allowing the use of small, low cost inductors.

The combination of BiCMOS process technology, internal synchronous rectification, variable frequency operation, and low supply current make the ML4851 ideal for 1 cell applications. The ML4851 is capable of start-up with input voltages as low as 1V and is available in 5V and 3.3V output versions with output voltage accuracy of ±3%.

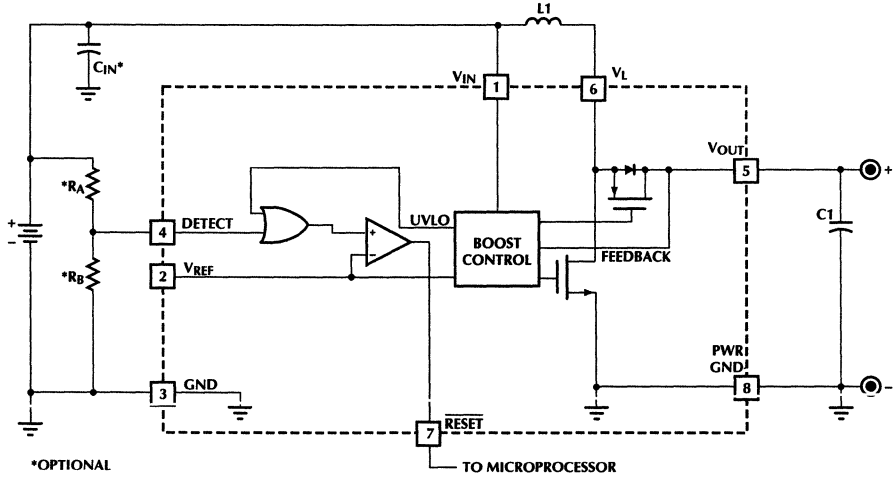
An integrated synchronous rectifier eliminates the need for an external Schottky diode and provides a lower forward voltage drop, resulting in higher conversion efficiency. In addition, low quiescent battery current and variable frequency operation result in high efficiency even at light loads. The ML4851 requires only one inductor and two capacitors to build a very small regulator circuit capable of achieving conversion efficiencies in excess of 90%.

The circuit also contains a $\overline{\text{RESET}}$ output which goes low when the IC can no longer function due to low input voltage, or when the DETECT input drops below 200mV.

FEATURES

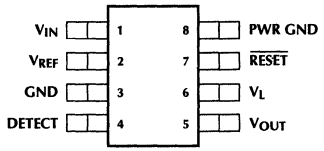
- Guaranteed full load start-up and operation at 1V input
- Maximum switching frequency > 100kHz
- Pulse Frequency Modulation and Internal Synchronous Rectification for high efficiency
- Minimum external components
- Low ON resistance internal switching FETs
- Micropower operation
- 5V and 3.3V output versions

BLOCK DIAGRAM



PIN CONNECTION

ML4851-5/-3
8-Pin SOIC (S08)



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	V_{IN}	Battery input voltage
2	V_{REF}	200mV reference output
3	GND	Analog signal ground
4	DETECT	Pulling this pin below V_{REF}, causes the $\overline{RESET}$ pin to go low
5	V_{OUT}	Boost regulator output
6	V_L	Boost inductor connection
7	$\overline{RESET}$	Output goes low when regulation cannot be achieved or when DETECT goes below 200mV
8	PWR GND	Return for the NMOS output transistor

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ORDERING INFORMATION

PART NUMBER	OUTPUT VOLTAGE	TEMPERATURE RANGE	PACKAGE
ML4851ES-3	3.3V	–20°C to +70°C	8-Pin SOIC (S08)
ML4851ES-5	5.0V	–20°C to +70°C	8-Pin SOIC (S08)
ML4851IS-3	3.3V	–40°C to +85°C	8-Pin SOIC (S08)
ML4851IS-5	5.0V	–40°C to +85°C	8-Pin SOIC (S08)

FEATURING
Extended Commercial Temperature Range
-20°C to 70°C
for Portable Handheld Equipment

December 1994

ML4861

Low Voltage Boost Regulator

GENERAL DESCRIPTION

The ML4861 is a boost regulator designed for DC to DC conversion in 1 to 3 cell battery powered systems. The combination of BiCMOS process technology, internal synchronous rectification, variable frequency operation, and low supply current make the ML4861 ideal for 1 cell applications. The ML4861 is capable of start-up with input voltages as low as 1V and is available in 6V, 5V, and 3.3V output versions with output voltage accuracy of ±3%.

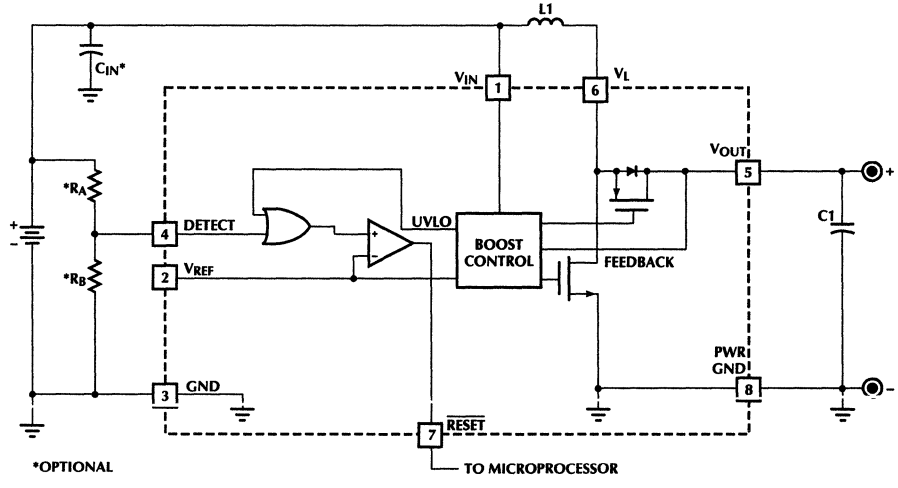
An integrated synchronous rectifier eliminates the need for an external Schottky diode and provides a lower forward voltage drop, resulting in higher conversion efficiency. In addition, low quiescent battery current and variable frequency operation result in high efficiency even at light loads. The ML4861 requires only one inductor and two capacitors to build a very small regulator circuit capable of achieving conversion efficiencies in excess of 90%.

The circuit also contains a $\overline{\text{RESET}}$ output which goes low when the IC can no longer function due to low input voltage, or when the DETECT input drops below 200mV.

FEATURES

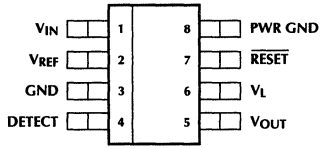
- Guaranteed full load start-up and operation at 1V input
- Pulse Frequency Modulation and Internal Synchronous Rectification for high efficiency
- Minimum external components
- Low ON resistance internal switching FETs
- Micropower operation
- 6V, 5V, and 3.3V output versions

BLOCK DIAGRAM



PIN CONNECTION

ML4861-6/-5/-3
8-Pin SOIC (S08)



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	V_{IN}	Battery input voltage
2	V_{REF}	200mV reference output
3	GND	Analog signal ground
4	DETECT	When this pin below V_{REF}, causes the $\overline{RESET}$ pin to go low
5	V_{OUT}	Boost regulator output
6	V_L	Boost inductor connection
7	$\overline{RESET}$	Output goes low when regulation cannot be achieved or when DETECT goes below 200mV
8	PWR GND	Return for the NMOS output transistor

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ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Voltage on any pin 7V
Peak Switch Current, $I_{(PEAK)}$ 2A
Average Switch Current, $I_{(AVG)}$ 500mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA}) ..... 110°C/W

OPERATING CONDITIONS

Temperature Range
ML4861CS-X ..... 0°C to +70°C
ML4861ES-X ..... –20°C to +70°C
ML4861IS-X ..... –40°C to +85°C
V_{IN} Operating Range
ML4861CS-X ..... 1.0V to V_{OUT} – 0.2V
ML4861ES-X, ML4861IS-X ..... 1.1V to V_{OUT} – 0.2V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = Operating Voltage Range, T_A = Operating Temperature Range.

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Supply					
V_{IN} Current	$V_{IN} = V_{OUT} - 0.2V$		45	55	µA
V_{OUT} Quiescent Current			8	10	µA
V_L Quiescent Current				1	µA
Reference					
Output Voltage (V_{REF})	$0 < I_{PIN2} < -5\mu A$,	190	200	210	mV
PFM Regulator					
Pulse Width (T_{ON})		9	10	11	µs
Output Voltage (V_{OUT})					
ML4861-6	T_{ON} = 0 at V_{OUT}(MAX),	5.82	6.0	6.18	V
ML4861-5	9µs ≤ T_{ON} ≤ 11µs V_{OUT}(MIN)	4.85	5.0	5.15	V
ML4861-3		3.2	3.3	3.4	V
Load Regulation	See Figure 1				
ML4861-6	V_{IN} = 1.2V, I_{OUT} ≤ 20mA	5.82	6.0	6.18	V
	V_{IN} = 2.4V, I_{OUT} ≤ 95mA	5.82	6.0	6.18	V
ML4861-5	V_{IN} = 1.2V, I_{OUT} ≤ 25mA	4.85	5.0	5.15	V
	V_{IN} = 2.4V, I_{OUT} ≤ 135mA	4.85	5.0	5.15	V
ML4861-3	V_{IN} = 1.2V, I_{OUT} ≤ 40mA	3.2	3.3	3.4	V
	V_{IN} = 2.4V, I_{OUT} ≤ 180mA	3.2	3.3	3.4	V
Under-Voltage Lockout Threshold			0.85	0.95	V
$\overline{\text{RESET}}$ Comparator					
DETECT Threshold		190	200	210	mV
DETECT Bias Current		–100		100	nA
$\overline{\text{RESET}}$ Output High Voltage (V_{OH})	I_{OH} = –100µA	V_{OUT} – 0.2			V
$\overline{\text{RESET}}$ Output Low Voltage (V_{OL})	I_{OL} = 100µA			0.2	V

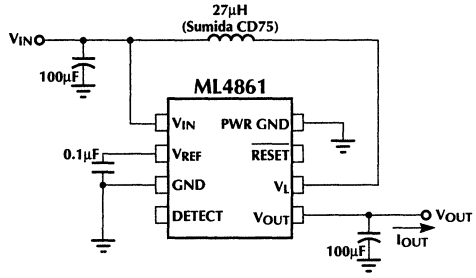


Figure 1. Application Test Circuit

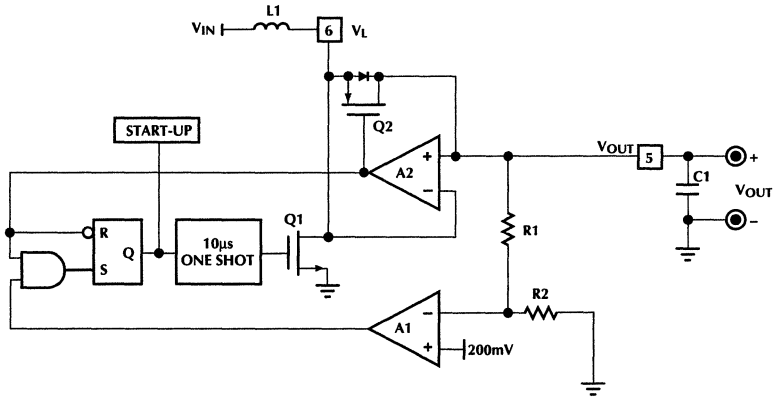


Figure 2. PFM Regulator Block Diagram

FUNCTIONAL DESCRIPTION

The ML4861 combines Pulse Frequency Modulation (PFM) and synchronous rectification to create a boost converter that is both highly efficient and simple to use. A PFM regulator charges a single inductor for a fixed period of time and then completely discharges before another cycle begins, simplifying the design by eliminating the need for conventional current limiting circuitry. Synchronous rectification is accomplished by replacing an external Schottky diode with an on-chip PMOS device, reducing switching losses and external component count.

REGULATOR OPERATION

A block diagram of the boost converter is shown in Figure 2. The circuit remains idle when V_{OUT} is at or above the desired output voltage, drawing 45µA from V_{IN}, and 8µA from V_{OUT} through the feedback resistors R1 and R2. When V_{OUT} drops below the desired output level, the output of amplifier A1 goes high, signaling the regulator to deliver charge to the output. Since the output of amplifier A2 is normally high, the flip-flop captures the A1 set signal and creates a pulse at the gate of the NMOS transistor Q1. The NMOS transistor will charge the inductor L1 for 10µs, resulting in a peak current given by:

$$I_{L(PEAK)} = \frac{T_{ON} \times V_{IN}}{L_1} \approx \frac{10\mu s \times V_{IN}}{L_1} \qquad (1)$$

For reliable operation, L1 should be chosen so that $I_{L(PEAK)}$ does not exceed 2A.

When the one-shot times out, the NMOS transistor releases the V_L pin, allowing the inductor to fly-back and momentarily charge the output through the body diode of PMOS transistor Q2. But, as the voltage across the PMOS transistor changes polarity, its gate will be driven low by the current sense amplifier A2, causing Q2 to short out its body diode. The inductor then discharges into the load through Q2. The output of A2 also serves to reset the flip-flop and one-shot in preparation for the next charging cycle. A2 releases the gate of Q2 when its current falls to zero. If V_{OUT} is still low, the flip-flop will immediately initiate another pulse. The output capacitor (C1) filters the inductor current, limiting output voltage ripple. Inductor current and one-shot waveforms are shown in Figure 3.

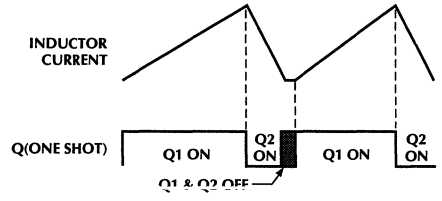


Figure 3. PFM Inductor Current Waveforms and Timing.

$\overline{\text{RESET}}$ COMPARATOR

An additional comparator is provided to detect low V_{IN}, or any other error condition that is important to the user. The inverting input of the comparator is internally connected to V_{REF}, while the non-inverting input is provided externally at the DETECT pin. The output of the comparator is the $\overline{\text{RESET}}$ pin, which swings from V_{OUT} to GND when an error is detected.

DESIGN CONSIDERATIONS

INDUCTOR

Selecting the proper inductor for a specific application usually involves a trade-off between efficiency and maximum output current. Choosing too high a value will keep the regulator from delivering the required output current under worst case conditions. Choosing too low a value causes efficiency to suffer. It is necessary to know the maximum required output current and the input voltage range to select the proper inductor value. The maximum inductor value can be estimated using the following formula:

$$L_{MAX} = \frac{V_{IN(MIN)}^{2} \times T_{ON(MIN)} \times \eta}{2 \times V_{OUT} \times I_{OUT(MAX)}} \qquad (2)$$

where η is the efficiency, typically between 0.8 and 0.9. Note that this is the value of inductance that just barely delivers the required output current under worst case conditions. A lower value may be required to cover inductor tolerance, the effect of lower peak inductor currents caused by resistive losses, and minimum dead time between pulses.

Another method of determining the appropriate inductor value is to make an estimate based on the typical performance curves given in Figures 4 and 5. Figure 4 shows maximum output current as a function of input voltage for several inductor values. These are typical performance curves and leave no margin for inductance and ON-time variations. To accommodate worst case conditions, it is necessary to derate these curves by at least 10% in addition to inductor tolerance.

For example, a two cell to 5V application requires 80mA of output current while using an inductor with 15% tolerance. The output current should be derated by 25% to 100mA to cover the combined inductor and ON-time tolerances. Assuming that 2V is the end of life voltage of a two cell input, Figure 4 shows that with a 2V input, the ML4861-5 delivers 108mA with a 27µH inductor.

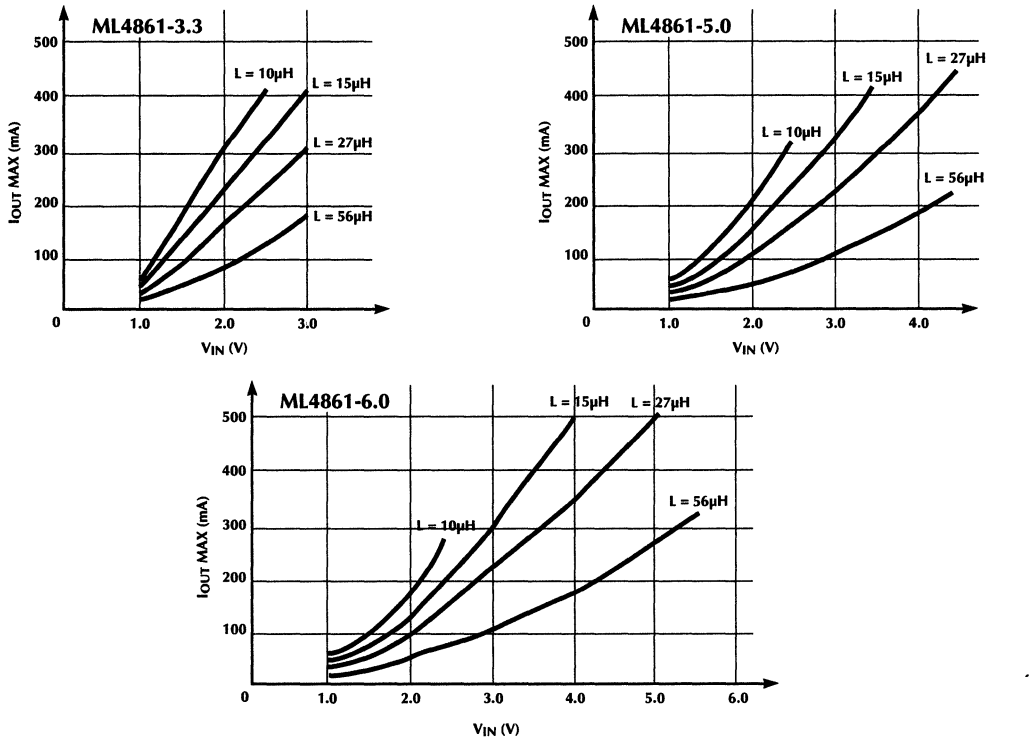


Figure 4. Output Current vs Input Voltage.

Figure 5 shows efficiency under the conditions used to create Figure 4. It can be seen that efficiency is mostly independent of input voltage and is closely related to inductor value. This illustrates the need to keep the inductor value as high as possible to attain peak system efficiency. As the inductor value goes down to 10µH, the efficiency drops to between 70% and 75%. With 56µH, the efficiency exceeds 90% and there is little room for improvement. At values greater than 100µH, the operation of the synchronous rectifier becomes unreliable because the inductor current is so small that it is difficult for the control circuitry to detect. The data used to generate Figures 4 and 5 is provided in Table 1.

After the appropriate inductor value is chosen, it is necessary to find the minimum inductor current rating required. Peak inductor current is determined from the following formula:

$$I_{L(PEAK)} = \frac{T_{ON(MAX)} \times V_{IN(MAX)}}{L_{MIN}} \qquad (3)$$

In the two cell application previously described, a maximum input voltage of 3V would give a peak current of 1.2A. When comparing various inductors, it is important to keep in mind that suppliers use different criteria to determine their ratings. Many use a conservative current level, where inductance has dropped to 90% of its normal level. In any case, it is a good idea to try inductors of various current ratings with the ML4861 to determine which inductor is the best choice. Check efficiency and maximum output current, and if a current probe is available, look at the inductor current to see if it looks like the waveform shown in Figure 3. For additional information, see Applications Note 29, "Choosing an Inductor for Your ML4861 Application."

Suitable inductors can be purchased from the following suppliers:

Coilcraft	(708) 639-6400
Coiltronics	(407) 241-7876
Dale	(605) 665-9301
Sumida	(708) 956-0666

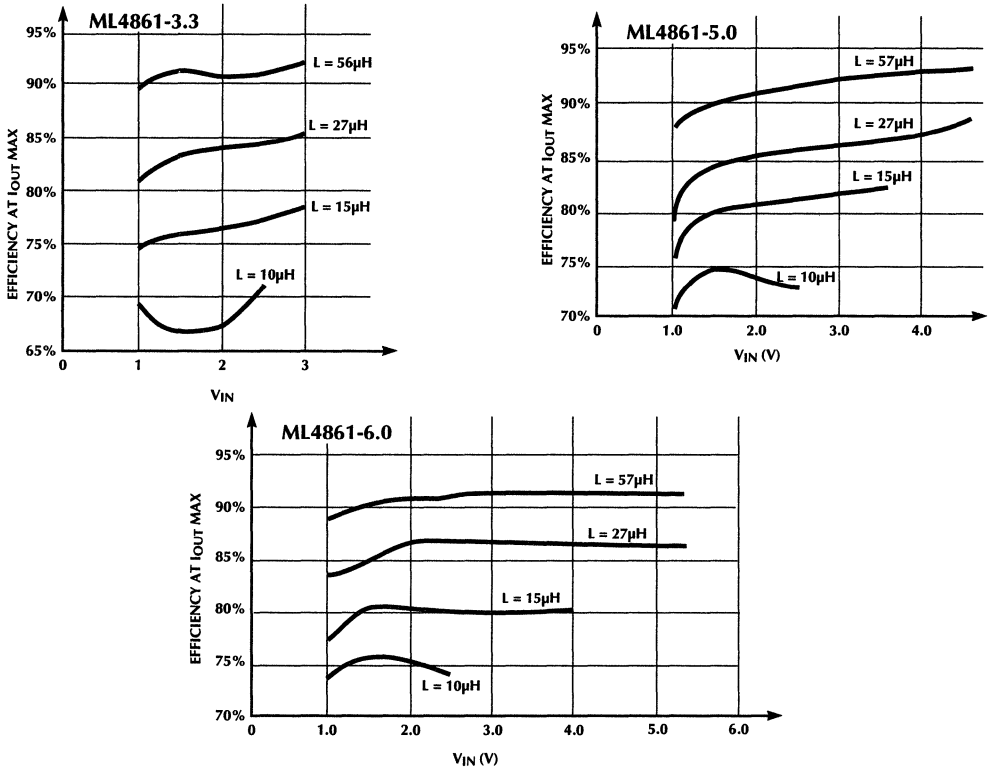


Figure 5. Typical Efficiency as a Function of V_{IN}.

OUTPUT CAPACITOR

The choice of output capacitor is also important, as it controls the output ripple and optimizes the efficiency of the circuit. Output ripple is influenced by three capacitor parameters: capacitance, ESR, and ESL. The contribution due to capacitance can be determined by looking at the change in capacitor voltage required to store the energy delivered by the inductor in a single charge-discharge cycle, as determined by the following formula:

$$\Delta V_{OUT} = \frac{T_{ON}^2 \times V_{IN}^2}{2 \times L \times C \times (V_{OUT} - V_{IN})} \qquad (4)$$

For a 2.4V input, and 5V output, a 27µH inductor, and a 47µF capacitor, the expected output ripple due to capacitor value is 87mV.

Capacitor Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL), also contribute to the output ripple due to the inductor discharge current waveform. Just after the NMOS transistor turns off, the output current ramps quickly to match the peak inductor current. This fast change in current through the output capacitor's ESL causes a high frequency (5ns) spike that can be over 1V in magnitude. After the ESL spike settles, the output voltage still has a ripple component equal to the inductor discharge current times the ESR. This component will have a sawtooth shape and a peak value equal to the peak inductor current times the ESR. ESR also has a negative effect on efficiency by contributing I-squared R losses during the discharge cycle.

An output capacitor with a capacitance of 100µF, an ESR of less than 0.1Ω, and an ESL of less than 5nH is a good general purpose choice. Tantalum capacitors which meet these requirements can be obtained from the following suppliers:

Matsuo	(714) 969-2491
Sprague	(603) 224-1961

If ESL spikes are causing output noise problems, an EMI filter can be added in series with the output.

INPUT CAPACITOR

Unless the input source is a very low impedance battery, it will be necessary to decouple the input with a capacitor with a value of between 47µF and 100µF. This provides the benefits of preventing input ripple from affecting the ML4861 control circuitry, and it also improves efficiency by reducing I-squared R losses during the charge and discharge cycles of the inductor. Again, a low ESR capacitor (such as tantalum) is recommended.

REFERENCE CAPACITOR

Under some circumstances input ripple cannot be reduced effectively. This occurs primarily in applications where inductor currents are high, causing excess output ripple due to "pulse grouping", where the charge-discharge pulses are not evenly spaced in time. In such cases it may be necessary to decouple the reference pin (V_{REF}) with a small 10nF to 100nF ceramic capacitor. This is particularly true if the ripple voltage at V_{IN} is greater than 100mV.

SETTING THE $\overline{\text{RESET}}$ THRESHOLD

To use the $\overline{\text{RESET}}$ comparator as an input voltage monitor, it is necessary to use an external resistor divider tied to the DETECT pin as shown in the block diagram. The resistor values R_A and R_B can be calculated using the following equation:

$$V_{IN(MIN)} = 0.2 \times \frac{(R_A + R_B)}{R_B} \qquad (5)$$

The value of R_B should be 100kΩ or less to minimize bias current errors. R_A is then found by rearranging the equation:

$$R_A = R_B \times \left(\frac{V_{IN(MIN)}}{0.2} - 1 \right) \qquad (6)$$

LAYOUT

Good PC board layout practices will ensure the proper operation of the ML4861. Important layout considerations include:

- Use adequate ground and power traces or planes
- Keep components as close as possible to the ML4861
- Use short trace lengths from the inductor to the V_L pin and from the output capacitor to the V_{OUT} pin
- Use a single point ground for the ML4861 ground pins, and the input and output capacitors

A sample PC board layout is shown in Figure 6.

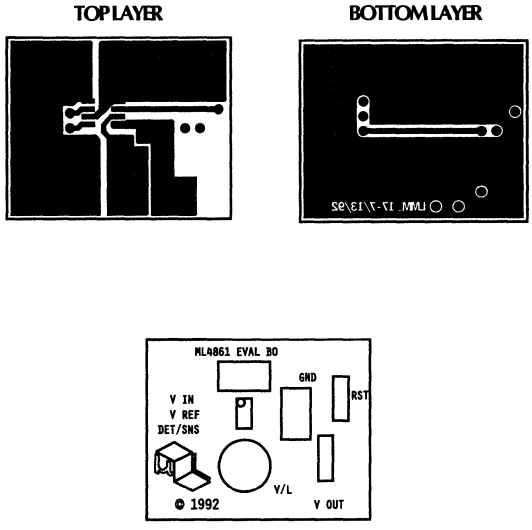


Figure 6. Sample PC Board Layout.

TABLE 1. MAXIMUM OUTPUT CURRENT AND EFFICIENCY.

ML4861-3.3

V_{IN}	I_{OUT} (mA)	EFFICIENCY PERCENTAGE
L = 10µH		
1.0	77.5	69.7
1.5	191.7	67.2
2.0	310.2	67.8
2.5	409.7	71.1
L = 15µH		
1.0	58.5	74.5
1.5	137.1	75.7
2.0	232.1	76.4
2.5	335.3	76.9
3.0	405.0	78.2
L = 27µH		
1.0	40.0	81.1
1.5	95.4	82.9
2.0	163.8	83.6
2.5	242.5	84.2
3.0	306.0	85.2
L = 56µH		
1.0	19.5	89.4
1.5	45.5	90.9
2.0	79.3	90.6
2.5	122.6	91.1
3.0	168.3	91.7

ML4861-5.0

V_{IN}	I_{OUT} (mA)	EFFICIENCY PERCENTAGE
L = 10µH		
1.0	45.8	70.6
1.5	112.6	74.2
2.0	210.7	74.0
2.5	331.6	73.0
L = 15µH		
1.0	32.4	75.7
1.5	85.6	79.5
2.0	156.3	80.6
2.5	240.2	80.9
3.0	332.5	81.2
3.5	432.3	81.6
L = 27µH		
1.0	20.8	78.7
1.5	59.3	83.6
2.0	108.6	84.9
2.5	167.6	85.6
3.0	236.6	86.2
3.5	311.2	86.6
4.0	385.4	87.2
4.5	442.3	88.0
L = 56µH		
1.0	11.3	87.3
1.5	27.4	89.4
2.0	49.8	90.5
2.5	78.1	91.2
3.0	112.0	91.7
3.5	151.2	92.2
4.0	194.2	92.6
4.5	237.0	93.1

TABLE 1. MAXIMUM OUTPUT CURRENT AND EFFICIENCY (Continued)

ML4861-6.0

V_{IN} (V)	I_{IN} (mA)	V_{OUT} (V)	I_{OUT} (mA)	EFFICIENCY %
L = 10µH				
1.0	325.8	5.975	40.1	73.5
1.5	524.6	5.990	100.0	76.1
2.0	730.0	5.995	184.5	75.7
2.5	910.8	5.992	284.0	74.7
L = 15µH				
1.0	220.5	5.993	28.5	77.5
1.5	365.7	5.981	73.8	80.5
2.0	516.7	5.998	139.9	81.2
2.5	639.3	5.995	216.3	81.1
3.0	755.1	5.999	305.1	80.8
3.5	855.1	5.996	402.0	80.5
4.0	916.1	5.992	493.0	80.6
L = 27µH				
1.0	154.1	5.992	21.6	84.0
1.5	235.7	5.982	50.7	85.8
2.0	329.5	5.990	95.9	87.2
2.5	404.6	6.000	147.5	87.5
3.0	478.2	5.995	209.6	87.6
3.5	551.0	5.999	281.6	87.6
4.0	610.5	5.997	356.7	87.6
4.5	659.9	5.993	434.0	87.6
5.0	689.1	5.991	504.3	87.7
5.5	665.0	5.999	534.7	87.7
L = 60µH				
1.0	67.6	5.977	10.0	88.4
1.5	108.8	5.961	24.7	90.2
2.0	148.0	5.976	45.1	91.1
2.5	186.0	5.978	71.2	91.5
3.0	222.4	5.973	102.6	91.9
3.5	257.2	5.975	138.6	92.0
4.0	290.2	5.989	178.7	92.2
4.5	321.2	5.995	222.7	92.4
5.0	346.4	5.997	267.1	92.5
5.5	356.1	6.000	302.4	92.6

ORDERING INFORMATION

PART NUMBER	OUTPUT VOLTAGE	TEMPERATURE RANGE	PACKAGE
ML4861CS-3	3.3V	0°C to +70°C	8-Pin SOIC (S08)
ML4861CS-5	5.0V	0°C to +70°C	8-Pin SOIC (S08)
ML4861CS-6	6.0V	0°C to +70°C	8-Pin SOIC (S08)
ML4861ES-3	3.3V	–20°C to +70°C	8-Pin SOIC (S08)
ML4861ES-5	5.0V	–20°C to +70°C	8-Pin SOIC (S08)
ML4861ES-6	6.0V	–20°C to +70°C	8-Pin SOIC (S08)
ML4861IS-3	3.3V	–40°C to +85°C	8-Pin SOIC (S08)
ML4861IS-5	5.0V	–40°C to +85°C	8-Pin SOIC (S08)
ML4861IS-6	6.0V	–40°C to +85°C	8-Pin SOIC (S08)

ML4861EVAL

Low Voltage Boost Regulator Evaluation Kit

GENERAL DESCRIPTION

The ML4861EVAL kit provides a convenient vehicle to evaluate the ML4861 low voltage boost regulator IC. The kit contains a fully assembled circuit board and all of the necessary documentation to quickly evaluate a typical application circuit. The board was designed to demonstrate performance and to illustrate critical layout practices necessary for reliable operation of the circuit.

The ML4861 is complete solution for DC to DC conversion in 1 to 3 cell battery powered systems. The circuit is ideal in applications requiring high efficiency, and a minimum number of external components.

The boost IC is capable of running with input voltages as low as 1.0V and is available in four different output versions: a 3.3V output (ML4861-3.3), a 5.0V output (ML4861-5), a 6.0V output (ML4861-6), or adjustable output versions (ML4761 and ML4961).

FEATURES

- Synchronous Rectification for High Efficiency
- Wide Input Voltage Range
- Minimal External Components
- Micro Power Operation
- Low Battery/Output Voltage Regulation Flag
- 3.3V, 5.0V, 6.0V, and Adjustable Output Versions
- Auto-Suspend Mode for Low Power Standby System Operation

KIT COMPONENTS

The evaluation package contains the following items:

- ML4861EVAL User's guide
- ML4861 Data Sheet
- Application Note 29
- ML4861 Evaluation Board

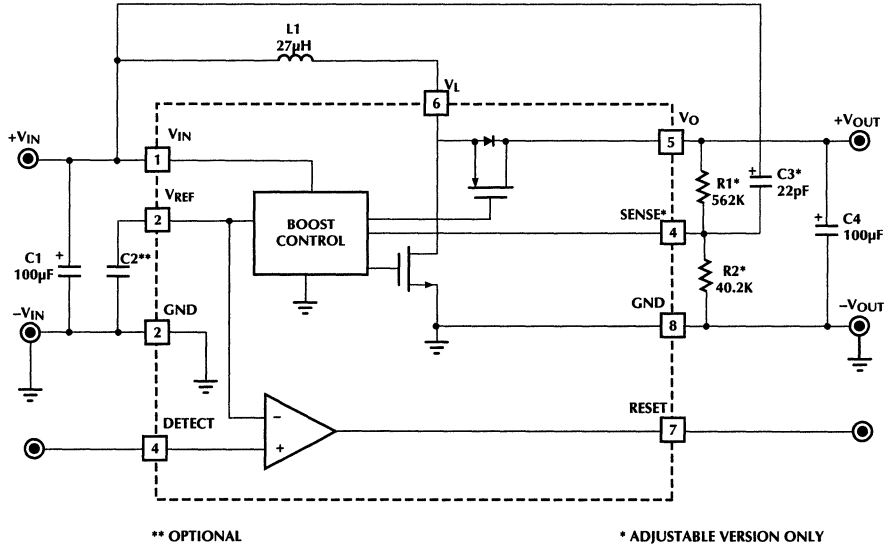


FIGURE 1: ML4861 Evaluation Board Schematic

ML4862

Battery Power Control IC

GENERAL DESCRIPTION

The ML4862 is a complete solution for DC to DC conversion and power management in multi-cell battery powered portable computers and instruments. Several advanced techniques are incorporated in the IC for the highest possible systems efficiency and lowest possible battery drain.

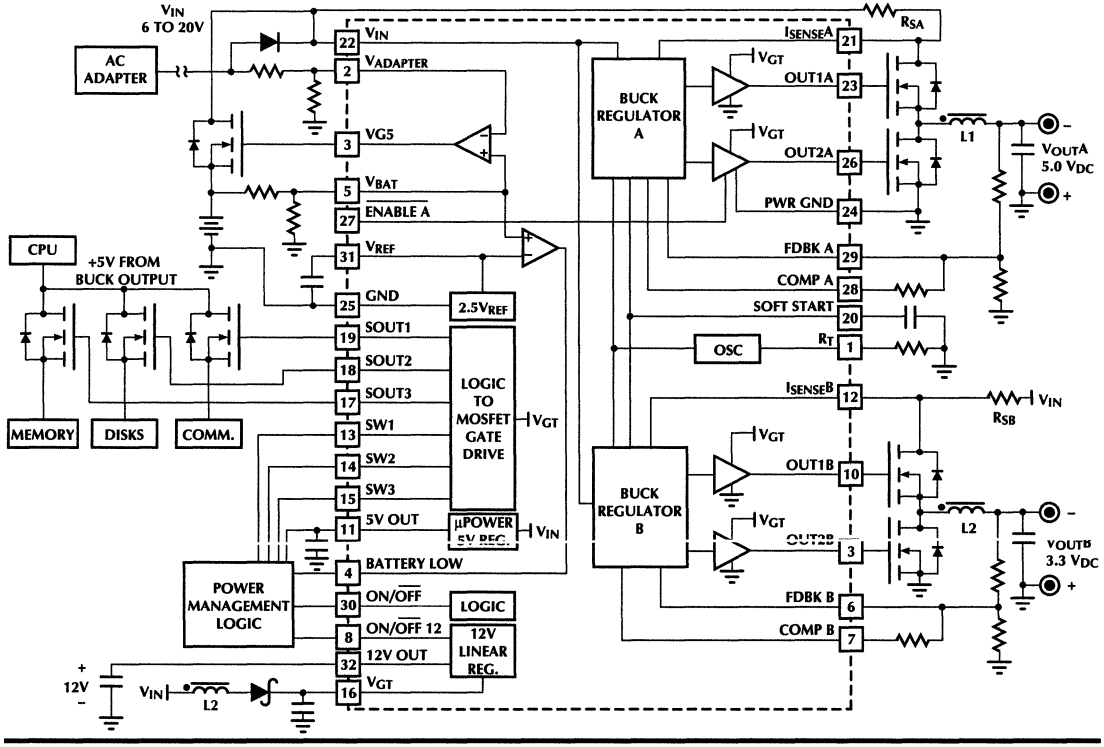
The 5.0V and 3.3V main regulators in the ML4862 each controls a Synchronous Rectified buck regulator and each drives two N-Channel MOSFETs. This allows high conversion efficiencies (90% or greater). Bias for all N-Channel MOSFETs in the system as well as the input for the 12V regulator for programming EEPROMs comes from an auxiliary winding on the buck regulator choke.

The ML4862 also contains 3 outputs to drive external N-Channel MOSFETs to power down disk drives and memory under control of external logic. Automatic switch-over to battery operation is also provided when the charger is removed. A µPower 5V linear regulator and low battery indicator are provided for the power monitoring logic.

FEATURES

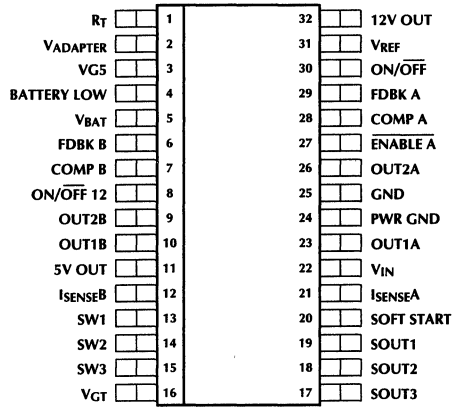
- Two Synchronously Rectified, 100KHz Buck Regulators: for 5V and 3.3V outputs
- Regulation to ±3% maximum; provides 2% PCMCIA switch matrix margin
- Low Cost All N-Channel MOSFET Switching
- Three Logic to N-Channel Gate Drive translators for power management
- µPower 5V standby linear regulator to run power management logic
- Output and logic for N-Channel MOSFET to disconnect battery when charger is connected
- 12V Auxiliary output available with On/Off Control for E^2 memory programming
- Low battery detect comparator
- Wide Input Voltage Range (5V to 20V)
- Customizable Tile Array Technology - Consult factory for additional options

BLOCK DIAGRAM



PIN CONFIGURATION

ML4862
32-Pin SOIC (S32W)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	R_T	Timing Resistor which sets oscillator frequency
2	$V_{ADAPTER}$	Input to sense whether adapter is active. When this pin is above V_{BAT}, VG5 goes low.
3	VG5	Output to drive N-Channel MOSFET gate to switch battery out when adapter is present
4	BATTERY LOW	A logic low level indicates the voltage on V_{BAT} is below 2.5V. This is an open-collector output.
5	V_{BAT}	Battery Comparator input
6	FDBK B	Voltage Feedback for buck regulator B
7	COMP B	Buck Regulator B frequency compensation terminal
8	ON/$\overline{OFF}$ 12	A logic high turns on the 12V linear regulator
9	OUT2B	5V Buck Regulator Synchronous Rectifier Output
10	OUT1B	5V Buck Regulator Switch Output
11	5V OUT	Output of the µPower 5V regulator. Normally used to power external management circuits and logic
12	$I_{SENSE}B$	Current Sensing for buck regulator B current limit
13-15	SW1-3	Inputs for power management MOSFET gate drivers
16	V_{GT}	Boosted voltage to drive N-Channel gates and input to 12V linear regulator
17-19	SOUT3-1	MOSFET gate drive outputs for power management
20	SOFT START	Connected to a soft start capacitor
21	$I_{SENSE}A$	Current Sensing for buck regulator A current limit
22	V_{IN}	Input from Battery or AC Adapter
23	OUT1A	3.3V Buck Regulator Switch Output
24	PWR GND	Power Ground
25	GND	Logic and signal Ground
26	OUT2A	3.3V Buck Regulator Synchronous Rectifier Output
27	$\overline{ENABLE A}$	A logic low disables Buck Regulator A's Synchronous Rectifier output
28	COMP A	Buck Regulator A frequency compensation terminal
29	FDBK A	Voltage Feedback for buck regulator A
30	ON/$\overline{OFF}$	A low on this pin disables all IC functions except the low battery detection comparator, the linear 5V regulator and the 2.5V reference, and puts the IC into a low current consumption mode
31	V_{REF}	Buffered 2.5V reference output
32	12V OUT	Output of the 12V linear regulator

7

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Voltage on any pin 36V
Output Current, Source or Sink (Pins 9,10, 23, 26)
Pulsed 300mA
VG5 Source Current 20mA
VG5 Sink Current 200mA
12V Linear Regulator Output Current 200mA
5V Linear Regulator Output Current 50mA
Logic Inputs (pins 8,13,14,15,27,30) ..... –0.3V to 5.5V
I_{SENSE} Inputs (pins 12 ,21) ..... V_{IN}
Comparator Inputs (pins 2, 5) ..... –0.3V to 5.5V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 Sec.) ..... +260°C
Thermal Resistance (θ_{JA}) Plastic SOIC ..... 60°C/W

OPERATING CONDITIONS

Temperature Range
Commercial ..... 0°C to +70°C
V_{IN} Voltage Range ..... 5.4V to 24V
V_{GT} Voltage Range ..... V_{IN} –0.5 to 35V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, V_{IN} = 12V, V_{GT} = 22V, R_T = 200kΩ, $I_{LOAD(12V)}$ < 10mA.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial Accuracy	T_A = 25°C	95	102	105	kHz
Accuracy Over Temperature		90		110	kHz
Dead Time	50kΩ ≤ R_T ≤ 300kΩ	400	800	1000	ns
Maximum Duty Cycle		90	94	98	%
Voltage Stability	6V ≤ V_{IN} <≤ 20V		2		%
Error Amplifiers					
Input Offset Voltage			2	10	mV
Input Bias Current	T_A > 0°C		10	200	nA
Output High Voltage	I_{OUT} = –2mA, T_A = 25°C	2.8	2.95		V
Output Low Voltage	I_{OUT} = 15µA, T_A = 25°C			0.6	V
Source Current	V_{OUT} = 2.5V	–5	–7		mA
Sink Current	V_{OUT} = 2.5V	10	50		µA
Gain-Bandwidth Product			675		kHz
High Side (OUT1) Outputs (Pins 10, 23)					
Output High Voltage	I_{OUT} = –20mA	19.5	21.3		V
Output Low Voltage	I_{OUT} = 20mA		0.2	0.5	V
Low Side (OUT2) **Outputs** (Pins 9, 26)					
Output High Voltage	I_{OUT} = –20mA	12.5	14.4		V
Output Low Voltage	I_{OUT} = 20mA		0.2	0.5	V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Soft Start and Current Limits (Pins 12, 20 21)					
Voltage Threshold	From V_{IN}	–250	–200	–150	mV
Bias Current	$V_{ISENSE} = V_{IN} - 200mV$		27	50	µA
Soft Start I_{CHARGE}		–6	–13		µA
Soft Start $I_{DISCHARGE}$		2	6.2		mA
Reference Section					
Output Voltage	$T_A = 25°C$, $I_{PIN31} = -1mA$	2.45	2.5	2.55	V
Line regulation	$5.4V < VIN < 20V$, $I_{PIN31} \leq -1mA$		0.3	2.0	mV/V
Total Variation	Line, load and temp.		7		%
12V Linear Regulator					
Output Voltage	$I_O = 60mA$	11.25	12	12.75	V
Line regulation	$16V < V_{GT} < 30V$		0.01		%/V
Drop Out Voltage (V_{GT}–V_{OUT})	$I_O = 10mA$		2.3	2.7	V
Load regulation	$10µA < I_O < 60mA$		±1.6	±3.2	%
5V Linear Regulator					
Output Voltage	$I_{OUT} = 1mA$	4.85	5.0	5.15	V
Input Voltage	$V_{OUT} \geq 4.85V$, $I_O = 1mA$	6.2			V
Line Regulation	$5.4V < V_{IN} < 20V$, $I_O = 1mA$		0.75	1.5	%
Load Regulation	$10µA < I_O < 25mA$		±1.5	±3	%
V_{BAT} and $V_{ADAPTER}$ Comparators					
Input Bias Current	$V_{IN} = 20V$, $T_A > 0°C$			200	nA
Input Offset Voltage				±40	mV
Battery Low V_{OL}	$I_{OL} = 200µA$			0.4	V
Battery Low V_{OH}	30KΩ pullup to 5V	4.5	5.0		V
VG5 Source Current	$V_{G5} = 12V$	–5	–10		mA
VG5 Sink Current	$V_{G5} = 12V$	85			mA
Power Management Drivers (Pins 13-15, 17-19)					
Source Current	$V_{SOUT} = 10V$	–8	–15	–30	µA
Sink Current	$V_{SOUT} = 10V$	8	15	30	µA
Output High Voltage	$I_{SOUT} = -20µA$	14.5	15.6		V
Output Low Voltage	$I_{SOUT} = 20µA$		0.16	0.4	V
Logic Inputs (Pins 8, 13-15, 30, 27)					
Logic Low (V_{IL}) (except Pin 8)	$I_{IN} \geq -5µA$			1.1	V
Logic Low (V_{IL}) Pin 8	$I_{IN} \geq -5µA$			0.6	V
Logic High (V_{IH})	$I_{IN} \geq 5µA$	2.5			V
Supply Current					
$I_{IN} + I_{GT}$	Sleep Mode, $T_A = 25°C$		115	250	µA
I_{IN}	Run Mode, $T_A = 25°C$		6	10	mA
I_{GT}	Run Mode, $T_A = 25°C$		4	6	mA

FUNCTIONAL DESCRIPTION

POWER DOWN MODES

The ML4862 operates in either a powered down mode or a run mode according to the state of the ON/OFF pin (Table 1). When the ON/OFF pin is high, the IC is in the run mode and all IC sections are functioning. When the ON/OFF pin is low, the IC is in the standby mode and only the µPower 5V linear regulator and 2.5V reference are on. All gate drive outputs are low. The 5V linear regulator then provides the power to run the system's power management logic. When the BURST pin is high, and the output is above the lower threshold of the burst comparator, the IC is also in standby mode, but with the burst comparator logic also running.

BUCK REGULATORS

The two buck regulators (Figure 3) are synchronously rectifying voltage mode PWM regulators capable of being used over a wide variety of loads and input voltages. The use of synchronous rectification improves system efficiency by reducing the fixed drop associated with the "freewheeling" diode in conventional regulators. These regulators also drive all N-Channel power MOSFETs, significantly improving system efficiency at a low cost. In order to drive the MOSFET gates adequately, a V_{GT} supply must be provided which is higher than the battery voltage by an amount sufficient to provide full enhancement voltage to the MOSFETs. This can be generated as shown below.

TABLE 1. ML4862 POWER DOWN MODES

MODE	ON/$\overline{OFF}$	$\overline{ENABLE\ A}$	ON/$\overline{OFF}$ 12	FUNCTION	TOTAL SUPPLY CURRENT
Sleep	0	X	X	Micro Power 5V Reg Only	130µA
12V	1	X	1	12V Linear Regulator on	600µA*
Partial Run	1	0	0	Reg. A Disabled, All Other Functions Running	8mA
Run	1	1	0	All Functions Enabled	10mA

***Note** This figure represents the total quiescent current for the Bust and 5V regulator. Actual current consumed will vary in proportion to load current.

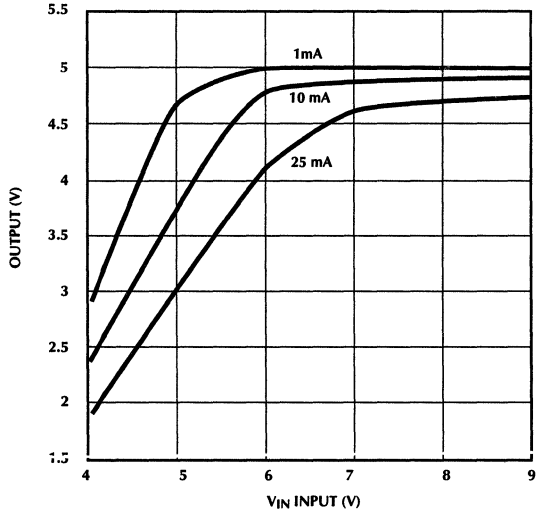


Figure 1. 5V Linear Regulator Output at low V_{IN}

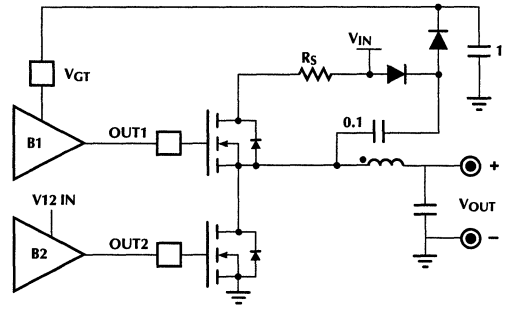


Figure 2. Generating V_{GT} Bias Voltage

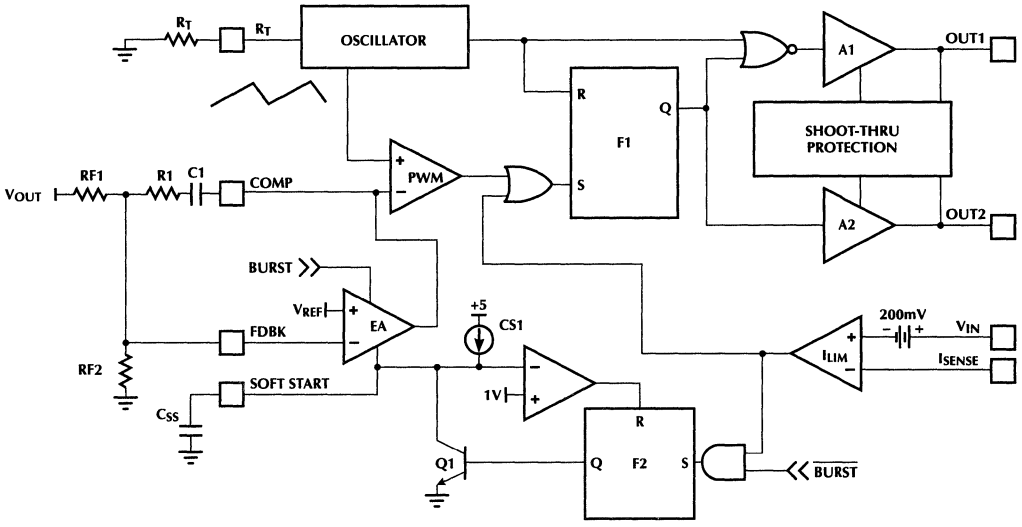


Figure 3. Buck Regulator Block Diagram

Regulator A includes a pin which shuts down the IC and puts Regulator A into "Burst mode". When in "Burst mode" the regulator comes on when the burst comparator is below its lower threshold and goes off again when the output capacitor has charged to the burst comparator's upper threshold. Burst mode is useful for running the regulator at light modes, such as memory keep-alive or "suspend" mode.

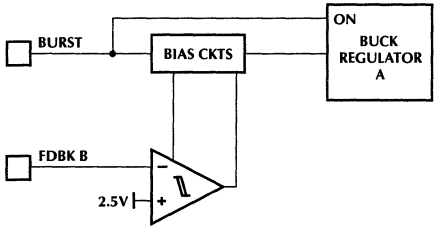


Figure 4. Burst Mode Comparator and Logic

When burst mode is enabled the C_{SS} discharge circuit (Figure 3) is disabled. C_{SS} is floating until CS1 is enabled when a burst occurs. When probing the C_{SS} pin in burst mode, use a high impedance probe to prevent discharge of the C_{SS} pin from disturbing the circuit operation.

Selection of the external MOSFETs, output inductor and capacitor determine the output capabilities of the regulator. Output voltage is set by RF1 and RF2 where.

$$V_{OUT} = \frac{2.5 \times (RF1 + RF2)}{RF2} \quad (1)$$

The short circuit limit is set by external resistor R_S.

$$I_{SHORT\ CKT} \approx \frac{0.2}{R_S} \quad (2)$$

C_{SS} is discharged when the regulator is off or when the voltage across R_S exceeds 200mV. F2 ensures that C_{SS} is fully discharged. This circuit provides reliable output short circuit protection with very little power wasted in the sensing element. The error amplifier's output voltage is limited to the voltage on the SOFT START pin. When C_{SS} is discharged, the regulator's duty cycle is 0.

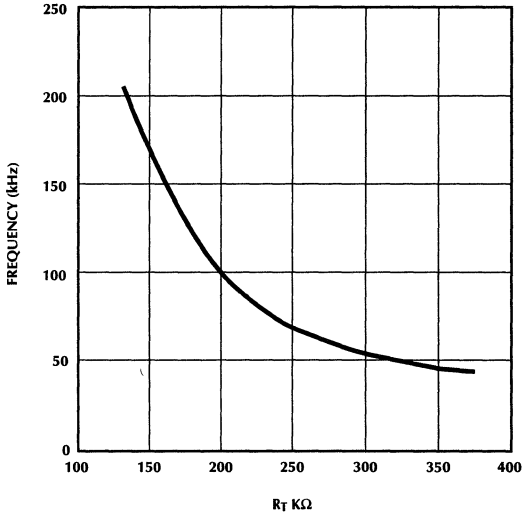


Figure 5. Oscillator Frequency vs. R_T

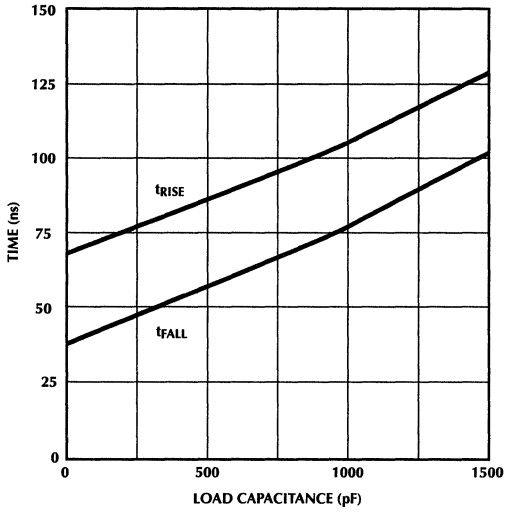


Figure 6. OUT1 Rise and Fall Time vs. Load C_{LOAD}

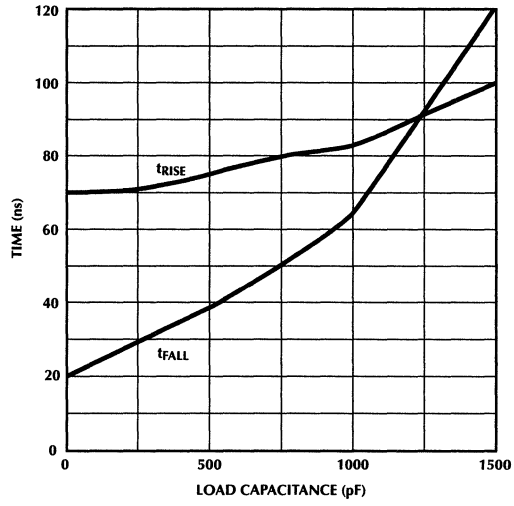


Figure 7. OUT2 Rise and Fall Time vs. Load C_{LOAD}

ADAPTER SWITCH

This function is provided by a comparator whose output (VG5) is pulled to V_{GT} when $V_{ADAPTER}$ goes above 2.5V. By connecting an N-Channel MOSFET gate to VG5, the system can run from the battery without the loss associated with a diode. When the AC adapter is plugged in, the voltage on pin 2 goes high, VG5 swings low, and the system runs from the AC adapter. This circuit functions in all modes of IC operation except SLEEP, when the VG5 output goes low.

12V LINEAR REGULATOR

The 12V regulator includes a shut-off pin. To operate the regulator as a low drop-out regulator, a separate 12VBIAS pin is provided. If this pin is 1.5V higher than V12 IN, the output transistor can be driven to saturation. Input for this regulator may come from either V_{IN} (for high voltage battery packs) or from a coupled inductor winding as shown in Figure 8. If the low drop-out feature is not necessary, V12 BIAS can be tied to V12 IN.

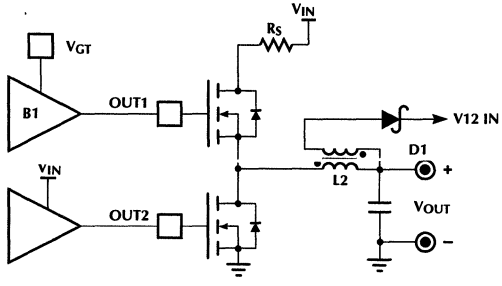


Figure 8. Coupled Inductor to generated V12 IN

APPLICATIONS

BUCK REGULATOR INDUCTOR

Inductors are specified with three main parameters; inductance (L), maximum current ($I_{OUT(MAX)}$), and DC resistance (R_L).

Inductance for a given set of requirements can be calculated using the following:

$$L = \frac{(V_{IN} - V_{OUT}) \times \left(\frac{D}{F}\right)}{(2) \times (I_{OUT(MIN)})} \qquad (3)$$

In this equation, D is the duty cycle, and F is the switching frequency.

Selecting the inductor value using this formula ensures that the inductor stays in the continuous current mode, and never goes discontinuous at light loads ($I_{OUT(MIN)}$). This is important, as high current spikes occur and losses go up when operating in the discontinuous mode.

A good rule of thumb for choosing inductor core size is to make sure that the maximum output current of the regulator doesn't exceed 80% of the maximum current rating of the inductor. Otherwise, core saturation may occur. This is especially important for ferrites, which have a harder saturation characteristic than powdered iron cores.

In order to distribute conduction losses evenly among all components, the DC resistance should be selected to be 1/4 of the sum of the RDS_{ON}s of the power MOSFETs.

Core losses, which contribute significantly to overall efficiency losses, should be minimized by using an inductor designed for minimum losses at the chosen operating frequency. This is a function of the core material, and is lowest in "Kool Mu" and molyperm cores. Of course, efficiency and cost are often inversely related when it comes to magnetic materials.

Figure 9 is a typical ML4862 Application Circuit. Table 2 provides a bill of materials for the circuit.

DESIGNATOR	DESCRIPTION	PART NUMBER
C14, C15	0.1µF, 50V (optional)	see text
D1	3A, 30V Rectifier	see text
D2	100mA, 50V (min) Rectifier	1N4148
D3–D7	Schottky Diode	1N5817 or MBRS130T3
L1	47µH, 1A	Sumida CRD125
L2	50µH, 1.5A	Coiltronics CTX05-11209-1
Q1–Q4	N-Channel Power MOSFET	MTD10N05E
Q5–Q7	N-Channel Power MOSFET	MMDF4N02
Q8	N-Channel Power MOSFET	Si9410
R10, R11	0.02 Ohm	see text

Table 2. Circuit Values for Typical Application (Figure 9).

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FREQUENCY SELECTION

Frequency is set by the resistor R_T, which establishes the charge current for the internal capacitor. Since the discharge current is a constant, the dead time of the oscillator is constant, the maximum duty cycle increases as the oscillator frequency decreases. For low input voltage applications, a lower switching frequency may be required to maintain regulation at minimum input voltage.

Losses are heavily comprised of AC losses from the switching characteristic of the power MOSFETs and inductor core losses. Hence, reducing the switching frequency may result in higher efficiencies. As inductor conduction losses will increase at lower frequencies (size goes up, hence there are more copper losses), there will be a point at which this effect cancels the beneficial effect on the AC losses and further reductions no longer increase efficiencies. Also, reductions in operating frequency will result in larger magnetics, and a larger overall supply.

COMPENSATION

Proper compensation is the most critical part of designing a working supply. The compensation network must ensure stability over the full range of input voltage and load conditions, as well as maximize the available bandwidth for good transient response.

If an appreciable ESR exists such than ResrC > LC/5, then we can get away with adding one additional zero to the error amplifier's feedback network, and make use of the other zero created by the combination of the ESR and the output capacitance. We must also add an additional resistance in parallel with the zero we have added, this will give us increased bandwidth and lower the DC gain. Its size is determined by the gain necessary to bring the system to 0dB at the desired crossover point. As a rule of thumb, this point should be no more than 1/5 the switching frequency.

In cases where the ESR of the output capacitors is minimal, we no longer have a zero for free.

Now, we must use a zero on the input of the error amplifier in addition to the zero in the feedback network. The parallel feedback resistor is also still required; the gain is now the parallel combination of the feedback zero resistor and this resistor.

The internal error amplifier has an open loop gain of 90 dB, and a single pole at 31Hz. These must be taken into account in order to adequately compensate the supply.

SEMI-STANDARD OPTIONS

The ML4862 can be quickly and easily modified to suit individual customer requirements. Examples of some of the possible customizations might include:

- Reducing the number of pins, or IC cost by eliminating unwanted functions
- Replacing unwanted functions with other functions
- Putting certain external programming components on chip to save board space

Please contact Micro Linear for more information on Semi-Standard options for the ML4862.

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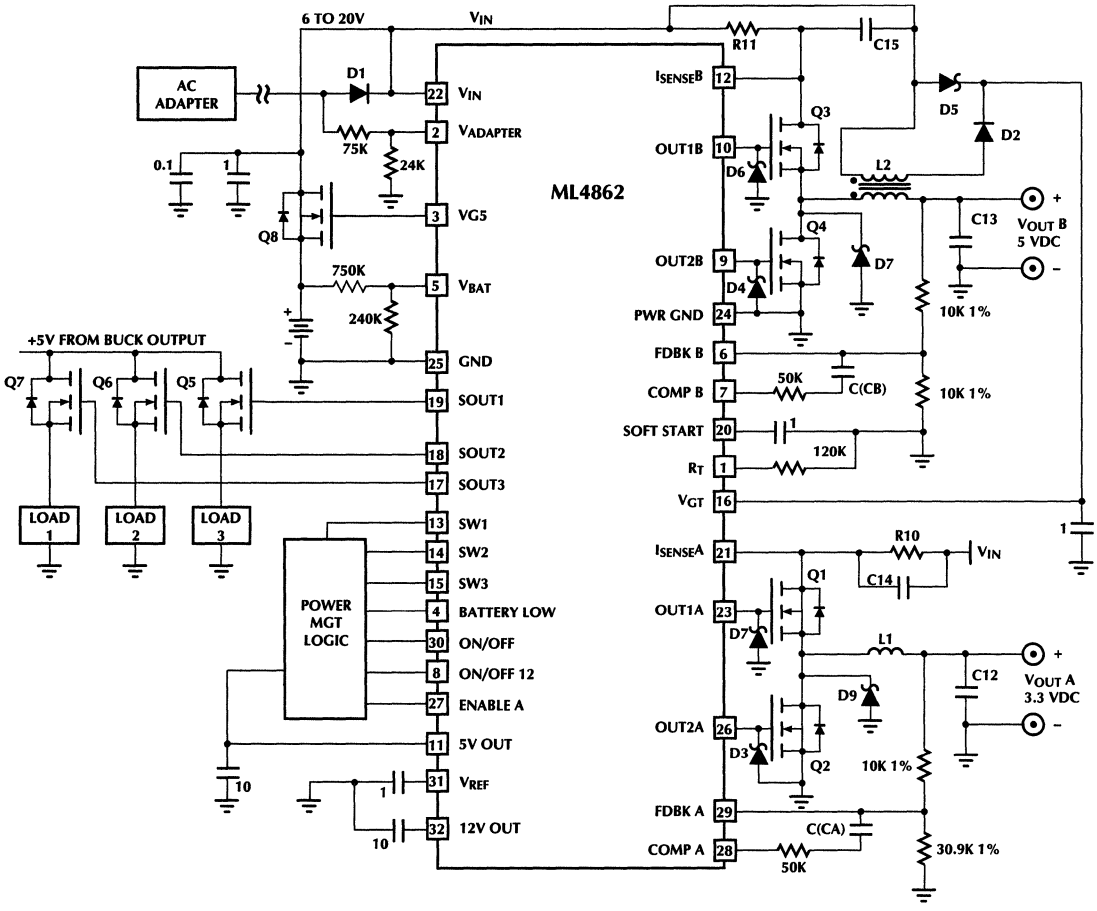


All Capacitors in µF, Schottky Diodes are 1N5817 except D6, D7 which are 1N5818 or 1N5819.

Figure 9. ML4862 Typical Application

TYPICAL PERFORMANCE CHARACTERISTICS

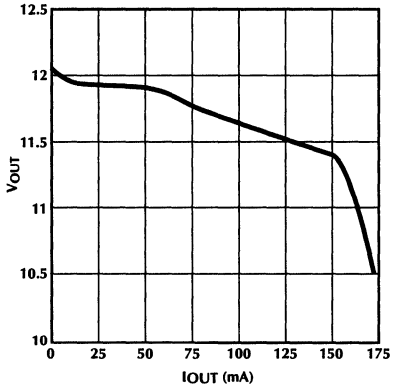


Figure 10. 12V Regulator Load Regulation

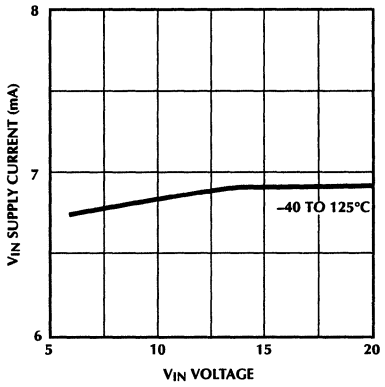


Figure 11. Supply Current (V_{IN}) vs. V_{IN} Voltage

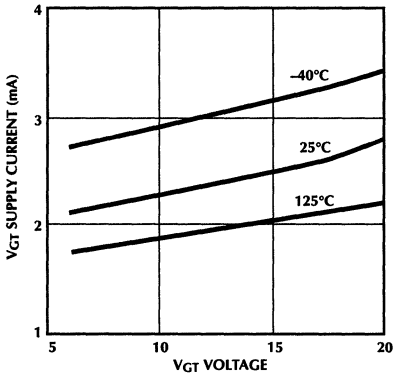


Figure 12. Supply Current (V_{GT}) vs V_{GT} Voltage

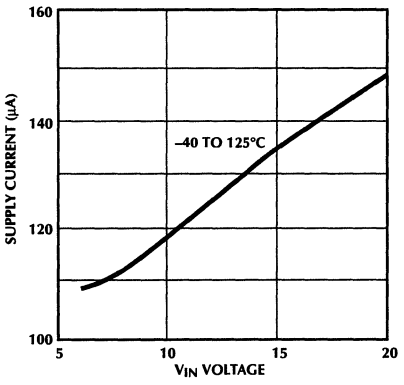


Figure 13. SLEEP Mode Current (V_{IN}) vs. V_{IN} Voltage

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4862CS	0°C to +70°C	28-Pin SOIC (S28W)

Micro Linear

ML4862EVAL

Battery Power Controller Evaluation Kit

GENERAL DESCRIPTION

The ML4862EVAL kit provides a convenient vehicle to evaluate the ML4862 battery power control IC. It contains all of the necessary documentation with the evaluation board and key components to quickly evaluate the application circuit. The board is designed for a 11W dual output power supply. However power components can be selected for higher or lower power applications.

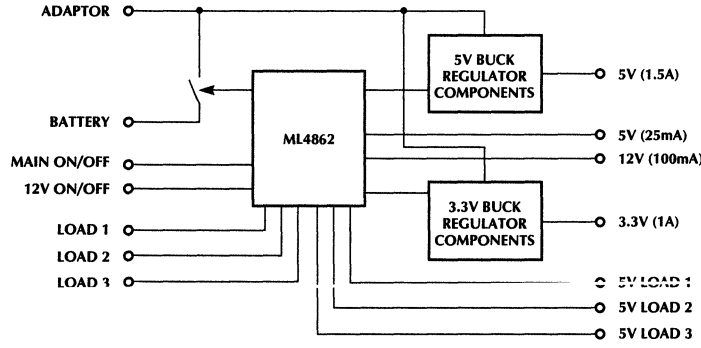
KIT COMPONENTS

- User's Guide
- ML4862 Datasheet
- Application Note
- ML4862 Sample
- Evaluation Board
- Key power semiconductor components
- SMD power inductors for both 5V and 3.3V outputs
- "Kool Mu®" toroid for inductor prototyping

FEATURES

- Wide Input Range (5.5V to 25V)
- Dual Outputs (5V at 1.5A and 3.3V at 1A)
- Efficiency as high as 95%.
- Line and Load Reg better than 5% at all conditions.
- Output Ripple to under 50mV pk-pk.
- Complete Short Circuit Protection
- Flash Memory Program Voltage (12V at 100mA)
- Load switching outputs.
- Battery connect terminals.

BLOCK DIAGRAM



Kool Mu is a registered trademark of Magnetics Division, Spang and Company.

FEATURING
Extended Commercial Temperature Range
–20°C to 70°C
for Portable Handheld Equipment

December 1994
PRELIMINARY

ML4863

High Efficiency Battery Pack Converter

GENERAL DESCRIPTION

The ML4863 is a complete solution for DC to DC conversion in multi-cell battery-powered portable computers and instruments. The circuit is optimized for flyback operation to enable power conversion from battery packs whose input voltage varies both above and below the output voltage requirements.

The ML4863 controls a synchronous rectified flyback regulator which drives low-cost N-Channel MOSFETs. This topology results high conversion efficiencies in PDAs and Personal Communications Devices.

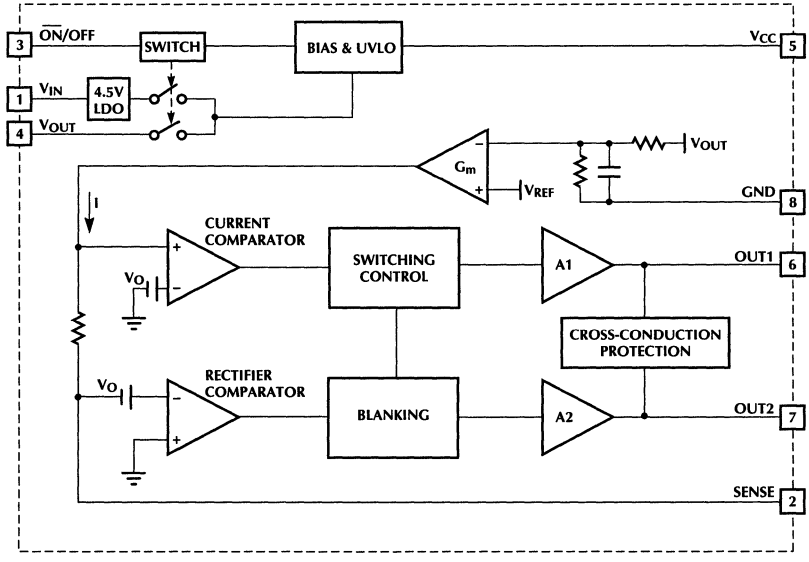
Current mode variable frequency operation is combined with synchronous switching to provide the highest power conversion efficiency over the widely varying loads required in today's power-managed portable computers (greater than 85% efficiency over a 1mA to 1A load range).

The circuit has been designed to operate with a minimum amount of off the shelf external components, optimizing space and cost. A totally configured DC-to-DC converter requires only 6 external components.

FEATURES

- Synchronous rectification for high efficiency
- N-Channel MOSFET drive for lowest cost
- Current mode, variable frequency operation for high efficiency over 3 decades of load current
- Start-up guaranteed at 3.15V
- Extended commercial temperature range (–20°C to 70°C) available
- Operates over a wide input voltage range (3.15V to 15V)
- Bootstrapped operation for improved performance with high impedance Alkaline or Lithium-Ion batteries
- High frequency operation (>200KHz) minimizes the size of the magnetics
- Over-voltage, and over-current protection on-board
- Active high shutdown
- Available in 8-pin DIP and SOIC packages
- Fixed 5V output and multiple output applications

BLOCK DIAGRAM



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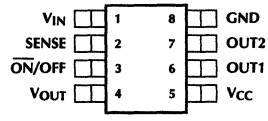
PIN CONFIGURATION

ML4863
8-Pin SOIC (SO8N)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	V_{IN}	Battery input voltage
2	SENSE	Secondary side current sense (voltage in)
3	$\overline{ON}$/OFF	Active low (CMOS) ON
4	V_{OUT}	Feedback from transformer secondary output, and input voltage for IC when $V_{IN} > V_{OUT}$
5	V_{CC}	Internal power supply connection for bypass capacitor
6	OUT1	Flyback primary switch driver
7	OUT2	Flyback secondary switch driver
8	GND	Ground

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Voltage on any pin (except V_{IN}) ..... –0.3V to 7V
Voltage on V_{IN} 18V
Source Current (OUT1 & OUT2) 1A
Sink Current (OUT1 & OUT2) 1A
Sink Current (Burst Mode) 165mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –60°C to +150°C
Lead Temperature (Soldering 10 Sec.) ..... +260°C
Thermal Resistance (θ_{JA}) Plastic SOIC ..... 110°C/W

OPERATING CONDITIONS

Ambient Temperature Range
ML4863CS ..... 0°C to +70°C
ML4863ES ..... –20°C to +70°C
V_{IN} Voltage Range ..... 3.15V to 15V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, V_{IN} = 12V, V_{OUT} = 5V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator						
On Time, T_{ON}		V_{IN} = 5V, V_{OUT} = 0V	2.35	2.5	2.65	µs
Minimum Off Time, T_{OFF}		V_{IN} = 5V, V_{OUT} = 0V	0.9	1	1.1	µs
Regulation						
Total Variation		Line, load, and temperature		±2	±3	%
Output Drivers (3nF load)						
OUT1	Rise Time, t_R			60	70	ns
	Fall time, t_F			60	70	ns
OUT2	Rise Time, t_R			60	70	ns
	Fall Time, t_F	Continuous mode		60	70	ns
		Burst mode		125	150	ns
$\overline{ON}$/OFF Pin						
Input High Voltage, V_{IH}			2.0			V
Input Low Voltage, V_{IL}					0.8	V
Input Bias Current		$\overline{ON}$/OFF = 5V		5		µA
Power Supply						
I_{CC}, Supply Current				100	150	µA
Protection						
Under-Voltage Lockout		Bypass Capacitor = 100nF	2.85	3.0	3.15	V
I_{SC}, Short Circuit Current Limit		R_{SENSE} = 100mΩ, L = 22µH		2	2.5	A

FUNCTIONAL DESCRIPTION

The ML4863 is a current mode, variable frequency controller with synchronous rectification. This device was designed primarily for use as a flyback converter in circuits where the user wishes to utilize 100% of a battery pack's available energy.

Initially, the circuit generates its bias from the input voltage. If the output voltage rises above the input voltage, the circuit will switch to the output for its bias, shutting off the low drop-out linear regulator at V_{IN} and turning on the bias network from the output pin.

The circuit uses constant on-time pulse frequency modulation, and runs in the continuous or discontinuous current mode depending on the load current sensed through R_{SENSE}.

Under-voltage lock-out, current limit, and cross-conduction protection are built-in.

DESIGN CONSIDERATIONS

CURRENT LIMIT AND MODE OF OPERATION

Operational mode and current limit are determined by the current programming comparator. They are dependent on

R_{SENSE}, the current sense resistor on the source of the secondary side synchronous FET,

L, the nominal transformer inductance,

and V_i, the input voltage (V_{IN}).

R_{SENSE} is determined by;

$$R_{SENSE} = \frac{165mV}{5 + V_{i\,MIN}} \times \frac{V_{i\,MIN}}{I_{O\,MAX}} \qquad (1)$$

Once R_{SENSE} has been determined, the nominal transformer inductance, L, can be derived from,

$$L = (25 \times 10^{-6}) \times V_{i\,MAX} \times R_{SENSE} \qquad (2)$$

Three operational modes are now defined by the value of SENSE at the end of the off-time: discontinuous mode, continuous mode, and current limit. The following values can be used to determine the current levels of each mode:

SENSE ≤ 0V → discontinuous mode

0V < SENSE < 165mV → continuous mode

165mV > SENSE > 210mV → current limit

To determine the current levels for:

$$I_O = \frac{V_i}{V_O + V_i} \times \left[\frac{SENSE}{R_{SENSE}} + \frac{t_{ON} \times V_i}{2 \times L} \right]$$

where

V_O = output voltage

t_{ON} = 2.5µs

and everything is defined as before. Using the values SENSE = 0V, SENSE = 165mV and SENSE = 210mV, the current levels for all operational modes are defined.

DESIGN PROCEDURE

A typical design can be implemented by using the following process.

1. Rate the application by determining

   $V_{i\,MAX}$, the maximum input voltage

   $V_{i\,MIN}$, the minimum input voltage

   $I_{O\,MAX}$, the maximum output current

   ΔV_{OUT}, the maximum output voltage ripple

   The maximum output voltage ripple must be below $100mV_{PP}$ to ensure stability.

2. Select a sense resistor, R_{SENSE}, using equation 1.

3. Determine the inductance required for optimum output ripple using

   $$L = (25 \times 10^{-6}) \times (V_{i\,MAX} \times R_{SENSE})$$

4. Establish the maximum allowable ESR for the output capacitor from

   $$R_{ESR} < \frac{\Delta V_{OUT} \times R_{SENSE}}{165mV}$$

5. Ensure system stability (no compensation/single pole response) by evaluating the following equation;

   $$\Delta V_{OUT} < \frac{100mV_{PP} \times L}{L_{ACTUAL}}$$

where

L_{ACTUAL} is the actual worst case inductance used.

DESIGN EXAMPLE

1. Rate the application by determining

$$V_{i\,MAX} = 9V$$

$$V_{i\,MIN} = 3V$$

$$I_{O\,MAX} = 1A$$

$$\Delta V_{OUT} = 100mV$$

The maximum output voltage ripple must be below 100mVPP to ensure stability.

2. Select a sense resistor, R_{SENSE},

$$R_{SENSE} = \frac{165mV}{5+3} \times \frac{5}{1} = 100m\Omega$$

3. Determine the inductance required for minimum output ripple using

$$L = (25 \times 10^{-6}) \times 9V \times 100m\Omega = 22\mu H$$

4. Establish the maximum allowable ESR for the output capacitor from

$$R_{ESR} < \frac{100mV \times 100m\Omega}{165mV} = 61m\Omega$$

5. Ensure system stability (no compensation/single pole response) by evaluating the following equation using 20% (typical inductance variation) for ΔL;

$$\Delta V_{OUT} < \frac{100mV_{PP} \times 22\mu H}{22\mu H(1-0.2)} = 125m\Omega$$

This design is shown in Figure 1. Figure 2 is the application circuit for an output of 2A at 5V.

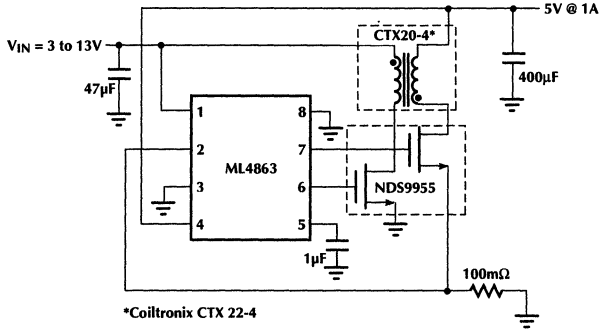


Figure 1. Design Example

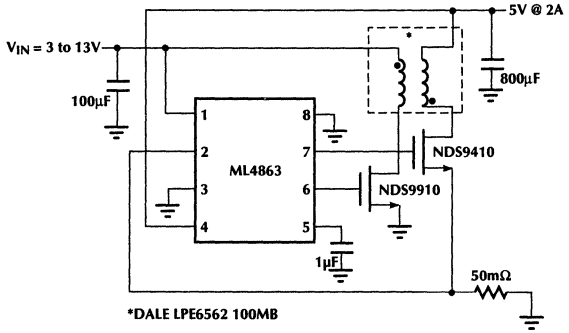


Figure 2. 5V, 2A Circuit

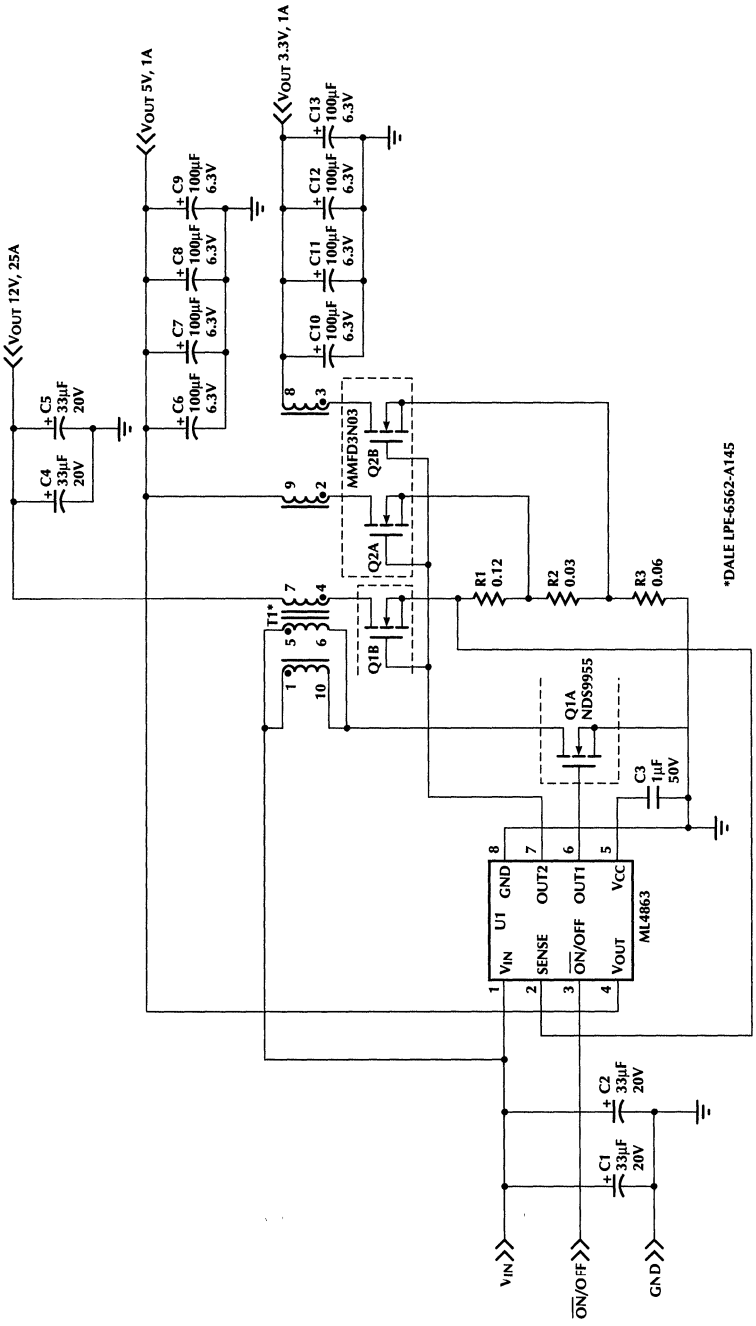


Figure 3. 5W Multiple Output Circuit.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4863CS	0°C to +70°C	8-Pin SOIC (SO8N)
ML4863ES	–20°C to +70°C	8-Pin SOIC (SO8N)

FEATURING
Extended Commercial Temperature Range
-20°C to 70°C
for Portable Handheld Equipment

September 1994
PRELIMINARY

ML4864

LCD Backlight Lamp Driver with Contrast

GENERAL DESCRIPTION

The ML4864 is a complete solution for controlling small cold cathode fluorescent tubes (CCFL) used in liquid crystal display (LCD) backlight applications. It provides the dimming ballast control combined with a contrast control for the LCD display.

The ML4864 is optimized for portable applications where high efficiency is critical to maximize battery life. The high efficiency is achieved by using a switching regulator in a buck configuration that feeds an inverter driver. The inverter uses a self synchronizing scheme with zero voltage switching for the lowest possible losses. The complete system implementation can be easily realized with standard off the shelf power components, including the magnetics.

A positive or negative contrast control voltage is generated with a separate flyback output. A unique feature of the ML4864 is that this contrast control voltage can remain active even though the main lamp driver circuit is disabled. It has a duty cycle adjustment range from 0% to 95%.

All of the regulators on the chip are synchronized to the inverter frequency to eliminate the ghosting and flicker common to asynchronous circuits.

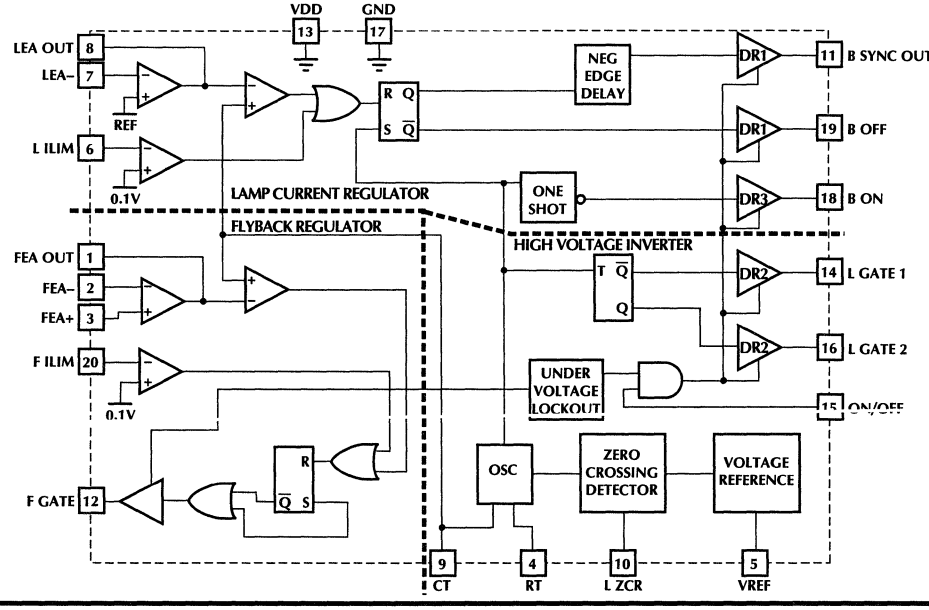
The ML4864 is available in very small form factor package (20-pin SSOP) making it ideal for hand held portable applications.

The ML4864 is designed using Micro Linear's Tile Array methodology. Customized versions of this IC, optimized to specific applications can be made available. Contact Micro Linear or an authorized representative for more information.

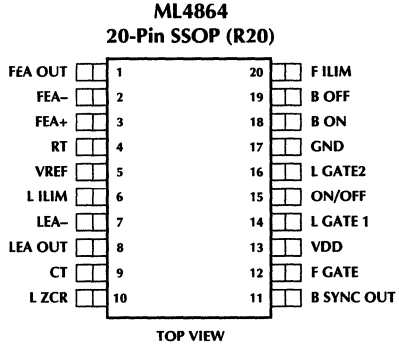
FEATURES

- Backlight Lamp Ballast and Contrast Control
- Low Standby Current (<300µA)
- Contrast Voltage is Active with Lamp Driver Disabled
- Improved Efficiency (≈95%)
- Allows All N-Channel MOSFET Drive
- Positive or Negative Contrast Control Voltage
- Driven Self-Timing Resonant Lamp Architecture
- Low Switching Losses
- Zero Voltage Switching
- Buck Regulator uses Synchronous Rectification

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	FEA OUT	Output of flyback (contrast) error amplifier. External compensation capacitor connects between this pin and FEA–.
2	FEA–	Negative input of the flyback (contrast) error amplifier. Connects to the center point of the voltage divider that sets the contrast voltage.
3	FEA+	Positive input of flyback (contrast) error amplifier. Connects to ground through an offset compensating resistor.
4	RT	Oscillator timing resistor.
5	VREF	Voltage reference output. The bottom or return connection for the voltage divider that sets the contrast voltage.
6	L ILIM	Current limit resistor connection. This resistor sets the current limit to protect lamp driver MOSFET pair.
7	LEA–	Negative input of the lamp error amplifier.
8	LEA OUT	Output of lamp error amplifier. External compensation capacitor connects between this pin and B EA–.
9	CT	Oscillator timing capacitor.
10	L ZCR	Zero crossing detector input. Connects to primary center tap of the output transformer.
11	B SYNC OUT	Output of MOSFET driver. Connects to switch device.
12	F GATE	Connects to gate of MOSFET in primary side of contrast control.
13	VDD	Positive power 5 volt input.
14	LGATE 1	Output of MOSFET driver. Connects to gate of one side of output MOSFET pair.
15	ON/OFF	Chip enable.
16	LGATE 2	Output of MOSFET driver. Connects to gate of one side of output MOSFET pair.
17	GND	Circuit and power common.
18	B ON	Drives the primary of the pulse transformer that supplies the bootstrap voltage for the synchronous rectifier device.
19	B OFF	Output of MOSFET driver. Connects to gate of device that disables the input power.
20	F ILIM	Current limit resistor connection. This resistor sets the current limit to protect the flyback MOSFET.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 75mA
Output Current, Source or Sink DC 250mA
Voltage on Pins 1-9, 11-20 ..... –0.3V to VDD + 0.3V
Current into Pin 10 ..... ±10mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic SSOP ..... 100°C/W

OPERATING CONDITIONS

Temperature Range
ML4864C ..... 0°C to 70°C
ML4864E ..... –20°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VDD = 5V ±5%, T_A = –20°C to 70°C, R_T = 82K, C_T = 47pF (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LAMP DRIVER SECTION					
Error Amplifier					
Open Loop Gain		50	60		dB
Offset Voltage		–15		+15	mV
Output High	I_{LOAD} = 5µA	2.8	3.0		V
Output Low	I_{LOAD} = 25µA		0.4	0.7	V
Bandwidth (–3dB)			1		MHz
Common Mode Range		–0.3		VREF	V
Input Bias Current			50	100	nA
Output Drivers					
Output High – B SYNC OUT, B OFF	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
Output Low – B SYNC OUT, B OFF	I_{LOAD} = 12mA		200	375	mV
Rise Time – B SYNC OUT, B OFF	C_{LOAD} = 100pF		20	50	ns
Fall Time – B SYNC OUT, B OFF	C_{LOAD} = 100pF		20	50	ns
Output High – B ON	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
Output Low – B ON	I_{LOAD} = 50mA		200	375	mV
Fall Time – B ON	C_{LOAD} = 2400pF, Note 2		45	80	ns
Oneshot					
Pulse Width		100	150	200	ns
Delay Timer					
Delay Time		20	35	55	ns
Current Limit Comparator					
Current Threshold		180	200	220	mV
Input Bias Current	V_{LILIM} = 0.1V		10	100	nA
Propagation Delay			125	250	ns

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FLYBACK REGULATOR SECTION					
Error Amplifier					
Open Loop Gain		60	70		dB
Offset Voltage		–15		+15	mV
Output High	I_{LOAD} = 5µA	2.8	3.0		V
Output Low	I_{LOAD} = 25µA		0.4	0.7	V
Bandwidth (–3dB)			1		MHz
Common Mode Range		–0.3		VREF	V
Input Bias Current			50	100	nA
Output Drivers					
Output High – F GATE	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
Output Low – F GATE	I_{LOAD} = 12mA		200	375	mV
Rise Time – F GATE	C_{LOAD} 100pF		20	50	ns
Fall Time – F GATE	C_{LOAD} = 100pF		20	50	ns
HIGH VOLTAGE INVERTER SECTION					
Oscillator					
Nominal Frequency		68	80	92	KHz
Discharge Current	V_{CT} = 2V	500	700	900	µA
Peak Voltage			2.5	2.7	V
Valley Voltage		0.8	1	1.2	V
Output Drivers					
Output High – LGATE 1, 2	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
Output Low – L GATE 1, 2	I_{LOAD} = 50mA		200	375	mV
Rise Time – L GATE 1, 2	C_{LOAD} = 1000pF		20	50	ns
Fall Time – L GATE 1, 2	C_{LOAD} = 1000pF		20	50	ns
Zero Crossing Detector					
Threshold		0.75	1.1	1.45	V
Hysteresis		250	500	750	mV
Under Voltage Detector					
Start Up Threshold		3.8	4.2	4.4	V
Hysteresis		150	300	450	mV
Logic Interface (ON/OFF)					
V_{IH}		2.0			V
V_{IL}				0.5	V
Input Bias Current			1	25	µA
Current Limit Comparator					
Current Threshold		180	200	220	mV
Input Bias Current	V_{FILIM} = 0.1V		10	100	nA
Propagation Delay			125	250	µs

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BIAS SECTION					
VDD Supply Current	ON/OFF = "1"		400	600	µA
VDD Current	ON/OFF = "0"		200	300	µA
VREF Load Regulation	I_{VREF} = 25µA		10	20	mV
VREF Output Voltage	T_A = 25°	2.47	2.5	2.53	V
VREF Output Voltage		2.465	2.5	2.535	V
VREF Line Regulation			20	30	mV

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.
Note 2: Actual load is 1200pF. The 2:1 transformer reflects an effective 2400pF.

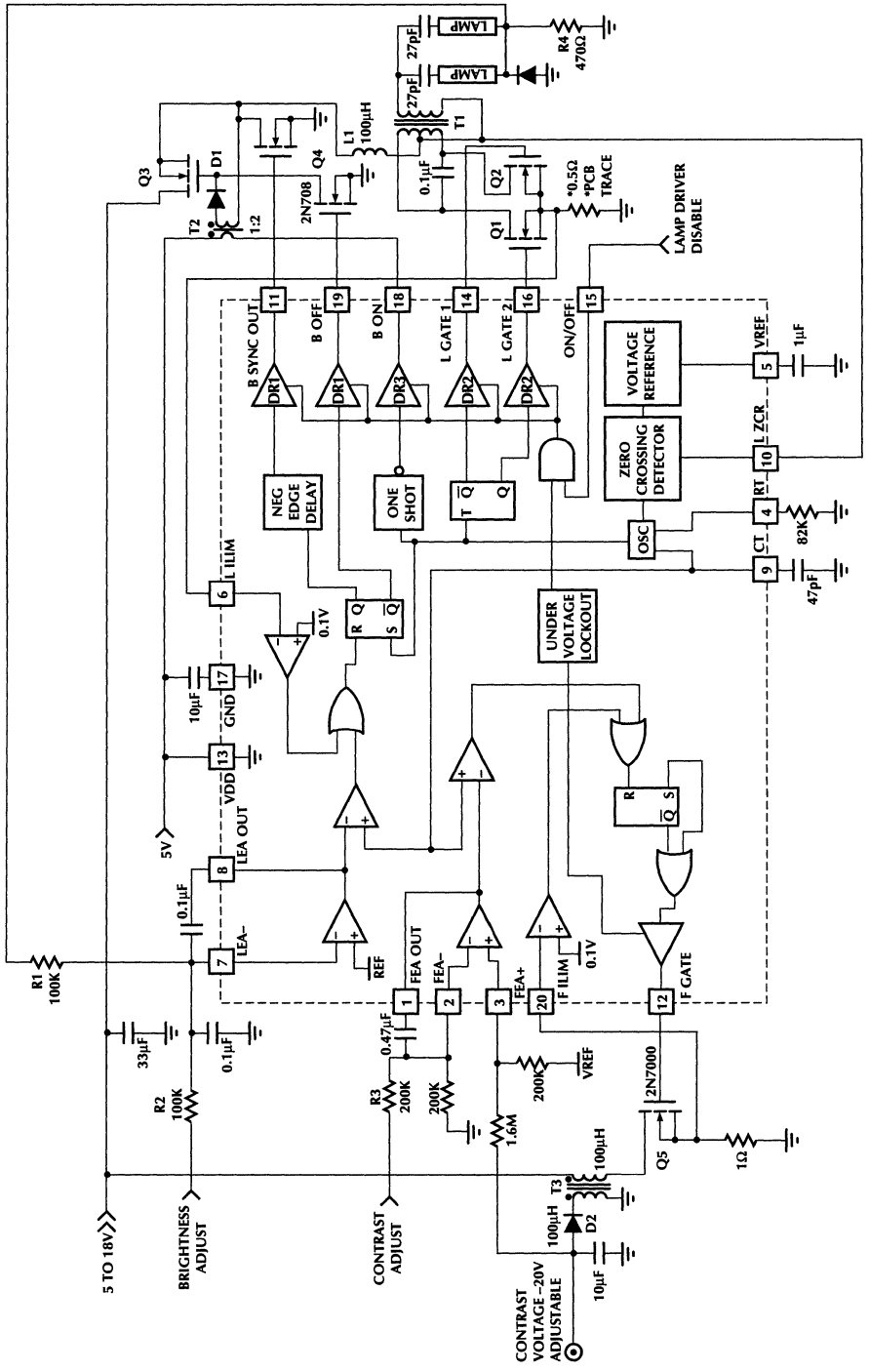


Figure 1. Typical Application Circuit.

FUNCTIONAL DESCRIPTION

The ML4864 consists of a PWM regulator, a lamp driver/ inverter, a flyback regulator, and control circuits. This IC, in conjunction with external components, converts a DC battery voltage into the high voltage and high frequency AC signal required to start and drive miniature cold cathode florescent lamps. In addition it generates the DC voltage for the contrast requirements of LCD screens. A typical application circuit is shown in figure 1. Please refer to application note 24 for detailed application information beyond what is presented here.

Note: Please read the Power Sequencing section below prior to using the ML4864.

LAMP DRIVER

The lamp driver, sometimes referred to as a lamp inverter, is comprised of a PWM regulator and a Royer type inverter circuit to drive the lamp. The PWM regulator, in a buck configuration, controls the magnitude of the lamp current to provide the dimming capability. Figure 2 shows a simplified circuit to more easily illustrate the operation of the circuit.

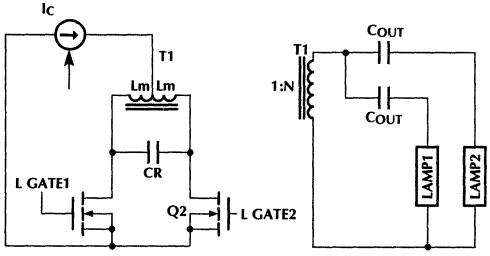


Figure 2. Simplified Lamp Driver Circuit.

Due to the presence of the buck inductor, L1, the circuit shown in figure 2 is essentially a current fed parallel loaded resonant circuit. Lm is the primary inductance of the output transformer, T1, which tunes with the resonant capacitor CR to set the resonant frequency of the inverter. The oscillator frequency is always set lower than the natural resonant frequency to ensure synchronization. The current source I_C models the current through the buck inductor L1.

The MOSFETs, Q1 and Q2 are alternately turned on with a constant 50% duty cycle signal (L GATE1 , L GATE2) at one-half the frequency of the oscillator. In this way each transistor pulses, or excites, the resonant tank on each half cycle. The combination of these two signals appear across the primary winding of the output transformer as a sinusoidal waveform. This voltage is multiplied by the step-up turns ratio of the output transformer and impressed across the lamp.

The output transitions are controlled by feedback through the L RTD pin by sensing the voltage at the center tap of the output transformer. Each time this signal reaches the minimum resonant threshold detection point an internal clock pulse is generated to keep the system synchronized. Figure 3 shows some of these representative waveforms at the important nodes of the circuit.

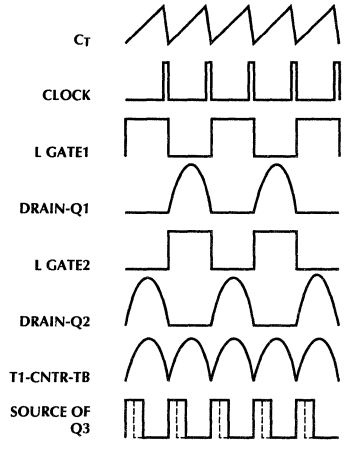


Figure 3. Operating Waveforms of the Lamp Driver Section.

The PWM regulator is comprised of a MOSFET Q3, inductor L1, and the gate control and drive circuitry as shown in figure 1. A signal with a constant pulse width of 150ns is applied to the primary of the 2:1 pulse transformer T2, rectified by diode D1, and used to charge the gate capacitance of Q3, thereby turning it on. The turn off is controlled by discharging this capacitance through MOSFET Q4. The pulse width of the signal on the gate of Q4 (B OFF) varies according to the amplitude of the feedback signal on LEA–, which is proportional to the AC current flowing in the lamp. This feedback signal is developed across resistor R4 which is in series with the lamp. The lamp current, and therefore brightness, is adjusted by varying the voltage applied to R2, at the brightness adjust control point. Increasing this voltage decreases the brightness.

CONTRAST CONTROL GENERATOR

The contrast voltage generator is a separate regulator in a flyback configuration. In conjunction with the external transformer (T3), MOSFET (Q5), diode (D2), and assorted capacitors and resistors, it provides an adjustable DC output contrast voltage necessary to drive LCD screens. The voltage is adjusted by controlling the voltage applied to R3, at the contrast adjustment point.

The contrast voltage can be made either positive or negative simply by changing the connection of the external components.. The schematic shown in figure 1 is connected for a negative voltage. Please refer to application note 24 for the circuit connection for a positive output voltage.

OSCILLATOR

The frequency of the oscillator in the ML4864 is set by selecting the values of RT and CT.

LOGIC CONTROL

The ML4864 is controlled by a logic input, ON/OFF. A logic level high on the ON/OFF pin enables just the lamp driver. A logic zero on the ON/OFF pin disables the lamp driver only.

POWER SEQUENCING

It is important to observe correct power and logic input sequencing when powering up the ML4864. The following procedure must be observed to avoid damaging the device.

1. Apply the VDD voltage.
2. Apply a logic high to the ON/OFF input.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4864CR	0°C to +70°C	Molded SSOP (R20)
ML4864ER	–20°C to +70°C	Molded SSOP (R20)

ML4864EVAL

LCD Backlight with Contrast Evaluation Kit

GENERAL DESCRIPTION

The ML4864 is a cold cathode fluorescent lamp (CCFL) controller featuring and dimming control and contrast voltage generation. It is commonly used to power the entire LCD display found in many handheld instruments. This evaluation board enables the designer to explore the capabilities of the circuit for a current or upcoming design.

The printed circuit board uses surface mount components for space efficiency with two adjustment potentiometers provided for controlling lamp intensity and contrast voltage levels.

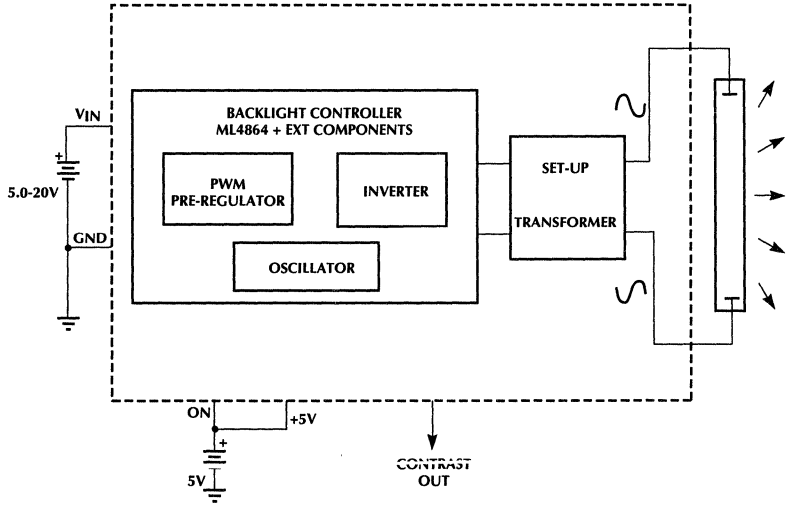
FEATURES

- Operates over a 5.0 to 20V supply range
- Efficiency greater than 90%
- Negative contrast voltage output (0 to –20V)
- Capable of driving lamp to greater than 5W
- Low profile, high Density PC board layout

KIT COMPONENTS

- ML4864 User's guide
- ML4864 Data Sheet
- A fully functional evaluation board
- Application Notes 26 and 32
- Miniature Fluorescent Lamp
- PCB Layout Gerber File

BLOCK DIAGRAM



ML4865

High Voltage High Current Boost Regulator

GENERAL DESCRIPTION

The ML4865 is a high voltage, continuous conduction boost regulator designed for DC to DC conversion in multiple cell battery powered systems. Continuous conduction allows the regulator to maximize output current for a given inductor. The maximum switching frequency can exceed 200kHz, allowing the use of small, low cost inductors. The ML4865 is capable of start-up with input voltages as low as 1.8V and is available in 15V and 12 V output versions with output voltage accuracy of ±3%.

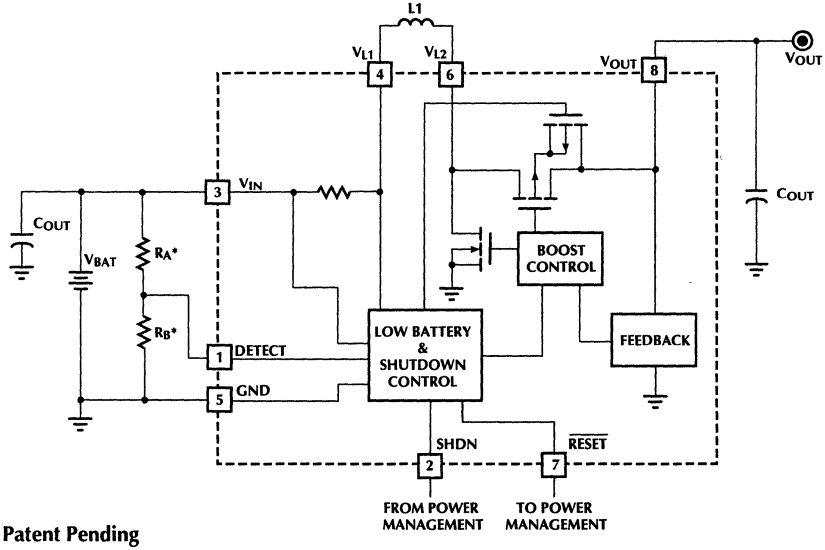
Unlike regulators using external Schottky diodes, the ML4875 isolates the load from the battery when the SHDN pin is high. This is accomplished by an integrated synchronous rectifier which eliminates the need for an external Schottky diode and provides a lower forward voltage drop, resulting in higher conversion efficiency. In addition, low quiescent battery current and variable frequency operation result in high efficiency even at light loads. The ML4865 requires only one inductor and two capacitors to build a very small regulator circuit capable of achieving conversion efficiencies approaching 90%.

The circuit also contains a $\overline{\text{RESET}}$ output which goes low when the DETECT input drops below 1.25V.

FEATURES

- Guaranteed full load start-up and operation at 1.8V input
- Continuous conduction mode for high output current
- Very low supply current (25µA output referenced) for micropower operation
- Pulse Frequency Modulation and Internal Synchronous Rectification for high efficiency
- Maximum switching frequency > 200kHz
- Minimum external components
- Low ON resistance internal switching FETs
- 15V and 12V output versions

BLOCK DIAGRAM

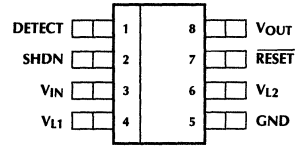


Patent Pending

***Optional**

PIN CONFIGURATION

ML4865-5/-2
8-Pin SOIC (S08)



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	DETECT	Pulling this pin below 1.25V causes the $\overline{\text{RESET}}$ pin to go low
2	SHDN	Pulling this pin to V_{IN}, through an external resistor shuts down the regulator, isolating the load from the input
3	V_{IN}	Battery input voltage
4	V_{L1}	Boost inductor connection
5	GND	Ground
6	V_{L2}	Boost inductor connection
7	$\overline{\text{RESET}}$	Output goes low when DETECT goes below 1.25V
8	V_{OUT}	Boost regulator output

ORDERING INFORMATION

PART NUMBER	OUTPUT VOLTAGE	TEMPERATURE RANGE	PACKAGE
ML4865ES-2	12.0V	–20°C to +70°C	8-Pin SOIC (S08)
ML4865ES-5	15.0V	–20°C to +70°C	8-Pin SOIC (S08)

ML4866

3.3V Output DC-DC Step-Down Converter

GENERAL DESCRIPTION

The ML4866 is a fully monolithic high efficiency (>90%), pulse width modulated (PWM) buck regulator. The device switches at 120kHz and uses synchronous rectification to optimize power conversion efficiency. Unlike other solutions, the ML4866 requires no external diodes or FETs.

Designed for use in systems using mixed-voltages (5V and 3.3V) or in portable computing equipment designed with 3.3V ICs, the ML4866 can provide up to 750mA of output current at 3.3V. The circuit operates over an input voltage range of 3.5V to 6.5V (3 to 4 AA batteries in series or a 5V DC supply).

A complete 3.3V, 750mA switched mode power converter can be quickly and easily implemented with few external components. Power conversion efficiency of this DC-DC converter can exceed 90% over more than 2 decades of output current loading.

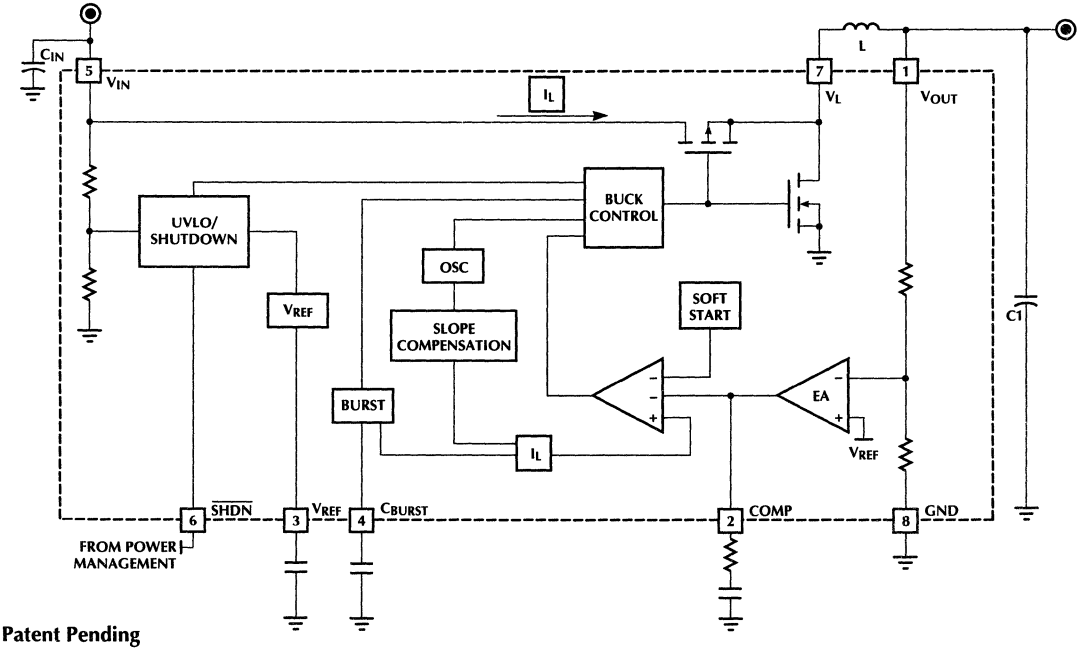
The device also has a $\overline{\text{SHDN}}$ pin for use in systems which have power management control. In shutdown mode, the circuit uses less than 20µA of input current.

Stability and fast loop response are provided by current programming and a patented current sense circuit. Undervoltage lockout and soft start are also built in.

FEATURES

- High Power Conversion Efficiency (>90%) over more than 2 decades of load current
- Minimal external components required
- Works down to 3.5V input
- Extends battery life up to 30% over linear regulator based solutions
- Micropower operation (I_Q < 350µA)
- Shutdown quiescent current (I_{SD} < 20µA)
- No external FETs or diodes required

BLOCK DIAGRAM



Patent Pending

FEATURING
Extended Commercial Temperature Range
–20°C to 70°C
for Portable Handheld Equipment

December 1994
PRELIMINARY

ML4868

High Frequency, Low Voltage Boost Regulator

GENERAL DESCRIPTION

The ML4868 is a high frequency boost regulator designed for DC to DC conversion in 2 to 3 cell battery powered systems. The maximum switching frequency can exceed 150kHz, allowing the use of small, low cost inductors. The ML4868 is capable of start-up with input voltages as low as 1V and is available in 5V and 3.3V output versions with an output voltage accuracy of ±3%.

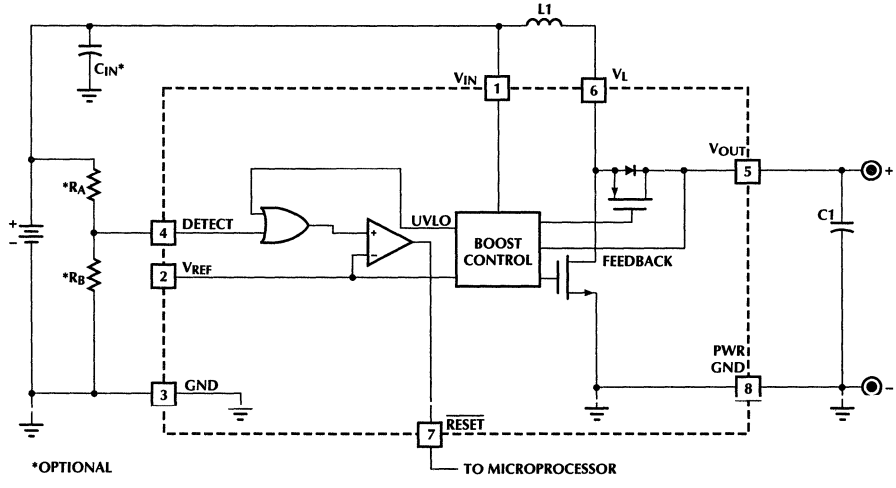
An integrated synchronous rectifier eliminates the need for an external Schottky diode and provides a lower forward voltage drop, resulting in higher conversion efficiency. In addition, low quiescent battery current and variable frequency operation result in high efficiency even at light loads. The ML4868 requires only one inductor and two capacitors to build a very small regulator circuit capable of achieving conversion efficiencies in excess of 90%.

The circuit also contains a $\overline{\text{RESET}}$ output which goes low when the IC can no longer function due to low input voltage, or when the DETECT input drops below 200mV.

FEATURES

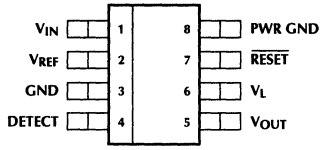
- Maximum switching frequency > 150kHz
- Pulse Frequency Modulation and Internal Synchronous Rectification for high efficiency
- Minimum external components
- Low ON resistance internal switching FETs
- Micropower operation
- 5V and 3.3V output versions

BLOCK DIAGRAM



PIN CONNECTION

ML4868-5/-3
8-Pin SOIC (S08)



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	V_{IN}	Battery input voltage
2	V_{REF}	200mV reference output
3	GND	Analog signal ground
4	DETECT	When this pin below V_{REF}, causes the $\overline{RESET}$ pin to go low
5	V_{OUT}	Boost regulator output
6	V_L	Boost inductor connection
7	$\overline{RESET}$	Output goes low when regulation cannot be achieved or when DETECT goes below 200mV
8	PWR GND	Return for the NMOS output transistor

7

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Voltage on any pin 7V
Peak Switch Current, $I_{(PEAK)}$ 2A
Average Switch Current, $I_{(AVG)}$ 500mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C

Thermal Resistance (θ_{JA})
Plastic SOIC ..... 110°C/W

OPERATING CONDITIONS

Temperature Range
ML4868CS-X ..... 0°C to +70°C
ML4868ES-X ..... –20°C to +70°C
ML4868IS-X ..... –40°C to +85°C
V_{IN} Operating Range
ML4868CS-X ..... 1.0V to V_{OUT} –0.2V
ML4868ES-X, ML4868IS-X ..... 1.1V to V_{OUT} –0.2V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = Operating Voltage Range, T_A = Operating Temperature Range.

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Supply					
V_{IN} Current	$V_{IN} = V_{OUT} - 0.2V$		45	55	µA
V_{OUT} Quiescent Current			8	10	µA
V_L Quiescent Current				1	µA
Reference					
Output Voltage (V_{REF})	$0 < I_{PIN2} < -5µA$,	190	200	210	mV
PFM Regulator					
Pulse Width (T_{ON})		2.5	3	3.5	µs
Output Voltage (V_{OUT})					
ML4868-5	T_{ON} = 0 at V_{OUT}(MAX),	4.85	5.0	5.15	V
ML4868-3	2.5µs ≤ T_{ON} ≤ 3.5µs V_{OUT}(MIN)	3.2	3.3	3.4	V
Load Regulation	See Figure 1				
ML4861-5	V_{IN} = 2.4V, I_{OUT} ≤ 25mA	4.85	5.0	5.15	V
ML4861-3	V_{IN} = 2.4V, I_{OUT} ≤ 40mA	3.2	3.3	3.4	V
Under-Voltage Lockout Threshold			0.85	0.95	V
$\overline{\text{RESET}}$ Comparator					
DETECT Threshold		190	200	210	mV
DETECT Bias Current		–100		100	nA
$\overline{\text{RESET}}$ Output High Voltage (V_{OH})	I_{OH} = –100µA	V_{OUT} – 0.2			V
$\overline{\text{RESET}}$ Output Low Voltage (V_{OL})	I_{OL} = 100µA			0.2	V

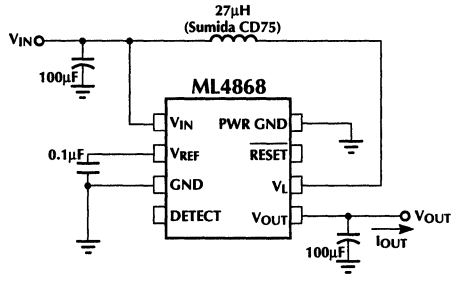


Figure 1. Application Test Circuit

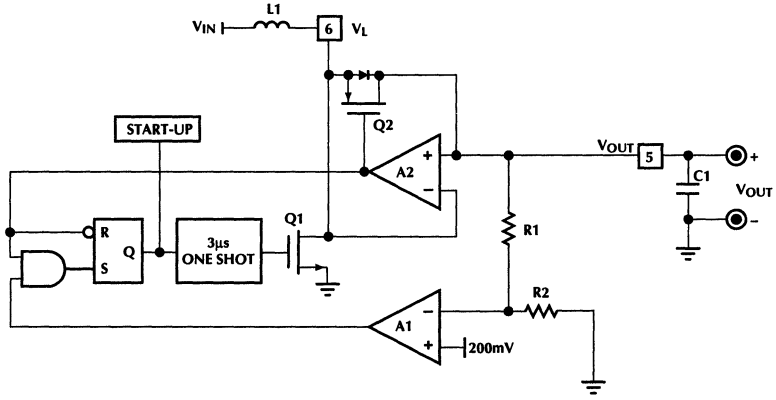


Figure 2. PFM Regulator Block Diagram

7

FUNCTIONAL DESCRIPTION

The ML4868 combines Pulse Frequency Modulation (PFM) and synchronous rectification to create a boost converter that is both highly efficient and simple to use. A PFM regulator charges a single inductor for a fixed period of time and then completely discharges before another cycle begins, simplifying the design by eliminating the need for conventional current limiting circuitry. Synchronous rectification is accomplished by replacing an external Schottky diode with an on-chip PMOS device, reducing switching losses and external component count.

REGULATOR OPERATION

A block diagram of the boost converter is shown in Figure 2. The circuit remains idle when V_{OUT} is at or above the desired output voltage, drawing 45µA from V_{IN}, and 8µA from V_{OUT} through the feedback resistors R1 and R2. When V_{OUT} drops below the desired output level, the output of amplifier A1 goes high, signaling the regulator to deliver charge to the output. Since the output of amplifier A2 is normally high, the flip-flop captures the A1 set signal and creates a pulse at the gate of the NMOS transistor Q1. The NMOS transistor will charge the inductor L1 for 3µs, resulting in a peak current given by:

$$I_{L(PEAK)} = \frac{T_{ON} \times V_{IN}}{L_1} \approx \frac{3\mu s \times V_{IN}}{L_1} \qquad (1)$$

For reliable operation, L1 should be chosen so that $I_{L(PEAK)}$ does not exceed 2A.

When the one-shot times out, the NMOS transistor releases the V_L pin, allowing the inductor to fly-back and momentarily charge the output through the body diode of PMOS transistor Q2. But, as the voltage across the PMOS transistor changes polarity, its gate will be driven low by the current sense amplifier A2, causing Q2 to short out its body diode. The inductor then discharges into the load through Q2. The output of A2 also serves to reset the flip-flop and one-shot in preparation for the next charging cycle. A2 releases the gate of Q2 when its current falls to zero. If V_{OUT} is still low, the flip-flop will immediately initiate another pulse. The output capacitor (C1) filters the inductor current, limiting output voltage ripple. Inductor current and one-shot waveforms are shown in Figure 3.

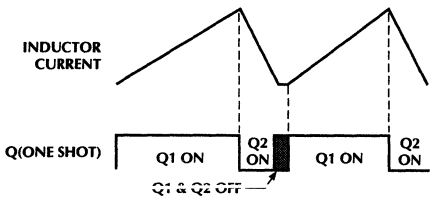


Figure 3. PFM Inductor Current Waveforms and Timing.

$\overline{\text{RESET}}$ COMPARATOR

An additional comparator is provided to detect low V_{IN}, or any other error condition that is important to the user. The inverting input of the comparator is internally connected to V_{REF}, while the non-inverting input is provided externally at the DETECT pin. The output of the comparator is the $\overline{\text{RESET}}$ pin, which swings from V_{OUT} to GND when an error is detected.

DESIGN CONSIDERATIONS

INDUCTOR

Selecting the proper inductor for a specific application usually involves a trade-off between efficiency and maximum output current. Choosing too high a value will keep the regulator from delivering the required output current under worst case conditions. Choosing too low a value causes efficiency to suffer. It is necessary to know the maximum required output current and the input voltage range to select the proper inductor value. The maximum inductor value can be estimated using the following formula:

$$L_{MAX} = \frac{V_{IN(MIN)}^{2} \times T_{ON(MIN)} \times \eta}{2 \times V_{OUT} \times I_{OUT(MAX)}} \qquad (2)$$

where η is the efficiency, typically between 0.8 and 0.9. Note that this is the value of inductance that just barely delivers the required output current under worst case conditions. A lower value may be required to cover inductor tolerance, the effect of lower peak inductor currents caused by resistive losses, and minimum dead time between pulses.

Another method of determining the appropriate inductor value is to make an estimate based on the typical performance curves given in Figures 4 and 5. Figure 4 shows maximum output current as a function of input voltage for several inductor values. These are typical performance curves and leave no margin for inductance and ON-time variations. To accommodate worst case conditions, it is necessary to derate these curves by at least 10% in addition to inductor tolerance.

For example, a two cell to 5V application requires 25mA of output current while using an inductor with 15% tolerance. The output current should be derated by 25% to 31mA to cover the combined inductor and ON-time tolerances. Assuming that 2V is the end of life voltage of a two cell input, Figure 4 shows that with a 2V input, the ML4868-5 delivers 34mA with a 22µH inductor.

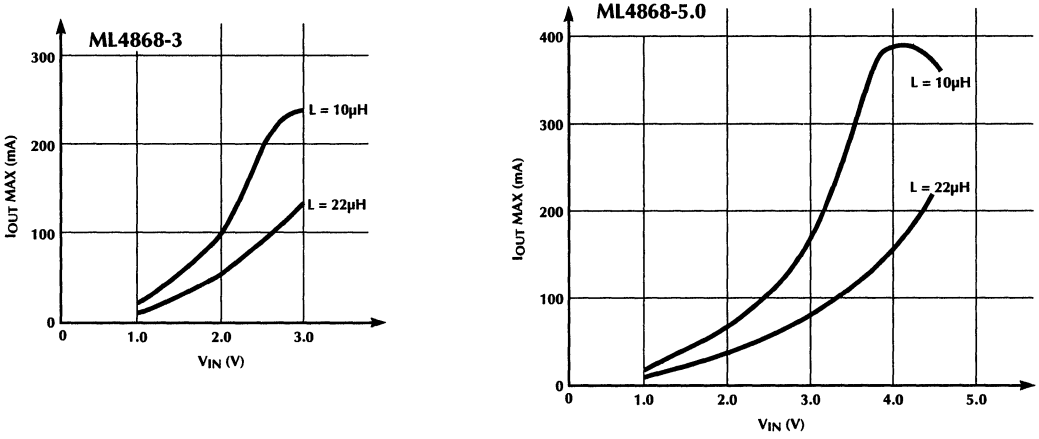


Figure 4. Output Current vs Input Voltage.

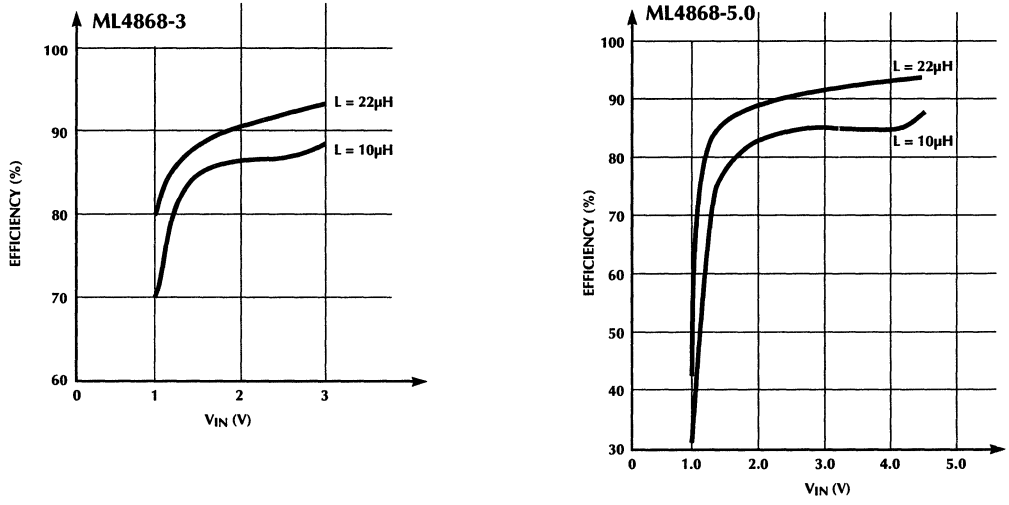


Figure 5. Typical Efficiency as a Function of V_{IN}.

7

Figure 5 shows efficiency under the conditions used to create Figure 4. It can be seen that efficiency is closely related to inductor value. This illustrates the need to keep the inductor value as high as possible to attain peak system efficiency. With 22µH, the efficiency exceeds 90% and there is little room for improvement. At values greater than 39µH, the operation of the synchronous rectifier becomes unreliable because the inductor current is so small that it is difficult for the control circuitry to detect. The data used to generate Figures 4 and 5 is provided in Table 1.

Figures 4 and 5 also show that efficiency and output current fall off at low input voltages. This is caused by propagation delays in the synchronous rectifier control circuitry that degrade performance when the discharge time is less than 1µs. Although it is possible to operate the ML4868 from a single cell, other devices in the Micro Linear product line will provide much better performance in this type of application.

After the appropriate inductor value is chosen, it is necessary to find the minimum inductor current rating required. Peak inductor current is determined from the following formula:

$$I_{L(PEAK)} = \frac{T_{ON(MAX)} \times V_{IN(MAX)}}{L_{MIN}} \quad (3)$$

In the two cell application previously described, a maximum input voltage of 3V would give a peak current of 560mA. When comparing various inductors, it is important to keep in mind that suppliers use different criteria to determine their ratings. Many use a conservative current level, where inductance has dropped to 90% of its normal level. In any case, it is a good idea to try inductors of various current ratings with the ML4868 to determine which inductor is the best choice. Check efficiency and maximum output current, and if a current probe is available, look at the inductor current to see if it looks like the waveform shown in Figure 3. For additional information, see Applications Note 29, "Choosing an Inductor for Your ML4861 Application."

Suitable inductors can be purchased from the following suppliers:

Coilcraft	(708) 639-6400
Coiltronics	(407) 241-7876
Dale	(605) 665-9301
Sumida	(708) 956-0666

OUTPUT CAPACITOR

The choice of output capacitor is also important, as it controls the output ripple and optimizes the efficiency of the circuit. Output ripple is influenced by three capacitor parameters: capacitance, ESR, and ESL. The contribution due to capacitance can be determined by looking at the change in capacitor voltage required to store the energy delivered by the inductor in a single charge-discharge cycle, as determined by the following formula:

$$\Delta V_{OUT} = \frac{T_{ON}^2 \times V_{IN}^2}{2 \times L \times C \times (V_{OUT} - V_{IN})} \quad (4)$$

For a 2.4V input, and 5V output, a 22µH inductor, and a 22µF capacitor, the expected output ripple due to capacitor value is 20mV.

Capacitor Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL), also contribute to the output ripple due to the inductor discharge current waveform. Just after the NMOS transistor turns off, the output current ramps quickly to match the peak inductor current. This fast change in current through the output capacitor's ESL causes a high frequency (5ns) spike that can be over 1V in magnitude. After the ESL spike settles, the output voltage still has a ripple component equal to the inductor discharge current times the ESR. This component will have a sawtooth shape and a peak value equal to the peak inductor current times the ESR. ESR also has a negative effect on efficiency by contributing I-squared R losses during the discharge cycle.

An output capacitor with a capacitance of 100µF, an ESR of less than 0.1Ω, and an ESL of less than 5nH is a good general purpose choice. Tantalum capacitors which meet these requirements can be obtained from the following supplier:

Sprague	(603) 224-1961

If ESL spikes are causing output noise problems, an EMI filter can be added in series with the output.

INPUT CAPACITOR

Unless the input source is a very low impedance battery, it will be necessary to decouple the input with a capacitor with a value of between 22µF and 47µF. This provides the benefits of preventing input ripple from affecting the ML4868 control circuitry, and it also improves efficiency by reducing I-squared R losses during the charge and discharge cycles of the inductor. Again, a low ESR capacitor (such as tantalum) is recommended.

REFERENCE CAPACITOR

Under some circumstances input ripple cannot be reduced effectively. This occurs primarily in applications where inductor currents are high, causing excess output ripple due to "pulse grouping", where the charge-discharge pulses are not evenly spaced in time. In such cases it may be necessary to decouple the reference pin (V_{REF}) with a small 10nF to 100nF ceramic capacitor. This is particularly true if the ripple voltage at V_{IN} is greater than 100mV.

SETTING THE $\overline{\text{RESET}}$ THRESHOLD

To use the $\overline{\text{RESET}}$ comparator as an input voltage monitor, it is necessary to use an external resistor divider tied to the DETECT pin as shown in the block diagram. The resistor values R_A and R_B can be calculated using the following equation:

$$V_{IN(MIN)} = 0.2 \times \frac{(R_A + R_B)}{R_B} \quad (5)$$

The value of R_B should be 100kΩ or less to minimize bias current errors. R_A is then found by rearranging the equation:

$$R_A = R_B \times \left(\frac{V_{IN(MIN)}}{0.2} - 1 \right) \quad (6)$$

LAYOUT

Good PC board layout practices will ensure the proper operation of the ML4868. Important layout considerations include:

- Use adequate ground and power traces or planes
- Keep components as close as possible to the ML4868
- Use short trace lengths from the inductor to the V_L pin and from the output capacitor to the V_{OUT} pin
- Use a single point ground for the ML4868 ground pins, and the input and output capacitors

TABLE 1. MAXIMUM OUTPUT CURRENT AND EFFICIENCY.

ML4868-3.3

V_{IN} (V)	I_{IN} (mA)	I_{OUT} (mA)	EFFICIENCY %
L = 22µH			
1.0	41.7	10.1	79.9
1.5	72.6	29.2	88.5
2.0	109.2	59.8	90.4
2.5	139.9	96.8	91.3
3.0	168.4	141.3	92.3
L = 10µH			
1.0	75.1	15.9	69.9
1.5	136.4	51.0	82.3
2.0	200.1	103.2	85.1
2.5	311.6	198.6	84.1
3.0	297.5	235.7	87.1

ML4868-5.0

V_{IN} (V)	I_{IN} (mA)	I_{OUT} (mA)	EFFICIENCY %
L = 22µH			
1.0	30.7	2.7	44.0
1.5	65.5	16.2	82.4
2.0	95.9	33.7	87.9
2.5	133.0	59.8	89.9
3.0	163.8	89.4	91.0
3.5	194.5	124.8	91.7
4.0	224.1	165.4	92.3
4.5	247.7	207.4	93.0
L = 10µH			
1.0	54.5	3.4	31.2
1.5	124.4	28.0	75.0
2.0	183.3	60.1	82.0
2.5	248.8	105.1	84.5
3.0	317.5	163.1	85.6
3.5	454.8	270.7	85.0
4.0	573.0	386.6	84.3
4.5	459.9	364.9	88.2

7

ORDERING INFORMATION

PART NUMBER	OUTPUT VOLTAGE	TEMPERATURE RANGE	PACKAGE
ML4868CS-3	3.3V	0°C to +70°C	8-Pin SOIC (S08)
ML4868CS-5	5.0V	0°C to +70°C	8-Pin SOIC (S08)
ML4868ES-3	3.3V	–20°C to +70°C	8-Pin SOIC (S08)
ML4868ES-5	5.0V	–20°C to +70°C	8-Pin SOIC (S08)
ML4868IS-3	3.3V	–40°C to +85°C	8-Pin SOIC (S08)
ML4868IS-5	5.0V	–40°C to +85°C	8-Pin SOIC (S08)

FEATURING
Extended Commercial Temperature Range
–20°C to 70°C
for Portable Handheld Equipment

December 1994
ADVANCED INFORMATION

ML4871

High Current Boost Regulator

GENERAL DESCRIPTION

The ML4871 is a continuous conduction boost regulator designed for DC to DC conversion in multiple cell battery powered systems. Continuous conduction allows the regulator to maximize output current for a given inductor. The maximum switching frequency can exceed 200kHz, allowing the use of small, low cost inductors. The ML4871 is capable of start-up with input voltages as low as 1.8V and is available in 5V and 3.3V output versions with output voltage accuracy of ±3%.

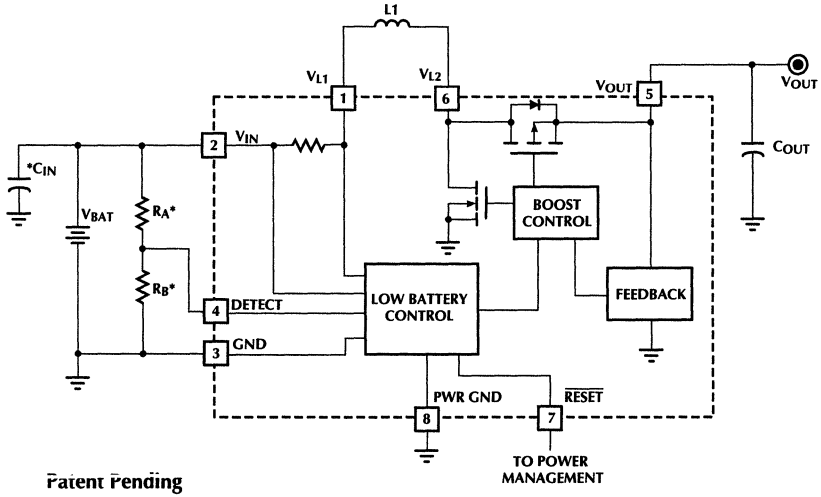
An integrated synchronous rectifier eliminates the need for an external Schottky diode and provides a lower forward voltage drop, resulting in higher conversion efficiency. In addition, low quiescent battery current and variable frequency operation result in high efficiency even at light loads. The ML4871 requires only one inductor and two capacitors to build a very small regulator circuit capable of achieving conversion efficiencies approaching 90%.

The circuit also contains a $\overline{\text{RESET}}$ output which goes low when the DETECT input drops below 1.25V.

FEATURES

- Guaranteed full load start-up and operation at 1.8V input
- Continuous conduction mode for high output current
- Very low supply current (15µA output referenced) for micropower operation
- Pulse Frequency Modulation and Internal Synchronous Rectification for high efficiency
- Maximum switching frequency > 200kHz
- Minimum external components
- Low ON resistance internal switching FETs
- 5V and 3.3V output versions

BLOCK DIAGRAM

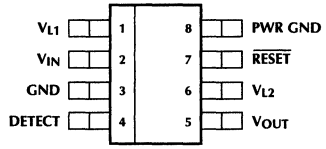


Patent Pending

•Optional

PIN CONFIGURATION

ML4871-5/-3
8-Pin SOIC (S08)



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	V_{L1}	Boost inductor connection
2	V_{IN}	Battery input voltage
3	GND	Analog signal ground
4	DETECT	Pulling this pin below 1.25V causes the $\overline{RESET}$ pin to go low
5	V_{OUT}	Output of the Boost Regulator
6	V_{L2}	Boost inductor connection
7	$\overline{RESET}$	Output goes low when DETECT goes below 1.25V
8	PWR GND	Return for the NMOS output transistor

7

ORDERING INFORMATION

PART NUMBER	OUTPUT VOLTAGE	TEMPERATURE RANGE	PACKAGE
ML4871ES-3	3.3V	–20°C to +70°C	8-Pin SOIC (S08)
ML4871ES-5	5.0V	–20°C to +70°C	8-Pin SOIC (S08)

FEATURING
Extended Commercial Temperature Range
–20°C to 70°C
for Portable Handheld Equipment

December 1994
ADVANCED INFORMATION

ML4872

High Current Boost Regulator with Shutdown

GENERAL DESCRIPTION

The ML4872 is a continuous conduction boost regulator designed for DC to DC conversion in multiple cell battery powered systems. Continuous conduction allows the regulator to maximize output current for a given inductor. The maximum switching frequency can exceed 200kHz, allowing the use of small, low cost inductors. The ML4872 is capable of start-up with input voltages as low as 1.8V and is available in 5V and 3.3V output versions with output voltage accuracy of ±3%.

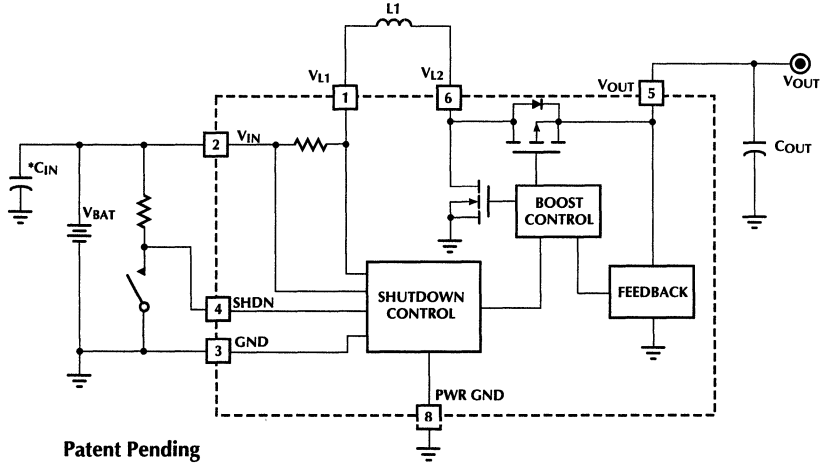
An integrated synchronous rectifier eliminates the need for an external Schottky diode and provides a lower forward voltage drop, resulting in higher conversion efficiency. In addition, low quiescent battery current and variable frequency operation result in high efficiency even at light loads. The ML4872 requires only one inductor and two capacitors to build a very small regulator circuit capable of achieving conversion efficiencies approaching 90%.

The SHDN input allows the user to stop the regulator from switching and powers down the control circuitry.

FEATURES

- Guaranteed full load start-up and operation at 1.8V input
- Continuous conduction mode for high output current
- Very low supply current (15µA output referenced) for micropower operation
- Pulse Frequency Modulation and Internal Synchronous Rectification for high efficiency
- Maximum switching frequency > 200kHz
- Minimum external components
- Low ON resistance internal switching FETs
- 5V and 3.3V output versions

BLOCK DIAGRAM

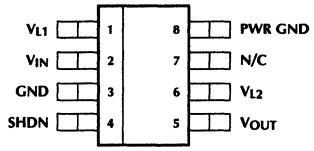


Patent Pending

•Optional

PIN CONFIGURATION

ML4872-5/-3
8-Pin SOIC (S08)



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	V_{L1}	Boost inductor connection
2	V_{IN}	Battery input voltage
3	GND	Analog signal ground
4	SHDN	Pulling this pin to V_{IN} through an external resistor causes the regulator to stop switching, and powers down the control circuitry
5	V_{OUT}	Output of the Boost Regulator
6	V_{L2}	Boost inductor connection
7	N/C	No connection
8	PWR GND	Return for the NMOS output transistor

7

ORDERING INFORMATION

PART NUMBER	OUTPUT VOLTAGE	TEMPERATURE RANGE	PACKAGE
ML4872ES-3	3.3V	–20°C to +70°C	8-Pin SOIC (S08)
ML4872ES-5	5.0V	–20°C to +70°C	8-Pin SOIC (S08)

Micro Linear

ML4873

Battery Power Control IC

GENERAL DESCRIPTION

The ML4873 is a complete solution for DC to DC conversion and power management in multi-cell battery powered portable computers and instruments. Several advanced techniques are incorporated in the IC for the highest possible system efficiency and lowest battery drain.

The 5.0V and 3.3V main regulators in the ML4873 each control Synchronous Rectified buck regulators and drive N-Channel MOSFETs. This allows high conversion efficiencies (90% or greater). The drive for the upper N-Channel MOSFETs in the system is provided via a separate input from a charge pump.

A special "burst mode" for efficient low current operation is provided on one of the regulators for suspend mode.

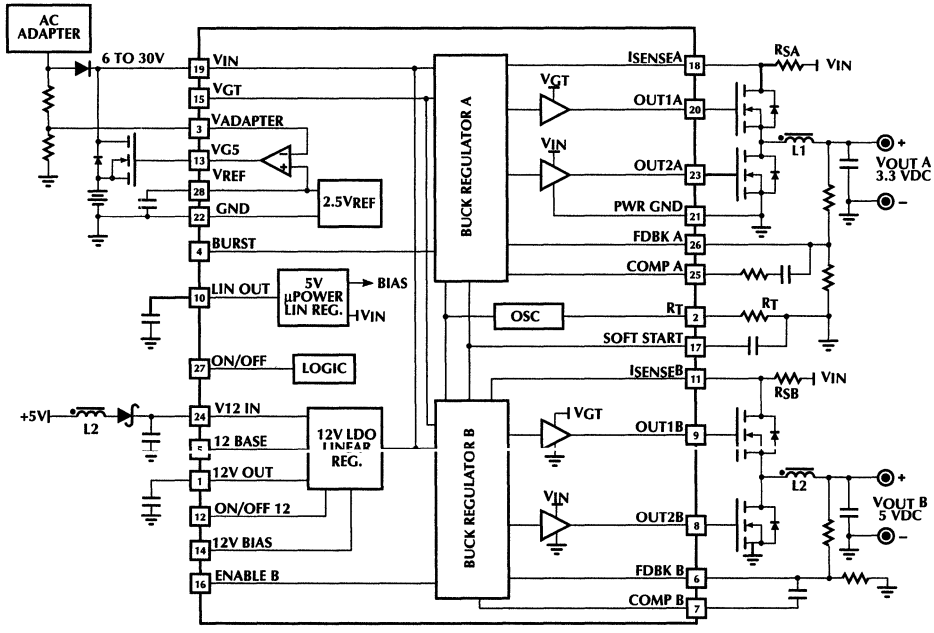
A low drop-out 12V linear regulator for programming EEPROMs or PCMCIA is provided on chip with a separate input, provided by either a winding on the main inductor or from the battery pack.

A µPower 5V linear regulator is provided for the power monitoring logic. The IC can be turned off with only the 5V regulator operating.

FEATURES

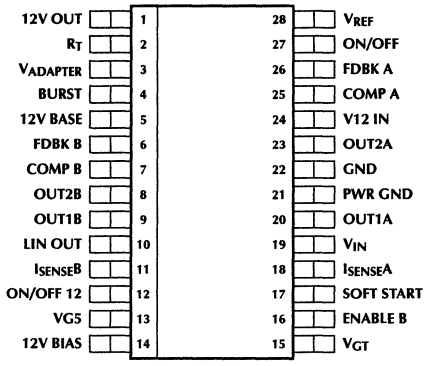
- Two synchronously rectified, 100kHz buck regulators for 5V and 3.3V outputs
- Regulation to ±3% maximum: provides 2% PCMCIA switch matrix margin.
- N-channel MOSFET drive for lowest cost
- Burst mode for efficient operation at light load
- µPower 5V standby linear regulator for power management logic
- 12V low drop out linear regulator with high output (to 300mA) capability
- Automatic charger disconnect switch comparator and N-channel driver
- Wide input voltage range (5.5V to 30V)
- 28-Lead SOIC or SSOP packages

BLOCK DIAGRAM



PIN CONFIGURATION

ML4873
28-PinSOIC (S28W)
or 28-Pin SSOP (R28)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	12V OUT	12V Low Drop-Out regulator output
2	R_T	Timing Resistor which sets oscillator frequency
3	$V_{ADAPTER}$	Input to sense whether adapter is active. VG5 goes high when this pin is above V_{REF}.
4	BURST	A logic 1 sets Buck Regulator A into burst mode (see table 1)
5	12V BASE	Connection to increase 12V regulator output current with external NPN pass transistor
6	FDBK B	Voltage Feedback for buck regulator B
7	COMP B	Buck Regulator B frequency compensation terminal
8	OUT2B	3.3V Buck Regulator Switch Output
9	OUT1B	3.3V Buck Regulator Synchronous Rectifier Output
10	LIN OUT	Output of the µPower 5V regulator. Normally used to power external management circuits and logic
11	$I_{SENSE}B$	Current Sensing for buck regulator B Current limit
12	ON/OFF 12	A logic 1 turns on the 12V regulator
13	VG5	Output to drive N-Channel MOSFET gate to switch battery out when adapter is present
14	12V BIAS	Bias supply for 12V Regulator
15	V_{GT}	N-Channel high side gate drive
16	ENABLE B	A logic 1 enables buck regulator B
17	SOFT START	Soft Start Capacitor
18	$I_{SENSE}A$	Current Sensing for buck regulator A current limit
19	V_{IN}	Input from Battery or AC Adapter
20	OUT1A	3.3V Buck Regulator Switch Output
21	PWR GND	Power Ground
22	GND	Logic and signal Ground
23	OUT2A	3.3V Buck Regulator Synchronous Rectifier Output
24	V12 IN	Power Input for the 12V regulator
25	COMP A	Buck Regulator A frequency compensation terminal
26	FDBK A	Voltage Feedback for buck regulator A
27	ON/OFF	A low on this pin disables all IC functions except the linear 5V regulator and the 2.5V reference, and puts the IC onto a low current consumption mode
28	V_{REF}	Buffered 2.5V reference output

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Voltage on any pin 36V
Output Current Source or Sink (Pins 8, 9, 20, 23) .....
Pulsed 300mA
VG5 Source Current 20mA
VG5 Sink Current 200mA
12V Linear Regulator Output Current 200mA
5V Linear Regulator Output Current 50mA
Inputs (Pins 3, 4, 12, 16, 27) ..... –0.3 to 5.5V
I_{SENSE} Inputs (Pins 11, 18) ..... V_{IN}
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to + 150°C
Lead Temperature (Soldering 10 Sec.) ..... +260°C
Thermal Resistance (θ_{JA}) Plastic SOIC ..... 70°C/W
Thermal Resistance (θ_{JA}) Plastic SSOP ..... 80°C/W

OPERATING CONDITIONS

Temperature Range
Commercial ..... 0°C to +70°C
V_{IN} Voltage Range ..... 5.4V to 30V
V_{GT} Voltage Range ..... V_{IN} –0.5 to 35V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, V_{IN} = 12V, V12 IN = 14V, V_{GT} = 22V, R_T = 200KΩ

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial Accuracy		95	100	105	KHz
Dead Time	50K ≤ R_T ≤ 300K	600	800	1000	ns
Maximum Duty Cycle		90		97	%
Voltage Stability	6V ≤ V_{IN} ≤ 20V		2		%
Error Amplifiers					
Input Offset Voltage			2	10	mV
Input Bias Current			10	200	nA
Output High Voltage	I_{OUT} = –2mA	2.7	2.95		V
Output Low Voltage	I_{OUT} = 20µA			0.5	V
Source Current	V_{OUT} = 2.5V	–5	–7		mA
Sink Current	V_{OUT} = 2.5V		500		µA
Gain Bandwidth Product			675		KHz
High Side (Out 1) Outputs (Pins 9, 20)					
Output High Voltage	I_{OUT} = –20mA	19	21.3		V
Output Low Voltage	I_{OUT} = 20mA		0.2	0.5	V
Low Side (Out 2) Outputs (Pins 8, 23)					
Output High Voltage	I_{OUT} = –20mA	10	13		V
Output Low Voltage	I_{OUT} = 20mA		0.2	0.5	V
Soft Start and Current Limit (Pins 11, 17, 18)					
Voltage Threshold	From V_{IN}	–250	–200	–150	mV
Bias Current	V_{ISENSE} = V_{IN} –200mV		27	75	µA
Soft Start I_{CHARGE}		–10	–13	–20	µA
Soft Start $I_{DISCHARGE}$		3	6.2		mA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Burst Regulator					
Start Threshold			V_{REF} – 25		mV
Stop Threshold			V_{REF} + 25		mV
Reference					
Output Voltage	T_A = 25°C, I_{PIN28} = –100µA	2.45	2.5	2.55	V
Line Regulation	5.4V < V_{IN} < 20V, I_{PIN28} ≤ –mA		0.3	1.2	mV/V
12V Linear Regulator					
Output Voltage	I_O = 60mA	11.5	12	12.5	V
Line Regulation	14V < V12 IN < 24V		0.01		%/V
Drop Out Voltage (V12 IN – 12V OUT)	I_O = 60mA		0.4		V
Load Regulation	10µA < I_O < 60mA		0.8	2.5	%
5V Linear Regulator					
Output Voltage	I_{OUT} = 100µA	4.8	5.0	5.2	V
Input Voltage	V_{OUT} ≥ 4.85V, I_O = 1mA	5.5			V
Line Regulation	5.4V < V_{IN} < 20V, I_O = 1mA		0.75	1.5	%
Load Regulation	10µA < I_O < 10mA		0.25	0.5	%
$V_{ADAPTER}$ Comparator					
Input Bias Current				100	nA
Input Offset Voltage		–30		+30	mV
VG5 Source Current	V_{VG5} = 12V	–5	–10		mA
VG5 Sink Current	V_{VG5} = 12V	85			mA
Logic Inputs (Pins 4, 12, 16, 27)					
Logic Low (V_{IL})	I_{IN} ≥ –5µA			1.1	V
Logic High (V_{IH})	I_{IN} ≥ 5µA	2.5			V
Supply Current					
I_{VIN} + I_{VGT}	Sleep Mode, T_A = 25°C		190	250	µA
I_{VIN} + I_{VGT}	Bust Mode, T_A = 25°C		250		µA
I_{VIN}	Run Mode, T_A = 25°C		7	10	mA
I_{VGT}	Run Mode, T_A = 25°C		2	4	mA

FUNCTIONAL DESCRIPTION

POWER DOWN MODES

The ML4873 operates in either a powered down mode or a run mode according to the state of the ON/OFF pin (Table 1). When the ON/OFF pin is high, the IC is in the run mode and all IC sections are functioning. When the ON/OFF pin is low, the IC is in the standby mode and only the µPower 5V linear regulator and 2.5V reference are on. All gate drive outputs are low. The 5V linear regulator then provides the power to run the system's power management logic. When the BURST pin is high, and the output is above the lower threshold of the burst comparator, the IC is also in standby mode, but with the burst comparator logic also running.

BUCK REGULATORS

The two buck regulators (Figure 3) are synchronously rectifying voltage mode PWM regulators capable of being used over a wide variety of loads and input voltages. The use of synchronous rectification improves system efficiency by reducing the fixed drop associated with the "freewheeling" diode in conventional regulators. These regulators also drive all N-Channel power MOSFETs, significantly improving system efficiency at a low cost. In order to drive the MOSFET gates adequately, a V_{GT} supply must be provided which is higher than the battery voltage by an amount sufficient to provide full enhancement voltage to the MOSFETs. This can be generated as shown in figure 2.

TABLE 1. ML4873 POWER DOWN MODES

Mode	On/Off	Enable B	Burst	Function	Total Supply Current
Sleep	0	X	X	Micro Power 5V Reg Only	130µA
Suspend	1	X	1	Buck Reg A in Burst Mode 5V Reg on	250µA*
Partial Run	1	0	0	Reg. B Disabled, All Other Functions Running	8mA
Run	1	1	0	All Functions Enabled	10mA

*Note This figure represents the total quiescent current for the Bust and 5V regulator. Actual current consumed will vary in proportion to load current.

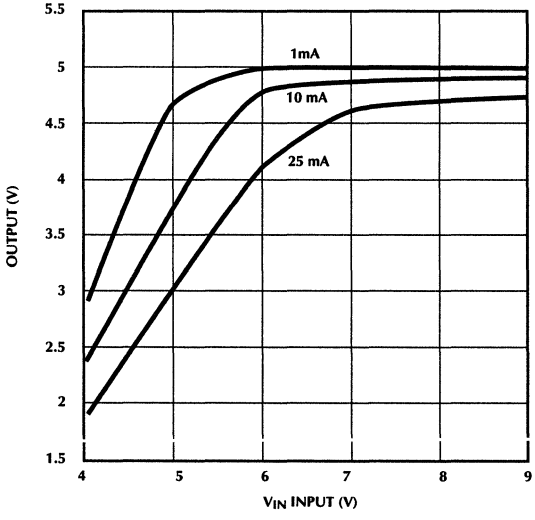


Figure 1. 5V Linear Regulator Output at low V_{IN}

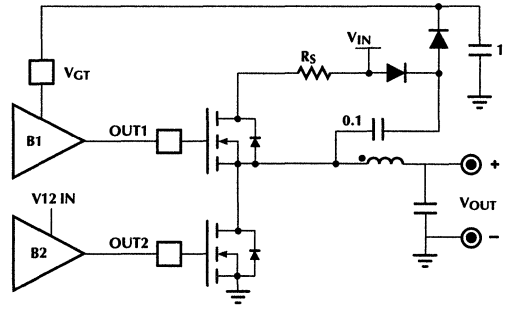


Figure 2. Generating V_{GT} Bias Voltage

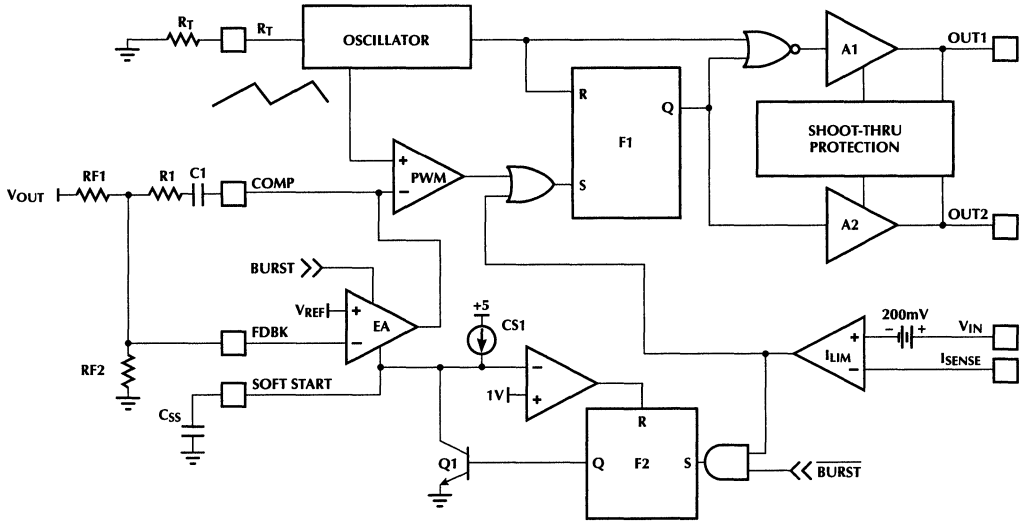


Figure 3. Buck Regulator Block Diagram

Regulator A includes a pin which shuts down the IC and puts Regulator A into "Burst mode". When in "Burst mode" the regulator comes on when the burst comparator is below its lower threshold and goes off again when the output capacitor has charged to the burst comparator's upper threshold. Burst mode is useful for running the regulator at light modes, such as memory keep-alive or "suspend" mode.

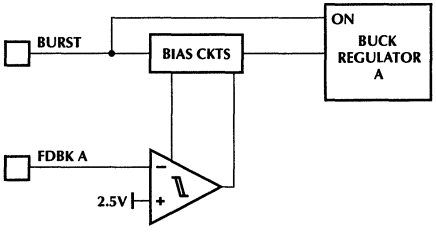


Figure 4. Burst Mode Comparator and Logic

When burst mode is enabled the C_{SS} discharge circuit (Figure 3) is disabled. C_{SS} is floating until CS1 is enabled when a burst occurs. When probing the C_{SS} pin in burst mode, use a high impedance probe to prevent discharge of the C_{SS} pin from disturbing the circuit operation.

Selection of the external MOSFETs, output inductor and capacitor determine the output capabilities of the regulator. Output voltage is set by RF1 and RF2 where.

$$V_{OUT} = \frac{2.5 \times (RF1 + RF2)}{RF2} \qquad (1)$$

The short circuit limit is set by external resistor R_S.

$$I_{SHORT\ CKT} \approx \frac{0.2}{R_S} \qquad (2)$$

C_{SS} is discharged when the regulator is off or when the voltage across R_S exceeds 200mV. F2 ensures that C_{SS} is fully discharged. This circuit provides reliable output short circuit protection with very little power wasted in the sensing element. The error amplifier's output voltage is limited to the voltage on the SOFT START pin. When C_{SS} is discharged, the regulator's duty cycle is 0.

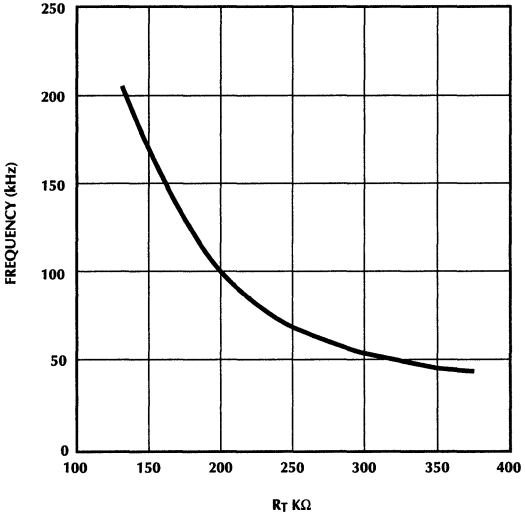


Figure 5. Oscillator Frequency vs. R_T

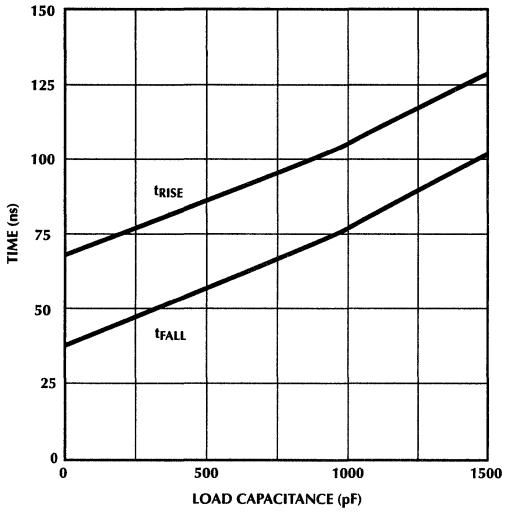


Figure 6. OUT1 Rise and Fall Time vs. Load C_{LOAD}

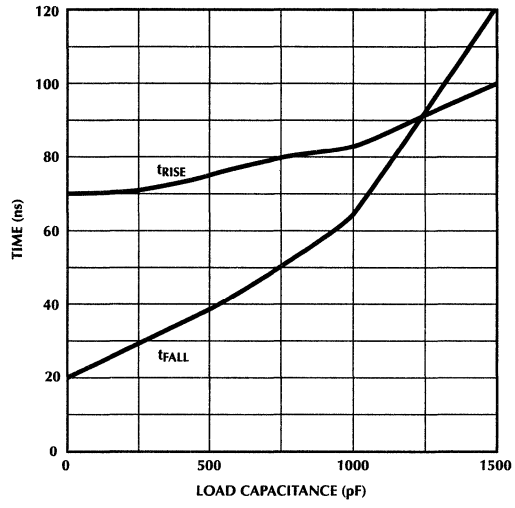


Figure 7. OUT2 Rise and Fall Time vs. Load C_{LOAD}

ADAPTER SWITCH

This function is provided by a comparator whose output (VG5) is pulled to V_{GT} when $V_{ADAPTER}$ goes above 2.5V. By connecting an N-Channel MOSFET gate to VG5, the system can run from the battery without the loss associated with a diode. When the AC adapter is plugged in, the voltage on pin 3 goes high, VG5 swings low, and the system runs from the AC adapter. This circuit functions in all modes of IC operation except SLEEP, when the VG5 output goes low.

12V LINEAR REGULATOR

The 12V regulator includes a shut-off pin. To operate the regulator as a low drop-out regulator, a separate 12VBIAS pin is provided. If this pin is 1.5V higher than V12 IN, the output transistor can be driven to saturation. Input for this regulator may come from either V_{IN} (for high voltage battery packs) or from a coupled inductor winding as shown in Figure 8. If the low drop-out feature is not necessary, V12 BIAS can be tied to V12 IN.

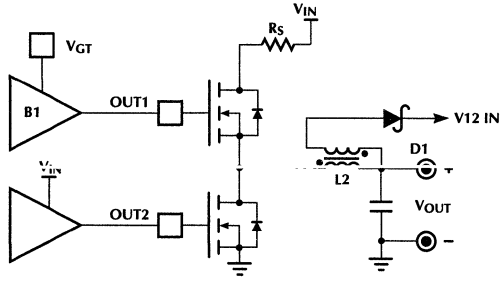


Figure 8. Coupled Inductor to generated V12 IN

APPLICATIONS

BUCK REGULATOR INDUCTOR

Inductors are specified with three main parameters; inductance (L), maximum current ($I_{OUT(MAX)}$), and DC resistance (R_L).

Inductance for a given set of requirements can be calculated using the following:

$$L = \frac{(V_{IN} - V_{OUT}) \times \left(\frac{D}{F}\right)}{(2) \times (I_{OUT(MIN)})} \qquad (3)$$

In this equation, D is the duty cycle, and F is the switching frequency.

Selecting the inductor value using this formula ensures that the inductor stays in the continuous current mode, and never goes discontinuous at light loads ($I_{OUT(MIN)}$). This is important, as high current spikes occur and losses go up when operating in the discontinuous mode.

A good rule of thumb for choosing inductor core size is to make sure that the maximum output current of the regulator doesn't exceed 80% of the maximum current rating of the inductor. Otherwise, core saturation may occur. This is especially important for ferrites, which have a harder saturation characteristic than powdered iron cores.

In order to distribute conduction losses evenly among all components, the DC resistance should be selected to be 1/4 of the sum of the RDS_{ON}s of the power MOSFETs.

Core losses, which contribute significantly to overall efficiency losses, should be minimized by using an inductor designed for minimum losses at the chosen operating frequency. This is a function of the core material, and is lowest in "Kool Mu" and molyperm cores. Of course, efficiency and cost are often inversely related when it comes to magnetic materials.

FREQUENCY SELECTION

Frequency is set by the resistor R_T, which establishes the charge current for the internal capacitor. Since the discharge current is a constant, the dead time of the oscillator is constant, the maximum duty cycle increases as the oscillator frequency decreases. For low input voltage applications, a lower switching frequency may be required to maintain regulation at minimum input voltage.

Losses are heavily comprised of AC losses from the switching characteristic of the power MOSFETs and inductor core losses. Hence, reducing the switching frequency may result in higher efficiencies. As inductor conduction losses will increase at lower frequencies (size goes up, hence there are more copper losses), there will be a point at which this effect cancels the beneficial effect on the AC losses and further reductions no longer increase efficiencies. Also, reductions in operating frequency will result in larger magnetics, and a larger overall supply.

COMPENSATION

Proper compensation is the most critical part of designing a working supply. The compensation network must ensure stability over the full range of input voltage and load conditions, as well as maximize the available bandwidth for good transient response.

If an appreciable ESR exists such that ResrC > LC/5, then we can get away with adding one additional zero to the error amplifier's feedback network, and make use of the other zero created by the combination of the ESR and the output capacitance. We must also add an additional resistance in parallel with the zero we have added, this will give us increased bandwidth and lower the DC gain. Its size is determined by the gain necessary to bring the system to 0dB at the desired crossover point. As a rule of thumb, this point should be no more than 1/5 the switching frequency.

In cases where the ESR of the output capacitors is minimal, we no longer have a zero for free.

Now, we must use a zero on the input of the error amplifier in addition to the zero in the feedback network. The parallel feedback resistor is also still required; the gain is now the parallel combination of the feedback zero resistor and this resistor.

The internal error amplifier has an open loop gain of 90 dB, and a single pole at 31Hz. These must be taken into account in order to adequately compensate the supply.

TYPICAL PERFORMANCE CHARACTERISTICS

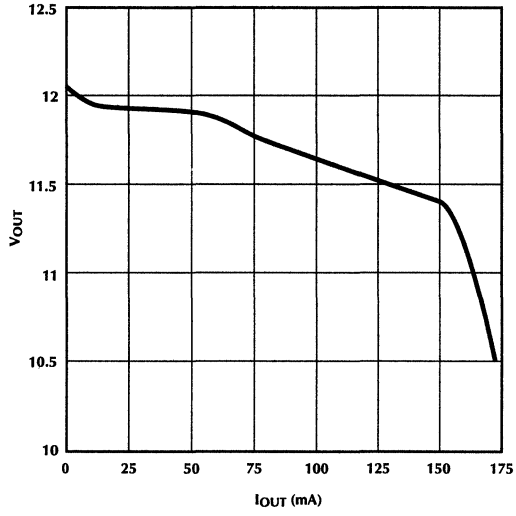


Figure 9. 12V Regulator Load Regulation

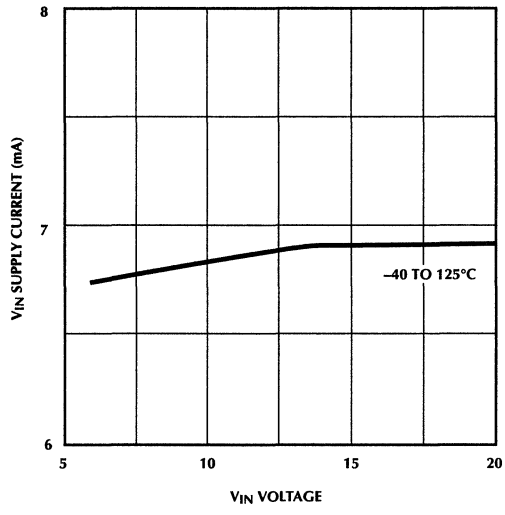


Figure 10. Supply Current (V_{IN}) vs. V_{IN} Voltage

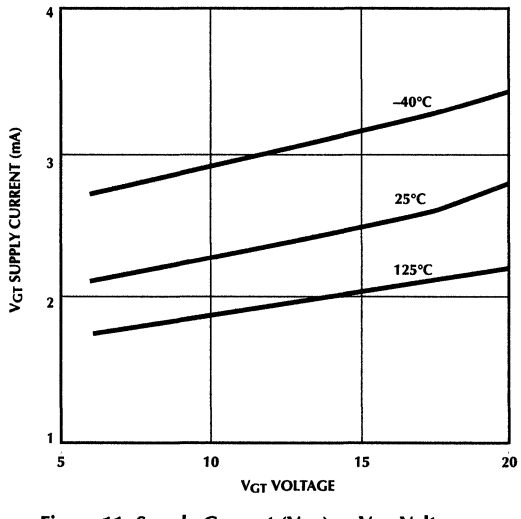


Figure 11. Supply Current (V_{GT}) vs V_{GT} Voltage

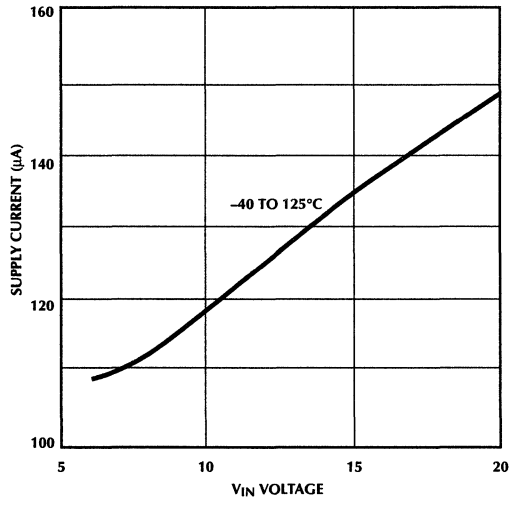


Figure 12. SLEEP Mode Current (V_{IN}) vs. V_{IN} Voltage

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4873CS	0°C to +70°C	28-PIN SOIC (S28W)
ML4873CR	0°C to +70°C	28-PIN SSOP (R28)

ML4873EVAL

Battery Management IC Evaluation Kit

GENERAL DESCRIPTION

The ML4873 evaluation board provides a convenient tool for demonstrating the performance and efficiency of this battery management IC.

This board is designed to demonstrate the ML4873 in a 12 W buck DC to DC converter circuit. If other power levels and /or operating conditions are desired, modifications can easily be made to accommodate them.

Operating from a wide input range, 5.5V to 18V; this board is designed to provide a 3.3V and a 5V output that can deliver up to 1.5A, a 12 V linear regulator output that can provide 25 mA, and a 5 V linear output that can provide 25 mA. The chosen switching frequency is 100kHz. Efficiency can be as high as 94% with an input voltage of 6 V. Output ripple voltage was designed to be 50 mV pk - pk max., and line and load regulation are designed to be no more than ±5%.

The full schematic of this board is shown in Figure 1. An additional winding was added to the 3.3V inductor to provide the necessary for the 12 V linear regulator. As logic level FETs are used, an additional winding is added to the 3.3V inductor to provide the necessary additional 5 V of enhancement.

As the output capacitors are three paralleled surface mount tantalums, the ESR is very low (measured to be about 0.05 ohm). A double zero compensation scheme is used in order to provide the necessary 45 degrees of phase margin.

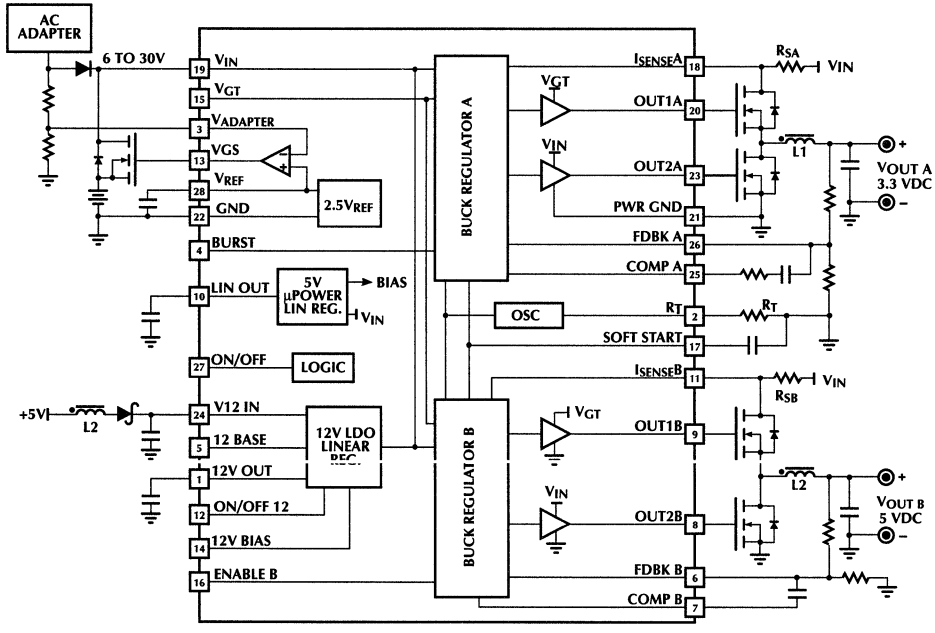
FEATURES

- High efficiency synchronous rectification
- Surface mount construction for minimum size/parasitics
- Enable and burst mode selectable via dip switches
- 3.3V, 5W output and 5V, 7.5W output

KIT COMPONENTS

- ML4873EVAL board with one ML4873
- ML4873 Data Sheet
- Applications Note 37

BLOCK DIAGRAM



HOW TO OPERATE

1) Set all DIP switches to logic low.
2) Connect a small, separate 5V supply to the supply pin for the DIP switches.
3) Connect a power supply capable of delivering 2A to Vin. Set it for 12 V just for initialization of the system.
4) With both supplies turned on and all DIP switches in the off position, check to see if V_{REF} (Pin 25) and linear 5V outputs are functional.
5) If all is well with V_{REF} and the linear regulator, turn the "On/Off" DIP switch to the on position and verify that
6) Turn on the DIP switch to verify that regulator B is working, once again, with an adequate load. Next, check the 12V linear regulator as well.

Micro Linear

FEATURING
Extended Commercial Temperature Range
–20°C to 70°C
for Portable Handheld Equipment

September 1994
PRELIMINARY

ML4874

LCD Backlight Lamp Driver

GENERAL DESCRIPTION

The ML4874 is an ideal solution for driving small cold cathode fluorescent tubes (CCFL) used in liquid crystal display (LCD) backlight applications. It provides the dimming ballast control for the LCD display.

By utilizing differential drive the ML4874 can deliver the same light output with significantly less input power compared to existing single ended drive schemes. Improvements as high as 30% can be realized when using low power lamps and advanced LCD screen housings. This increased light output is achieved because the differential drive configuration is much less sensitive, and therefore less power is wasted in the capacitive parasitics that exist in the backlight housing. An additional benefit of this configuration is an even distribution of light.

The ML4874 is optimized for portable applications where high efficiency is critical to maximize battery life. The high efficiency is achieved by a resonant scheme with zero voltage switching. The complete system, including the magnetics, can be easily realized with standard off the shelf power components.

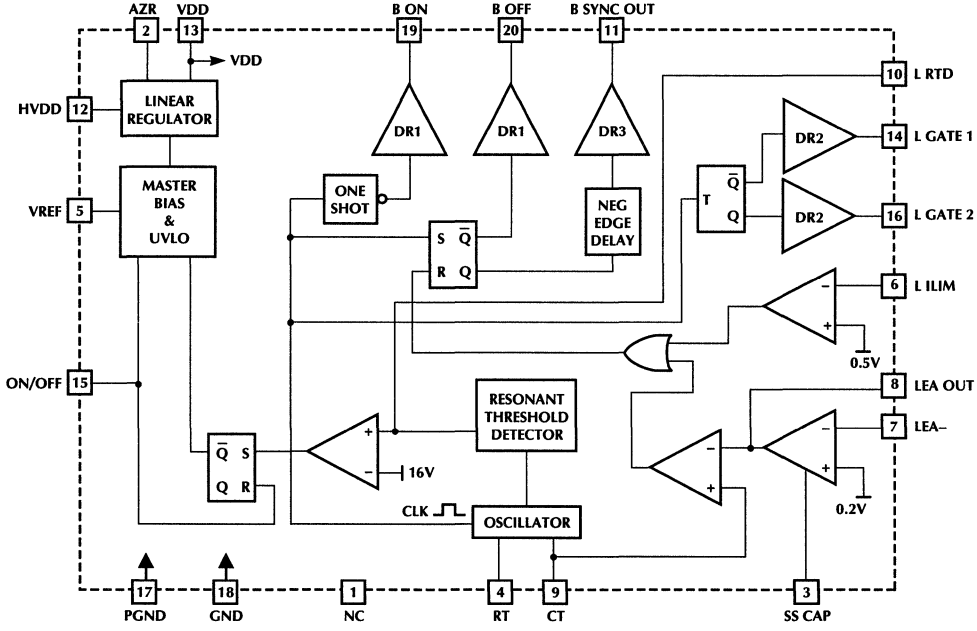
All of the regulators on the chip are synchronized to the inverter frequency to eliminate the ghosting and flicker common to asynchronous circuits.

The ML4874 is available in very small form factor package (20 pin SSOP) making it ideal for hand held portable applications.

FEATURES

- Backlight Lamp Driver with Differential Drive
- Up to 30% Lower Power for Same Light Output
- Low Standby Current (< 10µA)
- Improved Efficiency (≈95%)
- Allows All N-Channel MOSFET Drive
- Low Switching Losses
- Resonant Threshold Detection
- Buck Regulator uses Synchronous Rectification

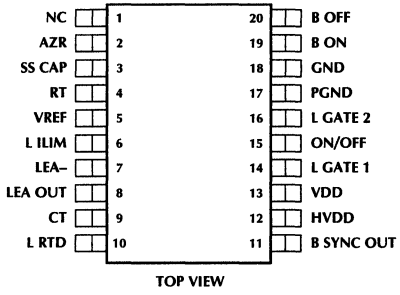
BLOCK DIAGRAM



NOTE: FOR 16 PIN VERSION L ILM AND LEA– ARE COMMON, PGND AND GND ARE COMMON, AZR IS NOT AVAILABLE.

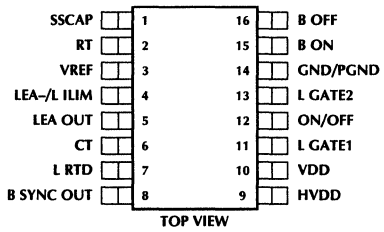
PIN CONFIGURATION

ML4874
20-Pin SSOP (R20)



TOP VIEW

ML4874
16-Pin SOIC (S16)



TOP VIEW

PIN DESCRIPTION

PIN# *		NAME	DESCRIPTION
1	N/A	NC	This pin should be left open.
2	N/A	AZR	Connection to gate of external FET for high voltage regulator. Internally a zener diode to ground.
3	1	SS CAP	Connection of optional external soft start capacitor.
4	2	RT	Oscillator timing resistor.
5	3	VREF	Voltage reference output.
6	4	L ILIM	Input to current limit amplifier.
7	4	LEA–	Negative input for lamp error amplifier.
8	5	LEA OUT	Output of lamp error amplifier. External compensation capacitor connects between this pin and LEA.
9	6	CT	Oscillator timing capacitor.
10	7	L RTD	Input to resonant threshold detector.
11	8	B SYNC OUT	Output of MOSFET driver to gate of synchronous FET catch diode.
12	9	HVDD	Battery power input to linear regulator.
13	10	VDD	Output of linear regulator. Positive power for IC.
14	11	L GATE1	Output of MOSFET driver. Connection to gate of one side of inverter FET drive pair.
15	12	ON/OFF	Logic input for chip
16	13	L GATE2	Output of MOSFET driver. Connection to gate of one side of inverter FET drive pair.
17	14	PGND	Power ground
18	14	GND	Signal ground.
19	15	B ON	Connection to primary side of gate pulse transformer.
20	16	B OFF	Output of MOSFET driver. Connection to gate of FET that disables the input power.

* For 16-Pin SOIC version.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 75mA
Output Current, Source or Sink 250mA
Voltage on Pins* 1-9, 11, 13-20 ..... –0.3V to VDD +0.3V
Voltage on Pin 12 ..... 20V
Current into Pin* 10 ..... ±10mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA}) Plastic SSOP ..... 100°C/W

*Note: Pin designation for 20-pin SSOP. For 16-pin SOIC please refer to pin configuration on previous page.

OPERATING CONDITIONS

Temperature Range
ML4874C ..... 0°C to +70°C
ML4874E ..... –20°C to +70°C

ELECTRICAL CHARACTERISTICS

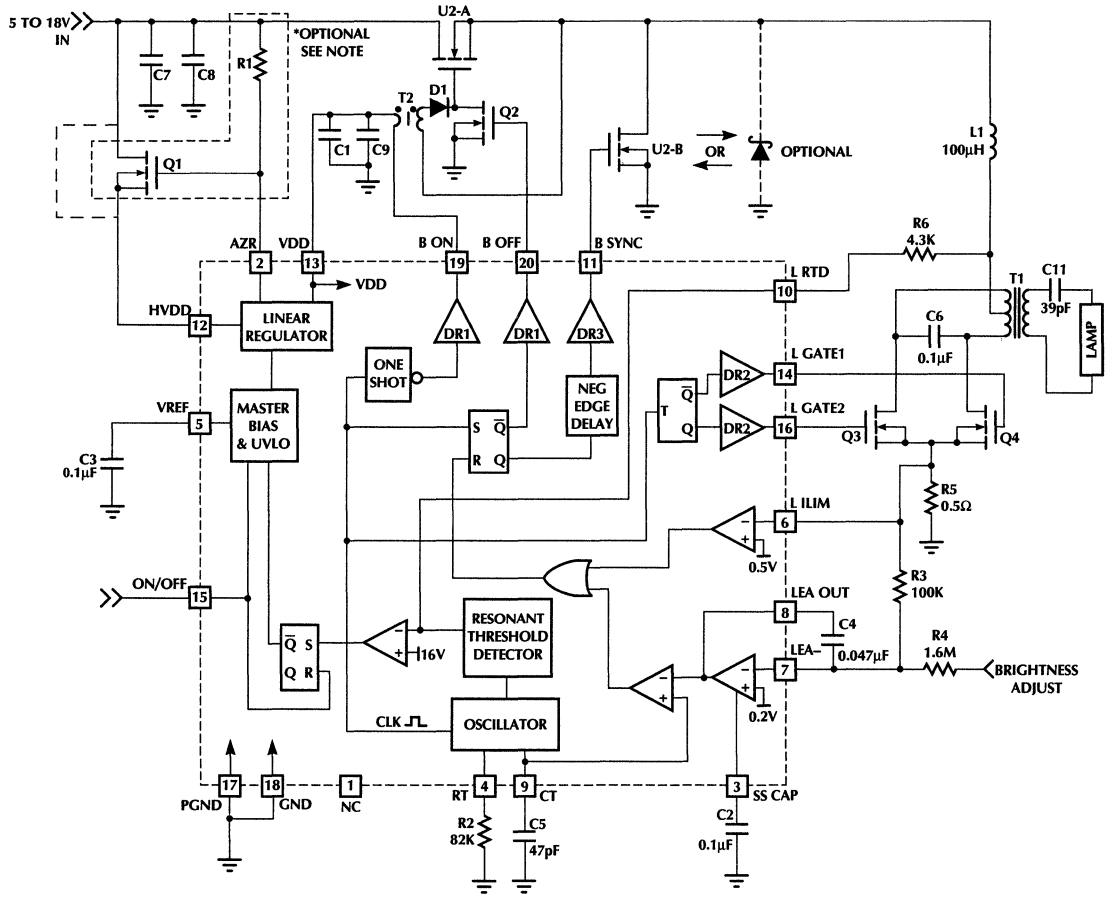
Unless otherwise specified, VDD = 5V ±5%, T_A= –20°C to 70°C, CT = 47pF (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT REGULATOR SECTION					
Error Amplifier					
Open Loop Gain		60	70		dB
Bias Point	Closed loop	0.18	0.2	0.22	V
Output High	I_{LOAD} = 5µA	2.8	3.0		V
Output Low	I_{LOAD} = 25µA		0.4	0.7	V
Bandwidth (–3dB)			1		MHz
Input Voltage Range		–0.3	0.2	VREF	V
Input Bias Current			50	100	nA
Soft Start Charge Current	V_{SSCAP} = 1V	300	500	700	nA
Soft Start Threshold (LEA OUT)	V_{SSCAP} = 1V	2		2.5	V
Current Limit Comparator					
Current Threshold		450	500	550	mV
Input Bias Current	V_{LILM} = 0.1V		50	100	nA
Propagation Delay	(Note 2)		150	250	ns
Output Drivers					
Output High - B SYNC OUT, B OFF	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
Output Low - B SYNC OUT, B OFF	I_{LOAD} = 12mA		0.2	0.375	V
Rise & Fall time - B SYNC OUT, B OFF	C_{LOAD} = 100pF		20	50	ns
Output High - B ON	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
Output Low - B ON	I_{LOAD} = 50mA		0.2	0.375	V
Fall Time - B ON	C_{LOAD} = 2400pF (Note 2)		45	80	ns
ONE SHOT Pulse Width		100	150	200	ns
DELAY TIMER Delay Time		20	35	55	ns

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH VOLTAGE INVERTER SECTION					
Oscillator					
Nominal Frequency		68	80	92	kHz
Discharge Current	V_{CT} = 2V	500	700	900	µA
Peak Voltage		2.3	2.5	2.7	V
Valley Voltage		0.8	1	1.2	V
Output Drivers					
Output High - L GATE 1, 2	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
Output Low - L GATE 1, 2	I_{LOAD} = 50mA		0.2	0.375	V
Rise & Fall Time - L GATE 1, 2	C_{LOAD} = 1000pF		20	50	ns
Resonant threshold Detector					
Threshold		0.75	1.1	1.45	V
Hysteresis		250	500	750	mV
Lamp Out Detect					
Threshold		16	18	20	V
Under Voltage Detector					
Start Up Threshold		3.8	4.1	4.4	V
Hysteresis		150	300	450	mV
Logic Interface (On/Off)					
VIH		2.5			V
VIL				0.5	V
Input Bias Current	On/Off = 3V		10	25	µA
Linear Regulator Section					
Aux Zener Reference Voltage (AZR)	I_{AZR} = 10µA	7.4	7.9	8.4	V
Regulator Voltage (VDD)	HVDD = 12V	4.75	5.0	5.35	V
Regulator Source Current	External to device		10		mA
Drop Out Voltage	I_{HVDD} = 1mA		30	90	mA
Drop Out Voltage	I_{HVDD} = 5mA		125	275	mA
HVDD Input Voltage Range		5		18	V
Bias Section					
VDD Supply Current	On/Off = "1", no load		375	450	µA
VDD Supply Current	On/Off = "0", HVDD = 12V		1	10	µA
VREF Load Regulation	I_{LOAD} = 25µA		10	20	mV
VREF Output Voltage	T_A = 25°C	2.47	2.5	2.53	V
VREF Line Regulation			20	30	mV
VREF Line, Load, Temp		2.465	2.5	2.535	V

Note 1: Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.
Note 2: Actual load is 1200pF. The 2:1 transformer reflects an effective 2400pF.



*NOTE: USED FOR INPUT VOLTAGES GREATER THAN 18 VOLTS

Figure 1. Typical Application Schematic for the ML4874

FUNCTIONAL DESCRIPTION

The ML4874 consists of a PWM regulator, a lamp driver/ inverter, a linear regulator and control circuits. This IC, in conjunction with external components, converts a DC battery voltage into the high voltage and high frequency AC signal required to start and drive miniature cold cathode fluorescent lamps. A typical application circuit is shown in figure 1. Please refer to Application Note 32 for detailed application information beyond what is presented here.

Note: Please read the Power Sequencing section below prior to using the ML4874.

LAMP DRIVER

The lamp driver, sometimes referred to as a lamp inverter, is comprised of a PWM regulator and a Royer type inverter circuit to drive the lamp. The PWM regulator, in a buck configuration, controls the magnitude of the lamp current to provide the dimming capability. Figure 2 shows a simplified circuit to more easily illustrate the operation of the circuit.

Due to the presence of the buck inductor, L1, the circuit shown in figure 2 is essentially a current fed parallel loaded resonant circuit. Lm is the primary inductance of the output transformer, T1, which tunes with the resonant capacitor C_R to set the resonant frequency of the inverter. The oscillator frequency is always set lower than the natural resonant frequency to ensure synchronization. The current source IC models the current through the buck inductor L1.

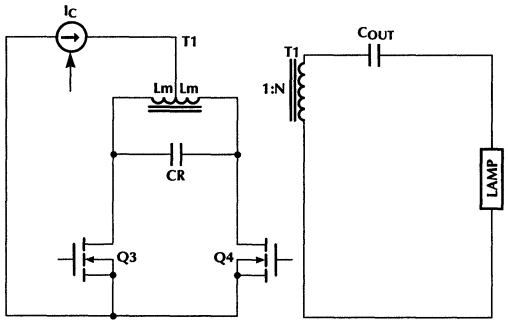


Figure 2. Simplified Lamp Driver Circuit

The MOSFETs, Q3 and Q4 are alternately turned on with a constant 50% duty cycle signal (L GATE1, L GATE2) at one-half the frequency of the oscillator. In this way each transistor pulses, or excites, the resonant tank on each half cycle. The combination of these two signals appear across the primary winding of the output transformer as a sinusoidal waveform. This voltage is multiplied by the step-up turns ratio of the output transformer and impressed across the lamp.

The output transitions are controlled by feedback through the L RTD pin by sensing the voltage at the center tap of the output transformer. Each time this signal reaches the minimum resonant threshold detection point an internal clock pulse is generated to keep the system synchronized. Figure 3 shows some of these representative waveforms at the important nodes of the circuit.

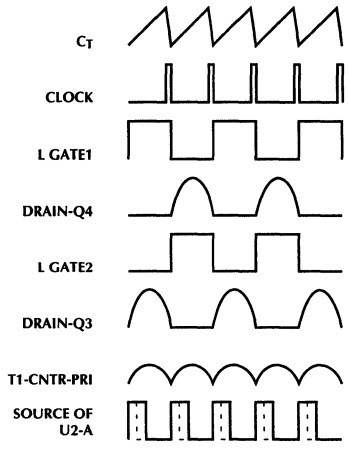


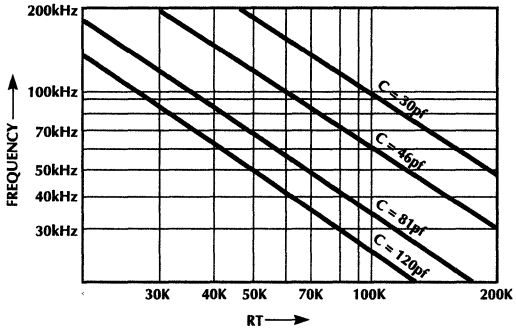
Figure 3. Operating Waveforms of the Lamp Driver Section

The PWM regulator is comprised of a MOSFET (U2-A), inductor L1, and the gate control and drive circuitry as shown in figure 1. A signal with a constant pulse width of 150nS is applied to the primary of the 2:1 pulse transformer T2, rectified by diode D1, and used to charge the gate capacitance of U2-A, thereby turning it on. The turn off is controlled by discharging this capacitance through MOSFET Q2. The pulse width of the signal on the gate of Q2 (B OFF) varies according to the amplitude of the feedback signal on LEA–, which is proportional to the ac current flowing in the lamp. This feedback signal is developed by monitoring the current through resistor R5 in the common source connection of the inverter MOSFETs, Q3 and Q4. The lamp current, and therefore brightness, is adjusted by varying the voltage applied to R4, at the brightness adjust control point. Increasing this voltage decreases the brightness.

OSCILLATOR

The frequency of the oscillator in the ML4874 is set by selecting the values of C_T and R_T.

The following graph shows the oscillator frequency versus the value of RT for different values of CT. This nomograph may be used to select the appropriate value of Rt and CT to achieve the desired oscillator frequency for the ML4874.



LINEAR REGULATOR

A linear voltage regulator is provided to power the low voltage and low current control circuitry on the ML4874. This is typically used when there is no separate 5 volt supply available at the inverter board. For operatiozxn up to 18 volts the linear regulator is used by connecting the HVDD pin to the input battery voltage. For operation over 18 volts, a MOSFET, and a resistor (Q1 and R1, in figure 1) are connected as shown. The MOSFET is required to stand off the high voltage. The AZR pin is just a zener diode to ground used to bias the gate of Q1.

LAMP OUT DETECT

In those cases when there is no lamp connected, or the connection is faulty, the output voltage of the lamp driver circuit will tend to rise to a high level in an attempt to start the nonexistent lamp. The lamp out detect circuit on the ML4874 will detect this condition by sensing the center tap voltage on the primary of the output transformer, T1 on the L RTD pin. When this voltage exceeds 16 volts, an internal latch is set and the lamp driver goes into a shutdown mode. The logic control pin ON/OFF must be cycled low, then high to reset the latch and return the lamp driver to the normal state.

SOFT START

The capability to control the start up behavior is achieved by setting the value of a single capacitor, C2 in figure 1. By selecting the appropriate value the ac lamp current can be set to slowly increase with a controlled time constant. The capacitor value can be calculated according to the following formula.

$$C = (5 \times 10^{-7})T_S$$

Where T_S = Duration of the soft start sequence in seconds

LOGIC CONTROL

The ML4874 is controlled by a single logic input, ON/OFF. A logic level high on this pin enables the lamp driver. A logic zero puts the circuit into a very low power state.

POWER SEQUENCING

It is important to observe correct power and logic input sequencing when powering up the ML4874. The following procedure must be observed to avoid damaging the device.

1. Apply the battery power to HVDD.
2. Apply the VDD voltage (if HVDD is not used). With HVDD connected this voltage is supplied by the internal regulator on the ML4874.
3. Apply a logic high to the ON/OFF input.

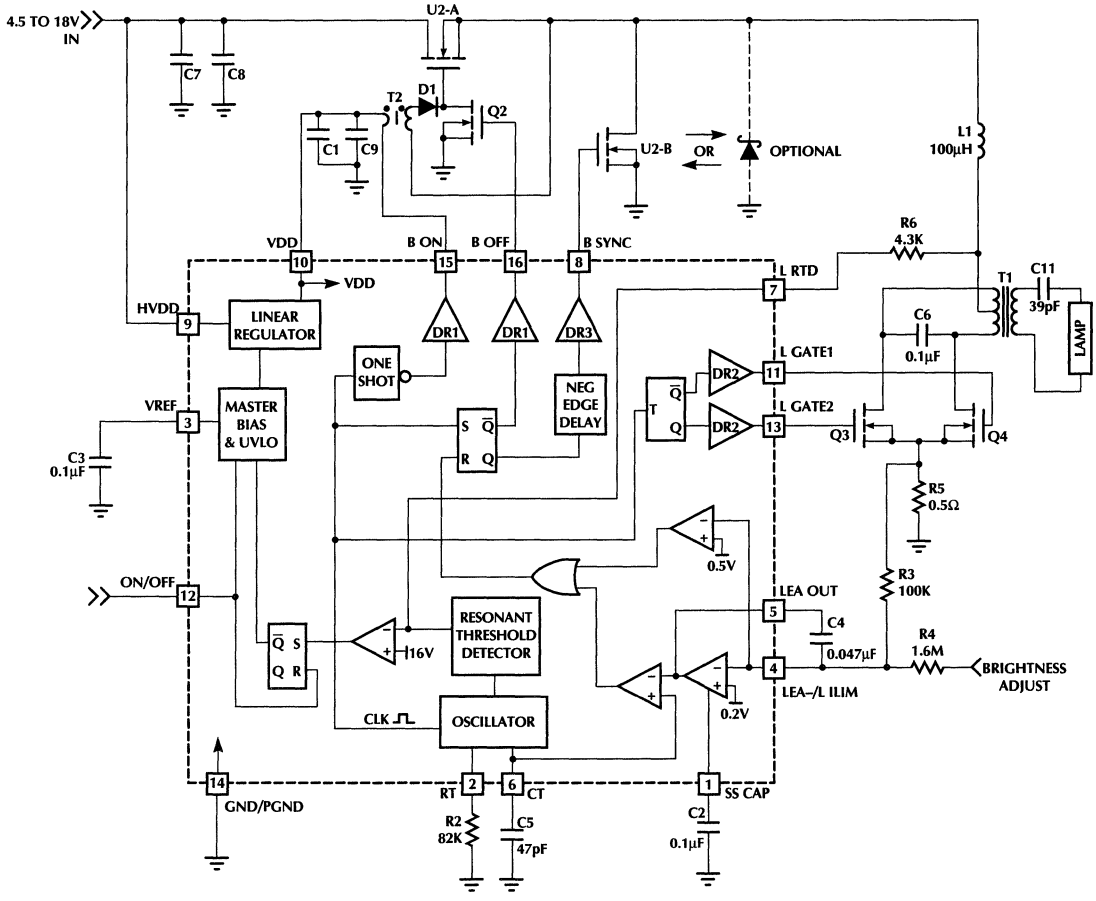


Figure 4. Typical Application Schematic for the 16 pin SOIC ML4874.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4874CS	0°C to +70°C	Molded SOIC (S16)
ML4874ER	–20°C to +70°C	Molded SSOP (R20)

ML4874EVAL

Differential Drive LCD Backlight Evaluation Kit

GENERAL DESCRIPTION

The ML4874 is a cold cathode fluorescent lamp (CCFL) backlight controller featuring differential lamp drive and dimming control. It is commonly used to power the backlight of the LCD display found in many handheld instruments. This evaluation board enables the designer to explore the capabilities of the circuit and determine its suitability for a current or new design. A miniature lamp is included in the evaluation package to speed design turn around times.

The ML4874 evaluation board is a miniaturized design for space efficiency, and can be readily interfaced with most systems. The assembled board measures 0.65" W x 3.175" L x 0.235" H.

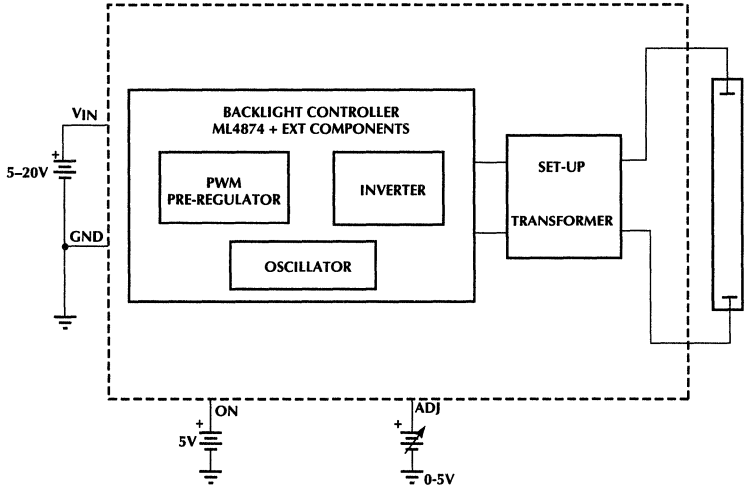
FEATURES

- Operates Over a 5 to 20V Supply Range
- Efficiency Greater than 90%
- Differential Lamp Drive Improves Dimming Range
- Capable of Driving Lamp to Greater than 5W
- Low Profile, High Density PC Board Layout

KIT COMPONENTS

- ML4874 User's guide
- ML4874 Data Sheet
- A fully functional evaluation board
- Application Notes 26 and 32
- Miniature Fluorescent Lamp
- PCB Layout Gerber File

BLOCK DIAGRAM



Low Voltage Boost Regulator with Shutdown

GENERAL DESCRIPTION

The ML4875 is a boost regulator designed for DC to DC conversion in 1 to 3 cell battery powered systems. The combination of BiCMOS process technology, internal synchronous rectification, variable frequency operation, and low supply current make the ML4875 ideal for 1 cell applications. The ML4875 is capable of start-up with input voltages as low as 1V and is available in 5V, 3.3V, and 3V output versions with an output voltage accuracy of ±3%.

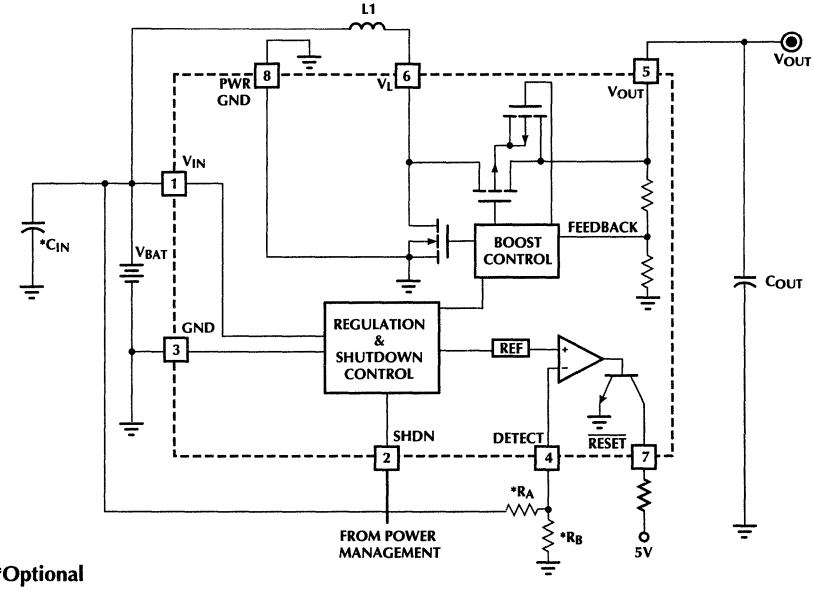
Unlike regulators using external Schottky diodes, the ML4875 isolates the load from the battery when the SHDN pin is high. This is accomplished by an integrated synchronous rectifier which eliminates the need for an external Schottky diode and provides a lower forward voltage drop, resulting in higher conversion efficiency. In addition, low quiescent battery current and variable frequency operation result in high efficiency even at light loads. The ML4875 requires only one inductor and two capacitors to build a very small regulator circuit capable of achieving conversion efficiencies in excess of 90%.

The circuit contains a $\overline{\text{RESET}}$ output which goes low when the DETECT input drops below 200mV.

FEATURES

- Guaranteed start-up and operation at 1V input
- Pulse Frequency Modulation and Internal Synchronous Rectification for high efficiency
- Isolates the load from the input during shutdown
- Minimum external components
- Low ON resistance internal switching FETs
- Micropower operation
- 5V, 3.3V, and 3V output versions

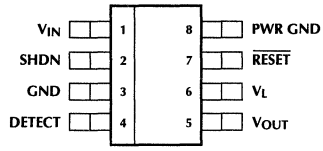
BLOCK DIAGRAM



*Optional

PIN CONNECTION

ML4875-5/-3/-T
8-Pin SOIC (S08)



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	V_{IN}	Battery input voltage
2	SHDN	Pulling this pin high shuts down the regulator, isolating the load from the input
3	GND	Analog signal ground
4	DETECT	When this pin below V_{REF}, causes the $\overline{RESET}$ pin to go low
5	V_{OUT}	Boost regulator output
6	V_L	Boost inductor connection
7	$\overline{RESET}$	Output goes low when regulation cannot be achieved or when DETECT goes below 200mV
8	PWR GND	Return for the NMOS output transistor

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Voltage on any pin 7V
Peak Switch Current, $I_{(PEAK)}$ 1.5A
Average Switch Current, $I_{(AVG)}$ 300mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C

Thermal Resistance (θ_{JA})
Plastic SOIC ..... 110°C/W

OPERATING CONDITIONS

Temperature Range
ML4875CS-X ..... 0°C to +70°C
ML4875ES-X ..... –20°C to +70°C
V_{IN} Operating Range
ML4875CS-X ..... 1.0V to V_{OUT} –0.2V
ML4875ES-X ..... 1.1V to V_{OUT} –0.2V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = Operating Voltage Range, T_A = Operating Temperature Range.

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Supply					
V_{IN} Current	$V_{IN} = V_{OUT} - 0.2V$		50	65	µA
	V_{IN} = 4.8V, SHDN = high		20	30	µA
V_{OUT} Quiescent Current			8	12	µA
V_L Quiescent Current				1	µA
PFM Regulator					
Pulse Width (T_{ON})		9	10	11	µs
Output Voltage (V_{OUT})					
ML4875-5	T_{ON} = 0 at V_{OUT}(MAX),	4.85	5.0	5.15	V
ML4875-3	9µs ≤ T_{ON} ≤ 11µs V_{OUT}(MIN)	3.2	3.3	3.4	V
ML4875-T		2.91	3.0	3.09	V
Load Regulation	See Figure 1				
ML4875-5	V_{IN} = 1.2V, I_{OUT} ≤ 20mA	4.85	5.0	5.15	V
	V_{IN} = 2.4V, I_{OUT} ≤ 105mA	4.85	5.0	5.15	V
ML4875-3	V_{IN} = 1.2V, I_{OUT} ≤ 30mA	3.2	3.3	3.4	V
	V_{IN} = 2.4V, I_{OUT} ≤ 140mA	3.2	3.3	3.4	V
ML4875-T	V_{IN} = 1.2V, I_{OUT} ≤ 35mA	2.91	3.0	3.09	V
	V_{IN} = 2.4V, I_{OUT} ≤ 160mA	2.91	3.0	3.09	V
Under-Voltage Lockout Threshold			0.85	0.95	V
Shutdown					
Input Bias Current		–100		100	nA
Shutdown Threshold	V_{SHDN} = high to low	180	200	220	mV
Shutdown Hysteresis			50	70	mV
$\overline{\text{RESET}}$ Comparator					
DETECT Threshold		190	200	210	mV
DETECT Bias Current		–100		100	nA
$\overline{\text{RESET}}$ ON Voltage	$I_{\overline{\text{RESET}}}$ = 50µA		0.1	0.2	V
$\overline{\text{RESET}}$ OFF Current	$V_{\overline{\text{RESET}}}$ = 5V			100	nA

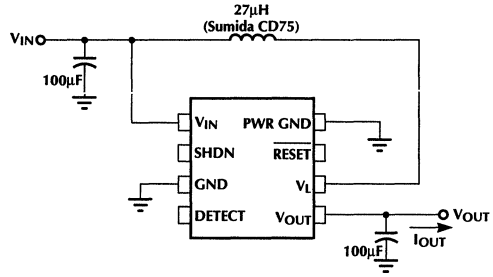


Figure 1. Application Test Circuit

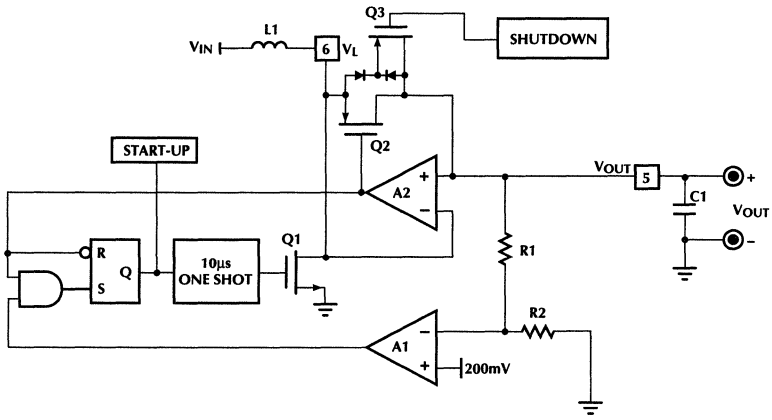


Figure 2. PFM Regulator Block Diagram

FUNCTIONAL DESCRIPTION

The ML4875 combines Pulse Frequency Modulation (PFM) and synchronous rectification to create a boost converter that is both highly efficient and simple to use. A PFM regulator charges a single inductor for a fixed period of time and then completely discharges before another cycle begins, simplifying the design by eliminating the need for conventional current limiting circuitry. Synchronous rectification is accomplished by replacing an external Schottky diode with an on-chip PMOS device, reducing switching losses and external component count.

REGULATOR OPERATION

A block diagram of the boost converter is shown in Figure 2. The circuit remains idle when V_{OUT} is at or above the desired output voltage, drawing 50µA from V_{IN}, and 8µA from V_{OUT} through the feedback resistors R1 and R2. When V_{OUT} drops below the desired output level, the output of amplifier A1 goes high, signaling the regulator to deliver charge to the output. Since the output of amplifier A2 is normally high, the flip-flop captures the A1 set signal and creates a pulse at the gate of the NMOS transistor Q1. The NMOS transistor will charge the inductor L1 for 10µs, resulting in a peak current given by:

$$I_{L(PEAK)} = \frac{T_{ON} \times V_{IN}}{L_1} \approx \frac{10\mu s \times V_{IN}}{L_1} \qquad (1)$$

For reliable operation, L1 should be chosen so that $I_{L(PEAK)}$ does not exceed 1.5A.

When the one-shot times out, the NMOS transistor releases the V_L pin, allowing the inductor to fly-back and momentarily charge the output through the body diode of PMOS transistor Q2 in series with shutdown transistor Q3. But, as the voltage across the PMOS transistor changes polarity, its gate will be driven low by the current sense amplifier A2, causing Q2 to short out its body diode. The inductor then discharges into the load through Q2. The output of A2 also serves to reset the flip-flop and one-shot in preparation for the next charging cycle. A2 releases the gate of Q2 when its current falls to zero. If V_{OUT} is still low, the flip-flop will immediately initiate another pulse. The output capacitor (C1) filters the inductor current, limiting output voltage ripple. Inductor current and one-shot waveforms are shown in Figure 3.

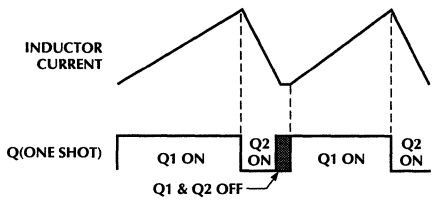


Figure 3. PFM Inductor Current Waveforms and Timing.

SHUTDOWN

The ML4875 output can be shut down by pulling the SHDN pin high. When SHDN is high, the regulator stops switching, the control circuitry is powered down, and the body diode of the PMOS synchronous rectifier is disconnected from the output, allowing the output voltage to drop below the input voltage. This feature is unique to the ML4875, as most boost regulators use external Schottky diode rectifier which cannot be disconnected during shutdown. Leaving the Schottky diode connected causes excess power dissipation in the load during shutdown because the Schottky conducts whenever the output voltage drops 300mV below the input voltage.

$\overline{\text{RESET}}$ COMPARATOR

An additional comparator is provided to detect low V_{IN}, or any other error condition that is important to the user. The inverting input of the comparator is internally connected to V_{REF}, while the non-inverting input is provided externally at the DETECT pin. The output of the comparator is the $\overline{\text{RESET}}$ pin, which swings from V_{OUT} to GND when an error is detected.

DESIGN CONSIDERATIONS

INDUCTOR

Selecting the proper inductor for a specific application usually involves a trade-off between efficiency and maximum output current. Choosing too high a value will keep the regulator from delivering the required output current under worst case conditions. Choosing too low a value causes efficiency to suffer. It is necessary to know the maximum required output current and the input voltage range to select the proper inductor value. The maximum inductor value can be estimated using the following formula:

$$L_{MAX} = \frac{V_{IN(MIN)}^{2} \times T_{ON(MIN)} \times \eta}{2 \times V_{OUT} \times I_{OUT(MAX)}} \qquad (2)$$

where η is the efficiency, typically between 0.8 and 0.9. Note that this is the value of inductance that just barely delivers the required output current under worst case conditions. A lower value may be required to cover inductor tolerance, the effect of lower peak inductor currents caused by resistive losses, and minimum dead time between pulses.

Another method of determining the appropriate inductor value is to make an estimate based on the typical performance curves given in Figures 4 and 5. Figure 4 shows maximum output current as a function of input voltage for several inductor values. These are typical performance curves and leave no margin for inductance and ON-time variations. To accommodate worst case conditions, it is necessary to derate these curves by at least 10% in addition to inductor tolerance.

For example, a two cell to 5V application requires 80mA of output current while using an inductor with 15% tolerance. The output current should be derated by 25% to 100mA to cover the combined inductor and ON-time

7

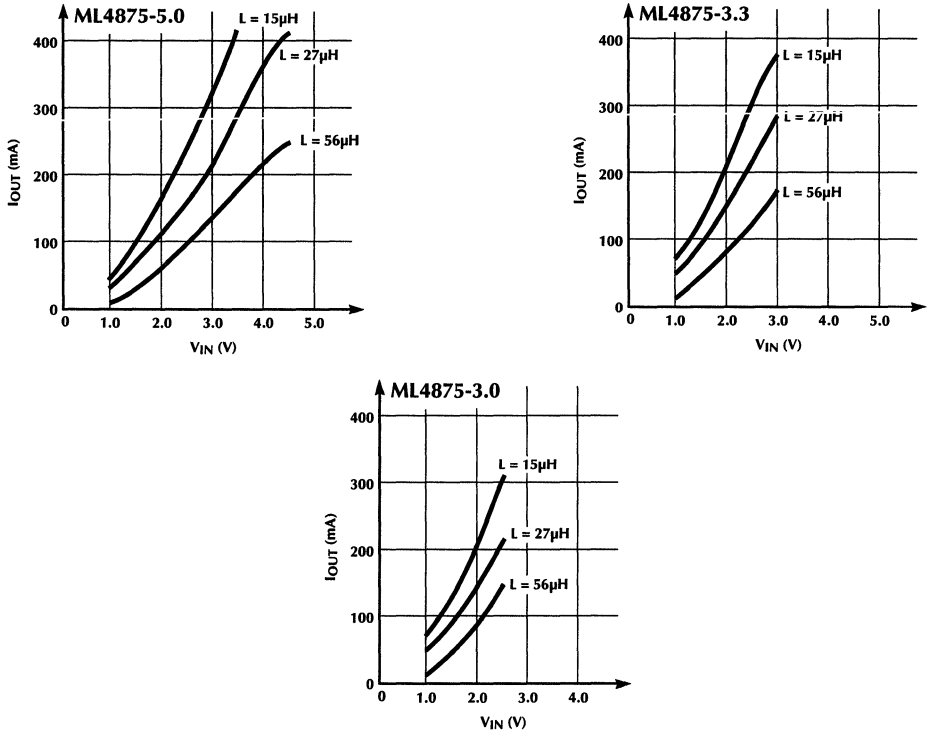


Figure 4. Output Current vs Input Voltage.

tolerances. Assuming that 2V is the end of life voltage of a two cell input, Figure 4 shows that with a 2V input, the ML4875-5 delivers 99mA with a 27µH inductor.

Figure 5 shows efficiency under the conditions used to create Figure 4. It can be seen that efficiency is mostly independent of input voltage and is closely related to inductor value. This illustrates the need to keep the inductor value as high as possible to attain peak system efficiency. As the inductor value goes down to 15µH, the efficiency drops to between 70% and 75%. With 56µH, the efficiency approaches 90% and there is little room for improvement. At values greater than 100µH, the operation of the synchronous rectifier becomes unreliable because the inductor current is so small that it is difficult for the control circuitry to detect. The data used to generate Figures 4 and 5 is provided in Table 1.

After the appropriate inductor value is chosen, it is necessary to find the minimum inductor current rating required. Peak inductor current is determined from the following formula:

$$I_{L(PEAK)} = \frac{T_{ON(MAX)} \times V_{IN(MAX)}}{L_{MIN}} \qquad (3)$$

In the two cell application previously described, a maximum input voltage of 3V would give a peak current of 1.2A. When comparing various inductors, it is important to keep in mind that suppliers use different criteria to determine their ratings. Many use a conservative current level, where inductance has dropped to 90% of its normal level. In any case, it is a good idea to try inductors of various current ratings with the ML4875 to determine which inductor is the best choice. Check efficiency and maximum output current, and if a current probe is available, look at the inductor current to see if it looks like the waveform shown in Figure 3. For additional information, see Applications Note 29.

Suitable inductors can be purchased from the following suppliers:

Coilcraft	(708) 639-6400
Coiltronics	(407) 241-7876
Dale	(605) 665-9301
Sumida	(708) 956-0666

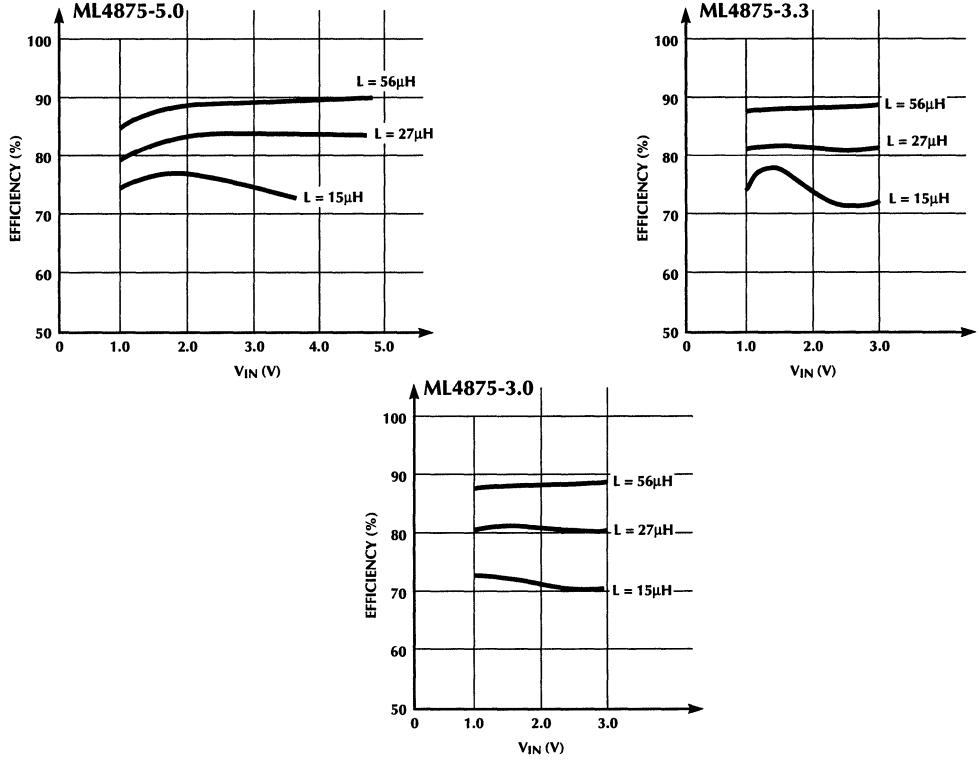


Figure 5. Typical Efficiency as a Function of V_{IN}.

OUTPUT CAPACITOR

The choice of output capacitor is also important, as it controls the output ripple and optimizes the efficiency of the circuit. Output ripple is influenced by three capacitor parameters: capacitance, ESR, and ESL. The contribution due to capacitance can be determined by looking at the change in capacitor voltage required to store the energy delivered by the inductor in a single charge-discharge cycle, as determined by the following formula:

$$\Delta V_{OUT} = \frac{T_{ON}^2 \times V_{IN}^2}{2 \times L \times C \times (V_{OUT} - V_{IN})} \qquad (4)$$

For a 2.4V input, and 5V output, a 27µH inductor, and a 47µF capacitor, the expected output ripple due to capacitor value is 87mV.

Capacitor Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL), also contribute to the output ripple due to the inductor discharge current waveform. Just after the NMOS transistor turns off, the output current ramps quickly to match the peak inductor current. This fast change in current through the output capacitor's ESL causes a high frequency (5ns) spike that can be over 1V in magnitude. After the ESL spike settles, the output voltage still has a ripple component equal to the inductor discharge current times the ESR. This component will have a sawtooth shape and a peak value equal to the peak inductor current times the ESR. ESR also has a negative effect on efficiency by contributing I-squared R losses during the discharge cycle.

An output capacitor with a capacitance of 100µF, an ESR of less than 0.1Ω, and an ESL of less than 5nH is a good general purpose choice. Tantalum capacitors which meet these requirements can be obtained from the following suppliers:

Matsuo	(714) 969-2491
Sprague	(603) 224-1961

If ESL spikes are causing output noise problems, an EMI filter can be added in series with the output.

7

INPUT CAPACITOR

Unless the input source is a very low impedance battery, it will be necessary to decouple the input with a capacitor with a value of between 47µF and 100µF. This provides the benefits of preventing input ripple from affecting the ML4875 control circuitry, and it also improves efficiency by reducing I-squared R losses during the charge and discharge cycles of the inductor. Again, a low ESR capacitor (such as tantalum) is recommended.

DRIVING THE SHDN INPUT

Unlike other boost regulators which use external Schottky diodes, the ML4875 has the ability to isolate the load from the battery input when the SHDN pin is high. Since there may be no other voltage available when the regulator is in shutdown, the SHDN input threshold is set well below the minimum V_{IN} voltage. SHDN can be driven directly from an open collector device with a high value pull-up resistor to V_{IN}. If SHDN is driven from a TTL or CMOS output device, a resistor divider should be used to prevent the SHDN input high level from exceeding V_{IN}, and to ensure the SHDN input low level is below the 200mV threshold.

SETTING THE $\overline{\text{RESET}}$ THRESHOLD

To use the $\overline{\text{RESET}}$ comparator as an input voltage monitor, it is necessary to use an external resistor divider tied to the DETECT pin as shown in the block diagram. The resistor values R_A and R_B can be calculated using the following equation:

$$V_{IN(MIN)} = 0.2 \times \frac{(R_A + R_B)}{R_B} \quad (5)$$

The value of R_B should be 100kΩ or less to minimize bias current errors. R_A is then found by rearranging the equation:

$$R_A = R_B \times \left(\frac{V_{IN(MIN)}}{0.2} - 1 \right) \quad (6)$$

LAYOUT

Good PC board layout practices will ensure the proper operation of the ML4875. Important layout considerations include:

- Use adequate ground and power traces or planes
- Keep components as close as possible to the ML4875
- Use short trace lengths from the inductor to the V_L pin and from the output capacitor to the V_{OUT} pin
- Use a single point ground for the ML4875 ground pins, and the input and output capacitors

TABLE 1. MAXIMUM OUTPUT CURRENT AND EFFICIENCY.

ML4875-5.0

V_{IN} (V)	I_{IN} (mA)	I_{OUT} (mA)	EFFICIENCY %
L = 15µH			
1.0	237.5	35.7	75.2
1.5	373.3	86.2	77.0
2.0	494.6	151.8	76.7
2.5	616.0	233.5	75.8
3.0	710.5	319.7	75.0
3.5	793.9	410.5	73.9
L = 27µH			
1.0	138.2	22.0	79.6
1.5	220.7	54.8	82.8
2.0	296.2	98.8	83.4
2.5	374.1	156.1	83.5
3.0	441.6	220.7	83.3
3.5	496.4	289.4	83.3
4.0	538.2	358.5	83.3
4.5	542.6	408.0	83.5
L = 56µH			
1.0	72.5	12.2	84.1
1.5	113.1	29.8	87.8
2.0	158.7	56.3	88.7
2.5	201.6	89.7	89.0
3.0	237.5	127.0	89.1
3.5	270.4	169.0	89.3
4.0	297.4	212.9	89.5
4.5	310.4	251.0	89.8

ML4875-3.3

V_{IN} (V)	I_{IN} (mA)	I_{OUT} (mA)	EFFICIENCY %
L = 15µH			
1.0	243.1	54.6	74.1
1.5	346.6	122.1	77.5
2.0	473.6	207.8	72.4
2.5	551.9	299.9	71.7
3.0	563.6	368.0	71.8
L = 27µH			
1.0	144.5	35.4	80.8
1.5	218.4	80.9	81.5
2.0	292.3	143.6	81.1
2.5	345.7	211.8	80.9
3.0	357.2	263.7	81.2
L = 56µH			
1.0	73.9	19.5	87.1
1.5	118.5	47.2	87.6
2.0	156.8	83.4	87.8
2.5	189.0	125.7	87.8
3.0	206.6	165.5	88.1

ML4875-3.0

V_{IN} (V)	I_{IN} (mA)	I_{OUT} (mA)	EFFICIENCY %
L = 15µH			
1.0	242.8	59.2	73.1
1.5	362.6	131.3	72.4
2.0	461.6	219.2	71.2
2.5	523.5	308.5	70.7
L = 27µH			
1.0	144.9	38.9	80.5
1.5	218.7	88.2	80.7
2.0	286.8	153.4	80.2
2.5	325.6	217.5	80.2
L = 56µH			
1.0	74.3	21.5	86.8
1.5	119.1	52.0	87.3
2.0	154.9	90.2	87.3
2.5	183.0	133.2	87.3

ORDERING INFORMATION

PART NUMBER	OUTPUT VOLTAGE	TEMPERATURE RANGE	PACKAGE
ML4875CS-T	3.0V	0°C to +70°C	8-Pin SOIC (S08)
ML4875CS-3	3.3V	0°C to +70°C	8-Pin SOIC (S08)
ML4875CS-5	5.0V	0°C to 70°C	8-Pin SOIC (S08)
ML4875ES-T	3.0V	–20°C to +70°C	8-Pin SOIC (S08)
ML4875ES-3	3.3V	–20°C to +70°C	8-Pin SOIC (S08)
ML4875ES-5	5.0V	–20°C to +70°C	8-Pin SOIC (S08)

LCD Backlight Lamp Driver with Contrast

GENERAL DESCRIPTION

The ML4876 is an ideal solution for driving small cold cathode fluorescent tubes (CCFL) used in liquid crystal display (LCD) backlight applications. It provides the dimming ballast control and the contrast control for the LCD display.

By utilizing differential drive the ML4876 can deliver the same light output with significantly less input power compared to existing single ended drive schemes. Improvements as high as 30% can be realized when using low power lamps and advanced LCD screen housings. This increased light output is achieved because the differential drive configuration is much less sensitive, and therefore less power is wasted in the capacitive parasitics that exist in the backlight housing. An additional benefit of this configuration is an even distribution of light.

The ML4876 is optimized for portable applications where high efficiency is critical to maximize battery life. The high efficiency is achieved by a resonant scheme with zero voltage switching. The complete system, including the magnetics, can be easily implemented with standard off the shelf power components.

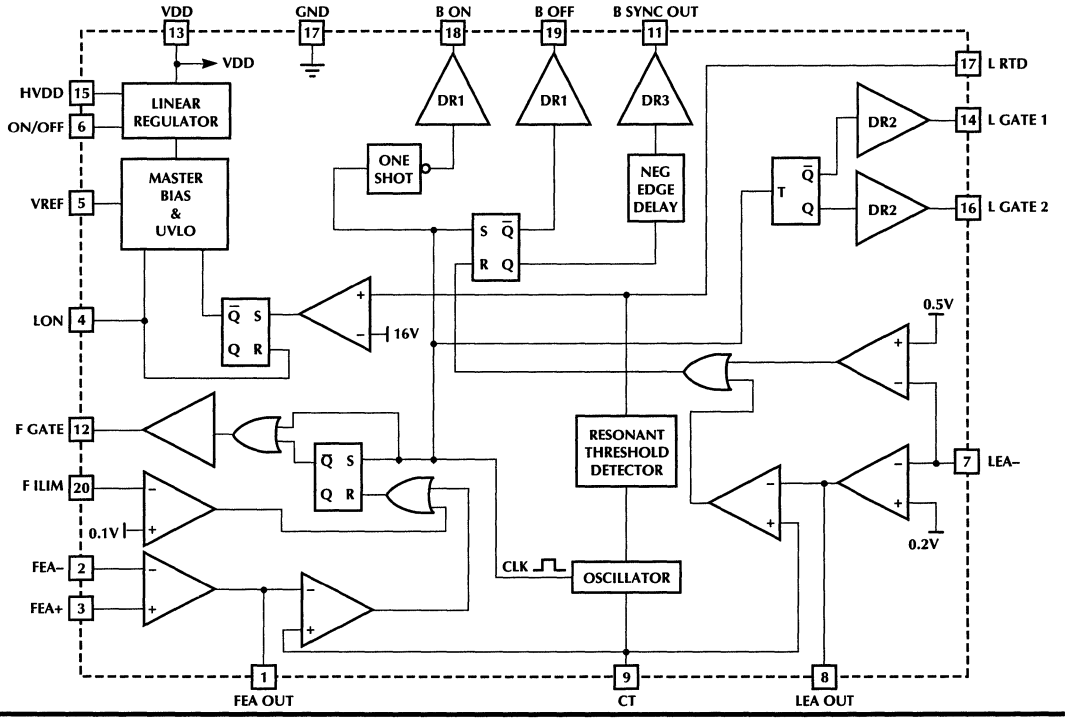
All of the regulators on the chip are synchronized to the inverter frequency to eliminate the ghosting and flicker common to asynchronous circuits.

The ML4876 is available in very small form factor package (20 pin SSOP) making it ideal for hand held portable applications.

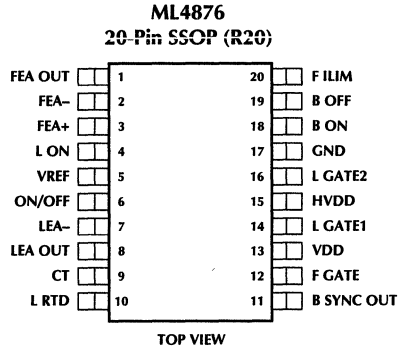
FEATURES

- Backlight Lamp Driver with Differential Drive
- Up to 30% Lower Power for Same Light Output
- Low Standby Current (< 10µA)
- Improved Efficiency (≈95%)
- Allows All N-Channel MOSFET Drive
- Low Switching Losses
- Resonant Threshold Detection
- Buck Regulator uses Synchronous Rectification

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

PIN#	NAME	DESCRIPTION
1	FEA OUT	Output of flyback (contrast) error amplifier.
2	FEA–	Negative input of flyback (contrast) error amplifier.
3	FEA+	Positive input of flyback (contrast) error amplifier.
4	L ON	Logic input. A "0" on this pin disables the lamp driver section only.
5	VREF	Voltage reference output.
6	ON/OFF	Logic input. A "0" on this pin disables the linear regulator.
7	LEA–	Negative input for lamp error amplifier.
8	LEAOUT	Output of lamp error amplifier.
9	CT	Oscillator timing capacitor.
10	L RTD	Input to resonant threshold detector.
11	B SYNC OUT	Output of MOSFET driver. Connects to gate of synchronous FET catch diode.
12	F GATE	Connects to gate of MOSFET in primary side of contrast control.
13	VDD	Output of linear regulator. Positive power for IC.
14	L GATE1	Output of MOSFET driver. Connection to gate of one side of inverter FET drive pair.
15	HVDD	Battery power input to linear regulator.
16	L GATE2	Output of MOSFET driver. Connection to gate of one side of inverter FET drive pair.
17	GND	Ground
18	B ON	Connection to primary side of gate pulse transformer.
19	B OFF	Output of MOSFET driver. Connection to gate of FET that disables the input power.
20	F ILIM	Input to current limit comparator.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 75mA
Output Current, Source or Sink 250mA
Voltage on Pins 1-9, 11-14, 16-20 ....–0.3V to VDD +0.3V
Voltage on Pin 15 ..... 20V
Current into Pin 10 ..... ±10mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA}) Plastic SSOP ..... 100°C/W

OPERATING CONDITIONS

Temperature Range
ML4876C ..... 0°C to +70°C
ML4876E ..... –20°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VDD = 5V ±5%, T_A= –20°C to 70°C, CT = 47pF (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT REGULATOR SECTION					
Error Amplifier					
Open Loop Gain		60	70		dB
Bias Point	Closed loop	0.18	0.2	0.22	V
Output High	I_{LOAD} = 5µA	2.8	3.0		V
Output Low	I_{LOAD} = 25µA		0.4	0.7	V
Bandwidth (–3dB)			1		MHz
Input Voltage Range		–0.3	0.2	VREF	V
Input Bias Current			50	100	nA
Current Limit Comparator					
Current Threshold		450	500	550	mV
Input Bias Current	V_{LILIM} = 0.1V		50	100	nA
Propagation Delay	(Note 2)		30		ns
Output Drivers					
Output High - B SYNC OUT, B OFF	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
Output Low - B SYNC OUT, B OFF	I_{LOAD} = 12mA		0.2	0.375	V
Rise & Fall time - B SYNC OUT, B OFF	C_{LOAD} = 100pF		20	50	ns
Output High - B ON	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
Output Low - B ON	I_{LOAD} = 50mA		0.2	0.375	V
Fall Time - B ON	C_{LOAD} = 2400pF (Note 2)		45	80	ns
ONE SHOT Pulse Width		100	150	200	ns
DELAY TIMER Delay Time		20	35	55	ns
FLYBACK REGULATOR SECTION					
Error Amplifier					
Open Loop Gain		60	70		dB
Offset Voltage		–15		+15	mV
Output High	I_{LOAD} = 5µA	2.8	3.0		V
Output Low	I_{LOAD} = 25µA		0.4	0.7	V

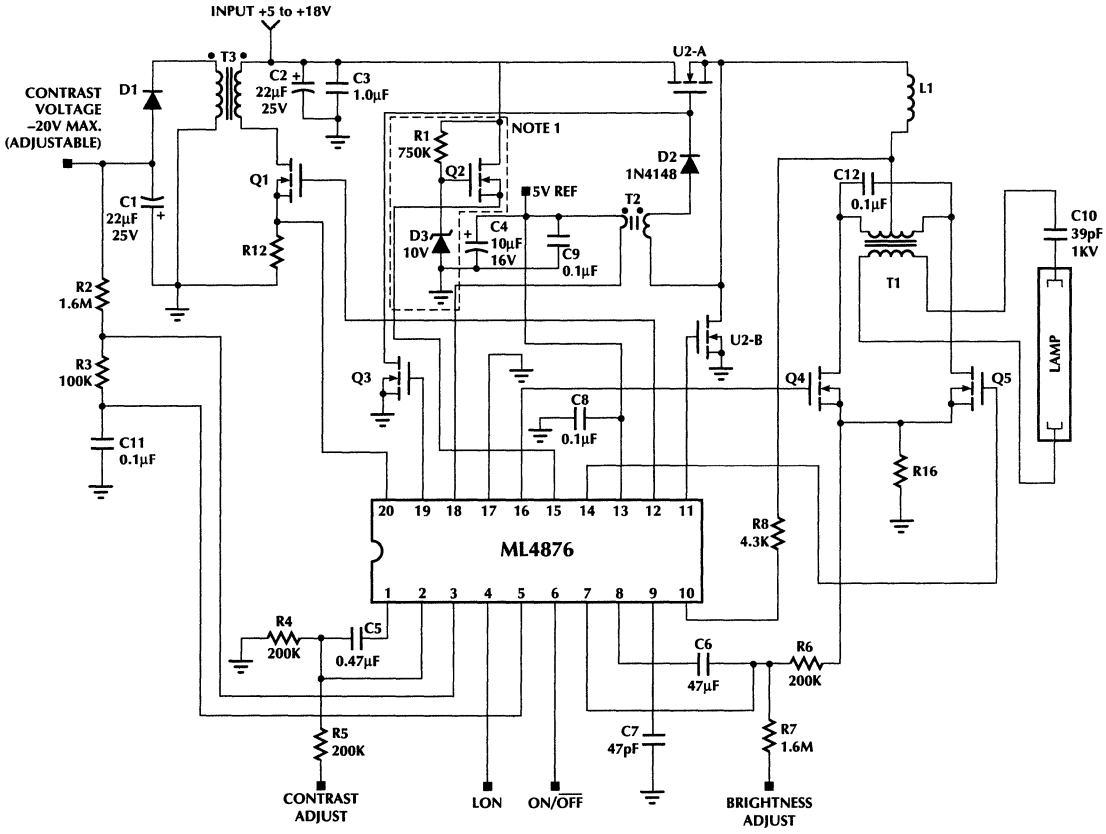
ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FLYBACK REGULATOR SECTION					
Current Limit Comparator					
Threshold		70	100	130	mV
Input Bias Current	V_{LILIM} = 0.1V		50	100	nA
Propagation Delay			125	250	ns
Output Drivers					
Output High - F Gate	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
Output Low - F Gate	I_{LOAD} = 50mA		0.2	0.375	V
Rise & Fall Time	C_{LOAD} = 1000pF		20	50	ns
HIGH VOLTAGE INVERTER SECTION					
Oscillator					
Nominal Frequency		59	70	81	kHz
Discharge Current	V_{CT} = 2V	600	700	900	µA
Peak Voltage		2.3	2.5	2.7	V
Valley Voltage		0.8	1	1.2	V
Output Drivers					
Output High - L GATE 1, 2	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
Output Low - L GATE 1, 2	I_{LOAD} = 50mA		0.2	0.375	V
Rise & Fall Time - L GATE 1, 2	C_{LOAD} = 1000pF		20	50	ns
Resonant threshold Detector					
Threshold		0.75	1.1	1.45	V
Hysteresis		250	500	750	mV
Lamp Out Detect					
Threshold		16	18	20	V
Under Voltage Detector					
Start Up Threshold		3.8	4.1	4.4	V
Hysteresis		150	300	450	mV
Logic Interface (On/Off, LON)					
VIH		2.6			V
VIL				0.5	V
Input Bias Current	VI = 3V		10	25	µA
Linear Regulator Section					
Regulator Voltage (VDD)	HVDD = 12V	4.75	5.0	5.35	V
Regulator Source Current	External to device		10		mA
Drop Out Voltage	I_{HVDD} = 1mA		30	90	mV
Drop Out Voltage	I_{HVDD} = 5mA		125	275	mA
HVDD Input Voltage Range		5		18	V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Bias Section					
VDD Supply Current (No Load)	On/Off = 3V, L_{ON} = 3V		0.45	0.6	mA
VDD Supply Current	On/Off = 3V, L_{ON} = 0V		200	350	µA
VDD Supply Current	On/Off = "0", HVDD = 12V			10	µA
VREF Output Voltage	T_A = 25°C	2.47	2.5	2.53	V
VREF Load Regulation	I_{VREF} = 25µA		10	20	mV
VREF Line Regulation			20	30	mV
VREF Line, Load, Temp		2.465	2.5	2.535	V

Note 1: Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.
Note 2: Actual load is 1200pF. The 2:1 transformer reflects an effective 2400pF.



NOTE 1
R1, D3, Q2 ARE OPTIONAL AND ALLOWS A BATTERY VOLTAGE RANGE FROM +7 TO +28V. REMOVING THESE COMPONENTS AND CONNECTING DIRECTLY TO THE INPUT VOLTAGE ALLOWS +5.0 TO +18V.

Figure 1. Typical Application Schematic for the ML4876

FUNCTIONAL DESCRIPTION

The ML4876 consists of a PWM regulator, a lamp driver/ inverter, a linear regulator, a flyback regulator, and control circuits. This IC, in conjunction with external components, converts a DC battery voltage into the high voltage and high frequency ac signal required to start and drive miniature cold cathode fluorescent lamps. In addition it generates the DC voltage for the contrast requirements of LCD screens. A typical application circuit is shown in figure 1. Please refer to Application Note 32 for detailed application information beyond what is presented here.

Note: Please read the Power Sequencing section below prior to using the ML4876.

LAMP DRIVER

The lamp driver, sometimes referred to as a lamp inverter, is comprised of a PWM regulator and a Royer type inverter circuit to drive the lamp. The PWM regulator, in a buck configuration, controls the magnitude of the lamp current to provide the dimming capability. Figure 2 shows a simplified circuit to more easily illustrate the operation of the circuit.

Due to the presence of the buck inductor, L1, the circuit shown in figure 2 is essentially a current fed parallel loaded resonant circuit. Lm is the primary inductance of the output transformer, T1, which tunes with the resonant capacitor C_R to set the resonant frequency of the inverter. The oscillator frequency is always set lower than the natural resonant frequency to ensure synchronization. The current source IC models the current through the buck inductor L1.

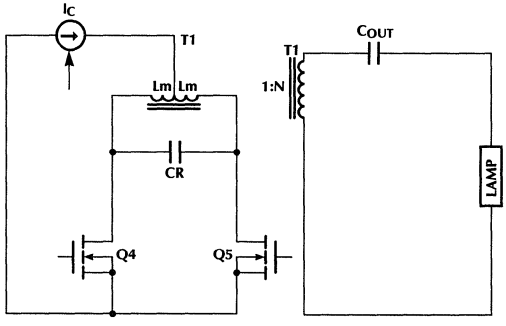


Figure 2. Simplified Lamp Driver Circuit

The MOSFETs, Q4 and Q5 are alternately turned on with a constant 50% duty cycle signal (L GATE1, L GATE2) at one-half the frequency of the oscillator. In this way each transistor pulses, or excites, the resonant tank on each half cycle. The combination of these two signals appear across the primary winding of the output transformer as a sinusoidal waveform. This voltage is multiplied by the step-up turns ratio of the output transformer and impressed across the lamp.

The output transitions are controlled by feedback through the L RTD pin by sensing the voltage at the center tap of the output transformer. Each time this signal reaches the minimum resonant threshold detection point an internal clock pulse is generated to keep the system synchronized. Figure 3 shows some of these representative waveforms at the important nodes of the circuit.

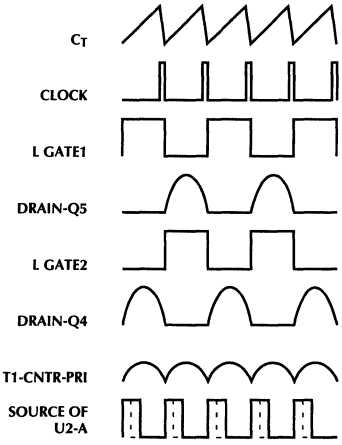


Figure 3. Operating Waveforms of the Lamp Driver Section

The PWM regulator is comprised of a MOSFET (U2-A), inductor L1, and the gate control and drive circuitry as shown in figure 1. A signal with a constant pulse width of 150nS is applied to the primary of the 2:1 pulse transformer T2, rectified by diode D2, and used to charge the gate capacitance of U2-A, thereby turning it on. The turn off is controlled by discharging this capacitance through MOSFET U2-B. The pulse width of the signal on the gate of U2-B (B OFF) varies according to the amplitude of the feedback signal on LEA–, pin 7, which is proportional to the ac current flowing in the lamp. This feedback signal is developed by monitoring the current through resistor R6 in the common source connection of the inverter MOSFETs, Q4 and Q5. The lamp current, and therefore brightness, is adjusted by varying the voltage applied to R7, at the brightness adjust control point. Increasing this voltage decreases the brightness.

CONTRAST CONTROL GENERATOR

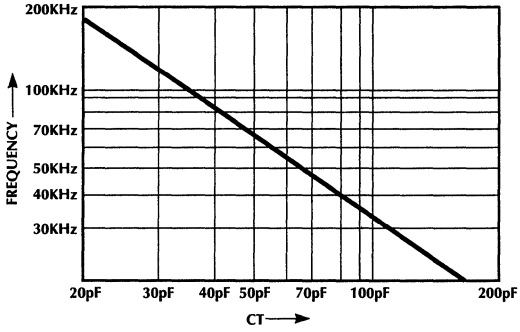
The contrast voltage generator is a separate regulator in a flyback configuration. In conjunction with the external transformer (T3), MOSFET (Q1), diode (D1), and assorted capacitors and resistors, it provides an adjustable DC output contrast voltage necessary to drive LCD screens. The voltage is adjusted by controlling the voltage applied to R5, at the contrast adjustment point.

The contrast voltage can be made either positive or negative simply by changing the connection of the external components. The schematic shown in figure 1 is connected for a negative voltage. Please refer to Application Note 32 for the circuit connection for a positive output voltage.

OSCILLATOR

The frequency of the oscillator in-the ML4876 is set by selecting the value of CT.

The following graph shows the oscillator frequency versus the value of CT. This nomograph may be used to select the appropriate value of CT to achieve the desired oscillator frequency.



LINEAR REGULATOR

A linear voltage regulator is provided to power the low voltage and low current control circuitry on the ML4876. This is typically used when there is no separate 5 volt supply available at the inverter board. For operation up to 18 volts the linear regulator is used by connecting the HVDD pin to the input battery voltage. For operation over 18 volts, a MOSFET, and a resistor (Q2 and R1, in figure 1) are connected as shown. The MOSFET is required to stand off the high voltage.

LAMP OUT DETECT

In those cases when there is no lamp connected, or the connection is faulty, the output voltage of the lamp driver circuit will tend to rise to a high level in an attempt to start the nonexistent lamp. The lamp out detect circuit on the ML4876 will detect this condition by sensing the center tap voltage on the primary of the output transformer, T1 on the L RTD pin. When this voltage exceeds 16 volts, an internal latch is set and the lamp driver goes into a shutdown mode. The logic control pin L ON must be cycled low, then high to reset the latch and return the lamp driver to the normal state.

LOGIC CONTROL

The ML4876 is controlled by a two logic inputs, L ON and ON/OFF. A logic level high on the L ON pin enables just the lamp driver. A logic zero on the L ON pin disable the lamp driver only. A logic level high on the ON/OFF pin enable the complete circuit. A logic level low on the ON/OFF pin puts the circuit into a very low power state.

POWER SEQUENCING

It is important to observe correct power and logic input sequencing when powering up the ML4876. The following procedure must be observed to avoid damaging the device.

1. Apply the battery power to HVDD
2. Apply the VDD voltage (if HVDD is not used). With HVDD connected this voltage is supplied by the internal regulator on the ML4876.
3. Apply a logic high to the ON/OFF input. This will enable the internal linear regulator to ensure the VDD supply is on (when HVDD is used).
4. Apply a logic high to the L ON input.

7

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4876CR	0°C to +70°C	Molded SSOP (R20)
ML4876ER	–20°C to +70°C	Molded SSOP (R20)

ML4876EVAL

Differential Drive LCD Backlight with Contrast Evaluation Kit

GENERAL DESCRIPTION

The ML4876 is a cold cathode fluorescent lamp (CCFL) controller featuring dimming control and contrast voltage generation. It is commonly used to power the entire LCD display found in many handheld instruments. This evaluation board enables the designer to explore the capabilities of the circuit and determine its suitability for a current or new design.

The printed circuit board is miniaturized using surface mount components for space efficiency, and can be readily interfaced to most systems. The board measures 0.65"W x 5.31"L x 0.235"H including the tallest component when assembled with the optional contrast/ dimming potentiometers and switches. The board can be shortened to 4" by cutting off the control section.

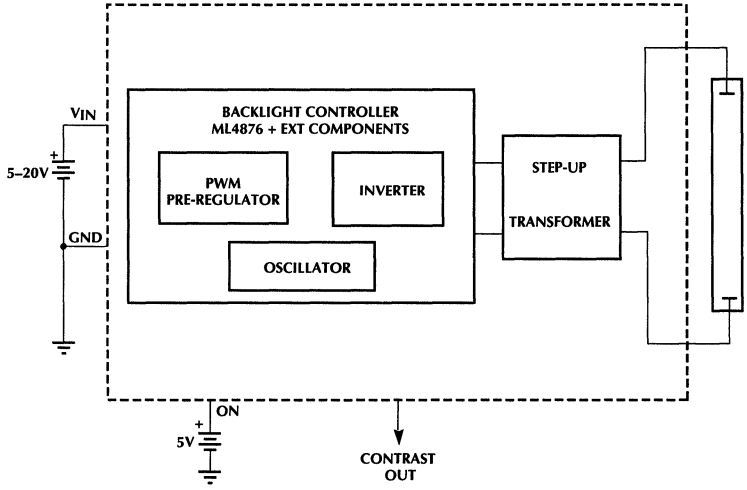
FEATURES

- Operates Over a 5 to 20V Supply Range
- Efficiency Greater than 90%
- Differential Lamp Drive Improves Dimming Range
- Negative Contrast Voltage output (0 to –20V)
- Capable of Driving Lamp Up to 5W
- Low Profile, High Density PC Board Layout

KIT COMPONENTS

- ML4876 User's guide
- ML4876 Data Sheet
- A fully functional evaluation board
- Application Notes 26 and 32
- Miniature Fluorescent Lamp
- PCB Layout Gerber File

BLOCK DIAGRAM



FEATURING
Extended Commercial Temperature Range
–20°C to 70°C
for Portable Handheld Equipment

December 1994
ADVANCED INFORMATION

ML4880

Portable PC and PCMCIA Power Controller

GENERAL DESCRIPTION

The ML4880 Portable PC and PCMCIA Power Controller is a complete solution for DC/DC power conversion for portable computing systems with single or multiple PCMCIA slots. A complete Pulse Frequency Modulated (PFM) power conversion and management system can be realized with the addition of one of Micro Linear's Backlight and Contrast Controllers (ML4864, ML4874, or ML4876).

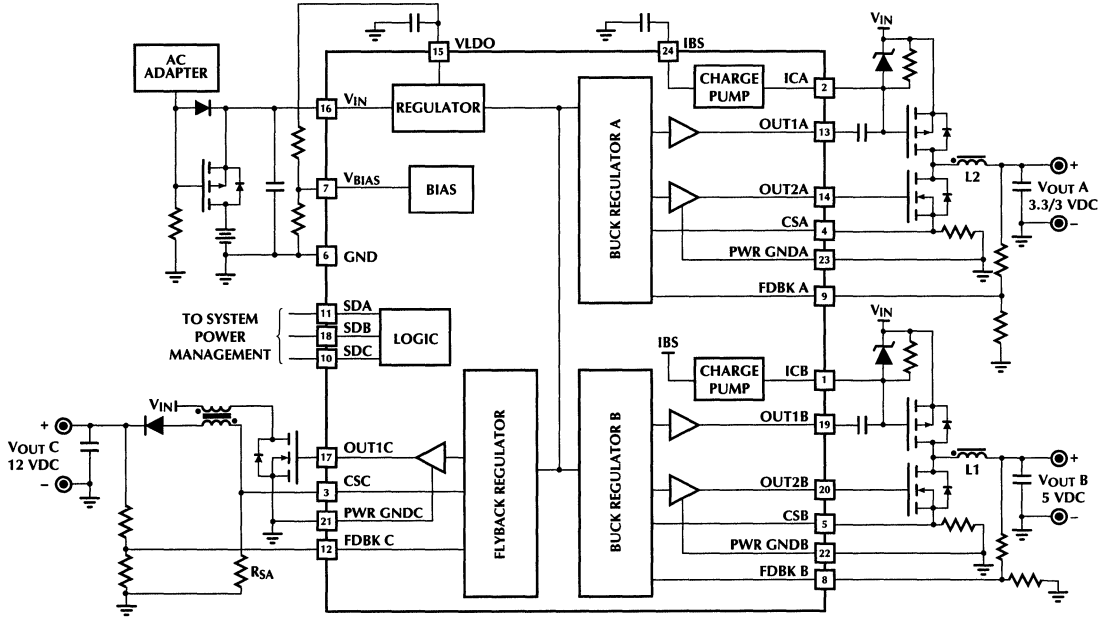
The device provides two synchronous buck converters to implement mixed voltage systems and a flyback converter for 12V V_{PP} generation for PCMCIA. The flyback architecture enables generation of high currents (150mA or more per slot) on the 12V bus for multiple slot PCMCIA applications.

Each regulator can be independently switched off to fully isolate the load from the power supply. The PFM architecture will automatically adjust switching frequency at light loads in order to maintain power conversion efficiencies in excess of 90%. Overall power conversion efficiencies are greater than 90% over an output power range of almost 3 decades (50mW to 33W). High switching frequencies allow use of small external components, reducing power supply size and cost.

FEATURES

- Regulation to ±3% maximum: provides 2% PCMCIA switch matrix margin
- Two synchronous buck converters for 3.3/3V, 5V generation, and a flyback for high current, 12V generation from 5.5V to 18V input
- Regulator power conversion efficiencies > 90% over 3 decades (5mA to 2A) of output current
- Pulse Frequency Modulation for high efficiency operation
- Independent regulator shutdown for full load isolation
- Operation up to 300kHz
- Adjustable current limit
- Wide input voltage range (5.5V to 18V)
- Micropower operation (I_Q < 300µA)

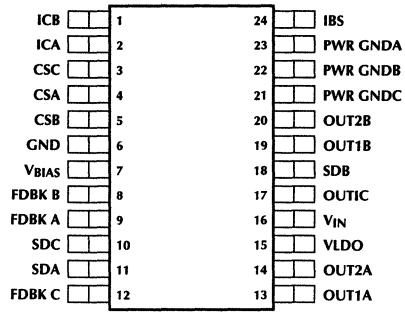
BLOCK DIAGRAM



7

PIN CONFIGURATION

ML4880
24-Pin SOIC (S24W)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	ICB	Charge pump, output 1B
2	ICA	Charge pump, output 1A
3	CSC	Current sense, regulator C
4	CSA	Current sense, regulator A
5	CSB	Current sense, regulator B
6	GND	Ground
7	V_{BIAS}	Bias voltage
8	FDBK B	Feedback node, buck regulator B
9	FDBK A	Feedback node, buck regulator A
10	SDC	Shutdown regulator C
11	SDA	Shutdown regulator A
12	FDBK C	Feedback node, flyback regulator

PIN#	NAME	FUNCTION
13	OUT1A	P-channel drive, regulator A
14	OUT2A	N-channel drive, regulator A
15	VLDO	Linear regulator output
16	V_{IN}	Power supply input voltage
17	OUT1C	N-channel drive, regulator C
18	SDB	Shutdown regulator B
19	OUT1B	P-channel drive, regulator B
20	OUT2B	N-channel drive, regulator B
21	PWR GNDC	Power Ground, regulator C
22	PWR GNDB	Power Ground, regulator B
23	PWR GNDA	Power Ground, regulator A
24	IBS	Charge pump capacitor input

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4880ES	–20°C to +70°C	24-PIN SOIC (S24W)

FEATURING
Extended Commercial Temperature Range
–20°C to 70°C
for Portable Handheld Equipment

December 1994
ADVANCED INFORMATION

ML4890

High Efficiency Low Ripple Boost Regulator

GENERAL DESCRIPTION

The ML4890 is a high efficiency, PFM (Pulse Frequency Modulation), boost switching regulator connected in series with an integrated LDO (Low Dropout Regulator) that incorporates "Silent Switcher"™ technology. This technique incorporates a patented tracking scheme to minimize the voltage drop across the LDO and increase the total efficiency of the regulator beyond that which can be obtained by using a descrete external LDO regulator.

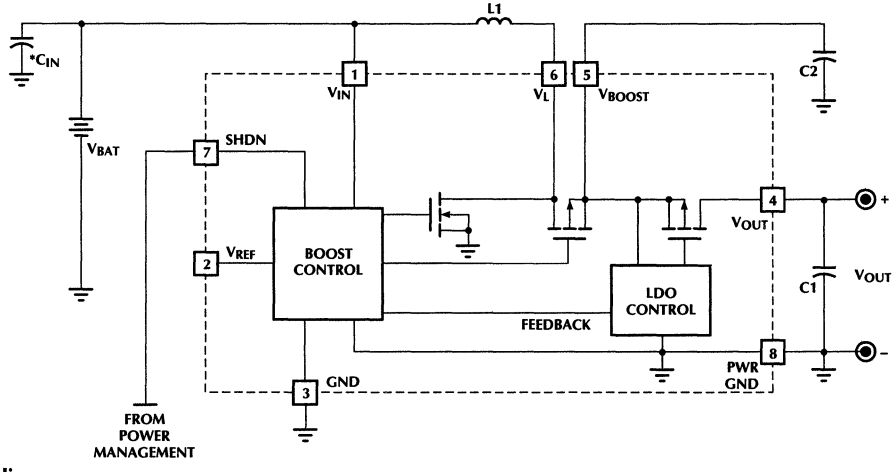
The ML4890 is designed to convert multiple cell battery inputs to regulated output voltages for integrated circuits and is ideal for portable communications equipment that cannot tolerate the output voltage ripple normally associated with switching regulators.

An integrated synchronous rectifier eliminates the need for an external Schottky diode and provides a lower forward voltage drop, resulting in higher conversion efficiency.

FEATURES

- Incorporates "Silent Switcher"™ technology to deliver very low output voltage ripple (<5mV)
- Guaranteed full load start-up and operation at 1.0V input and low operating quiescent current (<100µA) for extended battery life
- Pulse Frequency Modulation and Internal Synchronous Rectification for high efficiency
- Minimum external components
- Low ON resistance internal switching FETs
- 5V, 3.3V, and 3V output versions

BLOCK DIAGRAM

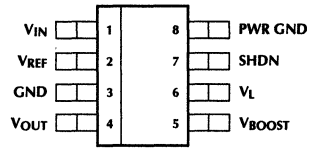


Patent Pending

***Optional**

PIN CONNECTION

ML4890-5/-3/-T
8-Pin SOIC (S08)



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	V_{IN}	Battery input voltage
2	V_{REF}	200mV reference pin
3	GND	Analog signal ground
4	V_{OUT}	LDO linear regulator output
5	V_{BOOST}	Boost regulator output for connection of an output filter capacitor
6	V_L	Boost inductor connection
7	SHDN	Pulling this pin to V_{IN} through an external resistor shuts down the regulator, isolating the load from the input
8	PWR GND	Return for the NMOS boost transistor

ORDERING INFORMATION

PART NUMBER	OUTPUT VOLTAGE	TEMPERATURE RANGE	PACKAGE
ML4890CS-T	3.0V	0°C to +70°C	8-Pin SOIC (S08)
ML4890CS-3	3.3V	0°C to +70°C	8-Pin SOIC (S08)
ML4890CS-5	5.0V	0°C to +70°C	8-Pin SOIC (S08)
ML4890ES-T	3.0V	–20°C to +70°C	8-Pin SOIC (S08)
ML4890ES-3	3.3V	–20°C to +70°C	8-Pin SOIC (S08)
ML4890ES-5	5.0V	–20°C to +70°C	8-Pin SOIC (S08)

ML4890EVAL

Low Ripple Boost Regulator Evaluation Kit

GENERAL DESCRIPTION

The ML4890EVAL kit provides a convenient vehicle to evaluate the ML4890 low ripple boost regulator IC. The kit contains a fully assembled circuit board and all of the necessary documentation to quickly evaluate a typical application circuit. The board was designed to demonstrate performance and to illustrate critical layout practices necessary for reliable operation of the circuit.

The ML4890 is complete solution for DC to DC conversion in 1 to 3 cell battery powered systems. The circuit is ideal in applications requiring high effeciency, low ripple and a minimum number of external components.

The boost IC is capable of running with input voltages as low as 0.95V and is available in four different output versions: a 3V output (ML4890-T), a 3.3V output (ML4890-3.3), a 5V output (ML4890-5), or adjustable output versions (ML4790 and ML4990).

FEATURES

- High Efficiency
- Low Output Ripple Voltage
- Minimal External Components
- Micro Power Operation
- Shutdown Current less than 8µA
- 3V, 3.3V, 5V, and Adjustable Output Versions

KIT COMPONENTS

The evaluation package contains the following items:

- ML4890EVAL User's guide
- ML4890 Data Sheet
- ML4890 Evaluation Board

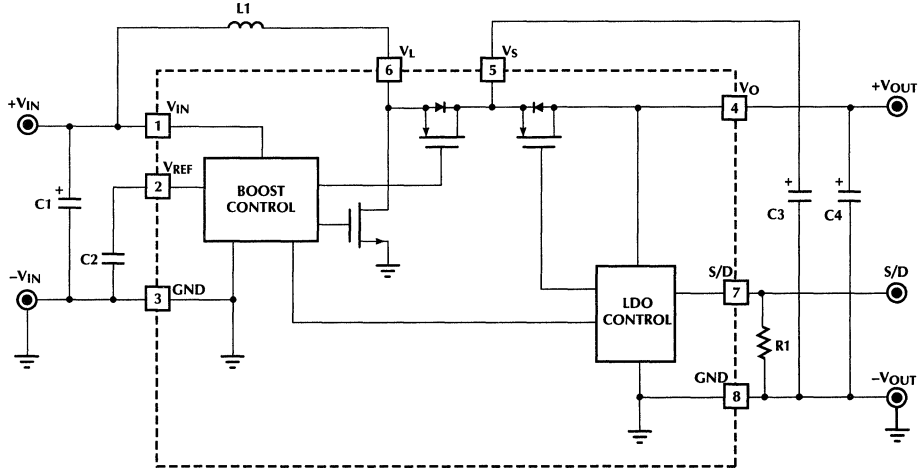


FIGURE 1: ML4890 Evaluation Board Schematic

ML4961

Adjustable Output Low Voltage Boost Regulator with Detect

GENERAL DESCRIPTION

The ML4961 is a boost regulator designed for DC to DC conversion in 1 to 3 cell battery powered systems. The combination of BiCMOS process technology, internal synchronous rectification, variable frequency operation, and low supply current make the ML4961 ideal for 1 cell applications. The ML4961 is capable of start-up with input voltages as low as 1V, and the output voltage can be set anywhere between 2.5V and 6V by an external resistor divider connected to the SENSE pin.

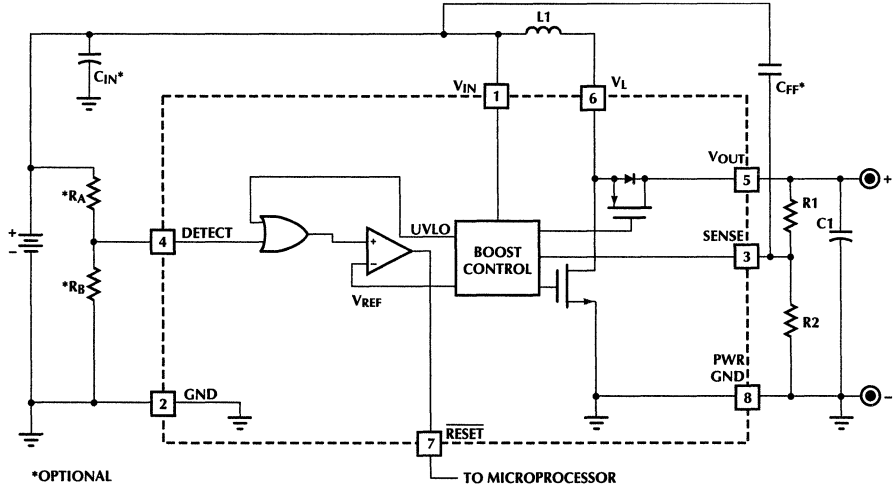
An integrated synchronous rectifier eliminates the need for an external Schottky diode and provides a lower forward voltage drop, resulting in higher conversion efficiency. In addition, low quiescent battery current and variable frequency operation result in high efficiency even at light loads. The ML4961 requires a minimum number of external components to build a very small adjustable regulator circuit capable of achieving conversion efficiencies in excess of 90%.

The circuit also contains a $\overline{\text{RESET}}$ output which goes low when the IC can no longer function due to low input voltage, or when the DETECT input drops below 200mV.

FEATURES

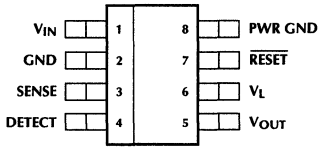
- Guaranteed full load start-up and operation at 1V input
- Pulse Frequency Modulation and Internal Synchronous Rectification for high efficiency
- Minimum external components
- Low ON resistance internal switching FETs
- Micropower operation
- Adjustable output voltage (2.5V to 6V)

BLOCK DIAGRAM



PIN CONNECTION

ML4961
8-Pin SOIC (S08)



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	V_{IN}	Battery input voltage
2	GND	Analog signal ground
3	SENSE	Programming pin for setting the output voltage
4	DETECT	Pulling this pin below V_{REF}, causes the $\overline{RESET}$ pin to go low
5	V_{OUT}	Boost regulator output
6	V_L	Boost inductor connection
7	$\overline{RESET}$	Output goes low when regulation cannot be achieved, or when DETECT goes below 200mV
8	PWR GND	Return for the NMOS output transistor

7

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Voltage on any pin 7V
Peak Switch Current, $I_{(PEAK)}$ 2A
Average Switch Current, $I_{(AVG)}$ 500mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA}) ..... 110°C/W

OPERATING CONDITIONS

Temperature Range
ML4961CS ..... 0°C to +70°C
ML4961ES ..... –20°C to +70°C
ML4961IS ..... –40°C to +85°C
V_{IN} Operating Range
ML4961CS ..... 1.0V to V_{OUT} –0.2V
ML4961ES, ML4961IS ..... 1.1V to V_{OUT} –0.2V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = Operating Voltage Range, T_A = Operating Temperature Range

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Supply					
V_{IN} Current	$V_{IN} = V_{OUT} - 0.2V$		45	55	µA
V_{OUT} Quiescent Current			3	5	µA
V_L Quiescent Current				1	µA
PFM Regulator					
Pulse Width (T_{ON})		9	10	11	µs
SENSE Comparator Threshold Voltage (V_{SENSE})		194	200	206	mV
Load Regulation	See Figure 1 V_{IN} = 1.2V, $I_{OUT} \leq$ 25mA V_{IN} = 2.4V, $I_{OUT} \leq$ 135mA	 4.85 4.85	 5.0 5.0	 5.15 5.15	 V V
Undervoltage Lockout Threshold			0.85	0.95	V
$\overline{\text{RESET}}$ Comparator					
DETECT Threshold		190	200	210	mV
DETECT Bias Current		–100		100	nA
$\overline{\text{RESET}}$ Output High Voltage (V_{OH})	I_{OH} = –100µA	V_{OUT} – 0.2			V
$\overline{\text{RESET}}$ Output Low Voltage (V_{OL})	I_{OL} = 100µA			0.2	V

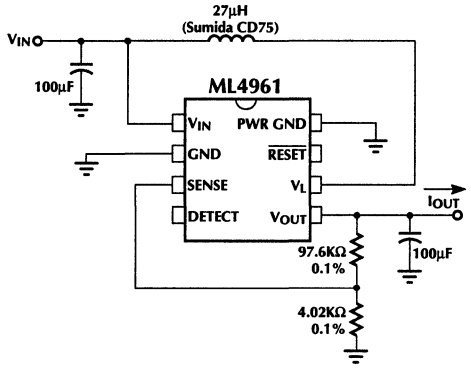


Figure 1. PFM Regulator Block Diagram.

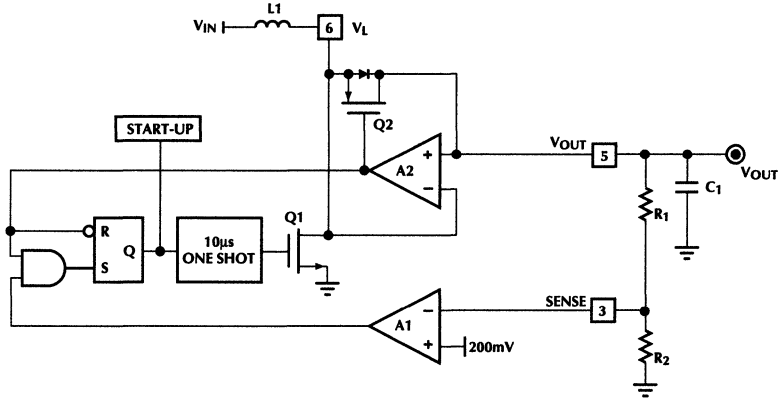


Figure 2. PFM Regulator Block Diagram.

FUNCTIONAL DESCRIPTION

The ML4961 combines Pulse Frequency Modulation (PFM) and synchronous rectification to create a boost converter that is both highly efficient and simple to use. A PFM regulator charges a single inductor for a fixed period of time and then completely discharges before another cycle begins, simplifying the design by eliminating the need for conventional current limiting circuitry. Synchronous rectification is accomplished by replacing an external Schottky diode with an on-chip PMOS device, reducing switching losses and external component count.

REGULATOR OPERATION

A block diagram of the boost converter is shown in Figure 2. The circuit remains idle when V_{OUT} is at or above the desired output voltage, drawing 45µA from V_{IN}, and 8µA from V_{OUT} through the feedback resistors R1 and R2. When V_{OUT} drops below the desired output level, the output of amplifier A1 goes high, signaling the regulator to deliver charge to the output. Since the output of amplifier A2 is normally high, the flip-flop captures the A1 set signal and creates a pulse at the gate of the NMOS transistor Q1. The NMOS transistor will charge the inductor L1 for 10µs, resulting in a peak current given by:

$$I_{L(PEAK)} = \frac{T_{ON} \times V_{IN}}{L1} \approx \frac{10\mu s \times V_{IN}}{L1} \qquad (1)$$

For reliable operation, L1 should be chosen so that $I_{L(PEAK)}$ does not exceed 2A.

When the one-shot times out, the NMOS FET releases the V_L pin, allowing the inductor to fly-back and momentarily charge the output through the body diode of PMOS transistor Q2. But, as the voltage across the PMOS transistor changes polarity, its gate will be driven low by the current sense amplifier A2, causing Q2 to short out its body diode. The inductor then discharges into the load through Q2. The output of A2 also serves to reset the flip-flop and one-shot in preparation for the next charging cycle. A2 releases the gate of Q2 when its current falls to zero. If V_{OUT} is still low, the flip-flop will immediately initiate another pulse. The output capacitor (C1) filters the inductor current, limiting output voltage ripple. Inductor current and one-shot waveforms are shown in Figure 3.

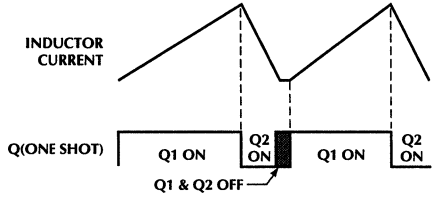


Figure 3. PFM Inductor Current Waveforms and Timing.

$\overline{\text{RESET}}$ COMPARATOR

An additional comparator is provided to detect low V_{IN}, or any other error condition that is important to the user. The inverting input of the comparator is internally connected to V_{REF}, while the non-inverting input is provided externally at the DETECT pin. The output of the comparator is the $\overline{\text{RESET}}$ pin, which swings from V_{OUT} to GND when an error is detected.

DESIGN CONSIDERATIONS

INDUCTOR

Selecting the proper inductor for a specific application usually involves a trade-off between efficiency and maximum output current. Choosing too high a value will keep the regulator from delivering the required output current under worst case conditions. Choosing too low a value causes efficiency to suffer. It is necessary to know the maximum required output current and the input voltage range to select the proper inductor value. The maximum inductor value can be estimated using the following formula:

$$L_{MAX} = \frac{V_{IN(MIN)}^{2} \times T_{ON(MIN)} \times \eta}{2 \times V_{OUT} \times I_{OUT(MAX)}} \qquad (2)$$

where η is the efficiency, typically between 0.8 and 0.9. Note that this is the value of inductance that just barely delivers the required output current under worst case conditions. A lower value may be required to cover inductor tolerance, the effect of lower peak inductor currents caused by resistive losses, and minimum dead time between pulses.

Another method of determining the appropriate inductor value is to make an estimate based on the typical performance curves given in Figures 4 and 5. Figure 4 shows maximum output current as a function of input voltage for several inductor values. These are typical performance curves and leave no margin for inductance and ON-time variations. To accommodate worst case conditions, it is necessary to derate these curves by at least 10% in addition to inductor tolerance. Interpolation between the different curves will give a reasonable starting point for an inductor value.

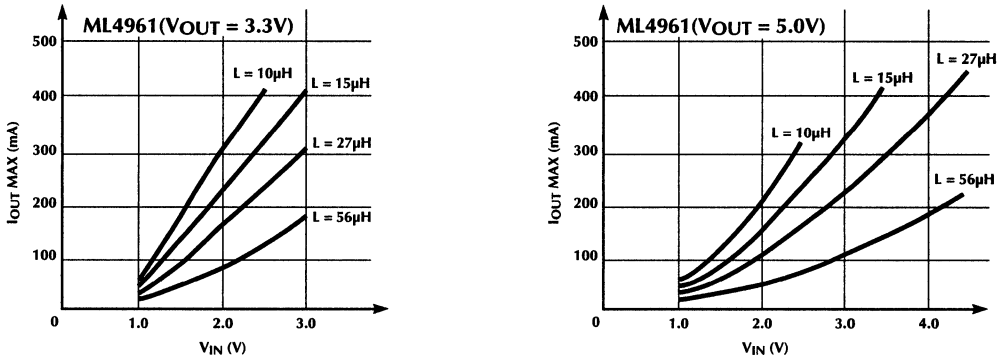


Figure 4. Output Current vs. Input Voltage.

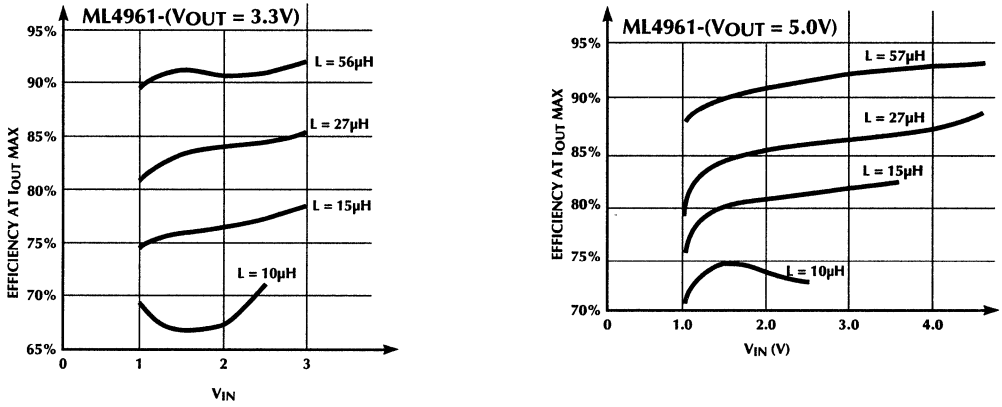


Figure 5. Typical Efficiency as a Function of V_{IN}.

Figure 5 shows efficiency under the conditions used to create Figure 4. It can be seen that efficiency is mostly independent of input voltage and is closely related to inductor value. This illustrates the need to keep the inductor value as high as possible to attain peak system efficiency. As the inductor value goes down to 10µH, the efficiency drops to between 70% and 75%. With 56µH, the efficiency exceeds 90% and there is little room for improvement. At values greater than 100µH, the operation of the synchronous rectifier becomes unreliable because the inductor current is so small that it is difficult for the control circuitry to detect.

After the appropriate inductor value is chosen, it is necessary to find the minimum inductor current rating required. Peak inductor current is determined from the following formula:

$$I_{L(PEAK)} = \frac{T_{ON(MAX)} \times V_{IN(MAX)}}{L_{MIN}} \qquad (3)$$

When comparing various inductors, it is important to keep in mind that suppliers use different criteria to determine their ratings. Many use a conservative current level, where inductance has dropped to 90% of its normal level. In any case, it is a good idea to try inductors of various current ratings with the ML4961 to determine which inductor is the best choice. Check efficiency and maximum output current, and if a current probe is available, look at the inductor current to see if it looks like the waveform shown in Figure 3. For additional information, see Application Note 29.

Suitable inductors can be purchased from the following suppliers:

Coilcraft	(708) 639-6400
Coiltronics	(407) 241-7876
Dale	(605) 665-9301
Sumida	(708) 956-0666

OUTPUT CAPACITOR

The choice of output capacitor is also important, as it controls the output ripple and optimizes the efficiency of the circuit. Output ripple is influenced by three capacitor parameters: capacitance, ESR, and ESL. The contribution due to capacitance can be determined by looking at the change in capacitor voltage required to store the energy delivered by the inductor in a single charge-discharge cycle, as determined by the following formula:

$$\Delta V_{OUT} = \frac{T_{ON}^2 \times V_{IN}^2}{2 \times L \times C \times (V_{OUT} - V_{IN})} \quad (4)$$

For a 2.4V input, and 5V output, a 27µH inductor, and a 47µF capacitor, the expected output ripple due to capacitor value is 87mV.

Capacitor Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL), also contribute to the output ripple due to the inductor discharge current waveform. Just after the NMOS transistor turns off, the output current ramps quickly to match the peak inductor current. This fast change in current through the output capacitor's ESL causes a high frequency (5ns) spike that can be over 1V in magnitude. After the ESL spike settles, the output voltage still has a ripple component equal to the inductor discharge current times the ESR. This component will have a sawtooth shape and a peak value equal to the peak inductor current times the ESR. ESR also has a negative effect on efficiency by contributing I-squared R losses during the discharge cycle.

An output capacitor with a capacitance of 100µF, an ESR of less than 0.1Ω, and an ESL of less than 5nH is a good general purpose choice. Tantalum capacitors which meet these requirements can be obtained from the following suppliers:

Matsuo	(714) 969-2491
Sprague	(603) 224-1961

If ESL spikes are causing output noise problems, an EMI filter can be added in series with the output.

INPUT CAPACITOR

Unless the input source is a very low impedance battery, it will be necessary to decouple the input with a capacitor with a value of between 47µF and 100µF. This provides the benefits of preventing input ripple from affecting the ML4961 control circuitry, and it also improves efficiency by reducing I-squared R losses during the charge and discharge cycles of the inductor. Again, a low ESR capacitor (such as tantalum) is recommended.

SETTING THE OUTPUT VOLTAGE

The adjustable output can be set to any voltage between 2.5V and 6V by connecting a resistor divider to the SENSE pin as shown in the block diagram. The resistor values R_1 and R_2 can be calculated using the following equation:

$$V_{OUT} = 0.2 \times \frac{(R_1 + R_2)}{R_2} \quad (5)$$

The value of R_2 should be 40kΩ or less to minimize bias current errors. R_1 is then found by rearranging the equation:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{0.2} - 1 \right) \quad (6)$$

It is important to note that the accuracy of these resistors directly affects the accuracy of the output voltage. The SENSE pin threshold variation is ±3%, and the tolerances of R_1 and R_2 will add to this to determine the total output variation.

In some applications, input noise may cause output ripple to become excessive due to "pulse grouping", where the charge-discharge pulses are not evenly spaced in time. In such cases it may be necessary to add a small 20pF to 100pF ceramic feedforward capacitor (C_{FF}) from the V_{IN} pin to the SENSE pin.

SETTING THE $\overline{\text{RESET}}$ THRESHOLD

To use the $\overline{\text{RESET}}$ comparator as an input voltage monitor, it is necessary to use an external resistor divider tied to the DETECT pin as shown in the block diagram. The resistor values R_A and R_B can be calculated using the following equation:

$$V_{IN(MIN)} = 0.2 \times \frac{(R_A + R_B)}{R_B} \quad (7)$$

The value of R_B should be 100kΩ or less to minimize bias current errors. R_A is then found by rearranging the equation:

$$R_A = R_B \times \left(\frac{V_{IN(MIN)}}{0.2} - 1 \right) \quad (8)$$

LAYOUT

Good PC board layout practices will ensure the proper operation of the ML4961. Important layout considerations include:

- Use adequate ground and power traces or planes
- Keep components as close as possible to the ML4961
- Use short trace lengths from the inductor to the V_L pin and from the output capacitor to the V_{OUT} pin
- Use a single point ground for the ML4961 ground pins, and the input and output capacitors

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4961CS	0°C to +70°C	8-Pin SOIC (S08)
ML4961ES	–20°C to +70°C	8-Pin SOIC (S08)
ML4961IS	–40°C to +85°C	8-Pin SOIC (S08)

Quality and Reliability

Section 8

Quality and Reliability

Micro Linear is dedicated to excellence in its people and products. By adopting a policy of continuous improvement, we pledge to provide defect free products and services which meet or exceed our customer's expectation.

TOTAL QUALITY MANAGEMENT (TQM)

TQM is an operating methodology focused on continuous improvement of employees, products, manufacturing techniques and services to achieve our mission "100% Quality, 100% On Time" for our customers. The meaning of the word Customer at Micro Linear starts from within the company.

Under the TQM philosophy, quality is built into every step of the manufacturing process from design to product qualification; from receiving to shipping. The TQM program at Micro Linear Corporation is a detailed program involving engineering and manufacturing to achieve the highest quality linear integrated circuits available.

QUALITY SYSTEM

The system is design to meet the requirements of:

- ISO 9002 Quality Systems, Model for Quality Assurance in Production and Installation
- MIL-STD-883 Test Methods and Procedures for Microelectronics
- MIL-I-38535 Appendix A Integrated Circuits (Microcircuits) Manufacturing, General Specification
- MIL-M-38510 Microcircuits, General Specification for (superseded by MIL- I-38535, Appendix A)
- MIL-Q-9858 Quality Program Requirements
- MIL-STD-45662 Calibration System Requirements
- MIL-I-45208 Inspection System Requirements
- MIL-STD-105 Sampling Procedures and Tables for Inspection by Attributes
- Other requirements from customers

INTERNAL QUALITY AUDITS

The internal quality audit system requirements are according to procedure as defined in ISO 9000. It ensures that production and quality activities comply with established procedures, and regularly measures the effectiveness of the quality system. Internal quality audits are scheduled on the basis of the status and importance of the activity to be audited, and the result of the audits is recorded and brought to the attention of the functional manager of the area audited. Follow-up audit activities are performed to verify the implementation and effectiveness of the corrective action taken.

The audit areas include Calibration, Fab, Assembly, Test, Receiving Inspection, Document Control, Shipping Inspection, Finished Goods, MPC, Contract Review, Purchasing, ESD, Particle Counts.

CORRECTIVE ACTION COMMITTEE (CAC)

The Corrective Action Committee (CAC) is comprised of representatives from Manufacturing, Process Engineering, Product Engineering, and Quality and Reliability at a minimum who is responsible for assuring that the corrective and preventive actions are implemented. The vehicles for defining the corrective and preventive actions at Micro Linear are:

- Discrepant Material Report (DMR) generated when non conformance occurs on material at any manufacturing operation.
- Customer Material Return (CMR) generated when material is returned for nonconformance occurring in shipped material.
- Corrective Action Request (CAR) generated when any employee sees a need for corrective action to take place or to document customer complaints.

MANAGEMENT REVIEW

The whole quality system is review at least once a year by the quality department to ensure continuing compliance to the requirements mentioned above.

Management reviews the Quality Indices reports as well as the Corrective Actions reports against Micro Linear's goals and objectives every quarter. The Quality Indices report includes Return Rate, AOQ Electrical and Mechanical, Reliability Data by process, Process Capabilities (Cpk) of critical parameters from each wafer fabrication facility and assembly, Vendor Lot Rejection Rate for each subcontractor, Visual Defect Density of each Foundry, and the Internal Quality Audit performance. The Corrective Actions report summarizes the corrective and preventive actions taken from DMRs, CMRs, and CARs.

DOCUMENT CONTROL

All company documents for procedures, specifications, drawings, travelers, flow charts, schematics, etc. that define customer requirements, raw material requirements, design, manufacture, and testing of products are controlled by a Document Control organization within the Micro Linear's Quality Department.

SUPPLIER CONTROL

Control of the quality of the incoming material is critical to the success of Micro Linear. Under the TQM philosophy, Micro Linear has an audit program of its suppliers of Class 1 material defined by those directly associated with the final products. Such audit is carried out on a defined frequency and performed by both manufacturing and quality personnel. Information gathered from the audit is reviewed with the supplier to incorporate programs to improve the quality of the material provided to Micro Linear.

PRODUCT IDENTIFICATION AND TRACEABILITY

All units are marked with unique lot numbers. These lot numbers provide complete traceability all the way to wafer fab as well as assembly and test.

Micro Linear considers traceability to be essential for good engineering control and additional insurance for its customers.

PROCESS CONTROL

All critical process nodes as well as test yield data are closely monitored and analyzed using statistical tools and techniques such as process capability (Cpk), Trend Chart, Paretto Analysis, etc. The data is also used for verifying the effectiveness of the corrective actions and to help focusing on areas that needs improvement under the TQM philosophy of continuous improvement.

MAJOR CHANGE NOTIFICATION

Micro Linear reviews all process, product, and package changes. All changes with possible impact are submitted for re-qualification which may include electrical, mechanical, and/or thermal characterization, in accordance to Micro Linear's Reliability program. The system is in place to notify customers with test data in accordance with MIL-M-38510.

RELIABILITY PROGRAM

Micro Linear's Reliability Program consistent with those of other semiconductor manufacturers utilizes various accelerated life tests as tools for establishing reliability status and progress. These tests are undertaken to identify infant mortality and wear-out failure mechanisms for specific or generically similar device families.

Micro Linear's Reliability program has three components: Qualification, Quality Conformance and Reliability Audit. Each design/process technology set, each wafer fabrication facility, and each assembly location by package type is initially qualified. Periodic re-evaluation (Quality Conformance Testing) is performed, thereafter, to evaluate the on-going reliability of product and processes. In addition, Micro Linear has the third component Reliability Audit named ACT (Advanced Conformance Testing) to ensure the reliability of products shipped to customers. ACT defines auditing of samples from each process and wafer fab facility and subjecting them to an accelerated life testing. Plan for each program is summarized below:

PROGRAM	PLAN
Qualification Testing	
• New Product	see Table 1
• Design/Process Set	see Table 2
• Wafer Fabrication Facility	**PLAN**
• Assembly Location	see Table 3
• Major Change	**PLAN**
Quality Conformance Testing	Every six month
• Wafer Fabrication Facility by Design/Process Set	see Table 1
• Assembly by Package	see Table 3
Advance Conformance Testing (ACT)	Every month
• Wafer Fabrication Facility by Design/Process Set	see Table 4

Note: "PLAN" are the appropriate stresses and tests determined by a qualification committee.

TESTING AND CALIBRATION

Micro Linear has invested in the latest "state-of-the-art" analog testers to achieve the most complete and thorough parametric testing of integrated circuits in the industry. Data sheets provide the customer a precise listing of parameters which are 100% tested.

The calibration system is in compliance with MIL-STD-45662 Calibration Systems Requirements.

CUSTOMER RETURNS

A formal program exists to record, analyze and take appropriate action on all returns. The customer is shortly notified with the initial test result. When needed, a report is generated and sent to the customer stating our findings and corrective actions to prevent re-occurrence.

ESD (ELECTRO STATIC DISCHARGE)

All semiconductor devices are sensitive to Electro Static Discharge (ESD) to some degree. For this reason a very strict control on handling and packaging are observed through all the employees and facility areas that handle or test semiconductor devices.

Strong emphasis is put on the sensitivity of Micro Linear products to ESD, from design, lay-out and process perspectives. All the products are fully characterized to MIL-STD-883, Method 3015.

TABLE 1

STRESS/TEST	METHOD	CONDITION	QUANTITY
Life Test	Mil-Std-883 Method 1005	1000 hrs @ 125°C	77
ESD Characterization	Mil-Std-883 Method 3015	Human Body Model	min. 3

TABLE 2

STRESS/TEST	METHOD	CONDITION	QUANTITY
Life Test	Mil-Std-883 Method 1005	1000 hrs @ 125°C	77
HAST		50 hrs @ 130°C, 85%RH	45
Autoclave	QAP 36004	168 hrs @ 121°C, 15 psi	45
Temperature Cycling	Mil-Std-883 Method 1010	1000 cycles @ –55°C to +125°C	45
Thermal Shock	Mil-Std-883 Method 1011	200 cycles @ –55°C to +125°C	45
High Temperature Storage	Mil-Std-883 Method 1010	1000 hrs @ 150°C	45

TABLE 3

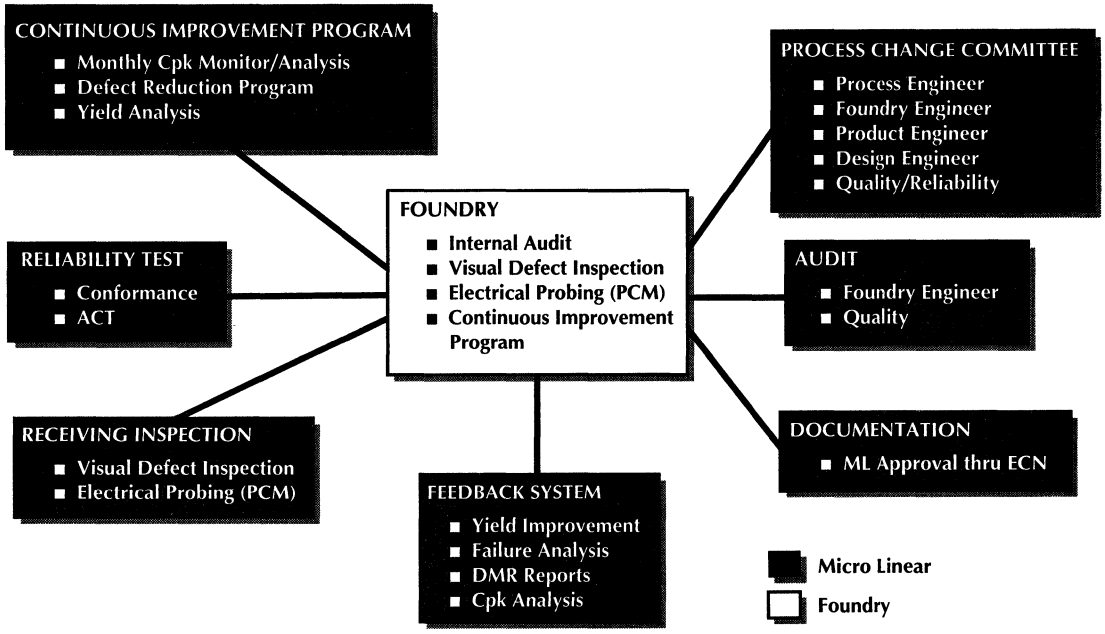
STRESS/TEST	METHOD	CONDITION	QUANTITY
Life Test	Mil-Std-883 Method 1005	1000 hrs @ 125°C	77
HAST		50 hrs @ 130°C, 85%RH	45
Autoclave (*)	QAP 36004	168 hrs @ 121°C, 15 psi	45
Temperature Cycling	Mil-Std-883 Method 1010	1000 cycles @ –55°C to +125°C	45
Thermal Shock (*)	Mil-Std-883 Method 1011	200 cycles @ –55°C to +125°C	45
High Temperature Storage	Mil-Std-883 Method 1010	1000 hrs @ 150°C	45
Physical Dimensions	Mil-Std-883 Method 2016		15
Solderability	Mil-Std-883 Method 2003	22 leads	3
Resistance to Solder Heat	Mil-Std-750	260°C, 10 sec.	32
Resistance to Solvents	Mil-Std-883 Method 2015		4
External Visual Inspection	QAP 30038		15
Lead Integrity	Mil-Std-883 Method 2004		3

Note: (*) Qualification testing only.

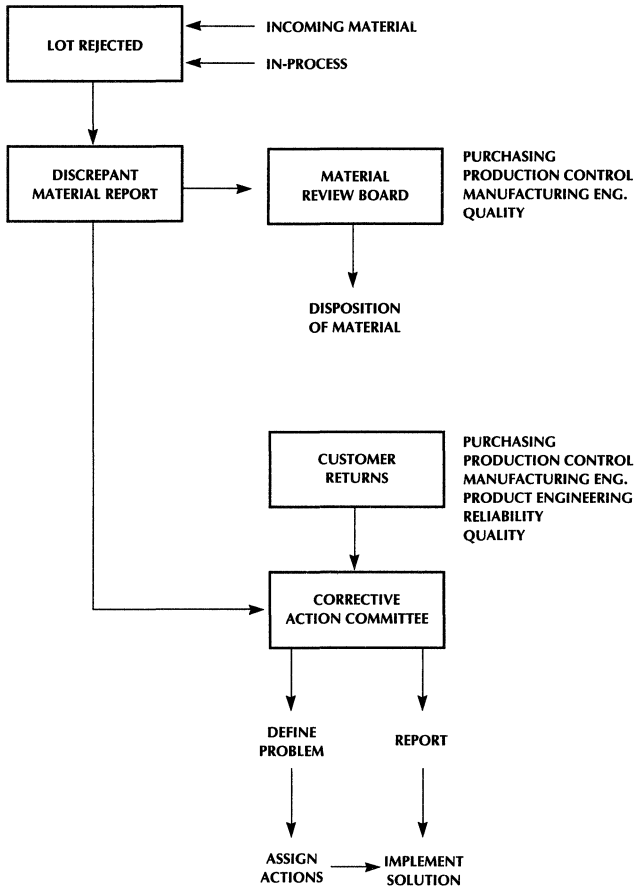
TABLE 4

STRESS/TEST	METHOD	CONDITION	QUANTITY
Burn-in Test	QAP 34004	48 hrs @ 125°C	125

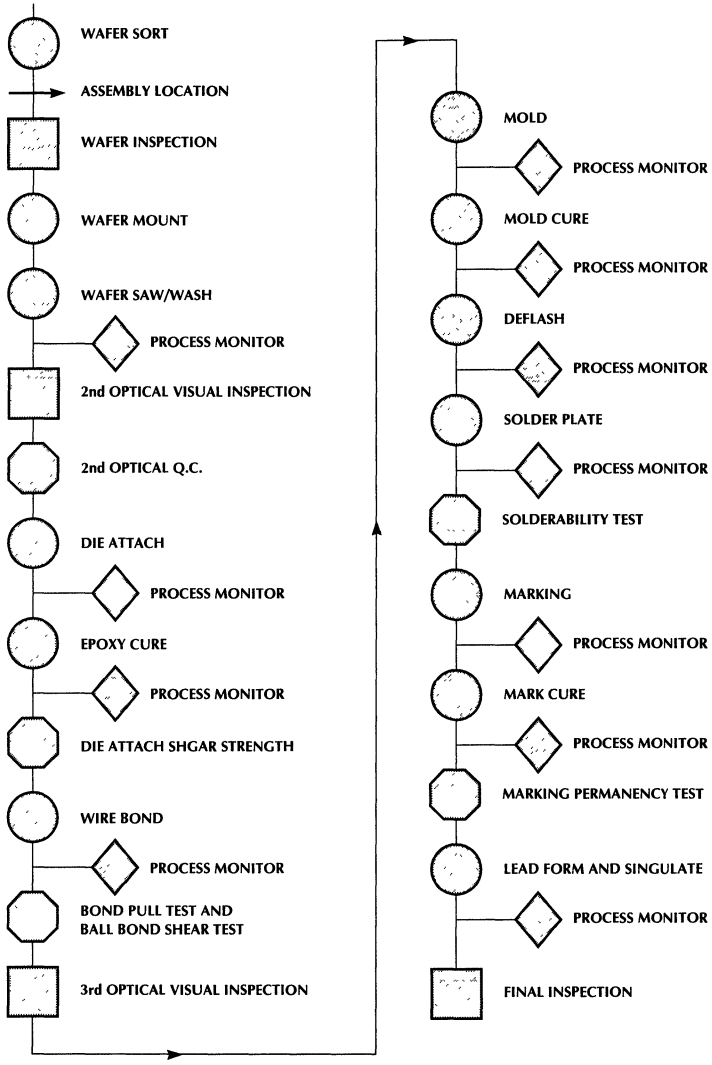
FOUNDRY CONTROL SYSTEM

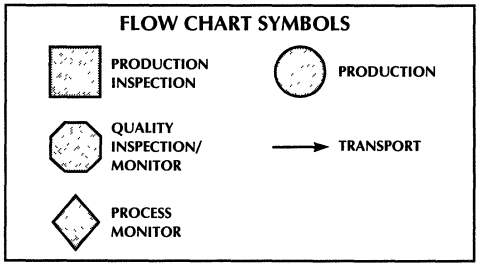


CORRECTIVE ACTION PROGRAM

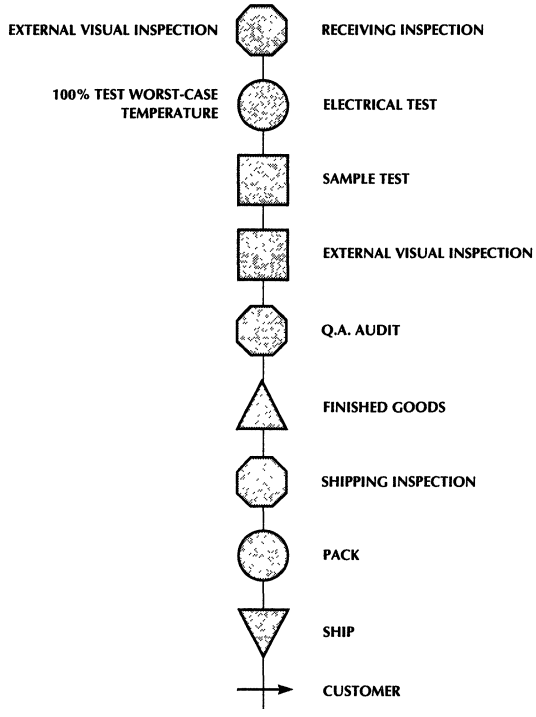


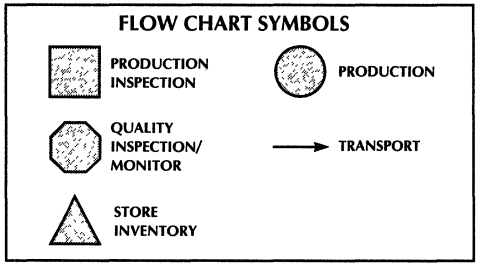
TYPICAL MOLDED PACKAGE ASSEMBLY FLOW





TYPICAL TEST FLOW





APPENDIX A: FAILURE RATE CALCULATIONS

In order to predict the rate at which product will fail, it is necessary to accelerate the life of the product. This is most commonly done by a temperature and/or voltage stress, a process known as burn-in. The equation for both stresses is exponential, hence large acceleration factors can be achieved. In our studies, only temperature was used in the acceleration equation; the devices were biased at nominal voltages. The equation is shown below. It is known as the Arrhenius Reaction Rate Equation, named for the man who modeled the relationship between temperature and the relationship between temperature and the chemical reaction property of materials.

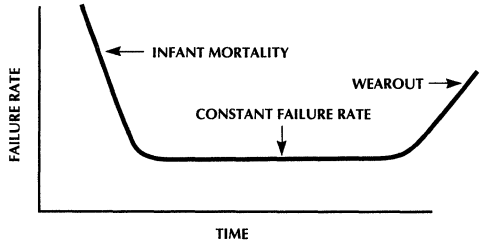
ARRHENIUS REACTION RATE EQUATION

$$Af = Exp\left[\frac{Ea}{K}\left(\frac{1}{T1} - \frac{1}{T2}\right)\right]$$

Af: Acceleration Factor
Ea: Activation Energy (in electron volts)
K: Boltzmanns Constant (8.62×10^{-5})
T1: Temperature of System Operation (°K)
T2: Temperature of Life Test (°K)

Burn-in when run for 1000 hours, is call "life test." Interim readouts normally occur at 168 and 500 hours. The hypothesis is that a "bathtub curve" will result. This curve, shown below, illustrates a device's failure rate versus time. Certain manufacturing defects have a tendency to cause failures early in the life of a device (infant mortality). The failure rate associated with these defects can be accelerated by applying stresses, such as temperature and voltage, which do not appreciably affect the normal failure rates or wear out mechanisms.

BATHTUB CURVE



ACTIVATION ENERGIES

In order to calculate the acceleration factor, the activation energies for various failure modes encountered in the semiconductor industry are required. Initially, failure modes are assumed based on industry experience. As failures occur, they are rigorously analyzed and the failure modes then used to determine which activation energies are appropriate for determining failure rates. The following table describes the most common failure modes and their activation energies.

Table 1.

FAILURE MECHANISM	Ea	STRESS
Oxide Defects	0.3eV	High Voltage Op Life
Contamination	1.0eV	High Voltage Bias
Silicon Defects	0.5eV	High Voltage
Metal Line Electromigration	0.5eV	High Voltage Op Life
Contact Electromigration	0.9eV	High Voltage Op Life
Masking Defects Assembly Defects	0.5eV	High Temperature Storage Op Life
Microcracks	N/A	Temperature Cycling
Short Channel Charge Trapping	-0.06eV	Low Voltage High Voltage Op Life

ACCELERATION FACTORS

Once the activating energy is determined for a given failure mechanism, the acceleration factor can be calculated using the Arrhenius equation. The following table lists some of the common activation energies and its associated acceleration factors between different ambient temperature.

Table 2.

Est. T_J Accelerated Temperature	Estimated T_J Typical application Temp.				Activation Energy (eV)
	25°C	40°C	55°C	70°C	
125°C	133	52	22	10	0.5
150°C	315	124	53	24	
125°C	941	255	78	26	0.7
150°C	3142	851	260	88	
125°C	6655	1241	270	67	0.9
150°C	31368	5852	1273	316	

FAILURE RATES

At Micro Linear, failure rates are generally stated at 60% confidence level using Chi square statistic per the following formula.

$$\lambda_{MAX} = \frac{\chi^2_{1-\alpha}[\text{with df} = 2(r+1)]}{2t}$$

where: λ_{MAX} = maximum failure rate
χ^2 = chi square distribution
r = number of failures
df = degree of freedom
t = total number of test hours
α = statistical error expected in estimate. For 60% confidence level, $\alpha = 0.4$ or $1-\alpha = 0.6$

Selected values of Chi Square distribution are listed in Table 3.

Table 3. Percentiles of the Chi Square Distribution. (Values of chi² corresponding to certain selected probabilities).

		60% CONFIDENCE LEVEL	90% CONFIDENCE LEVEL
PROBABILITY IN %		60.0	90.0
1–α		0.60	0.90
df	TOTAL FAILURES		
1		0.708	2.71
2	0	1.830	4.61
3		2.950	6.25
4	1	4.040	7.78
5		5.130	9.24
6	2	6.210	10.60
7		7.280	12.00
8	3	8.350	13.40
9		9.410	14.70
10	4	10.500	16.00
11		11.500	17.30
12	5	12.600	18.50
13		13.600	19.80
14	6	14.700	21.10
15		15.700	22.30
16	7	16.800	23.50
17		17.800	24.80
18	8	18.900	26.00
19		19.900	27.20
20	9	21.000	28.40

Failure rate may be expressed a number of ways. Table 4 compares various ways of expressing failure rates.

Table 4. Failure Rates

NO. OF FAILURES PER DEVICE HOURS	FAILURE RATE	% PER 1000 HOURS	PPM (HOURS)	FITS	MTBF (HOURS)
$1/1 \times 10^9$	0.000000001	0.0001	0.001	1	1×10^9
$1/1 \times 10^8$	0.00000001	0.001	0.01	10	1×10^8
$1/1 \times 10^7$	0.0000001	0.01	0.1	100	1×10^7
$1/1 \times 10^6$	0.000001	0.1	1	1000	1×10^6
$1/1 \times 10^5$	0.00001	1	10	10000	1×10^5
$1/1 \times 10^4$	0.0001	10	100	100000	1×10^4
$1/1 \times 10^3$	0.001	100	1000	1000000	1×10^3

APPENDIX B: RADIATION HARDNESS OF 12V BIPOLAR PROCESS

The Micro Linear 12V bipolar process has demonstrated selective hardness to radiation exposure. The components most commonly used in the 12V process which are described in table 1, were exposed up to 10^6 Rads total dose ionizing radiation. A second group of the same components were exposed to non-ionizing radiation of up to 10^{14} fluence neutrons/sq. cm. Neither group was exposed to both types of radiation.

DESCRIPTION	BIAS DURING IRRADIATION	POST IRRADIATION MEASUREMENTS	FIGURES
Minimum Geometry NPN	V_{CES} = 5V	Δh_{fe}	1, 4
Lateral Quad Collector PNP	V_{CES} = –5V	Δh_{fe}	2, 5
Vertical PNP	V_{CES} = –5V	Δh_{fe}	3, 6
45Ω N+ Resistor	No bias	ΔR	3, 6
850Ω P+ Resistor	No bias	ΔR	3, 6
10KΩ Implanted P Resistor	No bias	ΔR	3, 6
10pF Capacitor	No bias	ΔI_L	3, 6

Table 1. Components

Figures 1 through 3 show the results of the ionizing radiation tests. Figures 4 through 6 show the results of the non-ionizing radiation tests.

* The resistors and capacitors were not significantly altered by exposure to these radiation levels. They are not included in the figures.

SUMMARY

The h_{fe} of the NPN transistors degrade by approximately 50% at 10^5 Rads and 80% at 10^6 Rads. The PNPs degrade more severely by approximately 80% at 10^5 Rads and reach unity at 10^6 Rads. Degradation vs. neutron fluence is similar but less severe.

Micro Linear circuits, exclusively using NPN devices and passive components, can be designed to perform in a high radiation environment.

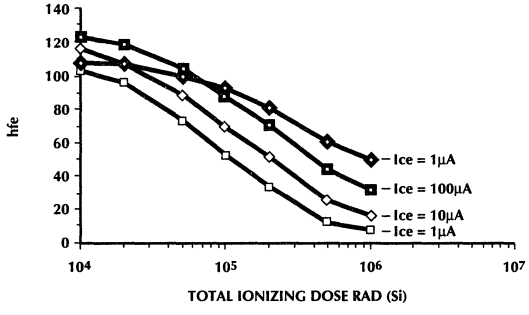


Figure 1.

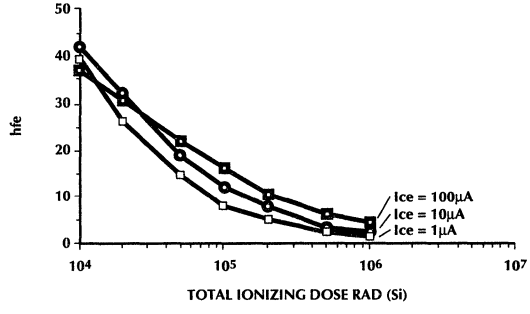


Figure 2.

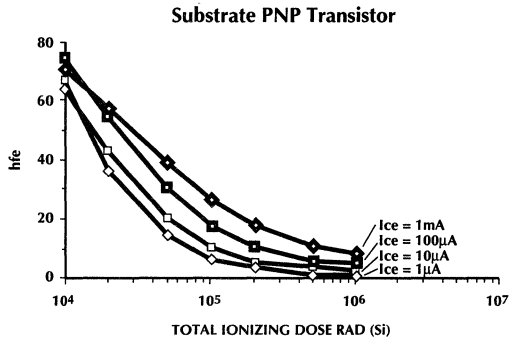


Figure 3.

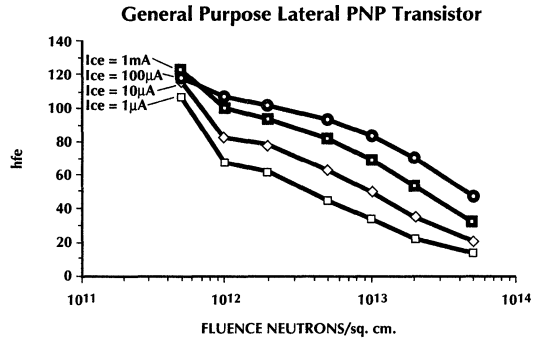


Figure 4.

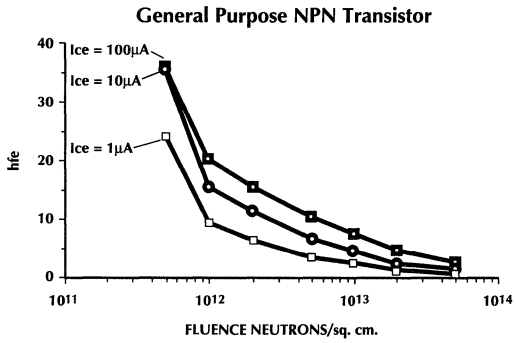


Figure 5.

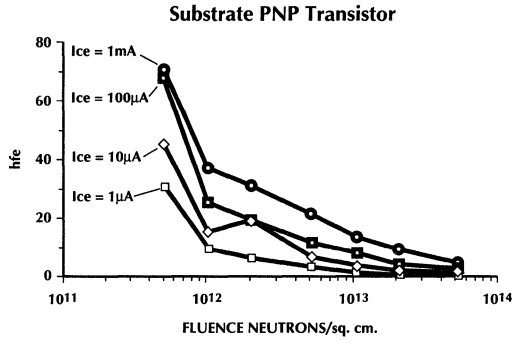


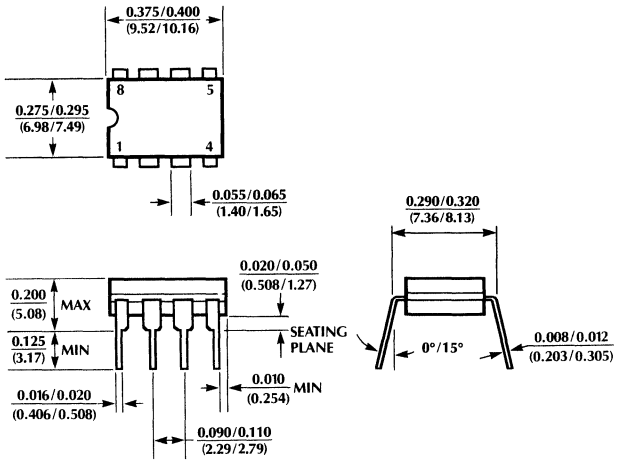
Figure 6.

Packaging Information

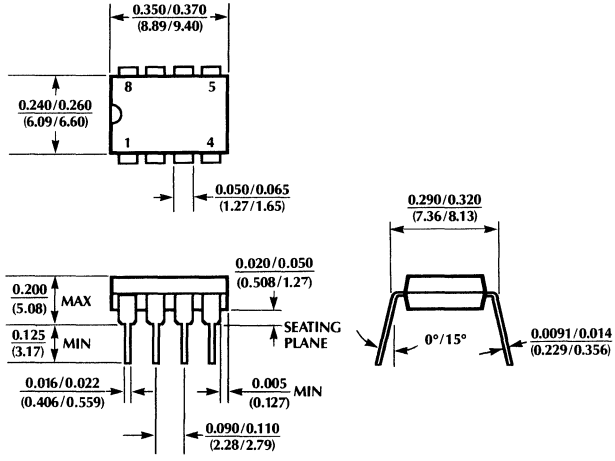
Section 9

Note 1: Dimensions are in inches/(millimeters).
Note 2: Coplanarity not to exceed 0.005" (0.127mm) for all surface mount packages.
Note 3: Bent leads for all surface mount packages not to exceed 0.005" (0.127mm) from its true position
Note 4: Bent leads for all PDIP and CDIP packages not to exceed 0.010" (0.254mm) from their true position.

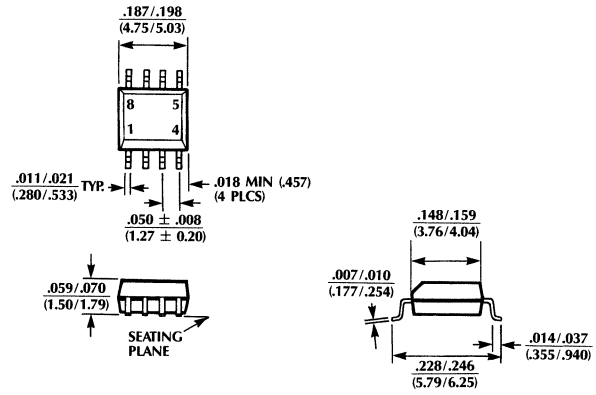
Package: J08
8-Pin Hermetic DIP (CERDIP)



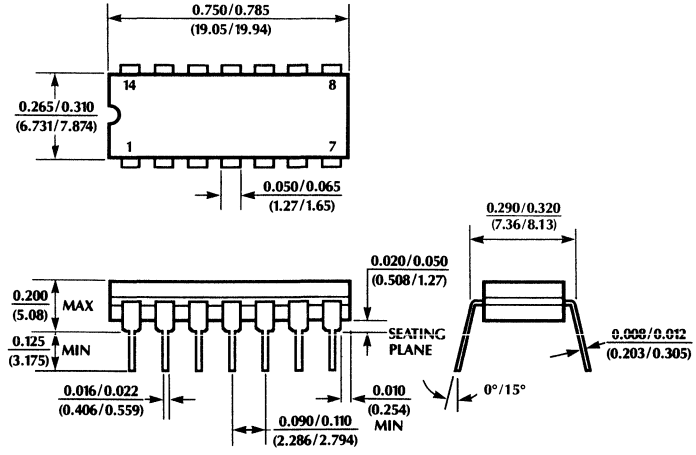
Package: P08
8-Pin Molded DIP



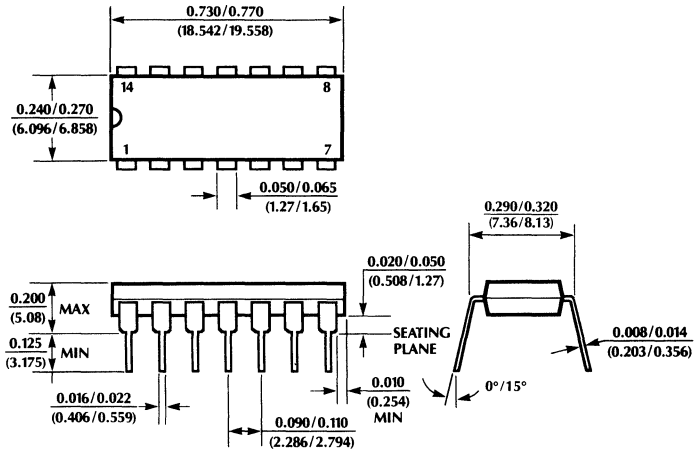
Package: S08N
8-Pin SOIC (Narrow)



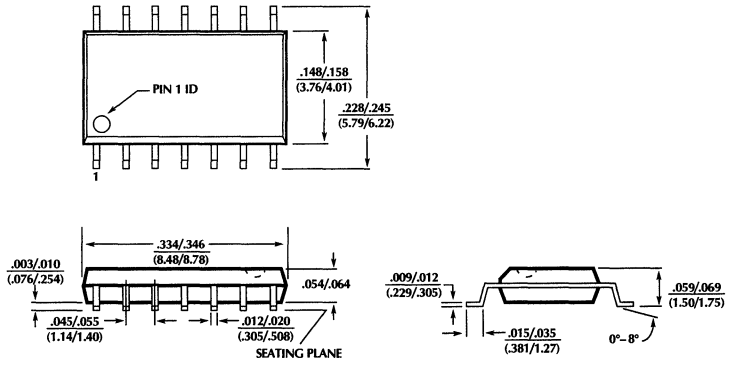
Package: J14
14-Pin Hermetic DIP (CERDIP)



Package: P14
14-Pin Molded DIP

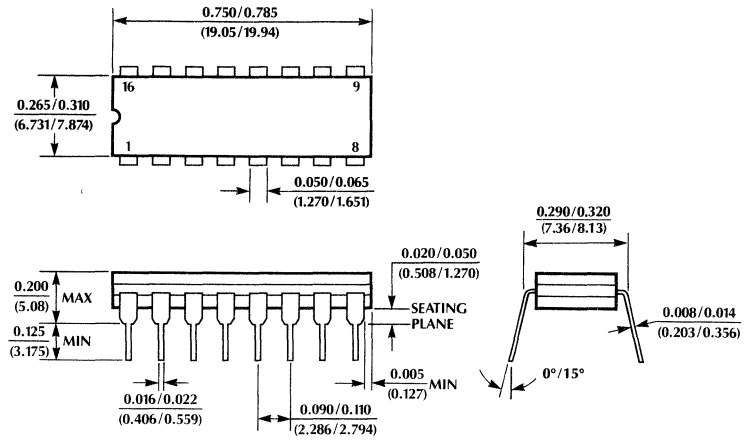


Package: S14N
14-Pin SOIC (Narrow)

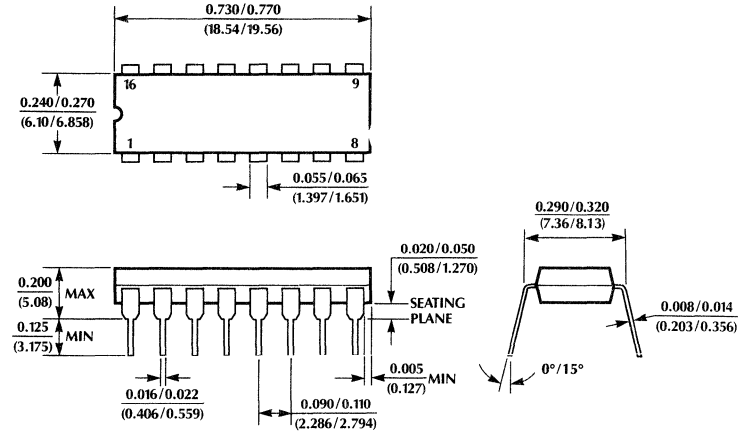


9

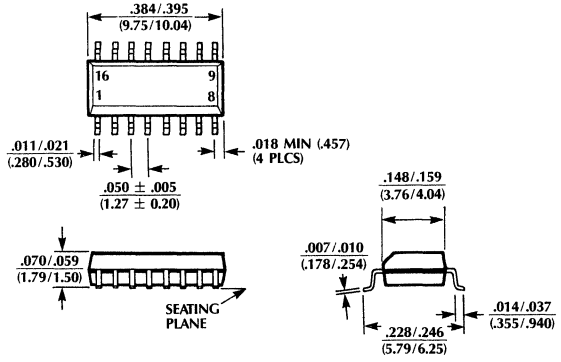
Package: J16
16-Pin Hermetic DIP (CERDIP)



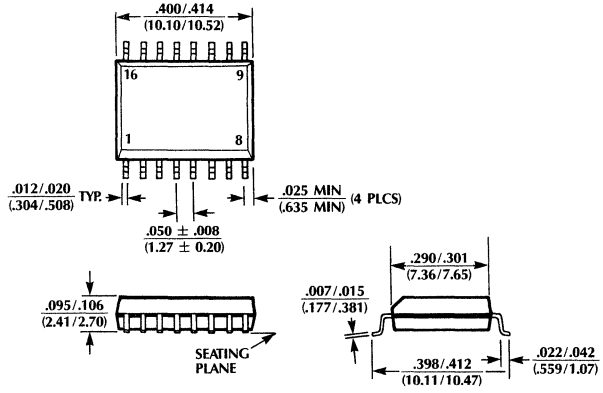
Package: P16
16-Pin Molded DIP



Package: S16N
16-Pin SOIC (Narrow)

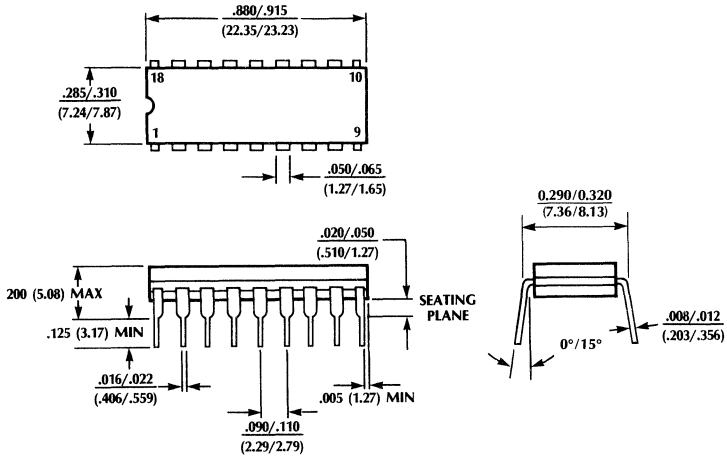


Package: S16W
16-Pin SOIC (Wide)

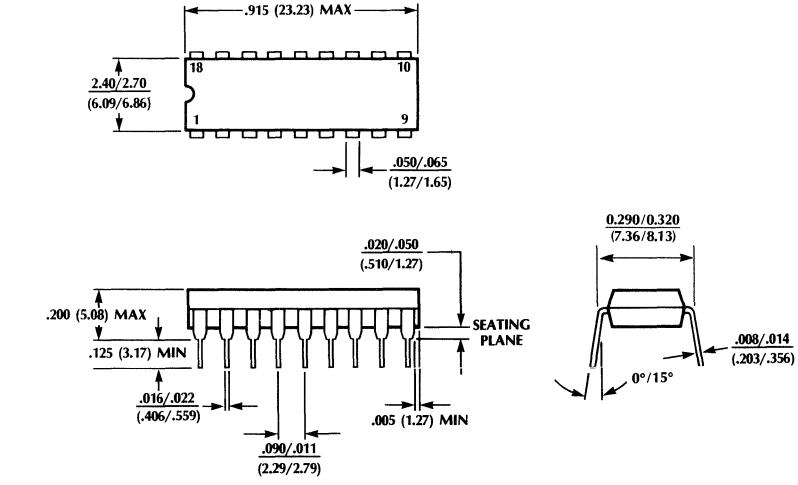


9

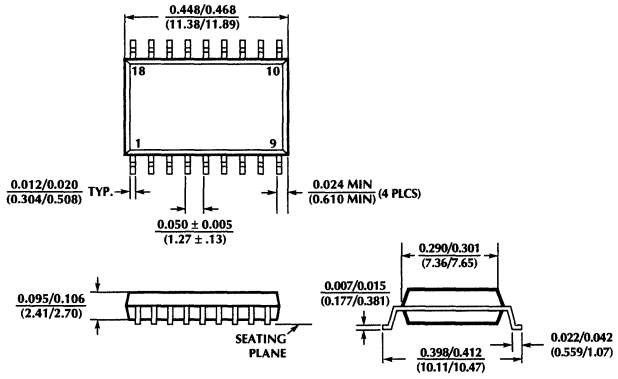
Package: J18
18-Pin Hermetic DIP (CERDIP)



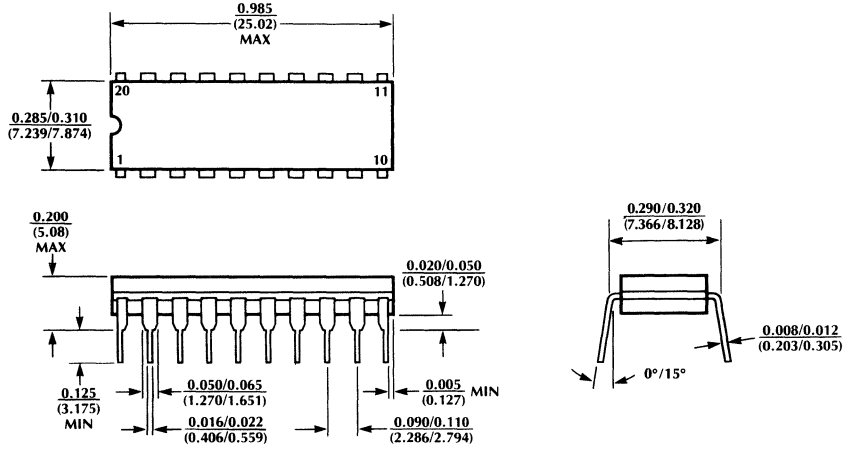
Package: P18
18-Pin Molded DIP



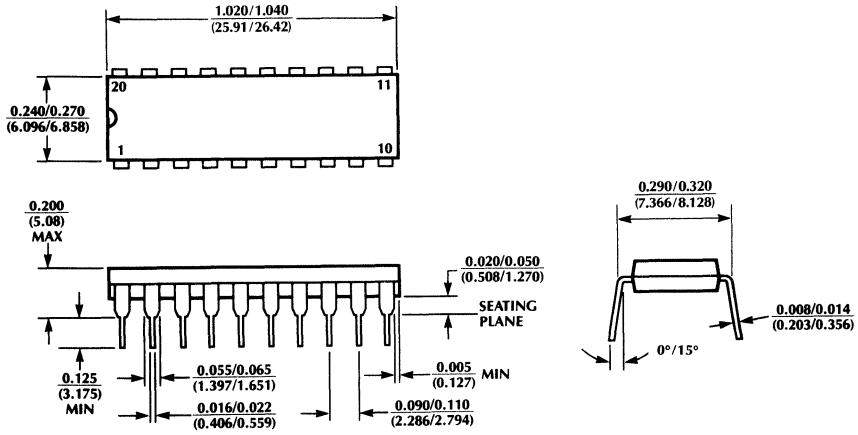
Package: S18W
18-Pin SOIC (Wide)



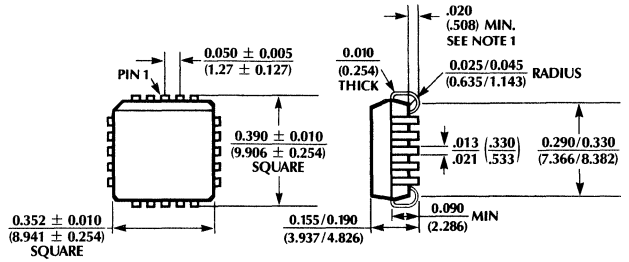
Package: J20
20-Pin Hermetic DIP (CERDIP)



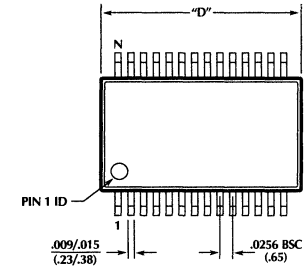
Package: P20
20-Pin Molded DIP



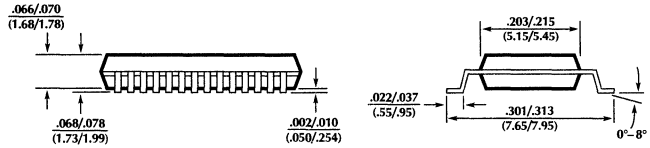
Package: Q20
20-Pin Molded Leaded PCC



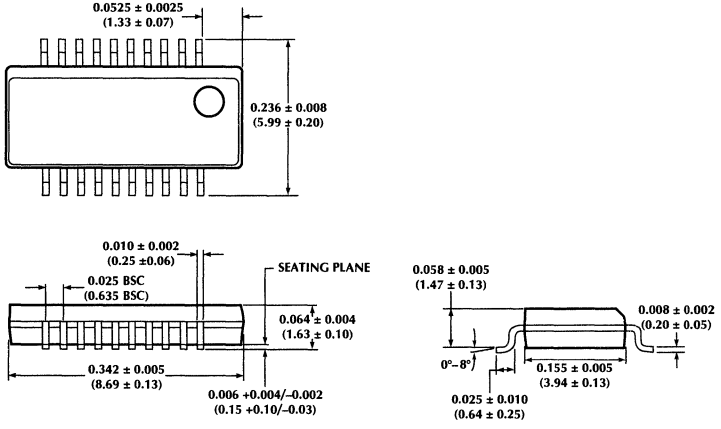
Package: R20, R24, R28
20-Pin SSOP, 24-Pin SSOP, 28-Pin SSOP



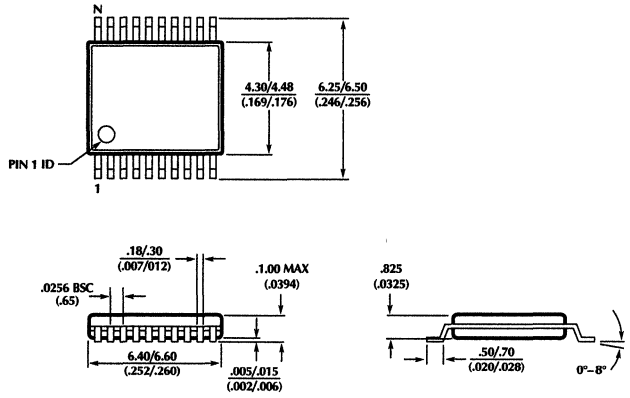
"N" LEADS	DIM. "D" inches	(mm)	PACKAGE I.D.
20	.274/.294	(6.95/7.45)	R20
24	.313/.333	(7.95/8.45)	R24
28	.392/.412	(9.95/10.45)	R28



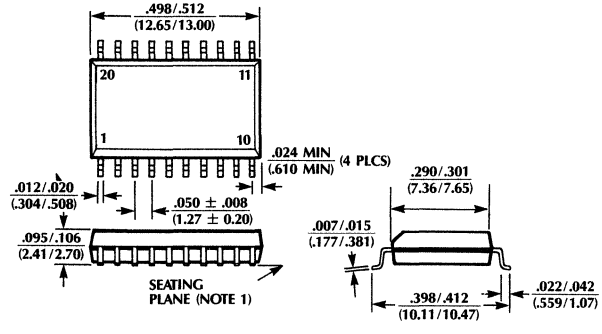
Package: K20
20-Pin QSOP



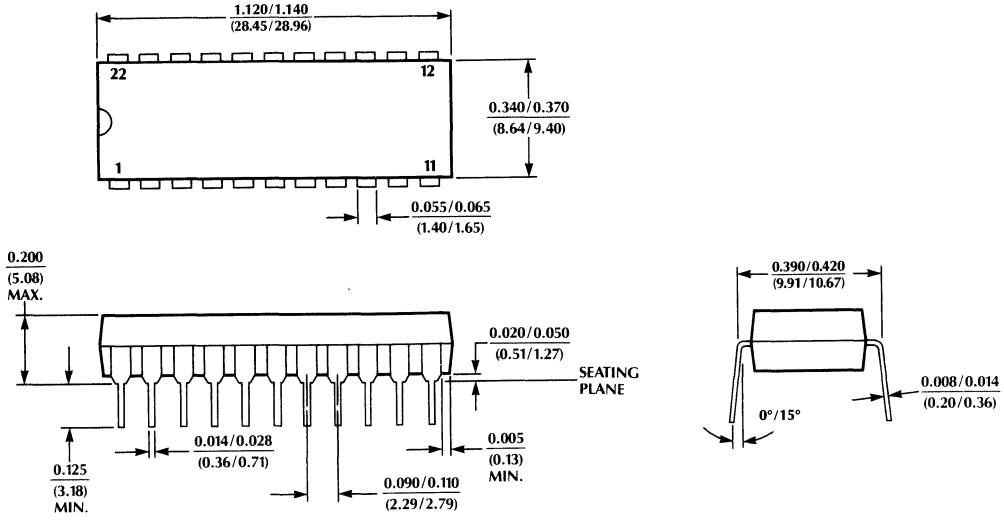
Package: T20
20-Pin TSSOP



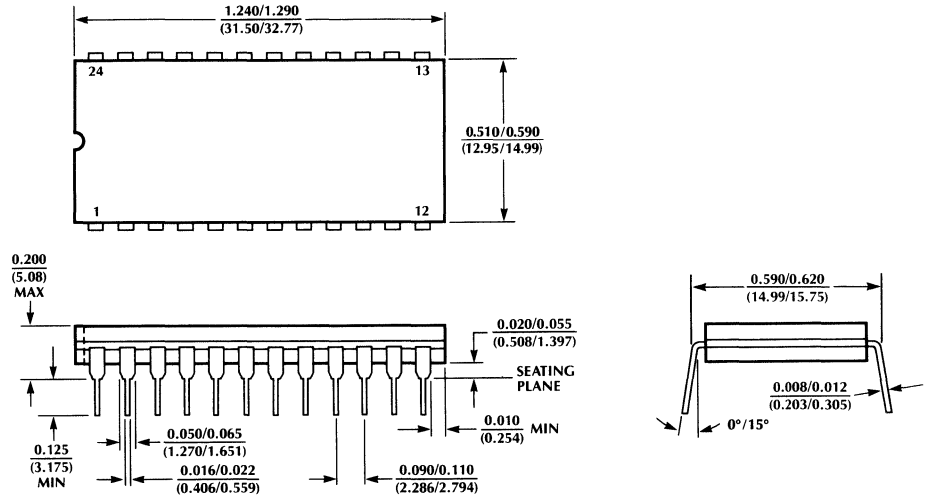
Package: S20W
20-Pin SOIC



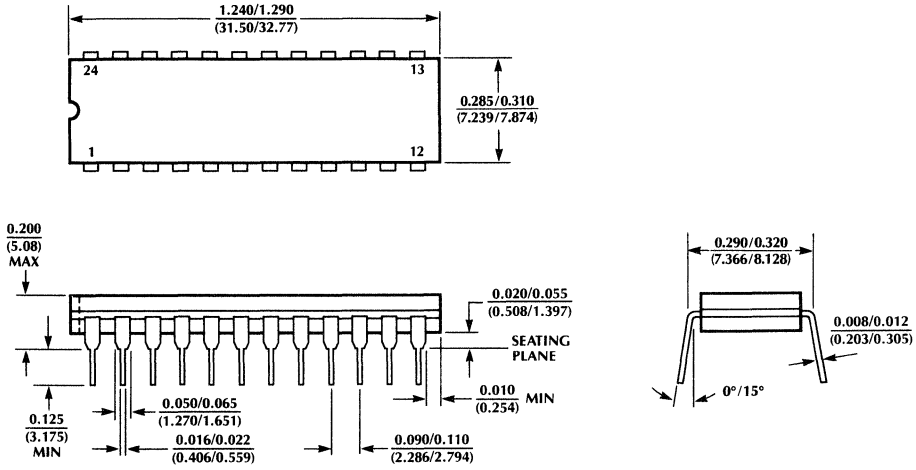
Package: P22
22-Pin Molded DIP



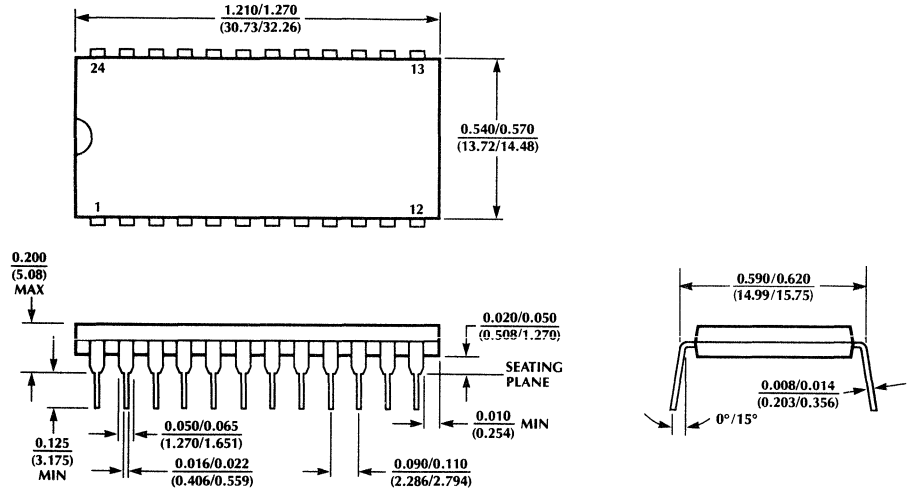
Package: J24W
24-Pin Hermetic DIP (CERDIP)



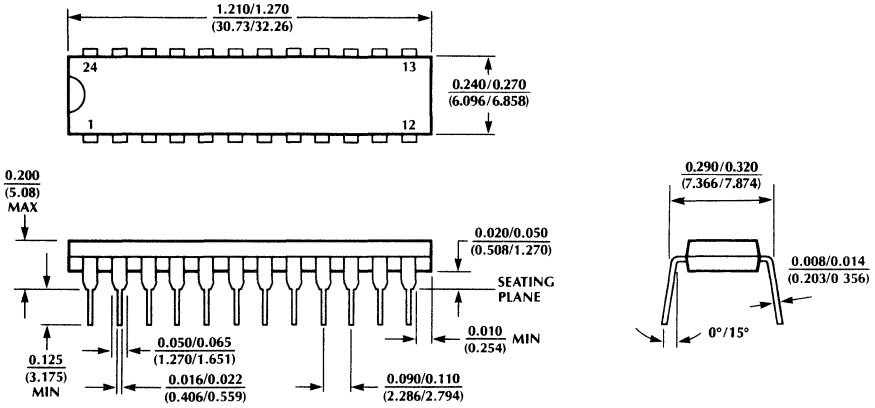
Package: J24N
24-Pin Hermetic Ceramic DIP (Narrow)



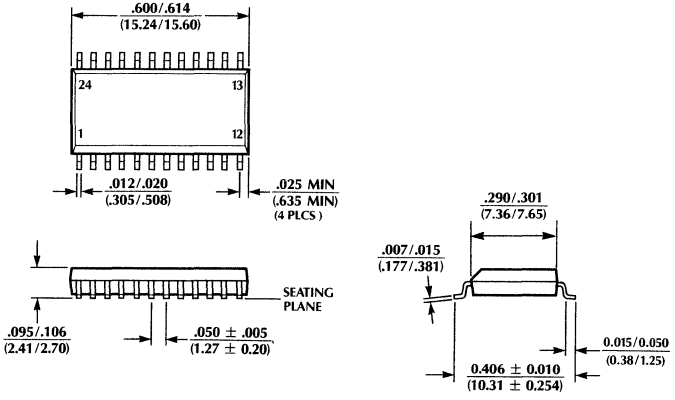
Package: P24W
24-Pin Molded DIP (Wide)



Package: P24N
24-Pin Molded DIP (Narrow)

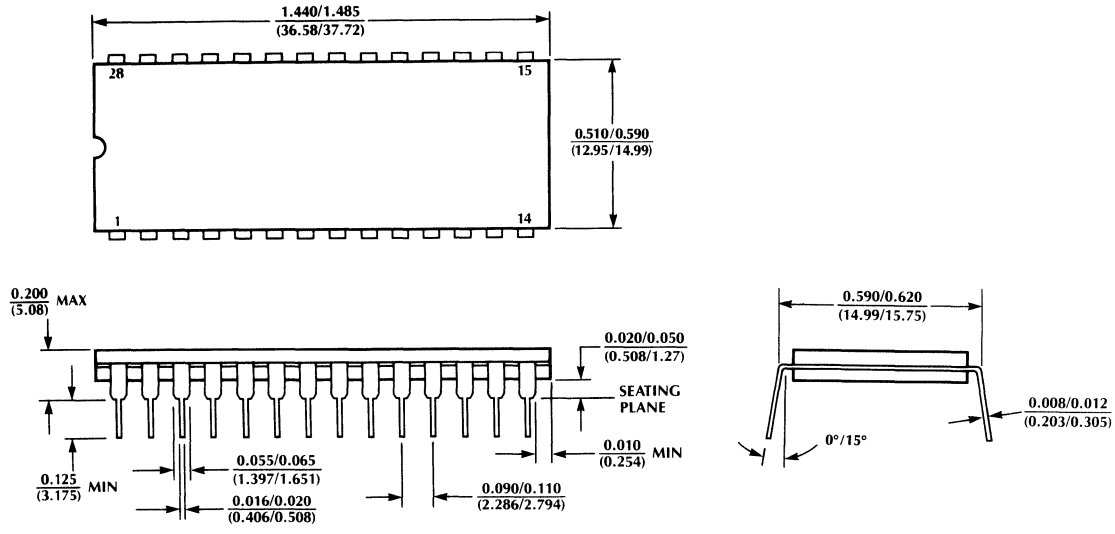


Package: S24W
24-Pin SOIC

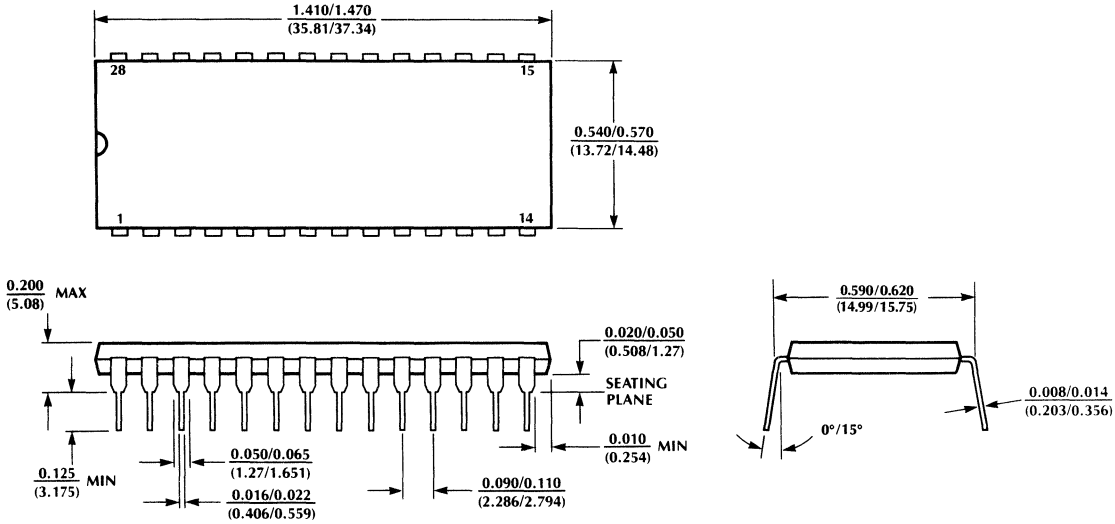


9

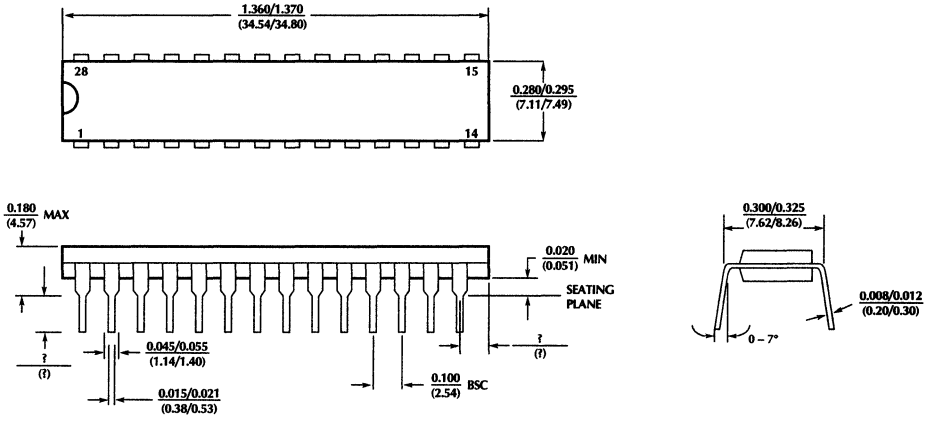
Package: J28W
28-Pin Hermetic DIP (CREDIP)



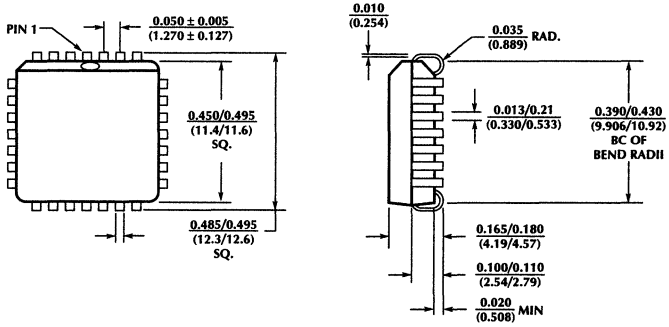
Package: P28W
28-Pin Molded DIP



Package: P28N
28-Pin Molded DIP (Narrow)

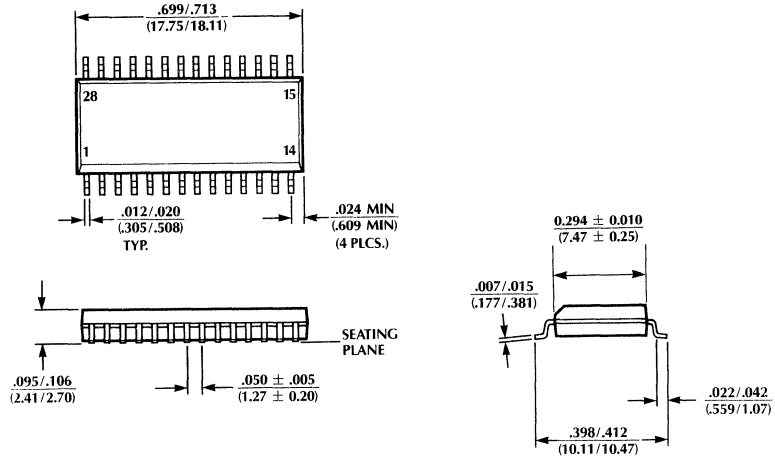


Package: Q28
28-Pin Molded Leaded PCC

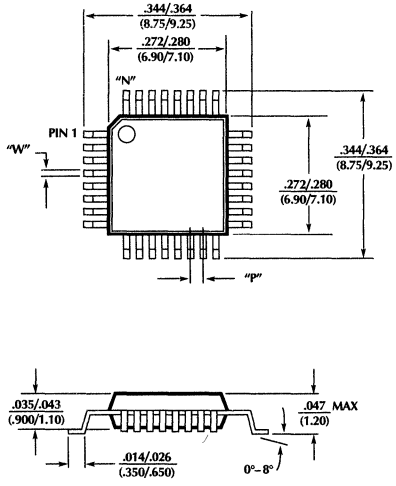


9

Package: S28W
28-Pin SOIC

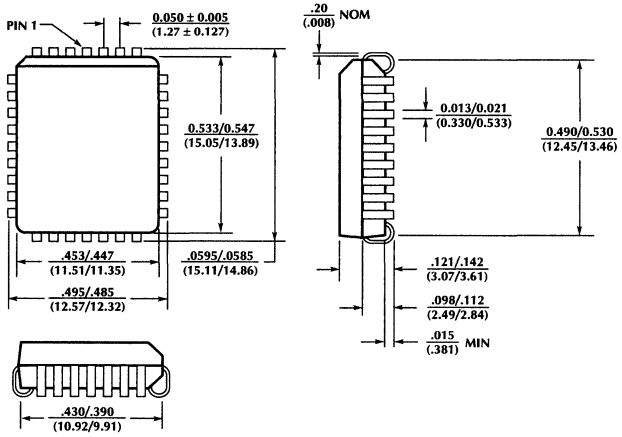


Package: H32, H48
32-Pin TQFP, 48-Pin TQFP

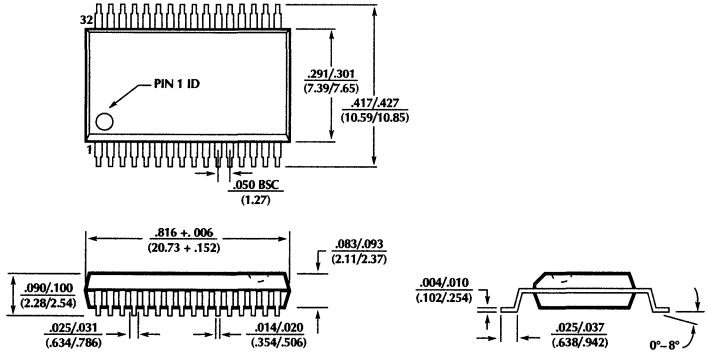


"N"	32L	48L
"P"	.315 BASIC (.80)	.0197 BASIC (.50)
"W"	.009/.015 (.23/.38)	.008/.012 (.20/.30)
PACKAGE ID	H32	H48

Package: Q32
32-Pin Molded Leaded PCC

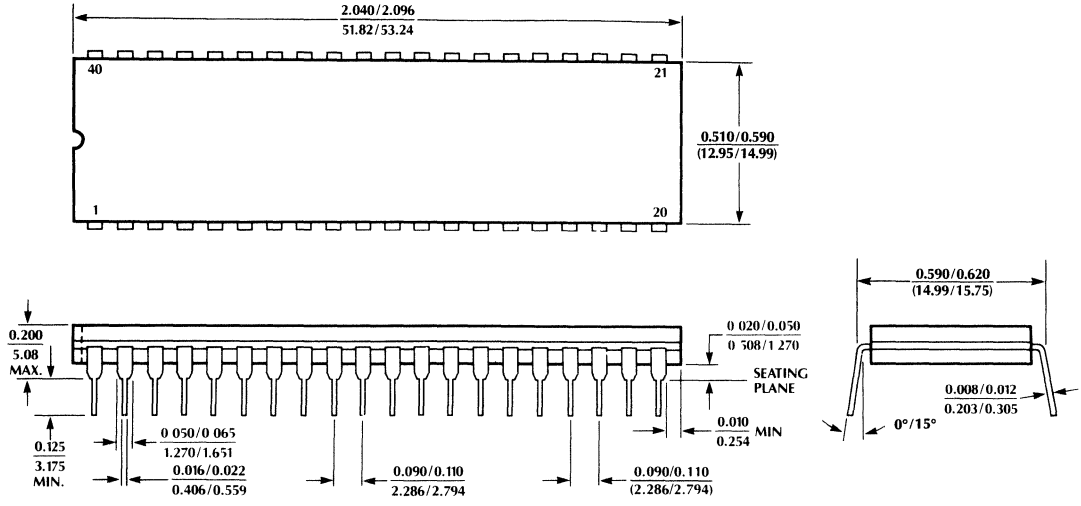


Package: S32W
32-Pin SOIC

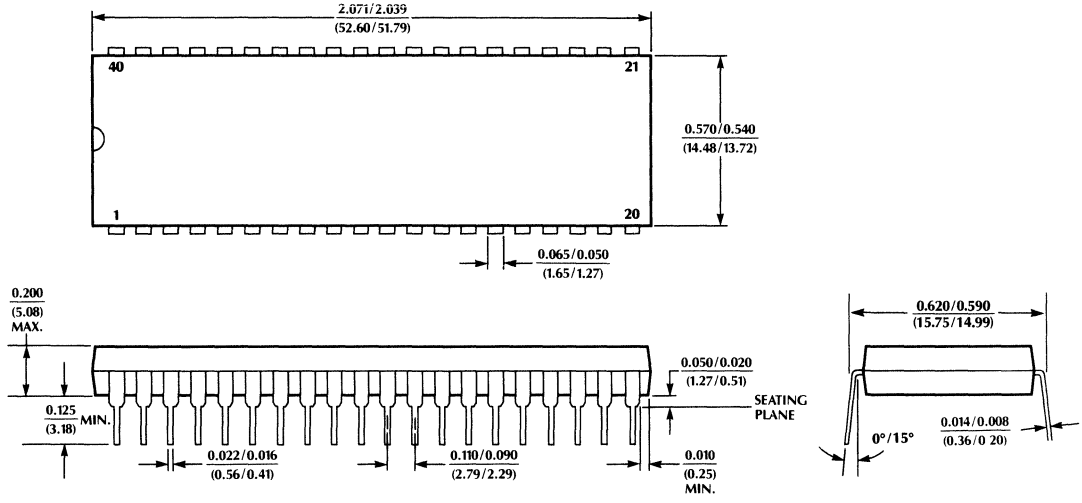


9

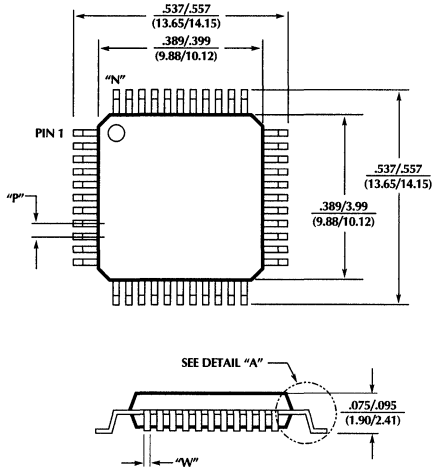
Package: J40
40-Pin Hermetic DIP (CERDIP)



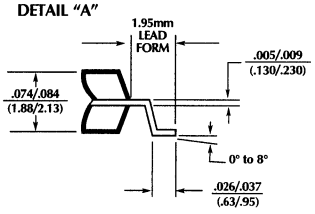
Package: P40
40-Pin Molded Plastic DIP



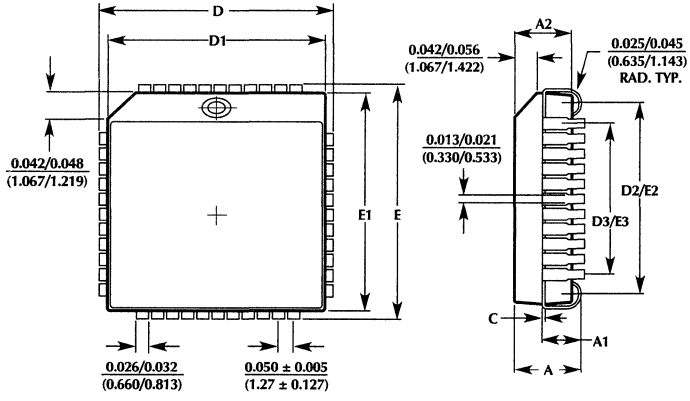
Package: G44, G52
44-Pin PQFP, 52-Pin PQFP



"N"	44L		52L	
"P"	.0315	(.80) BSC	.0265	(.65) BSC
"W"	.012/.018	(.30/.45)	.090/.014	(.22/.35)
PACKAGE ID	G44		G52	

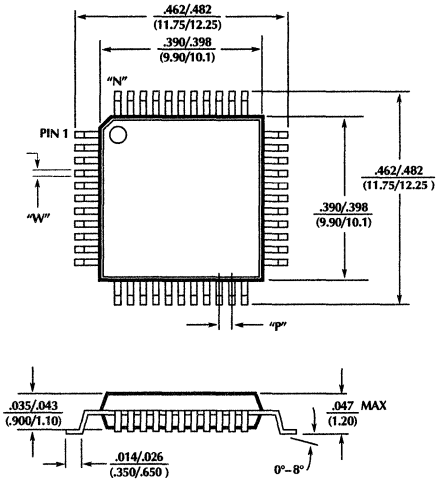


Package: Q44, Q52, Q68, Q84
44-Pin, 52-Pin, 68-Pin and 84-Pin Molded Leaded PCC



Lead Count	44L	52L	68L	84L
A	0.165/0.180 (4.191/4.572)	0.165/0.180 (4 191/4.572)	0.165/0.180 (4.191/4.572)	0.165/0.180 (4.191/4.572)
A1	0.100/0.110 (2.540/2.794)	0.100/0.110 (2.540/2.794)	0.095/0.118 (2.413/2.997)	0.095/0.118 (2.413/2.997)
A2	0.148/0.156 (3.759/3.962)	0.148/0.156 (3.759/3.962)	0.146/0.154 (3.708/3.911)	0.146/0.154 (3.708/3.911)
D	0.685/0.695 (17.39/17.65)	0.785/0.795 (19.94/20.19)	0.985/0.995 (25.02/25.27)	1.185/1.195 (30.09/30.35)
D1	0.650/0.654 (16.51/16.61)	0.750/0.754 (19.05/19.15)	0.950/0.954 (24.13/24.23)	1.150/1.154 (29.21/29.31)
D2	0.590/0.630 (14.99/16.00)	0.690/0.730 (17.53/18.54)	0.890/0.930 (22.61/23.62)	1.090/1.130 (27.69/28.70)
D3	0.500 REF (12.70 REF)	0.600 REF (15.24 REF)	0.800 REF (20.32 REF)	1.00 REF (25.40 REF)
E	0.685/0.695 (17.39/17.65)	0.785/0.795 (19.94/20.19)	0.985/0.995 (25.02/25.27)	1.185/1.195 (30.09/30.35)
E1	0.650/0.654 (16.51/16.61)	0.750/0.754 (19.05/19.15)	0.950/0.954 (24.13/24.23)	1.150/1.154 (29.21/29.31)
E2	0.590/0.630 (14.99/16.00)	0.690/0.730 (17.53/18.54)	0.890/0.930 (22.61/23.62)	1.090/1.130 (27.69/28.70)
E3	0.500 REF (12.70 REF)	0.600 REF (15.24 REF)	0.800 REF (20.32 REF)	1.00 REF (25.40 REF)
C	0.009/0.0103 (0.228/0.261)	0.009/0.0103 (0.228/0.261)	0.007/0.008 (0.178/0.203)	0.007/0.008 (0.178/0.203)
PACKAGE ID	Q44	Q52	Q68	Q84

Package: H44, H52, H64
44-Pin, 52-Pin and 64-Pin TQFP



"N"	44L	52L	64L
"P"	.80 BASIC (.0315)	.65 BASIC (.0256)	.50 BASIC (.0197)
"W"	.18/.32 (.007/.013)	.23/.37 (.009/.015)	.18/.32 (.007/.013)
PACKAGE ID	H44	H52	H64

G527 GE/CP 30K 295

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