ML501, ML501R, ML502, ML502R, ML502S–Series

6, 7, or 8-Channel Read/Write Circuits

GENERAL DESCRIPTION

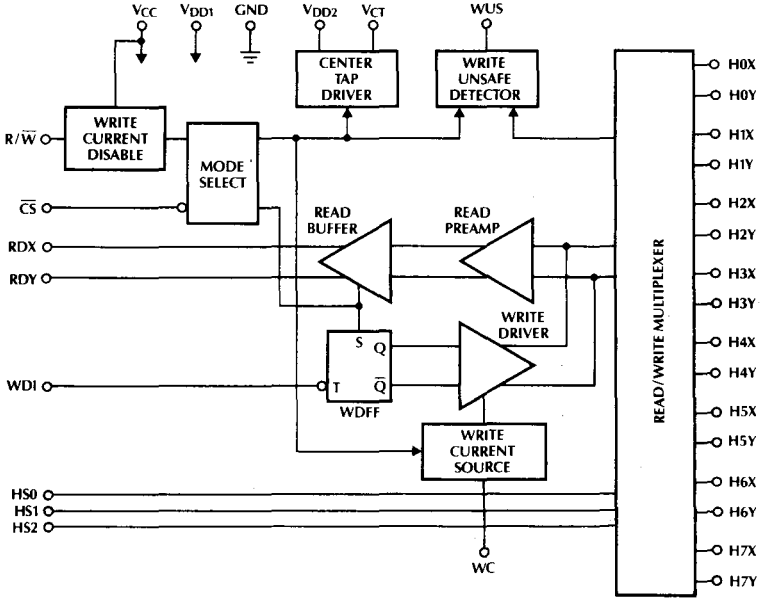
The ML501, ML502 family of devices are bipolar monolithic read/write circuits designed for use with fixed disk center-tapped recording heads. The ML501 and ML501R are designed for use with ferrite recording heads while the ML502, ML502R and ML502S are designed for thin film or composite heads. The R and S designation in the part number indicate that these parts have internal head damping resistors.

The ML501, ML502 family provides up to eight multiplexed read/write data channels. These circuits exhibit features not found in similar read/write circuits such as improved write current stability and the elimination of write current "glitches" during power-up. The exclusive ML502 is identical to the ML501 except that the write unsafe detect circuitry is designed to operate with lower head inductance.

FEATURES

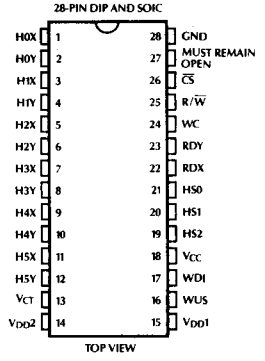
- Exclusive write current disable during power-up
- Enhanced write current stability
- ML501, ML501R is replacement for SSI 32R501/501R and is designed for center-tapped ferrite heads
- ML502, ML502R, and ML502S are designed for center-tapped thin film or composite heads
- Single or multi-platter Winchester drives
- Easily multiplexed for larger systems
- Available in 6, 7 or 8 channels
- TTL compatible control signals
- Programmable write current source
- Includes write unsafe detection
- Available in a selection of packages
- +5V, +12V power supplies

BLOCK DIAGRAM

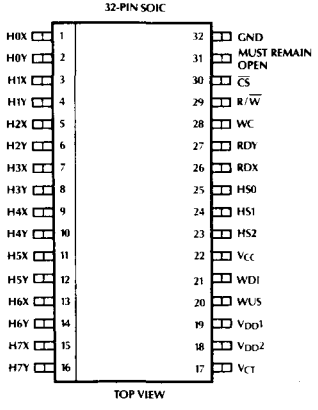


PIN CONNECTIONS

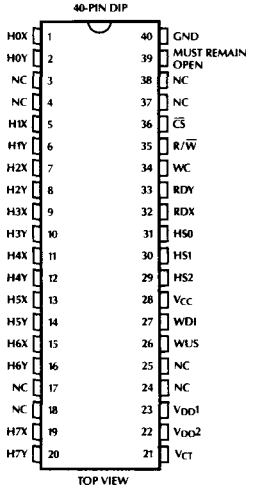
ML501-6 OR ML501R-6 OR ML502-6 OR ML502R-6 6 Channels



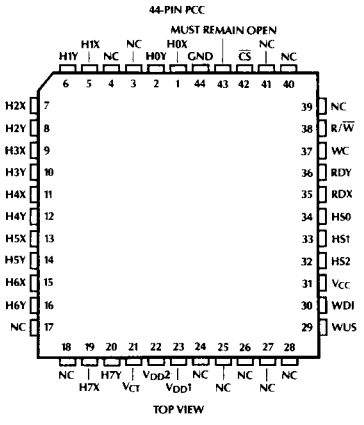
ML501-8 OR ML501R-8 OR ML502-8 OR ML502R-8 8 Channels



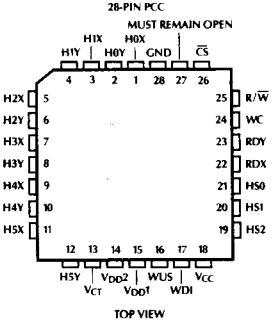
ML501-8 OR ML501R-8 OR ML502-8 OR ML502R-8 8 Channels



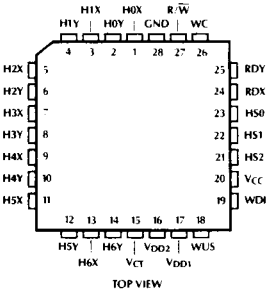
ML501-8 OR ML501R-8 OR ML502-8 OR ML502R-8 OR ML502S-8 8 Channels



ML501-6 OR ML501R-6 OR ML502-6 OR ML502R-6 OR ML502S-6 6 Channels



ML502S-7CQ ML502R-7CQ



PIN DESCRIPTION

NAME	FUNCTION
HS0–HS2	Head Select (eight heads)
$\overline{CS}$	Chip Select (low level enables chip)
R/$\overline{W}$	Read/Write (high level selects Read mode)
WUS	Write Unsafe, open collecter output (high level indicates an unsafe writing condition)
WDI	Write Data In (negative transition toggles head current direction)
H0X–H7X	X head connections
H0Y–H7Y	Y head connections

NAME	FUNCTION
RDX, RDY	X, Y Read Data (differential read signal out)
WC	Write Current (used to set the write current magnitude)
V_{CT}	Voltage Center Tap (center tap voltage source)
V_{CC}	+5 volts
$V_{DD}1$	+12 volts
$V_{DD}2$	Positive supply for center tap
GND	Ground

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- $V_{DD}1$ ..... −0.3 to 14 V_{DC}
- $V_{DD}2$ ..... −0.3 to 14 V_{DC}
- V_{CC} ..... −0.3 to 6 V_{DC}

Input Voltage Range
- Digital Inputs ($\overline{CS}$, R/$\overline{W}$, HS, WDI) ..... −0.3 to V_{CC} +0.3 V_{DC}
- Head Ports (H0X–H7X, H0Y–H7Y .... −0.3 to $V_{DD}1$ +0.3 V_{DC}
- Write Unsafe (WUS) ..... −0.3 to 14 V_{DC}

Write Current (I_W) ..... 60 mA

Output Current
- Read Data (RDX, RDY) ..... −10 mA
- Center Tap Current (I_{CT}) ..... −60 mA
- Write Unsafe (WUS) ..... 12 mA

Storage Temperature ..... −65°C to 150°C

Junction Temperature (T_J) ..... 135°C

Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Supply Voltage
- $V_{DD}1$ ..... 12 V ± 10%
- V_{CC} ..... 5 V ± 10%

Head Inductance
- L_H, ML501 or ML501R only ..... 5 to 15 µH
- L_H, ML502, ML502R, ML502S only ..... 400 to 1000 nH

Damping Resistor (R_D, ML501 only) ..... 500 to 2000 Ω

RCT Resistor (1/2 Watt) ..... 120 Ω ± 5%

Write Current (I_W) ..... 22 to 50 mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $V_{DD}1 = 12\,V \pm 10\%$, $V_{CC} = 5\,V \pm 10\%$, $R_{CT} = 120\,\Omega \pm 5\%$, $I_W = 45\,mA$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC OPERATING CHARACTERISTICS						
POWER SUPPLY						
I_{CC}	V_{CC} Supply Current	Read or Idle Mode			25	mA
		Write Mode			25	mA
I_{DD}	V_{DD} Supply Current	Read Mode			48	mA
		Write Mode			$25 + I_W$	mA
		Idle Mode			20	mA
P_D	Power Dissipation	Read Mode			770	mW
		Write Mode $I_W = 50\,mA$			830	mW
		Write Mode $I_W = 50\,mA$, $R_{CT} = 0\,\Omega$			1125	mW
		Idle Mode			400	mW
DIGITAL INPUTS ($\overline{CS}$, R/$\overline{W}$, HS, WDI)						
V_{IH}	High Voltage		2			V_{DC}
V_{IL}	Low Voltage				0.8	V_{DC}
I_{IH}	High Current	$V_{IH} = 2.0\,V$			100	µA
I_{IL}	Low Current	$V_{IL} = 0.8\,V$	−0.4			mA
WUS OUTPUT						
V_{OL}	Output Low Voltage	$I_{OL} = 8\,mA$ (Safe)			0.5	V_{DC}
I_{OH}	Output High Current	$V_{OH} = 5\,V$ (Unsafe)			100	µA
CENTER TAP VOLTAGES						
V_{CT}	Read Mode	Read Mode		4		V_{DC}
V_{CT}	Write Mode	Write Mode		6		V_{DC}

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ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 45mA$, $L_H = 10\mu H$ (ML501, ML501R), $L_H = 600nH$ (ML502, ML502R, ML502S), $R_D = 750\Omega$ (ML501), $f_{DATA} = 5MHz$, C_L (RDX, RDY) $\leq 20pF$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE CHARACTERISTICS						
I_{WR}	Write Current Range	$I_W = K/R_{WC}$	10		50	mA
K	Write Current Constant		129		151	V
V_{HD}	Differential Head Voltage Swing		7.5			V_{PK}
I_{HU}	Unselected Head Transient Current				2	mA_{PK}
C_{OD}	Differential Output Capacitance				15	pF
R_{OD}	Differential Output Resistance	ML501, ML502	10k			Ω
		$T_J = 25°C$ ML501R, ML502S/ML502R	560/180		940/300	Ω
f_{WDI}	WDI Transition Frequency	WUS = Low	250			kHz
A_I	I_{WC} to Head Current Gain			20		A/A
I_L	Unselected Head Leakage	Sum of X & Y Side Leakage Current			85	μA
READ MODE CHARACTERISTICS						
A_V	Differential Voltage Gain	$V_{IN} = 1mV_{P-P}$ @ 300kHz, R_L (RDX, RDY) = 1kΩ	90		120	V/V
DR	Dynamic Range	DC Input Voltage (V_I) Where Gain Falls 10%, $V_{IN} = V_I + 0.5mV_{P-P}$ @ 300kHz	−3		+3	mV
BW	Bandwidth (−3dB)	$\|Z_S\| < 5\Omega$, $V_{IN} = 1mV_{P-P}$	30			MHz
e_{IN}	Input Noise Voltage	BW = 15MHz, $L_H = 0$, $R_H = 0$			1.5	$nV/\sqrt{Hz}$
C_{IN}	Differential Input Capacitance	f = 5MHz			23	pF
R_{IN}	Differential Input Resistance	f = 5MHz, $T_J = 25°C$ ML501, ML502	2k			Ω
		$V_{IN} = 6mV_{P-P}$ ML501R, ML502S/ML502R	530/180		790/300	Ω
I_{IN}	Input Bias Current (1 side)				100	μA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V_{CT} + 100mV_{P-P}$ @ f = 5MHz	50			dB
PSRR	Power Supply Rejection Ratio	$100mV_{P-P}$ @ 5MHz on $V_{DD}1$, $V_{DD}2$, or V_{CC}	45			dB
CS	Channel Separation	Unselected Channels: $V_{IN} = 100mV_{P-P}$ @ 5MHz and Selected Channel: $V_{IN} = 0mV_{P-P}$	45			dB
V_{OS}	Output Offset Voltage		−480		+480	mV
V_{OCM}	Common-Mode Output Voltage	Read Mode	5		7	V
		Write or Idle Mode		4.3		V
R_{OUT}	Single-Ended Output Resistance	f = 5MHz			30	Ω
R_L	External Resistive Load (AC Coupled to Output)	Per Side to GND	100			Ω
I_L	Leakage Current, RDX, RDY	3V < (RDX, RDY) < 8V Write or Idle Mode	−50		50	μA
Z_O	Center Tap Output Impedance	0MHz ≤ f ≤ 5MHz			150	Ω
I_O	Output Current	AC Coupled Load, RDX to RDY	2			mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 45mA$, $L_H = 10\mu H$ (ML501, ML501R), $L_H = 600nH$ (ML502, ML502R, ML502S), $R_D = 750\Omega$ (ML501), $f_{DATA} = 5MHz$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_{RW}	R/$\overline{W}$ to Write Switching Delay	To 90% of Write Current Output			600	ns
t_{WR}	R/$\overline{W}$ to Read Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			600	ns
t_{IW} or t_{IR}	$\overline{CS}$ to Select Switching Delay	To 90% of Write Current or to 90% of 100mV, 10MHz Read Signal Envelope			600	ns
t_{WI} or t_{RI}	$\overline{CS}$ to Unselect Switching Delay	To 90% Decay of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			600	ns
t_{HS}	Head Select Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope			600	ns
tD1	Safe to Unsafe Write Unsafe Delay	$I_W = 50mA$	1.6		8	us
tD2	Unsafe to Safe Write Unsafe Delay	$I_W = 20mA$			1	us
tD3	Prop. Delay Head Current	$L_H = 0$, $R_H = 0$ From 50% points		25	40	ns
tD3	Asymmetry Head Current	WDI has 50% Duty Cycle and 1nS Rise/Fall Time			2	ns
	Rise/Fall Head Current	10% and 90% Points			20	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Maximum junction temperature (T_J) should not exceed 135°C.

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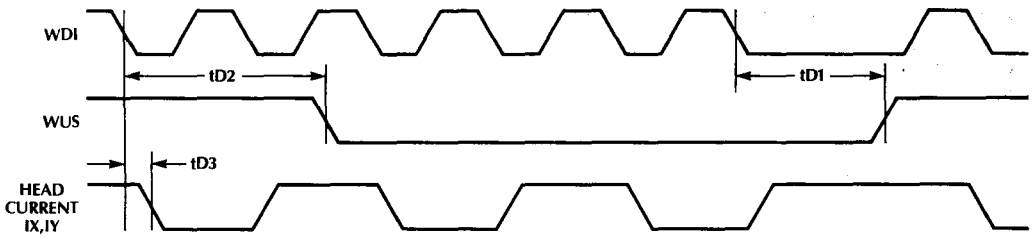
TIMING DIAGRAM



Write Mode Timing Diagram

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

For any selected head, the ML501, ML502 functions as a read amplifier when in the Read mode, or as a write current switch when in the Write mode. Pins $\overline{HS0}$, HS1 and HS2 determine head selection while pin $R/\overline{W}$ controls the Read/Write mode. A detected "write-unsafe" condition is indicated by pin WUS.

READ MODE

When the ML501, ML502 is in the Read Mode, it operates as a low-noise differential amplifier on the selected channel. In Read mode the write data flip-flop is set and both the write unsafe detector and the write current source are deactivated. The center tap voltage is also lowered. Pins RDX and RDY provide differential emitter follower outputs which are in phase with the X and Y head input pins.

Note that during the Read or Chip Deselect mode the internal write current is deactivated, thus making external write current gating unnecessary.

WRITE MODE

The ML501, ML502 operates as a write-current switch when in the Write mode. Write current magnitude is determined by the following relationship:

$I_W = K/R_{WC}$

Where: K = Write Current Constant

R_{WC} = Resistance connected between pin WC and GND.

The head current is toggled between the X and Y side of the selected head by a negative transition on WDI (Write Data Input). When switching the ML501, ML502 to write mode, the WDFF (Write Data Flip-Flop) is initialized to pass write current through the X-side of the head.

The ML501, ML502 exhibit enhanced write current stability, compared to similar read/write circuits, which reduces the problem of oscillation. This is a result of increased internal write current compensation. Also, write current "glitches" during power-up, common in similar read/write circuits, are eliminated with an exclusive write current disabling function.

The WUS (Write Unsafe) pin is an open collector output that gives a logic high level for any of the following unsafe write conditions:

- Open head
- Open head center-tap
- Too low WDI frequency
- Read mode selected
- Device not selected
- No write current

Two negative transitions on WDI are required to clear WUS after the fault condition is removed.

The ML502, ML502R, ML502S differ from the ML501, ML501R by having write unsafe detect circuitry that is designed to operate with lower amplitude write pulse voltages, which result from the lower head inductance of thin film or composite heads.

Table 1.

Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

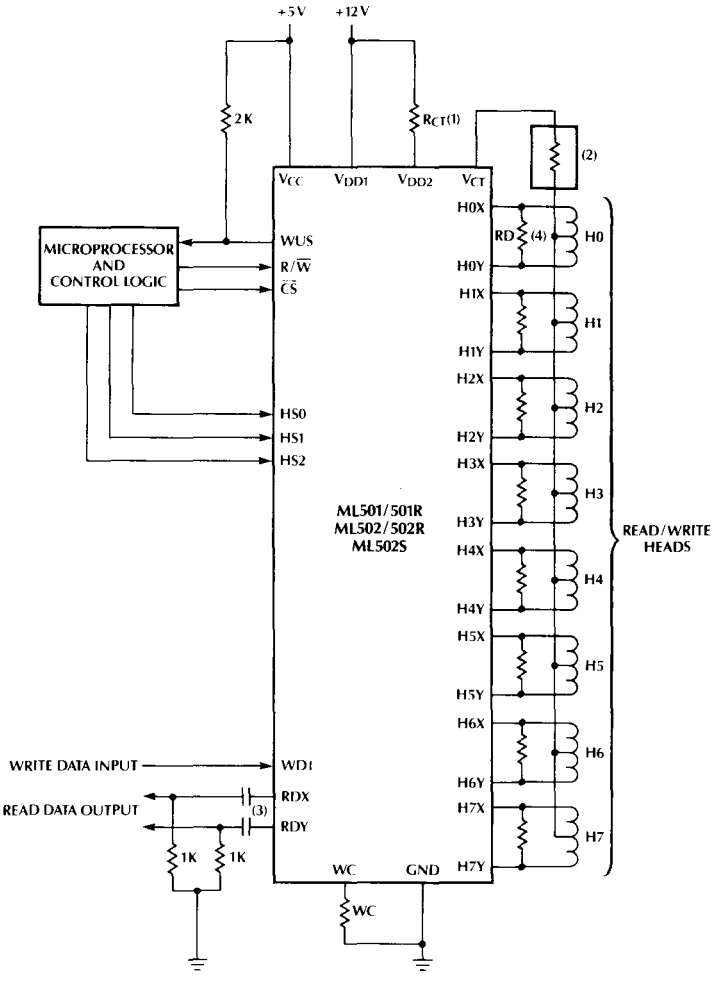
Table 2.

Mode Select

$\overline{CS}$	$R/\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

TYPICAL APPLICATION



NOTES:

1. RCT is optional and is used to limit internal power dissipation (Otherwise connect $V_{DD}1$ to $V_{DD}2$).
   RCT (1/2 Watt) = 120 (50/I_W) ohms
   where I_W = Write Current, in mA
2. Ferrite bead optional: used to suppress write current overshoot and ringing. Recommend Ferroxcube 3659065/4A6.
3. RDX and RDY load capacitance 20 pF maximum. RDX and RDY output current must be limited to 100 μA.
4. Damping resistors not required on ML501R or ML502R.

ORDERING INFORMATION

PART NUMBER	PACKAGE	NUMBER OF CHANNELS	TRANSDUCER HEAD TYPE
ML501-6CP	28-Lead Molded DIP (P28)	6	Ferrite Heads
ML501-6CQ	28-Lead PCC (Q28)	6	
ML501-6CS	28-Lead SOIC (S28)	6	
ML501-8CP	40-Lead Molded DIP (P40)	8	
ML501-8CQ	44-Lead PCC (Q44)	8	
ML501-8CS*	32-Lead SOIC (S32)	8	
ML501R-6CP	28-Lead Molded DIP (P28)	6	Ferrite Heads
ML501R-6CQ	28-Lead PCC (Q28)	6	
ML501R-6CS	28-Lead SOIC (S28)	6	
ML501R-8CP	40-Lead Molded DIP (P40)	8	
ML501R-8CQ	44-Lead PCC (Q44)	8	
ML501R-8CS*	32-Lead SOIC (S32)	8	
ML502-6CP	28-Lead Molded DIP (P28)	6	Thin Film or Composite Heads
ML502-6CQ	28-Lead PCC (Q28)	6	
ML502-6CS	28-Lead SOIC (S28)	6	
ML502-8CP	40-Lead Molded DIP (P40)	8	
ML502-8CQ	44-Lead PCC (Q44)	8	
ML502-8CS*	32-Lead SOIC (S32)	8	
ML502R-6CP	28-Lead Molded DIP (P28)	6	Thin Film or Composite Heads
ML502R-6CQ	28-Lead PCC (Q28)	6	
ML502R-6CS	28-Lead SOIC (S28)	6	
ML502R-7CQ	28-Lead PCC (Q28)	7	
ML502R-8CP	40-Lead Molded DIP (P40)	8	
ML502R-8CQ	44-Lead PCC (Q44)	8	
ML502R-8CS*	32-Lead SOIC (S32)	8	
ML502S-6CQ	28-Lead PCC (Q28)	6	Thin Film or Composite Heads
ML502S-7CQ	28-Lead PCC (Q28)	7	
ML502S-8CQ	44-Lead PCC (Q44)	8	

* This package is available as a special order only.