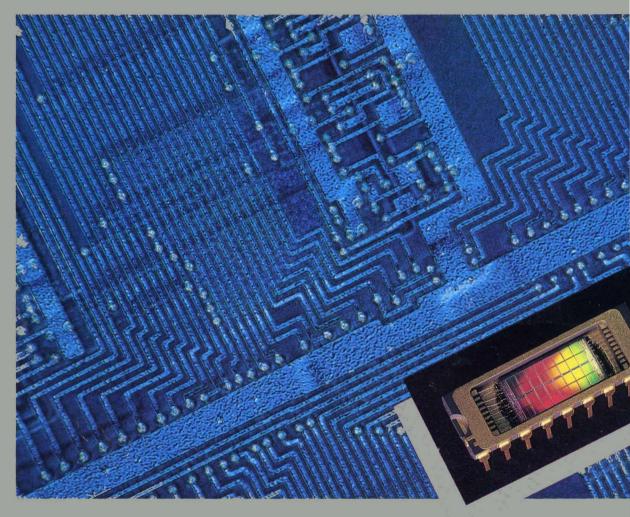
# **MOS DATA BOOK**



MCRON TECHNOLOGY, INC.

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# MOS DATA BOOK

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The MOS Data Book has been organized into nine sections and includes complete detailed specifications on our growing, high performance CMOS and NMOS product line.

Sections 1 through 7 cover individual product families. Each section contains a product selection guide followed by data sheets. Three different types of data sheets are used: Advance Information, which contains initial descriptions of products still under development; Preliminary Information, which contains initial device characterization limits which are subject to change upon full characterization of production devices; and Final Information, which contains minimum and maximum limits specified over the complete power supply and temperature range for production devices.

Section 8 contains detailed mechanical data on each package used by Micron.

Section 9 contains sales information, with a list of sales representatives and distributors by geographical location for the North American Continent, Europe and Asia.

Additional or updated information on any Micron product is available from:

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42C4064 883C       VRAM       7-65         42C4256       VRAM       3-29         5C1001       SRAM       4-129         5C1005       SRAM       4-127         5C1008       SRAM       4-125         5C1601       SRAM       4-45         5C1601 883C       SRAM       7-111         5C1604       SRAM       4-11         5C1605       SRAM       4-19         5C1606       SRAM       4-27         5C1607       SRAM       4-27         5C1608       SRAM       4-3         5C1608 883C       SRAM       7-95         5C2561       SRAM       7-151         5C2564       SRAM       7-151         5C2564       SRAM       4-101         5C2565       SRAM       7-143         5C2565       SRAM       4-109				
42C4256       VRAM       3-29         5C1001       SRAM       4-129         5C1005       SRAM       4-127         5C1008       SRAM       4-125         5C1601       SRAM       4-45         5C1601 883C       SRAM       7-111         5C1604       SRAM       4-11         5C1605       SRAM       4-19         5C1606       SRAM       4-27         5C1607       SRAM       4-27         5C1608       SRAM       4-3         5C1608 883C       SRAM       7-95         5C2561       SRAM       4-117         5C2564       SRAM       7-151         5C2564 883C       SRAM       4-101         5C2565       SRAM       7-143         5C2565       SRAM       4-109				
5C1001       SRAM       4-129         5C1005       SRAM       4-127         5C1008       SRAM       4-125         5C1601       SRAM       4-45         5C1601 883C       SRAM       7-111         5C1604       SRAM       4-11         5C1605       SRAM       4-19         5C1606       SRAM       4-27         5C1607       SRAM       4-27         5C1608       SRAM       4-3         5C1608 883C       SRAM       4-3         5C2561       SRAM       7-95         5C2561       SRAM       7-151         5C2564       SRAM       4-101         5C2565       SRAM       7-143         5C2565       SRAM       4-109				
5C1005       SRAM       4-127         5C1008       SRAM       4-125         5C1601       SRAM       4-45         5C1601 883C       SRAM       7-111         5C1604       SRAM       4-11         5C1605       SRAM       4-19         5C1606       SRAM       4-27         5C1607       SRAM       4-27         5C1608       SRAM       4-3         5C1608 883C       SRAM       7-95         5C2561       SRAM       4-117         5C2564       SRAM       7-151         5C2564       SRAM       4-101         5C2565       SRAM       7-143         5C2565       SRAM       4-109				
5C1008       SRAM       4-125         5C1601       SRAM       4-45         5C1601 883C       SRAM       7-111         5C1604       SRAM       4-11         5C1605       SRAM       4-19         5C1606       SRAM       4-27         5C1607       SRAM       4-27         5C1608       SRAM       4-3         5C1608 883C       SRAM       7-95         5C2561       SRAM       4-117         5C2564 883C       SRAM       7-151         5C2564       SRAM       4-101         5C2565       SRAM       7-143         5C2565       SRAM       4-109				
5C1601       SRAM       4-45         5C1601 883C       SRAM       7-111         5C1604       SRAM       4-11         5C1605       SRAM       4-19         5C1606       SRAM       4-27         5C1607       SRAM       4-27         5C1608       SRAM       4-3         5C1608 883C       SRAM       7-95         5C2561       SRAM       4-117         5C2564 883C       SRAM       7-151         5C2564       SRAM       4-101         5C2565       SRAM       7-143         5C2565       SRAM       4-109				
5C1601 883C       SRAM       7-111         5C1604       SRAM       4-11         5C1605       SRAM       4-19         5C1606       SRAM       4-27         5C1607       SRAM       4-27         5C1608       SRAM       4-3         5C1608 883C       SRAM       7-95         5C2561       SRAM       4-117         5C2564       SRAM       7-151         5C2564       SRAM       4-101         5C2565       SRAM       7-143         5C2565       SRAM       4-109				
5C1604       SRAM       4-11         5C1605       SRAM       4-19         5C1606       SRAM       4-27         5C1607       SRAM       4-27         5C1608       SRAM       4-3         5C1608 883C       SRAM       7-95         5C2561       SRAM       4-117         5C2561 883C       SRAM       7-151         5C2564       SRAM       4-101         5C2564 883C       SRAM       7-143         5C2565       SRAM       4-109				
5C1605       SRAM       4-19         5C1606       SRAM       4-27         5C1607       SRAM       4-27         5C1608       SRAM       4-3         5C1608 883C       SRAM       7-95         5C2561       SRAM       4-117         5C2561 883C       SRAM       7-151         5C2564       SRAM       4-101         5C2564 883C       SRAM       7-143         5C2565       SRAM       4-109				
5C1606       SRAM       4-27         5C1607       SRAM       4-27         5C1608       SRAM       4-3         5C1608 883C       SRAM       7-95         5C2561       SRAM       4-117         5C2561 883C       SRAM       7-151         5C2564       SRAM       4-101         5C2564 883C       SRAM       7-143         5C2565       SRAM       4-109				
5C1607       SRAM       4-27         5C1608       SRAM       4-3         5C1608 883C       SRAM       7-95         5C2561       SRAM       4-117         5C2561 883C       SRAM       7-151         5C2564       SRAM       4-101         5C2564 883C       SRAM       7-143         5C2565       SRAM       4-109				
5C1608       SRAM       4-3         5C1608 883C       SRAM       7-95         5C2561       SRAM       4-117         5C2561 883C       SRAM       7-151         5C2564       SRAM       4-101         5C2564 883C       SRAM       7-143         5C2565       SRAM       4-109				
5C1608 883C       SRAM       7-95         5C2561       SRAM       4-117         5C2561 883C       SRAM       7-151         5C2564       SRAM       4-101         5C2564 883C       SRAM       7-143         5C2565       SRAM       4-109				
5C2561       SRAM       4-117         5C2561 883C       SRAM       7-151         5C2564       SRAM       4-101         5C2564 883C       SRAM       7-143         5C2565       SRAM       4-109				
5C2561 883C       SRAM       7-151         5C2564       SRAM       4-101         5C2564 883C       SRAM       7-143         5C2565       SRAM       4-109			***************************************	
5C2564       SRAM       4-101         5C2564 883C       SRAM       7-143         5C2565       SRAM       4-109				
5C2564 883C       SRAM       7-143         5C2565       SRAM       4-109				
5C2565 SRAM 4-109				
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#### **DRAM PRODUCT SELECTION GUIDE**

Memory	Optional			Power D	issipation		Pac	kage and	Number o	f Pins Pro	cess			
Configuration	Access Cycle	Part Number	Access Time (ns)	Standby	Active	PDIP	PLCC	ZIP	SOJ	CDIP	CLCC	Flat Pack	Process	Page
64K x 1	Page Mode	MT4264	100,120,150,200	15mw	75mw	16	-	-	-	16	18	16	NMOS	1-3
64K x 4	Page Mode	MT4067	80,100,120,150	15mw	150mw	18	18	20	-	18	18	16	NMOS	1-13
256K x 1	Page Mode	MT1259	80,100,120,150	15mw	150mw	16	18	16	-	16	18	16	NMOS	1-23
256K x 4	Fast Page Mode	MT4C4256	80,100,120,150	5mw	175mw	20	-	20	20	20	-	20	CMOS	1-33
256K x 4	Static Column	MT4C4258	80,100,120,150	5mw	175mw	20	-	20	20	20	-	20	CMOS	1-45
1 Meg x 1	Fast Page Mode	MT4C1024	80,100,120,150	5mw	175mw	18	-	20	20	18	-	18	CMOS	1-57
1 Meg x 1	Nibble Mode	MT4C1025	80,100,120,150	5mw	175mw	18		20	20	18	-	18	CMOS	1-69
1 Meg x 1	Static Column	MT4C1026	80,100,120,150	5mw	175mw	18	-	20	20	18	-	18	CMOS	1-81
1 Meg x 4	Fast Page Mode	MT4C4001	80,100,120	5mw	175mw	20	-	-	20	20	-	-	CMOS	1-93
1 Meg x 4	Static Column	MT4C4003	80,100,120	5mw	175mw	20	-	-	20	20	-		CMOS	1-105
4 Meg x 1	Fast Page Mode	MT4C1004	80,100,120	5mw	175mw	18	-	-	20	18	-	-	CMOS	1-117
4 Meg x 1	Nibble Mode	MT4C1005	80,100,120	5mw	175mw	18	-	-	20	18	-	-	CMOS	1-129
4 Meg x 1	Static Column	MT4C1006	80,100,120	5mw	175mw	18		-	20	18	-	-	CMOS	1-141

### **DRAM**

## **64K x 1 DRAM**

PAGE MODE

#### **FEATURES**

- Industry standard pin-out, funtions, timing
- Single +5V ±10% power supply
- Low power, 15mW standby, 75mW active, typical
- Common I/O using EARLY-WRITE
- DOUT held indefinitely by CAS
- 256 cycle refresh in 4ms
- Fully compatible with MT1259 (256K)
- Optional Page Mode

OPTIONS	MARKING
<ul> <li>Timing</li> </ul>	
100ns access	-10
120ns access	-12
150ns access	-15
200ns access	-20
Packages:	
Plastic DIP	None
Ceramic DIP	С

### PIN ASSIGNMENT (Top View) MT4264 16 Pin DIP NC 11. 16 1 VSS DIN 12 15 TCAS WE [3 14∏Dout RAS 14 13∏A6 A0∏5 12∏A3 А2∏6 11∏A4 А1∏7 10∏A5 Vcc∏8 PA, CA

#### GENERAL DESCRIPTION

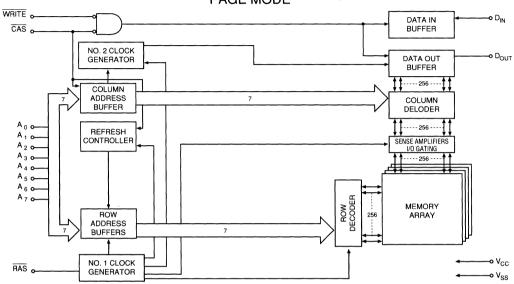
The MT4264 is a randomly accessed solid-state memory containing 65,536 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 16 address bits which are entered 8 bits (A0-A7) at a time. RAS is used to latch the first 8 bits and CAS the latter 8 bits. A READ or WRITE cycle is selected with the WE input. A logic high on WE dictates READ mode while a logic low on WE dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes low prior to CAS going low, the output pin(s) remain open (High Z) until the next CAS cycle. If WE goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as  $\overline{CAS}$  remains low (regardless of  $\overline{WE}$  or  $\overline{RAS}$ ). This late  $\overline{WE}$  pulse results in a READ-WRITE cycle.

Returning  $\overline{RAS}$  and  $\overline{CAS}$  high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{RAS}$  cycle (READ, WRITE,  $\overline{RAS}$  only or Hidden refresh) so that all 256 combinations of  $\overline{RAS}$  addresses (A0-A7) are executed at least every 4ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0 - A7) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by RAS followed by a column address strobed in by CAS. By holding RAS low, CAS may be toggled strobing in different column addresses executing faster memory cycles. Returning RAS high terminates the PAGE MODE operation.



## FUNCTIONAL BLOCK DIAGRAM PAGE MODE



#### **FUNCTIONAL TRUTH TABLE**

				Addr	esses		
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	į
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	-
PAGE-MODE READ	L	H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	



#### **ABSOLUTE MAXIMUM RATINGS\***

 \*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}C \leq T_{\mbox{\scriptsize A}} \leq 70^{\circ}) \; (\mbox{\scriptsize Vcc} = 5.0 \mbox{\scriptsize V} \pm 10\%)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
STANDBY CURRENT (RAS = CAS = VIH after 8 RAS cycles)	lcc1		4	mA	
OPERATING CURRENT (RAS and CAS Cycling)	lcc2		30	mA	2
RAS ONLY REFRESH CURRENT (CAS = Vih)	Іссз		20	mA	2
PAGE MODE CURRENT (RAS = VIL, CAS = Cycling)	Icc4		30	mA	2
INPUT LEAKAGE Input leakage current, any input (0V ≤ VIN ≤ Vcc), all other pins not under test = 0 volts)	lı .	-10	10	μА	
OUTPUT LEAKAGE Output leakage current (Dou⊤ is disabled, 0V ≤ Vouт ≤ Vcc)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High (Logic 1) voltage (Iout = -5mA)	Vон	2.4		V	1
Output Low (logic 0) voltage (lout = 5mA)	Vol		0.4	V	1

#### RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{A} \leq 70^{\circ})$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	<b>V</b> cc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	<b>V</b> cc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1

#### CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A <sub>0</sub> -A <sub>7</sub> ), D <sub>IN</sub>	Cl1		5	pF	18
Input Capacitance RAS, CAS, WE	CI2		8	pF	18
Output Capacitance Dout	Co		8	pF	18



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 3, 4, 5, 10, 11, 17, 18) (0°C $\leq$ T $_{A}$ $\leq$ 70°C) (Vcc = 5.0V $\pm$ 10%)

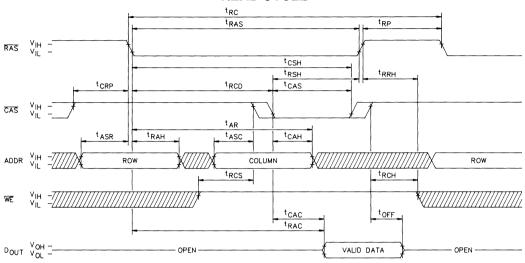
A.C. CHARACTERISTICS			10	-	12	-	15	_	-20		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	195		230		260		330		ns	6, 7
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	220		255		295		370		ns	
PAGE-MODE cycle time	<sup>t</sup> PC	90		100		120		170		ns	6, 7
Access time from RAS	t <sub>RAC</sub>		100		120		150		200	ns	7, 8
Access time from CAS	t <sub>CAC</sub>		50		60		75		120	ns	7, 9
RAS pulse width	t <sub>RAS</sub>	100	10,000	120	10,000	150	10,000	200	10,000	ns	
RAS hold time	t <sub>RSH</sub>	50		60		75		100		ns	
RAS precharge time	<sup>t</sup> RP	80	20,000	90	20,000	100	20,000	120	20,000	ns	
CAS pulse width	tCAS	50	10,000	60	10,000	75	10,000	120	10,000	ns	
CAS hold time	t <sub>CSH</sub>	100		120		150		200		ns	
CAS precharge time	<sup>t</sup> CPN	25		25		30		35		ns	19
CAS precharge time (PAGE-MODE)	<sup>t</sup> CP	30		30		35		40		ns	
RAS to CAS delay time	t <sub>RCD</sub>	25	50	25	60	25	75	30	80	ns	13
Row address set-up time	t <sub>ASR</sub>	0		0		0		0		ns	
Row address hold time	t <sub>RAH</sub>	15		15		20		25		ns	
Column address set-up time	†ASC	0		0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	20		20		25		50		ns	
Column address hold time referenced to RAS	t <sub>AR</sub>	70		80		100		130		ns	
READ command set-up time	tRCS	0		0		0		0		ns	
READ command hold time referenced to CAS	<sup>t</sup> RCH	0		0		0		0	i	ns	14
READ command hold time referenced to RAS	<sup>t</sup> RRH	0		0		0	i	0		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	30	0	30	0	35	0	40	ns	12
WE command set-up time	twcs	0		0		0		0		ns	16
WRITE command hold time	tWCH	35		40		45		60		ns	
WRITE command hold time referenced to RAS	tWCR	85		100		120		140		ns	
WRITE command pulse width	t <sub>WP</sub>	35		40	1	45	T	50		ns	
WRITE command to RAS lead time	t <sub>RWL</sub>	35		40		45		55		ns	
WRITE command to CAS lead time	tCWL	35		40		45	1	55		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		0		ns	15
Data-in hold time	t <sub>DH</sub>	35		40		45		55		ns	15
Data-in hold time referenced to RAS	t <sub>DHR</sub>	85		100		120		135		ns	
CAS to WE delay	tCWD	40		50	1	60	<b> </b>	100	<del>                                     </del>	ns	16
RAS to WE delay	tRWD	90	<b> </b>	110	1	135	<b>†</b>	180	<b> </b>	ns	16
Transition time (rise or fall)	t <sub>T</sub>	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	tREF		4	-	4		4		4	ms	3, 17
CAS to RAS set-up time	tCRP	10	<del>                                     </del>	15	+	20	+-	20	+	ns	<del>                                     </del>

#### **NOTES**

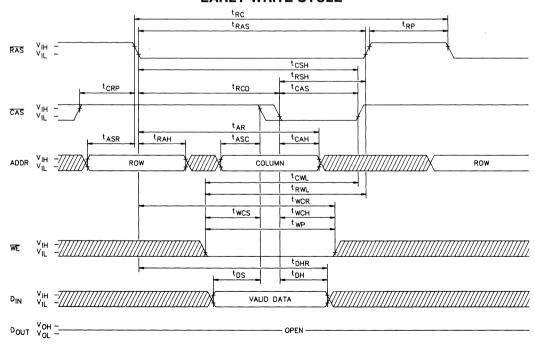
- 1. All voltages referenced to Vss.
- 2. Icc is dependent on output loading and cycle rates. Specified values are obtained the output open.
- 3. An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 4. AC characteristics assume  ${}^{t}T = 5ns$ .
- 5. Vih min and Vil max are reference levels for measuring timing of input signals. Transition times are measured between Vih and Vil (or between Vil and VIH).
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range  $(0^{\circ}C) \le T_A \le 70^{\circ}C$ ) is assured. 7. Measured with a load equivalent to 2 TTL gates and
- 100pF.
- 8. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- Assumes that <sup>t</sup>RCD ≥ <sup>t</sup>RCD (max). pulsed high for <sup>t</sup>CPN.
- 10. Îf  $\overline{CAS} = \overline{V}_{IH}$ , data output is high impedance.
- 11. If  $\overline{CAS} = VIL$ , data output may contain data from the last valid READ cycle.
- 12. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to Voh ot Vol.

- 13. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified fRCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 14. tRCH is referenced to the first rising edge of RAS or
- 15. These parameters are referenced to  $\overline{CAS}$  leading edge in early WRITE cycles and WE leading edge in late WRITE or READ-WRITE cycles.
- 16. tWCS, tRWD and tCWD are restrictive operating parameters in late READ-WRITE and READ-MODIFY-WRITE cycles only. If  ${}^{t}WCS \ge {}^{t}WCS$  (min) the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If  ${}^{t}CWD \ge {}^{t}CWD$  (min) and  ${}^{t}RWD \ge$ <sup>t</sup>RWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to Vін) is indeterminate.
- 17. In addition to meeting the transition rate specification, all input signals must transit between Vih and VIL (or between VIL and VIH) in a monotonic manner.
- 18. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and VCC =
- 19. If  $\overline{CAS}$  is low at the falling edge of  $\overline{RAS}$ , DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be

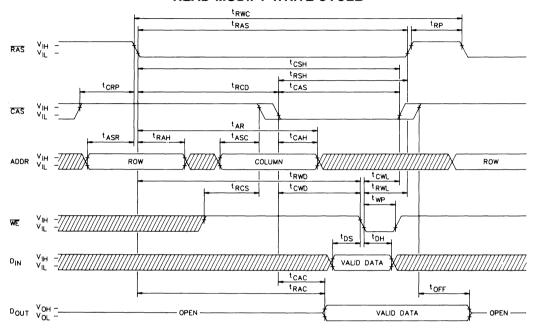
#### **READ CYCLE**



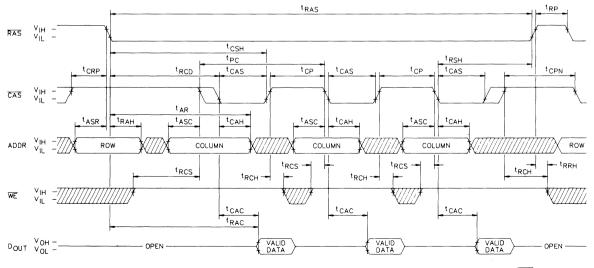
#### **EARLY-WRITE CYCLE**



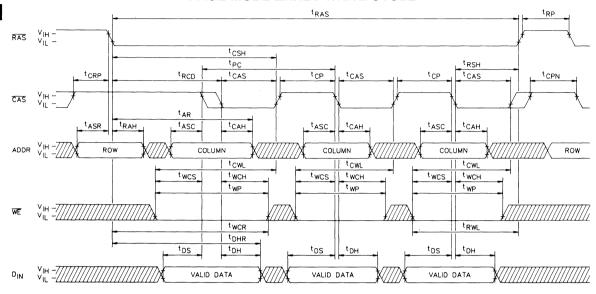
## READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE



#### **PAGE-MODE READ CYCLE**

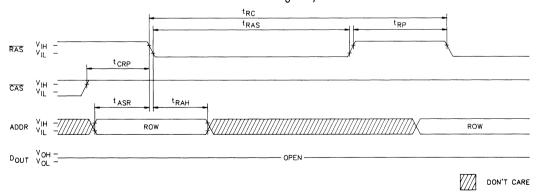


#### PAGE-MODE EARLY-WRITE CYCLE



### **RAS ONLY REFRESH CYCLE**

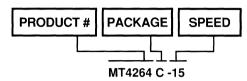
 $(\mathsf{ADDR} = \mathsf{A}_0 - \mathsf{A}_7)$ 



### MICHON

#### **ORDER INFORMATION**

64K x 1, 150ns in Ceramic DIP



The Micron MT4264 is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the NMOS double-poly

process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burnin and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

## **DRAM**

## **64K x 4 DRAM**

#### **FEATURES**

ODTIONIC

- · Industry standard pin-out, timing, functions
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby, 150mW active, typical

NAA DIZINIC

- Refresh modes: RAS only, CAS before RAS, and Hidden
- 256 cycle refresh in 4ms
- Optional Page Mode access cycle

OPTIONS	MAKKING
Timing	
80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15
<ul> <li>Packages:         Plastic DIP         Ceramic DIP         Plastic ZIP         Plastic PLCC     </li> </ul>	None C Z EJ
Temperature	
$0^{\circ}\text{C} \le \text{T}_{\text{A}} \le 70^{\circ}\text{C}$	None
$-55^{\circ}\text{C} \le \text{T}_{\text{A}} \le 110^{\circ}\text{C}$	XT

#### **GENERAL DESCRIPTION**

The MT4067 is randomly accessed solid-state memory containing 262,144 bits organized in a x4 configuration. The 16 address bits are entered 8 bits at a time using  $\overline{RAS}$  to latch the first 8 bits and  $\overline{CAS}$  the latter 8 bits. If the  $\overline{WE}$  pin goes low prior to  $\overline{CAS}$  going low, the output pin remains open until the next  $\overline{CAS}$  cycle. If  $\overline{WE}$  goes low after Data reaches the output pin, the output pin is activated and retains the selected cell data as long as  $\overline{CAS}$  remains low (regardless of  $\overline{WE}$  or  $\overline{RAS}$ ). This late  $\overline{WE}$  pulse results in a READ-MODIFY-WRITE cycle. Data-in is latched when  $\overline{WE}$  strobes low.

By holding RAS low, CAS may be toggled to execute

#### PIN ASSIGNMENT (Top View) MT4067 18 Pin DIP OE (1. 18) Vss 17 DQ4 DQ1 ∏2 DQ2 [13 16 TCAS ₩E ∏4 15Праз RAS 15 14ПАО PB. CB **А6**П6 13∏A1 12 DA2 А5∏7 11[] A3 A4∏8 Vcc∏9 10 A7 MT4067 18 Pin PLCC 12 1 18 7 [ DQ2 WE RAS þ16 CAS b15 DQ3 50 b14 A0 13 A1 Α6 b12 A2 EJA 4 > 4 A A W

several faster READ, WRITE, READ-WRITE or READ-MODIFY-WRITE cycles within the RAS address defined PAGE boundary. Returning RAS high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the RAS high-time. Memory cell data is retained in its correct state by maintaining power and executing a RAS (Refresh) cycle so that all 256 combinations of RAS addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

**⊸** ∨<sub>SS</sub>

#### **FUNCTIONAL BLOCK DIAGRAM** PAGE MODE WRITE . DATA IN o I/O 1 CAS \_ BUFFER **-0** I/O 2 **-0** I/O 3 NO. 2 CLOCK **⊸** I/O 4 DATA OUT GENERATOR BUFFER TF o 1--- 256 x 4 --- 1 • ŌE COLUMN ADDRESS 8 COLUMN DELODER BUFFER A 0 0 ---- 256 x 4 --- 1 REFRESH A 2 0-CONTROLLER SENSE AMPLIFIERS I/O GATING A 3 o-A 4 o-1 1 --- 256 x 4 ---A 5 0-REFRESH A 6 0 COUNTER A 7 0-रुष्ट A 8 0-ROW DECODER MEMORY ROW ARRAY ADDRESS 8 8 BUFFERS (8) ⊸ V<sub>CC</sub> NO. 1 CLOCK RAS . GENERATOR

#### **FUNCTIONAL TRUTH TABLE**

					Addre	esses		
Function	RAS	CAS	WE	ŌĒ	tR	tC		NOTES
Standby	Н	Н	Н	Н	Х	Х	High Impedance	
READ	L	L	Н	L	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	Н	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	Н	L	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	Н	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Н	Х	Х	High Impedance	



#### **ABSOLUTE MAXIMUM RATINGS\***

 \*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (0°C $\leq$ T $_{A}$ $\leq$ 70°C) (Vcc = 5.0V $\pm10\%$ )

SYMBOL	MIN	MAX	UNITS	NOTES
Vcc	4.5	5.5	٧	
Vih	2.4	Vcc+1	٧	1
VIL	-1.0	0.8	٧	1
lı	-10	10	μА	
loz	-10	10	μΑ	
Vон	2.4	0.4	٧	1
	Vcc VIH VIL II	Vcc 4.5  ViH 2.4  ViL -1.0  II -10  Voh 2.4	Vcc 4.5 5.5 VIH 2.4 Vcc+1 VIL -1.0 0.8 II -10 10 Ioz -10 10	Vcc 4.5 5.5 V VIH 2.4 Vcc+1 V VIL -1.0 0.8 V II -10 10 μA Ioz -10 10 μA

(Notes: 1.2.3.4.6) ( $0^{\circ}$ C  $\leq T_{\bullet} \leq 70^{\circ}$ C) ( $V_{CC} = 5.0V \pm 10\%$ )

(Notes: 1,2,3,4,6) $(0^{\circ}C \le 1_{A} \le 70^{\circ}C)$ (Vcc = 5.0V ±10%)			MA	X			
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels (RAS = CAS = VIH after 8 RAS cycles)	lcc1	5	5	5	5	mA	
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc2	65	55	55	45	mA	2
OPERATING CURRENT: PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	Іссз	65	55	55	45	mA	2
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih: trc = trc(MIN))	icc4	55	40	40	35	mA	2
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = cycling, trc = trc(MIN))	lcc5	65	55	55	45	mA	2,22

#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As), DIN	C <sub>11</sub>		5	pF	18
Input Capacitance RAS, CAS, WE, OE	CI2		8	pF	18
Output Capacitance Dout	Co		7	pF	18



# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 3, 4, 5, 10, 11, 17, 18) (0°C $\leq$ T $_A$ $\leq$ 70°C) (Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS PARAMETER		-8		-10		-12		-15			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	200		250		295		345		ns	
PAGE-MODE cycle time	t <sub>PC</sub>	75		90		100		120		ns	6, 7
Access time from RAS	t <sub>RAC</sub>		80		100		120		150	ns	7, 8
Access time from CAS	†CAC		40		50		60		75	ns	7. 9
Output Enable	t <sub>OE</sub>		25		25		30		40	ns	
RAS pulse width	t <sub>RAS</sub>	80	10,000	100	10.000	120	10,000	150	10,000	ns	
RAS hold time	tRSH	40		50		60		75		ns	
RAS precharge time	t <sub>RP</sub>	60		80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	40	10,000	50	10,000	60	10,000	75	10,000	ns	
CAS hold time	tCSH	80	1.0,000	100	, , , , , , ,	120	10,000	150	1.0,000	ns	
CAS precharge time	t <sub>CPN</sub>	20	<u> </u>	25		25		30	<u> </u>	ns	19
CAS precharge time (PAGE-MODE)	t <sub>CP</sub>	25		30		30		35		ns	<u> </u>
RAS to CAS delay time	tRCD	20	40	25	50	25	60	25	75	ns	13
CAS to RAS set-up time	tCRP	10	"	15	"	20	"	20	1.0	ns	"
Row address set-up time	tASR	0	<u> </u>	0	†	0	·	0	1	ns	
Row address hold time	†RAH	15		15	<b></b>	15		15		ns	
Column address set-up time	tASC	0	<del>†                                      </del>	0	†	0		0	<del> </del>	ns	
Column address hold time	<sup>t</sup> CAH	15	<del>                                     </del>	20		20		25	<del>                                     </del>	ns	
Column address hold time	t <sub>AR</sub>	50	<u> </u>	70		80	<u> </u>	100	<del>                                     </del>	ns	<u> </u>
referenced to RAS	70	30		/0		60		100		115	
READ command set-up time	tRCS	0	1	0		0		0	+		
READ command hold time	t <sub>RCH</sub>	0	<del>                                     </del>	0	<b></b>	0	<del> </del>	0	1	ns ns	14
referenced to CAS				0				0		ns	14
READ command hold time referenced to RAS	t <sub>RRH</sub>	0		0		0		0		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	25	0	30	0	30	0	35	ns	12
Output Disable	tOD		25		30		30		35	ns	
WE command set-up time	twcs	0		0		0		0		ns	16
WRITE command hold time	tWCH	15		35		40		45		ns	
WRITE command hold time referenced to RAS	twcR	35		85		100		120		ns	
WRITE command pulse width	tWP	15		35		40		45		ns	T
WRITE command to RAS lead time	t <sub>RWL</sub>	35		35		40		45		ns	
WRITE command to CAS lead time	tCWL	35		35		40		45		ns	
Data-in set-up time	t <sub>DS</sub>	0	1	0		0		0		ns	15
Data-in hold time	t <sub>DH</sub>	15	<b>†</b>	35	1	40		45		ns	15
Data-in hold time	†DHR	35		60	<b>†</b>	65	<del>                                     </del>	70	<b>†</b>	ns	1
referenced to RAS	51111	33		33		33		, 0	1	"13	
CAS to WE delay	tCWD	50	<b>†</b>	70	<b>†</b>	90	<b>†</b>	110	<b>†</b>	ns	16
RAS to WE delay	t <sub>RWD</sub>	90	<del>                                     </del>	120	<del> </del>	150	<del>                                     </del>	185	+	ns	16
Transition time (rise or fall)	t <sub>T</sub>	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	t <sub>REF</sub>		4		4	-	4	3	4	ms	22
CAS hold time (CAS-before-RAS refresh)	tCHR	15	+	20	<del>  "</del> -	25	+	30	4	ns	21

### MICRON

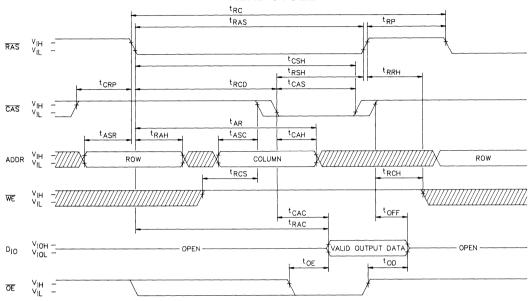
#### **NOTES**

- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of  $100\mu s$  is required after power-up followed by any  $8 \overline{RAS}$  cycles before proper device operation is assured. The  $8 \overline{RAS}$  cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
- 4. AC characteristics assume  ${}^{t}T = 5$ ns.
- 5. Vih min and Vil max are reference levels for measuring timing of input signals. Transition times are measured between Vih and Vil.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- Measured with a load equivalent to 2 TTL gates and 100pF.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 9. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 10. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 11. If  $\overline{\text{CAS}} = \text{Vil}$ , data output may contain data from the last valid READ cycle.
- 12. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to Voн or Vol.
- 13. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 14. <sup>t</sup>RCH is referenced to the first rising edge of <del>RAS</del> or <del>CAS</del>.

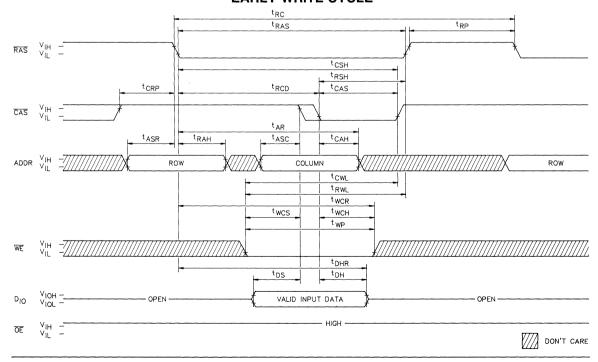
- 15. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles and to the  $\overline{\text{WE}}$  leading edge in late WRITE or READ-MODIFY-WRITE cycles.
- 16. tWCS, tCWD and tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (min) the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tCWD ≥ tCWD (min) and tRWD ≥ tRWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to VIH) is indeterminate.
- 17. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 18. Capacitance calculated from the equation  $C = \underline{I\Delta t} \Delta V$  with  $\Delta V = 3V$  and Vcc = 5V. This parameter is sampled.
- 19. If CAS is low at the falling edge of RAS, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CP. Note 8 applies to determine valid data out.
- 20. During a READ cycle if  $\overline{OE}$  is low then taken high (VIH) Dout goes open. If  $\overline{OE}$  is tied permanently low a READ-MODIFY-WRITE operation is not possible.
- 21. On-chip refresh and address counters are enabled.
- 22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{WE}$  = LOW and  $\overline{OE}$  = HIGH.



#### **READ CYCLE**

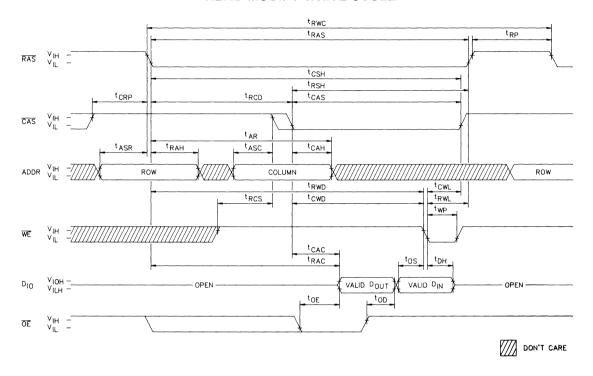


#### **EARLY-WRITE CYCLE**

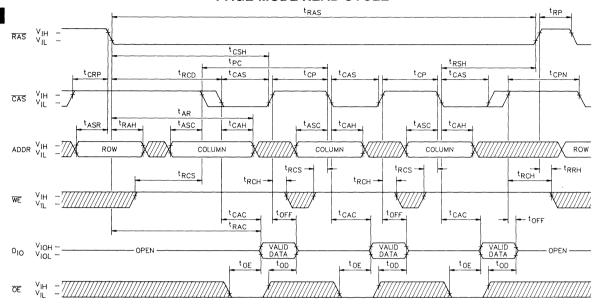




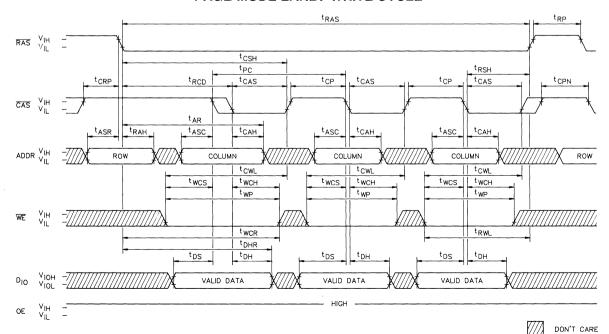
## READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE



#### PAGE-MODE READ CYCLE



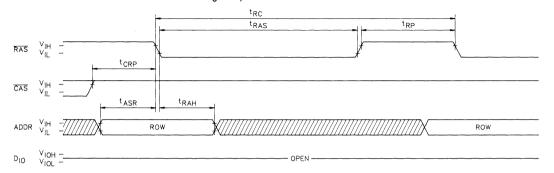
#### PAGE-MODE EARLY-WRITE CYCLE





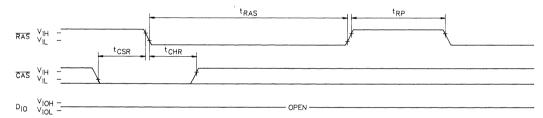
#### **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0 - A_7$ ; and  $\overline{WE} = DON'T CARE$ .)

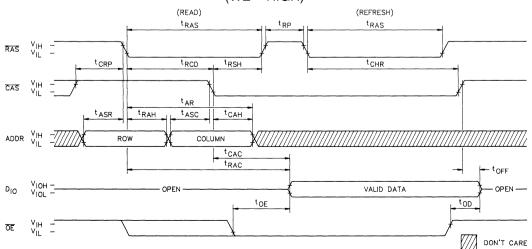


## **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_7 \overline{WE}, \overline{OE} = DON'T CARE.)$ 

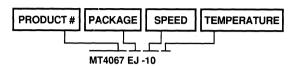


# $\begin{array}{l} \textbf{HIDDEN REFRESH CYCLE} \\ (\overline{\text{WE}} = \text{HIGH})^{22} \end{array}$



#### ORDER INFORMATION

64K x 4, 100ns in Plastic PLCC



The Micron MT4067 is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the NMOS double-poly

process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burnin and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

# DRAM

# 256K x 1 DRAM

#### **FEATURES**

- Industry standard pin-out, timing, functions
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby, 150mW active, typical
- Refresh modes: RAS only, CAS before RAS, and Hidden
- 256 cycle refresh in 4ms
- Optional Page Mode access cycle

OPTIONS	MARKING
Timing	
80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15
• Packages:	
Plastic DIP	None
Ceramic DIP	С
Plastic ZIP	Z
Plastic PLCC	EJ
Temperature	
$0^{\circ}\text{C} \le \text{T}_{\text{A}} \le 70^{\circ}\text{C}$	None
$-55^{\circ}\text{C} \le \text{T}_{A} \le 110^{\circ}\text{C}$	XT

#### PIN ASSIGNMENT (Top View) MT1259 16 Pin ZIP MT1259 16 Pin DIP А8\*П1• 16∏Vss 2 Dout \_\_\_ CAS DIN∏2 15 TCAS 4 Vss **A8**\* 5 **=**= WE [3 14 DOUT 6 DIN $\Gamma$ WF RAS 14 13∏A6 -= 8 RAS A<sub>0</sub> := А0∏5 12∏A3 == 10 A2 Α1 == А2Γ 11∏A4 == 12 Vcc 13k= 10 DA5 Α7 A1[17 c= 14 A5 15 EJ Vcc∏8 9ПА7 = 16 A3 PA, CA ZΑ MT1259 18 Pin PLCC A8\* VSS CAS α-**Ь**16 Dо∪т RAS NC þ15 A6 EJA b14 NC 13 A3 ΑO b12 A4 0005 A V C C A 7 \* ADDRESS NOT USED FOR RAS ONLY REFRESH

#### GENERAL DESCRIPTION

The MT1259 is randomly accessed solid-state memory containing 262,144 bits organized in a x1 configuration. The 18 address bits are entered 9 bits at a time using RAS to latch the first 9 bits and  $\overline{CAS}$  the latter 9 bits. If the  $\overline{WE}$  pin goes low prior to  $\overline{\text{CAS}}$  going low, the output pin remains open until the next CAS cycle. If WE goes low after Data reaches the output pin, the output pin is activated and retains the selected cell data as long as CAS remains low (regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ ). This late  $\overline{\text{WE}}$  pulse results in a READ-MODIFY-WRITE cycle. Data-in is latched when WE strobes low.

By holding RAS low, CAS may be toggled to execute

several faster READ, WRITE, READ-WRITE or READ-MODIFY-WRITE cycles within the RAS address defined PAGE boundary. Returning RAS high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the RAS high-time. Memory cell data is retained in its correct state by maintaining power and executing a RAS (Refresh) cycle so that all 256 combinations of RAS addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.



#### **FUNCTIONAL BLOCK DIAGRAM** PAGE MODE WRITE 0-DATA IN → D<sub>IN</sub> CAS . **BUFFER** NO. 2 CLOCK GENERATOR → D<sub>OUT</sub> DATA OUT BUFFER --- 1024 ---COLUMN ADDRESS COLUMN BUFFER (10) **DELODER** A 0 0-A 1 0---- 1024 ---REFRESH A 2 0-SENSE AMPLIFIERS I/O GATING CONTROLLER A 3 0-A 4 0---- 1024 ---A 5 0-REFRESH A 6 0-COUNTER A 7 0-A 8 0-۲۰۲ ROW DECODER MEMORY ROW 256 ARRAY ADDRESS 8 BUFFERS (9) ⊸ ν<sub>cc</sub> NO. 1 CLOCK RAS . GENERATOR **⊸** ۷<sub>SS</sub>

#### **FUNCTIONAL TRUTH TABLE**

F	540	010	WE	Addresses			NOTES
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Χ	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	٦	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	ROW COL		Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	



#### **ABSOLUTE MAXIMUM RATINGS\***

 \*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (0°C $\leq$ T $_{A}$ $\leq$ 70°C) (Vcc = 5.0V $\pm10\%$ )

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ VIN ≤ Vcc), all other pins not under test = 0 volts	lı	-10	10	μΑ	
OUTPUT LEAKAGE Output leakage current (Doυτ is disabled, 0V ≤ Voυτ ≤ Vcc)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High (Logic 1) voltage (Iout = -5mA) Output Low (Logic 0) voltage (Iout = 5mA)	Voh Vol	2.4	0.4	V	. 1

(Notes: 1,2,3,4,6) (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C) (Vcc = 5.0V  $\pm$ 10%) MAX PARAMETER/CONDITION SYMBOL -8 -10 -12 -15 UNITS NOTES 5 5 STANDBY CURRENT: TTL input levels lcc1 5 5 mΑ  $\overline{(RAS} = \overline{CAS} = V_{IH} \text{ after } 8 \overline{RAS} \text{ cycles})$ OPERATING CURRENT 65 55 55 45 mΑ 2 lcc2  $(\overline{RAS} \text{ and } \overline{CAS} = Cycling: trc = trc(MIN))$ OPERATING CURRENT: PAGE MODE 65 55 55 45 Icc<sub>3</sub> mA 2  $(\overline{RAS} = V_{IL}, \overline{CAS} = Cycling: tpc = tpc(MIN))$ REFRESH CURRENT: RAS ONLY 40 ICC4 55 40 35 mA 2 (RAS = Cycling: CAS = VIH: trc = trc(MIN)) REFRESH CURRENT: CAS-before-RAS 65 55 55 45 lcc<sub>5</sub> mΑ 2,20  $(\overline{RAS} \text{ and } \overline{CAS} = \text{cycling}, \text{ trc} = \text{trc}(MIN))$ 

#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As), DIN	C <sub>I1</sub>		5	pF	18
Input Capacitance RAS, CAS, WE	CI2		8	pF	18
Output Capacitance Dout	Co		7	pF	18



# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 3, 4, 5, 10, 11, 17, 18) (0°C $\leq$ T $_A$ $\leq$ 70°C) (Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS		-	8		10	-1	12	-	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	180		220		255		295		ns	
PAGE-MODE cycle time	<sup>t</sup> PC	75	i	90		100		120		ns	6, 7
Access time from RAS	t <sub>RAC</sub>		80		100		120		150	ns	7, 8
Access time from CAS	t <sub>CAC</sub>		40		50		60		75	ns	7, 9
RAS pulse width	t <sub>RAS</sub>	80	10,000	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	t <sub>RSH</sub>	40		50		60		75		ns	
RAS precharge time	<sup>t</sup> RP	60		80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	40	10,000	50	10,000	60	10,000	75	10,000	ns	
CAS hold time	t <sub>CSH</sub>	80		100		120		150		ns	
CAS precharge time	<sup>t</sup> CPN	20		25		25		30		ns	19
CAS precharge time (PAGE-MODE)	<sup>t</sup> CP	25		30		30		35		ns	
RAS to CAS delay time	tRCD	20	40	25	50	25	60	25	75	ns	13
CAS to RAS set-up time	tCRP	10		15		20		20		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		0		ns	
Row address hold time	t <sub>RAH</sub>	15		15		15		15		ns	
Column address set-up time	t <sub>ASC</sub>	0		0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		20		20		25		ns	
Column address hold time referenced to RAS	<sup>t</sup> AR	50		70		80		100		ns	
READ command set-up time	t <sub>RCS</sub>	0		0		0		0		ns	
READ command hold time referenced to CAS	<sup>t</sup> RCH	0		0		0		0		ns	14
READ command hold time referenced to RAS	t <sub>RRH</sub>	0		0		0		0		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	25	0	30	0	30	0	35	ns	12
WE command set-up time	twcs	0	1 -5	0	- 55	0	- 55	0	"	ns	16
WRITE command hold time	tWCH	15		35		40		45		ns	
WRITE command hold time referenced to RAS	tWCR	35		85		100		120		ns	
WRITE command pulse width	t <sub>WP</sub>	15		35		40		45		ns	
WRITE command to RAS lead time	t <sub>RWL</sub>	35		35		40		45		ns	
WRITE command to CAS lead time	tCWL	35		35		40		45		ns	
Data-in set-up time	t <sub>DS</sub>	0	T	0		0		0		ns	15
Data-in hold time	tDH	15		35		40	1	45		ns	15
Data-in hold time referenced to RAS	<sup>t</sup> DHR	35		85		100		120		ns	
CAS to WE delay	tCWD	30		40		50		60		ns	16
RAS to WE delay	t <sub>RWD</sub>	70		90		110		135	1	ns	16
Transition time (rise or fall)	t <sub>T</sub>	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	t <sub>REF</sub>		4		4		4		4	ms	21
CAS hold time (CAS-before-RAS refresh)	tCHR	15		20		25		30		ns	20

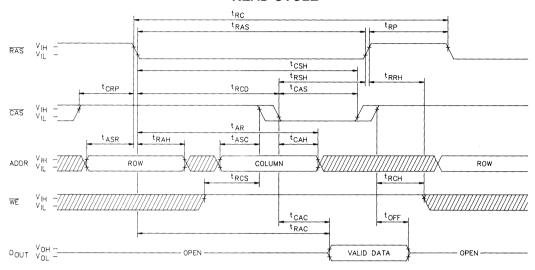
## MICHON

#### **NOTES**

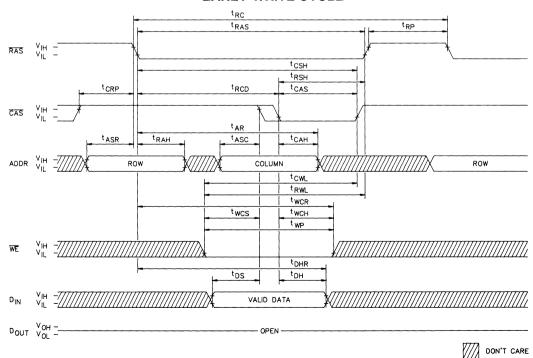
- 1. All voltages referenced to Vss.
- 2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of  $100\mu s$  is required after power-up followed by any  $8 \overline{RAS}$  cycles before proper device operation is assured. The  $8 \overline{RAS}$  cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
- 4. AC characteristics assume  ${}^{t}T = 5$ ns.
- 5. Vih min and Vil max are reference levels for measuring timing of input signals. Transition times are measured between Vih and Vil.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- 7. Measured with a load equivalent to 2 TTL gates and 100pF.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 9. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 10. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 11. If  $\overline{CAS} = VIL$ , data output may contain data from the last valid READ cycle.
- 12. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to Voн or Vol.
- 13. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is con-

- trolled exclusively by <sup>t</sup>CAC.
- 14. <sup>t</sup>RCH is referenced to the first rising edge of <del>RAS</del> or <del>CAS</del>.
- 15. These parameters are referenced to CAS leading edge in early WRITE cycles and to the WE leading edge in late WRITE or READ-MODIFY-WRITE cycles
- 16. tWCS, tCWD and tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (min) the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tCWD ≥ tCWD (min) and tRWD ≥ tRWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to VIH) is indeterminate.
- 17. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 18. Capacitance calculated from the equation  $C = \underline{I\Delta t} \Delta V$  with  $\Delta V = 3V$  and Vcc = 5V. This parameter is sampled.
- 19. If  $\overline{CAS}$  is low at the falling edge of  $\overline{RAS}$ , DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{CAS}$  must be pulsed high for <sup>t</sup>CP. Note 8 applies to determine valid data out.
- 20. On-chip refresh and address counters are enabled.
- 21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case WE = LOW.

#### **READ CYCLE**

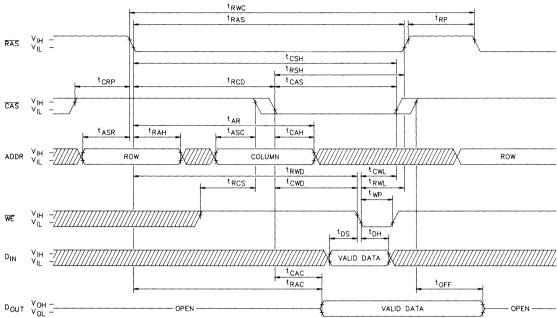


## **EARLY-WRITE CYCLE**



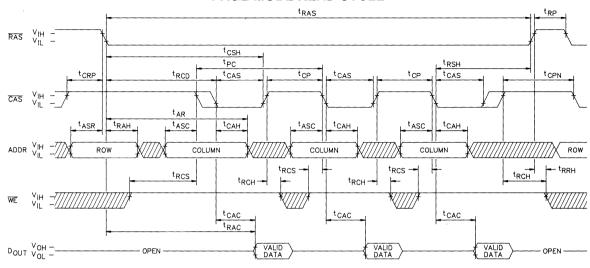


# READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE

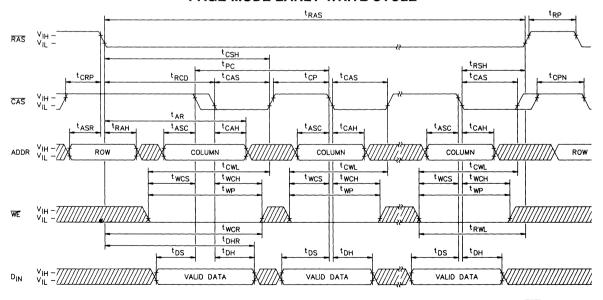


DON'T CARE

#### **PAGE-MODE READ CYCLE**



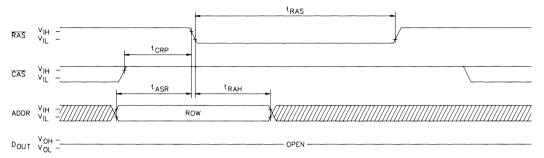
#### **PAGE-MODE EARLY-WRITE CYCLE**





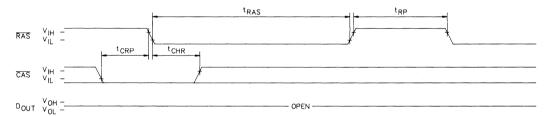
#### **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0 - A_7$ ;  $A_8$  and  $\overline{WE} = DON'T CARE.)$ 



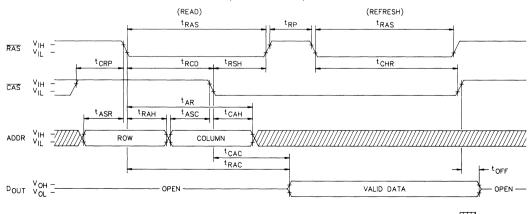
## **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_8 \overline{WE} = DON'T CARE.)$ 



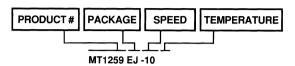
## **HIDDEN REFRESH CYCLE**

 $(\overline{WE} = HIGH)^{21}$ 



#### **ORDER INFORMATION**

256K x 1, 100ns in Plastic PLCC



The Micron MT1259 is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the NMOS double-poly

process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burnin and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

# DRAM

# 256K x 4 DRAM

FAST PAGE MODE

#### **FEATURES**

**OPTIONS** 

- Industry standard x4 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: RAS only, CAS before RAS, and Hidden

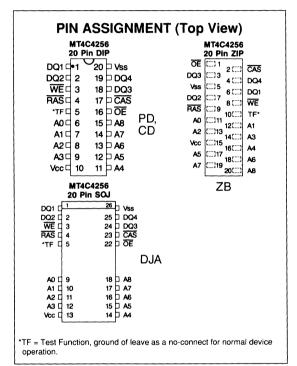
**MARKING** 

• Optional Fast Page Mode access cycle

<ul> <li>Timing</li> </ul>	
100ns access	-10
120ns access	-12
150ns access	-15
<ul> <li>Organization</li> </ul>	
256K x 4	MT4C4256
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

#### GENERAL DESCRIPTION

The MT4C4265 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. A READ or WRITE cycle is selected with the WE input. A logic high on WE dictates READ mode while a logic low on WE dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes low prior to CAS going low, the output pin(s) remain open (High Z) until the next CAS cycle. If WE goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as  $\overline{CAS}$  remains low (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin direction is controlled by WE and OE.



Returning  $\overline{RAS}$  and  $\overline{CAS}$  high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{RAS}$  cycle (READ, WRITE,  $\overline{RAS}$  only,  $\overline{CAS}$ -before- $\overline{RAS}$ , or Hidden refresh) so that all 512 combinations of  $\overline{RAS}$  addresses (A0-A8) are executed at least every 8ms, regardless of sequence

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The PAGEMODE cycle is always initiated with a row address strobed in by RAS followed by a column address strobed in by CAS. By holding RAS low, CAS may be toggled strobing in different column addresses executing faster memory cycles. Returning RAS high terminates the PAGEMODE operation.

#### **FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE** WRITE . DATA IN **⊸** I/O 1 CAS o-BUFFER **-0** 1/O 2 **-0** I/O 3 NO. 2 CLOCK GENERATOR DATA OUT **o** I/O 4 BUFFER --- 2048 ---- 🕽 🕽 • ŌE COLUMN ADDRESS BUFFER 9 COLUMN A 0 0-A 1 0---- 512x4 --REFRESH A 2 0-SENSE AMPLIFIERS CONTROLLER I/O GATING A 3 0-A 4 0-A 5 0-REFRESH A 6 0-COUNTER A 7 0-रुष्ट A 8 0-ROW DECODER MEMORY ROW ADDRESS 512 ARRAY BUFFERS (9) 9 ⊸ V<sub>CC</sub> NO. 1 CLOCK RAS -GENERATOR ∙o V<sub>SS</sub>

### **FUNCTIONAL TRUTH TABLE**

						Addre	esses		
Function	RAS	CAS	WE	ŌĒ	TF	tR	tC		NOTES
Standby	Н	Н	н	Н	GND/NC	Х	Х	High Impedance	
READ	L	L	Н	L	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	Н	GND/NC	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	Н	L	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	Н	GND/NC	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	н	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	Н	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Н	GND/NC	Х	Х	High Impedance	
TEST FUNCTION	L	L	Н	Н	Н	ROW	COL	Data Out, Test Funtion Mode	



#### ABSOLUTE MAXIMUM RATINGS\*

Voltage on Vcc supply relative to Vss1.0V to +7.0V
Operating Temperature, TA(Ambient)0°C to +70°C
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation 1 Watt
Short Circuit Output Current50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq$   $T_{\Delta}$   $\leq$  70°C, = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	Icc1		50	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS  Power supply standby current (RAS = CAS = VIH after 8 RAS cycles min.)	lcc3		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	Icc4		1	mA	
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vін)	lcc5		35	mA	3
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = Cycling)	lcc <sub>6</sub>		35	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ VIN ≤ Vcc), all other pins not under test = 0 volts)	lı	-10	10	μΑ	
OUTPUT LEAKAGE CURRENT (Dou⊤ is disabled, 0V ≤ Vouт ≤ Vcc)	loz	-10	10	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA)	Vон	2.4		V	1
Output Low voltage (lout = 5mA)	<b>V</b> ol		0.4	V	1

#### RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \le T_A \le 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1

### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9), DIN	C <sub>11</sub>		5	pF	2
Input Capacitance RAS, CAS, WE, OE	CI2		7	pF	2
Output Capacitance Dout	Co		7	pF	2

## **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13)  $(0^{\circ}C \le T_{A} \le +70^{\circ}C, Vcc = 5.0V \pm 10\%)$ 

A.C. CHARACTERISTICS	-10 -12		12		15				
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	190		220		260		ns	
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	220		255		295		ns	
PAGE-MODE READ or WRITE	t <sub>PC</sub>	55		70		85		ns	
cycle time									
Access time from RAS	t <sub>RAC</sub>		100		120		150	ns	14
Access time from CAS	tCAC		25		30		45	ns	15
Output Enable	<sup>t</sup> OE		25		25		30	ns	
Access time from column address	<sup>t</sup> AA		50		60		70	ns	
Access time from CAS precharge	t <sub>CPA</sub>		50		65		75	ns	
RAS pulse width	t <sub>RAS</sub>	100	10,000	120	10,000	150	10,000	ns	
RAS pulse width (PAGE MODE)	t <sub>RASP</sub>	100	100,000	120	100,000	150	100,000	ns	
RAS hold time	t <sub>RSH</sub>	25		30		45		ns	
RAS precharge time	<sup>t</sup> RP	80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	25	10,000	30	10,000	45	10,000	ns	
CAS hold time	t <sub>CSH</sub>	100		120		150		ns	
CAS precharge time	t <sub>CPN</sub>	15		20		25		ns	16
CAS precharge time (PAGE MODE)	<sup>t</sup> CP	10		15		20		ns	
RAS to CAS delay time	t <sub>RCD</sub>	10	75	15	90	15	105	ns	17
CAS to RAS precharge time	t <sub>CRP</sub>	10		10		10		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		ns	
Row address hold time	t <sub>RAH</sub>	10		15		15		ns	
RAS to column address delay time	<sup>t</sup> RAD	10	50	15	60	15	70	ns	18
Column address set-up time	†ASC	0		0		0	<b>†</b>	ns	
Column address hold time	t <sub>CAH</sub>	15		20	1	25		ns	
Column address hold time (referenced to RAS)	t <sub>AR</sub>	60		70		80		ns	
Column address to RAS lead time	<sup>t</sup> RAL	50		60		70		ns	
Read command set-up time	<sup>t</sup> RCS	0		0		0		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19
CAS to output in low-Z	t <sub>CLZ</sub>	5		5		5		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	25	0	25	0	30	ns	20
Output Disable	t <sub>OD</sub>		25		25		30	ns	



# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq$ T $_A$ $\leq$ +70°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS	-10			_	12		15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command set-up time	tWCS	0		0		0		ns	21
Write command hold time	twcH	20		25		30		ns	
Write command hold time (referenced to RAS)	tWCR	70		80		90		ns	
Write command pulse width	t <sub>WP</sub>	20		25		30		ns	
Write command to RAS lead time	t <sub>RWL</sub>	25		30		35		ns	
Write command to CAS lead time	tCWL	25		30		35		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	22
Data-in hold time	HD	15		20		25		ns	22
Data-in hold time (referenced to RAS)	<sup>t</sup> DHR	70		80		90		ns	i
RAS to WE delay time	t <sub>RWD</sub>	120		150		185		ns	21
Column address to WE delay time	<sup>t</sup> AWD	80		100		120		ns	21
CAS to WE delay time	tCWD	65		75		85		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		8		8		8	ms	
RAS to CAS Precharge time	t <sub>RPC</sub>	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	tCHR	20		25		30		ns	5

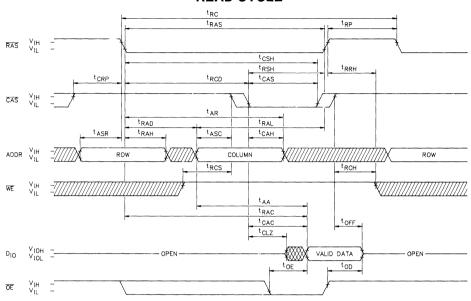
#### **NOTES**

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and Vcc = 5V.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range  $(0^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq 70^{\circ}\text{C})$  is assured.
- An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>) in a monotonic manner.
- 11. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 12. If  $\overline{CAS} = V_{1L}$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If CAS is low at the falling edge of RAS, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CPN.

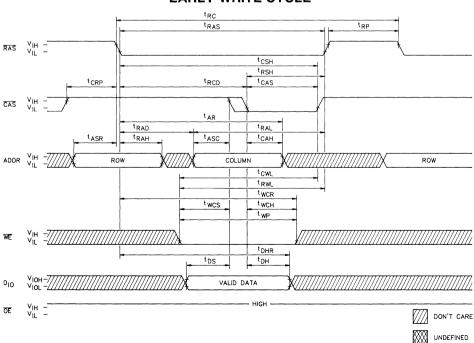
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- 19. Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 21. <sup>t</sup>WCS, <sup>t</sup>RWD, <sup>t</sup>AWD and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), <sup>t</sup>AWD ≥ <sup>t</sup>AWD (min) and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to Vih) is indeterminate.
- 22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles and  $\overline{\text{WE}}$  leading edge in late WRITE or READ-WRITE cycles.
- 23. During a READ cycle, if OE is LOW then taken HIGH DOUT goes open. If OE is tied permanently low a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case WE = LOW and OE=HIGH.



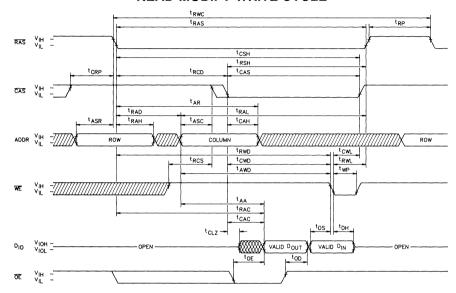
#### **READ CYCLE**



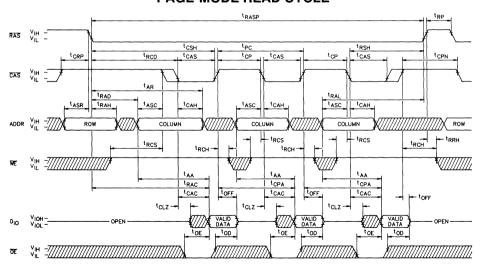
#### **EARLY-WRITE CYCLE**



# READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE



#### PAGE-MODE READ CYCLE

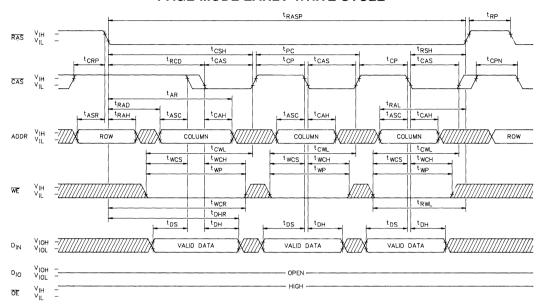


DON'T CARE

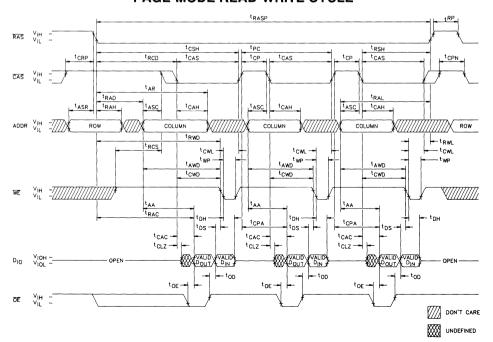




#### PAGE-MODE EARLY-WRITE CYCLE



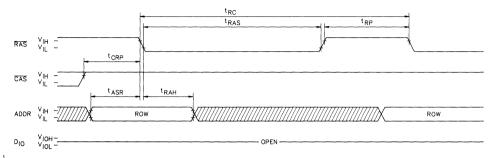
#### PAGE-MODE READ-WRITE CYCLE



# MICRON

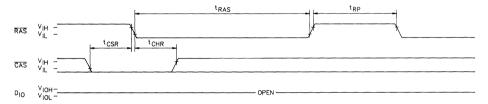
#### **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0 - A_8$ ;  $A_9$  and  $\overline{WE}$  = DON'T CARE.)



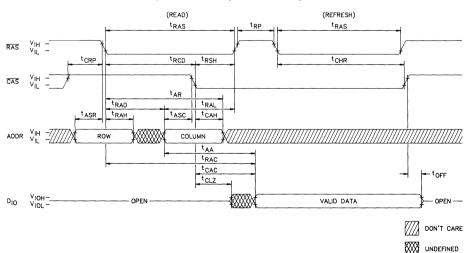
## **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_0, \overline{WE} \text{ and } \overline{OE} = DON'T CARE)$ 



### **HIDDEN REFRESH CYCLE**

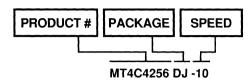
 $(\overline{WE} = HIGH); \overline{OE} = LOW)^{24}$ 





#### ORDER INFORMATION

256K x 4, 120ns in Plastic DJ



The Micron 1 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS

silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.


# DRAM

# 256K x 4 DRAM

STATIC COLUMN

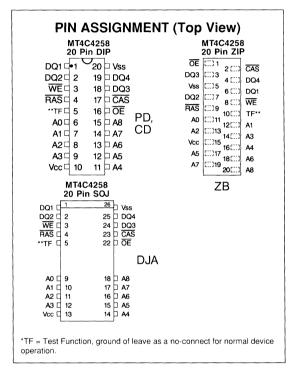
#### **FEATURES**

- Industry standard x4 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- · All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: RAS only, CAS before RAS, and Hidden
- Optional Static Column access cycle

OPTIONS	MARKING
<ul> <li>Timing</li> </ul>	
100ns access	-10
120ns access	-12
150ns access	-15
<ul> <li>Organization</li> </ul>	
256K x 4	MT4C4258
<ul> <li>Packages</li> </ul>	
Plastic DIP	None
Ceramic DIP	С
Plastic ZIP	Z
Plastic SOI	DI

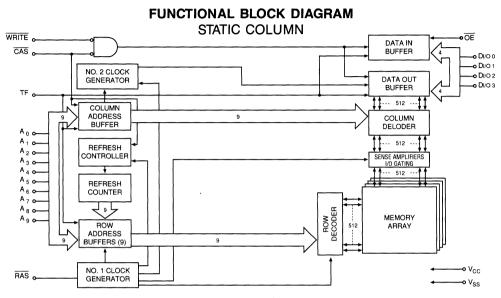
#### GENERAL DESCRIPTION

The MT4C4258 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time.  $\overline{RAS}$  is used to latch the first 9 bits and CAS the latter 9 bits. A READ or WRITE cycle is selected with the WE input. A logic high on WE dictates READ mode while a logic low on WE dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes low prior to CAS going low, the output pin(s) remain open (High Z) until the next CAS cycle. If WE goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as CAS remains low (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin direction is controlled by  $\overline{WE}$  and  $\overline{OE}$ .



Returning RAS and CAS high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS only, CAS-before-RAS, or Hidden refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless

STATIC COLUMN operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed in by RAS followed by a column address strobed in by CAS. By holding RAS low, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning RAS high terminates the STATIC COLUMN operation.



#### **FUNCTIONAL TRUTH TABLE**

						Addre	esses		
Function	RAS	CAS	WE	ŌĒ	TF	tR	tC		NOTES
Standby	Н	Н	Н	Н	GND/NC	Х	Х	High Impedance	
READ	L	L	Н	L	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	Н	GND/NC	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
STATIC COLUMN READ	L	L	Н	L	GND/NC	ROW	COL→COL	Valid Data Out, Valid Data Out	
STATIC COLUMN WRITE	L	L	L	Н	GND/NC	ROW	COL→COL	Valid Data In, Valid Data In	
STATIC COLUMN READ-WRITE	L	L	H→L→H	L→H	GND/NC	ROW	COL→COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	Н	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	Н	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Н	GND/NC	Х	Х	High Impedance	
TEST FUNCTION	L	L	Н	Н	Н	ROW	COL	Data Out, Test Funtion Mode	



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on VCC supply relative to Vss	1.0V to +7.0V
Operating Temperature, TA(Ambient)	
Storage Temperature (Ceramic)	65°C to +150°C
Storage Temperature (Plastic)	55°C to +150°C
Power Dissipation	1 Watt
Short Circuit Output Current	50m A

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq$   $T_{A} \leq$  70°C, = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc1		50	mA	3, 4
OPERATING CURRENT: STATIC COLUMN (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS  Power supply standby current (RAS = CAS = VIH  after 8 RAS cycles min.)	lcc3		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	Icc4		1	mA	
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = VIH)	lcc5		35	mA	3
REFRESH CURRENT: $\overline{CAS}$ -before- $\overline{RAS}$ ( $\overline{RAS}$ and $\overline{CAS}$ = Cycling)	Icc6		35	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ VIN ≤ Vcc), all other pins not under test = 0 volts)	lı	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dour is disabled, 0V ≤ Vour ≤ Vcc)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High voltage (Iouт = -5mA)	Vон	2.4		V	1
Output Low voltage (lout = 5mA)	Vol		0.4	V	

### RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{{\color{blue}A}} \leq 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1

#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9), DIN	CI1		5	pF	2
Input Capacitance RAS, CAS, WE, OE	C12		7	pF	2
Output Capacitance Dout	Co		7	pF	2

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq$ T $_A$ $\leq$ +70°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS	-10		-12		-	15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	190		220		260		ns	
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	220		255		295		ns	
Access time from RAS	t <sub>RAC</sub>		100		120		150	ns	14
Access time from CAS	t <sub>CAC</sub>		25		30		45	ns	15
Output Enable	<sup>t</sup> OE		25		25		30	ns	
Access time from column address	<sup>t</sup> AA		50		60		70	ns	
Access time from CAS precharge	<sup>t</sup> CPA		50		65		75	ns	
RAS pulse width	t <sub>RAS</sub>	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	t <sub>RSH</sub>	25		30		45		ns	
RAS precharge time	t <sub>RP</sub>	80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	25	10,000	30	10,000	45	10,000	ns	
CAS hold time	t <sub>CSH</sub>	100		120		150		ns	
CAS precharge time	t <sub>CPN</sub>	15		20		25		ns	16
RAS to CAS delay time	t <sub>RCD</sub>	10	75	15	90	15	105	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	10		15		15		ns	
RAS to column	<sup>t</sup> RAD	10	50	15	60	15	70	ns	18
address delay time									
Column address set-up time	t <sub>ASC</sub>	0		0		0		ns	
Column address hold time	tCAH_	15		20		25		ns	
Column address hold time (referenced to RAS)	<sup>t</sup> AR	60		70		80		ns	
Column address to RAS lead time	<sup>t</sup> RAL	50		60		. 70		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19
CAS to output in low-Z	tCLZ	5		5		5		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	25	0	25	0	30	ns	20
Output Disable	tOD		25		25		30	ns	
WE command set-up time	twcs	0		0		0		ns	21
Write command hold time	tWCH	20		25		30		ns	



#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ( $0^{\circ}$ C  $\leq$  T<sub>A</sub>  $\leq$  +70 $^{\circ}$ C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS		-	10	-12		-	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCR	70		80		90		ns	
(referenced to RAS)					1				
Write command pulse width	<sup>t</sup> WP	20		25		30		ns	
Write command to RAS lead time	<sup>t</sup> RWL	25		30		35		ns	
Write command to CAS lead time	tCWL	25		30		35		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	22
Data-in hold time	t <sub>DH</sub>	15		20		25		ns	22
Data-in hold time (referenced to RAS)	<sup>t</sup> DHR	70		80		90		ns	
RAS to WE delay time	t <sub>RWD</sub>	120		150		185		ns	21
Column address to WE delay time	<sup>t</sup> AWD	80		100		120		ns	21
CAS to WE delay time	tCWD	65		80		95		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		8		8		8	ms	
RAS to CAS Precharge time	t <sub>RPC</sub>	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	t <sub>CSR</sub>	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	<sup>t</sup> CHR	20		25		30		ns	5
STATIC COLUMN MODE cycle time	<sup>t</sup> SC	55		65		75		ns	
RAS pulse width (STATIC COLUMN)	<sup>t</sup> RASC	100	100,000	120	100,000	150	100,000	ns	
CAS precharge time (STATIC COLUMN)	<sup>t</sup> CP	10		15		20		ns	
STATIC COLUMN READ-MODIFY- WRITE cycle time	<sup>t</sup> SRMW	135		160		185		ns	
Last write to column address delay time	<sup>t</sup> LWAD	25	45	30	55	45	70	ns	
Last write to column address hold time	<sup>t</sup> AHLW		95		115		135	ns	
RAS hold time referenced to OE	<sup>t</sup> ROH	20		20		20		ns	
Output data hold time from column address	<sup>t</sup> AOH	5	_	5	_	5	_	ns	
Output data enable from write	tow		30		35		40	ns	
OE to data delay	<sup>t</sup> OED	25		30		35		ns	
OE command hold time	<sup>t</sup> OEH	25		25		30		ns	
Access time from last write	<sup>t</sup> ALW		95		115		140	ns	

## MICHON

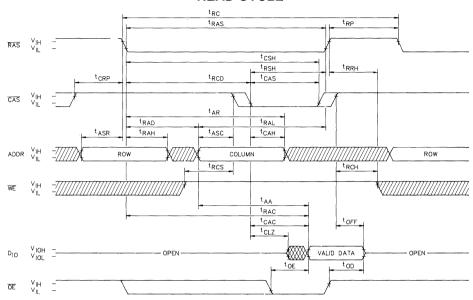
#### **NOTES**

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and  $V_{CC} = 5V$ .
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VII. and VIH) in a monotonic manner.
- 11. If  $\overline{CAS} = VIH$ , data output is high impedance.
- 12. If  $\overline{\text{CAS}} = \text{Vil.}$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If CAS is low at the falling edge of RAS, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CPN.

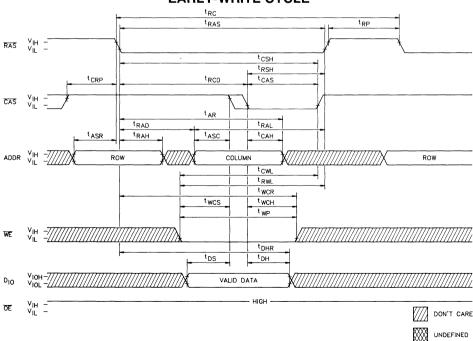
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- 19. Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to Voh ot Vol.
- 21. <sup>t</sup>WCS, <sup>t</sup>RWD, <sup>t</sup>AWD and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), <sup>t</sup>AWD ≥ <sup>t</sup>AWD (min) and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to VIH) is indeterminate.
- 22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles and  $\overline{\text{WE}}$  leading edge in late WRITE or READ-WRITE cycles.
- 23. During a READ cycle, if OE is LOW then taken HIGH DOUT goes open. If OE is tied permanently low a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case WE = LOW and OE=HIGH.



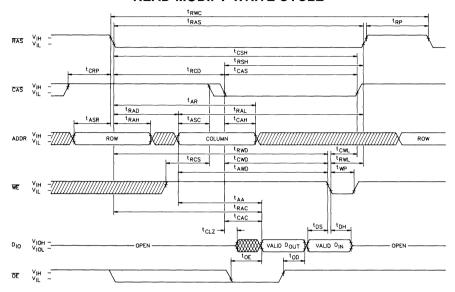
### **READ CYCLE**



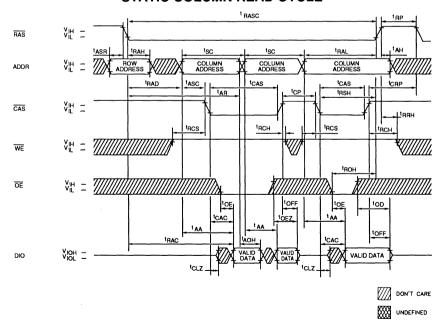
## **EARLY-WRITE CYCLE**



# READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE

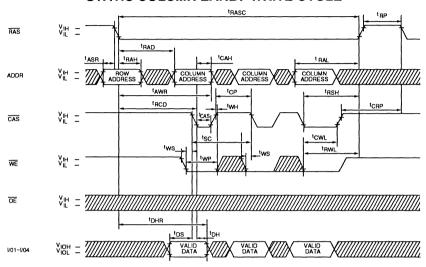


#### STATIC COLUMN READ CYCLE

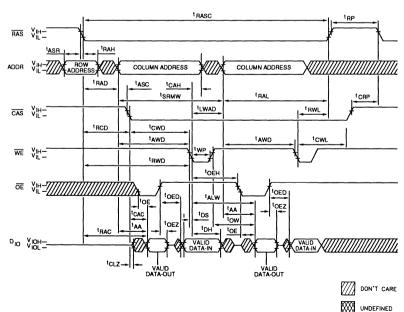




#### STATIC COLUMN EARLY-WRITE CYCLE



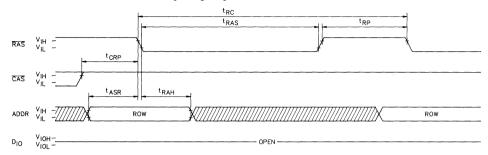
#### STATIC COLUMN READ-WRITE CYCLE



# MICHON

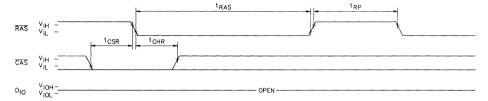
### **RAS ONLY REFRESH CYCLE**

 $(ADDR = A_0 - A_8; A_9 \text{ and } \overline{WE} = DON'T \text{ CARE.})$ 



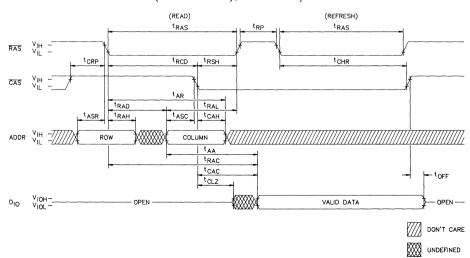
#### CAS-BEFORE-RAS REFRESH CYCLE

 $(A_0 - A_0, \overline{WE} \text{ and } \overline{OE} = DON'T CARE)$ 



### **HIDDEN REFRESH CYCLE**

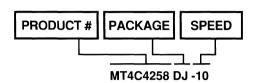
 $(\overline{WE} = HIGH); \overline{OE} = LOW)^{24}$ 





#### ORDER INFORMATION

256K x 4, 120ns in Plastic DJ



The Micron 1 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS

silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

# **DRAM**

# 1MEG x 1 DRAM

**FAST PAGE MODE** 

#### **FEATURES**

ODTIONS

- Industry standard x1 pin-out, timing, functions and packages
- · High performance CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: RAS only, CAS before RAS, and Hidden

MADEINIC

• Optional Fast Page Mode access cycle

OFTIONS	MAKKING
<ul> <li>Timing</li> </ul>	
100ns access	-10
120ns access	-12
150ns access	-15
<ul> <li>Organization</li> </ul>	
1 MEG x 1	MT4C1024
• Packages	
Plastic DIP	None
Ceramic DIP	С
Plastic ZIP	Z
Plastic SOJ	DJ

### GENERAL DESCRIPTION

The MT4C1024 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time.  $\overline{RAS}$  is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic high on WE dictates READ mode while a logic low on WE dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. If  $\overline{\text{WE}}$ goes low prior to CAS going low, the output pin(s) remain open (High Z) until the next CAS cycle. If WE goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as CAS remains low (regardless of  $\overline{WE}$  or  $\overline{RAS}$ ). This late  $\overline{WE}$  pulse results in a READ-WRITE cycle.

Returning RAS and CAS high terminates a memory

PIN ASSIGNMENT (Top View) MT4C1024 18 Pin DIP 20 Pin ZIP \* A9 Din □•1 18 🗆 Vss [:::3]1 2 :::: CAS :::13 WEd 2 17 Dout Dout 4 []] Vss Din []]5 RAS 3 16 CAS 6 [... WE RAS :::37 \*\*TF 🖒 4 15 A9 \* 8 []] TF\*\* PC. 10(11) NC NC A0 ☐ 5 14 🗆 A8 CC A0 A1 4 6 13 A7 [::]11 12[:] A1 [::]13 14[:] A3 A2 A2 7 12 1 A6 1315 16(11) A4 11317 18(11) A6 11319 20(11) A8 Vcc A3 🗆 8 11 1 A5 **A**5 Vcc □ 9 10 \( \bar{2} \) A4 MT4C1024 ZB 20 Pin SOJ 26 Vss Din 🗗 25 Dout 24 CAS 23 NC 22 A9\* WE 🗆 2 RAS | 3 "TF [ 5 DJA 18 A8 17 A7 16 A6 15 A5 14 A4 A0 🗆 9 A1 🗆 10 A2 🗆 11 A3 🗆 12 Vcc 🗆 13 \*Address not used for RAS only refresh \*\*TF = Test Function, ground of leave as a no-connect for normal device operation

cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{RAS}$  cycle (READ, WRITE,  $\overline{RAS}$  only,  $\overline{CAS}$ -before- $\overline{RAS}$ , or Hidden refresh) so that all 512 combinations of  $\overline{RAS}$  addresses (A0-A8) are executed at least every 8ms, regardless of sequence

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by RAS followed by a column address strobed in by CAS. By holding RAS low, CAS may be toggled strobing in different column addresses executing faster memory cycles. Returning RAS high terminates the PAGE MODE operation.

#### **FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE** WRITE . DATA IN BUFFER o D<sub>IN</sub> CAS o NO. 2 CLOCK GENERATOR ⊸ D<sub>OUT</sub> DATA OUT **BUFFER** 2048 ---- 1 COLUMN ADDRESS BUFFER (10) 10 COLUMN DELODER A 0 0-A 1 0-2048 ----REFRESH A 2 0-SENSE AMPLIFIERS CONTROLLER A 3 0-A 4 0-A 5 0---- 2048 ---REFRESH COUNTER A 6 0-A 7 0-A 8 0-ROW DECODER MEMORY A 9 0-ROW 512 ARRAY ADDRESS 10 BUFFERS (10) NO. 1 CLOCK GENERATOR ∙ V<sub>CC</sub> RAS \_\_ ⊸ V<sub>SS</sub>

### **FUNCTIONAL TRUTH TABLE**

					Addre	esses		
Function	RAS	CAS	WE	TF	tR	tC		NOTES
Standby	Н	Н	Н	GND/NC	Х	Х	High Impedance	
READ	L	L	Н	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	Н	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	GND/NC	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	GND/NC	Х	Х	High Impedance	
TEST FUNCTION	L	L	н	Н	ROW	COL	Data Out, Test Funtion Mode	



### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V to +7.0V
Operating Temperature, TA(Ambient)0°C to +70°C
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation 1 Watt
Short Circuit Output Current50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc1		50	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS  Power supply standby current (RAS = CAS = VIH  after 8 RAS cycles min.)	lcc3		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	lcc4		1	mA	
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih)	lcc5		35	mA	3
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = Cycling)	Icc6		35	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ VIN ≤ Vcc), all other pins not under test = 0 volts)	lı	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dour is disabled, 0V ≤ Vour ≤ Vcc)	loz	-10	10	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA)	<b>V</b> oн	2.4		V	1
Output Low voltage (lout = 5mA)	<b>V</b> OL		0.4	V	

# RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \le T_{\Delta} \le 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1



# **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9), DIN	CI1		5	pF	2
Input Capacitance RAS, CAS, WE	CI2		7	рF	2
Output Capacitance Dout	Co		7	рF	2

# **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$  T<sub>A</sub>  $\leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS		-	10		-12		-15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	190		220		260		ns	
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	220		255		295		ns	
PAGE-MODE READ or WRITE	<sup>t</sup> PC	55		70		85		ns	
cycle time									
Access time from RAS	t <sub>RAC</sub>		100		120		150	ns	14
Access time from CAS	<sup>t</sup> CAC		25		30		45	ns	15
Access time from column address	<sup>t</sup> AA		50		60		70	ns	
Access time from CAS precharge	t <sub>CPA</sub>		50		65		75	ns	
RAS pulse width	t <sub>RAS</sub>	100	10,000	120	10,000	150	10,000	ns	
RAS pulse width (PAGE MODE)	<sup>t</sup> RASP	100	100,000	120	100,000	150	100,000	ns	
RAS hold time	t <sub>RSH</sub>	25		30		45		ns	
RAS precharge time	<sup>t</sup> RP	80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	25	10,000	30	10,000	45	10,000	ns	
CAS hold time	t <sub>CSH</sub>	100		120		150		ns	
CAS precharge time	t <sub>CPN</sub>	15		20		25		ns	16
CAS precharge time (PAGE MODE)	<sup>t</sup> CP	10		15		20		ns	
RAS to CAS delay time	t <sub>RCD</sub>	10	75	15	90	15	105	ns	17
CAS to RAS precharge time	t <sub>CRP</sub>	10		10		10		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	10		15		15		ns	
RAS to column	t <sub>RAD</sub>	10	50	15	60	15	70	ns	18
address delay time						!			
Column address set-up time	tASC	00		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		20		25		ns	
Column address hold time	t <sub>AR</sub>	60		70		80		ns	
(referenced to RAS)									
Column address to	t <sub>RAL</sub>	50		60		70		ns	
RAS lead time									
Read command set-up time	tRCS	00		0		0		ns	
Read command hold time	t <sub>RCH</sub>	0		0		0		ns	19
(referenced to CAS)									
Read command hold time	<sup>t</sup> RRH	0		0		0		ns	19
(referenced to RAS)									
CAS to output in low-Z	t <sub>CLZ</sub>	5		5		5		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	25	0	25	0	30	ns	20
WE command set-up time	twcs	0		0		0		ns	21
Write command hold time	tWCH	20		25		30		ns	



# **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq T_{\Delta} \leq +70$ °C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS		-1	10		12		15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time (referenced to RAS)	tWCR	70		80		90		ns	
Write command pulse width	<sup>t</sup> WP	20		25		30		ns	
Write command to RAS lead time	t <sub>RWL</sub>	25		30		35		ns	
Write command to CAS lead time	tCWL	25		30		35		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	22
Data-in hold time	t <sub>DH</sub>	15		20		25		ns	22
Data-in hold time (referenced to RAS)	t <sub>DHR</sub>	70		80		90		ns	
RAS to WE delay time	t <sub>RWD</sub>	90		110		135		ns	21
Column address to WE delay time	<sup>t</sup> AWD	50		60		70		ns	21
CAS to WE delay time	tCWD	25		30		45		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		8		8		8	ms	
RAS to CAS Precharge time	t <sub>RPC</sub>	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	t <sub>CSR</sub>	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	tCHR	20		25		30		ns	5

#### NOTES

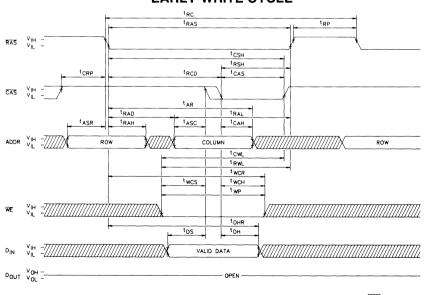
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and VCC = 5V.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 12. If  $\overline{\text{CAS}} = \text{Vil}$ , data output may contain data from the last valid READ cycle.
- Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If  $\overline{CAS}$  is low at the falling edge of  $\overline{RAS}$ , DOUT will

- be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for  ${}^{\text{t}}\text{CPN}$ .
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 21. <sup>t</sup>WCS, <sup>t</sup>RWD, <sup>t</sup>AWD and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), <sup>t</sup>AWD ≥ <sup>t</sup>AWD (min) and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to Vih) is indeterminate
- 22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles and  $\overline{\text{WE}}$  leading edge in late WRITE or READ-WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{WE} = LOW$ .

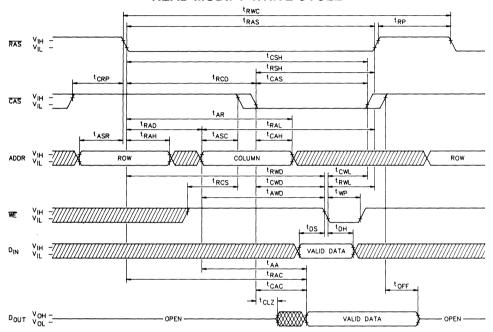


### **READ CYCLE** t<sub>CSH</sub> t<sub>RSH</sub> t CRP t<sub>RCD</sub> tCAS t AR t<sub>RAD</sub> t<sub>RAL</sub> t<sub>RAH</sub> tASC t<sub>CAH</sub> t ASR COLUMN t<sub>RCS</sub> <sup>t</sup>RCH t<sub>AA</sub> t<sub>RAC</sub> tCAC t OFF t<sub>CLZ</sub> DOUT VOH -- OPEN VALID DATA OPEN -

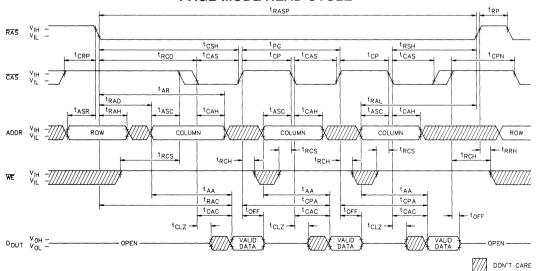
### **EARLY-WRITE CYCLE**



## **READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE**

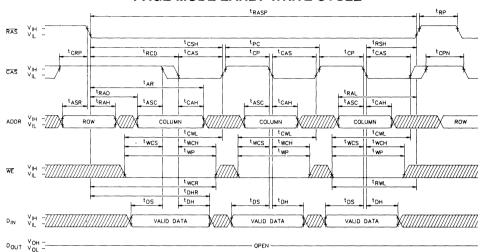


### PAGE-MODE READ CYCLE

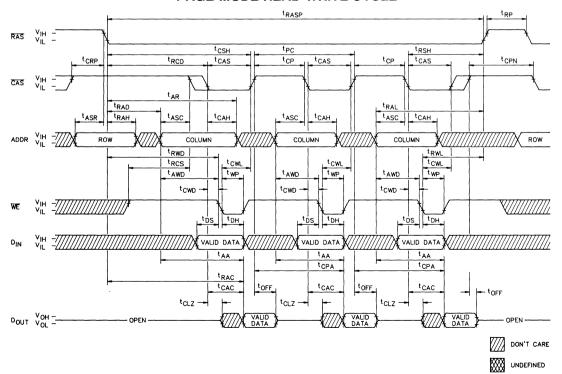




### PAGE-MODE EARLY-WRITE CYCLE

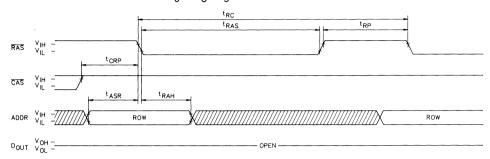


### PAGE-MODE READ-WRITE CYCLE



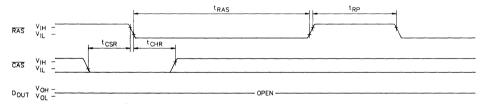
### **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0 - A_8$ ;  $A_9$  and  $\overline{WE} = DON'T CARE.)$ 



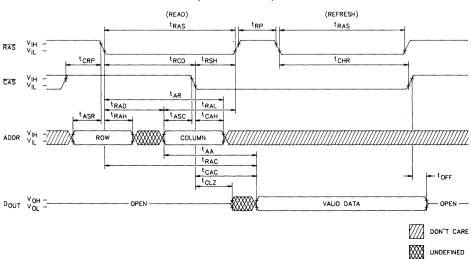
# CAS-BEFORE-RAS REFRESH CYCLE

 $(A_0 - A_9 \text{ and } \overline{WE} = DON'T CARE)$ 



# **HIDDEN REFRESH CYCLE**

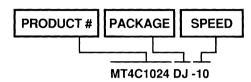
 $(\overline{WE} = HIGH)$ 





### ORDER INFORMATION

1 MEG x 1, 100ns in Plastic SOJ



The Micron 1 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS

silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

			*	



# DRAM

# 1MEG x 1 DRAM

NIBBLE MODE

#### **FEATURES**

**OPTIONS** 

- Industry standard x1 pin-out, timing, functions and packages.
- High performance CMOS silicon gate process.
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: RAS only, CAS before RAS, and Hidden

MARKING

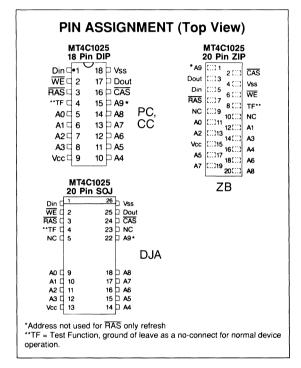
• Optional Nibble Mode access cycle

<ul> <li>Timing</li> </ul>	
100ns access	-10
120ns access	-12
150ns access	-15
Organization	
1 MEG x 1	MT4C1025
• Packages	
Plastic DIP	None
Ceramic DIP	С
Plastic ZIP	Z
Plastic SOJ	DI

#### **GENERAL DESCRIPTION**

The MT4C1025 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time.  $\overline{RAS}$  is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic high on WE dictates READ mode while a logic low on WE dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. If  $\overline{\text{WE}}$ goes low prior to CAS going low, the output pin(s) remain open (High Z) until the next CAS cycle. If WE goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as CAS remains low (regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ ). This late  $\overline{\text{WE}}$  pulse results in a READ-WRITE cycle.

Returning RAS and CAS high terminates a memory



cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{RAS}$  cycle (READ, WRITE,  $\overline{RAS}$  only,  $\overline{CAS}$ -before- $\overline{RAS}$ , or Hidden refresh) so that all 512 combinations of  $\overline{RAS}$  addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

Nibble Mode operation allows faster sequential serial data operations (READ, WRITE or READ-MODIFY-WRITE) on up to 4 bits. The first of 4 bits is accessed in the usual manner with  $\overline{CAS}$  address A9 (nibble MSB) and RAS address A9 (nibble LSB) selecting on of 4 bits within a nibble for initial access. By holding  $\overline{RAS}$  low,

CAS can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around (see below).

CA<sub>9</sub> RA<sub>9</sub> (0,0) (0,1) (1,0) (1,1)

**⊸** ∨<sub>SS</sub>

#### **FUNCTIONAL BLOCK DIAGRAM** NIBBLE MODE WRITE . DATA IN ⊸ D<sub>IN</sub> CAS . BUFFER NO. 2 CLOCK → D<sub>OUT</sub> DATA OUT GENERATOR BUFFER COLUMN NIBBLE SELECTOR ADDRESS 10 COLUMN BUFFER (10) DELODER A 0 0-A 1 0-2048 ----REFRESH A 2 0-CONTROLLER SENSE AMPLIFIERS A 3 o-A 4 0---- 2048 ---A 5 0-REFRESH A 6 0-COUNTER A 7 0-ROW DECODER A 8 0-MEMORY A 9 0-ROW 512 ARRAY ADDRESS 9 BUFFERS (10) NO. 1 CLOCK ⊸ V<sub>CC</sub> RAS \_\_

# **FUNCTIONAL TRUTH TABLE**

GENERATOR

			-		Addre	esses		
Function	RAS	CAS	WE	TF	tR	tC		NOTES
Standby	Н	Н	Н	GND/NC	Х	Х	High Impedance	
READ	L	L	Н	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
NIBBLE READ	L	H→L→H	Н	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
NIBBLE WRITE	L	H→L→H	L	GND/NC	ROW	COL	Valid Data In, Valid Data In	
NIBBLE READ-WRITE	L	H→L→H	H→L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	GND/NC	Х	Х	High Impedance	
TEST FUNCTION	L	L	Н	Н	ROW	COL	Data Out, Test Funtion Mode	



### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V to +7.0V
Operating Temperature, TA(Ambient) 0°C to +70°C
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation1 Watt
Short Circuit Output Current 50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq$  T  $_{A} \leq$  70°C = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc1		50	mA	3, 4
OPERATING CURRENT: NIBBLE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS  Power supply standby current (RAS = CAS = VIH  after 8 RAS cycles min.)	lcc3		4	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	Icc4		1	mA	
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih)	lcc5		35	mA	3
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = Cycling)	lcc <sub>6</sub>		35	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ VIN ≤ Vcc), all other pins not under test ≈ 0 volts)	lı	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dou⊤ is disabled, 0V ≤ Vouт ≤ Vcc)	loz	-10	10	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA)	Vон	2.4	0.4	V	1
Output Low voltage (Iout = 5mA)	Vol		0.4	1V	1

# RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \le T_{\Delta} \le 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1

# **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9), DIN	C <sub>11</sub>		5	pF	2
Input Capacitance RAS, CAS, WE	C12		7	pF	2
Output Capacitance Dout	Co		7	pF	2

# **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$   $T_A \leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS			10	-	12	-	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	190		220		260		ns	
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	220		255		295		ns	
Access time from RAS	t <sub>RAC</sub>		100		120		150	ns	14
Access time from CAS	tCAC		25		30		45	ns	15
Access time from column address	<sup>t</sup> AA		50		60		70	ns	
Access time from CAS precharge	<sup>t</sup> CPA		50		65		75	ns	
RAS pulse width	<sup>t</sup> RAS	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	t <sub>RSH</sub>	25		30		45		ns	
RAS precharge time	t <sub>RP</sub>	80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	25	10,000	30	10,000	45	10,000	ns	
CAS hold time	tCSH	100		120		150		ns	
CAS precharge time	t <sub>CPN</sub>	15		20		25		ns	16
RAS to CAS delay time	<sup>t</sup> RCD	10	75	15	90	15	105	ns	17
CAS to RAS precharge time	t <sub>CRP</sub>	10		10		10		ns	
Row address set-up time	tasr.	0		0		0		ns	
Row address hold time	t <sub>RAH</sub>	10		15		15		ns	
RAS to column	t <sub>RAD</sub>	10	50	15	60	15	70	ns	18
address delay time									
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		20		25		ns	
Column address hold time (referenced to RAS)	<sup>t</sup> AR	60		70		80		ns	
Column address to RAS lead time	<sup>t</sup> RAL	50		60		70		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19
CAS to output in low-Z	tCLZ	5		5		5		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	25	0	25	0	30	ns	20
WE command set-up time	twcs	0		0		0		ns	21
Write command hold time	tWCH	20		25		30		ns	
Write command hold time (referenced to RAS)	tWCR	70		80		90		ns	
Write command pulse width	tWP	20		25		30		ns	



# **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq T_A \leq +70$ °C, Vcc =  $5.0V \pm 10\%$ )

A.C. CHARACTERISTICS		-	10	-12		-	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command to RAS lead time	t <sub>RWL</sub>	25		30		35		ns	
Write command to CAS lead time	t <sub>CWL</sub>	25		30		35		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	22
Data-in hold time	t <sub>DH</sub>	15		20		25		ns	22
Data-in hold time (referenced to RAS)	<sup>t</sup> DHR	70		80		90		ns	
RAS to WE delay time	<sup>t</sup> RWD	90		110		135		ns	21
Column address to WE delay time	<sup>t</sup> AWD	50		60		70		ns	21
CAS to WE delay time	tCWD	35		40		45		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		8		8		8	ms	
RAS to CAS Precharge time	<sup>t</sup> RPC	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	t <sub>CSR</sub>	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	<sup>t</sup> CHR	20		25		30		ns	5
RAS pulse width (NIBBLE MODE)	<sup>t</sup> RASN	100	100,000	120	100,000	150	100,000	ns	
CAS precharge time (NIBBLE MODE)	<sup>t</sup> NCP	10		15		20		ns	
NIBBLE MODE cycle time	<sup>t</sup> NC	35		40		45		ns	
NIBBLE MODE READ-MODIFY- WRITE cycle time	<sup>t</sup> NRWC	55		65		75		ns	
NIBBLE MODE access time	<sup>t</sup> NCAC	15		20		25		ns	15
NIBBLE MODE pulse width	tNCAS	15		20		25		ns	
NIBBLE MODE CAS precharge time	tNCP	10		10		10		ns	
NIBBLE MODE RAS hold time	<sup>t</sup> NRSH	15		20		25		ns	
NIBBLE MODE CAS to WRITE delay time	tNCWD	15		20		25		ns	
NIBBLE MODE WRITE command to RAS lead time	<sup>t</sup> NRWL	15		20		25		ns	
NIBBLE MODE WRITE command to CAS lead time	<sup>t</sup> NCWL	15		20		25		ns	

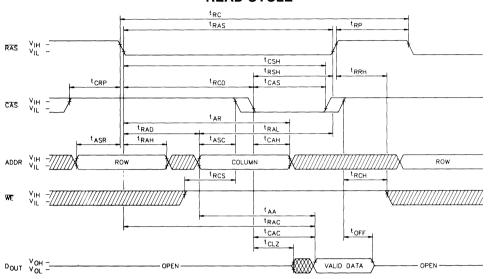
#### NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and Vcc = 5V
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>) in a monotonic manner.
- 11. If  $\overline{CAS}$  = ViH, data output is high impedance.
- 12. If  $\overline{\text{CAS}} = \text{Vil.}$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If  $\overline{CAS}$  is low at the falling edge of  $\overline{RAS}$ , Dout will

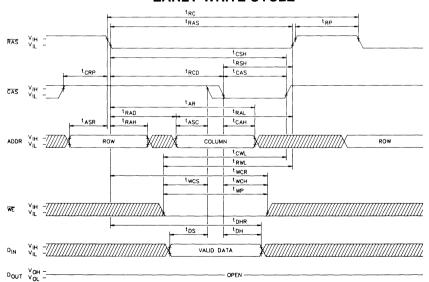
- be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for  ${}^{\text{t}}\text{CPN}$ .
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle.
- 20. OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 21. <sup>t</sup>WCS, <sup>t</sup>RWD, <sup>t</sup>AWD and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), <sup>t</sup>AWD ≥ <sup>t</sup>AWD (min) and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to Vih) is indeterminate.
- 22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles and  $\overline{\text{WE}}$  leading edge in late WRITE or READ-WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{WE} = LOW$ .



### READ CYCLE



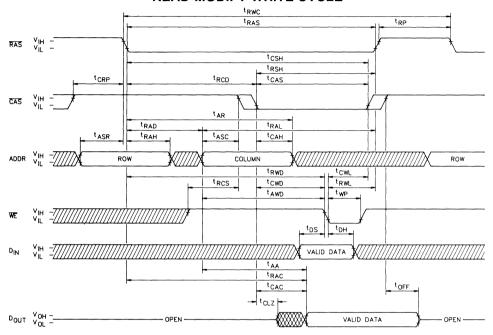
# **EARLY-WRITE CYCLE**



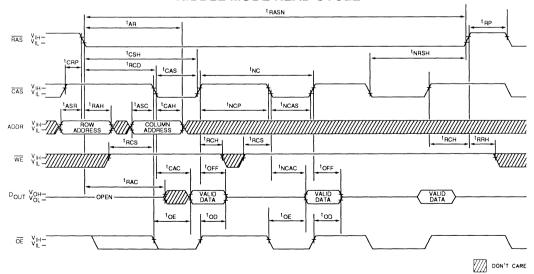
DON'T CARE

UNDEFINED

# READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE

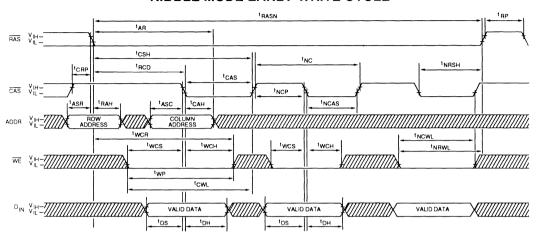


### **NIBBLE MODE READ CYCLE**

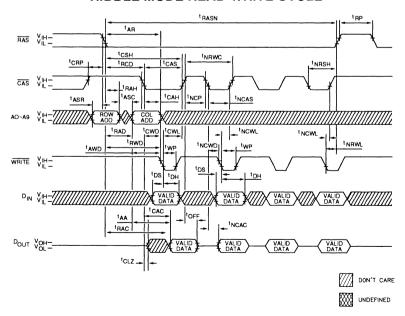




### **NIBBLE MODE EARLY-WRITE CYCLE**

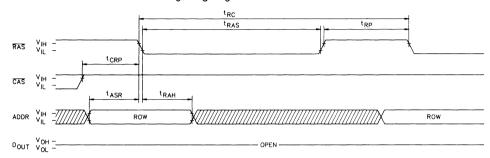


### **NIBBLE MODE READ-WRITE CYCLE**



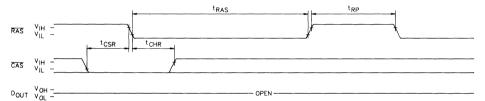
### **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0$  -  $A_8$ ;  $A_9$  and  $\overline{WE}$  = DON'T CARE.)



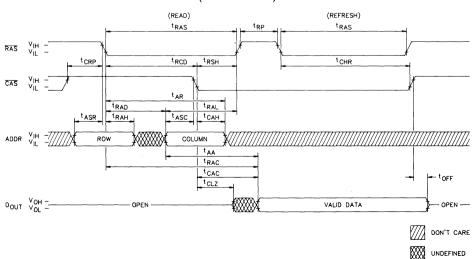
# **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_9 \text{ and } \overline{WE} = DON'T CARE)$ 



### **HIDDEN REFRESH CYCLE**

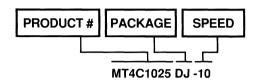
 $(\overline{WE} = HIGH)$ 



# MICRON

### **ORDER INFORMATION**

1 MEG x 1, 100ns in Plastic SOJ



The Micron 1 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS

silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

# DRAM

# 1MEG x 1 DRAM

STATIC COLUMN

#### **FEATURES**

OPTIONS

- Industry standard x1 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: RAS only, CAS before RAS, and Hidden

NAA DIZINIO

• Optional Static Column access cycle

MAKKING
-10
-12
-15
MT4C1026
None
С
Z
DJ

### **GENERAL DESCRIPTION**

The MT4C1026 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic high on WE dictates READ mode while a logic low on WE dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes low prior to CAS going low, the output pin(s) remain open (High Z) until the next CAS cycle. If WE goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as CAS remains low (regardless of  $\overline{WE}$  or  $\overline{RAS}$ ). This late  $\overline{WE}$  pulse results in a READ-WRITE cycle.

Returning  $\overline{RAS}$  and  $\overline{CAS}$  high terminates a memory

PIN ASSIGNMENT (Top View) MT4C1026 18 Pin DIP 20 Pin ZIP 0 18 □ Vss Din □•1 \*A9 []] 1 2 []] CAS Dout £:::3 17 Dout WE 2 4 []] Vss Din [:::35 RAS 3 16 CAS 6 :::: WE RAS 0037 ..TF ☐ 4 15 A9 \* 8 (III) TF\*\* PC, C:::39 NC A0 □ 5 14 🗅 A8 10:00 NC CC A0 E::311 A1 ☐ 6 13 \( \bar{A7} A2 [[]]13 14[]] A3 A2 7 12 A6 Vcc [:::15 14(:::) A3 A5 [:::17 18(:::) A6 A7 [:::19 20(:::) A8 A3 □ 8 11 A5 Vcc 🗆 10 A4 MT4C1026 ZB 20 Pin SOJ Din 1 26 Vss 25 Dout 24 CAS WE C 2 RAS 0 3 NC 0 5 DJA A0 4 9 18 D A8 A1 [ 10 A2 [ 11 17 A7 16 A6 15 A5 \*Address not used for RAS only refresh \*\*TF = Test Function, ground of leave as a no-connect for normal device operation.

cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{RAS}$  cycle (READ, WRITE,  $\overline{RAS}$  only,  $\overline{CAS}$ -before- $\overline{RAS}$ , or Hidden refresh) so that all 512 combinations of  $\overline{RAS}$  addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

STATIC COLUMN operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0 - A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed in by RAS followed by a column address strobed in by CAS. By holding RAS low, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning RAS high terminates the STATIC COLUMN operation.



#### **FUNCTIONAL BLOCK DIAGRAM** STATIC COLUMN WRITE a DATA IN → D<sub>IN</sub> CAS . NO. 2 CLOCK → D<sub>OUT</sub> DATA OUT GENERATOR BUFFER 2048 ---- 1 COLUMN ADDRESS 10 COLUMN BUFFER (10) DELODER A 0 0-A 1 0-REFRESH A 2 0-SENSE AMPLIFIERS CONTROLLER A 3 o-A 4 0---- 2048 ---A 5 o-REFRESH A 6 0-COUNTER A 7 o-A 8 0-ROW DECODER MEMORY A 9 0-ROW ARRAY 512 ADDRESS 9 10 BUFFERS (10) ⊸ V<sub>CC</sub> NO. 1 CLOCK GENERATOR RAS . ⊸ V<sub>SS</sub>

### **FUNCTIONAL TRUTH TABLE**

					Addr	esses		
Function	RAS	CAS	WE	TF	tR	tC		NOTES
Standby	Н	Н	Н	GND/NC	Х	Х	High Impedance	
READ	L	L	Н	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
STATIC COLUMN READ	L	L	Н	GND/NC	ROW	COL→COL	Valid Data Out, Valid Data Out	
STATIC COLUMN WRITE	L	L	L	GND/NC	ROW	COL→COL	Valid Data In, Valid Data Out	
STATIC COLUMN READ-WRITE	L	L	H→L→H	GND/NC	ROW	COL→COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	GND/NC	Х	х	High Impedance	
TEST FUNCTION	L	L	Н	н	ROW	COL	Data Out, Test Funtion Mode	



### **ABSOLUTE MAXIMUM RATINGS\***

77 to
Voltage on VCC supply relative to Vss1.0V to +7.0V
Operating Temperature, TA(Ambient)0°C to +70°C
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation 1 Wat
Short Circuit Output Current 50m/

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc <sub>1</sub>		50	mA	3, 4
OPERATING CURRENT: STATIC COLUMN (RAS = VIL, CAS = VIL, Addr. = Cycling, tpc = tpc(MIN))	lcc2		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS  Power supply standby current (RAS = CAS = VIH  after 8 RAS cycles min.)	lcc3		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	Icc4		1	mA	
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = VIH)	lcc5		35	mA	3
REFRESH CURRENT: $\overline{CAS}$ -before- $\overline{RAS}$ ( $\overline{RAS}$ and $\overline{CAS}$ = Cycling)	Icc6		35	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ VIN ≤ Vcc), all other pins not under test = 0 volts)	lı .	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dou⊤ is disabled, 0V ≤ Vouт ≤ Vcc)	loz	-10	10	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA) Output Low voltage (lout = -5mA)	Vон	2.4	0.4	V	1
Output Low voltage (lout = 5mA)	Vol	1	0.4	V	

# RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{{\color{blue}A}} \leq 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	VIH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1



### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9), DIN	CI1,		5	pF	2
Input Capacitance RAS, CAS, WE	C <sub>12</sub>		7	pF	2
Output Capacitance Dout	Co		7	pF	2

# **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$  T<sub>A</sub>  $\leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS		-	10	-	12	-	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	190		220		260		ns	
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	220		255		295		ns	
Access time from RAS	<sup>t</sup> RAC		100		120		150	ns	14
Access time from CAS	t <sub>CAC</sub>		25		30		45	ns	15
Access time from column address	<sup>t</sup> AA		50		60		70	ns	
Access time from CAS precharge	<sup>t</sup> CPA		50		65		75	ns	
RAS pulse width	t <sub>RAS</sub>	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	<sup>t</sup> RSH	25		30		45		ns	
RAS precharge time	t <sub>RP</sub>	80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	25	10,000	30	10,000	45	10,000	ns	
CAS hold time	tCSH	100		120		150		ns	
CAS precharge time	tCPN	15		20		25		ns	16
RAS to CAS delay time	t <sub>RCD</sub>	10	75	15	90	15	105	ns	17
CAS to RAS precharge time	t <sub>CRP</sub>	10		10		10		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	10		15		15		ns	
RAS to column	t <sub>RAD</sub>	10	50	15	60	15	70	ns	18
address delay time									
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		20		25		ns	
Column address hold time (referenced to RAS)	<sup>t</sup> AR	60		70		80		ns	
Column address to RAS lead time	<sup>t</sup> RAL	50		60		70		ns	
Read command set-up time	t <sub>RCS</sub>	0		0		0		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19
CAS to output in low-Z	tCLZ	5		5		5		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	25	0	25	0	30	ns	20
WE command set-up time	twcs	0		0		0		ns	21
Write command hold time	tWCH	20		25		30		ns	
Write command hold time (referenced to RAS)	tWCR	70		80		90		ns	



# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq$ T $_A$ $\leq$ +70°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS PARAMETER		-	-10		-12		-15		
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command pulse width	<sup>t</sup> WP	20		25		30		ns	
Write command to RAS lead time	t <sub>RWL</sub>	25		30		35		ns	
Write command to CAS lead time	tCWL	25		30		35		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	22
Data-in hold time	t <sub>DH</sub>	15		20		25		ns	22
Data-in hold time (referenced to RAS)	<sup>t</sup> DHR	70		80		90		ns	
RAS to WE delay time	t <sub>RWD</sub>	90		110		135		ns	21
Column address to WE delay time	<sup>t</sup> AWD	50		60		70		ns	21
CAS to WE delay time	tCWD	25		30		45		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		8		8		8	ms	
RAS to CAS Precharge time	t <sub>RPC</sub>	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	<sup>t</sup> CSR	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	<sup>t</sup> CHR	20		25		30		ns	5
RAS pulse width (STATIC COLUMN)	<sup>t</sup> RASC	100	100,000	120	100,000	150	100,000	ns	
CAS precharge time (STATIC COLUMN)	<sup>t</sup> CP	10		15		20		ns	
STATIC COLUMN MODE cycle time	tsc	55		65		75		ns	
STATIC COLUMN READ-MODIFY- WRITE cycle time	<sup>t</sup> SRMW	135		160		185		ns	
Last Write to column address delay time	<sup>t</sup> LWAD	25	45	30	55	45	70	ns	
Last Write to column address hold time	<sup>t</sup> AHLW		95		115		135	ns	
RAS hold time referenced to OE	<sup>t</sup> ROH	20		20		20		ns	
Output data hold time from column address	<sup>t</sup> AOH	5	_	5	_	5	_	ns	
Output data enable from Write	tow		25	_	25	_	25	ns	

#### NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and  $V_{CC} = 5V$ .
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIL and VIH) in a monotonic manner.
- 11. If  $\overline{CAS}$  = ViH, data output is high impedance.
- 12. If CAS = VIL, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If  $\overline{CAS}$  is low at the falling edge of  $\overline{RAS}$ , DOUT will

- be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for  ${}^{\text{t}}\text{CPN}$ .
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle.
- 20. tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 21. <sup>t</sup>WCS, <sup>t</sup>RWD, <sup>t</sup>AWD and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), <sup>t</sup>AWD ≥ <sup>t</sup>AWD (min) and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to Vih) is indeterminate
- 22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles and  $\overline{\text{WE}}$  leading edge in late WRITE or READ-WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{WE} = LOW$ .

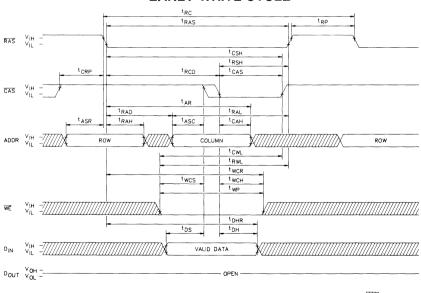


### **READ CYCLE** tRAS tRP t<sub>CSH</sub> t<sub>RSH</sub> <sup>t</sup> RRH tCAS t CRP tRCD tRAD tRAL t ASR tRAH tASC t<sub>CAH</sub> tRCH t<sub>RCS</sub> $t_{AA}$ tRAC tCAC t OFF t<sub>CLZ</sub> DOUT VOL -

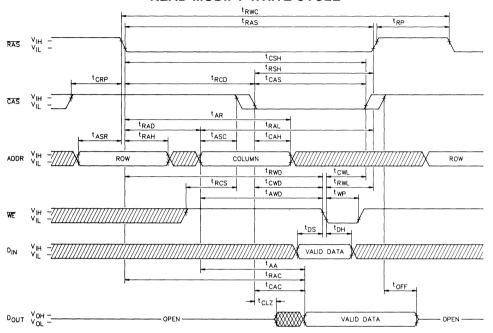
### **EARLY-WRITE CYCLE**

VALID DATA

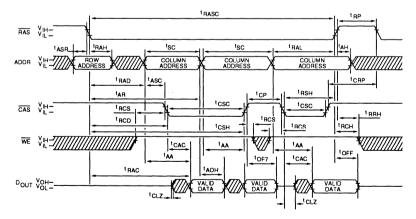
OPEN -



# READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE



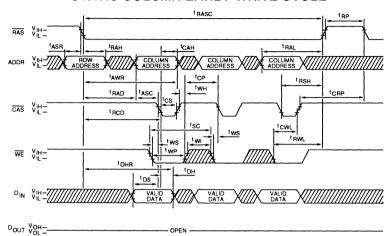
# STATIC COLUMN READ CYCLE



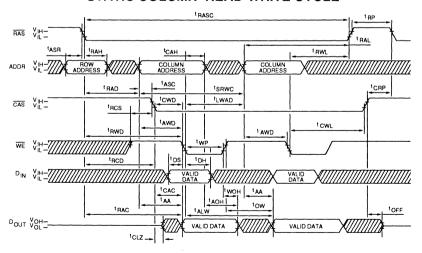




### STATIC COLUMN EARLY-WRITE CYCLE



### STATIC COLUMN READ-WRITE CYCLE

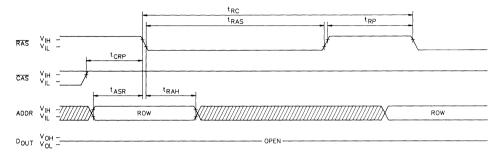




# MICHON

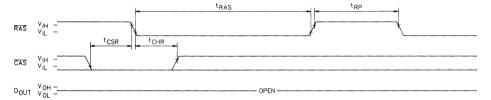
### **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0$  -  $A_8$ ;  $A_9$  and  $\overline{WE}$  = DON'T CARE.)



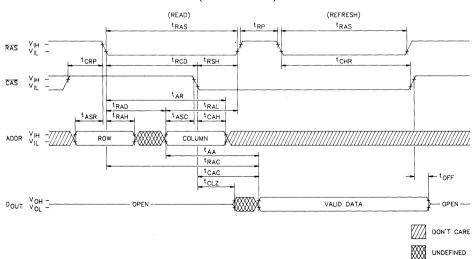
## CAS-BEFORE-RAS REFRESH CYCLE

 $(A_0 - A_9 \text{ and } \overline{WE} = DON'T CARE)$ 



# **HIDDEN REFRESH CYCLE**

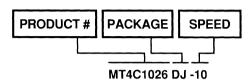
 $(\overline{WE} = HIGH)$ 





### ORDER INFORMATION

1 MEG x 1, 100ns in Plastic SOJ



The Micron 1 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS

silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

## MICRON

## **DRAM**

## 1MEG x 4 DRAM

**FAST PAGE MODE** 

#### **FEATURES**

**OPTIONS** 

- Industry standard x4 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024 cycle refresh distributed across 16ms
- Refresh modes: RAS only, CAS before RAS, and Hidden

**MARKING** 

Optional Fast Page Mode access cycle

<ul> <li>Timing 80ns access</li> <li>100ns access</li> <li>120ns access</li> <li>Organization</li> <li>1 MEG x 4</li> </ul>	-8 -10 -12 MT4C4001
<ul> <li>Packages         Plastic DIP         Ceramic DIP         Plastic ZIP         Plastic SOJ     </li> </ul>	None C Z DJ

#### **GENERAL DESCRIPTION**

The MT4C4001 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time.  $\overline{RAS}$  is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the  $\overline{\mathrm{WE}}$  input. A logic high on  $\overline{\mathrm{WE}}$  dictates READ mode while a logic low on WE dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. If  $\overline{\text{WE}}$ goes low prior to CAS going low, the output pin(s) remain open (High Z) until the next CAS cycle. If WE goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as CAS remains low (regardless of  $\overline{WE}$  or  $\overline{RAS}$ ). This late  $\overline{WE}$  pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin

# PIN ASSIGNMENT (Top View)

MT4C4 20 Pin			T4C4001 Pin ZIP
DQ1 = 1 2 DQ2 = 2 WE = 3 RAS = 4 A9 = 5 A0 = 6 A1 = 7 A2 = 8	DIP 20   Vss 19   DQ4 18   DQ3 17   CAS 16   OE 15   A8 14   A7 13   A6 12   A5	OE C DQ3 C Vss C DQ2 C RAS C A0 C A2 C Vcc C	7 Pin ZIP  2 C CAS  3 4 C DO4  35 6 C DO1  37 8 C WE  39 10 A9  311 12 A1  315 16 C A3  317 18 C A4  317 18 C A6
Vcc□ 10	11 A4	A7 [:	20[]] A8



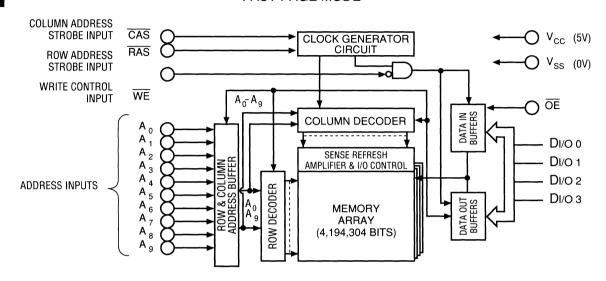
NOTE: Package Information To Be Determined.

direction is controlled by  $\overline{WE}$  and  $\overline{OE}$ .

Returning  $\overline{RAS}$  and  $\overline{CAS}$  high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{RAS}$  cycle (READ, WRITE,  $\overline{RAS}$  only,  $\overline{CAS}$ -before- $\overline{RAS}$ , or Hidden refresh) so that all 1024 combinations of  $\overline{RAS}$  addresses (A0-A9) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by RAS followed by a column address strobed in by CAS. By holding RAS low, CAS may be toggled strobing in different column addresses executing faster memory cycles. Returning RAS high terminates the PAGE MODE operation.

#### FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE



#### **FUNCTIONAL TRUTH TABLE**

				Addre	esses		
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE MODE READ	L	H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
PAGE MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	

## MICHON

## MT4C4001

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V to +7.0V
Operating Temperature, Ta(Ambient)0°C to +70°C
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation 1 Watt
Short Circuit Output Current 50m A

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq$   $T_{\mbox{\scriptsize A}} \leq$  70°C, = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: tac = tac(MIN))	lcc1		60	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS  Power supply standby current (RAS = CAS = VIH  after 8 RAS cycles min.)	lcc3		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	ICC4		0.5	mA	
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih)	lcc5		60	mA	3
REFRESH CURRENT: $\overline{CAS}$ -before- $\overline{RAS}$ ( $\overline{RAS}$ and $\overline{CAS}$ = Cycling)	Icc6		60	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ VIN ≤ Vcc), all other pins not under test = 0 volts)	(ı	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ Vout ≤ Vcc)	loz	-10	10	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA)	Vон	2.4		V	1
Output Low voltage (lout = 5mA)	Vol	1	0.4	V	

### RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{{\color{blue}A}} \leq 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VıL	-1.0	0.8	٧	1

#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9), DIN	C <sub>11</sub>		5	pF	2
Input Capacitance RAS, CAS, WE, OE	C12		7	pF	2
Output Capacitance Dout	Co		7	pF	2

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq$ T<sub>A</sub> $\leq$ +70°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS	-8			-10	-12			1	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	160		190		220		ns	
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	185		220		295		ns	
PAGE-MODE READ or WRITE	<sup>t</sup> PC	50		55		70		ns	
cycle time									
Access time from RAS	tRAC		80		100		120	ns	14
Access time from CAS	tCAC_		20		25		35	ns	15
Output Enable	<sup>t</sup> OE		25		25		30	ns	
Access time from column address	<sup>t</sup> AA		40		50		60	ns	
Access time from CAS precharge	<sup>t</sup> CPA		40		50		65	ns	
RAS pulse width	<sup>t</sup> RAS	80	10,000	100	10,000	120	10,000	ns	
RAS pulse width (PAGE MODE)	<sup>t</sup> RASP	80	100,000	100	100,000	120	100,000	ns	
RAS hold time	<sup>t</sup> RSH	20		25		35		ns	
RAS precharge time	<sup>t</sup> RP	70		80		90		ns	
CAS pulse width	t <sub>CAS</sub>	20	10,000	25	10,000	35	10,000	ns	
CAS hold time	tCSH	80		100		120		ns	
CAS precharge time	<sup>t</sup> CPN	10		15		20		ns	16
CAS precharge time (PAGE MODE)	<sup>t</sup> CP	10	25	10	25	15		ns	
RAS to CAS delay time	<sup>t</sup> RCD	10	60	10	75	25	85	ns	17
CAS to RAS precharge time	t <sub>CRP</sub>	10		10		10		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		'ns	
Row address hold time	t <sub>RAH</sub>	10		10		15		ns	
RAS to column	t <sub>RAD</sub>	10	40	10	50	15		ns	18
address delay time									
Column address set-up time	tASC	0_		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		15		25		ns	
Column address hold time (referenced to RAS)	t <sub>AR</sub>	50		60		90		ns	
Column address to RAS lead time	<sup>t</sup> RAL	40		50		60		ns	
Read command set-up time	t <sub>RCS</sub>	0		0		0		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19
CAS to output in low-Z	t <sub>CLZ</sub>	5		5		5		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	25	0	25	0	25	ns	20
Output Disable	tOD		25		25	30	25	ns	



MT4C4001

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$  T<sub>A</sub>  $\leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

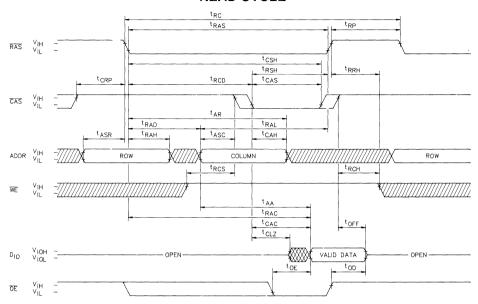
A.C. CHARACTERISTICS			-8		10	-1	2		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command set-up time	twcs	0		0		0		ns	21
Write command hold time	twcH	15		20		25		ns	
FAST PAGE MODE READ- MODIFY-WRITE cycle time	<sup>t</sup> PRWC	75		90		140		ns	
Write command hold time (referenced to RAS)	tWCR	60		70		90		ns	
Write command pulse width	t <sub>WP</sub>	15		20		25		ns	
Write command to RAS lead time	<sup>t</sup> RWL	20		25		30		ns	
Write command to CAS lead time	tCWL	20		25		30		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	22
Data-in hold time	t <sub>DH</sub>	15		15		25		ns	22
Data-in hold time (referenced to RAS)	t <sub>DHR</sub>	60		70		90		ns	
RAS to WE delay time	t <sub>RWD</sub>	90		120		160		ns	21
Column address to WE delay time	<sup>t</sup> AWD	70		80		100		ns	21
CAS to WE delay time	tCWD	50		65		75		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		8		8		8	ms	
RAS to CAS Precharge time	t <sub>RPC</sub>	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	t <sub>CHR</sub>	15		20		15		ns	5

#### **NOTES**

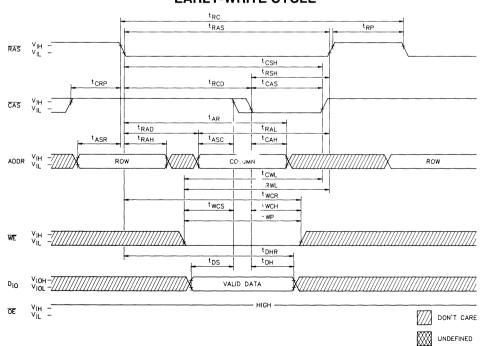
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and  $V_{CC} = 5V$
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 12. If  $\overline{\text{CAS}} = \text{V}_{1L}$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If  $\overline{\text{CAS}}$  is low at the falling edge of  $\overline{\text{RAS}}$ , DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for <sup>t</sup>CPN.

- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- 19. Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to Voh ot Vol.
- 21. <sup>t</sup>WCS, <sup>t</sup>RWD, <sup>t</sup>AWD and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), <sup>t</sup>AWD ≥ <sup>t</sup>AWD (min) and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to VIH) is indeterminate.
- 22. These parameters are referenced to CAS leading edge in early WRITE cycles and WE leading edge in late WRITE or READ-WRITE cycles.
- 23. During a READ cycle, if  $\overline{OE}$  is LOW then taken HIGH DOUT goes open. If  $\overline{OE}$  is tied permanently low a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case WE = LOW and OE=HIGH.

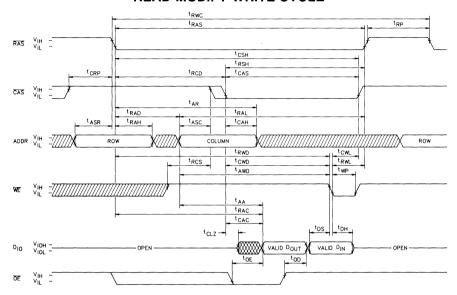
#### **READ CYCLE**



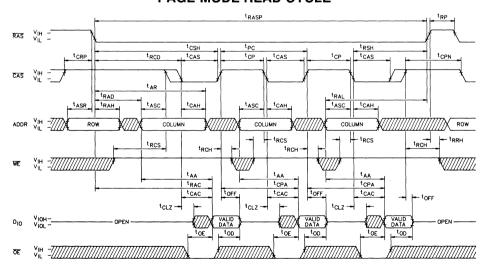
#### **EARLY-WRITE CYCLE**



# READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE



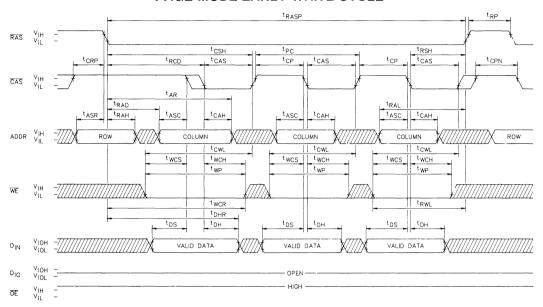
#### **PAGE-MODE READ CYCLE**



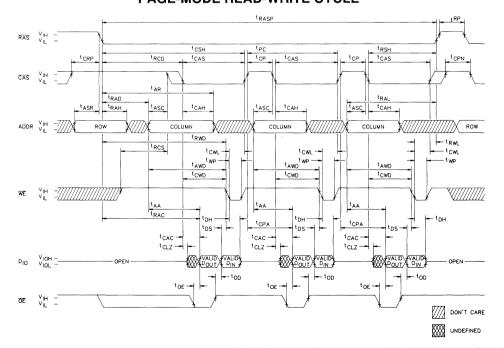




#### PAGE-MODE EARLY-WRITE CYCLE

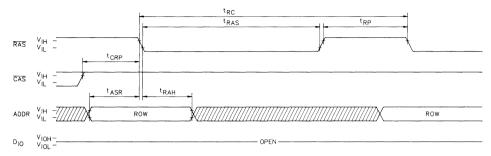


#### PAGE-MODE READ-WRITE CYCLE



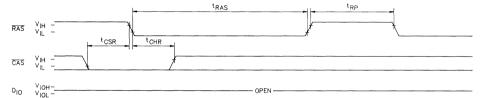
## **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0$  -  $A_8$ ;  $A_9$  and  $\overline{WE}$  = DON'T CARE.)



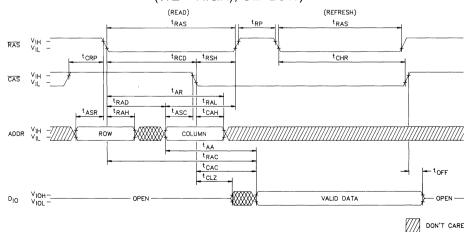
#### CAS-BEFORE-RAS REFRESH CYCLE

 $(A_0 - A_9, \overline{WE} \text{ and } \overline{OE} = DON'T CARE)$ 



#### **HIDDEN REFRESH CYCLE**

 $(\overline{WE} = HIGH); \overline{OE} = LOW)^{24}$ 

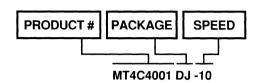


MICHON

MT4C4001

#### ORDER INFORMATION

1MEG x 4, 100ns in Plastic DJ



The Micron 4 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS

silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

## **DRAM**

# 1MEG x 4 DRAM

STATIC COLUMN

#### **FEATURES**

OPTIONS

- Industry standard x4 pin-out, timing, functions and packages.
- High performance CMOS silicon gate process.
- Single +5V±10% power supply.
- Low power, 5mW standby, 175mW active, typical.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- 1024 cycle refresh distributed across 16ms.
- Refresh modes: RAS only, CAS before RAS, and Hidden.

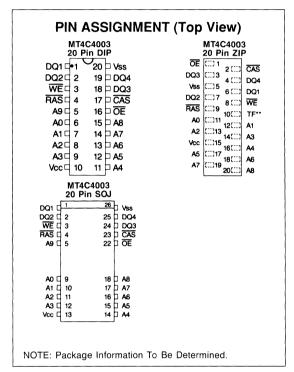
MARKING

• Optional Static Column access cycle.

OFTIONS	MAKKING
<ul> <li>Timing</li> </ul>	
80ns access	-8
100ns access	-10
120ns access	-12
<ul> <li>Organization</li> </ul>	
1 MEG x 4	MT4C4003
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

#### GENERAL DESCRIPTION

The MT4C4003 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time.  $\overline{RAS}$  is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic high on WE dictates READ mode while a logic low on WE dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. If  $\overline{\text{WE}}$ goes low prior to  $\overline{CAS}$  going low, the output pin(s) remain open (High Z) until the next CAS cycle. If WE goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as CAS remains low (regardless of  $\overline{WE}$  or  $\overline{RAS}$ ). This late  $\overline{WE}$  pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin

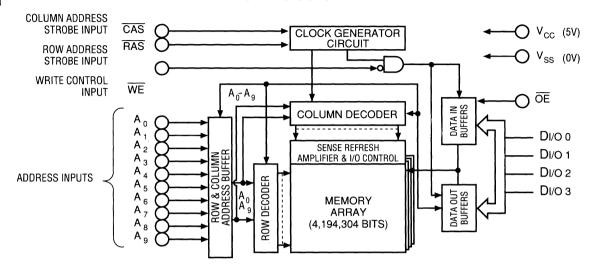


direction is controlled by  $\overline{\text{WE}}$  and  $\overline{\text{OE}}$ .

Returning  $\overline{RAS}$  and  $\overline{CAS}$  high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{RAS}$  cycle (READ, WRITE,  $\overline{RAS}$  only,  $\overline{CAS}$ -before- $\overline{RAS}$ , or Hidden refresh) so that all 1024 combinations of  $\overline{RAS}$  addresses (A0-A9) are executed at least every 8ms, regardless of sequence.

The STATIC COLUMN cycle is always initiated with a row address strobed in by  $\overline{RAS}$  followed by a column address strobed in by  $\overline{CAS}$ . By holding  $\overline{RAS}$  low, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning  $\overline{RAS}$  high terminates the STATIC COLUMN operation.

# FUNCTIONAL BLOCK DIAGRAM STATIC COLUMN



#### **FUNCTIONAL TRUTH TABLE**

				Addre	esses		
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	н	Х	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
STATIC COLUMN READ	L	L	Н	ROW	COL	Valid Data Out Valid Data Out	
STATIC COLUMN WRITE	L	L	L	ROW	COL	Valid Data In Valid Data In	
STATIC COLUMN READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V to +7.0V
Operating Temperature, TA(Ambient)0°C to +70°C
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation1 Watt
Short Circuit Output Current50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq$   $T_{\mbox{\scriptsize A}} \leq$  70°C, = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc1		60	mA	3, 4
OPERATING CURRENT: FAST STATIC COLUMN (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current $(\overline{RAS} = \overline{CAS} = V_{IH})$ after 8 $\overline{RAS}$ cycles min.)	lcc3		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	Icc4		0.5	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY $(\overline{RAS} = \text{Cycling: } \overline{CAS} = \text{V}_{\text{IH}})$	lcc5		60	mA	3
REFRESH CURRENT: $\overline{CAS}$ -before- $\overline{RAS}$ ( $\overline{RAS}$ and $\overline{CAS}$ = Cycling)	Icc6		60	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ VIN ≤ Vcc), all other pins not under test = 0 volts)	lı	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ Vout ≤ Vcc)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High voltage (lout = -5mA)	Vон	2.4		V	1
Output Low voltage (lout = 5mA)	Vol		0.4	V	

## RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \le T_{A} \le 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1

#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9), DIN	CI1		5	pF	2
Input Capacitance RAS, CAS, WE, OE	CI2		7	pF	2
Output Capacitance Dout	Co		7	pF	2

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13)  $(0^{\circ}C \le T_{A} \le +70^{\circ}C, Vcc = 5.0V \pm 10\%)$ 

A.C. CHARACTERISTICS			-8		-10		-12		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	160		190		220		ns	
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	185		220		295		ns	
Access time from RAS	<sup>t</sup> RAC		80		100		120	ns	14
Access time from CAS	tCAC		20		25		35	ns	15
Output Enable	<sup>t</sup> OE		25		25		35	ns	
Access time from column address	<sup>t</sup> AA		40		50		60	ns	
Access time from CAS precharge	<sup>t</sup> CPA		40		50		60	ns	
RAS pulse width	<sup>t</sup> RAS	80	10,000	100	10,000	120	10,000	ns	
RAS hold time	<sup>t</sup> RSH	20		25		35		ns	
RAS precharge time	<sup>t</sup> RP	70		80		90		ns	
CAS pulse width	t <sub>CAS</sub>	20	10,000	25	10,000	35	10,000	ns	
CAS hold time	t <sub>CSH</sub>	80		100		120		ns	
CAS precharge time	t <sub>CPN</sub>	10		15		20		ns	16
RAS to CAS delay time	t <sub>RCD</sub>	10	60	10	75	15	85	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address set-up time	tasr	0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	10		10		10		ns	<u> </u>
RAS to column address delay time	<sup>t</sup> RAD	10	40	10	50	15	45	ns	18
Column address set-up time	t <sub>ASC</sub>	0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		15		25		ns	
Column address hold time (referenced to RAS)	<sup>t</sup> AR	50		60		140		ns	
Column address to RAS lead time	<sup>t</sup> RAL	40		50		60		ns	
Read command set-up time	t <sub>RCS</sub>	0		0		0		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19
CAS to output in low-Z	t <sub>CLZ</sub>	5		5		5		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	25	0	25	0	35	ns	20
Output Disable	<sup>t</sup> OD		25		25		30	ns	



#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq T_A \leq +70$ °C, Vcc = 5.0V  $\pm$  10%)

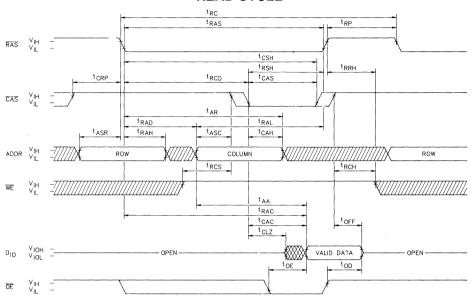
A.C. CHARACTERISTICS			-8	-10			12		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command set-up time	twcs	0		0		0		ns	21
Write command hold time	<sup>t</sup> WCH	15		20		25		ns	
Write command hold time	twcR	60		70		90		ns	
(referenced to RAS)			1		1				ļ
Write command pulse width	<sup>t</sup> WP	15		20		25		ns	
Write command to RAS lead time	t <sub>RWL</sub>	20		25		30		ns	
Write command to CAS lead time	tCWL	20		25		30		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	22
Data-in hold time	<sup>t</sup> DH	15		15		25		ns	22
Data-in hold time	t <sub>DHR</sub>	60		70		90		ns	
(referenced to RAS)									
RAS to WE delay time	<sup>t</sup> RWD	90		120		160		ns	21
Column address	<sup>t</sup> AWD	70		80		100		ns	21
to WE delay time									
CAS to WE delay time	tCWD	50		65		75		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		8		8		8	ms	
RAS to CAS Precharge time	<sup>t</sup> RPC	0		0		0		ns	
CAS set-up time	t <sub>CSR</sub>	10		10		10		ns	5
(CAS-before-RAS refresh)									
CAS hold time	tCHR	15		20		15		ns	5
(CAS-before-RAS refresh)									
RAS pulse width (STATIC COLUMN)	tRASC	80	100,000	100	100,000	120	100,000	ns	
CAS precharge time (STATIC COLUMN)	<sup>t</sup> CP	10	25	10	25	15	30	ns	
STATIC COLUMN MODE	tsc	55		65		55		ns	
cycle time									
STATIC COLUMN READ-MODIFY-	tSRMW	135		160		160		ns	
WRITE cycle time		ĺ			Ì				
Last write to column address	tLWAD	25	45	30	55	30	55	ns	
delay time									
Last write to column address	<sup>t</sup> AHLW		95		115	115		ns	
hold time									
RAS hold time precharged to OE	<sup>t</sup> ROH	20		20		20		ns	
Output data hold time from	<sup>t</sup> AOH	5		5	_	5	_	ns	
column address		]						'	
Output data enable from write	tow	_	30	_	35	_	40	ns	
OE to data delay	<sup>t</sup> OED	25		30	١.	30		ns	
OE command hold time	<sup>t</sup> OEH	25		25		30		ns	7
Access time from last Write	t <sub>ALW</sub>		95		115		115	ns	

#### **NOTES**

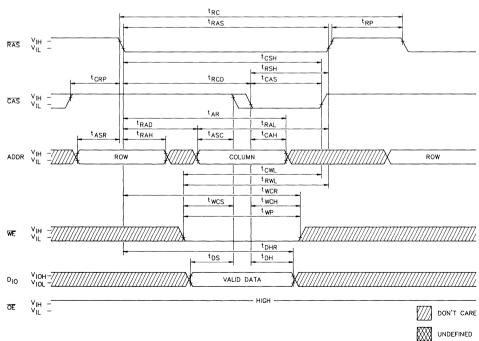
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and VCC = 5V.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C) is assured.
- An initial pause of 100μs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between Vih and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If  $\overline{CAS}$  = Vih, data output is high impedance.
- 12. If  $\overline{\text{CAS}} = \text{Vil.}$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If <del>CAS</del> is low at the falling edge of <del>RAS</del>, Dout will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer <del>CAS</del> must be pulsed high for <sup>t</sup>CPN.

- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- 19. Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 21. <sup>t</sup>WCS, <sup>t</sup>RWD, <sup>t</sup>AWD and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), <sup>t</sup>AWD ≥ <sup>t</sup>AWD (min) and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to Vih) is indeterminate.
- 22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles and  $\overline{\text{WE}}$  leading edge in late WRITE or READ-WRITE cycles.
- 23. During a READ cycle, if  $\overline{OE}$  is LOW then taken HIGH DOUT goes open. If  $\overline{OE}$  is tied permanently low a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{WE}$  = LOW and  $\overline{OE}$ =HIGH.

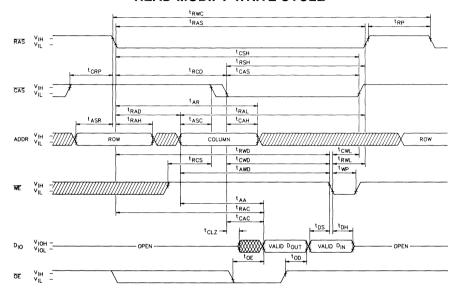
#### **READ CYCLE**



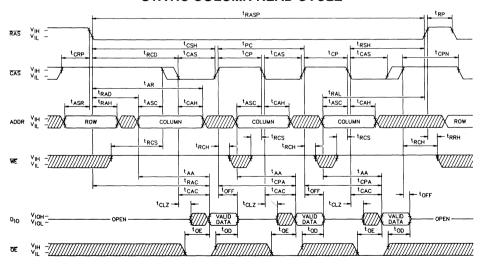
#### **EARLY-WRITE CYCLE**



# READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE



#### STATIC COLUMN READ CYCLE

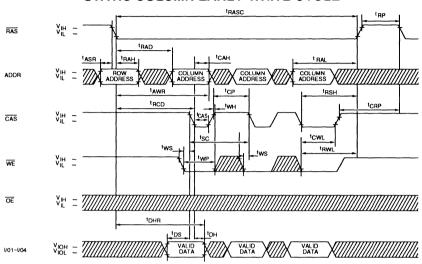




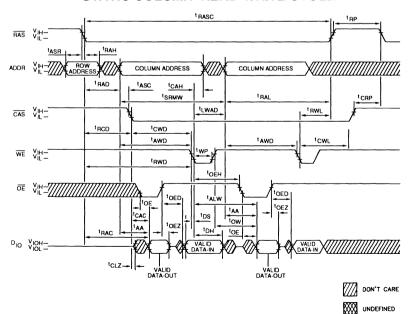
UNDEFINED



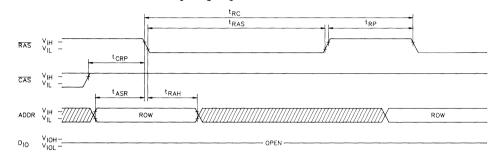
#### STATIC COLUMN EARLY-WRITE CYCLE



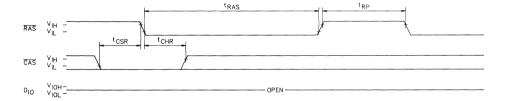
#### STATIC COLUMN READ-WRITE CYCLE



# $\overline{\text{RAS}}$ ONLY REFRESH CYCLE (ADDR = A $_0$ - A $_8$ ; A $_9$ and $\overline{\text{WE}}$ = DON'T CARE.)

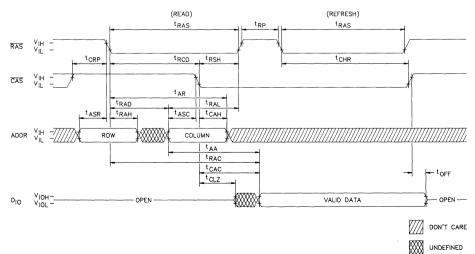


# $\overline{\text{CAS-BEFORE-RAS}}$ REFRESH CYCLE $(A_0 - A_0, \overline{\text{WE}} \text{ and } \overline{\text{OE}} = \text{DON'T CARE})$



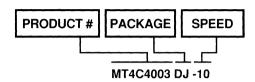
### **HIDDEN REFRESH CYCLE**

 $(\overline{WE} = HIGH); \overline{OE} = LOW)^{24}$ 



#### ORDER INFORMATION

1MEG x 4, 100ns in Plastic DJ



The Micron 4 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS

silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.


# DRAM

## 4MEG x 1 DRAM

**FAST PAGE MODE** 

#### **FEATURES**

**OPTIONS** 

- Industry standard x1 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024 cycle refresh distributed across 16ms
- Refresh modes: RAS only, CAS before RAS, and Hidden

MARKING

• Optional Fast Page Mode access cycle

#### **GENERAL DESCRIPTION**

The MT4C1004 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the  $\overline{WE}$  input. A logic high on  $\overline{WE}$  dictates READ mode while a logic low on WE dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes low prior to CAS going low, the output pin(s) remain open (High Z) until the next CAS cycle. If WE goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as <del>CAS</del> remains low (regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ ). This late  $\overline{\text{WE}}$  pulse results in a READ-WRITE cycle.

Returning RAS and CAS high terminates a memory

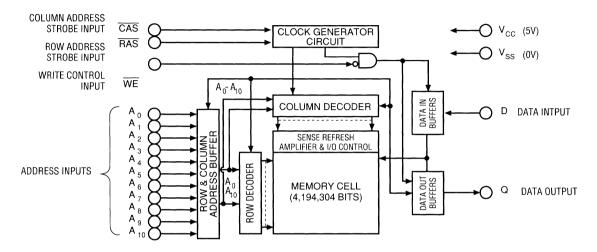
PIN AS	SIGNMENT (To	p View)
MT4C100 18 Pin D		MT4C1004 20 Pin ZIP
A1 G 6 13 A2 G 7 12 A3 G 8 11	7 Dout Dou 6 Dout Dou 6 Dout Park 6 Dout Park 6 Dout Park 6 Dout Park 7 Dout Park 8 Dout P	2 C. CAS 1 C. CAS 2 C. CAS 1 C. CAS 2 C. CAS 2 C. CAS 3 C. CAS 4 C
MT4C100 20 Pin S		20(:::) A8
Din 0 2 RAS 0 3 NC 0 4 *A10 0 5	25 Dout 25 Dout 24 CAS 23 NC 22 A9	
A0 C 9 A1 C 10 A2 C 11 A3 C 12 Vcc C 13	18	
*Address not used for NOTE: Package I	r <del>RAS</del> only refresh nformation To Be Dete	rmined.

cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{RAS}$  cycle (READ, WRITE,  $\overline{RAS}$  only,  $\overline{CAS}$ -before- $\overline{RAS}$ , or Hidden refresh) so that all 1024 combinations of  $\overline{RAS}$  addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A10) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by  $\overline{RAS}$  followed by a column address strobed in by  $\overline{CAS}$ . By holding  $\overline{RAS}$  low,  $\overline{CAS}$  may be toggled strobing in different column addresses executing faster memory cycles. Returning  $\overline{RAS}$  high terminates the PAGE MODE operation.

# MICHON

#### FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE



#### **FUNCTIONAL TRUTH TABLE**

				ما ما ما			
				Addre	esses		į
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	н	Н	Χ	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE MODE READ	L	H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
PAGE MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	

## MICRON

## MT4C1004

#### **ABSOLUTE MAXIMUM RATINGS\***

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq$   $T_{\Delta} \leq$  70°C = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc1		60	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE $(\overline{RAS} = V_{IL}, \overline{CAS} = Cycling: tpc = tpc(min))$	lcc2		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = VIH after 8 RAS cycles min.)	Icc3		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current (RAS = CAS = Vcc -0.2V after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	Icc4		0.5	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY $(\overline{RAS} = \text{Cycling: } \overline{CAS} = \text{V}_{\text{IH}})$	lcc5		60	mA	3
REFRESH CURRENT: $\overline{CAS}$ -before- $\overline{RAS}$ ( $\overline{RAS}$ and $\overline{CAS}$ = Cycling)	Icc6		60	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V $\leq$ Vin $\leq$ Vcc), all other pins not under test = 0 volts)	lı	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ Vout ≤ Vcc)	loz	-10	10	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA)	Vон	2.4		V	1
Output Low voltage (lout = 5mA)	Vol		0.4	V	

#### RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{{\color{blue}A}} \leq 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	Vін	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1

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#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9), DIN	C <sub>11</sub>		5	pF	. 2
Input Capacitance RAS, CAS, WE	C12		7	pF	2
Output Capacitance Dout	C <sub>0</sub>		7	pF	2

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$   $T_{A} \leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS PARAMETER		-8			10		-12		
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	160		190		220		ns	
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	185		220		255		ns	
PAGE-MODE READ or WRITE	<sup>t</sup> PC	50		55		70		ns	
cycle time									
Access time from RAS	<sup>t</sup> RAC		80		100	120		ns	14
Access time from CAS	tCAC		20		25	35		ns	15
Access time from column address	<sup>t</sup> AA		40		50	60		ns	
Access time from CAS precharge	<sup>t</sup> CPA		40		50	60		ns	
RAS pulse width	<sup>t</sup> RAS	80	10,000	100	10,000	120	10,000	ns	
RAS pulse width (PAGE MODE)	<sup>t</sup> RASP	80	100,000	100	100,000	120	100,000	ns	
RAS hold time	<sup>t</sup> RSH	20		25		35		ns	
RAS precharge time	<sup>t</sup> RP	70		80		90		ns	
CAS pulse width	t <sub>CAS</sub>	20	10,000	25	10,000	35	10,000	ns	
CAS hold time	t <sub>CSH</sub>	80		100		120		ns	
CAS precharge time	t <sub>CPN</sub>	10		10		20		ns	16
CAS precharge time (PAGE MODE)	<sup>t</sup> CP	10	25	10	25	15		ns	
RAS to CAS delay time	<sup>t</sup> RCD	10	60	15	75	25	85	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address set-up time	t <sub>ASR</sub>	0_		0		0		ns	
Row address hold time	<sup>t</sup> RAH	10		10		15		ns	
RAS to column	<sup>t</sup> RAD	10	40	10	50	10	60	ns	18
address delay time					1				
Column address set-up time	t <sub>ASC</sub>	0		0		0		ns	
Column address hold time	<sup>t</sup> CAH	15		15		25		ns	
Column address hold time	<sup>t</sup> AR	50		60		110		ns	
(referenced to RAS)									
Column address to	<sup>t</sup> RAL	40		50		60		ns	
RAS lead time									
Read command set-up time	t <sub>RCS</sub>	0		0_		0		ns	
Read command hold time	t <sub>RCH</sub>	0		0		0		ns	19
(referenced to CAS)									
Read command hold time	t <sub>RRH</sub>	0		0		10		ns	19
(referenced to RAS)									
CAS to output in low-Z	<sup>t</sup> CLZ	5		5		5		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	25	0	25	0	25	ns	20
WE command set-up time	twcs	0		0		0		ns	21
Write command hold time	tWCH	15		20		25		ns	

MT4C1004

### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$   $T_{A}^{} \leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time (referenced to RAS)	tWCR	60		70		110		ns	
Write command pulse width	t <sub>WP</sub>	15		20		25		ns	
Write command to RAS lead time	t <sub>RWL</sub>	20		25		35		ns	
Write command to CAS lead time	tCWL	20		25		35		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	22
Data-in hold time	t <sub>DH</sub>	15		15		25		ns	22
Data-in hold time (referenced to RAS)	t <sub>DHR</sub>	60		70		110		ns	
RAS to WE delay time	t <sub>RWD</sub>	70		80		120		ns	21
Column address to WE delay time	<sup>t</sup> AWD	40		50		60		ns	21
CAS to WE delay time	tCWD	20		25		35		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		16		16		16	ms	
RAS to CAS Precharge time	tRPC	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	<sup>t</sup> CHR	15		20		20		ns	5

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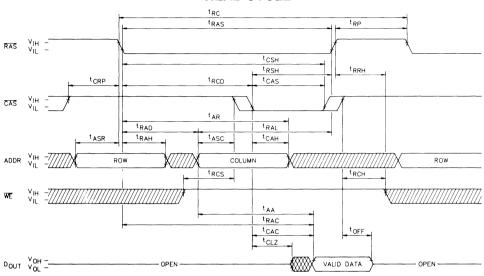
MT4C1004

#### NOTES

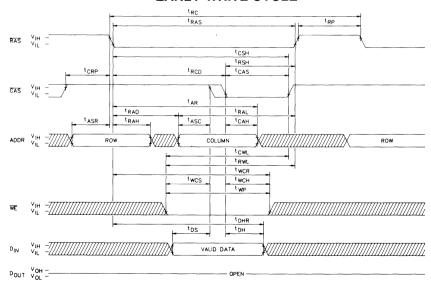
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and VCC = 5V.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ( $0^{\circ}C \leq T_{A} \leq 70^{\circ}C$ ) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between Vih and Vil (or between VIL and VIH) in a monotonic manner.
- 11. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 12. If CAS = VIL, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If  $\overline{CAS}$  is low at the falling edge of  $\overline{RAS}$ , DOUT will

- be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for  ${}^{\text{t}}\text{CPN}$ .
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle.
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 21. <sup>t</sup>WCS, <sup>t</sup>RWD, <sup>t</sup>AWD and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), <sup>t</sup>AWD ≥ <sup>t</sup>AWD (min) and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to Vih) is indeterminate
- 22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles and  $\overline{\text{WE}}$  leading edge in late WRITE or READ-WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{WE}$  = LOW.

#### **READ CYCLE**

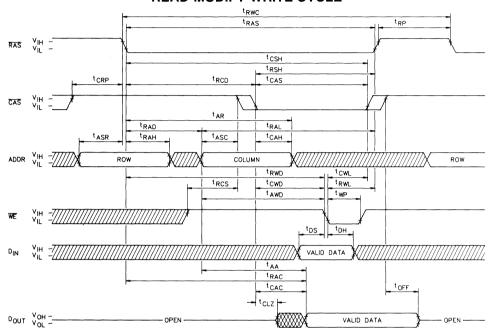


#### **EARLY-WRITE CYCLE**

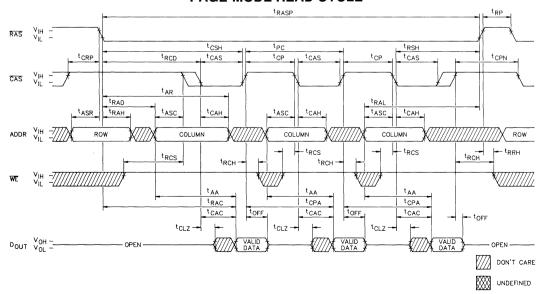


DON'T CARE

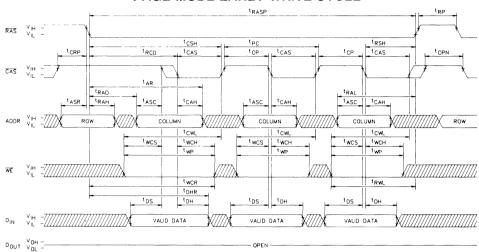
# READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE



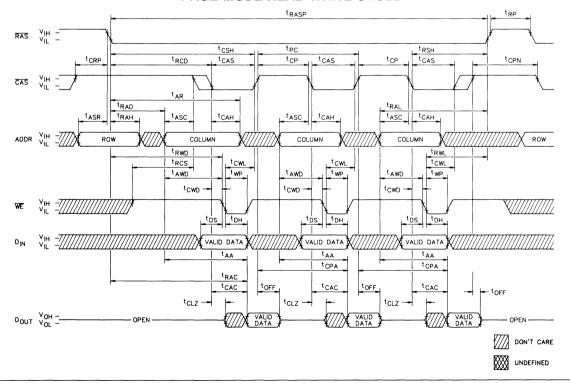
#### **PAGE-MODE READ CYCLE**



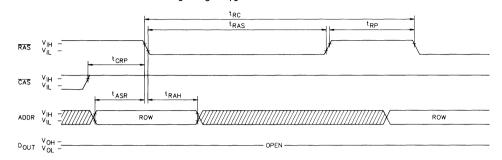
#### PAGE-MODE EARLY-WRITE CYCLE



#### PAGE-MODE READ-WRITE CYCLE



### 



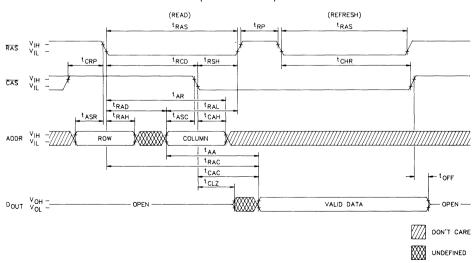
### **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_9 \text{ and } \overline{WE} = DON'T CARE)$ 



## HIDDEN REFRESH CYCLE

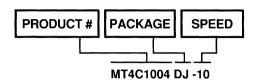
 $(\overline{WE} = HIGH)$ 



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#### ORDER INFORMATION

4 MEG x 1, 100ns in Plastic SOJ



The Micron 4 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS

silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

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# DRAM

# 4MEG x 1 DRAM

**NIBBLE MODE** 

#### **FEATURES**

**OPTIONS** 

- Industry standard x1 pin-out, timing, functions and
- High performance CMOS silicon gate process
- Single +5V±10% power supply.
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024 cycle refresh distributed across 16ms
- Refresh modes: RAS only, CAS before RAS, and

**MARKING** 

· Optional Nibble Mode access cycle

• Timing 80ns access 100ns access 120ns access	-8 -10 -12
• Organization 4 MEG x 1	MT4C1005
<ul> <li>Packages         Plastic DIP         Ceramic DIP         Plastic ZIP         Plastic SOJ</li> </ul>	None C Z DJ

#### GENERAL DESCRIPTION

The MT4C1005 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time.  $\overline{RAS}$  is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the  $\overline{\text{WE}}$  input. A logic high on  $\overline{\text{WE}}$  dictates READ mode while a logic low on WE dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. If  $\overline{\text{WE}}$ goes low prior to CAS going low, the output pin(s) remain open (High Z) until the next CAS cycle. If WE goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as CAS remains low (regardless of  $\overline{WE}$  or  $\overline{RAS}$ ). This late  $\overline{WE}$  pulse results in a READ-WRITE cycle.

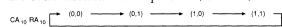
Returning RAS and CAS high terminates a memory

PIN	ASSIGNME	NT (Top View)
	C1005 n DIP	MT4C1005 20 Pin ZIP
Din (=1) WE   2 RAS   3 *A10   4 A0   5 A1   6 A2   7 A3   8 Vcc   9	18	A9
	C1005 n SOJ	20t) A8
Din C 1 WE C 2 RAS C 3 NC C 4 *A10 C 5	26	
A0 [ 9 A1 [ 10 A2 [ 11 A3 [ 12 Vcc [ 13	18	
*Address not used	d for RAS only refre	sh
NOTE: Packag	je Information To	Be Determined.

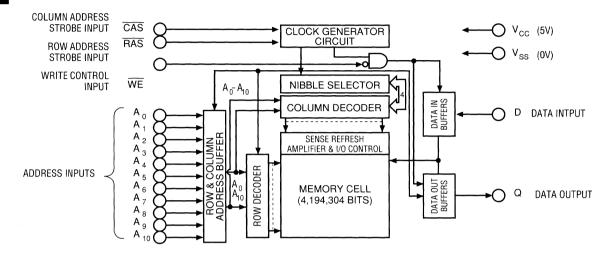
cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS only, CAS-before-RAS, or Hidden refresh) so that all 1024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

Nibble Mode operation allows faster sequential serial data operations (READ, WRITE or READ-MODIFY-WRITE) on up to 4 bits. The first of 4 bits is accessed in the usual manner with CAS address A9 (nibble MSB) and RAS address A9 (nibble LSB) selecting on of 4 bits within a nibble for initial access. By holding RAS low,

CAS can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around (see below).



## FUNCTIONAL BLOCK DIAGRAM NIBBLE MODE



#### **FUNCTIONAL TRUTH TABLE**

				Addresses			
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	Х	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
NIBBLE MODE READ	L	H→L→H, L→H→L	Н	ROW	COL	Valid Data Out, Valid Data Out	
NIBBLE MODE WRITE	L	H→L→H, L→H→L	L	ROW	COL	Valid Data In, Valid Data In	
NIBBLE MODE READ-WRITE	L	H→L→H, L→H→L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	

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## MT4C1005

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on VCC supply relative to Vss1.0V to +7.0V
Operating Temperature, TA(Ambient)0°C to +70°C
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation 1 Watt
Short Circuit Output Current 50m A

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	Icc1		60	mA	3, 4
OPERATING CURRENT: NIBBLE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS  Power supply standby current (RAS = CAS = VIH  after 8 RAS cycles min.)	Іссз		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	Icc4		0.5	mA	
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = VIH)	lcc5		60	mA	3
REFRESH CURRENT: $\overline{CAS}$ -before- $\overline{RAS}$ ( $\overline{RAS}$ and $\overline{CAS}$ = Cycling)	Icc6		60	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ VIN ≤ Vcc), all other pins not under test = 0 volts)	li	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dour is disabled, 0V ≤ Vour ≤ Vcc)	loz	-10	10	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA)	Vон	2.4		V	1
Output Low voltage (lout = 5mA)	Vol		0.4	\ V	,

## RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \le T_A \le 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VıL	-1.0	0.8	٧	1

#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9), DIN	C <sub>I1</sub>		5	pF	2
Input Capacitance RAS, CAS, WE	Cl2		7	pF	2
Output Capacitance Dout	Co		7	рF	2

## **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$   $T_A \leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS	-8		-8	-10			12		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	160		190		220		ns	
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	185	l.	220		255		ns	
Access time from RAS	t <sub>RAC</sub>		80		100	120		ns	14
Access time from CAS	t <sub>CAC</sub>		20		25	35		ns	15
Access time from column address	<sup>t</sup> AA		40		50	60		ns	
Access time from CAS precharge	t <sub>CPA</sub>		40		50	60		ns	
RAS pulse width	t <sub>RAS</sub>	80	10,000	100	10,000	120	10,000	ns	
RAS hold time	t <sub>RSH</sub>	20		25		35		ns	
RAS precharge time	t <sub>RP</sub>	70		80		90		ns	
CAS pulse width	t <sub>CAS</sub>	20	10,000	25	10,000	35	10,000	ns	
CAS hold time	t <sub>CSH</sub>	80		100		120		ns	
CAS precharge time	t <sub>CPN</sub>	10		15		20		ns	16
RAS to CAS delay time	<sup>t</sup> RCD	10	60	15	75	25	85	ns	17
CAS to RAS precharge time	<sup>t</sup> CRP	10		10		10		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	10		10		15		ns	
RAS to column address delay time	<sup>t</sup> RAD	10	40	10	50	10	60	ns	18
Column address set-up time	t <sub>ASC</sub>	0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		15		25		ns	
Column address hold time (referenced to RAS)	<sup>t</sup> AR	50		60		110		ns	
Column address to RAS lead time	<sup>t</sup> RAL	40		50		60		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19
CAS to output in low-Z	<sup>t</sup> CLZ	5		5		5		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	25	0	25	0	25	ns	20
WE command set-up time	twcs	0		0		0	25	ns	21
Write command hold time	tWCH	15		20		0		ns	
Write command hold time (referenced to RAS)	tWCR	60		70		25		ns	

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## **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq T_A \leq +70$ °C, Vcc =  $5.0V \pm 10$ %)

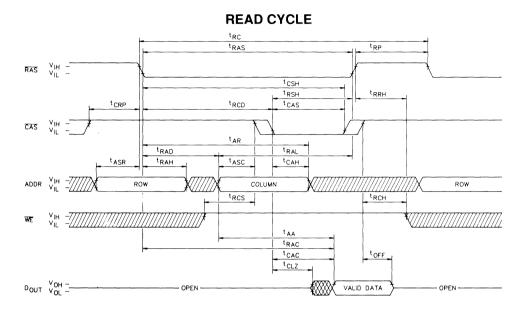
A.C. CHARACTERISTICS	-8			10		12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command pulse width	t <sub>WP</sub>	15		20		25		ns	
Write command to RAS lead time	<sup>t</sup> RWL	20		25		35		ns	
Write command to CAS lead time	t <sub>CWL</sub>	20		25		35		ns	
Data-in set-up time	<sup>t</sup> DS	0		0		0		ns	22
Data-in hold time	<sup>t</sup> DH	15		15		25		ns	22
Data-in hold time (referenced to RAS)	<sup>t</sup> DHR	60		70		110		ns	
RAS to WE delay time	<sup>t</sup> RWD	70		90		120		ns	21
Column address to WE delay time	<sup>t</sup> AWD	40		50		60		ns	21
CAS to WE delay time	t <sub>CWD</sub>	20		35		35		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	<sup>t</sup> REF		16		16		16	ms	
RAS to CAS Precharge time	t <sub>RPC</sub>	0		0			0	ns	
CAS set-up time (CAS-before-RAS refresh)	<sup>t</sup> CSR	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	t <sub>CHR</sub>	15		20		20		ns	5
RAS pulse width (NIBBLE MODE)	<sup>t</sup> RASN	80	100,000	100	100,000	120	100,000	ns	
CAS precharge time (NIBBLE MODE)	<sup>t</sup> NCP	10	25	10	25	15	30	ns	
NIBBLE MODE cycle time	<sup>t</sup> NC	35		35		40		ns	
NIBBLE MODE READ- MODIFY-WRITE cycle time	<sup>t</sup> NRWL	50		55		70		ns	
NIBBLE MODE READ-MODIFY- WRITE cycle time	<sup>t</sup> NRWC	55		55		60		ns	
NIBBLE MODE access time	<sup>t</sup> NCAC	15		15		20		ns	15
NIBBLE MODE pulse width	<sup>t</sup> NCAS	15		15		20		ns	
NIBBLE MODE CAS precharge time	<sup>t</sup> NCP	10		10		15		ns	
NIBBLE MODE RAS hold time	<sup>t</sup> NRSH	15		15		20		ns	
NIBBLE MODE CAS to WRITE delay time	<sup>t</sup> NCWD	15		15		20		ns	
NIBBLE MODE WRITE command to RAS load time	<sup>t</sup> NRWL	15		15		20		ns	
NIBBLE MODE WRITE command to CAS load time	<sup>t</sup> NCWL	15		15		20		ns	

#### **NOTES**

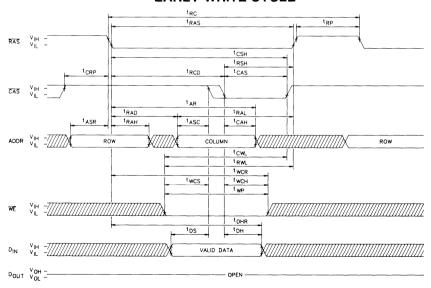
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and  $V_{CC} = 5V$ .
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C) is assured.
- An initial pause of 100μs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIL and VIH) in a monotonic manner.
- 11. If  $\overline{CAS}$  = Vih, data output is high impedance.
- 12. If  $\overline{\text{CAS}} = \text{Vil.}$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If  $\overline{CAS}$  is low at the falling edge of  $\overline{RAS}$ , Dout will

- be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for  ${}^{\text{t}}\text{CPN}$ .
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- 19. Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle.
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to Voh ot Vol.
- 21. <sup>t</sup>WCS, <sup>t</sup>RWD, <sup>t</sup>AWD and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), <sup>t</sup>AWD ≥ <sup>t</sup>AWD (min) and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to Vih) is indeterminate.
- 22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles and  $\overline{\text{WE}}$  leading edge in late WRITE or READ-WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{WE}$  = LOW.

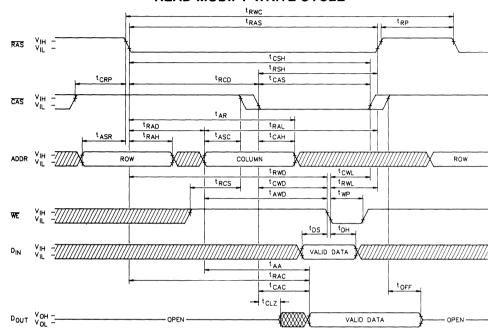
# MICRON



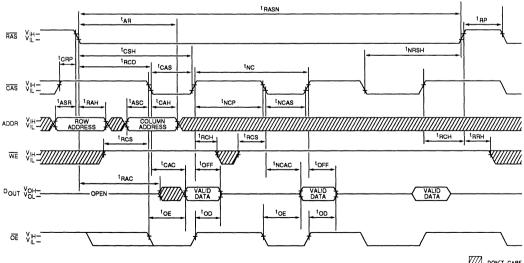
#### **EARLY-WRITE CYCLE**



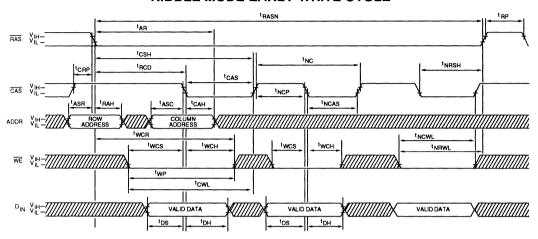
# READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE



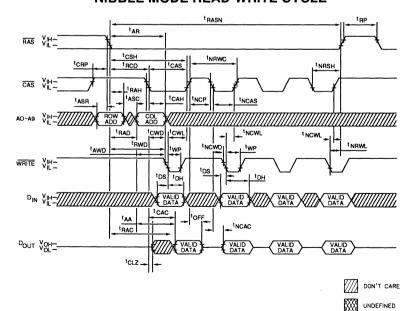
#### **NIBBLE MODE READ CYCLE**



#### NIBBLE MODE EARLY-WRITE CYCLE

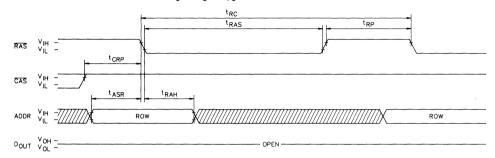


#### **NIBBLE MODE READ-WRITE CYCLE**



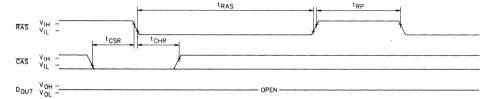
#### **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0$  -  $A_9$ ;  $A_{10}$  and  $\overline{WE}$  = DON'T CARE.)



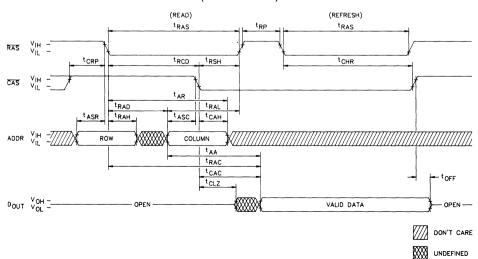
## **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_{10} \text{ and } \overline{WE} = DON'T CARE)$ 



#### HIDDEN REFRESH CYCLE

 $(\overline{WE} = HIGH)$ 

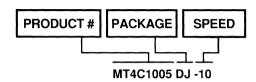


MICHON

MT4C1005

#### **ORDER INFORMATION**

4 MEG x 1, 100ns in Plastic SOJ



The Micron 4 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS

silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

# MICRON

# DRAM

# **4MEG x 1 DRAM**

STATIC COLUMN

#### **FEATURES**

**OPTIONS** 

- Industry standard x1 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply.
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024 cycle refresh distributed across 16ms
- Refresh modes: RAS only, CAS before RAS, and Hidden

MARKING

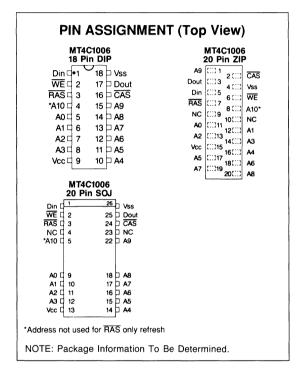
• Optional Static Column access cycle

• Timing 80ns access 100ns access 120ns access	-8 -10 -12
• Organization 4 MEG x 1	MT4C1006
<ul> <li>Packages         Plastic DIP         Ceramic DIP         Plastic ZIP         Plastic SOJ</li> </ul>	None C Z DJ

#### **GENERAL DESCRIPTION**

The MT4C1006 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time.  $\overline{RAS}$  is used to latch the first 11 bits and  $\overline{CAS}$  the latter 11 bits. A READ or WRITE cycle is selected with the  $\overline{WE}$  input. A logic high on  $\overline{WE}$  dictates READ mode while a logic low on  $\overline{WE}$  dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of  $\overline{WE}$  or  $\overline{CAS}$ , whichever occurs last. If  $\overline{WE}$  goes low prior to  $\overline{CAS}$  going low, the output pin(s) remain open (High Z) until the next  $\overline{CAS}$  cycle. If  $\overline{WE}$  goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as  $\overline{CAS}$  remains low (regardless of  $\overline{WE}$  or  $\overline{RAS}$ ).

Returning RAS and CAS high terminates a memory cycle and decreases chip current to a reduced standby level.

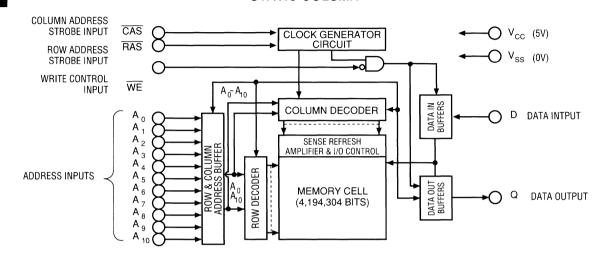


Also, the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{RAS}$  cycle (READ, WRITE,  $\overline{RAS}$  only,  $\overline{CAS}$ -before- $\overline{RAS}$ , or Hidden refresh) so that all 1024 combinations of  $\overline{RAS}$  addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

STATIC COLUMN operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary.

The STATIC COLUMN cycle is always initiated with a row address strobed in by  $\overline{RAS}$  followed by a column address strobed in by  $\overline{CAS}$ . By holding  $\overline{RAS}$  low, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning  $\overline{RAS}$  high terminates the STATIC COLUMN operation.

## FUNCTIONAL BLOCK DIAGRAM STATIC COLUMN



#### **FUNCTIONAL TRUTH TABLE**

				Addresses			
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	X	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
STATIC COLUMN READ	L	L	Н	ROW	COL	Valid Data Out, Valid Data Out	
STATIC COLUMN WRITE	L	L	L	ROW	COL	Valid Data In Valid Data In	
STATIC COLUMN READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	

MICHON

MT4C1006

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on VCC supply relative to Vss1.0V to +7.0V
Operating Temperature, TA(Ambient)0°C to +70°C
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation 1 Watt
Short Circuit Output Current50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq T_{\mbox{\scriptsize A}} \leq 70 ^{\circ} \mbox{\scriptsize C},$  = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc1		60	mA	3, 4
OPERATING CURRENT: STATIC COLUMN (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS  Power supply standby current (RAS = CAS = VIH  after 8 RAS cycles min.)	Іссз		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ( $\overline{RAS} = \overline{CAS} = Vcc -0.2V$ after 8 $\overline{RAS}$ cycles min. All other inputs at $Vcc -0.2V$ or $Vss + 0.2V$ )	Icc4		0.5	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY $(\overline{RAS} = \text{Cycling: } \overline{CAS} = \text{V}_{\text{IH}})$	lcc5		60	mA	3
REFRESH CURRENT: $\overline{CAS}$ -before- $\overline{RAS}$ ( $\overline{RAS}$ and $\overline{CAS}$ = Cycling)	Icc6		60	mA	3, 5
INPUT LEAKAGE CURRENT (any input $(0V \le V_{IN} \le V_{CC})$ , all other pins not under test = 0 volts)	lı	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ Vout ≤ Vcc)	loz	-10	10	μА	
OUTPUT LEVELS Output High voltage (Iout = -5mA)	Vон	2.4		V	1
Output Low voltage (lout = 5mA)	Vol	1	0.4	V	

## RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \le T_{A} \le 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1



#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9), DIN	CI1		5	pF	2
Input Capacitance RAS, CAS, WE	C <sub>12</sub>		7	pF	2
Output Capacitance Dout	Co		7	pF	2

## **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ( $0^{\circ}$ C  $\leq$  T<sub>A</sub>  $\leq$  +70 $^{\circ}$ C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS			-8	-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	150		190		220		ns	
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	180		220		255		ns	
Access time from RAS	tRAC		80		100	120		ns	14
Access time from CAS	tCAC		20		25	35		ns	15
Access time from column address	<sup>t</sup> AA		40		50	60		ns	
Access time from CAS precharge	t <sub>CPA</sub>		40		50	60		ns	
RAS pulse width	t <sub>RAS</sub>	80	10,000	100	10,000	120	10,000	ns	
RAS hold time	<sup>t</sup> RSH	20		25		35		ns	
RAS precharge time	t <sub>RP</sub>	60		80		90		ns	
CAS pulse width	t <sub>CAS</sub>	20	10,000	25	10,000	35	10,000	ns	
CAS hold time	t <sub>CSH</sub>	80		100		120		ns	
CAS precharge time	t <sub>CPN</sub>	15		15		20		ns	16
RAS to CAS delay time	<sup>t</sup> RCD	10	75	10	75	25	85	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	10		10		15		ns	
RAS to column	<sup>t</sup> RAD	10	50	10	50	10	60	ns	18
address delay time									
Column address set-up time	†ASC	0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		15		25		ns	
Column address hold time (referenced to $\overline{RAS}$ )	t <sub>AR</sub>	50		60		110		ns	
Column address to RAS lead time	<sup>t</sup> RAL	40		50		60		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19
CAS to output in low-Z	t <sub>CLZ</sub>	5		5		5		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	25	0	25	5		ns	20
WE command set-up time	twcs	0		0		0		ns	21
Write command hold time	tWCH	15		20		0		ns	

MT4C1006

## **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ( $0^{\circ}C \le T_{A} \le +70^{\circ}C$ ,  $Vcc = 5.0V \pm 10\%$ )

A.C. CHARACTERISTICS	-8		-8		10	-	12		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time (referenced to RAS)	<sup>t</sup> WCR	35		70		105		ns	
Write command pulse width	<sup>t</sup> WP	15		20		25		ns	
Write command to RAS lead time	t <sub>RWL</sub>	25		25		35		ns	
Write command to CAS lead time	t <sub>CWL</sub>	25		25		35		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	22
Data-in hold time	tDH	15		15		25		ns	22
Data-in hold time (referenced to RAS)	<sup>t</sup> DHR	35		70		110		ns	
RAS to WE delay time	t <sub>RWD</sub>	70		90		120		ns	21
Column address to WE delay time	<sup>t</sup> AWD	40		50		60		ns	21
CAS to WE delay time	tCWD	30		35		35		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		16		16		16	ms	
RAS to CAS Precharge time	t <sub>RPC</sub>	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	<sup>t</sup> CSR	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	<sup>t</sup> CHR	20		20		20		ns	5
RAS pulse width (STATIC COLUMN)	<sup>t</sup> RASC	80	100,000	100	100,000	120	100,000	ns	
CAS precharge time (STATIC COLUMN)	<sup>t</sup> CP	10		10		15		ns	
STATIC COLUMN MODE cycle time	<sup>t</sup> SC	55		55		60		ns	
STATIC COLUMN READ-MODIFY- WRITE cycle time	<sup>t</sup> SRMW	135		135		140		ns	
Last write to column address delay time	<sup>t</sup> LWAD	20	85	25	95	30	100	ns	
Last write to column address hold time	<sup>t</sup> AHLW		85		95		100	ns	
Output data hold time from column address	<sup>t</sup> AOH	5		5	<u></u>	5	_	ns	
Output data enable from write	tOW	_	25		25	_	30	ns	

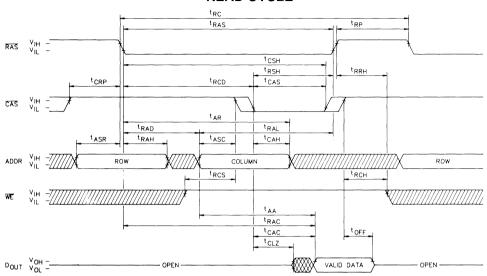
#### **NOTES**

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and  $V_{CC} = 5V$ .
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C  $\leq$  T $_{\!A}$   $\leq$  70°C) is assured.
- An initial pause of 100μs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between Vih and Vil (or between Vil and Vih) in a monotonic manner.
- 11. If  $\overline{CAS}$  = ViH, data output is high impedance.
- 12. If  $\overline{\text{CAS}} = \text{Vil}$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If  $\overline{CAS}$  is low at the falling edge of  $\overline{RAS}$ , Dout will

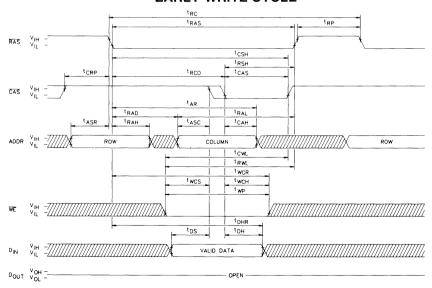
- be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for  ${}^{\text{t}}\text{CPN}$ .
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle.
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to Voh ot Vol.
- 21. <sup>t</sup>WCS, <sup>t</sup>RWD, <sup>t</sup>AWD and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), <sup>t</sup>AWD ≥ <sup>t</sup>AWD (min) and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to VIH) is indeterminate.
- 22. These parameters are referenced to CAS leading edge in early WRITE cycles and WE leading edge in late WRITE or READ-WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{WE}$  = LOW.



#### **READ CYCLE**

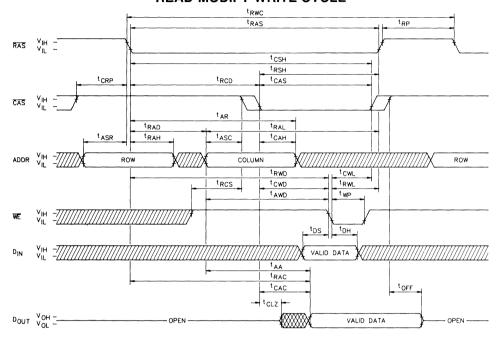


#### **EARLY-WRITE CYCLE**

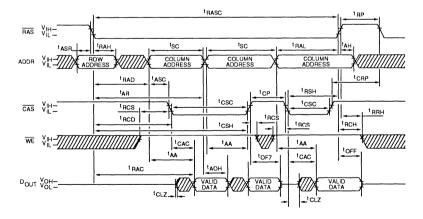


DON'T CARE
UNDEFINED

# READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE



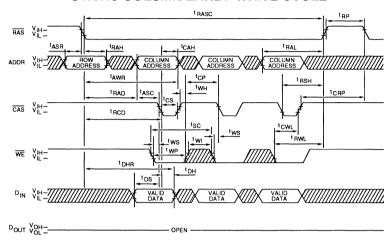
#### STATIC COLUMN READ CYCLE



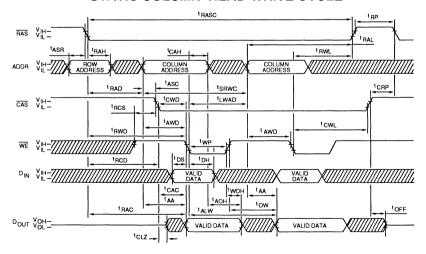




#### STATIC COLUMN EARLY-WRITE CYCLE



#### STATIC COLUMN READ-WRITE CYCLE

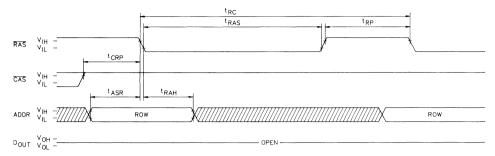


DON'T CARE
UNDEFINED

# MICRON

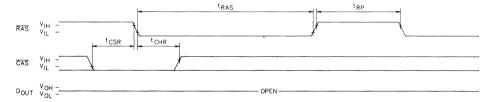
#### **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0 - A_9$ ;  $A_{10}$  and  $\overline{WE} = DON'T CARE.)$ 



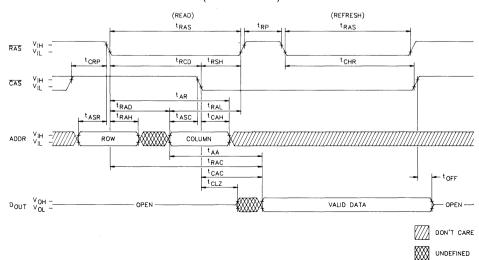
## **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_{10}, \overline{WE} \text{ and } \overline{OE} = DON'T CARE)$ 



## **HIDDEN REFRESH CYCLE**

 $(\overline{WE} = HIGH)$ 

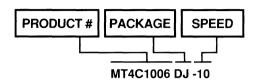


MICRON

MT4C1006

#### ORDER INFORMATION

4 MEG x 1, 100ns in Plastic SOJ



The Micron 4 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS

silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.



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Memory	Optional			Power	Dissipation	Pac	kage		
Configuration	Access Cycle	Part Number	Access Time (ns)	Standby	Active	SIP	SIMM	Process	Page
64K x 8	Page Mode	MT8068M,MN	100,120,150,200	45mw	450mw	30	30	NMOS	2-3
64K x 9	Page Mode	MT9068M,MN	100,120,150,200	45mw	450mw	30	30	NMOS	2-13
256K x 4	Page Mode	MT4259M,MN	80,100,120,150	60mw	600mw	22	22	NMOS	2-23
256K x 5	Page Mode	MT85259M,MN	80,100,120,150	60mw	600mw	24	24	NMOS	2-33
256K x 8	Page Mode	MT8259DMN	80,100,120,150	135mw	1350mw	30	30	NMOS	2-43
256K x 8	Page Mode	MT8259M,MN	80,100,120,150	135mw	1350mw	30	30	NMOS	2-53
256K x 9	Page Mode	MT9259DMN	80,100,120,150	135mw	1350mw	30	30	NMOS	2-63
256K x 9	Page Mode	MT9259M,MN	80,100,120,150	135mw	1350mw	30	30	NMOS	2-73
256K x 36	Page Mode	MT8C3656M,MN	100,120,150	140mw	2000mw	72	72	C/NMOS	2-83
1 Meg x 8	Static Column	MT8C8026M,MN	100,120,150	45mw	1575mw	30	30	CMOS	2-115
1 Meg x 8	Nibble Mode	MT8C8025M,MN	100,120,150	45mw	1575mw	30	30	CMOS	2-103
1 Meg x 8	Fast Page Mode	MT8C8024M,MN	100,120,150	45mw	1575mw	30	30	CMOS	2-93
1 Meg x 9	Static Column	MT8C9026M,MN	100,120,150	45mw	1575mw	30	30	CMOS	2-149
1 Meg x 9	Nibble Mode	MT8C9025M,MN	100,120,150	45mw	1575mw	30	30	CMOS	2-137
1 Meg x 9	Fast Page Mode	MT8C9024M,MN	100,120,150	45mw	1575mw	30	30	CMOS	2-127

# DRAM MODULES

# **64K x 8 DRAM**

#### **FEATURES**

- Industry standard pin-out in a 30-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 45mW standby, 450mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: RAS only, CAS before RAS, and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS M	ARKING
Timing	
80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15
Organization	
64K x 8	MT8068
Packages: Leadless 30-pin SIMM	M

Leaded 30-pin SIP

A0-A7	Address Inputs	CAS	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
Q9	Data-Out	RAS	Row Address Strobe
W	Write Enable	VDD	Power (+5V)
Vss	Ground		

MN

# GENERAL DESCRIPTION

The MT8068M/MN is a randomly accessed solid-state memory containing 65,536 bits organized in a x8 configuration. The 14 address bits are entered 7 bits at a time using RAS to latch the first 7 bits and CAS the latter 7 bits. If the

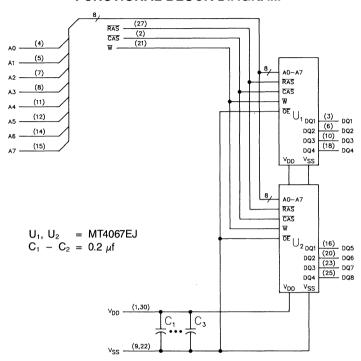
PIN ASS	IGNMENT (Top Vi	ew)
V <sub>0D</sub> 3 1 1  CAS	Vob (1)  CAS (2)  DO1 (3)  A0 (4)  A1 (5)  DO2 (6)  A2 (7)  A3 (8)  Vss (9)  DO3 (10)  A4 (11)  A5 (12)  DO4 (13)  A6 (14)  A7 (15)  DO5 (16)  NC (17)  NC (18)  NC (17)  NC (19)  DO6 (20)  W (21)  Vss (22)  DO7 (23)  NC (24)  DO8 (25)  NC (26)  RAS (27)  NC (28)  NC (29)  NC (29)	MT8068MN
MH		MC
IVIII		

WE pin goes low prior to CAS going low, the output pin remains open until the next CAS cycle.

By holding  $\overline{RAS}$  low,  $\overline{CAS}$  may be toggled to execute several faster READ or WRITE cycles within the  $\overline{RAS}$  address defined PAGE boundary. Returning  $\overline{RAS}$  high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high-time. Memory cell data is retained in its correct state by maintaining power and executing a  $\overline{RAS}$  (Refresh) cycle so that all 256 combinations of  $\overline{RAS}$  addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.



## **FUNCTIONAL BLOCK DIAGRAM**



#### **FUNCTIONAL TRUTH TABLE**

	540	0.00	WE	Addr	esses		NOTEO
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on VCC supply relative to Vss1.0V to +7.0	)V
Operating Temperature, TA(Ambient)0°C to +70°	°C
Storage Temperature55°C to +150°	°C
Power Dissipation8 Wa	att
Short Circuit Output Current50m	ıA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (0°C $\leq$ T<sub>A</sub> $\leq$ 70°C) (Vcc = 5.0V $\pm$ 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1
INPUT LEAKAGE Input leakage current, any input (0V $\leq$ VIN $\leq$ VCC), all other pins not under test = 0 volts	lı .	-80	80	μА	
OUTPUT LEAKAGE Output leakage current (Dou⊤ is disabled, 0V ≤ Vou⊤ ≤ Vcc)	loz	-80	80	μА	
OUTPUT LEVELS Output High (Logic 1) voltage (lout = -5mA)	. <b>V</b> он	2.4		V	1
Output Low (Logic 0) voltage (lout = 5mA)	Vol		0.4	l V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels (RAS = CAS = Vih after 8 RAS cycles)	lcc1	15	15	15	15	mA	
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc2	195	165	165	135	mA	2
OPERATING CURRENT: PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc3	195	165	165	135	mA	2
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih: trc = trc(MIN))	ICC4	165	120	120	105	mA	2
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = cycling, trc = trc(MIN))	lcc5	195	165	165	135	mA	2,19

#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As)	C <sub>I1</sub>		15	pF	17
Input Capacitance RAS, CAS, WE	C <sub>12</sub>		24	pF	17
Output Capacitance Dout, DIN	Co		7	pF	17

MICHON

# **DRAM MODULES**

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 3, 4, 5, 10, 11, 17, 18) (0°C $\leq$ T $_{A} \leq$ 70°C) (Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS	-8		-10		-12		-15			T	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	<sup>t</sup> PC	75		90		100		120		ns	6, 7
Access time from RAS	<sup>t</sup> RAC		80		100		120		150	ns	7, 8
Access time from CAS	<sup>t</sup> CAC		40		50		60		75	ns	7, 9
RAS pulse width	t <sub>RAS</sub>	80	10,000	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	<sup>t</sup> RSH	40		50		60		75		ns	
RAS precharge time	<sup>t</sup> RP	60		80		90		100		ns	
CAS pulse width	tCAS	40	10,000	60	10,000	60	10,000	75	10,000	ns	
CAS hold time	tCSH	80		110		120		150		ns	
CAS precharge time	<sup>t</sup> CPN	20		25		25		30		ns	18
CAS precharge time (PAGE-MODE)	<sup>t</sup> CP	25		30		30		35		ns	
RAS to CAS delay time	tRCD	20	40	25	50	25	60	25	75	ns	13
CAS to RAS set-up time	tCRP	10		15		20		20		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	15		15		15		15		ns	
Column address set-up time	t <sub>ASC</sub>	0		0	1	0		0		ns	
Column address hold time	<sup>t</sup> CAH	15		20		20		25		ns	
Column address hold time referenced to RAS	<sup>t</sup> AR	50		70		80		100		ns	
READ command hold time referenced to CAS	<sup>t</sup> RCH	0		0		0		0		ns	14
READ command hold time referenced to RAS	<sup>t</sup> RRH	0		0		0		0		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	25	0	30	0	30	0	35	ns	12
WE command set-up time	twcs	0		0		0		0		ns	
WRITE command hold time	tWCH	15		35		40		45		ns	
WRITE command hold time referenced to RAS	tWCR	35		85		100		120		ns	
WRITE command pulse width	tWP	15		35		40		45		ns	
WRITE command to RAS lead time	t <sub>RWL</sub>	35		35		40		45		ns	
WRITE command to CAS lead time	tCWL	35		35		40		45		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		0		ns	15
Data-in hold time	t <sub>DH</sub>	15		35		40		45		ns	15
Data-in hold time referenced to RAS	t <sub>DHR</sub>	35		85		100		120		ns	
Transition time (rise or fall)	t <sub>T</sub>	3	100	3	100	3	100	3	100	ns	5, 16
Refresh Period (256 cycles)	t <sub>REF</sub>		4		4		4		4	ms	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		10		ns	19
CAS hold time (CAS-before-RAS refresh)	tCHR	15		20		25		30		ns	19

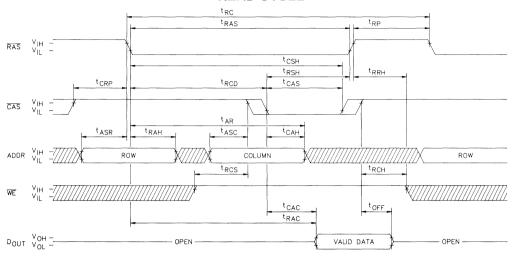


#### **NOTES**

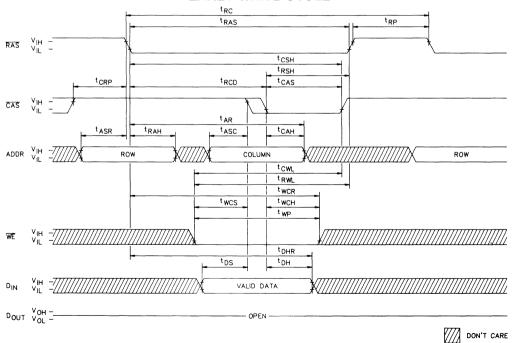
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
- 4. AC characteristics assume  ${}^{t}T = 5$ ns.
- 5. VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- 7. Measured with a load equivalent to 2 TTL gates and 100pF.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 9. Assumes that  ${}^{t}RCD \ge {}^{t}RCD \pmod{n}$ .
- 10. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 11. If  $\overline{CAS} = V_{1L}$ , data output may contain data from the last valid READ cycle.

- 12. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
  - 14. <sup>t</sup>RCH is referenced to the first rising edge of RAS or CAS.
  - 15. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles.
  - 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
  - 17. Capacitance calculated from the equation  $C = \underline{I\Delta t} \Delta V$  with  $\Delta V = 3V$  and VCC = 5V. This parameter is sampled.
  - 18. If CAS is low at the falling edge of RAS, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CP. Note 8 applies to determine valid data out.
  - 19. On-chip refresh and address counters are enabled.
  - 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set  $\overline{WE} = LOW$ .

#### **READ CYCLE**

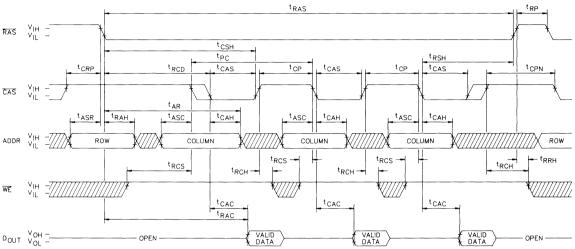


#### **EARLY-WRITE CYCLE**

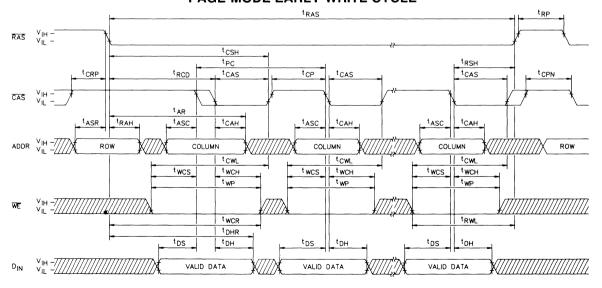


#### PAGE-MODE READ CYCLE

1CRON

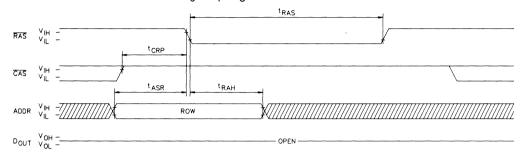


#### PAGE-MODE EARLY-WRITE CYCLE



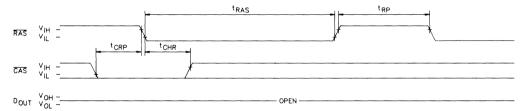
### **RAS ONLY REFRESH CYCLE**

 $(ADDR = A_0 - A_7; A_8 \text{ and } \overline{WE} = DON'T CARE.)$ 



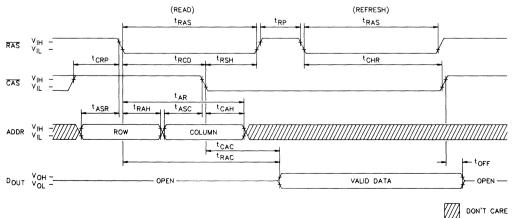
# CAS-BEFORE-RAS REFRESH CYCLE

 $(A_0 - A_8 \overline{WE}, \overline{OE} = DON'T CARE.)$ 



# **HIDDEN REFRESH CYCLE**

 $(\overline{WE} = HIGH)$ 





### **ORDER INFORMATION**

64K x 8, 120ns access, Leadless SIMM



The Micron 64K x 8 DRAM module is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance NMOS

double-poly process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

***************************************			

# DRAM MODULES

# **64K x 9 DRAM**

#### **FEATURES**

 Organization 64K x 9

- Industry standard pin-out in a 30-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 45mW standby, 450mW active, typical
- On-board power supply decoupling capacitors (0.2μf) for low noise
- Refresh modes:  $\overline{RAS}$  only,  $\overline{CAS}$  before  $\overline{RAS}$ , and Hidden
- 256 cycle refresh distributed across 4ms
- · Optional Page Mode access cycle

OPTIONS	MARKING				
• Timing					
80ns access	-8				
100ns access	-10				
120ns access	-12				
150ns access	-15				

<ul> <li>Packages: Leadless 30-pin SIMM</li> </ul>	M
Leaded 30-pin SIP	MN

F	PIN ASS	IGNMENT (Top V	iew)
V <sub>DO</sub> CAS DO1 A0 A1 DO2 A2 A3 V <sub>SS</sub> DO3 A4 A5 DO4 A6 A7 DO5 NC NC NC NC DO6 W V <sub>SS</sub> DO7 NC DO8 O9 RAS CAS9 D9 V <sub>DO</sub>	MT9068    1	Voo (1)  CAS (2)  DO1 (3)  A0 (4)  A1 (5)  DO2 (6)  A2 (7)  A3 (8)  Vss (9)  DO3 (10)  A4 (11)  A5 (12)  DO4 (13)  A6 (14)  A7 (15)  DO5 (16)  NC (17)  NC (18)  NC (19)  DO6 (20)  W (21)  Vss (22)  DO7 (23)  NC (24)  DO8 (25)  O9 (26)  PAS (27)  CAS9 (28)  D9 (29)	MT9068MN
Ĺ	МН	J	MC

A0-A7	Address Inputs	CAS, CAS9	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
Q9	Data-Out	RAS	Row Address Strobe
W	Write Enable	VDD	Power (+5V)
Vss	Ground		

MT9068

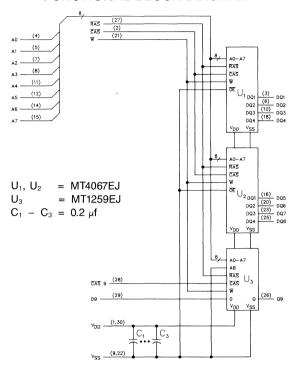
#### GENERAL DESCRIPTION

The MT9068M/MN is a randomly accessed solid-state memory containing 65,536 bits organized in a x9 configuration. The 16 address bits are entered 8 bits at a time using  $\overline{RAS}$  to latch the first 8 bits and  $\overline{CAS}$  the latter 8 bits. If the

 $\overline{\text{WE}}$  pin goes low prior to  $\overline{\text{CAS}}$  going low, the output pin remains open until the next  $\overline{\text{CAS}}$  cycle.

By holding  $\overline{RAS}$  low,  $\overline{CAS}$  may be toggled to execute several faster READ or WRITE cycles within the  $\overline{RAS}$  address defined PAGE boundary. Returning  $\overline{RAS}$  high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high-time. Memory cell data is retained in its correct state by maintaining power and executing a  $\overline{RAS}$  (Refresh) cycle so that all 256 combinations of  $\overline{RAS}$  addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

# **FUNCTIONAL BLOCK DIAGRAM**



### **FUNCTIONAL TRUTH TABLE**

F	D40	040	WE	Addr	esses		NOTES
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	



#### **ABSOLUTE MAXIMUM RATINGS\***

 \*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (0°C $\leq$ T<sub>A</sub> $\leq$ 70°C) (Vcc = 5.0V $\pm$ 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1
INPUT LEAKAGE Input leakage current, any input (0V $\leq$ Vin $\leq$ Vcc), all other pins not under test = 0 volts	lı .	-90	90	μА	
OUTPUT LEAKAGE Output leakage current (Doυτ is disabled, 0V ≤ Voυτ ≤ Vcc)	loz	-90	90	μА	
OUTPUT LEVELS Output High (Logic 1) voltage (lout = -5mA) Output Low (Logic 0) voltage (lout = 5mA)	Vон Vol	2.4	0.4	V	1

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels (RAS = CAS = ViH after 8 RAS cycles)	lcc1	15	15	15	15	mA	
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc2	195	165	165	135	mA	2
OPERATING CURRENT: PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	Іссз	195	165	165	135	mA	2
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih: trc = trc(MIN))	lcc4	165	120	120	105	mA	2
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = cycling, trc = trc(MIN))	lcc5	195	165	165	135	mA	2,19

### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As)	C <sub>l1</sub>		15	pF	17
Input Capacitance RAS, CAS, WE	Cl2		24	pF	17
Output Capacitance Dout, DIN	Co		7	pF	17



# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 3, 4, 5, 10, 11, 17, 18) (0°C $\leq$ T $_A$ $\leq$ 70°C) (Vcc = 5.0V $\pm$ 10%)

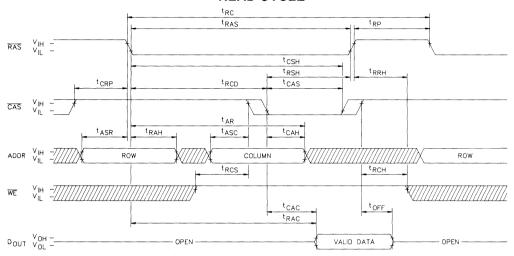
A.C. CHARACTERISTICS		-8		-10		-12		-15		ļ	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	<sup>t</sup> PC	75		90		100		120		ns	6, 7
Access time from RAS	t <sub>RAC</sub>		80		100		120		150	ns	7, 8
Access time from CAS	t <sub>CAC</sub>		40		50		60		75	ns	7, 9
RAS pulse width	t <sub>RAS</sub>	80	10,000	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	<sup>t</sup> RSH	40		50		60		75		ns	
RAS precharge time	t <sub>RP</sub>	60		80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	40	10,000	60	10,000	60	10,000	75	10,000	ns	
CAS hold time	<sup>t</sup> CSH	80		110		120		150		ns	
CAS precharge time	t <sub>CPN</sub>	20		25		25		30		ns	18
CAS precharge time (PAGE-MODE)	<sup>t</sup> CP	25		30		30		35		ns	
RAS to CAS delay time	<sup>t</sup> RCD	20	40	25	50	25	60	25	75	ns	13
CAS to RAS set-up time	t <sub>CRP</sub>	10		15		20		20		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	15		15		15		15		ns	
Column address set-up time	t <sub>ASC</sub>	0		0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		20		20		25		ns	
Column address hold time referenced to RAS	<sup>t</sup> AR	50		70		80		100		ns	
READ command hold time referenced to CAS	<sup>t</sup> RCH	0		0		0		0		ns	14
READ command hold time	<sup>t</sup> RRH	0		0		0		0		ns	
referenced to RAS	10==	-					<b>-</b>			-	1.5
Output buffer turn-off delay	toff to the second	0	25	0	30	0	30	0	35	ns	12
WE command set-up time	tweet	0		0		0		0	-	ns	
WRITE command hold time	tWCH	15		35	-	40	-	45	-	ns	1
WRITE command hold time referenced to RAS	<sup>t</sup> WCR	35		85		100		120		ns	
WRITE command pulse width	t <sub>WP</sub>	15		35		40		45		ns	
WRITE command to RAS lead time	<sup>t</sup> RWL	35		35		40		45		ns	
WRITE command to CAS lead time	tCWL	35		35		40		45		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		0		ns	15
Data-in hold time	t <sub>DH</sub>	15		35		40		45		ns	15
Data-in hold time referenced to RAS	t <sub>DHR</sub>	35		85		100		120		ns	
Transition time (rise or fall)	t <sub>T</sub>	3	100	3	100	3	100	3	100	ns	5, 16
Refresh Period (256 cycles)	tREF		4		4		4		4	ms	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		10		ns	19
CAS hold time (CAS-before-RAS refresh)	tCHR	15		20		25		30		ns	19

### **NOTES**

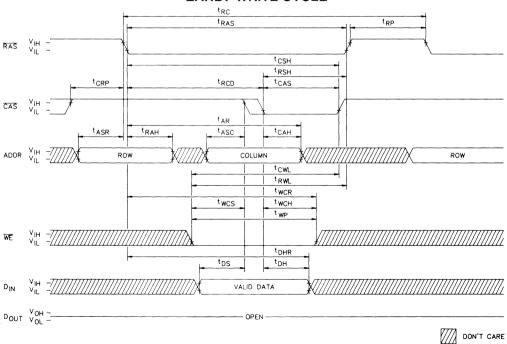
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- An initial pause of 100μs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
- 4. AC characteristics assume  ${}^{t}T = 5$ ns.
- 5. Vih min and Vil max are reference levels for measuring timing of input signals. Transition times are measured between Vih and Vil.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C) is assured.
- 7. Measured with a load equivalent to 2 TTL gates and 100pF.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 9. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 10. If  $\overline{CAS} = VIH$ , data output is high impedance.
- 11. If  $\overline{\text{CAS}} = \text{Vil.}$ , data output may contain data from the last valid READ cycle.

- 12. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
  - 14. <sup>t</sup>RCH is referenced to the first rising edge of RAS or CAS.
  - 15. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles.
  - 16. In addition to meeting the transition rate specification, all input signals must transit between VIII and VIII (or between VIII and VIII) in a monotonic manner.
  - 17. Capacitance calculated from the equation  $C = \underline{I\Delta t} \Delta V$  with  $\Delta V = 3V$  and Vcc = 5V. This parameter is sampled.
  - 18. If CAS is low at the falling edge of RAS, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CP. Note 8 applies to determine valid data out.
  - 19. On-chip refresh and address counters are enabled.
  - 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set  $\overline{WE}$  = LOW.

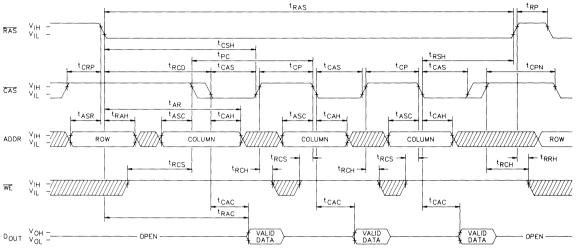
### **READ CYCLE**



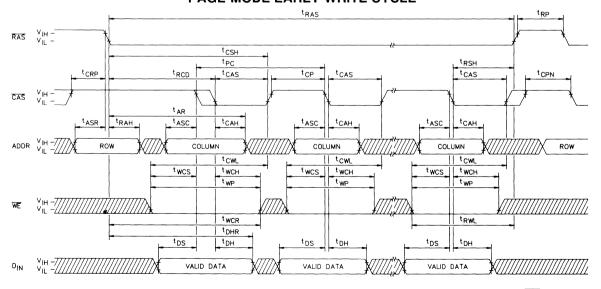
# **EARLY-WRITE CYCLE**



### PAGE-MODE READ CYCLE



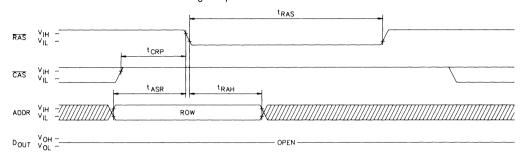
### PAGE-MODE EARLY-WRITE CYCLE





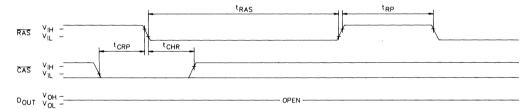
### **RAS ONLY REFRESH CYCLE**

 $(ADDR = A_0 - A_7; and \overline{WE} = DON'T CARE.)$ 



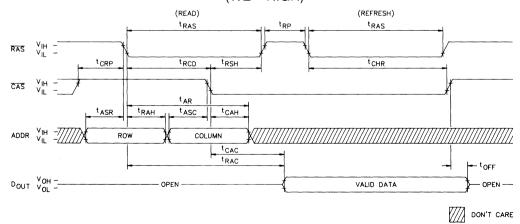
# **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_8 \overline{WE}, \overline{OE} = DON'T CARE.)$ 



# HIDDEN REFRESH CYCLE

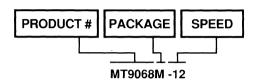
 $(\overline{WE} = HIGH)$ 





#### ORDER INFORMATION

64K x 9, 120ns access, Leadless SIMM



The Micron 64K x 9 DRAM module is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance NMOS

double-poly process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

# DRAM MODULES

# 256K x 4 DRAM

#### **FEATURES**

- Industry standard pin-out in a 22-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 60mW standby, 600mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: RAS only, CAS before RAS, and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS	MARKING
Timing	
80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15
Organization	
256K x 4	MT4259
• Packages: Leaded 22-pin SIP	MN

PIN ASSIGNMENT (Top View)
A8 (1) VCC (2) D1 (3) Q1 (4) CAS (5) A7 (6) A5 (7) A4 (8) D2 (9) Q2 (10) W (11) A1 (12) A3 (13) A6 (14) Q3 (15) D3 (16) A2 (17) A0 (18) RAS (19) D4 (20) Q4 (21) VSS (22)
MA

A0-A8	Address Inputs	CAS	Column Address Strobe
D1 - D4	Data-In	Q1 - Q4	Data-Out
RAS	Row Address Strobe	$\overline{\mathbb{W}}$	Write Enable
Vcc	Power (+5V)	Vss	Ground

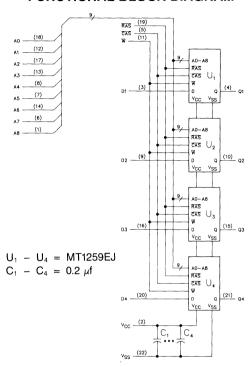
### **GENERAL DESCRIPTION**

The MT4259MN is a randomly accessed solid-state memory containing 262,144 bits organized in a x4 configuration. The 16 address bits are entered 8 bits at a time using RAS to latch the first 8 bits and CAS the latter 8 bits. If the

WE pin goes low prior to CAS going low, the output pin remains open until the next CAS cycle.

By holding  $\overline{RAS}$  low,  $\overline{CAS}$  may be toggled to execute several faster READ or WRITE cycles within the  $\overline{RAS}$  address defined PAGE boundary. Returning  $\overline{RAS}$  high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high-time. Memory cell data is retained in its correct state by maintaining power and executing a  $\overline{RAS}$  (Refresh) cycle so that all 256 combinations of  $\overline{RAS}$  addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

# **FUNCTIONAL BLOCK DIAGRAM**



# **FUNCTIONAL TRUTH TABLE**

-	546	0.00	WE	Addr	esses		NOTES
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	



### **ABSOLUTE MAXIMUM RATINGS\***

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (0°C $\leq$ T $_{\Delta}$ $\leq$ 70°C) (Vcc = 5.0V $\pm10\%$ )

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1
INPUT LEAKAGE Input leakage current, any input (0V $\leq$ VIN $\leq$ VCC), all other pins not under test = 0 volts	lı .	-40	40	μА	
OUTPUT LEAKAGE Output leakage current (Dou⊤ is disabled, 0V ≤ Vou⊤ ≤ Vcc)	loz	-40	40	μА	
OUTPUT LEVELS Output High (Logic 1) voltage (Iout = -5mA)	Vон	2.4		V	1
Output Low (Logic 0) voltage (Iout = 5mA)	Vol		0.4	V	

			MAX				
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels (RAS = CAS = VIH after 8 RAS cycles)	lcc1	20	20	20	20	mA	
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc2	260	220	220	180	mA	2
OPERATING CURRENT: PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc3	260	220	220	180	mA	2
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih: trc = trc(MIN))	Icc4	220	160	160	140	mA	2
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = cycling, trc = trc(MIN))	lcc5	260	220	220	180	mA	2,19

#### CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As)	C <sub>11</sub>		20	pF	17
Input Capacitance RAS, CAS, WE	CI2		32	pF	17
Output Capacitance Dout, DIN	Co		7	pF	17

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 3, 4, 5, 10, 11, 17, 18) (0°C $\leq$ T $_{A}$ $\leq$ 70°C) (Vcc = 5.0V $\pm$ 10%)

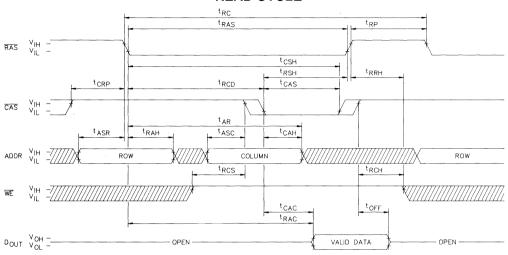
A.C. CHARACTERISTICS		-	8	-10 -12			12				
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	<sup>t</sup> PC	75		90		100		120		ns	6, 7
Access time from RAS	tRAC		80		100		120		150	ns	7, 8
Access time from CAS	t <sub>CAC</sub>		40		50		60		75	ns	7, 9
RAS pulse width	t <sub>RAS</sub>	80	10,000	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	t <sub>RSH</sub>	40		50		60		75		ns	
RAS precharge time	t <sub>RP</sub>	60		80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	40	10,000	60	10,000	60	10,000	75	10,000	ns	
CAS hold time	t <sub>CSH</sub>	80		110		120		150		ns	
CAS precharge time	<sup>t</sup> CPN	20		25		25		30		ns	18
CAS precharge time (PAGE-MODE)	<sup>t</sup> CP	25		30		30		35		ns	
RAS to CAS delay time	t <sub>RCD</sub>	20	40	25	50	25	60	25	75	ns	13
CAS to RAS set-up time	tCRP	10		15		20		20		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		0		ns	
Row address hold time	t <sub>RAH</sub>	15		15		15		15		ns	
Column address set-up time	t <sub>ASC</sub>	0		0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		20		20		25		ns	
Column address hold time referenced to RAS	<sup>t</sup> AR	50	i	70		80		100		ns	
READ command hold time referenced to CAS	<sup>t</sup> RCH	0		0		0		0		ns	14
READ command hold time referenced to RAS	<sup>t</sup> RRH	0		0		0		0		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	25	0	30	0	30	0	35	ns	12
WE command set-up time	twcs	0		0		0		0		ns	
WRITE command hold time	tWCH	15		35		40		45		ns	
WRITE command hold time referenced to RAS	tWCR	35		85		100		120		ns	
WRITE command pulse width	<sup>t</sup> WP	15		35		40		45		ns	
WRITE command to RAS lead time	<sup>t</sup> RWL	35		35		40		45		ns	
WRITE command to CAS lead time	tCWL	35		35		40		45		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		0		ns	15
Data-in hold time	t <sub>DH</sub>	15		35		40		45		ns	15
Data-in hold time referenced to RAS	t <sub>DHR</sub>	35		85		100		120		ns	
Transition time (rise or fall)	t <sub>T</sub>	3	100	3	100	3	100	3	100	ns	5, 16
Refresh Period (256 cycles)	tREF		4		4		4		4	ms	1
CAS set-up time (CAS-before-RAS refresh)	t <sub>CSR</sub>	10		10		10		10		ns	19
CAS hold time (CAS-before-RAS refresh)	<sup>t</sup> CHR	15		20		25		30		ns	19

### **NOTES**

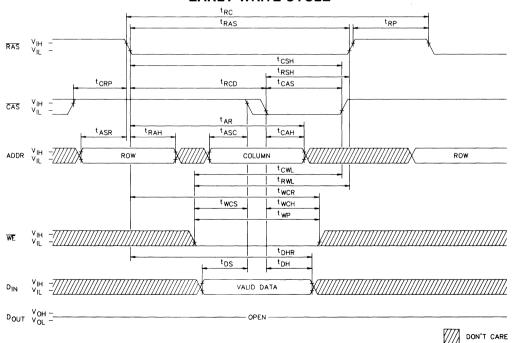
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
- 4. AC characteristics assume  ${}^{t}T = 5ns$ .
- 5. Vih min and Vil max are reference levels for measuring timing of input signals. Transition times are measured between Vih and Vil.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C  $\leq$  T $_{\rm A}$   $\leq$  70°C) is assured.
- 7. Measured with a load equivalent to 2 TTL gates and 100pF.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 9. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 10. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 11. If  $\overline{CAS} = V_{1L}$ , data output may contain data from the last valid READ cycle.

- 12. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 14.  ${}^{t}RCH$  is referenced to the first rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ .
- These parameters are referenced to CAS leading edge in early WRITE cycles.
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 17. Capacitance calculated from the equation  $C = \frac{I\Delta t}{\Delta V}$  with  $\Delta V = 3V$  and Vcc = 5V. This parameter is
- 18. If CAS is low at the falling edge of RAS, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CP. Note 8 applies to determine valid data out.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set WE = LOW.

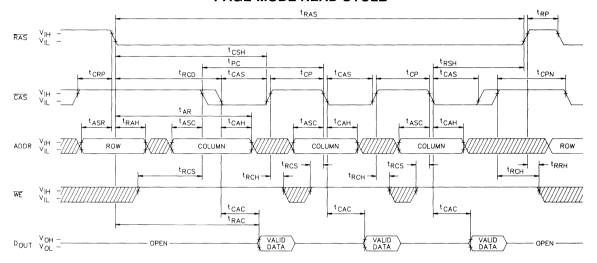
### **READ CYCLE**



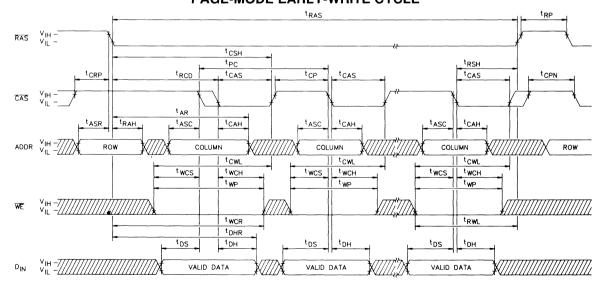
# **EARLY-WRITE CYCLE**



### PAGE-MODE READ CYCLE



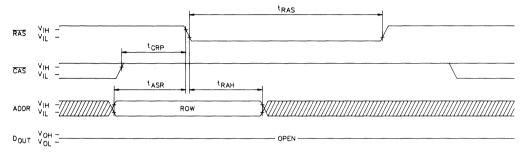
# PAGE-MODE EARLY-WRITE CYCLE



# MICRON

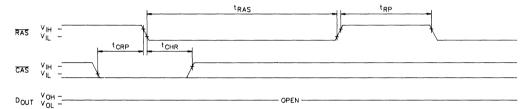
### **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0 - A_7$ ;  $A_8$  and  $\overline{WE}$  = DON'T CARE.)



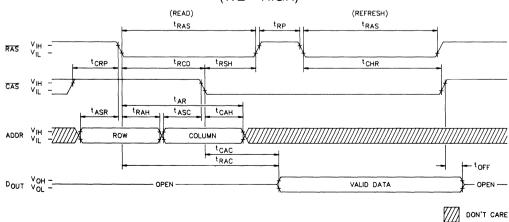
# **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_8 \overline{WE}, \overline{OE} = DON'T CARE.)$ 



# **HIDDEN REFRESH CYCLE**

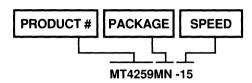
 $(\overline{WE} = HIGH)$ 





### ORDER INFORMATION

256K x 4, 150ns access, Leaded SIP



The Micron 256K x 4 DRAM module is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in

Micron's modern Boise, Idaho USA facility using the NMOS double-poly process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

# DRAM MODULES

# 256K x 5 DRAM

### **FEATURES**

ODTIONIC

- Industry standard pin-out in a 24-pin single-in-line memory module
- Low profile (0.415 inch, typical)
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 75mW standby, 750mW active, typical

A CADICIDAC

- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: RAS only, CAS before RAS, and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS	MAKKING
Timing	
80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15
Organization	
256K x 5	MT85259
Packages: Leaded 24-pin SIP	MN

PIN AS	SSIGNMENT	(Top View	ı)
A8 VDD D1 Q1 CAS A7 A5 A4 D2 Q2 W A1 A3 A6 Q3 D3 A2 A0 RAS D4 VSS D5 Q5	(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13) (14) (15) (16) (17) (18) (19) (20) (21) (22) (23) (24)	MT85259MN	
	<u> </u>	МВ	•

A0-A8	Address Inputs	CAS	Column Address Strobe
D1 - D5	Data-In	Q1 - Q5	Data-Out
RAS	Row Address Strobe	W	Write Enable
VDD	Power (+5V)	Vss	Ground

### **GENERAL DESCRIPTION**

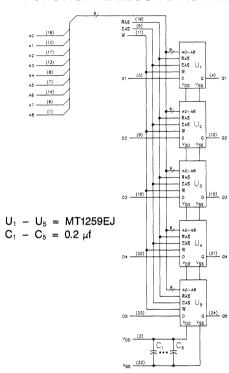
The MT85259MN is a randomly accessed solid-state memory containing 262,144 bits organized in a x5 configuration. The 16 address bits are entered 8 bits at a time using RAS to latch the first 8 bits and CAS the latter 8 bits. If the

WE pin goes low prior to CAS going low, the output pin remains open until the next CAS cycle.

By holding  $\overline{RAS}$  low,  $\overline{CAS}$  may be toggled to execute several faster READ or WRITE cycles within the  $\overline{RAS}$  address defined PAGE boundary. Returning  $\overline{RAS}$  high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high-time. Memory cell data is retained in its correct state by maintaining power and executing a  $\overline{RAS}$  (Refresh) cycle so that all 256 combinations of  $\overline{RAS}$  addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.



# **FUNCTIONAL BLOCK DIAGRAM**



# **FUNCTIONAL TRUTH TABLE**

-	510	010	WE	Addr	esses		NOTES
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	I	Н	Н	X	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	х	Х	High Impedance	



### **ABSOLUTE MAXIMUM RATINGS\***

 \*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (0°C $\leq$ T $_{A}$ $\leq$ 70°C) (Vcc = 5.0V $\pm10\%$ )

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1
INPUT LEAKAGE Input leakage current, any input (0V $\leq$ Vin $\leq$ Vcc), all other pins not under test = 0 volts	lı	-50	50	μА	
OUTPUT LEAKAGE Output leakage current (Dou⊤ is disabled, 0V ≤ Vou⊤ ≤ Vcc)	loz	-50	50	μА	
OUTPUT LEVELS Output High (Logic 1) voltage (IouT = -5mA) Output Low (Logic 0) voltage (IouT = 5mA)	Vон Vol	2.4	0.4	V	1

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels (RAS = CAS = VIH after 8 RAS cycles)	lcc1	25	25	25	25	mA	
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc2	325	275	275	225	mA	2
OPERATING CURRENT: PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc3	325	275	275	225	mA	2
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih: trc = trc(MIN))	ICC4	275	200	200	175	mA	2
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = cycling, trc = trc(MIN))	lcc5	325	275	275	225	mA	2,19

#### CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As)	Cıı		25	pF	17
Input Capacitance RAS, CAS, WE	C <sub>12</sub>		40	pF	17
Output Capacitance Dout, DIN	Co		7	pF	17



# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 3, 4, 5, 10, 11, 17, 18) (0°C $\leq$ T $_{A} \leq$ 70°C) (Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS			8		10		12		15		<del></del>
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	<sup>t</sup> PC	75		90		100		120		ns	6, 7
Access time from RAS	t <sub>RAC</sub>		80		100		120		150	ns	7, 8
Access time from CAS	t <sub>CAC</sub>		40		50		60		75	ns	7, 9
RAS pulse width	t <sub>RAS</sub>	80	10,000	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	<sup>t</sup> RSH	40		50		60		75		ns	
RAS precharge time	t <sub>RP</sub>	60		80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	40	10,000	60	10,000	60	10,000	75	10,000	ns	
CAS hold time	t <sub>CSH</sub>	80		110		120		150		ns	
CAS precharge time	t <sub>CPN</sub>	20		25		25		30		ns	18
CAS precharge time (PAGE-MODE)	<sup>t</sup> CP	25		30		30		35		ns	
RAS to CAS delay time	t <sub>RCD</sub>	20	40	25	50	25	60	25	75	ns	13
CAS to RAS set-up time	t <sub>CRP</sub>	10		15		20		20		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		0		ns	
Row address hold time	t <sub>RAH</sub>	15		15		15		15		ns	
Column address set-up time	t <sub>ASC</sub>	0		0		0		0		ns	
Column address hold time	<sup>t</sup> CAH	15		20		20		25		ns	
Column address hold time referenced to RAS	<sup>t</sup> AR	50		70		80		100		ns	
READ command hold time referenced to CAS	<sup>t</sup> RCH	0		0		0		0		ns	14
READ command hold time	<sup>t</sup> RRH	0		0		0		0		ns	
referenced to RAS					ļ				ļ	ļ	-
Output buffer turn-off delay	t <sub>OFF</sub>	0	25	0	30	0	30	0	35	ns	12
WE command set-up time	twcs	0		0	<del>  </del>	0		0		ns	-
WRITE command hold time	tWCH	15	-	35	ļ	40	ļ	45		ns	<u> </u>
WRITE command hold time referenced to RAS	tWCR	35		85		100		120		ns	
WRITE command pulse width	t <sub>WP</sub>	15		35		40		45		ns	
WRITE command to RAS lead time	<sup>t</sup> RWL	35		35		40		45		ns	
WRITE command to CAS lead time	tCWL	35		35		40		45		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		0		ns	15
Data-in hold time	t <sub>DH</sub>	15		35		40		45		ns	15
Data-in hold time referenced to RAS	t <sub>DHR</sub>	35		85		100		120		ns	
Transition time (rise or fall)	<sup>t</sup> T	3	100	3	100	3	100	3	100	ns	5, 16
Refresh Period (256 cycles)	tREF		4		4		4		4	ms	1
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		10		ns	19
CAS hold time (CAS-before-RAS refresh)	tCHR	15		20		25		30		ns	19

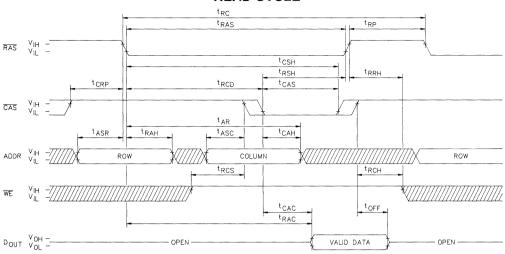
### **NOTES**

- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
- 4. AC characteristics assume  ${}^{t}T = 5$ ns.
- 5. VIH min and VII. max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VII..
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>Δ</sub> ≤ 70°C) is assured.
- Measured with a load equivalent to 2 TTL gates and 100pF.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 9. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 10. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 11. If  $\overline{\text{CAS}} = \text{Vil.}$ , data output may contain data from the last valid READ cycle.

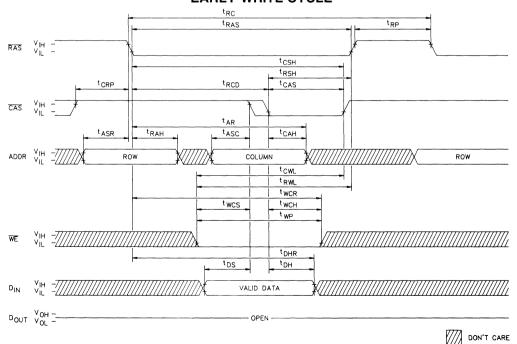
- 12. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VoII or VoII.
- 13. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 14.  ${}^{t}RCH$  is referenced to the first rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ .
- 15. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIL and VIH) in a monotonic manner.
- 17. Capacitance calculated from the equation C =  $\underline{I\Delta t}$   $\Delta V$  with  $\Delta V$  = 3V and VCC = 5V. This parameter is sampled.
- 18. If CAS is low at the falling edge of RAS, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CP. Note 8 applies to determine valid data out.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set WE = LOW.

MICRON

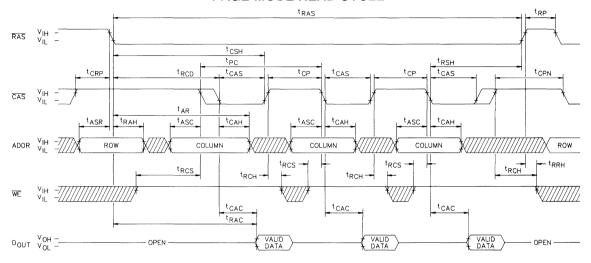
# **READ CYCLE**



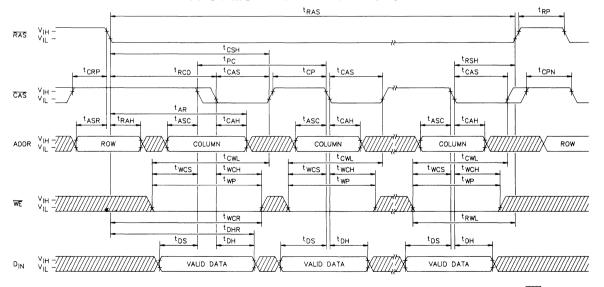
# **EARLY-WRITE CYCLE**



### PAGE-MODE READ CYCLE

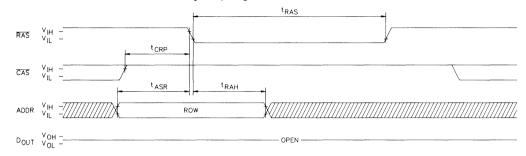


### PAGE-MODE EARLY-WRITE CYCLE



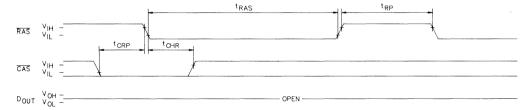
# **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0 - A_7$ ;  $A_8$  and  $\overline{WE} = DON'T CARE.)$ 



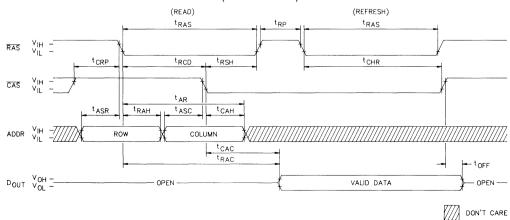
# **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_8 \overline{WE}, \overline{OE} = DON'T CARE.)$ 



# **HIDDEN REFRESH CYCLE**

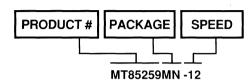
 $(\overline{WE} = HIGH)$ 





#### ORDER INFORMATION

256K x 5, 120ns access, Leaded SIP



The Micron 256K x 5 DRAM module is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in

Micron's modern Boise, Idaho USA facility using the NMOS double-poly process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. .

# DRAM MODULES

# 256K x 8 DRAM

#### **FEATURES**

- Industry standard pin-out in a 30-pin single-in-line package
- Low profile, double-side mount (0.45 in)
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 135mW standby, 1350mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: RAS only, CAS before RAS, and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS	MARKING
Timing	
80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15
• Organization 256K x 8	MT8259
• Packages: Leaded 30-pin SIP (low profile)	DMN

A0-A8	Address Inputs	CAS	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
PRD	Presence Detect	Q9	Data-Out
RAS	Row Address Strobe	W	Write Enable
Vcc	Power (+5V)	Vss	Ground

### **GENERAL DESCRIPTION**

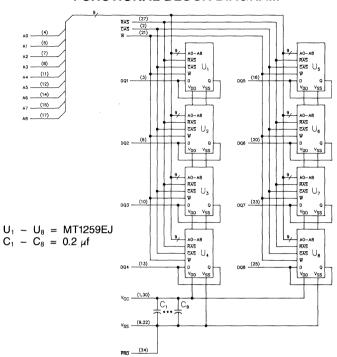
The MT8259DMN is a randomly accessed solid-state memory containing 262,144 bits organized in a x8 configuration. The 18 address bits are entered 9 bits at a time using RAS to latch the first 9 bits and CAS the latter 9 bits. If the

PIN AS	SIGNMEN	Γ (Top Vi	ew)
VCC CAS DQ1 A0 A1 DQ2 A2 A3 VSS DQ3 A4 A5 DQ4 A6 A7 DQ5 A8 NC NC DQ6 W VSS DQ7 PRD DQ8 NC PRS NC NC COVCC	(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13) (14) (15) (16) (17) (18) (19) (20) (21) (22) (23) (24) (25) (26) (27) (28) (29) (30)	MT8259DMN	ME

 $\overline{\text{WE}}$  pin goes low prior to  $\overline{\text{CAS}}$  going low, the output pin remains open until the next  $\overline{\text{CAS}}$  cycle.

By holding  $\overline{RAS}$  low,  $\overline{CAS}$  may be toggled to execute several faster READ or WRITE cycles within the  $\overline{RAS}$  address defined PAGE boundary. Returning  $\overline{RAS}$  high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high-time. Memory cell data is retained in its correct state by maintaining power and executing a  $\overline{RAS}$  (Refresh) cycle so that all 256 combinations of  $\overline{RAS}$  addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

# **FUNCTIONAL BLOCK DIAGRAM**



# **FUNCTIONAL TRUTH TABLE**

	RAS	CAS	WE	Addr	esses		NOTES
Function	HAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	Х	High Impedance	
READ	L	L	Н	ROW	COL	Ďata Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	



### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V	to +7.0V
Operating Temperature, TA(Ambient)0°C	to +70°C
Storage Temperature55°C to	+150°C
Power Dissipation	8 Watt
Short Circuit Output Current	50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (0°C $\leq$ T<sub>A</sub> $\leq$ 70°C) (Vcc = 5.0V $\pm$ 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1
INPUT LEAKAGE Input leakage current, any input (0V $\leq$ Vin $\leq$ Vcc), all other pins not under test = 0 volts	lı .	-80	80	μΑ	
OUTPUT LEAKAGE Output leakage current (Dou⊤ is disabled, 0V ≤ Vou⊤ ≤ Vcc)	loz	-80	80	μΑ	
OUTPUT LEVELS Output High (Logic 1) voltage (lout = -5mA)	Vон	2.4		V	1
Output Low (Logic 0) voltage (lout = 5mA)	Vol	ļ	0.4	V	

			MAX				
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels (RAS = CAS = Vih after 8 RAS cycles)	lcc1	40	40	40	40	mA	
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc2	500	440	440	360	mA	2
OPERATING CURRENT: PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc3	520	440	440	360	mA	2
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = VIH: trc = trc(MIN))	Icc4	440	320	320	280	mA	2
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = cycling, trc = trc(MIN))	lcc5	520	440	440	360	mA	2,19

### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As)	C <sub>I1</sub>		40	pF	17
Input Capacitance RAS, CAS, WE	C <sub>12</sub>		64	pF	17
Output Capacitance Dout, DIN	Co		12	pF	17



# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 3, 4, 5, 10, 11, 17, 18) (0°C $\leq$ T $_{A}$ $\leq$ 70°C) (Vcc = 5.0V $\pm10\%$ )

A.C. CHARACTERISTICS		-	8	-	10	-1	12	-	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	<sup>t</sup> PC	75		90		100		120		ns	6, 7
Access time from RAS	<sup>t</sup> RAÇ		80		100		120		150	ns	7, 8
Access time from CAS	t <sub>CAC</sub>		40		50		60		75	ns	7, 9
RAS pulse width	t <sub>RAS</sub>	80	10,000	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	t <sub>RSH</sub>	40		50		60		75		ns	
RAS precharge time	t <sub>RP</sub>	60		80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	40	10,000	60	10,000	60	10,000	75	10,000	ns	
CAS hold time	t <sub>CSH</sub>	80		110		120		150		ns	
CAS precharge time	<sup>t</sup> CPN	20		25		25		30		ns	18
CAS precharge time (PAGE-MODE)	<sup>t</sup> CP	25		30		30		35		ns	
RAS to CAS delay time	t <sub>RCD</sub>	20	40	25	50	25	60	25	75	ns	13
CAS to RAS set-up time	t <sub>CRP</sub>	10		15		20		20		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		. 0		0		ns	
Row address hold time	t <sub>RAH</sub>	15		15		15		15		ns	
Column address set-up time	t <sub>ASC</sub>	0		0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		20		20		25		ns	
Column address hold time referenced to RAS	<sup>t</sup> AR	50		70		80		100		ns	
READ command hold time referenced to CAS	<sup>t</sup> RCH	0		0		0		0		ns	14
READ command hold time referenced to RAS	<sup>t</sup> RRH	0		0		0		0		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	25	0	30	0	30	0	35	ns	12
WE command set-up time	twcs	0		0		0		0		ns	16
WRITE command hold time	tWCH	15		35		40		45		ns	
WRITE command hold time referenced to RAS	tWCR	35		85		100		120		ns	
WRITE command pulse width	t <sub>WP</sub>	15		35		40		45		ns	
WRITE command to RAS lead time	t <sub>RWL</sub>	35		35		40		45		ns	
WRITE command to CAS lead time	t <sub>CWL</sub>	35		35		40		45		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		0		ns	15
Data-in hold time	t <sub>DH</sub>	15		35		40		45		ns	15
Data-in hold time	t <sub>DHR</sub>	35		85		100		120		ns	
referenced to RAS											
Transition time (rise or fall)	t <sub>T</sub>	3	100	3	100	3	100	3	100	ns	5, 16
Refresh Period (256 cycles)	t <sub>REF</sub>		4		4		4		4	ms	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		10		ns	19
CAS hold time (CAS-before-RAS refresh)	tCHR	15		20		25		30		ns	19

# MICRON

#### **NOTES**

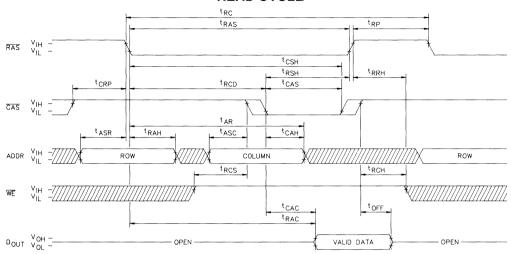
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- An initial pause of 100μs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
- 4. AC characteristics assume  ${}^{t}T = 5$ ns.
- 5. VIII min and VII. max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VII.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>Δ</sub> ≤ 70°C) is assured.
- 7. Measured with a load equivalent to 2 TTL gates and 100pF.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 9. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 10. If  $\overline{CAS} = V_{1H}$ , data output is high impedance.
- 11. If  $\overline{CAS} = V_{1L}$ , data output may contain data from the last valid READ cycle.
- 12. <sup>t</sup>OFF (max) defines the time at which the output

- achieves the open circuit condition and is not referenced to Voh or Vol.
- 13. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 14. <sup>t</sup>RCH is referenced to the first rising edge of RAS or CAS.
- 15. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 17. Capacitance calculated from the equation  $C = \underline{I\Delta t} \Delta V$  with  $\Delta V = 3V$  and Vcc = 5V. This parameter is
  - with  $\Delta V = 3V$  and VCC = 5V. This parameter is sampled.

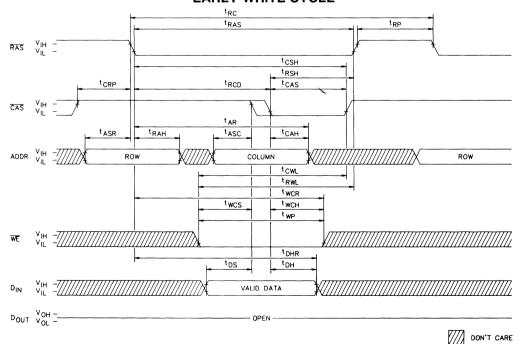
    If  $\overline{CAS}$  is low at the falling edge of  $\overline{RAS}$ . Dougly
- 18. If CAS is low at the falling edge of RAS, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CP. Note 8 applies to determine valid data out.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set  $\overline{WE}$  = LOW.



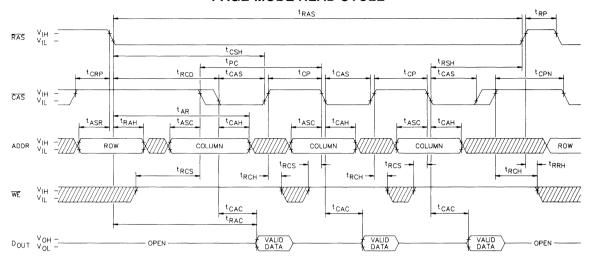
#### **READ CYCLE**



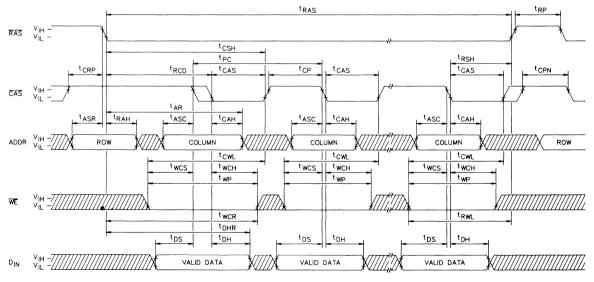
# **EARLY-WRITE CYCLE**



#### PAGE-MODE READ CYCLE

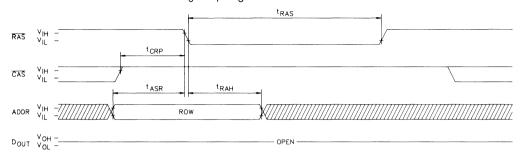


## PAGE-MODE EARLY-WRITE CYCLE



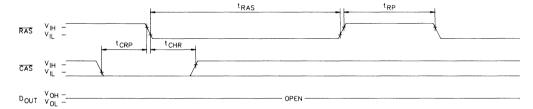
## RAS-BEFORE-CAS REFRESH CYCLE

 $(ADDR = A_0 - A_7; A_8 \text{ and } \overline{WE} = DON'T \text{ CARE.})$ 

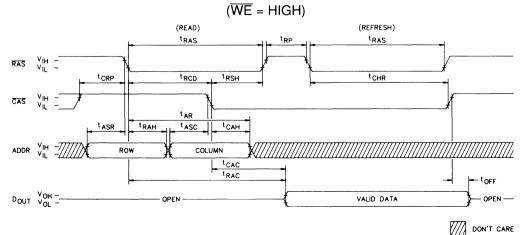


# **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_8 \overline{WE}, \overline{OE} = DON'T CARE.)$ 



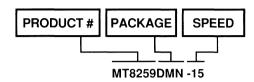
# **HIDDEN REFRESH CYCLE**





#### ORDER INFORMATION

256K x 8, 150ns access, Leaded SIP



The Micron 256K x 8 DRAM module is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in

Micron's modern Boise, Idaho USA facility using the NMOS double-poly process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>IM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.



# DRAM MODULES

# 256K x 8 DRAM

#### **FEATURES**

- Industry standard pin-out in a 30-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 120mW standby, 1200mW active, typical
- On-board power supply decoupling capacitors (0.2μf) for low noise
- Refresh modes: RAS only, CAS before RAS, and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS M.	ARKING
Timing	
80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15
<ul> <li>Organization 256K x 8</li> <li>Packages: Leadless 30-pin SIMM Leaded 30-pin SIP</li> </ul>	MT8259 M MN

A0-A8	Address Inputs	CAS	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
PRD	Presence Detect	Q9	Data-Out
RAS	Row Address Strobe	W	Write Enable
Vcc	Power (+5V)	Vss	Ground

#### GENERAL DESCRIPTION

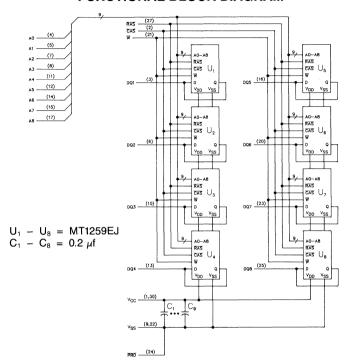
The MT8259M/MN is a randomly accessed solid-state memory containing 262,144 bits organized in a x8 configuration. The 18 address bits are entered 9 bits at a time using RAS to latch the first 9 bits and CAS the latter 9 bits. If the

VDD (1) CAS (2) DQ1 (3) A0 (4) A1 (5) DQ2 (6) A2 (7) A3 (8) VSS (9) DQ3 (10) A4 (11) A5 (12) DQ4 (13) A6 (14) A7 (15) DQ5 (16) A8 (17) NC (18) NC (18) NC (18) DQ6 (20) W (21) VSS (22) DQ7 (23) PRD (24) DQ8 (25) DQ7 (23) PRD (24) DQ8 (25) DQ9 (26) PAS (27) CAS9 (28) D9 (29) VDD (30)
MD MI

 $\overline{\text{WE}}$  pin goes low prior to  $\overline{\text{CAS}}$  going low, the output pin remains open until the next  $\overline{\text{CAS}}$  cycle.

By holding RAS low, CAS may be toggled to execute several faster READ or WRITE cycles within the RAS address defined PAGE boundary. Returning RAS high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the RAS high-time. Memory cell data is retained in its correct state by maintaining power and executing a RAS (Refresh) cycle so that all 256 combinations of RAS addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

#### **FUNCTIONAL BLOCK DIAGRAM**



## **FUNCTIONAL TRUTH TABLE**

	<b>B.1.</b>			Addresses			
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	H	Х	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	



#### **ABSOLUTE MAXIMUM RATINGS\***

 \*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS $(0^{\circ}C \le T_{\Delta} \le 70^{\circ}C) \ (Vcc = 5.0V \pm 10\%)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	· VIL	-1.0	0.8	٧	1
INPUT LEAKAGE Input leakage current, any input (0V $\leq$ VIN $\leq$ VCC), all other pins not under test = 0 volts	lı .	-80	80	μА	
OUTPUT LEAKAGE Output leakage current (Doυτ is disabled, 0V ≤ Voυτ ≤ Vcc)	loz	-80	80	μА	
OUTPUT LEVELS Output High (Logic 1) voltage (Iout = -5mA)	Vон	2.4		V	1
Output Low (Logic 0) voltage (lout = 5mA)	Vol	1	0.4	l V	

		МАХ					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels (RAS = CAS = ViH after 8 RAS cycles)	lcc1	40	40	40	40	mA	
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc2	520	440	440	360	mA	2
OPERATING CURRENT: PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc3	520	440	440	360	mA	2
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih: trc = trc(MIN))	lcc4	440	320	320	280	mA	2
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = cycling, trc = trc(MIN))	lcc5	520	440	440	360	mA	2,19

## **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As)	C <sub>I1</sub>		40	pF	17
Input Capacitance RAS, CAS, WE	C12		64	pF	17
Output Capacitance Dout, DIN	Co		12	pF	17



# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 3, 4, 5, 10, 11, 17, 18) (0°C $\leq$ T $_A$ $\leq$ 70°C) (Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS		-	8	-	10	-1	12	-	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	<sup>t</sup> PC	75		90		100		120		ns	6, 7
Access time from RAS	t <sub>RAC</sub>		80		100		120		150	ns	7, 8
Access time from CAS	t <sub>CAC</sub>		40		50		60		75	ns	7, 9
RAS pulse width	t <sub>RAS</sub>	80	10,000	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	t <sub>RSH</sub>	40		50		60		75		ns	
RAS precharge time	t <sub>RP</sub>	60		80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	40	10,000	60	10,000	60	10,000	75	10,000	ns	
CAS hold time	t <sub>CSH</sub>	80		110		120		150		ns	
CAS precharge time	<sup>t</sup> CPN	20		25		25		30		ns	18
CAS precharge time (PAGE-MODE)	<sup>t</sup> CP	25		30		30		35		ns	
RAS to CAS delay time	t <sub>RCD</sub>	20	40	25	50	25	60	25	75	ns	13
CAS to RAS set-up time	tCRP	10		15		20		20		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	15		15		15		15		ns	
Column address set-up time	t <sub>ASC</sub>	0		0		0		0		ns	
Column address hold time	<sup>t</sup> CAH	15		20		20		25		ns	
Column address hold time referenced to RAS	t <sub>AR</sub>	50		70		80		100		ns	
READ command hold time referenced to CAS	<sup>t</sup> RCH	0		0		0		0		ns	14
READ command hold time referenced to RAS	<sup>t</sup> RRH	0		0		0		0		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	25	0	30	0	30	0	35	ns	12
WE command set-up time	twcs	0		0		0		0		ns	
WRITE command hold time	tWCH	15		35		40		45		ns	
WRITE command hold time referenced to RAS	tWCR	35		85		100		120		ns	
WRITE command pulse width	t <sub>WP</sub>	15		35		40		45		ns	
WRITE command to RAS lead time	t <sub>RWL</sub>	35		35		40		45		ns	
WRITE command to CAS lead time	<sup>t</sup> CWL	35		35		40		45		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		0		ns	15
Data-in hold time	t <sub>DH</sub>	15		35		40		45		ns	15
Data-in hold time referenced to RAS	<sup>t</sup> DHR	35		85		100		120		ns	
Transition time (rise or fall)	t <sub>T</sub>	3	100	3	100	3	100	3	100	ns	5, 16
Refresh Period (256 cycles)	tREF		4		4		4		4	ms	
CAS set-up time (CAS-before-RAS refresh)	<sup>t</sup> CSR	10		10		10		10		ns	19
CAS hold time (CAS-before-RAS refresh)	<sup>t</sup> CHR	15		20		25		30		ns	19

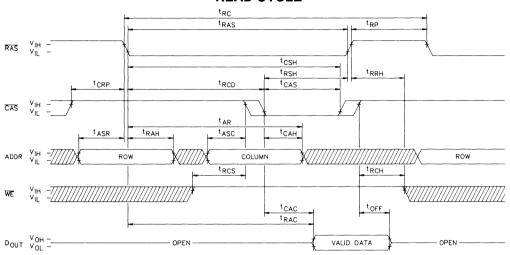
# DRAM MODULES

#### **NOTES**

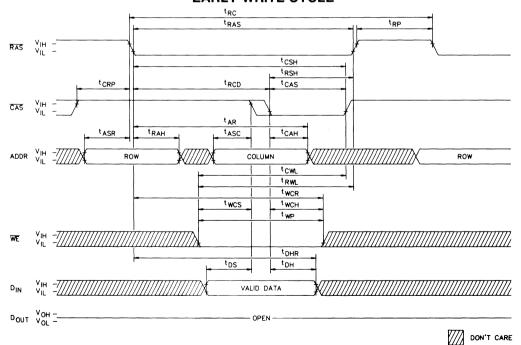
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of  $100\mu s$  is required after power-up followed by any  $8 \overline{RAS}$  cycles before proper device operation is assured. The  $8 \overline{RAS}$  cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
- 4. AC characteristics assume  ${}^{t}T = 5ns$ .
- 5. Vih min and Vil max are reference levels for measuring timing of input signals. Transition times are measured between Vih and Vil.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C  $\leq$  T $_{\rm A}$   $\leq$  70°C) is assured.
- Measured with a load equivalent to 2 TTL gates and 100pF.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 9. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 10. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 11. If  $\overline{\text{CAS}} = \text{Vil}$ , data output may contain data from the last valid READ cycle.

- 12. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 14.  ${}^{t}RCH$  is referenced to the first rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ .
- 15. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIL and VIH) in a monotonic manner.
- 17. Capacitance calculated from the equation C =  $\underline{L\Delta t}$   $\Delta V$  with  $\Delta V$  = 3V and VCC = 5V. This parameter is sampled.
- 18. If CAS is low at the falling edge of RAS, Dout will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CP. Note 8 applies to determine valid data out.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set WE = LOW.

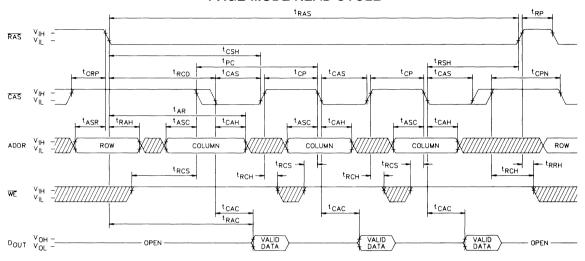
#### **READ CYCLE**



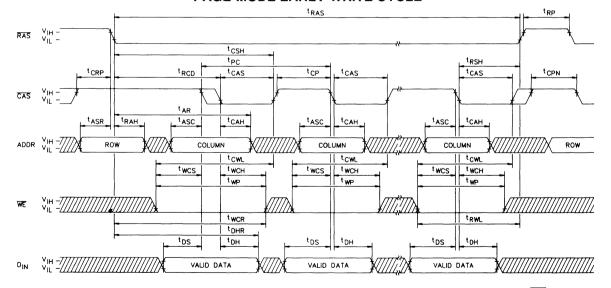
# **EARLY-WRITE CYCLE**



#### **PAGE-MODE READ CYCLE**



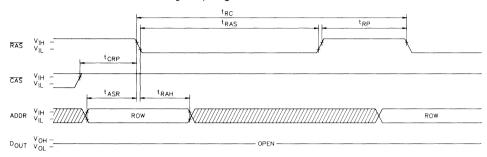
# PAGE-MODE EARLY-WRITE CYCLE



DOUT VOH -

## RAS-BEFORE-CAS REFRESH CYCLE

(ADDR =  $A_0 - A_7$ ;  $A_8$  and  $\overline{WE} = DON'T CARE.)$ 



## CAS-BEFORE-RAS REFRESH CYCLE

 $(A_0 - A_8 \overline{WE}, \overline{OE} = DON'T CARE.)$   $(A_0 - A_8 \overline{WE}, \overline{OE} = DON'T CARE.)$ 

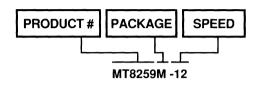
# **HIDDEN REFRESH CYCLE**

 $(\overline{WE} = HIGH)$ (READ) (REFRESH) t<sub>RAS</sub> t CHR t CRP <sup>t</sup>RCD <sup>t</sup>RSH t AR t ASC t<sub>CAH</sub> COLUMN t<sub>CAC</sub> t<sub>RAC</sub> DOUT VOH -VALID DATA OPEN ---DON'T CARE ated burn-in and several hours of AMBYX™ system level

testing prior to final test and shipment.

#### ORDER INFORMATION

256K x 8, 120ns access, Leaded SIP



The Micron 256K x 8 DRAM module is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in

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# DRAM MODULES

# 256K x 9 DRAM

#### **FEATURES**

- Industry standard pin-out in a 30-pin single-in-line package (SIP)
- Low profile, double-side mount (0.45 in)
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible.
- Low power, 135mW standby, 1350mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes:  $\overline{RAS}$  only,  $\overline{CAS}$  before  $\overline{RAS}$ , and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS	MARKING
<ul> <li>Timing</li> </ul>	
80ns access	-8
100ns access ,	-10
120ns access	-12
150ns access	-15
• Organization 256K x 9	MT9259
• Packages: Leaded 30-pin SIP (low profile)	DMN

A0-A8	Address Inputs	CAS, CAS9	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
PRD	Presence Detect	Q9	Data-Out
RAS	Row Address Strobe	$\overline{\mathbb{W}}$	Write Enable
Vcc	Power (+5V)	Vss	Ground

#### GENERAL DESCRIPTION

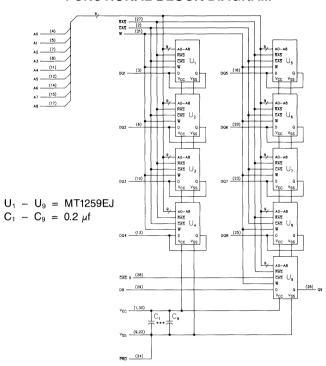
The MT9259DMN is a randomly accessed solid-state memory containing 262,144 bits organized in a x9 configuration. The 18 address bits are entered 9 bits at a time using RAS to latch the first 9 bits and CAS the latter 9 bits. If the

PIN AS	SIGNMEN	Γ (Top Vi	ew)
VCC CAS DQ1 A0 A1 DQ2 A2 A3 VSS DQ3 A4 A5 DQ4 A6 A7 DQ5 A8 NC NC DQ6 W VSS DQ7 PRD DQ8 NC RAS NC NC VCC	(1) (2) (3) (4) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13) (14) (15) (16) (17) (18) (20) (21) (22) (23) (24) (25) (26) (27) (28) (29) (30)	MT9259DMN	ME

 $\overline{\text{WE}}$  pin goes low prior to  $\overline{\text{CAS}}$  going low, the output pin remains open until the next  $\overline{\text{CAS}}$  cycle.

By holding RAS low, CAS may be toggled to execute several faster READ or WRITE cycles within the RAS address defined PAGE boundary. Returning RAS high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the RAS high-time. Memory cell data is retained in its correct state by maintaining power and executing a RAS (Refresh) cycle so that all 256 combinations of RAS addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

# **FUNCTIONAL BLOCK DIAGRAM**



# **FUNCTIONAL TRUTH TABLE**

		A10	·	Addr	esses		
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on VCC supply relative to Vss	1.0V to +7.0V
Operating Temperature, TA(Ambient)	0°C to +70°C
Storage Temperature	55°C to +150°C
Power Dissipation	9 Watt
Short Circuit Output Current	50m A

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (0°C $\leq$ T $_{A}$ $\leq$ 70°C) (Vcc = 5.0V $\pm10\%$ )

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V $\leq$ Vin $\leq$ Vcc), all other pins not under test = 0 volts	łı	-90	90	μΑ	
OUTPUT LEAKAGE Output leakage current (Doυτ is disabled, 0V ≤ Voυτ ≤ Vcc)	loz	-90	90	μΑ	
OUTPUT LEVELS Output High (Logic 1) voltage (Iout = -5mA)	Vон	2.4		V	1
Output Low (Logic 0) voltage (Iout = 5mA)	Vol	ł	0.4	V	1

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels (RAS = CAS = VIH after 8 RAS cycles)	lcc1	45	45	45	45	mA	
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc2	585	495	495	405	mA	2
OPERATING CURRENT: PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc3	585	495	495	405	mA	2
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih: trc = trc(MIN))	ICC4	495	360	360	315	mA	2
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = cycling, trc = trc(MIN))	lcc5	585	495	495	405	mA	2,19

## **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As)	C <sub>I1</sub>		45	pF	17
Input Capacitance RAS, CAS, WE	C12		72	pF	17
Output Capacitance Dout, Din	Co		12	pF	17

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 3, 4, 5, 10, 11, 17, 18) (0°C $\leq$ T $_{A}$ $\leq$ 70°C) (Vcc = 5.0V $\pm$ 10%)

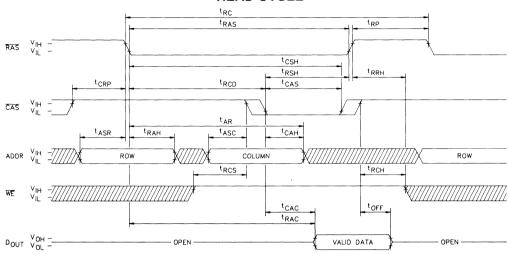
A.C. CHARACTERISTICS			8		10		12		-15		<u> </u>
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	150		195	1	230		260	ļ	ns	6, 7
PAGE-MODE cycle time	t <sub>PC</sub>	75	-	90		100		120		ns	6, 7
Access time from RAS	t <sub>RAC</sub>		80		100		120		150	ns	7, 8
Access time from CAS	t <sub>CAC</sub>		40		50		60		75	ns	7, 9
RAS pulse width	t <sub>RAS</sub>	80	10,000	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	<sup>t</sup> RSH	40		50		60		75		ns	
RAS precharge time	t <sub>RP</sub>	60		80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	40	10,000	60	10,000	60	10,000	75	10,000	ns	
CAS hold time	<sup>t</sup> CSH	80		110		120		150		ns	
CAS precharge time	t <sub>CPN</sub>	20		25		25		30		ns	18
CAS precharge time (PAGE-MODE)	<sup>t</sup> CP	25		30		30		35		ns	1
RAS to CAS delay time	<sup>t</sup> RCD	20	40	25	50	25	60	25	75	ns	13
CAS to RAS set-up time	t <sub>CRP</sub>	10		15		20		20		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0	1	0		ns	<u> </u>
Row address hold time	t <sub>RAH</sub>	15		15		15		15	1	ns	
Column address set-up time	t <sub>ASC</sub>	0		0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		20		20		25		ns	
Column address hold time referenced to RAS	tAR	50		70		80		100		ns	
READ command hold time referenced to CAS	<sup>t</sup> RCH	0		0		0		0		ns	14
READ command hold time referenced to RAS	<sup>t</sup> RRH	0		0		0		0		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	25	0	30	0	30	0	35	ns	12
WE command set-up time	twcs	0		0		0		0		ns	
WRITE command hold time	tWCH	15		35		40		45		ns	
WRITE command hold time referenced to RAS	tWCR	35		85		100		120		ns	
WRITE command pulse width	t <sub>WP</sub>	15		35		40		45		ns	
WRITE command to RAS lead time	t <sub>RWL</sub>	35		35		40		45		ns	
WRITE command to CAS lead time	<sup>t</sup> CWL	35		35		40		45		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		0		ns	15
Data-in hold time	t <sub>DH</sub>	15		35	1	40		45		ns	15
Data-in hold time referenced to RAS	t <sub>DHR</sub>	35		85		100		120		ns	
Transition time (rise or fall)	t <sub>T</sub>	3	100	3	100	3	100	3	100	ns	5. 16
Refresh Period (256 cycles)	<sup>t</sup> REF		4		4	<u> </u>	4		4	ms	1
CAS set-up time (CAS-before-RAS refresh)	<sup>t</sup> CSR	10		10		10		10		ns	19
CAS hold time (CAS-before-RAS refresh)	tCHR	15		20		25		30		ns	19

#### **NOTES**

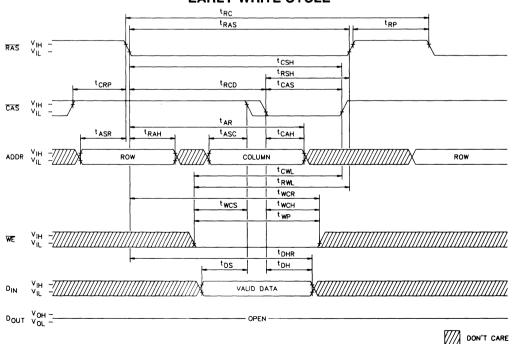
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
- 4. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C) is assured.
- 7. Measured with a load equivalent to 2 TTL gates and 100pF.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 9. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 10. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 11. If  $\overline{CAS} = V_{IL}$ , data output may contain data from the last valid READ cycle.
- 12. <sup>t</sup>OFF (max) defines the time at which the output

- achieves the open circuit condition and is not referenced to Voh or Vol.
- 13. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 14.  ${}^{t}RCH$  is referenced to the first rising edge of  $\overline{RAS}$  or  $\overline{CAS}$
- 15. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between Vih and Vil (or between VIL and VIH) in a monotonic manner.
- 17. Capacitance calculated from the equation  $C = \frac{I\Delta t}{\Delta V}$ 
  - with  $\Delta V = 3V$  and  $V_{CC} = 5V$ . This parameter is sampled.
- 18. If CAS is low at the falling edge of RAS, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CP. Note 8 applies to determine valid data out.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set  $\overline{WE}$  = LOW.

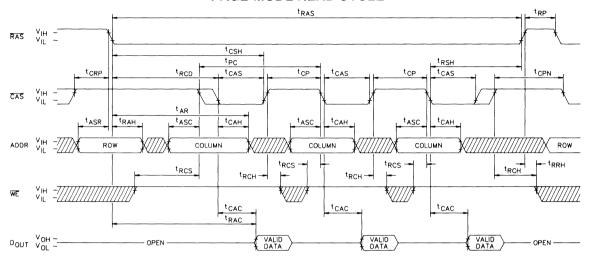
#### **READ CYCLE**



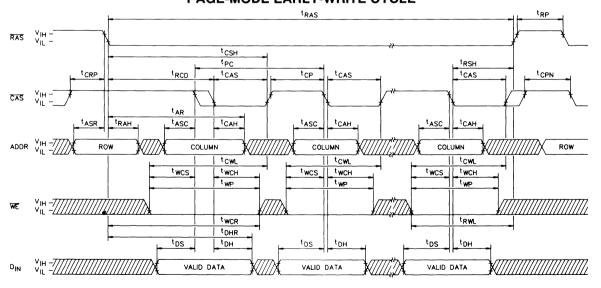
#### **EARLY-WRITE CYCLE**



#### PAGE-MODE READ CYCLE



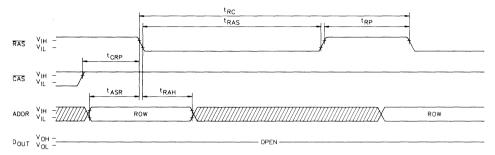
#### PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

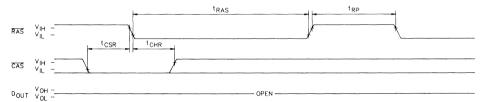
# RAS-BEFORE-CAS REFRESH CYCLE

 $(ADDR = A_0 - A_7; A_8 \text{ and } \overline{WE} = DON'T CARE.)$ 



# **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_8 \overline{WE}, \overline{OE} = DON'T CARE.)$ 

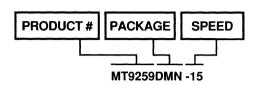


# **HIDDEN REFRESH CYCLE**

 $(\overline{WE} = HIGH)$ (READ) (REFRESH) t<sub>RAS</sub> <sup>t</sup>RSH t CHR t CRP t<sub>RCD</sub> t AR t ASC <sup>t</sup>CAH ROW COLUMN <sup>t</sup>CAC t<sub>RAC</sub> VALID DATA OPEN -

#### **ORDER INFORMATION**

256K x 9, 150ns access, Leaded SIP



The Micron 256K x 9 DRAM module is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in

Micron's modern Boise, Idaho USA facility using the NMOS double-poly process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

# DRAM MODULES

# 256K x 9 DRAM

#### **FEATURES**

- Industry standard pin-out in a 30-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 135mW standby, 1350mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: RAS only, CAS before RAS, and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS	MARKING
<ul> <li>Timing</li> </ul>	
80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15 .
Organization	
256K x 9	MT9259

•	Packages: Leadless 30-pin SIMM	M
	Leaded 30-pin SIP	MN

A0-A8	Address Inputs	CAS CAS9	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
PRD	Presence Detect	Q9	Data-Out
RA\$	Row Address Strobe	$\overline{\mathbb{W}}$	Write Enable
Vcc	Power (+5V)	Vss	Ground

#### **GENERAL DESCRIPTION**

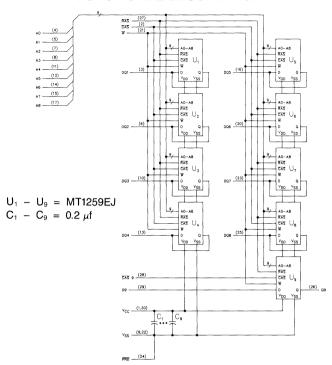
The MT9259M/MN is a randomly accessed solid-state memory containing 262,144 bits organized in a x9 configuration. The 18 address bits are entered 9 bits at a time using RAS to latch the first 9 bits and CAS the latter 9 bits. If the

	PIN ASS	IGNME	NT (Top View)
VDD CAS DQ1 A1 DQ2 A3 VSS DQ3 A4 A5 DQ4 A6 A7 DQ5 A8 NC DQ6 W VSS DQ7 PRD DQ8 Q9 FAS CAS9 VDD	(1) (2) (3) (4) (5) (6) (7) (1) (12) (13) (14) (15) (16) (17) (19) (20) (21) (23) (24) (27) (28) (29) (30)	MT9259MN	V <sub>DO</sub> 1 1 CAS 2 2 DQ1 3 3 A0 4 A1 5 DQ2 6 A2 7 A3 8 8 V <sub>SS</sub> 9 DQ3 10 A4 11 A5 12 DQ4 13 A6 14 A5 12 DQ5 16 NC 17 NC 11 NC 11 NC 11 NC 11 NC 11 DQ6 20 W 21 V <sub>SS</sub> 22 DQ7 23 NC 12 V <sub>SS</sub> 22 DQ7 23 NC 12 CAS 20 RAS 27 CAS 28 CB 28 CB 29 V <sub>DO</sub> 30
	<u> </u>	MD	
			MI

WE pin goes low prior to CAS going low, the output pin remains open until the next CAS cycle.

By holding RAS low, CAS may be toggled to execute several faster READ or WRITE cycles within the RAS address defined PAGE boundary. Returning RAS high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the RAS high-time. Memory cell data is retained in its correct state by maintaining power and executing a RAS (Refresh) cycle so that all 256 combinations of RAS addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

# **FUNCTIONAL BLOCK DIAGRAM**



#### **FUNCTIONAL TRUTH TABLE**

			VIII.	Addr	esses		
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	Χ	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	,
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	



#### **ABSOLUTE MAXIMUM RATINGS\***

 \*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (0°C $\leq$ T $_{A}$ $\leq$ 70°C) (Vcc = 5.0V $\pm10\%$ )

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V $\leq$ Vin $\leq$ Vcc), all other pins not under test = 0 volts	lı	-90	90	μА	
OUTPUT LEAKAGE Output leakage current (Do∪⊤ is disabled, 0V ≤ Vo∪⊤ ≤ Vcc)	loz	-90	90	μА	
OUTPUT LEVELS Output High (Logic 1) voltage (Iout = -5mA)	Vон	2.4		V	1
Output Low (Logic 0) voltage (lout = 5mA)	<b>V</b> ol	1	0.4	V	1

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels (RAS = CAS = ViH after 8 RAS cycles)	lcc1	45	45	45	45	mA	
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc2	585	495	495	405	mA	2
OPERATING CURRENT: PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc3	585	495	495	405	mA	2
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih: trc = trc(MIN))	Icc4	495	360	360	315	mA	2
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = cycling, the = the(MIN))	lcc5	585	495	495	405	mA	2,19

#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As)	C <sub>I1</sub>		45	pF	17
Input Capacitance RAS, CAS, WE	C <sub>12</sub>		72	pF	17
Output Capacitance Dout, DIN	Co		12	pF	17



# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 3, 4, 5, 10, 11, 17, 18) $(0^{\circ}C \leq T_{A} \leq 70^{\circ}C)$ (Vcc = 5.0V $\pm 10\%$ )

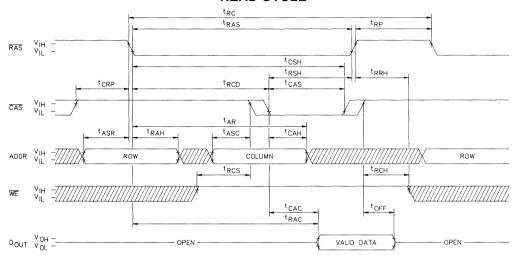
A.C. CHARACTERISTICS	-8		-10		-12		-15			<del> </del>	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC_	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	<sup>t</sup> PC	75		90		100		120		ns	6, 7
Access time from RAS	t <sub>RAC</sub>		80		100		120		150	ns	7, 8
Access time from CAS	<sup>t</sup> CAC		40		50		60		75	ns	7, 9
RAS pulse width	t <sub>RAS</sub>	80	10,000	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	t <sub>RSH</sub>	40		50		60		75		ns	
RAS precharge time	t <sub>RP</sub>	60		80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	40	10,000	60	10,000	60	10,000	75	10,000	ns	
CAS hold time	t <sub>CSH</sub>	80		110		120		150		ns	
CAS precharge time	<sup>t</sup> CPN	20		25		25		30		ns	18
CAS precharge time (PAGE-MODE)	<sup>t</sup> CP	25		30		30		35		ns	
RAS to CAS delay time	t <sub>RCD</sub>	20	40	25	50	25	60	25	75	ns	13
CAS to RAS set-up time	t <sub>CRP</sub>	10		15		20		20		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	15		15		15		15		ns	
Column address set-up time	†ASC	0		0		0		0		ns	
Column address hold time	<sup>t</sup> CAH	15		20		20		25		ns	
Column address hold time referenced to RAS	<sup>t</sup> AR	50		70		80		100		ns	
READ command hold time referenced to CAS	<sup>t</sup> RCH	0		0		0		0		ns	14
READ command hold time referenced to RAS	t <sub>RRH</sub>	0		0		0		0		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	25	0	30	0	30	0	35	ns	12
WE command set-up time	twcs	0		0		0		0		ns	
WRITE command hold time	tWCH	15		35		40		45		ns	
WRITE command hold time referenced to RAS	twcr	35		85		100		120		ns	
WRITE command pulse width	<sup>t</sup> WP	15		35		40		45		ns	
WRITE command to RAS lead time	t <sub>RWL</sub>	35		35		40		45		ns	
WRITE command to CAS lead time	tCWL	35		35		40		45		ns	
Data-in set-up time	t <sub>DS</sub>	0	ĺ	0		0		0		ns	15
Data-in hold time	tDH	15		35		40		45		ns	15
Data-in hold time referenced to RAS	<sup>t</sup> DHR	35		85		100		120		ns	
Transition time (rise or fall)	t <sub>T</sub>	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	tREF		4		4		4		4	ms	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		10		ns	19
CAS hold time (CAS-before-RAS refresh)	<sup>t</sup> CHR	15		20		25		30		ns	19

#### **NOTES**

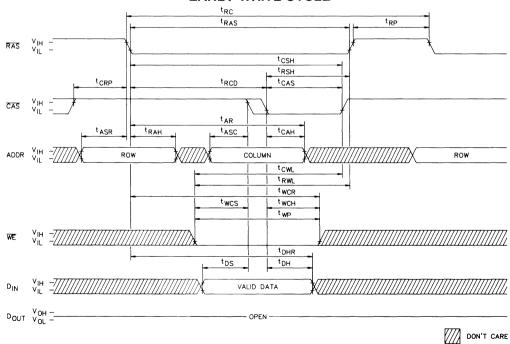
- 1. All voltages referenced to Vss.
- 2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
- 4. AC characteristics assume  ${}^{t}T = 5$ ns.
- 5. Vih min and Vil max are reference levels for measuring timing of input signals. Transition times are measured between Vih and Vil.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C) is assured.
- Measured with a load equivalent to 2 TTL gates and 100pF.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 9. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 10. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 11. If  $\overline{\text{CAS}} = \text{V}_{1L}$ , data output may contain data from the last valid READ cycle.

- 12. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 14.  ${}^{t}RCH$  is referenced to the first rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ .
- 15. These parameters are referenced to CAS leading edge in early WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 17. Capacitance calculated from the equation  $C = \underline{I\Delta t} \Delta V$  with  $\Delta V = 3V$  and Vcc = 5V. This parameter is sampled.
- 18. If CAS is low at the falling edge of RAS, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CP. Note 8 applies to determine valid data out.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set  $\overline{WE} = LOW$ .

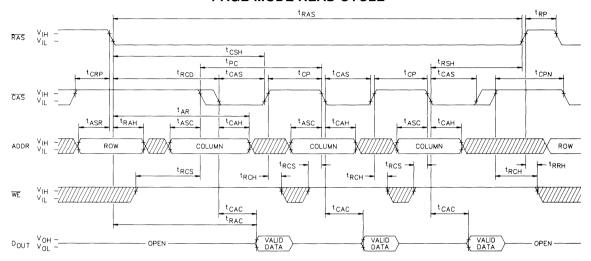
#### **READ CYCLE**



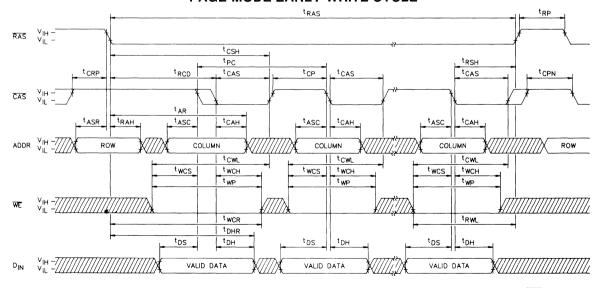
## **EARLY-WRITE CYCLE**



## **PAGE-MODE READ CYCLE**



#### PAGE-MODE EARLY-WRITE CYCLE

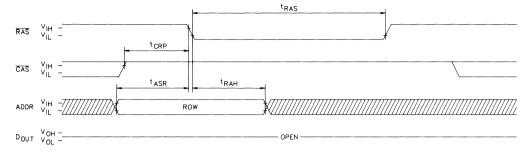


**DRAM MODULES** 



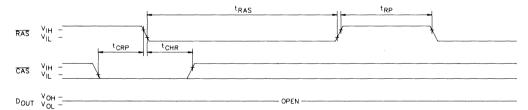
## RAS-BEFORE-CAS REFRESH CYCLE

 $(ADDR = A_0 - A_7; A_8 \text{ and } \overline{WE} = DON'T CARE.)$ 



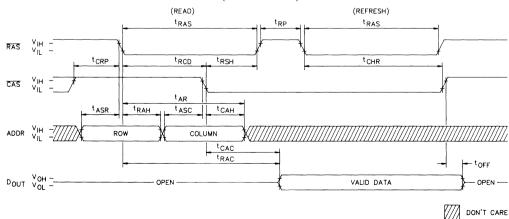
## CAS-BEFORE-RAS REFRESH CYCLE

 $(A_0 - A_8 \overline{WE}, \overline{OE} = DON'T CARE.)$ 



#### HIDDEN REFRESH CYCLE

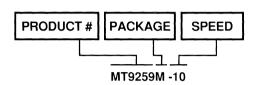
 $(\overline{WE} = HIGH)$ 





#### ORDER INFORMATION

256K x 9, 100ns access, Leadless SIP



The Micron 256K x 9 DRAM module is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in

Micron's modern Boise, Idaho USA facility using the NMOS double-poly process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burn-in and several hours of AMBYX<sup>IM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.


## DRAM MODULES

## 256K x 36 DRAM

PAGE MODE

#### **FEATURES**

256K x 36

- Industry standard pin-out in a 72-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 100mW standby, 2000mW active, typical.
- On-board power supply decoupling capacitors (0.2µf) for low noise.
- Refresh modes: RAS only, CAS before RAS, and Hidden.
- 512 cycle refresh distributed across 8ms.
- Optional Fast Page Mode.

#### OPTIONS MARKING • Timing 100ns access 120ns access -12 150ns access -15 • Organization

Packages: Leadless 72-pin SIMM M
 Leaded 72-pin SIP MN

A0-A8	Address Inputs	CASO - CAS3	Column Address Strobe
DQ0-DQ35	Data-In/Data-Out	PRD0-PRD3	Presence Detect
W	Write Enable	RASO, RAS2	Row Address Strobe
NC	No Connection	Voo	Power (+5V)
Vss	Ground		

MT8C3656

#### **GENERAL DESCRIPTION**

The MT8C3656 is a randomly accessed solid-state memory containing 262,144 bits organized in a x36 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time.  $\overline{RAS}$  is used to latch the first 9 bits and  $\overline{CAS}$  the latter 9 bits. A READ or WRITE cycle is selected with the  $\overline{WE}$  input. A logic high on  $\overline{WE}$  dictates READ mode while a logic low on  $\overline{WE}$  dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of  $\overline{WE}$  or  $\overline{CAS}$ , whichever occurs last. If  $\overline{WE}$  goes low prior to  $\overline{CAS}$  going low, the output

PIN ASSIGNMENT (Top View)								
O WIGGS WIGG								
1 35 36 72							72	
PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	
1	Vcc	19	NC	37	DQ17	55	D012	

PIN#	SAMROF	PIN#	SAMROF	PIN#	SAMROF	PIN#	SIMBOL
1	Vcc	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	Vss	57	DQ13
4	DQ1	22	DQ5	40	CASO	58	DQ31
5	DQ19	23	DQ23	41	CAS2	59	Vcc
6	DQ2	24	DQ6	42	CAS3	60	DQ32
7	DQ20	25	DQ24	43	CAS1	61	DQ14
8	DQ3	26	DQ7	44	RAS0	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ27	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ28	70	PRD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	Vss

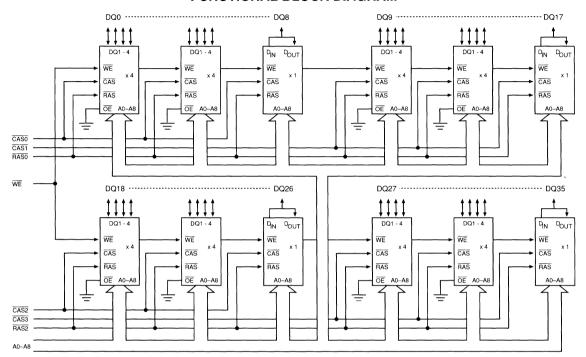
pin(s) remain open (High Z) until the next  $\overline{CAS}$  cycle. If  $\overline{WE}$  goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as  $\overline{CAS}$  remains low (regardless of  $\overline{WE}$  or  $\overline{RAS}$ ). This late  $\overline{WE}$  pulse results in a READ-WRITE cycle.

Returning RAS and CAS high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS only, CAS-before-RAS, or Hidden refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by RAS followed by a column address strobed in by CAS. By holding RAS low, CAS may be toggled strobing in different column addresses executing faster memory cycles. Returning RAS high terminates the PAGE MODE operation.

## MICRON

#### **FUNCTIONAL BLOCK DIAGRAM**



#### **FUNCTIONAL TRUTH TABLE**

	546		WE	Addr	esses		110750
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	

## MICHON

MT8C3656

#### **ABSOLUTE MAXIMUM RATINGS\***

 \*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq T_{\Delta} \leq 70^{\circ}C = 5.0V \pm 10\%)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc1		720	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		720	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ( $\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles min.)	lcc3		55	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	Icc4		28	mA	
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih)	lcc5	1	500	mA	3
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = Cycling)	lcc <sub>6</sub>		500	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V $\leq$ VIN $\leq$ Vcc), all other pins not under test = 0 volts) (For each package input)	lı .	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ Vout ≤ Vcc) (For each package input)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High voltage (lout = -5mA)	Vон	2.4		V	1
Output Low voltage (lout = 5mA)	Vol		0.4	\ V	

#### RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{{\color{blue}A}} \leq 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	
Input High (Logic 1) Voltage, All Inputs	VIH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1



#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As)	C <sub>11</sub>		60	pF	18
Input Capacitance (WE)	Ci2		84	pF	18
Input Capacitance (RAS0, RAS2)	Сіз		42	pF	18
Input Capacitance (CAS0, CAS1, CAS2, CAS3)	C14		21	pF	18
Input Capacitance (DQ0 - DQ35)	C <sub>15</sub>		7	pF	18
Output Capacitance (DQ0 - DQ35)	Co1		7	pF	18

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$   $T_{\mbox{\scriptsize A}} \leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS			10	-	12	-	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	190		220		260		ns	
PAGE-MODE READ or WRITE	t <sub>PC</sub>	90		100		120		ns	
cycle time	İ								
Access time from RAS	t <sub>RAC</sub>		100		120		150	ns	14
Access time from CAS	t <sub>CAC</sub>		50		60		75	ns	15
Access time from column address	<sup>t</sup> AA		50		60		75	ns	
Access time from CAS precharge	<sup>t</sup> CPA		50		65		75	ns	
RAS pulse width	t <sub>RAS</sub>	100	10,000	120	10,000	150	10,000	ns	
RAS pulse width (PAGE MODE)	tRASP	100	100,000	120	100,000	150	100,000	ns	
RAS hold time	<sup>t</sup> RSH	50		60		75		ns	
RAS precharge time	<sup>t</sup> RP	80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	50	10,000	60	10,000	75	10,000	ns	
CAS hold time	t <sub>CSH</sub>	100		120		150		ns	
CAS precharge time	t <sub>CPN</sub>	25		25		30		ns	16
CAS precharge time (PAGE MODE)	<sup>t</sup> CP	30		30		35		ns	
RAS to CAS delay time	t <sub>RCD</sub>	25	50	25	60	25	75	ns	17
CAS to RAS precharge time	t <sub>CRP</sub>	15		20		20		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		ns	
Row address hold time	t <sub>RAH</sub>	15		15		15		ns	
RAS to column address delay time	<sup>t</sup> RAD	20	50	20	60	20	75	ns	18
Column address set-up time	t <sub>ASC</sub>	0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	20		20		25		ns	
Column address hold time (referenced to RAS)	<sup>t</sup> AR	70		80		100		ns	
Column address to RAS lead time	<sup>t</sup> RAL	50		60		75		ns	
Read command set-up time	<sup>t</sup> RCS	0		0		0		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19



#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$  T<sub> $\Delta$ </sub>  $\leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS			10		12	-	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in low-Z	t <sub>CLZ</sub>	5		5		5		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	30	0	30	0	30	ns	20
WE command set-up time	tWCS	0		0		0		ns	21
Write command hold time	tWCH	35		40		45		ns	
Write command hold time (referenced to RAS)	tWCR	85		100		120		ns	
Write command pulse width	t <sub>WP</sub>	35		40		45		ns	
Write command to RAS lead time	t <sub>RWL</sub>	35		40		45		ns	
Write command to CAS lead time	tCWL	35		40		45		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	22
Data-in hold time	t <sub>DH</sub>	35		40		45		ns	22
Data-in hold time (referenced to RAS)	t <sub>DHR</sub>	70		80		90		ns	
RAS to WE delay time	t <sub>RWD</sub>	90		110		135		ns	21
Column address to WE delay time	<sup>t</sup> AWD	50		60		70		ns	21
CAS to WE delay time	tCWD	35		40		45		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		4		4		4	ms	
RAS to CAS Precharge time	t <sub>RPC</sub>	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	tCHR	20		25		30		ns	5

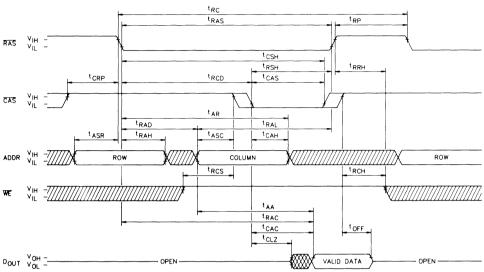
## MICHON

#### **NOTES**

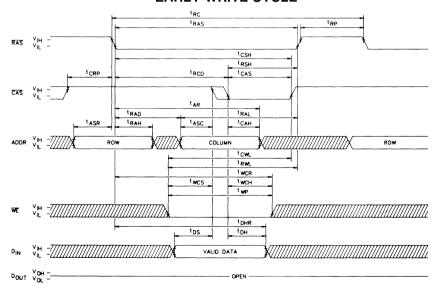
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = I\Delta t$  with  $\Delta V = 3V$  and VCC = 5V
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume <sup>t</sup>T = 5ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 11. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 12. If  $\overline{\text{CAS}} = \text{VIL}$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If  $\overline{CAS}$  is low at the falling edge of  $\overline{RAS}$ , DOUT will

- be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for  ${}^{\text{t}}\text{CPN}$ .
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle.
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 21. <sup>t</sup>WCS, <sup>t</sup>RWD, <sup>t</sup>AWD and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), <sup>t</sup>AWD ≥ <sup>t</sup>AWD (min) and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to Vih) is indeterminate
- 22. These parameters are referenced to CAS leading edge in early WRITE cycles and WE leading edge in late WRITE or READ-WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case WE = LOW.

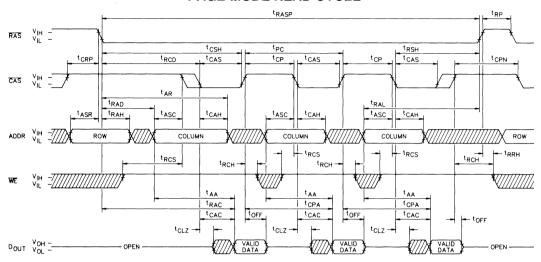
# **READ CYCLE**



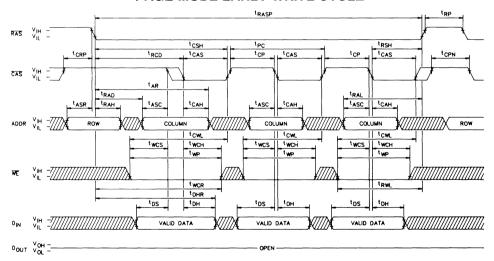
#### **EARLY-WRITE CYCLE**



#### **PAGE-MODE READ CYCLE**



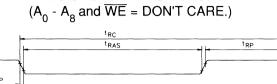
#### **PAGE-MODE EARLY-WRITE CYCLE**

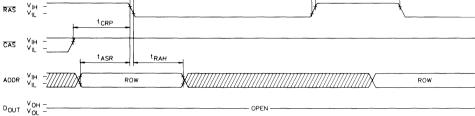


DON'T CARE

UNDEFINED

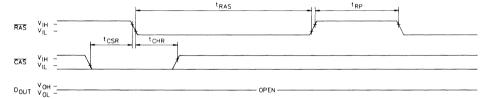
## RAS ONLY REFRESH CYCLE





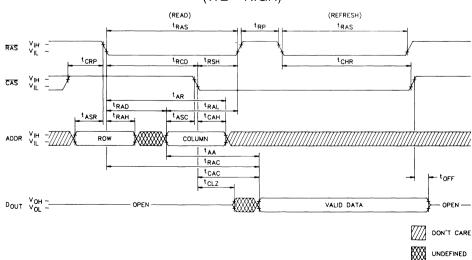
#### **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_8 \text{ and } \overline{WE} = DON'T \text{ CARE.})$ 



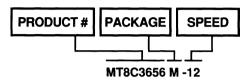
#### **HIDDEN REFRESH CYCLE**

 $(\overline{WE} = HIGH)$ 



#### ORDER INFORMATION

256K x 36, 120ns access, Page Mode Access, SIMM



The Micron DRAM module family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS and

NMOS silicon gate processes. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AM-BYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

## DRAM MODULES

## 1MEG x 8 DRAM

**FAST PAGE MODE** 

#### **FEATURES**

- Industry standard pin-out in a 30-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 40mW standby, 1400mW active, typical.
- On-board power supply decoupling capacitors (0.2µf) for low noise.
- Refresh modes: RAS only, CAS before RAS, and Hidden.
- 512 cycle refresh distributed across 8ms.
- Optional Fast Page Mode.

Access Mode Option

Fast Page Mode

# OPTIONS MARKING • Timing 80ns access 100ns access 120ns access 150ns access -15

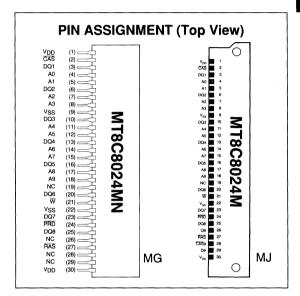
Packages:	Leadless 30-pin SIMM	M
0	Leaded 30-pin SIP	MN

A0-A9	Address Inputs	CAS, CAS9	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
PRD	Presence Detect	Q9	Data-Out
RAS	Row Address Strobe	₩	Write Enable
VDD	Power (+5V)	Vss	Ground

MT8C8024

#### **GENERAL DESCRIPTION**

The MT8C8024M/MN is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x8 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time.  $\overline{RAS}$  is used to latch the first 10 bits and  $\overline{CAS}$  the latter 10 bits. A READ or WRITE cycle is selected with the  $\overline{WE}$  input. A logic high on  $\overline{WE}$  dictates READ mode while a logic low on  $\overline{WE}$  dictates

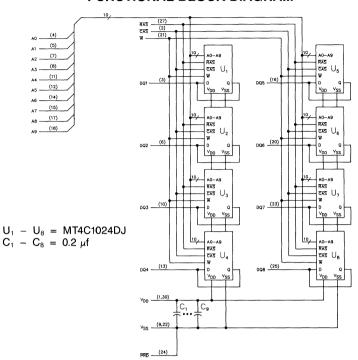


WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. If  $\overline{\text{WE}}$  goes low prior to  $\overline{\text{CAS}}$  going low, the output pin(s) remain open (High Z) until the next  $\overline{\text{CAS}}$  cycle. If  $\overline{\text{WE}}$  goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as  $\overline{\text{CAS}}$  remains low (regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ ). This late  $\overline{\text{WE}}$  pulse results in a READ-WRITE cycle.

Returning RAS and CAS high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS only, CAS-before-RAS, or Hidden refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by RAS followed by a column address strobed in by CAS. By holding RAS low, CAS may be toggled strobing in different column addresses executing faster memory cycles. Returning RAS high terminates the PAGE MODE operation.

#### **FUNCTIONAL BLOCK DIAGRAM**



#### **FUNCTIONAL TRUTH TABLE**

		~		Addr	esses		
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V to +7	'.0V
Operating Temperature, TA(Ambient)0°C to +7	0°C
Storage Temperature (Plastic)55°C to +15	0°C
Power Dissipation8 V	Vatt
Short Circuit Output Current50	mΑ

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq T_{\Delta} \leq 70^{\circ}C = 5.0V \pm 10\%)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc1		400	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		400	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS  Power supply standby current (RAS = CAS = VIH  after 8 RAS cycles min.)	lcc3		16	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	ICC4		8	mA	
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = VIH)	lcc5		280	mA	3
REFRESH CURRENT: $\overline{CAS}$ -before- $\overline{RAS}$ ( $\overline{RAS}$ and $\overline{CAS}$ = Cycling)	lcc6		280	mA	3, 5
INPUT LEAKAGE CURRENT (any input $(0V \le V_{IN} \le V_{CC})$ , all other pins not under test = 0 volts)	11	-80	80	μА	
OUTPUT LEAKAGE CURRENT (Dou⊤ is disabled, 0V ≤ Vouт ≤ Vcc)	loz	-80	80	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA) Output Levelsge (lour = FmA)	Vон Vol	2.4	0.4	V	1
Output Low voltage (Iout = 5mA)	/ VOL	1	0.4	\ V	1

#### RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{A} \leq 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1



#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9)	Cı1		40	pF	18
Input Capacitance RAS, CAS, WE	C <sub>12</sub>		56	pF	18
Output Capacitance Dout, DIN	Co		12	pF	18

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq T_{\Delta} \leq +70$ °C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS	-10		-12			15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	190		220		260		ns	
PAGE-MODE READ or WRITE cycle time	<sup>t</sup> PC	55		70		85		ns	
Access time from RAS	tRAC		100		120		150	ns	14
Access time from CAS	tCAC -		25		30		45	ns	15
Access time from column address	<sup>t</sup> AA		50		60		70	ns	
Access time from CAS precharge	t <sub>CPA</sub>		50		65		75	ns	
RAS pulse width	t <sub>RAS</sub>	100	10,000	120	10,000	150	10,000	ns	
RAS pulse width (PAGE MODE)	<sup>t</sup> RASP	100	100,000	120	100,000	150	100,000	ns	
RAS hold time	<sup>t</sup> RSH	25		30		45		ns	
RAS precharge time	<sup>t</sup> RP	80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	25	10,000	30	10,000	45	10,000	ns	
CAS hold time	t <sub>CSH</sub>	100		120		150		ns	
CAS precharge time	t <sub>CPN</sub>	15		20		25		ns	16
CAS precharge time (PAGE MODE)	<sup>t</sup> CP	10		15		20		ns	
RAS to CAS delay time	<sup>t</sup> RCD	10	75	15	90	15	105	ns	17
CAS to RAS precharge time	tCRP_	_ 10		10		10		ns	
Row address set-up time	<sup>t</sup> ASR	0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	10		15		15		ns	
RAS to column address delay time	<sup>t</sup> RAD	10	50	15	60	15	70	ns	18
Column address set-up time	t <sub>ASC</sub>	0		0		0	-	ns	
Column address hold time	t <sub>CAH</sub>	15		20		25		ns	
Column address hold time (referenced to RAS)	<sup>t</sup> AR	60		70		80		ns	
Column address to RAS lead time	<sup>t</sup> RAL	50		60		70		ns	
Read command set-up time	t <sub>RCS</sub>	0		0		0		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19
CAS to output in low-Z	tCLZ	5		5		5		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	25	0	25	0	30	ns	20
Write command hold time	twcH	20		25		30		ns	



# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq$ T $_{A}$ $\leq$ +70°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS			10	-	12	-	15	1	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time (referenced to RAS)	tWCR	70		80		90		ns	
Write command pulse width	<sup>t</sup> WP	20		25		30		ns	
Write command to RAS lead time	t <sub>RWL</sub>	25		30		35		ns	
Write command to CAS lead time	tCWL	25		30		35		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	21
Data-in hold time	t <sub>DH</sub>	15		20		25		ns	21
Data-in hold time (referenced to RAS)	t <sub>DHR</sub>	70		80		90		ns	
RAS to WE delay time	t <sub>RWD</sub>	90		110		135		ns	
Column address to WE delay time	<sup>t</sup> AWD	50		60		70		ns	
CAS to WE delay time	tCWD	. 35		40		45		ns	
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		8		8		8	ms	
RAS to CAS Precharge time	t <sub>RPC</sub>	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	tCHR	20		25		30		ns	5

#### NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and Vcc = 5V.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
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- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 11. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 12. If  $\overline{CAS} = VIL$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.

- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If <del>CAS</del> is low at the falling edge of <del>RAS</del>, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer <del>CAS</del> must be pulsed high for <sup>t</sup>CPN.
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle.
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{WE}$  = LOW.

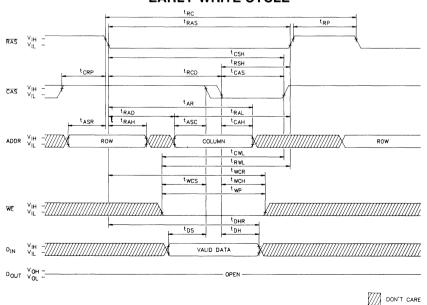


#### **READ CYCLE** tRAS tRP RAS VIH tcsh t<sub>RRH</sub> tRSH tCAS t CRP t<sub>RCD</sub> t AR tRAD t<sub>RAL</sub> t ASR t<sub>RAH</sub> tASC tCAH COLUMN tRCS t<sub>RCH</sub> tRAC tCAC t off t<sub>CLZ</sub> DOUT VOL -

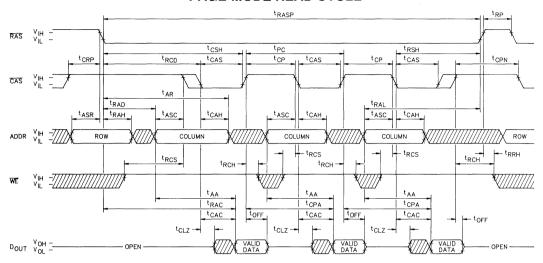
#### **EARLY-WRITE CYCLE**

VALID DATA

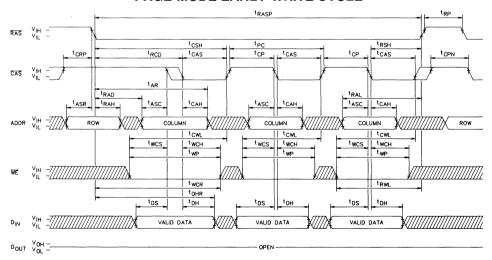
OPEN -



#### PAGE-MODE READ CYCLE



#### PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

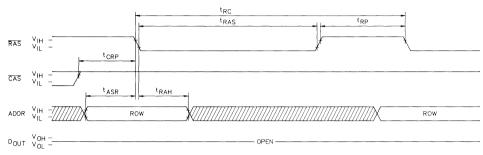


UNDEFINED



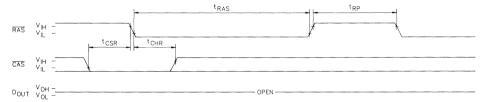
#### **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0 - A_8$ ;  $A_9$  and  $\overline{WE}$  = DON'T CARE.)



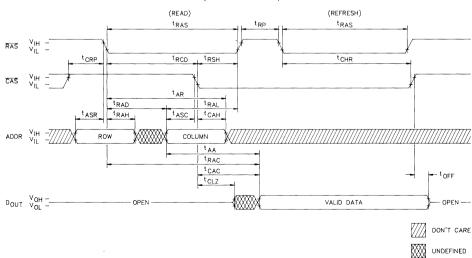
#### **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_0 \overline{WE}) = DON'T CARE.$ 



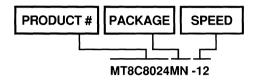
#### **HIDDEN REFRESH CYCLE**

 $(\overline{WE} = HIGH)$ 



#### ORDER INFORMATION

1 MEG x 8, 120ns access, Fast Page Mode Access, Leaded SIP



The Micron 1 MEG DRAM module family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance

CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AM-BYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

# DRAM MODULES

## 1MEG x 8 DRAM

NIBBLE MODE

#### **FEATURES**

- Industry standard pin-out in a 30-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 45mW standby, 1575mW active, typical.
- On-board power supply decoupling capacitors (0.2µf) for low noise.
- Refresh modes: RAS only, CAS before RAS, and Hidden.
- 512 cycle refresh distributed across 8ms.
- Optional Nibble access mode.

OPTIONS	MARKING
<ul> <li>Timing</li> </ul>	
100ns access	-10
120ns access	-12
150ns access	-15

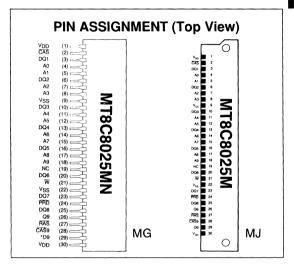
<ul> <li>Access Mode Option</li> </ul>	
Nibble Mode	MT8C8025

•	Packages: Leaded 30-pin SIP	MN
	Leadless 30-pin SIMM	M

A0-A9	Address Inputs	CAS, CAS9	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
PRD	Presence Detect	Q9	Data-Out
RAS	Row Address Strobe	$\overline{\mathbb{W}}$	Write Enable
VDD	Power (+5V)	Vss	Ground

#### **GENERAL DESCRIPTION**

The MT8C8025 M/MN is a randomly accessed solidstate memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time.  $\overline{RAS}$  is used to latch the first 10 bits and  $\overline{CAS}$  the latter 10 bits. A READ or WRITE cycle is selected with the  $\overline{WE}$  input. A logic high on  $\overline{WE}$ dictates READ mode while a logic low on  $\overline{WE}$  dictates



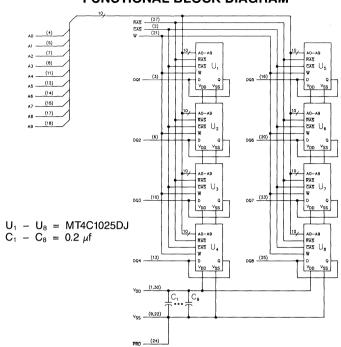
WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. If  $\overline{\text{WE}}$  goes low prior to  $\overline{\text{CAS}}$  going low, the output pin(s) remain open (High Z) until the next  $\overline{\text{CAS}}$  cycle. If  $\overline{\text{WE}}$  goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as  $\overline{\text{CAS}}$  remains low (regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ ). This late  $\overline{\text{WE}}$  pulse results in a READ-WRITE cycle.

Returning RAS and CAS high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS only, CAS-before-RAS, or Hidden refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

Nibble Mode operation allows faster sequential serial data operations (READ, WRITE or READ-MODIFY-WRITE) on up to 4 bits. The first of 4 bits is accessed in the usual manner with  $\overline{\text{CAS}}$  address A9 (nibble MSB) and  $\overline{\text{RAS}}$  address A9 (nibble LSB) selecting on of 4 bits within a nibble for initial access. By holding  $\overline{\text{RAS}}$  low,  $\overline{\text{CAS}}$  can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around (see below).



#### **FUNCTIONAL BLOCK DIAGRAM**



#### **FUNCTIONAL TRUTH TABLE**

					Addresses			
Function	RAS	CAS	WE	TF	tR	tC		NOTES
Standby	Н	Н	Н	GND/NC	Х	Х	High Impedance	
READ	L	L	Н	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
NIBBLE MODE READ	L	H→L→H	Н	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
NIBBLE MODE WRITE	L	H→L→H	L	GND/NC	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	GND/NC	Х	Х	High Impedance	
TEST FUNCTION	L	L	Н	Н	ROW	COL	Data Out, Test Funtion Mode	



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on VCC supply relative to Vss1.0V to +7.0V
Operating Temperature, TA(Ambient)0°C to +70°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation 8 Watt
Short Circuit Output Current50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc1		400	mA	3, 4
OPERATING CURRENT: NIBBLE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		400	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS  Power supply standby current (RAS = CAS = VIH  after 8 RAS cycles min.)	Іссз		16	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	ICC4		8	mA	
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = VIH)	lcc5		280	mA	3
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = Cycling)	Icce		280	mA	3, 5
INPUT LEAKAGE CURRENT (any input $(0V \le V_{IN} \le V_{CC})$ , all other pins not under test = 0 volts)	lı	-80	80	μА	
OUTPUT LEAKAGE CURRENT (Dour is disabled, 0V ≤ Vour ≤ Vcc)	loz	-80	80	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA)	Vон	2.4		V	1
Output Low voltage (lout = 5mA)	Vol	1	0.4	V	1

#### RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \le T_{A} \le 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1



#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9)	C <sub>11</sub>		40	pF	2
Input Capacitance RAS, CAS, WE	C12		56	pF	2
Output Capacitance Dout, Din	Co		12	pF	2

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq$ T $_A$ $\leq$ +70°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	190		220		260		ns	
Access time from RAS	<sup>t</sup> RAC		100		120		150	ns	14
Access time from CAS	<sup>t</sup> CAC		25		30		45	ns	15
Access time from column address	<sup>t</sup> AA		50		60		70	ns	
Access time from CAS precharge	<sup>t</sup> CPA		50		65		75	ns	
RAS pulse width	<sup>t</sup> RAS	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	<sup>t</sup> RSH	25		30		45		ns	
RAS precharge time	<sup>t</sup> RP	80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	25_	10,000	30	10,000	45	10,000	ns	
CAS hold time	<sup>t</sup> CSH	100		120		150		ns	
CAS precharge time	<sup>t</sup> CPN	15		20		25		ns	16
RAS to CAS delay time	<sup>t</sup> RCD	10	75	15	90	15	105	ns	17
CAS to RAS precharge time	<sup>t</sup> CRP	10		10		10		ns	
Row address set-up time	<sup>t</sup> ASR	0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	10		15		15		ns	
RAS to column	<sup>t</sup> RAD	10	50	15	60	15	70	ns	18
address delay time									
Column address set-up time	t <sub>ASC</sub>	0		0		0		ns	
Column address hold time	<sup>t</sup> CAH	15		20		25		ns	
Column address hold time (referenced to RAS)	<sup>t</sup> AR	60		70		80		ns	
Column address to RAS lead time	<sup>t</sup> RAL	50		60		70		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19
CAS to output in low-Z	t <sub>CLZ</sub>	5		5		5		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	25	0	25	0	30	ns	20
WE command set-up time	twcs	0		0		0		ns	
Write command hold time	tWCH	20		25		30		ns	
Write command hold time (referenced to RAS)	twcR	70		80		90		ns	



#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$  T<sub>A</sub>  $\leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS		-	10	-12		-	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command pulse width	<sup>t</sup> WP	20		25		30		ns	
Write command to RAS lead time	t <sub>RWL</sub>	25		30		35		ns	
Write command to CAS lead time	tCWL	25		30		35		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	21
Data-in hold time	t <sub>DH</sub>	15		20		25		ns	21
Data-in hold time (referenced to RAS)	<sup>t</sup> DHR	70		80		90		ns	
Column address to WE delay time	<sup>t</sup> AWD	50		60		70		ns	
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		8		8		8	ms	
RAS to CAS Precharge time	<sup>t</sup> RPC	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	t <sub>CSR</sub>	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	<sup>t</sup> CHR	20		25		30		ns	5
RAS pulse width (NIBBLE MODE)	t <sub>RASN</sub>	100	100,000	120	100,000	150	100,000	ns	
CAS precharge time (NIBBLE MODE)	<sup>t</sup> NCP	10		15		20		ns	
NIBBLE MODE cycle time	<sup>t</sup> NC	35		40		45		ns	
NIBBLE MODE access time	<sup>t</sup> NCAC	15		20		25		ns	15
NIBBLE MODE pulse width	<sup>t</sup> NCAS	15		20		25		ns	
NIBBLE MODE CAS precharge time	<sup>t</sup> NCP	10		10		10		ns	
NIBBLE MODE RAS hold time	<sup>t</sup> NRSH	15		20		25		ns	
NIBBLE MODE CAS to WRITE delay time	tNCMD	15		20		25		ns	
NIBBLE MODE WRITE command to RAS lead time	<sup>t</sup> NRWL	15		20		25		ns	
NIBBLE MODE WRITE command to CAS lead time	<sup>t</sup> NCWL	15		20		25		ns	

#### NOTES

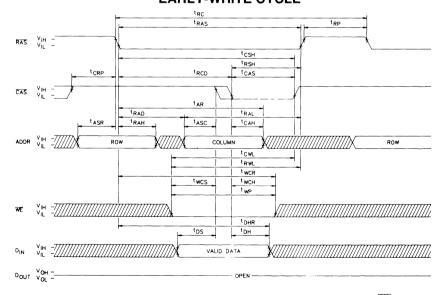
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and  $V_{CC} = 5V$ .
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- An initial pause of 100μs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- 9. Vih min and Vil max are reference levels for measuring timing of input signals. Transition times are measured between Vih and Vil (or between Vil and Vih).
- In addition to meeting the transition rate specification, all input signals must transit between Vih and Vil (or between Vil and Vih) in a monotonic manner.
- 11. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 12. If  $\overline{CAS} = Vit$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.

- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD \pmod{max}$ .
- 16. If CAS is low at the falling edge of RAS, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CPN.
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle.
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 21. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles.
- 22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{\text{WE}}$  = LOW.



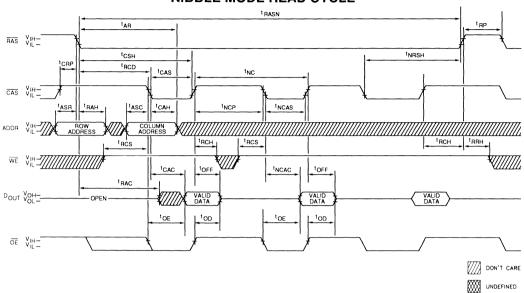
#### **READ CYCLE** tRAS RAS VIH t<sub>CSH</sub> tRSH t<sub>RRH</sub> tCAS t CRP t<sub>RCD</sub> tRAD t RAL tRAH t<sub>ASC</sub> t<sub>CAH</sub> t ASR COLUMN t<sub>RCH</sub> t<sub>RCS</sub> t<sub>AA</sub> TRAC tCAC t OFF t<sub>CLZ</sub> DOUT VOH -

#### **EARLY-WRITE CYCLE**





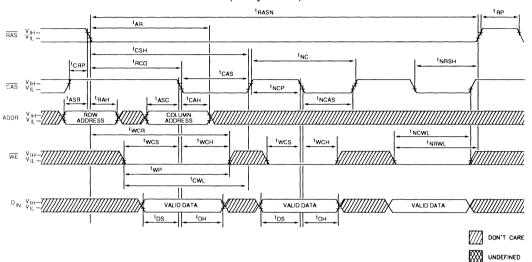
#### **NIBBLE MODE READ CYCLE**





#### **NIBBLE MODE WRITE CYCLE**

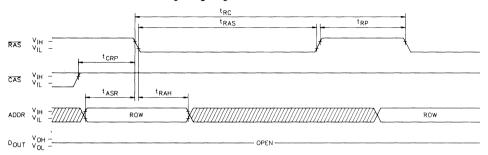
(Early Write)



## MICRON

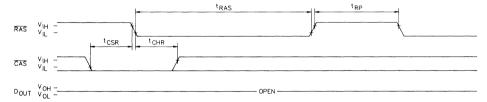
#### **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0$  -  $A_8$ ;  $A_9$  and  $\overline{WE}$  = DON'T CARE.)



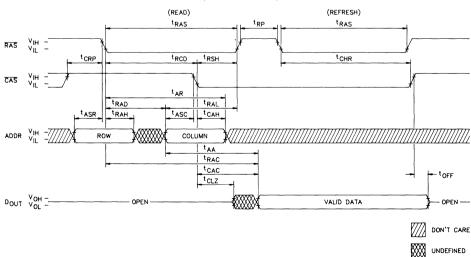
### **CAS-BEFORE-RAS** REFRESH CYCLE

 $(A_0 - A_9 \overline{WE}, = DON'T CARE.)$ 



#### **HIDDEN REFRESH CYCLE**

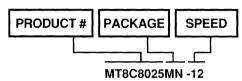
 $\overline{\text{WE}} = \text{HIGH}$ 





#### **ORDER INFORMATION**

1 MEG x 8, 120ns access, Nibble Mode Access, Leaded SIP



The Micron 1 MEG DRAM module family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance

CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AM-BYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

			50 disk to 2
	1 9		
			*

# DRAM MODULES

## 1MEG x 8 DRAM

STATIC COLUMN

#### **FEATURES**

- Industry standard pin-out in a 30-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 45mW standby, 1575mW active, typical.
- On-board power supply decoupling capacitors (0.2uf) for low noise.
- Refresh modes: RAS only, CAS before RAS, and Hidden.
- 512 cycle refresh distributed across 8ms.
- Optional Static Column access mode.

## OPTIONS MARKING • Timing 100ns access -10 120ns access 120ns access -12 150ns access • Access Mode Option

<ul> <li>Packages: Leaded 30-pin SIP</li> </ul>	MN
Leadless 30-pin SIMM	M

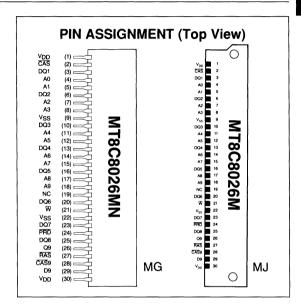
Static Column

A0-A9	Address Inputs	CAS, CAS9	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
PRD	Presence Detect	Q9	Data-Out
RAS	Row Address Strobe	W	Write Enable
VDD	Power (+5V)	Vss	Ground

MT8C8026

#### GENERAL DESCRIPTION

The MT8C8026 M/MN is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time.  $\overline{RAS}$  is used to latch the first 10 bits and  $\overline{CAS}$  the latter 10 bits. A READ or WRITE cycle is selected with the  $\overline{WE}$  input. A logic high on  $\overline{WE}$  dictates READ mode while a logic low on  $\overline{WE}$  dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of  $\overline{WE}$  or  $\overline{CAS}$ , whichever occurs



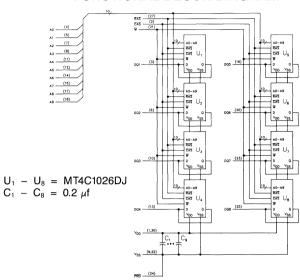
last. If  $\overline{\text{WE}}$  goes low prior to  $\overline{\text{CAS}}$  going low, the output pin(s) remain open (High Z) until the next  $\overline{\text{CAS}}$  cycle. If  $\overline{\text{WE}}$  goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as  $\overline{\text{CAS}}$  remains low (regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ ). This late  $\overline{\text{WE}}$  pulse results in a READ-WRITE cycle.

Returning RAS and CAS high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS only, CAS-before-RAS, or Hidden refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

STATIC COLUMN operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0 -A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed in by RAS followed by a column address strobed in by CAS. By holding RAS low, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning RAS high terminates the STATIC COLUMN operation.



#### **FUNCTIONAL BLOCK DIAGRAM**



#### **FUNCTIONAL TRUTH TABLE**

					Addresses			
Function	RAS	CAS	WE	TF	tR	tC		NOTES
Standby	Н	Н	Н	GND/NC	Х	Х	High Impedance	
READ	L	L	Н	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
STATIC COLUMN READ	L	L	Н	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
STATIC COLUMN WRITE	L	L	L	GND/NC	ROW	COL	Valid Data In, Valid Data Out	
RAS ONLY REFRESH	L	Н	Н	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	GND/NC	Х	Х	High Impedance	
TEST FUNCTION	L	L	Н	Н	ROW	COL	Data Out, Test Funtion Mode	



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V to +7.0V
Operating Temperature, TA(Ambient)0°C to +70°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation
Short Circuit Output Current 50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq$   $T_{\mbox{\scriptsize A}} \leq 70^{\circ} \mbox{\scriptsize C}$  = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: thc = thc(MIN))	lcc1		400	mA	3, 4
OPERATING CURRENT: STATIC COLUMN (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		400	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS  Power supply standby current (RAS = CAS = VIH  after 8 RAS cycles min.)	lcc3		16	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	Icc4		8	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY $(\overline{RAS} = \text{Cycling: } \overline{CAS} = \text{V}_{\text{IH}})$	lcc5		280	mA	3
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = Cycling)	lcc <sub>6</sub>		200	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ VIN ≤ Vcc), all other pins not under test = 0 volts)	lı	-80	80	μА	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ Vout ≤ Vcc)	loz	-80	80	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA)	Vон	2.4		V	1
Output Low voltage (lout = 5mA)	Vol		0.4	V	

#### RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{\Delta} \leq 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1



#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A <sub>0</sub> -A <sub>9</sub> )	Cl1		40	pF	2
Input Capacitance RAS, CAS, WE	C12		56	pF	2
Output Capacitance Dout, DIN	Co		12	pF	2

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq$ T $_A$ $\leq$ +70°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS			10		12		15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	190		220		260		ns	
Access time from RAS	t <sub>RAC</sub>		100		120		150	ns	14
Access time from CAS	t <sub>CAC</sub>		25		30		45	ns	15
Access time from column address	t <sub>AA</sub>		50		60		70	ns	
Access time from CAS precharge	tCPA		50		65		75	ns	
RAS pulse width	<sup>t</sup> RAS	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	<sup>t</sup> RSH	25		30		45		ns	
RAS precharge time	t <sub>RP</sub>	80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	25	10,000	30	10,000	45	10,000	ns	
CAS hold time	t <sub>CSH</sub>	100		120		150		ns	
CAS precharge time	t <sub>CPN</sub>	15		20		25		ns	16
RAS to CAS delay time	tRCD_	10	75	15	90	15	105	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		ns	
Row address hold time	t <sub>RAH</sub>	10_		15		15		ns	
RAS to column	<sup>t</sup> RAD	10	50	15	60	15	70	ns	18
address delay time									
Column address set-up time	t <sub>ASC</sub>	0		0		0		ns	
Column address hold time	tCAH	15		20		25		ns	
Column address hold time (referenced to RAS)	<sup>t</sup> AR	60		70		80		ns	
Column address to RAS lead time	<sup>t</sup> RAL	50		60		70		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19
CAS to output in low-Z	tCLZ	5		5		5		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	25	0	25	0	30	ns	20
WE command set-up time	twcs	0		0		0		ns	
Write command hold time	tWCH	20		25		30		ns	
Write command hold time (referenced to RAS)	tWCR	70		80		90		ns	



#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$   $T_{A}$   $\leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS		-	10	-	12		15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command pulse width	t <sub>WP</sub>	20		25		30		ns	
Write command to RAS lead time	t <sub>RWL</sub>	25		30		35		ns	
Write command to CAS lead time	tCWL	25		30		35		ns	
Data-in set-up time	<sup>t</sup> DS	0		0		00		ns	21
Data-in hold time	<sup>t</sup> DH	15		20		25		ns	21
Data-in hold time (referenced to RAS)	<sup>t</sup> DHR	70		80		90		ns	
Column address to WE delay time	<sup>t</sup> AWD	50		60		70		ns	
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	<sup>t</sup> REF		8		8		8	ms	
RAS to CAS Precharge time	<sup>t</sup> RPC	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	<sup>t</sup> CSR	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	t <sub>CHR</sub>	20		25		30		ns	5
RAS pulse width (STATIC COLUMN)	<sup>t</sup> RASC	100	100,000	120	100,000	150	100,000	ns	
CAS precharge time (STATIC COLUMN)	<sup>t</sup> CP	10		15		20		ns	
STATIC COLUMN MODE cycle time	tsc tsc	55		65		75		ns	
Last Write to column address delay time	<sup>t</sup> LWAD	25	45	30	55	45	70	ns	
Last Write to column address hold time	<sup>t</sup> AHLW		95		115		135	ns	
RAS hold time referenced to OE	<sup>t</sup> ROH	20		20		20		ns	
Output data hold time from column address	<sup>t</sup> AOH	5	_	5	_	5		ns	
Output data enable from Write	tOW		25	_	25	_	25	ns	

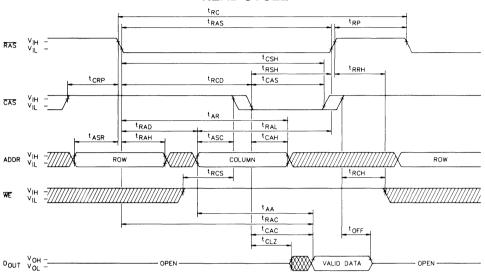
#### NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and VCC = 5V.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 12. If  $\overline{CAS} = V_{1L}$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.

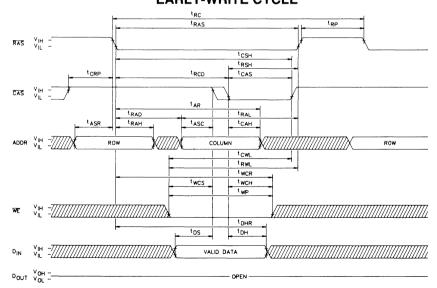
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If CAS is low at the falling edge of RAS, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CPN.
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- 19. Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle.
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 21. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles.
- 22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{WE}$  = LOW.



#### **READ CYCLE**

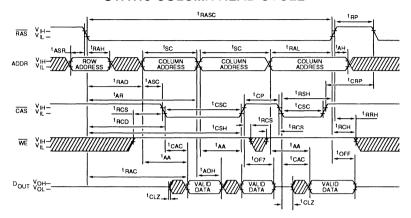


#### **EARLY-WRITE CYCLE**





#### STATIC COLUMN READ CYCLE

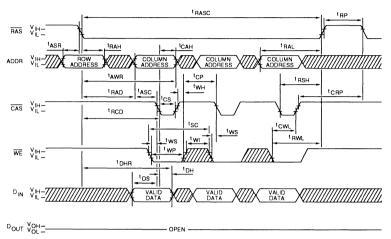


DON'T CARE

UNDEFINED



#### STATIC COLUMN EARLY-WRITE CYCLE

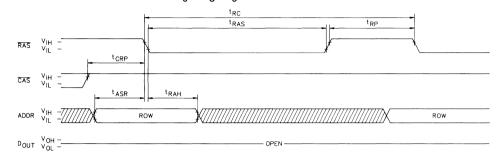


DON'T CARE

UNDEFINED

UNDEFINED

# $\overline{RAS}$ ONLY REFRESH CYCLE (ADDR = A<sub>0</sub> - A<sub>8</sub>; A<sub>9</sub> and $\overline{WE}$ = DON'T CARE.)



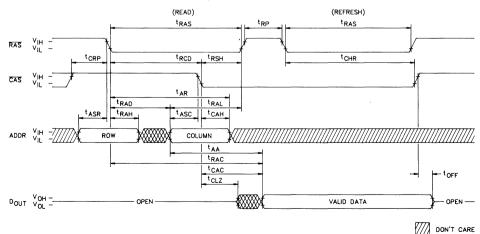
### CAS-BEFORE-RAS REFRESH CYCLE

 $(A_0 - A_9 \overline{WE}) = DON'T CARE.$ 



#### **HIDDEN REFRESH CYCLE**

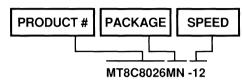
 $(\overline{WE} = HIGH)$ 





#### **ORDER INFORMATION**

1 MEG x 8, 120ns access, Static Column Access, Leaded SIP



The Micron 1 MEG DRAM module family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance

CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AM-BYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.



# DRAM MODULES

## 1MEG x 9 DRAM

**FAST PAGE MODE** 

#### **FEATURES**

- Industry standard pin-out in a 30-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 45mW standby, 1575mW active, typical.
- On-board power supply decoupling capacitors (0.2µf) for low noise.
- Refresh modes: RAS only, CAS before RAS, and Hidden.
- 512 cycle refresh distributed across 8ms.
- Optional Fast Page Mode.

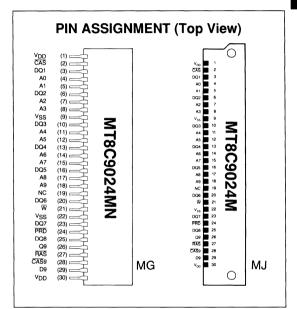
OPTIONS	MARKING
<ul> <li>Timing</li> </ul>	
100ns access	-10
120ns access	-12
150ns access	-15
<ul> <li>Organization</li> </ul>	
1 MEG x 9	MT8C9024

• Packages: Leadless 30-pin SIMM	M
Leadless 30-pim SIP	MN

A0-A9	Address Inputs	CAS, CAS9	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
PRD	Presence Detect	Q9	Data-Out
RAS	Row Address Strobe	W	Write Enable
VDD	Power (+5V)	Vss	Ground

#### GENERAL DESCRIPTION

The MT8C9024M/MN is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x8 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time.  $\overline{RAS}$  is used to latch the first 10 bits and  $\overline{CAS}$  the latter 10 bits. A READ or WRITE cycle is selected with the  $\overline{WE}$  input. A logic high on  $\overline{WE}$  dictates READ mode while a logic low on  $\overline{WE}$  dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of  $\overline{WE}$  or  $\overline{CAS}$ , whichever occurs

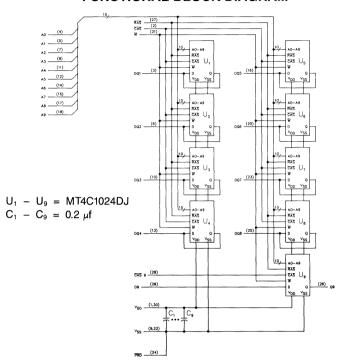


last. If  $\overline{\text{WE}}$  goes low prior to  $\overline{\text{CAS}}$  going low, the output pin(s) remain open (High Z) until the next  $\overline{\text{CAS}}$  cycle. If  $\overline{\text{WE}}$  goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as  $\overline{\text{CAS}}$  remains low (regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ ). This late  $\overline{\text{WE}}$  pulse results in a READ-WRITE cycle.

Returning RAS and CAS high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS only, CAS-before-RAS, or Hidden refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by RAS followed by a column address strobed in by CAS. By holding RAS low, CAS may be toggled strobing in different column addresses executing faster memory cycles. Returning RAS high terminates the PAGE MODE operation.

#### **FUNCTIONAL BLOCK DIAGRAM**



#### **FUNCTIONAL TRUTH TABLE**

				Addr	esses		
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	х	High Impedance	



#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$  T<sub>A</sub>  $\leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS			10	-	12	-	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time (referenced to RAS)	tWCR	70		80		90		ns	
Write command pulse width	<sup>t</sup> WP	20		25		30		ns	
Write command to RAS lead time	t <sub>RWL</sub>	25		30		35		ns	
Write command to CAS lead time	tCWL	25		30		35		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	22
Data-in hold time	t <sub>DH</sub>	15		20		25		ns	22
Data-in hold time (referenced to RAS)	<sup>t</sup> DHR	70		80		90		ns	
RAS to WE delay time	t <sub>RWD</sub>	90		110		135		ns	21
Column address to WE delay time	<sup>t</sup> AWD	50		60		70		ns	21
CAS to WE delay time	tCWD	35		40		45		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		8		8		8	ms	
RAS to CAS Precharge time	t <sub>RPC</sub>	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	t <sub>CSR</sub>	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	tCHR	20		25		30		ns	5

#### NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and  $V_{CC} = 5V$ .
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between Vih and Vil (or between Vil and Vih) in a monotonic manner.
- 11. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 12. If  $\overline{\text{CAS}} = \text{Vil.}$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If  $\overline{CAS}$  is low at the falling edge of  $\overline{RAS}$ , Dout will

- be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for  ${}^{\text{t}}\text{CPN}$ .
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle.
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to Voh ot Vol.
- 21. <sup>t</sup>WCS, <sup>t</sup>RWD, <sup>t</sup>AWD and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), <sup>t</sup>AWD ≥ <sup>t</sup>AWD (min) and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to Vih) is indeterminate.
- 22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles and  $\overline{\text{WE}}$  leading edge in late WRITE or READ-WRITE cycles.
- A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case WE = LOW.

#### ABSOLUTE MAXIMUM RATINGS\*

Voltage on VCC supply relative to Vss ....... $^{-1.0V}$  to  $^{+7.0V}$  Operating Temperature, Ta(Ambient) ...... $^{0}$ °C to  $^{+70}$ °C Storage Temperature (Plastic) ..... $^{-55}$ °C to  $^{+150}$ °C Power Dissipation ...... $^{9}$  Watt Short Circuit Output Current ..... $^{50}$ mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq$  T  $_{\Delta} \leq$  70°C = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	Icc1		450	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		450	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = VIH after 8 RAS cycles min.)	lcc3		18	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current (RAS = CAS = Vcc -0.2V after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	Icc4		9	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY $(\overline{RAS} = \text{Cycling: } \overline{CAS} = \text{V}_{\text{IH}})$	lcc5		315	mA	3
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = Cycling)	Icc6		315	mA	3, 5
INPUT LEAKAGE CURRENT (any input $(0V \le V_{IN} \le V_{CC})$ , all other pins not under test = 0 volts)	11	<sub>.</sub> -90	90	μА	
OUTPUT LEAKAGE CURRENT (Doυτ is disabled, 0V ≤ Voυτ ≤ Vcc)	loz	-90	90	μА	
OUTPUT LEVELS Output High voltage (Iout = -5mA)	Vон	2.4		V	1
Output Low voltage (lout = 5mA)	Vol		0.4	V	

#### RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{\Delta} \leq 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1



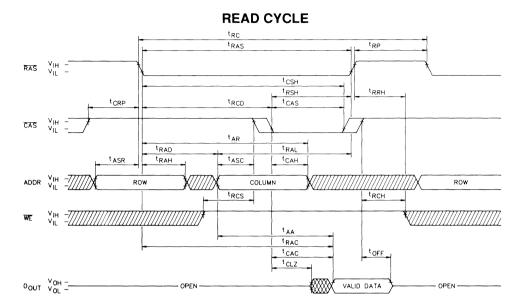
#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9)	CI1		45	pF	2
Input Capacitance RAS, CAS, WE	CI2		63	pF	2
Output Capacitance Dout, Din	Co		12	pF	2

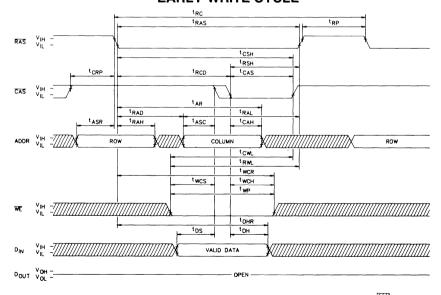
# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq$ T<sub>A</sub> $\leq$ +70°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS		-	10	-	12	-	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	190		220		260		ns	
PAGE-MODE READ or WRITE	t <sub>PC</sub>	55		70		85		ns	
cycle time									
Access time from RAS	t <sub>RAC</sub>		100		120		150	ns	14
Access time from CAS	t <sub>CAC</sub>		25		30		45	ns	15
Access time from column address	<sup>t</sup> AA		50		60		70	ns	
Access time from CAS precharge	t <sub>CPA</sub>		50		65		75	ns	
RAS pulse width	t <sub>RAS</sub>	100	10,000	120	10,000	150	10,000	ns	
RAS pulse width (PAGE MODE)	t <sub>RASP</sub>	100	100,000	120	100,000	150	100,000	ns	
RAS hold time	t <sub>RSH</sub>	25		30		45		ns	
RAS precharge time	t <sub>RP</sub>	80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	25	10,000	30	10,000	45	10,000	ns	
CAS hold time	tCSH	100		120		150		ns	
CAS precharge time	tCPN	15		20		25		ns	16
CAS precharge time (PAGE MODE)	<sup>t</sup> CP	10		15		20		ns	
RAS to CAS delay time	t <sub>RCD</sub>	10	75	15	90	15	105	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address set-up time	tasr.	0		0		0		ns	
Row address hold time	t <sub>RAH</sub>	10		15		15		ns	
RAS to column	t <sub>RAD</sub>	10	50	15	60	15	70	ns	18
address delay time									
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		20		25		ns	
Column address hold time	t <sub>AR</sub>	60		70		80		ns	
(referenced to RAS)									
Column address to	t <sub>RAL</sub>	50		60		70		ns	
RAS lead time									
Read command set-up time	t <sub>RCS</sub>	0		0		0		ns	
Read command hold time	t <sub>RCH</sub>	0		0		0		ns	19
(referenced to CAS)									
Read command hold time	t <sub>RRH</sub>	0		0		0		ns	19
(referenced to RAS)									
CAS to output in low-Z	tCLZ	5		5		5		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	25	0	25	0	30	ns	20
WE command set-up time	twcs	0		0		0		ns	21
Write command hold time	tWCH	20		25		30		ns	

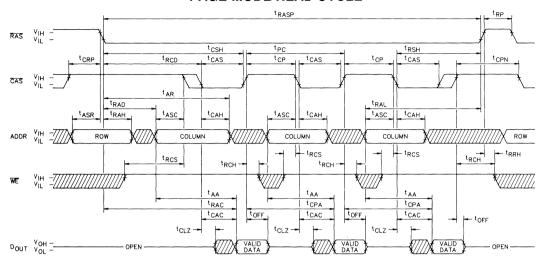




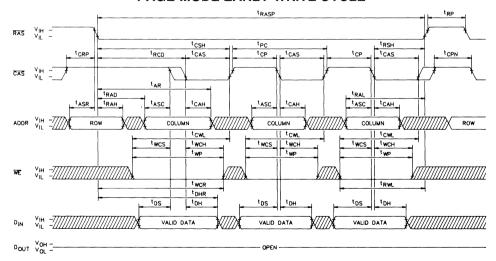
#### **EARLY-WRITE CYCLE**



#### PAGE-MODE READ CYCLE



#### PAGE-MODE EARLY-WRITE CYCLE



DOV

DON'T CARE

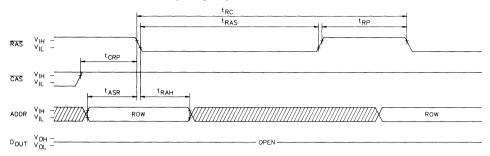


UNDEFINED



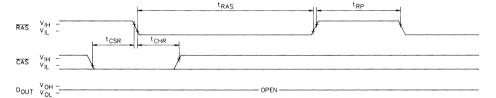
#### RAS ONLY REFRESH CYCLE

(ADDR =  $A_0 - A_8$ ;  $A_9$  and  $\overline{WE} = DON'T CARE.)$ 



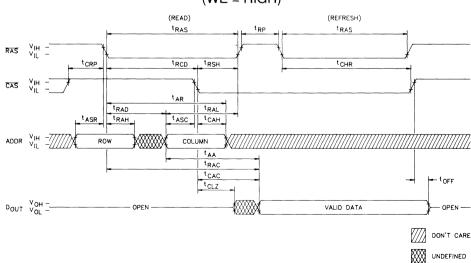
#### **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_9 \overline{WE}, \overline{OE} = DON'T CARE.)$ 



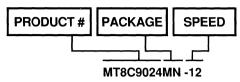
#### **HIDDEN REFRESH CYCLE**

 $(\overline{WE} = HIGH)$ 



#### ORDER INFORMATION

1 MEG x 9, 120ns access, Fast Page Mode Access, Leaded SIP



The Micron 1 MEG DRAM module family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance

CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AM-BYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

# DRAM MODULES

## 1MEG x 9 DRAM

NIBBLE MODE

#### **FEATURES**

- Industry standard pin-out in a 30-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 45mW standby, 1575mW active, typical.
- On-board power supply decoupling capacitors (0.2uf) for low noise.
- Refresh modes: RAS only, CAS before RAS, and Hidden
- 512 cycle refresh distributed across 8ms.
- Optional Nibble access mode.

# OPTIONS MARKING • Timing 100ns access 120ns access 150ns access -15

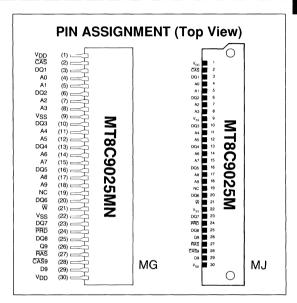
• Access Mode Option Nibble Mode MT8C9025

 Packages: Leaded 30-pin SIP MN Leadless 30-pin SIMM N

A0-A9	Address Inputs	CAS, CAS9	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
PRD	Presence Detect	Q9	Data-Out
RAS	Row Address Strobe	W	Write Enable
VDD	Power (+5V)	Vss	Ground

#### **GENERAL DESCRIPTION**

The MT8C9025 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time.  $\overline{RAS}$  is used to latch the first 10 bits and  $\overline{CAS}$  the latter 10 bits. A READ or WRITE cycle is selected with the  $\overline{WE}$  input. A logic high on  $\overline{WE}$  dictates READ mode while a logic low on  $\overline{WE}$  dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of  $\overline{WE}$  or  $\overline{CAS}$ , whichever occurs



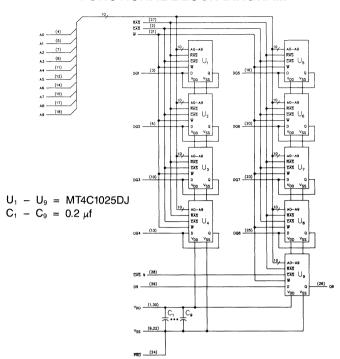
last. If  $\overline{\text{WE}}$  goes low prior to  $\overline{\text{CAS}}$  going low, the output pin(s) remain open (High Z) until the next  $\overline{\text{CAS}}$  cycle. If  $\overline{\text{WE}}$  goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as  $\overline{\text{CAS}}$  remains low (regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ ). This late  $\overline{\text{WE}}$  pulse results in a READ-WRITE cycle.

Returning RAS and CAS high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS only, CAS-before-RAS, or Hidden refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

Nibble Mode operation allows faster sequential serial data operations (READ, WRITE or READ-MODIFY-WRITE) on up to 4 bits. The first of 4 bits is accessed in the usual manner with  $\overline{\text{CAS}}$  address A9 (nibble MSB) and  $\overline{\text{RAS}}$  address A9 (nibble LSB) selecting on of 4 bits within a nibble for initial access. By holding  $\overline{\text{RAS}}$  low,  $\overline{\text{CAS}}$  can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around (see below).



#### **FUNCTIONAL BLOCK DIAGRAM**



#### **FUNCTIONAL TRUTH TABLE**

	546	-	WE	Addr	esses		NOTES.
Function	RAS	CAS	WE	WE tR tC			NOTES
Standby	Н	Н	Н	Х	X	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
NIBBLE MODE READ	L	H→L→H, H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
NIBBLE MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V to +	-7.0V
Operating Temperature, TA(Ambient)0°C to +	70°C
Storage Temperature (Plastic)55°C to +1	50°C
Power Dissipation9	Watt
Short Circuit Output Current5	0mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq$  T  $_{A} \leq$  70°C = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc1		450	mA	3, 4
OPERATING CURRENT: NIBBLE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		450	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS  Power supply standby current (RAS = CAS = VIH  after 8 RAS cycles min.)	lcc3		18	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	Icc4		9	mA	
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih)	lcc5		315	mA	3
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = Cycling)	Icce		315	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> ), all other pins not under test = 0 volts)	lı .	-90	90	μА	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ Vout ≤ Vcc)	loz	-90	90	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA)	Vон	2.4	0.4	V	1
Output Low voltage (Iout = 5mA)	Vol		0.4	\ \	

#### RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{{\color{blue}A}} \leq 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1

#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A <sub>0</sub> -A <sub>9</sub> )	CI1		45	pF	2
Input Capacitance RAS, CAS, WE	CI2		63	pF	2
Output Capacitance Dout, DIN	Co		12	pF	2

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq$ T\_A $\leq$ +70°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS		-	10	-	12	-	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	190		220		260		ns	
Access time from RAS	t <sub>RAC</sub>		100		120		150	ns	14
Access time from CAS	t <sub>CAC</sub>		25		30		45	ns	15
Access time from column address	<sup>t</sup> AA		50		60		70	ns	
Access time from CAS precharge	tCPA		50		65		75	ns	
RAS pulse width	tRAS	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	<sup>t</sup> RSH	25		30		45		ns	
RAS precharge time	t <sub>RP</sub>	80		90		100		ns	
CAS pulse width	tCAS	25	10,000	30	10,000	45	10,000	ns	
CAS hold time	t <sub>CSH</sub>	100		120		150		ns	
CAS precharge time	t <sub>CPN</sub>	15		20		25		ns	16
RAS to CAS delay time	t <sub>RCD</sub>	10	75	15	90	15	105	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address set-up time	<sup>t</sup> ASR	0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	10		15		15		ns	
RAS to column	<sup>t</sup> RAD	10	50	15	60	15	70	ns	18
address delay time									
Column address set-up time	t <sub>ASC</sub>	0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		20		25		ns	
Column address hold time (referenced to RAS)	<sup>t</sup> AR	60		70		80		ns	
Column address to RAS lead time	<sup>t</sup> RAL	50		60		70		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19
CAS to output in low-Z	t <sub>CLZ</sub>	5		5		5		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	25	0	25	0	30	ns	20
WE command set-up time	twcs	0		0		0		ns	
Write command hold time	tWCH	20		25		30		ns	
Write command hold time (referenced to RAS)	tWCR	70		80		90		ns	



#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$  T<sub>A</sub>  $\leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS	-10		-12		-15				
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command pulse width	<sup>t</sup> WP	20		25		30		ns	
Write command to RAS lead time	t <sub>RWL</sub>	25		30		35		ns	
Write command to CAS lead time	tCWL	25		30		35		ns	
Data-in set-up time	<sup>t</sup> DS	0		0		0		ns	21
Data-in hold time	tDH	15		20		25		ns	21
Data-in hold time (referenced to RAS)	<sup>t</sup> DHR	70		80		90		ns	
Column address to WE delay time	<sup>t</sup> AWD	50		60		70		ns	
Transition time (rise or fall)	<sup>t</sup> T	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	<sup>t</sup> REF		8		8		8	ms	
RAS to CAS Precharge time	t <sub>RPC</sub>	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	<sup>t</sup> CSR	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	<sup>t</sup> CHR	20		25		30		ns	5
RAS pulse width (NIBBLE MODE)	<sup>t</sup> RASN	100	100,000	120	100,000	150	100,000	ns	
CAS precharge time (NIBBLE MODE)	<sup>t</sup> NCP	10		15		20		ns	
NIBBLE MODE cycle time	<sup>t</sup> NC	35		40		45		ns	
NIBBLE MODE access time	<sup>t</sup> NCAC	15		20		25		ns	15
NIBBLE MODE pulse width	t <sub>NCAS</sub>	15		20		25		ns	
NIBBLE MODE CAS precharge time	<sup>t</sup> NCP	10		10		10		ns	
NIBBLE MODE RAS hold time	<sup>t</sup> NRSH	15		20		25		ns	
NIBBLE MODE CAS to WRITE delay time	tNCWD	15		20		25		ns	
NIBBLE MODE WRITE command to RAS lead time	<sup>t</sup> NRWL	15		20		25		ns	
NIBBLE MODE WRITE command to CAS lead time	tNCWL	15		20		25		ns	

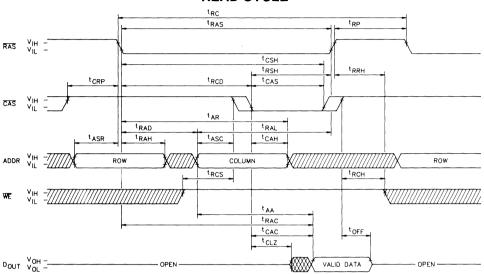
#### NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and VCC = 5V
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- An initial pause of 100μs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VII. and VIH) in a monotonic manner.
- 11. If  $\overline{CAS} = VIH$ , data output is high impedance.
- 12. If  $\overline{\text{CAS}} = \text{VIL}$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.

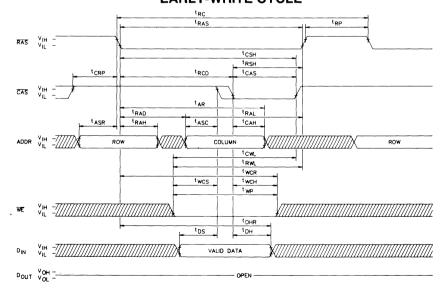
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If CAS is low at the falling edge of RAS, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CPN.
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- 19. Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle.
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 21. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles.
- 22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{WE} = LOW$ .



#### **READ CYCLE**



#### **EARLY-WRITE CYCLE**







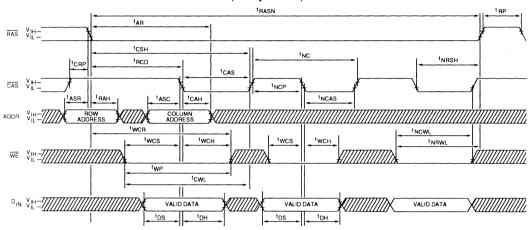
DON'T CARE
UNDEFINED

#### **NIBBLE MODE READ CYCLE** <sup>t</sup> RASN 1AR t RP RAS VIHt<sub>CSH</sub> INRSH CRP <sup>t</sup>RCD †CAS CAS VIH-<sup>t</sup>CAH <sup>1</sup>NCAS trich trich ¹RCH I 1<sub>RCS</sub> IRCS V////// 1CAC tOFF INCAC tOFF DOUT VOH-VALID DATA VALID <sup>t</sup>OE toD <sup>t</sup>OE top OE VIH-



#### **NIBBLE MODE WRITE CYCLE**

(Early Write)



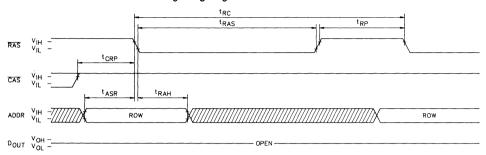
DON'T CARE

UNDEFINED



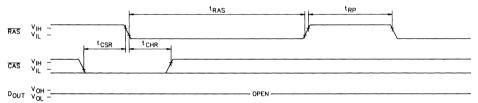
#### **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0 - A_8$ ;  $A_9$  and  $\overline{WE}$  = DON'T CARE.)



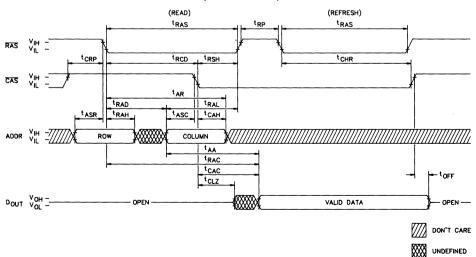
## CAS-BEFORE-RAS REFRESH CYCLE

 $(A_0 - A_9 \overline{WE}, = DON'T CARE.)$ 



#### **HIDDEN REFRESH CYCLE**

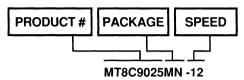
 $(\overline{WE} = HIGH)$ 





#### ORDER INFORMATION

1 MEG  $\times$  9, 120ns access, Nibble Mode Access, Leaded SIP



The Micron 1 MEG DRAM module family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance

CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AM-BYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. .

# DRAM MODULES

## 1MEG x 9 DRAM

STATIC COLUMN

#### **FEATURES**

- Industry standard pin-out in a 30-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 45mW standby, 1575mW active, typical.
- On-board power supply decoupling capacitors (0.2μf) for low noise.
- Refresh modes: RAS only, CAS before RAS, and Hidden.
- 512 cycle refresh distributed across 8ms.
- Optional Static Column access mode.

## OPTIONS

#### MARKING

0	********
<ul><li>Timing</li></ul>	
100ns access	-10
120ns access	-12
150ns access	-15

 Access Mode Option Static Column

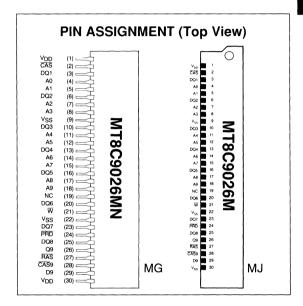
MT8C9026

<ul> <li>Packages: Leaded 30-pin SIP</li> </ul>	MN
Leadless 30-pin SIMM	M

A0-A9	Address Inputs	CAS, CAS9	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
PRD	Presence Detect	Q9	Data-Out
RAS	Row Address Strobe	$\overline{\mathbb{W}}$	Write Enable
VDD	Power (+5V)	Vss	Ground

#### **GENERAL DESCRIPTION**

The MT8C9026M/MN is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic high on WE dictates READ mode while a logic low on WE dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of WE or CAS, whichever occurs

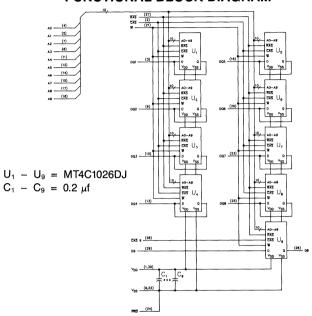


last. If  $\overline{\text{WE}}$  goes low prior to  $\overline{\text{CAS}}$  going low, the output pin(s) remain open (High Z) until the next  $\overline{\text{CAS}}$  cycle. If  $\overline{\text{WE}}$  goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as  $\overline{\text{CAS}}$  remains low (regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ ). This late  $\overline{\text{WE}}$  pulse results in a READ-WRITE cycle.

Returning RAS and CAS high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS only, CAS-before-RAS, or Hidden refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

STATIC COLUMN operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed in by RAS followed by a column address strobed in by CAS. By holding RAS low, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning RAS high terminates the STATIC COLUMN operation.

#### **FUNCTIONAL BLOCK DIAGRAM**



#### **FUNCTIONAL TRUTH TABLE**

					Addresses			
Function	RAS	CAS	WE	TF	tR	tC		NOTES
Standby	Н	н	Н	GND/NC	Х	Х	High Impedance	
READ	L	L	Н	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
STATIC COLUMN READ	L	H→L→H	Н	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
STATIC COLUMN WRITE	L	H→L→H	L	GND/NC	ROW	COL	Valid Data In, Valid Data Out	
RAS ONLY REFRESH	L	н	Н	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	GND/NC	Х	×	High Impedance	
TEST FUNCTION	L	L	Н	Н	ROW	COL	Data Out, Test Funtion Mode	



#### ABSOLUTE MAXIMUM RATINGS\*

Voltage on VCC supply relative to Vss	1.0V to +7.0V
Operating Temperature, TA(Ambient)	0°C to +70°C
Storage Temperature (Plastic)	-55°C to +150°C
Power Dissipation	9 Watt
Short Circuit Output Current	50m A

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C  $\leq$  T $_{\Delta} \leq$  70°C = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc1		450	mA	3, 4
OPERATING CURRENT: STATIC COLUMN (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		450	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ( $\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles min.)	lcc3		18	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ( $\overline{RAS} = \overline{CAS} = Vcc -0.2V$ after 8 $\overline{RAS}$ cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	Icc4		9	mA	
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih)	lcc5		315	mA	3
REFRESH CURRENT: CAS-before-RAS (RAS and CAS = Cycling)	Icc6		315	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V $\leq$ Vin $\leq$ Vcc), all other pins not under test = 0 volts)	lı	-90	90	μА	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ Vout ≤ Vcc)	loz	-90	90	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA)	Vон	2.4		V	1
Output Low voltage (lout = 5mA)	Vol	1	0.4	V	

#### RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \le T_{A} \le 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1



#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A <sub>0</sub> -A <sub>9</sub> )	CI1		45	pF	2
Input Capacitance RAS, CAS, WE	Cl2		63	pF	2
Output Capacitance Dout, Din	Co		12	pF	2

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq$ T $_A$ $\leq$ +70°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	190		220		260		ns	
Access time from RAS	<sup>t</sup> RAC		100		120		150	ns	14
Access time from CAS	t <sub>CAC</sub>		25		30		45	ns	15
Access time from column address	<sup>t</sup> AA		50		60		70	ns	
Access time from CAS precharge	t <sub>CPA</sub>		50		65		75	ns	
RAS pulse width	tRAS	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	t <sub>RSH</sub>	25		30		45		ns	
RAS precharge time	t <sub>RP</sub>	80	}	90		100		ns	
CAS pulse width	t <sub>CAS</sub>	25	10,000	30	10,000	45	10,000	ns	
CAS hold time	<sup>t</sup> CSH	100		120		150		ns	
CAS precharge time	t <sub>CPN</sub>	15		20		25		ns	16
RAS to CAS delay time	t <sub>RCD</sub>	10	75	15	90	15	105	ns	17
CAS to RAS precharge time	t <sub>CRP</sub>	10		10		10		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		ns	
Row address hold time	t <sub>RAH</sub>	10		15		15		ns	
RAS to column	<sup>t</sup> RAD	10	50	15	60	15	70	ns	18
address delay time									
Column address set-up time	t <sub>ASC</sub>	0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		20		25		ns	
Column address hold time (referenced to RAS)	<sup>t</sup> AR	60		70		80		ns	
Column address to RAS lead time	<sup>t</sup> RAL	50		60		70		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19
CAS to output in low-Z	t <sub>CLZ</sub>	5		5		5		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	25	0	25	0	30	ns	20
WE command set-up time	twcs	0		0		0		ns	
Write command hold time	twcH	20		25		30		ns	
Write command hold time (referenced to RAS)	twcr	70		80		90		ns	



#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$  T<sub>A</sub>  $\leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS	-10		-12		-15				
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command pulse width	t <sub>WP</sub>	20		25		30		ns	
Write command to RAS lead time	t <sub>RWL</sub>	25		30		35		ns	
Write command to CAS lead time	tCWL	25		30		35		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	21
Data-in hold time	t <sub>DH</sub>	15		20		25		ns	21
Data-in hold time (referenced to RAS)	<sup>t</sup> DHR	70		80		90		ns	
Column address to WE delay time	<sup>t</sup> AWD	50		60		70		ns	
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	<sup>t</sup> REF		8		8		8	ms	
RAS to CAS Precharge time	<sup>t</sup> RPC	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	<sup>t</sup> CSR	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	<sup>t</sup> CHR	20		25		30		ns	5
RAS pulse width (STATIC COLUMN)	tRASC	100	100,000	120	100,000	150	100,000	ns	
CAS precharge time (STATIC COLUMN)	<sup>t</sup> CP	10		15		20		ns	
STATIC COLUMN MODE cycle time	<sup>t</sup> SC	55		65		75		ns	
Last Write to column address delay time	<sup>t</sup> LWAD	25	45	30	55	45	70	ns	
Last Write to column address hold time	<sup>t</sup> AHLW		95		115		135	ns	
RAS hold time referenced to OE	<sup>t</sup> ROH	20		20		20		ns	
Output data hold time from column address	<sup>t</sup> AOH	5	_	5	_	5	_	ns	
Output data enable from Write	t <sub>OW</sub>	_	25	_	25		25	ns	

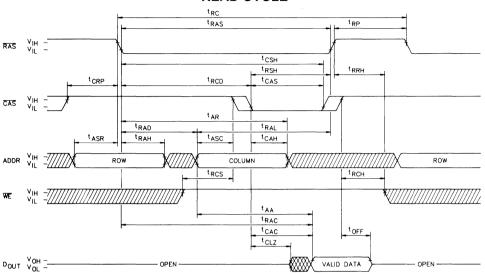
#### **NOTES**

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and  $V_{CC} = 5V$ .
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading. Specified values are obtained the output open.
- Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between Vih and Vil (or between Vil and Vih) in a monotonic manner.
- 11. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 12. If  $\overline{\text{CAS}} = \text{Vil}$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.

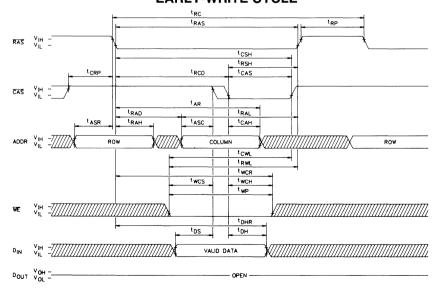
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If CAS is low at the falling edge of RAS, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for <sup>t</sup>CPN.
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle.
- 20. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 21. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles.
- 22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{WE} = LOW$ .



#### READ CYCLE

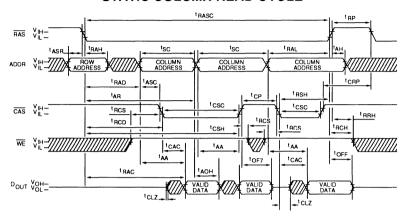


#### **EARLY-WRITE CYCLE**





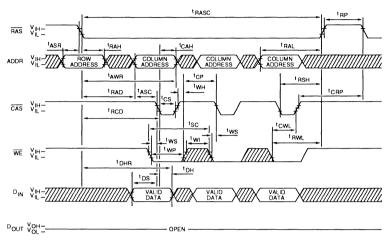
#### STATIC COLUMN READ CYCLE



DON'T CARE



### STATIC COLUMN EARLY-WRITE CYCLE

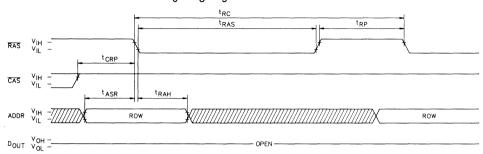


DON'T CARE



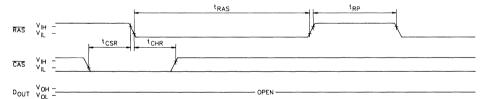
#### **RAS ONLY REFRESH CYCLE**

(ADDR =  $A_0 - A_8$ ;  $A_9$  and  $\overline{WE} = DON'T CARE.)$ 



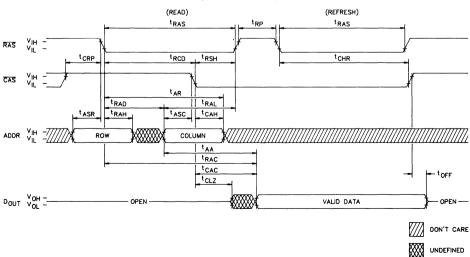
### **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_9 \overline{WE}, = DON'T CARE.)$ 



#### **HIDDEN REFRESH CYCLE**

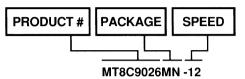
 $(\overline{WE} = HIGH)$ 





#### ORDER INFORMATION

1 MEG x 9, 120ns access, Static Column Access, Leaded SIP



The Micron 1 MEG DRAM module family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance

CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AM-BYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. . . . . . .

DYNAMIC RAMS	1
DYNAMIC RAM MODULES	2
MULTIPORT DYNAMIC RAMs (VRAMs)	3
STATIC RAMS	4
CACHE DATA RAMS	5
FIFO MEMORIES	6
MILITARY PRODUCTS	7
PACKAGE INFORMATION	. 8
SALES INFORMATION	9

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#### **VRAM PRODUCT SELECTION GUIDE**

Memory	Access	Part	Access	Power D	issipation		Package & Ni	ımber of Pin	S		
Configuration	Cycle	Number	Time (ns)	Standby	Active	PDIP	ZIP	SOJ	CDIP	Process	Page
64K x 4	Page Mode	MT42C4064	100,120,150	10mw	150mw	24	24	24	24	CMOS	3-3
256K x 4	Fast Page Mode	MT42C4256	80,100,120,150	20mw	300mw	28	28	28	28	CMOS	3-29

#### **FOOTNOTES:**

All devices require +5 Volt ± 10% power supply.

24-Pin ZIP

2 DQ4

6 Vss

8 SDQ1

= 10 TR / OE

==12 DQ2

== 14 RAS

SDQ3

DQ3

SDQ4

SDQ2 9

SE 3

SC

DQ1 11 ==

A6 15 ==

ME/WE 13 ==

# VRAM

# 64K x 4 DRAM with 256 x 4 SAM

PIN ASSIGNMENT (Top View)

24 NVss

23 | SDQ4

22 | SDQ3

21 | SE

20 DQ4

19Проз

18 CAS

17 TAO

24-Pin DIP

sc II1

SDQ1112

SDQ2 / 3

DQ1 15

DQ2 [6

RAS [18

ME/WE [] 7

TR/OE | 4

#### **FEATURES**

- · Industry standard pin-out, timing, and functions
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS, and HIDDEN
- 256 cycle refresh within 4ms
- Optional PAGE MODE access cycles
- Dual port organization: 64K x 4 DRAM port 256 x 4 SAM port
- Bit MASK-WRITE mode capability on DRAM port
- No refresh required for Serial Access Memory

OPTIONS • Timing (DRAM, SAM)	MARKING
100ns, 40ns	-10
120ns, 40ns	-12
150ns, 60ns	-15
• Packages	
Plastic DIP (400 mil)	None
Ceramic DIP (400 mil)	C
Plastic ZIP	Z
Plastic SOJ (300 mil)	DJ

#### ==116 A5 **А6**П9 16 A1 A4 17 E3 • Low power: 10mW standby, 150mW active, typical ⊏=18 Vcc A5[10 15 TA2 A7 19 == • Fast access times – 100ns parallel, 40ns serial == 20 A3 A4 11 14 | A3 A2 21== == 22 A1 Vcc [ 12 13 🛮 A7 A0 23 == G == 24 CAS PH, CG ZC 24-Pin SOJ 24 D Vss 23 D SDQ4 22 D SDQ3 21 D SE SC [1 • SDQ1 [2 SDQ2 C 3 DQ1 0 5 DQ2 0 6 ME/WE 0 7 RAS 0 8 20 0004 19 D DQ3 18 D CAS 17 D A0 15 b A2 13 E DJB

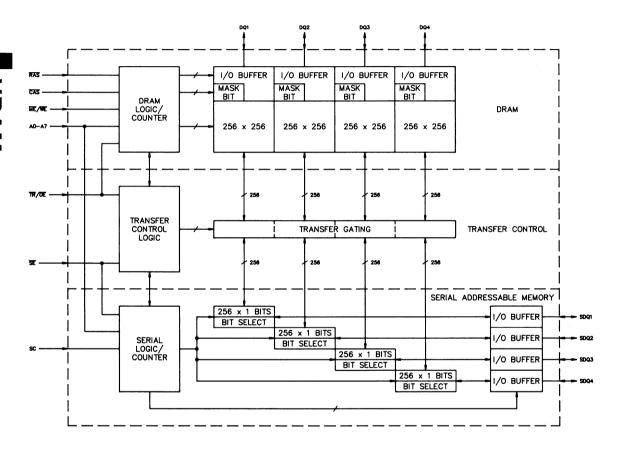
#### GENERAL DESCRIPTION

The MT42C4064 is a high speed, dual port CMOS dynamic random access memory (DPDRAM) containing 262,144 bits. They can be accessed either by a four bit wide DRAM port or by a 256 x 4 bit serial access memory (SAM) port. Data can be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the DPDRAM is functionally identical to the MT4067 64K x 4 bit DRAM. Four 256 bit data registers make up the serial access memory portion of the DPDRAM. Data I/O and internal data transfer is accomplished using three separate bidirectional data paths; the four bit random access I/O port, the four internal 256 bit wide paths between the DRAM and the SAM, and the four bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs the DPDRAM must be refreshed in order to maintain data. The refresh cycles must be timed so that all 256 combinations of RAS addresses are executed at least every 4ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the DPDRAM is fully static and does not require any refresh.

# Figure 1 MT42C4064 BLOCK DIAGRAM





### **PIN DESCRIPTIONS**

PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
1	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
2, 3, 22, 23	SDQ1 - SDQ4	Input/ Output	Serial Data I/O: Input, Output, or high impedance.
4	TR/OE	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{\text{RAS}}$ (H $\rightarrow$ L), or
			Output Enable: Enables the DRAM output buffers when taken LOW after RAS goes LOW (CAS must also be LOW), otherwise the output buffers are in a high impedance state.
5, 6, 19, 20	DQ1 - DQ4	Input/ Output	DRAM Data I/O: Inputs, Outputs, or high impedance, and/or Mask Data Inputs: For MASK-WRITE cycle only.
7	ME/WE	Input	Mask Enable: If ME/WE is LOW at the falling edge of RAS a MASK-WRITE cycle is performed, or
			Write Enable: $\overline{WE}$ is used to select a READ ( $\overline{WE}$ = H) or WRITE ( $\overline{WE}$ = L) cycle when accessing the DRAM. This includes a DRAM-TO-SAM TRANSFER ( $\overline{WE}$ = H) or SAM-TO-DRAM TRANSFER ( $\overline{WE}$ = L).
8	RAS	Input	Row Address Strobe: RAS is used to clock in the 8 Row Address bits and as a strobe for the MASK ENABLE and TRANSFER functions.
9, 10, 11, 13, 14, 15, 16, 17	A0 to A7	Input	Address Inputs: For the DRAM operation these inputs are multiplexed and clocked by RAS and CAS to select 4 bits out of the 256K available. During TRANSFER operations, A0 to A7 indicate the DRAM row being accessed (when RAS goes low) and the SAM start address (when CAS goes slow).
12	Vcc	Supply	Power Supply: +5 Volts ±10%
18	CAS	Input	Column Address Strobe: RAS is used to clock in the 8 column address bits and enable the DRAM output buffers (TR/OE must also be LOW).
21	SE	Input	Serial Port Enable: SE enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a high impedance state. SE is also used during a TRANSFER operation to indicate whether a SAM-TO-DRAM TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
24	Vss	Supply	Ground

#### **FUNCTIONAL DESCRIPTION**

The DPDRAM can be divided into three functional blocks (see Figure 1); the DRAM, the Transfer Control circuitry, and the Serial Access Memory (SAM). All of the operations described below are also shown in the AC Timing Diagrams section of this data sheet as well as summarized in the Functional Truth Table.

Note:

For dual function pins, the function that is not being discussed will be surrounded by paranthesis. For example, when discussing transfer operations the  $\overline{TR}/\overline{OE}$  pin will be shown as  $\overline{TR}/\overline{OE}$ ).

#### DRAM OPERATION

The DRAM portion of the DPDRAM is functionally identical to standard 64K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or "don't care" states for the DRAM are specified for the DPDRAM. These conditions are highlighted in the following discussion.

#### **READ/WRITE Cycles**

The 16 address bits that are used to select four memory bits from the  $65,536 \times 4$  available are latched into the chip using the A0 -A7,  $\overline{RAS}$ , and  $\overline{CAS}$  inputs. First, the 8 row address bits are set up on the address inputs and clocked into the part when  $\overline{RAS}$  transitions from HIGH to LOW. Next, the 8 column address bits are set up on the address inputs and clocked in when  $\overline{CAS}$  goes from HIGH to LOW.

For single port DRAMs the  $\overline{OE}$  pin is a "don't care" when  $\overline{RAS}$  goes LOW. For the DPDRAM,  $(\overline{TR})/\overline{OE}$  is used, when  $\overline{RAS}$  goes LOW, to select between an internal transfer operation and a DRAM operation.

(TR)/OE must be HIGH at the RAS HIGH to LOW transition for a DRAM port READ or WRITE operation.

If (ME)/WE is HIGH when CAS goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1 - DQ4 port. The (TR)/OE input must be LOW to enable the DRAM output port.

For single port DRAMS,  $\overline{WE}$  is a "don't care" when  $\overline{RAS}$  goes LOW. For the DPDRAM,  $\overline{(ME)}/\overline{WE}$  is used, when  $\overline{RAS}$  goes LOW, to select between a MASK WRITE cycle and a normal WRITE cycle. If  $\overline{(ME)}/\overline{WE}$  is LOW at the  $\overline{RAS}$  HIGH to LOW transition a MASK WRITE operation is selected. For a normal DRAM WRITE operation,  $\overline{(ME)}/\overline{WE}$  must be HIGH at the  $\overline{RAS}$  HIGH to LOW transition.  $\overline{(ME)}/\overline{WE}$  is a "don't care" at the  $\overline{RAS}$  HIGH to LOW transition for a DRAM READ cycle.

If  $(\overline{\text{ME}})/\overline{\text{WE}}$  is LOW when  $\overline{\text{CAS}}$  goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1 - DQ4 port will be written into the selected memory cells. If  $\overline{\text{ME}}/(\overline{\text{WE}})$  is LOW when  $\overline{\text{RAS}}$  goes LOW the input data will be "masked" before being stored in the DRAM.

The DPDRAM can perform all the normal DRAM cycles including EARLY-WRITE, LATE-WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE-MODE READ, PAGE-MODE WRITE, and PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in this data sheet for more details on these operations.

#### MASK-WRITE

If  $\overline{\text{ME}}/(\overline{\text{WE}})$  is LOW at the  $\overline{\text{RAS}}$  HIGH to LOW transition, the data (mask data) present on the DQ1 - DQ4 inputs will be written into the bit mask data register. The mask data acts as an individual write enable for each of the four DQ1 - DQ4 pins. If a LOW (logic 0) is written to a mask data register bit the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. Note that  $\overline{\text{CAS}}$  is still HIGH. When CAS goes LOW, the bits present on the DQ1 - DQ4 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. Since the mask data register is reset (to all 1's) at the end of every MASK-WRITE cycle, new mask data must be supplied at the beginning of each MASK-WRITE cycle. An example of a typical MASK-WRITE cycle is shown in Figure 2.



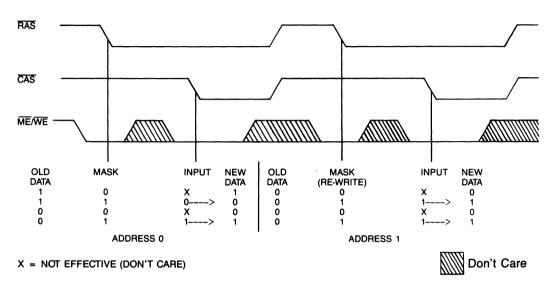


Figure 2
MT42C4064 Bit MASK-WRITE

#### **REFRESH**

The MT42C4064 supports  $\overline{RAS}$  ONLY,  $\overline{CAS}$ -BEFORE- $\overline{RAS}$ , and HIDDEN types of refresh cycles. All 256 row address combinations must be accessed within 4ms. For the  $\overline{CAS}$ -BEFORE- $\overline{RAS}$  refresh mode the row addresses are generated internally and the user need not supply them

as he must in  $\overline{RAS}$  ONLY refresh.  $\overline{TR}/(\overline{OE})$  must be HIGH when  $\overline{RAS}$  goes LOW for the  $\overline{RAS}$  ONLY and  $\overline{CAS}$ -BEFORE- $\overline{RAS}$  types of refresh cycles. Any READ, WRITE, or TRANSFER operation also refreshes the DRAM row that is being accessed.

# TRANSFER OPERATION DRAM-TO-SAM TRANSFER (READ TRANSFER)

A TRANSFER operation is initiated when  $\overline{TR}/(\overline{OE})$  is LOW at  $\overline{RAS}$  (HIGH to LOW) time.  $(\overline{ME})/\overline{WE}$  indicates the direction of the transfer and must be HIGH as  $\overline{RAS}$  goes LOW for a DRAM-TO-SAM TRANSFER. In this case, the row address bits indicate the four 256 bit DRAM rows that are to be transferred to the four SAM data registers and the column address bits indicate the start address of the next SERIAL OUTPUT cycle from the SAM data registers. RAS and  $\overline{\text{CAS}}$  are used to strobe the address bits into the part. To complete the TRANSFER, TR/(OE) is taken HIGH while RAS and CAS are still LOW. The 1024 bits of DRAM data are then written into the SAM data registers and the serial shift start address is stored in an internal 8 bit register. There must be no rising edges on the Serial Clock (SC) input while the transfer is taking place (refer to the AC timing diagrams). TRANSFER cycles are the only time when SC must be synchronized with the DRAM RAS and  $\overline{CAS}$  timing. If  $\overline{SE}$  is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. SE enables the serial outputs and may be either HIGH or LOW during this operation.

#### SAM-TO-DRAM TRANSFER (WRITE TRANSFER)

The SAM-TO-DRAM TRANSFER operation is identical to the DRAM-TO-SAM TRANSFER described above except that  $(\overline{\text{ME}})/\overline{\text{WE}}$  and  $\overline{\text{SE}}$  must be LOW when  $\overline{\text{RAS}}$  goes LOW. The row address indicates the DRAM row that the SAM data registers will be written to and the column address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. If  $\overline{\text{SE}}$  is HIGH when  $\overline{\text{RAS}}$  goes LOW, a SERIAL INPUT MODE ENABLE cycle is performed.

# SAM OPERATION SERIAL INPUT/OUTPUT MODE CONTROL

The SAM port is automatically placed in the serial output mode after a DRAM-TO-SAM TRANSFER operation. Conversely, after a SAM-TO-DRAM TRANSFER the SAM port will be in the serial input mode.

## SERIAL INPUT MODE ENABLE (PSEUDO WRITE TRANSFER)

It is possible to change the direction of the SAM port from output to input without performing a SAM-TO-DRAM TRANSFER. This operation, called a SERIAL INPUT MODE ENABLE cycle, is simply a SAM-TO-DRAM TRANSFER cycle with SE held HIGH instead of LOW. The DRAM data will not be disturbed and the data registers will be ready to accept input data.

The only way to put the SAM port in the serial output mode is to do a DRAM-TO-SAM TRANSFER.

#### SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and  $\overline{\text{SE}}$ . The rising edge of SC increments the serial address counter and provides access to the next SAM location.  $\overline{\text{SE}}$  enables or disables the serial input/output buffers.

Serial output of the SAM data register contents will start at the serial start address that was loaded during the DRAM-TO-SAM TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the four bit port.  $\overline{SE}$  is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW to HIGH transition, regardless of whether  $\overline{SE}$  is HIGH or LOW, and will wrap around to location 0 after reaching its maximum count of 255.

SC is also used to clock in data when the device is in the serial input mode. As in the serial output operation, the contents of the serial address register, which was loaded when the serial input mode was enabled, will determine the serial address that the first bit will be written.  $\overline{SE}$  acts as an enable for serial data input and must be LOW for normal serial input. If  $\overline{SE}$  is HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address register is incremented with every  $L \rightarrow H$  transition of SC, regardless of the logic level on the  $\overline{SE}$  input.

### MICRON

#### **FUNCTIONAL TRUTH TABLE**

DRAM Operations (SC, SE, and SDQ1 — SDQ4 are don't care)

F Ai	546	040	ME	WE	TR	/OE	Addre	sses	DQ1	11-4
Function	RAS	CAS	tR*	tC*	tR*	tC*	tR*	tC*	to DQ4	Notes
Standby	Н	Н	Х	Х	Х	Х	Х	Х	High Impedance	
READ	L	L	Х	Н	Н	H→L	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	Н	L	Н	Х	ROW	COL	Data In	1
MASK-WRITE	H→L	L	L	L	Н	Х	ROW	COL	Mask Data In, Valid Data In	
READ-WRITE	L	L	Н	H→L	Н	L→H	ROW	COL	Valid Data Out,	1
PAGE-MODE READ	L	H→L→H, H→L→H	Н	Н	Н	H→L	ROW	COL	Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	Н	L	Н	Х	ROW	COL	Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H, H→L→H	Н	H→L	Н	L→H	ROW	COL	Valid Data Out, Valid Data In	1
RAS ONLY REFRESH	L	Н	X	n/a	Н	n/a	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Х	Н	Н	L	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Х	Х	Н	Х	Х	Х	High Impedance	

#### TRANSFER Operations (DQ1 — DQ4 are don't care)

Function	RAS	CAS	ME	WE	TR	OE	Addr	esses	sc	SE	SDQ1	Notes
	IIAG	CAS	tR*	tC*	tR*	tC*	tR*	tC*			SDQ4	
DRAM-TO-SAM TRANSFER	L	L	Н	Х	L	L	ROW	SSA**	Х	Х	Х	2
SAM-TO-DRAM TRANSFER	L	L	L	Х	L	Х	ROW	SSA**	Х	L	Х	3
SERIAL INPUT MODE ENABLE	L	L	L	Х	L	Х	ROW	SSA**	Х	Н	Х	4

- \*  $tR = when \overline{RAS} goes from HIGH to LOW$
- tC = when CAS goes from HIGH to LOW
- \*\* SSA = SAM Start Address, the serial address that the next serial input or output cycle will start with.
- Notes: 1. Any type of WRITE cycle may also be a MASK-WRITE cycle.
  - The SAM will be in a SERIAL OUTPUT mode after a DRAM-TO-SAM TRANSFER.
  - The SAM will be in a SERIAL INPUT mode after a SAM-TO-DRAM TRANSFER.
  - The SAM will be put in the SERIAL INPUT mode but the SAM-TO-DRAM TRANSFER will not occur.

## MICHON

#### Serial I/O Operations (RAS, CAS, ME/WE, TR/OE, and DQ1 - DQ4 are don't care)

Function	sc	SE	SDQ1 — SDQ4	Notes
SERIAL OUTPUT	L→H	L	Valid Data Out	5
SERIAL INPUT	L→H	L	Valid Data In	6

Notes: 5. The SAM must be in the SERIAL OUTPUT mode.

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V to +7.0V
Operating Temperature, Ta(Ambient)0°C to +70°C
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation1 Watt
Short Circuit Output Current50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### **RECOMMENDED DC OPERATING CONDITIONS**

 $(0^{\circ}C \le T_{\mathbf{A}} \le 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1

### DC ELECTRICAL CHARACTERISTICS

(Notes 3, 4, 5)  $(0^{\circ}C \le T_{A} \le 70^{\circ}C, Vcc = 5.0V \pm 10\%)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input (0V≤Vin≤Vcc, all other pins not under test = 0 volts).	lL	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V≤Vouт≤Vcc).	loz	-10	10	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA)	Vон	2.4		v	
Output Low voltage (louт = 5mA)	Vol		0.4	V	1

<sup>6.</sup> The SAM must be in the SERIAL INPUT mode.



#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A7), DIN	CI1		5	pF	18
Input Capacitance RAS, CAS, WE, OE, SC, SE	Cı2		7	pF	18
Output Capacitance Dout	Co		7	pF	18

CURRENT DRAIN, SAM IN STANDBY (Notes 2, 3) (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C, Vcc = 5.0V  $\pm$  10%)

PARAMETER/CONDITION OF DRAM	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS=Cycling; Trc=Trc(MIN)).	lcc1		40	mA	4
OPERATING CURRENT: PAGE-MODE (RAS=VIL, CAS=Cycling; TPC=TPC(MIN)).	lcc2		40	mA	4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS=CAS=VIH after 8 RAS cycles min).	Іссз		10	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current (RAS=CAS=Vcc-0.2V after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V).	lcc4		4	mA	
REFRESH CURRENT: RAS ONLY (RAS=Cycling; CAS=Vih).	lc c5		30	mA	
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS=Cycling).	lcc6		30	mA	5
SAM/DRAM DATA TRANSFER	lcc7		60	mA	

CURRENT DRAIN, SAM ACTIVE (tsc = MIN) (Notes 2, 3) (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C, Vcc = 5.0V  $\pm$  10%)

PARAMETER/CONDITION OF DRAM	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS=Cycling; Trc=Trc(MIN)).	lc c8		60	mA	4
OPERATING CURRENT: PAGE-MODE (RAS=VIL, CAS=Cycling; Tpc=Tpc(MIN)).	lc c9		60	mA	4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS=CAS=VIH after 8 RAS cycles min).	Icc10		30	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current (RAS=CAS=Vcc-0.2V after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V).	lcc11		25	mA	
REFRESH CURRENT: RAS ONLY (RAS=Cycling; CAS=Vih).	Icc12		50	mA	
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS=Cycling).	lcc13		50	mA	5
SAM/DRAM DATA TRANSFER	lcc14		90	mA	



#### **DRAM TIMING PARAMETERS**

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes 3, 4, 5, 10, 11, 17) (0°C $\leq$ T<sub>A</sub> $\leq$ + 70°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS			10		12		15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	250		295		345		ns	20, 21
PAGE-MODE READ or WRITE cycle time	<sup>t</sup> PC	75		90		110		ns	6, 7
PAGE-MODE READ-MODIFY- WRITE cycle time	<sup>t</sup> PRWC	125		150		175		ns	20, 21
Access time from RAS	<sup>t</sup> RAC		100		120		150	ns	7, 8
Access time from CAS	<sup>t</sup> CAC		50		60		75	ns	7, 9
RAS pulse width	<sup>t</sup> RAS	100	10,000	120	10,000	150	10,000	ns	
RAS pulse width (PAGE-MODE)	t <sub>RASP</sub>	100	100,000	120	100,000	150	100,000	ns	
RAS hold time	<sup>t</sup> RSH	50		60		75		ns	
RAS precharge time	t <sub>RP</sub>	80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	50	10,000	60	10,000	75	10,000	ns	
CAS hold time	t <sub>CSH</sub>	100		120		150		ns	
CAS precharge time	<sup>t</sup> CPN	15		20		25		ns	
CAS precharge time (PAGE-MODE)	t <sub>CP</sub>	15		20		25		ns	19
RAS to CAS delay	t <sub>RCD</sub>	10	50	15	60	15	75	ns	13
CAS to RAS precharge time	t <sub>CRP</sub>	10		10		10		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	10		15		15		ns	
Column address set-up time	t <sub>ASC</sub>	0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	20		20		25		ns	
Column address hold time (referenced to RAS)	t <sub>AR</sub>	60		70		80		ns	
READ command set-up time	t <sub>RCS</sub>	0		0		0		ns	
READ command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	14
READ command hold time (referenced to RAS)	tRRH	0		Ö		0		ns	



DRAM TIMING PARAMETERS (Continued) ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes 3, 4, 5, 10, 11, 17) (0°C  $\leq$  T<sub>A</sub>  $\leq$  + 70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS PARAMETER	T		10	-12		-15			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command set-up time	twcs	0		0		0		ns	16
WRITE command hold time	twcH	20		25		30		ns	
WRITE command hold time (referenced to RAS)	twcR	70		80		90		ns	
WRITE command pulse width	t <sub>WP</sub>	20		25		30		ns	
WRITE command to RAS lead time	t <sub>RWL</sub>	25		30		35		ns	
WRITE command to CAS lead time	tCWL	25		30		35		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	15
Data-in hold time	t <sub>DH</sub>	15		20		25		ns	15
Data-in hold time (referenced to RAS)	t <sub>DHR</sub>	70		80		90		ns	
CAS to WE delay	tCWD	65		80		95		ns	16, 20
RAS to WE delay	t <sub>RWD</sub>	120		150		185		ns	16, 20
ME/WE to RAS Set Up Time	twsR	0		0		0	ns		
ME/WE to RAS Hold Time	<sup>t</sup> RWH	10		10		15	ns		
Mask Data (DQ_) to RAS Set Up Time	t <sub>MS</sub>	0		0		0		ns	
Mask Data (DQ_) to RAS Hold Time	<sup>t</sup> MH	20		20		25		ns	
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	
Refresh Period (256 cycles)	t <sub>REF</sub>		4		4		4	ms	
CAS set-up time (CAS-before-RAS refresh)	tcsr	10		10		10		ns	
CAS hold time (CAS-before- refresh)	tCHR	20		25		30		ns	22
CAS to output in low-Z	t <sub>CLZ</sub>	5		5		5		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	25	0	25	0	30	ns	12
Output Enable	<sup>t</sup> OE		25		25		30	ns	
Output Disable	t <sub>OD</sub>		25		25		30	ns	

#### NOTES

- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- An initial pause of 100μs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The RAS cycle wake-up should be repeated any time the 4ms static refresh requirement is exceeded.
- 4. AC characteristics assume <sup>t</sup>T = 5ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- Measured with a load equivalent to 2 TTL gates and 100pF.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 9. Assumes that  ${}^{t}RCD \ge {}^{t}RCD \pmod{max}$ .
- 10. If  $\overline{CAS}$  = VIH, DRAM data output is high impedance.
- 11. If  $\overline{\text{CAS}} = \text{Vil.}$ , DRAM data output may contain data from the last valid READ cycle.
- 12. <sup>†</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to Voн or Vol.
- 13. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is con trolled exclusively by <sup>t</sup>CAC.
- 14. <sup>t</sup>RCH is referenced to the first rising edge of <del>RAS</del> or <del>CAS</del>.

- These parameters are referenced to CAS leading edge in EARLY WRITE cycles and to WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
- 16. <sup>t</sup>WCS, <sup>t</sup>CWD and <sup>t</sup>RWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an EARLY-WRITE cycle and the data output will remain open circuit throughout the entire cycle. If <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) and <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back toV1H) is indeterminate.
- 17. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 18. Capacitance calculated from the equation  $C = \underline{I\Delta t} \Delta V$  with  $\Delta V = 3V$  and Vcc = 5V. This parameter is sampled.
- 19. If <del>CAS</del> is low at the falling edge of <del>RAS</del>, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer <del>CAS</del> must be pulsed high for <sup>t</sup>CP. Note 8 applies to determine valid data out.
- 20. Includes the  $\overline{\text{OE}}$  delay time (30ns for the -10, 40ns for the -12, and 50ns for the -15).
- 21. During a READ cycle if  $\overline{OE}$  is low then taken high (VIH) DOUT goes open. If  $\overline{OE}$  is tied permanently low a READ-MODIFY-WRITE operation is not possible.
- 22. Enables on-chip refresh and address counters.
- 23. TRANSFER Command means that  $\overline{TR}/(\overline{OE})$  is LOW when  $\overline{RAS}$  goes LOW.
- 24. NON-TRANSFER Command means that  $\overline{TR}/(\overline{OE})$  is HIGH when  $\overline{RAS}$  goes LOW.
- 25. Measured with a load equivalent to 2 TTL gates and 50pF.



## TRANSFER AND MODE CONTROL TIMING PARAMETERS ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes 3, 4, 5, 17, 25) (0° C $\leq$ T<sub>A</sub> $\leq$ + 70°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS		-	10	-	12		15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
TRANSFER Command to RAS Set Up Time	<sup>t</sup> TS	0		0		0		ns	23
TRANSFER Command to RAS Hold Time	t <sub>RTH</sub>	80		90		100		ns	23
TRANSFER Command to CAS Hold Time	<sup>t</sup> CTH	30		30		35		ns	23
TRANSFER Command to SC Lead Time	<sup>t</sup> TSL	5		5		10		ns	23
TRANSFER Command to RAS Lead Time	t <sub>TRL</sub>	10		10		10		ns	23
TRANSFER Command to RAS Delay Time	<sup>t</sup> TRD	15		15		. 20		ns	23
TRANSFER Command to CAS Time	<sup>t</sup> TCL	10		10		10		ns	23
TRANSFER Command to CAS Delay Time	<sup>t</sup> TCD	15		15		20		ns	23
First SC edge to TRANSFER Command Delay Time	<sup>t</sup> TSD	10		10		20		ns	23
SAM-TO-DRAM (WRITE) Transfer Command to RAS Hold Time	tRTHW	10		10		15		ns	
Serial Output Buffer Turn Off Delay from RAS	t <sub>SDZ</sub>	10	40	10	50	10	60	ns	
SC to RAS Set Up Time	t <sub>SRS</sub>	35		40		45		ns	
RAS to SC Delay Time	<sup>t</sup> SRD	25		30		35		ns	
Serial Data Input to SE Delay Time	t <sub>SZE</sub>	0		0		0		ns	
RAS to SD Buffer Turn On Time	<sup>t</sup> SRO	0		0		0		ns	
Serial Data Input Delay from RAS	t <sub>SDD</sub>	50		55		60		ns	
Serial Data Input to RAS Delay Time	t <sub>SZS</sub>	0		0		0		ns	
Serial Input Mode Enable (SE) to RAS Set Up Time	t <sub>ESR</sub>	0		0		0		ns	
Serial Input Mode Enable (SE) to RAS Hold Time	<sup>t</sup> REH	10		10		15		ns	
NON-TRANSFER Command to RAS Set Up Time	<sup>t</sup> YS	0		0		0		ns	24
NON-TRANSFER Command to RAS Hold Time	<sup>t</sup> YH	10		10		10		ns	24



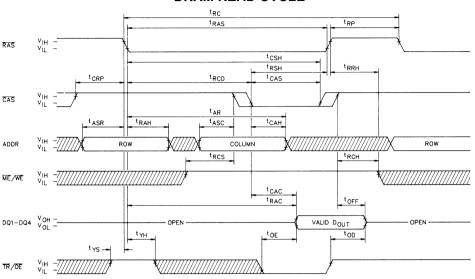
#### **SAM TIMING PARAMETERS**

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes 3, 4, 5, 17, 25) (0° C  $\leq$  T<sub>A</sub>  $\leq$  + 70°C, Vcc = 5.0V  $\pm$  10%)

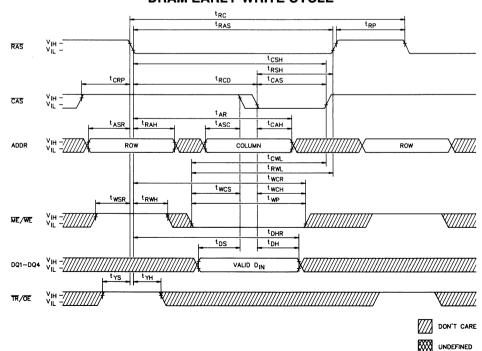
A.C. CHARACTERISTICS		-	10	-	-12		-12 -15		5		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES		
Serial Clock Cycle Time	tsc tsc	40	50000	40	50000	60	50000	ns			
Access Time from SC	t <sub>SAC</sub>		40	i	40		60	ns			
SC Precharge Time	<sup>t</sup> SP	10		10		20		ns			
SC Pulse Width	t <sub>SAS</sub>	10		10		20		ns			
Access Time from SE	<sup>t</sup> SEA		25		30		40	ns			
SE Precharge Time	t <sub>SEP</sub>	15		15		20		ns			
SE Pulse Width	<sup>t</sup> SE	15		15		20		ns			
Serial Data Out Hold Time after SC High	<sup>t</sup> soH	10		10		10		ns			
Serial Output Buffer Turn Off Delay from SE	<sup>t</sup> SEZ	0	15	0	25	0	30	ns	i		
Serial Data in Set Up Time	tsds	0		0		0		ns			
Serial Data in Hold Time	<sup>t</sup> SDH	20		20		25					
SERIAL INPUT (Write) Enable Set Up Time	tsws	0		0		0		ns			
SERIAL INPUT (Write) Enable Hold Time	<sup>t</sup> swH	30		35		45		ns			
SERIAL INPUT (Write) Disable Set Up Time	tswis	0		0		0		ns			
SERIAL INPUT (Write) Disable Hold Time	<sup>t</sup> SWIH	30		35		45		ns			

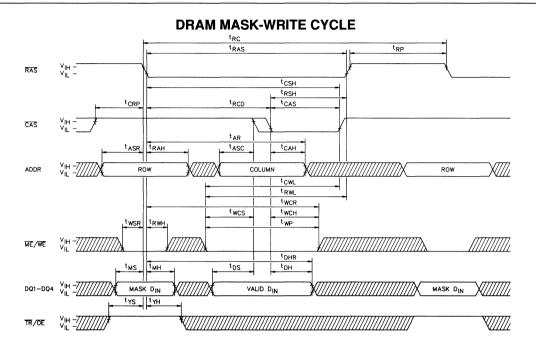


#### **DRAM READ CYCLE**

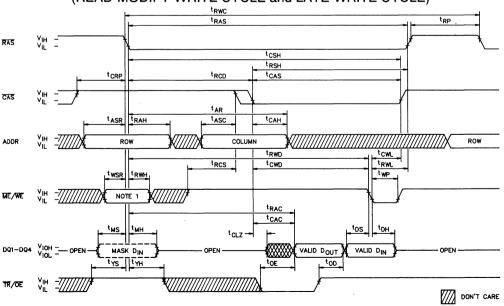


#### **DRAM EARLY-WRITE CYCLE**



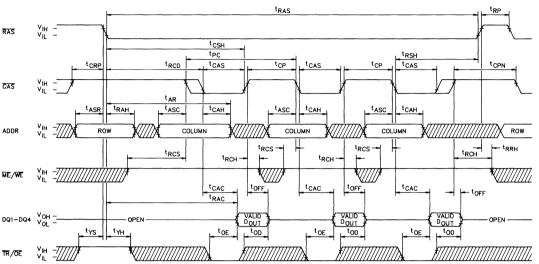


DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE and LATE-WRITE CYCLE)

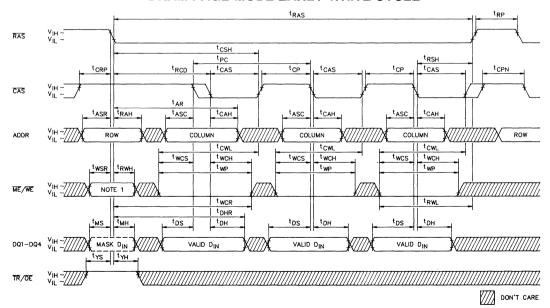




### **DRAM PAGE-MODE READ CYCLE**

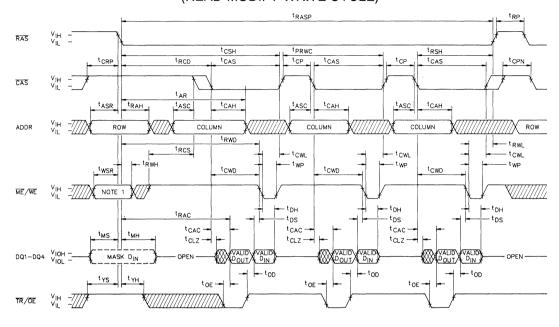


#### DRAM PAGE-MODE EARLY-WRITE CYCLE



NOTE: If ME/WE is LOW, a MASK-WRITE cycle will be performed.

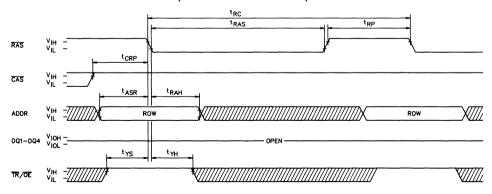
# DRAM PAGE-MODE READ-WRITE CYCLE (READ-MODIFY-WRITE CYCLE)



NOTE: 1: If ME/WE is LOW, a MASK-WRITE cycle will be performed

### **RAS** ONLY REFRESH CYCLE

(ME/WE = Don't Care)

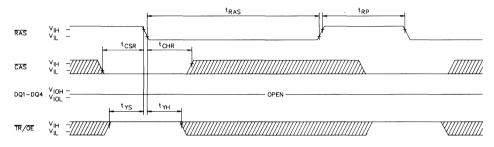


DON'T CARE

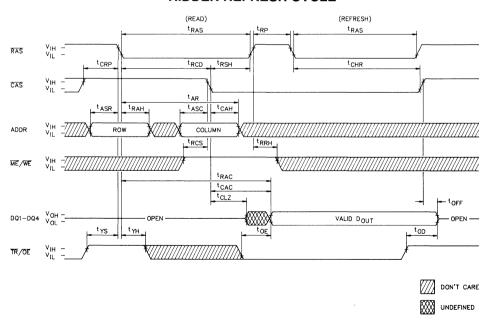


### **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_7 \text{ and } \overline{ME}/\overline{WE} \text{ are Don't Care.})$ 



#### **HIDDEN REFRESH CYCLE**

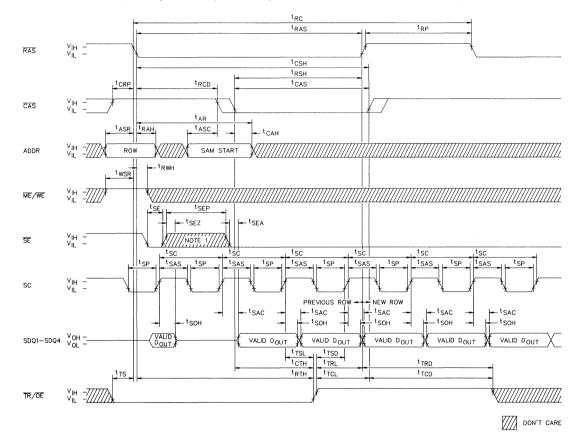


**NOTE:** A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{\text{ME/WE}} = \text{LOW}$  (when  $\overline{\text{CAS}}$  goes LOW) and  $\overline{\text{TR/OE}} = \text{HIGH}$ .



# DRAM-TO-SAM TRANSFER (READ TRANSFER)

(When part was previously in the SERIAL OUTPUT mode.)

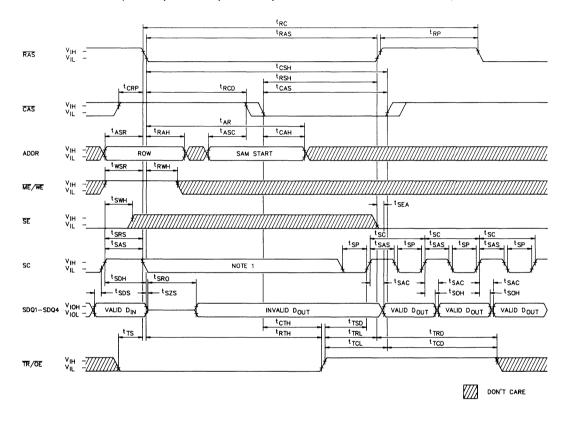


NOTE 1: This SE pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.



# DRAM-TO-SAM TRANSFER (READ TRANSFER)

(When part was previously in the SERIAL INPUT mode.)

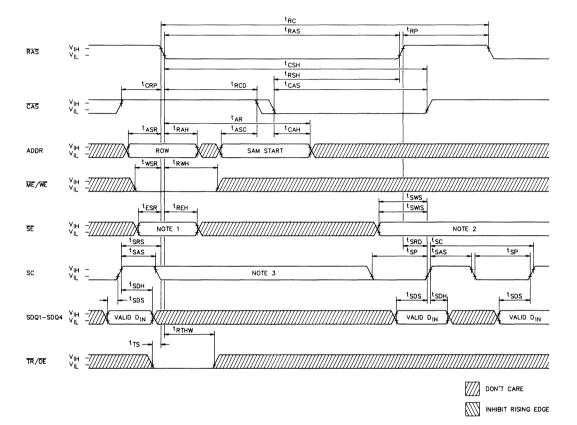


NOTE 1: There must be no rising edges on the SC input during this time.



# SAM-TO-DRAM TRANSFER (WRITE TRANSFER)

(When part was previously in the SERIAL INPUT mode.)



**NOTE 1:** If  $\overline{SE}$  is LOW, the SAM data will be transferred to the DRAM.

If SE is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless

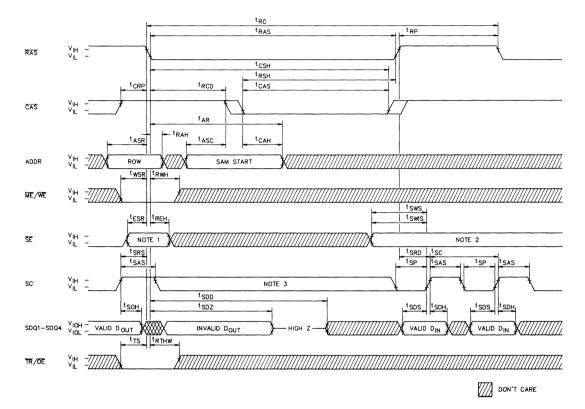
of SE.

NOTE 3: There must be no rising edges on the SC input during this time.



# SAM-TO-DRAM TRANSFER (WRITE TRANSFER or PSEUDO WRITE TRANFER)

(When part was perviously in the SERIAL OUTPUT mode.)



**NOTE 1:** If  $\overline{SE}$  is LOW, the SAM data will be transferred to the DRAM.

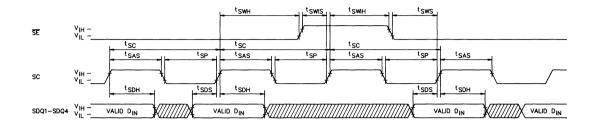
If SE is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless of SE.

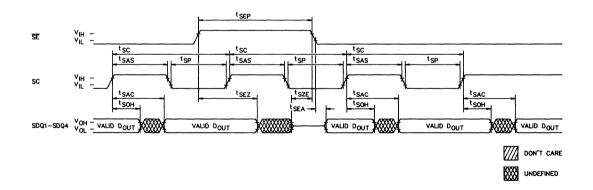
NOTE 3: There must be no rising edges on the SC input during this time.



#### **SAM SERIAL INPUT**

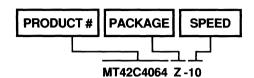


### **SAM SERIAL OUTPUT**





#### **ORDER INFORMATION**



The Micron MT42C4064 is functionally equivalent to other manufacturer's products meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the high speed,

low power CMOS double poly, single metal process. Micron's QUALITY ASSURED policy is to offer prompt, accurate, and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply, temperature, and refresh range than specified. Each unit receives accelerated burn-in and and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. ,

# 256K x 4 DRAM with 512 x 4 SAM

### **FEATURES**

VRAM

- Industry standard pin-out, timing, and functions
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS, and HIDDEN
- 512 cycle refresh within 8ms
- Optional FAST PAGE MODE access cycles
- Dual port organization: 256K x 4 DRAM port
   512 x 4 SAM port
- No refresh required for Serial Access Memory
- Low power: 5mw standby, 200mw active, typical
- Fast access times 80ns random, 25ns serial

#### SPECIAL FUNCTIONS

- Masked Write
- · Persistent Masked Write
- Split READ and WRITE Transfers
- · Block Write
- Serial Input

OPTIONS	MARKING
<ul> <li>Timing (DRAM, SAM)</li> </ul>	
80ns, 25ns	-8
100ns, 30ns	-10
120ns, 35ns	-12
150ns, 40ns	-15

#### **GENERAL DESCRIPTION**

The MT42C4256 is a high speed, dual port CMOS dynamic random access memory (DPDRAM) containing 1,048,576 bits. They can be accessed either by a four bit wide DRAM port or by a 512 x 4 bit serial access memory (SAM) port. Data can be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the DPDRAM is functionally identical to the MT4C4256 (256K  $\times$  4) bit DRAM. Four 512 bit data registers make up the serial access memory portion of the DPDRAM. Data I/O and internal data transfer is accomplished using three separate bidirectional data paths; the four bit random access I/O port, the four internal 512 bit wide paths between the DRAM and the SAM, and the four bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

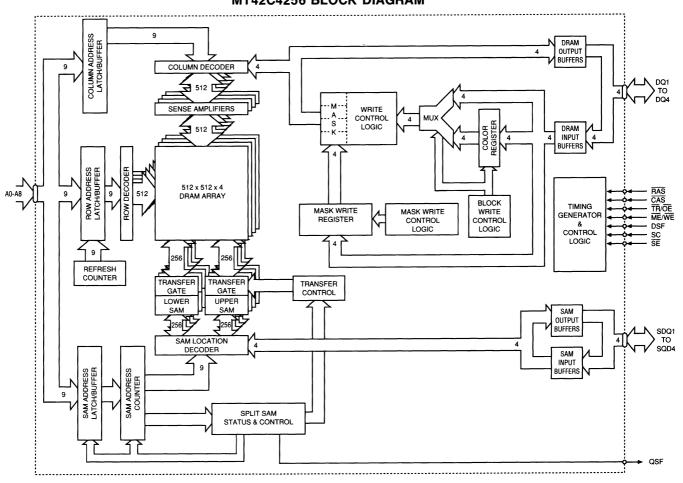
28-Pin DIP  SC (1 28) Vss  SD01   2 27   SD04  S0 1   2 27   SD04
1 and 1 and 2 DQ3
SDUCT   2   27   SDUC4   SDUC3   SDU

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs the DPDRAM must be refreshed in order to maintain data. The refresh cycles must be timed so that all 512 combinations of RAS addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the DPDRAM is fully static and does not require any refresh.

The operation and control of the MT42C4256 is compatible with (and can be identical to) the operation of the MT42C4064 64Kx4 Video RAM. However, the MT42C4256 offers several additional functions which may be used to increase system performance or ease critical timing requirements. These "special functions" are described in detail in the following section.

MT42C4256

# MT42C4256 BLOCK DIAGRAM



3-30



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# **PIN DESCRIPTIONS**

DIP/SOJ PIN NUMBER(S)	ZIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
5, 6, 23, 24	12, 13, 2, 3	DQ1 - DQ4	Input/ Output	DRAM Data I/O, inputs for MASK REGISTER and COLOR REGISTER load cycles, and ADDRESS MASK inputs for BLOCK WRITE.
19, 18, 17, 16, 13, 12, 11, 15, 10	26, 25, 24, 23, 20, 19, 18, 22, 17	A0 to A8	Input	Address Inputs: For the DRAM operation these inputs are multiplexed and clocked by RAS and CAS to select 4 bits out of the 256K x 4 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when RAS goes low) and the SAM start address (when CAS goes low).
9	16	RAS	Input	Row Address Strobe: RAS is used to clock in the 9 Row Address bits and as a strobe for the ME/WE, TR/OE, and DSF inputs.
21	28	CAS	Input	Column Address Strobe: CAS is used to clock in the 9 column address bits and enable the DRAM output buffers (along with TR/OE) and as a strobe for the DSF input.
7	14	ME/WE	Input	Mask Enable: If ME/WE is LOW at the falling edge of RAS a MASK-WRITE cycle is performed, or Write Enable: ME/WE is also used to select a READ
				(ME/WE = H) or WRITE (ME/WE = L) cycle when accessing the DRAM. This includes a READ TRANSFER (ME/WE = H) or WRITE TRANSFER (ME/WE = L).
4	11	TR/OE	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H $\rightarrow$ L), or
				Output Enable: Enables the DRAM output buffers when taken LOW after RAS goes LOW (CAS must also be LOW), otherwise the output buffers are in a high impedance state.
2, 3, 26, 27	9, 10, 5, 6	SDQ1 - SDQ4	Input/ Output	Serial Data I/O: Input, Output, or high impedance.
1	8	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
25	4	SE	Input	Serial Port Enable: SE enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a high impedance state. SE is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
22	1	DSF	Input	Special Function Select: DSF is used to indicate which special functions (Block Write, Masked Write vs. Persistent Masked Write, etc.) are used on a particular access cycle.
20	27	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed when the Split SAM Transfer mode is being used.
8	15	NC	_	No Connect - This pin should be either left unconnected or tied to ground.
14	21	Vcc	Supply	Power Supply: +5 Volts ±10%
28	7	Vss	Supply	

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#### **FUNCTIONAL DESCRIPTION**

The MT42C4256 can be divided into three functional blocks (see Figure 1); the DRAM, the Transfer circuitry, and the Serial Access Memory (SAM). All of the operations described below are also shown in the AC Timing Diagrams section of this data sheet as well as summarized in the Functional Truth Table.

Note:

For dual function pins, the function that is not being discussed will be surrounded by paranthesis. For example, when discussing transfer operations the  $\overline{TR}/\overline{OE}$  pin will be shown as  $\overline{TR}/\overline{OE}$ ).

### **DRAM OPERATION**

#### DRAM REFRESH

Like any DRAM based memory, the MT42C4256 Video RAM must be refreshed in order to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C4256 supports CAS-BEFORE-RAS, RAS ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS refresh mode the row addresses are generated and stored in an internal address counter. The user need not supply any address data and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for  $\overline{RAS}$  ONLY refresh cycles. The DQ I/O pins remain in a high -Z state for both the  $\overline{RAS}$  ONLY and  $\overline{CAS}$ -BEFORE- $\overline{RAS}$  refresh cycles.

HIDDEN refresh cycles are performed by toggling  $\overline{RAS}$  (and keeping  $\overline{CAS}$  low) after a READ or WRITE cycle. This performs  $\overline{CAS}$ -BEFORE- $\overline{RAS}$  refresh cycles but does not disturb the DO lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM portion of the MT42C4256 does not require any refreshing.

#### DRAM READ AND WRITE CYCLES

The DRAM portion of the DPDRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or

"don't care" states for the DRAM are specified for the DPDRAM. These conditions are highlighted in the following discussion. In addition, the DPDRAM has several special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select four memory bits from the 262,144 x 4 available are latched into the chip using the A0-A8,  $\overline{RAS}$  and  $\overline{CAS}$  inputs. First, the 9 row address bits are set-up on the address inputs and clocked into the part when  $\overline{RAS}$  transitions from high to low. Next, the 9 column address bits are set-up on the address inputs and clocked in when  $\overline{CAS}$  goes from high to low.

For single port DRAMS the  $\overline{OE}$  pin is a "don't care" when  $\overline{RAS}$  goes low. For the DPDRAM,  $(\overline{TR})/\overline{OE}$  is used, when  $\overline{RAS}$  goes low, to select between DRAM and TRANSFER CYCLES.  $(\overline{TR})/\overline{OE}$  must be high at the  $\overline{RAS}$  high to low transistion for all DRAM operations (except  $\overline{CAS}$ -BEFORE- $\overline{RAS}$  refresh).

If  $(\overline{\text{ME}})/\overline{\text{WE}}$  is high when  $\overline{\text{CAS}}$  goes low, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The  $(\overline{\text{TR}})/\overline{\text{OE}}$  input must transistion from high to low sometime after  $\overline{\text{RAS}}$  falls in order to enable the DRAM output port.

For single port normal DRAMs,  $\overline{WE}$  is a "don't care" when  $\overline{RAS}$  goes low. For the DPDRAM,  $(\overline{ME})/\overline{WE}$  is used, when  $\overline{RAS}$  goes low, to select between a MASK WRITE cycle and a normal WRITE cycle. If  $(\overline{ME})/\overline{WE}$  is low at the  $\overline{RAS}$  high to low transition a MASK WRITE operation is selected. For a normal DRAM WRITE operation,  $(\overline{ME})/\overline{WE}$  must be high at the  $\overline{RAS}$  high to low transition.  $(\overline{ME})/\overline{WE}$  is a "don't care" at the  $\overline{RAS}$  high to low tansition for a DRAM READ cycle.

If  $(\overline{\text{ME}})/\overline{\text{WE}}$  is low when  $\overline{\text{CAS}}$  goes low, a DRAM WRITE operation is performed and the data present on the DQ1-DQ4 data port will be written into the selected memory cells. If  $\overline{\text{ME}}/(\overline{\text{WE}})$  is low when  $\overline{\text{RAS}}$  goes low the input data will be "masked" before being stored in the DRAM.

The DPDRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, PAGE-MODE READ, PAGE-MODE WRITE, and PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

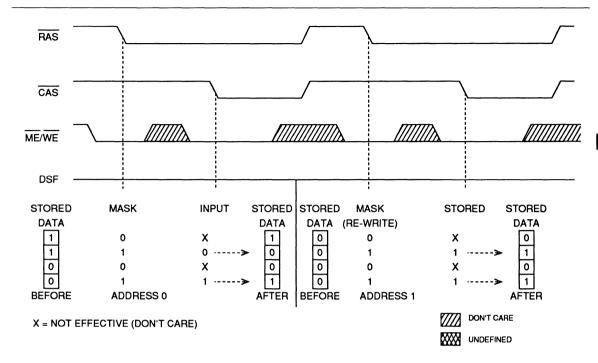


Figure 2
NON-PERSISTENT MASKED WRITE EXAMPLE

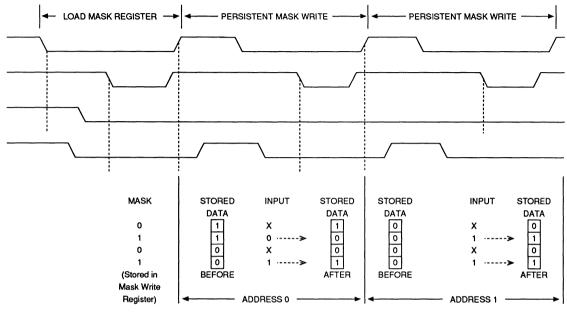
#### NON-PERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only certain bits within a four bit word. The MT42C4256 supports two types of MASKED WRITE cycles, NON-PERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If  $\overline{\text{ME}}/(\overline{\text{WE}})$  is low and DSF is low at the  $\overline{\text{RAS}}$  high to low transition, the data (mask data) present on the DQ1-DQ4 inputs will be written into the MASK WRITE data register. The mask data acts as an individual write enable for each of the four DQ1-DQ4 pins. If a low(logic 0) is written to a mask data register bit the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A high (logic 1)

on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that  $\overline{CAS}$  is still high. When  $\overline{CAS}$  goes low, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit was high) or ignored (if the mask data bit was low). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. For NON-PERSISTENT MASKED WRITE cycles the mask data register is reset (to all ones) at the end of the cycle and new mask data must be supplied for each NON-PERSISTENT MASKED WRITE cycle, even if the same mask data is being used repeatedly. An example of NON-PERSISTENT MASKED WRITE cycle is shown in Figure 2.

VRAM



X = NOT EFFECTIVE (DON'T CARE)

Figure 3 PERSISTENT MASKED WRITE EXAMPLE

### PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the MASK data before each MASK WRITE cycle if the same MASK data is being used repeatedly. The internal MASK WRITE DATA REGISTER is loaded when  $\overline{RAS}$  goes low by holding  $\overline{ME}/(\overline{WE})$  high and DSF high (see LOAD MASK REGISTER).

PERSISTENT MASKED WRITE cycles can then be performed by simply taking ME/(WE) low and DSF high when RAS goes low. The contents of the PERSISTENT MASK DATA REGISTER will then be used as the mask data for the DRAM inputs. Unlike the NON-PERSISTENT MASKED WRITE cycle, the contents of the MASK WRITE DATA REGISTER are not reset at the end of a PERSIS-TENT MASKED WRITE cycle. Another PERSISTENT MASKED WRITE cycle can be performed without having to reload the MASK DATA register. Figure 3 shows the LOAD WRITE MASK REGISTER and PERSISTENT MASKED WRITE cycle operation.

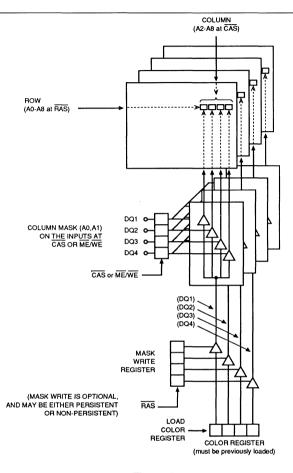


Figure 4
BLOCK WRITE EXAMPLE

#### **BLOCK WRITE**

If DSF is low when  $\overline{\text{CAS}}$  goes low the MT42C4256 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the Color Register are directly written to four adjacent column locations (see Figure 4). The Color Register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The ROW is addressed as in a normal DRAM WRITE cycle, however when  $\overline{CAS}$  goes low only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs are then used to determine what combination of the four column

locations will be changed. DQ1 acts as a write enable for column location A0=0, A1=0; DQ2 controls column location A0=1, A1=0; DQ3 controls A0=0, A1=1, and DQ4 controls A0=1, A1=1. The write enable controls are active high, a logic 1 enables and a logic 0 disables the WRITE function.

The contents of the Color Register will then be written to the column locations enabled. Each DQ location of the Color Register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

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#### NON-PERSISTENT MASKED BLOCK WRITE

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NON-PERSISTENT MASKED BLOCK WRITE operates exactly like the normal NON-PERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NON-PERSISTENT MASKED WRITE, the combination of  $\overline{\text{ME}}/(\overline{\text{WE}})$  low and DSF low when  $\overline{\text{CAS}}$  goes low initiates the NON-PERSISTENT MASKED BLOCK WRITE. By using both the Column Mask input and the MASKED WRITE function, any combination of the four bit planes can be masked and any combination fo the four column locations can be masked.

### PERSISTENT MASKED BLOCK WRITE

This cycle is also performed exactly like the normal PER-SISTENT MASKED WRITE except that DSF is high when CAS goes low to indicate the BLOCK WRITE function. Both the Mask Register and the Color Register must be loaded with the appropriate data prior to starting a PER-SISTENT MASKED BLOCK WRITE.

#### LOAD MASK REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is high when  $\overline{RAS}$  goes low. As shown in the Truth Table, the

combination of  $\overline{TR}/(\overline{OE})$ ,  $\overline{ME}/(\overline{WE})$ , and DSF being high when  $\overline{RAS}$  goes low indicates the cycle is a register load cycle. DSF is used when  $\overline{CAS}$  goes low to select the register to be loaded and must be low for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the MASK REGISTER.

Note: For a normal DRAM WRITE cycle the WRITE MASK REGISTER is disabled but not modified. The contents of WRITE MASK REGISTER will not be changed unless a NON-PERSISTENT MASK WRITE cycle or a LOAD MASK REGISTER cycle is performed

The ROW address supplied will be refreshed, but it is not necessary to provide any particular ROW address. The COLUMN address inputs are ignored during a LOAD MASK REGISTER cycle.

The MASK REGISTER contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the four DQ planes.

#### LOAD COLOR REGISTER

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is high when CAS goes low. The contents of the COLOR REGISTER are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

#### TRANSFER OPERATIONS

TRANSFER operations are initiated when  $\overline{TR}/(\overline{OE})$  is low when  $\overline{RAS}$  goes low. The state of  $\overline{(ME)}/\overline{WE}$  when  $\overline{RAS}$ goes low indicates the direction of the TRANSFER, and DSF is used to select between NORMAL TRANSFER cycles and SPLIT TRANSFER cycles. Each of the TRANSFER cycles available are described below.

#### READ TRANSFER (DRAM-TO-SAM TRANSFER)

If  $(\overline{ME})/\overline{WE}$  is high and DSF is low when  $\overline{RAS}$  goes low a READ TRANSFER cycle is selected. The row address bits indicate the four 512 bit DRAM rows that are to be tranferred to the four SAM data registers and the column address bits indicate the start address (or Tap point) of the next serial output cycle from the SAM data registers. To complete the TRANSFER,  $\overline{TR}/(\overline{OE})$  is taken high while  $\overline{RAS}$ and  $\overline{CAS}$  are still low. The rising edge of  $\overline{TR}/(\overline{OE})$  must occur between the rising edges of successive clocks on the SC input (refer to the AC Timing Diagrams). The 2048 bits of DRAM data are then written into the SAM data registers and the serial shift start address is stored in an internal 9 bit register. If SE is low, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. SE enables the serial outputs and may be either high or low during this operation. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

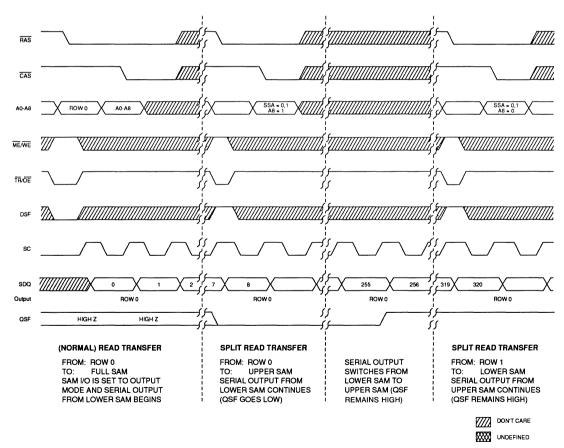


Figure 5 TYPICAL SPLIT READ TRANSFER INITIATION SEQUENCE

# SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the READ TRANSFER cycle had to occur immediately after the last bit of "old data" was clocked out the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data can be transferred to the other half. The transfer can occur at any time while the other half is sending data and need not be synchronized with the SC clock.

SPLIT TRANSFERS do not change the SAM I/O direction. A normal, or non-split, READ TRANSFER cycle must precede any sequence of SPLIT READ TRANSFER cycles in order to put the SAM I/O in the output mode and provide a SAM access (which half) reference. Then SPLIT READ TRANSFERS can be initiated by taking DSF high when RAS goes low during the transfer cycle. As in non-split transfers, the row address is used to specify the DRAM row to be transferred. The most significant column address, A8, is used to select which SAM half accepts the transfer (1=upper half, 0=lower half). The remainder of the column address bits determine the starting address (Tap) for the SAM half selected by A8.

Figure 5 shows a typical SPLIT READ TRANSFER initiation sequence. The normal READ TRANSFER is first performed, followed by a SPLIT READ TRANSFER of the same row to the upper half of the SAM. The purpose of the SPLIT TRANSFER of the same data is to initiate the split SAM operating mode and enable the QSF output. Serial

access continues, and when the SAM address counter reaches 256 (A8=1, A0-A7=0) the QSF output goes high. Since the serial access has now switched to the upper SAM, new data can now be transferred to the lower SAM. This sequence of waiting for the state of QSF to change and then transferring new data to the SAM half that is not being accessed can now be repreated. For example, the next step in Figure 5 would be to wait until QSF went low (indicating that Row 1 data is shifting out the lower SAM) and then transferring the upper half of Row 1 to the upper SAM.

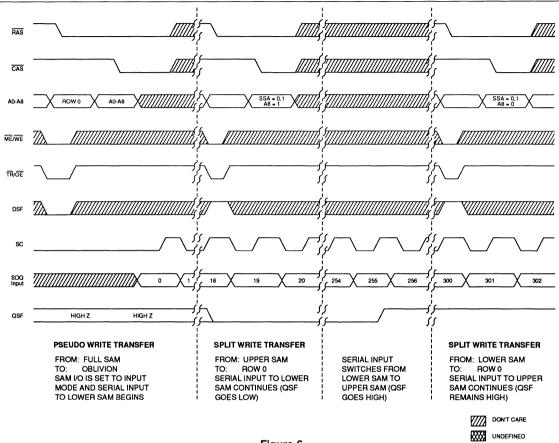
#### WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER function is identical to the READ TRANSFER FUNCTION described previously except  $\overline{(ME)}/\overline{WE}$  and  $\overline{SE}$  must be low when  $\overline{RAS}$  goes low. The row address indicates the DRAM row that the SAM data registers will be written to and the column address (SSA or Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. Performing a WRITE TRANSFER sets the direction of the SAM I/O buffers to the input mode.

# PSEUDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle can be used to change the direction of SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with SE held high instead of low. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

# MICRON



# Figure 6 TYPICAL SPLIT WRITE TRANSFER INITIATION SEQUENCE

# SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER)

The SPLIT WRITE TRANSFER feature makes it possible to input and transfer uninterrupted bit streams. Figure 6 shows a typical initiation sequence for SPLIT WRITE TRANSFER input cycles.

Like the SPLIT READ TRANSFER, the SPLIT WRITE TRANSFER cycle does not change the state of the SAM I/O buffers. Performing a normal WRITE TRANSFER cycle or PSUEDO WRITE TRANSFER cycle is required to set the Tap point and set the SAM I/O buffers to input mode.

The next step is to perform a SPLIT WRITE TRANSFER to enter the SPLIT SAM operating mode and enable the QSF output. Usually, the upper SAM is immediately trans-

ferred to the first destination row. The upper SAM may not yet contain valid data, but another write to the same row would normally occur after the next SPLIT WRITE TRANSFER cycle.

Once in the SPLIT TRANSFER operating mode, the QSF output will indicate which half of the SAM is currently accepting data. After QSF goes high, indicating that serial input has now switched to the upper SAM, the contents of the lower SAM may be transferred to any DRAM row. The cycle of checking for a change in QSF and then transferring the SAM half just filled can now be repeated. The next step on Figure 6 would be to wait for QSF to go low and then SPLIT WRITE TRANSFER the contents of the Upper SAM to row 0.

### **FUNCTIONAL TRUTH TABLE**

CODE	FUNCTION		RAS	FALLING	EDGE		CAS FALL	A0 -	- A8 <sup>1</sup>	DQ1 -	DQ4 <sup>2</sup>	REGIS	STERS
		CAS	TR/OE	ME / WE	DSF	SE	DSF	RAS	CAS	RAS	CAS <sup>3</sup>	MASK	COLOR
	DRAM OPERATIONS												
CBR	CAS-BEFORE-RAS REFRESH	0	Х	1	Х	х	х		x	-	×	×	х
ROR	RAS ONLY REFRESH	1	1	х	Х	×	T -	ROW	_	X	_	х	х
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	х	0	ROW	COLUMN	х	VALID	х	X
RWNM	NON-PERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	×	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	×
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	×	0	ROW	COLUMN	х	VALID DATA	USE	Х
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	х	1	ROW	COLUMN (A2 - A8)	Х	COLUMN	×	USE
BWNM	NON-PERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	х	1	ROW	COLUMN (A2 - A8)		COLUMN MASK	LOAD & USE	USE
виом	PERSISTENT (USE MASK REGISTER)	1	1	0	1	х	1	ROW	COLUMN	х	COLUMN	USE	USE
	REGISTER OPERATIONS												
LMR	LOAD MASK REGISTER	1	1	1	1	х	0	ROW⁴	х	х	WRITE MASK	LOAD	х
LCR	LOAD COLOR REGISTER	1	1	1	1	X	1	ROW <sup>4</sup>	х	×	COLOR DATA	х	LOAD
	TRANSFER OPERATIONS												
RT	DRAM-TO-SAM TRANSFER (READ TRANSFER)	1	0	1	0	Х	х	ROW	SSA <sup>5</sup> (TAP)	X	X	х	×
SRT	SPLIT DRAM-TO-SAM TRANSFER (SPLIT READ TRANSFER)	1	0	1	1	Х	х	ROW	SSA⁵ (TAP)	Х	х	Х	х
WT	SAM-TO-DRAM TRANSFER (WRITE TRANSFER)	1	0	0	0	0	X	ROW	SSA <sup>5</sup> (TAP)	Х	Х	Х	х
PWT	SERIAL INPUT MODE ENABLE (PSEUDO WRITE TRANSFER)	1	0	0	0	1	х	ROW⁴	SSA <sup>5</sup> (TAP)	Х	х	Х	х
SWT	SPLIT SAM-TO-DRAM TRANSFER WITH MASK (SPLIT WRITE TRANSFER)	1	0	0	1	Х	X	ROW	SSA <sup>5</sup> (TAP)	WRITE MASK	X	LOAD & USE	×

NOTES: 1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.

- 2. These columns show what must be present on the DQ1-DQ4 inputs when RAS falls and when CAS falls.
- On WRITE cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. similarly, on READ cycles, the output data is latched at the falling edge of CAS or TR/OE, whichever is later.
- 4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
- 5. SSA = SAM Starting Address or Tap Point. This is the first SAM location that the next SC cycle will access.



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### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V to +7.0V
Operating Temperature, Ta(Ambient)0°C to +70°C
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation1 Watt
Short Circuit Output Current

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \le T_{\Delta} \le 70^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1

### DC ELECTRICAL CHARACTERISTICS

(Notes 3, 4, 5) (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C, Vcc = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input (0V≤VIN≤Vcc, all other pins not under test = 0 volts).	lı.	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V≤Vouт≤Vcc).	loz	-10	10	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA)	Vон	2.4		V	
Output Low voltage (lout = 5mA)	Vol		0.4	v	1

### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As), DIN	Cıı		5	pF	2
Input Capacitance RAS, CAS, ME/WE, TR/OE, SC, SE, DSF	C <sub>12</sub>		7	pF	2
Output Capacitance Dout, QSF	Co		7	pF	2

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CURRENT DRAIN, SAM IN STANDBY (Notes 2, 3) (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C, Vcc = 5.0V  $\pm$  10%)

PARAMETER/CONDITION OF DRAM	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS=Cycling; Trc=Trc(MIN)).	lcc1		90	mA	3, 4
OPERATING CURRENT: PAGE-MODE (RAS=VIL, CAS=Cycling; TPC=TPC(MIN)).	lcc2		70	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS=CAS=VIH after 8 RAS cycles min).	lc c3		3	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current (RAS=CAS=Vcc-0.2V after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V).	lcc4		1	mA	
REFRESH CURRENT: RAS ONLY (RAS=Cycling; CAS=Vih).	lc c5		90	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS=Cycling).	lc ce		80	mA	3, 5
SAM/DRAM DATA TRANSFER	lcc7		90	mA	3, 4

# CURRENT DRAIN, SAM ACTIVE (tsc = MIN) (Notes 2, 3) (0°C $\leq$ T<sub>A</sub> $\leq$ 70°C, Vcc = 5.0V $\pm$ 10%)

PARAMETER/CONDITION OF DRAM	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS=Cycling; Trc=Trc(MIN)).	lcc8		115	mA	3, 4
OPERATING CURRENT: PAGE-MODE (RAS=VIL, CAS=Cycling; Tpc=Tpc(MIN)).	lc c9		95	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS=CAS=VIH after 8 RAS cycles min).	lcc10		30	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current (RAS=CAS=Vcc-0.2V after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V).	lcc11		25	mA	
REFRESH CURRENT: RAS ONLY (RAS=Cycling; CAS=VIH).	ICC12		115	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS=Cycling).	Icc13		105	mA	3, 5
SAM/DRAM DATA TRANSFER	lcc14		115	mA	3,4



# **DRAM TIMING PARAMETERS**

### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ( $0^{\circ}$ C  $\leq$  T<sub>A</sub>  $\leq$  +70 $^{\circ}$ C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS			-8	-	10	-1:	2		-15		L
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	160		190		220		260		ns	
READ-MODIFY-WRITE cycle time	tRWC	190		220		255		295		ns	
PAGE-MODE READ or WRITE	<sup>t</sup> PC	45		55		70		85		ns	
cycle time		1									
Access time from RAS	tRAC		80		100		120		150	ns	14
Access time from CAS	tCAC		20		25		30		45	ns	15
Access time from (TR)/OE	<sup>t</sup> OE		20		25		25		30	ns	
Access time from column address	<sup>t</sup> AA		40		50		60		70	ns	
Access time from CAS precharge	<sup>t</sup> CPA		40		50		65		75	ns	
RAS pulse width	tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
RAS pulse width (PAGE MODE)	<sup>t</sup> RASP	80	100,000	100	100,000	120	100,000	150	100,000	ns	
RAS hold time	t <sub>RSH</sub>	20		25		30		45		ns	
RAS precharge time	t <sub>RP</sub>	70		80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	20	10,000	25	10,000	30	10,000	45	10,000	ns	
CAS hold time	t <sub>CSH</sub>	80		100		120		150		ns	
CAS precharge time	t <sub>CPN</sub>	10		15		20		25		ns	16
CAS precharge time (PAGE MODE)	<sup>t</sup> CP	10		10		15		20		ns	
RAS to CAS delay time	tRCD	10	60	10	75	15	90	15	105	ns	17
CAS to RAS precharge time	t <sub>CRP</sub>	5		10		10		10		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	t <sub>RAH</sub>	10		10		15		15		ns	
RAS to column	tRAD	10	40	10	50	15	60	15	70	ns	18
address delay time											
Column address set-up time	tASC	0		0		0	}	0		ns	
Column address hold time	tCAH	15		15		20		25		ns	
Column address hold time (referenced to RAS)	<sup>t</sup> AR	50		60		70		80		ns	
Column address to RAS lead time	<sup>t</sup> RAL	40		50		60		70		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time (referenced to CAS)	tRCH	0		0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		0		ns	19
CAS to output in low-Z	tCLZ	5		5		5		5		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	20	0	25	0	25	0	30	ns	20
Output Disable	tOD		20		25		25		30	ns	1



# **DRAM TIMING PARAMETERS (Continued)**

### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C  $\leq$  T<sub>A</sub>  $\leq$  +70°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS		_	8		10	-12	2		-15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command set-up time	twcs	0		0		0		0		ns	21
Write command hold time	tWCH	15		20		25		30		ns	
Write command hold time (referenced to RAS)	tWCR	60		70		80		90		ns	
Write command pulse width	t <sub>WP</sub>	15		20		25		30		ns	
Write command to RAS lead time	t <sub>RWL</sub>	20		25		30		35		ns	
Write command to CAS lead time	tCWL	20		25		30		35		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		0		ns	22
Data-in hold time	t <sub>DH</sub>	15		15		20		25		ns	22
Data-in hold time (referenced to RAS)	t <sub>DHR</sub>	60		70		80		90		ns	
RAS to WE delay time	t <sub>RWD</sub>	100		120		150		185		ns	21
Column address to WE delay time	<sup>t</sup> AWD	60		80		100		120		ns	21
CAS to WE delay time	tCWD	50		65		75		85		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		8		8		8		8	ms	
RAS to CAS Precharge time	t <sub>RPC</sub>	0		0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	tCHR	15		20		25		30		ns	5
ME/WE to RAS set-up time	twsR	0		0		0		0		ns	
ME/WE to RAS hold time	t <sub>RWH</sub>	10		10		10		15		ns	
Mask Data to RAS set-up time	t <sub>MS</sub>	0		0		0		0		ns	
Mask Data to RAS hold time	t <sub>MH</sub>	10		15		15		20		ns	

# MICHON

#### NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and  $V_{CC} = 5V$ .
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- An initial pause of 100μs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIL and VIH) in a monotonic manner.
- 11. If  $\overline{\text{CAS}}$  = V<sub>IH</sub>, DRAM data output (DQ1-DQ4) is high impedance.
- 12. If CAS = VIL, DRAM data output (DQ1-DQ4) may contain data from the last valid READ cycle.
- 13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If  $\overline{\text{CAS}}$  is low at the falling edge of  $\overline{\text{RAS}}$ , DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for  $^{\text{t}}\text{CPN}$ .
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that

- <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- 19. Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle
- 20. tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 21. <sup>t</sup>WCS, <sup>t</sup>RWD, <sup>t</sup>AWD and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), <sup>t</sup>AWD ≥ <sup>t</sup>AWD (min) and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to Vih) is indeterminate.
- 22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles and  $\overline{\text{WE}/\text{WE}}$  leading edge in late WRITE or READ-WRITE cycles.
- 23. During a READ cycle, if TR/OE is LOW then taken HIGH DOUT goes open.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case WE/WE = LOW and TR/OE=HIGH.
- 25. SAM output timing is measured with a load equivalent to 2TTL gate and 50pF.
- 26. TRANSFER command mean that  $\overline{TR}/\overline{OE}$  is low when RAS goes low.
- 27. NON-TRANSFER command means that  $\overline{TR}/\overline{OE}$  is high when  $\overline{RAS}$  goes low.

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# TRANSFER AND MODE CONTROL TIMING PARAMETERS ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes 3, 4, 5, 17, 25) (0° C $\leq$ T<sub>A</sub> $\leq$ + 70°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS	-8		-10		-12		-15		Γ		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
TRANSFER Command to RAS Set Up Time	<sup>t</sup> TLS	0		0		0		0		ns	26
Transfer Command to RAS Hold Time	t <sub>TLH</sub>	10	10,000	10	10,000	10	10,000	15	10,000	ns	
TRANSFER Command to RAS Hold Time (REAL-TIME READ TRANSFER only)	<sup>t</sup> RTH	70	10,000	80	10,000	90	10,000	100	10,000	ns	26
TRANSFER Command to CAS Hold Time (REAL-TIME READ TRANSFER only)	<sup>t</sup> CTH	20		25		30		35		ns	26
TRANFER Command to Column Address Hold Time (For REAL TIME READ TRANSFER only)	<sup>t</sup> ATH	25		30		35		40		ns	
TRANSFER Command to SC Lead Time	t <sub>TSL</sub>	5		5		5		10		ns	26
TRANSFER Command to RAS Lead Time	<sup>t</sup> TRL	10		10		10		10		ns	26
TRANSFER Command to RAS Delay Time	<sup>t</sup> TRD	15		15		15		20		ns	26
TRANSFER Command to CAS Time	<sup>t</sup> TCL	10		10		10		10		ns	26
TRANSFER Command to CAS Delay Time	<sup>t</sup> TCD	15		15		15		20		ns	26
First SC edge to TRANSFER Command Delay Time	<sup>t</sup> TSD	10		10		10		20		ns	26
Serial Output Buffer Turn Off Delay from RAS	<sup>t</sup> SDZ	10	35	10	40	10	50	10	60	ns	
SC to RAS Set Up Time	t <sub>SRS</sub>	30		35		40		45		ns	
RAS to SC Delay Time	<sup>t</sup> SRD	20		25		30		35	1	ns	
Serial Data Input to SE Delay Time	t <sub>SZE</sub>	0		0		0		0		ns	
RAS to SD Buffer Turn On Time	t <sub>SRO</sub>	0		0		0		0		ns	
Serial Data Input Delay from RAS	tSDD	45		50		55		60		ns	
Serial Data Input to RAS Delay Time	t <sub>SZS</sub>	0		0		0		0		ns	
Serial Input Mode Enable (SE) to RAS Set Up Time	<sup>t</sup> ESR	0		0		0		0		ns	
Serial Input Mode Enable (SE) to RAS Hold Time	<sup>t</sup> REH	10		10		10		15		ns	
NON-TRANSFER Command to RAS Set Up Time	t <sub>YS</sub>	0		0		0		0		ns	27
NON-TRANSFER Command to RAS Hold Time	tYH	10		10		10		10		ns	27
DSF to RAS Set Up Time	<sup>t</sup> FSR	0		0		0		0		ns	
DSF to RAS Hold Time	tRFH	10	1	15		15		20		ns	
DSF to RAS Hold Time	t <sub>FHR</sub>	60		65		70		75		ns	
DSF to CAS Set-up Time	<sup>t</sup> FSC	0		0		0		0		ns	
DSF to CAS Hold Time	<sup>t</sup> CFH	15		20		20		25		ns	
SC to QSF Delay Time	tsQD		25		30		35		40	ns	
SPLIT TRANSFER Set Up Time	tSTS	30		35		40		45		ns	
SPLIT TRANSFER Hold Time	<sup>t</sup> STH	30		35		40		45	1	ns	
TR/OE to QSF Delay Time	<sup>t</sup> TQD		25		30		35		40	ns	
CAS to QSF Delay Time	tCQD		35		40		45		50	ns	1



### **SAM TIMING PARAMETERS**

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes 3, 4, 5, 17, 25) (0° C $\leq$ T<sub>A</sub> $\leq$ + 70°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Serial Clock Cycle Time	tsc	25		30		35		40		ns	
Access Time from SC	t <sub>SAC</sub>		25		30		35		40	ns	
SC Precharge Time (SC Low Time)	<sup>t</sup> SP	10		10		12		15		ns	
SC Pulse Width (SC High Time)	t <sub>SAS</sub>	10		10		12		15		ns	
Access Time from SE	t <sub>SEA</sub>		20		25		30		40	ns	
SE Precharge Time	t <sub>SEP</sub>	15		15		15		20		ns	
SE Pulse Width	<sup>t</sup> SE	15		15		15		20		ns	
Serial Data Out Hold Time after SC High	<sup>t</sup> soH	5		10		10		10		ns	
Serial Output Buffer Turn Off Delay from SE	<sup>t</sup> SEZ	0	15	0	15	0	25	0	30	ns	
Serial Data in Set Up Time	t <sub>SDS</sub>	0		0		0		0		ns	
Serial Data in Hold Time	<sup>t</sup> SDH	20		20		20		25			
SERIAL INPUT (Write) Enable Set Up Time	tsws	0		0		0		0		ns	
SERIAL INPUT (Write) Enable Hold Time	<sup>t</sup> swH	25		30		35		45		ns	
SERIAL INPUT (Write) Disable Set Up Time	tswis	0		0		0		0		ns	
SERIAL INPUT (Write) Disable Hold Time	<sup>t</sup> swiH	25		30		35		45		ns	

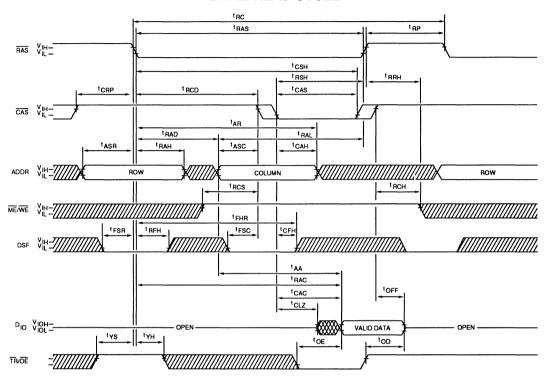


# WRITE CYCLE FUNCTION TABLE

		LO	GIC STATE	S				
	RAS Falling Edge			CAS Fall	ing Edge	FUNCTION		
M	A IE/WE	-   -		D E DSF DQ (Input)				
	1	0	Х	0	DRAM Data	Normal DRAM WRITE (or READ)		
	0	0	Write Mask	0	DRAM Data (Masked)	Non-Persistent (Load and Use) Masked Write to DRAM		
	0	1	Х	0	DRAM Data (Masked)	Persistent (Use Register) Masked Write to DRAM		
	1	0	Х	1	Column Mask	Block Write to DRAM (No Data Mask)		
	0	0	Write Mask	1	Column Mask	Non-Persistent (Load and Use) Masked Block Write to DRAM		
	0	1	Х	1	Column Mask	Persistent (Use Register) Masked Block Write to DRAM		
	1	1	Х	0	Write Mask	Load Mask Register		
	1	1	Х	1	Color Data	Load Color Register		

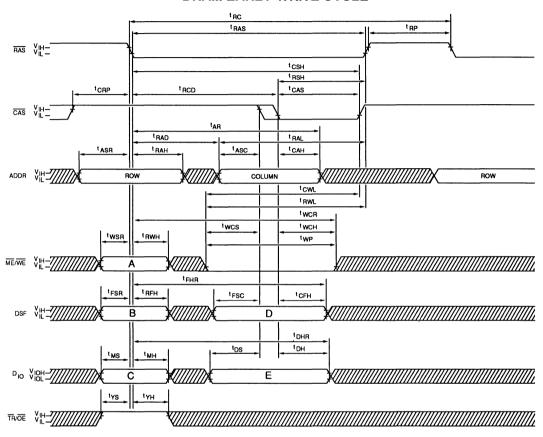


### **DRAM READ CYCLE**



# MICHON

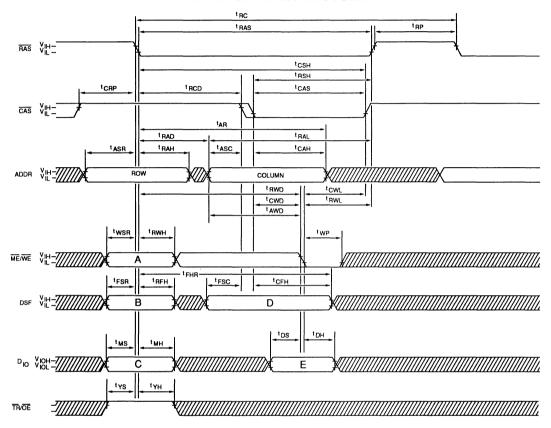
### **DRAM EARLY-WRITE CYCLE**



DON'T CARE
UNDEFINED

**NOTE:** The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

### **DRAM LATE-WRITE CYCLE**

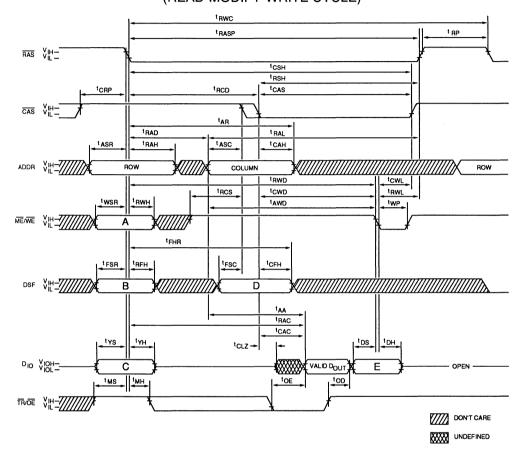


DON'T CARE
UNDEFINED

**NOTE:** The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

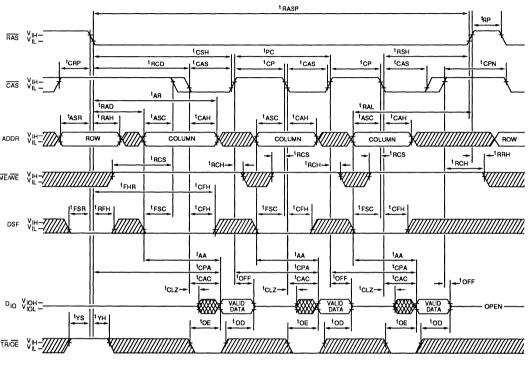
# MICRON

# **DRAM READ-WRITE CYCLE** (READ-MODIFY-WRITE CYCLE)



**NOTE:** The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

### DRAM PAGE-MODE READ CYCLE

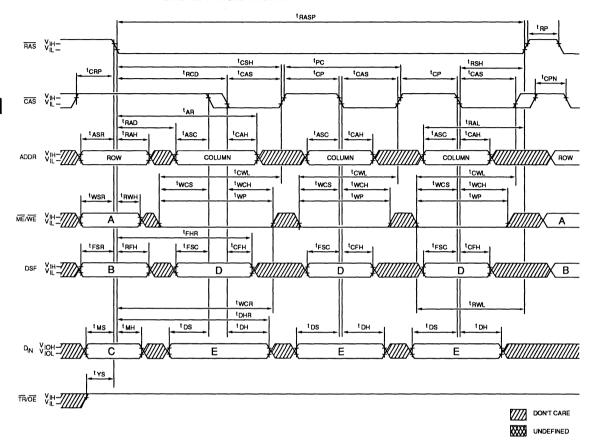


DON'T CARE
UNDEFINED

**Note1:** WRITE cycles or READ-MODIFY-WRITE cycles can be mixed with READ cycles while in PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.

# MICRON

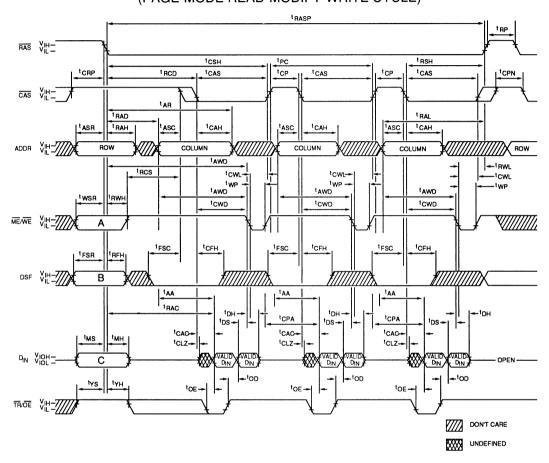
### DRAM PAGE-MODE EARLY-WRITE CYCLE



**Note1:** READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in PAGE-MODE.

**Note 2:** The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

# **DRAM PAGE-MODE READ-WRITE CYCLE**(PAGE-MODE READ-MODIFY-WRITE CYCLE)

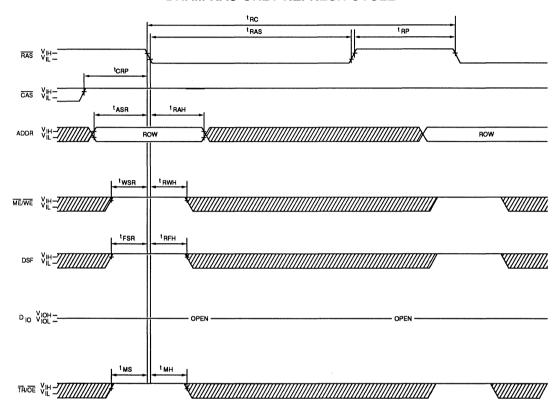


**Note1:** READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in PAGE- MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.

**Note 2:** The Logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

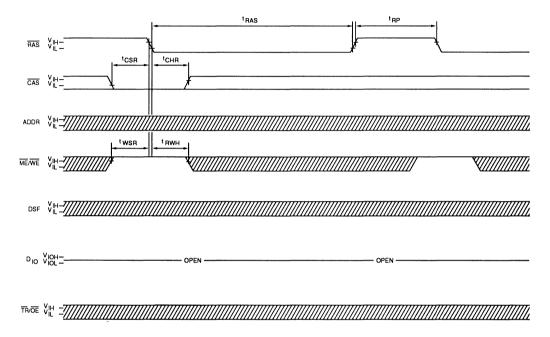
MICRON

# DRAM RAS ONLY REFRESH CYCLE

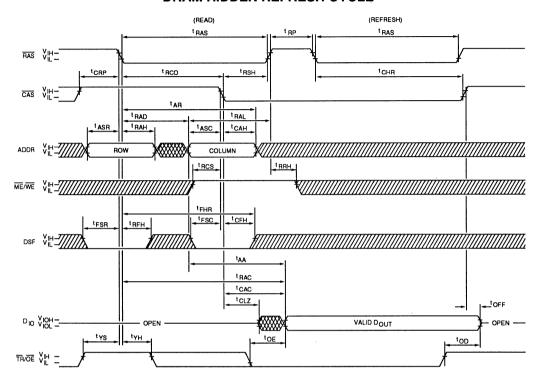




# **CAS-BEFORE-RAS REFRESH CYCLE**



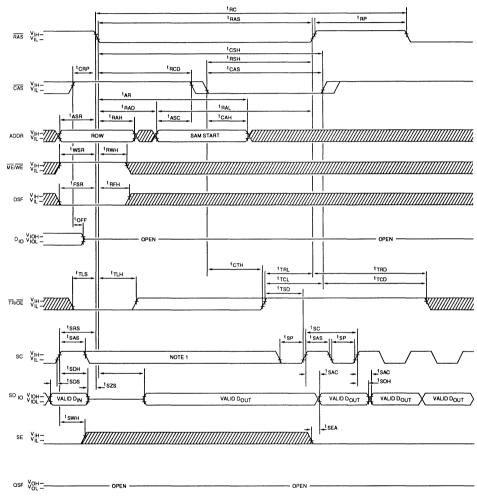
### **DRAM HIDDEN REFRESH CYCLE**





# READ TRANSFER (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL INPUT mode.)



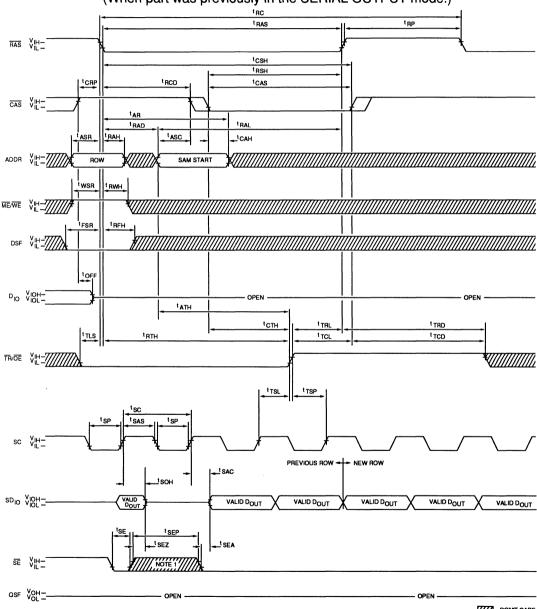
NOTE 1: There must be no rising edges on the SC input during this time period.

Note 1: There must be no rising edges on the SC input during this time period.

# MICHON

# REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode.)

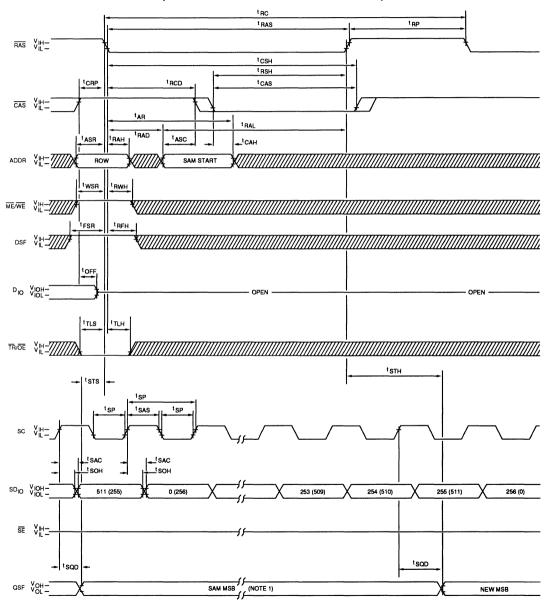


DON'T CARE

UNDEFINED

Note 1: If  $\overline{SE}$  pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

# SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

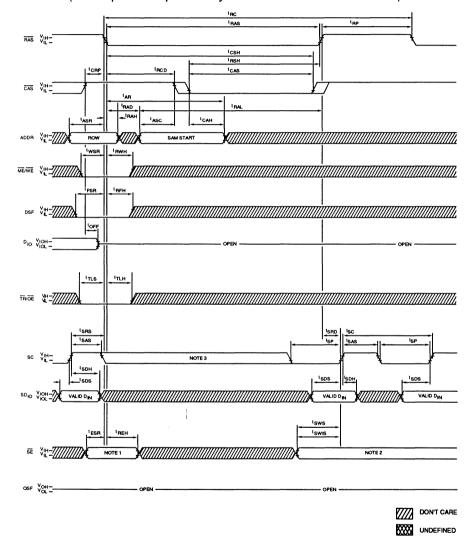


Note 1: QSF = 0 when the Lower SAM (bits 0–255) is being accessed. QSF = 1 when the Upper SAM (bits 256–511) is being accessed.



# WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was perviously in the SERIAL INPUT mode.)



NOTE 1: If SE is LOW, the SAM data will be transferred to the DRAM.

If SE is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless

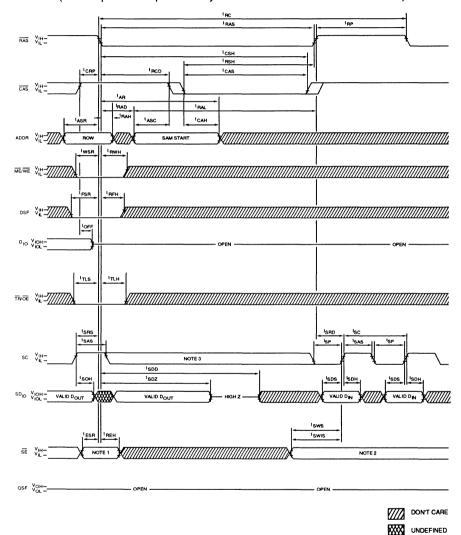
of SE.

NOTE 3: There must be no rising edges on the SC input during this time period.



# WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode.)



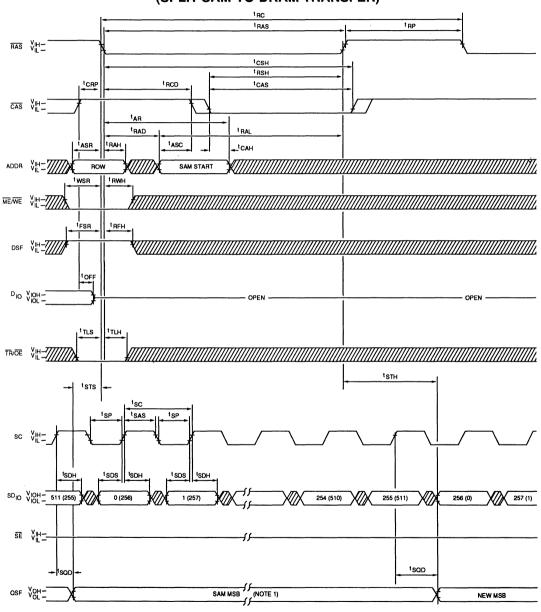
NOTE 1: If  $\overline{SE}$  is LOW, the SAM data will be transferred to the DRAM.

If SE is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless of SE.

NOTE 3: There must be no rising edges on the SC input during this time period.

## SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER)

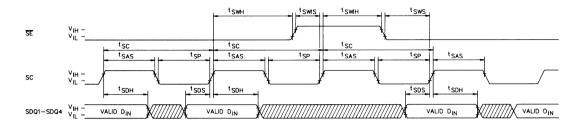


Note 1: QSF = 0 when the Lower SAM (bits 0–255) is being accessed. QSF = 1 when the Upper SAM (bits 256–511) is being accessed. DON'T CARE

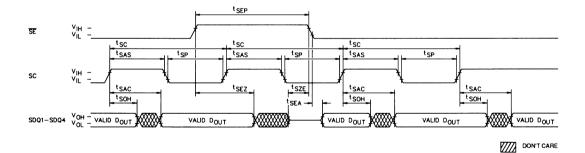
UNDEFINED

UNDEFINED

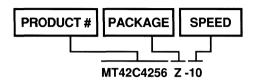
#### **SAM SERIAL INPUT**



#### **SAM SERIAL OUTPUT**



#### **ORDER INFORMATION**



The Micron MT42C4256 is functionally equivalent to other manufacturer's products meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the high speed,

low power CMOS double poly, single metal process. Micron's QUALITY ASSURED policy is to offer prompt, accurate, and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply, temperature, and refresh range than specified. Each unit receives accelerated burn-in and and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

## **SECTION GUIDE**

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#### **SRAM PRODUCT SELECTION GUIDE**

Memory	Control	Part	Access	1	Package and I	ns			
Configuration	Functions	Number	Time (ns)	PDIP	SOJ	CDIP	CLCC	Process	Page
2K x 8	CE & OE	MT5C1608	12 to 35	24	24	24	24	CMOS	4-3
4K x 4	CE only	MT5C1604	12 to 35	20	24	20	20	CMOS	4-11
4K x 4	CE & OE	MT5C1605	12 to 35	22	24	22	22	CMOS	4-19
4K x 4	Separate I/O	MT5C1606	12 to 35	24	24	24	28	CMOS	4-27
4K x 4	Separate I/O HI-Z	MT5C1607	12 to 35	24	24	24	28	CMOS	4-27
4K x 16	CE, OE & ALE	MT5C6416	25 to 45	40	-	40	-	CMOS	4-35
8K x 8	CE1, CE2 & OE	MT5C6408	12 to 35	28	28	28	32	CMOS	4-37
16K x 1	CE only	MT5C1601	12 to 35	20	24	20	20	CMOS	4-45
16K x 4	CE only	MT5C6404	12 to 35	22	24	22	22	CMOS	4-53
16K x 4	CE & OE	MT5C6405	12 to 35	24	24	24	28	CMOS	4-61
16K x 4	Cache Tag	MT5C6405T	12 to 35	24	24	24	28	CMOS	4-69
16K x 4	Separate I/O, CE1, CE2	MT5C6406	12 to 35	28	28	28	28	CMOS	4-77
16K x 4	Separate I/O HI-Z	MT5C6407	12 to 35	28	28	28	28	CMOS	4-77
32K x 8	CE & OE	MT5C2568	25 to 45	28	28	28	32	CMOS	4-93
64K x 1	CE only	MT5C6401	12 to 35	22	24	22	22	CMOS	4-85
64K x 4	CE only	MT5C2564	25 to 45	24	24	24	28	CMOS	4-101
64K x 4	CE & OE	MT5C2565	25 to 45	28	28	28	28	CMOS	4-109
128K x 8	CE & OE	MT5C1008	25 to 45	28	-	28	-	CMOS	4-125
256K x 1	CE only	MT5C2561	25 to 45	24	24	24	28	CMOS	4-117
256K x 4	CE & OE	MT5C1005	25 to 45	28	-	28	-	CMOS	4-127
1MEG x 1	CE & OE	MT5C1001	25 to 45	28	-	28	-	CMOS	4-129

## **SRAM**

## 2K x 8 SRAM

#### **FEATURES**

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC (28 pin)	EC
Two Volt Data Retention	L

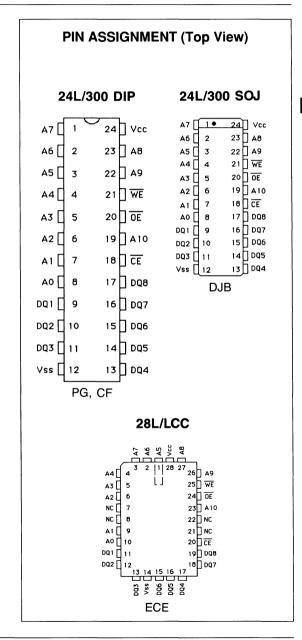
#### GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

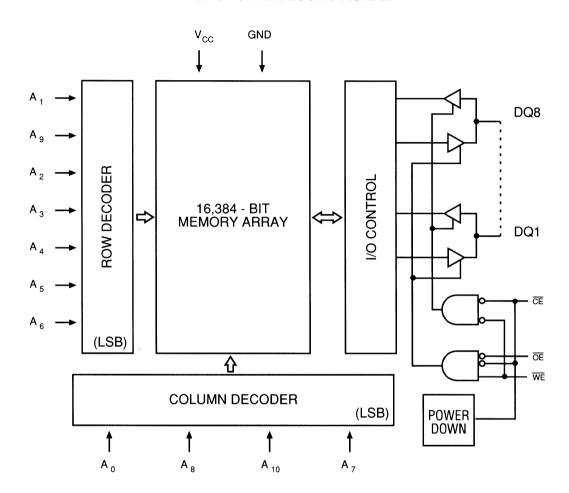
For flexibility in high speed memory applications, Micron offers chip enable  $(\overline{CE})$  on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.



#### **FUNCTIONAL BLOCK DIAGRAM**



#### **TRUTH TABLE**

MODE	ŌĒ	CE	WE	DQ	POWER
STANDBY	Х	Н	Х	HIGH Z	STANDBY
READ	L	L	Н	DOUT	ACTIVE
READ	Н	L	Н	HIGH Z	ACTIVE
WRITE	Х	L	L	DIN	ACTIVE

## MICRON

#### ABSOLUTE MAXIMUM RATINGS\*

Voltage on Vcc supply relative to Vss1.0V to +7.0V
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation
Short Circuit Output Current50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 $(0^{\circ}C \leq T_{\mbox{\scriptsize A}} \leq 70^{\circ}C, \ Vcc = 5.0V \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		Vih	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VCC	1Lı	-10	10	μА	
Output Leakage Current	Output(s) Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -2.0mA	Vон	2.4		V	1
Output Low Voltage	loL = 4.2mA	Vol		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	CE ≤ VIL, Vcc = Max., Outputs Open	lcc	140	130	120	110	100	100	mA	3
	CE ≥ ViH, Vcc = Max	Is <sub>B1</sub>	60	50	45	40	40	40	mA	
Power Supply Current: Standby	$\overline{\text{CE}} \ge \text{Vcc} - 0.2$ , $\text{Vcc} = \text{Max}$ . $\text{ViL} \le \text{Vss} + 0.2$ , $\text{ViH} \ge \text{Vcc} - 0.2$ , $\text{f} = 0$	IsB2	5	5	5	5	5	5	mA	

#### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Cı		7	pF	4
Output Capacitance	Vcc = 5V	Co		7	pF	4



#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

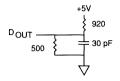
(Note 5) (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C, Vcc = 5V  $\pm$  10%)

DESCRIPTION		-1	12	-1	5	-20		-25		-30		-35			
DESCRIPTION	SYM	MIN	MAX	UNITS	NOTES										
READ Cycle															
READ cycle time	<sup>t</sup> RC	12		15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		12		15		20		25		30		35	ns	
Chip enable access time	t <sub>ACE</sub>		12		15		20		25		30		35	ns	
Output hold from access change	t <sub>OH</sub>	3		3		3		3		3		3		ns	
Chip enable to output in low Z	<sup>t</sup> LZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		12		15		20		25		30		35	ns	
Output enable access time	<sup>t</sup> AOE		10		12		15		15		20		20	ns	
Output enable to output in low Z	t <sub>LZOE</sub>	0		0		0		0		0		0		ns	
Output disable to output in high Z	<sup>t</sup> HZOE		10		10		15		15		20		20	ns	6
WRITE Cycle									,						
WRITE cycle time	t <sub>WC</sub>	12		15		20		25		30		35		ns	
Chip enable to end of write	tcw	10		12		15		20		25		30		ns	
Address valid to end of write	<sup>t</sup> AW	12		15		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		0		ns	
Address hold from end of write	t <sub>AH</sub>	0		0		0		0		0		0		ns	
Write pulse width	t <sub>WP</sub>	10		12		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		10		12		15		15		15		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		0		ns	
Write disable to output in low Z	t <sub>LZWE</sub>	0		0		0		0		0		0		ns	
Write enable to output in high Z	t <sub>HZWE</sub>	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

## MICHON

#### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2



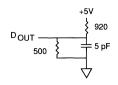


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

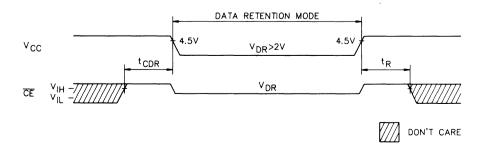
#### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- 6. <sup>t</sup>HZCE, <sup>t</sup>HZWE and <sup>t</sup>HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8.  $\overline{\text{WE}}$  is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

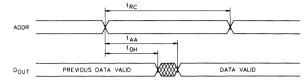
#### **DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)**

SYMBOL	PARAMETER	TEST CONDITI	ONS	MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2			٧
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V) Vin ≥ (Vcc - 0.2V)			95	500	μΑ
		$or \le 0.2V$	Vcc=3v		350	750	μΑ
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

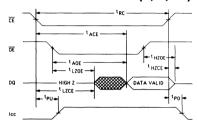
#### LOW Vcc DATA RETENTION WAVEFORM



#### **READ CYCLE NO. 1 (8, 9)**

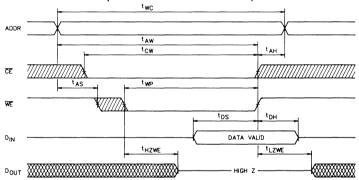


#### **READ CYCLE NO. 2 (7, 8, 10)**



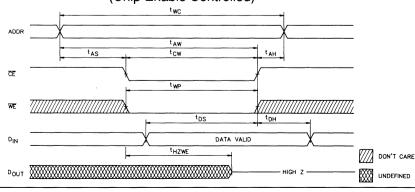
#### **WRITE CYCLE NO. 1**

(Write Enable Controlled)



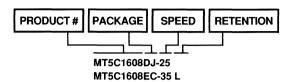
#### **WRITE CYCLE NO. 2**

(Chip Enable Controlled)





#### ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled

in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.



## **SRAM**

## 4K x 4 SRAM

#### **FEATURES**

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V ( $\pm 10\%$ ) power supply
- Easy memory expansion with  $\overline{\text{CE}}$  option
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
Two Volt Data Retention	L

#### GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

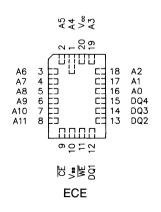
For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

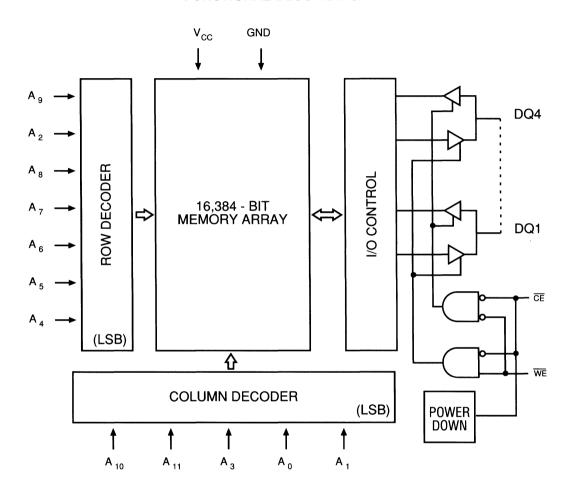
All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

#### PIN ASSIGNMENT (Top View) 20L/300 DIP 24L/300 SQJ 24 23 22 20 Vcc Vcc Α3 2345678910 11 Α6 Α2 Α5 19 Α3 22 µ A2 21 □ A1 20 □ A0 19 □ NC 18 □ NC 17 □ DQ4 Α7 Α8 Α6 18 Α2 Α9 Α7 17 Α1 NC A10 A11 CE NC 16 DQ3 Α8 16 Α0 15 D DQ2 14 D DQ1 13 D WE Α9 15 DQ4 d 11 A10 14 DQ3 DJB DQ2 A11 13 CE 12 DQ1 Vss U 11 D WE PE, CD

#### 20L/LCC



#### **FUNCTIONAL BLOCK DIAGRAM**



#### **TRUTH TABLE**

MODE	CE	WE	DQ	POWER
STANDBY	Н	Х	HIGH Z	STANDBY
READ	L	Н	DOUT	ACTIVE
WRITE	L	L	DIN	ACTIVE

## MICRON

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vs	s1.0V to +7.0V
Storage Temperature (Ceramic)	65°C to +150°C
Storage Temperature (Plastic)	55°C to +150°C
Power Dissipation	1 Wat
Short Circuit Output Current	50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{\Delta} \leq 70^{\circ}C,~Vcc = 5.0V \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Input High (Logic 1) Voltage		2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ Vin ≤ Vcc	ILı	-10	10	μΑ	
Output Leakage Current	Output(s) Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	<b>V</b> он	2.4		V	1
Output Low Voltage	loL = 8.0mA	Vol		0.4	V	1

					M	AX				
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	CE ≤ VIL, Vcc = Max., Outputs Open	lcc	140	130	120	110	100	100	mA	3
	CE ≥ VIH, Vcc = Max	Is <sub>B</sub> 1	60	50	45	40	40	40	mA	
Power Supply Current: Standby	CE ≥ Vcc - 0.2, Vcc = Max.         VIL ≤ Vss + 0.2, f = 0         VIH ≥ Vcc - 0.2	IsB2	5	5	5	5	5	5	mA	

#### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Ci		7	pF	4
Output Capacitance	Vcc = 5V	Со		7	pF	4



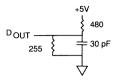
#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(Note 5) (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C, Vcc = 5V  $\pm$  10%)

DESCRIPTION		-1	12	-1	15	-2	20	-2	25	-3	80	-3	35		
DESCRIPTION	SYM	MIN	MAX	UNITS	NOTES										
READ Cycle															
READ cycle time	<sup>t</sup> RC	12		15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		12		15		20		25		30		35	ns	
Chip enable access time	<sup>t</sup> ACE		12		15		20		25		30		35	ns	
Output hold from access change	t <sub>OH</sub>	3		3		3		3		3		3		ns	
Chip enable to output in low Z	<sup>t</sup> LZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		0		ns	
Chip disable to power down time	<sup>t</sup> PD		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	twc	12		15		20		25		30		35		ns	
Chip enable to end of write	tcw	10		12		15		20		25		30		ns	
Address valid to end of write	<sup>t</sup> AW	12		15		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		0		ns	
Address hold from end of write	t <sub>AH</sub>	0		0		0		0		0		0		ns	
Write pulse width	<sup>t</sup> WP	10		12		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		10		12		15		15		17		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		0		ns	
Write disable to output in low Z	t <sub>LZWE</sub>	0		0		0		0		0		0		ns	
Write enable to output in high Z	<sup>t</sup> HZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

#### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	
Input timing reference levels	
Output reference levels	1.5V
Output load	See figures 1 and 2



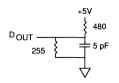


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

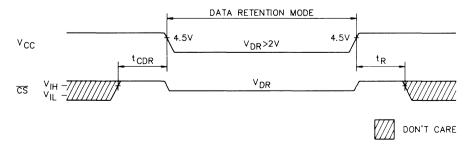
#### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- tHZCE and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8.  $\overline{\text{WE}}$  is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

#### DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

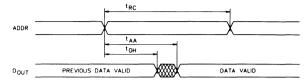
SYMBOL	PARAMETER	TEST CONDITI	ONS	MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2			٧
Iccdr	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V)		_	95	500	μА
		Vin ≥ (Vc'c - 0.2V) or ≤ 0.2V	Vcc=3v	_	350	750	μΑ
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time		•	0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

#### LOW Vcc DATA RETENTION WAVEFORM

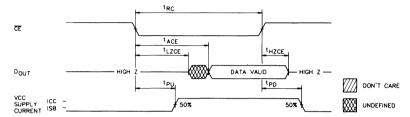




#### **READ CYCLE NO. 1 (8, 9)**

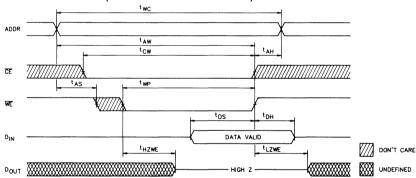


#### **READ CYCLE NO. 2 (7, 8, 10)**



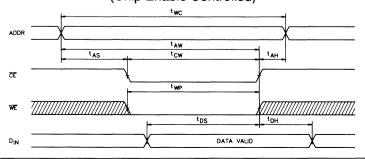
#### WRITE CYCLE NO. 1

(Write Enable Controlled)



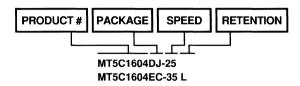
#### **WRITE CYCLE NO. 2**

(Chip Enable Controlled)





#### ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled

in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

· · · · · · · · · · · · · · · · · · ·		

## **SRAM**

## 4K x 4 SRAM

WITH OUTPUT ENABLE

#### **FEATURES**

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  options
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	С
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
Two Volt Data Retention	L

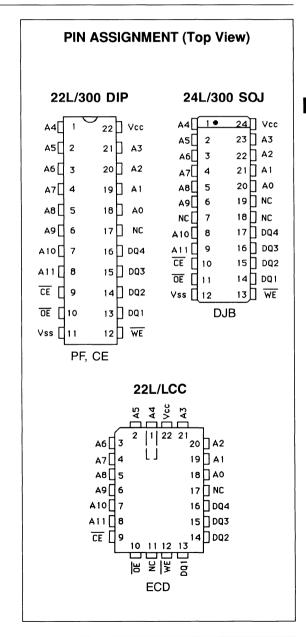
#### **GENERAL DESCRIPTION**

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

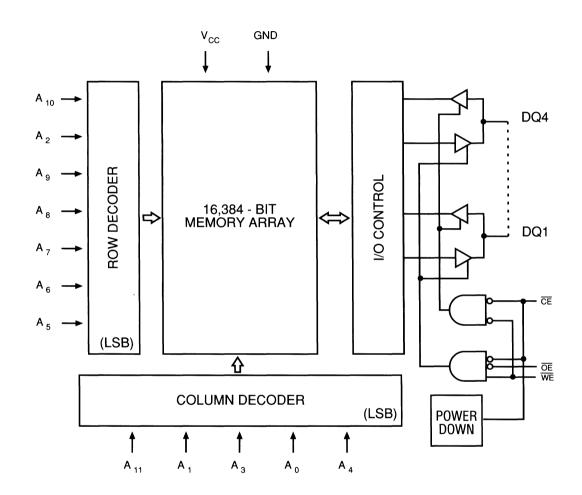
For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.



#### **FUNCTIONAL BLOCK DIAGRAM**



#### **TRUTH TABLE**

MODE	ŌĒ	CE	WE	DQ	POWER
STANDBY	Х	Н	Х	HIGH Z	STANDBY
READ	L	L	Н	DOUT	ACTIVE
READ	Н	L	Н	HIGH Z	ACTIVE
WRITE	Х	L	L	DIN	ACTIVE



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on VCC supply relative to Vss	1.0V to +7.0V
Storage Temperature (Ceramic)	65°C to +150°C
Storage Temperature (Plastic)	55°C to +150°C
Power Dissipation	1 Watt
Short Circuit Output Current	50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 $(0^{\circ}C \le T_{\Delta} \le 70^{\circ}C, Vcc = 5.0V \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		Vih	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VCC	ILı	-10	10	μА	
Output Leakage Current	Output(s) Disabled, 0V ≤ Vout ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	lон = -4.0mA	Vон	2.4		V	1
Output Low Voltage	loL = 8.0mA	Vol		0.4	٧	1

					М	AX				
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	CE ≤ VIL, Vcc = Max., Outputs Open	lcc	140	130	120	110	100	100	mA	3
	CE ≥ VIH, Vcc = Max	IsB1	60	50	45	40	40	40	mA	
Power Supply Current: Standby	$\overline{CE} \ge V_{CC} - 0.2$ , $V_{CC} = Max$ . $V_{IL} \le V_{SS} + 0.2$ , $f = 0$ $V_{IH} \ge V_{CC} - 0.2$	ISB2	5	5	5	5	5	5	mA	

#### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Cı		7	pF	4
Output Capacitance	Vcc = 5V	Co		7	pF	4

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (Note 5) (0°C $\leq$ T $_{A}$ $\leq$ 70°C, Vcc = 5V $\pm$ 10%)

DESCRIPTION			12	-1	5	-2	20	-2	25	-30 -35					
DESCRIPTION	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	<sup>t</sup> RC	12		15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		12		15		20		25		30		35	ns	
Chip enable access time	t <sub>ACE</sub>		12		15		20		25		30		35	ns	
Output hold from access change	t <sub>OH</sub>	3		3		3		3		3		3		ns	
Chip enable to output in low, Z	<sup>t</sup> LZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		12		15		20		25		30		35	ns	
Output enable access time	t <sub>AOE</sub>		10		12		15		15		20		20	ns	
Output enable to output in low Z	<sup>t</sup> LZOE	0		0		0		0		0		0		ns	
Output disable to output in high Z	<sup>t</sup> HZOE		10		10		15		15		20		20	ns	6
WRITE Cycle															
WRITE cycle time	twc	12		15		20		25		30		35		ns	
Chip enable to end of write	tcw	12		15		15		20		25		30		ns	
Address valid to end of write	<sup>t</sup> AW	10		12		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	0		0		0		0		0		0		ns	
Write pulse width	t <sub>WP</sub>	10		12		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		10		12		15		15		15		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		0		ns	
Write disable to output in low Z	<sup>t</sup> LZWE	0		0		0		0		0		0		ns	
Write enable to output in high Z	<sup>t</sup> HZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

Input pulse levels	Vss to 3.0V
Input rise and fall times	
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

# DOUT 480 255 30 pF

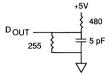


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

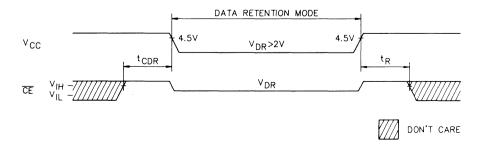
#### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- 6. <sup>t</sup>HZCE, <sup>t</sup>HZWE and <sup>t</sup>HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8. WE is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

#### DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

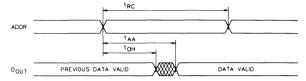
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2		_	٧
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V) Vin ≥ (Vcc - 0.2V)			95	500	μΑ
i		, ,	Vcc=3v		350	750	μΑ
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

#### LOW Vcc DATA RETENTION WAVEFORM

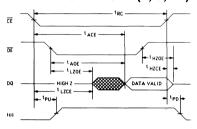


DON'T CARE

#### **READ CYCLE NO. 1 (8, 9)**

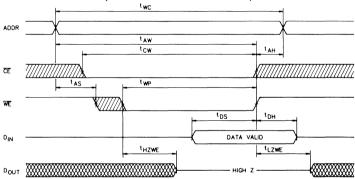


#### **READ CYCLE NO. 2 (7, 8, 10)**



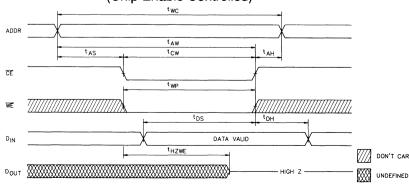
#### **WRITE CYCLE NO. 1**

(Write Enable Controlled)



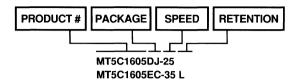
#### **WRITE CYCLE NO. 2**

(Chip Enable Controlled)





#### ORDER INFORMATION



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in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

	* 1 2 2 2	

## **SRAM**

## 4K x 4 SRAM

WITH SEPARATE INPUTS AND OUTPUTS

#### **FEATURES**

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with CE option
- All inputs and outputs are TTL compatible
- MT5C1606 output tracks input during WRITE
- MT5C1607 output high impedance during WRITE

OPTIONS	MARKING
Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
Two Volt Data Retention	L

#### **GENERAL DESCRIPTION**

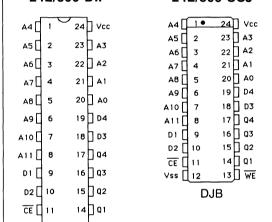
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 4 configuration features separate data input and output.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

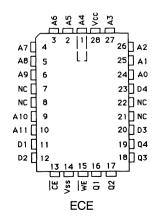
# PIN ASSIGNMENT (Top View) 24L/300 DIP 24L/300 SOJ



#### 28L/LCC

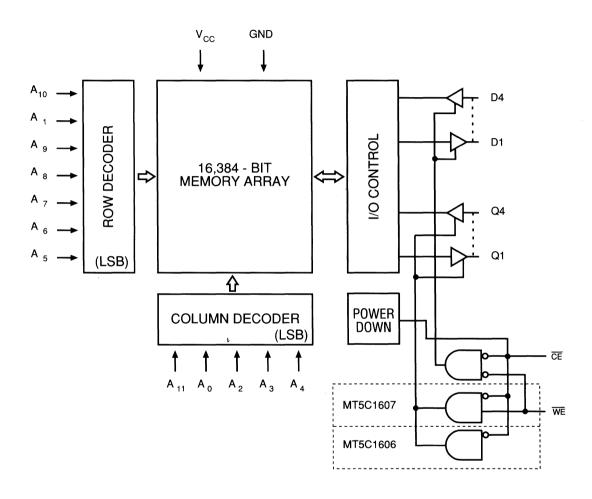
13 WE

PG. CF



Vss ∏ 12

#### **FUNCTIONAL BLOCK DIAGRAM**



#### **TRUTH TABLE**

MODE	CE	WE	DQ	POWER
STANDBY	Н	Х	HIGH Z	STANDBY
READ	L	н	DOUT	ACTIVE
WRITE (1)	L	L	HIGH Z	ACTIVE
WRITE (2)	L	L	DIN	ACTIVE

NOTES:

1. MT5C1607 ONLY

2. MT5C1606 ONLY



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V to +7.0V
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation 1 Wat
Short Circuit Output Current50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{\mbox{\scriptsize A}} \leq 70^{\circ}C, \ \mbox{Vcc} = 5.0 \mbox{\scriptsize V} \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		ViH	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ Vcc	ILı	-10	10	μΑ	
Output Leakage Current Output(s) Disabled 0V ≤ Vouт ≤ Voc		ILo	-10	10	μА	
Output High Voltage IoH = -4.0mA		<b>V</b> oн	2.4		V	1
Output Low Voltage	loL = 8.0mA	Vol		0.4	V	1

		MAX								
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	CE ≤ VIL, Vcc = Max., Outputs Open	lcc	140	130	120	110	100	100	mA	3
	CE ≥ ViH, Vcc = Max	Is <sub>B1</sub>	60	50	45	40	40	40	mA	
Power Supply Current: Standby	CE ≥ Vcc - 0.2, Vcc = Max.         VIL ≤ Vss + 0.2, f = 0         VIH ≥ Vcc - 0.2	IsB2	5	5	5	5	5	5	mA	

#### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Cı		7	pF	4
Output Capacitance	Vcc = 5V	Со		7	pF	4

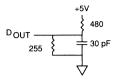


# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (Note 5) (0°C $\leq$ T $_{A}$ $\leq$ 70°C, Vcc = 5V $\pm$ 10%)

DESCRIPTION		1	2	-1	5	-2	20	-2	!5	9	10	-3	35		
DESCRIPTION	SYM	MIN	MAX	UNITS	NOTES										
READ Cycle															
READ cycle time	<sup>t</sup> RC	12		15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		12		15		20		25		30		35	ns	
Chip enable access time	t <sub>ACE</sub>		12		15		20		25		30		35	ns	
Output hold from access change	<sup>t</sup> OH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	<sup>t</sup> LZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	<sup>t</sup> PU	0		0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	twc	12		15		20		25		30		35		ns	
Chip enable to end of write	tcw	10		12		15		20		25		30		ns	
Address valid to end of write	<sup>t</sup> AW	12		15		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	0		0		0		0		0		0		ns	
Write pulse width	<sup>t</sup> WP	10		12		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		10		12		15		15		15		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		0		ns	
Write disable to output in low Z	t <sub>LZWE</sub>	0		0		0		.0		0		0		ns	
Write enable to output valid	t <sub>AWE</sub>		12		15		20		25		30		35	ns	
Data valid to output valid	<sup>t</sup> ADV		12		15		20		25		30		35	ns	

#### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	s1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2



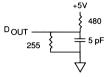


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

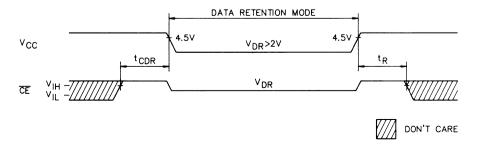
#### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- tHZCE and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8. WE is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

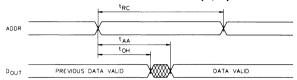
#### **DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)**

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2			٧
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V)	Vcc=2v		95	500	μΑ
		Vin ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=3v		350	750	μА
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0			ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

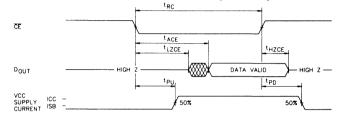
#### LOW Vcc DATA RETENTION WAVEFORM



#### **READ CYCLE NO. 1 (8, 9)**

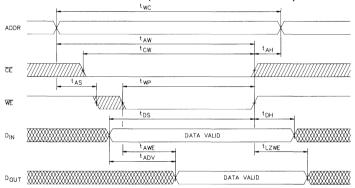


### **READ CYCLE NO. 2 (7, 8, 10)**



### WRITE CYCLE NO. 1

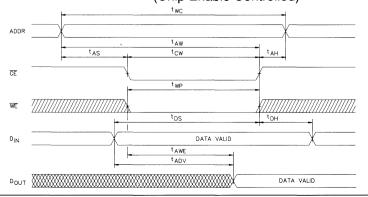
(Write Enable Controlled)



DON'T CARE



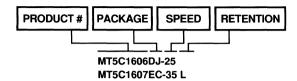
## WRITE CYCLE NO. 2 (Chip Enable Controlled)



DON'T CARE



#### **ORDER INFORMATION**



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled

in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

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		-		

### **SRAM**

### **4K x 16 SRAM**

LATCHED CACHE DATA RAM

#### **FEATURES**

- On-chip address latch.
- Compatible with the Intel 82385 cache memory controller.
- Fast access times: 25ns, 35ns and 45ns.
- Upper and lower byte selects.
- Fast output enable: 10ns into 100pF load.

OPTIONS	MARKING
• Timing	
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	<b>X</b> Y
Plastic DIP (600 mil)	None
Ceramic DIP (600 mil)	C
PLCC	EJ

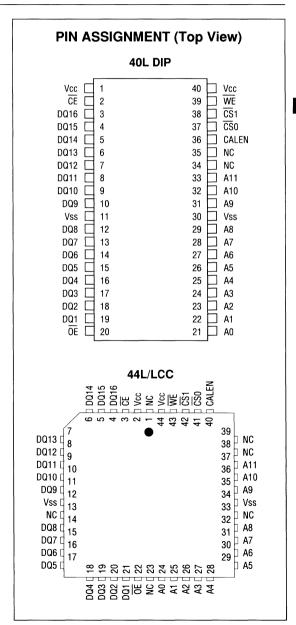
#### **GENERAL DESCRIPTION**

The MT5C6416 is one of a family of fast SRAM latched cache memories. It employs a high speed, low power design using a 4-transistor memory cell. It is fabricated using double layer metal, double layer polysilicon CMOS technology.

The MT5C6416 is designed to be a cache data memory cell building block. It easily interfaces with the Intel 82385 cache memory controller.

The device operates from a single +5V power supply and all inputs and outputs are TTL compatible.

Micron applies the highest level of design and process technology in all their Static RAM products. With a full line of 256K density SRAM's at access times of 25 nanoseconds, Micron has firmly established itself as the leading fast SRAM supplier. So, for your fastest memory requirements, come to the fast memory supplier. . . Micron.



					•

### **SRAM**

## 8K x 8 SRAM

#### **FEATURES**

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with CE, CE2 and OE options
- · All inputs and outputs are TTL compatible

OPTIONS	MARKING
Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
Ceramic DIP (300 mil)	С
Ceramic DIP (600 mil)	CW
Plastic SOJ (300 mil)	DJ
Ceramic LCC (28 pin)	EC
Ceramic LCC (32 pin)	ECW
Two Volt Data Retention	L

#### **GENERAL DESCRIPTION**

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

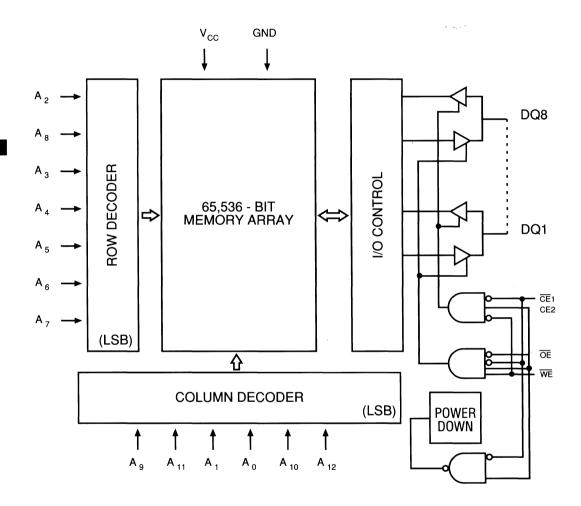
For flexibility in high speed memory applications, Micron offers two chip enables on the x 8 organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

#### PIN ASSIGNMENT (Top View) 28L/300/600 DIP 28L/300 SQJ 28 ] Vcc NC I 28) Vcc NC d1 27 D VE A12 [ 2 27 | VE A12 | 2 A7 ₫ 3 56 p CES A6 d 4 25 h A8 A7 ∏ 3 56 | CES A5 | 5 24 A9 A4 d 6 23 A11 25 AB A6 🛮 4 A3 [ 7 55 1 05 A5 🛮 5 24 A9 21 A10 45 [] 8 A1 [ 9 20 D CE1 A4 [ 6 23 A11 A0 [10 19 | 108 DQ1 d 11 18 DQ7 A3 ∏ 7 55 J DE DQ2 | 12 17 DQ6 DQ3 🛮 13 16 DQ5 21 A10 A2 ∏ 8 Vs**s**□14 15 DQ4 A1 [ 20 CE1 DJC 19 DQ8 A0 10 DQ1 | 11 18 DQ7 28L/LCC בוף כמת DQ6 раз ∏ 13 16 DQ5 1 28 27 Vs**s**[]14 15 ] DQ4 56 p CES 25 | 48 PJ. PK. CH DA9 24 23 DA11 22 DOE 32L/LCC 21 DA10 20 DCE1 DQ1 d11 19 DQ8 A12 DNC DVC DVC DVE no2 d12 18 DQ7 29 D A8 A6 🛮 5 28 49 A5d6 27 A11 A4 [] 7 **ECE** 56 D NC **АЗЦВ** A2 d 9 25 DE 24 b A10 A1 ☐10 A0 (11 23 D CE 1 NC 012 22 DQ8 DQ1 [13 21 | 1007 14 15 1617 181920 0021 VSSI VSSI NCI 0041 0051 **ECF**

#### **FUNCTIONAL BLOCK DIAGRAM**



#### **TRUTH TABLE**

MODE	CE1	CE2 WE O		ŌĒ	DQ OPERATION	POWER
STANDBY	Н	х	Х	X	HIGH Z	STANDBY
STANDBY	Х	L	Х	Х	HIGH Z	STANDBY
READ	L	Н	Н	L	DOUT	ACTIVE
READ	L	Н	Н	Н	HIGH Z	ACTIVE
WRITE	L	Н	L	Х	DIN	ACTIVE



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on VCC supply relative to Vss1.0V to	o +7.0V
Storage Temperature (Ceramic)65°C to	+150°C
Storage Temperature (Plastic)55°C to	+150°C
Power Dissipation	.1 Watt
Short Circuit Output Current	50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 $(0^{\circ}C \leq T_{\mbox{\scriptsize A}} \leq 70^{\circ}C, \ Vcc = 5.0V \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		ViH	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VCC	ILı	-10	10	μА	
Output Leakage Current	Output(s) Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -2.0mA	Vон	2.4		V	1
Output Low Voltage	loL = 4.2mA	Vol		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
		lcc	140	130	120	110	100	100	mA	3
	CE ≥ VIH, Vcc = Max	Is <sub>B1</sub>	60	50	45	40	40	40	mA	
Power Supply Current: Standby	$\overline{\text{CE}} \ge \text{Vcc} - 0.2$ , $\text{Vcc} = \text{Max}$ . $\text{Vil} \ge \text{Vss} + 0.2$ , $\text{ViH} \ge \text{Vcc} - 0.2$ , $\text{f} = 0$	IsB2	5	5	5	5	5	5	mA	

#### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Cı		7	pF	4
Output Capacitance	Vcc = 5V	Co		7	pF	4

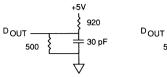
# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (Note 5) (0°C $\leq$ T $_{A}$ $\leq$ 70°C, Vcc = 5V $\pm$ 10%)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
DESCRIPTION	SYM	MIN	MAX	UNITS	NOTES										
READ Cycle															
READ cycle time	<sup>t</sup> RC	12		15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		12		15		20		25		30		35	ns	
Chip enable access time	<sup>t</sup> ACE		12		15		20		25		30		35	ns	
Output hold from access change	t <sub>OH</sub>	3		3		3		3		3		3		ns	
Chip enable to output in low Z	<sup>t</sup> LZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>	i	12		15		20		25		30		35	ns	
Output enable access time	<sup>t</sup> AOE		10		12		15		15		20		20	ns	
Output enable to output in low Z	<sup>t</sup> LZOE	0		0		0		0		0		0		ns	
Output disable to output in high Z	<sup>t</sup> HZOE		10		10		15		15		20		20	ns	6
WRITE Cycle															
WRITE cycle time	twc	12		15		20		25		30		35		ns	
Chip enable to end of write	tcw	10		12		15		20		25		30		ns	
Address valid to end of write	<sup>t</sup> AW	12		15		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	0		0		0		0		0		0		ns	
Write pulse width	t <sub>WP</sub>	10		12		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		10		12		15		15		17		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		0		ns	
Write disable to output in low Z	t <sub>LZWE</sub>	0		0		0		0		0		0		ns	
Write enable to output in high Z	t <sub>HZWE</sub>	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

### MICRON

#### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2





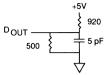


Fig. 2 OUTPUT LOAD EQUIVALENT

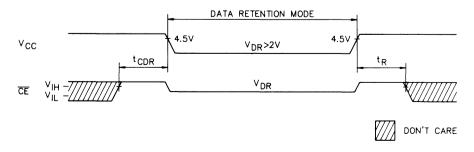
#### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- 6. <sup>t</sup>HZCE, <sup>t</sup>HZWE and <sup>t</sup>HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8.  $\overline{\text{WE}}$  is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

#### **DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)**

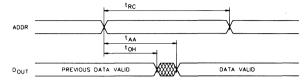
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2		_	٧
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V)	Vcc=2v		95	500	μА
		Vin ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=3v		350	750	μА
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

#### LOW Vcc DATA RETENTION WAVEFORM

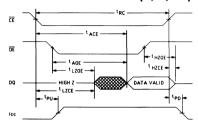


DON'T CARE

#### **READ CYCLE NO. 1 (8, 9)**

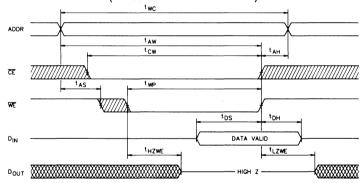


#### **READ CYCLE NO. 2 (7, 8, 10)**



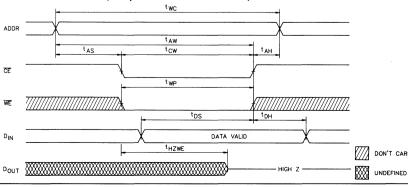
#### **WRITE CYCLE NO. 1**

(Write Enable Controlled)



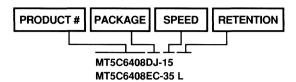
#### **WRITE CYCLE NO. 2**

(Chip Enable Controlled)





#### ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled

in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

### SRAM

## **16K x 1 SRAM**

#### **FEATURES**

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V ( $\pm 10\%$ ) power supply
- Easy memory expansion with CE option
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	С
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
Two Volt Data Retention	L

#### GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable  $(\overline{WE})$  and  $\overline{CE}$  inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

#### PIN ASSIGNMENT (Top View)

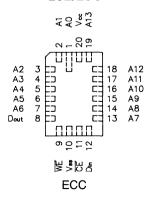
#### 24L/300 SQJ 20L/300 DIP 20 АО ₫ ΑO Vcc 24 D Vcc 23 D A13 A0 01 A1 02 A2 03 A3 04 A4 05 NC 06 NC 07 A5 08 A6 09 Dout 010 WE 011 Vss 012 22 A12 Α1 19 A13 21 5 A11 20 D A10 19 D NC 18 D NC Α2 18 A12 17 A11 A3 17 A9 16 D A8 15 D A7 1 A10 **A4** 16 15 A9 14 DIN 13 D CE Α5 14 Α6 Α8 DJB 13 Α7 Dout WE ! 12 Din

#### 20L/LCC

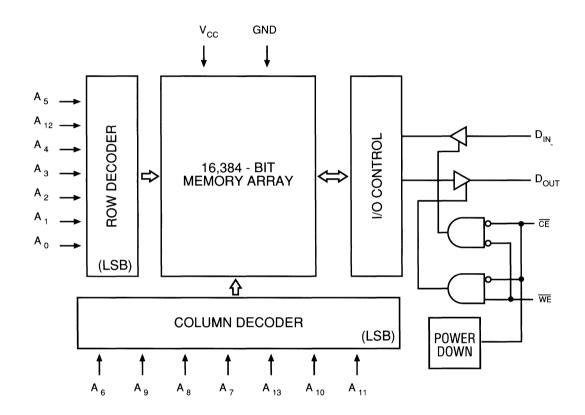
11 CE

Vss [] 10

PD. CD



#### **FUNCTIONAL BLOCK DIAGRAM**



#### **TRUTH TABLE**

MODE	CE	WE	OUTPUT	POWER
STANDBY	Н	Х	HIGH Z	STANDBY
READ	L	Н	DOUT	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

### MICHON

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on VCC supply relative to Vss	1.0V to +7.0V
Storage Temperature (Ceramic)	65°C to +150°C
Storage Temperature (Plastic)	55°C to +150°C
Power Dissipation	1 Watt
Short Circuit Output Current	

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 $(0^{\circ}C \leq T_{\mbox{\scriptsize A}} \leq 70^{\circ}C, \mbox{\ensuremath{Vcc}} = 5.0 \mbox{\ensuremath{V}} \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		Vih	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VCC	ILı	-10	10	μА	
Output Leakage Current	Output(s) Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	Vон	2.4		V	1
Output Low Voltage	IoL = 8.0mA	Vol		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	CE ≤ ViL, Vcc = Max., Outputs Open	lcc	140	130	120	110	100	100	mA	3
	CE ≥ VIH, Vcc = Max	Is <sub>B1</sub>	60	50	45	40	40	40	mA	
Power Supply Current: Standby	$\overline{CE} \ge Vcc - 0.2$ , $Vcc = Max$ . $Vil \le Vss + 0.2$ , $f = 0$ $Vih \ge Vcc - 0.2$	ISB2	5	5	5	5	5	5	mA	

#### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Cı		7	pF	4
Output Capacitance	Vcc = 5V	Co		7	pF	4



#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

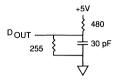
(Note 5) (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C, Vcc = 5V  $\pm$  10%)

DESCRIPTION		-1	2	-1	5	-2	<u>'</u> 0	-2	!5	-3	0	-3	35		
DESCRIPTION	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	<sup>t</sup> RC	12		15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		12		15		20		25		30		35	ns	
Chip enable access time	t <sub>ACE</sub>		12		15		20		25		30		35	ns	
Output hold from access change	<sup>t</sup> OH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	<sup>t</sup> LZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	twc	12		15		20		25		30		35		ns	
Chip enable to end of write	tcw	10		12		15		20		25		30		ns	
Address valid to end of write	<sup>t</sup> AW	12		15		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	0		0		0		0		0		0		ns	
Write pulse width	t <sub>WP</sub>	10		12		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		10		12		15		15		17		ns	
Data hold time	<sup>t</sup> DH	0		0		0		0		0		0		ns	
Write disable to output in low Z	<sup>t</sup> LZWE	0		0		0		0		0		0		ns	
Write enable to output in high Z	<sup>t</sup> HZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6



#### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels .	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2



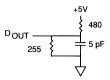


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

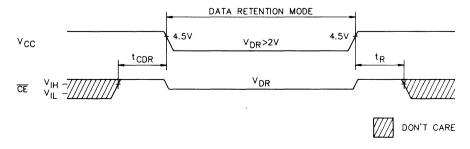
#### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. A ICC is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- tHZCE and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8. WE is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

#### DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2			٧
ICCDR	Data Retention Current	<u>CE</u> ≥ Vcc - 0.2V	Vcc=2v	_	95	500	μА
		Vin ≥ Vcc - 0.2V or ≤ 0.2V	Vcc=3v	_	350	750	μΑ
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			<sup>t</sup> RC <sup>(11)</sup>			ns

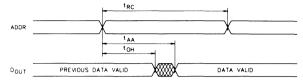
#### LOW Vcc DATA RETENTION WAVEFORM



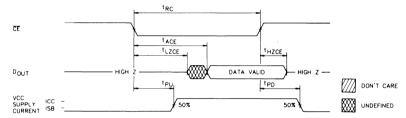
DON'T CARE



#### **READ CYCLE NO. 1 (8, 9)**

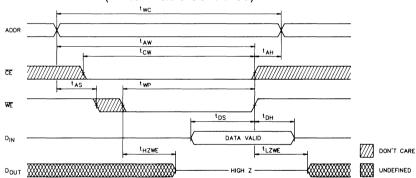


#### **READ CYCLE NO. 2 (7, 8, 10)**



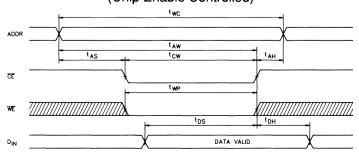
#### **WRITE CYCLE NO. 1**

(Write Enable Controlled)



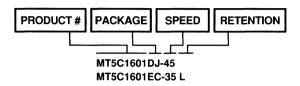
#### **WRITE CYCLE NO. 2**

(Chip Enable Controlled)





#### **ORDER INFORMATION**



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in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

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### SRAM

### **16K x 4 SRAM**

#### **FEATURES**

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal
- Single +5V (±10%) power supply
- Easy memory expansion with CE option
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
Two Volt Data Retention	L

#### GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable  $(\overline{CE})$  on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

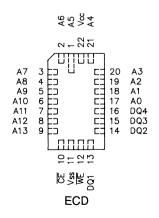
#### PIN ASSIGNMENT (Top View)

#### 22L/300 DIP 24L/300 SQJ A5 [1 A6 [2 A7 [3 A8 [4 A9 [5 A10 [6] 24 23 Vcc 22 Α5 Vcc Δ4 22 b А3 2 21 46 Δ4 21 b A2 20 Α7 20 A3 19 A11 0 7 A12 0 8 A13 0 9 CE 0 10 NC 0 11 18 17 NC 19 A2 Α8 DQ4 16 DQ3 Α9 18 Α1 15 D DQ2 DQ1 A10 17 A0 Vss [ 12 13 D WE DQ4 A11 16 DJB 15 DQ3 A12 A13 DQ2 CE 10 13 DQ1

#### 22L/LCC

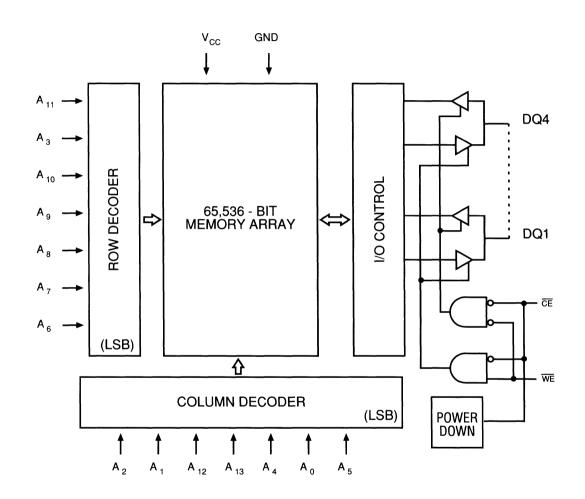
12

PF, CE



Vss [

#### **FUNCTIONAL BLOCK DIAGRAM**



#### **TRUTH TABLE**

MODE	CE	WE	DQ	POWER
STANDBY	Н	Х	HIGH Z	STANDBY
READ	L	Н	DOUT	ACTIVE
WRITE	L	L	DIN	ACTIVE



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V to +7.0V
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation 1 Watt
Short Circuit Output Current50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 $(0^{\circ}C \leq T_{\mbox{\scriptsize A}} \leq 70^{\circ}C, \ Vcc = 5.0V \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		Vih	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ Vin ≤ Vcc	ILı	-10	10	μΑ	
Output Leakage Current	Output(s) Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	Vон	2.4		V	1
Output Low Voltage	IoL = 8.0mA	Vol		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	CE ≤ V <sub>IL</sub> , Vcc = Max., Outputs Open	lcc	140	130	120	110	100	100	mA	3
	CE ≥ VIH, Vcc = Max	Is <sub>B1</sub>	60	50	45	40	40	40	mA	
Power Supply Current: Standby	$\overline{\text{CE}} \ge \text{Vcc} - 0.2$ , $\text{Vcc} = \text{Max}$ . $\text{Vil} \le \text{Vss} + 0.2$ , $\text{Vih} \ge \text{Vcc} - 0.2$ , $\text{f} = 0$	IsB2	5	5	5	5	5	5	mA	

#### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Cı		7	pF	4
Output Capacitance	Vcc = 5V	Со		7	pF	4



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

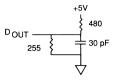
(Note 5) (0°C  $\leq$   $T_{\mbox{\scriptsize A}} \leq$  70°C, Vcc = 5V  $\pm$  10%)

DESCRIPTION		-1	2	-1	5	-2	20	-2	:5	-30		-35			
DESCRIPTION	SYM	MIN	MAX	UNITS	NOTES										
READ Cycle															
READ cycle time	<sup>t</sup> RC	12		15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		12		15		20		25		30		35	ns	
Chip enable access time	<sup>t</sup> ACE		12		15		20		25		30		35	ns	
Output hold from access change	<sup>t</sup> OH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	<sup>t</sup> LZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	twc	12		15		20		25		30		35		ns	
Chip enable to end of write	tcw	10		12		15		20		25		30		ns	
Address valid to end of write	<sup>t</sup> AW	12		15		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	0		0		0		0		0		0		ns	
Write pulse width	<sup>t</sup> WP	10		12		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		10		12		15		15		17		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		0		ns	
Write disable to output in low Z	t <sub>LZWE</sub>	0		0		0		0		0		0		ns	
Write enable to output in high Z	tHZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

### MICRON

#### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2



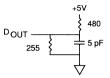


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

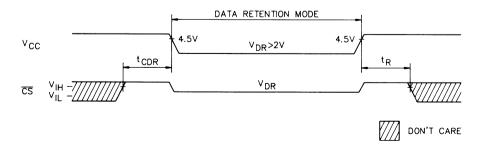
#### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- tHZCE and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8.  $\overline{\text{WE}}$  is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

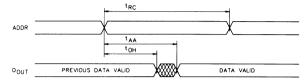
#### **DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)**

SYMBOL	PARAMETER	TEST CONDITI	MIN	TYP	MAX	UNIT	
<b>V</b> DR	Vcc for Retention Data			2		_	٧
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V)			95	500	μΑ
		$\begin{array}{c} \text{Vin} \geq (\text{Vcc - } 0.2\text{V}) \\ \text{or} \leq 0.2\text{V} \end{array}$	Vcc=3v		350	750	μА
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0			ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

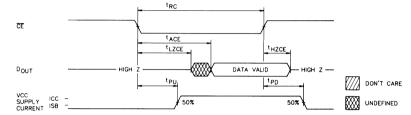
#### LOW Vcc DATA RETENTION WAVEFORM



#### **READ CYCLE NO. 1 (8, 9)**

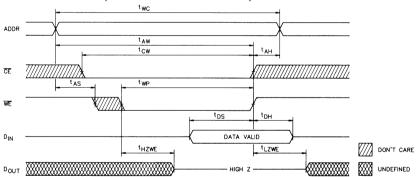


#### **READ CYCLE NO. 2 (7, 8, 10)**



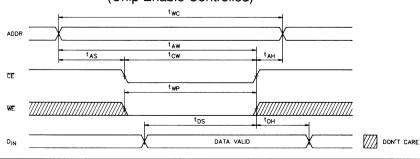
### **WRITE CYCLE NO. 1**

(Write Enable Controlled)



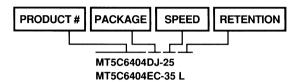
#### **WRITE CYCLE NO. 2**

(Chip Enable Controlled)





#### ORDER INFORMATION



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in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

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### **SRAM**

## **16K x 4 SRAM**

#### WITH OUTPUT ENABLE

#### **FEATURES**

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- · All inputs and outputs are TTL compatible

OPTIONS	MARKING
Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
Two Volt Data Retention	L

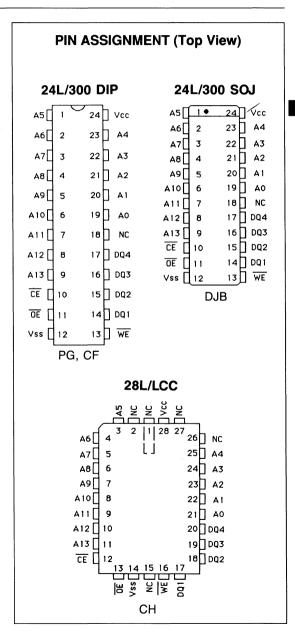
#### **GENERAL DESCRIPTION**

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

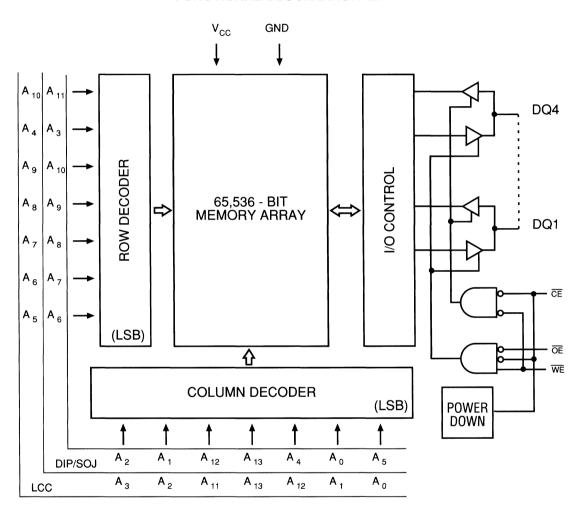
For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.



#### **FUNCTIONAL BLOCK DIAGRAM**



#### **TRUTH TABLE**

MODE	OE	CE	WE	DQ	POWER
STANDBY	X	Н	Х	HIGH Z	STANDBY
READ	L	L	Н	DOUT	ACTIVE
READ	Н	L	Н	HIGH Z	ACTIVE
WRITE	Х	L	L	DIN	ACTIVE



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V to +7.0V
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation 1 Watt
Short Circuit Output Current50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 $(0^{\circ}C \leq T_{\Delta} \leq 70^{\circ}C, \ Vcc = 5.0V \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		Vih	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ Vcc	ILı	-10	10	μΑ	
Output Leakage Current	Output(s) Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	Vон	2.4		V	1
Output Low Voltage	lot = 8.0mA	Vol		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	, , ,		140	130	120	110	100	100	mA	3
	CE ≥ VIH, Vcc = Max	IsB1	60	50	45	40	40	40	mA	
Power Supply Current: Standby	CE       ≥ Vcc - 0.2, Vcc = Max.         ViL ≤ Vss + 0.2,         ViH ≥ Vcc - 0.2, f = 0	IsB2	5	5	5	5	5	5	mA	

#### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Cı		7	pF	4
Output Capacitance	Vcc = 5V	Со		7	pF	4

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (Note 5) (0°C $\leq$ T $_{A}$ $\leq$ 70°C, Vcc = 5V $\pm$ 10%)

DESCRIPTION		-1	2	-15		-20	-25		-30		-35				
DESCRIPTION	SYM	MIN	MAX	UNITS	NOTES										
READ Cycle															
READ cycle time	<sup>t</sup> RC	12		15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		12		15		20		25		30		35	ns	
Chip enable access time	<sup>t</sup> ACE		12		15		20		25		30		35	ns	
Output hold from access change	<sup>t</sup> OH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	<sup>t</sup> LZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		0		ns	
Chip disable to power down time	<sup>t</sup> PD		12		15		20		25		30		35	ns	
Output enable access time	<sup>t</sup> AOE		10		12		15		15		20		20	ns	
Output enable to output in low Z	<sup>t</sup> LZOE	0		0		0		0		0		0		ns	
Output disable to output in high Z	<sup>t</sup> HZOE		10		10		15		15		20		20	ns	6
WRITE Cycle															
WRITE cycle time	twc	12		15		20		25		30		35		ns	
Chip enable to end of write	tcw	10		12		15		20		25		30		ns	
Address valid to end of write	<sup>t</sup> AW	12		15		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	0		0		0		0		0		0		ns	
Write pulse width	<sup>t</sup> WP	10		12		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		10		12		15		15		15		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		0		ns	
Write disable to output in low Z	<sup>t</sup> LZWE	0		0		0		0		0		0		ns	
Write enable to output in high Z	<sup>t</sup> HZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

+5V

480

5 pF

### MICRON

#### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output loadSe	e figures 1 and 2

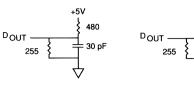


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

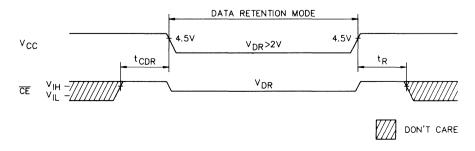
#### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- 6. <sup>t</sup>HZCE, <sup>t</sup>HZWE and <sup>t</sup>HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8. WE is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

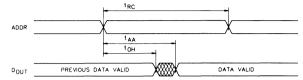
#### **DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)**

SYMBOL	PARAMETER	TEST CONDITI	ONS	MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2		_	٧
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V)	Vcc=2v		95	500	μА
		Vin ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=3v		350	750	μА
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0			ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

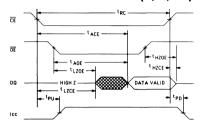
#### LOW Vcc DATA RETENTION WAVEFORM



#### **READ CYCLE NO. 1 (8, 9)**

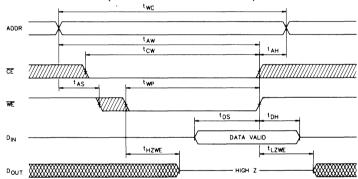


#### **READ CYCLE NO. 2 (7, 8, 10)**



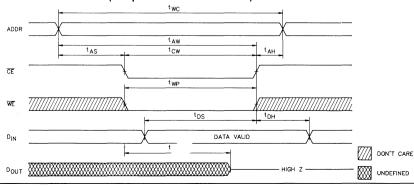
#### **WRITE CYCLE NO. 1**

(Write Enable Controlled)



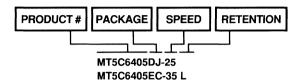
### **WRITE CYCLE NO. 2**

(Chip Enable Controlled)





#### ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled

in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

	-	

## **SRAM**

## **16K x 4 SRAM**

**CACHE-TAG** 

#### **FEATURES**

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  options
- All inputs and outputs are TTL compatible
- Fast match time: 15ns

OPTIONS	MARKING
Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	С
Plastic SOJ (300 mil)	DI
Ceramic LCC	EC

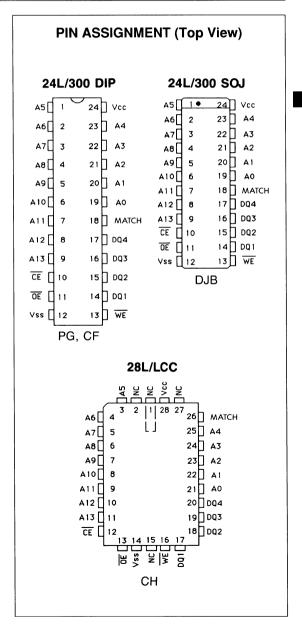
#### **GENERAL DESCRIPTION**

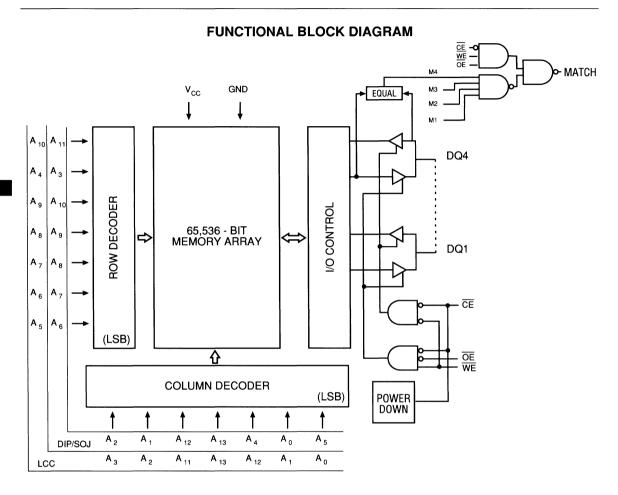
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable  $\overline{\text{CE}}$  on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.





## **TRUTH TABLE**

MODE	OE	CE	WE	DQ	POWER	MATCH
STANDBY	Х	Н	Х	HIGH Z	STANDBY	HIGH
READ	L	L	Н	DOUT	ACTIVE	HIGH
READ	Н	L	Н	HIGH Z	ACTIVE	ACTIVE
WRITE	Х	L	L	DIN	ACTIVE	HIGH



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on VCC supply relative to Vss1.0V t	o +7.0V
Storage Temperature (Ceramic)65°C to	+150°C
Storage Temperature (Plastic)55°C to	+150°C
Power Dissipation	1 Watt
Short Circuit Output Current	50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 $(0^{\circ}C \le T_{\Delta} \le 70^{\circ}C, Vcc = 5.0V \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		Vih	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VCC	1Lı	-10	10	μΑ	
Output Leakage Current	Output(s) Disabled, 0V ≤ Vout ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	Vон	2.4		V	1
Output Low Voltage	loL = 8.0mA	Vol		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	CE ≤ VIL, Vcc = Max., Outputs Open	lcc	140	130	120	110	100	100	mA	3
	CE ≥ VIH, Vcc = Max	Is <sub>B</sub> 1	60	50	45	40	40	40	mA	
Power Supply Current: Standby	$\overline{\text{CE}} \ge \text{Vcc} - 0.2$ , $\text{Vcc} = \text{Max}$ . $\text{ViL} \le \text{Vss} + 0.2$ $\text{ViH} \ge \text{Vcc} - 0.2$ , $\text{f} = 0$	IsB2	5	5	5	5	5	5	mA	

#### CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Cı		7	pF	4
Output Capacitance	Vcc = 5V	Со		7	pF	4

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Note 5) (0°C $\leq$ T $_{A}$ $\leq$ 70°C, Vcc = 5V $\pm$ 10%)

		-1	12	-1	5	-2	20	-2	25	-30		-3	35		
DESCRIPTION	SYM	MIN	MAX	UNITS	NOTES										
READ Cycle															
READ cycle time	<sup>t</sup> RC	12		15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		12		15		20		25		30		35	ns	
Chip enable access time	<sup>t</sup> ACE		12		15		20		25		30		35	ns	
Output hold from access change	<sup>t</sup> OH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	t <sub>LZCE</sub>	5		5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	<sup>t</sup> PU	0		0		0		0		0		0		ns	
Chip disable to power down time	<sup>t</sup> PD		12		15		20		25		30		35	ns	
Output enable access time	t <sub>AOE</sub>		10		12		15		15		20		20	ns	
Output enable to output in low Z	<sup>t</sup> LZOE	0		0		0		0		0		0		ns	
Output disable to output in high Z	<sup>t</sup> HZOE		10		10		15		15		20		20	ns	6
WRITE Cycle															
WRITE cycle time	twc	12		15		20		25		30		35		ns	
Chip enable to end of write	tcw	10		12		15		20		25		30		ns	
Address valid to end of write	<sup>t</sup> AW	12		15		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	0		0		0		0		0		0		ns	
Write pulse width	t <sub>WP</sub>	10		12		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		10		12		15		15		15		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		0		ns	
Write disable to output in low Z	<sup>t</sup> LZWE	0		0		0		0		0		0		ns	
Write enable to output in high Z	<sup>t</sup> HZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

#### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

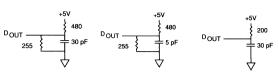


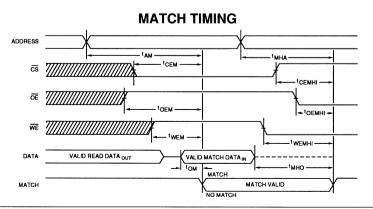
Fig. 1 OUTPUT

Fig. 2 OUTPUT

Fig. 3 OUTPUT LOAD EQUIVALENT LOAD EQUIVALENT LOAD EQUIVALENT

### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

DECODIDATION		-1	12	-1	5	-2	0	-2	:5	-3	10	-3	35		
DESCRIPTION	SYM	MIN	мах	MIN	MAX	UNITS	NOTES								
MATCH cycle															
Address to MATCH valid	<sup>t</sup> AM		15		17		22		25		30		35	ns	12
MATCH hold from address	t <sub>MHA</sub>	5		5		5		5		5		5		ns	12
CE to MATCH	<sup>t</sup> CEM		10		12		15		20		20		20	ns	12
CE to MATCH high	<sup>t</sup> CEMhi		10		12		15		20		20		20	ns	12
OE to MATCH valid	<sup>t</sup> OEM		10		12		15		20		20		25	ns	12
OE to MATCH high	<sup>t</sup> OEMhi		10		12		15		20		20		25	ns	12
WE to MATCH valid	<sup>t</sup> WEM		10		12		15		20		20		25	ns	12
WE to MATCH high	<sup>t</sup> WEMhi		10		12		15		20		20		25	ns	12
Data input to MATCH valid	<sup>t</sup> DM		10		12		15		20		20		25	ns	12
MATCH hold from data	<sup>t</sup> MHD	5		5		5		5		5		5		ns	12

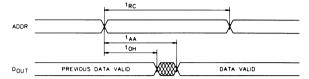


#### **NOTES**

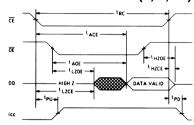
- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- tHZCE, tHZWE and tHZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- 7. At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8.  $\overline{\text{WE}}$  is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. Match timing parameters are tested with RL = 200 and CL = 30pF as shown in Fig. 3.



### **READ CYCLE NO. 1 (8, 9)**

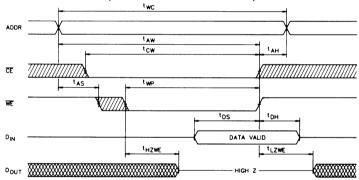


### **READ CYCLE NO. 2 (7, 8, 10)**



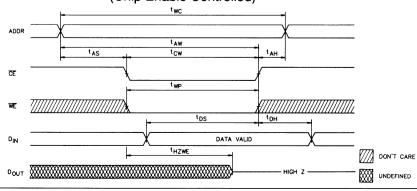
### **WRITE CYCLE NO. 1**

(Write Enable Controlled)



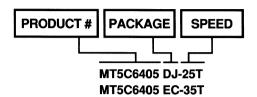
## **WRITE CYCLE NO. 2**

(Chip Enable Controlled)





#### **ORDER INFORMATION**



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled

in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

## SRAM

## **16K x 4 SRAM**

WITH SEPARATE INPUTS AND OUTPUTS

#### **FEATURES**

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal
- Single +5V (±10%) power supply
- Easy memory expansion with  $\overline{CE1}$ ,  $\overline{CE2}$  and  $\overline{OE}$
- All inputs and outputs are TTL compatible
- MT5C6406 output tracks input during WRITE
- MT5C6407 output high impedance during WRITE

OPTIONS	MARKING
Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
Two Volt Data Retention	L

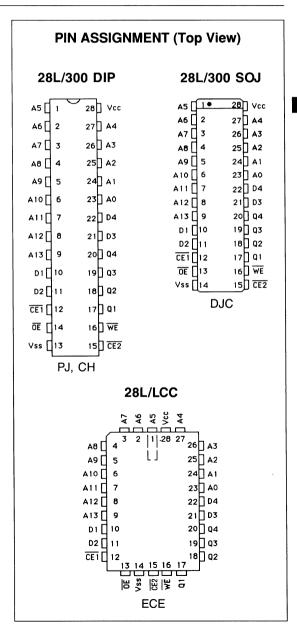
#### **GENERAL DESCRIPTION**

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

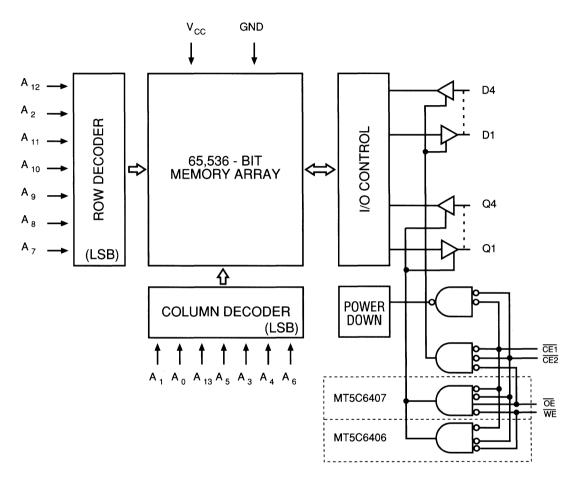
For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 4 configuration features separate data input and output.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.



#### **FUNCTIONAL BLOCK DIAGRAM**



### **TRUTH TABLE**

MODE	CE1	CE2	ŌĒ	WE	OUTPUTS	POWER
STANDBY	Н	Х	Х	Х	HIGH Z	STANDBY
STANDBY	Х	Н	Х	Х	HIGH Z	STANDBY
READ	L	L	L	Н	DOUT	ACTIVE
READ	L	L	Н	Н	HIGH Z	ACTIVE
WRITE (1)	L	L	Х	L	HIGH Z	ACTIVE
WRITE (2)	L	L	L	L	DIN	ACTIVE
WRITE (2)	L	L	Н	L	HIGH Z	ACTIVE

NOTES: 1. MT5C6407 ONLY 2. MT5C6406 ONLY



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on VCC supply relative to Vss	1.0V to +7.0V
Storage Temperature (Ceramic)	65°C to +150°C
Storage Temperature (Plastic)	55°C to +150°C
Power Dissipation	1 Watt
Short Circuit Output Current	50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS** $(0^{\circ}C \le T_{\Delta} \le 70^{\circ}C, Vcc = 5.0V \pm 10\%)$

DECODIDATION

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		Vін	2.2	Vcc +1	٧	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	٧	1, 2
Input Leakage Current	0V ≤ Vin ≤ Vcc	ILı	-10,	10	μА	
Output Leakage Current	Output(s) Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μΑ	
Output High Voltage	lон = -4.0mA	Vон	2.4		V	1
Output Low Voltage	loL = 8.0mA	Vol		0.4	V	1

					М	AX				
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	CE ≤ VIL, Vcc = Max., Outputs Open	lcc	140	130	120	110	100	100	mA	3
	CE ≥ VIH, Vcc = Max	Is <sub>B1</sub>	60	50	45	40	40	40	mA	
Power Supply Current: Standby	$\overline{\text{CE}} \ge \text{Vcc} - 0.2$ , $\text{Vcc} = \text{Max}$ . $\text{Vil} \le \text{Vss} + 0.2$ , $\text{f} = 0$ $\text{Vih} \ge \text{Vcc} - 0.2$	IsB2	5	5	5	5	5	5	mA	

#### **CAPACITANCE**

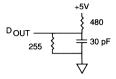
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Cı		7	pF	4
Output Capacitance	Vcc = 5V	Co		7	pF	4

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (Note 5) (0°C $\leq$ T<sub>A</sub> $\leq$ 70°C, Vcc = 5V $\pm$ 10%)

DESCRIPTION		-1	2	-1	5	-2	20	-2	:5	-3	30	-3	35		
DESCRIPTION	SYM	MIN	MAX	UNITS	NOTES										
READ Cycle															
READ cycle time	<sup>t</sup> RC	12		15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		12		15		20		25		30		35	ns	
Chip enable access time	<sup>t</sup> ACE		12		15		20		25		30		35	ns	
Output hold from access change	<sup>t</sup> OH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	t <sub>LZCE</sub>	5		5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	<sup>t</sup> PU	0		0		0		0		0		0		ns	
Chip disable to power down time	<sup>t</sup> PD		12		15		20		25		30		35	ns	
Output enable access time	<sup>t</sup> AOE		10		12		15		15		20		20	ns	
Output enable to output in low Z	<sup>t</sup> LZOE	0		0		0		0		0		0		ns	
Output disable to output in high Z	<sup>t</sup> HZOE		10		10		15		15		20		20	ns	6
WRITE Cycle															
WRITE cycle time	twc	12		15		20		25		30		35		ns	
Chip enable to end of write	tcw	10		12		15		20		25		30		ns	
Address valid to end of write	<sup>t</sup> AW	12		15		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	0		0		0		0		0		0		ns	
Write pulse width	<sup>t</sup> WP	10		12		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		10		12		15		15		15		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		0		ns	
Write disable to output in low Z	t <sub>LZWE</sub>	0		0		0		0		0		0		ns	
Write enable to output valid	<sup>t</sup> AWE		12		15		20		25		30		35	ns	
Data valid to output valid	tADV		12		15		20		25		30		35	ns	

#### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2



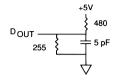


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

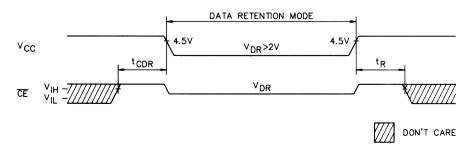
#### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- 6. <sup>t</sup>HZCE, <sup>t</sup>HZWE and <sup>t</sup>HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8. WE is high for READ cycle.
- Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

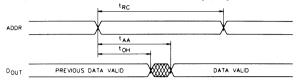
## DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2			٧
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V)			95	500	μΑ
		Vin ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=3v		350	750	μА
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

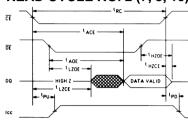
#### LOW Vcc DATA RETENTION WAVEFORM



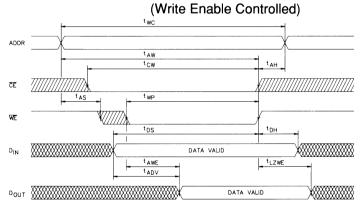
## **READ CYCLE NO. 1 (8, 9)**



## **READ CYCLE NO. 2 (7, 8, 10)**



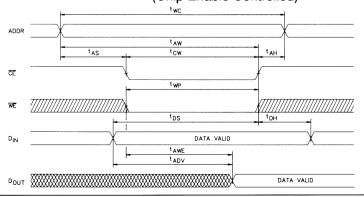
## **WRITE CYCLE NO. 1**



DON'T CARE

UNDEFINED

## **WRITE CYCLE NO. 2** (Chip Enable Controlled)



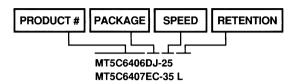
DON'T CARE



UNDEFINED



#### ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled

in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.


## **SRAM**

## **32K x 8 SRAM**

#### **FEATURES**

- High speed: 25, 30, 35, 45 and 55ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with CE and OE options
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
Timing	
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
55ns access	-55
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
Ceramic DIP (300 mil)	С
Ceramic DIP (600 mil)	CW
Plastic SOJ (300 mil)	DJ
Ceramic LCC (28 pin)	EC
Ceramic LCC (32 pin)	ECW
Two Volt Data Retention	L

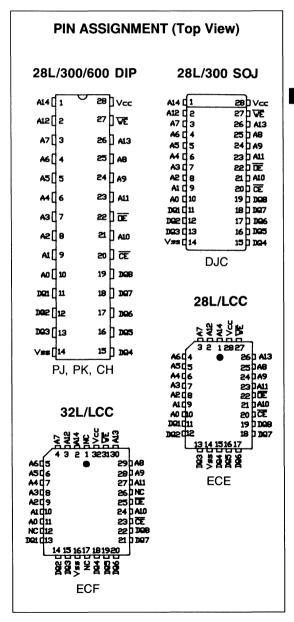
#### **GENERAL DESCRIPTION**

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

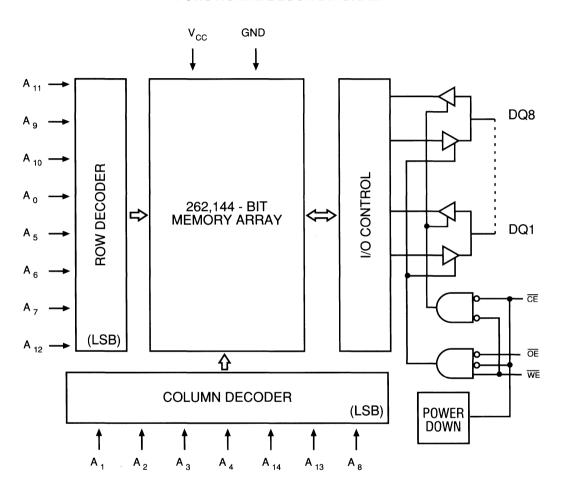
For flexibility in high speed memory applications, Micron offers chip enable  $(\overline{CE})$  on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.



### **FUNCTIONAL BLOCK DIAGRAM**



#### **TRUTH TABLE**

MODE	ŌĒ	CE	WE	DQ	POWER
STANDBY	Х	Н	Х	HIGH Z	STANDBY
READ	L	L	Н	DOUT	ACTIVE
READ	Н	L	Н	HIGH Z	ACTIVE
WRITE	Х	L	L	DIN	ACTIVE



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on VCC supply relative to Vss1.0V to +7.0V
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation
Short Circuit Output Current50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 $(0^{\circ}C \le T_{\Delta} \le 70^{\circ}C, Vcc = 5.0V \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		Vıн	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	٧	1, 2
Power Supply	CE ≤ VIL, Vcc = Max.,	lcc		100	mA	3
Current: Operating	Outputs Open					
	CE ≥ VIH, Vcc = Max.	ISB1		40	mA	
Power Supply Current: Standby	VEE ≥ Vcc - 0.2, Vcc = Max.         VIL ≤ Vss + 0.2,         VIH ≥ Vcc - 0.2, f = 0	Is B2		7	mA	
Input Leakage Current	0V ≤ VIN ≤ Vcc	ILı	-10	10	μΑ	
Output Leakage Current	Output(s) Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -2.0mA	Vон	2.4		V	1
Output Low Voltage	loL = 4.2mA	Vol		0.4	V	1

#### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Cı		8	pF	4
Output Capacitance	Vcc = 5V	Со		8	pF	4



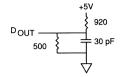
## **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(Note 5) (0°C  $\leq$   $T_{\mbox{\scriptsize A}} \leq$  70°C, Vcc = 5V  $\pm$  10%)

DESCRIPTION		-2	25	-3	30	-35		-45		-55			
DESCRIPTION	SYM	MIN	MAX	UNITS	NOTES								
READ Cycle													
READ cycle time	<sup>t</sup> RC	25		30		35		45		55		ns	
Address access time	t <sub>AA</sub>		25		30		35		45		55	ns	
Chip enable access time	<sup>t</sup> ACE		25		30		35		45		55	ns	
Output hold from address change	<sup>t</sup> OH	5		5		5		5		5		ns	
Chip enable to output in low Z	t <sub>LZCE</sub>	5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		15		20		20		20		20	ns	6, 7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		25		30		35		45		55	ns	
Output Enable Access Time	<sup>t</sup> AOE		15		20		20		20		20	ns	
Output Enable to output in low Z	t <sub>LZOE</sub>	0		0		0		0		0		ns	
Output disable to out put in high Z	<sup>t</sup> HZOE		15		20		20		20		20	ns	
WRITE Cycle													
WRITE cycle time	twc	25		30		35		45		55		ns	
Chip enable to end of write	tcw	20		25		30		40		50		ns	
Address Valid to end of write	t <sub>AW</sub>	20		25		30		40		50		ns	
Address set-up time	<sup>t</sup> AS	0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	2		2		2		2		2		ns	
Write pulse width	t <sub>WP</sub>	20		25		25		30		35		ns	
Data set-up time	t <sub>DS</sub>	15		15		17		20		20		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		ns	
Write disable to output in low Z	tLZWE	0		0		0		0		0		ns	
Write enable to output in high Z	tHZWE	0	15	0	15	0	15	0	20	0	20	ns	6

#### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output loadS	ee figures 1 and 2



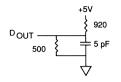


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

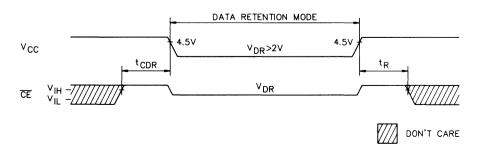
#### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- tHZCE and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8.  $\overline{\text{WE}}$  is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

## **DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)**

SYMBOL	PARAMETER	TEST CONDITI	ONS	MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2		_	٧
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V)			95	500	μΑ
		Vin ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=3v		350	750	μА
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

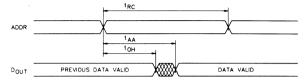
#### LOW Vcc DATA RETENTION WAVEFORM



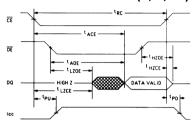
DON'T CARE

UNDEFINED

### **READ CYCLE NO. 1 (8, 9)**

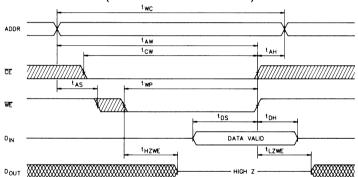


## **READ CYCLE NO. 2 (7, 8, 10)**



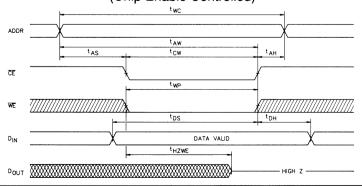
## **WRITE CYCLE NO. 1**

(Write Enable Controlled)



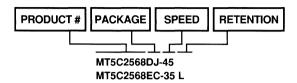
## **WRITE CYCLE NO. 2**

(Chip Enable Controlled)





#### ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled

in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.



## SRAM

## **64K x 1 SRAM**

#### **FEATURES**

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with CE option
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	С
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
Two Volt Data Retention	L

#### GENERAL DESCRIPTION

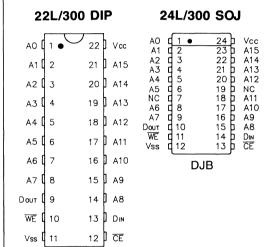
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable  $(\overline{CE})$  on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable (WE) and  $\overline{\text{CE}}$  inputs are both LOW. Reading is accomplished when  $\overline{\text{WE}}$  remains HIGH and  $\overline{\text{CE}}$  goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

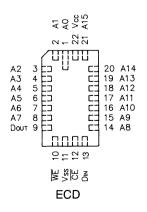
All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

## PIN ASSIGNMENT (Top View)

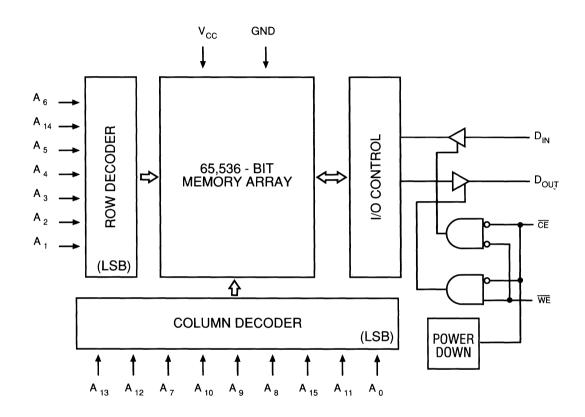


#### 22L/LCC

PF, CE



#### **FUNCTIONAL BLOCK DIAGRAM**



### **TRUTH TABLE**

MODE	CE	WE	DQ	POWER
STANDBY	Н	Х	HIGH Z	STANDBY
READ	L	Н	DOUT	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V to +7.0V
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation1 Watt
Short Circuit Output Current50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{{\color{blue}\Delta}} \leq 70^{\circ}C, \ Vcc = 5.0V \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	YMBOL MIN		UNITS	NOTES	
Input High (Logic 1) Voltage		<b>V</b> IH	2.2	Vcc +1	V	1	
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2	
Input Leakage Current	0V ≤ VIN ≤ Vcc	ILı	-10	10	μА		
Output Leakage Current	Output(s) Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА		
Output High Voltage	lон = -4.0mA	Vон	2.4		V	1	
Output Low Voltage	lot = 8.0mA	Vol		0.4	V	1	

					M	AX				
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	CE ≤ VIL, Vcc = Max., Outputs Open	lcc	140	130	120	110	100	100	mA	3
	CE ≥ VIH, Vcc = Max	Is <sub>B</sub> 1	60	50	45	40	40	40	mA	
Power Supply Current: Standby	CE       ≥ Vcc - 0.2, Vcc = Max.         VIL ≤ Vss + 0.2, f = 0         VIH ≥ Vcc - 0.2	IsB2	5	5	5	5	5	5	mA	

#### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Cı		7	pF	4
Output Capacitance	Vcc = 5V	Со		7	pF	4



## **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

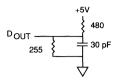
(Note 5) (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C, Vcc = 5V  $\pm$  10%)

DESCRIPTION		-1	2	-1	5	-20		-2	25	-30		-35			
DESCRIPTION	SYM	MIN	MAX	UNITS	NOTES										
READ Cycle															
READ cycle time	t <sub>RC</sub>	12		15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		12		15		20		25		30		35	ns	
Chip enable access time	<sup>t</sup> ACE		12		15		20		25		30		35	ns	
Output hold from access change	<sup>t</sup> OH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	<sup>t</sup> LZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	twc	12		15		20		25		30		35		ns	
Chip enable to end of write	tcw	10		12		15		20		25		30		ns	
Address valid to end of write	<sup>t</sup> AW	12		15		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		0		ns	
Address hold from end of write	t <sub>AH</sub>	0		0		0		0		0		0		ns	
Write pulse width	t <sub>WP</sub>	10		12		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		10		12		15		15		17		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		0		ns	
Write disable to output in low Z	t <sub>LZWE</sub>	0		0		0		0		0		0		ns	
Write enable to output in high Z	tHZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

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#### **AC TEST CONDITIONS**

Input puls	se levels	Vss to 3.0V
Input rise	and fall times	5ns
Input timi	ng reference levels	1.5V
Output re	ference levels	1.5V
Output lo	ad	See figures 1 and 2



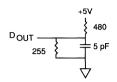


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

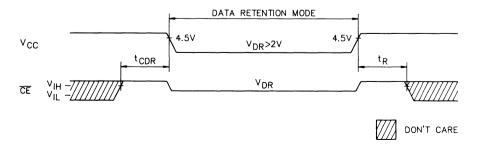
#### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- tHZCE and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>T</sup>LZCE.
- 8. WE is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

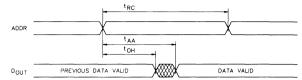
## DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2		_	٧
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V)		_	95	500	μА
		Vin ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=3v		350	750	μΑ
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

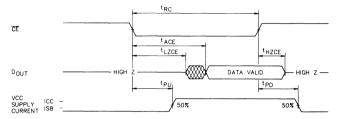
#### LOW Vcc DATA RETENTION WAVEFORM



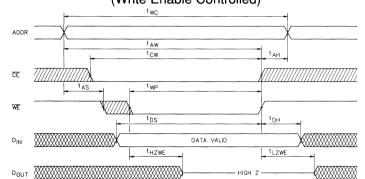
### **READ CYCLE NO. 1 (8, 9)**



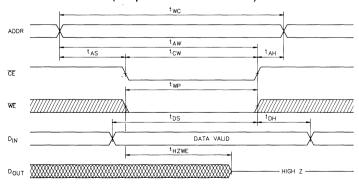
### **READ CYCLE NO. 2 (7, 8, 10)**



# WRITE CYCLE NO. 1 (Write Enable Controlled)

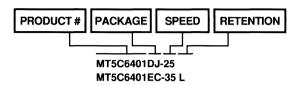


# WRITE CYCLE NO. 2 (Chip Enable Controlled)





#### ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled

in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

.

## **SRAM**

## **64K x 4 SRAM**

#### **FEATURES**

- High speed: 25, 30, 35, 45 and 55ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with CE option
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
Timing	
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
55ns access	-55
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
Two Volt Data Retention	L

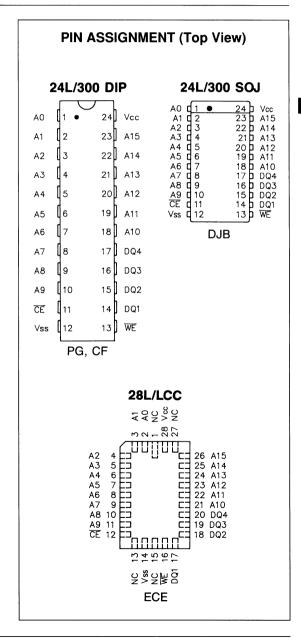
#### GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

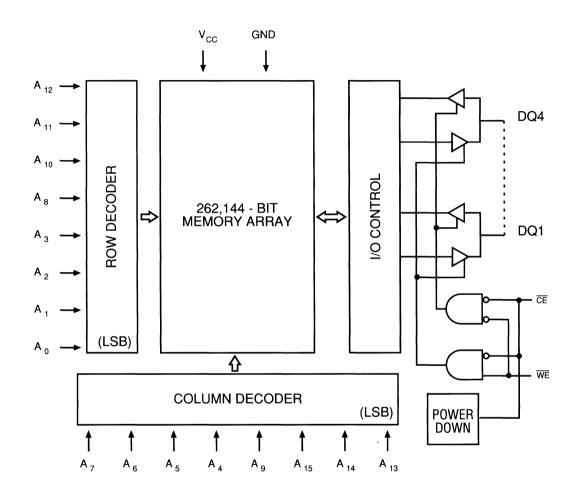
For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.



#### **FUNCTIONAL BLOCK DIAGRAM**



### **TRUTH TABLE**

MODE	CE	WE	DQ	POWER	
STANDBY	Н	Х	HIGH Z	STANDBY	
READ	L	Н	DOUT	ACTIVE	
WRITE	L	L	DIN	ACTIVE	



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on VCC supply relative to Vss1.0V to +7.0V
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation
Short Circuit Output Current50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 $(0^{\circ}C \le T_{\Delta} \le 70^{\circ}C, \ Vcc = 5.0V \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		ViH	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Power Supply	CE ≤ VIL, Vcc = Max.,	lcc		100	mA	3
Current: Operating	Outputs Open					
	CE ≥ VIH, Vcc = Max.	Is <sub>B1</sub>		40	mA	
Power Supply Current: Standby	CE ≥ Vcc - 0.2, Vcc = Max.         VIL ≤ Vss + 0.2,         VIH ≥ Vcc - 0.2, f = 0	IsB2		7	mA	
Input Leakage Current	0V ≤ VIN ≤ Vcc	ILı	-10	10	μА	
Output Leakage Current	Output(s) Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	Vон	2.4		٧	1
Output Low Voltage	IoL = 8.0mA	Vol		0.4	V	1

#### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Cı		8	pF	4
Output Capacitance	Vcc = 5V	Co		8	pF	4

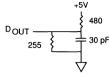
# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (Note 5) (0°C $\leq$ T<sub>A</sub> $\leq$ 70°C, Vcc = 5V $\pm$ 10%)

DESCRIPTION		-2	25	-3	30	-9	35	-4	-5	-5	55		
DESCRIPTION	SYM	MIN	MAX	UNITS	NOTES								
READ Cycle													
READ cycle time	t <sub>RC</sub>	25		30		35		45		55		ns	
Address access time	<sup>t</sup> AA		25		30		35		45		55	ns	
Chip enable access time	<sup>t</sup> ACE		25		30		35		45		55	ns	
Output hold from address change	t <sub>OH</sub>	5		5		5		5		5		ns	
Chip enable to output in low Z	t <sub>LZCE</sub>	5		5		5		5		5		ns	
Chip disable to output in high Z	t <sub>HZCE</sub>		15		20		20		20		20	ns	6, 7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		25		30		35		45		55	ns	
WRITE Cycle													
WRITE cycle time	twc	25		30		35		45		55		ns	
Chip enable to end of write	tcw	20		25		30		40		50		ns	
Address Valid to end of write	<sup>t</sup> AW	20		25		30		40		50		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		ns	
Address hold from end of write	t <sub>AH</sub>	2		2		2		2		2		ns	
Write pulse width	t <sub>WP</sub>	20		25		25		30		35		ns	
Data set-up time	t <sub>DS</sub>	15		15		17		20		20		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		ns	
Write disable to output in low Z	t <sub>LZWE</sub>	0		0		0		0		0		ns	
Write enable to output in high Z	<sup>t</sup> HZWE	0	15	0	15	0	15	0	20	0	20	ns	6

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#### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output loadSee figu	res 1 and 2



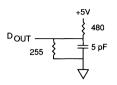


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

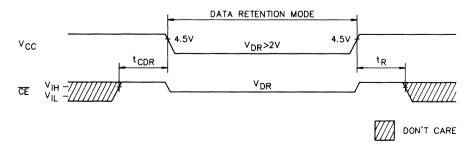
#### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- 6. <sup>t</sup>HZCE and <sup>t</sup>HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8. WE is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

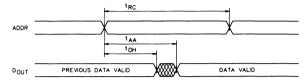
#### DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITI	MIN	TYP	MAX	UNIT	
<b>V</b> DR	Vcc for Retention Data			2		_	٧
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V)			95	500	μА
		Vin ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=3v		350	750	μА
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0			ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			<sup>t</sup> RC <sup>(11)</sup>			ns

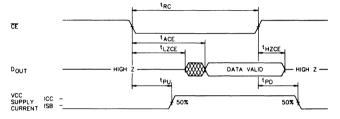
#### **LOW Vcc DATA RETENTION WAVEFORM**



#### **READ CYCLE NO. 1 (8, 9)**

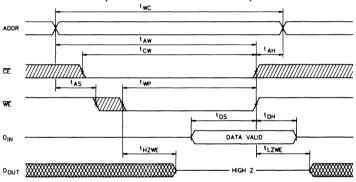


#### **READ CYCLE NO. 2 (7, 8, 10)**

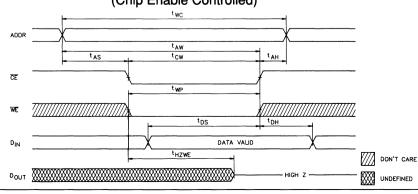


#### WRITE CYCLE NO. 1

(Write Enable Controlled)

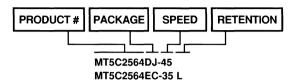


# WRITE CYCLE NO. 2 (Chip Enable Controlled)





#### ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.



### **SRAM**

# **64K x 4 SRAM**

WITH OUTPUT ENABLE

#### **FEATURES**

- High speed: 25, 30, 35, 45 and 55ns
- High performance, low power, CMOS double metal process
- Single +5V ( $\pm 10\%$ ) power supply
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
Timing	
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
55ns access	-55
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
Two Volt Data Retention	L

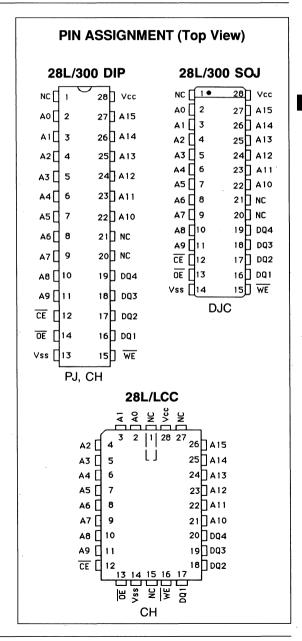
#### GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

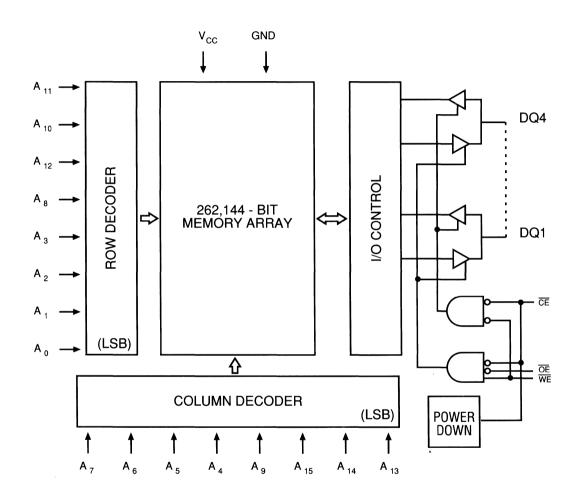
For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.



#### **FUNCTIONAL BLOCK DIAGRAM**



#### **TRUTH TABLE**

MODE	ŌĒ	CE	WE	DQ	POWER
STANDBY	Х	Н	Х	HIGH Z	STANDBY
READ	L	L	Н	DOUT	ACTIVE
READ	Н	L	Н	HIGH Z	ACTIVE
WRITE	Х	L	L	DIN	ACTIVE



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss1.0V to +7.0V
Storage Temperature (Ceramic)65°C to +150°C
Storage Temperature (Plastic)55°C to +150°C
Power Dissipation1 Watt
Short Circuit Output Current50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 $(0^{\circ}C \leq T_{\mbox{\scriptsize A}} \leq 70^{\circ}C, \ \mbox{\scriptsize Vcc} = 5.0 \mbox{\scriptsize V} \pm 10\%)$ 

DESCRIPTION CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		ViH	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	٧	1, 2
Power Supply Current: Operating	lcc		100	mA	3	
	CE ≥ VIH, Vcc = Max.	IsB1		40	mA	
Power Supply Current: Standby	VEE ≥ Vcc - 0.2, Vcc = Max.         VIL ≤ Vss + 0.2,         VIH ≥ Vcc - 0.2, f = 0	IsB2		7	mA	
Input Leakage Current	0V ≤ Vin ≤ Vcc	ILı	-10	10	μΑ	
Output Leakage Current	Output(s) Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	Vон	2.4		V	1
Output Low Voltage loL = 8.0mA		Vol		0.4	V	1

#### **CAPACITANCE**

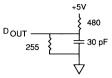
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Cı		8	pF	4
Output Capacitance	Vcc = 5V	Со		8	pF	4

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS (Note 5) (0°C $\leq$ T $_{A}$ $\leq$ 70°C, Vcc = 5V $\pm$ 10%)

DESCRIPTION		-2	25	-3	30	Ÿ	35	-4	<b>1</b> 5	47	55		
DESCRIPTION	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	<sup>t</sup> RC	25		30		35		45		55		ns	
Address access time	<sup>t</sup> AA		25		30		35		45		55	ns	
Chip enable access time	<sup>t</sup> ACE		25		30		35		45		55	ns	
Output hold from address change	<sup>t</sup> OH	5		5		5		5		5		ns	
Chip enable to output in low Z	t <sub>LZCE</sub>	<sub>.</sub> 5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		15		20		20		20		20	ns	6, 7
Chip enable to power up time	<sup>t</sup> PU	0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		25		30		35		45		55	ns	
Output Enable Access Time	<sup>t</sup> AOE		15		20		20		20		20	ns	
Output Enable to output in low Z	t <sub>LZOE</sub>	0		0		0		0		0		ns	
Output disable to output in high Z	<sup>t</sup> HZOE		15		20		20		20		20	ns	6
WRITE Cycle													
WRITE cycle time	twc	25		30		35		45		55		ns	
Chip enable to end of write	tcw	20		25		30		40		50		ns	
Address Valid to end of write	<sup>t</sup> AW	20		25		30		40		50		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		ns	
Address hold from end of write	t <sub>AH</sub>	2		2		2		2		2		ns	
Write pulse width	tWP	20		25		25		30		35		ns	
Data set-up time	t <sub>DS</sub>	15		15		17		20		20		ns	
Data hold time	<sup>t</sup> DH	0		0		0		0		0		ns	
Write disable to output in low Z	tLZWE	0		0		0		0		0		ns	
Write enable to output in high Z	<sup>t</sup> HZWE	0	15	0	15	0	15	0	20	0	20	ns	6

#### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2



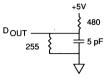


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

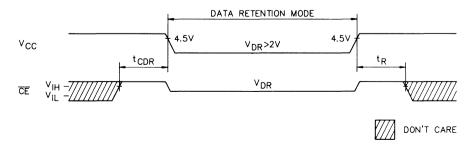
#### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- tHZCE, tHZOE and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8.  $\overline{\text{WE}}$  is high for READ cycle.
  - 9. Device is continuously selected. All Chip Enables held in their active state.
  - 10. Address valid prior to or coincident with latest occurring Chip Enable.
  - 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

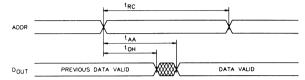
#### **DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)**

SYMBOL	PARAMETER	TEST CONDITI	MIN	TYP	MAX	UNIT	
<b>V</b> DR	Vcc for Retention Data			2		_	٧
Iccor	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V)			95	500	μΑ
		$Vin \ge (Vcc - 0.2V)$ or $\le 0.2V$	Vcc=3v		350	750	μА
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

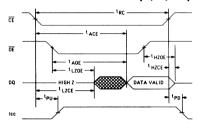
#### LOW Vcc DATA RETENTION WAVEFORM



#### **READ CYCLE NO. 1 (8, 9)**

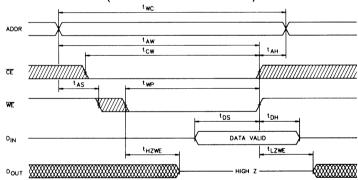


#### **READ CYCLE NO. 2 (7, 8, 10)**



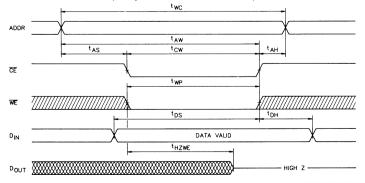
#### **WRITE CYCLE NO. 1**

(Write Enable Controlled)



#### **WRITE CYCLE NO. 2**

(Chip Enable Controlled)

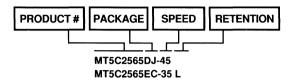


DON'T CARE

UNDEFINED



#### ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled

in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

### SRAM

# 128K x 8 SRAM

#### **FEATURES**

- High speed: 25, 35 and 45ns
- Automatic chip enable power down
- All inputs and outputs are TTL compatible
- High performance, low power, CMOS process
- Single +5V (±10%) power supply
- Low power, ICC (max.) 70mA

OPTIONS	MARKIN				
Timing					
25ns access	-25				
35ns access	-35				
45ns access	-45				
• Packages					
Plastic DIP	None				
Ceramic DIP	C				
Two Volt Data Retention	L				

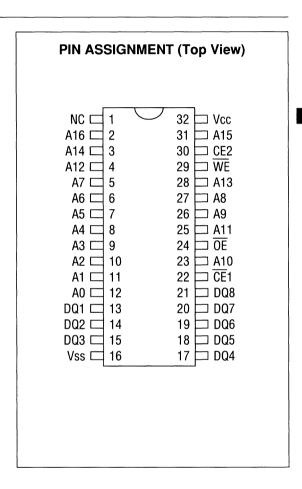
#### GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. Output Enable (OE) is an enhancement available for all common I/O organizations. This enhancement can place the output in a high impedance state for additional flexibility in system design. The x 1 organization features separate data input and output.

Writing to these devices is accomplished when write enable (WE) and  $\overline{\text{CE}}$  inputs are both LOW. Reading is accomplished when  $\overline{\text{WE}}$  remains HIGH and  $\overline{\text{CE}}$  goes to LOW. When the  $\overline{\text{OE}}$  option is present, it must also be LOW to read the device. The devices offer a reduced power standby mode when disabled. This allows system designs for low power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.



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## **SRAM**

# 256K x 1 SRAM

#### **FEATURES**

- High speed: 25, 30, 35, 45 and 55ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with CE option
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
• Timing	
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
55ns access	-55
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	С
Plastic SOJ (300 mil)	DI
Ceramic LCC	EĆ
Two Volt Data Retention	L

#### GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

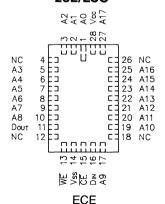
For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

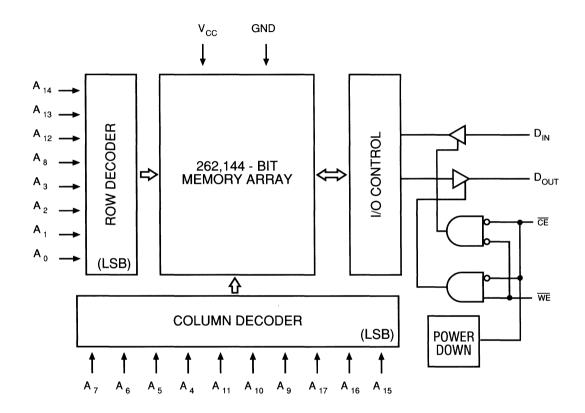
All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

#### PIN ASSIGNMENT (Top View) 24L/300 DIP 24L/300 SQJ A0 d 1 ● 24 D Vcc 23 D A17 24 Noc A2 3 22 h A16 23 A17 A1 l A3 4 21 D A15 20 D A14 A2 3 22 A16 A5 d 6 19 A13 A6 0 7 A7 0 8 18 A12 АЗ 21 A15 17 A11 A8 L 9 16 A10 20 A14 A4 | 5 Dout | 10 WE | 11 14 DIN A5 | 6 19 A13 Vss 🗖 12 13 D CE 18 A12 Α6 DJB [] A11 Α7 18 17 8A 16 A10 N A9 Dout 15 WĒ 14 DIN 13 CE Vss PG, CF

#### 28L/LCC



#### **FUNCTIONAL BLOCK DIAGRAM**



#### **TRUTH TABLE**

MODE	CE	WE	ОИТРИТ	POWER
STANDBY	Н	Х	HIGH Z	STANDBY
READ	L	Н	DOUT	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE



#### **ABSOLUTE MAXIMUM RATINGS\***

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 $(0^{\circ}C \leq T_{\mbox{\scriptsize A}} \leq 70^{\circ}C, \ \mbox{\scriptsize Vcc} = 5.0 \mbox{\scriptsize V} \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		ViH	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Power Supply Current: Operating	CE ≤ V <sub>IL</sub> , Vcc = Max., Outputs Open	lcc		100	mA	3
	CE ≥ VIH, Vcc = Max.	ISB1		40	mA	
Power Supply Current: Standby	CE ≥ Vcc - 0.2, Vcc = Max.         VIL ≤ Vss + 0.2,         VIH ≥ Vcc - 0.2, f = 0	Is B2		10	mA	
Input Leakage Current	0V ≤ Vin ≤ Vcc	ILı	-10	10	μΑ	
Output Leakage Current	Output(s) Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	Vон	2.4		V	1
Output Low Voltage	lot = 8.0mA	Vol		0.4	V	1

#### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz	Cı		8	pF	4
Output Capacitance	Vcc = 5V	Co		8	pF	4

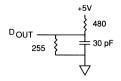
MICHON

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS** (Note 5) (0°C $\leq$ T<sub>A</sub> $\leq$ 70°C, Vcc = 5V $\pm$ 10%)

DESCRIPTION		-2	25	-(	30	-3	35	-4	5	-5	55		
DESCRIPTION	SYM	MIN	MAX	UNITS	NOTES								
READ Cycle													
READ cycle time	t <sub>RC</sub>	25		30		35		45		55		ns	
Address access time	<sup>t</sup> AA		25		30		35		45		55	ns	
Chip enable access time	t <sub>ACE</sub>		25		30		35		45		55	ns	
Output hold from address change	<sup>t</sup> OH	5		5		5		5		5		ns	
Chip enable to output in low Z	<sup>t</sup> LZCE	5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		15		20		20		20		20	ns	6, 7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		25		30		35		45		55	ns	
WRITE Cycle													
WRITE cycle time	twc	25		30		35		45	i	55		ns	
Chip enable to end of write	tcw	20		25		30		40		50		ns	
Address Valid to end of write	<sup>t</sup> AW	20		25		30		40		50		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	2		2		2		2		2		ns	
Write pulse width	t <sub>WP</sub>	20		25		25		30		35		ns	
Data set-up time	t <sub>DS</sub>	15		15		17		20		20		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		ns	
Write disable to output in low Z	tLZWE	0		0		0		0		0		ns	
Write enable to output in high Z	<sup>t</sup> HZWE	0	15	0	15	0	15	0	20	0	20	ns	6

#### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2



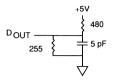


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

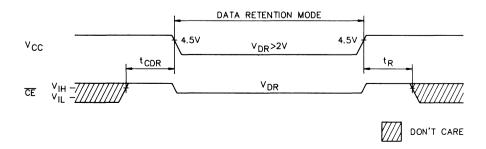
#### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- tHZCE and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8.  $\overline{\text{WE}}$  is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. at Vcc = 2V.
- 12. at Vcc = 3V.
- 13. <sup>t</sup>RC = Read Cycle Time. (Page 4)

#### **DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)**

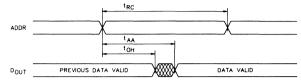
SYMBOL	PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data		2		V
ICCDR	Data Retention Current	CE ≥ (Vcc - 0.2V) V <sub>IN</sub> ≥ (Vcc - 0.2V) or ≤ 0.2V	95 350	500 <sup>(11)</sup> 750 <sup>(12)</sup>	μ <b>Α</b> μ <b>Α</b>
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time		0		ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time		<sup>t</sup> RC <sup>(13)</sup>		ns

#### LOW Vcc DATA RETENTION WAVEFORM

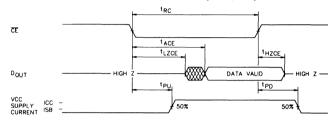


DON'T CARE
UNDEFINED

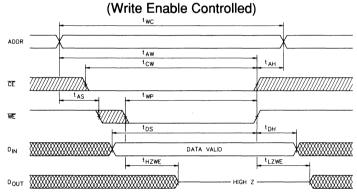
#### **READ CYCLE NO. 1 (8, 9)**



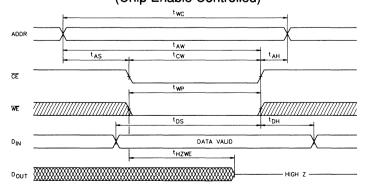
#### **READ CYCLE NO. 2 (7, 8, 10)**



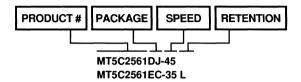
### WRITE CYCLE NO. 1



# WRITE CYCLE NO. 2 (Chip Enable Controlled)



#### **ORDER INFORMATION**



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled

in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

	 Manufacture Co.		

## **SRAM**

# 256K x 4 SRAM

WITH OUTPUT ENABLE

#### **FEATURES**

- High speed: 25, 35 and 45ns
- Automatic chip enable power down
- All inputs and outputs are TTL compatible
- High performance, low power, CMOS process
- Single +5V (±10%) power supply
- Low power, ICC (max.) 70mA

OPTIONS	MARKING
Timing	
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP	None
Ceramic DIP	С
• Two Volt Data Retention	L

#### GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ( $\overline{\text{CE}}$ ) on all organizations. Output Enable ( $\overline{\text{OE}}$ ) is an enhancement available for all common I/O organizations. This enhancement can place the output in a high impedance state for additional flexibility in system design. The x 1 organization features separate data input and output.

Writing to these devices is accomplished when write enable ( $\overline{WE}$ ) and  $\overline{CE}$  inputs are both LOW. Reading is accomplished when  $\overline{WE}$  remains HIGH and  $\overline{CE}$  goes to LOW. When the  $\overline{OE}$  option is present, it must also be LOW to read the device. The devices offer a reduced power standby mode when disabled. This allows system designs for low power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

#### PIN ASSIGNMENT (Top View) **28L DIP** A7 d 1 28 TVcc 27 h A6 A9 d 3 26 h A5 A10 d 4 25 h A4 24 h A3 A12 d 6 23 h A2 A13 ₫ 7 22 h A1 A14 d 8 21 h A6 A15 d 9 20 h NC 19 | DQ4 18 | DQ3 CE | 12 17 h DQ2 16 h DQ1 15 \ WE


# **SRAM**

# 1MEG x 1 SRAM

#### **FEATURES**

- High speed: 25, 35 and 45ns
- Automatic chip enable power down
- All inputs and outputs are TTL compatible
- High performance, low power, CMOS process
- Single +5V ( $\pm 10\%$ ) power supply
- Low power, ICC (max.) 70mA

OPTIONS	MARKING
Timing	
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP	None
Ceramic DIP	С
Two Volt Data Retention	L

#### **GENERAL DESCRIPTION**

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable  $(\overline{CE})$  on all organizations. Output Enable  $(\overline{OE})$  is an enhancement available for all common I/O organizations. This enhancement can place the output in a high impedance state for additional flexibility in system design. The x 1 organization features separate data input and output.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. When the OE option is present, it must also be LOW to read the device. The devices offer a reduced power standby mode when disabled. This allows system designs for low power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

PIN ASSIGNMENT (Top View)								
28L DIP								
A11 [ 1	28	Vcc						
A12 [ 2	27	] A10						
A13 [ 3	26	A9						
A14 [ 4	25	A8						
A15 🛚 5	24	A7						
A16 [ 6	23	A6						
NC [ 7	22	A5						
A17 [ 8	21	<b>A4</b>						
A18 [ 9	20	A3						
A19 [ 1	0 19	A2						
A20 🛚 1	1 18	□ <b>A1</b>						
<b>D</b> оит [ <b>1</b>	2 17	<b>A0</b>						
<b>W</b> E [ 1	3 16	D IN						
Vss [ 1	4 15	D CE						

		*			
				~	
 	-		 		-

# **SECTION GUIDE**

DYNAMIC RAMs	1
DYNAMIC RAM MODULES	2
MULTIPORT DYNAMIC RAMs (VRAMs)	3
STATIC RAMs	· <b>4</b>
CACHE DATA RAMs	5
FIFO MEMORIES	6
FIFO MEMORIES	
	7

# CACHE DATA STATIC RAMS

#### **CACHE DATA RAM PRODUCT SELECTION GUIDE**

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package	Process	Page
Dual 4K x 16/18	Mode, Byte Select	MT56C0416	25, 35, 45	52-Pin PLCC	CMOS	5-1
or	CE, OE,	}				
Single 8K x16/18	Address Latch					

5-1

•

# CACHE DATA STATIC RAMS

# DUAL 4K x 16/18 SRAM, SINGLE 8K x 16/18

CONFIGURABLE CACHE DATA RAM

#### **FEATURES**

- Operates as two 4K x 16/18 SRAMs with common addresses, common data and separate control signals.
- Configurable as a single 8K x 16/18 SRAM with MODE input.
- Two parity bit utilization when operated in x 18 mode.
- · Built-in address input latches.
- Separate byte selects.
- Fast access times: 25ns, 35ns and 45ns.
- Upper and lower byte selects.
- Fast output enable: 8ns.
- Compatible with the Intel 82385 cache memory controller.

OPTIONS • Timing 25ns access	MARKING
Timing	
25ns access	-25
35ns access	-35
45ns access	-45

#### GENERAL DESCRIPTION

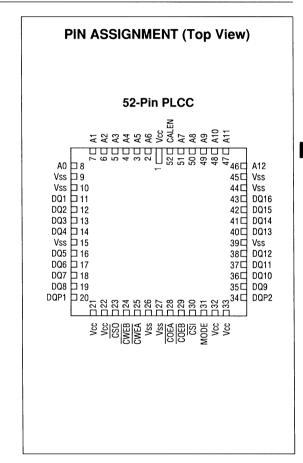
The MT56C0416 is one of a family of fast SRAM cache memories. It employs a high speed, low power design using a 4-transistor memory cell. It is fabricated using double layer metal, double layer polysilicon CMOS technology.

The MT56C0416 is designed to be a cache data memory cell building block. It easily interfaces with the Intel 82385 cache controller in either the direct mapped or two-way set associative mode. A mode control pin determines the configuration of the memory. When this pin is held low, the device functions as an 8K by 16 or 18 bit SRAM. When the mode pin is high, the device is configured as a dual 4K by 16 or 18 bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are contolled by the output enable, write enable and chip select signals. Outputs of the "A" bank SRAM are enabled when the  $\overline{\text{COEA}}$  pin makes a high to low level transition. Outputs of the "B" bank SRAM are enabled when the  $\overline{\text{COEB}}$  pin makes a high to low transistion.

Write enables are also activated on the high to low



transitions.  $\overline{\text{CWEA}}$  allows data to be written in the "A" bank and  $\overline{\text{CWEB}}$  causes data to be written in the "B" bank.  $\overline{\text{CS0}}$  and  $\overline{\text{CS1}}$  determine the byte selection.  $\overline{\text{CS0}}$  controls the lower byte and  $\overline{\text{CS1}}$  controls the upper byte.

Micron applies the highest level of design and process technology in all their Static RAM products. With a full line of 256K density SRAM's at access times of 25 nanoseconds, Micron has firmly established itself as the leading fast SRAM supplier. So, for your fastest memory requirements, come to the fast memory supplier. . . Micron.

DYNAMIC RAMs	1
DYNAMIC RAM MODULES	2
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CACHE DATA RAMs	5
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#### FIFO PRODUCT SELECTION GUIDE

Memory Control		Part	Part Access		Package & Number of Pins			
Configuration	Functions	Number	Time (ns)	PDIP	CDIP	LCC	PLCC	Page
512 x 8	MB, VF	MT52C8006	25, 30, 35	28	28	-	-	6-3
512 x 9	E	MT52C9005	25, 30, 35	28	28	32	32	6-5
512 x 9	MB	MT52C9006	25, 30, 35	28	28	32	32	6-7
512 x 9	VF	MT52C9007	25, 30, 35	28	28	32	32	6-9
512 x 16	E, MB, VF	MT52C1605	25, 30, 35	48	48	-	-	6-11
512 x 16/8	E, MB, VF	MT52C1607	25, 30, 35	40	40	-	-	6-13
1K x 8	MB, VF	MT52C8011	25, 30, 35	28	28	-	-	6-15
1K x 9	E	MT52C9010	25, 30, 35	28	28	32	32	6-17
1K x 9	МВ	MT52C9011	25, 30, 35	28	28	32	32	6-19
1K x 9	VF	MT52C9012	25, 30, 35	28	28	32	32	6-21
1K x 16	E, MB, VF	MT52C1610	25, 30, 35	48	48	-	-	6-23
1K x 16/8	E, MB, VF	MT52C1612	25, 30, 35	40	40	-	-	6-25
2K x 8	MB, VF	MT52C8021	25, 30, 35	28	28	-	-	6-27
2K x 9	E	MT52C9020	25, 30, 35	28	28	32	32	6-29
2K x 9	МВ	MT52C9021	25, 30, 35	28	28	32	32	6-31
2K x 9	VF	MT52C9022	25, 30, 35	28	28	32	32	6-33
2K x 16	E, MB, VF	MT52C1620	25, 30, 35	48	48	-	-	6-35
2K x 16/8	E, MB, VF	MT52C1622	25, 30, 35	40	40	-	-	6-37
4K x 8	MB, VF	MT52C8041	25, 30, 35	28	28	-	-	6-39
4K x 9	E	MT52C9040	25, 30, 35	28	28	32	32	6-41
4K x 9	МВ	MT52C9041	25, 30, 35	28	28	32	32	6-43
4K x 9	VF	MT52C9042	25, 30, 35	28	28	32	32	6-45

MB ..... Mailbox Register
VF ..... Variable Flags
E ..Depth and Width Expandable



# 512 x 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- · Automatic retransmit
- Low power

Transistor loads for maximum data integrity

OPTIONS	MARKING			
Timing				
25ns access time	-25			
30ns access time	-30			
35ns access time	-35			
Packages				
Plastic DIP	None			
Ceramic DIP	С			

## **GENERAL DESCRIPTION**

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

There are three types of FIFO's in the Micron family: Expandable, Mailbox Register, and Variable Flags. Expandable FIFO's are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFO's have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFO's allow the user to program the level of the full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

## PIN ASSIGNMENT (Top View) **28L DIP** 28 h Vcc MBS □ 2 27 h D5 D4 d 3 26 h D6 D3 d 4 25 h D7 D2 | 5 24 h D8 23 h RT D1 d 6 22 h RS FF d 21 h EF 20 h VE Q1 d 9 Q2 d 10 19 h Q8 Q3 d 11 18 h Q7 Q4 | 12 17 \( \) Q6 MBF **13** 16 h Q5 Vss [] 14 15 | R

# 512 x 9 FIFO

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Industry standard pin-out
- · Empty and Full warning flags
- Asynchronous READ and WRITE
- Depth and Width expansion capability
- · Automatic retransmit
- Low power consumption
- Transistor loads for maximum data integrity

OPTIONS	MARKING
Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

## **GENERAL DESCRIPTION**

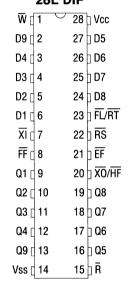
The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

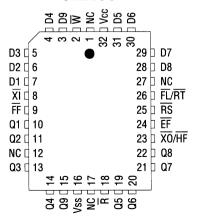
There are three types of FIFO's in the Micron family: Expandable, Mailbox Register, and Variable Flags. Expandable FIFO's are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFO's have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFO's allow the user to program the level of the full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

## PIN ASSIGNMENT (Top View)

## 28L DIP





## MICR<u>ON</u>

# **FIFO**

# 512 x 9 FIFO

MAILBOX REGISTER

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Asynchronous READ and WRITE
- · Automatic retransmit
- Low power

**OPTIONS** 

• Transistor loads for maximum data integrity

MARKING

Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

#### GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

#### PIN ASSIGNMENT (Top View) **28L DIP** 28 Vcc D9 d 2 27 h D5 D4 d 3 26 | D6 D3 d 4 25 h D7 D2 d 5 24 h D8 23 h RT D1 d 6 22 h RS FF 8 21 h EF 20 h MBF Q1 / 9 Q2 d 10 19 h Q8 18 h Q7 Q3 | 11 Q4 d 12 17 \quad Q6 Q9 d 13 16 h Q5 15 🛭 R 32L/LCC 29 h D7 D3 🛚 5 D2 🛚 6 28 D8 27 h NC D1 🛮 7 MBS 2 8 26 RT 25 h RS FF 🛮 9 24 \( \bar{\text{EF}} Q1 🛮 10 Q2 [ 11 23 T MBF NC [ 12 22 D Q8 21 b Q7 Q3 [ 13 14 15 17 17 19 20 20 04 03 NC 38 05 05 05

# 512 x 9 FIFO

VARIABLE FLAGS

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- · Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS	MARKING
Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	С
Plastic LCC	EJ
Ceramic LCC	EC

## GENERAL DESCRIPTION

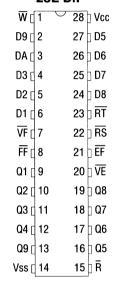
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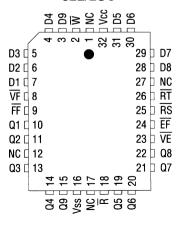
There are three types of FIFO's in the Micron family: Expandable, Mailbox Register, and Variable Flags. Expandable FIFO's are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFO's have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFO's allow the user to program the level of the full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

## PIN ASSIGNMENT (Top View)

## 28L DIP





# 512 x 16 FIFO

**VARIABLE FLAGS/MAILBOX REGISTER** 

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- 16-bit word width
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- · Easy expansion capability
- · Automatic retransmit
- Low power

**OPTIONS** 

Transistor loads for maximum data integrity

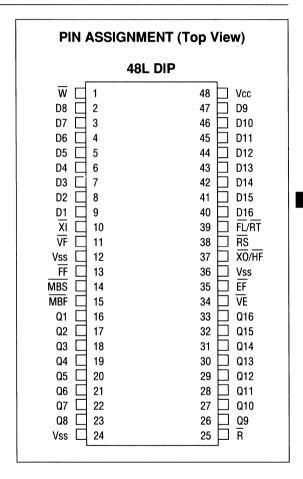
Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

MARKING

## **GENERAL DESCRIPTION**

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

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# 512 x 16 to 8 FIFO

PIN ASSIGNMENT (Top View)

**VARIABLE FLAGS/MAILBOX REGISTER** 

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE.
- Easy expansion capability
- · Automatic retransmit
- Low power

Ceramic DIP

- Transistor loads for maximum data integrity
- One chip interface between a 16 bit bus and an 8 bit

OPTIONS	MARKING			
Timing				
25ns access time	-25			
30ns access time	-30			
35ns access time	-35			
• Packages				
Plastic DIP	None			

 $\mathbf{C}$ 

#### 40L DIP w 40 1 Vcc D8 2 39 D9 D7 3 38 D10 D11 D6 37 4 5 D5 36 D12 D4 6 35 D13 7 D3 34 D14 33 D15 D2 8 D1 9 32 D16 Χı FL/RT 10 31 VF RS 30 11 FF 29 XO/HF 12 EF MBS 13 28 VΕ **MBF** 14 27 26 NC 15 RC Q1 25 Q8 16 Q2 17 24 Q7 23 06 Q3 18 22 04 19 Q5 $\bar{R}$ 20 21 Vss

## **GENERAL DESCRIPTION**

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

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# 1K x 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

#### **FEATURES**

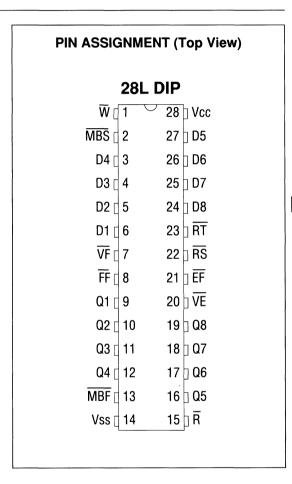
- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- · Automatic retransmit
- Low power
- · Transistor loads for maximum data integrity

OPTIONS	MARKING
• Timing 25ns access time	25
	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

#### GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

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# 1K x 9 FIFO

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Industry standard pin-out
- Empty and Full warning flags
- Asynchronous READ and WRITE
- · Depth and Width expansion capability
- · Automatic retransmit
- Low power consumption
- Transistor loads for maximum data integrity

OPTIONS	MARKING			
Timing				
25ns access time	-25			
30ns access time	-30			
35ns access time	-35			
Packages				
Plastic DIP	None			
Ceramic DIP	C			
Plastic LCC	EJ			
Ceramic LCC	EC			

## **GENERAL DESCRIPTION**

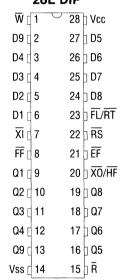
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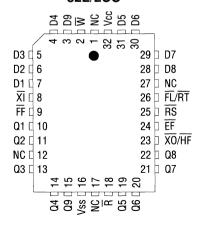
There are three types of FIFO's in the Micron family: Expandable, Mailbox Register, and Variable Flags. Expandable FIFO's are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFO's have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFO's allow the user to program the level of the full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

## PIN ASSIGNMENT (Top View)

## 28L DIP





# **1K x 9 FIFO**

## MAILBOX REGISTER

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS	MARKING
• Timing 25ns access time 30ns access time 35ns access time	-25 -30 -35
• Packages Plastic DIP	None
Ceramic DIP	С
Plastic LCC	EJ
Ceramic LCC	EC

## **GENERAL DESCRIPTION**

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

#### PIN ASSIGNMENT (Top View) **28L DIP** 28 Vcc D9 [ 27 h D5 D4 1 3 26 D6 D3 d 4 25 h D7 D2 d 5 24 h D8 23 h RT D1 d 6 MBS d 7 22 h RS FF d 8 21 | EF Q1 d 9 20 MBF 19 h Q8 Q2 d 10 Q3 d 11 Q7 Q4 d 12 17 h Q6 Q9 d 13 16 h Q5 15 🛭 R 32L/LCC D3 🛚 5 29 D D7 D2 d 6 28 D8 D1 🛮 7 27 D NC MBS 8 26 | RT FF D 9 25 RS 24 | EF Q1 d 10 Q2 d 11 23 MBF NC 🛮 12 22 D Q8 Q3 d 13 21 🛭 Q7 14 11 11 11 11 10 10 10 04 08 08 N N 08 08 08

# **1K x 9 FIFO**

**VARIABLE FLAGS** 

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- · Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS	MARKING		
Timing			
25ns access time	-25		
30ns access time	-30		
35ns access time	-35		
• Packages			
Plastic DIP	None		
Ceramic DIP	С		
Plastic LCC	EJ		
Ceramic LCC	EC		

#### **GENERAL DESCRIPTION**

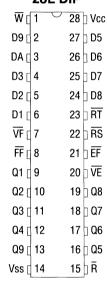
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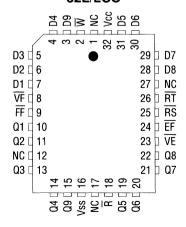
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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

## PIN ASSIGNMENT (Top View)

## **28L DIP**





	•	

# 1K x 16 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- · 16-bit word width
- · Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Easy expansion capability
- Automatic retransmit
- Low power

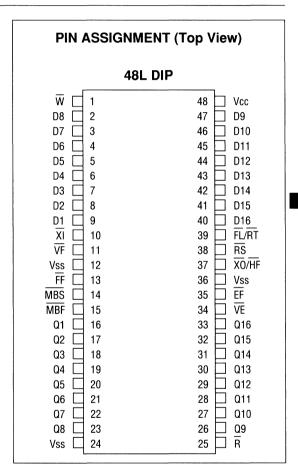
Transistor loads for maximum data integrity

OPTIONS	MARKING				
Timing					
25ns access time	-25				
30ns access time	-30				
35ns access time	-35				
• Packages					
Plastic DIP	None				
Ceramic DIP	C				

#### GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

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		,			
	*				

# 1K x 16 to 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- · Easy expansion capability
- · Automatic retransmit
- Low power
- Transistor loads for maximum data integrity
- One chip interface between a 16 bit bus and an 8 bit bus

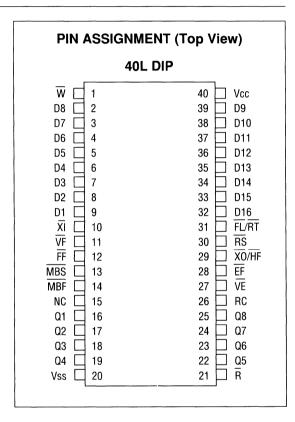
OPTIONS	MARKING			
Timing				
25ns access time	-25			
30ns access time	-30			
35ns access time	-35			
• Packages				
Plastic DIP	None			
Ceramic DIP	C			

# Ceramic DII

#### **GENERAL DESCRIPTION**

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

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# **2K x 8 FIFO**

VARIABLE FLAGS/MAILBOX REGISTER

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power

Ceramic DIP

• Transistor loads for maximum data integrity

OPTIONS	MARKING				
Timing					
25ns access time	-25				
30ns access time	-30				
35ns access time	-35				
• Packages					
Plastic DIP	None				

C

## **GENERAL DESCRIPTION**

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

## PIN ASSIGNMENT (Top View) **28L DIP** 28 h Vcc MBS | 2 27 h D5 D4 1 3 26 h D6 25 | D7 D3 d 4 D2 1 5 24 h D8 23 | RT D1 d 6 VF d 7 22 h RS FF d 8 21 h EF 20 h VE Q1 d 9 19 \quad Q8 $Q2 \, d \, 10$ Q3 d 11 18 | Q7 Q4 d 12 17 \( \) Q6 MBF 13 16 | Q5 15 | R



# 2K x 9 FIFO

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Industry standard pin-out
- · Empty and Full warning flags
- Asynchronous READ and WRITE
- Depth and Width expansion capability
- Automatic retransmit
- Low power consumption
- Transistor loads for maximum data integrity

OPTIONS	MARKING
Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

#### GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

#### PIN ASSIGNMENT (Top View) **28L DIP** 28 h Vcc 27 D5 D9 d 2 D4 d 3 26 h D6 D3 f 4 25 h D7 D2 | 5 24 D8 D1 d 23 h FL/RT **XI** ₫ 7 22 h RS FF 18 21 h EF Q1 d 9 20 \ XO/HF $02 \, \text{d} \, 10$ 19 h Q8 Q3 d 11 18 h Q7 Q4 I 12 17 \ Q6 Q9 d 13 16 \ Q5 15 | R Vss / 14 32L/LCC 29 h D7 D3 🗆 5 D2 d 6 28 D8 D1 🛮 7 27 D NC 26 | FL/RT FF d 25 | RS 9 24 🗆 EF Q1 [ 10 23 XO/HF Q2 🛮 11 NC [ 12 22 D Q8 21 🛭 Q7 Q3 🛚 13 14 15 17 17 19 20 04 09 NC NS NS 05 05

# **2K x 9 FIFO**

MAILBOX REGISTER

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Asynchronous READ and WRITE
- · Automatic retransmit
- Low power

**OPTIONS** 

Transistor loads for maximum data integrity

0 = 1 = 0 = 10	
Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

MARKING

## **GENERAL DESCRIPTION**

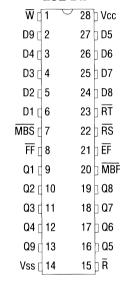
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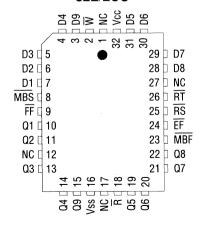
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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

## PIN ASSIGNMENT (Top View)

## 28L DIP





	* *		
		,	

# **2K x 9 FIFO**

**VARIABLE FLAGS** 

## **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- · Automatic retransmit
- Low power
- · Transistor loads for maximum data integrity

OPTIONS	MARKING
Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

## **GENERAL DESCRIPTION**

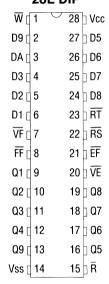
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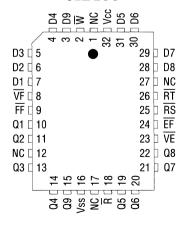
There are three types of FIFO's in the Micron family: Expandable, Mailbox Register, and Variable Flags. Expandable FIFO's are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFO's have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFO's allow the user to program the level of the full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

## PIN ASSIGNMENT (Top View)

## **28L DIP**





# 2K x 16 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- 16-bit word width
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- · Easy expansion capability
- · Automatic retransmit
- Low power

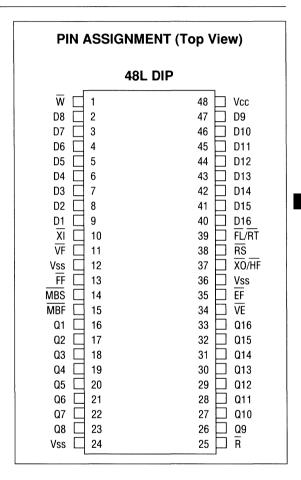
Transistor loads for maximum data integrity

OPTIONS	MARKING				
Timing					
25ns access time	-25				
30ns access time	-30				
35ns access time	-35				
• Packages					
Plastic DIP	None				
Ceramic DIP	C				

#### GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

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# 2Kx16 to 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

#### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Easy expansion capability
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity
- One chip interface between a 16 bit bus and an 8 bit bus

OPTIONS • Timing	MARKING
25ns access time	-25
30ns access time	-30
35ns access time	-35
Packages     Plastic DIP	None
Ceramic DIP	C

#### PIN ASSIGNMENT (Top View) 40L DIP $\overline{\mathsf{w}}$ 40 Vcc 2 D8 39 D9 3 D7 38 D10 D6 4 37 D11 D5 5 36 D12 6 D4 35 D13 D3 7 34 D14 D2 8 33 D15 D1 9 32 D16 Χī 10 31 FL/RT VF 11 30 RS FF 12 29 XO/HF MBS 13 28 ĒF MBF VF 14 27 NC 15 26 RC Q1 16 25 08 Q2 17 24 Ω7 03 18 23 Q6Q4 19 22 Q5 20 21 R Vss

## **GENERAL DESCRIPTION**

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

There are three types of FIFO's in the Micron family: Expandable, Mailbox Register, and Variable Flags. Expandable FIFO's are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFO's have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFO's allow the user to program the level of the full and empty flags.



# **FIFO**

# 4K x 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- · Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

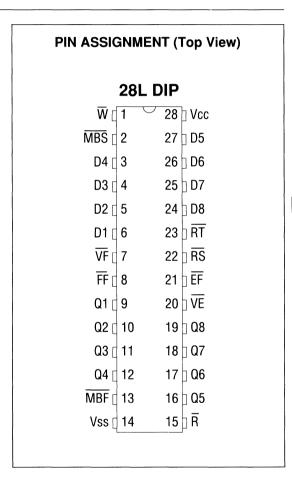
OPTIONS	MARKING
Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.





# MICRON

# **FIFO**

# 4K x 9 FIFO

### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Industry standard pin-out
- Empty and Full warning flags
- · Asynchronous READ and WRITE
- Depth and Width expansion capability
- Automatic retransmit
- Low power consumption
- Transistor loads for maximum data integrity

25ns access time 30ns access time 35ns access time Packages Plastic DIP Ceramic DIP Plastic LCC	MARKING				
Timing					
25ns access time	-25				
30ns access time	-30				
35ns access time	-35				
• Packages					
Plastic DIP	None				
Ceramic DIP	C				
Plastic LCC	EJ				
Ceramic LCC	EC				

### **GENERAL DESCRIPTION**

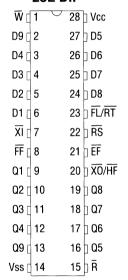
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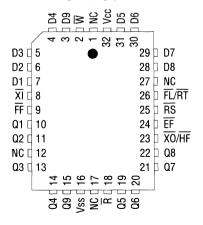
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### **PIN ASSIGNMENT (Top View)**

### **28L DIP**



### 32L/LCC





## **FIFO**

# 4K x 9 FIFO

### MAILBOX REGISTER

### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS	MARKINO
Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
Packages	
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Plastic LCC	EJ
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### PIN ASSIGNMENT (Top View) **28L DIP** ₩ 1 28 7 Vcc D9 d 2 27 h D5 D4 | 3 26 h D6 D3 d 4 25 h D7 24 h D8 D2 d 5 23 h RT D1 d 6 MBS | 7 22 h RS 21 h EF FF d 8 Q1 d 9 20 h MBF Q2 d 10 19 \ Q8 Q3 d 11 18 h Q7 Q4 d 12 17 \quad Q6 Q9 d 13 16 \ Q5 15 h R Vss 🛚 14 32L/LCC 32 33 30 30 29 h D7 D3 🛚 5 D2 d 6 28 D D8 D1 🛮 7 27 D NC 26 RT MBS d 8 FF d 9 25 | RS 24 | EF Q1 d 10 23 MBF $02 \, \text{d} \, 11$ NC | 12 22 D Q8 Q3 I 13 21 D Q7 14 15 16 17 17 19 20 04 09 NC NS NC 05 06

,

## **FIFO**

# **4K x 9 FIFO**

**VARIABLE FLAGS** 

### **FEATURES**

- High speed: 25ns access, 35ns cycle time
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS	MARKING
Timing	
25ns access time	-25
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• Packages	
Plastic DIP	None
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Ceramic LCC	EC

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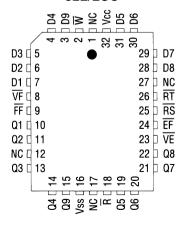
All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

### PIN ASSIGNMENT (Top View)

### **28L DIP**



### 32L/LCC



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### MICRON TECHNOLOGY

Micron Technology is one of the only manufacturers of military-grade memory components that offers 100% on-shore fabrication.

Located in Boise, Idaho, Micron currently maintains two wafer fabrication (fab) facilities with full assembly, test, quality assurance and failure analysis capabilities. Our third wafer fabrication facility, also located in Boise, is scheduled to begin production in 1989.

Micron's design rules for Fab I and II are 1.2 drawn and 1.0 micron effective. Under Fab III guidelines, this will progress down to 1.0 and 0.8 micron effective.

As a supplier to the defense electronics industry, Micron offers memory products certified to JAN 38510, DESC Standard Military Drawings (SMD) and 883 Rev. C Class B. Our wafer fabrication is currently certified to the level of 38510 for NMOS processes.

### MILITARY PRODUCTS — MICRON

Since 1987 Micron has been the sole source of JAN 38510 256K DRAMs. We have also introduced an 883 dual port DRAM (Video RAM) and the first  $256K \times 1$  and  $64K \times 4$  high-speed static RAMs. We will soon be introducing the industry's first SMD Video RAM.

As a leader in the high-density memory market, Micron is a founding participant in Sematech, a U.S. government sponsored consortium aimed at the memory needs of the defense industry. Plans for future devices include a 1 megabit static RAM, a 1 megabit video RAM and a 4 megabit DRAM. These devices are currently under development independent of Sematech or Defense Advanced Research Projects Agency (DARPA) support.

### MILITARY PRODUCTS — FUTURE REQUIREMENTS

In the area of radiation tolerance, Micron believes most contracts will require a defined level of radiation immunity. In response, we are currently testing SRAM and DRAM CMOS products through total dose, dose rate and single event upset.

We believe the defense industry is heading toward higher-density memory, faster speeds and more sophisticated "memory solutions." This may include a non-standard packaging concept specially designed for cooling or possibly higher density than currently available from a single component.

We also believe that the defense memory industry will move towards tighter processing geometries, new packaging concepts and more advanced hardware development through an interface of the component designer and the systems design engineer. Our processes, technology and marketing resources are poised to support such requirements.

### **MILITARY PRODUCT SELECTION GUIDE**

### DRAM

Memory	Optional			Power D	issipation	Packag	e and Numi	ber of Pins P	rocess	
Configuration	Access Cycle	Part Number	Access Time (ns)	Standby	Active	CDIP	CLCC	Flat Pack	Process	Page
64K x 1	Page Mode	MT4264 883	100,120,150	15mw	75mw	16	18	16	NMOS	7-5_
64K x 4	Page Mode	MT4067 883	100,120,150	15mw	150mw	16	18	16	NMOS	7-17
256K x 1	Page Mode	MT1259 883	100,120,150	15mw	150mw	16	18	16	NMOS	7-29
256K x 4	Fast Page Mode	MT4C4256 883	100,120,150	5mw	175mw	20	-	20	CMOS	7-41
1 Meg x 1	Fast Page Mode	MT4C1024 883	100,120,150	5mw	175mw	18	-	18	CMOS	7-53

### VRAM

Memory	Access	Part	Access	Power Di	ssipation	Package &	No. of Pins	
Configuration	Cycle	Number	Time (ns)	Standby	Active	CDIP	Process	Page
64K x 4	Page Mode	MT42C4064 883	120,150,200	10mw	150mw	24	CMOS	7-65

### SRAM

Memory	Control	Part	Access	Package &	Package & No. of Pins		
Configuration	Functions	Number	Time (ns)	CDIP	CLCC	Process	Page
2K x 8	CE & OE	MT5C1608 883	15 to 35	24	24	CMOS	7-95
8K x 8	CE1, CE2 & OE	MT5C6408 883	15 to 35	28	32	CMOS	7-103
16K x 1	CE only	MT5C1601 883	15 to 35	20	20	CMOS	7-111
16K x 4	CE only	MT5C6404 883	15 to 35	22	22	CMOS	7-119
32K x 8	CE & OE	MT5C2568 883	25 to 45	28	32	CMOS	7-127
64K x 1	CE only	MT5C6401 883	15 to 35	22	22	CMOS	7-135
64K x 4	CE only	MT5C2564 883	25 to 45	24	28	CMOS	7-141
256K x 1	CE only	MT5C2561 883	25 to 45	24	28	CMOS	7-149

# MILITARY DRAN

# MILITARY DRAM

# **64K x 1 DRAM**

### ADDITIONAL MILITARY SPECIFICATIONS

• SMD 82010

### **FEATURES**

- · Industry standard pin-out and timing
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby, 75mW active, typical
- Common I/O capability using "Early Write"
- Optional Page Mode access cycle
- Refresh modes: RAS only, CAS before RAS, and Hidden
- 256 cycle refresh distributed across 4ms
- Specifications guaranteed over full military DRAM temperature range (-55°C to +110°C)
- MIL-STD 883C processing

### **OPTIONS**

### MARKING

Process Level	
MIL-STD 883C (-55°C to +110°C)	883C
Parts processed to full requirements	
of MIL-STD-883C, method 5004	
and 5005	

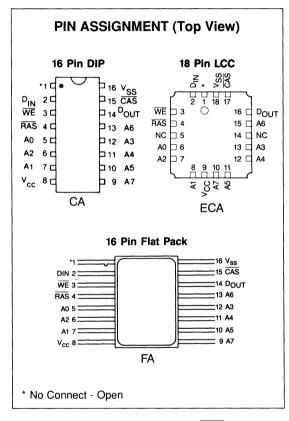
MIL-STD 883C with the exception M070 that final electrical testing is performed at 0°C to 70°C

Timing	
100ns access	-10
120ns access	-12
150ns access	-15

Packages:	
Ceramic DIP	C
Ceramic LCC	EC
Ceramic Flat Pack	F

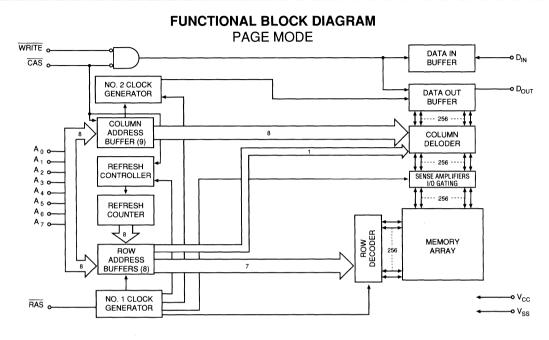
### **GENERAL DESCRIPTION**

The MT4264 883C is a randomly accessed solid-state memory containing 65,536 bits organized in a x1 configuration. The 16 address bits are entered 8 bits at a time using  $\overline{RAS}$  to latch the first 8 bits and  $\overline{CAS}$  the latter 8 bits. If the  $\overline{WE}$  pin goes low prior to  $\overline{CAS}$  going low, the output pin remains open until the next  $\overline{CAS}$  cycle. If  $\overline{WE}$  goes low after Data reaches the output pin, the output pin is activated and



retains the selected cell data as long as  $\overline{CAS}$  remains low (regardless of  $\overline{WE}$  or  $\overline{RAS}$ ). This late  $\overline{WE}$  pulse results in a READ-MODIFY-WRITE cycle. Data-in is latched when  $\overline{WE}$  strobes low.

By holding  $\overline{RAS}$  low,  $\overline{CAS}$  may be toggled to execute several faster READ, WRITE, READ-WRITE or READ-MODIFY-WRITE cycles within the  $\overline{RAS}$  address defined PAGE boundary. Returning  $\overline{RAS}$  high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high-time. Memory cell data is retained in its correct state by maintaining power and executing a  $\overline{RAS}$  (Refresh) cycle so that all 256 combinations of  $\overline{RAS}$  addresses are executed at least every 4 msec (regardless of sequence).



### **FUNCTIONAL TRUTH TABLE**

	510	010	we	Addr	esses		NOTES
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	Х	High Impedance	
READ	L	L	н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	X High Impedance		



### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any pin relative to Vss1.5V to +7.0V
Storage temperature range65°C to +150°C
Power Dissipation 1 Wat
Lead temperature (soldering 5 sec.)300°C
Juction temperature (Tj)+150°C
Short Circuit Output Current50mA
Thermal resistance (θic) 16 pin DIP50°C/W

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### DC ELECTRICAL PERORMANCE CHARACTERISTICS

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Current from Vcc (active); RAS and CAS = Cycling; TRC = TRC(MIN)	lcc1		40	mA	3
Supply Current from Vcc (active, page mode); $\overline{RAS} = VIL$ , $\overline{CAS} = Cycling$ ; $TPC = TPC(MIN)$	Icc2		40	mA	3
Supply Current from Vcc (standby); RAS and CAS = ViH	Іссз		6	mA	
Supply Current from Vcc (refresh, RAS only); RAS = Cycling: CAS = Vih	Icc4		30	mA	3
Output High Voltage (Iон = -5mA)	<b>V</b> он	2.4		V	1
Output Low Voltage (IoL = 5mA)	Vol		0.4	V	1
Input Leakage	Іін	-10	10	μА	
Any input (0V ≤ Vın ≤ Vcc), all other pins = 0V	lıL	-10	10	μА	
Output Leakage (0 ≤ Voυτ ≤ Vcc)	loz	-10	10	μА	

### RECOMMENDED DC OPERATING CONDITIONS

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc Supply Voltage	Vcc	4.5	5.5	٧	
Vss power supply and signal reference	Vss	0.0	0.0	٧	1
High level input voltage (all inputs)	Vih	2.4	Vcc+1	V	1
Low level input voltage (all inputs)	VIL	-1.0	0.8	٧	1
Operating Case Temperature	Tc	-55	+110	°C	

### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As), DIN	C <sub>11</sub>		5	pF	3
Input Capacitance RAS, CAS, WE	CI2		8	pF	3
Output Capacitance Dout	Co		8	pF	3

# **MILITARY DRAM**

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 8) (-55°C  $\leq$  T<sub>C</sub>  $\leq$  110°C, Vcc = 5.0V  $\pm$ 10%)

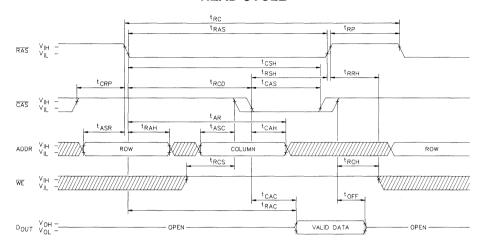
A.C. CHARACTERISTICS		-	10		12		15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	195		230		250		ns	
READ-MODIFY-WRITE cycle time	<sup>t</sup> RWC	230		255		270		ns	
PAGE-MODE cycle time	t <sub>PC</sub>	90		100		120		ns	18
Access time from RAS	t <sub>RAC</sub>		100		120		150	ns	9
Access time from CAS	tCAC		50		60		75	ns	10
RAS pulse width	t <sub>RAS</sub>	100	10,000	120	10,000	150	10,000	ns	
CAS pulse width	t <sub>CAS</sub>	50	10,000	60	10,000	75	10,000	ns	
RAS precharge time	t <sub>RP</sub>	80		90		90		ns	
CAS precharge time	t <sub>CPN</sub>	25		25		30		ns	11,19
CAS precharge time (PAGE-MODE)	<sup>t</sup> CP	30		30		40		ns	
RAS to CAS delay time	t <sub>RCD</sub>	25	50	25	60	35	75	ns	12
RAS hold time	t <sub>RSH</sub>	50		60		75		ns	
CAS hold time	tcsh	110		120		150		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		ns	19
Row address hold time	t <sub>RAH</sub>	15		15		20		ns	
Column address set-up time	t <sub>ASC</sub>	0		0		0		ns	19
Column address hold time	t <sub>CAH</sub>	20		20		25		ns	
Column address hold time	t <sub>AR</sub>	70		80		100		ns	
referenced to RAS			1	İ					
READ command set-up time	t <sub>RCS</sub>	0		0		0		ns	19
READ command hold time	t <sub>RCH</sub>	0		0		0		ns	13, 19
referenced to CAS			1	{		ĺ	1	ľ	
READ command hold time	t <sub>RRH</sub>	10		10		10		ns	
referenced to RAS									
Output disable delay	<sup>t</sup> OFF	0	35	0	30	0	35	ns	14
WRITE command set-up time	twcs	0		0		0		ns	15
WRITE command hold time	twch	35		40		45		ns	
WRITE command hold time	tWCR	85		100		120		ns	
referenced to RAS									
WRITE command pulse width	twP	35		40		45		ns	
WRITE command to RAS lead time	<sup>t</sup> RWL	35		40		45		ns	
WRITE command to CAS lead time	tCWL	35		40		45		ns	
Data-in set-up time	t <sub>DS</sub>	0		0_		0		ns	16, 19
Data-in hold time	t <sub>DH</sub>	35		40	<u> </u>	45		ns	16
Data-in hold time	t <sub>DHR</sub>	85		100		120		ns	
referenced to RAS			1						
CAS to WRITE delay	tCWD	40		50		60		ns	15
RAS to WRITE delay	t <sub>RWD</sub>	90		110		135		ns	15
Transition time (rise or fall)	t <sub>T</sub>	3	100	3	100	3	100	ns	6, 7
CAS to RAS set-up time	t <sub>CRP</sub>	10		10		10		ns	
Refresh Period (256 cycles distributed)	tREFD		4		4		4	ms	17
Refresh Period (256 cycles burst)	tREFB		4	1	4	1	4	ms	18

### **NOTES**

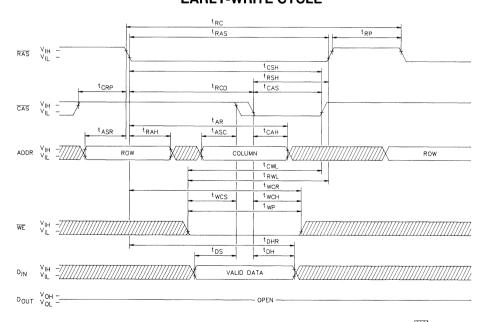
- 1. Vss is common for all voltages.
- 2. This parameter is sampled, not 100% tested. Capacitance calculated from the equation C =  $\frac{I\Delta t}{\Delta V}$ 
  - with  $\Delta V = 3V$  and Vcc = 5V.
- 3. Specified values are obtained with the output load equal to 2TTL loads and 100pF to Vss.
- An initial pause of 100μs is required after power-up followed by any 8 RAS cycles, (READ, WRITE, READ-MODIFY-WRITE, RAS refresh) before proper device operation is assured.
- 5. AC characteristics assume transistion time ( ${}^{t}T$ ) = 5ns.
- 6. VIL (max) and VIH (min) are reference levels for measuring timing of input signals. Transition times are measured between VIL and VIH.
- 7. In addition to meeting the transition rate specification, all input signals must transit between VIL and VIH (or between VIH and VIL) in a monotonic manner.
- If CAS = VIH, data output is high impedance. If CAS = VIL, data output may contain data from the last valid READ cycle.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 10. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 11. If  $\overline{\text{CAS}}$  is low at the falling edge of  $\overline{\text{RAS}}$ , DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for <sup>t</sup>CP. Note 9 applies to determine valid data out.
- 12. Operation within <sup>t</sup>RCD (max) limit ensures the <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access is controlled excusively by <sup>t</sup>CAC.

- 13.  ${}^{t}RCH$  is referenced to the first rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ .
- 14. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 15. <sup>t</sup>WCS, <sup>t</sup>CWD and <sup>t</sup>RWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) and <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the conditions of the data out (at access time and until CAS goes back to Vih) is indeterminate.
- 16. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles and to the  $\overline{\text{WE}}$  leading edge in late WRITE or READ-MODIFY-WRITE cycles.
- 17. Å 256 cycle distibuted refresh consists of an address location refresh cycle being performed within 15.625µS so that all 256 RAS address combinations are executed within 4ms (regardless of sequence). Micron recommends distributed refresh.
- 18. A 256 cycle burst refresh consists of refreshing, as rapidly as minimum cycle time allows, all 256 combinations of RAS addresses (regardless of sequence). The refresh mode must be executed within 4ms.
- 19. This parameter is "conditionally" guaranteed parameter that is specified to aid with device application. It is not directly verified by a specific test but is used, with several other parameters, in the performance verification of other attributes.

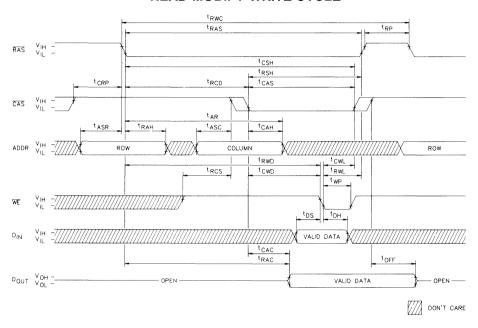
### **READ CYCLE**



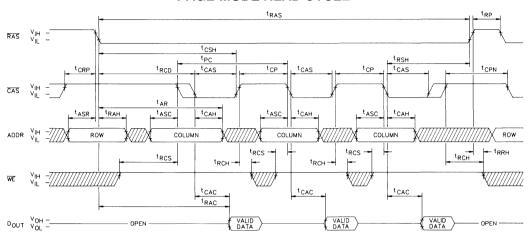
### **EARLY-WRITE CYCLE**



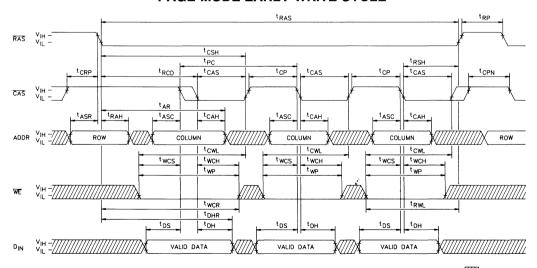
# READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE



### **PAGE-MODE READ CYCLE**

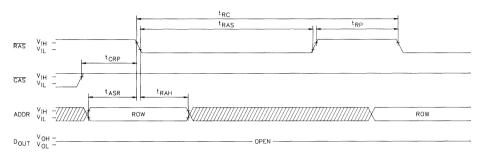


### **PAGE-MODE EARLY-WRITE CYCLE**

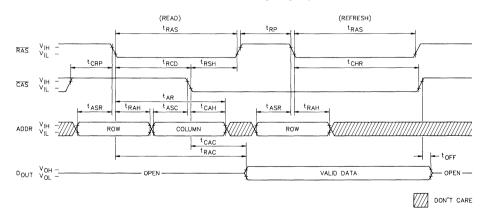




# RAS ONLY REFRESH CYCLE $(ADDR = A_0 - A_7)$



### **HIDDEN REFRESH CYCLE**



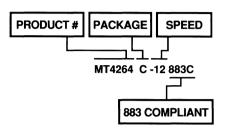
### MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

	MICRON MIL	-STD 883C PRODUCT ASSURANC	E FLOW
Description of Requirements and Scr		ethods and Test onditions	Comment
General MIL-M-38510			
1. MIL-STD 883, Class I	a pla	tablish and implement product assurance program an and qualification test plan d submit to qualifying activity.	Approved by DESC
<ol> <li>Certification</li> <li>Traceability</li> <li>Country of Origin (Not required for 883)</li> </ol>	Ma Tro Na	anufacturer's QA survey aceable to wafer production lot.	Self audit Computer lot history records Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD 883 Fabrication	on		
5. Incoming Inspections Direct Materials	s All M	IL-STD-105D	In-line
6. Wafer Fabrication		ethod 2018	100%
7. Assembly	Cl	ass B Process Monitors	100%
MIL-STD 883, Class B,	Rev. C, Method 50	04 Screening	
8. Internal Visual	Me	ethod 2010, cond. B	100%
9. Stabilization Bake		ethod 1008, cond. C	100%
10. Temperature Cycle		ethod 1010, cond. C	100%
11. Constant Acceleration	on M	ethod 2001, cond. E	100%
12. Hermeticity			1000
A. Fine Leak		ethod 1014, cond. A	100%
B. Gross Leak		ethod 1014, cond. C	100%
13. Initial Electricals	da	anufacturer's documented ta sheet @ +118°C	100%
14. Marking		ethod 2015	100%
15. Burn-in		ethod 1015, subgroups A-2 for endpoint 2 hours @ 125°C	100%
16. Final Electrical Post		ethod 5004, Class B,	100%
Burn-in Test		1.16 @ -55°C, +25°C, +113°C	
		6 PDA and in-line Group A	
17 External Visual		er method 5005	1000
17. External Visual		ethod 2009	100% 100%
18. Pack/Ship		cludes C of C, with QCI ta (attributes only)	100%
19. Quality Conformano Inspection		ethod 5005 in-line Class B	Groups A, B, C, D
Quality Conformance I	nspection per Met	thod 5005 (attributes data only)	
19. Group A		anufacturer's documented	
20. Group B	Pa	nta sheet nckage functional and nstruction tests	Each lot/sublot Each package type on each lot
21. Group C	D:	ie related	Generic every 13 weeks
22. Group D		000 hr. operating life) ackage related test	Each package type Generic every 26 weeks



### **ORDER INFORMATION**

64Kx1, 120ns access, -55°C to +110°C, in Ceramic DIP



The Micron MT4264-883C serves the special needs of the Defense/Aerospace market. The Micron Military Product Assurance Program provides state-of-the-art screened to MIL-STD-883C Class B Revision C Methods 5004 and 5005. All IC's furnished under this program are produces on certified lines and are manufactured, assembled, tested quality controlled in Micron's modern Boise, Idaho USA facility.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

# MILITARY DRAM

# **64K x 4 DRAM**

### ADDITIONAL MILITARY SPECIFICATIONS

• SMD 87676

### **FEATURES**

- · Industry standard pin-out and timing
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby, 150mW active, typical
- Optional Page Mode access cycle
- Refresh modes: RAS only, CAS before RAS, and Hidden
- 256 cycle refresh distributed across 4ms
- Specifications guaranteed over full military DRAM temperature range (-55°C to +110°C)
- MIL-STD 883C processing

### **OPTIONS**

Ceramic LCC

### MARKING

EC.

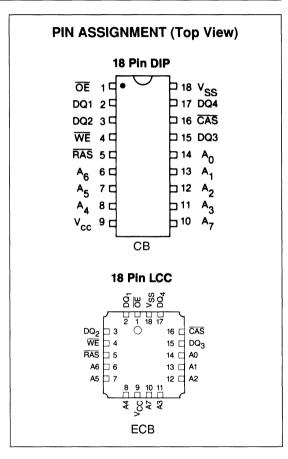
Process Level
 MIL-STD 883C (-55°C to +110°C)
 Parts processed to full requirements
 of MIL-STD 883C, method 5004
 and 5005

MIL-STD 883C with the exception	M070
that final electrical testing is	
performed at 0°C to 70°C	

Timing	
100ns access	-10
120ns access	-12
150ns access	-15
• Packages:	
Ceramic DIP	C

### **GENERAL DESCRIPTION**

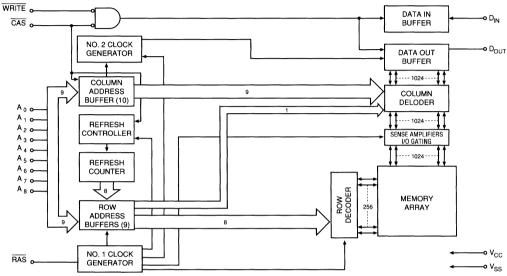
The MT4067 883C is a randomly accessed solid-state memory containing 262,144 bits organized in a 65,536 word x4 configuration. The 16 address bits are entered 8 bits at a time using  $\overline{RAS}$  to latch the first 8 bits and  $\overline{CAS}$  the latter 8 bits. If  $\overline{WE}$  goes low after Data reaches the output pin, the output pin is activated and retains the selected cell data as long as  $\overline{CAS}$  and  $\overline{OE}$  remains low (regardless of  $\overline{WE}$ 



or  $\overline{RAS}$ ). This late  $\overline{WE}$  pulse results in a READ-MODIFY-WRITE cycle. Data-in is latched when  $\overline{WE}$  strobes low.

By holding  $\overline{RAS}$  low,  $\overline{CAS}$  may be toggled to execute several faster READ, WRITE, or READ-MODIFY-WRITE cycles within the  $\overline{RAS}$  address defined PAGE boundary. Returning  $\overline{RAS}$  high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high-time. Memory cell data is retained in its correct state by maintaining power and executing a  $\overline{RAS}$  (Refresh) cycle so that all 256 combinations of  $\overline{RAS}$  addresses are executed at least every 4 msec (regardless of sequence).

# **FUNCTIONAL BLOCK DIAGRAM** PAGE MODE



### **FUNCTIONAL TRUTH TABLE**

F	540		WE	Addr	esses		NOTEO
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Χ	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Х	Х	High Impedance	

# MICRON

### **ABSOLUTE MAXIMUM RATINGS\***

TIDO CECTE IVII DI IVI IVI IVI IVI IVI IVI IVI IVI	
Voltage on any pin relative to Vss1.5	V to +7.0V
Storage temperature range65°C	to +150°C
Power Dissipation	1 Watt
Lead temperature (soldering 5 sec.)	300°C
Juction temperature (Tj)	+150°C
Short Circuit Output Current	50mA
Thermal resistance (θjc) 16 pin DIP	

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### DC ELECTRICAL PERORMANCE CHARACTERISTICS

(Notes: 3,4,6,7) (-55°C  $\leq$  T<sub>C</sub>  $\leq$  =110°C) (Vcc = 5.0V  $\pm$ 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Current from Vcc (active); $\overline{RAS}$ and $\overline{CAS}$ = Cycling; $TRC = TRC(MIN)$	Icc1		55	mA	2
Supply Current from Vcc (active, page mode); $\overline{RAS}$ = V <sub>I</sub> L, $\overline{CAS}$ = Cycling; TPC = TPC(MIN)	lcc2		55	mA	2
Supply Current from Vcc (standby); RAS and CAS = ViH	Іссз		8	mA	
Supply Current from Vcc (refresh, $\overline{RAS}$ only); $\overline{RAS}$ = Cycling: $\overline{CAS}$ = V <sub>IH</sub>	ICC4		45	mA	2
Supply Current from Vcc (refresh, $\overline{CAS}$ -before- $\overline{RAS}$ ); $\overline{RAS}$ and $\overline{CAS}$ = cycling	lcc5		55	mA	2
Output High Voltage (Iон = -5mA)	<b>V</b> он	2.4		V	1
Output Low Voltage (IoL = 5mA)	Vol		0.4	V	1
Input Leakage	Іін	-10	10	μΑ	
Any input $(0V \le V in \le V cc)$ , all other pins = $0V$	lıL	-10	10	μΑ	
Output Leakage (0 ≤ Vouт ≤ Vcc)	loz	-10	10	μΑ	

### RECOMMENDED DC OPERATING CONDITIONS

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc Supply Voltage	Vcc	4.5	5.5	٧	
Vss power supply and signal reference	Vss	0.0	0.0	٧	1
High level input voltage (all inputs)	Vih	2.4	Vcc+1	٧	1
Low level input voltage (all inputs)	VIL	-1.0	0.8	٧	1
Operating Case Temperature	Tc	-55	+110	°C	

### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As), DIN	Cıı		5	pF	3
Input Capacitance RAS, CAS, WE, OE	C <sub>12</sub>		8	pF	3
Output Capacitance Dout	Co		7	pF	3



### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 3, 4, 5, 6, 7, 8) (-55°C  $\leq$  T<sub>C</sub>  $\leq$  +110°C, Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS			10		12		15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	195		220		250		ns	
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	250		290		315		ns	20
PAGE-MODE cycle time	t <sub>PC</sub>	90		100		120		ns	20
Access time from RAS	tRAC		100		120		150	ns	9
Access time from CAS	t <sub>CAC</sub>		50		60		75	ns	10
RAS pulse width	t <sub>RAS</sub>	100	10,000	120	10,000	150	10,000	ns	
CAS pulse width	tCAS	50	10,000	60	10,000	75	10,000	ns	
RAS precharge time	t <sub>RP</sub>	80		90		90		ns	
RAS hold time	t <sub>RSH</sub>	50		60		75		ns	
RAS to CAS delay time	t <sub>RCD</sub>	25	50	30	60	30	75	ns	
CAS precharge time	<sup>t</sup> CPN	25		25		30	,	ns	20
CAS precharge time (PAGE-MODE)	<sup>t</sup> CP	30		30		35		ns	11
CAS to RAS set-up time	<sup>t</sup> CRP	5		5		5		ns	
CAS hold time	tCSH	110		120		150		ns	
Row address set-up time	†ASR	0		0		0		ns	20
Row address hold time	t <sub>BAH</sub>	15		20		20		ns	
Column address set-up time	†ASC	0		0		0		ns	20
Column address hold time	<sup>t</sup> CAH	20		30		30		ns	
Column address hold time reference to RAS	tAR.	70		80		100		ns	
READ command set-up time	t <sub>RCS</sub>	0		0		0		ns	20
READ command hold time	t <sub>RCH</sub>	0	1	0	1	0		ns	20
referenced to CAS	1.7.7.		1		1				
READ command hold time	t <sub>RRH</sub>	10		10		10		ns	
referenced to RAS			1	}		,		ļ	
Output disable delay	<sup>t</sup> OFF	0	40	0	40	0	40	ns	12
Output disable	t <sub>OD</sub>		35		40		40	ns	
Output enable	t <sub>OE</sub>		25		25		30	ns	13
WRITE command set-up time	twcs	0		0		0		ns	14
WRITE command hold time	tWCH	35		40		45		ns	
WRITE command hold time	tWCR	85		100		120		ns	
referenced to RAS				ļ			1		
WRITE command pulse width	<sup>t</sup> WP	35		40		45		ns	
WRITE command to RAS lead time	t <sub>RWL</sub>	35		40		45		ns	
WRITE command to CAS lead time	tCWL	35		40		45		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	15, 20
Data-in hold time	t <sub>DH</sub>	35		40		45		ns	15
Data-in hold time referenced to RAS	t <sub>DHR</sub>	85	1	100		120		ns	
CAS to WRITE delay	tCWD	40		50		60		ns	14,16,20
RAS to WRITE delay	t <sub>RWD</sub>	90		110		135		ns	14,16,20
Transition time (rise or fall)	t <sub>T</sub>	3	100	3	100	3	100	ns	
CAS set-up time	<sup>t</sup> CSR	10		10		10		ns	17
(CAS-before-RAS refresh)		}			1				
CAS hold time	tCHR	20		25		30		ns	17
(CAS-before-RAS refresh)		-		1				-	
Refresh Period (256 cycles distributed)	t <sub>REFD</sub>		4		4		4	ms	18
Refresh Period (256 cycles burst)	tREFB		4		4		4	ms	19

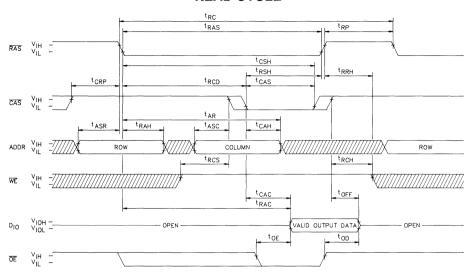
# MILITARY DRAM

### NOTES

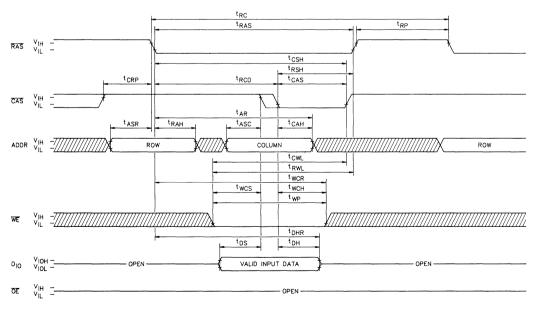
- 1. Vss is common for all voltages.
- Specified values are obtained with the output load equal to 2TTL loads and 100pF to Vss.
- 3. This parameter is sampled, not 100% tested. Capacitance calculated from the equation  $C = I\Delta t$   $\Delta V$ 
  - with  $\Delta V = 3V$  and Vcc = 5V.
- An initial pause of 100μs is required after power-up followed by any 8 RAS cycles, (READ, WRITE, READ-MODIFY-WRITE, RAS refresh) before proper device operation is assured.
- 5. AC characteristics assume transistion time  $({}^{t}T) = 5$ ns.
- VIL (max) and VIH (min) are reference levels for measuring timing of input signals. Transition times are measured between VIL and VIH.
- In addition to meeting the transition rate specification, all input signals must transit between VIL and VIH (or between VIH and VIL) in a monotonic manner.
- 8. If  $\overline{CAS} = V_{IH}$  or  $\overline{OE} = V_{IH}$ , data output is high imped ance. If  $\overline{CAS} = V_{IL}$  and  $\overline{OE} = V_{IL}$ , data output may contain data from the last valid READ cycle.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 10. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 11. If  $\overline{\text{CAS}}$  is low at the falling edge of  $\overline{\text{RAS}}$ , DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for  $^{\text{t}}\text{CP}$ . Note 8 applies to determine valid data out.
- 12. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to Voн or Vol.
- 13. If  $\overline{OE}$  is taken LOW then HIGH DOUT goes open. If  $\overline{OE}$  is tied permanently LOW a READ-WRITE or

- READ-MODIFY-WRITE operation requires a separate READ and WRITE cycle.
- 14. <sup>t</sup>WCS, <sup>t</sup>CWD and <sup>t</sup>RWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) and <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the conditions of the data out (at access time and until CAS goes back to VIH) is indeterminate.
- 15. These parameters are referenced to CAS leading edge in early WRITE cycles and to the WE leading edge in late WRITE or READ-MODIFY-WRITE cycles.
- 16. During a READ-WRITE or READ-MODIFY-WRITE cycle the minimum specifications for <sup>t</sup>RWD and <sup>t</sup>CWD must be modified by adding 40 ns to each specification due to OE delay.
- 17. Enables on-chip refresh and address counters.
- 18. A 256 cycle distibuted refresh consists of an address location refresh cycle being performed within 15.625μS so that all 256 RAS address combinations are executed within 4ms (regardless of sequence). Micron recommends distributed refresh.
- 19. A 256 cycle burst refresh consists of refreshing, as rapidly as minimum cycle time allows, all 256 combinations of RAS addresses (regardless of sequence). The refresh mode must be executed within 4ms.
- 20. This parameter is "conditionally" guaranteed parameter that is specified to aid with device application. It is not directly verified by a specific test but is used, with several other parameters, in the performance verification of other attributes.

### **READ CYCLE**

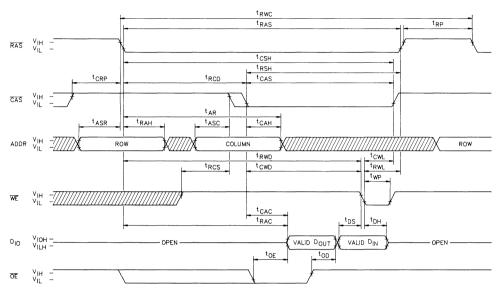


### **EARLY-WRITE CYCLE**

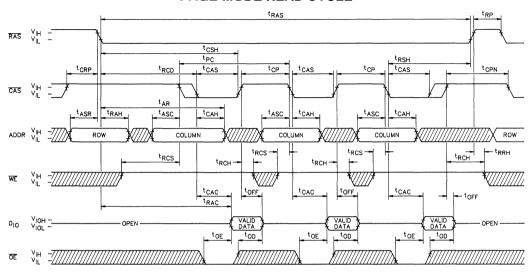




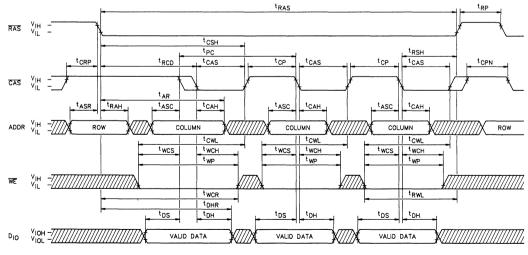
# READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE



### PAGE-MODE READ CYCLE

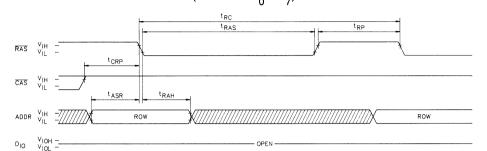


### PAGE-MODE EARLY-WRITE CYCLE



# MILITARY

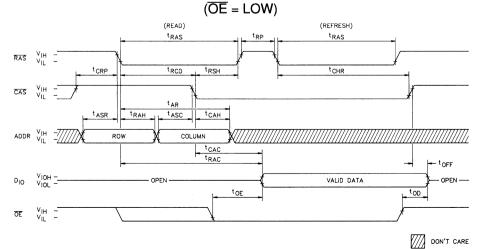
# RAS ONLY REFRESH CYCLE $(ADDR = A_0 - A_7)$



# CAS-BEFORE-RAS REFRESH CYCLE (ADDRESS INPUTS ARE IGNORED)



### HIDDEN REFRESH CYCLE



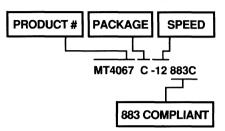


Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan and submit to qualifying activity.	Approved by DESC
<ol> <li>Certification</li> <li>Traceability</li> <li>Country of Origin (Not required for 883C)</li> </ol>	Manufacturer's QA survey Traceable to wafer production lot. N/A	Self audit Computer lot history records Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD 883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication 7. Assembly	Method 2018 Class B Process Monitors	100% 100%
MIL-STD 883, Class B, Rev. C, Me	thod 5004 Screening	
8. Internal Visual 9. Stabilization Bake 10. Temperature Cycle 11. Constant Acceleration	Method 2010, cond. B Method 1008, cond. C Method 1010, cond. C Method 2001, cond. E	100% 100% 100% 100%
<ul><li>12. Hermeticity</li><li>A. Fine Leak</li><li>B. Gross Leak</li><li>13. Initial Electricals</li></ul>	Method 1014, cond. A Method 1014, cond. C Manufacturer's documented	100% 100% 100%
14. Marking 15. Burn-in	data sheet @ +118°C Method 2015 Method 1015, subgroups A-2 for endpoint 162 hours @ 125°C	100%
16. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +113°C 5% PDA and in-line Group A per method 5005	100%
17. External Visual 18. Pack/Ship	Method 2009 Includes C of C, with QCI data (attributes only)	100% 100%
19. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection	per Method 5005 (attributes data only)	
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and construction tests	Each package type on each lot
21. Group C	Die related (1000 hr. operating life)	Generic every 13 weeks
22. Group D	Package related test	Each package type Generic every 26 weeks



#### ORDER INFORMATION

64Kx4, 120ns access, -55°C to +110°C, in Ceramic DIP



The Micron MT4067-883C serves the special needs of the Defense/Aerospace market. The Micron Military Product Assurance Program provides state-of-the-art screened to MIL-STD 883C Class B Revision C Methods 5004 and 5005. All IC's furnished under this program are produces on certified lines and are manufactured, assembled, tested quality controlled in Micron's modern Boise, Idaho USA facility.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

## MILITARY DRAM

## 256K x 1 DRAM

#### ADDITIONAL MILITARY SPECIFICATIONS

- SMD 85152
- JAN M38150/246

#### **FEATURES**

- · Industry standard pin-out and timing
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby, 150mW active, typical
- Common I/O capability using "Early Write"
- Optional Page Mode access cycle
- Refresh modes: RAS only, CAS before RAS, and Hidden
- 256 cycle refresh distributed across 4ms
- Specifications guaranteed over full military DRAM temperature range (-55°C to +110°C)
- MIL-STD 883C processing

#### **OPTIONS**

Timing

#### MARKING

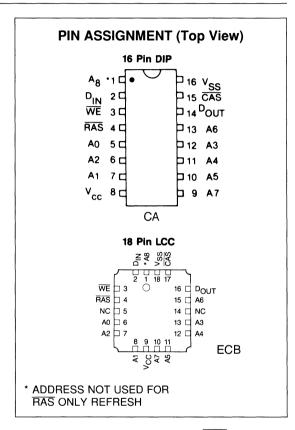
•	Process Level	
	MIL-STD 883C (-55°C to +110°C)	883C
	Parts processed to full requirements	
	of MIL-STD 883C, method 5004	
	and 5005	

MIL-STD 883C with the exception M070 that final electrical testing is performed at 0°C to 70°C

100ns access	-10
120ns access	-12
150ns access	-15
• Packages:	
Ceramic DIP	C
Ceramic LCC	EC

#### **GENERAL DESCRIPTION**

The MT1259 883C is a randomly accessed solid-state memory containing 262,144 bits organized in a x1 configuration. The 18 address bits are entered 9 bits at a time using RAS to latch the first 9 bits and CAS the latter 9 bits. If the WE pin goes low prior to CAS going low, the output pin remains open until the next CAS cycle. If WE goes low after Data reaches the output pin, the output pin is activated and



retains the selected cell data as long as  $\overline{CAS}$  remains low (regardless of  $\overline{WE}$  or  $\overline{RAS}$ ). This late  $\overline{WE}$  pulse results in a READ-MODIFY-WRITE cycle. Data-in is latched when  $\overline{WE}$  strobes low.

By holding  $\overline{RAS}$  low,  $\overline{CAS}$  may be toggled to execute several faster READ, WRITE, READ-WRITE or READ-MODIFY-WRITE cycles within the  $\overline{RAS}$  address defined PAGE boundary. Returning  $\overline{RAS}$  high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the  $\overline{RAS}$  high-time. Memory cell data is retained in its correct state by maintaining power and executing a  $\overline{RAS}$  (Refresh) cycle so that all 256 combinations of  $\overline{RAS}$  addresses are executed at least every 4 msec (regardless of sequence).

**⊸** ∨<sub>SS</sub>

#### **FUNCTIONAL BLOCK DIAGRAM** PAGE MODE WRITE . DATA IN → D<sub>IN</sub> CAS **BUFFER** NO. 2 CLOCK ⊸ D<sub>OUT</sub> GENERATOR DATA OUT BUFFER 1024----COLUMN ADDRESS BUFFER (10) 9 COLUMN DELODER A 0 0 A 1 0-. ---- 1024---REFRESH A 2 0-SENSE AMPLIFIERS I/O GATING CONTROLLER A 3 o-A 4 0---- 1024 ---A 5 0-REFRESH A 6 0-COUNTER A 7 0-A 8 0-ROW DECODER **MEMORY** 256 ROW ARRAY ADDRESS 8 BUFFERS (9) **-∘** ∨<sub>cc</sub> NO. 1 CLOCK

#### **FUNCTIONAL TRUTH TABLE**

GENERATOR

	B10			Addr	esses		
Function	RAS	CAS	WE	tR	tC		NOTES
Standby	Н	Н	Н	Х	Х	High Impedance	
READ	L	L	Н	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	Н	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	х	х	High Impedance	



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any pin relative to Vss	1.5V to +7.0V
Storage temperature range	
Power Dissipation	1 Watt
Lead temperature (soldering 5 sec.)	300°C
Juction temperature (Tj)	+150°C
Short Circuit Output Current	50mA
Thermal resistance (θjc) 16 pin DIP	

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL PERORMANCE CHARACTERISTICS

(Notes: 3,4,6,7) (-55°C  $\leq$  T  $_{C} \leq$  =110°C) (Vcc = 5.0V  $\pm 10\%$ )

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Current from Vcc (active); RAS and CAS = Cycling; TRC = TRC(MIN)	lcc <sub>1</sub>		55	mA	2
Supply Current from Vcc (active, page mode); $\overline{RAS} = V_{IL}$ , $\overline{CAS} = Cycling$ ; $T_{PC} = T_{PC}(MIN)$	lcc2		55	mA	2
Supply Current from Vcc (standby);  RAS and CAS = VIH	lcc3		8	mA	2
Supply Current from Vcc (refresh, RAS only); RAS = Cycling: CAS = Vih	Icc4		45	mA	2
Supply Current from Vcc (refresh, $\overline{CAS}$ -before- $\overline{RAS}$ ); $\overline{RAS}$ and $\overline{CAS}$ = cycling	lcc5		55	mA	2
Output High Voltage (Iон = -5mA)	<b>V</b> он	2.4		V	1
Output Low Voltage (IoL = 5mA)	Vol		0.4	V	1
Input Leakage	lін	-10	10	μA	
Any input (0V ≤ VIN ≤ Vcc), all other pins = 0V	liL	-10	10	μA	
Output Leakage (0 ≤ Vouт ≤ Vcc)	loz	-10	10	μA	

#### RECOMMENDED DC OPERATING CONDITIONS

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc Supply Voltage	Vcc	4.5	5.5	٧	
Vss power supply and signal reference	Vss	0.0	0.0	٧	1
High level input voltage (all inputs)	Vih	2.4	Vcc+1	٧	1
Low level input voltage (all inputs)	VIL	-1.0	0.8	٧	1
Operating Case Temperature	Tc	-55	+110	°C	

#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-As), DIN	Cl1		5	pF	3
Input Capacitance RAS, CAS, WE	C <sub>12</sub>		8	pF	3
Output Capacitance Dout	Co		7	pF	3

MICHON

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 3, 4, 5, 6, 7, 8) (-55°C $\leq$ T $_{C}$ $\leq$ +110°C, Vcc = 5.0V $\pm10\%$ )

A.C. CHARACTERISTICS			10		12		15	<del> </del>	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t <sub>RC</sub>	195		220		250		ns	
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	230		250		275		ns	
PAGE-MODE cycle time	<sup>t</sup> PC	90		100		120		ns	18
Access time from RAS	t <sub>RAC</sub>		100		120		150	ns	9
Access time from CAS	t <sub>CAC</sub>		50		60		75	ns	10
RAS pulse width	t <sub>RAS</sub>	100	10,000	120	10,000	150	10,000	ns	
CAS pulse width	t <sub>CAS</sub>	50	10,000	60	10,000	75	10,000	ns	
RAS precharge time	t <sub>RP</sub>	80		90		90		ns	
RAS hold time	<sup>t</sup> RSH	50		60		75		ns	
RAS to CAS delay time	t <sub>RCD</sub>	30	50	30	60	30	75	ns	
CAS precharge time	<sup>t</sup> CPN	25		25		30		ns	18
CAS precharge time (PAGE-MODE)	<sup>t</sup> CP	30		30		35		ns	11
CAS to RAS set-up time	t <sub>CRP</sub>	5		5		5		ns	
CAS hold time	t <sub>CSH</sub>	110		120		150		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		ns	18
Row address hold time	t <sub>RAH</sub>	15		20		20		ns	
Column address set-up time	t <sub>ASC</sub>	0		0		0		ns	18
Column address hold time	<sup>t</sup> CAH	20		30		30		ns	
Column address hold time referenced to RAS	<sup>t</sup> AR	70		80		100		ns	
	tRCS	-			-		1		10
READ command set-up time	t <sub>RCH</sub>	0	-	0	<del></del>	0		ns	18
READ command hold time referenced to CAS		0		0		0		ns	18
READ command hold time	t <sub>RRH</sub>	10		10		10		ns	
referenced to RAS									
Output disable delay	t <sub>OFF</sub>	0	40	0	40	0	40	ns	12
WRITE command set-up time	twcs	0		0		0		ns	13
WRITE command hold time	tWCH	35		40		45		ns	
WRITE command hold time referenced to RAS	<sup>t</sup> WCR	85		100		120		ns	
WRITE command pulse width	t <sub>WP</sub>	35		40		45		ns	
WRITE command to RAS lead time	t <sub>RWL</sub>	35		40	1	45		ns	
WRITE command to CAS lead time	tCWL	35		40		45		ns	
Data-in set-up time	<sup>t</sup> DS	0		0	1	0	1	ns	14, 18
Data-in hold time	t <sub>DH</sub>	35	<del> </del>	40	<u> </u>	45		ns	14
Data-in hold time referenced to RAS	t <sub>DHR</sub>	85		100		120		ns	'-
CAS to WRITE delay	tCWD	40	<b> </b>	50	-	60	-		40
RAS to WRITE delay	tRWD	40	-	<del> </del>	+	60	<del> </del>	ns	13
	t <sub>T</sub>	90	100	110	100	135	100	ns	13
Transition time (rise or fall)		3	100	3	100	3	100	ns	1-
CAS set-up time (CAS-before-RAS refresh)	<sup>t</sup> CSR	10		10		10		ns	15
CAS hold time (CAS-before-RAS refresh)	<sup>t</sup> CHR	20		25		30		ns	15
Refresh Period (256 cycles distributed)	t <sub>REFD</sub>	1	4		4		4	ms	16
Refresh Period (256 cycles burst)	t <sub>REFB</sub>		4		4		4	ms	17

#### MICRON

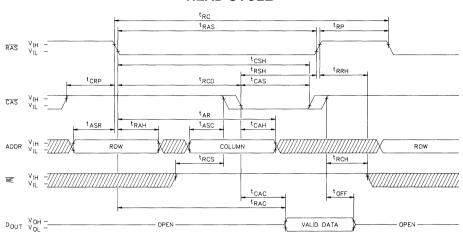
#### MT1259 883C

#### **NOTES**

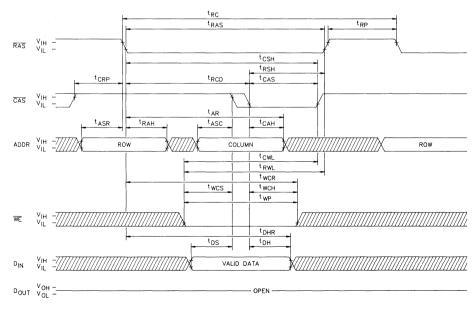
- 1. Vss is common for all voltages.
- 2. Specified values are obtained with the output load equal to 2TTL loads and 100pF to Vss.
- 3. This parameter is sampled, not 100% tested. Capacitance calculated from the equation  $C = \underline{I\Delta t}$ 
  - with  $\Delta V = 3V$  and V = 5V.
- An initial pause of 100µs is required after power-up followed by any 8 RAS cycles, (READ, WRITE, READ-MODIFY-WRITE, RAS refresh) before proper device operation is assured.
- 5. AC characteristics assume transistion time  $({}^{t}T) = 5$ ns.
- 6. VIL (max) and VIH (min) are reference levels for measuring timing of input signals. Transition times are measured between VIL and VIH.
- In addition to meeting the transition rate specification, all input signals must transit between VIL and VIH (or between VIH and VIL) in a monotonic manner.
- If CAS = Vih, data output is high impedance. If CAS = Vil, data output may contain data from the last valid READ cycle.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 10. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 11. If  $\overline{\text{CAS}}$  is low at the falling edge of  $\overline{\text{RAS}}$ , DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for <sup>t</sup>CP. Note 8 applies to determine valid data out.
- 12. <sup>t</sup>OFF (max) defines the time at which the output

- achieves the open circuit condition and is not referenced to Voh or Vol.
- 13. <sup>t</sup>WCS, <sup>t</sup>CWD and <sup>t</sup>RWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) and <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the conditions of the data out (at access time and until CAS goes back to Vih) is indeterminate.
- 14. These parameters are referenced to CAS leading edge in early WRITE cycles and to the WE leading edge in late WRITE or READ-MODIFY-WRITE cycles.
- 15. Enable on-chip refresh and address counters.
- 16. A 256 cycle distibuted refresh consists of an address location refresh cycle being performed within  $15.625\mu S$  so that all  $256 \overline{RAS}$  address combinations are executed within 4ms (regardless of sequence). Micron recommends distributed refresh.
- 17. A 256 cycle burst refresh consists of refreshing, as rapidly as minimum cycle time allows, all 256 combinations of RAS addresses (regardless of sequence). The refresh mode must be executed within 4ms.
- 18. This parameter is "conditionally" guaranteed parameter that is specified to aid with device application. It is not directly verified by a specific test but is used, with several other parameters, in the performance verification of other attributes.

#### **READ CYCLE**

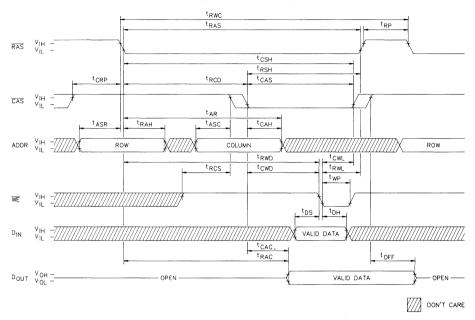


#### **EARLY-WRITE CYCLE**

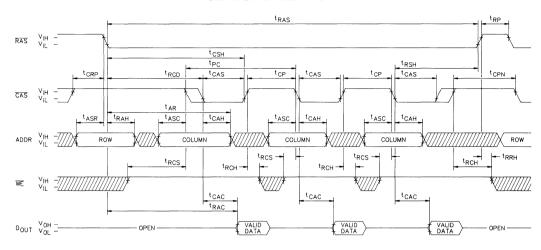


# MILITARY DRAM

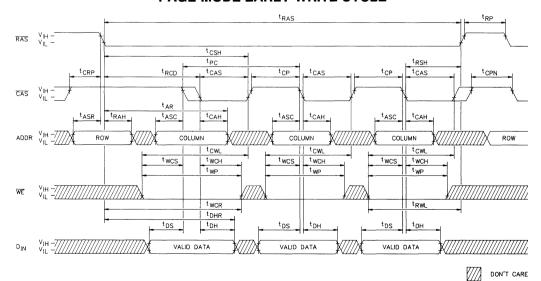
## READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE



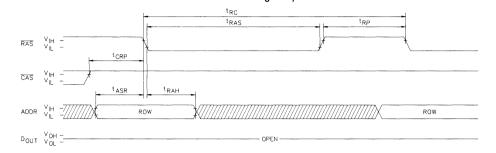
#### PAGE-MODE READ CYCLE



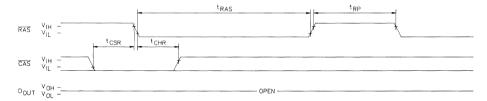
#### **PAGE-MODE EARLY-WRITE CYCLE**



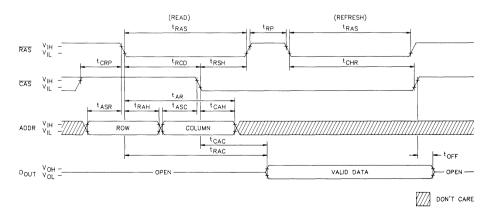
# $\overline{RAS} \text{ ONLY REFRESH CYCLE}$ $(ADDR = A_0 - A_7)$



## CAS-BEFORE-RAS REFRESH CYCLE (ADDRESS INPUTS ARE IGNORED)



#### **HIDDEN REFRESH CYCLE**



#### MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

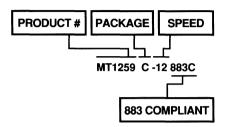
irements and Screens Conditions ral MIL-M-38510	Comment
ral MIL-M-38510	
IL-STD 883, Class B, Rev C  Establish and implement a product assurance program plan and qualification test plan and submit to qualifying activity.	Approved by DESC
ertification Manufacturer's QA survey raceability Traceable to wafer production lot. buntry of Origin N/A Iot required for 883C)	Self audit Computer lot history records Devices manufactured, assembed and tested in Boise, Idaho USA.
STD 883 Fabrication	
coming Inspections All MIL-STD-105D irect Materials	In-line
fer Fabrication Method 2018	100%
sembly Class B Process Monitors	100%
STD 883, Class B, Rev. C, Method 5004 Screening	
ternal Visual Method 2010, cond. B	100%
abilization Bake Method 1008, cond. C	100%
emperature Cycle Method 1010, cond. C	100%
onstant Acceleration Method 2001, cond. E	100%
ermeticity	
. Fine Leak Method 1014, cond. A	100%
Gross Leak Method 1014, cond. C	100%
itial Electricals Manufacturer's documented data sheet @ +118°C	100%
arking Method 2015	100%
urn-in Method 1015, subgroups A-2 for endpoir 162 hours @ 125°C	at 100%
nal Electrical Post Method 5004, Class B, urn-in Test 3.1.16 @ -55°C, +25°C, +113°C 5% PDA and in-line Group A per method 5005	100%
kternal Visual Method 2009	100%
ack/Ship Includes C of C, with QCI data (attributes only)	100%
uality Conformance Method 5005 in-line Class B spection	Groups A, B, C, D
ity Conformance Inspection per Method 5005 (attributes data only)	
roup A Manufacturer's documented	T 11./ 11.
data sheet	Each lot/sublot
roup B Package functional and	Each package type
construction tests	on each lot
roup C Die related	Generic every 13 weeks
roup D (1000 hr. operating life) Package related test	Each package type

Generic every 26 weeks



#### **ORDER INFORMATION**

256Kx1, 120ns access, -55°C to +110°C, in Ceramic DIP



The Micron MT1259-883C serves the special needs of the Defense/Aerospace market. The Micron Military Product Assurance Program provides state-of-the-art screened to MIL-STD 883C Class B Revision C Methods 5004 and 5005. All IC's furnished under this program are produces on certified lines and are manufactured, assembled, tested quality controlled in Micron's modern Boise, Idaho USA facility.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.



## MILITARY DRAM

### 256K x 4 DRAM

**FAST PAGE MODE** 

#### ADDITIONAL MILITARY SPECIFICATIONS

SMD 87676

#### **FEATURES**

- Industry standard pin-out and timing
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby, 150mW active, typical
- Optional Page Mode access cycle
- Refresh modes: RAS only, CAS before RAS, and Hidden
- 512 cycle refresh distributed across 8ms
- Specifications guaranteed over full military DRAM temperature range (-55°C to +110°C)
- MIL-STD 883C processing

#### **OPTIONS**

#### MARKING

Process Level
 MIL-STD 883C (-55°C to +110°C)
 883C
 Parts processed to full requirements
 of MIL-STD 883C, method 5004
 and 5005

MIL-STD 883C with the exception M070 that final electrical testing is performed at 0°C to 70°C

Timing
 100ns access
 120ns access
 150ns access
 -15
 Packages:
 Ceramic DIP
 Ceramic LCC
 EC

#### **GENERAL DESCRIPTION**

The MT4C4265 883C is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time.  $\overline{RAS}$  is used to latch the first 9 bits and  $\overline{CAS}$  the latter 9 bits. A READ or WRITE cycle is selected with the  $\overline{WE}$  input. A logic high on  $\overline{WE}$  dictates READ mode while a logic low on  $\overline{WE}$  dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of  $\overline{WE}$  or  $\overline{CAS}$ , whichever occurs last. If  $\overline{WE}$  goes low prior to  $\overline{CAS}$  going low, the output pin(s) remain

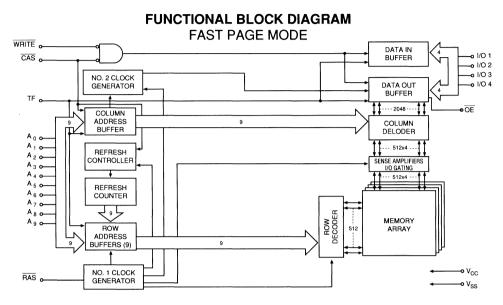
PIN ASSIGNMENT (Top View) MT4C4256 MT4C4256 20 Pin DIP 20 Pin LCC 20 ⊵ Vss DQ1 □•1 DQ1 20 Vss DQ2 19 DQ4 19 DQ4 DQ2 □ 2 118 DQ3 WF 3 WE □ 3 18 DQ3 RAS 4 117 CAS RAS ☐ 4 17 🗆 CAS \*TF 16 \*TF ☐ 5 16 🗅 OE A0 □ 6 15 🗅 A8 ΑO 15 A8 6 **A**1 □ 7 14 🗅 A7 Α1 7 14 A7 13 🗅 A6 A2 □ 8 A2 8 ::::13 A6 12 A5 A3 9 12 A5 **A3** □ 9 Vcc 10 111 A4 11 🗅 A4 Vcc ☐ 10 CD TBD

 ${}^{\star}\mathsf{TF} = \mathsf{Test}$  Function, ground or leave as a no-connect for normal device operation.

open (High Z) until the next  $\overline{CAS}$  cycle. If  $\overline{WE}$  goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as  $\overline{CAS}$  remains low (regardless of  $\overline{WE}$  or  $\overline{RAS}$ ). This late  $\overline{WE}$  pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin direction is controlled by  $\overline{WE}$  and  $\overline{OE}$ .

Returning RAS and CAS high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS only, CAS-before-RAS, or Hidden refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by RAS followed by a column address strobed in by CAS. By holding RAS low, CAS may be toggled strobing in different column addresses executing faster memory cycles. Returning RAS high terminates the PAGE MODE operation.



#### **FUNCTIONAL TRUTH TABLE**

						Addre	esses		
Function	RAS	CAS	WE	OE	TF	tR	tC		NOTES
Standby	Н	Н	Н	Н	GND/NC	Х	Х	High Impedance	
READ	L	L	Н	L	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	Н	GND/NC	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	Н	L	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	Н	GND/NC	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	Н	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	Н	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	Н	GND/NC	Х	Х	High Impedance	
TEST FUNCTION	L	L	Н	Н	Н	ROW	COL	Data Out, Test Funtion Mode	

# **MILITARY DRAM**

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any pin relative to Vss	1.5V to +7.0V
Storage temperature range	65°C to +150°C
Power Dissipation	1 Watt
Lead temperature (soldering 5 sec.)	270°C
Juction temperature (Tj)	+175°C
Short Circuit Output Current	50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### DC ELECTRICAL PERFORMANCE CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (-55°C  $\leq$   $T_{\mbox{\scriptsize C}} \leq$  +110°C, = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: Trc = Trc(MIN))	lcc1		50	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL, CAS = Cycling: TPC = TPC(MIN))	lcc2		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS  Power supply standby current (RAS = CAS = VIH  after 8 RAS cycles min.)	lcc3		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	ICC4		1	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY $(\overline{RAS} = \text{Cycling: } \overline{CAS} = \text{V}_{\text{IH}})$	lcc5		35	mA	3
REFRESH CURRENT: $\overline{CAS}$ -before- $\overline{RAS}$ ( $\overline{RAS}$ and $\overline{CAS}$ = Cycling)	Icc6		35	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ VIN ≤ Vcc), all other pins not under test = 0 volts)	lı	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dour is disabled, 0V ≤ Vour ≤ Vcc)	loz	-10	10	μА	
OUTPUT LEVELS Output High voltage (Ιουτ = -5mA)	Vон	2.4		V	1
Output Low voltage (lout = 5mA)	Vol		0.4	V	

#### RECOMMENDED DC OPERATING CONDITIONS

 $(-55^{\circ}\text{C} \le \text{T}_{\text{C}} \le +110^{\circ}\text{C})$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1

#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9), DIN	Cl1		5	pF	2
Input Capacitance RAS, CAS, WE, OE	CI2		7	pF	2
Output Capacitance Dout	Co		7	pF	2

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C $\leq$ T $_{C}$ $\leq$ +110°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS		-	10	-	12	_	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	190		220		260		ns	
READ-MODIFY-WRITE cycle time	tRWC	220		255		295		ns	
PAGE-MODE READ or WRITE	<sup>t</sup> PC	55		70		85		ns	
cycle time									
Access time from RAS	tRAC		100		120		150	ns	14
Access time from CAS	tCAC		25		30		45	ns	15
Output Enable	t <sub>OE</sub>		25		25		30	ns	
Access time from column address	<sup>t</sup> AA		50		60		70	ns	
Access time from CAS precharge	t <sub>CPA</sub>		50		65		75	ns	
RAS pulse width	t <sub>RAS</sub>	100	10,000	120	10,000	150	10,000	ns	
RAS pulse width (PAGE MODE)	t <sub>RASP</sub>	100	100,000	120	100,000	150	100,000	ns	
RAS hold time	<sup>t</sup> RSH	25		30		45		ns	
RAS precharge time	t <sub>RP</sub>	80		90		100		ns	
CAS pulse width	t <sub>CAS</sub>	25	10,000	30	10,000	45	10,000	ns	
CAS hold time	t <sub>CSH</sub>	100		120		150		ns	
CAS precharge time	<sup>t</sup> CPN	15		20		25		ns	16
CAS precharge time (PAGE MODE)	<sup>t</sup> CP	10		15		20		ns	
RAS to CAS delay time	t <sub>RCD</sub>	10	75	15	90	15	105	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		ns	
Row address hold time	t <sub>RAH</sub>	10		15		15		ns	
RAS to column	t <sub>RAD</sub>	10	50	15	60	15	70	ns	18
address delay time									
Column address set-up time	t <sub>ASC</sub>	0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		20		25		ns	
Column address hold time (referenced to RAS)	<sup>t</sup> AR	60		70		80		ns	
Column address to RAS lead time	<sup>t</sup> RAL	50		60		70		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	19
CAS to output in low-Z	t <sub>CLZ</sub>	5		5		5		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	25	0	25	0	30	ns	20
Output Disable	t <sub>OD</sub>		25		25		30	ns	



#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C  $\leq$  T  $\leq$  +110°C, Vcc = 5.0V  $\pm$  10%)

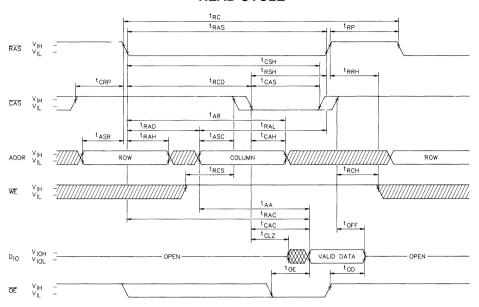
A.C. CHARACTERISTICS		-1	10		12	_	15		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command set-up time	twcs	0		0		0		ns	21
Write command hold time	tWCH	20		25		30		ns	
Write command hold time (referenced to RAS)	tWCR	70		80		90		ns	
Write command pulse width	<sup>t</sup> WP	20		25		30		ns	
Write command to RAS lead time	t <sub>RWL</sub>	25		30		35		ns	
Write command to CAS lead time	tCWL	25		30		35		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		ns	22
Data-in hold time	t <sub>DH</sub>	15		20		25		ns	22
Data-in hold time (referenced to RAS)	t <sub>DHR</sub>	70		80		90		ns	
RAS to WE delay time	t <sub>RWD</sub>	120		150		185		ns	21
Column address to WE delay time	t <sub>AWD</sub>	80		100		120		ns	21
CAS to WE delay time	tCWD	65		75		85		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		8		8		8	ms	
RAS to CAS Precharge time	t <sub>RPC</sub>	0		0		0		ns	
CAS set-up time (CAS-before-RAS refresh)	t <sub>CSR</sub>	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	tCHR	20		25		30		ns	5

#### **NOTES**

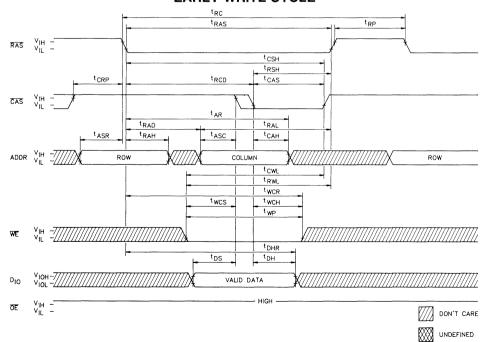
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and  $V_{CC} = 5V$ .
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>C</sub> ≤ 110°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- AC characteristics assume <sup>t</sup>T = 5ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 12. If  $\overline{\text{CAS}} = \text{Vil.}$ , data output may contain data from the last valid READ cycle.
- Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If <del>CAS</del> is low at the falling edge of <del>RAS</del>, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer <del>CAS</del> must be pulsed high for <sup>t</sup>CPN.

- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Operation within the <sup>t</sup>RAD (max) limit ensures that <sup>t</sup>RCD (max) can be met. <sup>t</sup>RAD (max) is specified as a reference point only; if <sup>t</sup>RAD is greater than the specified <sup>t</sup>RAD (max) limit, then access time is controlled exclusively by <sup>t</sup>AA.
- 19. Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle
- 20. tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 21. <sup>t</sup>WCS, <sup>t</sup>RWD, <sup>t</sup>AWD and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), <sup>t</sup>AWD ≥ <sup>t</sup>AWD (min) and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to VIH) is indeterminate.
- 22. These parameters are referenced to CAS leading edge in early WRITE cycles and WE leading edge in late WRITE or READ-WRITE cycles.
- 23. During a READ cycle, if  $\overline{OE}$  is LOW then taken HIGH DOUT goes open. If  $\overline{OE}$  is tied permanently low a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case WE = LOW and OE=HIGH.

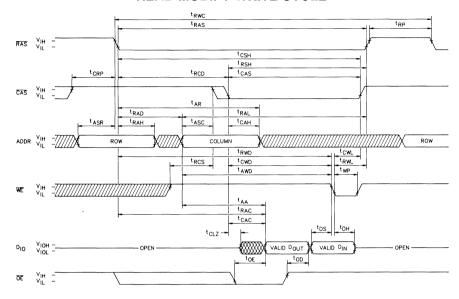
#### **READ CYCLE**



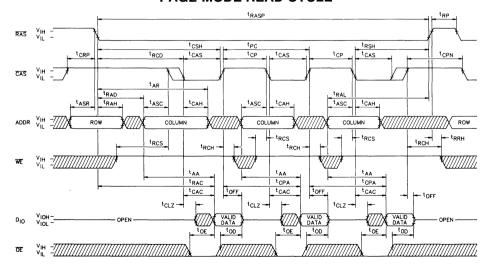
#### **EARLY-WRITE CYCLE**



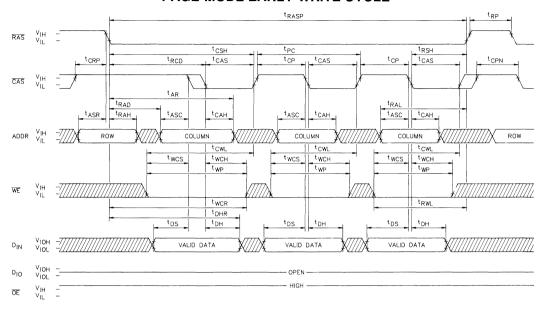
## READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE



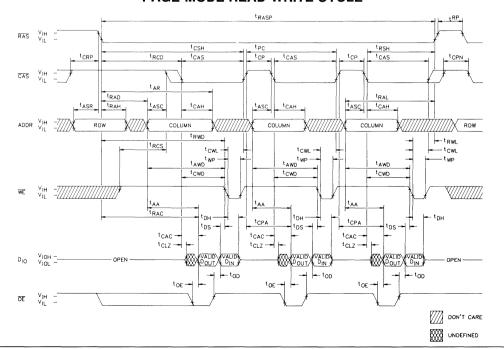
#### PAGE-MODE READ CYCLE



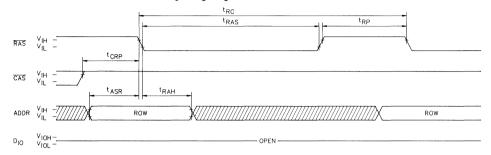
#### PAGE-MODE EARLY-WRITE CYCLE



#### **PAGE-MODE READ-WRITE CYCLE**

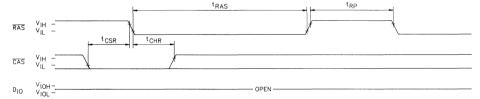


# $\overline{\text{RAS}}$ ONLY REFRESH CYCLE (ADDR = A<sub>0</sub> - A<sub>8</sub>; A<sub>9</sub> and $\overline{\text{WE}}$ = DON'T CARE.)



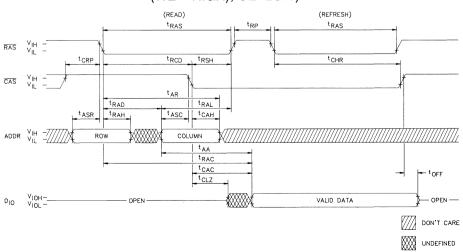
#### **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_q, \overline{WE} \text{ and } \overline{OE} = DON'T CARE)$ 



#### **HIDDEN REFRESH CYCLE**

 $(\overline{WE} = HIGH); \overline{OE} = LOW)^{24}$ 



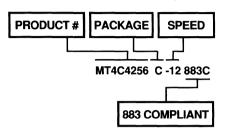


#### MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

MICROI	N MIL-STD 883C PRODUCT ASSURANC	E FLOW
Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan and submit to qualifying activity.	Approved by DESC
<ol> <li>Certification</li> <li>Traceability</li> <li>Country of Origin (Not required for 883C)</li> </ol>	Manufacturer's QA survey Traceable to wafer production lot. N/A	Self audit Computer lot history records Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD 883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD 883, Class B, Rev. C, Metl	hod 5004 Screening	
8. Internal Visual	Method 2010, cond. B	100%
9. Stabilization Bake	Method 1008, cond. C	100%
10. Temperature Cycle	Method 1010, cond. C	100%
11. Constant Acceleration	Method 2001, cond. E	100%
12. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
13. Initial Electricals	Manufacturer's documented data sheet @ +118°C	100%
14. Marking	Method 2015	100%
15. Burn-in	Method 1015, subgroups A-2 for endpoint 162 hours @ 125°C	100%
16. Final Electrical Post	Method 5004, Class B,	100%
Burn-in Test	3.1.16 @ -55°C, +25°C, +113°C	
	5% PDA and in-line Group A	
	per method 5005	
17. External Visual	Method 2009	100%
18. Pack/Ship	Includes C of C, with QCI	100%
19. Quality Conformance	data (attributes only) Method 5005 in-line Class B	Groups A, B, C, D
Inspection		
Quality Conformance Inspection pe	er Method 5005 (attributes data only)	
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and construction tests	Each package type on each lot
21. Group C	Die related (1000 hr. operating life)	Generic every 13 weeks
22. Group D	Package related test	Each package type Generic every 26 weeks

#### ORDER INFORMATION

256K x 4, 120ns access, -55°C to +110°C, in Ceramic DIP



The Micron MT4C4256-883C serves the special needs of the Defense / Aerospace market. The Micron Military Product Assurance Program provides state-of-the-art screened to MIL-STD 883C Class B Revision C Methods 5004 and 5005. All IC's furnished under this program are produces on certified lines and are manufactured, assembled, tested quality controlled in Micron's modern Boise, Idaho USA facility.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

## MILITARY DRAM

### 1MEG x 1 DRAM

**FAST PAGE MODE** 

#### ADDITIONAL MILITARY SPECIFICATIONS

- SMD (consult factory for reference number)
- JAN M3510/249

#### **FEATURES**

- · Industry standard pin-out and timing
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby, 150mW active, typical
- Optional Page Mode access cycle
- Refresh modes: RAS only, CAS before RAS, and Hidden
- · 512 cycle refresh distributed across 4ms
- Specifications guaranteed over full military DRAM temperature range (-55°C to +110°C)
- MIL-STD 883C processing

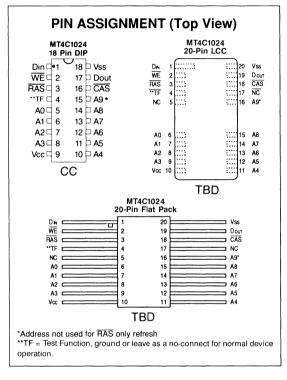
#### **OPTIONS** MARKING Timing -10 100ns access 120ns access -12 150ns access -15 · Process Level MIL-STD 883C (-55°C to +110°C) 883C · Packages: Ceramic DIP C Ceramic LCC EC

#### GENERAL DESCRIPTION

Flat Pack

The MT4C1024 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time.  $\overline{RAS}$  is used to latch the first 10 bits and  $\overline{CAS}$  the latter 10 bits. A READ or WRITE cycle is selected with the  $\overline{WE}$  input. A logic high on  $\overline{WE}$  dictates READ mode while a logic low on  $\overline{WE}$  dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of  $\overline{WE}$  or  $\overline{CAS}$ , whichever occurs last. If  $\overline{WE}$  goes low prior to  $\overline{CAS}$  going low, the output pin(s) remain open (High Z) until the next  $\overline{CAS}$  cycle. If  $\overline{WE}$  goes low after data reaches the output pin(s), Dout is activated and retains the selected cell data as long as  $\overline{CAS}$  remains low (regardless of  $\overline{WE}$  or  $\overline{RAS}$ ). This late  $\overline{WE}$  pulse results in a

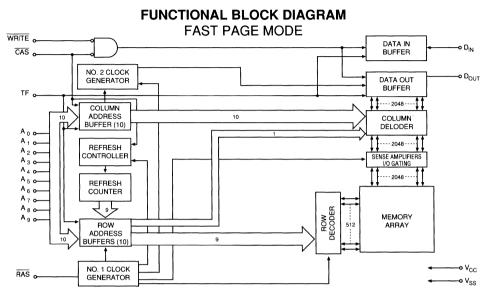
F



#### READ-WRITE cycle.

Returning  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{\text{RAS}}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{\text{RAS}}$  cycle (READ, WRITE,  $\overline{\text{RAS}}$  only,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ , or Hidden refresh) so that all 512 combinations of  $\overline{\text{RAS}}$  addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by RAS followed by a column address strobed in by CAS. By holding RAS low, CAS may be toggled strobing in different column addresses executing faster memory cycles. Returning RAS high terminates the PAGE MODE operation.



#### **FUNCTIONAL TRUTH TABLE**

					Addre	esses		
Function	RAS	CAS	WE	TF	tR	tC		NOTES
Standby	Н	Н	Н	GND/NC	Х	Х	High Impedance	
READ	L	L	Н	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	Н	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	GND/NC	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	Н	Н	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Н	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Н	GND/NC	Х	Х	High Impedance	
TEST FUNCTION	L	L	Н	Н	ROW	COL	Data Out, Test Funtion Mode	



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any pin relative to Vss	1.5V to +7.0V
Storage temperature range	65°C to +150°C
Power Dissipation	1 Wat
Lead temperature (soldering 5 sec	.)270°C
Juction temperature (Tj)	+175°C
Short Circuit Output Current	50m <i>A</i>

the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

\*Stresses greater than those listed under "Absolute Maxi-

#### DC ELECTRICAL PERFORMANCE CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (-55°C  $\leq$  T  $_{C} \leq$  +110°C = 5.0V  $\pm$  10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN))	lcc1		50	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL, CAS = Cycling: tpc = tpc(MIN))	lcc2		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = VIH after 8 RAS cycles min.)	lcc3		4	mA	
STANDBY CURRENT: CMOS INPUT LEVELS  Power supply standby current (RAS = CAS = Vcc -0.2V  after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	Icc4		1	mA	
REFRESH CURRENT: RAS ONLY (RAS = Cycling: CAS = Vih)	lcc5		35	mA	3
REFRESH CURRENT: $\overline{CAS}$ -before- $\overline{RAS}$ ( $\overline{RAS}$ and $\overline{CAS}$ = Cycling)	lcc <sub>6</sub>		35	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V $\leq$ Vin $\leq$ Vcc), all other pins not under test = 0 volts. Vcc = 5.5 volts)	lı .	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ Vout, 6.5V, Vcc = 5.5 volts)	loz	-10	10	μА	
OUTPUT LEVELS Output High voltage (lout = -5mA)	<b>V</b> oн	2.4		V	1
Output Low voltage (IOUT = 5mA)	<b>V</b> OL		0.4	V	

#### RECOMMENDED DC OPERATING CONDITIONS

 $(-55^{\circ}C \le T_{C} \le +110^{\circ}C)$ 

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	<b>V</b> cc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1
Refresh cycle time	TREF		4.0	ms	

#### **CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (Ao-A9)	C <sub>l1</sub>		6	pF	2
Input Capacitance RAS, CAS, WE, DIN	CI2		7	pF	2
Output Capacitance Dout	Co		7	pF	2

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C $\leq$ T $_{C}$ $\leq$ +110°C, Vcc = 5.0V $\pm$ 10%)

A.C. CHARACTERISTICS PARAMETER		-10		-12		-15			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	<sup>t</sup> RC	190		220		260		ns	
READ-MODIFY-WRITE cycle time	<sup>t</sup> RWC	220		255		295		ns	
PAGE-MODE READ or WRITE cycle time	<sup>t</sup> PC	75		90		110		ns	22
Access time from RAS	tRAC		100		120		150	ns	14
Access time from CAS	tCAC		50		60		75	ns	15
RAS pulse width	t <sub>RAS</sub>	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	t <sub>RSH</sub>	50		60		75		ns	
RAS precharge time	t <sub>RP</sub>	80		90		100		ns	
CAS pulse width	<sup>t</sup> CAS	50	10,000	60	10,000	75	10,000	ns	
CAS hold time	tCSH	100		120		150		ns	
CAS precharge time	t <sub>CPN</sub>	20		25		25		ns	16
CAS precharge time (PAGE MODE)	<sup>t</sup> CP	20		25		25		ns	
RAS to CAS delay time	t <sub>RCD</sub>	25	50	25	60	25	75	ns	17
CAS to RAS precharge time	t <sub>CRP</sub>	10		10		10		ns	
Row address set-up time	<sup>t</sup> ASR	5		5		5		ns	
Row address hold time address delay time	<sup>t</sup> RAH	15		20		20		ns	
Column address set-up time	tASC	5		5		5		ns	
Column address hold time	t <sub>CAH</sub>	20		20		25		ns	
Column address hold time (referenced to RAS)	<sup>t</sup> AR	60		70		80		ns	
Read command set-up time	t <sub>RCS</sub>	0		0		0		ns	
Read command hold time (referenced to CAS)	<sup>t</sup> RCH	0		0		0		ns	18
Read command hold time (referenced to RAS)	<sup>t</sup> RRH	0		0		0		ns	18
Output buffer turn-off delay	<sup>t</sup> OFF	0	40	0	40	0	40	ns	19
WE command set-up time	twcs	0		0		0		ns	20
Write command hold time	tWCH	20		25		30		ns	

## MICHON

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

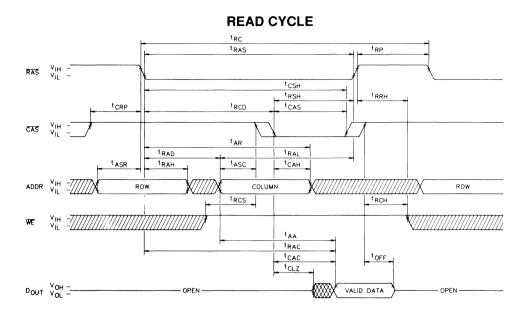
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C  $\leq$  TC  $\leq$  +110°C, Vcc = 5.0V  $\pm$  10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time (referenced to RAS)	tWCR	70		80		90		ns	
Write command pulse width	t <sub>WP</sub>	20		25		30		ns	
Write command to RAS lead time	t <sub>RWL</sub>	20		30		35		ns	
Write command to CAS lead time	tCWL	25		30		35		ns	
Data-in set-up time	t <sub>DS</sub>	5		5		5		ns	21
Data-in hold time	t <sub>DH</sub>	15		20		25		ns	21
Data-in hold time (referenced to RAS)	t <sub>DHR</sub>	70		80		90		ns	
RAS to WE delay time	t <sub>RWD</sub>	90		110		135		ns	20
CAS to WE delay time	tCWD	30		40		45		ns	20
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t <sub>REF</sub>		4		4		4	ms	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		ns	5
CAS hold time (CAS-before-RAS refresh)	tCHR	20		25		30		ns	5

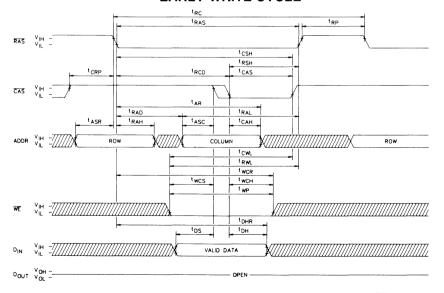
#### **NOTES**

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is calculated from the equation  $C = \underline{I\Delta t}$  with  $\Delta V = 3V$  and  $V_{CC} = 5V$ .
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading. Specified values are obtained the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-55°C ≤ T<sub>C</sub> ≤ +110°C) is assured.
- An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
- 8. AC characteristics assume <sup>t</sup>T = 5ns.
- 9. VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- In addition to meeting the transition rate specification, all input signals must transit between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>) in a monotonic manner.
- 11. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
- 12. If  $\overline{\text{CAS}} = \text{Vil}$ , data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 15. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 16. If  $\overline{CAS}$  is low at the falling edge of  $\overline{RAS}$ , DOUT will

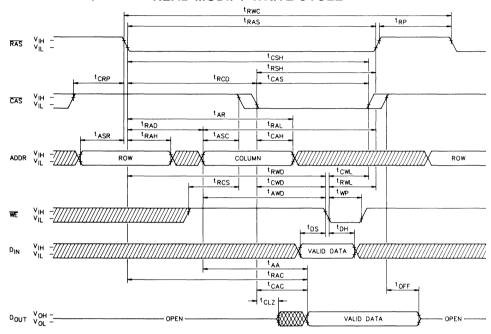
- be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for  ${}^{\text{t}}\text{CPN}$ .
- 17. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is controlled exclusively by <sup>t</sup>CAC.
- 18. Either <sup>t</sup>RCH or <sup>t</sup>RRH must be satisfied for a READ cycle
- 19. tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH ot VOL.
- 20. <sup>t</sup>WCS, <sup>t</sup>RWD, and <sup>t</sup>CWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min), and <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back to VIH) is indeterminate.
- 21. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles and  $\overline{\text{WE}}$  leading edge in late WRITE or READ-WRITE cycles.
- 22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{WE}$  = LOW.



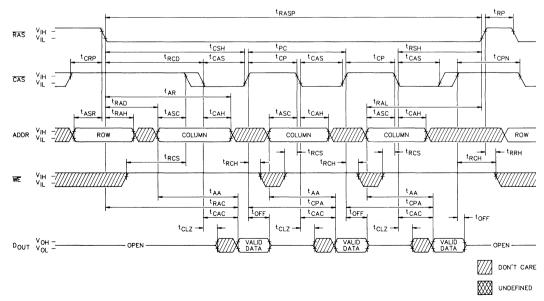




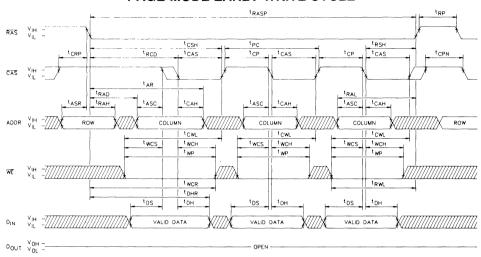
## READ-WRITE CYCLE READ-MODIFY-WRITE CYCLE



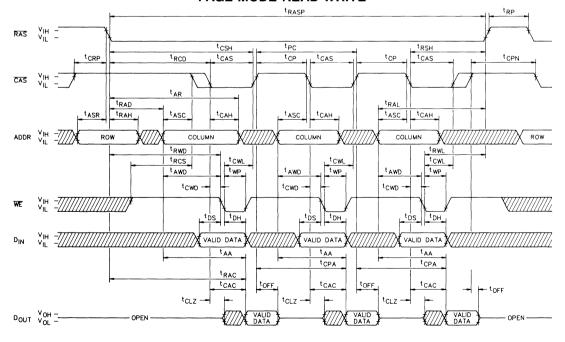
#### **PAGE-MODE READ CYCLE**



#### PAGE-MODE EARLY-WRITE CYCLE

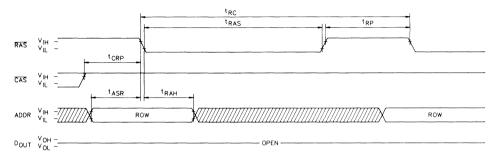


#### PAGE-MODE READ-WRITE



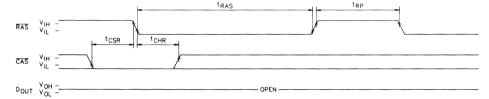
### **RAS ONLY REFRESH CYCLE**

 $(ADDR = A_0 - A_8; A_9 \text{ and } \overline{WE} = DON'T CARE.)$ 



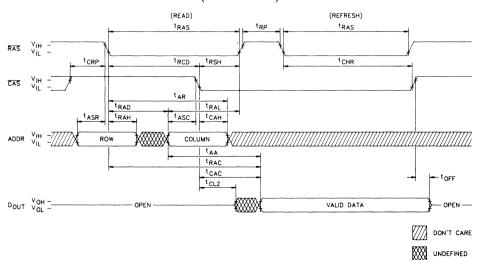
### **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_9 \text{ and } \overline{WE} = DON'T \text{ CARE})$ 



### **HIDDEN REFRESH CYCLE**

 $(\overline{WE} = HIGH)$ 



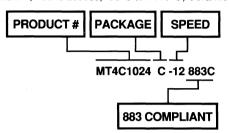


### MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

MICRO	N MIL-STD 883C PRODUCT ASSURANC	E FLOW
Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan and submit to qualifying activity.	Approved by DESC
<ol> <li>Certification</li> <li>Traceability</li> <li>Country of Origin (Not required for 883C)</li> </ol>	Manufacturer's QA survey Traceable to wafer production lot. N/A	Self audit Computer lot history records Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD 883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
<ul><li>6. Wafer Fabrication</li><li>7. Assembly</li></ul>	Method 2018 Class B Process Monitors	100% 100%
MIL-STD 883, Class B, Rev. C, Met	hod 5004 Screening	
<ol> <li>8. Internal Visual</li> <li>9. Stabilization Bake</li> <li>10. Temperature Cycle</li> <li>11. Constant Acceleration</li> <li>12. Hermeticity         <ul> <li>A. Fine Leak</li> <li>B. Gross Leak</li> </ul> </li> <li>13. Initial Electricals</li> <li>14. Marking</li> <li>15. Burn-in</li> <li>16. Final Electrical Post         <ul> <li>Burn-in Test</li> </ul> </li> <li>17. External Visual</li> <li>18. Pack/Ship</li> <li>19. Quality Conformance</li> </ol>	Method 2010, cond. B Method 1008, cond. C Method 1010, cond. C Method 2001, cond. E  Method 1014, cond. A Method 1014, cond. C Manufacturer's documented data sheet @ +118°C Method 2015 Method 2015 Method 1015, subgroups A-2 for endpoint 162 hours @ 125°C Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +113°C 5% PDA and in-line Group A per method 5005 Method 2009 Includes C of C, with QCI data (attributes only) Method 5005 in-line Class B	100% 100% 100% 100% 100% 100% 100% 100% 100% 100% Groups A, B, C, D
Inspection		
	er Method 5005 (attributes data only)	
19. Group A 20. Group B	Manufacturer's documented data sheet Package functional and	Each lot/sublot Each package type
21. Group C	construction tests Die related	on each lot Generic every 13 weeks
22. Group D	(1000 hr. operating life) Package related test	Each package type Generic every 26 weeks

### **ORDER INFORMATION**

1 MEG x 1, 100ns access, -55°C to +110°C, Ceramic DIP



The Micron MT4C1024-883C serves the special needs of the Defense/Aerospace market. The Micron Military Product Assurance Program provides state-of-the-art screened to MIL-STD 883C Class B Revision C Methods 5004 and 5005. All IC's furnished under this program are produces on certified lines and are manufactured, assembled, tested quality controlled in Micron's modern Boise, Idaho USA facility.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

# MILITARY VRAM

# 64K x 4 DRAM with 256 x 4 SAM

### ADDITIONAL MILITARY SPECIFICATIONS

• SMD (consult factory for reference number)

#### **FEATURES**

- Industry standard pin-out, timing, and functions
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS, and HIDDEN
- 256 cycle refresh within 4ms
- Optional PAGE MODE access cycles
- Dual port organization: 64K x 4 DRAM port 256 x 4 SAM port
- Bit MASK-WRITE mode capability on DRAM port
- No refresh required for Serial Access Memory
- Low power: 10mW standby, 150mW active, typical
- Fast access times 120ns parallel, 40ns serial
- Specifications guaranteed over Full Military DRAM temperature range (-55°C to +110°C)
- MIL-STD-883 Rev. C, Class B

### **OPTIONS**

### MARKING

883C

 Process Level MIL-STD-883C (-55°C to +110°C)
 Parts processed to full requirements of MIL-STD-883C, method 5004 and 5005

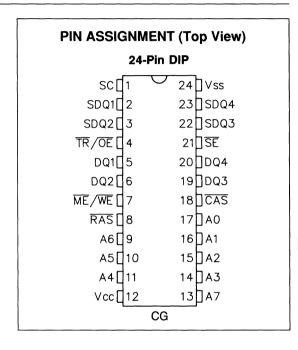
MIL-STD-883C with the exception that M070 final electrical testing is performed at 0°C to +70°C

• Timing (DRAM, SAM)
120ns, 40ns -12
150ns, 60ns -15
200ns, 60ns -20

Packages
 Ceramic DIP (400 mil)
 C

### GENERAL DESCRIPTION

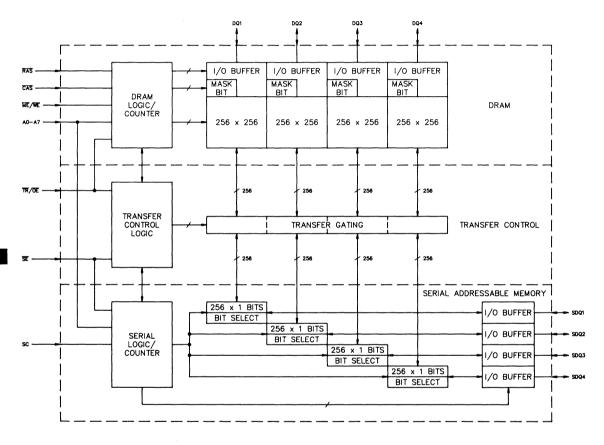
The MT42C4064 883C is a high speed, dual port CMOS dynamic random access memory (DPDRAM) containing 262,144 bits. It can be accessed either by a four bit wide DRAM port or by a 256 x 4 bit serial access memory (SAM) port. Data can be transferred bidirectionally between the



#### DRAM and the SAM.

The DRAM portion of the DPDRAM is functionally identical to the MT4067 64K x 4 bit DRAM. Four 256 bit data registers make up the serial access memory portion of the DPDRAM. Data I/O and internal data transfer is accomplished using three separate bidirectional data paths; the four bit random access I/O port, the four internal 256 bit wide paths between the DRAM and the SAM, and the four bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic. Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs the DPDRAM must be refreshed in order to maintain data. The refresh cycles must be timed so that all 256 combinations of RAS addresses are executed at least every 4ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the DPDRAM is fully static and does not require any refresh.

# Figure 1 MT42C4064 BLOCK DIAGRAM



### **PIN DESCRIPTIONS**

PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
1	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
2, 3, 22, 23	SDQ1 - SDQ4	Input/ Output	Serial Data I/O: Input, Output, or high impedance.
4	TR/OE	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{\text{RAS}}$ (H $\rightarrow$ L), or
			Output Enable: Enables the DRAM output buffers when taken LOW after RAS goes LOW (CAS must also be LOW), otherwise the output buffers are in a high impedance state.
5, 6, 19, 20	DQ1 - DQ4	Input/ Output	DRAM Data I/O: Inputs, Outputs, or high impedance, and/or Mask Data Inputs: For MASK-WRITE cycle only.
7	ME/WE	Input	Mask Enable: If $\overline{\text{ME}/\text{WE}}$ is LOW at the falling edge of $\overline{\text{RAS}}$ a MASK-WRITE cycle is performed, or
			Write Enable: $\overline{WE}$ is used to select a READ ( $\overline{WE}$ = H) or WRITE ( $\overline{WE}$ = L) cycle when accessing the DRAM. This includes a DRAM-TO-SAM TRANSFER ( $\overline{WE}$ = H) or SAM-TO-DRAM TRANSFER ( $\overline{WE}$ = L).
8	RAS	Input	Row Address Strobe: RAS is used to clock in the 8 Row Address bits and as a strobe for the MASK ENABLE and TRANSFER functions.
9, 10, 11, 13, 14, 15, 16, 17	A0 to A7	Input	Address Inputs: For the DRAM operation these inputs are multiplexed and clocked by RAS and CAS to select 4 bits out of the 256K available. During TRANSFER operations, A0 to A7 indicate the DRAM row being accessed (when RAS goes low) and the SAM start address (when CAS goes slow).
12	Vcc	Supply	Power Supply: +5 Volts ±10%
18	CAS	Input	Column Address Strobe: RAS is used to clock in the 8 column address bits and enable the DRAM output buffers (TR/OE must also be LOW).
21	SE	Input	Serial Port Enable: SE enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a high impedance state. SE is also used during a TRANSFER operation to indicate whether a SAM-TO-DRAM TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
24	Vss	Supply	Ground

### **FUNCTIONAL DESCRIPTION**

The DPDRAM can be divided into three functional blocks (see Figure 1); the DRAM, the Transfer Control circuitry, and the Serial Access Memory (SAM). All of the operations described below are also shown in the AC Timing Diagrams section of this data sheet as well as summarized in the Functional Truth Table.

Note:

For dual function pins, the function that is not being discussed will be surrounded by paranthesis. For example, when discussing transfer operations the  $\overline{TR}/\overline{OE}$  pin will be shown as  $\overline{TR}/(\overline{OE})$ .

### DRAM OPERATION

The DRAM portion of the DPDRAM is functionally identical to standard 64K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or "don't care" states for the DRAM are specified for the DPDRAM. These conditions are highlighted in the following discussion.

### **READ/WRITE Cycles**

The 16 address bits that are used to select four memory bits from the  $65,536 \times 4$  available are latched into the chip using the A0 -A7,  $\overline{RAS}$ , and  $\overline{CAS}$  inputs. First, the 8 row address bits are set up on the address inputs and clocked into the part when  $\overline{RAS}$  transitions from HIGH to LOW. Next, the 8 column address bits are set up on the address inputs and clocked in when  $\overline{CAS}$  goes from HIGH to LOW.

For single port DRAMs the  $\overline{OE}$  pin is a "don't care" when  $\overline{RAS}$  goes LOW. For the DPDRAM,  $(\overline{TR})/\overline{OE}$  is used, when  $\overline{RAS}$  goes LOW, to select between an internal transfer operation and a DRAM operation.  $(\overline{TR})/\overline{OE}$  must be HIGH at the  $\overline{RAS}$  HIGH to LOW transition for a DRAM port READ or WRITE operation.

If (ME)/WE is HIGH when CAS goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1 - DQ4 port. The (TR)/OE input must be LOW to enable the DRAM output port.

For single port DRAMS,  $\overline{WE}$  is a "don't care" when  $\overline{RAS}$  goes LOW. For the DPDRAM,  $(\overline{ME})/\overline{WE}$  is used, when  $\overline{RAS}$  goes LOW, to select between a MASK WRITE cycle and a normal WRITE cycle. If  $(\overline{ME})/\overline{WE}$  is LOW at the  $\overline{RAS}$  HIGH to LOW transition a MASK WRITE operation is selected. For a normal DRAM WRITE operation,  $(\overline{ME})/\overline{WE}$  must be HIGH at the  $\overline{RAS}$  HIGH to LOW transition.  $(\overline{ME})/\overline{WE}$  is a "don't care" at the  $\overline{RAS}$  HIGH to LOW transition for a DRAM READ cycle.

If (ME)/WE is LOW when CAS goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1 - DQ4 port will be written into the selected memory cells. If ME/(WE) is LOW when RAS goes LOW the input data will be "masked" before being stored in the DRAM.

The DPDRAM can perform all the normal DRAM cycles including EARLY-WRITE, LATE-WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE-MODE READ, PAGE-MODE WRITE, and PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in this data sheet for more details on these operations.

#### MASK-WRITE

If  $\overline{\text{ME}}/(\overline{\text{WE}})$  is LOW at the  $\overline{\text{RAS}}$  HIGH to LOW transition, the data (mask data) present on the DQ1 - DQ4 inputs will be written into the bit mask data register. The mask data acts as an individual write enable for each of the four DQ1 - DQ4 pins. If a LOW (logic 0) is written to a mask data register bit the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. Note that CAS is still HIGH. When CAS goes LOW, the bits present on the DQ1 - DQ4 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. Since the mask data register is reset (to all 1's) at the end of every MASK-WRITE cycle, new mask data must be supplied at the beginning of each MASK-WRITE cycle. An example of a typical MASK-WRITE cycle is shown in Figure 2.

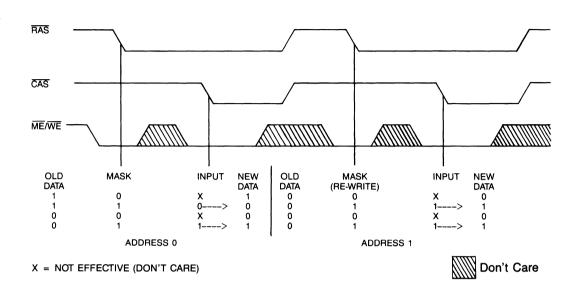


Figure 2
MT42C4064 Bit MASK-WRITE

### REFRESH

The MT42C4064 supports RAS ONLY, CAS-BEFORE-RAS, and HIDDEN types of refresh cycles. All 256 row address combinations must be accessed within 4ms. For the CAS-BEFORE-RAS refresh mode the row addresses are generated internally and the user need not supply them

as he must in  $\overline{RAS}$  ONLY refresh.  $\overline{TR}/(\overline{OE})$  must be HIGH when  $\overline{RAS}$  goes LOW for the  $\overline{RAS}$  ONLY and  $\overline{CAS}$ -BEFORE- $\overline{RAS}$  types of refresh cycles. Any READ, WRITE, or TRANSFER operation also refreshes the DRAM row that is being accessed.

### TRANSFER OPERATION DRAM-TO-SAM TRANSFER (READ TRANSFER)

A TRANSFER operation is initiated when  $\overline{TR}/(\overline{OE})$  is LOW at  $\overline{RAS}$  (HIGH to LOW) time.  $(\overline{ME})/\overline{WE}$  indicates the direction of the transfer and must be HIGH as RAS goes LOW for a DRAM-TO-SAM TRANSFER. In this case, the row address bits indicate the four 256 bit DRAM rows that are to be transferred to the four SAM data registers and the column address bits indicate the start address of the next SERIAL OUTPUT cycle from the SAM data registers. RAS and  $\overline{CAS}$  are used to strobe the address bits into the part. To complete the TRANSFER, TR/(OE) is taken HIGH while  $\overline{RAS}$  and  $\overline{CAS}$  are still LOW. The 1024 bits of DRAM data are then written into the SAM data registers and the serial shift start address is stored in an internal 8 bit register. There must be no rising edges on the Serial Clock (SC) input while the transfer is taking place (refer to the AC timing diagrams). TRANSFER cycles are the only time when SC must be synchronized with the DRAM RAS and CAS timing. If SE is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. SE enables the serial outputs and may be either HIGH or LOW during this operation.

### SAM-TO-DRAM TRANSFER (WRITE TRANSFER)

The SAM-TO-DRAM TRANSFER operation is identical to the DRAM-TO-SAM TRANSFER described above except that  $(\overline{\text{ME}})/\overline{\text{WE}}$  and  $\overline{\text{SE}}$  must be LOW when  $\overline{\text{RAS}}$  goes LOW. The row address indicates the DRAM row that the SAM data registers will be written to and the column address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. If  $\overline{\text{SE}}$  is HIGH when  $\overline{\text{RAS}}$  goes LOW, a SERIAL INPUT MODE ENABLE cycle is performed.

### SAM OPERATION SERIAL INPUT/OUTPUT MODE CONTROL

The SAM port is automatically placed in the serial output mode after a DRAM-TO-SAM TRANSFER operation. Conversely, after a SAM-TO-DRAM TRANSFER the SAM port will be in the serial input mode.

### SERIAL INPUT MODE ENABLE (PSEUDO WRITE TRANSFER)

It is possible to change the direction of the SAM port from output to input without performing a SAM-TO-DRAM TRANSFER. This operation, called a SERIAL INPUT MODE ENABLE cycle, is simply a SAM-TO-DRAM TRANSFER cycle with  $\overline{\text{SE}}$  held HIGH instead of LOW. The DRAM data will not be disturbed and the data registers will be ready to accept input data.

The only way to put the SAM port in the serial output mode is to do a DRAM-TO-SAM TRANSFER.

#### SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and  $\overline{\text{SE}}$ . The rising edge of SC increments the serial address counter and provides access to the next SAM location.  $\overline{\text{SE}}$  enables or disables the serial input/output buffers.

Serial output of the SAM data register contents will start at the serial start address that was loaded during the DRAM-TO-SAM TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the four bit port.  $\overline{SE}$  is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW to HIGH transition, regardless of whether  $\overline{SE}$  is HIGH or LOW, and will wrap around to location 0 after reaching its maximum count of 255.

SC is also used to clock in data when the device is in the serial input mode. As in the serial output operation, the contents of the serial address register, which was loaded when the serial input mode was enabled, will determine the serial address that the first bit will be written.  $\overline{SE}$  acts as an enable for serial data input and must be LOW for normal serial input. If  $\overline{SE}$  is HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address register is incremented with every  $L \rightarrow H$  transition of SC, regardless of the logic level on the  $\overline{SE}$  input.

### **FUNCTIONAL TRUTH TABLE**

DRAM Operations (SC, SE, and SDQ1 — SDQ4 are don't care)

Function	RAS	CAS	ME	WE	TF	7/OE	Addre	sses	DQ1	Natas
Function	HAS	CAS	tR*	tC*	tR*	tC*	tR*	tC*	to DQ4	Notes
Standby	Н	Н	Х	Х	Х	Х	Х	Х	High Impedance	
READ	L	L	Х	Н	Н	H→L	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	Н	L	Н	Х	ROW	COL	Data In	1
MASK-WRITE	H→L	L	L	L	Н	Х	ROW	COL	Mask Data In, Valid Data In	
READ-WRITE	L	L	Н	H→L	Н	L→H	ROW	COL	Valid Data Out,	1
PAGE-MODE READ	L	H→L→H, H→L→H	Н	Н	Н	H→L	ROW	COL	Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	Н	L	Н	Х	ROW	COL	Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H, H→L→H	Н	H→L	Н	L→H	ROW	COL	Valid Data Out, Valid Data In	1
RAS ONLY REFRESH	L	Н	Х	n/a	Н	n/a	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	Х	Н	Н	L	ROW	COL	Valid Data Out	
CAS-BEFORE- RAS REFRESH	H→L	L	Х	Х	Н	Х	Х	Х	High Impedance	

### TRANSFER Operations (DQ1 — DQ4 are don't care)

Function	RAS	CAS	ME	WE	TR	OE	Addr	esses	sc	SE	SDQ1	Notes
runction		CAS	tR*	tC*	tR*	tC*	tR*	tC*			SDQ4	
DRAM-TO-SAM TRANSFER	L	L	Н	Х	L	L	ROW	SSA**	Х	Х	Х	2
SAM-TO-DRAM TRANSFER	L	L	L	Х	L	Х	ROW	SSA**	Х	L	Х	3
SERIAL INPUT MODE ENABLE	L	L	L	Х	L	Х	ROW	SSA**	Х	Н	Х	4

<sup>=</sup> when  $\overline{RAS}$  goes from HIGH to LOW tR

<sup>=</sup> when CAS goes from HIGH to LOW

<sup>\*\*</sup> SSA = SAM Start Address, the serial address that the next serial input or output cycle will start with.

Notes: 1. Any type of WRITE cycle may also be a MASK-WRITE cycle.

<sup>2.</sup> The SAM will be in a SERIAL OUTPUT mode after a DRAM-TO-SAM TRANSFER.

<sup>3.</sup> The SAM will be in a SERIAL INPUT mode after a SAM-TO-DRAM TRANSFER.

<sup>4.</sup> The SAM will be put in the SERIAL INPUT mode but the SAM-TO-DRAM TRANSFER will not occur.

### Serial I/O Operations (RAS, CAS, ME/WE, TR/OE, and DQ1 - DQ4 are don't care)

Function	SC	SE	SDQ1 — SDQ4	Notes
SERIAL OUTPUT	L→H	L	Valid Data Out	5
SERIAL INPUT	L→H	L	Valid Data In	6

**Notes:** 5. The SAM must be in the SERIAL OUTPUT mode. 6. The SAM must be in the SERIAL INPUT mode.

### ABSOLUTE MAXIMUM RATINGS\*

Voltage on any pin relative to Vss	1.5V to +7.0V
Operating Temperature Range	65°C to +150°C
Power Dissipation	1 Watt
Lead Temperature (soldering 5 sec.)	300°C
Juction Temperature Tj)	+150°C
Short Circuit Output Current	50mA
Thermal Resistance (θjc) 24 pin DIP	

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# **RECOMMENDED DC OPERATING CONDITIONS** $(0^{\circ}C \le T_{A} \le 70^{\circ}C)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc Supply Voltage	Vcc	4.5	5.5	٧	1
Vss power supply and signal reference	Vss	0.0	0.0	٧	1
Operating case temperature	Tc	-55	+110	°C	
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1

### DC ELECTRICAL CHARACTERISTICS

(Notes 3, 4, 5) ( $Vcc = 5.0V \pm 10\%$ )

ITEM	TEST	NOTES	SYMBOL	ALT.	CONDITIONS	DEVICE	GROUP A	LIM	ITS	UNIT
				SYMBOL	-55°C ≤ Tc ≤ +110°C	TYPE	SUBGROUPS	MIN	MAX	
1	High level output voltage	1	<b>V</b> он		VCC = 4.5 $V$ , IOH = 5 $m$ A $V$ IL = 0.8 $V$ , $V$ IH = 2.4 $V$	All	1, 2, 3	2.4		٧
2	Low level output voltage	1	Vol		Vcc = 4.5V, lot = -5mA VIL = 0.8V, VIH = 2.4V	All	1, 2, 3		0.4	٧
3	High level input leakage current		lıн		Vcc = 5.5V, Vı = 6.5V	All	1, 2, 3		10	μА
4	Low level input leakage current		lıL		Vcc = 5.5V, VI = 0.0V	All	1, 2, 3		-10	μА
5	Output leakage current		loz		Vcc = 5.5V, outputs are disabled, 0V ≤ Voυτ ≤ Vcc	All	1, 2, 3	-10	10	μА

# MICHON

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### **CAPACITANCE**

ITEM	TEST	NOTES	SYMBOL	ALT.	CONDITIONS	DEVICE	GROUP A	LIM	IITS	UNIT
				SYMBOL	-55°C ≤ Tc ≤ +110°C	TYPE	SUBGROUPS	MIN	MAX	
1	Input capacitance (A0 - A7, DIN)	18	Сп		Sampled parameter	All	4		5	pF
2	Input capacitance (RAS, CAS, WE, OE, SC, SE	18	Cı2		Sampled parameter	All	4		7	pF
3	Input capacitance (A0 - A7, Dout)	18	Co		Sampled parameter	All	4		7	pF

### **NOTES**

- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of  $100\mu s$  is required after power-up followed by any  $8 \overline{RAS}$  cycles before proper device operation is assured. The  $\overline{RAS}$  cycle wake-up should be repeated any time the 4ms static refresh requirement is exceeded.
- 4. AC characteristics assume  ${}^{t}T = 5$ ns.
- VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-55°C ≤ T<sub>C</sub> ≤ +110°C) is assured.
- Measured with a load equivalent to 2 TTL gates and 100pF.
- Assumes that <sup>t</sup>RCD < <sup>t</sup>RCD (max). If <sup>t</sup>RCD is greater than the maximum recommended value shown in this table, <sup>t</sup>RAC will increase by the amount that <sup>t</sup>RCD exceeds the value shown.
- 9. Assumes that  ${}^{t}RCD \ge {}^{t}RCD$  (max).
- 10. If  $\overline{CAS} = V_{IH}$ , DRAM data output is high impedance.
- 11. If  $\overline{\text{CAS}} = \text{VIL}$ , DRAM data output may contain data from the last valid READ cycle.
- 12. <sup>t</sup>OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to Voн or Vol.
- 13. Operation within the <sup>t</sup>RCD (max) limit ensures that <sup>t</sup>RAC (max) can be met. <sup>t</sup>RCD (max) is specified as a reference point only; if <sup>t</sup>RCD is greater than the specified <sup>t</sup>RCD (max) limit, then access time is con trolled exclusively by <sup>t</sup>CAC.
- 14. <sup>t</sup>RCH is referenced to the first rising edge of RAS or CAS.
- 15. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and to WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.

- 16. <sup>t</sup>WCS, <sup>t</sup>CWD and <sup>t</sup>RWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If <sup>t</sup>WCS ≥ <sup>t</sup>WCS (min) the cycle is an EARLY-WRITE cycle and the data output will remain open circuit throughout the entire cycle. If <sup>t</sup>CWD ≥ <sup>t</sup>CWD (min) and <sup>t</sup>RWD ≥ <sup>t</sup>RWD (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until CAS goes back toVih) is indeterminate.
- 17. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 18. Capacitance calculated from the equation  $C = \underline{I\Delta t} \Delta V$  with  $\Delta V = 3V$  and  $V_{CC} = 5V$ . This parameter is

with  $\Delta V = 3V$  and VCC = 5V. This parameter is sampled.

- 19. If  $\overline{\text{CAS}}$  is low at the falling edge of  $\overline{\text{RAS}}$ , DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer  $\overline{\text{CAS}}$  must be pulsed high for  ${}^{\text{t}}\text{CP}$ . Note 8 applies to determine valid data out.
- 20. Includes the  $\overline{\text{OE}}$  delay time (25ns for the -12, 30ns for the -15, and 45ns for the -20).
- 21. During a READ cycle if  $\overline{OE}$  is low then taken high (VIH) DOUT goes open. If  $\overline{OE}$  is tied permanently low a READ-MODIFY-WRITE operation is not possible.
- 22. Enables on-chip refresh and address counters.
- 23. TRANSFER Command means that  $\overline{TR}/(\overline{OE})$  is LOW when  $\overline{RAS}$  goes LOW.
- 24. NON-TRANSFER Command means that  $\overline{TR}/(\overline{OE})$  is HIGH when  $\overline{RAS}$  goes LOW.
- 25. Measured with a load equivalent to 2 TTL gates and 50pF.
- 26. The parameter is a "conditionally" guaranteed parameter that is specified to aid with device application. It is not directly verified by a specific test but is used, along with several other parameters, in the performance verification of other attributes..

# MICHON

### DC ELECTRICAL CHARACTERISTICS

(Notes 3, 4, 5) (Vcc =  $5.0V \pm 10\%$ )

TEM	TEST	NOTES	SYMBOL	ALT.	CONDITIONS	DEVICE	GROUP A	LIN	IITS	UNIT
				SYMBOL	-55°C ≤ Tc ≤ +110°C	TYPE	SUBGROUPS	MIN	MAX	
1	Average operating current during READ or WRITE cycles.	4	Icc1		RAS and CAS = cycling, <sup>t</sup> RC = <sup>t</sup> RC (min), SAM in Standby	All	1, 2, 3		40	mA
2	Average operating current during PAGE-MODE READ or WRITE cycles.	4	lcc2		$\overline{RAS} = V_{IL}, \overline{CAS} =$ cycling, ${}^{t}PC = {}^{t}PC$ (min), SAM in Standby	All	1, 2, 3		40	mA
3	Standby current: TTL input levels		lcc3		RAS = CAS = VIH after 8 RAS cycles, SAM in Standby	All	1, 2, 3		10	mA
4	Standby current: CMOS input levels		Icc4		RAS = CAS = Vcc -0.2V after 8 RAS cycles. All other inputs at Vcc -0.2V or Vss +0.2V, SAM in Standby	All	1, 2, 3		6	miA
5	Refresh current: RAS only refresh		lcc5		RAS = Cycling, CAS = VIH, SAM in Standby	All	1, 2, 3		30	mA
6	Refresh current: CAS-before-RAS refresh	5	Icc6		RAS and CAS = cycling, SAM in Standby	All	1, 2, 3		30	mA
7	Data transfer current: DRAM-TO-SAM or SAM-TO-DRAM		lcc7		Data transfer cycle, SAM in Standby	All	1, 2, 3		60	mA
8	Average operating current during READ or WRITE cycles.	4	lcc8		RAS and CAS = cycling, <sup>t</sup> RC = <sup>t</sup> RC (min), SAM active, <sup>t</sup> SC = <sup>t</sup> SC (min)	Ali	1, 2, 3		60	mA
9	Average operating current during PAGE-MODE READ or WRITE cycles.	4	lcc9		RAS = VIL, CAS = cycling, <sup>t</sup> PC = <sup>t</sup> PC (min), SAM active, <sup>t</sup> SC = <sup>t</sup> SC (min)	All	1, 2, 3		60	mA
10	Standby current: TTL input levels		Icc10		RAS = CAS = VIH after 8 RAS cycles, SAM active, <sup>t</sup> SC = <sup>t</sup> SC (min)	All	1, 2, 3		30	mA
11	Standby current: CMOS input levels		Ícc11		RAS = CAS = Vcc -0.2V after 8 RAS cycles. All other inputs at Vcc -0.2V or Vss +0.2V, SAM active, tSC = tSC (min)	All	1, 2, 3		25	mA
12	Refresh current: RAS only refresh		lcc12		RAS = Cycling, CAS = VIH, SAM active,  tSC = tSC (min)	All	1, 2, 3		50	mA
13	Refresh current: CAS-before-RAS refresh	5	Icc13		RAS and CAS = cycling, Sam active,  tSC = tSC (min)	All	1, 2, 3		50	mA

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### **DRAM TIMING PARAMETERS**

### DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 10, 11, 17) ( $Vcc = 5.0V \pm 10\%$ )

ITEM	TEST	NOTES	SYMBOL	ALT. Symbol	CONDITIONS -55°C ≤ Tc ≤ +110°C	DEVICE TYPE	GROUP A Subgroups	MIN	IMITS Max	UNIT
1	Random READ or WRITE	6, 7	<sup>t</sup> RC	tc(RD)	All cycle times	-12	9, 10, 11	220	MAX	ns
	cycle time	ļ		tc(W)	assume <sup>t</sup> T = 5ns.	-15 -20		260 300		
2	READ-MODIFY-WRITE	20, 21	t <sub>RWC</sub>	t <sub>c(RDW)</sub>		-12	9, 10, 11	295		ns
-	cycle time	20, 21	11110	C(TIDVV)		-15	3, 10, 11	345		113
	•					-20		400		
3	PAGE-MODE READ-	6, 7,	<sup>t</sup> PRWC	tc(PRDW)		-12	9, 10, 11	150		ns
	MODIFY-WRITE cycle time	26				-15		175		
		-				-20		200		<u> </u>
4	PAGE-MODE READ or	6, 7,	<sup>t</sup> PC	t <sub>c(PRD)</sub>		-12	9, 10, 11	90		ns
- 1	WRITE cycle time	26		tc(PW)		-15		110		
		+	tnac	1 (5)	01 100 5	-20	0.10.11	200		-
5	Access time from RAS	7, 8	tRAC	<sup>t</sup> a(R)	CL = 100pF	-12 -15	9, 10, 11	120 150		ns
						-20		200		
6	Access time from CAS	7, 9	t <sub>CAC</sub>	ta(C)	CL = 100pF	-12	9, 10, 11	60		ns
	riodede time mem erie	',"	0,10	(0)	02 = 100pi	-15	0, 10, 11	75		
						-20		100		
7	RAS pulse width		<sup>t</sup> RAS	tw(RL)		-12	9, 10, 11	120	10,000	ns
						-15		150	10,000	
						-20		200	10,000	
8	RAS pulse width		<sup>t</sup> RASP	<sup>t</sup> w(RLP)		-12	9, 10, 11	120	100,000	
	(PAGE-MODE)	1				-15		150	100,000	
	5-5		t <sub>RSH</sub>	t. (01 DL1)		-20			100,000	
9	RAS hold time		HSH	th(CLRH)		-12 -15	9, 10, 11	60 75		ns
						-20		100		i
10	RAS precharge time		t <sub>RP</sub>	tw(RH)		-12	9, 10, 11	90		ns
'	The precharge line		'"	<b>W</b> (1111)		-15	3, 10, 11	100		113
						-20		100		
11	CAS pulse width		t <sub>CAS</sub>	tw(CL)		-12	9, 10, 11	60	10,000	ns
						-15		75	10,000	
						-20		100	10,000	<u> </u>
12	CAS hold time	26	t <sub>CSH</sub>	th(RLCH)		-12	9, 10, 11	120		ns
						-15		150		
-10	010 mark mark have	+	t <sub>CPN</sub>	1 (01)		-20	0.40.44	200		<del>  </del>
13	CAS precharge time	26	CPN	<sup>t</sup> w(CH)		-12 -15	9, 10, 11	20 25		ns
		1				-20		35		
14	CAS precharge time	19,	<sup>t</sup> CP	tw(CH)		-12	9, 10, 11	20		ns
	(PAGE-MODE)	26	0.	"(0,		-15	, 10, 11	25		
	,					-20		35		
15	RAS to CAS delay	13	t <sub>RCD</sub>	<sup>t</sup> RLCL		-12	9, 10, 11	20	60	ns
	•			İ		-15		20	75	
						-20		25	85	<u> </u>
16	CAS to RAS	26	<sup>t</sup> CRP	<sup>t</sup> CHRL		-12	9, 10, 11	10		ns
	precharge time					-15		10		
			L	L	1	-20	L	10	<u> </u>	Ь

# DRAM TIMING PARAMETERS (Continued) DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes 3, 4, 5, 10, 11, 17) ( $Vcc = 5.0V \pm 10\%$ )

ITEM	TEST	NOTES	SYMBOL	ALT.	CONDITIONS	DEVICE	GROUP A	L	IMITS	UNI
				SYMBOL	-55°C ≤ Tc ≤+110°C	TYPE	SUBGROUPS	MIN	MAX	l
17	Row address set-up time		<sup>t</sup> ASR	<sup>t</sup> su(RA)	All cycle times	-12	9, 10, 11	0		ns
					assume <sup>t</sup> T = 5ns.	-15		0		
						-20		0		4
18	Row address hold time		<sup>t</sup> RAH	<sup>t</sup> h(RA)		-12	9, 10, 11	15		ns
						-15		15		1
						-20		20		┷
19	Column address		<sup>t</sup> ASC	<sup>t</sup> su(CA)		-12	9, 10, 11	0		ns
	set-up time		i			-15		0		
				+		-20		0		+
20	Column address		<sup>t</sup> CAH	th(CLCA)		-12	9, 10, 11	20		ns
	hold time					-15		25		
			1	t		-20		35		+
21	Column address		<sup>t</sup> AR	<sup>t</sup> h(RLCA)		-12	9, 10, 11	70		ns
	hold time (referenced to RAS)					-15 -20		80 100		
22	<del></del>		tRCS	t <sub>su(RD)</sub>			0.40.44	1		+_
22	READ command set-up time		HUS	Su(HD)		-12 -15	9, 10, 11	0		ns
	Set-up time					-20		0		
23	READ command	14,	t <sub>RCH</sub>	th(CHRD)		-12	9, 10, 11	0		ns
23	hold time	26	поп	II(CHND)		-15	9, 10, 11	0		118
	(referenced to CAS)					-20		0		ł
24	READ command	26	t <sub>RRH</sub>	th(RHRD)		-12	9, 10, 11	0		ns
	hold time	20	'''''	()	i	-15	0, 10, 11	0		'''
	(referenced to RAS)					-20		0		İ
25	WE command	16	twcs	t <sub>su(WCL)</sub>		-12	9, 10, 11	0		ns
	set-up time			, ,		-15	·	0		ļ
						-20		0		$\perp$
26	WRITE command		tWCH	th(CLW)		-12	9, 10, 11	25		ns
	hold time		!			-15		30		ļ
						-20		45		
27	WRITE command		tWCR	th(RLW)		-12	9, 10, 11	80		ns
	hold time			İ		-15		90		
	(referenced to RAS)					-20		120		
28	WRITE command		tWP	<sup>t</sup> w(W)		-12	9, 10, 11	25		ns
	pulse width					-15		30		
			1	t		-20	<del>                                     </del>	45		+
29	WRITE command to		<sup>t</sup> RWL	<sup>t</sup> h(WRH)		-12	9, 10, 11	30		ns
	RAS lead time	1	1			-15 -20		35 50		1
	WEITE		tCWL	ti augus			0.40.44	+		+
30	WRITE command to CAS lead time		CWL	th(WCH)		-12	9, 10, 11	30 35		ns
	CAS lead time	1		}		-15 -20		50	ļ	-
31	Data in cot up time	15	tDS	t <sub>su(D)</sub>		-12	9, 10, 11	0		ns
31	Data-in set-up time	15	פט	Su(D)		-12	9, 10, 11	0		108
			1			-20		10	l	
32	Data-in hold time	15	<sup>t</sup> DH	th(CLD)		-12	9, 10, 11	20		ns
JŁ	(referenced to CAS)	'3	J.,	II(OLD)		-15	3, 10, 11	25		'"
	1				1	-20		50		- 1

# DRAM TIMING PARAMETERS (Continued) DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes 3, 4, 5, 10, 11, 17) ( $Vcc = 5.0V \pm 10\%$ )

ITEM	TEST	NOTES	SYMBOL	ALT.	CONDITIONS	DEVICE	GROUP A		IMITS	UNIT
-	Data in baldaina	-	<sup>t</sup> DH	SYMBOL	-55°C ≤ Tc ≤ +110°C	TYPE	SUBGROUPS	MIN	MAX	1
33	Data-in hold time (referenced to ME/WE		.DH	<sup>t</sup> h(WLD)	All cycle times assume <sup>t</sup> T = 5ns.	-12 -15	9, 10, 11	20 25		ns
	(referenced to MIL/VVL				assume 1 = 5ns.	-20		50		
34	Data-in hold time		t <sub>DHR</sub>	th(RLD)		-12	9, 10, 11	80		ns
٠. ا	(referenced to RAS		5	(1125)		-15	0, 10, 11	90		'''
						-20		120		
35	CAS to WE delay	16,20	tCMD	t <sub>CLWL</sub>		-12	9, 10, 11	80		ns
						-15		95		
						-20		130		—
36	RAS to WE delay	16, 20	<sup>t</sup> RWD	t <sub>RLWL</sub>		-12	9, 10, 11	150		ns
						-15		185		
		+	twos	† a.e.		-20		220		+
37	ME/WE (Mask Write Mode) to RAS set-up time	26	twsr	<sup>t</sup> su(WE)		-12 -15	9, 10, 11	0		ns
	Mode) to HAS set-up time					-20		0		
38	ME/WE (Mask Write	26	t <sub>RWH</sub>	th(WE)		-12	9, 10, 11	10	<u> </u>	ns
36	Mode) to RAS hold time	20	110011	11(**)		-15	3, 10, 11	15	ļ	113
	mode, to the more time					-20		20		
39	Mask Data (DQ) to	26	t <sub>MS</sub>	t <sub>su(W)</sub>		-12	9, 10, 11	0		ns
	RAS set-up time			. ,		-15	, ,	0		
						-20		0		
40	Mask Data (DQ) to		<sup>t</sup> MH	th(W)		-12	9, 10, 11	20		ns
	RAS hold time					-15		25		
						-20		40		
41	Transition time	26	t <sub>T</sub>	t <sub>T</sub>		-12	9, 10, 11	3	50	ns
	(rise or fall)					-15		3	50	
			<del></del>	·	<u></u>	-20	<u> </u>	3	50	+
42	Refresh period		<sup>t</sup> REF	<sup>t</sup> c(RF)	All 256 row	-12 -15	9, 10, 11		4	ms
	(256 cycle)				addresses must be accessed.	-15			4 4	
43	CAS set-up time	+	t <sub>CSR</sub>	tsu(RCR)	be accessed.	12	9, 10, 11	ļ	10	ns
43	(CAS-before-RAS refresh)		Con	Su(non)		-15	9, 10, 11		10	1115
	(67.6 20.6.6 12.6 10.1001.)					-20			10	
44	CAS hold time	22	tCHR	th(RRC)		-12	9, 10, 11		25	ns
	(CAS-before-RAS refresh			''(' '' ' ' '		-15			30	'
						-20			40	
45	CAS to output in	26	tCLZ			-12	9, 10, 11	1	5	ns
	low-Z					-15			5	
						-20		-	10	-
46	Output buffer	12	<sup>t</sup> OFF	<sup>t</sup> dis(CH)		-12	9, 10, 11	0	25	ns
	turn-off delay					-15		0	30	
	(referenced from CAS)	+	to-	t (==:	-	-20	0.45.1:	0	35	+
47	Output enable		<sup>t</sup> OE	ta(OE)	[	-12	9, 10, 11		25	ns
	(referenced from TR/OE)					-15 -20			30 45	
10	Output disable		t <sub>OD</sub>	tdis(OE)		-12	9, 10, 11	+	25	ns
48	(referenced from		00	uis(OE)		-12	9, 10, 11		30	lus
	TR/OE)					-20			35	

# MILITARY VRAM

# TRANSFER AND MODE CONTROL TIMING PARAMETERS ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes 3, 4, 5, 10, 11, 17) (Vcc = $5.0V\pm10\%$ )

ITEM	TEST	NOTES	SYMBOL	ALT.	CONDITIONS	DEVICE	GROUP A	L	IMITS	UNIT
				SYMBOL	-55°C ≤ Tc ≤ +110°C	TYPE	SUBGROUPS	MIN	MAX	1_
1	TRANSFER command to RAS set-up time	23	<sup>t</sup> TS	<sup>t</sup> su(DT)	All cycle times assume <sup>t</sup> T = 5ns.	-12 -15 -20	9, 10, 11	0 0		ns
2	TRANSFER command to RAS hold time	23	<sup>t</sup> RTH	<sup>t</sup> h(DT)		-12 -15 -20	9, 10, 11	90 100 140		ns
3	TRANSFER command to CAS hold time	23	<sup>t</sup> CTH	<sup>t</sup> h(CLDT)		-12 -15 -20	9, 10, 11	30 35 50		ns
4	TRANSFER command to to SC lead time	23, 26	<sup>t</sup> TSL	<sup>t</sup> SHDH		-12 -15 -20	9, 10, 11	5 10 20		ns
5	TRANSFER command to RAS lead time	23, 26	<sup>t</sup> TRL	<sup>t</sup> su(DTRH)		-12 -15 -20	9, 10, 11	10 10 20		ns
6	TRANSFER command to RAS delay time	23, 26	<sup>t</sup> TRD	<sup>t</sup> h(DTRH)		-12 -15 -20	9, 10, 11	15 20 40		ns
7	TRANSFER command to CAS lead time	23, 26	<sup>t</sup> TCL	<sup>t</sup> su(DTCH)		-12 -15 -20	9, 10, 11	10 10 20		ns
8	TRANSFER command to CAS delay time	23, 26	<sup>t</sup> TCD	th(DTCH)		-12 -15 -20	9, 10, 11	15 20 40	-	ns
9	First SC edge to TRANSFER command delay time	26	<sup>t</sup> TSD	<sup>t</sup> h(SCDT)		-12 -15 -20	9, 10, 11	10 20 40		ns
10	SAM-to-DRAM (Write) TRANSFER command to RAS hold time		<sup>t</sup> RTHW	<sup>t</sup> h(TR)		-12 -15 -20	9, 10, 11	15 15 30		ns
11	Serial output buffer turn off delay from RAS	26	tSDZ			-12 -15 -20	9, 10, 11	10 10 10	50 60 80	ns
12	SC to RAS set-up time	26	<sup>t</sup> SRS	<sup>t</sup> su(SCRL)		-12 -15 -20	9, 10, 11	40 45 60		ns
13	RAS to SC delay time	26	<sup>t</sup> SRD	<sup>t</sup> RHSC		-12 -15 -20	9, 10, 11	30 35 50		ns
14	Serial data input to SE delay time	26	<sup>t</sup> SZE			-12 -15 -20	9, 10, 11	0 0		ns
15	RAS to SD buffer turn on time	26	<sup>t</sup> SRO			-12 -15 -20	9, 10, 11	0 0		ns
16	Serial data input delay from RAS	26	tSDD			-12 -15 -20	9, 10, 11	55 60 80		ns



MT42C4064 883C

### TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes 3, 4, 5, 10, 11, 17) (Vcc =  $5.0V \pm 10\%$ )

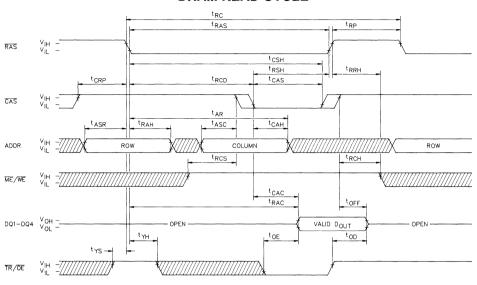
ITEM	TEST	NOTES SYMBOL ALT. CONDITIONS I		DEVICE	GROUP A	L	IMITS	UNIT		
				SYMBOL	-55°C ≤ Tc ≤ +110°C	TYPE	SUBGROUPS	MIN	MAX	
17	Serial data input to RAS delay time	26	<sup>t</sup> SZS		All cycle times assume <sup>t</sup> T = 5ns.	-12 -15 -20	9, 10, 11	0 0 0		ns
18	Serial input mode Enable (SE) to RAS set-up time	26	<sup>t</sup> ESR	<sup>t</sup> su(SE)		-12 -15 -20	9, 10, 11	0 0 0		ns
19	Serial input mode Enable (SE) to RAS hold time	26	<sup>t</sup> REH	<sup>t</sup> h(SE)		-12 -15 -20	9, 10, 11	10 15 30		ns
20	NON-TRANSFER command to RAS set-up time	24, 26	<sup>t</sup> YS	<sup>t</sup> su(DTH)		-12 -15 -20	9, 10, 11	0 0 0		ns
21	NON-TRANSFER command to RAS hold time	24, 26	<sup>t</sup> YS	<sup>t</sup> h(DTH)		-12 -15 -20	9, 10, 11	10 10 20		ns

### MICHON

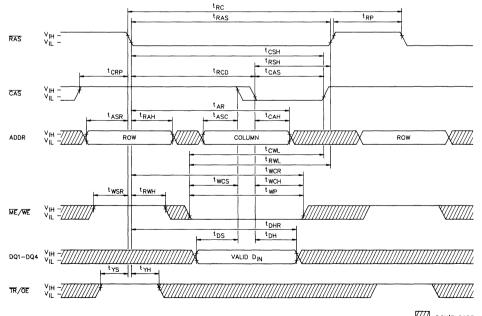
# TRANSFER AND MODE CONTROL TIMING PARAMETERS ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes 3, 4, 5, 10, 11, 17) (Vcc = 5.0V ± 10%)

ITEM TEST NOTES SYMBOL ALT. CONDITIONS DEVICE GROUP A LIMITS UNIT SYMBOL TYPE **SUBGROUPS** MIN MAX -55°C ≤ Tc ≤ +110°C 1 Serial clock cycle time 26 tsc. tc(SC) All cycle times 12 40 9, 10, 11 assume tT = 5ns. -15 60 -20 80 tSAC ta(SC) 2 Access time from SC -12 9, 10, 11 40 -15 60 -20 80 t<sub>SP</sub> tw(SCH) SC precharge time -12 9, 10, 11 10 -15 20 -20 30 tSAS 4 SC pulse width 26 tw(SCL) 9, 10, 11 10 -12 -15 20 -20 30 5 Access time from SE 26 <sup>t</sup>SFA ta(SE) -12 9, 10, 11 30 40 -15 -20 60 <sup>t</sup>SEP tw(SEH) 6 SE precharge time 26 -12 9, 10, 11 15 -15 20 -20 30 tSE 7 tw(SEL) SE pulse width 26 -12 9, 10, 11 15 -15 20 -20 30 <sup>t</sup>SOH 8 Serial data out hold th(SCHD) 26 -12 9, 10, 11 10 time after SC high -15 10 -20 10 tSEZ 9 26 tdis(SE) Serial output buffer -12 9, 10, 11 0 25 turn off delay from SE 30 -15 0 -20 0 50 t<sub>SDS</sub> tsu(SD) 10 Serial data in -12 9, 10, 11 0 set-up time -15 0 -20 0 11 Serial data in t<sub>SDH</sub> th(SD) -12 9. 10. 11 20 hold time -15 25 -20 40 12 tsws Serial input (Write) tsu(SEL) 26 -12 9, 10, 11 0 enable set-up time -15 0 0 -20 tswH 13 Serial input (Write) 26 th(SEL) -12 9, 10, 11 35 enable hold time -15 45 60 -20 14 Serial input (Write) 26 tswis <sup>t</sup>su(SEH) -12 9, 10, 11 0 ns disable set-up time -15 0 -20 0 tswiH 15 Serial input (Write) 26 th(SEH) -12 9, 10, 11 35 ns disable hold time -15 45 -20 60

### **DRAM READ CYCLE**

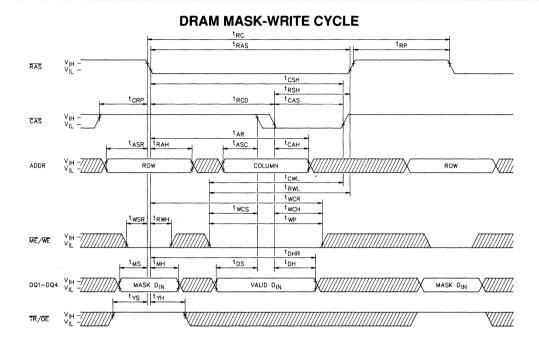


### DRAM EARLY-WRITE CYCLE

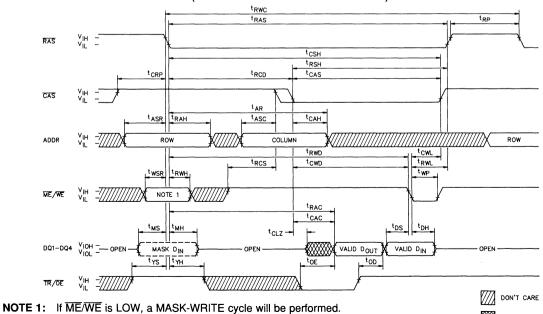


DON'T CARE

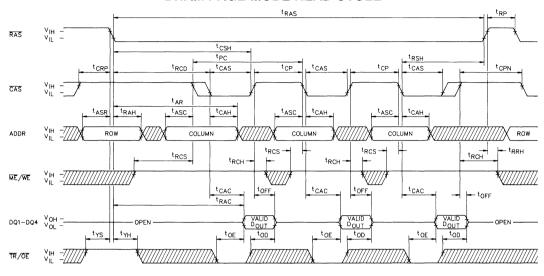
UNDEFINED



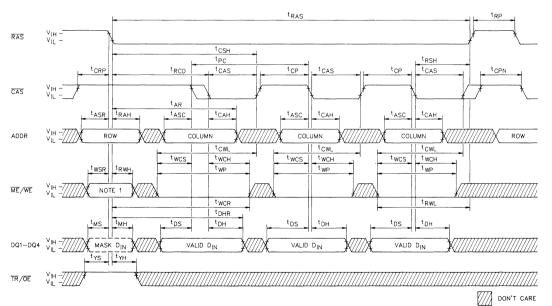
# DRAM READ-WRITE CYCLE (READ-MODIFY-WRITE CYCLE)



### DRAM PAGE-MODE READ CYCLE

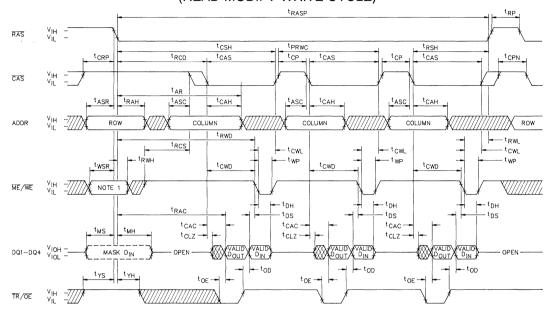


### DRAM PAGE-MODE EARLY-WRITE CYCLE



**NOTE 1:** If ME/WE is LOW, a MASK-WRITE cycle will be performed.

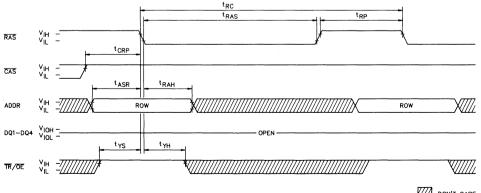
# DRAM PAGE-MODE READ-WRITE CYCLE (READ-MODIFY-WRITE CYCLE)



NOTE: 1: If ME/WE is LOW, a MASK-WRITE cycle will be performed

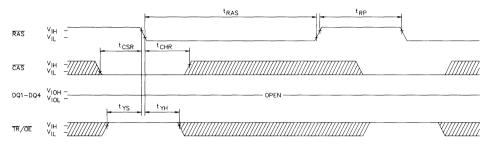
### **RAS ONLY REFRESH CYCLE**

 $(\overline{ME}/\overline{WE} = Don't Care)$ 

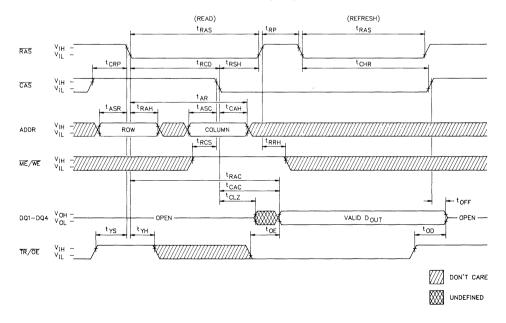


### **CAS-BEFORE-RAS REFRESH CYCLE**

 $(A_0 - A_7 \text{ and } \overline{\text{ME}}/\overline{\text{WE}} \text{ are Don't Care.})$ 



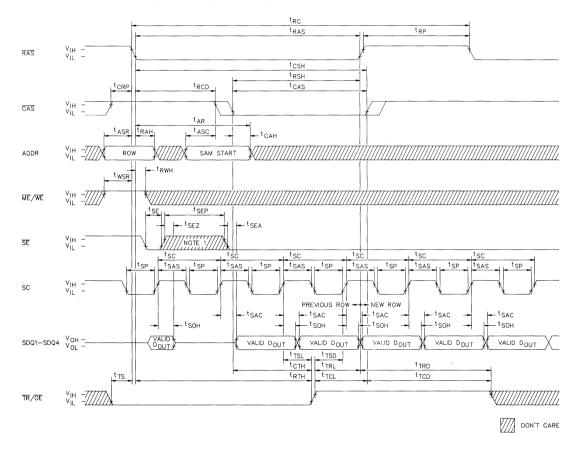
### **HIDDEN REFRESH CYCLE**



**NOTE:** A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case  $\overline{\text{ME/WE}} = \text{LOW}$  (when  $\overline{\text{CAS}}$  goes LOW) and  $\overline{\text{TR/OE}} = \text{HIGH}$ .

# DRAM-TO-SAM TRANSFER (READ TRANSFER)

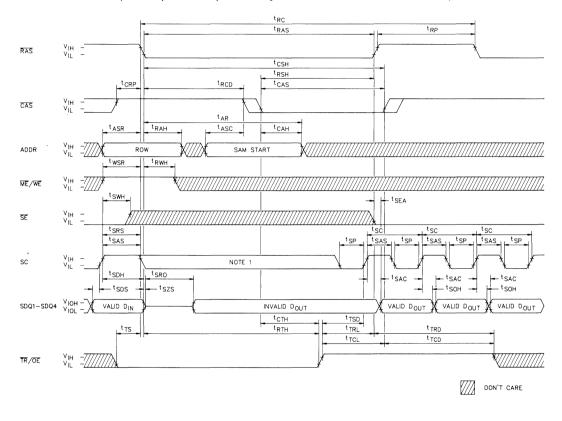
(When part was previously in the SERIAL OUTPUT mode.)



NOTE 1: This SE pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

# DRAM-TO-SAM TRANSFER (READ TRANSFER)

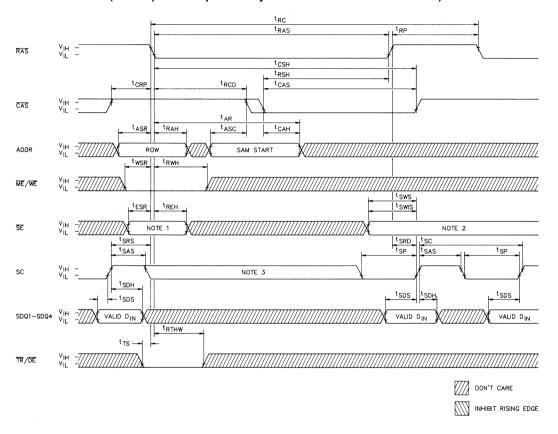
(When part was previously in the SERIAL INPUT mode.)



NOTE 1: There must be no rising edges on the SC input during this time period.

### SAM-TO-DRAM TRANSFER (WRITE TRANSFER)

(When part was previously in the SERIAL INPUT mode.)



**NOTE 1:** If SE is LOW, the SAM data will be transferred to the DRAM.

If SE is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

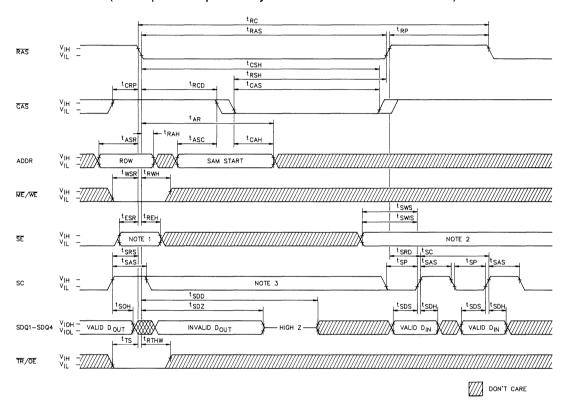
NOTE 2: SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless

of SE.

NOTE 3: There must be no rising edges on the SC input during this time period.

# SAM-TO-DRAM TRANSFER (WRITE TRANSFER/PSEUDO WRITE TRANSFER)

(When part was perviously in the SERIAL OUTPUT mode.)



**NOTE 1:** If SE is LOW, the SAM data will be transferred to the DRAM.

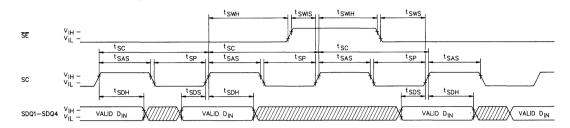
If SE is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless

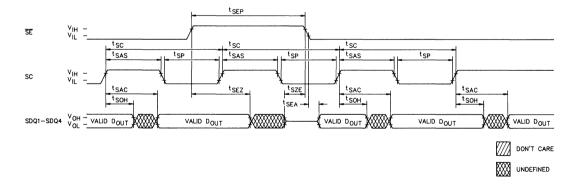
of SE.

NOTE 3: There must be no rising edges on the SC input during this time period.

### **SAM SERIAL INPUT**



### **SAM SERIAL OUTPUT**





20. Group B

21. Group C

22. Group D

### MT42C4064 883C

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510	Conditions	- Comment
1. MIL-STD-883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan	Approved by DESC
<ol> <li>Certification</li> <li>Traceability</li> <li>Country of Origin (Not required for 883C)</li> </ol>	and submit to qualifying activity. Manufacturer's QA survey Traceable to wafer production lot. N/A	Self audit Computer lot history records Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD-883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018 SEM Monitors	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD-883, Class B, Rev. C, Me	thod 5004 Screening	
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration 11. Hermeticity	Method 2001, cond. E	100%
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented data sheet @ +118°C	100%
13. Burn-in	Method 1015, 162 hours @ 125°C	100%
14. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +113°C 5% PDA and in-line Group A per method 5005	100%
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection p	er Method 5005 (attributes data only)	
19. Group A	Manufacturer's documented	
20.0	data sheet	Each lot/sublot

Package functional and

(1000 hr. operating life)

Package related test

construction tests

Die related

7-01		

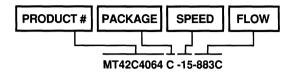
Each package type

Each package type Generic every 26 weeks

Micro circuit group/every quarter

on each lot

### ORDER INFORMATION



The Micron MT42C4064 is functionally equivalent to other manufacturer's products meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the high speed,

low power CMOS double poly, single metal process. Micron's QUALITY ASSURED policy is to offer prompt, accurate, and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply, temperature, and refresh range than specified. Each unit receives accelerated burn-in and and several hours of AMBYX<sup>TM</sup> system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

# MILITARY SRAM

# 2K x 8 SRAM

### ADDITIONAL MILITARY SPECIFICATIONS

- SMD 84036
- JAN (consult factory for reference number)
- RAD-tolerant (consult factory)

### **FEATURES**

- Battery Backup 2 volt data retention
- High speed: 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS	MARKING
Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Ceramic DIP (300 mil)	С
Ceramic LCC	EC
Two Volt Data Retention	L

#### PIN ASSIGNMENT (Top View) 24L/300 DIP 28L/LCC 24 | Vcc 1 28 27 A6 2 A8 A3 [] A2 [ 22 A9 A5 🗌 3 NC [ 21 | WE NC [ Πĸc A4 [] AιΓ 21 NC **АО** Г 2011正 аз П 20 OE 001 19 008 DQ2 A2 | 19 A10 18 007 003 Vss 006 005 A1 Α0 Π 17 DQ8 8 **ECE** DQ1 $\Pi$ 9 16 D07 DQ2 15 DQ6 DQ3 14 ∏ DQ5 Vss | 12 13 D04 CF

### GENERAL DESCRIPTION

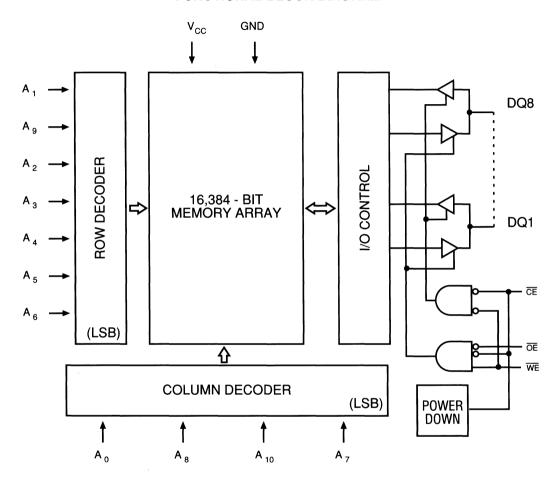
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology. All fabrication is 100% domestic.

For flexibility in high speed memory applications, Micron offers chip enable  $(\overline{CE})$  on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ( $\overline{WE}$ ) and  $\overline{CE}$  inputs are both LOW. Reading is accomplished when  $\overline{WE}$  remains HIGH and  $\overline{CE}$  goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

### **FUNCTIONAL BLOCK DIAGRAM**



### **TRUTH TABLE**

MODE	OE	CE	WE	DQ	POWER
STANDBY	X	Н	Х	HIGH Z	STANDBY
READ	L	L	Н	DOUT	ACTIVE
READ	Н	L	Н	HIGH Z	ACTIVE
WRITE	Х	L	L	DIN	ACTIVE

### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any input relative to Vss2.0 to	+7.0V
Voltage on Vcc supply relative to Vss1.0V to	+7.0V
Storage Temperature65°C to +	-150°C
Power Dissipation	1 Watt
Short Circuit Output Current	50mA
Lead Temperature (soldering, 10 seconds)+	-260°C
Junction Temperature+	-175°C

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

 $(-55^{\circ}\text{C} \le \text{T}_{\text{C}} \le 125^{\circ}\text{C}, \, \text{Vcc} = 5\text{V} \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		Vih	2.2	6.0	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VCC	ILı	-10	10	μА	
Output Leakage Current	Outputs Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	Vон	2.4		V	1
Output Low Voltage	loL = 8.0mA	Vol		0.4	V	1

					MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	CE ≤ V <sub>I</sub> L, Vcc = Max., Outputs Open	lcc	130	120	110	100	95	mA	3
	$\overline{CE} \ge V_{IH}, V_{CC} = Max.,$ $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}} Hz$	IsbT1	50	45	40	40	40	mA	
Power Supply Current: Standby	$\overline{\text{CE}}$ ≥ Vih, all other inputs ≤ Vil or ≥ Vih, Vcc = Max., f = 0Hz	Isвт2	35	35	35	35	35	mA	
	$\overline{\text{CE}} \ge (\text{Vcc} - 0.2),  \text{Vcc} = \text{Max.},$ all other inputs $\le 0.2\text{V}$ or $\ge (\text{Vcc} - 0.2\text{V}),  \text{f} = \text{OHz}$	IsBC2	10	10	10	10	10	mA	

### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz,	Cı		8	pF	4
Output Capacitance	Vcc = 5V	Co		8	pF	4

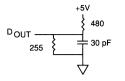
### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Note 5) (-55°C  $\leq$  T $_{C}$   $\leq$  125°C, Vcc = 5V  $\pm$  10%)

DESCRIPTION		-1	5	-2	20	-2	25	-3	80	-35	5		
DESCRIPTION	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	<sup>t</sup> RC	15		20		25		30		35		ns	
Address access time	t <sub>AA</sub>		15		20		25		30		35	ns	
Chip enable access time	t <sub>ACE</sub>		15		20		25		30		35	ns	
Output hold from address change	t <sub>OH</sub>	3		3		3		3		3		ns	
Chip enable to output in low Z	t <sub>LZCE</sub>	5		5		5		5		5		ns	
Chip disable to output in high Z	tHZCE		10		15		15		20		20	ns	6,7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		15		20		25		30		35	ns	
Output enable access time	<sup>t</sup> AOE		12		15		15		20		20	ns	
Output enable to output in low Z	<sup>t</sup> LZOE	0		0		0		0		0		ns	
Output disable to output in high Z	t <sub>HZOE</sub>		10		15		15		20		20	ns	6
WRITE Cycle													
WRITE cycle time	twc	15		20		25		30		35		ns	
Chip enable to end of write	tcw	13		15		20		25		30		ns	
Address valid to end of write	t <sub>AW</sub>	15		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	0		0		0		0		0		ns	
Write pulse width	t <sub>WP</sub>	13		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		12		15		15		15		ns	
Data hold time	<sup>t</sup> DH	0		0		0		0		0		ns	
Write disable to output in low Z	<sup>t</sup> LZWE	0		0		0		0		0		ns	
Write enable to output in high Z	<sup>t</sup> HZWE	0	10	0	12	0	15	0	15	0	15	ns	6

### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2



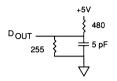


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

### **NOTES**

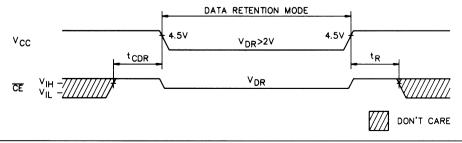
- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs  $unloaded, and \ f = \frac{1}{TRC(MIN)} = \frac{1}{TWC(MIN)} = Hz.$
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- 6. <sup>t</sup>HZCE and <sup>t</sup>HZWE are tested with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from

- steady state voltage, allowing for actual tester RC time constant.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8. WE is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

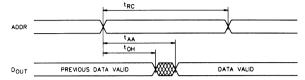
### DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
VDR	Vcc for Retention Data			2			٧
ICCDR	Data Retention Current	CE ≥ (Vcc - 0.2V)   Vin ≥ (Vcc - 0.2V)   or ≤ 0.2V	Vcc=2v	_	95	1000	μА
			Vcc=3v	_	350	1500	μΑ
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

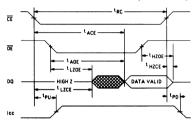
### LOW Vcc DATA RETENTION WAVEFORM



### **READ CYCLE NO. 1 (8, 9)**

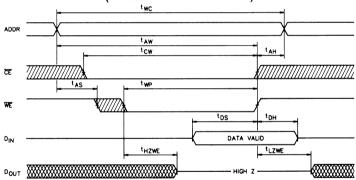


### **READ CYCLE NO. 2 (7, 8, 10)**



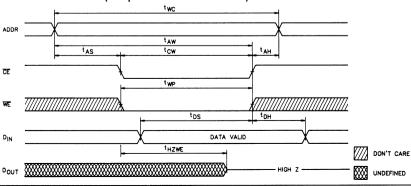
### **WRITE CYCLE NO. 1**

(Write Enable Controlled)



### **WRITE CYCLE NO. 2**

(Chip Enable Controlled)



22. Group D

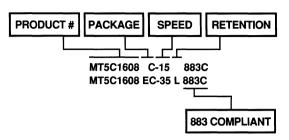
### MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW								
Description of Requirements and Screens	Methods and Test Conditions	Comment						
General MIL-M-38510								
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved						
<ol> <li>Certification</li> <li>Traceability</li> <li>Country of Origin (Not required for 883C)</li> </ol>	Manufacturer's QA survey Traceable to wafer production lot. N/A	Self audit Computer lot history records Devices manufactured, assembed and tested in Boise, Idaho USA.						
MIL-STD-883 Fabrication								
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line						
6. Wafer Fabrication	Method 2018 SEM Monitors	100%						
7. Assembly	Class B Process Monitors	100%						
MIL-STD-883, Class B, Rev. C, Met	hod 5004 Screening	······································						
8. Internal Visual	Method 2010, cond. B	100%						
9. Temperature Cycle	Method 1010, cond. C	100%						
<ul><li>10. Constant Acceleration</li><li>11. Hermeticity</li></ul>	Method 2001, cond. E	100%						
A. Fine Leak	Method 1014, cond. A	100%						
B. Gross Leak	Method 1014, cond. C	100%						
12. Initial Electricals	Manufacturer's documented data sheet @ +125°C	100%						
13. Burn-in	Method 1015	100%						
14. Final Electrical Post	Method 5004, Class B,	100%						
Burn-in Test	3.1.16 @ -55°C, +25°C, +125°C 5% PDA and in-line Group A							
15 Markina	per method 5005	1000						
15. Marking 16. External Visual	Method 2015 Method 2009	100% 100%						
17. Pack/Ship	Includes C of C, with QCI	100%						
17.1 ack/ 5hip	data (attributes only)	100 %						
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D						
Quality Conformance Inspection po	er Method 5005 (attributes data only)							
19. Group A	Manufacturer's documented data sheet	Each lot/sublot						
20. Group B	Package functional and construction tests	Each package type on each lot						
21. Group C	Die related	on each for Micro circuit group/every quarter						

Each package type Generic every 26 weeks

Package related test

### ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's 883 compliant devices. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

# MILITARY SRAM

# 8K x 8 SRAM

### ADDITIONAL MILITARY SPECIFICATIONS

- SMD 85525
- JAN (consult factory for reference number)
- RAD-tolerant (consult factory)

### **FEATURES**

- Battery Backup 2 volt data retention
- High speed: 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- · All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS	MARKING
Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Ceramic DIP (300 mil)	C
Ceramic DIP (600 mil)	CW
Ceramic LCC (28 leads)	EC
Ceramic LCC (32 leads)	ECW
Two Volt Data Retention	L

### PIN ASSIGNMENT (Top View) 28L/300/600 DIP 28L/LCC A A I S 28 ] Vcc ис Ц 12827 27 | VE A12 [ 26 CES A5 d 5 25 DAB 4416 24 DA9 A3 07 25 A8 A6 [ A2 08 25 P DE 24 1 49 DAIG A5 [ 20 DCEI **A0** C10 19 DQ8 23 A11 DQ1 d11 DQ2 (12 18 þ pq7 22 DE ΑЗ 2 × 500 2005 2005 21 A10 A2 [ 20 T CE1 **ECE** A0 10 19 DQ8 18 ד סע 🏻 no1 ∏ 11 32L/LCC DQ2 ∏12 17 DQ6 DQ3 | 13 16 DQ5 29 A8 15 DQ4 Vss[]14 28 49 27 DA11 CH 26 NC A10 CEI 21 DQ7 4 15 1617 181920 **ECF**

### GENERAL DESCRIPTION

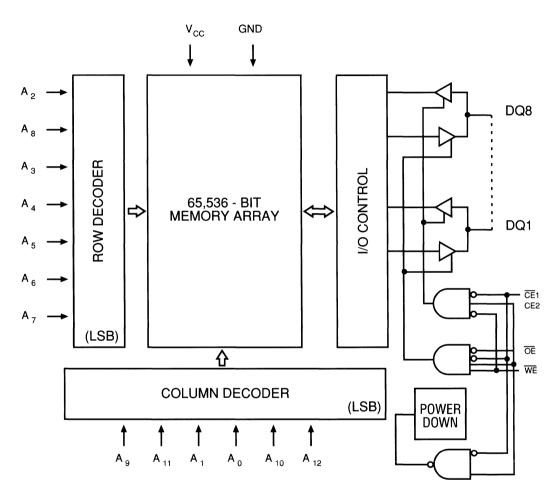
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology. All fabrication is 100% domestic.

For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

### **FUNCTIONAL BLOCK DIAGRAM**



### **TRUTH TABLE**

MODE	CE1	CE2	WE	ŌĒ	DQ	POWER
STANDBY	Н	Х	Х	Х	HIGH Z	STANDBY
STANDBY	Х	L	Х	Х	HIGH Z	STANDBY
READ	L	Н	Н	L	DOUT	ACTIVE
READ	L	Н	Н	Н	HIGH Z	ACTIVE
WRITE	L	Н	L	Х	DIN	ACTIVE

### **ABSOLUTE MAXIMUM RATINGS\***

 \*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 $(-55^{\circ}C \le T_{C} \le 125^{\circ}C, Vcc = 5V \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		Vih	2.2	6.0	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ Vin ≤ Vcc	ILı	-10	10	μА	
Output Leakage Current	Outputs Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	Vон	2.4		٧	1
Output Low Voltage	IoL = 8.0mA	Vol		0.4	V	1

					MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	CE ≤ VIL, Vcc = Max., Outputs Open	lcc	130	120	110	100	95	mA	3
	$\overline{CE} \ge V_{IH}, V_{CC} = Max.,$ $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}} Hz$	Isbt1	50	45	40	40	40	mA	
Power Supply Current: Standby	CE ≥ VIH, all other inputs ≤ VIL or ≥ VIH, Vcc = Max., f = 0Hz	Іѕвт2	35	35	35	35	35	mA	
	$\overline{\text{CE}} \ge (\text{Vcc - 0.2}),  \text{Vcc = Max.},$ all other inputs $\le 0.2\text{V}$ or $\ge (\text{Vcc - 0.2V}),  \text{f = 0Hz}$	IsBC2	10	10	10	10	10	mA	

### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25^{\circ}C$ , $f = 1MHz$ ,	Cı		8	pF	4
Output Capacitance	Vcc = 5V	Co		8	pF	4



# MICHON

### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

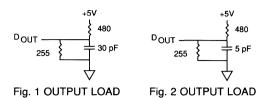
(Note 5) (-55°C  $\leq$  T $_{C}$   $\leq$  125°C, Vcc = 5V  $\pm$  10%)

DECORIDATION		-1	5	-2	:0	-2	25	-3	80	-35	5		
DESCRIPTION	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	<sup>t</sup> RC	15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		15		20		25		30		35	ns	
Chip enable access time	<sup>t</sup> ACE		15		20		25		30		35	ns	
Output hold from address change	<sup>t</sup> OH	3		3		3		3		3		ns	
Chip enable to output in low Z	t <sub>LZCE</sub>	5		5		5		5		5		ns	
Chip disable to output in high Z	tHZCE		10		15		15		20		20	ns	6,7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		15		20		25		30		35	ns	
Output enable access time	t <sub>AOE</sub>		12		15		15		20		20	ns	
Output enable to output in low Z	t <sub>LZOE</sub>	0		0		0		0		0		ns	
Output disable to output in high Z	tHZOE		10		15		15		20		20	ns	6
WRITE Cycle													
WRITE cycle time	twc	15		20		25		30		35		ns	
Chip enable to end of write	tcw	13		15		20		25		30		ns	
Address valid to end of write	<sup>t</sup> AW	15		15		20		25		30		ns	
Address set-up time	<sup>t</sup> AS	0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	0		0		0		0		0		ns	
Write pulse width	t <sub>WP</sub>	13		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		12		15		15		15		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		ns	
Write disable to output in low Z	t <sub>LZWE</sub>	0		0		0		0		0		ns	
Write enable to output in high Z	t <sub>HZWE</sub>	0	10	0	12	0	15	0	15	0	15	ns	6

**EQUIVALENT** 

### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2



### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and  $f = \frac{1}{TRC(MIN)} = \frac{1}{TWC(MIN)} = Hz$ .
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- tHZCE and tHZWE are tested with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from

- steady state voltage, allowing for actual tester RC time constant.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8.  $\overline{\text{WE}}$  is high for READ cycle.

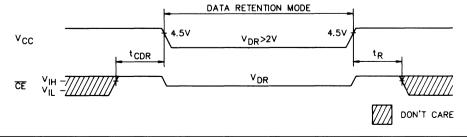
**EQUIVALENT** 

- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

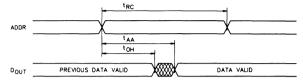
### DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2		_	٧
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V)	Vcc=2v		95	1000	μА
		Vin ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=3v		350	1500	μА
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			<sup>t</sup> RC <sup>(11)</sup>			ns

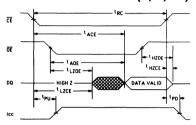
### **LOW Vcc DATA RETENTION WAVEFORM**



### **READ CYCLE NO. 1 (8, 9)**

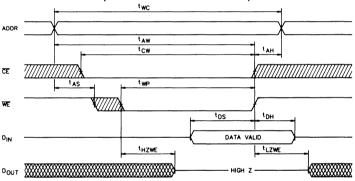


### **READ CYCLE NO. 2 (7, 8, 10)**



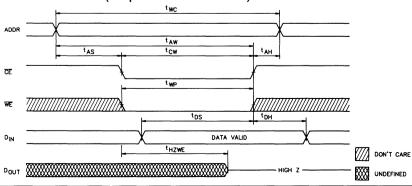
### **WRITE CYCLE NO. 1**

(Write Enable Controlled)



### **WRITE CYCLE NO. 2**

(Chip Enable Controlled)



## Comment

### Description of Requirements and Screens

## General MIL-M-38510

1. MIL-STD 883, Class B, Rev C

Establish and implement

Methods and Test **Conditions** 

a product assurance program plan and qualification test plan.

MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

2. Certification Manufacturer's QA survey 3. Traceability

4. Country of Origin (Not required for 883C)

Traceable to wafer production lot.

N/A

Approved

Self audit Computer lot history records Devices manufactured.

assembed and tested in Boise, Idaho USA.

### MIL-STD-883 Fabrication

5.	Incoming Inspections All
	Direct Materials
6	Wafer Fabrication

Wafer Fabrication 7. Assembly

MIL-STD-105D

Method 2018 SEM Monitors Class B Process Monitors

In-line

100% 100%

100% 100% 100%

100%

100%

100%

100%

100%

### MIL-STD-883, Class B, Rev. C, Method 5004 Screening

8. Intérnal Visual
9. Temperature Cycle
10. Constant Acceleration
11. Hermeticity
A. Fine Leak
B. Gross Leak
12. Initial Electricals

13. Burn-in 14. Final Electrical Post

Burn-in Test 15. Marking 16. External Visual

17. Pack/Ship

18. Quality Conformance Inspection

Method	2010,	cond.	В
Method	1010,	cond.	C
Method	2001	cond	$\mathbf{E}$

Method 2001, cond. E Method 1014, cond. A

Method 1014, cond. C Manufacturer's documented data sheet @ +125°C

Method 1015 Method 5004, Class B,

3.1.16 @ -55°C, +25°C, +125°C 5% PDA and in-line Group A per method 5005

Method 2015 Method 2009 Includes C of C, with QCI

data (attributes only) Method 5005 in-line Class B

100%

100% 100%

Groups A, B, C, D

### Quality Conformance Inspection per Method 5005 (attributes data only)

19. Group A 20. Group B 21. Group C Manufacturer's documented data sheet Package functional and construction tests

Die related

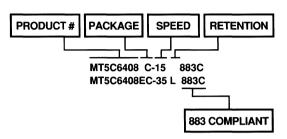
Each lot/sublot Each package type

on each lot Micro circuit group/every quarter

22. Group D Package related test

Each package type Generic every 26 weeks

### **ORDER INFORMATION**



The Micron Fast SRAM family is functionally equivalent to other manufacturer's 883 compliant devices. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

# MILITARY SRAM

# **16K x 1 SRAM**

### ADDITIONAL MILITARY SPECIFICATIONS

- SMD 84132
- IAN M38510/291
- RAD-tolerant (consult factory)

### **FEATURES**

- Battery Backup 2 volt data retention
- High speed: 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS	MARKING
Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Ceramic DIP (300 mil)	С
Ceramic LCC	EC
• Two Volt Data Retention	L

### PIN ASSIGNMENT (Top View) 20L/LCC 20L/300 DIP A0 813 813 20 12021 A13 19 A12 Α2 18 A2 A3 A4 A5 3 4 5 6 7 A12 17 A11 17 U A11 16 A10 15 A9 16 A10 Α8 13 Α5 15 A9 Α6 14 | A8 9015 Dout | 8 13 A7 를 일을 된 12 DIN WE 9 **ECC** 11 CE Vss 10 CD

### GENERAL DESCRIPTION

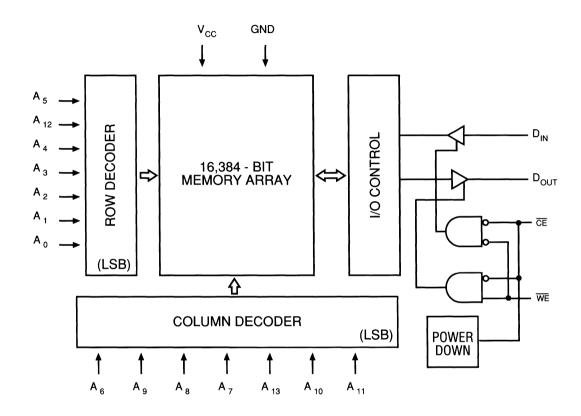
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology. All fabrication is 100% domestic.

For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ( $\overline{WE}$ ) and  $\overline{CE}$  inputs are both LOW. Reading is accomplished when  $\overline{WE}$  remains HIGH and  $\overline{CE}$  goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

### **FUNCTIONAL BLOCK DIAGRAM**



### **TRUTH TABLE**

MODE	CE	WE	DQ	POWER
STANDBY	Н	Х	HIGH Z	STANDBY
READ	L	Н	DOUT	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any input relative to Vss2.0 to +7.0V
Voltage on Vcc supply relative to Vss1.0V to +7.0V
Storage Temperature65°C to +150°C
Power Dissipation1 Watt
Short Circuit Output Current50mA
Lead Temperature (soldering, 10 seconds)+260°C
Junction Temperature+175°C

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C  $\leq$  T<sub>C</sub>  $\leq$  125°C, Vcc = 5V  $\pm$  10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		Vih	2.2	6.0	٧	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VCC	ILı	-10	10	μА	
Output Leakage Current	Output Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	Vон	2.4		٧	1
Output Low Voltage	IoL = 8.0mA	Vol		0.4	V	1

					MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	CE ≤ VIL, Vcc = Max., Output Open	lcc	130	120	110	100	95	mA	3
	$\overline{CE} \ge V_{IH}, V_{CC} = Max.,$ $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}} Hz$	Isbt1	50	45	40	40	40	mA	
Power Supply Current: Standby	CE ≥ VIH, all other inputs         ≤ VIL or ≥ VIH, Vcc = Max.,         f = 0Hz	Isвт2	35	35	35	35	35	mA	
	$\overline{\text{CE}} \ge (\text{Vcc} - 0.2),  \text{Vcc} = \text{Max.},$ all other inputs $\le 0.2\text{V}$ or $\ge (\text{Vcc} - 0.2\text{V}),  f = 0\text{Hz}$	lsBC2	10	10	10	10	10	mA	

### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz,	Cı		8	pF	4
Output Capacitance	Vcc = 5V	Co		8	pF	4

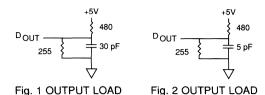
# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Note 5) (-55°C $\leq$ T $_{C}$ $\leq$ 125°C, Vcc = 5V $\pm$ 10%)

DESCRIPTION		-1	5	-2	20	-2	5	-3	0	-3	35		
DESCRIPTION	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	t <sub>RC</sub>	15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		15		20		25		30		35	ns	
Chip enable access time	t <sub>ACE</sub>		15		20		25		30		35	ns	
Output hold from address change	<sup>t</sup> OH	3		3		3		3		3		ns	
Chip enable to output in low Z	<sup>t</sup> LZCE	5		5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		10		15		15		20		20	ns	6,7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		15		20		25		30		35	ns	
WRITE Cycle													
WRITE cycle time	twc	15		20		25		30		35		ns	
Chip enable to end of write	tcw	13		15		20		25		30		ns	
Address valid to end of write	<sup>t</sup> AW	15		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		ns	
Address hold from end of write	t <sub>AH</sub>	0		0		0		0		0		ns	
Write pulse width	twp	13		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		12		15		15		15		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		ns	
Write disable to output in low Z	t <sub>LZWE</sub>	0		0		0		0		0		ns	
Write enable to output in high Z	t <sub>HZWE</sub>	0	10	0	12	0	15	0	15	0	15	ns	6

**EQUIVALENT** 

### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2



### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates. The specified value applies with the output unloaded, and  $f = \frac{1}{TRC(MIN)} = \frac{1}{TWC(MIN)} = Hz$ .
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- 6. <sup>t</sup>HZCE and <sup>t</sup>HZWE are tested with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from

- steady state voltage, allowing for actual tester RC time constant.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8. WE is high for READ cycle.

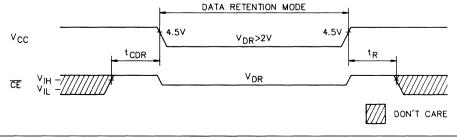
**EQUIVALENT** 

- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

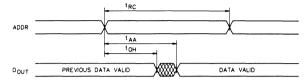
### DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
VDR	Vcc for Retention Data			2		_	٧
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V) Vin ≥ (Vcc - 0.2V)	Vcc=2v	_	95	1000	μА
		or ≤ 0.2V	Vcc=3v	_	350	1500	μА
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0			ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

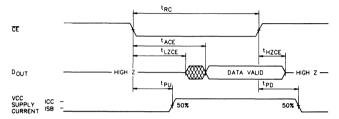
### LOW Vcc DATA RETENTION WAVEFORM



### **READ CYCLE NO. 1 (8, 9)**

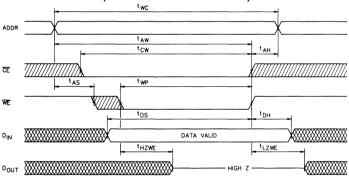


### **READ CYCLE NO. 2 (7, 8, 10)**

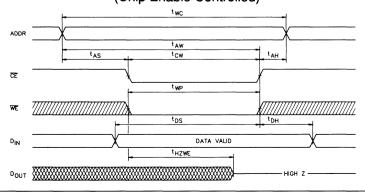


### WRITE CYCLE NO. 1

(Write Enable Controlled)



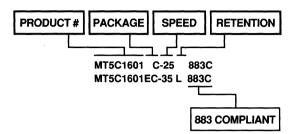
# WRITE CYCLE NO. 2 (Chip Enable Controlled)





MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW						
Description of Requirements and Screens	Methods and Test Conditions	Comment				
General MIL-M-38510						
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved				
<ol> <li>Certification</li> <li>Traceability</li> <li>Country of Origin (Not required for 883C)</li> </ol>	Manufacturer's QA survey Traceable to wafer production lot. N/A	Self audit Computer lot history records Devices manufactured, assembed and tested in Boise, Idaho USA.				
MIL-STD-883 Fabrication						
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line				
6. Wafer Fabrication	Method 2018 SEM Monitors	100%				
7. Assembly	Class B Process Monitors	100%				
MIL-STD-883, Class B, Rev. C, Me	thod 5004 Screening					
8. Internal Visual	Method 2010, cond. B	100%				
9. Temperature Cycle	Method 1010, cond. C	100%				
10. Constant Acceleration	Method 2001, cond. E	100%				
11. Hermeticity						
A. Fine Leak	Method 1014, cond. A	100%				
B. Gross Leak	Method 1014, cond. C	100%				
12. Initial Electricals	Manufacturer's documented data sheet @ +125°C	100%				
13. Burn-in	Method 1015	100%				
14. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +125°C 5% PDA and in-line Group A	100%				
15 Marilia	per method 5005	1000				
15. Marking 16. External Visual	Method 2015 Method 2009	100% 100%				
17. Pack/Ship	Includes C of C, with QCI	100%				
17. Fack/ 5htp	data (attributes only)	100%				
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D				
Quality Conformance Inspection p	per Method 5005 (attributes data only)					
19. Group A	Manufacturer's documented data sheet	Each lot/sublot				
20. Group B	Package functional and construction tests	Each package type on each lot				
21. Group C	Die related	Micro circuit group/every quarter				
22. Group D	Package related test	Each package type Generic every 26 weeks				

### **ORDER INFORMATION**



The Micron Fast SRAM family is functionally equivalent to other manufacturer's 883 compliant devices. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

# MILITARY SRAM

# **16K x 4 SRAM**

### ADDITIONAL MILITARY SPECIFICATIONS

- SMD 86859
- JAN (consult factory for reference number)
- RAD-tolerant (consult factory)

### **FEATURES**

- Battery Backup 2 volt data retention
- High speed: 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS	MARKING
Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Ceramic DIP (300 mil)	С
Ceramic LCC	EC
Two Volt Data Retention	L

### PIN ASSIGNMENT (Top View) 22L/300 DIP 22L/LCC 22 Vcc 2 22 21 Α6 21 Α7 20 Α3 19 18 **8**A Α2 19 A2 **A8** A9 Α1 Α9 18 Α1 A10 17 ΑO A11 16 DQ4 15 A10 17 ΑO DQ3 A12 A11 16 DQ4 A12 15 DQ3 5125 의 활동 인 A13 CE [ 10 DQ1 13 **ECD** Vss U 11 12 WE CE

### **GENERAL DESCRIPTION**

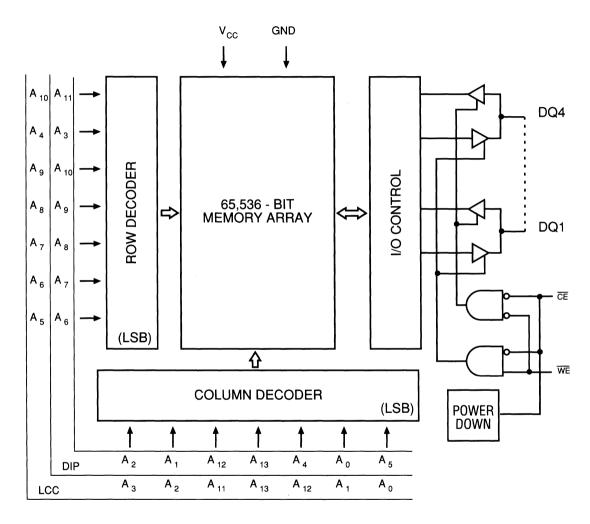
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology. All fabrication is 100% domestic.

For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ( $\overline{WE}$ ) and  $\overline{CE}$  inputs are both LOW. Reading is accomplished when  $\overline{WE}$  remains HIGH and  $\overline{CE}$  goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

### **FUNCTIONAL BLOCK DIAGRAM**



### **TRUTH TABLE**

MODE	CE	WE	DQ	POWER
STANDBY	Н	Х	HIGH Z	STANDBY
READ	L	Н	DOUT	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any input or DQ relative to Vss2.0 to +7.0V
Voltage on Vcc supply relative to Vss1.0V to +7.0V
Storage Temperature65°C to +150°C
Power Dissipation1 Watt
Short Circuit Output Current50mA
Lead Temperature (soldering, 10 seconds)+260°C
Junction Temperature+175°C

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 $(-55^{\circ}\text{C} \le \text{T}_{\text{C}} \le 125^{\circ}\text{C}, \, \text{Vcc} = 5\text{V} \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		Vih	2.2	6.0	٧	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VCC	ILı	-10	10	μА	
Output Leakage Current	Outputs Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	Vон	2.4		V	1
Output Low Voltage	loL = 8.0mA	Vol		0.4	V	1

					MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	CE ≤ V <sub>IL</sub> , Vcc = Max., Outputs Open	lcc	130	120	110	100	95	mA	3
	TRC(MIN) TCC = Max.,  f = 1/TRC(MIN) = 1/TWC(MIN)	lsbt1	50	45	40	40	40	mA	
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$ , all other inputs $\le V_{IL}$ or $\ge V_{IH}$ , $V_{CC} = Max.$ , f = OHz	lsвт2	35	35	35	35	35	mA	
	$\overline{\text{CE}} \ge (\text{Vcc} - 0.2),  \text{Vcc} = \text{Max.},$ all other inputs $\le 0.2\text{V}$ or $\ge (\text{Vcc} - 0.2\text{V}),  \text{f} = 0\text{Hz}$	lsBC2	10	10	10	10	10	mA	

### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz,	Cı		8	pF	4
Output Capacitance	Vcc = 5V	Со		8	pF	4

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Note 5) (-55°C $\leq$ T $_{C}$ $\leq$ 125°C, Vcc = 5V $\pm$ 10%)

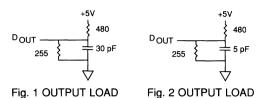
DESCRIPTION		-1	15	-2	20	-2	:5	-3	80		35		
DESCRIPTION	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle												,	
READ cycle time	t <sub>RC</sub>	15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		15		20		25		30		35	ns	
Chip enable access time	tACE		15		20		25		30		35	ns	
Output hold from address change	t <sub>OH</sub>	3		3		3		3		3		ns	
Chip enable to output in low Z	tLZCE	5		5		5		5		5		ns	
Chip disable to output in high Z	tHZCE		10		15		15		20		20	ns	6,7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		15		20		25		30		35	ns	
WRITE Cycle													
WRITE cycle time	twc	15		20		25		30		35		ns	
Chip enable to end of write	tcw	13		15		20		25		30		ns	
Address valid to end of write	t <sub>AW</sub>	15		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	0		0		0		0		0		ns	
Write pulse width	tWP	13		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		12		15		15		15		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		ns	
Write disable to output in low Z	t <sub>LZWE</sub>	0		0		0		0		0		ns	
Write enable to output in high Z	tHZWE	0	10	0	12	0	15	0	15	0	15	ns	6

**EQUIVALENT** 

# MILITARY FAST SRAN

### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2



### **NOTES**

- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and  $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}} = Hz$ .
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- tHZCE and tHZWE are tested with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from

- steady state voltage, allowing for actual tester RC time constant.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8.  $\overline{\text{WE}}$  is high for READ cycle.

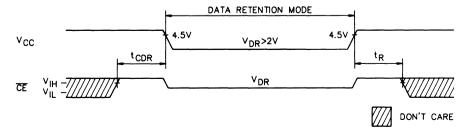
**EQUIVALENT** 

- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

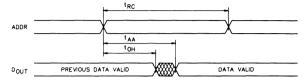
### DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2		_	٧
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V) Vin ≥ (Vcc - 0.2V)		_	95	1000	μА
		or ≤ 0.2V	Vcc=3v	_	350	1500	μΑ
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0			ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

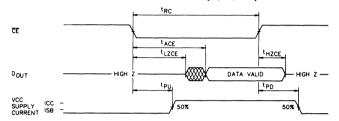
### LOW Vcc DATA RETENTION WAVEFORM



### **READ CYCLE NO. 1 (8, 9)**

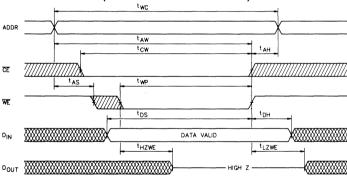


### **READ CYCLE NO. 2 (7, 8, 10)**



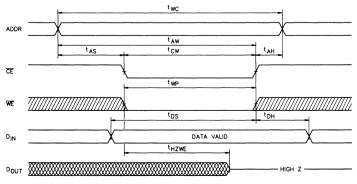
### WRITE CYCLE NO. 1

(Write Enable Controlled)



# WRITE CYCLE NO. 2

(Chip Enable Controlled)

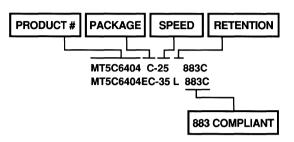


MICRON MIL	-STD 883C	PRODUCT	ASSURANCE	FLOW

Description of	Methods and Test	
Requirements and Screens	Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved.
<ol> <li>Certification</li> <li>Traceability</li> <li>Country of Origin (Not required for 883C)</li> </ol>	Manufacturer's QA survey Traceable to wafer production lot. N/A	Self audit Computer lot history records Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD-883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018 SEM Monitors	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD-883, Class B, Rev. C, Me	thod 5004 Screening	
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented	100%
	data sheet @ +125°C	
13. Burn-in	Method 1015	100%
14. Final Electrical Post	Method 5004, Class B,	100%
Burn-in Test	3.1.16 @ -55°C, +25°C, +125°C	
	5% PDA and in-line Group A	
	per method 5005	
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI	100%
	data (attributes only)	
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection p	er Method 5005 (attributes data only)	
19. Group A	Manufacturer's documented	F. d. 1. (
20. Group B	data sheet Package functional and	Each lot/sublot Each package type
ZU. CHUUD D	Lackage fullchollal allu	Cacii Dackage LVDe

19. Group A	Manufacturer's documented	
	data sheet	Each lot/sublot
20. Group B	Package functional and	Each package type
•	construction tests	on each lot
21. Group C	Die related	Micro circuit group/every quarter
•		0 1 1 1
22. Group D	Package related test	Each package type
1	8	Generic every 26 weeks
		<i>j</i> == ··· =

### **ORDER INFORMATION**



The Micron Fast SRAM family is functionally equivalent to other manufacturer's 883 compliant devices. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

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# MILITARY **SRAM**

# **32K x 8 SRAM**

### ADDITIONAL MILITARY SPECIFICATIONS

- SMD 88662
- · JAN (consult factory for reference number
- RAD-tolerant (consult factory)

### **FEATURES**

- Battery Backup 2 volt data retention
- High speed: 25, 30, 35 and 45ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS	MARKING
Timing	
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
Packages	
Ceramic DIP (300 mil)	C
Ceramic DIP (600 mil)	CW
Ceramic LCC (28 pin)	EC
Ceramic LCC (32 pin)	ECW
Two Volt Data Retention	L

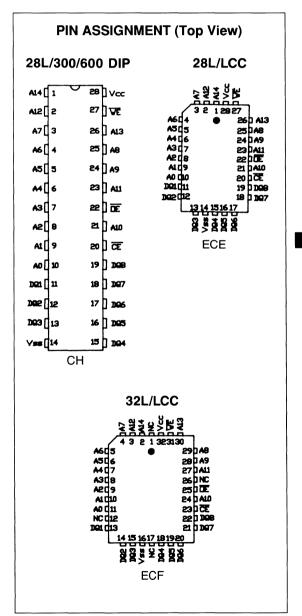
### GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

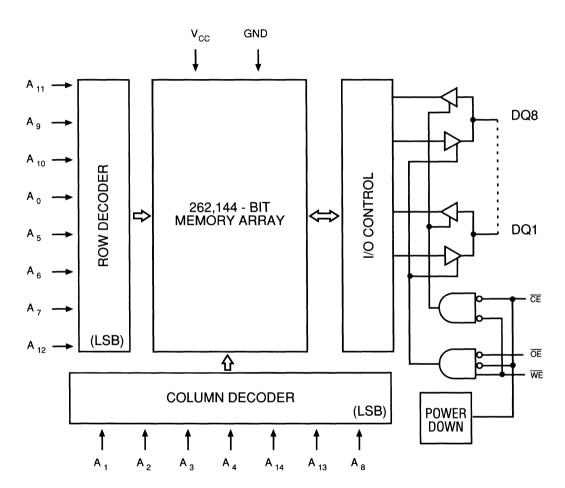
For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.



### **FUNCTIONAL BLOCK DIAGRAM**



### **TRUTH TABLE**

MODE	OE	CE	WE	DQ	POWER
STANDBY	Х	Н	Х	HIGH Z	STANDBY
READ	L	L	Н	DOUT	ACTIVE
READ	Н	L	Н	HIGH Z	ACTIVE
WRITE	Х	L	L	DIN	ACTIVE

### **ABSOLUTE MAXIMUM RATINGS\***

 \*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

 $(\text{-}55^{\circ}\text{C} \leq \text{T}_{\text{C}} \leq \text{125}^{\circ}\text{C}, \, \text{Vcc} = 5.0\text{V} \pm \text{10\%})$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	ligh (Logic 1) Voltage		2.2	6.0	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	٧	1, 2
Power Supply Current: Operating	CE ≤ VIL, Vcc = Max., Outputs Open	lcc		100	mA	3
	$\overline{CE} \ge V_{IH}, V_{CC} = Max.,$ $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}} Hz$	Іѕвт1		40	mA	
Power Supply Current: Standby	CE ≥ VIH, all other inputs       ≤ VIL or ≥ VIH, Vcc = Max.,       f = 0Hz	Isвт2		20	mA	
	$\overline{CE} \geq (Vcc - 0.2V), \ Vcc = Max., \\ all \ other \ inputs \leq 0.2V \\ or \geq (Vcc - 0.2V), \ f = 0Hz$	IsBC2		10	mA	
Input Leakage Current	0V ≤ Vin ≤ Vcc	ILı	-5	5	μА	
Output Leakage Current	Outputs Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	Vон	2.4		V	1
Output Low Voltage	IoL = 8.0mA	<b>V</b> OL		0.4	V	1

### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz,	Cı		8	pF	4
Output Capacitance	Vcc = 5V	Со		8	pF	4

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Note 5) (-55°C $\leq$ T $_{C}$ $\leq$ 125°C, Vcc = 5V $\pm$ 10%)

DECORIDATION		-2	25	-3	30	-3	35	-4	15		
DESCRIPTION	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	<sup>t</sup> RC	25		30		35		45		ns	
Address access time	<sup>t</sup> AA		25		30		35		45	ns	
Chip enable access time	t <sub>ACE</sub>		25		30		35		45	ns	
Output hold from address change	tон	5		5		5		5		ns	
Chip enable to output in low Z	t <sub>LZCE</sub>	5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		15		20		20		20	ns	6, 7
Chip enable to power up time	<sup>t</sup> PU	0		0		0		0		ns	
Chip disable to power down time	<sup>t</sup> PD		25		30		35		45	ns	
Output Enable Access Time	<sup>t</sup> AOE		15		20		20		20	ns	
Output Enable to output in low Z	t <sub>LZOE</sub>	0		0		0		0		ns	
Output disable to out put in high Z	<sup>t</sup> HZOE		15		20		20		20	ns	
WRITE Cycle											
WRITE cycle time	twc	25		30		35		45		ns	
Chip enable to end of write	tcw	20		25		30		40		ns	
Address Valid to end of write	<sup>t</sup> AW	20		25		30		40		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	2		2		2		2		ns	
Write pulse width	t <sub>WP</sub>	20		25		25		30		ns	
Data set-up time	t <sub>DS</sub>	16		18		20		20		ns	
Data hold time	<sup>t</sup> DH	2		2		2		2		ns	
Write disable to output in low Z	t <sub>LZWE</sub>	0		0		0		0		ns	
Write enable to output in high Z	tHZWE	0	15	О	15	0	15	0	20	ns	6

# MILITARY FAST SRAM

### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2

# POUT 480 480 30 pF

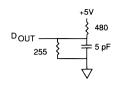


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

### **NOTES**

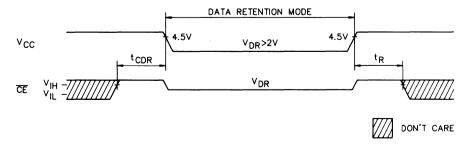
- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs  $unloaded, and f = \frac{1}{TRC(MIN)} = \frac{1}{TWC(MIN)} Hz.$
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- 6. <sup>t</sup>HZCE and <sup>t</sup>HZWE are specified with CL = 5pF as

- in Fig. 2. Transition is measured  $\pm$  500mV from steady state voltage, allowing for actual tester RC time constant.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8. WE is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

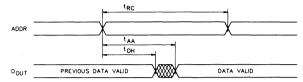
### DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2		٧	
ICCDR	Data Retention Current	CE ≥ (Vcc - 0.2V) Vin ≥ (Vcc - 0.2V)	Vcc=2v		95	1000	μА
		$or \le 0.2V$	Vcc=3v		350	1500	μА
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

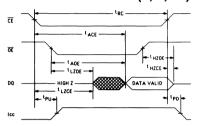
### LOW Vcc DATA RETENTION WAVEFORM



### **READ CYCLE NO. 1 (8, 9)**

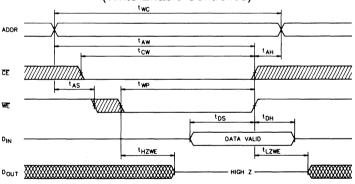


### **READ CYCLE NO. 2 (7, 8, 10)**

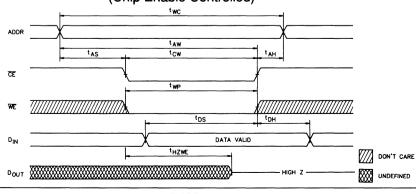


### WRITE CYCLE NO. 1

(Write Enable Controlled)



# WRITE CYCLE NO. 2 (Chip Enable Controlled)



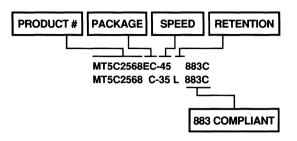
### MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens General MIL-M-38510	Methods and Test Conditions	Comment
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved
<ol> <li>Certification</li> <li>Traceability</li> <li>Country of Origin (Not required for 883C)</li> </ol>	Manufacturer's QA survey Traceable to wafer production lot. N/A	Self audit Computer lot history records Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD 883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018 SEM Monitors	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD 883, Class B, Rev. C, Meth	nod 5004 Screening	
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented	100%
	data sheet @ +125°C	
13. Burn-in	Method 1015	100%
14. Final Electrical Post	Method 5004, Class B,	100%
Burn-in Test	3.1.16 @ -55°C, +25°C, +125°C	
	5% PDA and in-line Group A	
v.	per method 5005	
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI	100%
10.0 11. 6 (	data (attributes only)	
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection pe	er Method 5005 (attributes data only)	
19. Group A	Manufacturer's documented data sheet	Each lot/sublot

19. Group A	Manufacturer's documented	
	data sheet	Each lot/sublot
20. Group B	Package functional and	Each package type
	construction tests	on each lot
21. Group C	Die related	Micro circuit group/every quarter

22. Group D Package related test Each package type
Generic every 26 weeks

### ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's 883 compliant devices. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

# MILITARY FAST SRAM

# MILITARY SRAM

# **64K x 1 SRAM**

### ADDITIONAL MILITARY SPECIFICATIONS

- SMD 86105
- JAN M38510/292
- RAD-tolerance (consult factory)

### **FEATURES**

- Battery Backup 2 volt data retention
- High speed: 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- All inputs and output are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS	MARKING
Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Ceramic DIP (300 mil)	C
Ceramic LCC	EC
Two Volt Data Retention	L

### PIN ASSIGNMENT (Top View) 22L/300 DIP 22L/LCC 22 Vcc 21 22 12 21 A15 טטווט A2 🛛 3 20 A14 3456789 A2 A3 A4 A5 A6 A7 19 A13 Α.3 19 A13 17 A11 18 A12 16 A10 15 A9 A5 17 A11 14 A8 16 A6 A10 15 Α9 5 1 2 5 14 Dout A8 WE 13 D DIN **ECD** ∨ss [ 12 CE

### **GENERAL DESCRIPTION**

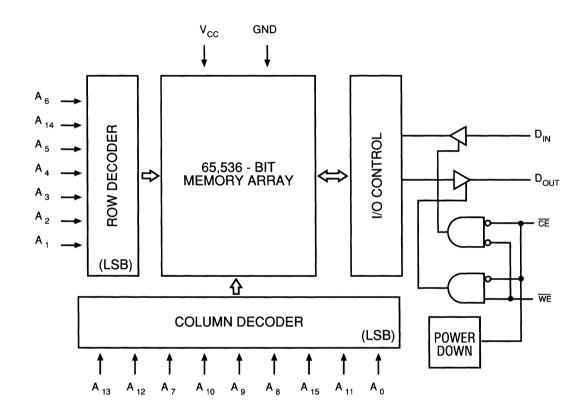
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology. All fabrication is 100% domestic.

For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable  $(\overline{WE})$  and  $\overline{CE}$  inputs are both LOW. Reading is accomplished when  $\overline{WE}$  remains HIGH and  $\overline{CE}$  goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

### **FUNCTIONAL BLOCK DIAGRAM**



### **TRUTH TABLE**

MODE	CE	WE	DQ	POWER
STANDBY	Н	Х	HIGH Z	STANDBY
READ	L	Н	DOUT	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any input relative to Vss2.0 to +7.0V
Voltage on Vcc supply relative to Vss1.0V to +7.0V
Storage Temperature65°C to +150°C
Power Dissipation1 Watt
Short Circuit Output Current50mA
Lead Temperature (soldering, 10 seconds)+260°C
Junction Temperature+175°C

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(-55°C  $\leq$  T<sub>C</sub>  $\leq$  125°C, Vcc = 5V  $\pm$  10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		ViH	2.2	6.0	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	٧	1, 2
Input Leakage Current	0V ≤ VIN ≤ VCC	ILı	-10	10	μА	
Output Leakage Current	Output Disabled, 0V ≤ Vout ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	Vон	2.4		V	1
Output Low Voltage	IoL = 8.0mA	Vol		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	CE ≤ VIL, Vcc = Max., Output Open	lcc	130	120	110	100	95	mA	3
	$\overline{CE} \ge V_{IH}, V_{CC} = Max.,$ $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}} Hz$	lsbt1	50	45	40	40	40	mA	
Power Supply Current: Standby	$\overline{\text{CE}}$ ≥ Vih, all other inputs ≤ Vil or ≥ Vih, Vcc = Max., f = 0Hz	ISBT2	35	35	35	35	35	mA	
	$\overline{\text{CE}} \ge (\text{Vcc} - 0.2),  \text{Vcc} = \text{Max.},$ all other inputs $\le 0.2\text{V}$ or $\ge (\text{Vcc} - 0.2\text{V}),  \text{f} = 0\text{Hz}$	lsBC2	10	10	10	10	10	mA	

### **CAPACITANCE**

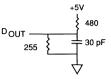
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz,	Cı		8	pF	4
Output Capacitance	Vcc = 5V	Co		8	pF	4

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Note 5) (-55°C $\leq$ T $_{C}$ $\leq$ 125°C, Vcc = 5V $\pm$ 10%)

DESCRIPTION		-1	15	-2	<u>:</u> 0	-25		-30		-3	35		
DESCRIPTION -		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	<sup>t</sup> RC	15		20		25		30		35		ns	
Address access time	<sup>t</sup> AA		15		20		25		30		35	ns	
Chip enable access time	tACE		15		20		25		30		35	ns	
Output hold from address change	t <sub>OH</sub>	3		3		3		3		3		ns	
Chip enable to output in low Z	tLZCE	5		5		5		5		5		ns	
Chip disable to output in high Z	tHZCE		10		15		15		20		20	ns	6,7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		15		20		25		30		35	ns	
WRITE Cycle													
WRITE cycle time	twc	15		20		25		30		35		ns	
Chip enable to end of write	tcw	13		15		20		25		30		ns	
Address valid to end of write	<sup>t</sup> AW	15		15		20		25		30		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	0		0		0		0		0		ns	
Write pulse width	t <sub>WP</sub>	13		15		20		25		25		ns	
Data set-up time	t <sub>DS</sub>	10		12		15		15		15		ns	
Data hold time	t <sub>DH</sub>	0		0		0		0		0		ns	
Write disable to output in low Z	t <sub>LZWE</sub>	0		0		0		0		0		ns	
Write enable to output in high Z	<sup>t</sup> HZWE	0	10	0	12	0	15	0	15	0	15	ns	6

### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	s5ns
Input timing reference	levels1.5V
Output reference levels	s1.5V
Output load	See figures 1 and 2



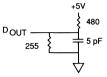


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

### **NOTES**

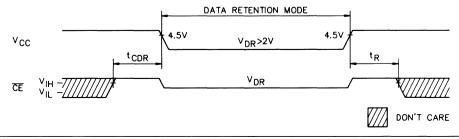
- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates. The specified value applies with the output unloaded, and  $f = \frac{1}{TRC(MIN)} = \frac{1}{TWC(MIN)} = Hz$ .
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- tHZCE and tHZWE are tested with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from

- steady state voltage, allowing for actual tester RC time constant.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8.  $\overline{\text{WE}}$  is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

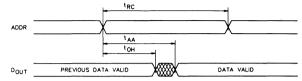
### DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2		_	٧
ICCDR	Data Retention Current	CE ≥ (Vcc - 0.2V) Vin ≥ (Vcc - 0.2V)	Vcc=2v	_	95	1000	μΑ
		or ≤ 0.2V	Vcc=3v	_	350	1500	μΑ
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

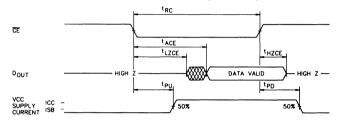
### **LOW Vcc DATA RETENTION WAVEFORM**



### **READ CYCLE NO. 1 (8, 9)**

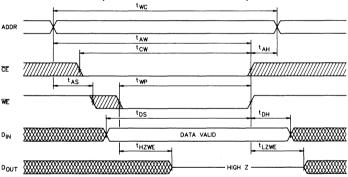


### **READ CYCLE NO. 2 (7, 8, 10)**



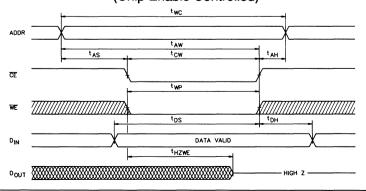
### **WRITE CYCLE NO. 1**

(Write Enable Controlled)



## WRITE CYCLE NO. 2

(Chip Enable Controlled)



Each package type

Each package type Generic every 26 weeks

Micro circuit group/every quarter

on each lot

20. Group B

21. Group C

22. Group D

### MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved
<ol> <li>Certification</li> <li>Traceability</li> <li>Country of Origin (Not required for 883C)</li> </ol>	Manufacturer's QA survey Traceable to wafer production lot. N/A	Self audit Computer lot history records Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD-883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018 SEM Monitors	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD-883, Class B, Rev. C, Me	thod 5004 Screening	
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity	37.1.14044	100%
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented	100%
	data sheet @ +125°C	
13. Burn-in	Method 1015	100%
14. Final Electrical Post	Method 5004, Class B,	100%
Burn-in Test	3.1.16 @ -55°C, +25°C, +125°C	
	5% PDA and in-line Group A	
	per method 5005	
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI	100%
18. Quality Conformance Inspection	data (attributes only) Method 5005 in-line Class B	Groups A, B, C, D
Ouality Conformance Inspection r	per Method 5005 (attributes data only)	
19. Group A	Manufacturer's documented	
1	data sheet	Each lot/sublot
20 Croup P	Da alsa as functional and	Each madeans trong

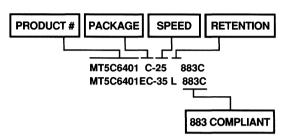
Package functional and

construction tests

Package related test

Die related

### **ORDER INFORMATION**



The Micron Fast SRAM family is functionally equivalent to other manufacturer's 883 compliant devices. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

# MILITARY SRAM

# **64K x 4 SRAM**

### ADDITIONAL MILITARY SPECIFICATIONS

- SMD 88681
- JAN (consult factory for reference number)
- RAD-tolerant (consult factory)

### **FEATURES**

- Battery backup 2 volt data retention
- High speed: 25, 30, 35 and 45ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS	MARKING
Timing	
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Ceramic DIP (300 mil)	C
Ceramic LCC	EC
Two Volt Data Retention	L

### PIN ASSIGNMENT (Top View) 24L/300 DIP 28L/LCC **48588** A٥ 24 Vcc 3 1 28 27 Α1 2 23 A15 שטווטע A2 A3 A4 A5 A6 A7 22 A14 A2 25 A14 24 A13 23 A12 22 A11 21 A10 5 6 7 21 Α3 A13 20 A12 Α4 A8 20 DQ4 10 19 [ Α5 A10 18 DQ2 18 | 46 17 DQ4 Α7 5 4 5 9 7 16 DQ3 Α8 5 % 5 F & C 15 DQ2 Α9 **ECE** CE Vss 12 13 CF

### **GENERAL DESCRIPTION**

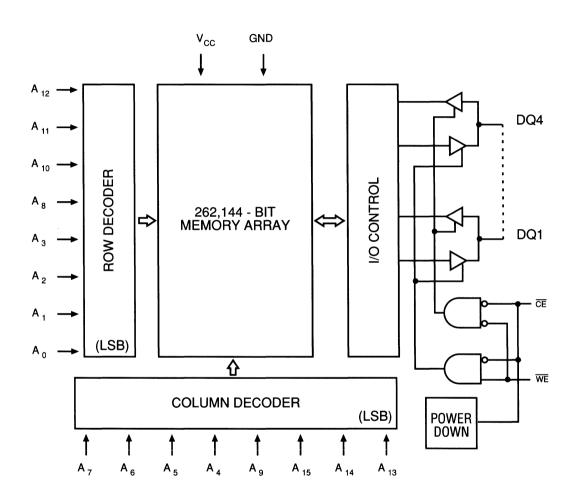
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ( $\overline{WE}$ ) and  $\overline{CE}$  inputs are both LOW. Reading is accomplished when  $\overline{WE}$  remains HIGH and  $\overline{CE}$  goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

### **FUNCTIONAL BLOCK DIAGRAM**



### **TRUTH TABLE**

MODE	CE	WE	DQ	POWER
STANDBY	н	Х	HIGH Z	STANDBY
READ	L	н	DOUT	ACTIVE
WRITE	L	L	DIN	ACTIVE

### **ABSOLUTE MAXIMUM RATINGS\***

 \*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 $(-55^{\circ}C \le T_{C} \le 125^{\circ}C, Vcc = 5.0V \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		ViH	2.2	6.0	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	٧	1, 2
Power Supply Current: Operating	CE ≤ V <sub>IL</sub> , Vcc = Max., Outputs Open	lcc		100	mA	3
	$\overline{CE} \ge V_{IH}, V_{CC} = Max.,$ $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}} Hz$	Іѕвт1		40	mA	
Power Supply Current: Standby	CE ≥ VIH, all other inputs       ≤ VIL or ≥ VIH, Vcc = Max.,       f = 0Hz	Isвт2	,	20	mA	
	$\overline{CE} \geq (Vcc - 0.2V), \ Vcc = Max.,$ all other inputs $\leq 0.2V$ or $\geq (Vcc - 0.2V), \ f = 0Hz$	IsBC2		10	mA	
Input Leakage Current	0V ≤ VIN ≤ VCC	ILı	-5	5	μА	
Output Leakage Current	Outputs Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	<b>V</b> OH	2.4		V	1
Output Low Voltage	IoL = 8.0mA	<b>V</b> OL		0.4	V	1

### CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz,	Cı		8	pF	4
Output Capacitance	Vcc = 5V	Co		8	pF	4

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Note 5) (-55°C $\leq$ T $_{C}$ $\leq$ 125°C, Vcc = 5V $\pm$ 10%)

DESCRIPTION		-2	25	-3	30	-35		-45			
DESCRIPTION	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	t <sub>RC</sub>	25		30		35		45		ns	
Address access time	<sup>t</sup> AA		25		30		35		45	ns	
Chip enable access time	t <sub>ACE</sub>		25		30		35		45	ns	
Output hold from address change	t <sub>OH</sub>	5		5		5		5		ns	
Chip enable to output in low Z	tLZCE	5		5		5		5		ns	
Chip disable to output in high Z	tHZCE		15		20		20		20	ns	6, 7
Chip enable to power up time	<sup>t</sup> PU	0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		25		30		35		45	ns	
WRITE Cycle											
WRITE cycle time	twc	25		30		35		45		ns	
Chip enable to end of write	tcw	20		25		30		40		ns	
Address Valid to end of write	t <sub>AW</sub>	20		25		30		40		ns	
Address set-up time	<sup>t</sup> AS	0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	2		2		2		2		ns	
Write pulse width	tWP	20		25		25		30		ns	
Data set-up time	t <sub>DS</sub>	16		18		20		20		ns	
Data hold time	<sup>t</sup> DH	2		2		2		2		ns	
Write disable to output in low Z	t <sub>LZWE</sub>	0		0		0		0		ns	
Write enable to output in high Z	tHZWE	0	15	0	15	0	15	0	20	ns	6

### **AC TEST CONDITIONS**

Input pulse levelsVss to 3	3.0V
Input rise and fall times	5ns
Intput timing reference level	1.5V
Output reference level	1.5V
Output load See figures 1 a	nd 2

# DOUT 480 DOUT 255 POUT 255

Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

+5V

480

5 pF

### **NOTES**

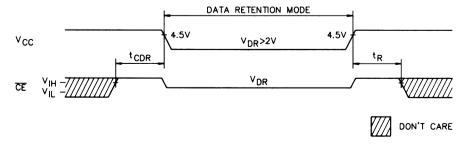
- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and  $f = \frac{1}{TRC(MIN)} = \frac{1}{TWC(MIN)} Hz$ .
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- 6.  ${}^{t}HZCE$  and  ${}^{t}HZWE$  are specified with CL = 5pF as

- in Fig. 2. Transition is measured ± 500mV from steady state voltage, allowing for actual tester RC time constant.
- 7. At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8. WE is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- 10. Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

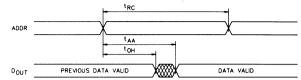
### DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2		٧	
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V) Vin ≥ (Vcc - 0.2V)	Vcc=2v	_	95	1000	μΑ
		or ≤ 0.2V	Vcc=3v		350	1500	μ <b>A</b>
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time	•		0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

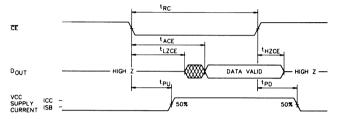
### **LOW Vcc DATA RETENTION WAVEFORM**



### **READ CYCLE NO. 1 (8, 9)**

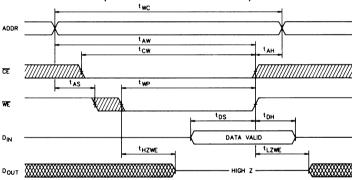


### **READ CYCLE NO. 2 (7, 8, 10)**



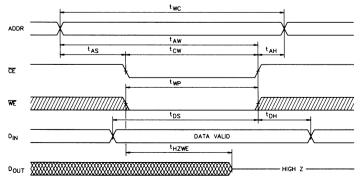
### **WRITE CYCLE NO. 1**

(Write Enable Controlled)



### WRITE CYCLE NO. 2

(Chip Enable Controlled)





DON'T CARE

21. Group C

22. Group D

### MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

MIGHOR	I MIL-OTD 0000 I HODGOT AGGOTA	ANOL I LOW
Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved.
<ol> <li>Certification</li> <li>Traceability</li> <li>Country of Origin (Not required for 883C)</li> </ol>	Manufacturer's QA survey Traceable to wafer production lot. $N/A$	Self audit Computer lot history records Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD 883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
<ul><li>6. Wafer Fabrication</li><li>7. Assembly</li></ul>	Method 2018 SEM Monitors Class B Process Monitors	100% 100%
MIL-STD 883, Class B, Rev. C, Meth	od 5004 Screening	
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration 11. Hermeticity	Method 2001, cond. E	100%
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented data sheet @ +125°C	100%
13. Burn-in	Method 1015	100%
14. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +125°C 5% PDA and in-line Group A per method 5005	100%
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection pe	r Method 5005 (attributes data only)	
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and	Each package type

on each lot

Each package type Generic every 26 weeks

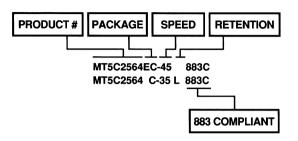
Micro circuit group/every quarter

construction tests

Package related test

Die related

### ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's 883 compliant devices. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

# MILITARY FAST SRAM

# MILITARY SRAM

# 256K x 1 SRAM

### ADDITIONAL MILITARY SPECIFICATIONS

- SMD 88725
- JAN (consult factory for reference number)
- RAD-tolerant (consult factory)

### **FEATURES**

- Battery backup 2 volt data retention
- High speed: 25, 30, 35 and 45ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with CE option
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS	MARKING
Timing	
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Ceramic DIP (300 mil)	С
Ceramic LCC	EC
• Two Volt Data Retention	L

### PIN ASSIGNMENT (Top View) 24L/300 DIP 28L/LCC 24 Vcc AO [ 24 28 27 A1 1 2 23 A17 NC A3 A4 A5 A2 3 22 A16 25 24 23 22 21 A16 A3 21 A15 A6 A7 20 A14 A4 | A12 Α8 10 20 19 A13 A11 Α5 Dout NC 19 A10 18 A12 A6 [ 17 A11 Α7 54597 A8 9 16 A10 B S B S S Dout 10 15 A9 **ECE** WE 11 14 Din Vss 12 13 CE CF

### GENERAL DESCRIPTION

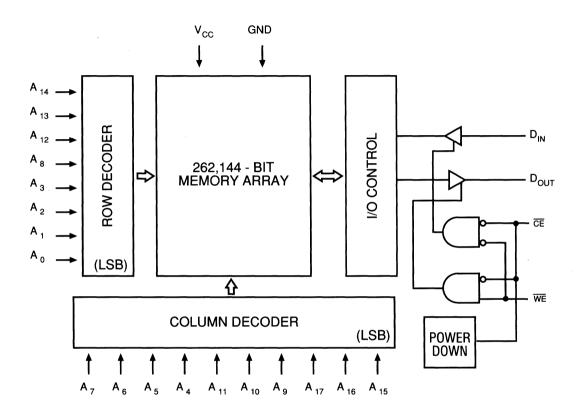
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ( $\overline{WE}$ ) and  $\overline{CE}$  inputs are both LOW. Reading is accomplished when  $\overline{WE}$  remains HIGH and  $\overline{CE}$  goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

### **FUNCTIONAL BLOCK DIAGRAM**



### **TRUTH TABLE**

MODE	CE	WE	OUTPUT	POWER
STANDBY	Н	Х	HIGH Z	STANDBY
READ	L	Н	DOUT	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any input relative to Vss	2.0V to +7.0V
Voltage on Vcc supply relative to Vss	1.0V to +7.0V
Voltage applied to Dout	1.0V to 6.0V
Storage Temperature	-65°C to +150°C
Power Dissipation	1 Watt
Short Circuit Output Current	50mA
Lead Temperature (soldering, 10 seconds)	)+260°C
Juction Temperature	+175°C

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C  $\leq$  T<sub>C</sub>  $\leq$  125°C, Vcc = 5.0V  $\pm$  10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		Vıн	2.2	6.0	٧	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	٧	1, 2
Power Supply Current: Operating	CE ≤ VIL, Vcc = Max., Output Open	lcc		100	mA	3
	$\overline{CE} \ge V_{IH}, \ V_{CC} = Max.,$ $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}} Hz$	IsbT1		40	mA	
Power Supply Current: Standby	$\overline{\text{CE}}$ ≥ ViH, all other inputs ≤ ViL or ≥ ViH, Vcc = Max., f = 0Hz			20	mA	
	$\overline{CE} \geq (Vcc - 0.2V), \ Vcc = Max.,$ all other inputs $\leq 0.2V$ or $\geq (Vcc - 0.2V), \ f = 0Hz$	IsBc2		10	mA	
Input Leakage Current	0V ≤ Vin ≤ Vcc	ILı	-5	5	μА	
Output Leakage Current	Output Disabled, 0V ≤ Vouт ≤ Vcc	ILo	-10	10	μА	
Output High Voltage	loн = -4.0mA	<b>V</b> oн	2.4		٧	1
Output Low Voltage	IoL = 8.0mA	<b>V</b> OL		0.4	V	1

### **CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz,	Cı		8	pF	4
Output Capacitance	Vcc = 5V	Co		8	pF	4

# ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Note 5) (-55°C $\leq$ T $_{C}$ $\leq$ 125°C, Vcc = 5V $\pm$ 10%)

DESCRIPTION		-2	25	-3	30	-3	35	-4	5		
DESCRIPTION	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	<sup>t</sup> RC	25		30		35		45		ns	
Address access time	<sup>t</sup> AA		25		30		35		45	ns	
Chip enable access time	<sup>t</sup> ACE		25		30		35		45	ns	
Output hold from address change	t <sub>OH</sub>	5		5		5		5		ns	
Chip enable to output in low Z	tLZCE	5		5		5		5		ns	
Chip disable to output in high Z	<sup>t</sup> HZCE		15		20		20		20	ns	6, 7
Chip enable to power up time	t <sub>PU</sub>	0		0		0		0		ns	
Chip disable to power down time	t <sub>PD</sub>		25		30		35		45	ns	
WRITE Cycle											
WRITE cycle time	twc	25		30		35		45		ns	
Chip enable to end of write	tcw	20		25		30		40		ns	
Address Valid to end of write	t <sub>AW</sub>	20		25		30		40		ns	
Address set-up time	t <sub>AS</sub>	0		0		0		0		ns	
Address hold from end of write	t <sub>AH</sub>	2		2		2		2		ns	
Write pulse width	t <sub>WP</sub>	20		25		25		30		ns	
Data set-up time	t <sub>DS</sub>	16		18		20		20		ns	
Data hold time	t <sub>DH</sub>	2		2		2		2		ns	
Write disable to output in low Z	tLZWE	0		0		0		0		ns	
Write enable to output in high Z	<sup>t</sup> HZWE	0	15	0	15	0	15	0	20	ns	6

### **AC TEST CONDITIONS**

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2

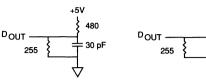


Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

480

5 pF

### **NOTES**

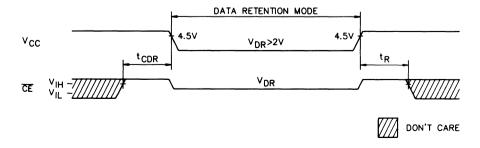
- 1. All voltages referenced to Vss (GND).
- 2. -3.0V for pulse width < 20ns.
- 3. Icc is dependent on output loading and cycle rates. The specified value applies with the output unloaded, and  $f = \frac{1}{TRC(MIN)} = \frac{1}{TWC(MIN)}$  Hz.
- 4. This parameter is sampled.
- 5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- 6. <sup>t</sup>HZCE and <sup>t</sup>HZWE are tested with CL = 5pF as

- in Fig. 2. Transition is measured  $\pm$  500mV from steady state voltage, allowing for actual tester RC time constant.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE.
- 8. WE is high for READ cycle.
- 9. Device is continuously selected. All Chip Enables held in their active state.
- Address valid prior to or coincident with latest occurring Chip Enable.
- 11. <sup>t</sup>RC = Read Cycle Time. (Page 4)

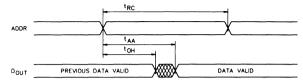
### DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITI	ONS	MIN	TYP	MAX	UNIT
<b>V</b> DR	Vcc for Retention Data			2	_	V	
ICCDR	Data Retention Current	<u>CE</u> ≥ (Vcc - 0.2V) Vin ≥ (Vcc - 0.2V)	Vcc=2v		95	1000	μА
		or ≤ 0.2V	Vcc=3v		350	1500	μΑ
tCDR <sup>(4)</sup>	Chip Deselect to Data Retention Time			0		_	ns
<sup>t</sup> R <sup>(4)</sup>	Operation Recovery Time			tRC <sup>(11)</sup>			ns

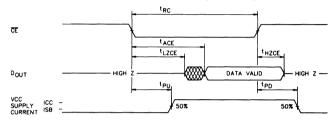
### LOW Vcc DATA RETENTION WAVEFORM



### **READ CYCLE NO. 1 (8, 9)**

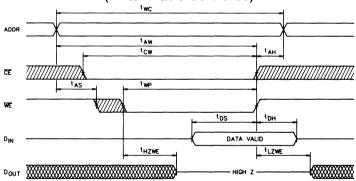


### **READ CYCLE NO. 2 (7, 8, 10)**



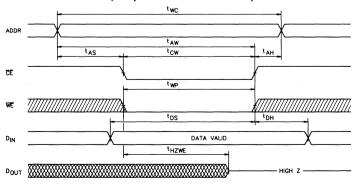
### **WRITE CYCLE NO. 1**

(Write Enable Controlled)



### WRITE CYCLE NO. 2

(Chip Enable Controlled)



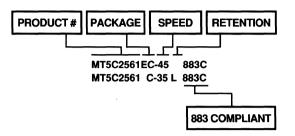
### MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved
<ol> <li>Certification</li> <li>Traceability</li> <li>Country of Origin (Not required for 883C)</li> </ol>	Manufacturer's QA survey Traceable to wafer production lot. N/A	Self audit Computer lot history records Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD 883 Fabrication		
<ol><li>Incoming Inspections All Direct Materials</li></ol>	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018 SEM Monitors	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD 883, Class B, Rev. C, Met	thod 5004 Screening	
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented	100%
12 B	data sheet @ +125°C	1000
13. Burn-in	Method 1015	100%
14. Final Electrical Post	Method 5004, Class B,	100%
Burn-in Test	3.1.16 @ -55°C, +25°C, +125°C 5% PDA and in-line Group A	
	per method 5005	
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI	100%
are a design of the party of th	data (attributes only)	10070
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection r	per Method 5005 (attributes data only)	
19. Group A	Manufacturer's documented	
-	data sheet	Each lot/sublot

19. Group A	Manufacturer's documented			
-	data sheet	Each lot/sublot		
20. Group B	Package functional and construction tests	Each package type on each lot		
21. Group C	Die related	Micro circuit group/every quarter		

22. Group D Package related test Each package type
Generic every 26 weeks

### ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's 883 compliant devices. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

# MICRON

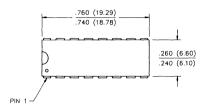
# TABLE OF CONTENTS

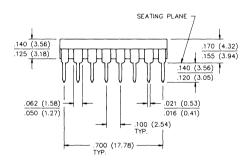
DYNAMIC RAMS	1
DYNAMIC RAM MODULES.	. 2
MULTIPORT DYNAMIC RAMS (VRAMS)	3
	4
CACHE DATA RAMS	5
	6
VILLEN PRODUCTS	7
PACKAGE INFORMATION	8
SALES INFORMATION CONTRACTOR OF THE PROPERTY O	. g

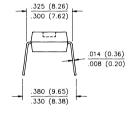
PACKAGE TYPE	PIN CO	J <b>NT</b>	PAGE
PLASTIC DIP	16		8-3
	18		8-4
	20		8-5
	22		8-6
	24		8-7
	28		8-8
CERAMIC DIP	16		8-9
	18		
	20		
	22		8-12
	24		8-13
	28		8-14
PLASTIC ZIP	16		8-15
	20		8-15
	24		8-16
	28		8-16
PLCC	18		8-17
PLASTIC SOJ	20		8-18
•	24		8-18
	28		8-19
CERAMIC LCC	18		8-20
	20		8-21
	22		8-21
	28		8-22
	32		8-22
FLAT PACK	16		8-23
	18		8-23
	20		8-24
MODULE SIP	22		8-25
	24		
	30		8-26
MODULE SIMM	30		8-28
	72		

	· · · · · · · · · · · · · · · · · · ·	
4		

### 16-PIN PLASTIC DIP PA

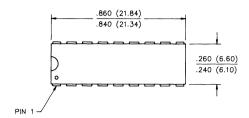


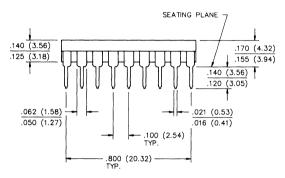


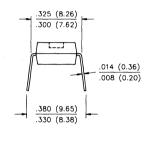


All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

### 18-PIN PLASTIC DIP PB

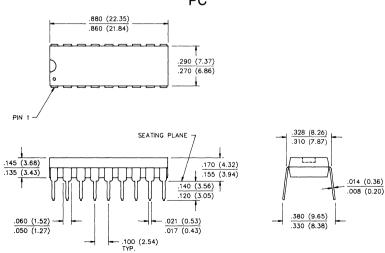






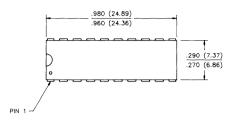
All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

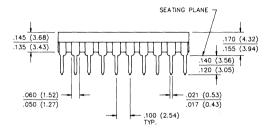
### 18-PIN PLASTIC DIP PC



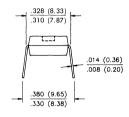
All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

# 20-PIN PLASTIC DIP

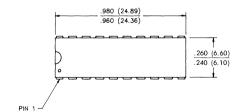


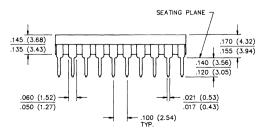


All dimensions in inches (millimeters)  $\frac{Max}{Min}$ .

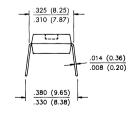


### 20-PIN PLASTIC DIP PE

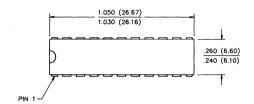


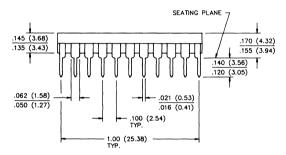


All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

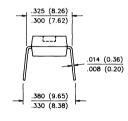


# 22-PIN PLASTIC DIP

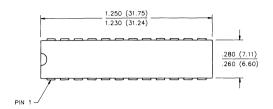


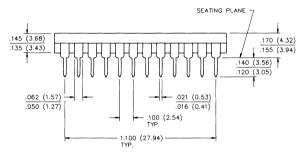


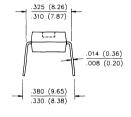




### 24-PIN PLASTIC DIP PG

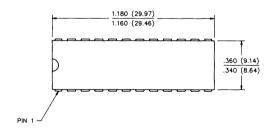


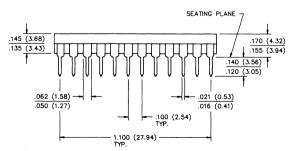


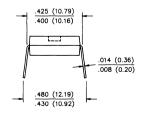


All dimensions in inches (millimeters)  $\frac{Max}{Min}$ 

# 24-PIN PLASTIC DIP

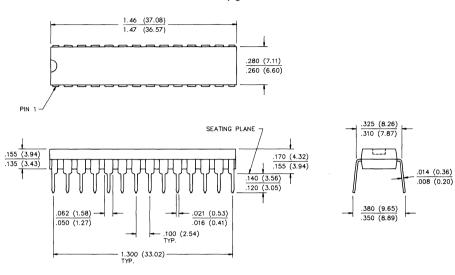






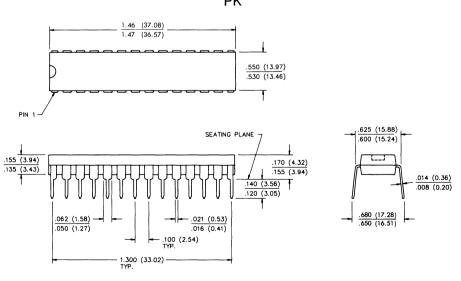
All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ .

# 28-PIN PLASTIC DIP

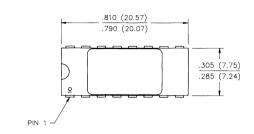


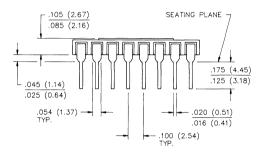
### All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$

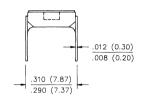
# 28-PIN PLASTIC DIP



### 16-PIN CERAMIC DIP CA

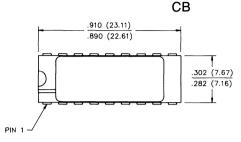


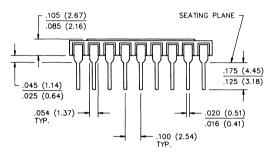


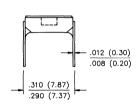


All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

### 18-PIN CERAMIC DIP



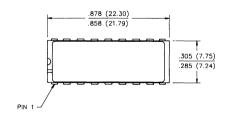


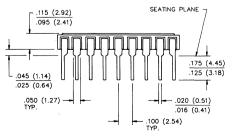


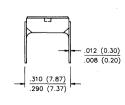
All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

### **18-PIN CERAMIC DIP**

CC

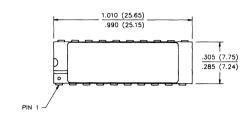


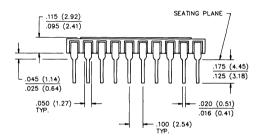


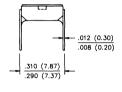


All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

# 20-PIN CERAMIC DIP

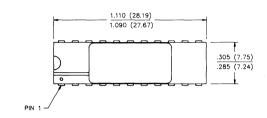


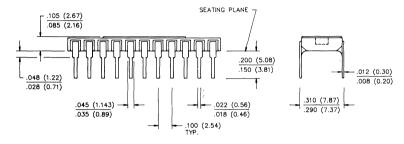




All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

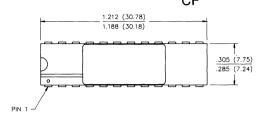
### 22-PIN CERAMIC DIP CE

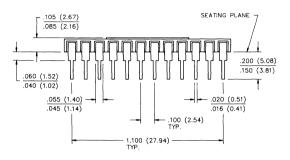


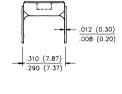


All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

### 24-PIN CERAMIC DIP CF



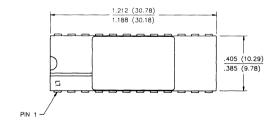


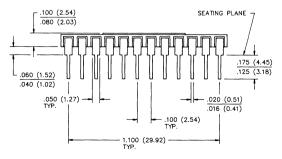


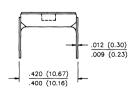
All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

### 24-PIN CERAMIC DIP

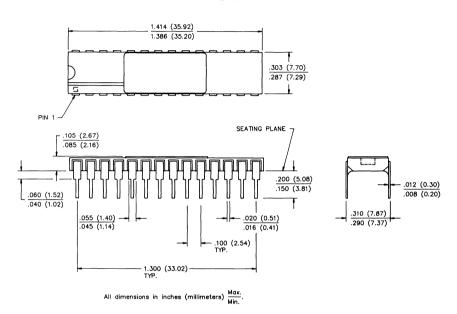
CG





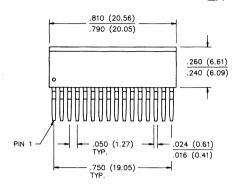


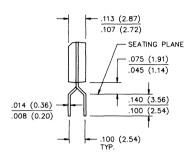
### 28-PIN CERAMIC DIP CH

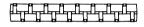


# PACKAGE INFORMATION

### 16-PIN PLASTIC ZIP ZA

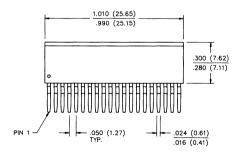


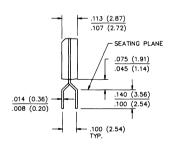


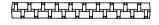


All dimensions in inches (millimeters)  $\frac{Max.}{Min.}$ 

### 20-PIN PLASTIC ZIP ZB







.113 (2.87) .107 (2.72)

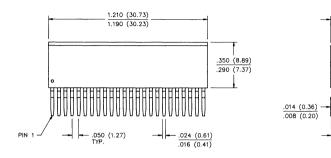
.100 (2.54) TYP.

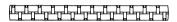
SEATING PLANE

.075 (1.91) .045 (1.14)

100 (2.54)

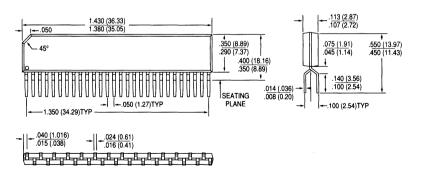
### 24-PIN PLASTIC ZIP ZC



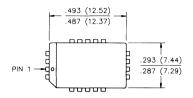


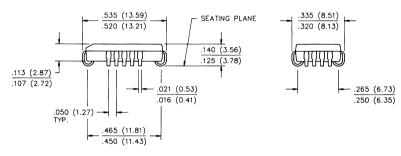
All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

### 28-PIN PLASTIC ZIP ZD



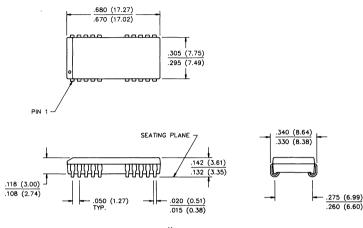
### 18-PIN PLCC EJA





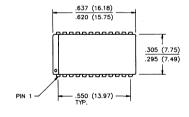
All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

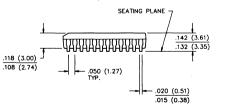
### 20-PIN PLASTIC SOJ DJA



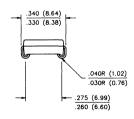
All dimensions in inches (millimeters)  $\frac{Max}{Min}$ 

### 24-PIN PLASTIC SOJ DJB

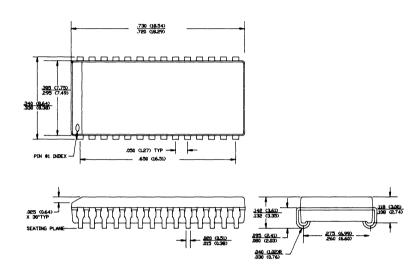




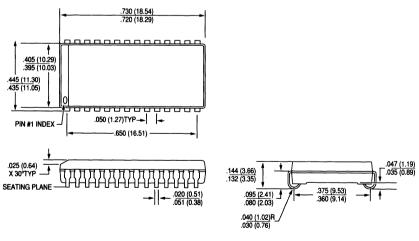
All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 



### 28-PIN PLASTIC SOJ DJC

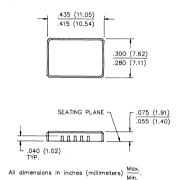


### 28-PIN PLASTIC SOJ DJD

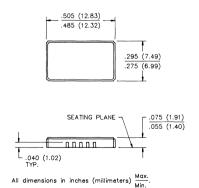


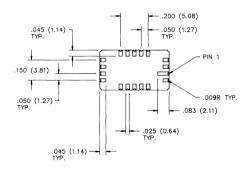
All dimensions in inches (millimeters)

### 18-PIN CERAMIC LCC ECA

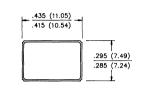


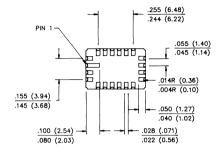
### 18-PIN CERAMIC LCC ECB

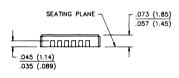




### 20-PIN CERAMIC LCC ECC





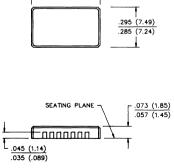


All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

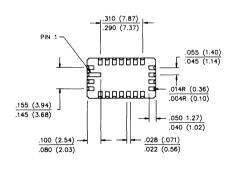
.500 (12.70)

480 (12.19)

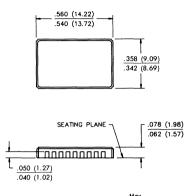
### 22-PIN CERAMIC LCC ECD



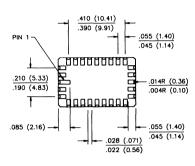




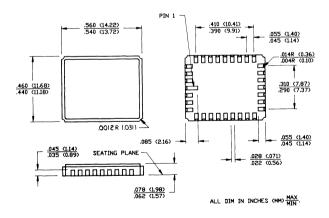
### 28-PIN CERAMIC LCC ECE



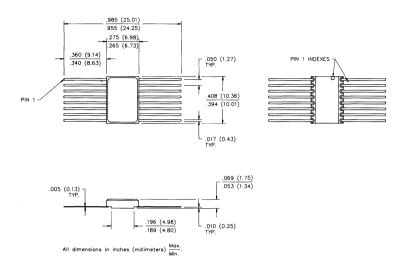
All dimensions in inches (millimeters)  $\frac{Max}{Min}$ .



### 32-PIN CERAMIC LCC ECF



### **16-PIN FLAT PACK** FA



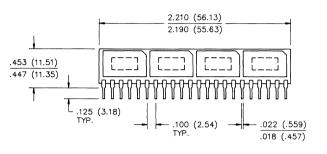
### 18-PIN FLAT PACK

**TBD** 

### **20-PIN FLAT PACK**

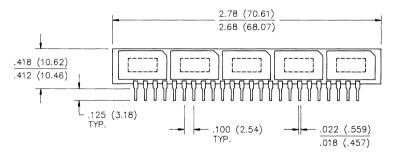
TBD

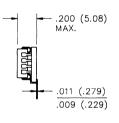
### 22-PIN MODULE SIP MA



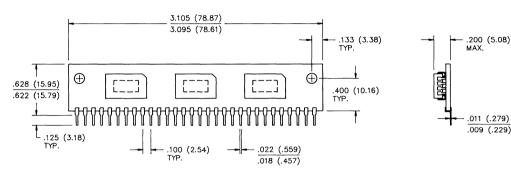
All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

### 24-PIN MODULE SIP MB



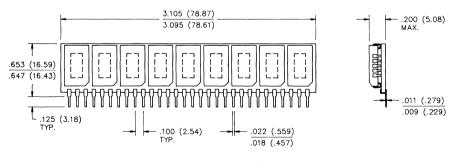


### 30-PIN MODULE SIP MC

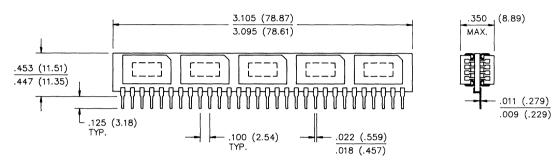


All dimensions in inches (millimeters)  $\frac{Max.}{Min.}$ 

### 30-PIN MODULE SIP

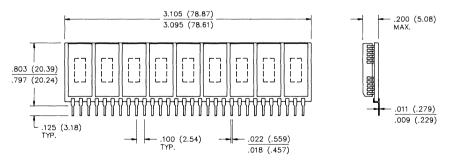


### 30-PIN MODULE SIP ME

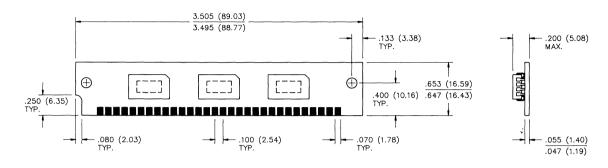


All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

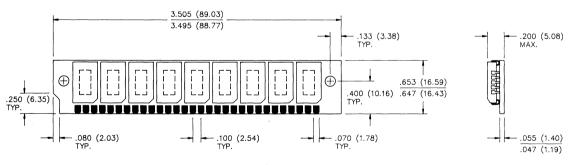
### 30-PIN MODULE SIP MG



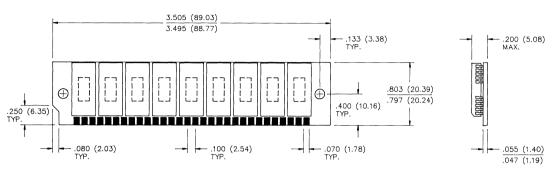
### 30-PIN MODULE SIMM MH



### 30-PIN MODULE SIMM MI

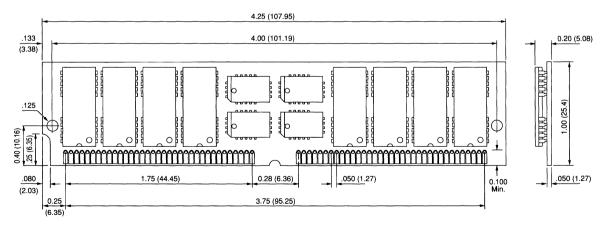


### 30-PIN MODULE SIMM MJ



All dimensions in inches (millimeters)  $\frac{\text{Max.}}{\text{Min.}}$ 

### 72-PIN MODULE SIMM MK



Notes: All dimensions are in inches (millimeters). Tolerances are to be determined.



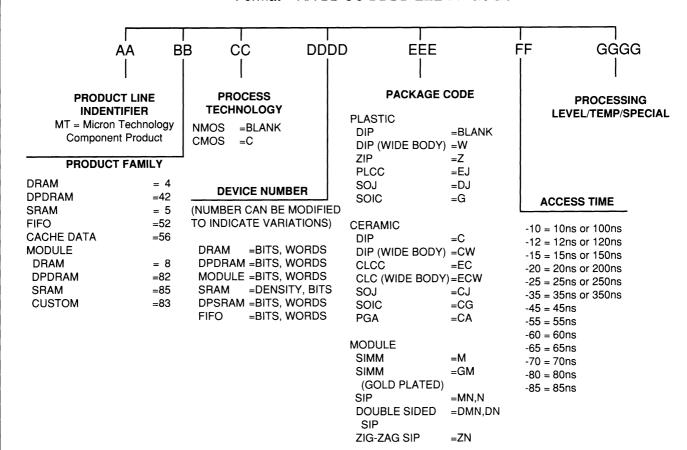
### **SECTION GUIDE**

SALES INFORMATION	9
PACKAGE INFORMATION	
1000 1000 1000 1000 1000 1000 1000 100	
FIFO MEMORIES ************************************	Ê
CACHE DATA RAMS (14/2/2/2/2/2/2/2/2/2/2/2/2/2/2/2/2/2/2/2	5
STATIC PARTS SAXESTOCKS CONSISTENCY SERVER S	4
MULTIPORT DYNAMIC RAMS (VRAMS)	3
DYNAMIC RAM MODULES	2
DVNAMIC FAMS	



### **Micron Component Group Product Numbering**

Format = AA BB CC DDDD EEE-FF GGGG



<b>V</b>		

### **ALABAMA**

### Representative

Electronic Sales Incorporated 303 Williams Avenue Suite 422 Huntsville, AL 35801 Phone - 205-533-1735 TWX - 810-726-2107 FAX - 205-534-4404

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Hall-Mark Electronics Corporation #07 4900 Bradford Drive Huntsville, AL 35807 Phone - 205-837-8700 TWX - 810-726-2187

Pioneer Technology 4825 University Square Huntsville, AL 35816 Phone - 205-837-9300 TWX - 810-726-2197 FAX - 205-837-9358

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### Representative

Quatra Electronic Sales Incorporated 4645 South Lakeshore Drive Tempe, AZ 85282 Phone 602-820-7050 FAX 602-820-7054

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### Representative

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Anthem Electronics Incorporated 1040 E. Brokaw Road San Jose, CA 95131 Phone - 408-295-4200 FAX - 408-282-1542

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Wyle Laboratories 124 Maryland Street El Segundo, CA 90245 Phone - 213-322-8100

Wyle Laboratories 3000 Bowers Avenue Santa Clara, CA 95051 Phone - 408-727-2500 TWX - 910-338-0296 FAX - 408-727-5896

Wyle Laboratories 17872 Cowan Avenue Irvine, CA 92714 Phone - 714-863-9953 Telex - 714-371-9599 FAX - 714-863-0473

Wyle Laboratories 11151 Sun Center Drive Rancho Cordova, CA 95670 Phone - 916-638-5282 TWX - 713719279 Telex - 3103719279 FAX - 916-638-1491

Wyle Laboratories 9625 Chesapeake Drive San Diego, CA 92123 Phone - 619-565-9171 Telex - 3719592

Wyle Laboratories 26677 W. Agoura Road Calabasas, CA 91302 Phone - 818-880-9000 Telex - 3103720232

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Clark-Hurman Associates 37 George Street North Suite 404 Brampton, Ontario L6X1RS Canada Phone - 416-453-1118 Telex - 06988501 FAX 416-453-5609

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### Representative

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### Representative

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Pioneer Electronics 112 Main Street Norwalk, CT 06851 Phone - 203-853-1515 TWX - 710-468-3373 FAX - 203-838-9901

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### Distributor

Pioneer Technologies Incorporated 261 Gebralta Road Horsham, PA 19044 Phone - 215-674-4000 TWX - 510-665-6778 FAX - 215-674-3107

### DISTRICT OF COLUMBIA

### Representative

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### Distributor

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### Representatives

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Delmac Sales Incorporated 1170 Woodlawn Street Clearwater, FL 33516 Phone - 813-447-5192 TWX 510-100-5606 FAX - 813-447-2622

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