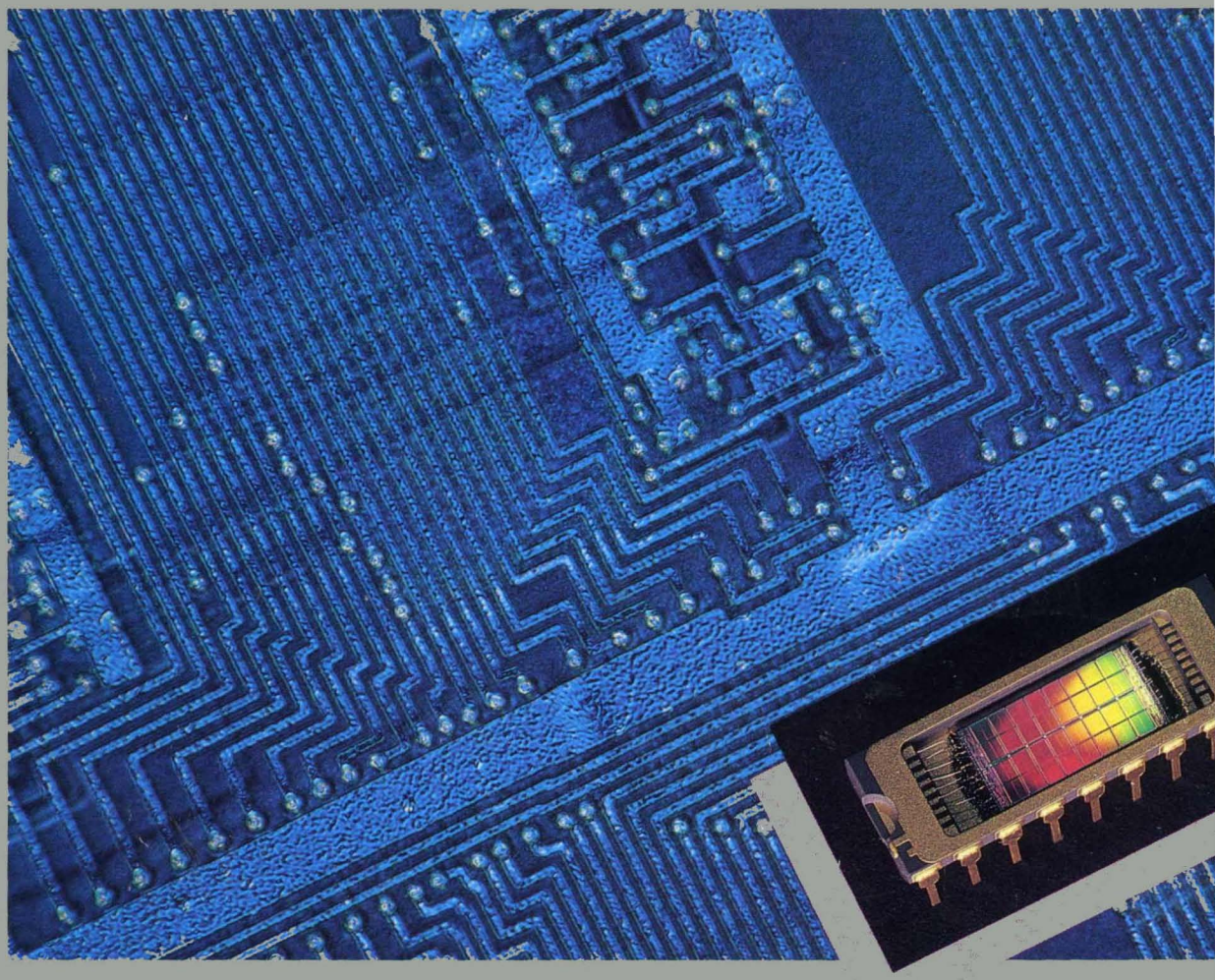
MOS DATA BOOK



MICRON
TECHNOLOGY, INC.

MICRON TECHNOLOGY, INC.

MOS DATA BOOK

1988

MICRON

SECTION GUIDE

MICRON

MOS DATA BOOK

2805 East Columbia Road
Boise, Idaho 83706
Telephone: (208) 386-3900
TWX - (910)-970-5973
FAX - (208)343-2536

12/88

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The MOS Data Book has been organized into nine sections and includes complete detailed specifications on our growing, high performance CMOS and NMOS product line.

Sections 1 through 7 cover individual product families. Each section contains a product selection guide followed by data sheets. Three different types of data sheets are used: Advance Information, which contains initial descriptions of products still under development; Preliminary Information, which contains initial device characterization limits which are subject to change upon full characterization of production devices; and Final Information, which contains minimum and maximum limits specified over the complete power supply and temperature range for production devices.

Section 8 contains detailed mechanical data on each package used by Micron.

Section 9 contains sales information, with a list of sales representatives and distributors by geographical location for the North American Continent, Europe and Asia.

Additional or updated information on any Micron product is available from:

MICRON TECHNOLOGY, INC.
Marketing Department
2805 East Columbia Road
Boise, Idaho 83706
Telephone: (208) 386-3900
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DYNAMIC RAMS

DYNAMIC RAM MODULES

MUTIPORT DYNAMIC RAMS (VIDEO RAMS)

STATIC RAMS

OE ..... With Output Enable
SI/O ..... Separate Data Inputs and Outputs
OT ..... Outputs Track Inputs During Write
HZ ..... High Impedince Outputs During Write

CACHE DATA STATIC RAMS

FIFO MEMORIES (FIRST-IN FIRST-OUT)

E ..... With Expansion Logic
MB ..... With Mailbox Register Logic
VF ..... With Variable Flag Logic

MILITARY PRODUCTS

MILITARY PRODUCTS (Continued)

M ..... MIL-STD 883
SMD ..... DESC Standardized Military Drawing
JAN ..... QPL 1 Listing
R+ ..... Rad-tolerant (available mid 1989)
VHSIC ..... Very High Speed Integrated Circuit (available 4th Quarter 1989)

PACKAGE INFORMATION

SALES INFORMATION

NUMERICAL INDEX

NUMERICAL INDEX (Continued)

NUMERICAL INDEX (Continued)

DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package and Number of Pins Process							Process	Page
				Standby	Active	PDIP	PLCC	ZIP	SOJ	CDIP	CLCC	Flat Pack		
64K x 1	Page Mode	MT4264	100,120,150,200	15mw	75mw	16	-	-	-	16	18	16	NMOS	1-3
64K x 4	Page Mode	MT4067	80,100,120,150	15mw	150mw	18	18	20	-	18	18	16	NMOS	1-13
256K x 1	Page Mode	MT1259	80,100,120,150	15mw	150mw	16	18	16	-	16	18	16	NMOS	1-23
256K x 4	Fast Page Mode	MT4C4256	80,100,120,150	5mw	175mw	20	-	20	20	20	-	20	CMOS	1-33
256K x 4	Static Column	MT4C4258	80,100,120,150	5mw	175mw	20	-	20	20	20	-	20	CMOS	1-45
1 Meg x 1	Fast Page Mode	MT4C1024	80,100,120,150	5mw	175mw	18	-	20	20	18	-	18	CMOS	1-57
1 Meg x 1	Nibble Mode	MT4C1025	80,100,120,150	5mw	175mw	18	-	20	20	18	-	18	CMOS	1-69
1 Meg x 1	Static Column	MT4C1026	80,100,120,150	5mw	175mw	18	-	20	20	18	-	18	CMOS	1-81
1 Meg x 4	Fast Page Mode	MT4C4001	80,100,120	5mw	175mw	20	-	-	20	20	-	-	CMOS	1-93
1 Meg x 4	Static Column	MT4C4003	80,100,120	5mw	175mw	20	-	-	20	20	-	-	CMOS	1-105
4 Meg x 1	Fast Page Mode	MT4C1004	80,100,120	5mw	175mw	18	-	-	20	18	-	-	CMOS	1-117
4 Meg x 1	Nibble Mode	MT4C1005	80,100,120	5mw	175mw	18	-	-	20	18	-	-	CMOS	1-129
4 Meg x 1	Static Column	MT4C1006	80,100,120	5mw	175mw	18	-	-	20	18	-	-	CMOS	1-141

DRAM

64K x 1 DRAM

PAGE MODE

FEATURES

- Industry standard pin-out, funtions, timing
- Single +5V ±10% power supply
- Low power, 15mW standby, 75mW active, typical
- Common I/O using EARLY-WRITE
- DOUT held indefinitely by $\overline{CAS}$
- 256 cycle refresh in 4ms
- Fully compatible with MT1259 (256K)
- Optional Page Mode

OPTIONS MARKING

- Timing

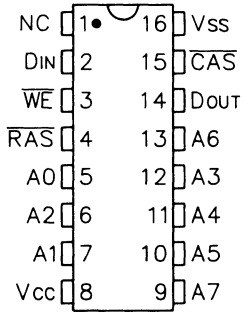
100ns access	-10
120ns access	-12
150ns access	-15
200ns access	-20

- Packages:

Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

MT4264 16 Pin DIP



PA, CA

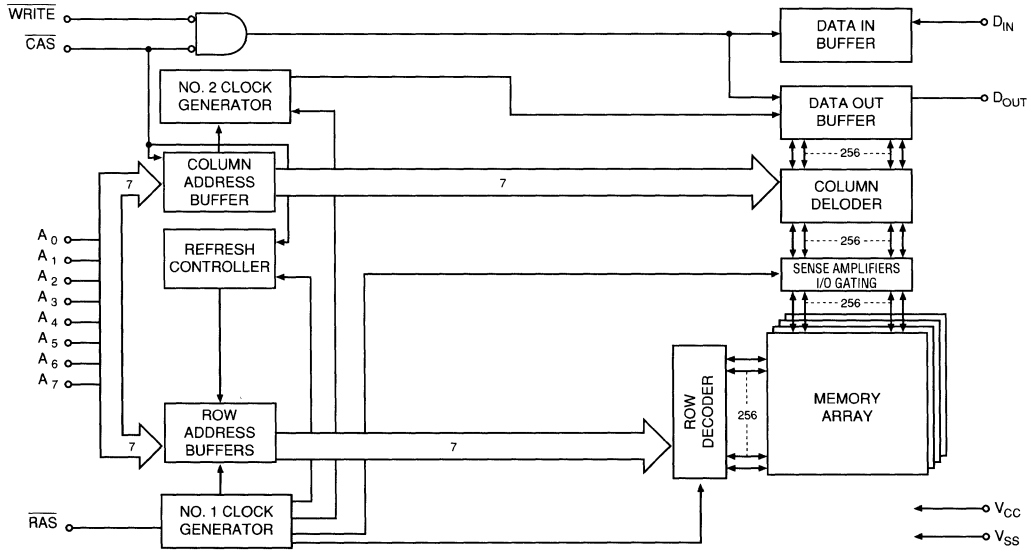
GENERAL DESCRIPTION

The MT4264 is a randomly accessed solid-state memory containing 65,536 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 16 address bits which are entered 8 bits (A0-A7) at a time. $\overline{RAS}$ is used to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only or Hidden refresh) so that all 256 combinations of $\overline{RAS}$ addresses (A0-A7) are executed at least every 4ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°) (V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}		4	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ Cycling)	I_{CC2}		30	mA	2
$\overline{RAS}$ ONLY REFRESH CURRENT ($\overline{CAS}$ = V_{IH})	I_{CC3}		20	mA	2
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling)	I_{CC4}		30	mA	2
INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_7), D_{IN}	C_{I1}		5	pF	18
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		8	pF	18
Output Capacitance D_{OUT}	C_O		8	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

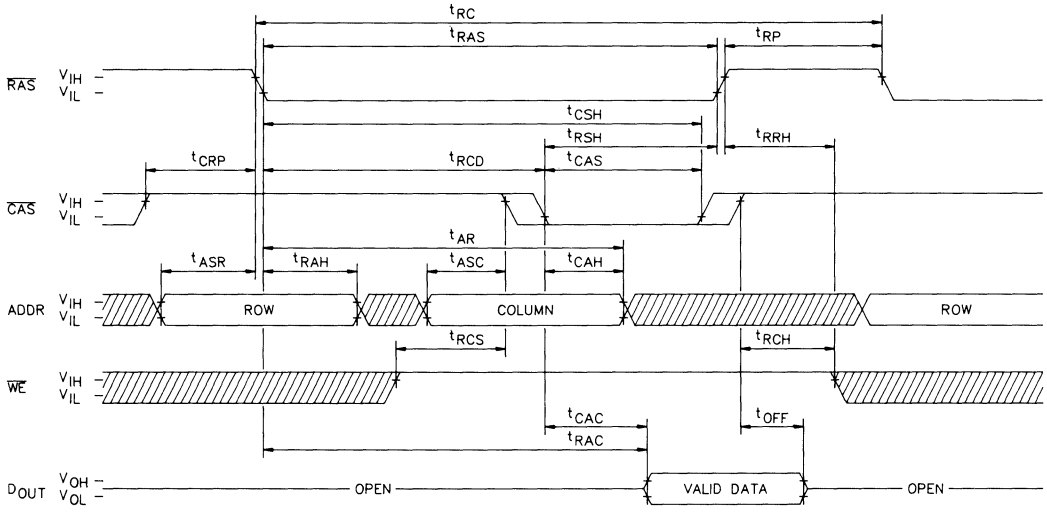
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-10		-12		-15		-20			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	195		230		260		330		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	220		255		295		370		ns	
PAGE-MODE cycle time	^tPC	90		100		120		170		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		100		120		150		200	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		50		60		75		120	ns	7, 9
RAS pulse width	^tRAS	100	10,000	120	10,000	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	50		60		75		100		ns	
$\overline{RAS}$ precharge time	^tRP	80	20,000	90	20,000	100	20,000	120	20,000	ns	
$\overline{CAS}$ pulse width	^tCAS	50	10,000	60	10,000	75	10,000	120	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		200		ns	
$\overline{CAS}$ precharge time	^tCPN	25		25		30		35		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	30		30		35		40		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	25	50	25	60	25	75	30	80	ns	13
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		20		25		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	20		20		25		50		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	70		80		100		130		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	30	0	30	0	35	0	40	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	35		40		45		60		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	85		100		120		140		ns	
WRITE command pulse width	^tWP	35		40		45		50		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		40		45		55		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		40		45		55		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	35		40		45		55		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	85		100		120		135		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	40		50		60		100		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	90		110		135		180		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	

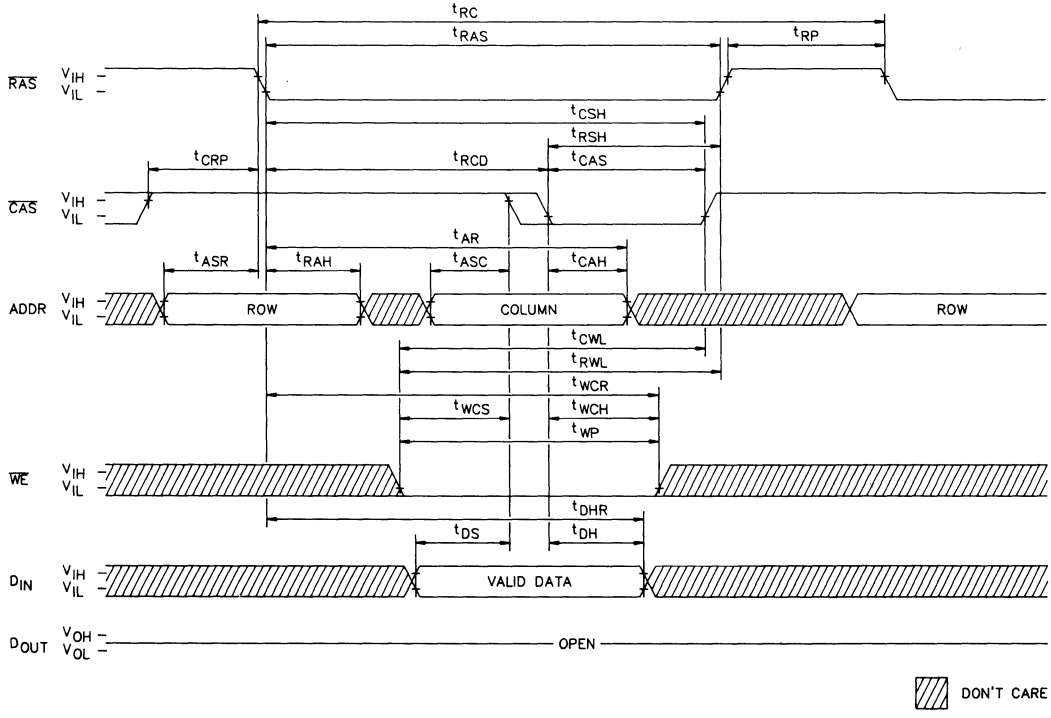
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (max).
   pulsed high for ^tCPN.
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
16. ^tWCS, ^tRWD and ^tCWD are restrictive operating parameters in late READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min) the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \geq ^tCWD$ (min) and $^tRWD \geq ^tRWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
19. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be

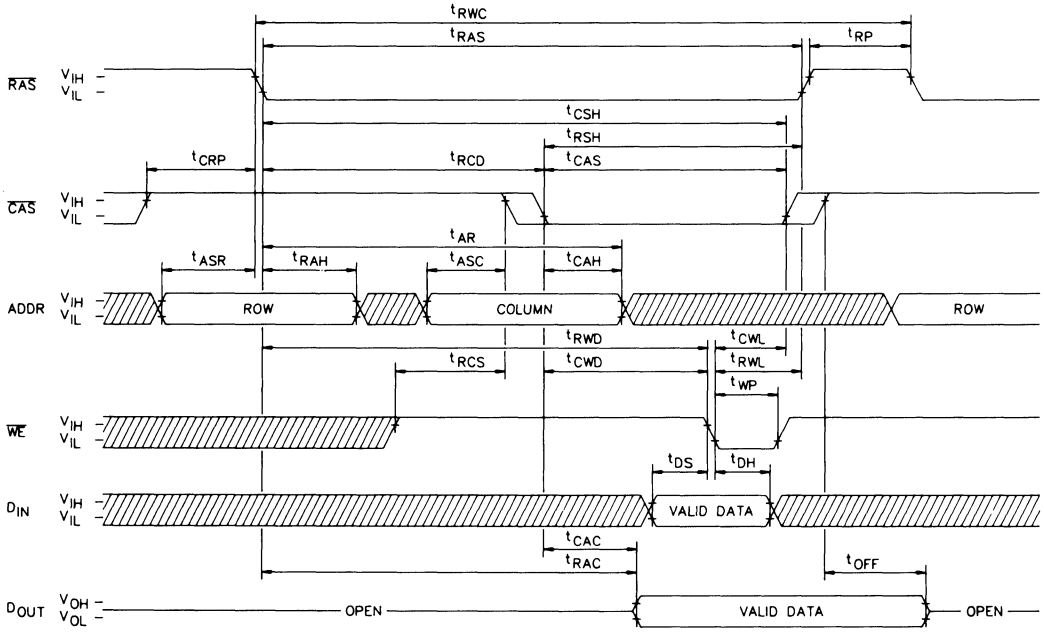
READ CYCLE



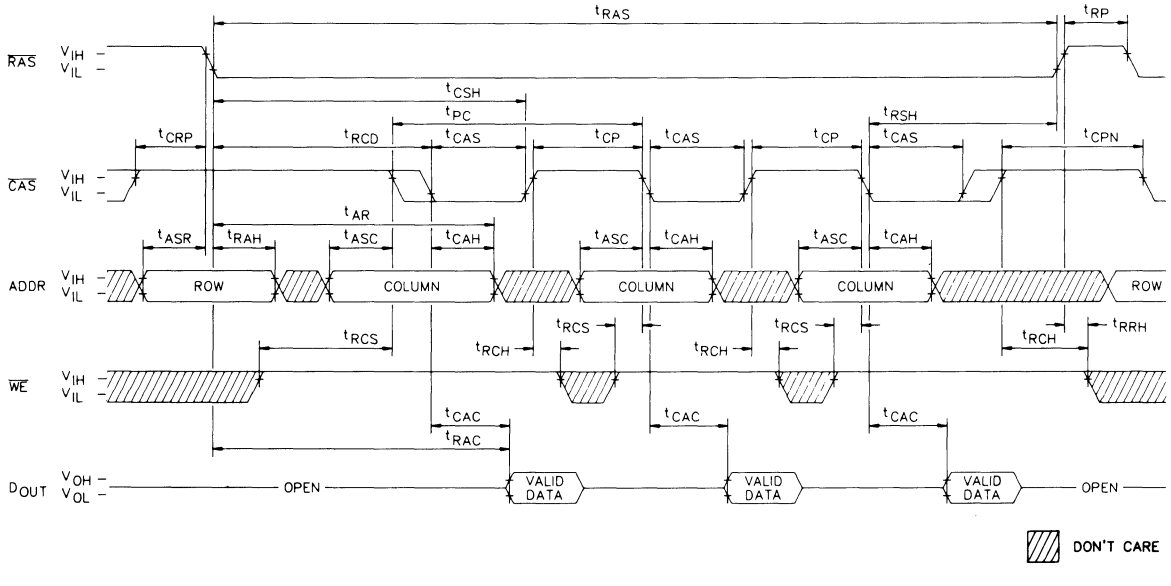
EARLY-WRITE CYCLE



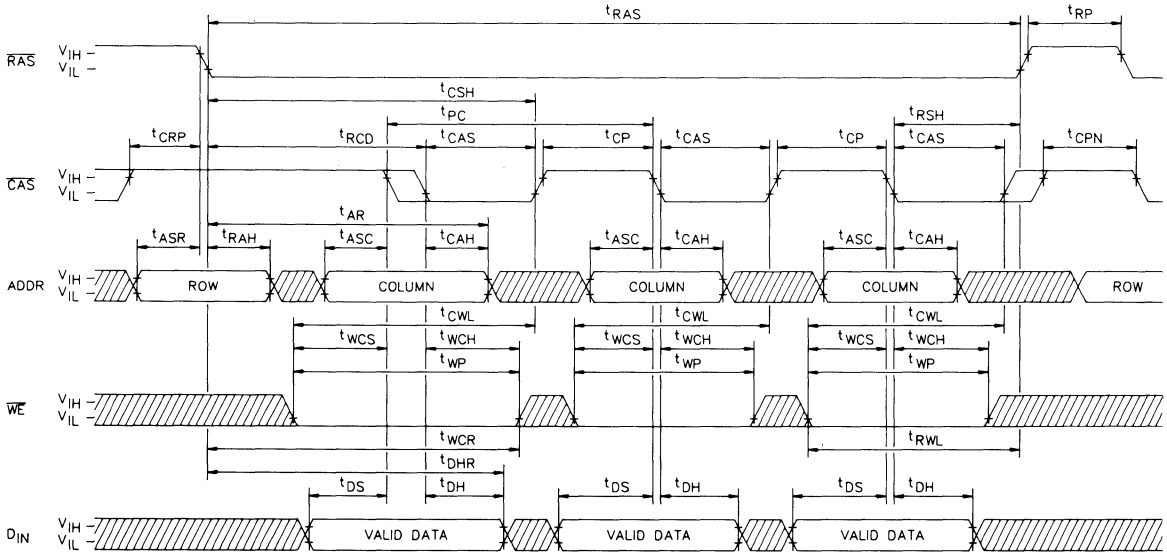
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



PAGE-MODE READ CYCLE

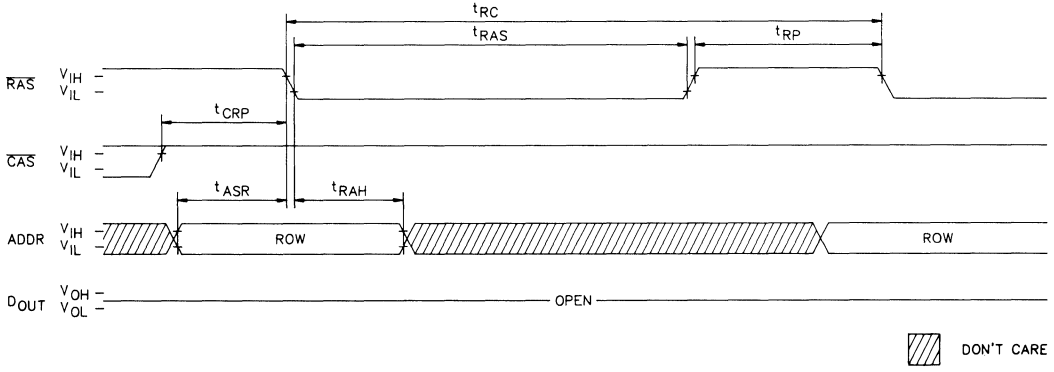


PAGE-MODE EARLY-WRITE CYCLE



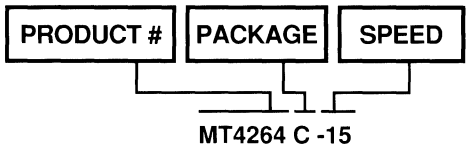
RAS ONLY REFRESH CYCLE

(ADDR = A_0 - A_7)



ORDER INFORMATION

64K x 1, 150ns in Ceramic DIP



The Micron MT4264 is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the NMOS double-poly process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM 64K x 4 DRAM

FEATURES

- Industry standard pin-out, timing, functions
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby, 150mW active, typical
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 256 cycle refresh in 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

- Timing

80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15

- Packages:

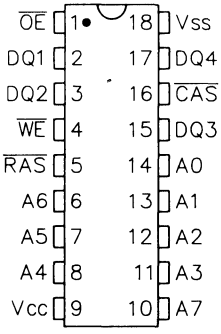
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic PLCC	EJ

- Temperature

$0°C \le T_A \le 70°C$	None
$-55°C \le T_A \le 110°C$	XT

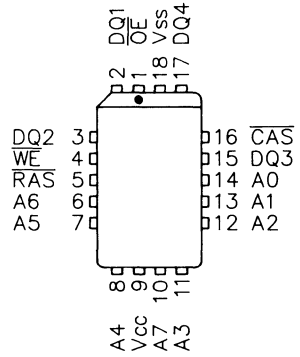
PIN ASSIGNMENT (Top View)

MT4067 18 Pin DIP



PB, CB

MT4067 18 Pin PLCC



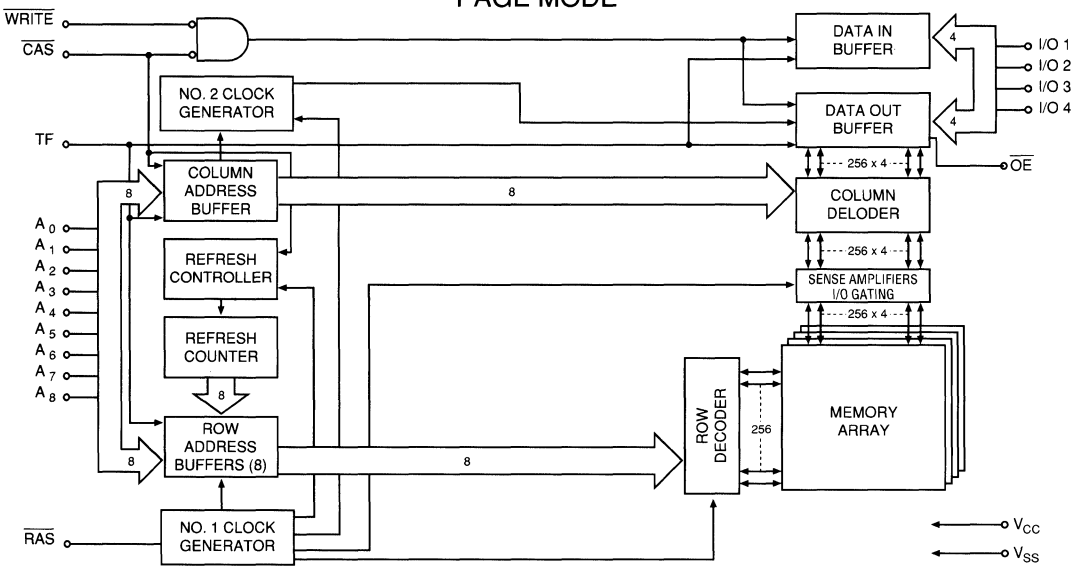
EJA

GENERAL DESCRIPTION

The MT4067 is randomly accessed solid-state memory containing 262,144 bits organized in a x4 configuration. The 16 address bits are entered 8 bits at a time using $\overline{RAS}$ to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. If the $\overline{WE}$ pin goes low prior to $\overline{CAS}$ going low, the output pin remains open until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after Data reaches the output pin, the output pin is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-MODIFY-WRITE cycle. Data-in is latched when $\overline{WE}$ strobes low.

By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled to execute several faster READ, WRITE, READ-WRITE or READ-MODIFY-WRITE cycles within the $\overline{RAS}$ address defined PAGE boundary. Returning $\overline{RAS}$ high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the $\overline{RAS}$ high-time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (Refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	OE	Addresses tR	Addresses tC		NOTES
Standby	H	H	H	H	X	X	High Impedance	
READ	L	L	H	L	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	H	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	H	L	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	H	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts	I_I	-10	10	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

(Notes: 1,2,3,4,6) (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	5	5	5	5	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	65	55	55	45	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	65	55	55	45	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	55	40	40	35	mA	2
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	65	55	55	45	mA	2,22

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8), D_{IN}	C_{I1}		5	pF	18
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		8	pF	18
Output Capacitance D_{OUT}	C_O		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

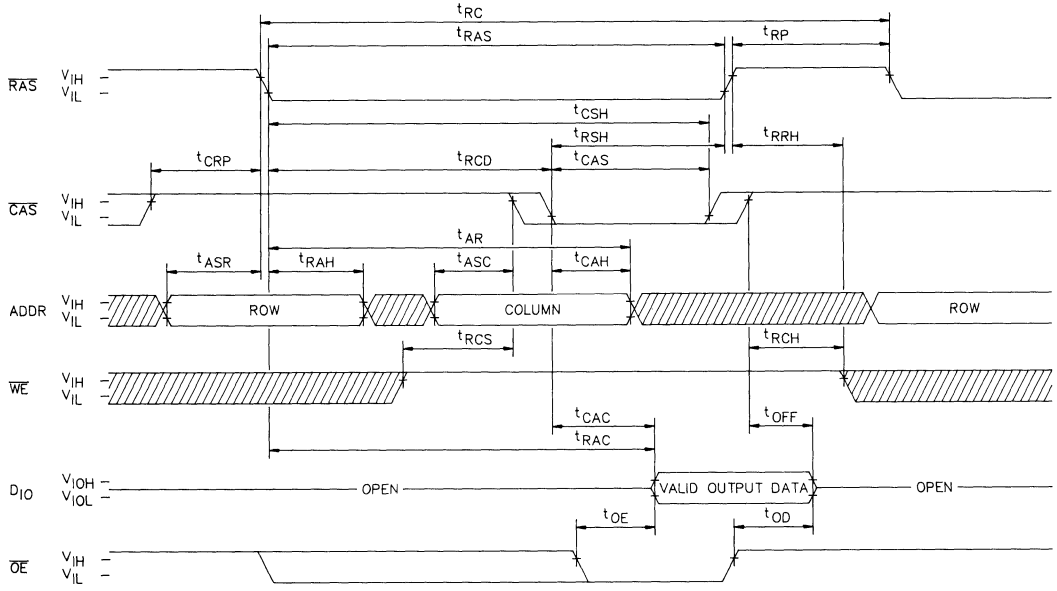
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	200		250		295		345		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
Output Enable	^tOE		25		25		30		40	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
Output Disable	^tOD		25		30		30		35	ns	
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		60		65		70		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	50		70		90		110		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	90		120		150		185		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	22
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	21

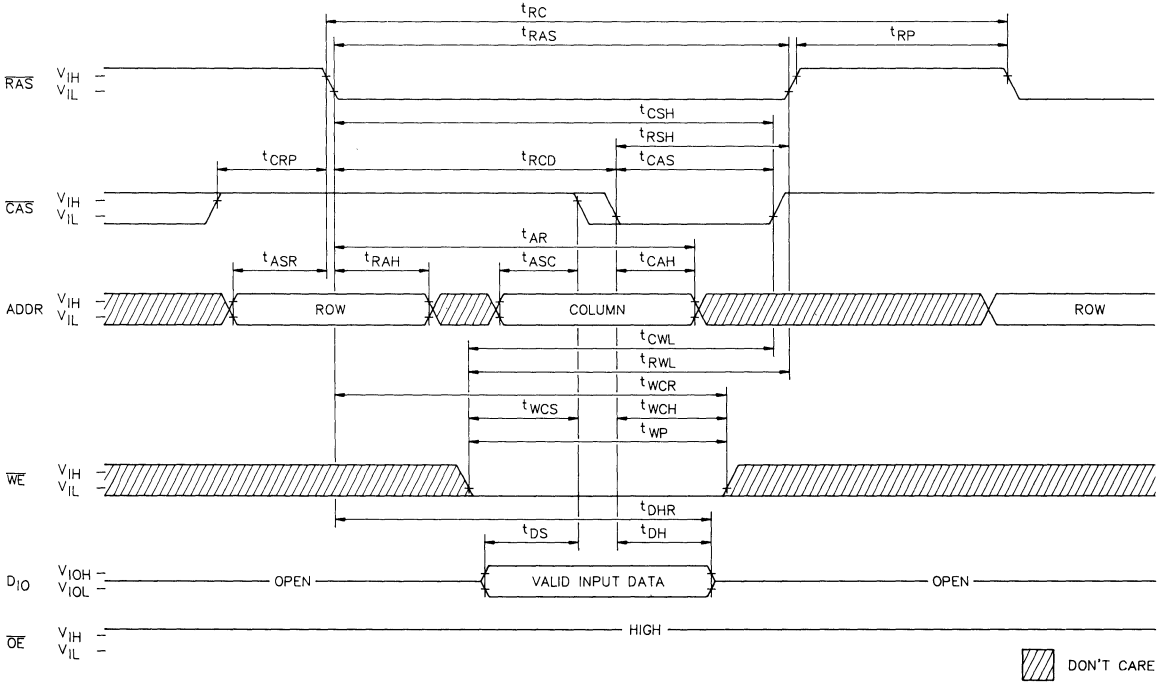
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (min) the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \ge ^tCWD$ (min) and $^tRWD \ge ^tRWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is inde terminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCP. Note 8 applies to determine valid data out.
20. During a READ cycle if $\overline{OE}$ is low then taken high (V_{IH}) Dout goes open. If $\overline{OE}$ is tied permanently low a READ-MODIFY-WRITE operation is not possible.
21. On-chip refresh and address counters are enabled.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.

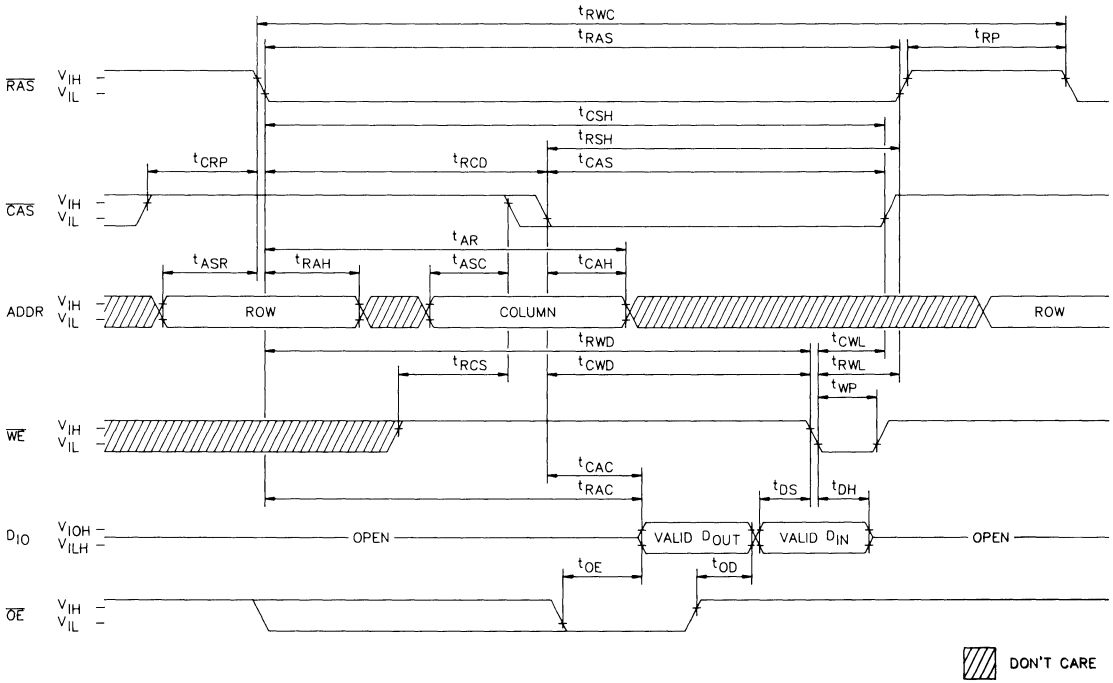
READ CYCLE



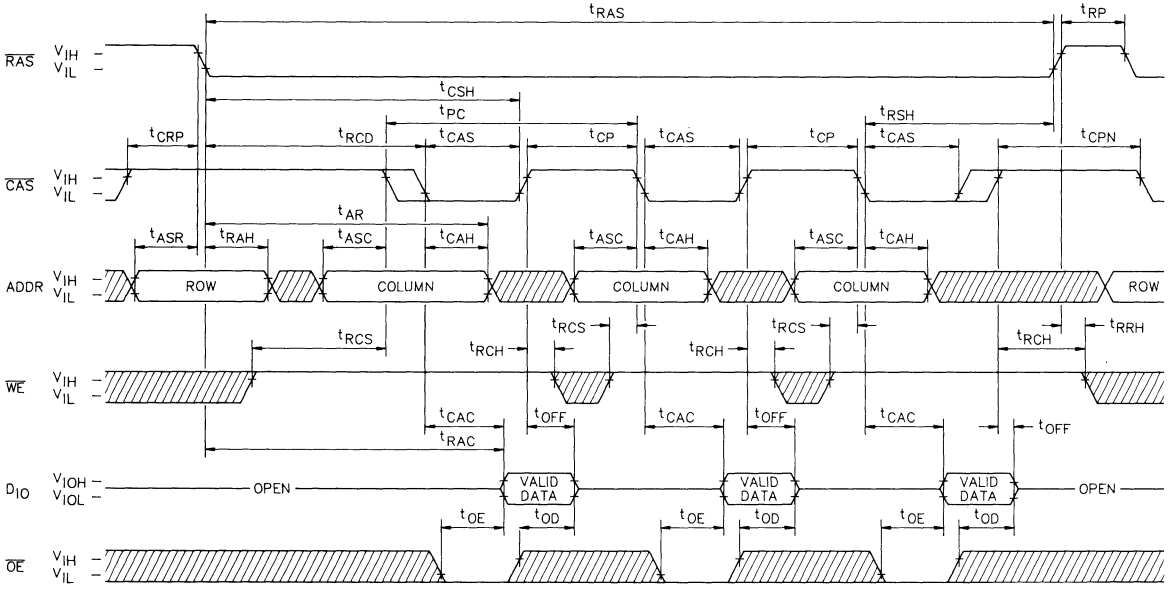
EARLY-WRITE CYCLE



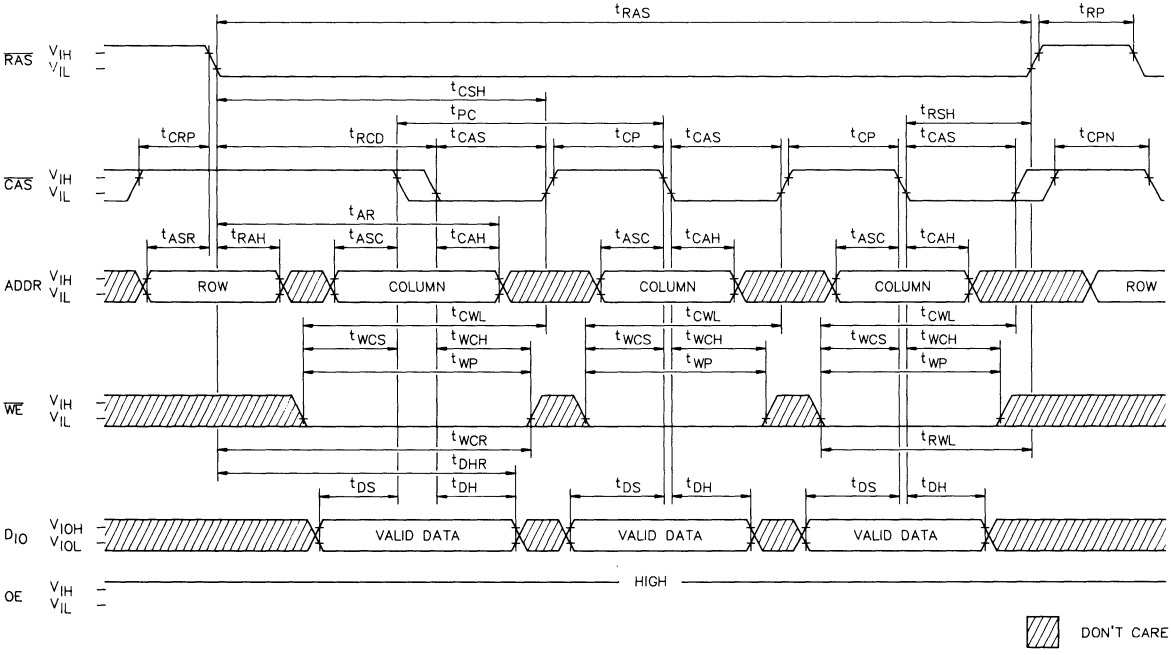
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



PAGE-MODE READ CYCLE

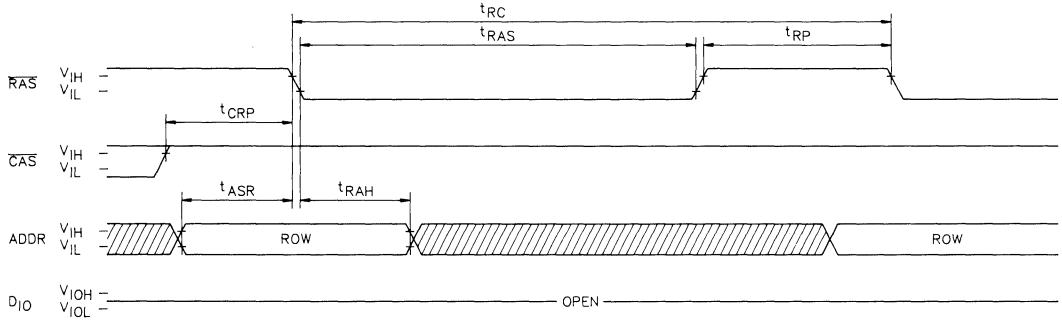


PAGE-MODE EARLY-WRITE CYCLE



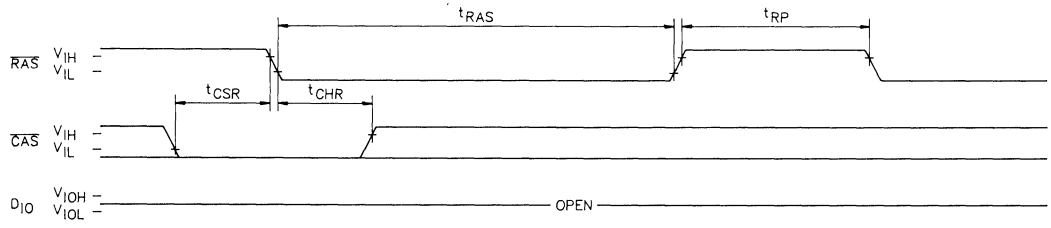
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; and $\overline{WE}$ = DON'T CARE.)



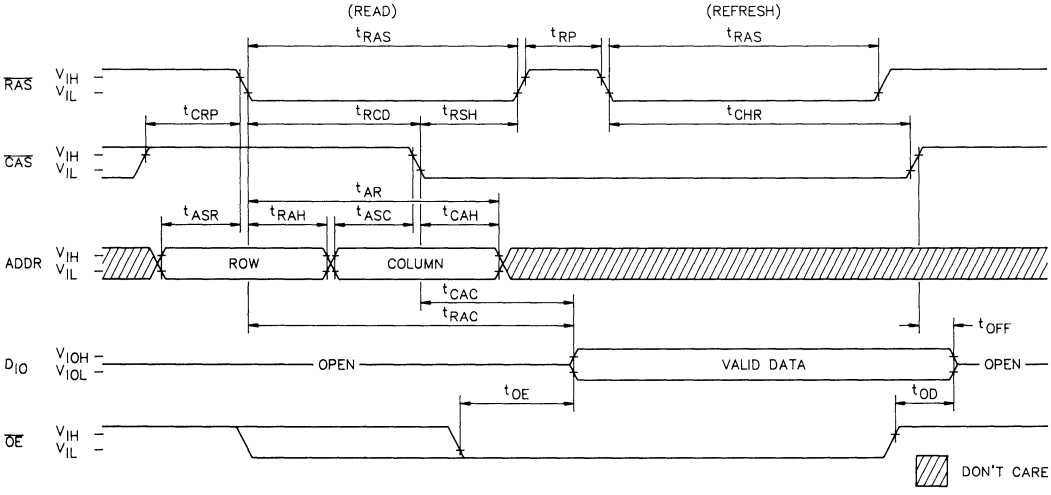
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_7 $\overline{WE}$, $\overline{OE}$ = DON'T CARE.)



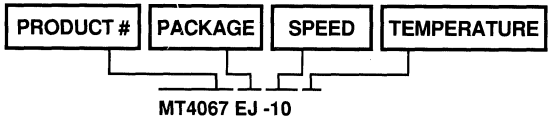
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[22]



ORDER INFORMATION

64K x 4, 100ns in Plastic PLCC



The Micron MT4067 is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the NMOS double-poly process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM 256K x 1 DRAM

FEATURES

- Industry standard pin-out, timing, functions
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby, 150mW active, typical
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 256 cycle refresh in 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

- Timing

80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15

- Packages:

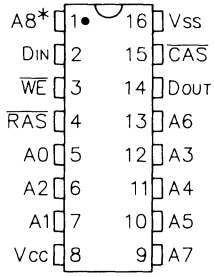
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic PLCC	EJ

- Temperature

$0°C \le T_A \le 70°C$	None
$-55°C \le T_A \le 110°C$	XT

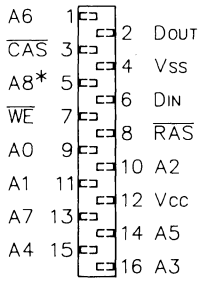
PIN ASSIGNMENT (Top View)

MT1259 16 Pin DIP



PA, CA

MT1259 16 Pin ZIP



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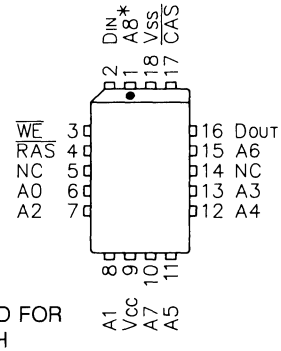
MT1259 18 Pin PLCC



EJA

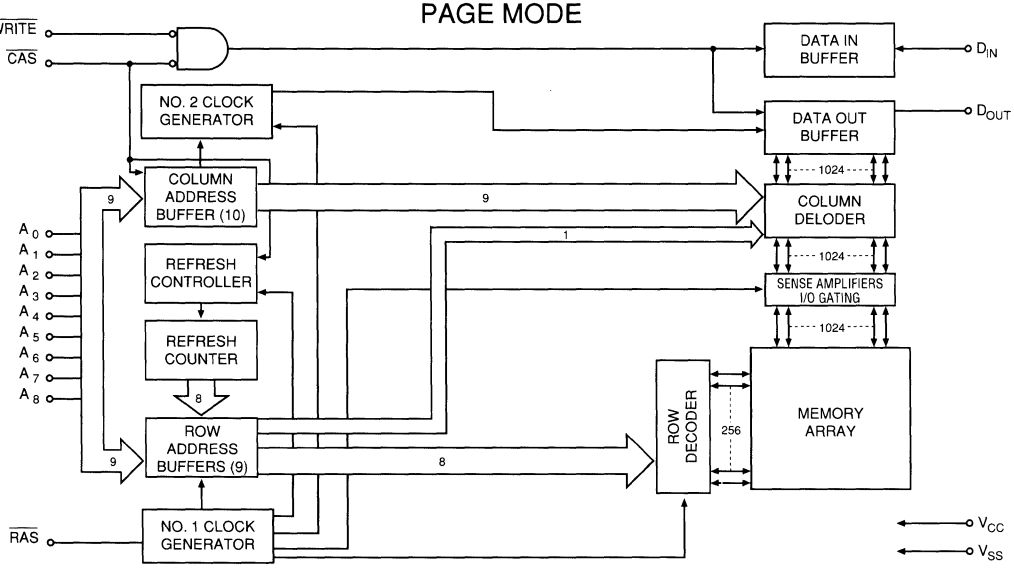
* ADDRESS NOT USED FOR $\overline{RAS}$ ONLY REFRESH

GENERAL DESCRIPTION

The MT1259 is randomly accessed solid-state memory containing 262,144 bits organized in a x1 configuration. The 18 address bits are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes low prior to $\overline{CAS}$ going low, the output pin remains open until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after Data reaches the output pin, the output pin is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-MODIFY-WRITE cycle. Data-in is latched when $\overline{WE}$ strobes low.

By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled to execute several faster READ, WRITE, READ-WRITE or READ-MODIFY-WRITE cycles within the $\overline{RAS}$ address defined PAGE boundary. Returning $\overline{RAS}$ high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the $\overline{RAS}$ high-time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (Refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts	I_I	-10	10	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

(Notes: 1,2,3,4,6) (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	5	5	5	5	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	65	55	55	45	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	65	55	55	45	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	55	40	40	35	mA	2
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	65	55	55	45	mA	2,20

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8), D_{IN}	C_{I1}		5	pF	18
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		8	pF	18
Output Capacitance D_{OUT}	C_O		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

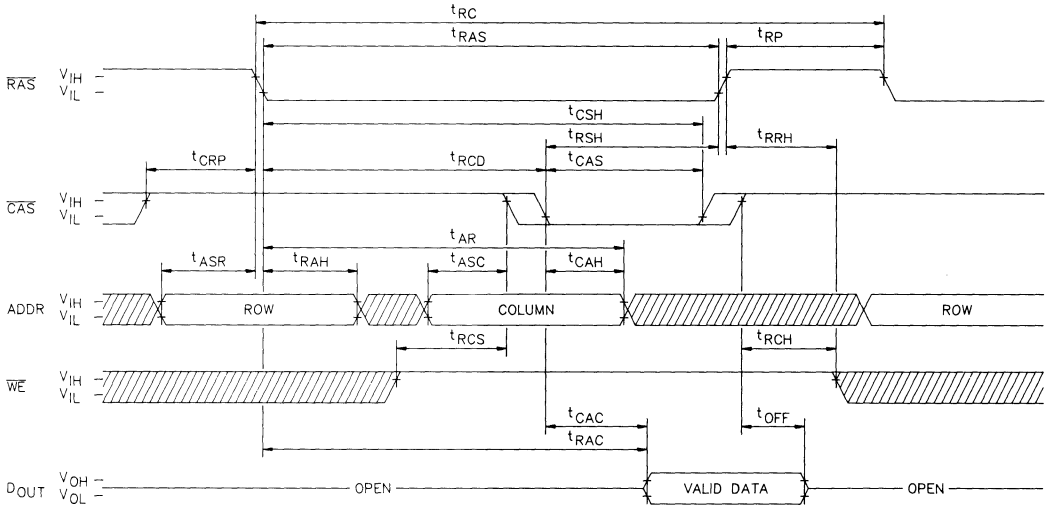
(Notes: 3, 4, 5, 10, 11, 17, 18) ($0°C \le T_A \le 70°C$) (V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	180		220		255		295		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
RAS pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	30		40		50		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	70		90		110		135		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	21
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	20

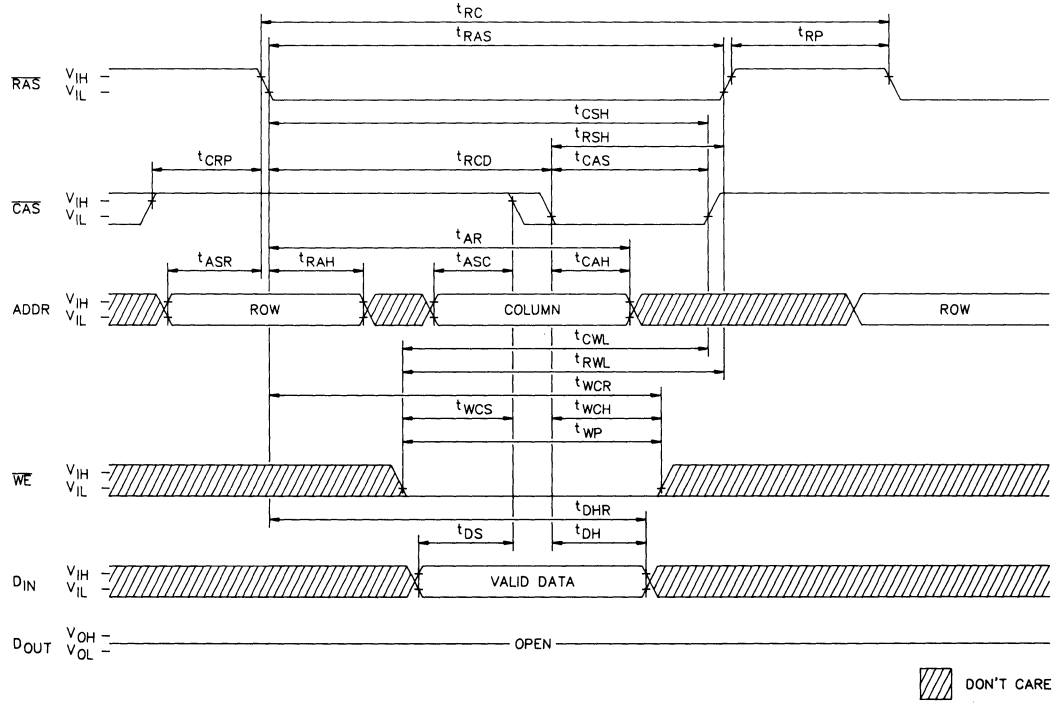
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq {}^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min) the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \geq {}^tCWD$ (min) and $^tRWD \geq {}^tRWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is inde terminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

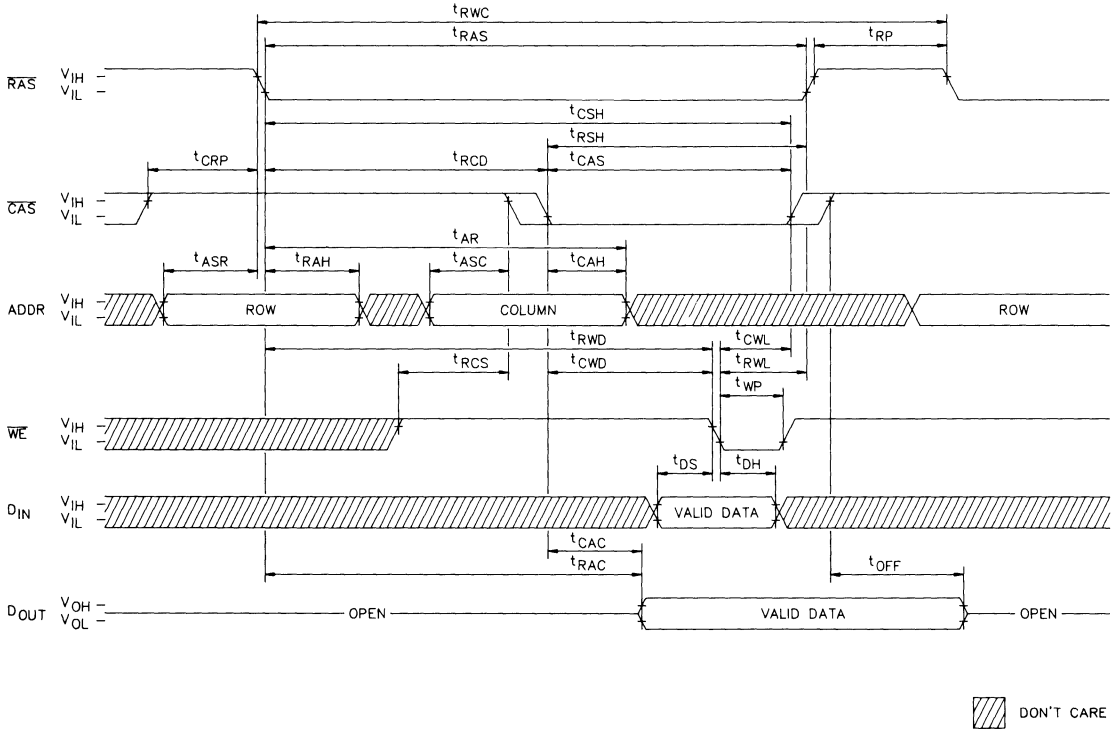
READ CYCLE



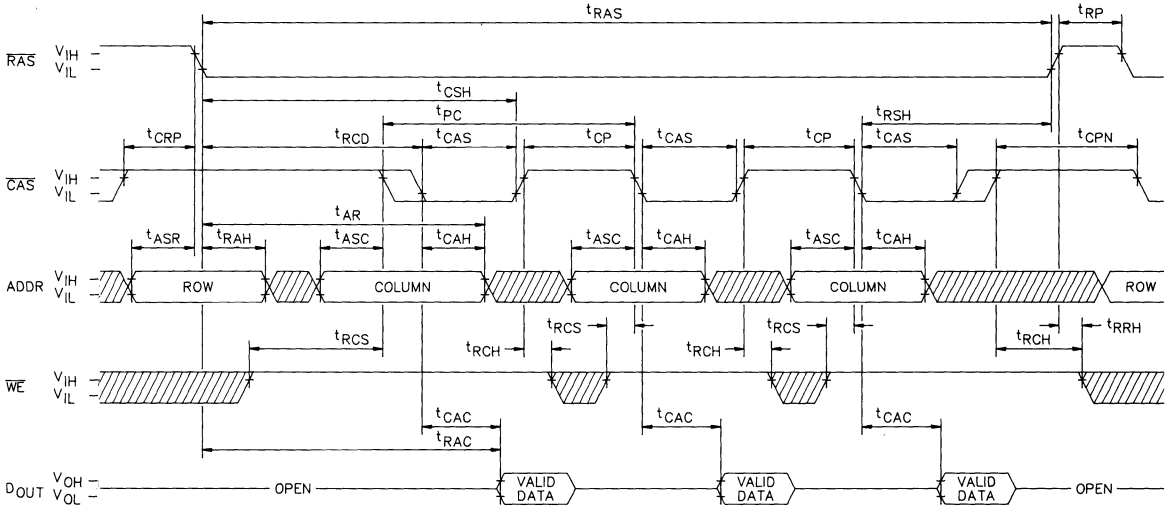
EARLY-WRITE CYCLE



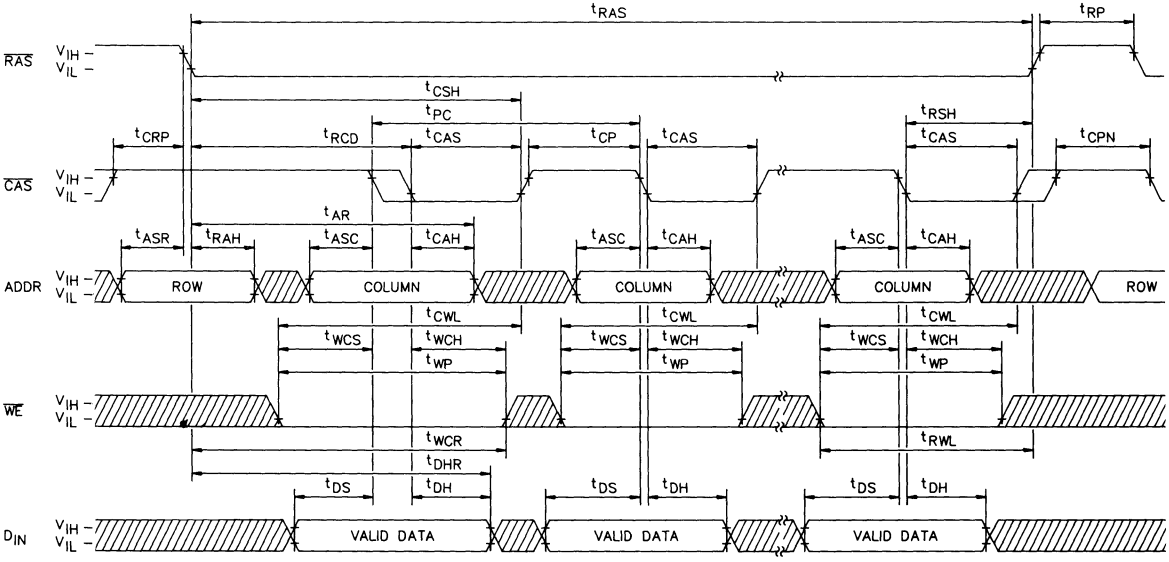
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



PAGE-MODE READ CYCLE

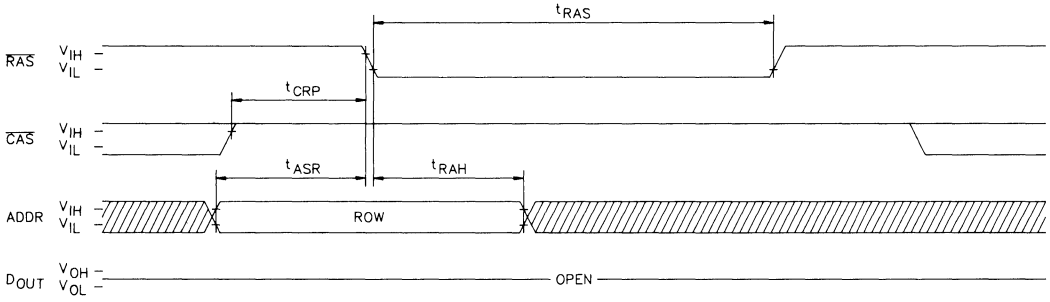


PAGE-MODE EARLY-WRITE CYCLE



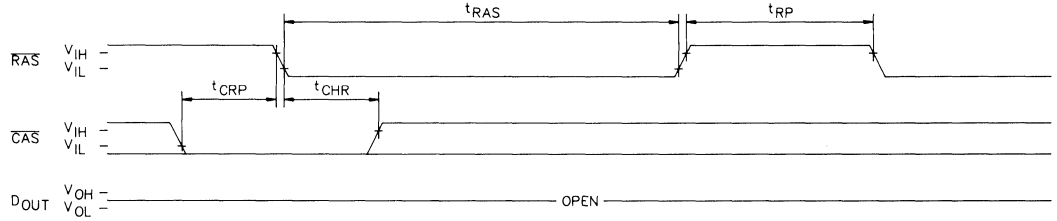
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



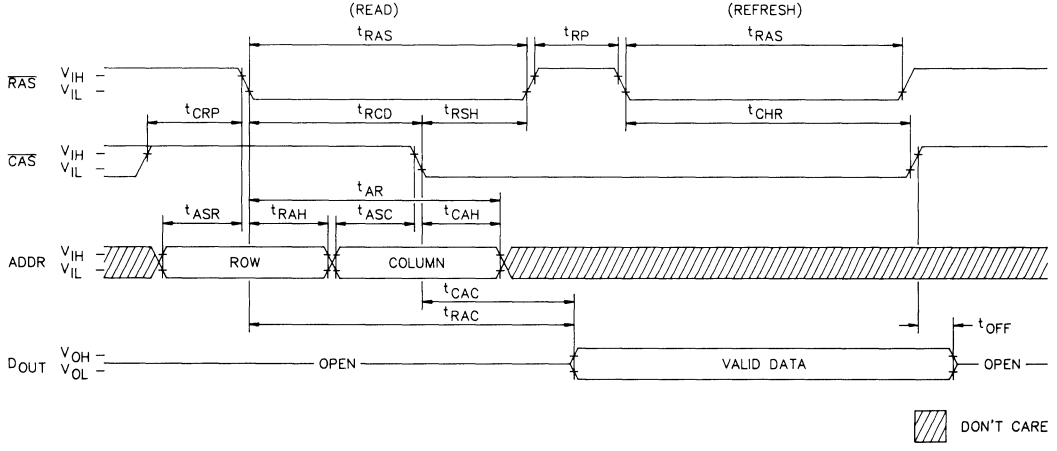
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 $\overline{WE}$ = DON'T CARE.)



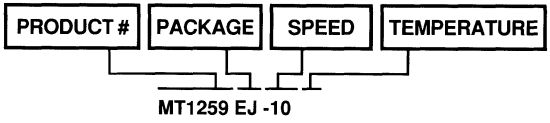
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[21]



ORDER INFORMATION

256K x 1, 100ns in Plastic PLCC



The Micron MT1259 is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the NMOS double-poly process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM

256K x 4 DRAM

FAST PAGE MODE

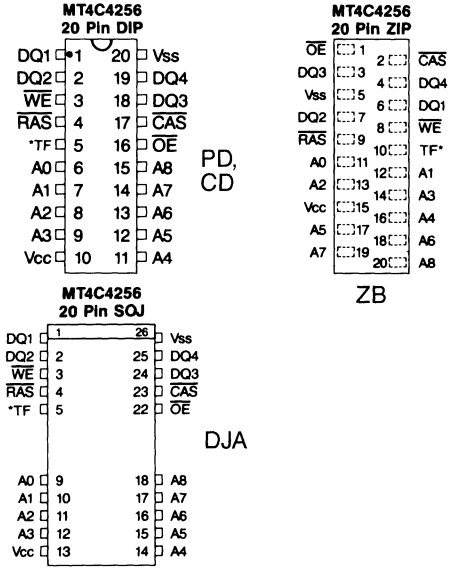
FEATURES

- Industry standard x4 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- Optional Fast Page Mode access cycle

OPTIONS

	MARKING
• Timing	
100ns access	-10
120ns access	-12
150ns access	-15
• Organization	
256K x 4	MT4C4256
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)



*TF = Test Function, ground of leave as a no-connect for normal device operation.

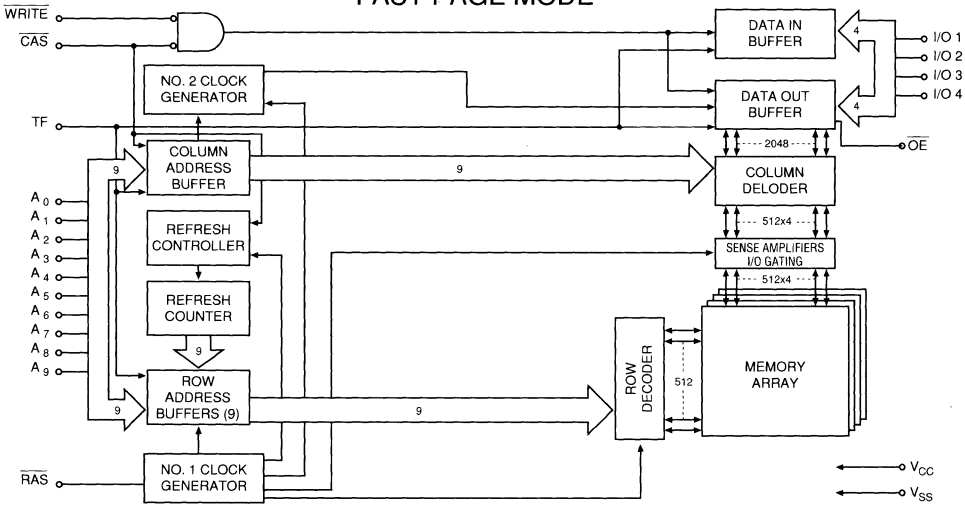
GENERAL DESCRIPTION

The MT4C4265 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	OE	TF	Addresses			NOTES
						tR	tC		
Standby	H	H	H	H	GND/NC	X	X	High Impedance	
READ	L	L	H	L	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	H	GND/NC	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	H	L	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	H	GND/NC	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	H	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	H	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	H	GND/NC	X	X	High Impedance	
TEST FUNCTION	L	L	H	H	H	ROW	COL	Data Out, Test Funtion Mode	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$, = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		50	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		1	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		35	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		35	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9), D_{IN}	C_{I1}		5	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Output Capacitance D_{OUT}	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	190		220		260		ns	
READ-MODIFY-WRITE cycle time	t_{RWC}	220		255		295		ns	
PAGE-MODE READ or WRITE cycle time	t_{PC}	55		70		85		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	14
Access time from $\overline{CAS}$	t_{CAC}		25		30		45	ns	15
Output Enable	t_{OE}		25		25		30	ns	
Access time from column address	t_{AA}		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		65		75	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	t_{RASP}	100	100,000	120	100,000	150	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	80		90		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{CAS}$ precharge time	t_{CPN}	15		20		25		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	t_{CP}	10		15		20		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	10	75	15	90	15	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	10	50	15	60	15	70	ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	50		60		70		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	5		5		5		ns	
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	30	ns	20
Output Disable	t_{OD}		25		25		30	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

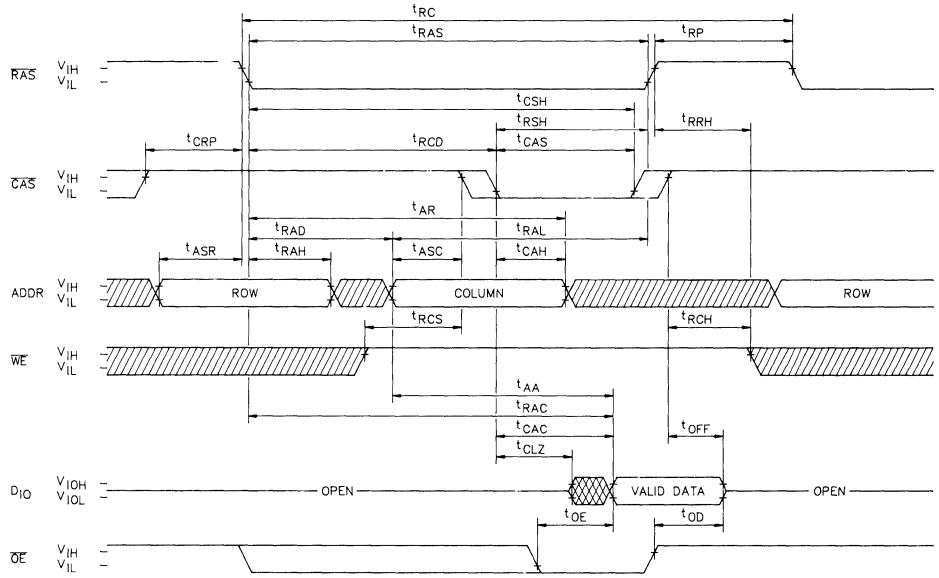
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	20		25		30		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	
Write command pulse width	^tWP	20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	120		150		185		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	80		100		120		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	65		75		85		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5

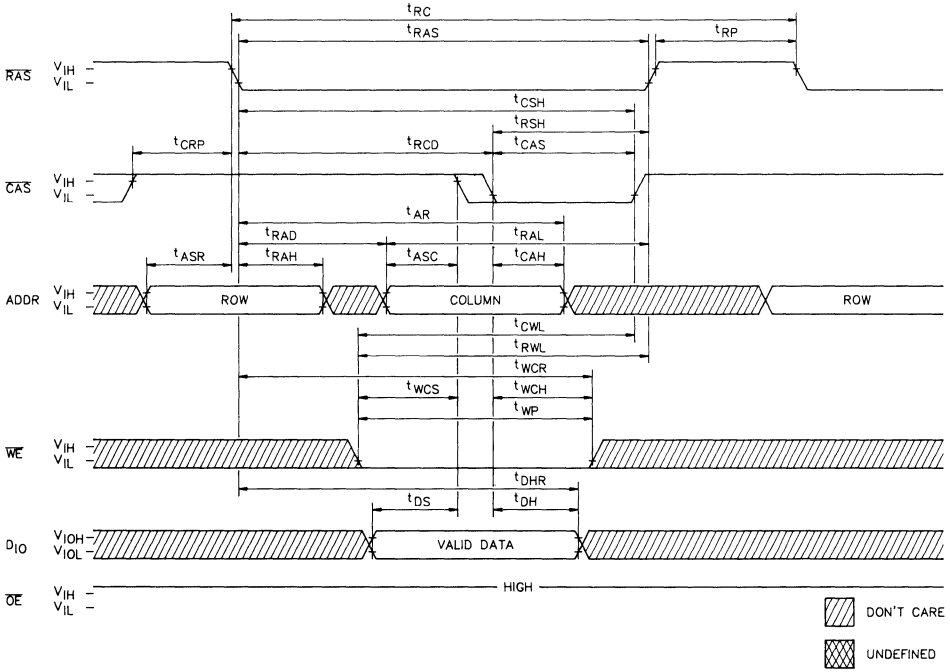
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH D_{OUT} goes open. If $\overline{OE}$ is tied permanently low a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.

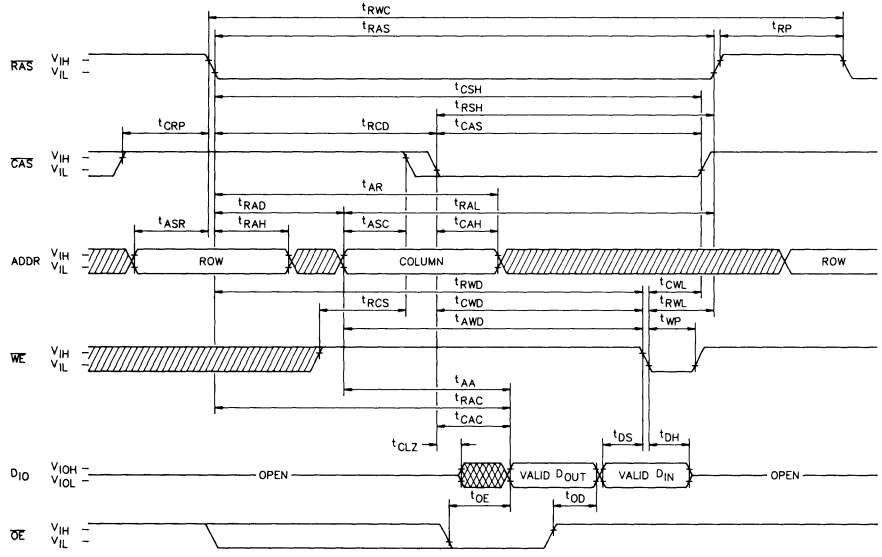
READ CYCLE



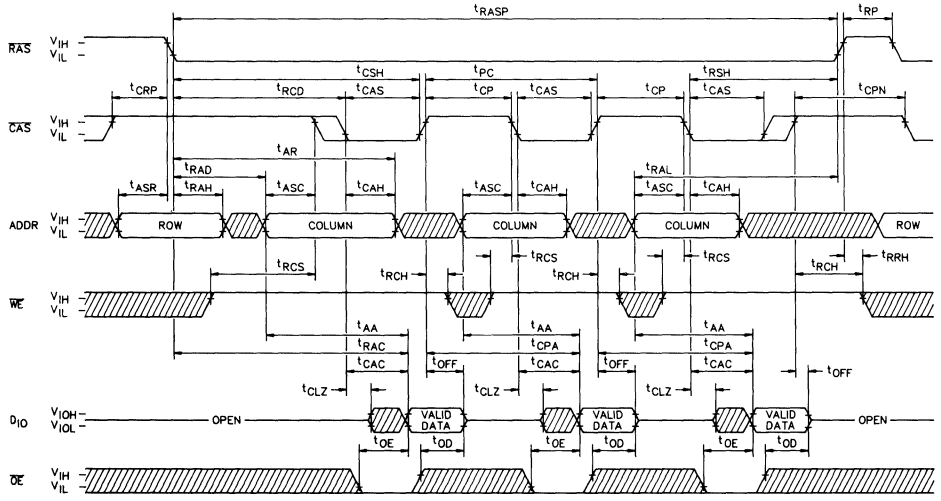
EARLY-WRITE CYCLE



READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



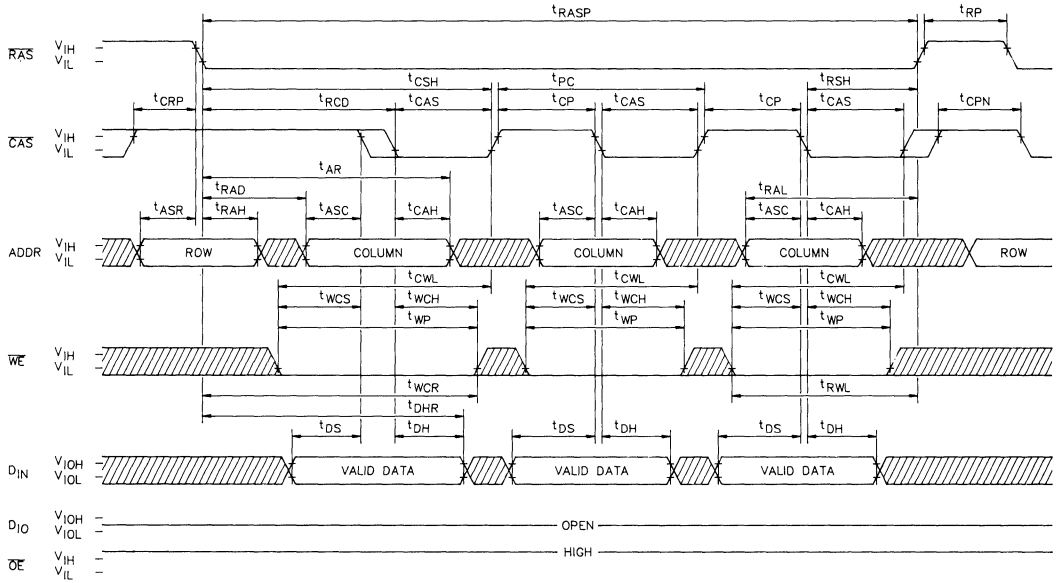
PAGE-MODE READ CYCLE



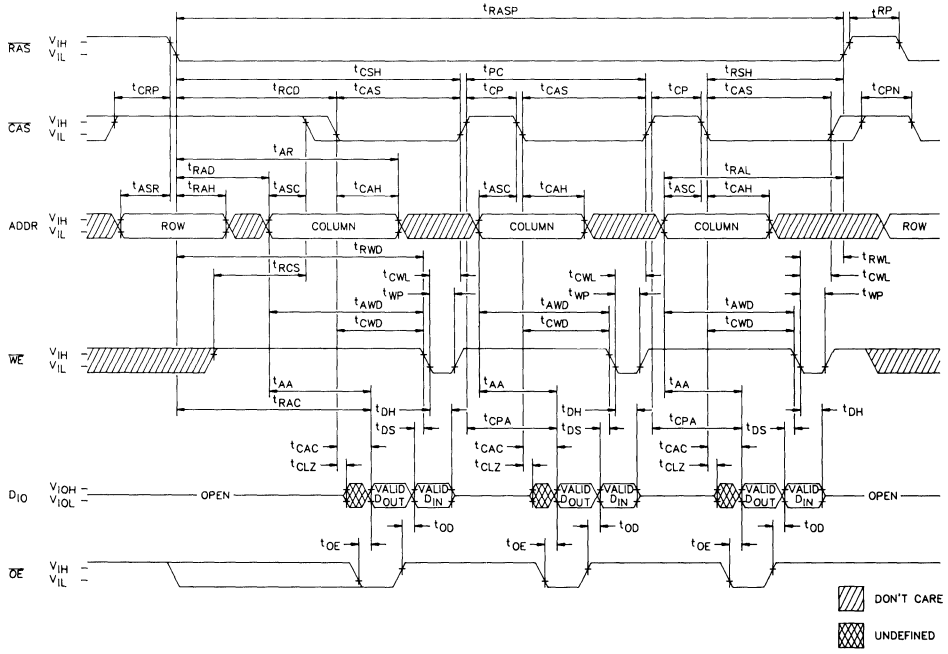
DON'T CARE

UNDEFINED

PAGE-MODE EARLY-WRITE CYCLE

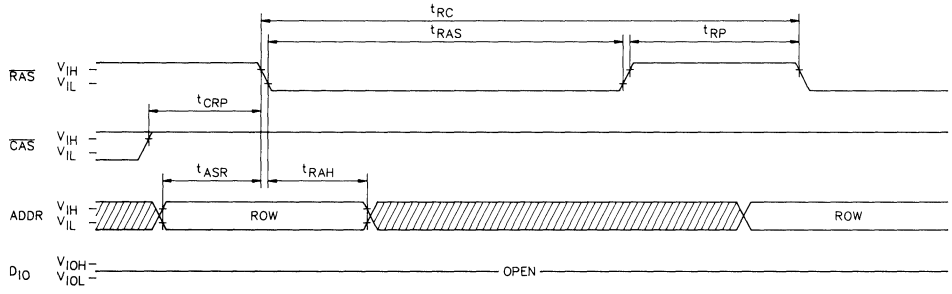


PAGE-MODE READ-WRITE CYCLE



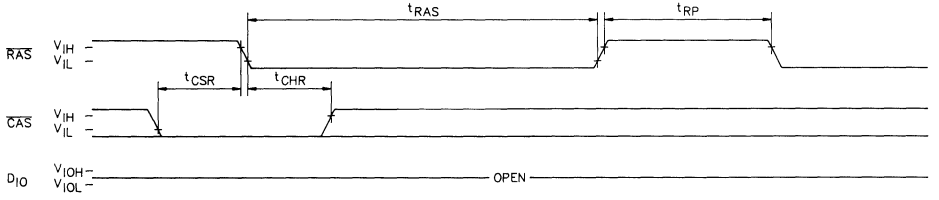
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



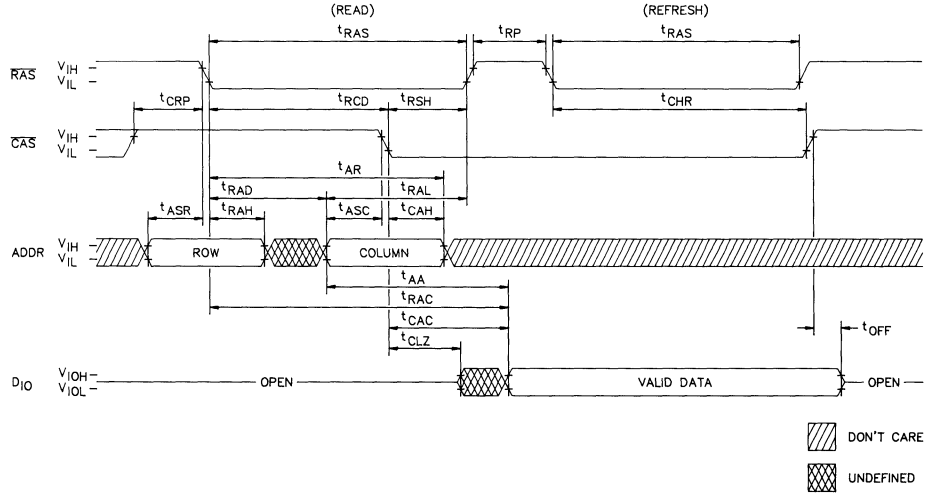
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



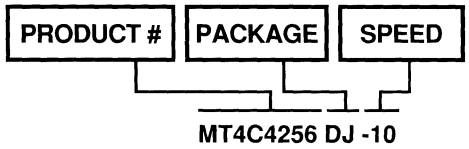
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH); $\overline{OE}$=LOW)[24]



ORDER INFORMATION

256K x 4, 120ns in Plastic DJ



The Micron 1 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM

256K x 4 DRAM

STATIC COLUMN

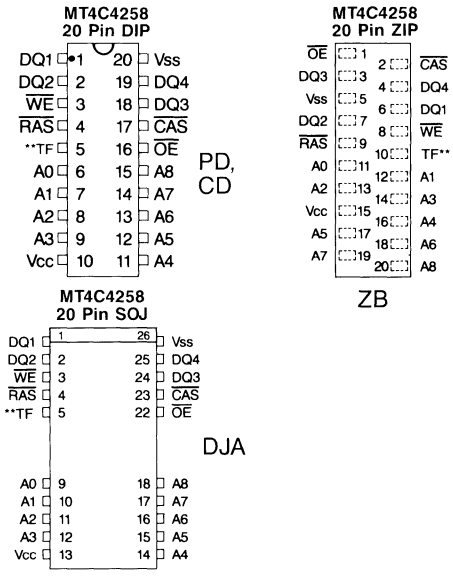
FEATURES

- Industry standard x4 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- Optional Static Column access cycle

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
100ns access	-10
120ns access	-12
150ns access	-15
• Organization	
256K x 4	MT4C4258
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)



*TF = Test Function, ground of leave as a no-connect for normal device operation.

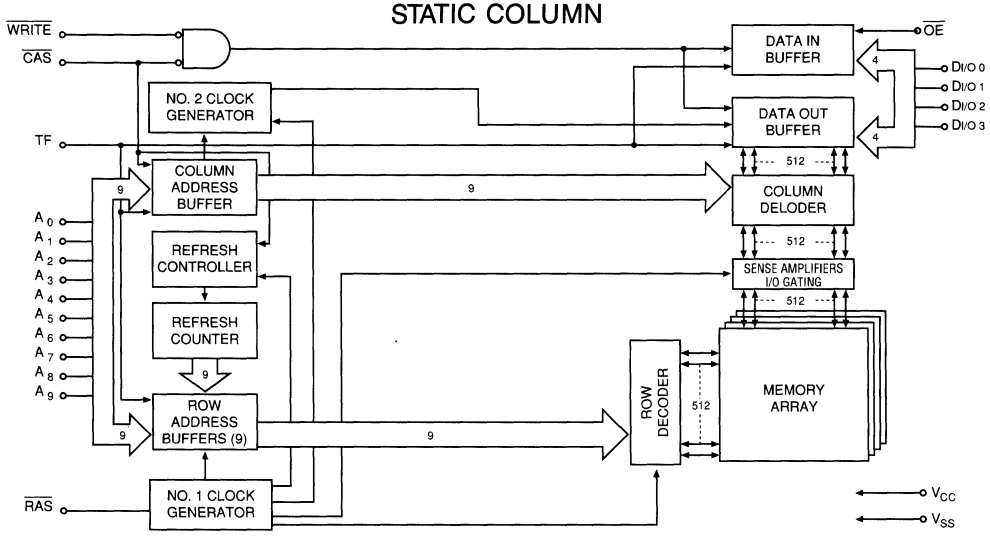
GENERAL DESCRIPTION

The MT4C4258 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

STATIC COLUMN operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the STATIC COLUMN operation.

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



FUNCTIONAL TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	TF	Addresses			NOTES
						tR	tC		
Standby	H	H	H	H	GND/NC	X	X	High Impedance	
READ	L	L	H	L	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	H	GND/NC	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
STATIC COLUMN READ	L	L	H	L	GND/NC	ROW	COL→COL	Valid Data Out, Valid Data Out	
STATIC COLUMN WRITE	L	L	L	H	GND/NC	ROW	COL→COL	Valid Data In, Valid Data In	
STATIC COLUMN READ-WRITE	L	L	H→L→H	L→H	GND/NC	ROW	COL→COL	Valid Data Out, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	H	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	H	GND/NC	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	H	GND/NC	X	X	High Impedance	
TEST FUNCTION	L	L	H	H	H	ROW	COL	Data Out, Test Funtion Mode	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$, = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		50	mA	3, 4
OPERATING CURRENT: STATIC COLUMN ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		1	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		35	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		35	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9), D_{IN}	C_{I1}		5	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Output Capacitance D_{OUT}	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	190		220		260		ns	
READ-MODIFY-WRITE cycle time	^tRWC	220		255		295		ns	
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	14
Access time from $\overline{CAS}$	^tCAC		25		30		45	ns	15
Output Enable	^tOE		25		25		30	ns	
Access time from column address	^tAA		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		50		65		75	ns	
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		30		45		ns	
$\overline{RAS}$ precharge time	^tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	15		20		25		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	75	15	90	15	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	10	50	15	60	15	70	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	50		60		70		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	5		5		5		ns	
Output buffer turn-off delay	^tOFF	0	25	0	25	0	30	ns	20
Output Disable	^tOD		25		25		30	ns	
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	20		25		30		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

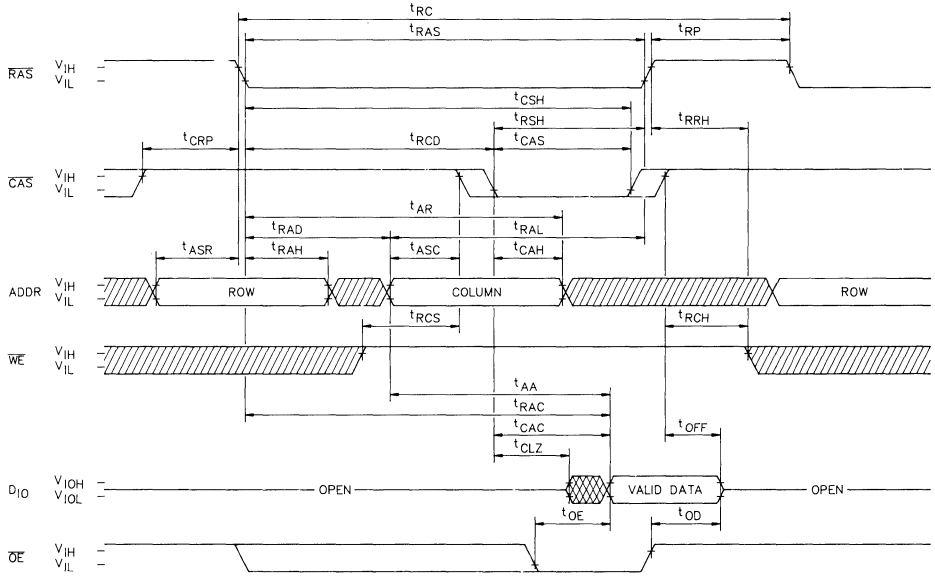
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	
Write command pulse width	^tWP	20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	120		150		185		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	80		100		120		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	65		80		95		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5
STATIC COLUMN MODE cycle time	^tSC	55		65		75		ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	100	100,000	120	100,000	150	100,000	ns	
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		15		20		ns	
STATIC COLUMN READ-MODIFY-WRITE cycle time	^tSRMW	135		160		185		ns	
Last write to column address delay time	^tLWAD	25	45	30	55	45	70	ns	
Last write to column address hold time	^tAHLW		95		115		135	ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	^tROH	20		20		20		ns	
Output data hold time from column address	^tAOH	5	—	5	—	5	—	ns	
Output data enable from write	^tOW		30		35		40	ns	
$\overline{OE}$ to data delay	^tOED	25		30		35		ns	
$\overline{OE}$ command hold time	^tOEH	25		25		30		ns	
Access time from last write	^tALW		95		115		140	ns	

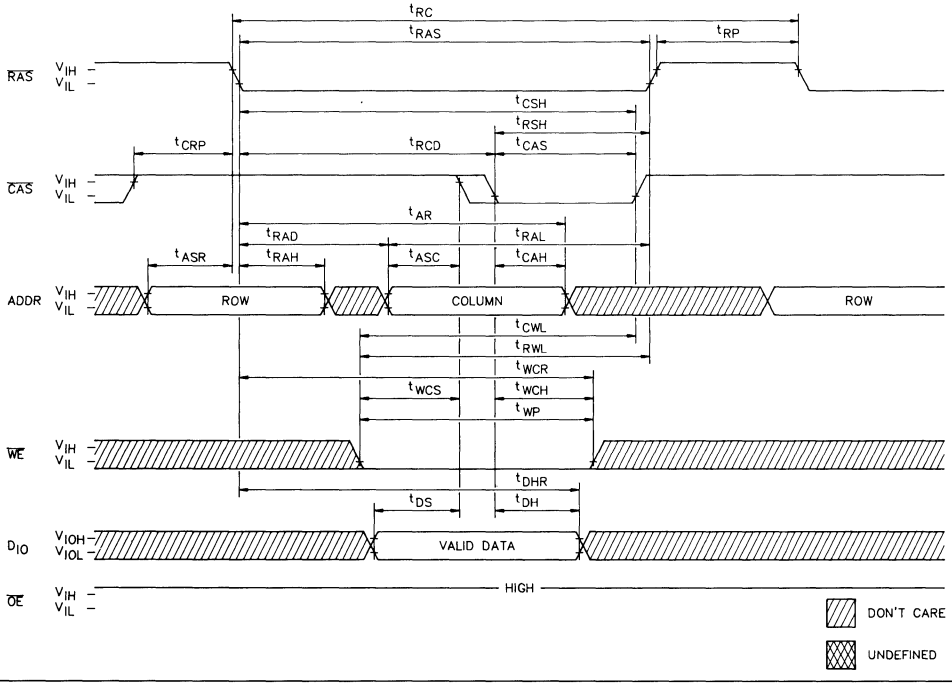
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (min), $^tAWD \geq {}^tAWD$ (min) and $^tCWD \geq {}^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH D_{OUT} goes open. If $\overline{OE}$ is tied permanently low a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.

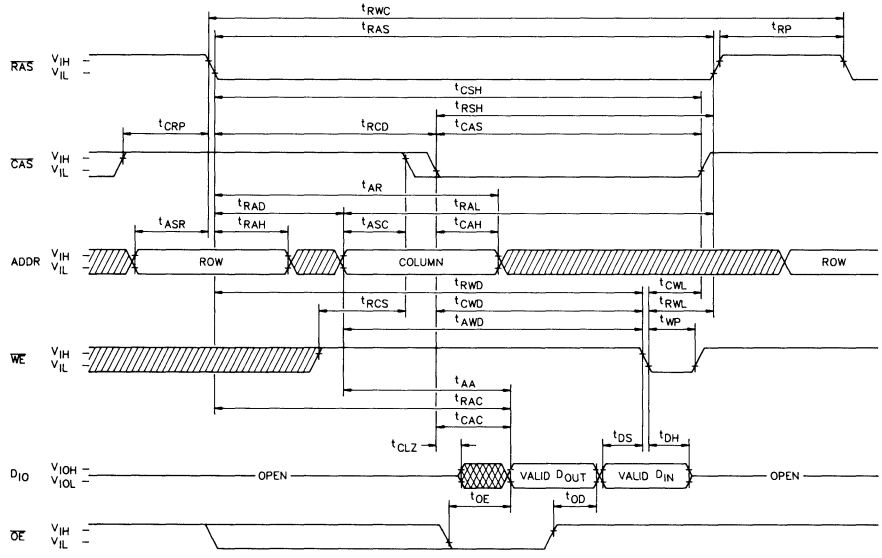
READ CYCLE



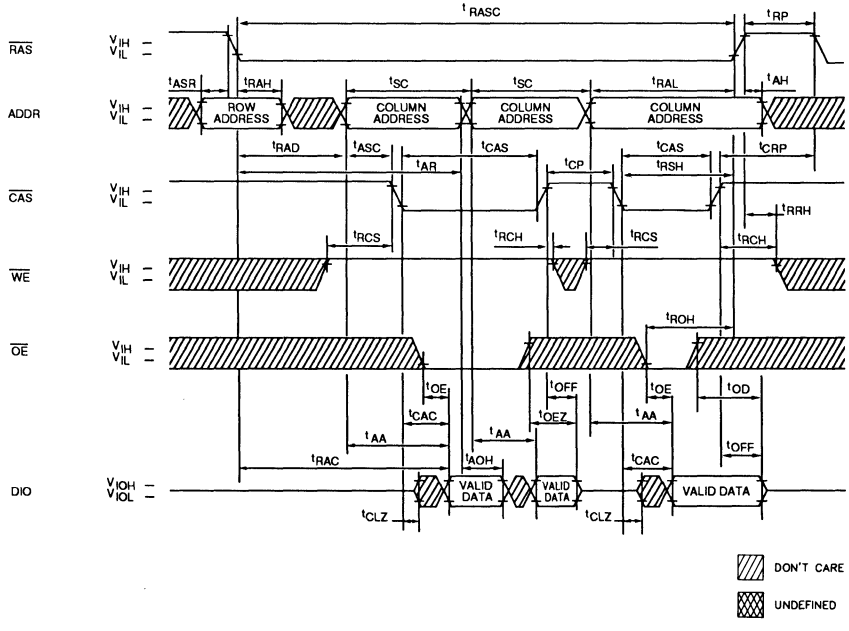
EARLY-WRITE CYCLE



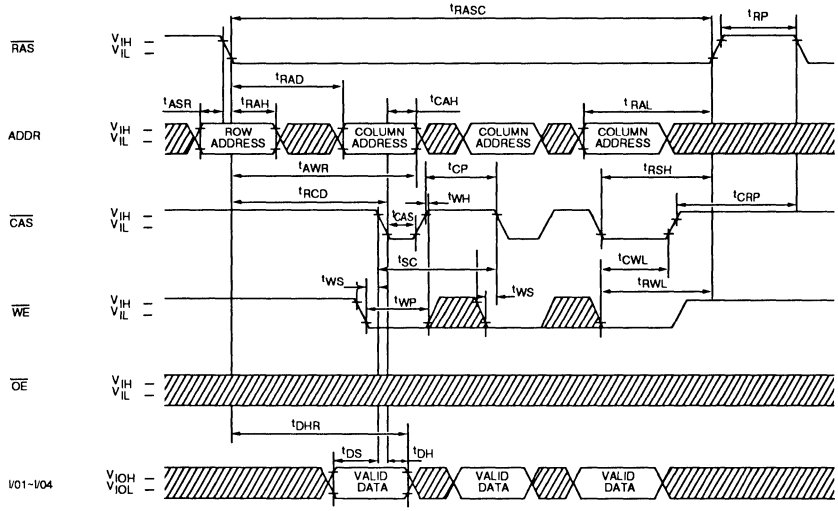
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



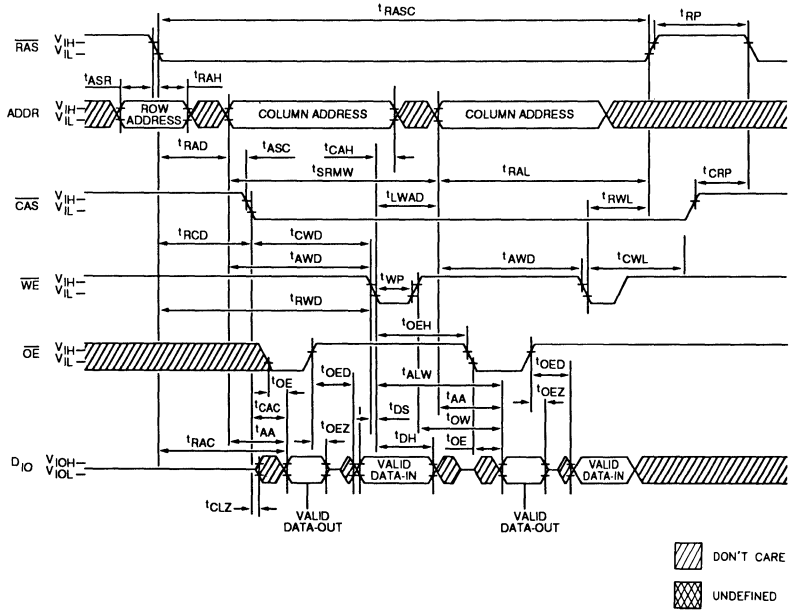
STATIC COLUMN READ CYCLE



STATIC COLUMN EARLY-WRITE CYCLE

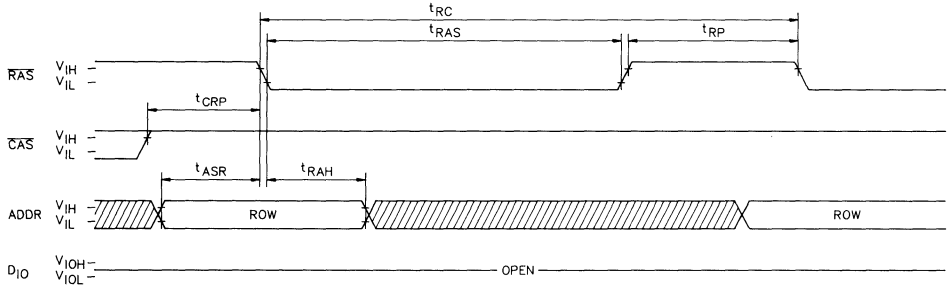


STATIC COLUMN READ-WRITE CYCLE



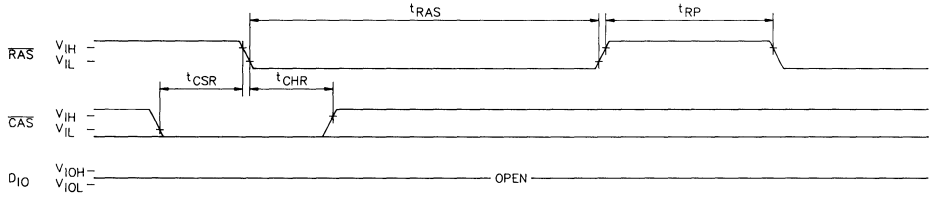
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



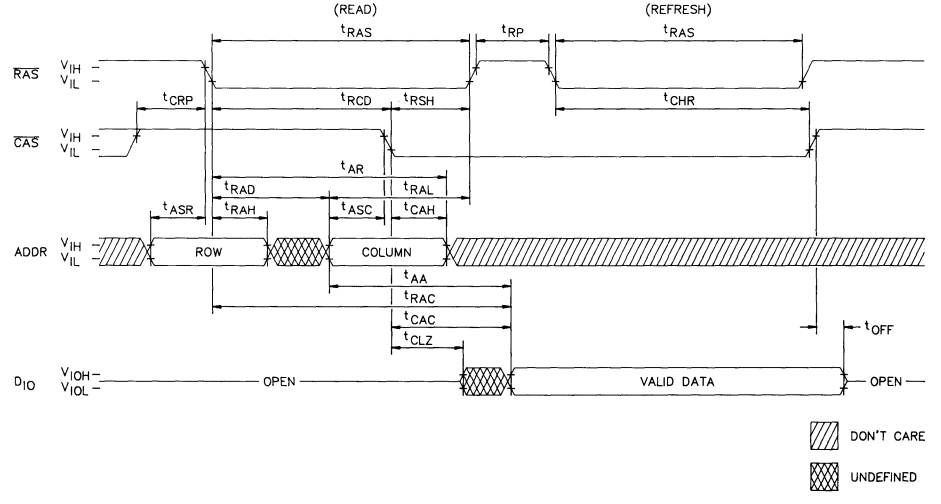
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



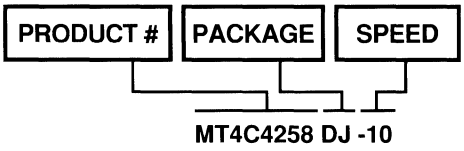
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH); $\overline{OE}$=LOW)[24]



ORDER INFORMATION

256K x 4, 120ns in Plastic DJ



The Micron 1 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM

1MEG x 1 DRAM

FAST PAGE MODE

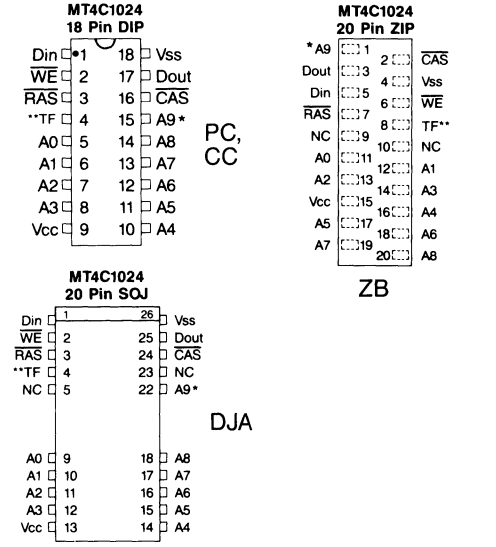
FEATURES

- Industry standard x1 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- Optional Fast Page Mode access cycle

OPTIONS

	MARKING
• Timing	
100ns access	-10
120ns access	-12
150ns access	-15
• Organization	
1 MEG x 1	MT4C1024
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)



*Address not used for $\overline{RAS}$ only refresh
**TF = Test Function, ground of leave as a no-connect for normal device operation.

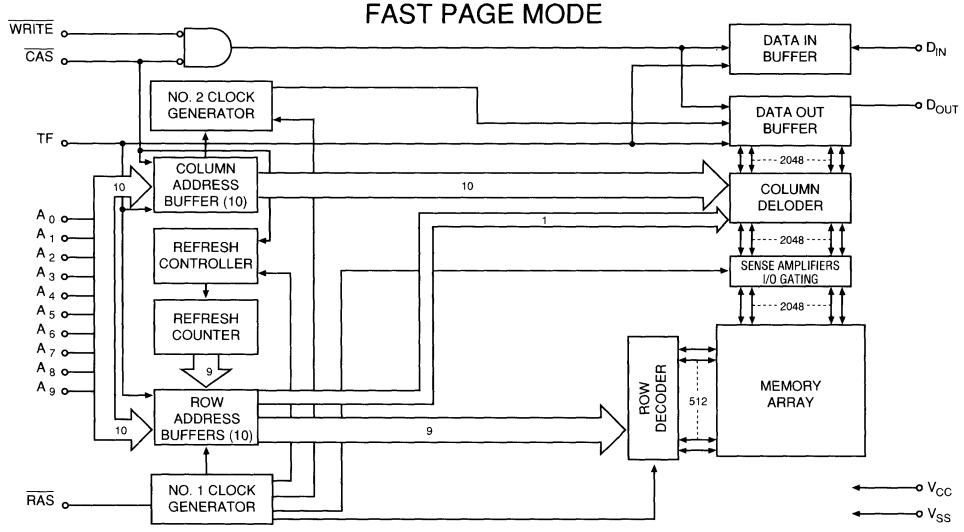
GENERAL DESCRIPTION

The MT4C1024 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	TF	Addresses tR	Addresses tC		NOTES
Standby	H	H	H	GND/NC	X	X	High Impedance	
READ	L	L	H	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	H	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	GND/NC	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	GND/NC	X	X	High Impedance	
TEST FUNCTION	L	L	H	H	ROW	COL	Data Out, Test Funtion Mode	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$ = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		50	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		1	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		35	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		35	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9), D_{IN}	C_{I1}		5	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance D_{OUT}	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	190		220		260		ns	
READ-MODIFY-WRITE cycle time	^tRWC	220		255		295		ns	
PAGE-MODE READ or WRITE cycle time	^tPC	55		70		85		ns	
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	14
Access time from $\overline{CAS}$	^tCAC		25		30		45	ns	15
Access time from column address	^tAA		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		50		65		75	ns	
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	100	100,000	120	100,000	150	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		30		45		ns	
$\overline{RAS}$ precharge time	^tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	15		20		25		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	10		15		20		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	75	15	90	15	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	10	50	15	60	15	70	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	50		60		70		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	5		5		5		ns	
Output buffer turn-off delay	^tOFF	0	25	0	25	0	30	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	20		25		30		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

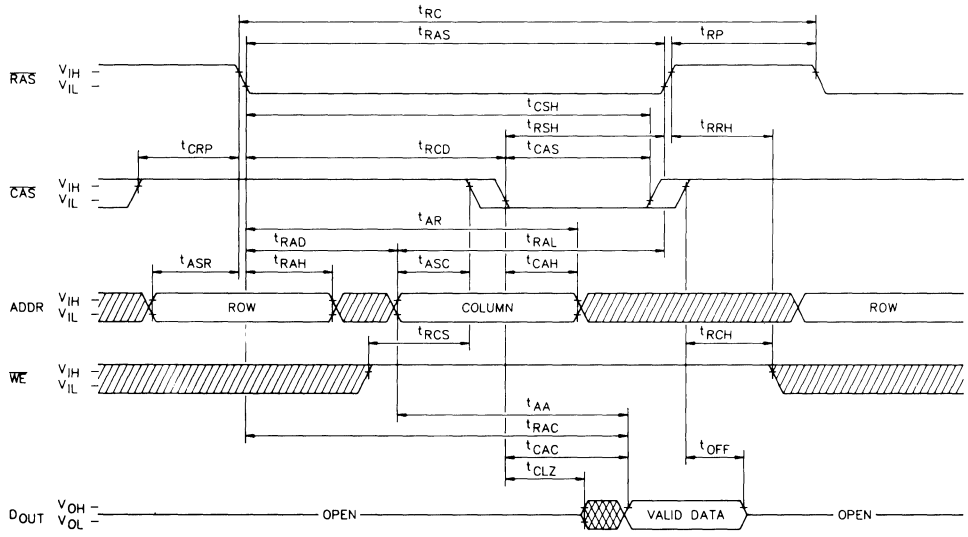
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	
Write command pulse width	^tWP	20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		110		135		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	50		60		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	25		30		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5

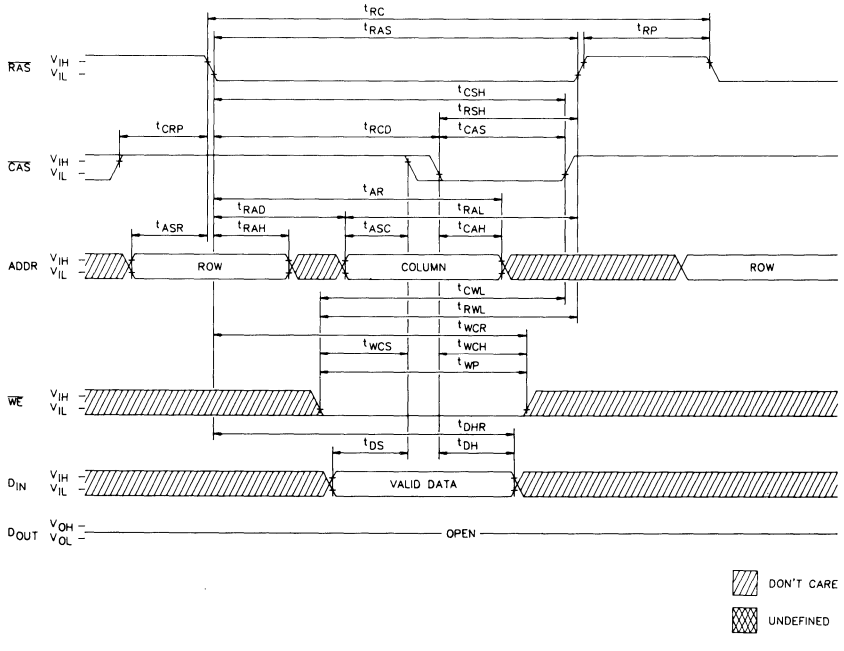
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

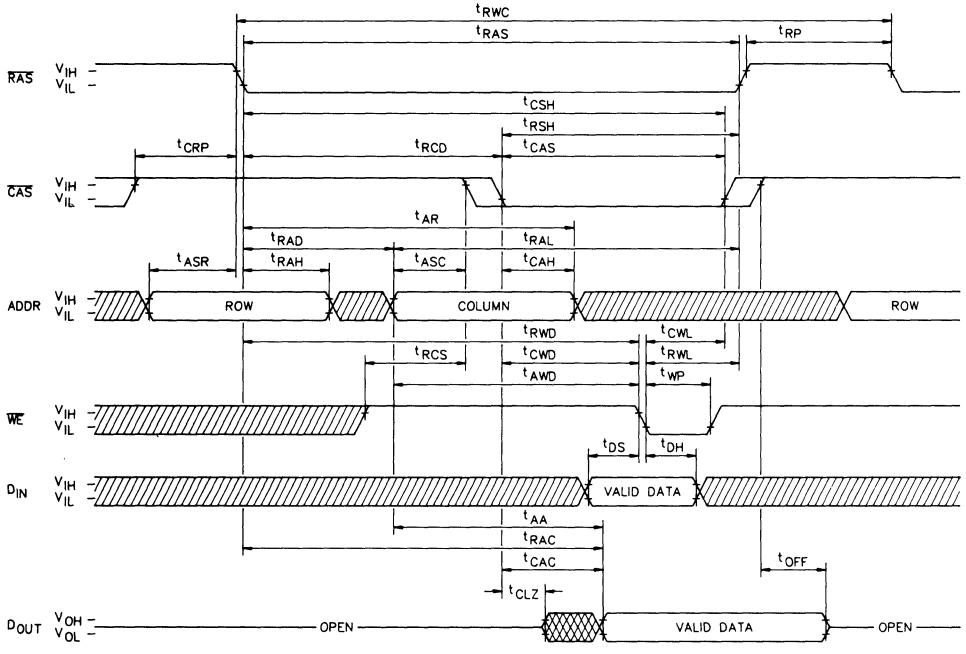
READ CYCLE



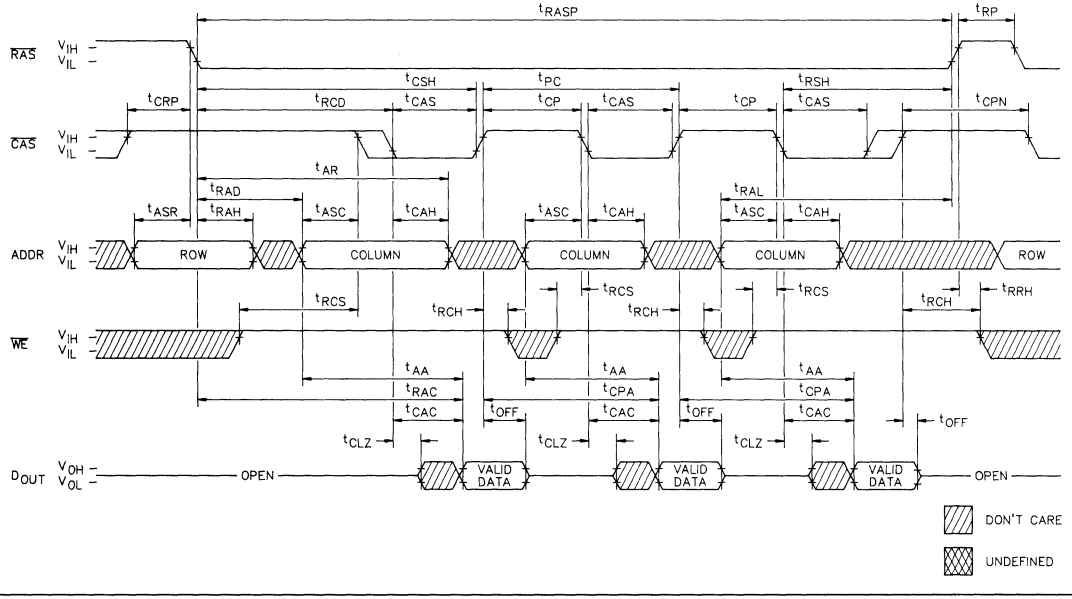
EARLY-WRITE CYCLE



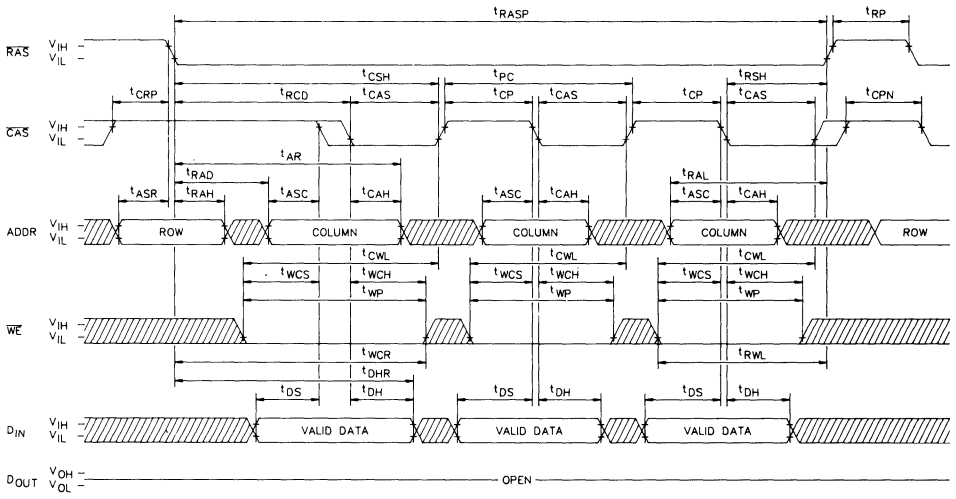
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



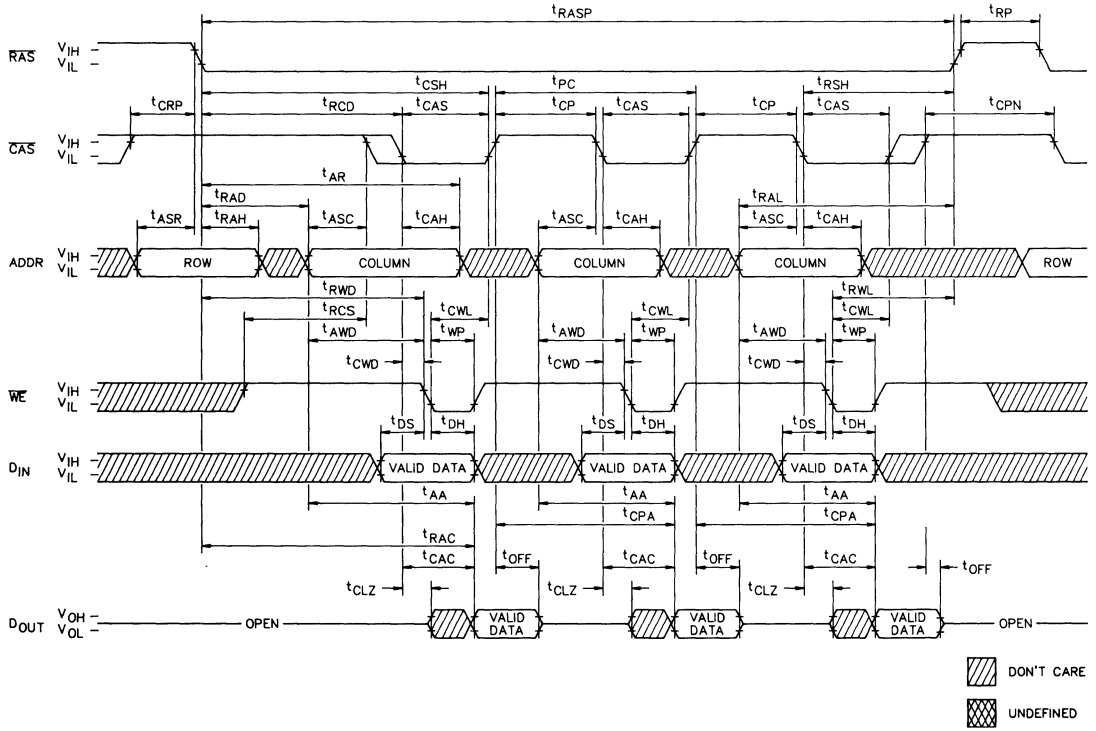
PAGE-MODE READ CYCLE



PAGE-MODE EARLY-WRITE CYCLE

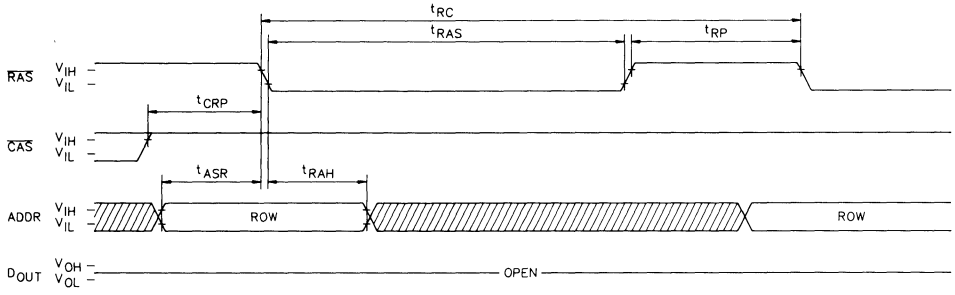


PAGE-MODE READ-WRITE CYCLE



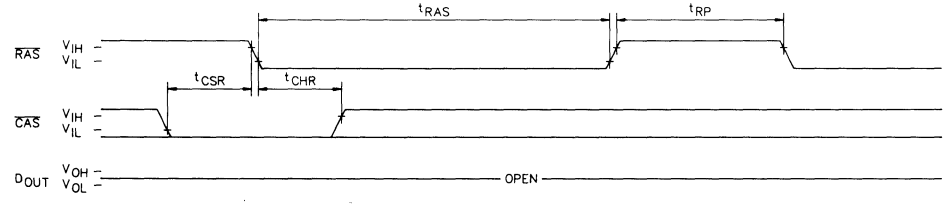
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



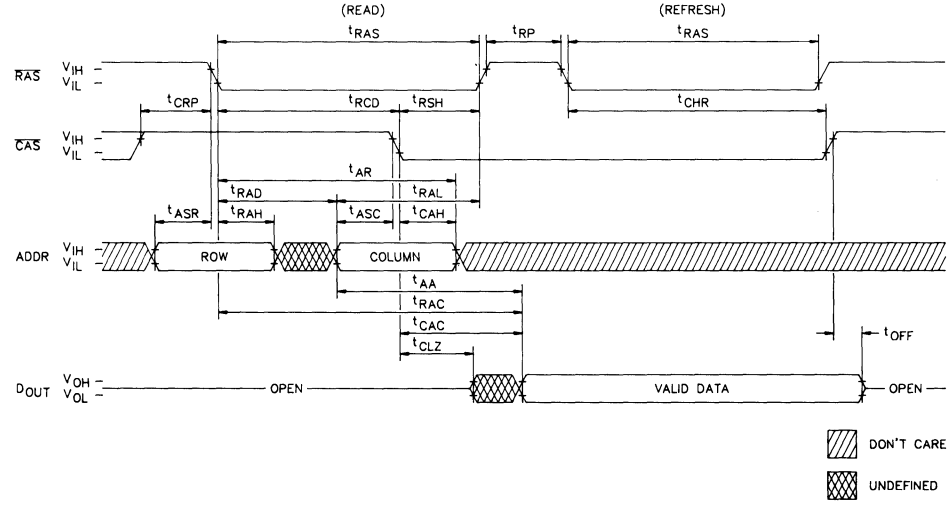
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



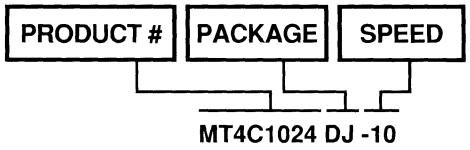
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

1 MEG x 1, 100ns in Plastic SOJ



The Micron 1 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM

1MEG x 1 DRAM

NIBBLE MODE

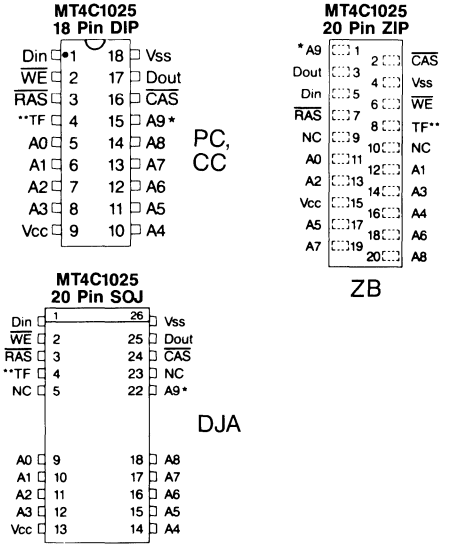
FEATURES

- Industry standard x1 pin-out, timing, functions and packages.
- High performance CMOS silicon gate process.
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- Optional Nibble Mode access cycle

OPTIONS / MARKING

• Timing	
100ns access	-10
120ns access	-12
150ns access	-15
• Organization	
1 MEG x 1	MT4C1025
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)



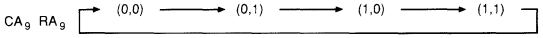
*Address not used for $\overline{RAS}$ only refresh
**TF = Test Function, ground of leave as a no-connect for normal device operation.

GENERAL DESCRIPTION

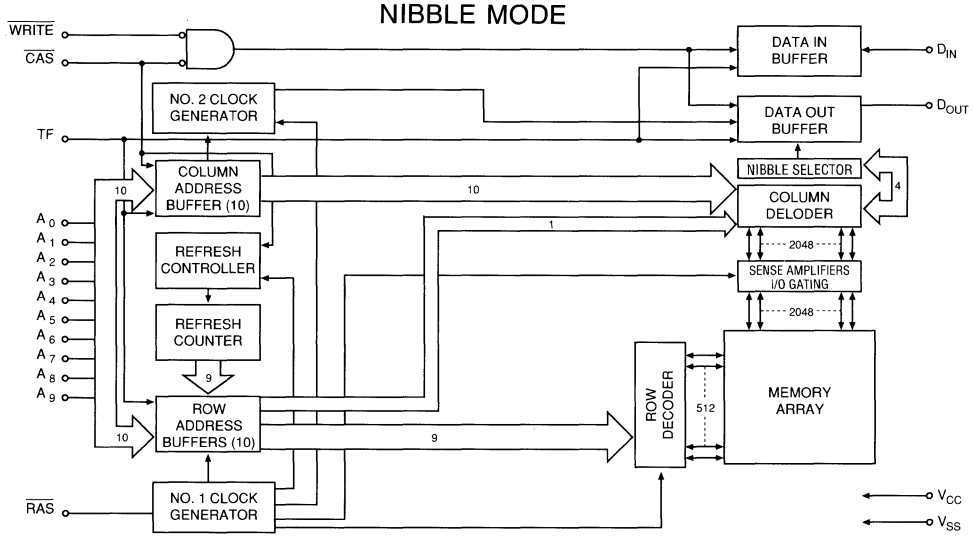
The MT4C1025 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

Nibble Mode operation allows faster sequential serial data operations (READ, WRITE or READ-MODIFY-WRITE) on up to 4 bits. The first of 4 bits is accessed in the usual manner with $\overline{CAS}$ address A9 (nibble MSB) and RAS address A9 (nibble LSB) selecting on of 4 bits within a nibble for initial access. By holding $\overline{RAS}$ low, $\overline{CAS}$ can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around (see below).



FUNCTIONAL BLOCK DIAGRAM
NIBBLE MODE



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	TF	Addresses tR	Addresses tC		NOTES
Standby	H	H	H	GND/NC	X	X	High Impedance	
READ	L	L	H	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
NIBBLE READ	L	H→L→H	H	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
NIBBLE WRITE	L	H→L→H	L	GND/NC	ROW	COL	Valid Data In, Valid Data In	
NIBBLE READ-WRITE	L	H→L→H	H→L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	GND/NC	X	X	High Impedance	
TEST FUNCTION	L	L	H	H	ROW	COL	Data Out, Test Funtion Mode	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$ = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		50	mA	3, 4
OPERATING CURRENT: NIBBLE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		4	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		1	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		35	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		35	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9), D_{IN}	C_{I1}		5	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance D_{OUT}	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	190		220		260		ns	
READ-MODIFY-WRITE cycle time	t_{RWC}	220		255		295		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	14
Access time from $\overline{CAS}$	t_{CAC}		25		30		45	ns	15
Access time from column address	t_{AA}		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		65		75	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	80		90		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{CAS}$ precharge time	t_{CPN}	15		20		25		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	10	75	15	90	15	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	10	50	15	60	15	70	ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	50		60		70		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	5		5		5		ns	
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	30	ns	20
$\overline{WE}$ command set-up time	t_{WCS}	0		0		0		ns	21
Write command hold time	t_{WCH}	20		25		30		ns	
Write command hold time (referenced to $\overline{RAS}$)	t_{WCR}	70		80		90		ns	
Write command pulse width	t_{WP}	20		25		30		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

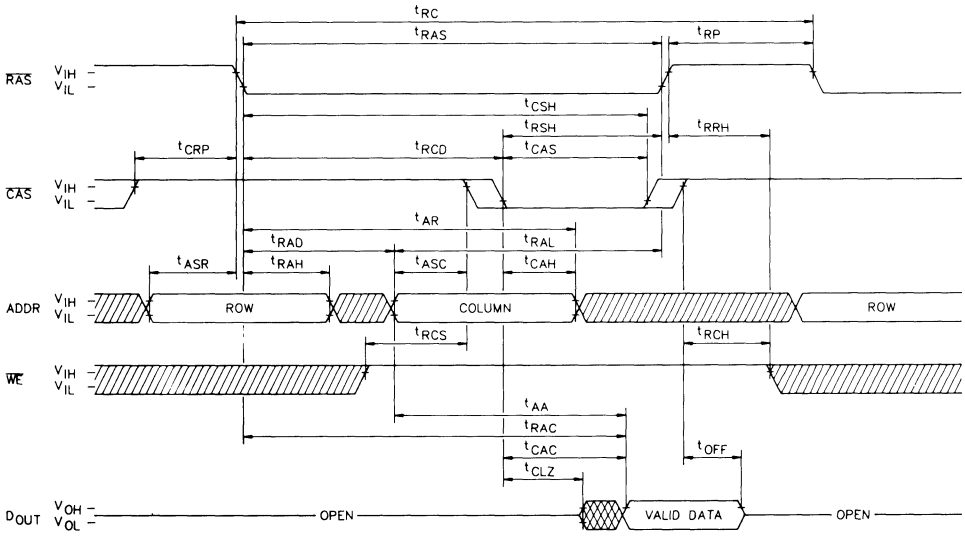
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		110		135		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	50		60		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	35		40		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5
$\overline{RAS}$ pulse width (NIBBLE MODE)	^tRASN	100	100,000	120	100,000	150	100,000	ns	
$\overline{CAS}$ precharge time (NIBBLE MODE)	^tNCP	10		15		20		ns	
NIBBLE MODE cycle time	^tNC	35		40		45		ns	
NIBBLE MODE READ-MODIFY-WRITE cycle time	^tNRWC	55		65		75		ns	
NIBBLE MODE access time	^tNCAC	15		20		25		ns	15
NIBBLE MODE pulse width	^tNCAS	15		20		25		ns	
NIBBLE MODE $\overline{CAS}$ precharge time	^tNCP	10		10		10		ns	
NIBBLE MODE $\overline{RAS}$ hold time	^tNRSH	15		20		25		ns	
NIBBLE MODE $\overline{CAS}$ to $\overline{WRITE}$ delay time	^tNCWD	15		20		25		ns	
NIBBLE MODE $\overline{WRITE}$ command to $\overline{RAS}$ lead time	^tNRWL	15		20		25		ns	
NIBBLE MODE $\overline{WRITE}$ command to $\overline{CAS}$ lead time	^tNCWL	15		20		25		ns	

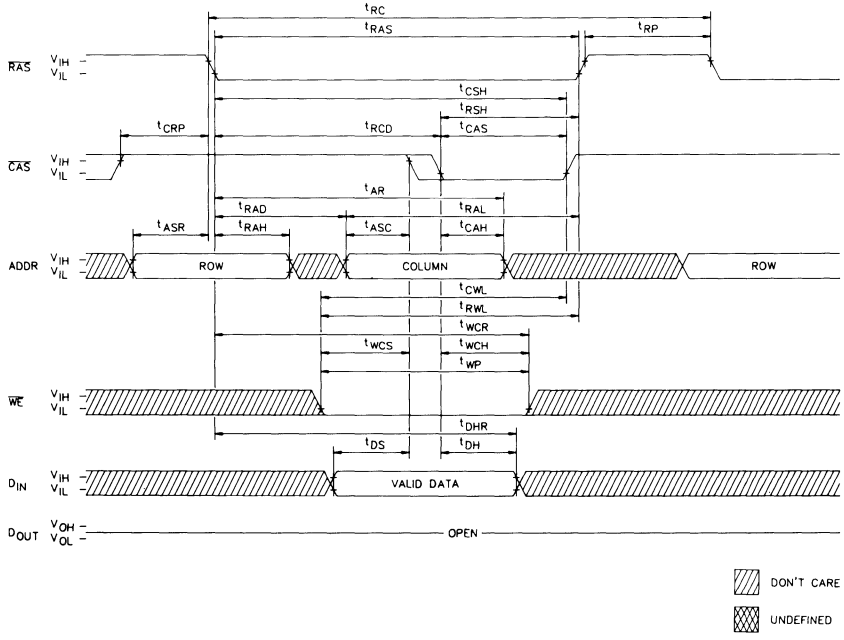
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (min), $^tAWD \geq {}^tAWD$ (min) and $^tCWD \geq {}^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

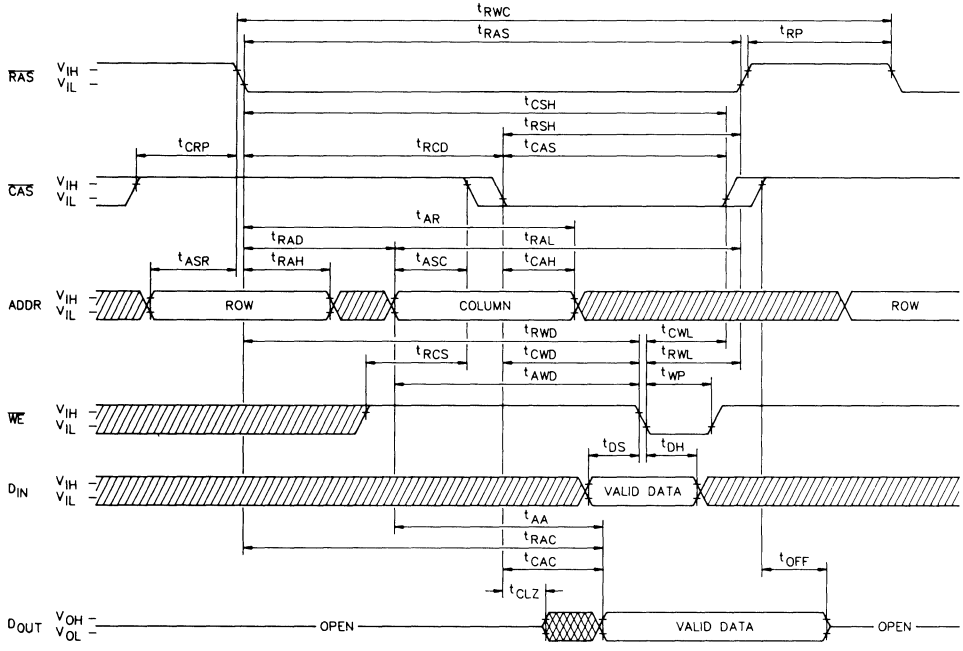
READ CYCLE



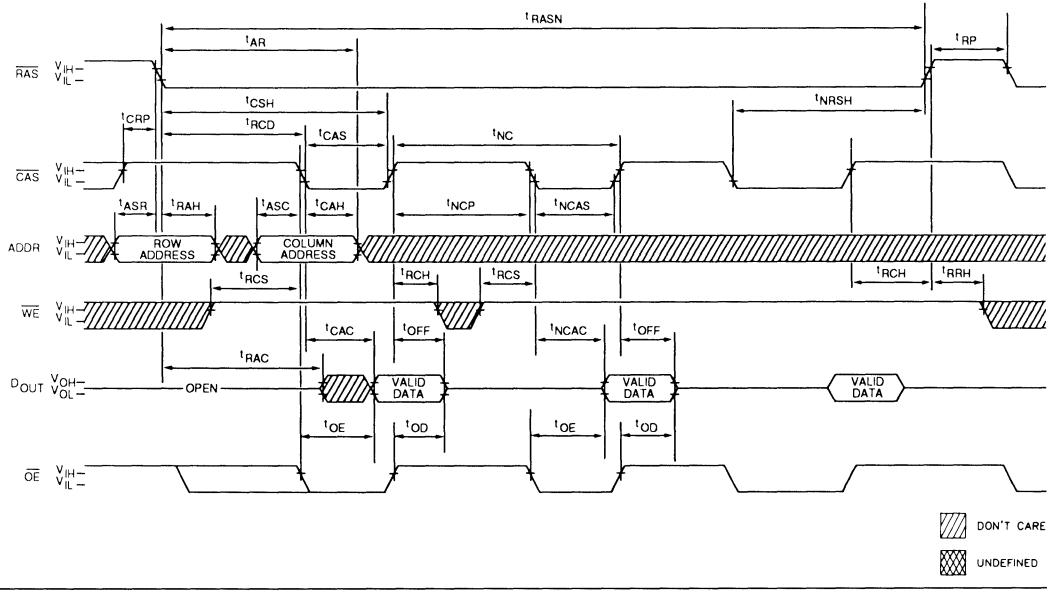
EARLY-WRITE CYCLE



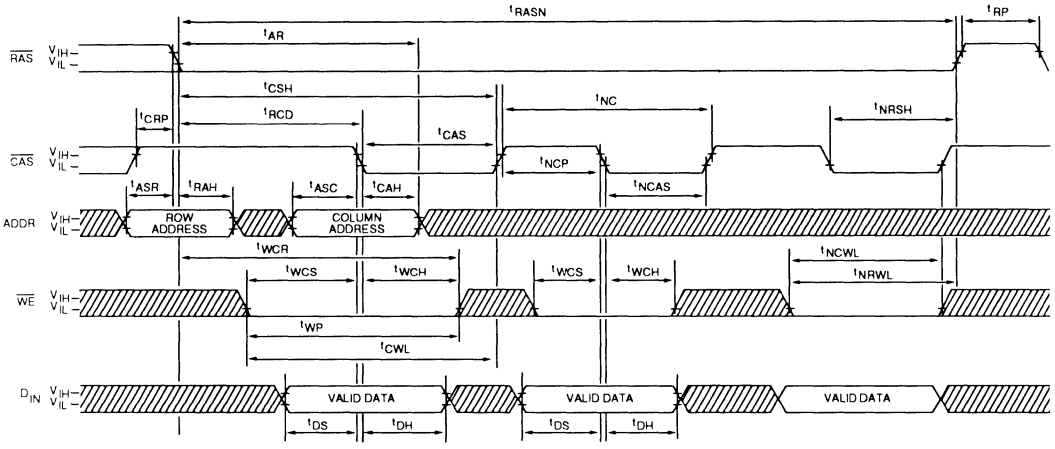
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



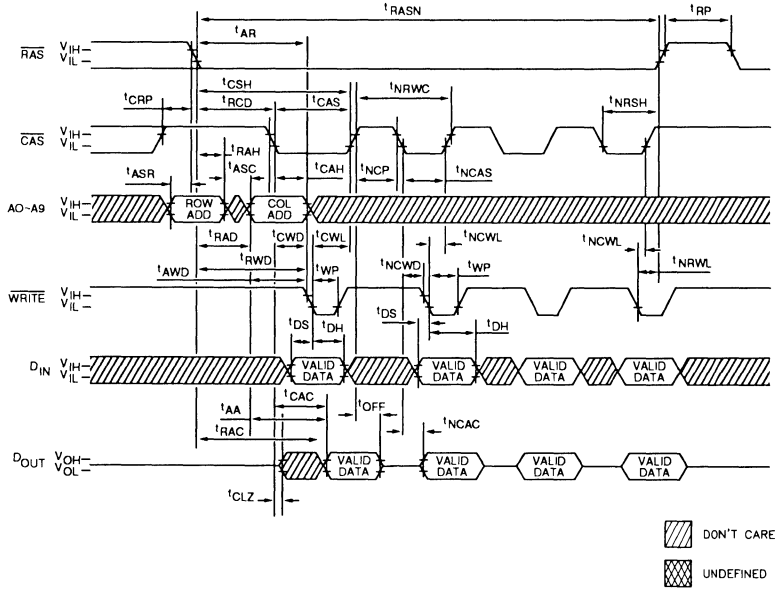
NIBBLE MODE READ CYCLE



NIBBLE MODE EARLY-WRITE CYCLE

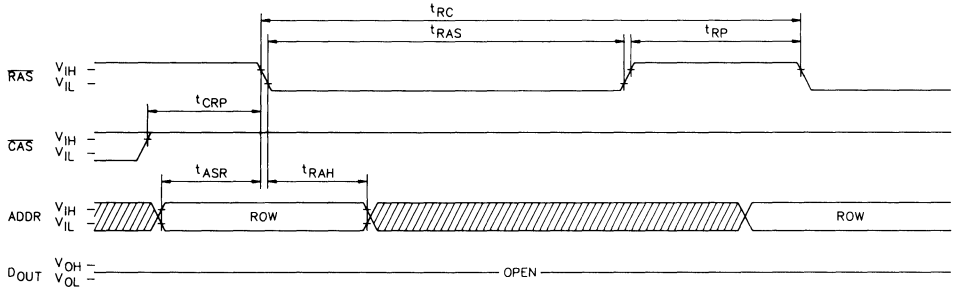


NIBBLE MODE READ-WRITE CYCLE



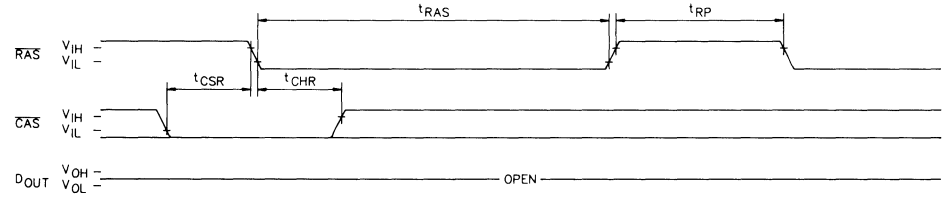
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



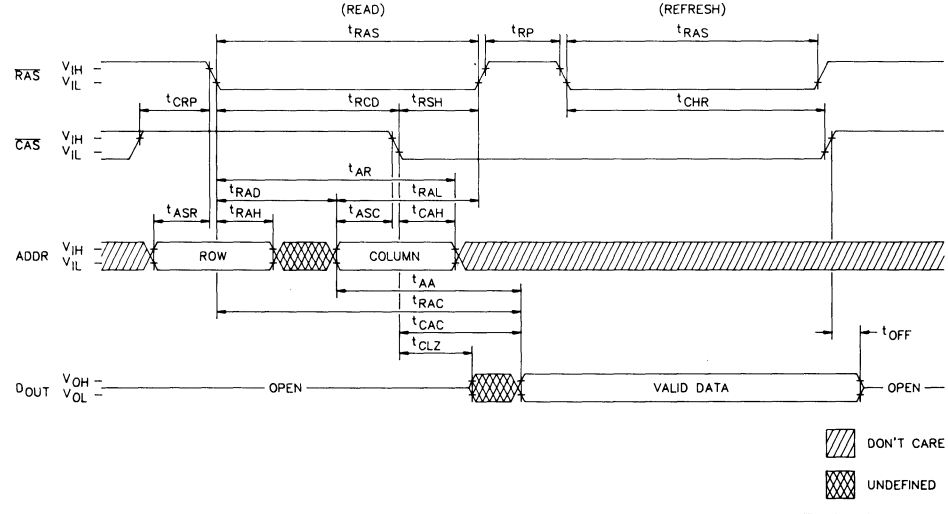
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



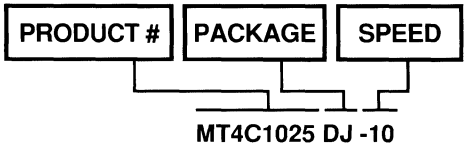
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

1 MEG x 1, 100ns in Plastic SOJ



The Micron 1 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM

1MEG x 1 DRAM

STATIC COLUMN

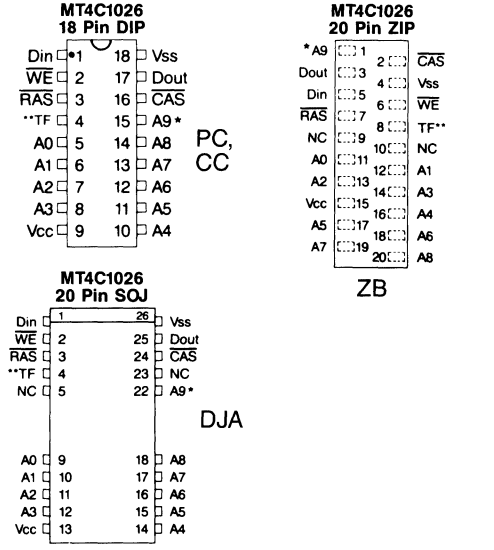
FEATURES

- Industry standard x1 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- Optional Static Column access cycle

OPTIONS

	MARKING
• Timing	
100ns access	-10
120ns access	-12
150ns access	-15
• Organization	
1 MEG x 1	MT4C1026
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)



*Address not used for $\overline{RAS}$ only refresh
**TF = Test Function, ground of leave as a no-connect for normal device operation.

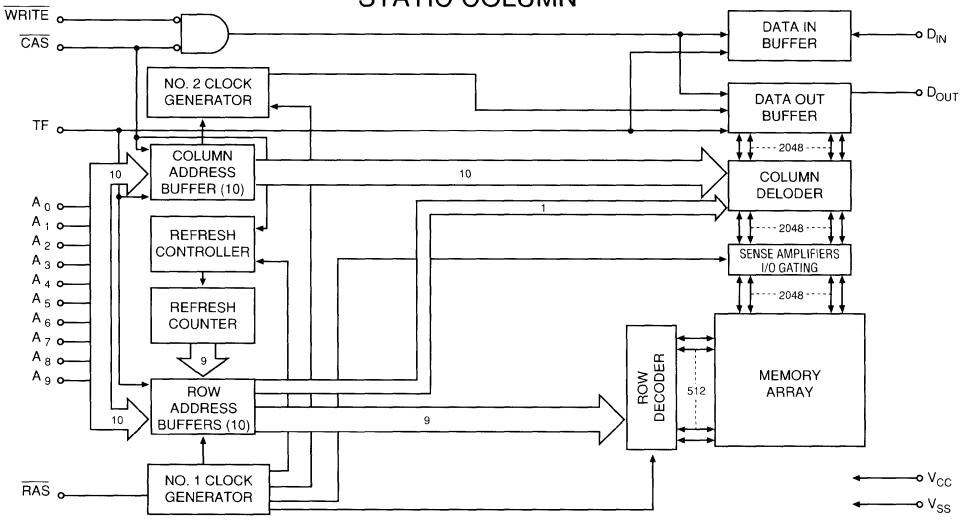
GENERAL DESCRIPTION

The MT4C1026 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0 -A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0 -A8) are executed at least every 8ms, regardless of sequence.

STATIC COLUMN operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0 -A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the STATIC COLUMN operation.

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	TF	Addresses tR	Addresses tC		NOTES
Standby	H	H	H	GND/NC	X	X	High Impedance	
READ	L	L	H	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
STATIC COLUMN READ	L	L	H	GND/NC	ROW	COL→COL	Valid Data Out, Valid Data Out	
STATIC COLUMN WRITE	L	L	L	GND/NC	ROW	COL→COL	Valid Data In, Valid Data Out	
STATIC COLUMN READ-WRITE	L	L	H→L→H	GND/NC	ROW	COL→COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	GND/NC	X	X	High Impedance	
TEST FUNCTION	L	L	H	H	ROW	COL	Data Out, Test Funtion Mode	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$ = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		50	mA	3, 4
OPERATING CURRENT: STATIC COLUMN ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = V_{IL}, Addr. = Cycling, t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		1	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		35	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		35	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9), D_{IN}	C_{I1}		5	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance D_{OUT}	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	190		220		260		ns	
READ-MODIFY-WRITE cycle time	t_{RWC}	220		255		295		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	14
Access time from $\overline{CAS}$	t_{CAC}		25		30		45	ns	15
Access time from column address	t_{AA}		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		65		75	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	80		90		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{CAS}$ precharge time	t_{CPN}	15		20		25		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	10	75	15	90	15	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	10	50	15	60	15	70	ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	50		60		70		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	5		5		5		ns	
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	30	ns	20
$\overline{WE}$ command set-up time	t_{WCS}	0		0		0		ns	21
Write command hold time	t_{WCH}	20		25		30		ns	
Write command hold time (referenced to $\overline{RAS}$)	t_{WCR}	70		80		90		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

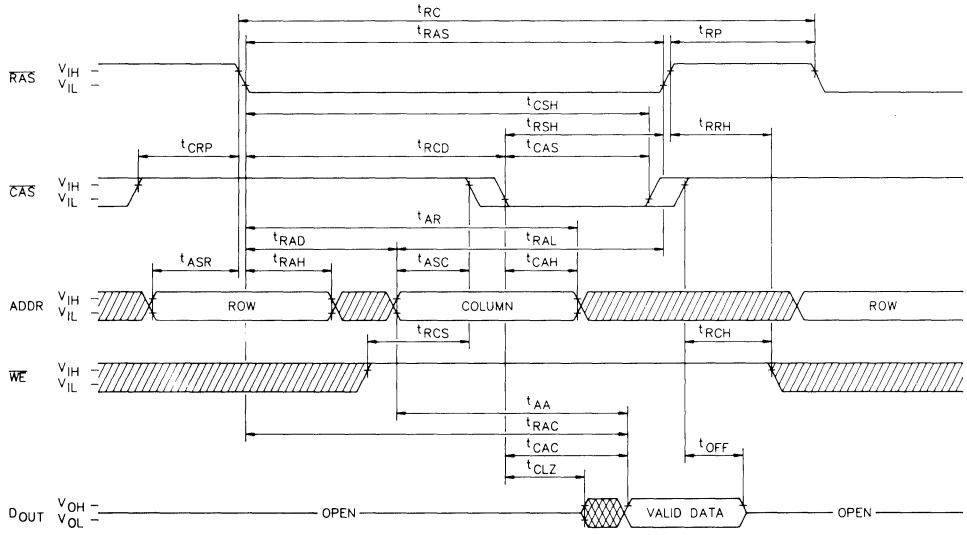
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command pulse width	^tWP	20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		110		135		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	50		60		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	25		30		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	100	100,000	120	100,000	150	100,000	ns	
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		15		20		ns	
STATIC COLUMN MODE cycle time	^tSC	55		65		75		ns	
STATIC COLUMN READ-MODIFY-WRITE cycle time	^tSRMW	135		160		185		ns	
Last Write to column address delay time	^tLWAD	25	45	30	55	45	70	ns	
Last Write to column address hold time	^tAHLW		95		115		135	ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	^tROH	20		20		20		ns	
Output data hold time from column address	^tAOH	5	—	5	—	5	—	ns	
Output data enable from Write	^tOW	—	25	—	25	—	25	ns	

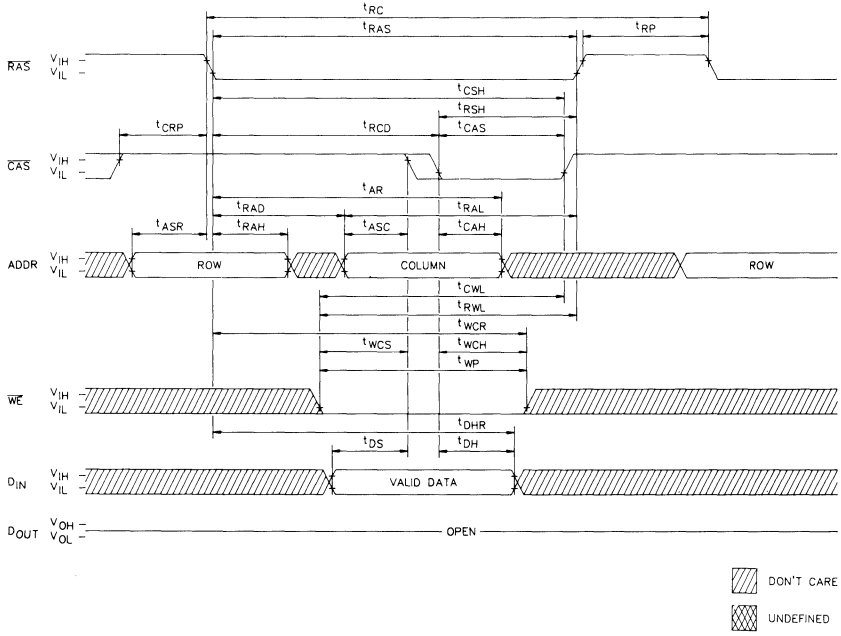
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

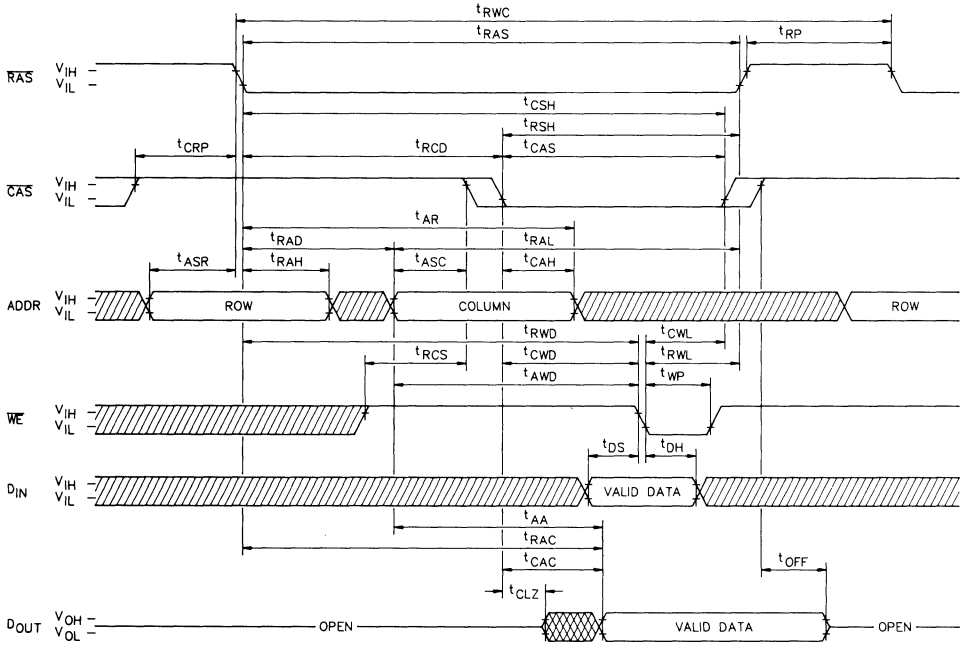
READ CYCLE



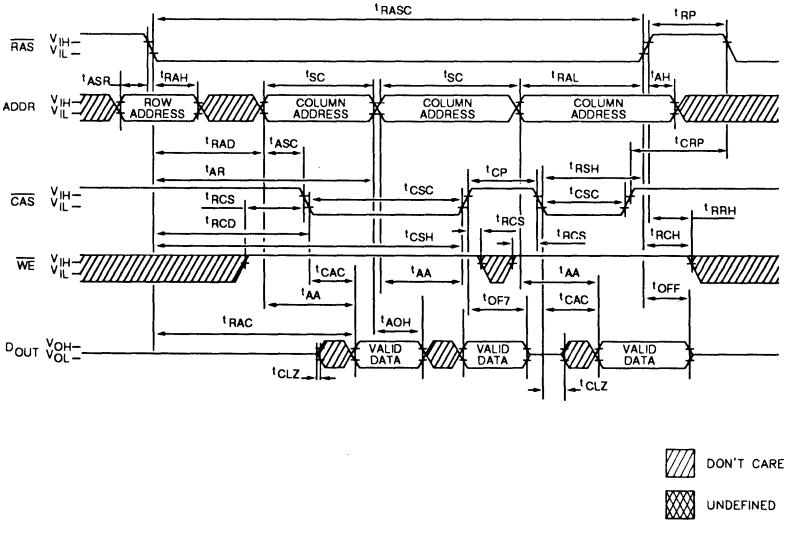
EARLY-WRITE CYCLE



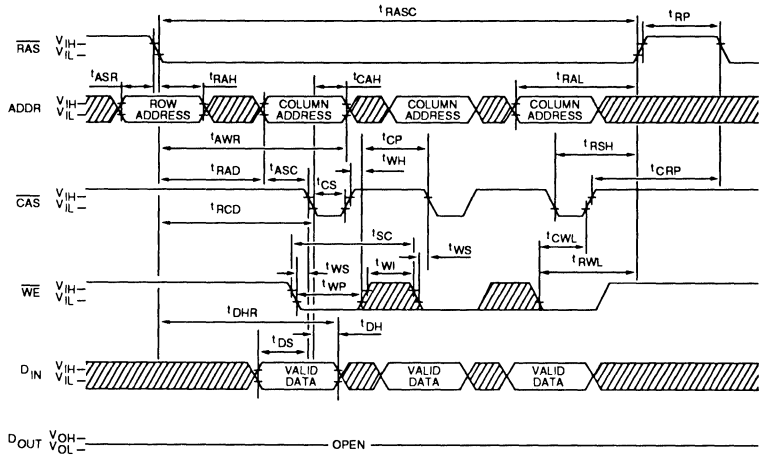
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



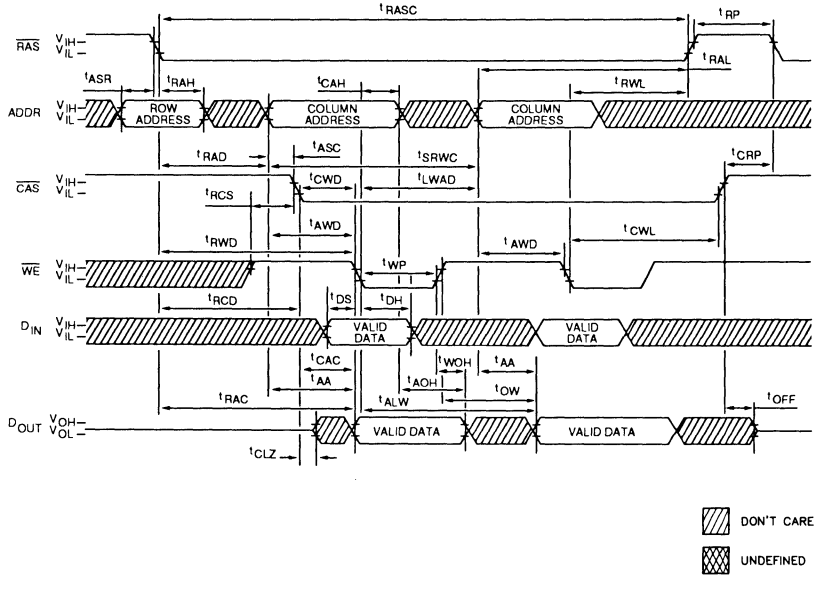
STATIC COLUMN READ CYCLE



STATIC COLUMN EARLY-WRITE CYCLE

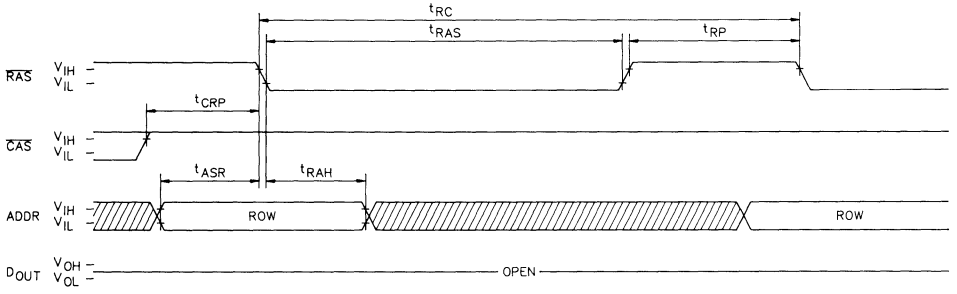


STATIC COLUMN READ-WRITE CYCLE



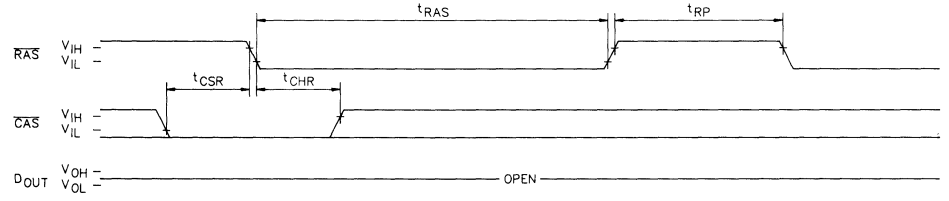
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



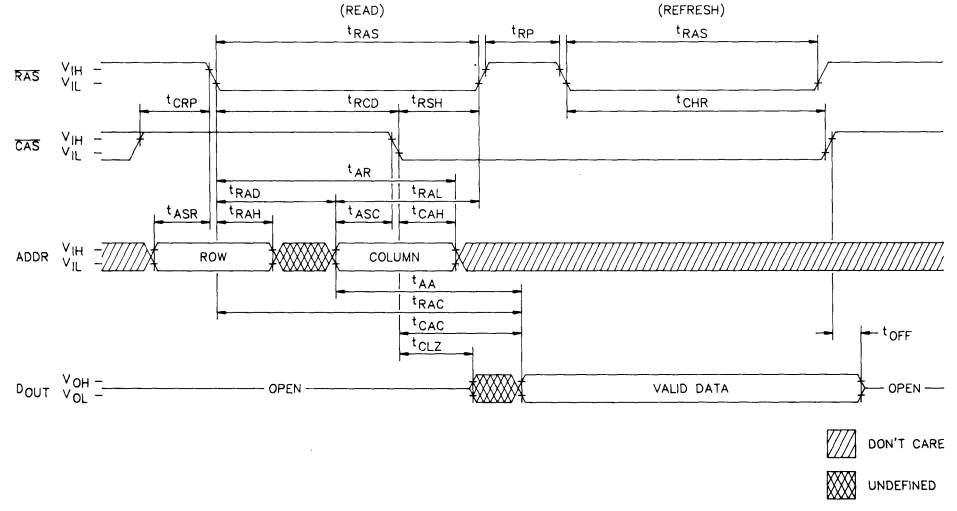
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



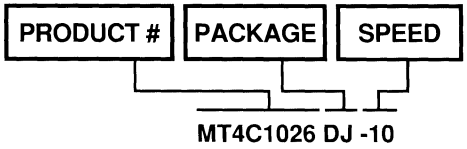
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

1 MEG x 1, 100ns in Plastic SOJ



The Micron 1 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM

1MEG x 4 DRAM

FAST PAGE MODE

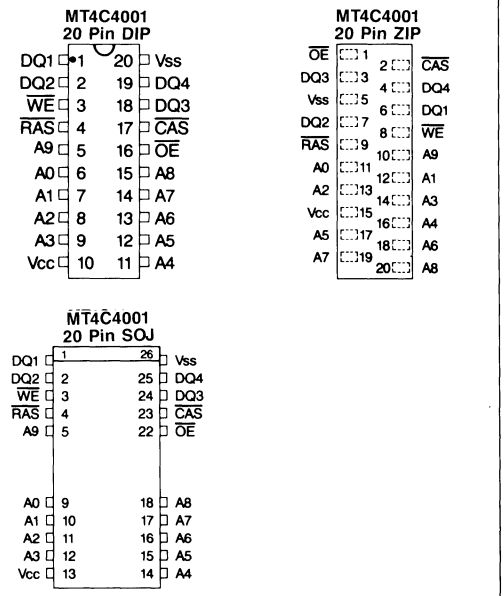
FEATURES

- Industry standard x4 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024 cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- Optional Fast Page Mode access cycle

OPTIONS

	MARKING
• Timing	
80ns access	-8
100ns access	-10
120ns access	-12
• Organization	
1 MEG x 4	MT4C4001
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)



NOTE: Package Information To Be Determined.

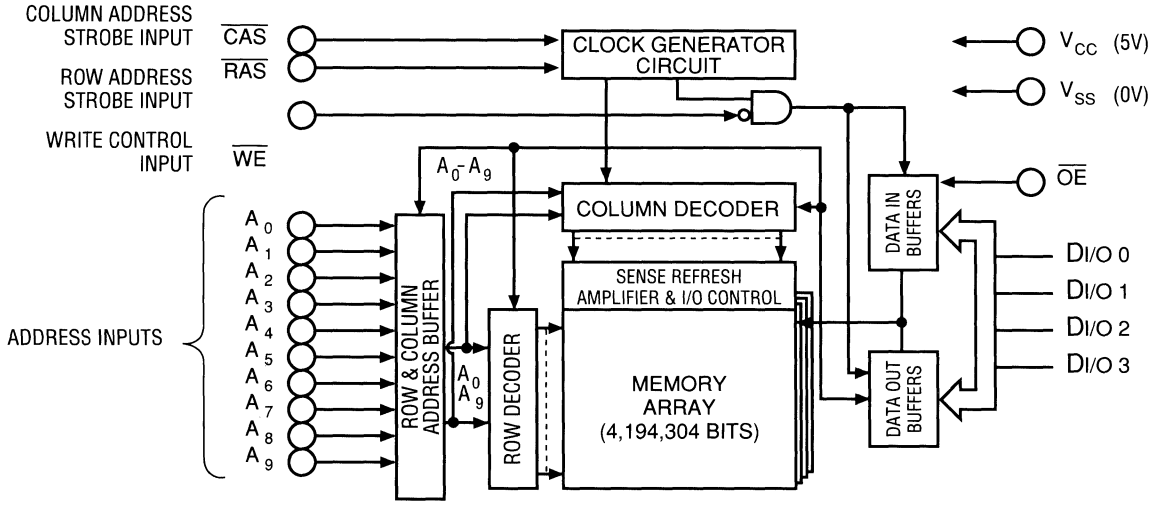
GENERAL DESCRIPTION

The MT4C4001 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	Addresses tR	Addresses tC		NOTES
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
PAGE MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$, = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: $t_{RC} = t_{RC(MIN)}$)	I_{CC1}		60	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: $t_{PC} = t_{PC(MIN)}$)	I_{CC2}		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		0.5	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		60	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		60	mA	3, 5
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DRAM

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9), D_{IN}	C_{I1}		5	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Output Capacitance D_{OUT}	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	160		190		220		ns	
READ-MODIFY-WRITE cycle time	t_{RWC}	185		220		295		ns	
PAGE-MODE READ or WRITE cycle time	t_{PC}	50		55		70		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		25		35	ns	15
Output Enable	t_{OE}		25		25		30	ns	
Access time from column address	t_{AA}		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		50		65	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	t_{RASP}	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		35		ns	
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		15		20		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	t_{CP}	10	25	10	25	15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	10	60	10	75	25	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	10	40	10	50	15		ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		60		90		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		50		60		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	5		5		5		ns	
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	25	ns	20
Output Disable	t_{OD}		25		25	30	25	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

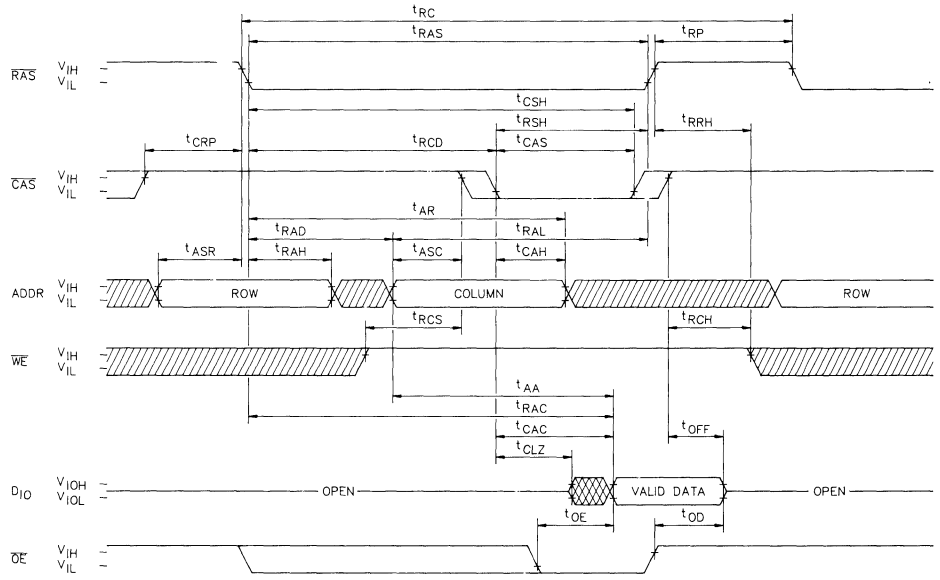
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
FAST PAGE MODE READ-MODIFY-WRITE cycle time	^tPRWC	75		90		140		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		70		90		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		70		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		120		160		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		80		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		65		75		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		15		ns	5

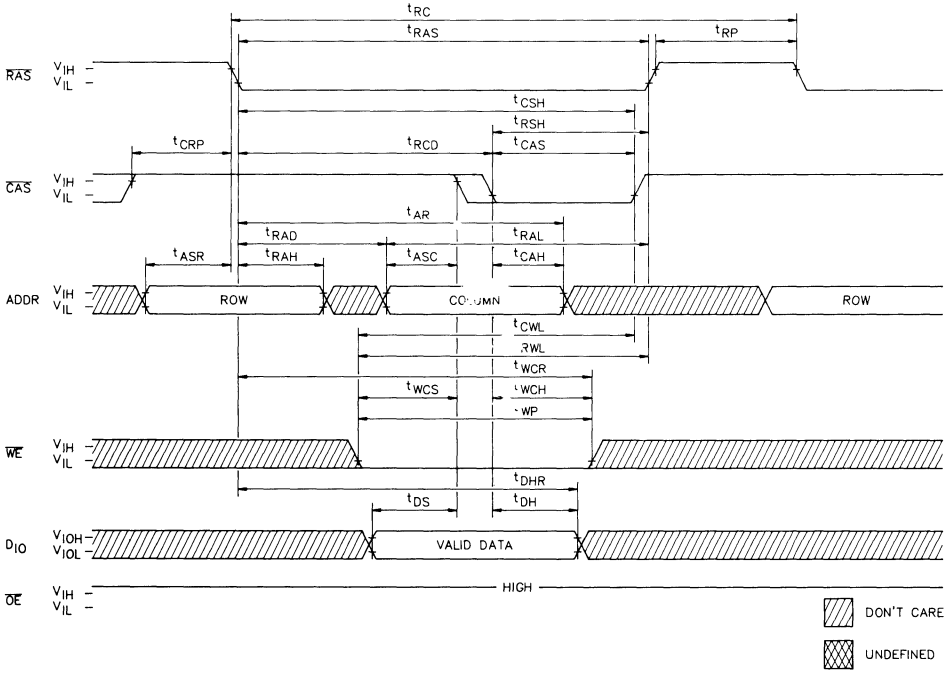
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (min), $^tAWD \geq {}^tAWD$ (min) and $^tCWD \geq {}^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH D_{OUT} goes open. If $\overline{OE}$ is tied permanently low a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.

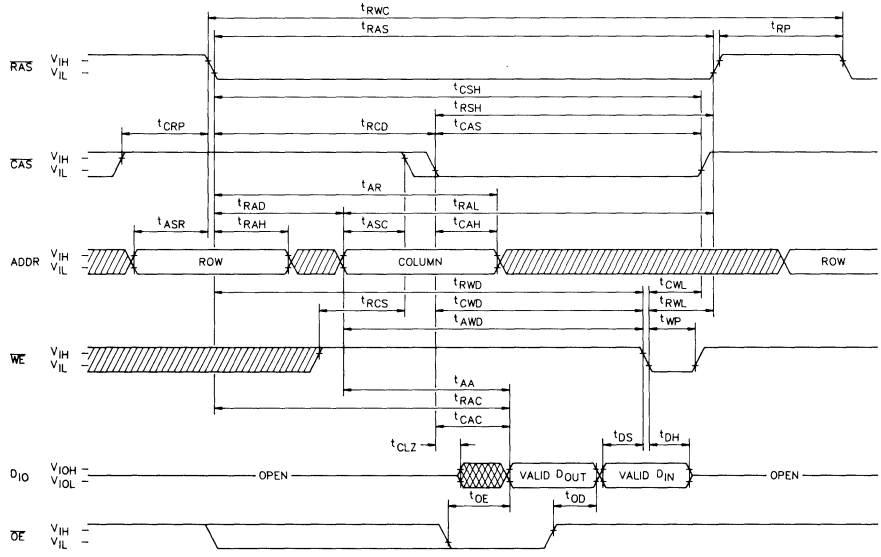
READ CYCLE



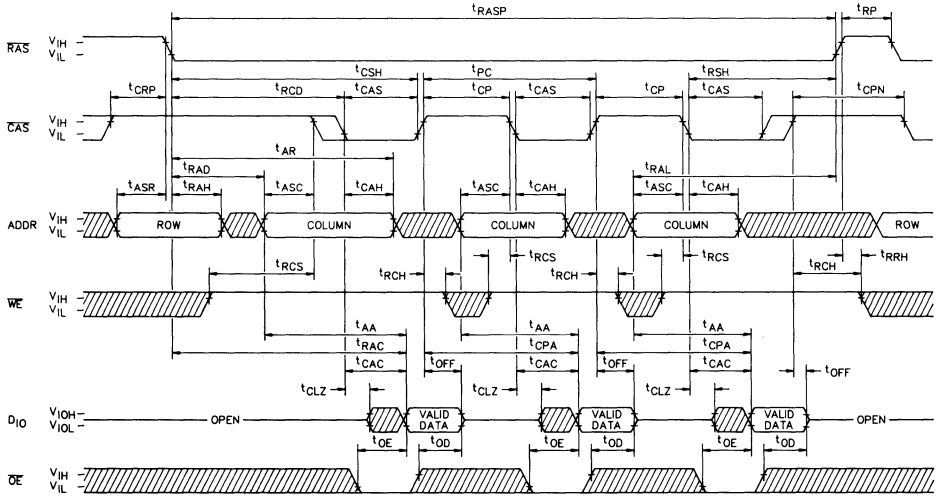
EARLY-WRITE CYCLE



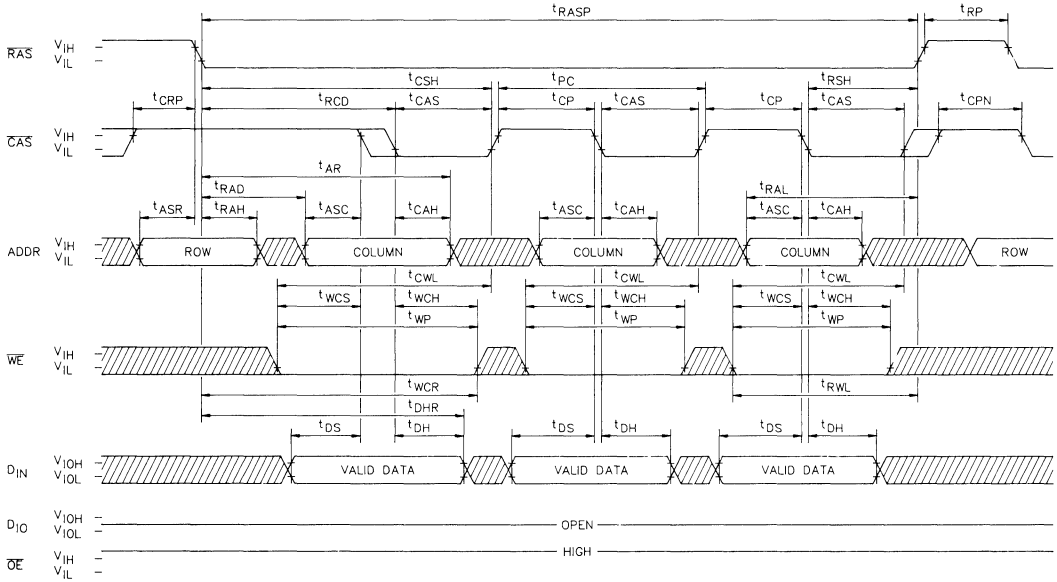
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



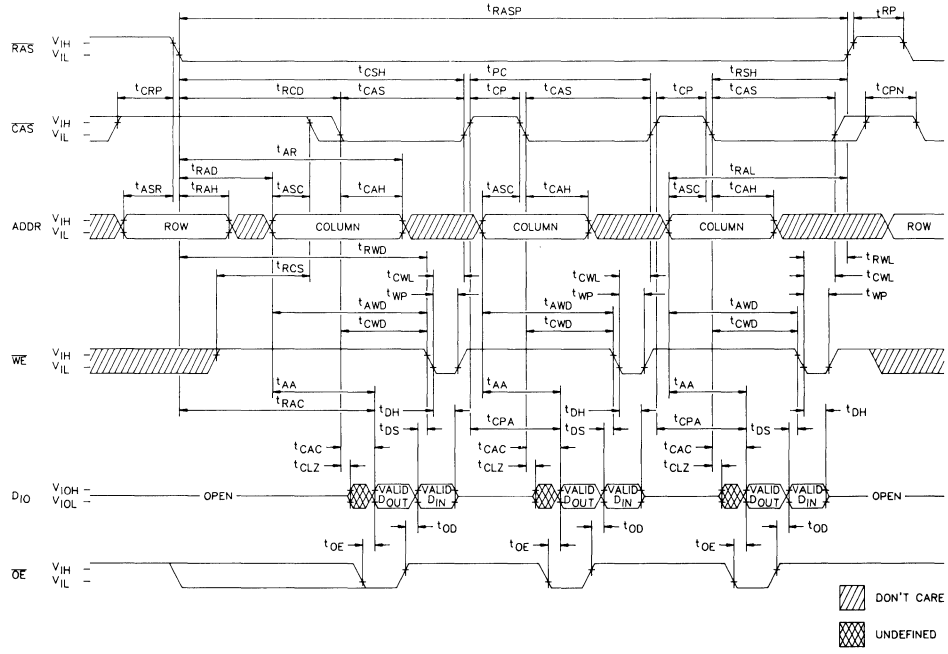
PAGE-MODE READ CYCLE



PAGE-MODE EARLY-WRITE CYCLE

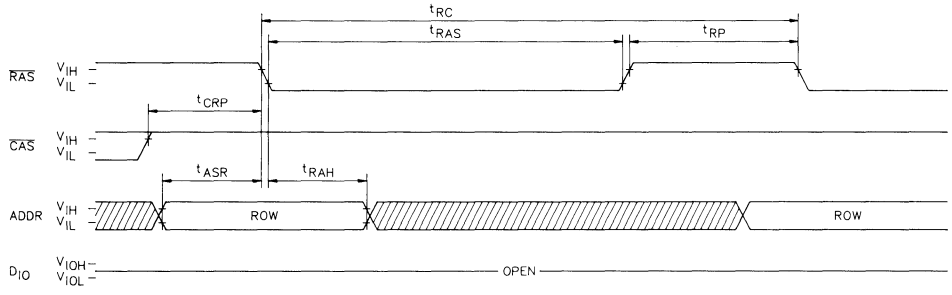


PAGE-MODE READ-WRITE CYCLE



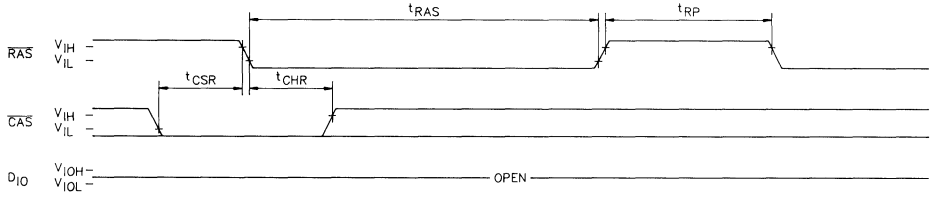
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



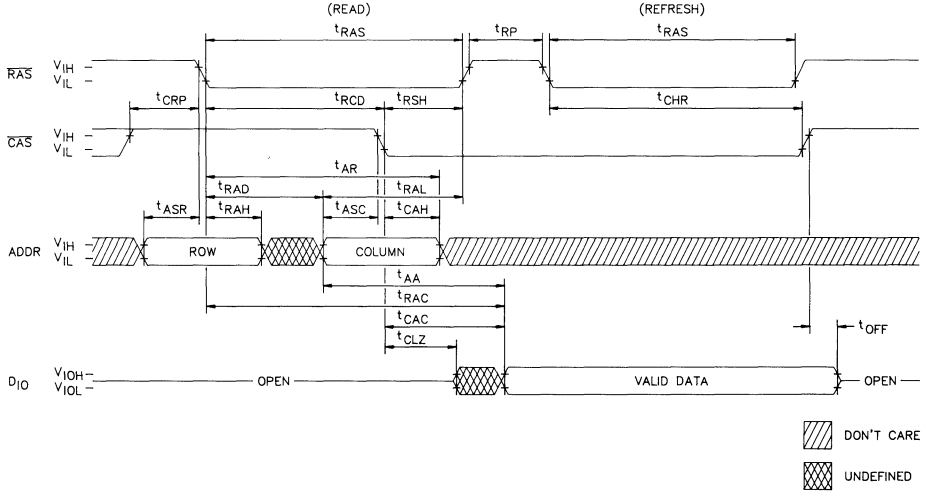
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



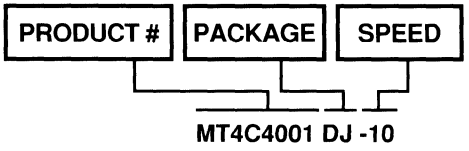
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH); $\overline{OE}$=LOW)[24]



ORDER INFORMATION

1MEG x 4, 100ns in Plastic DJ



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DRAM

1MEG x 4 DRAM

STATIC COLUMN

FEATURES

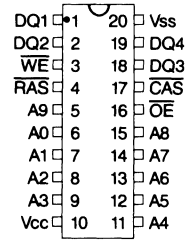
- Industry standard x4 pin-out, timing, functions and packages.
- High performance CMOS silicon gate process.
- Single +5V±10% power supply.
- Low power, 5mW standby, 175mW active, typical.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- 1024 cycle refresh distributed across 16ms.
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden.
- Optional Static Column access cycle.

OPTIONS MARKING

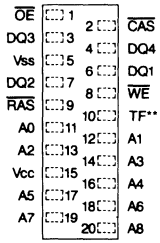
- Timing
  - 80ns access -8
  - 100ns access -10
  - 120ns access -12
- Organization
  - 1 MEG x 4 MT4C4003
- Packages
  - Plastic DIP None
  - Ceramic DIP C
  - Plastic ZIP Z
  - Plastic SOJ DJ

PIN ASSIGNMENT (Top View)

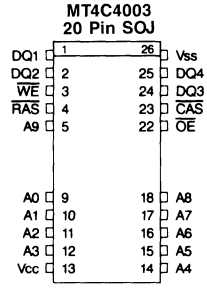
MT4C4003
20 Pin DIP



MT4C4003
20 Pin ZIP



MT4C4003
20 Pin SOJ



NOTE: Package Information To Be Determined.

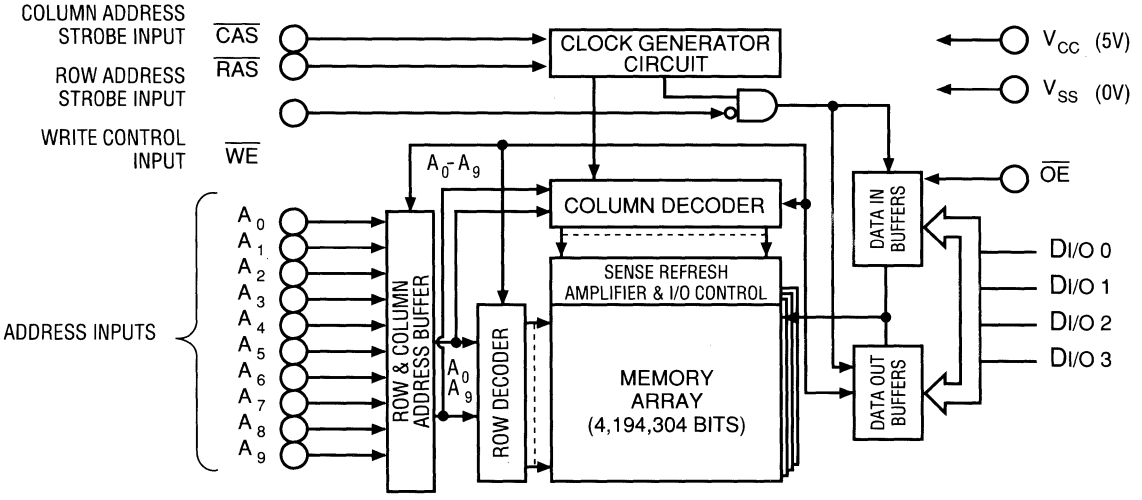
GENERAL DESCRIPTION

The MT4C4003 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 8ms, regardless of sequence.

The STATIC COLUMN cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the STATIC COLUMN operation.

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	Addresses tR	Addresses tC		NOTES
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
STATIC COLUMN READ	L	L	H	ROW	COL COL	Valid Data Out Valid Data Out	
STATIC COLUMN WRITE	L	L	L	ROW	COL COL	Valid Data In Valid Data In	
STATIC COLUMN READ-WRITE	L	L	H→L→H	ROW	COL COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C, = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		60	mA	3, 4
OPERATING CURRENT: FAST STATIC COLUMN ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		0.5	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		60	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		60	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9), D_{IN}	C_{I1}		5	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Output Capacitance D_{OUT}	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	160		190		220		ns	
READ-MODIFY-WRITE cycle time	^tRWC	185		220		295		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		35	ns	15
Output Enable	^tOE		25		25		35	ns	
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		50		60	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		35		ns	
$\overline{RAS}$ precharge time	^tRP	70		80		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	10		15		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	60	10	75	15	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	10	40	10	50	15	45	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		60		140		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	5		5		5		ns	
Output buffer turn-off delay	^tOFF	0	25	0	25	0	35	ns	20
Output Disable	^tOD		25		25		30	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

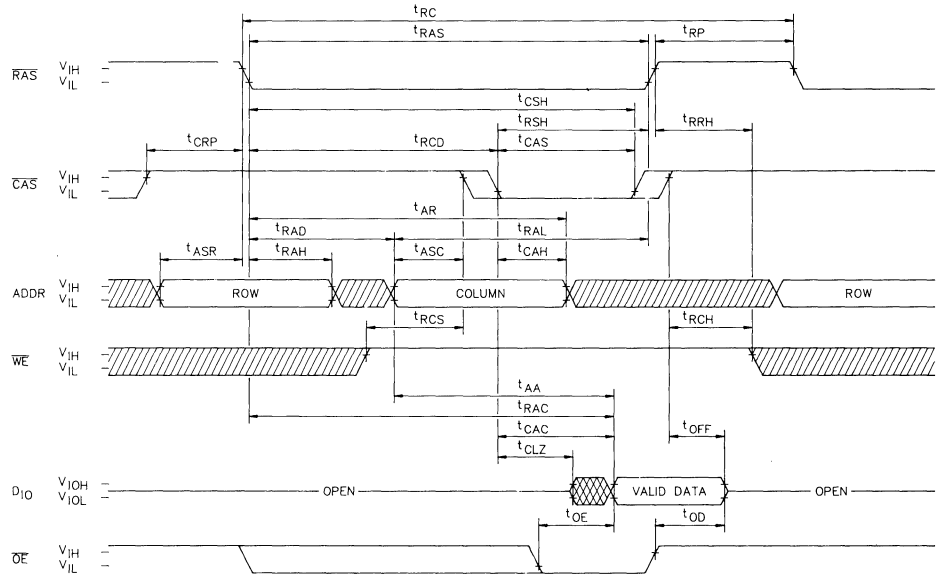
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		70		90		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		70		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		120		160		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		80		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		65		75		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		15		ns	5
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	80	100,000	100	100,000	120	100,000	ns	
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10	25	10	25	15	30	ns	
STATIC COLUMN MODE cycle time	^tSC	55		65		55		ns	
STATIC COLUMN READ-MODIFY-WRITE cycle time	^tSRMW	135		160		160		ns	
Last write to column address delay time	^tLWAD	25	45	30	55	30	55	ns	
Last write to column address hold time	^tAHLW		95		115	115		ns	
$\overline{RAS}$ hold time precharged to $\overline{OE}$	^tROH	20		20		20		ns	
Output data hold time from column address	^tAOH	5	—	5	—	5	—	ns	
Output data enable from write	^tOW	—	30	—	35	—	40	ns	
$\overline{OE}$ to data delay	^tOED	25		30		30		ns	
$\overline{OE}$ command hold time	^tOEH	25		25		30		ns	
Access time from last Write	^tALW		95		115		115	ns	

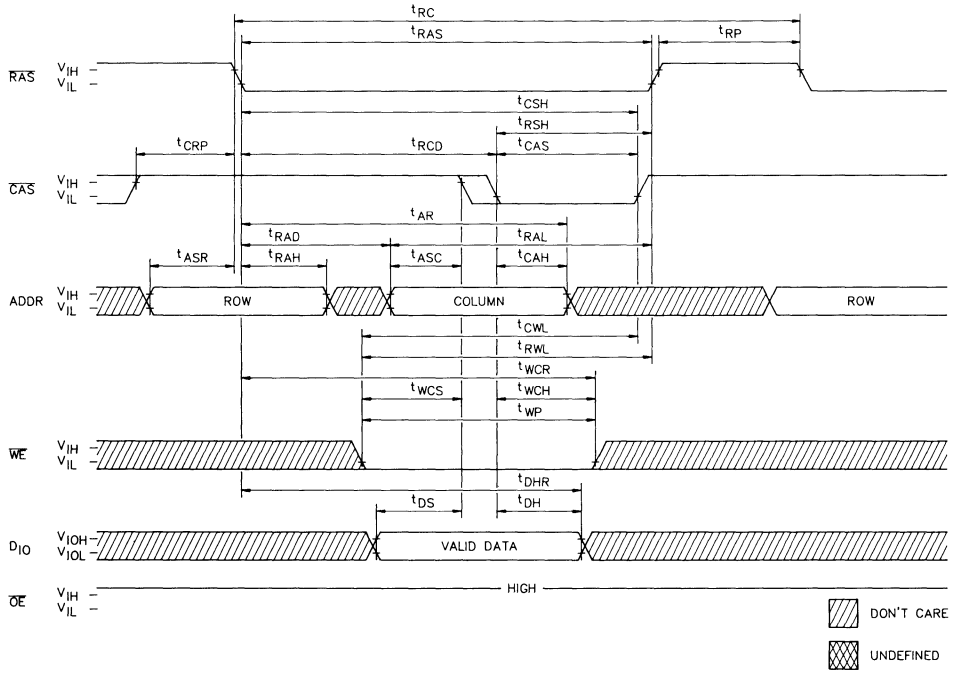
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (min), $^tAWD \geq ^tAWD$ (min) and $^tCWD \geq ^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH D_{OUT} goes open. If $\overline{OE}$ is tied permanently low a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.

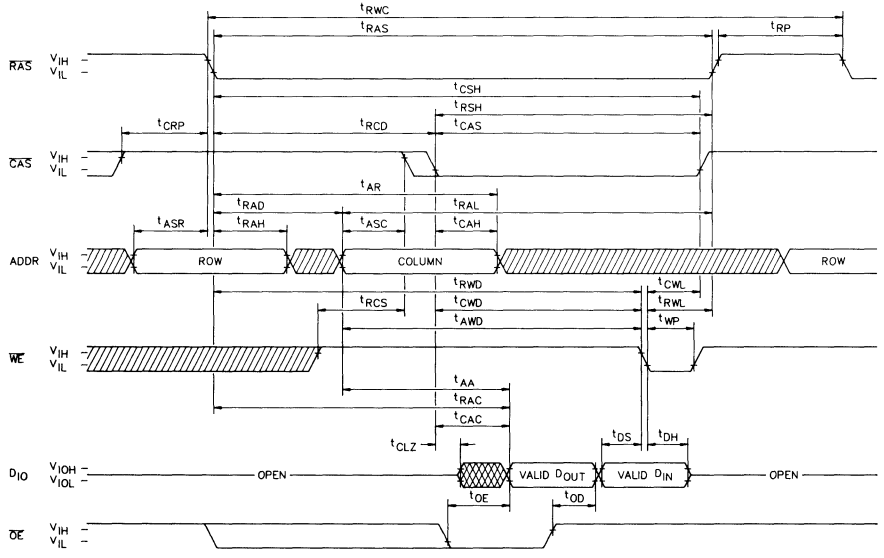
READ CYCLE



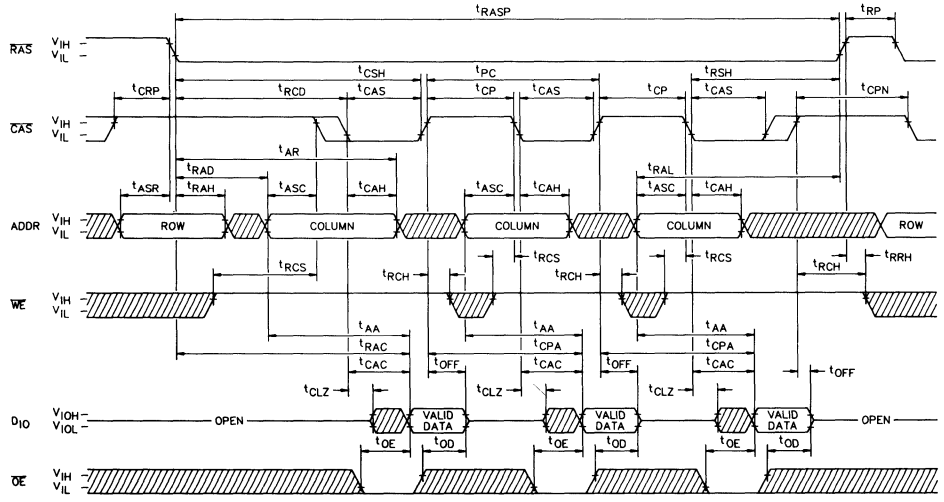
EARLY-WRITE CYCLE



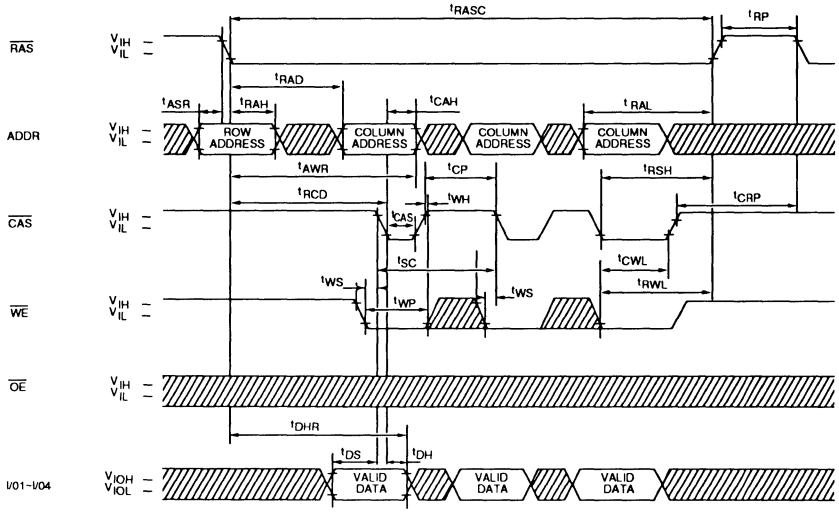
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



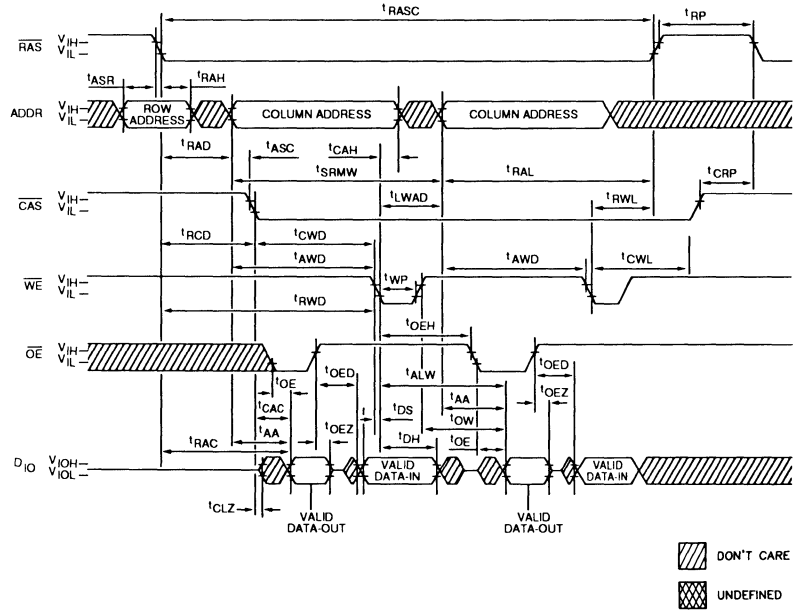
STATIC COLUMN READ CYCLE



STATIC COLUMN EARLY-WRITE CYCLE

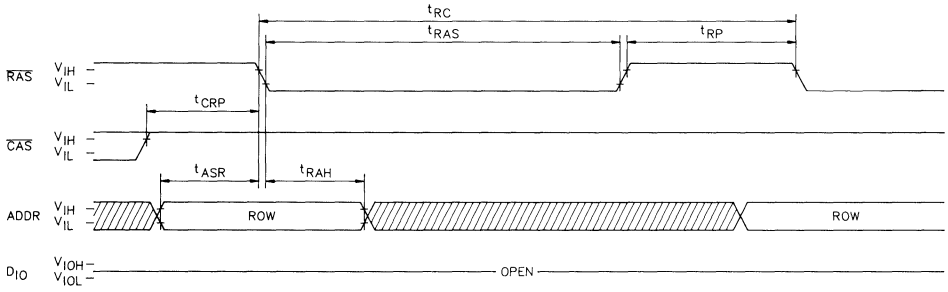


STATIC COLUMN READ-WRITE CYCLE



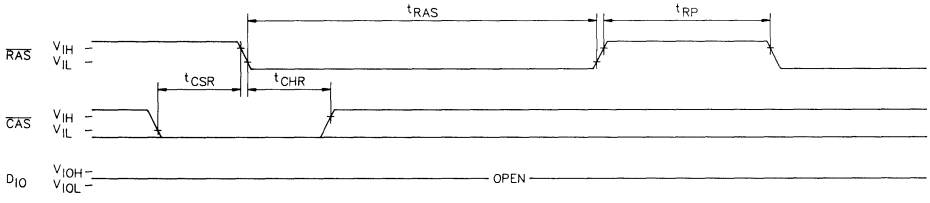
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



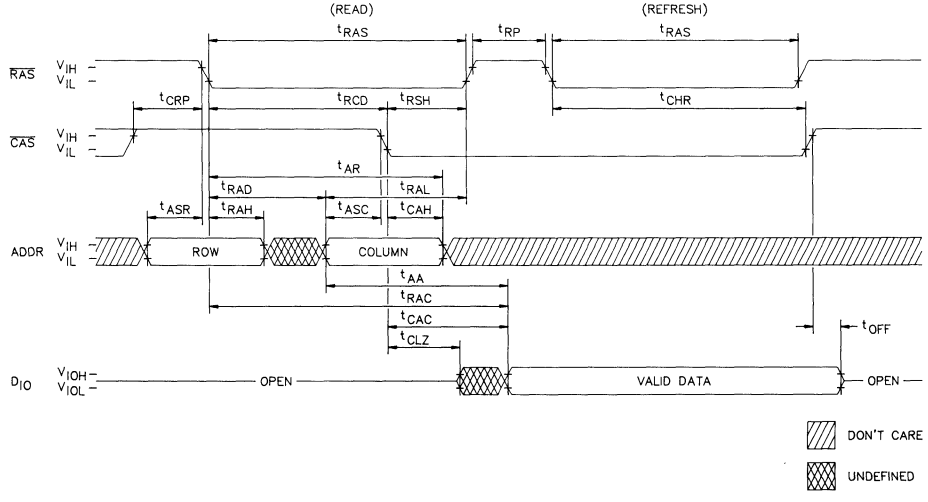
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



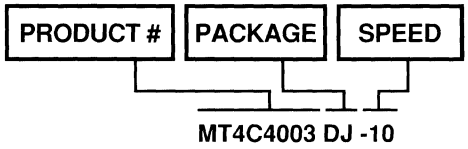
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH); $\overline{OE}$=LOW)[24]



ORDER INFORMATION

1MEG x 4, 100ns in Plastic DJ



The Micron 4 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM

4MEG x 1 DRAM

FAST PAGE MODE

FEATURES

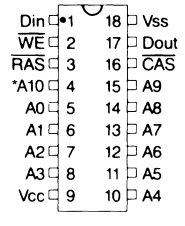
- Industry standard x1 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024 cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- Optional Fast Page Mode access cycle

OPTIONS / MARKING

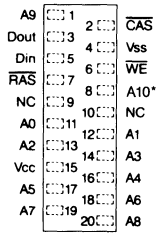
• Timing	
80ns access	-8
100ns access	-10
120ns access	-12
• Organization	
4 MEG x 1	MT4C1004
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

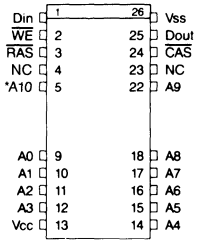
MT4C1004
18 Pin DIP



MT4C1004
20 Pin ZIP



MT4C1004
20 Pin SOJ



*Address not used for $\overline{RAS}$ only refresh

NOTE: Package Information To Be Determined.

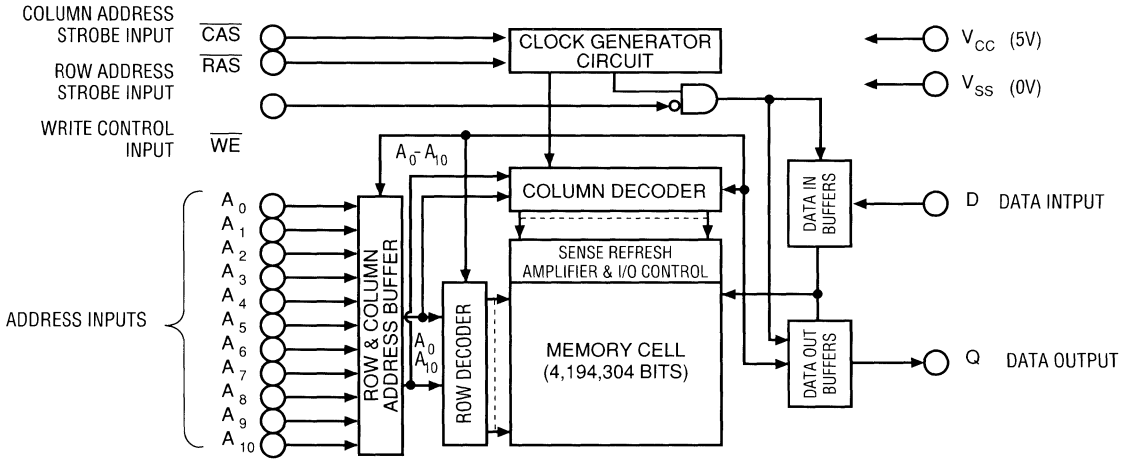
GENERAL DESCRIPTION

The MT4C1004 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A10) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	Addresses tR	Addresses tC		NOTES
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
PAGE MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$ = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		60	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		0.5	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		60	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		60	mA	3, 5
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9), D_{IN}	C_{I1}		5	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance D_{OUT}	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	160		190		220		ns	
READ-MODIFY-WRITE cycle time	t_{RWC}	185		220		255		ns	
PAGE-MODE READ or WRITE cycle time	t_{PC}	50		55		70		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100	120		ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		25	35		ns	15
Access time from column address	t_{AA}		40		50	60		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		50	60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	t_{RASP}	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		35		ns	
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		20		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	t_{CP}	10	25	10	25	15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	10	60	15	75	25	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	10	40	10	50	10	60	ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		60		110		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		50		60		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		10		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	5		5		5		ns	
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	25	ns	20
$\overline{WE}$ command set-up time	t_{WCS}	0		0		0		ns	21
Write command hold time	t_{WCH}	15		20		25		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

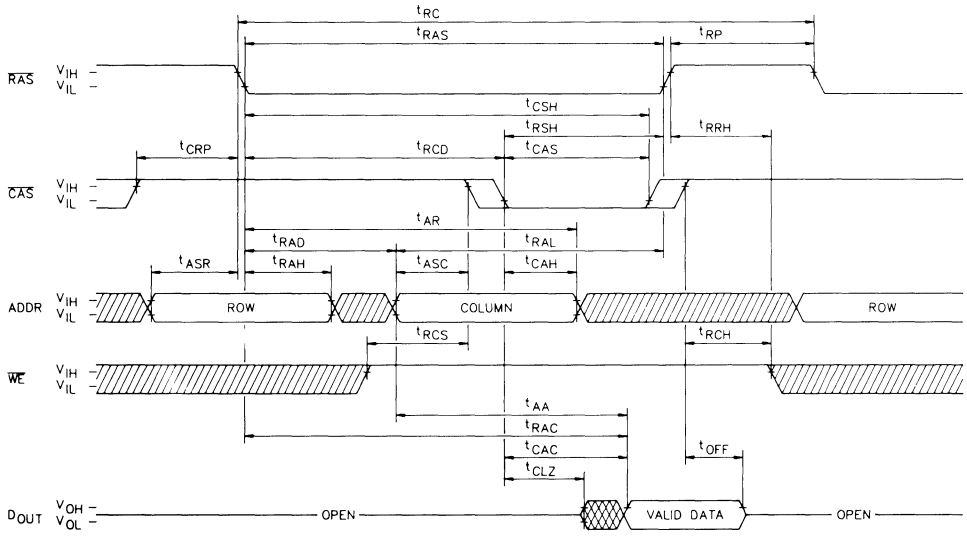
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		70		110		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		70		110		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	70		80		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		35		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		20		ns	5

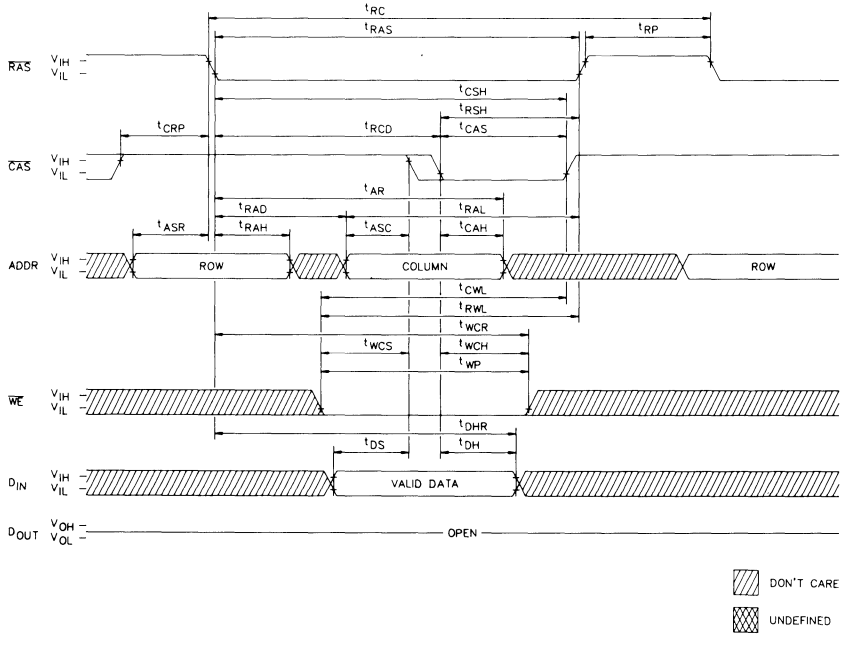
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (min), $^tAWD \geq ^tAWD$ (min) and $^tCWD \geq ^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

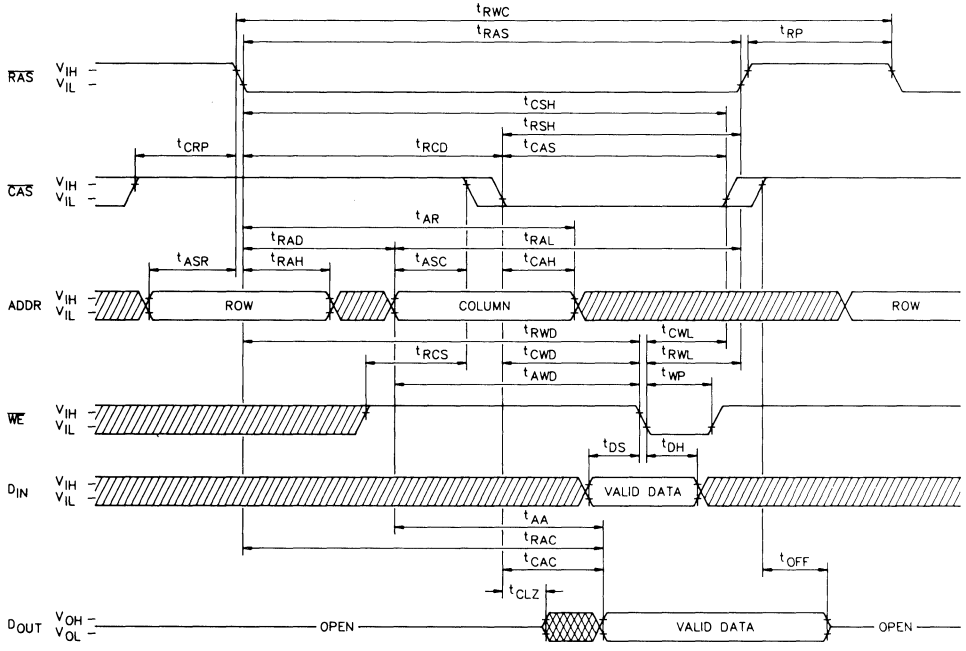
READ CYCLE



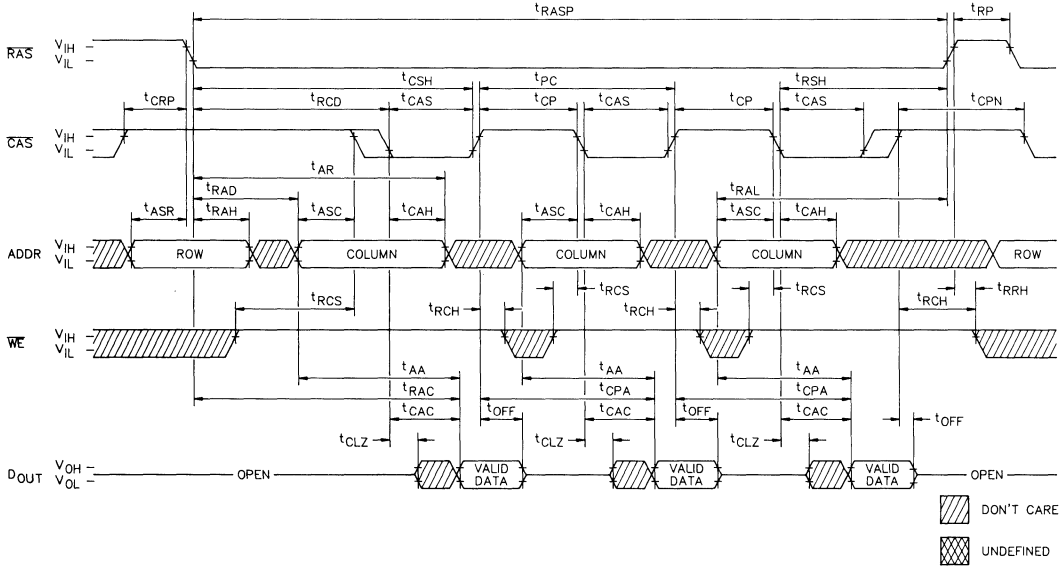
EARLY-WRITE CYCLE



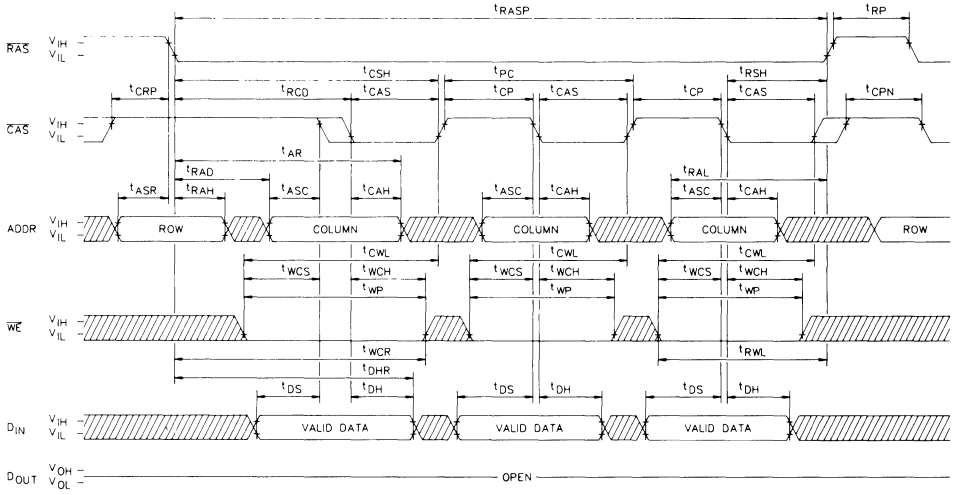
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



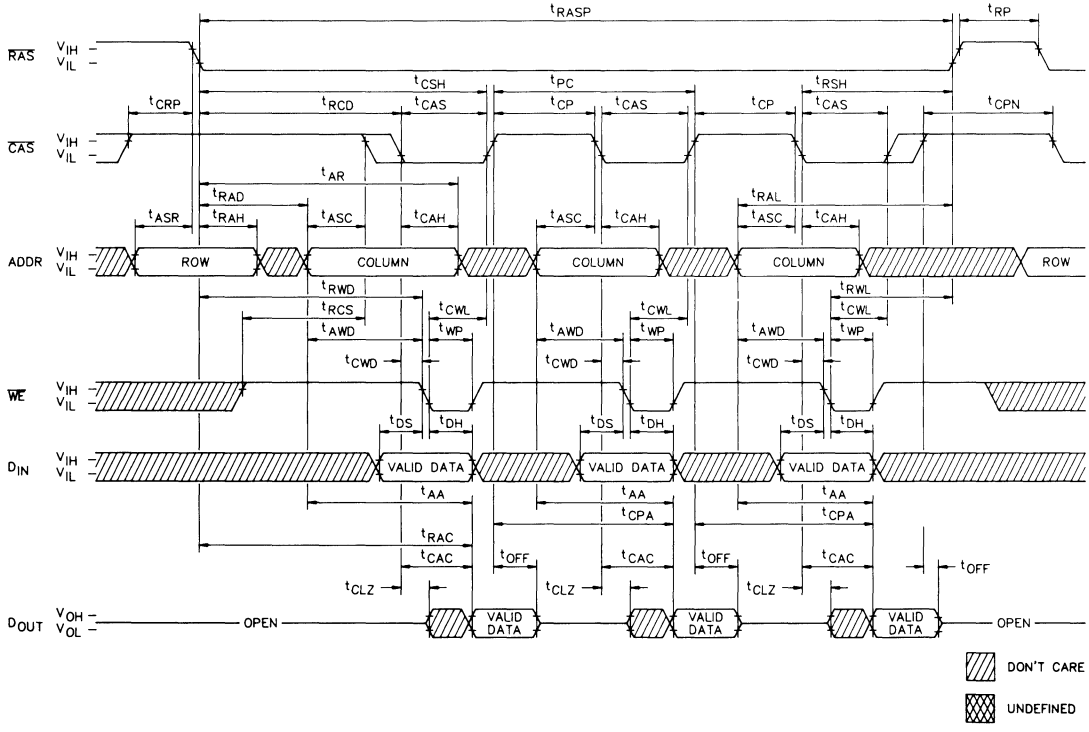
PAGE-MODE READ CYCLE



PAGE-MODE EARLY-WRITE CYCLE

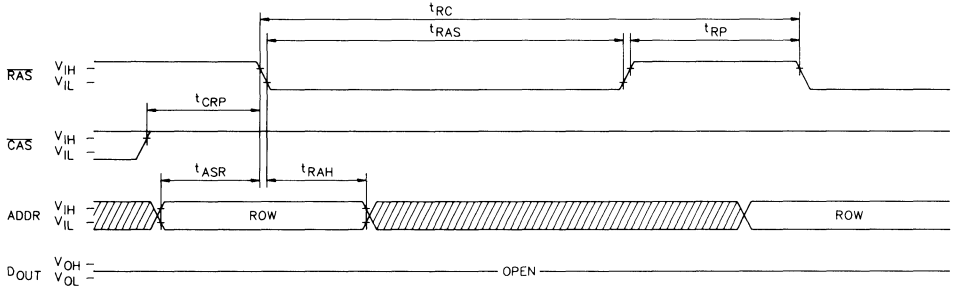


PAGE-MODE READ-WRITE CYCLE



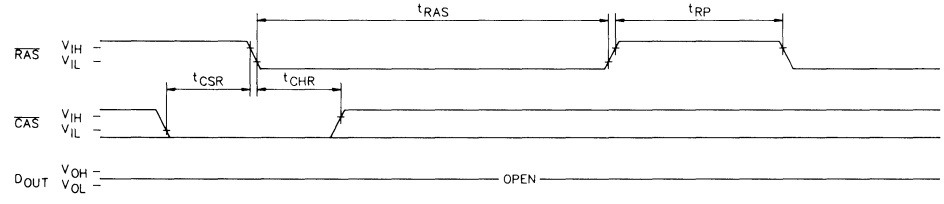
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_9; A_{10} and $\overline{WE}$ = DON'T CARE.)



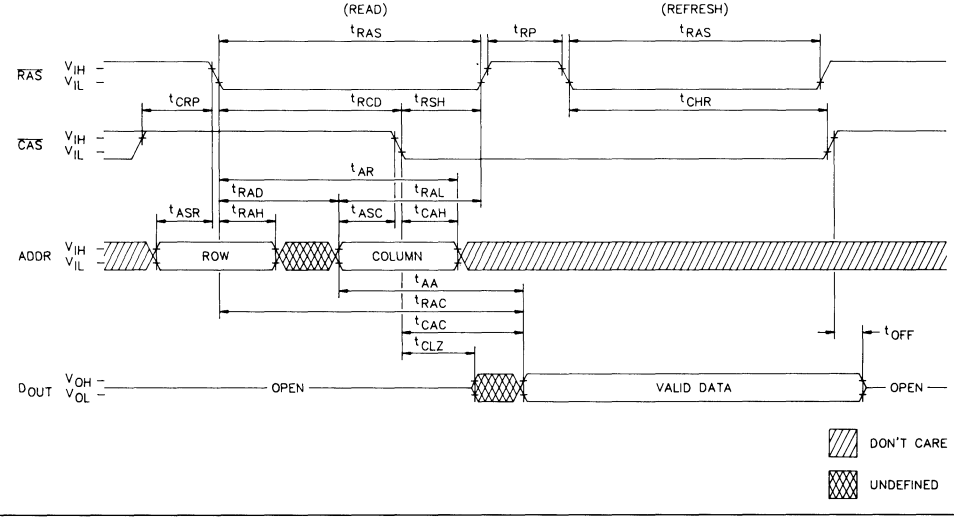
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



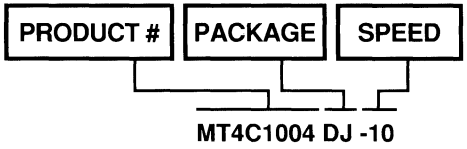
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

4 MEG x 1, 100ns in Plastic SOJ



The Micron 4 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM

4MEG x 1 DRAM

NIBBLE MODE

FEATURES

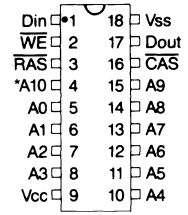
- Industry standard x1 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply.
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024 cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- Optional Nibble Mode access cycle

OPTIONS

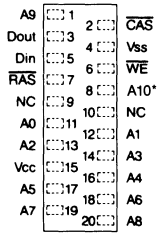
	MARKING
• Timing	
80ns access	-8
100ns access	-10
120ns access	-12
• Organization	
4 MEG x 1	MT4C1005
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

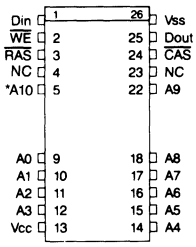
MT4C1005
18 Pin DIP



MT4C1005
20 Pin ZIP



MT4C1005
20 Pin SOJ



*Address not used for $\overline{RAS}$ only refresh

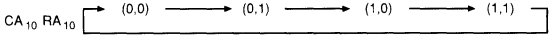
NOTE: Package Information To Be Determined.

GENERAL DESCRIPTION

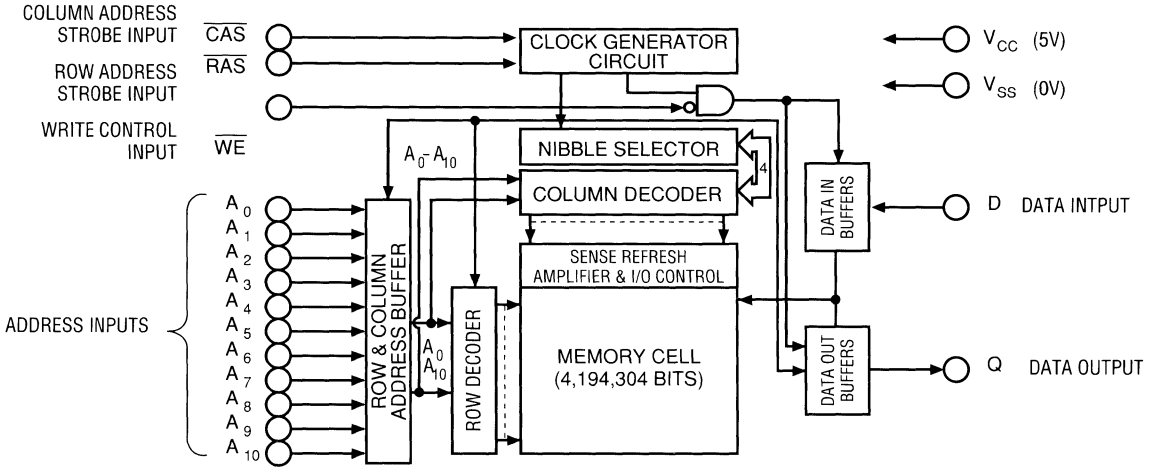
The MT4C1005 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

Nibble Mode operation allows faster sequential serial data operations (READ, WRITE or READ-MODIFY-WRITE) on up to 4 bits. The first of 4 bits is accessed in the usual manner with $\overline{CAS}$ address A9 (nibble MSB) and RAS address A9 (nibble LSB) selecting on of 4 bits within a nibble for initial access. By holding $\overline{RAS}$ low, $\overline{CAS}$ can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around (see below).



FUNCTIONAL BLOCK DIAGRAM
NIBBLE MODE



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	Addresses tR	Addresses tC		NOTES
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
NIBBLE MODE READ	L	H→L→H, L→H→L	H	ROW	COL	Valid Data Out, Valid Data Out	
NIBBLE MODE WRITE	L	H→L→H, L→H→L	L	ROW	COL	Valid Data In, Valid Data In	
NIBBLE MODE READ-WRITE	L	H→L→H, L→H→L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$ = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		60	mA	3, 4
OPERATING CURRENT: NIBBLE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		0.5	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		60	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		60	mA	3, 5
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9), D_{IN}	C_{I1}		5	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance D_{OUT}	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	160		190		220		ns	
READ-MODIFY-WRITE cycle time	t_{RWC}	185		220		255		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100	120		ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		25	35		ns	15
Access time from column address	t_{AA}		40		50	60		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		50	60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		35		ns	
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		15		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	10	60	15	75	25	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	10	40	10	50	10	60	ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		60		110		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		50		60		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	5		5		5		ns	
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	25	ns	20
$\overline{WE}$ command set-up time	t_{WCS}	0		0		0	25	ns	21
Write command hold time	t_{WCH}	15		20		0		ns	
Write command hold time (referenced to $\overline{RAS}$)	t_{WCR}	60		70		25		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

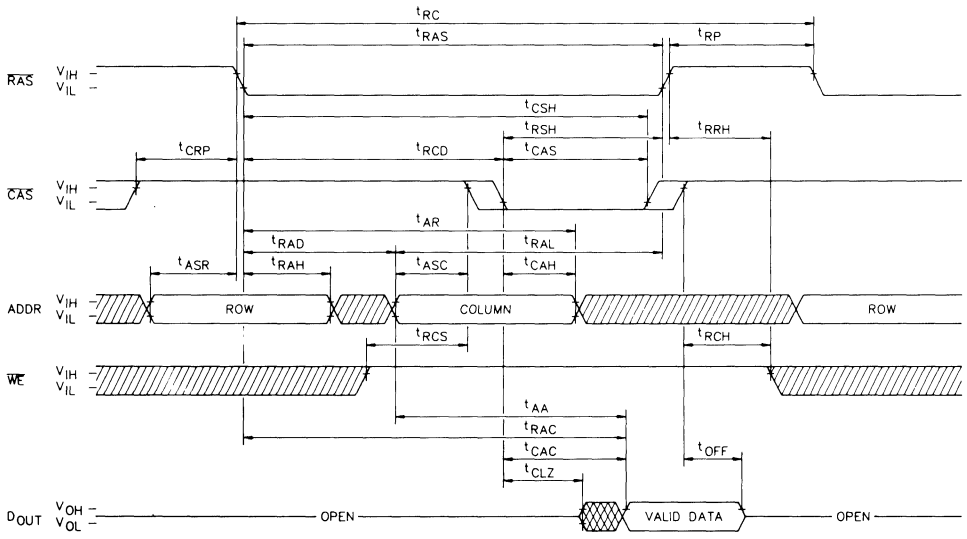
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		70		110		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	70		90		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		35		35		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0			0	ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		20		ns	5
$\overline{RAS}$ pulse width (NIBBLE MODE)	^tRASN	80	100,000	100	100,000	120	100,000	ns	
$\overline{CAS}$ precharge time (NIBBLE MODE)	^tNCP	10	25	10	25	15	30	ns	
NIBBLE MODE cycle time	^tNC	35		35		40		ns	
NIBBLE MODE READ-MODIFY-WRITE cycle time	^tNRWL	50		55		70		ns	
NIBBLE MODE READ-MODIFY-WRITE cycle time	^tNRWC	55		55		60		ns	
NIBBLE MODE access time	^tNCAC	15		15		20		ns	15
NIBBLE MODE pulse width	^tNCAS	15		15		20		ns	
NIBBLE MODE $\overline{CAS}$ precharge time	^tNCP	10		10		15		ns	
NIBBLE MODE $\overline{RAS}$ hold time	^tNRSH	15		15		20		ns	
NIBBLE MODE $\overline{CAS}$ to $\overline{WRITE}$ delay time	^tNCWD	15		15		20		ns	
NIBBLE MODE $\overline{WRITE}$ command to $\overline{RAS}$ load time	^tNRWL	15		15		20		ns	
NIBBLE MODE $\overline{WRITE}$ command to $\overline{CAS}$ load time	^tNCWL	15		15		20		ns	

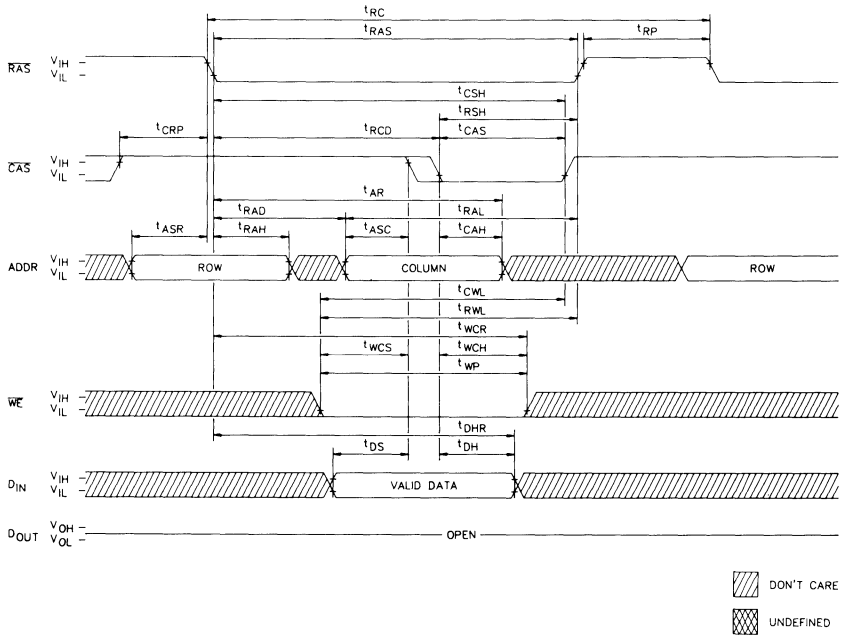
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (min), $^tAWD \geq {}^tAWD$ (min) and $^tCWD \geq {}^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

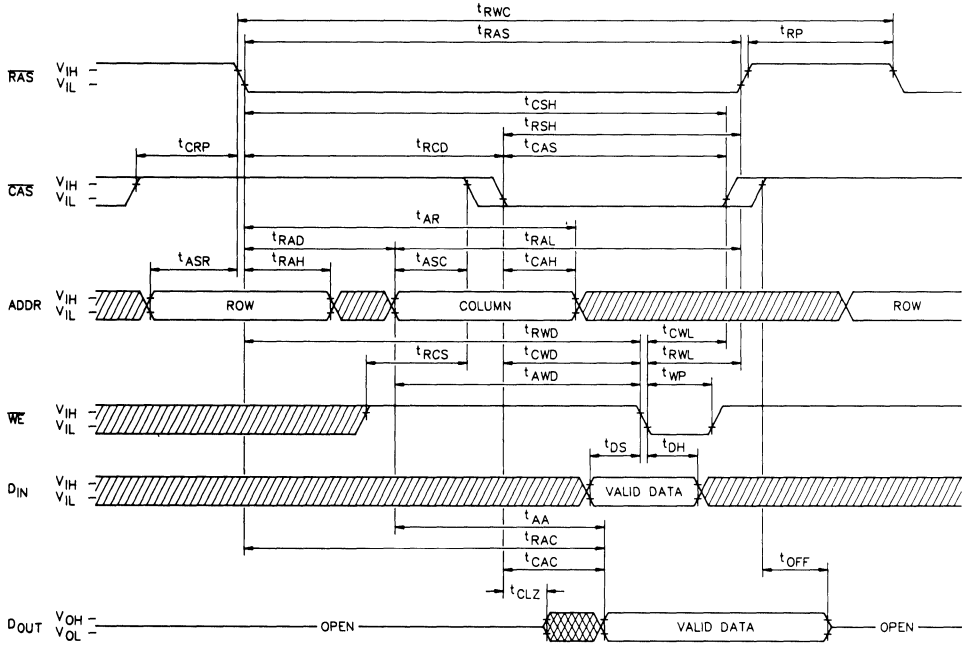
READ CYCLE



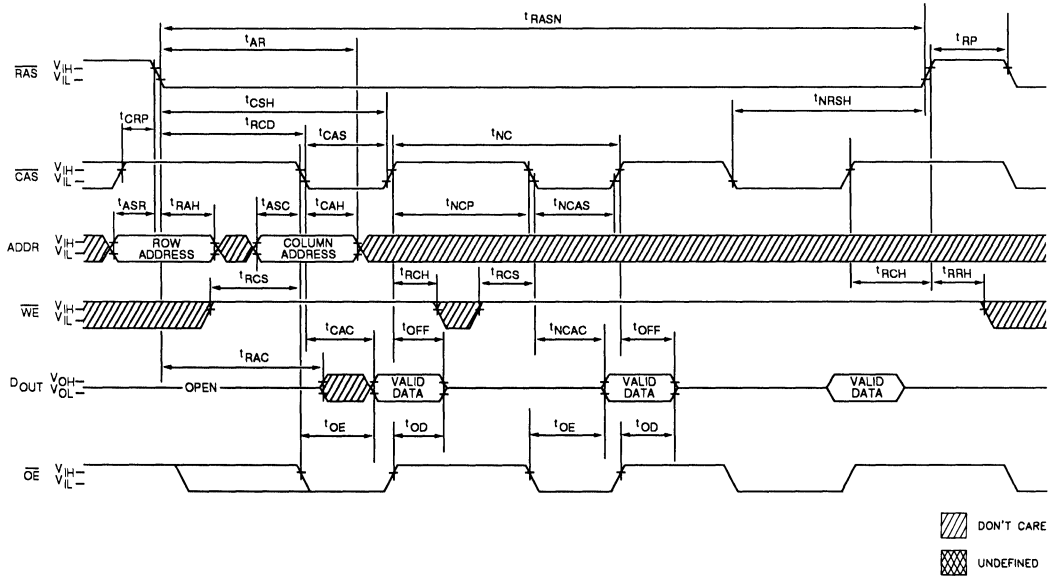
EARLY-WRITE CYCLE



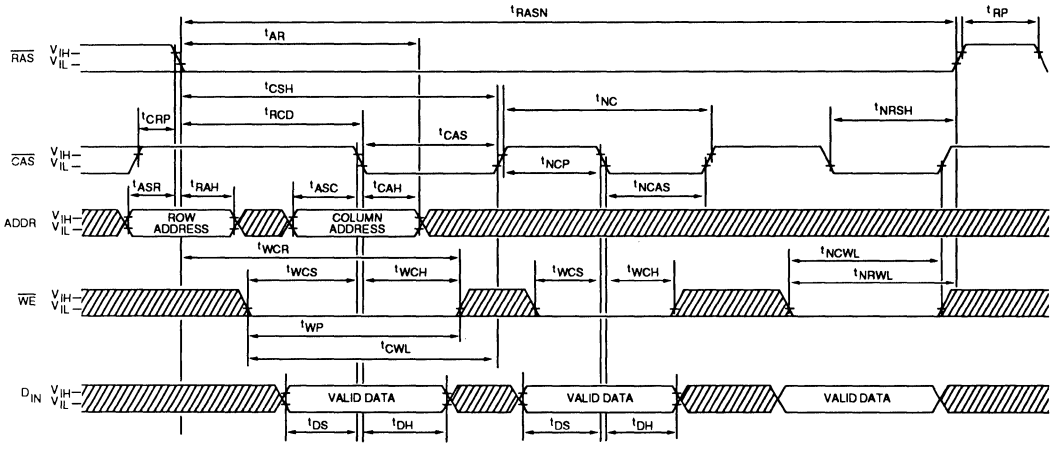
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



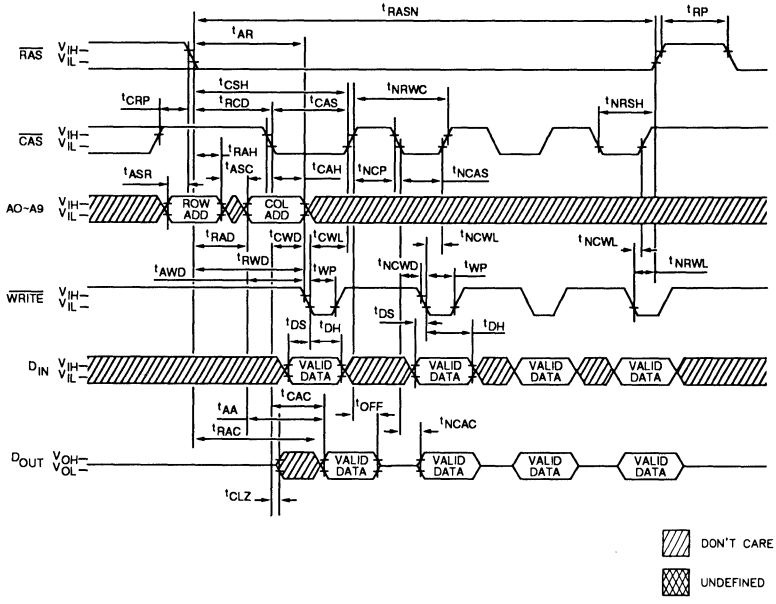
NIBBLE MODE READ CYCLE



NIBBLE MODE EARLY-WRITE CYCLE

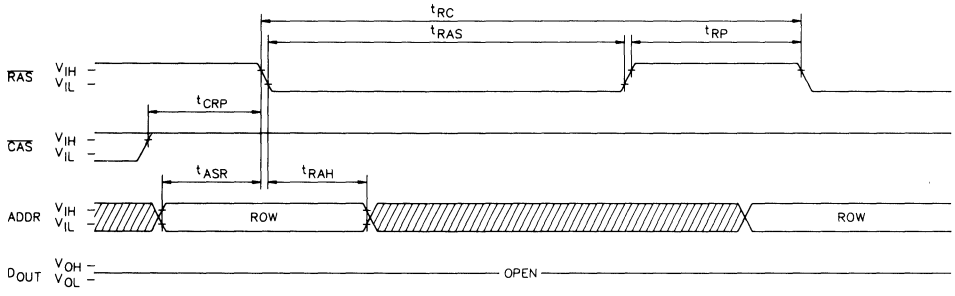


NIBBLE MODE READ-WRITE CYCLE



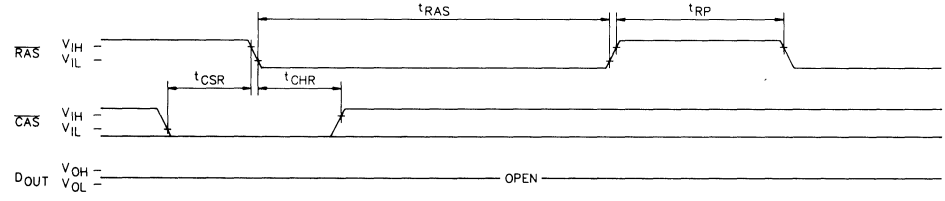
$\overline{RAS}$ ONLY REFRESH CYCLE

($ADDR = A_0 - A_9$; A_{10} and $\overline{WE}$ = DON'T CARE.)



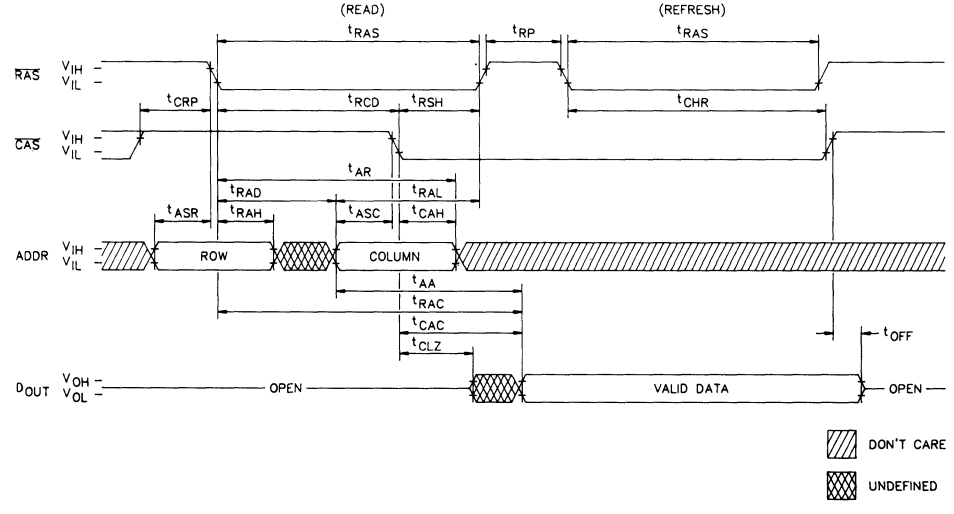
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

($A_0 - A_{10}$ and $\overline{WE}$ = DON'T CARE)



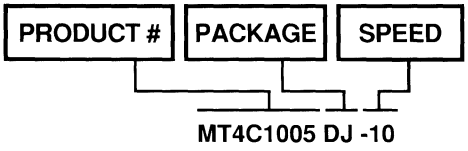
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

4 MEG x 1, 100ns in Plastic SOJ



The Micron 4 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM

4 MEG x 1 DRAM

STATIC COLUMN

FEATURES

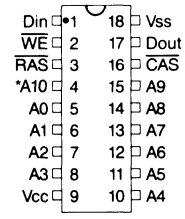
- Industry standard x1 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply.
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024 cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- Optional Static Column access cycle

OPTIONS

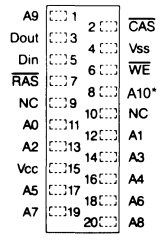
	MARKING
• Timing	
80ns access	-8
100ns access	-10
120ns access	-12
• Organization	
4 MEG x 1	MT4C1006
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

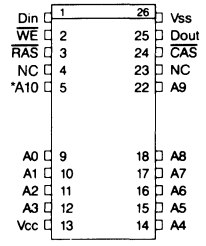
MT4C1006
18 Pin DIP



MT4C1006
20 Pin ZIP



MT4C1006
20 Pin SOJ



*Address not used for $\overline{RAS}$ only refresh

NOTE: Package Information To Be Determined.

GENERAL DESCRIPTION

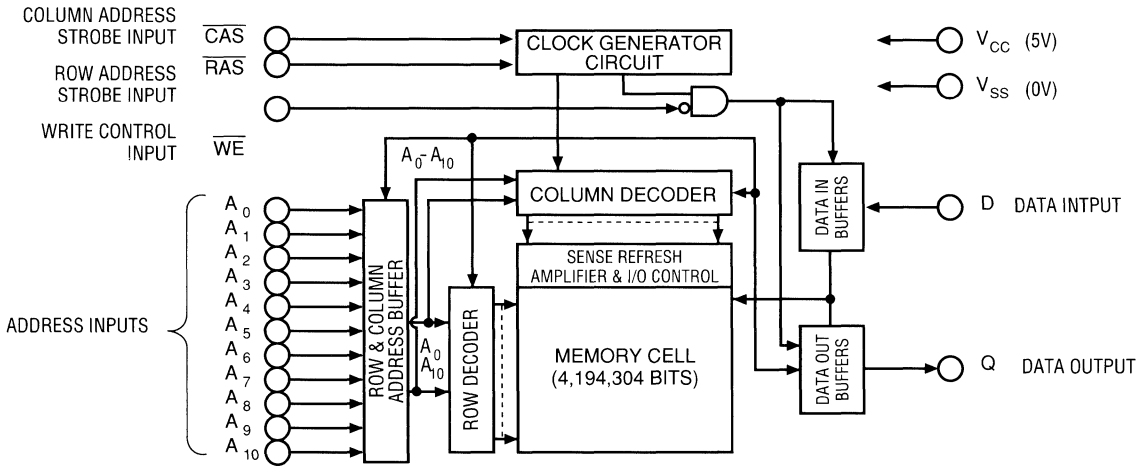
The MT4C1006 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$).

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

STATIC COLUMN operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary.

The STATIC COLUMN cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the STATIC COLUMN operation.

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	Addresses tR	Addresses tC		NOTES
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
STATIC COLUMN READ	L	L	H	ROW	COL COL	Valid Data Out, Valid Data Out	
STATIC COLUMN WRITE	L	L	L	ROW	COL COL	Valid Data In Valid Data In	
STATIC COLUMN READ-WRITE	L	L	H→L→H	ROW	COL COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C, = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		60	mA	3, 4
OPERATING CURRENT: STATIC COLUMN ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		0.5	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		60	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		60	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DRAM

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9), D_{IN}	C_{I1}		5	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance D_{OUT}	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	150		190		220		ns	
READ-MODIFY-WRITE cycle time	^tRWC	180		220		255		ns	
Access time from $\overline{RAS}$	^tRAC		80		100	120		ns	14
Access time from $\overline{CAS}$	^tCAC		20		25	35		ns	15
Access time from column address	^tAA		40		50	60		ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		50	60		ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		35		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	75	10	75	25	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	10	50	10	50	10	60	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		60		110		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	5		5		5		ns	
Output buffer turn-off delay	^tOFF	0	25	0	25	5		ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

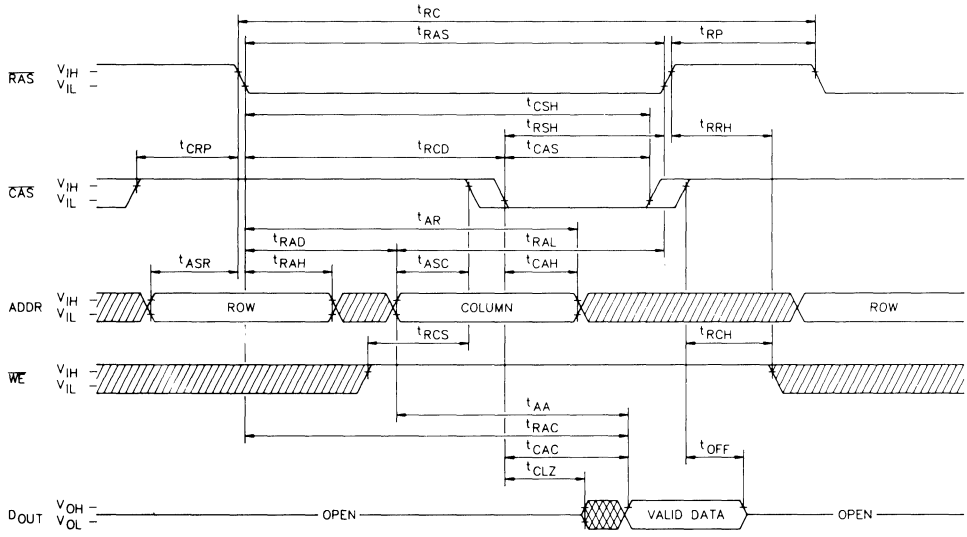
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	35		70		105		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		25		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		25		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	35		70		110		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	70		90		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	30		35		35		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		20		20		ns	5
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	80	100,000	100	100,000	120	100,000	ns	
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		15		ns	
STATIC COLUMN MODE cycle time	^tSC	55		55		60		ns	
STATIC COLUMN READ-MODIFY-WRITE cycle time	^tSRMW	135		135		140		ns	
Last write to column address delay time	^tLWAD	20	85	25	95	30	100	ns	
Last write to column address hold time	^tAHLW		85		95		100	ns	
Output data hold time from column address	^tAOH	5	—	5	—	5	—	ns	
Output data enable from write	^tOW	—	25	—	25	—	30	ns	

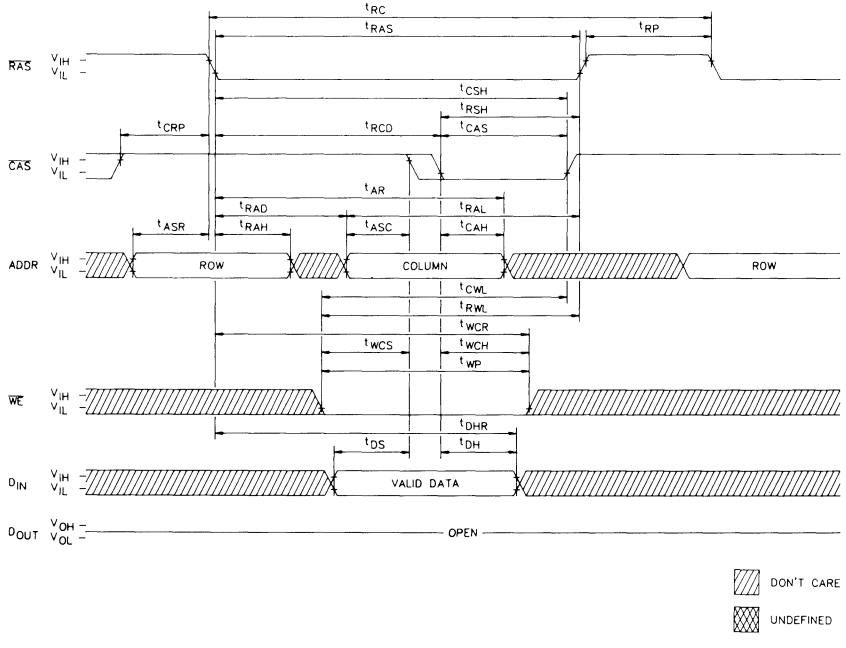
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (min), $^tAWD \geq ^tAWD$ (min) and $^tCWD \geq ^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

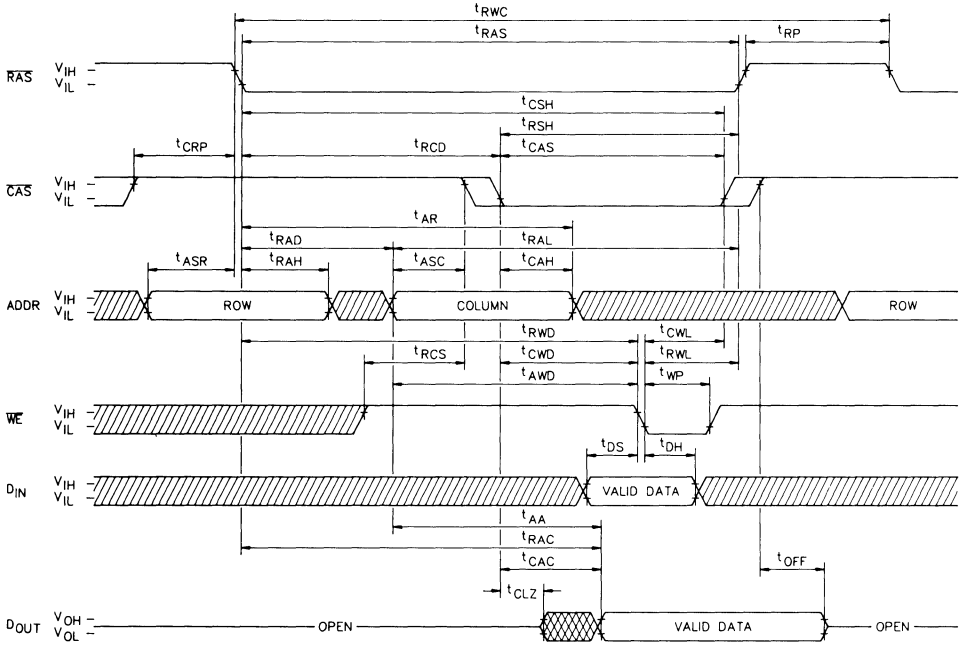
READ CYCLE



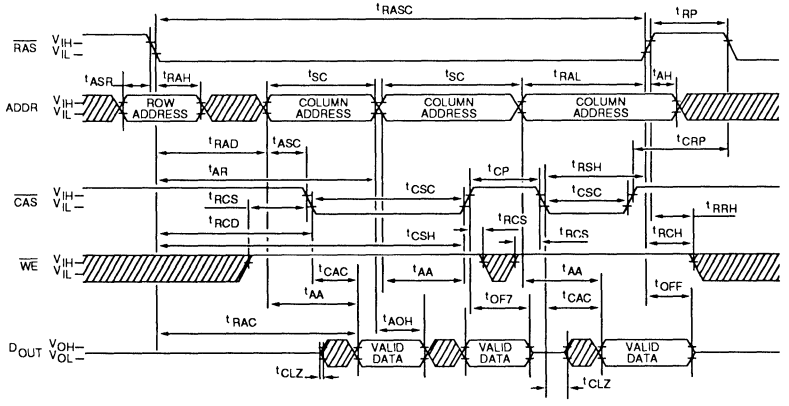
EARLY-WRITE CYCLE



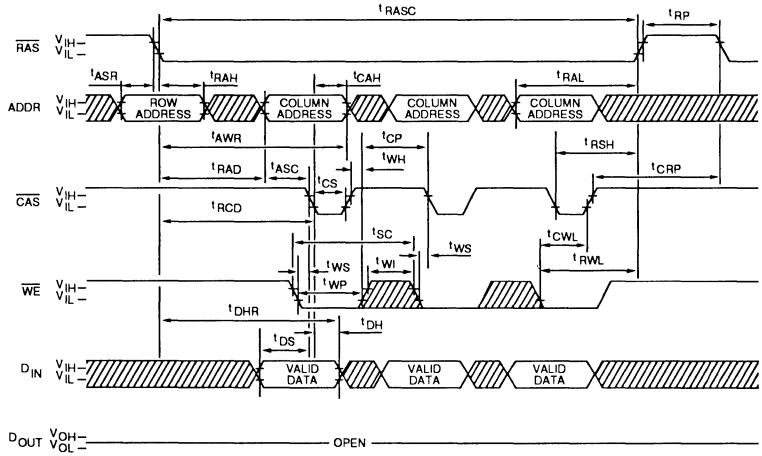
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



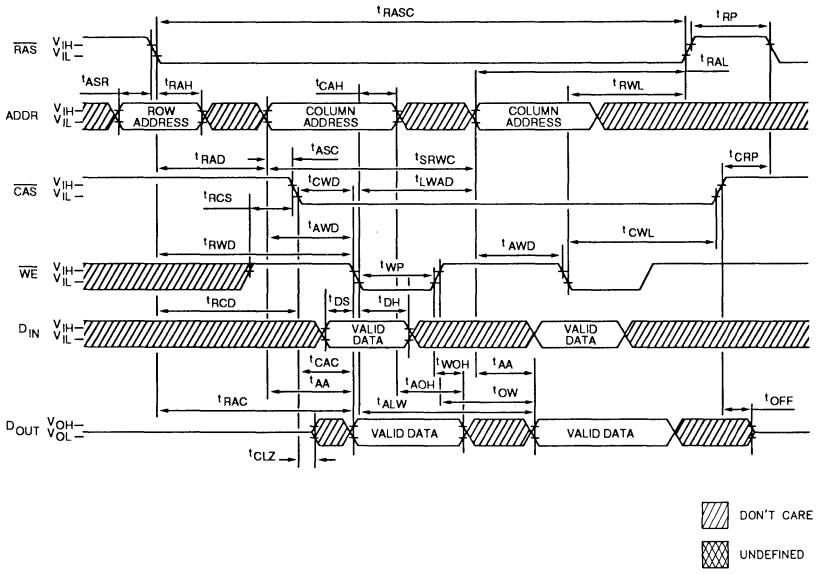
STATIC COLUMN READ CYCLE



STATIC COLUMN EARLY-WRITE CYCLE

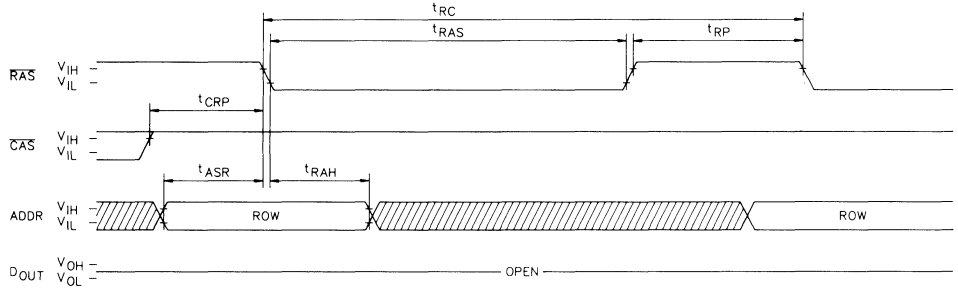


STATIC COLUMN READ-WRITE CYCLE



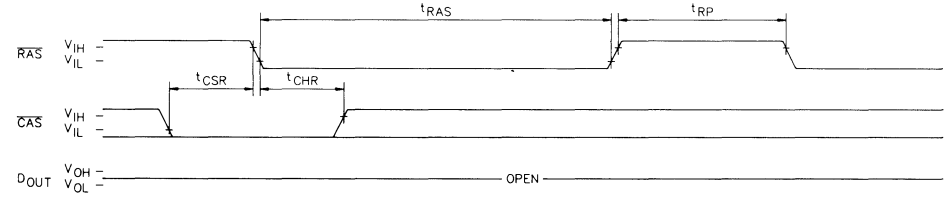
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_9; A_{10} and $\overline{WE}$ = DON'T CARE.)



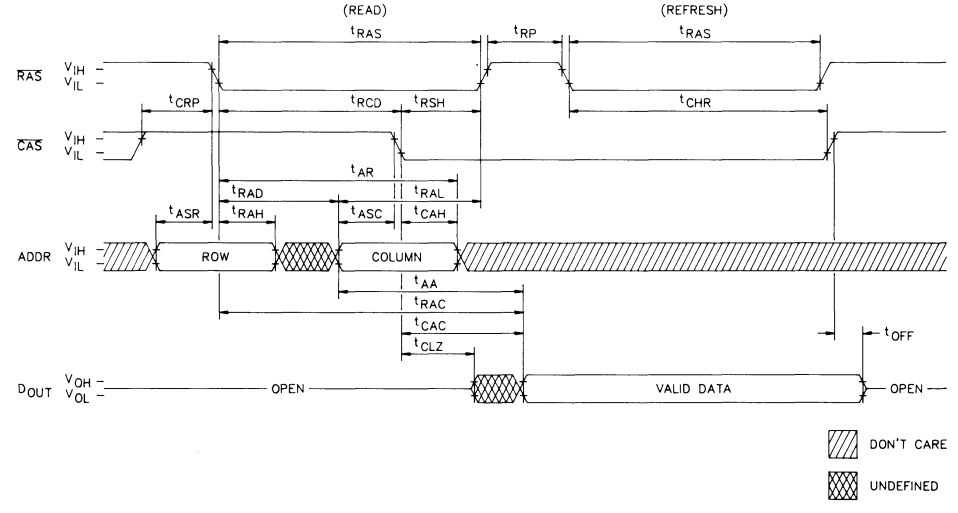
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_{10}, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



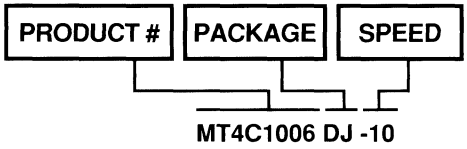
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

4 MEG x 1, 100ns in Plastic SOJ



The Micron 4 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package		Process	Page
				Standby	Active	SIP	SIMM		
64K x 8	Page Mode	MT8068M,MN	100,120,150,200	45mw	450mw	30	30	NMOS	2-3
64K x 9	Page Mode	MT9068M,MN	100,120,150,200	45mw	450mw	30	30	NMOS	2-13
256K x 4	Page Mode	MT4259M,MN	80,100,120,150	60mw	600mw	22	22	NMOS	2-23
256K x 5	Page Mode	MT85259M,MN	80,100,120,150	60mw	600mw	24	24	NMOS	2-33
256K x 8	Page Mode	MT8259DMN	80,100,120,150	135mw	1350mw	30	30	NMOS	2-43
256K x 8	Page Mode	MT8259M,MN	80,100,120,150	135mw	1350mw	30	30	NMOS	2-53
256K x 9	Page Mode	MT9259DMN	80,100,120,150	135mw	1350mw	30	30	NMOS	2-63
256K x 9	Page Mode	MT9259M,MN	80,100,120,150	135mw	1350mw	30	30	NMOS	2-73
256K x 36	Page Mode	MT8C3656M,MN	100,120,150	140mw	2000mw	72	72	C/NMOS	2-83
1 Meg x 8	Static Column	MT8C8026M,MN	100,120,150	45mw	1575mw	30	30	CMOS	2-115
1 Meg x 8	Nibble Mode	MT8C8025M,MN	100,120,150	45mw	1575mw	30	30	CMOS	2-103
1 Meg x 8	Fast Page Mode	MT8C8024M,MN	100,120,150	45mw	1575mw	30	30	CMOS	2-93
1 Meg x 9	Static Column	MT8C9026M,MN	100,120,150	45mw	1575mw	30	30	CMOS	2-149
1 Meg x 9	Nibble Mode	MT8C9025M,MN	100,120,150	45mw	1575mw	30	30	CMOS	2-137
1 Meg x 9	Fast Page Mode	MT8C9024M,MN	100,120,150	45mw	1575mw	30	30	CMOS	2-127

DRAM MODULES

64K x 8 DRAM

FEATURES

- Industry standard pin-out in a 30-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 45mW standby, 450mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

- Timing

80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15

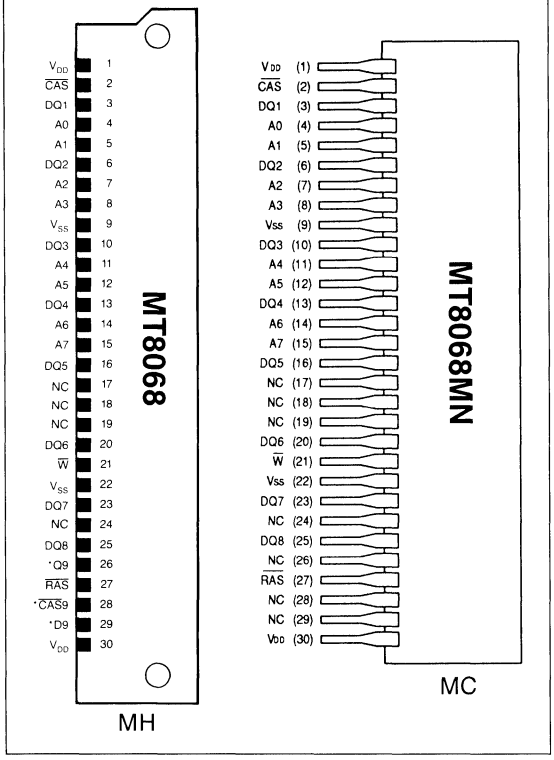
- Organization

64K x 8	MT8068

- Packages:

Leadless 30-pin SIMM	M
Leaded 30-pin SIP	MN

PIN ASSIGNMENT (Top View)



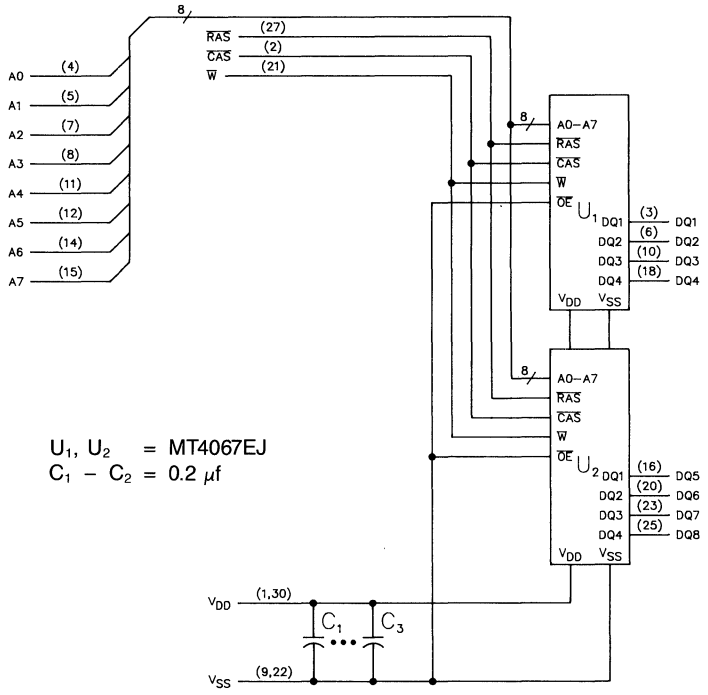
A0-A7	Address Inputs	$\overline{CAS}$	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
Q9	Data-Out	$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Write Enable	VDD	Power (+5V)
Vss	Ground		

GENERAL DESCRIPTION

The MT8068M/MN is a randomly accessed solid-state memory containing 65,536 bits organized in a x8 configuration. The 14 address bits are entered 7 bits at a time using $\overline{RAS}$ to latch the first 7 bits and $\overline{CAS}$ the latter 7 bits. If the $\overline{WE}$ pin goes low prior to $\overline{CAS}$ going low, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined PAGE boundary. Returning $\overline{RAS}$ high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the $\overline{RAS}$ high-time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (Refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$) (V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-80	80	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-80	80	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	15	15	15	15	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	195	165	165	135	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	195	165	165	135	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	165	120	120	105	mA	2
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	195	165	165	135	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8)	C_{I1}		15	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		24	pF	17
Output Capacitance D_{OUT}, D_{IN}	C_O		7	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

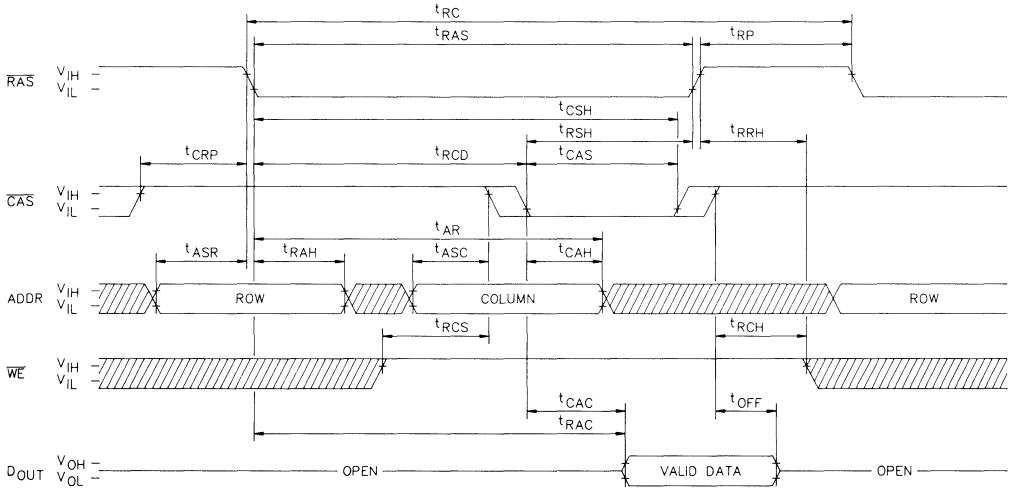
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
RAS pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	60	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		110		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	18
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 16
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	19

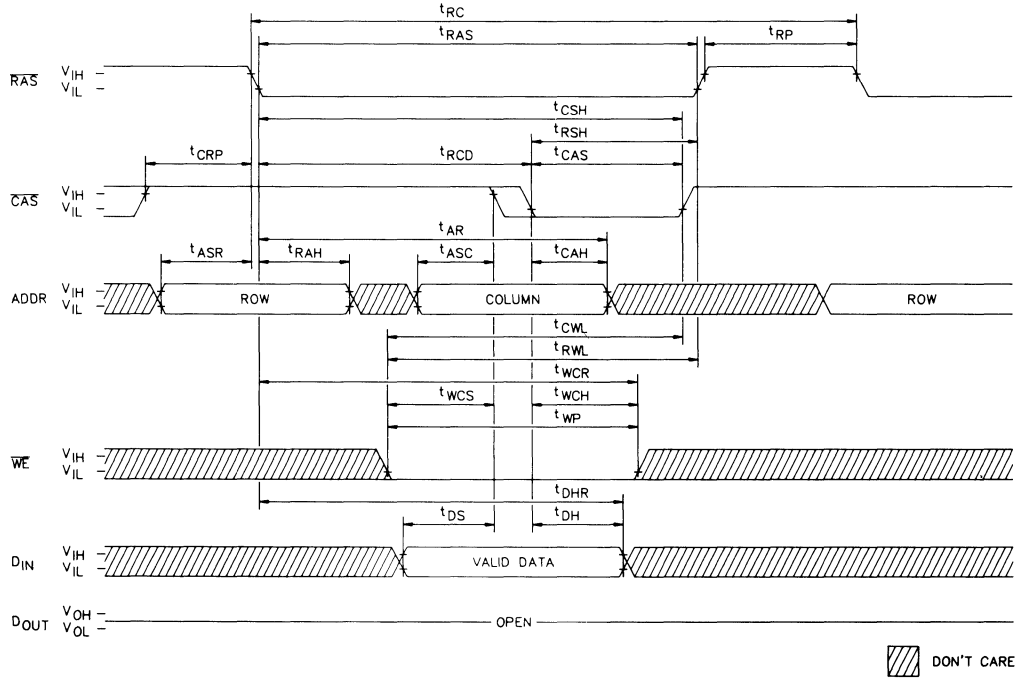
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
18. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set $\overline{WE}$ = LOW.

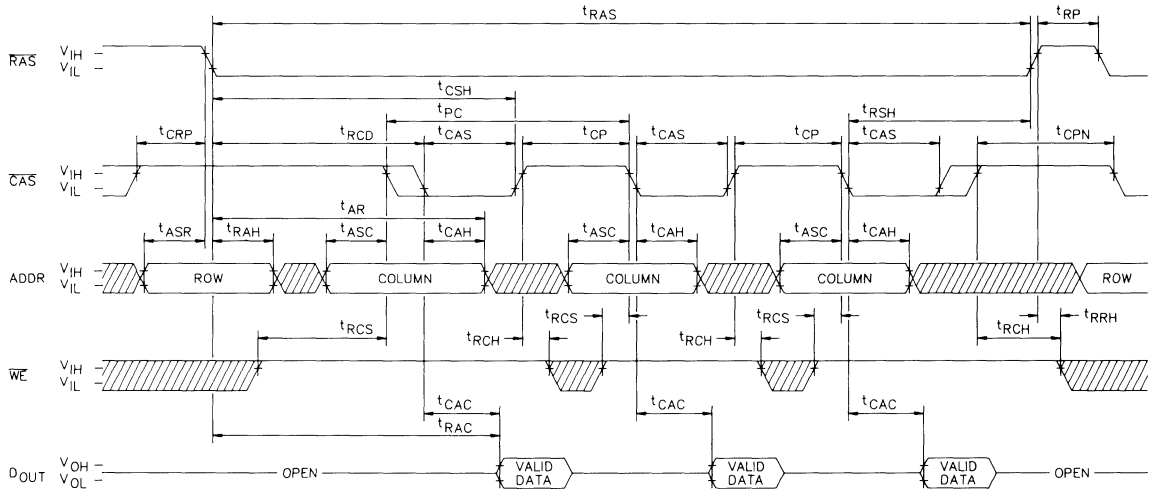
READ CYCLE



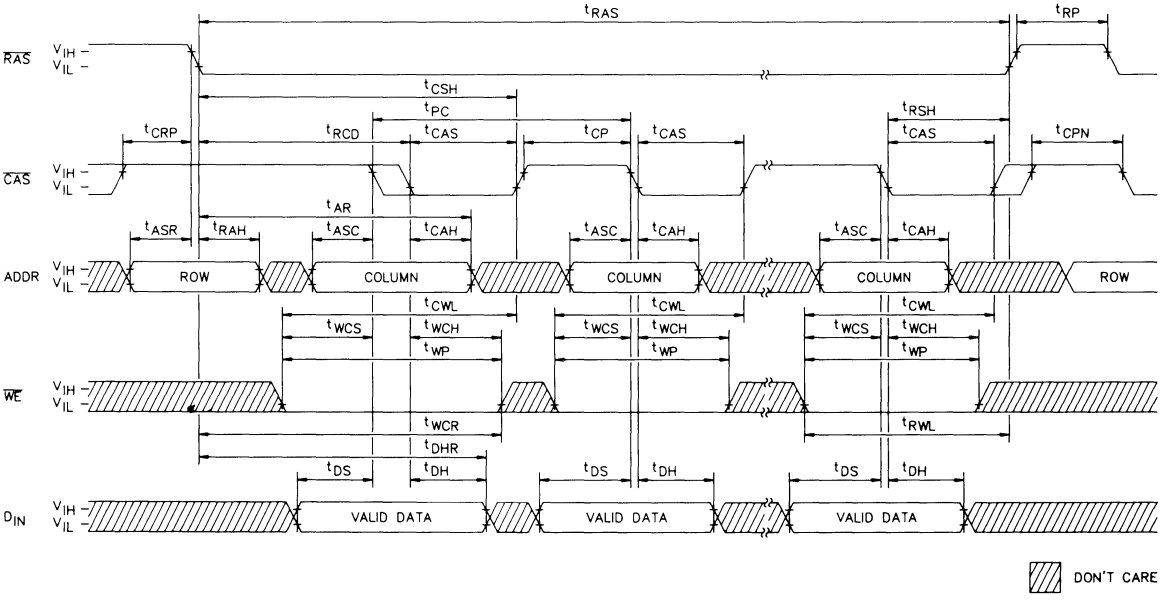
EARLY-WRITE CYCLE



PAGE-MODE READ CYCLE



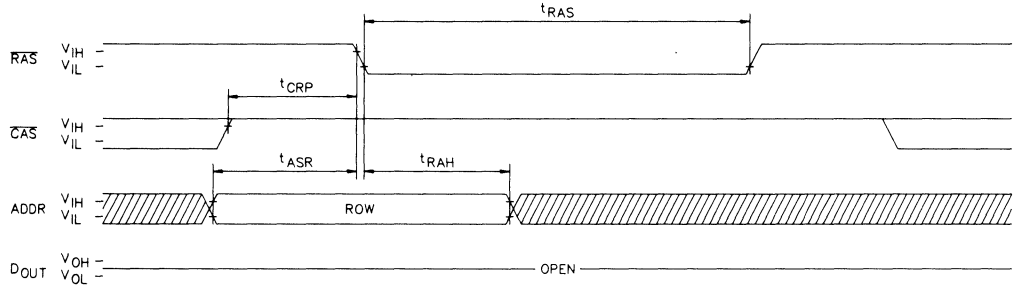
PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

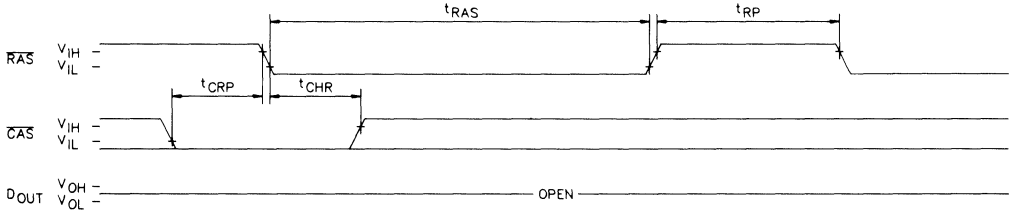
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



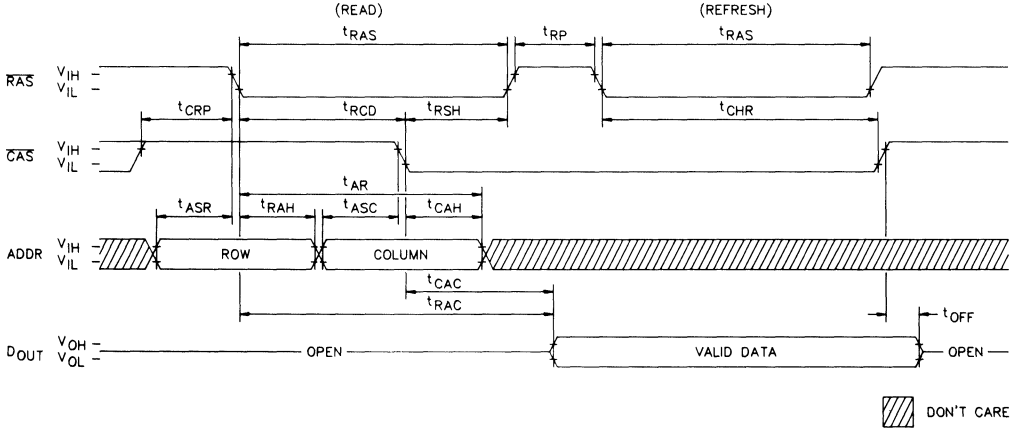
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 $\overline{WE}$, $\overline{OE}$ = DON'T CARE.)



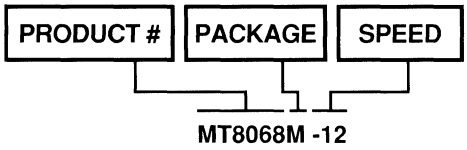
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

64K x 8, 120ns access, Leadless SIMM



The Micron 64K x 8 DRAM module is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance NMOS double-poly process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM MODULES

64K x 9 DRAM

FEATURES

- Industry standard pin-out in a 30-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 45mW standby, 450mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

- Timing

80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15

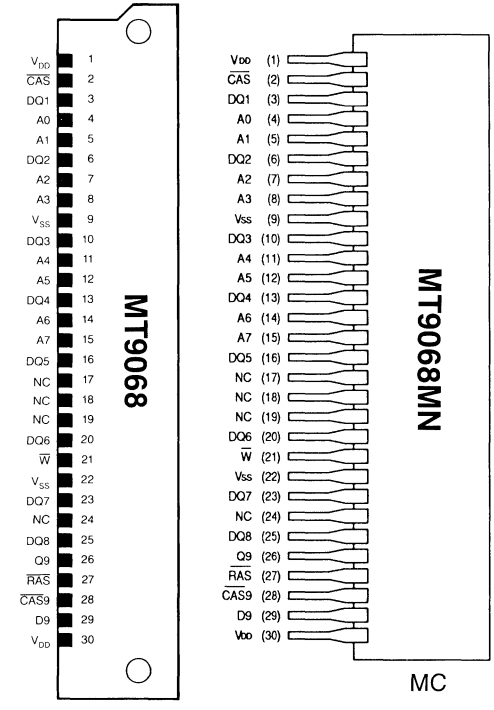
- Organization

64K x 9	MT9068

- Packages:

Leadless 30-pin SIMM	M
Leaded 30-pin SIP	MN

PIN ASSIGNMENT (Top View)



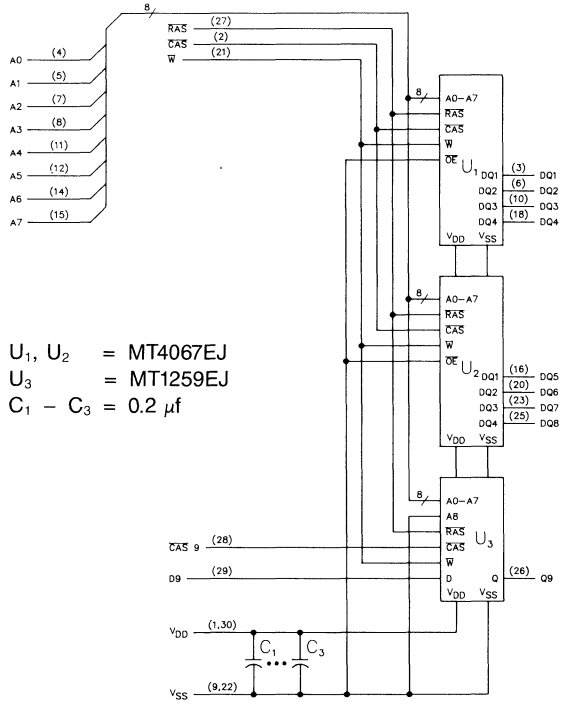
A0-A7	Address Inputs	$\overline{CAS}$, $\overline{CAS9}$	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
Q9	Data-Out	$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Write Enable	VDD	Power (+5V)
Vss	Ground		

GENERAL DESCRIPTION

The MT9068M/MN is a randomly accessed solid-state memory containing 65,536 bits organized in a x9 configuration. The 16 address bits are entered 8 bits at a time using $\overline{RAS}$ to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. If the $\overline{WE}$ pin goes low prior to $\overline{CAS}$ going low, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined PAGE boundary. Returning $\overline{RAS}$ high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the $\overline{RAS}$ high-time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (Refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



U_1, U_2 = MT4067EJ
U_3 = MT1259EJ
C_1 – C_3 = 0.2 μf

FUNCTIONAL TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 9 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$) (V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-90	90	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-90	90	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	15	15	15	15	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	195	165	165	135	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	195	165	165	135	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	165	120	120	105	mA	2
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	195	165	165	135	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8)	C_{I1}		15	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		24	pF	17
Output Capacitance D_{OUT}, D_{IN}	C_O		7	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

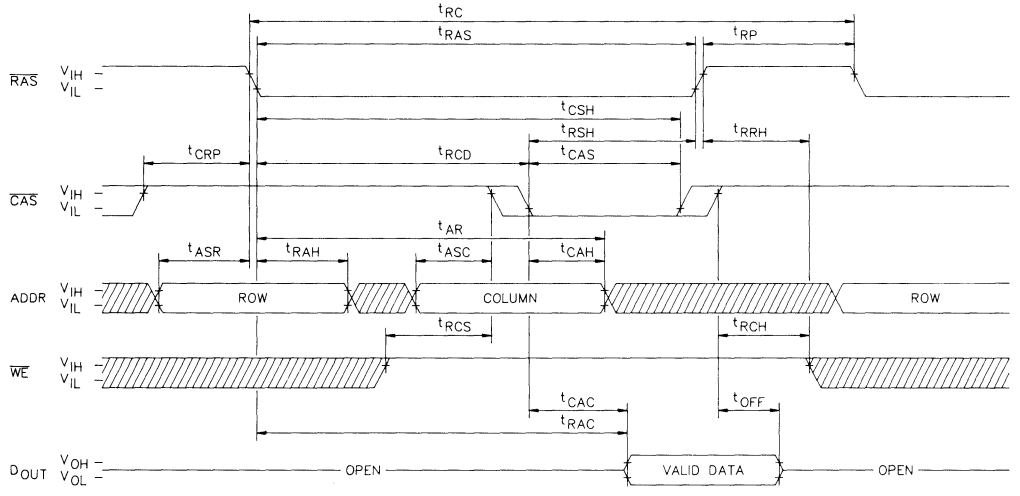
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
RAS pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	60	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		110		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	18
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 16
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	19

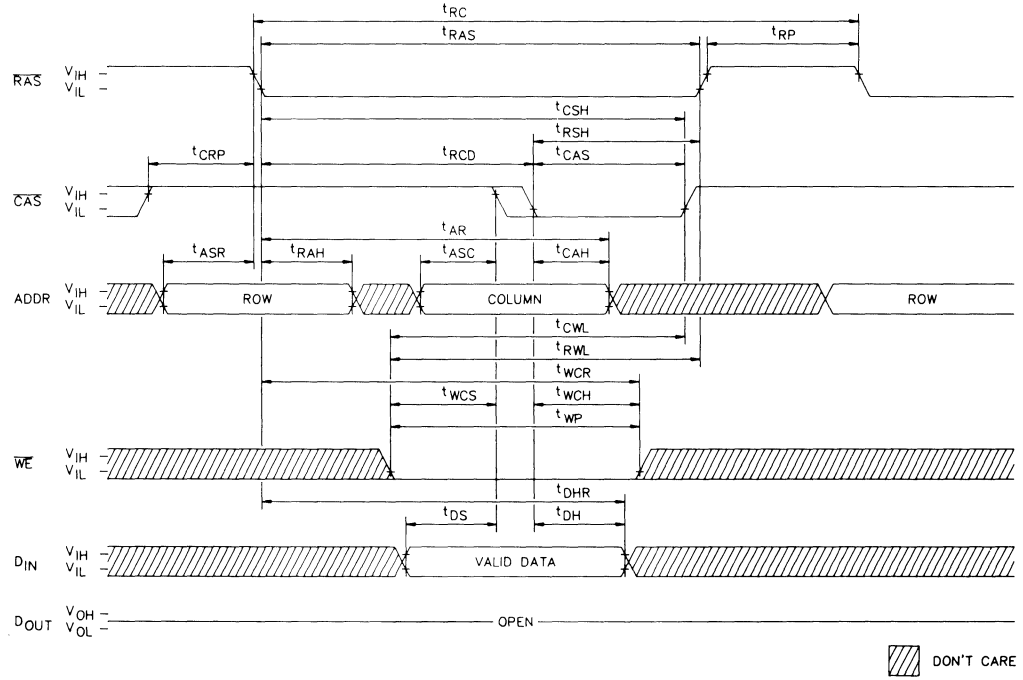
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq {}^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
18. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set $\overline{WE}$ = LOW.

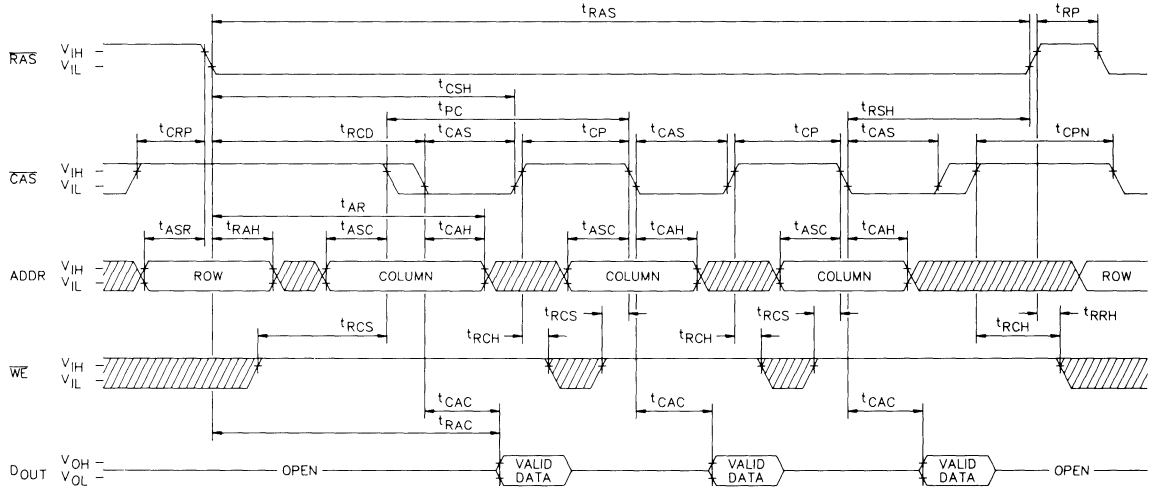
READ CYCLE



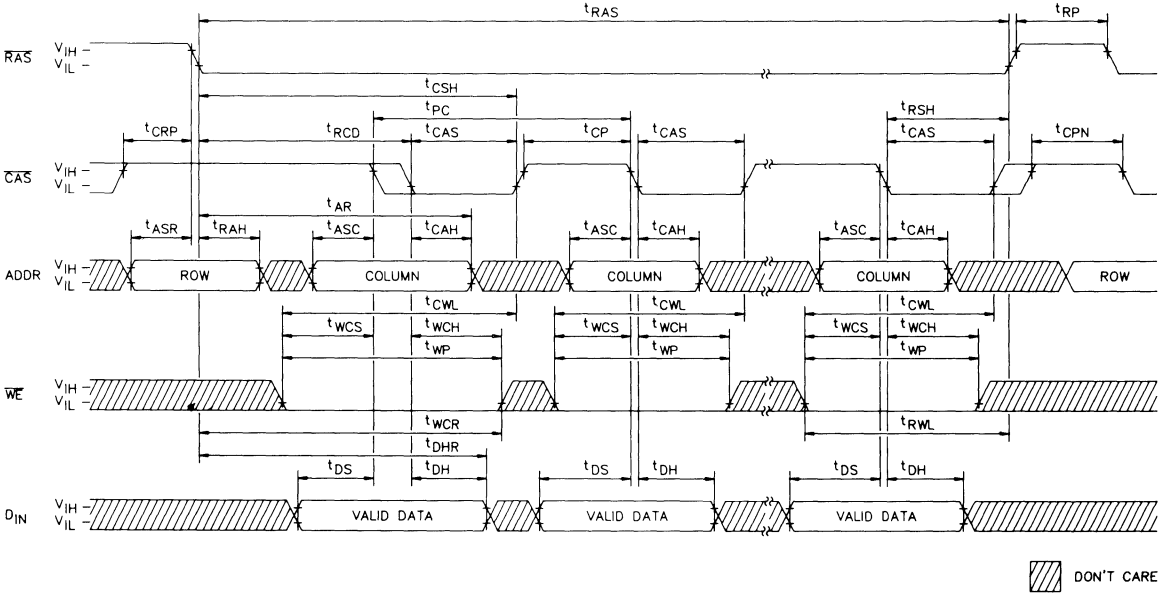
EARLY-WRITE CYCLE



PAGE-MODE READ CYCLE

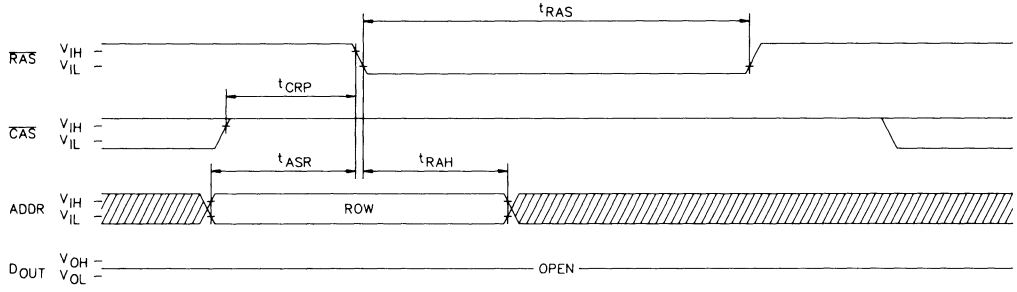


PAGE-MODE EARLY-WRITE CYCLE



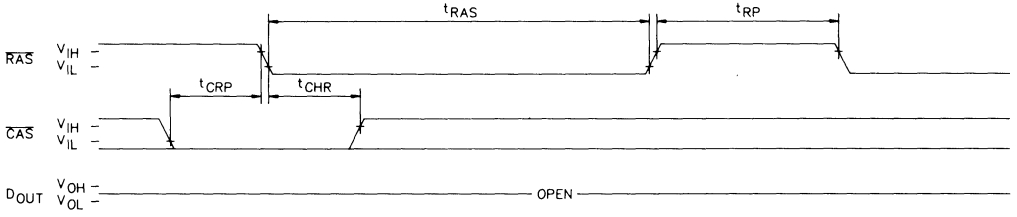
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; and $\overline{WE}$ = DON'T CARE.)



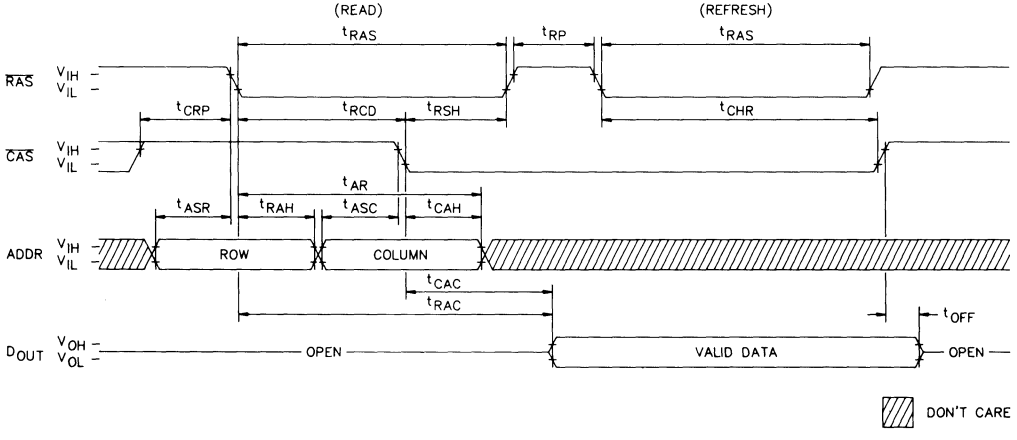
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 $\overline{WE}$, $\overline{OE}$ = DON'T CARE.)



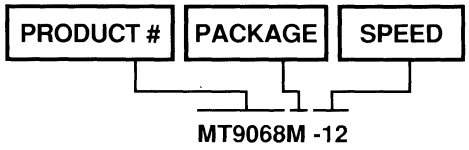
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

64K x 9, 120ns access, Leadless SIMM



The Micron 64K x 9 DRAM module is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance NMOS double-poly process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM MODULES

256K x 4 DRAM

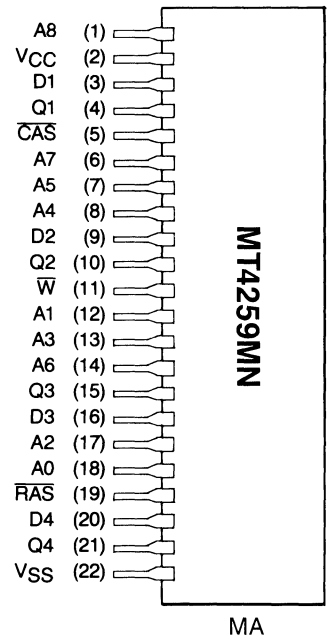
FEATURES

- Industry standard pin-out in a 22-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 60mW standby, 600mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

- Timing
  - 80ns access -8
  - 100ns access -10
  - 120ns access -12
  - 150ns access -15
- Organization
  - 256K x 4 MT4259
- Packages: Leaded 22-pin SIP MN

PIN ASSIGNMENT (Top View)



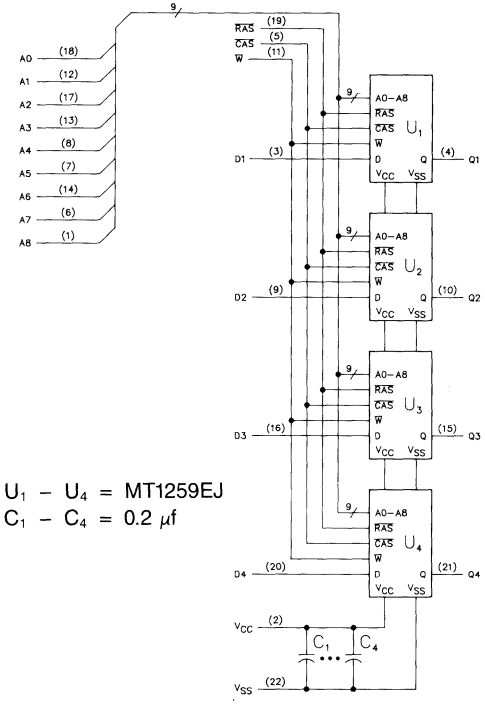
A0-A8	Address Inputs	$\overline{CAS}$	Column Address Strobe
D1 - D4	Data-In	Q1 - Q4	Data-Out
$\overline{RAS}$	Row Address Strobe	$\overline{W}$	Write Enable
Vcc	Power (+5V)	Vss	Ground

GENERAL DESCRIPTION

The MT4259MN is a randomly accessed solid-state memory containing 262,144 bits organized in a x4 configuration. The 16 address bits are entered 8 bits at a time using $\overline{RAS}$ to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. If the $\overline{WE}$ pin goes low prior to $\overline{CAS}$ going low, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined PAGE boundary. Returning $\overline{RAS}$ high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the $\overline{RAS}$ high-time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (Refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



$U_1 - U_4$ = MT1259EJ
$C_1 - C_4$ = 0.2 μf

FUNCTIONAL TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 4 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts	I_I	-40	40	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-40	40	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	20	20	20	20	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	260	220	220	180	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	260	220	220	180	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	220	160	160	140	mA	2
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	260	220	220	180	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8)	C_{I1}		20	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		32	pF	17
Output Capacitance D_{OUT}, D_{IN}	C_O		7	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

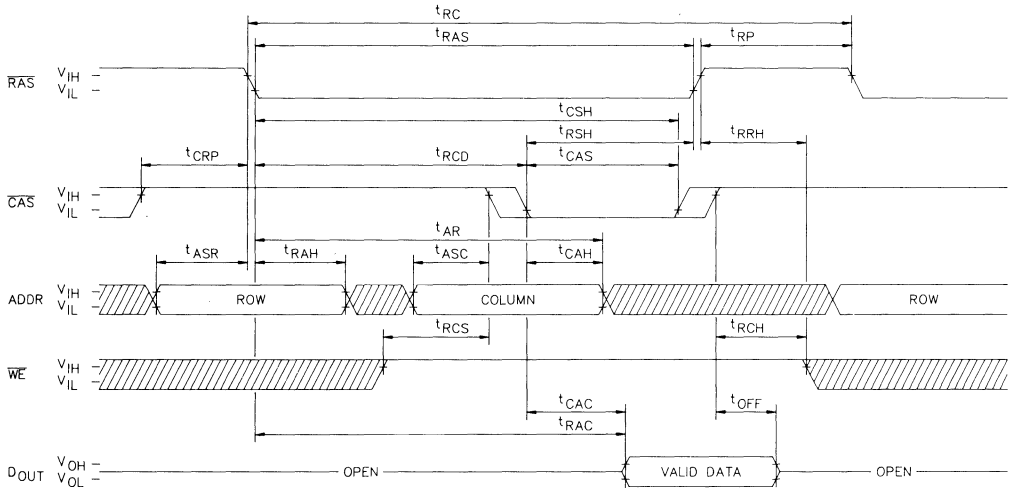
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
RAS pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	60	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		110		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	18
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 16
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	19

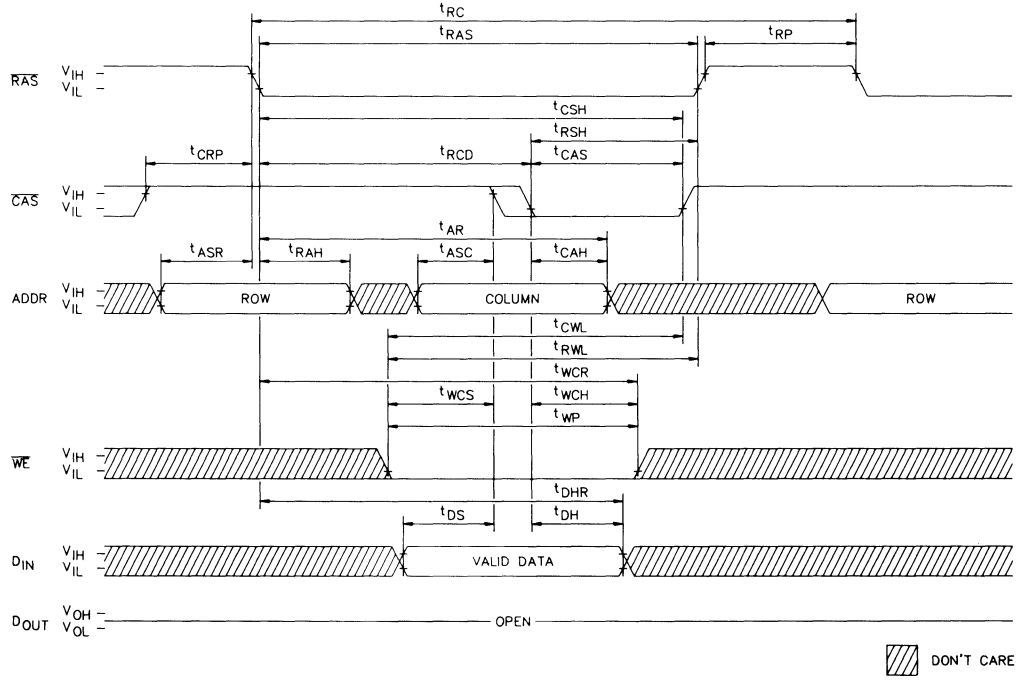
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
18. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set $\overline{WE}$ = LOW.

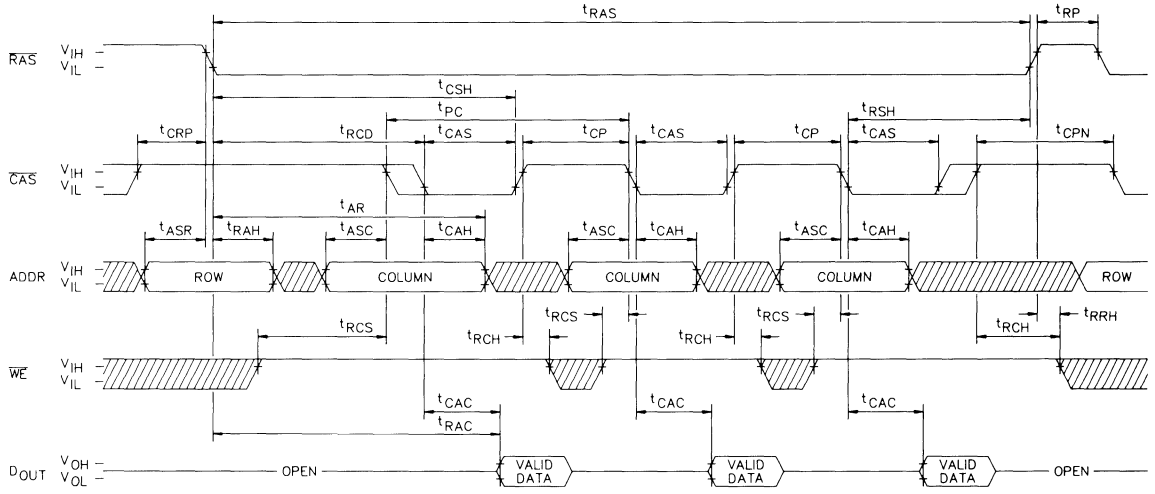
READ CYCLE



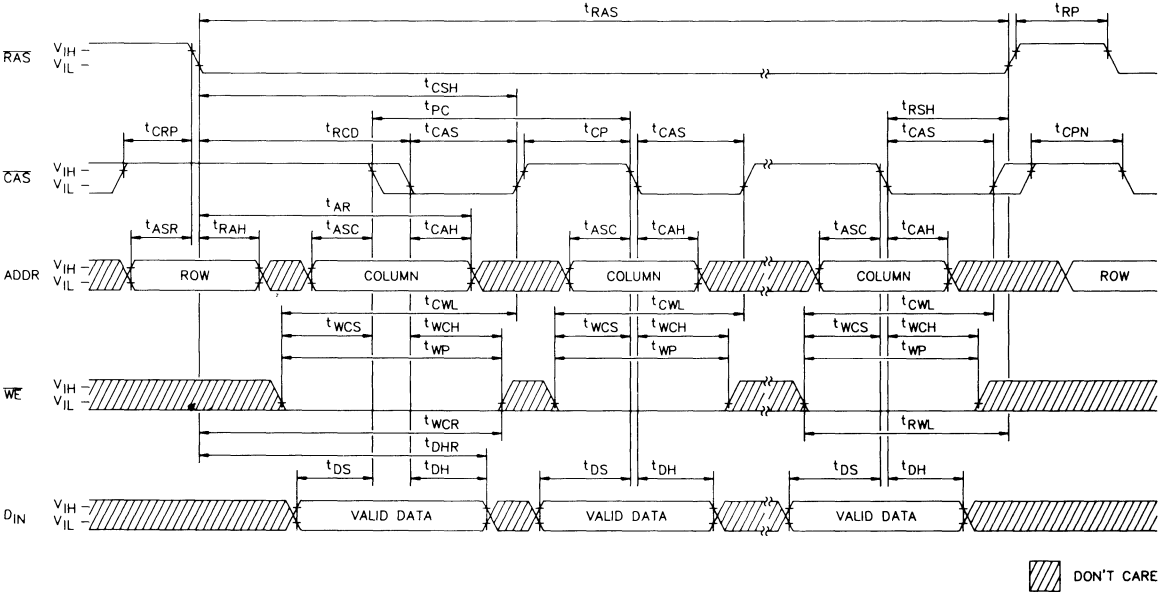
EARLY-WRITE CYCLE



PAGE-MODE READ CYCLE



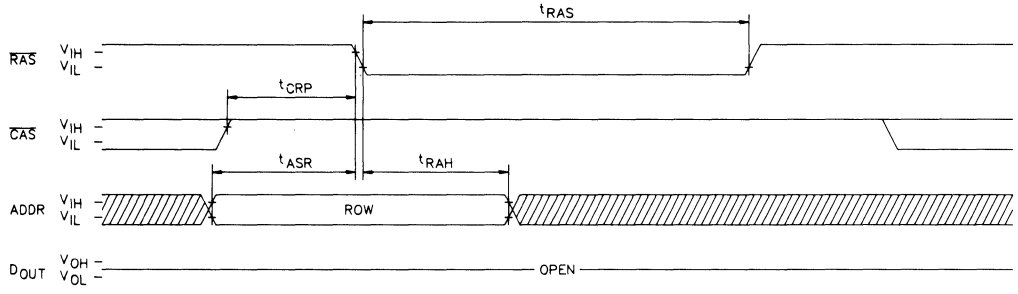
PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

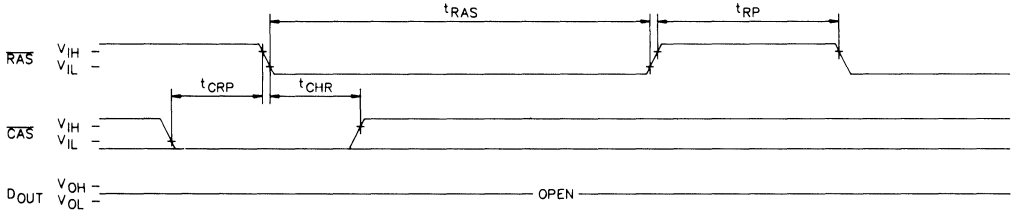
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



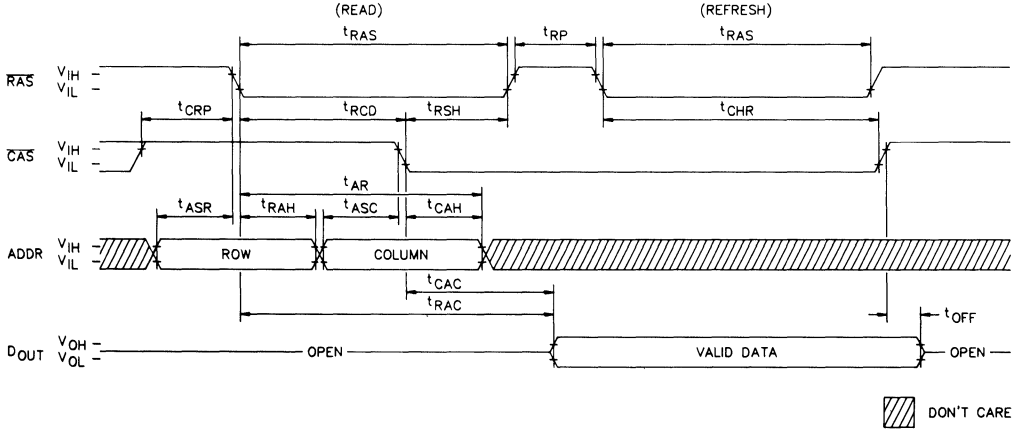
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 $\overline{WE}$, $\overline{OE}$ = DON'T CARE.)



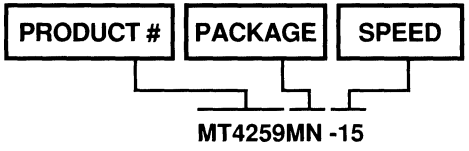
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

256K x 4, 150ns access, Leaded SIP



The Micron 256K x 4 DRAM module is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the NMOS double-poly process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

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DRAM MODULES

256K x 5 DRAM

FEATURES

- Industry standard pin-out in a 24-pin single-in-line memory module
- Low profile (0.415 inch, typical)
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 75mW standby, 750mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

- Timing

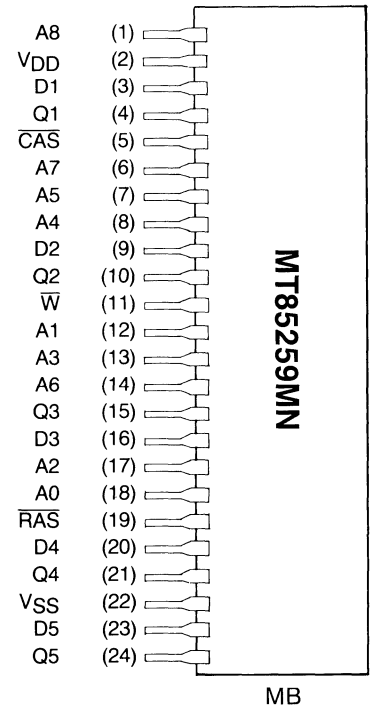
80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15

- Organization

256K x 5	MT85259

- Packages: Leaded 24-pin SIP MN

PIN ASSIGNMENT (Top View)



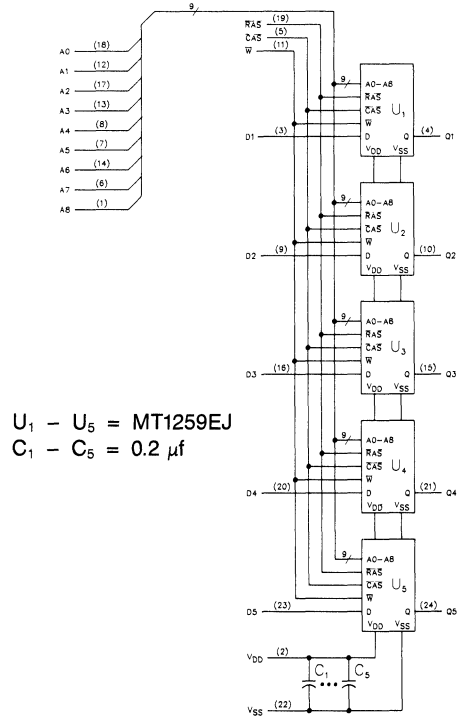
A0-A8	Address Inputs	$\overline{CAS}$	Column Address Strobe
D1 - D5	Data-In	Q1 - Q5	Data-Out
$\overline{RAS}$	Row Address Strobe	$\overline{W}$	Write Enable
VDD	Power (+5V)	Vss	Ground

GENERAL DESCRIPTION

The MT85259MN is a randomly accessed solid-state memory containing 262,144 bits organized in a x5 configuration. The 16 address bits are entered 8 bits at a time using $\overline{RAS}$ to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. If the $\overline{WE}$ pin goes low prior to $\overline{CAS}$ going low, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined PAGE boundary. Returning $\overline{RAS}$ high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the $\overline{RAS}$ high-time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (Refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



$U_1 - U_5$ = MT1259EJ
$C_1 - C_5$ = 0.2 µf

FUNCTIONAL TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 5 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts	I_I	-50	50	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-50	50	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	25	25	25	25	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	325	275	275	225	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	325	275	275	225	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	275	200	200	175	mA	2
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	325	275	275	225	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8)	C_{I1}		25	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		40	pF	17
Output Capacitance D_{OUT}, D_{IN}	C_O		7	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

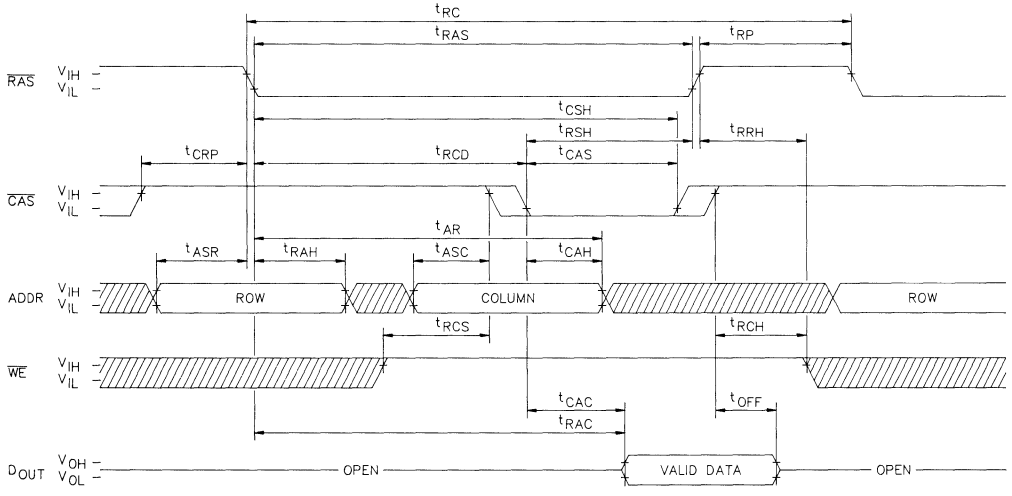
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
RAS pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	60	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		110		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	18
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 16
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	19

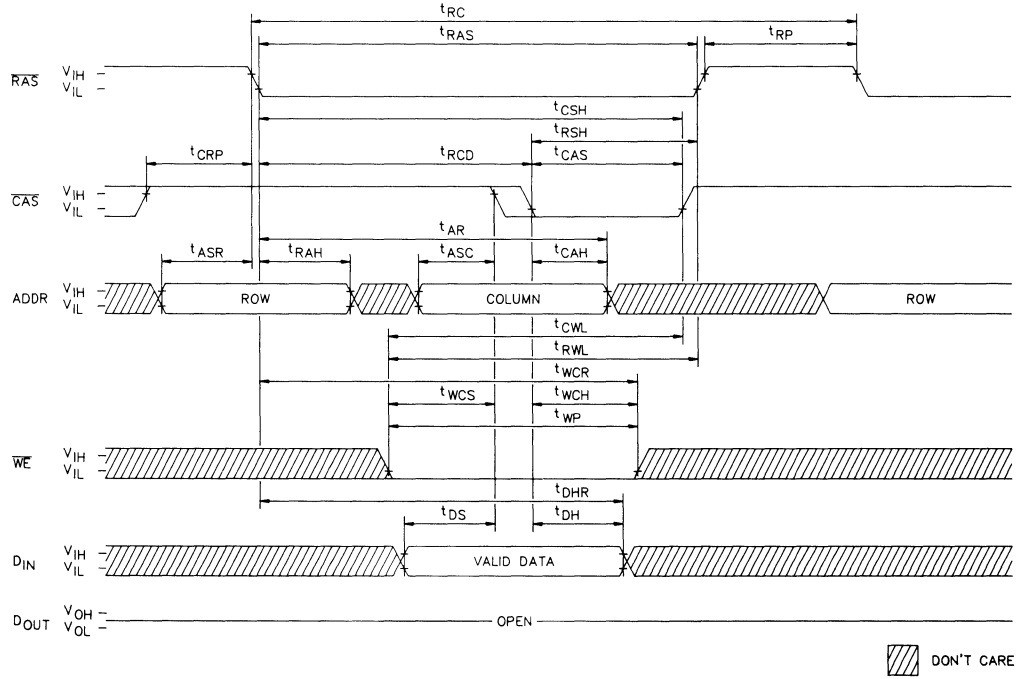
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq {}^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
18. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set $\overline{WE}$ = LOW.

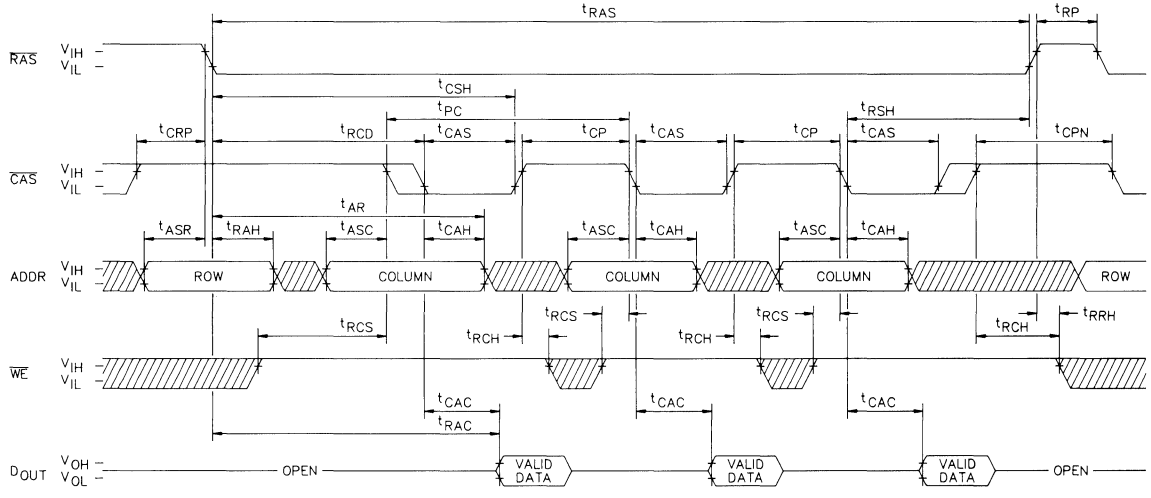
READ CYCLE



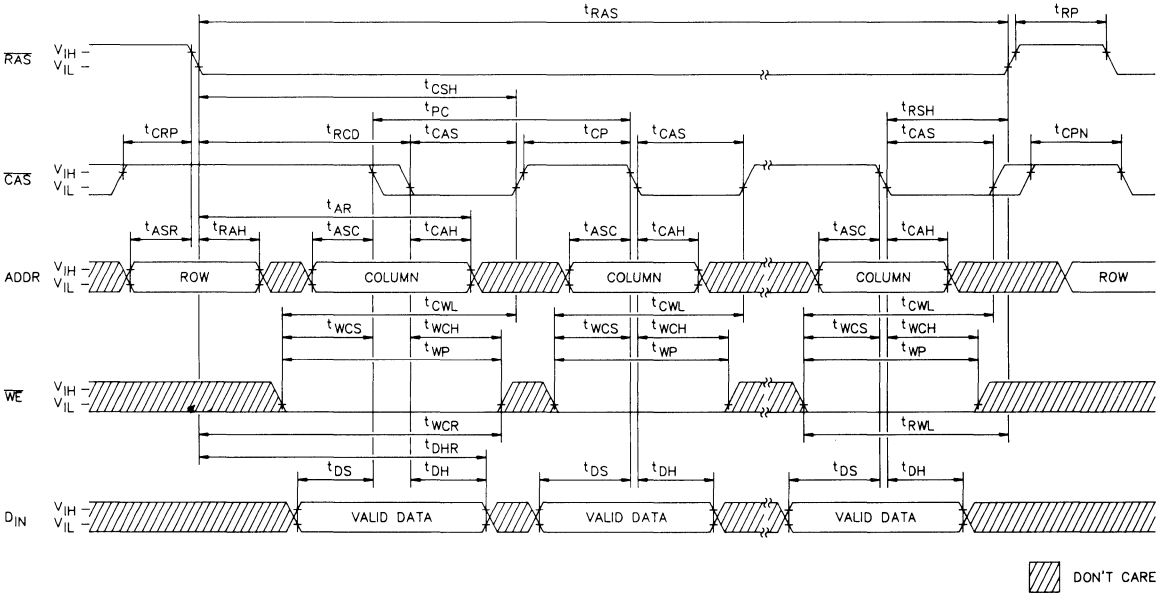
EARLY-WRITE CYCLE



PAGE-MODE READ CYCLE



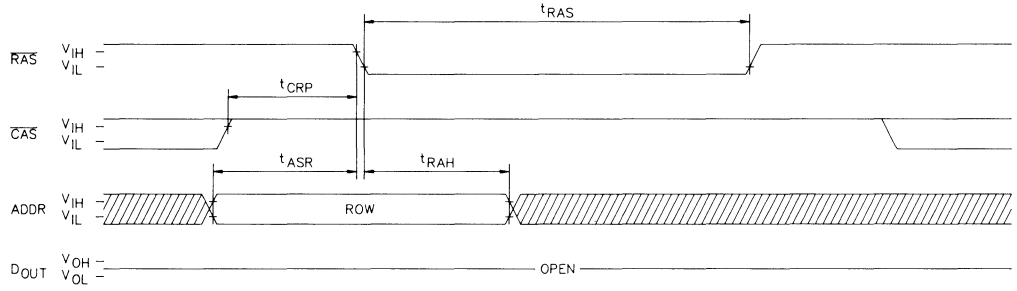
PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

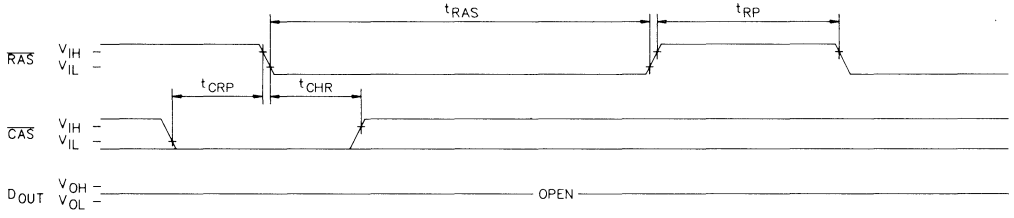
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



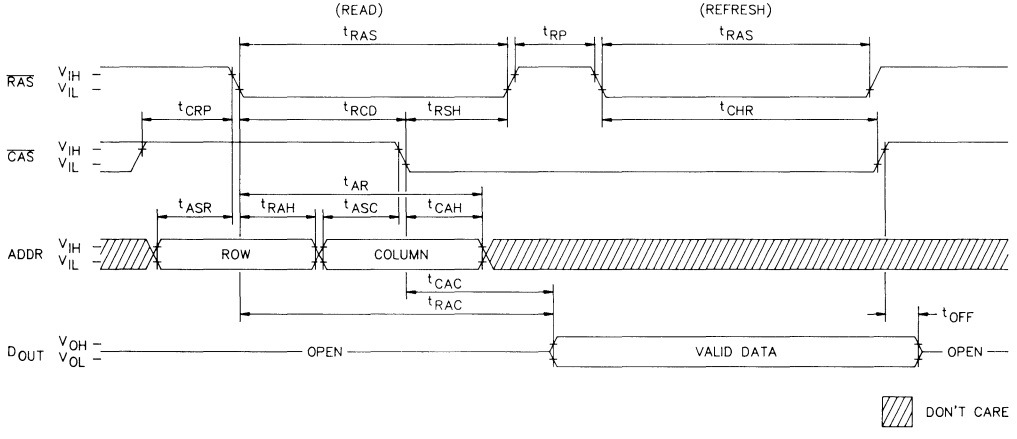
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 $\overline{WE}$, $\overline{OE}$ = DON'T CARE.)



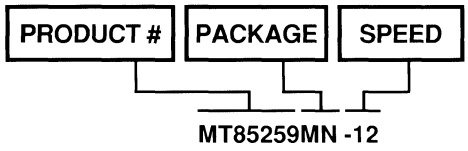
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

256K x 5, 120ns access, Leaded SIP



The Micron 256K x 5 DRAM module is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the NMOS double-poly process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM MODULES

256K x 8 DRAM

FEATURES

- Industry standard pin-out in a 30-pin single-in-line package
- Low profile, double-side mount (0.45 in)
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 135mW standby, 1350mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

- Timing

80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15

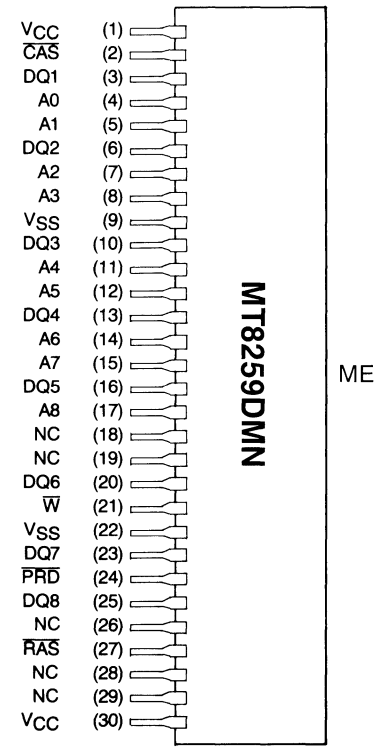
- Organization

256K x 8	MT8259

- Packages: Leaded 30-pin SIP

(low profile)	DMN

PIN ASSIGNMENT (Top View)



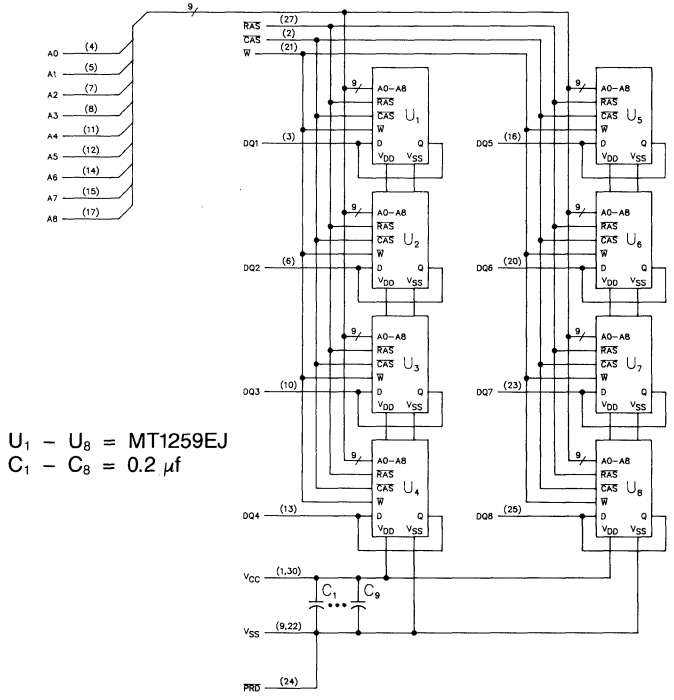
A0-A8	Address Inputs	$\overline{CAS}$	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
$\overline{PRD}$	Presence Detect	Q9	Data-Out
$\overline{RAS}$	Row Address Strobe	$\overline{W}$	Write Enable
Vcc	Power (+5V)	Vss	Ground

GENERAL DESCRIPTION

The MT8259DMN is a randomly accessed solid-state memory containing 262,144 bits organized in a x8 configuration. The 18 address bits are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes low prior to $\overline{CAS}$ going low, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined PAGE boundary. Returning $\overline{RAS}$ high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the $\overline{RAS}$ high-time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (Refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



$U_1 - U_8$ = MT1259EJ
$C_1 - C_8$ = 0.2 μf

FUNCTIONAL TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts	I_I	-80	80	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-80	80	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	40	40	40	40	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	500	440	440	360	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	520	440	440	360	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	440	320	320	280	mA	2
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	520	440	440	360	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8)	C_{I1}		40	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		64	pF	17
Output Capacitance D_{OUT}, D_{IN}	C_O		12	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

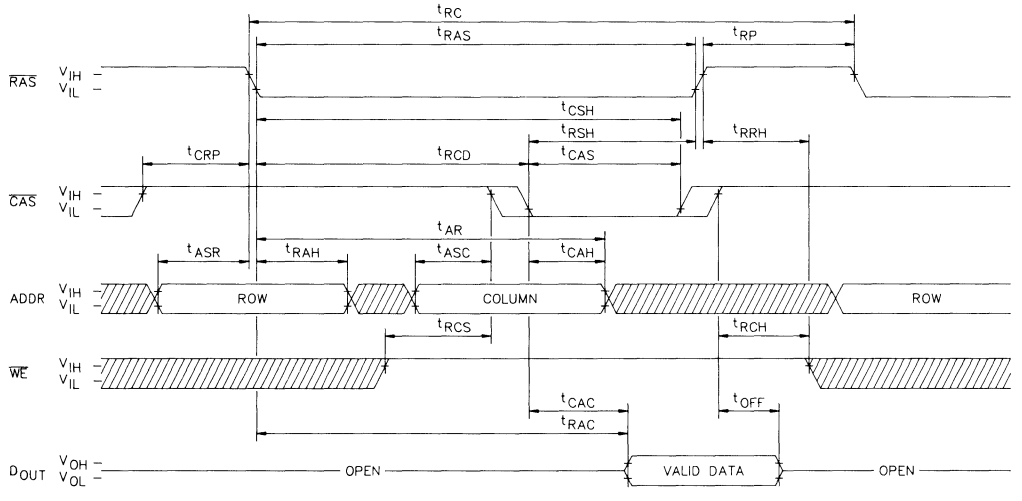
(Notes: 3, 4, 5, 10, 11, 17, 18) ($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
RAS pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	60	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		110		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	18
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 16
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	19

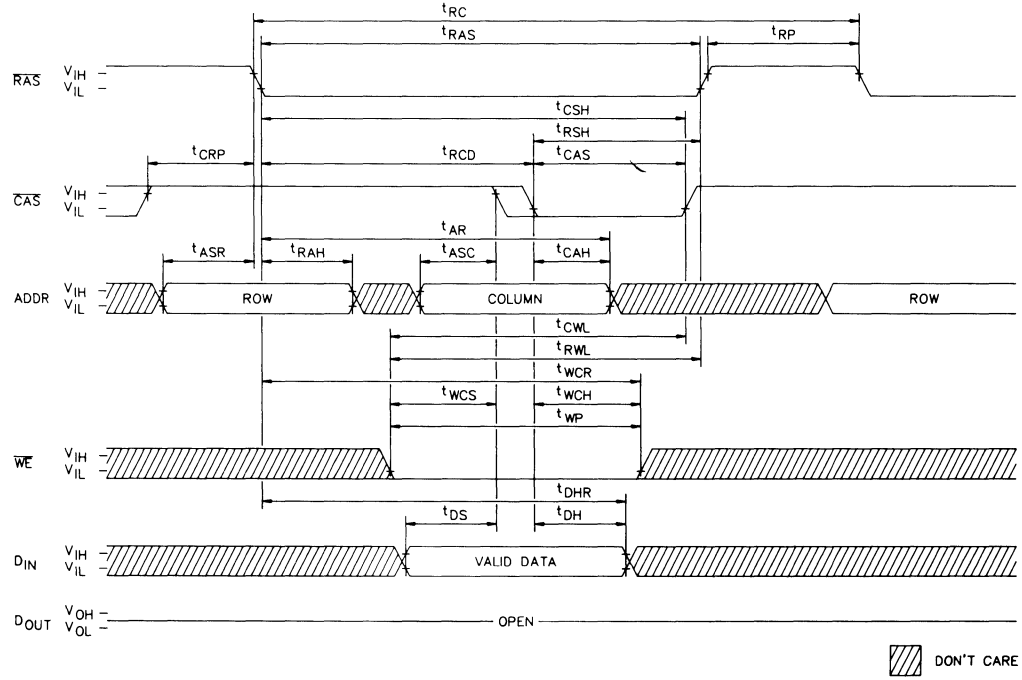
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq {}^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
18. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set $\overline{WE}$ = LOW.

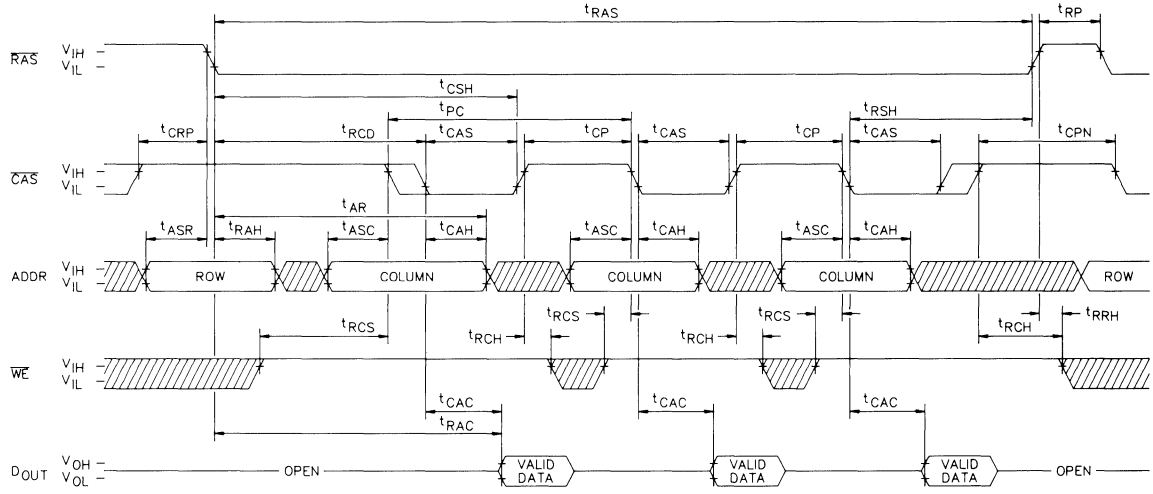
READ CYCLE



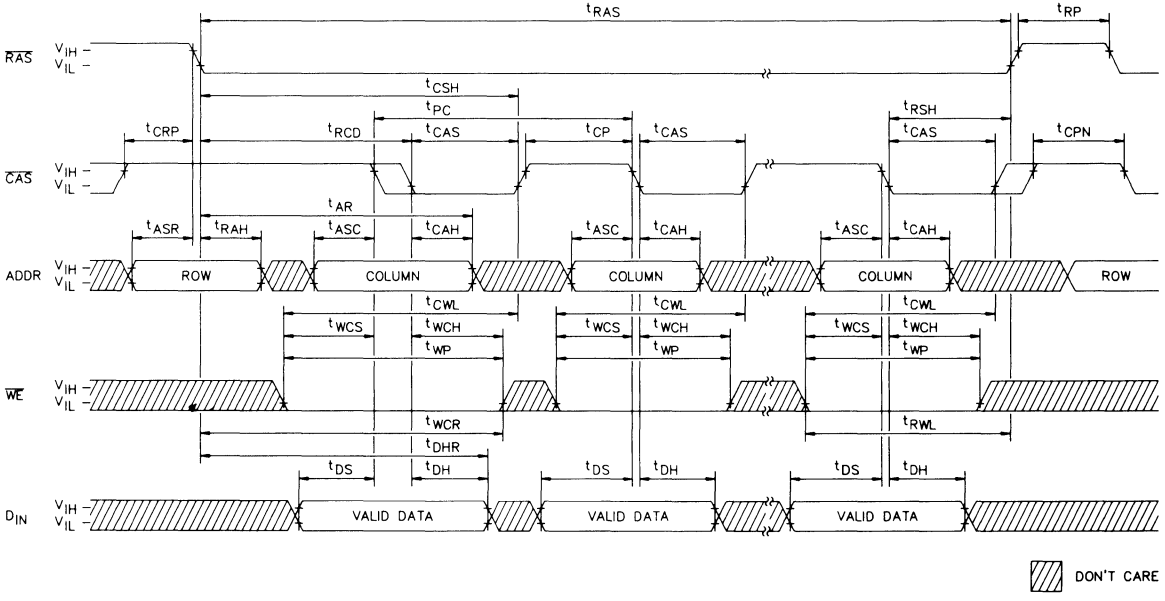
EARLY-WRITE CYCLE



PAGE-MODE READ CYCLE



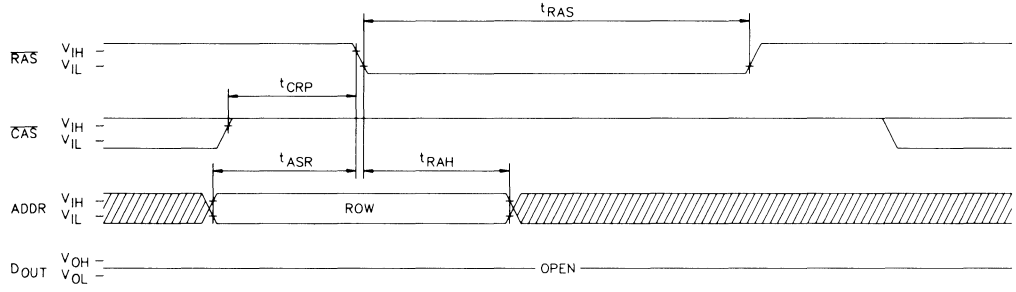
PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

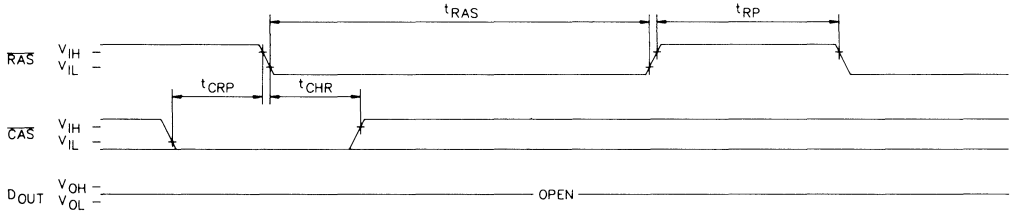
$\overline{RAS}$-BEFORE-$\overline{CAS}$ REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



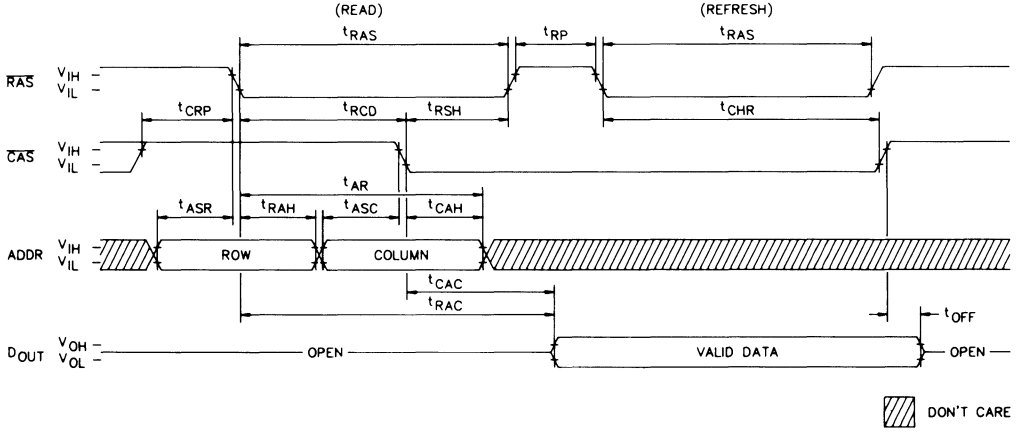
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 $\overline{WE}$, $\overline{OE}$ = DON'T CARE.)



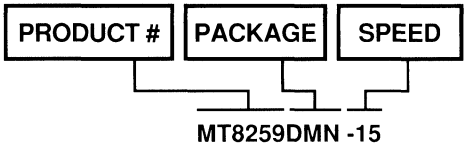
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

256K x 8, 150ns access, Leaded SIP



The Micron 256K x 8 DRAM module is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the NMOS double-poly process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM MODULES

256K x 8 DRAM

FEATURES

- Industry standard pin-out in a 30-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 120mW standby, 1200mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

- Timing

80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15

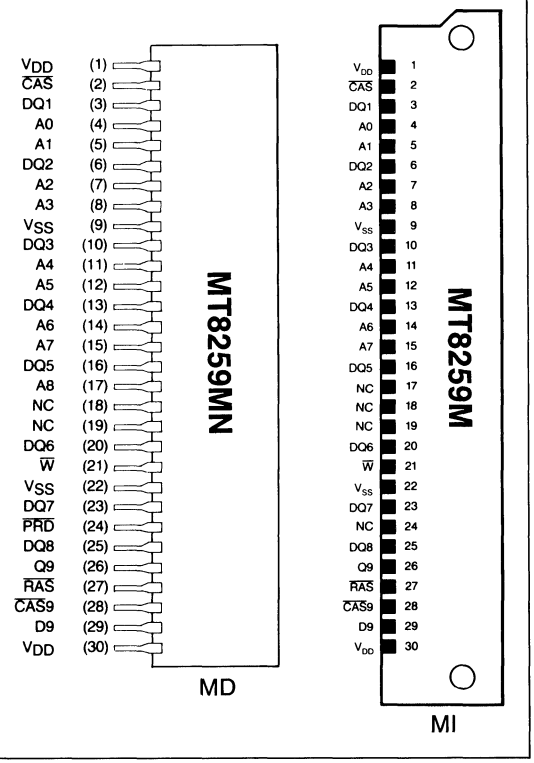
- Organization

256K x 8	MT8259

- Packages:

Leadless 30-pin SIMM	M
Leaded 30-pin SIP	MN

PIN ASSIGNMENT (Top View)



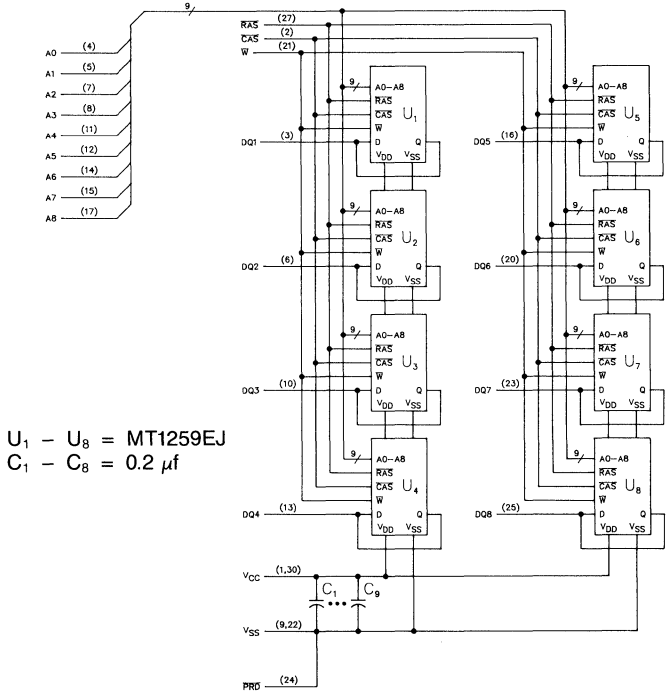
A0-A8	Address Inputs	$\overline{CAS}$	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
$\overline{PRD}$	Presence Detect	Q9	Data-Out
$\overline{RAS}$	Row Address Strobe	$\overline{W}$	Write Enable
Vcc	Power (+5V)	Vss	Ground

GENERAL DESCRIPTION

The MT8259M/MN is a randomly accessed solid-state memory containing 262,144 bits organized in a x8 configuration. The 18 address bits are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes low prior to $\overline{CAS}$ going low, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined PAGE boundary. Returning $\overline{RAS}$ high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the $\overline{RAS}$ high-time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (Refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



$U_1 - U_8$ = MT1259EJ
$C_1 - C_8$ = 0.2 μf

FUNCTIONAL TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$) (V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-80	80	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-80	80	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	40	40	40	40	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	520	440	440	360	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	520	440	440	360	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	440	320	320	280	mA	2
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	520	440	440	360	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8)	C_{I1}		40	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		64	pF	17
Output Capacitance D_{OUT}, D_{IN}	C_O		12	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

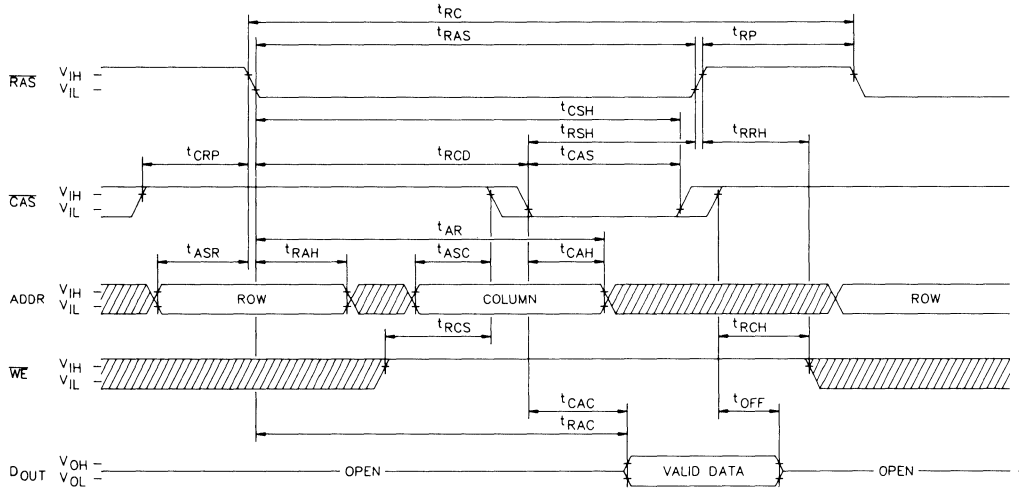
(Notes: 3, 4, 5, 10, 11, 17, 18) ($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	60	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		110		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	18
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 16
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	19

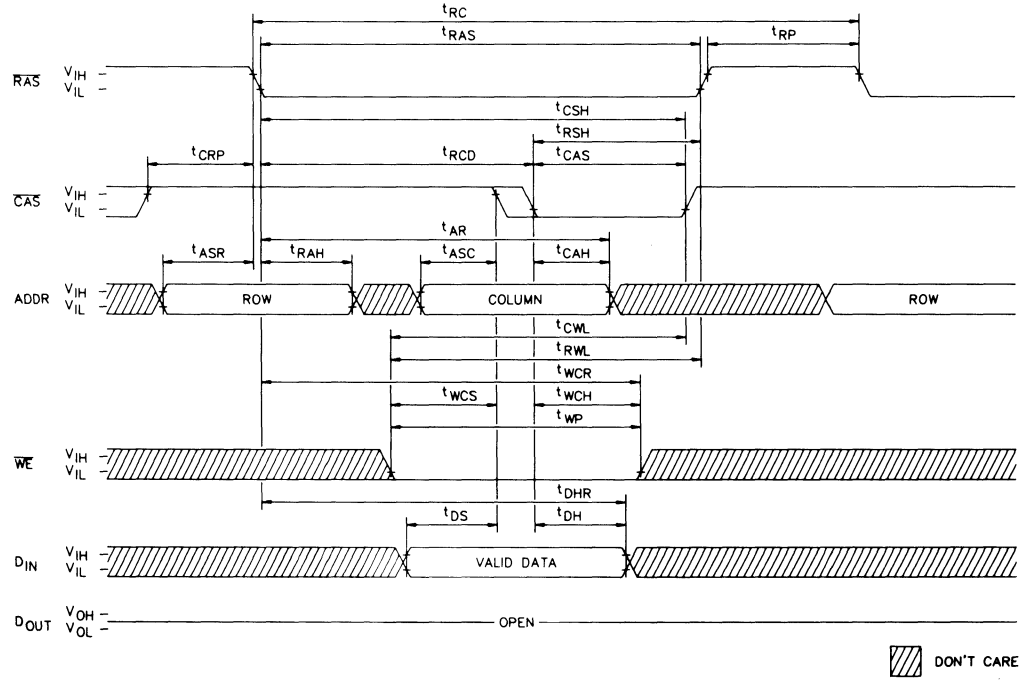
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq {}^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
18. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set $\overline{WE}$ = LOW.

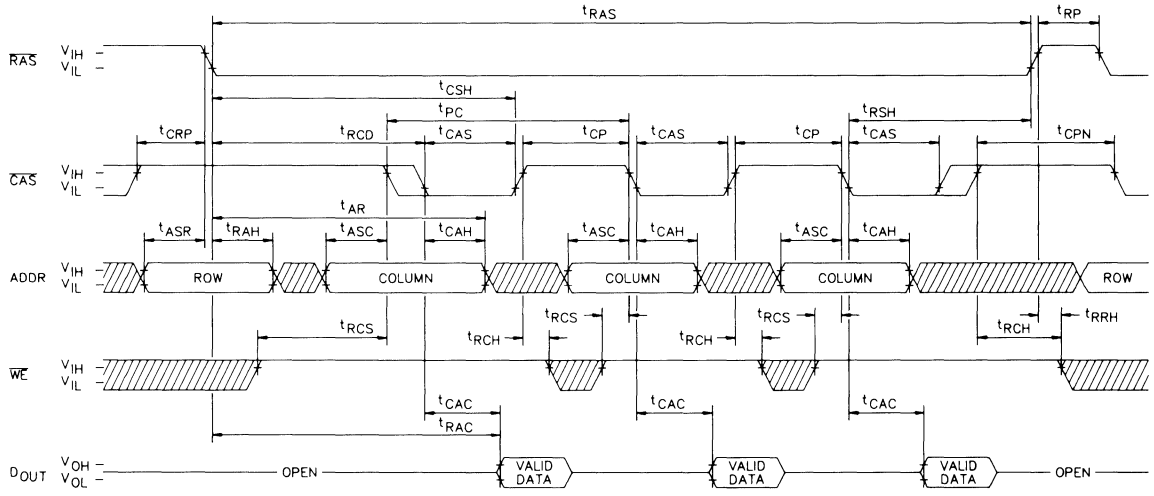
READ CYCLE



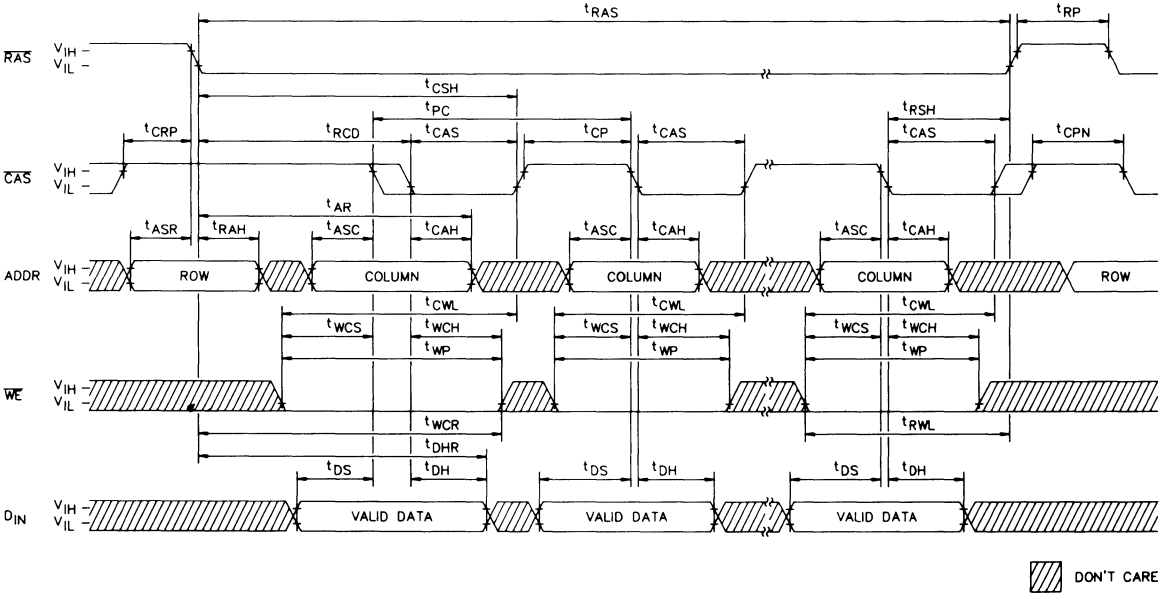
EARLY-WRITE CYCLE



PAGE-MODE READ CYCLE



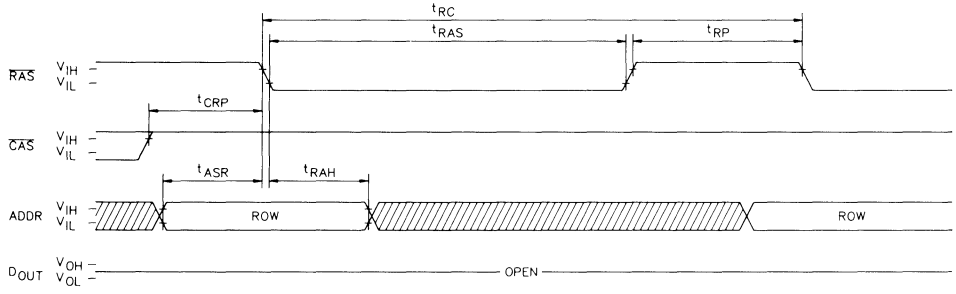
PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

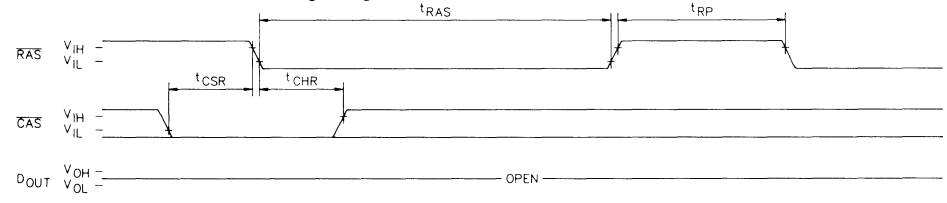
$\overline{RAS}$-BEFORE-$\overline{CAS}$ REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



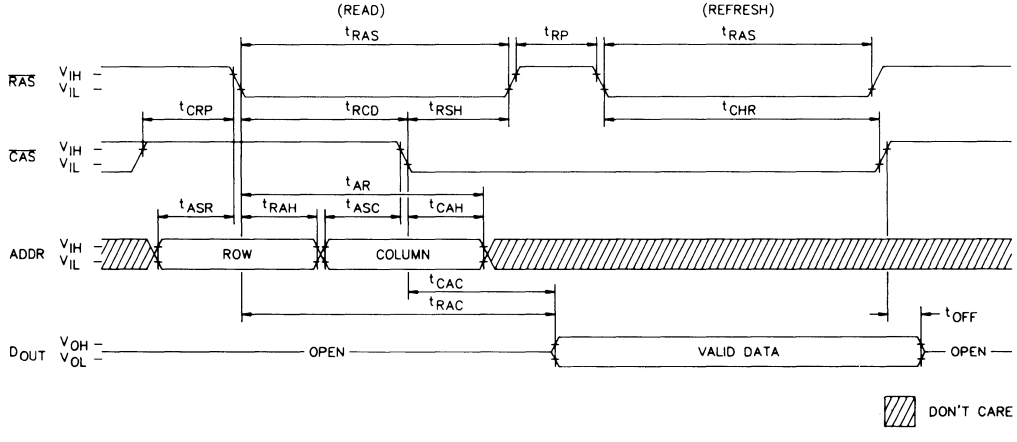
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 $\overline{WE}$, $\overline{OE}$ = DON'T CARE.)



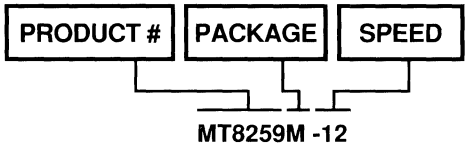
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

256K x 8, 120ns access, Leaded SIP



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DRAM MODULES

256K x 9 DRAM

FEATURES

- Industry standard pin-out in a 30-pin single-in-line package (SIP)
- Low profile, double-side mount (0.45 in)
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible.
- Low power, 135mW standby, 1350mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

- Timing

80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15

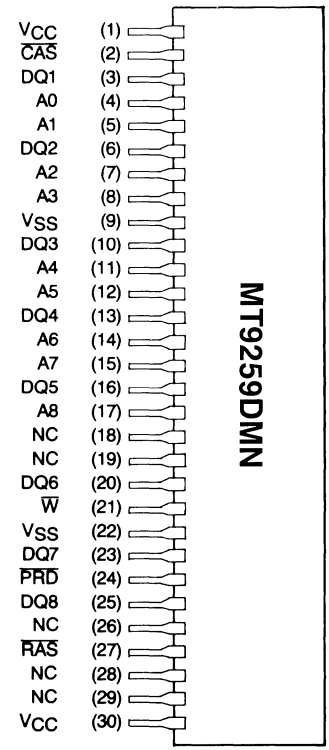
- Organization

256K x 9	MT9259

- Packages: Leaded 30-pin SIP

(low profile)	DMN

PIN ASSIGNMENT (Top View)



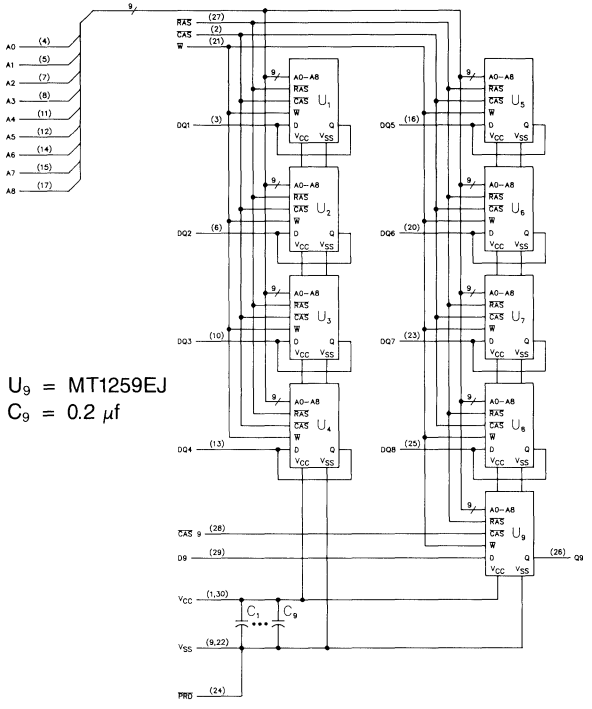
A0-A8	Address Inputs	$\overline{CAS}$, $\overline{CAS9}$	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
$\overline{PRD}$	Presence Detect	Q9	Data-Out
$\overline{RAS}$	Row Address Strobe	$\overline{W}$	Write Enable
Vcc	Power (+5V)	Vss	Ground

GENERAL DESCRIPTION

The MT9259DMN is a randomly accessed solid-state memory containing 262,144 bits organized in a x9 configuration. The 18 address bits are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes low prior to $\overline{CAS}$ going low, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined PAGE boundary. Returning $\overline{RAS}$ high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the $\overline{RAS}$ high-time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (Refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



$U_1 - U_9 = MT1259EJ$
$C_1 - C_9 = 0.2\ \mu f$

FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 9 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$) (V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-90	90	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-90	90	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	45	45	45	45	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	585	495	495	405	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	585	495	495	405	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	495	360	360	315	mA	2
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	585	495	495	405	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8)	C_{I1}		45	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		72	pF	17
Output Capacitance D_{OUT}, D_{IN}	C_O		12	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

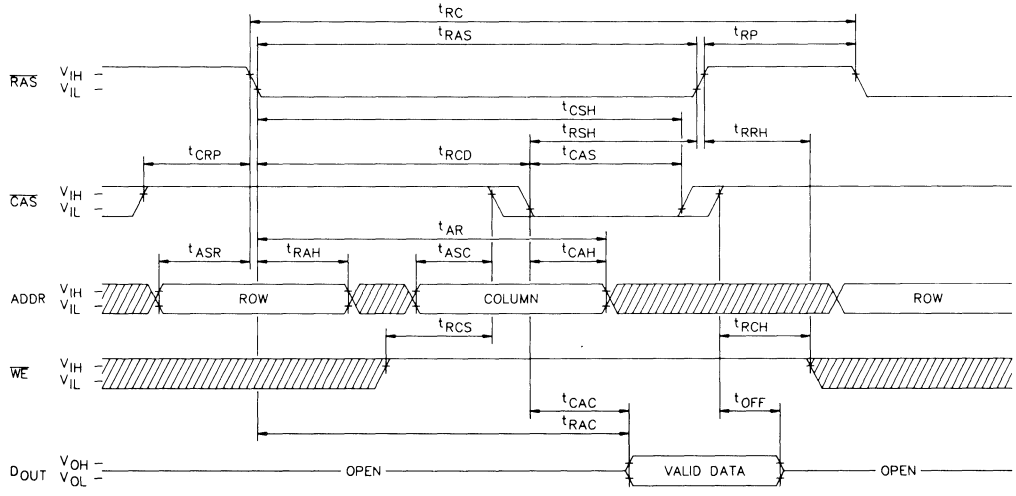
(Notes: 3, 4, 5, 10, 11, 17, 18) ($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
RAS pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	60	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		110		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	18
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 16
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	19

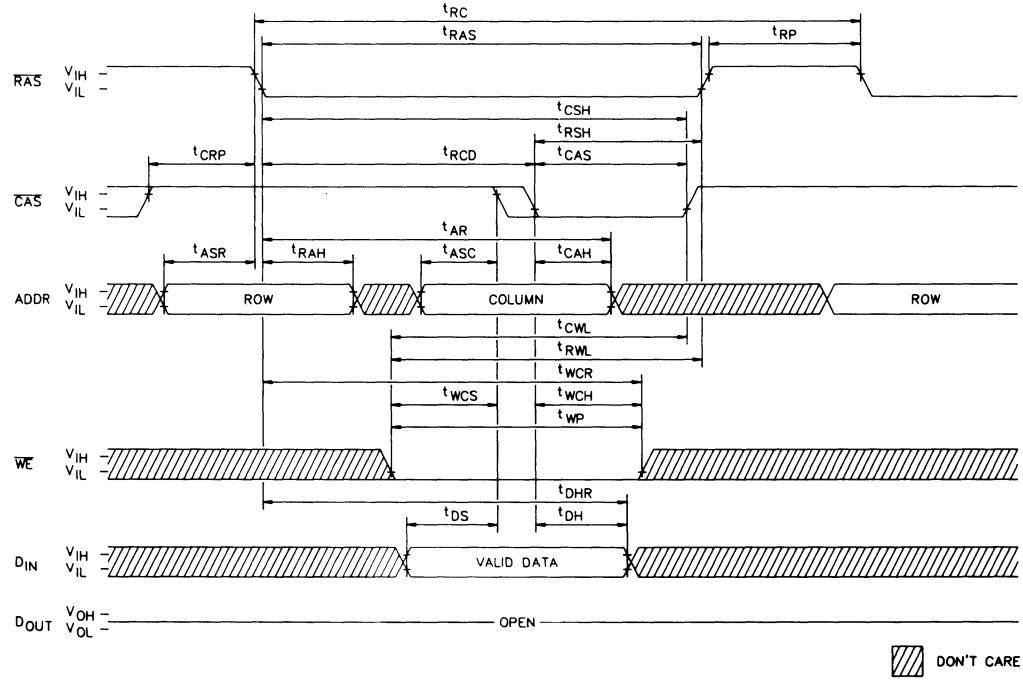
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq {}^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
18. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set $\overline{WE}$ = LOW.

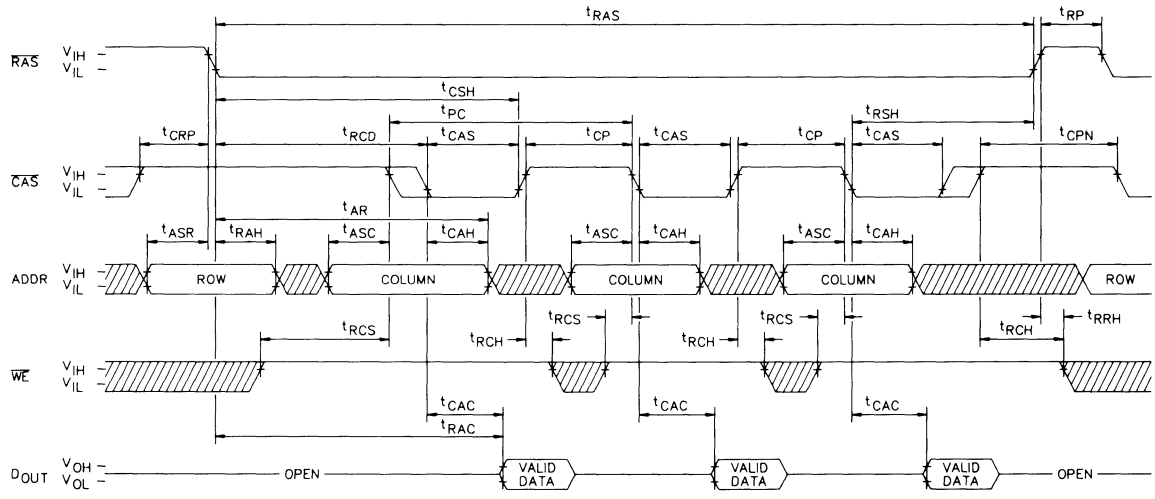
READ CYCLE



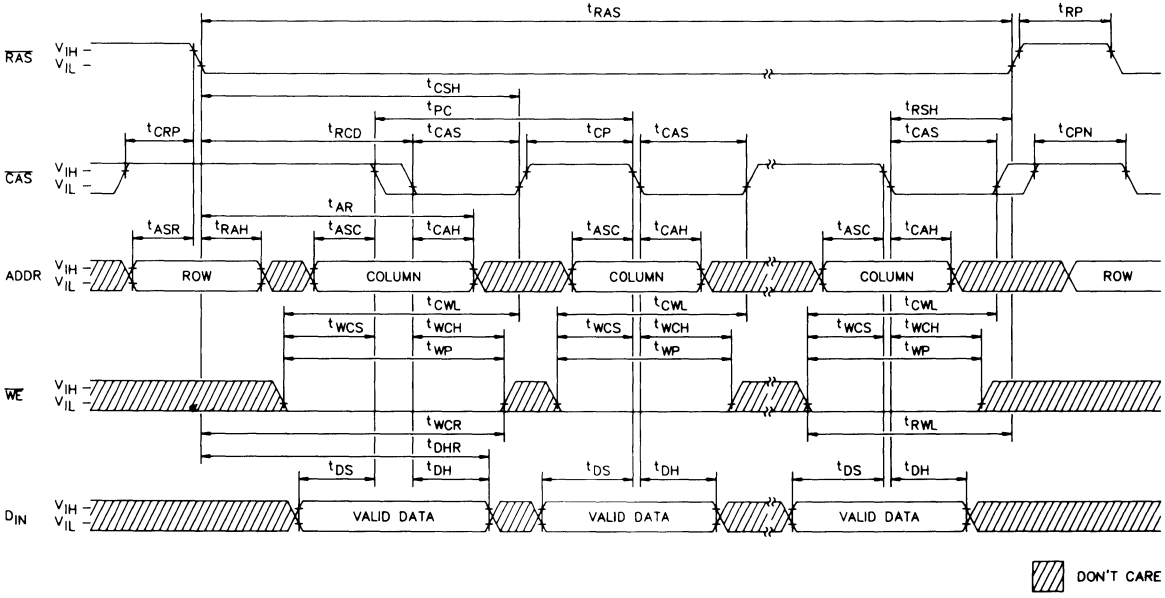
EARLY-WRITE CYCLE



PAGE-MODE READ CYCLE



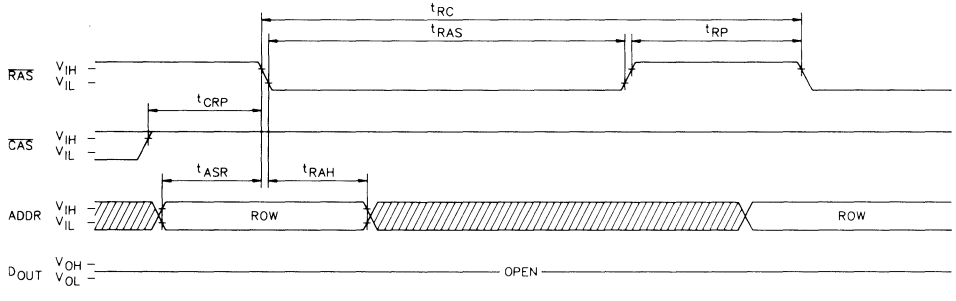
PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

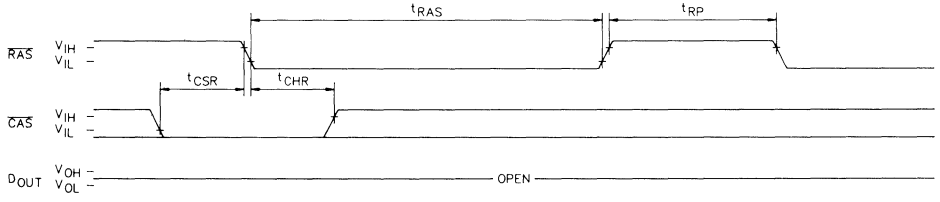
$\overline{RAS}$-BEFORE-$\overline{CAS}$ REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



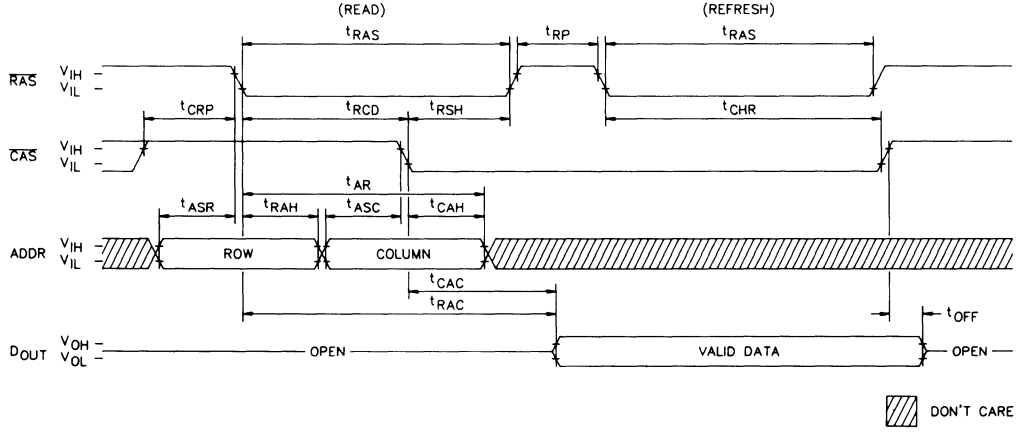
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 $\overline{WE}$, $\overline{OE}$ = DON'T CARE.)



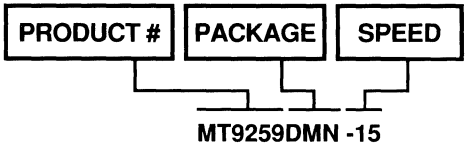
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

256K x 9, 150ns access, Leaded SIP



The Micron 256K x 9 DRAM module is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the NMOS double-poly process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM MODULES

256K x 9 DRAM

FEATURES

- Industry standard pin-out in a 30-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 135mW standby, 1350mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

- Timing

80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15

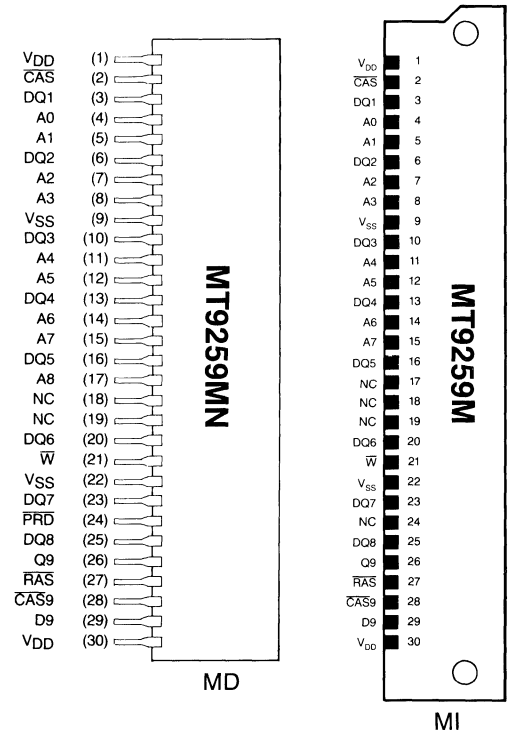
- Organization

256K x 9	MT9259

- Packages:

Leadless 30-pin SIMM	M
Leaded 30-pin SIP	MN

PIN ASSIGNMENT (Top View)



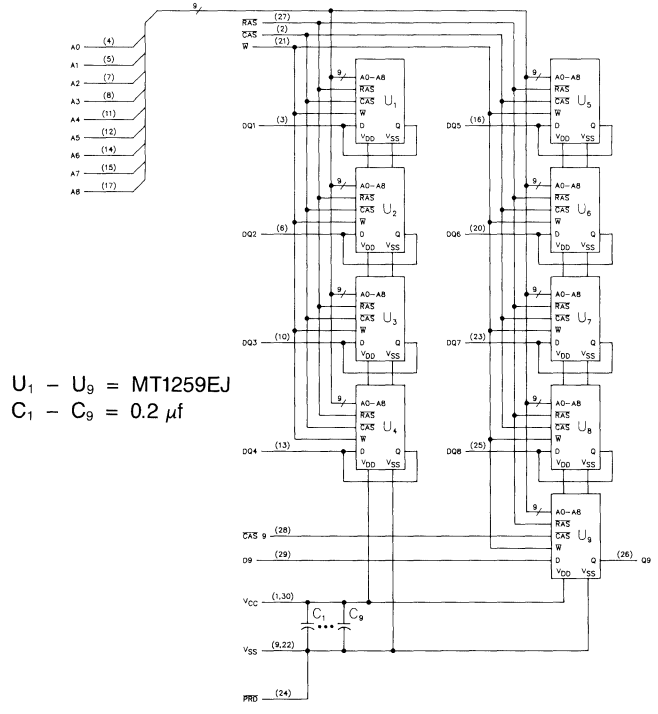
A0-A8	Address Inputs	$\overline{CAS}$ $\overline{CAS9}$	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
$\overline{PRD}$	Presence Detect	Q9	Data-Out
$\overline{RAS}$	Row Address Strobe	$\overline{W}$	Write Enable
Vcc	Power (+5V)	Vss	Ground

GENERAL DESCRIPTION

The MT9259M/MN is a randomly accessed solid-state memory containing 262,144 bits organized in a x9 configuration. The 18 address bits are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes low prior to $\overline{CAS}$ going low, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined PAGE boundary. Returning $\overline{RAS}$ high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the $\overline{RAS}$ high-time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (Refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 msec (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



$U_1 - U_9$ = MT1259EJ
$C_1 - C_9$ = 0.2 μf

FUNCTIONAL TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 9 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$) (V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-90	90	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-90	90	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	45	45	45	45	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	585	495	495	405	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	585	495	495	405	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	495	360	360	315	mA	2
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	585	495	495	405	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8)	C_{I1}		45	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		72	pF	17
Output Capacitance D_{OUT}, D_{IN}	C_O		12	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

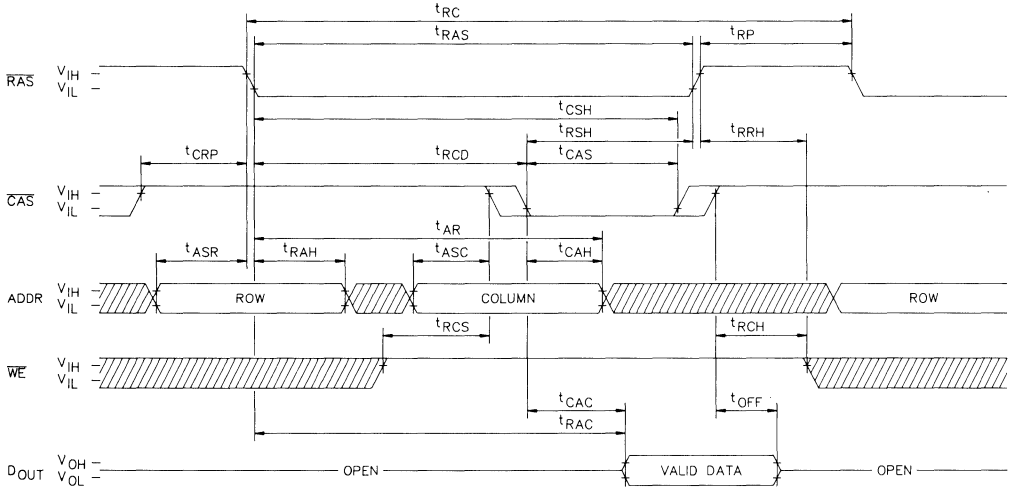
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		195		230		260		ns	6, 7
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
RAS pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	60	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		110		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	18
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	19

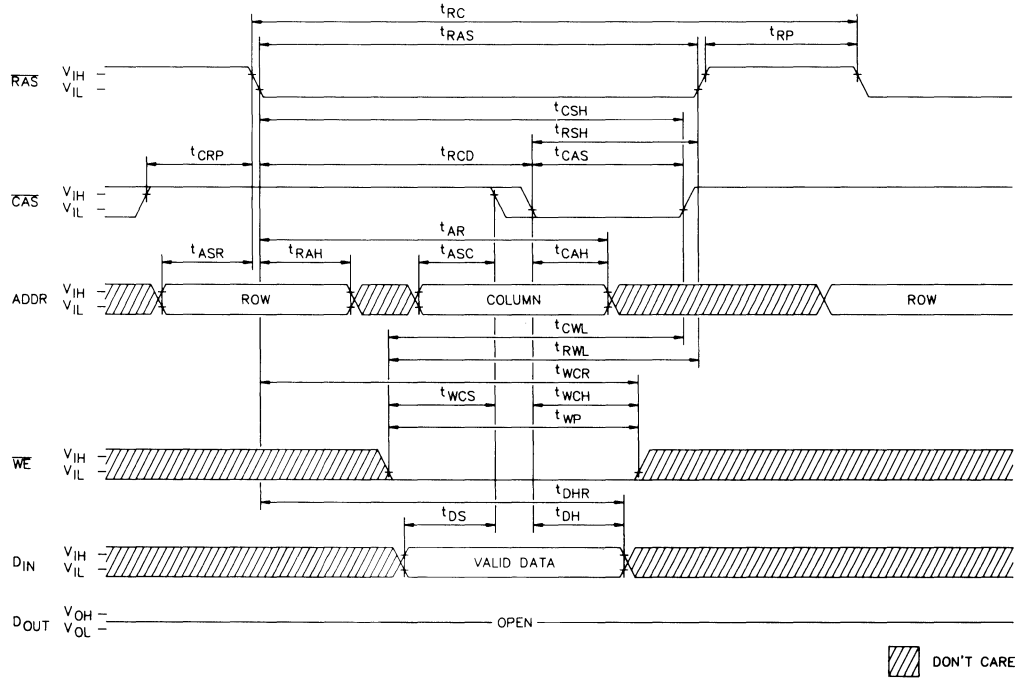
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^{t}RCD < {}^{t}RCD$ (max). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \geq {}^{t}RCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (max) limit ensures that ^{t}RAC (max) can be met. ^{t}RCD (max) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (max) limit, then access time is controlled exclusively by ^{t}CAC.
14. ^{t}RCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
18. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^{t}CP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case set $\overline{WE}$ = LOW.

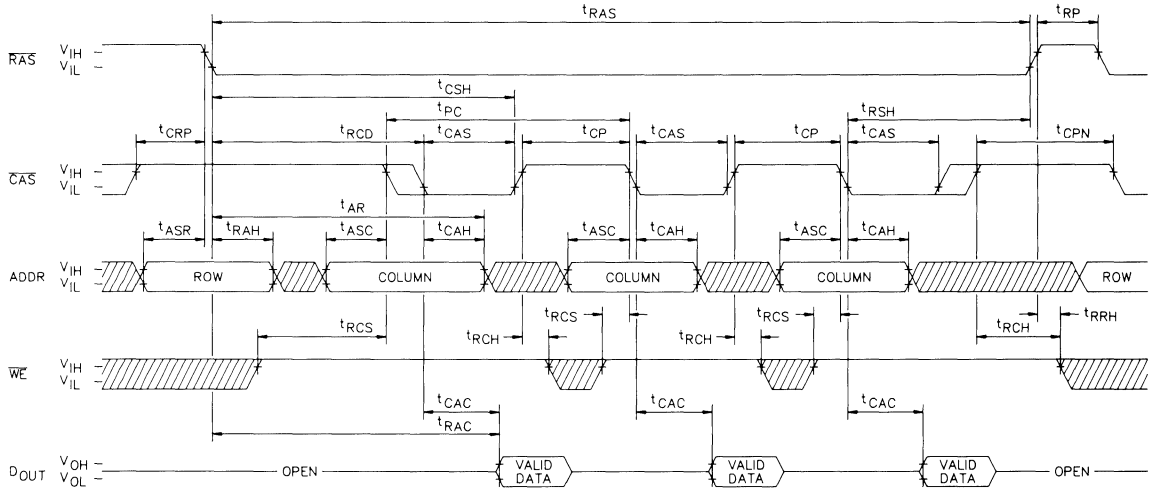
READ CYCLE



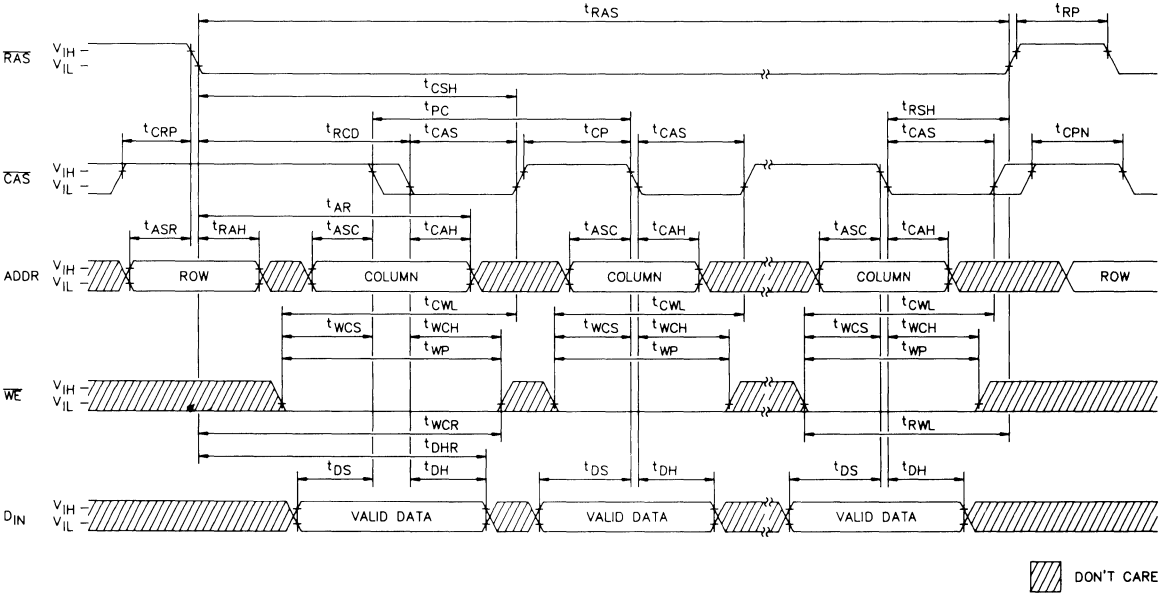
EARLY-WRITE CYCLE



PAGE-MODE READ CYCLE

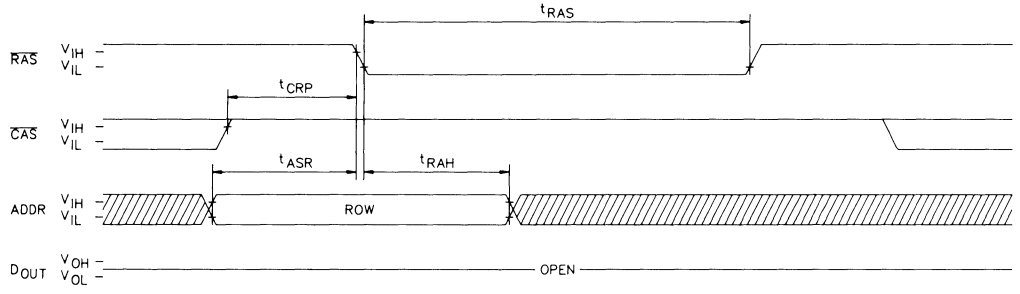


PAGE-MODE EARLY-WRITE CYCLE



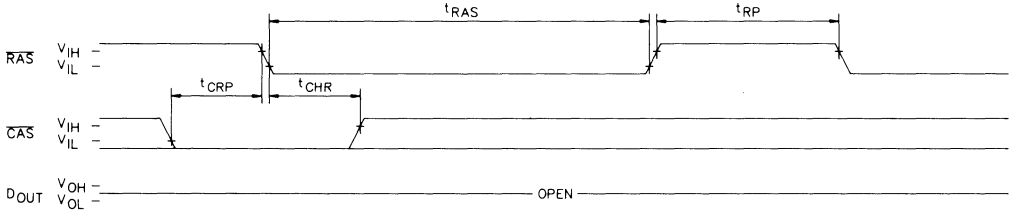
$\overline{RAS}$-BEFORE-$\overline{CAS}$ REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



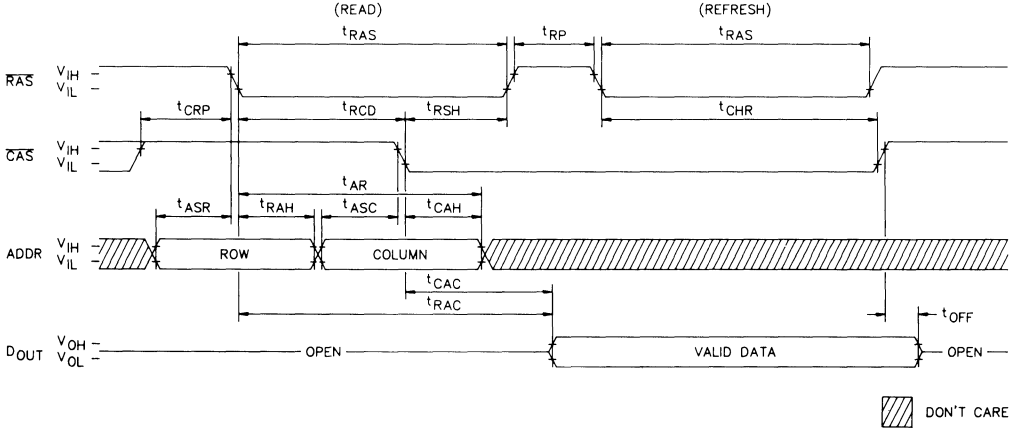
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 $\overline{WE}$, $\overline{OE}$ = DON'T CARE.)



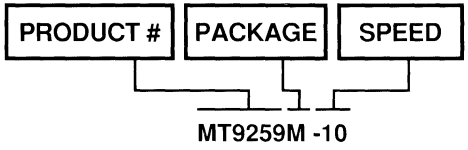
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

256K x 9, 100ns access, Leadless SIP



The Micron 256K x 9 DRAM module is functionally equivalent to other manufacturers' product meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the NMOS double-poly process. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply range, temperature and refresh than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM MODULES

256K x 36 DRAM

PAGE MODE

FEATURES

- Industry standard pin-out in a 72-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 100mW standby, 2000mW active, typical.
- On-board power supply decoupling capacitors (0.2µf) for low noise.
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden.
- 512 cycle refresh distributed across 8ms.
- Optional Fast Page Mode.

OPTIONS MARKING

- Timing
  - 100ns access -10
  - 120ns access -12
  - 150ns access -15
- Organization
  - 256K x 36 MT8C3656
- Packages: Leadless 72-pin SIMM M
  - Leaded 72-pin SIP MN

A0-A8	Address Inputs	$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
DQ0-DQ35	Data-In/Data-Out	PRD0-PRD3	Presence Detect
$\overline{W}$	Write Enable	$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
NC	No Connection	VDD	Power (+5V)
Vss	Ground		

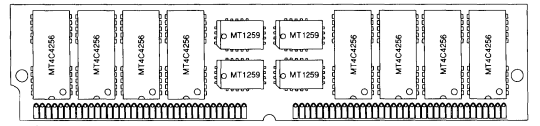
GENERAL DESCRIPTION

The MT8C3656 is a randomly accessed solid-state memory containing 262,144 bits organized in a x36 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

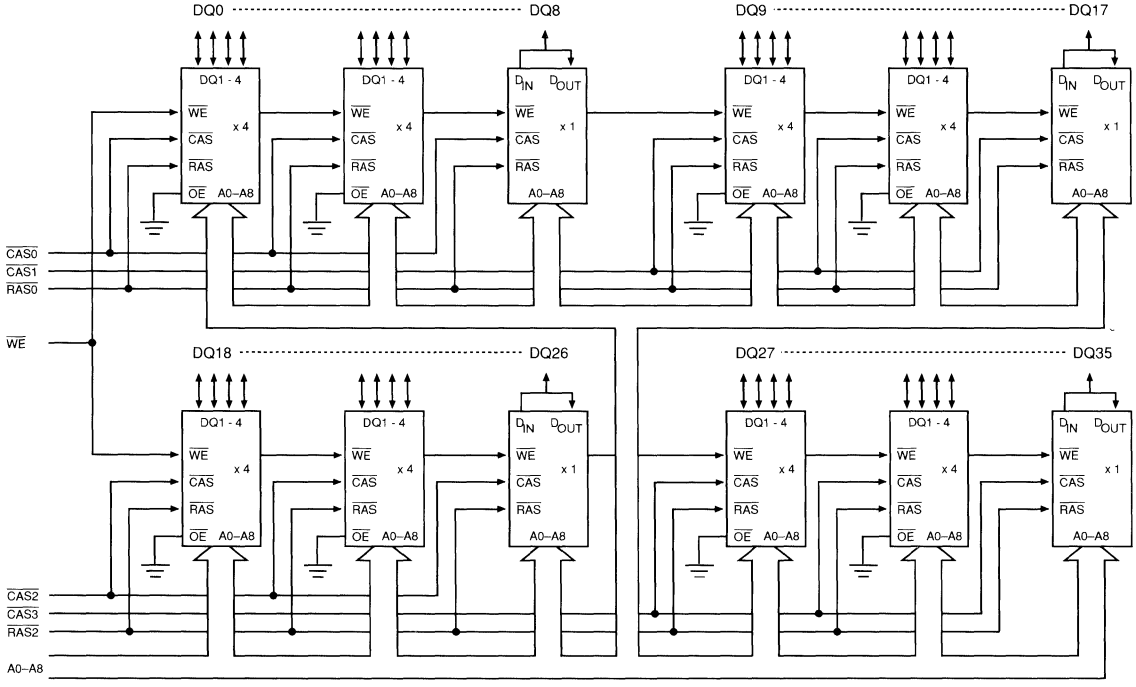
PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the PAGE MODE operation.

PIN ASSIGNMENT (Top View) MK



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vcc	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	Vss	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	Vcc
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ27	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PRD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	Vss

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 12 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$ = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: $t_{RC} = t_{RC(MIN)}$)	I_{CC1}		720	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: $t_{PC} = t_{PC(MIN)}$)	I_{CC2}		720	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		55	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		28	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		500	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		500	mA	3, 5
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts) (For each package input)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \le V_{OUT} \le V_{CC}$) (For each package input)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8)	C_{I1}		60	pF	18
Input Capacitance ($\overline{WE}$)	C_{I2}		84	pF	18
Input Capacitance ($\overline{RAS}0$, $\overline{RAS}2$)	C_{I3}		42	pF	18
Input Capacitance ($\overline{CAS}0$, $\overline{CAS}1$, $\overline{CAS}2$, $\overline{CAS}3$)	C_{I4}		21	pF	18
Input Capacitance (DQ0 - DQ35)	C_{I5}		7	pF	18
Output Capacitance (DQ0 - DQ35)	C_{O1}		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	190		220		260		ns	
PAGE-MODE READ or WRITE cycle time	^tPC	90		100		120		ns	
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	14
Access time from $\overline{CAS}$	^tCAC		50		60		75	ns	15
Access time from column address	^tAA		50		60		75	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		50		65		75	ns	
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	100	100,000	120	100,000	150	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	25		25		30		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	25	50	25	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	15		20		20		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	15		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	20	50	20	60	20	75	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	20		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	70		80		100		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	50		60		75		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

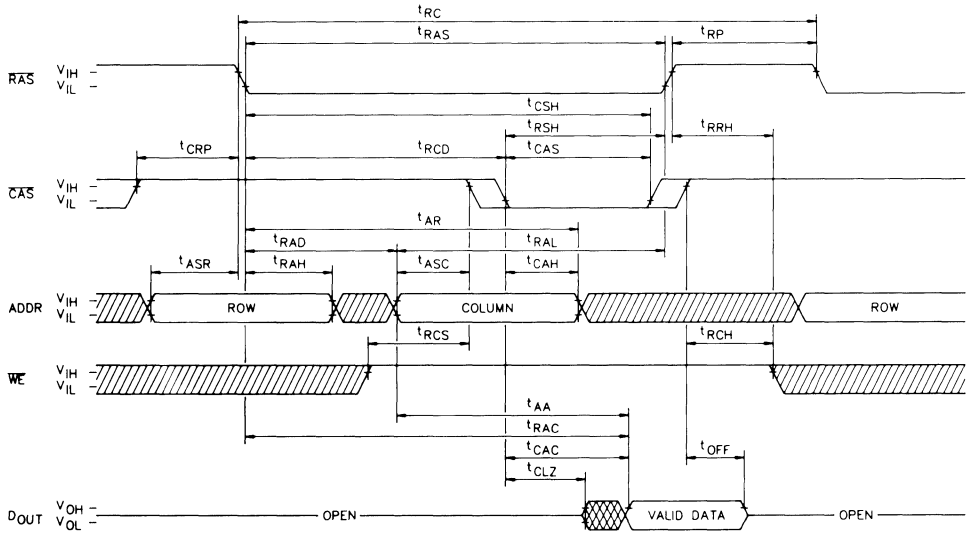
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in low-Z	^tCLZ	5		5		5		ns	
Output buffer turn-off delay	^tOFF	0	30	0	30	0	30	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	35		40		45		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	85		100		120		ns	
Write command pulse width	^tWP	35		40		45		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	35		40		45		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	35		40		45		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		110		135		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	50		60		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	35		40		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		4		4		4	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5

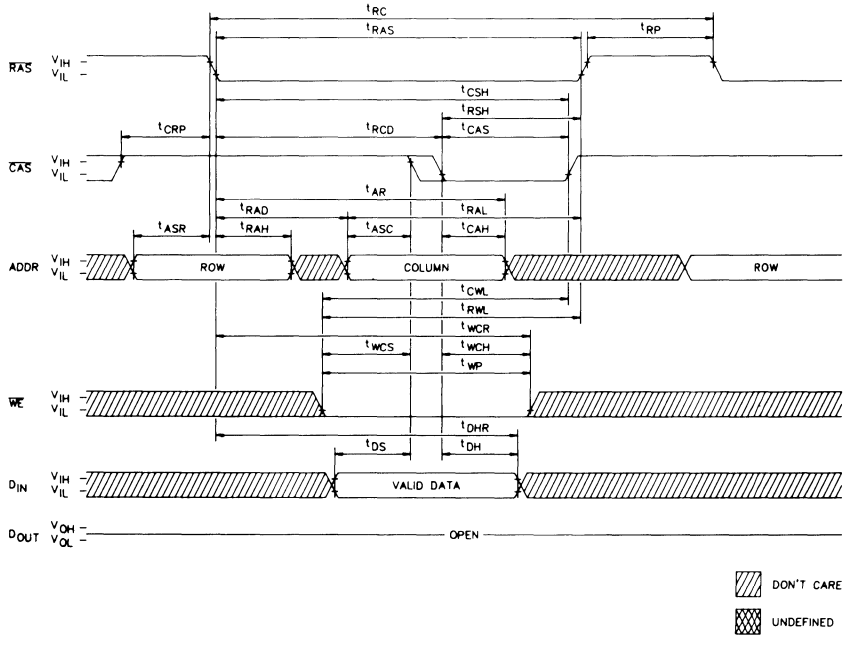
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (min), $^tAWD \geq ^tAWD$ (min) and $^tCWD \geq ^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

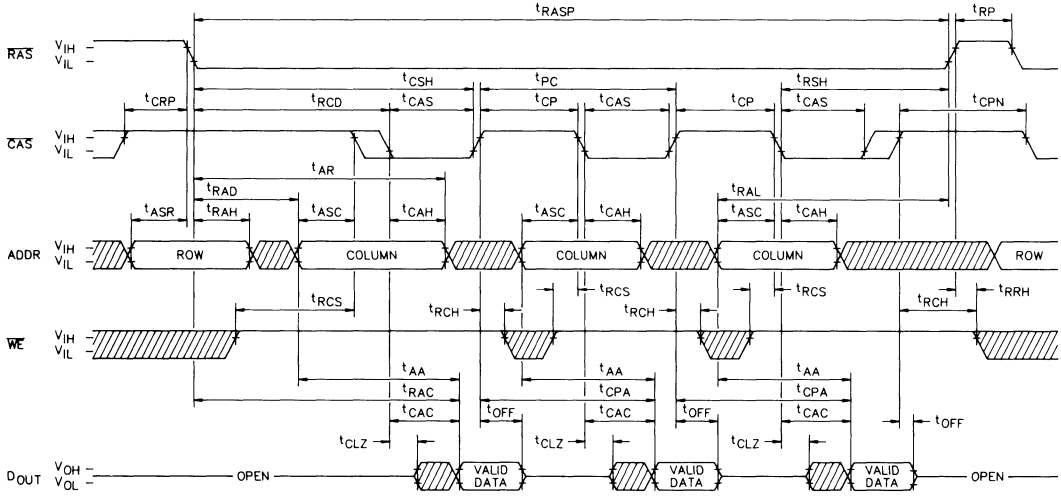
READ CYCLE



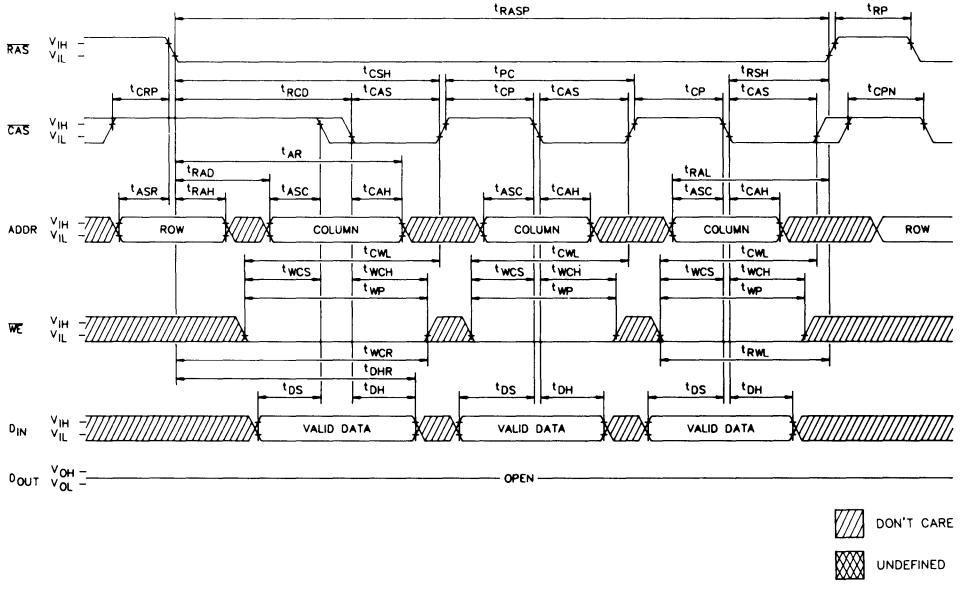
EARLY-WRITE CYCLE



PAGE-MODE READ CYCLE

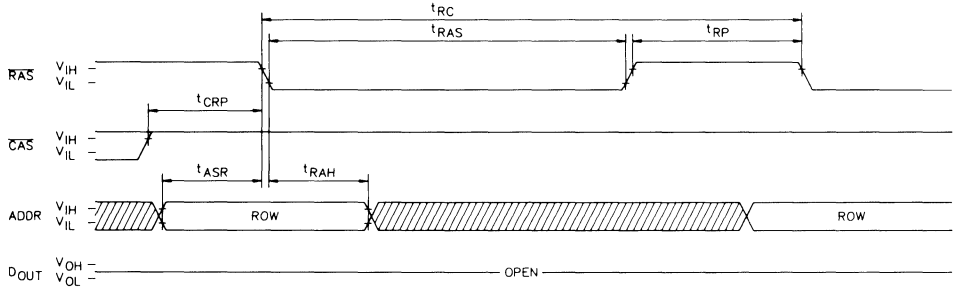


PAGE-MODE EARLY-WRITE CYCLE



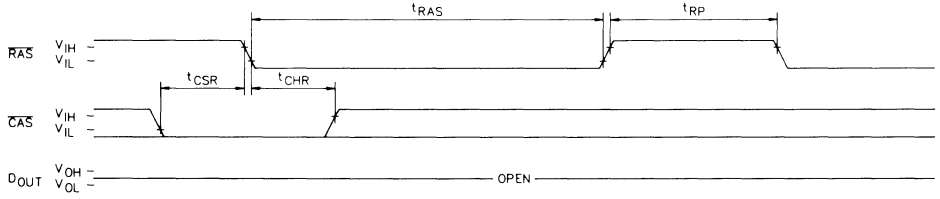
$\overline{RAS}$ ONLY REFRESH CYCLE

(A_0 - A_8 and $\overline{WE}$ = DON'T CARE.)



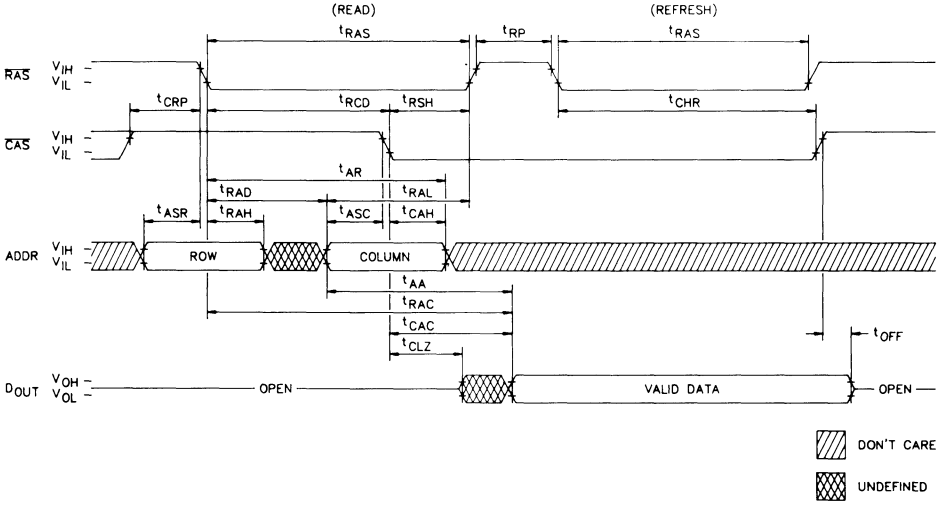
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 and $\overline{WE}$ = DON'T CARE.)



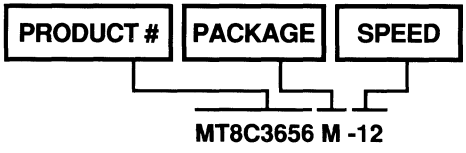
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

256K x 36, 120ns access, Page Mode Access, SIMM



The Micron DRAM module family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS and NMOS silicon gate processes. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM MODULES

1MEG x 8 DRAM

FAST PAGE MODE

FEATURES

- Industry standard pin-out in a 30-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 40mW standby, 1400mW active, typical.
- On-board power supply decoupling capacitors (0.2µf) for low noise.
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden.
- 512 cycle refresh distributed across 8ms.
- Optional Fast Page Mode.

OPTIONS — MARKING

- Timing

80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15

- Access Mode Option

Fast Page Mode	MT8C8024

- Packages:

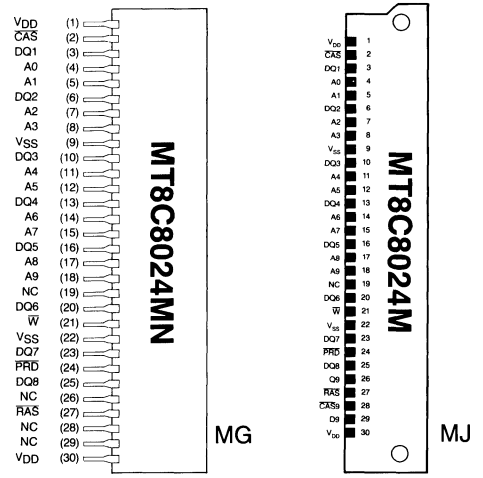
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	MN

A0-A9	Address Inputs	$\overline{CAS}$, $\overline{CAS9}$	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
$\overline{PRD}$	Presence Detect	Q9	Data-Out
$\overline{RAS}$	Row Address Strobe	$\overline{W}$	Write Enable
VDD	Power (+5V)	Vss	Ground

GENERAL DESCRIPTION

The MT8C8024M/MN is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x8 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates

PIN ASSIGNMENT (Top View)

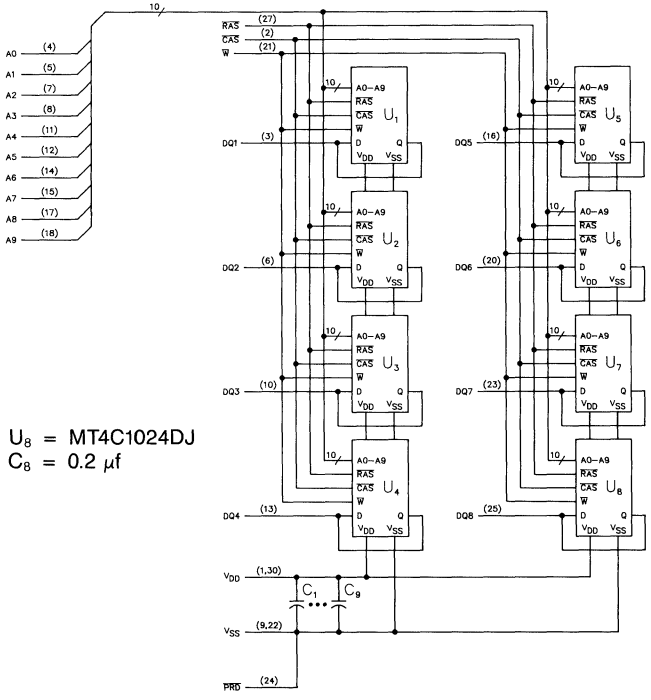


WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM



$U_1 - U_8$ = MT4C1024DJ
$C_1 - C_8$ = 0.2 µf

FUNCTIONAL TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		400	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		400	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		16	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		8	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		280	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		280	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-80	80	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-80	80	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9)	C_{I1}		40	pF	18
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		56	pF	18
Output Capacitance D_{OUT}, D_{IN}	C_O		12	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	190		220		260		ns	
PAGE-MODE READ or WRITE cycle time	t_{PC}	55		70		85		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	14
Access time from $\overline{CAS}$	t_{CAC}		25		30		45	ns	15
Access time from column address	t_{AA}		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		65		75	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	t_{RASP}	100	100,000	120	100,000	150	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	80		90		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{CAS}$ precharge time	t_{CPN}	15		20		25		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	t_{CP}	10		15		20		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	10	75	15	90	15	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	10	50	15	60	15	70	ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	50		60		70		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	5		5		5		ns	
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	30	ns	20
Write command hold time	t_{WCH}	20		25		30		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

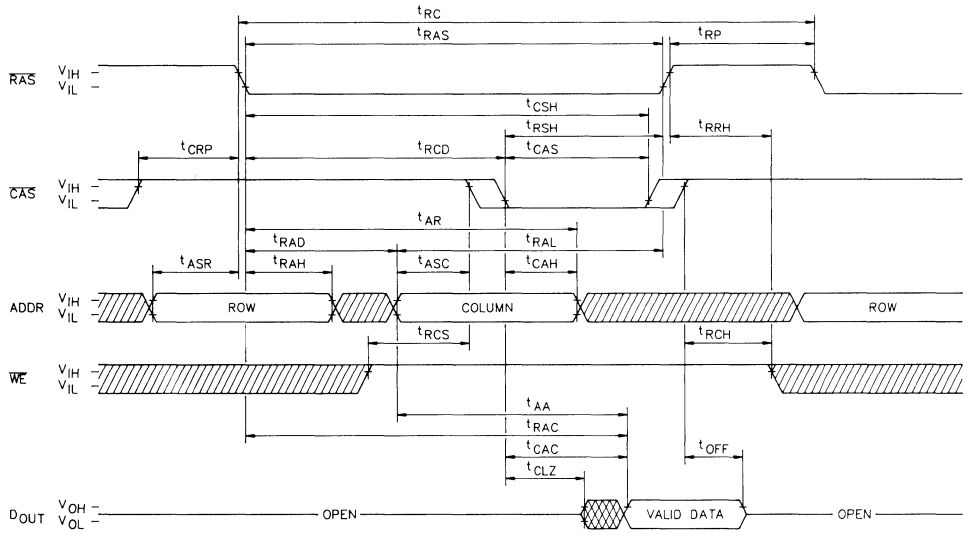
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	
Write command pulse width	^tWP	20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	15		20		25		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		110		135		ns	
Column address to $\overline{WE}$ delay time	^tAWD	50		60		70		ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	35		40		45		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5

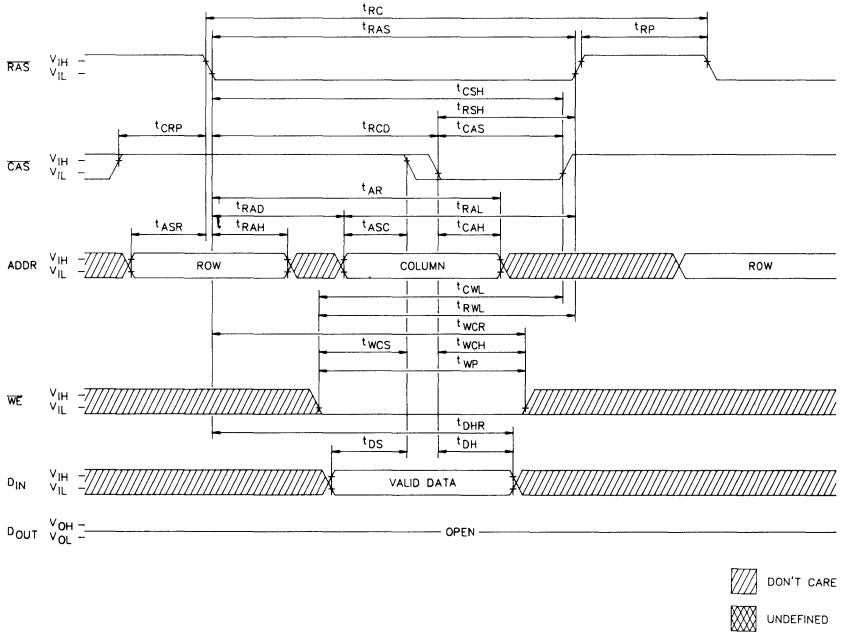
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

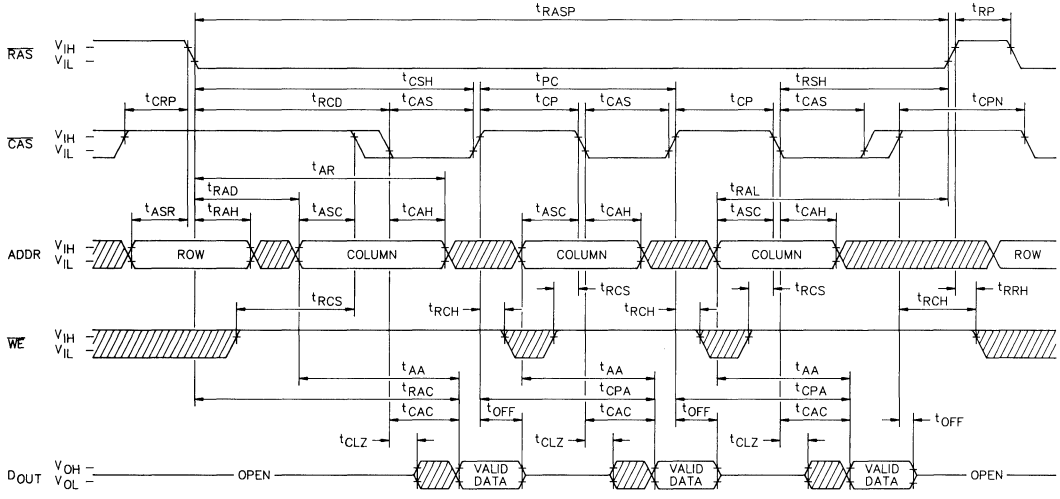
READ CYCLE



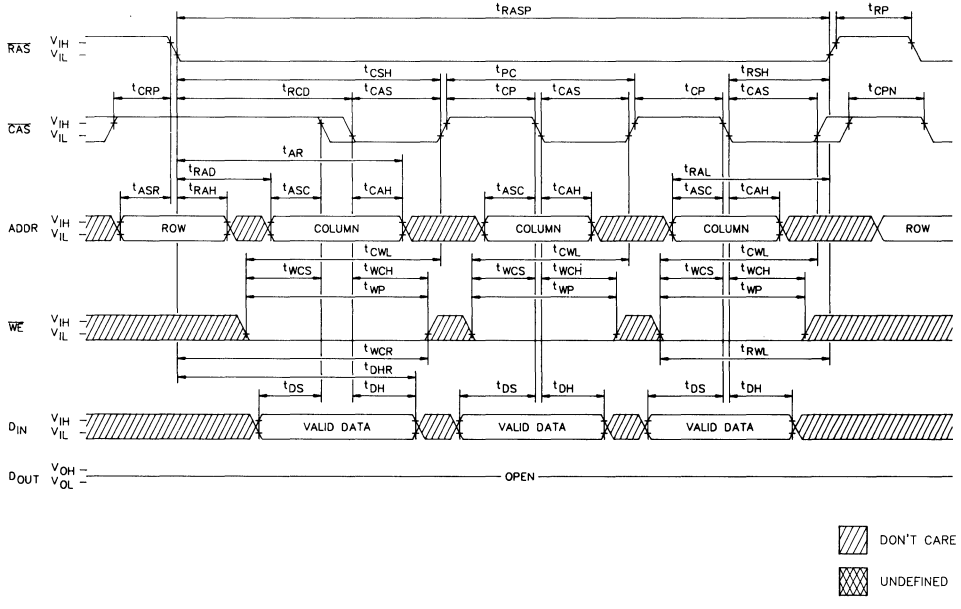
EARLY-WRITE CYCLE



PAGE-MODE READ CYCLE

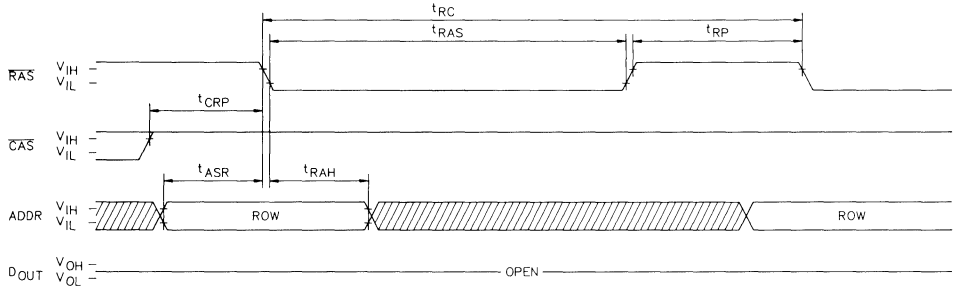


PAGE-MODE EARLY-WRITE CYCLE



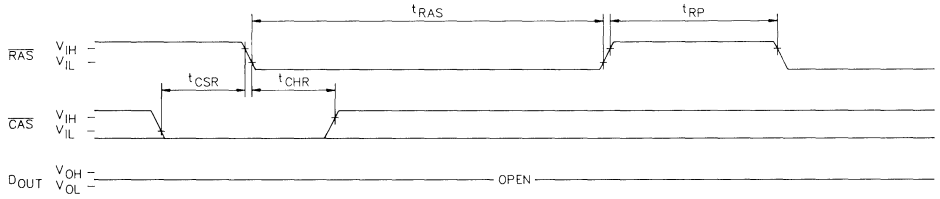
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



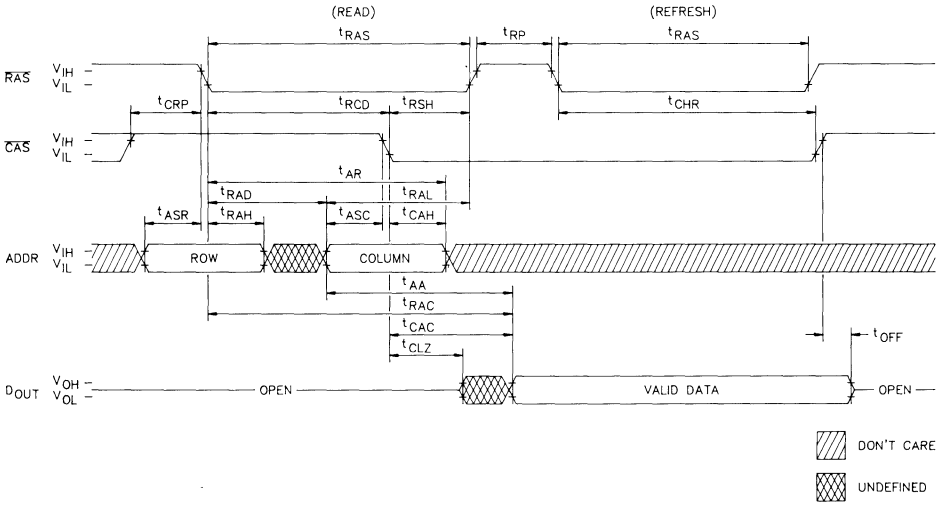
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 $\overline{WE}$, = DON'T CARE.)



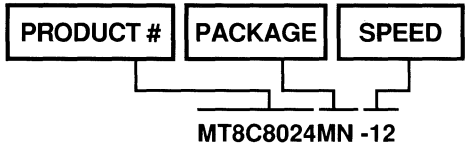
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

1 MEG x 8, 120ns access, Fast Page Mode Access, Leaded SIP



The Micron 1 MEG DRAM module family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

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DRAM MODULES

1MEG x 8 DRAM

NIBBLE MODE

FEATURES

- Industry standard pin-out in a 30-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 45mW standby, 1575mW active, typical.
- On-board power supply decoupling capacitors (0.2µf) for low noise.
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden.
- 512 cycle refresh distributed across 8ms.
- Optional Nibble access mode.

OPTIONS MARKING

- Timing

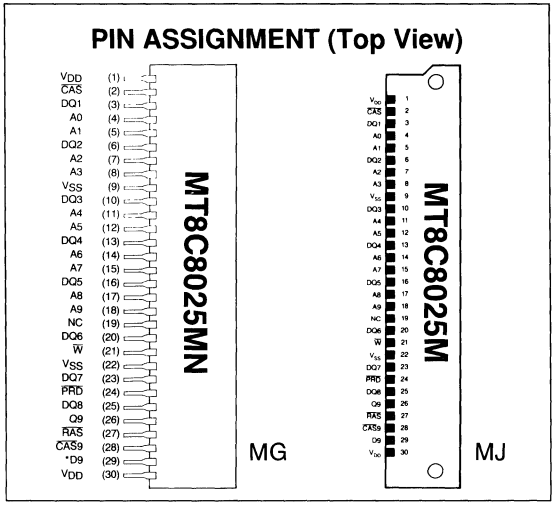
100ns access	-10
120ns access	-12
150ns access	-15

- Access Mode Option

Nibble Mode	MT8C8025

- Packages:

Leaded 30-pin SIP	MN
Leadless 30-pin SIMM	M



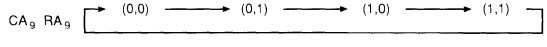
A0-A9	Address Inputs	$\overline{CAS}$, $\overline{CAS9}$	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
$\overline{PRD}$	Presence Detect	Q9	Data-Out
$\overline{RAS}$	Row Address Strobe	$\overline{W}$	Write Enable
VDD	Power (+5V)	Vss	Ground

GENERAL DESCRIPTION

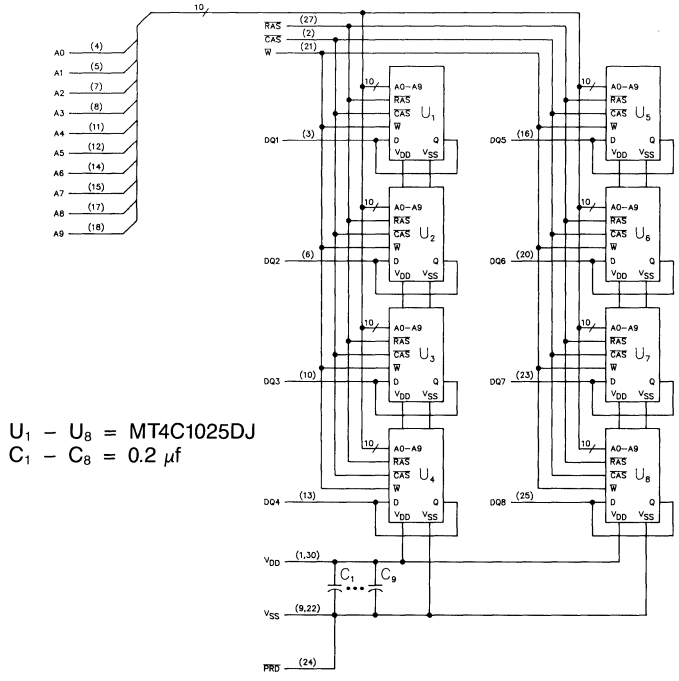
The MT8C8025 M/MN is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

Nibble Mode operation allows faster sequential serial data operations (READ, WRITE or READ-MODIFY-WRITE) on up to 4 bits. The first of 4 bits is accessed in the usual manner with $\overline{CAS}$ address A9 (nibble MSB) and $\overline{RAS}$ address A9 (nibble LSB) selecting on of 4 bits within a nibble for initial access. By holding $\overline{RAS}$ low, $\overline{CAS}$ can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around (see below).



FUNCTIONAL BLOCK DIAGRAM



$U_1 - U_8$ = MT4C1025DJ
$C_1 - C_8$ = 0.2 μf

FUNCTIONAL TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	TF	Addresses			NOTES
					tR	tC		
Standby	H	H	H	GND/NC	X	X	High Impedance	
READ	L	L	H	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
NIBBLE MODE READ	L	H→L→H	H	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
NIBBLE MODE WRITE	L	H→L→H	L	GND/NC	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	GND/NC	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	GND/NC	X	X	High Impedance	
TEST FUNCTION	L	L	H	H	ROW	COL	Data Out, Test Funtion Mode	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		400	mA	3, 4
OPERATING CURRENT: NIBBLE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		400	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		16	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		8	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		280	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		280	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-80	80	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-80	80	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9)	C_{I1}		40	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		56	pF	2
Output Capacitance D_{OUT}, D_{IN}	C_O		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	190		220		260		ns	
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	14
Access time from $\overline{CAS}$	^tCAC		25		30		45	ns	15
Access time from column address	^tAA		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		50		65		75	ns	
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		30		45		ns	
$\overline{RAS}$ precharge time	^tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	15		20		25		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	75	15	90	15	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	10	50	15	60	15	70	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	50		60		70		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	5		5		5		ns	
Output buffer turn-off delay	^tOFF	0	25	0	25	0	30	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	20		25		30		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

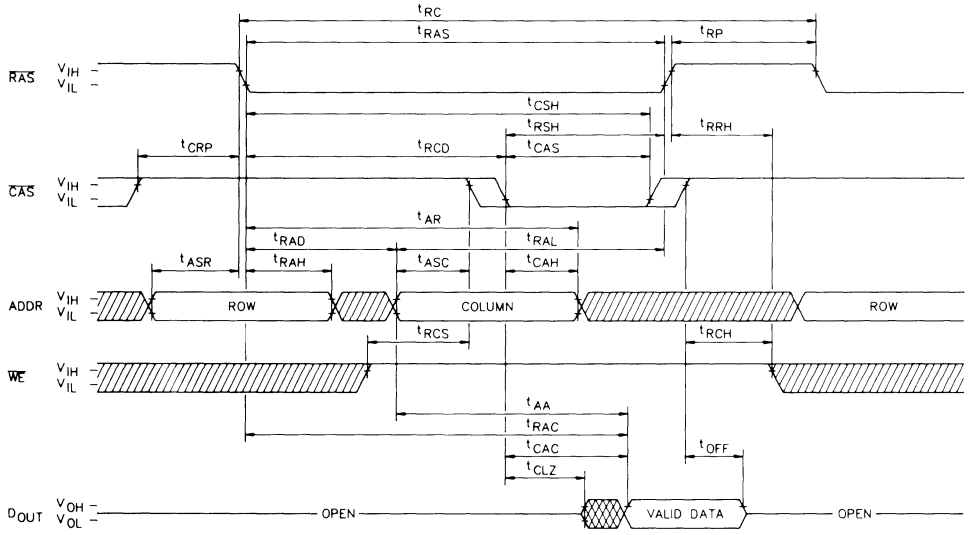
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command pulse width	^tWP	20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	15		20		25		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
Column address to $\overline{WE}$ delay time	^tAWD	50		60		70		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5
$\overline{RAS}$ pulse width (NIBBLE MODE)	^tRASN	100	100,000	120	100,000	150	100,000	ns	
$\overline{CAS}$ precharge time (NIBBLE MODE)	^tNCP	10		15		20		ns	
NIBBLE MODE cycle time	^tNC	35		40		45		ns	
NIBBLE MODE access time	^tNCAC	15		20		25		ns	15
NIBBLE MODE pulse width	^tNCAS	15		20		25		ns	
NIBBLE MODE $\overline{CAS}$ precharge time	^tNCP	10		10		10		ns	
NIBBLE MODE $\overline{RAS}$ hold time	^tNRSH	15		20		25		ns	
NIBBLE MODE $\overline{CAS}$ to $\overline{WRITE}$ delay time	^tNCWD	15		20		25		ns	
NIBBLE MODE $\overline{WRITE}$ command to $\overline{RAS}$ lead time	^tNRWL	15		20		25		ns	
NIBBLE MODE $\overline{WRITE}$ command to $\overline{CAS}$ lead time	^tNCWL	15		20		25		ns	

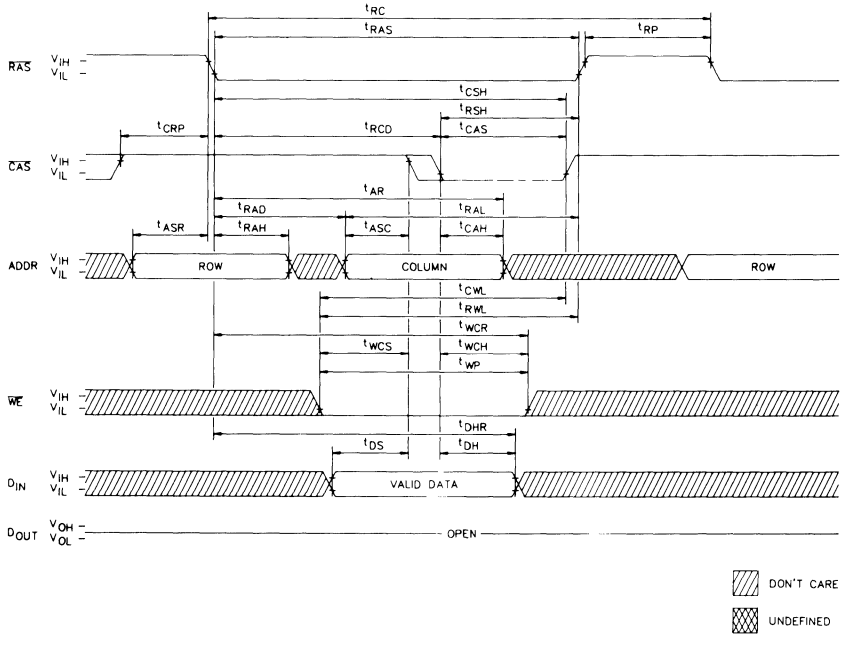
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

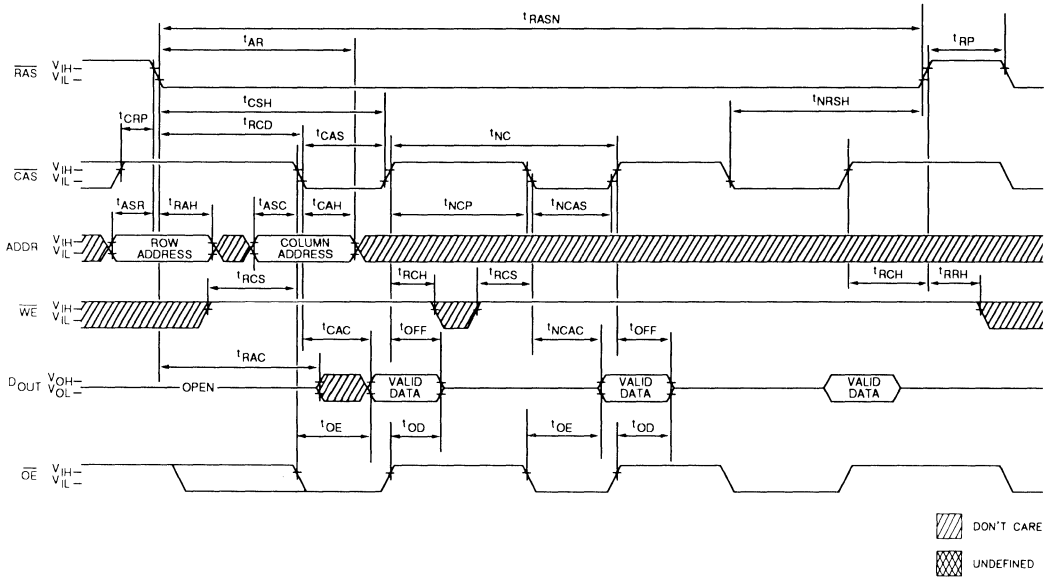
READ CYCLE



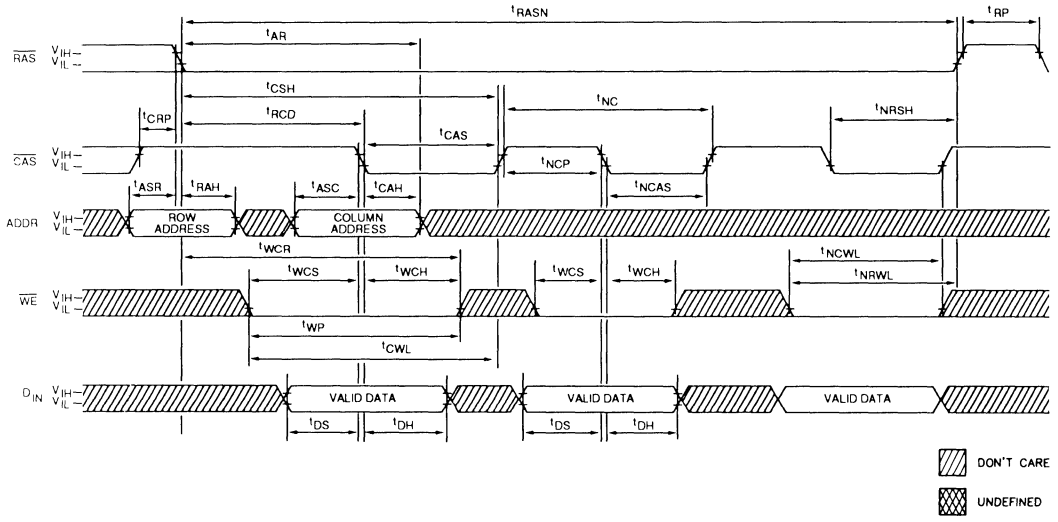
EARLY-WRITE CYCLE



NIBBLE MODE READ CYCLE

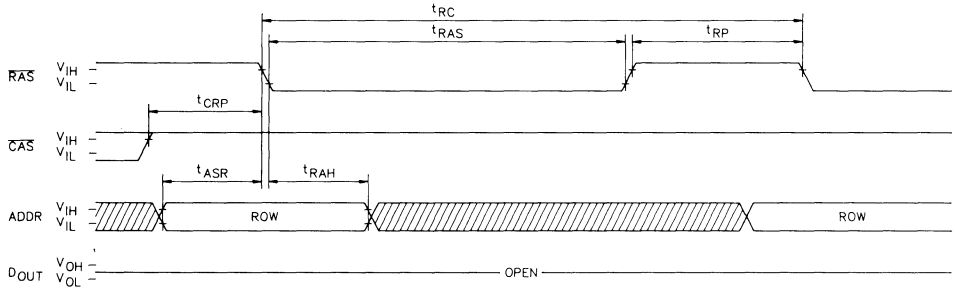


NIBBLE MODE WRITE CYCLE
(Early Write)



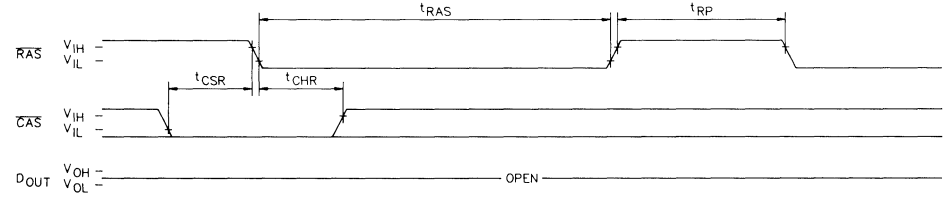
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



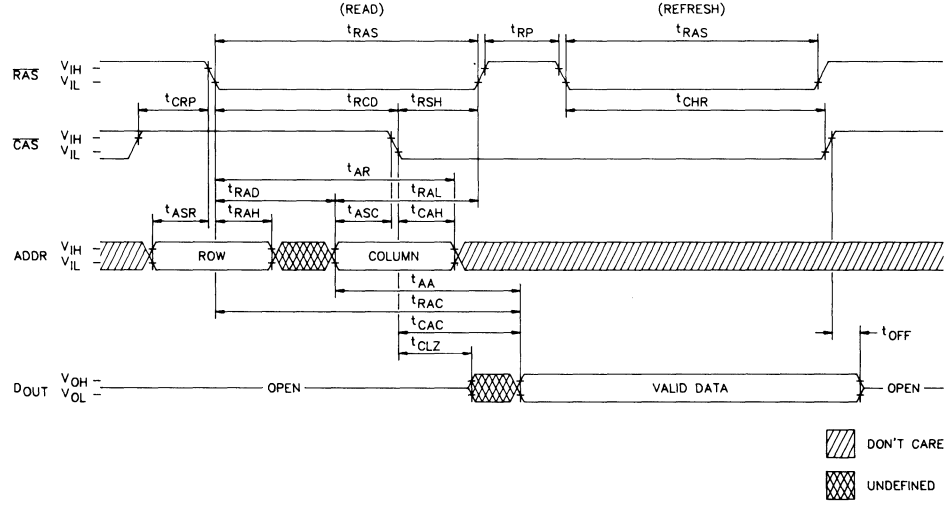
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 $\overline{WE}$, = DON'T CARE.)



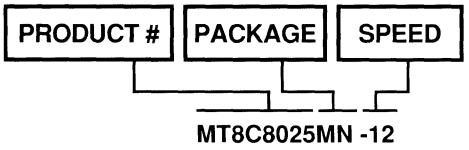
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

1 MEG x 8, 120ns access, Nibble Mode Access, Leaded SIP



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DRAM MODULES

1MEG x 8 DRAM

STATIC COLUMN

FEATURES

- Industry standard pin-out in a 30-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 45mW standby, 1575mW active, typical.
- On-board power supply decoupling capacitors (0.2µf) for low noise.
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden.
- 512 cycle refresh distributed across 8ms.
- Optional Static Column access mode.

OPTIONS MARKING

- Timing
  - 100ns access -10
  - 120ns access -12
  - 150ns access -15
- Access Mode Option
  - Static Column MT8C8026
- Packages: Leaded 30-pin SIP MN
  - Leadless 30-pin SIMM M

A0-A9	Address Inputs	$\overline{CAS}$, $\overline{CAS9}$	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
$\overline{PRD}$	Presence Detect	Q9	Data-Out
$\overline{RAS}$	Row Address Strobe	$\overline{W}$	Write Enable
VDD	Power (+5V)	Vss	Ground

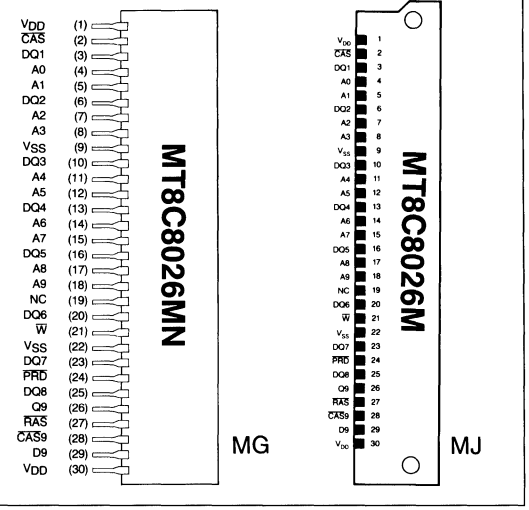
GENERAL DESCRIPTION

The MT8C8026 M/MN is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

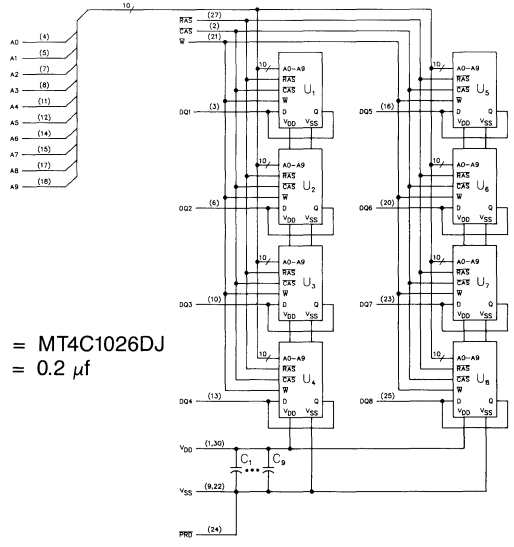
Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

STATIC COLUMN operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the STATIC COLUMN operation.

PIN ASSIGNMENT (Top View)



FUNCTIONAL BLOCK DIAGRAM



$U_1 - U_8$ = MT4C1026DJ
$C_1 - C_8$ = 0.2 μf

FUNCTIONAL TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	TF	Addresses			NOTES
					tR	tC		
Standby	H	H	H	GND/NC	X	X	High Impedance	
READ	L	L	H	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
STATIC COLUMN READ	L	L	H	GND/NC	ROW	COL COL	Valid Data Out, Valid Data Out	
STATIC COLUMN WRITE	L	L	L	GND/NC	ROW	COL COL	Valid Data In, Valid Data Out	
$\overline{RAS}$ ONLY REFRESH	L	H	H	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	GND/NC	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	GND/NC	X	X	High Impedance	
TEST FUNCTION	L	L	H	H	ROW	COL	Data Out, Test Funtion Mode	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		400	mA	3, 4
OPERATING CURRENT: STATIC COLUMN ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		400	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		16	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		8	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		280	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		200	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-80	80	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-80	80	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9)	C_{I1}		40	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		56	pF	2
Output Capacitance D_{OUT}, D_{IN}	C_O		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	190		220		260		ns	
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	14
Access time from $\overline{CAS}$	^tCAC		25		30		45	ns	15
Access time from column address	^tAA		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		50		65		75	ns	
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		30		45		ns	
$\overline{RAS}$ precharge time	^tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	15		20		25		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	75	15	90	15	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	10	50	15	60	15	70	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	50		60		70		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	5		5		5		ns	
Output buffer turn-off delay	^tOFF	0	25	0	25	0	30	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	20		25		30		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

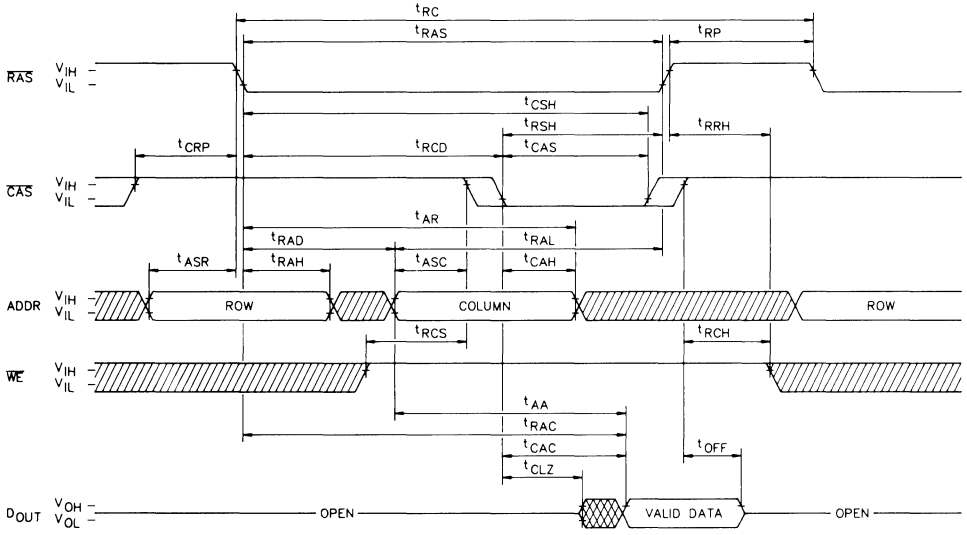
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command pulse width	^tWP	20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	15		20		25		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
Column address to $\overline{WE}$ delay time	^tAWD	50		60		70		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	100	100,000	120	100,000	150	100,000	ns	
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		15		20		ns	
STATIC COLUMN MODE cycle time	^tSC	55		65		75		ns	
Last Write to column address delay time	^tLWAD	25	45	30	55	45	70	ns	
Last Write to column address hold time	^tAHLW		95		115		135	ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	^tROH	20		20		20		ns	
Output data hold time from column address	^tAOH	5	—	5	—	5	—	ns	
Output data enable from Write	^tOW	—	25	—	25	—	25	ns	

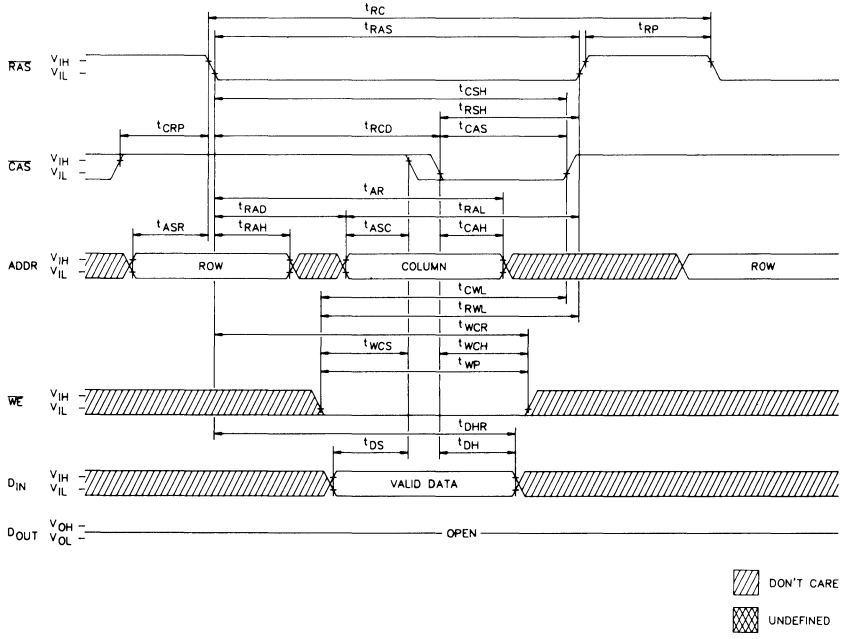
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

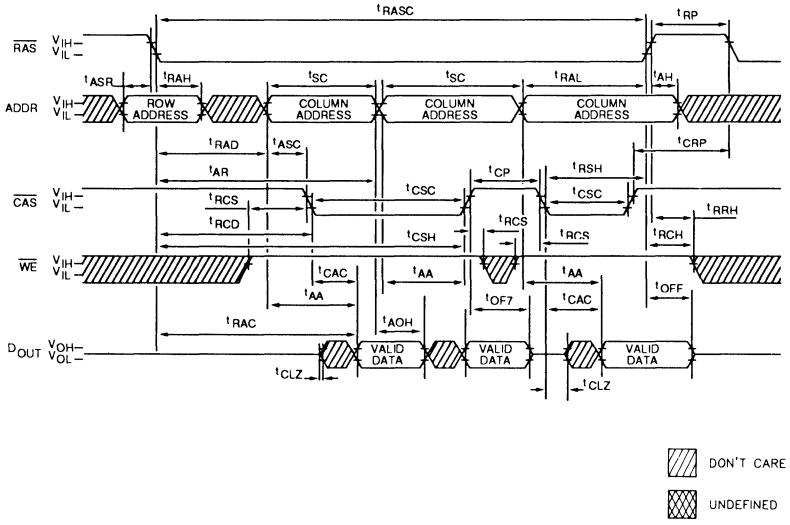
READ CYCLE



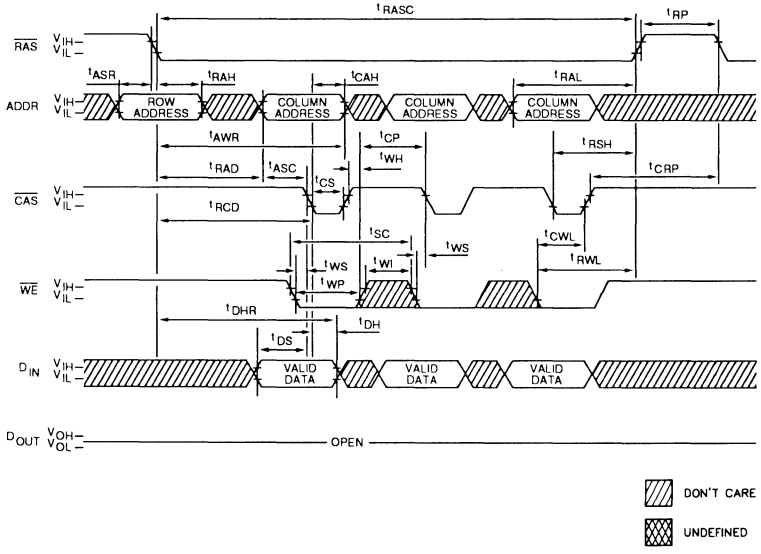
EARLY-WRITE CYCLE



STATIC COLUMN READ CYCLE

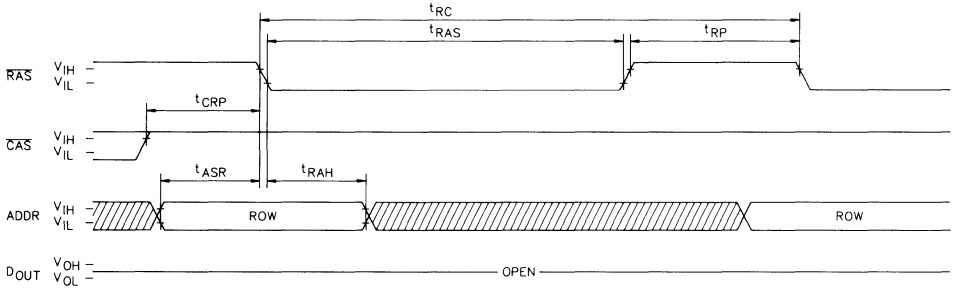


STATIC COLUMN EARLY-WRITE CYCLE



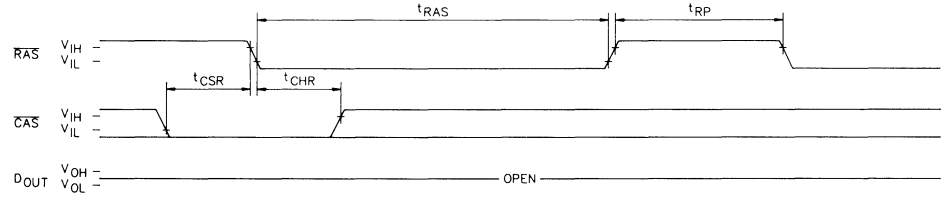
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



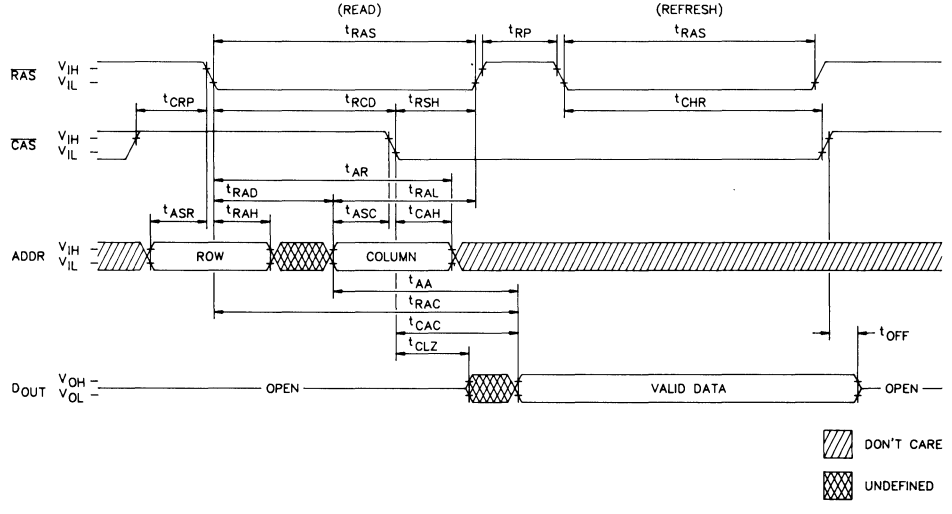
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 $\overline{WE}$, = DON'T CARE.)



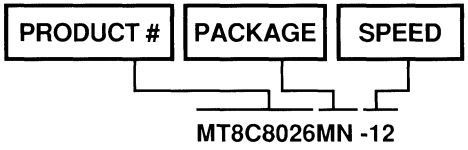
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

1 MEG x 8, 120ns access, Static Column Access, Leaded SIP



The Micron 1 MEG DRAM module family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM MODULES

1MEG x 9 DRAM

FAST PAGE MODE

FEATURES

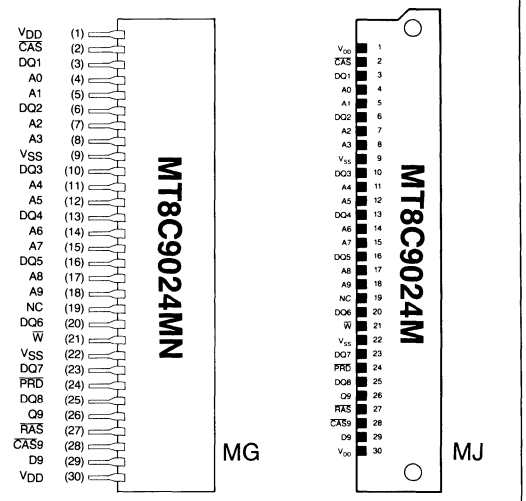
- Industry standard pin-out in a 30-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 45mW standby, 1575mW active, typical.
- On-board power supply decoupling capacitors (0.2µf) for low noise.
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden.
- 512 cycle refresh distributed across 8ms.
- Optional Fast Page Mode.

OPTIONS MARKING

- Timing
  - 100ns access -10
  - 120ns access -12
  - 150ns access -15
- Organization
  - 1 MEG x 9 MT8C9024
- Packages: Leadless 30-pin SIMM M
  Leadless 30-pim SIP MN

A0-A9	Address Inputs	$\overline{CAS}$, $\overline{CAS9}$	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
$\overline{PRD}$	Presence Detect	Q9	Data-Out
$\overline{RAS}$	Row Address Strobe	$\overline{W}$	Write Enable
V_{DD}	Power (+5V)	Vss	Ground

PIN ASSIGNMENT (Top View)



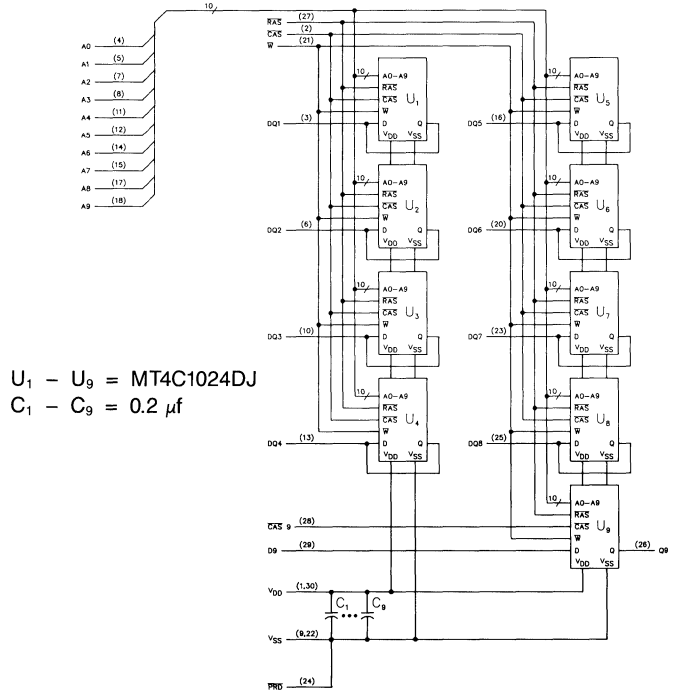
GENERAL DESCRIPTION

The MT8C9024M/MN is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x8 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM



$U_1 - U_9$ = MT4C1024DJ
$C_1 - C_9$ = 0.2 μf

FUNCTIONAL TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	
Write command pulse width	^tWP	20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		110		135		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	50		60		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	35		40		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 9 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$ = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		450	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		450	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		18	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		9	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		315	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		315	mA	3, 5
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts)	I_I	-90	90	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-90	90	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

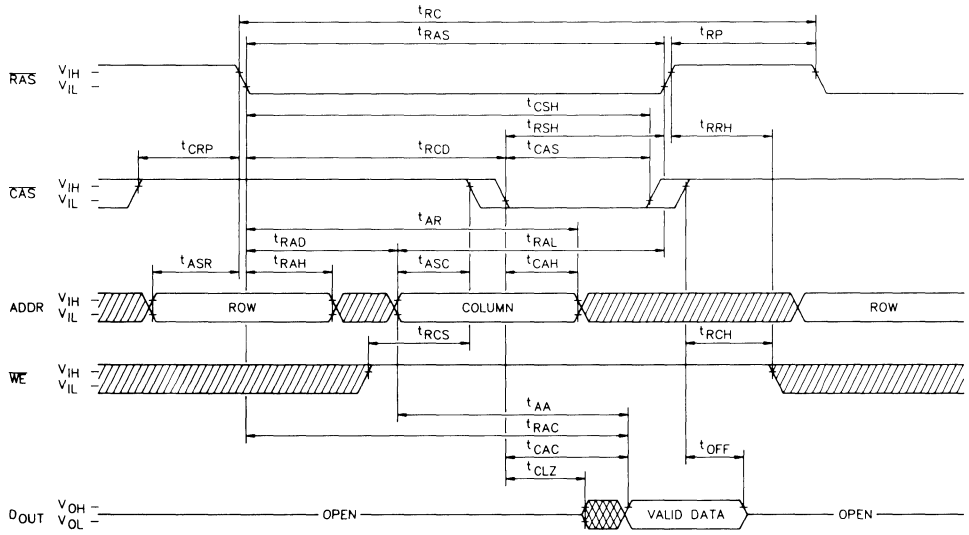
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9)	C_{I1}		45	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		63	pF	2
Output Capacitance D_{OUT}, D_{IN}	C_O		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

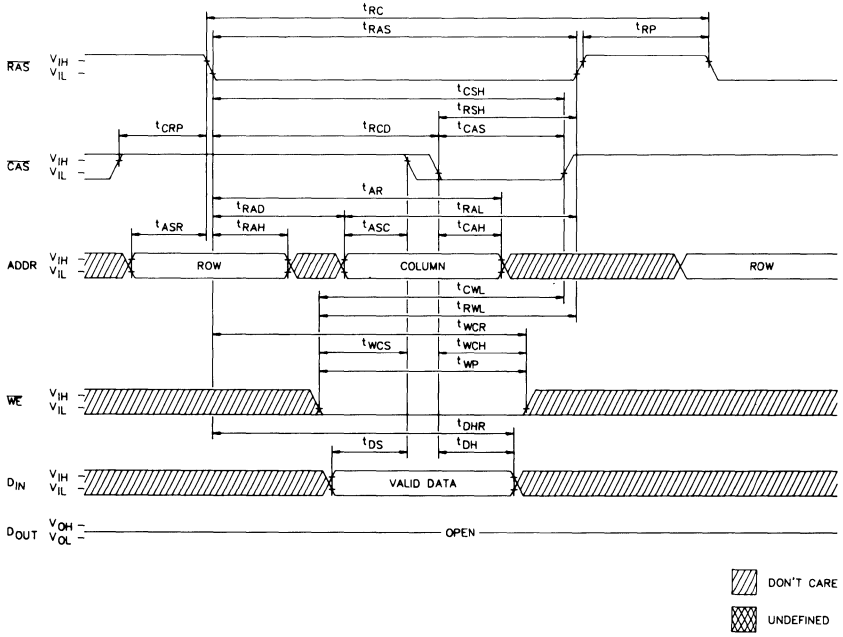
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	190		220		260		ns	
PAGE-MODE READ or WRITE cycle time	t_{PC}	55		70		85		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	14
Access time from $\overline{CAS}$	t_{CAC}		25		30		45	ns	15
Access time from column address	t_{AA}		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		65		75	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	t_{RASP}	100	100,000	120	100,000	150	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	80		90		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{CAS}$ precharge time	t_{CPN}	15		20		25		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	t_{CP}	10		15		20		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	10	75	15	90	15	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	10	50	15	60	15	70	ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	50		60		70		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	5		5		5		ns	
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	30	ns	20
$\overline{WE}$ command set-up time	t_{WCS}	0		0		0		ns	21
Write command hold time	t_{WCH}	20		25		30		ns	

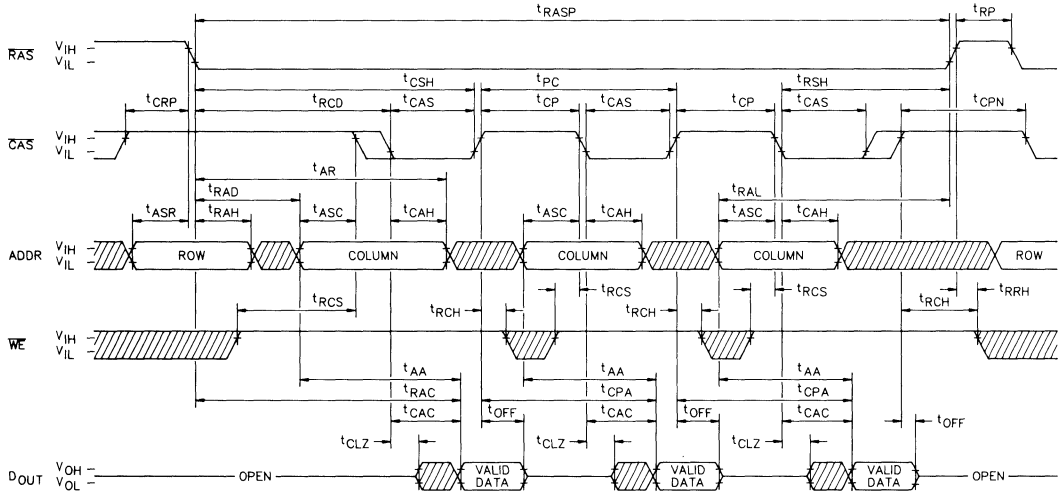
READ CYCLE



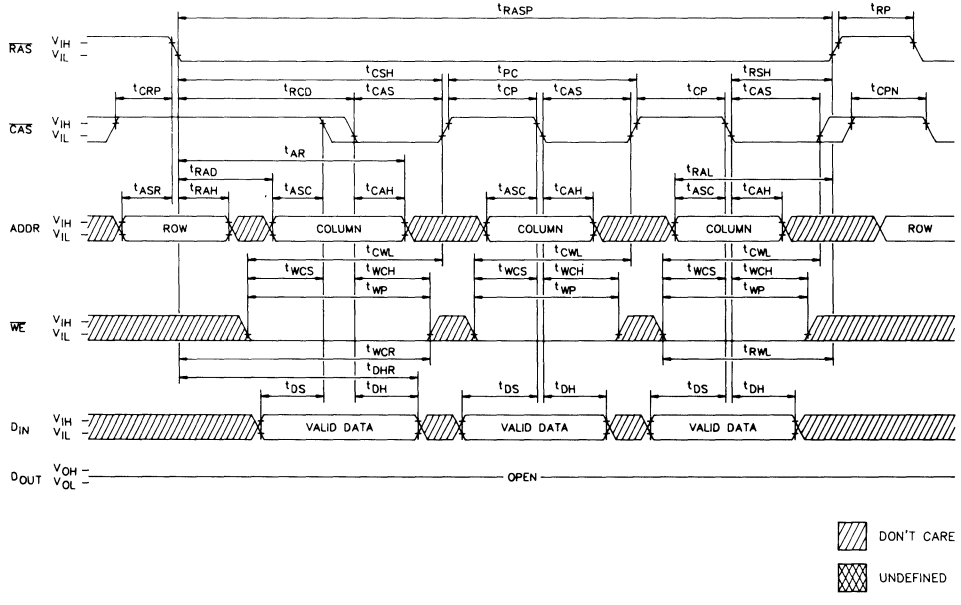
EARLY-WRITE CYCLE



PAGE-MODE READ CYCLE

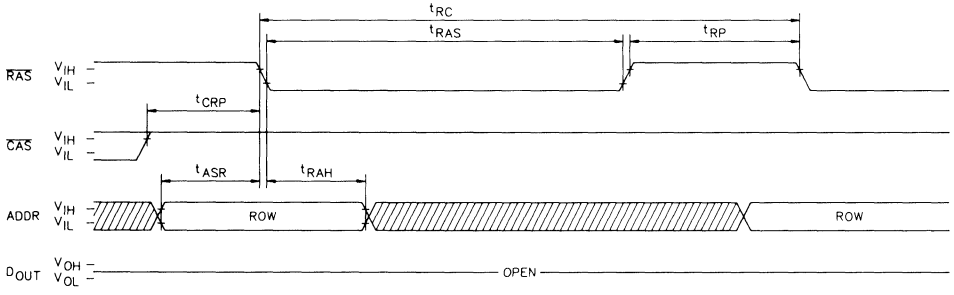


PAGE-MODE EARLY-WRITE CYCLE



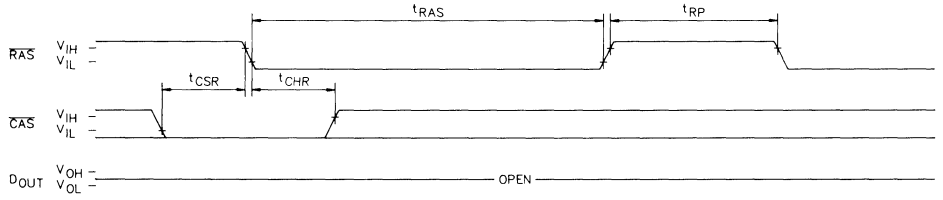
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



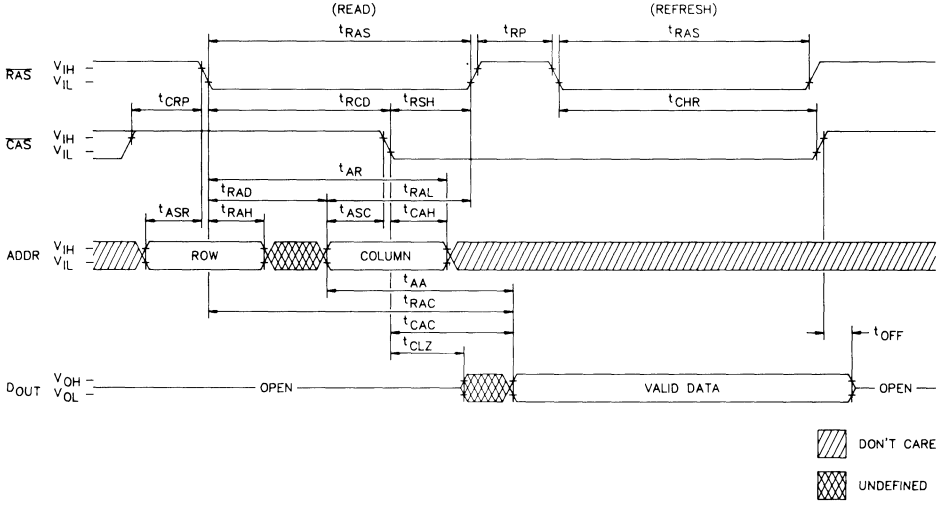
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 $\overline{WE}$, $\overline{OE}$ = DON'T CARE.)



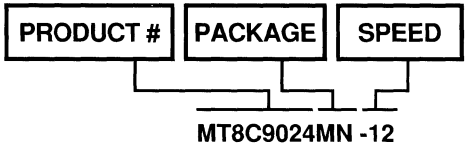
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

1 MEG x 9, 120ns access, Fast Page Mode Access, Leaded SIP



The Micron 1 MEG DRAM module family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM MODULES

1MEG x 9 DRAM

NIBBLE MODE

FEATURES

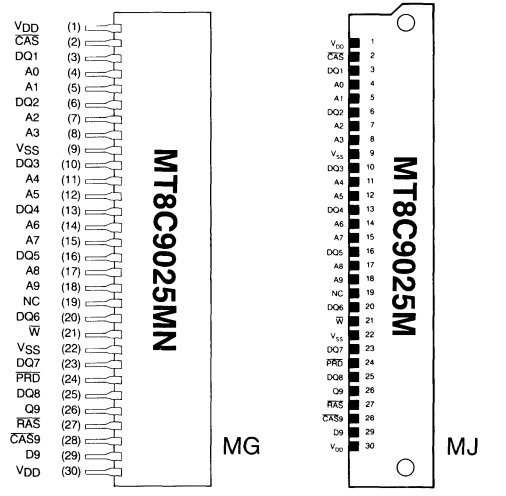
- Industry standard pin-out in a 30-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 45mW standby, 1575mW active, typical.
- On-board power supply decoupling capacitors (0.2µf) for low noise.
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden.
- 512 cycle refresh distributed across 8ms.
- Optional Nibble access mode.

OPTIONS MARKING

- Timing
  - 100ns access -10
  - 120ns access -12
  - 150ns access -15
- Access Mode Option
  - Nibble Mode MT8C9025
- Packages: Leaded 30-pin SIP MN
  - Leadless 30-pin SIMM N

A0-A9	Address Inputs	$\overline{CAS}$, $\overline{CAS9}$	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
$\overline{PRD}$	Presence Detect	Q9	Data-Out
$\overline{RAS}$	Row Address Strobe	$\overline{W}$	Write Enable
VDD	Power (+5V)	Vss	Ground

PIN ASSIGNMENT (Top View)

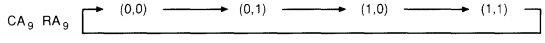


GENERAL DESCRIPTION

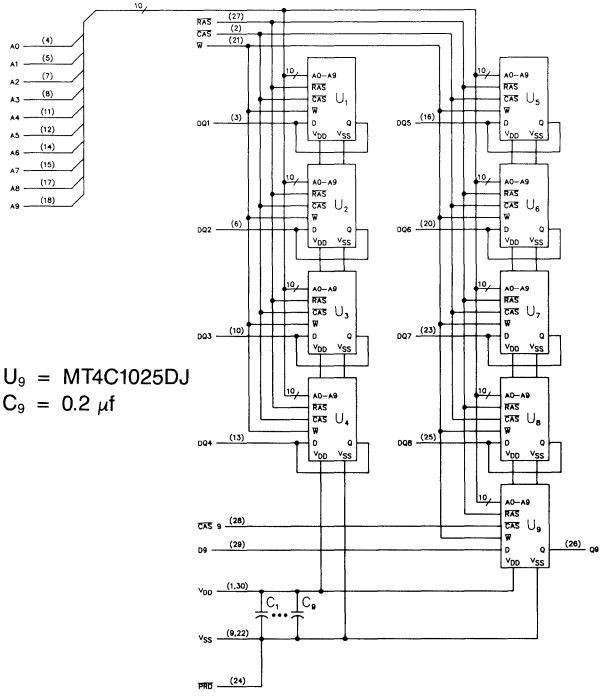
The MT8C9025 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

Nibble Mode operation allows faster sequential serial data operations (READ, WRITE or READ-MODIFY-WRITE) on up to 4 bits. The first of 4 bits is accessed in the usual manner with $\overline{CAS}$ address A9 (nibble MSB) and $\overline{RAS}$ address A9 (nibble LSB) selecting on of 4 bits within a nibble for initial access. By holding $\overline{RAS}$ low, $\overline{CAS}$ can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around (see below).



FUNCTIONAL BLOCK DIAGRAM



$U_1 - U_9$ = MT4C1025DJ
$C_1 - C_9$ = 0.2 μf

FUNCTIONAL TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
NIBBLE MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
NIBBLE MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 9 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		450	mA	3, 4
OPERATING CURRENT: NIBBLE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		450	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		18	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		9	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		315	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		315	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-90	90	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-90	90	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9)	C_{I1}		45	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		63	pF	2
Output Capacitance D_{OUT}, D_{IN}	C_O		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	190		220		260		ns	
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	14
Access time from $\overline{CAS}$	^tCAC		25		30		45	ns	15
Access time from column address	^tAA		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		50		65		75	ns	
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		30		45		ns	
$\overline{RAS}$ precharge time	^tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	15		20		25		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	75	15	90	15	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	10	50	15	60	15	70	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	50		60		70		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	5		5		5		ns	
Output buffer turn-off delay	^tOFF	0	25	0	25	0	30	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	20		25		30		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

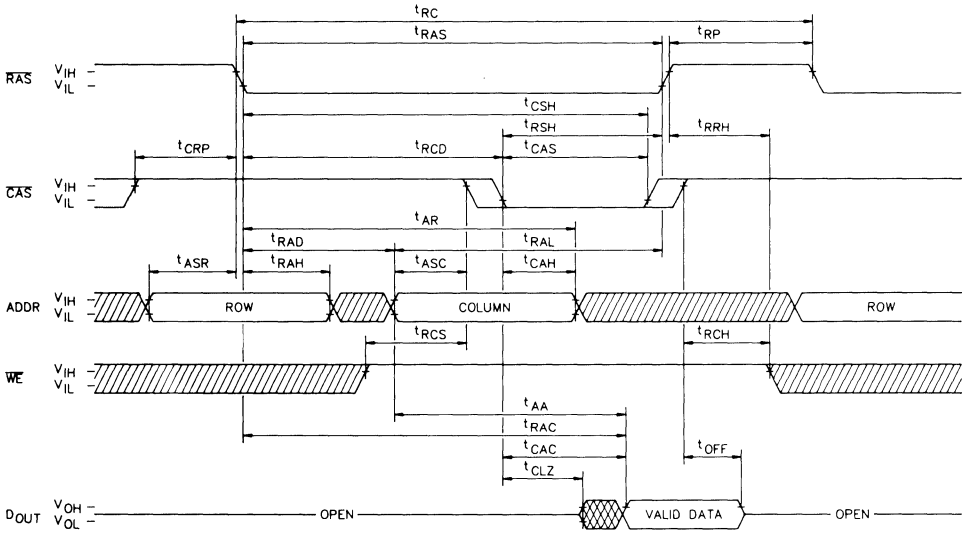
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command pulse width	^tWP	20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	15		20		25		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
Column address to $\overline{WE}$ delay time	^tAWD	50		60		70		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5
$\overline{RAS}$ pulse width (NIBBLE MODE)	^tRASN	100	100,000	120	100,000	150	100,000	ns	
$\overline{CAS}$ precharge time (NIBBLE MODE)	^tNCP	10		15		20		ns	
NIBBLE MODE cycle time	^tNC	35		40		45		ns	
NIBBLE MODE access time	^tNCAC	15		20		25		ns	15
NIBBLE MODE pulse width	^tNCAS	15		20		25		ns	
NIBBLE MODE $\overline{CAS}$ precharge time	^tNCP	10		10		10		ns	
NIBBLE MODE $\overline{RAS}$ hold time	^tNRSH	15		20		25		ns	
NIBBLE MODE $\overline{CAS}$ to $\overline{WRITE}$ delay time	^tNCWD	15		20		25		ns	
NIBBLE MODE $\overline{WRITE}$ command to $\overline{RAS}$ lead time	^tNRWL	15		20		25		ns	
NIBBLE MODE $\overline{WRITE}$ command to $\overline{CAS}$ lead time	^tNCWL	15		20		25		ns	

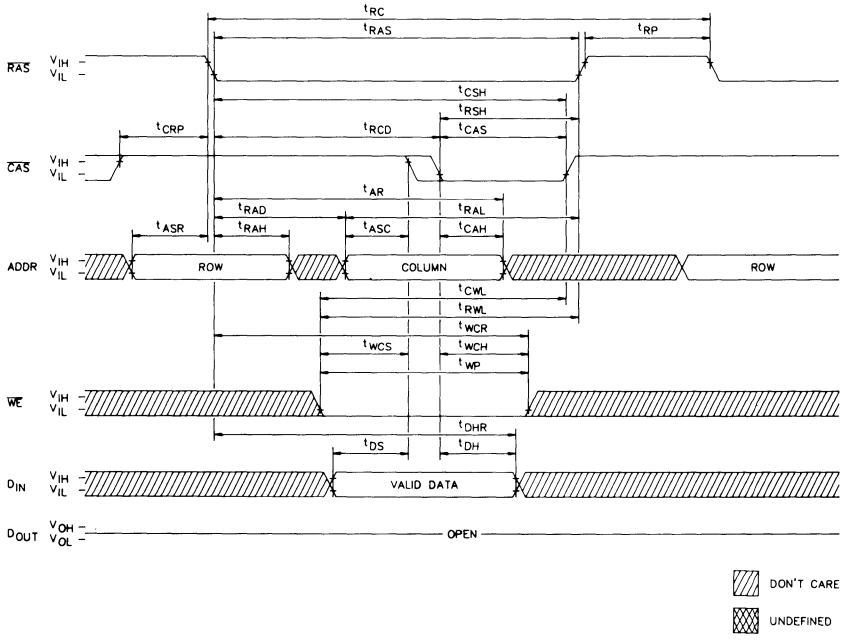
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

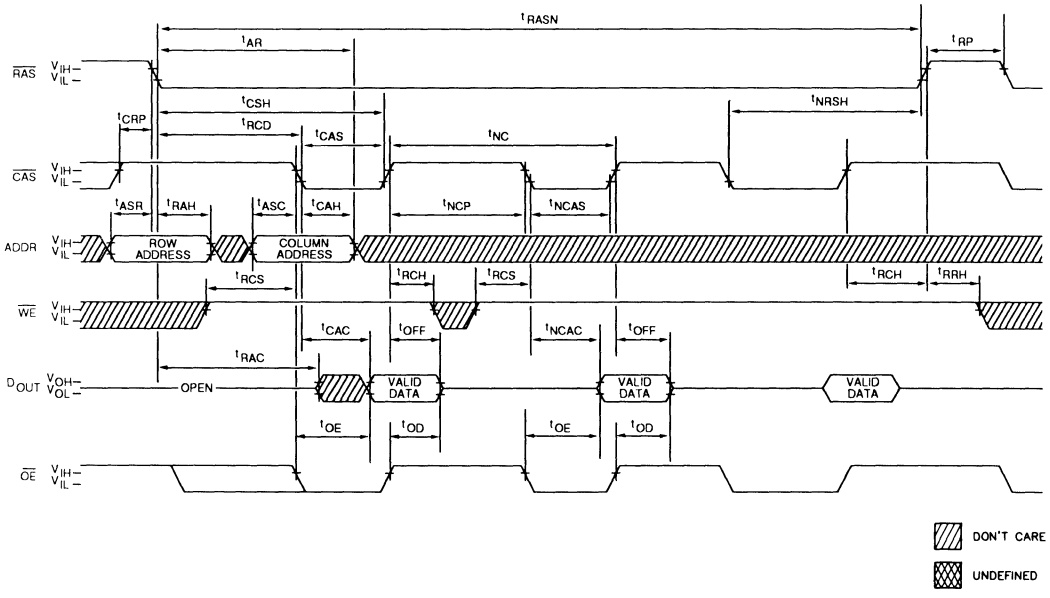
READ CYCLE



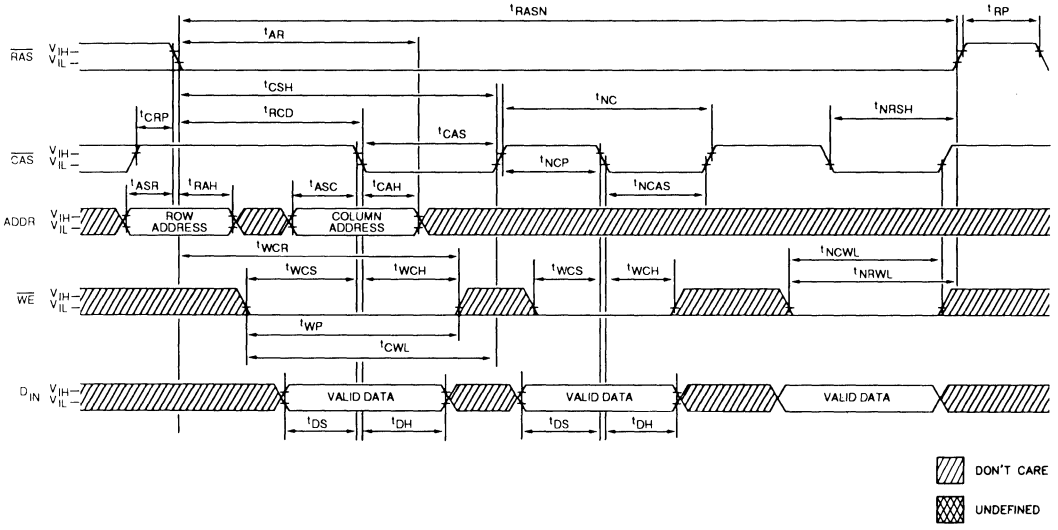
EARLY-WRITE CYCLE



NIBBLE MODE READ CYCLE

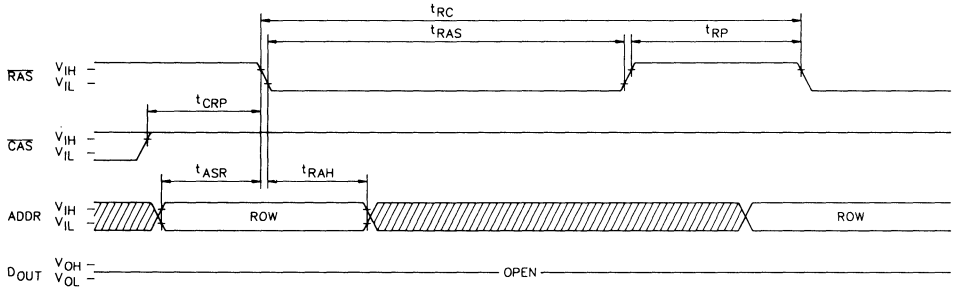


NIBBLE MODE WRITE CYCLE
(Early Write)



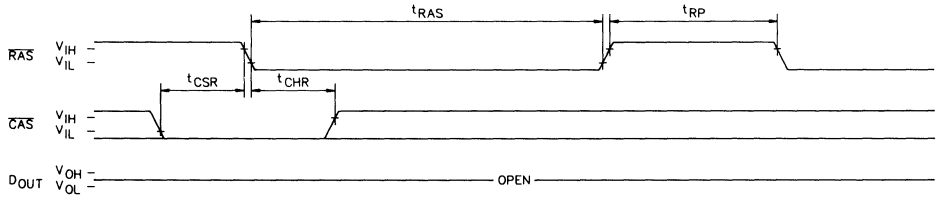
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



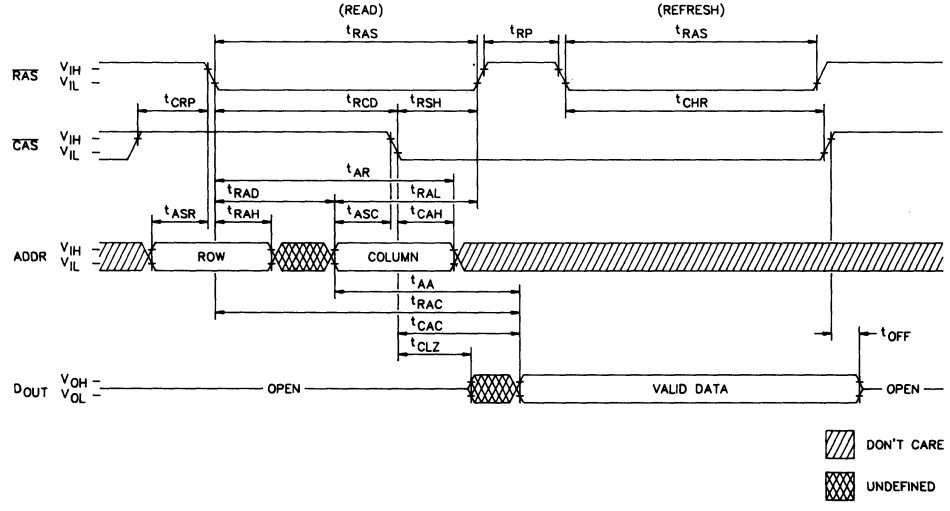
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 $\overline{WE}$, = DON'T CARE.)



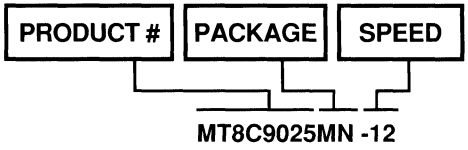
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

1 MEG x 9, 120ns access, Nibble Mode Access, Leaded SIP



The Micron 1 MEG DRAM module family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

DRAM MODULES

1MEG x 9 DRAM

STATIC COLUMN

FEATURES

- Industry standard pin-out in a 30-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 45mW standby, 1575mW active, typical.
- On-board power supply decoupling capacitors (0.2µf) for low noise.
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden.
- 512 cycle refresh distributed across 8ms.
- Optional Static Column access mode.

OPTIONS MARKING

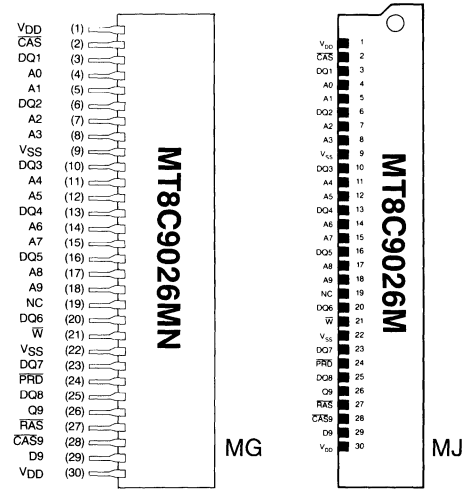
- Timing
  - 100ns access -10
  - 120ns access -12
  - 150ns access -15
- Access Mode Option
  - Static Column MT8C9026
- Packages: Leaded 30-pin SIP MN
  - Leadless 30-pin SIMM M

A0-A9	Address Inputs	$\overline{CAS}$, $\overline{CAS9}$	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
$\overline{PRD}$	Presence Detect	Q9	Data-Out
$\overline{RAS}$	Row Address Strobe	$\overline{W}$	Write Enable
V_{DD}	Power (+5V)	Vss	Ground

GENERAL DESCRIPTION

The MT8C9026M/MN is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs

PIN ASSIGNMENT (Top View)

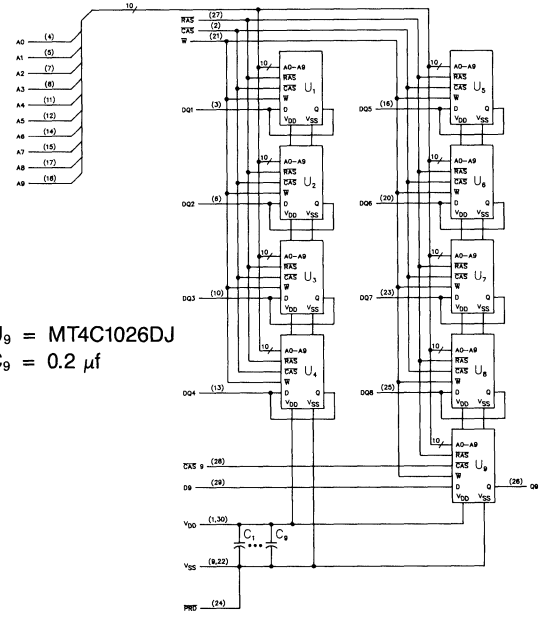


last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

STATIC COLUMN operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the STATIC COLUMN operation.

FUNCTIONAL BLOCK DIAGRAM



$U_1 - U_9$ = MT4C1026DJ
$C_1 - C_9$ = 0.2 µf

FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	TF	Addresses tR	Addresses tC		NOTES
Standby	H	H	H	GND/NC	X	X	High Impedance	
READ	L	L	H	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
STATIC COLUMN READ	L	H→L→H	H	GND/NC	ROW	COL COL	Valid Data Out, Valid Data Out	
STATIC COLUMN WRITE	L	H→L→H	L	GND/NC	ROW	COL COL	Valid Data In, Valid Data Out	
RAS ONLY REFRESH	L	H	H	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	GND/NC	X	X	High Impedance	
TEST FUNCTION	L	L	H	H	ROW	COL	Data Out, Test Funtion Mode	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 9 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C = 5.0V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: $t_{RC} = t_{RC(MIN)}$)	I_{CC1}		450	mA	3, 4
OPERATING CURRENT: STATIC COLUMN ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ = Cycling: $t_{PC} = t_{PC(MIN)}$)	I_{CC2}		450	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		18	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{CC}$ -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		9	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS} = V_{IH}$)	I_{CC5}		315	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		315	mA	3, 5
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts)	I_I	-90	90	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-90	90	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A0-A9)	C_{I1}		45	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		63	pF	2
Output Capacitance DOUT, DIN	C_O		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	190		220		260		ns	
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	14
Access time from $\overline{CAS}$	^tCAC		25		30		45	ns	15
Access time from column address	^tAA		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		50		65		75	ns	
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		30		45		ns	
$\overline{RAS}$ precharge time	^tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	15		20		25		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	75	15	90	15	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	10	50	15	60	15	70	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	50		60		70		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	5		5		5		ns	
Output buffer turn-off delay	^tOFF	0	25	0	25	0	30	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	20		25		30		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

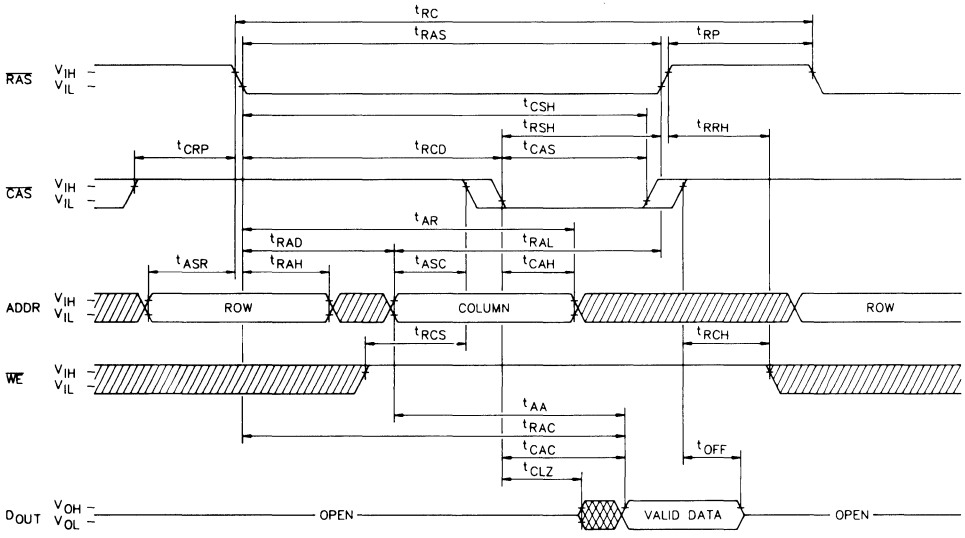
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command pulse width	^tWP	20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	15		20		25		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
Column address to $\overline{WE}$ delay time	^tAWD	50		60		70		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	100	100,000	120	100,000	150	100,000	ns	
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		15		20		ns	
STATIC COLUMN MODE cycle time	^tSC	55		65		75		ns	
Last Write to column address delay time	^tLWAD	25	45	30	55	45	70	ns	
Last Write to column address hold time	^tAHLW		95		115		135	ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	^tROH	20		20		20		ns	
Output data hold time from column address	^tAOH	5	—	5	—	5	—	ns	
Output data enable from Write	^tOW	—	25	—	25	—	25	ns	

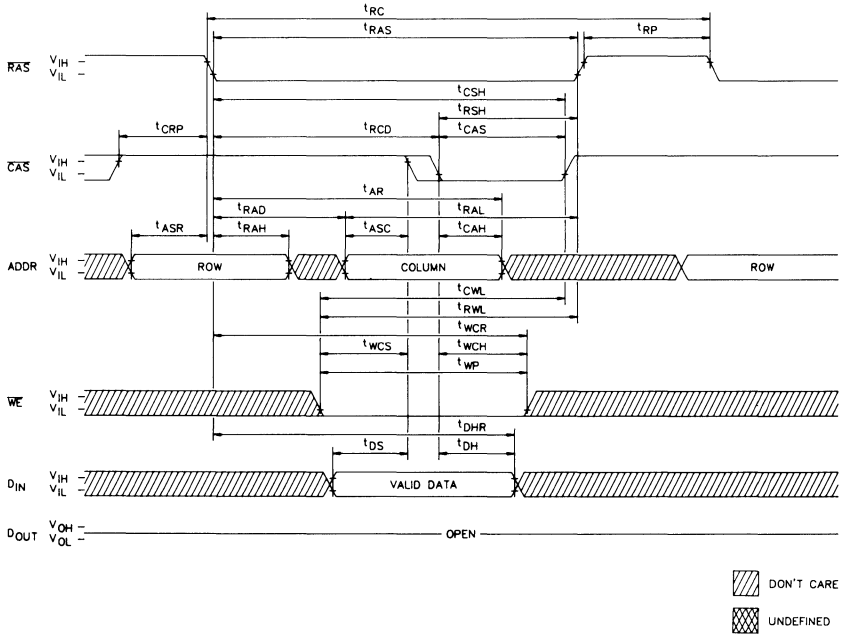
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

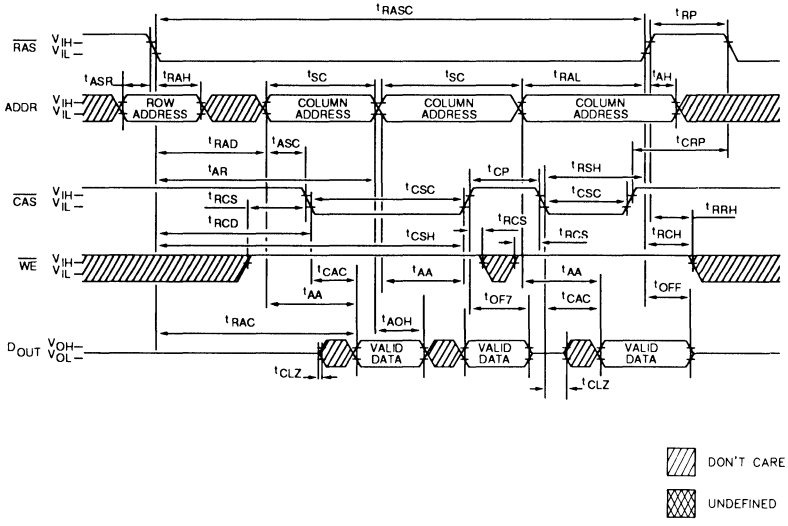
READ CYCLE



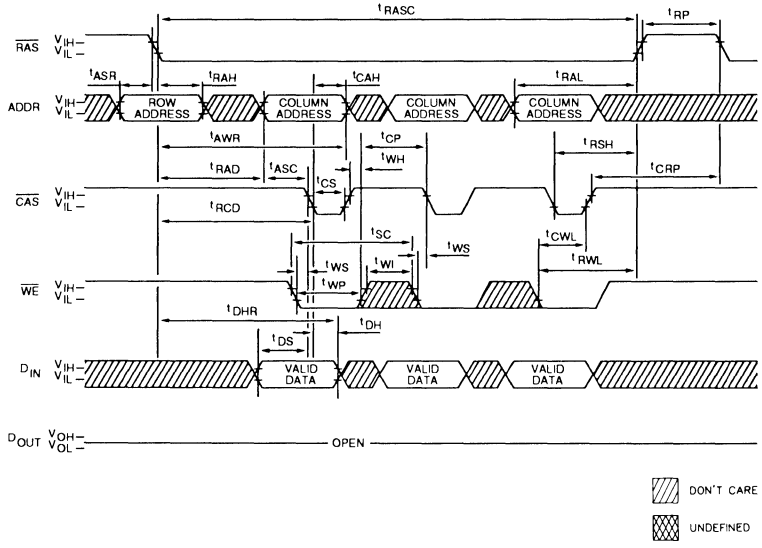
EARLY-WRITE CYCLE



STATIC COLUMN READ CYCLE

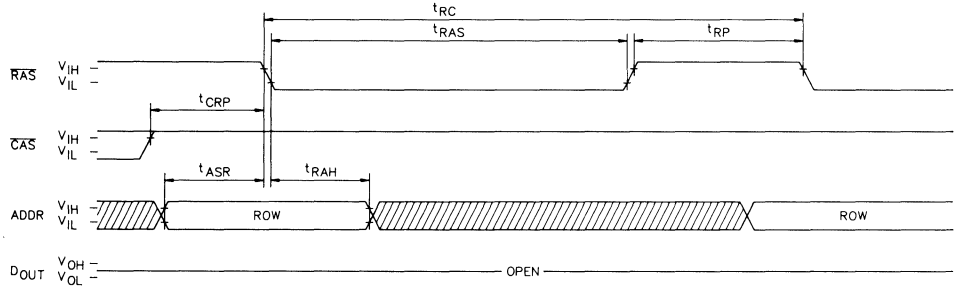


STATIC COLUMN EARLY-WRITE CYCLE



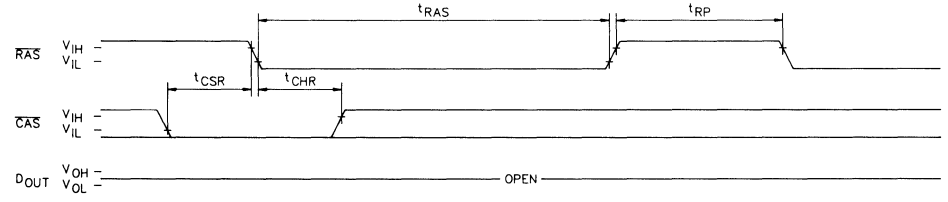
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



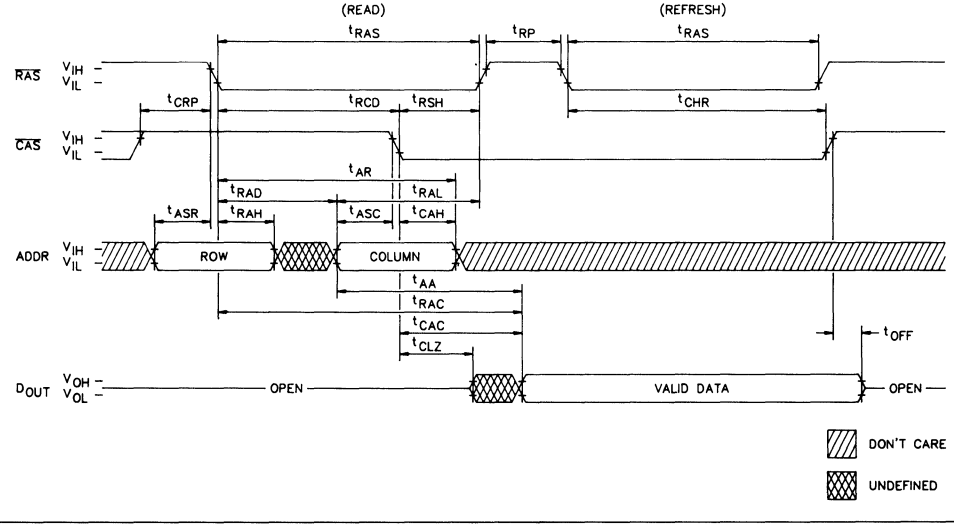
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 $\overline{WE}$, = DON'T CARE.)



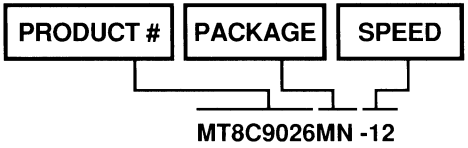
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

1 MEG x 9, 120ns access, Static Column Access, Leaded SIP



The Micron 1 MEG DRAM module family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

VRAM PRODUCT SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package & Number of Pins				Process	Page
				Standby	Active	PDIP	ZIP	SOJ	CDIP		
64K x 4	Page Mode	MT42C4064	100,120,150	10mw	150mw	24	24	24	24	CMOS	3-3
256K x 4	Fast Page Mode	MT42C4256	80,100,120,150	20mw	300mw	28	28	28	28	CMOS	3-29

FOOTNOTES:
All devices require +5 Volt ± 10% power supply.

VRAM

64K x 4 DRAM with 256 x 4 SAM

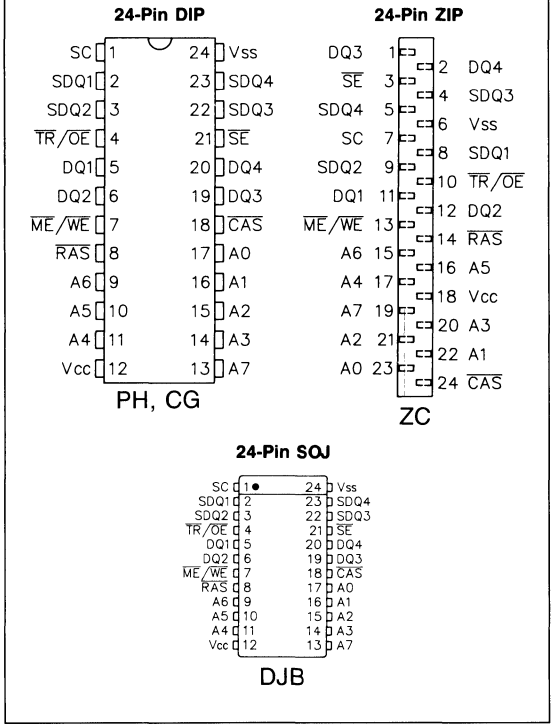
FEATURES

- Industry standard pin-out, timing, and functions
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256 cycle refresh within 4ms
- Optional PAGE MODE access cycles
- Dual port organization: 64K x 4 DRAM port
  256 x 4 SAM port
- Bit MASK-WRITE mode capability on DRAM port
- No refresh required for Serial Access Memory
- Low power: 10mW standby, 150mW active, typical
- Fast access times – 100ns parallel, 40ns serial

OPTIONS

	MARKING
• Timing (DRAM, SAM)	
100ns, 40ns	-10
120ns, 40ns	-12
150ns, 60ns	-15
• Packages	
Plastic DIP (400 mil)	None
Ceramic DIP (400 mil)	C
Plastic ZIP	Z
Plastic SOJ (300 mil)	DJ

PIN ASSIGNMENT (Top View)



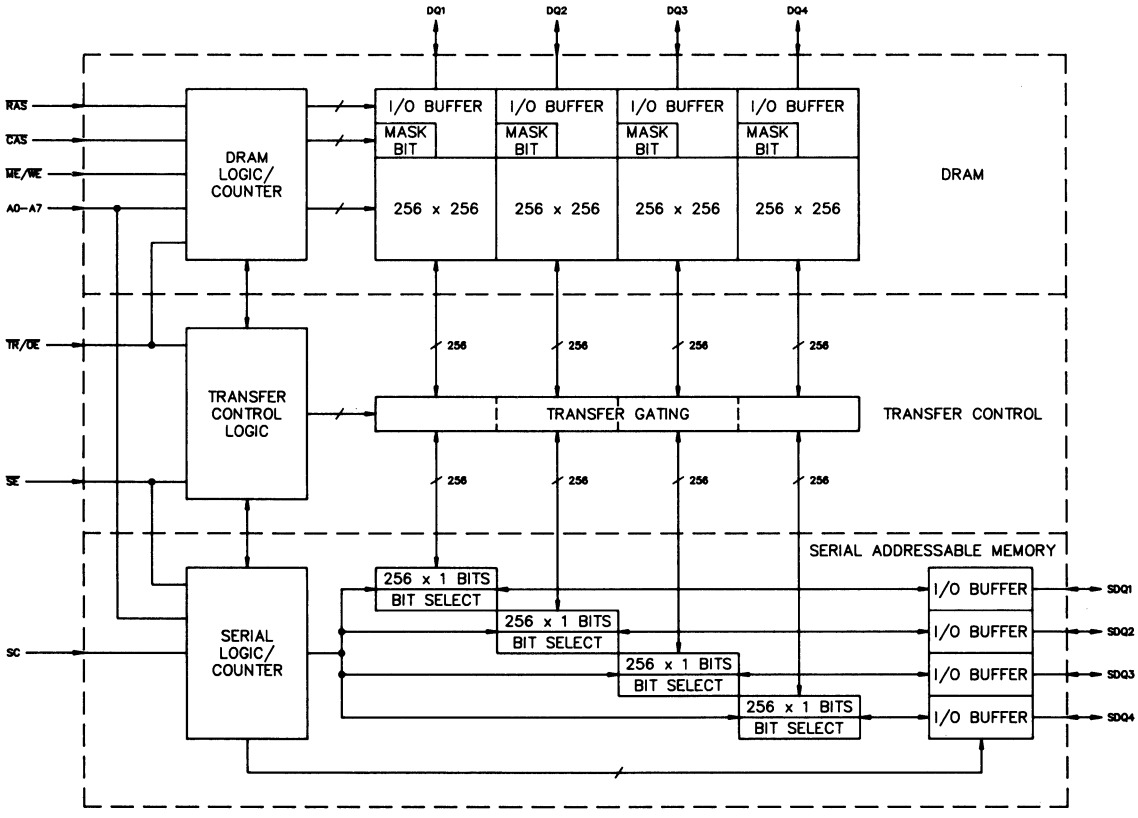
GENERAL DESCRIPTION

The MT42C4064 is a high speed, dual port CMOS dynamic random access memory (DPDRAM) containing 262,144 bits. They can be accessed either by a four bit wide DRAM port or by a 256 x 4 bit serial access memory (SAM) port. Data can be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the DPDRAM is functionally identical to the MT4067 64K x 4 bit DRAM. Four 256 bit data registers make up the serial access memory portion of the DPDRAM. Data I/O and internal data transfer is accomplished using three separate bidirectional data paths; the four bit random access I/O port, the four internal 256 bit wide paths between the DRAM and the SAM, and the four bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs the DPDRAM must be refreshed in order to maintain data. The refresh cycles must be timed so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the DPDRAM is fully static and does not require any refresh.

Figure 1
MT42C4064 BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
1	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
2, 3, 22, 23	SDQ1 - SDQ4	Input/ Output	Serial Data I/O: Input, Output, or high impedance.
4	$\overline{TR}/\overline{OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a high impedance state.
5, 6, 19, 20	DQ1 - DQ4	Input/ Output	DRAM Data I/O: Inputs, Outputs, or high impedance, and/or Mask Data Inputs: For MASK-WRITE cycle only.
7	$\overline{ME}/\overline{WE}$	Input	Mask Enable: If $\overline{ME}/\overline{WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASK-WRITE cycle is performed, or Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = H) or WRITE ($\overline{WE}$ = L) cycle when accessing the DRAM. This includes a DRAM-TO-SAM TRANSFER ($\overline{WE}$ = H) or SAM-TO-DRAM TRANSFER ($\overline{WE}$ = L).
8	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 8 Row Address bits and as a strobe for the MASK ENABLE and TRANSFER functions.
9, 10, 11, 13, 14, 15, 16, 17	A0 to A7	Input	Address Inputs: For the DRAM operation these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select 4 bits out of the 256K available. During TRANSFER operations, A0 to A7 indicate the DRAM row being accessed (when $\overline{RAS}$ goes low) and the SAM start address (when $\overline{CAS}$ goes slow).
12	V_{CC}	Supply	Power Supply: +5 Volts ±10%
18	$\overline{CAS}$	Input	Column Address Strobe: RAS is used to clock in the 8 column address bits and enable the DRAM output buffers ($\overline{TR}/\overline{OE}$ must also be LOW).
21	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a high impedance state. $\overline{SE}$ is also used during a TRANSFER operation to indicate whether a SAM-TO-DRAM TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
24	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

The DPDRAM can be divided into three functional blocks (see Figure 1); the DRAM, the Transfer Control circuitry, and the Serial Access Memory (SAM). All of the operations described below are also shown in the AC Timing Diagrams section of this data sheet as well as summarized in the Functional Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by paranthesis. For example, when discussing transfer operations the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$.*

DRAM OPERATION

The DRAM portion of the DPDRAM is functionally identical to standard 64K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or "don't care" states for the DRAM are specified for the DPDRAM. These conditions are highlighted in the following discussion.

READ/WRITE Cycles

The 16 address bits that are used to select four memory bits from the 65,536 x 4 available are latched into the chip using the A0 -A7, $\overline{RAS}$, and $\overline{CAS}$ inputs. First, the 8 row address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH to LOW. Next, the 8 column address bits are set up on the address inputs and clocked in when $\overline{CAS}$ goes from HIGH to LOW.

For single port DRAMs the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. For the DPDRAM, $(\overline{TR})/\overline{OE}$ is used, when $\overline{RAS}$ goes LOW, to select between an internal transfer operation and a DRAM operation. $(\overline{TR})/\overline{OE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition for a DRAM port READ or WRITE operation.

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1 - DQ4 port. The $(\overline{TR})/\overline{OE}$ input must be LOW to enable the DRAM output port.

For single port DRAMS, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the DPDRAM, $(\overline{ME})/\overline{WE}$ is used, when $\overline{RAS}$ goes LOW, to select between a MASK WRITE cycle and a normal WRITE cycle. If $(\overline{ME})/\overline{WE}$ is LOW at the $\overline{RAS}$ HIGH to LOW transition a MASK WRITE operation is selected. For a normal DRAM WRITE operation, $(\overline{ME})/\overline{WE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition. $(\overline{ME})/\overline{WE}$ is a "don't care" at the $\overline{RAS}$ HIGH to LOW transition for a DRAM READ cycle.

If $(\overline{ME})/\overline{WE}$ is LOW when $\overline{CAS}$ goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1 - DQ4 port will be written into the selected memory cells. If $\overline{ME}/(\overline{WE})$ is LOW when $\overline{RAS}$ goes LOW the input data will be "masked" before being stored in the DRAM.

The DPDRAM can perform all the normal DRAM cycles including EARLY-WRITE, LATE-WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE-MODE READ, PAGE-MODE WRITE, and PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in this data sheet for more details on these operations.

MASK-WRITE

If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH to LOW transition, the data (mask data) present on the DQ1 - DQ4 inputs will be written into the bit mask data register. The mask data acts as an individual write enable for each of the four DQ1 - DQ4 pins. If a LOW (logic 0) is written to a mask data register bit the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1 - DQ4 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. Since the mask data register is reset (to all 1's) at the end of every MASK-WRITE cycle, new mask data must be supplied at the beginning of each MASK-WRITE cycle. An example of a typical MASK-WRITE cycle is shown in Figure 2.

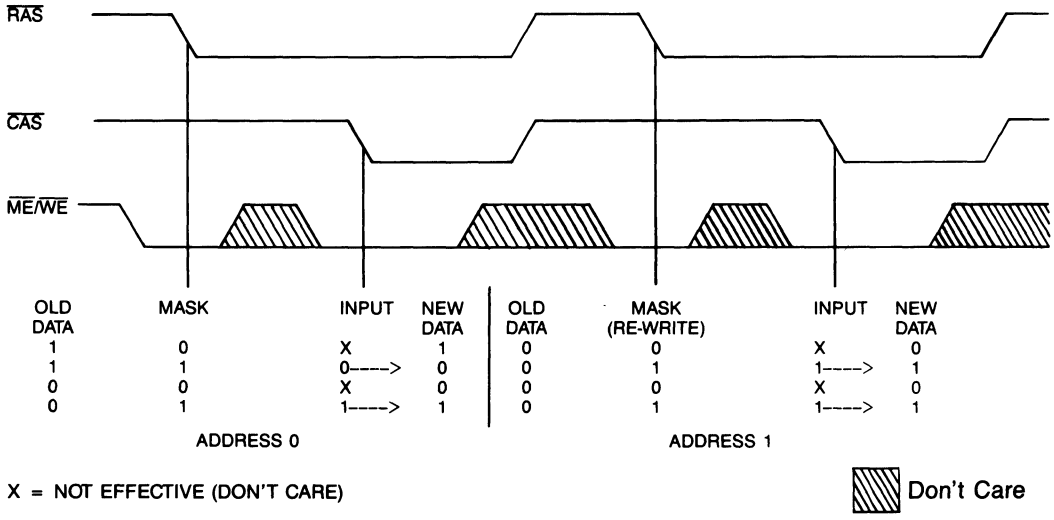


Figure 2
MT42C4064 Bit MASK-WRITE

REFRESH

The MT42C4064 supports $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN types of refresh cycles. All 256 row address combinations must be accessed within 4ms. For the $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh mode the row addresses are generated internally and the user need not supply them as he must in $\overline{RAS}$ ONLY refresh. $\overline{TR}$/($\overline{OE}$) must be HIGH when $\overline{RAS}$ goes LOW for the $\overline{RAS}$ ONLY and $\overline{CAS}$-BEFORE-$\overline{RAS}$ types of refresh cycles. Any READ, WRITE, or TRANSFER operation also refreshes the DRAM row that is being accessed.

TRANSFER OPERATION

DRAM-TO-SAM TRANSFER (READ TRANSFER)

A TRANSFER operation is initiated when $\overline{TR}/(\overline{OE})$ is LOW at $\overline{RAS}$ (HIGH to LOW) time. $(\overline{ME})/\overline{WE}$ indicates the direction of the transfer and must be HIGH as $\overline{RAS}$ goes LOW for a DRAM-TO-SAM TRANSFER. In this case, the row address bits indicate the four 256 bit DRAM rows that are to be transferred to the four SAM data registers and the column address bits indicate the start address of the next SERIAL OUTPUT cycle from the SAM data registers. $\overline{RAS}$ and $\overline{CAS}$ are used to strobe the address bits into the part. To complete the TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while $\overline{RAS}$ and $\overline{CAS}$ are still LOW. The 1024 bits of DRAM data are then written into the SAM data registers and the serial shift start address is stored in an internal 8 bit register. There must be no rising edges on the Serial Clock (SC) input while the transfer is taking place (refer to the AC timing diagrams). TRANSFER cycles are the only time when SC must be synchronized with the DRAM $\overline{RAS}$ and $\overline{CAS}$ timing. If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation.

SAM-TO-DRAM TRANSFER (WRITE TRANSFER)

The SAM-TO-DRAM TRANSFER operation is identical to the DRAM-TO-SAM TRANSFER described above except that $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row that the SAM data registers will be written to and the column address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. If $\overline{SE}$ is HIGH when $\overline{RAS}$ goes LOW, a SERIAL INPUT MODE ENABLE cycle is performed.

SAM OPERATION

SERIAL INPUT/OUTPUT MODE CONTROL

The SAM port is automatically placed in the serial output mode after a DRAM-TO-SAM TRANSFER operation. Conversely, after a SAM-TO-DRAM TRANSFER the SAM port will be in the serial input mode.

SERIAL INPUT MODE ENABLE (PSEUDO WRITE TRANSFER)

It is possible to change the direction of the SAM port from output to input without performing a SAM-TO-DRAM TRANSFER. This operation, called a SERIAL INPUT MODE ENABLE cycle, is simply a SAM-TO-DRAM TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the data registers will be ready to accept input data.

The only way to put the SAM port in the serial output mode is to do a DRAM-TO-SAM TRANSFER.

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM data register contents will start at the serial start address that was loaded during the DRAM-TO-SAM TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the four bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW to HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW, and will wrap around to location 0 after reaching its maximum count of 255.

SC is also used to clock in data when the device is in the serial input mode. As in the serial output operation, the contents of the serial address register, which was loaded when the serial input mode was enabled, will determine the serial address that the first bit will be written. $\overline{SE}$ acts as an enable for serial data input and must be LOW for normal serial input. If $\overline{SE}$ is HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address register is incremented with every L → H transition of SC, regardless of the logic level on the $\overline{SE}$ input.

FUNCTIONAL TRUTH TABLE

DRAM Operations (SC, $\overline{SE}$, and SDQ1 — SDQ4 are don't care)

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{ME}/\overline{WE}$		$\overline{TR}/\overline{OE}$		Addresses		DQ1 to DQ4	Notes
			tR*	tC*	tR*	tC*	tR*	tC*		
Standby	H	H	X	X	X	X	X	X	High Impedance	
READ	L	L	X	H	H	H→L	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	H	L	H	X	ROW	COL	Data In	1
MASK-WRITE	H→L	L	L	L	H	X	ROW	COL	Mask Data In, Valid Data In	
READ-WRITE	L	L	H	H→L	H	L→H	ROW	COL	Valid Data Out,	1
PAGE-MODE READ	L	H→L→H, H→L→H	H	H	H	H→L	ROW	COL	Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	H	L	H	X	ROW	COL	Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H, H→L→H	H	H→L	H	L→H	ROW	COL	Valid Data Out, Valid Data In	1
$\overline{RAS}$ ONLY REFRESH	L	H	X	n/a	H	n/a	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	X	H	H	L	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	X	X	H	X	X	X	High Impedance	

TRANSFER Operations (DQ1 — DQ4 are don't care)

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{ME}/\overline{WE}$		$\overline{TR}/\overline{OE}$		Addresses		SC	$\overline{SE}$	SDQ1 to SDQ4	Notes
			tR*	tC*	tR*	tC*	tR*	tC*				
DRAM-TO-SAM TRANSFER	L	L	H	X	L	L	ROW	SSA**	X	X	X	2
SAM-TO-DRAM TRANSFER	L	L	L	X	L	X	ROW	SSA**	X	L	X	3
SERIAL INPUT MODE ENABLE	L	L	L	X	L	X	ROW	SSA**	X	H	X	4

* tR = when $\overline{RAS}$ goes from HIGH to LOW
tC = when $\overline{CAS}$ goes from HIGH to LOW
** SSA = SAM Start Address, the serial address that the next serial input or output cycle will start with.

Notes: 1. Any type of WRITE cycle may also be a MASK-WRITE cycle.
2. The SAM will be in a SERIAL OUTPUT mode after a DRAM-TO-SAM TRANSFER.
3. The SAM will be in a SERIAL INPUT mode after a SAM-TO-DRAM TRANSFER.
4. The SAM will be put in the SERIAL INPUT mode but the SAM-TO-DRAM TRANSFER will not occur.

Serial I/O Operations ($\overline{RAS}$, $\overline{CAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{TR}$/$\overline{OE}$, and DQ1 - DQ4 are don't care)

Function	SC	$\overline{SE}$	SDQ1 — SDQ4	Notes
SERIAL OUTPUT	L→H	L	Valid Data Out	5
SERIAL INPUT	L→H	L	Valid Data In	6

Notes: 5. The SAM must be in the SERIAL OUTPUT mode.
6. The SAM must be in the SERIAL INPUT mode.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Operating Temperature, Ta(Ambient) .....0°C to +70°C
Storage Temperature (Ceramic) .....-65°C to +150°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation .....1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(Notes 3, 4, 5) ($0°C \le T_A \le 70°C$, Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input (0V≤VIN≤Vcc, all other pins not under test = 0 volts).	IL	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V≤VOUT≤Vcc).	Ioz	-10	10	µA	
OUTPUT LEVELS Output High voltage (IOUT = -5mA)	VOH	2.4		V	
Output Low voltage (IOUT = 5mA)	VOL		0.4	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_7), D_{IN}	C_{I1}		5	pF	18
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, SC, $\overline{SE}$	C_{I2}		7	pF	18
Output Capacitance D_{OUT}	C_O		7	pF	18

CURRENT DRAIN, SAM IN STANDBY

(Notes 2, 3) ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION OF DRAM	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$=Cycling; $T_{RC}=T_{RC(MIN)}$).	I_{CC1}		40	mA	4
OPERATING CURRENT: PAGE-MODE ($\overline{RAS}=V_{IL}$,$\overline{CAS}$=Cycling; $T_{PC}=T_{PC(MIN)}$).	I_{CC2}		40	mA	4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}=\overline{CAS}=V_{IH}$ after 8 $\overline{RAS}$ cycles min).	I_{CC3}		10	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}=\overline{CAS}=V_{CC}$-0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V).	I_{CC4}		4	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}=V_{IH}$).	I_{CC5}		30	mA	
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling).	I_{CC6}		30	mA	5
SAM/DRAM DATA TRANSFER	I_{CC7}		60	mA	

CURRENT DRAIN, SAM ACTIVE (tsc = MIN)

(Notes 2, 3) ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION OF DRAM	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$=Cycling; $T_{RC}=T_{RC(MIN)}$).	I_{CC8}		60	mA	4
OPERATING CURRENT: PAGE-MODE ($\overline{RAS}=V_{IL}$,$\overline{CAS}$=Cycling; $T_{PC}=T_{PC(MIN)}$).	I_{CC9}		60	mA	4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}=\overline{CAS}=V_{IH}$ after 8 $\overline{RAS}$ cycles min).	I_{CC10}		30	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}=\overline{CAS}=V_{CC}$-0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V).	I_{CC11}		25	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}=V_{IH}$).	I_{CC12}		50	mA	
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling).	I_{CC13}		50	mA	5
SAM/DRAM DATA TRANSFER	I_{CC14}		90	mA	

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 10, 11, 17) (0°C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	250		295		345		ns	20, 21
PAGE-MODE READ or WRITE cycle time	^tPC	75		90		110		ns	6, 7
PAGE-MODE READ-MODIFY-WRITE cycle time	^tPRWC	125		150		175		ns	20, 21
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ pulse width (PAGE-MODE)	^tRASP	100	100,000	120	100,000	150	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	15		20		25		ns	
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	15		20		25		ns	19
$\overline{RAS}$ to $\overline{CAS}$ delay	^tRCD	10	50	15	60	15	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		15		ns	
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	20		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		80		ns	
READ command set-up time	^tRCS	0		0		0		ns	
READ command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
READ command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	

DRAM TIMING PARAMETERS (Continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 10, 11, 17) (0°C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	16
WRITE command hold time	^tWCH	20		25		30		ns	
WRITE command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	
WRITE command pulse width	^tWP	20		25		30		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		20		25		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	65		80		95		ns	16, 20
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	120		150		185		ns	16, 20
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ Set Up Time	^tWSR	0		0		0	ns		
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ Hold Time	^tRWH	10		10		15	ns		
Mask Data (DQ_) to $\overline{RAS}$ Set Up Time	^tMS	0		0		0		ns	
Mask Data (DQ_) to $\overline{RAS}$ Hold Time	^tMH	20		20		25		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	
Refresh Period (256 cycles)	^tREF		4		4		4	ms	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before- refresh)	^tCHR	20		25		30		ns	22
$\overline{CAS}$ to output in low-Z	^tCLZ	5		5		5		ns	
Output buffer turn-off delay	^tOFF	0	25	0	25	0	30	ns	12
Output Enable	^tOE		25		25		30	ns	
Output Disable	^tOD		25		25		30	ns	

NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms static refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, DRAM data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, DRAM data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and to $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min) the cycle is an EARLY-WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $^tCWD \geq ^tCWD$ (min) and $^tRWD \geq ^tRWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back toV_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCP. Note 8 applies to determine valid data out.
20. Includes the $\overline{OE}$ delay time (30ns for the -10, 40ns for the -12, and 50ns for the -15).
21. During a READ cycle if $\overline{OE}$ is low then taken high (V_{IH}) D_{OUT} goes open. If $\overline{OE}$ is tied permanently low a READ-MODIFY-WRITE operation is not possible.
22. Enables on-chip refresh and address counters.
23. TRANSFER Command means that $\overline{TR}/(\overline{OE})$ is LOW when $\overline{RAS}$ goes LOW.
24. NON-TRANSFER Command means that $\overline{TR}/(\overline{OE})$ is HIGH when $\overline{RAS}$ goes LOW.
25. Measured with a load equivalent to 2 TTL gates and 50pF.

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 17, 25) (0° C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
TRANSFER Command to $\overline{RAS}$ Set Up Time	^tTS	0		0		0		ns	23
TRANSFER Command to $\overline{RAS}$ Hold Time	^tRTH	80		90		100		ns	23
TRANSFER Command to $\overline{CAS}$ Hold Time	^tCTH	30		30		35		ns	23
TRANSFER Command to SC Lead Time	^tTSL	5		5		10		ns	23
TRANSFER Command to $\overline{RAS}$ Lead Time	^tTRL	10		10		10		ns	23
TRANSFER Command to $\overline{RAS}$ Delay Time	^tTRD	15		15		20		ns	23
TRANSFER Command to $\overline{CAS}$ Time	^tTCL	10		10		10		ns	23
TRANSFER Command to $\overline{CAS}$ Delay Time	^tTCD	15		15		20		ns	23
First SC edge to TRANSFER Command Delay Time	^tTSD	10		10		20		ns	23
SAM-TO-DRAM (WRITE) Transfer Command to $\overline{RAS}$ Hold Time	^tRTHW	10		10		15		ns	
Serial Output Buffer Turn Off Delay from $\overline{RAS}$	^tSDZ	10	40	10	50	10	60	ns	
SC to $\overline{RAS}$ Set Up Time	^tSRS	35		40		45		ns	
$\overline{RAS}$ to SC Delay Time	^tSRD	25		30		35		ns	
Serial Data Input to SE Delay Time	^tSZE	0		0		0		ns	
$\overline{RAS}$ to SD Buffer Turn On Time	^tSRO	0		0		0		ns	
Serial Data Input Delay from $\overline{RAS}$	^tSDD	50		55		60		ns	
Serial Data Input to $\overline{RAS}$ Delay Time	^tSZS	0		0		0		ns	
Serial Input Mode Enable (SE) to $\overline{RAS}$ Set Up Time	^tESR	0		0		0		ns	
Serial Input Mode Enable (SE) to $\overline{RAS}$ Hold Time	^tREH	10		10		15		ns	
NON-TRANSFER Command to $\overline{RAS}$ Set Up Time	^tYS	0		0		0		ns	24
NON-TRANSFER Command to $\overline{RAS}$ Hold Time	^tYH	10		10		10		ns	24

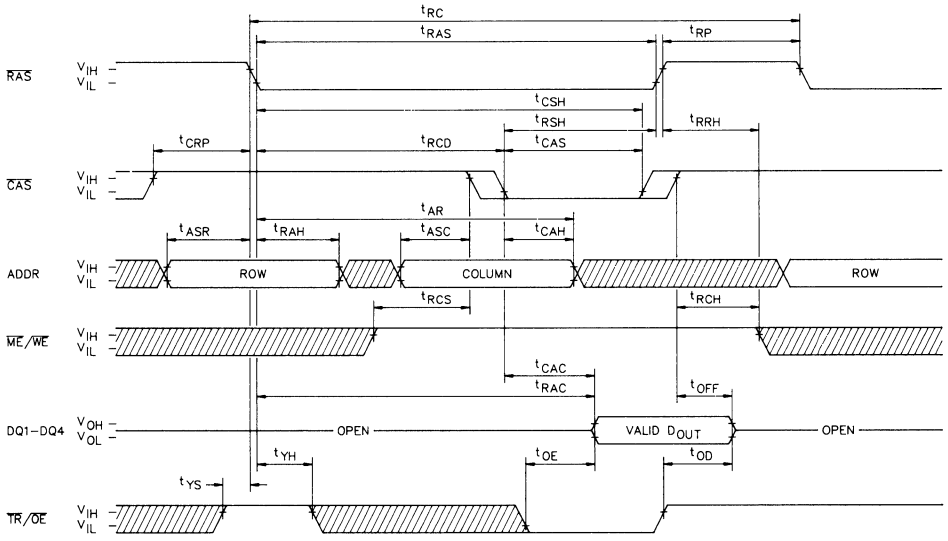
SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

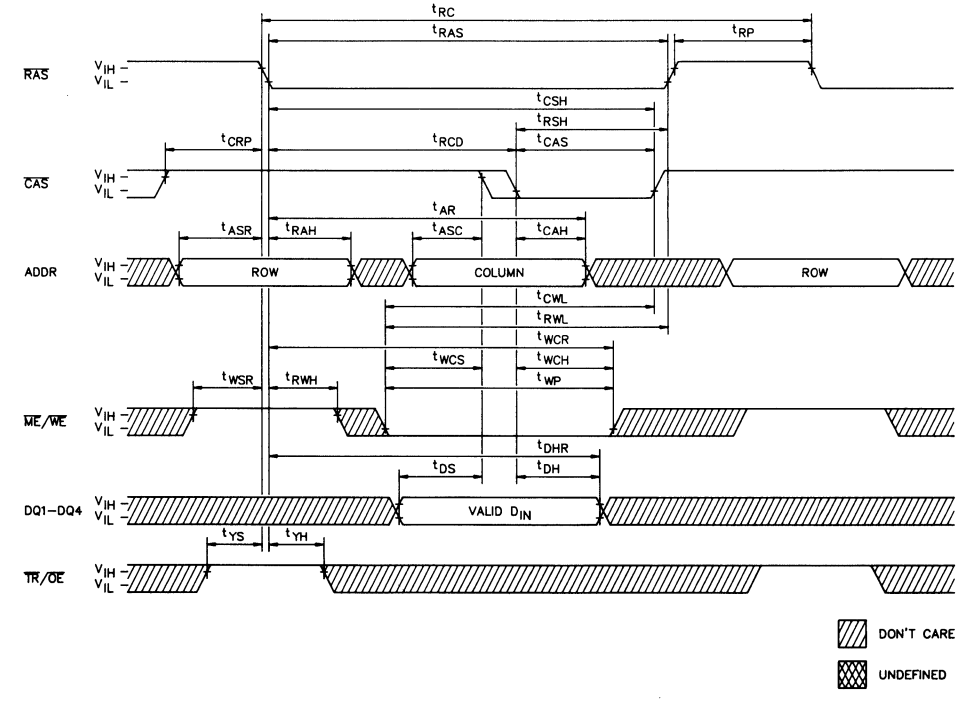
(Notes 3, 4, 5, 17, 25) (0° C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial Clock Cycle Time	^tSC	40	50000	40	50000	60	50000	ns	
Access Time from SC	^tSAC		40		40		60	ns	
SC Precharge Time	^tSP	10		10		20		ns	
SC Pulse Width	^tSAS	10		10		20		ns	
Access Time from SE	^tSEA		25		30		40	ns	
SE Precharge Time	^tSEP	15		15		20		ns	
SE Pulse Width	^tSE	15		15		20		ns	
Serial Data Out Hold Time after SC High	^tSOH	10		10		10		ns	
Serial Output Buffer Turn Off Delay from SE	^tSEZ	0	15	0	25	0	30	ns	
Serial Data in Set Up Time	^tSDS	0		0		0		ns	
Serial Data in Hold Time	^tSDH	20		20		25			
SERIAL INPUT (Write) Enable Set Up Time	^tSWS	0		0		0		ns	
SERIAL INPUT (Write) Enable Hold Time	^tSWH	30		35		45		ns	
SERIAL INPUT (Write) Disable Set Up Time	^tSWIS	0		0		0		ns	
SERIAL INPUT (Write) Disable Hold Time	^tSWIH	30		35		45		ns	

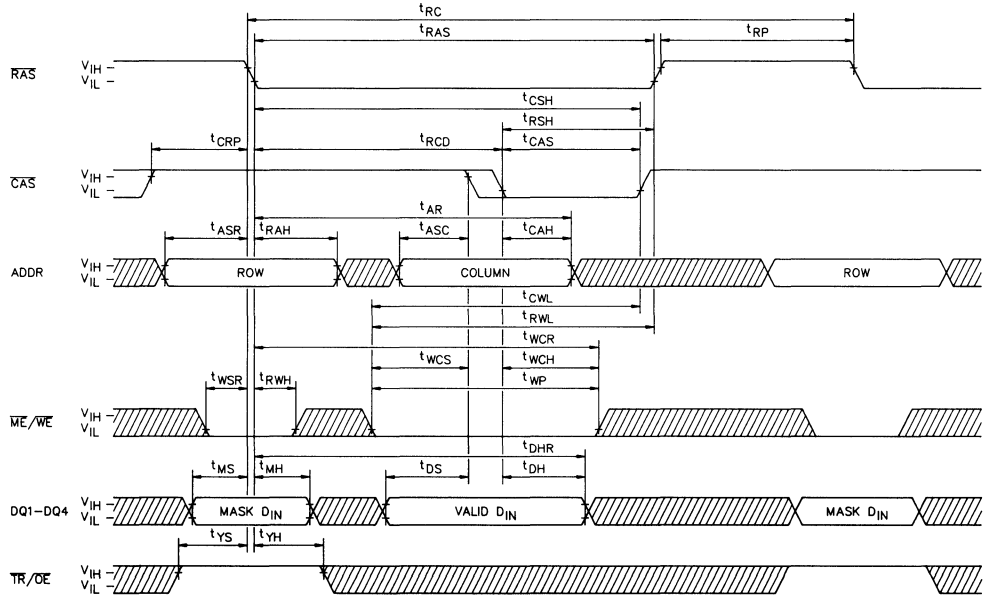
DRAM READ CYCLE



DRAM EARLY-WRITE CYCLE

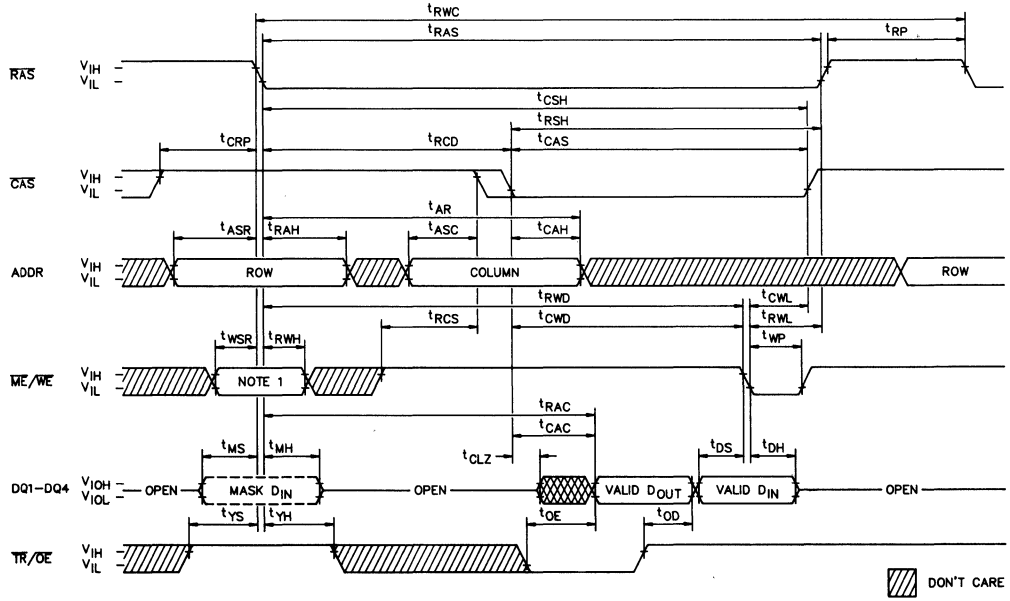


DRAM MASK-WRITE CYCLE



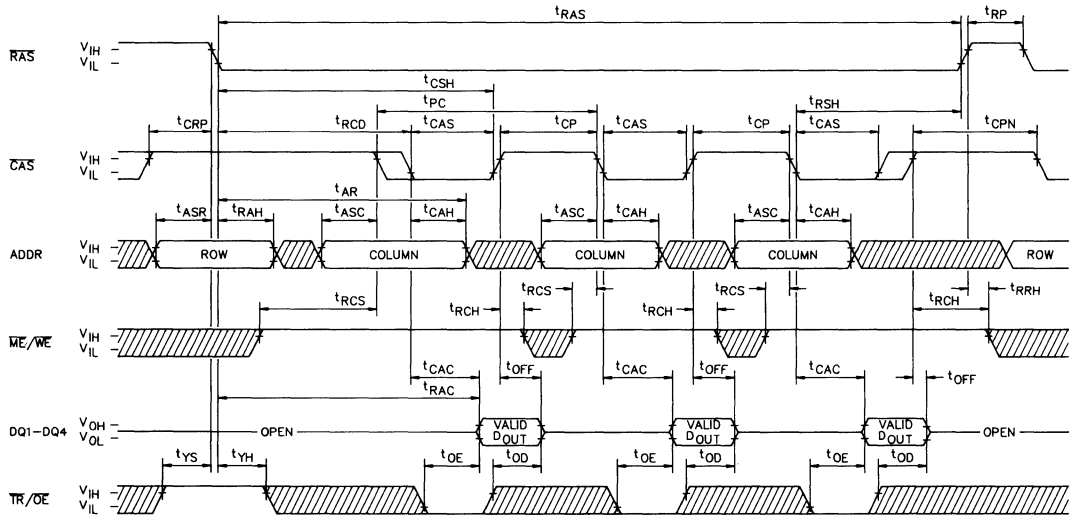
DRAM READ-WRITE CYCLE

(READ-MODIFY-WRITE CYCLE and LATE-WRITE CYCLE)

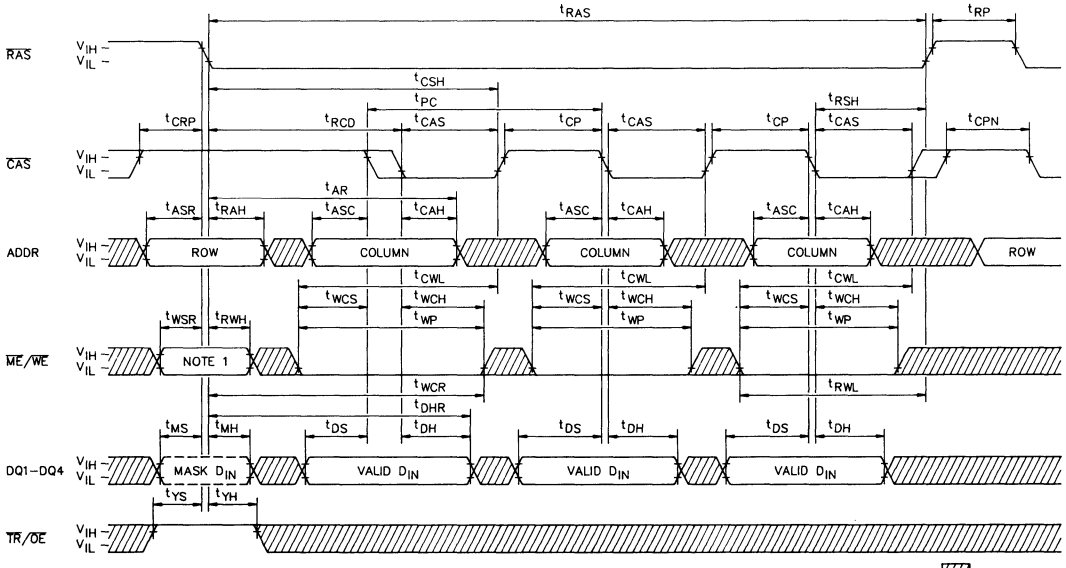


NOTE 1: If $\overline{ME}/\overline{WE}$ is LOW, a MASK-WRITE cycle will be performed.

DRAM PAGE-MODE READ CYCLE

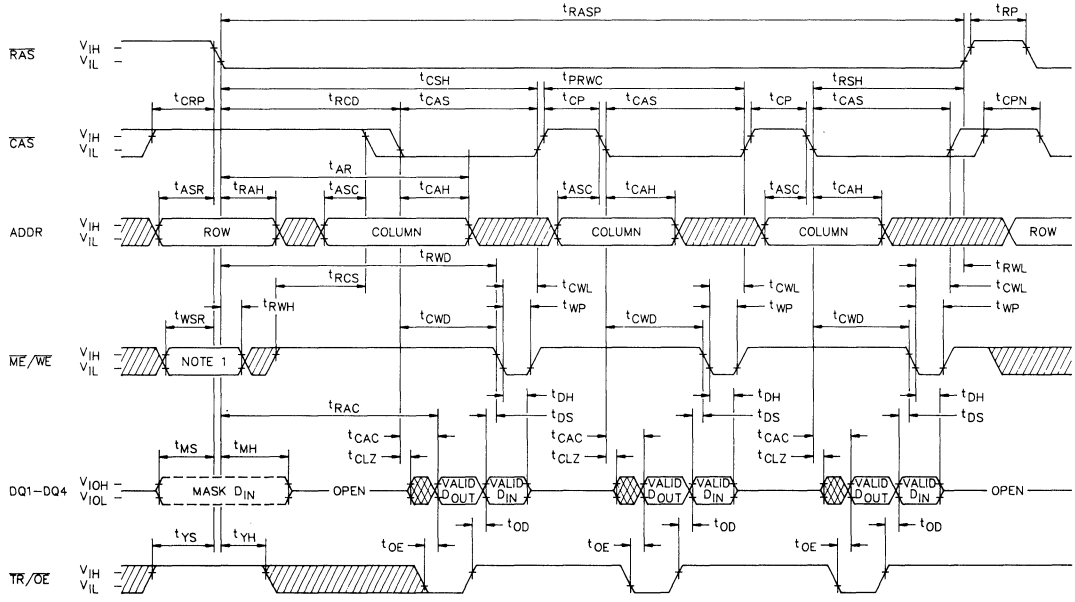


DRAM PAGE-MODE EARLY-WRITE CYCLE



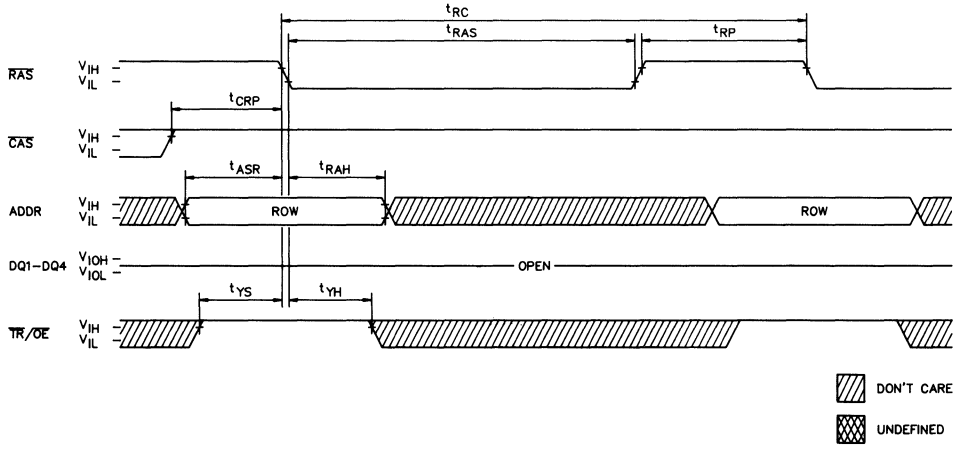
NOTE: If $\overline{ME}/\overline{WE}$ is LOW, a MASK-WRITE cycle will be performed.

DRAM PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



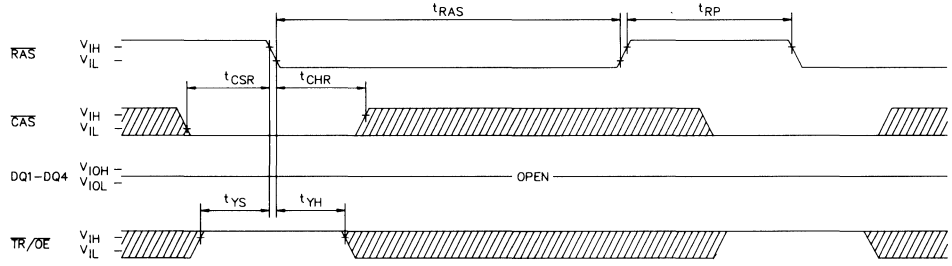
NOTE: 1: If $\overline{ME}/\overline{WE}$ is LOW, a MASK-WRITE cycle will be performed

$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{ME}/\overline{WE}$ = Don't Care)

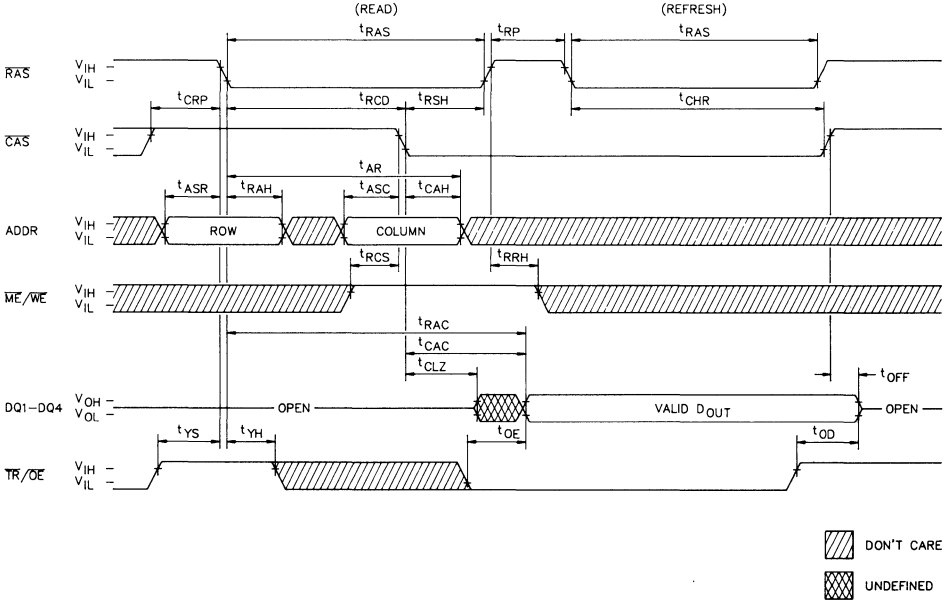


$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE

(A_0 - A_7 and $\overline{\text{ME}}/\overline{\text{WE}}$ are Don't Care.)

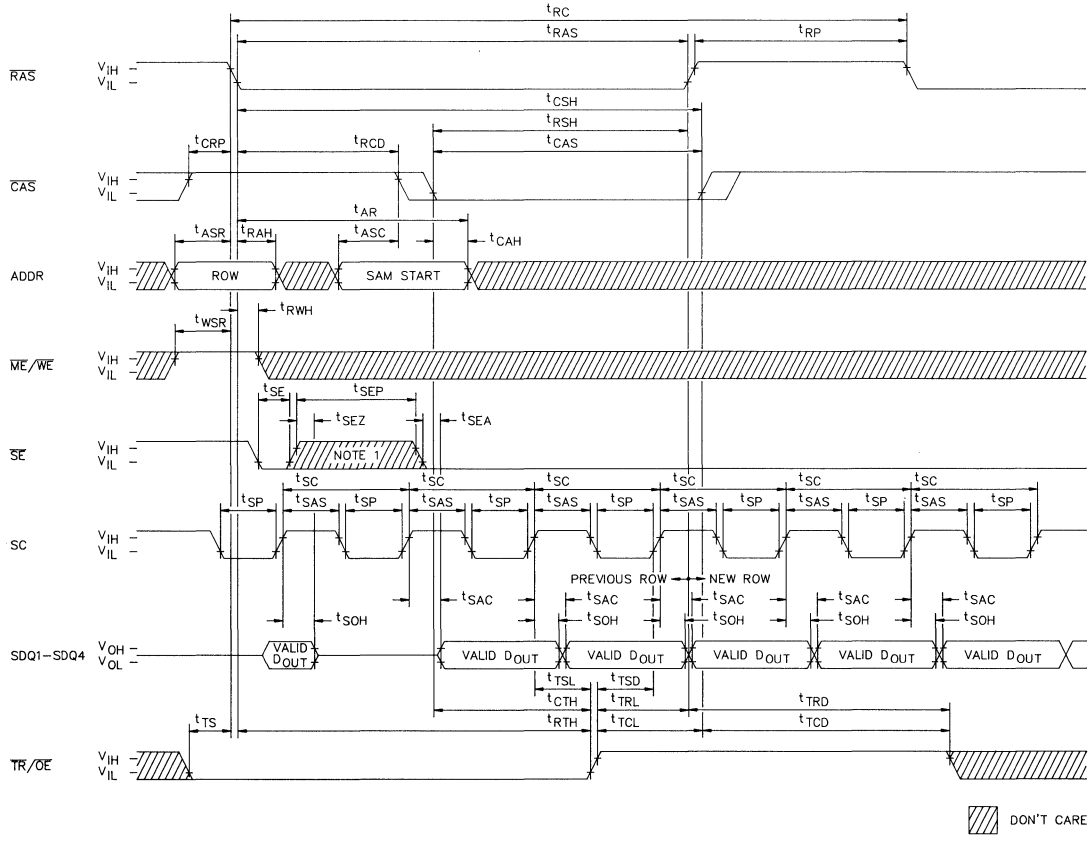


HIDDEN REFRESH CYCLE



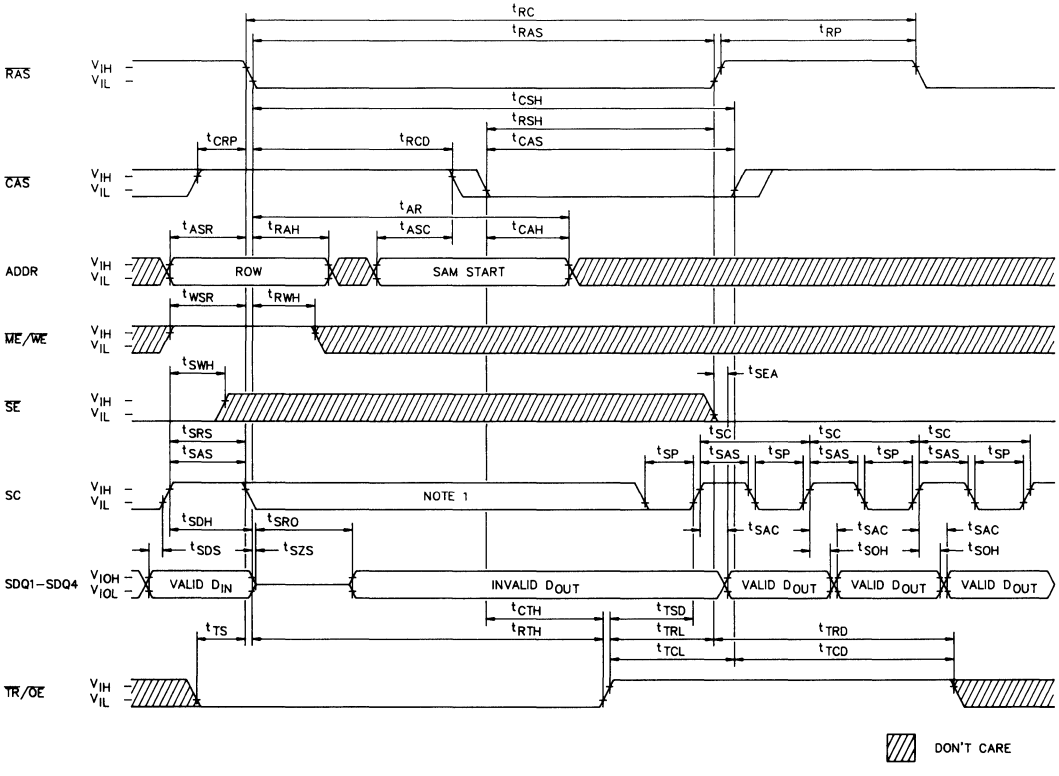
NOTE: A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{\text{ME}}/\overline{\text{WE}}$ = LOW (when $\overline{\text{CAS}}$ goes LOW) and $\overline{\text{TR}}/\overline{\text{OE}}$ = HIGH.

DRAM-TO-SAM TRANSFER
(READ TRANSFER)
(When part was previously in the SERIAL OUTPUT mode.)



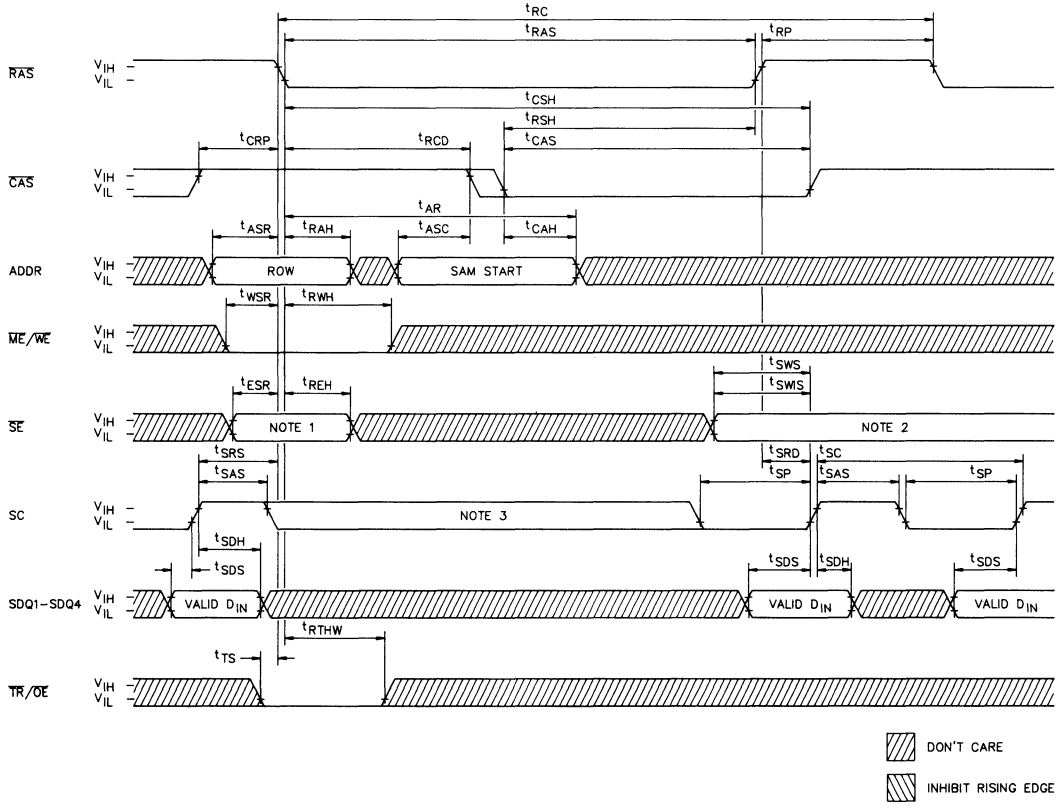
NOTE 1: This $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

DRAM-TO-SAM TRANSFER
(READ TRANSFER)
(When part was previously in the SERIAL INPUT mode.)



NOTE 1: There must be no rising edges on the SC input during this time.

SAM-TO-DRAM TRANSFER
(WRITE TRANSFER)
(When part was previously in the SERIAL INPUT mode.)

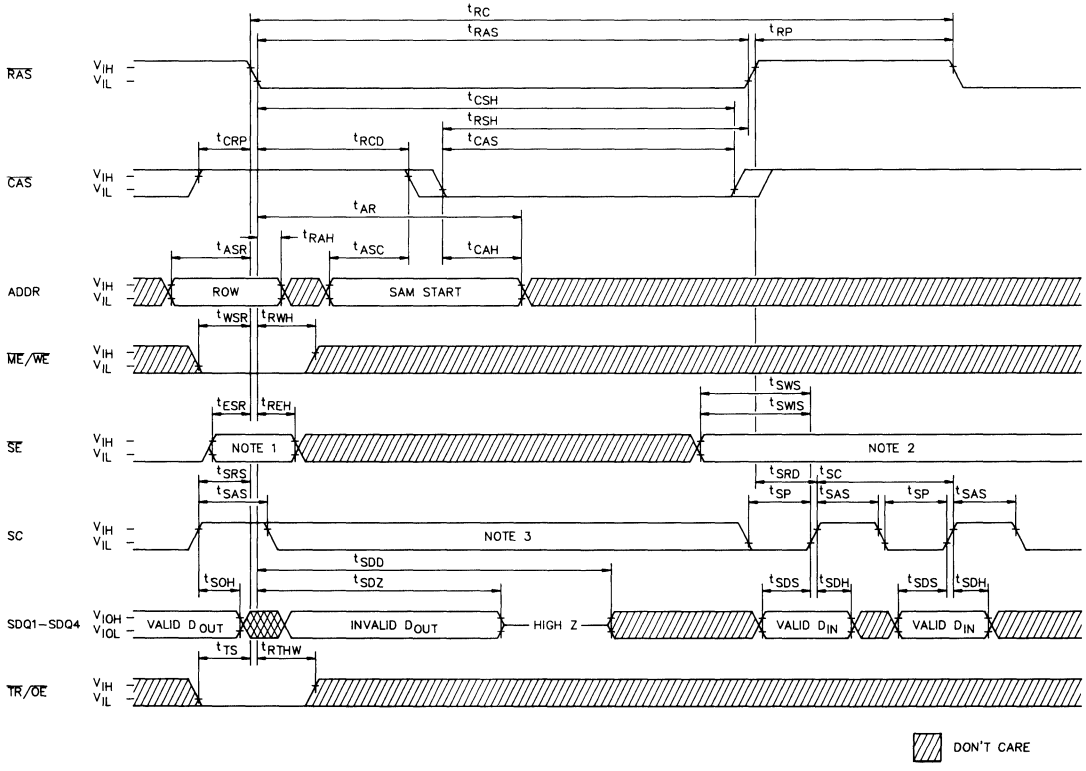


NOTE 1: If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

NOTE 3: There must be no rising edges on the SC input during this time.

SAM-TO-DRAM TRANSFER
(WRITE TRANSFER or PSEUDO WRITE TRANFER)
(When part was perviously in the SERIAL OUTPUT mode.)

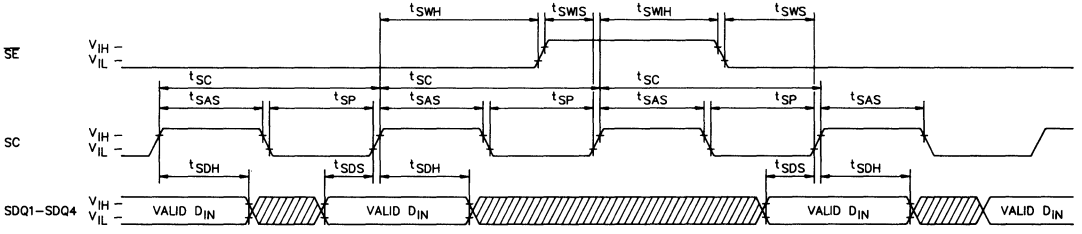


NOTE 1: If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

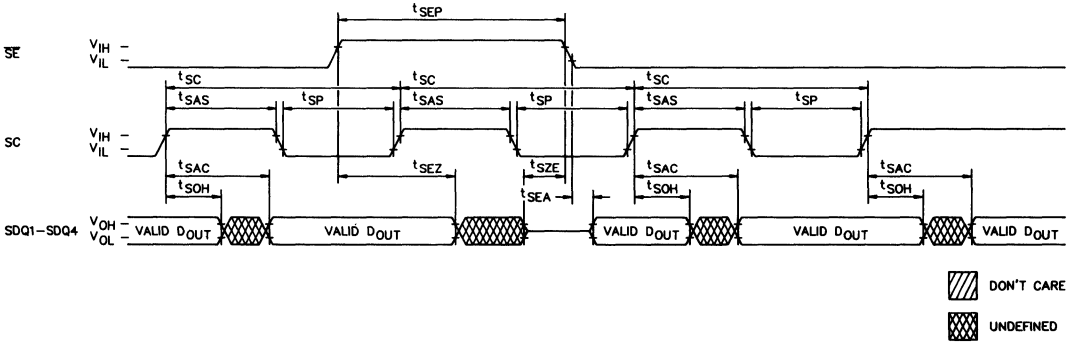
NOTE 2: $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

NOTE 3: There must be no rising edges on the SC input during this time.

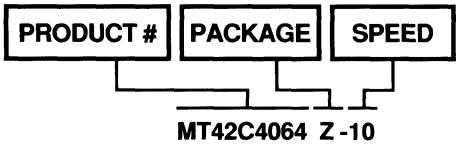
SAM SERIAL INPUT



SAM SERIAL OUTPUT



ORDER INFORMATION



The Micron MT42C4064 is functionally equivalent to other manufacturer's products meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the high speed, low power CMOS double poly, single metal process. Micron's QUALITY ASSURED policy is to offer prompt, accurate, and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply, temperature, and refresh range than specified. Each unit receives accelerated burn-in and and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

VRAM

256K x 4 DRAM with 512 x 4 SAM

FEATURES

- Industry standard pin-out, timing, and functions
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512 cycle refresh within 8ms
- Optional FAST PAGE MODE access cycles
- Dual port organization: 256K x 4 DRAM port
  512 x 4 SAM port
- No refresh required for Serial Access Memory
- Low power: 5mw standby, 200mw active, typical
- Fast access times – 80ns random, 25ns serial

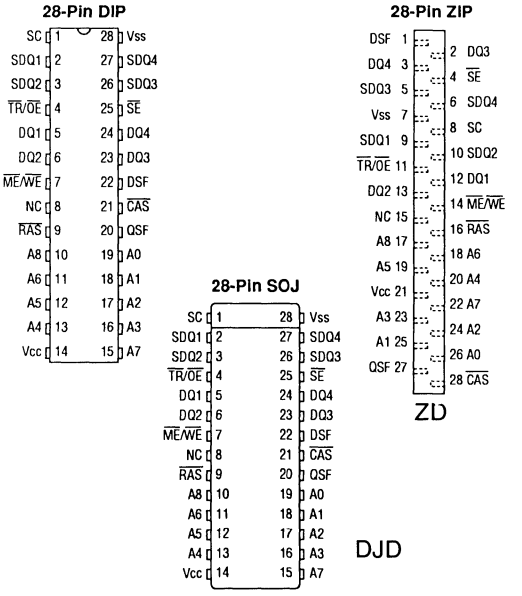
SPECIAL FUNCTIONS

- Masked Write
- Persistent Masked Write
- Split READ and WRITE Transfers
- Block Write
- Serial Input

OPTIONS / MARKING

OPTIONS	MARKING
• Timing (DRAM, SAM)	
80ns, 25ns	-8
100ns, 30ns	-10
120ns, 35ns	-12
150ns, 40ns	-15

PIN ASSIGNMENT (Top View)



NOTE: 28-Pin Packaging To Be Determined.

GENERAL DESCRIPTION

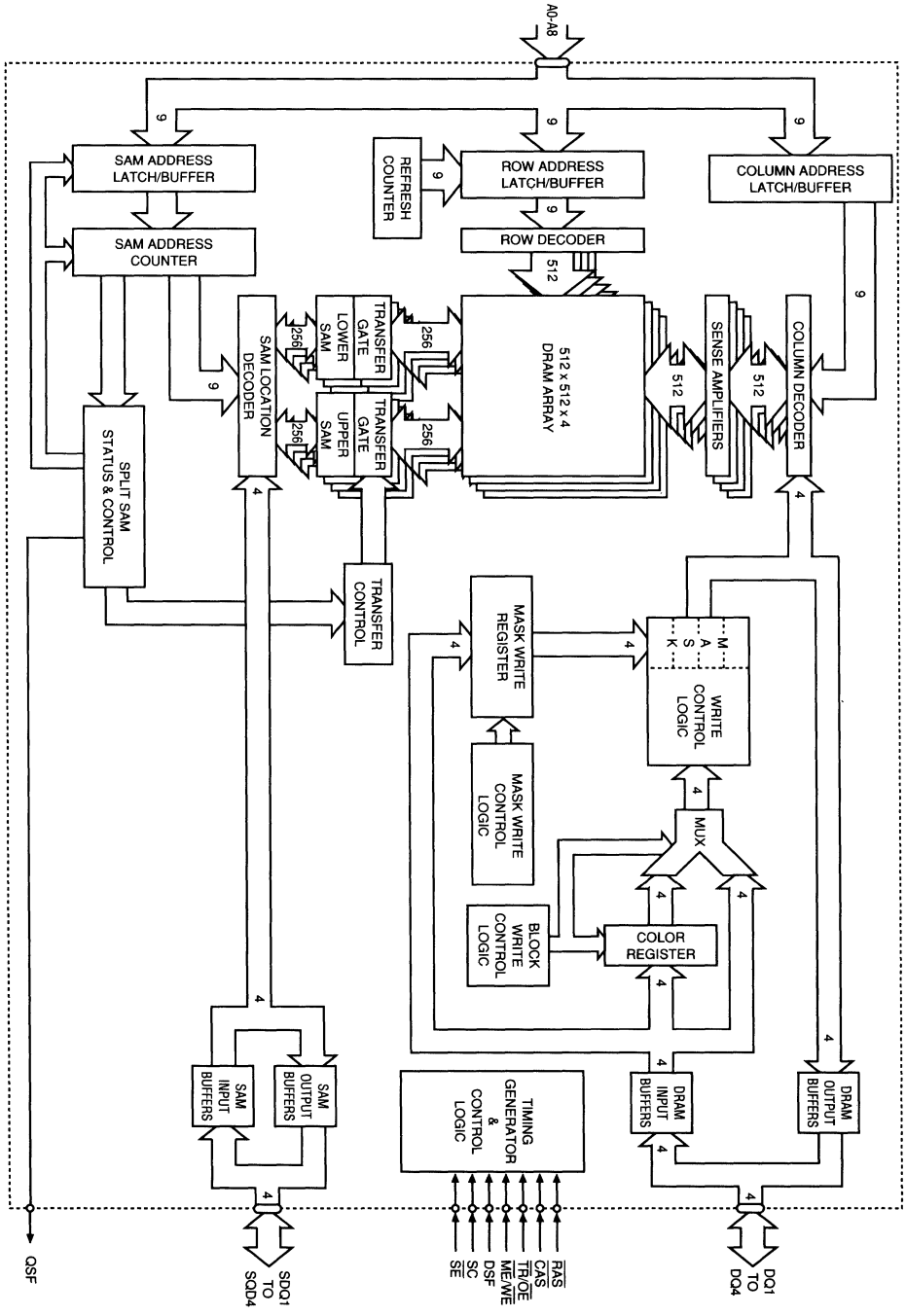
The MT42C4256 is a high speed, dual port CMOS dynamic random access memory (DPDRAM) containing 1,048,576 bits. They can be accessed either by a four bit wide DRAM port or by a 512 x 4 bit serial access memory (SAM) port. Data can be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the DPDRAM is functionally identical to the MT4C4256 (256K x 4) bit DRAM. Four 512 bit data registers make up the serial access memory portion of the DPDRAM. Data I/O and internal data transfer is accomplished using three separate bidirectional data paths; the four bit random access I/O port, the four internal 512 bit wide paths between the DRAM and the SAM, and the four bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs the DPDRAM must be refreshed in order to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the DPDRAM is fully static and does not require any refresh.

The operation and control of the MT42C4256 is compatible with (and can be identical to) the operation of the MT42C4064 64Kx4 Video RAM. However, the MT42C4256 offers several additional functions which may be used to increase system performance or ease critical timing requirements. These "special functions" are described in detail in the following section.

MT42C4256 BLOCK DIAGRAM



PIN DESCRIPTIONS

DIP/SOJ PIN NUMBER(S)	ZIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
5, 6, 23, 24	12, 13, 2, 3	DQ1 - DQ4	Input/ Output	DRAM Data I/O, inputs for MASK REGISTER and COLOR REGISTER load cycles, and ADDRESS MASK inputs for BLOCK WRITE.
19, 18, 17, 16, 13, 12, 11, 15, 10	26, 25, 24, 23, 20, 19, 18, 22, 17	A0 to A8	Input	Address Inputs: For the DRAM operation these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select 4 bits out of the 256K x 4 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes low) and the SAM start address (when $\overline{CAS}$ goes low).
9	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 Row Address bits and as a strobe for the $\overline{ME/WE}$, $\overline{TR/OE}$, and DSF inputs.
21	28	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 9 column address bits and enable the DRAM output buffers (along with $\overline{TR/OE}$) and as a strobe for the DSF input.
7	14	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASK-WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
4	11	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a high impedance state.
2, 3, 26, 27	9, 10, 5, 6	SDQ1 - SDQ4	Input/ Output	Serial Data I/O: Input, Output, or high impedance.
1	8	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
25	4	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a high impedance state. $\overline{SE}$ is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
22	1	DSF	Input	Special Function Select: DSF is used to indicate which special functions (Block Write, Masked Write vs. Persistent Masked Write, etc.) are used on a particular access cycle.
20	27	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed when the Split SAM Transfer mode is being used.
8	15	NC	–	No Connect - This pin should be either left unconnected or tied to ground.
14	21	Vcc	Supply	Power Supply: +5 Volts ±10%
28	7	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C4256 can be divided into three functional blocks (see Figure 1); the DRAM, the Transfer circuitry, and the Serial Access Memory (SAM). All of the operations described below are also shown in the AC Timing Diagrams section of this data sheet as well as summarized in the Functional Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by paranthesis. For example, when discussing transfer operations the TR/OE pin will be shown as TR/(OE).*

DRAM OPERATION

DRAM REFRESH

Like any DRAM based memory, the MT42C4256 Video RAM must be refreshed in order to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C4256 supports CAS-BEFORE-RAS, RAS ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS refresh mode the row addresses are generated and stored in an internal address counter. The user need not supply any address data and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for RAS ONLY refresh cycles. The DQ I/O pins remain in a high -Z state for both the RAS ONLY and CAS-BEFORE-RAS refresh cycles.

HIDDEN refresh cycles are performed by toggling RAS (and keeping CAS low) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS refresh cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM portion of the MT42C4256 does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the DPDRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or "don't care" states for the DRAM are specified for the DPDRAM. These conditions are highlighted in the following discussion. In addition, the DPDRAM has several special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select four memory bits from the 262,144 x 4 available are latched into the chip using the A0-A8, RAS and CAS inputs. First, the 9 row address bits are set-up on the address inputs and clocked into the part when RAS transitions from high to low. Next, the 9 column address bits are set-up on the address inputs and clocked in when CAS goes from high to low.

For single port DRAMS the OE pin is a "don't care" when RAS goes low. For the DPDRAM, (TR)/OE is used, when RAS goes low, to select between DRAM and TRANSFER CYCLES. (TR)/OE must be high at the RAS high to low transistion for all DRAM operations (except CAS-BEFORE-RAS refresh).

If (ME)/WE is high when CAS goes low, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The (TR)/OE input must transistion from high to low sometime after RAS falls in order to enable the DRAM output port.

For single port normal DRAMs, WE is a "don't care" when RAS goes low. For the DPDRAM, (ME)/WE is used, when RAS goes low, to select between a MASK WRITE cycle and a normal WRITE cycle. If (ME)/WE is low at the RAS high to low transition a MASK WRITE operation is selected. For a normal DRAM WRITE operation, (ME)/WE must be high at the RAS high to low transition. (ME)/WE is a "don't care" at the RAS high to low tansition for a DRAM READ cycle.

If (ME)/WE is low when CAS goes low, a DRAM WRITE operation is performed and the data present on the DQ1-DQ4 data port will be written into the selected memory cells. If ME/(WE) is low when RAS goes low the input data will be "masked" before being stored in the DRAM.

The DPDRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, PAGE-MODE READ, PAGE-MODE WRITE, and PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

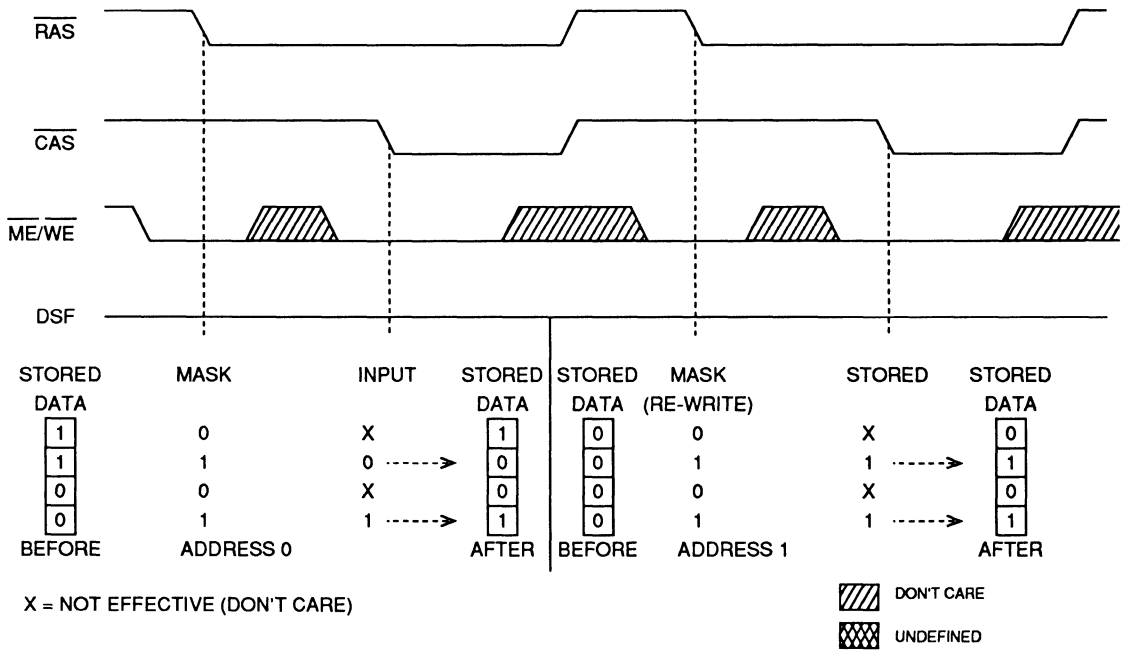
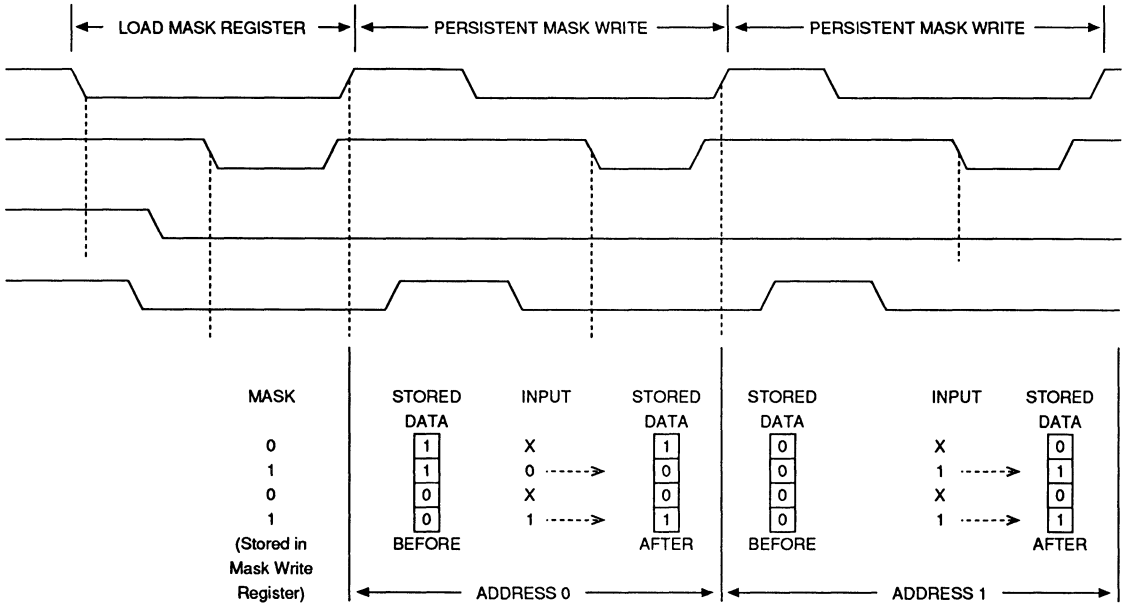


Figure 2
NON-PERSISTENT MASKED WRITE EXAMPLE

NON-PERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only certain bits within a four bit word. The MT42C4256 supports two types of MASKED WRITE cycles, NON-PERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$) is low and DSF is low at the $\overline{RAS}$ high to low transition, the data (mask data) present on the DQ1-DQ4 inputs will be written into the MASK WRITE data register. The mask data acts as an individual write enable for each of the four DQ1-DQ4 pins. If a low(logic 0) is written to a mask data register bit the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A high (logic 1) on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still high. When $\overline{CAS}$ goes low, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit was high) or ignored (if the mask data bit was low). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. For NON-PERSISTENT MASKED WRITE cycles the mask data register is reset (to all ones) at the end of the cycle and new mask data must be supplied for each NON-PERSISTENT MASKED WRITE cycle, even if the same mask data is being used repeatedly. An example of NON-PERSISTENT MASKED WRITE cycle is shown in Figure 2.



X = NOT EFFECTIVE (DON'T CARE)

Figure 3
PERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the MASK data before each MASK WRITE cycle if the same MASK data is being used repeatedly. The internal MASK WRITE DATA REGISTER is loaded when $\overline{RAS}$ goes low by holding $\overline{ME}$/($\overline{WE}$) high and DSF high (see LOAD MASK REGISTER).

PERSISTENT MASKED WRITE cycles can then be performed by simply taking $\overline{ME}$/($\overline{WE}$) low and DSF high when $\overline{RAS}$ goes low. The contents of the PERSISTENT MASK DATA REGISTER will then be used as the mask data for the DRAM inputs. Unlike the NON-PERSISTENT MASKED WRITE cycle, the contents of the MASK WRITE DATA REGISTER are not reset at the end of a PERSISTENT MASKED WRITE cycle. Another PERSISTENT MASKED WRITE cycle can be performed without having to reload the MASK DATA register. Figure 3 shows the LOAD WRITE MASK REGISTER and PERSISTENT MASKED WRITE cycle operation.

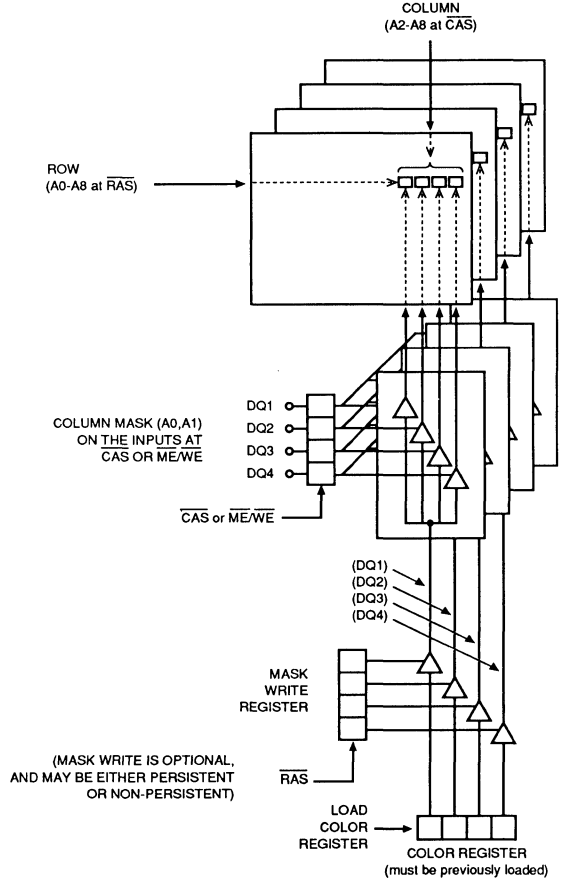


Figure 4
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is low when $\overline{CAS}$ goes low the MT42C4256 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the Color Register are directly written to four adjacent column locations (see Figure 4). The Color Register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The ROW is addressed as in a normal DRAM WRITE cycle, however when $\overline{CAS}$ goes low only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs are then used to determine what combination of the four column locations will be changed. DQ1 acts as a write enable for column location A0=0, A1=0; DQ2 controls column location A0=1, A1=0; DQ3 controls A0=0, A1=1, and DQ4 controls A0=1, A1=1. The write enable controls are active high, a logic 1 enables and a logic 0 disables the WRITE function.

The contents of the Color Register will then be written to the column locations enabled. Each DQ location of the Color Register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

NON-PERSISTENT MASKED BLOCK WRITE

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NON-PERSISTENT MASKED BLOCK WRITE operates exactly like the normal NON-PERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NON-PERSISTENT MASKED WRITE, the combination of $\overline{ME}/(\overline{WE})$ low and DSF low when $\overline{CAS}$ goes low initiates the NON-PERSISTENT MASKED BLOCK WRITE. By using both the Column Mask input and the MASKED WRITE function, any combination of the four bit planes can be masked and any combination fo the four column locations can be masked.

PERSISTENT MASKED BLOCK WRITE

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF is high when $\overline{CAS}$ goes low to indicate the BLOCK WRITE function. Both the Mask Register and the Color Register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

LOAD MASK REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is high when $\overline{RAS}$ goes low. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF being high when $\overline{RAS}$ goes low indicates the cycle is a register load cycle. DSF is used when $\overline{CAS}$ goes low to select the register to be loaded and must be low for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the MASK REGISTER.

Note: For a normal DRAM WRITE cycle the WRITE MASK REGISTER is disabled but not modified. The contents of WRITE MASK REGISTER will not be changed unless a NON-PERSISTENT MASK WRITE cycle or a LOAD MASK REGISTER cycle is performed

The ROW address supplied will be refreshed, but it is not necessary to provide any particular ROW address. The COLUMN address inputs are ignored during a LOAD MASK REGISTER cycle.

The MASK REGISTER contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the four DQ planes.

LOAD COLOR REGISTER

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is high when $\overline{CAS}$ goes low. The contents of the COLOR REGISTER are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is low when $\overline{RAS}$ goes low. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes low indicates the direction of the TRANSFER, and DSF is used to select between NORMAL TRANSFER cycles and SPLIT TRANSFER cycles. Each of the TRANSFER cycles available are described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If $(\overline{ME})/\overline{WE}$ is high and DSF is low when $\overline{RAS}$ goes low a READ TRANSFER cycle is selected. The row address bits indicate the four 512 bit DRAM rows that are to be tranferred to the four SAM data registers and the column address bits indicate the start address (or Tap point) of the next serial output cycle from the SAM data registers. To complete the TRANSFER, $\overline{TR}/(\overline{OE})$ is taken high while $\overline{RAS}$ and $\overline{CAS}$ are still low. The rising edge of $\overline{TR}/(\overline{OE})$ must occur between the rising edges of successive clocks on the SC input (refer to the AC Timing Diagrams). The 2048 bits of DRAM data are then written into the SAM data registers and the serial shift start address is stored in an internal 9 bit register. If $\overline{SE}$ is low, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either high or low during this operation. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

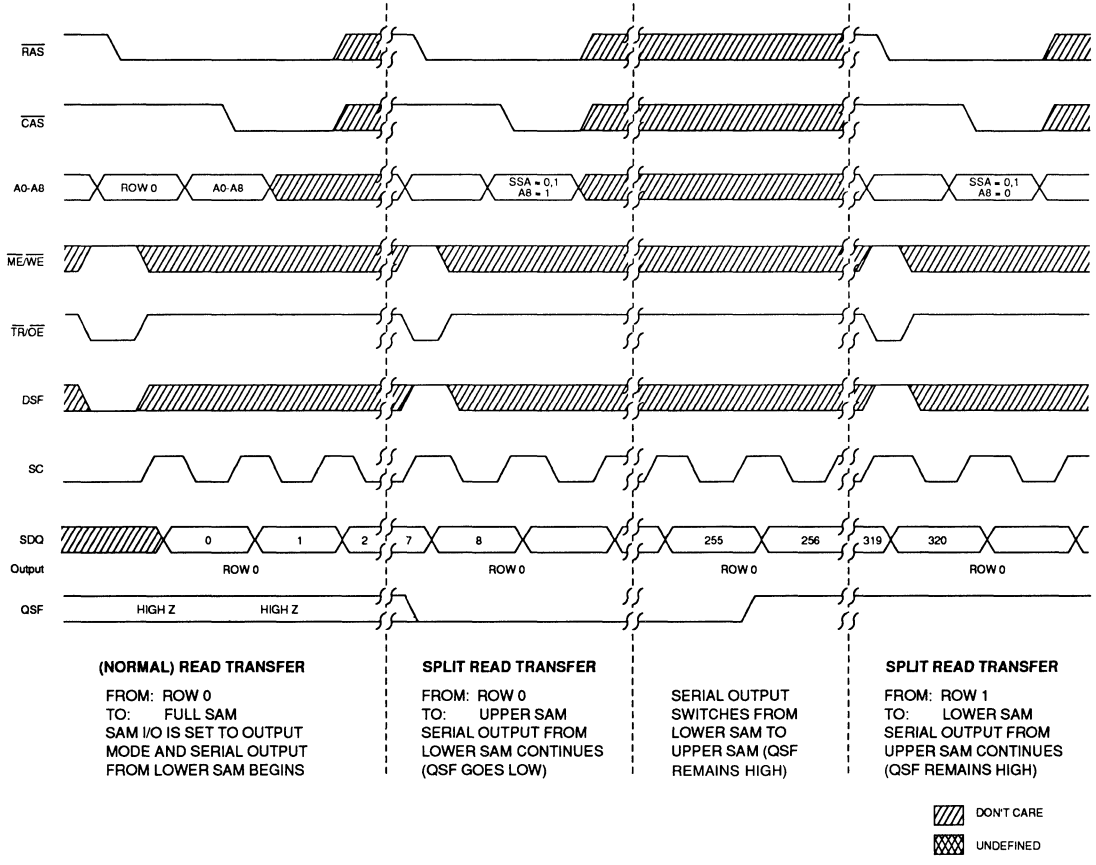


Figure 5
TYPICAL SPLIT READ TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the READ TRANSFER cycle had to occur immediately after the last bit of "old data" was clocked out the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data can be transferred to the other half. The transfer can occur at any time while the other half is sending data and need not be synchronized with the SC clock.

SPLIT TRANSFERS do not change the SAM I/O direction. A normal, or non-split, READ TRANSFER cycle must precede any sequence of SPLIT READ TRANSFER cycles in order to put the SAM I/O in the output mode and provide a SAM access (which half) reference. Then SPLIT READ TRANSFERS can be initiated by taking DSF high when $\overline{RAS}$ goes low during the transfer cycle. As in non-split transfers, the row address is used to specify the DRAM row to be transferred. The most significant column address, A8, is used to select which SAM half accepts the transfer (1=upper half, 0=lower half). The remainder of the column address bits determine the starting address (Tap) for the SAM half selected by A8.

Figure 5 shows a typical SPLIT READ TRANSFER initiation sequence. The normal READ TRANSFER is first performed, followed by a SPLIT READ TRANSFER of the same row to the upper half of the SAM. The purpose of the SPLIT TRANSFER of the same data is to initiate the split SAM operating mode and enable the QSF output. Serial access continues, and when the SAM address counter reaches 256 (A8=1, A0-A7=0) the QSF output goes high. Since the serial access has now switched to the upper SAM, new data can now be transferred to the lower SAM. This sequence of waiting for the state of QSF to change and then transferring new data to the SAM half that is not being accessed can now be repreated. For example, the next step in Figure 5 would be to wait until QSF went low (indicating that Row 1 data is shifting out the lower SAM) and then transferring the upper half of Row 1 to the upper SAM.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER function is identical to the READ TRANSFER FUNCTION described previously except ($\overline{ME}$)/$\overline{WE}$ and $\overline{SE}$ must be low when $\overline{RAS}$ goes low. The row address indicates the DRAM row that the SAM data registers will be written to and the column address (SSA or Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. Performing a WRITE TRANSFER sets the direction of the SAM I/O buffers to the input mode.

PSEUDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle can be used to change the direction of SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with $\overline{SE}$ held high instead of low. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

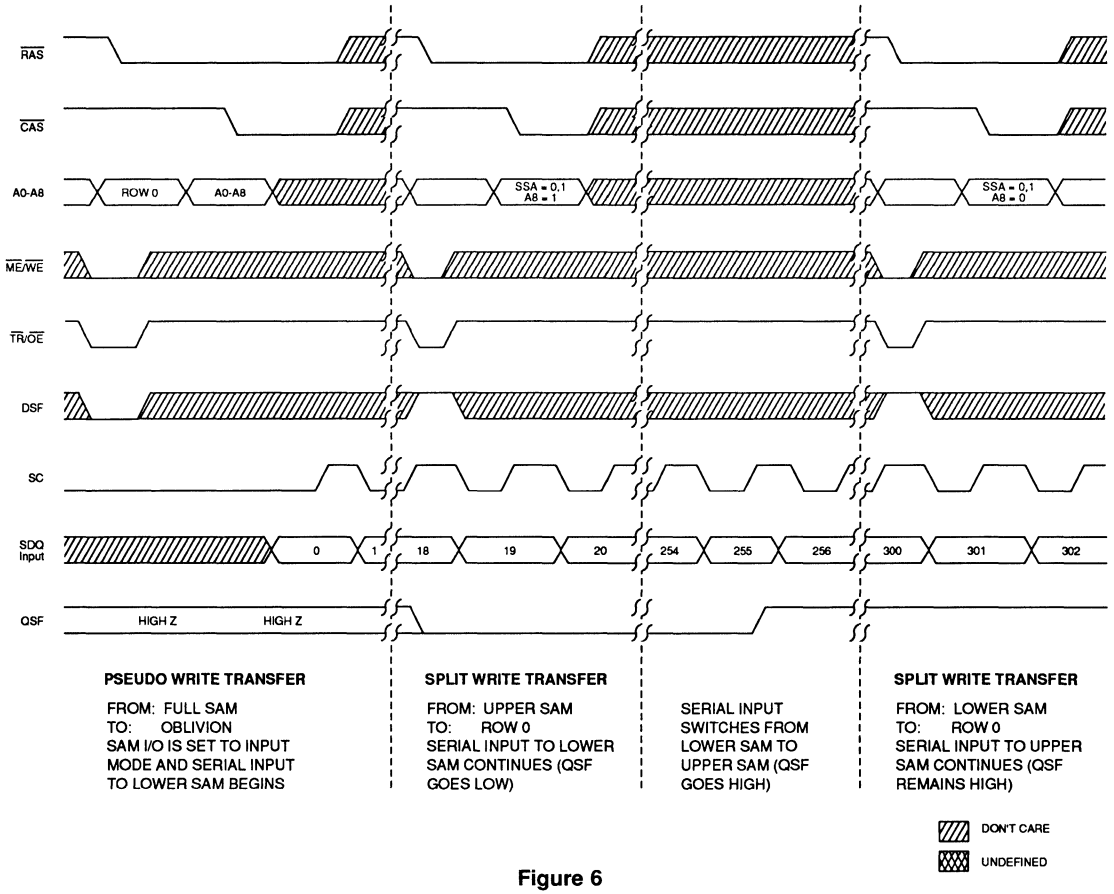


Figure 6
TYPICAL SPLIT WRITE TRANSFER INITIATION SEQUENCE

SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER)

The SPLIT WRITE TRANSFER feature makes it possible to input and transfer uninterrupted bit streams. Figure 6 shows a typical initiation sequence for SPLIT WRITE TRANSFER input cycles.

Like the SPLIT READ TRANSFER, the SPLIT WRITE TRANSFER cycle does not change the state of the SAM I/O buffers. Performing a normal WRITE TRANSFER cycle or PSUEDO WRITE TRANSFER cycle is required to set the Tap point and set the SAM I/O buffers to input mode.

The next step is to perform a SPLIT WRITE TRANSFER to enter the SPLIT SAM operating mode and enable the QSF output. Usually, the upper SAM is immediately transferred to the first destination row. The upper SAM may not yet contain valid data, but another write to the same row would normally occur after the next SPLIT WRITE TRANSFER cycle.

Once in the SPLIT TRANSFER operating mode, the QSF output will indicate which half of the SAM is currently accepting data. After QSF goes high, indicating that serial input has now switched to the upper SAM, the contents of the lower SAM may be transferred to any DRAM row. The cycle of checking for a change in QSF and then transferring the SAM half just filled can now be repeated. The next step on Figure 6 would be to wait for QSF to go low and then SPLIT WRITE TRANSFER the contents of the Upper SAM to row 0.

FUNCTIONAL TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE					CAS FALL	A0 - A8[1]		DQ1 - DQ4[2]		REGISTERS	
		CAS	TR / OE	ME / WE	DSF	SE	DSF	RAS	CAS	RAS	CAS[3]	MASK	COLOR
	DRAM OPERATIONS												
CBR	CAS-BEFORE-RAS REFRESH	0	X	1	X	X	X	—	X	—	X	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	X	0	ROW	COLUMN	X	VALID DATA	X	X
RWNM	NON-PERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	X	0	ROW	COLUMN	X	VALID DATA	USE	X
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	X	1	ROW	COLUMN (A2 - A8)	X	COLUMN MASK	X	USE
BWNM	NON-PERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	X	1	ROW	COLUMN (A2 - A8)	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER)	1	1	0	1	X	1	ROW	COLUMN	X	COLUMN	USE	USE
	REGISTER OPERATIONS												
LMR	LOAD MASK REGISTER	1	1	1	1	X	0	ROW[4]	X	X	WRITE MASK	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	X	1	ROW[4]	X	X	COLOR DATA	X	LOAD
	TRANSFER OPERATIONS												
RT	DRAM-TO-SAM TRANSFER (READ TRANSFER)	1	0	1	0	X	X	ROW	SSA[5] (TAP)	X	X	X	X
SRT	SPLIT DRAM-TO-SAM TRANSFER (SPLIT READ TRANSFER)	1	0	1	1	X	X	ROW	SSA[5] (TAP)	X	X	X	X
WT	SAM-TO-DRAM TRANSFER (WRITE TRANSFER)	1	0	0	0	0	X	ROW	SSA[5] (TAP)	X	X	X	X
PWT	SERIAL INPUT MODE ENABLE (PSEUDO WRITE TRANSFER)	1	0	0	0	1	X	ROW[4]	SSA[5] (TAP)	X	X	X	X
SWT	SPLIT SAM-TO-DRAM TRANSFER WITH MASK (SPLIT WRITE TRANSFER)	1	0	0	1	X	X	ROW	SSA[5] (TAP)	WRITE MASK	X	LOAD & USE	X

NOTES:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ4 inputs when RAS falls and when CAS falls.
3. On WRITE cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. similarly, on READ cycles, the output data is latched at the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
5. SSA = SAM Starting Address or Tap Point. This is the first SAM location that the next SC cycle will access.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Operating Temperature, Ta(Ambient) .....0°C to +70°C
Storage Temperature (Ceramic) .....-65°C to +150°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation .....1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(Notes 3, 4, 5) ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$, all other pins not under test = 0 volts).	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Dout is disabled, $0V \le V_{OUT} \le V_{CC}$).	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8), D_{IN}	C_{I1}		5	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SC, $\overline{SE}$, DSF	C_{I2}		7	pF	2
Output Capacitance D_{OUT}, QSF	C_O		7	pF	2

CURRENT DRAIN, SAM IN STANDBY

(Notes 2, 3) ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION OF DRAM	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$=Cycling; $T_{RC}=T_{RC(MIN)}$).	I_{CC1}		90	mA	3, 4
OPERATING CURRENT: PAGE-MODE ($\overline{RAS}=V_{IL}$,$\overline{CAS}$=Cycling; $T_{PC}=T_{PC(MIN)}$).	I_{CC2}		70	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}=\overline{CAS}=V_{IH}$ after 8 $\overline{RAS}$ cycles min).	I_{CC3}		3	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}=\overline{CAS}=V_{CC}$-0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V).	I_{CC4}		1	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}=V_{IH}$).	I_{CC5}		90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling).	I_{CC6}		80	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC7}		90	mA	3, 4

CURRENT DRAIN, SAM ACTIVE (tsc = MIN)

(Notes 2, 3) ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION OF DRAM	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$=Cycling; $T_{RC}=T_{RC(MIN)}$).	I_{CC8}		115	mA	3, 4
OPERATING CURRENT: PAGE-MODE ($\overline{RAS}=V_{IL}$,$\overline{CAS}$=Cycling; $T_{PC}=T_{PC(MIN)}$).	I_{CC9}		95	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}=\overline{CAS}=V_{IH}$ after 8 $\overline{RAS}$ cycles min).	I_{CC10}		30	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}=\overline{CAS}=V_{CC}$-0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V).	I_{CC11}		25	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}=V_{IH}$).	I_{CC12}		115	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling).	I_{CC13}		105	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC14}		115	mA	3,4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	160		190		220		260		ns	
READ-MODIFY-WRITE cycle time	^tRWC	190		220		255		295		ns	
PAGE-MODE READ or WRITE cycle time	^tPC	45		55		70		85		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30		45	ns	15
Access time from ($\overline{TR}$)/OE	^tOE		20		25		25		30	ns	
Access time from column address	^tAA		40		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		50		65		75	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	150	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		30		45		ns	
$\overline{RAS}$ precharge time	^tRP	70		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	10		15		20		25		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	10		10		15		20		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	60	10	75	15	90	15	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		10		10		10		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	10		10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	10	40	10	50	15	60	15	70	ns	18
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		60		70		80		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		70		ns	
Read command set-up time	^tRCS	0		0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	5		5		5		5		ns	
Output buffer turn-off delay	^tOFF	0	20	0	25	0	25	0	30	ns	20
Output Disable	^tOD		20		25		25		30	ns	

DRAM TIMING PARAMETERS (Continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command set-up time	^tWCS	0		0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		30		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		70		80		90		ns	
Write command pulse width	^tWP	15		20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		70		80		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	100		120		150		185		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	60		80		100		120		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		65		75		85		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ set-up time	^tWSR	0		0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	10		10		10		15		ns	
Mask Data to $\overline{RAS}$ set-up time	^tMS	0		0		0		0		ns	
Mask Data to $\overline{RAS}$ hold time	^tMH	10		15		15		20		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ4) is high impedance.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ4) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (min), $^tAWD \geq {}^tAWD$ (min) and $^tCWD \geq {}^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}/\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH D_{OUT} goes open.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}/\overline{WE}$ = LOW and $\overline{TR}/\overline{OE}$=HIGH.
25. SAM output timing is measured with a load equivalent to 2TTL gate and 50pF.
26. TRANSFER command mean that $\overline{TR}/\overline{OE}$ is low when RAS goes low.
27. NON-TRANSFER command means that $\overline{TR}/\overline{OE}$ is high when $\overline{RAS}$ goes low.

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 17, 25) (0° C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
TRANSFER Command to $\overline{RAS}$ Set Up Time	^tTLS	0		0		0		0		ns	26
Transfer Command to $\overline{RAS}$ Hold Time	^tTLH	10	10,000	10	10,000	10	10,000	15	10,000	ns	
TRANSFER Command to $\overline{RAS}$ Hold Time (REAL-TIME READ TRANSFER only)	^tRTH	70	10,000	80	10,000	90	10,000	100	10,000	ns	26
TRANSFER Command to $\overline{CAS}$ Hold Time (REAL-TIME READ TRANSFER only)	^tCTH	20		25		30		35		ns	26
TRANFER Command to Column Address Hold Time (For REAL TIME READ TRANSFER only)	^tATH	25		30		35		40		ns	
TRANSFER Command to SC Lead Time	^tTSL	5		5		5		10		ns	26
TRANSFER Command to $\overline{RAS}$ Lead Time	^tTRL	10		10		10		10		ns	26
TRANSFER Command to $\overline{RAS}$ Delay Time	^tTRD	15		15		15		20		ns	26
TRANSFER Command to $\overline{CAS}$ Time	^tTCL	10		10		10		10		ns	26
TRANSFER Command to $\overline{CAS}$ Delay Time	^tTCD	15		15		15		20		ns	26
First SC edge to TRANSFER Command Delay Time	^tTSD	10		10		10		20		ns	26
Serial Output Buffer Turn Off Delay from $\overline{RAS}$	^tSDZ	10	35	10	40	10	50	10	60	ns	
SC to $\overline{RAS}$ Set Up Time	^tSRS	30		35		40		45		ns	
$\overline{RAS}$ to SC Delay Time	^tSRD	20		25		30		35		ns	
Serial Data Input to $\overline{SE}$ Delay Time	^tSZE	0		0		0		0		ns	
$\overline{RAS}$ to SD Buffer Turn On Time	^tSRO	0		0		0		0		ns	
Serial Data Input Delay from $\overline{RAS}$	^tSDD	45		50		55		60		ns	
Serial Data Input to $\overline{RAS}$ Delay Time	^tSZS	0		0		0		0		ns	
Serial Input Mode Enable ($\overline{SE}$) to $\overline{RAS}$ Set Up Time	^tESR	0		0		0		0		ns	
Serial Input Mode Enable ($\overline{SE}$) to $\overline{RAS}$ Hold Time	^tREH	10		10		10		15		ns	
NON-TRANSFER Command to $\overline{RAS}$ Set Up Time	^tYS	0		0		0		0		ns	27
NON-TRANSFER Command to $\overline{RAS}$ Hold Time	^tYH	10		10		10		10		ns	27
DSF to $\overline{RAS}$ Set Up Time	^tFSR	0		0		0		0		ns	
DSF to $\overline{RAS}$ Hold Time	^tRFH	10		15		15		20		ns	
DSF to $\overline{RAS}$ Hold Time	^tFHR	60		65		70		75		ns	
DSF to $\overline{CAS}$ Set-up Time	^tFSC	0		0		0		0		ns	
DSF to $\overline{CAS}$ Hold Time	^tCFH	15		20		20		25		ns	
SC to QSF Delay Time	^tSQD		25		30		35		40	ns	
SPLIT TRANSFER Set Up Time	^tSTS	30		35		40		45		ns	
SPLIT TRANSFER Hold Time	^tSTH	30		35		40		45		ns	
$\overline{TR/OE}$ to QSF Delay Time	^tTQD		25		30		35		40	ns	
$\overline{CAS}$ to QSF Delay Time	^tCQD		35		40		45		50	ns	

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

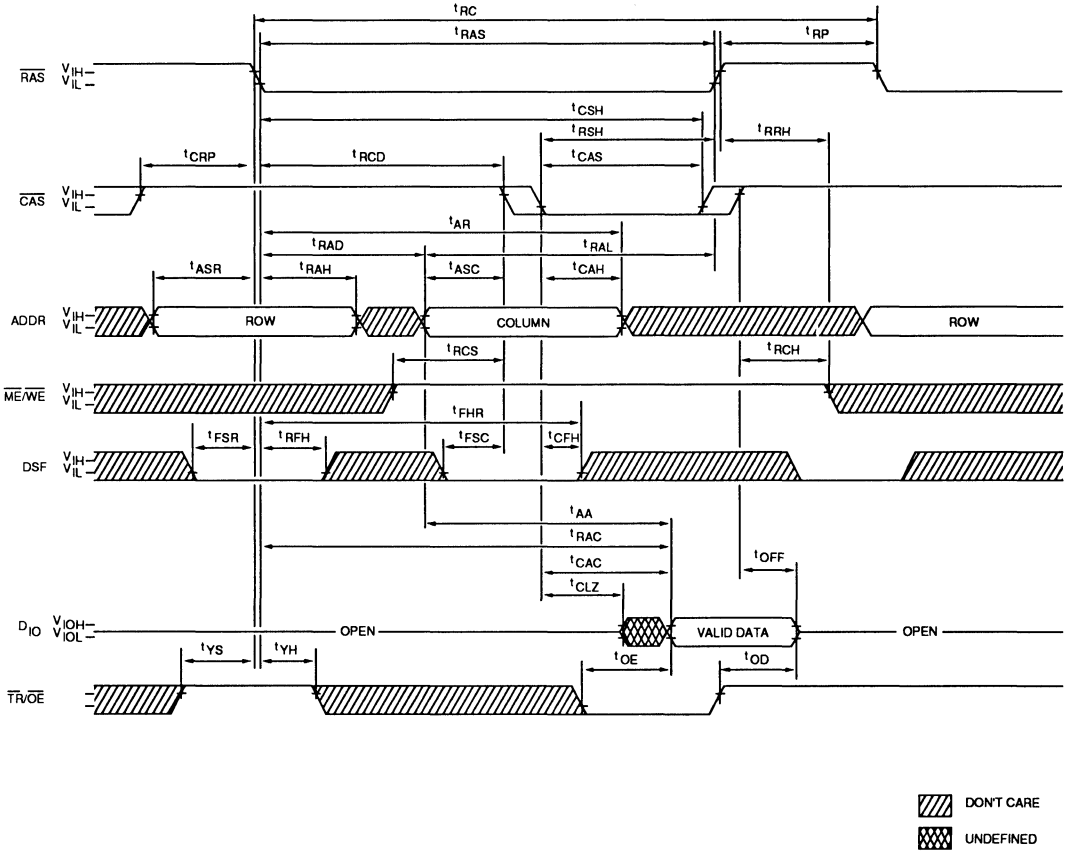
(Notes 3, 4, 5, 17, 25) (0° C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial Clock Cycle Time	^tSC	25		30		35		40		ns	
Access Time from SC	^tSAC		25		30		35		40	ns	
SC Precharge Time (SC Low Time)	^tSP	10		10		12		15		ns	
SC Pulse Width (SC High Time)	^tSAS	10		10		12		15		ns	
Access Time from $\overline{SE}$	^tSEA		20		25		30		40	ns	
$\overline{SE}$ Precharge Time	^tSEP	15		15		15		20		ns	
$\overline{SE}$ Pulse Width	^tSE	15		15		15		20		ns	
Serial Data Out Hold Time after SC High	^tSOH	5		10		10		10		ns	
Serial Output Buffer Turn Off Delay from SE	^tSEZ	0	15	0	15	0	25	0	30	ns	
Serial Data in Set Up Time	^tSDS	0		0		0		0		ns	
Serial Data in Hold Time	^tSDH	20		20		20		25			
SERIAL INPUT (Write) Enable Set Up Time	^tSWS	0		0		0		0		ns	
SERIAL INPUT (Write) Enable Hold Time	^tSWH	25		30		35		45		ns	
SERIAL INPUT (Write) Disable Set Up Time	^tSWIS	0		0		0		0		ns	
SERIAL INPUT (Write) Disable Hold Time	^tSWIH	25		30		35		45		ns	

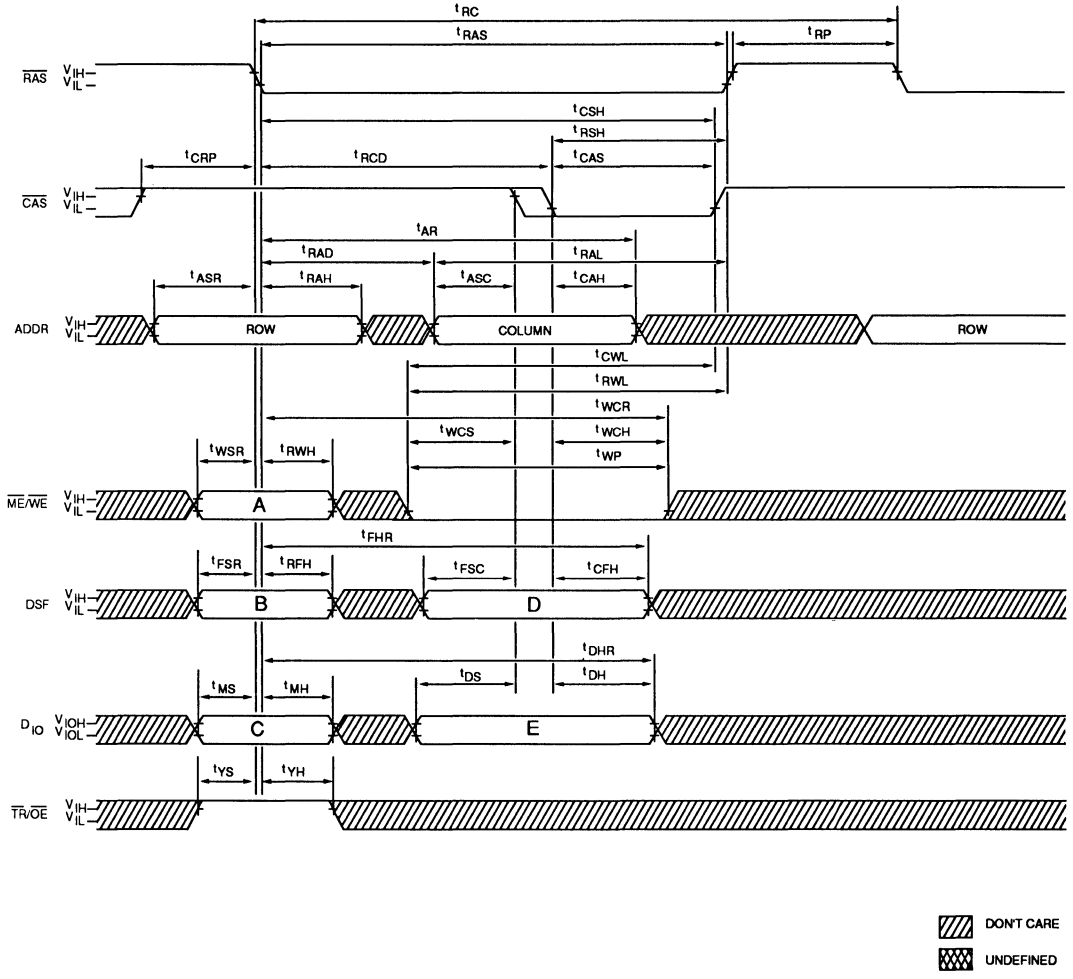
WRITE CYCLE FUNCTION TABLE

LOGIC STATES					FUNCTION
$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge		
A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DSF	E DQ (Input)	
1	0	X	0	DRAM Data	Normal DRAM WRITE (or READ)
0	0	Write Mask	0	DRAM Data (Masked)	Non-Persistent (Load and Use) Masked Write to DRAM
0	1	X	0	DRAM Data (Masked)	Persistent (Use Register) Masked Write to DRAM
1	0	X	1	Column Mask	Block Write to DRAM (No Data Mask)
0	0	Write Mask	1	Column Mask	Non-Persistent (Load and Use) Masked Block Write to DRAM
0	1	X	1	Column Mask	Persistent (Use Register) Masked Block Write to DRAM
1	1	X	0	Write Mask	Load Mask Register
1	1	X	1	Color Data	Load Color Register

DRAM READ CYCLE

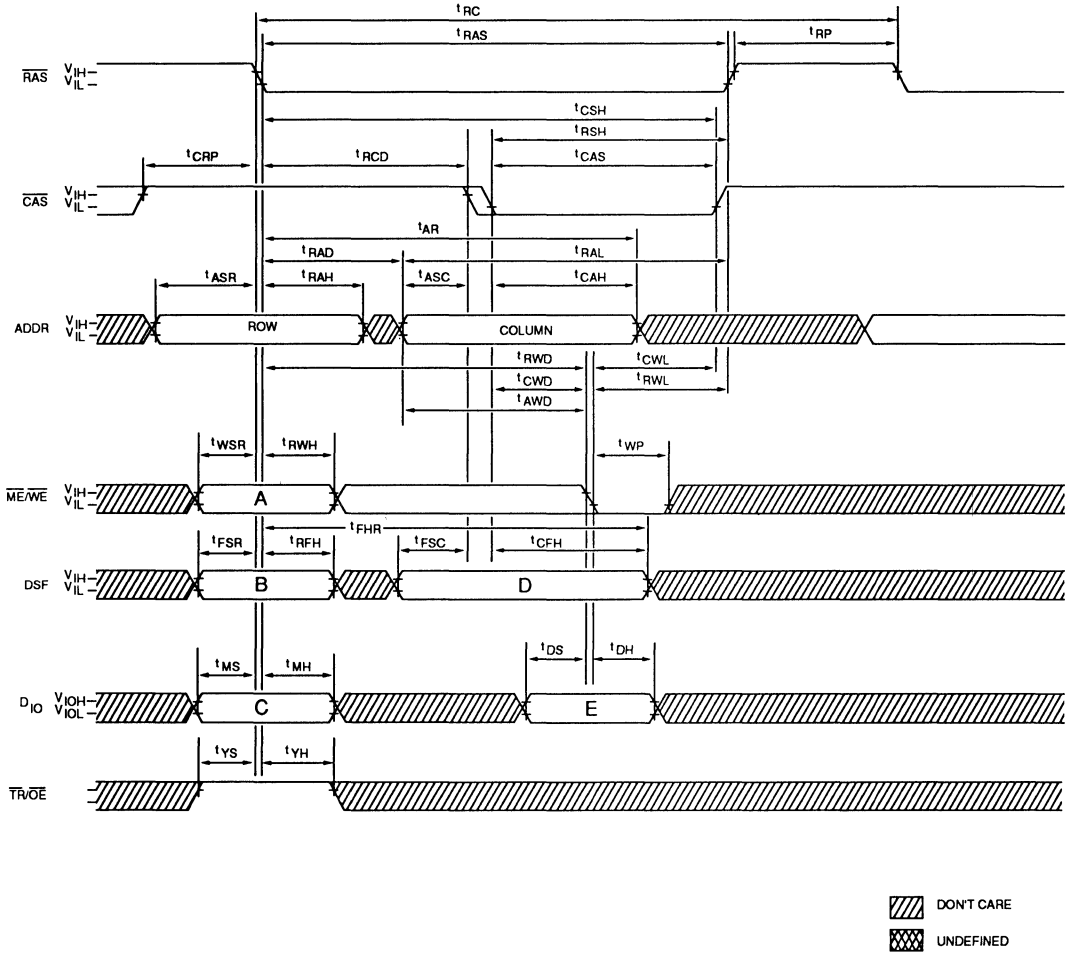


DRAM EARLY-WRITE CYCLE



NOTE: The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

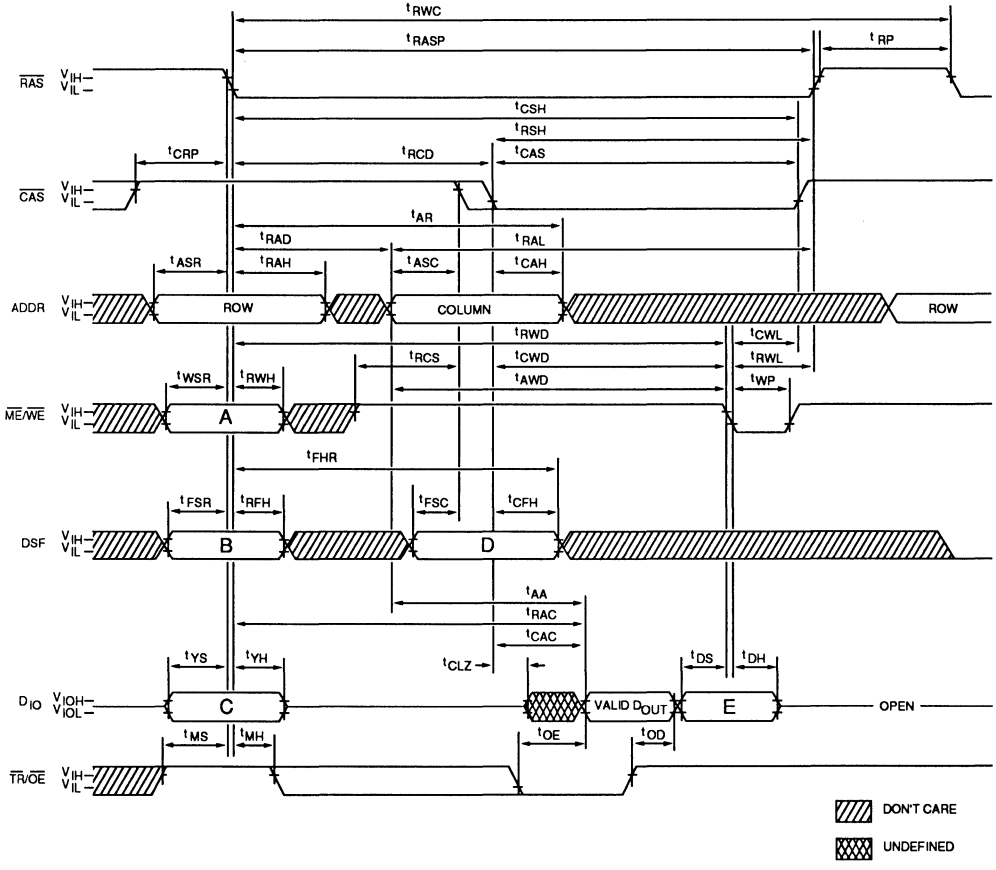
DRAM LATE-WRITE CYCLE



NOTE: The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

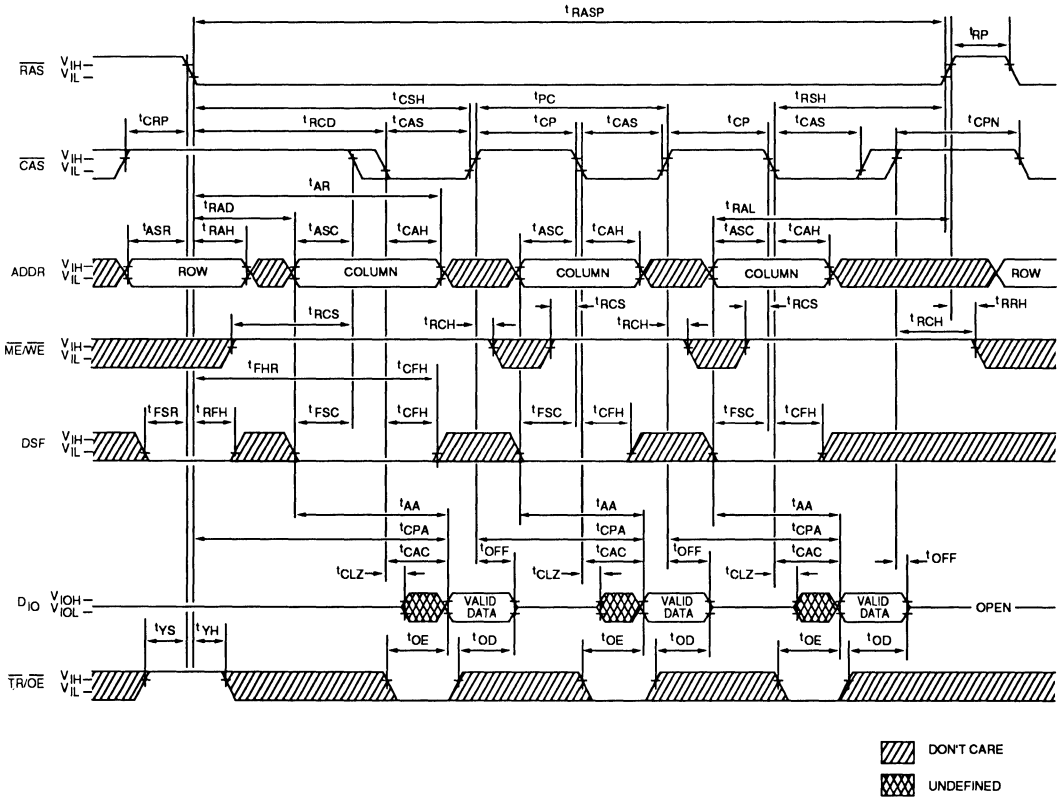
VRAM

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



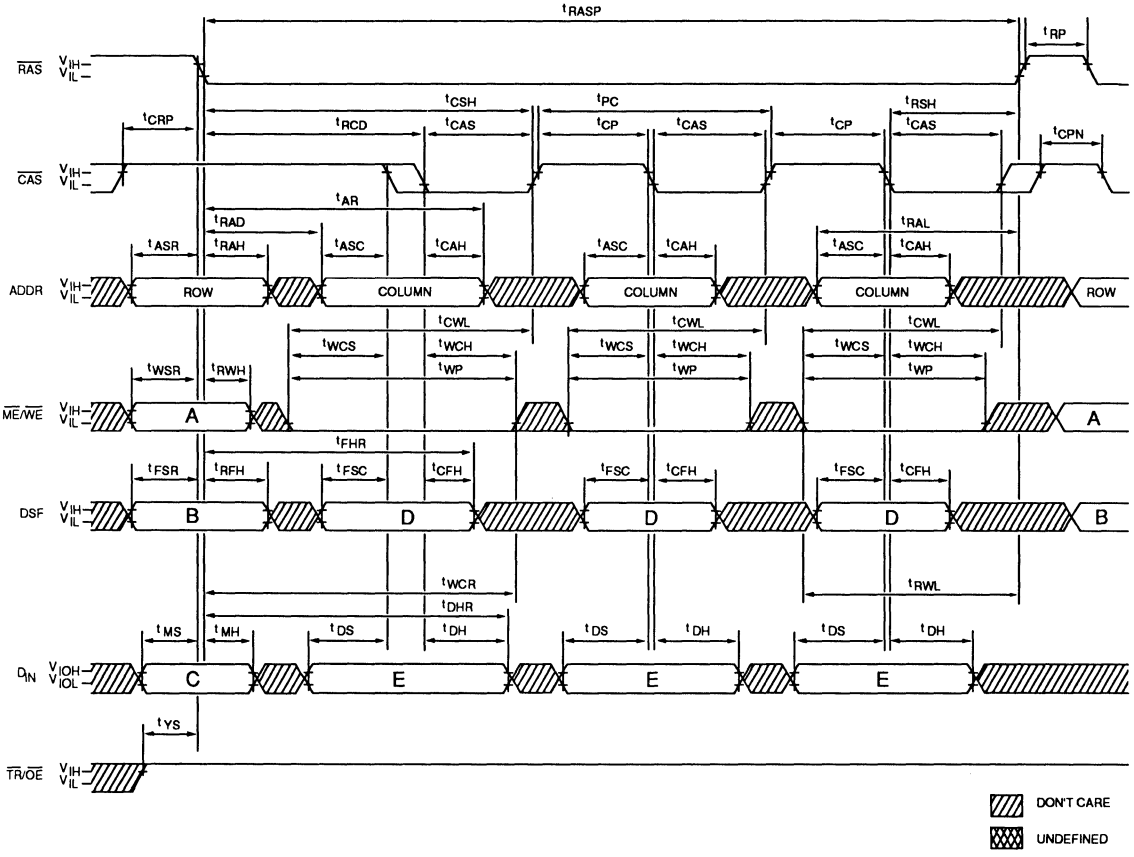
NOTE: The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM PAGE-MODE READ CYCLE



Note1: WRITE cycles or READ-MODIFY-WRITE cycles can be mixed with READ cycles while in PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.

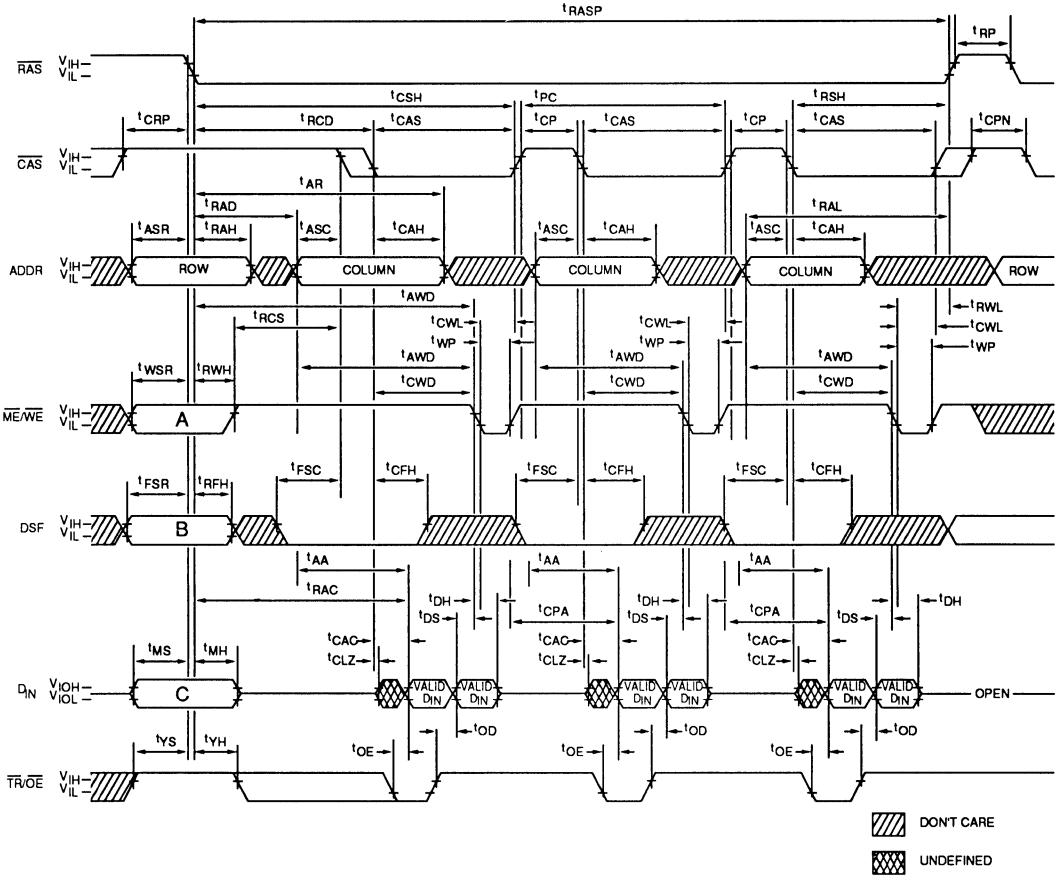
DRAM PAGE-MODE EARLY-WRITE CYCLE



Note1: READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in PAGE-MODE.

Note 2: The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

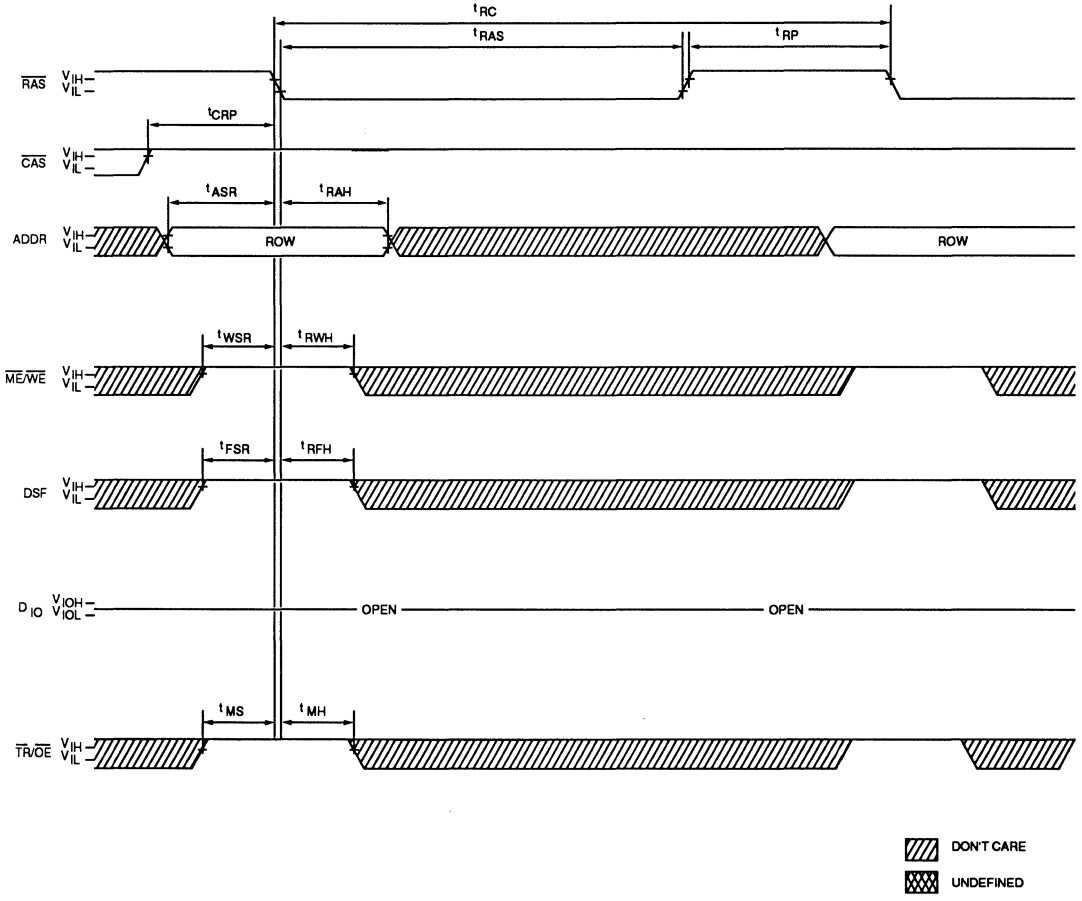
DRAM PAGE-MODE READ-WRITE CYCLE
(PAGE-MODE READ-MODIFY-WRITE CYCLE)



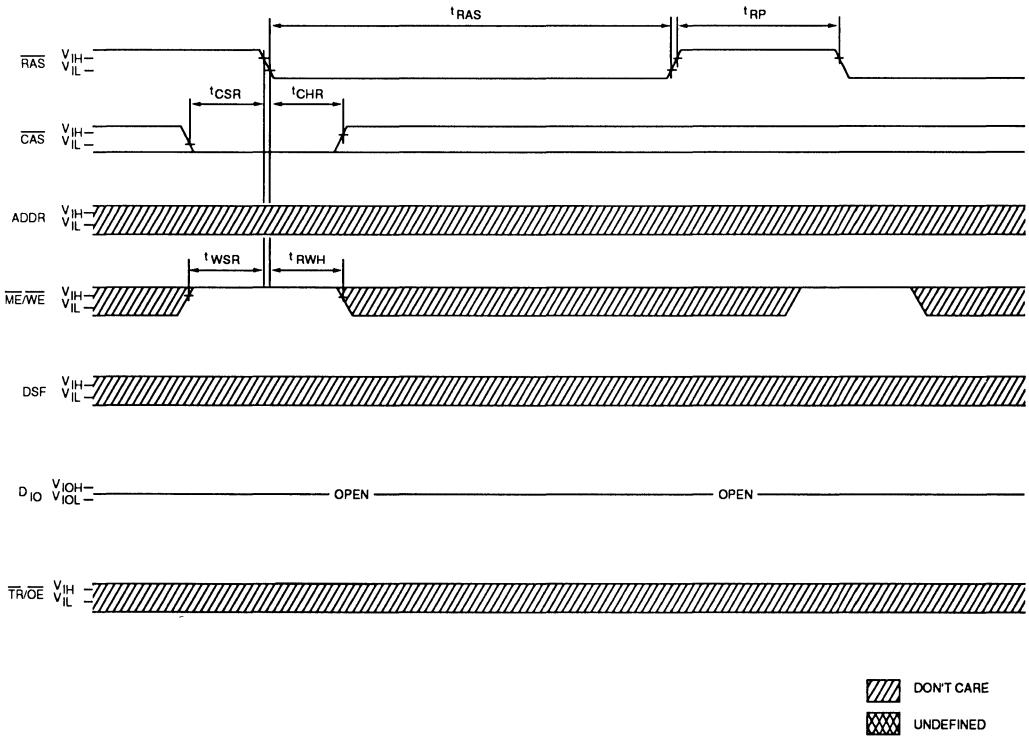
Note1: READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in PAGE- MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.

Note 2: The Logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

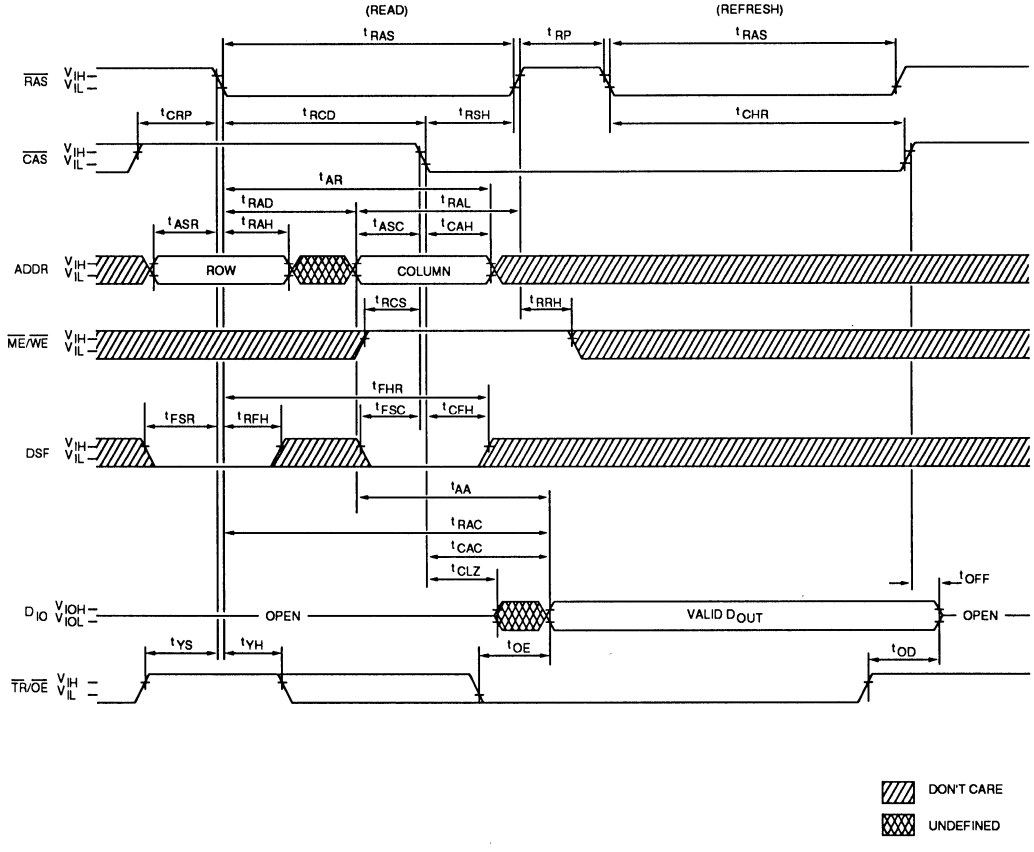
DRAM $\overline{RAS}$ ONLY REFRESH CYCLE



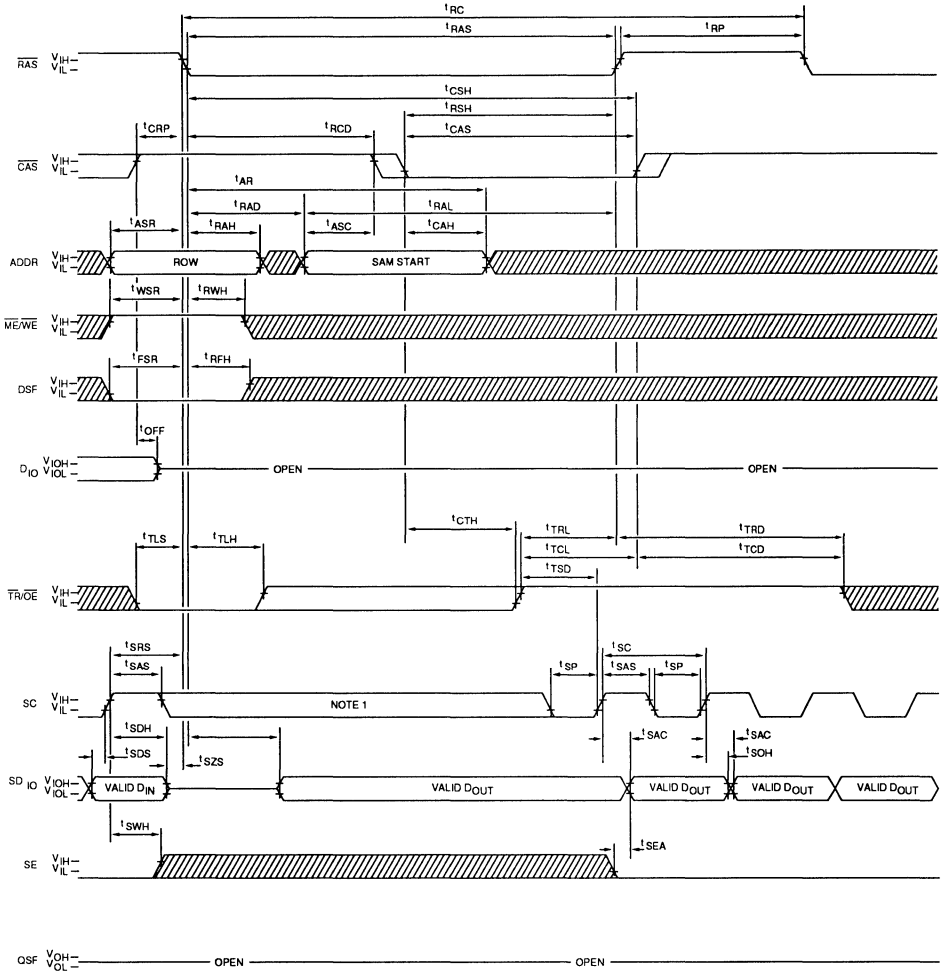
CAS-BEFORE-RAS REFRESH CYCLE



DRAM HIDDEN REFRESH CYCLE



READ TRANSFER
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode.)



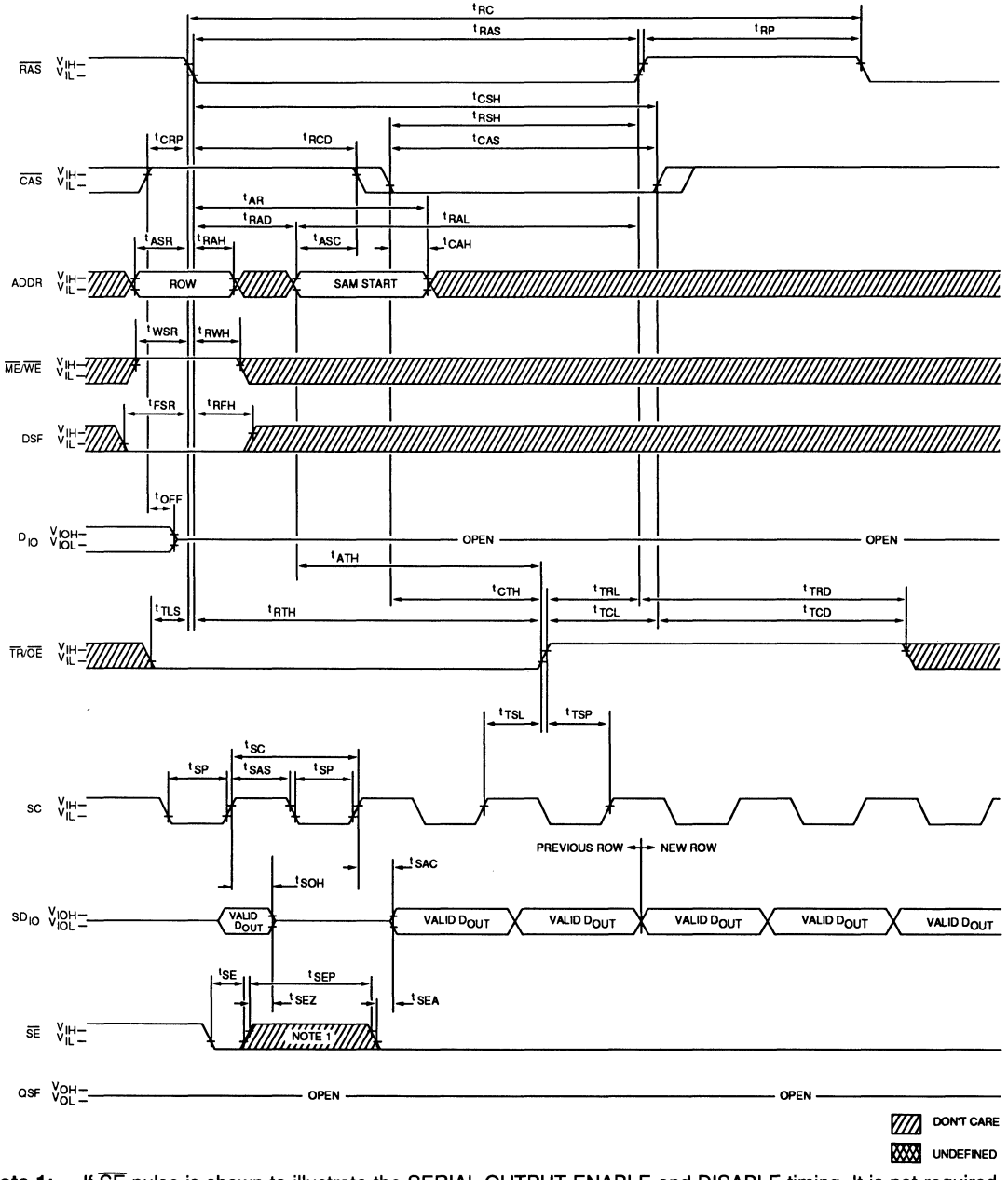
NOTE 1: There must be no rising edges on the SC input during this time period.

Note 1: There must be no rising edges on the SC input during this time period.

VRAM

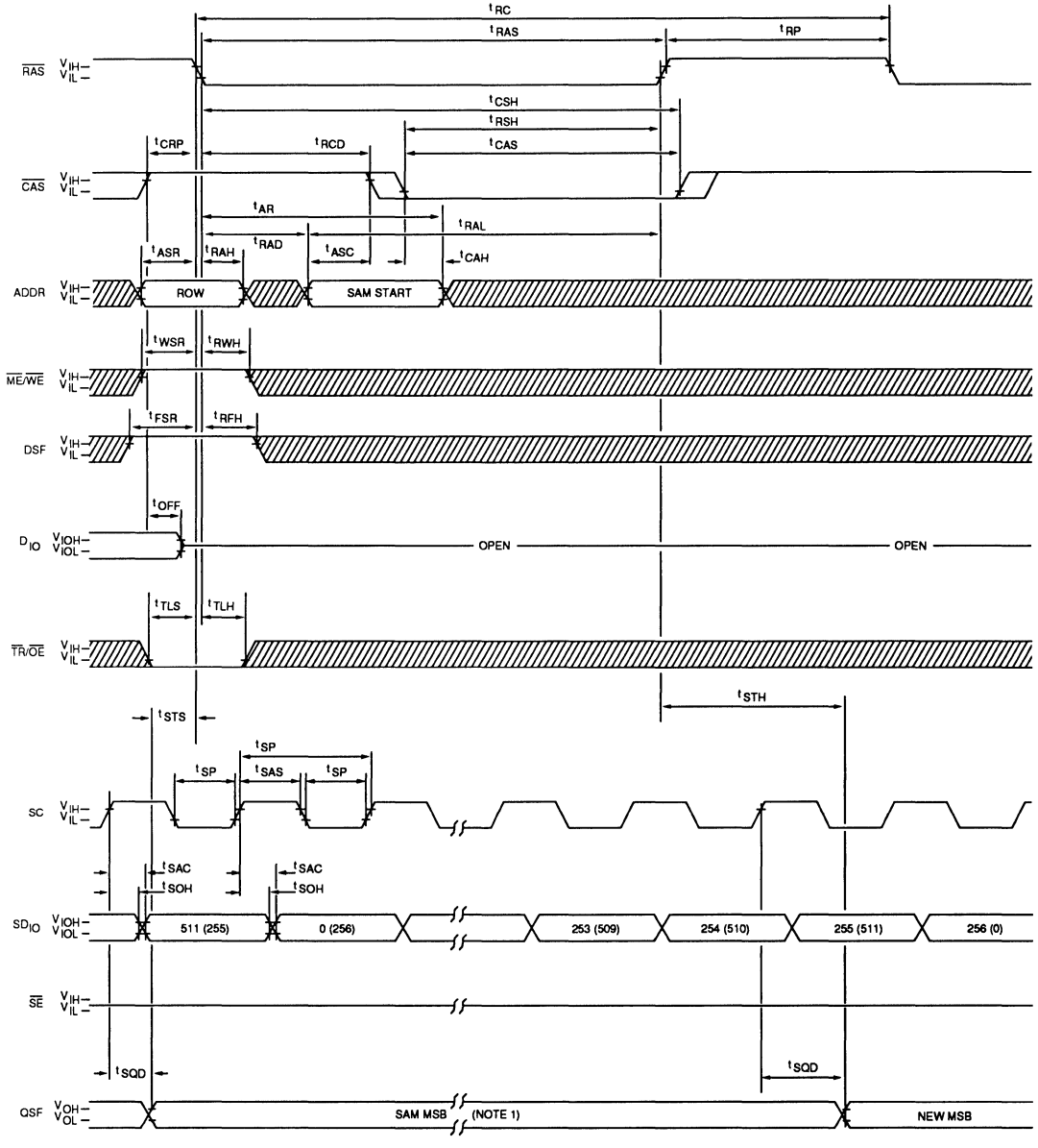
REAL-TIME READ TRANSFER
(DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode.)



Note 1: If $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

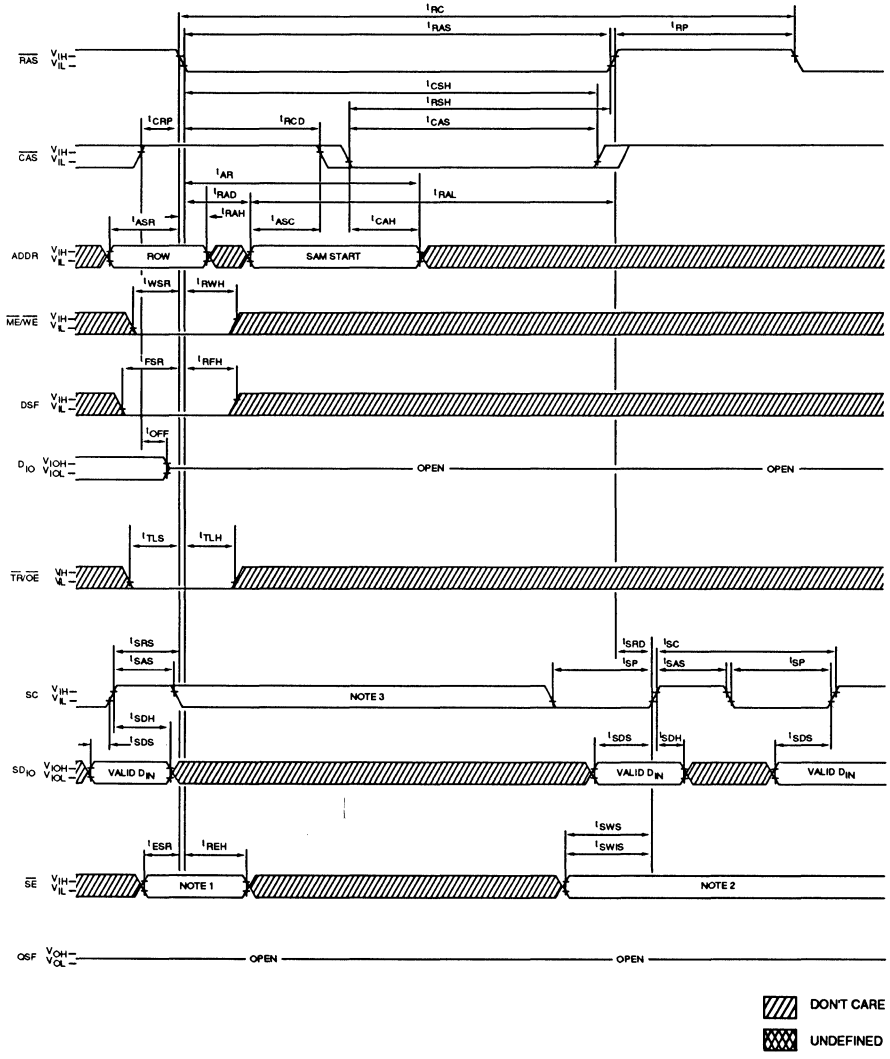
SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



Note 1: QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

VRAM

WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was perviously in the SERIAL INPUT mode.)



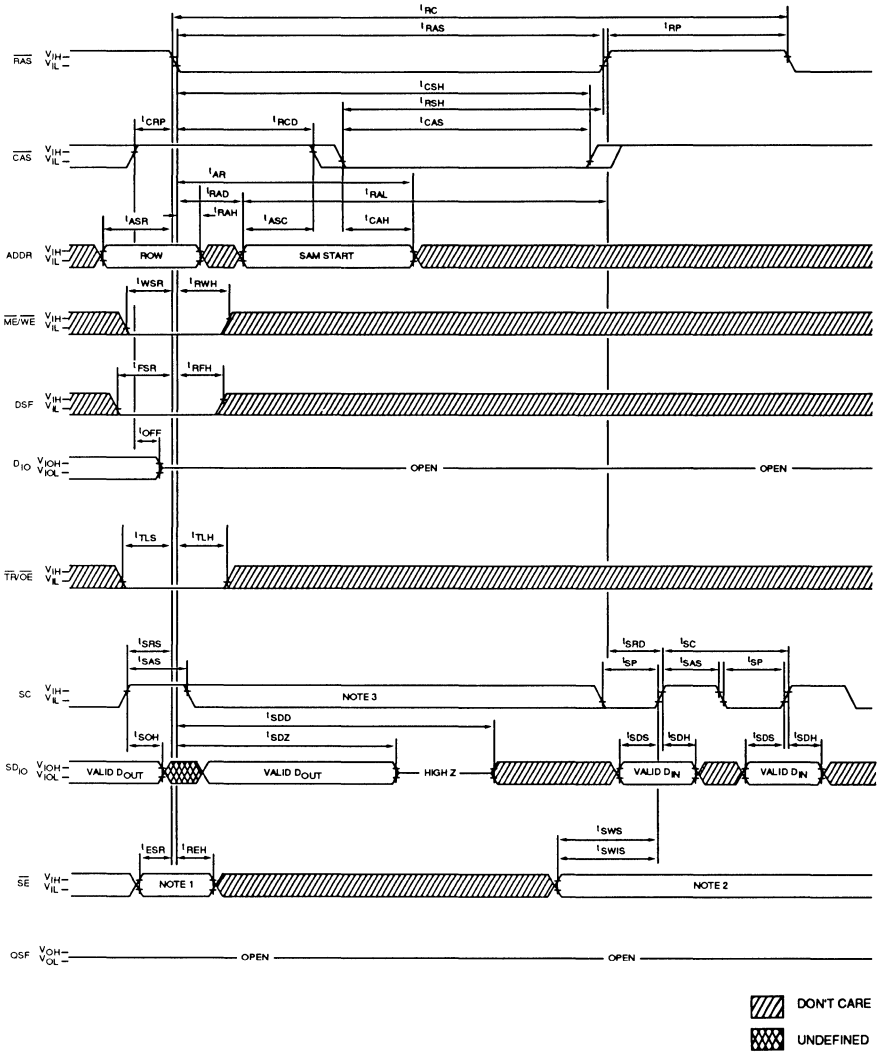
NOTE 1: If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

NOTE 3: There must be no rising edges on the SC input during this time period.

WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode.)



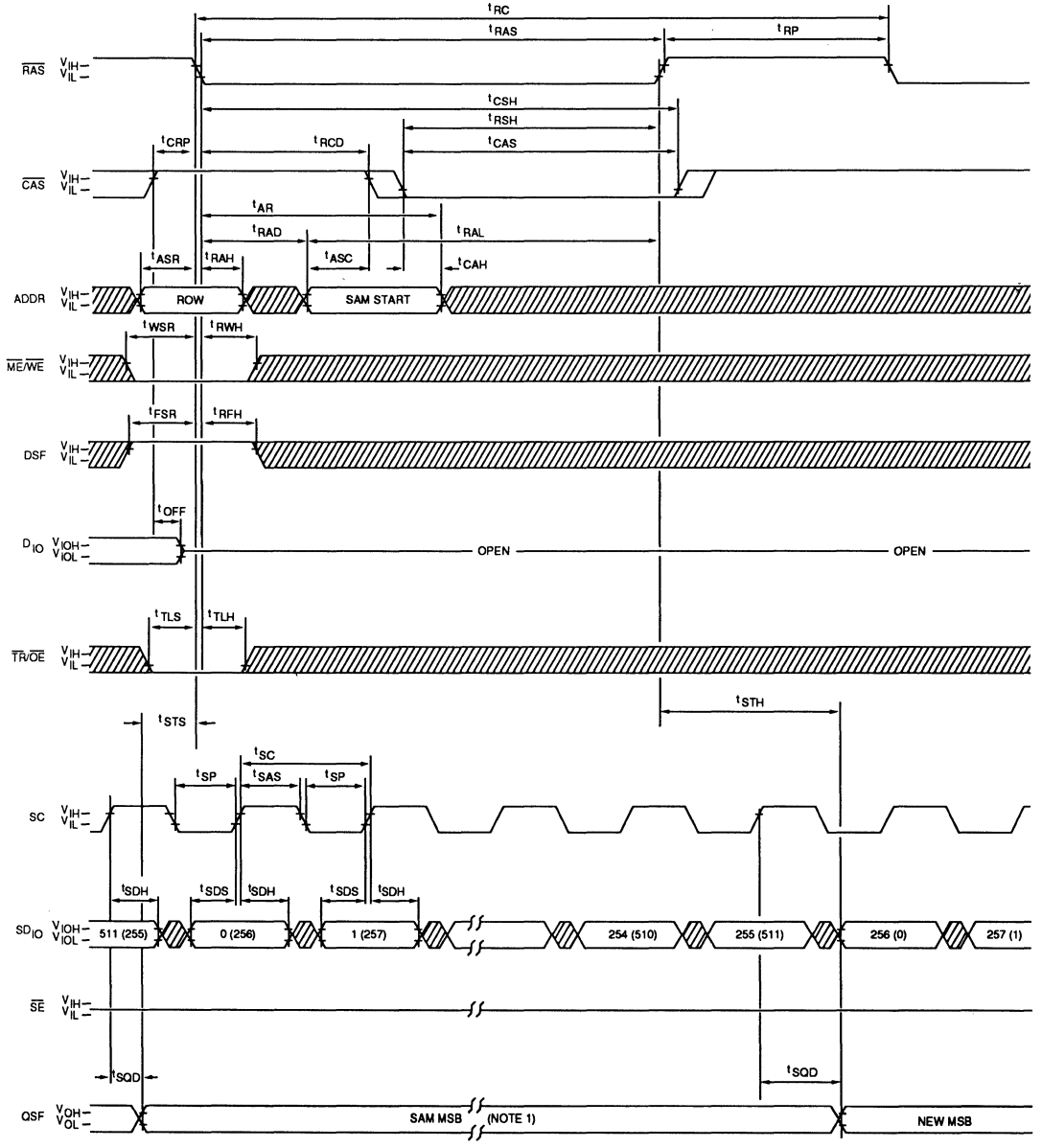
NOTE 1: If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

NOTE 3: There must be no rising edges on the SC input during this time period.

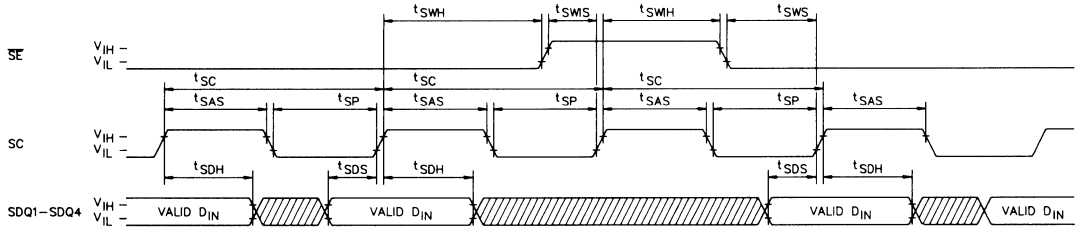
VRAM

SPLIT WRITE TRANSFER
(SPLIT SAM-TO-DRAM TRANSFER)

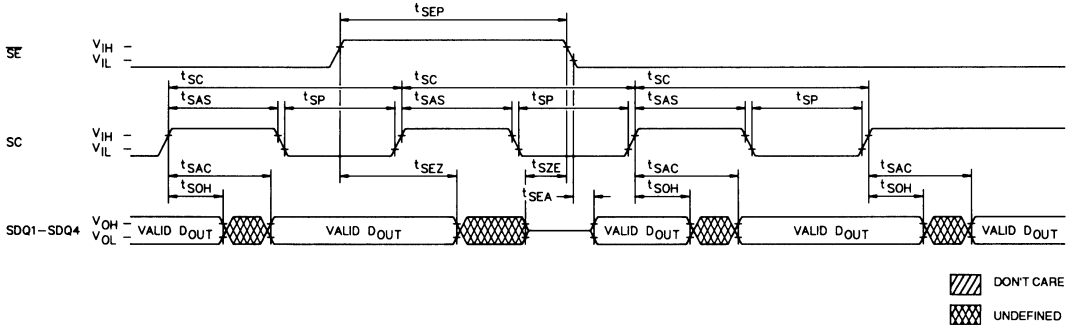


Note 1: QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

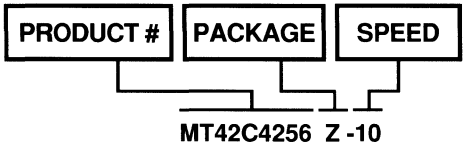
SAM SERIAL INPUT



SAM SERIAL OUTPUT



ORDER INFORMATION



The Micron MT42C4256 is functionally equivalent to other manufacturer's products meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the high speed, low power CMOS double poly, single metal process. Micron's QUALITY ASSURED policy is to offer prompt, accurate, and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply, temperature, and refresh range than specified. Each unit receives accelerated burn-in and and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and Number of Pins				Process	Page
				PDIP	SOJ	CDIP	CLCC		
2K x 8	CE & OE	MT5C1608	12 to 35	24	24	24	24	CMOS	4-3
4K x 4	CE only	MT5C1604	12 to 35	20	24	20	20	CMOS	4-11
4K x 4	CE & OE	MT5C1605	12 to 35	22	24	22	22	CMOS	4-19
4K x 4	Separate I/O	MT5C1606	12 to 35	24	24	24	28	CMOS	4-27
4K x 4	Separate I/O HI-Z	MT5C1607	12 to 35	24	24	24	28	CMOS	4-27
4K x 16	CE, OE & ALE	MT5C6416	25 to 45	40	-	40	-	CMOS	4-35
8K x 8	CE1, CE2 & OE	MT5C6408	12 to 35	28	28	28	32	CMOS	4-37
16K x 1	CE only	MT5C1601	12 to 35	20	24	20	20	CMOS	4-45
16K x 4	CE only	MT5C6404	12 to 35	22	24	22	22	CMOS	4-53
16K x 4	CE & OE	MT5C6405	12 to 35	24	24	24	28	CMOS	4-61
16K x 4	Cache Tag	MT5C6405T	12 to 35	24	24	24	28	CMOS	4-69
16K x 4	Separate I/O, CE1, CE2	MT5C6406	12 to 35	28	28	28	28	CMOS	4-77
16K x 4	Separate I/O HI-Z	MT5C6407	12 to 35	28	28	28	28	CMOS	4-77
32K x 8	CE & OE	MT5C2568	25 to 45	28	28	28	32	CMOS	4-93
64K x 1	CE only	MT5C6401	12 to 35	22	24	22	22	CMOS	4-85
64K x 4	CE only	MT5C2564	25 to 45	24	24	24	28	CMOS	4-101
64K x 4	CE & OE	MT5C2565	25 to 45	28	28	28	28	CMOS	4-109
128K x 8	CE & OE	MT5C1008	25 to 45	28	-	28	-	CMOS	4-125
256K x 1	CE only	MT5C2561	25 to 45	24	24	24	28	CMOS	4-117
256K x 4	CE & OE	MT5C1005	25 to 45	28	-	28	-	CMOS	4-127
1MEG x 1	CE & OE	MT5C1001	25 to 45	28	-	28	-	CMOS	4-129

SRAM 2K x 8 SRAM

FEATURES

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC (28 pin)	EC
• Two Volt Data Retention	L

GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

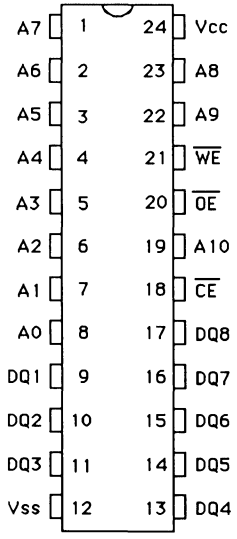
For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

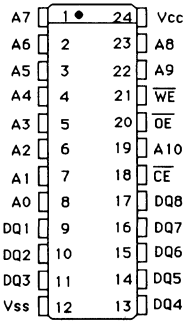
PIN ASSIGNMENT (Top View)

24L/300 DIP



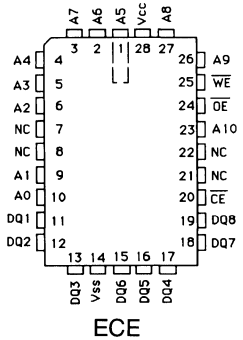
PG, CF

24L/300 SOJ



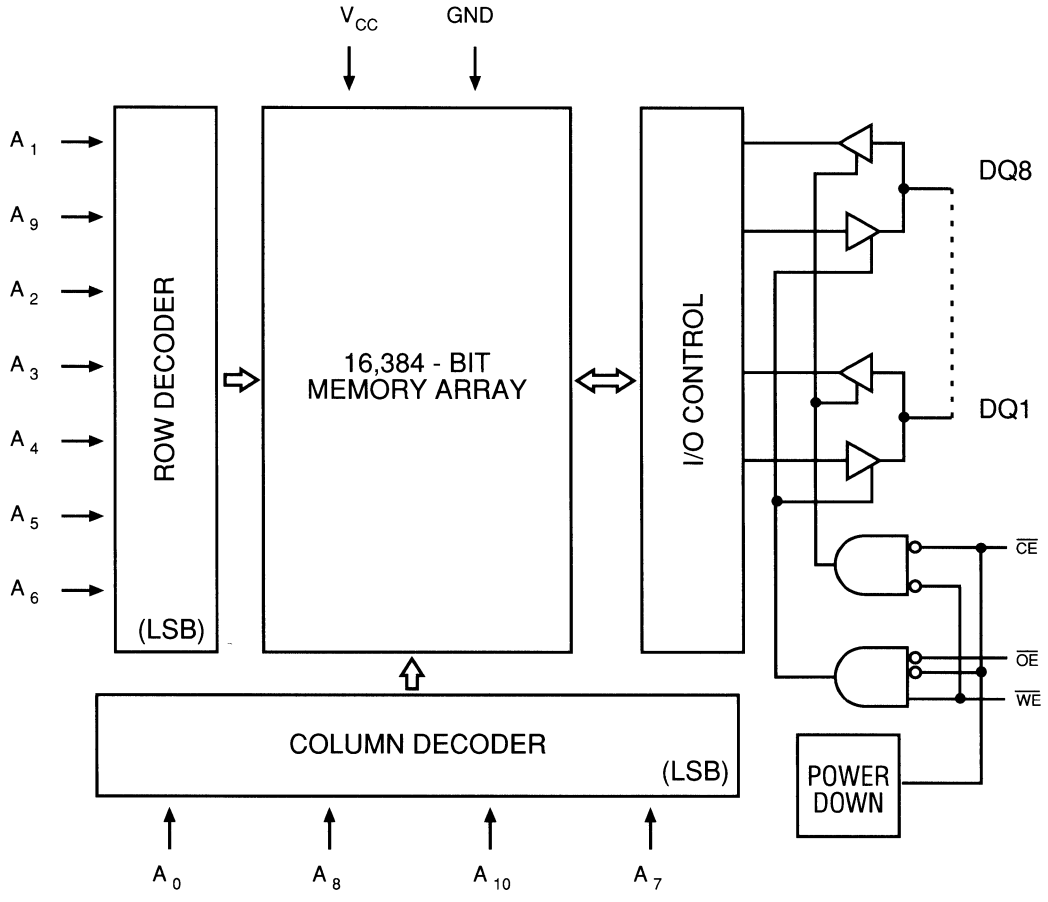
DJB

28L/LCC



ECE

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	DOUT	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 4.2mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip enable access time	^tACE		12		15		20		25		30		35	ns	
Output hold from access change	^tOH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power down time	^tPD		12		15		20		25		30		35	ns	
Output enable access time	^tAOE		10		12		15		15		20		20	ns	
Output enable to output in low Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in high Z	^tHZOE		10		10		15		15		20		20	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip enable to end of write	^tCW	10		12		15		20		25		30		ns	
Address valid to end of write	^tAW	12		15		15		20		25		30		ns	
Address set-up time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data set-up time	^tDS	10		10		12		15		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

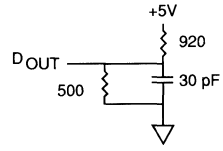


Fig. 1 OUTPUT LOAD EQUIVALENT

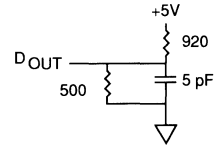


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

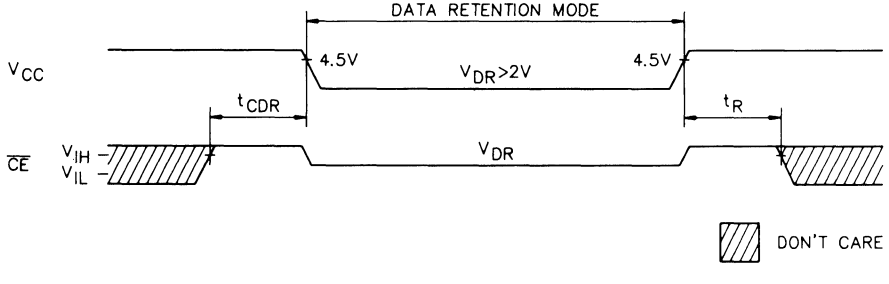
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

FAST SRAM

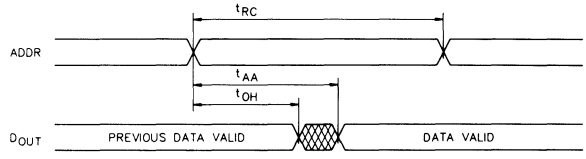
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	Vcc=2v		95	500	µA
			Vcc=3v		350	750	µA
^{t}CDR(4)	Chip Deselect to Data Retention Time			0		—	ns
^{t}R(4)	Operation Recovery Time			^{t}RC(11)			ns

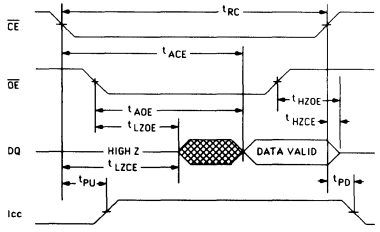
LOW Vcc DATA RETENTION WAVEFORM



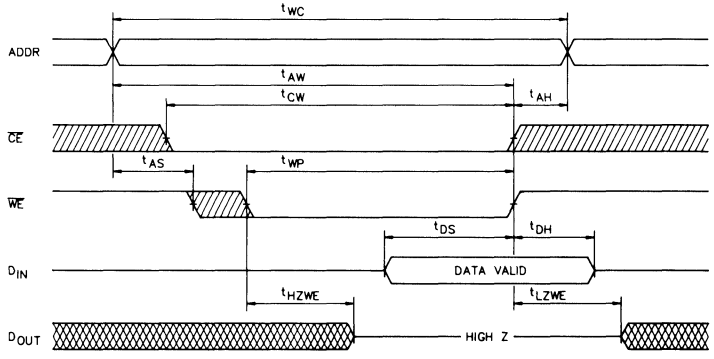
READ CYCLE NO. 1 (8, 9)



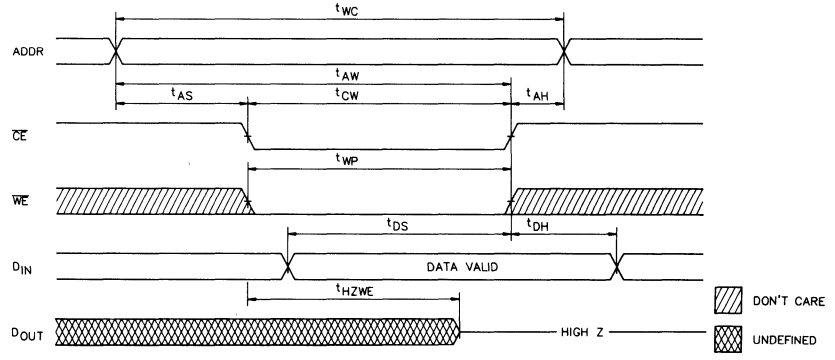
READ CYCLE NO. 2 (7, 8, 10)



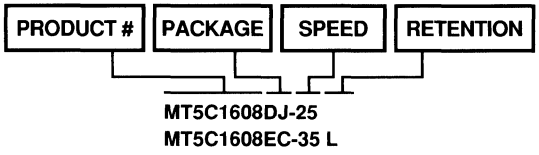
WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ORDER INFORMATION



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Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

SRAM 4K x 4 SRAM

FEATURES

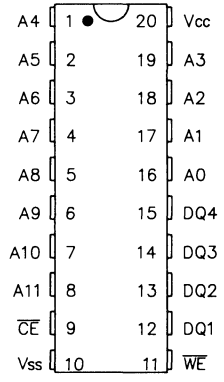
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

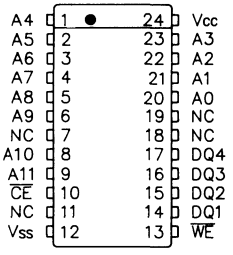
PIN ASSIGNMENT (Top View)

20L/300 DIP



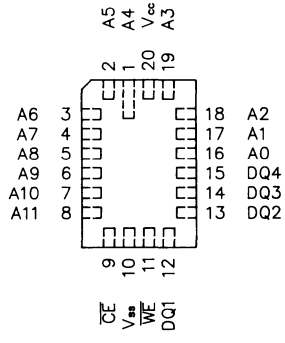
PE, CD

24L/300 SOJ



DJB

20L/LCC



ECE

GENERAL DESCRIPTION

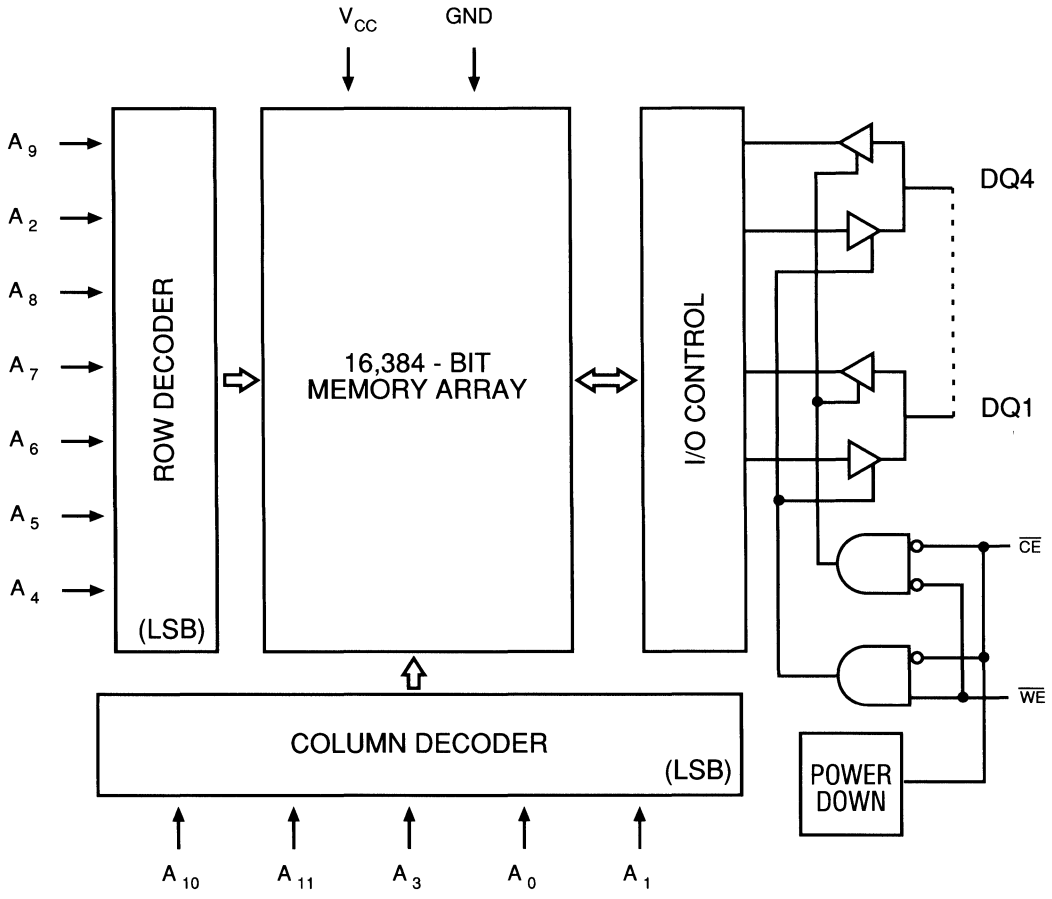
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	DOUT	ACTIVE
WRITE	L	L	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, f = 0 $V_{IH} \ge V_{CC}$ - 0.2	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip enable access time	^tACE		12		15		20		25		30		35	ns	
Output hold from access change	^tOH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power down time	^tPD		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip enable to end of write	^tCW	10		12		15		20		25		30		ns	
Address valid to end of write	^tAW	12		15		15		20		25		30		ns	
Address set-up time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data set-up time	^tDS	10		10		12		15		15		17		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

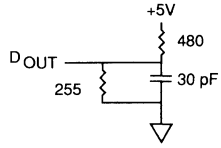


Fig. 1 OUTPUT LOAD EQUIVALENT

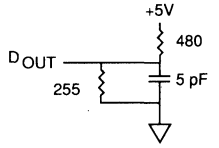


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

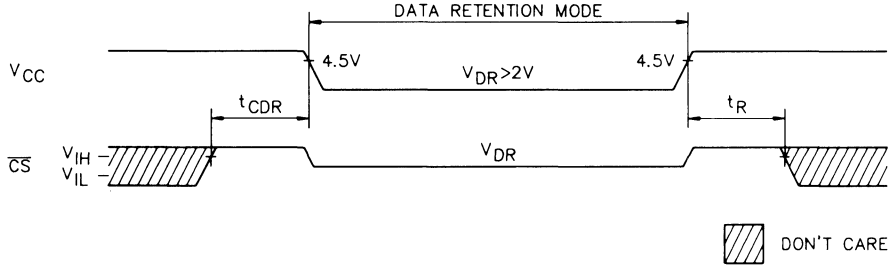
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

FAST SRAM

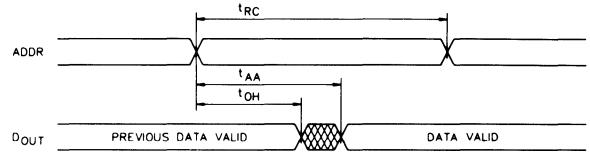
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	Vcc=2v	—	95	500	µA
			Vcc=3v	—	350	750	µA
^{t}CDR(4)	Chip Deselect to Data Retention Time			0		—	ns
^{t}R(4)	Operation Recovery Time			^{t}RC(11)			ns

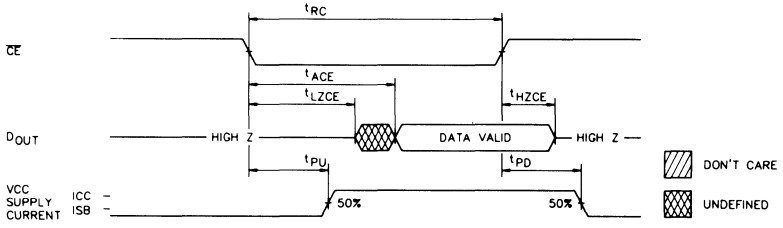
LOW Vcc DATA RETENTION WAVEFORM



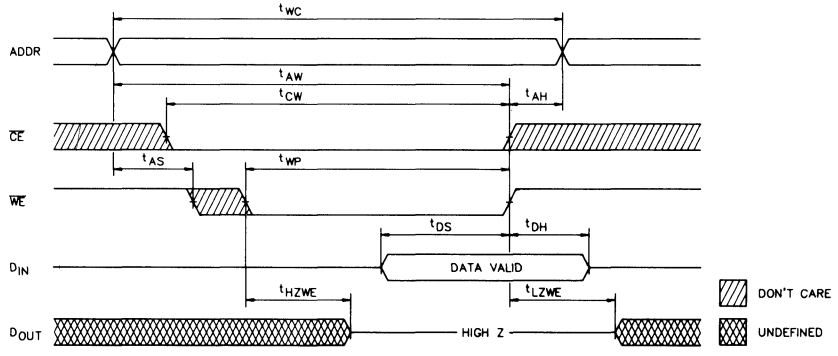
READ CYCLE NO. 1 (8, 9)



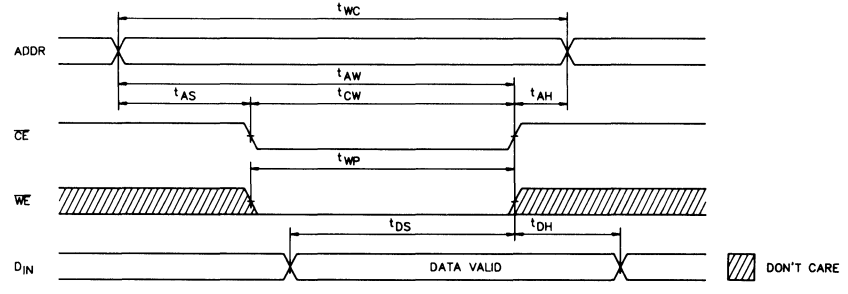
READ CYCLE NO. 2 (7, 8, 10)



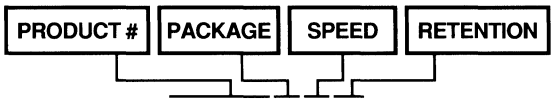
WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ORDER INFORMATION



MT5C1604DJ-25
MT5C1604EC-35 L

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SRAM

4K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

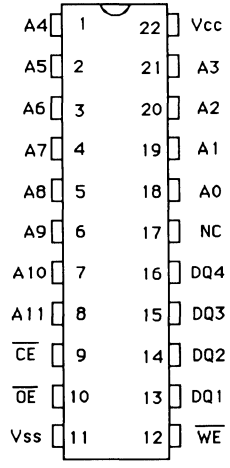
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

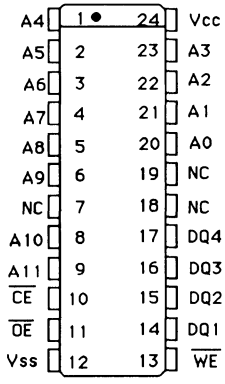
PIN ASSIGNMENT (Top View)

22L/300 DIP



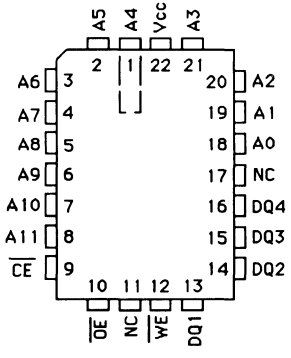
PF, CE

24L/300 SOJ



DJB

22L/LCC



ECD

GENERAL DESCRIPTION

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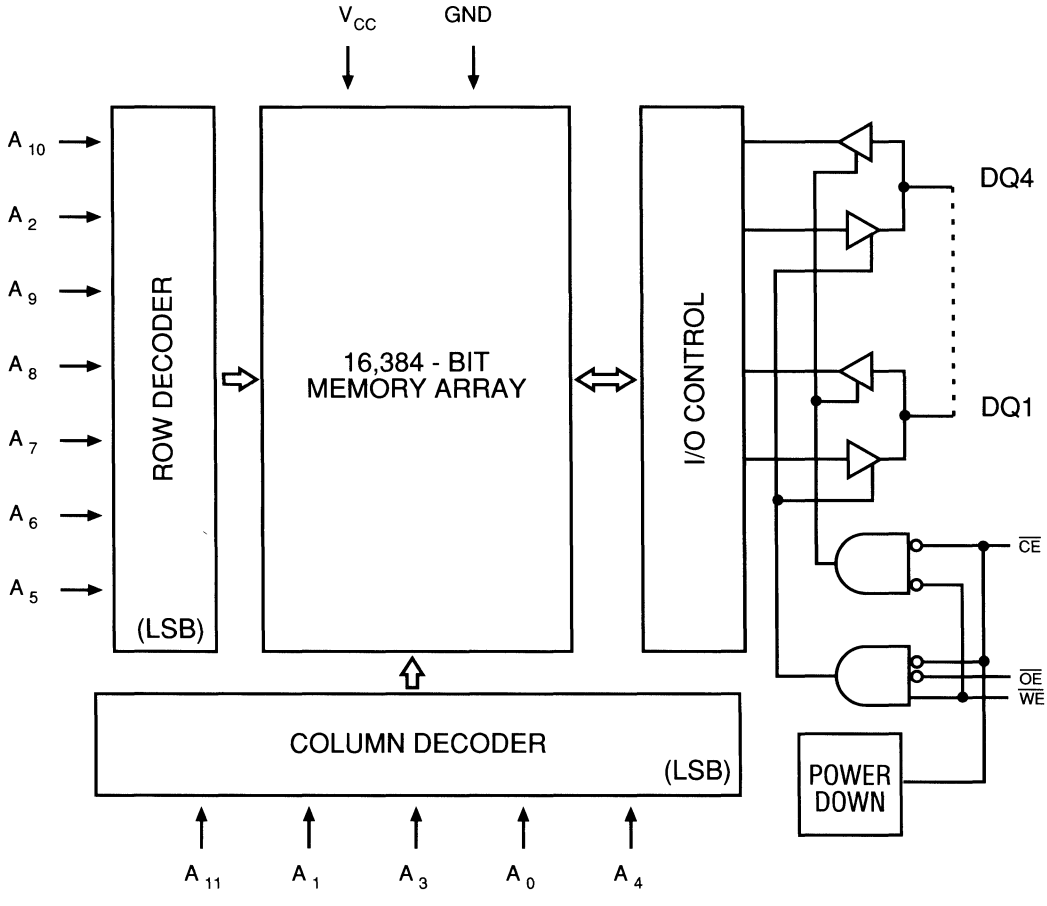
For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	DOUT	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \leq V_{OUT} \leq V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	45	40	40	40	mA	
	$\overline{CE} \geq V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \leq V_{SS}$ + 0.2, f = 0 $V_{IH} \geq V_{CC}$ - 0.2	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip enable access time	^tACE		12		15		20		25		30		35	ns	
Output hold from access change	^tOH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power down time	^tPD		12		15		20		25		30		35	ns	
Output enable access time	^tAOE		10		12		15		15		20		20	ns	
Output enable to output in low Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in high Z	^tHZOE		10		10		15		15		20		20	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip enable to end of write	^tCW	12		15		15		20		25		30		ns	
Address valid to end of write	^tAW	10		12		15		20		25		30		ns	
Address set-up time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data set-up time	^tDS	10		10		12		15		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

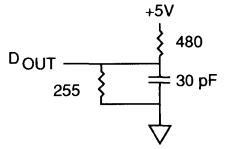


Fig. 1 OUTPUT LOAD EQUIVALENT

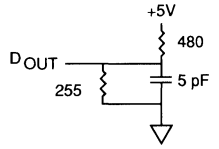


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

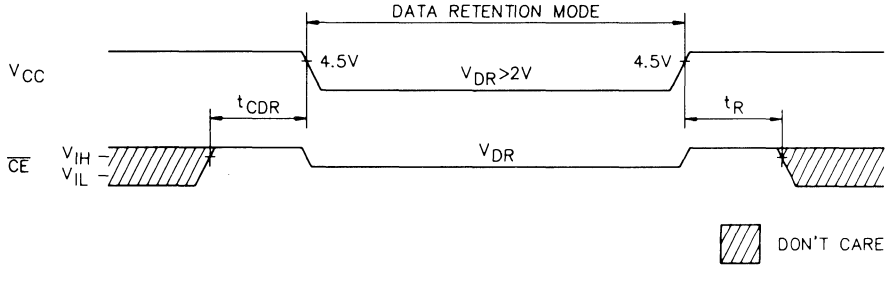
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

FAST SRAM

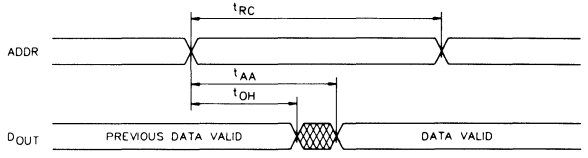
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v		95	500	µA
			Vcc=3v		350	750	µA
^{t}CDR(4)	Chip Deselect to Data Retention Time			0		—	ns
^{t}R(4)	Operation Recovery Time			^{t}RC(11)			ns

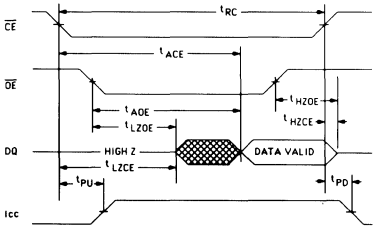
LOW Vcc DATA RETENTION WAVEFORM



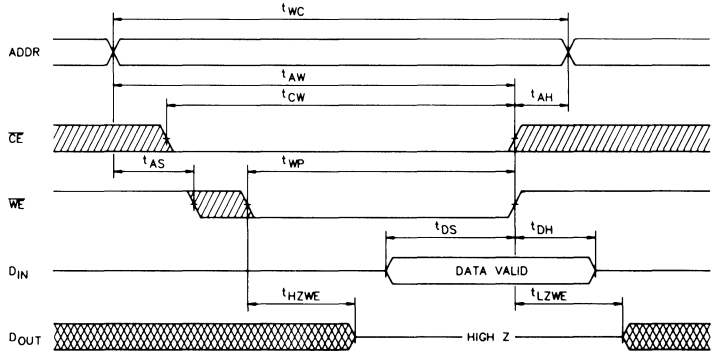
READ CYCLE NO. 1 (8, 9)



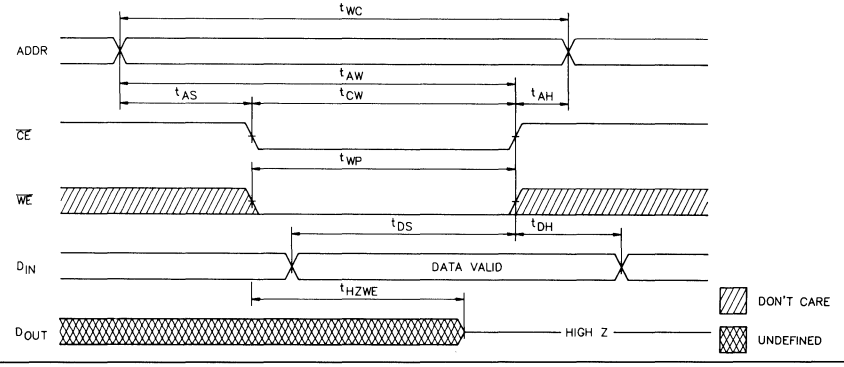
READ CYCLE NO. 2 (7, 8, 10)



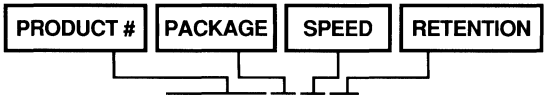
WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

SRAM

4K x 4 SRAM

WITH SEPARATE INPUTS AND OUTPUTS

FEATURES

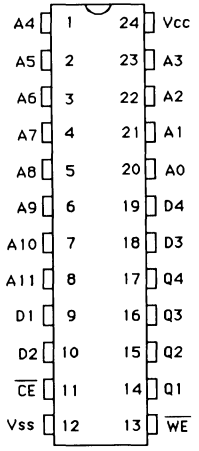
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible
- MT5C1606 – output tracks input during WRITE
- MT5C1607 – output high impedance during WRITE

OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

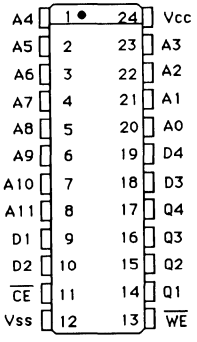
PIN ASSIGNMENT (Top View)

24L/300 DIP



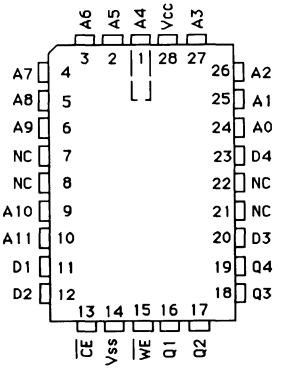
PG, CF

24L/300 SOJ



DJB

28L/LCC



ECE

GENERAL DESCRIPTION

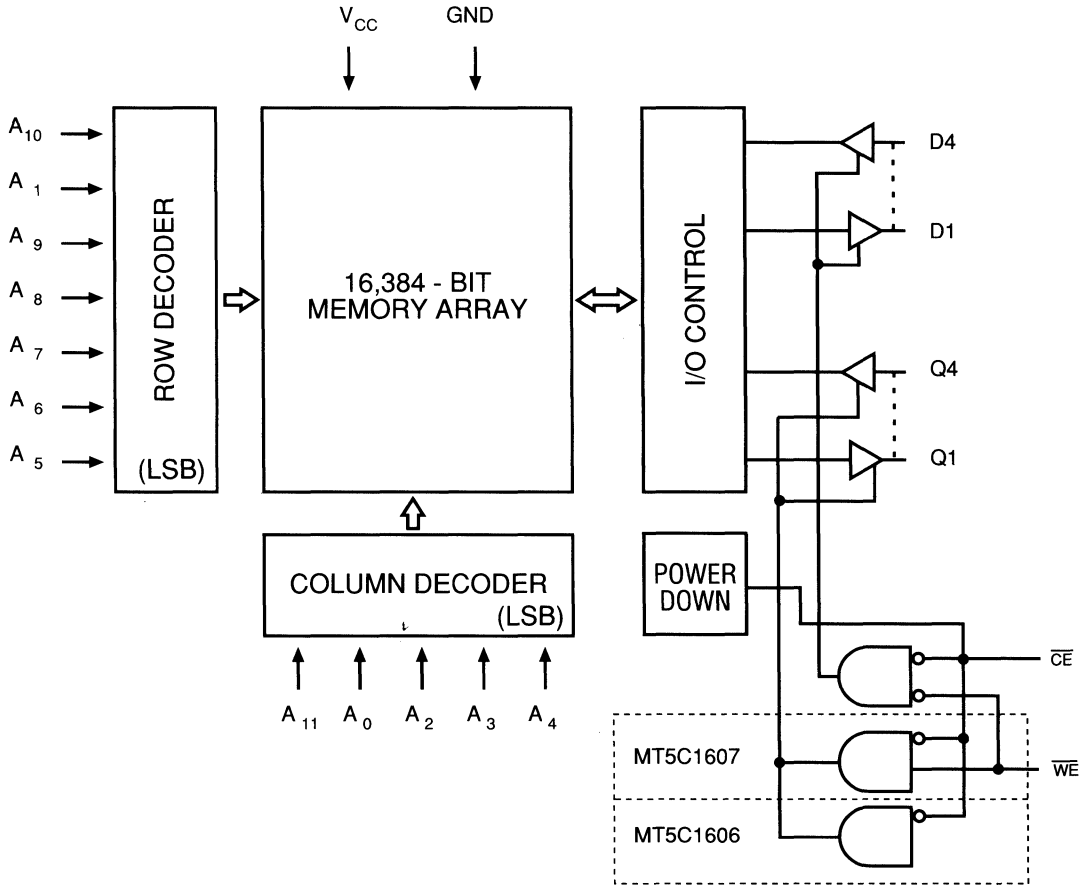
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 4 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	DOUT	ACTIVE
WRITE (1)	L	L	HIGH Z	ACTIVE
WRITE (2)	L	L	DIN	ACTIVE

NOTES: 1. MT5C1607 ONLY
2. MT5C1606 ONLY

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, f = 0 $V_{IH} \ge V_{CC}$ - 0.2	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	12		15		20		25		30		35		ns	
Address access time	t_{AA}		12		15		20		25		30		35	ns	
Chip enable access time	t_{ACE}		12		15		20		25		30		35	ns	
Output hold from access change	t_{OH}	3		3		3		3		3		3		ns	
Chip enable to output in low Z	t_{LZCE}	5		5		5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	t_{PU}	0		0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	t_{WC}	12		15		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	10		12		15		20		25		30		ns	
Address valid to end of write	t_{AW}	12		15		15		20		25		30		ns	
Address set-up time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	10		12		15		20		25		25		ns	
Data set-up time	t_{DS}	10		10		12		15		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	0		0		0		0		0		0		ns	
Write enable to output valid	t_{AWE}		12		15		20		25		30		35	ns	
Data valid to output valid	t_{ADV}		12		15		20		25		30		35	ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

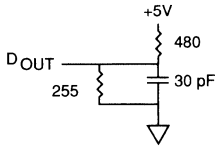


Fig. 1 OUTPUT LOAD EQUIVALENT

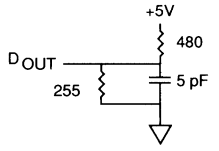


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

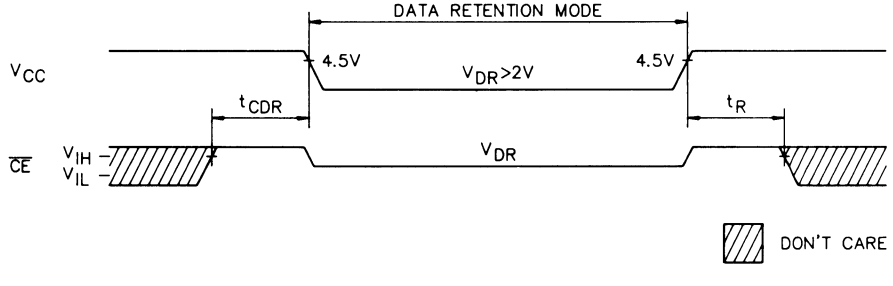
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

FAST SRAM

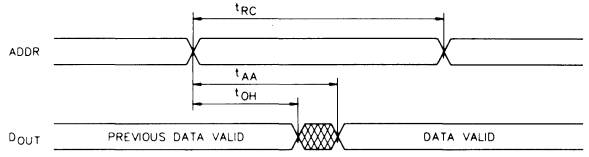
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	Vcc=2v		95	500	µA
			Vcc=3v		350	750	µA
^{t}CDR(4)	Chip Deselect to Data Retention Time			0		—	ns
^{t}R(4)	Operation Recovery Time			^{t}RC(11)			ns

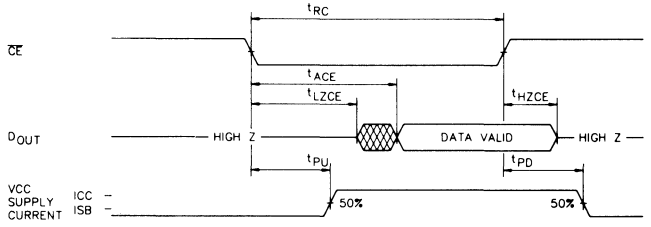
LOW Vcc DATA RETENTION WAVEFORM



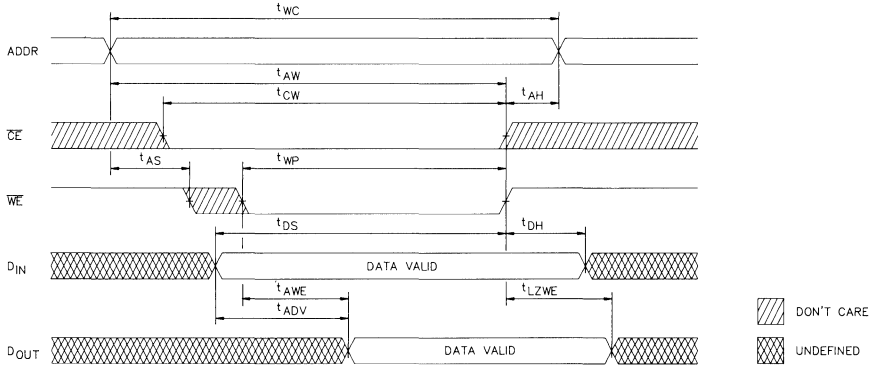
READ CYCLE NO. 1 (8, 9)



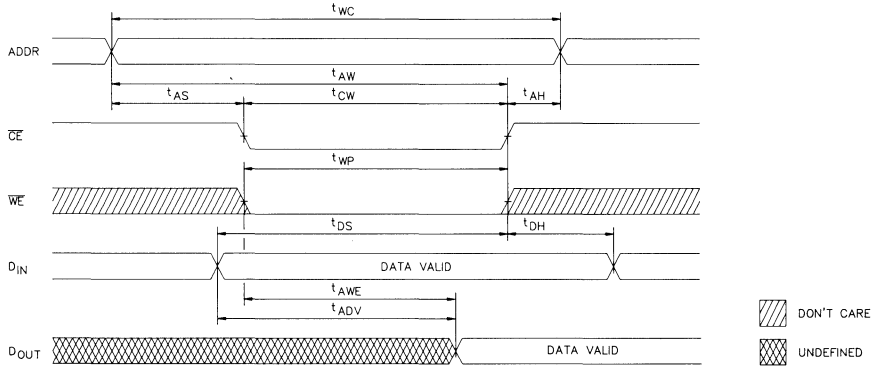
READ CYCLE NO. 2 (7, 8, 10)



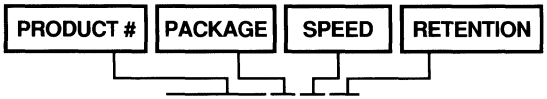
WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ORDER INFORMATION



MT5C1606DJ-25
MT5C1607EC-35 L

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Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

SRAM

4K x 16 SRAM

LATCHED CACHE DATA RAM

FEATURES

- On-chip address latch.
- Compatible with the Intel 82385 cache memory controller.
- Fast access times: 25ns, 35ns and 45ns.
- Upper and lower byte selects.
- Fast output enable: 10ns into 100pF load.

OPTIONS — MARKING

- Timing

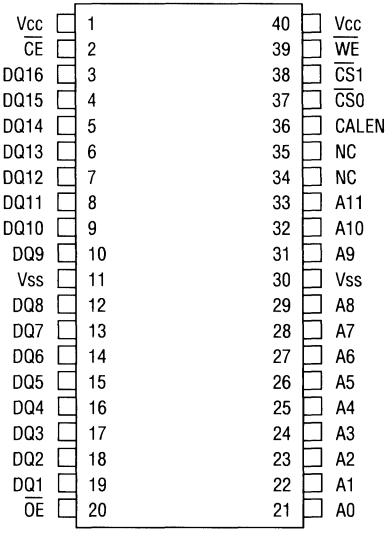
25ns access	-25
35ns access	-35
45ns access	-45

- Packages

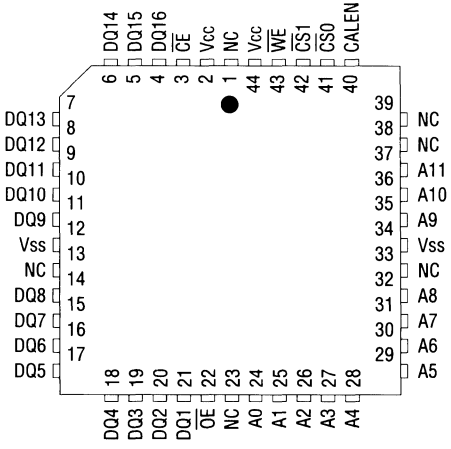
Plastic DIP (600 mil)	None
Ceramic DIP (600 mil)	C
PLCC	EJ

PIN ASSIGNMENT (Top View)

40L DIP



44L/LCC



GENERAL DESCRIPTION

The MT5C6416 is one of a family of fast SRAM latched cache memories. It employs a high speed, low power design using a 4-transistor memory cell. It is fabricated using double layer metal, double layer polysilicon CMOS technology.

The MT5C6416 is designed to be a cache data memory cell building block. It easily interfaces with the Intel 82385 cache memory controller.

The device operates from a single +5V power supply and all inputs and outputs are TTL compatible.

Micron applies the highest level of design and process technology in all their Static RAM products. With a full line of 256K density SRAM's at access times of 25 nanoseconds, Micron has firmly established itself as the leading fast SRAM supplier. So, for your fastest memory requirements, come to the fast memory supplier. . .
Micron.

SRAM 8K x 8 SRAM

FEATURES

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
Ceramic DIP (300 mil)	C
Ceramic DIP (600 mil)	CW
Plastic SOJ (300 mil)	DJ
Ceramic LCC (28 pin)	EC
Ceramic LCC (32 pin)	ECW
• Two Volt Data Retention	L

GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

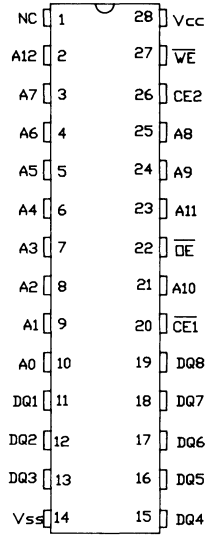
For flexibility in high speed memory applications, Micron offers two chip enables on the x 8 organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

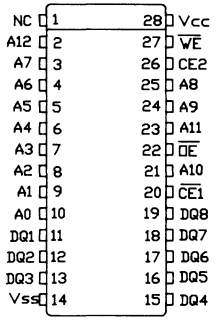
PIN ASSIGNMENT (Top View)

28L/300/600 DIP



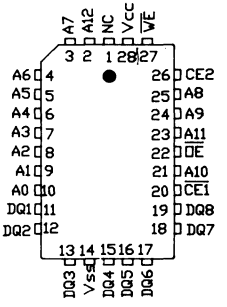
PJ, PK, CH

28L/300 SOJ



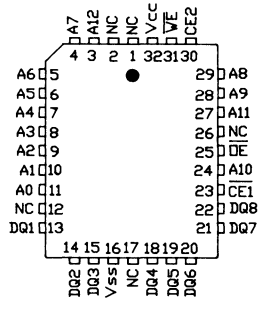
DJC

28L/LCC



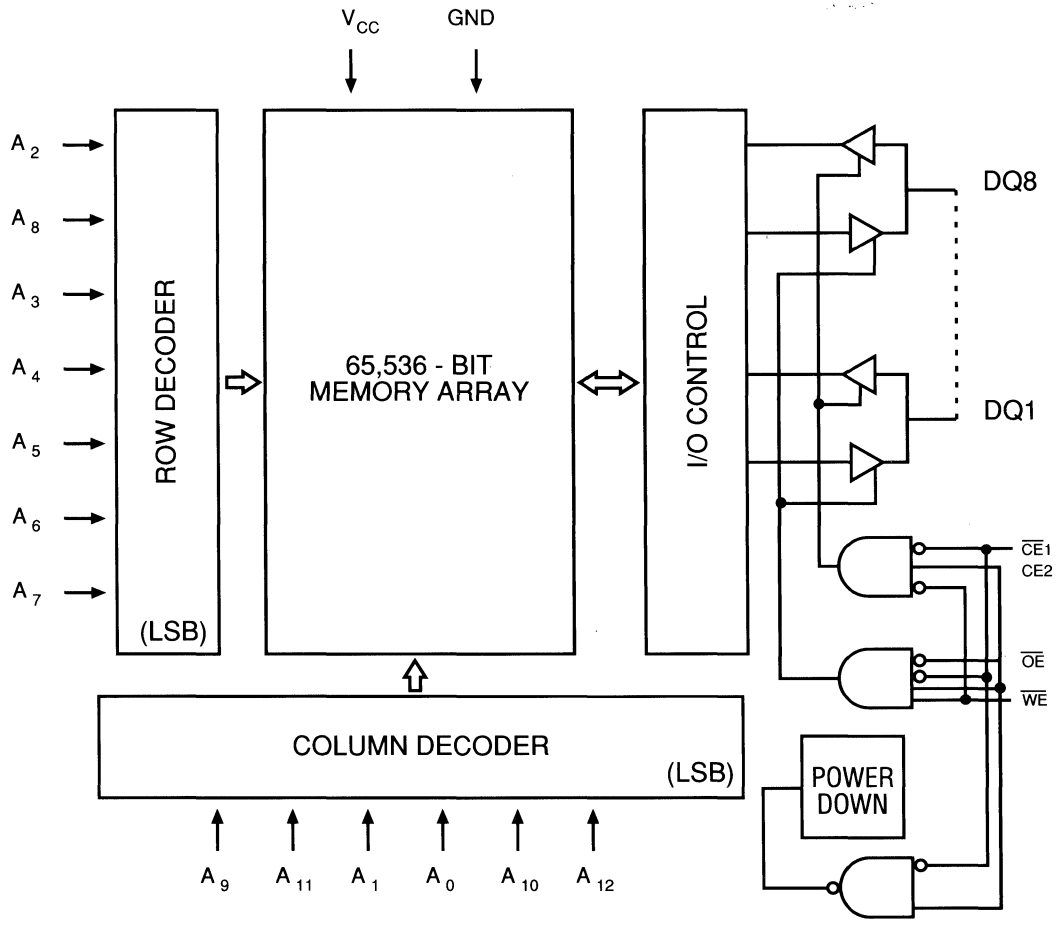
ECE

32L/LCC



ECF

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	DQ OPERATION	POWER
STANDBY	H	X	X	X	HIGH Z	STANDBY
STANDBY	X	L	X	X	HIGH Z	STANDBY
READ	L	H	H	L	DOUT	ACTIVE
READ	L	H	H	H	HIGH Z	ACTIVE
WRITE	L	H	L	X	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \leq V_{OUT} \leq V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 4.2mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	45	40	40	40	mA	
	$\overline{CE} \geq V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \geq V_{SS}$ + 0.2, $V_{IH} \geq V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip enable access time	^tACE		12		15		20		25		30		35	ns	
Output hold from access change	^tOH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power down time	^tPD		12		15		20		25		30		35	ns	
Output enable access time	^tAOE		10		12		15		15		20		20	ns	
Output enable to output in low Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in high Z	^tHZOE		10		10		15		15		20		20	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip enable to end of write	^tCW	10		12		15		20		25		30		ns	
Address valid to end of write	^tAW	12		15		15		20		25		30		ns	
Address set-up time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data set-up time	^tDS	10		10		12		15		15		17		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

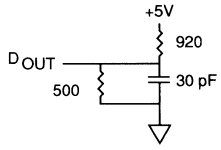


Fig. 1 OUTPUT LOAD EQUIVALENT

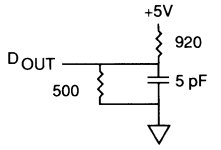


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

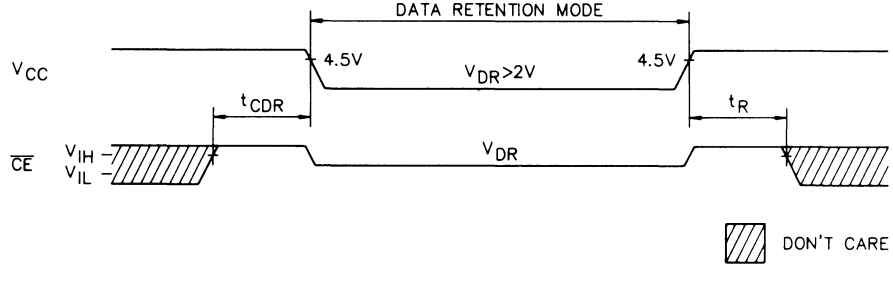
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

FAST SRAM

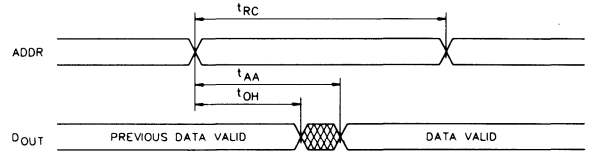
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	Vcc=2v		95	500	µA
			Vcc=3v		350	750	µA
$^{t}CDR^{(4)}$	Chip Deselect to Data Retention Time			0		—	ns
$^{t}R^{(4)}$	Operation Recovery Time			$^{t}RC^{(11)}$			ns

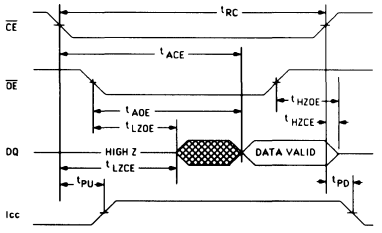
LOW Vcc DATA RETENTION WAVEFORM



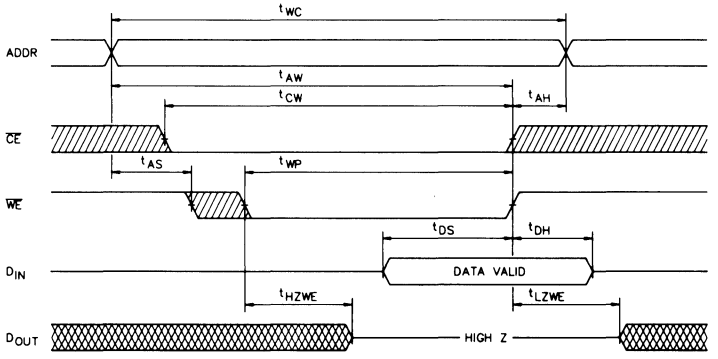
READ CYCLE NO. 1 (8, 9)



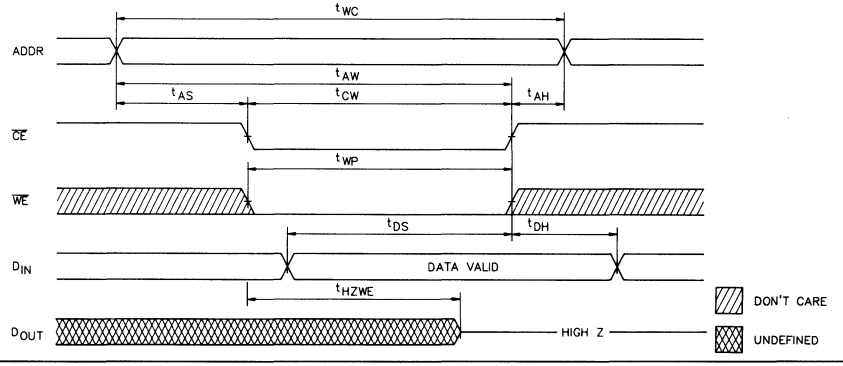
READ CYCLE NO. 2 (7, 8, 10)



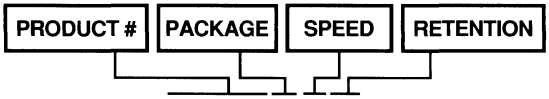
WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ORDER INFORMATION



MT5C6408DJ-15
MT5C6408EC-35 L

The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

SRAM 16K x 1 SRAM

FEATURES

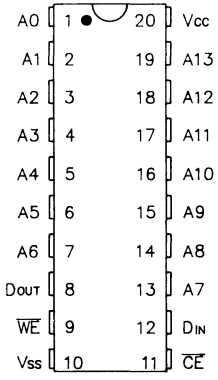
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

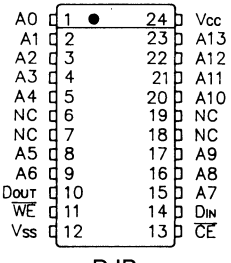
PIN ASSIGNMENT (Top View)

20L/300 DIP



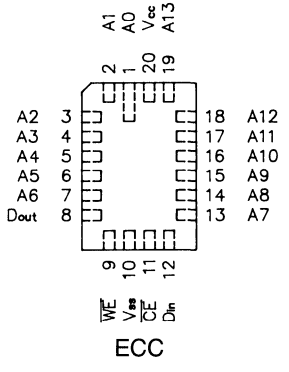
PD, CD

24L/300 SOJ



DJB

20L/LCC



ECC

GENERAL DESCRIPTION

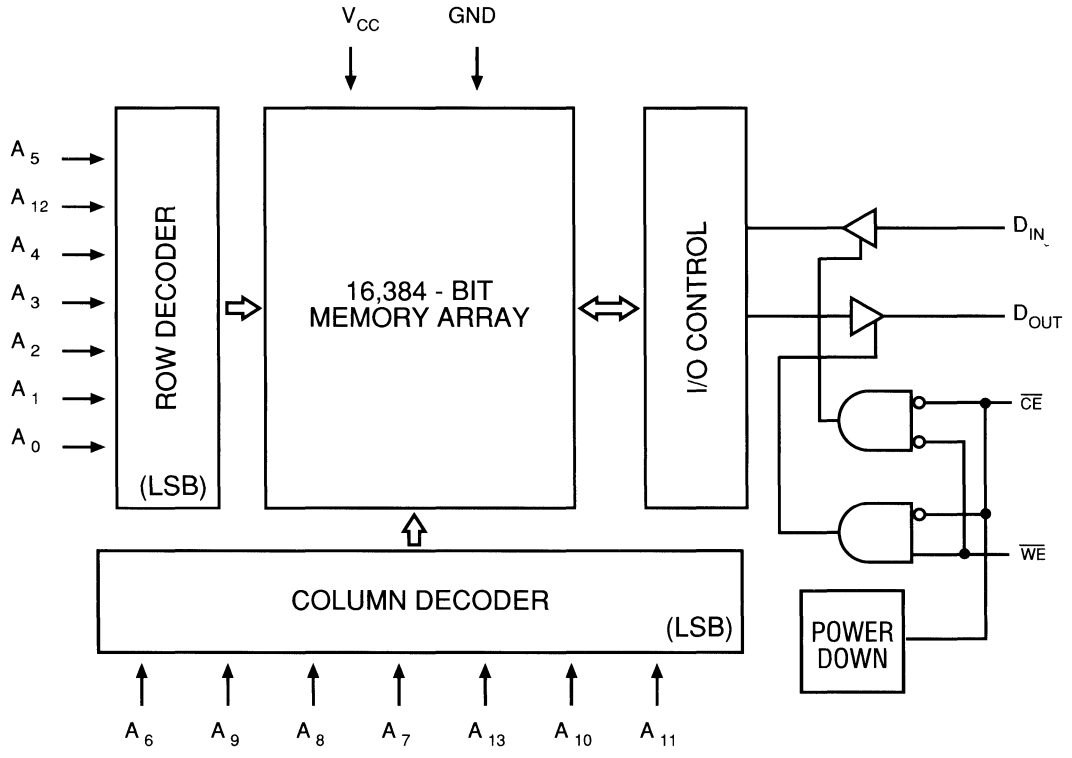
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	DOUT	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, f = 0 $V_{IH} \ge V_{CC}$ - 0.2	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip enable access time	^tACE		12		15		20		25		30		35	ns	
Output hold from access change	^tOH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power down time	^tPD		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip enable to end of write	^tCW	10		12		15		20		25		30		ns	
Address valid to end of write	^tAW	12		15		15		20		25		30		ns	
Address set-up time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data set-up time	^tDS	10		10		12		15		15		17		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

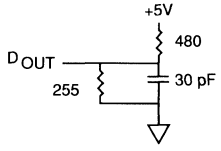


Fig. 1 OUTPUT LOAD EQUIVALENT

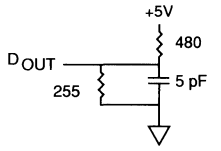


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

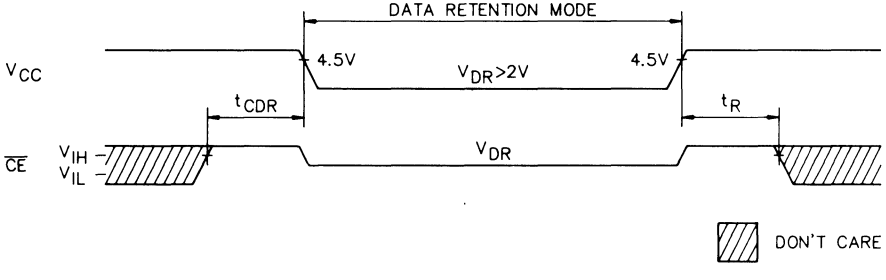
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. ICC is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

FAST SRAM

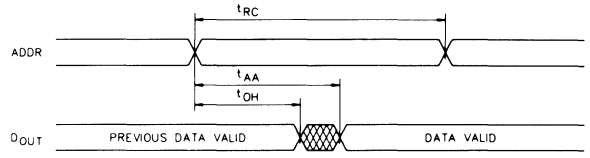
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
VDR	Vcc for Retention Data			2		—	V
ICCDR	Data Retention Current	$\overline{CE}$ ≥ Vcc - 0.2V VIN ≥ Vcc - 0.2V or ≤ 0.2V	Vcc=2v	—	95	500	µA
			Vcc=3v	—	350	750	µA
^{t}CDR(4)	Chip Deselect to Data Retention Time			0		—	ns
^{t}R(4)	Operation Recovery Time			^{t}RC(11)			ns

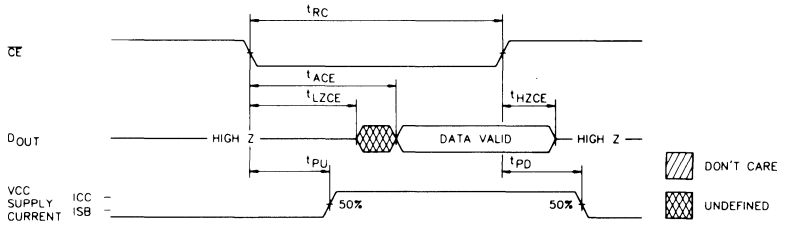
LOW Vcc DATA RETENTION WAVEFORM



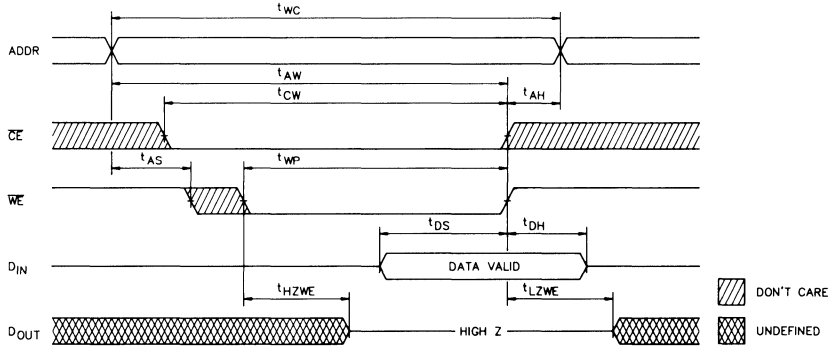
READ CYCLE NO. 1 (8, 9)



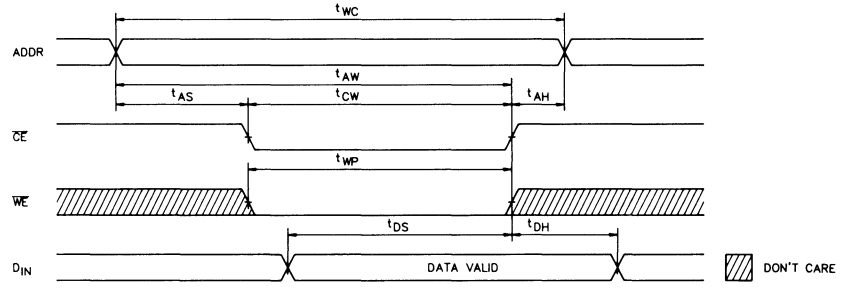
READ CYCLE NO. 2 (7, 8, 10)



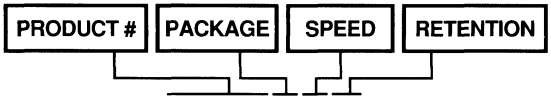
WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ORDER INFORMATION



MT5C1601DJ-45
MT5C1601EC-35 L

The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

SRAM 16K x 4 SRAM

FEATURES

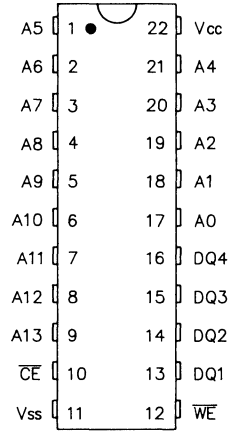
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

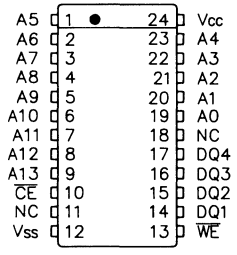
PIN ASSIGNMENT (Top View)

22L/300 DIP



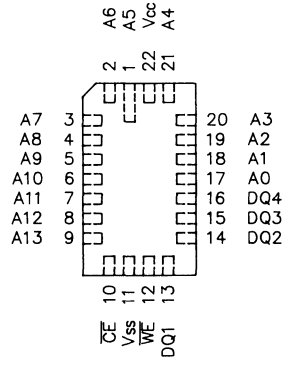
PF, CE

24L/300 SOJ



DJB

22L/LCC



ECD

GENERAL DESCRIPTION

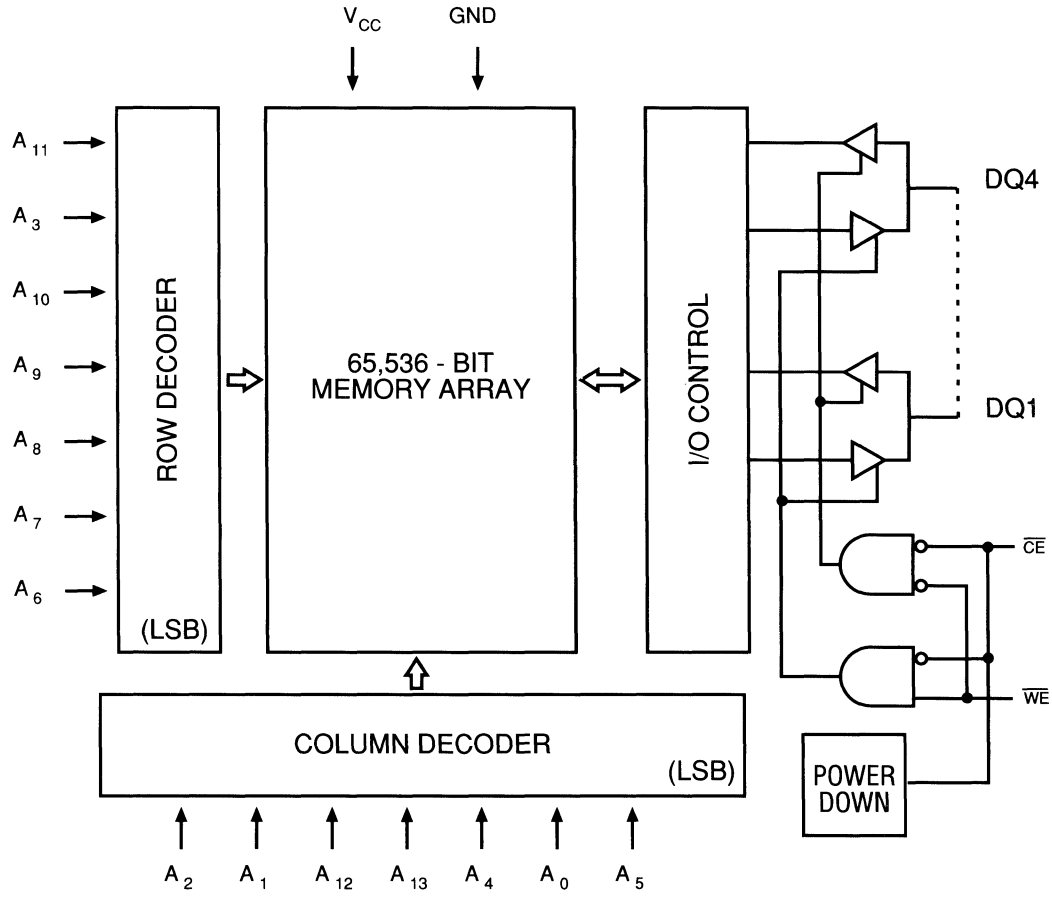
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	DOUT	ACTIVE
WRITE	L	L	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip enable access time	^tACE		12		15		20		25		30		35	ns	
Output hold from access change	^tOH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power down time	^tPD		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip enable to end of write	^tCW	10		12		15		20		25		30		ns	
Address valid to end of write	^tAW	12		15		15		20		25		30		ns	
Address set-up time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data set-up time	^tDS	10		10		12		15		15		17		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

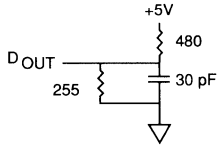


Fig. 1 OUTPUT LOAD EQUIVALENT

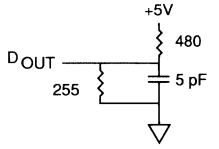


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

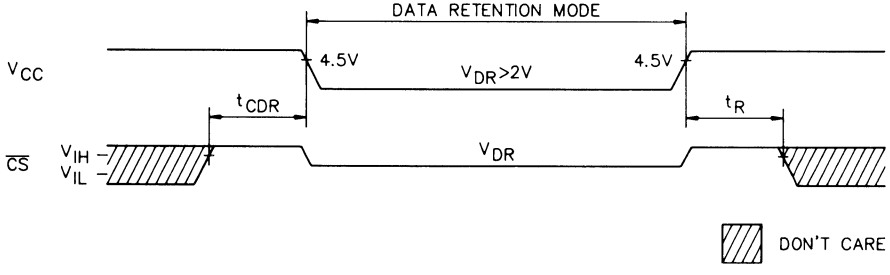
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

FAST SRAM

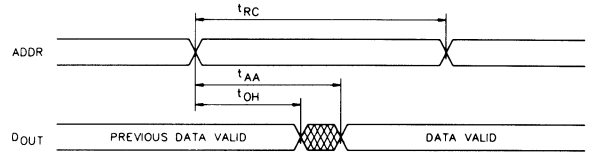
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	Vcc=2v		95	500	µA
			Vcc=3v		350	750	µA
^{t}CDR(4)	Chip Deselect to Data Retention Time			0		—	ns
^{t}R(4)	Operation Recovery Time			^{t}RC(11)			ns

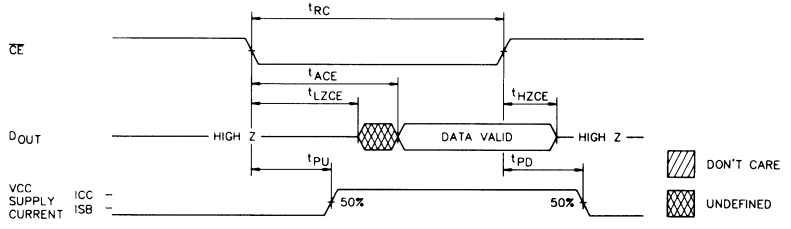
LOW Vcc DATA RETENTION WAVEFORM



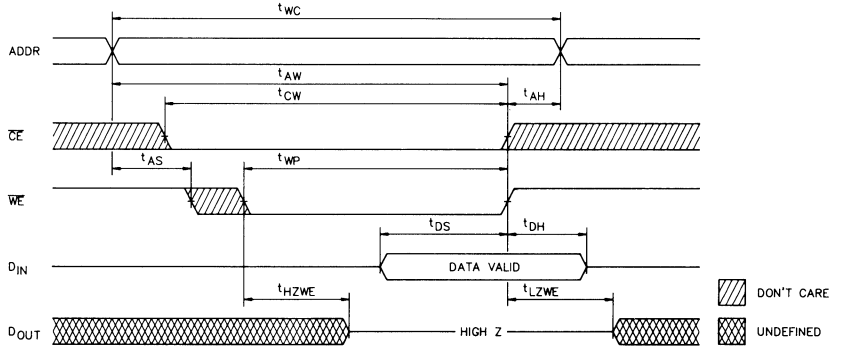
READ CYCLE NO. 1 (8, 9)



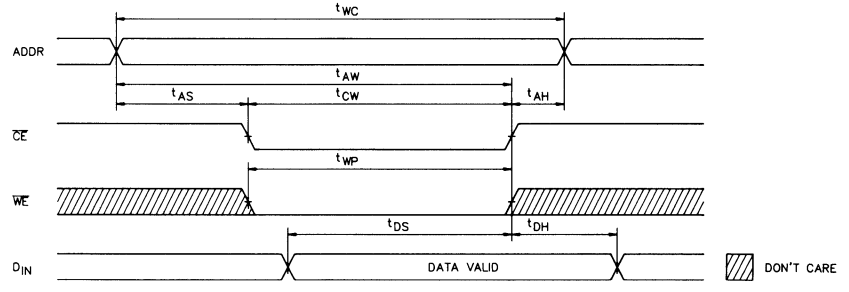
READ CYCLE NO. 2 (7, 8, 10)



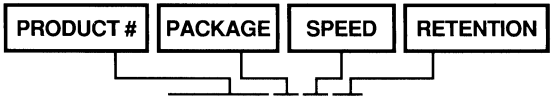
WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ORDER INFORMATION



MT5C6404DJ-25
MT5C6404EC-35 L

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SRAM

16K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

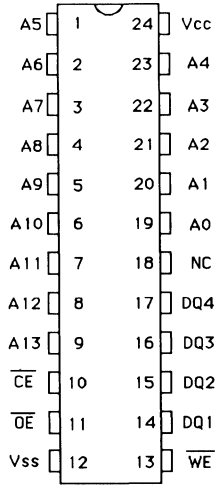
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

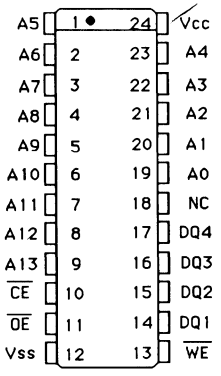
PIN ASSIGNMENT (Top View)

24L/300 DIP



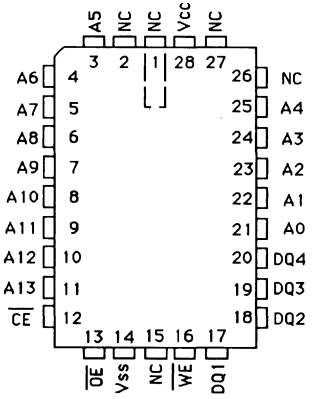
PG, CF

24L/300 SOJ



DJB

28L/LCC



CH

GENERAL DESCRIPTION

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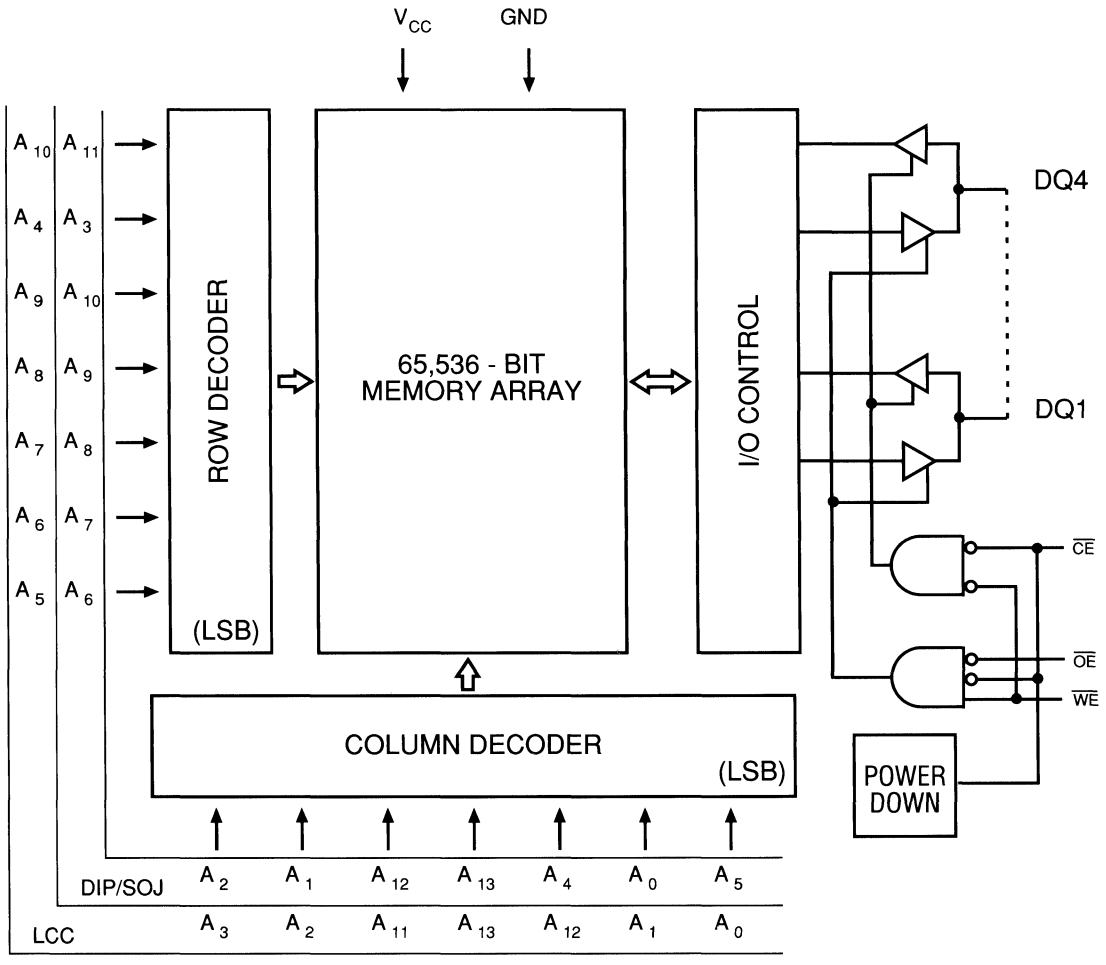
For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	DOUT	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, Vcc = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip enable access time	^tACE		12		15		20		25		30		35	ns	
Output hold from access change	^tOH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power down time	^tPD		12		15		20		25		30		35	ns	
Output enable access time	^tAOE		10		12		15		15		20		20	ns	
Output enable to output in low Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in high Z	^tHZOE		10		10		15		15		20		20	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip enable to end of write	^tCW	10		12		15		20		25		30		ns	
Address valid to end of write	^tAW	12		15		15		20		25		30		ns	
Address set-up time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data set-up time	^tDS	10		10		12		15		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

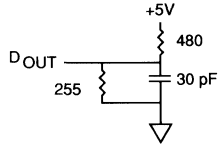


Fig. 1 OUTPUT LOAD EQUIVALENT

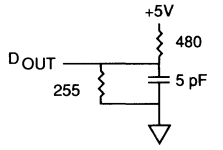


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

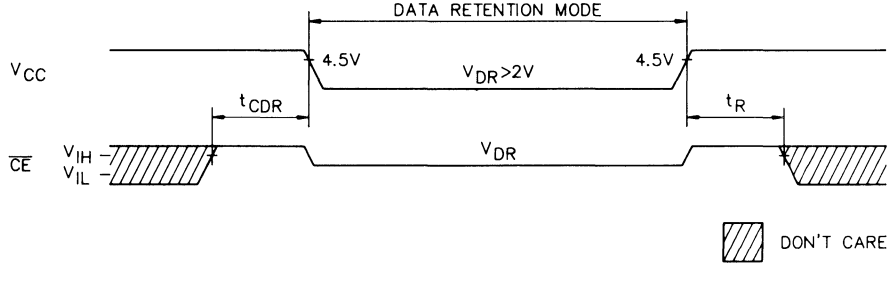
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

FAST SRAM

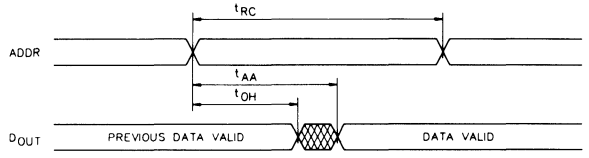
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	Vcc=2v		95	500	µA
			Vcc=3v		350	750	µA
^{t}CDR(4)	Chip Deselect to Data Retention Time			0		—	ns
^{t}R(4)	Operation Recovery Time			^{t}RC(11)			ns

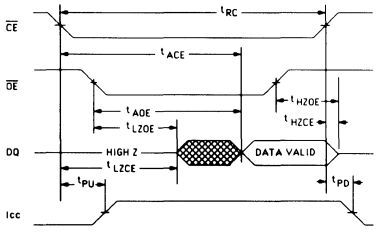
LOW Vcc DATA RETENTION WAVEFORM



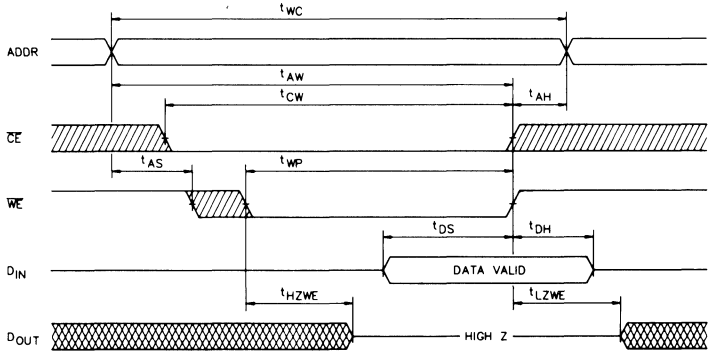
READ CYCLE NO. 1 (8, 9)



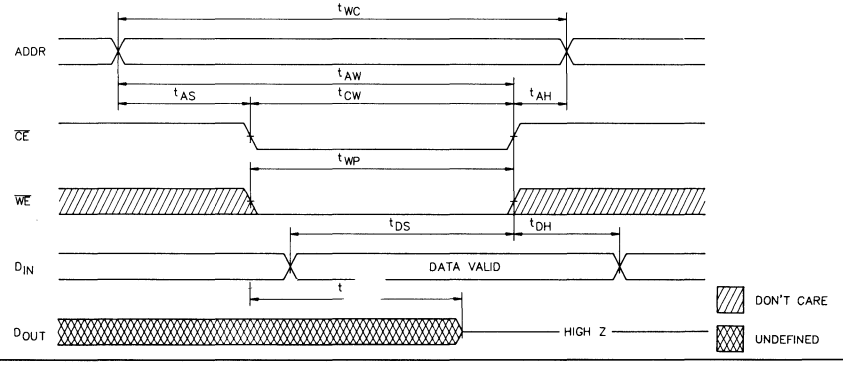
READ CYCLE NO. 2 (7, 8, 10)



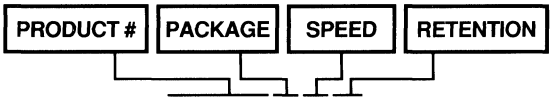
WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

SRAM

16K x 4 SRAM

CACHE-TAG

FEATURES

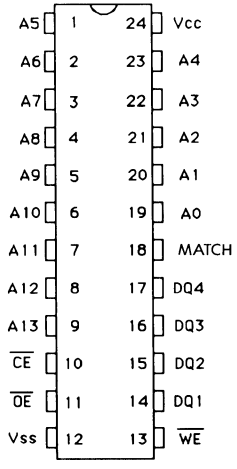
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast match time: 15ns

OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC

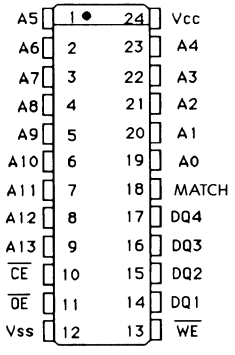
PIN ASSIGNMENT (Top View)

24L/300 DIP



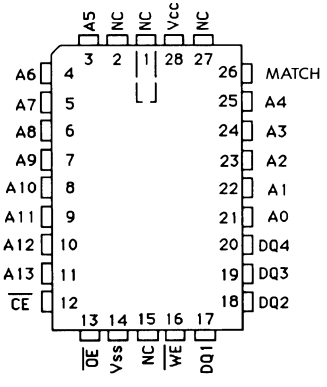
PG, CF

24L/300 SOJ



DJB

28L/LCC



CH

GENERAL DESCRIPTION

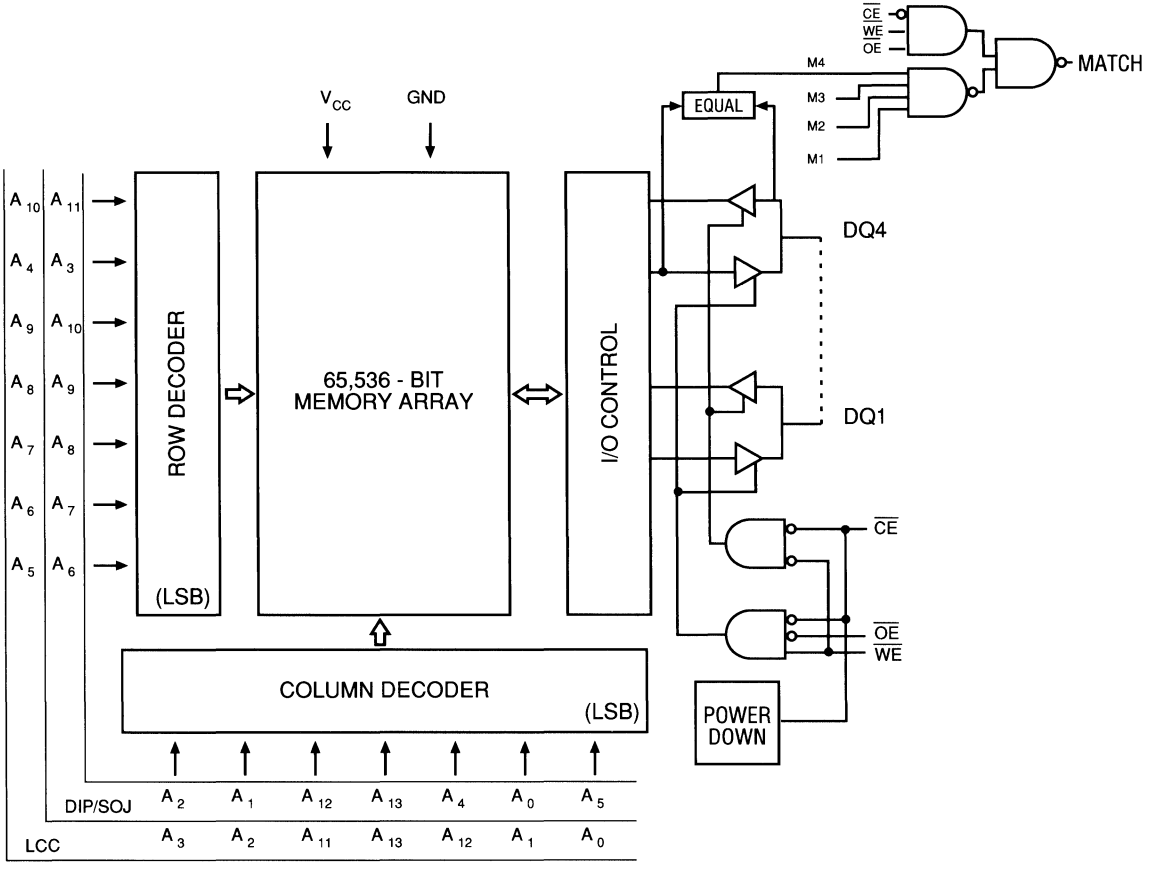
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable $\overline{CE}$ on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER	MATCH
STANDBY	X	H	X	HIGH Z	STANDBY	HIGH
READ	L	L	H	DOUT	ACTIVE	HIGH
READ	H	L	H	HIGH Z	ACTIVE	ACTIVE
WRITE	X	L	L	DIN	ACTIVE	HIGH

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2 $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C, Vcc = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip enable access time	^tACE		12		15		20		25		30		35	ns	
Output hold from access change	^tOH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power down time	^tPD		12		15		20		25		30		35	ns	
Output enable access time	^tAOE		10		12		15		15		20		20	ns	
Output enable to output in low Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in high Z	^tHZOE		10		10		15		15		20		20	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip enable to end of write	^tCW	10		12		15		20		25		30		ns	
Address valid to end of write	^tAW	12		15		15		20		25		30		ns	
Address set-up time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data set-up time	^tDS	10		10		12		15		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

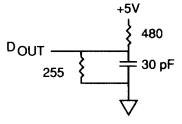


Fig. 1 OUTPUT LOAD EQUIVALENT

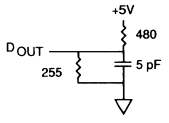


Fig. 2 OUTPUT LOAD EQUIVALENT

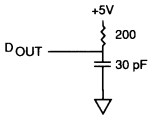
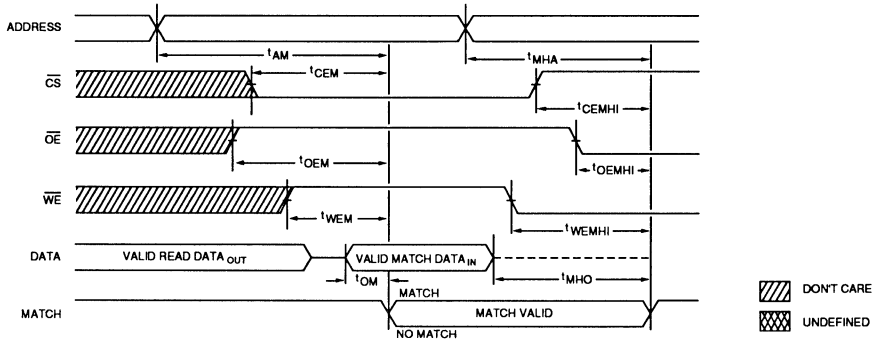


Fig. 3 OUTPUT LOAD EQUIVALENT

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
MATCH cycle															
Address to MATCH valid	^tAM		15		17		22		25		30		35	ns	12
MATCH hold from address	^tMHA	5		5		5		5		5		5		ns	12
$\overline{CE}$ to MATCH	^tCEM		10		12		15		20		20		20	ns	12
$\overline{CE}$ to MATCH high	^tCEMhi		10		12		15		20		20		20	ns	12
$\overline{OE}$ to MATCH valid	^tOEM		10		12		15		20		20		25	ns	12
$\overline{OE}$ to MATCH high	^tOEMhi		10		12		15		20		20		25	ns	12
$\overline{WE}$ to MATCH valid	^tWEM		10		12		15		20		20		25	ns	12
$\overline{WE}$ to MATCH high	^tWEMhi		10		12		15		20		20		25	ns	12
Data input to MATCH valid	^tDM		10		12		15		20		20		25	ns	12
MATCH hold from data	^tMHD	5		5		5		5		5		5		ns	12

MATCH TIMING

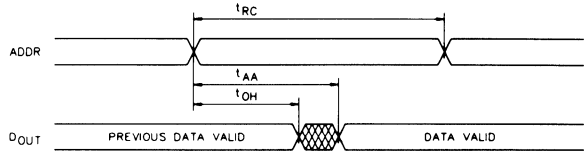


FAST SRAM

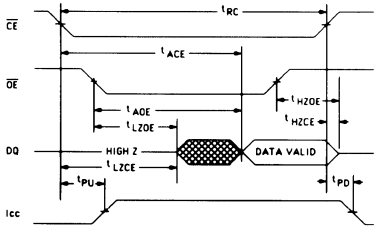
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3.0V for pulse width < 20ns.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. $^{t}HZCE$, $^{t}HZWE$ and $^{t}HZOE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}HZCE$ is less than $^{t}LZCE$.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. Match timing parameters are tested with RL = 200 and CL = 30pF as shown in Fig. 3.

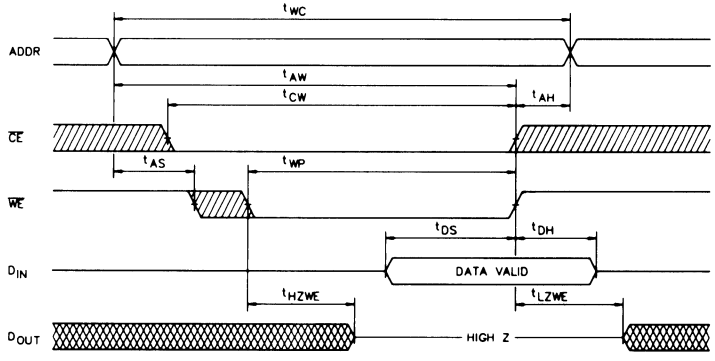
READ CYCLE NO. 1 (8, 9)



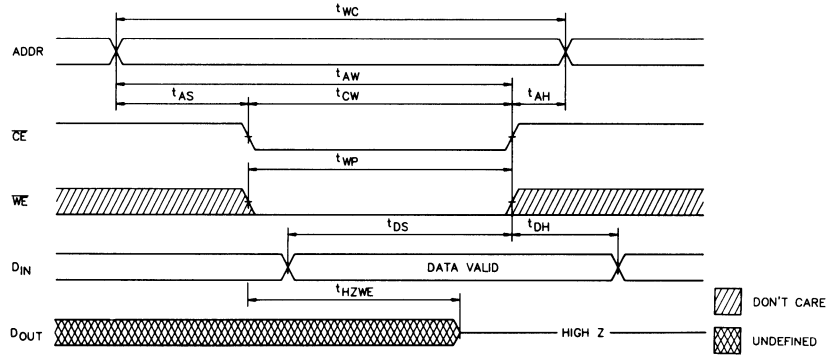
READ CYCLE NO. 2 (7, 8, 10)



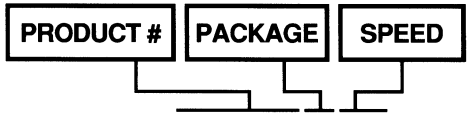
WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ORDER INFORMATION



MT5C6405 DJ-25T
MT5C6405 EC-35T

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SRAM

16K x 4 SRAM

WITH SEPARATE INPUTS AND OUTPUTS

FEATURES

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE1}$, $\overline{CE2}$ and $\overline{OE}$ option
- All inputs and outputs are TTL compatible
- MT5C6406 – output tracks input during WRITE
- MT5C6407 – output high impedance during WRITE

OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

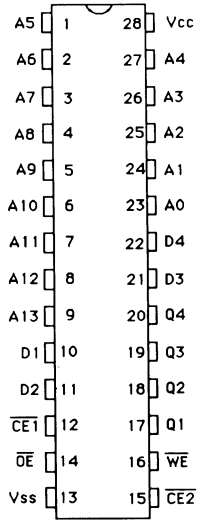
For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 4 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

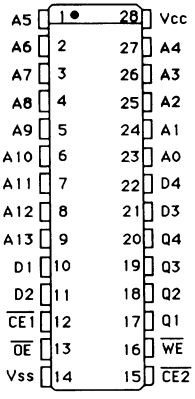
PIN ASSIGNMENT (Top View)

28L/300 DIP



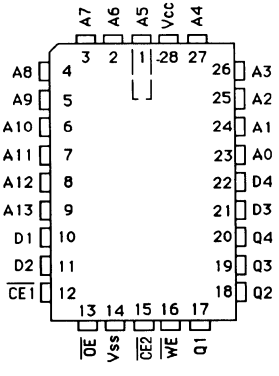
PJ, CH

28L/300 SOJ



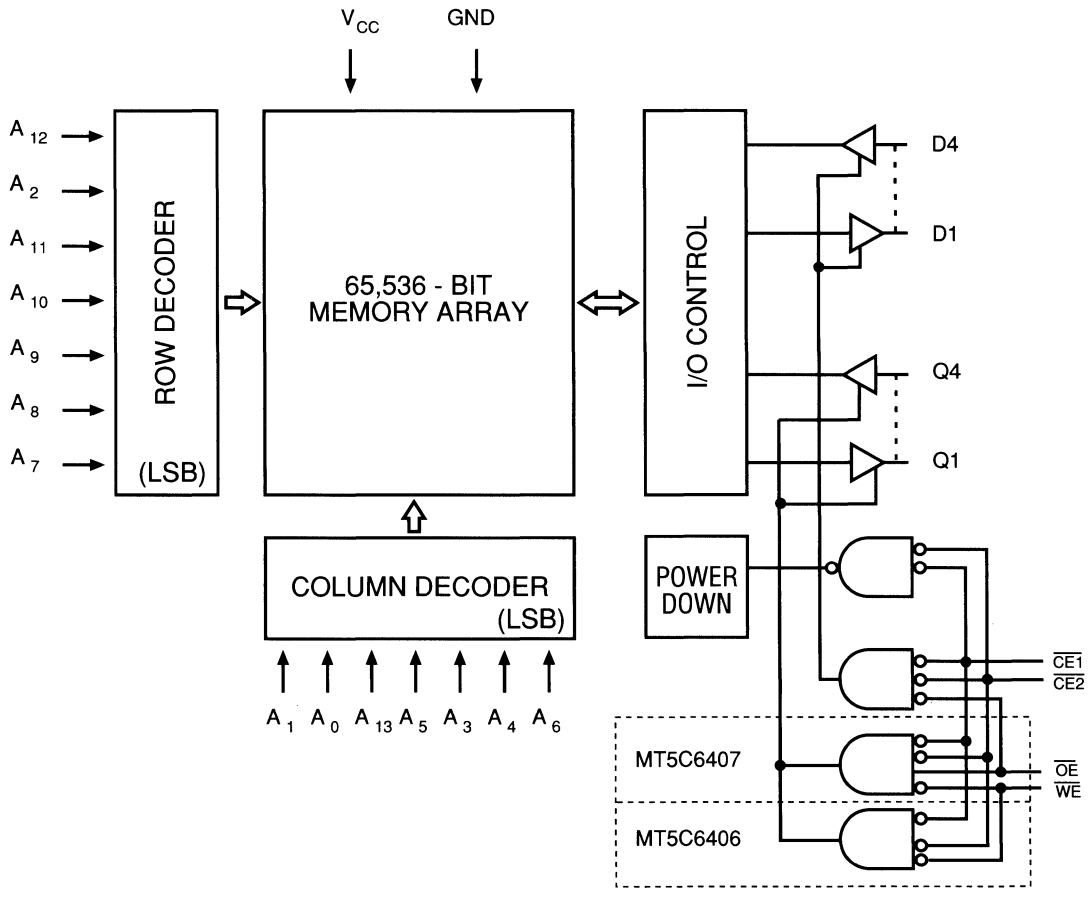
DJC

28L/LCC



ECE

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE1}$	$\overline{CE2}$	$\overline{OE}$	$\overline{WE}$	OUTPUTS	POWER
STANDBY	H	X	X	X	HIGH Z	STANDBY
STANDBY	X	H	X	X	HIGH Z	STANDBY
READ	L	L	L	H	DOUT	ACTIVE
READ	L	L	H	H	HIGH Z	ACTIVE
WRITE (1)	L	L	X	L	HIGH Z	ACTIVE
WRITE (2)	L	L	L	L	DIN	ACTIVE
WRITE (2)	L	L	H	L	HIGH Z	ACTIVE

NOTES: 1. MT5C6407 ONLY
2. MT5C6406 ONLY

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, f = 0 $V_{IH} \ge V_{CC}$ - 0.2	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip enable access time	^tACE		12		15		20		25		30		35	ns	
Output hold from access change	^tOH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power down time	^tPD		12		15		20		25		30		35	ns	
Output enable access time	^tAOE		10		12		15		15		20		20	ns	
Output enable to output in low Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in high Z	^tHZOE		10		10		15		15		20		20	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip enable to end of write	^tCW	10		12		15		20		25		30		ns	
Address valid to end of write	^tAW	12		15		15		20		25		30		ns	
Address set-up time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data set-up time	^tDS	10		10		12		15		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		0		0		ns	
Write enable to output valid	^tAWE		12		15		20		25		30		35	ns	
Data valid to output valid	tADV		12		15		20		25		30		35	ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

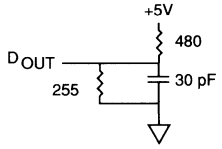


Fig. 1 OUTPUT LOAD EQUIVALENT

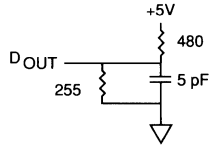


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

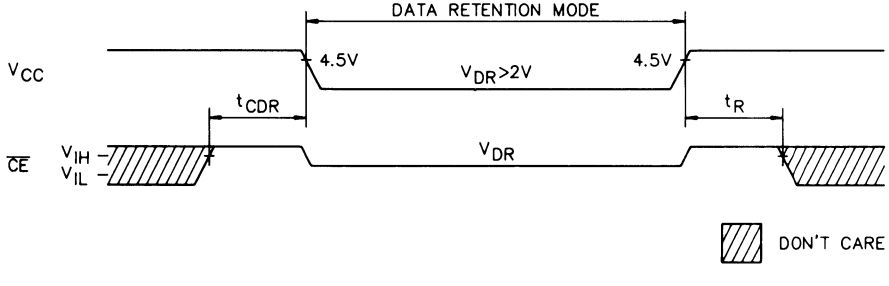
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

FAST SRAM

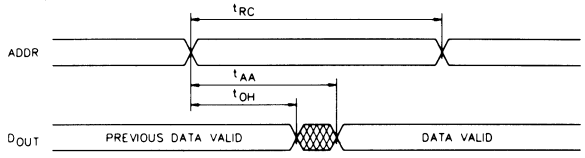
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	Vcc=2v		95	500	µA
			Vcc=3v		350	750	µA
$^{t}CDR^{(4)}$	Chip Deselect to Data Retention Time			0		—	ns
$^{t}R^{(4)}$	Operation Recovery Time			$^{t}RC^{(11)}$			ns

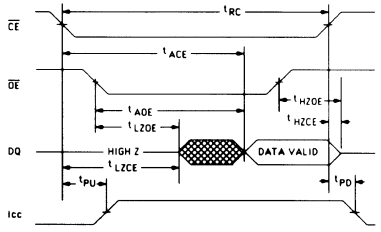
LOW Vcc DATA RETENTION WAVEFORM



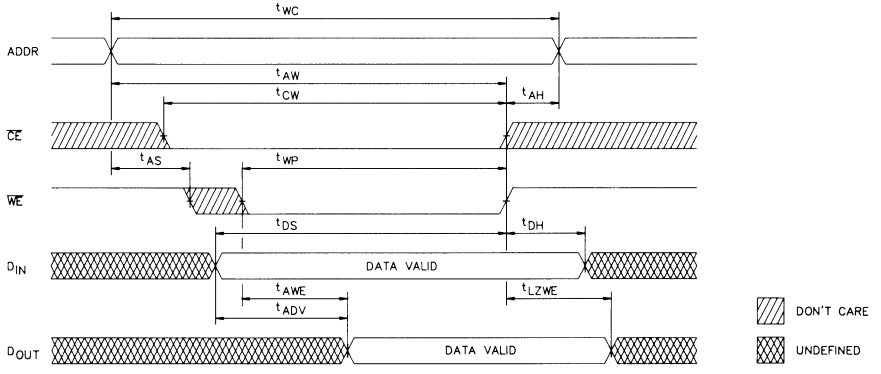
READ CYCLE NO. 1 (8, 9)



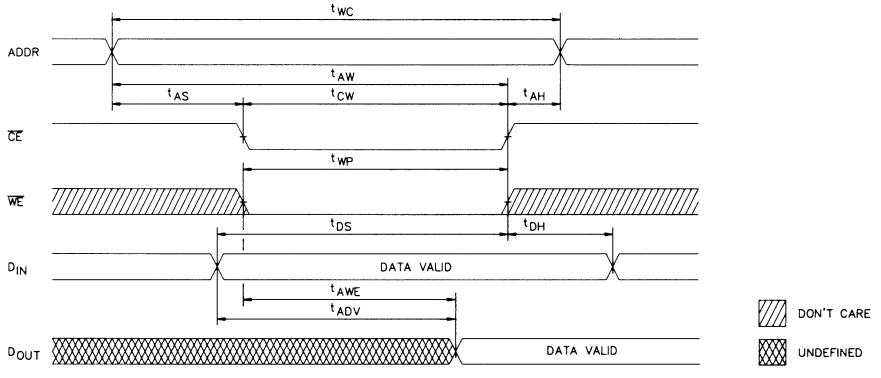
READ CYCLE NO. 2 (7, 8, 10)



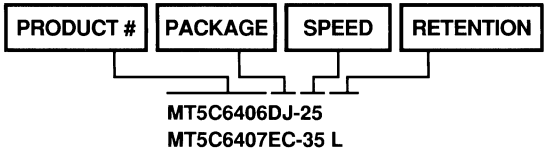
WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

SRAM

32K x 8 SRAM

FEATURES

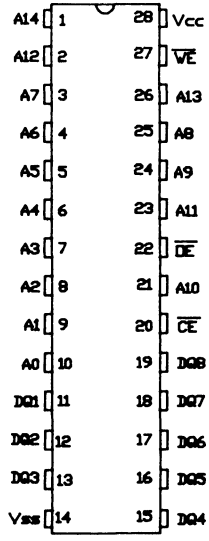
- High speed: 25, 30, 35, 45 and 55ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
55ns access	-55
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
Ceramic DIP (300 mil)	C
Ceramic DIP (600 mil)	CW
Plastic SOJ (300 mil)	DJ
Ceramic LCC (28 pin)	EC
Ceramic LCC (32 pin)	ECW
• Two Volt Data Retention	L

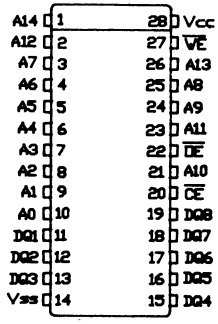
PIN ASSIGNMENT (Top View)

28L/300/600 DIP



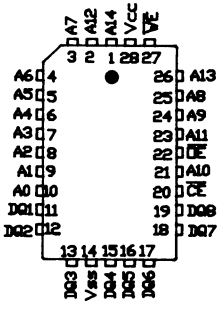
PJ, PK, CH

28L/300 SOJ



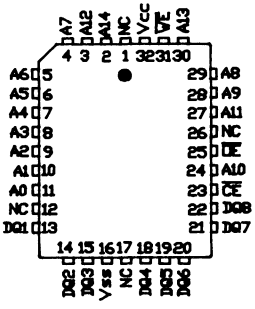
DJC

28L/LCC



ECE

32L/LCC



ECF

GENERAL DESCRIPTION

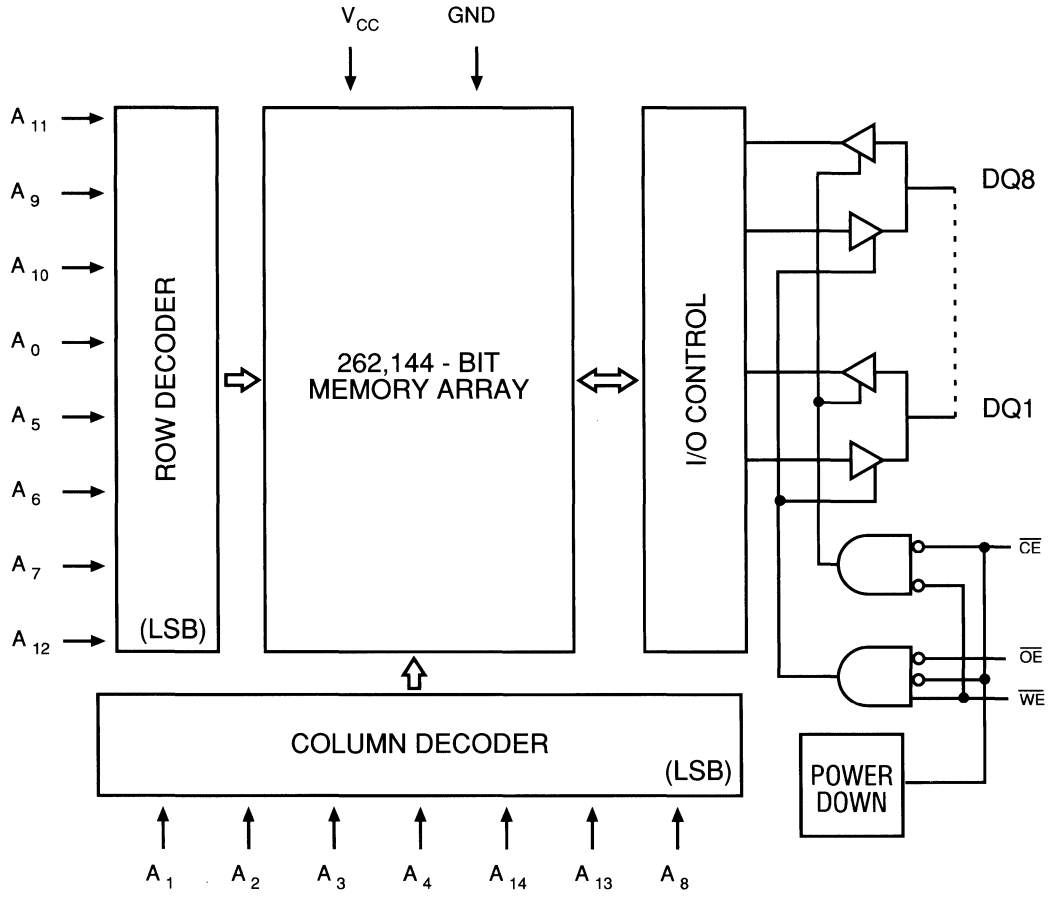
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	DOUT	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}		100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max.	I_{SB1}		40	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}		7	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 4.2mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-25		-30		-35		-45		-55			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	t_{RC}	25		30		35		45		55		ns	
Address access time	t_{AA}		25		30		35		45		55	ns	
Chip enable access time	t_{ACE}		25		30		35		45		55	ns	
Output hold from address change	t_{OH}	5		5		5		5		5		ns	
Chip enable to output in low Z	t_{LZCE}	5		5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		15		20		20		20		20	ns	6, 7
Chip enable to power up time	t_{PU}	0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		25		30		35		45		55	ns	
Output Enable Access Time	t_{AOE}		15		20		20		20		20	ns	
Output Enable to output in low Z	t_{LZOE}	0		0		0		0		0		ns	
Output disable to out put in high Z	t_{HZOE}		15		20		20		20		20	ns	
WRITE Cycle													
WRITE cycle time	t_{WC}	25		30		35		45		55		ns	
Chip enable to end of write	t_{CW}	20		25		30		40		50		ns	
Address Valid to end of write	t_{AW}	20		25		30		40		50		ns	
Address set-up time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	2		2		2		2		2		ns	
Write pulse width	t_{WP}	20		25		25		30		35		ns	
Data set-up time	t_{DS}	15		15		17		20		20		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	0		0		0		0		0		ns	
Write enable to output in high Z	t_{HZWE}	0	15	0	15	0	15	0	20	0	20	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

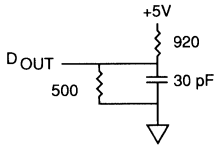


Fig. 1 OUTPUT LOAD EQUIVALENT

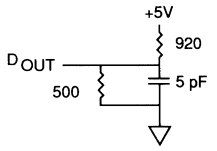


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

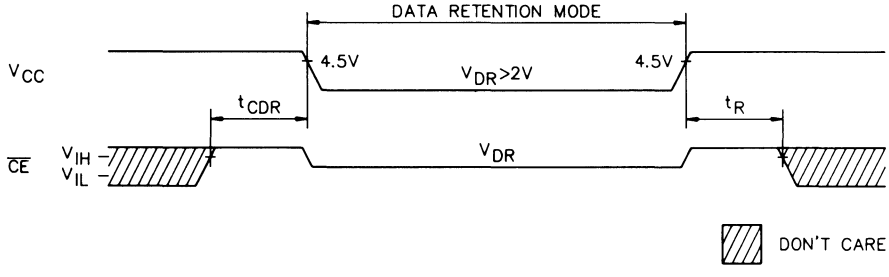
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

FAST SRAM

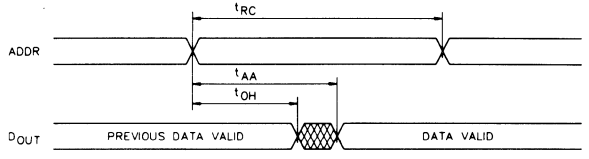
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	Vcc=2v		95	500	µA
			Vcc=3v		350	750	µA
^{t}CDR(4)	Chip Deselect to Data Retention Time			0		—	ns
^{t}R(4)	Operation Recovery Time			^{t}RC(11)			ns

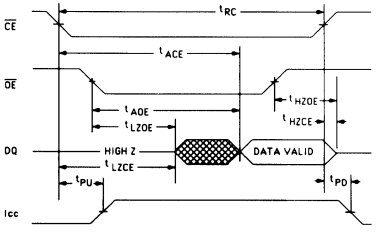
LOW Vcc DATA RETENTION WAVEFORM



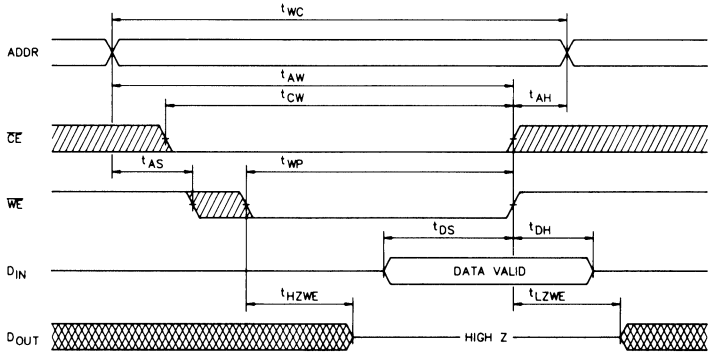
READ CYCLE NO. 1 (8, 9)



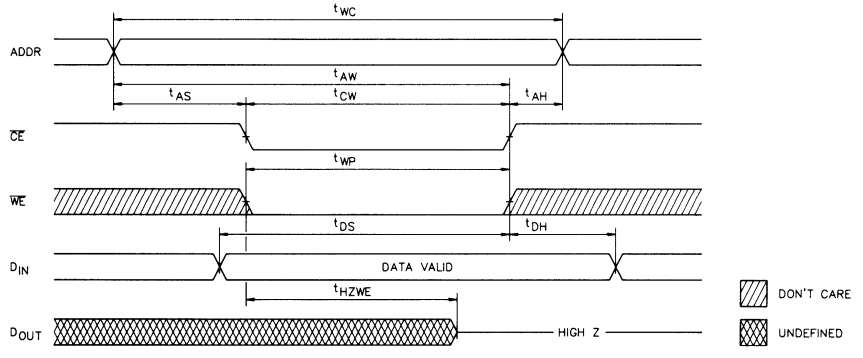
READ CYCLE NO. 2 (7, 8, 10)



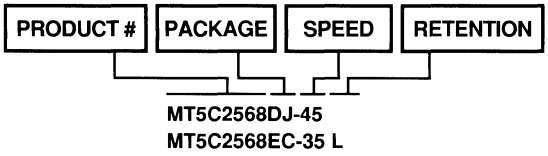
WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

SRAM 64K x 1 SRAM

FEATURES

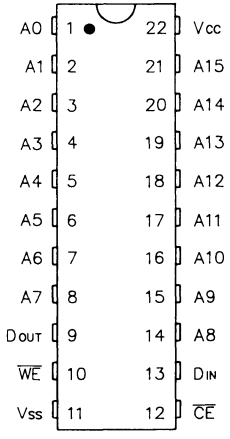
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

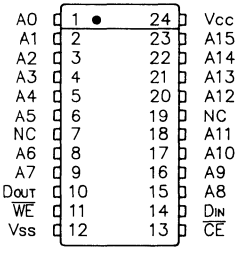
PIN ASSIGNMENT (Top View)

22L/300 DIP



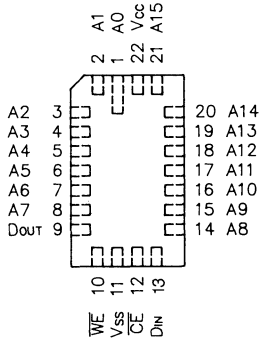
PF, CE

24L/300 SOJ



DJB

22L/LCC



ECD

GENERAL DESCRIPTION

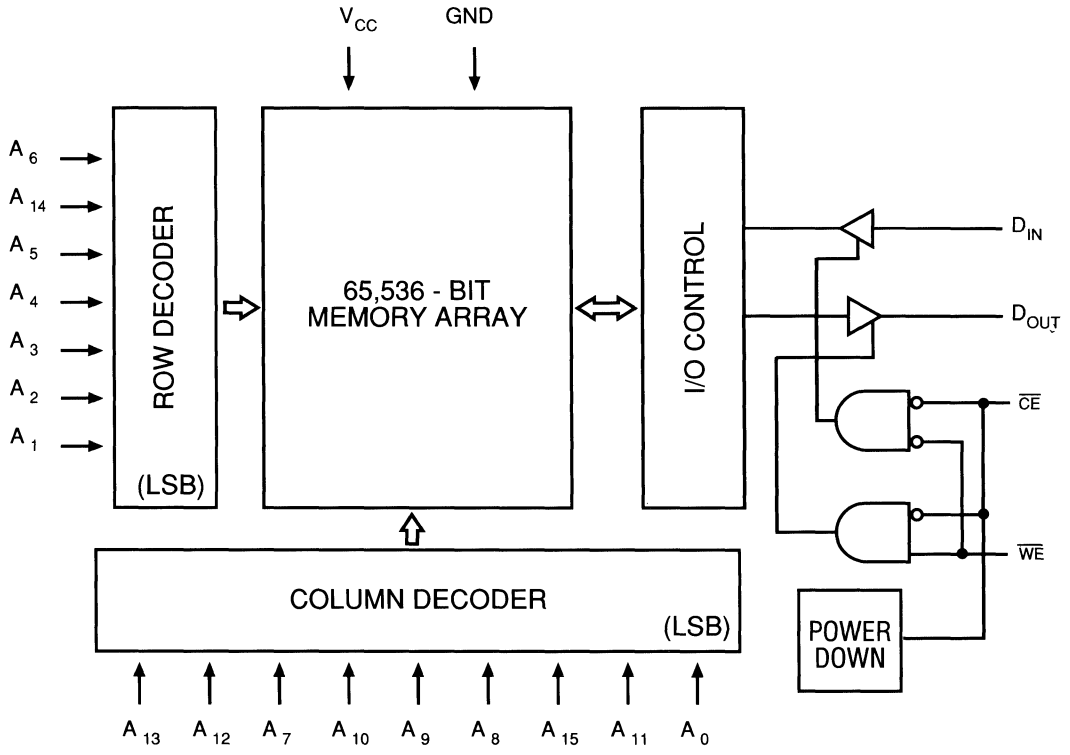
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	DOUT	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, f = 0 $V_{IH} \ge V_{CC}$ - 0.2	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip enable access time	^tACE		12		15		20		25		30		35	ns	
Output hold from access change	^tOH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		10		10		15		15		20		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power down time	^tPD		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip enable to end of write	^tCW	10		12		15		20		25		30		ns	
Address valid to end of write	^tAW	12		15		15		20		25		30		ns	
Address set-up time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data set-up time	^tDS	10		10		12		15		15		17		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	10	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

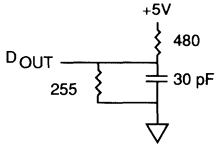


Fig. 1 OUTPUT LOAD EQUIVALENT

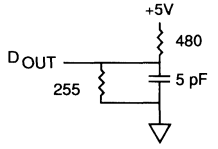


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

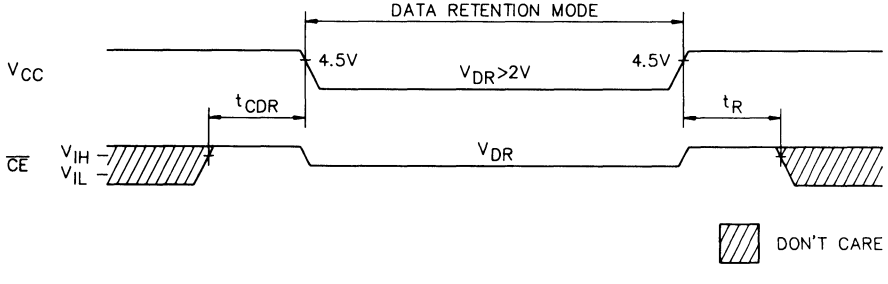
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{T}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

FAST SRAM

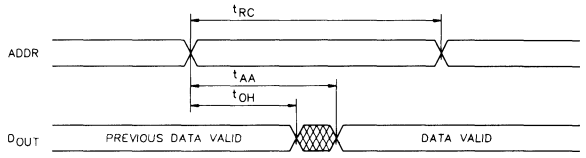
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	Vcc=2v	—	95	500	µA
			Vcc=3v	—	350	750	µA
$^{t}CDR^{(4)}$	Chip Deselect to Data Retention Time			0		—	ns
$^{t}R^{(4)}$	Operation Recovery Time			$^{t}RC^{(11)}$			ns

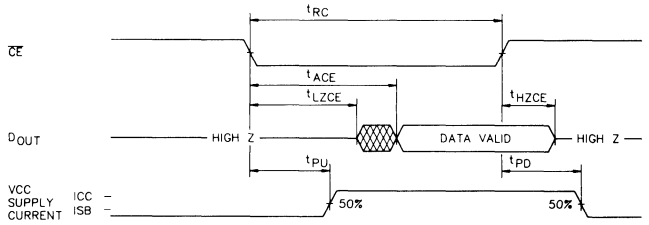
LOW Vcc DATA RETENTION WAVEFORM



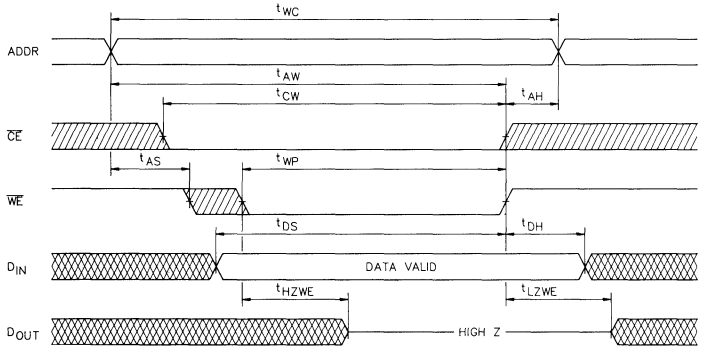
READ CYCLE NO. 1 (8, 9)



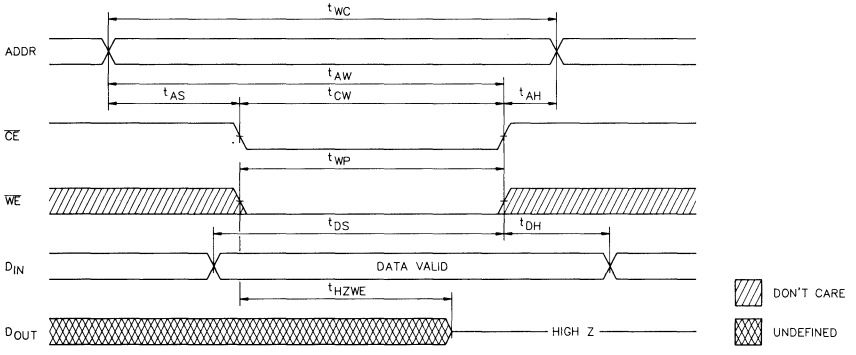
READ CYCLE NO. 2 (7, 8, 10)



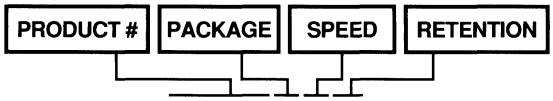
WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ORDER INFORMATION



MT5C6401DJ-25
MT5C6401EC-35 L

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Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

SRAM 64K x 4 SRAM

FEATURES

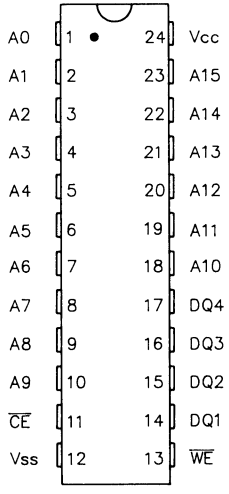
- High speed: 25, 30, 35, 45 and 55ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
55ns access	-55
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

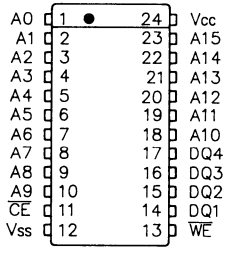
PIN ASSIGNMENT (Top View)

24L/300 DIP



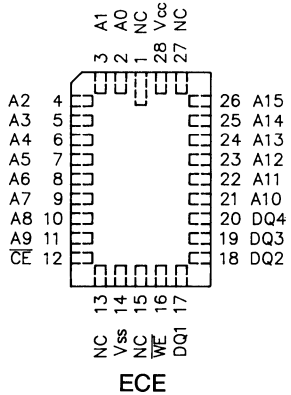
PG, CF

24L/300 SOJ



DJB

28L/LCC



ECE

GENERAL DESCRIPTION

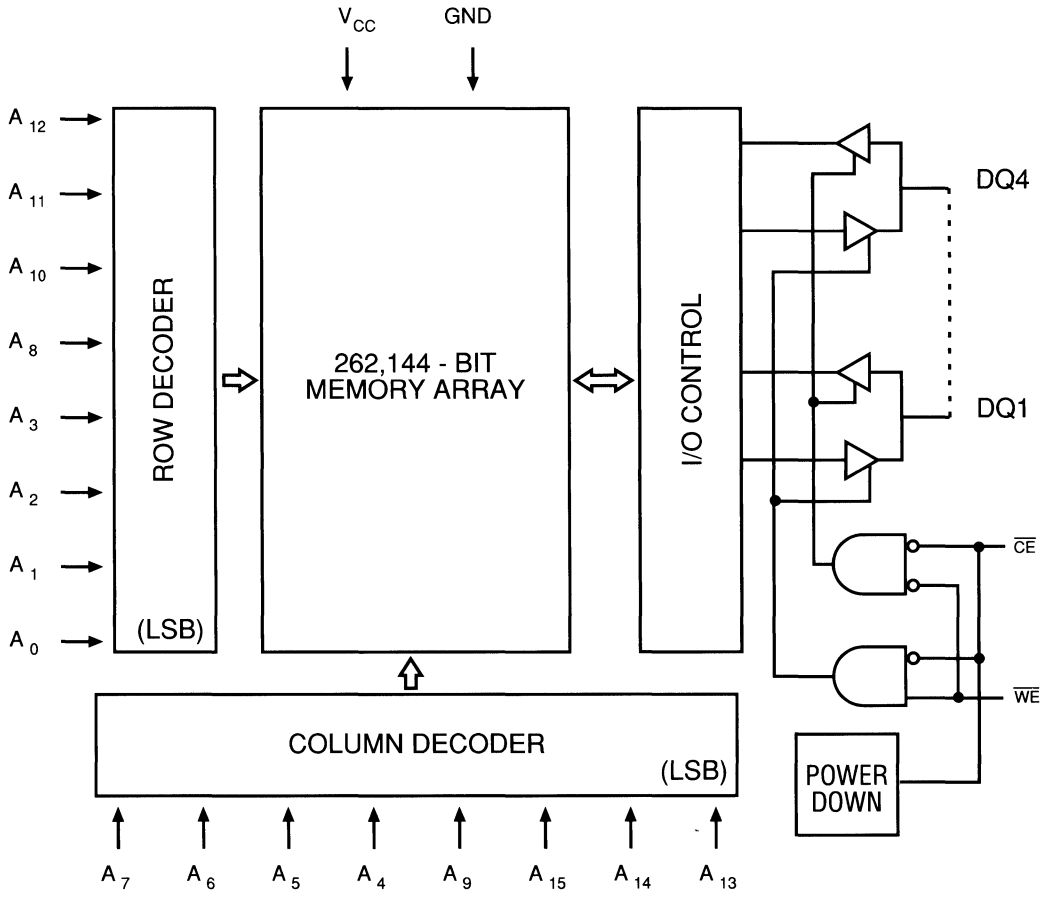
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	DOUT	ACTIVE
WRITE	L	L	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}		100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max.	I_{SB1}		40	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}		7	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-25		-30		-35		-45		-55			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	t_{RC}	25		30		35		45		55		ns	
Address access time	t_{AA}		25		30		35		45		55	ns	
Chip enable access time	t_{ACE}		25		30		35		45		55	ns	
Output hold from address change	t_{OH}	5		5		5		5		5		ns	
Chip enable to output in low Z	t_{LZCE}	5		5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		15		20		20		20		20	ns	6, 7
Chip enable to power up time	t_{PU}	0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		25		30		35		45		55	ns	
WRITE Cycle													
WRITE cycle time	t_{WC}	25		30		35		45		55		ns	
Chip enable to end of write	t_{CW}	20		25		30		40		50		ns	
Address Valid to end of write	t_{AW}	20		25		30		40		50		ns	
Address set-up time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	2		2		2		2		2		ns	
Write pulse width	t_{WP}	20		25		25		30		35		ns	
Data set-up time	t_{DS}	15		15		17		20		20		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	0		0		0		0		0		ns	
Write enable to output in high Z	t_{HZWE}	0	15	0	15	0	15	0	20	0	20	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

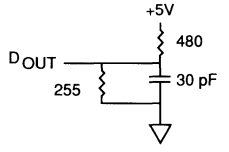


Fig. 1 OUTPUT LOAD EQUIVALENT

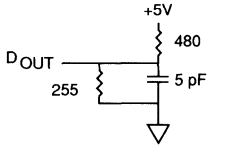


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

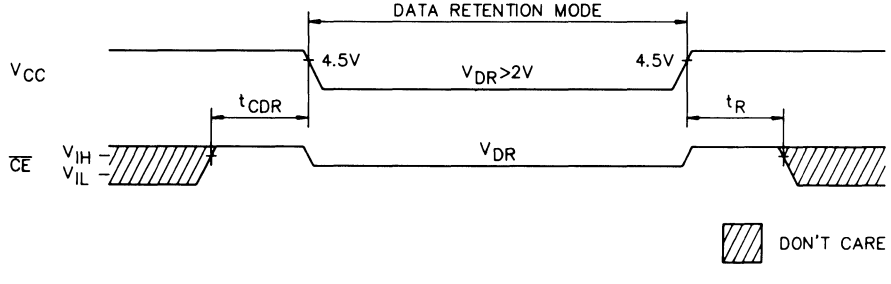
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

FAST SRAM

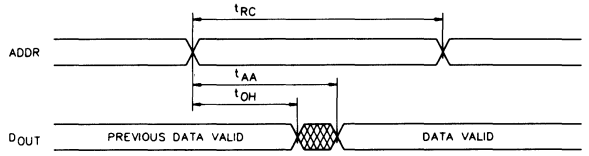
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v		95	500	µA
			Vcc=3v		350	750	µA
^{t}CDR(4)	Chip Deselect to Data Retention Time			0		—	ns
^{t}R(4)	Operation Recovery Time			^{t}RC(11)			ns

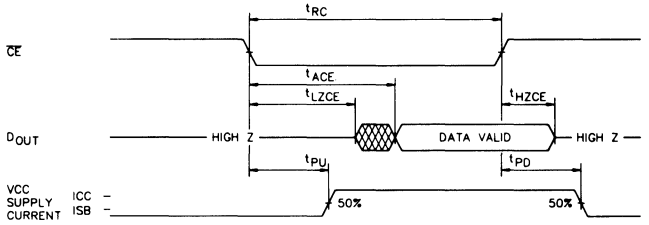
LOW Vcc DATA RETENTION WAVEFORM



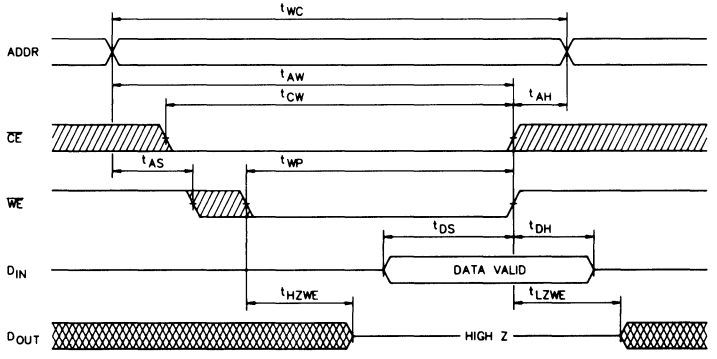
READ CYCLE NO. 1 (8, 9)



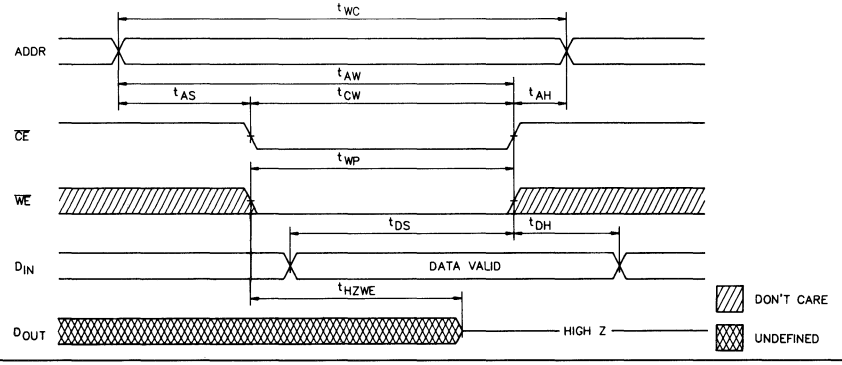
READ CYCLE NO. 2 (7, 8, 10)



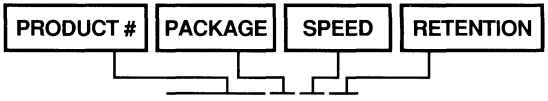
WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ORDER INFORMATION



MT5C2564DJ-45
MT5C2564EC-35 L

The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

SRAM

64K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

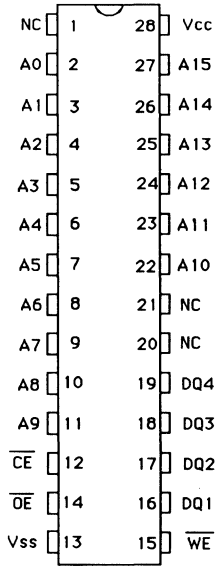
- High speed: 25, 30, 35, 45 and 55ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS / MARKING

• Timing	
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
55ns access	-55
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

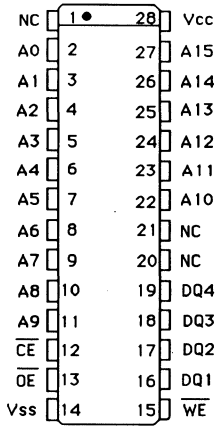
PIN ASSIGNMENT (Top View)

28L/300 DIP



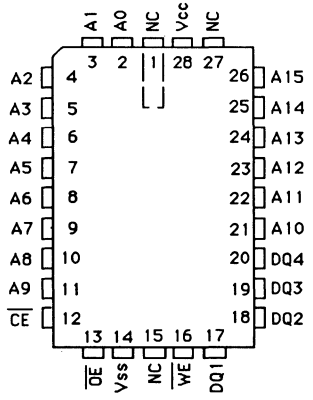
PJ, CH

28L/300 SOJ



DJC

28L/LCC



CH

GENERAL DESCRIPTION

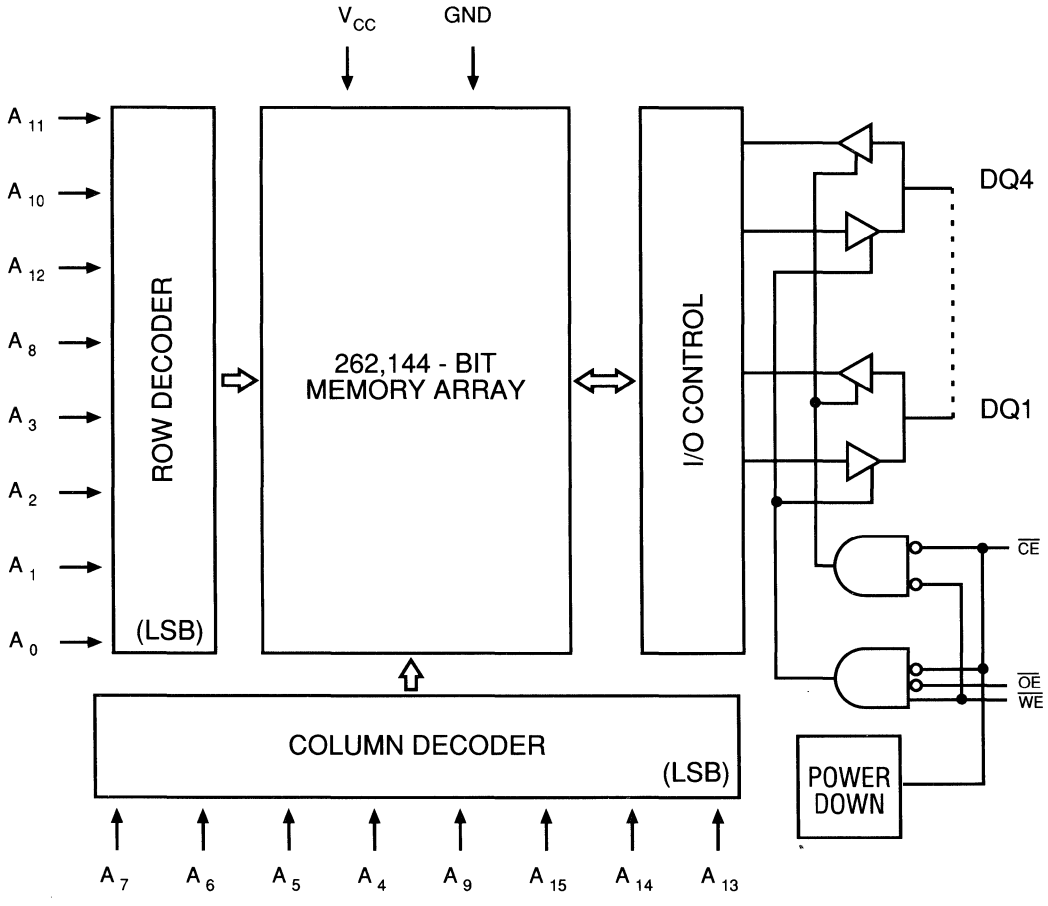
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	DOUT	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}		100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max.	I_{SB1}		40	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}		7	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz V_{CC} = 5V	C_I		8	pF	4
Output Capacitance		C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-25		-30		-35		-45		-55			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	t_{RC}	25		30		35		45		55		ns	
Address access time	t_{AA}		25		30		35		45		55	ns	
Chip enable access time	t_{ACE}		25		30		35		45		55	ns	
Output hold from address change	t_{OH}	5		5		5		5		5		ns	
Chip enable to output in low Z	t_{LZCE}	5		5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		15		20		20		20		20	ns	6, 7
Chip enable to power up time	t_{PU}	0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		25		30		35		45		55	ns	
Output Enable Access Time	t_{AOE}		15		20		20		20		20	ns	
Output Enable to output in low Z	t_{LZOE}	0		0		0		0		0		ns	
Output disable to output in high Z	t_{HZOE}		15		20		20		20		20	ns	6
WRITE Cycle													
WRITE cycle time	t_{WC}	25		30		35		45		55		ns	
Chip enable to end of write	t_{CW}	20		25		30		40		50		ns	
Address Valid to end of write	t_{AW}	20		25		30		40		50		ns	
Address set-up time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	2		2		2		2		2		ns	
Write pulse width	t_{WP}	20		25		25		30		35		ns	
Data set-up time	t_{DS}	15		15		17		20		20		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	0		0		0		0		0		ns	
Write enable to output in high Z	t_{HZWE}	0	15	0	15	0	15	0	20	0	20	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

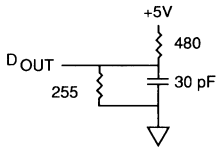


Fig. 1 OUTPUT LOAD EQUIVALENT

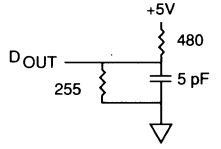


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

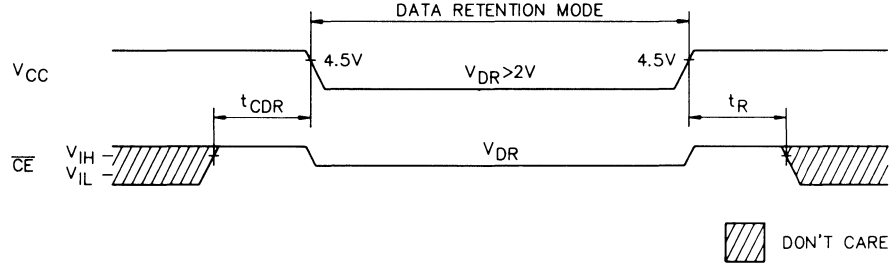
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

FAST SRAM

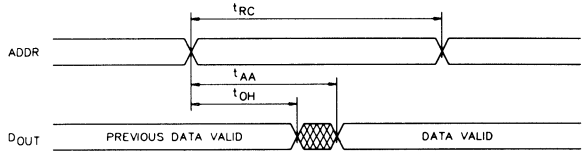
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	Vcc=2v		95	500	µA
			Vcc=3v		350	750	µA
$^{t}CDR^{(4)}$	Chip Deselect to Data Retention Time			0		—	ns
$^{t}R^{(4)}$	Operation Recovery Time			$^{t}RC^{(11)}$			ns

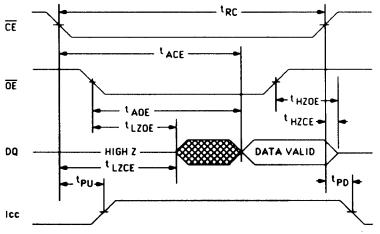
LOW Vcc DATA RETENTION WAVEFORM



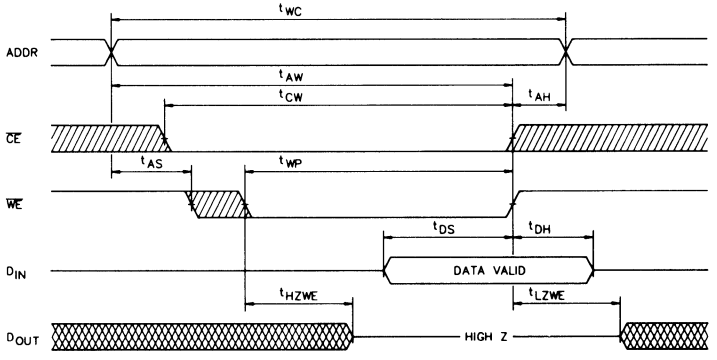
READ CYCLE NO. 1 (8, 9)



READ CYCLE NO. 2 (7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



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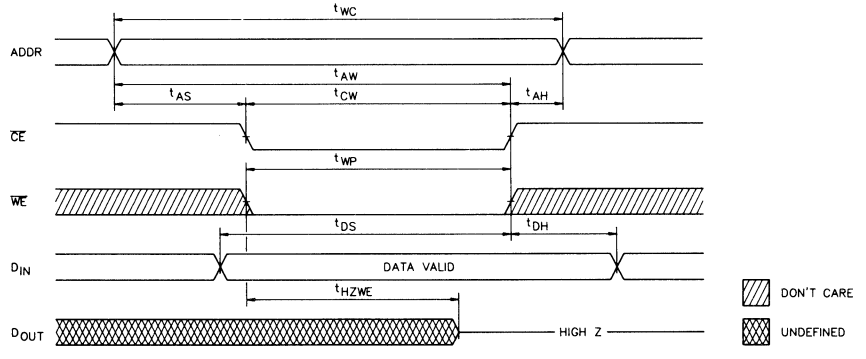
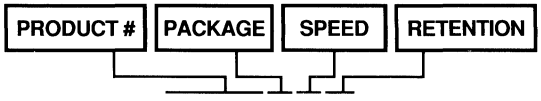
(Chip Enable Controlled)



ORDER INFORMATION



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Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

SRAM

128K x 8 SRAM

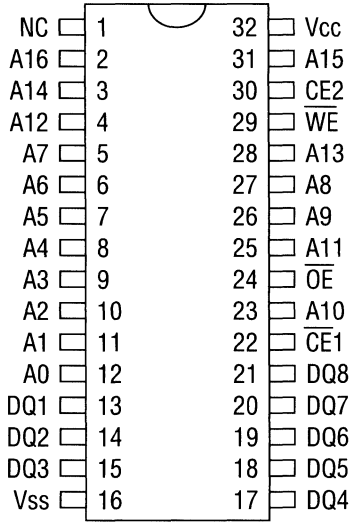
FEATURES

- High speed: 25, 35 and 45ns
- Automatic chip enable power down
- All inputs and outputs are TTL compatible
- High performance, low power, CMOS process
- Single +5V (±10%) power supply
- Low power, ICC (max.) 70mA

OPTIONS

	MARKING
• Timing	
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP	None
Ceramic DIP	C
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)



GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. Output Enable ($\overline{OE}$) is an enhancement available for all common I/O organizations. This enhancement can place the output in a high impedance state for additional flexibility in system design. The x 1 organization features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. When the $\overline{OE}$ option is present, it must also be LOW to read the device. The devices offer a reduced power standby mode when disabled. This allows system designs for low power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

SRAM 256K x 1 SRAM

FEATURES

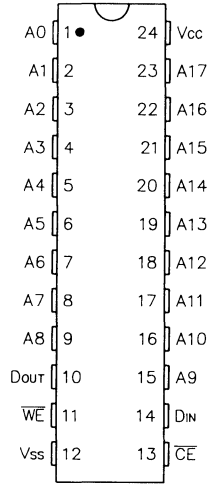
- High speed: 25, 30, 35, 45 and 55ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
55ns access	-55
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

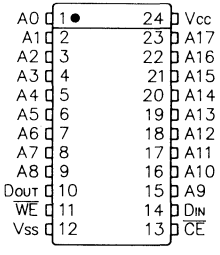
PIN ASSIGNMENT (Top View)

24L/300 DIP



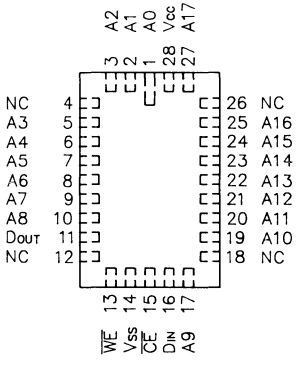
PG, CF

24L/300 SOJ



DJB

28L/LCC



ECE

GENERAL DESCRIPTION

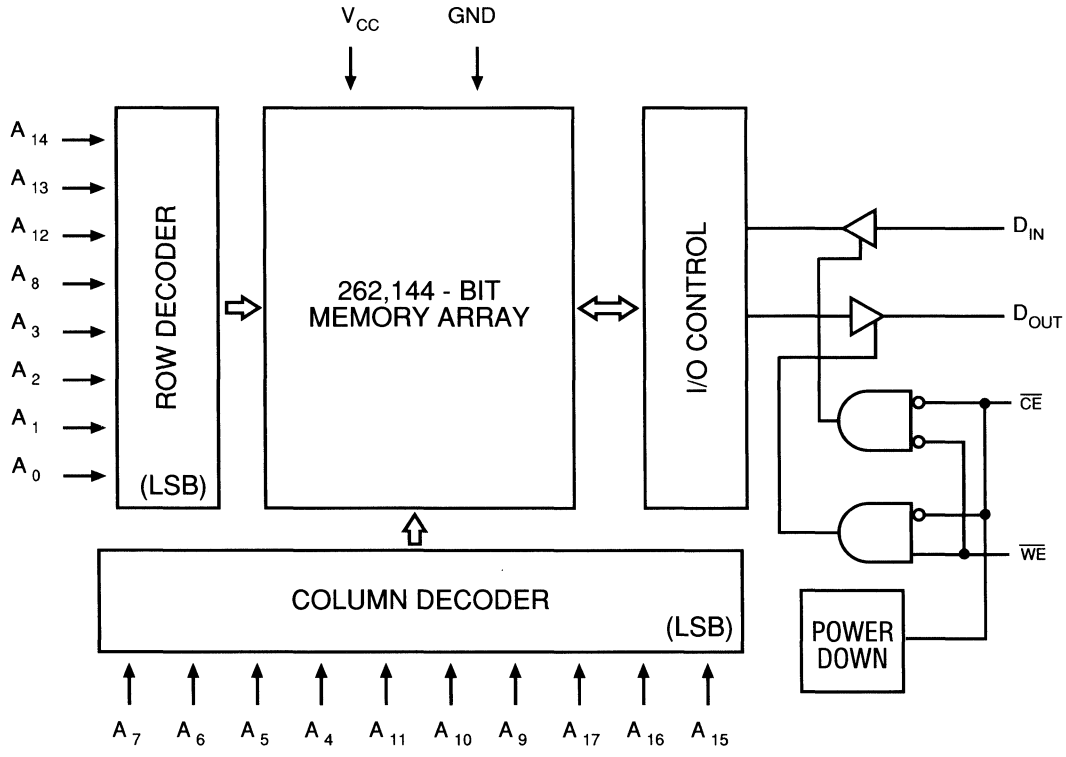
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	DOUT	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}		100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max.	I_{SB1}		40	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}		10	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-25		-30		-35		-45		-55			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	t_{RC}	25		30		35		45		55		ns	
Address access time	t_{AA}		25		30		35		45		55	ns	
Chip enable access time	t_{ACE}		25		30		35		45		55	ns	
Output hold from address change	t_{OH}	5		5		5		5		5		ns	
Chip enable to output in low Z	t_{LZCE}	5		5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		15		20		20		20		20	ns	6, 7
Chip enable to power up time	t_{PU}	0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		25		30		35		45		55	ns	
WRITE Cycle													
WRITE cycle time	t_{WC}	25		30		35		45		55		ns	
Chip enable to end of write	t_{CW}	20		25		30		40		50		ns	
Address Valid to end of write	t_{AW}	20		25		30		40		50		ns	
Address set-up time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	2		2		2		2		2		ns	
Write pulse width	t_{WP}	20		25		25		30		35		ns	
Data set-up time	t_{DS}	15		15		17		20		20		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	0		0		0		0		0		ns	
Write enable to output in high Z	t_{HZWE}	0	15	0	15	0	15	0	20	0	20	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

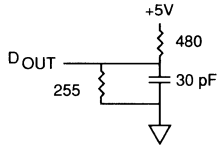


Fig. 1 OUTPUT LOAD EQUIVALENT

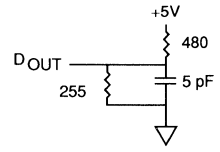


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

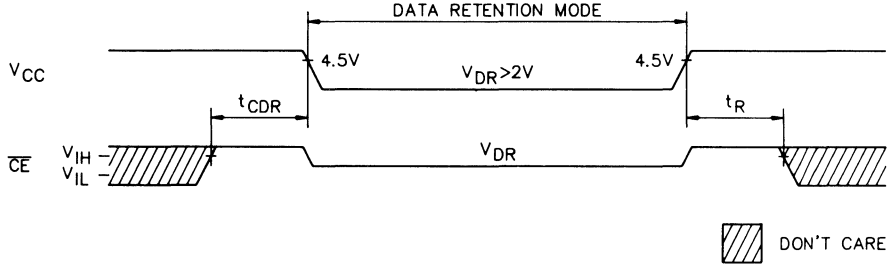
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. at Vcc = 2V.
12. at Vcc = 3V.
13. ^{t}RC = Read Cycle Time. (Page 4)

FAST SRAM

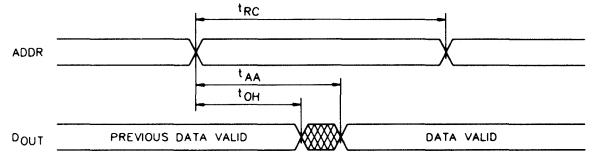
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data		2	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$	95 350	500(11) 750(12)	µA µA
^{t}CDR(4)	Chip Deselect to Data Retention Time		0	—	ns
^{t}R(4)	Operation Recovery Time		^{t}RC(13)		ns

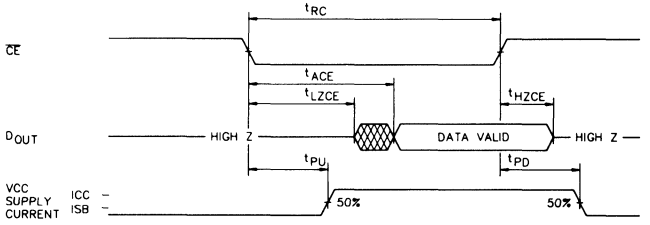
LOW Vcc DATA RETENTION WAVEFORM



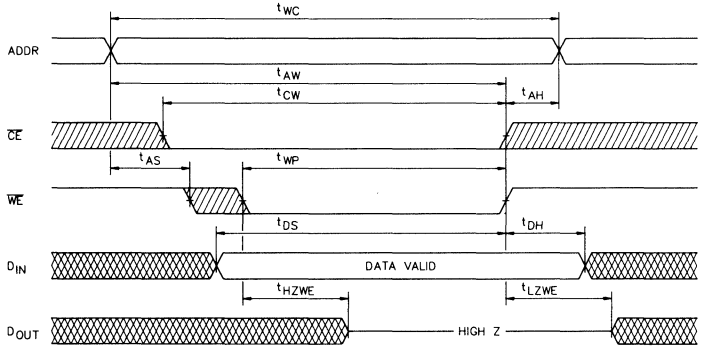
READ CYCLE NO. 1 (8, 9)



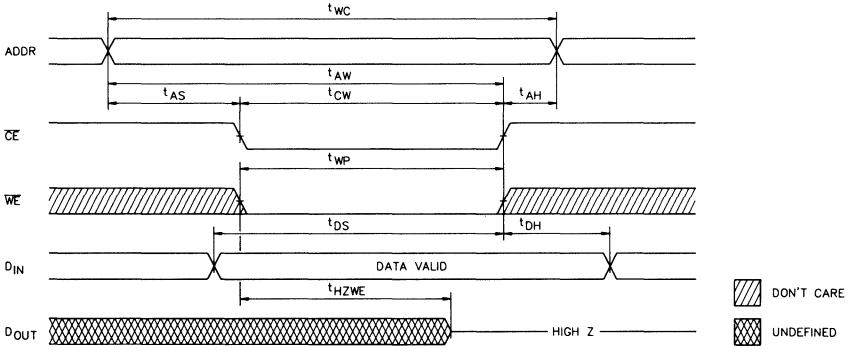
READ CYCLE NO. 2 (7, 8, 10)



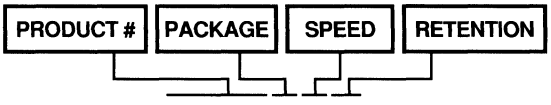
WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ORDER INFORMATION



MT5C2561DJ-45
MT5C2561EC-35 L

The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

SRAM

256K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

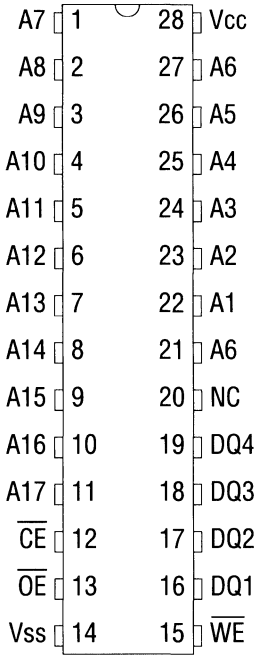
- High speed: 25, 35 and 45ns
- Automatic chip enable power down
- All inputs and outputs are TTL compatible
- High performance, low power, CMOS process
- Single +5V (±10%) power supply
- Low power, ICC (max.) 70mA

OPTIONS

	MARKING
• Timing	
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP	None
Ceramic DIP	C
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

28L DIP



GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. Output Enable ($\overline{OE}$) is an enhancement available for all common I/O organizations. This enhancement can place the output in a high impedance state for additional flexibility in system design. The x 1 organization features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. When the $\overline{OE}$ option is present, it must also be LOW to read the device. The devices offer a reduced power standby mode when disabled. This allows system designs for low power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

SRAM 1MEG x 1 SRAM

FEATURES

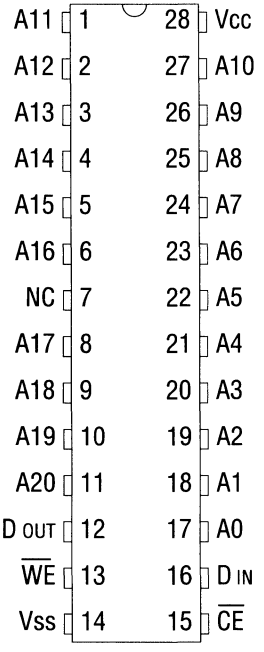
- High speed: 25, 35 and 45ns
- Automatic chip enable power down
- All inputs and outputs are TTL compatible
- High performance, low power, CMOS process
- Single +5V (±10%) power supply
- Low power, ICC (max.) 70mA

OPTIONS MARKING

• Timing	
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP	None
Ceramic DIP	C
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

28L DIP



GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

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All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

CACHE DATA STATIC RAMS

CACHE DATA RAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package	Process	Page
Dual 4K x 16/18 or Single 8K x16/18	Mode, Byte Select CE, OE, Address Latch	MT56C0416	25, 35, 45	52-Pin PLCC	CMOS	5-1

CACHE DATA STATIC RAMS

DUAL 4K x 16/18 SRAM, SINGLE 8K x 16/18

CONFIGURABLE CACHE DATA RAM

FEATURES

- Operates as two 4K x 16/18 SRAMs with common addresses, common data and separate control signals.
- Configurable as a single 8K x 16/18 SRAM with MODE input.
- Two parity bit utilization when operated in x 18 mode.
- Built-in address input latches.
- Separate byte selects.
- Fast access times: 25ns, 35ns and 45ns.
- Upper and lower byte selects.
- Fast output enable: 8ns.
- Compatible with the Intel 82385 cache memory controller.

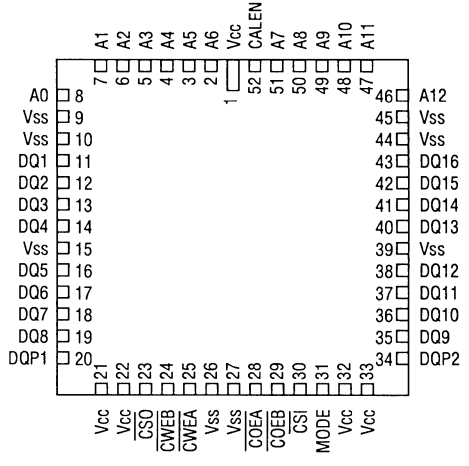
OPTIONS MARKING

- Timing

25ns access	-25
35ns access	-35
45ns access	-45

PIN ASSIGNMENT (Top View)

52-Pin PLCC



GENERAL DESCRIPTION

The MT56C0416 is one of a family of fast SRAM cache memories. It employs a high speed, low power design using a 4-transistor memory cell. It is fabricated using double layer metal, double layer polysilicon CMOS technology.

The MT56C0416 is designed to be a cache data memory cell building block. It easily interfaces with the Intel 82385 cache controller in either the direct mapped or two-way set associative mode. A mode control pin determines the configuration of the memory. When this pin is held low, the device functions as an 8K by 16 or 18 bit SRAM. When the mode pin is high, the device is configured as a dual 4K by 16 or 18 bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are contolled by the output enable, write enable and chip select signals. Outputs of the "A" bank SRAM are enabled when the $\overline{COEA}$ pin makes a high to low level transition. Outputs of the "B" bank SRAM are enabled when the $\overline{COEB}$ pin makes a high to low transistion.

Write enables are also activated on the high to low transitions. $\overline{CWEA}$ allows data to be written in the "A" bank and $\overline{CWEB}$ causes data to be written in the "B" bank. $\overline{CS0}$ and $\overline{CS1}$ determine the byte selection. $\overline{CS0}$ controls the lower byte and $\overline{CS1}$ controls the upper byte.

Micron applies the highest level of design and process technology in all their Static RAM products. With a full line of 256K density SRAM's at access times of 25 nanoseconds, Micron has firmly established itself as the leading fast SRAM supplier. So, for your fastest memory requirements, come to the fast memory supplier. . .
Micron.

FIFO PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package & Number of Pins				Page
				PDIP	CDIP	LCC	PLCC	
512 x 8	MB, VF	MT52C8006	25, 30, 35	28	28	-	-	6-3
512 x 9	E	MT52C9005	25, 30, 35	28	28	32	32	6-5
512 x 9	MB	MT52C9006	25, 30, 35	28	28	32	32	6-7
512 x 9	VF	MT52C9007	25, 30, 35	28	28	32	32	6-9
512 x 16	E, MB, VF	MT52C1605	25, 30, 35	48	48	-	-	6-11
512 x 16/8	E, MB, VF	MT52C1607	25, 30, 35	40	40	-	-	6-13
1K x 8	MB, VF	MT52C8011	25, 30, 35	28	28	-	-	6-15
1K x 9	E	MT52C9010	25, 30, 35	28	28	32	32	6-17
1K x 9	MB	MT52C9011	25, 30, 35	28	28	32	32	6-19
1K x 9	VF	MT52C9012	25, 30, 35	28	28	32	32	6-21
1K x 16	E, MB, VF	MT52C1610	25, 30, 35	48	48	-	-	6-23
1K x 16/8	E, MB, VF	MT52C1612	25, 30, 35	40	40	-	-	6-25
2K x 8	MB, VF	MT52C8021	25, 30, 35	28	28	-	-	6-27
2K x 9	E	MT52C9020	25, 30, 35	28	28	32	32	6-29
2K x 9	MB	MT52C9021	25, 30, 35	28	28	32	32	6-31
2K x 9	VF	MT52C9022	25, 30, 35	28	28	32	32	6-33
2K x 16	E, MB, VF	MT52C1620	25, 30, 35	48	48	-	-	6-35
2K x 16/8	E, MB, VF	MT52C1622	25, 30, 35	40	40	-	-	6-37
4K x 8	MB, VF	MT52C8041	25, 30, 35	28	28	-	-	6-39
4K x 9	E	MT52C9040	25, 30, 35	28	28	32	32	6-41
4K x 9	MB	MT52C9041	25, 30, 35	28	28	32	32	6-43
4K x 9	VF	MT52C9042	25, 30, 35	28	28	32	32	6-45

MB . . . . . Mailbox Register
VF . . . . . Variable Flags
E . . Depth and Width Expandable

FIFO

512 x 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

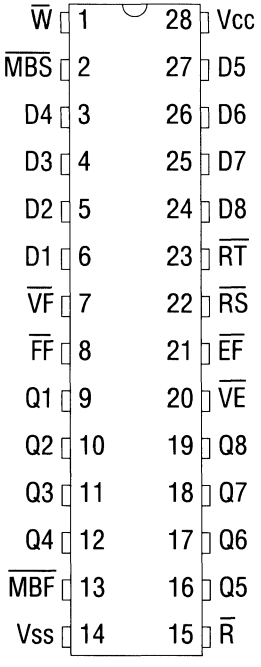
- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

28L DIP



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

There are three types of FIFO's in the Micron family: Expandable, Mailbox Register, and Variable Flags. Expandable FIFO's are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFO's have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFO's allow the user to program the level of the full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO 512 x 9 FIFO

FEATURES

- High speed: 25ns access, 35ns cycle time
- Industry standard pin-out
- Empty and Full warning flags
- Asynchronous READ and WRITE
- Depth and Width expansion capability
- Automatic retransmit
- Low power consumption
- Transistor loads for maximum data integrity

OPTIONS MARKING

- Timing

25ns access time	-25
30ns access time	-30
35ns access time	-35

- Packages

Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

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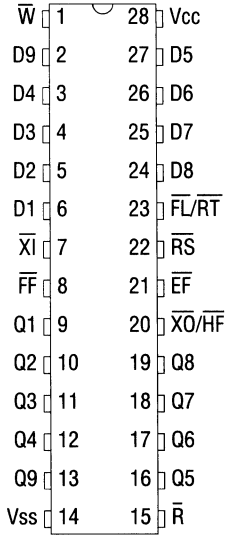
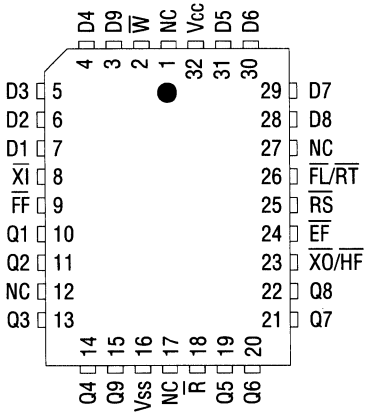
All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



FIFO

FIFO

512 x 9 FIFO

MAILBOX REGISTER

FEATURES

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS — MARKING

- Timing

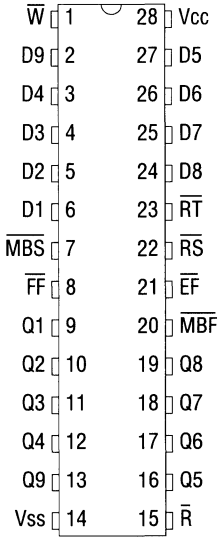
25ns access time	-25
30ns access time	-30
35ns access time	-35

- Packages

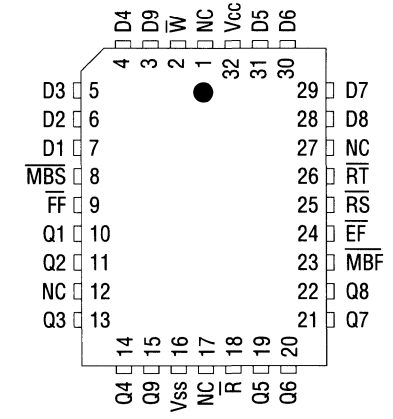
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

There are three types of FIFO's in the Micron family: Expandable, Mailbox Register, and Variable Flags. Expandable FIFO's are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFO's have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFO's allow the user to program the level of the full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

512 x 9 FIFO

VARIABLE FLAGS

FEATURES

- High speed: 25ns access, 35ns cycle time
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS — MARKING

- Timing

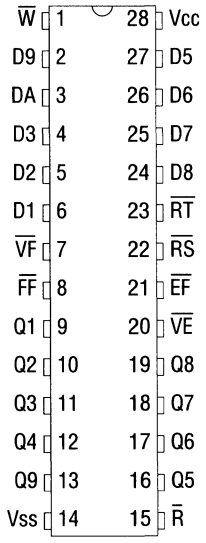
25ns access time	-25
30ns access time	-30
35ns access time	-35

- Packages

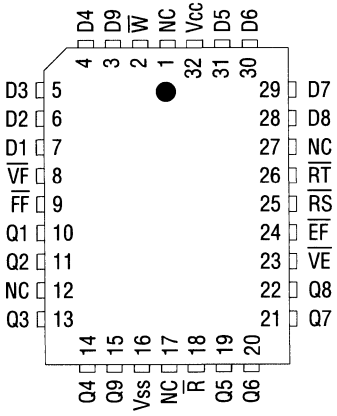
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

There are three types of FIFO's in the Micron family: Expandable, Mailbox Register, and Variable Flags. Expandable FIFO's are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFO's have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFO's allow the user to program the level of the full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

512 x 16 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

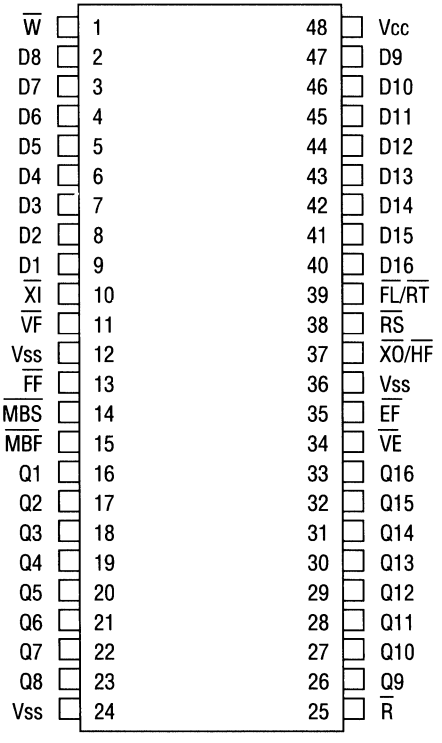
- High speed: 25ns access, 35ns cycle time
- 16-bit word width
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Easy expansion capability
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS

OPTIONS	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

48L DIP



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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

512 x 16 to 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

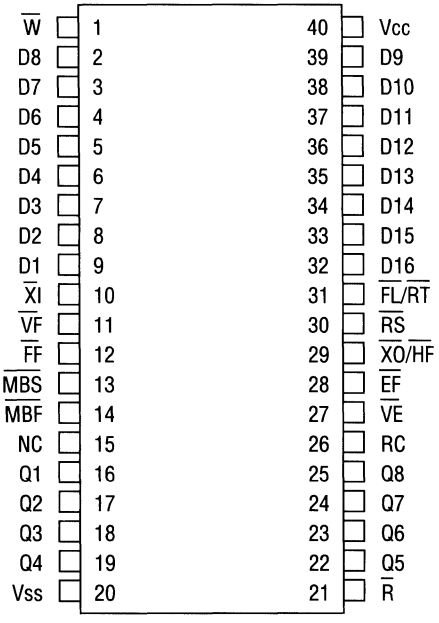
- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE.
- Easy expansion capability
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity
- One chip interface between a 16 bit bus and an 8 bit bus

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

40L DIP



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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

1K x 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

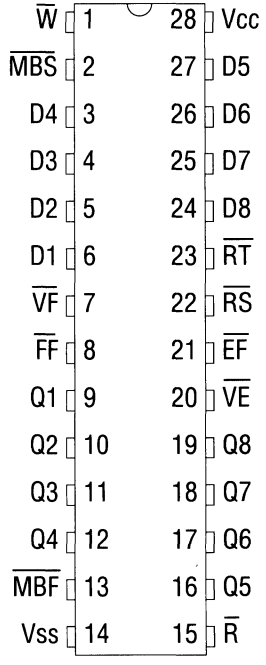
- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

28L DIP



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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO 1K x 9 FIFO

FEATURES

- High speed: 25ns access, 35ns cycle time
- Industry standard pin-out
- Empty and Full warning flags
- Asynchronous READ and WRITE
- Depth and Width expansion capability
- Automatic retransmit
- Low power consumption
- Transistor loads for maximum data integrity

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

GENERAL DESCRIPTION

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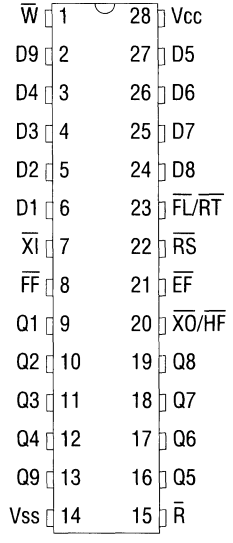
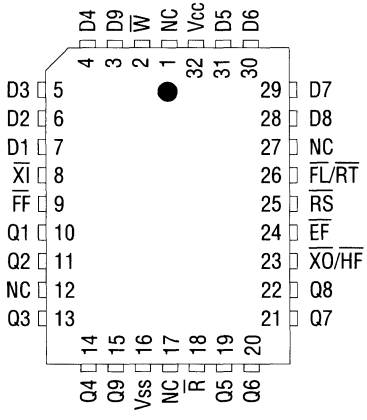
PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



FIFO

1K x 9 FIFO

MAILBOX REGISTER

FEATURES

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS — MARKING

- Timing

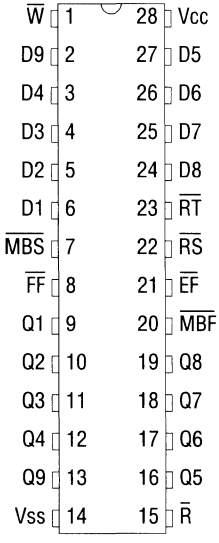
25ns access time	-25
30ns access time	-30
35ns access time	-35

- Packages

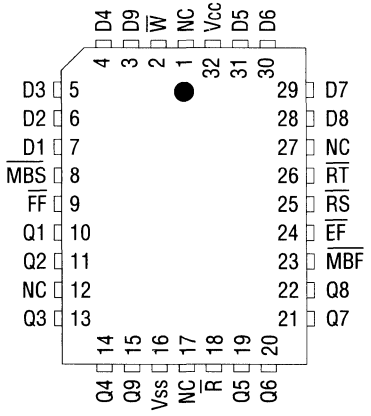
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

1K x 9 FIFO

VARIABLE FLAGS

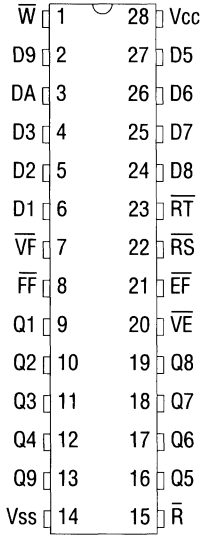
FEATURES

- High speed: 25ns access, 35ns cycle time
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

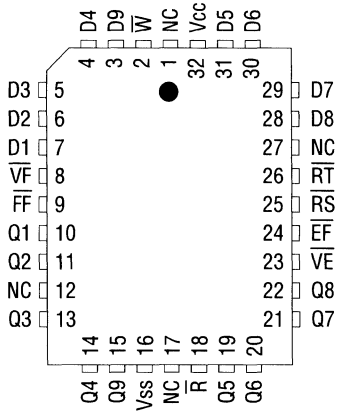
OPTIONS	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

1K x 16 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

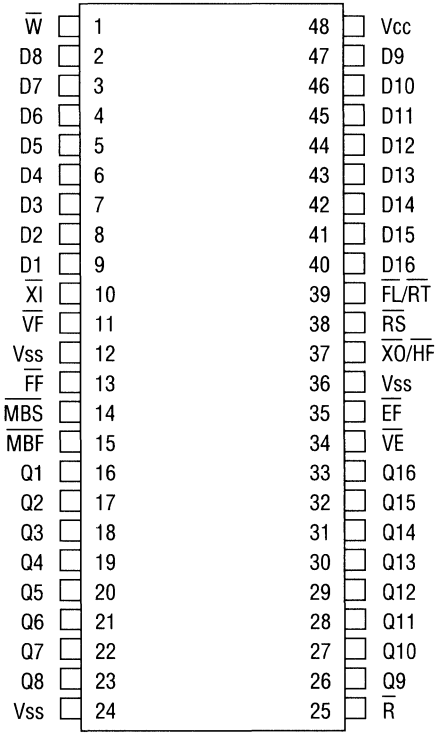
- High speed: 25ns access, 35ns cycle time
- 16-bit word width
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Easy expansion capability
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

48L DIP



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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

1K x 16 to 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

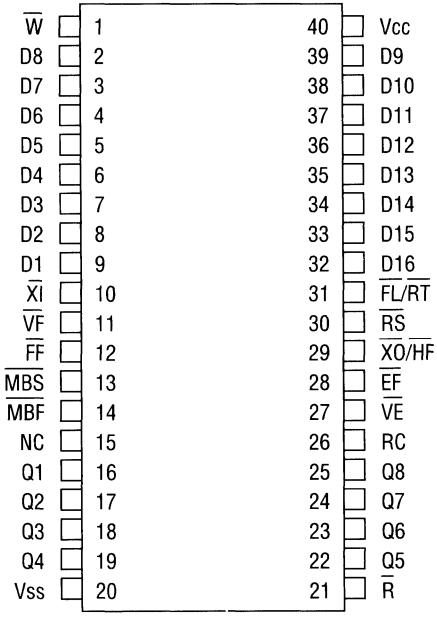
- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Easy expansion capability
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity
- One chip interface between a 16 bit bus and an 8 bit bus

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

40L DIP



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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

2K x 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

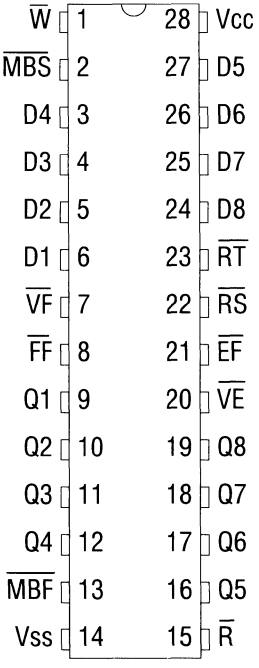
FEATURES

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

28L DIP



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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO 2K x 9 FIFO

FEATURES

- High speed: 25ns access, 35ns cycle time
- Industry standard pin-out
- Empty and Full warning flags
- Asynchronous READ and WRITE
- Depth and Width expansion capability
- Automatic retransmit
- Low power consumption
- Transistor loads for maximum data integrity

OPTIONS MARKING

• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

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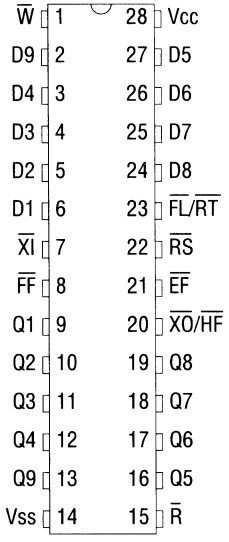
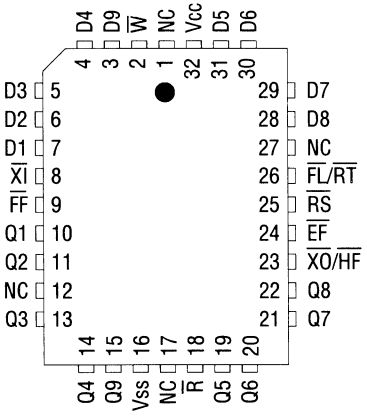
PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



FIFO

2K x 9 FIFO

MAILBOX REGISTER

FEATURES

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS — MARKING

- Timing

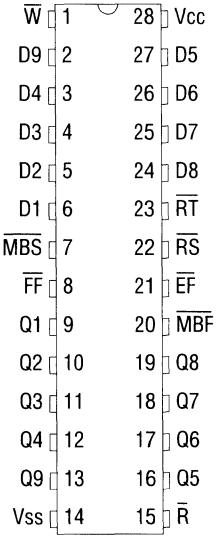
25ns access time	-25
30ns access time	-30
35ns access time	-35

- Packages

Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

28L DIP



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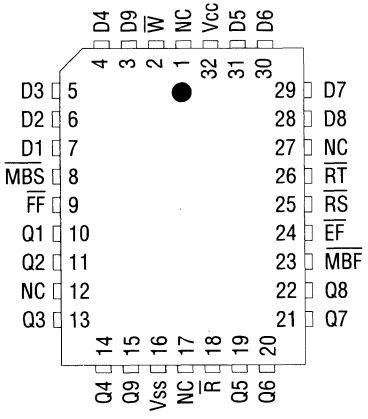

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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

2K x 9 FIFO

VARIABLE FLAGS

FEATURES

- High speed: 25ns access, 35ns cycle time
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS — MARKING

- Timing

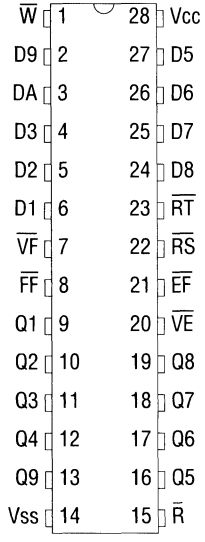
25ns access time	-25
30ns access time	-30
35ns access time	-35

- Packages

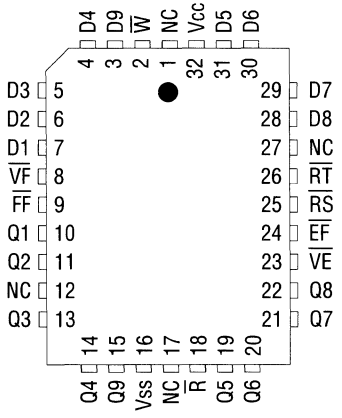
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



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FIFO

2K x 16 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

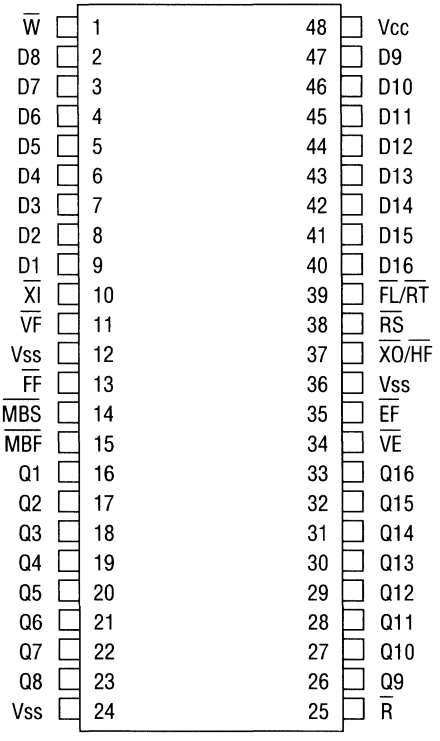
FEATURES

- High speed: 25ns access, 35ns cycle time
- 16-bit word width
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Easy expansion capability
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

48L DIP



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

There are three types of FIFO's in the Micron family: Expandable, Mailbox Register, and Variable Flags. Expandable FIFO's are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFO's have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFO's allow the user to program the level of the full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

2Kx16 to 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

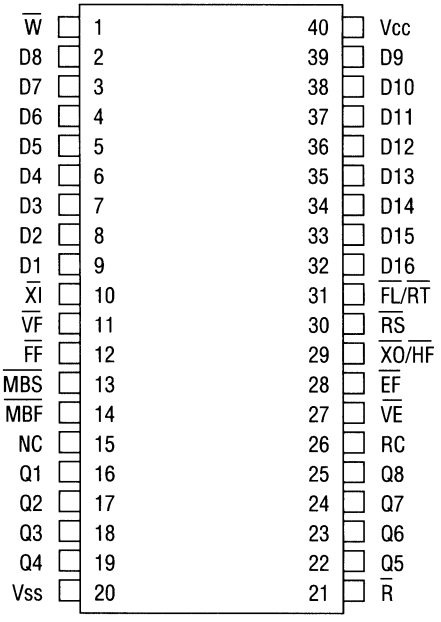
- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Easy expansion capability
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity
- One chip interface between a 16 bit bus and an 8 bit bus

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

40L DIP



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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

4K x 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

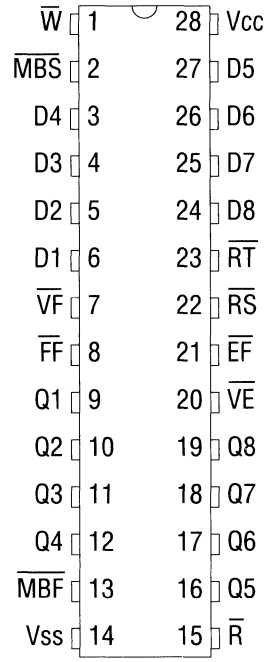
- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

28L DIP



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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO 4K x 9 FIFO

FEATURES

- High speed: 25ns access, 35ns cycle time
- Industry standard pin-out
- Empty and Full warning flags
- Asynchronous READ and WRITE
- Depth and Width expansion capability
- Automatic retransmit
- Low power consumption
- Transistor loads for maximum data integrity

OPTIONS MARKING

• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 8-transistor memory cell with P-channel loads. They are fabricated using twin tub, silicon gate CMOS technology. An eight transistor memory cell produces a device that has the minimum possible power dissipation and maximum data integrity.

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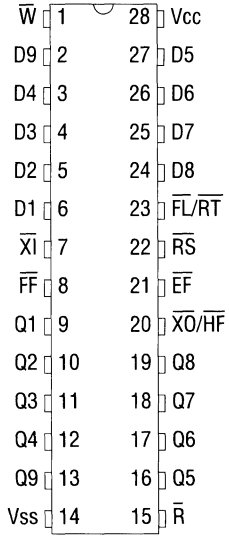
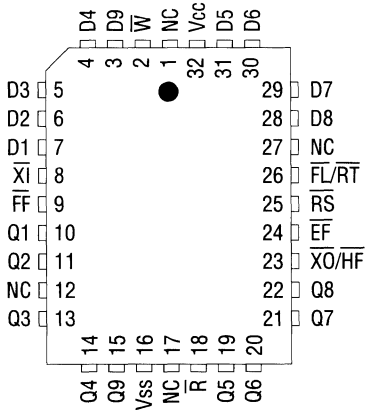
PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



FIFO

4K x 9 FIFO

MAILBOX REGISTER

FEATURES

- High speed: 25ns access, 35ns cycle time
- Programmable Mailbox register
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS — MARKING

- Timing

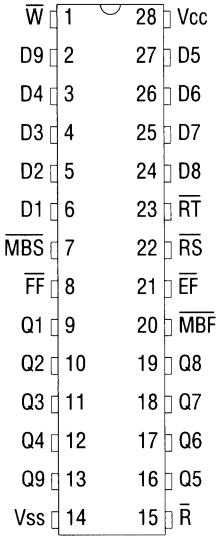
25ns access time	-25
30ns access time	-30
35ns access time	-35

- Packages

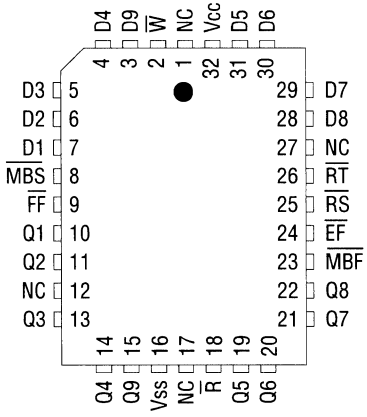
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



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FIFO

4K x 9 FIFO

VARIABLE FLAGS

FEATURES

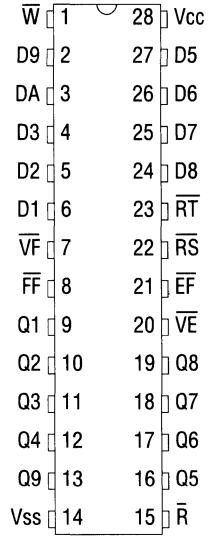
- High speed: 25ns access, 35ns cycle time
- Programmable Empty/Full flags (128 increments)
- Asynchronous READ and WRITE
- Automatic retransmit
- Low power
- Transistor loads for maximum data integrity

OPTIONS — MARKING

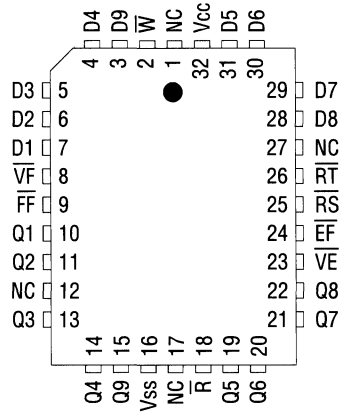
- Timing
  - 25ns access time — -25
  - 30ns access time — -30
  - 35ns access time — -35
- Packages
  - Plastic DIP — None
  - Ceramic DIP — C
  - Plastic LCC — EJ
  - Ceramic LCC — EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



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MICRON TECHNOLOGY

Micron Technology is one of the only manufacturers of military-grade memory components that offers 100% on-shore fabrication.

Located in Boise, Idaho, Micron currently maintains two wafer fabrication (fab) facilities with full assembly, test, quality assurance and failure analysis capabilities. Our third wafer fabrication facility, also located in Boise, is scheduled to begin production in 1989.

Micron's design rules for Fab I and II are 1.2 drawn and 1.0 micron effective. Under Fab III guidelines, this will progress down to 1.0 and 0.8 micron effective.

As a supplier to the defense electronics industry, Micron offers memory products certified to JAN 38510, DESC Standard Military Drawings (SMD) and 883 Rev. C Class B. Our wafer fabrication is currently certified to the level of 38510 for NMOS processes.

MILITARY PRODUCTS — MICRON

Since 1987 Micron has been the sole source of JAN 38510 256K DRAMs. We have also introduced an 883 dual port DRAM (Video RAM) and the first 256K x 1 and 64K x 4 high-speed static RAMs. We will soon be introducing the industry's first SMD Video RAM.

As a leader in the high-density memory market, Micron is a founding participant in Sematech, a U.S. government sponsored consortium aimed at the memory needs of the defense industry. Plans for future devices include a 1 megabit static RAM, a 1 megabit video RAM and a 4 megabit DRAM. These devices are currently under development independent of Sematech or Defense Advanced Research Projects Agency (DARPA) support.

MILITARY PRODUCTS — FUTURE REQUIREMENTS

In the area of radiation tolerance, Micron believes most contracts will require a defined level of radiation immunity. In response, we are currently testing SRAM and DRAM CMOS products through total dose, dose rate and single event upset.

We believe the defense industry is heading toward higher-density memory, faster speeds and more sophisticated "memory solutions." This may include a non-standard packaging concept specially designed for cooling or possibly higher density than currently available from a single component.

We also believe that the defense memory industry will move towards tighter processing geometries, new packaging concepts and more advanced hardware development through an interface of the component designer andthe systems design engineer. Our processes, technology and marketing resources are poised to support such requirements.

MILITARY PRODUCT SELECTION GUIDE

DRAM

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package and Number of Pins Process				Page
				Standby	Active	CDIP	CLCC	Flat Pack	Process	
64K x 1	Page Mode	MT4264 883	100,120,150	15mw	75mw	16	18	16	NMOS	7-5
64K x 4	Page Mode	MT4067 883	100,120,150	15mw	150mw	16	18	16	NMOS	7-17
256K x 1	Page Mode	MT1259 883	100,120,150	15mw	150mw	16	18	16	NMOS	7-29
256K x 4	Fast Page Mode	MT4C4256 883	100,120,150	5mw	175mw	20	-	20	CMOS	7-41
1 Meg x 1	Fast Page Mode	MT4C1024 883	100,120,150	5mw	175mw	18	-	18	CMOS	7-53

VRAM

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package & No. of Pins		Page
				Standby	Active	CDIP	Process	
64K x 4	Page Mode	MT42C4064 883	120,150,200	10mw	150mw	24	CMOS	7-65

SRAM

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package & No. of Pins		Process	Page
				CDIP	CLCC		
2K x 8	CE & OE	MT5C1608 883	15 to 35	24	24	CMOS	7-95
8K x 8	CE1, CE2 & OE	MT5C6408 883	15 to 35	28	32	CMOS	7-103
16K x 1	CE only	MT5C1601 883	15 to 35	20	20	CMOS	7-111
16K x 4	CE only	MT5C6404 883	15 to 35	22	22	CMOS	7-119
32K x 8	CE & OE	MT5C2568 883	25 to 45	28	32	CMOS	7-127
64K x 1	CE only	MT5C6401 883	15 to 35	22	22	CMOS	7-135
64K x 4	CE only	MT5C2564 883	25 to 45	24	28	CMOS	7-141
256K x 1	CE only	MT5C2561 883	25 to 45	24	28	CMOS	7-149

MILITARY DRAM

64K x 1 DRAM

ADDITIONAL MILITARY SPECIFICATIONS

- SMD 82010

FEATURES

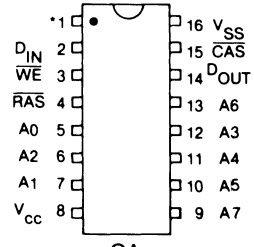
- Industry standard pin-out and timing
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby, 75mW active, typical
- Common I/O capability using "Early Write"
- Optional Page Mode access cycle
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 256 cycle refresh distributed across 4ms
- Specifications guaranteed over full military DRAM temperature range (-55°C to +110°C)
- MIL-STD 883C processing

OPTIONS MARKING

- Process Level
  - MIL-STD 883C (-55°C to +110°C) Parts processed to full requirements of MIL-STD-883C, method 5004 and 5005 — 883C
  - MIL-STD 883C with the exception that final electrical testing is performed at 0°C to 70°C — M070
- Timing
  - 100ns access — -10
  - 120ns access — -12
  - 150ns access — -15
- Packages:
  - Ceramic DIP — C
  - Ceramic LCC — EC
  - Ceramic Flat Pack — F

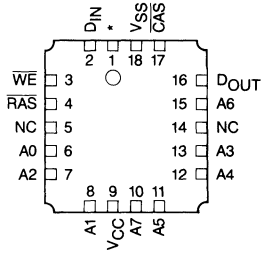
PIN ASSIGNMENT (Top View)

16 Pin DIP



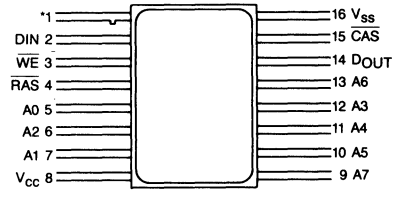
CA

18 Pin LCC



ECA

16 Pin Flat Pack



FA

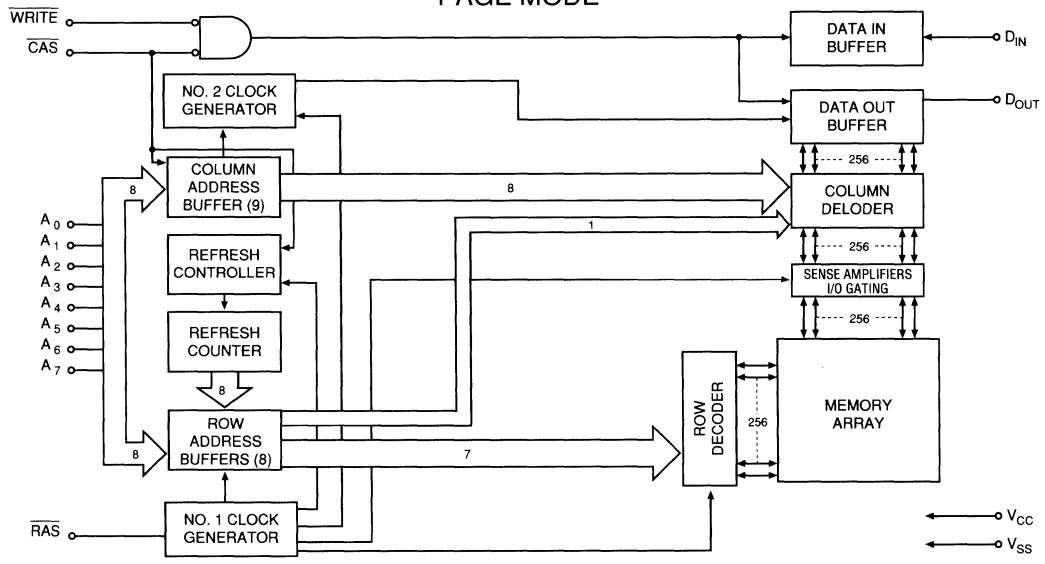
* No Connect - Open

GENERAL DESCRIPTION

The MT4264 883C is a randomly accessed solid-state memory containing 65,536 bits organized in a x1 configuration. The 16 address bits are entered 8 bits at a time using $\overline{RAS}$ to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. If the $\overline{WE}$ pin goes low prior to $\overline{CAS}$ going low, the output pin remains open until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after Data reaches the output pin, the output pin is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-MODIFY-WRITE cycle. Data-in is latched when $\overline{WE}$ strobes low.

By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled to execute several faster READ, WRITE, READ-WRITE or READ-MODIFY-WRITE cycles within the $\overline{RAS}$ address defined PAGE boundary. Returning $\overline{RAS}$ high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the $\overline{RAS}$ high-time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (Refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 msec (regardless of sequence).

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -1.5V to +7.0V
Storage temperature range ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Lead temperature (soldering 5 sec.) ..... 300°C
Juction temperature (Tj) ..... +150°C
Short Circuit Output Current 50mA
Thermal resistance (θjc) 16 pin DIP ..... 50°C/W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL PERORMANCE CHARACTERISTICS

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Current from V_{CC} (active); $\overline{RAS}$ and $\overline{CAS}$ = Cycling; $T_{RC} = T_{RC(MIN)}$	I_{CC1}		40	mA	3
Supply Current from V_{CC} (active, page mode); $\overline{RAS} = V_{IL}$, $\overline{CAS}$ = Cycling; $T_{PC} = T_{PC(MIN)}$	I_{CC2}		40	mA	3
Supply Current from V_{CC} (standby); $\overline{RAS}$ and $\overline{CAS} = V_{IH}$	I_{CC3}		6	mA	
Supply Current from V_{CC} (refresh, $\overline{RAS}$ only); $\overline{RAS}$ = Cycling: $\overline{CAS} = V_{IH}$	I_{CC4}		30	mA	3
Output High Voltage (I_{OH} = -5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OL} = 5mA)	V_{OL}		0.4	V	1
Input Leakage	I_{IH}	-10	10	µA	
Any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins = 0V	I_{IL}	-10	10	µA	
Output Leakage (0 ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} Supply Voltage	V_{CC}	4.5	5.5	V	
Vss power supply and signal reference	Vss	0.0	0.0	V	1
High level input voltage (all inputs)	V_{IH}	2.4	V_{CC}+1	V	1
Low level input voltage (all inputs)	V_{IL}	-1.0	0.8	V	1
Operating Case Temperature	Tc	-55	+110	°C	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8), D_{IN}	C_{I1}		5	pF	3
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		8	pF	3
Output Capacitance D_{OUT}	C_O		8	pF	3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

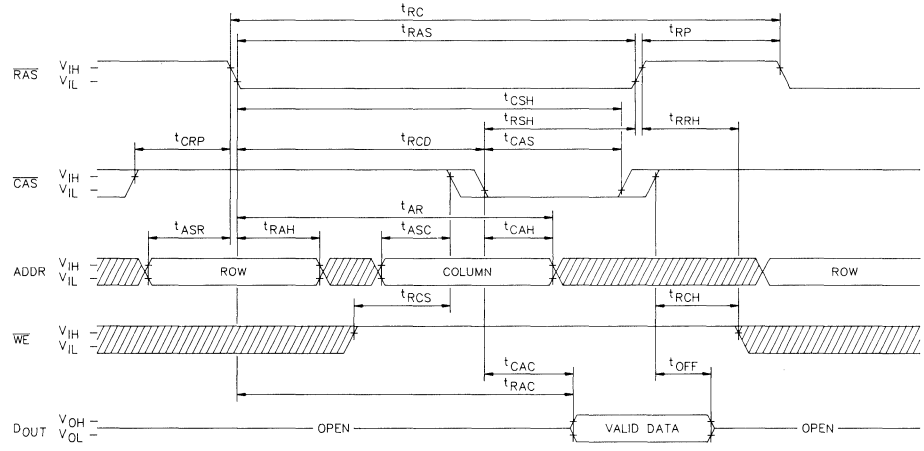
(Notes: 3, 4, 5, 6, 7, 8) (-55°C ≤ T_C ≤ 110°C, Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	195		230		250		ns	
READ-MODIFY-WRITE cycle time	^tRWC	230		255		270		ns	
PAGE-MODE cycle time	^tPC	90		100		120		ns	18
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	9
Access time from $\overline{CAS}$	^tCAC		50		60		75	ns	10
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{CAS}$ pulse width	^tCAS	50	10,000	60	10,000	75	10,000	ns	
$\overline{RAS}$ precharge time	^tRP	80		90		90		ns	
$\overline{CAS}$ precharge time	^tCPN	25		25		30		ns	11,19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	30		30		40		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	25	50	25	60	35	75	ns	12
$\overline{RAS}$ hold time	^tRSH	50		60		75		ns	
$\overline{CAS}$ hold time	^tCSH	110		120		150		ns	
Row address set-up time	^tASR	0		0		0		ns	19
Row address hold time	^tRAH	15		15		20		ns	
Column address set-up time	^tASC	0		0		0		ns	19
Column address hold time	^tCAH	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		ns	19
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		ns	13, 19
READ command hold time referenced to $\overline{RAS}$	^tRRH	10		10		10		ns	
Output disable delay	^tOFF	0	35	0	30	0	35	ns	14
WRITE command set-up time	^tWCS	0		0		0		ns	15
WRITE command hold time	^tWCH	35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	85		100		120		ns	
WRITE command pulse width	^tWP	35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		ns	16, 19
Data-in hold time	^tDH	35		40		45		ns	16
Data-in hold time referenced to $\overline{RAS}$	^tDHR	85		100		120		ns	
$\overline{CAS}$ to WRITE delay	^tCWD	40		50		60		ns	15
$\overline{RAS}$ to WRITE delay	^tRWD	90		110		135		ns	15
Transition time (rise or fall)	^tT	3	100	3	100	3	100	ns	6, 7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		10		10		ns	
Refresh Period (256 cycles distributed)	^tREFD		4		4		4	ms	17
Refresh Period (256 cycles burst)	^tREFB		4		4		4	ms	18

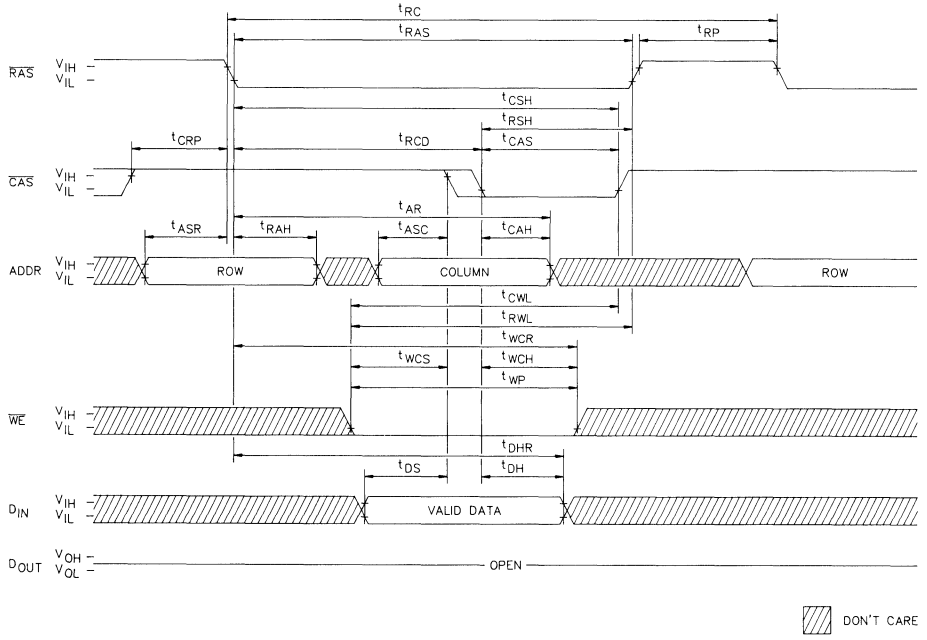
NOTES

1. V_{SS} is common for all voltages.
2. This parameter is sampled, not 100% tested. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. Specified values are obtained with the output load equal to 2TTL loads and 100pF to V_{SS}.
4. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles, (READ, WRITE, READ-MODIFY-WRITE, $\overline{RAS}$ refresh) before proper device operation is assured.
5. AC characteristics assume transistion time (^tT) = 5ns.
6. V_{IL} (max) and V_{IH} (min) are reference levels for measuring timing of input signals. Transition times are measured between V_{IL} and V_{IH}.
7. In addition to meeting the transition rate specification, all input signals must transit between V_{IL} and V_{IH} (or between V_{IH} and V_{IL}) in a monotonic manner.
8. If $\overline{CAS}$ = V_{IH}, data output is high impedance. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
9. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
10. Assumes that $^tRCD \geq {}^tRCD$ (max).
11. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCP. Note 9 applies to determine valid data out.
12. Operation within ^tRCD (max) limit ensures the ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access is controlled excusively by ^tCAC.
13. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
14. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
15. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min) the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \geq {}^tCWD$ (min) and $^tRWD \geq {}^tRWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the conditions of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
16. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
17. A 256 cycle distibuted refresh consists of an address location refresh cycle being performed within 15.625µS so that all 256 $\overline{RAS}$ address combinations are executed within 4ms (regardless of sequence). Micron recommends distributed refresh.
18. A 256 cycle burst refresh consists of refreshing, as rapidly as minimum cycle time allows, all 256 combinations of $\overline{RAS}$ addresses (regardless of sequence). The refresh mode must be executed within 4ms.
19. This parameter is "conditionally" guaranteed parameter that is specified to aid with device application. It is not directly verified by a specific test but is used, with several other parameters, in the performance verification of other attributes.

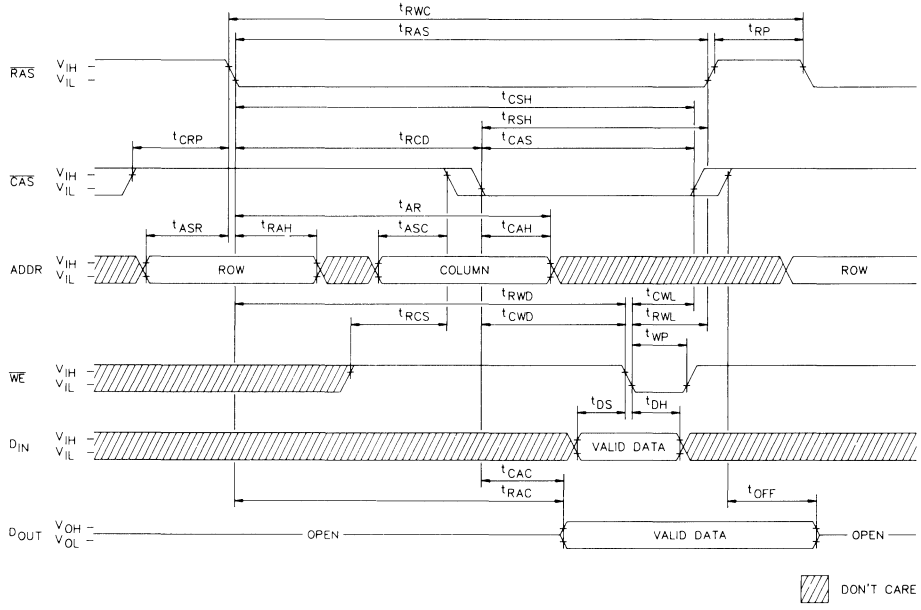
READ CYCLE



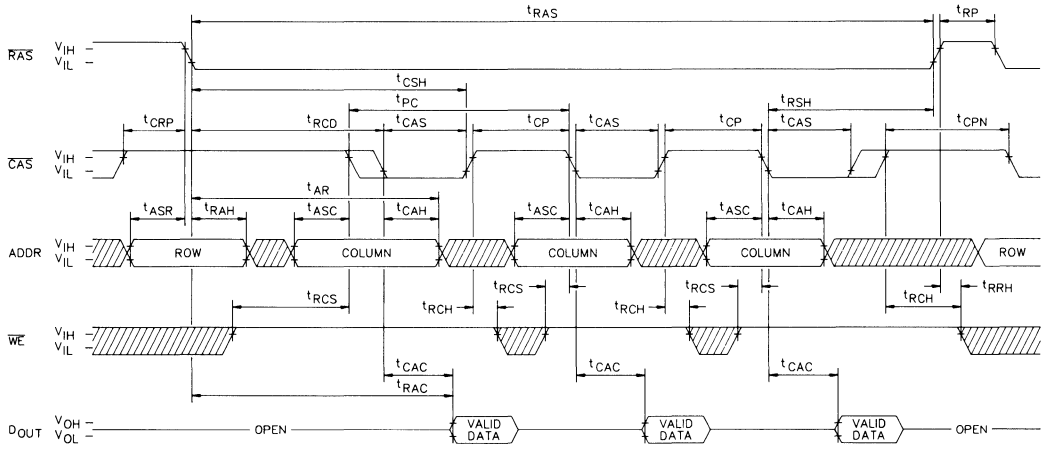
EARLY-WRITE CYCLE



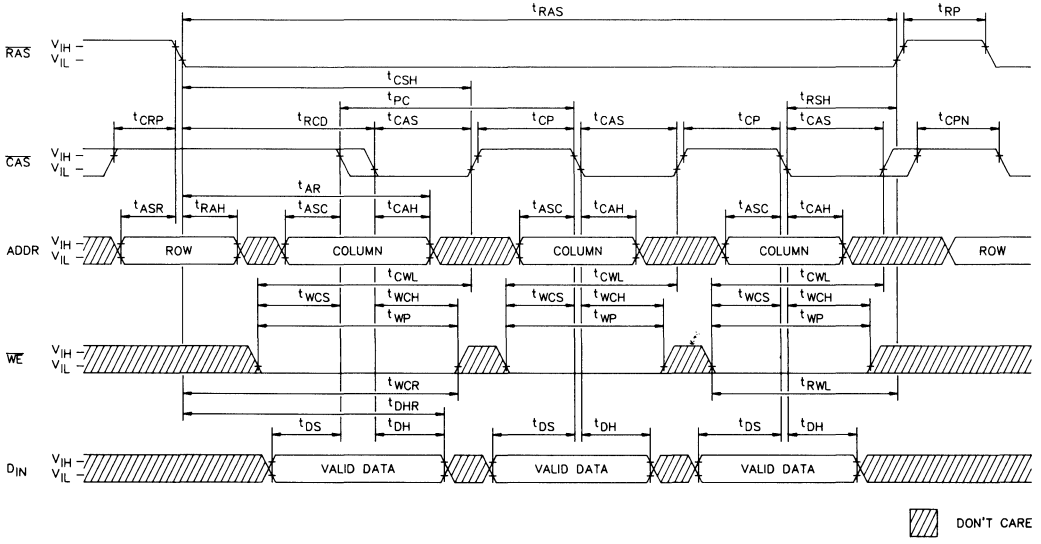
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



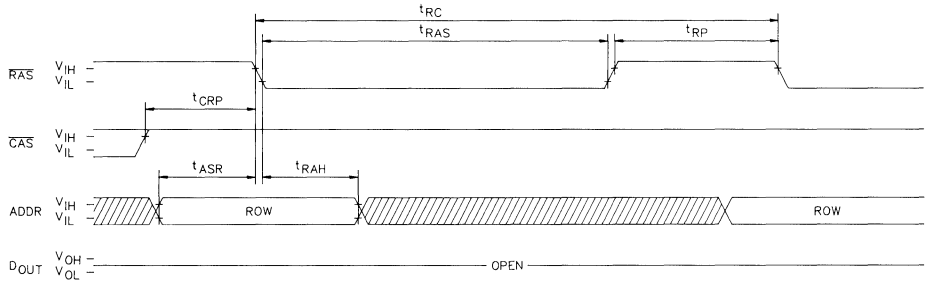
PAGE-MODE READ CYCLE



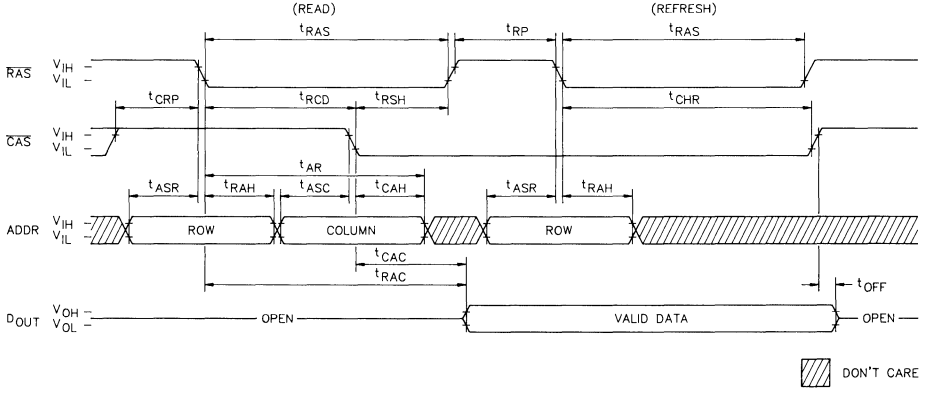
PAGE-MODE EARLY-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE
(ADDR = A_0 - A_7)



HIDDEN REFRESH CYCLE

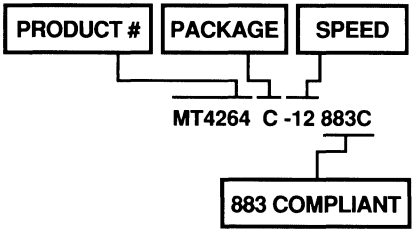


MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan and submit to qualifying activity.	Approved by DESC
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot.	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD 883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD 883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Stabilization Bake	Method 1008, cond. C	100%
10. Temperature Cycle	Method 1010, cond. C	100%
11. Constant Acceleration	Method 2001, cond. E	100%
12. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
13. Initial Electricals	Manufacturer's documented data sheet @ +118°C	100%
14. Marking	Method 2015	100%
15. Burn-in	Method 1015, subgroups A-2 for endpoint 162 hours @ 125°C	100%
16. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +113°C 5% PDA and in-line Group A per method 5005	100%
17. External Visual	Method 2009	100%
18. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
19. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection per Method 5005 (attributes data only)		
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and construction tests	Each package type on each lot
21. Group C	Die related (1000 hr. operating life)	Generic every 13 weeks
22. Group D	Package related test	Each package type Generic every 26 weeks

ORDER INFORMATION

64Kx1, 120ns access, -55°C to +110°C, in Ceramic DIP



The Micron MT4264-883C serves the special needs of the Defense/Aerospace market. The Micron Military Product Assurance Program provides state-of-the-art screened to MIL-STD-883C Class B Revision C Methods 5004 and 5005. All IC's furnished under this program are produces on certified lines and are manufactured, assembled, tested quality controlled in Micron's modern Boise, Idaho USA facility.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

MILITARY DRAM

64K x 4 DRAM

ADDITIONAL MILITARY SPECIFICATIONS

- SMD 87676

FEATURES

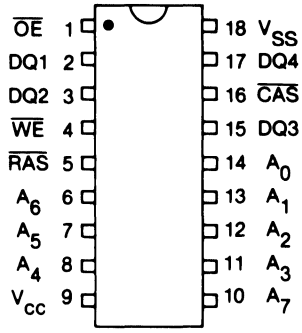
- Industry standard pin-out and timing
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby, 150mW active, typical
- Optional Page Mode access cycle
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 256 cycle refresh distributed across 4ms
- Specifications guaranteed over full military DRAM temperature range (-55°C to +110°C)
- MIL-STD 883C processing

OPTIONS MARKING

- Process Level
  - MIL-STD 883C (-55°C to +110°C) Parts processed to full requirements of MIL-STD 883C, method 5004 and 5005 — 883C
  - MIL-STD 883C with the exception that final electrical testing is performed at 0°C to 70°C — M070
- Timing
  - 100ns access — -10
  - 120ns access — -12
  - 150ns access — -15
- Packages:
  - Ceramic DIP — C
  - Ceramic LCC — EC

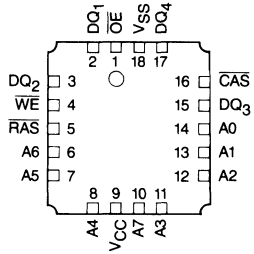
PIN ASSIGNMENT (Top View)

18 Pin DIP



CB

18 Pin LCC



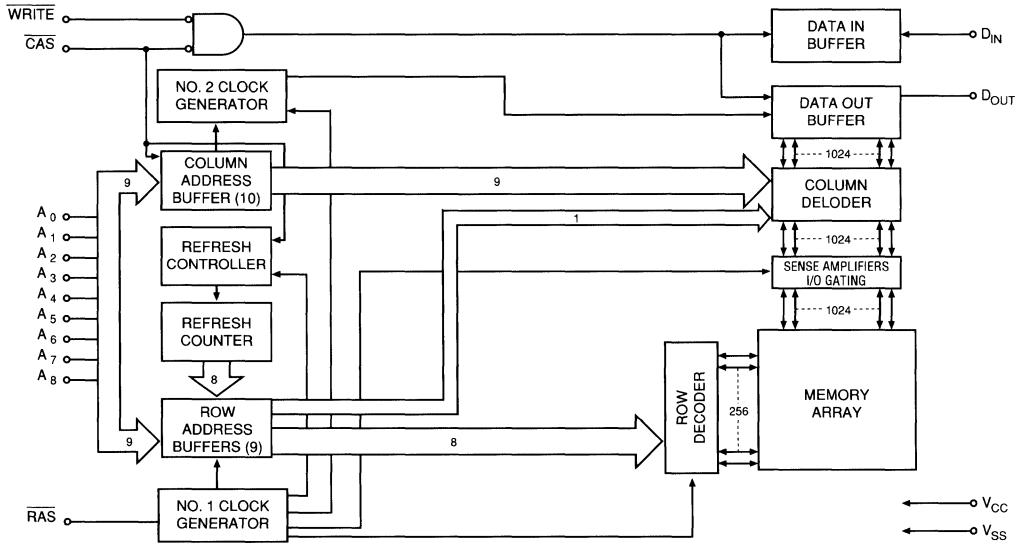
ECB

GENERAL DESCRIPTION

The MT4067 883C is a randomly accessed solid-state memory containing 262,144 bits organized in a 65,536 word x4 configuration. The 16 address bits are entered 8 bits at a time using $\overline{RAS}$ to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. If $\overline{WE}$ goes low after Data reaches the output pin, the output pin is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-MODIFY-WRITE cycle. Data-in is latched when $\overline{WE}$ strobes low.

By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled to execute several faster READ, WRITE, or READ-MODIFY-WRITE cycles within the $\overline{RAS}$ address defined PAGE boundary. Returning $\overline{RAS}$ high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the $\overline{RAS}$ high-time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (Refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 msec (regardless of sequence).

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss ..... -1.5V to +7.0V
Storage temperature range ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Lead temperature (soldering 5 sec.) ..... 300°C
Juction temperature (Tj) ..... +150°C
Short Circuit Output Current 50mA
Thermal resistance (θjc) 16 pin DIP ..... 50°C/W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL PERORMANCE CHARACTERISTICS

(Notes: 3,4,6,7) (-55°C ≤ T_C ≤ =110°C) (V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Current from Vcc (active); $\overline{RAS}$ and $\overline{CAS}$ = Cycling; T_{RC} = $T_{RC(MIN)}$	I_{CC1}		55	mA	2
Supply Current from Vcc (active, page mode); $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling; T_{PC} = $T_{PC(MIN)}$	I_{CC2}		55	mA	2
Supply Current from Vcc (standby); $\overline{RAS}$ and $\overline{CAS}$ = V_{IH}	I_{CC3}		8	mA	
Supply Current from Vcc (refresh, $\overline{RAS}$ only); $\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}	I_{CC4}		45	mA	2
Supply Current from Vcc (refresh, $\overline{CAS}$-before-$\overline{RAS}$); $\overline{RAS}$ and $\overline{CAS}$ = cycling	I_{CC5}		55	mA	2
Output High Voltage (I_{OH} = -5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OL} = 5mA)	V_{OL}		0.4	V	1
Input Leakage	I_{IH}	-10	10	µA	
Any input (0V ≤ V_{IN} ≤ Vcc), all other pins = 0V	I_{IL}	-10	10	µA	
Output Leakage (0 ≤ V_{OUT} ≤ Vcc)	I_{OZ}	-10	10	µA	

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc Supply Voltage	Vcc	4.5	5.5	V	
Vss power supply and signal reference	Vss	0.0	0.0	V	1
High level input voltage (all inputs)	V_{IH}	2.4	Vcc+1	V	1
Low level input voltage (all inputs)	V_{IL}	-1.0	0.8	V	1
Operating Case Temperature	Tc	-55	+110	°C	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8), D_{IN}	C_{I1}		5	pF	3
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		8	pF	3
Output Capacitance D_{OUT}	C_O		7	pF	3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

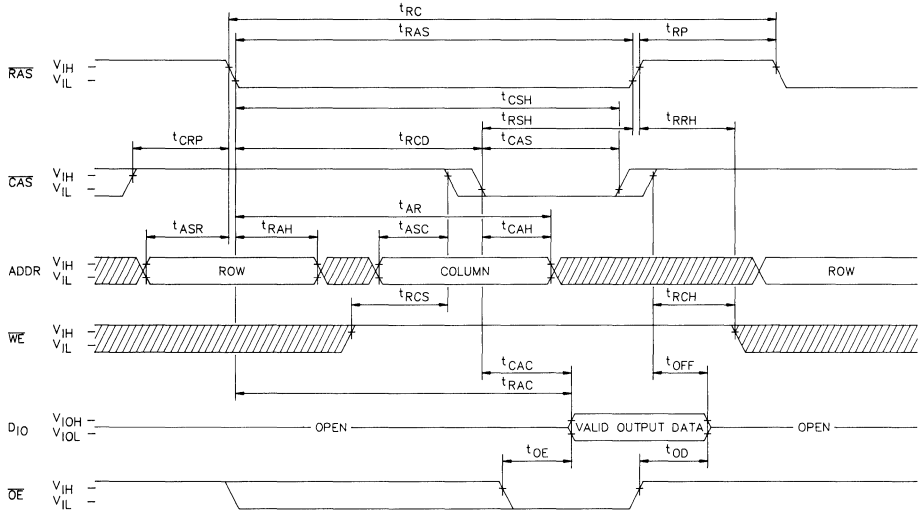
(Notes: 3, 4, 5, 6, 7, 8) (-55°C ≤ T_C ≤ +110°C, Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	195		220		250		ns	
READ-MODIFY-WRITE cycle time	^tRWC	250		290		315		ns	20
PAGE-MODE cycle time	^tPC	90		100		120		ns	20
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	9
Access time from $\overline{CAS}$	^tCAC		50		60		75	ns	10
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{CAS}$ pulse width	^tCAS	50	10,000	60	10,000	75	10,000	ns	
$\overline{RAS}$ precharge time	^tRP	80		90		90		ns	
$\overline{RAS}$ hold time	^tRSH	50		60		75		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	25	50	30	60	30	75	ns	
$\overline{CAS}$ precharge time	^tCPN	25		25		30		ns	20
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	30		30		35		ns	11
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	5		5		5		ns	
$\overline{CAS}$ hold time	^tCSH	110		120		150		ns	
Row address set-up time	^tASR	0		0		0		ns	20
Row address hold time	^tRAH	15		20		20		ns	
Column address set-up time	^tASC	0		0		0		ns	20
Column address hold time	^tCAH	20		30		30		ns	
Column address hold time reference to $\overline{RAS}$	^tAR	70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		ns	20
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		ns	20
READ command hold time referenced to $\overline{RAS}$	^tRRH	10		10		10		ns	
Output disable delay	^tOFF	0	40	0	40	0	40	ns	12
Output disable	^tOD		35		40		40	ns	
Output enable	^tOE		25		25		30	ns	13
WRITE command set-up time	^tWCS	0		0		0		ns	14
WRITE command hold time	^tWCH	35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	85		100		120		ns	
WRITE command pulse width	^tWP	35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		ns	15, 20
Data-in hold time	^tDH	35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	85		100		120		ns	
$\overline{CAS}$ to WRITE delay	^tCWD	40		50		60		ns	14,16,20
$\overline{RAS}$ to WRITE delay	^tRWD	90		110		135		ns	14,16,20
Transition time (rise or fall)	^tT	3	100	3	100	3	100	ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	17
Refresh Period (256 cycles distributed)	^tREFD		4		4		4	ms	18
Refresh Period (256 cycles burst)	^tREFB		4		4		4	ms	19

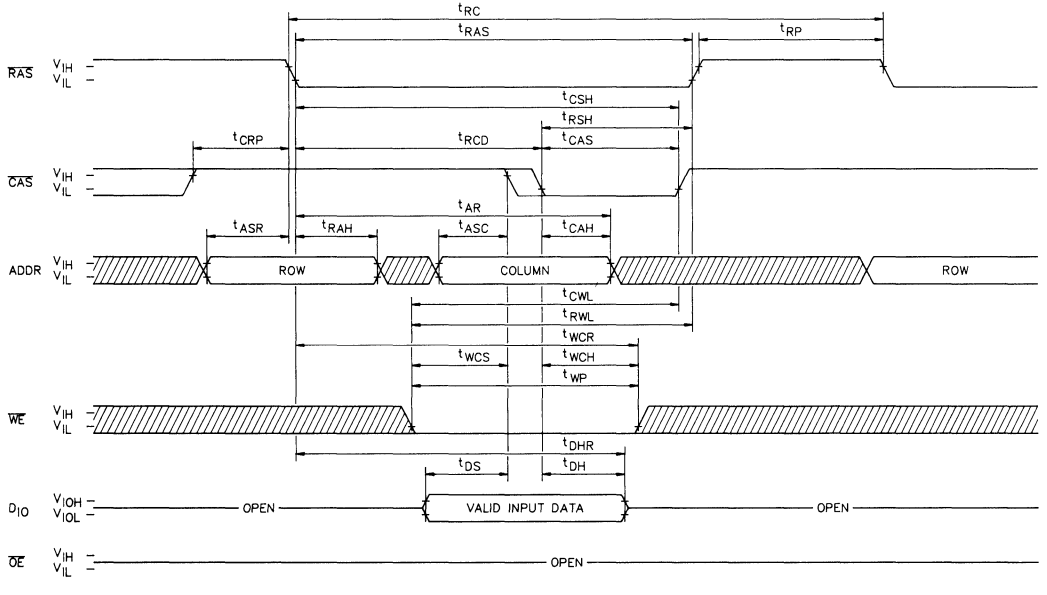
NOTES

1. V_{SS} is common for all voltages.
2. Specified values are obtained with the output load equal to 2TTL loads and 100pF to V_{SS}.
3. This parameter is sampled, not 100% tested. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
4. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles, (READ, WRITE, READ-MODIFY-WRITE, $\overline{RAS}$ refresh) before proper device operation is assured.
5. AC characteristics assume transistion time (^tT) = 5ns.
6. V_{IL} (max) and V_{IH} (min) are reference levels for measuring timing of input signals. Transition times are measured between V_{IL} and V_{IH}.
7. In addition to meeting the transition rate specification, all input signals must transit between V_{IL} and V_{IH} (or between V_{IH} and V_{IL}) in a monotonic manner.
8. If $\overline{CAS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, data output is high imped ance. If $\overline{CAS}$ = V_{IL} and $\overline{OE}$ = V_{IL}, data output may contain data from the last valid READ cycle.
9. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
10. Assumes that $^tRCD \geq {}^tRCD$ (max).
11. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCP. Note 8 applies to determine valid data out.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. If $\overline{OE}$ is taken LOW then HIGH D_{OUT} goes open. If $\overline{OE}$ is tied permanently LOW a READ-WRITE or READ-MODIFY-WRITE operation requires a separate READ and WRITE cycle.
14. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min) the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \geq {}^tCWD$ (min) and $^tRWD \geq {}^tRWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the conditions of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. During a READ-WRITE or READ-MODIFY-WRITE cycle the minimum specifications for ^tRWD and ^tCWD must be modified by adding 40 ns to each specification due to $\overline{OE}$ delay.
17. Enables on-chip refresh and address counters.
18. A 256 cycle distibuted refresh consists of an address location refresh cycle being performed within 15.625µS so that all 256 $\overline{RAS}$ address combinations are executed within 4ms (regardless of sequence). Micron recommends distributed refresh.
19. A 256 cycle burst refresh consists of refreshing, as rapidly as minimum cycle time allows, all 256 combinations of $\overline{RAS}$ addresses (regardless of sequence). The refresh mode must be executed within 4ms.
20. This parameter is "conditionally" guaranteed parameter that is specified to aid with device application. It is not directly verified by a specific test but is used, with several other parameters, in the performance verification of other attributes.

READ CYCLE

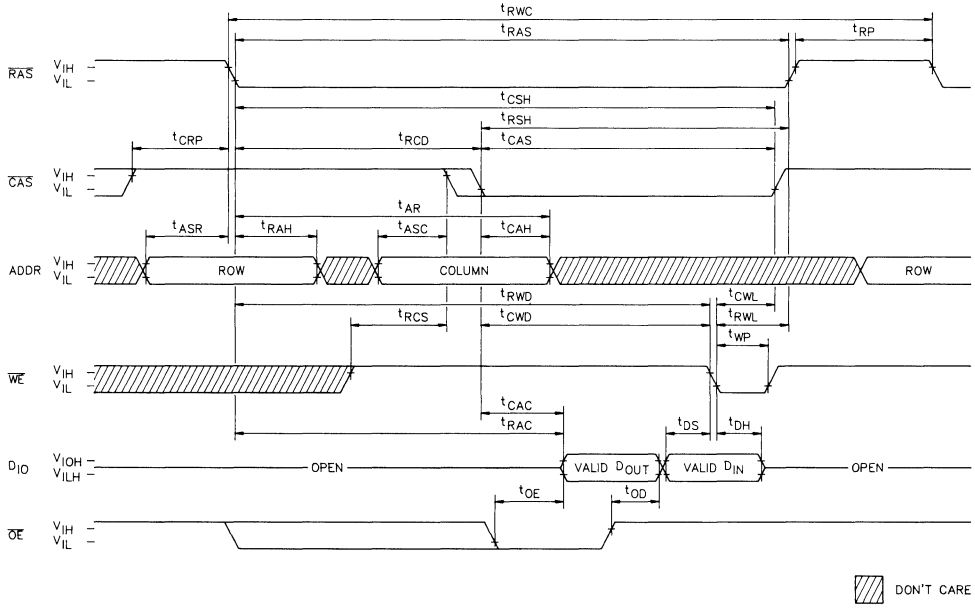


EARLY-WRITE CYCLE

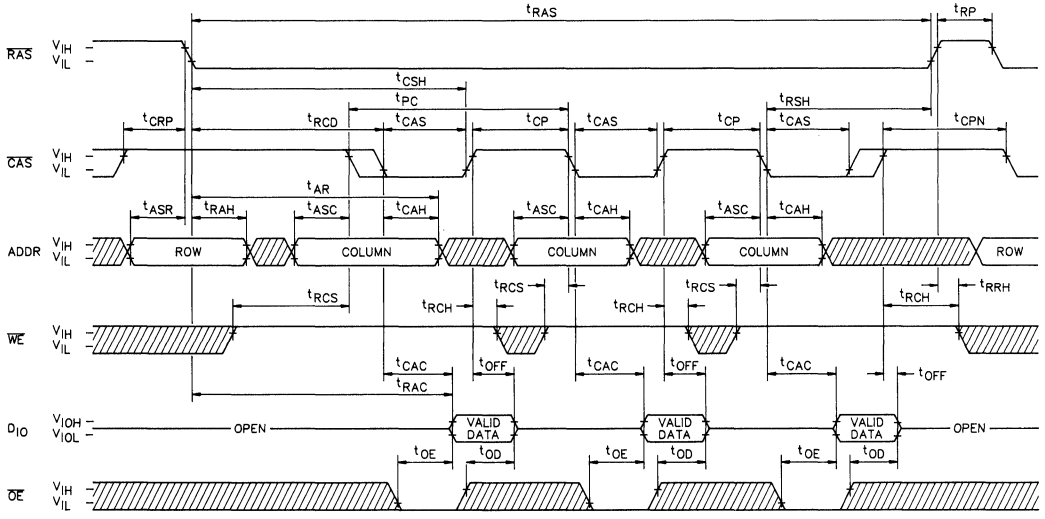


MILITARY DRAM

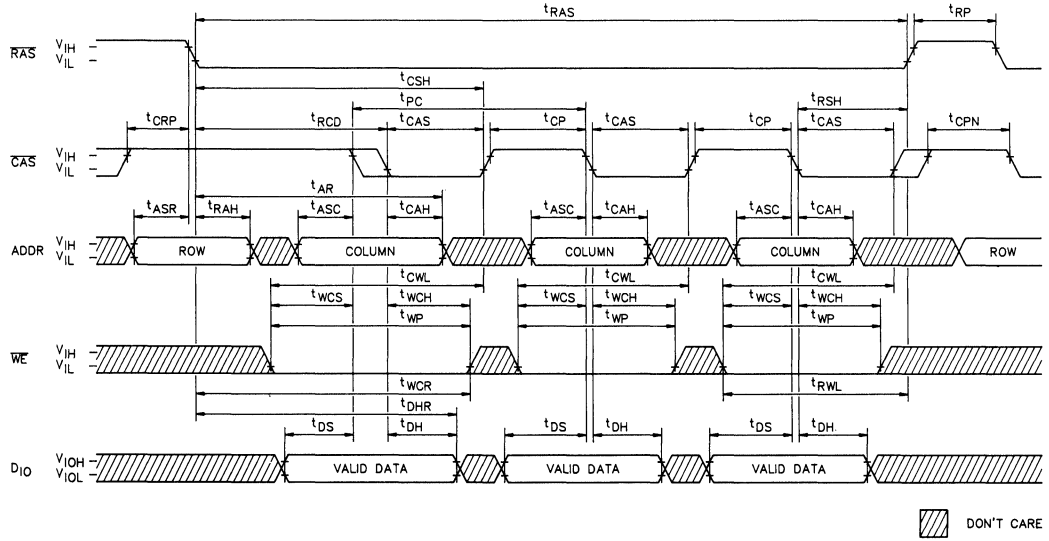
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



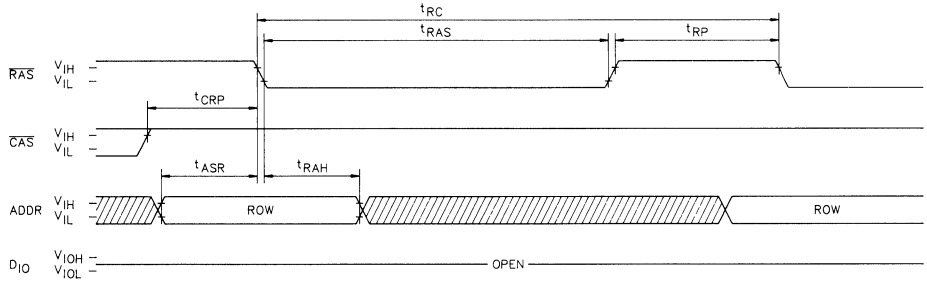
PAGE-MODE READ CYCLE



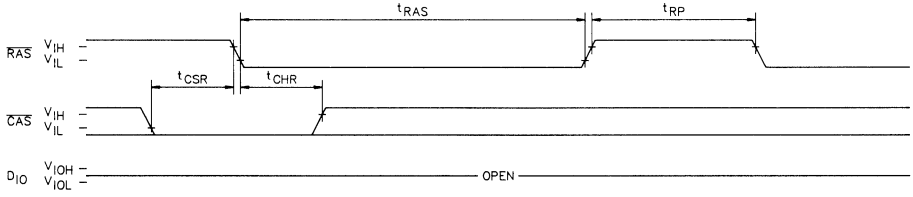
PAGE-MODE EARLY-WRITE CYCLE



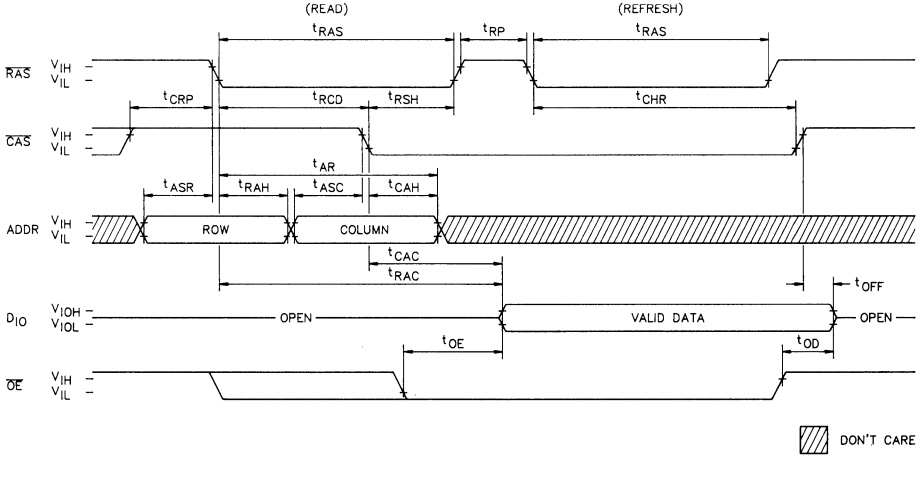
$\overline{RAS}$ ONLY REFRESH CYCLE
(ADDR = A_0 - A_7)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(ADDRESS INPUTS ARE IGNORED)



HIDDEN REFRESH CYCLE
($\overline{OE}$ = LOW)

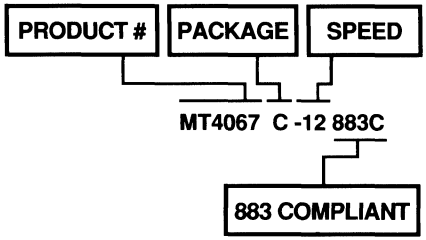


MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan and submit to qualifying activity.	Approved by DESC
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot.	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD 883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD 883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Stabilization Bake	Method 1008, cond. C	100%
10. Temperature Cycle	Method 1010, cond. C	100%
11. Constant Acceleration	Method 2001, cond. E	100%
12. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
13. Initial Electricals	Manufacturer's documented data sheet @ +118°C	100%
14. Marking	Method 2015	100%
15. Burn-in	Method 1015, subgroups A-2 for endpoint 162 hours @ 125°C	100%
16. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +113°C 5% PDA and in-line Group A per method 5005	100%
17. External Visual	Method 2009	100%
18. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
19. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection per Method 5005 (attributes data only)		
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and construction tests	Each package type on each lot
21. Group C	Die related (1000 hr. operating life)	Generic every 13 weeks
22. Group D	Package related test	Each package type Generic every 26 weeks

ORDER INFORMATION

64Kx4, 120ns access, -55°C to +110°C, in Ceramic DIP



The Micron MT4067-883C serves the special needs of the Defense/Aerospace market. The Micron Military Product Assurance Program provides state-of-the-art screened to MIL-STD 883C Class B Revision C Methods 5004 and 5005. All IC's furnished under this program are produces on certified lines and are manufactured, assembled, tested quality controlled in Micron's modern Boise, Idaho USA facility.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

MILITARY DRAM

256K x 1 DRAM

ADDITIONAL MILITARY SPECIFICATIONS

- SMD 85152
- JAN M38150/246

FEATURES

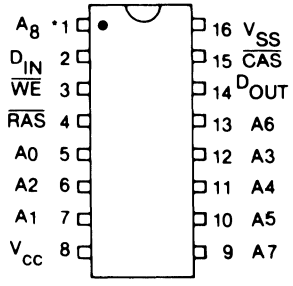
- Industry standard pin-out and timing
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby, 150mW active, typical
- Common I/O capability using "Early Write"
- Optional Page Mode access cycle
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 256 cycle refresh distributed across 4ms
- Specifications guaranteed over full military DRAM temperature range (-55°C to +110°C)
- MIL-STD 883C processing

OPTIONS MARKING

- Process Level
  - MIL-STD 883C (-55°C to +110°C) Parts processed to full requirements of MIL-STD 883C, method 5004 and 5005 — 883C
  - MIL-STD 883C with the exception that final electrical testing is performed at 0°C to 70°C — M070
- Timing
  - 100ns access — -10
  - 120ns access — -12
  - 150ns access — -15
- Packages:
  - Ceramic DIP — C
  - Ceramic LCC — EC

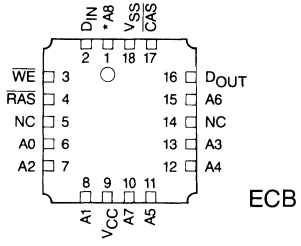
PIN ASSIGNMENT (Top View)

16 Pin DIP



CA

18 Pin LCC



ECB

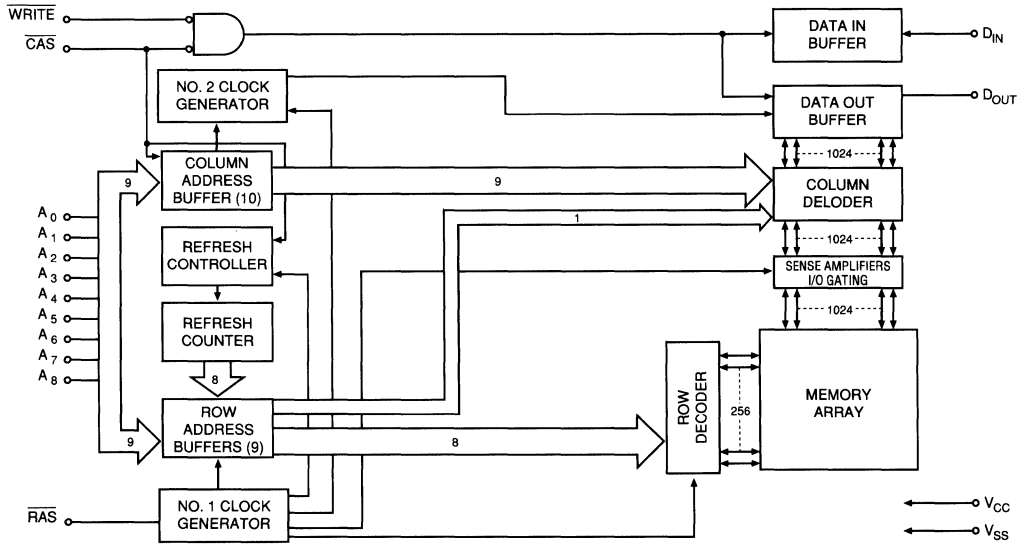
* ADDRESS NOT USED FOR $\overline{RAS}$ ONLY REFRESH

GENERAL DESCRIPTION

The MT1259 883C is a randomly accessed solid-state memory containing 262,144 bits organized in a x1 configuration. The 18 address bits are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes low prior to $\overline{CAS}$ going low, the output pin remains open until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after Data reaches the output pin, the output pin is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-MODIFY-WRITE cycle. Data-in is latched when $\overline{WE}$ strobes low.

By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled to execute several faster READ, WRITE, READ-WRITE or READ-MODIFY-WRITE cycles within the $\overline{RAS}$ address defined PAGE boundary. Returning $\overline{RAS}$ high terminates the memory cycle and decreases chip current to a reduced standby level. Also the chip is preconditioned for the next cycle during the $\overline{RAS}$ high-time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (Refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 msec (regardless of sequence).

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -1.5V to +7.0V
Storage temperature range ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Lead temperature (soldering 5 sec.) ..... 300°C
Junction temperature (Tj) ..... +150°C
Short Circuit Output Current 50mA
Thermal resistance (θjc) 16 pin DIP ..... 50°C/W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL PERORMANCE CHARACTERISTICS

(Notes: 3,4,6,7) (-55°C ≤ T_C ≤ =110°C) (V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Current from V_{CC} (active); $\overline{RAS}$ and $\overline{CAS}$ = Cycling; T_{RC} = $T_{RC(MIN)}$	I_{CC1}		55	mA	2
Supply Current from V_{CC} (active, page mode); $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling; T_{PC} = $T_{PC(MIN)}$	I_{CC2}		55	mA	2
Supply Current from V_{CC} (standby); $\overline{RAS}$ and $\overline{CAS}$ = V_{IH}	I_{CC3}		8	mA	2
Supply Current from V_{CC} (refresh, $\overline{RAS}$ only); $\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}	I_{CC4}		45	mA	2
Supply Current from V_{CC} (refresh, $\overline{CAS}$-before-$\overline{RAS}$); $\overline{RAS}$ and $\overline{CAS}$ = cycling	I_{CC5}		55	mA	2
Output High Voltage (I_{OH} = -5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OL} = 5mA)	V_{OL}		0.4	V	1
Input Leakage	I_{IH}	-10	10	µA	
Any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins = 0V	I_{IL}	-10	10	µA	
Output Leakage (0 ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc Supply Voltage	V_{CC}	4.5	5.5	V	
Vss power supply and signal reference	Vss	0.0	0.0	V	1
High level input voltage (all inputs)	V_{IH}	2.4	V_{CC}+1	V	1
Low level input voltage (all inputs)	V_{IL}	-1.0	0.8	V	1
Operating Case Temperature	Tc	-55	+110	°C	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_8), D_{IN}	C_{I1}		5	pF	3
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		8	pF	3
Output Capacitance D_{OUT}	C_O		7	pF	3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

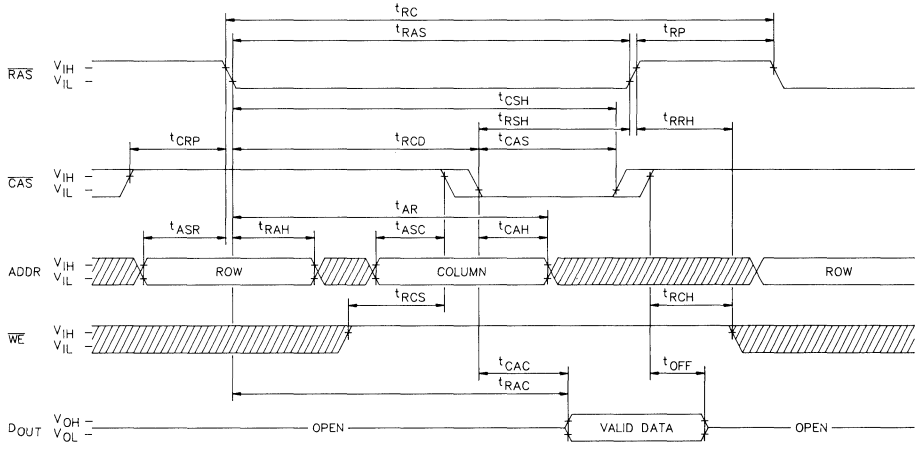
(Notes: 3, 4, 5, 6, 7, 8) (-55°C ≤ T_C ≤ +110°C, Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	195		220		250		ns	
READ-MODIFY-WRITE cycle time	^tRWC	230		250		275		ns	
PAGE-MODE cycle time	^tPC	90		100		120		ns	18
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	9
Access time from $\overline{CAS}$	^tCAC		50		60		75	ns	10
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{CAS}$ pulse width	^tCAS	50	10,000	60	10,000	75	10,000	ns	
$\overline{RAS}$ precharge time	^tRP	80		90		90		ns	
$\overline{RAS}$ hold time	^tRSH	50		60		75		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	30	50	30	60	30	75	ns	
$\overline{CAS}$ precharge time	^tCPN	25		25		30		ns	18
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	30		30		35		ns	11
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	5		5		5		ns	
$\overline{CAS}$ hold time	^tCSH	110		120		150		ns	
Row address set-up time	^tASR	0		0		0		ns	18
Row address hold time	^tRAH	15		20		20		ns	
Column address set-up time	^tASC	0		0		0		ns	18
Column address hold time	^tCAH	20		30		30		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		ns	18
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		ns	18
READ command hold time referenced to $\overline{RAS}$	^tRRH	10		10		10		ns	
Output disable delay	^tOFF	0	40	0	40	0	40	ns	12
WRITE command set-up time	^tWCS	0		0		0		ns	13
WRITE command hold time	^tWCH	35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	85		100		120		ns	
WRITE command pulse width	^tWP	35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		ns	14, 18
Data-in hold time	^tDH	35		40		45		ns	14
Data-in hold time referenced to $\overline{RAS}$	^tDHR	85		100		120		ns	
$\overline{CAS}$ to WRITE delay	^tCWD	40		50		60		ns	13
$\overline{RAS}$ to WRITE delay	^tRWD	90		110		135		ns	13
Transition time (rise or fall)	^tT	3	100	3	100	3	100	ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	15
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	15
Refresh Period (256 cycles distributed)	^tREFD		4		4		4	ms	16
Refresh Period (256 cycles burst)	^tREFB		4		4		4	ms	17

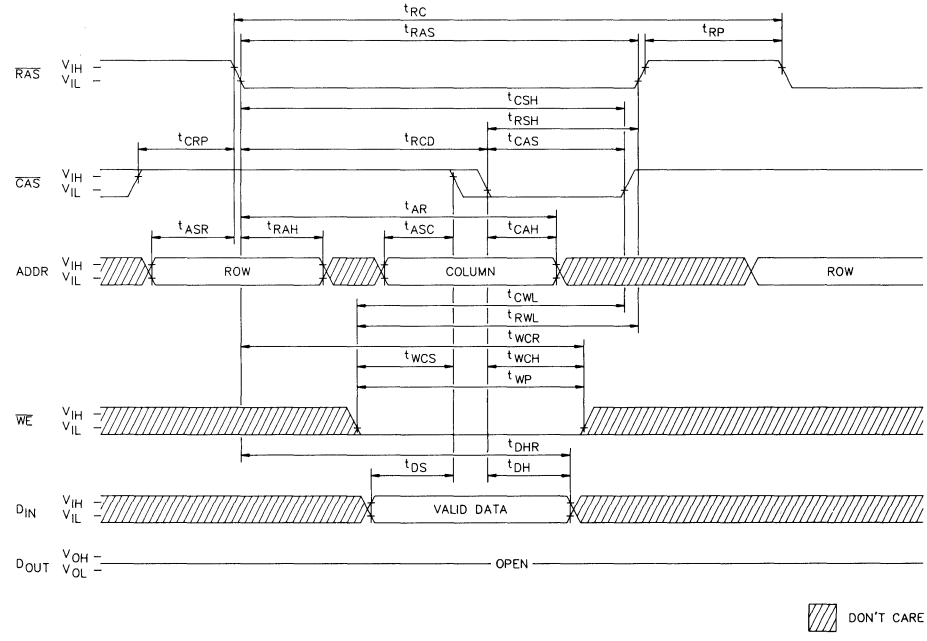
NOTES

1. V_{SS} is common for all voltages.
2. Specified values are obtained with the output load equal to 2TTL loads and 100pF to V_{SS}.
3. This parameter is sampled, not 100% tested. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
4. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles, (READ, WRITE, READ-MODIFY-WRITE, $\overline{RAS}$ refresh) before proper device operation is assured.
5. AC characteristics assume transistion time (^tT) = 5ns.
6. V_{IL} (max) and V_{IH} (min) are reference levels for measuring timing of input signals. Transition times are measured between V_{IL} and V_{IH}.
7. In addition to meeting the transition rate specification, all input signals must transit between V_{IL} and V_{IH} (or between V_{IH} and V_{IL}) in a monotonic manner.
8. If $\overline{CAS}$ = V_{IH}, data output is high impedance. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
9. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
10. Assumes that $^tRCD \geq {}^tRCD$ (max).
11. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCP. Note 8 applies to determine valid data out.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min) the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \geq {}^tCWD$ (min) and $^tRWD \geq {}^tRWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the conditions of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
15. Enable on-chip refresh and address counters.
16. A 256 cycle distibuted refresh consists of an address location refresh cycle being performed within 15.625µS so that all 256 $\overline{RAS}$ address combinations are executed within 4ms (regardless of sequence). Micron recommends distributed refresh.
17. A 256 cycle burst refresh consists of refreshing, as rapidly as minimum cycle time allows, all 256 combinations of $\overline{RAS}$ addresses (regardless of sequence). The refresh mode must be executed within 4ms.
18. This parameter is "conditionally" guaranteed parameter that is specified to aid with device application. It is not directly verified by a specific test but is used, with several other parameters, in the performance verification of other attributes.

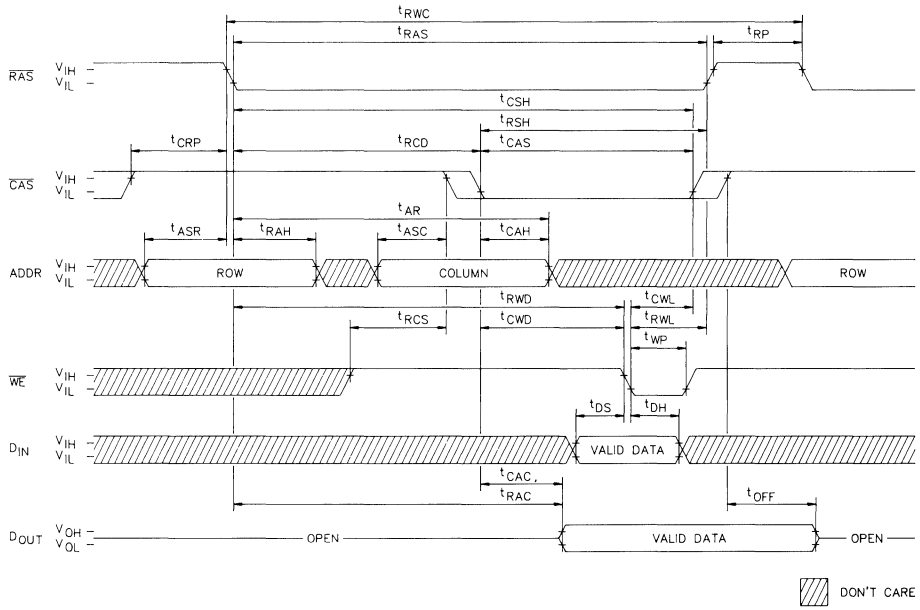
READ CYCLE



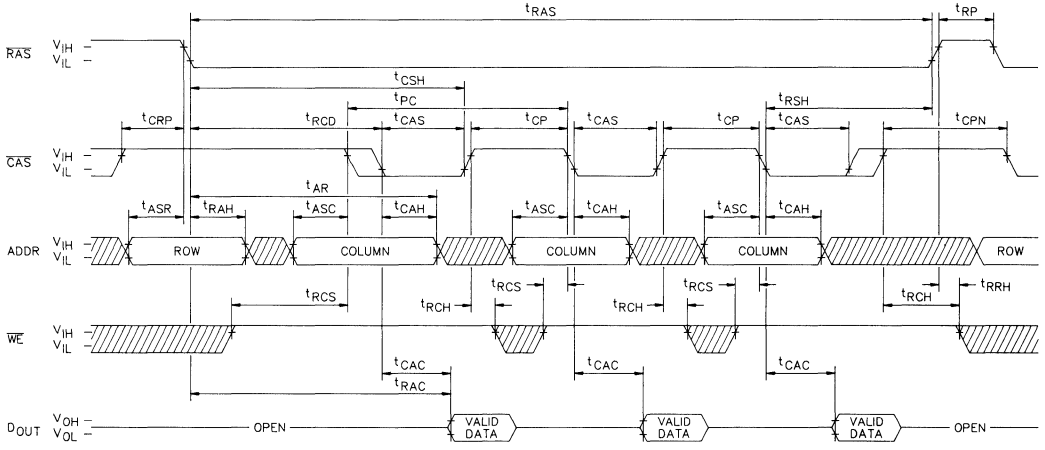
EARLY-WRITE CYCLE



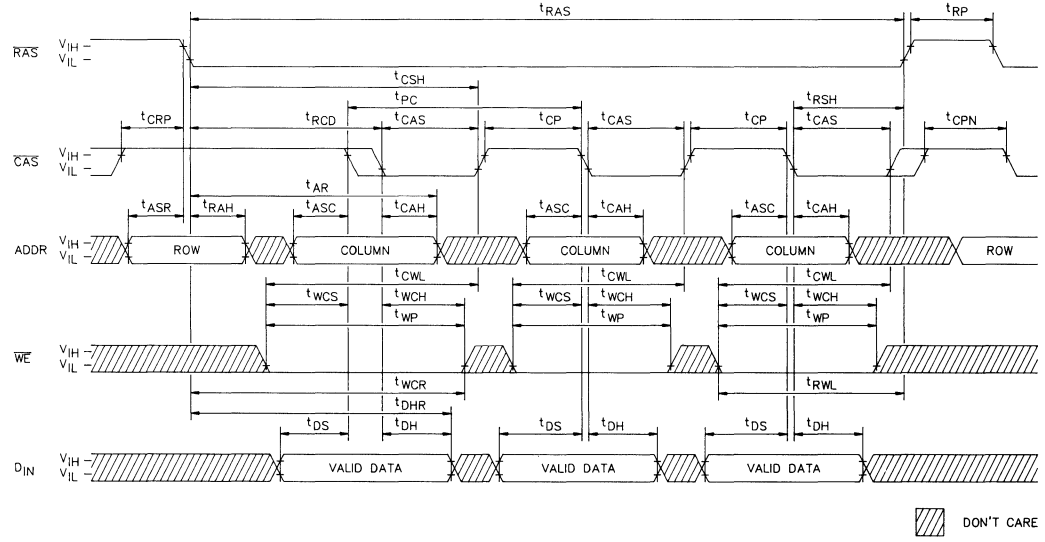
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



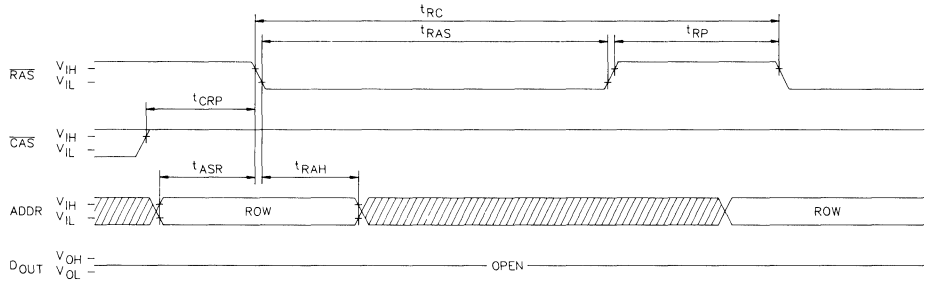
PAGE-MODE READ CYCLE



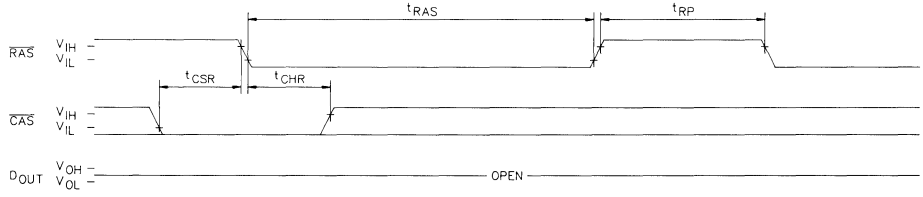
PAGE-MODE EARLY-WRITE CYCLE



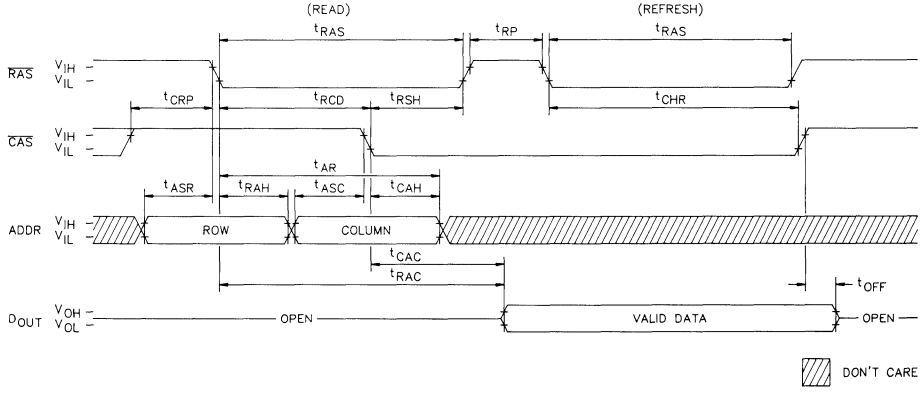
$\overline{RAS}$ ONLY REFRESH CYCLE
(ADDR = A_0 - A_7)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(ADDRESS INPUTS ARE IGNORED)



HIDDEN REFRESH CYCLE

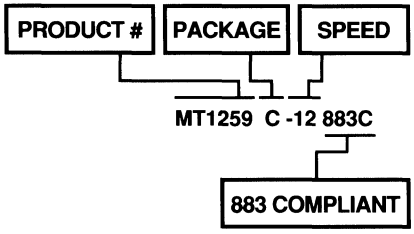


MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan and submit to qualifying activity.	Approved by DESC
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot.	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD 883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD 883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Stabilization Bake	Method 1008, cond. C	100%
10. Temperature Cycle	Method 1010, cond. C	100%
11. Constant Acceleration	Method 2001, cond. E	100%
12. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
13. Initial Electricals	Manufacturer's documented data sheet @ +118°C	100%
14. Marking	Method 2015	100%
15. Burn-in	Method 1015, subgroups A-2 for endpoint 162 hours @ 125°C	100%
16. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +113°C 5% PDA and in-line Group A per method 5005	100%
17. External Visual	Method 2009	100%
18. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
19. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection per Method 5005 (attributes data only)		
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and construction tests	Each package type on each lot
21. Group C	Die related (1000 hr. operating life)	Generic every 13 weeks
22. Group D	Package related test	Each package type Generic every 26 weeks

ORDER INFORMATION

256Kx1, 120ns access, -55°C to +110°C, in Ceramic DIP



The Micron MT1259-883C serves the special needs of the Defense/Aerospace market. The Micron Military Product Assurance Program provides state-of-the-art screened to MIL-STD 883C Class B Revision C Methods 5004 and 5005. All IC's furnished under this program are produces on certified lines and are manufactured, assembled, tested quality controlled in Micron's modern Boise, Idaho USA facility.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

MILITARY DRAM

256K x 4 DRAM

FAST PAGE MODE

ADDITIONAL MILITARY SPECIFICATIONS

- SMD 87676

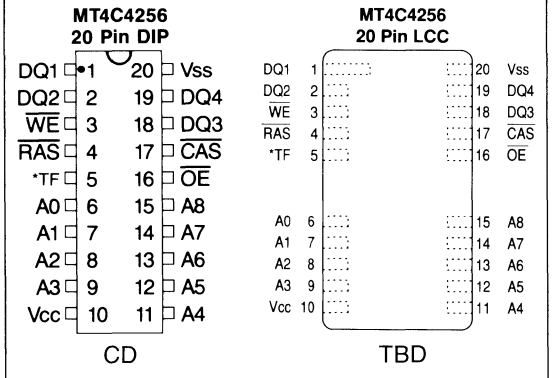
FEATURES

- Industry standard pin-out and timing
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby, 150mW active, typical
- Optional Page Mode access cycle
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 512 cycle refresh distributed across 8ms
- Specifications guaranteed over full military DRAM temperature range (-55°C to +110°C)
- MIL-STD 883C processing

OPTIONS MARKING

- Process Level
  - MIL-STD 883C (-55°C to +110°C) Parts processed to full requirements of MIL-STD 883C, method 5004 and 5005 — 883C
  - MIL-STD 883C with the exception that final electrical testing is performed at 0°C to 70°C — M070
- Timing
  - 100ns access — -10
  - 120ns access — -12
  - 150ns access — -15
- Packages:
  - Ceramic DIP — C
  - Ceramic LCC — EC

PIN ASSIGNMENT (Top View)



*TF = Test Function, ground or leave as a no-connect for normal device operation.

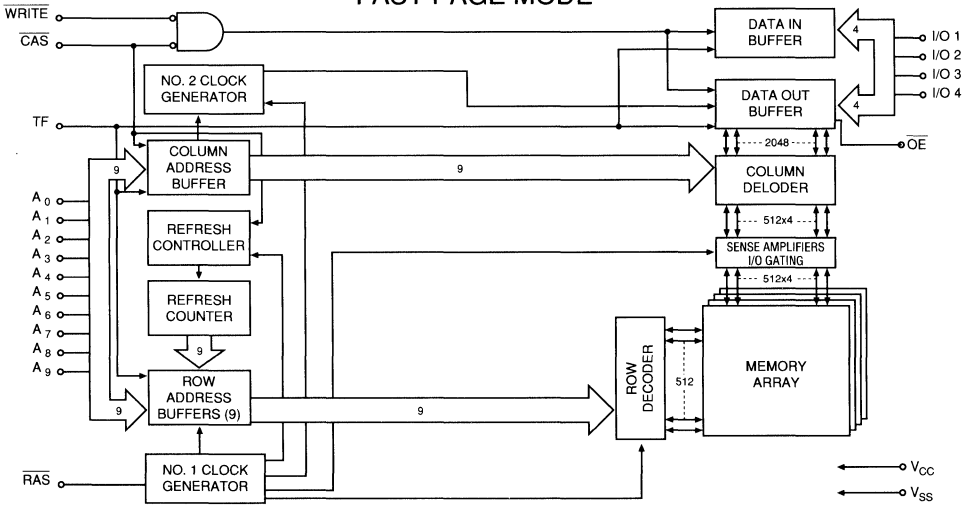
GENERAL DESCRIPTION

The MT4C4265 883C is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	OE	TF	Addresses tR	Addresses tC		NOTES
Standby	H	H	H	H	GND/NC	X	X	High Impedance	
READ	L	L	H	L	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	H	GND/NC	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	H	L	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	H	GND/NC	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	H	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	H	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	H	GND/NC	X	X	High Impedance	
TEST FUNCTION	L	L	H	H	H	ROW	COL	Data Out, Test Funtion Mode	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -1.5V to +7.0V
Storage temperature range ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Lead temperature (soldering 5 sec.) ..... 270°C
Juction temperature (Tj) ..... +175°C
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL PERFORMANCE CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (-55°C ≤ T_C ≤ +110°C, = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: T_{RC} = $T_{RC(MIN)}$)	I_{CC1}		50	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: T_{PC} = $T_{PC(MIN)}$)	I_{CC2}		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		1	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		35	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		35	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T_C ≤ +110°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9), D_{IN}	C_{I1}		5	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Output Capacitance D_{OUT}	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($-55°C \le T_C \le +110°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	190		220		260		ns	
READ-MODIFY-WRITE cycle time	t_{RWC}	220		255		295		ns	
PAGE-MODE READ or WRITE cycle time	t_{PC}	55		70		85		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	14
Access time from $\overline{CAS}$	t_{CAC}		25		30		45	ns	15
Output Enable	t_{OE}		25		25		30	ns	
Access time from column address	t_{AA}		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		65		75	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	t_{RASP}	100	100,000	120	100,000	150	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	80		90		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{CAS}$ precharge time	t_{CPN}	15		20		25		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	t_{CP}	10		15		20		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	10	75	15	90	15	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	10	50	15	60	15	70	ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	50		60		70		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	5		5		5		ns	
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	30	ns	20
Output Disable	t_{OD}		25		25		30	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

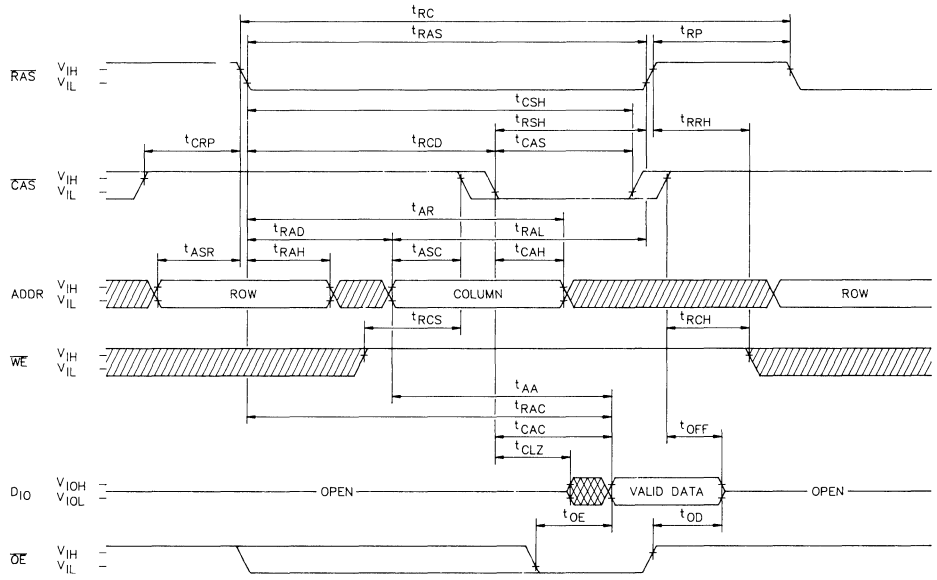
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C ≤ T_C ≤ +110°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	20		25		30		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	
Write command pulse width	^tWP	20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	120		150		185		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	80		100		120		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	65		75		85		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5

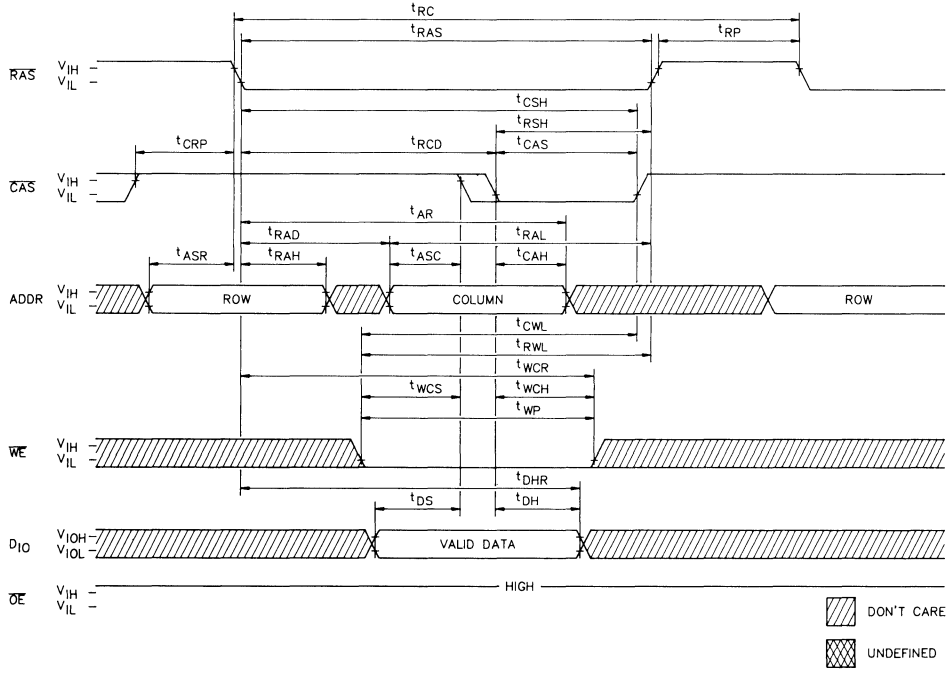
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_C \le 110°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH D_{OUT} goes open. If $\overline{OE}$ is tied permanently low a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.

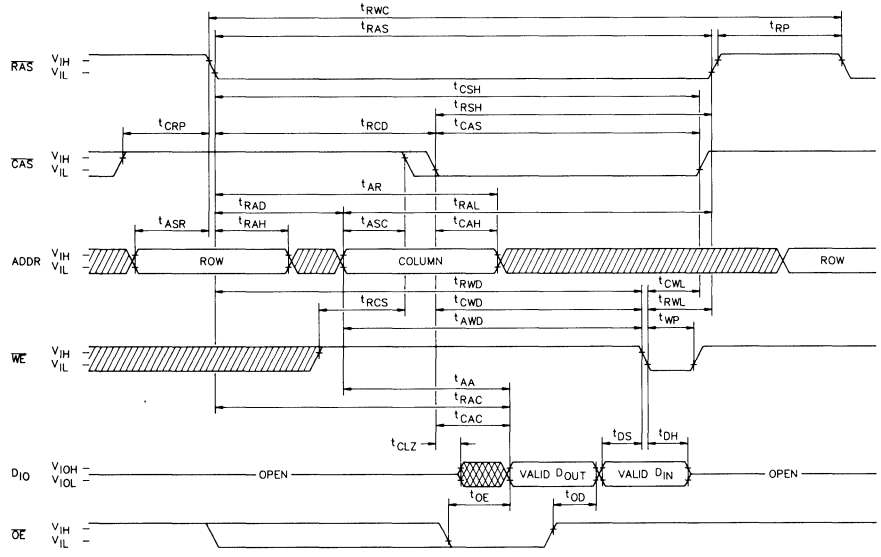
READ CYCLE



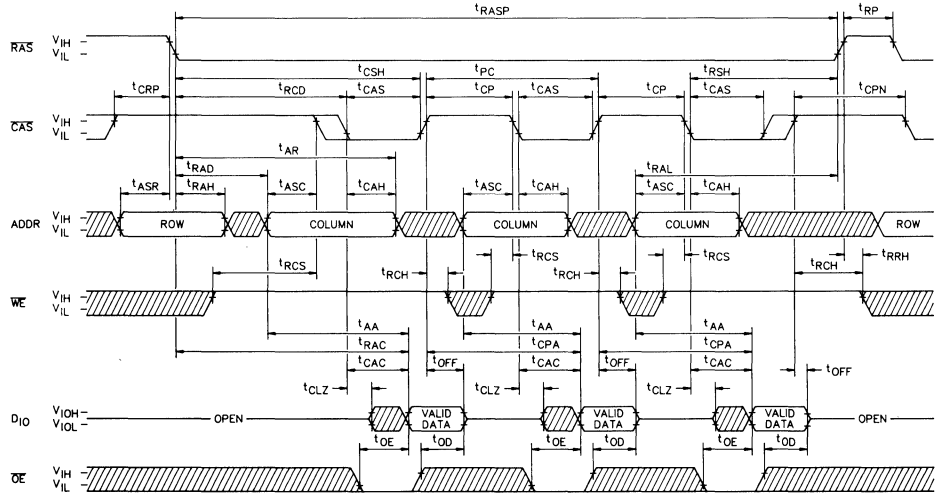
EARLY-WRITE CYCLE



READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



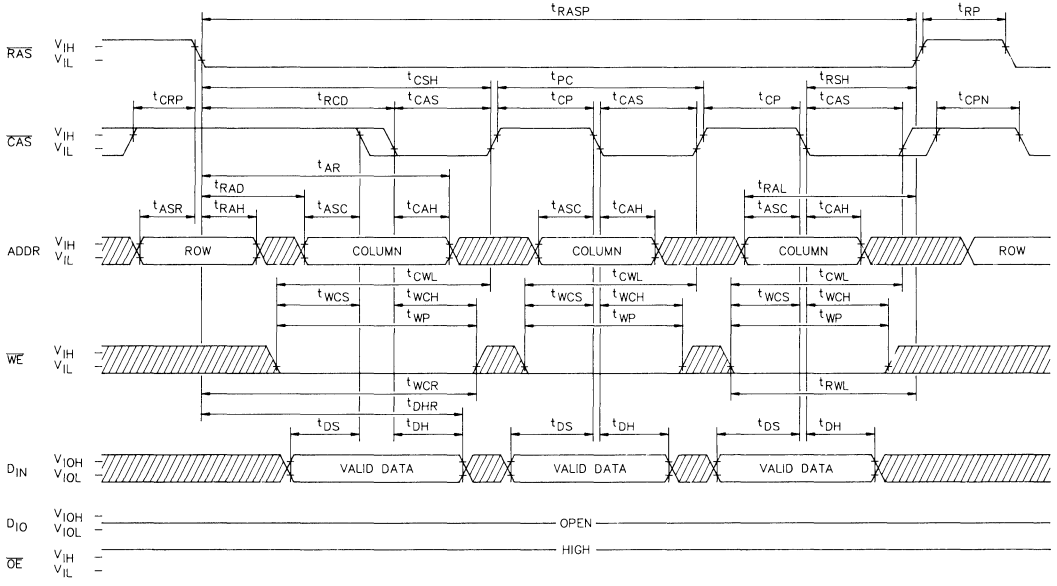
PAGE-MODE READ CYCLE



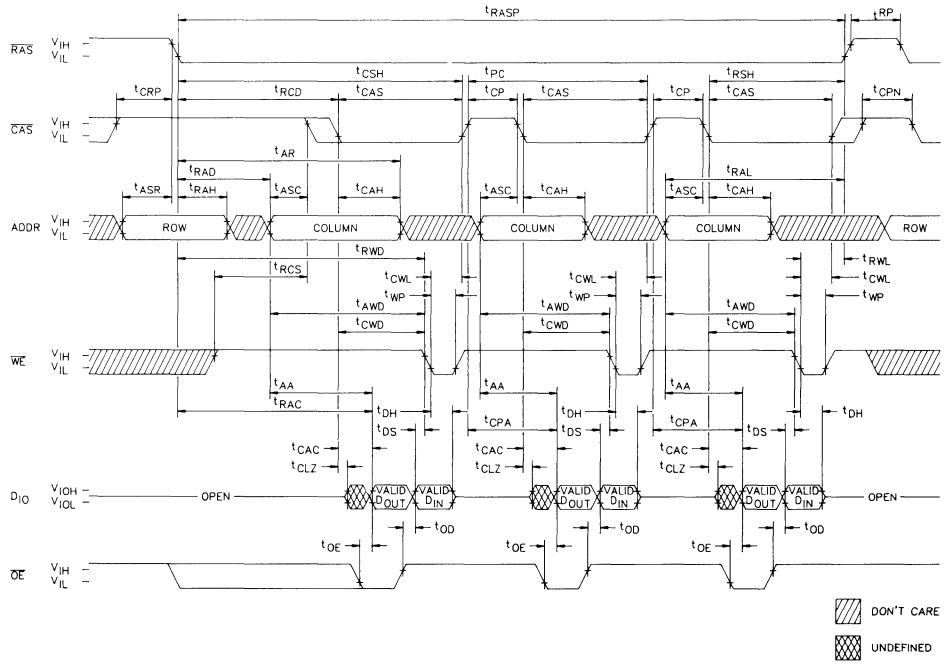
DON'T CARE

UNDEFINED

PAGE-MODE EARLY-WRITE CYCLE

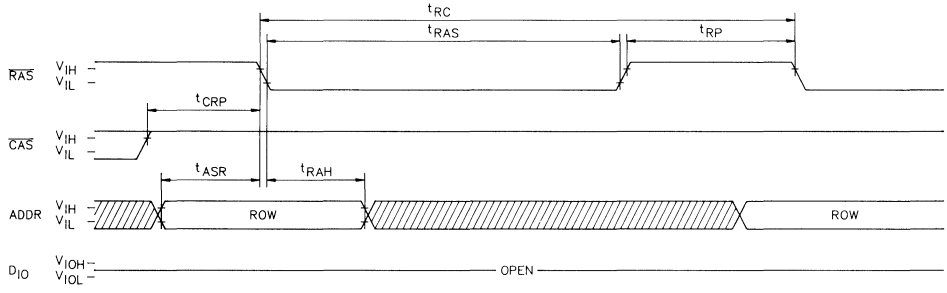


PAGE-MODE READ-WRITE CYCLE



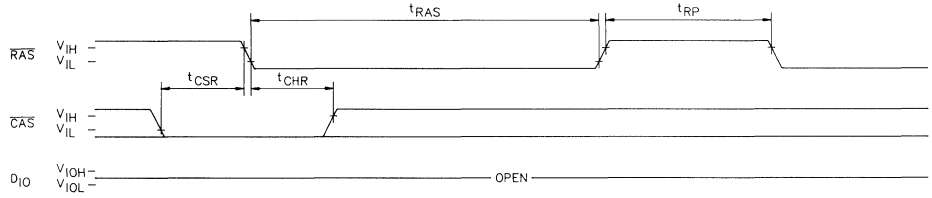
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



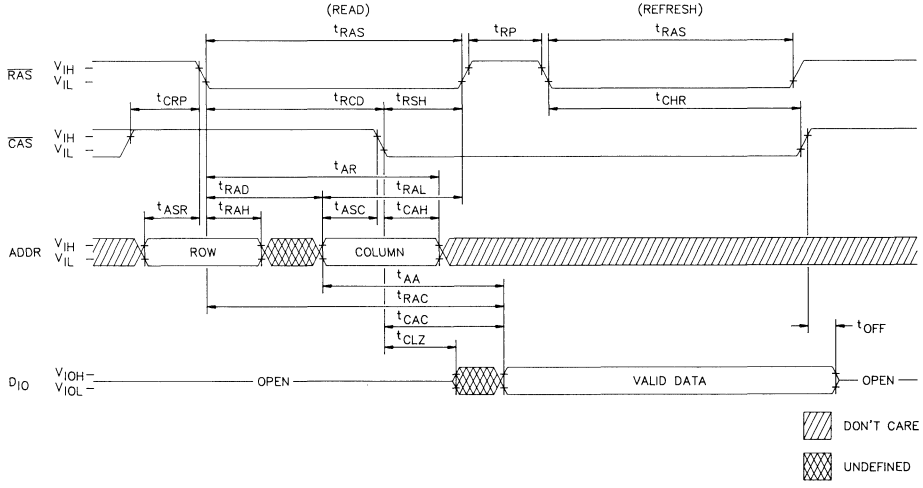
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH); $\overline{OE}$=LOW)[24]



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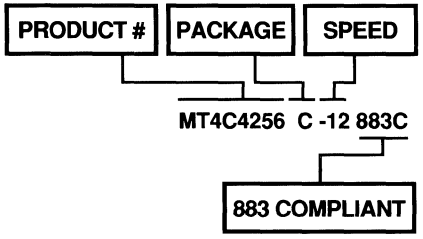
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan and submit to qualifying activity.	Approved by DESC
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot.	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD 883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD 883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Stabilization Bake	Method 1008, cond. C	100%
10. Temperature Cycle	Method 1010, cond. C	100%
11. Constant Acceleration	Method 2001, cond. E	100%
12. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
13. Initial Electricals	Manufacturer's documented data sheet @ +118°C	100%
14. Marking	Method 2015	100%
15. Burn-in	Method 1015, subgroups A-2 for endpoint 162 hours @ 125°C	100%
16. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +113°C 5% PDA and in-line Group A per method 5005	100%
17. External Visual	Method 2009	100%
18. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
19. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection per Method 5005 (attributes data only)		
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and construction tests	Each package type on each lot
21. Group C	Die related (1000 hr. operating life)	Generic every 13 weeks
22. Group D	Package related test	Each package type Generic every 26 weeks

ORDER INFORMATION

256K x 4, 120ns access, -55°C to +110°C, in Ceramic DIP



The Micron MT4C4256-883C serves the special needs of the Defense/Aerospace market. The Micron Military Product Assurance Program provides state-of-the-art screened to MIL-STD 883C Class B Revision C Methods 5004 and 5005. All IC's furnished under this program are produces on certified lines and are manufactured, assembled, tested quality controlled in Micron's modern Boise, Idaho USA facility.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

MILITARY DRAM

1MEG x 1 DRAM

FAST PAGE MODE

ADDITIONAL MILITARY SPECIFICATIONS

- SMD (consult factory for reference number)
- JAN M3510/249

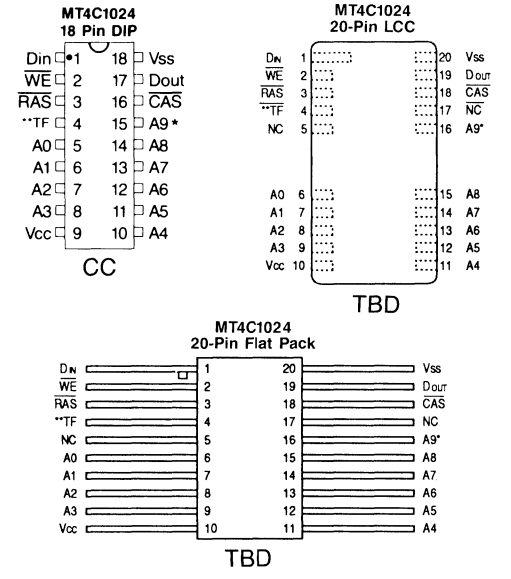
FEATURES

- Industry standard pin-out and timing
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby, 150mW active, typical
- Optional Page Mode access cycle
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden
- 512 cycle refresh distributed across 4ms
- Specifications guaranteed over full military DRAM temperature range (-55°C to +110°C)
- MIL-STD 883C processing

OPTIONS MARKING

- Timing
  - 100ns access -10
  - 120ns access -12
  - 150ns access -15
- Process Level
  - MIL-STD 883C (-55°C to +110°C) 883C
- Packages:
  - Ceramic DIP C
  - Ceramic LCC EC
  - Flat Pack F

PIN ASSIGNMENT (Top View)



*Address not used for $\overline{RAS}$ only refresh
**TF = Test Function, ground or leave as a no-connect for normal device operation.

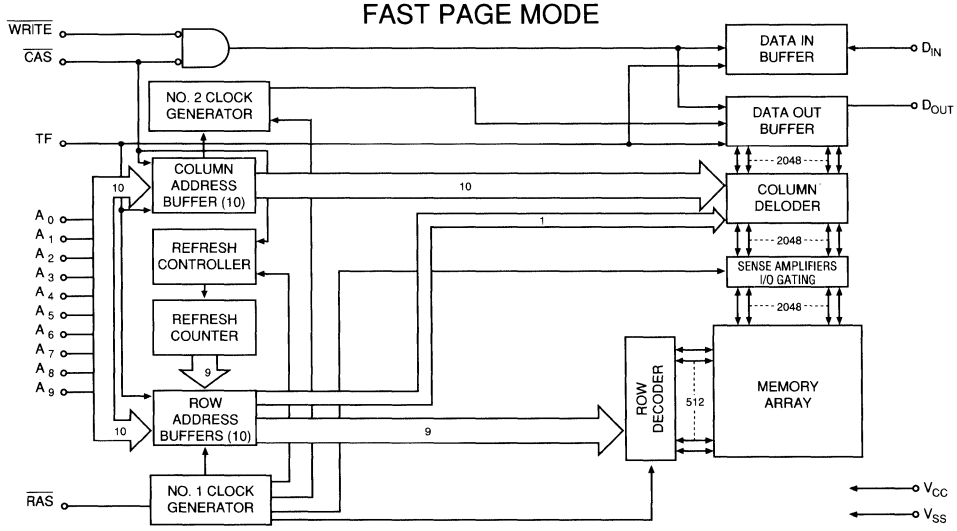
GENERAL DESCRIPTION

The MT4C1024 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



FUNCTIONAL TRUTH TABLE

Function	RAS	CAS	WE	TF	Addresses tR	Addresses tC		NOTES
Standby	H	H	H	GND/NC	X	X	High Impedance	
READ	L	L	H	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
READ-WRITE	L	L	H→L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
PAGE-MODE READ	L	H→L→H	H	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H	L	GND/NC	ROW	COL	Valid Data In, Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	GND/NC	ROW	COL	Valid Data Out, Valid Data In	
RAS ONLY REFRESH	L	H	H	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	GND/NC	X	X	High Impedance	
TEST FUNCTION	L	L	H	H	ROW	COL	Data Out, Test Funtion Mode	

MILITARY DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -1.5V to +7.0V
Storage temperature range ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Lead temperature (soldering 5 sec.) ..... 270°C
Juction temperature (Tj) ..... +175°C
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL PERFORMANCE CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) (-55°C ≤ T_C ≤ +110°C = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		50	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		4	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		1	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		35	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		35	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts. Vcc = 5.5 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT}, 6.5V, Vcc = 5.5 volts)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T_C ≤ +110°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
Refresh cycle time	T_{REF}		4.0	ms	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9)	C_{I1}		6	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, D_{IN}	C_{I2}		7	pF	2
Output Capacitance D_{OUT}	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($-55°C \le T_C \le +110°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	190		220		260		ns	
READ-MODIFY-WRITE cycle time	^tRWC	220		255		295		ns	
PAGE-MODE READ or WRITE cycle time	^tPC	75		90		110		ns	22
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	14
Access time from $\overline{CAS}$	^tCAC		50		60		75	ns	15
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	20		25		25		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	25	50	25	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address set-up time	^tASR	5		5		5		ns	
Row address hold time address delay time	^tRAH	15		20		20		ns	
Column address set-up time	^tASC	5		5		5		ns	
Column address hold time	^tCAH	20		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		80		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	18
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	18
Output buffer turn-off delay	^tOFF	0	40	0	40	0	40	ns	19
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	20
Write command hold time	^tWCH	20		25		30		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

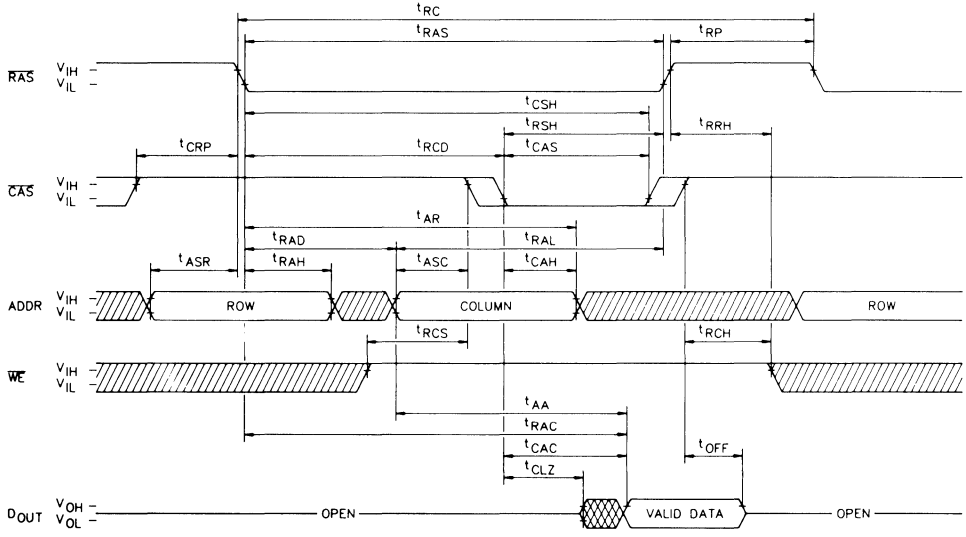
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C ≤ TC ≤ +110°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	
Write command pulse width	^tWP	20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	5		5		5		ns	21
Data-in hold time	^tDH	15		20		25		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		110		135		ns	20
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	30		40		45		ns	20
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		4		4		4	ms	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5

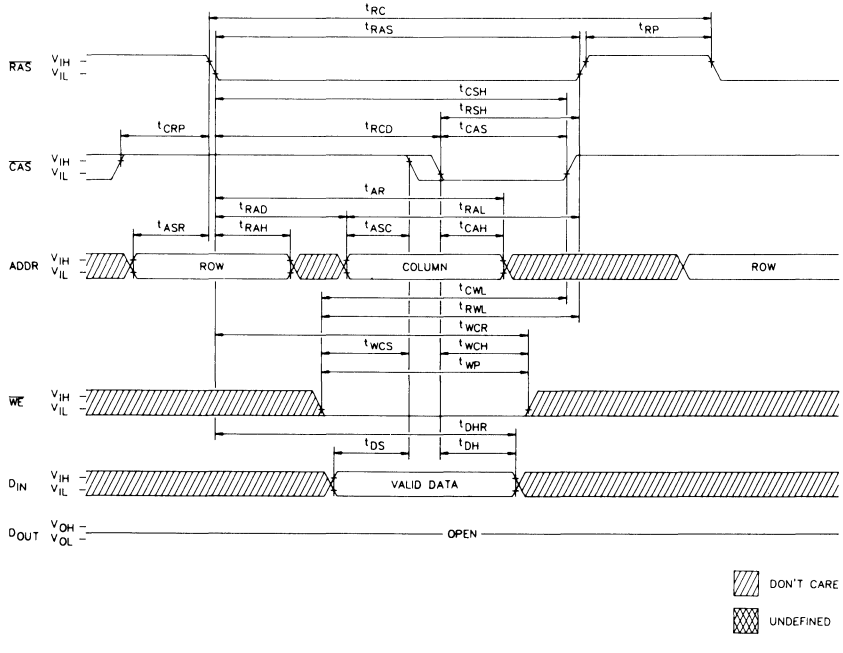
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-55°C ≤ T_C ≤ +110°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Either ^tRCH or ^tRRH must be satisfied for a READ cycle
19. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
20. ^tWCS, ^tRWD, and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min) the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (min), and $^tCWD \geq {}^tCWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
21. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

READ CYCLE

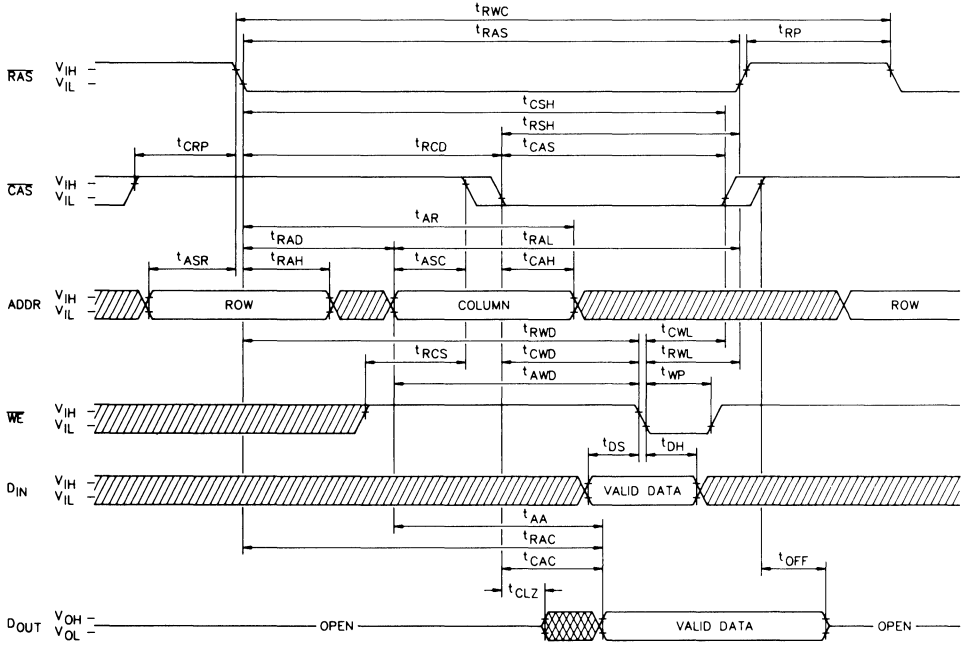


EARLY-WRITE CYCLE

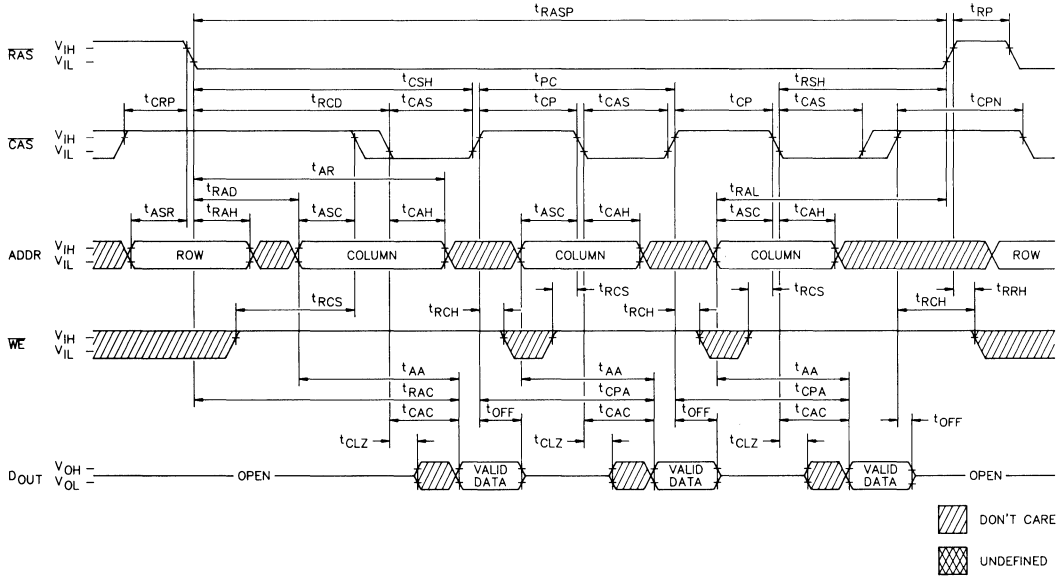


MILITARY DRAM

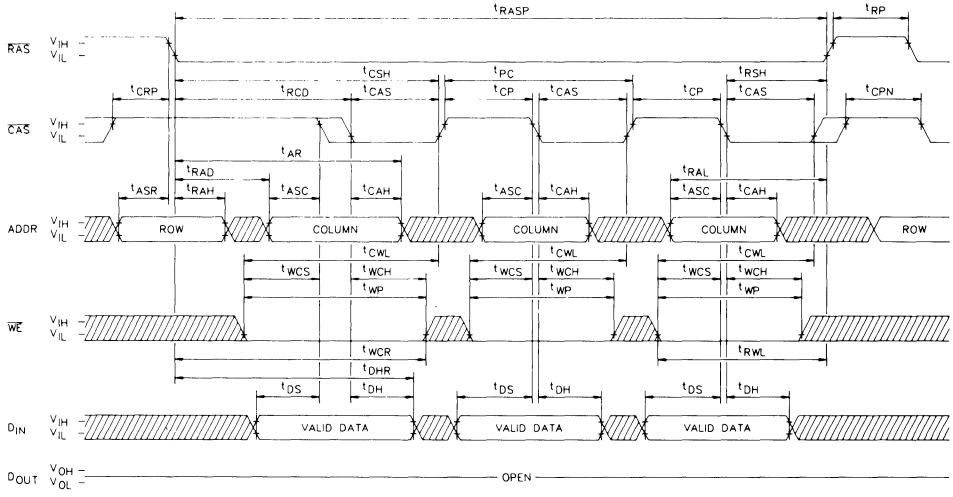
READ-WRITE CYCLE
READ-MODIFY-WRITE CYCLE



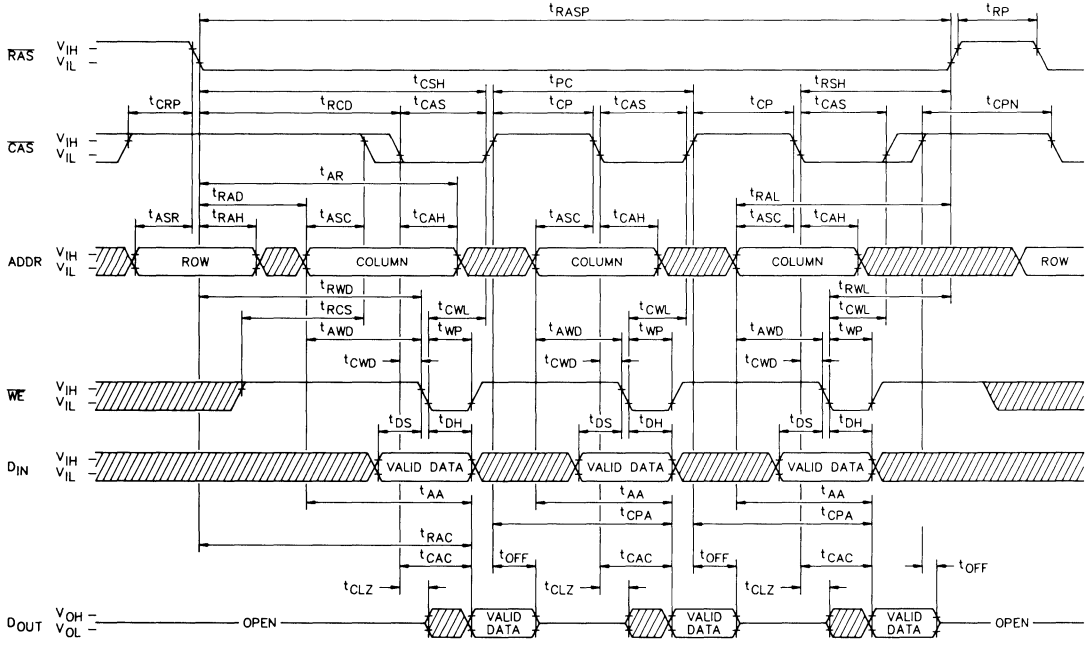
PAGE-MODE READ CYCLE



PAGE-MODE EARLY-WRITE CYCLE

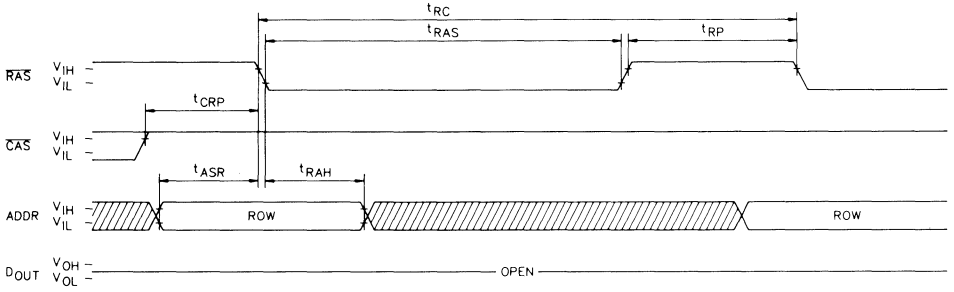


PAGE-MODE READ-WRITE



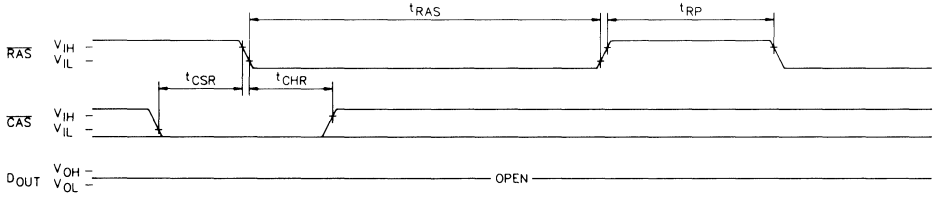
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



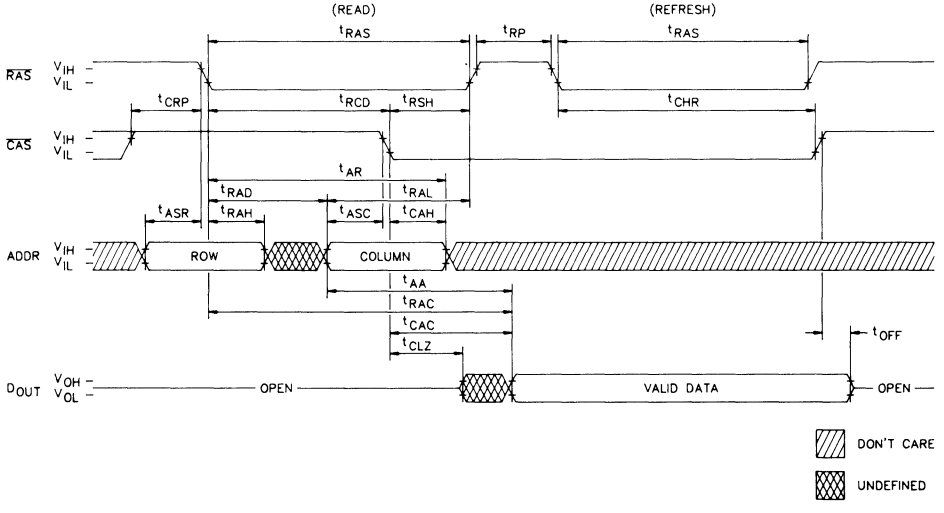
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan and submit to qualifying activity.	Approved by DESC
2. Certification	Manufacturer's QA survey	Self audit
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B. Gross Leak	Method 1014, cond. C	100%
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14. Marking	Method 2015	100%
15. Burn-in	Method 1015, subgroups A-2 for endpoint 162 hours @ 125°C	100%
16. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +113°C 5% PDA and in-line Group A per method 5005	100%
17. External Visual	Method 2009	100%
18. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
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Quality Conformance Inspection per Method 5005 (attributes data only)		
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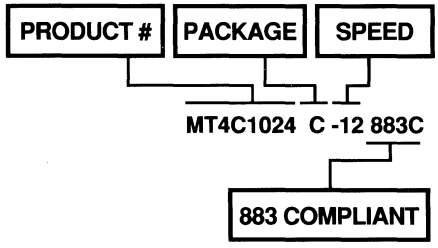
ORDER INFORMATION

1 MEG x 1, 100ns access, -55°C to +110°C, Ceramic DIP



The Micron MT4C1024-883C serves the special needs of the Defense/Aerospace market. The Micron Military Product Assurance Program provides state-of-the-art screened to MIL-STD 883C Class B Revision C Methods 5004 and 5005. All IC's furnished under this program are produces on certified lines and are manufactured, assembled, tested quality controlled in Micron's modern Boise, Idaho USA facility.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

MILITARY VRAM

64K x 4 DRAM with 256 x 4 SAM

ADDITIONAL MILITARY SPECIFICATIONS

- SMD (consult factory for reference number)

FEATURES

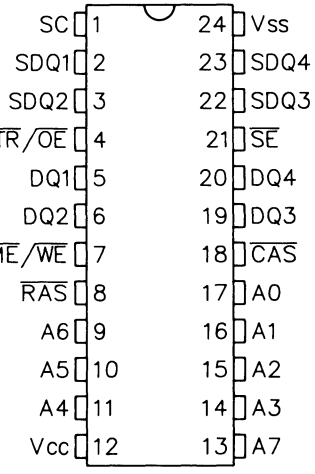
- Industry standard pin-out, timing, and functions
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256 cycle refresh within 4ms
- Optional PAGE MODE access cycles
- Dual port organization: 64K x 4 DRAM port
  256 x 4 SAM port
- Bit MASK-WRITE mode capability on DRAM port
- No refresh required for Serial Access Memory
- Low power: 10mW standby, 150mW active, typical
- Fast access times – 120ns parallel, 40ns serial
- Specifications guaranteed over Full Military DRAM temperature range (-55°C to +110°C)
- MIL-STD-883 Rev. C, Class B

OPTIONS — MARKING

- Process Level
  - MIL-STD-883C (-55°C to +110°C) — 883C
    Parts processed to full requirements of MIL-STD-883C, method 5004 and 5005
  - MIL-STD-883C with the exception that final electrical testing is performed at 0°C to +70°C — M070
- Timing (DRAM, SAM)
  - 120ns, 40ns — -12
  - 150ns, 60ns — -15
  - 200ns, 60ns — -20
- Packages
  - Ceramic DIP (400 mil) — C

PIN ASSIGNMENT (Top View)

24-Pin DIP



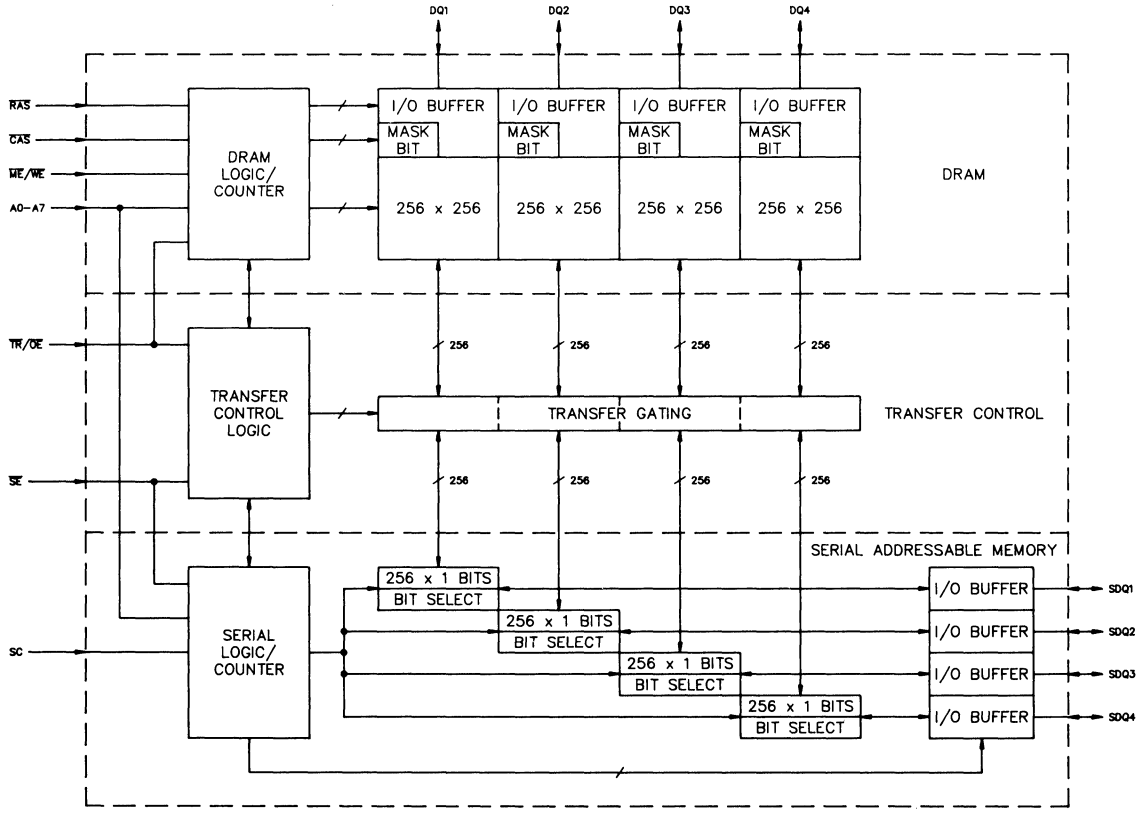
CG

GENERAL DESCRIPTION

The MT42C4064 883C is a high speed, dual port CMOS dynamic random access memory (DPDRAM) containing 262,144 bits. It can be accessed either by a four bit wide DRAM port or by a 256 x 4 bit serial access memory (SAM) port. Data can be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the DPDRAM is functionally identical to the MT4067 64K x 4 bit DRAM. Four 256 bit data registers make up the serial access memory portion of the DPDRAM. Data I/O and internal data transfer is accomplished using three separate bidirectional data paths; the four bit random access I/O port, the four internal 256 bit wide paths between the DRAM and the SAM, and the four bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic. Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs the DPDRAM must be refreshed in order to maintain data. The refresh cycles must be timed so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the DPDRAM is fully static and does not require any refresh.

Figure 1
MT42C4064 BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
1	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
2, 3, 22, 23	SDQ1 - SDQ4	Input/ Output	Serial Data I/O: Input, Output, or high impedance.
4	$\overline{TR}/\overline{OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a high impedance state.
5, 6, 19, 20	DQ1 - DQ4	Input/ Output	DRAM Data I/O: Inputs, Outputs, or high impedance, and/or Mask Data Inputs: For MASK-WRITE cycle only.
7	$\overline{ME}/\overline{WE}$	Input	Mask Enable: If $\overline{ME}/\overline{WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASK-WRITE cycle is performed, or Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = H) or WRITE ($\overline{WE}$ = L) cycle when accessing the DRAM. This includes a DRAM-TO-SAM TRANSFER ($\overline{WE}$ = H) or SAM-TO-DRAM TRANSFER ($\overline{WE}$ = L).
8	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 8 Row Address bits and as a strobe for the MASK ENABLE and TRANSFER functions.
9, 10, 11, 13, 14, 15, 16, 17	A0 to A7	Input	Address Inputs: For the DRAM operation these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select 4 bits out of the 256K available. During TRANSFER operations, A0 to A7 indicate the DRAM row being accessed (when $\overline{RAS}$ goes low) and the SAM start address (when $\overline{CAS}$ goes slow).
12	V_{CC}	Supply	Power Supply: +5 Volts ±10%
18	$\overline{CAS}$	Input	Column Address Strobe: RAS is used to clock in the 8 column address bits and enable the DRAM output buffers ($\overline{TR}/\overline{OE}$ must also be LOW).
21	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a high impedance state. $\overline{SE}$ is also used during a TRANSFER operation to indicate whether a SAM-TO-DRAM TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
24	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

The DPDRAM can be divided into three functional blocks (see Figure 1); the DRAM, the Transfer Control circuitry, and the Serial Access Memory (SAM). All of the operations described below are also shown in the AC Timing Diagrams section of this data sheet as well as summarized in the Functional Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by paranthesis. For example, when discussing transfer operations the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$.*

DRAM OPERATION

The DRAM portion of the DPDRAM is functionally identical to standard 64K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or "don't care" states for the DRAM are specified for the DPDRAM. These conditions are highlighted in the following discussion.

READ/WRITE Cycles

The 16 address bits that are used to select four memory bits from the 65,536 x 4 available are latched into the chip using the A0 -A7, $\overline{RAS}$, and $\overline{CAS}$ inputs. First, the 8 row address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH to LOW. Next, the 8 column address bits are set up on the address inputs and clocked in when $\overline{CAS}$ goes from HIGH to LOW.

For single port DRAMs the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. For the DPDRAM, $(\overline{TR})/\overline{OE}$ is used, when $\overline{RAS}$ goes LOW, to select between an internal transfer operation and a DRAM operation. $(\overline{TR})/\overline{OE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition for a DRAM port READ or WRITE operation.

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1 - DQ4 port. The $(\overline{TR})/\overline{OE}$ input must be LOW to enable the DRAM output port.

For single port DRAMS, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the DPDRAM, $(\overline{ME})/\overline{WE}$ is used, when $\overline{RAS}$ goes LOW, to select between a MASK WRITE cycle and a normal WRITE cycle. If $(\overline{ME})/\overline{WE}$ is LOW at the $\overline{RAS}$ HIGH to LOW transition a MASK WRITE operation is selected. For a normal DRAM WRITE operation, $(\overline{ME})/\overline{WE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition. $(\overline{ME})/\overline{WE}$ is a "don't care" at the $\overline{RAS}$ HIGH to LOW transition for a DRAM READ cycle.

If $(\overline{ME})/\overline{WE}$ is LOW when $\overline{CAS}$ goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1 - DQ4 port will be written into the selected memory cells. If $\overline{ME}/(\overline{WE})$ is LOW when $\overline{RAS}$ goes LOW the input data will be "masked" before being stored in the DRAM.

The DPDRAM can perform all the normal DRAM cycles including EARLY-WRITE, LATE-WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE-MODE READ, PAGE-MODE WRITE, and PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in this data sheet for more details on these operations.

MASK-WRITE

If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH to LOW transition, the data (mask data) present on the DQ1 - DQ4 inputs will be written into the bit mask data register. The mask data acts as an individual write enable for each of the four DQ1 - DQ4 pins. If a LOW (logic 0) is written to a mask data register bit the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1 - DQ4 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. Since the mask data register is reset (to all 1's) at the end of every MASK-WRITE cycle, new mask data must be supplied at the beginning of each MASK-WRITE cycle. An example of a typical MASK-WRITE cycle is shown in Figure 2.

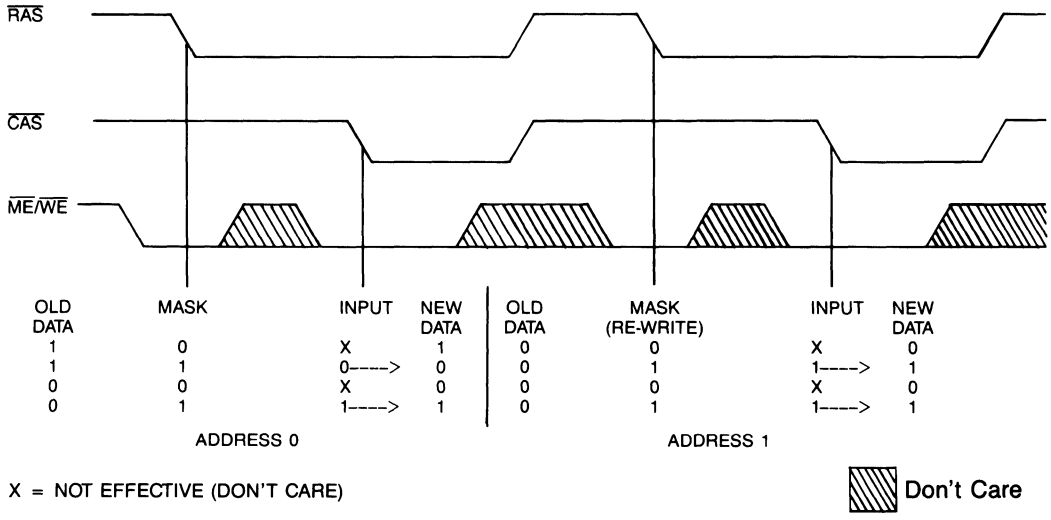


Figure 2
MT42C4064 Bit MASK-WRITE

REFRESH

The MT42C4064 supports $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN types of refresh cycles. All 256 row address combinations must be accessed within 4ms. For the $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh mode the row addresses are generated internally and the user need not supply them as he must in $\overline{RAS}$ ONLY refresh. $\overline{TR}$/($\overline{OE}$) must be HIGH when $\overline{RAS}$ goes LOW for the $\overline{RAS}$ ONLY and $\overline{CAS}$-BEFORE-$\overline{RAS}$ types of refresh cycles. Any READ, WRITE, or TRANSFER operation also refreshes the DRAM row that is being accessed.

TRANSFER OPERATION

DRAM-TO-SAM TRANSFER (READ TRANSFER)

A TRANSFER operation is initiated when $\overline{TR}/(\overline{OE})$ is LOW at $\overline{RAS}$ (HIGH to LOW) time. $(\overline{ME})/\overline{WE}$ indicates the direction of the transfer and must be HIGH as $\overline{RAS}$ goes LOW for a DRAM-TO-SAM TRANSFER. In this case, the row address bits indicate the four 256 bit DRAM rows that are to be transferred to the four SAM data registers and the column address bits indicate the start address of the next SERIAL OUTPUT cycle from the SAM data registers. $\overline{RAS}$ and $\overline{CAS}$ are used to strobe the address bits into the part. To complete the TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while $\overline{RAS}$ and $\overline{CAS}$ are still LOW. The 1024 bits of DRAM data are then written into the SAM data registers and the serial shift start address is stored in an internal 8 bit register. There must be no rising edges on the Serial Clock (SC) input while the transfer is taking place (refer to the AC timing diagrams). TRANSFER cycles are the only time when SC must be synchronized with the DRAM $\overline{RAS}$ and $\overline{CAS}$ timing. If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation.

SAM-TO-DRAM TRANSFER (WRITE TRANSFER)

The SAM-TO-DRAM TRANSFER operation is identical to the DRAM-TO-SAM TRANSFER described above except that $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row that the SAM data registers will be written to and the column address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. If $\overline{SE}$ is HIGH when $\overline{RAS}$ goes LOW, a SERIAL INPUT MODE ENABLE cycle is performed.

SAM OPERATION

SERIAL INPUT/OUTPUT MODE CONTROL

The SAM port is automatically placed in the serial output mode after a DRAM-TO-SAM TRANSFER operation. Conversely, after a SAM-TO-DRAM TRANSFER the SAM port will be in the serial input mode.

SERIAL INPUT MODE ENABLE (PSEUDO WRITE TRANSFER)

It is possible to change the direction of the SAM port from output to input without performing a SAM-TO-DRAM TRANSFER. This operation, called a SERIAL INPUT MODE ENABLE cycle, is simply a SAM-TO-DRAM TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the data registers will be ready to accept input data.

The only way to put the SAM port in the serial output mode is to do a DRAM-TO-SAM TRANSFER.

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM data register contents will start at the serial start address that was loaded during the DRAM-TO-SAM TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the four bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW to HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW, and will wrap around to location 0 after reaching its maximum count of 255.

SC is also used to clock in data when the device is in the serial input mode. As in the serial output operation, the contents of the serial address register, which was loaded when the serial input mode was enabled, will determine the serial address that the first bit will be written. $\overline{SE}$ acts as an enable for serial data input and must be LOW for normal serial input. If $\overline{SE}$ is HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address register is incremented with every L → H transition of SC, regardless of the logic level on the $\overline{SE}$ input.

FUNCTIONAL TRUTH TABLE

DRAM Operations (SC, $\overline{SE}$, and SDQ1 — SDQ4 are don't care)

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{ME}/\overline{WE}$		$\overline{TR}/\overline{OE}$		Addresses		DQ1 to DQ4	Notes
			tR*	tC*	tR*	tC*	tR*	tC*		
Standby	H	H	X	X	X	X	X	X	High Impedance	
READ	L	L	X	H	H	H→L	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	H	L	H	X	ROW	COL	Data In	1
MASK-WRITE	H→L	L	L	L	H	X	ROW	COL	Mask Data In, Valid Data In	
READ-WRITE	L	L	H	H→L	H	L→H	ROW	COL	Valid Data Out,	1
PAGE-MODE READ	L	H→L→H, H→L→H	H	H	H	H→L	ROW	COL	Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	H	L	H	X	ROW	COL	Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H, H→L→H	H	H→L	H	L→H	ROW	COL	Valid Data Out, Valid Data In	1
$\overline{RAS}$ ONLY REFRESH	L	H	X	n/a	H	n/a	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	X	H	H	L	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	X	X	H	X	X	X	High Impedance	

TRANSFER Operations (DQ1 — DQ4 are don't care)

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{ME}/\overline{WE}$		$\overline{TR}/\overline{OE}$		Addresses		SC	$\overline{SE}$	SDQ1 to SDQ4	Notes
			tR*	tC*	tR*	tC*	tR*	tC*				
DRAM-TO-SAM TRANSFER	L	L	H	X	L	L	ROW	SSA**	X	X	X	2
SAM-TO-DRAM TRANSFER	L	L	L	X	L	X	ROW	SSA**	X	L	X	3
SERIAL INPUT MODE ENABLE	L	L	L	X	L	X	ROW	SSA**	X	H	X	4

* tR = when $\overline{RAS}$ goes from HIGH to LOW
tC = when $\overline{CAS}$ goes from HIGH to LOW
** SSA = SAM Start Address, the serial address that the next serial input or output cycle will start with.

Notes: 1. Any type of WRITE cycle may also be a MASK-WRITE cycle.
2. The SAM will be in a SERIAL OUTPUT mode after a DRAM-TO-SAM TRANSFER.
3. The SAM will be in a SERIAL INPUT mode after a SAM-TO-DRAM TRANSFER.
4. The SAM will be put in the SERIAL INPUT mode but the SAM-TO-DRAM TRANSFER will not occur.

Serial I/O Operations (RAS, CAS, ME/WE, TR/OE, and DQ1 - DQ4 are don't care)

Function	SC	SE	SDQ1 — SDQ4	Notes
SERIAL OUTPUT	L→H	L	Valid Data Out	5
SERIAL INPUT	L→H	L	Valid Data In	6

Notes: 5. The SAM must be in the SERIAL OUTPUT mode.
6. The SAM must be in the SERIAL INPUT mode.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss ..... -1.5V to +7.0V
Operating Temperature Range ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Lead Temperature (soldering 5 sec.) ..... 300°C
Juction Temperature Tj) ..... +150°C
Short Circuit Output Current 50mA
Thermal Resistance (θjc) 24 pin DIP .....

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc Supply Voltage	Vcc	4.5	5.5	V	1
Vss power supply and signal reference	Vss	0.0	0.0	V	1
Operating case temperature	Tc	-55	+110	°C	
Input High (Logic 1) Voltage, All Inputs	VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(Notes 3, 4, 5) (Vcc = 5.0V ± 10%)

ITEM	TEST	NOTES	SYMBOL	ALT. SYMBOL	CONDITIONS -55°C ≤ Tc ≤ +110°C	DEVICE TYPE	GROUP A SUBGROUPS	LIMITS MIN	LIMITS MAX	UNIT
1	High level output voltage	1	VOH		Vcc = 4.5V, IOH = 5mA VIL = 0.8V, VIH = 2.4V	All	1, 2, 3	2.4		V
2	Low level output voltage	1	VOL		Vcc = 4.5V, IOL = -5mA VIL = 0.8V, VIH = 2.4V	All	1, 2, 3		0.4	V
3	High level input leakage current		IIH		Vcc = 5.5V, VI = 6.5V	All	1, 2, 3		10	µA
4	Low level input leakage current		IIL		Vcc = 5.5V, VI = 0.0V	All	1, 2, 3		-10	µA
5	Output leakage current		IOZ		Vcc = 5.5V, outputs are disabled, 0V ≤ VOUT ≤ Vcc	All	1, 2, 3	-10	10	µA

CAPACITANCE

ITEM	TEST	NOTES	SYMBOL	ALT. SYMBOL	CONDITIONS -55°C ≤ Tc ≤ +110°C	DEVICE TYPE	GROUP A SUBGROUPS	LIMITS MIN	LIMITS MAX	UNIT
1	Input capacitance (A0 - A7, DIN)	18	C_{I1}		Sampled parameter	All	4		5	pF
2	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, SC, $\overline{SE}$	18	C_{I2}		Sampled parameter	All	4		7	pF
3	Input capacitance (A0 - A7, DOUT)	18	C_O		Sampled parameter	All	4		7	pF

NOTES

1. All voltages referenced to VSS.
2. ICC is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms static refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-55°C ≤ T_C ≤ +110°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (max).
10. If $\overline{CAS}$ = VIH, DRAM data output is high impedance.
11. If $\overline{CAS}$ = VIL, DRAM data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is con trolled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and to $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min) the cycle is an EARLY-WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $^tCWD \geq ^tCWD$ (min) and $^tRWD \geq ^tRWD$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back toVIH) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and VCC = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, DOUT will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCP. Note 8 applies to determine valid data out.
20. Includes the $\overline{OE}$ delay time (25ns for the -12, 30ns for the -15, and 45ns for the -20).
21. During a READ cycle if $\overline{OE}$ is low then taken high (VIH) DOUT goes open. If $\overline{OE}$ is tied permanently low a READ-MODIFY-WRITE operation is not possible.
22. Enables on-chip refresh and address counters.
23. TRANSFER Command means that $\overline{TR}/(\overline{OE})$ is LOW when $\overline{RAS}$ goes LOW.
24. NON-TRANSFER Command means that $\overline{TR}/(\overline{OE})$ is HIGH when $\overline{RAS}$ goes LOW.
25. Measured with a load equivalent to 2 TTL gates and 50pF.
26. The parameter is a "conditionally" guaranteed parameter that is specified to aid with device application. It is not directly verified by a specific test but is used, along with several other parameters, in the performance verification of other attributes..

DC ELECTRICAL CHARACTERISTICS

(Notes 3, 4, 5) (V_{CC} = 5.0V ± 10%)

ITEM	TEST	NOTES	SYMBOL	ALT. SYMBOL	CONDITIONS -55°C ≤ Tc ≤ +110°C	DEVICE TYPE	GROUP A SUBGROUPS	LIMITS MIN	LIMITS MAX	UNIT
1	Average operating current during READ or WRITE cycles.	4	I_{CC1}		$\overline{RAS}$ and $\overline{CAS}$ = cycling, ^tRC = ^tRC (min), SAM in Standby	All	1, 2, 3		40	mA
2	Average operating current during PAGE-MODE READ or WRITE cycles.	4	I_{CC2}		$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, ^tPC = ^tPC (min), SAM in Standby	All	1, 2, 3		40	mA
3	Standby current: TTL input levels		I_{CC3}		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles, SAM in Standby	All	1, 2, 3		10	mA
4	Standby current: CMOS input levels		I_{CC4}		$\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles. All other inputs at V_{CC} -0.2V or V_{SS} +0.2V, SAM in Standby	All	1, 2, 3		6	mA
5	Refresh current: $\overline{RAS}$ only refresh		I_{CC5}		$\overline{RAS}$ = Cycling, $\overline{CAS}$ = V_{IH}, SAM in Standby	All	1, 2, 3		30	mA
6	Refresh current: $\overline{CAS}$-before-$\overline{RAS}$ refresh	5	I_{CC6}		$\overline{RAS}$ and $\overline{CAS}$ = cycling, SAM in Standby	All	1, 2, 3		30	mA
7	Data transfer current: DRAM-TO-SAM or SAM-TO-DRAM		I_{CC7}		Data transfer cycle, SAM in Standby	All	1, 2, 3		60	mA
8	Average operating current during READ or WRITE cycles.	4	I_{CC8}		$\overline{RAS}$ and $\overline{CAS}$ = cycling, ^tRC = ^tRC (min), SAM active, ^tSC = ^tSC (min)	All	1, 2, 3		60	mA
9	Average operating current during PAGE-MODE READ or WRITE cycles.	4	I_{CC9}		$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, ^tPC = ^tPC (min), SAM active, ^tSC = ^tSC (min)	All	1, 2, 3		60	mA
10	Standby current: TTL input levels		I_{CC10}		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles, SAM active, ^tSC = ^tSC (min)	All	1, 2, 3		30	mA
11	Standby current: CMOS input levels		I_{CC11}		$\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles. All other inputs at V_{CC} -0.2V or V_{SS} +0.2V, SAM active, ^tSC = ^tSC (min)	All	1, 2, 3		25	mA
12	Refresh current: $\overline{RAS}$ only refresh		I_{CC12}		$\overline{RAS}$ = Cycling, $\overline{CAS}$ = V_{IH}, SAM active, ^tSC = ^tSC (min)	All	1, 2, 3		50	mA
13	Refresh current: $\overline{CAS}$-before-$\overline{RAS}$ refresh	5	I_{CC13}		$\overline{RAS}$ and $\overline{CAS}$ = cycling, Sam active, ^tSC = ^tSC (min)	All	1, 2, 3		50	mA

DRAM TIMING PARAMETERS

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 10, 11, 17) (V_{CC} = 5.0V ± 10%)

ITEM	TEST	NOTES	SYMBOL	ALT. SYMBOL	CONDITIONS -55°C ≤ Tc ≤ +110°C	DEVICE TYPE	GROUP A SUBGROUPS	LIMITS MIN	LIMITS MAX	UNIT
1	Random READ or WRITE cycle time	6, 7	^tRC	$^tc(RD)$ $^tc(W)$	All cycle times assume ^tT = 5ns.	-12 -15 -20	9, 10, 11	220 260 300		ns
2	READ-MODIFY-WRITE cycle time	20, 21	^tRWC	$^tc(RDW)$		-12 -15 -20	9, 10, 11	295 345 400		ns
3	PAGE-MODE READ-MODIFY-WRITE cycle time	6, 7, 26	^tPRWC	$^tc(PRDW)$		-12 -15 -20	9, 10, 11	150 175 200		ns
4	PAGE-MODE READ or WRITE cycle time	6, 7, 26	^tPC	$^tc(PRD)$ $^tc(PW)$		-12 -15 -20	9, 10, 11	90 110 200		ns
5	Access time from $\overline{RAS}$	7, 8	^tRAC	$^ta(R)$	CL = 100pF	-12 -15 -20	9, 10, 11	120 150 200		ns
6	Access time from $\overline{CAS}$	7, 9	^tCAC	$^ta(C)$	CL = 100pF	-12 -15 -20	9, 10, 11	60 75 100		ns
7	$\overline{RAS}$ pulse width		^tRAS	$^tw(RL)$		-12 -15 -20	9, 10, 11	120 150 200	10,000 10,000 10,000	ns
8	$\overline{RAS}$ pulse width (PAGE-MODE)		^tRASP	$^tw(RLP)$		-12 -15 -20	9, 10, 11	120 150 200	100,000 100,000 100,000	ns
9	$\overline{RAS}$ hold time		^tRSH	$^th(CLRH)$		-12 -15 -20	9, 10, 11	60 75 100		ns
10	$\overline{RAS}$ precharge time		^tRP	$^tw(RH)$		-12 -15 -20	9, 10, 11	90 100 100		ns
11	$\overline{CAS}$ pulse width		^tCAS	$^tw(CL)$		-12 -15 -20	9, 10, 11	60 75 100	10,000 10,000 10,000	ns
12	$\overline{CAS}$ hold time	26	^tCSH	$^th(RLCH)$		-12 -15 -20	9, 10, 11	120 150 200		ns
13	$\overline{CAS}$ precharge time	26	^tCPN	$^tw(CH)$		-12 -15 -20	9, 10, 11	20 25 35		ns
14	$\overline{CAS}$ precharge time (PAGE-MODE)	19, 26	^tCP	$^tw(CH)$		-12 -15 -20	9, 10, 11	20 25 35		ns
15	$\overline{RAS}$ to $\overline{CAS}$ delay	13	^tRCD	^tRLCL		-12 -15 -20	9, 10, 11	20 20 25	60 75 85	ns
16	$\overline{CAS}$ to $\overline{RAS}$ precharge time	26	^tCRP	^tCHRL		-12 -15 -20	9, 10, 11	10 10 10		ns

DRAM TIMING PARAMETERS (Continued)

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 10, 11, 17) (V_{CC} = 5.0V ± 10%)

ITEM	TEST	NOTES	SYMBOL	ALT. SYMBOL	CONDITIONS -55°C ≤ Tc ≤ +110°C	DEVICE TYPE	GROUP A SUBGROUPS	LIMITS MIN	LIMITS MAX	UNIT
17	Row address set-up time		^tASR	$^tsu(RA)$	All cycle times assume ^tT = 5ns.	-12 -15 -20	9, 10, 11	0 0 0		ns
18	Row address hold time		^tRAH	$^th(RA)$		-12 -15 -20	9, 10, 11	15 15 20		ns
19	Column address set-up time		^tASC	$^tsu(CA)$		-12 -15 -20	9, 10, 11	0 0 0		ns
20	Column address hold time		^tCAH	$^th(CLCA)$		-12 -15 -20	9, 10, 11	20 25 35		ns
21	Column address hold time (referenced to $\overline{RAS}$)		^tAR	$^th(RLCA)$		-12 -15 -20	9, 10, 11	70 80 100		ns
22	READ command set-up time		^tRCS	$^tsu(RD)$		-12 -15 -20	9, 10, 11	0 0 0		ns
23	READ command hold time (referenced to $\overline{CAS}$)	14, 26	^tRCH	$^th(CHRD)$		-12 -15 -20	9, 10, 11	0 0 0		ns
24	READ command hold time (referenced to $\overline{RAS}$)	26	^tRRH	$^th(RHRD)$		-12 -15 -20	9, 10, 11	0 0 0		ns
25	WE command set-up time	16	^tWCS	$^tsu(WCL)$		-12 -15 -20	9, 10, 11	0 0 0		ns
26	WRITE command hold time		^tWCH	$^th(CLW)$		-12 -15 -20	9, 10, 11	25 30 45		ns
27	WRITE command hold time (referenced to RAS)		^tWCR	$^th(RLW)$		-12 -15 -20	9, 10, 11	80 90 120		ns
28	WRITE command pulse width		^tWP	$^tw(W)$		-12 -15 -20	9, 10, 11	25 30 45		ns
29	WRITE command to RAS lead time		^tRWL	$^th(WRH)$		-12 -15 -20	9, 10, 11	30 35 50		ns
30	WRITE command to $\overline{CAS}$ lead time		^tCWL	$^th(WCH)$		-12 -15 -20	9, 10, 11	30 35 50		ns
31	Data-in set-up time	15	^tDS	$^tsu(D)$		-12 -15 -20	9, 10, 11	0 0 10		ns
32	Data-in hold time (referenced to $\overline{CAS}$)	15	^tDH	$^th(CLD)$		-12 -15 -20	9, 10, 11	20 25 50		ns

DRAM TIMING PARAMETERS (Continued)

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 10, 11, 17) (V_{CC} = 5.0V ± 10%)

ITEM	TEST	NOTES	SYMBOL	ALT. SYMBOL	CONDITIONS -55°C ≤ T_C ≤ +110°C	DEVICE TYPE	GROUP A SUBGROUPS	LIMITS MIN	LIMITS MAX	UNIT
33	Data-in hold time (referenced to $\overline{ME}/\overline{WE}$		^tDH	$^th(WLD)$	All cycle times assume ^tT = 5ns.	-12 -15 -20	9, 10, 11	20 25 50		ns
34	Data-in hold time (referenced to $\overline{RAS}$		^tDHR	$^th(RLD)$		-12 -15 -20	9, 10, 11	80 90 120		ns
35	$\overline{CAS}$ to $\overline{WE}$ delay	16,20	^tCWD	^tCLWL		-12 -15 -20	9, 10, 11	80 95 130		ns
36	$\overline{RAS}$ to $\overline{WE}$ delay	16, 20	^tRWD	^tRLWL		-12 -15 -20	9, 10, 11	150 185 220		ns
37	$\overline{ME}/\overline{WE}$ (Mask Write Mode) to $\overline{RAS}$ set-up time	26	^tWSR	$^tsu(WE)$		-12 -15 -20	9, 10, 11	0 0 0		ns
38	$\overline{ME}/\overline{WE}$ (Mask Write Mode) to $\overline{RAS}$ hold time	26	^tRWH	$^th(WE)$		-12 -15 -20	9, 10, 11	10 15 20		ns
39	Mask Data (DQ__) to $\overline{RAS}$ set-up time	26	^tMS	$^tsu(W)$		-12 -15 -20	9, 10, 11	0 0 0		ns
40	Mask Data (DQ__) to $\overline{RAS}$ hold time		^tMH	$^th(W)$		-12 -15 -20	9, 10, 11	20 25 40		ns
41	Transition time (rise or fall)	26	^tT	^tT		-12 -15 -20	9, 10, 11	3 3 3	50 50 50	ns
42	Refresh period (256 cycle)		^tREF	$^tc(RF)$	All 256 row addresses must be accessed.	-12 -15 -20	9, 10, 11		4 4 4	ms
43	$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)		^tCSR	$^tsu(RCR)$		12 -15 -20	9, 10, 11		10 10 10	ns
44	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh	22	^tCHR	$^th(RRC)$		-12 -15 -20	9, 10, 11		25 30 40	ns
45	$\overline{CAS}$ to output in low-Z	26	^tCLZ			-12 -15 -20	9, 10, 11		5 5 10	ns
46	Output buffer turn-off delay (referenced from $\overline{CAS}$)	12	^tOFF	$^tdis(CH)$		-12 -15 -20	9, 10, 11	0 0 0	25 30 35	ns
47	Output enable (referenced from $\overline{TR}/\overline{OE}$)		^tOE	$^ta(OE)$		-12 -15 -20	9, 10, 11		25 30 45	ns
48	Output disable (referenced from $\overline{TR}/\overline{OE}$)		^tOD	$^tdis(OE)$		-12 -15 -20	9, 10, 11		25 30 35	ns

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 10, 11, 17) (V_{CC} = 5.0V ± 10%)

ITEM	TEST	NOTES	SYMBOL	ALT. SYMBOL	CONDITIONS -55°C ≤ T_C ≤ +110°C	DEVICE TYPE	GROUP A SUBGROUPS	LIMITS MIN	LIMITS MAX	UNIT
1	TRANSFER command to $\overline{RAS}$ set-up time	23	^tTS	$^tsu(DT)$	All cycle times assume ^tT = 5ns.	-12 -15 -20	9, 10, 11	0 0 0		ns
2	TRANSFER command to $\overline{RAS}$ hold time	23	^tRTH	$^th(DT)$		-12 -15 -20	9, 10, 11	90 100 140		ns
3	TRANSFER command to $\overline{CAS}$ hold time	23	^tCTH	$^th(CLDT)$		-12 -15 -20	9, 10, 11	30 35 50		ns
4	TRANSFER command to to SC lead time	23, 26	^tTSL	^tSHDH		-12 -15 -20	9, 10, 11	5 10 20		ns
5	TRANSFER command to $\overline{RAS}$ lead time	23, 26	^tTRL	$^tsu(DTRH)$		-12 -15 -20	9, 10, 11	10 10 20		ns
6	TRANSFER command to $\overline{RAS}$ delay time	23, 26	^tTRD	$^th(DTRH)$		-12 -15 -20	9, 10, 11	15 20 40		ns
7	TRANSFER command to $\overline{CAS}$ lead time	23, 26	^tTCL	$^tsu(DTCH)$		-12 -15 -20	9, 10, 11	10 10 20		ns
8	TRANSFER command to $\overline{CAS}$ delay time	23, 26	^tTCD	$^th(DTCH)$		-12 -15 -20	9, 10, 11	15 20 40		ns
9	First SC edge to TRANSFER command delay time	26	^tTSD	$^th(SCDT)$		-12 -15 -20	9, 10, 11	10 20 40		ns
10	SAM-to-DRAM (Write) TRANSFER command to $\overline{RAS}$ hold time		^tRTHW	$^th(TR)$		-12 -15 -20	9, 10, 11	15 15 30		ns
11	Serial output buffer turn off delay from $\overline{RAS}$	26	^tSDZ			-12 -15 -20	9, 10, 11	10 10 10	50 60 80	ns
12	SC to $\overline{RAS}$ set-up time	26	^tSRS	$^tsu(SCRL)$		-12 -15 -20	9, 10, 11	40 45 60		ns
13	$\overline{RAS}$ to SC delay time	26	^tSRD	^tRHSC		-12 -15 -20	9, 10, 11	30 35 50		ns
14	Serial data input to SE delay time	26	^tSZE			-12 -15 -20	9, 10, 11	0 0 0		ns
15	$\overline{RAS}$ to SD buffer turn on time	26	^tSRO			-12 -15 -20	9, 10, 11	0 0 0		ns
16	Serial data input delay from $\overline{RAS}$	26	^tSDD			-12 -15 -20	9, 10, 11	55 60 80		ns

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 10, 11, 17) (V_{CC} = 5.0V ± 10%)

ITEM	TEST	NOTES	SYMBOL	ALT. SYMBOL	CONDITIONS -55°C ≤ Tc ≤ +110°C	DEVICE TYPE	GROUP A SUBGROUPS	LIMITS MIN	LIMITS MAX	UNIT
17	Serial data input to $\overline{RAS}$ delay time	26	^tSZS		All cycle times assume ^tT = 5ns.	-12 -15 -20	9, 10, 11	0 0 0		ns
18	Serial input mode Enable (SE) to $\overline{RAS}$ set-up time	26	^tESR	$^tsu(SE)$		-12 -15 -20	9, 10, 11	0 0 0		ns
19	Serial input mode Enable (SE) to $\overline{RAS}$ hold time	26	^tREH	$^th(SE)$		-12 -15 -20	9, 10, 11	10 15 30		ns
20	NON-TRANSFER command to $\overline{RAS}$ set-up time	24, 26	^tYS	$^tsu(DTH)$		-12 -15 -20	9, 10, 11	0 0 0		ns
21	NON-TRANSFER command to $\overline{RAS}$ hold time	24, 26	^tYS	$^th(DTH)$		-12 -15 -20	9, 10, 11	10 10 20		ns

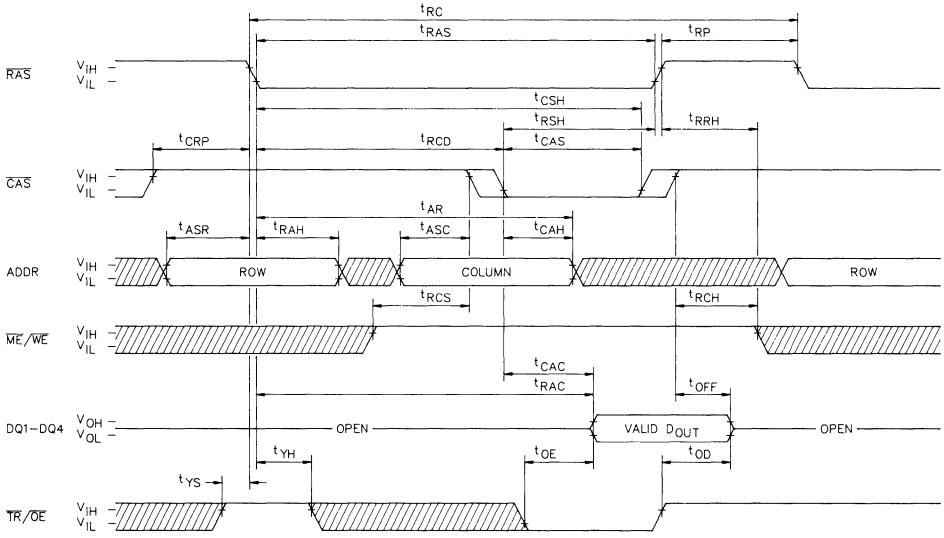
TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

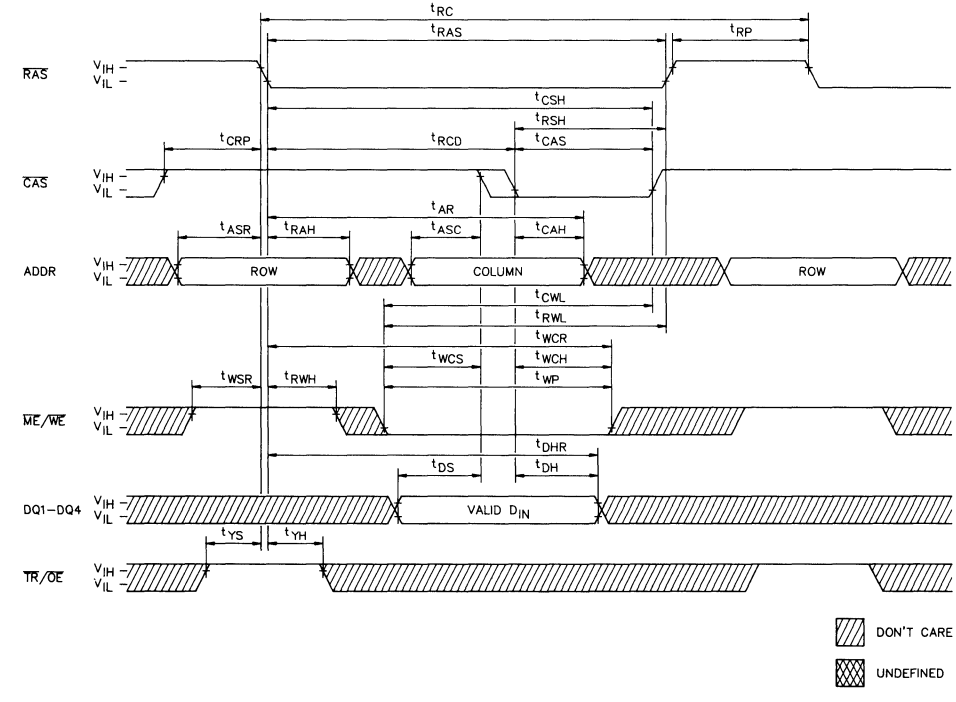
(Notes 3, 4, 5, 10, 11, 17) (V_{CC} = 5.0V ± 10%)

ITEM	TEST	NOTES	SYMBOL	ALT. SYMBOL	CONDITIONS -55°C ≤ T_C ≤ +110°C	DEVICE TYPE	GROUP A SUBGROUPS	LIMITS MIN	LIMITS MAX	UNIT
1	Serial clock cycle time	26	^tSC	$^tc(SC)$	All cycle times assume ^tT = 5ns.	12 -15 -20	9, 10, 11	40 60 80		
2	Access time from SC		^tSAC	$^ta(SC)$		-12 -15 -20	9, 10, 11	40 60 80		
3	SC precharge time	26	^tSP	$^tw(SCH)$		-12 -15 -20	9, 10, 11	10 20 30		
4	SC pulse width	26	^tSAS	$^tw(SCL)$		-12 -15 -20	9, 10, 11	10 20 30		
5	Access time from SE	26	^tSEA	$^ta(SE)$		-12 -15 -20	9, 10, 11	30 40 60		
6	SE precharge time	26	^tSEP	$^tw(SEH)$		-12 -15 -20	9, 10, 11	15 20 30		
7	SE pulse width	26	^tSE	$^tw(SEL)$		-12 -15 -20	9, 10, 11	15 20 30		
8	Serial data out hold time after SC high	26	^tSOH	$^th(SCHD)$		-12 -15 -20	9, 10, 11	10 10 10		
9	Serial output buffer turn off delay from SE	26	^tSEZ	$^tdis(SE)$		-12 -15 -20	9, 10, 11	0 0 0	25 30 50	
10	Serial data in set-up time		^tSDS	$^tsu(SD)$		-12 -15 -20	9, 10, 11	0 0 0		
11	Serial data in hold time		^tSDH	$^th(SD)$		-12 -15 -20	9, 10, 11	20 25 40		
12	Serial input (Write) enable set-up time	26	^tSWS	$^tsu(SEL)$		-12 -15 -20	9, 10, 11	0 0 0		
13	Serial input (Write) enable hold time	26	^tSWH	$^th(SEL)$		-12 -15 -20	9, 10, 11	35 45 60		
14	Serial input (Write) disable set-up time	26	^tSWIS	$^tsu(SEH)$		-12 -15 -20	9, 10, 11	0 0 0		ns
15	Serial input (Write) disable hold time	26	^tSWIH	$^th(SEH)$		-12 -15 -20	9, 10, 11	35 45 60		ns

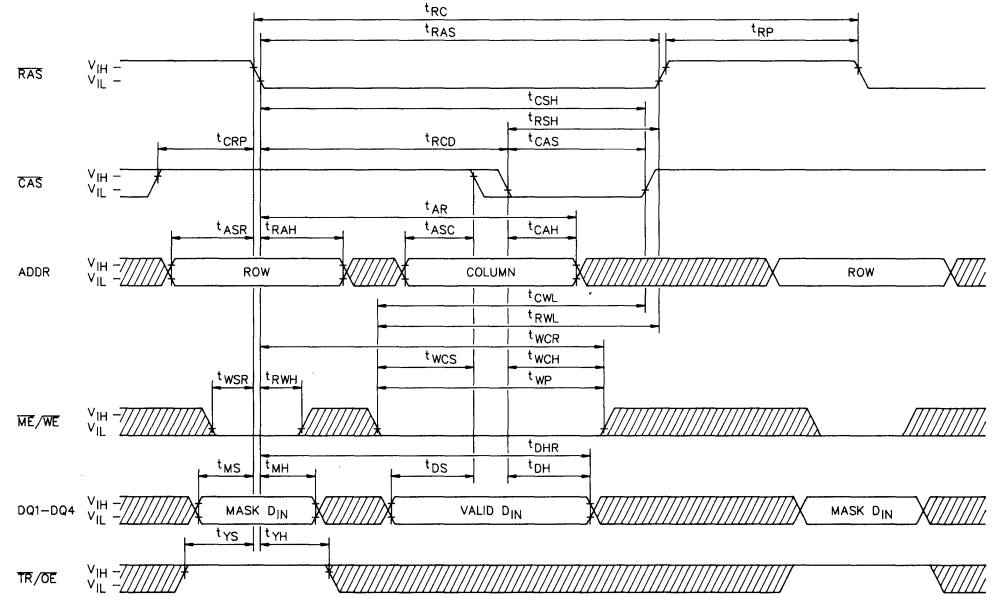
DRAM READ CYCLE



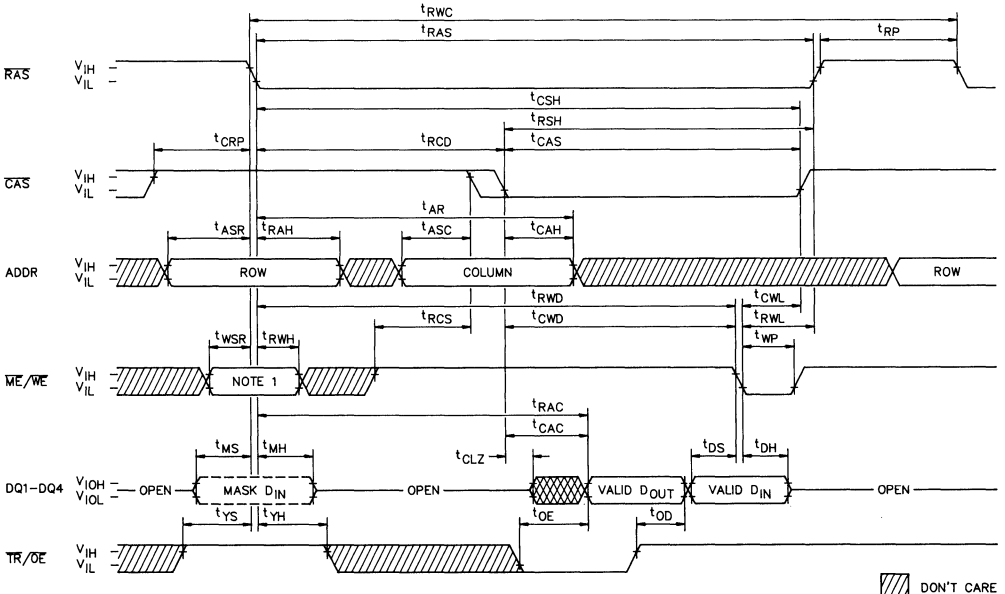
DRAM EARLY-WRITE CYCLE



DRAM MASK-WRITE CYCLE

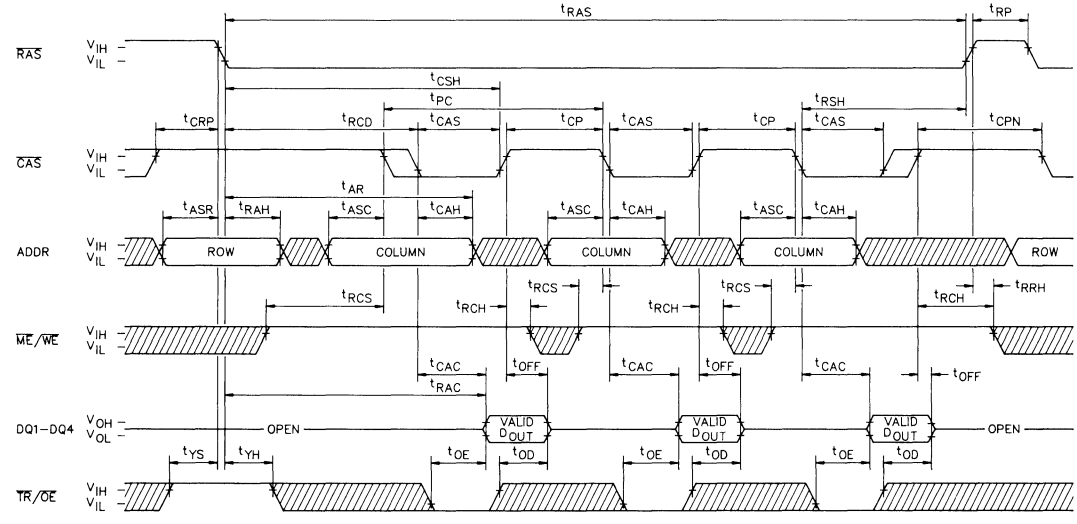


DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)

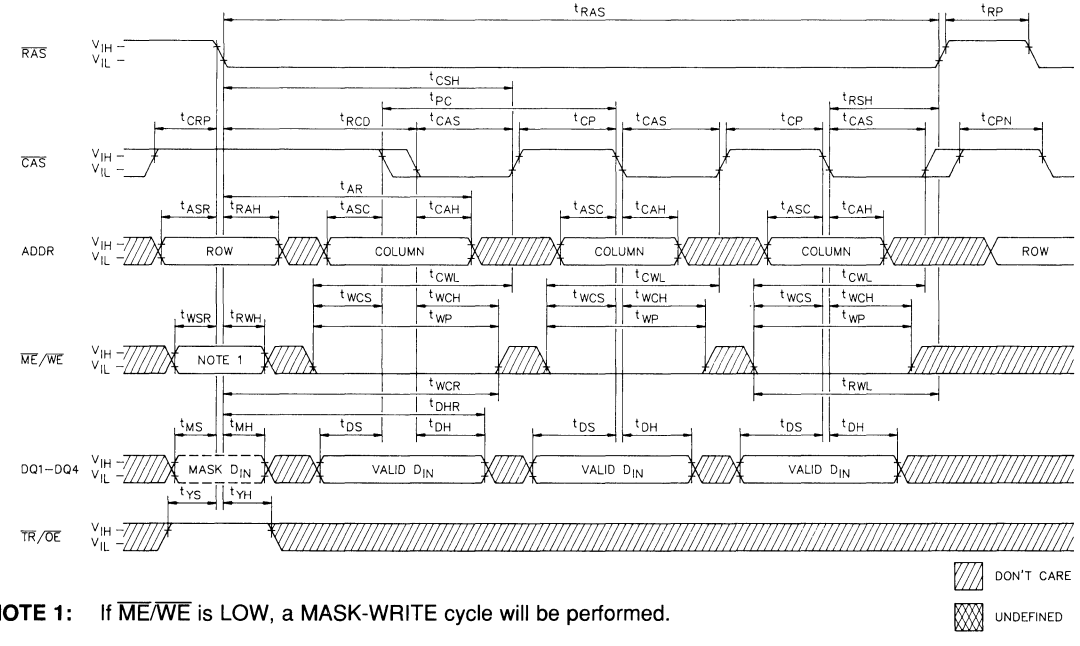


NOTE 1: If $\overline{ME}/\overline{WE}$ is LOW, a MASK-WRITE cycle will be performed.

DRAM PAGE-MODE READ CYCLE

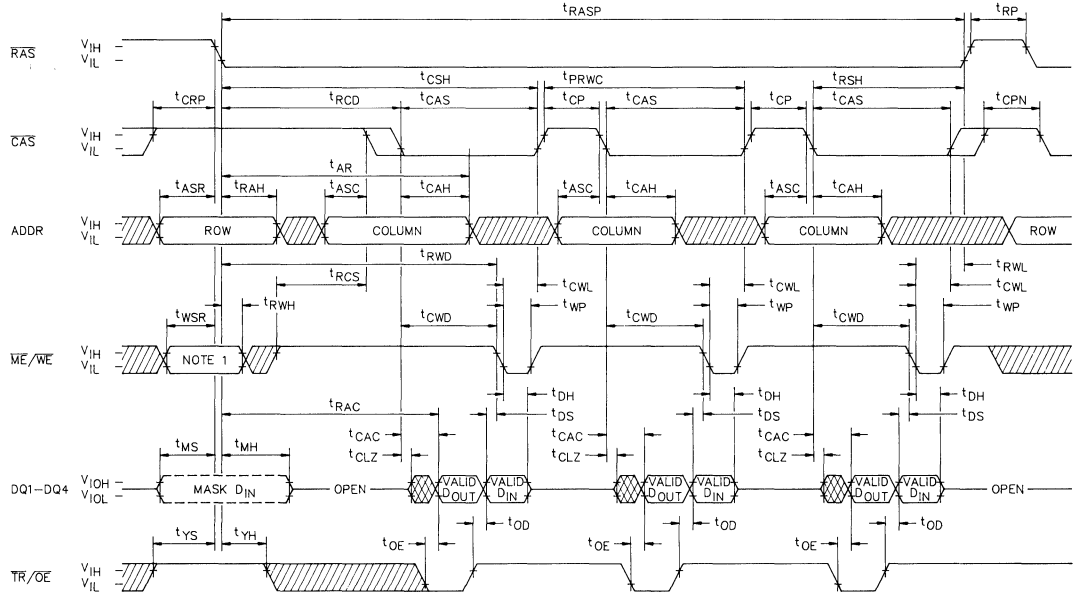


DRAM PAGE-MODE EARLY-WRITE CYCLE



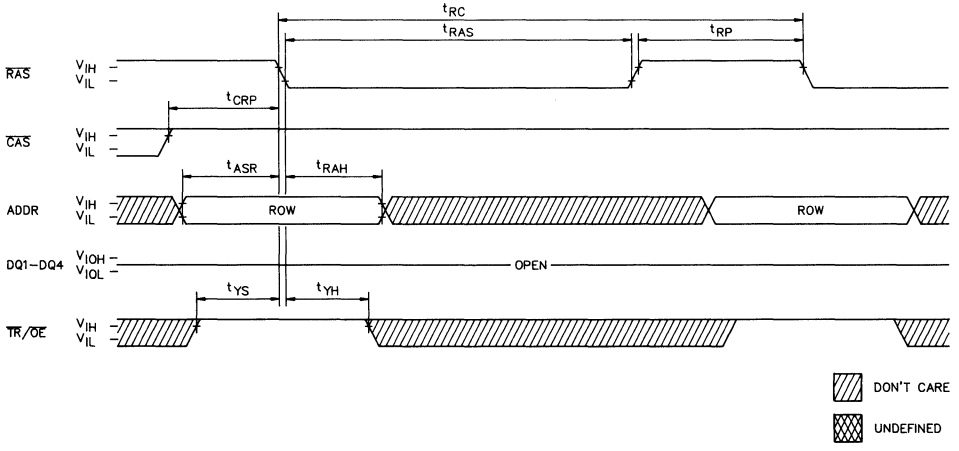
NOTE 1: If $\overline{ME}/\overline{WE}$ is LOW, a MASK-WRITE cycle will be performed.

DRAM PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



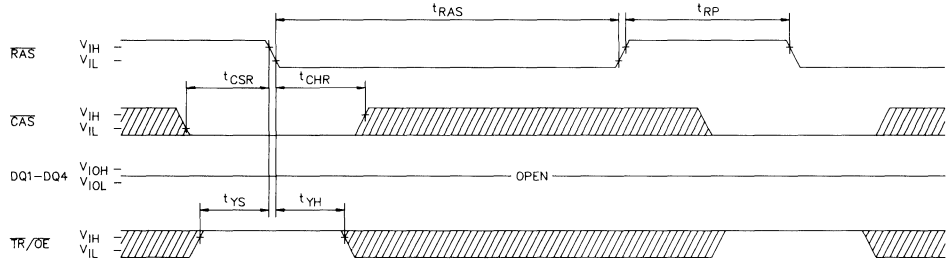
NOTE: 1: If $\overline{ME}/\overline{WE}$ is LOW, a MASK-WRITE cycle will be performed

$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{ME}/\overline{WE}$ = Don't Care)

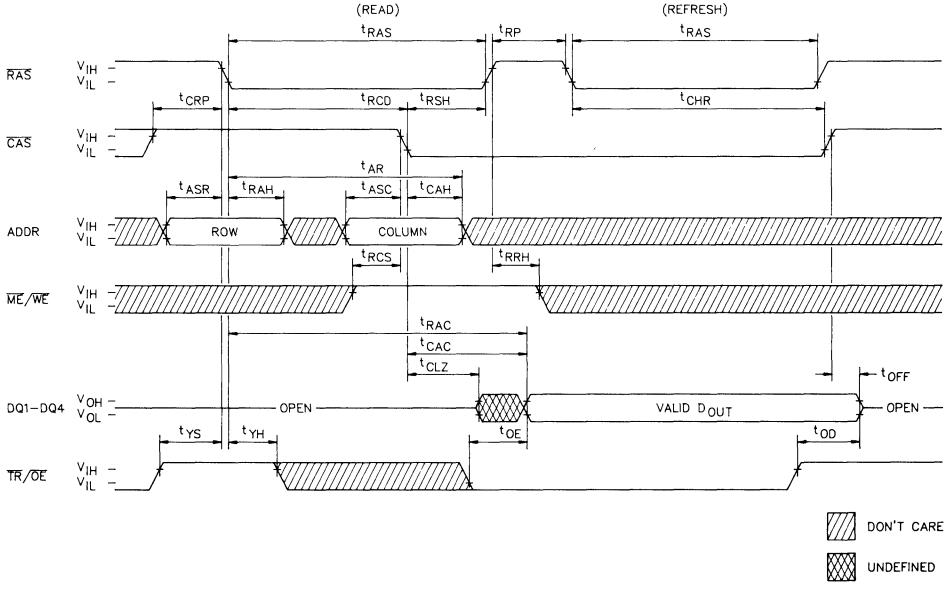


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_7 and $\overline{ME}/\overline{WE}$ are Don't Care.)



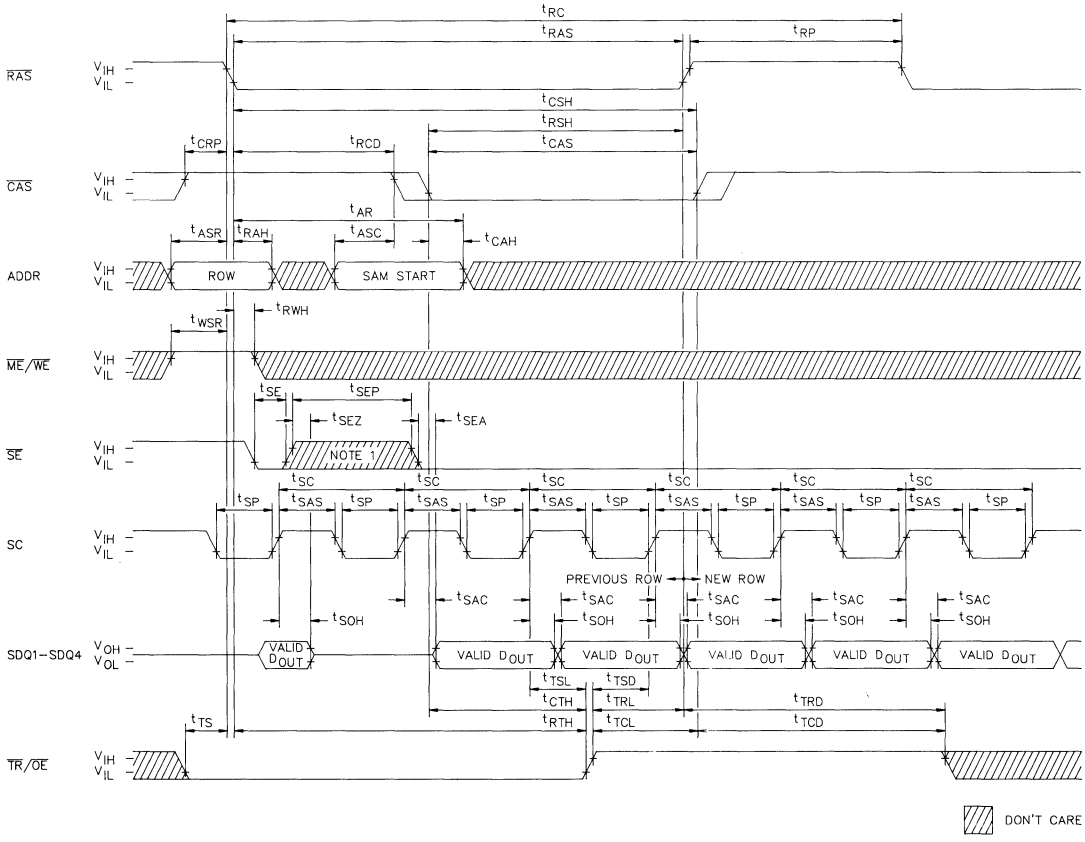
HIDDEN REFRESH CYCLE



NOTE: A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH.

DRAM-TO-SAM TRANSFER
(READ TRANSFER)

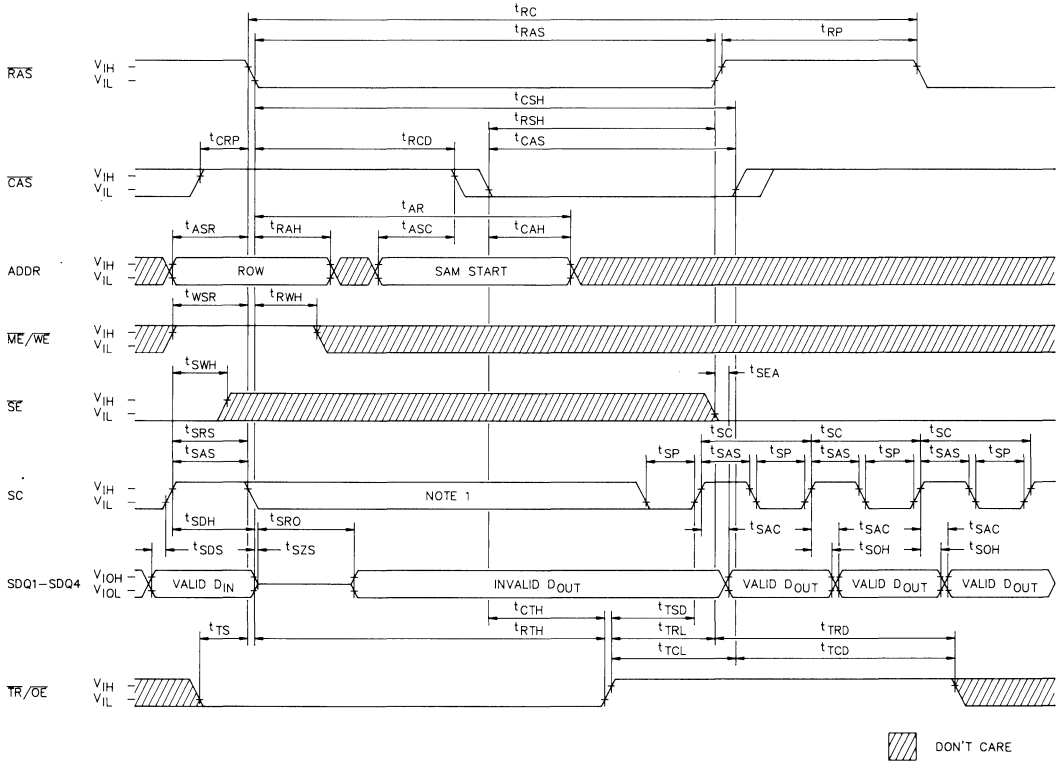
(When part was previously in the SERIAL OUTPUT mode.)



NOTE 1: This $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

DRAM-TO-SAM TRANSFER
(READ TRANSFER)

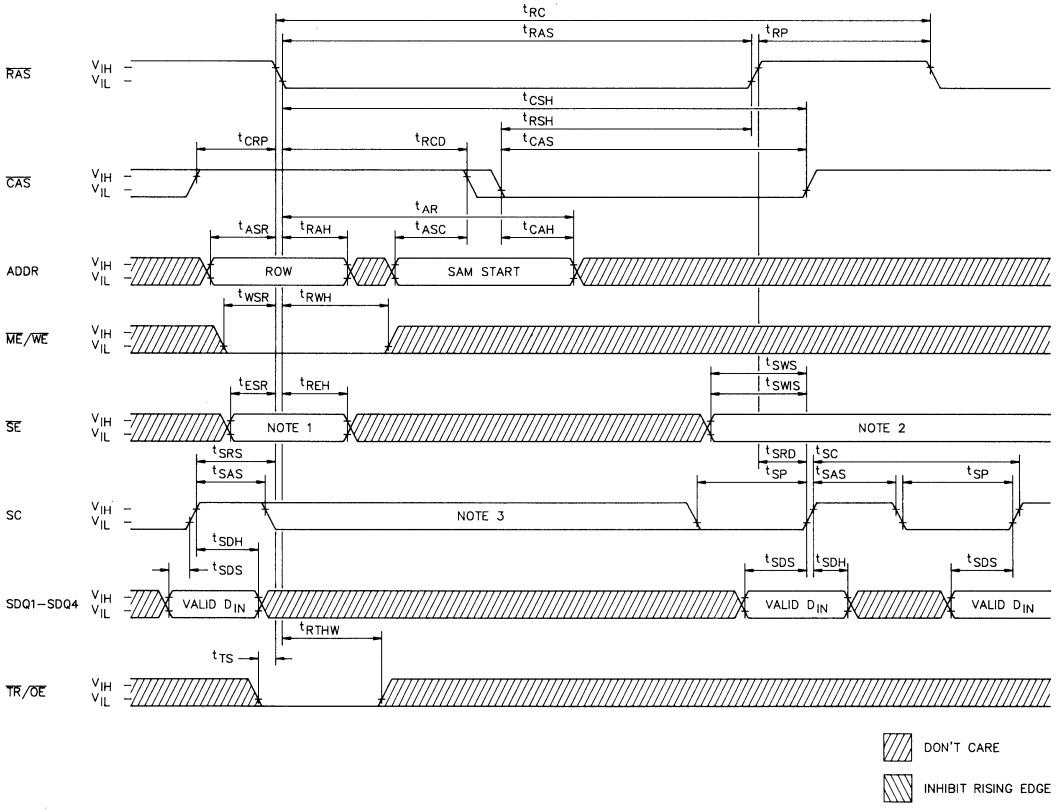
(When part was previously in the SERIAL INPUT mode.)



NOTE 1: There must be no rising edges on the SC input during this time period.

SAM-TO-DRAM TRANSFER
(WRITE TRANSFER)

(When part was previously in the SERIAL INPUT mode.)



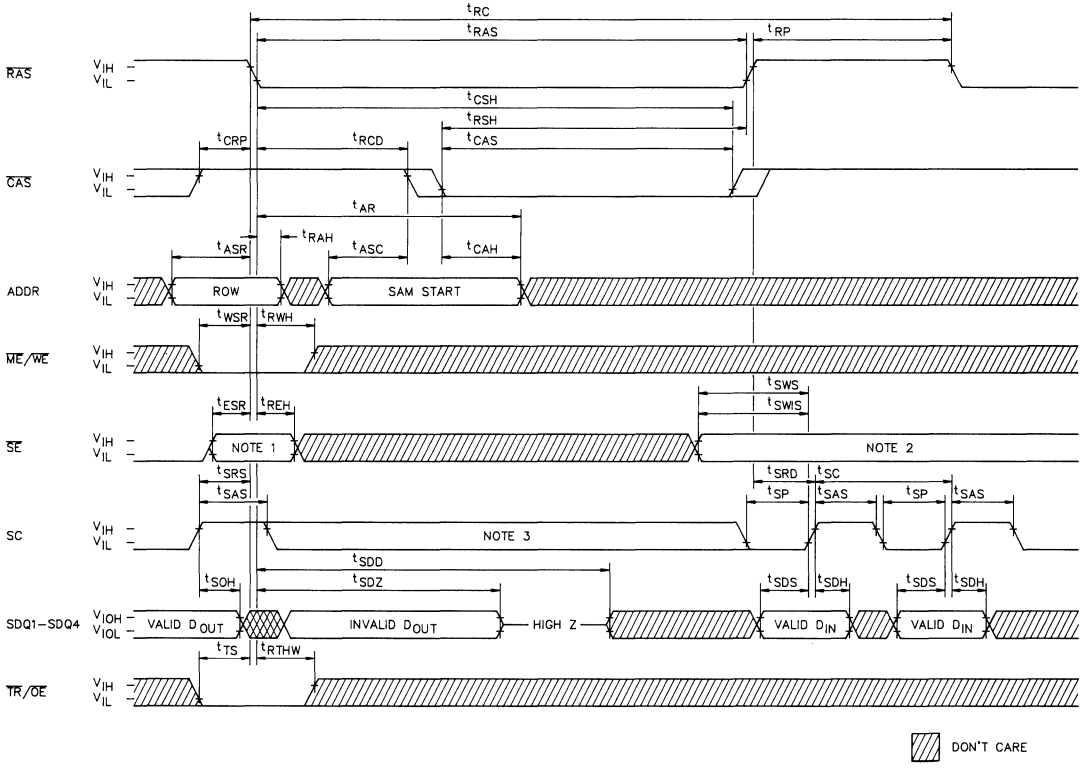
NOTE 1: If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

NOTE 3: There must be no rising edges on the SC input during this time period.

SAM-TO-DRAM TRANSFER
(WRITE TRANSFER/PSEUDO WRITE TRANSFER)

(When part was perviously in the SERIAL OUTPUT mode.)

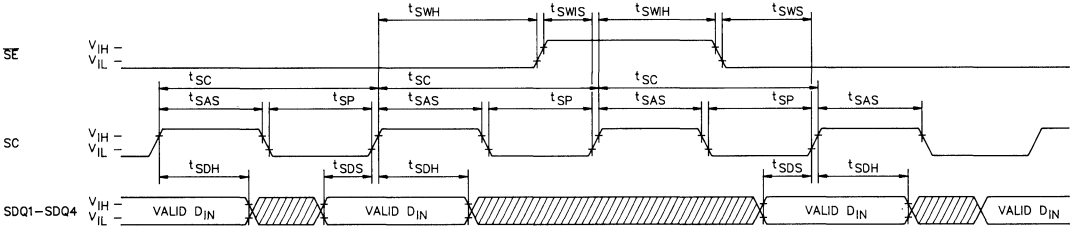


NOTE 1: If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

NOTE 3: There must be no rising edges on the SC input during this time period.

SAM SERIAL INPUT

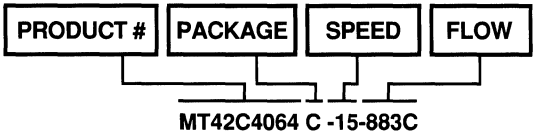


SAM SERIAL OUTPUT

MICRON MIL-STD-883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD-883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan and submit to qualifying activity.	Approved by DESC
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot.	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD-883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018 SEM Monitors	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD-883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented data sheet @ +118°C	100%
13. Burn-in	Method 1015, 162 hours @ 125°C	100%
14. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +113°C 5% PDA and in-line Group A per method 5005	100%
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection per Method 5005 (attributes data only)		
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and construction tests	Each package type on each lot
21. Group C	Die related (1000 hr. operating life)	Micro circuit group/every quarter
22. Group D	Package related test	Each package type Generic every 26 weeks

ORDER INFORMATION



The Micron MT42C4064 is functionally equivalent to other manufacturer's products meeting JEDEC standards. It is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using the high speed, low power CMOS double poly, single metal process. Micron's QUALITY ASSURED policy is to offer prompt, accurate, and courteous service while assuring reliability and quality. Functionality is consistently assured over a wider power supply, temperature, and refresh range than specified. Each unit receives accelerated burn-in and and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

MILITARY SRAM

2K x 8 SRAM

ADDITIONAL MILITARY SPECIFICATIONS

- SMD 84036
- JAN (consult factory for reference number)
- RAD-tolerant (consult factory)

FEATURES

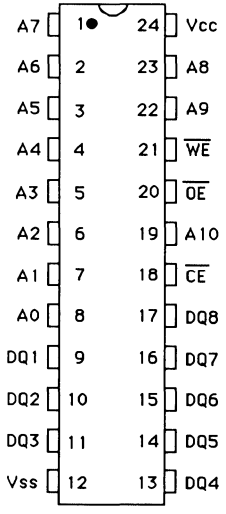
- Battery Backup – 2 volt data retention
- High speed: 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS / MARKING

• Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Ceramic DIP (300 mil)	C
Ceramic LCC	EC
• Two Volt Data Retention	L

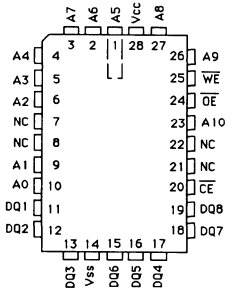
PIN ASSIGNMENT (Top View)

24L/300 DIP



CF

28L/LCC



ECE

GENERAL DESCRIPTION

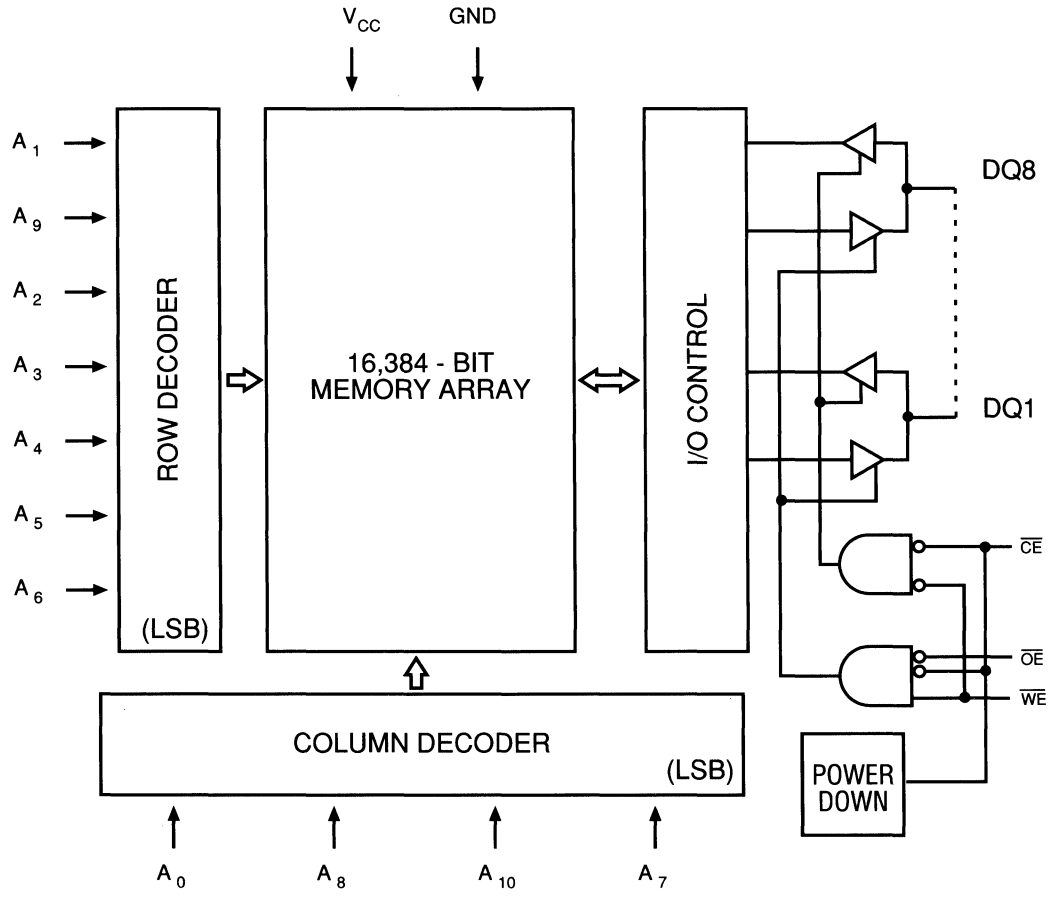
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology. All fabrication is 100% domestic.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	DOUT	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on any input relative to Vss ..... -2.0 to +7.0V
Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA
Lead Temperature (soldering, 10 seconds) ..... +260°C
Junction Temperature ..... +175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55°C \le T_C \le 125°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	6.0	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Outputs Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	130	120	110	100	95	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max., $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ Hz	I_{SBT1}	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, V_{CC} = Max., f = 0Hz	I_{SBT2}	35	35	35	35	35	mA	
	$\overline{CE} \ge (V_{CC} - 0.2)$, V_{CC} = Max., all other inputs $\le 0.2V$ or $\ge (V_{CC} - 0.2V)$, f = 0Hz	I_{SBC2}	10	10	10	10	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz, V_{CC} = 5V	C_I		8	pF	4
Output Capacitance		C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-55°C ≤ T_C ≤ 125°C, Vcc = 5V ± 10%)

DESCRIPTION		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	15		20		25		30		35		ns	
Address access time	^tAA		15		20		25		30		35	ns	
Chip enable access time	^tACE		15		20		25		30		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		10		15		15		20		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		ns	
Chip disable to power down time	^tPD		15		20		25		30		35	ns	
Output enable access time	^tAOE		12		15		15		20		20	ns	
Output enable to output in low Z	^tLZOE	0		0		0		0		0		ns	
Output disable to output in high Z	^tHZOE		10		15		15		20		20	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	15		20		25		30		35		ns	
Chip enable to end of write	^tCW	13		15		20		25		30		ns	
Address valid to end of write	^tAW	15		15		20		25		30		ns	
Address set-up time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
Write pulse width	^tWP	13		15		20		25		25		ns	
Data set-up time	^tDS	10		12		15		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2

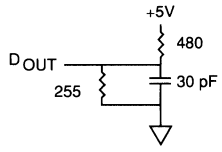


Fig. 1 OUTPUT LOAD EQUIVALENT

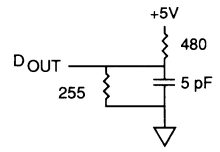


Fig. 2 OUTPUT LOAD EQUIVALENT

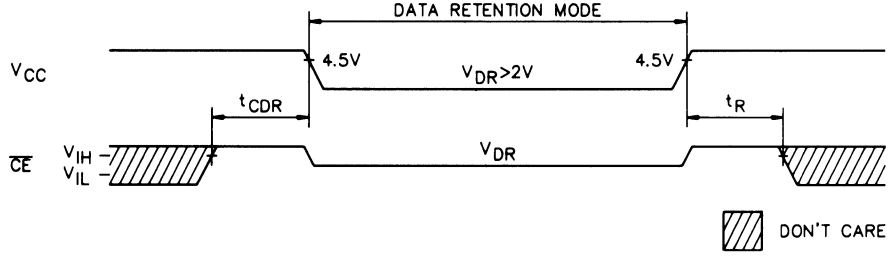
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ = Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are tested with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

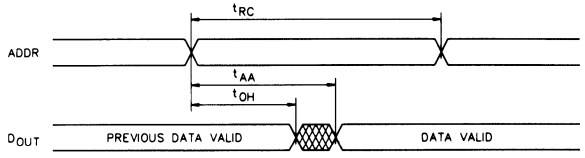
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	Vcc=2v	—	95	1000	µA
			Vcc=3v	—	350	1500	µA
$^{t}CDR^{(4)}$	Chip Deselect to Data Retention Time			0		—	ns
$^{t}R^{(4)}$	Operation Recovery Time			$^{t}RC^{(11)}$			ns

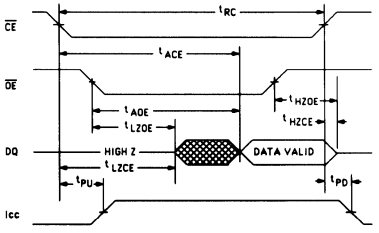
LOW Vcc DATA RETENTION WAVEFORM



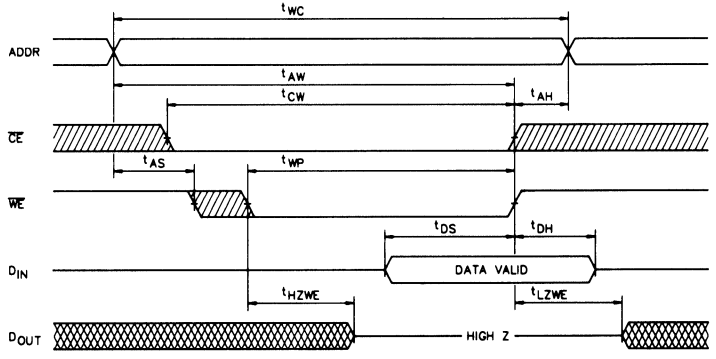
READ CYCLE NO. 1 (8, 9)



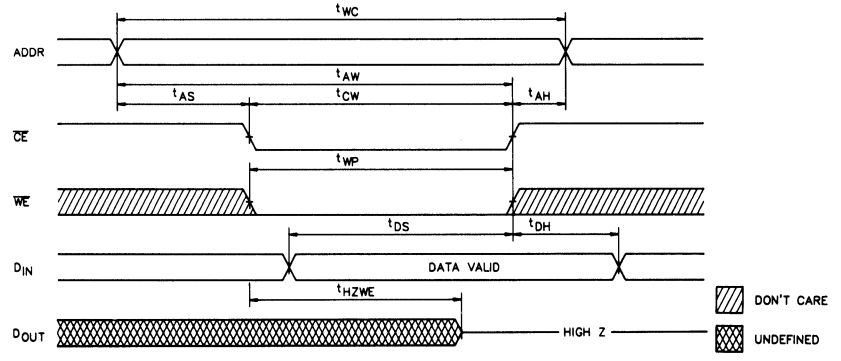
READ CYCLE NO. 2 (7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



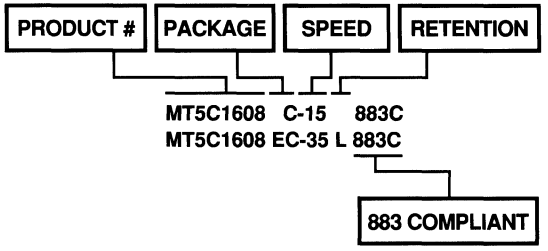
WRITE CYCLE NO. 2
(Chip Enable Controlled)



MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot.	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD-883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018 SEM Monitors	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD-883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented data sheet @ +125°C	100%
13. Burn-in	Method 1015	100%
14. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +125°C 5% PDA and in-line Group A per method 5005	100%
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection per Method 5005 (attributes data only)		
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and construction tests	Each package type on each lot
21. Group C	Die related	Micro circuit group/every quarter
22. Group D	Package related test	Each package type Generic every 26 weeks

ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's 883 compliant devices. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

MILITARY SRAM

8K x 8 SRAM

ADDITIONAL MILITARY SPECIFICATIONS

- SMD 85525
- JAN (consult factory for reference number)
- RAD-tolerant (consult factory)

FEATURES

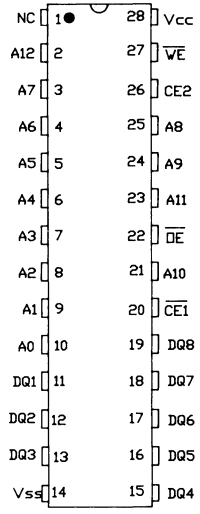
- Battery Backup – 2 volt data retention
- High speed: 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS

	MARKING
• Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Ceramic DIP (300 mil)	C
Ceramic DIP (600 mil)	CW
Ceramic LCC (28 leads)	EC
Ceramic LCC (32 leads)	ECW
• Two Volt Data Retention	L

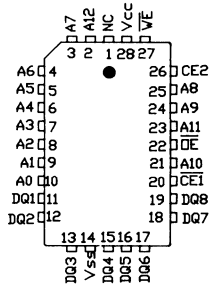
PIN ASSIGNMENT (Top View)

28L/300/600 DIP



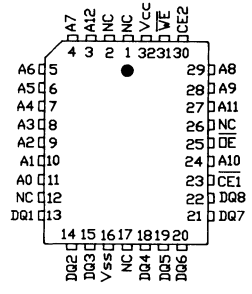
CH

28L/LCC



ECE

32L/LCC



ECF

GENERAL DESCRIPTION

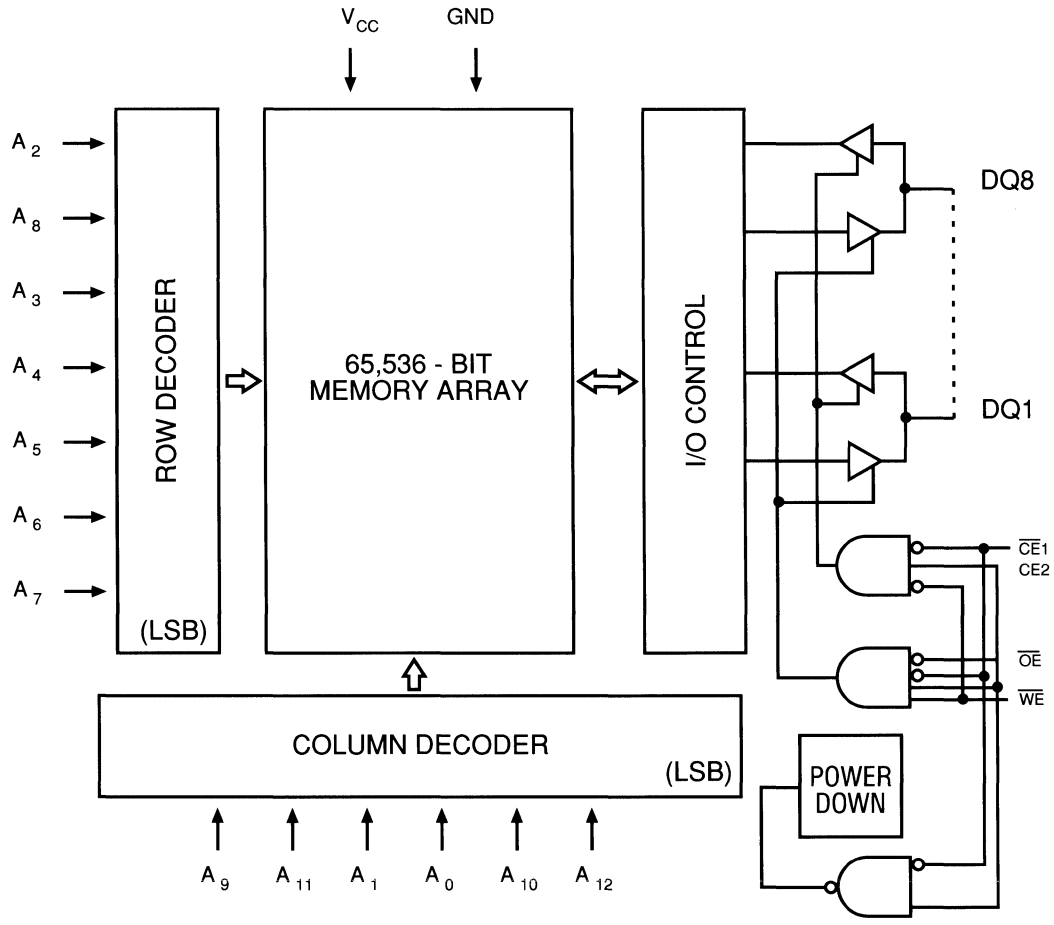
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology. All fabrication is 100% domestic.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	DQ	POWER
STANDBY	H	X	X	X	HIGH Z	STANDBY
STANDBY	X	L	X	X	HIGH Z	STANDBY
READ	L	H	H	L	DOUT	ACTIVE
READ	L	H	H	H	HIGH Z	ACTIVE
WRITE	L	H	L	X	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on any input or DQ relative to Vss ..-2.0 to +7.0V
Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Storage Temperature .....-65°C to +150°C
Power Dissipation .....1 Watt
Short Circuit Output Current 50mA
Lead Temperature (soldering, 10 seconds) .....+260°C
Junction Temperature .....+175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55°C \le T_C \le 125°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	6.0	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Outputs Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	130	120	110	100	95	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max., $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ Hz	I_{SBT1}	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, V_{CC} = Max., f = 0Hz	I_{SBT2}	35	35	35	35	35	mA	
	$\overline{CE} \ge (V_{CC} - 0.2)$, V_{CC} = Max., all other inputs $\le 0.2V$ or $\ge (V_{CC} - 0.2V)$, f = 0Hz	I_{SBC2}	10	10	10	10	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz, V_{CC} = 5V	C_I		8	pF	4
Output Capacitance		C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-55°C ≤ T_C ≤ 125°C, Vcc = 5V ± 10%)

DESCRIPTION		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	15		20		25		30		35		ns	
Address access time	^tAA		15		20		25		30		35	ns	
Chip enable access time	^tACE		15		20		25		30		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		10		15		15		20		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		ns	
Chip disable to power down time	^tPD		15		20		25		30		35	ns	
Output enable access time	^tAOE		12		15		15		20		20	ns	
Output enable to output in low Z	^tLZOE	0		0		0		0		0		ns	
Output disable to output in high Z	^tHZOE		10		15		15		20		20	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	15		20		25		30		35		ns	
Chip enable to end of write	^tCW	13		15		20		25		30		ns	
Address valid to end of write	^tAW	15		15		20		25		30		ns	
Address set-up time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
Write pulse width	^tWP	13		15		20		25		25		ns	
Data set-up time	^tDS	10		12		15		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2

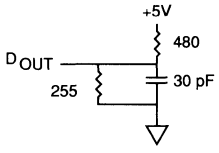


Fig. 1 OUTPUT LOAD EQUIVALENT

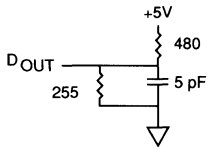


Fig. 2 OUTPUT LOAD EQUIVALENT

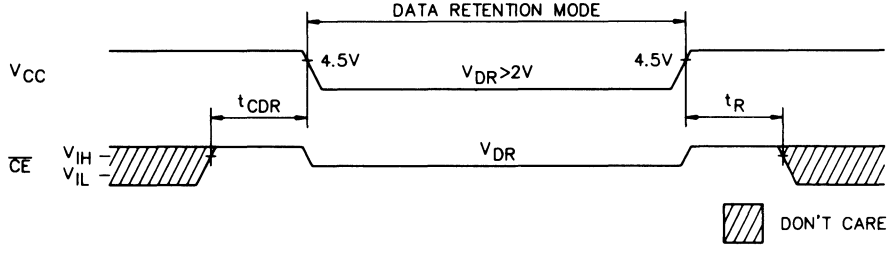
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{TRC(MIN)} = \frac{1}{TWC(MIN)}$ = Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are tested with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

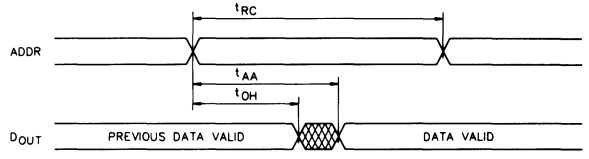
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
VDR	Vcc for Retention Data			2		—	V
ICCDR	Data Retention Current	$\overline{CE} \geq$ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	—	95	1000	µA
			Vcc=3v	—	350	1500	µA
^{t}CDR(4)	Chip Deselect to Data Retention Time			0		—	ns
^{t}R(4)	Operation Recovery Time			^{t}RC(11)			ns

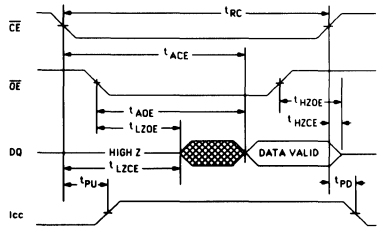
LOW Vcc DATA RETENTION WAVEFORM



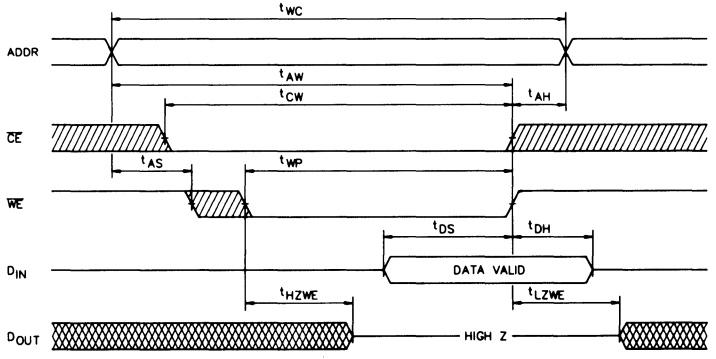
READ CYCLE NO. 1 (8, 9)



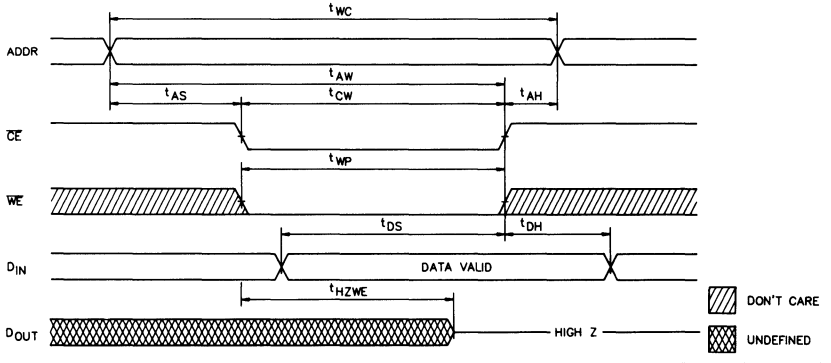
READ CYCLE NO. 2 (7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



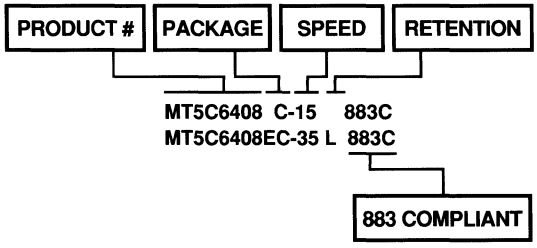
WRITE CYCLE NO. 2
(Chip Enable Controlled)



MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot.	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembled and tested in Boise, Idaho USA.
MIL-STD-883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018 SEM Monitors	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD-883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented data sheet @ +125°C	100%
13. Burn-in	Method 1015	100%
14. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +125°C 5% PDA and in-line Group A per method 5005	100%
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection per Method 5005 (attributes data only)		
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and construction tests	Each package type on each lot
21. Group C	Die related	Micro circuit group/every quarter
22. Group D	Package related test	Each package type Generic every 26 weeks

ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's 883 compliant devices. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

MILITARY SRAM

16K x 1 SRAM

ADDITIONAL MILITARY SPECIFICATIONS

- SMD 84132
- JAN M38510/291
- RAD-tolerant (consult factory)

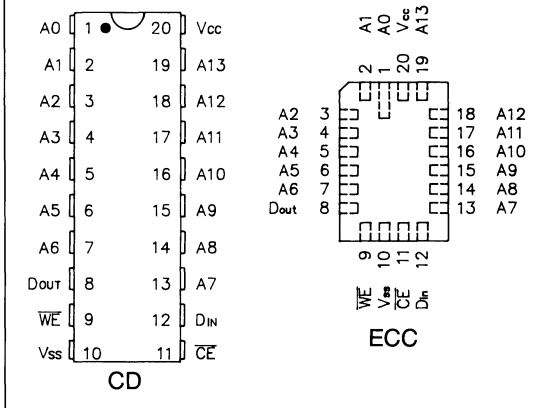
FEATURES

- Battery Backup – 2 volt data retention
- High speed: 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS

	MARKING
• Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Ceramic DIP (300 mil)	C
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)



GENERAL DESCRIPTION

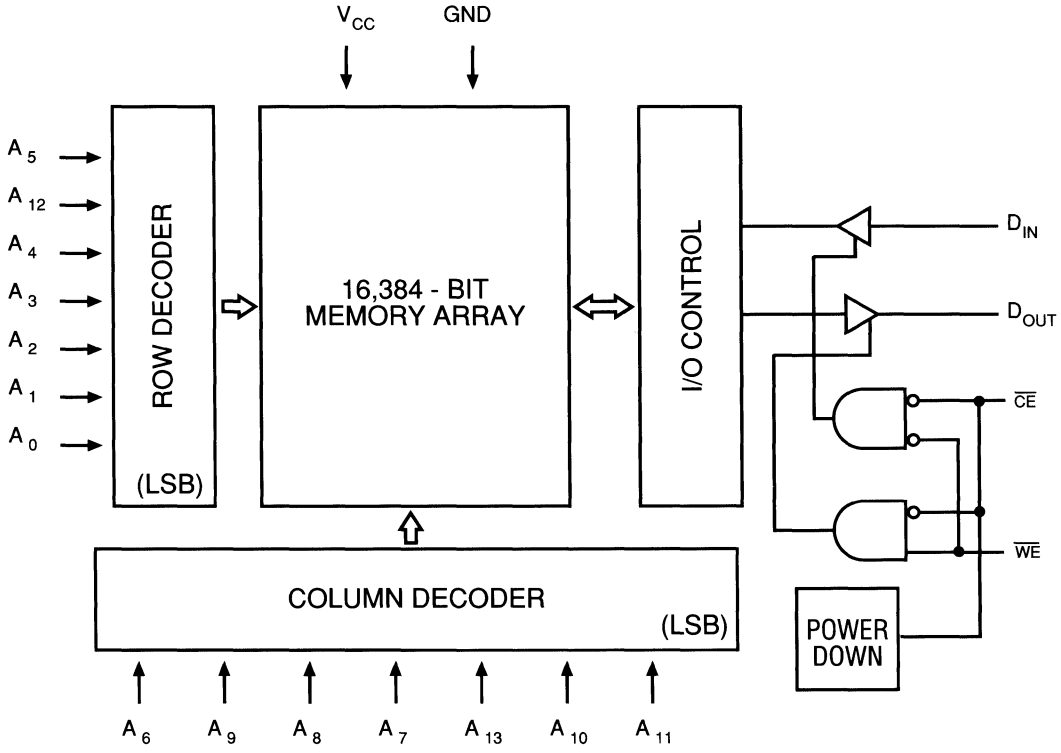
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology. All fabrication is 100% domestic.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	DOUT	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on any input relative to Vss ..... -2.0 to +7.0V
Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA
Lead Temperature (soldering, 10 seconds) ..... +260°C
Junction Temperature ..... +175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55°C \le T_C \le 125°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	6.0	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	$I_{OH} = -4.0mA$	V_{OH}	2.4		V	1
Output Low Voltage	$I_{OL} = 8.0mA$	V_{OL}		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Output Open	I_{CC}	130	120	110	100	95	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max., $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ Hz	I_{SBT1}	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, V_{CC} = Max., f = 0Hz	I_{SBT2}	35	35	35	35	35	mA	
	$\overline{CE} \ge (V_{CC} - 0.2)$, V_{CC} = Max., all other inputs $\le 0.2V$ or $\ge (V_{CC} - 0.2V)$, f = 0Hz	I_{SBC2}	10	10	10	10	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25°C$, f = 1MHz, $V_{CC} = 5V$	C_I		8	pF	4
Output Capacitance		C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-55°C ≤ T_C ≤ 125°C, Vcc = 5V ± 10%)

DESCRIPTION		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	15		20		25		30		35		ns	
Address access time	^tAA		15		20		25		30		35	ns	
Chip enable access time	^tACE		15		20		25		30		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		10		15		15		20		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		ns	
Chip disable to power down time	^tPD		15		20		25		30		35	ns	
WRITE Cycle													
WRITE cycle time	^tWC	15		20		25		30		35		ns	
Chip enable to end of write	^tCW	13		15		20		25		30		ns	
Address valid to end of write	^tAW	15		15		20		25		30		ns	
Address set-up time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
Write pulse width	^tWP	13		15		20		25		25		ns	
Data set-up time	^tDS	10		12		15		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2

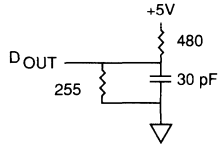


Fig. 1 OUTPUT LOAD EQUIVALENT

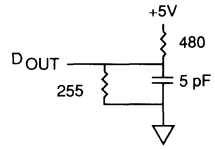


Fig. 2 OUTPUT LOAD EQUIVALENT

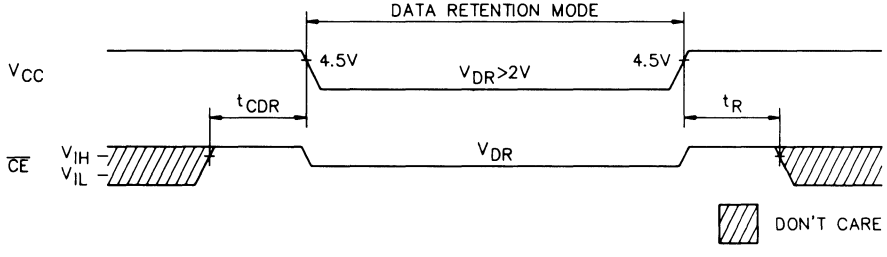
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the output unloaded, and $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ = Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are tested with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

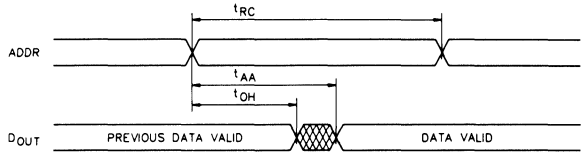
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	Vcc=2v	—	95	1000	µA
			Vcc=3v	—	350	1500	µA
$^{t}CDR^{(4)}$	Chip Deselect to Data Retention Time			0		—	ns
$^{t}R^{(4)}$	Operation Recovery Time			$^{t}RC^{(11)}$			ns

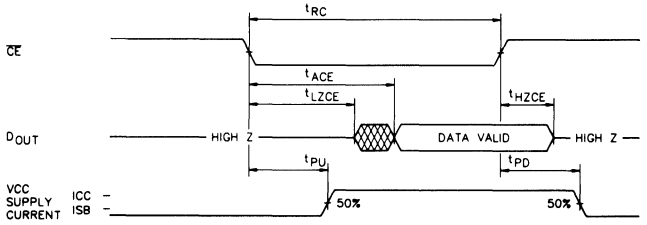
LOW Vcc DATA RETENTION WAVEFORM



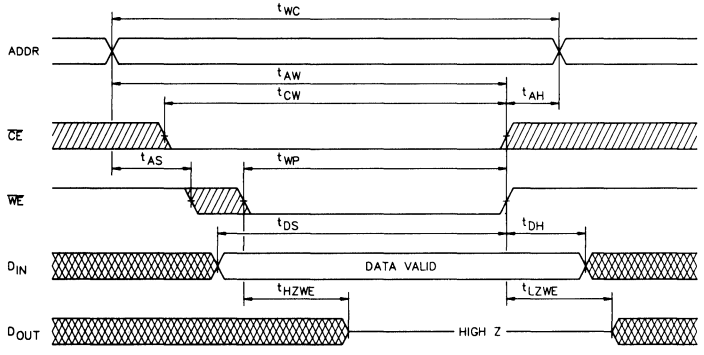
READ CYCLE NO. 1 (8, 9)



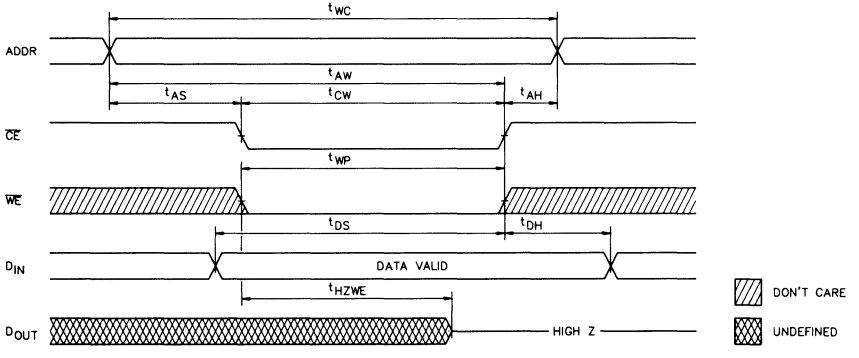
READ CYCLE NO. 2 (7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



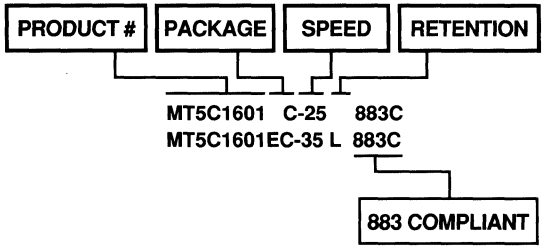
WRITE CYCLE NO. 2
(Chip Enable Controlled)



MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot.	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD-883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018 SEM Monitors	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD-883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented data sheet @ +125°C	100%
13. Burn-in	Method 1015	100%
14. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +125°C 5% PDA and in-line Group A per method 5005	100%
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection per Method 5005 (attributes data only)		
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and construction tests	Each package type on each lot
21. Group C	Die related	Micro circuit group/every quarter
22. Group D	Package related test	Each package type Generic every 26 weeks

ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's 883 compliant devices. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

MILITARY SRAM

16K x 4 SRAM

ADDITIONAL MILITARY SPECIFICATIONS

- SMD 86859
- JAN (consult factory for reference number)
- RAD-tolerant (consult factory)

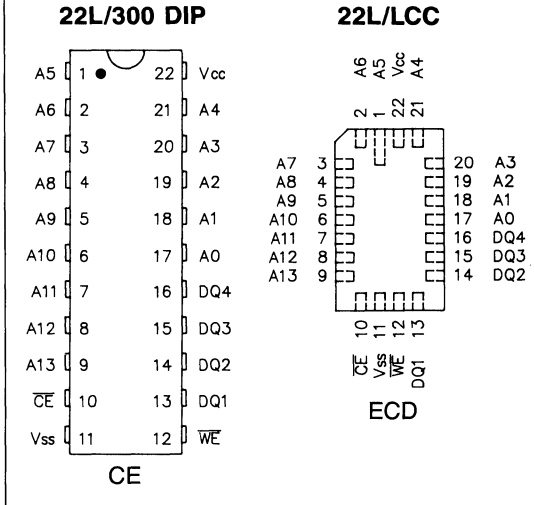
FEATURES

- Battery Backup – 2 volt data retention
- High speed: 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS

	MARKING
• Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Ceramic DIP (300 mil)	C
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)



GENERAL DESCRIPTION

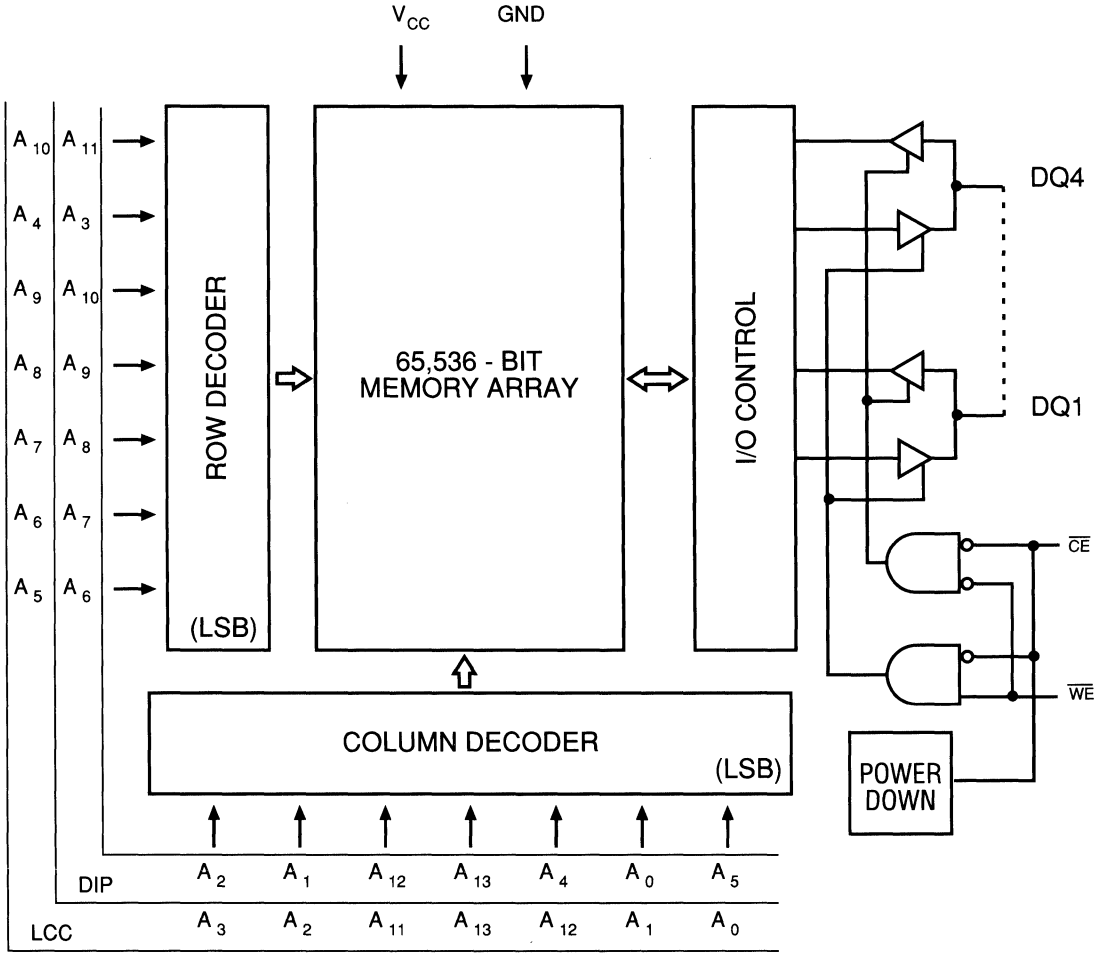
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology. All fabrication is 100% domestic.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	DOUT	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on any input or DQ relative to Vss .. -2.0 to +7.0V
Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA
Lead Temperature (soldering, 10 seconds) ..... +260°C
Junction Temperature ..... +175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55°C \le T_C \le 125°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	6.0	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Outputs Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	130	120	110	100	95	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max., $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ Hz	I_{SBT1}	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, V_{CC} = Max., f = 0Hz	I_{SBT2}	35	35	35	35	35	mA	
	$\overline{CE} \ge (V_{CC} - 0.2)$, V_{CC} = Max., all other inputs $\le 0.2V$ or $\ge (V_{CC} - 0.2V)$, f = 0Hz	I_{SBC2}	10	10	10	10	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz, V_{CC} = 5V	C_I		8	pF	4
Output Capacitance		C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-55°C ≤ T_C ≤ 125°C, Vcc = 5V ± 10%)

DESCRIPTION		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	t_{RC}	15		20		25		30		35		ns	
Address access time	t_{AA}		15		20		25		30		35	ns	
Chip enable access time	t_{ACE}		15		20		25		30		35	ns	
Output hold from address change	t_{OH}	3		3		3		3		3		ns	
Chip enable to output in low Z	t_{LZCE}	5		5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		10		15		15		20		20	ns	6,7
Chip enable to power up time	t_{PU}	0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		15		20		25		30		35	ns	
WRITE Cycle													
WRITE cycle time	t_{WC}	15		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	13		15		20		25		30		ns	
Address valid to end of write	t_{AW}	15		15		20		25		30		ns	
Address set-up time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		ns	
Write pulse width	t_{WP}	13		15		20		25		25		ns	
Data set-up time	t_{DS}	10		12		15		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	0		0		0		0		0		ns	
Write enable to output in high Z	t_{HZWE}	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2

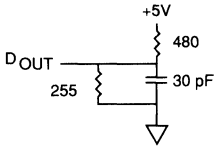


Fig. 1 OUTPUT LOAD EQUIVALENT

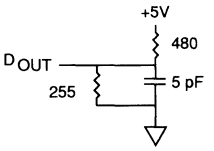


Fig. 2 OUTPUT LOAD EQUIVALENT

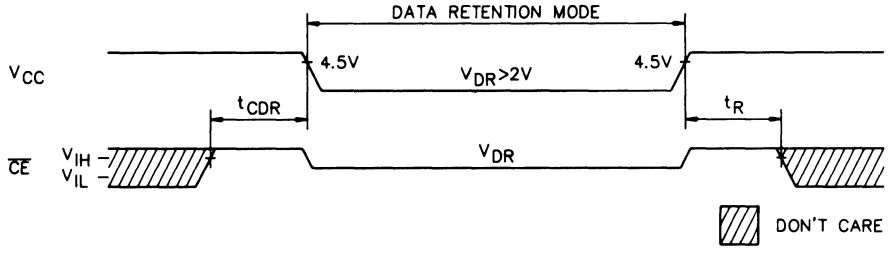
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. ICC is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{TRC(MIN)} = \frac{1}{TWC(MIN)}$ = Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^tHZCE and ^tHZWE are tested with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^tRC = Read Cycle Time. (Page 4)

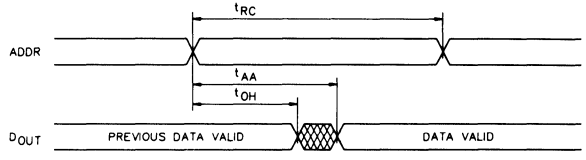
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
VDR	Vcc for Retention Data			2		—	V
ICCDR	Data Retention Current	$\overline{CE} \geq$ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	—	95	1000	µA
			Vcc=3v	—	350	1500	µA
^tCDR(4)	Chip Deselect to Data Retention Time			0		—	ns
^tR(4)	Operation Recovery Time			^tRC(11)			ns

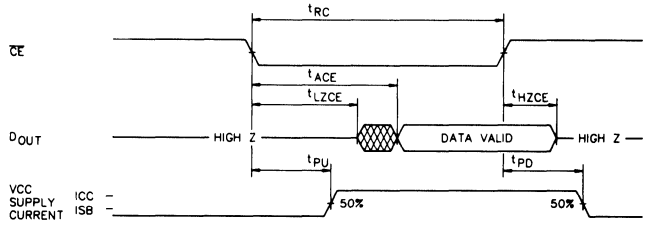
LOW Vcc DATA RETENTION WAVEFORM



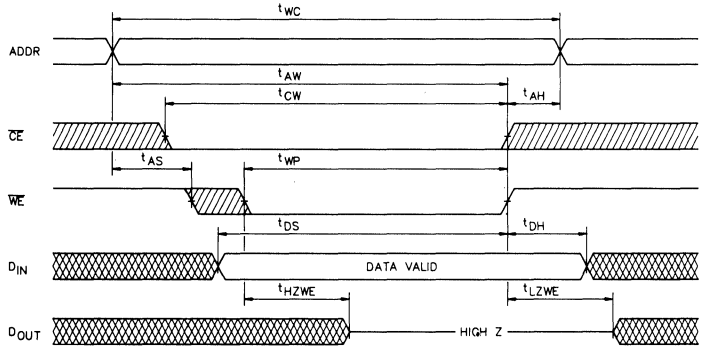
READ CYCLE NO. 1 (8, 9)



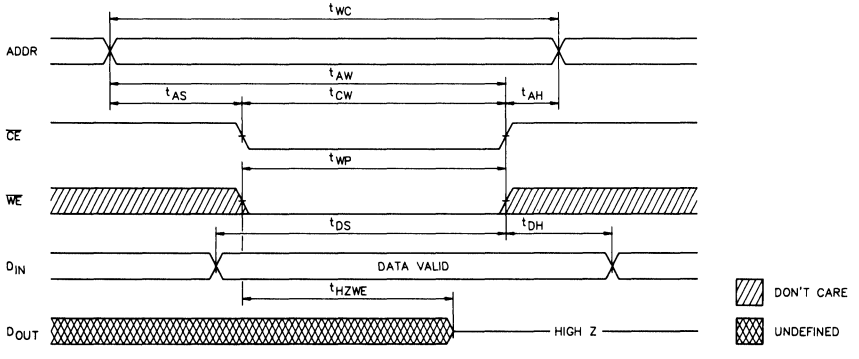
READ CYCLE NO. 2 (7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



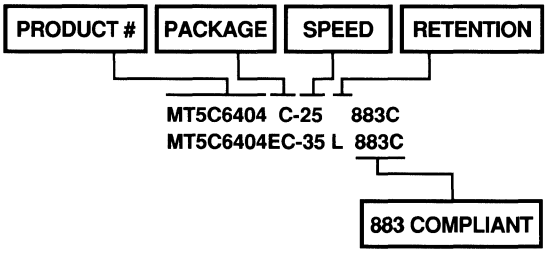
WRITE CYCLE NO. 2
(Chip Enable Controlled)



MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved.
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot.	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD-883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018 SEM Monitors	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD-883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented data sheet @ +125°C	100%
13. Burn-in	Method 1015	100%
14. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +125°C 5% PDA and in-line Group A per method 5005	100%
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection per Method 5005 (attributes data only)		
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and construction tests	Each package type on each lot
21. Group C	Die related	Micro circuit group/every quarter
22. Group D	Package related test	Each package type Generic every 26 weeks

ORDER INFORMATION



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Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

MILITARY SRAM

32K x 8 SRAM

ADDITIONAL MILITARY SPECIFICATIONS

- SMD 88662
- JAN (consult factory for reference number
- RAD-tolerant (consult factory)

FEATURES

- Battery Backup – 2 volt data retention
- High speed: 25, 30, 35 and 45ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS / MARKING

• Timing	
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Ceramic DIP (300 mil)	C
Ceramic DIP (600 mil)	CW
Ceramic LCC (28 pin)	EC
Ceramic LCC (32 pin)	ECW
• Two Volt Data Retention	L

GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

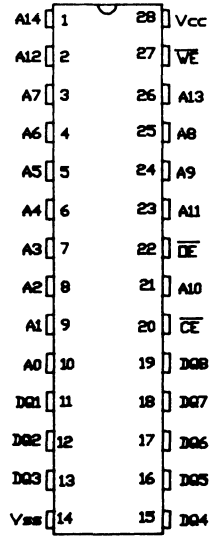
For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

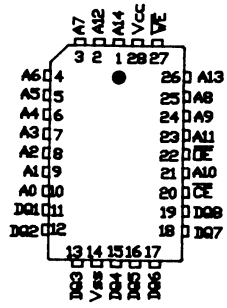
PIN ASSIGNMENT (Top View)

28L/300/600 DIP



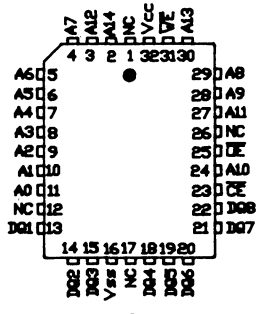
CH

28L/LCC



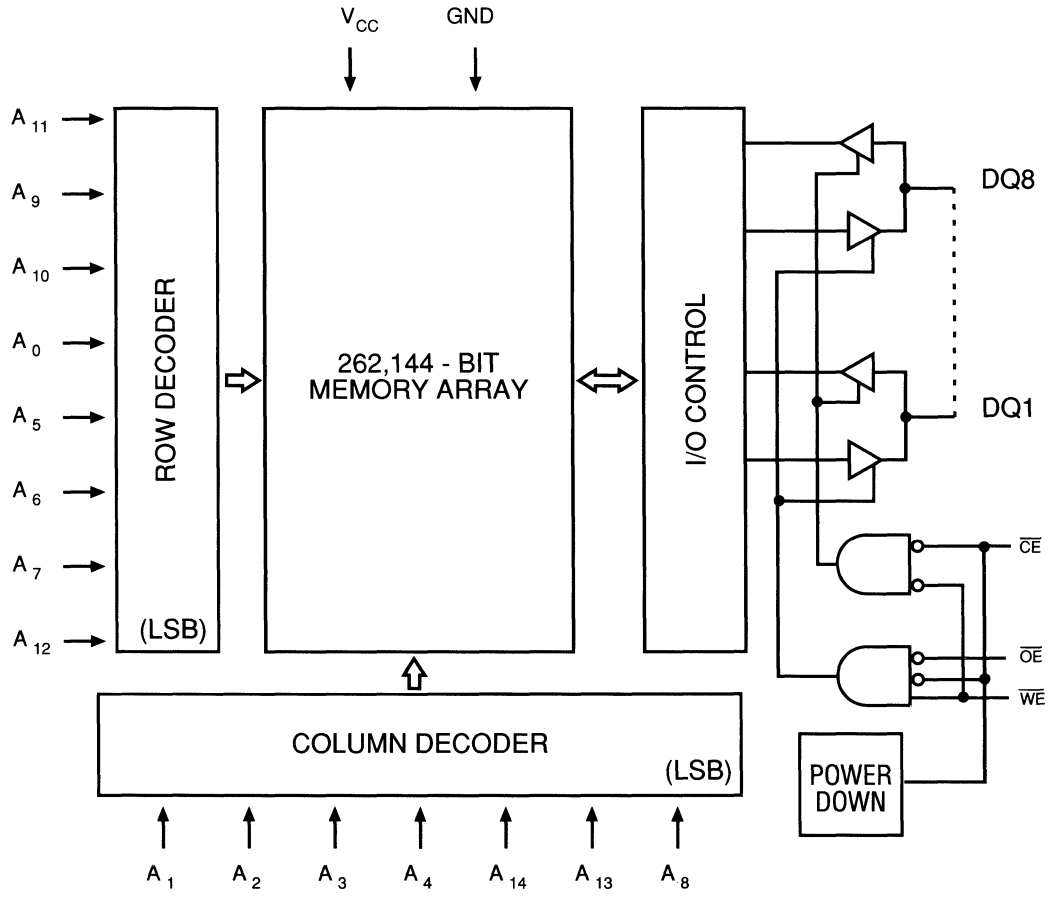
ECE

32L/LCC



ECF

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	DOUT	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on any input or DQ relative to V_{SS} -2.0V to +7.0V
Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA
Lead Temperature (soldering, 10 seconds) ..... +260°C
Juction Temperature ..... +175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55°C \le T_C \le 125°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	6.0	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}		100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max., $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ Hz	I_{SBT1}		40	mA	
	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, V_{CC} = Max., f = 0Hz	I_{SBT2}		20	mA	
	$\overline{CE} \ge (V_{CC} - 0.2V)$, V_{CC} = Max., all other inputs $\le 0.2V$ or $\ge (V_{CC} - 0.2V)$, f = 0Hz	I_{SBC2}		10	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Outputs Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz, V_{CC} = 5V	C_I		8	pF	4
Output Capacitance		C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-55°C ≤ T_C ≤ 125°C, Vcc = 5V ± 10%)

DESCRIPTION		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	25		30		35		45		ns	
Address access time	^tAA		25		30		35		45	ns	
Chip enable access time	^tACE		25		30		35		45	ns	
Output hold from address change	^tOH	5		5		5		5		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		15		20		20		20	ns	6, 7
Chip enable to power up time	^tPU	0		0		0		0		ns	
Chip disable to power down time	^tPD		25		30		35		45	ns	
Output Enable Access Time	^tAOE		15		20		20		20	ns	
Output Enable to output in low Z	^tLZOE	0		0		0		0		ns	
Output disable to out put in high Z	^tHZOE		15		20		20		20	ns	
WRITE Cycle											
WRITE cycle time	^tWC	25		30		35		45		ns	
Chip enable to end of write	^tCW	20		25		30		40		ns	
Address Valid to end of write	^tAW	20		25		30		40		ns	
Address set-up time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	2		2		2		2		ns	
Write pulse width	^tWP	20		25		25		30		ns	
Data set-up time	^tDS	16		18		20		20		ns	
Data hold time	^tDH	2		2		2		2		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	15	0	15	0	15	0	20	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2

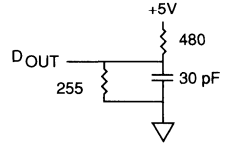


Fig. 1 OUTPUT LOAD EQUIVALENT

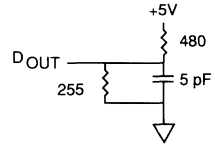


Fig. 2 OUTPUT LOAD EQUIVALENT

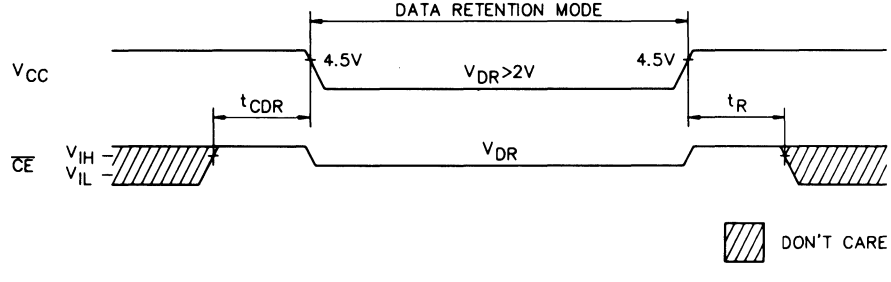
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{TRC(MIN)} = \frac{1}{TWC(MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

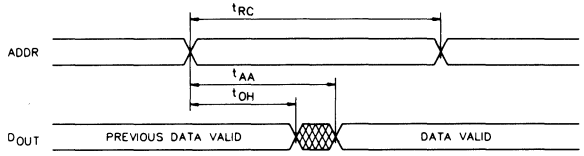
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
VDR	Vcc for Retention Data			2	—	V	
ICCDR	Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v		95	1000	µA
			Vcc=3v		350	1500	µA
^{t}CDR(4)	Chip Deselect to Data Retention Time			0		—	ns
^{t}R(4)	Operation Recovery Time			^{t}RC(11)			ns

LOW Vcc DATA RETENTION WAVEFORM

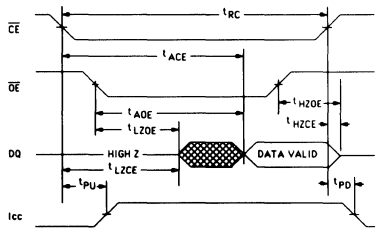


MILITARY FAST SRAM

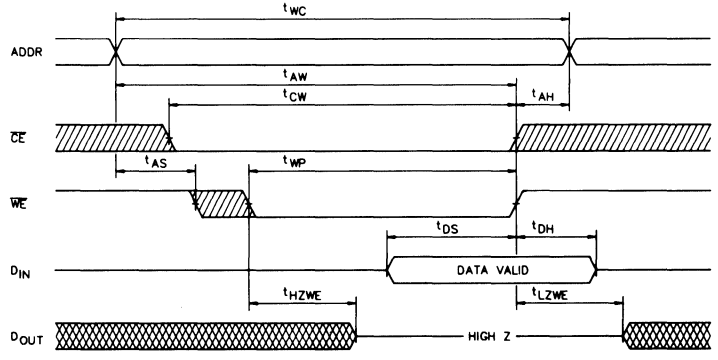
READ CYCLE NO. 1 (8, 9)



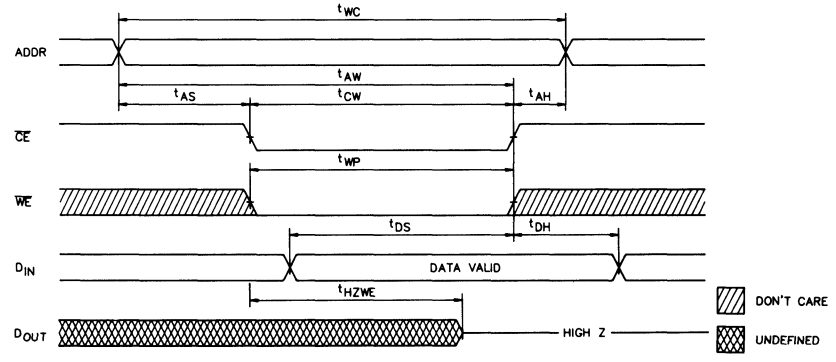
READ CYCLE NO. 2 (7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



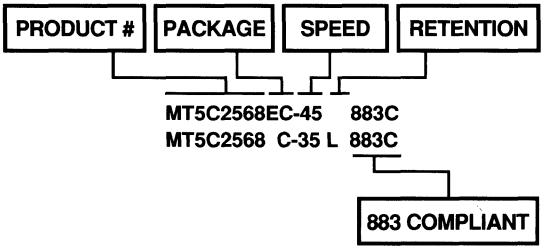
WRITE CYCLE NO. 2
(Chip Enable Controlled)



MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot.	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD 883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018 SEM Monitors	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD 883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented data sheet @ +125°C	100%
13. Burn-in	Method 1015	100%
14. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +125°C 5% PDA and in-line Group A per method 5005	100%
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection per Method 5005 (attributes data only)		
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and construction tests	Each package type on each lot
21. Group C	Die related	Micro circuit group/every quarter
22. Group D	Package related test	Each package type Generic every 26 weeks

ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's 883 compliant devices. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

MILITARY SRAM

64K x 1 SRAM

ADDITIONAL MILITARY SPECIFICATIONS

- SMD 86105
- JAN M38510/292
- RAD-tolerance (consult factory)

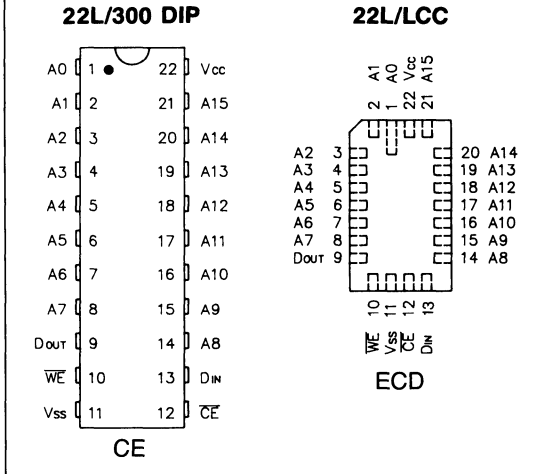
FEATURES

- Battery Backup – 2 volt data retention
- High speed: 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- All inputs and output are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS

	MARKING
• Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Ceramic DIP (300 mil)	C
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)



GENERAL DESCRIPTION

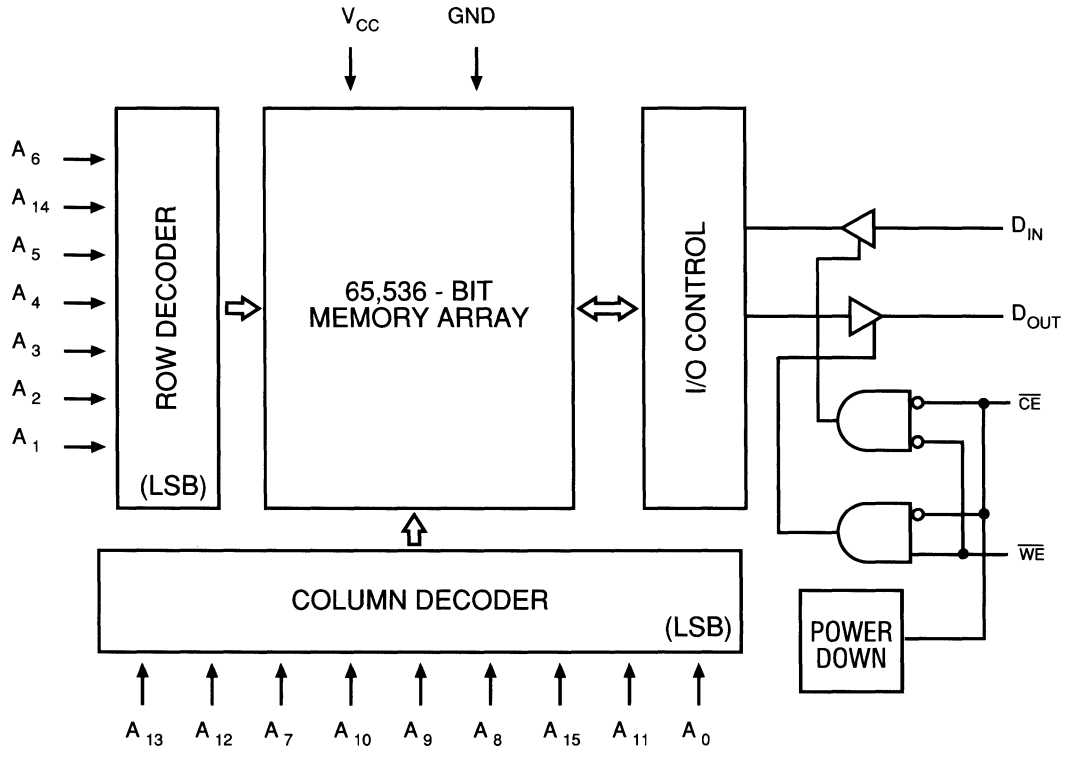
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology. All fabrication is 100% domestic.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	DOUT	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on any input relative to Vss ..... -2.0 to +7.0V
Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA
Lead Temperature (soldering, 10 seconds) ..... +260°C
Junction Temperature ..... +175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55°C \le T_C \le 125°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	6.0	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Output Open	I_{CC}	130	120	110	100	95	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max., $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ Hz	I_{SBT1}	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, V_{CC} = Max., f = 0Hz	I_{SBT2}	35	35	35	35	35	mA	
	$\overline{CE} \ge (V_{CC} - 0.2)$, V_{CC} = Max., all other inputs $\le 0.2V$ or $\ge (V_{CC} - 0.2V)$, f = 0Hz	I_{SBC2}	10	10	10	10	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz, V_{CC} = 5V	C_I		8	pF	4
Output Capacitance		C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-55°C ≤ T_C ≤ 125°C, Vcc = 5V ± 10%)

DESCRIPTION		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	15		20		25		30		35		ns	
Address access time	^tAA		15		20		25		30		35	ns	
Chip enable access time	^tACE		15		20		25		30		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		10		15		15		20		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		ns	
Chip disable to power down time	^tPD		15		20		25		30		35	ns	
WRITE Cycle													
WRITE cycle time	^tWC	15		20		25		30		35		ns	
Chip enable to end of write	^tCW	13		15		20		25		30		ns	
Address valid to end of write	^tAW	15		15		20		25		30		ns	
Address set-up time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
Write pulse width	^tWP	13		15		20		25		25		ns	
Data set-up time	^tDS	10		12		15		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

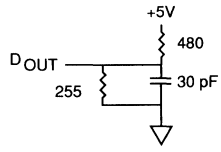


Fig. 1 OUTPUT LOAD EQUIVALENT

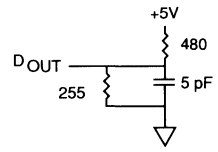


Fig. 2 OUTPUT LOAD EQUIVALENT

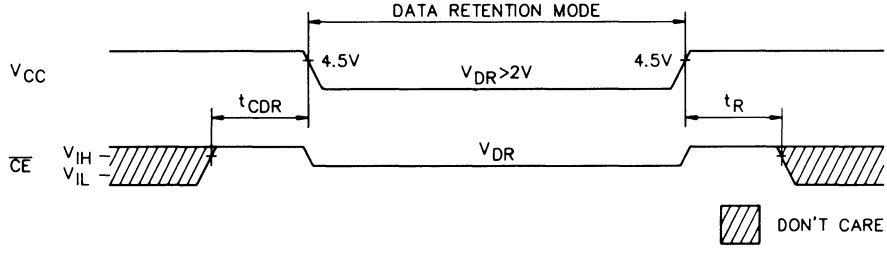
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the output unloaded, and $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ = Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are tested with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

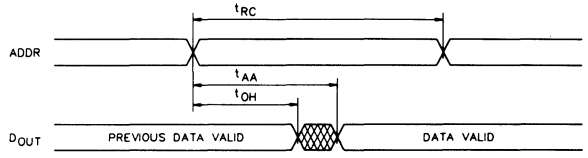
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2		—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	Vcc=2v	—	95	1000	µA
			Vcc=3v	—	350	1500	µA
$^{t}CDR^{(4)}$	Chip Deselect to Data Retention Time			0		—	ns
$^{t}R^{(4)}$	Operation Recovery Time			$^{t}RC^{(11)}$			ns

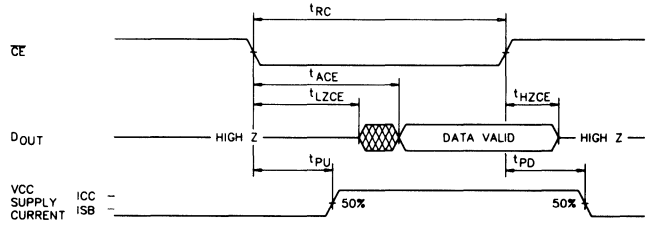
LOW Vcc DATA RETENTION WAVEFORM



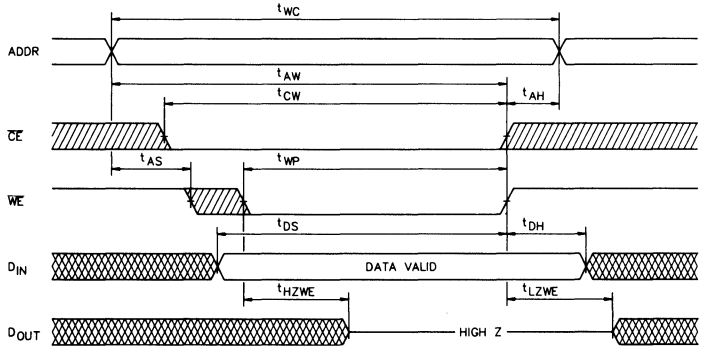
READ CYCLE NO. 1 (8, 9)



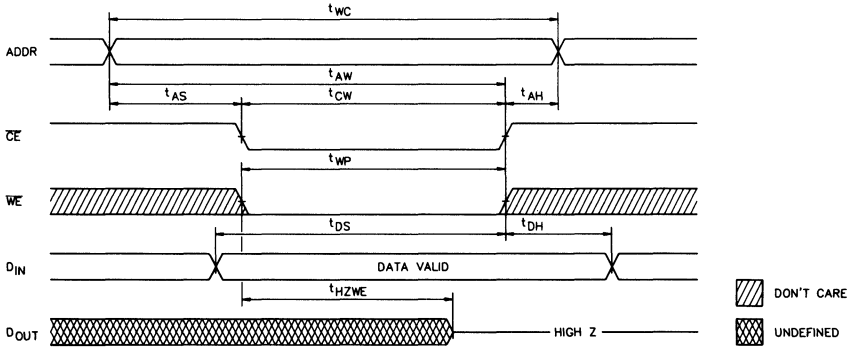
READ CYCLE NO. 2 (7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot.	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD-883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018 SEM Monitors	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD-883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented data sheet @ +125°C	100%
13. Burn-in	Method 1015	100%
14. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +125°C 5% PDA and in-line Group A per method 5005	100%
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
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19. Group A	Manufacturer's documented data sheet	Each lot/sublot
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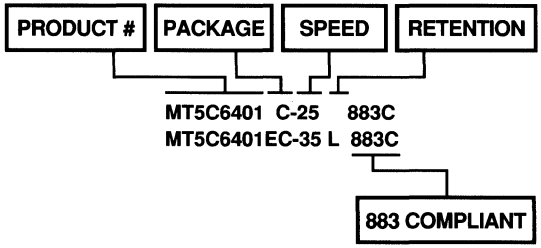

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MILITARY SRAM

64K x 4 SRAM

ADDITIONAL MILITARY SPECIFICATIONS

- SMD 88681
- JAN (consult factory for reference number)
- RAD-tolerant (consult factory)

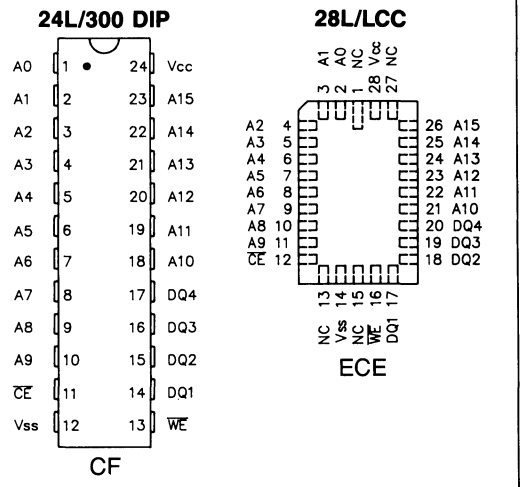
FEATURES

- Battery backup – 2 volt data retention
- High speed: 25, 30, 35 and 45ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS

	MARKING
• Timing	
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Ceramic DIP (300 mil)	C
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)



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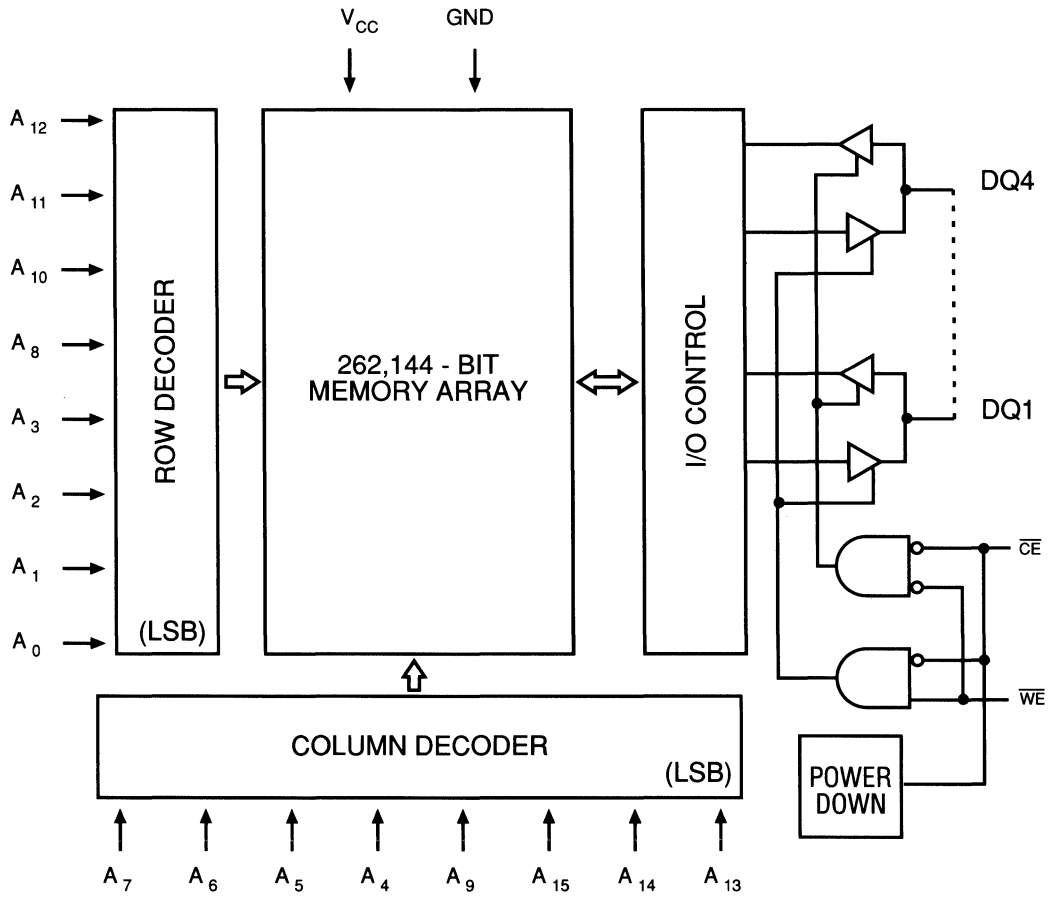
Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	DOUT	ACTIVE
WRITE	L	L	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on any input or DQ relative to V_{SS} -2.0V to +7.0V
Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA
Lead Temperature (soldering, 10 seconds) ..... +260°C
Juction Temperature ..... +175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55°C \le T_C \le 125°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	6.0	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}		100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max., $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ Hz	I_{SBT1}		40	mA	
	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, V_{CC} = Max., f = 0Hz	I_{SBT2}		20	mA	
	$\overline{CE} \ge (V_{CC} - 0.2V)$, V_{CC} = Max., all other inputs $\le 0.2V$ or $\ge (V_{CC} - 0.2V)$, f = 0Hz	I_{SBC2}		10	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Outputs Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz, V_{CC} = 5V	C_I		8	pF	4
Output Capacitance		C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-55°C ≤ T_C ≤ 125°C, V_{CC} = 5V ± 10%)

DESCRIPTION		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	t_{RC}	25		30		35		45		ns	
Address access time	t_{AA}		25		30		35		45	ns	
Chip enable access time	t_{ACE}		25		30		35		45	ns	
Output hold from address change	t_{OH}	5		5		5		5		ns	
Chip enable to output in low Z	t_{LZCE}	5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		15		20		20		20	ns	6, 7
Chip enable to power up time	t_{PU}	0		0		0		0		ns	
Chip disable to power down time	t_{PD}		25		30		35		45	ns	
WRITE Cycle											
WRITE cycle time	t_{WC}	25		30		35		45		ns	
Chip enable to end of write	t_{CW}	20		25		30		40		ns	
Address Valid to end of write	t_{AW}	20		25		30		40		ns	
Address set-up time	t_{AS}	0		0		0		0		ns	
Address hold from end of write	t_{AH}	2		2		2		2		ns	
Write pulse width	t_{WP}	20		25		25		30		ns	
Data set-up time	t_{DS}	16		18		20		20		ns	
Data hold time	t_{DH}	2		2		2		2		ns	
Write disable to output in low Z	t_{LZWE}	0		0		0		0		ns	
Write enable to output in high Z	t_{HZWE}	0	15	0	15	0	15	0	20	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Intput timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2

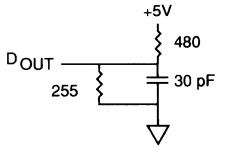


Fig. 1 OUTPUT LOAD EQUIVALENT

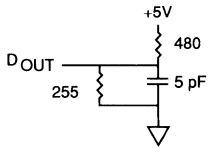


Fig. 2 OUTPUT LOAD EQUIVALENT

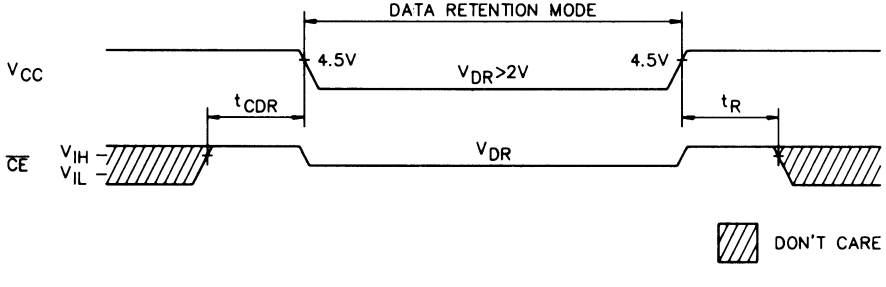
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. ICC is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

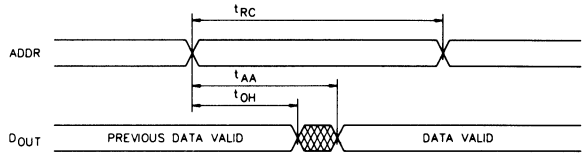
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
VDR	Vcc for Retention Data			2	—	V	
ICCDR	Data Retention Current	$\overline{CE} \geq$ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	—	95	1000	µA
			Vcc=3v	—	350	1500	µA
^{t}CDR(4)	Chip Deselect to Data Retention Time			0		—	ns
^{t}R(4)	Operation Recovery Time			^{t}RC(11)			ns

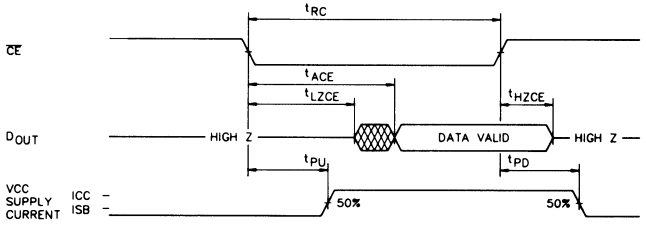
LOW Vcc DATA RETENTION WAVEFORM



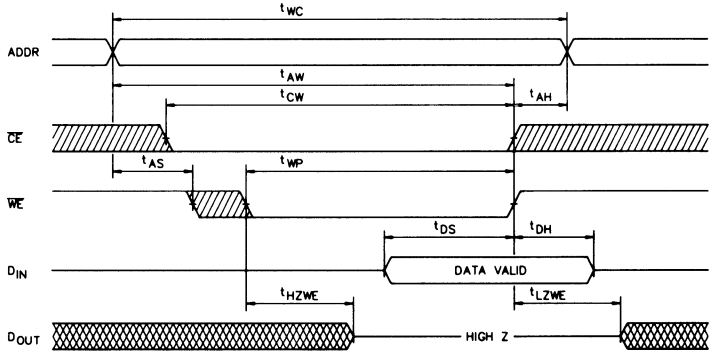
READ CYCLE NO. 1 (8, 9)



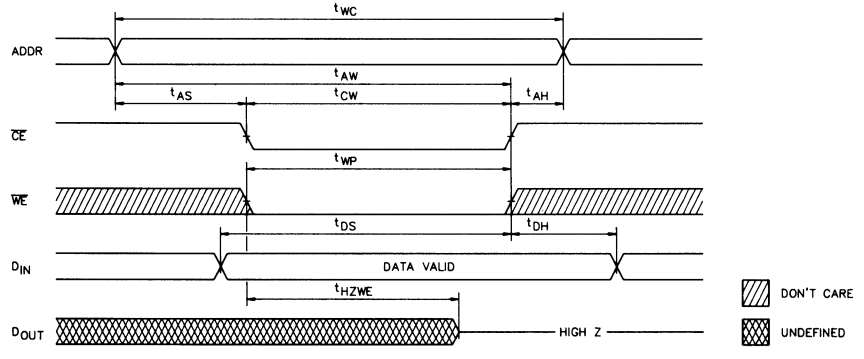
READ CYCLE NO. 2 (7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



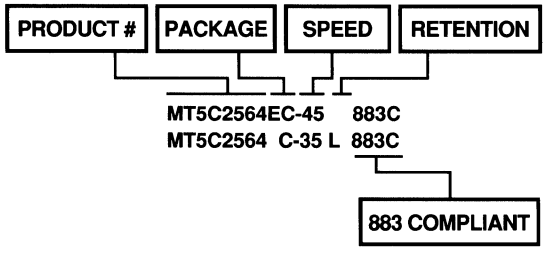
WRITE CYCLE NO. 2
(Chip Enable Controlled)



MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved.
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot.	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD 883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018 SEM Monitors	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD 883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented data sheet @ +125°C	100%
13. Burn-in	Method 1015	100%
14. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +125°C 5% PDA and in-line Group A per method 5005	100%
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection per Method 5005 (attributes data only)		
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and construction tests	Each package type on each lot
21. Group C	Die related	Micro circuit group/every quarter
22. Group D	Package related test	Each package type Generic every 26 weeks

ORDER INFORMATION



The Micron Fast SRAM family is functionally equivalent to other manufacturer's 883 compliant devices. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

MILITARY SRAM

256K x 1 SRAM

ADDITIONAL MILITARY SPECIFICATIONS

- SMD 88725
- JAN (consult factory for reference number)
- RAD-tolerant (consult factory)

FEATURES

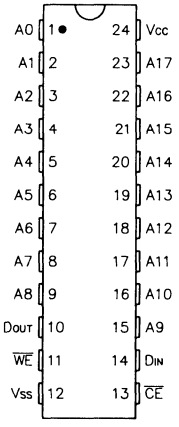
- Battery backup – 2 volt data retention
- High speed: 25, 30, 35 and 45ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS / MARKING

• Timing	
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Ceramic DIP (300 mil)	C
Ceramic LCC	EC
• Two Volt Data Retention	L

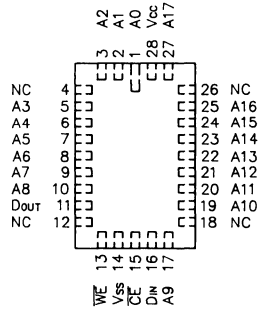
PIN ASSIGNMENT (Top View)

24L/300 DIP



CF

28L/LCC



ECE

GENERAL DESCRIPTION

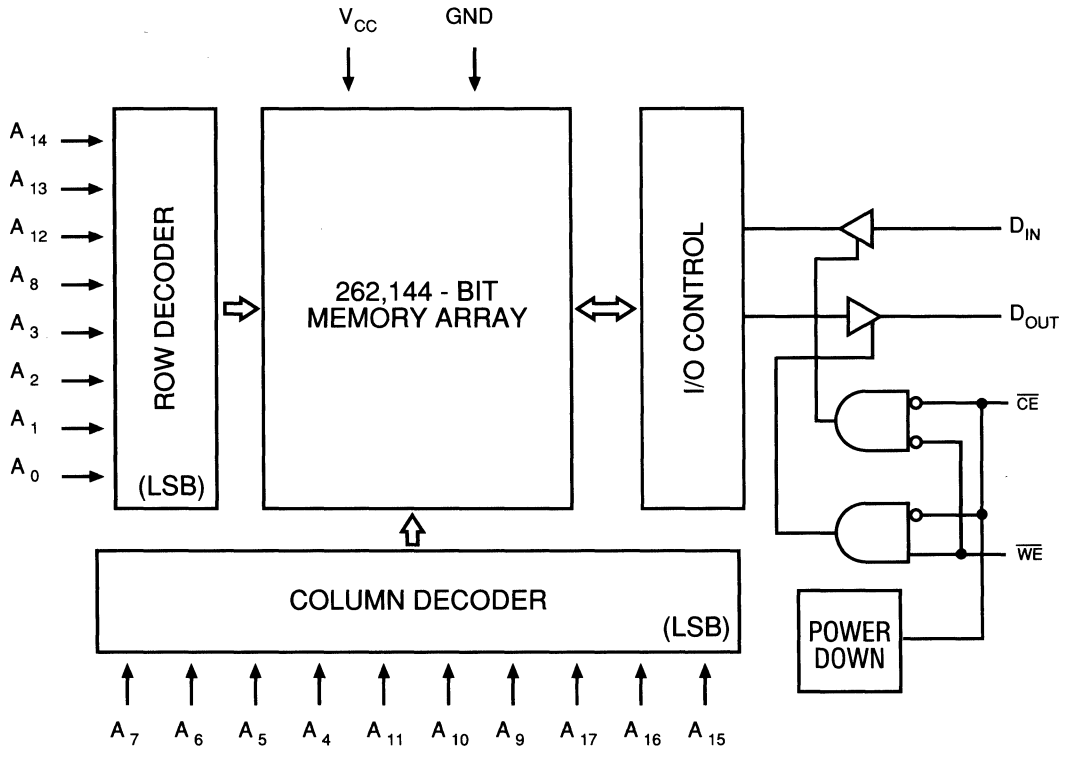
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	DOUT	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on any input relative to V_{SS} ..... -2.0V to +7.0V
Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Voltage applied to D_{OUT} ..... -1.0V to 6.0V
Storage Temperature ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA
Lead Temperature (soldering, 10 seconds) ..... +260°C
Juction Temperature ..... +175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55°C \le T_C \le 125°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	6.0	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Output Open	I_{CC}		100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max., $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ Hz	I_{SBT1}		40	mA	
	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, V_{CC} = Max., f = 0Hz	I_{SBT2}		20	mA	
	$\overline{CE} \ge (V_{CC} - 0.2V)$, V_{CC} = Max., all other inputs $\le 0.2V$ or $\ge (V_{CC} - 0.2V)$, f = 0Hz	I_{SBC2}		10	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz, V_{CC} = 5V	C_I		8	pF	4
Output Capacitance		C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-55°C ≤ T_C ≤ 125°C, Vcc = 5V ± 10%)

DESCRIPTION		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	25		30		35		45		ns	
Address access time	^tAA		25		30		35		45	ns	
Chip enable access time	^tACE		25		30		35		45	ns	
Output hold from address change	^tOH	5		5		5		5		ns	
Chip enable to output in low Z	^tLZCE	5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		15		20		20		20	ns	6, 7
Chip enable to power up time	^tPU	0		0		0		0		ns	
Chip disable to power down time	^tPD		25		30		35		45	ns	
WRITE Cycle											
WRITE cycle time	^tWC	25		30		35		45		ns	
Chip enable to end of write	^tCW	20		25		30		40		ns	
Address Valid to end of write	^tAW	20		25		30		40		ns	
Address set-up time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	2		2		2		2		ns	
Write pulse width	^tWP	20		25		25		30		ns	
Data set-up time	^tDS	16		18		20		20		ns	
Data hold time	^tDH	2		2		2		2		ns	
Write disable to output in low Z	^tLZWE	0		0		0		0		ns	
Write enable to output in high Z	^tHZWE	0	15	0	15	0	15	0	20	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2

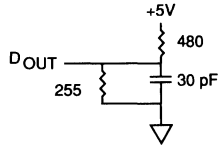


Fig. 1 OUTPUT LOAD EQUIVALENT

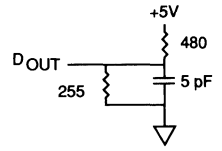


Fig. 2 OUTPUT LOAD EQUIVALENT

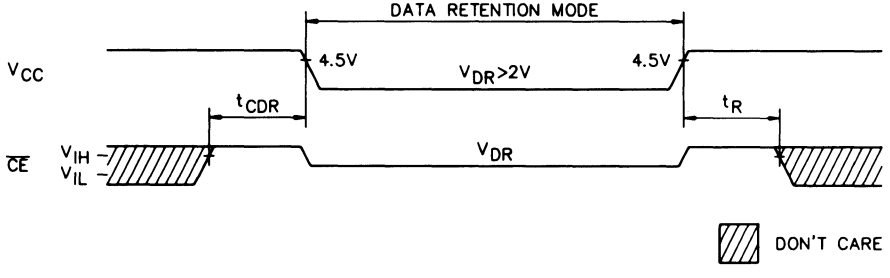
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the output unloaded, and $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are tested with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. ^{t}RC = Read Cycle Time. (Page 4)

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

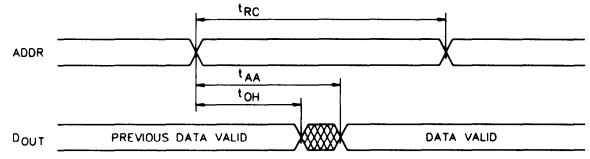
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DR}	Vcc for Retention Data			2	—	V	
I_{CCDR}	Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	Vcc=2v	—	95	1000	µA
			Vcc=3v	—	350	1500	µA
^{t}CDR(4)	Chip Deselect to Data Retention Time			0		—	ns
^{t}R(4)	Operation Recovery Time			^{t}RC(11)			ns

LOW Vcc DATA RETENTION WAVEFORM

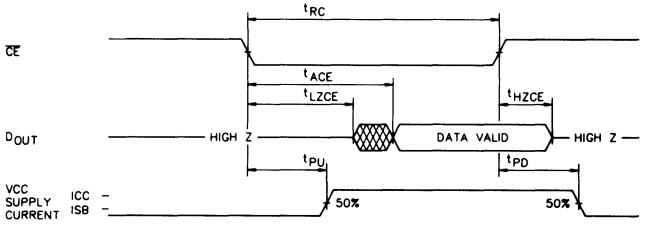


MILITARY FAST SRAM

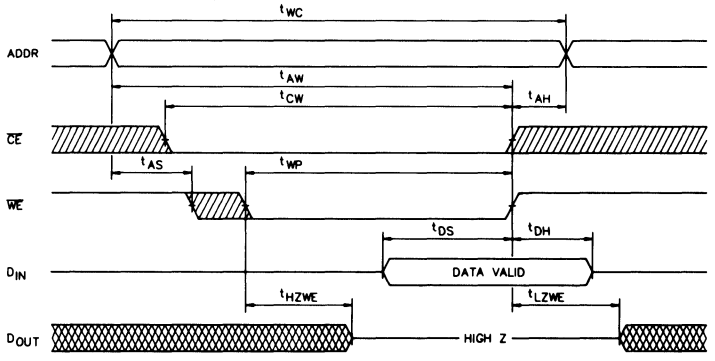
READ CYCLE NO. 1 (8, 9)



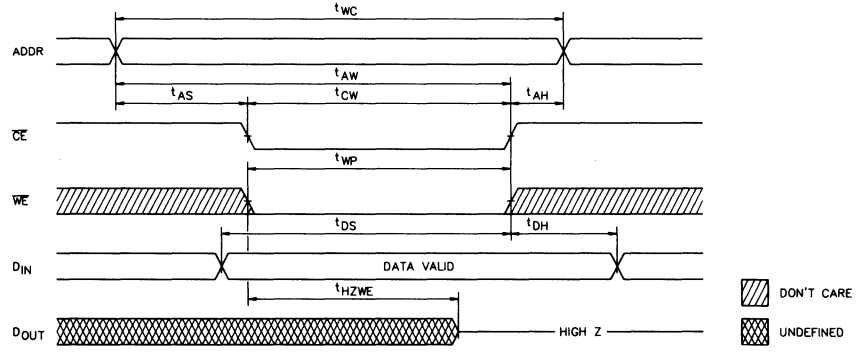
READ CYCLE NO. 2 (7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



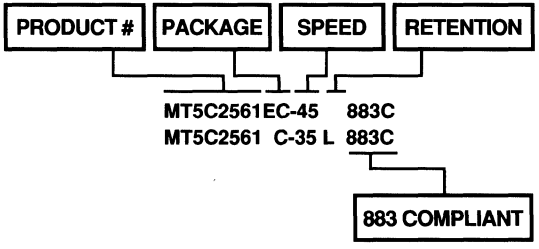
WRITE CYCLE NO. 2
(Chip Enable Controlled)



MICRON MIL-STD 883C PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev C	Establish and implement a product assurance program plan and qualification test plan.	Approved
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot.	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembed and tested in Boise, Idaho USA.
MIL-STD 883 Fabrication		
5. Incoming Inspections All Direct Materials	MIL-STD-105D	In-line
6. Wafer Fabrication	Method 2018 SEM Monitors	100%
7. Assembly	Class B Process Monitors	100%
MIL-STD 883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented data sheet @ +125°C	100%
13. Burn-in	Method 1015	100%
14. Final Electrical Post Burn-in Test	Method 5004, Class B, 3.1.16 @ -55°C, +25°C, +125°C 5% PDA and in-line Group A per method 5005	100%
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
18. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
Quality Conformance Inspection per Method 5005 (attributes data only)		
19. Group A	Manufacturer's documented data sheet	Each lot/sublot
20. Group B	Package functional and construction tests	Each package type on each lot
21. Group C	Die related	Micro circuit group/every quarter
22. Group D	Package related test	Each package type Generic every 26 weeks

ORDER INFORMATION



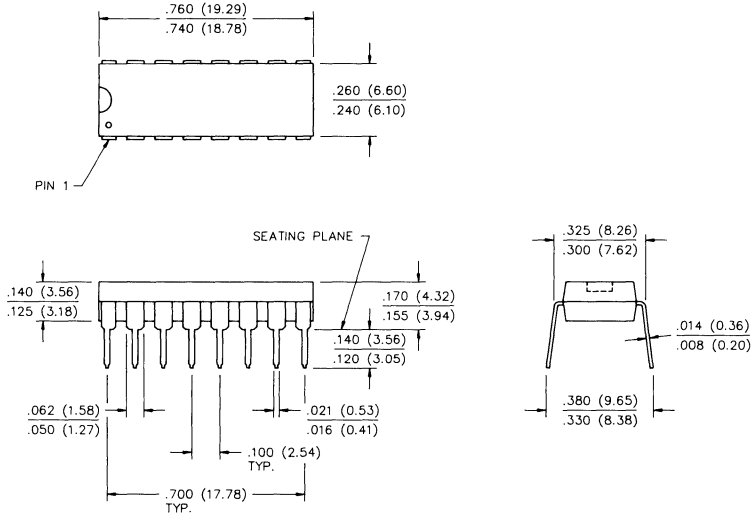
The Micron Fast SRAM family is functionally equivalent to other manufacturer's 883 compliant devices. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.

MICRON

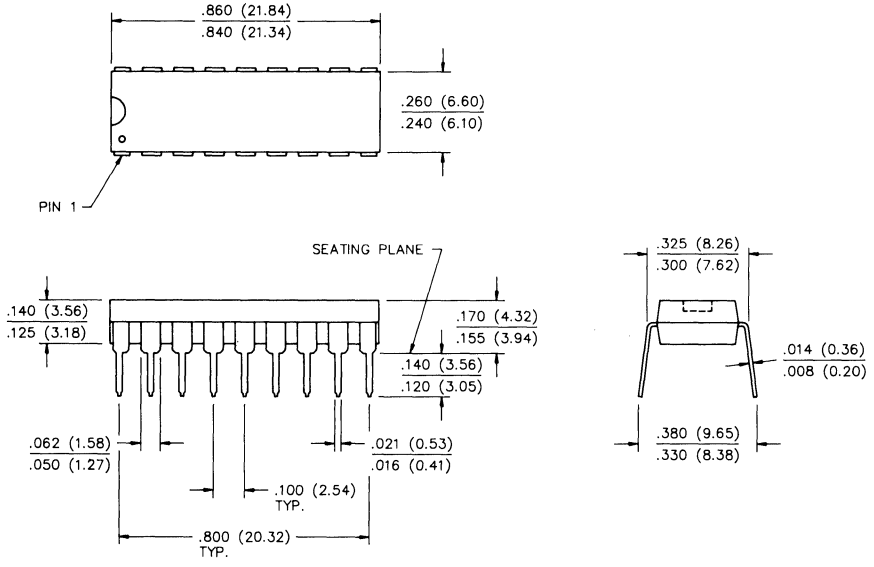
TABLE OF CONTENTS

16-PIN PLASTIC DIP
PA



All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

18-PIN PLASTIC DIP
PB



All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

18-PIN PLASTIC DIP
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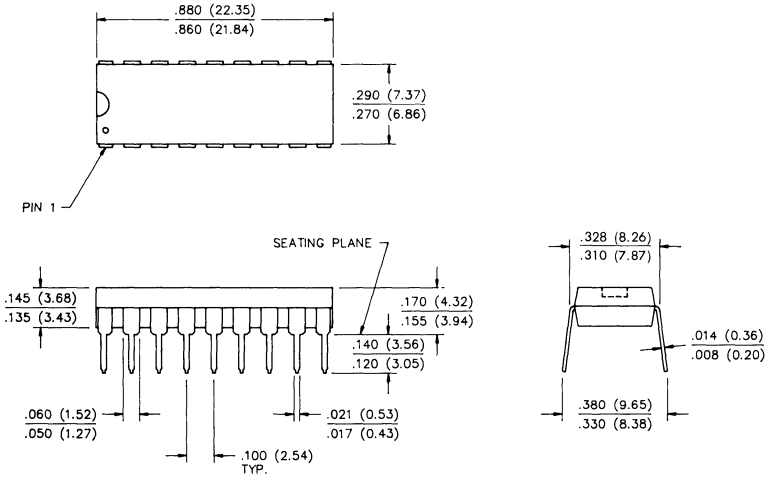
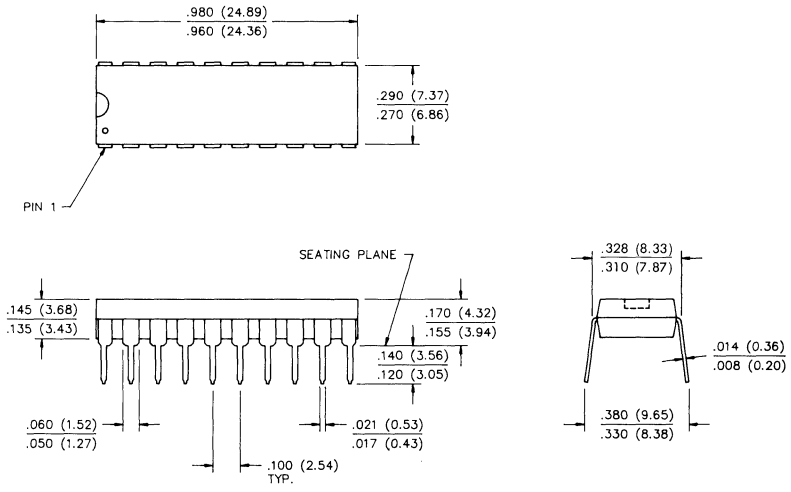


All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

20-PIN PLASTIC DIP
PD



All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

20-PIN PLASTIC DIP
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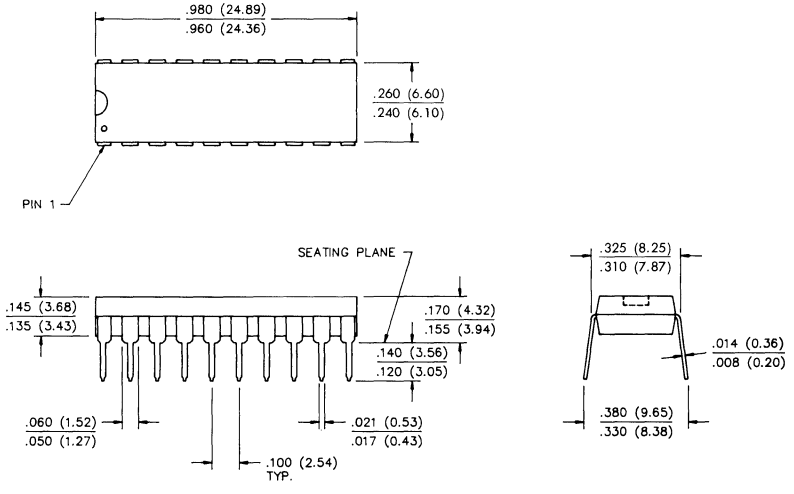
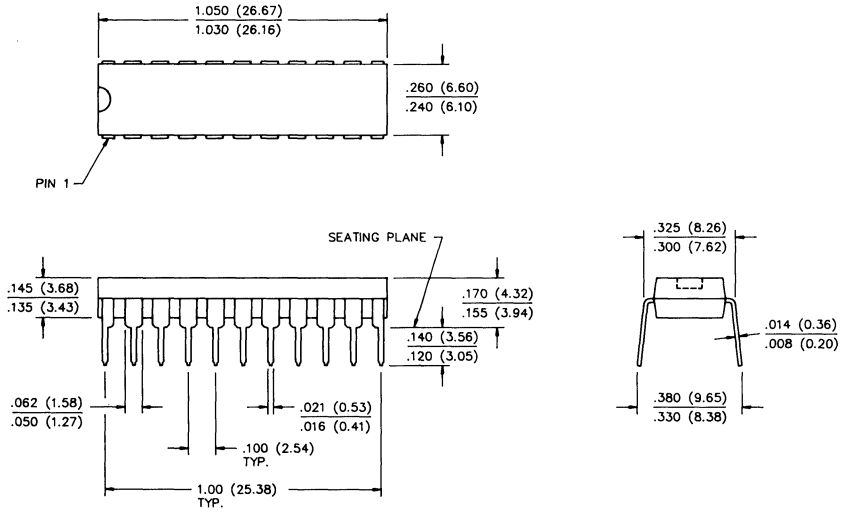


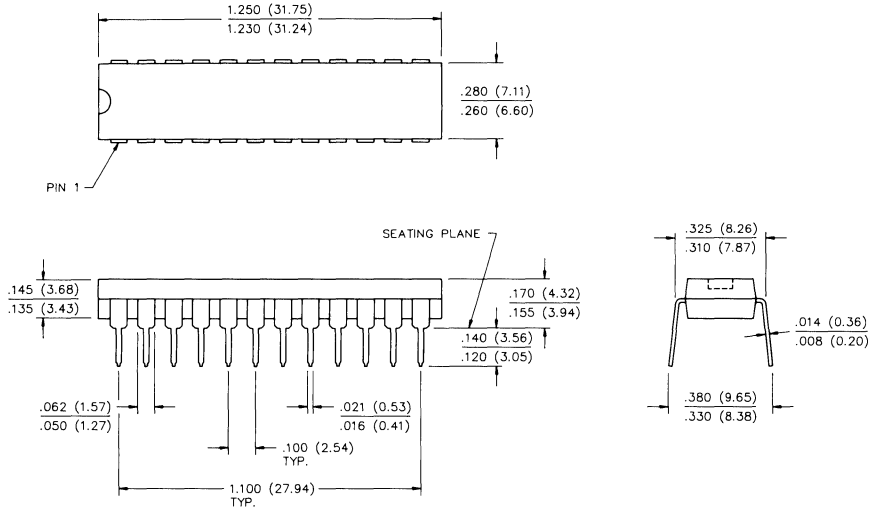
All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

22-PIN PLASTIC DIP
PF



All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$

24-PIN PLASTIC DIP
PG



All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

24-PIN PLASTIC DIP
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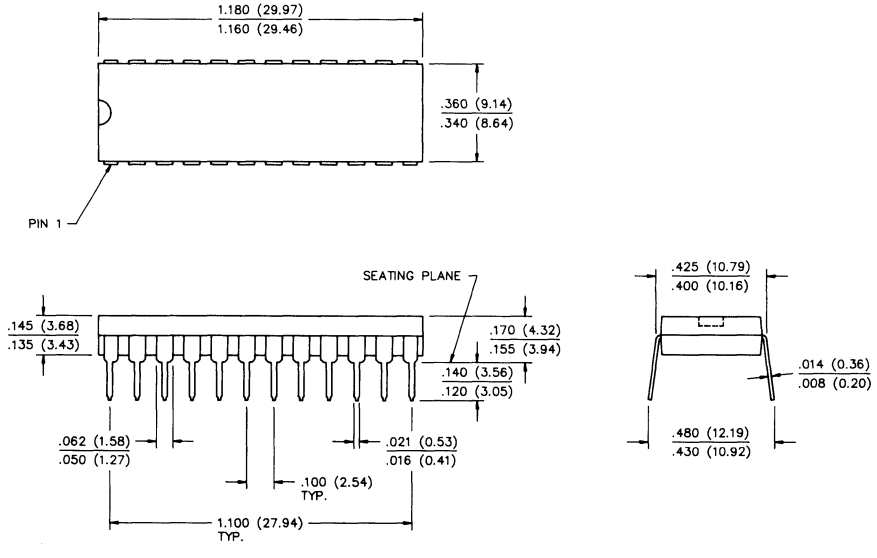
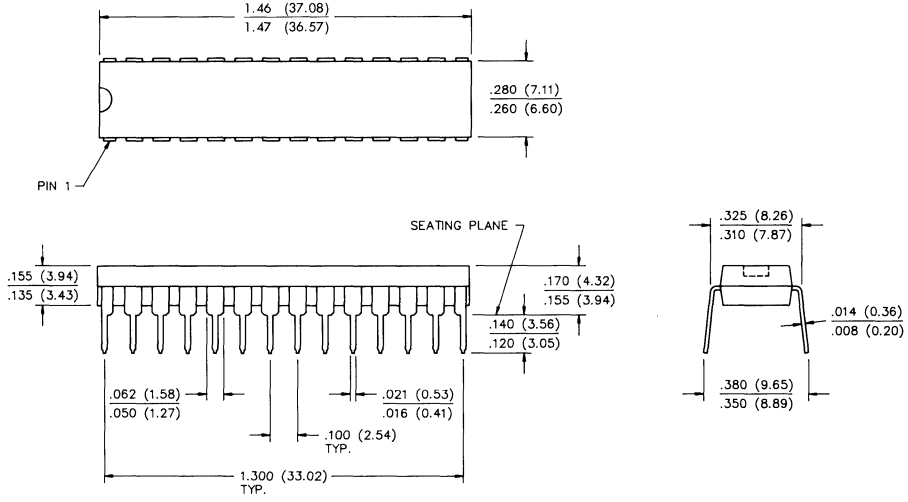


All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

28-PIN PLASTIC DIP
PJ



All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

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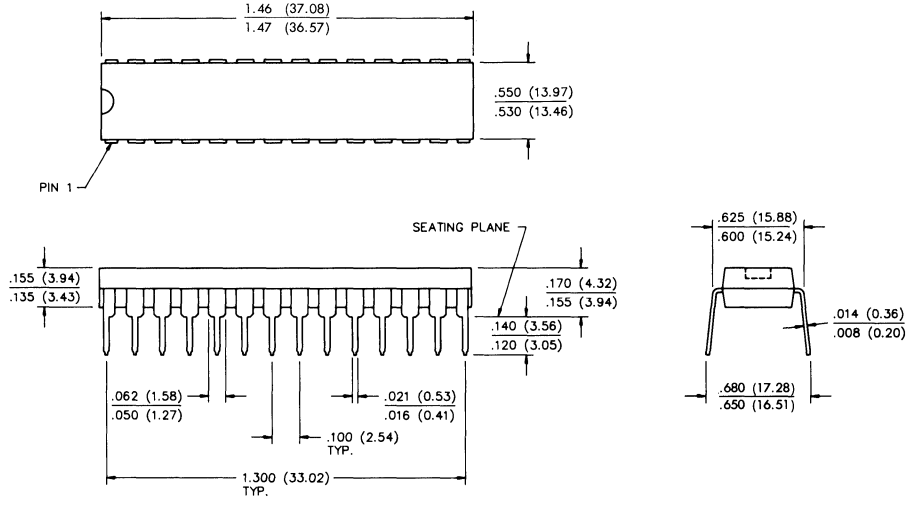

All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

16-PIN CERAMIC DIP
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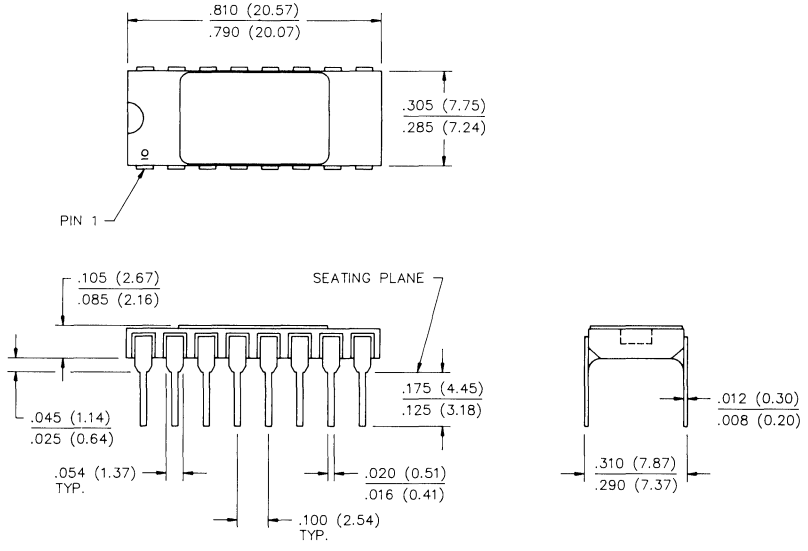
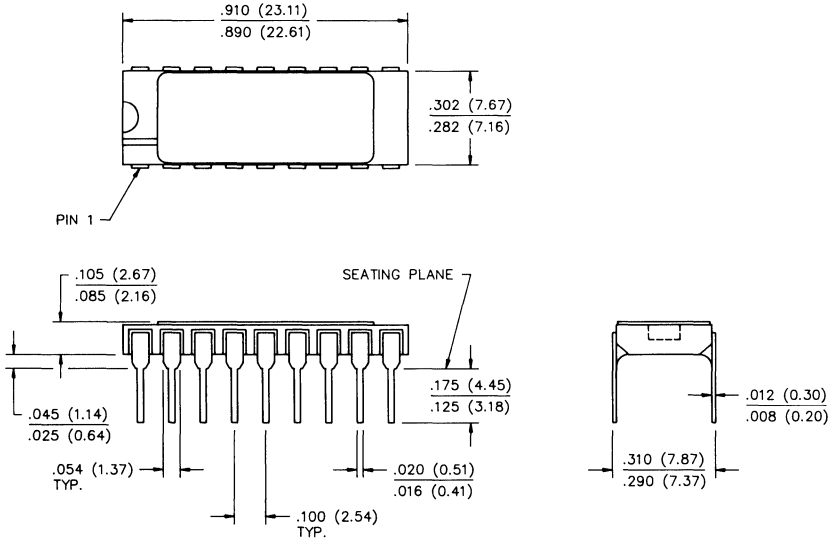


All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

18-PIN CERAMIC DIP
CB



All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

18-PIN CERAMIC DIP
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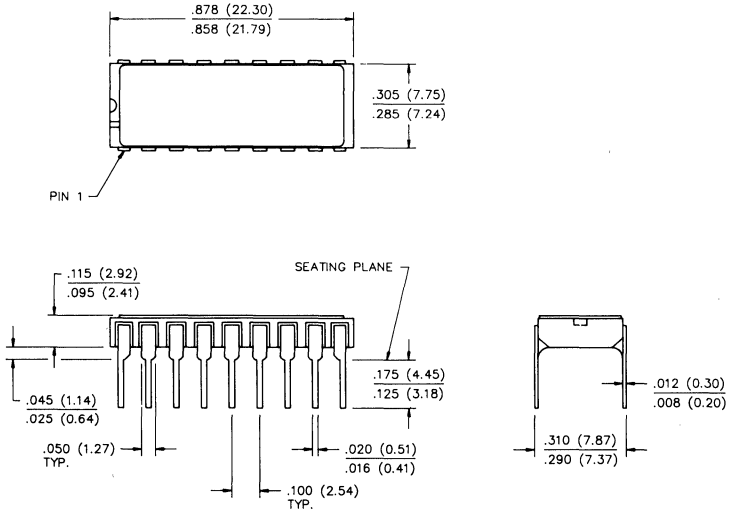

All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

20-PIN CERAMIC DIP
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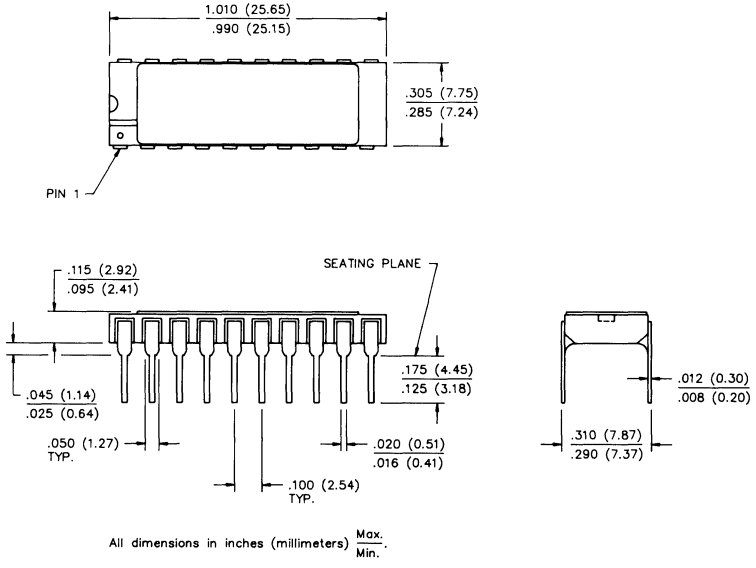

All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

22-PIN CERAMIC DIP
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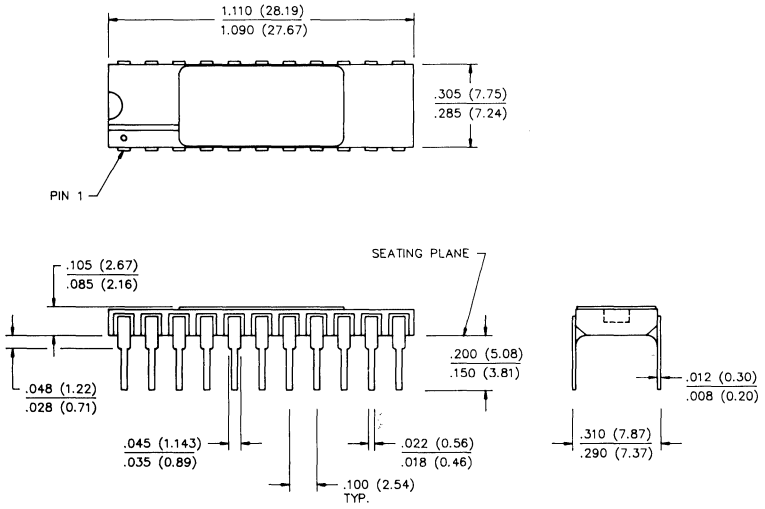

All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

24-PIN CERAMIC DIP
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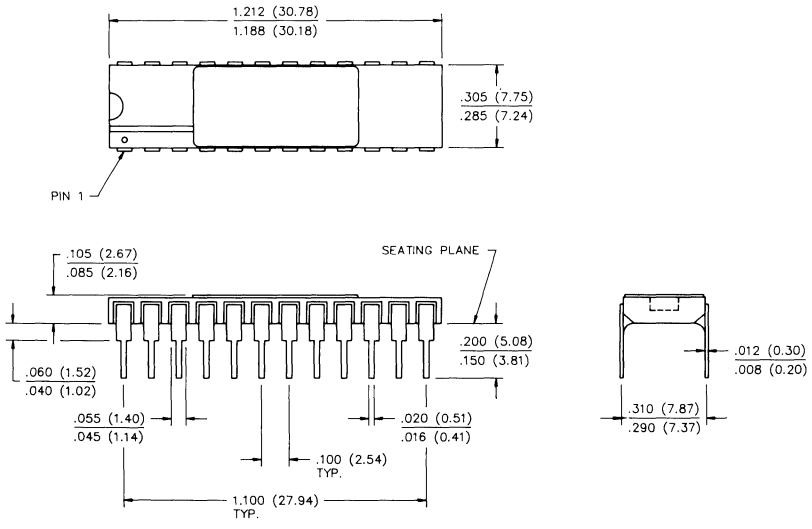

All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

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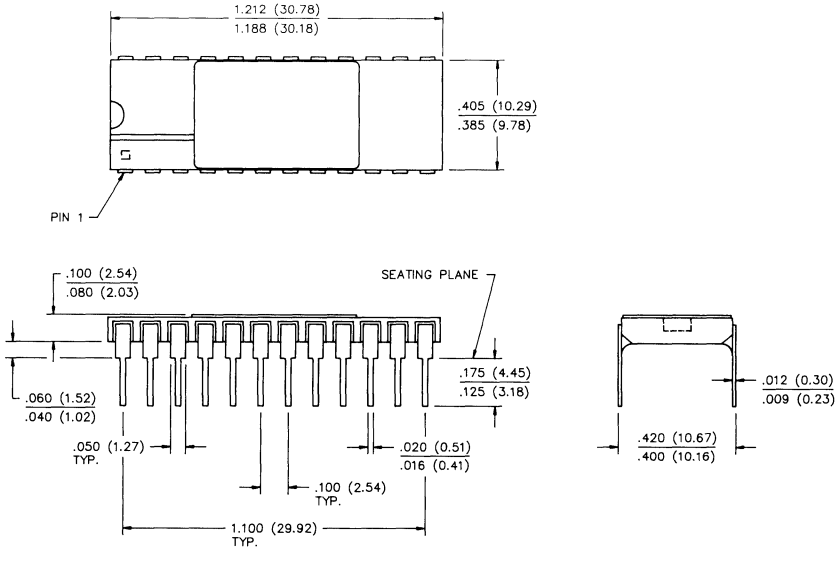
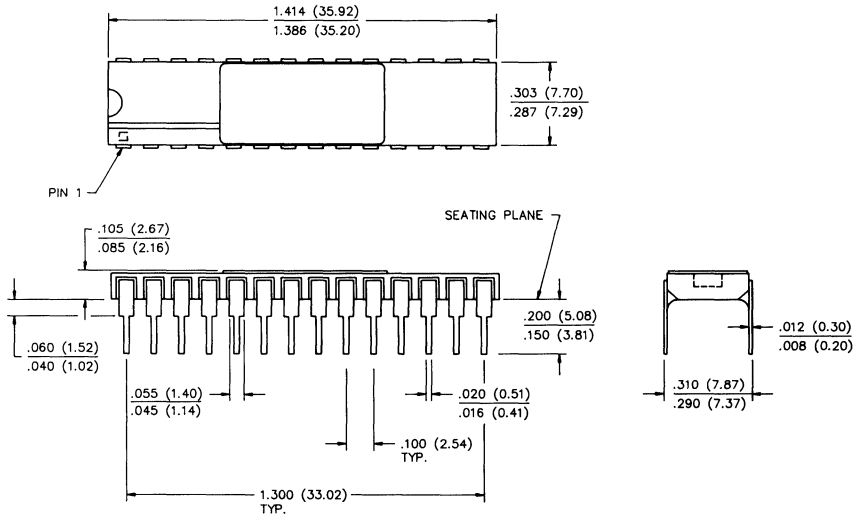


All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

28-PIN CERAMIC DIP
CH



All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

16-PIN PLASTIC ZIP
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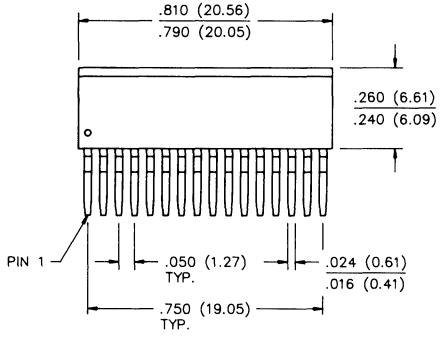
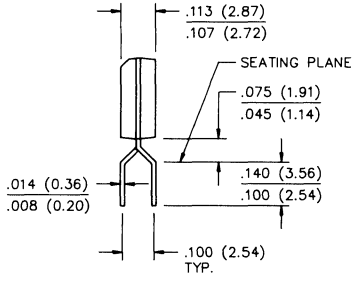
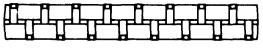
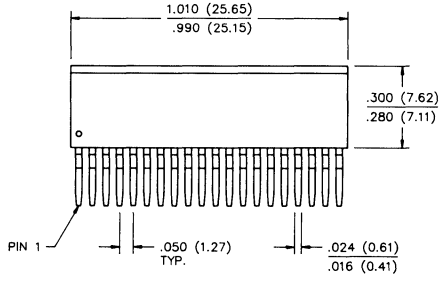


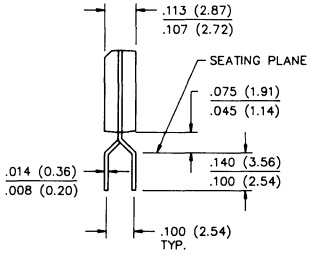


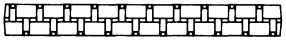


All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$

20-PIN PLASTIC ZIP
ZB

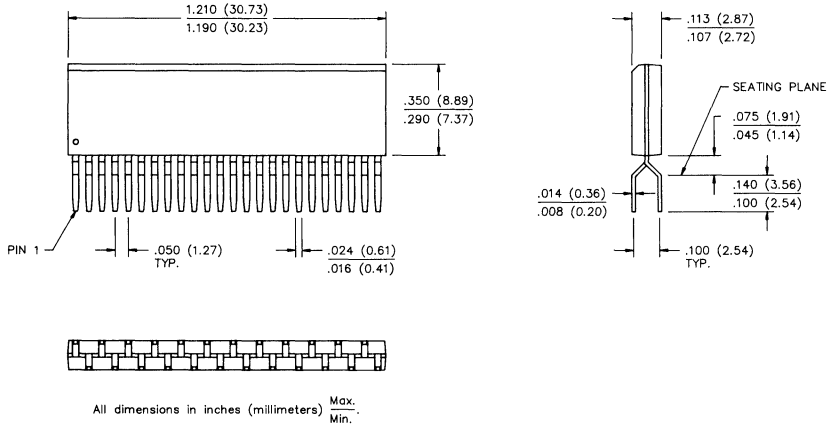






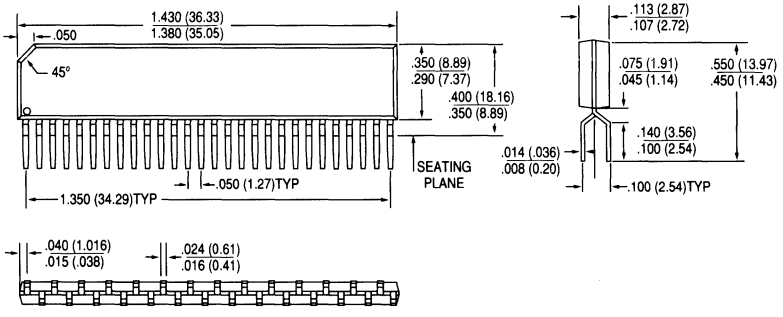
All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$

24-PIN PLASTIC ZIP
ZC



All dimensions in inches (millimeters) Max./Min.

28-PIN PLASTIC ZIP
ZD



18-PIN PLCC
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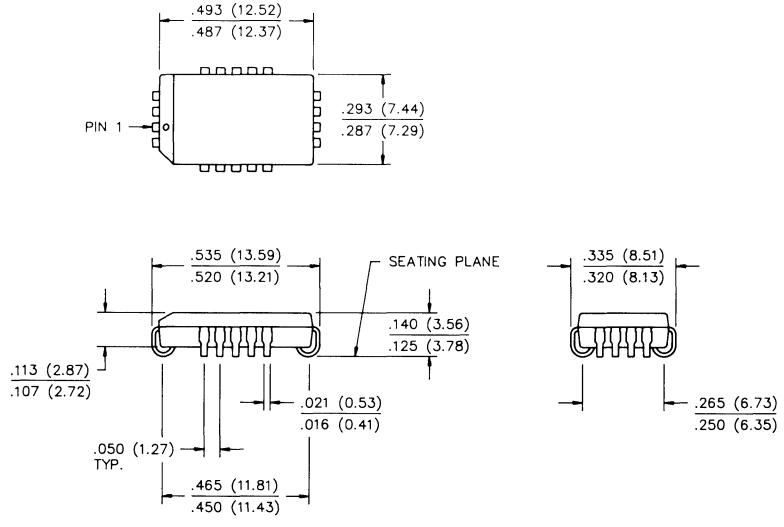
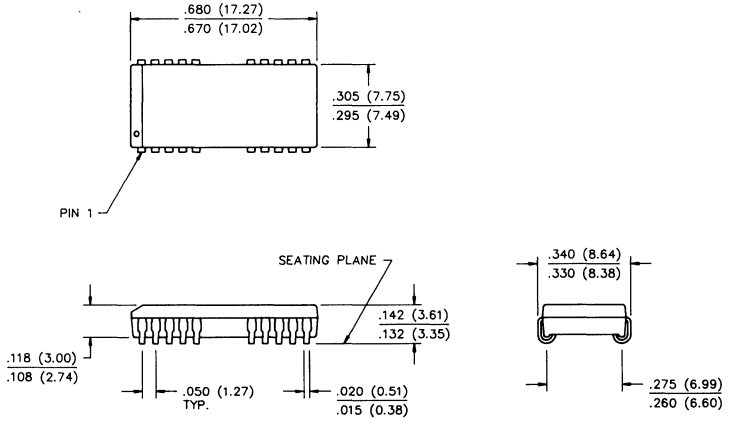


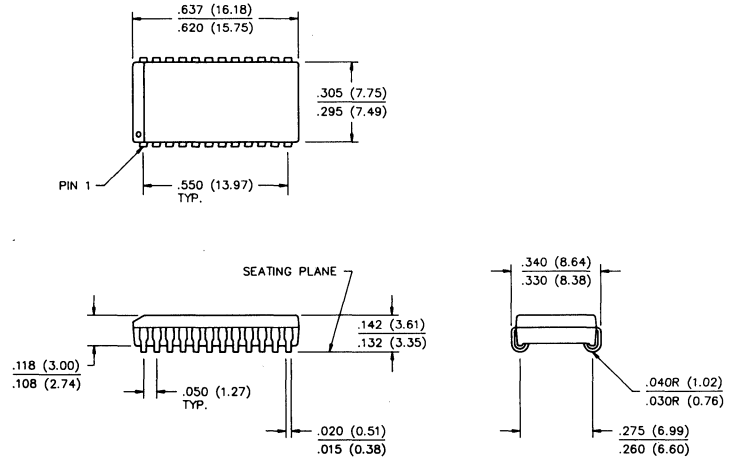
All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

20-PIN PLASTIC SOJ
DJA



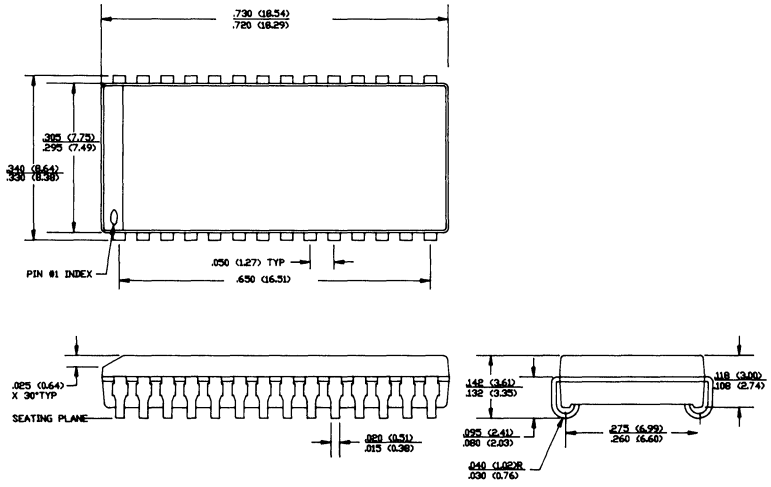
All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

24-PIN PLASTIC SOJ
DJB

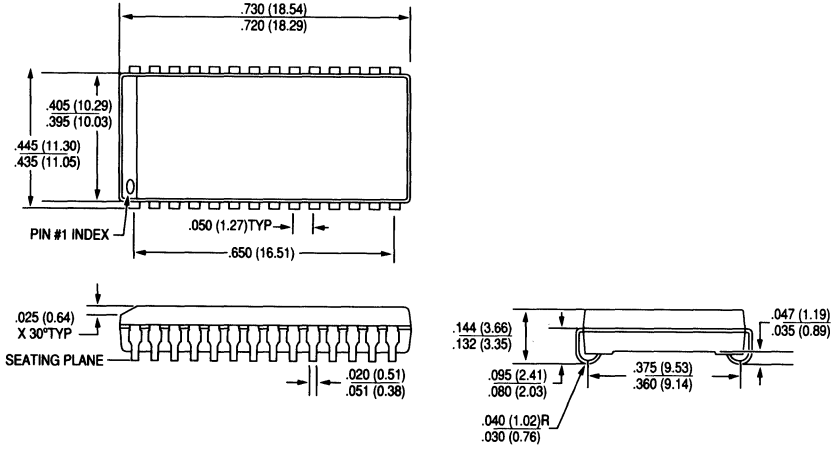


All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

28-PIN PLASTIC SOJ
DJC

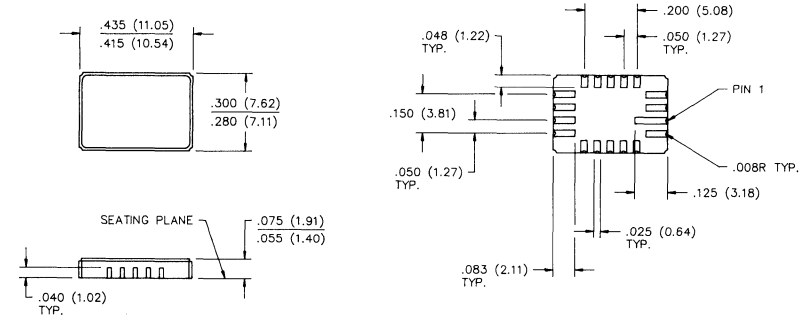


28-PIN PLASTIC SOJ
DJD



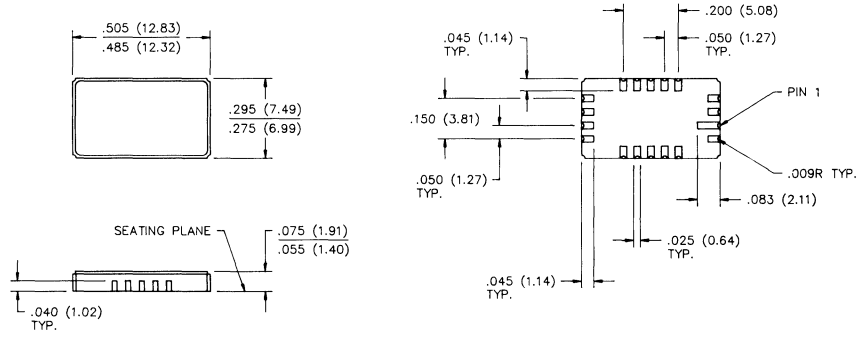
All dimensions in inches (millimeters) Max. / Min.

18-PIN CERAMIC LCC
ECA



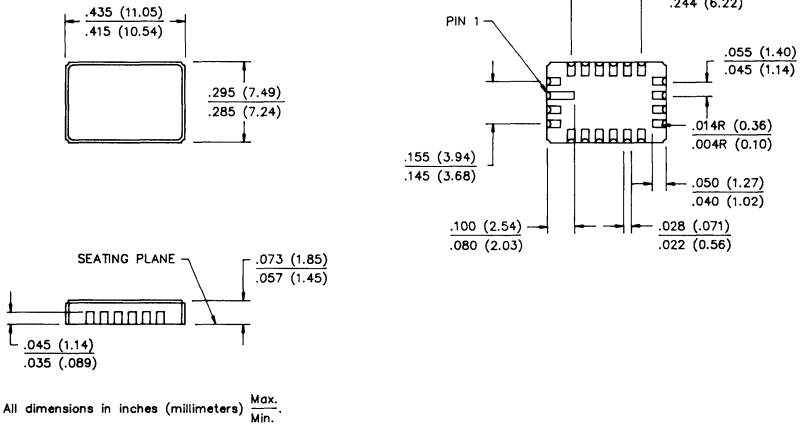
All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

18-PIN CERAMIC LCC
ECB



All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

20-PIN CERAMIC LCC
ECC



All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

22-PIN CERAMIC LCC
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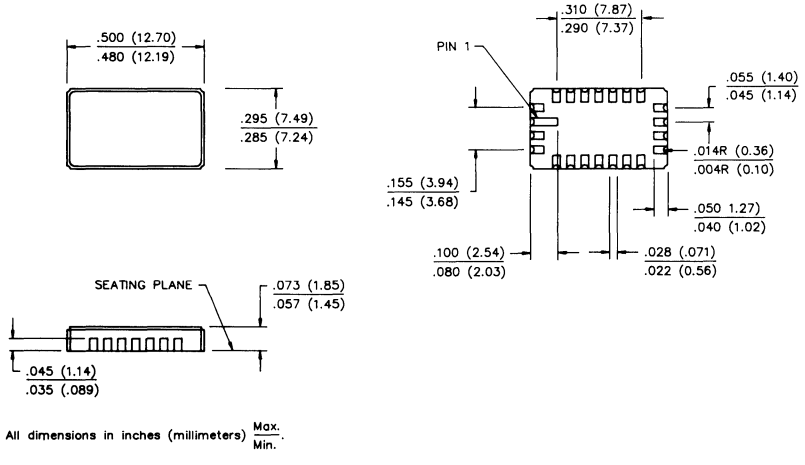
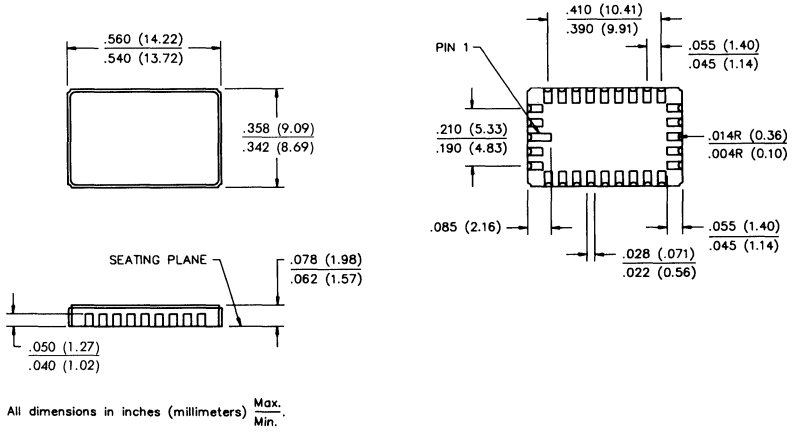


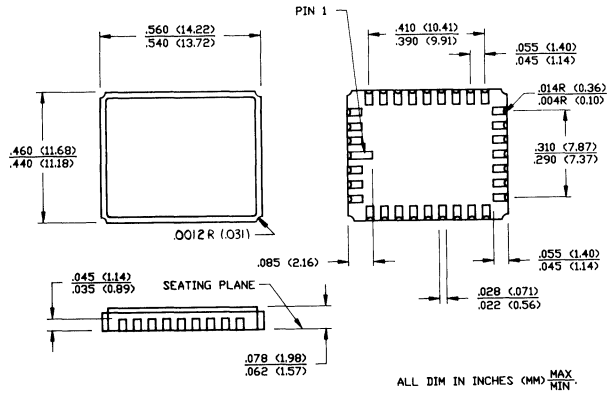
All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

28-PIN CERAMIC LCC
ECE



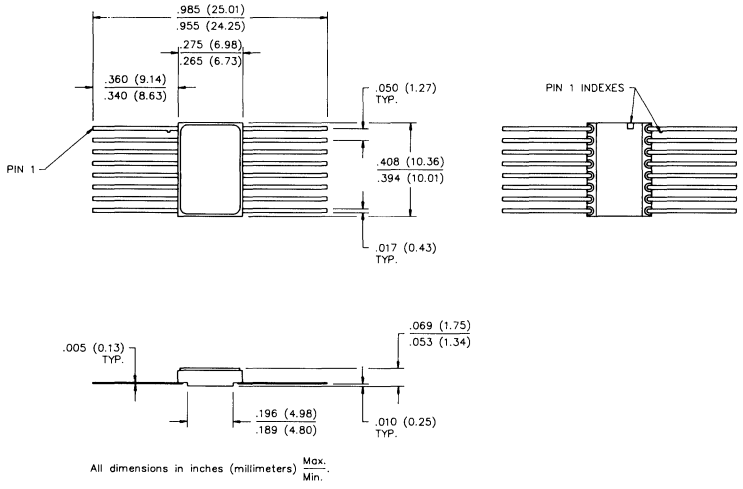
All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

32-PIN CERAMIC LCC
ECF



ALL DIM IN INCHES (MM) $\frac{\text{MAX}}{\text{MIN}}$.

16-PIN FLAT PACK
FA



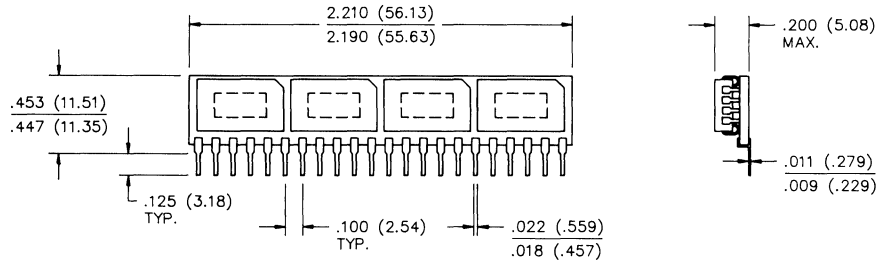
18-PIN FLAT PACK

TBD

20-PIN FLAT PACK

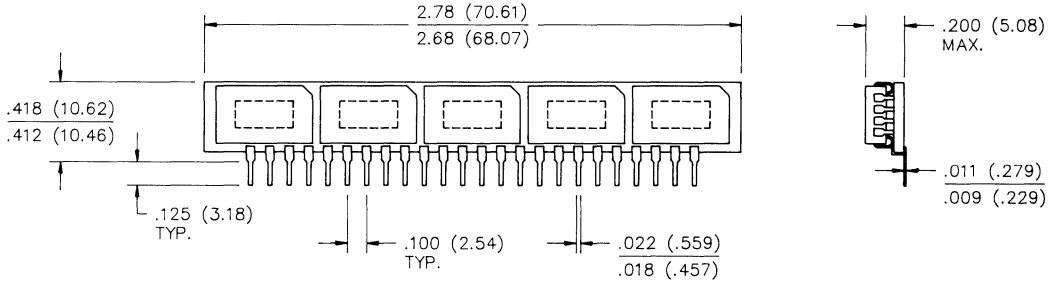
TBD

22-PIN MODULE SIP
MA



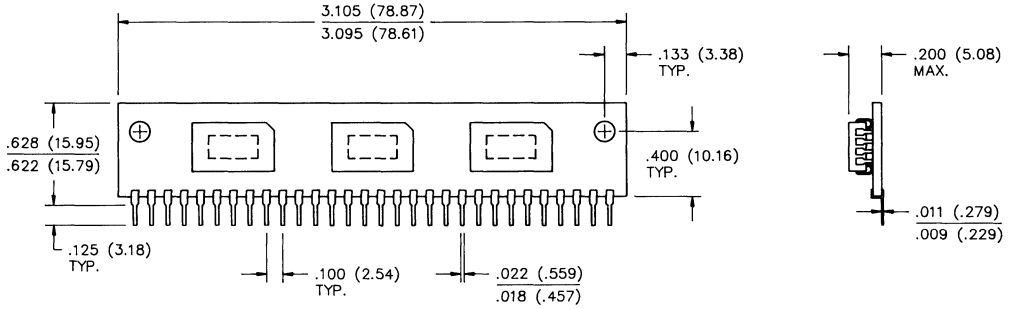
All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

24-PIN MODULE SIP
MB



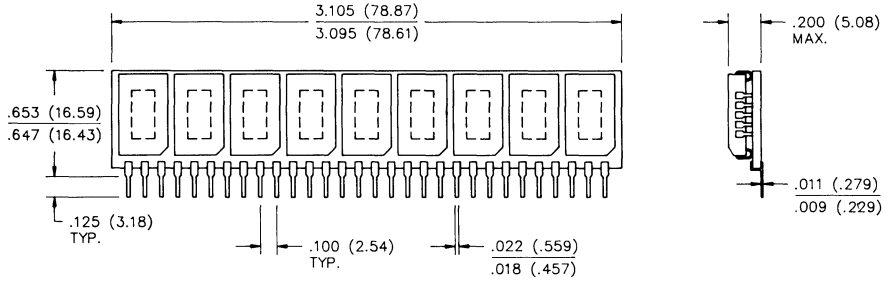
All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

30-PIN MODULE SIP
MC



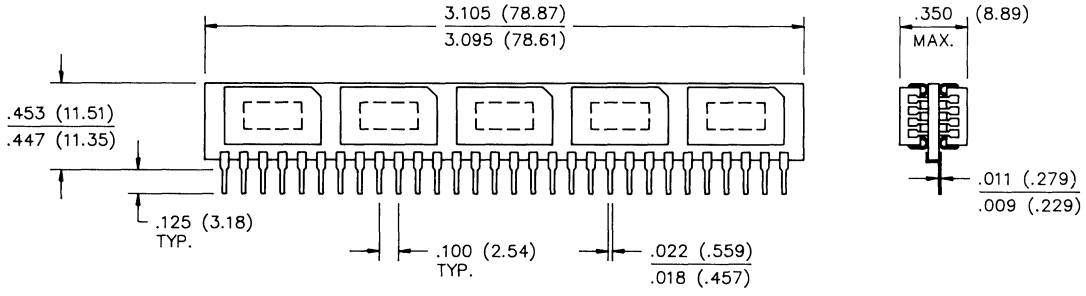
All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

30-PIN MODULE SIP
MD



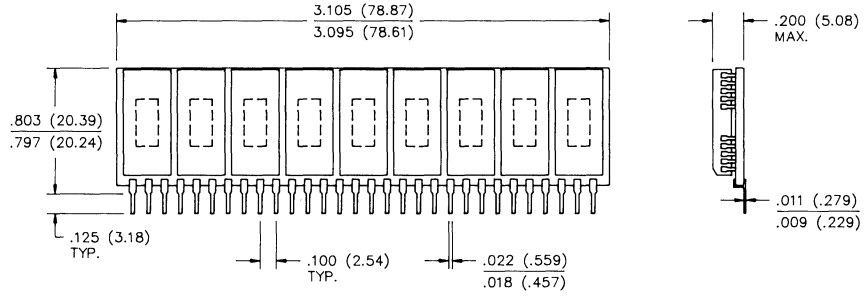
All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

30-PIN MODULE SIP
ME



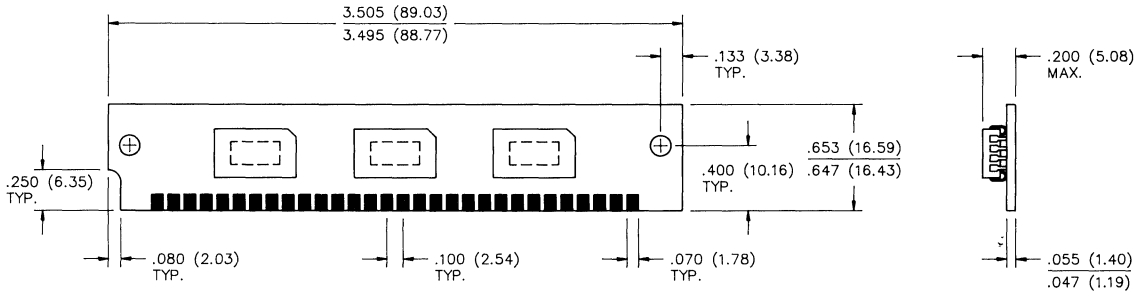
All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

30-PIN MODULE SIP
MG

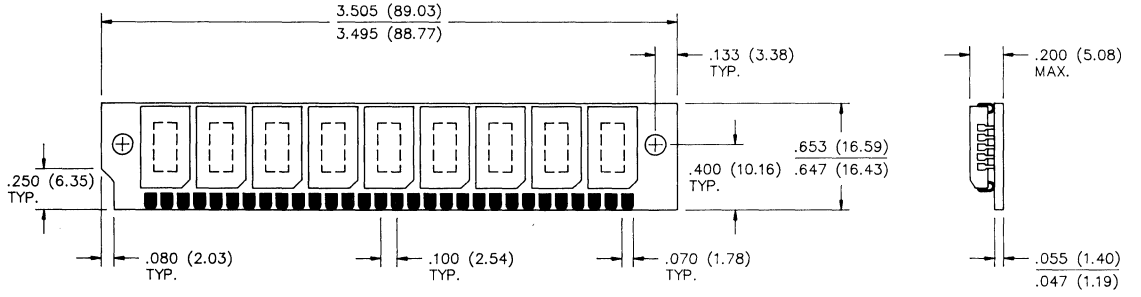


All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

30-PIN MODULE SIMM
MH

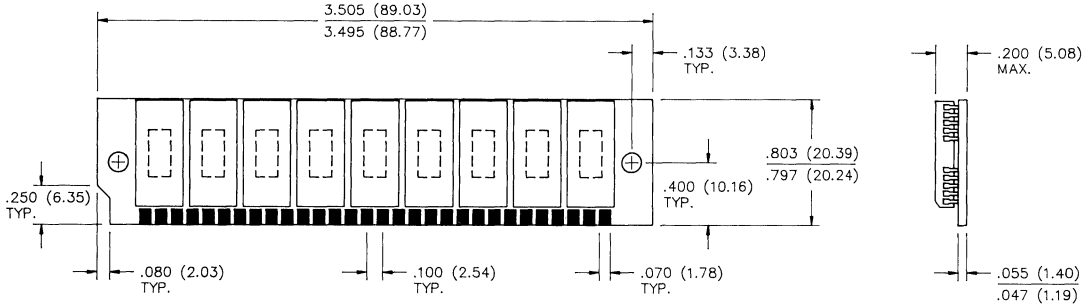


30-PIN MODULE SIMM
MI



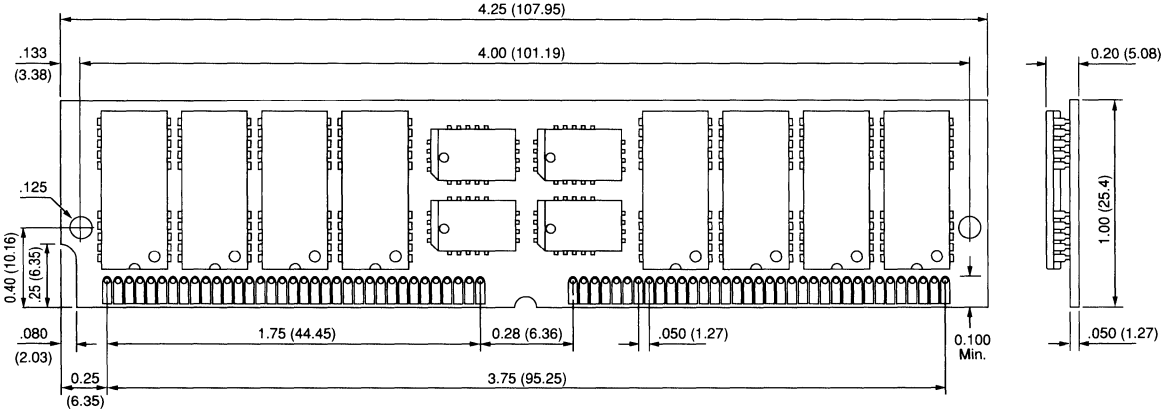
All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

30-PIN MODULE SIMM
MJ



All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min.}}$.

72-PIN MODULE SIMM
MK



Notes: All dimensions are in inches (millimeters). Tolerances are to be determined.

Micron Component Group Product Numbering

Format = AA BB CC DDDD EEE-FF GGGG

AA BB CC DDDD EEE FF GGGG

PRODUCT LINE INDENTIFIER

MT = Micron Technology Component Product

PRODUCT FAMILY

DRAM	= 4
DPDRAM	=42
SRAM	= 5
FIFO	=52
CACHE DATA	=56
MODULE	
DRAM	= 8
DPDRAM	=82
SRAM	=85
CUSTOM	=83

PROCESS TECHNOLOGY

NMOS	=BLANK
CMOS	=C

DEVICE NUMBER

(NUMBER CAN BE MODIFIED TO INDICATE VARIATIONS)

DRAM	=BITS, WORDS
DPDRAM	=BITS, WORDS
MODULE	=BITS, WORDS
SRAM	=DENSITY, BITS
DPSRAM	=BITS, WORDS
FIFO	=BITS, WORDS

PACKAGE CODE

PLASTIC	
DIP	=BLANK
DIP (WIDE BODY)	=W
ZIP	=Z
PLCC	=EJ
SOJ	=DJ
SOIC	=G
CERAMIC	
DIP	=C
DIP (WIDE BODY)	=CW
CLCC	=EC
CLC (WIDE BODY)	=ECW
SOJ	=CJ
SOIC	=CG
PGA	=CA
MODULE	
SIMM	=M
SIMM (GOLD PLATED)	=GM
SIP	=MN,N
DOUBLE SIDED SIP	=DMN,DN
ZIG-ZAG SIP	=ZN

PROCESSING LEVEL/TEMP/SPECIAL

ACCESS TIME

-10 = 10ns or 100ns
-12 = 12ns or 120ns
-15 = 15ns or 150ns
-20 = 20ns or 200ns
-25 = 25ns or 250ns
-35 = 35ns or 350ns
-45 = 45ns
-55 = 55ns
-60 = 60ns
-65 = 65ns
-70 = 70ns
-80 = 80ns
-85 = 85ns

ALABAMA

Representative

Electronic Sales Incorporated
303 Williams Avenue
Suite 422
Huntsville, AL 35801
Phone - 205-533-1735
TWX - 810-726-2107
FAX - 205-534-4404

Distributors

Hall-Mark Electronics Corporation #07
4900 Bradford Drive
Huntsville, AL 35807
Phone - 205-837-8700
TWX - 810-726-2187

Pioneer Technology
4825 University Square
Huntsville, AL 35816
Phone - 205-837-9300
TWX - 810-726-2197
FAX - 205-837-9358

ARIZONA

Representative

Quatra Electronic Sales Incorporated
4645 South Lakeshore Drive
Tempe, AZ 85282
Phone 602-820-7050
FAX 602-820-7054

Distributors

Anthem Electronics Incorporated
1727 East Weber Drive
Tempe, AZ 85281
Phone - 602-966-6600
TWX - 910-950-0110
FAX - 602-966-4826

Hall-Mark Electronics Corporation
4937 S. 36th Place
Phoenix, AZ 85040
Phone - 602-437-1200
FAX - 602-437-2348

Wyle Laboratories
17855 North Black Canyon Highway
Phoenix, AZ 85623
Phone - 602-866-2888
TWX - 371-2871
FAX - 602-866-6957

ARKANSAS

Representative

Nova Marketing Incorporated
7955 East 50th Street
Suite 1339
Tulsa, OK 74145
Phone - 918-660-5105

Distributors

Hall-Mark Electronics Corporation
11420 Pagemill Road
Dallas, TX 75243
Phone - 214-553-4300
TWX - 910-860-5577
FAX - 214-343-5988

Pioneer Electronics
13710 Omega Road
Dallas, TX 75234
Phone - 214-386-7300
TWX - 910-860-5563
FAX - 214-490-6419

Wyle Laboratories
1810 N. Greenville Avenue
Richardson, TX 75083
Phone - 214- 235-9953
FAX - 214-644-5064

CALIFORNIA

Representatives

C-K Associates
8333 Clairemont Mesa Boulevard
Suite 102
San Diego, CA 92111
Phone - 619-279-0420
TWX - 910-335-2009
FAX - 619-279-7650

Jones & McGeoy Sales Incorporated
801 Parkcenter Drive
Suite 250
Santa Ana, CA 92705
Phone - 714-547-6466
TWX - 510-601-4878
Telex - 989057
FAX - 714-547-7670

Jones & McGeoy Sales Incorporated
15350 Sherman Way
Van Nuys, CA 91406
Phone - 818-994-6500
FAX - 818-994-8929

Distributors

Anthem Electronics Incorporated
1040 E. Brokaw Road
San Jose, CA 95131
Phone - 408-295-4200
FAX - 408-282-1542

Anthem Electronics Incorporated
20640 Bahama Street
Chatsworth, CA 91311
Phone - 818-700-1000
FAX - 818-709-7639

Anthem Electronics Incorporated
1 Old Field Drive
East Irvine, CA 92718
Phone - 714-768-4444
TWX - 910-595-1583
FAX - 714-480-4747

Anthem Electronics Incorporated
4700 Northgate Boulevard
Sacramento, CA 95834
Phone - 916-922-6800
FAX - 916-922-3439

Anthem Electronics Incorporated
9369 Carroll Park Drive
San Diego, CA 92121
Phone - 619-453-9005
FAX - 619-546-7893

Hall-Mark Electronics Corporation
6341 Auburn Boulevard
Suite D
Citrus Heights, CA 95610
Phone - 916-722-8600

Hall-Mark Electronics Corporation
3878 Ruffin Road
Unit 10A
San Diego, CA 92123
Phone - 619-268-1201

Hall-Mark Electronics Corporation
8130 Remmet Avenue
Canoga Park, CA 91304
Phone - 818-716-7300

Hall-Mark Electronics Corporation
1110 Ringwood Court
San Jose, CA 95131
Phone - 408-432-0900
TWX - 910-339-9505
FAX - 408-433-0745

Hall-Mark Electronics Corporation
19220 South Normandie Avenue
Torrance, CA 90502
Phone - 213-217-8400

Wyle Laboratories
124 Maryland Street
El Segundo, CA 90245
Phone - 213-322-8100

Wyle Laboratories
3000 Bowers Avenue
Santa Clara, CA 95051
Phone - 408-727-2500
TWX - 910-338-0296
FAX - 408-727-5896

Wyle Laboratories
17872 Cowan Avenue
Irvine, CA 92714
Phone - 714-863-9953
Telex - 714-371-9599
FAX - 714-863-0473

Wyle Laboratories
11151 Sun Center Drive
Rancho Cordova, CA 95670
Phone - 916-638-5282
TWX - 713719279
Telex - 3103719279
FAX - 916-638-1491

Wyle Laboratories
9625 Chesapeake Drive
San Diego, CA 92123
Phone - 619-565-9171
Telex - 3719592

Wyle Laboratories
26677 W. Agoura Road
Calabasas, CA 91302
Phone - 818-880-9000
Telex - 3103720232

CANADA

Representatives

Clark-Hurman Associates
37 George Street North
Suite 404
Brampton, Ontario
L6X1RS
Canada
Phone - 416-453-1118
Telex - 06988501
FAX 416-453-5609

Clark-Hurman Associates
66 Colonnade Road
Suite 205
Nepean, Canada
Canada
Phone - 613-727-5626
FAX - 613-727-1707

Distributor

Semad Electronic
85 Spy Court
Markham, Ontario
Canada L3R 424
Phone - 416-475-8500
FAX - 416-475-4158

COLORADO

Representative

Wescom Marketing
4851 Independence Street
Suite 159
Wheatridge, CO 80033
Phone - 303-422-8957
FAX - 303-422-9892

Distributors

Anthem Electronics Incorporated
373 Inverness Drive South
Englewood, CO 80112
Phone - 303-790-4500
FAX - 303-790-4532

Hall-Mark Electronics Corporation
6950 South Tucson Way
Englewood, CO 80112
Phone - 303-790-1662
TWX - 910-931-0472
FAX - 303-790-4991

Wyle Laboratories
451 E 124th Street
Thornton, CO 80241
Phone - 303-457-9953
Telex - 372-0529
FAX - 303-457-4831

CONNECTICUT

Representative

Advanced Tech Sales Incorporated
Park Place West,
Suite 102,
348 Park Street
North Reading, MA 01864
Phone - 617-664-0888
TWX - 510-100-9762
FAX - 617-664-5503

Distributors

Hall-Mark Electronics Corporation
33 Village Lane
Wallingford, CT 06492
Phone - 203-271-2844
FAX - 203-271-1704

Anthem Electronics
170 Research Parkway
Meriden, CT 06450
Phone - 203-237-2282

Pioneer Electronics
112 Main Street
Norwalk, CT 06851
Phone - 203-853-1515
TWX - 710-468-3373
FAX - 203-838-9901

DELAWARE

Representative

Omega Electronic Sales Incorporated
1 Fairway Plaza
Suite 108
Huntingdon Valley, PA 19006
Phone - 215-947-4135
TWX - 510-665-5485
FAX - 215-938-1984

Distributor

Pioneer Technologies Incorporated
261 Gebralta Road
Horsham, PA 19044
Phone - 215-674-4000
TWX - 510-665-6778
FAX - 215-674-3107

DISTRICT OF COLUMBIA

Representative

Electronic Engineering & Sales, Inc.
235 Prince George Street
Annapolis, MD 21401
Phone - 301-269-4234
FAX - 301-269-6476
Mobile - 301-440-0818

Distributor

Pioneer Technologies Corporation
9100 Gaither Road
Gaithersburg, MD 20877
Phone - 301-921-0660
TWX - 710-828-0545
FAX - 301-921-4255

FLORIDA

Representatives

Delmac Sales Incorporated
2000 Tree Fork Lane
Suite 106
Longwood, FL 32750
Phone - 407-831-0040
FAX - 407-831-0025

Delmac Sales Incorporated
1701 W. Hillsboro Boulevard
Suite 304
Deerfield Beach, FL 33441
Phone - 305-427-7788
TWX - 510-956-3151
FAX - 305-427-7949

Delmac Sales Incorporated
1170 Woodlawn Street
Clearwater, FL 33516
Phone - 813-447-5192
TWX 510-100-5606
FAX - 813-447-2622

Distributors

Hall-Mark Electronics Corporation
15301 Roosevelt Boulevard
Suite 303
Clearwater, FL 33520
Phone - 813-530-4543
TWX - 810-863-0410
FAX - 813-535-3865

Hall-Mark Electronics Corporation
3161 Southwest 15th Street
Pompano Beach, FL 33069
Phone - 305-971-9280
TWX - 510-956-9720

Hall-Mark Electronics Corporation
7648 Southland Boulevard
Suite 100
Orlando, FL 32809
Phone - 407-855-4020
TWX - 810-850-0105

Pioneer Electronics
337 South-North Lake #1000
Altamonte Springs, FL 32701
Phone - 407-834-9090
TWX - 810-853-0284
FAX - 407-834-0865

Pioneer Electronics
674 S. Military Trail
Deerfield Beach, FL 33442
Phones - 305-428-8877
TWX - 510-955-9653
FAX - 305-481-2950

GEORGIA

Representative

Electronic Sales Incorporated
3103A Medlock Bridge Road
Norcross, Georgia 30071
Phone - 404-448-6554
TWX - 910-380-7192

Distributors

Hall-Mark Electornics Corporation
6410 Atlantic Boulevard
Suite 115
Norcross, GA 30071
Phone - 404-447-8000
TWX - 810-766-4510

Pioneer Technology
3100F Northwoods Place
Norcross, GA 30071
Phone - 404-448-1711
TWX - 810-766-4515
FAX - 404-446-8270

HAWAII

Representative

Anthem Electronics Incorporated
1040 E. Brokaw Road
San Jose, CA 95131
Phone - 408-295-4200
FAX - 408-282-1542

Distributors

Anthem Electronics Incorporated
1040 Brokaw Road
San Jose, CA 95131
Phone - 408-295-4200
FAX - 408-2822-1542

Hall-Mark Electronics Corporation
1110 Ringwood Court
San Jose, CA 95131
Phone - 408-432-0900
TWX - 910-339-9505
FAX - 408-433-0745

Wyle Laboratories
3000 Bowers Avenue
Santa Clara, CA 95051
Phone - 408-727-2500
TWX - 910-338-0296
FAX - 408-727-5896

IDAHO

Representative

Wescom Marketing
3501 South Main
Salt Lake City, Utah 84115
Phone - 801-269-0419
FAX - 801-269-0665

Distributor

Oakley Electronics
2801 West Idaho
Boise, Idaho 82702
Phone - 208-343-7937

ILLINOIS

Representatives

Hitec Central Incorporated
803 Choctaw
Independence, MO 64056
Phone - 816-796-6684
FAX - 816-796-6562

Oasis Sales Corporation
1101 Tonne Road
Elk Grove Village, IL 60007
Phone - 312-640-1850
TWX - 62578340
FAX - 312-640-9432

Distributors

Anthem Electronics Incorporated
180 Crossen Avenue
Elk Grove Village, IL 60007
Phone - 312-640-6066
FAX - 312-640-6302

Hall-Mark Electronics Corporation
210 Mittel Drive
Wooddale, IL 60191
Phone - 312-860-3800
FAX - 312-860-0239

Pioneer Electronics
2171 Executive Drive
Suite 200
Addison, IL 60101
Phone - 312-495-9680
FAX - 312-495-9831

INDIANA

Representative

Electronic Marketing Consultants Incorporated
4470 North College Avenue
Indianapolis, IN 46205
Phone - 317-921-3450
FAX - 317-921-3459
Telex - 62880527

Distributors

Hall-Mark Electronics Corporation
4275 W. 96th Street
Indianapolis, IN 46268
Phone - 317-872-8875

Pioneer Electronics
6408 Castle Place Drive
Indianapolis, IN 46250
Phone - 317-849-7300
TWX - 810-260-1794
FAX - 317-842-5998

IOWA

Representative

HITEC Central Incorporated
1644 26th Street N.W.
Cedar Rapids, IA 52405
Phone - 319-396-3228

Distributors

Anthem Electronics Incorporated
10025 Valley View Road
Suite 160
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3405

Hall-Mark Electronics Corporation
13750 Shoreline Drive
Earth City, MO 63045
Phone - 314-291-5350
TWX - 910-762-0672

Hall-Mark Electronics Corporation
210 Mittel Drive
Wooddale, IL 60191
Phone - 312-860-3800
FAX - 312-860-0239

Pioneer Electronics
7625 Golden Triangle Drive
Eden Prarie, MN 55344
Phone - 612-944-3355
TWX- 910-576-2737
FAX - 612-935-1921

KANSAS

Representative

HITEC Central Incorporated
803 Choctaw
Independence, MO 64056
Phone - 816-796-6684
FAX - 816-796-6562

Distributors

Hall-Mark Electronics Corporation
10809 Lakeview Avenue
Lenexa, KS 66215
Phone - 913-888-4747
TWX - 910-380-6767
FAX - 913 - 888-0532

Pioneer Electronics
10551 Lackman Road
Lenexa, KS 66215
Phone - 913-492-0500
TWX - 510-601-6411
FAX - 913-492-7832

KENTUCKY

Representative

Electronic Marketing Consultants Incorporated
4470 North College Avenue
Indianapolis, IN 46205
Phone - 317-921-3450
Telex - 62880527
FAX - 317-921-3459

Distributors

Hall-Mark Electronics Corporation
400 East Welson Bride Road
Suite S
Worthington, OH 43085
Phone - 614-888-3313
TWX - 810-339-2586
FAX - 614-888-0767

Pioneer Electronics
4433 Interpoint Boulevard
Dayton, OH 45424
Phone - 513-236-9900
TWX - 810-459-1622
FAX - 513-236-8133

LOUISIANA

Representative

Nova Marketing Incorporated
8350 Meadow Road Suite 174
Dallas, TX 75231
Phone - 214-750-6082
TWX - 910-861-9185
FAX - 214-750-6068

Distributors

Hall-Mark Electronics Corporation
11420 Pagemill Road
Dallas, TX 75243
Phone - 214-553-4300
TWX - 910-860-5577
FAX - 214-343-5988

Pioneer Electronics
13710 Omega Road
Dallas, TX 75234
Phone - 214-386-7300
TWX - 910-860-5563
FAX - 214-490-6419

Wyle Laboratories
1810 North Greenville Avenue
Richardson, TX 75083
Phone - 214-235-9953
FAX - 214-644-5064

MAINE

Representative

Advanced Technology Sales Incorporated
Park Place West,
Suite 102,
348 Park Street
North Reading, MA 01864
Phone - 617-664-0888
TWX - 510-100-9762
FAX - 617-664-5503

Distributors

Anthem Electronics
36 Jonspin Road
Wilmington, MA 01887
Phone - 617-657-5170
FAX - 617-657-6008

Hall-Mark Electronics Corporation
6 Cook Street
Billerica, MA 01821
Phone - 617-935-9777
TWX - 710-348-0617
FAX - 617-667-4129

Pioneer Electronics
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
TWX - 710-326-6617
FAX - 617-863-1547

MARYLAND

Representative

Electronic Engineering & Sales Inc.
235 Prince George Street
Annapolis, Maryland 21401
Phone - 301-269-4234
FAX - 301-269-6476
Mobile - 301-440-0818

Distributors

Anthem Electronics
9020A Menden Hall Court
Columbia, MD 21045
Phone - 301-381-0040

Hall-Mark Electronics Corporation
10240 Old Columbia Road
Columbia, MD 21046
Phone - 301-988-9800
TWX - 910-862-1907
FAX - 301-381-2036

Pioneer Technology Corporation
9100 Gaither Road
Gaithersburg, MD 20877
Phone - 301-921-0660
TWX - 710-828-0545
FAX - 301-921-4255

MASSACHUSETTS

Representative

Advanced Tech Sales Incorporated
Park Place West,
Suite 102,
348 Park Street
North Reading, ME 01864
Phone - 617-664-0888
TWX - 510-100-9762
FAX - 617-664-5503

Distributors

Anthem Electronics
36 Jonspin Road
Wilmington, MA 01887
Phone - 6117-657-5170
FAX - 617-657-6008

Hall-Mark Electronics Corporation
6 Cook Street
Billerica, MA 01821
Phone - 617-935-9777
TWX - 710-348-0617
FAX - 617-667-4129

Pioneer Electronics
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
TWX - 710-326-6617
FAX - 617-863-1547

MICHIGAN

Representatives

Rathsburg Associates Incorporated
17600 Northland Park Court
Suite 100
P.O. Box 5037
Southfield, MI 48086-5037
Phone - 313-559-9700
TWX - 810-243-4064
FAX - 313-559-1405

Rathsburg Associates Incorporated
2680 Horizon, S.E.
Grand Rapids, MI 49506
Phone - 616-949-7400
FAX - 616-949-1909

Distributors

Hall-Mark Electronics Corporation
38027 Schoolcraft Road
Livonia, MI 48150
Phone - 313-462-1205

Pioneer Electronics
4505 Broadmoor Avenue, S.E.
Grand Rapids, MI 46508
Phone - 616-698-1800
TWX - 510-600-1800
FAX - 616-698-1831

Pioneer Electronics
13485 Stanford
Livonia, MI 48150
Phone - 313-525-1800
TWX - 810-242-3271
FAX - 313-427 3720

MINNESOTA

Representative

HMR Incorporated
9065 Lyndale Avenue South
Minneapolis, MN 55420
Phone - 612-888-2122
TWX - 910-576-2755
FAX - 612-576-2755

Distributors

Anthem Electronics Incorporated
10025 Valley View Raod
Suite 160
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3405

Hall-Mark Electronics Corporation
10300 Valley View Road
Suite 101
Eden Prairie, MN 55344
Phone - 612-941-2600
FAX - 612-941-5778

Pioneer Electronics
7625 Golden Triangle Drive
Eden Prairie, MN 55344
Phone - 612-944-3355
TWX - 910-576-2737
FAX - 612-935-1921

MISSISSIPPI

Representative

Electronic Sales Incorporated
303 Williams Avenue,
Suite 422,
Huntsville, AL 35801
Phone - 205-533-1735
TWX - 810-726-2107
FAX - 205-534-4404

Distributor

Hall-Mark Electronics Corporation
4900 Bradford Drive
Huntsville, AL 35807
Phone - 205-837-8700
TWX - 810-726-2187

MISSOURI

Representatives

HITEC Central Incorporated
2282 Goldfinch
Florissant, MO 63031
Phone - 314-831-9377
FAX - 314-838-1148

HITEC Central Incorporated
803 Choctaw
Independence, MO 64056
Phone - 816-796-6684
FAX - 816-796-6562

Distributors

Hall-Mark Electronics Corporation
13750 Shoreline Drive
Earth City, MO 63045
Phone - 314-291-5350
TWX - 910-762-0672

Pioneer Electronics
655 Craig Road
St Louis, MO 63141
Phone - 314-432-4350

MONTANA

Distributors

Almac Electronics
E 10905 Montgomery
Spokane, WA 99206
Phone - 509-924-9500
1-800-325-6545

Oakley Electronics
2801 West Idaho
Boise, ID 83702
Phone - 208-343-7937

NEBRASKA

Representative

Wescom Marketing
4851 Independence Street
Suite 159
Wheatridge, CO 80033
Phone - 303-422-8957
FAX - 303-422-9892

Distributors

Hall-Mark Electronics Corporation
6950 South Tucson Way
Englewood, CO 80112
Phone - 303-790-1662
TWX - 910-931-0472
FAX - 303-790-4991

Wyle Laboratories
451 E 124th Street
Thornton, CO 80241
Phone - 303-457-9953
TWX - 372-0529
FAX - 303-457-4831

NEVADA

Distributors

Anthem Electronics Incorporated
4700 Northgate Boulevard
Sacramento, CA 95834
Phone - 916-922-6800
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Hall-Mark Electronics Corporation
6341 Auburn Boulevard
Suite D
Citrus Heights, CA 95610
Phone - 916-922-8600

Wyle Laboratories
11151 Sun Center Drive
Rancho Cordova, CA 95670
Phone - 916-638-5282
TWX - 713719279
Telex - 3103719279
FAX - 916-638-1491

NEW HAMPSHIRE

Representative

Advanced Technology Sales Incorporated
Park Place West,
Suite 102,
348 Park Street
North Reading, MA 01864
Phone - 617-664-0888
TWX - 510-100-9762
FAX - 617-664-5503

Distributors

Hall-Mark Electronics Corporation
6 Cook Street
Billerica, MA 01821
Phone - 617-935-9777
TWX - 710-348-0617
FAX - 617-667-4129

Anthem Electronics
36 Jonspin Road
Wilmington, MA 01887
Phone - 617-657-5170
FAX - 617-657-6008

Pioneer Electronics
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
TWX - 710-326-6617
FAX - 617-863-1547

NEW JERSEY

Representative

Omega Electronics Sales Incorporated
1 Fairway Plaza
Suite 108
Huntingdon Valley, PA 19006
Phone - 215-947-4135
TWX - 510-665-5485
FAX - 215-938-1984

Distributors

Anthem Electronics
311 Rt 46 West
Fairfield, NJ 07006
Phone - 210-227-7960

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107 Fairfield Road
Fairfield, NJ 07006
Phone - 201-575-4415
TWX - 710-734-4409

Hall-Mark Electronics Corporation
11000 Midlantic Drive
Mt. Laurel, NJ 08054
Phone - 609-235-1900
TWX - 710-940-0660

Hall-Mark Electronics Corporation
10 Old Bloomfield Avenue
Pinebrook, NJ 07058
Phone - 201-882-9773

Pioneer Electronics
45 Route 46
Pinebrook, NJ 07058
Phone - 201-575-3510
TWX - 710-734-4382
FAX - 201-575-3454

NEW MEXICO

Representative

Quatra Associates Incorporated
9704 Admiral Dewey Northeast
Albuquerque, NM 87111
Phone - 505-821-1455

Emtec Sales Incorporated
299 Ridgedale Avenue
East Hanover, N.J. 07936
Phone - 201-428-0600
TWX - 710-994
FAX - 201-428-9594

Distributors

Anthem Electronics Inc.
1727 East Weber Drive
Tempe, AZ 85281
Phone - 602-966-6600
TWX - 910-950-0110
FAX - 602-966-4826

Hall-Mark Electronics Corporation
4937 South 36th Place
Phoenix, AZ 85040
Phone - 602-437-1200
FAX - 602-437-2348

Wyle Laboratories
17855 North Black Canyon Highway
Phoenix, AZ 85023
Phone - 602-866-2888
Telex - 3712871
FAX - 602-866-6937

NEW YORK

Representatives

Emtec Sales Incorporated
299 Ridgedale Avenue
East Hanover, NJ 07936
Phone - 201-428-0600
TWX - 710-994-4867
FAX - 201-428-9594

Gen-Tech Electronics
4855 Executive Drive
Liverpool, NY 13088
Phone - 315-451-3480
TWX - 710-545-0250
FAX - 315-451-0988

Gen -Tech Electronics
41 Burning Tree Lane
Penfield, NY 14526
Phone - 716-381-5159

Gen-Tech Electronics
70 Sandoris Circle
Rochester, NY 14622
Phone - 716-467-5016

Gen-Tech Electronics
5 Arbutus Lane
MR 97 Binghamton, NY 13901
Phone - 607-648-8833

Distributors

Anthem Electronics
400 Oser Avenue
Hauppaugen N.Y. 11787
Phone - 516-273-1660

Hall-Mark Electronics Corporation
101 Comac Street
Ronkonkoma, NY 11779
Phone - 516-737-0600
TWX - 516-222-0162

Hall-Mark Electronics Corporation
-80 Rockwood Place
Rochester, NY 14610
Phone - 716-244-9290

Pioneer Electronics
68 Corporate Dirve
Binghamton, NY 13904
Phone - 607-722-9300
TWX - 510-252-0893
FAX - 607-722-9562

Pioneer Electronics
840 Fairport Park
Fairport, NY 14450
Phone - 716-381-7070
TWX - 510-253-7001
FAX - 716-381-5955

Pioneer Electronics
60 Crossways Park West
Woodbury, NY 11797
Phone - 516-921-8700
TWX - 510-221-2184
FAX - 516-921-2143

NORTH CAROLINA

Representatives

Electronic Sales Incorporated
315 N. Academy,
Suite 206,
Cary, NC 27511
Phone - 919-467-8486
TWX - 881605
FAX - 919-469-4286

Electronic Sales Incorporated
441 E. Arrowood Road
Apartment E2
Charlotte, NC 28217
Phone - 704-522-8428
FAX - 704-522-8419

Distributors

Hall-Mark Electronics Corporation
5237 North Boulevard
Raleigh, NC 27604
Phone - 919-872-0712
TWX - 510-928-1831

Pioneer Technology
9801A Southern Pine Boulevard
Charlotte, NC 28210
Phone - 704-527-8188
TWX - 810-621-0366
FAX - 704-522-8564

Pioneer Electronics
2810 Meridian Parkway
#148
Durham, NC 27713
Phone - 919-544-5400

NORTH DAKOTA

Representative

HMR Incorporated
9065 Lyndale Avenue South
MInneapolis, MN 55420
Phone - 612-888-2722
TWX - 910-576-2755
FAX - 612-884-4768

Distributors

Anthem Electronics Incorporated
10025 Valley View Road
Suite 160
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3405

Hall-Mark Electronics Corporation
10300 Valley View Road
Suite 101
Eden Prairie, MN 55344
Phone - 612-941-2600
FAX - 612-941-5778

Pioneer Electronics
7625 Golden Triangle Drive
Eden Prairie, MN 55344
Phone - 612-944-3355
TWX - 910-576-2737
FAX - 612-955-1921

OHIO

Representatives

Rathsburg Associates
P.O. Box 652
13965 Chillicothe
Chesterland, OH 44026
Phone - 216-338-8899
FAX - 216-729-6435

Rathsburg Associates
4433 Interpoint Boulevard
Dayton, OH 45424
Phone - 513-236-9900
FAX - 513-236-8133

Distributors

Hall-Mark Electronics Corporation
5821 Harper Road
Solon, OH 44139
Phone - 216-349-4632
FAX - 216-248-4803

Hall-Mark Electronics Corporation
400 E. Welson Bridge Road
Suite S
Worthington, OH 43085
Phone - 614-888-3313
TWX - 810-339-2586
FAX - 614-888-0767

Pioneer Electronics
4800 E 131st Street
Cleveland, OH 44105
Phone - 216-587-3600
TWX - 810-421-0011
FAX - 216-663-1004

Pioneer Electronics
4433 Interpoint Boulevard
Dayton, OH 45424
Phone - 513-236-9900
TWX - 810-459-1622
FAX - 513-236-8133

Pioneer Electronics
5400 Naiman Parkway
Solon, OH 44139
Phone - 216-349-1300

OKLAHOMA

Representative

Nova Marketing Incorporated
7955 East 50th Street
Suite 1339
Tulsa, OK 74145
Phone - 918-660-5105

Distributor

Hall-Mark Electronics Corporation
2510 N. Hemlock Lane
Broken Arrow, OK 74012
Phone - 918-251-1108

OREGON

Representative

Northwest Marketing Associates
6975 SW Sandburg Road
Suite 330
Portland, OR 97223
Phone - 503-620-0441
TWX - 910-464-5157
FAX - 503-684-2451

Distributors

Almac Electronics
1885 N.W. 169th Place
Beaverton, OR 97006
Phone - 503-629-8090
FAX - 503-645-0611

Anthem Electronics Incorporated
9705 SW Sunshine Ct
#900
Beaverton, OR 97005
Phone - 503-643-1114
FAX - 503-626-7928

Wyle Laboratories
5289 N.E. Elam Young Parkway
Bldg. E100
Hillsboro, OR 97123
Phone - 503-640-6000
TWX - 371-0379
FAX - 503-640-5846

PENNSYLVANIA

Representatives

(Western Pennsylvania)
Rathsburg & Associates
4433 Interpoint Boulevard
Dayton, OH 45424
Phone - 513-236-9900
FAX - 513-236-8133

(Eastern Pennsylvania)
Omega Electronic Sales Incorporated
1 Fairway Plaza
Suite 108
Huntingdon Valley, PA 19006
Phone - 215-947-4135
TWX - 510-665-5485
FAX - 215-938-1984

Distributors

Anthem Electronics
101 Rock Road
Horsham, PA 19044
Phone - 215-443-5150

Hall-Mark Electronics Corporation
11000 Midlantic Drive
Mt. Laurel, NJ 08054
Phone - 609-235-1900
TWX - 710-940-0660

Pioneer Technology
261 Gibraltar Road
Horsham, PA 19044
Phone - 215-674-4000
TWX - 510-665-6778
FAX - 215-674-3107

Pioneer Electronics
259 Kappa Drive
Pittsburgh, PA 15238
Phone - 412-782-2300
TWX - 710-795-3122
FAX - 412-963-8255

RHODE ISLAND

Representative

Advanced Technology Sales Incorporated
Park Place West,
Suite 102
348 Park Street
North Reading, MA 01864
Phone - 617-664-0888
TWX - 510-100-9726
FAX - 617-664-5503

Distributors

Anthem Electronics
170 Research Parkway
Meriden, CT 06450
Phone - 203-237-2282

Hall-Mark Electronics Corporation
33 Village Lane
Wallingford, CT 06492
Phone - 203-271-2844
FAX - 203-271-1704

Pioneer Electronics
112 Main Street
Norwalk, CT 06851
Phone - 203-853-1515
TWX - 710-468-3373
FAX - 203-838-9901

SOUTH CAROLINA

Representative

Electronic Sales Incorporated
441 E. Arrowhead Road
Apartment E2
Charlotte, NC 28217
Phone - 704-522-8428
FAX - 704-522-8419

Distributor

Pioneer Technology
9801A Southern Pine Boulevard
Charlotte, NC 28210
Phone - 704-527-8188
TWX - 810-621-0366
FAX - 704-522-8564

SOUTH DAKOTA

Representative

HMR Incorporated
9065 Lyndale Avenue South
Minneapolis, MN 55420
Phone - 612-888-2122
TWX - 910-576-2755
FAX - 612-884-4768

Distributors

Anthem Electronics Incorporated
10025 Valley View Road
Suite 160
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3405

Hall-Mark Electronics Corporation
10300 Valley View Road
Suite 101
Eden Prairie, MN 55344
Phone - 612-941-2600
FAX - 612-941-5778

Pioneer Electronics
7625 Golden Triangle Drive
Eden Prairie, MN 55344
Phone - 612-944-3355
TWX - 910-576-2737
FAX - 612-935-1921

TENNESSEE

Representative

Electronic Sales Incorporated
303 Williams Avenue
Suite 422
Huntsville, AL 35801
Phone - 205-533-1735
TWX - 810-726-2107
FAX - 205-534-4404

Distributors

Hall-Mark Electronics Corporation
4900 Bradford Drive
Huntsville, AL 35807
Phone - 205-837-8700
TWX - 810-726-2187

Pioneer Technology
4825 University Square
Huntsville, AL 35816
Phone - 205-837-9300
TWX - 810-726-2197
FAX - 205-837-9358

TEXAS

Representatives

Nova Marketing Incorporated
8350 Meadow Road
Suite 174
Dallas, TX 75231
Phone - 214-750-6082
TWX - 910-861-9185
FAX - 214-750-6068

Nova Marketing Incorporated
9207 Country Creek
#150
Houston, TX 77036
Phone - 713-988-6082
FAX - 713-774-1014

Nova Marketing Incorporated
Stillhouse Canyon Office Park
4807 Spicewood Springs Road
Building 3, Suite 3140
Austin, TX 78759
Phone - 512-343-2321
FAX - 512-343-2487

Quatra Associates Incorporated
9704 Admiral Dewey NE
Albuquerque, NM 87111
Phone - 505-821-1455

Distributors

Anthem Electronics
651 North Plan Road
Suite 429
Richardson, TX 75081
Phone - 214-238-7100
FAX - 214-238-0237

Hall-Mark Electronics Corporation
11333 Pagemill Road
P.O. Box 660091
Dallas, TX 75266
Phone - 214-343-5000
FAX - 214-343-5988

Hall-Mark Electronics Corporation
12211 Technology Boulevard
Austin, TX 78727
Phone - 512-258-8848
TWX - 910-874-2031
FAX - 512-258-3777

Hall-Mark Electronics Corporation
11420 Pagemill Road
Dallas, TX 75243
Phone - 214-553-4300
TWX - 910-860-5577
FAX - 214-343-5988

Hall-Mark Electronics Corporation
8000 Westglen
Houston, TX 77063
Phone - 713-781-6100
TWX - 910-881-2711

Wyle Laboratories
2120-F West Braker Lane
Austin, TX 78758
Phone - 512-834-9957
FAX - 512-834-0981

Wyle Laboratories
1810 N. Greenville Avenue
Richardson, TX 75083
Phone - 214-235-9953
FAX - 214-644-5064

Wyle Laboratories
1101 S. Wilcrest,
Suite 105
Houston, TX 77099
Phone - 713-879-9953
FAX - 713-879-6540

UTAH

Representative

Wescom Marketing
3501 S. Main
Salt Lake City, UT 84115
Phone - 801-269-0419
FAX - 801-269-0665

Distributors

Anthem Electronics Incorporated
1279 West 2200 South
Salt Lake City, UT 84119
Phone - 801-973-8555
FAX - 801-973-8909

Hall-Mark Electronics Corporation
2265 South 1300 West
West Valley City, UT 84119
Phone - 801-972-1008

Wyle Laboratories
1325 West 2200 South
West Valley City, UT 84119
Phone - 801-974-9953
TWX - 310-371-0506
Telex - 713-710-506
FAX - 801-972-2524

VERMONT

Representative

Advanced Technology Sales Incorporated
Park Place West,
Suite 1-2
348 Park Street
North Reading, MA 01864
Phone - 617-664-0888
TWX - 510-100-9762
FAX - 617-664-5503

Distributors

Anthem Electronics
36 Jonspin Road
Wilmington, MA 01887
Phone - 617-657-5170
FAX - 617-657-6008

Hall-Mark Electronic Corporation
6 Cook Street
Billerica, MA 01821
Phone - 617-935-9777
TWX - 710-348-0617
FAX - 617-667-4129

Pioneer Electronics
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
TWX - 710-326-6617
FAX - 617-863-1547

VIRGINIA

Representative

Electronic Enginnering & Sales Incorporated
235 Prince George Street
Annapolis, MD 21401
Phone - 301-269-4234
FAX - 301-269-6476
Mobile - 301-440-0818

Distributors

Anthem Electronics
9020A Menden Hall Court
Columbia, MD 21045
Phone - 301-381-0040

Hall-Mark Electronics Corporation
10240 Old Columbia Road
Columbia, MD 21046
Phone - 301-988-9800
TWX - 910-862-1907
FAX - 301-381-2036

Pioneer Technology Corporation
9100 Gaither Road
Gaithersburg, MD 20877
Phone - 301-921-0660
TWX - 710-828-8545
FAX - 301-921-4255

WASHINGTON

Representative

Northwest Marketing Associates
12835 Bellevue-Redmond Road
Suite 330N
Bellevue, WA 98005
Phone - 206-455-5846
TWX - 910-443-2445
FAX - 206-452-1130

Distributors

Almac Electronics
14360 Southeast Eastgate West
Bellevue, WA 98007
Phone - 206-643-9992
FAX - 206-643-9709

Almac Electronics
East 10905 Montgomery
Spokane, WA 99026
Phone - 509-924-9500
1-800-325-6545

Anthem Electronics Incorporated
5020 148th Avenue N.E.
Redmond, WA 98052
Phone - 206-881-0850
Telex - 910-997-0118
FAX - 206-885-4041

Wyle Laboratories
1750 132nd Avenue, N.E.
Bellevue, WA 98005
Phone - 206-453-8300
TWX - 310-372-42600
Telex - 713724260
FAX - 206-453-0071

WEST VIRGINIA

Representative

Rathsburg & Associates
4433 Interpoint Boulevard
Dayton, OH 45424
Phone - 513-236-9900
FAX - 513-236-8133

Distributor

Hall-Mark Electronics Corporation
400 E Welson Bridge Road
Suite S
Worthington, OH 43085
Phone - 614-888-3313
TWX - 810-339-2586
FAX - 614-888-0767

WISCONSIN

Representative

HMR Incorporated
9065 Lyndale Avenue South
Minneapolis, MN 55420
Phone - 612-888-2122
TWX - 910-576-2755
FAX - 612-884-4768

Oasis Sales Corporation
1305 North Barker Road
Brookfield, WI 53005
Phone - 414-782-6660
TWX - 62951740
FAX - 414-782-7921

Distributor

Hall-Mark Electronics Corporation
16255 West Lincoln Avenue
New Berlin, Wisconsin 53151
Phone - 414-797-7844

WYOMING

Representative

Wescom Marketing
3501 South Main
Salt Lake City, UT 84115
Phone - 801-269-0419
FAX - 801-269-0665

Distributors

Anthem Electronics Incorporated
1279 West 2200 South
Salt Lake City, UT 84119
Phone - 801-973-8555
FAX - 801-973-8909

Hall-Mark Electronics Corporation
2265 South 1300 West
West Valley City, UT 84119
Phone - 801-972-1008

Wyle Laboratories
1325 West 2200 South
West Valley City, UT 84119
Phone - 801-974-9953
TWX - 310-371-0506
Telex - 713-710-506
FAX - 801-972-2524

ARGENTINA

Distributor

Systar - Startsis S.A.
Avenue Pte. Roue Saenz
Rena 720 - Riso 7
1035 Buenos Aires
Argentina
Phone - 1-71-8763

AUSTRALIA

Representative

Reptechnic Pte. Ltd.
Suite #5
130-134 Pacific Highway
St. Leonards NSW 2065
Australia
Phone - 02-436-3422
FAX - 02-436-3764

Distributor

N.S.D. Australia
205 Middleborough Road
Box Hill 3128
Victoria
Australia
Phone - 3-890-0900
FAX - 3-899-0819

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Distributor

MCA - Tronix SPRL
Parc Industriel
de Recherches
Du Sart Tilman
Avenue Des Noisetiers
B4900 Angleur
Belgium
Phone - 041-674208
Telex - 42052
FAX - 41-67-6331

DENMARK

Distributor

Henkel Electronic
Industriparken 4
4960 Holeby
Denmark
Phone - 03-906333
Telex - 43219
FAX - 3-906422

FINLAND

Distributor

Turion Oy
Granittitie 9
00710 Helsinki SF- Finland
Phone - 0-372144
Telex - 124388 Turio SF
Liusketie 3, Pihlajamaki
FAX - 0373558

FRANCE

Representative

Rep'Tronic, SA
11, Escalier des Ulis
91400 Orsay, France
Phone - 1-69288700
Telex - 610-969
FAX - 1-69281750

Distributors

A2M
6, Avenue Charles
De Gaulle
78150 Le Chesnay, Cedex
France
Phone - 1-39549113
Telex - 698-376
FAX - 1-9543061

RTF Diffusion
59-63 Rue Desnouettes
75015 Paris
France
Phone - 1-47460113
Telex - 260832
FAX - 142665814

ISRAEL

Representative/Distributor

Rapac Electronic, Ltd.
P.O. 18053
Tel Aviv, Israel 61180
Street address:
#7, Saloniki Street
Tel Aviv, Israel 61100
Phone - 3-477115
Telex - 342173
FAX - 3-493-272

ITALY

Distributor

Moxel S.r.L.
Via C Frova 34
20092 Cinisello Balsamo
(MI) Italy
Phone - 02-61290521
Telex - 352045
FAX - 261-72582

NEW ZEALAND

Distributor

IRH Components
80 Mokoia Road
Birkenhead, Aukland
New Zealand
Phone - 9-419-0514

NETHERLANDS

Distributor

Akam Electronics B.V.
Bleiswijkseweg 43
2712 PB Zoetermeer
The Netherlands
Phone - 079-443200
Telex - 33183 AKAMNL
FAX - 079-421734

NORWAY

Distributor

BIT Elektronikk AS
Postboks 36-Lier
3401 Lier
Norway
Phone - 03-847099
FAX - 03-845510

REPUBLIC OF KOREA

Representative

Eastern Electronics, Inc.
3rd Floor, Yoowha Building
995-16, Daechi-Ding,
Kangnam Ku
Seoul, Korea
Phone - 2-566-0511
FAX - 2-553-2998

SINGAPORE, PHILLIPINES & INDONESIA

Representative

Desner Electronics
(FE) Ltd.
190 Middle Road
16-07 Fortune Centre
Singapore, 0718
Phone - 3373188
Telex - 39191
FAX - 3373180

SPAIN

Distributor

ATD Electronica, S.A.
Paza Cuidad de Veena, 6
28040 Madrid
Spain
Phone - 1-2344000
1-2344009
Telex - 42754
FAX - 1-234-7663

SWEDEN

Distributor

IE Komponenter AB
Box 11 113
S161 11
Stockholm, Sweden
Phone - 08-804685
FAX - 08-262286

SWITZERLAND

Representative

Micron Technology
Casa Fuchs CH-6984
Pura Switzerland
Phone - 1-9171-3785
FAX - 1-9171-3889

TAIWAN, R.O.C & HONG KONG

Representative

Kaltec International Ltd.
Rm 1204, Hanford House
221 Nathan Road
Kowloon, Hong Kong
Phone - 3-7391618
Telex - 51695
FAX - 3-7214570

UNITED KINGDOM

Representative

Micron Technology
European Office
Trafalgar House
Grenville Place
Mill Hill London
Phone - 01-959-3611
FAX - 01-959-6168

Representative/Distributor

Micro Call Ltd.
Thame Park Road
Thame, Oxon
OX93XD
United Kingdom
Phone - 084-421-5405
Telex - 0-837917
FAX - 084-421-7185

Distributor

Abacus Electronics PLC
Abacus House, Bone Lane
Newbury, Bukshire
RG14 55F
United Kingdom
Phone - 0635-30680
Telex - 847589
FAX - 0635-38670

WEST GERMANY

Distributor

A.S.P.
Leon Hardsweg 2
8025 Unterhaching
Munich, W. Germany
Phone - 49-89-61-10-80

MICRON
TECHNOLOGY, INC.

Micron Technology, Inc.
Marketing Department
2805 East Columbia Road
Boise, Idaho 83706
Telephone: (208) 386-3900
TWX: (910) 970-5973
FAX: (208) 343-2536