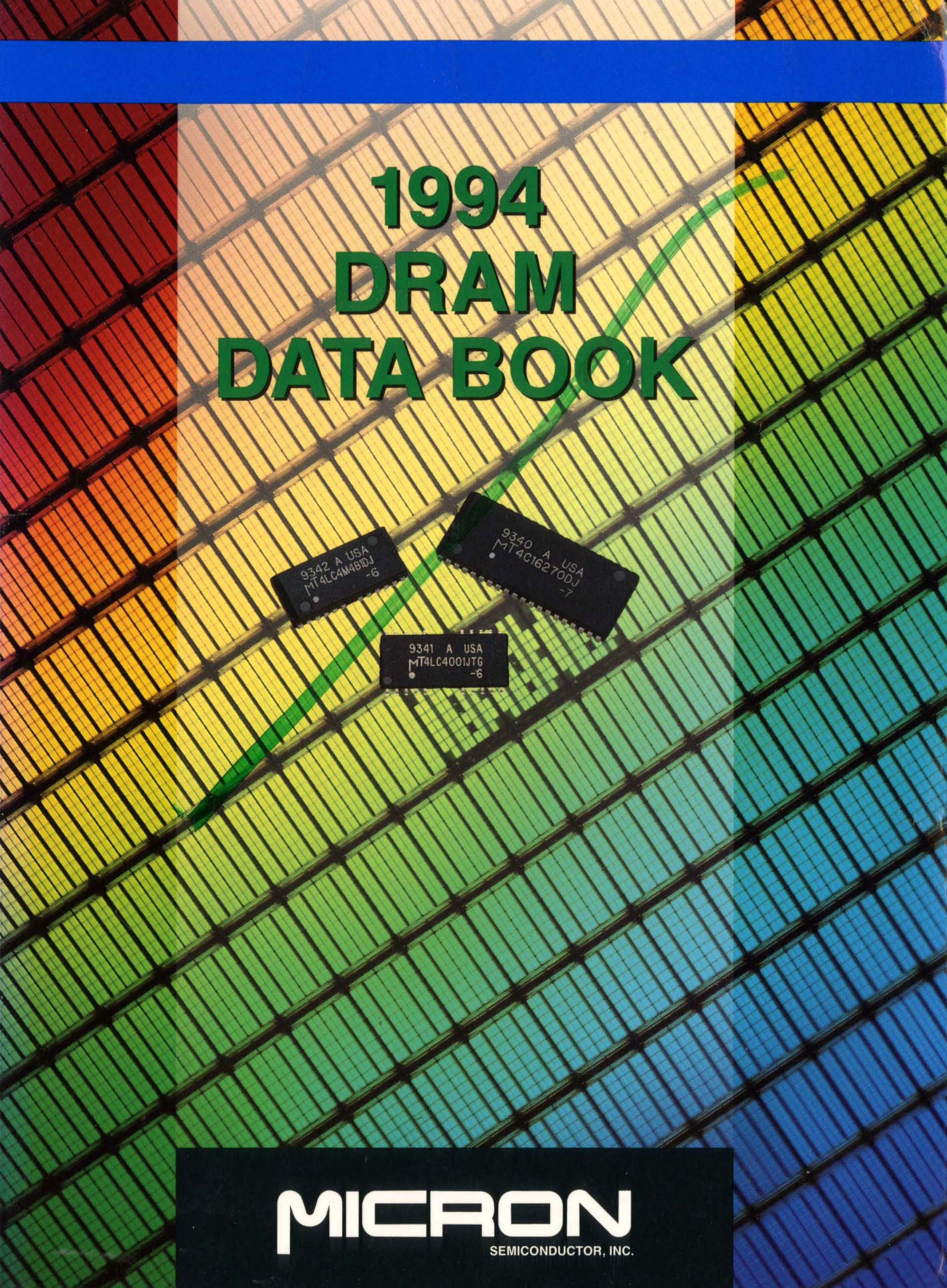
1994
DRAM
DATA BOOK
9342 A USA
MT4LC4M4B1DJ
-6
9340 A USA
MT4C16270DJ
-7
9341 A USA
MT4LC4001JTG
-6
MICRON
SEMICONDUCTOR, INC.

DRAM DATA BOOK

2805 East Columbia Road
Boise, Idaho 83706
Telephone: 208-368-3900
Fax: 208-368-4431
Micron DataFax℠: 208-368-5800
Customer Comment Line:
U.S.A. 800-932-4992
Intl. 01-208-368-3410
Fax 208-368-3342

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MICRON
SEMICONDUCTOR, INC.

DRAMs 1

SYNCHRONOUS DRAMs 2

DRAM MODULES 3

DRAM CARDS 4

TECHNICAL NOTES 5

PRODUCT RELIABILITY 6

PACKAGE INFORMATION 7

SALES INFORMATION 8

ABOUT THE COVER:

Front — Micron's DRAM products, shown here atop a 4 Meg DRAM wafer, offer a variety of features and advantages. Pictured are Micron's 3.3-volt, 16 Meg DRAM SOJ; 4 Meg DRAM SOJ with Extended Data-Out; and 3.3-volt, 4 Meg DRAM TSOP.

Back — Micron's Boise, Idaho, headquarters.

IMPORTANT NOTICE

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A. LIFE SUPPORT DEVICES OR SYSTEMS ARE DEVICES OR SYSTEMS WHICH (1) ARE INTENDED FOR SURGICAL IMPLANT INTO THE BODY, OR (2) SUPPORT OR SUSTAIN LIFE AND WHOSE FAILURE TO PERFORM WHEN PROPERLY USED IN ACCORDANCE WITH INSTRUCTIONS FOR USE PROVIDED IN THE LABELING CAN BE REASONABLY EXPECTED TO RESULT IN A SIGNIFICANT INJURY TO THE USER.

B. CRITICAL COMPONENT IS ANY COMPONENT OF A LIFE SUPPORT DEVICE OR SYSTEM WHOSE FAILURE TO PERFORM CAN BE REASONABLY EXPECTED TO CAUSE THE FAILURE OF THE LIFE SUPPORT DEVICE OR SYSTEM OR TO AFFECT ITS SAFETY OR EFFECTIVENESS.

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Dear Customer:

Micron Semiconductor, Inc., is dedicated to the design, manufacture and marketing of high-quality, highly reliable memory components. Our corporate mission is:

"To be a world-class team developing advantages for our customers."

At Micron, we are investing time, talent and resources to bring you the finest DRAMs, SRAMs, VRAMs and other specialty memory products. We have developed a unique intelligent burn-in system, AMBYX®, which evaluates and reports the quality level of each and every component we produce.

We are dedicated to continuous improvement of all our products and services. This means continual reduction of electrical and mechanical defect levels. It also means the addition of new services such as "just-in-time" delivery and electronic data interchange programs. And when you have a design or application question, you can get the answers you need from one of Micron's applications engineers.

We're proud of our products, our progress and our performance. And we're pleased that you're choosing Micron as your memory supplier.

The Micron Team

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ADVANTAGES

Micron Semiconductor brings quality, productivity and innovation together to provide advantages for our customers. Our products feature some of the industry's fastest speeds and smallest die sizes. And we establish delivery standards based on customer expectations, including JIT programs, made possible by ever-increasing product reliability.

COMPONENT INTEGRATED CIRCUITS

Micron entered the memory market 14 years ago, first designing, then manufacturing dynamic random access memory (DRAM). From there, we developed high-performance fast static RAM (SRAM), multiport DRAM (VRAM and triple-port DRAM), and a variety of other memory products.

As we bring innovative memory solutions to our customers, we enjoy recognition for our achievements. Micron's Triple-Port DRAM was the first IC ever to incorporate a second, independent serial access port, allowing unparalleled flexibility in data manipulation. Micron's Triple-Port received the 1990 "Product of the Year" award from *Electronic Products* magazine.

SPECIALTY MEMORY PRODUCTS

Beyond our standard component memory, Micron is introducing many revolutionary products that we expect will follow the triple-port's tradition. From synchronous burst SRAMs to programmable products, Micron continues to forge ahead into new and exciting frontiers.

We are pleased to be first to market with our compact, easy-to-install 88-pin DRAM card. Ideal for laptop, notebook and other portable systems, Micron's DRAM Card offers both high density and low power within JEDEC and JEIDA specifications.*

DIE SALES

In addition to our durable packaging, Micron also provides memory devices in bare die form. These are increasingly in demand for use in highly specialized applications. Micron's bare die products are available both in 6" wafers and wafflepacks.

CUSTOM MANUFACTURING SERVICES

For total project management, Micron offers value-added services. These include both standard contract manufacturing services for system-level products including design, assembly, customer kitted assembly, comprehensive quality testing or shipping as well as complete turnkey services covering all phases of production. Our component and system-level manufacturing facilities are centrally located in Boise, Idaho, so the component products you need are readily available.

MICRON DATAFAX

When you can't afford to wait for critical product information or specifications, Micron offers a convenient solution available 24 hours a day, every day. Micron DataFax enables you to make automated requests for data sheets, product literature, and other information from your fax machine. Just dial 208-368-5800 from your fax machine and Micron DataFax will give you instructions on how to order documents, including an index of documents. Once your order is placed, Micron DataFax will process you order, faxing up to two documents per call to your fax machine.

QUALITY

Without a doubt, quality is the most important thing we provide to every Micron customer with each Micron shipment. That's because we believe that quality must be internalized consistently at each level of our company. We provide every Micron team member with the training and motivation needed to make Micron's quality philosophy a reality.

One way we have measurably improved both productivity and product quality is through our own quality improvement program formed by individuals throughout the company. Micron quality teams get together to address a wide range of issues within their areas. We consistently and regularly perform a company-wide self-assessment based on the Malcolm Baldrige National Quality Award criteria. We've also implemented statistical process controls to evaluate every facet of the memory design, fabrication, assembly and shipping process. And our AMBYX intelligent burn-in and test system** gives Micron a unique edge in product reliability.

These quality programs recently resulted in Micron becoming one of the first U.S. semiconductor manufacturers to receive ISO 9001 certification. ISO 9001 is the most comprehensive level of certification in the internationally recognized ISO family of specifications. The certification implies that Micron's systems for accepting orders, reviewing customers' specifications, manufacturing and testing products, and delivering those products to its customers are quality controlled and produce consistent results.

*See NOTE, page v.
**For more information on AMBYX, see Section 6.

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ABOUT THIS BOOK

CONTENT

The 1994 *DRAM Data Book* from Micron Semiconductor provides complete specifications on all standard DRAMs and DRAM modules as well as specialty and derivative products based on our DRAM production process.

The *DRAM Data Book* is one of three product data books Micron currently publishes. Its two companion volumes include our *SRAM Data Book* and the *Specialty DRAM Data Book*. As product lines continue to diversify, more data books will be released.

SECTION ORGANIZATION

Micron's 1994 *DRAM Data Book* contains a detailed Table of Contents with sequential and numerical indexes of products as well as a complete product selection guide. The *Data Book* is organized into nine sections:

- **Sections 1–4:** Individual product families. Each contains a product selection guide followed by data sheets.
- **Section 5:** Technical/application notes.
- **Section 6:** Summary of Micron's unique quality and reliability programs and testing operation, including our AMBYX intelligent burn-in and test system.*
- **Section 7:** Packaging information.
- **Section 8:** Sales information, including a list of sales representatives and distributors worldwide.

DATA SHEET SEQUENCE

Data sheets in this book are ordered first by width and second by depth. For example, the DRAM section begins with the 1 Meg x 1 followed by 4 Meg x 1 and all other x1 configurations in order of ascending depth. Next come the x4 products, followed by x8, etc., as applicable to the specific product family.

DATA SHEET DESIGNATIONS

As detailed in the table below, each Micron product data sheet is classified as either Advance, Preliminary or Final. In addition, new product data sheets that are new additions are designated with a "New" indicator in the tab area of each page.

SURVEY

We have included a removable, postage-paid survey form in the front of this book. Your time in completing and returning this survey will enhance our efforts to continually improve our product literature.

For more information on Micron product literature, or to order additional copies of this publication, contact

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U.S.A. 800-932-4992
Intl. 01-208-368-3410
Fax 208-368-3342

DATA SHEET DESIGNATIONS

DATA SHEET MARKING	DEFINITION
Advance	This data sheet contains initial descriptions of products still under development.
Preliminary	This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.
No Marking	This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.
New	This data sheet (which may be either Advance, Preliminary or Final) is a new addition to the data book.

NOTE: Micron's *DRAM Data Book* uses acronyms to refer to certain industry-standard-setting bodies. These are defined below:
EIA/JEDEC—Electronics Industry Association/Joint Electron Device Engineering Council
JEIDA—Japanese Electronics Industry Development Association
PCMCIA—Personal Computer Memory Card International Association

*Micron's *Quality/Reliability Handbook* is available by calling 208-368-3900.

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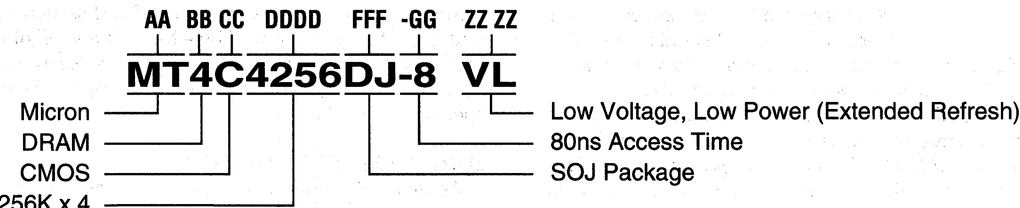
EXPANDED COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product	MT

BB – PRODUCT FAMILY

DRAM	4
DPDRAM (VRAM)	42
TPDRAM	43
SRAM	5
Synchronous SRAM	58

CC – PROCESS TECHNOLOGY

CMOS	C
Low Voltage CMOS	LC

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

DRAM	Width, Density
DPDRAM (VRAM)	Width, Density
TPDRAM	Width, Density
SRAM	Total Bits, Width
Synchronous SRAM	Density, Width

E – DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required.)

JEDEC Test Mode (4 Meg DRAM)	J
Errata on Base Part	Q

FFF – PACKAGE CODES

PLASTIC

DIP	Blank
DIP (Wide Body)	W
ZIP	Z
LCC	EJ
SOP/SOIC	SG
QFP	LG
TSOP (Type II)	TG
TSOP (Reversed)	RG
TSOP (Longer)	TL
SOJ	DJ
SOJ (Reversed)	DR
SOJ (Longer)	DL

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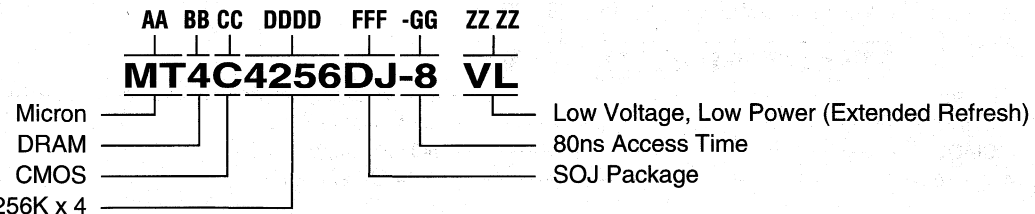
EXPANDED COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-50 (SRAM only)	50ns
-53	53ns
-55	55ns
-70 (SRAM only)	70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

Interim	I
Low Voltage	V

ZZ ZZ – PROCESSING CODES (continued)

DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh)	S
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

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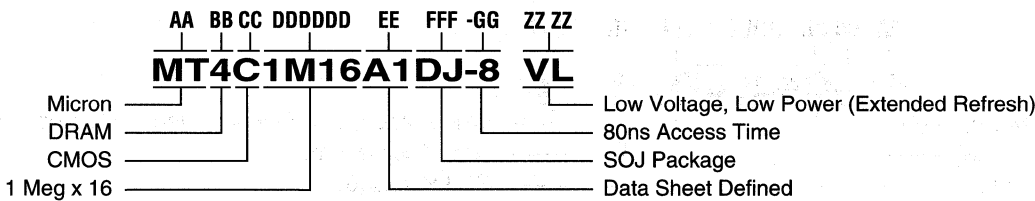
NEW COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product	MT

BB – PRODUCT FAMILY

DRAM	4
DPDRAM (VRAM)	42
TPDRAM	43
Synchronous DRAM	48
SRAM	5
Synchronous SRAM	58

CC – PROCESS TECHNOLOGY

CMOS	C
Low Voltage CMOS	LC
BiCMOS	B
Low Voltage BiCMOS	LB

DDDDDD – DEVICE NUMBER

Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter	Bits
K	Kilobits
M	Megabits
G	Gigabits

EE – DEVICE VERSIONS

(The first character is an alphabetic character only; the second character is a numeric character only.)
Specified by individual data sheet.

FFF – PACKAGE CODES

Plastic

DIP	Blank
DIP (Wide Body)	W
ZIP	Z
LCC	EJ
SOP/SOIC	SG
QFP	LG
TSOP (Type II)	TG
TSOP (Reversed)	RG
TSOP (Longer)	TL
SOJ	DJ
SOJ (Wide)	DW
SOJ (Reversed)	DR
SOJ (Longer)	DL

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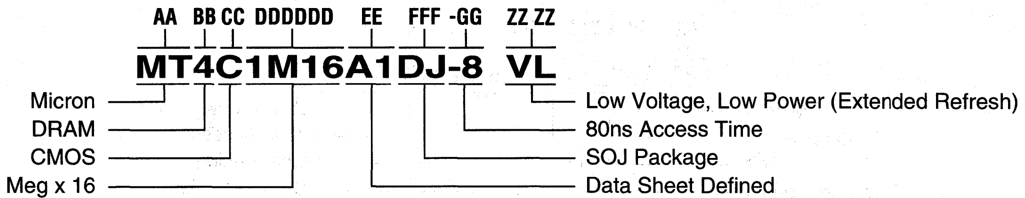
NEW COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-9	9ns or 90ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-53	53ns
-55	55ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

Interim	I
Low Voltage	V

ZZ ZZ – PROCESSING CODES (continued)

DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh)	S
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Volt Data Retention, Low Power	LP
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

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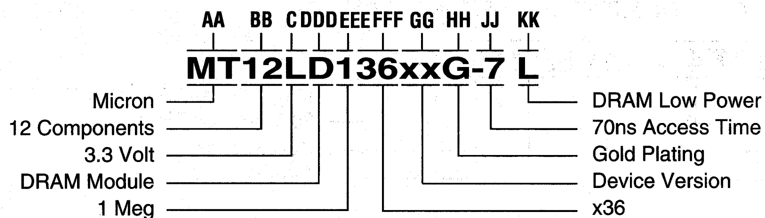
MODULE NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Semiconductor Product .... MT

BB – NUMBER OF MEMORY COMPONENTS

C – PROCESS TECHNOLOGY

LOW VOLTAGE (3.3V) L

DDD – RAM FAMILY

DRAM .... D
DRAM TSOP .... DT
SRAM .... S
SRAM TSOP .... ST
SYNCHRONOUS SRAM .... SY
SYNCHRONOUS SRAM TQFP .... SYT
VRAM V

EEE – DEPTH

FFF – WIDTH

GG – DEVICE VERSIONS

Specified by individual data sheet (Synchronous SRAM only)

HH – PACKAGE CODE

Gold Plated SIMM/DIMM .... G
ZIP .... Z
SIP .... N
SIMM/DIMM .... M
Small Outline DIMM .... H
Small Outline Gold DIMM .... HG
Double-Sided SIMM (1 or 4 Meg x 36 Only) .... DM
Double-Sided SIMM (Gold 1 or 4 Meg x 36 Only) .... DG

JJ – ACCESS TIME

-10 .... 10ns or 100ns
-12 .... 12ns
-15 .... 15ns
-17 .... 17ns
-20 .... 20ns
-25 .... 25ns
-35 .... 35ns
-6 .... 60ns
-7 .... 70ns
-8 .... 80ns

KK – MODULE SPECIAL DESIGNATOR

SRAM
- 2V data retention L
- Low Power .... P
- Low Power, 2V data retention .... LP

DRAM
- Low Power (Extended Refresh) L
- ECC C
- Extended Data Out X
- Self Refresh .... S
- 16 Meg DRAM 4,096 Refresh .... B

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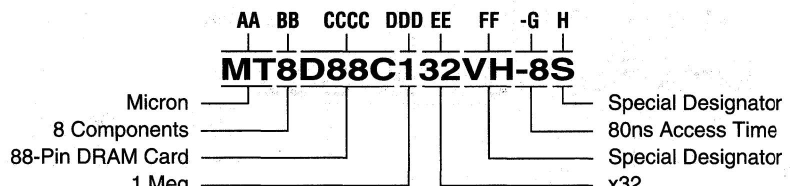
DRAM CARD NUMBERING SYSTEM



AA – Product Line Identifier
Micron Product .... MT

BB – NUMBER OF MEMORY COMPONENTS

CCCC – DRAM CARD DESIGNATOR AND PIN COUNT
88-Pin DRAM Card D88C

DDD – DEPTH

EE – WIDTH

FF – SPECIAL DESIGNATOR
3.3 Volts V
Reduced length (2") .... H

G – ACCESS TIME
-5 .... 50ns
-6 .... 60ns
-7 .... 70ns
-8 .... 80ns

H– SPECIAL DESIGNATOR
Self Refresh .... S

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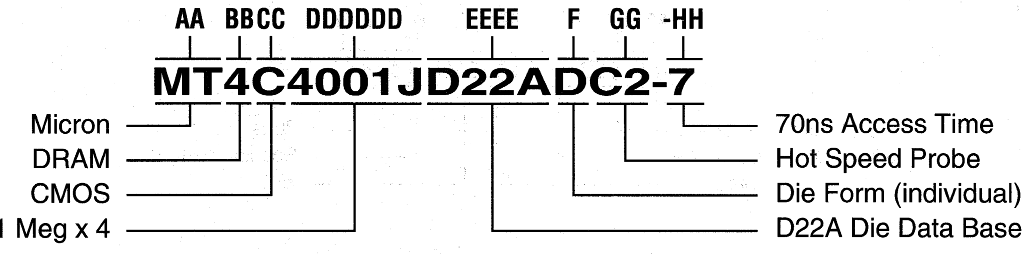
DIE PRODUCT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Component Product .... MT

BB – PRODUCT FAMILY

SRAM 5
DRAM 4
Synchronous SRAM 58
DPDRAM (VRAM) 42

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC

DDDDDD – DEVICE NUMBER

When no alpha character appears as part of this section, the section is defined as:

DRAM .... Width, Density
VRAM .... Width, Density
SRAM .... Total Bits, Width
Synchronous SRAM .... Depth, Width

When an alpha character occurs as part of this section, the section is defined as:
Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter .... Bits
K .... Kilobits
M .... Megabits
G .... Gigabits

EEEE – DIE DATA BASE REVISION

F – FORM

Die Form .... D
Wafer Form (6" Wafer) .... W

GG – TESTING LEVELS

Standard Probe (0° to 70°C) C1
Hot Speed Probe (0° to 70°C) C2
Known Good Die (0° to 70°C) C3

HH – ACCESS TIME

(Applicable for C2 and C3 only)

-5 .... 5ns or 50ns
-6 .... 6ns or 60ns
-7 .... 7ns or 70ns
-8 .... 8ns or 80ns
-9 .... 9ns or 90ns
-10 .... 10ns or 100ns
-12 .... 12ns or 120ns
-15 .... 15ns or 150ns
-17 .... 17ns
-20 .... 20ns
-25 .... 25ns
-35 .... 35ns
-45 .... 45ns
-50 (SRAM only) 50ns

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DRAMs

Part	Organization	Features	PAGE
MT4C1024	1 Meg x 1	FP	1-1
MT4C1024 L	1 Meg x 1	FP, LP	1-1
MT4C1026	1 Meg x 1	SC	1-13
MT4C1004J	4 Meg x 1	FP	1-25
MT4C1004J S	4 Meg x 1	FP, S	1-25
MT4C1006J	4 Meg x 1	SC	1-39
MT4C16M1A1	16 Meg x 1	FP, 4KR	1-51
MT4C4256	256K x 4	FP	1-63
MT4C4256 L	256K x 4	FP, LP	1-63
MT4C4258	256K x 4	SC	1-75
MT4C4001J	1 Meg x 4	FP	1-87
MT4C4001J S	1 Meg x 4	FP, S	1-87
MT4LC4001J	1 Meg x 4	FP, LV	1-103
MT4LC4001J S	1 Meg x 4	FP, LV, S	1-103
MT4C4003J	1 Meg x 4	SC	1-115
MT4LC4007J	1 Meg x 4	EDO, LV	1-127
MT4LC4007J S	1 Meg x 4	EDO, LV, S	1-127
MT4C4M4A1	4 Meg x 4	FP, 4KR	1-141
MT4C4M4B1	4 Meg x 4	FP, 2KR	1-141
MT4C4M4A1	4 Meg x 4	FP, 4KR	1-155
MT4C4M4B1	4 Meg x 4	FP, 2KR	1-155
MT4C4M4B1 S	4 Meg x 4	FP, 2KR, S	1-155
MT4LC4M4A1	4 Meg x 4	FP, 4KR, LV	1-169
MT4LC4M4B1	4 Meg x 4	FP, 2KR, LV	1-169
MT4LC4M4B1 S	4 Meg x 4	FP, 2KR, LV, S	1-169
MT4LC4M4E9	4 Meg x 4	EDO, LV	1-183
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MT4C8512	512K x 8	FP	1-197
MT4LC2M8B1	2 Meg x 8	FP, 2KR, LV	1-209
MT4LC2M8B1 S	2 Meg x 8	FP, 2KR, LV, S	1-209
MT4LC2M8E7	2 Meg x 8	EDO, 2KR, LV	1-221
MT4LC2M8E7 S	2 Meg x 8	EDO, 2KR, LV, S	1-221

Abbreviation	Meaning	Abbreviation	Meaning
FP	FAST PAGE MODE	**SC**	STATIC COLUMN
LP	Low Power, Extended Refresh	**WPB**	WRITE-PER-BIT
EDO	Extended Data-Out	**DW**	Dual WE
DC	Dual CAS	**2KR**	2,048 Refresh
4KR	4,096 Refresh	**S**	SELF REFRESH
ASY	Asymmetrical Addressing	**LV**	Low Voltage

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DRAMs (continued)

			PAGE
MT4C16256	256K x 16	FP, DW	1-223
MT4C16257	256K x 16	FP, DC	1-223
MT4LC16256	256K x 16		1-239
MT4LC16256 S	256K x 16	FP, DW, LP, S	1-239
MT4LC16257	256K x 16		1-239
MT4LC16257 S	256K x 16	FP, DC, LP, S	1-239
MT4C16270	256K x 16	EDO, DC	1-257
MT4LC16270	256K x 16		1-273
MT4C16260	256K x 16	FP, ASY, DW	1-289
MT4LC1M16C3	1 Meg x 16	FP, DC, LV	1-303
MT4LC1M16C3 S	1 Meg x 16	FP, DC, S, LP	1-303

FP	FAST PAGE MODE	**SC**	STATIC COLUMN
LP	Low Power, Extended Refresh	**WPB**	WRITE-PER-BIT
EDO	Extended Data-Out	**DW**	Dual WE
DC	Dual CAS	**2KR**	2,048 Refresh
4KR	4,096 Refresh	**S**	SELF REFRESH
ASY	Asymmetrical Addressing	**LV**	Low Voltage

SYNCHRONOUS DRAMs

		PAGE
MT48LC4M4R1	4 Meg x 4	2-1
MT48LC4M4R1 S	4 Meg x 4	2-1
MT48LC2M8S1	2 Meg x 8	2-3
MT48LC2M8S1 S	2 Meg x 8	2-3
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LP .... Low Power **LV** .... Low Voltage
S .... SELF REFRESH
NOTE: All modules include FAST PAGE MODE cycle.

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DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Typical Power Dissipation		Package and Number of Pins				Page
				Standby	Active	PDIP	ZIP	SOJ	TSOP	
1 Meg x 1	FP	MT4C1024	60, 70, 80	3mW	175mW	18	20	20/26	-	1-1
1 Meg x 1	FP, LP	MT4C1024 L	60, 70, 80	0.8mW	175mW	18	20	20/26	-	1-1
1 Meg x 1	SC	MT4C1026	70, 80, 100	3mW	175mW	18	20	20/26	-	1-13
4 Meg x 1	FP	MT4C1004J	60, 70, 80	3mW	225mW	-	20	20/26	20/26	1-25
4 Meg x 1	FP, S	MT4C1004J S	60, 70, 80	0.8mW	225mW	-	20	20/26	20/26	1-25
4 Meg x 1	SC	MT4C1006J	70, 80	3mW	225mW	-	20	20/26	-	1-39
16 Meg x 1	FP, 4KR	MT4C16M1A1	60, 70	4mW	200mW	-	-	24/26	-	1-51
256K x 4	FP	MT4C4256	60, 70, 80	3mW	175mW	20	20	20/26	-	1-63
256K x 4	FP, LP	MT4C4256 L	60, 70, 80	0.8mW	175mW	20	20	20/26	-	1-63
256K x 4	SC	MT4C4258	70, 80 ,100	3mW	175mW	20	20	20/26	-	1-75
1 Meg x 4	FP	MT4C4001J	60, 70, 80	3mW	225mW	-	20	20/26	20/26	1-87
1 Meg x 4	FP, S	MT4C4001J S	60, 70, 80	0.8mW	225mW	-	20	20/26	20/26	1-87
1 Meg x 4	FP, LV	MT4LC4001J	60, 70, 80	1.2mW	100mW	-	-	20/26	20/26	1-103
1 Meg x 4	FP, LV, S	MT4LC4001J S	60, 70, 80	250µW	100mW	-	-	20/26	20/26	1-103
1 Meg x 4	SC	MT4C4003J	70, 80	3mW	225mW	-	20	20/26	-	1-115
1 Meg x 4	EDO, LV	MT4LC4007J	60, 70, 80	1.2mW	100mW	-	-	20/26	20/26	1-127
1 Meg x 4	EDO, LV, S	MT4LC4007J S	60, 70, 80	250µW	100mW	-	-	20/26	20/26	1-127
4 Meg x 4	FP, 4KR	MT4C4M4A1	60, 70	3mW	200mW	-	-	24/28	-	1-141
4 Meg x 4	FP, 2KR	MT4C4M4B1	60, 70	3mW	275mW	-	-	24/28	-	1-141
4 Meg x 4	FP, 4KR	MT4C4M4A1	60, 70	3mW	225mW	-	-	24/26	24/26	1-155
4 Meg x 4	FP, 2KR	MT4C4M4B1	60, 70	3mW	275mW	-	-	24/26	24/26	1-155
4 Meg x 4	FP, 2KR, S	MT4C4M4B1 S	60, 70	1mW	275mW	-	-	24/26	24/26	1-155
4 Meg x 4	FP, 4KR, LV	MT4LC4M4A1	60, 70	1mW	150mW	-	-	24/26	24/26	1-169
4 Meg x 4	FP, 2KR, LV	MT4LC4M4B1	60, 70	1mW	180mW	-	-	24/26	24/26	1-169
4 Meg x 4	FP, 2KR, LV, S	MT4LC4M4B1 S	60, 70	0.4mW	180mW	-	-	24/26	24/26	1-169
4 Meg x 4	EDO, LV	MT4LC4M4E9	60, 70	1mW	150mW	-	-	24/26	24/26	1-183
4 Meg x 4	EDO, LV, S	MT4LC4M4E9 S	60, 70	0.4mW	150mW	-	-	24/26	24/26	1-183
512K x 8	FP	MT4C8512	60, 70, 80	3mW	250mW	-	-	28	-	1-197
2 Meg x 8	FP, 2KR, LV	MT4LC2M8B1	60, 70	1.2mW	200mW	-	-	28	28	1-209
2 Meg x 8	FP, 2KR, LV, S	MT4LC2M8B1 S	60, 70	1.2mW	200mW	-	-	28	28	1-209
2 Meg x 8	EDO, 2KR, LV	MT4LC2M8E7	60, 70	1.2mW	200mW	-	-	28	28	1-221
2 Meg x 8	EDO, 2KR, LV, S	MT4LC2M8E7 S	60, 70	1.2mW	200mW	-	-	28	28	1-221
256K x 16	FP, DW	MT4C16256	60, 70, 80	3mW	375mW	-	-	40	40/44	1-223
256K x 16	FP, DC	MT4C16257	60, 70, 80	3mW	375mW	-	-	40	40/44	1-223
256K x 16	FP, DW, LV	MT4LC16256	60, 70, 80	3mW	175mW	-	-	40	40/44	1-239
256K x 16	FP, DW, LV, S	MT4LC16256 S	60, 70, 80	0.3mW	175mW	-	-	40	40/44	1-239
256K x 16	FP, DC, LV	MT4LC16257	60, 70, 80	3mW	175mW	-	-	40	40/44	1-239
256K x 16	FP, DC, LV, S	MT4LC16257 S	60, 70, 80	0.3mW	175mW	-	-	40	40/44	1-239
256K x 16	EDO, DC	MT4C16270	60, 70, 80	3mW	375mW	-	-	40	40/44	1-257
256K x 16	EDO, DC, LV	MT4LC16270	60, 70, 80	0.3mW	165mW	-	-	40	40/44	1-273
256K x 16	FP, ASY, DW	MT4C16260	60, 70, 80	3mW	375mW	-	-	40	-	1-289
1 Meg x 16	FP, DC, LV	MT4LC1M16C3	60, 70, 80	3mW	225mW	-	-	42	44/50	1-303
1 Meg x 16	FP, DC, S, LV	MT4LC1M16C3 S	60, 70, 80	3mW	225mW	-	-	42	44/50	1-303

FP = FAST PAGE MODE, SC = STATIC COLUMN, LP = Low Power, Extended Refresh; WPB = WRITE-PER-BIT, EDO = Extended Data-Out, DW = Dual WE, DC = Dual CAS, 2KR = 2,048 Refresh, 4KR = 4,096 Refresh, S = SELF REFRESH, ASY = Asymmetrical Addressing, LV = Low Voltage

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SYNCHRONOUS DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package/# of Pins		
				Standby	Active	SOJ	TSOP	Page
4 Meg x 4	BURST	MT48LC4M4R1	10, 12, 13	3mW	200mW	-	44	2-1
4 Meg x 4	BURST	MT48LC4M4R1 S	10, 12, 13	3mW	200mW	-	44	2-1
2 Meg x 8	BURST	MT48LC2M8S1	10, 12, 13	3mW	200mW	-	44	2-3
2 Meg x 8	BURST	MT48LC2M8S1 S	10, 12, 13	3mW	200mW	-	44	2-3
2 Meg x 8	BURST	MT48LC2M8K3 S	10, 12, 13	2mW	200mW	32	44	2-5

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DRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Part Number	Optional Access Cycle	Access Time (ns)	Power Dissipation		Package		Page
				Standby	Active	SIMM	DIMM	
1 Meg x 8	MT2D18		60,70,80	6mW	450mW	30	-	3-1
4 Meg x 8	MT2D48		60,70	6mW	400mW	30	-	3-11
4 Meg x 8	MT8D48		60,70,80	24mW	1,800mW	30	-	3-21
1 Meg x 9	MT3D19		60,70,80	9mW	625mW	30	-	3-31
4 Meg x 9	MT3D49		60,70	9mW	575mW	30	-	3-41
4 Meg x 9	MT9D49		60,70,80	27mW	2,025mW	30	-	3-51
2 Meg x 16	MT8D132	LP	60,70,80	24mW	1,800mW	72	-	3-61
4 Meg x 16	MT16D(T)232	LP	60,70,80	48mW	1,824mW	72	-	3-87
8 Meg x 16	MT8D432		60,70	24mW	1,600mW	72	-	3-99
16 Meg x 16	MT16D832		60,70	48mW	1,624mW	72	-	3-137
2 Meg x 18	MT12D136	LP	60,70,80	36mW	2,500mW	72	-	3-149
4 Meg x 18	MT24D236	LP	60,70,80	72mW	2,536mW	72	-	3-161
8 Meg x 18	MT12D436		60,70	52mW	3,100mW	72	-	3-173
16 Meg x 18	MT24D836		60,70	72mW	2,536mW	72	-	3-197
1 Meg x 32	MT8D132	LP	60,70,80	24mW	1,800mW	72	-	3-61
1 Meg x 32	MT8LD132(S)	S, LV	60,70,80	1.6mW	1,440mW	72	-	3-73
2 Meg x 32	MT16D(T)232	LP	60,70,80	48mW	1,824mW	72	-	3-87
2 Meg x 32	MT16LD232(S)	S, LV	60,70,80	1.6mW	1,440mW	72	-	3-73
4 Meg x 32	MT8D432		60,70	24mW	1,600mW	72	-	3-99
4 Meg x 32	MT8LD432(S)	S, LV	60,70	8mW	1,440mW	72	-	3-111
4 Meg x 32	MT32D432	LP	60,70,80	96mW	7,200mW	72	-	3-125
8 Meg x 32	MT16LD832(S)	S, LV	60,70	16mW	1,440mW	72	-	3-111
8 Meg x 32	MT16D832		60,70	48mW	1,624mW	72	-	3-137
1 Meg x 36	MT12D136	LP	60,70,80	36mW	2,500mW	72	-	3-149
2 Meg x 36	MT24D236	LP	60,70,80	72mW	2,536mW	72	-	3-161
4 Meg x 36	MT12D436		60,70	36mW	2,500mW	72	-	3-173
4 Meg x 36	MT36D436	LP	60,70,80	108mW	8,100mW	72	-	3-185
8 Meg x 36	MT24D836		60,70	72mW	2,536mW	72	-	3-197
1 Meg x 40	MT10D140	LP	60,70,80	30mW	2,250mW	72	-	3-209
2 Meg x 40	MT20D240	LP	60,70,80	60mW	2,280mW	72	-	3-221
4 Meg x 40	MT10D440	LP	60,70	30mW	2,000mW	72	-	3-233
8 Meg x 40	MT20D840	LP	60,70	60mW	2,030mW	72	-	3-247
1 Meg x 64	MT16D(T)164	LP	60,70,80	48mW	3,600mW	-	168	3-261
1 Meg x 64	MT16LD(T)164(S)	S, LV	60,70,80	2mW	1,200mW	-	168	3-275
4 Meg x 64	MT16D(T)464		60,70	48mW	3,200mW	-	168	3-291
4 Meg x 64	MT16LD(T)464(S)	S, LV	60,70	16mW	2,400mW	-	168	3-305
4 Meg x 72	MT24D(T)472		60,70	56mW	5,000mW	-	168	3-321
4 Meg x 72	MT24LD(T)472(S)	S, LV	60,70	56mW	3,400mW	-	168	3-335

LP = Low Power, Extended Refresh; LV = Low Voltage; S = SELF REFRESH
NOTE: All modules include FAST PAGE MODE cycle.

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DRAM CARD PRODUCT SELECTION GUIDE

Memory Configuration		Part Number	Access Time (ns)	Number of Pins Card	Page
1 Meg x 32	4 Megabytes	MT8D88C132(S)	60, 70, 80	88	4-1
1 Meg x 32	4 Megabytes	MT8D88C132H(S)	60, 70, 80	88	4-17
1 Meg x 32	4 Megabytes	MT8D88C132V(S)	60, 70, 80	88	4-33
1 Meg x 32	4 Megabytes	MT8D88C132VH(S)	60, 70, 80	88	4-49
2 Meg x 32	8 Megabytes	MT16D88C232(S)	60, 70, 80	88	4-1
2 Meg x 32	8 Megabytes	MT16D88C232H(S)	60, 70, 80	88	4-17
2 Meg x 32	8 Megabytes	MT16D88C232V(S)	60, 70, 80	88	4-33
2 Meg x 32	8 Megabytes	MT16D88C232VH(S)	60, 70, 80	88	4-49
4 Meg x 32	16 Megabytes	MT8D88C432(S)	60, 70, 80	88	4-1
4 Meg x 32	16 Megabytes	MT8D88C432H(S)	60, 70, 80	88	4-17
4 Meg x 32	16 Megabytes	MT8D88C432V(S)	60, 70, 80	88	4-33
4 Meg x 32	16 Megabytes	MT8D88C432VH(S)	60, 70, 80	88	4-49
8 Meg x 32	32 Megabytes	MT16D88C832(S)	60, 70, 80	88	4-1
8 Meg x 32	32 Megabytes	MT16D88C832H(S)	60, 70, 80	88	4-17
8 Meg x 32	32 Megabytes	MT16D88C832V(S)	60, 70, 80	88	4-33
8 Meg x 32	32 Megabytes	MT16D88C832VH(S)	60, 70, 80	88	4-49

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DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Typical Power Dissipation		Package and Number of Pins				Page
				Standby	Active	PDIP	ZIP	SOJ	TSOP	
1 Meg x 1	FP	MT4C1024	60, 70, 80	3mW	175mW	18	20	20/26	-	1-1
1 Meg x 1	FP, LP	MT4C1024 L	60, 70, 80	0.8mW	175mW	18	20	20/26	-	1-1
1 Meg x 1	SC	MT4C1026	70, 80, 100	3mW	175mW	18	20	20/26	-	1-13
4 Meg x 1	FP	MT4C1004J	60, 70, 80	3mW	225mW	-	20	20/26	20/26	1-25
4 Meg x 1	FP, S	MT4C1004J S	60, 70, 80	0.8mW	225mW	-	20	20/26	20/26	1-25
4 Meg x 1	SC	MT4C1006J	70, 80	3mW	225mW	-	20	20/26	-	1-39
16 Meg x 1	FP, 4KR	MT4C16M1A1	60, 70	4mW	200mW	-	-	24/26	-	1-51
256K x 4	FP	MT4C4256	60, 70, 80	3mW	175mW	20	20	20/26	-	1-63
256K x 4	FP, LP	MT4C4256 L	60, 70, 80	0.8mW	175mW	20	20	20/26	-	1-63
256K x 4	SC	MT4C4258	70, 80 ,100	3mW	175mW	20	20	20/26	-	1-75
1 Meg x 4	FP	MT4C4001J	60, 70, 80	3mW	225mW	-	20	20/26	20/26	1-87
1 Meg x 4	FP, S	MT4C4001J S	60, 70, 80	0.8mW	225mW	-	20	20/26	20/26	1-87
1 Meg x 4	FP, LV	MT4LC4001J	60, 70, 80	1.2mW	100mW	-	-	20/26	20/26	1-103
1 Meg x 4	FP, LV, S	MT4LC4001J S	60, 70, 80	250µW	100mW	-	-	20/26	20/26	1-103
1 Meg x 4	SC	MT4C4003J	70, 80	3mW	225mW	-	20	20/26	-	1-115
1 Meg x 4	EDO, LV	MT4LC4007J	60, 70, 80	1.2mW	100mW	-	-	20/26	20/26	1-127
1 Meg x 4	EDO, LV, S	MT4LC4007J S	60, 70, 80	250µW	100mW	-	-	20/26	20/26	1-127
4 Meg x 4	FP, 4KR	MT4C4M4A1	60, 70	3mW	200mW	-	-	24/28	-	1-141
4 Meg x 4	FP, 2KR	MT4C4M4B1	60, 70	3mW	275mW	-	-	24/28	-	1-141
4 Meg x 4	FP, 4KR	MT4C4M4A1	60, 70	3mW	225mW	-	-	24/26	24/26	1-155
4 Meg x 4	FP, 2KR	MT4C4M4B1	60, 70	3mW	275mW	-	-	24/26	24/26	1-155
4 Meg x 4	FP, 2KR, S	MT4C4M4B1 S	60, 70	1mW	275mW	-	-	24/26	24/26	1-155
4 Meg x 4	FP, 4KR, LV	MT4LC4M4A1	60, 70	1mW	150mW	-	-	24/26	24/26	1-169
4 Meg x 4	FP, 2KR, LV	MT4LC4M4B1	60, 70	1mW	180mW	-	-	24/26	24/26	1-169
4 Meg x 4	FP, 2KR, LV, S	MT4LC4M4B1 S	60, 70	0.4mW	180mW	-	-	24/26	24/26	1-169
4 Meg x 4	EDO, LV	MT4LC4M4E9	60, 70	1mW	150mW	-	-	24/26	24/26	1-183
4 Meg x 4	EDO, LV, S	MT4LC4M4E9 S	60, 70	0.4mW	150mW	-	-	24/26	24/26	1-183
512K x 8	FP	MT4C8512	60, 70, 80	3mW	250mW	-	-	28	-	1-197
2 Meg x 8	FP, 2KR, LV	MT4LC2M8B1	60, 70	1.2mW	200mW	-	-	28	28	1-209
2 Meg x 8	FP, 2KR, LV, S	MT4LC2M8B1 S	60, 70	1.2mW	200mW	-	-	28	28	1-209
2 Meg x 8	EDO, 2KR, LV	MT4LC2M8E7	60, 70	1.2mW	200mW	-	-	28	28	1-221
2 Meg x 8	EDO, 2KR, LV, S	MT4LC2M8E7 S	60, 70	1.2mW	200mW	-	-	28	28	1-221
256K x 16	FP, DW	MT4C16256	60, 70, 80	3mW	375mW	-	-	40	40/44	1-223
256K x 16	FP, DC	MT4C16257	60, 70, 80	3mW	375mW	-	-	40	40/44	1-223
256K x 16	FP, DW, LV	MT4LC16256	60, 70, 80	3mW	175mW	-	-	40	40/44	1-239
256K x 16	FP, DW, LV, S	MT4LC16256 S	60, 70, 80	0.3mW	175mW	-	-	40	40/44	1-239
256K x 16	FP, DC, LV	MT4LC16257	60, 70, 80	3mW	175mW	-	-	40	40/44	1-239
256K x 16	FP, DC, LV, S	MT4LC16257 S	60, 70, 80	0.3mW	175mW	-	-	40	40/44	1-239
256K x 16	EDO, DC	MT4C16270	60, 70, 80	3mW	375mW	-	-	40	40/44	1-257
256K x 16	EDO, DC, LV	MT4LC16270	60, 70, 80	0.3mW	165mW	-	-	40	40/44	1-273
256K x 16	FP, ASY, DW	MT4C16260	60, 70, 80	3mW	375mW	-	-	40	-	1-289
1 Meg x 16	FP, DC, LV	MT4LC1M16C3	60, 70, 80	3mW	225mW	-	-	42	44/50	1-303
1 Meg x 16	FP, DC, S, LV	MT4LC1M16C3 S	60, 70, 80	3mW	225mW	-	-	42	44/50	1-303

FP = FAST PAGE MODE, SC = STATIC COLUMN, LP = Low Power, Extended Refresh; WPB = WRITE-PER-BIT, EDO = Extended Data-Out, DW = Dual WE, DC = Dual CAS, 2KR = 2,048 Refresh, 4KR = 4,096 Refresh, S = SELF REFRESH, ASY = Asymmetrical Addressing, LV = Low Voltage

DRAM

1 MEG x 1 DRAM

STANDARD OR LOW POWER, EXTENDED REFRESH

FEATURES

- 512-cycle refresh in 8ms (MT4C1024) or 64ms (MT4C1024 L)
- Industry-standard x1 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 0.8mW standby; 175mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- FAST PAGE MODE access cycle
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and Extended (MT4C1024 L)
- Low CMOS Standby Current, 200µA maximum (MT4C1024 L)

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic ZIP (350 mil)	Z
• Version	
1,024-cycle refresh in 8ms	None
1,024-cycle refresh in 64ms	L

- Part Number Example: MT4C1024DJ-7 L

PIN ASSIGNMENT (Top View)

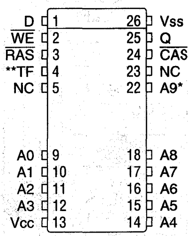
18-Pin DIP (DA-1)

Signal	Pin	Pin	Signal
D	1	18	Vss
WE	2	17	Q
RAS	3	16	CAS
**TF	4	15	A9*
A0	5	14	A8
A1	6	13	A7
A2	7	12	A6
A3	8	11	A5
Vcc	9	10	A4

20-Pin ZIP (DB-1)

Signal	Pin	Pin	Signal
*A9	1	2	CAS
Q	3	4	Vss
D	5	6	WE
RAS	7	8	TF**
NC	9	10	NC
A0	11	12	A1
A2	13	14	A3
Vcc	15	16	A4
A5	17	18	A6
A7	19	20	A8

20/26-Pin SOJ (DC-1)



*Address not used for RAS ONLY REFRESH
**TF = Test Function; VIN must not exceed Vcc+1V for normal operation.

GENERAL DESCRIPTION

The MT4C1024(L) is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin, data-out (Q), remains open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled by holding RAS LOW and

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strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms for the MT4C1024 or 64ms for the MT4C1024 L, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
LOW POWER, FAST PAGE MODE

$\overline{WE}$, $\overline{CAS}$, A0–A9, $\overline{RAS}$, D, Q, Vcc, Vss

*EARLY WRITE DETECTION CIRCUIT · NO. 2 CLOCK GENERATOR · DATA-IN BUFFER · DATA-OUT BUFFER · COLUMN-ADDRESS BUFFER (10) · COLUMN DECODER · REFRESH CONTROLLER · SENSE AMPLIFIERS I/O GATING · REFRESH COUNTER · ROW-ADDRESS BUFFERS (10) · ROW DECODER · COMPLEMENT SELECT · ROW SELECT (2 of 1024) · MEMORY ARRAY · ROW TRANSFER (1 of 2) · NO. 1 CLOCK GENERATOR

***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

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DRAM

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA D (Data-In)	DATA Q (Data-Out)
Standby		H	H→X	X	X	X	"don't care"	High-Z
READ		L	L	H	ROW	COL	"don't care"	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In	High-Z
READ WRITE		L	L	H→L	ROW	COL	Data-In	Data-Out
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	"don't care"	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	"don't care"	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In	High-Z
	2nd Cycle	L	H→L	L	n/a	COL	Data-In	High-Z
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Data-In	Data-Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Data-In	Data-Out
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	"don't care"	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	"don't care"	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In	High-Z
CBR REFRESH		H→L	L	X	X	X	"don't care"	High-Z
Extended Refresh (MT4C1024 L only)		H→L	L	X	X	X	"don't care"	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 600mW
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any inputs 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

PARAMETER/CONDITION	VERSION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)		ICC1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	MT4C1024	ICC2	1	1	1	mA	
	MT4C1024 L	ICC2	200	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Single Address Cycling: tRC = tRC [MIN])		ICC3	90	80	70	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])		ICC4	70	60	50	mA	3, 4, 26
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])		ICC5	90	80	70	mA	3, 26
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])		ICC6	90	80	70	mA	3, 5
REFRESH CURRENT: Extended Average power supply current during Extended Refresh: CAS = 0.2V or CBR cycling; RAS = tRAS (MIN) to1µs; WE, A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left open); tRC = 125µs (512 rows at 125µs = 64ms)	MT4C1024 L	ICC7	200	200	200	µA	3, 5, 24

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C_{I1}		5	pF	2
Input Capacitance: RAS, CAS, WE	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5.0V ± 10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	135		155		175		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	60		65		70		ns	
Access time from RAS	^tRAC		60		70		80	ns	14
Access time from CAS	^tCAC		20		20		20	ns	15
Access time from column-address	^tAA		30		35		40	ns	
Access time from CAS precharge	^tCPA		35		40		45	ns	
RAS pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^tRSH	20		20		20		ns	
RAS precharge time	^tRP	40		50		60		ns	
CAS pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	^tCSH	60		70		80		ns	
CAS precharge time (CBR REFRESH)	^tCPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
RAS to CAS delay time	^tRCD	20	40	20	50	20	60	ns	17
CAS to RAS precharge time	^tCRP	5		5		5		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
RAS to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	15		15		15		ns	
Column-address hold time (referenced to RAS)	^tAR	45		55		60		ns	
Column-address to RAS lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	^tRRH	0		0		0		ns	19
CAS to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	3	20	3	20	3	20	ns	20, 25
WE command setup time	^tWCS	0		0		0		ns	21

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	60		70		80		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	30		35		40		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	15		20		20		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles) MT4C1024 / MT4C1024 L	^tREF		8 / 64		8 / 64		8 / 64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		15		15		ns	5

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DRAM

NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 5V ±10%; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE WRITE, and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE WRITE and the state of Q is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. Extended refresh current is reduced as ^tRAS is reduced from its maximum specification during the extended refresh cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.

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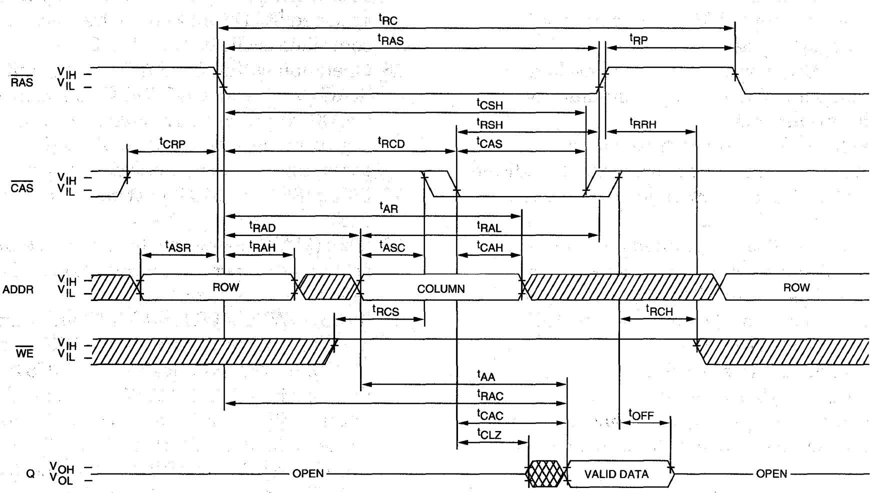
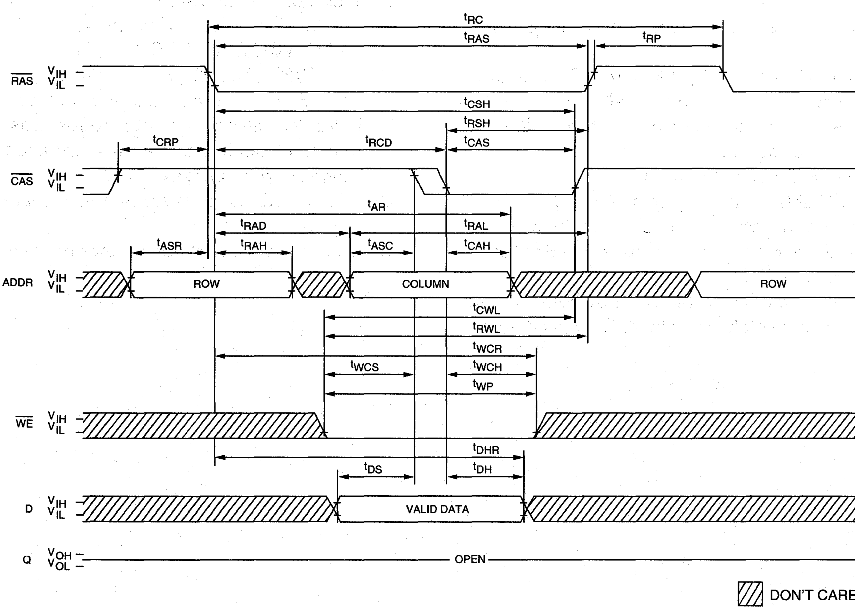
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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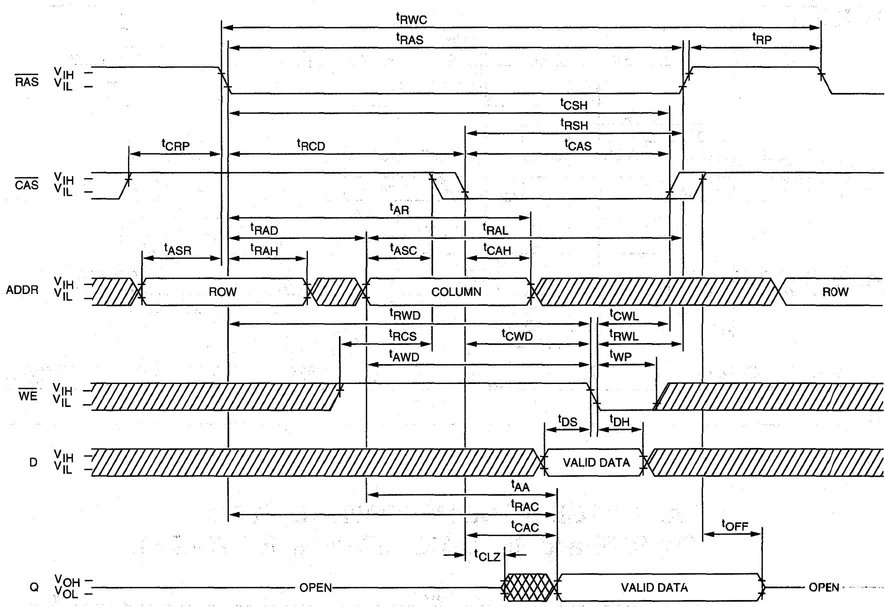
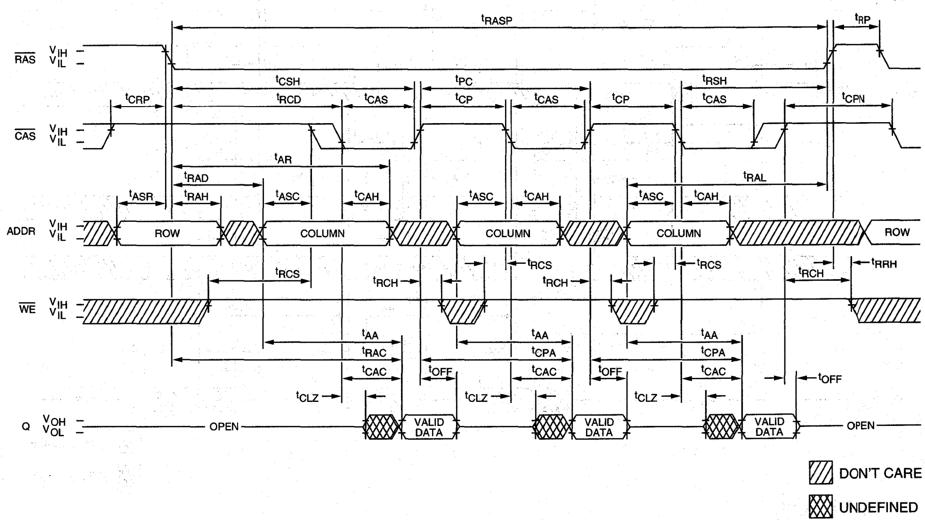
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

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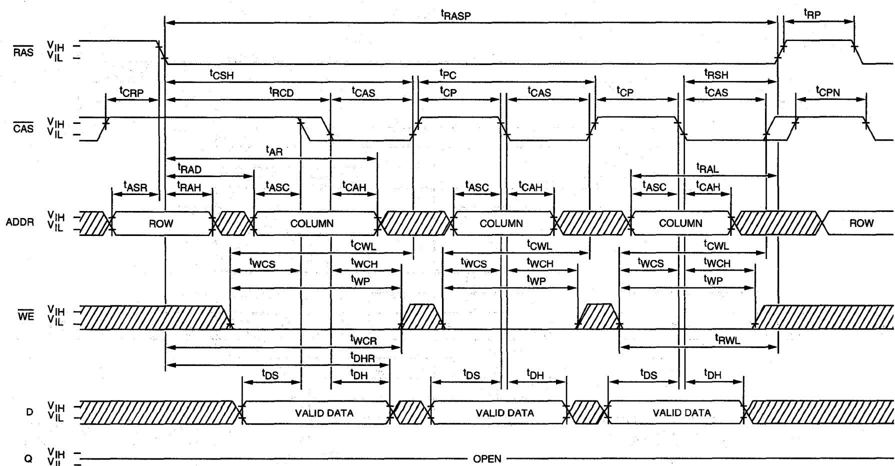
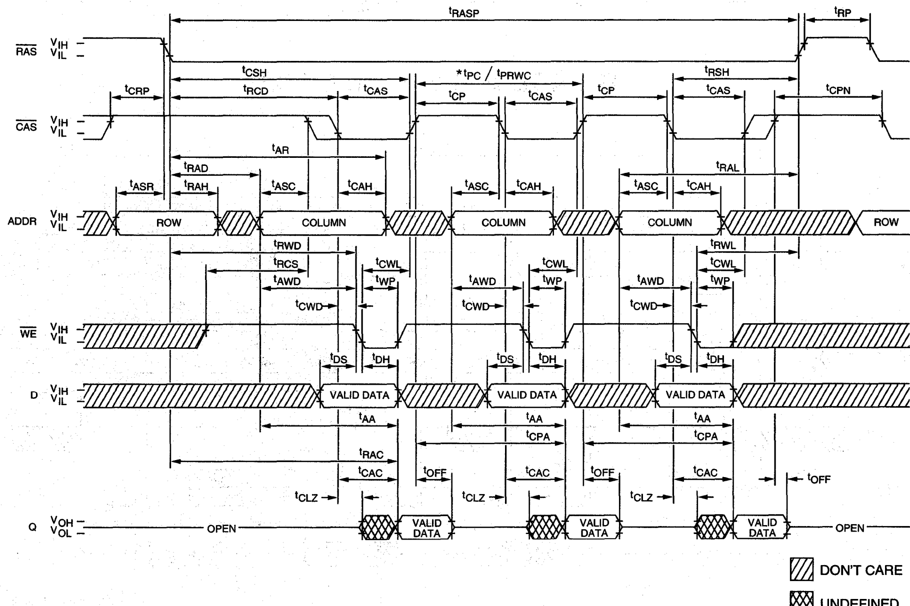
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



*tPC is for LATE WRITE only.

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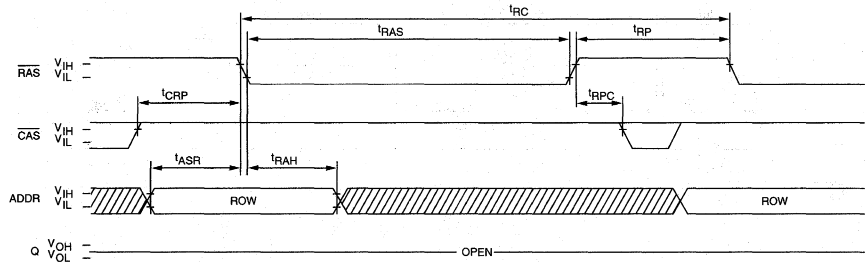
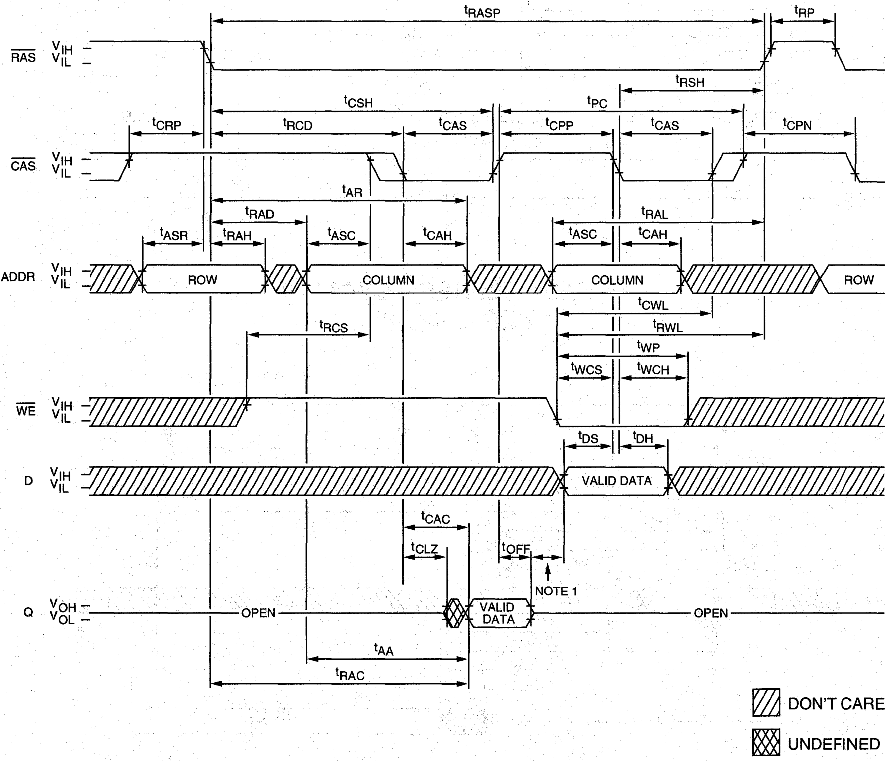
RAS ONLY REFRESH CYCLE
(ADDR = A0-A8; A9 and WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: ^{t}CPP(MIN) or ^{t}CP(whichever is greater) + ^{t}DS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

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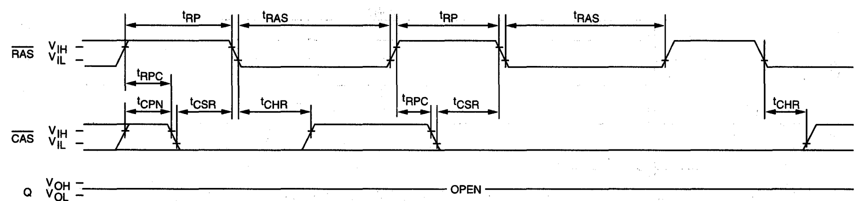
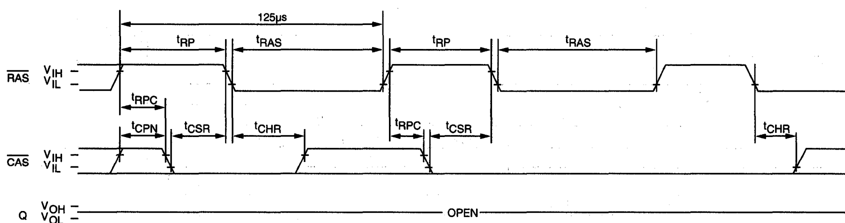
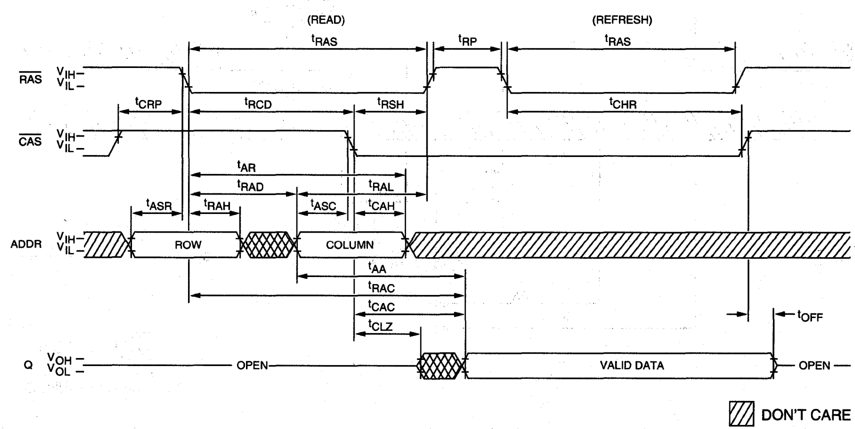
CBR REFRESH CYCLE
(A0-A9 and $\overline{WE}$ = DON'T CARE)



EXTENDED REFRESH CYCLE (MT4C1024 L ONLY)
(A0-A9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)



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DRAM

1 MEG x 1 DRAM

STATIC COLUMN

FEATURES

- Industry-standard x1 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- 512-cycle refresh in 8ms
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR), and HIDDEN
- STATIC COLUMN access cycle

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic ZIP (350 mil)	Z

- Part Number Example: MT4C1026DJ-7

PIN ASSIGNMENT (Top View)

18-Pin DIP (DA-1)

Pin	Signal	Pin	Signal
1	D	18	Vss
2	$\overline{\text{WE}}$	17	Q
3	$\overline{\text{RAS}}$	16	$\overline{\text{CAS}}$
4	**TF	15	A9*
5	A0	14	A8
6	A1	13	A7
7	A2	12	A6
8	A3	11	A5
9	Vcc	10	A4

20-Pin ZIP (DB-1)

Signal	Pin	Pin	Signal
*A9	1	2	$\overline{\text{CAS}}$
Q	3	4	Vss
D	5	6	$\overline{\text{WE}}$
$\overline{\text{RAS}}$	7	8	TF**
NC	9	10	NC
A0	11	12	A1
A2	13	14	A3
Vcc	15	16	A4
A5	17	18	A6
A7	19	20	A8

20/26-Pin SOJ (DC-1)

Signal	Pin	Pin	Signal
D	1	26	Vss
$\overline{\text{WE}}$	2	25	Q
$\overline{\text{RAS}}$	3	24	$\overline{\text{CAS}}$
**TF	4	23	NC
NC	5	22	A9*
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

*Address not used for $\overline{\text{RAS}}$ ONLY REFRESH
**TF = Test Function; V_{IN} must not exceed Vcc+1V for normal operation.

GENERAL DESCRIPTION

The MT4C1026 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{\text{RAS}}$ is used to latch the first 10 bits and $\overline{\text{CAS}}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin, data-out (Q), remains open (High-Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ WRITE cycle.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. After the first READ, any column-address transition will result in new data-out. Unlike the PAGE MODE, which requires $\overline{\text{CAS}}$ to be toggled for each successive PAGE MODE access, the STATIC COLUMN allows $\overline{\text{CAS}}$ to be left LOW for successive STATIC COLUMN accesses. Returning $\overline{\text{RAS}}$ HIGH terminates the STATIC COLUMN operation.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE) or $\overline{\text{RAS}}$ REFRESH cycle ($\overline{\text{RAS}}$ ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{\text{RAS}}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{\text{RAS}}$ addressing.

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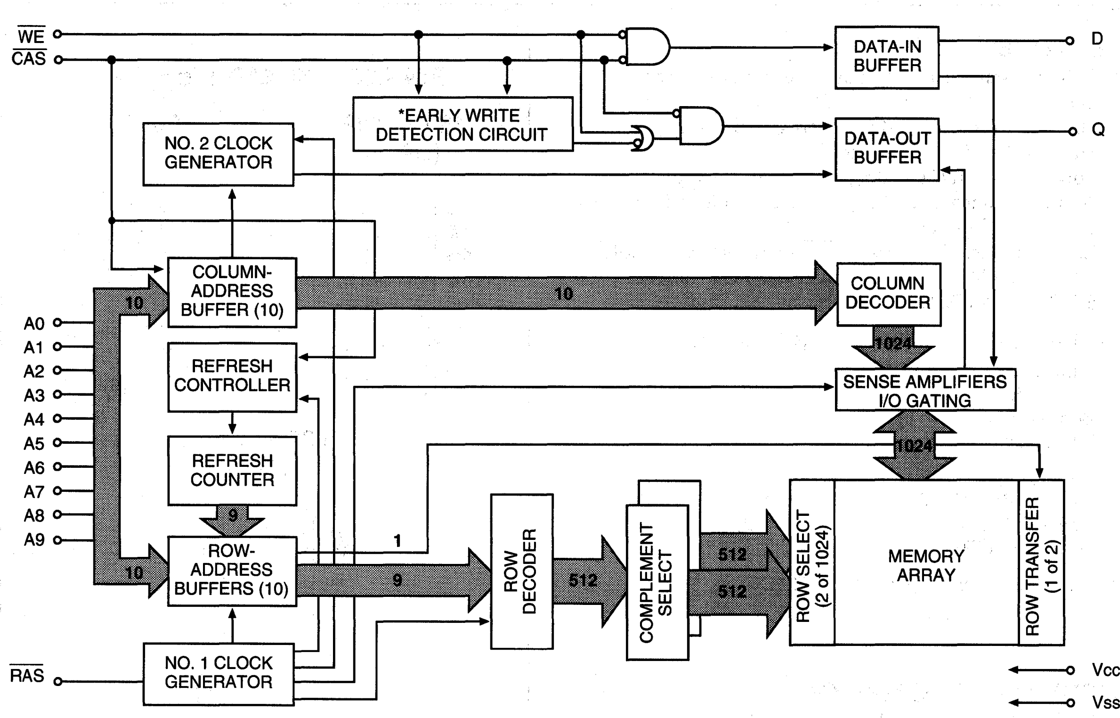
FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES		DATA	
					^tR	^tC	D (Data-In)	Q (Data-Out)
Standby		H	H→X	X	X	X	"don't care"	High-Z
READ		L	L	H	ROW	COL	"don't care"	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In	High-Z
READ WRITE		L	L	H→L	ROW	COL	Data-In	Data-Out
STATIC-COLUMN READ	1st Cycle	L	L	H	ROW	COL	"don't care"	Data-Out
	2nd Cycle	L	L	H	n/a	COL	"don't care"	Data-Out
STATIC-COLUMN EARLY-WRITE	1st Cycle	L	L	L	ROW	COL	Data-In	High-Z
	2nd Cycle	L	L	H→L	n/a	COL	Data-In	High-Z
STATIC-COLUMN READ-WRITE	1st Cycle	L	L	H→L	ROW	COL	Data-In	Data-Out
	2nd Cycle	L	L	H→L	n/a	COL	Data-In	Data-Out
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	"don't care"	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	"don't care"	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In	High-Z
CBR REFRESH		H→L	L	X	X	X	"don't care"	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 600mW
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-7	-8	-10		
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	80	70	60	mA	3, 4
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tSC = ^tSC [MIN])	I_{CC4}	60	50	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling; $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	80	70	60	mA	3
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	80	70	60	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C_{I1}		5	pF	2
Input Capacitance: RAS, CAS, WE	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ WRITE cycle time	^tRWC	155		175		205		ns	
STATIC-COLUMN READ or WRITE cycle time	^tSC	35		40		50		ns	
STATIC-COLUMN READ-WRITE cycle time	^tSRWC	70		80		100		ns	
Access time from RAS	^tRAC		70		80		100	ns	14
Access time from CAS	^tCAC		20		20		25	ns	15
Access time from column-address	^tAA		35		40		50	ns	
RAS pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
RAS pulse width (STATIC COLUMN)	^tRASC	70	100,000	80	100,000	100	100,000	ns	
RAS hold time	^tRSH	20		20		25		ns	
RAS precharge time	^tRP	50		60		70		ns	
CAS pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	
CAS hold time	^tCSH	70		80		100		ns	
CAS precharge time	^tCPN	10		10		15		ns	16
CAS precharge time (STATIC COLUMN)	^tCP	10		10		10		ns	
RAS to CAS delay time	^tRCD	20	50	20	60	25	75	ns	17
CAS to RAS precharge time	^tCRP	5		5		5		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		15		ns	
RAS to column-address delay time	^tRAD	15	35	15	40	20	50	ns	18
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	15		15		20		ns	
Column-address hold time (referenced to RAS)	^tAR	80		90		100		ns	
Column-address to RAS lead time	^tRAL	35		40		50		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	^tRRH	0		0		0		ns	19
CAS to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	3	20	3	20	3	20	ns	20, 24

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Column-address hold time EARLY WRITE (referenced to $\overline{RAS}$)	^tAWR	55		60		70		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	70		80		100		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	35		40		50		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		20		25		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		15		ns	5
Write inactive time	^tWI	10		10		10		ns	
Previous WRITE to column-address delay time	^tLWAD	20	30	20	35	25	45	ns	
Previous WRITE to column-address hold time	^tAHLW	65		75		95		ns	
Output data hold time from column-address	^tAOH	5		5		5		ns	
Output data enable from WRITE	^tOW	$^tAA + 5$		$^tAA + 5$		$^tAA + 5$		ns	
Access time from last WRITE	^tALW	65		75		95		ns	
Column-address hold time referenced to $\overline{RAS}$ HIGH	^tAH	5		5		10		ns	
$\overline{CAS}$ pulse width in STATIC COLUMN mode	^tCSC	^tCAS		^tCAS		^tCAS		ns	
Output data hold from WRITE	^tWOH	0		0		0		ns	

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 5V ±10%; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE, and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE WRITE and the state of Q is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. The 3ns minimum is a parameter guaranteed by design.

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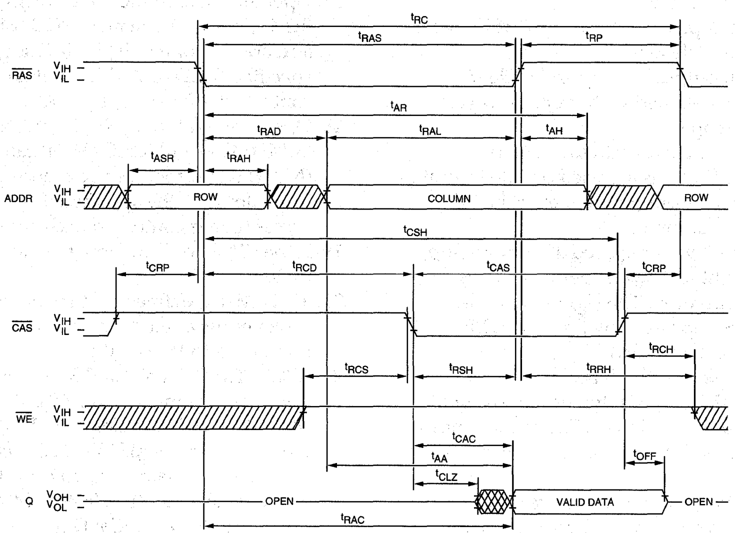
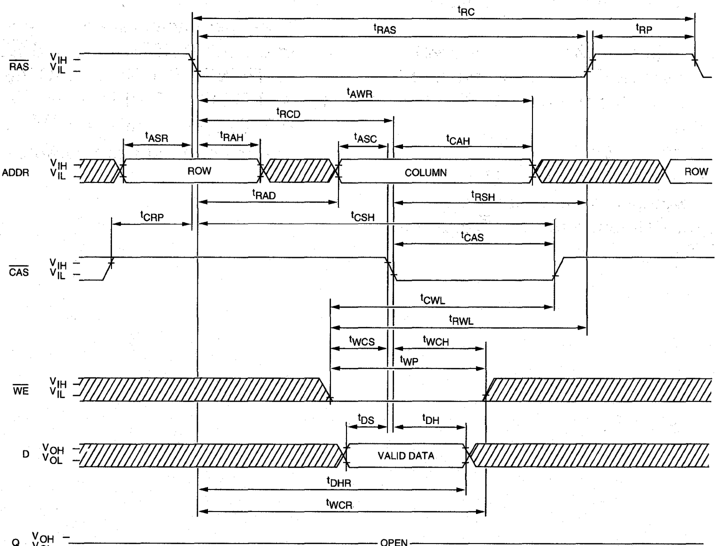
READ CYCLE



EARLY WRITE CYCLE



UNDEFINED

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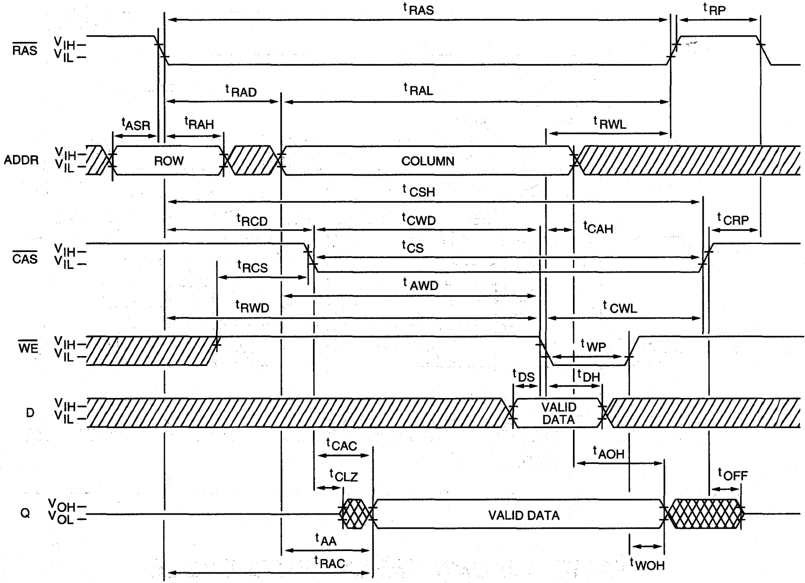
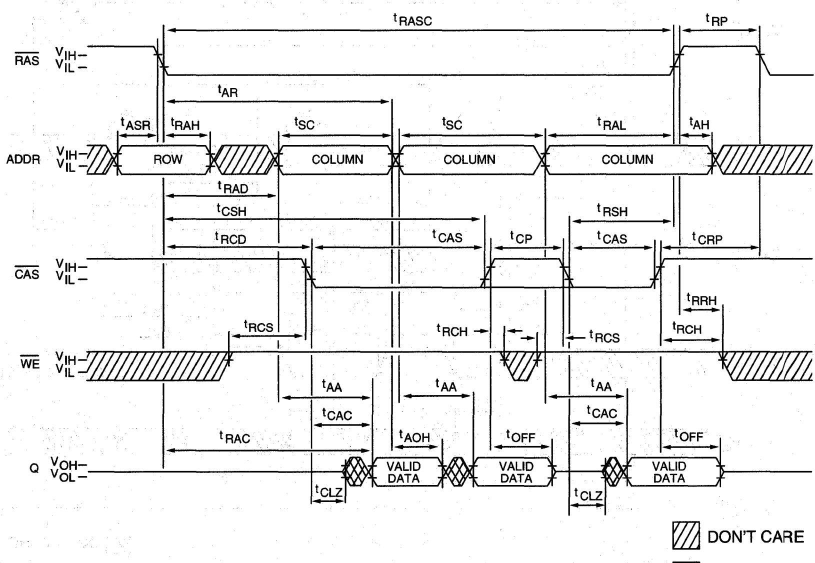
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



STATIC-COLUMN READ CYCLE



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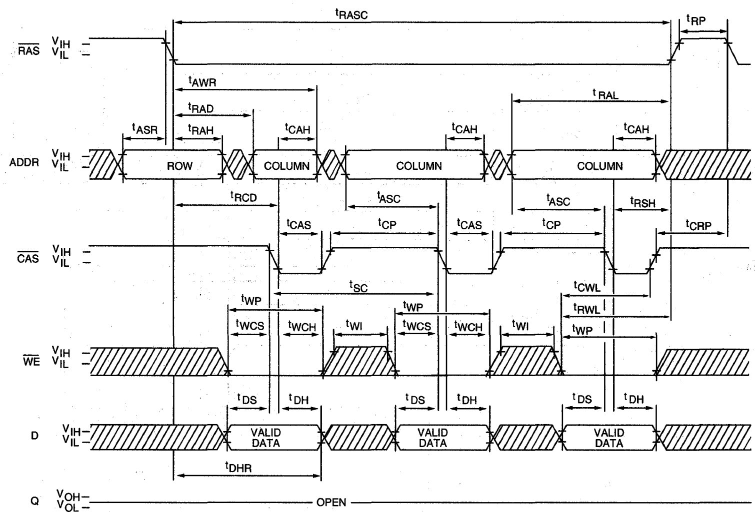
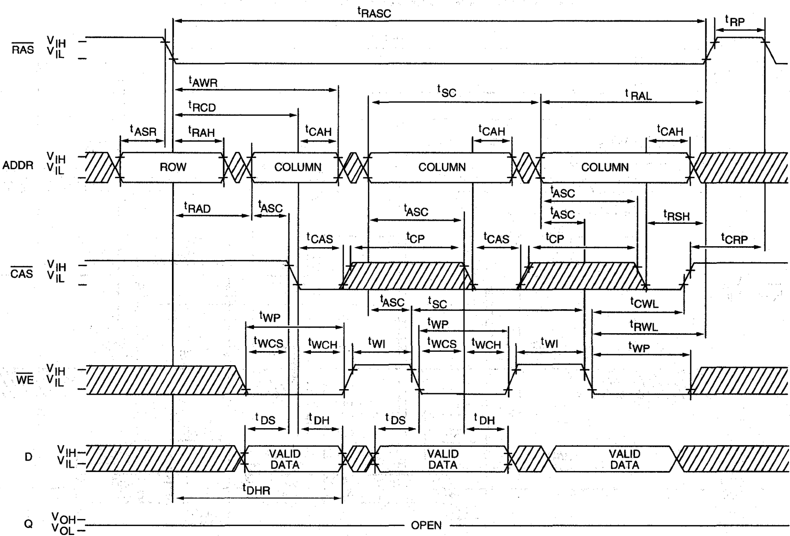
STATIC-COLUMN EARLY-WRITE CYCLE
(CAS Controlled)



STATIC-COLUMN EARLY-WRITE CYCLE
(WE Controlled)



DON'T CARE

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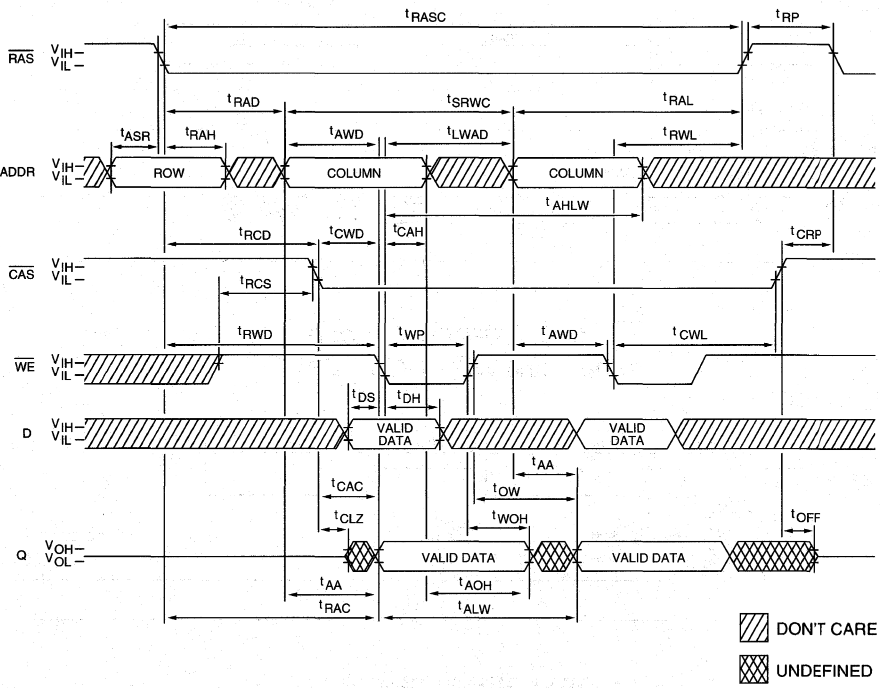
STATIC-COLUMN READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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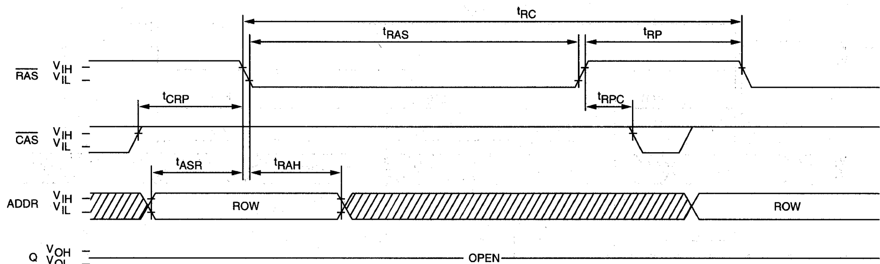
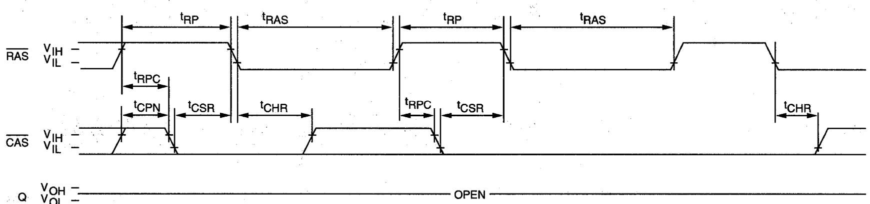
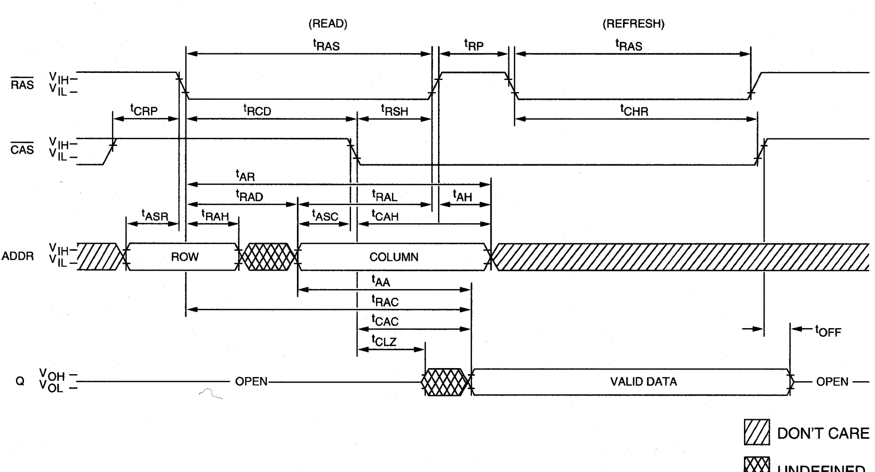
RAS ONLY REFRESH CYCLE
(ADDR = A0-A8; A9 and WE = DON'T CARE)



CBR REFRESH CYCLE
(A0-A9 and WE = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
(WE = HIGH)



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DRAM

4 MEG x 1 DRAM

STANDARD OR SELF REFRESH

FEATURES

- 1,024-cycle refresh distributed across 16ms (MT4C1004J) or 128ms (MT4C1004J S only)
- Industry-standard pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN; optional Extended and SELF REFRESH modes (MT4C1004J S only)
- FAST PAGE MODE access cycle
- Low power, 0.8mW standby; 225mW active, typical (MT4C1004J S)

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG
Plastic ZIP (400 mil)	Z
• Version	
1,024-cycle refresh in 16ms	None
1,024-cycle refresh in 128ms	S

- Part Number Example: MT4C1004JDJ-6 S

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ (DC-1)

Signal	Pin	Pin	Signal
D	1	26	Vss
WE	2	25	Q
RAS	3	24	CAS
NC	4	23	NC
*A10	5	22	A9
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

20-Pin ZIP (DB-2)

Signal	Pin	Pin	Signal
A9	1	2	CAS
Q	3	4	Vss
D	5	6	WE
RAS	7	8	A10*
NC	9	10	NC
A0	11	12	A1
A2	13	14	A3
Vcc	15	16	A4
A5	17	18	A6
A7	19	20	A8

20/26-Pin TSOP (DD-1)

Signal	Pin	Pin	Signal
D	1	26	Vss
WE	2	25	Q
RAS	3	24	CAS
NC	4	23	NC
*A10	5	22	A9
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

*Address not used for RAS ONLY REFRESH

GENERAL DESCRIPTION

The MT4C1004J(S) is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin remains open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin, data-out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR, or HIDDEN) so that all 1,024 combinations of

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RAS addresses (A0-A9) are executed at least every 16ms for the MT4C1004J and every 128ms for the MT4C1004J S, regardless of sequence. The CBR and extended refresh cycles will invoke the internal refresh counter for automatic RAS addressing.

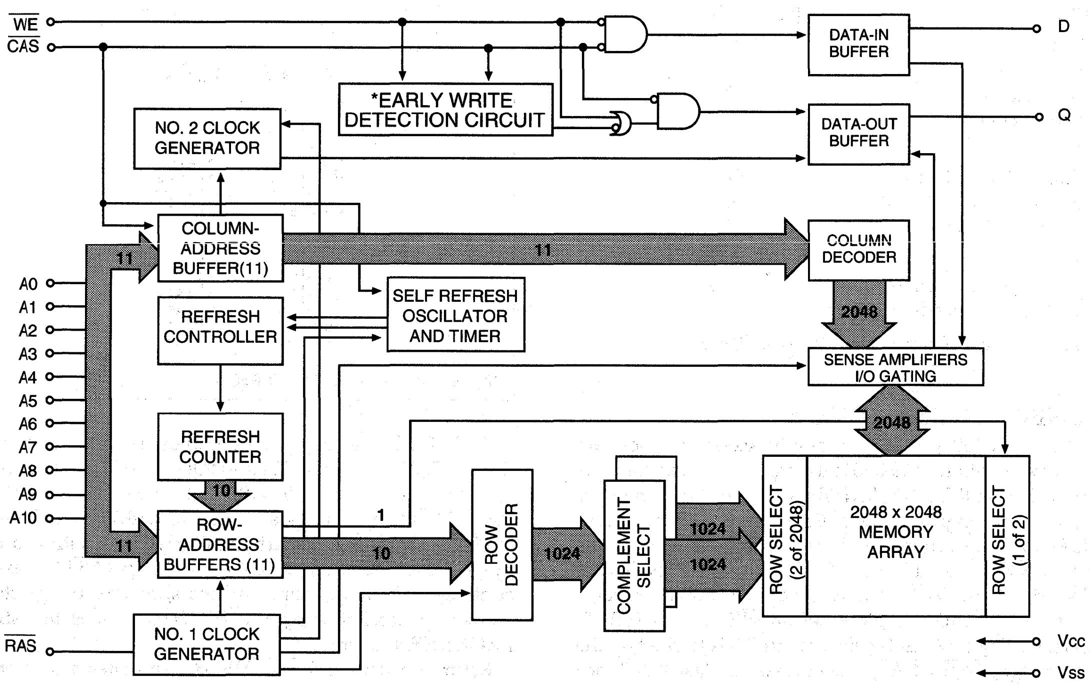
REFRESH

An optional SELF REFRESH mode is also available. The "S" option allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified tRASS. Additionally, the "S" option allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of tRPS (≈tRC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or BURST REFRESH sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



***NOTE:** 1. If WE goes LOW prior to CAS going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If CAS goes LOW prior to WE going LOW, EW detection circuit output is a LOW (LATE WRITE).

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES		DATA	
					ᵗR	ᵗC	D (Data-In)	Q (Data-Out)
Standby		H	H→X	X	X	X	"don't care"	High-Z
READ		L	L	H	ROW	COL	"don't care"	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In	High-Z
READ WRITE		L	L	H→L	ROW	COL	Data-In	Data-Out
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	"don't care"	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	"don't care"	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In	High-Z
	2nd Cycle	L	H→L	L	n/a	COL	Data-In	High-Z
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Data-In	Data-Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Data-In	Data-Out
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	"don't care"	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	"don't care"	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In	High-Z
CBR REFRESH		H→L	L	H	X	X	"don't care"	High-Z
SELF REFRESH (MT4C1004J S only)		H→L	L	H	X	X	"don't care"	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

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DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	VERSION	SYMBOL	MAX			UNITS	NOTES
			-6	-7	-8		
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	MT4C1004J	I_{CC2}	1	1	1	mA	
	MT4C1004J S	I_{CC2}	200	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: ^tRC = ^tRC [MIN])		I_{CC3}	110	100	90	mA	3, 4, 27
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])		I_{CC4}	80	70	60	mA	3, 4, 27
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])		I_{CC5}	110	100	90	mA	3, 27
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC6}	110	100	90	mA	3, 5
REFRESH CURRENT: Extended Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$, A0-A10 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	MT4C1004J S	I_{CC7}	300	300	300	µA	3, 5, 7, 25
SELF REFRESH CURRENT: (S-version only) Average power supply current during SELF REFRESH: CBR cycle with $^tRAS \geq {}^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -.2; A0-A10 and D_{IN} = V_{CC} -.2V or .2V (D_{IN} may be left open)	MT4C1004J S	I_{CC8}	300	300	300	µA	5, 28

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}	7	pF	2
Output Capacitance: Q	C_O	7	pF	2

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ WRITE cycle time	tRWC	130		155		175		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	60		70		75		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	15
Access time from column-address	tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	25
$\overline{RAS}$ pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	25
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time (CBR REFRESH)	tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10		10		10		ns	
Row-address setup time	tASR	0		0		0		ns	
Row-address hold time	tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		0		ns	
Column-address hold time	tCAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	tAR	45		50		55		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	tOFF	3	15	3	20	3	20	ns	20, 26
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	21
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		20		20		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	60		70		80		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	30		35		40		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	15		20		20		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles) MT4C1004J / MT4C1004J S	^tREF		16 / 128		16 / 128		16 / 128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	24
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^tRASS	100		100		100		µs	28
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^tRPS	110		130		150		ns	28
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH cycle	^tCHD	10		10		10		ns	28

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE WRITE, READ WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE WRITE and the state of data-out is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. ^tWTS and ^tWTH are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
25. Extended refresh current is reduced as ^tRAS is reduced from its maximum specification during the extended refresh cycle.
26. The 3ns minimum is a parameter guaranteed by design.
27. Column-address changed once each cycle.
28. If the DRAM controller uses a BURST REFRESH, a BURST REFRESH of all rows must be executed upon exiting SELF REFRESH.

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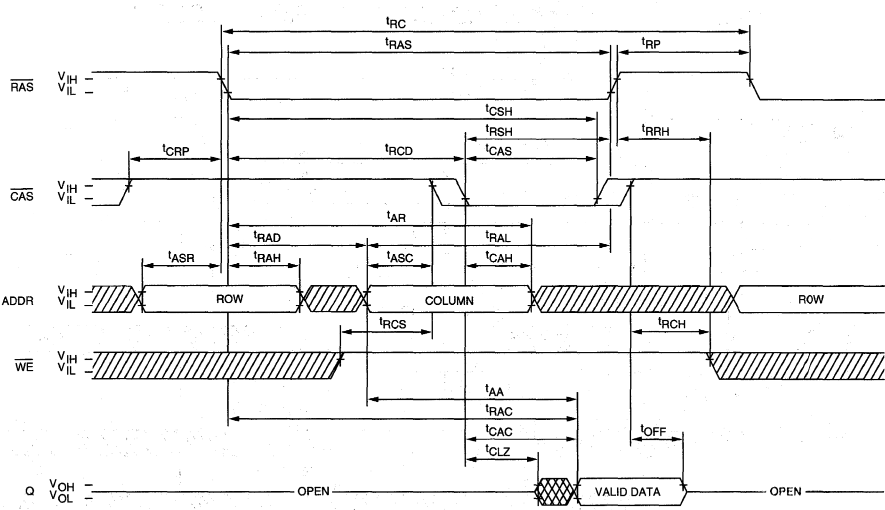
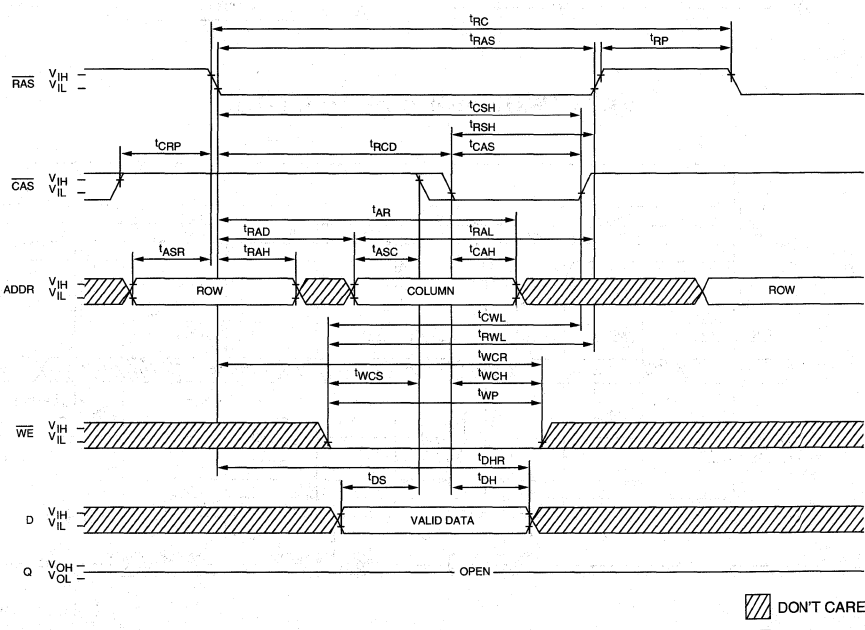
DRAM

READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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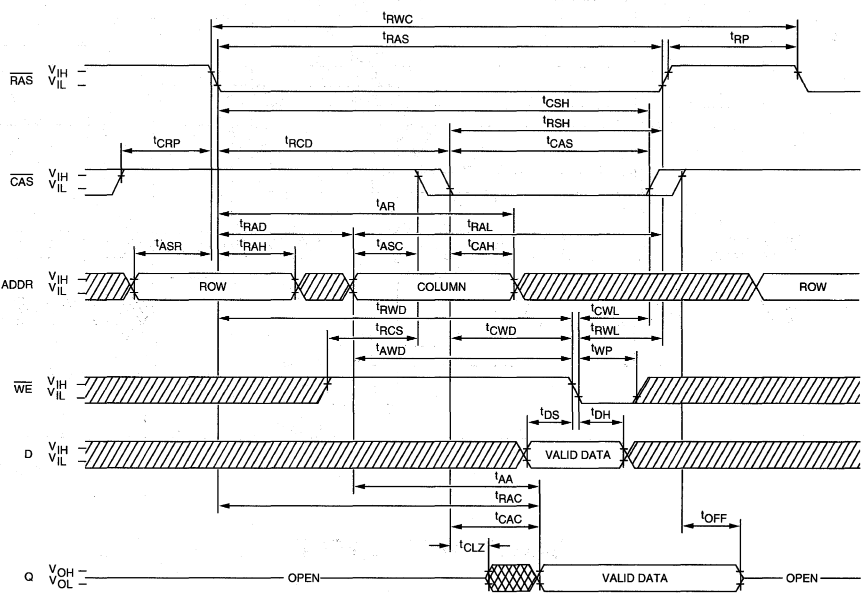
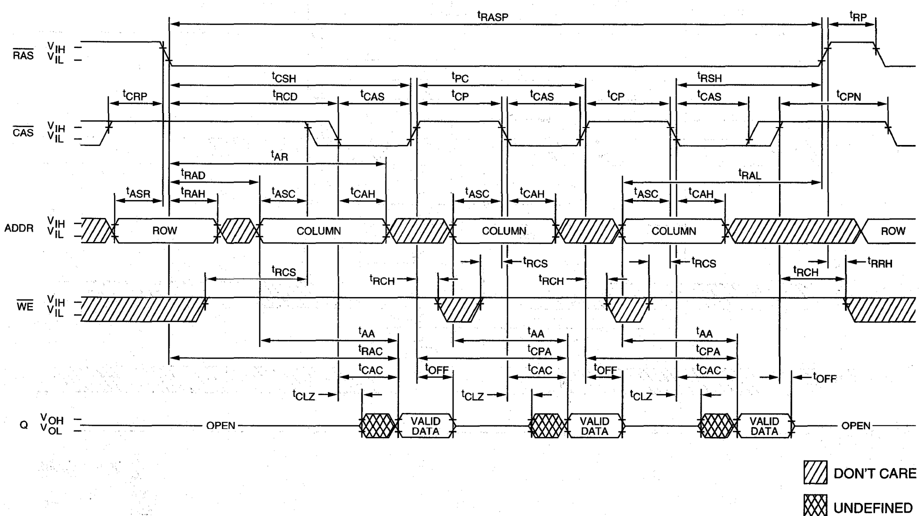
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

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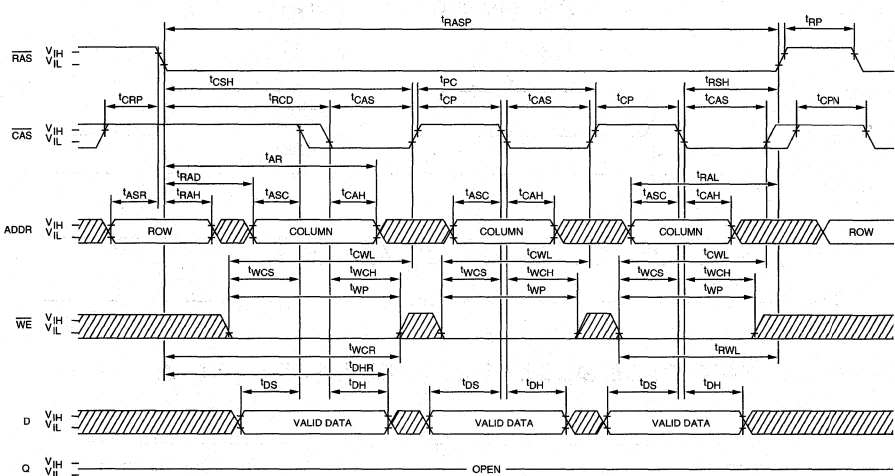
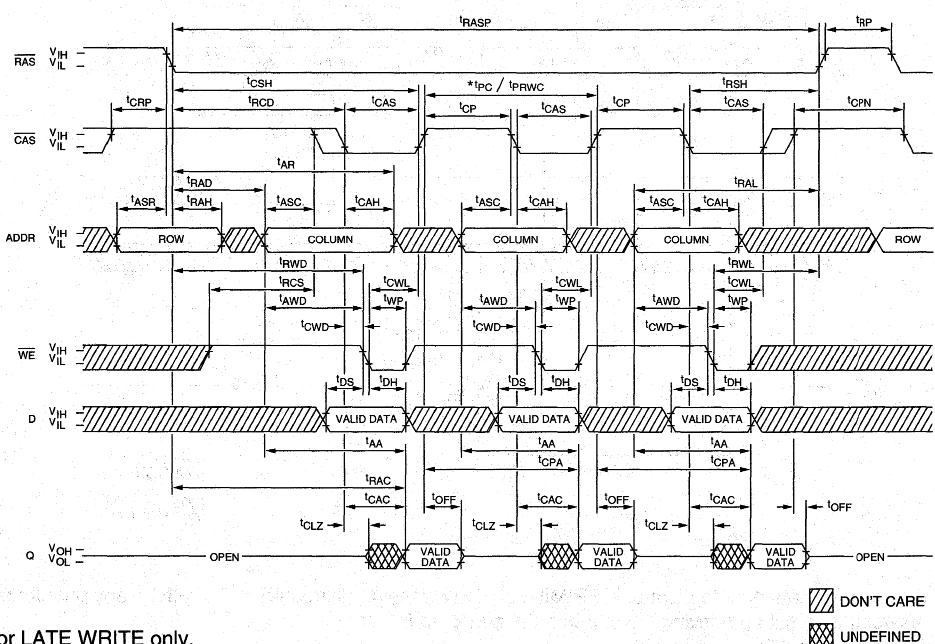
DRAM

FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



*^{t}PC is for LATE WRITE only.

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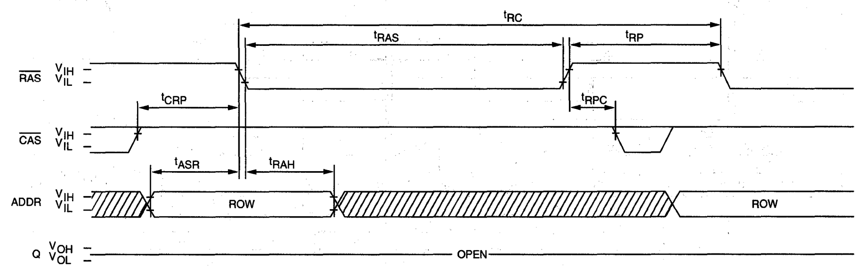
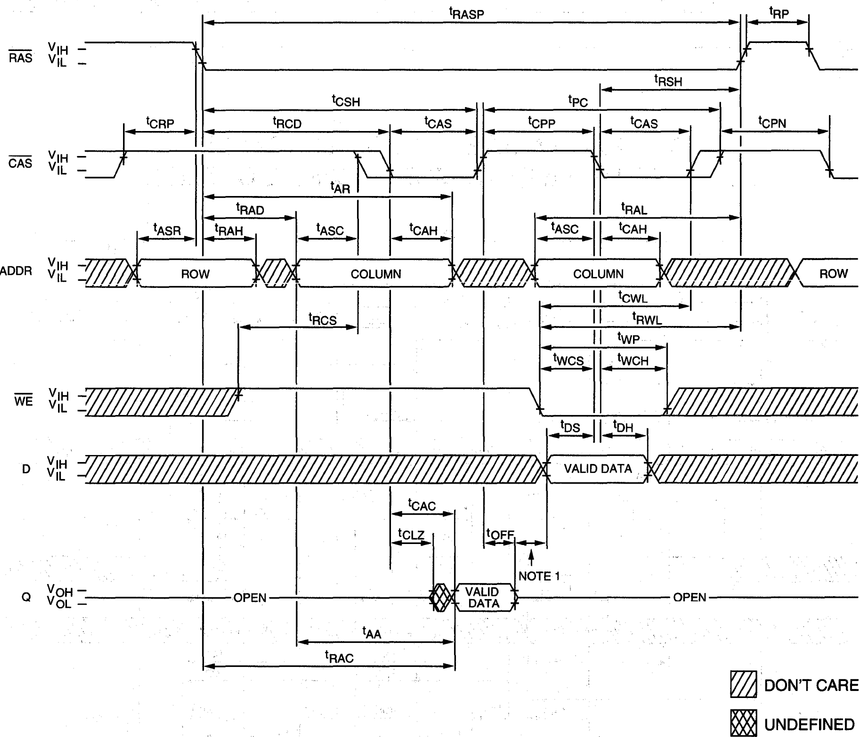
DRAM

RAS ONLY REFRESH CYCLE
(ADDR = A0-A9; A10 and WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE



NOTE:
1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

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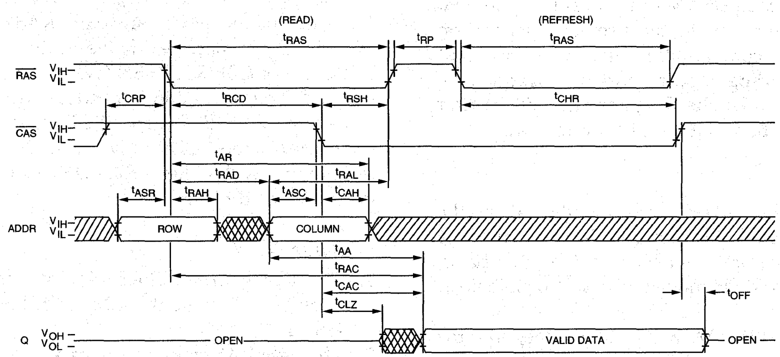
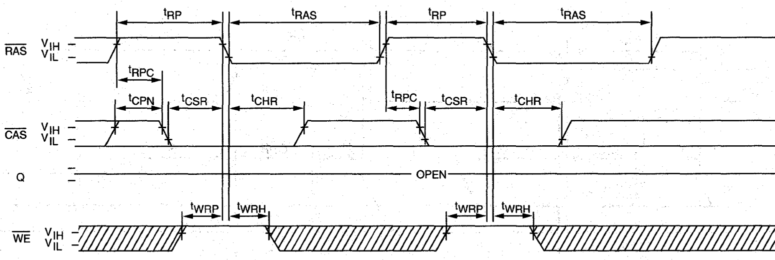
DRAM

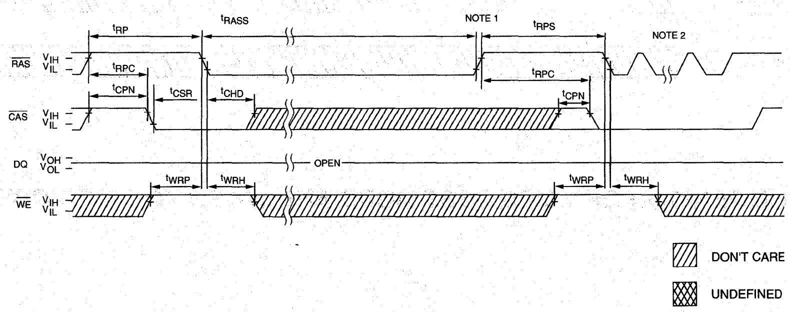
HIDDEN REFRESH CYCLE [23]
(WE = HIGH)



CBR REFRESH CYCLE
(A0-A10 = DON'T CARE)



SELF REFRESH CYCLE (MT4C1004J S ONLY)
(A0-A10 = DON'T CARE)



NOTE:
1. Once tRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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DRAM

4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh cycle of the 1 Meg is the CBR REFRESH cycle. The CBR for the 1 Meg specifies the WE pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the WE pin held at a voltage HIGH level.

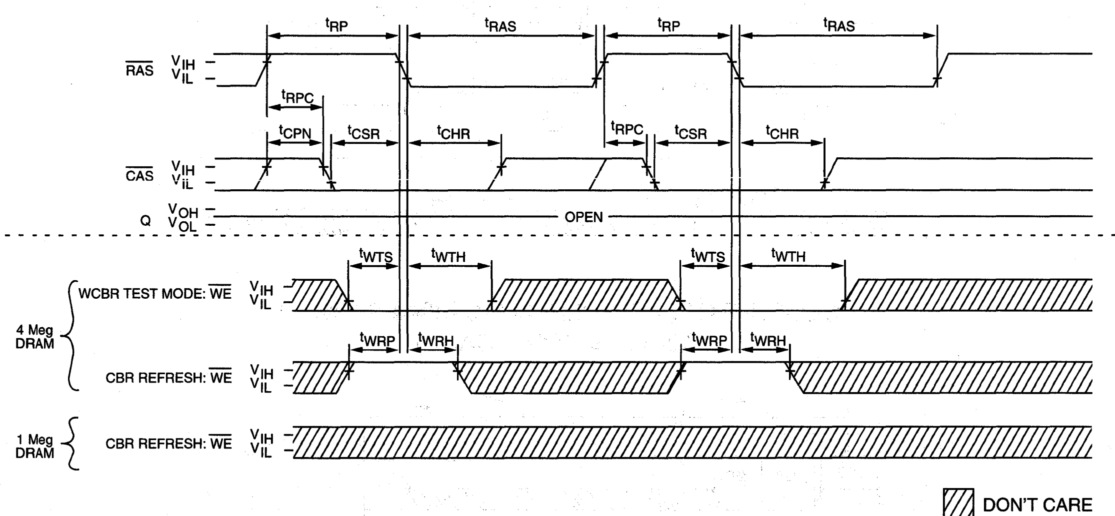
A CBR cycle with WE LOW will put the 4 Meg into the JEDEC-specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight RAS cycles. The 4 Meg POWER-UP is more restrictive in that eight RAS ONLY REFRESH or CBR REFRESH (WE held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC-specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a RAS ONLY or a CBR REFRESH cycle (WE held HIGH).

SUMMARY

1. The 1 Meg CBR REFRESH allows the WE pin to be "don't care" while the 4 Meg CBR requires WE to be HIGH.
2. The eight RAS wake-up cycles on the 1 Meg may be any valid RAS cycle while the 4 Meg may only use RAS ONLY or CBR REFRESH cycles (WE held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

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DRAM

4 MEG x 1 DRAM

STATIC COLUMN

FEATURES

- Industry-standard x1 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- STATIC COLUMN access cycle

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
70ns access	-7
80ns access	-8
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic ZIP (400 mil)	Z

- Part Number Example: MT4C1006JDJ-7

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ (DC-1)

Signal	Pin	Pin	Signal
D	1	26	Vss
WE	2	25	Q
RAS	3	24	CAS
NC	4	23	NC
*A10	5	22	A9
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

20-Pin ZIP (DB-2)

Signal	Pin	Pin	Signal
A9	1	2	CAS
Q	3	4	Vss
D	5	6	WE
RAS	7	8	A10*
NC	9	10	NC
A0	11	12	A1
A2	13	14	A3
Vcc	15	16	A4
A5	17	18	A6
A7	19	20	A8

*Address not used for RAS ONLY REFRESH

GENERAL DESCRIPTION

The MT4C1006J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin remains open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin, data-out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A10) page boundary. After the first read, any column-address transition will result in new data out. Unlike PAGE MODE, which requires CAS to be toggled for each successive PAGE MODE access, STATIC COLUMN allows CAS to be left LOW for successive STATIC COLUMN accesses. Returning RAS HIGH terminates the STATIC COLUMN operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR cycle will invoke the internal refresh counter for automatic RAS addressing.

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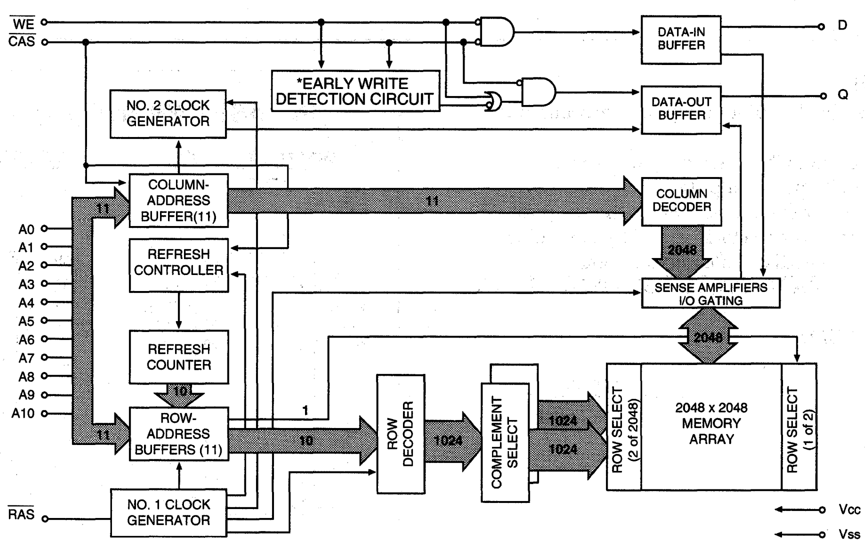
FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA D (Data-In)	DATA Q (Data-Out)
Standby		H	H→X	X	X	X	"don't care"	High-Z
READ		L	L	H	ROW	COL	"don't care"	Data Out
EARLY WRITE		L	L	L	ROW	COL	Data-In	High-Z
READ WRITE		L	L	H→L	ROW	COL	Data-In	Data-Out
STATIC-COLUMN READ	1st Cycle	L	L	H	ROW	COL	"don't care"	Data-Out
	2nd Cycle	L	L	H	n/a	COL	"don't care"	Data Out
STATIC-COLUMN EARLY-WRITE	1st Cycle	L	L	L	ROW	COL	Data-In	High-Z
	2nd Cycle	L	L	H→L	n/a	COL	Data-In	High-Z
STATIC-COLUMN READ-WRITE	1st Cycle	L	L	H→L	ROW	COL	Data-In	Data-Out
	2nd Cycle	L	L	H→L	n/a	COL	Data-In	Data-Out
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	"don't care"	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	"don't care"	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In	High-Z
CBR REFRESH		H→L	L	H	X	X	"don't care"	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX		UNITS	NOTES
		-7	-8		
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	ICC2	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ᵗRC = ᵗRC [MIN])	ICC3	100	90	mA	3, 4, 25
OPERATING CURRENT: STATIC COLUMN Average power supply current (RAS = VIL, CAS, Address Cycling: ᵗSC = ᵗSC [MIN])	ICC4	70	60	mA	3, 4, 25
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: ᵗRC = ᵗRC [MIN))	ICC5	100	90	mA	3, 25
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: ᵗRC = ᵗRC [MIN])	ICC6	100	90	mA	3, 5

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DRAM

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		ns	
READ WRITE cycle time	^tRWC	155		175		ns	
STATIC-COLUMN READ or WRITE cycle time	^tSC	40		45		ns	
STATIC-COLUMN READ-WRITE cycle time	^tSRWC	70		75		ns	
Access time from $\overline{RAS}$	^tRAC		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20	ns	15
Access time from column-address	^tAA		35		40	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	80		90		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	35		40		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		ns	
Output buffer turn-off delay	^tOFF	3	20	3	20	ns	20, 26
Column-address hold time (referenced to $\overline{RAS}$)	^tAWR	55		60		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5.0V ± 10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{\text{WE}}$ command setup time	^{t}WCS	0		0		ns	21
Write command hold time	^{t}WCH	15		15		ns	
Write command hold time (referenced to $\overline{\text{RAS}}$)	^{t}WCR	55		60		ns	
Write command pulse width	^{t}WP	15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	^{t}RWL	20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	^{t}CWL	20		20		ns	
Data-in setup time	^{t}DS	0		0		ns	22
Data-in hold time	^{t}DH	15		15		ns	22
Data-in hold time (referenced to $\overline{\text{RAS}}$)	^{t}DHR	55		60		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	^{t}RWD	70		80		ns	21
Column-address to $\overline{\text{WE}}$ delay time	^{t}AWD	35		40		ns	21
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	^{t}CWD	20		20		ns	21
Transition time (rise or fall)	^{t}T	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^{t}REF		16		16	ms	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	^{t}RPC	0		0		ns	
$\overline{\text{CAS}}$ setup time (CBR REFRESH)	^{t}CSR	10		10		ns	5
$\overline{\text{CAS}}$ hold time (CBR REFRESH)	^{t}CHR	15		15		ns	5
$\overline{\text{WE}}$ hold time (CBR REFRESH)	^{t}WRH	10		10		ns	24
$\overline{\text{WE}}$ setup time (CBR REFRESH)	^{t}WRP	10		10		ns	24
$\overline{\text{WE}}$ hold time (WCBR test cycle)	^{t}WTH	10		10		ns	24
$\overline{\text{WE}}$ setup time (WCBR test cycle)	^{t}WTS	10		10		ns	24
Write inactive time	^{t}WI	10		10		ns	
Previous WRITE to column-address delay time	^{t}LWAD	20	30	20	35	ns	
Previous WRITE to column-address hold time	^{t}AHLW	65		75		ns	
Output data hold time from column-address	^{t}AOH	5		5		ns	
Output data enable from WRITE	^{t}OW	^{t}AA + 5		^{t}AA + 5		ns	
Access time from last WRITE	^{t}ALW	65		75		ns	
Column-address hold time referenced to $\overline{\text{RAS}}$ HIGH	^{t}AH	5		10		ns	
$\overline{\text{CAS}}$ pulse width in STATIC COLUMN MODE	^{t}CSC	^{t}CAS		^{t}CAS		ns	
Output data hold from WRITE	^{t}WOH	0		0		ns	

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DRAM

NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 5V ±10%;f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If CAS = VIH, data output is High-Z.
12. If CAS = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE WRITE, READ WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE WRITE and the state of data-out is indeterminate (at access time and until CAS goes back to VIH).
22. These parameters are referenced to CAS leading edge in early WRITE cycles and WE leading edge in LATE WRITE or READ WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
24. ^tWTS and ^tWTH are set up and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.
25. Column-address changed once while RAS = VIL to CAS = VIH.
26. The 3ns minimum is a parameter guaranteed by design.

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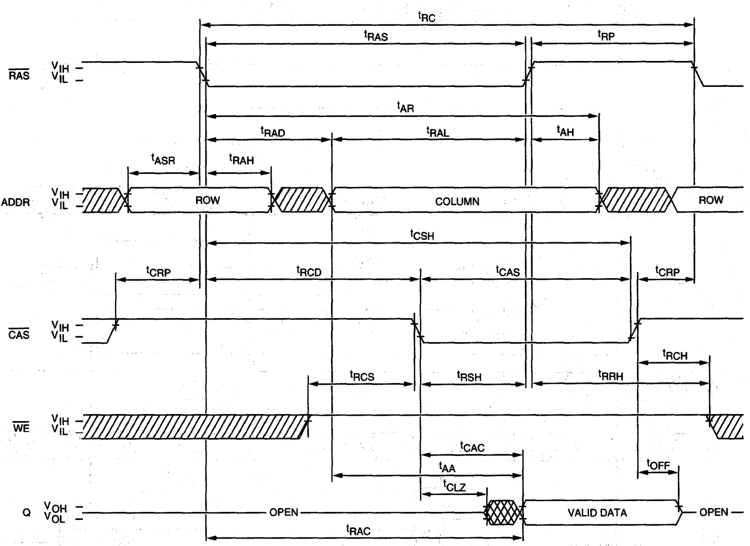
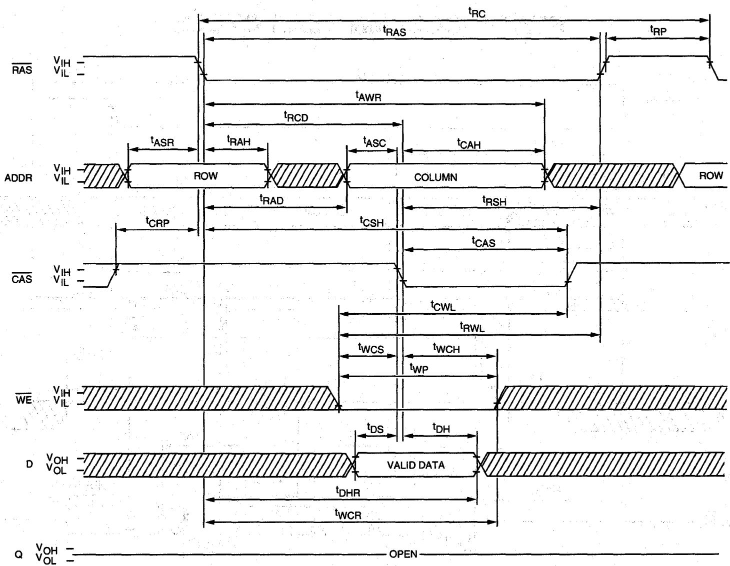
DRAM

READ CYCLE



EARLY WRITE CYCLE



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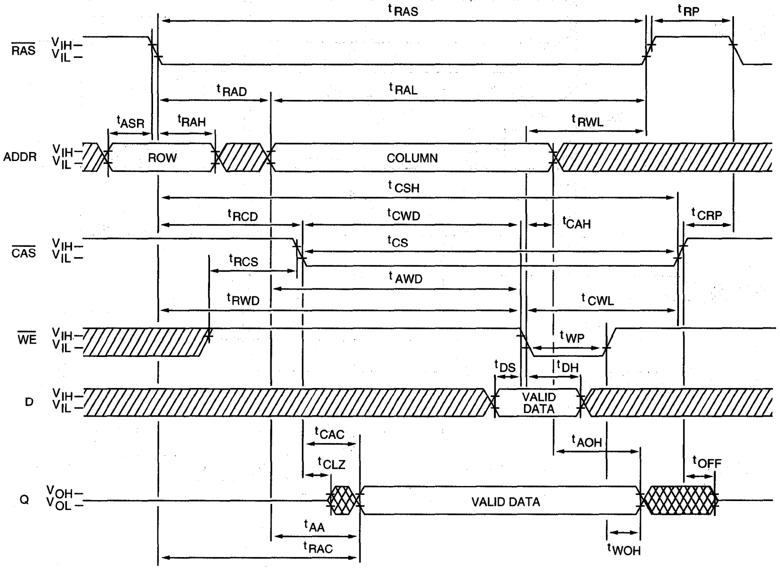
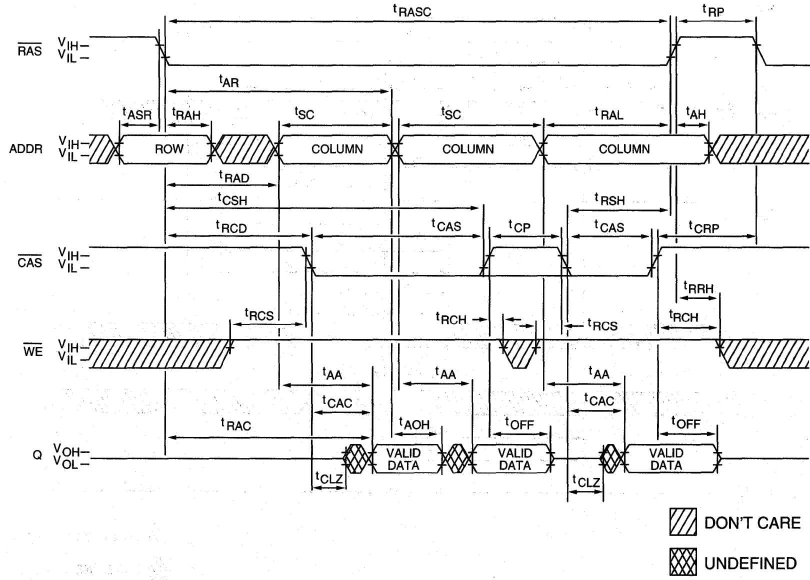
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



STATIC-COLUMN READ CYCLE



DON'T CARE

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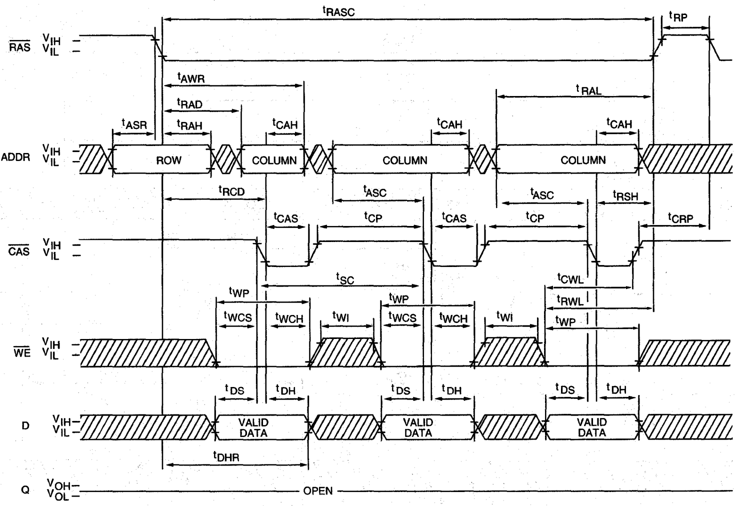
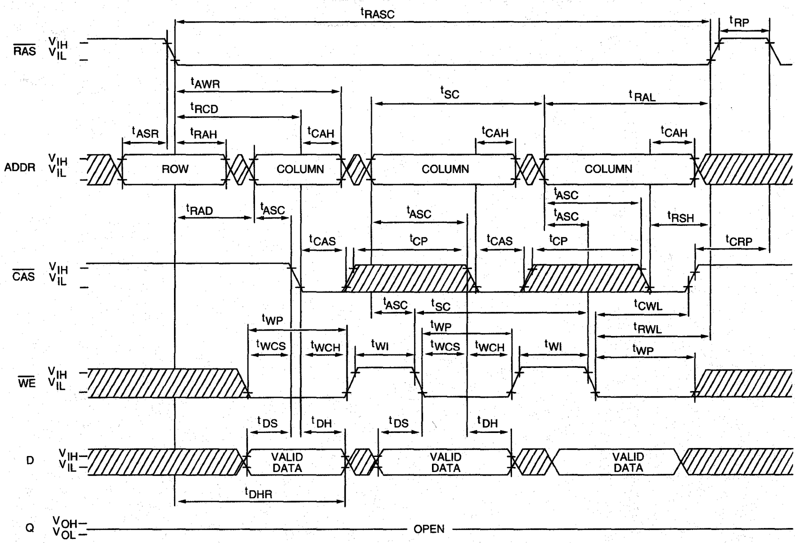
DRAM

STATIC-COLUMN EARLY-WRITE CYCLE
(CAS controlled)



STATIC-COLUMN EARLY-WRITE CYCLE
(WE controlled)



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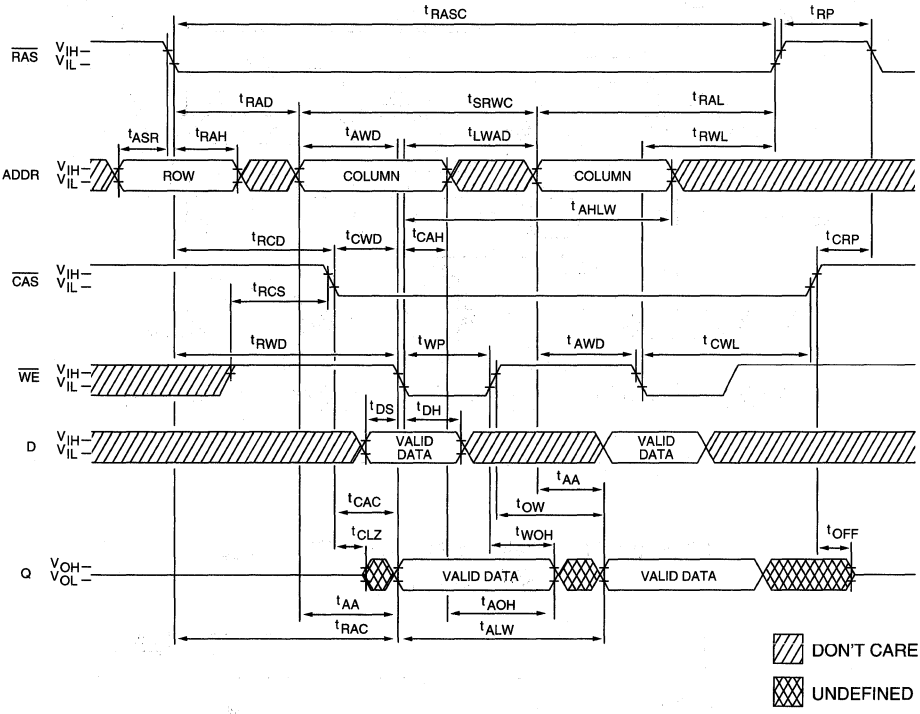
DRAM

STATIC-COLUMN READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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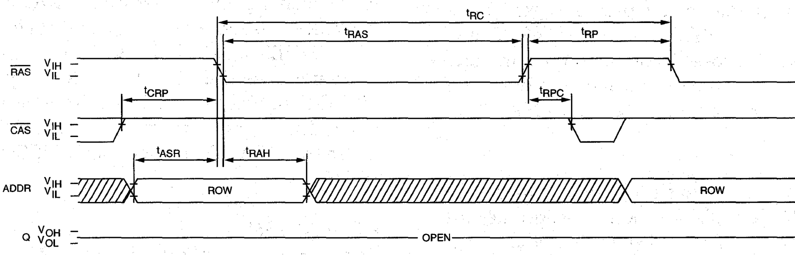
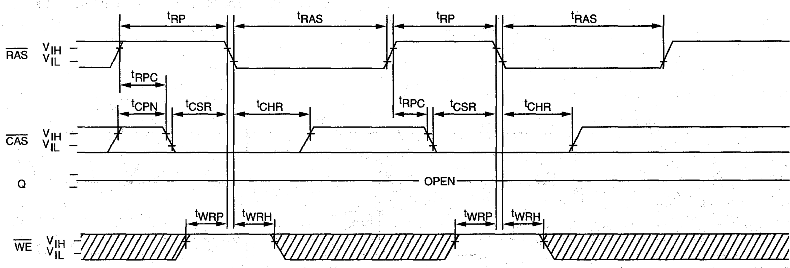
DRAM

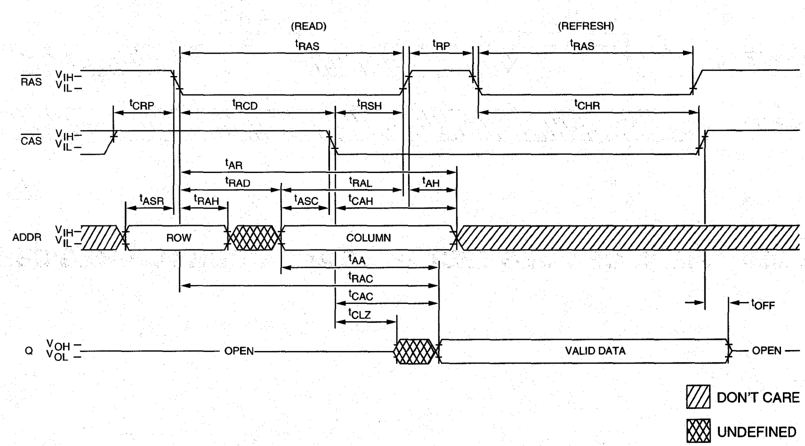
$\overline{RAS}$ ONLY REFRESH CYCLE
(ADDR = A0-A9; A10 and $\overline{WE}$ = DON'T CARE)



CBR REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)



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DRAM

4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh cycle of the 1 Meg is the CBR REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{WE}$ pin held at a voltage HIGH level.

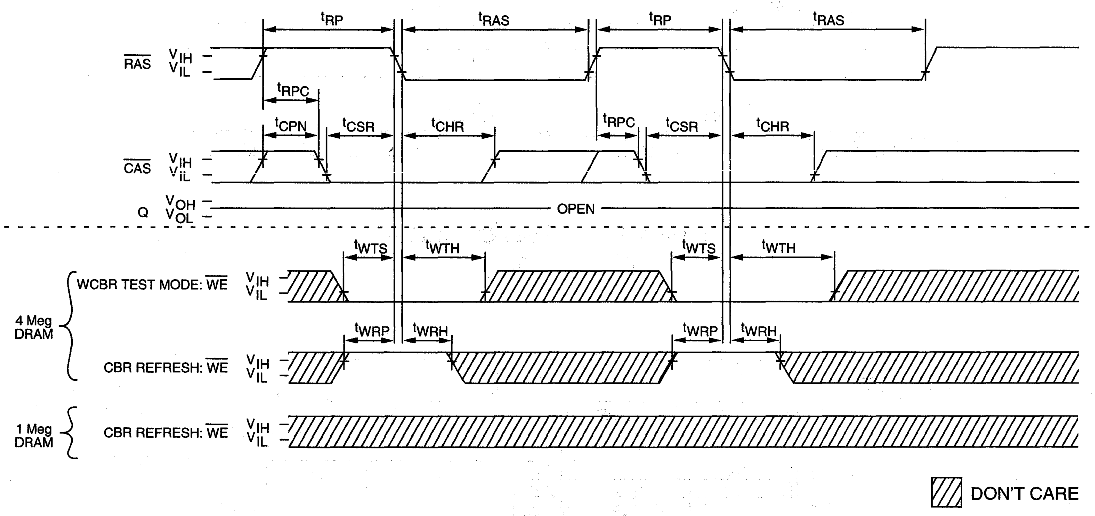
A CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC-specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{RAS}$ ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC-specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$ ONLY or a CBR REFRESH cycle ($\overline{WE}$ held HIGH).

SUMMARY

1. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH.
2. The eight $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$ ONLY or CBR REFRESH cycles ($\overline{WE}$ held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

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16 MEG x 1 DRAM

5.0V FAST PAGE MODE

FEATURES

- Industry-standard x1 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single power supply: +5V ±10%
- Low power, 4mW standby; 200mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (300 mil)	DJ

- Part Number Example: MT4C16M1A1DJ-6

PIN ASSIGNMENT (Top View)

24/26-Pin SOJ
(DC-2)

Signal	Pin	Pin	Signal
Vcc	1	26	Vss
D	2	25	Q
NC	3	24	NC
$\overline{\text{WE}}$	4	23	$\overline{\text{CAS}}$
$\overline{\text{RAS}}$	5	22	NC
A11	6	21	A9
A10	8	19	A8
A0	9	18	A7
A1	10	17	A6
A2	11	16	A5
A3	12	15	A4
Vcc	13	14	Vss

GENERAL DESCRIPTION

The MT4C16M1A1 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x1 configuration. During READ and WRITE cycles, each bit is uniquely addressed through the 24 address bits, which are entered 12 bits (A0-A11) at a time. $\overline{\text{RAS}}$ is used to latch the first 12 bits and $\overline{\text{CAS}}$ the latter 12 bits. READ and WRITE cycles are selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin remains open (High-Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after data reaches the output pin, data-out (Q) is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A11) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{\text{RAS}}$ followed by a column-address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE) or $\overline{\text{RAS}}$ REFRESH cycle ($\overline{\text{RAS}}$ ONLY, CBR, or HIDDEN) so that all 4,096 combinations of $\overline{\text{RAS}}$ addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{\text{RAS}}$ addressing.

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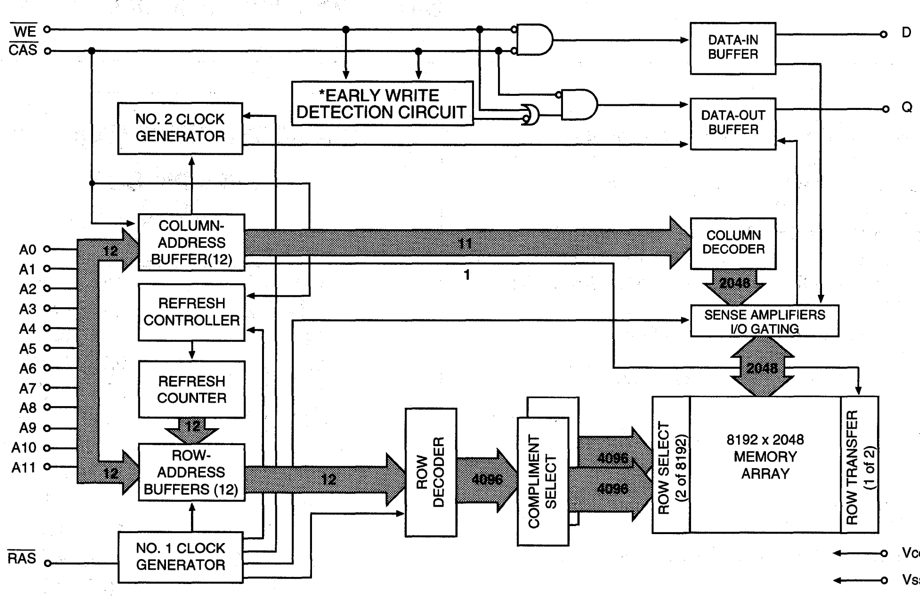
FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



***NOTE:** 1. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{\text{CAS}}$ goes LOW prior to $\overline{\text{WE}}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDRESSES ^{t}R	ADDRESSES ^{t}C	DATA D (Data-In)	DATA Q (Data-Out)
Standby		H	H→X	X	X	X	“don’t care”	High-Z
READ		L	L	H	ROW	COL	“don’t care”	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In	High-Z
READ WRITE		L	L	H→L	ROW	COL	Data-In	Data-Out
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	“don’t care”	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	“don’t care”	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In	High-Z
	2nd Cycle	L	H→L	L	n/a	COL	Data-In	High-Z
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Data-In	Data-Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Data-In	Data-Out
$\overline{\text{RAS}}$ ONLY REFRESH		L	H	X	ROW	n/a	“don’t care”	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	“don’t care”	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In	High-Z
CBR REFRESH		H→L	L	H	X	X	“don’t care”	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss (5V) .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

		MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	ICC2	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	90	80	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])	ICC4	70	60	mA	3, 4, 26
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])	ICC5	90	80	mA	3, 26
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC6	90	80	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A11, D	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}	7	pF	2
Output Capacitance: Q	C_O	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	
READ WRITE cycle time	^tRWC	130		155		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	60		70		ns	
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15
Access time from column-address	^tAA		30		35	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	25
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 25
$\overline{WE}$ command setup time	^tWCS	0		0		ns	21

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^{t}WCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	45		55		ns	
Write command pulse width	^{t}WP	10		15		ns	
Write command to $\overline{RAS}$ lead time	^{t}RWL	15		20		ns	
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		ns	
Data-in setup time	^{t}DS	0		0		ns	22
Data-in hold time	^{t}DH	10		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	60		70		ns	21
Column-address to $\overline{WE}$ delay time	^{t}AWD	30		35		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	15		20		ns	21
Transition time (rise or fall)	^{t}T	3	50	3	50	ns	9, 10
Refresh period (4,096 cycles)	^{t}REF		64		64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	5		5		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	15		15		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^{t}WTH	10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^{t}WTS	10		10		ns	24

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 5V ±10%; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ᵗREF refresh requirement is exceeded.
8. AC characteristics assume ᵗT = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If CAS = VIH, data output is High-Z.
12. If CAS = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ᵗRCD < ᵗRCD (MAX). If ᵗRCD is greater than the maximum recommended value shown in this table, ᵗRAC will increase by the amount that ᵗRCD exceeds the value shown.
15. Assumes that ᵗRCD ≥ ᵗRCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ᵗCPN.
17. Operation within the ᵗRCD (MAX) limit ensures that ᵗRAC (MAX) can be met. ᵗRCD (MAX) is specified as a reference point only; if ᵗRCD is greater than the specified ᵗRCD (MAX) limit, then access time is controlled exclusively by ᵗCAC.
18. Operation within the ᵗRAD (MAX) limit ensures that ᵗRAC (MIN) and ᵗCAC (MIN) can be met. ᵗRAD (MAX) is specified as a reference point only; if ᵗRAD is greater than the specified ᵗRAD (MAX) limit, then access time is controlled exclusively by ᵗAA.
19. Either ᵗRCH or ᵗRRH must be satisfied for a READ cycle.
20. ᵗOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
21. ᵗWCS, ᵗRWD, ᵗAWD and ᵗCWD are restrictive operating parameters in LATE WRITE, READ WRITE and READ-MODIFY-WRITE cycles only. If ᵗWCS ≥ ᵗWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ᵗRWD ≥ ᵗRWD (MIN), ᵗAWD ≥ ᵗAWD (MIN) and ᵗCWD ≥ ᵗCWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE WRITE and the state of data-out is indeterminate (at access time and until CAS goes back to VIH).
22. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
24. ᵗWTS and ᵗWTH are set up and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ᵗWRP and ᵗWRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.

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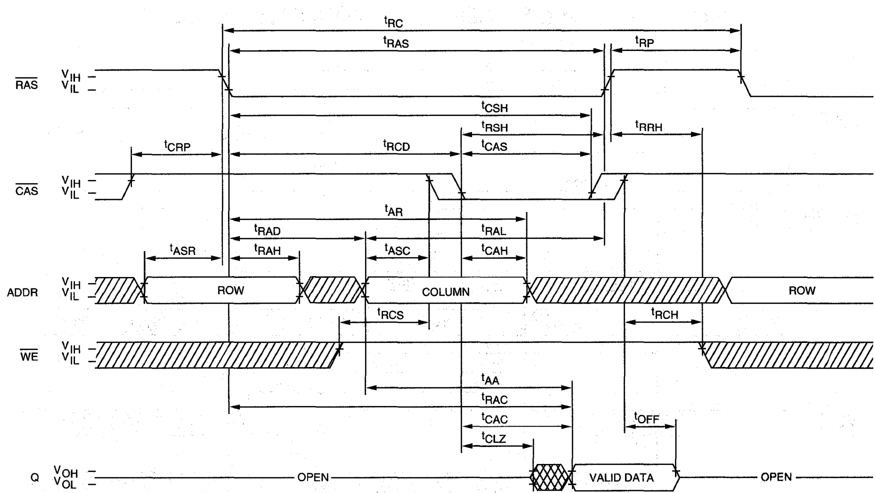
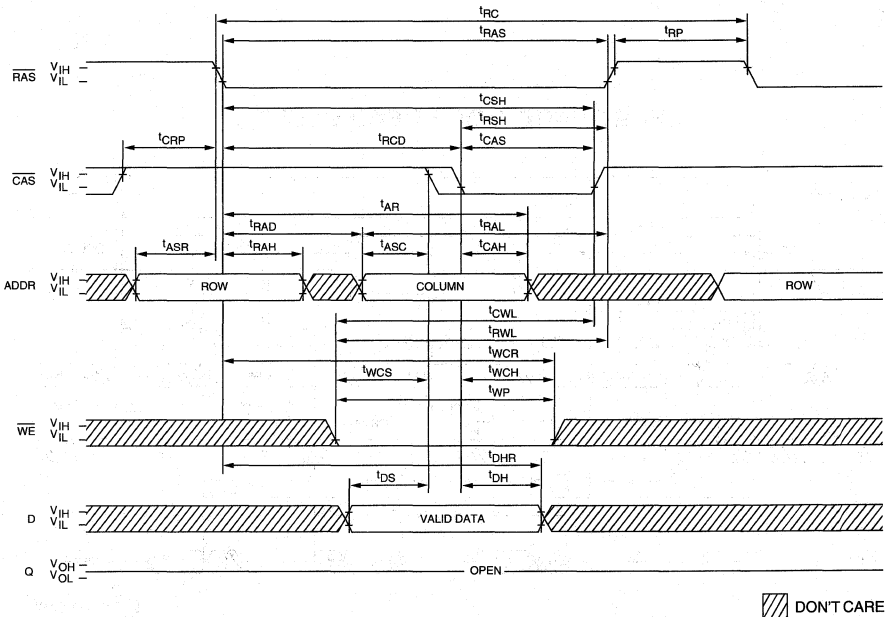
READ CYCLE



EARLY WRITE CYCLE



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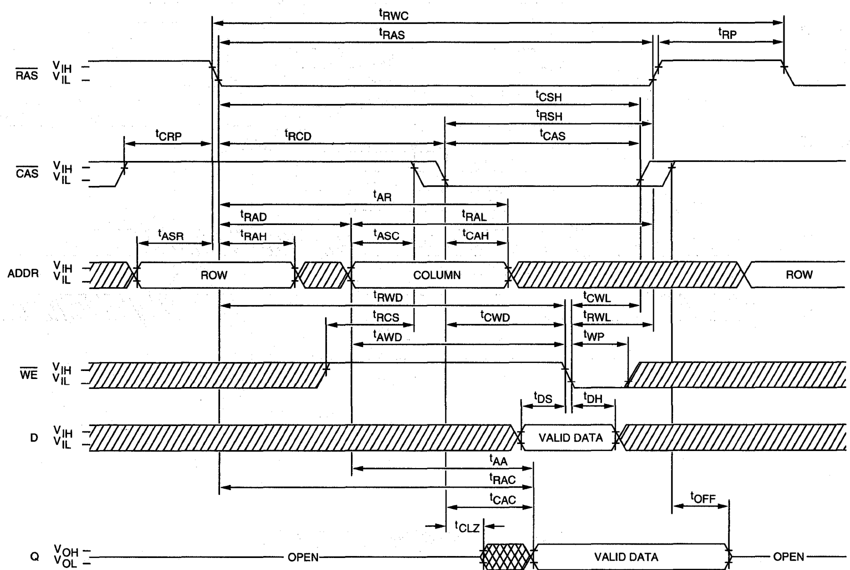
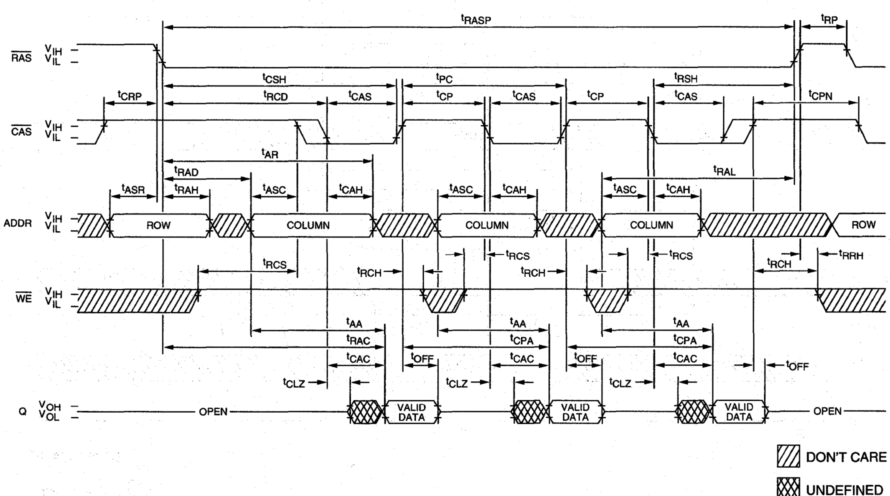
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



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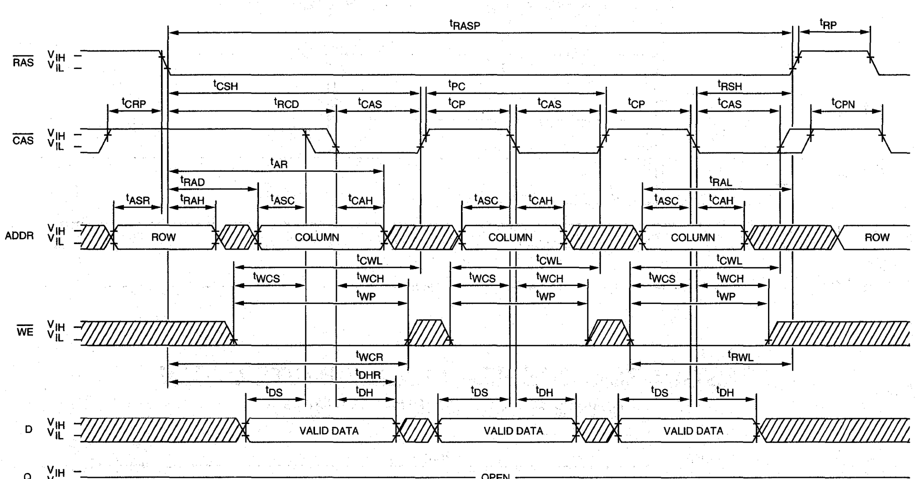
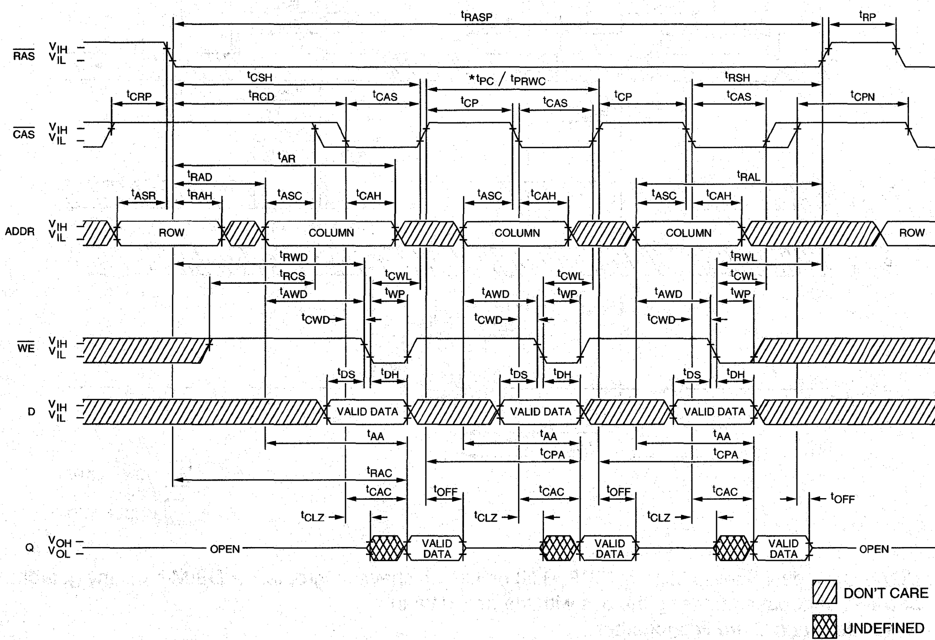
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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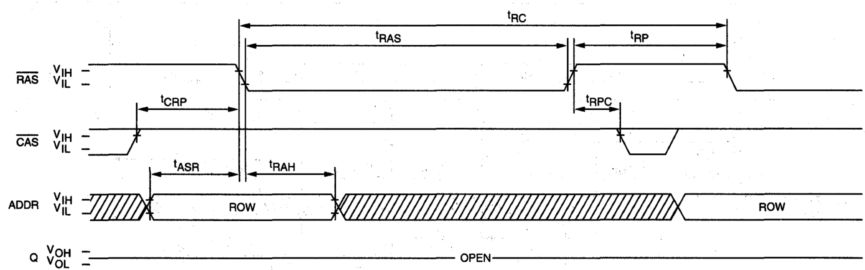
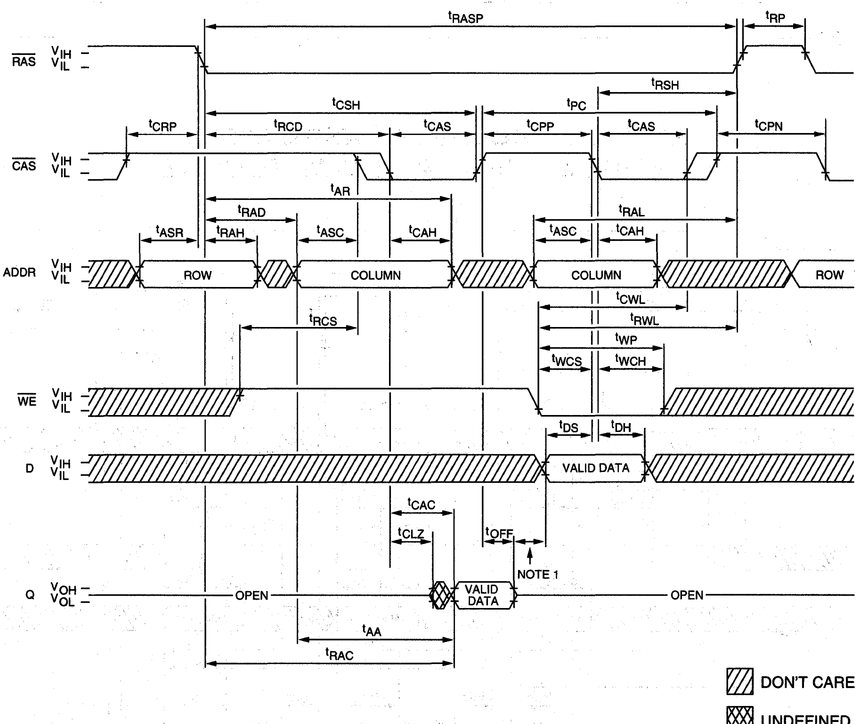
RAS ONLY REFRESH CYCLE
(ADDR = A0-A11; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE:
1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

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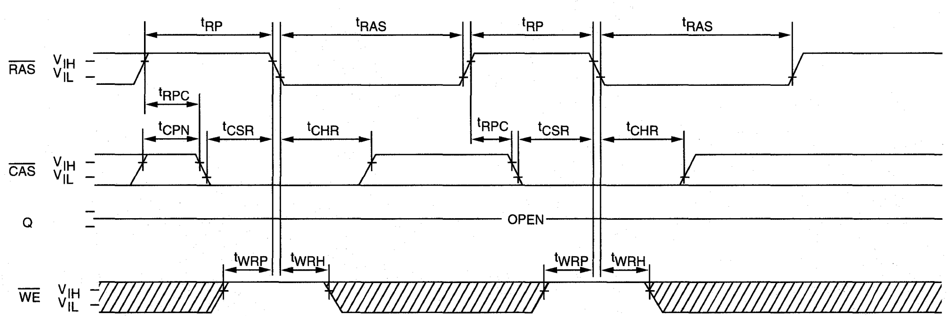
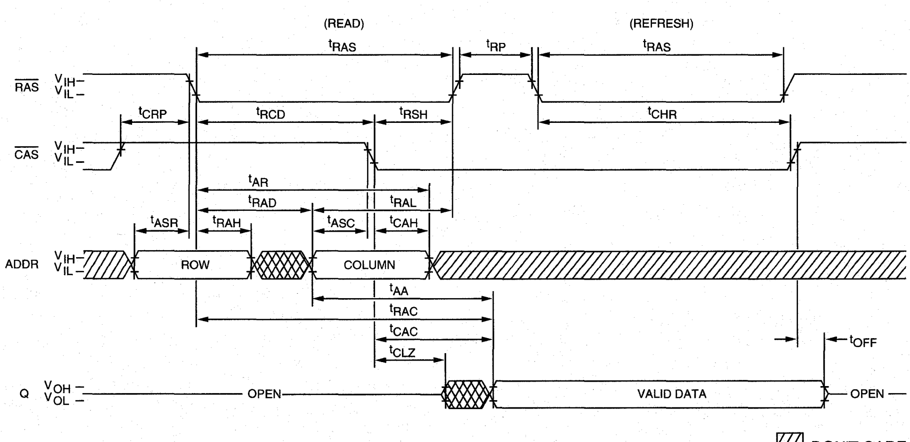
CBR REFRESH CYCLE

(A0-A11 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]

($\overline{WE}$ = HIGH)



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DRAM

256K x 4 DRAM

STANDARD OR LOW POWER, EXTENDED REFRESH

FEATURES

- 512-cycle refresh in 8ms (MT4C4256) or 64ms (MT4C4256 L)
- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 0.8mW standby; 175mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR), HIDDEN and Extended (MT4C4256 L only)
- Low CMOS Standby Current, 200µA maximum (MT4C4256 L)

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns acces	-7
80ns access	-8
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic ZIP (350 mil)	Z
• Version	
512-cycle refresh in 8 ms	None
512-cycle refresh in 64 ms	L

- Part Number Example: MT4C4256DJ-7 L

PIN ASSIGNMENT (Top View)

20-Pin DIP (DA-2)

Pin	Name	Pin	Name
1	DQ1	20	Vss
2	DQ2	19	DQ4
3	$\overline{\text{WE}}$	18	DQ3
4	$\overline{\text{RAS}}$	17	$\overline{\text{CAS}}$
5	NC	16	$\overline{\text{OE}}$
6	A0	15	A8
7	A1	14	A7
8	A2	13	A6
9	A3	12	A5
10	Vcc	11	A4

20-Pin ZIP (DB-1)

Pin	Name	Pin	Name
1	$\overline{\text{OE}}$	2	$\overline{\text{CAS}}$
3	DQ3	4	DQ4
5	Vss	6	DQ1
7	DQ2	8	$\overline{\text{WE}}$
9	$\overline{\text{RAS}}$	10	NC
11	A0	12	A1
13	A2	14	A3
15	Vcc	16	A4
17	A5	18	A6
19	A7	20	A8

20/26-Pin SOJ (DC-1)

Pin	Name	Pin	Name
1	DQ1	26	Vss
2	DQ2	25	DQ4
3	$\overline{\text{WE}}$	24	DQ3
4	$\overline{\text{RAS}}$	23	$\overline{\text{CAS}}$
5	NC	22	$\overline{\text{OE}}$
9	A0	18	A8
10	A1	17	A7
11	A2	16	A6
12	A3	15	A5
13	Vcc	14	A4

GENERAL DESCRIPTION

The MT4C4256(L) is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{\text{RAS}}$ is used to latch the first 9 bits and $\overline{\text{CAS}}$ the latter 9 bits. READ and WRITE cycles are selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after data reaches the output pin, data-out (Q) is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by $\overline{\text{WE}}$ and $\overline{\text{OE}}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{\text{RAS}}$ followed by a column-address strobed-

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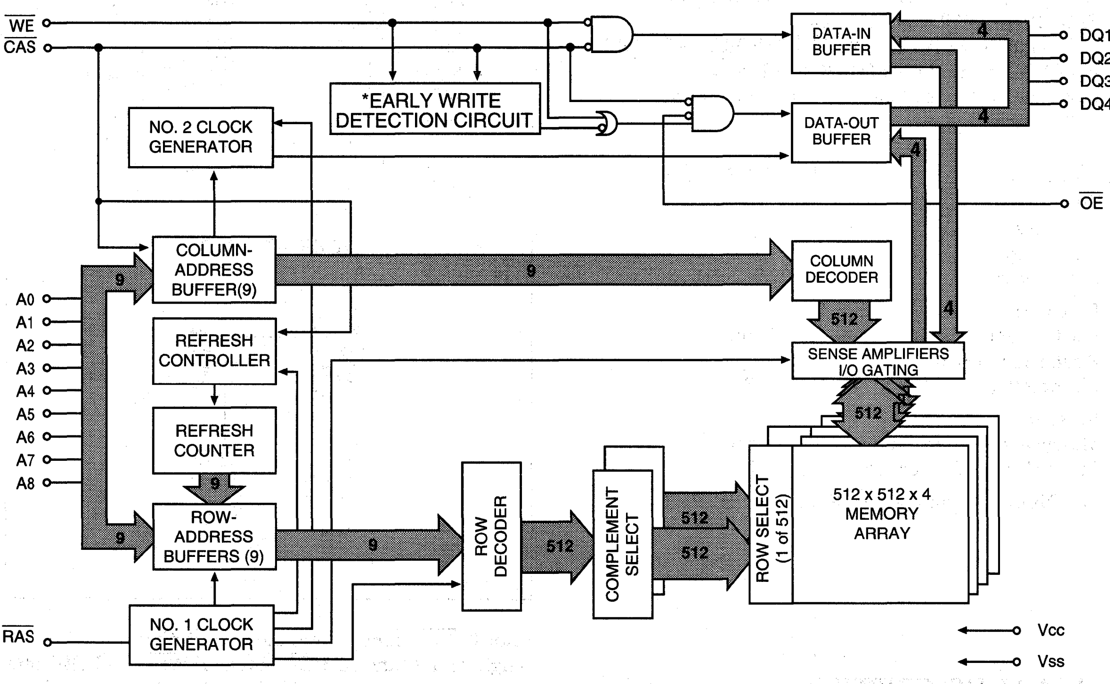
in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms for the MT4C4256 and every 64ms for the MT4C4256 L, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	X	X	X	X	High-Z
Extended Refresh (MT4C4256 L only)		H→L	L	X	X	X	X	High-Z

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DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT: (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

PARAMETER/CONDITION	VERSION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)		ICC1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	MT4C4256	ICC2	1	1	1	mA	
	MT4C4256 L	ICC2	200	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Single Address Cycling: tRC = tRC [MIN])		ICC3	90	80	70	mA	3, 4, 29
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])		ICC4	70	60	50	mA	3, 4, 29
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])		ICC5	90	80	70	mA	3, 29
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])		ICC6	90	80	70	mA	3, 5
REFRESH CURRENT: Extended Average power supply current during Extended Refresh: CAS = 0.2V or CBR cycling; RAS = tRAS (MIN) to1µs; WE, A0-A8 and DIN = Vcc -0.2V or 0.2V (DIN may be left open); tRC = 125µs (512 rows at 125µs = 64ms)	MT4C4256 L	ICC7	200	200	200	µA	3, 5, 27

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ WRITE cycle time	tRWC	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	90		95		100		ns	
Access time from RAS	tRAC		60		70		80	ns	14
Access time from CAS	tCAC		20		20		20	ns	15
Output Enable	tOE		20		20		20	ns	
Access time from column-address	tAA		30		35		40	ns	
Access time from CAS precharge	tCPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	tCAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	tCPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	17
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row-address setup time	tASR	0		0		0		ns	
Row-address hold time	tRAH	10		10		10		ns	
RAS to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		0		ns	
Column-address hold time	tCAH	15		15		15		ns	
Column-address hold time (referenced to RAS)	tAR	45		55		60		ns	
Column-address to RAS lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	tRCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	19
CAS to output in Low-Z	tCLZ	0		0		0		ns	

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DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	tOFF	3	20	3	20	3	20	ns	20, 26, 28
Output disable	tOD		15		20		20	ns	26
WE command setup time	tWCS	0		0		0		ns	21
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	20		20		20		ns	
Write command to CAS lead time	tCWL	20		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	15		15		15		ns	22
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
RAS to WE delay time	tRWD	85		100		110		ns	21
Column-address to WE delay time	tAWD	60		65		70		ns	21
CAS to WE delay time	tCWD	40		50		55		ns	21
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles) MT4C4256 / MT4C4256 L	tREF		8 / 64		8 / 64		8 / 64	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CBR REFRESH)	tCSR	10		10		10		ns	5
CAS hold time (CBR REFRESH)	tCHR	10		15		15		ns	5
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		20		20		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		0		ns	24

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%;f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle, and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE cycle, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
26. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
27. Extended refresh current is reduced as ^{t}RAS is reduced from its maximum specification during the extended refresh cycle.
28. The 3ns minimum is a parameter guaranteed by design.
29. Column-address changed once each cycle.

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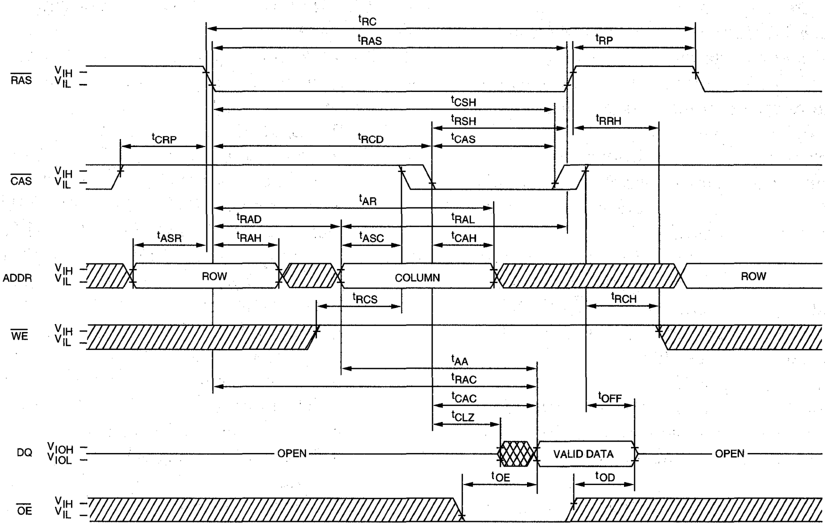
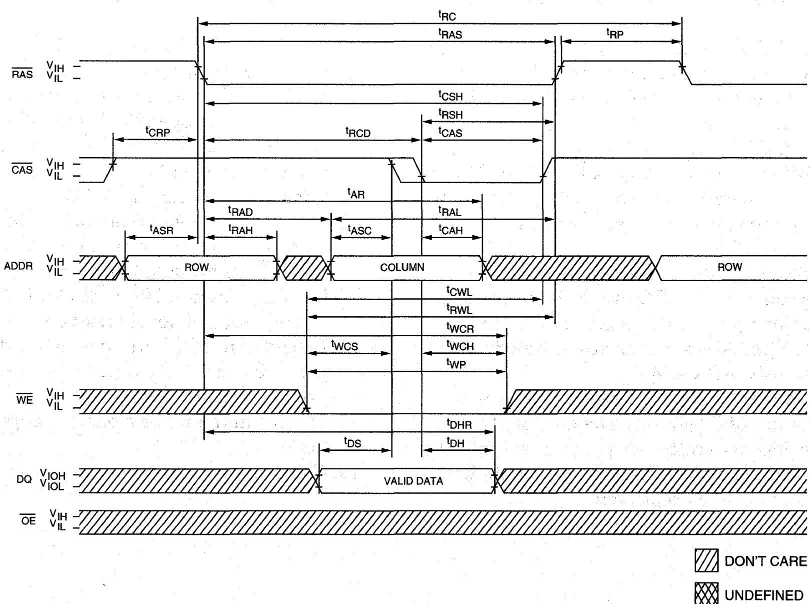
READ CYCLE



EARLY WRITE CYCLE



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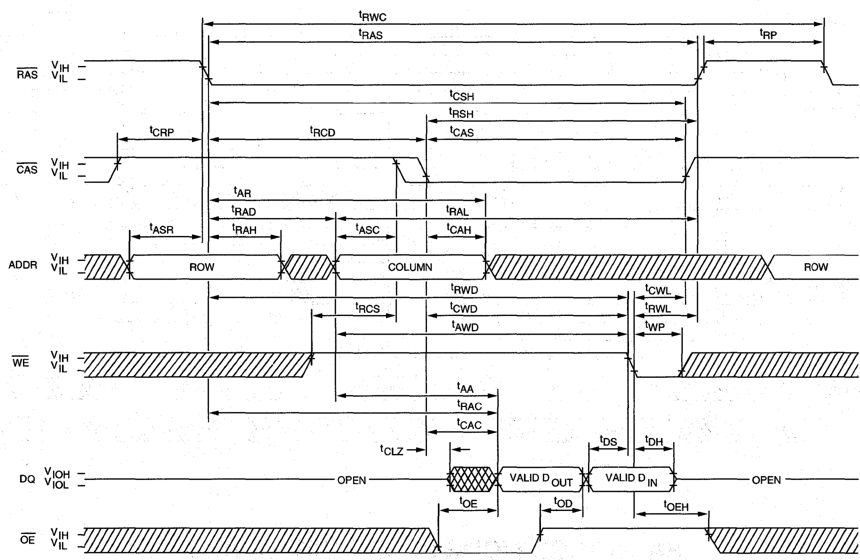
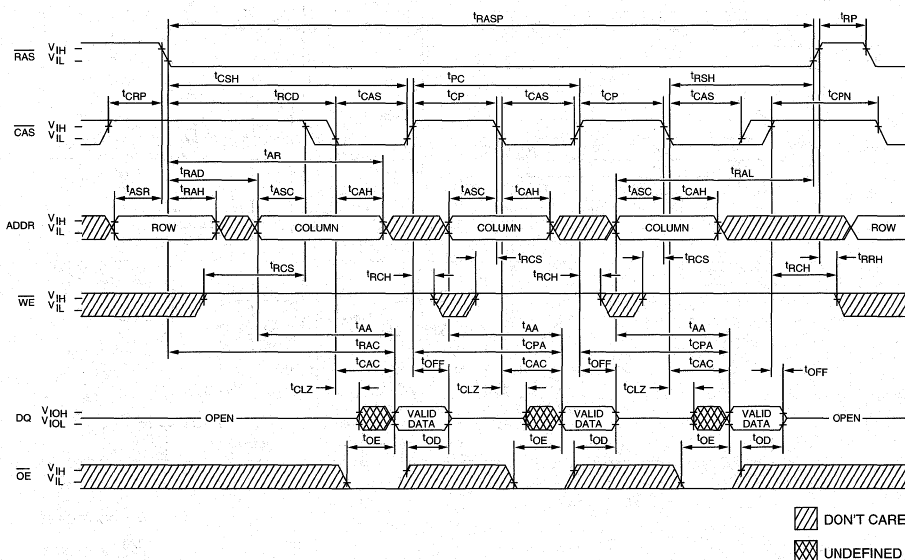
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

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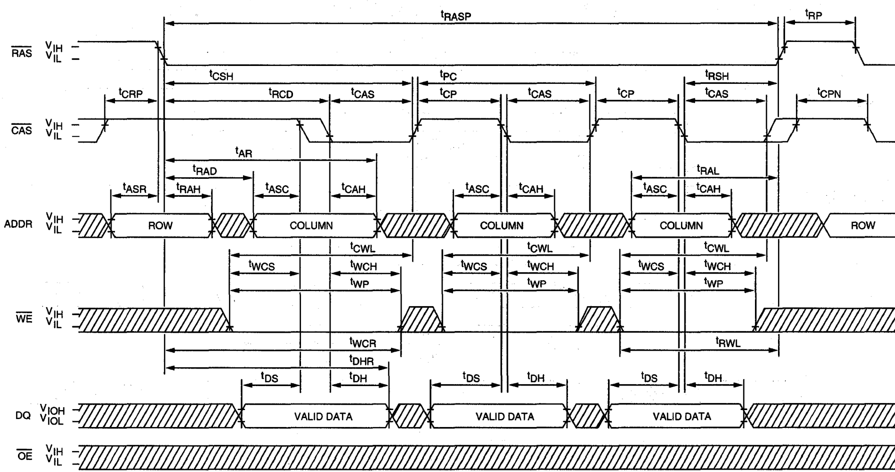
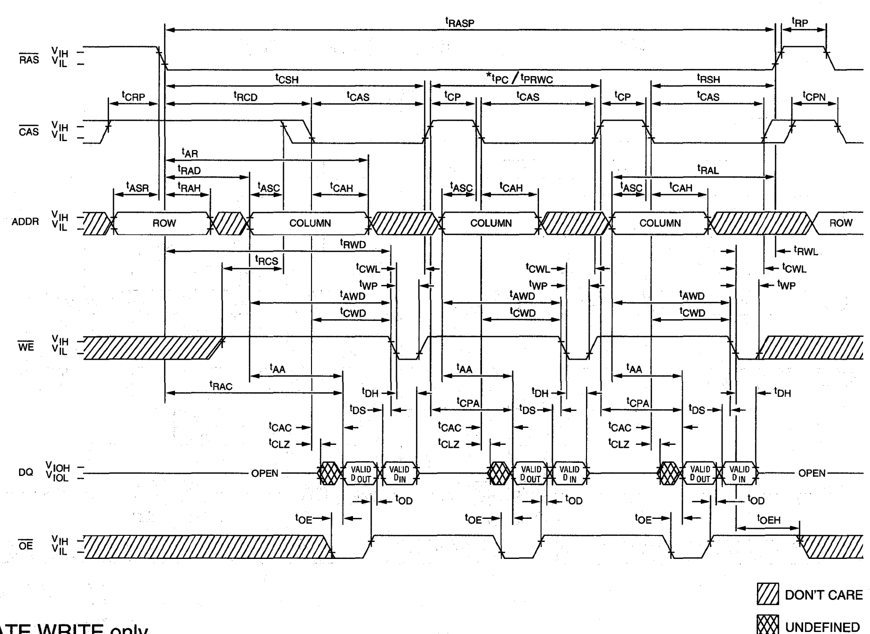
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



*tPC is for LATE WRITE only.

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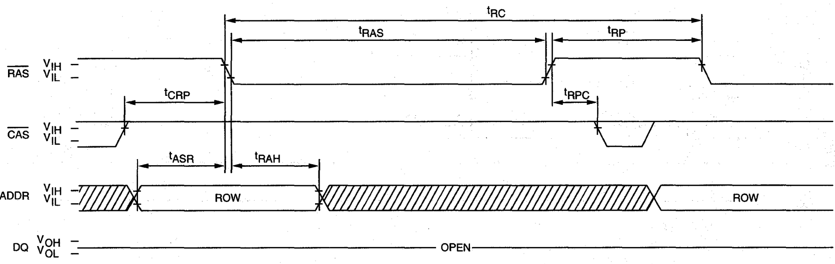
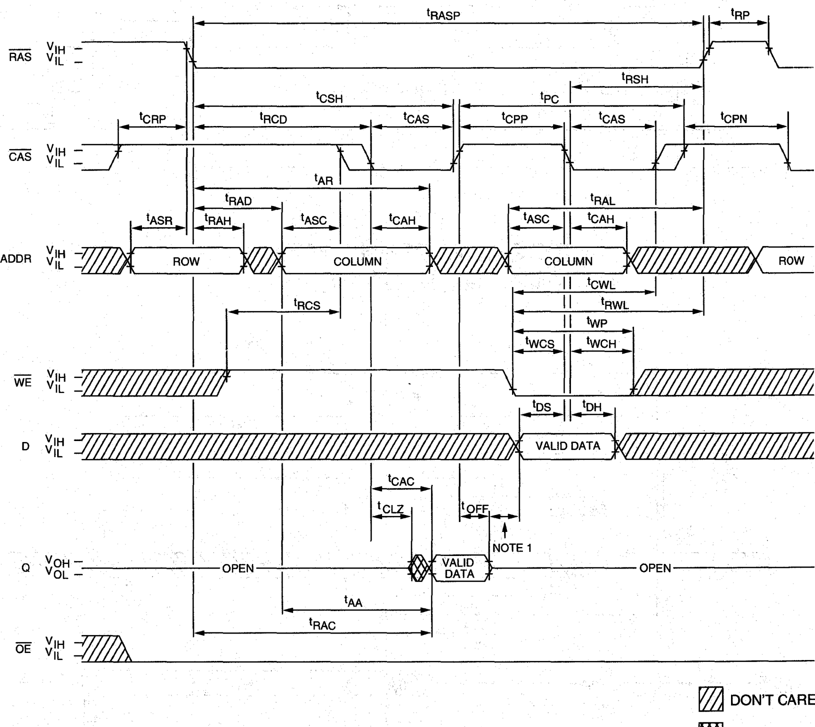
DRAM

$\overline{RAS}$ ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{WE}$ = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: ^{t}CPP(MIN) or ^{t}CP(whichever is greater) + ^{t}DS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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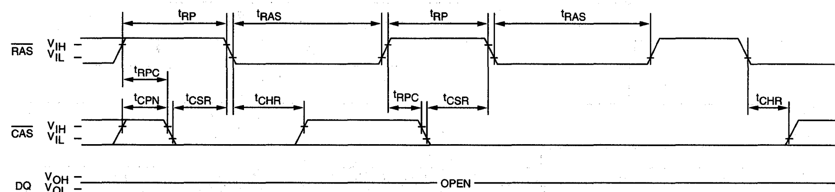
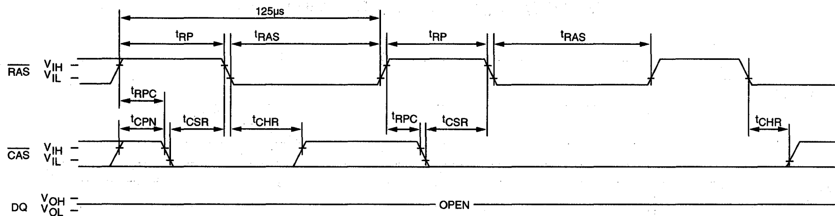
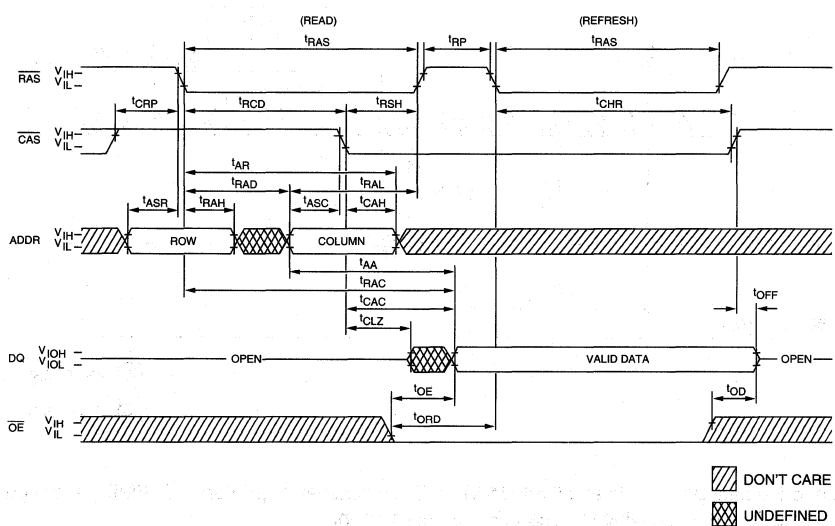
CBR REFRESH CYCLE
(A0-A8, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



EXTENDED REFRESH CYCLE (MT4C4256 L ONLY)
(A0-A8, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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DRAM

256K x 4 DRAM

STATIC COLUMN

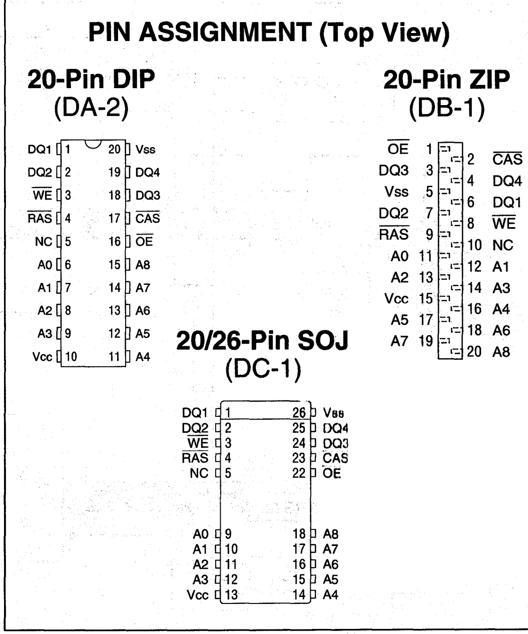
FEATURES

- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- 512-cycle refresh in 8ms
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- STATIC COLUMN access cycle

OPTIONS — MARKING

OPTIONS	MARKING
Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic ZIP (350 mil)	Z

- Part Number Example: MT4C4258DJ-7



GENERAL DESCRIPTION

The MT4C4258 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin(s), data-out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by WE and OE.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. After the first read, any column-address transition will result in new data-out. Unlike PAGE MODE, which requires CAS to be toggled for each successive PAGE MODE access, STATIC COLUMN allows CAS to be left LOW for successive STATIC COLUMN accesses. Returning RAS HIGH terminates the STATIC COLUMN operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR, or HIDDEN) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

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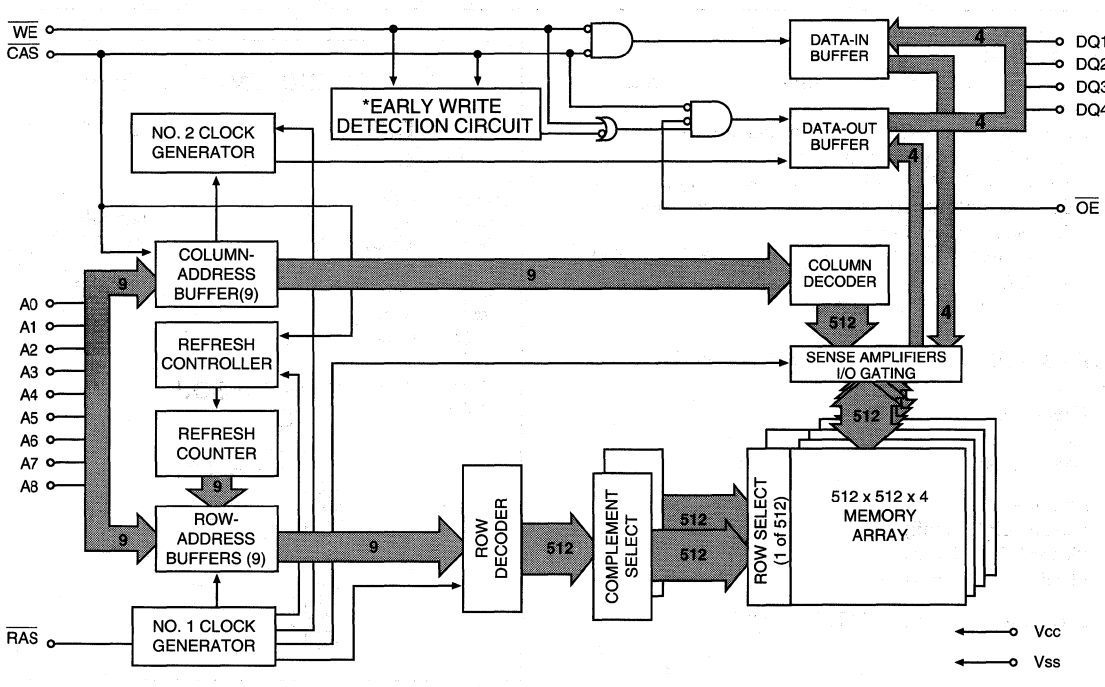
DRAM

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DATA-IN/OUT
						^tR	^tC	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
STATIC-COLUMN READ	1st Cycle	L	L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	L	H	L	n/a	COL	Data-Out
STATIC-COLUMN EARLY-WRITE	1st Cycle	L	L	L	X	ROW	COL	Data-In
	2nd Cycle	L	L	H→L	X	n/a	COL	Data-In
STATIC-COLUMN READ-WRITE	1st Cycle	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	X	X	X	X	High-Z

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DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	MAX -10	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	ICC2	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	80	70	60	mA	3, 4
OPERATING CURRENT: STATIC COLUMN Average power supply current (RAS = VIL, CAS, Address Cycling: tSC = tSC [MIN])	ICC4	60	50	40	mA	3, 4
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])	ICC5	80	70	60	mA	3
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC6	80	70	60	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	130		150		180		ns	
READ WRITE cycle time	^{t}RWC	185		205		245		ns	
STATIC-COLUMN READ or WRITE cycle time	^{t}SC	40		45		55		ns	
STATIC-COLUMN READ-WRITE cycle time	^{t}SRWC	100		110		135		ns	
Access time from $\overline{RAS}$	^{t}RAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^{t}CAC		20		20		25	ns	15
Output Enable	^{t}OE		20		20		25	ns	
Access time from column-address	^{t}AA		35		40		50	ns	
$\overline{RAS}$ pulse width	^{t}RAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	^{t}RASC	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^{t}RSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^{t}RP	50		60		70		ns	
$\overline{CAS}$ pulse width	^{t}CAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	^{t}CSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^{t}CPN	10		10		15		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	^{t}CP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	5		5		5		ns	
Row-address setup time	^{t}ASR	0		0		0		ns	
Row-address hold time	^{t}RAH	10		10		15		ns	
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	35	15	40	20	50	ns	18
Column-address setup time	^{t}ASC	0		0		0		ns	
Column-address hold time	^{t}CAH	15		15		20		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	80		90		100		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	35		40		50		ns	
Read command setup time	^{t}RCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	0		0		0		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	tOFF	3	20	3	20	3	20	ns	20, 26, 27
Output disable	tOD		20		20		20	ns	26
Column-address hold time EARLY WRITE (referenced to RAS)	tAWR		55		60		70	ns	
WE command setup time	tWCS	0		0		0		ns	21
Write command hold time	tWCH	15		15		20		ns	
Write command hold time (referenced to RAS)	tWCR	55		60		75		ns	
Write command pulse width	tWP	15		15		20		ns	
Write command to RAS lead time	tRWL	20		20		25		ns	
Write command to CAS lead time	tCWL	20		20		25		ns	
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	15		15		20		ns	22
Data-in hold time (referenced to RAS)	tDHR	55		60		75		ns	
RAS to WE delay time	tRWD	100		110		130		ns	21
Column-address to WE delay time	tAWD	65		70		80		ns	21
CAS to WE delay time	tCWD	50		55		60		ns	21
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	tREF		8		8		8	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CBR REFRESH)	tCSR	10		10		10		ns	5
CAS hold time (CBR REFRESH)	tCHR	15		15		15		ns	5
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	20		20		20		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		0		ns	24
Write inactive time	tWI	10		10		10		ns	
Previous WRITE to column-address delay time	tLWAD	20	30	20	35	25	45	ns	
Previous WRITE to column-address hold time	tAHLW	65		75		95		ns	
RAS hold time referenced to OE	tROH	10		10		10		ns	
Output data hold time from column-address	tAOH	5		5		5		ns	
Output data enable from WRITE	tOW	tAA + 5		tAA + 5		tAA + 5		ns	
Access time from last WRITE	tALW	65		75		95		ns	
Column-address hold time referenced to RAS HIGH	tAH	5		5		10		ns	
CAS pulse width in STATIC COLUMN MODE	tCSC	tCAS		tCAS		tCAS		ns	

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DRAM

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY WRITE cycles. ^tRWD, ^tAWD and ^tCWD apply to READ-MODIFY-WRITE cycles. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
26. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
27. The 3ns minimum is a parameter guaranteed by design.

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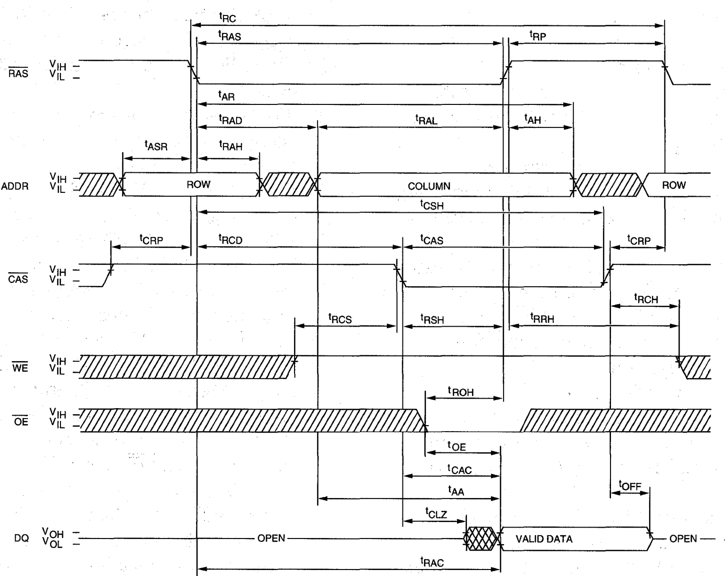
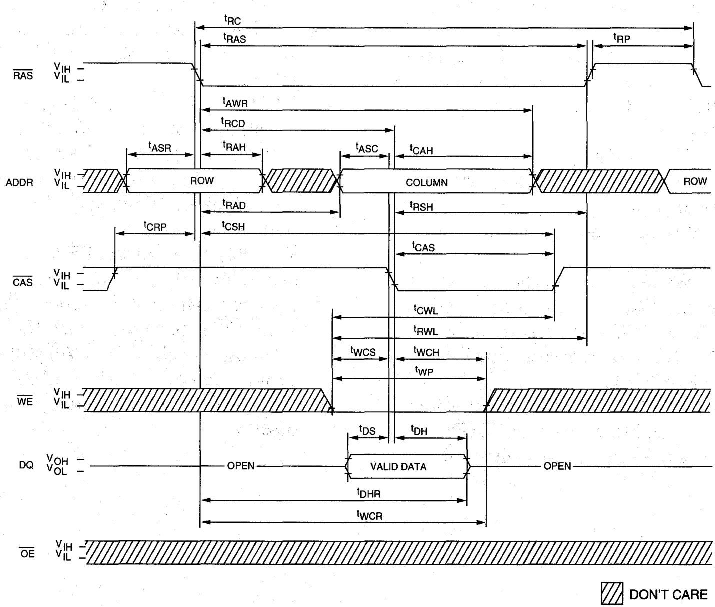
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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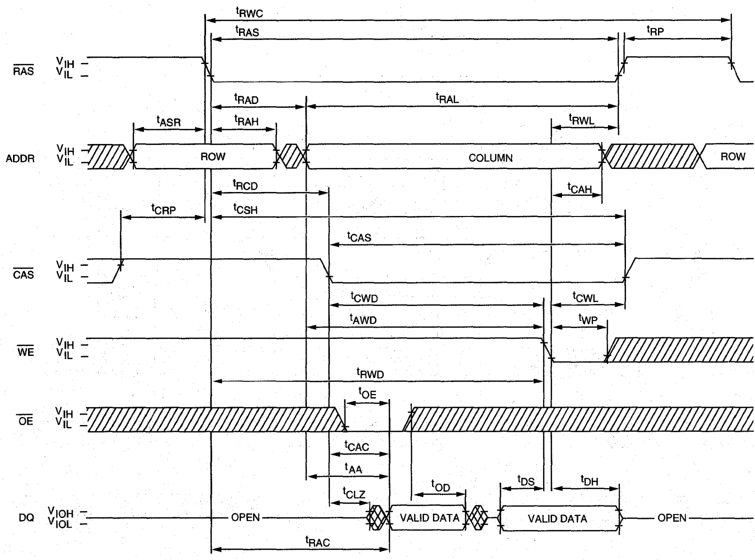
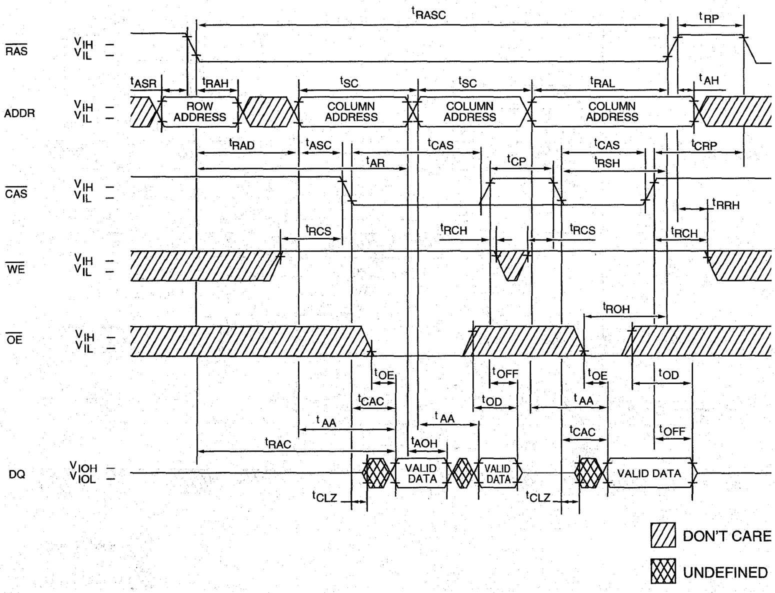
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



STATIC-COLUMN READ CYCLE



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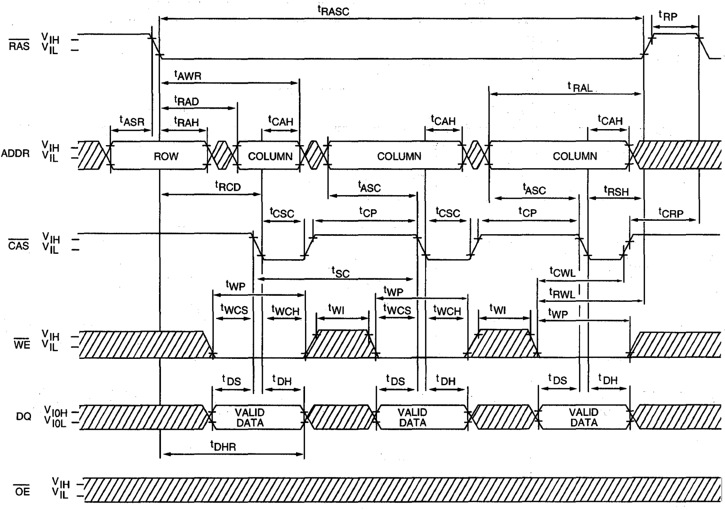
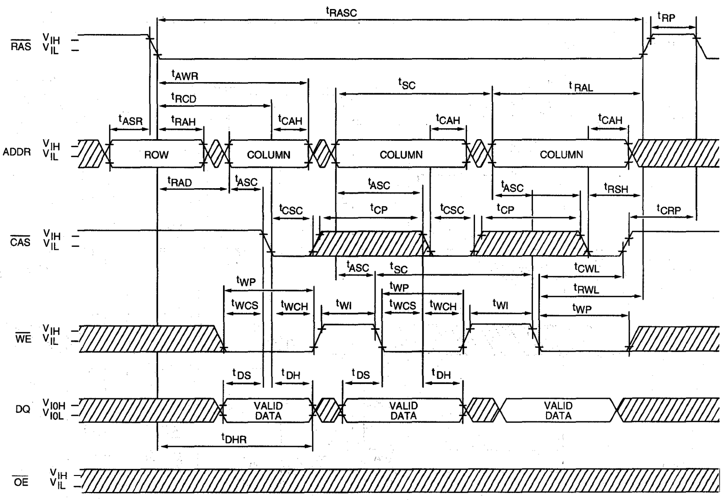
STATIC-COLUMN EARLY-WRITE CYCLE
(CAS controlled)



STATIC-COLUMN EARLY-WRITE CYCLE
(WE controlled)



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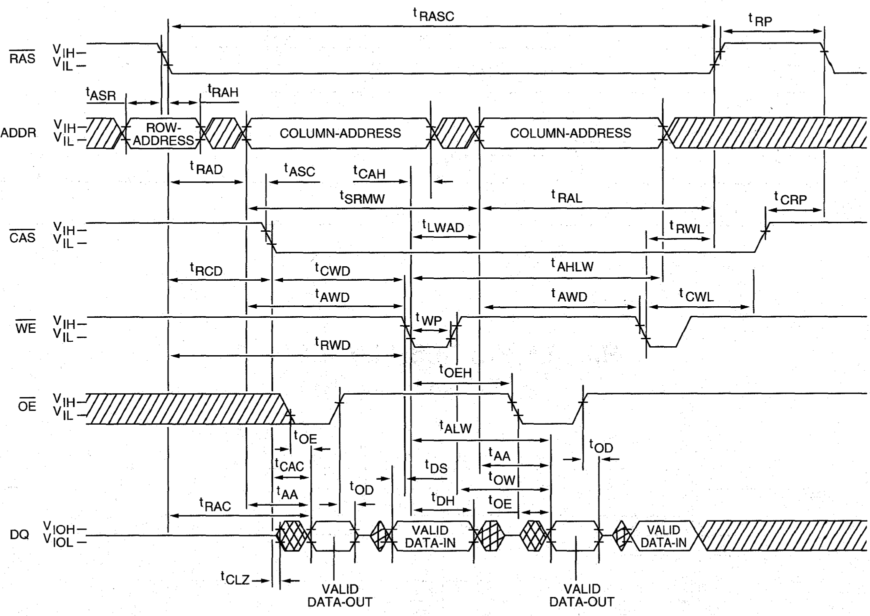
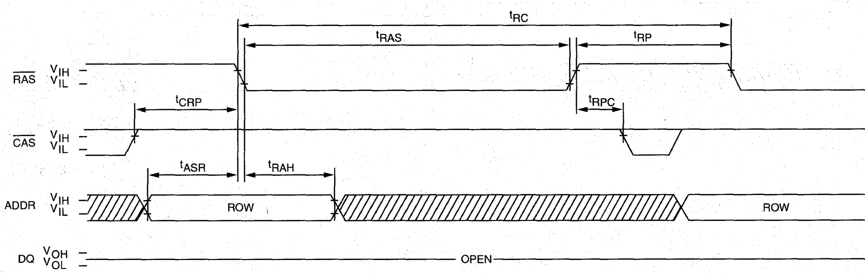
STATIC-COLUMN READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



RAS ONLY REFRESH CYCLE
(ADDR = A0-A8; WE = DON'T CARE)



DON'T CARE

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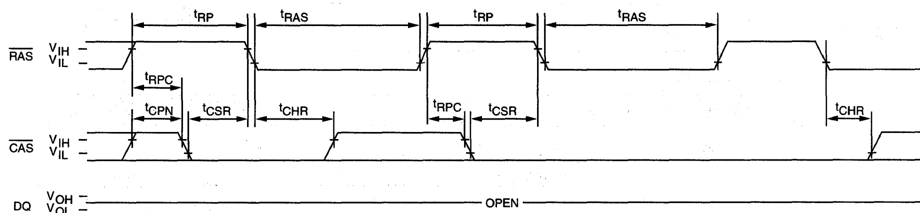
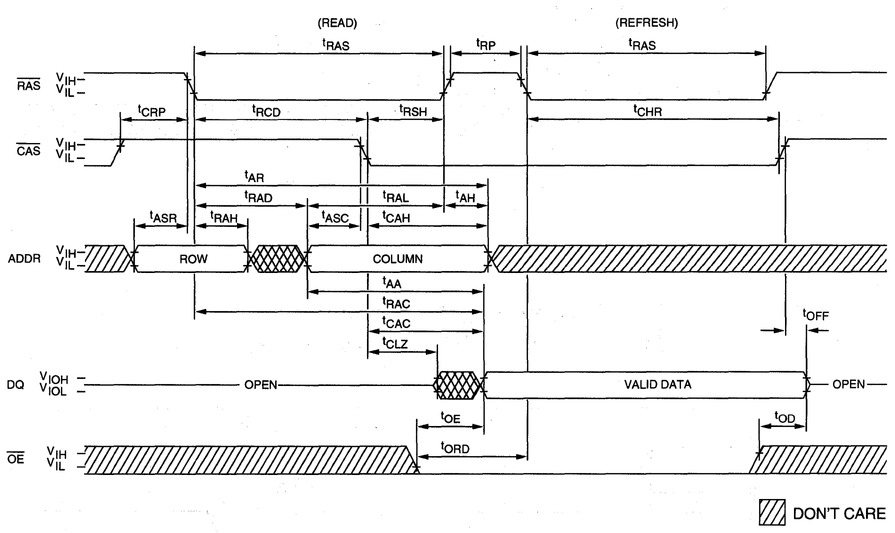
CBR REFRESH CYCLE
(A0-A8, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE[24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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DRAM

1 MEG x 4 DRAM

STANDARD OR SELF REFRESH

FEATURES

- 1,024-cycle refresh distributed across 16ms (MT4C4001J) or 128ms (MT4C4001J S)
- Industry-standard pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN; optional Extended and SELF REFRESH modes (MT4C4001J S only)
- FAST PAGE MODE access cycle
- Low power, 0.8mW standby; 225mW active, typical (MT4C4001J S)

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG
Plastic ZIP (400 mil)	Z
• Version	
1,024-cycle refresh in 16ms	None
1,024-cycle refresh in 128ms	S

- Part Number Example: MT4C4001JDJ-6 S

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ (DC-1)

Signal	Pin	Pin	Signal
DQ1	1	26	Vss
DQ2	2	25	DQ4
WE	3	24	DQ3
RAS	4	23	CAS
A9	5	22	OE
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

20-Pin ZIP (DB-2)

Signal	Pin	Pin	Signal
OE	1	2	CAS
DQ3	3	4	DQ4
Vss	5	6	DQ1
DQ2	7	8	WE
RAS	9	10	A9
A0	11	12	A1
A2	13	14	A3
Vcc	15	16	A4
A5	17	18	A6
A7	19	20	A8

20/26-Pin TSOP (DD-1)

Signal	Pin	Pin	Signal
DQ1	1	26	Vss
DQ2	2	25	DQ4
WE	3	24	DQ3
RAS	4	23	CAS
A9	5	22	OE
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

GENERAL DESCRIPTION

The MT4C4001J(S) is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pins, the outputs (Qs) are activated and retain the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by WE and OE.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the

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RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms for the MT4C4001J and every 128ms for the MT4C4001J S, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

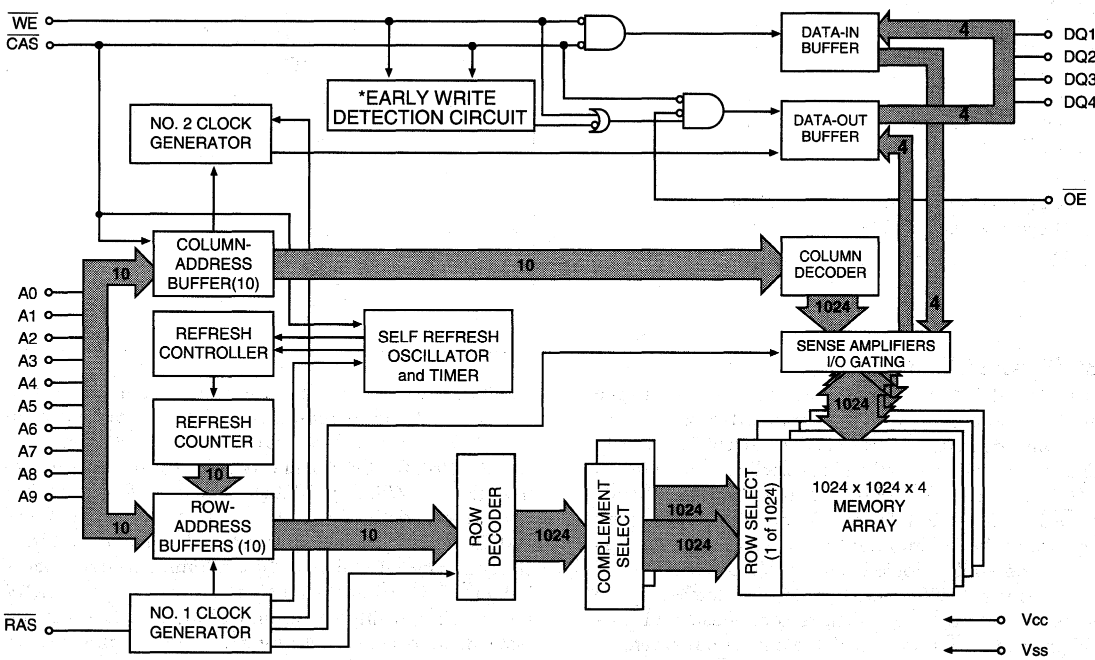
REFRESH

An optional SELF REFRESH mode is also available. The "S" option allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified ᵗRASS. Additionally, the "S" option allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ᵗRPS (≈ᵗRC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or BURST REFRESH sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



***NOTE:** 1. If WE goes LOW prior to CAS going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If CAS goes LOW prior to WE going LOW, EW detection circuit output is a LOW (LATE WRITE).

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DRAM

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ᵗR	ADDRESSES ᵗC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH (MT4C4001J S only)		H→L	L	H	X	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

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DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	VERSION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	MT4C4001J	I_{CC2}	1	1	1	mA	
	MT4C4001J S	I_{CC2}	200	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: ^tRC = ^tRC [MIN])		I_{CC3}	110	100	90	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])		I_{CC4}	80	70	60	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])		I_{CC5}	110	100	90	mA	3, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC6}	110	100	90	mA	3, 5
REFRESH CURRENT: Extended Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$, A0-A9 and D_{IN} = V_{CC} -0.2V or 0.2V; (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	MT4C4001J S	I_{CC7}	300	300	300	µA	3, 5, 28
SELF REFRESH CURRENT: Average power supply current during SELF REFRESH: CBR cycle with $^tRAS \geq {}^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -.2; A0-A9 and D_{IN} = V_{CC} -.2V or .2V (D_{IN} may be left open)	MT4C4001J S	I_{CC8}	300	300	300	µA	5, 31

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ WRITE cycle time	tRWC	150		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	85		100		105		ns	
Access time from RAS	tRAC		60		70		80	ns	14
Access time from CAS	tCAC		15		20		20	ns	15
Output Enable	tOE		15		20		20	ns	23
Access time from column-address	tAA		30		35		40	ns	
Access time from CAS precharge	tCPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time (CBR REFRESH)	tCPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row-address setup time	tASR	0		0		0		ns	
Row-address hold time	tRAH	10		10		10		ns	
RAS to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		0		ns	
Column-address hold time	tCAH	10		15		15		ns	
Column-address hold time (referenced to RAS)	tAR	45		50		55		ns	
Column-address to RAS lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	tRCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	19
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	tOFF	3	15	3	20	3	20	ns	20, 29

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DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 27
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		110		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		65		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		50		50		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles) MT4C4001J / MT4C4001J S	^tREF		16 / 128		16 / 128		16 / 128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	25
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	25
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Output disable	^tOD		15		20		20	ns	27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	26
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^tRASS	100		100		100		µs	31
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^tRPS	110		130		150		ns	31
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH cycle	^tCHD	10		10		10		ns	31

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
28. Extended refresh current is reduced as ^{t}RAS is reduced from its maximum specification during the extended refresh cycle.
29. The 3ns minimum is a parameter guaranteed by design.
30. Column-address changed once each cycle.
31. If the DRAM controller uses a BURST REFRESH, a BURST REFRESH of all rows must be executed upon exiting SELF REFRESH.

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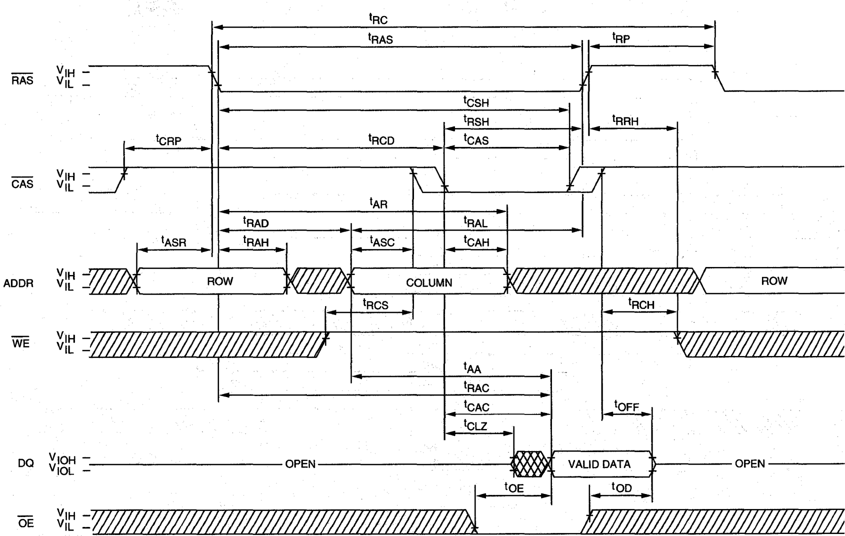
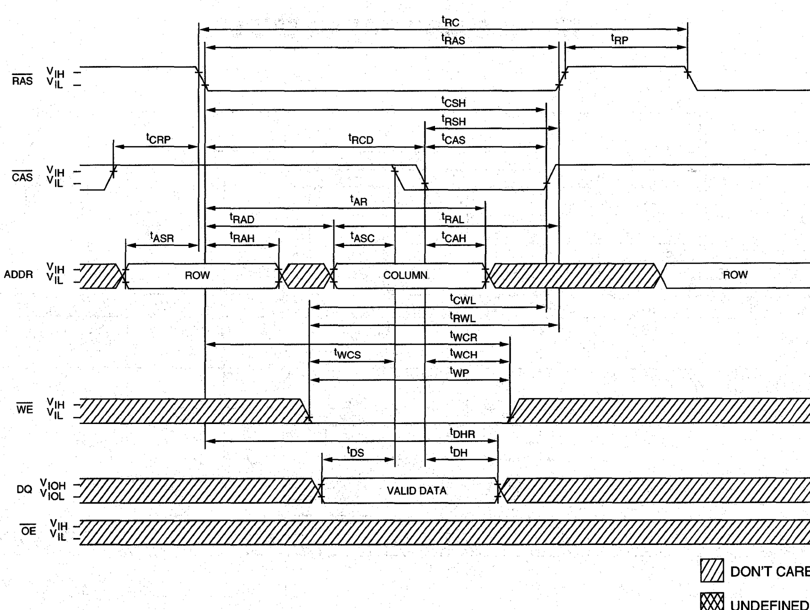
READ CYCLE



EARLY WRITE CYCLE



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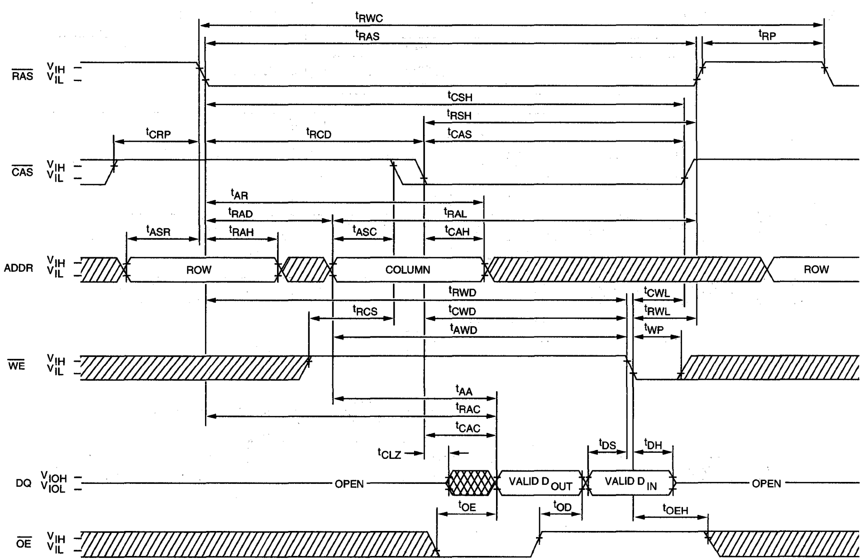
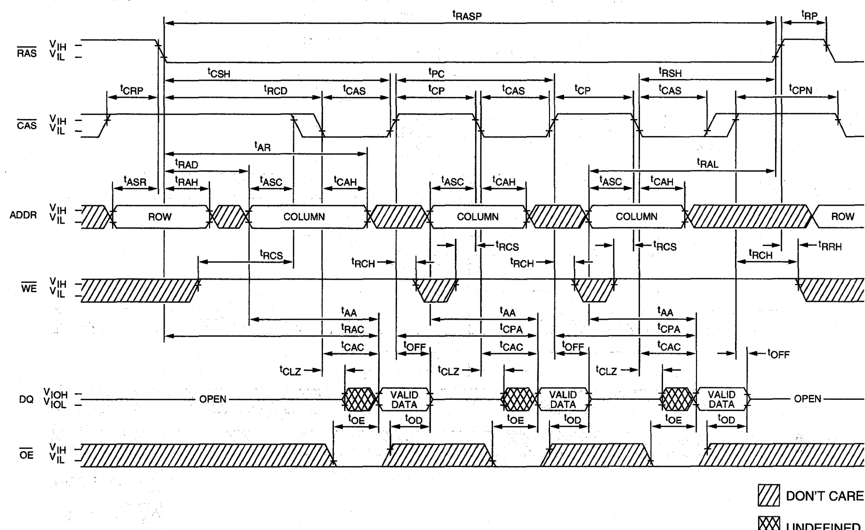
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

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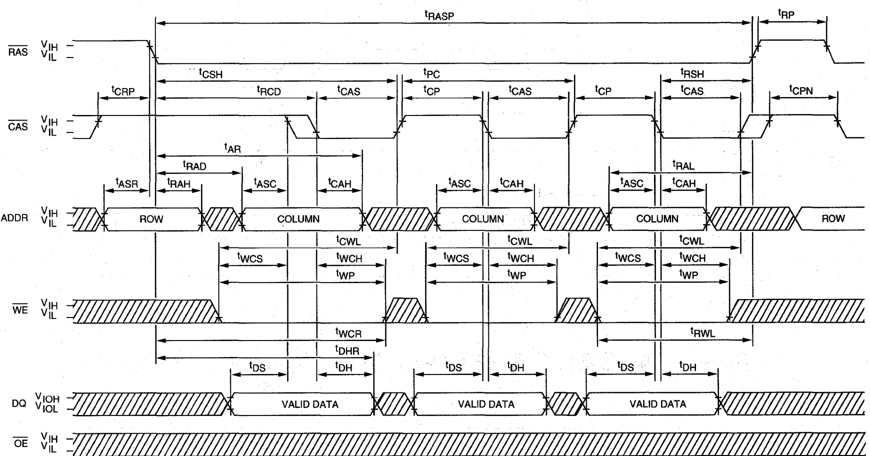
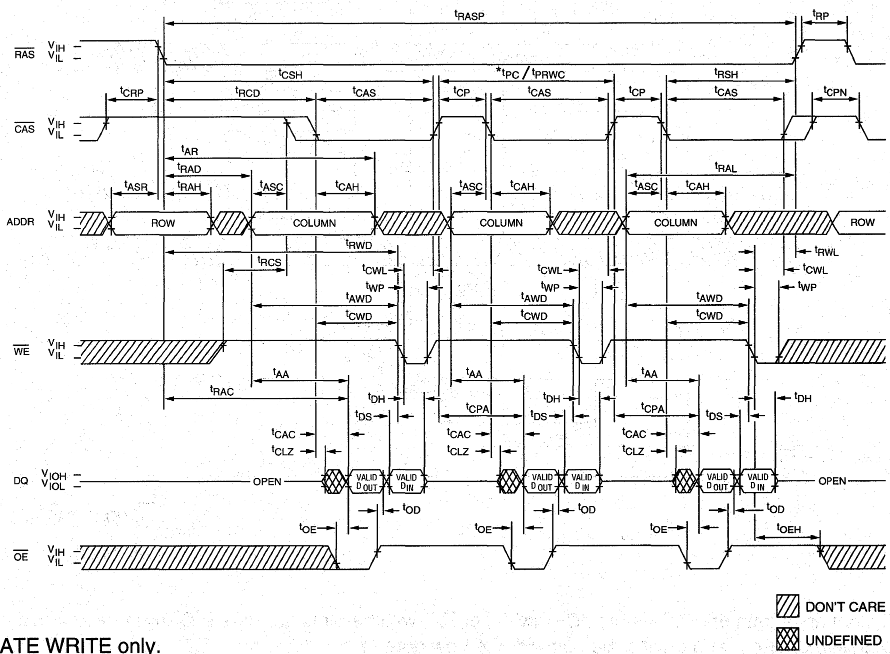
DRAM

FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



DON'T CARE

UNDEFINED

*tPC is for LATE WRITE only.

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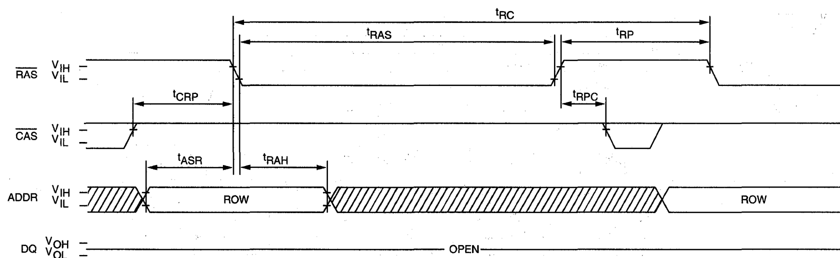
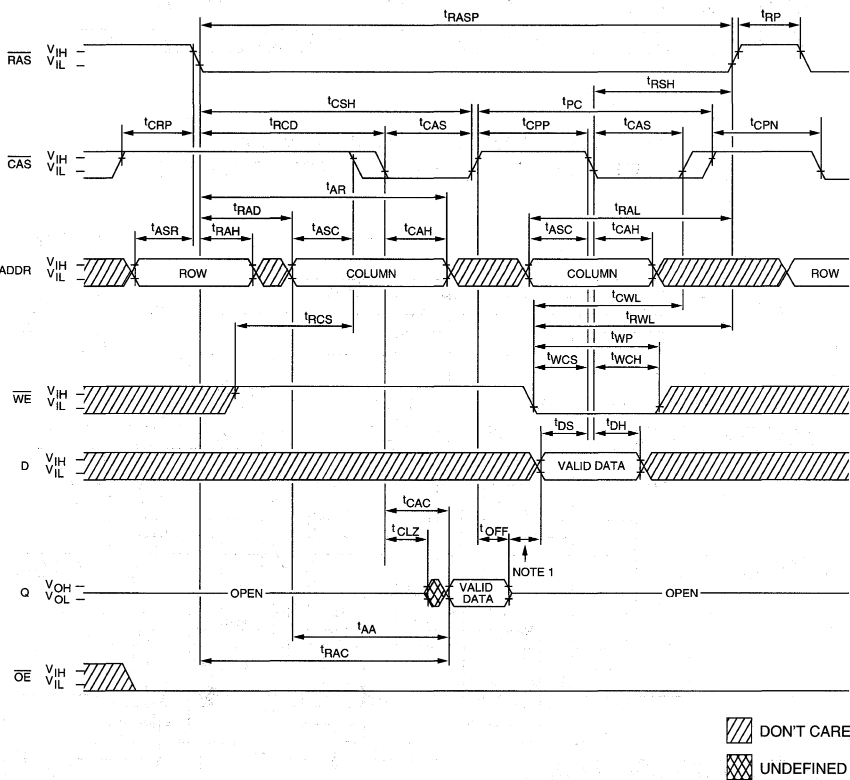
DRAM

$\overline{RAS}$ ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{WE}$ = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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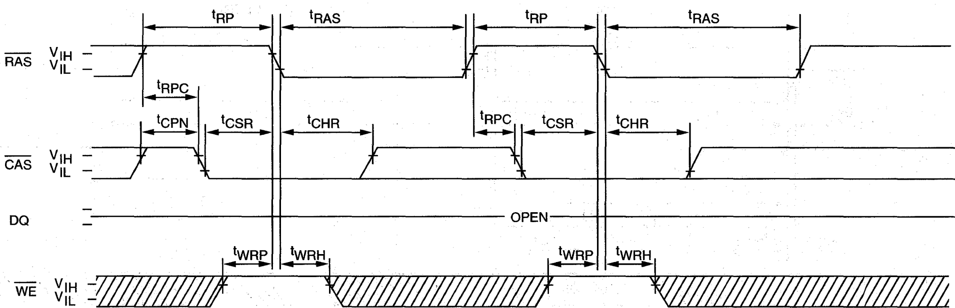
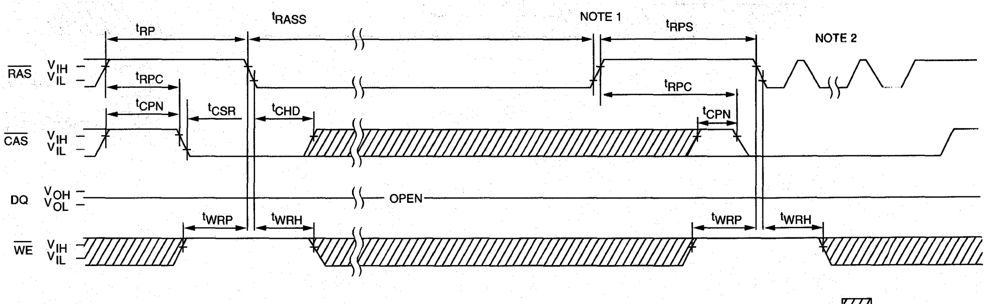
CBR REFRESH CYCLE
(A0-A9 and $\overline{OE}$ = DON'T CARE)



SELF REFRESH CYCLE (MT4C4001J S only)
(A0-A9 and $\overline{OE}$ = DON'T CARE)



DON'T CARE

UNDEFINED

NOTE: 1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a complete burst of all rows should be executed.

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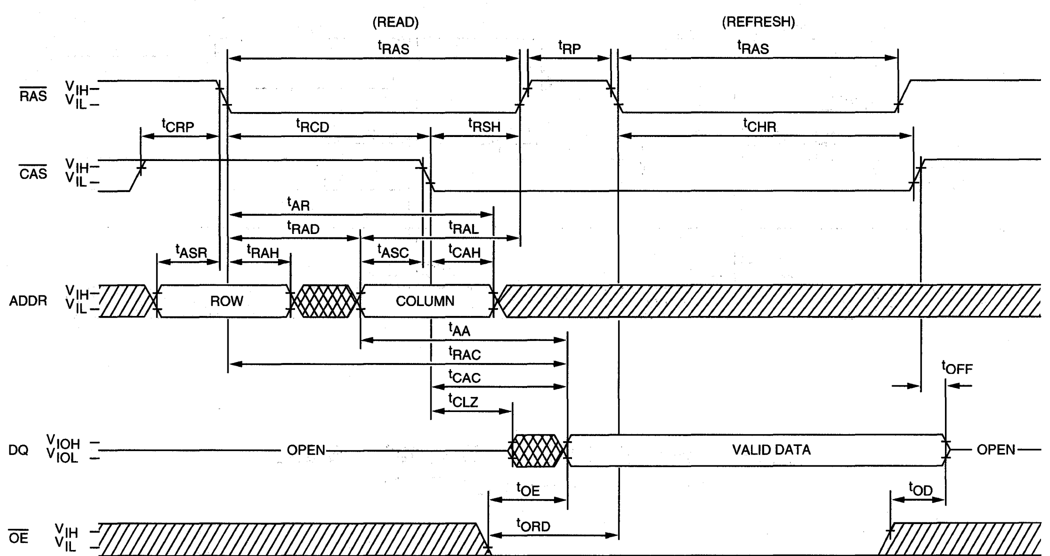
DRAM

HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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DRAM

4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh cycle of the 1 Meg is the CBR REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{\text{WE}}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{\text{WE}}$ pin held at a voltage HIGH level.

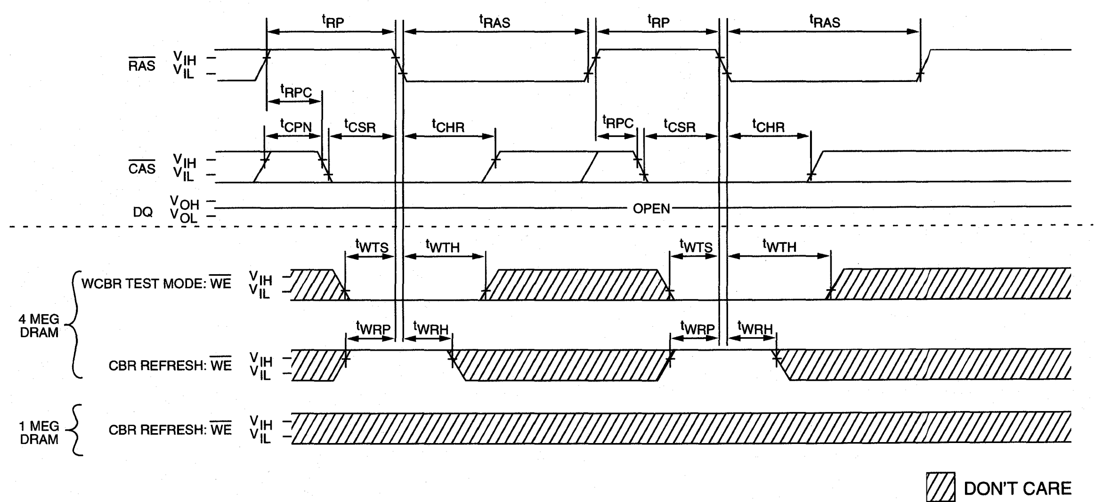
A CBR cycle with $\overline{\text{WE}}$ LOW will put the 4 Meg into the JEDEC-specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{\text{RAS}}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{\text{RAS}}$ ONLY or CBR REFRESH ($\overline{\text{WE}}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC-specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{\text{RAS}}$ ONLY or a CBR REFRESH cycle ($\overline{\text{WE}}$ held HIGH).

SUMMARY

1. The 1 Meg CBR REFRESH allows the $\overline{\text{WE}}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{\text{WE}}$ to be HIGH.
2. The eight $\overline{\text{RAS}}$ wake-up cycles on the 1 Meg may be any valid $\overline{\text{RAS}}$ cycle while the 4 Meg may only use $\overline{\text{RAS}}$ ONLY or CBR REFRESH cycles ($\overline{\text{WE}}$ held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

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DRAM

1 MEG x 4 DRAM

3.3V FAST PAGE MODE
OPTIONAL SELF REFRESH

FEATURES

- Single +3.3V ±.3V power supply
- Low power, 250µW standby; 100mW active, typical
- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN; optional Extended and SELF REFRESH modes
- FAST PAGE MODE access cycle
- 1,024-cycle Extended Refresh distributed across 16ms or 128ms
- Low SELF REFRESH current, 100µA typical, 150µA (MAX)

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Refresh	
Standard	None
Low-power SELF REFRESH	S
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG

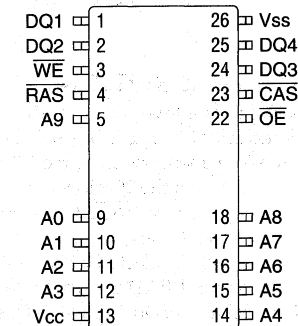
- Part Number Example: MT4LC4001JDJ-7 S

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ
(DC-1)

Signal	Pin	Pin	Signal
DQ1	1	26	Vss
DQ2	2	25	DQ4
WE	3	24	DQ3
RAS	4	23	CAS
A9	5	22	OE
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

20/26-Pin TSOP
(DD-1)



GENERAL DESCRIPTION

The MT4LC4001J(S) is specially designed to operate from 3.0V to 3.6V for low-voltage memory systems. It is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. This device operates in FAST PAGE MODE, which allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary.

The wide voltage range on this device allows it to be used in 3.3V ±.3V memory designs. The refresh period is available in the standard 16ms or 128ms to provide maximum power savings. An optional SELF REFRESH mode is also available. The "S" option allows the user to choose a fully static low-power data-retention mode, or a dynamic refresh mode at the extended-refresh period of 128ms, eight times longer than the standard 16ms specification.

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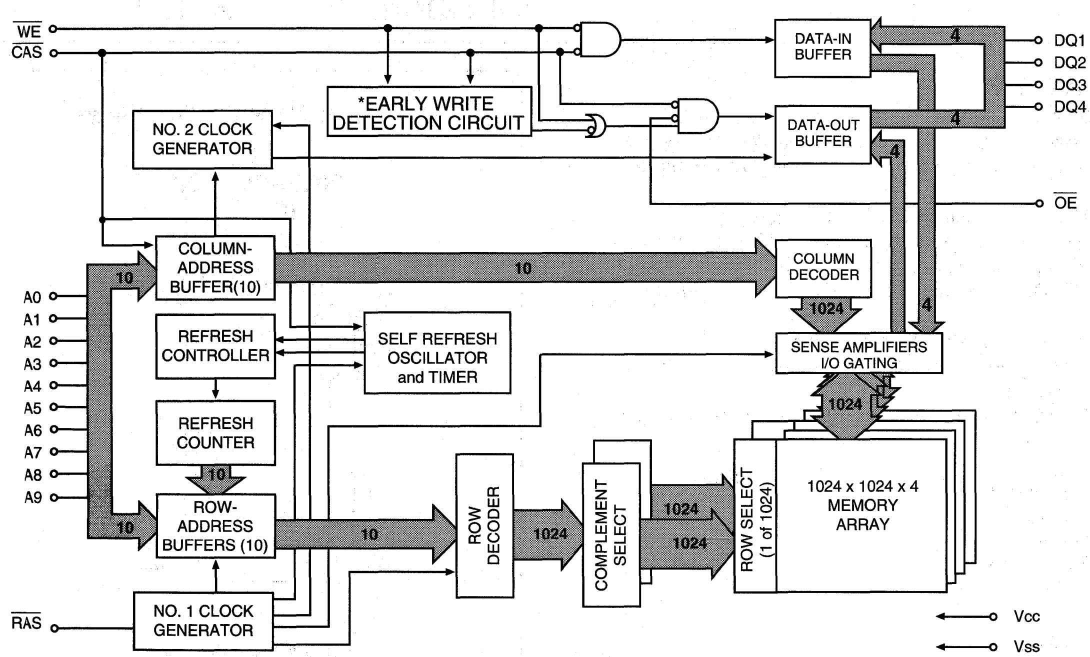
FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



***NOTE:** 1. If WE goes LOW prior to CAS going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If CAS goes LOW prior to WE going LOW, EW detection circuit output is a LOW (LATE WRITE).

FUNCTIONAL DESCRIPTION

The MT4LC4001J(S) is a low-power, 1 Meg x 4 DRAM with optional SELF REFRESH. During READ or WRITE cycles, each of the four memory bits (one bit per DQ) is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS latches the first 10 bits and CAS latches the latter 10 bits.

A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pins remain open (High-Z) until the next CAS cycle, which is an EARLY WRITE cycle.

If WE goes LOW after data reaches the output pins (minimal delay after CAS goes LOW), the outputs (Qs) are activated and retain the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in either a LATE WRITE (OE-controlled) or a READ WRITE (READ-MODIFY-WRITE) cycle.

The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE and OE.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) with lower power consumption within a row-address-defined (A0-A9) page boundary.

The FAST PAGE MODE cycle always initiates with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles.

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Returning $\overline{RAS}$ to HIGH terminates FAST PAGE MODE operation.

REFRESH

Preserve correct memory cell data by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed within ^{t}REF max, regardless of sequence. The CBR REFRESH cycle and SELF REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

An optional SELF REFRESH mode is also available on the MT4LC4001J S. The "S" option allows the user the choice of a fully static low power data rentention mode, or a dynamic refresh mode at the extended refresh period of 128ms. The optional SELF REFRESH feature is initiated by permorming a CBR refresh cycle, and holding $\overline{RAS}$ low for the specified ^{t}RASS. Additionally, the "S" option allows for an extended refresh period of 128ms, or 125µs per row if using distributed CBR refresh. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting SELF REFRESH. However, if the DRAM controller utilizes $\overline{RAS}$ only or burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate (~150µs), prior to the resumption of normal operation.

STANDBY

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time.

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^{t}R	ADDRESSES ^{t}C	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} .... -1.0V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.0V to 3.6V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC}+0.5V (All other pins not under test = 0V)		I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ V_{CC}+0.5V)		I_{OZ}	-10	10	µA	
TTL OUTPUT LEVELS	High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
	Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	VERSION	SYMBOL	MAX			UNITS	NOTES
			-6	-7	-8		
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC1}	1	1	1	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	MT4LC4001J	I_{CC2}	500	500	500	µA	
	MT4LC4001J S	I_{CC2}	100	100	100	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC3}	80	70	60	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])		I_{CC4}	60	50	40	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])		I_{CC5}	80	70	60	mA	3, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC6}	80	70	60	mA	3, 5
EXTENDED REFRESH CURRENT: Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; ^tRAS = ^tRAS (MIN); $\overline{WE}$ = V_{CC} - 0.2V; A0-A9 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	MT4LC4001J S	I_{CC7}	150	150	150	µA	3, 5, 28
SELF REFRESH CURRENT: Average power supply current during SELF REFRESH: CBR cycle with ^tRAS ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} - 0.2V; A0-A9 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	MT4LC4001J S	I_{CC8}	150	150	150	µA	5, 29

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +3.0V to 3.6V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	150		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		100		105		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Output Enable time	^tOE		15		20		20	ns	23
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	

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DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +3.0V to 3.6V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	tOFF	3	15	3	20	3	20	ns	20
WE command setup time	tWCS	0		0		0		ns	21, 27
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	10		15		15		ns	22
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
RAS to WE delay time	tRWD	85		100		110		ns	21
Column-address to WE delay time	tAWD	55		65		70		ns	21
CAS to WE delay time	tCWD	40		50		50		ns	21
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles) MT4LC4001J/MT4LC4001J S	tREF		16/128		16/128		16/128	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CBR REFRESH)	tCSR	10		10		10		ns	5
CAS hold time (CBR REFRESH)	tCHR	10		10		10		ns	5
WE hold time (CBR REFRESH)	tWRH	10		10		10		ns	25
WE setup time (CBR REFRESH)	tWRP	10		10		10		ns	25
WE hold time (WCBR test cycle)	tWTH	10		10		10		ns	25
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		0		ns	
Output disable	tOD		15		20		20	ns	27
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		20		20		ns	26
RAS pulse width during SELF REFRESH cycle	tRASS	100		100		100		µs	29
RAS precharge time during SELF REFRESH cycle	tRPS	110		130		150		ns	29
RAS LOW to "don't care" during SELF REFRESH cycle	tCHD	10		10		10		ns	29

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DRAM

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3V ±.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$ ONLY or CBR with $\overline{\text{WE}}$ HIGH) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{\text{CAS}}$ = V_{IH}, data output is High-Z.
12. If $\overline{\text{CAS}}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF. Output reference voltages are 0.8V for a low level and 2.0V for a high level.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE WRITE ($\overline{\text{OE}}$-controlled) cycle.
22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{\text{OE}}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{\text{WE}}$ = LOW and $\overline{\text{OE}}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{\text{WE}}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
26. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{\text{OE}}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{\text{OE}}$ is taken back LOW while $\overline{\text{CAS}}$ remains LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{\text{CAS}}$ goes HIGH before $\overline{\text{OE}}$, the DQs will open regardless of the state of $\overline{\text{OE}}$. If $\overline{\text{CAS}}$ stays LOW while $\overline{\text{OE}}$ is brought HIGH, the DQs will open. If $\overline{\text{OE}}$ is brought back LOW ($\overline{\text{CAS}}$ still LOW), the DQs will provide the previously read data.
28. Refresh current increases if ^{t}RAS is extended beyond its minimum specification.
29. If the DRAM controller uses a BURST REFRESH, a BURST REFRESH of all rows must be executed upon exiting SELF REFRESH.
30. Column-address changed once each cycle.

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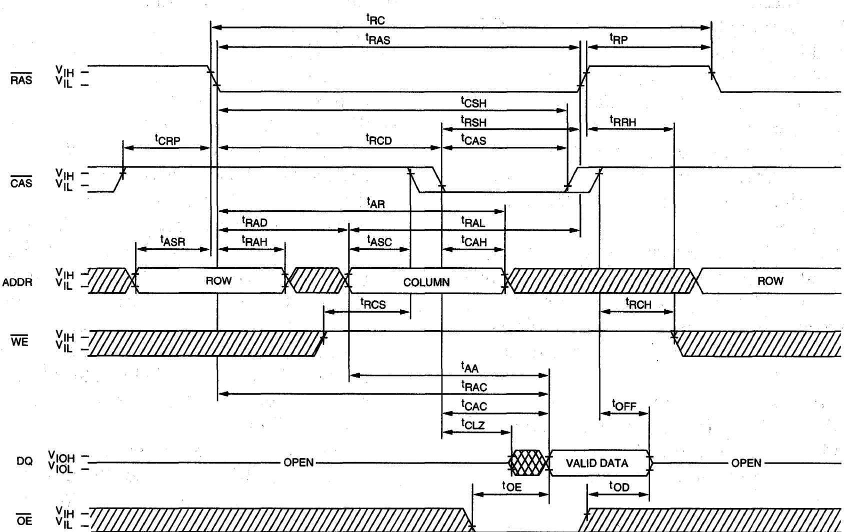
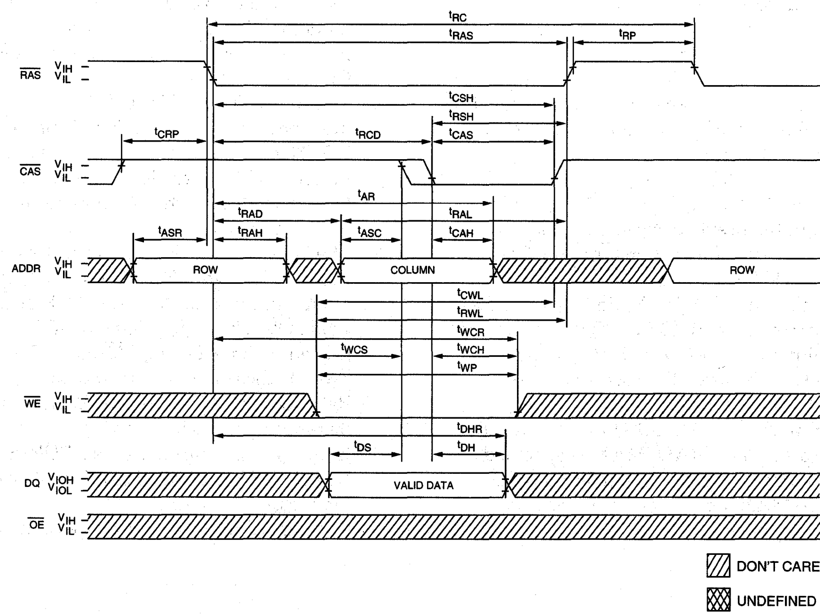
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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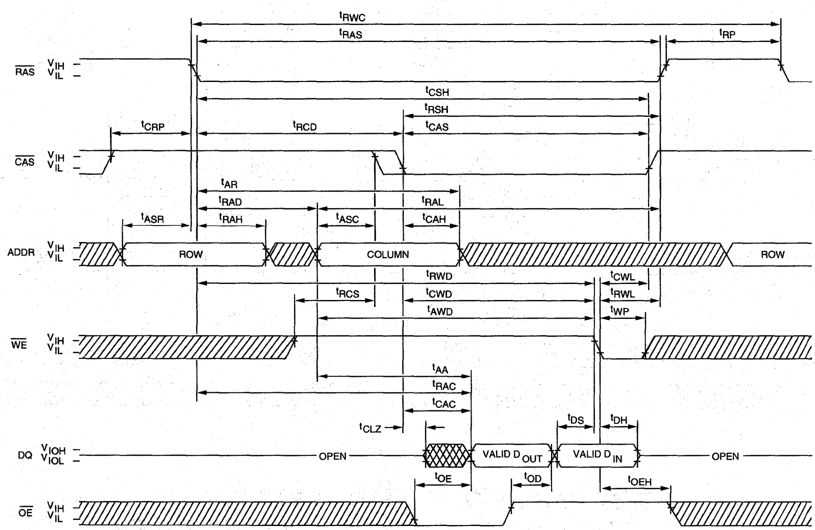
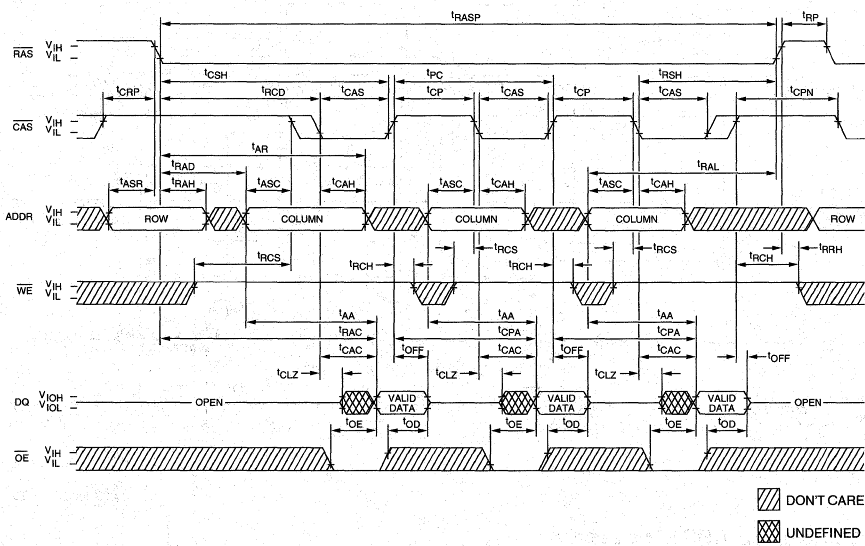
DRAM

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



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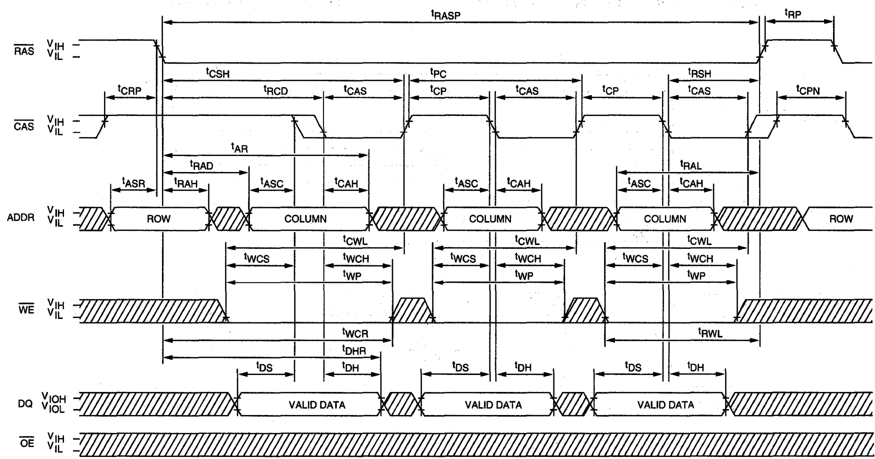
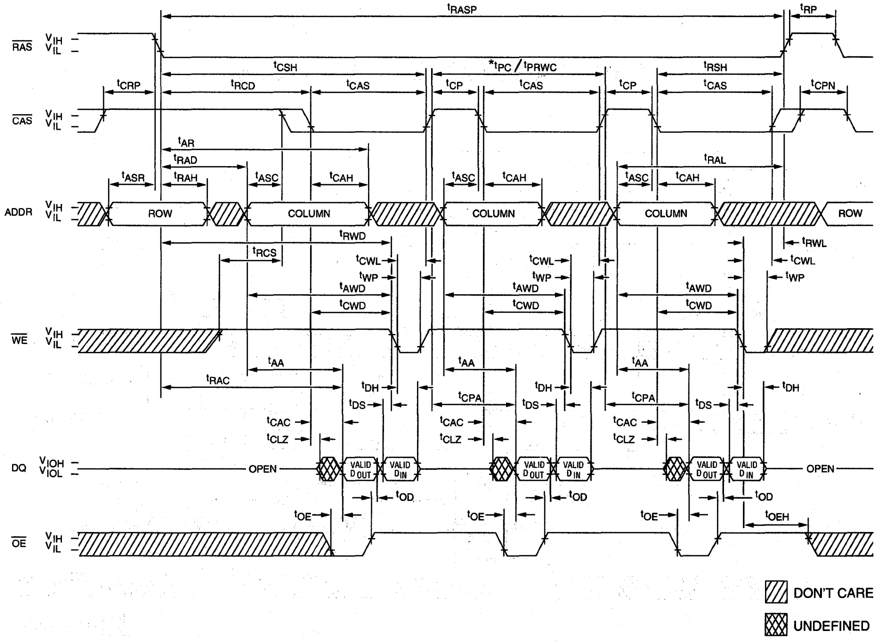
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



***NOTE:** ^tPC is for LATE WRITE cycles only.

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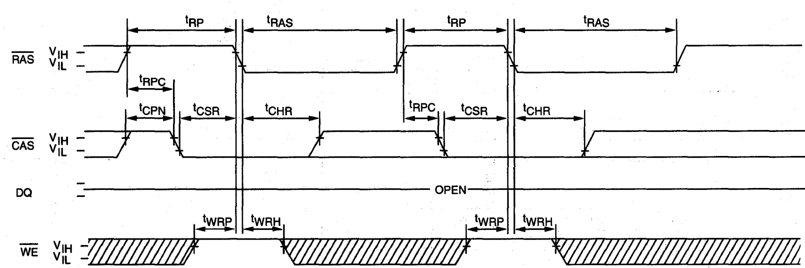
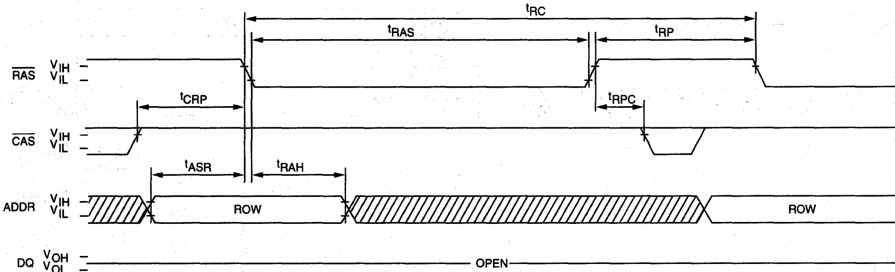
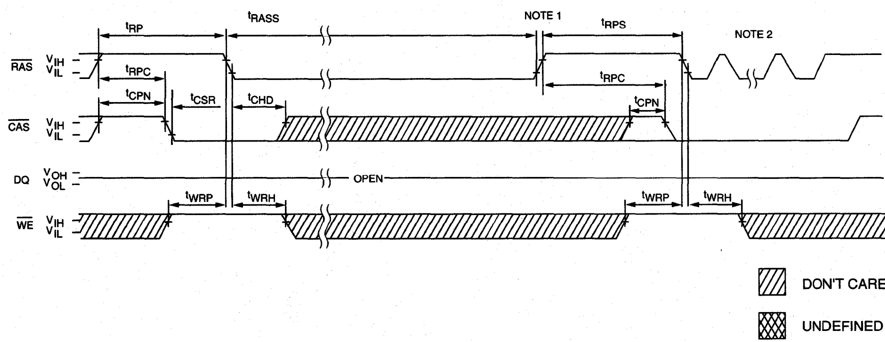
CBR REFRESH CYCLE
(A0-A9 and $\overline{OE}$ = DON'T CARE)



$\overline{RAS}$ ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{WE}$ = DON'T CARE)



SELF REFRESH CYCLE
(A0-A9 and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a complete burst of all rows should be executed.

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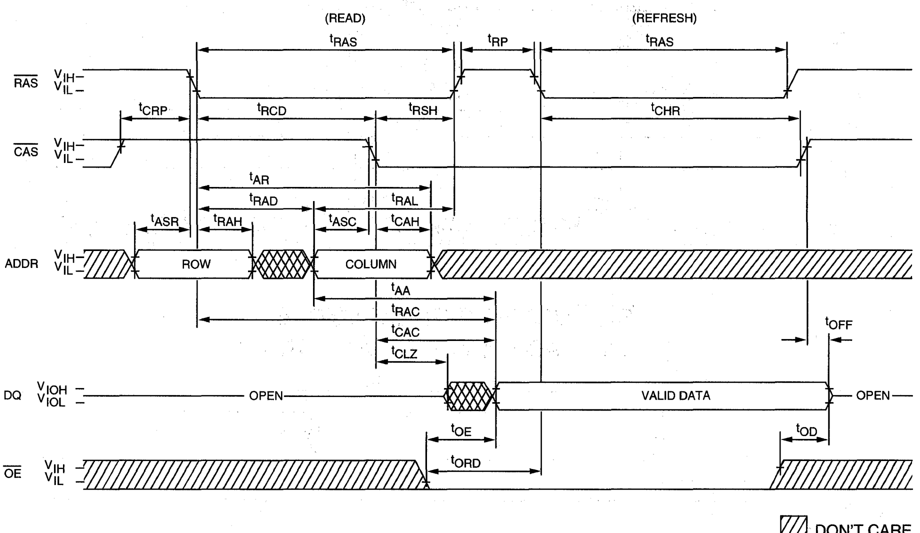
HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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DRAM

1 MEG x 4 DRAM

STATIC COLUMN

FEATURES

- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), and HIDDEN
- STATIC COLUMN access cycle

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
70ns access	-7
80ns access	-8
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic ZIP (350 mil)	Z

- Part Number Example: MT4C4003JDJ-7

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ (DC-1)

Signal	Pin	Pin	Signal
DQ1	1	26	Vss
DQ2	2	25	DQ4
$\overline{WE}$	3	24	DQ3
$\overline{RAS}$	4	23	$\overline{CAS}$
A9	5	22	$\overline{OE}$
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

20-Pin ZIP (DB-2)

Signal	Pin	Pin	Signal
$\overline{OE}$	1	2	$\overline{CAS}$
DQ3	3	4	DQ4
Vss	5	6	DQ1
DQ2	7	8	$\overline{WE}$
$\overline{RAS}$	9	10	A9
A0	11	12	A1
A2	13	14	A3
Vcc	15	16	A4
A5	17	18	A6
A7	19	20	A8

GENERAL DESCRIPTION

The MT4C4003J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. After the first read, any column-address transition will result in new data-out. Unlike PAGE MODE, which requires $\overline{CAS}$ to be toggled for each successive PAGE MODE access, STATIC COLUMN allows $\overline{CAS}$ to be left LOW for successive STATIC COLUMN accesses. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

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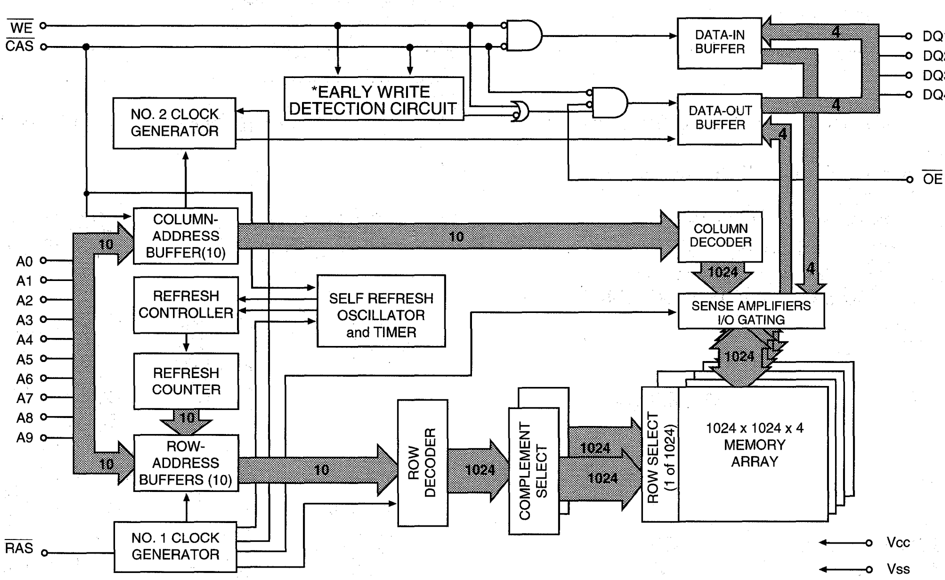
FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



***NOTE:** 1. If WE goes LOW prior to CAS going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If CAS goes LOW prior to WE going LOW, EW detection circuit output is a LOW (LATE WRITE).

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES ᵗR	ADDRESSES ᵗC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
STATIC-COLUMN READ	1st Cycle	L	L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	L	H	L	n/a	COL	Data-Out
STATIC-COLUMN EARLY-WRITE	1st Cycle	L	L	L	X	ROW	COL	Data-In
	2nd Cycle	L	L	L	X	n/a	COL	Data-In
STATIC-COLUMN READ-WRITE	1st Cycle	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	ICC3	100	90	mA	3, 4, 28
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	ICC4	70	60	mA	3, 4, 28
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = VIH: ^tRC = ^tRC [MIN])	ICC5	100	90	mA	3, 28
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	ICC6	100	90	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	CI1		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	CI2		7	pF	2
Input/Output Capacitance: DQ	CIO		7	pF	2

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DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5.V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	130		150		ns	
READ WRITE cycle time	tRWC	185		205		ns	
STATIC-COLUMN READ or WRITE cycle time	tSC	40		45		ns	
STATIC-COLUMN READ-WRITE cycle time	tSRWC	100		110		ns	
Access time from $\overline{RAS}$	tRAC		70		80	ns	14
Access time from $\overline{CAS}$	tCAC		20		20	ns	15
Output Enable	tOE		20		20	ns	23
Access time from column-address	tAA		35		40	ns	
$\overline{RAS}$ pulse width	tRAS	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	tRASC	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		20		ns	
$\overline{RAS}$ precharge time	tRP	50		60		ns	
$\overline{CAS}$ pulse width	tCAS	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	tCSH	70		80		ns	
$\overline{CAS}$ precharge time	tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10		10		ns	
Row-address setup time	tASR	0		0		ns	
Row-address hold time	tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	tRAD	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		ns	
Column-address hold time	tCAH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	tAR	75		85		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	35		40		ns	
Read command setup time	tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		ns	
Output buffer turn-off delay	tOFF	3	20	3	20	ns	20, 29
Column-address hold time (referenced to $\overline{RAS}$)	tAWR	55		60		ns	
$\overline{WE}$ command setup time	tWCS	0		0		ns	21, 27
Write command hold time	tWCH	15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	55		60		ns	
Write command pulse width	tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	20		20		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command to $\overline{\text{CAS}}$ lead time	^{t}CWL	20		20		ns	
Data-in setup time	^{t}DS	0		0		ns	22
Data-in hold time	^{t}DH	15		15		ns	22
Data-in hold time (referenced to $\overline{\text{RAS}}$)	^{t}DHR	55		60		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	^{t}RWD	100		110		ns	21
Column-address to $\overline{\text{WE}}$ delay time	^{t}AWD	65		70		ns	21
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	^{t}CWD	50		50		ns	21
Transition time (rise or fall)	^{t}T	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^{t}REF		16		16	ms	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	^{t}RPC	0		0		ns	
$\overline{\text{CAS}}$ setup time (CBR REFRESH)	^{t}CSR	10		10		ns	5
$\overline{\text{CAS}}$ hold time (CBR REFRESH)	^{t}CHR	15		15		ns	5
$\overline{\text{WE}}$ hold time (CBR REFRESH)	^{t}WRH	10		10		ns	25
$\overline{\text{WE}}$ setup time (CBR REFRESH)	^{t}WRP	10		10		ns	25
$\overline{\text{WE}}$ hold time (WCBR test cycle)	^{t}WTH	10		10		ns	25
$\overline{\text{WE}}$ setup time (WCBR test cycle)	^{t}WTS	10		10		ns	25
$\overline{\text{OE}}$ setup prior to $\overline{\text{RAS}}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		ns	
Output disable	^{t}OD		20		20	ns	27
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$ during READ-MODIFY-WRITE cycle	^{t}OEH	20		20		ns	26
Write inactive time	^{t}WI	10		10		ns	
Previous WRITE to column-address delay time	^{t}LWAD	20	30	20	35	ns	
Previous WRITE to column-address hold time	^{t}AHLW	65		75		ns	
$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	^{t}ROH	10		10		ns	
Output data hold time from column-address	^{t}AOH	5		5		ns	
Output data enable from WRITE	^{t}OW	^{t}AA + 5		^{t}AA + 5		ns	
Access time from last WRITE	^{t}ALW	65		75		ns	
Column-address hold time referenced to $\overline{\text{RAS}}$ HIGH	^{t}AH	5		10		ns	
$\overline{\text{CAS}}$ pulse width in STATIC COLUMN mode	^{t}CSC	^{t}CAS		^{t}CAS		ns	

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%;f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
28. Column-address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$= V_{IH}
29. The 3ns minimum is a parameter guaranteed by design.

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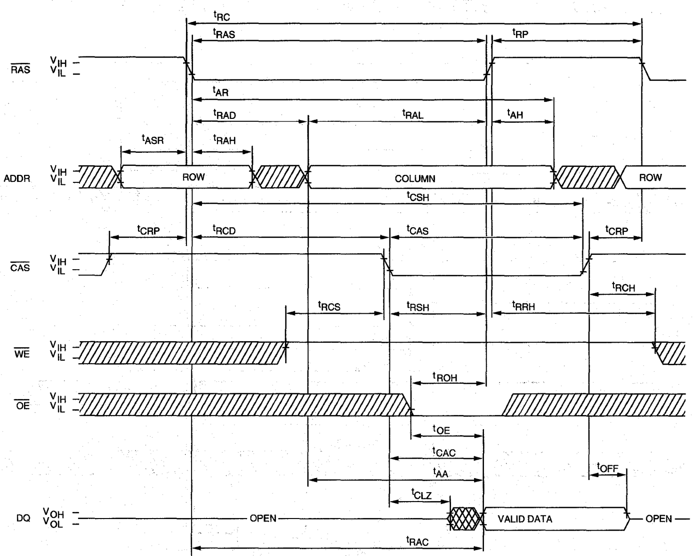
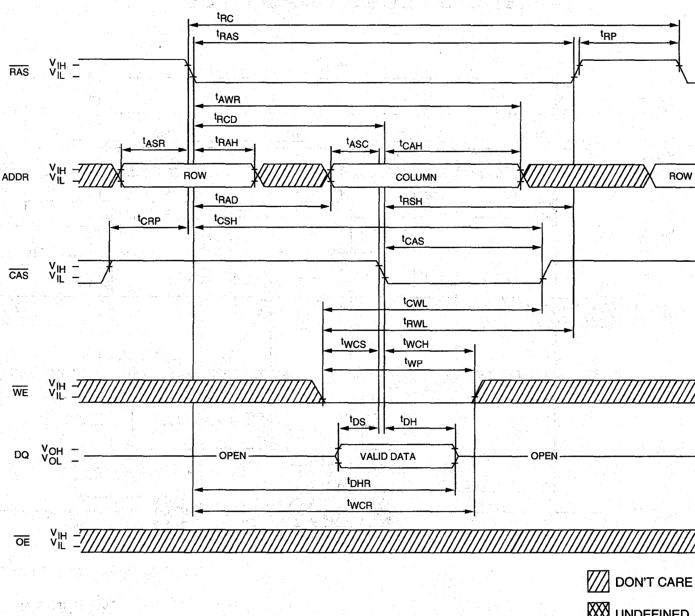
DRAM

READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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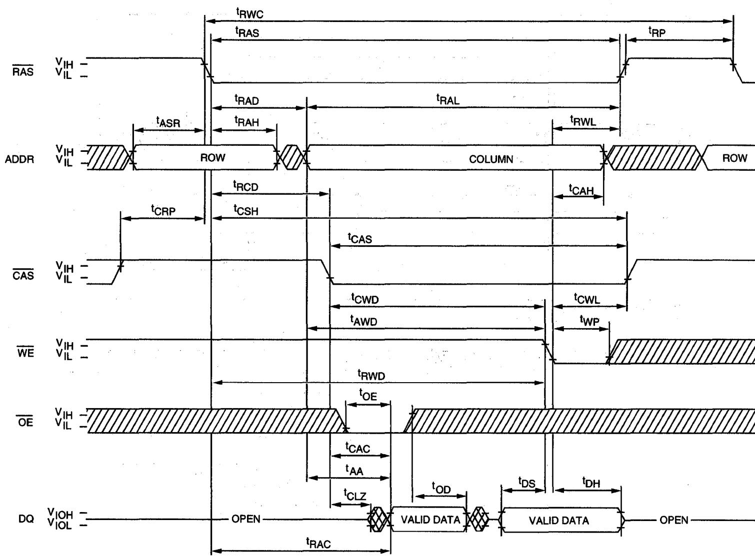
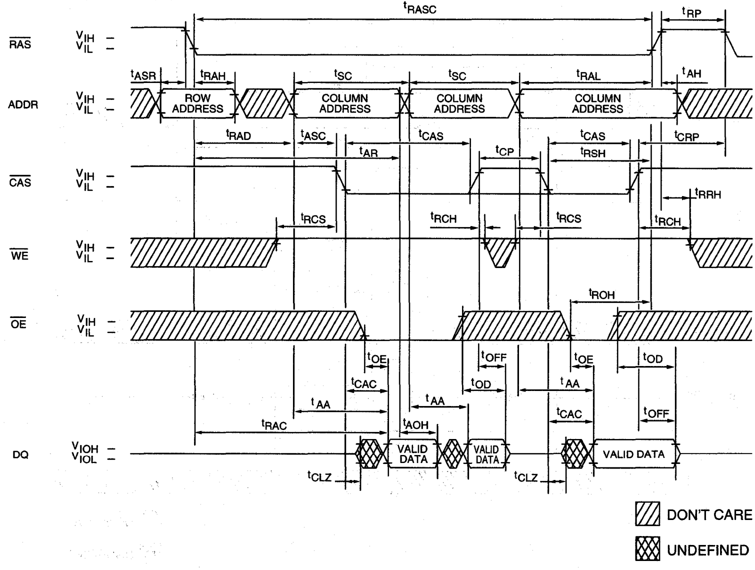
DRAM

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



STATIC-COLUMN READ CYCLE



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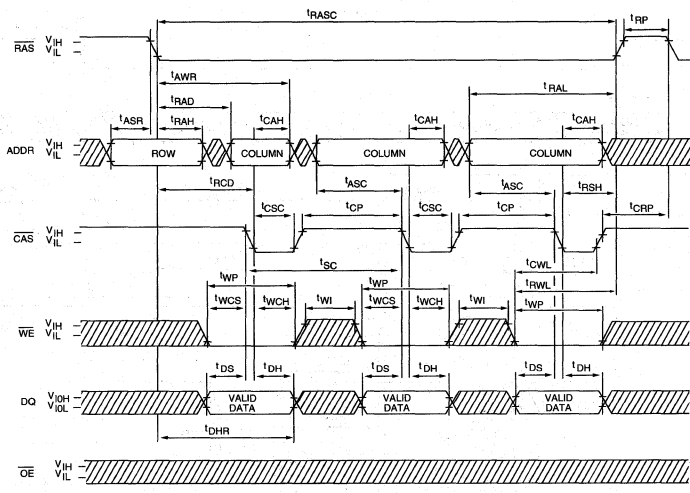
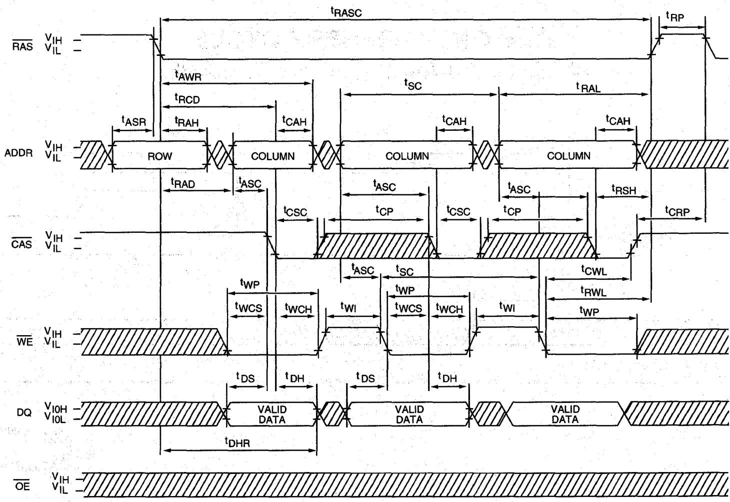
DRAM

STATIC-COLUMN EARLY-WRITE CYCLE
($\overline{CAS}$ Controlled)



STATIC-COLUMN EARLY-WRITE CYCLE
($\overline{WE}$ Controlled)



DON'T CARE

UNDEFINED

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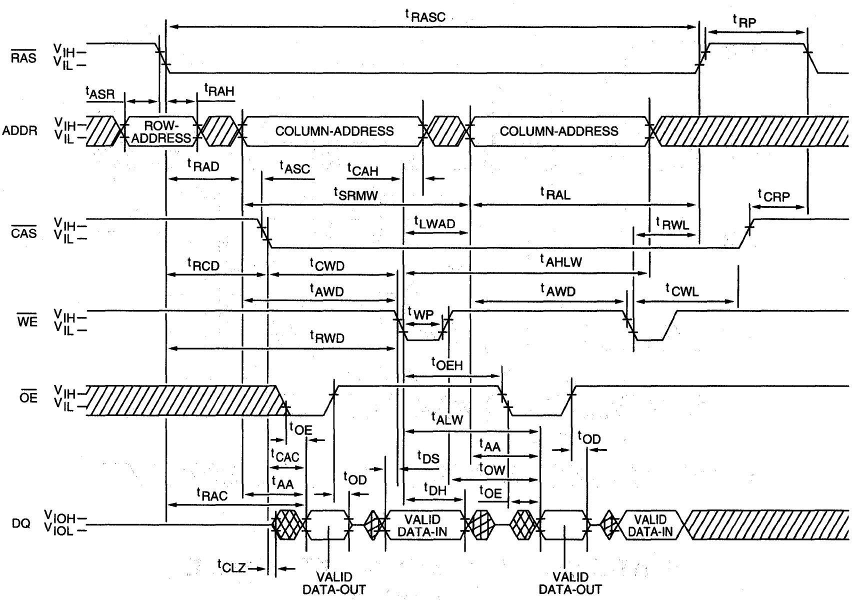
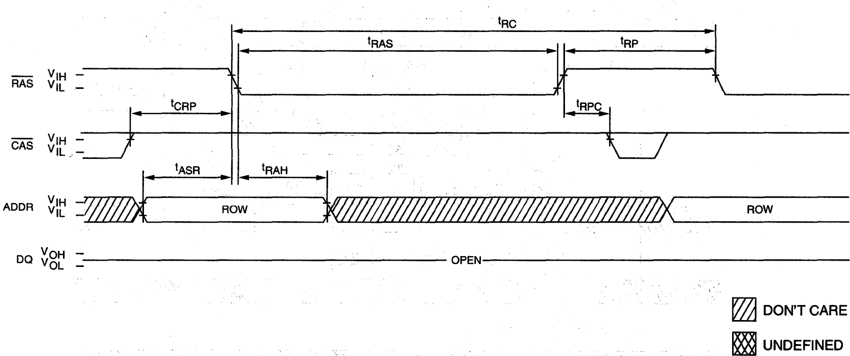
STATIC-COLUMN READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



$\overline{\text{RAS}}$ ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{\text{WE}}$ = DON'T CARE)



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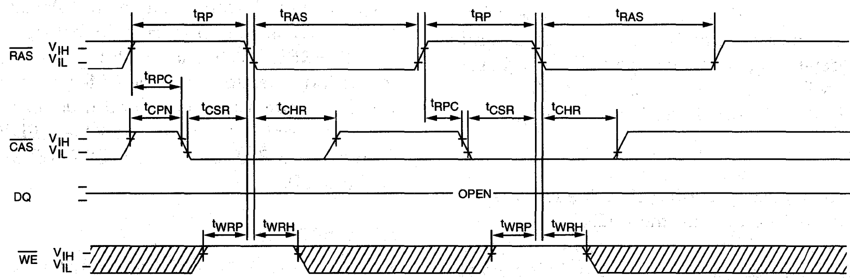
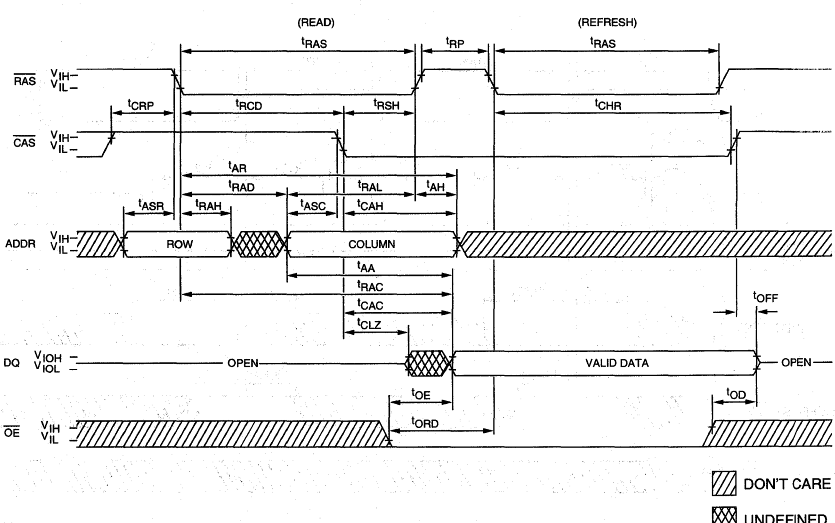
DRAM

CBR REFRESH CYCLE
(A0-A9 and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh cycle of the 1 Meg is the CBR REFRESH cycle. The CBR for the 1 Meg specifies the WE pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the WE pin held at a voltage HIGH level.

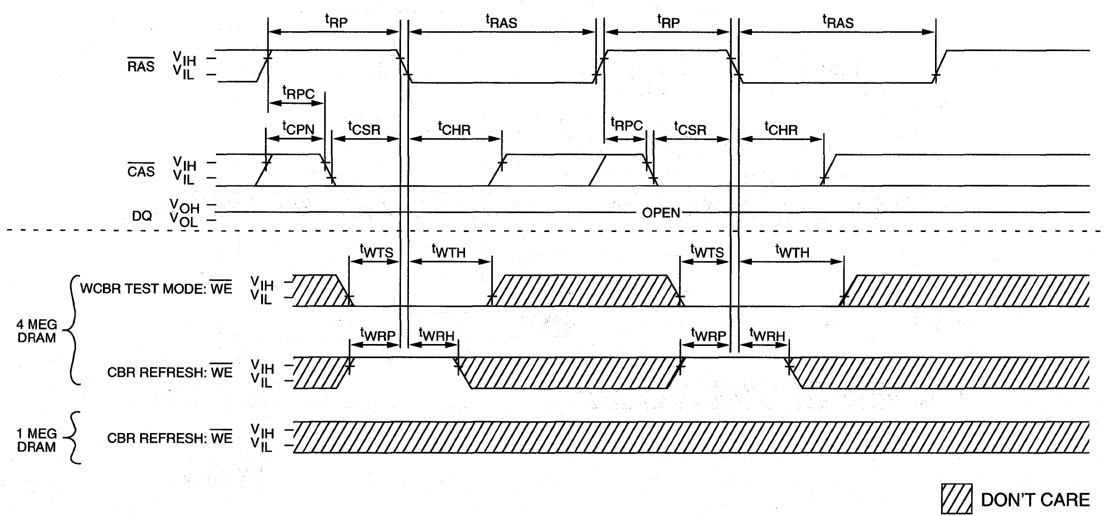
A CBR cycle with WE LOW will put the 4 Meg into the JEDEC-specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight RAS cycles. The 4 Meg POWER-UP is more restrictive in that eight RAS ONLY or CBR REFRESH (WE held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC-specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a RAS ONLY or a CBR REFRESH cycle (WE held HIGH).

SUMMARY

1. The 1 Meg CBR REFRESH allows the WE pin to be "don't care" while the 4 Meg CBR requires WE to be HIGH.
2. The eight RAS wake-up cycles on the 1 Meg may be any valid RAS cycle while the 4 Meg may only use RAS ONLY or CBR REFRESH cycles (WE held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

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DRAM

1 MEG x 4 DRAM

3.3V EDO PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- Single +3.3V ±0.3V power supply
- Low power, 250µW standby; 100mW active, typical
- JEDEC-standard pinout and packages
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN; optional Extended and SELF REFRESH modes
- Extended data-out (EDO) PAGE MODE access cycle
- 1,024-cycle Extended Refresh distributed across 16ms or 128ms
- Low SELF REFRESH current, 100µA typical, 150µA (MAX)
- EDO PAGE MODE cycle times, 25-35ns

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Refresh	
Standard	None
Low-power SELF REFRESH	S
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG

- Part Number Example: MT4LC4007JDJ-7 S

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ (DC-1) / **20/26-Pin TSOP (DD-1)**

Pin	Name	Pin	Name
1	DQ1	26	Vss
2	DQ2	25	DQ4
3	WE	24	DQ3
4	RAS	23	CAS
5	A9	22	OE
9	A0	18	A8
10	A1	17	A7
11	A2	16	A6
12	A3	15	A5
13	Vcc	14	A4

GENERAL DESCRIPTION

The MT4LC4007J(S) is specially designed to operate from 3.0V to 3.6V for low-voltage memory systems. It is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration with optional SELF REFRESH. During READ or WRITE cycles, each of the four memory bits (one bit per DQ) is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS latches the first ten bits and CAS latches the latter ten bits.

A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pins remain open (High-Z) until the next CAS cycle, which is an EARLY WRITE cycle.

The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE and OE.

PAGE ACCESS

PAGE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary.

The PAGE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates PAGE operation.

EDO PAGE MODE

The MT4LC4007J provides EDO PAGE MODE which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS goes back HIGH. EDO provides for CAS precharge time (^tCP) to occur without the output data going invalid. This elimination of CAS output control provides for pipeline READs.

PAGE MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. EDO operates as any DRAM READ or FAST-PAGE-MODE

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READ, except data will be held valid after CAS goes HIGH, as long as RAS and OE are held LOW and WE is held HIGH. OE can be brought LOW or HIGH while CAS and RAS are LOW, and the DQs will transition between valid data and High-Z. Using OE, there are two methods to disable the outputs and keep them disabled during the CAS HIGH time. The first method is to have OE HIGH when CAS transitions HIGH and keep OE HIGH for ᵗOEHC. This will tristate the DQs and they will remain tristate, regardless of OE, until CAS falls again. The second method is to have OE LOW when CAS transitions HIGH. Then OE can pulse HIGH for a minimum of ᵗOEP anytime during the CAS HIGH period and the DQs will tristate and remain tristate, regardless of OE, until CAS falls again (please reference Figure 1 for further detail on the toggling OE condition). During cycles other than PAGE-MODE READ, the outputs are disabled at ᵗOFF time after RAS and CAS are HIGH, or ᵗWHZ after WE transitions LOW. The ᵗOFF time is referenced from the rising edge of RAS or CAS, whichever occurs last. WE can also perform the function of turning off the output drivers under certain conditions, as shown in Figure 2.

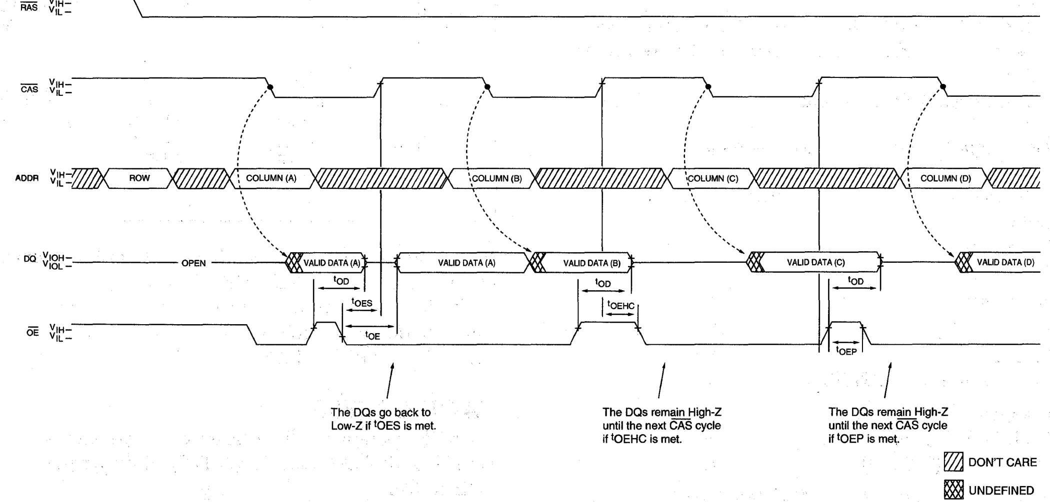

Figure 1
OUTPUT ENABLE AND DISABLE

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REFRESH

Preserve correct memory cell data by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed within ${}^tREF$ max, regardless of sequence. The CBR and SELF refresh cycles will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

An optional SELF REFRESH mode is also available on the MT4LC4007J S. The "S" option allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms. The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle, and holding $\overline{RAS}$ LOW for the specified ${}^tRASS$. Additionally, the "S" option allows for an extended refresh period of 128ms, or 125µs per row if using distributed CBR refresh. This refresh rate can be applied during normal operation, as well as during a standby or BATTERY BACKUP mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of ${}^tRPS$. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting SELF REFRESH. However, if the DRAM controller utilizes $\overline{RAS}$ only or burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

STANDBY

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time.

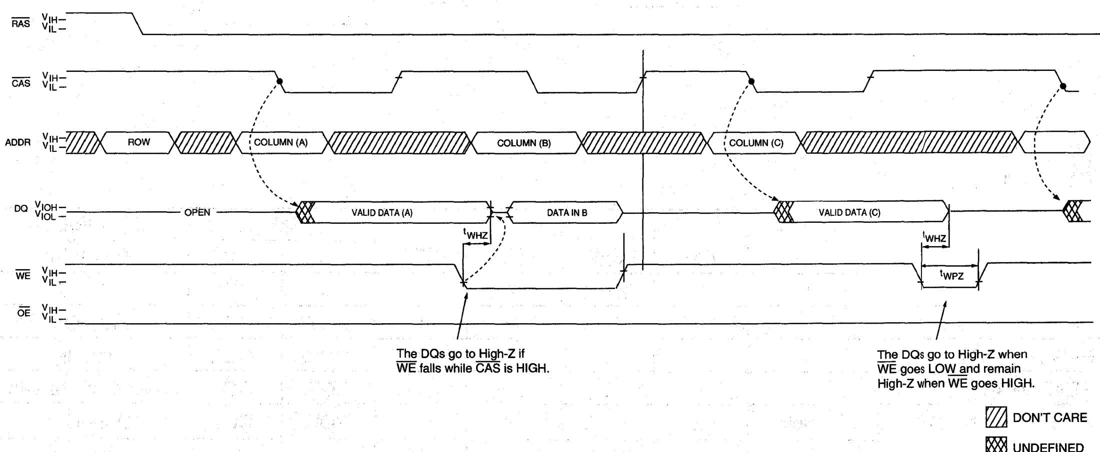

Figure 2
OUTPUT ENABLE AND DISABLE USING $\overline{WE}$

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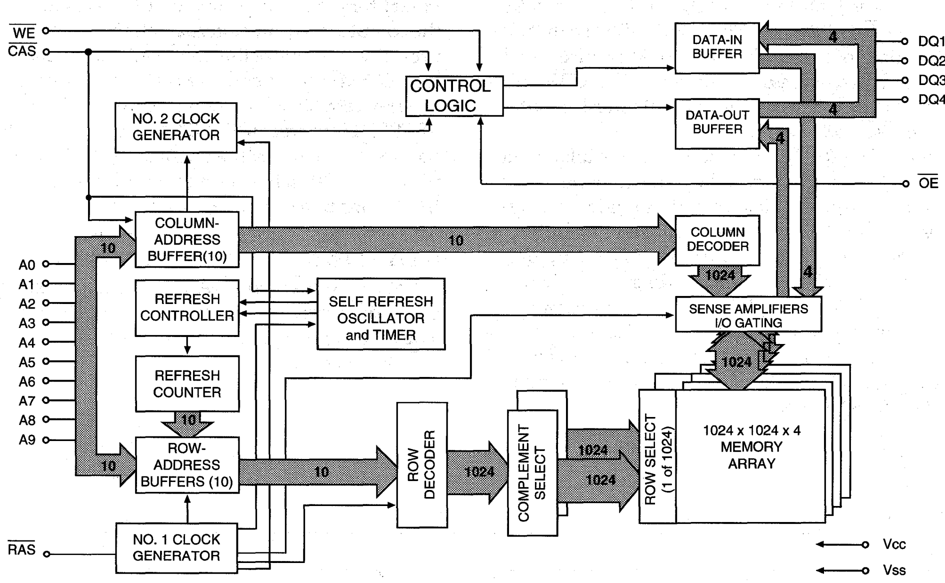
FUNCTIONAL BLOCK DIAGRAM
EDO PAGE MODE



TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE EARLY WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
EDO-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1.0V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc+0.5V (All other pins not under test = 0V)		II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ Vcc+0.5V)		IOZ	-10	10	µA	
TTL OUTPUT LEVELS	High Voltage (IOUT = -2mA)	VOH	2.4		V	
	Low Voltage (IOUT = 2mA)	VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	VERSION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC1}	1	1	1	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	MT4LC4007J	I_{CC2}	500	500	500	µA	
	MT4LC4007J S	I_{CC2}	100	100	100	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: ^tRC = ^tRC [MIN])		I_{CC3}	80	70	60	mA	3, 4, 30
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: ^tPC = ^tPC [MIN])		I_{CC4}	60	50	40	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])		I_{CC5}	80	70	60	mA	3, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: ^tRC = ^tRC [MIN])		I_{CC6}	80	70	60	mA	3, 5
EXTENDED REFRESH CURRENT: Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$= Vcc -0.2V; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	MT4LC4007J S	I_{CC7}	150	150	150	µA	3, 5, 28
SELF REFRESH CURRENT: Average power supply current during SELF REFRESH: CBR cycle with $^tRAS \geq {}^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -.2; A0-A9 and D_{IN} = Vcc -.2V or .2V (D_{IN} may be left open)	MT4LC4007J S	I_{CC8}	150	150	150	µA	5, 29

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	150		180		200		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^tPC	25		33		35		ns	
EDO-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		100		105		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Output Enable time	^tOE		15		20		20	ns	23
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	10	100,000	15	100,000	15	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	50		55		65		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (EDO PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	^tASC	3		3		3		ns	
Column-address hold time	^tCAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^{t}OFF	3	15	3	20	3	20	ns	20
$\overline{\text{WE}}$ command setup time	^{t}WCS	0		0		0		ns	21, 27
Write command hold time	^{t}WCH	10		15		15		ns	
Write command hold time (referenced to $\overline{\text{RAS}}$)	^{t}WCR	45		55		60		ns	
Write command pulse width	^{t}WP	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	^{t}RWL	15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	^{t}CWL	15		20		20		ns	
Data-in setup time	^{t}DS	0		0		0		ns	22
Data-in hold time	^{t}DH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{\text{RAS}}$)	^{t}DHR	45		55		60		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	^{t}RWD	85		100		110		ns	21
Column-address to $\overline{\text{WE}}$ delay time	^{t}AWD	55		65		70		ns	21
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	^{t}CWD	40		50		50		ns	21
Transition time (rise or fall)	^{t}T	2.5	50	2.5	50	2.5	50	ns	9, 10
Refresh period (1,024 cycles) MT4LC4007J/MT4LC4007J S	^{t}REF		16/128		16/128		16/128	ms	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	^{t}RPC	0		0		0		ns	
$\overline{\text{CAS}}$ setup time (CBR REFRESH)	^{t}CSR	10		10		10		ns	5
$\overline{\text{CAS}}$ hold time (CBR REFRESH)	^{t}CHR	10		10		10		ns	5
$\overline{\text{WE}}$ hold time (CBR REFRESH)	^{t}WRH	10		10		10		ns	25
$\overline{\text{WE}}$ setup time (CBR REFRESH)	^{t}WRP	10		10		10		ns	25
$\overline{\text{WE}}$ hold time (WCBR test cycle)	^{t}WTH	10		10		10		ns	25
$\overline{\text{WE}}$ setup time (WCBR test cycle)	^{t}WTS	10		10		10		ns	25
$\overline{\text{OE}}$ setup prior to $\overline{\text{RAS}}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
Output disable	^{t}OD		15		20		20	ns	27
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$ during READ-MODIFY-WRITE cycle	^{t}OEH	15		20		20		ns	26
$\overline{\text{RAS}}$ pulse width during SELF REFRESH cycle	^{t}RASS	100		100		100		µs	29
$\overline{\text{RAS}}$ precharge time during SELF REFRESH cycle	^{t}RPS	110		130		150		ns	29
$\overline{\text{RAS}}$ LOW to "don't care" during SELF REFRESH cycle	^{t}CHD	10		10		10		ns	29
$\overline{\text{OE}}$ HIGH hold time from $\overline{\text{CAS}}$ HIGH	^{t}OEHC	10		10		10		ns	
$\overline{\text{OE}}$ HIGH pulse width	^{t}OEP	10		10		10		ns	
Data output hold after $\overline{\text{CAS}}$ LOW	^{t}COH	5		5		5		ns	
Output disable delay from $\overline{\text{WE}}$ ($\overline{\text{CAS}}$ HIGH)	^{t}WHZ	3	15	3	15	3	15	ns	
$\overline{\text{WE}}$ pulse width for output disable when $\overline{\text{CAS}}$ HIGH	^{t}WPZ	10		10		10		ns	

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 2.5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF. Output reference voltages are 0.8V for a low level and 2.0V for a high level.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
28. Extended refresh current is reduced as ^{t}RAS is reduced from its maximum specification during the extended refresh cycle.
29. If the DRAM controller uses a BURST REFRESH, a BURST REFRESH of all rows must be executed upon exiting SELF REFRESH.
30. Column-address changed once each cycle.

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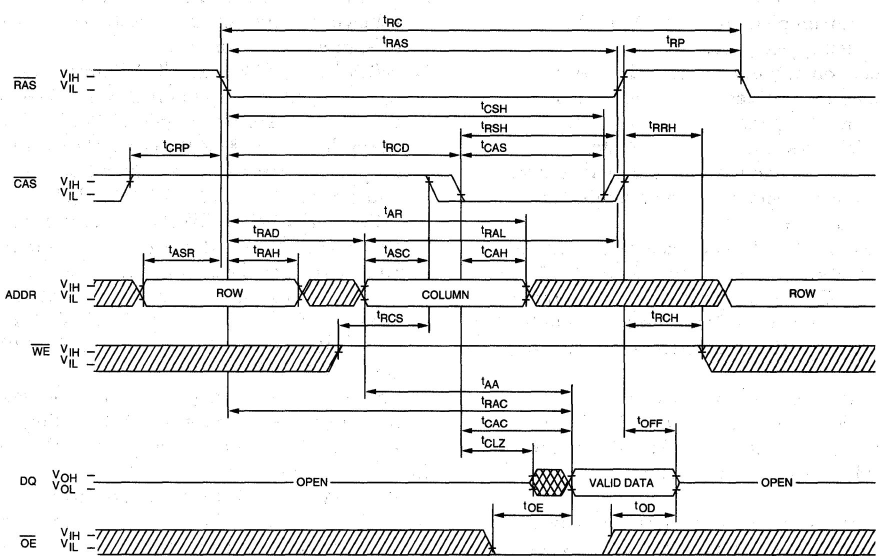
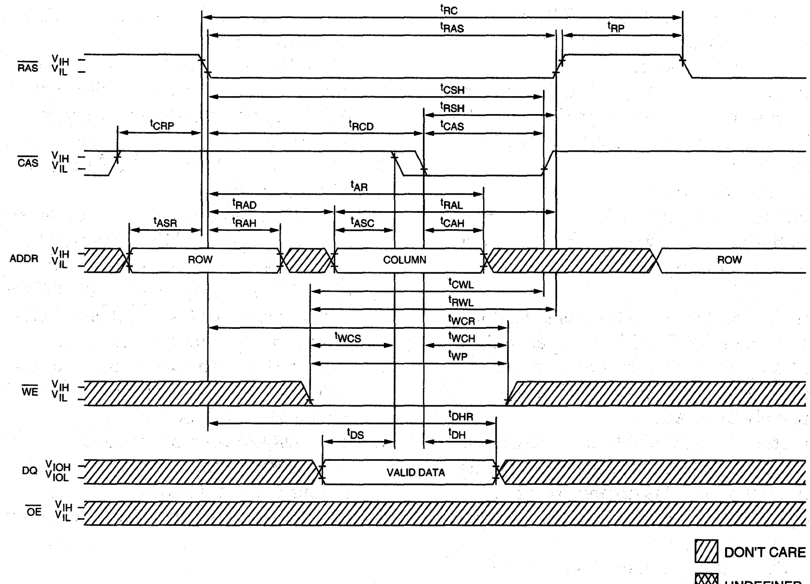
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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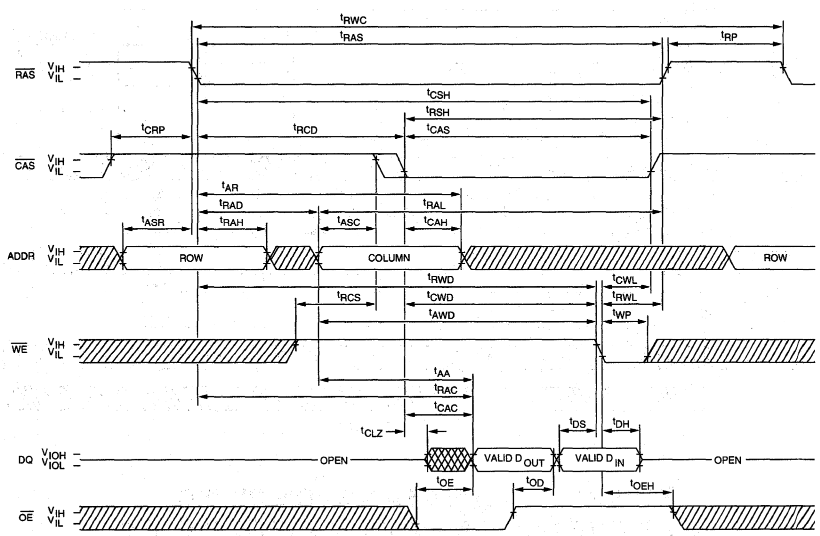
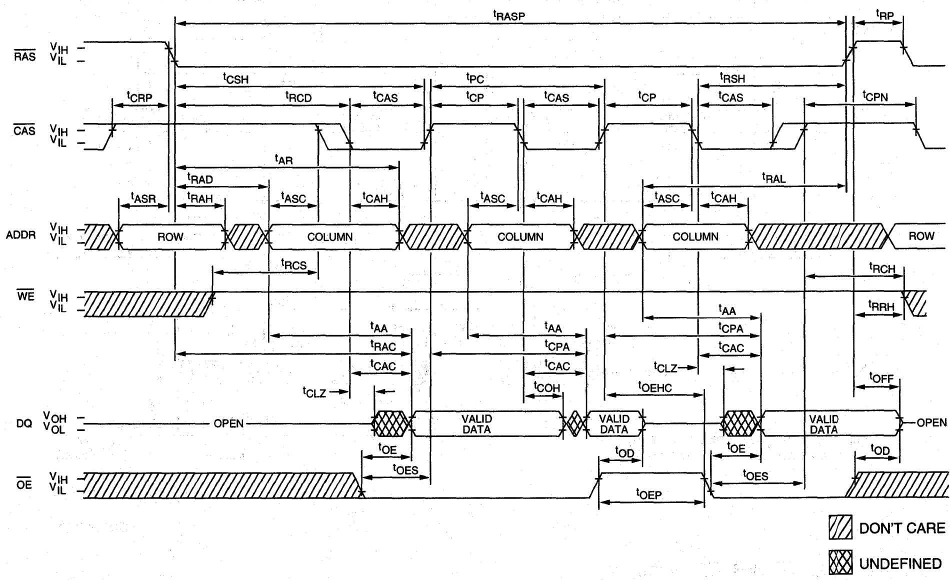
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



EDO-PAGE-MODE READ CYCLE



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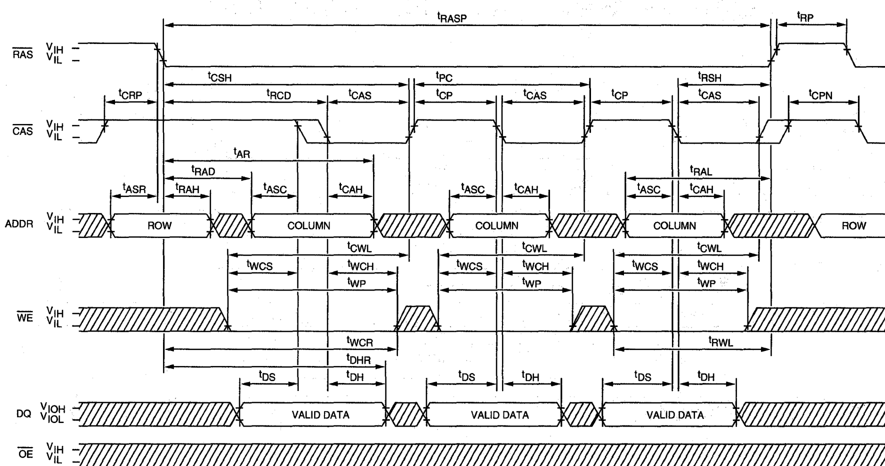
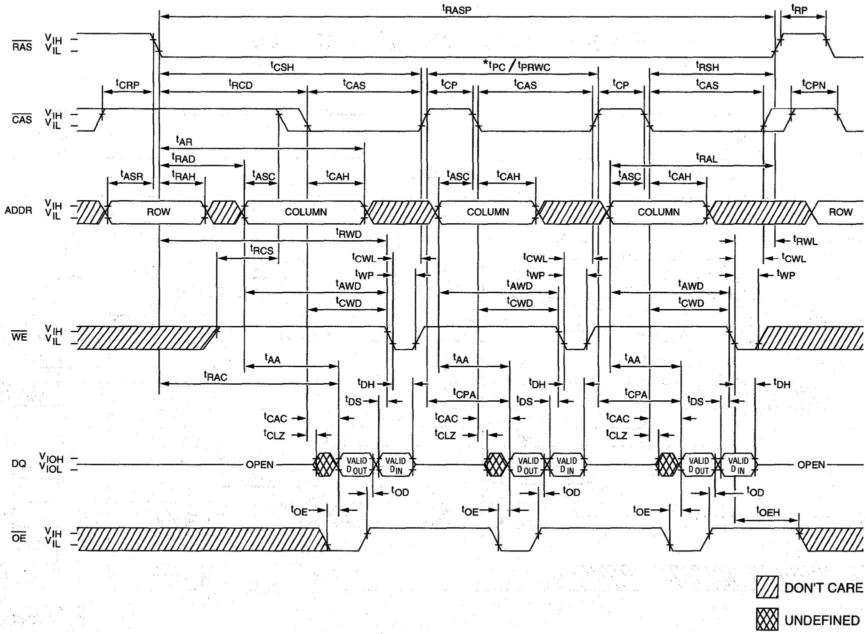
EDO-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



***NOTE:** ^{t}PC is for LATE WRITE cycles only.

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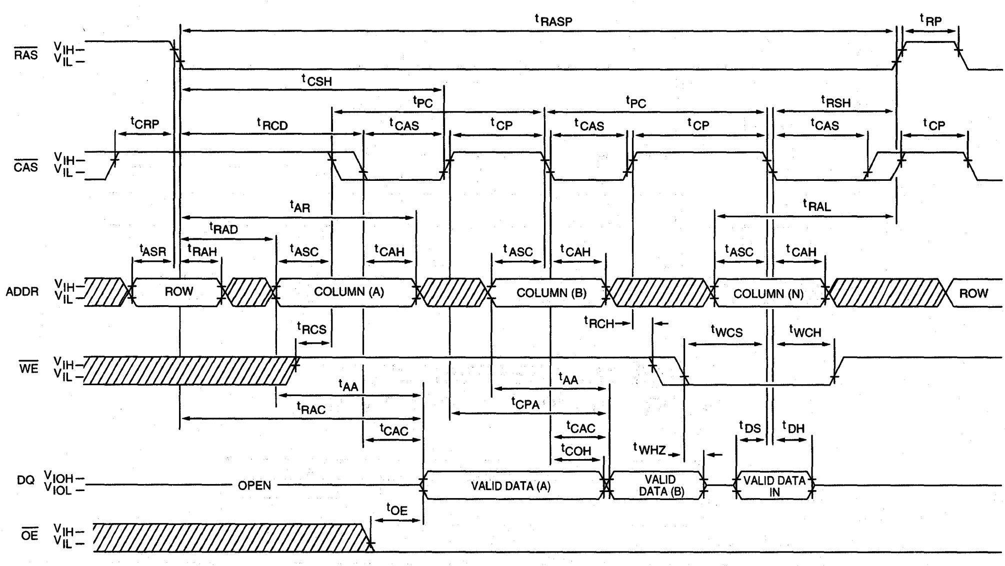
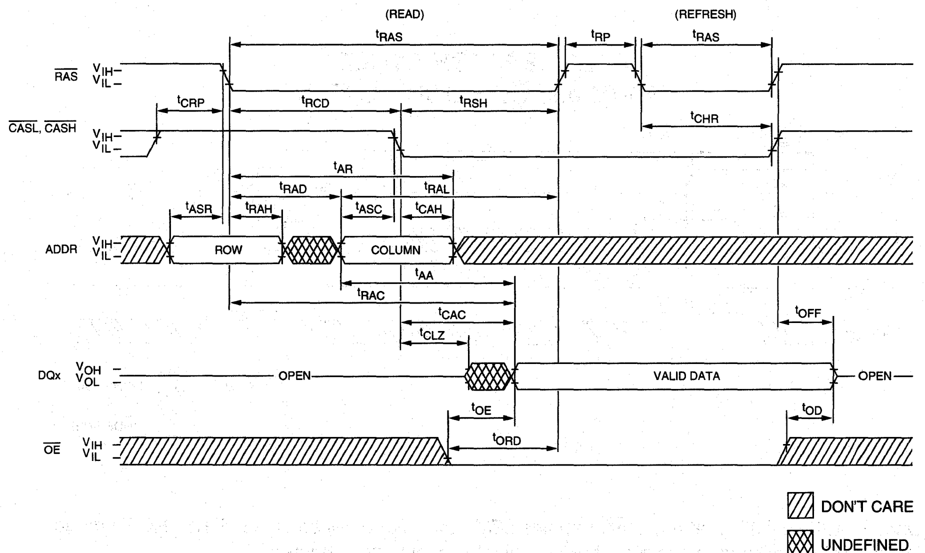
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE



HIDDEN REFRESH CYCLE [24]
(WE = HIGH; OE = LOW)



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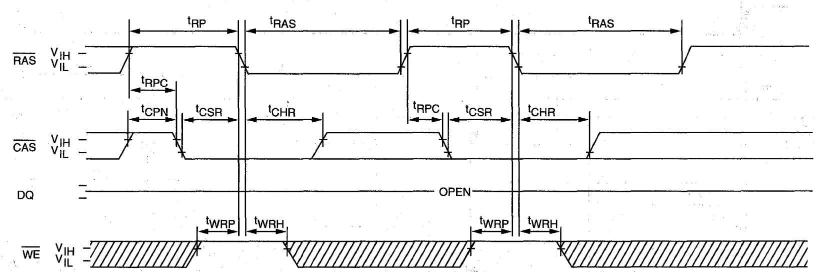
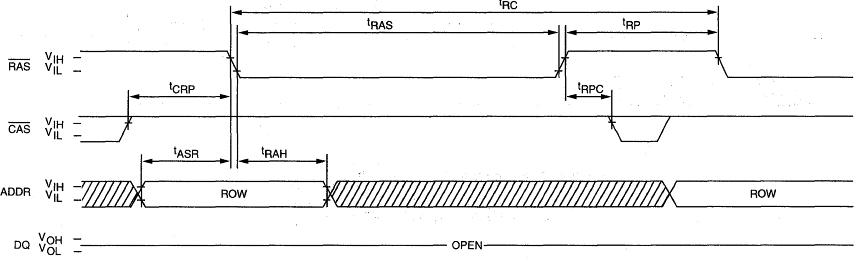
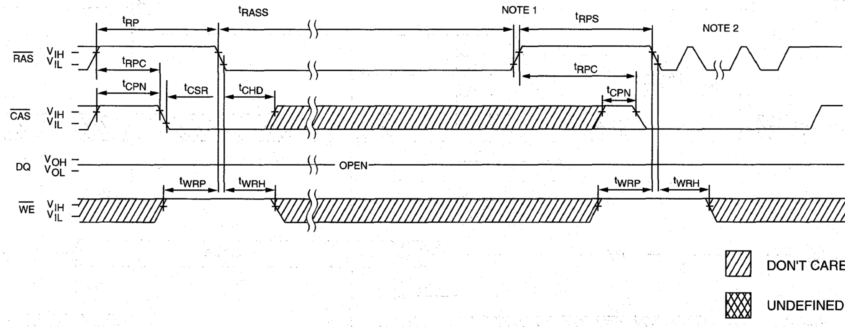
CBR REFRESH CYCLE
(A0-A9 and $\overline{OE}$ = DON'T CARE)



$\overline{RAS}$ ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{WE}$ = DON'T CARE)



SELF REFRESH CYCLE
(A0-A9 and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a complete burst of all rows should be executed.

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DRAM

4 MEG x 4 DRAM

5.0V FAST PAGE MODE

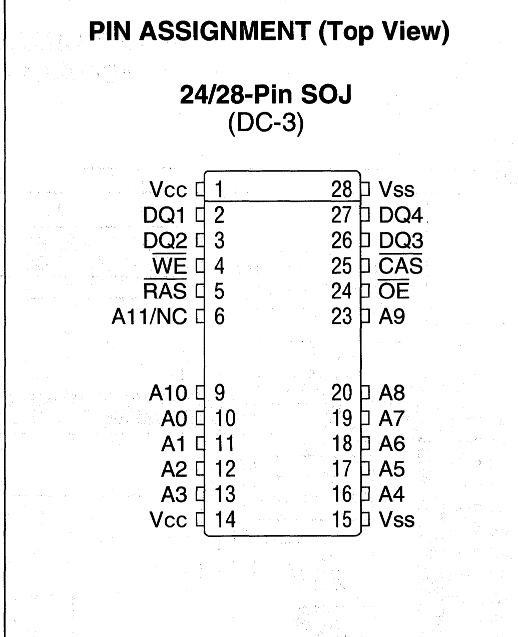
FEATURES

- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single power supply: +5V ±10%
- Low power, 3mW standby; 200mW active, typical (A1)
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms or 4,096-cycle refresh distributed across 64ms

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (400 mil)	DW
• Refresh Period	
2,048 cycles at 32ms, 11 row-addresses	B1
4,096 cycles at 64ms, 12 row-addresses	A1

- Part Number Example: MT4C4M4A1DW-6



GENERAL DESCRIPTION

The MT4C4M4A1/B1 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x4 configuration. The MT4C4M4A1 and MT4C4M4B1 are the same DRAM versions except that the MT4C4M4B1 has a 2,048-cycle refresh instead of a 4,096-cycle refresh. All further references made to the MT4C4M4A1 also apply to the MT4C4M4B1 unless specifically stated otherwise. For a device with a 2,048-cycle refresh, RAS is used to latch the first 11 bits and CAS the latter 11 bits. For a device with a 4,096-cycle refresh, RAS is used to latch the first 12 bits and CAS the latter 10 bits (A10 and A11 are "don't care" bits). READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pins remain open (High- Z) until the next CAS cycle. If WE goes LOW after data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE and OE.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0 -A9/10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the

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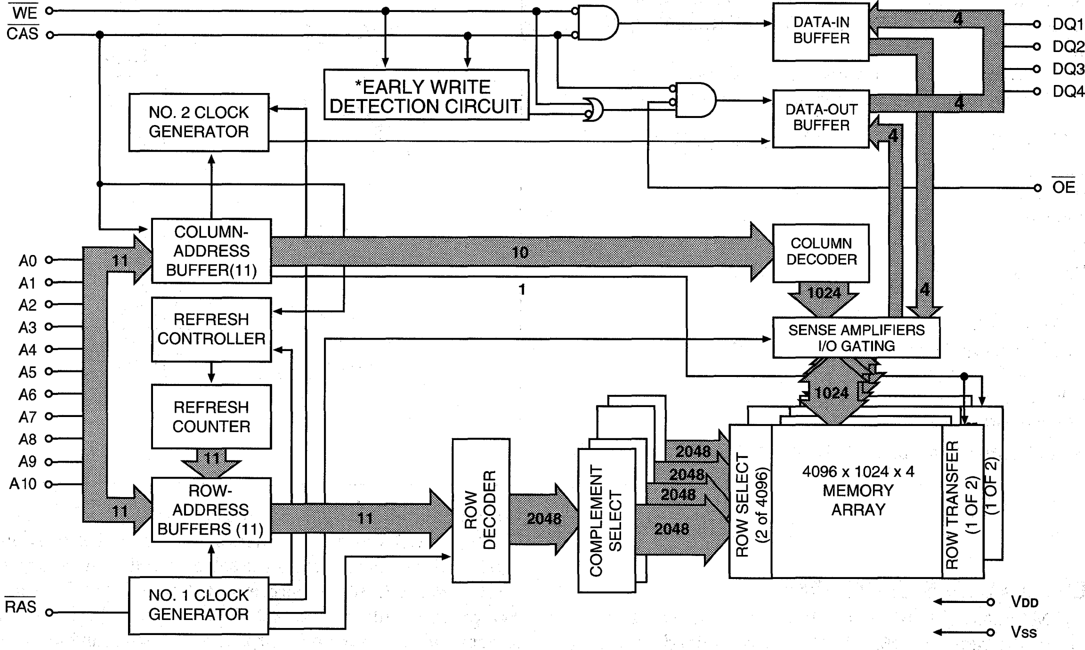
RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR, or HIDDEN) so that all 2,048/4,096 combinations of RAS addresses (A0 -A10/A11) are executed at least every 32ms/ 64ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

If CBR REFRESH is used, the number of cycles is a "don't care."

FUNCTIONAL BLOCK DIAGRAM
MT4C4M4B1 (11 row-addresses)



***NOTE:** 1. If WE goes LOW prior to CAS going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If CAS goes LOW prior to WE going LOW, EW detection circuit output is a LOW (LATE WRITE).

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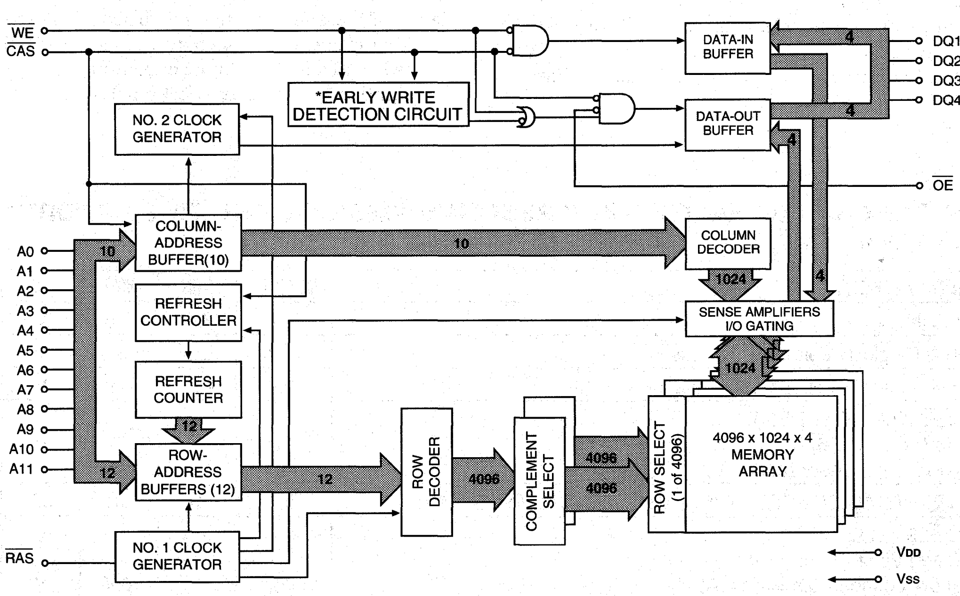
FUNCTIONAL BLOCK DIAGRAM
MT4C4M4A1 (12 row-addresses)



***NOTE:** 1. If WE goes LOW prior to CAS going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If CAS goes LOW prior to WE going LOW, EW detection circuit output is a LOW (LATE WRITE).

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z

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DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss (5.0V) .. -1.0V to +7.0V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic).................... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

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DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%), 4,096-cycle refresh

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	90	80	mA	3, 4, 28, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	70	60	mA	3, 4, 28, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	90	80	mA	3, 28, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	90	80	mA	3, 5, 28

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%), 2,048-cycle refresh

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	120	110	mA	3, 4, 27, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	90	80	mA	3, 4, 27, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	120	110	mA	3, 27, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	120	110	mA	3, 5, 27

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DRAM

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Addresses	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +5V±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	
READ WRITE cycle time	^tRWC	150		180		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		ns	
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15
Output Enable	^tOE		15		20	ns	23
Access time from column-address	^tAA		30		35	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	29
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 29

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command setup time	${}^tWCS$	0		0		ns	21, 27
Write command hold time	${}^tWCH$	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	${}^tWCR$	45		55		ns	
Write command pulse width	${}^tWP$	10		15		ns	
Write command to $\overline{RAS}$ lead time	${}^tRWL$	15		20		ns	
Write command to $\overline{CAS}$ lead time	${}^tCWL$	15		20		ns	
Data-in setup time	${}^tDS$	0		0		ns	22
Data-in hold time	${}^tDH$	10		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	${}^tDHR$	45		55		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	${}^tRWD$	85		95		ns	21
Column-address to $\overline{WE}$ delay time	${}^tAWD$	55		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	${}^tCWD$	40		45		ns	21
Transition time (rise or fall)	${}^tT$	3	50	3	50	ns	9, 10
Refresh period (2,048/4,096 cycles)	${}^tREF$		32/64		32/64	ms	26
$\overline{RAS}$ to $\overline{CAS}$ precharge time	${}^tRPC$	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	${}^tCSR$	5		5		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	${}^tCHR$	15		15		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	${}^tWRH$	10		10		ns	25
$\overline{WE}$ setup time (CBR REFRESH)	${}^tWRP$	10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	${}^tWTH$	10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	${}^tWTS$	10		10		ns	25
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	${}^tORD$	0		0		ns	
Output disable	${}^tOD$	3	15	3	20	ns	29
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	${}^tOEH$	15		15		ns	

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%;f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. 32ms is 2,048-cycle refresh; 64ms is 4,096-cycle refresh.
27. 2,048-row refresh.
28. 4,096-row refresh.
29. The 3ns minimum is a parameter guaranteed by design.
30. Column-address changed once each cycle.

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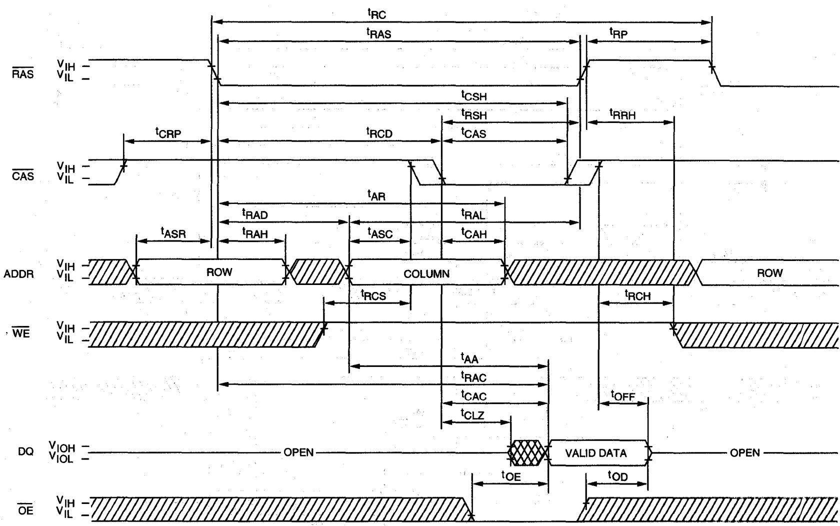
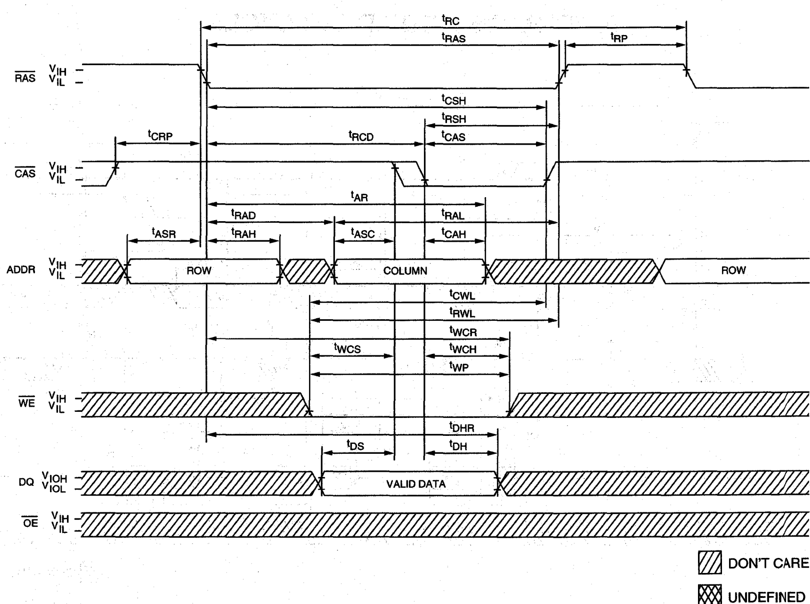
DRAM

READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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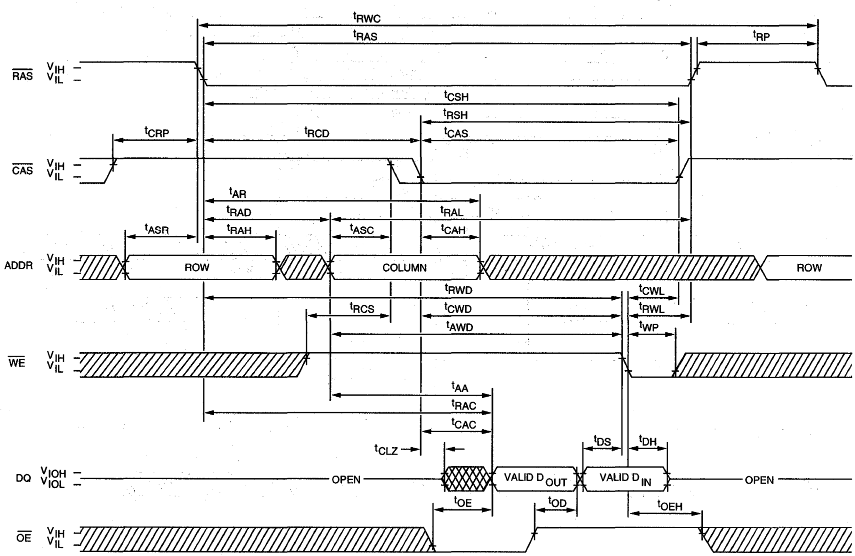
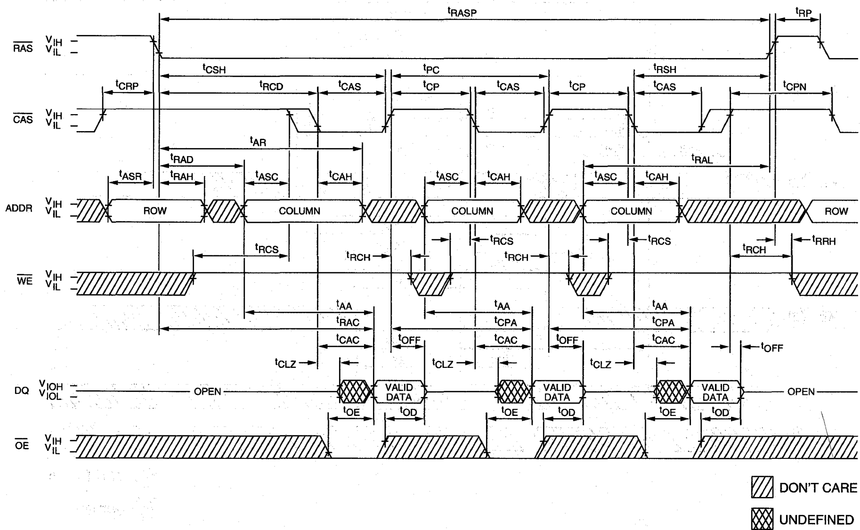
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



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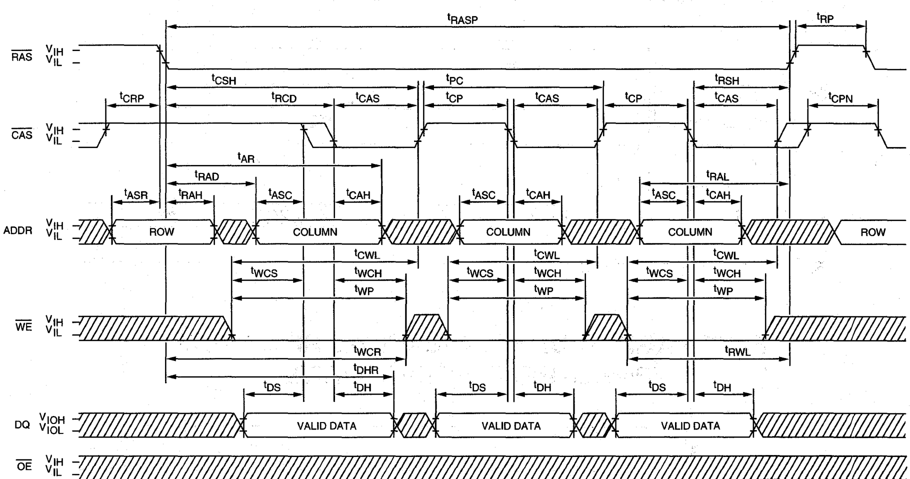
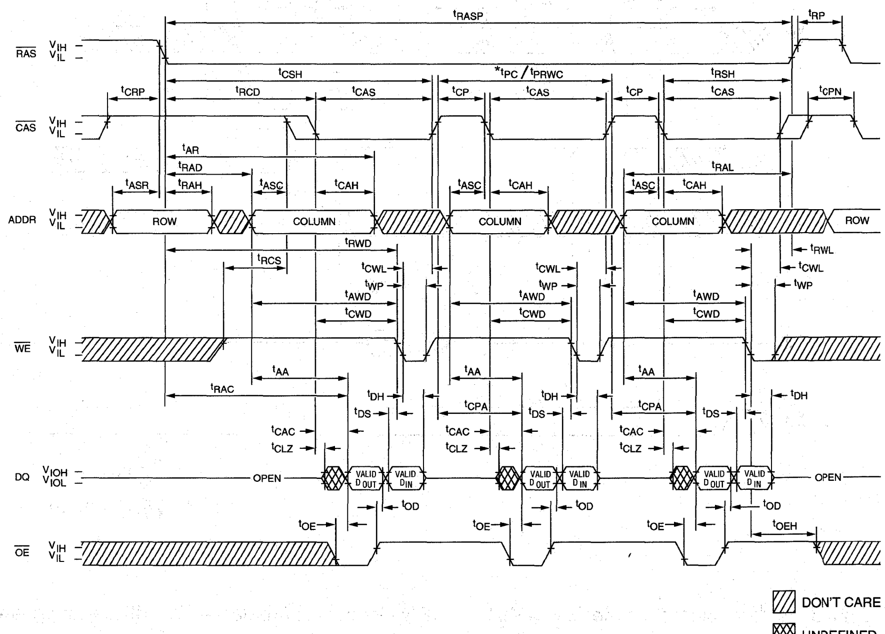
DRAM

FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



*tPC is for LATE WRITE only.

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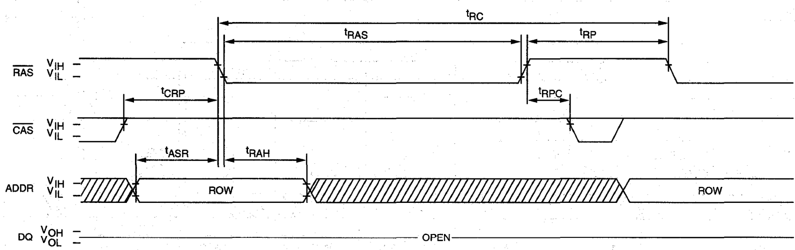
DRAM

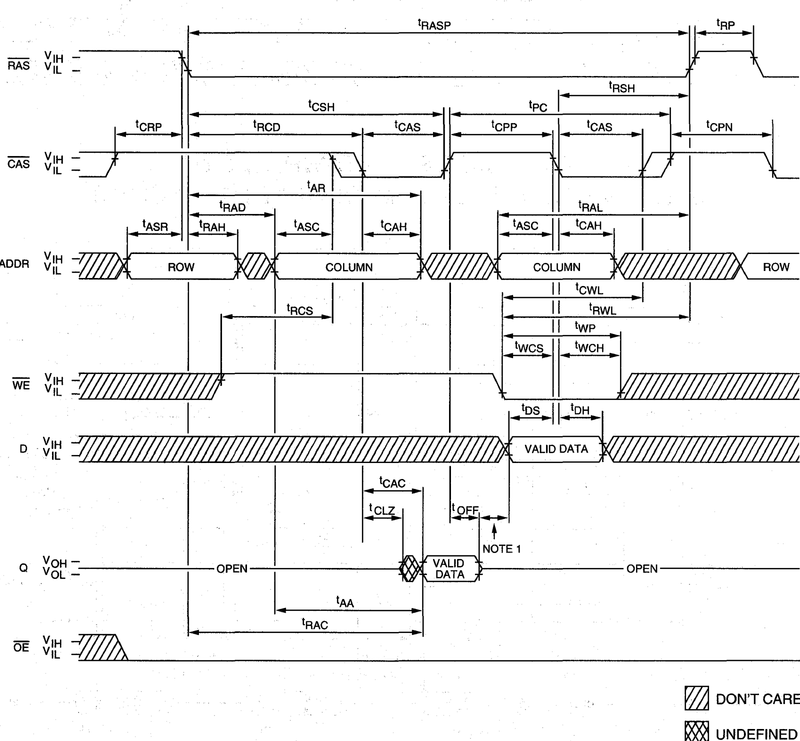
RAS ONLY REFRESH CYCLE

(ADDR = A0-A10, A11; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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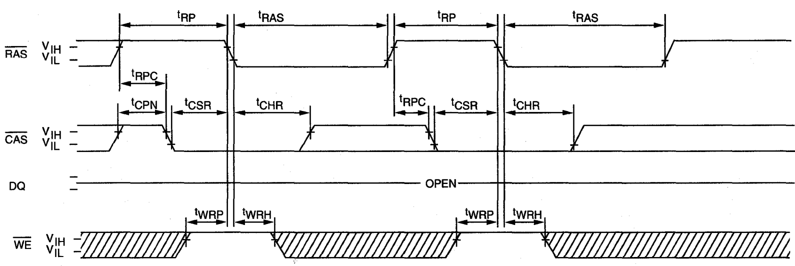
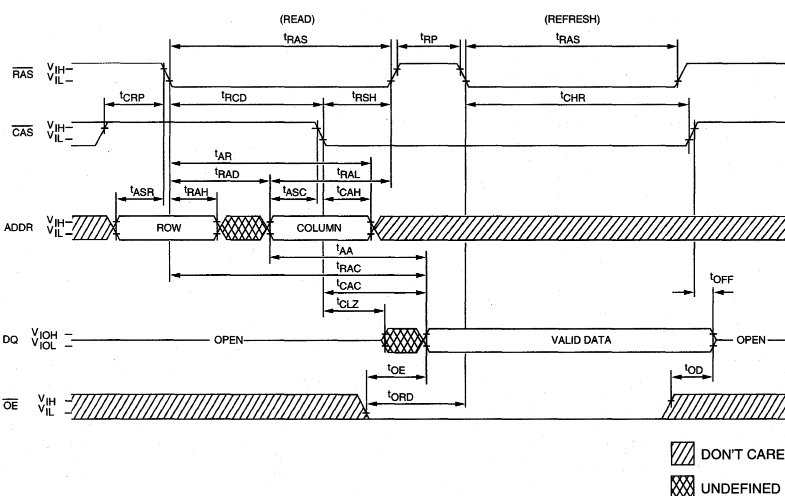
DRAM

CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



DON'T CARE

UNDEFINED

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DRAM

4 MEG x 4 DRAM

5.0V FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single power supply: +5.0V ±10%
- Low power, 1mW standby; 275mW active, typical (B1)
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and SELF
- 2,048-cycle (11 row, 11 column addresses) or 4,096-cycle (12 row, 10 column addresses)
- Optional SELF REFRESH mode, with Extended Refresh rate (4X)

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG
• Refresh	
Standard	none
Self refresh	S
• Refresh Period	
2,048 cycles at 32ms	B1
4,096 cycles at 64ms	A1
2,048 cycles at 128ms	B1 S

- Part Number Example: MT4C4M4B1DJ-6 S

PIN ASSIGNMENT (Top View)

24/26-Pin SOJ (DC-2) and 24/26-Pin TSOP (DD-2)

Pin	Name	Pin	Name
1	Vcc	26	Vss
2	DQ1	25	DQ4
3	DQ2	24	DQ3
4	WE	23	CAS
5	RAS	22	OE
6	A11/NC	21	A9
8	A10	19	A8
9	A0	18	A7
10	A1	17	A6
11	A2	16	A5
12	A3	15	A4
13	Vcc	14	Vss

GENERAL DESCRIPTION

The MT4C4M4A1/B1(S) are randomly accessed solid-state memories containing 16,777,216 bits organized in a x4 configuration. The MT4C4M4A1 and MT4C4M4B1 are the same DRAM versions except that the MT4C4M4B1 has a 2,048-cycle refresh instead of a 4,096-cycle refresh. All further references made to the MT4C4M4A1 also apply to the MT4C4M4B1 unless specifically stated otherwise. For a device with a 2,048-cycle refresh, RAS is used to latch the first 11 bits and CAS the latter 11 bits. For a device with a 4,096-cycle refresh, RAS is used to latch the first 12 bits and CAS the latter 10 bits (A10 and A11 are "don't care" bits).

READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pins remain open (High- Z) until the next CAS cycle.

If WE goes LOW after data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE and OE.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

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REFRESH

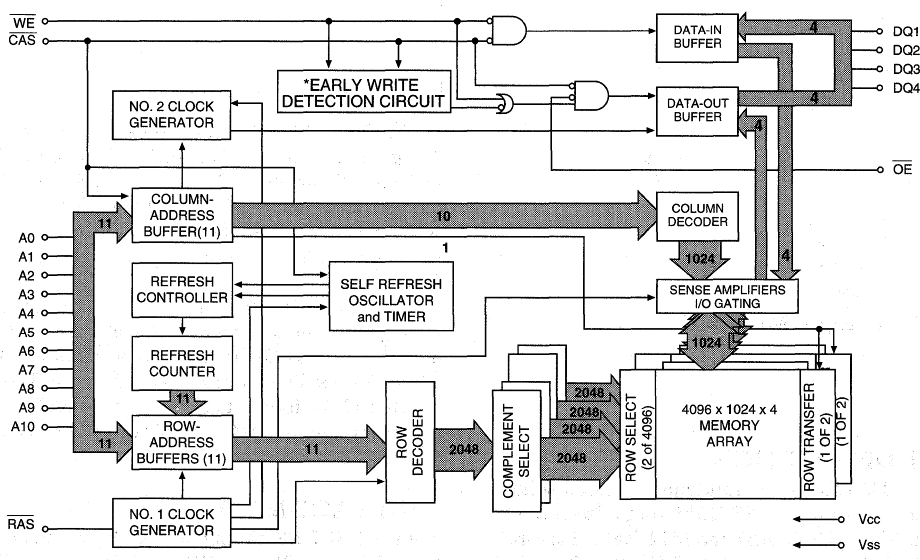
Preserve correct memory cell data by maintaining power and executing a RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR, or HIDDEN) so that all 2,048/4,096 combinations of RAS addresses are executed at least every 32ms/64ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

An optional SELF REFRESH mode is also available on the MT4C4M4B1 S. The "S" option allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms (B1) four times longer than the standard 32ms (B1) specification.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified ᵗRASS. Additionally, the "S" option allows for an extended refresh rate of 62.5µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby or BATTERY BACKUP mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ᵗRPS (≈ᵗRCns). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or BURST REFRESH sequence, all 2,048 (B1) rows must be refreshed within 300µs prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM
MT4C4M4B1 (11 row-addresses)



***NOTE:** 1. If WE goes LOW prior to CAS going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If CAS goes LOW prior to WE going LOW, EW detection circuit output is a LOW (LATE WRITE).
3. SELF REFRESH oscillator and timer - S option only.

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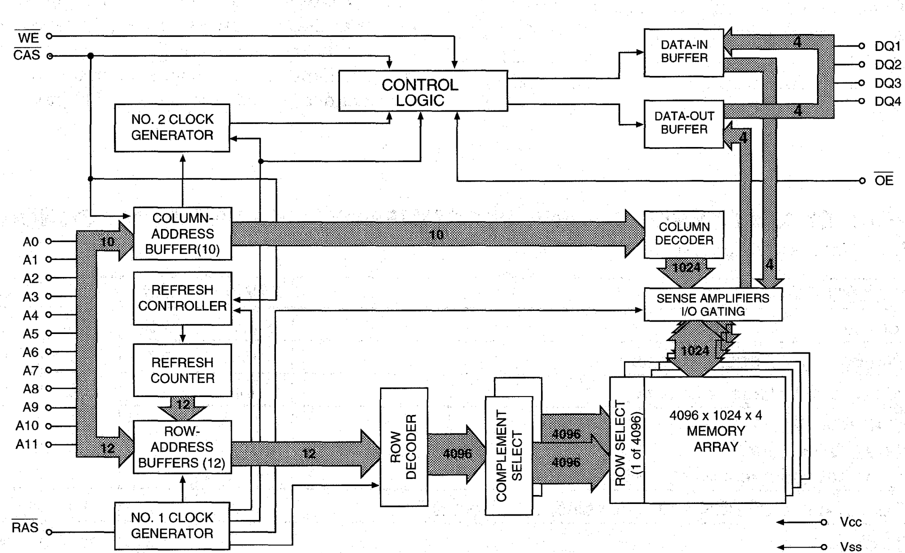
FUNCTIONAL BLOCK DIAGRAM
MT4C4M4A1 (12 row-addresses)



***NOTE:** 1. If WE goes LOW prior to CAS going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If CAS goes LOW prior to WE going LOW, EW detection circuit output is a LOW (LATE WRITE).

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

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NEW DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1.0V to +7.0V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 5.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5.0mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5.0V ±10%), 2,048-cycle refresh

PARAMETER/CONDITION	VERSION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = V_{IH})		I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = V_{CC} -0.2V)	MT4C4M4B1	I_{CC2}	1	1	mA	
	MT4C4M4B1(S)	I_{CC2}	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])		I_{CC3}	120	110	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V_{IL}, CAS, Address Cycling: ${}^tPC$ = ${}^tPC$ [MIN])		I_{CC4}	90	80	mA	3, 4, 27, 30
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = V_{IH}: ${}^tRC$ = ${}^tRC$ [MIN])		I_{CC5}	120	110	mA	3, 30
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])		I_{CC6}	120	110	mA	3, 5
REFRESH CURRENT: Extended Average power supply current, CAS = 0.2V or CBR cycling; RAS = ${}^tRAS$(MIN); WE = 0.2V; A0-A11 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open); ${}^tRC$ = 62.5µs	MT4C4M4B1 S	I_{CC7}	300	300	µA	3, 5
REFRESH CURRENT: SELF Average power supply current, CBR cycling with RAS ≥ ${}^tRASS$ (MIN)and CAS held LOW; WE = V_{CC}-0.2V; A0-A11 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	MT4C4M4B1 S	I_{CC8}	300	300	µA	5

(Notes: 1, 6, 7) (V_{CC} = +5.0V ±10%), 4,096-cycle refresh

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC3}	100	90	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V_{IL}, CAS, Address Cycling: ${}^tPC$ = ${}^tPC$ [MIN])	I_{CC4}	80	70	mA	3, 4, 30
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = V_{IH}: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC5}	100	90	mA	3, 30
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC6}	100	90	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +5.0V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
READ WRITE cycle time	^{t}RWC	150		180		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	85		95		ns	
Access time from $\overline{RAS}$	^{t}RAC		60		70	ns	14
Access time from $\overline{CAS}$	^{t}CAC		15		20	ns	15
Output Enable	^{t}OE		15		20	ns	23
Access time from column-address	^{t}AA		30		35	ns	
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40	ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	^{t}RSH	15		20		ns	
$\overline{RAS}$ precharge time	^{t}RP	40		50		ns	
$\overline{CAS}$ pulse width	^{t}CAS	15	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^{t}CSH	60		70		ns	
$\overline{CAS}$ precharge time (CBR REFRESH)	^{t}CPN	10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^{t}CP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	45	20	50	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	5		5		ns	
Row-address setup time	^{t}ASR	0		0		ns	
Row-address hold time	^{t}RAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	30	15	35	ns	18
Column-address setup time	^{t}ASC	0		0		ns	
Column-address hold time	^{t}CAH	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	50		55		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		ns	
Read command setup time	^{t}RCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	3		3		ns	28
Output buffer turn-off delay	^{t}OFF	3	15	3	20	ns	20, 28

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5.0V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command setup time	tWCS	0		0		ns	21
Write command hold time	tWCH	10		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		ns	
Write command pulse width	tWP	10		15		ns	
Write command to RAS lead time	tRWL	15		20		ns	
Write command to CAS lead time	tCWL	15		20		ns	
Data-in setup time	tDS	0		0		ns	22
Data-in hold time	tDH	10		15		ns	22
Data-in hold time (referenced to RAS)	tDHR	45		55		ns	
RAS to WE delay time	tRWD	85		95		ns	21
Column-address to WE delay time	tAWD	55		60		ns	21
CAS to WE delay time	tCWD	40		45		ns	21
Transition time (rise or fall)	tT	3	50	3	50	ns	9, 10
Refresh period (2,048/4,096 cycles)	tREF		32/64		32/64	ms	26
Refresh period - S option (2,048 cycles)	tREF		128		128	ms	27
RAS to CAS precharge time	tRPC	0		0		ns	
CAS setup time (CBR REFRESH)	tCSR	5		5		ns	5
CAS hold time (CBR REFRESH)	tCHR	15		15		ns	5
WE hold time (CBR REFRESH)	tWRH	10		10		ns	25
WE setup time (CBR REFRESH)	tWRP	10		10		ns	25
WE hold time (WCBR test cycle)	tWTH	10		10		ns	25
WE setup time (WCBR test cycle)	tWTS	10		10		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		ns	
Output disable	tOD	3	15	3	20	ns	28
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		15		ns	
RAS pulse width entering SELF REFRESH	tRASS	100		100		µs	27, 29
RAS precharge time exiting SELF REFRESH	tRPS	110		130		ns	27, 29
CAS hold time entering SELF REFRESH	tCHD	15		15		ns	27, 29

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5.0V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY WRITE cycles. ^tRWD, ^tAWD and ^tCWD apply to READ-MODIFY-WRITE cycles. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
26. 32ms is a 2,048-cycle refresh, 64ms is a 4,096-cycle refresh.
27. 2,048-row refresh.
28. The 3ns minimum is a parameter guaranteed by design.
29. Refresh must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in the active mode). Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.
30. Column-address changed once each cycle.

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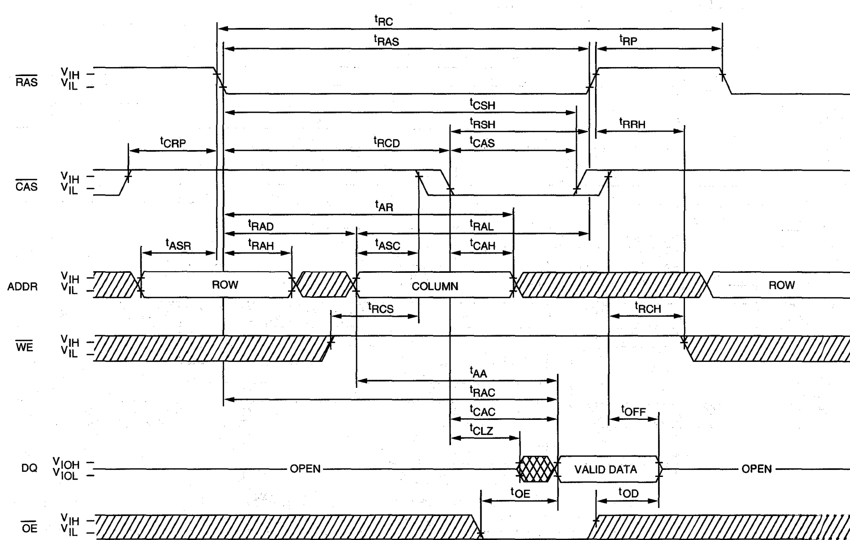
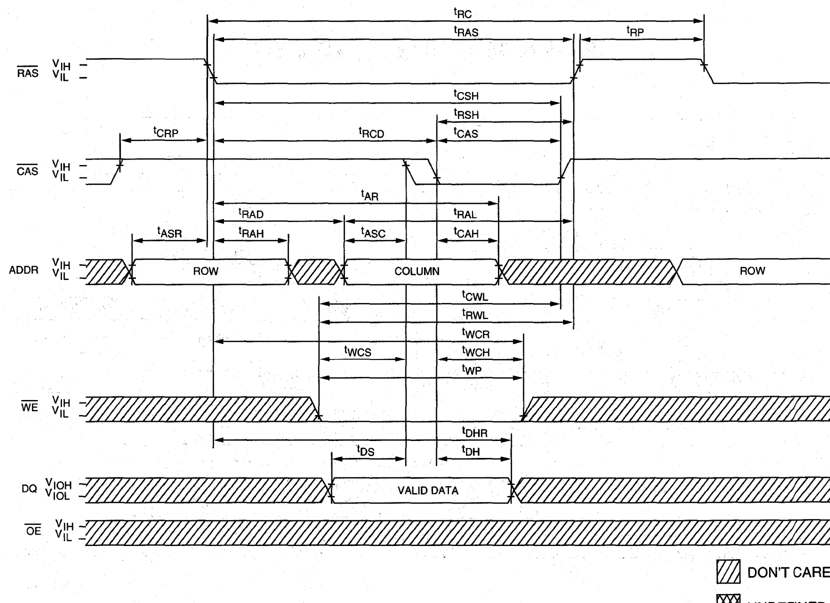
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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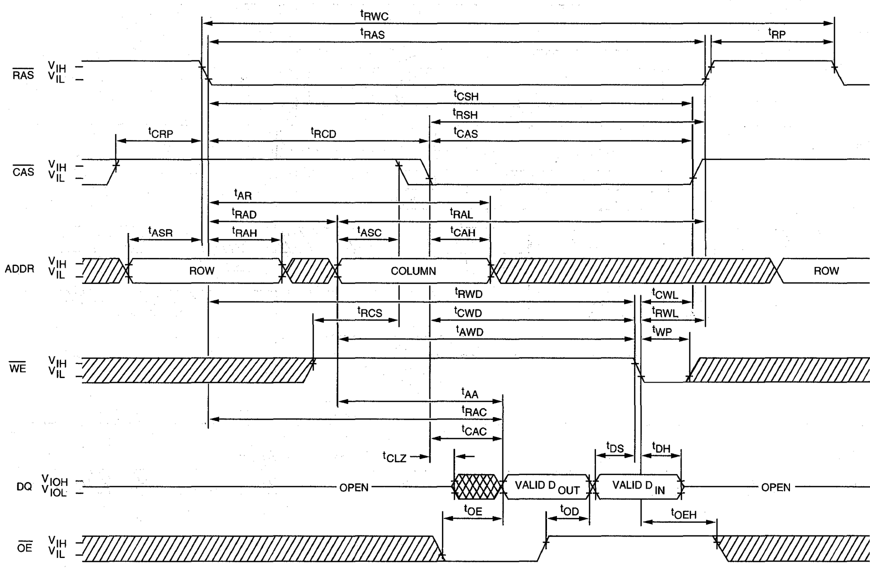
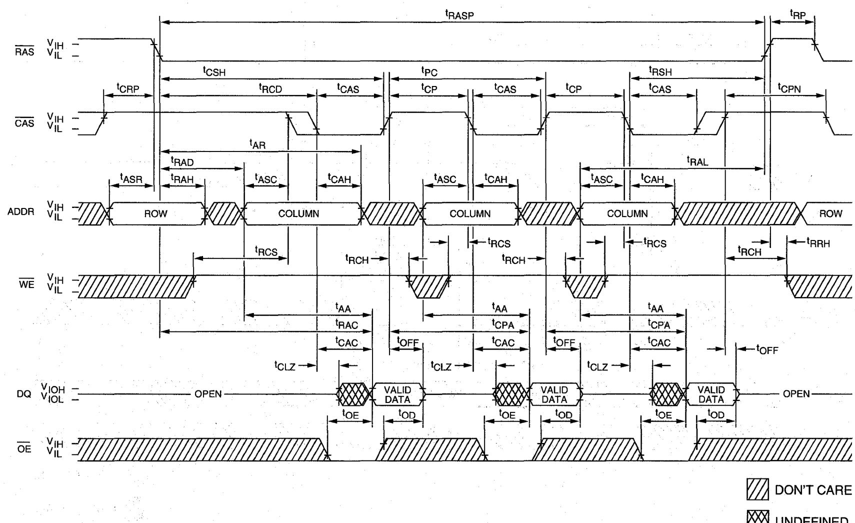
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

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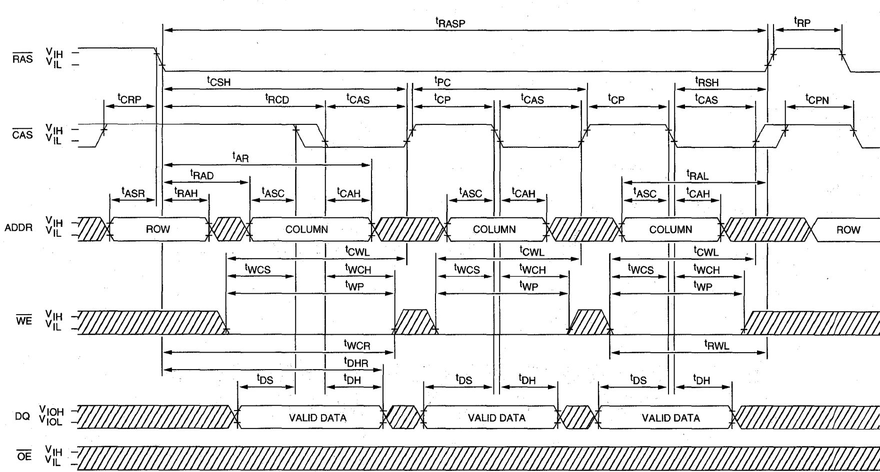
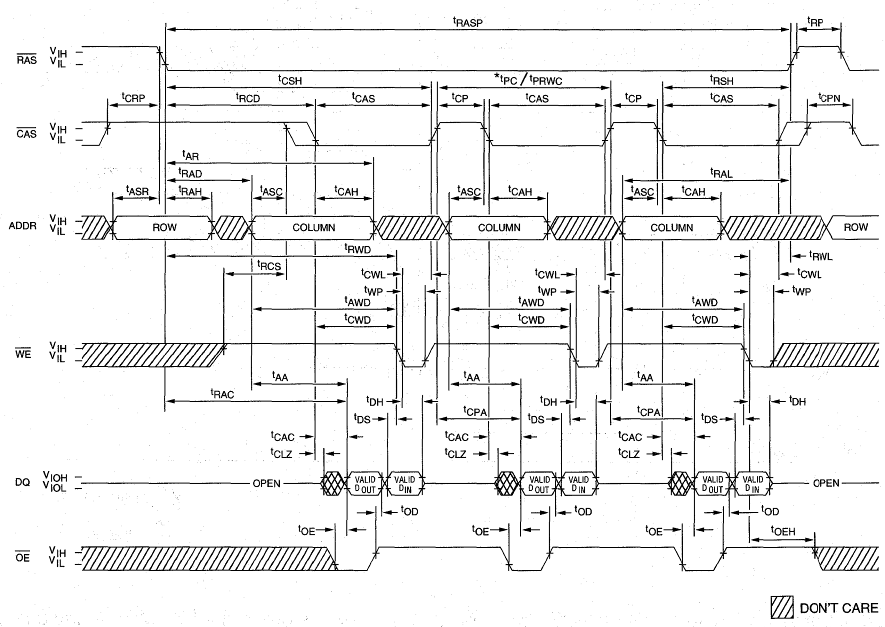
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



*tPC is for LATE WRITE only.

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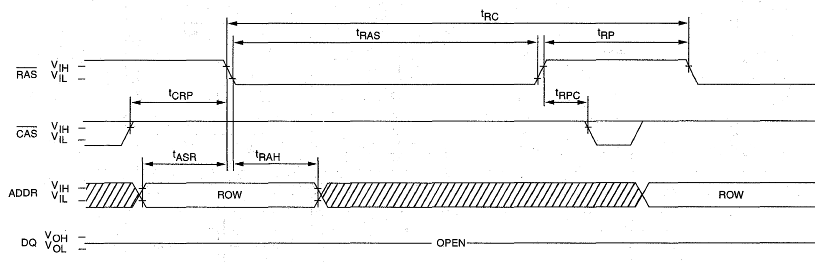
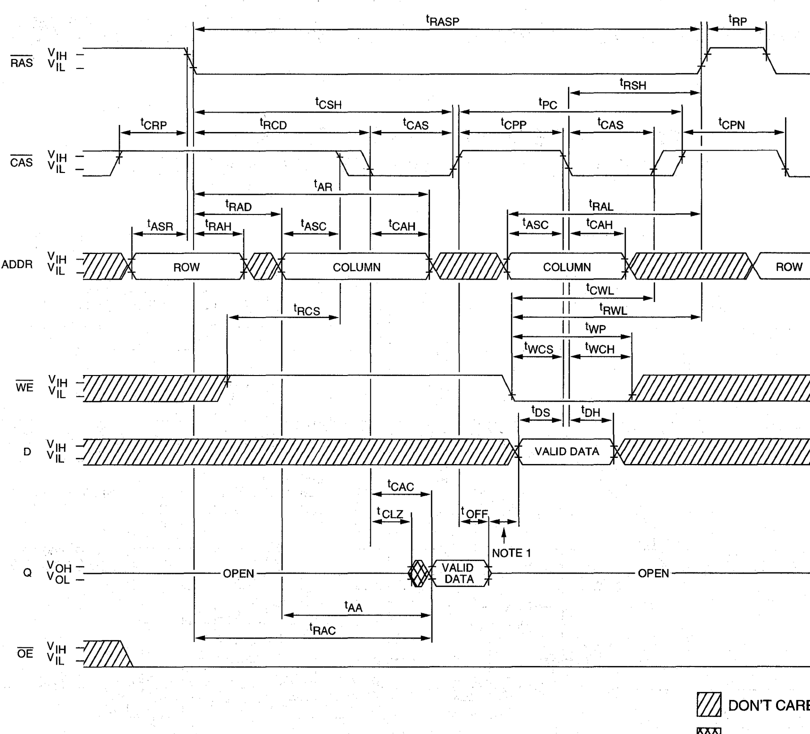
RAS ONLY REFRESH CYCLE

(ADDR = A0-A10, A11; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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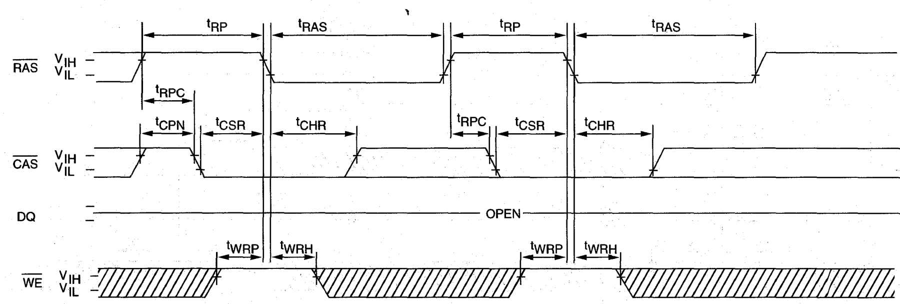
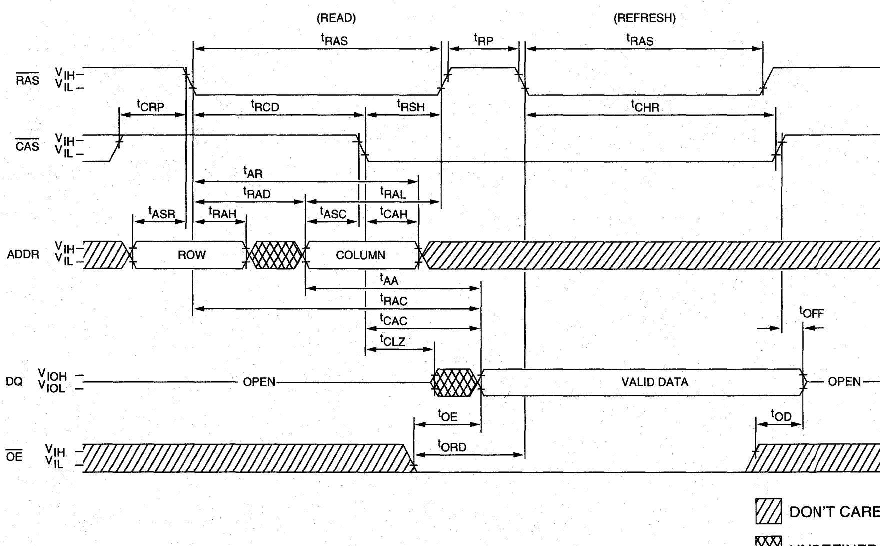
CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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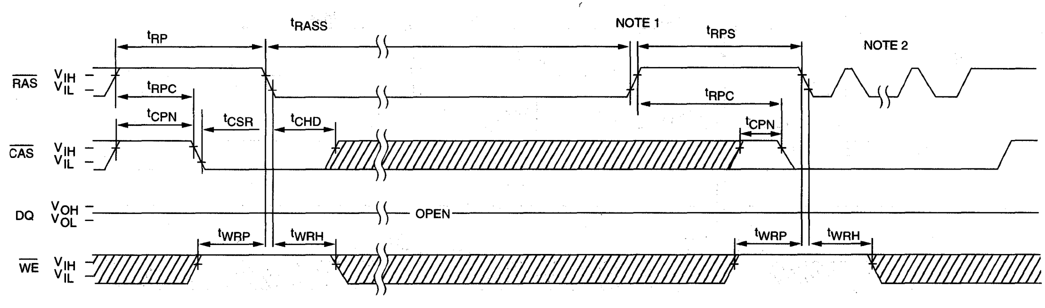
SELF REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once ^tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^tRPS is satisfied, a complete burst of all rows should be executed.

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DRAM

4 MEG x 4 DRAM

3.3V FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single power supply: +3.3V ±0.3V
- Low power, 0.4mW standby; 180mW active, typical (B1)
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and SELF
- 2,048-cycle (11 row, 11 column addresses) or 4,096-cycle (12 row, 10 column addresses)
- Optional SELF REFRESH mode, with Extended Refresh rate (4X)

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG
• Refresh	
Standard	none
Self refresh	S
• Refresh Period	
2,048 cycles at 32ms	B1
4,096 cycles at 64ms	A1
2,048 cycles at 128ms	B1 S

- Part Number Example: MT4LC4M4B1DJ-6 S

PIN ASSIGNMENT (Top View)

24/26-Pin SOJ (DC-2) and **24/26-Pin TSOP (DD-2)** (identical pinout)

Pin	Signal	Pin	Signal
1	Vcc	26	Vss
2	DQ1	25	DQ4
3	DQ2	24	DQ3
4	WE	23	CAS
5	RAS	22	OE
6	A11/NC	21	A9
8	A10	19	A8
9	A0	18	A7
10	A1	17	A6
11	A2	16	A5
12	A3	15	A4
13	Vcc	14	Vss

GENERAL DESCRIPTION

The MT4LC4M4A1/B1(S) are randomly accessed solid-state memories containing 16,777,216 bits organized in a x4 configuration. The MT4LC4M4A1 and MT4LC4M4B1 are the same DRAM versions except that the MT4LC4M4B1 has a 2,048-cycle refresh instead of a 4,096-cycle refresh. All further references made to the MT4LC4M4A1 also apply to the MT4LC4M4B1 unless specifically stated otherwise. For a device with a 2,048-cycle refresh, RAS is used to latch the first 11 bits and CAS the latter 11 bits. For a device with a 4,096-cycle refresh, RAS is used to latch the first 12 bits and CAS the latter 10 bits (A10 and A11 are "don't care" bits).

READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pins remain open (High- Z) until the next CAS cycle.

If WE goes LOW after data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE and OE.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

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REFRESH

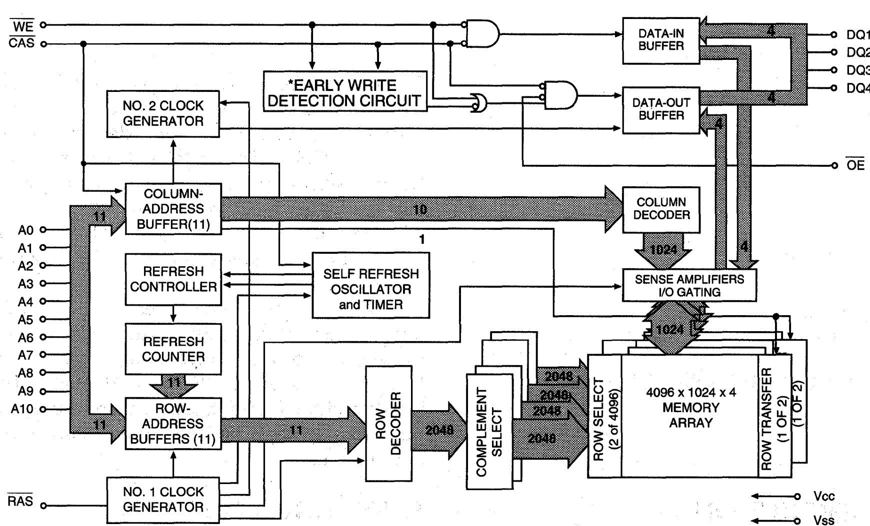
Preserve correct memory cell data by maintaining power and executing a $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 2,048/4,096 combinations of $\overline{RAS}$ addresses are executed at least every 32ms/64ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

An optional SELF REFRESH mode is also available on the MT4LC4M4B1 S. The "S" option allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms (B1) four times longer than the standard 32ms (B1) specification.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified ^{t}RASS. Additionally, the "S" option allows for an extended refresh rate of 62.5µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of ^{t}RPS ($\approx {}^{t}$RCns). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or BURST REFRESH sequence, all 2,048 (B1) rows must be refreshed within 300µs prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM
MT4LC4M4B1 (11 row-addresses)



***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).
3. SELF REFRESH oscillator and timer - S option only.

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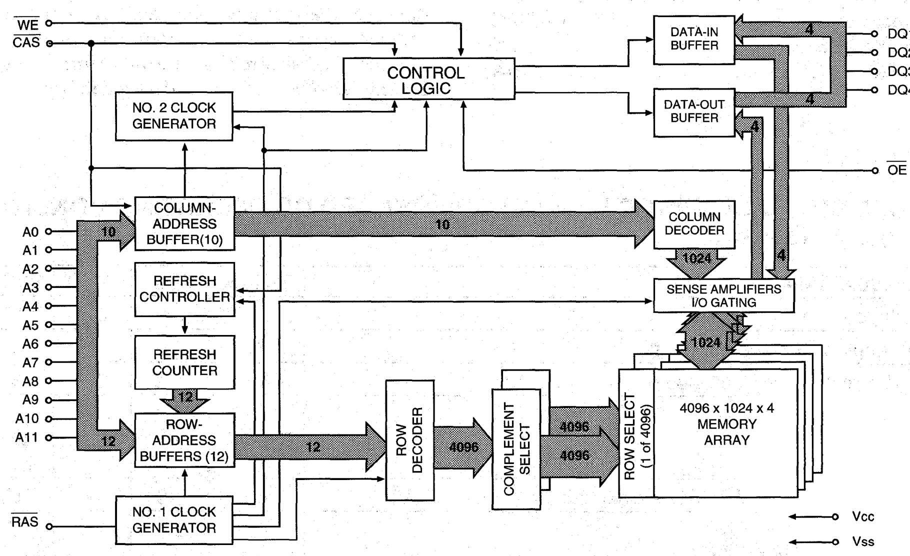
FUNCTIONAL BLOCK DIAGRAM
MT4LC4M4A1 (12 row-addresses)



***NOTE:** 1. If WE goes LOW prior to CAS going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If CAS goes LOW prior to WE going LOW, EW detection circuit output is a LOW (LATE WRITE).

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1.0V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 3.6V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 3.6V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V); 2,048-cycle refresh

PARAMETER/CONDITION	VERSION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC1}	1	1	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	MT4LC4M4B1	I_{CC2}	500	500	µA	
	MT4LC4M4B1 S	I_{CC2}	150	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC3}	120	110	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])		I_{CC4}	90	80	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])		I_{CC5}	120	110	mA	3, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC6}	120	110	mA	3, 5
REFRESH CURRENT: Extended Average power supply current, $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS(MIN); WE = 0.2V; A0-A11 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open); ^tRC = 62.5µs	MT4LC4M4B1 S	I_{CC7}	300	300	µA	3, 5
REFRESH CURRENT: SELF Average power supply current, CBR cycling with $\overline{RAS}$ ≥ ^tRASS(MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC}-0.2V; A0-A11 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	MT4LC4M4B1 S	I_{CC8}	300	300	µA	5

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V); 4,096-cycle refresh

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	1	1	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	500	500	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	100	90	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	80	70	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	100	90	mA	3, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	100	90	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	
READ WRITE cycle time	^tRWC	150		180		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		ns	
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15
Output Enable	^tOE		15		20	ns	23
Access time from column-address	^tAA		30		35	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ precharge time (CBR REFRESH)	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	28
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 28

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command setup time	tWCS	0		0		ns	21
Write command hold time	tWCH	10		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		ns	
Write command pulse width	tWP	10		15		ns	
Write command to RAS lead time	tRWL	15		20		ns	
Write command to CAS lead time	tCWL	15		20		ns	
Data-in setup time	tDS	0		0		ns	22
Data-in hold time	tDH	10		15		ns	22
Data-in hold time (referenced to RAS)	tDHR	45		55		ns	
RAS to WE delay time	tRWD	85		95		ns	21
Column-address to WE delay time	tAWD	55		60		ns	21
CAS to WE delay time	tCWD	40		45		ns	21
Transition time (rise or fall)	tT	3	50	3	50	ns	9, 10
Refresh period (2,048/4,096 cycles)	tREF		32/64		32/64	ms	26
Refresh period - S option (2,048 cycles)	tREF		128		128	ms	27
RAS to CAS precharge time	tRPC	0		0		ns	
CAS setup time (CBR REFRESH)	tCSR	5		5		ns	5
CAS hold time (CBR REFRESH)	tCHR	15		15		ns	5
WE hold time (CBR REFRESH)	tWRH	10		10		ns	25
WE setup time (CBR REFRESH)	tWRP	10		10		ns	25
WE hold time (WCBR test cycle)	tWTH	10		10		ns	25
WE setup time (WCBR test cycle)	tWTS	10		10		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		ns	
Output disable	tOD	3	15	3	20	ns	28
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		15		ns	
RAS pulse width entering SELF REFRESH	tRASS	100		100		µs	27, 29
RAS precharge time exiting SELF REFRESH	tRPS	110		130		ns	27, 29
CAS hold time entering SELF REFRESH	tCHD	15		15		ns	27, 29

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates, 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY WRITE cycles. ^tRWD, ^tAWD and ^tCWD apply to READ-MODIFY-WRITE cycles. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
26. 32ms is a 2,048-cycle refresh, 64ms is a 4,096-cycle refresh.
27. 2,048-row refresh.
28. The 3ns minimum is a parameter guaranteed by design.
29. Refresh must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in the active mode). Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.
30. Column-address changed once each cycle.

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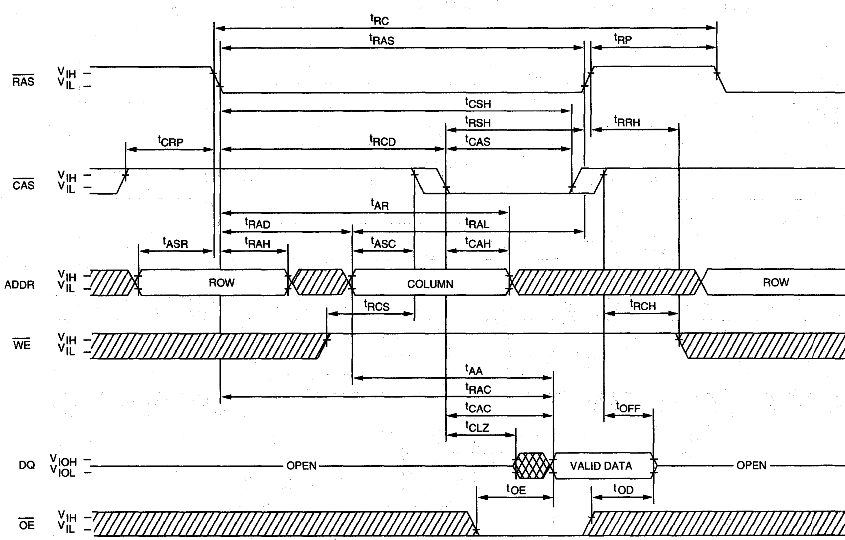
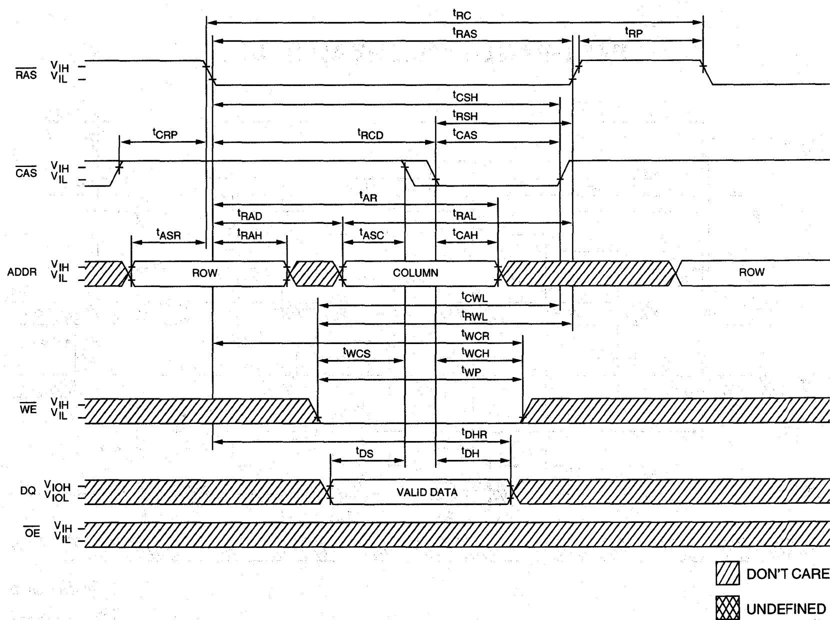
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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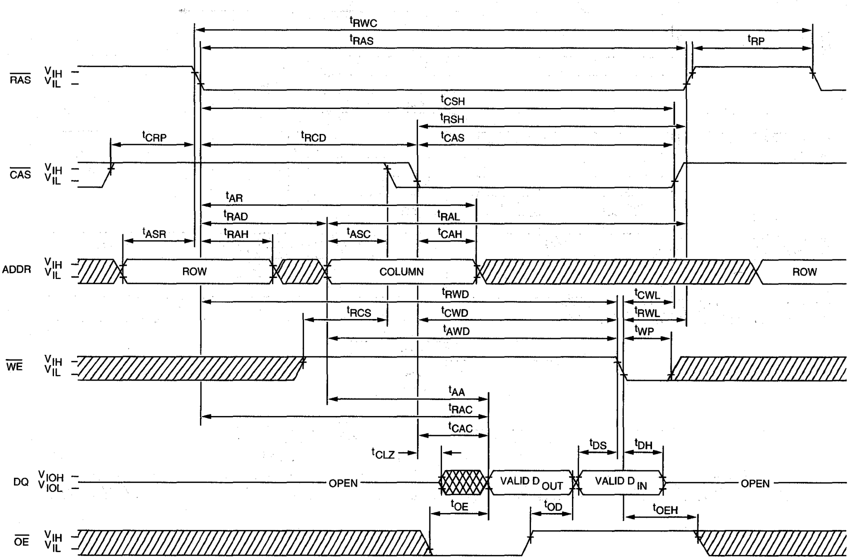
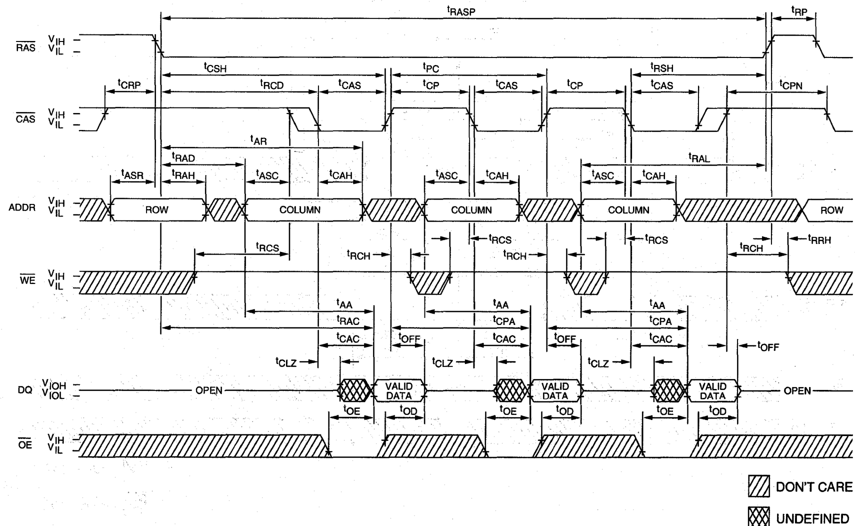
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



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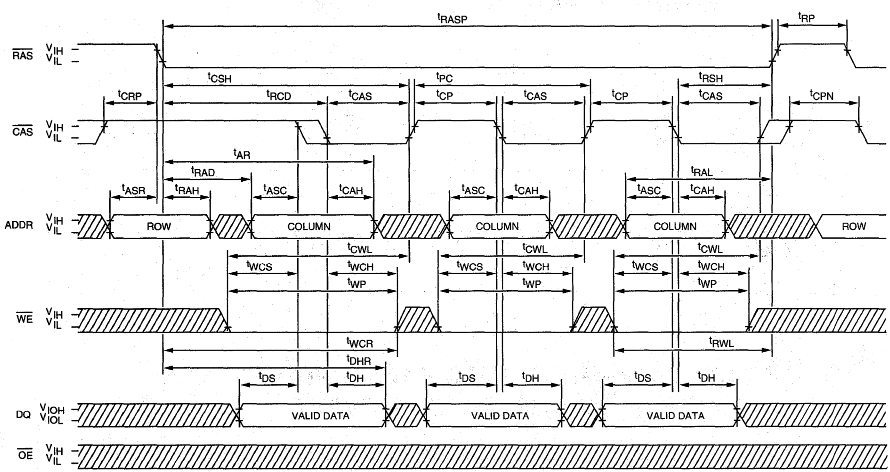
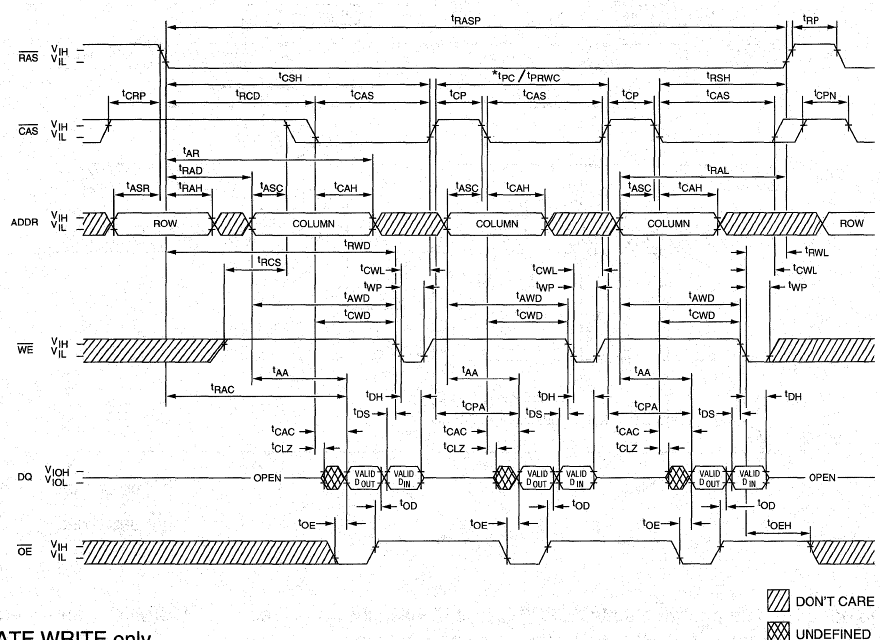
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



*tPC is for LATE WRITE only.

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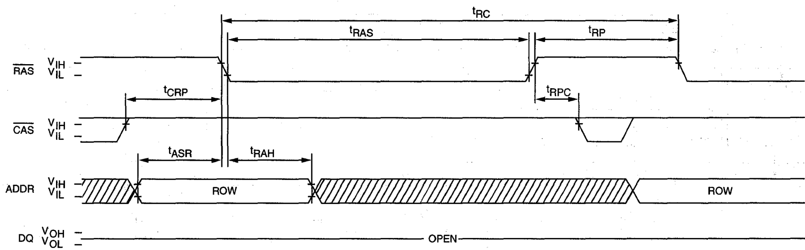
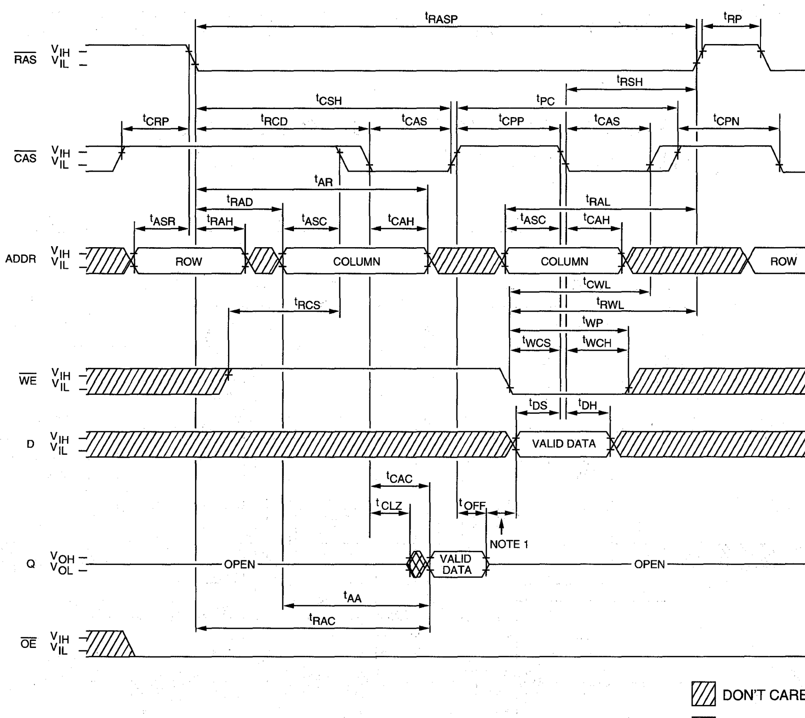
RAS ONLY REFRESH CYCLE

(ADDR = A0-A10, A11; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: ᵗCPP(MIN) or ᵗCP(whichever is greater) + ᵗDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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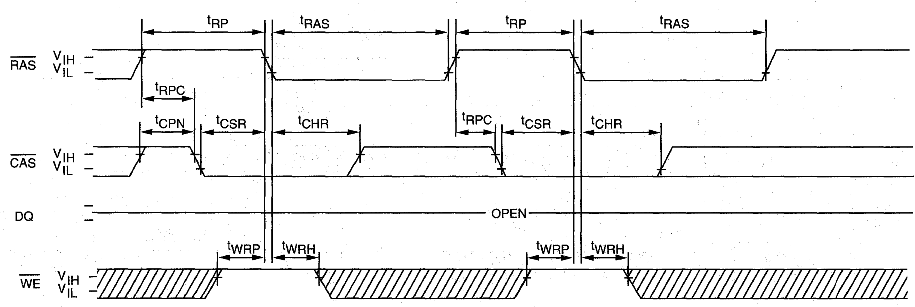
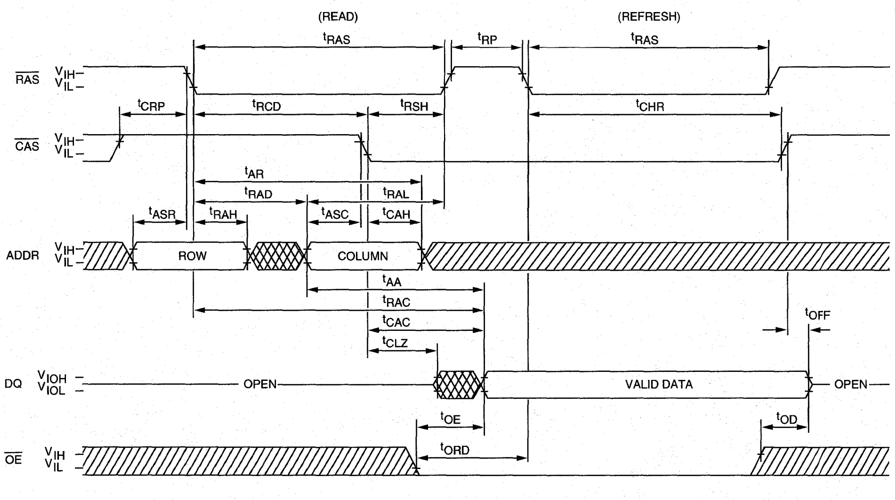
CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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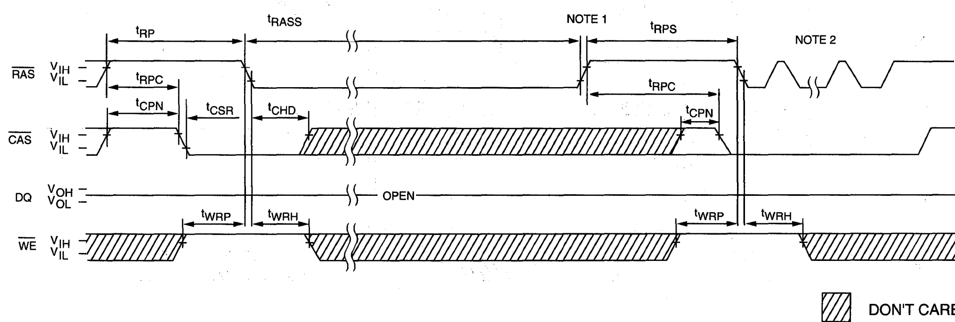
SELF REFRESH CYCLE
(A0-A11 and $\overline{OE}$ = DON'T CARE)



NOTE:
1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a complete burst of all rows should be executed.

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DRAM

4 MEG x 4 DRAM

3.3V EDO PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single power supply: +3.3V ±0.3V
- Low power, 0.4mW standby; 150mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and SELF
- 4,096-cycle (12 row-, 10 column-addresses)
- Optional SELF REFRESH, Extended Refresh rate (2X)
- Extended data-out (EDO) PAGE access cycle

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG
• Refresh	
Standard (4,096 cycles at 64ms)	none
Self (4,096 cycles at 128ms)	S

- Part Number Example: MT4LC4M4E9DJ-6 S

GENERAL DESCRIPTION

The MT4LC4M4E9(S) is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x4 configuration. The MT4LC4M4E9 RAS is used to latch the first 12 bits and CAS the latter 10 bits (A10 and A11 are ignored during CAS falling edge). READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pins remain open (High-Z) until the next CAS cycle, regardless of OE.

If WE goes LOW after CAS goes LOW, data-out (Q) is activated and retains the selected cell data as long as OE remains LOW and RAS or CAS remains LOW (regardless of WE). This late WE pulse results in a READ WRITE cycle. If WE toggles LOW after CAS goes back HIGH, the output pins will open (High-Z) until the next CAS cycle, regardless of OE.

PIN ASSIGNMENT (Top View)

24/26-Pin SOJ (DC-2) and **24/26-Pin TSOP (DD-2)** (same pinout)

Pin	Name	Pin	Name
1	Vcc	26	Vss
2	DQ1	25	DQ4
3	DQ2	24	DQ3
4	WE	23	CAS
5	RAS	22	OE
6	A11	21	A9
8	A10	19	A8
9	A0	18	A7
10	A1	17	A6
11	A2	16	A5
12	A3	15	A4
13	Vcc	14	Vss

The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE and OE.

PAGE ACCESS

PAGE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The PAGE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the PAGE MODE of operation.

EDO

The MT4C4M4E9 provides EDO PAGE MODE which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS returns HIGH. EDO allows CAS precharge time (^tCP) to occur without the output data going invalid. This elimination of CAS output control allows pipeline READs.

FAST PAGE MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. EDO PAGE MODE DRAMs operate similarly to FAST PAGE MODE DRAMs, except data will remain valid or become valid after CAS goes HIGH during READs,

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provided RAS and OE are held LOW. If OE is pulsed while RAS and CAS are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE is toggled or pulsed after CAS goes HIGH while RAS remains LOW, data will transition to and remain High-Z (refer to Figure 1).

If the DQ outputs are wire OR'd, OE must be used to disable idle banks of DRAMs. Alternatively, pulsing WE to the idle banks during CAS high time will also High-Z the outputs. Independent of OE control, the outputs will disable after ^tOFF, which is referenced from the rising edge of RAS or CAS, whichever occurs last.

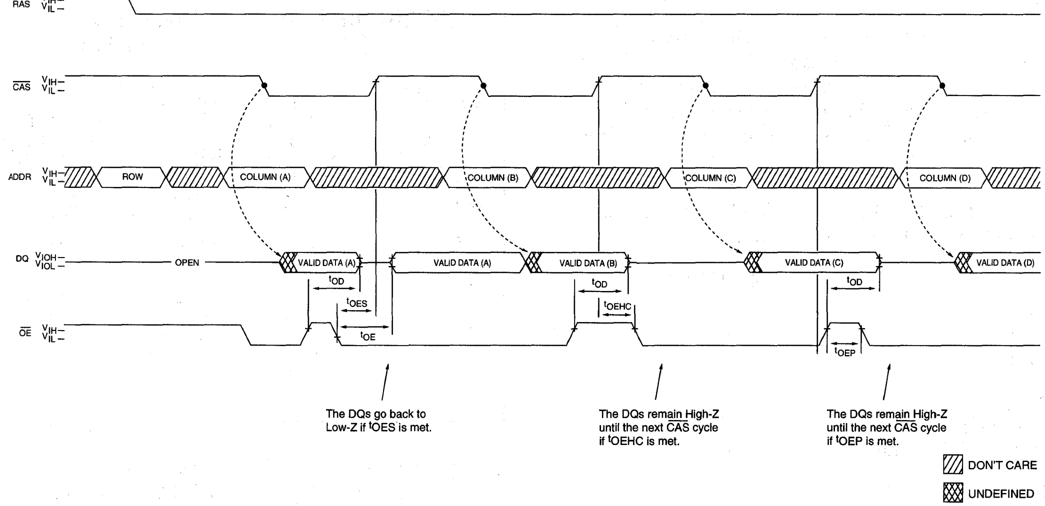

Figure 1
OUTPUT ENABLE AND DISABLE

REFRESH

Preserve correct memory cell data by maintaining power and executing a RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR, or HIDDEN) so that all 4,096 combinations of RAS addresses are executed at least every 64ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

An optional SELF REFRESH mode is also available on the MT4LC4M4E9 S. The "S" option allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms two times longer than the standard 64ms specification.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle, and holding RAS LOW for the specified ^tRASS. Additionally, the "S" option allows for an extended refresh rate of 31.3µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby or BATTERY BACKUP mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ^tRPS ($\approx {}^tRC$). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or BURST REFRESH sequence, all 4,096 rows must be refreshed within 600µs prior to the resumption of normal operation.

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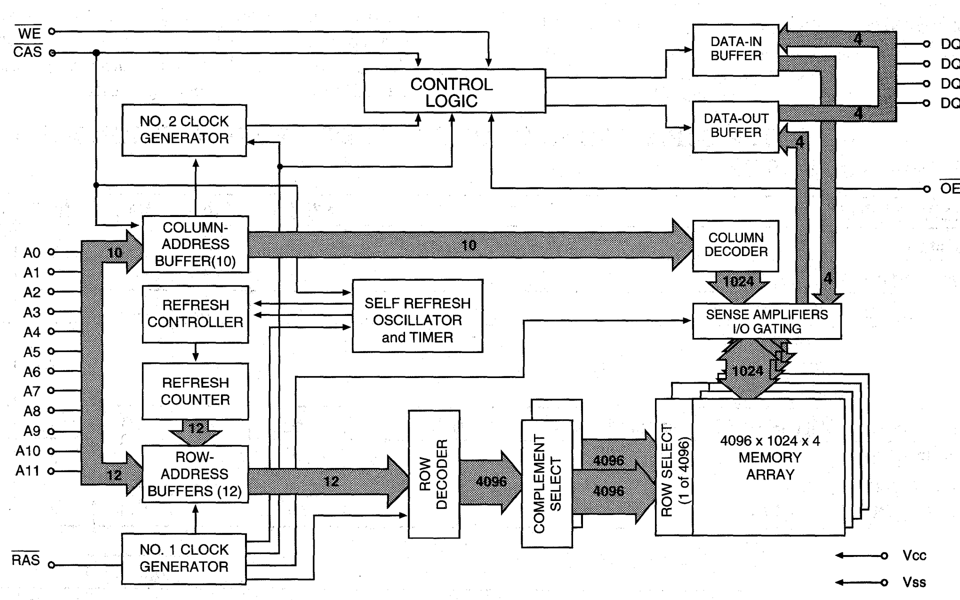
FUNCTIONAL BLOCK DIAGRAM
MT4LC4M4A1 (12 row-addresses)



TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES ᵗR	ADDRESSES ᵗC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
EDO-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss ....-1.0V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 3.6V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 3.6V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)	VOL		0.4	V	

PARAMETER/CONDITION	VERSION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)		ICC1	1	1	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	MT4LC4M4E9	ICC2	500	500	µA	
	MT4LC4M4E9 S	ICC2	150	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])		ICC3	100	90	mA	3, 4, 12
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])		ICC4	80	70	mA	3, 4, 12
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])		ICC5	100	90	mA	3, 12
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])		ICC6	100	90	mA	3, 5
REFRESH CURRENT: Extended (S-only) Average power supply current, CAS = 0.2V or CBR cycling; RAS = tRAS(MIN); WE = 0.2V; A0-A12 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open); tRC = 31.7µs	MT4LC4M4E9 S	ICC7	300	300	µA	3, 5
REFRESH CURRENT: SELF (S-only) Average power supply current, CBR cycling with RAS ≥ tRASS(MIN) and CAS held LOW; WE = Vcc-0.2V; A0-A12 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)	MT4LC4M4E9 S	ICC8	300	300	µA	5

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 13, 23) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	
READ WRITE cycle time	^tRWC	150		180		ns	
EDO PAGE MODE READ or WRITE cycle time	^tPC	25		30		ns	
EDO PAGE MODE READ-WRITE cycle time	^tPRWC	85		95		ns	
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
Access time from $\overline{CAS}$	^tCAC	5	15	5	20	ns	11, 15
Output Enable	^tOE		15		20	ns	23
Access time from column-address	^tAA	15	30	15	35	ns	11
Access time from $\overline{CAS}$ precharge	^tCPA	20	35	20	40	ns	11
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{CAS}$ pulse width	^tCAS	10	100,000	10	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	40		70		ns	
$\overline{CAS}$ precharge time (CBR REFRESH)	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (EDO PAGE MODE)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	26
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 26

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 13, 23) (Vcc = 3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command setup time	^tWCS	0		0		ns	21
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to RAS)	^tWCR	45		55		ns	
Write command pulse width	^tWP	10		10		ns	
Write command to RAS lead time	^tRWL	15		20		ns	
Write command to CAS lead time	^tCWL	15		20		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	10		15		ns	22
Data-in hold time (referenced to RAS)	^tDHR	45		55		ns	
RAS to WE delay time	^tRWD	85		95		ns	21
Column-address to WE delay time	^tAWD	55		60		ns	21
CAS to WE delay time	^tCWD	40		45		ns	21
Transition time (rise or fall)	^tT	2	50	2	50	ns	9, 10
Refresh period (4,096 cycles)	^tREF		64		64	ms	
Refresh period - S option (4,096 cycles)	^tREF		128		128	ms	
RAS to CAS precharge time	^tRPC	0		0		ns	
CAS setup time (CBR REFRESH)	^tCSR	5		5		ns	5
CAS hold time (CBR REFRESH)	^tCHR	15		15		ns	5
WE hold time (CBR REFRESH)	^tWRH	10		10		ns	25
WE setup time (CBR REFRESH)	^tWRP	10		10		ns	25
WE hold time (WCBR test cycle)	^tWTH	10		10		ns	25
WE setup time (WCBR test cycle)	^tWTS	10		10		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		ns	
Output disable	^tOD	3	15	3	20	ns	26
OE hold time from WE during READ-MODIFY-WRITE cycle	^tOEH	15		15		ns	
RAS pulse width entering SELF REFRESH	^tRASS	100		100		µs	27
RAS precharge time exiting SELF REFRESH	^tRPS	110		130		ns	27
CAS hold time entering SELF REFRESH	^tCHD	15		15		ns	27
OE HIGH hold time from CAS HIGH	^tOEHC	10		10		ns	
OE HIGH pulse width	^tOEP	10		10		ns	
Data output hold after CAS LOW	^tCOH	5		5		ns	
Output disable delay from WE (CAS HIGH)	^tWHZ	3	10	3	10	ns	
WE pulse width for output disable when CAS HIGH	^tWPZ	5		5		ns	

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +3.3V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{\text{RAS}}$ REFRESH cycles ($\overline{\text{RAS}}$ ONLY or CBR with $\overline{\text{WE}}$ HIGH) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 2.5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. ^{t}CAC (MIN), ^{t}CPA (MIN) and ^{t}AA (MIN) are for reference only to help aid the user as to when to expect the earliest data to be accessed. Only ^{t}CAC (MAX), ^{t}CPA (MAX) and ^{t}AA (MAX) are guaranteed and should be designed to.
12. Column address changed once each cycle.
13. Measured with a load equivalent to two TTL gates, 100pF and VOL = 0.8V and VOH = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC, provided ^{t}RAD is not exceeded.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA, provided ^{t}RCD is not exceeded.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL. It is referenced from the rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}WCS < ^{t}WCS (MIN) and ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE WRITE ($\overline{\text{OE}}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{\text{OE}}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible. Additionally, $\overline{\text{WE}}$ must be pulsed during $\overline{\text{CAS}}$ HIGH time inorder to palce I/O buffers in High-Z.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{\text{WE}}$ = LOW and $\overline{\text{OE}}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{\text{WE}}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. The 3ns minimum is a parameter guaranteed by design.
27. Refresh must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in the active mode). Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.

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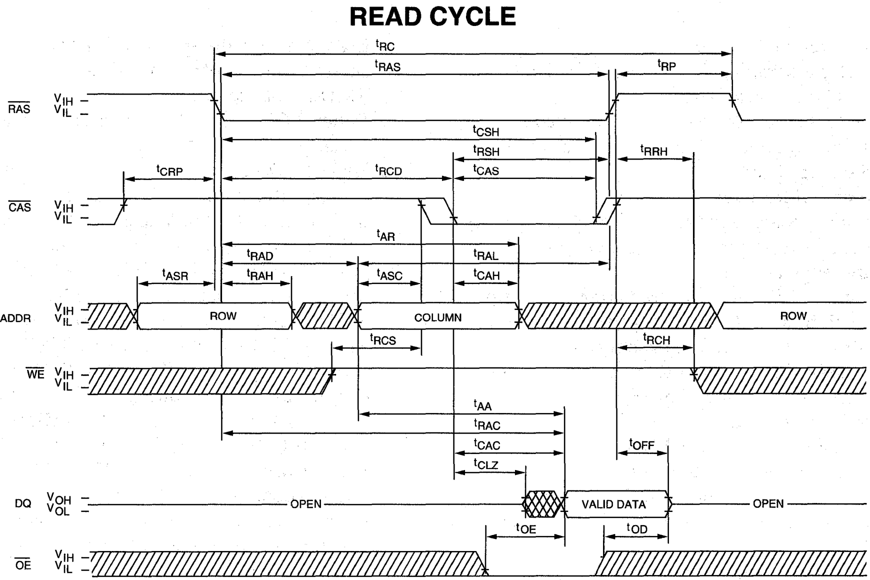
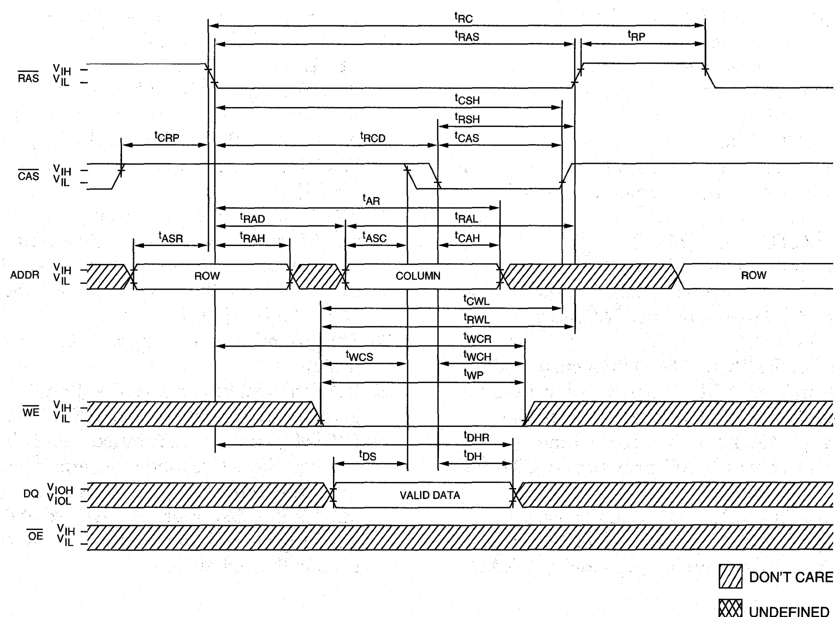
READ CYCLE



EARLY WRITE CYCLE



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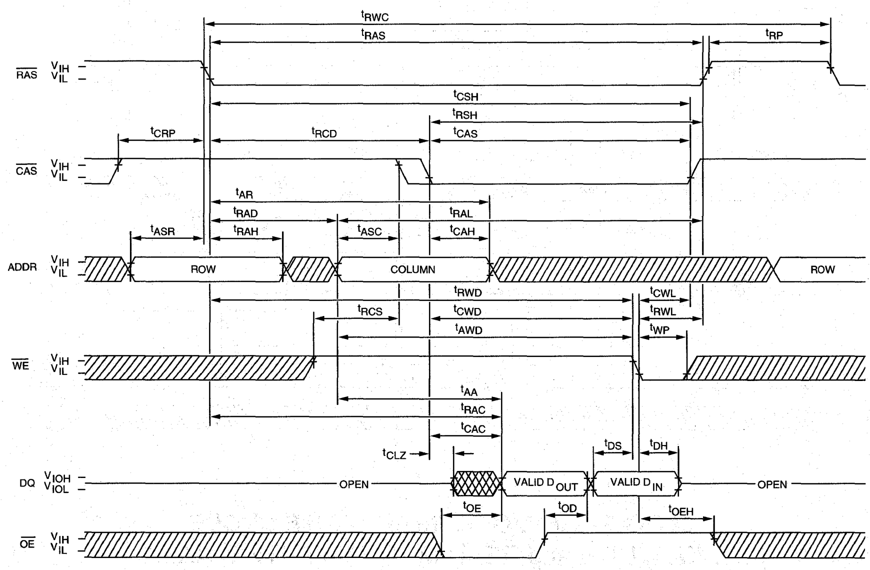
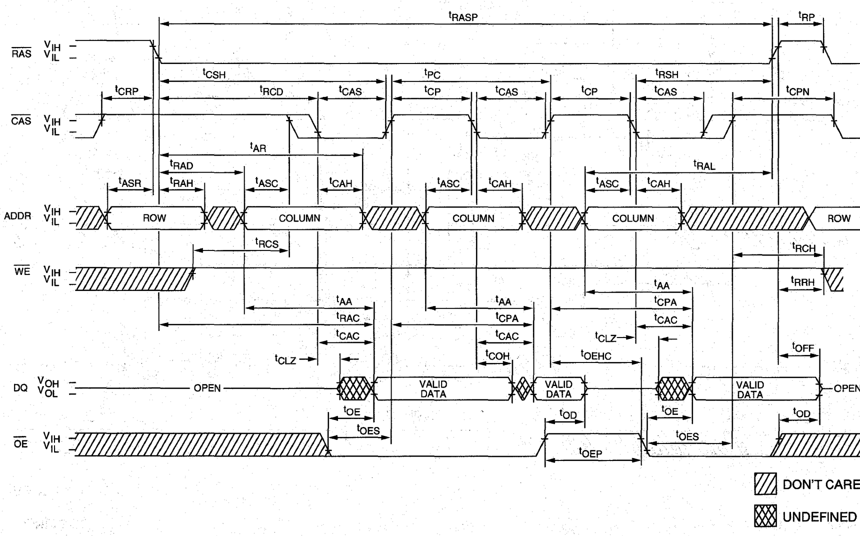
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



EDO-PAGE-MODE READ CYCLE



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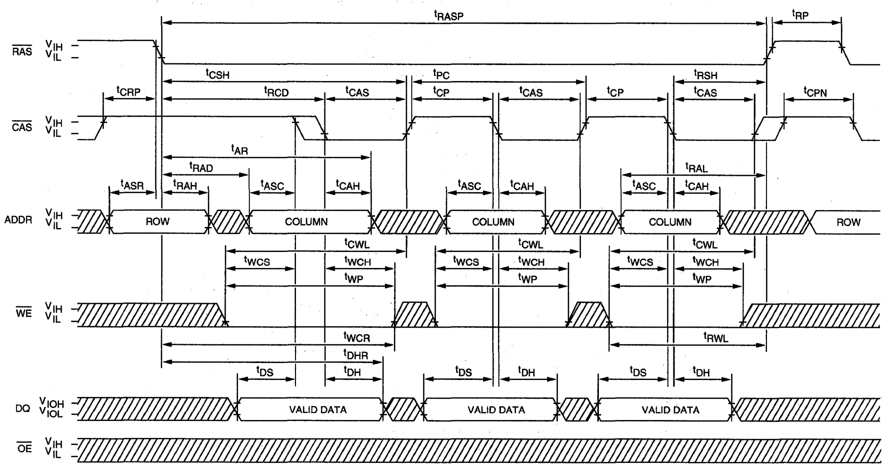
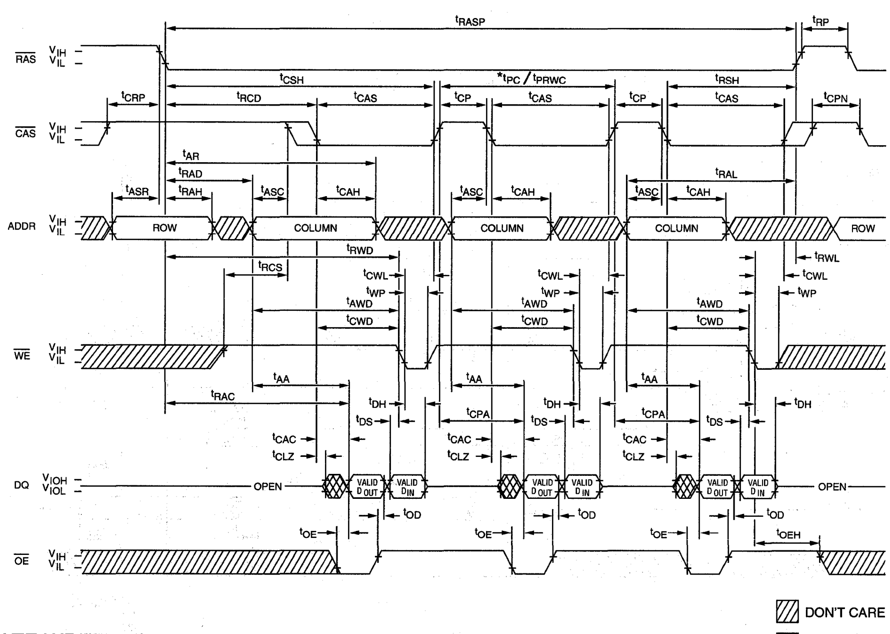
EDO-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



*tPC is for LATE WRITE only.

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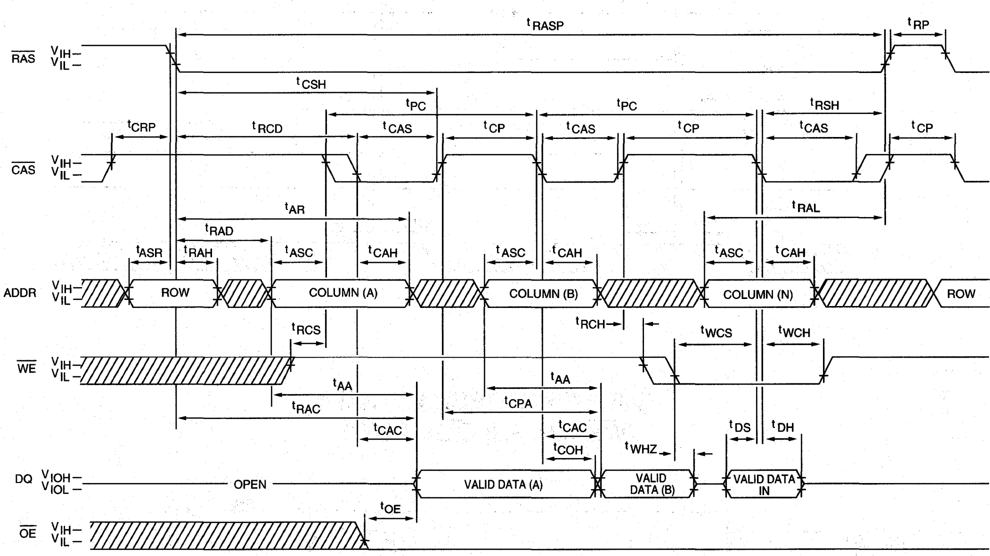
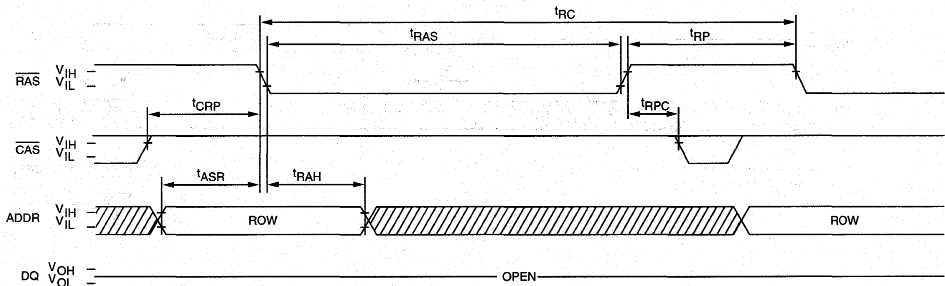
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



RAS ONLY REFRESH CYCLE
(ADDR = A0-A12; WE = DON'T CARE)



DON'T CARE

UNDEFINED

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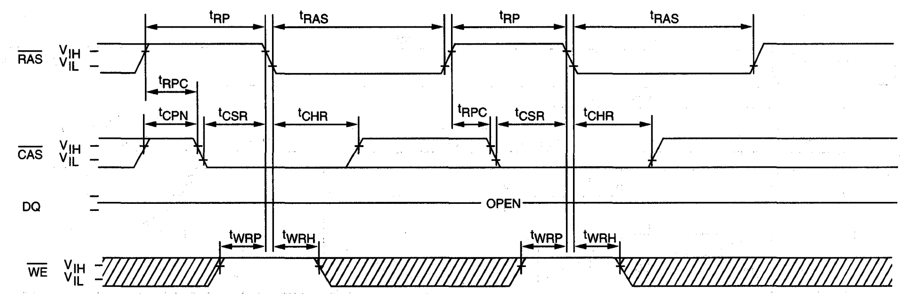
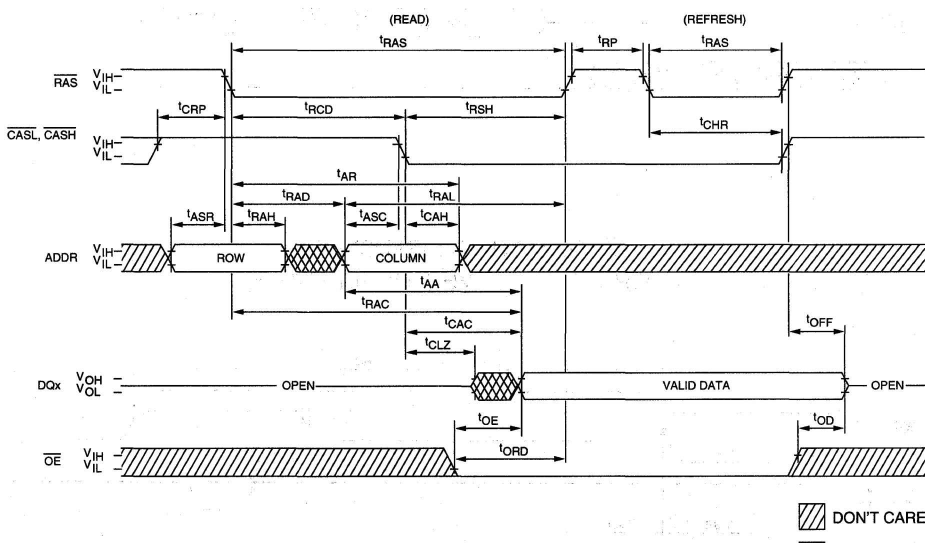
CBR REFRESH CYCLE
(A0-A12 and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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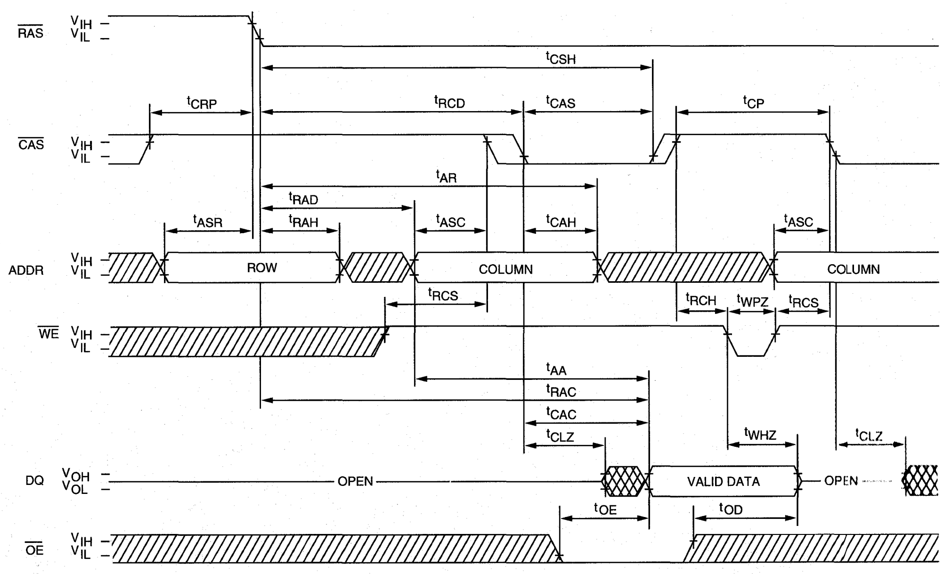
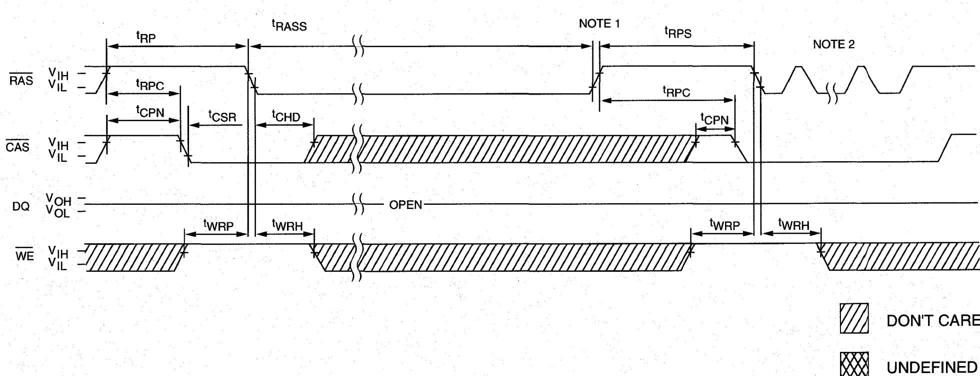
READ CYCLE with $\overline{WE}$-CONTROLLED DISABLE



SELF REFRESH CYCLE
(A0-A12 and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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DRAM

512K x 8 DRAM

FAST PAGE MODE

FEATURES

- Industry-standard x8 pinouts, timing, functions and packages
- Address entry: ten row-addresses, nine column-addresses
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply*
- Low power, 3mW standby; 250mW active, typical
- All device pins are TTL-compatible
- 1,024-cycle refresh in 16ms
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- FAST PAGE MODE access cycle

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6*
70ns access	-7
80ns access	-8
• Packages	
Plastic SOJ (400 mil)	DJ

- Part Number Example: MT4C8512DJ-7

*60ns specifications are limited to a Vcc range of ±5%.

PIN ASSIGNMENT (Top View)

28-Pin SOJ
(DC-4)

Pin name	Pin	Pin	Pin name
Vcc	1	28	Vss
DQ1	2	27	DQ8
DQ2	3	26	DQ7
DQ3	4	25	DQ6
DQ4	5	24	DQ5
NC	6	23	$\overline{\text{CAS}}$
$\overline{\text{WE}}$	7	22	$\overline{\text{OE}}$
$\overline{\text{RAS}}$	8	21	NC
A9	9	20	A8
A0	10	19	A7
A1	11	18	A6
A2	12	17	A5
A3	13	16	A4
Vcc	14	15	Vss

GENERAL DESCRIPTION

The MT4C8512 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x8 configuration. Each byte is uniquely addressed through the 19 address bits during READ or WRITE cycles. The address is entered first by $\overline{\text{RAS}}$ latching 10 bits (A0-A9) and then $\overline{\text{CAS}}$ latching 9 bits (A0-A8).

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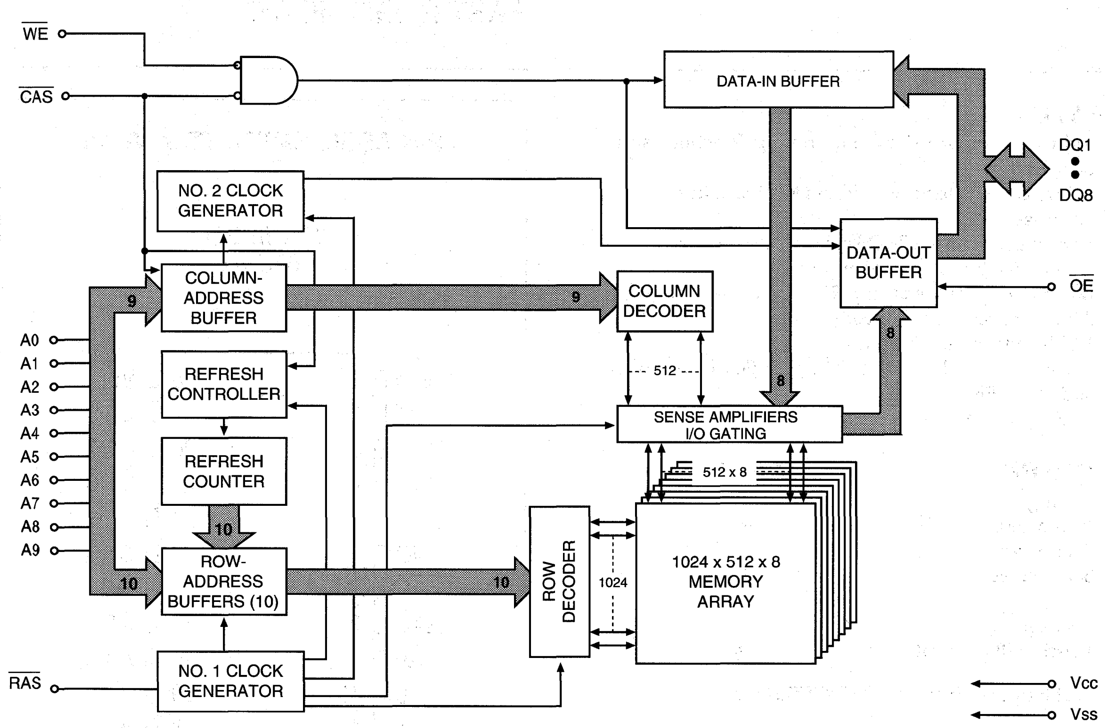
FUNCTIONAL BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 19 address bits during READ or WRITE cycles. First, $\overline{RAS}$ is used to latch 10 bits (A0-A9) then, $\overline{CAS}$ latches 9 bits (A0-A8).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$ ONLY) or an active cycle (READ, WRITE or READ WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

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DRAM

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ${}^{t}R$	ADDRESSES ${}^{t}C$	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY WRITE		L	L	L	X	ROW	COL	Data-In	
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	1
$\overline{RAS}$ ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	X	X	X	X	High-Z	

NOTE: 1. EARLY WRITE only.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%**)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6**	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	2	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	ICC3	120	110	100	mA	3, 4, 29
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: ${}^tPC$ = ${}^tPC$ [MIN]; ${}^tCP$, ${}^tASC$ = 10ns)	ICC4	100	90	80	mA	3, 4, 29
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = VIH: ${}^tRC$ = ${}^tRC$ [MIN])	ICC5	120	110	100	mA	3, 29
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	ICC6	110	100	90	mA	3, 5

**60ns specifications are limited to a Vcc range of ±5%.

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%*)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
READ WRITE cycle time	^{t}RWC	150		175		195		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	85		95		100		ns	
Access time from RAS	^{t}RAC		60		70		80	ns	14
Access time from CAS	^{t}CAC		15		20		20	ns	15
Output Enable time	^{t}OE		15		20		20	ns	
Access time from column-address	^{t}AA		30		35		40	ns	
Access time from CAS precharge	^{t}CPA		35		40		45	ns	
RAS pulse width	^{t}RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^{t}RSH	15		20		20		ns	
RAS precharge time	^{t}RP	40		50		60		ns	
CAS pulse width	^{t}CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^{t}CSH	60		70		80		ns	
CAS precharge time	^{t}CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^{t}CP	10		10		10		ns	
RAS to CAS delay time	^{t}RCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	^{t}CRP	10		10		10		ns	
Row-address setup time	^{t}ASR	0		0		0		ns	
Row-address hold time	^{t}RAH	10		10		10		ns	
RAS to column-address delay time	^{t}RAD	15	30	15	35	15	40	ns	18
Column-address setup time	^{t}ASC	0		0		0		ns	
Column-address hold time	^{t}CAH	10		15		15		ns	
Column-address hold time (referenced to RAS)	^{t}AR	50		55		60		ns	
Column-address to RAS lead time	^{t}RAL	30		35		40		ns	
Read command setup time	^{t}RCS	0		0		0		ns	26
Read command hold time (referenced to CAS)	^{t}RCH	0		0		0		ns	19, 26
Read command hold time (referenced to RAS)	^{t}RRH	0		0		0		ns	19
CAS to output in Low-Z	^{t}CLZ	3		3		3		ns	30

*60ns specifications are limited to a V_{CC} range of ±5%.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = +5V ±10%*)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^tOFF	3	15	3	15	3	15	ns	20, 28, 30
Output disable time	^tOD	3	15	3	15	3	15	ns	28, 30
Write command setup time	^tWCS	0		0		0		ns	21, 26
Write command hold time	^tWCH	10		10		10		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	26
Write command pulse width	^tWP	10		10		10		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	27
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	

*60ns specifications are limited to a Vcc range of ±5%.

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{\text{CAS}}$ = V_{IH}, data output is high impedance.
12. If $\overline{\text{CAS}}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OH} = 2.0V and V_{OL} = 0.8V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit conzdition; it is not a reference to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE WRITE ($\overline{\text{OE}}$-controlled) cycle.
22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{\text{OE}}$ is LOW then taken HIGH before $\overline{\text{CAS}}$ goes HIGH, Q goes open. If $\overline{\text{OE}}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{\text{WE}}$ = LOW and $\overline{\text{OE}}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{\text{WE}}$ going LOW.
27. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{\text{OE}}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{\text{CAS}}$ remains LOW and $\overline{\text{OE}}$ is taken back LOW after ^{t}OEH is met. If $\overline{\text{CAS}}$ goes HIGH prior to $\overline{\text{OE}}$ going back LOW, the DQs will remain open.
28. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{\text{CAS}}$ goes HIGH before $\overline{\text{OE}}$, the DQs will open regardless of the state of $\overline{\text{OE}}$. If $\overline{\text{CAS}}$ stays LOW while $\overline{\text{OE}}$ is brought HIGH, the DQs will open. If $\overline{\text{OE}}$ is brought back LOW ($\overline{\text{CAS}}$ still LOW), the DQs will provide the previously read data.
29. Column-address changed once each cycle.
30. The 3ns minimum is a parameter guaranteed by design.

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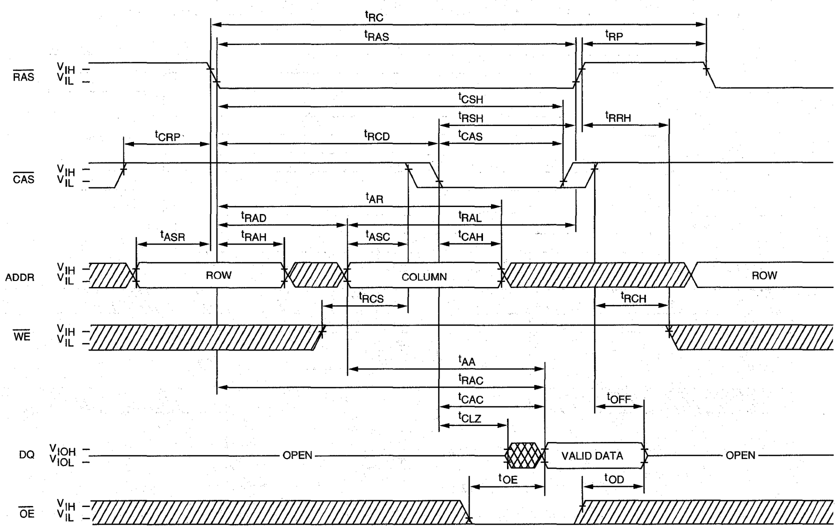
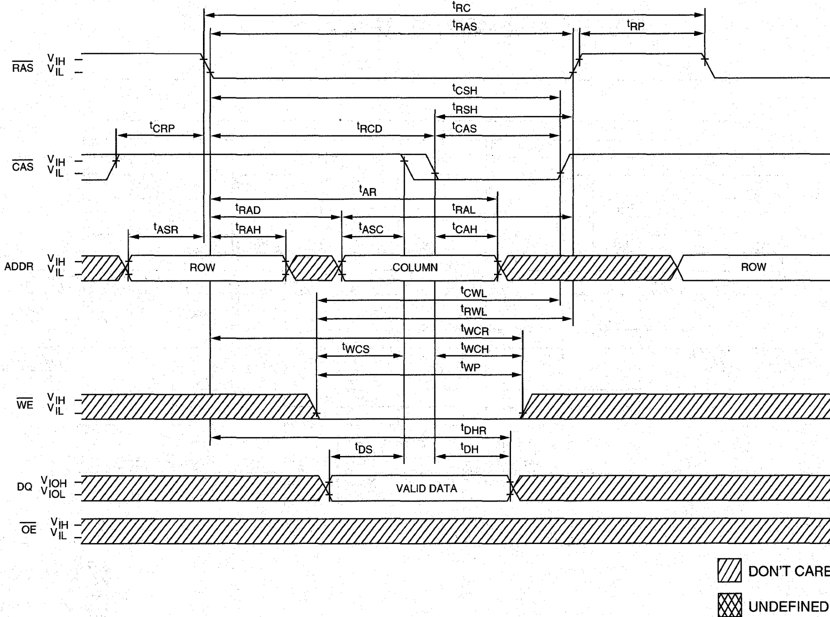
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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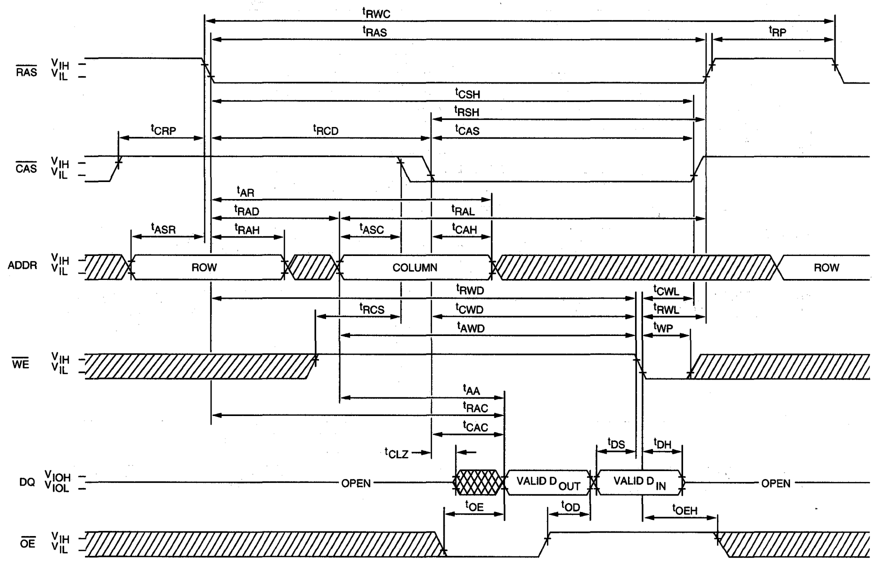
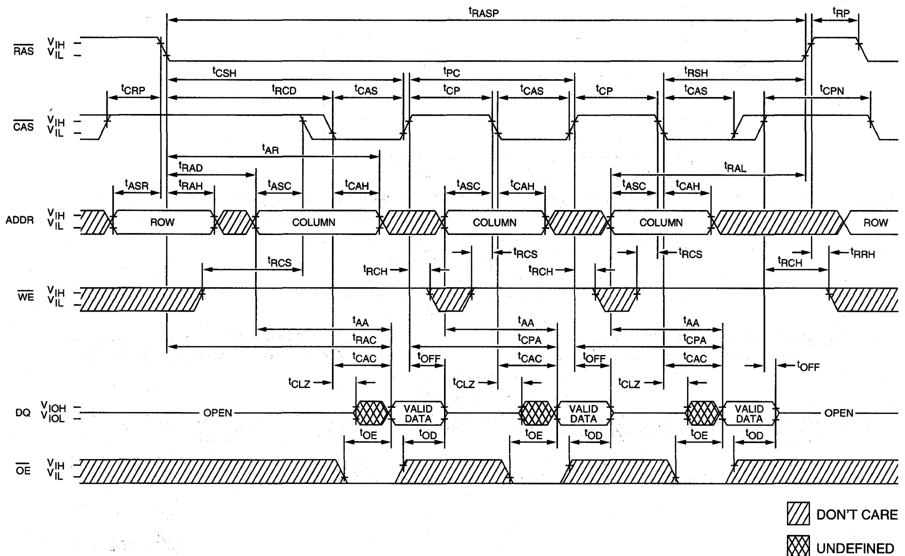
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



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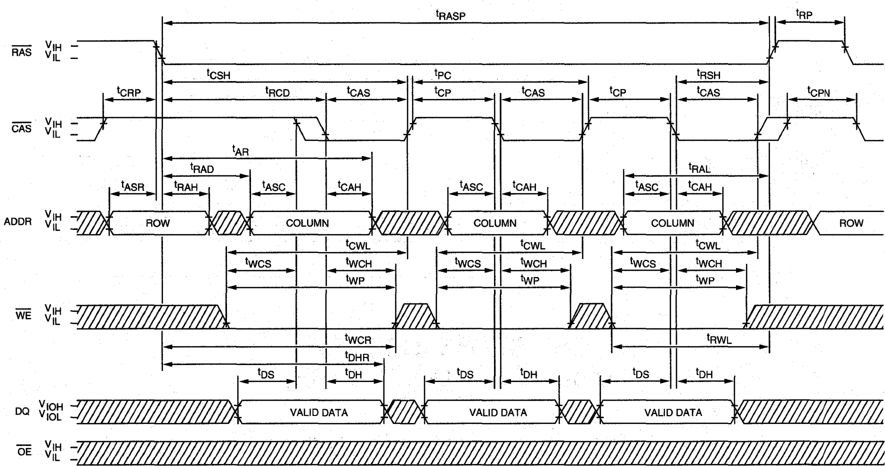
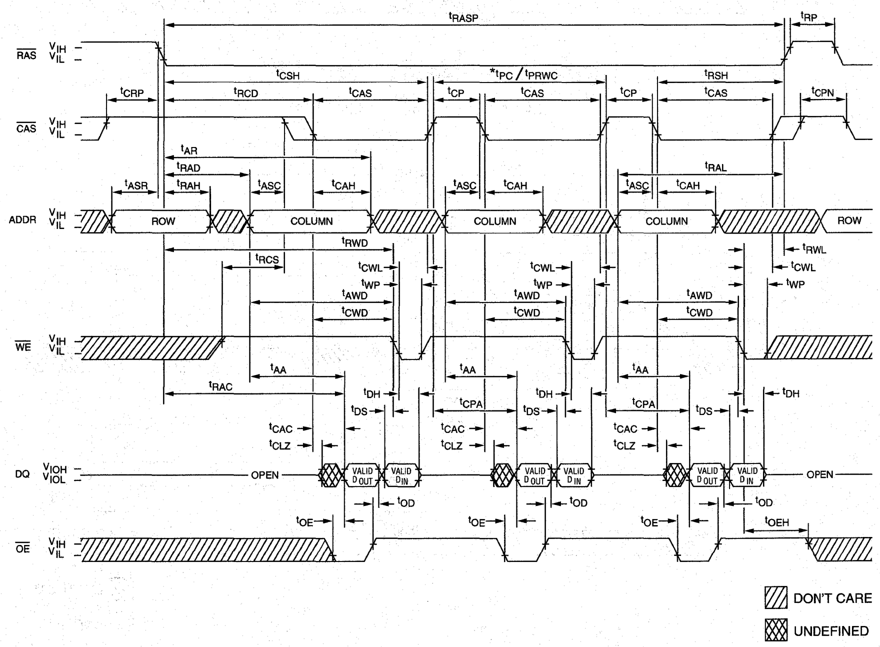
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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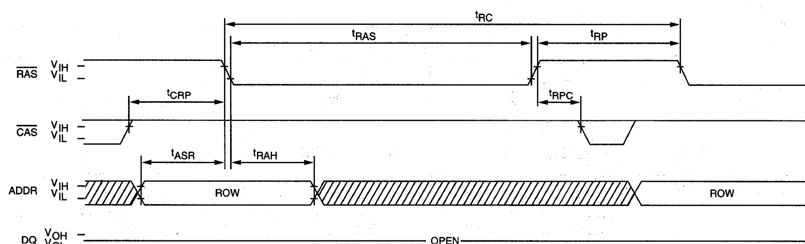
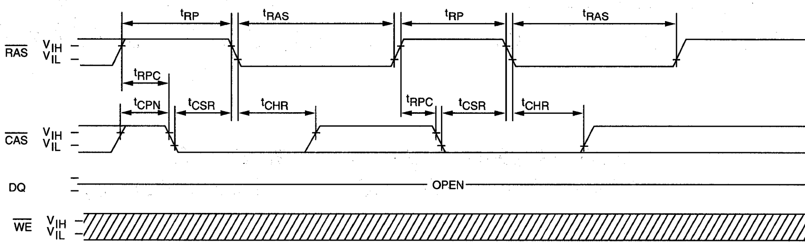
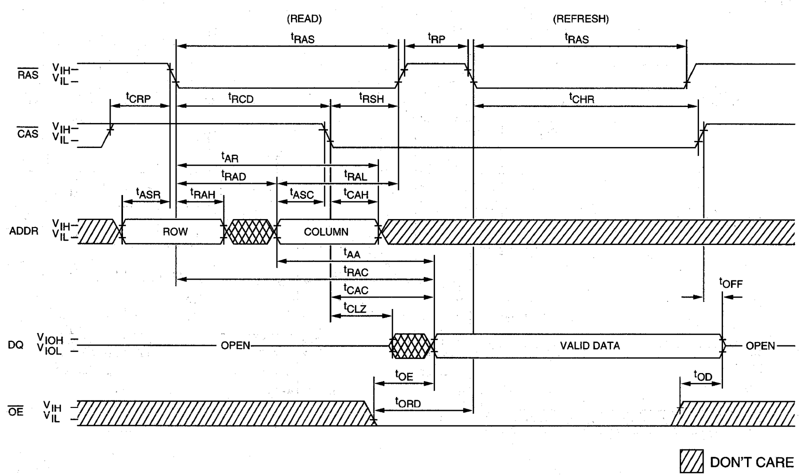
RAS ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



CBR REFRESH CYCLE
(A0-A9; OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
(WE = HIGH; OE = LOW)



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DRAM

2 MEG x 8 DRAM

3.3V FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard x8 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single power supply: +3.3V ±0.3V
- Low power, 1.2mW standby; 200mW active, typical
- All device pins are TTL-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and SELF
- 2,048-cycle refresh (11 row-, 10 column-addresses)
- Optional SELF REFRESH mode, with Extended Refresh rate (4X)

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Plastic 28-pin SOJ (300 mil)	DJ
Plastic 28-pin TSOP (300 mil)	TG
• Refresh	
Standard, at 32ms	none
SELF REFRESH, at 128ms	S

- Part Number Example: MT4LC2M8B1DJ-7 S

PIN ASSIGNMENT (Top View)

28-Pin SOJ (DC-8) and 28-Pin TSOP (DD-3)

Pin	Name	Pin	Name
1	Vcc	28	Vss
2	DQ1	27	DQ8
3	DQ2	26	DQ7
4	DQ3	25	DQ6
5	DQ4	24	DQ5
6	$\overline{WE}$	23	$\overline{CAS}$
7	$\overline{RAS}$	22	$\overline{OE}$
8	NC	21	A9
9	A10	20	A8
10	A0	19	A7
11	A1	18	A6
12	A2	17	A5
13	A3	16	A4
14	Vcc	15	Vss

GENERAL DESCRIPTION

The MT4LC2M8B1(S) is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x8 configuration. The MT4LC2M8B1 S is designed to operate in a 3.3V ±10% memory system. Each byte is uniquely addressed through the 21 address bits during READ or WRITE cycles. The address is entered first by $\overline{RAS}$ latching 11 bits (A0-A10) and then $\overline{CAS}$ latching 10 bits (A0-A9).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$ ONLY) or an active cycle (READ, WRITE or READ WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A11) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 2,048 combinations of $\overline{RAS}$ addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

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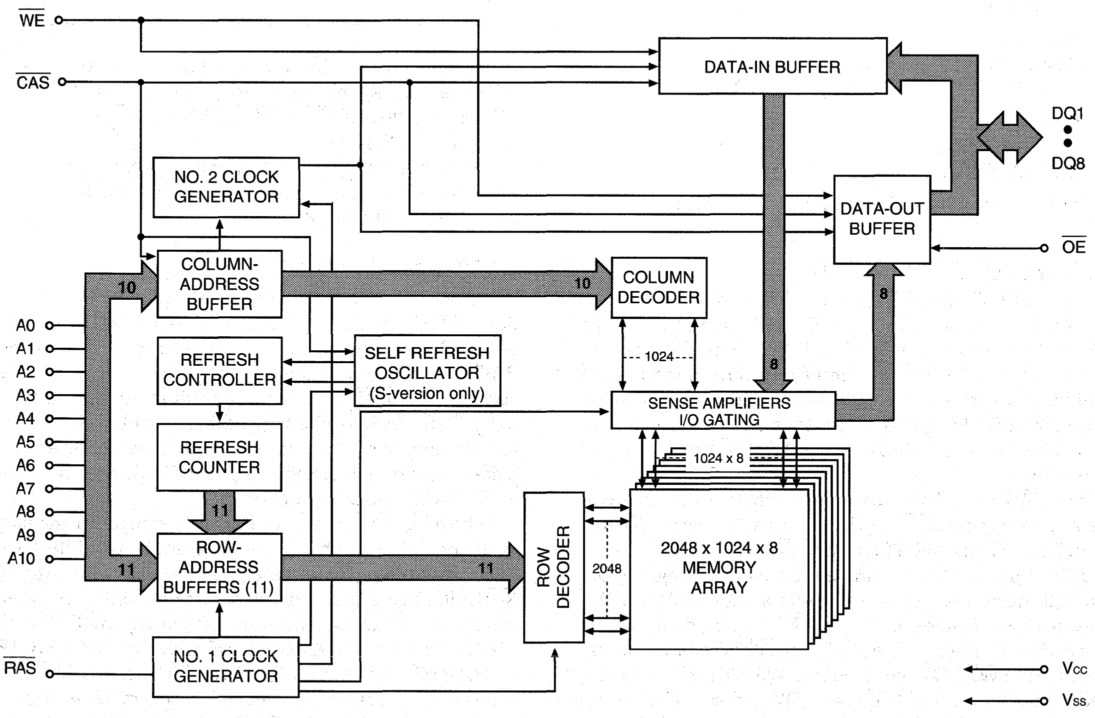
SELF REFRESH

SELF REFRESH is similar to CBR except that the DRAM provides its own internal clocking during SLEEP mode. Thus, an external clock is not required which provides additional power savings and design ease. The DRAM's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding both $\overline{RAS}$ and $\overline{CAS}$ LOW for a specified period. The industry standard for this value is 100µs minimum (^tRASS). The DRAM will remain in the SELF REFRESH mode while $\overline{RAS}$ and $\overline{CAS}$ remain LOW. Once $\overline{CAS}$ has been held LOW for ^tCHD, $\overline{CAS}$ is no longer required to remain LOW and becomes a "don't care." $\overline{CAS}$ is a "don't care" until ^tCHS, at which time $\overline{CAS}$ must be either HIGH or LOW.

The SELF REFRESH mode is terminated by taking $\overline{RAS}$ HIGH for the time minimum of an operation cycle, typically 200ns (^tRPS). Once the SELF REFRESH mode has been terminated, it is recommended that the user perform a refresh of all rows within the time of the external refresh rate prior to active use of the DRAM. The external refresh rate is typically 62.5µs per row-address. Once this burst has been completed, the DRAM may be used in the functional mode with distributed refreshes, such as CBR or $\overline{RAS}$ ONLY.

The alternative approach when exiting SELF REFRESH mode is to utilize distributed refreshes once ^tRPS has been met, provided CBR REFRESH cycles are employed. The first CBR pulse should occur within the time of the external refresh rate prior to active use of the DRAM to ensure maximum data integrity and must be executed within three external refresh rate periods.

FUNCTIONAL BLOCK DIAGRAM
2,048 ROWS



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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DQs
						^tR	^tC	
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ....-1V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS

(Notes: 1, 6, 7, 31) (Vcc = +3.0V to 3.6V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 3.6V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)	VOL		0.4	V	

ELECTRICAL CHARACTERISTICS AND DC OPERATING SPECIFICATIONS

(Notes: 1, 6, 7, 31) (Vcc = +3.0V to 3.6V)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: TTL (RAS = CAS = VIH)	ICC1	1	1	1	mA	
STANDBY CURRENT: CMOS (RAS = CAS = Vcc -0.2V)	ICC2	500	500	500	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	140	130	120	mA	3, 4, 27
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN]; tCP, tASC = 10ns)	ICC4	100	90	80	mA	3, 4, 27
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])	ICC5	140	130	120	mA	3, 27
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC6	140	130	120	mA	3, 5
REFRESH CURRENT: Extended (S-only) Average power supply current during BBU REFRESH: CAS = 0.2V or CBR cycling; RAS = tRAS (MIN) to 300ns; WE, A0-A10 and DIN = Vcc - 0.2V (DIN may be left open), tRC = 62.5µs (2,048 rows at 62.5µs = 128ms)	ICC7	300	300	300	µA	3, 5
REFRESH CURRENT: SELF (S-only) Average power supply current during SELF REFRESH: CBR cycle with RAS ≥ tRASS (MIN) and CAS held LOW; WE = Vcc - 0.2V; A0-A10 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)	ICC8	300	300	300	µA	5

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Addresses	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	
READ WRITE cycle time	^tRWC	150		180		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		ns	
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15
Output Enable	^tOE		15		20	ns	23
Access time from column-address	^tAA		30		35	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ precharge time (CBR REFRESH)	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	28
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 28

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command setup time	tWCS	0		0		ns	21
Write command hold time	tWCH	10		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		ns	
Write command pulse width	tWP	10		15		ns	
Write command to RAS lead time	tRWL	15		20		ns	
Write command to CAS lead time	tCWL	15		20		ns	
Data-in setup time	tDS	0		0		ns	22
Data-in hold time	tDH	10		15		ns	22
Data-in hold time (referenced to RAS)	tDHR	45		55		ns	
RAS to WE delay time	tRWD	85		95		ns	21
Column-address to WE delay time	tAWD	55		60		ns	21
CAS to WE delay time	tCWD	40		45		ns	21
Transition time (rise or fall)	tT	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	tREF		32		32	ms	
Refresh period - S option (2,048 cycles)	tREF		128		128	ms	26
RAS to CAS precharge time	tRPC	0		0		ns	
CAS setup time (CBR REFRESH)	tCSR	5		5		ns	5
CAS hold time (CBR REFRESH)	tCHR	15		15		ns	5
WE hold time (CBR REFRESH)	tWRH	10		10		ns	25
WE setup time (CBR REFRESH)	tWRP	10		10		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		ns	
Output disable	tOD	3	15	3	20	ns	28
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		15		ns	
RAS pulse width entering SELF REFRESH	tRASS	100		100		µs	26
RAS precharge time exiting SELF REFRESH	tRPS	110		130		ns	26
CAS hold time entering SELF REFRESH	tCHD	15		15		ns	26

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate, 50pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
26. Refresh must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in the active mode). Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.
27. Column-address changed once each cycle.
28. The 3ns minimum is guaranteed by design.

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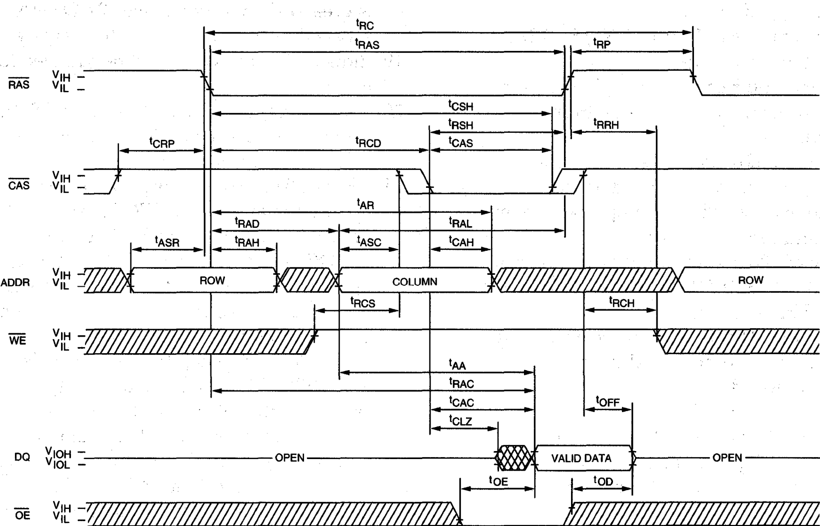
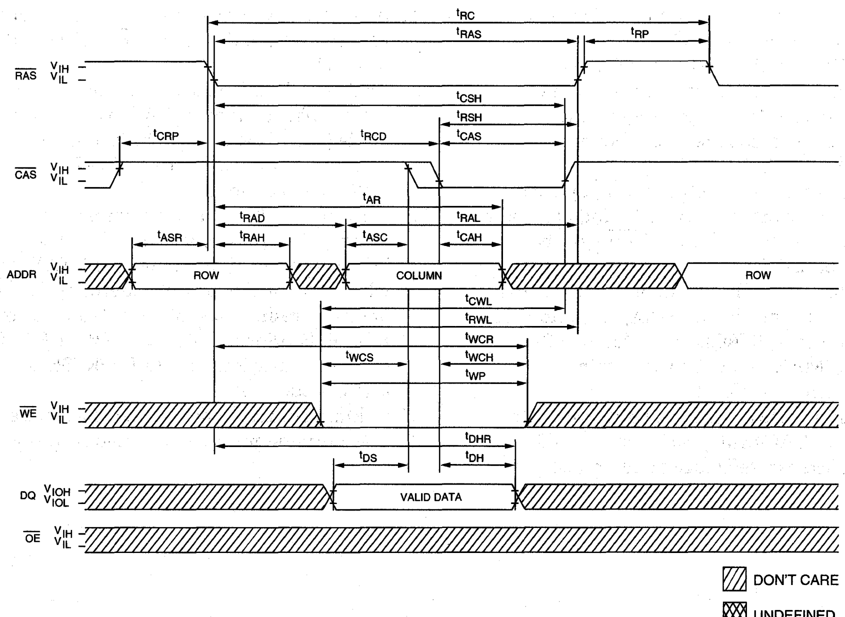
READ CYCLE



EARLY WRITE CYCLE



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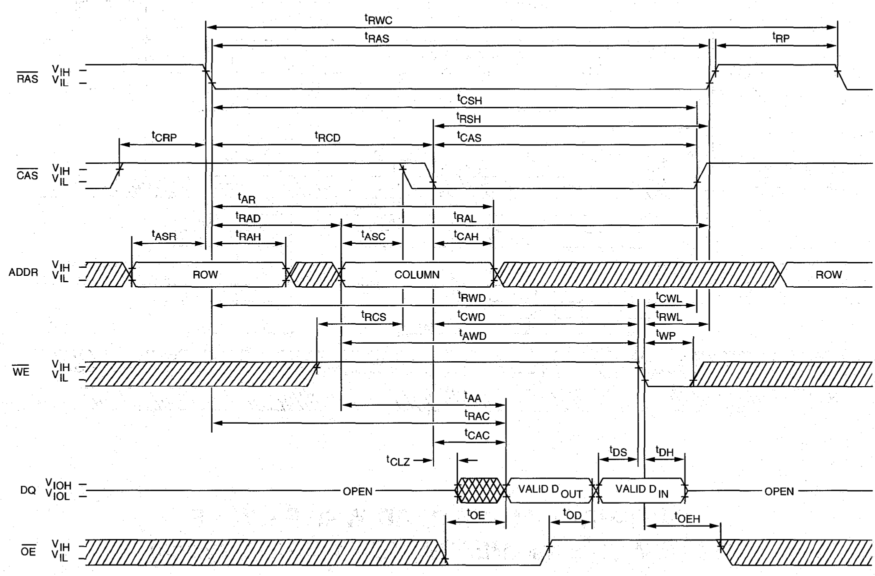
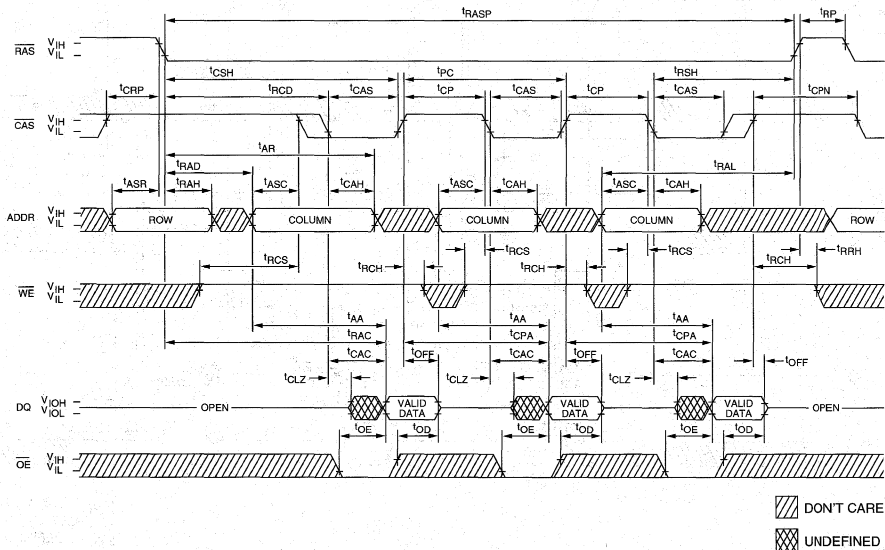
READ WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



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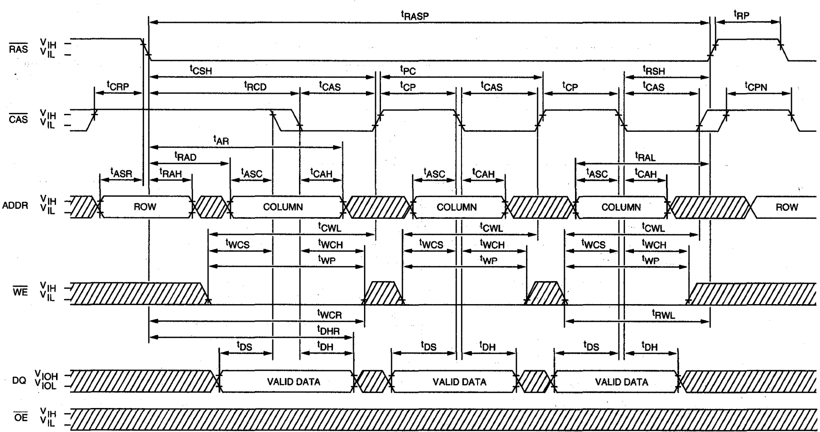
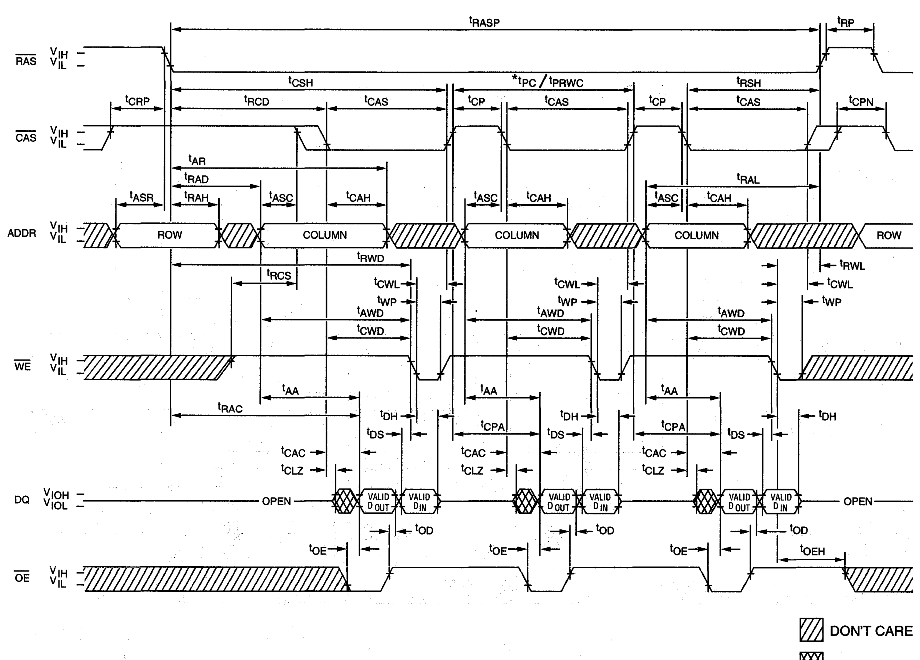
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



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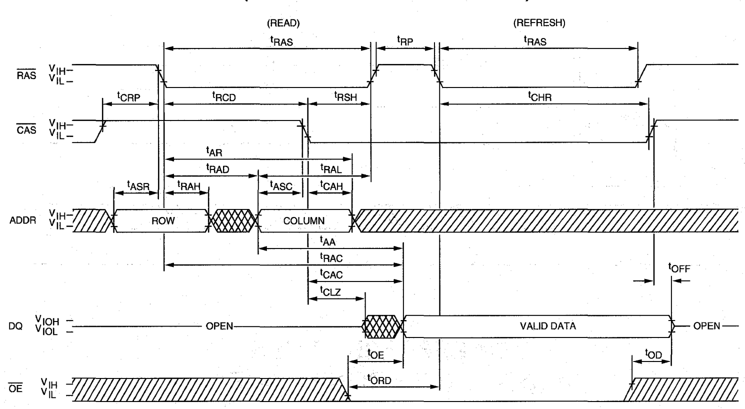
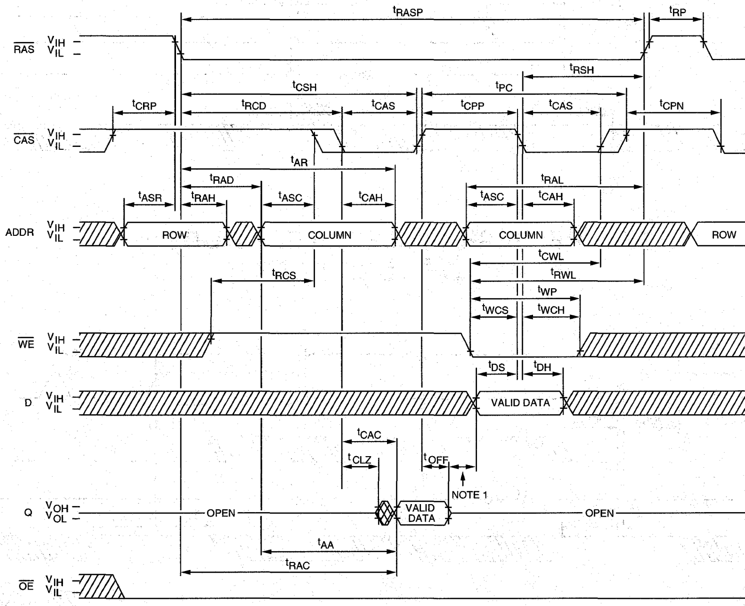
HIDDEN REFRESH CYCLE [24]

(WE = HIGH; OE = LOW)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to High-Z; that is completion of tOFF. tCPP is equal to tOFF + tDS(MIN) + guardband between data-out and driving new data-in.

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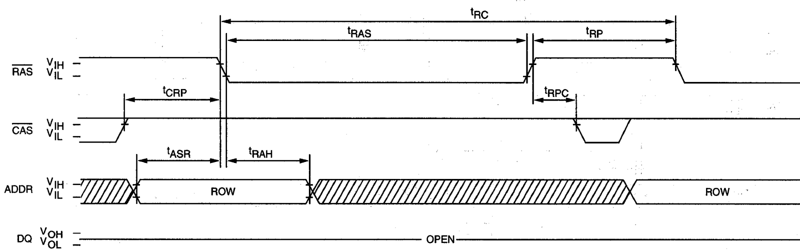
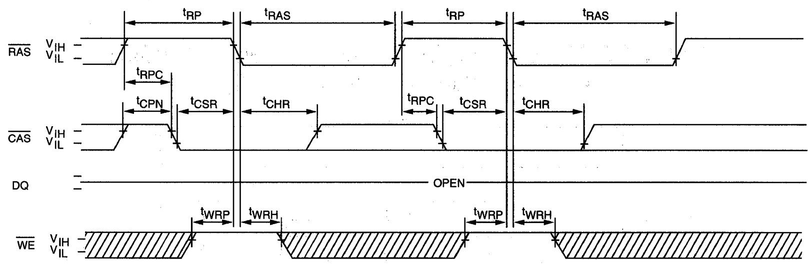
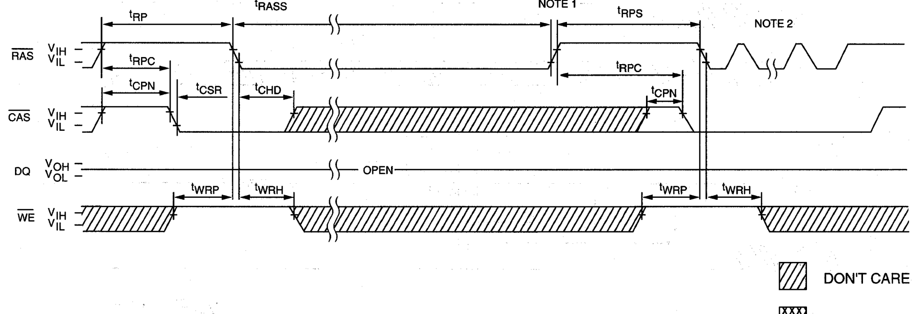
RAS ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



CBR REFRESH CYCLE
(A0-A10; OE = DON'T CARE)



SELF REFRESH CYCLE ("SLEEP MODE")
(A0-A10; OE = DON'T CARE)



NOTE:
1. Once tRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a compete burst of all rows should be executed.

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DRAM

2 MEG x 8 DRAM

3.3V EDO PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- Industry-standard x8 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single power supply: +3.3V ±0.3V
- Low power, 1.2mW standby; 200mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and SELF
- 2,048-cycle refresh (11 row-, 10 column-addresses)
- Optional SELF REFRESH, Extended Refresh rate (4X)
- Extended data-out (EDO) PAGE access cycle

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG
• Refresh	
Standard (2,048 cycles at 32ms)	none
SELF (2,048 cycles at 128ms)	S

- Part Number Example: MT4LC2M8E7DJ-6

GENERAL DESCRIPTION

The MT4LC2M8E7(S) is a randomly accessed solid-state memories containing 16,777,216 bits organized in a x8 configuration. The MT4LC2M8E7 RAS is used to latch the first 11 bits and CAS the latter 10 bits (A10 is ignored during CAS falling edge.) READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pins remain open (High-Z) until the next CAS cycle, regardless of OE.

If WE goes LOW after CAS goes LOW, data-out (Q) is activated and retains the selected cell data as long as OE remains LOW and RAS or CAS remains LOW (regardless of WE). This late WE pulse results in a READ WRITE cycle.

If WE toggles LOW after CAS goes back HIGH, the output pins will open (High- Z) until the next CAS cycle, regardless of OE.

PIN ASSIGNMENT (Top View)

28-Pin SOJ (DC-8) / 28-Pin TSOP (DD-3)

Pin	Name	Pin	Name
1	Vcc	28	Vss
2	DQ1	27	DQ8
3	DQ2	26	DQ7
4	DQ3	25	DQ6
5	DQ4	24	DQ5
6	WE	23	CAS
7	RAS	22	OE
8	NC	21	A9
9	A10	20	A8
10	A0	19	A7
11	A1	18	A6
12	A2	17	A5
13	A3	16	A4
14	Vcc	15	Vss

The eight data inputs and the eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by WE and OE.

PAGE ACCESS

PAGE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The PAGE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the PAGE MODE of operation.

EDO

The MT4C2M8E7 provides EDO PAGE MODE which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS returns HIGH. EDO provides for CAS precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS output control provides for pipeline READs.

FAST PAGE MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. EDO PAGE MODE DRAMs operate similar to FAST PAGE MODE DRAMs, except data will remain valid or

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become valid after $\overline{CAS}$ goes HIGH during READs, provided $\overline{RAS}$ and $\overline{OE}$ are held LOW. If $\overline{OE}$ is pulsed while $\overline{RAS}$ and $\overline{CAS}$ are LOW, data will toggle from valid data to High-Z and back to the same valid data. If $\overline{OE}$ is toggled or pulsed after $\overline{CAS}$ goes HIGH while $\overline{RAS}$ remains LOW, data will transition to and remain High-Z (refer to Figure 1).

If the DQ outputs are wire OR'd, $\overline{OE}$ must be used to disable idle banks of DRAMs. Alternatively, pulsing $\overline{WE}$ to the idle banks during $\overline{CAS}$ HIGH time will also High-Z the outputs. Independent of $\overline{OE}$ control, the outputs will disable after ^tOFF, which is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

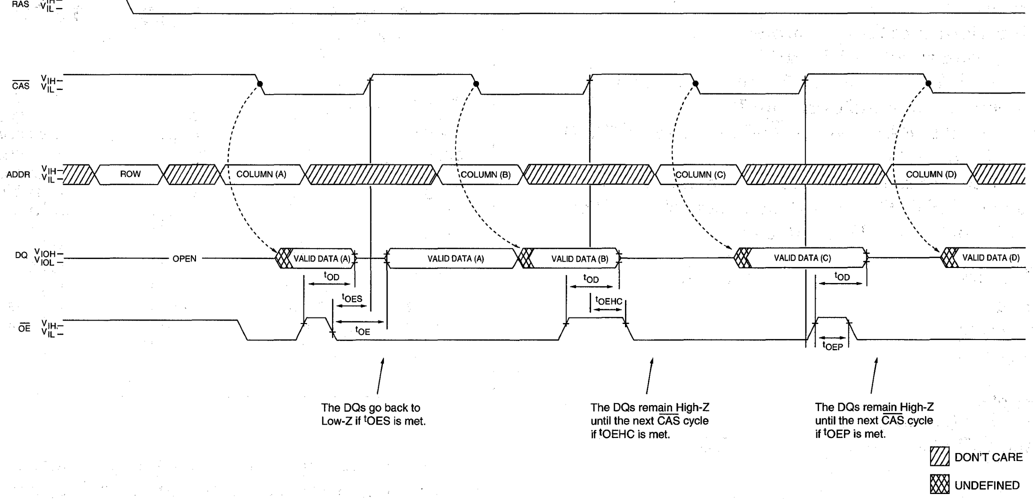

Figure 1
OUTPUT ENABLE AND DISABLE

REFRESH

Preserve correct memory cell data by maintaining power and executing a $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all 2,048 combinations of $\overline{RAS}$ addresses are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

An optional SELF REFRESH mode is also available on the MT4LC2M8E7 S. The "S" option allows the user the choice of a fully static low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms, four times longer than the standard 32ms specification.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified ^tRASS. Additionally, the "S" option allows for an extended refresh rate of 62.5µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby or BATTERY BACKUP mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of ^tRPS ($\approx{}^tRC$). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a BURST REFRESH is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or BURST REFRESH sequence, all 2,048 rows must be refreshed within 600µs prior to the resumption of normal operation.

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DRAM

256K x 16 DRAM

FAST PAGE MODE

FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply*
- Low power, 3mW standby; 375mW active, typical
- All device pins are fully TTL-compatible
- 512-cycle refresh in 8ms (nine rows and nine columns)
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C16257 only)

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6*
70ns access	-7
80ns access	-8
• Write Cycle Access	
BYTE or WORD via WE	16256
BYTE or WORD via CAS	16257
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

- Part Number Example: MT4C16256DJ-7

*60ns specifications are limited to a Vcc range of ±5%.

PIN ASSIGNMENT (Top View)

40-Pin SOJ (DC-6)

Signal	Pin	Pin	Signal
Vcc	1	40	Vss
DQ1	2	39	DQ16
DQ2	3	38	DQ15
DQ3	4	37	DQ14
DQ4	5	36	DQ13
Vcc	6	35	Vss
DQ5	7	34	DQ12
DQ6	8	33	DQ11
DQ7	9	32	DQ10
DQ8	10	31	DQ9
NC	11	30	NC
*WEL/NC	12	29	NC/CASL*
*WEH/WE	13	28	CAS/CASH*
RAS	14	27	OE
NC	15	26	A8
A0	16	25	A7
A1	17	24	A6
A2	18	23	A5
A3	19	22	A4
Vcc	20	21	Vss

40/44-Pin TSOP (DD-5)

Signal	Pin	Pin	Signal
Vcc	1	44	Vss
DQ1	2	43	DQ16
DQ2	3	42	DQ15
DQ3	4	41	DQ14
DQ4	5	40	DQ13
Vcc	6	39	Vss
DQ5	7	38	DQ12
DQ6	8	37	DQ11
DQ7	9	36	DQ10
DQ8	10	35	DQ9
NC	13	32	NC
*WEL/NC	14	31	NC/CASL*
*WEH/WE	15	30	CAS/CASH*
RAS	16	29	OE
NC	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
Vcc	22	23	Vss

*MT4C16256 / MT4C16257

GENERAL DESCRIPTION

The MT4C16256/7 are randomly accessed solid-state memories containing 4,194,304 bits organized in a x16 configuration. The MT4C16256 has both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C16257 has both BYTE WRITE and WORD WRITE access cycles via two CAS pins.

The MT4C16256 and MT4C16257 function in the same manner except that WEL and WEH on MT4C16256 and CASL and CASH on MT4C16257 control the selection of byte WRITE access cycles. WEL and WEH function in an identical manner to WE in that either WEL or WEH will generate an internal WE. CASL and CASH function in an identical manner to CAS in that either CASL or CASH will generate an internal CAS.

The MT4C16256 WE function and timing are determined by the first WE (WEL or WEH) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. WEL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and WEH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C16257 CAS function and timing are determined by the first CAS (CASL or CASH) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. CASL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and CASH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through CASL or CASH in the same manner during READ cycles for the MT4C16257.

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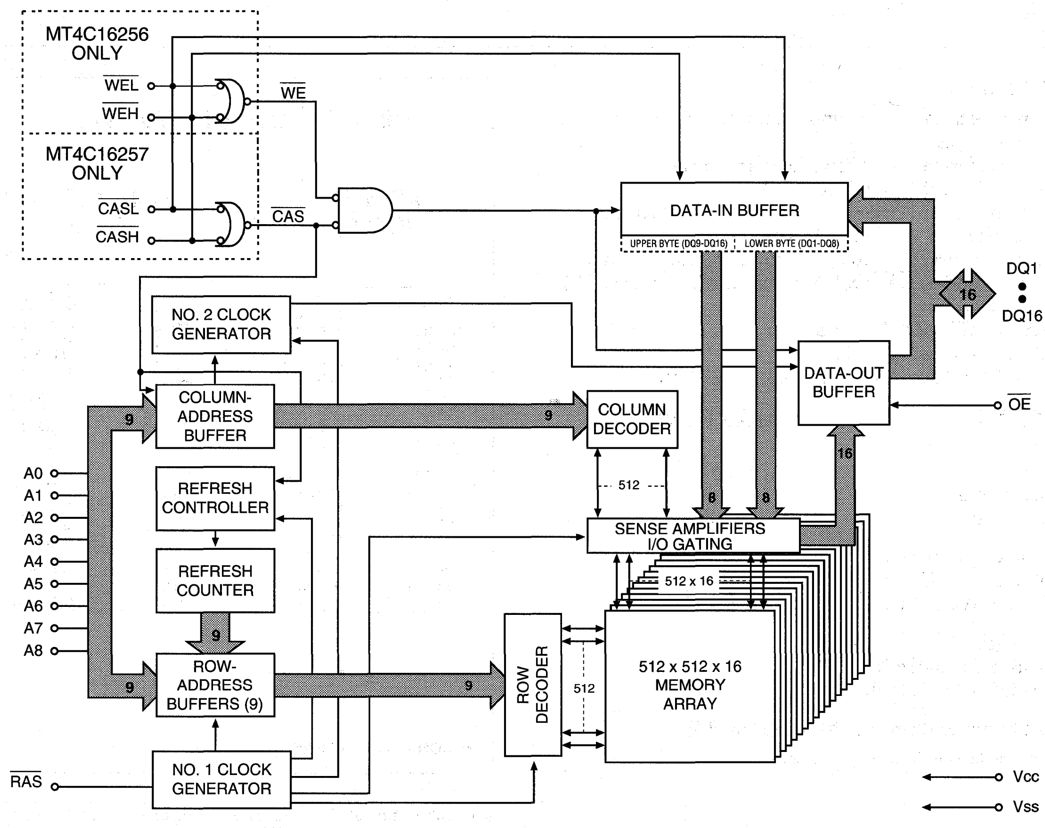
DRAM

FUNCTIONAL BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits.

The CAS control also determines whether the cycle will be a refresh cycle (RAS ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS goes LOW. The MT4C16256 has one CAS control while the MT4C16257 has two, CASL and CASH.

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input on the other 256K x 16 DRAMs. The key difference is each CAS controls its corresponding DQ tristate logic (in conjunction with OE and WE). CASL controls DQ1 through DQ8 and CASH controls DQ9 through DQ16.

The MT4C16257 CAS function is determined by the first CAS (CASL or CASH) to transition LOW and the last one to transition back HIGH. The two CAS controls give the MT4C16257 both BYTE READ and BYTE WRITE cycle capabilities.

READ or WRITE cycles on the MT4C16257 are selected with the WE input while either WEL or WEH perform the WE on the MT4C16256. The MT4C16256 WE function is determined by the first BYTE WRITE (WEL or WEH) to transition LOW and the last one to transition back HIGH.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High- Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O and pin direction is controlled by OE , WEL and WEH (MT4C16256) or WE (MT4C16257).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR, or HIDDEN) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of WEL and WEH or CASL and CASH. Enabling WEL/ CASL will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling WEH or CASH will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both WEL and WEH or CASL and CASH selects a WORD WRITE cycle.

The MT4C16256 and MT4C16257 can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the WE or the CAS inputs. Figure 1 illustrates the MT4C16256 BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C16257 BYTE WRITE and WORD WRITE cycles.

The MT4C16257 also has BYTE READ and WORD READ cycles, since it uses two CAS inputs to control its byte accesses. Figure 3 illustrates the MT4C16257 BYTE READ and WORD READ cycles.

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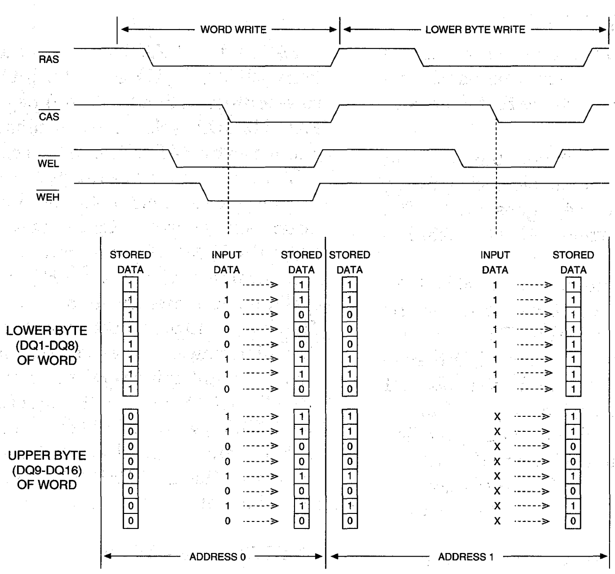

Figure 1
MT4C16256 WORD AND BYTE WRITE EXAMPLE

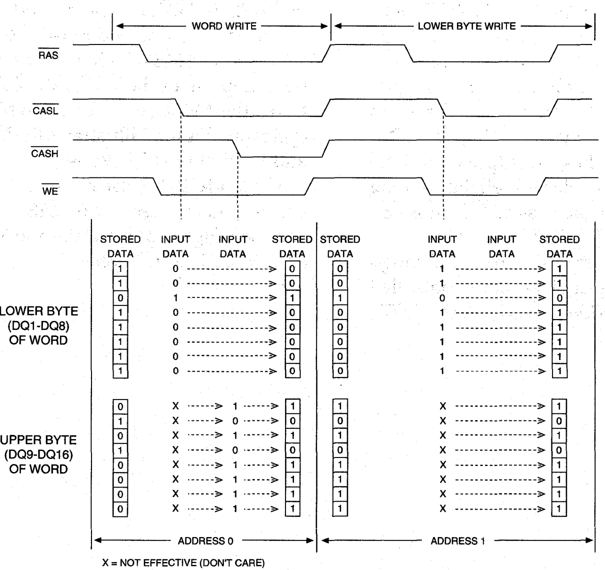

Figure 2
MT4C16257 WORD AND BYTE WRITE EXAMPLE

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DRAM

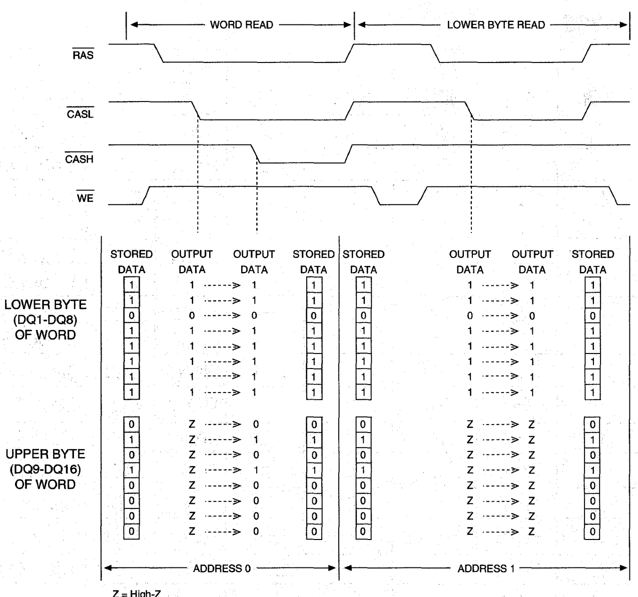

Figure 3
MT4C16257 WORD AND BYTE READ EXAMPLE

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DRAM

TRUTH TABLE: MT4C16256

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES ^tR	ADDRESSES ^tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data-Out	
PAGE-MODE WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 2
RAS ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY WRITE only.

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TRUTH TABLE: MT4C16257

FUNCTION		$\overline{RAS}$	$\overline{CASL}$	$\overline{CASH}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
$\overline{RAS}$ ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
3. EARLY WRITE only.
4. At least one of the two $\overline{CAS}$ signals must be active ($\overline{CASL}$ or $\overline{CASH}$).

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DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%**)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6**	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	ICC2	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	195	175	160	mA	3, 4, 41
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN]; tCP, tASC = 10ns)	ICC4	120	110	100	mA	3, 4, 41
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS=VIH: tRC = tRC [MIN])	ICC5	195	175	160	mA	3, 41
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC6	180	160	140	mA	3, 5

**60ns specifications are limited to a Vcc range of ±5%.

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DRAM

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: RAS, CAS/(CASL,CASH), (WEL, WEH)/ WE, OE	C_{I2}	7	pF	2
Input/Output Capacitance: DQ (SOJ, TSOP)	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%*)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
READ WRITE cycle time	^{t}RWC	150		175		195		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		45		ns	34
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	85		95		100		ns	34
Access time from RAS	^{t}RAC		60		70		80	ns	14
Access time from CAS	^{t}CAC		15		20		20	ns	15, 32
Output Enable time	^{t}OE		15		20		20	ns	32
Access time from column-address	^{t}AA		30		35		40	ns	
Access time from CAS precharge	^{t}CPA		35		40		45	ns	32
RAS pulse width	^{t}RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^{t}RSH	15		20		20		ns	39
RAS precharge time	^{t}RP	40		50		60		ns	
CAS pulse width	^{t}CAS	15	100,000	20	100,000	20	100,000	ns	38
CAS hold time	^{t}CSH	60		70		80		ns	31
CAS precharge time	^{t}CPN	10		10		10		ns	16, 35
CAS precharge time (PAGE MODE)	^{t}CP	10		10		10		ns	35
RAS to CAS delay time	^{t}RCD	20	45	20	50	20	60	ns	17, 30
CAS to RAS precharge time	^{t}CRP	10		10		10		ns	31
Row-address setup time	^{t}ASR	0		0		0		ns	
Row-address hold time	^{t}RAH	10		10		10		ns	
RAS to column-address delay time	^{t}RAD	15	30	15	35	15	40	ns	18
Column-address setup time	^{t}ASC	0		0		0		ns	30
Column-address hold time	^{t}CAH	10		15		15		ns	30
Column-address hold time (referenced to RAS)	^{t}AR	50		55		60		ns	
Column-address to RAS lead time	^{t}RAL	30		35		40		ns	
Read command setup time	^{t}RCS	0		0		0		ns	26, 30
Read command hold time (referenced to CAS)	^{t}RCH	0		0		0		ns	19, 26 ,31

*60ns specifications are limited to a Vcc range of ±5%.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%*)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	32
Output buffer turn-off delay	^tOFF	3	15	3	15	3	15	ns	20, 28, 32
Output disable time	^tOD	3	15	3	15	3	15	ns	28, 40
Write command setup time	^tWCS	0		0		0		ns	21, 26, 30
Write command hold time	^tWCH	10		10		10		ns	26, 39
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	26
Write command pulse width	^tWP	10		10		10		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26, 31
Data-in setup time	^tDS	0		0		0		ns	22, 32
Data-in hold time	^tDH	10		15		15		ns	22, 32
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21, 30
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5, 30
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5, 31
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	27
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ returning HIGH	^tCLCH	10		10		10		ns	33

*60ns specifications are limited to a Vcc range of ±5%.

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 5V ±10%;f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ${}^tREF$ refresh requirement is exceeded.
8. AC characteristics assume ${}^tT$ = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OL} = 0.80 and V_{OH} = 2.0V.
14. Assumes that ${}^tRCD$ < ${}^tRCD$ (MAX). If ${}^tRCD$ is greater than the maximum recommended value shown in this table, ${}^tRAC$ will increase by the amount that ${}^tRCD$ exceeds the value shown.
15. Assumes that ${}^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ${}^tCPN$.
17. Operation within the ${}^tRCD$ (MAX) limit ensures that ${}^tRAC$ (MAX) can be met. ${}^tRCD$ (MAX) is specified as a reference point only; if ${}^tRCD$ is greater than the specified ${}^tRCD$ (MAX) limit, access time is controlled exclusively by ${}^tCAC$.
18. Operation within the ${}^tRAD$ limit ensures that ${}^tRCD$ (MAX) can be met. ${}^tRAD$ (MAX) is specified as a reference point only; if ${}^tRAD$ is greater than the specified ${}^tRAD$ (MAX) limit, access time is controlled exclusively by ${}^tAA$.
19. Either ${}^tRCH$ or ${}^tRRH$ must be satisfied for a READ cycle.
20. ${}^tOFF$ (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.*
21. ${}^tWCS$, ${}^tRWD$, ${}^tAWD$ and ${}^tCWD$ are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ${}^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ${}^tRWD \ge {}^tRWD$ (MIN), ${}^tAWD \ge {}^tAWD$ (MIN) and ${}^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C16256. Write command is defined as $\overline{WE}$ going LOW on the MT4C16257.
27. LATE WRITE and READ-MODIFY-WRITE cycles must have both ${}^tOD$ and ${}^tOEH$ met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ${}^tOEH$ is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. The DQs open during READ cycles once ${}^tOD$ or ${}^tOFF$ occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of the $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.

*The 3ns minimum is a parameter guaranteed by design.

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DRAM

NOTES (continued)

29. Notes 31 through 41 apply to MT4C16257 only.
30. The first $\overline{CAS}$x edge to transition LOW.
31. The last $\overline{CAS}$x edge to transition HIGH.
32. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input, DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
33. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
34. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
35. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
36. First DQs controlled by the first $\overline{CAS}$x to go LOW.
37. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
38. Each $\overline{CAS}$x must meet minimum pulse width.
39. Last $\overline{CAS}$x to go LOW.
40. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
41. Column-address changed once each cycle.

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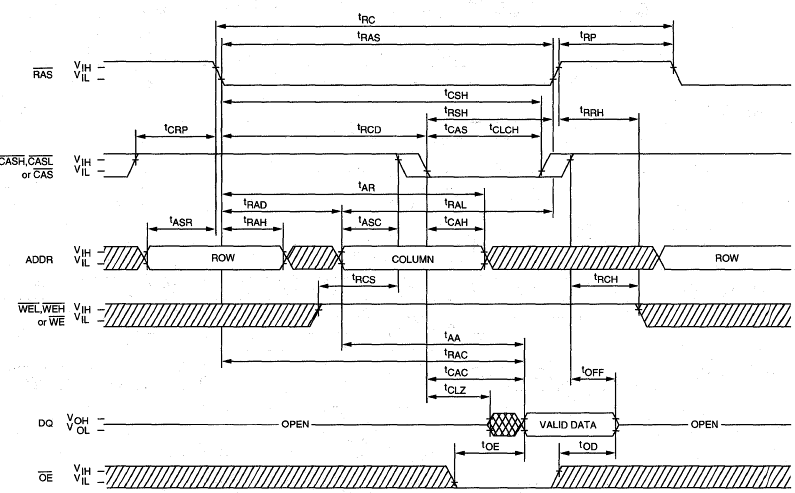
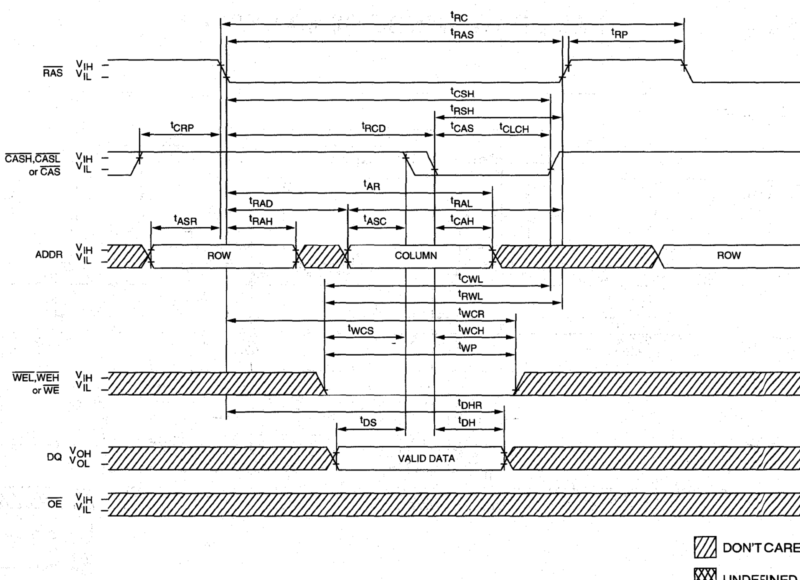
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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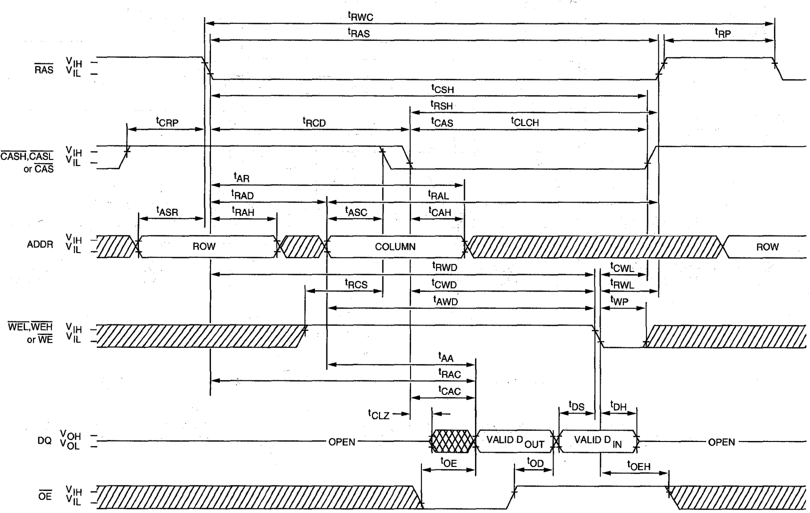
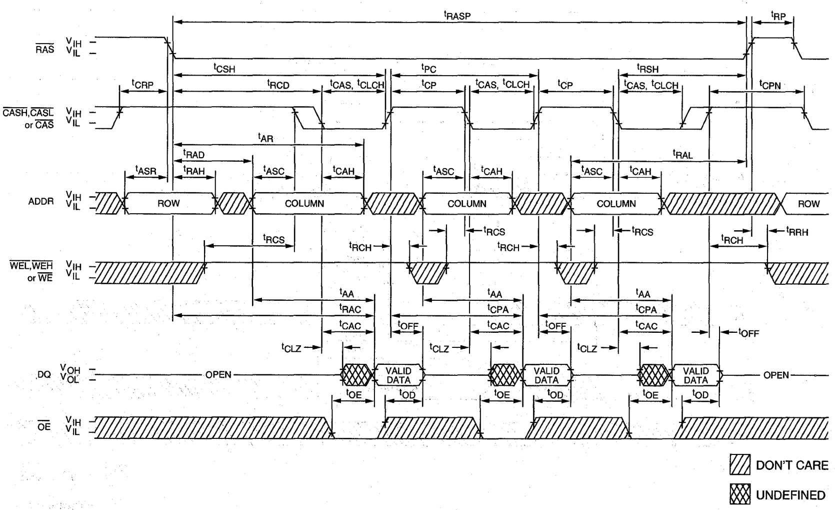
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

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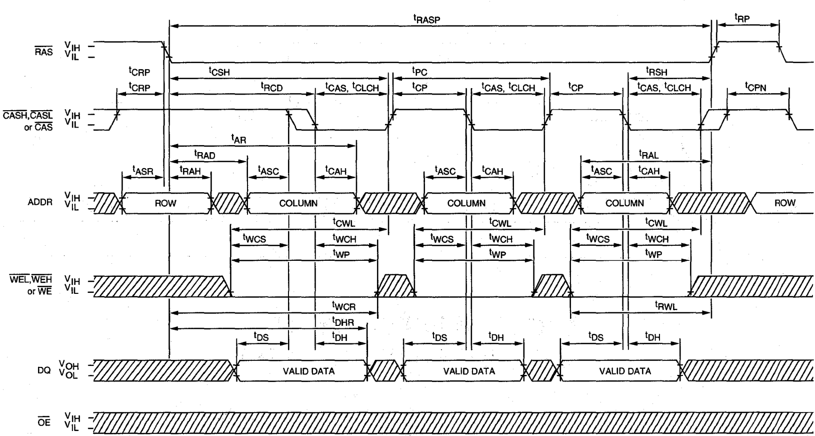
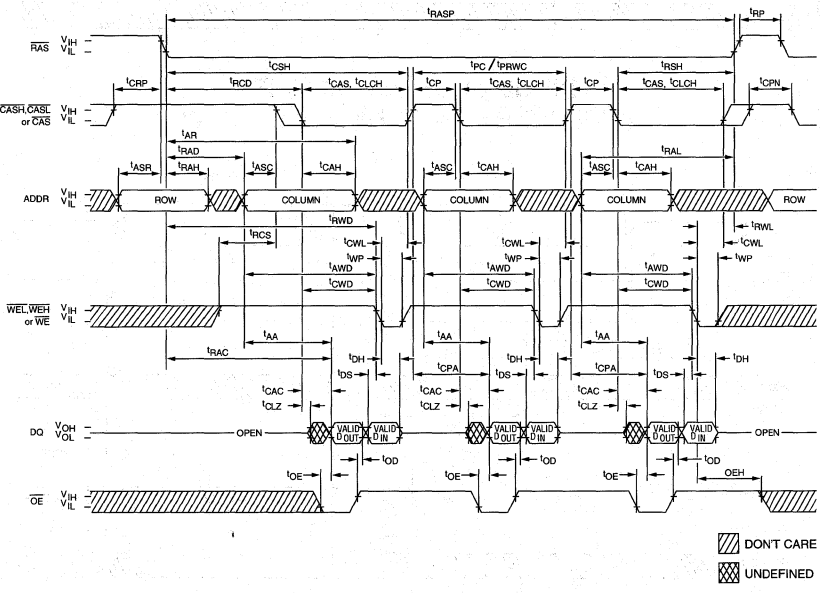
DRAM

FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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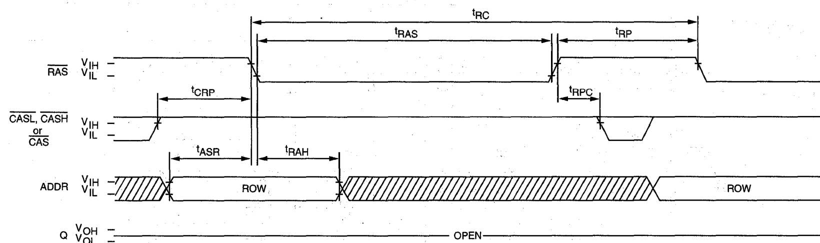
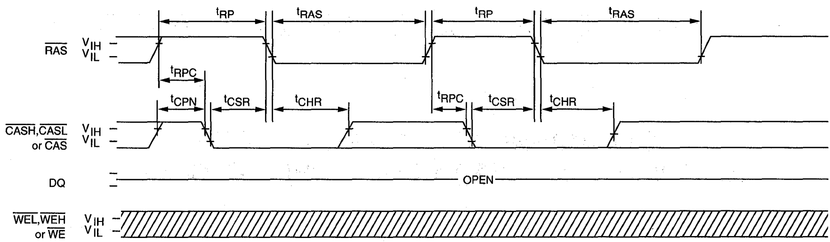
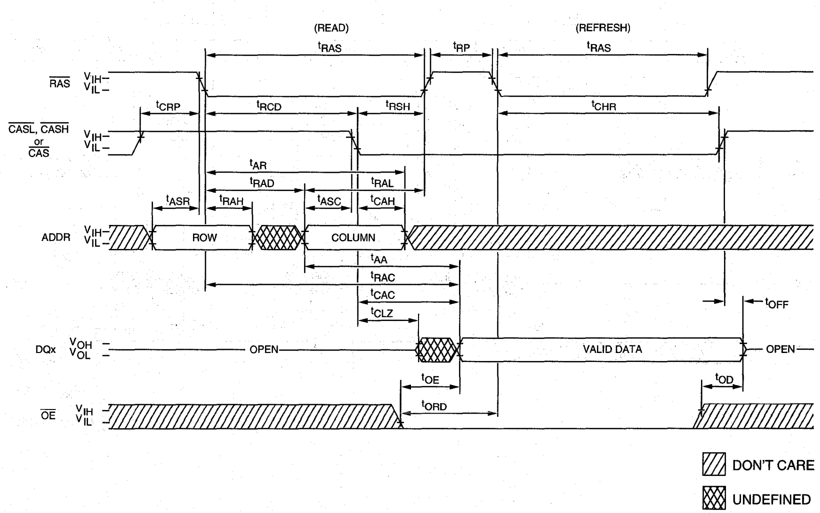
RAS ONLY REFRESH CYCLE
(ADDR = A0-A8; OE, WEL, WEH or WE = DON'T CARE)



CBR REFRESH CYCLE
(A0-A8; OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
(WEL, WEH or WE = HIGH; OE = LOW)



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DRAM

256K x 16 DRAM

3.3V FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply*
- Low power, 0.3mW standby; 175mW active, typical
- All device pins are fully LVTTL-compatible
- 512-cycle refresh in 8ms (MT4LC16256/7) or 64ms (MT4LC16256/7 S)
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and optional Extended and SELF
- FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4LC16257(S) only)
- Symmetrical addressing (nine rows, nine columns)

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6*
70ns access	-7
80ns access	-8
• Write Cycle Access	
BYTE or WORD via WE	16256
BYTE or WORD via CAS	16257
BYTE or WORD via WE SELF REFRESH and Extended Refresh	16256 S
BYTE or WORD via CAS SELF REFRESH and Extended Refresh	16257 S
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

- Part Number Example: MT4LC16257DJ-7 S

*60ns specifications are limited to a Vcc range of ±0.15V.

PIN ASSIGNMENT (Top View)

40-Pin SOJ (DC-6)

Signal	Pin	Pin	Signal
Vcc	1	40	Vss
DQ1	2	39	DQ16
DQ2	3	38	DQ15
DQ3	4	37	DQ14
DQ4	5	36	DQ13
Vcc	6	35	Vss
DQ5	7	34	DQ12
DQ6	8	33	DQ11
DQ7	9	32	DQ10
DQ8	10	31	DQ9
NC	11	30	NC
*WEL/NC	12	29	NC/CASL*
*WEH/WE	13	28	CAS/CASH*
RAS	14	27	OE
NC	15	26	A8
A0	16	25	A7
A1	17	24	A6
A2	18	23	A5
A3	19	22	A4
Vcc	20	21	Vss

40/44-Pin TSOP (DD-5)

Signal	Pin	Pin	Signal
Vcc	1	44	Vss
DQ1	2	43	DQ16
DQ2	3	42	DQ15
DQ3	4	41	DQ14
DQ4	5	40	DQ13
Vcc	6	39	Vss
DQ5	7	38	DQ12
DQ6	8	37	DQ11
DQ7	9	36	DQ10
DQ8	10	35	DQ9
NC	13	32	NC
*WEL/NC	14	31	NC/CASL*
*WEH/WE	15	30	CAS/CASH*
RAS	16	29	OE
NC	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
Vcc	22	23	Vss

*MT4LC16256(S)/MT4LC16257(S)

GENERAL DESCRIPTION

The MT4LC16256/7(S) are randomly accessed solid-state memories containing 4,194,304 bits organized in a x16 configuration. The MT4LC16256(S) has both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4LC16257(S) has both BYTE WRITE and WORD WRITE access cycles via two CAS pins.

The MT4LC16256(S) and MT4LC16257(S) function in the same manner except that WEL and WEH on MT4LC16256 and CASL and CASH on MT4LC16257 control the selection of byte WRITE access cycles. WEL and WEH function in an identical manner to WE in that either WEL or WEH will generate an internal WE. CASL and CASH function in an identical manner to CAS in that either CASL or CASH will generate an internal CAS.

The MT4LC16256(S) WE function and timing are determined by the first WE (WEL or WEH) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. WEL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and WEH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4LC16257(S) CAS function and timing are determined by the first CAS (CASL or CASH) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. CASL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and CASH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through CASL or CASH in the same manner during READ cycles for the MT4LC16257(S).

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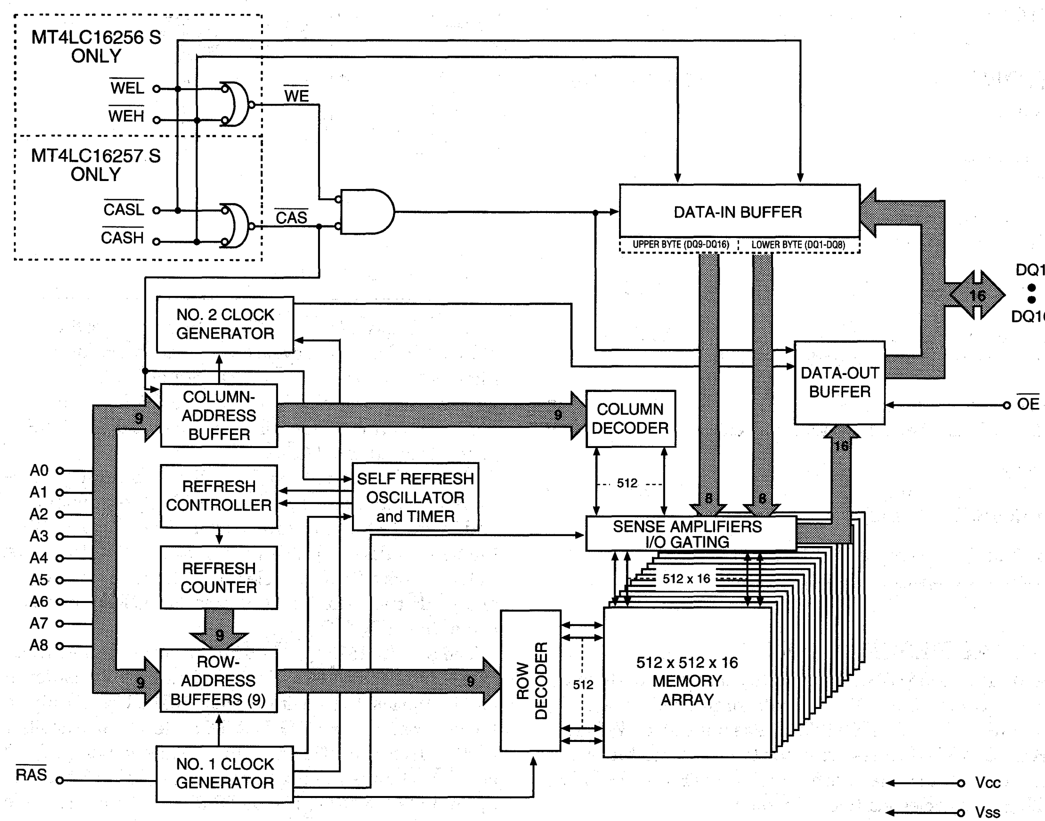
REFRESH

An optional SELF REFRESH mode is also available. The "S" option allows the user the choice of a fully static low-power data retention mode or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding $\overline{\text{RAS}}$ LOW for the specified ^{t}RASS. Additionally, the "S" option allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving $\overline{\text{RAS}}$ HIGH for a minimum time of ^{t}RPS (≈^{t}RC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{\text{RAS}}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{\text{RAS}}$ ONLY or BURST REFRESH sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM



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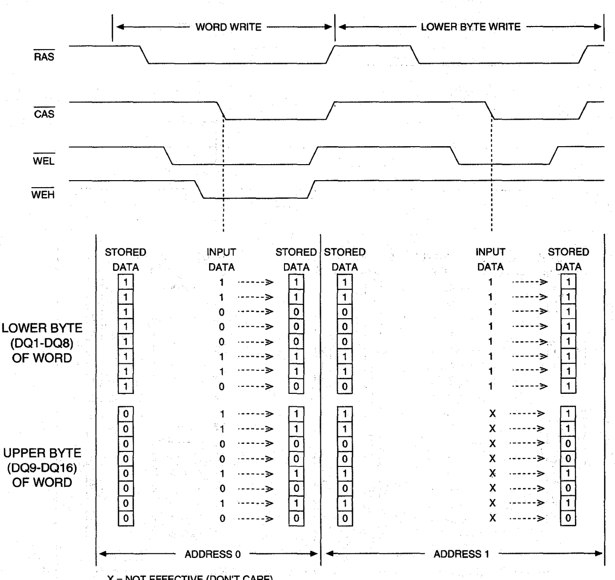

Figure 1
MT4LC16256(S) WORD AND BYTE WRITE EXAMPLE

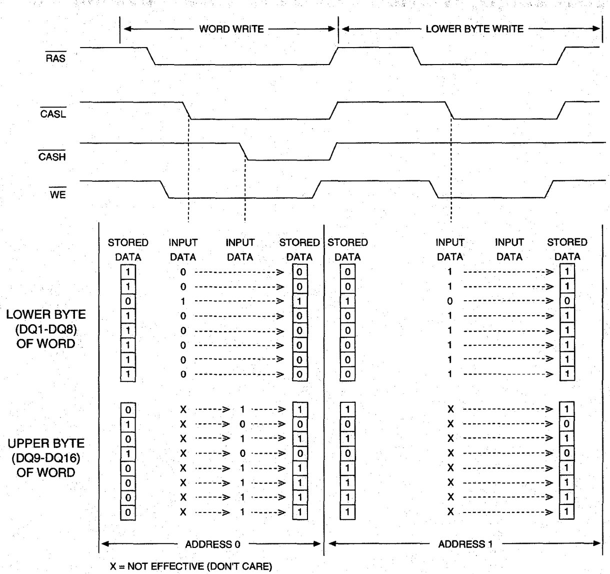

Figure 2
MT4LC16257(S) WORD AND BYTE WRITE EXAMPLE

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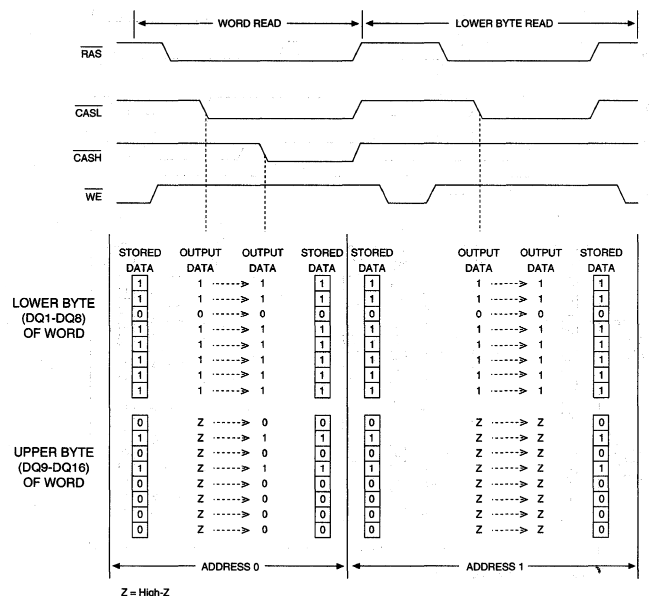

Figure 3
MT4LC16257(S) WORD AND BYTE READ EXAMPLE

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TRUTH TABLE: MT4LC16256(S)

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WEL}$	$\overline{WEH}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data-Out	
PAGE-MODE WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 2
$\overline{RAS}$ ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	X	X	X	X	X	High-Z	
SELF REFRESH (MT4C16256/7 S only)		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either $\overline{WEL}$ or $\overline{WEH}$ active).
2. EARLY WRITE only.

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TRUTH TABLE: MT4LC16257(S)

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES ᵗR	ADDRESSES ᵗC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
RAS ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4
SELF REFRESH (MT4C16256/7 S only)		H→L	L	X	X	X	X	X	High-Z	

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY WRITE only.
4. At least one of the two CAS signals must be active (CASL or CASH).

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = +3.3V ±0.3V**)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}**	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 3.6V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

**60ns specifications are limited to a Vcc range of ±0.15V.

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DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +3.3V ±0.3V**)

PARAMETER/CONDITION	VERSION	SYMBOL	MAX -6**	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC1}	1	1	1	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	MT4LC16256/7	I_{CC2}	500	500	500	µA	25
	MT4LC16256/7 S	I_{CC2}	100	100	100	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC3}	120	110	100	mA	3, 4, 41
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)		I_{CC4}	70	60	50	mA	3, 4, 41
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])		I_{CC5}	120	110	100	mA	3
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC6}	120	110	100	mA	3, 5
REFRESH CURRENT: Extended Average power supply current, $\overline{CAS}$ = 0.2V or CBR cycling; ^tRAS = ^tRAS (MIN); $\overline{WE}$, A0-A8 and D_{IN} = Vcc-0.2V or 0.2V (D_{IN} may be left open)	MT4LC16256/7 S	I_{CC7}	150	150	150	µA	3, 5
REFRESH CURRENT: SELF Average power supply current, CBR cycling with $^tRAS \geq {}^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc-0.2V; A0-A8 and D_{IN} = Vcc-0.2V or 0.2V (D_{IN} may be left open)	MT4LC16256/7 S	I_{CC8}	150	150	150	µA	5, 42

**60ns specifications are limited to a Vcc range of ±0.15V.

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: RAS, CAS/(CASL,CASH), (WEL, WEH)/ WE, OE	C_{I2}	7	pF	2
Input/Output Capacitance: DQ (SOJ, TSOP)	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V*)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ WRITE cycle time	tRWC	150		175		195		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	34
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	85		95		100		ns	34
Access time from RAS	tRAC		60		70		80	ns	14
Access time from CAS	tCAC		15		20		20	ns	15, 32
Output Enable time	tOE		15		20		20	ns	32
Access time from column-address	tAA		30		35		40	ns	
Access time from CAS precharge	tCPA		35		40		45	ns	32
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15		20		20		ns	39
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	38
CAS hold time	tCSH	60		70		80		ns	31
CAS precharge time	tCPN	10		10		10		ns	16, 35
CAS precharge time (PAGE MODE)	tCP	10		10		10		ns	35
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	17, 30
CAS to RAS precharge time	tCRP	5		5		5		ns	31
Row-address setup time	tASR	0		0		0		ns	
Row-address hold time	tRAH	10		10		10		ns	
RAS to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		0		ns	30
Column-address hold time	tCAH	10		15		15		ns	30
Column-address hold time (referenced to RAS)	tAR	50		55		60		ns	
Column-address to RAS lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	26, 30
Read command hold time (referenced to CAS)	tRCH	0		0		0		ns	19, 26, 31

*60ns specifications are limited to a Vcc range of ±0.15V.

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NEW DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V*)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	32
Output buffer turn-off delay	^tOFF	3	15	3	15	3	15	ns	20, 28, 32
Output disable time	^tOD	3	15	3	15	3	15	ns	28, 40
Write command setup time	^tWCS	0		0		0		ns	21, 26, 30
Write command hold time	^tWCH	10		10		10		ns	26, 39
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	26
Write command pulse width	^tWP	10		10		10		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26, 31
Data-in setup time	^tDS	0		0		0		ns	22, 32
Data-in hold time	^tDH	10		15		15		ns	22, 32
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21, 30
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles) MT4LC16256/7 / MT4LC16256/7S	^tREF		8/64		8/64		8/64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5, 30
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5, 31
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	27
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ returning HIGH	^tCLCH	10		10		10		ns	33
$\overline{RAS}$ pulse width entering SELF REFRESH	^tRASS	100		100		100		µs	42
$\overline{RAS}$ precharge time exiting SELF REFRESH	^tRPS	110		130		150		µs	42
$\overline{CAS}$ hold time entering SELF REFRESH	^tCHD	10		10		10		ns	42

*60ns specifications are limited to a Vcc range of ±0.15V.

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +3.3V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If $\overline{CAS}$ = VIH, data output is High-Z.
12. If $\overline{CAS}$ = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gates and 50pF, VOL = 0.80 and VOH = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL. The 3ns minimum is a parameter guaranteed by design.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4LC16256(S). Write command is defined as $\overline{WE}$ going LOW on the MT4LC16257(S).
27. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of the $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.

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NOTES (continued)

29. Notes 30 through 40 apply to MT4LC16257(S) only.
30. The first $\overline{CAS}$x edge to transition LOW.
31. The last $\overline{CAS}$x edge to transition HIGH.
32. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input, DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
33. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
34. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
35. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
36. First DQs controlled by the first $\overline{CAS}$x to go LOW.
37. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
38. Each $\overline{CAS}$x must meet minimum pulse width.
39. Last $\overline{CAS}$x to go LOW.
40. All DQs controlled, regardless of $\overline{CASL}$ and $\overline{CASH}$.
41. Column-address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
42. If the DRAM controller uses a BURST REFRESH, a BURST REFRESH of all rows must be executed upon exiting SELF REFRESH.

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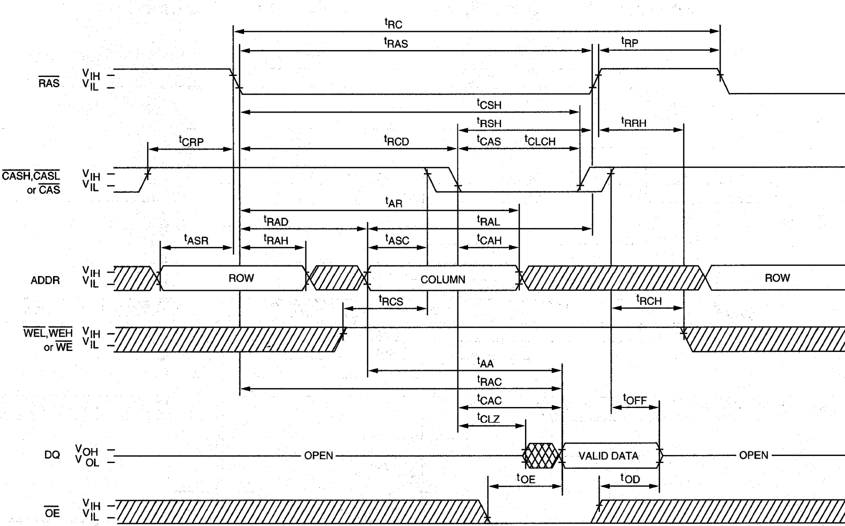
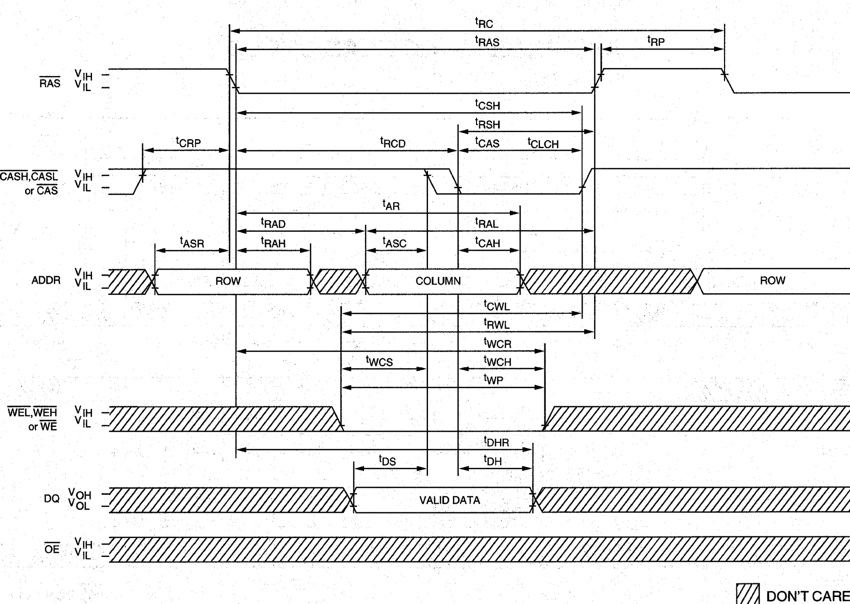
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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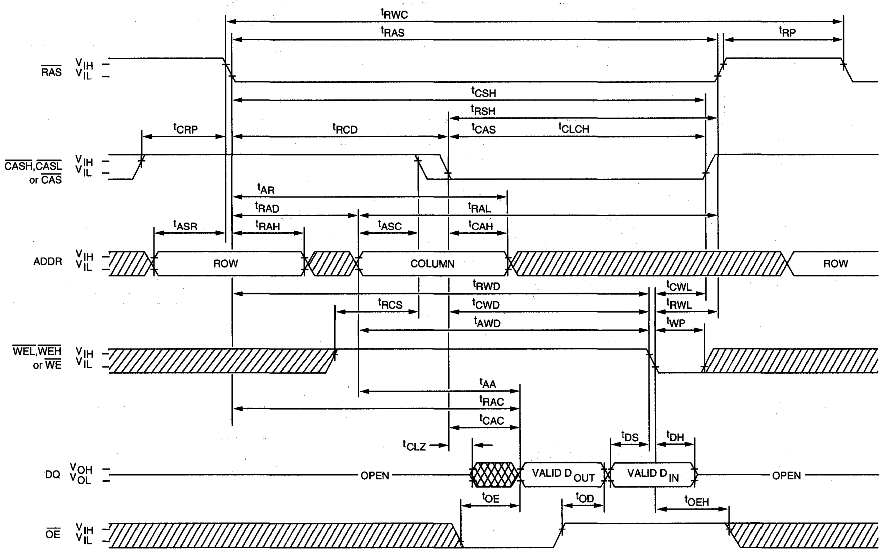
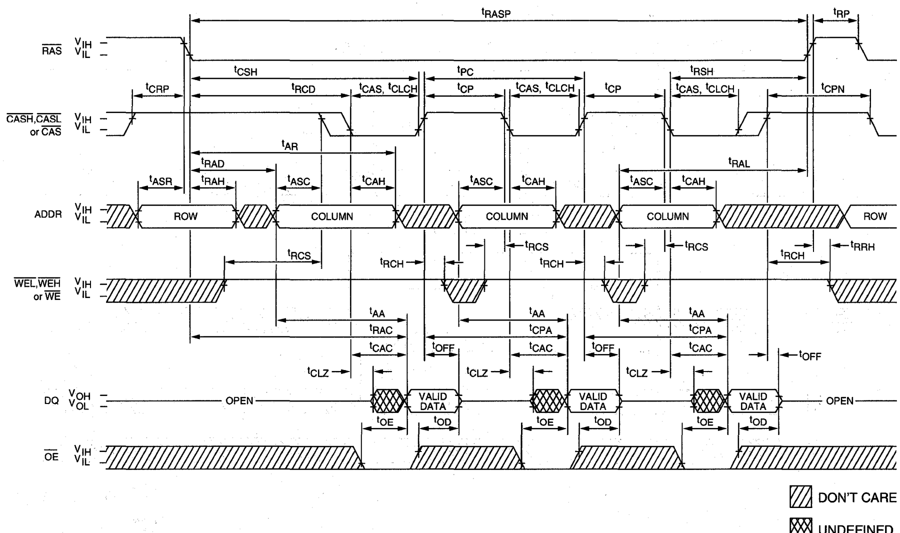
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



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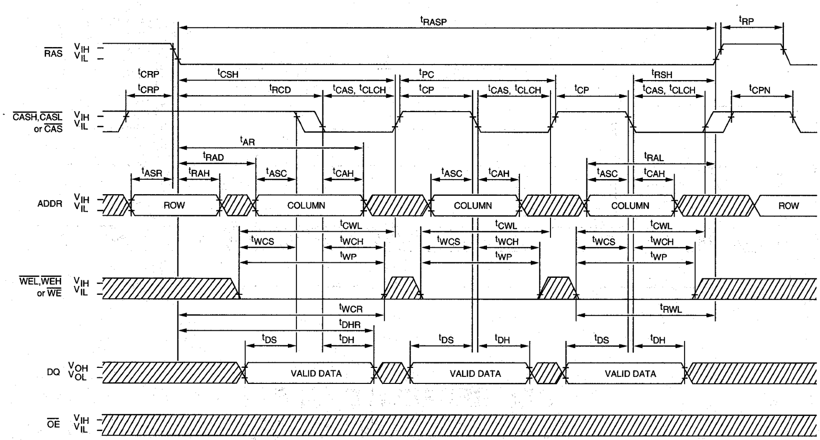
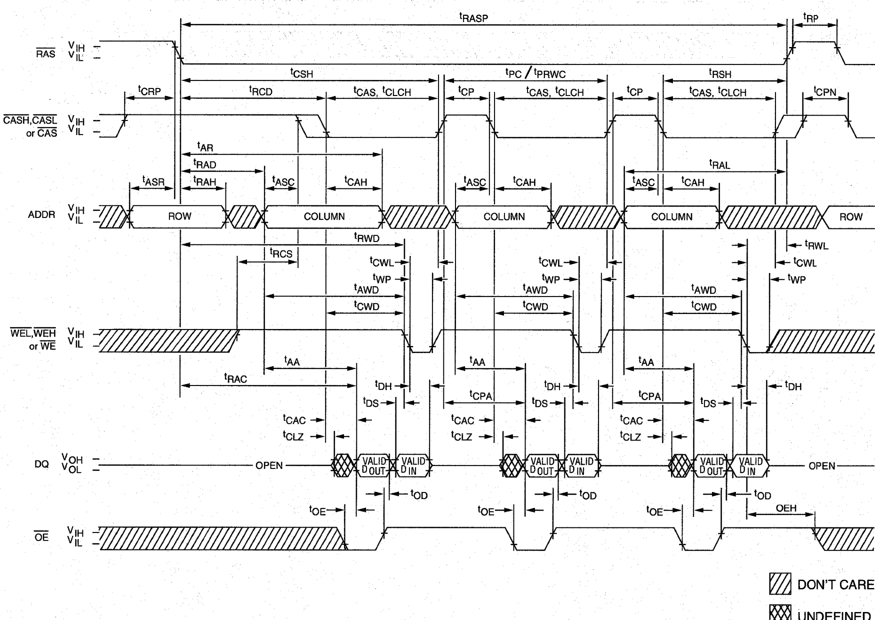
FAST-PAGE-MODE EARLY WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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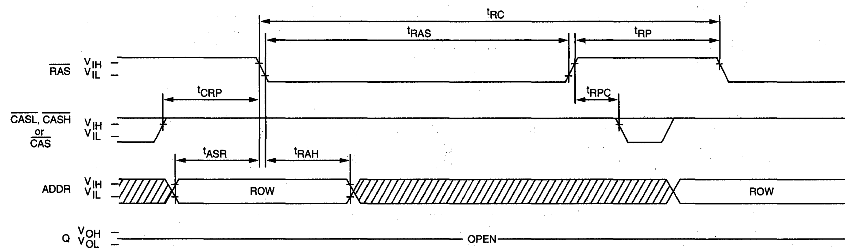
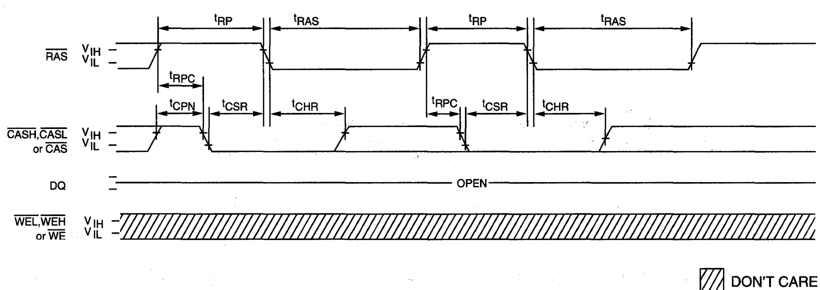
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A0-A8; $\overline{OE}$, $\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$ = DON'T CARE)



CBR REFRESH CYCLE

(A0-A8; $\overline{OE}$ = DON'T CARE)



DON'T CARE

UNDEFINED

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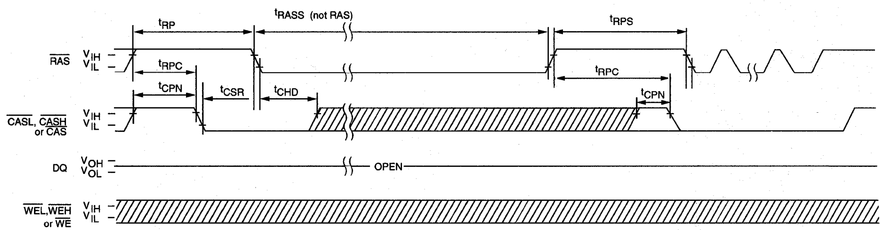
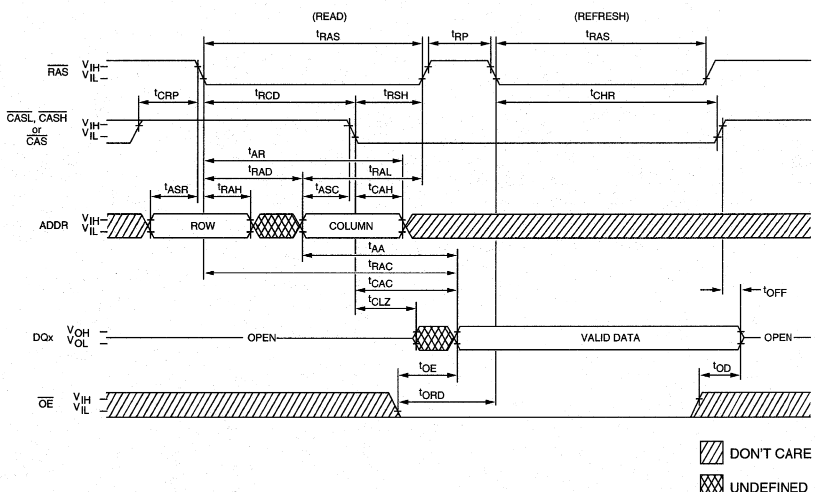
SELF REFRESH CYCLE
(A0-A8; $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE 24
($\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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DRAM

256K x 16 DRAM

EDO PAGE MODE

FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply*
- Low power, 3mW standby; 375mW active, typical
- All device pins are TTL-compatible
- 512-cycle refresh in 8ms (nine rows and nine columns)
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- Extended data-out (EDO) PAGE MODE access cycle
- BYTE WRITE and BYTE READ access cycles

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6*
70ns access	-7
80ns access	-8
• Write Cycle Access	
BYTE or WORD via $\overline{\text{CAS}}$	16270
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

- Part Number Example: MT4C16270DJ-7

*60ns specifications are limited to a Vcc range of ±5%. Contact factory for availability of 60ns.

PIN ASSIGNMENT (Top View)

40-Pin SOJ (DC-6)

Signal	Pin	Pin	Signal
Vcc	1	40	Vss
DQ1	2	39	DQ16
DQ2	3	38	DQ15
DQ3	4	37	DQ14
DQ4	5	36	DQ13
Vcc	6	35	Vss
DQ5	7	34	DQ12
DQ6	8	33	DQ11
DQ7	9	32	DQ10
DQ8	10	31	DQ9
NC	11	30	NC
NC	12	29	$\overline{\text{CASL}}$
$\overline{\text{WE}}$	13	28	$\overline{\text{CASH}}$
$\overline{\text{RAS}}$	14	27	$\overline{\text{OE}}$
NC	15	26	A8
A0	16	25	A7
A1	17	24	A6
A2	18	23	A5
A3	19	22	A4
Vcc	20	21	Vss

40/44-Pin TSOP (DD-5)

Signal	Pin	Pin	Signal
Vcc	1	44	Vss
DQ1	2	43	DQ16
DQ2	3	42	DQ15
DQ3	4	41	DQ14
DQ4	5	40	DQ13
Vcc	6	39	Vss
DQ5	7	38	DQ12
DQ6	8	37	DQ11
DQ7	9	36	DQ10
DQ8	10	35	DQ9
NC	13	32	NC
NC	14	31	$\overline{\text{CASL}}$
$\overline{\text{WE}}$	15	30	$\overline{\text{CASH}}$
$\overline{\text{RAS}}$	16	29	$\overline{\text{OE}}$
NC	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
Vcc	22	23	Vss

GENERAL DESCRIPTION

The MT4C16270 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x16 configuration. The MT4C16270 has both BYTE WRITE and WORD WRITE access cycles via two $\overline{\text{CAS}}$ pins.

The MT4C16270 offers an accelerated cycle access called EDO PAGE MODE.

The MT4C16270 $\overline{\text{CAS}}$ function and timing are determined by the first $\overline{\text{CAS}}$ ($\overline{\text{CASL}}$ or $\overline{\text{CASH}}$) to transition LOW and by the last to transition back HIGH. $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ function in an identical manner to $\overline{\text{CAS}}$ in that either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ will generate an internal $\overline{\text{CAS}}$. Use of only one of the two results in a BYTE WRITE cycle. $\overline{\text{CASL}}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{\text{CASH}}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ in the same manner.

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FUNCTIONAL BLOCK DIAGRAM

WE
CASL
CASH
CAS
CONTROL LOGIC
DATA-IN BUFFER
DQ1
16
DQ16
NO. 2 CLOCK GENERATOR
DATA-OUT BUFFER
COLUMN-ADDRESS BUFFER
9
COLUMN DECODER
OE
A0
A1
A2
A3
A4
A5
A6
A7
A8
REFRESH CONTROLLER
512
8
8
16
SENSE AMPLIFIERS I/O GATING
REFRESH COUNTER
512 x 16
9
ROW-ADDRESS BUFFERS (9)
ROW DECODER
512
512 x 512 x 16 MEMORY ARRAY
RAS
NO. 1 CLOCK GENERATOR
Vcc
Vss

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FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered nine bits (A0-A8) at a time. RAS is used to latch the first nine bits and CAS the latter nine bits.

The CAS control also determines whether the cycle will be a refresh cycle (RAS ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS goes LOW. The MT4C16270 has two CAS controls, CASL and CASH.

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input on the other 256K x 16 DRAMs. The key difference is that each CAS controls its corresponding DQ tristate logic (in conjunction with OE and WE and RAS). CASL controls DQ1 through DQ8 and CASH controls DQ9 through DQ16.

The MT4C16270 CAS function is determined by the first CAS (CASL or CASH) transitioning LOW and the last transitioning back HIGH. The two CAS controls give the MT4C16270 both byte READ and byte WRITE cycle capabilities.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High- Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by OE , WE and RAS.

EDO PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The EDO PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the EDO PAGE MODE operation.

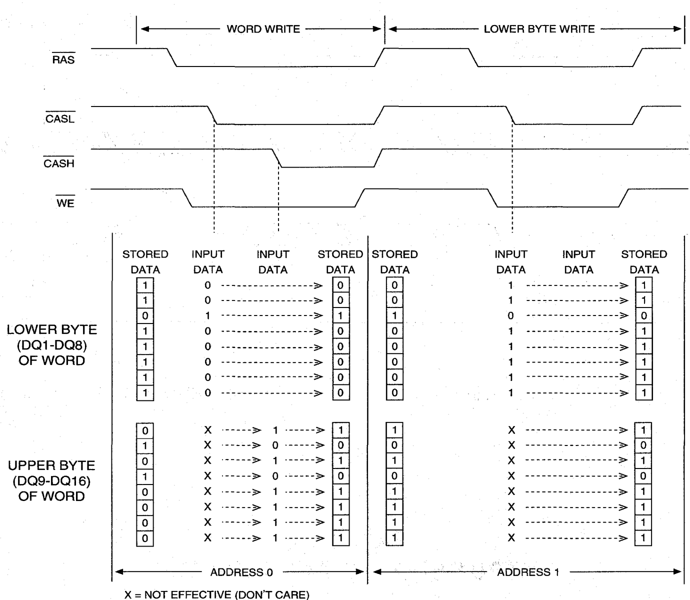

Figure 1
16270 WORD AND BYTE WRITE EXAMPLE

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BYTE ACCESS CYCLE

The BYTE WRITE cycle is determined by the use of $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$. Enabling $\overline{\text{CASL}}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling $\overline{\text{CASH}}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ selects a WORD WRITE cycle.

The MT4C16270 can be viewed as two 256K x 8 DRAMs which have common input controls. Figure 1 illustrates the MT4C16270 BYTE WRITE and WORD WRITE cycles. The BYTE READ is accomplished in the same manner.

EDO

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{\text{CAS}}$. If $\overline{\text{CAS}}$ goes HIGH, and $\overline{\text{OE}}$ is LOW (active), the output buffers will be disabled. The MT4C16270 offers an accelerated PAGE MODE cycle by eliminating output disable from $\overline{\text{CAS}}$ HIGH. This option is called EDO and it allows $\overline{\text{CAS}}$ precharge time (^{t}CP) to occur without the output data going invalid (see READ and EDO PAGE MODE READ waveforms).

EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after $\overline{\text{CAS}}$ goes HIGH, as long as $\overline{\text{RAS}}$ and $\overline{\text{OE}}$ are held LOW and $\overline{\text{WE}}$ is held HIGH. $\overline{\text{OE}}$ can be brought LOW or HIGH while $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ are LOW, and the DQs will transition between valid data and High-Z. Using $\overline{\text{OE}}$, there are two methods to disable the outputs and keep them disabled during the $\overline{\text{CAS}}$ HIGH time. The first method is to have $\overline{\text{OE}}$ HIGH when $\overline{\text{CAS}}$ transitions HIGH and keep $\overline{\text{OE}}$ HIGH for ^{t}OEHC. This will tristate the DQs and they will remain tristate, regardless of $\overline{\text{OE}}$, until $\overline{\text{CAS}}$ falls again. The second method is to have $\overline{\text{OE}}$ LOW when $\overline{\text{CAS}}$ transitions HIGH. Then $\overline{\text{OE}}$ can pulse HIGH for a minimum of ^{t}OEP anytime during the $\overline{\text{CAS}}$ HIGH period and the DQs will tristate and remain tristate, regardless of $\overline{\text{OE}}$, until $\overline{\text{CAS}}$ falls again (please reference Figure 2 for further detail on the

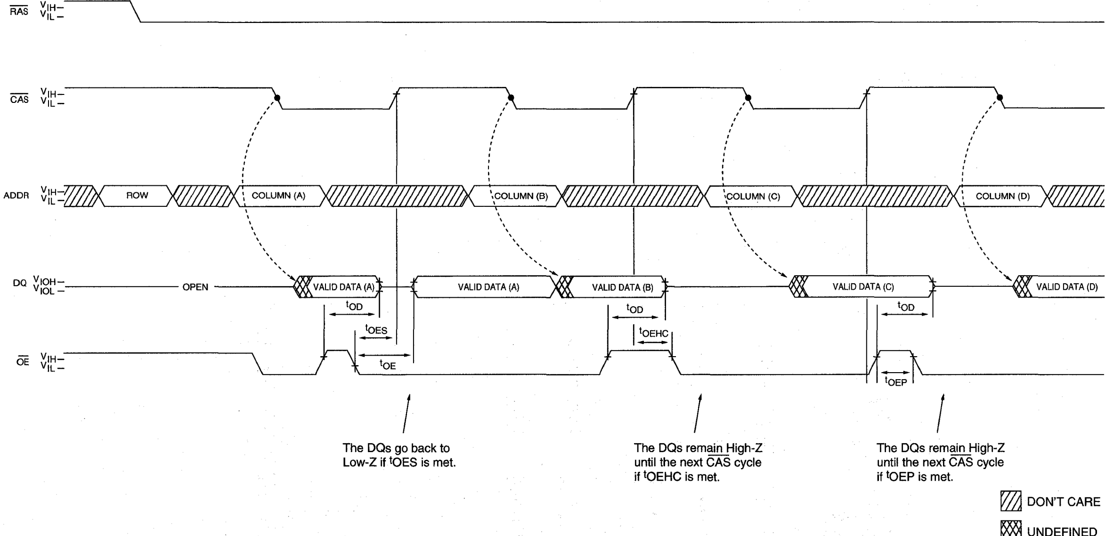

Figure 2
OUTPUT ENABLE AND DISABLE

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toggling $\overline{OE}$ condition). During other cycles, the outputs are disabled at tOFF time after $\overline{RAS}$ and $\overline{CAS}$ are HIGH, or tWHZ after $\overline{WE}$ transitions LOW. The tOFF time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last. $\overline{WE}$ can also perform the function of turning off the output drivers under certain conditions, as shown in Figure 3.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

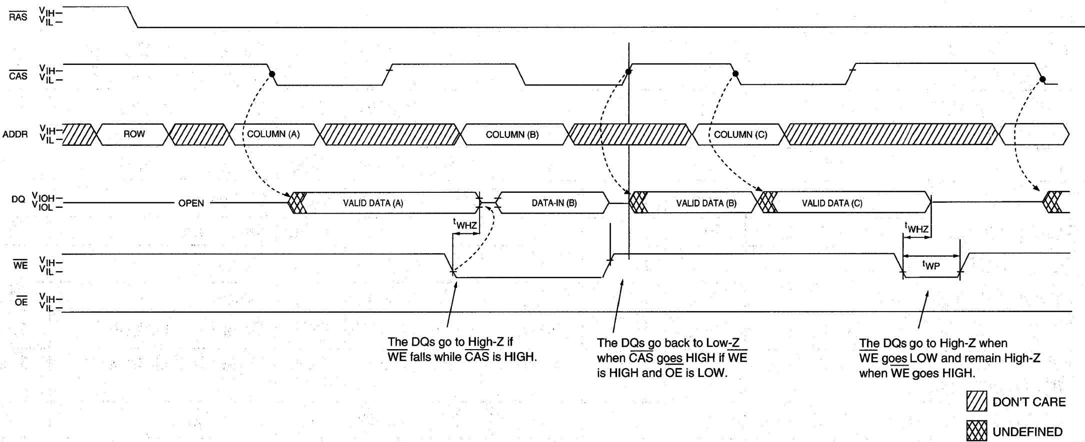

Figure 3
OUTPUT ENABLE AND DISABLE WITH $\overline{WE}$

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TRUTH TABLE: MT4C16270

FUNCTION		$\overline{RAS}$	$\overline{CASL}$	$\overline{CASH}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
EDO-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
EDO-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
$\overline{RAS}$ ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
3. EARLY WRITE only.
4. At least one of the two $\overline{CAS}$ signals must be active ($\overline{CASL}$ or $\overline{CASH}$).

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)**

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc**	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2.5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2.1mA)	VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6**	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	ICC2	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	195	175	160	mA	3, 4, 40
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN]; tCP, tASC = 10ns)	ICC4	130	125	120	mA	3, 4, 40
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS=VIH: tRC = tRC [MIN])	ICC5	195	175	160	mA	3
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC6	180	160	140	mA	3, 5

**60ns specifications are limited to a Vcc range of ±5%.

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CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CASL}$, $\overline{CASH}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)*

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
READ WRITE cycle time	^{t}RWC	140		157		187		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^{t}PC	25		30		33		ns	33
EDO-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	72		79		84		ns	33
Access time from $\overline{RAS}$	^{t}RAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^{t}CAC		15		20		20	ns	15, 31
Output Enable time	^{t}OE		15		20		20	ns	23, 31
Access time from column-address	^{t}AA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40		45	ns	31
$\overline{RAS}$ pulse width	^{t}RAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^{t}RSH	10		15		15		ns	38
$\overline{RAS}$ precharge time	^{t}RP	35		40		60		ns	
$\overline{CAS}$ pulse width	^{t}CAS	10	100,000	12	100,000	12	100,000	ns	37
$\overline{CAS}$ hold time	^{t}CSH	40		40		60		ns	30
$\overline{CAS}$ precharge time	^{t}CPN	10		10		10		ns	16, 34
$\overline{CAS}$ precharge time (EDO PAGE MODE)	^{t}CP	10		10		10		ns	34
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	45	20	50	20	60	ns	17, 29
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	5		5		5		ns	30
Row-address setup time	^{t}ASR	0		0		0		ns	
Row-address hold time	^{t}RAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	30	15	35	15	40	ns	18
Column-address setup time	^{t}ASC	0		0		0		ns	29
Column-address hold time	^{t}CAH	10		12		15		ns	29
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	40		40		55		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	22		27		30		ns	
Read command setup time	^{t}RCS	0		0		0		ns	26, 29
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		0		ns	19, 26, 30
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		0		ns	19

*60ns specifications are limited to a V_{CC} range of ±5%.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)*

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
CAS to output in Low-Z	^{t}CLZ	3		3		3		ns	31, 41
Output buffer turn-off delay from CAS or RAS	^{t}OFF	3	15	3	15	3	15	ns	20, 28, 31, 41
Output disable time	^{t}OD	3	15	3	15	3	15	ns	28, 39, 41
Write command setup time	^{t}WCS	0		0		0		ns	21, 26, 29
Write command hold time	^{t}WCH	10		10		10		ns	26, 38
Write command hold time (referenced to RAS)	^{t}WCR	40		40		60		ns	26
Write command pulse width	^{t}WP	10		10		10		ns	26
Write command to RAS lead time	^{t}RWL	10		12		12		ns	26
Write command to CAS lead time	^{t}CWL	10		12		12		ns	26, 30
Data-in setup time	^{t}DS	0		0		0		ns	22, 31
Data-in hold time	^{t}DH	10		15		15		ns	22, 31
Data-in hold time (referenced to RAS)	^{t}DHR	40		40		60		ns	
RAS to WE delay time	^{t}RWD	85		95		105		ns	21
Column-address to WE delay time	^{t}AWD	55		60		65		ns	21
CAS to WE delay time	^{t}CWD	40		45		45		ns	21, 29
Transition time (rise or fall)	^{t}T	2.5	50	2.5	50	2.5	50	ns	9, 10
Refresh period (512 cycles)	^{t}REF		8		8		8	ns	
RAS to CAS precharge time	^{t}RPC	10		10		10		ns	
CAS setup time (CBR REFRESH)	^{t}CSR	10		10		110		ns	5, 29
CAS hold time (CBR REFRESH)	^{t}CHR	10		10		10		ns	5, 30
OE hold time from WE during READ-MODIFY-WRITE cycle	^{t}OEH	15		20		20		ns	27
OE LOW to CAS HIGH setup time	^{t}OES	5		5		5		ns	
OE HIGH hold time from CAS HIGH	^{t}OEHC	10		10		10		ns	
OE HIGH pulse width	^{t}OEP	10		10		10		ns	
OE setup prior to RAS during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
Last CAS going LOW to first CAS returning HIGH	^{t}CLCH	10		10		10		ns	32
Data output hold after CAS LOW	^{t}COH	5		5		5		ns	
Output disable delay from WE	^{t}WHZ	3	15	3	15	3	15	ns	
Output enable delay from WE	^{t}WLZ	3		3		3		ns	

*60ns specifications are limited to a Vcc range of ±5%.

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 2.5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate and 50pF, V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW result in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met.
28. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur.
29. The first $\overline{CASx}$ edge to transition LOW.
30. The last $\overline{CASx}$ edge to transition HIGH.
31. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input, DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
32. Last falling $\overline{CASx}$ edge to first rising $\overline{CASx}$ edge.
33. Last rising $\overline{CASx}$ edge to next cycle's last rising $\overline{CASx}$ edge.
34. Last rising $\overline{CASx}$ edge to first falling $\overline{CASx}$ edge.
35. First DQs controlled by the first $\overline{CASx}$ to go LOW.
36. Last DQs controlled by the last $\overline{CASx}$ to go HIGH.
37. Each $\overline{CASx}$ must meet minimum pulse width.
38. Last $\overline{CASx}$ to go LOW.
39. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
40. Column-address changed once each cycle.
41. The 3ns minimum is a parameter guaranteed by design.

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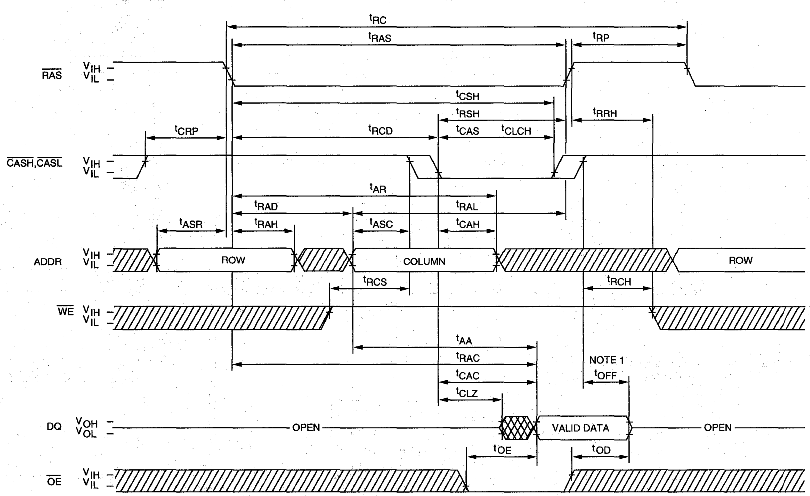
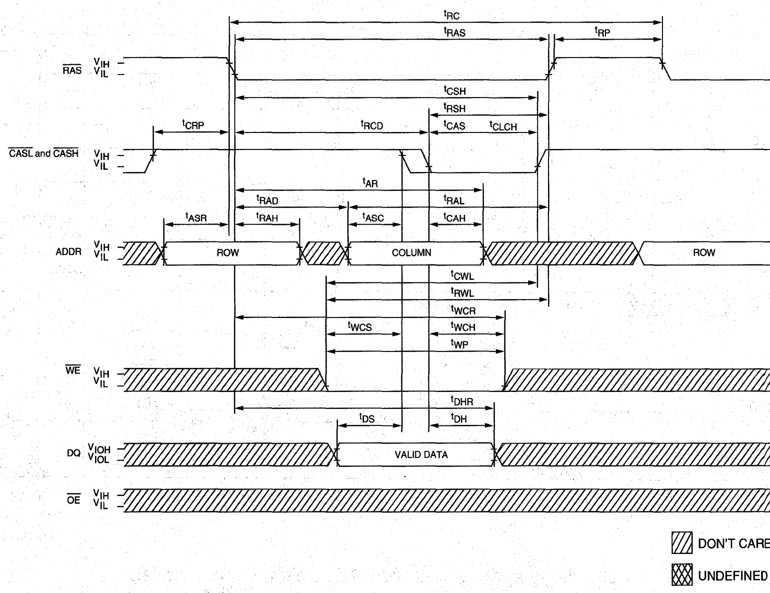
READ CYCLE



EARLY WRITE CYCLE



NOTE: 1. ᵗOFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

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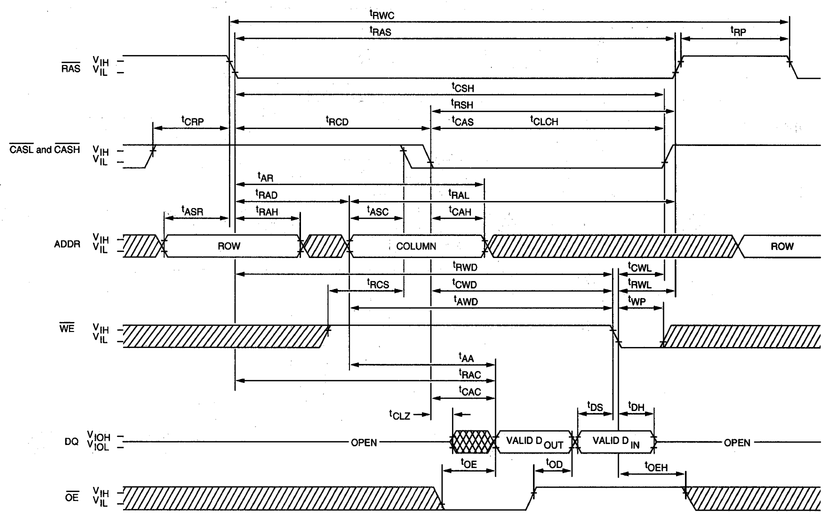
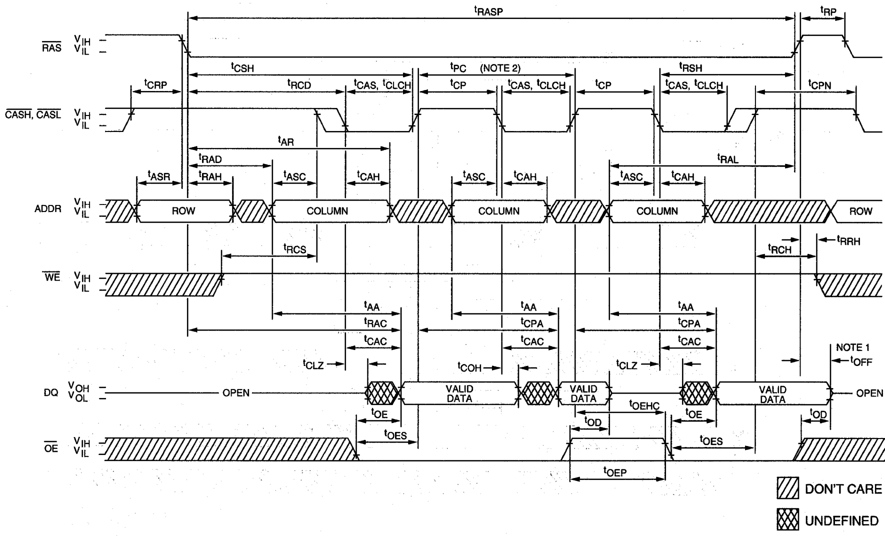
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



EDO-PAGE-MODE READ CYCLE



NOTE:
1. tOFF is referenced from the rising edge of RAS or CAS, whichever occurs last.
2. tPC can be measured from falling edge of CAS to falling edge of CAS, or from rising edge of CAS to rising edge of CAS. Both measurements must meet the tPC specification.

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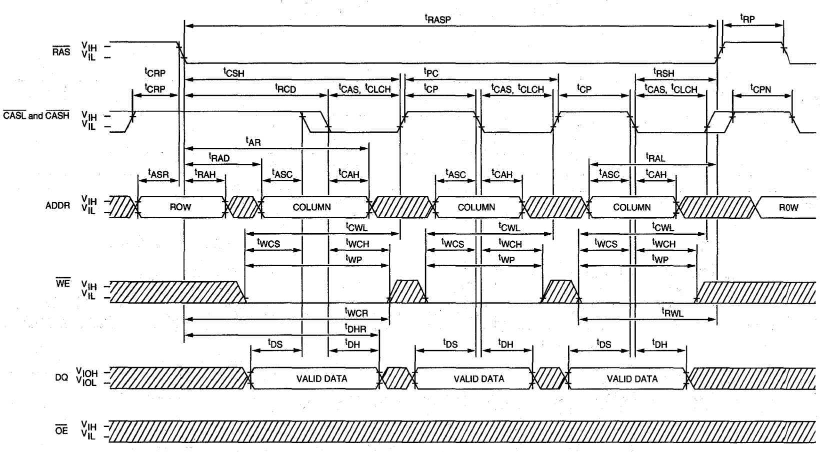
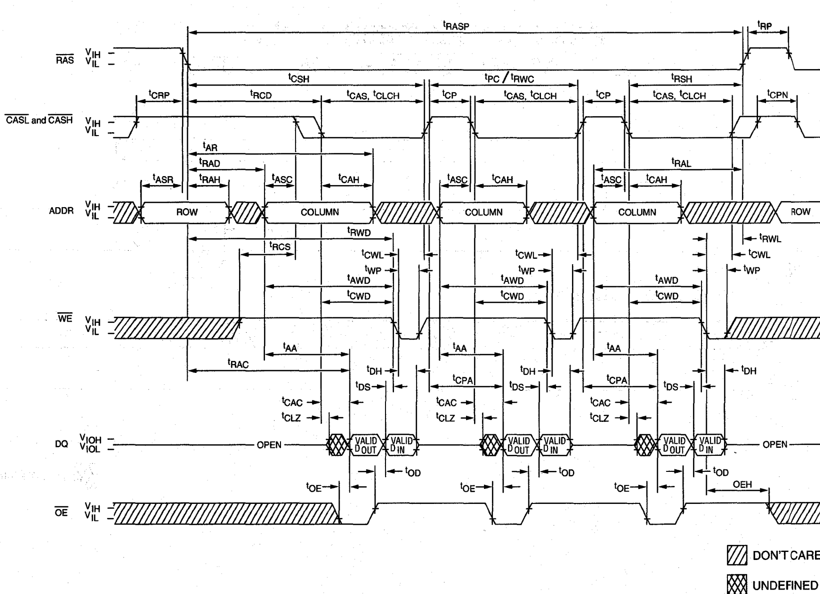
EDO-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. ^{t}PC can be measured from falling edge to falling edge of $\overline{CAS}$, or from rising edge to rising edge of $\overline{CAS}$. Both measurements must meet the ^{t}PC specification.

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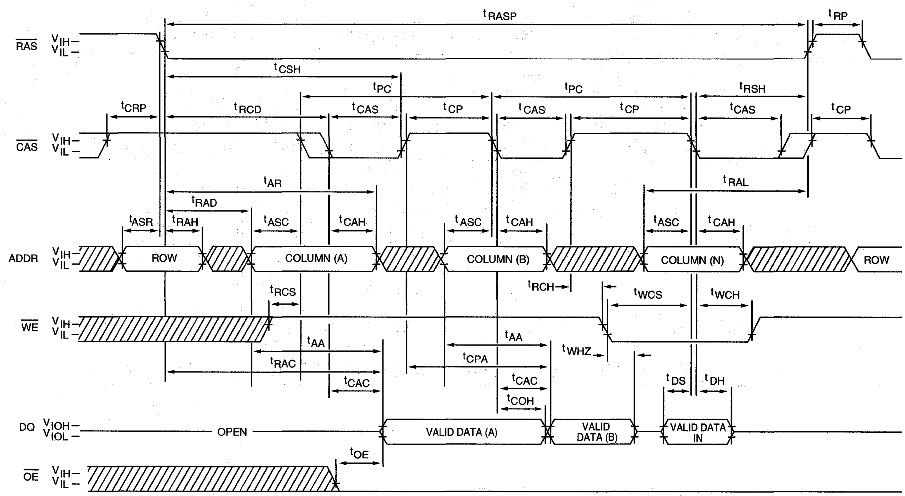
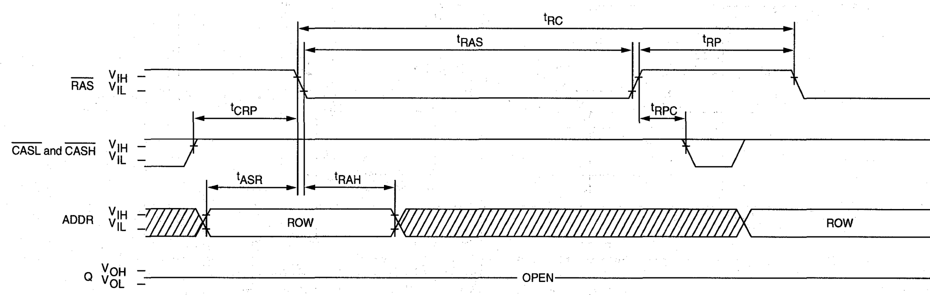
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Psuedo READ-MODIFY-WRITE)



RAS ONLY REFRESH CYCLE
(ADDR = A0-A8; OE, WE = DON'T CARE)



DON'T CARE

UNDEFINED

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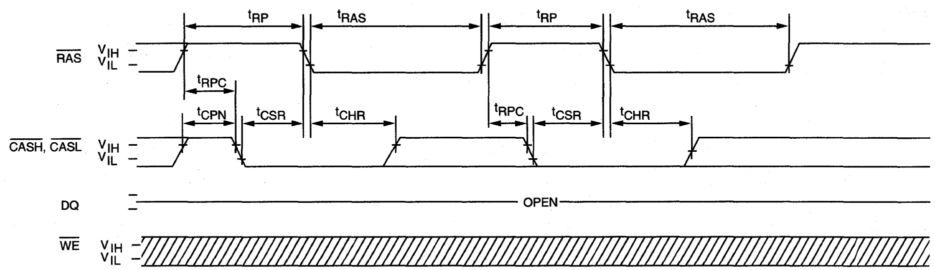
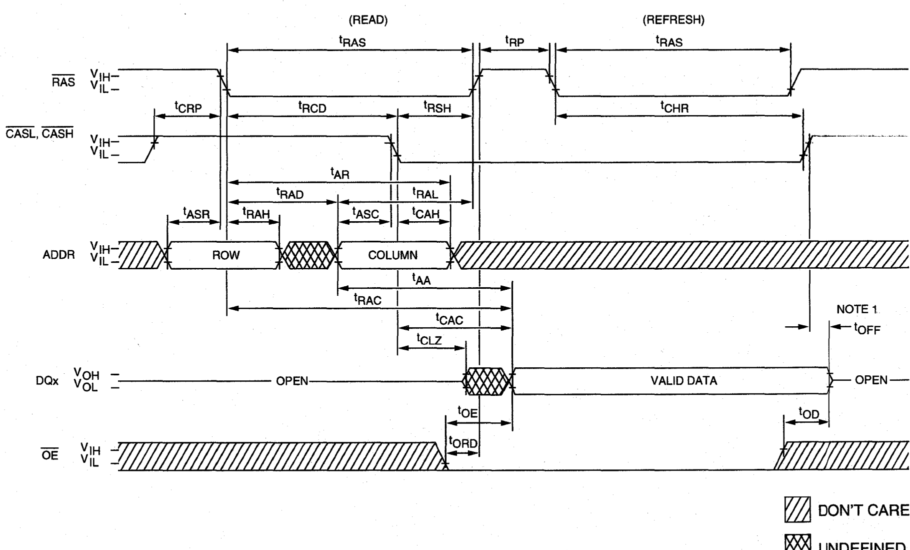
CBR REFRESH CYCLE
(A0-A8; $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



NOTE: 1. ^{t}OFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

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256K x 16 DRAM

3.3V EDO PAGE MODE

FEATURES

- Single +3.3V ±0.3V power supply*
- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Low power, 0.3mW standby; 165mW active, typical
- All device pins are TTL-compatible
- 512-cycle refresh in 8ms (nine rows and nine columns)
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- Extended data-out (EDO) PAGE MODE access cycle
- BYTE WRITE and BYTE READ access cycles

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6*
70ns access	-7
80ns access	-8
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

- Part Number Example: MT4LC16270DJ-7

* 60ns specifications are limited to a Vcc range of ±0.15V. Contact factory for availability of 60ns.

PIN ASSIGNMENT (Top View)

40-Pin SOJ (DC-6)

Signal	Pin	Pin	Signal
Vcc	1	40	Vss
DQ1	2	39	DQ16
DQ2	3	38	DQ15
DQ3	4	37	DQ14
DQ4	5	36	DQ13
Vcc	6	35	Vss
DQ5	7	34	DQ12
DQ6	8	33	DQ11
DQ7	9	32	DQ10
DQ8	10	31	DQ9
NC	11	30	NC
NC	12	29	$\overline{\text{CASL}}$
$\overline{\text{WE}}$	13	28	$\overline{\text{CASH}}$
$\overline{\text{RAS}}$	14	27	$\overline{\text{OE}}$
NC	15	26	A8
A0	16	25	A7
A1	17	24	A6
A2	18	23	A5
A3	19	22	A4
Vcc	20	21	Vss

40/44-Pin TSOP (DD-5)

Signal	Pin	Pin	Signal
Vcc	1	44	Vss
DQ1	2	43	DQ16
DQ2	3	42	DQ15
DQ3	4	41	DQ14
DQ4	5	40	DQ13
Vcc	6	39	Vss
DQ5	7	38	DQ12
DQ6	8	37	DQ11
DQ7	9	36	DQ10
DQ8	10	35	DQ9
NC	13	32	NC
NC	14	31	$\overline{\text{CASL}}$
$\overline{\text{WE}}$	15	30	$\overline{\text{CASH}}$
$\overline{\text{RAS}}$	16	29	$\overline{\text{OE}}$
NC	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
Vcc	22	23	Vss

GENERAL DESCRIPTION

The MT4LC16270 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x16 configuration. The MT4LC16270 has both BYTE WRITE and WORD WRITE access cycles via two $\overline{\text{CAS}}$ pins.

The MT4LC16270 offers an accelerated access cycle called EDO PAGE MODE.

The MT4LC16270 $\overline{\text{CAS}}$ function and timing are determined by the first $\overline{\text{CAS}}$ ($\overline{\text{CASL}}$ or $\overline{\text{CASH}}$) to transition LOW and by the last to transition back HIGH. $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ function in an identical manner to $\overline{\text{CAS}}$ in that either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ will generate an internal $\overline{\text{CAS}}$. Use of only one of the two results in a BYTE WRITE cycle. $\overline{\text{CASL}}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{\text{CASH}}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ in the same manner.

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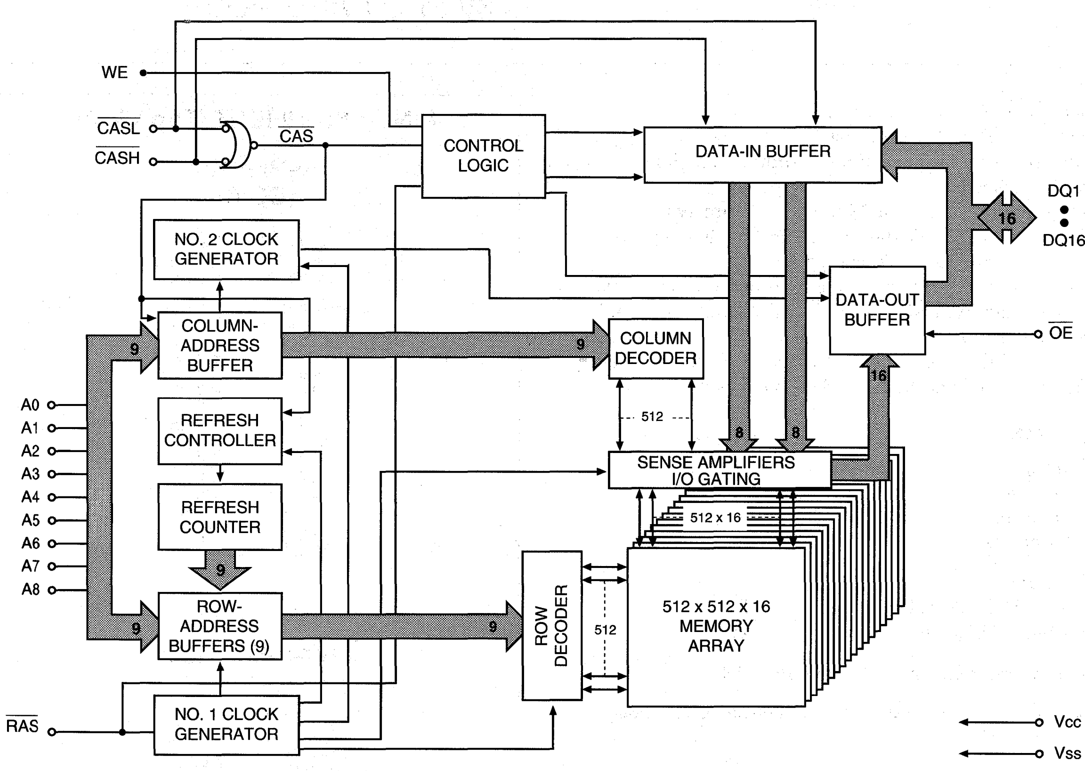
FUNCTIONAL BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered nine bits (A0-A8) at a time. RAS is used to latch the first nine bits and CAS the latter nine bits.

The CAS control also determines whether the cycle will be a refresh cycle (RAS ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS goes LOW. The MT4LC16270 has two CAS controls, CASL and CASH.

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input on the other 256K x 16 DRAMs. The key difference is that each CAS controls its corresponding DQ tristate logic (in conjunction with OE and WE and RAS). CASL controls DQ1 through DQ8 and CASH controls DQ9 through DQ16.

The MT4LC16270 CAS function is determined by the first CAS (CASL or CASH) transitioning LOW and the last transitioning back HIGH. The two CAS controls give the MT4LC16270 both BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High- Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by OE , WE and RAS.

EDO PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The EDO PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the EDO PAGE MODE operation.

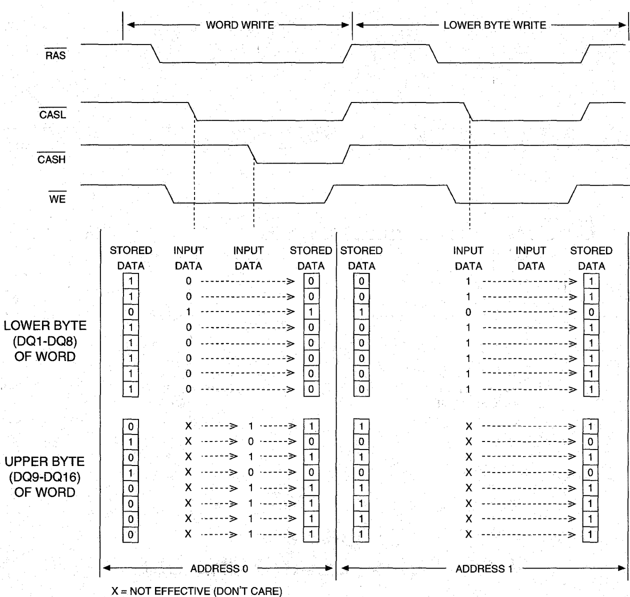

Figure1
16270 WORD AND BYTE WRITE EXAMPLE

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BYTE ACCESS CYCLE

The BYTE WRITE cycle is determined by the use of $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{CASL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling $\overline{CASH}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4LC16270 can be viewed as two 256K x 8 DRAMs which have common input controls. Figure 1 illustrates the MT4LC16270 BYTE WRITE and WORD WRITE cycles. The BYTE READ is accomplished in the same manner.

EDO

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. If $\overline{CAS}$ goes HIGH, and OE is LOW (active), the output buffers will be disabled. The MT4LC16270 offer an accelerated PAGE MODE cycle by eliminating output disable from $\overline{CAS}$ HIGH. This option is called EDO and it allows $\overline{CAS}$ precharge time (^tCP) to occur without the output data going invalid (see READ and EDO-PAGE-MODE READ waveforms).

Extended data-out operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after $\overline{CAS}$ goes HIGH, as long as $\overline{RAS}$ and $\overline{OE}$ are held LOW and $\overline{WE}$ is held HIGH. $\overline{OE}$ can be brought LOW or HIGH while $\overline{CAS}$ and $\overline{RAS}$ are LOW, and the DQs will transition between valid data and High-Z. Using $\overline{OE}$, there are two methods to disable the outputs and keep them disabled during the $\overline{CAS}$ HIGH time. The first method is to have $\overline{OE}$ HIGH when $\overline{CAS}$ transitions HIGH and keep $\overline{OE}$ HIGH for ^tOEHC. This will tristate the DQs and they will remain tristate, regardless of $\overline{OE}$, until $\overline{CAS}$ falls again. The second method is to have $\overline{OE}$ LOW when $\overline{CAS}$ transitions HIGH. Then $\overline{OE}$ can pulse HIGH for a minimum of ^tOEP anytime during the $\overline{CAS}$ HIGH period and the DQs will tristate and remain tristate, regardless of $\overline{OE}$, until $\overline{CAS}$ falls again (please reference Figure 2 for further detail on the

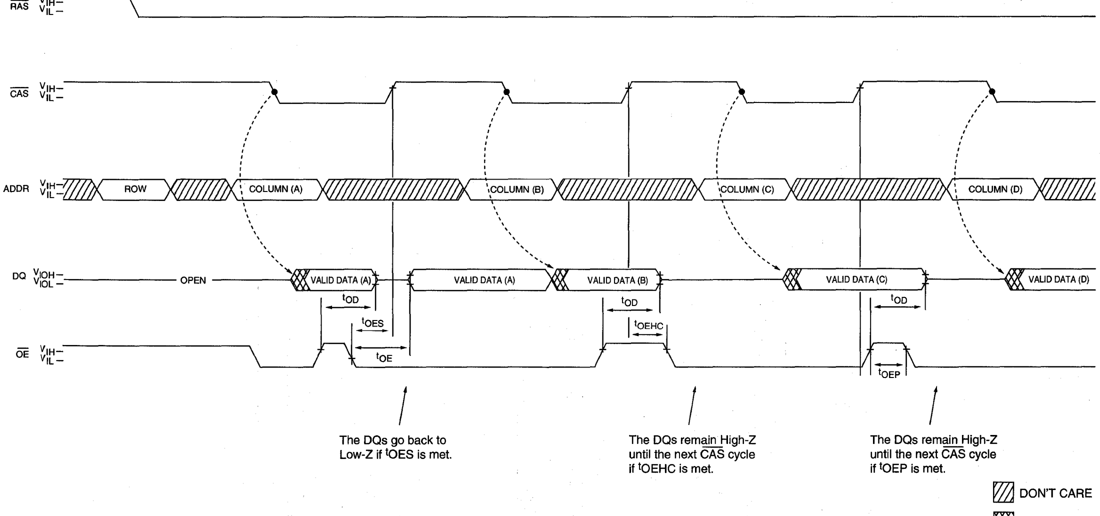

Figure 2
OUTPUT ENABLE AND DISABLE

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toggling $\overline{OE}$ condition). During other cycles, the outputs are disabled at ^tOFF time after $\overline{RAS}$ and $\overline{CAS}$ are HIGH or ^tWHZ after $\overline{WE}$ transitions LOW. The ^tOFF time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last. $\overline{WE}$ can also perform the function of turning off the output drivers under certain conditions, as shown in Fig. 3.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

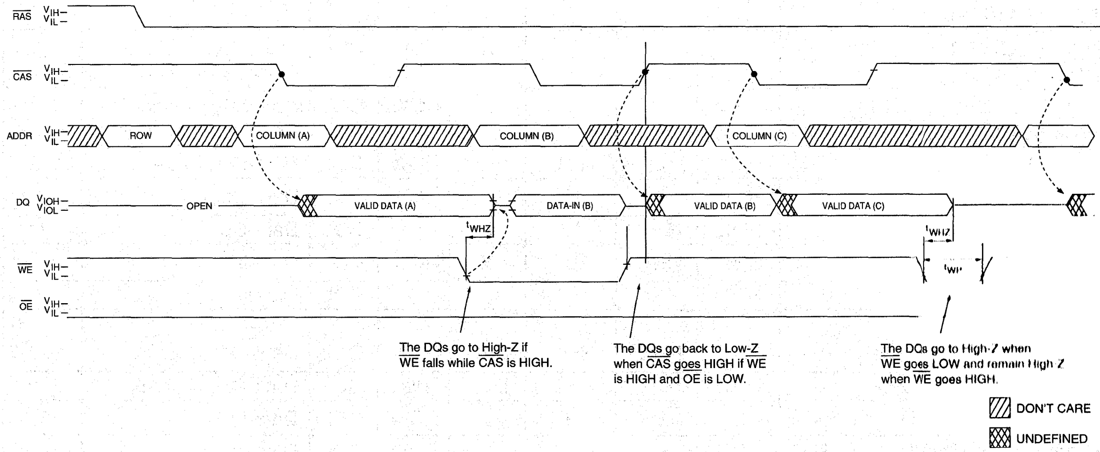

Figure 3
OUTPUT ENABLE AND DISABLE WITH $\overline{WE}$

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TRUTH TABLE: MT4LC16270

FUNCTION		$\overline{RAS}$	$\overline{CASL}$	$\overline{CASH}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
EDO-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
EDO-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
$\overline{RAS}$ ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
3. EARLY WRITE only.
4. At least one of the two $\overline{CAS}$ signals must be active ($\overline{CASL}$ or $\overline{CASH}$).

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +3.3V ±0.3V)**

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc**	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ Vcc+.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)	VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6**	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	500	500	500	µA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	100	100	100	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	ICC3	120	110	100	mA	3, 4, 40
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	ICC4	70	60	50	mA	3, 4, 40
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=VIH: ^tRC = ^tRC [MIN])	ICC5	120	110	100	mA	3
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	ICC6	120	110	100	mA	3, 5

**60ns specifications are limited to a Vcc range of ±0.15V.

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CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CASL}$,$\overline{CASH}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +3.3V ±0.3V)*

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	105		116		146		ns	
READ WRITE cycle time	^{t}RWC	140		157		187		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^{t}PC	25		30		33		ns	33
EDO-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	72		79		84		ns	33
Access time from $\overline{RAS}$	^{t}RAC		60	70		80	ns	14	
Access time from $\overline{CAS}$	^{t}CAC		15		20		20	ns	15, 31
Output Enable time	^{t}OE		15		20		20	ns	23, 31
Access time from column-address	^{t}AA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40		45	ns	31
$\overline{RAS}$ pulse width	^{t}RAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^{t}RSH	10		15		15		ns	38
$\overline{RAS}$ precharge time	^{t}RP	35		40		60		ns	
$\overline{CAS}$ pulse width	^{t}CAS	10	100,000	12	100,000	12	100,000	ns	37
$\overline{CAS}$ hold time	^{t}CSH	40		40		60		ns	30
$\overline{CAS}$ precharge time	^{t}CPN	10		10		10		ns	16, 34
$\overline{CAS}$ precharge time (EDO PAGE MODE)	^{t}CP	10		10		10		ns	34
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	45	20	50	20	60	ns	17, 29
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	5		5		5		ns	30
Row-address setup time	^{t}ASR	0		0		0		ns	
Row-address hold time	^{t}RAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	30	15	35	15	40	ns	18
Column-address setup time	^{t}ASC	0		0		0		ns	29
Column-address hold time	^{t}CAH	10		12		15		ns	29
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	40		40		55		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	22		27		30		ns	
Read command setup time	^{t}RCS	0		0		0		ns	26, 29
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		0		ns	19, 26, 30
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		0		ns	19

*60ns specifications are limited to a V_{CC} range of ±0.15V.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)*

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	31, 41
Output buffer turn-off delay from $\overline{CAS}$ or $\overline{RAS}$	^tOFF	3	15	3	15	3	15	ns	20, 28, 31, 41
Output disable time	^tOD	3	15	3	15	3	15	ns	28, 39, 41
Write command setup time	^tWCS	0		0		0		ns	21, 26, 29
Write command hold time	^tWCH	10		10		10		ns	26, 38
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	40		40		60		ns	26
Write command pulse width	^tWP	10		10		10		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	10		12		12		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	10		12		12		ns	26, 30
Data-in setup time	^tDS	0		0		0		ns	22, 31
Data-in hold time	^tDH	10		15		15		ns	22, 31
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	40		40		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21, 29
Transition time (rise or fall)	^tT	2.5	50	2.5	50	2.5	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		110		ns	5, 29
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5, 30
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	27
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	^tOES	5		5		5		ns	
$\overline{OE}$ HIGH hold time from $\overline{CAS}$ HIGH	^tOEHC	10		10		10		ns	
$\overline{OE}$ HIGH pulse width	^tOEP	10		10		10		ns	
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ returning HIGH	^tCLCH	10		10		10		ns	32
Data output hold after $\overline{CAS}$ LOW	^tCOH	5		5		5		ns	
Output disable delay from $\overline{WE}$	^tWHZ	3	15	3	15	3	15	ns	
Output enable delay from $\overline{WE}$	^tWLZ	3		3		3		ns	

*60ns specifications are limited to a Vcc range of ±0.15V.

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +3.3V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 2.5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If CAS and RAS = VIH, data output is High-Z.
12. If CAS = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate and 50pF, VOL = 0.8V and VOH = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS and RAS must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until CAS and RAS or OE go back to VIH) is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW result in a LATE WRITE (OE-controlled) cycle.
22. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if OE is LOW then taken HIGH before CAS goes HIGH, Q goes open. If OE is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as WE going LOW.
27. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if CAS remains LOW and OE is taken back LOW after ^{t}OEH is met.
28. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur.
29. The first CASx edge to transition LOW.
30. The last CASx edge to transition HIGH.
31. Output parameter (DQx) is referenced to corresponding CAS input, DQ1-DQ8 by CASL and DQ9-DQ16 by CASH.
32. Last falling CASx edge to first rising CASx edge.
33. Last rising CASx edge to next cycle's last rising CASx edge.
34. Last rising CASx edge to first falling CASx edge.
35. First DQs controlled by the first CASx to go LOW.
36. Last DQs controlled by the last CASx to go HIGH.
37. Each CASx must meet minimum pulse width.
38. Last CASx to go LOW.
39. All DQs controlled, regardless CASL and CASH.
40. Column-address changed once each cycle.
41. The 3ns minimum is a parameter guaranteed by design.

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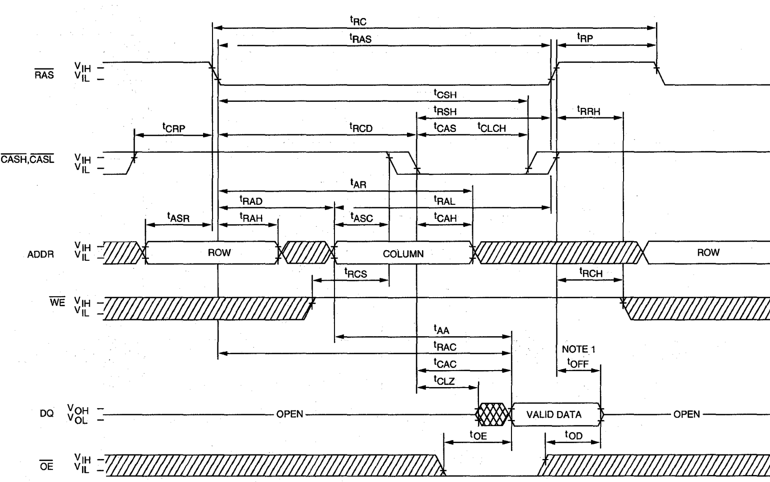
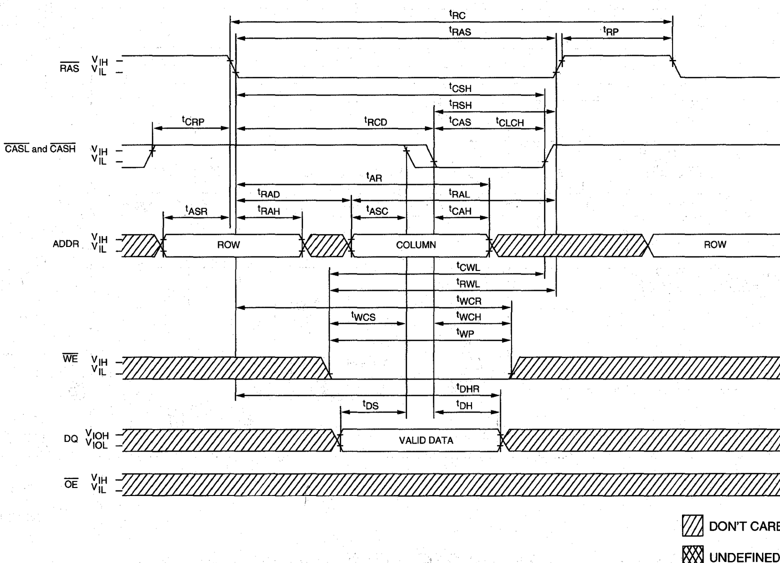
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

NOTE: 1. ^{t}OFF is referenced from the rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.

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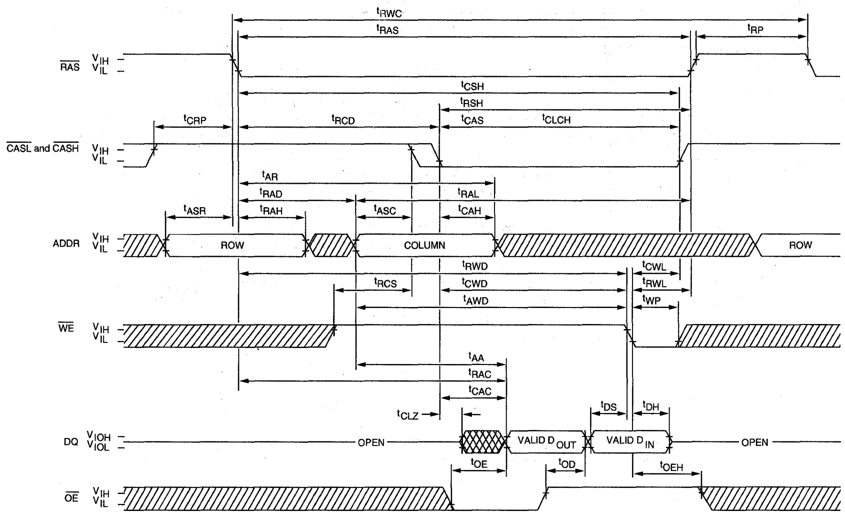
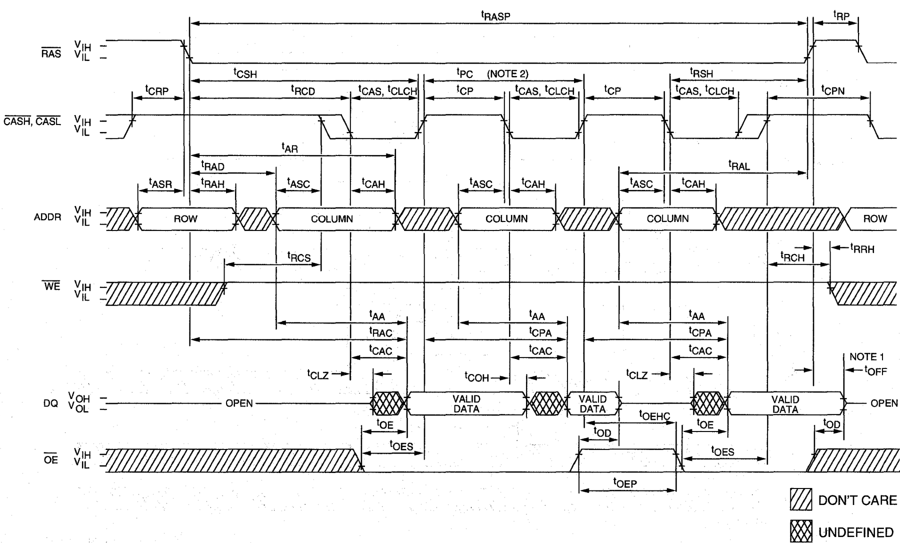
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



EDO-PAGE-MODE READ CYCLE



NOTE:
1. tOFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.
2. tPC can be measured from falling edge to falling edge of $\overline{CAS}$, or from rising edge to rising edge of $\overline{CAS}$. Both measurements must meet the tPC specification.

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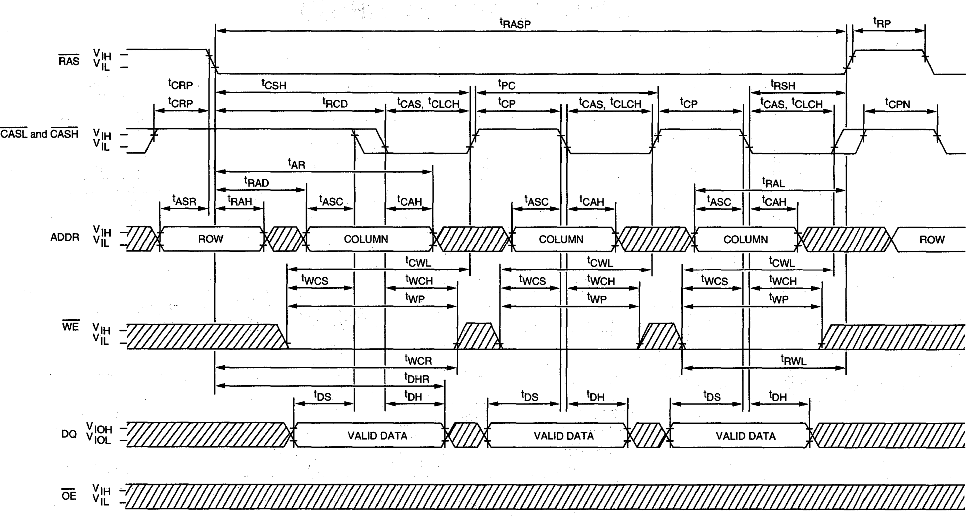
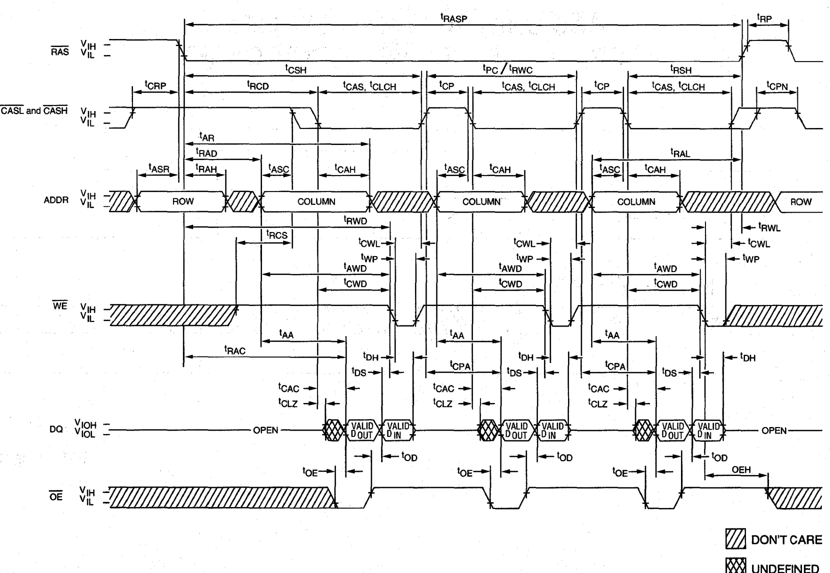
EDO-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. tPC can be measured from falling edge to falling edge of $\overline{CAS}$, or from rising edge to rising edge of $\overline{CAS}$. Both measurements must meet the tPC specification.

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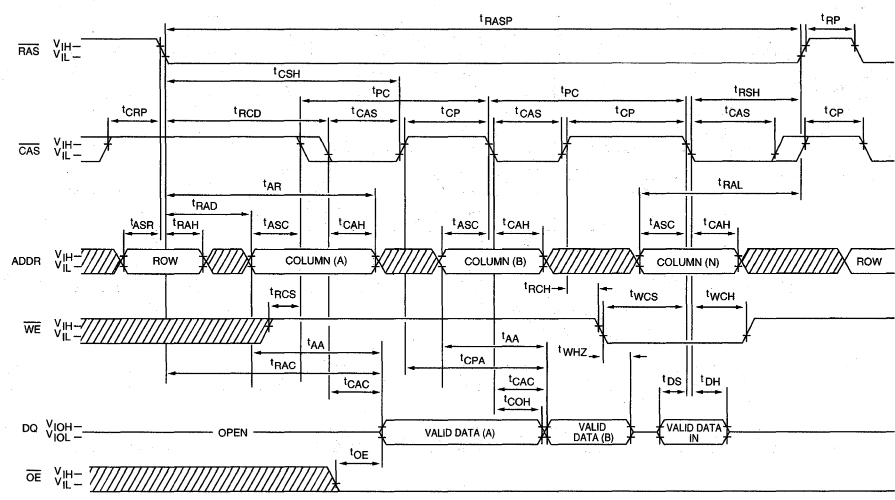
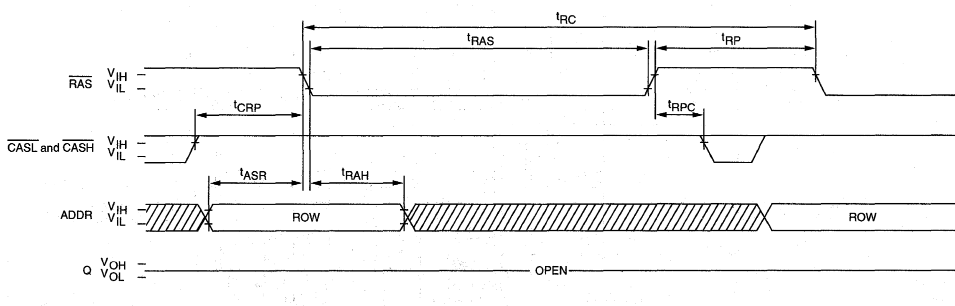
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



RAS ONLY REFRESH CYCLE
(ADDR = A0-A8, OE; WE = DON'T CARE)



DON'T CARE

UNDEFINED

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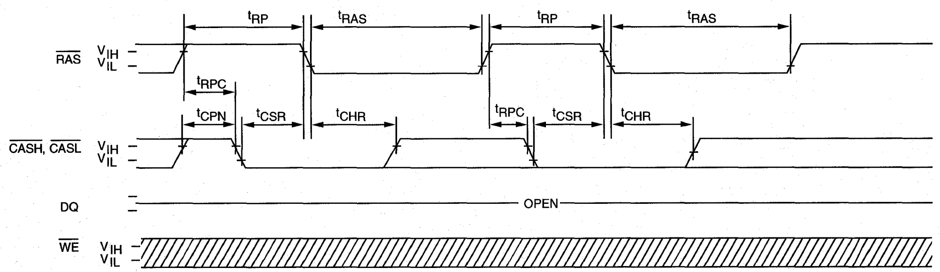
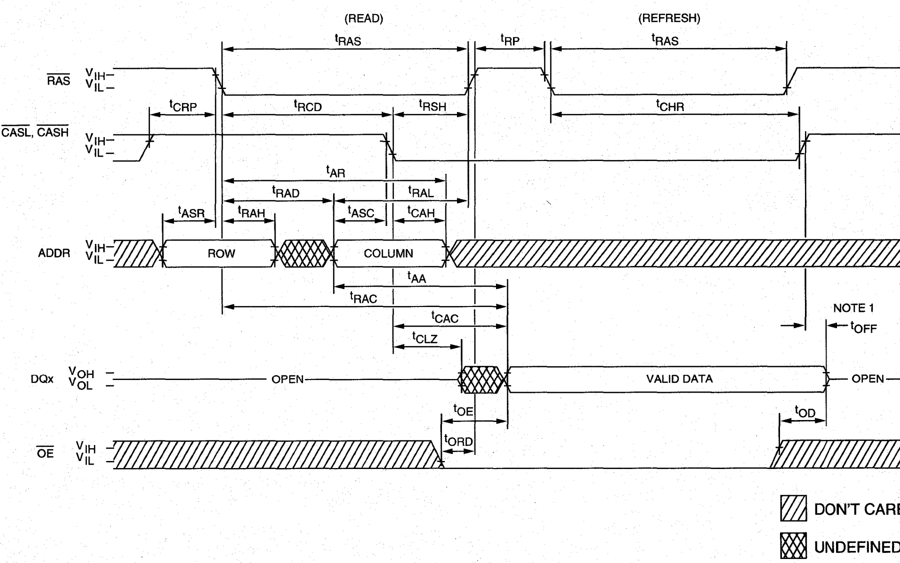
CBR REFRESH CYCLE
(A0-A8; $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



NOTE: 1. ^tOFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

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DRAM

256K x 16 DRAM

ASYMMETRICAL, FAST PAGE MODE

FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- Address entry: ten row-addresses, eight column-addresses
- High-performance CMOS silicon-gate process
- Single +5V±10% power supply*
- Low power, 3mW standby; 375mW active, typical
- All device pins are TTL-compatible
- 1,024-cycle refresh in 16ms
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- FAST PAGE MODE access cycle
- BYTE WRITE access cycle

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6*
70ns access	-7
80ns access	-8
• Packages	
Plastic SOJ (400mil)	DJ

- Part Number Example: MT4C16260DJ-7

*60ns specifications are limited to a Vcc range of ±5%.

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(DC-6)

Signal	Pin	Pin	Signal
Vcc	1	40	Vss
DQ1	2	39	DQ16
DQ2	3	38	DQ15
DQ3	4	37	DQ14
DQ4	5	36	DQ13
Vcc	6	35	VSS
DQ5	7	34	DQ12
DQ6	8	33	DQ11
DQ7	9	32	DQ10
DQ8	10	31	DQ9
NC	11	30	NC
$\overline{\text{WEL}}$	12	29	NC
$\overline{\text{WEH}}$	13	28	$\overline{\text{CAS}}$
$\overline{\text{RAS}}$	14	27	$\overline{\text{OE}}$
A9	15	26	A8
A0	16	25	A7
A1	17	24	A6
A2	18	23	A5
A3	19	22	A4
Vcc	20	21	Vss

GENERAL DESCRIPTION

The MT4C16260 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x16 configuration. Each word or byte is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) first, 8 bits second (A0-A7). $\overline{\text{RAS}}$ is used to latch the first 10 bits and $\overline{\text{CAS}}$ the latter 8 bits.

The MT4C16260 has both BYTE WRITE and WORD WRITE access cycles via two write enable pins.

The MT4C16260 functions in the same manner in that $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ control the selection of BYTE WRITE access cycles. $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ function identically to $\overline{\text{WE}}$ in that either $\overline{\text{WEL}}$ or $\overline{\text{WEH}}$ will generate an internal $\overline{\text{WE}}$.

The $\overline{\text{WE}}$ function and timing are determined by the first $\overline{\text{WE}}$ ($\overline{\text{WEL}}$ or $\overline{\text{WEH}}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{\text{WEL}}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{\text{WEH}}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

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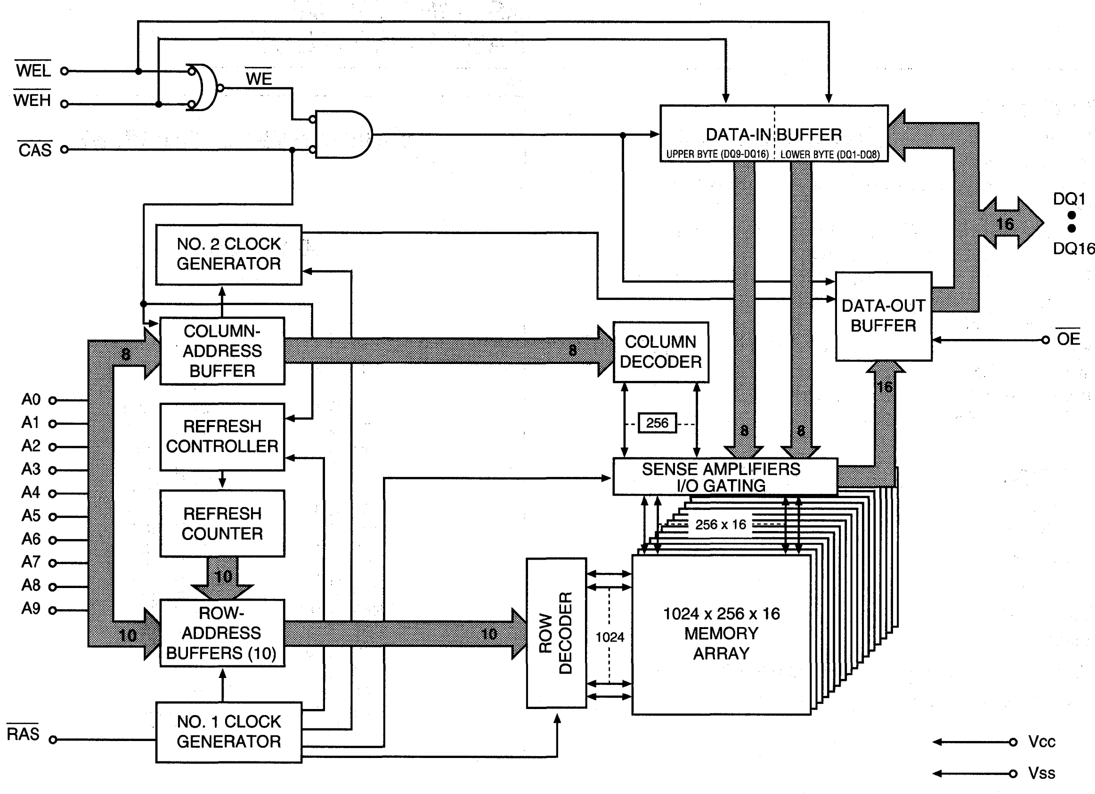
FUNCTIONAL BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. RAS is used to latch the first 10 bits (A0-A9) and CAS the latter 8 bits (A0-A7).

The CAS control also determines whether the cycle will be a refresh cycle (RAS ONLY) or an active cycle (READ, WRITE or READ-WRITE) once RAS goes LOW.

A READ or WRITE cycle is selected with either WEL or WEH performing the WE function. The WE function is determined by the first BYTE WRITE (WEL or WEH) to transition LOW and the last one to transition back HIGH.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High- Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O and pin direction is controlled by OE, WEL and WEH.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE)or RAS REFRESH cycle (RAS ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of WEL and WEH. Enabling WEL will select a lower byte WRITE cycle (DQ1-DQ8) while enabling WEH will select an upper byte WRITE cycle (DQ9-DQ16). Enabling both WEL and WEH selects a word WRITE cycle.

The MT4C16260 may be viewed as two 256K x 8 DRAMS that have common input controls, with the exception of the WE inputs. Figure 1 illustrates the MT4C16260 BYTE and WORD WRITE cycles.

DRAM

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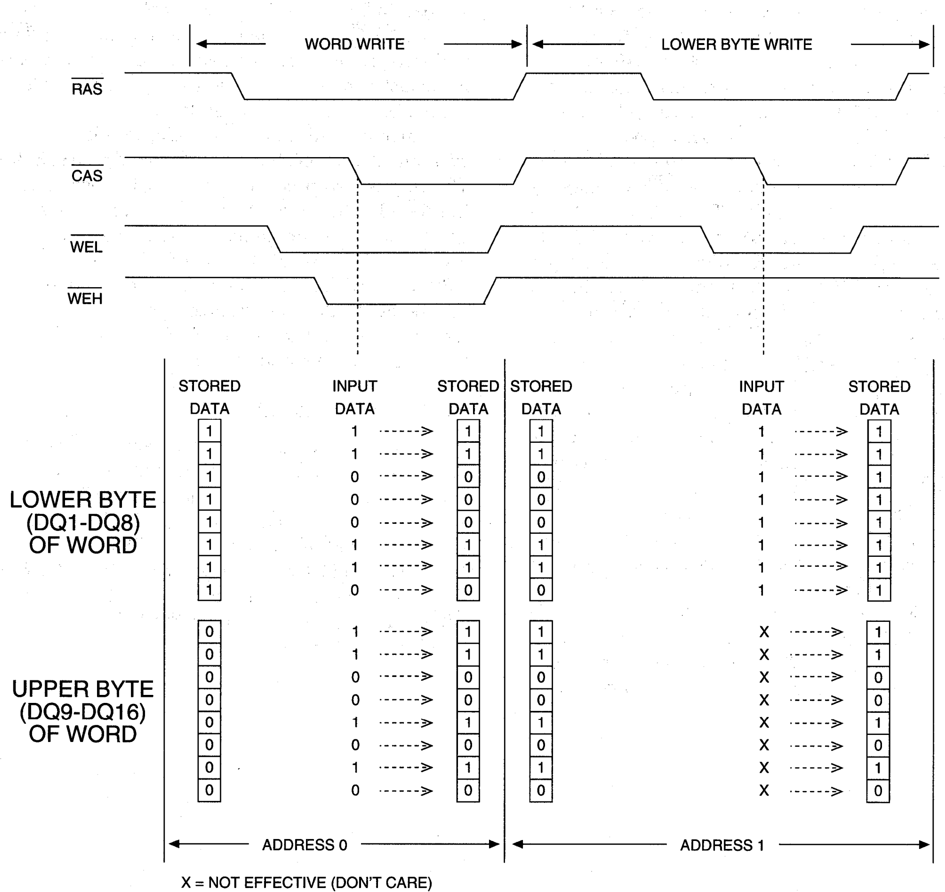

Figure 1
MT4C16260 WORD AND BYTE WRITE EXAMPLE

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DRAM

TRUTH TABLE: MT4C16260

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WEL}$	$\overline{WEH}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data-In	1
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 2
$\overline{RAS}$ ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either $\overline{WEL}$ or $\overline{WEH}$ active).
2. EARLY WRITE only.

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DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other coznditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Vcc = +5V ±10%**)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0 V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

(Notes: 1, 6, 7) (Vcc = +5V ± 10%**)

PARAMETER/CONDITION	SYMBOL	MAX -6**	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	Icc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	Icc2	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ᵗRC = ᵗRC [MIN])	Icc3	195	175	160	mA	3, 4, 29
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: ᵗPC = ᵗPC [MIN]; ᵗCP, ᵗASC = 10ns)	Icc4	120	110	100	mA	3, 4, 29
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=VIH: ᵗRC = ᵗRC [MIN])	Icc5	195	175	160	mA	3, 29
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ᵗRC = ᵗRC [MIN])	Icc6	180	160	140	mA	3, 5

**60ns specifications are limited to a Vcc range of ±5%.

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CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: RAS, CAS, WEL, WEH, OE	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%*)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ WRITE cycle time	tRWC	150		175		195		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	85		95		100		ns	
Access time from RAS	tRAC		60		70		80	ns	14
Access time from CAS	tCAC		15		20		20	ns	15
Output Enable time	tOE		15		20		20	ns	
Access time from column-address	tAA		30		35		40	ns	
Access time from CAS precharge	tCPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	tCPN	10		10		10		ns	16
CAS precharge time (PAGE MODE)	tCP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row-address setup time	tASR	0		0		0		ns	
Row-address hold time	tRAH	10		10		10		ns	
RAS to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		0		ns	
Column-address hold time	tCAH	10		15		15		ns	
Column-address hold time (referenced to RAS)	tAR	50		55		60		ns	
Column-address to RAS lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	26
Read command hold time (referenced to CAS)	tRCH	0		0		0		ns	19, 26
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	19
CAS to output in Low-Z	tCLZ	3		3		3		ns	30

*60ns specifications are limited to a Vcc range of ±5%.

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DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5+V ±10%*)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^tOFF	3	15	3	15	3	15	ns	20, 28, 30
Output disable time	^tOD	3	15	3	15	3	15	ns	28, 30
Write command setup time	^tWCS	0		0		0		ns	21, 26
Write command hold time	^tWCH	10		10		10		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	26
Write command pulse width	^tWP	10		10		10		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	27
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ returning HIGH	^tCLCH	10		10		10		ns	

*60ns specifications are limited to a Vcc range of ±5%.

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 5V ±10%; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or $\overline{CBR}$) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (max). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate. $\overline{WE}$ determines either EARLY WRITE (WCS), LATE WRITE (RWD, AWD and CWD) or an indeterminate (WCS or RWD, AWD and CWD not met) cycle when $\overline{WE}$ goes LOW in reference to $\overline{CAS}$ going LOW.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW.
27. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of OE. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
29. Column-address changed once each cycle.
30. The 3ns minimum is a parameter guaranteed by design.

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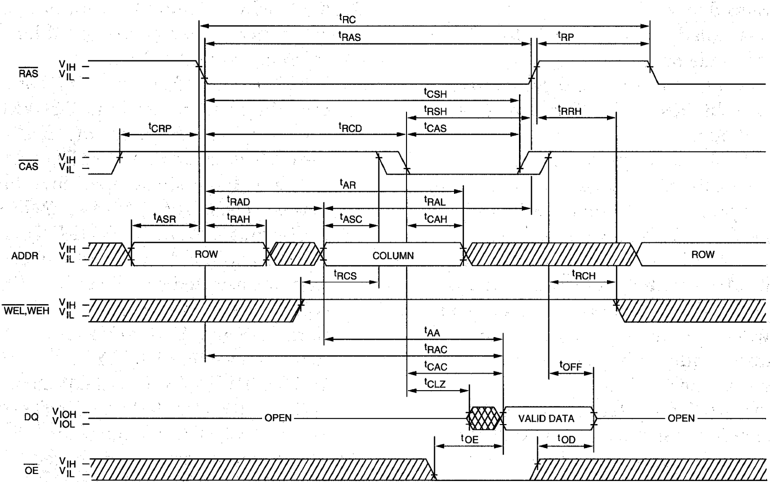
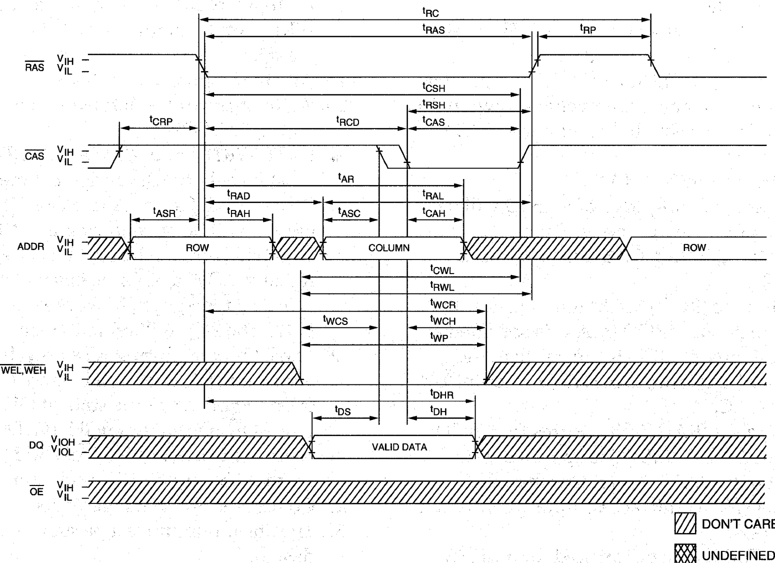
DRAM

READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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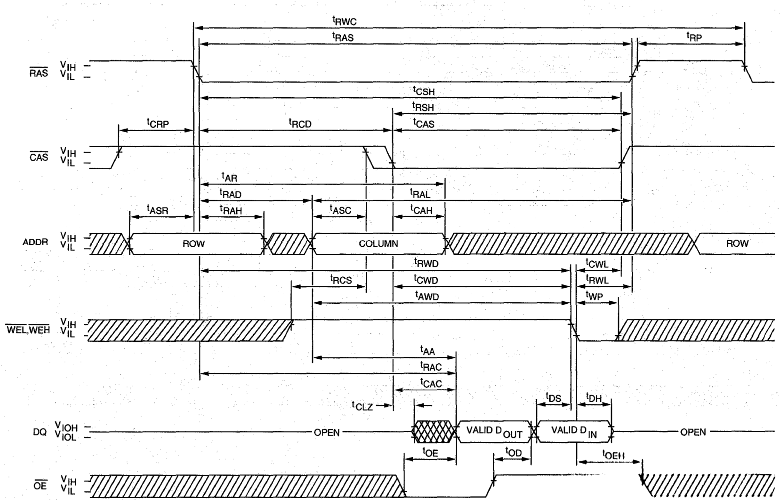
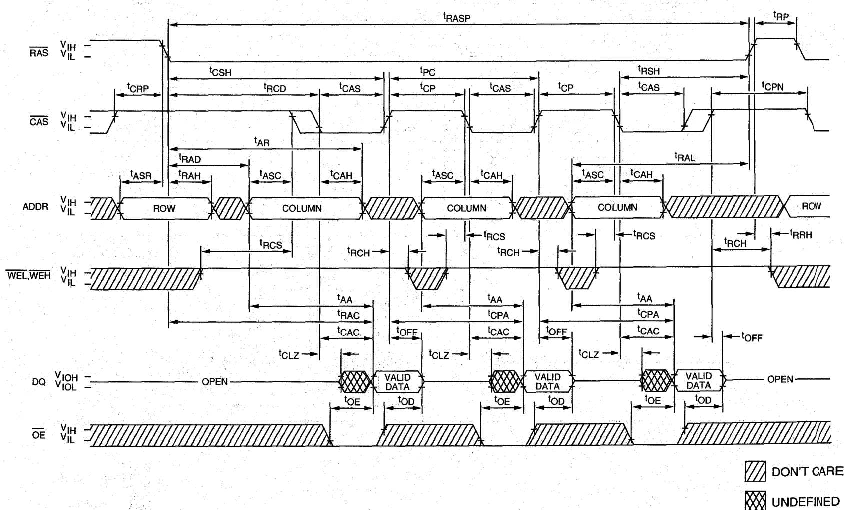
DRAM

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



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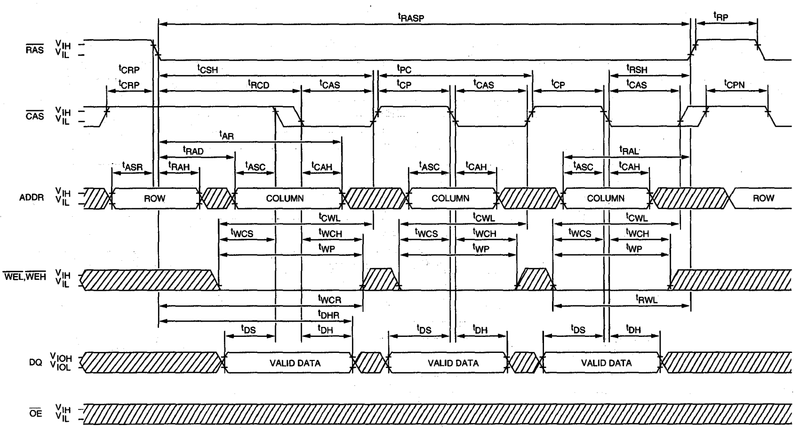
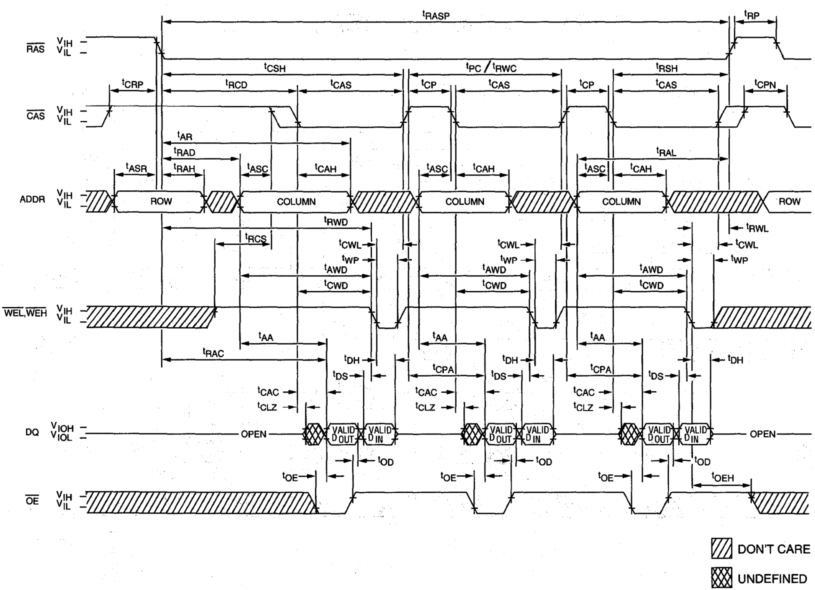
DRAM

FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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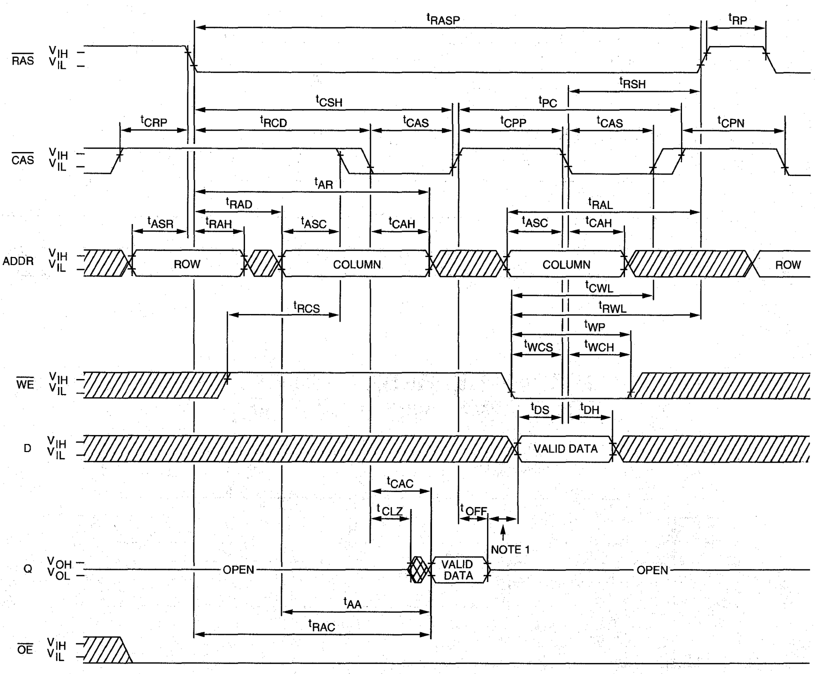
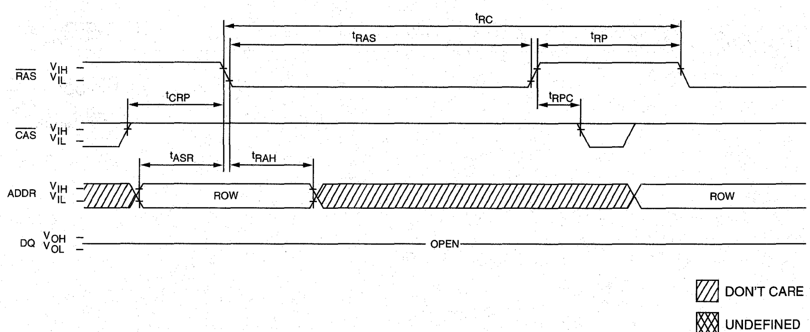
DRAM

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE



RAS ONLY REFRESH CYCLE
(ADDR = A0-A9,OE; WEL and WEH = DON'T CARE)



DON'T CARE

UNDEFINED

NOTE: 1. Do not drive data prior to High-Z; that is completion of tOFF. tCPP is equal to tOFF + tDS(MIN) + guardband between data-out and driving new data-in.

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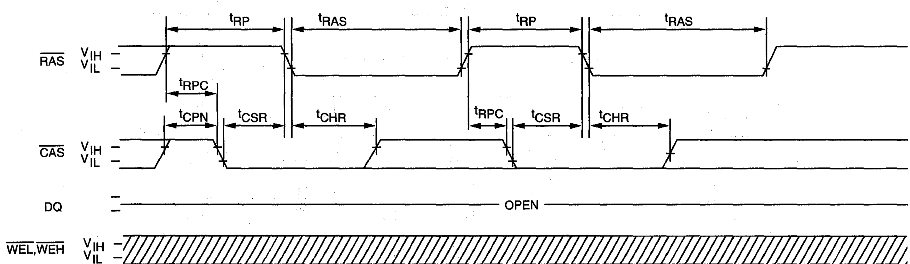
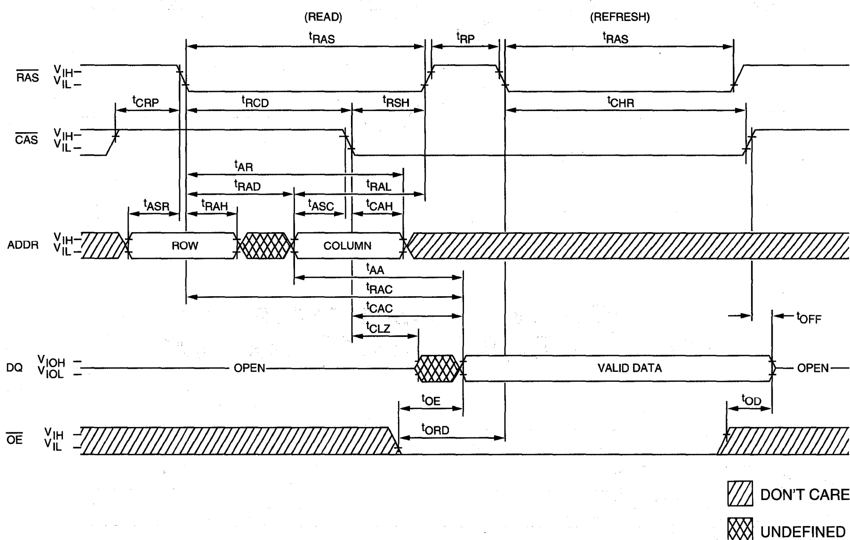
DRAM

CBR REFRESH CYCLE
(A0-A9 and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WEL}$, $\overline{WEH}$ = HIGH; $\overline{OE}$=LOW)



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DRAM

1 MEG x 16 DRAM

3.3V FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard x16 timing, functions, pinouts and packages
- High-performance CMOS silicon-gate process
- Single power supply: +3.3V ±0.3V
- All device pins are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and SELF
- BYTE WRITE and BYTE READ access cycles
- 1,024-cycle refresh (10 row-, 10 column-addresses)
- Low power, 3mW standby; 225mW active, typical
- Optional SELF REFRESH mode, with Extended Refresh rate (8X)

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Refresh Rate	
Standard and 16ms period	None
SELF REFRESH and 128ms period	S
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

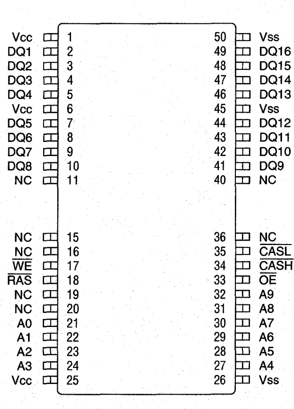
- Part Number Example: MT4LC1M16C3TG-7 S

PIN ASSIGNMENT (Top View)

42-Pin SOJ (DC-7)

Signal	Pin	Pin	Signal
Vcc	1	42	Vss
DQ1	2	41	DQ16
DQ2	3	40	DQ15
DQ3	4	39	DQ14
DQ4	5	38	DQ13
Vcc	6	37	Vss
DQ5	7	36	DQ12
DQ6	8	35	DQ11
DQ7	9	34	DQ10
DQ8	10	33	DQ9
NC	11	32	NC
NC	12	31	CASL
WE	13	30	CASH
RAS	14	29	OE
NC	15	28	A9
NC	16	27	A8
A0	17	26	A7
A1	18	25	A6
A2	19	24	A5
A3	20	23	A4
Vcc	21	22	Vss

44/50-Pin TSOP (DD-6)



GENERAL DESCRIPTION

The MT4LC1M163(S) is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x16 configuration. The MT4LC1M16C3 has both BYTE WRITE and WORD WRITE access cycles via two CAS pins (CASL and CASH). These function in an identical manner to a single CAS of other DRAMs in that either CASL or CASH will generate an internal CAS.

The MT4LC1M16C3 CAS function and timing are determined by the first CAS (CASL or CASH) to transition LOW and the last CAS to transition back HIGH. Use of only one of the two results in a BYTE access cycle. CASL transitioning LOW selects an access cycle for the lower byte (DQ1-DQ8) and CASH transitioning LOW selects an access cycle for the upper byte (DQ9-DQ16).

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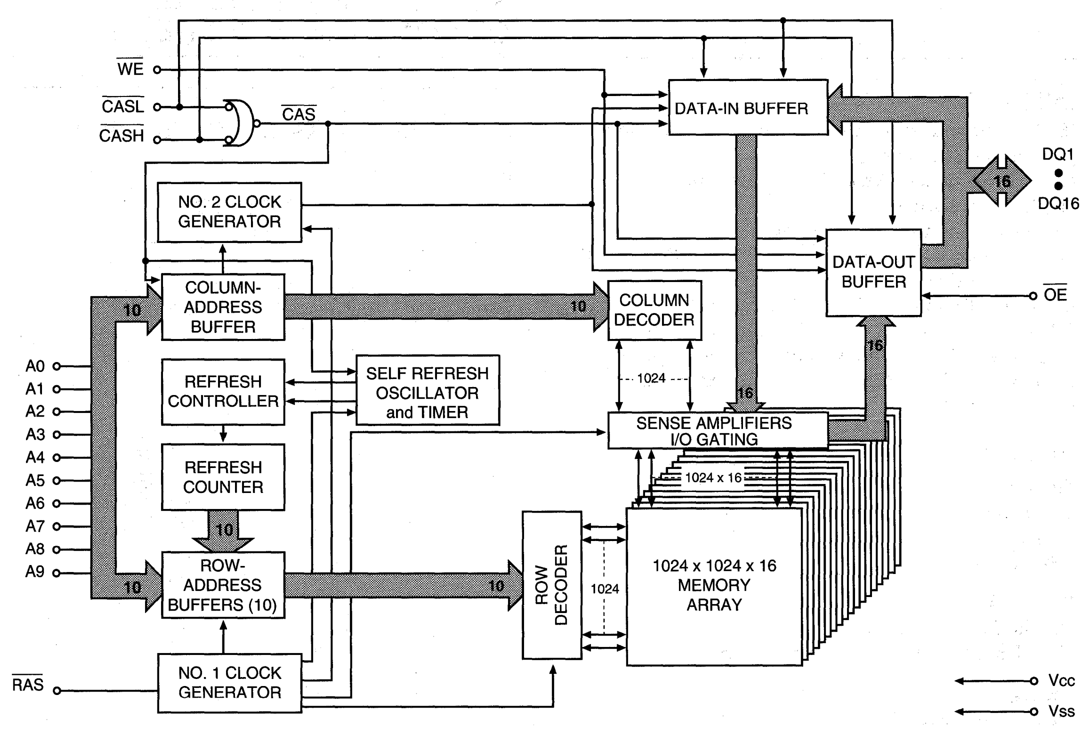
FUNCTIONAL BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered ten bits (A0-A9) at a time. RAS is used to latch the first ten bits and CAS the latter ten bits. The CAS function is determined by the first CAS (CASL or CASH) to transition LOW and the last one to transition back HIGH. The CAS function also determines whether the cycle will be a refresh cycle (RAS ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS goes LOW.

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input of other DRAMs. The key difference is each CAS input (CASL and CASH) controls its corresponding DQ tristate logic (in conjunction with OE and WE). CASL controls DQ1 through DQ8 and CASH controls DQ9 through DQ16. The two CAS controls give the MT4C1M16C3 both BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High- Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by OE and WE

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on S-version), regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BYTE ACCESS CYCLE

The BYTE WRITEs and BYTE READs are determined by the use of CASL and CASH. Enabling CASL will select a lower BYTE access (DQ1-DQ8). Enabling CASH will select an upper BYTE access (DQ9-DQ16). Enabling both CASL and CASH selects a WORD WRITE cycle.

The MT4C1M16C3 may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the CAS inputs. Figure 1 illustrates the BYTE WRITE and WORD WRITE cycles. Figure 2 illustrates BYTE READ and WORD READ cycles.

SELF REFRESH

SELF REFRESH is similar to CBR except that the DRAM provides its own internal clocking during SLEEP mode. Thus, an external clock is not required. This results in additional power savings and design ease. The DRAM's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding both RAS and CAS LOW for a specified period. The industry standard for this value is 100µs minimum (ᵗRASS). The DRAM will remain in the SELF REFRESH mode while RAS and CAS remain LOW. Once CAS has been held LOW for ᵗCHD, CAS is no longer required to remain LOW and becomes a "don't care." CAS is a "don't care" until ᵗCHS, at which time CAS must be either HIGH or LOW.

The SELF REFRESH mode is terminated by taking RAS HIGH for the time minimum of an operation cycle, ᵗRPS. Once the SELF REFRESH mode has been terminated, it is recommended that the user perform a refresh of all rows within the time of the external refresh rate prior to active use of the DRAM. The external refresh rate is typically 125µs per row-address. Once this burst has been completed, the DRAM may be used in the functional mode with distributed refreshes, such as CBR or RAS ONLY.

The alternative approach when exiting SELF REFRESH mode is to utilize distributed refreshes once ᵗRPS has been met, provided CBR REFRESH cycles are employed. The first CBR pulse should occur within the time of the external refresh rate prior to active use of the DRAM and must be executed within three external refresh rate periods. This will ensure maximum data integrity.

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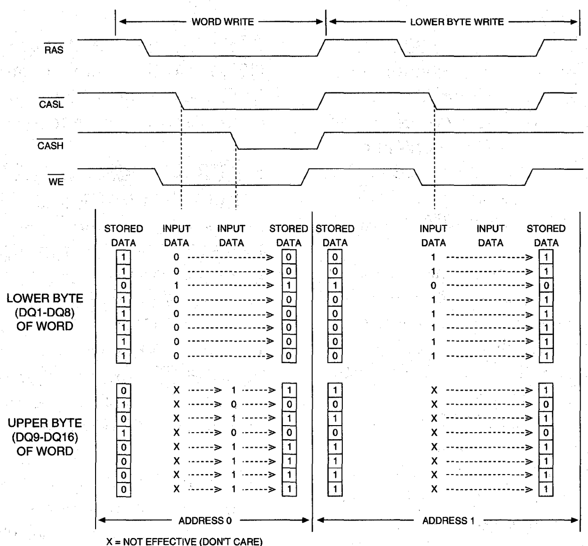

Figure 1
WORD AND BYTE WRITE EXAMPLE

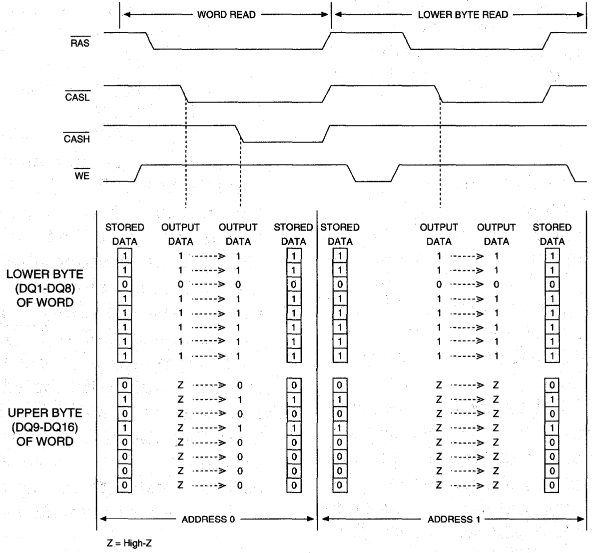

Figure 2
WORD AND BYTE READ EXAMPLE

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TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CASL}}$	$\overline{\text{CASH}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ADDRESSES ^{t}R	ADDRESSES ^{t}C	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
$\overline{\text{RAS}}$ ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	H	X	X	X	High-Z	4
SELF REFRESH		H→L	L	L	H	X	X	X	High-Z	

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ active).
3. EARLY WRITE only.
4. Only one $\overline{\text{CAS}}$ must be active ($\overline{\text{CASL}}$ or $\overline{\text{CASH}}$).

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS

(Notes: 1, 6, 7, 42) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 3.6V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2.0mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2.0mA)	VOL		0.4	V	

ELECTRICAL CHARACTERISTICS AND DC OPERATING SPECIFICATIONS

(Notes: 1, 6, 7, 42) (Vcc = +3.3V ±0.3V)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$ Address Cycling: tRC = tRC [MIN])	ICC3	150	140	130	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: tPC = tPC [MIN]; tCP, tASC = 10ns)	ICC4	80	70	60	mA	3, 4, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=VIH: tRC = tRC [MIN])	ICC5	150	140	130	mA	3
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$ Address Cycling: tRC = tRC [MIN])	ICC6	150	140	130	mA	3, 5
REFRESH CURRENT: Extended (S-only) Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = tRAS (MIN); $\overline{WE}$, A0-A9 and DIN = Vcc - 0.2V (DIN may be left open); tRC = 125µs (1,024 rows at 125µs = 128ms)	ICC7	150	150	150	µA	3, 5
REFRESH CURRENT: SELF (S-only) Average power supply current during SELF REFRESH: CBR cycle with $\overline{RAS}$ ≥ tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc - 0.2V; A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)	ICC8	150	150	150	µA	5, 27

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CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Addresses	C_{I1}	5	pF	2
Input Capacitance: RAS, CASL,CASH, WE, OE	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
READ WRITE cycle time	^{t}RWC	150		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		45		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	85		95		100		ns	35
Access time from RAS	^{t}RAC		60		70		80	ns	14
Access time from CAS	^{t}CAC		15		20		20	ns	15, 33
Output Enable	^{t}OE		15		15		15	ns	33
Access time from column-address	^{t}AA		30		35		40	ns	
Access time from CAS precharge	^{t}CPA		35		40		45	ns	33
RAS pulse width	^{t}RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^{t}RSH	15		20		20		ns	40
RAS precharge time	^{t}RP	40		50		60		ns	
CAS pulse width	^{t}CAS	15	100,000	20	100,000	20	100,000	ns	39
CAS hold time	^{t}CSH	60		70		80		ns	32
CAS precharge time	^{t}CPN	10		10		10		ns	16, 36
CAS precharge time (FAST PAGE MODE)	^{t}CP	10		10		10		ns	36
RAS to CAS delay time	^{t}RCD	20	45	20	50	20	60	ns	17, 31
CAS to RAS precharge time	^{t}CRP	5		5		5		ns	32
Row-address setup time	^{t}ASR	0		0		0		ns	
Row-address hold time	^{t}RAH	10		10		10		ns	
RAS to column-address delay time	^{t}RAD	15	30	15	35	15	40	ns	18
Column-address setup time	^{t}ASC	0		0		0		ns	31
Column-address hold time	^{t}CAH	10		15		15		ns	31
Column-address hold time (referenced to RAS)	^{t}AR	50		55		60		ns	
Column-address to RAS lead time	^{t}RAL	30		35		40		ns	
Read command setup time	^{t}RCS	0		0		0		ns	26, 31
Read command hold time (referenced to CAS)	^{t}RCH	0		0		0		ns	19, 26, 32
Read command hold time (referenced to RAS)	^{t}RRH	0		0		0		ns	19
CAS to output in Low-Z	^{t}CLZ	3		3		3		ns	33, 30

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^tOFF	3	15	3	20	3	20	ns	20, 30, 33
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 26, 31
Write command hold time	^tWCH	10		15		15		ns	26, 40
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	26
Write command pulse width	^tWP	10		15		15		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26, 32
Data-in setup time	^tDS	0		0		0		ns	22, 33
Data-in hold time	^tDH	10		15		15		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21, 31
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		16		16		16	ms	28
Refresh period - S option (1,024 cycles)	^tREF		128		128		128	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		5		ns	5, 31
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		15		ns	5, 32
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	26
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	26
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Output disable	^tOD	3	15	3	15	3	15	ns	29, 30, 41
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		15		15		ns	28
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^tCLCH	10		10		10		ns	34
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^tRASS	100		100		100		µs	27
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^tRPS	110		130		150		ns	27
$\overline{CAS}$ LOW to "don't care" during SELF REFRESH cycle	^tCHD	15		15		15		ns	

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +3.3V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the tREF refresh requirement is exceeded.
8. AC characteristics assume tT = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If CAS = VIH, data output is High-Z.
12. If CAS = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate, 50pF and VOL = 0.8V and VOH = 2.0V.
14. Assumes that tRCD < tRCD (MAX). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
15. Assumes that tRCD ≥ tRCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for tCPN.
17. Operation within the tRCD (MAX) limit ensures that tRAC (MAX) can be met. tRCD (MAX) is specified as a reference point only; if tRCD is greater than the specified tRCD (MAX) limit, access time is controlled exclusively by tCAC.
18. Operation within the tRAD limit ensures that tRCD (MAX) can be met. tRAD (MAX) is specified as a reference point only; if tRAD is greater than the specified tRAD (MAX) limit, access time is controlled exclusively by tAA.
19. Either tRCH or tRRH must be satisfied for a READ cycle.
20. tOFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL.
21. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tRWD ≥ tRWD (MIN), tAWD ≥ tAWD (MIN) and tCWD ≥ tCWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until CAS or OE goes back to VIH) is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE WRITE (OE-controlled) cycle.
22. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if OE is LOW then taken HIGH before CAS goes HIGH, Q goes open. If OE is tied permanently LOW, LATE WRITE and READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
25. All other inputs at 0.2V or Vcc -0.2V.
26. Column-address changed once each cycle.
27. When exiting the SELF REFRESH mode, a complete set of row refreshes should be executed in order to ensure that the DRAM will be fully refreshed. Alternatively, distributed refreshes may be utilized, provided CBR refreshes are employed.
28. LATE WRITE and READ-MODIFY-WRITE cycles must have both tOD and tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once tOD or tOFF occur. If CAS goes HIGH before OE, the DQs will open regardless of the state of OE. If CAS stays LOW while OE is brought HIGH, the DQs will open. If OE is brought back LOW (CAS still LOW), the DQs will provide the previously read data.

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NOTES (continued)

30. The 3ns minimum is a parameter guaranteed by design.
31. The first $\overline{CAS}$x edge to transition LOW.
32. The last $\overline{CAS}$x edge to transition HIGH.
33. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
34. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
35. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
36. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
37. First DQs controlled by the first $\overline{CAS}$x to go LOW.
38. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
39. Each $\overline{CAS}$x must meet minimum pulse width.
40. Last $\overline{CAS}$x to go LOW.
41. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.

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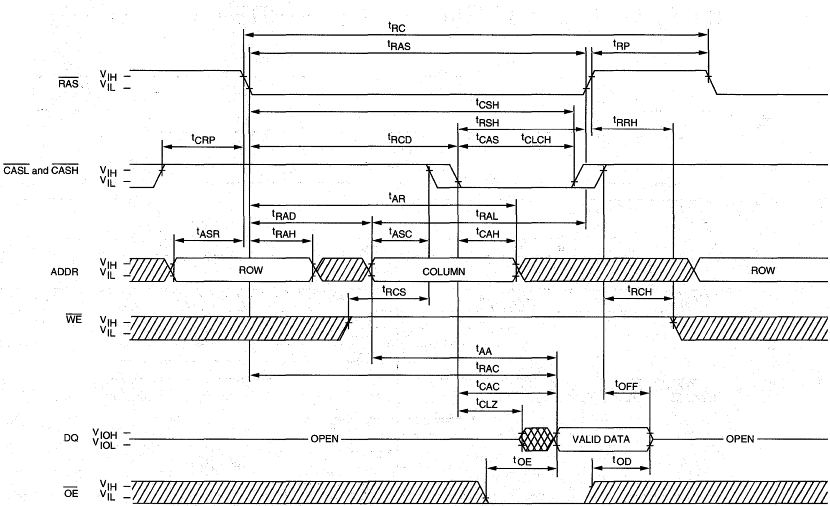
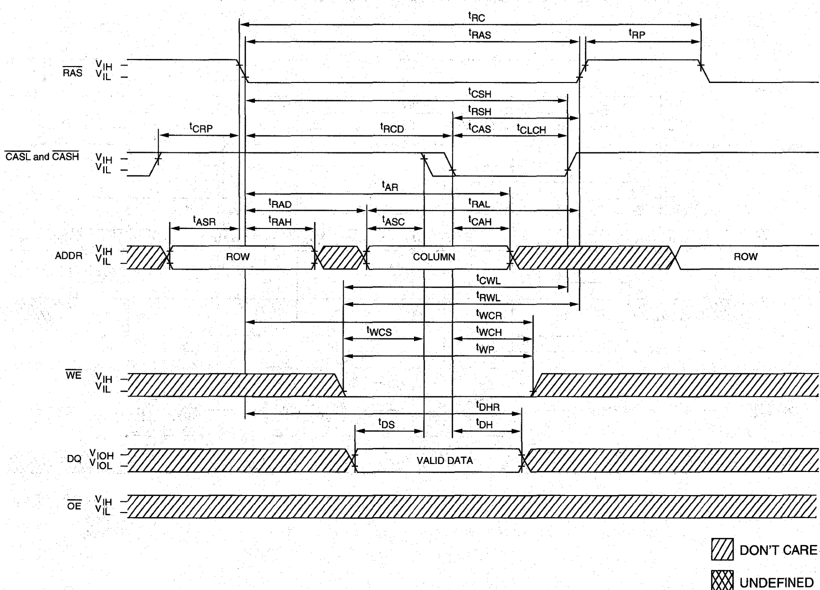
READ CYCLE



EARLY WRITE CYCLE



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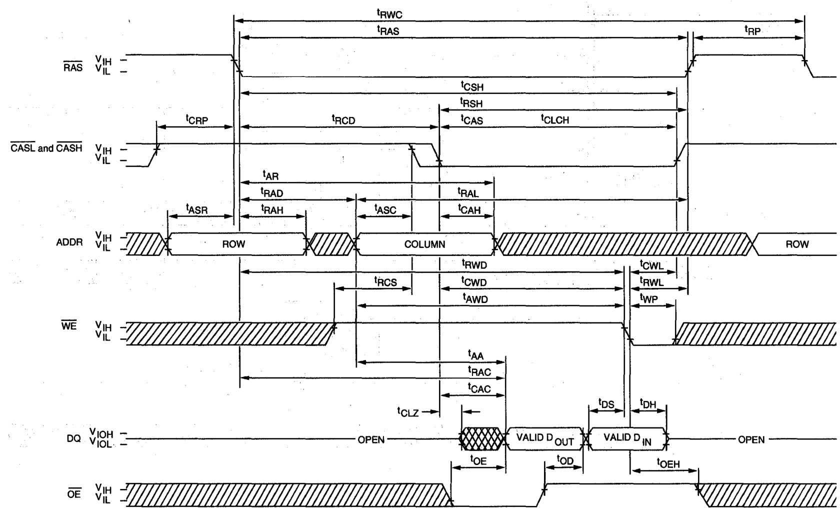
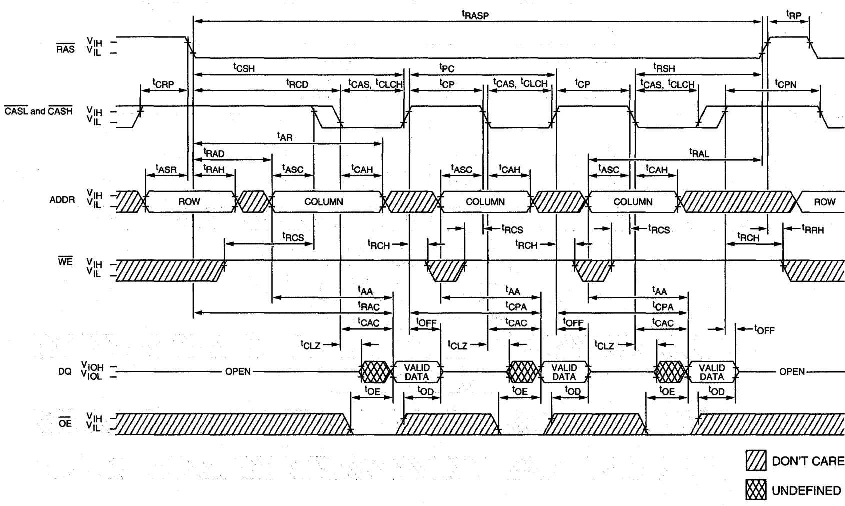
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



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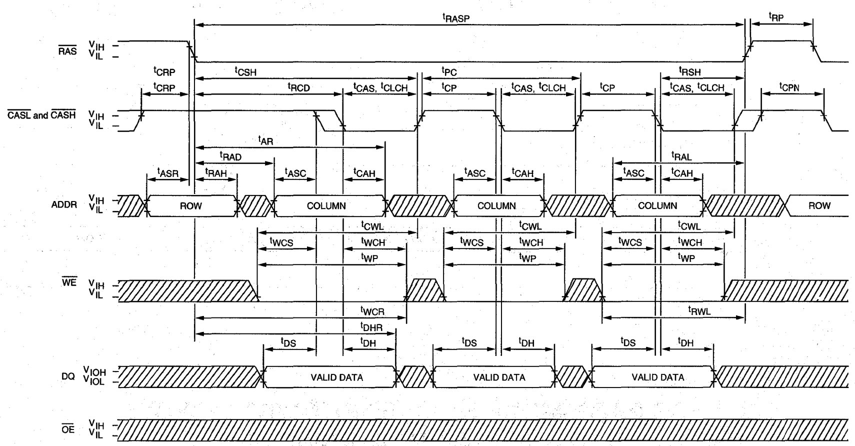
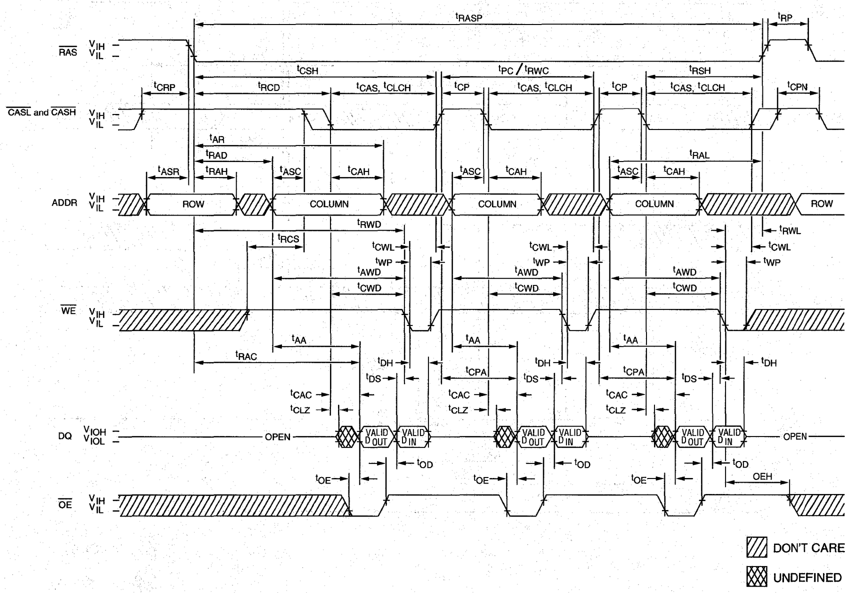
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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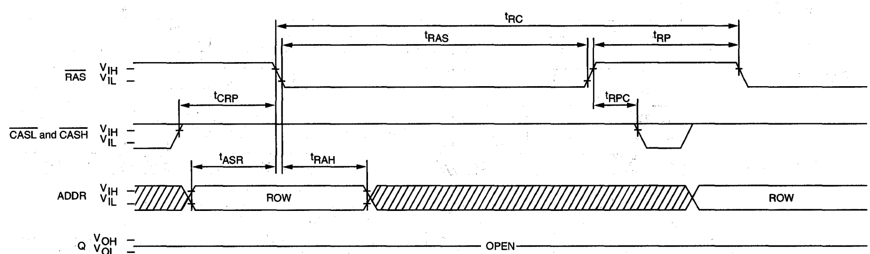
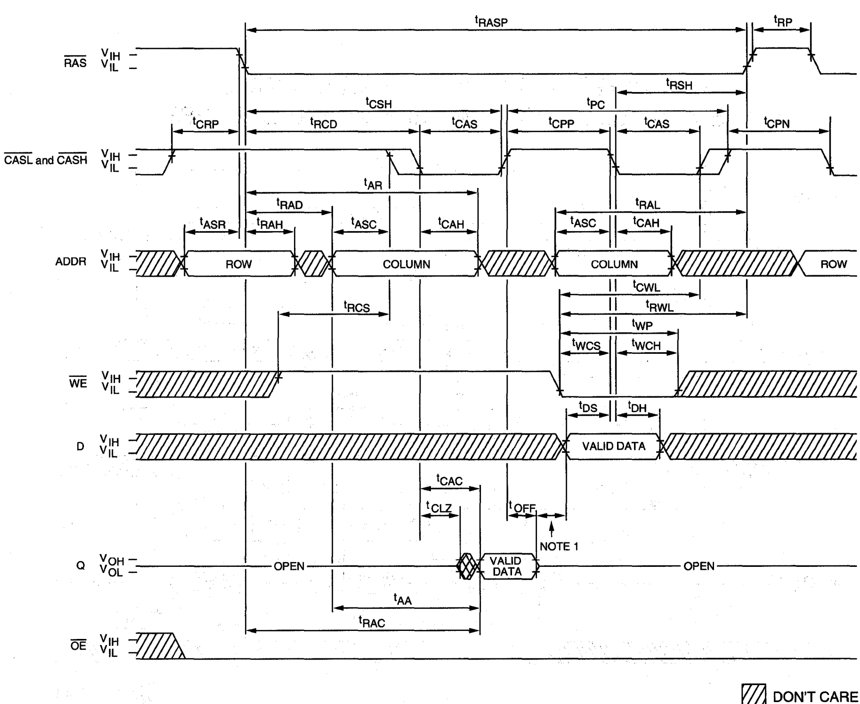
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE
(ADDR = A0-A9, $\overline{\text{OE}}$; $\overline{\text{WE}}$ = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to High-Z; that is completion of ^{t}OFF. ^{t}CPP is equal to ^{t}OFF + ^{t}DS(MIN) + guardband between data-out and driving new data-in.

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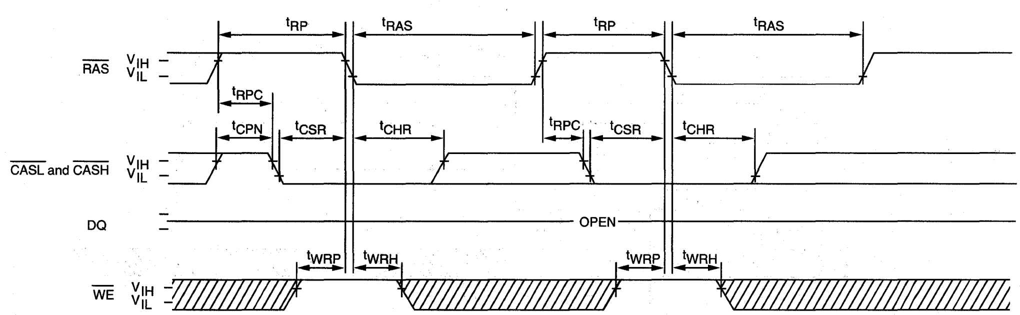
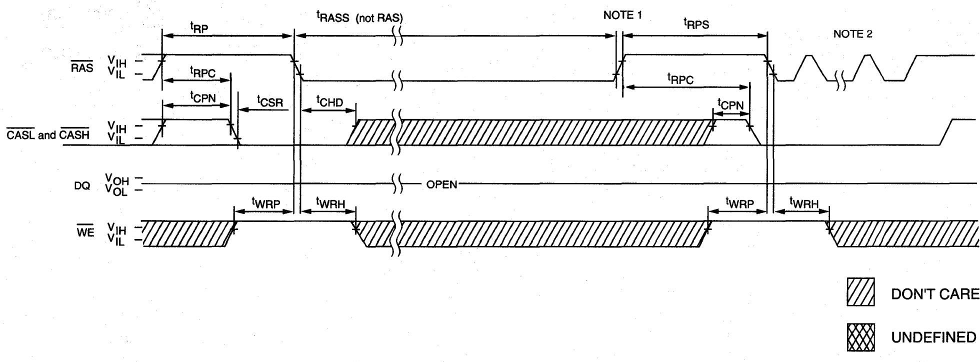
CBR REFRESH CYCLE
(A0-A9, $\overline{OE}$ = DON'T CARE)



SELF REFRESH CYCLE ("SLEEP MODE")
(A0-A9, $\overline{OE}$ = DON'T CARE)



DON'T CARE

UNDEFINED

NOTE:
1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a compete burst of all rows should be executed.

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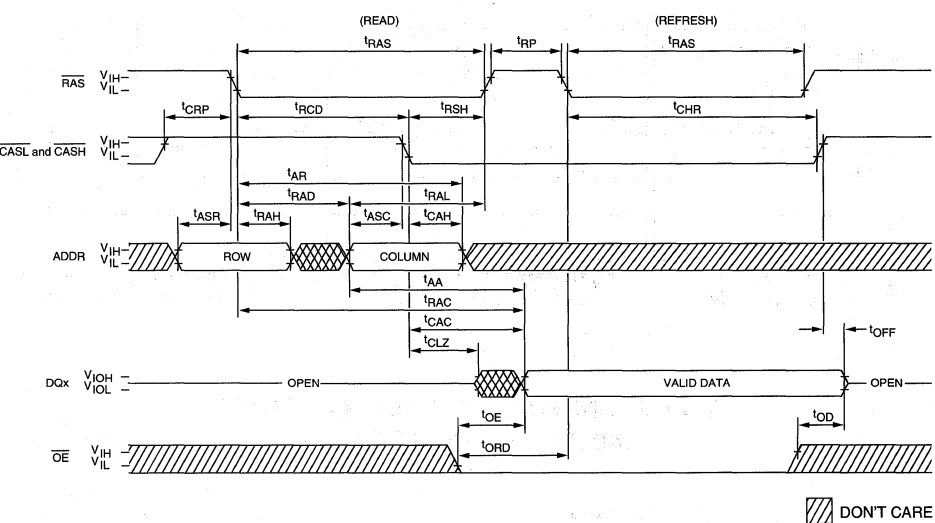
HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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DRAMs 1

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SYNCHRONOUS DRAM SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package/# of Pins		Page
				Standby	Active	SOJ	TSOP	
4 Meg x 4	BURST	MT48LC4M4R1	10, 12, 13	3mW	200mW	-	44	2-1
4 Meg x 4	BURST	MT48LC4M4R1 S	10, 12, 13	3mW	200mW	-	44	2-1
2 Meg x 8	BURST	MT48LC2M8S1	10, 12, 13	3mW	200mW	-	44	2-3
2 Meg x 8	BURST	MT48LC2M8S1 S	10, 12, 13	3mW	200mW	-	44	2-3
2 Meg x 8	BURST	MT48LC2M8K3 S	10, 12, 13	2mW	200mW	32	44	2-5

SYNCHRONOUS DRAM

4 MEG x 4 SDRAM

Pulsed $\overline{\text{RAS}}$, Dual Bank, BURST Mode, 3.3V, SELF REFRESH

FEATURES

- Fully synchronous; all signals (excluding clock enable) registered to positive edge of system clock
- Meets all JEDEC functional specifications
- Dual internal banks: dual 2 Meg x 4 architecture
- Programmable burst-lengths: 2, 4, 8 cycles or full-page burst
- Programmable burst-sequence: sequential or interleave
- Burst termination
- Multiple burst READ, single WRITE capability
- Hidden precharge capability with optional automatic precharge command
- Programmable READ latency: 1, 2 or 3 clocks
- Industry-standard x8 pinouts, timing, functions and packages
- Refresh modes: AUTO and SELF
- Standard and extended AUTO REFRESH rates
- High-performance CMOS silicon-gate process
- Lead-over-chip assembly architecture
- Single +3.3V ±0.3V power supply
- Low power, 3mW standby; 200mW active, typical
- LVTTL-compatible
- CKE-controlled power-down and suspend operations
- Mode register programming
- JEDEC-standard command set (pulsed $\overline{\text{RAS}}$)

OPTIONS

OPTIONS	MARKING
• Timing	
10ns access (≤100 MHz)	-10
12ns access (≤83 MHz)	-12
13.3ns access (≤75 MHz)	-13
• Auto Refresh	
4,096-cycle in 64ms (15.6µs/row)	none
4,096-cycle in 128ms (31.25µs/row)	S
• SELF REFRESH	
Not allowed	none
Allowed	S
• Plastic Packages	
44-pin TSOP (400 mil)—forward	TG

- Part Number Example: MT48LC4M4R1TG-10 S

PIN ASSIGNMENT (Top View)

44-Pin TSOP FORWARD
(DD-7)

MT48C4M4R1TG

Signal	Pin	Pin	Signal
Vcc	1	44	Vss
NC	2	43	NC
VssQ	3	42	VssQ
DQ1	4	41	DQ4
VccQ	5	40	VccQ
NC	6	39	NC
VssQ	7	38	VssQ
DQ2	8	37	DQ3
VccQ	9	36	VccQ
NC	10	35	NC
NC	11	34	NC
$\overline{\text{WE}}$	12	33	DQM
$\overline{\text{CAS}}$	13	32	CLK
$\overline{\text{RAS}}$	14	31	CKE
$\overline{\text{CS}}$	15	30	NC
BA	16	29	A9
A10	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
Vcc	22	23	Vss

GENERAL DESCRIPTION

The MT48LC4M4R1(S) is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x4 configuration. It is structured as a dual 2 Meg x 4 DRAM with a synchronous interface. Each byte is uniquely addressed through a bank-select bit and 20 address bits. The bank select and address are entered first by $\overline{\text{RAS}}$ registering (row active command) 12 bits (A0-A10, BA) and then $\overline{\text{CAS}}$ registering 11 bits (A0-A9, BA). At $\overline{\text{CAS}}$ registration (READ or WRITE command), address bit A10 defines auto-precharge state (active HIGH). Bank selection is controlled by BA during both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ registration.

The MT48LC4M4R1 is designed to operate in a synchronous, 3.3V memory system. All input and output signals, with the exception of clock enable (CKE) during POWER-DOWN and SELF REFRESH modes, are synchronized to the positive-going edge of the system clock (CLK).

The synchronous DRAM has several programmable features to allow maximum performance in each user's system. Additionally, bank switching between the two internal memory banks in conjunction with the programmable BURST mode provides very high-speed performance.

The synchronous DRAM allows both AUTO REFRESH (during normal operation) and SELF REFRESH (for low-power, data-retention operation).

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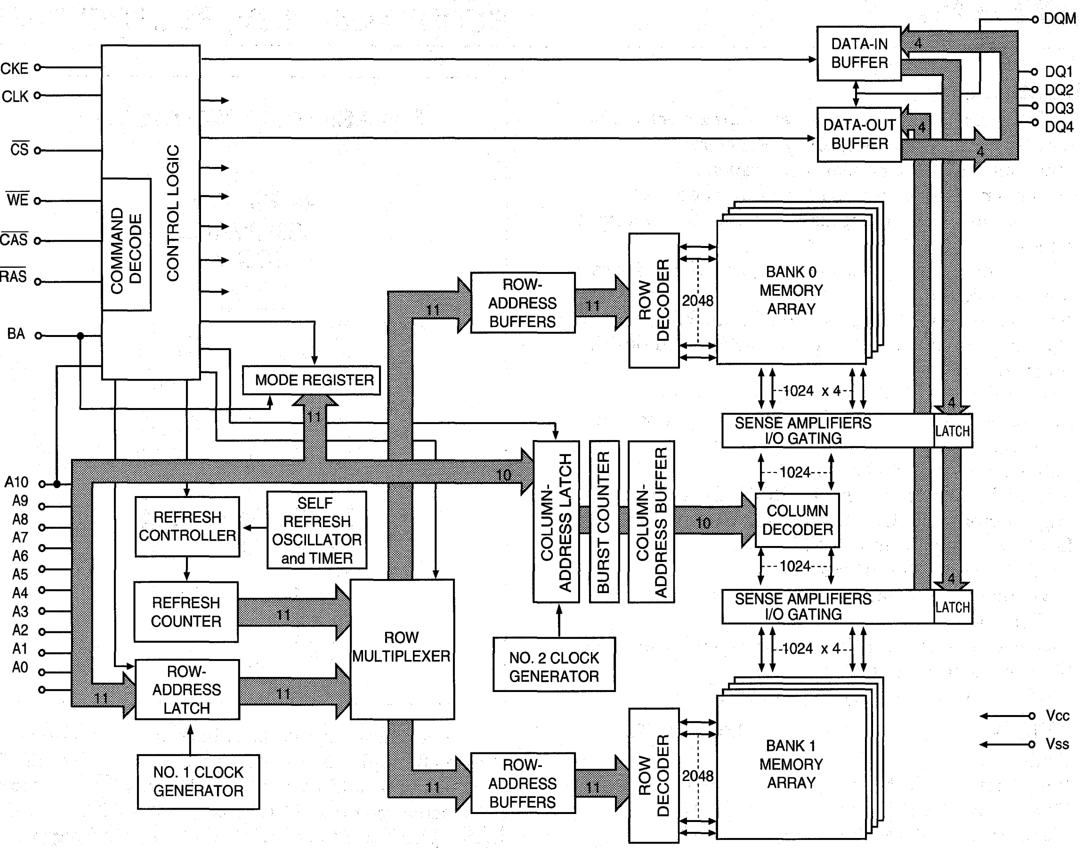
SYNCHRONOUS DRAM

FUNCTIONAL BLOCK DIAGRAM



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SYNCHRONOUS DRAM

2 MEG x 8 SDRAM

Pulsed $\overline{RAS}$, Dual Bank, BURST Mode, 3.3V, SELF REFRESH

FEATURES

- Fully synchronous; all signals (excluding clock enable) registered to positive edge of system clock
- Meets all JEDEC functional specifications
- Dual internal banks: dual 1 Meg x 8 architecture
- Programmable burst-lengths: 2, 4, 8 cycles or full-page burst
- Programmable burst-sequence: sequential or interleave
- Burst termination
- Multiple burst READ, single WRITE capability
- Hidden precharge capability with optional automatic precharge command
- Programmable READ latency: 1, 2 or 3 clocks
- Industry-standard x8 pinouts, timing, functions and packages
- Refresh modes: AUTO and SELF
- Standard and extended AUTO REFRESH rates
- High-performance CMOS silicon-gate process
- Lead-over-chip assembly architecture
- Single +3.3V ±0.3V power supply
- Low power, 3mW standby; 200mW active, typical
- LVTTL-compatible
- CKE-controlled power-down and suspend operations
- Mode register programming
- JEDEC-standard command set (pulsed $\overline{RAS}$)

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
10ns access (≤100 MHz)	-10
12ns access (≤83 MHz)	-12
13.3ns access (≤75 MHz)	-13
• AUTO REFRESH	
4,096-cycle in 64ms (15.6µs/row)	none
4,096-cycle in 128ms (31.25µs/row)	S
• SELF REFRESH	
Not allowed	none
Allowed	S
• Plastic Packages	
44-pin TSOP (400 mil)—forward	TG

- Part Number Example: MT48LC2M8S1TG-10 S

PIN ASSIGNMENT (Top View)

44-Pin TSOP FORWARD
(DD-7)

MT48C2M8S1TG

Signal	Pin	Pin	Signal
Vcc	1	44	Vss
DQ1	2	43	DQ8
VssQ	3	42	VssQ
DQ2	4	41	DQ7
VccQ	5	40	VccQ
DQ3	6	39	DQ6
VssQ	7	38	VssQ
DQ4	8	37	DQ5
VccQ	9	36	VccQ
NC	10	35	NC
NC	11	34	NC
$\overline{WE}$	12	33	DQM
$\overline{CAS}$	13	32	CLK
$\overline{RAS}$	14	31	CKE
$\overline{CS}$	15	30	NC
BA	16	29	A9
A10	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
Vcc	22	23	Vss

GENERAL DESCRIPTION

The MT48LC2M8S1(S) is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x8 configuration. It is structured as a dual 1 Meg x 8 DRAM with a synchronous interface. Each byte is uniquely addressed through a bank-select bit and 20 address bits. The bank select and address are entered first by $\overline{RAS}$ registering (row active command) 12 bits (A0-A10, BA) and then $\overline{CAS}$ registering 10 bits (A0-A8, BA). At $\overline{CAS}$ registration (READ or WRITE command), address bit A10 defines auto-precharge state (active HIGH). Bank selection is controlled by BA during both $\overline{RAS}$ and $\overline{CAS}$ registration.

The MT48LC2M8S1 is designed to operate in a synchronous, 3.3V memory system. All input and output signals, with the exception of clock enable (CKE) during POWER-DOWN and SELF REFRESH modes, are synchronized to the positive-going edge of the system clock (CLK).

The synchronous DRAM has several programmable features to allow maximum performance in each user's system. Additionally, bank switching between the two internal memory banks in conjunction with the programmable BURST mode provides very high-speed performance.

The synchronous DRAM allows both AUTO REFRESH (during normal operation) and SELF REFRESH (for low-power, data-retention operation).

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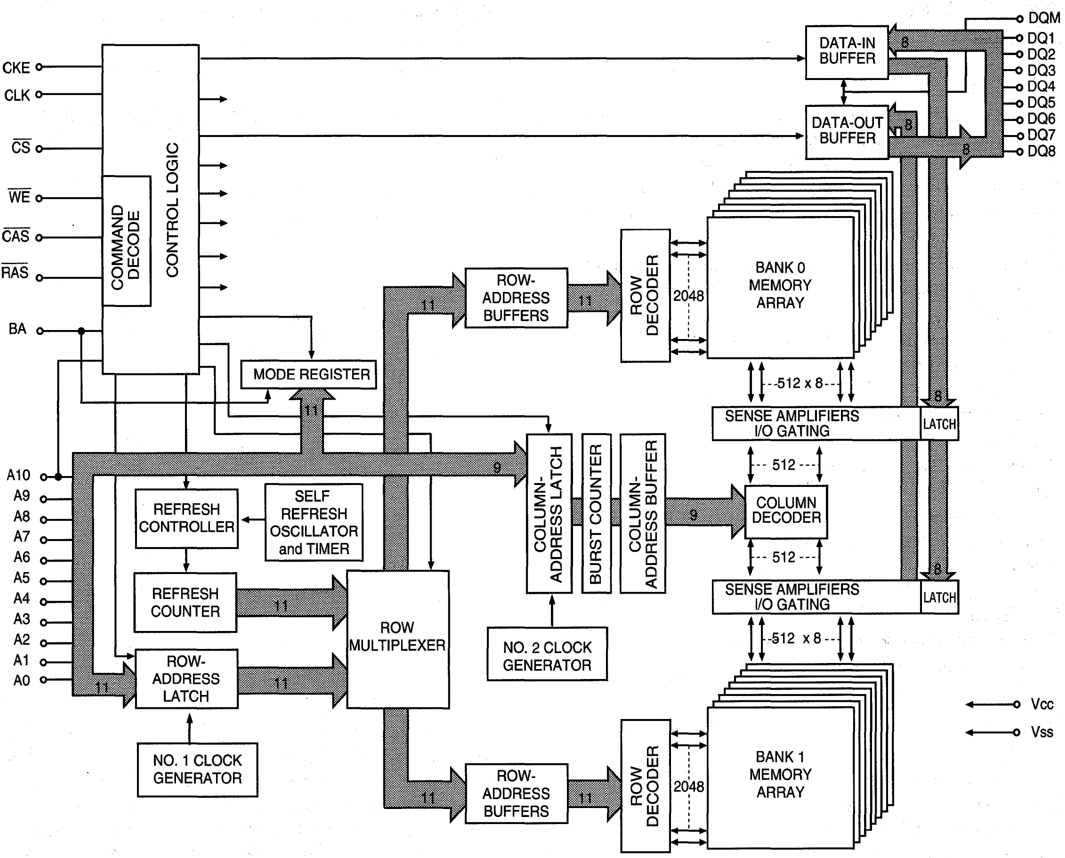
SYNCHRONOUS DRAM

FUNCTIONAL BLOCK DIAGRAM



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SYNCHRONOUS DRAM

2 MEG x 8 SDRAM

Level $\overline{RAS}$, Single Bank, BURST Mode, 3.3V, SELF REFRESH

FEATURES

- Fully synchronous; all signals registered to positive edge of system clock
- JEDEC-standard 3.3V power supply
- Single bank: 2 Meg x 8 architecture
- Programmable burst-lengths: 2, 4, 8 cycles or full-page burst
- Programmable burst-sequence: sequential or interleave
- Hidden precharge capability
- Programmable READ latency: 1, 2 or 3 clocks
- Standard x8 pinouts, timing, functions and packages
- Refresh modes: AUTO and SELF REFRESH
- High-performance CMOS silicon-gate process
- Lead-over-chip assembly architecture
- Single +3.3V ±0.3V power supply
- Low power, 2mW standby; 200mW active, typical
- LVTTL-compatible
- CKE-controlled power-down and suspend operations
- Mode register programming with power-up default
- Second source to Samsung's level-$\overline{RAS}$ synchronous DRAM (SDRAM)

OPTIONS

OPTIONS	MARKING
• Timing	
10ns access (≤100 MHz)	-10
12ns access (≤83 MHz)	-12
13ns access (≤77 MHz)	-13
• Auto Refresh	
2,048–cycle in 32ms (15.6µs/row)	none
• Plastic Packages	
32-pin SOJ (400 mil)	DJ
44-pin TSOP (400 mil)	TG

- Part Number Example: MT48LC2M8K3TG-10 S

PIN ASSIGNMENT (Top View)

32-Pin SOJ (DC-5)

Signal	Pin	Pin	Signal
VDD	1	32	Vss
DQ1	2	31	DQ8
DQ2	3	30	DQ7
DQ3	4	29	DQ6
DQ4	5	28	DQ5
Vss	6	27	VDD
$\overline{WE}$	7	26	DQM
$\overline{CAS}$	8	25	CLK
$\overline{RAS}$	9	24	CKE
A11	10	23	A9
A10	11	22	A8
A0	12	21	A7
A1	13	20	A6
A2	14	19	A5
A3	15	18	A4
VDD	16	17	Vss

44-Pin TSOP (DD-7)

Signal	Pin	Pin	Signal
VDD	1	44	Vss
DQ1	2	43	DQ8
VssQ	3	42	VssQ
DQ2	4	41	DQ7
VDDQ	5	40	VDDQ
DQ3	6	39	DQ6
VssQ	7	38	VssQ
DQ4	8	37	DQ5
VDDQ	9	36	VDDQ
NC	10	35	NC
NC	11	34	NC
$\overline{WE}$	12	33	DQM
$\overline{CAS}$	13	32	CLK
$\overline{RAS}$	14	31	CKE
NC	15	30	NC
A11	16	29	A9
A10	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
VDD	22	23	Vss

GENERAL DESCRIPTION

The MT48LC2M8K3 S is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x8 configuration. It is structured as a 2 Meg x 8 DRAM with a synchronous interface. Each byte is uniquely addressed through a bank-select bit and 20 address bits. The addresses are entered first by $\overline{RAS}$ registering 12 bits (A0-A11) and then $\overline{CAS}$ registering 9 bits (A0-A8).

The MT48LC2M8K3 S is designed to operate in a synchronous, 3.3V memory system. All input and output signals are synchronized to the positive going edge of the system clock (CLK).

The synchronous DRAM has several programmable features to allow maximum performance in each user's system. Additionally, the programmable BURST mode provides very high-speed performance.

The synchronous DRAM allows both AUTO REFRESH (during normal operation) and SELF REFRESH (for low-power, data-retention operation).

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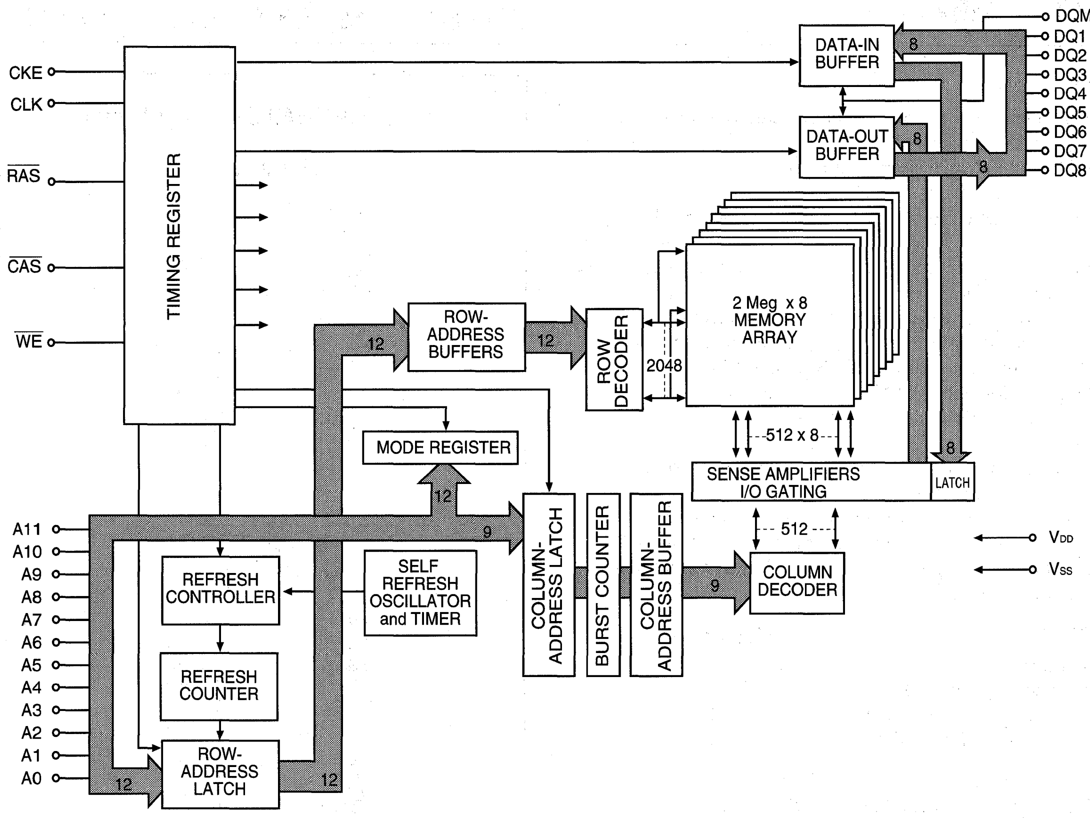
FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MT48LC2M8K3 S is a 16 Meg synchronous DRAM organized in a x8 configuration. It is structured as a 2 Meg x 8 DRAM with synchronous interfacing and control logic. The key advancement of the synchronous DRAM is its ability to synchronously burst data (BURST mode) at a high-speed data rate via automatic column-address generation. Additionally, all input and output signals are synchronized to the system's clock. The positive-going edge of the system clock (CLK) provides the registering trigger which synchronizes the synchronous DRAM.

The synchronous DRAM must first be initialized and have its mode register set or it will be in the default state. Once the mode register is set, the synchronous DRAM may be accessed. Each byte is uniquely accessed by registering the 12 row-address bits (A0-A11) via the active command ($\overline{RAS}$ latched LOW), followed by registering the nine column-address bits (A0-8) via a READ or WRITE command.

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DRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Part Number	Optional Access Cycle	Access Time (ns)	Power Dissipation		Package		Page
				Standby	Active	SIMM	DIMM	
1 Meg x 8	MT2D18		60,70,80	6mW	450mW	30	-	3-1
4 Meg x 8	MT2D48		60,70	6mW	400mW	30	-	3-11
4 Meg x 8	MT8D48		60,70,80	24mW	1,800mW	30	-	3-21
1 Meg x 9	MT3D19		60,70,80	9mW	625mW	30	-	3-31
4 Meg x 9	MT3D49		60,70	9mW	575mW	30	-	3-41
4 Meg x 9	MT9D49		60,70,80	27mW	2,025mW	30	-	3-51
2 Meg x 16	MT8D132	LP	60,70,80	24mW	1,800mW	72	-	3-61
4 Meg x 16	MT16D(T)232	LP	60,70,80	48mW	1,824mW	72	-	3-87
8 Meg x 16	MT8D432		60,70	24mW	1,600mW	72	-	3-99
16 Meg x 16	MT16D832		60,70	48mW	1,624mW	72	-	3-137
2 Meg x 18	MT12D136	LP	60,70,80	36mW	2,500mW	72	-	3-149
4 Meg x 18	MT24D236	LP	60,70,80	72mW	2,536mW	72	-	3-161
8 Meg x 18	MT12D436		60,70	52mW	3,100mW	72	-	3-173
16 Meg x 18	MT24D836		60,70	72mW	2,536mW	72	-	3-197
1 Meg x 32	MT8D132	LP	60,70,80	24mW	1,800mW	72	-	3-61
1 Meg x 32	MT8LD132(S)	S, LV	60,70,80	1.6mW	1,440mW	72	-	3-73
2 Meg x 32	MT16D(T)232	LP	60,70,80	48mW	1,824mW	72	-	3-87
2 Meg x 32	MT16LD232(S)	S, LV	60,70,80	1.6mW	1,440mW	72	-	3-73
4 Meg x 32	MT8D432		60,70	24mW	1,600mW	72	-	3-99
4 Meg x 32	MT8LD432(S)	S, LV	60,70	8mW	1,440mW	72	-	3-111
4 Meg x 32	MT32D432	LP	60,70,80	96mW	7,200mW	72	-	3-125
8 Meg x 32	MT16LD832(S)	S, LV	60,70	16mW	1,440mW	72	-	3-111
8 Meg x 32	MT16D832		60,70	48mW	1,624mW	72	-	3-137
1 Meg x 36	MT12D136	LP	60,70,80	36mW	2,500mW	72	-	3-149
2 Meg x 36	MT24D236	LP	60,70,80	72mW	2,536mW	72	-	3-161
4 Meg x 36	MT12D436		60,70	36mW	2,500mW	72	-	3-173
4 Meg x 36	MT36D436	LP	60,70,80	108mW	8,100mW	72	-	3-185
8 Meg x 36	MT24D836		60,70	72mW	2,536mW	72	-	3-197
1 Meg x 40	MT10D140	LP	60,70,80	30mW	2,250mW	72	-	3-209
2 Meg x 40	MT20D240	LP	60,70,80	60mW	2,280mW	72	-	3-221
4 Meg x 40	MT10D440	LP	60,70	30mW	2,000mW	72	-	3-233
8 Meg x 40	MT20D840	LP	60,70	60mW	2,030mW	72	-	3-247
1 Meg x 64	MT16D(T)164	LP	60,70,80	48mW	3,600mW	-	168	3-261
1 Meg x 64	MT16LD(T)164(S)	S, LV	60,70,80	2mW	1,200mW	-	168	3-275
4 Meg x 64	MT16D(T)464		60,70	48mW	3,200mW	-	168	3-291
4 Meg x 64	MT16LD(T)464(S)	S, LV	60,70	16mW	2,400mW	-	168	3-305
4 Meg x 72	MT24D(T)472		60,70	56mW	5,000mW	-	168	3-321
4 Meg x 72	MT24LD(T)472(S)	S, LV	60,70	56mW	3,400mW	-	168	3-335

LP = Low Power, Extended Refresh; LV = Low Voltage; S = SELF REFRESH
NOTE: All modules include FAST PAGE MODE cycle.

DRAM MODULE

1 MEG x 8 DRAM

FAST PAGE MODE

FEATURES

- Industry-standard pinout in a 30-pin, single-in-line memory module
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 6mW standby; 450mW active, typical
- All device pins are TTL-compatible
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- Low profile
- 1,024-cycle refresh distributed across 16ms

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Leadless 30-pin SIMM	M

- Part Number Example: MT2D18M-6

PIN ASSIGNMENT (Top View)

30-Pin SIMM
(DE-1)

MT2D18M

Pin	Signal
1	Vcc
2	$\overline{\text{CAS}}$
3	DQ1
4	A0
5	A1
6	DQ2
7	A2
8	A3
9	Vss
10	DQ3
11	A4
12	A5
13	DQ4
14	A6
15	A7
16	DQ5
17	A8
18	A9
19	NC
20	DQ6
21	$\overline{\text{WE}}$
22	Vss
23	DQ7
24	NC
25	DQ8
26	NC
27	$\overline{\text{RAS}}$
28	NC
29	NC
30	Vcc

GENERAL DESCRIPTION

The MT2D18 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{\text{RAS}}$ is used to latch the first 10 bits and $\overline{\text{CAS}}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. Early WRITE occurs when $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, and the output pins remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{\text{RAS}}$ followed by a column-address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE) or $\overline{\text{RAS}}$ REFRESH cycle ($\overline{\text{RAS}}$ ONLY, CBR or HIDDEN) so that all 1,024 combinations of $\overline{\text{RAS}}$ addresses (A0-A9) are executed at least every 16ms regardless of sequence.

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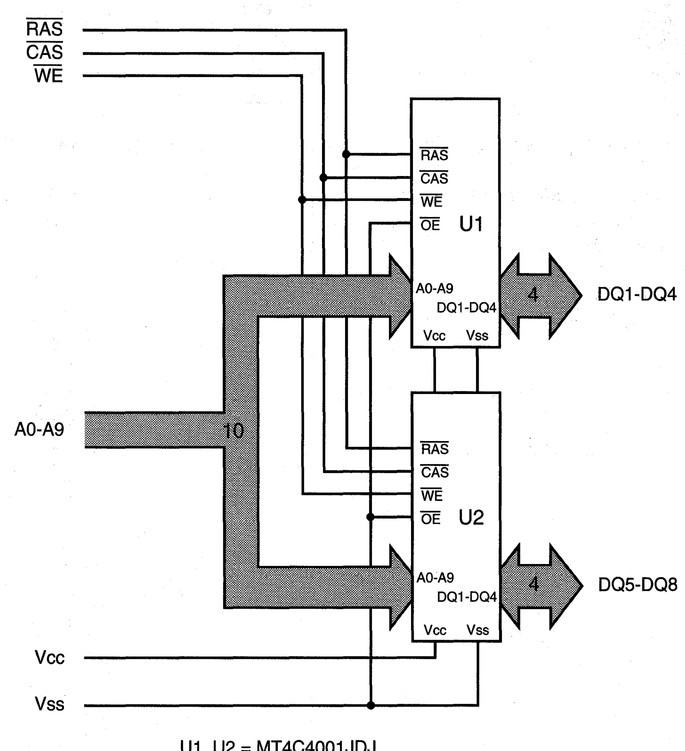
FUNCTIONAL BLOCK DIAGRAM



U1, U2 = MT4C4001JDJ

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature .... -55°C to +125°C
Power Dissipation 2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6, 26) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	A0-A9, RAS, CAS, WE	II	-4	4	µA	
OUTPUT LEAKAGE (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	DQ1-DQ8	IOZ	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low (Logic 0) Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	4	4	4	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	ICC2	2	2	2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	220	200	180	mA	2, 26, 29
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])	ICC4	160	140	120	mA	2, 26, 29
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])	ICC5	220	200	180	mA	26, 29
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC6	220	200	180	mA	19, 26

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		13	pF	17
Input Capacitance: RAS, CAS, WE	C_{I2}		17	pF	17
Input/Output Capacitance: DQ1-DQ8	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITEcycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		n/a	21
Access time from RAS	^tRAC		60		70		80	ns	8
Access time from CAS	^tCAC		15		20		20	ns	9
Access time from column-address	^tAA		30		35		40	ns	
Access time from CAS precharge	^tCPA		35		40		45	ns	
RAS pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^tRSH	15		20		20		ns	
RAS precharge time	^tRP	40		50		60		ns	
CAS pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^tCSH	60		70		80		ns	
CAS precharge time	^tCPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
RAS to CAS delay time	^tRCD	20	45	20	50	20	60	ns	13
CAS to RAS precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
RAS to column-address delay time	^tRAD	15	30	15	35	15	40	ns	22
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	10		15		15		ns	
Column-address hold time (referenced to RAS)	^tAR	45		50		55		ns	
Column-address to RAS lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^tRCH	0		0		0		ns	24
Read command hold time (referenced to RAS)	^tRRH	0		0		0		ns	24
CAS to output in Low-Z	^tCLZ	0		0		0		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^{t}OFF	3	15	3	20	3	20	ns	12, 28
$\overline{\text{WE}}$ command setup time	^{t}WCS	0		0		0		ns	
Write command hold time	^{t}WCH	10		15		15		ns	
Write command hold time (referenced to $\overline{\text{RAS}}$)	^{t}WCR	45		55		60		ns	
Write command pulse width	^{t}WP	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	^{t}RWL	15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	^{t}CWL	15		20		20		ns	
Data-in setup time	^{t}DS	0		0		0		ns	15
Data-in hold time	^{t}DH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{\text{RAS}}$)	^{t}DHR	45		55		60		ns	
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	^{t}REF		16		16		16	ms	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	^{t}RPC	0		0		0		ns	
$\overline{\text{CAS}}$ setup time (CBR REFRESH)	^{t}CSR	10		10		10		ns	19
$\overline{\text{CAS}}$ hold time (CBR REFRESH)	^{t}CHR	10		10		10		ns	19
$\overline{\text{WE}}$ hold time (CBR REFRESH)	^{t}WRH	10		10		10		ns	23
$\overline{\text{WE}}$ setup time (CBR REFRESH)	^{t}WRP	10		10		10		ns	23
$\overline{\text{WE}}$ hold time (WCBR test cycle)	^{t}WTH	10		10		10		ns	23
$\overline{\text{WE}}$ setup time (WCBR test cycle)	^{t}WTS	10		10		10		ns	23

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NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight RAS REFRESH cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ᵗREF refresh requirement is exceeded.
4. AC characteristics assume ᵗT = 5ns.
5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that ᵗRCD < ᵗRCD (MAX). If ᵗRCD is greater than the maximum recommended value shown in this table, ᵗRAC will increase by the amount that ᵗRCD exceeds the value shown.
9. Assumes that ᵗRCD ≥ ᵗRCD (MAX).
10. If CAS = VIH, data output is High-Z.
11. If CAS = VIL, data output may contain data from the last valid READ cycle.
12. ᵗOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the ᵗRCD (MAX) limit ensures that ᵗRAC (MAX) can be met. ᵗRCD (MAX) is specified as a reference point only; if ᵗRCD is greater than the specified ᵗRCD (MAX) limit, then access time is controlled exclusively by ᵗCAC.
14. ᵗRCH is referenced to the first rising edge of RAS or CAS.
15. These parameters are referenced to CAS leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ᵗCPN.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to OE being grounded on U1 and U2.
22. Operation within the ᵗRAD (MAX) limit ensures that ᵗRAC (MIN) and ᵗCAC (MIN) can be met. ᵗRAD (MAX) is specified as a reference point only; if ᵗRAD is greater than the specified ᵗRAD (MAX) limit, then access time is controlled exclusively by ᵗAA.
23. ᵗWTS and ᵗWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ᵗWRP and ᵗWRH in the CBR REFRESH cycle.
24. Either ᵗRCH or ᵗRRH must be satisfied for a READ cycle.
25. All other inputs at Vcc -0.2V.
26. Icc is dependent on cycle rates.
27. Extended refresh current is reduced as ᵗRAS is reduced from its maximum specification during the REFRESH cycle.
28. The 3ns minimum is a parameter guaranteed by design.
29. Column-address changed once each cycle.

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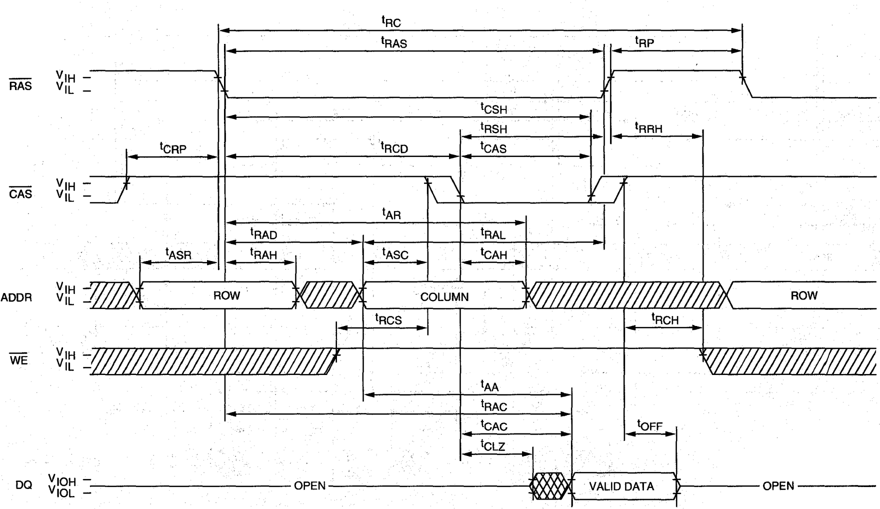
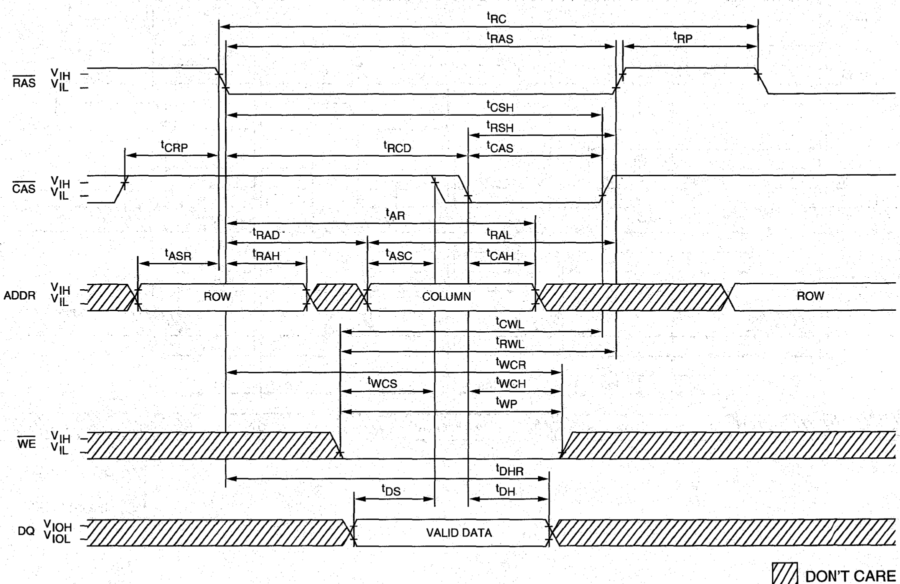
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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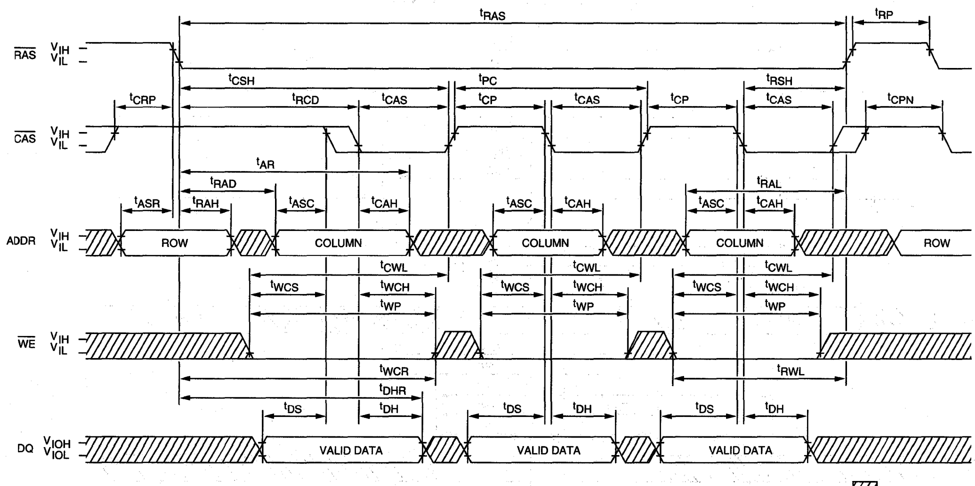
FAST-PAGE-MODE READ CYCLE

FAST-PAGE-MODE EARLY-WRITE CYCLE



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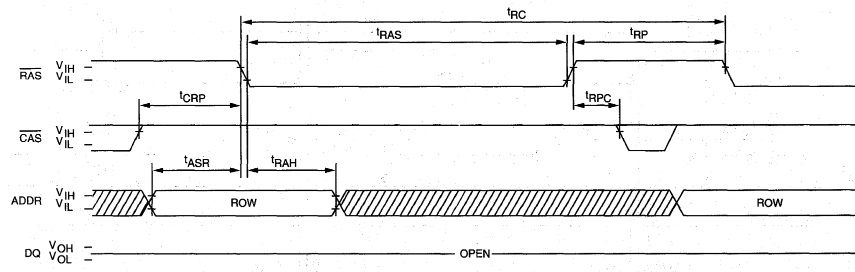
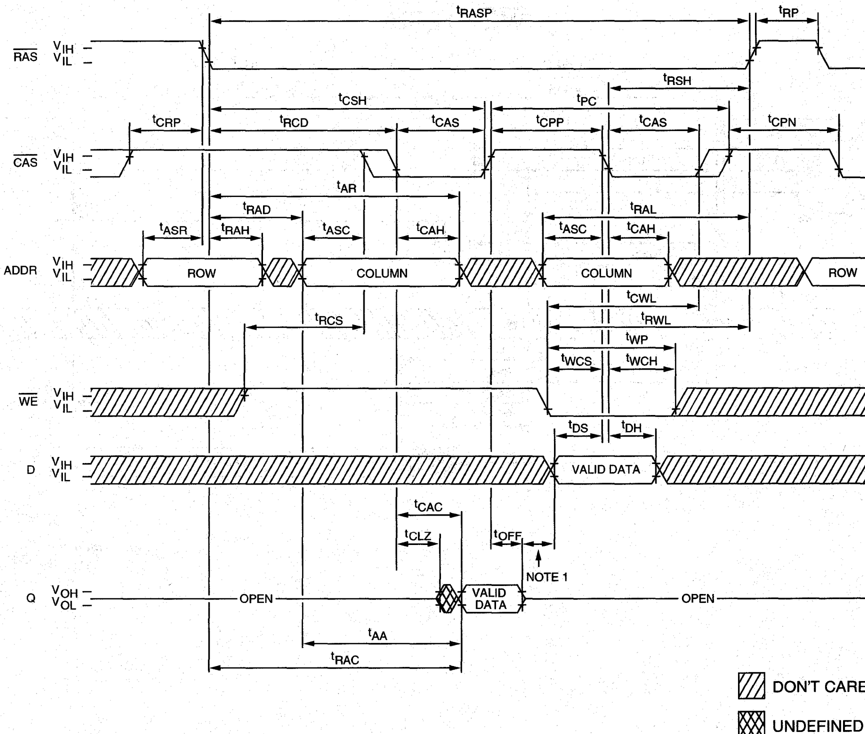
RAS ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

DRAM MODULE

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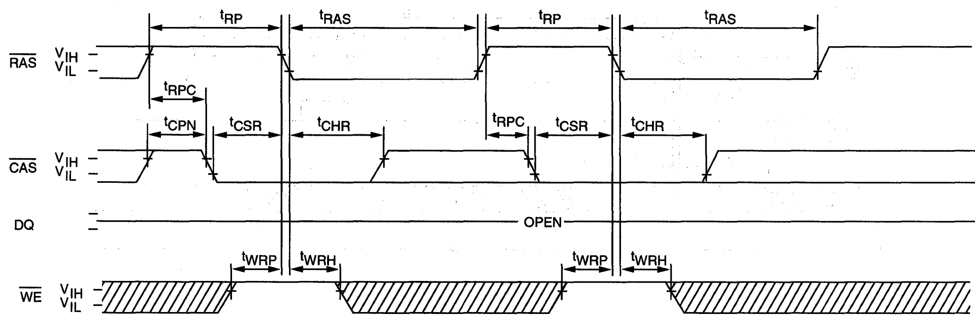
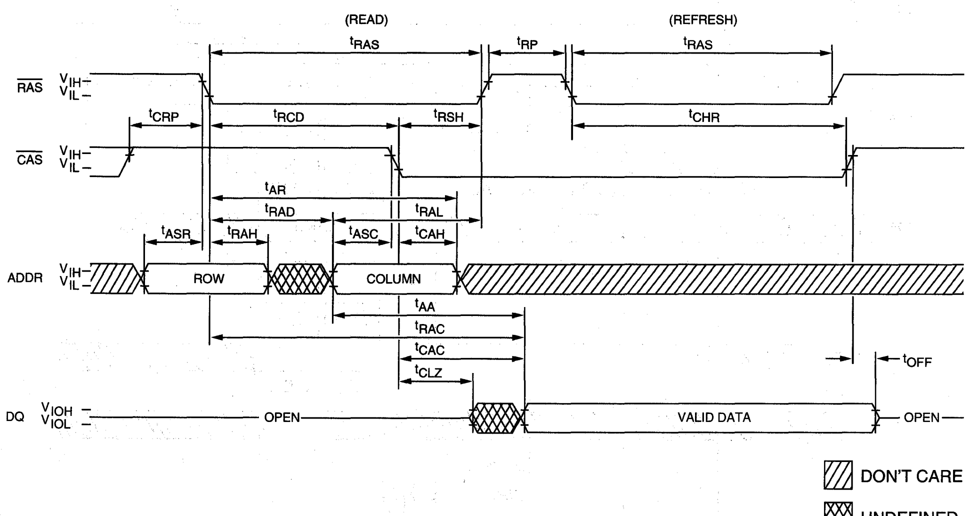
CBR REFRESH CYCLE
(A0-A9 = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
(WE = HIGH)



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DRAM MODULE

4 MEG x 8 DRAM
FAST PAGE MODE

FEATURES

- Industry-standard pinout in a 30-pin, single-in-line memory module
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 6mW standby; 400mW active, typical
- All device pins are TTL-compatible
- FAST PAGE MODE access cycle
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- Low profile

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Leadless 30-pin SIMM	M

- Part Number Example: MT2D48M-6

PIN ASSIGNMENT (Top View)

30-Pin SIMM
(DE-5)

MT2D48M

Pin	Signal
1	Vcc
2	CAS
3	DQ1
4	A0
5	A1
6	DQ2
7	A2
8	A3
9	Vss
10	DQ3
11	A4
12	A5
13	DQ4
14	A6
15	A7
16	DQ5
17	A8
18	A9
19	A10
20	DQ6
21	WE
22	Vss
23	DQ7
24	NC
25	DQ8
26	NC
27	RAS
28	NC
29	NC
30	Vcc

GENERAL DESCRIPTION

The MT2D48 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pins remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operations.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS-ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

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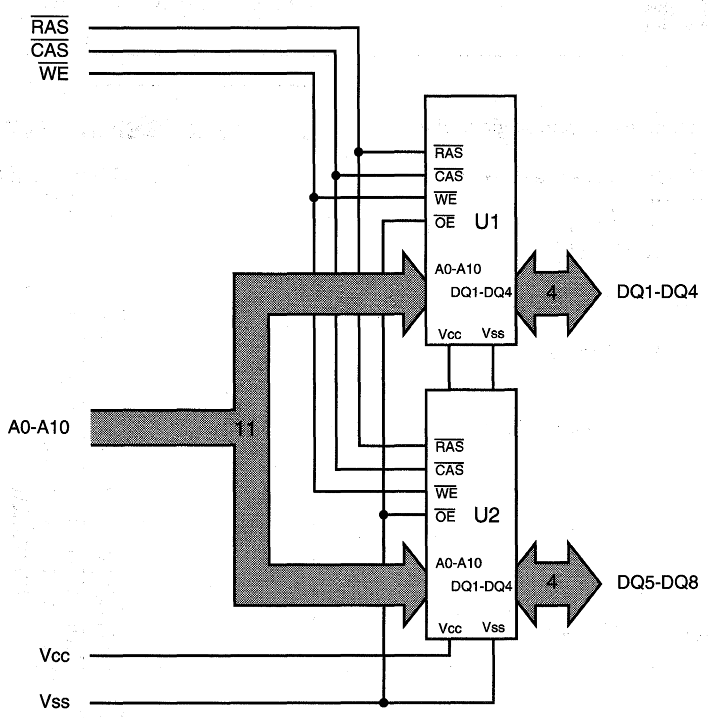
DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1, U2 = MT4C4M4B1DW

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature .... -55°C to +125°C
Power Dissipation 2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	A0-A10, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	I_I	-4	4	µA	
OUTPUT LEAKAGE (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	DQ1-DQ8	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low (Logic 0) Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	4	4	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = Vcc -0.2V)	I_{CC2}	2	2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC3}	240	220	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ${}^tPC$ = ${}^tPC$ [MIN])	I_{CC4}	180	160	mA	3, 4, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling; $\overline{CAS}$ = V_{IH}: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC5}	240	220	mA	3, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC6}	240	220	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		13	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		17	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		ns	22
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15
Access time from column-address	^tAA		30		35	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	25
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 25
$\overline{WE}$ command setup time	^tWCS	0		0		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
Write command pulse width	^tWP	10		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in setup time	^tDS	0		0		ns	21
Data-in hold time	^tDH	10		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	^tREF		32		32	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		ns	24

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
22. $\overline{OE}$ is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not possible.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
24. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.

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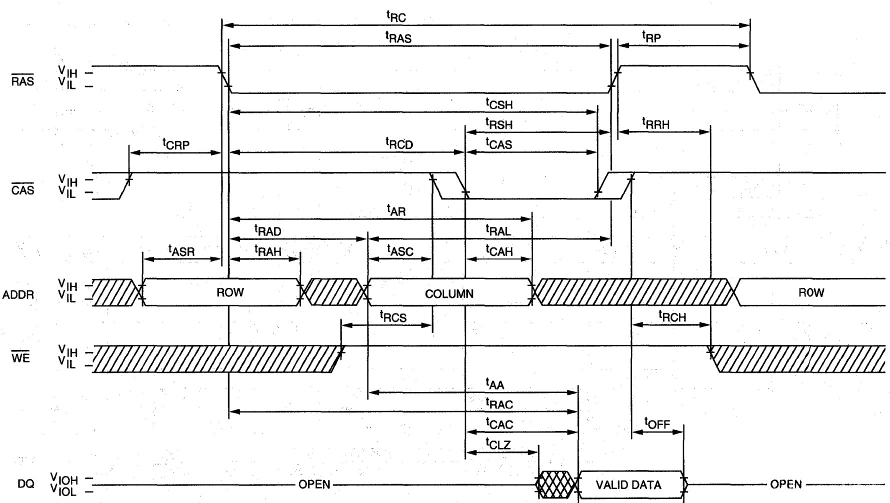
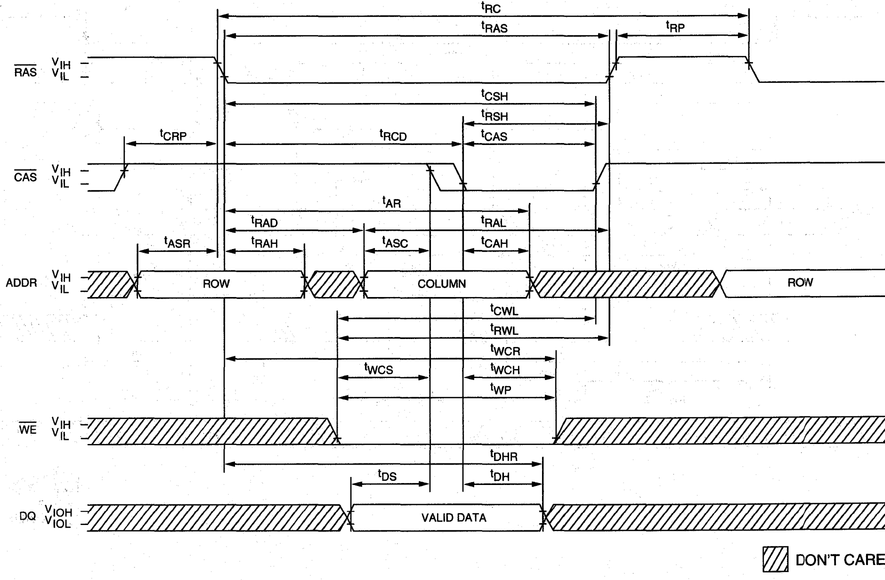
READ CYCLE



EARLY WRITE CYCLE



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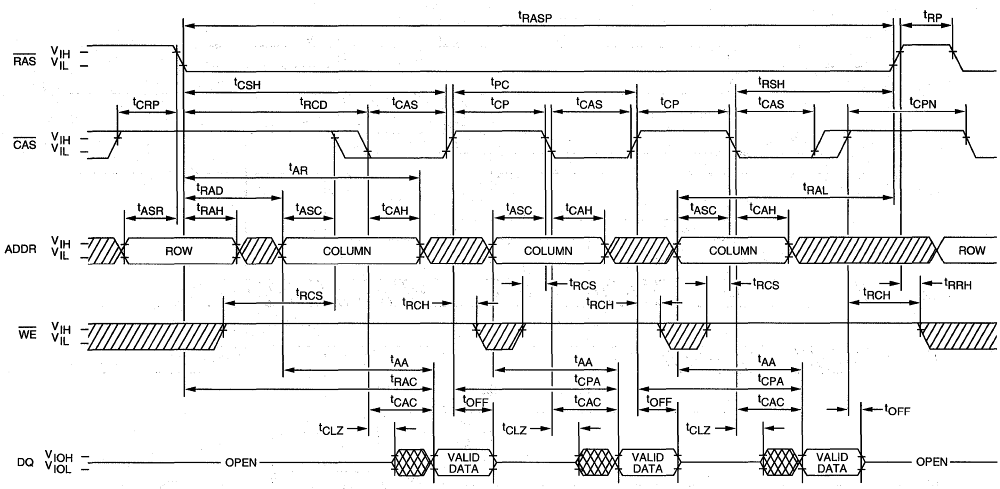
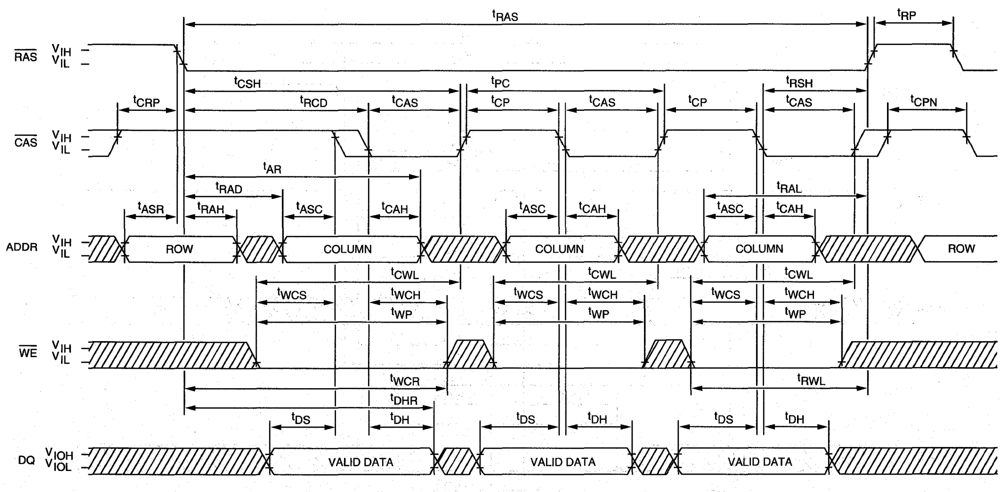
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



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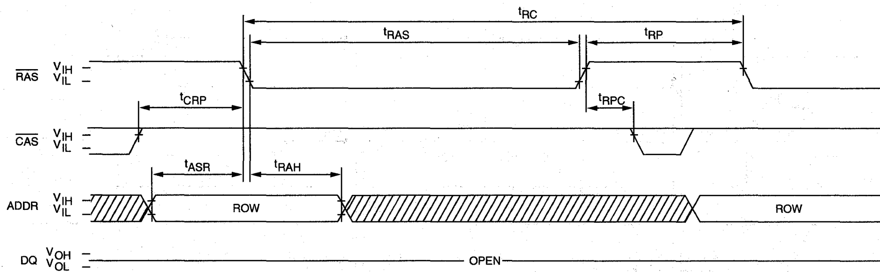
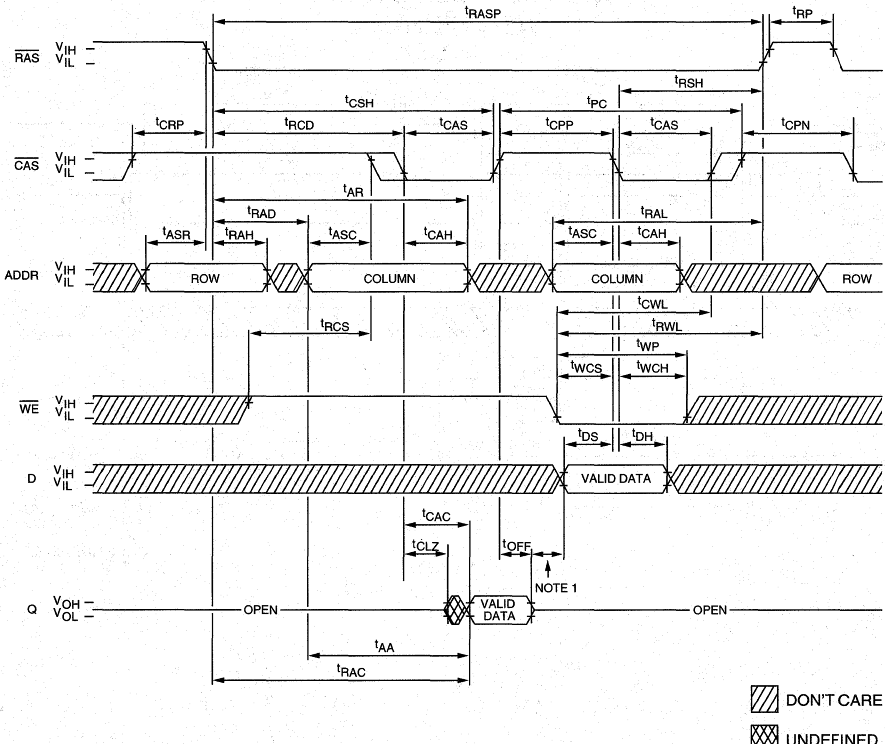
RAS ONLY REFRESH CYCLE
(ADDR = A0-A10; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

DRAM MODULE

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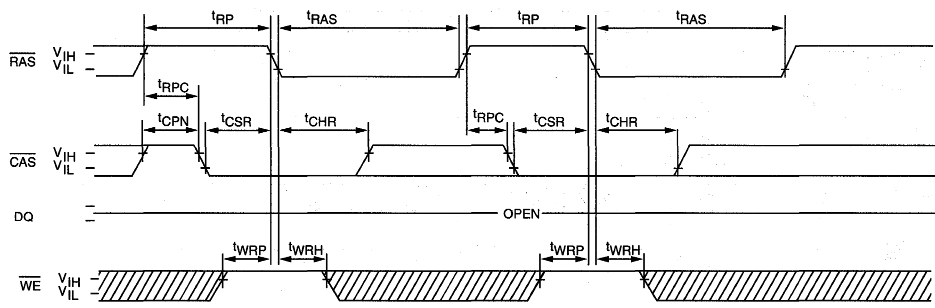
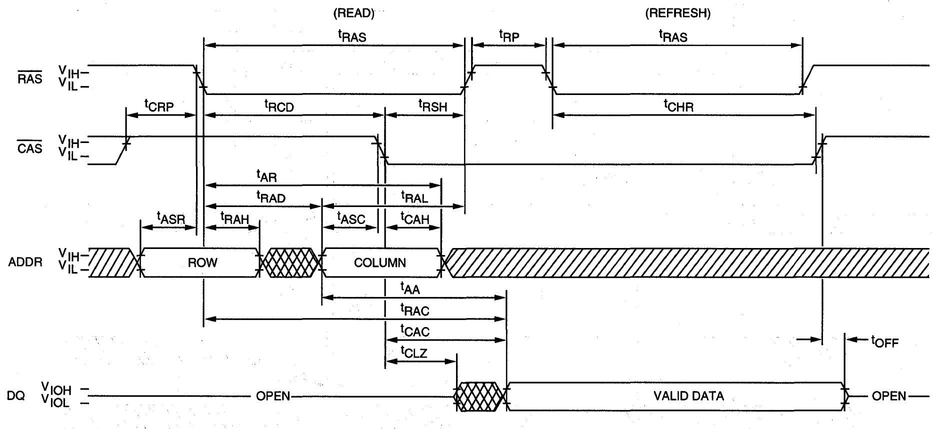
DRAM MODULE

CBR REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
(WE = HIGH)



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DRAM MODULE

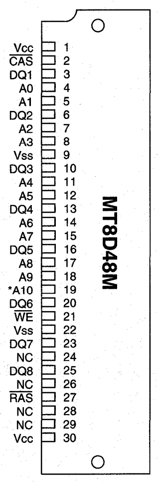
4 MEG x 8 DRAM
FAST PAGE MODE

FEATURES
- Industry-standard pinout in a 30-pin single-in-line package
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 24mW standby; 1,800mW active, typical
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- FAST PAGE MODE access cycle

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Leadless 30-pin SIMM	M

- Part Number Example: MT8D48M-6



*Address not used for RAS ONLY REFRESH

GENERAL DESCRIPTION

The MT8D48 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x8 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode, while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, and the ouput remains open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every16ms regardless of sequence.

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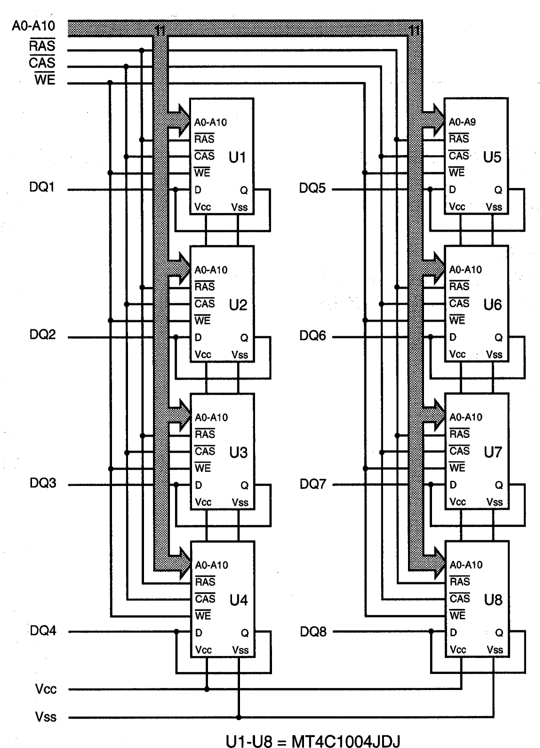
DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C1004JDJ

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES ᵗR	ADDRESSES ᵗC	DATA-IN/OUT DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	A0-A10, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$	II	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	DQ1-DQ8	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	16	16	16	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	8	8	8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: tRC = tRC [MIN])	ICC3	880	800	720	mA	3, 4, 27
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: tPC = tPC [MIN])	ICC4	640	560	480	mA	3, 4, 27
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = VIH: tRC = tRC [MIN])	ICC5	880	800	720	mA	3, 27
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: tRC = tRC [MIN])	ICC6	880	800	720	mA	3, 5

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CAPACITANCE

DESCRIPTION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	51	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{WE}$, $\overline{CAS}$	C_{I2}	67	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}	15	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a	23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		n/a	23
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	26
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	26
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	3	15	3	20	3	20	ns	20, 25
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	10		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	24
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	24

DRAM MODULE

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DRAM MODULE

NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {^tRCD}$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {^tRCD}$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
23. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
24. ^tWTS and ^tWTH are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Extended refresh current is reduced as ^tRAS is reduced from its maximum specification during the extended refresh cycle.
27. Column-address changed once each cycle.

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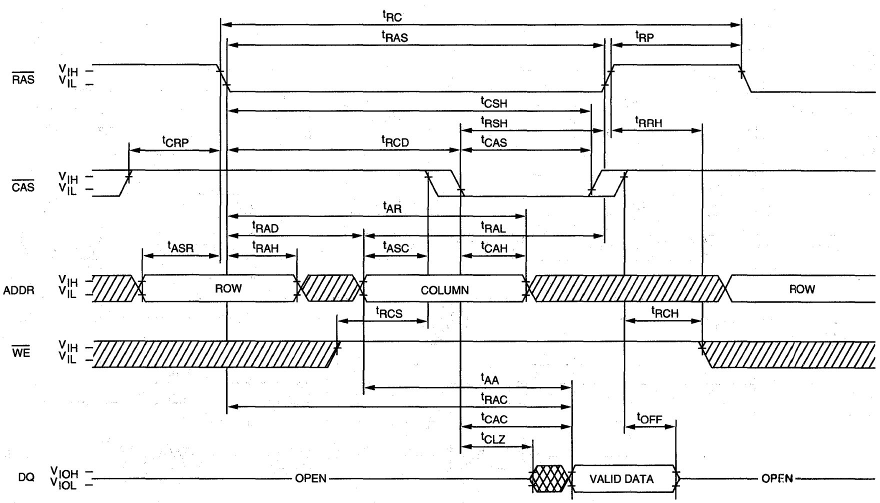
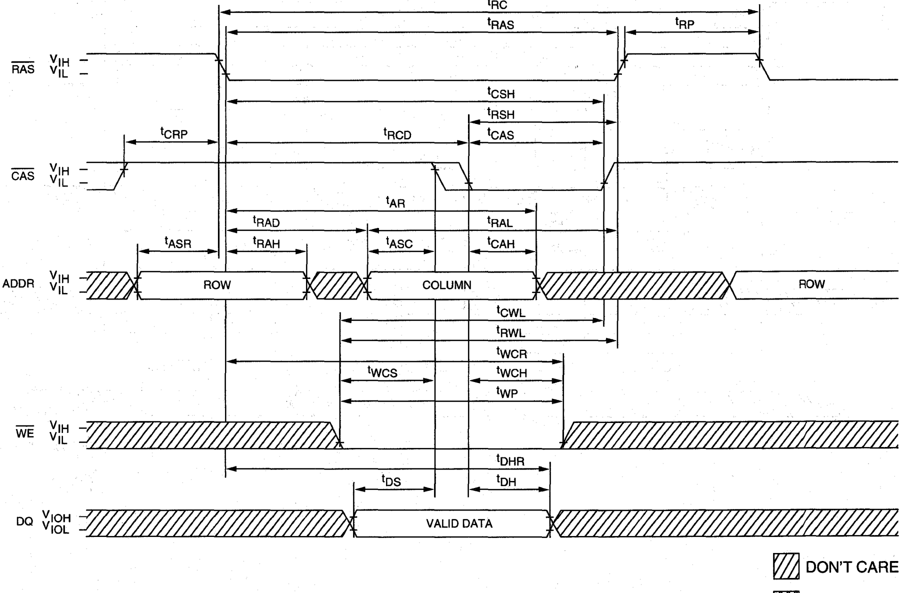
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

DRAM MODULE

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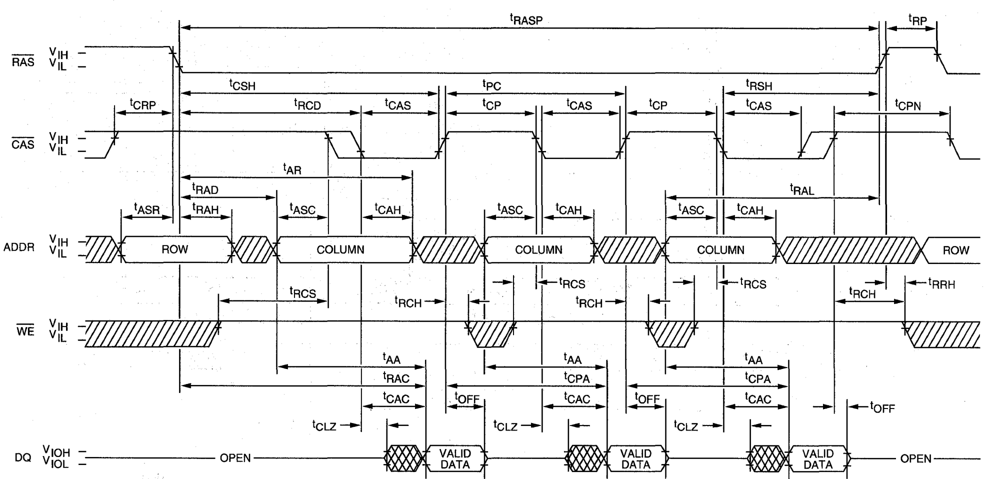
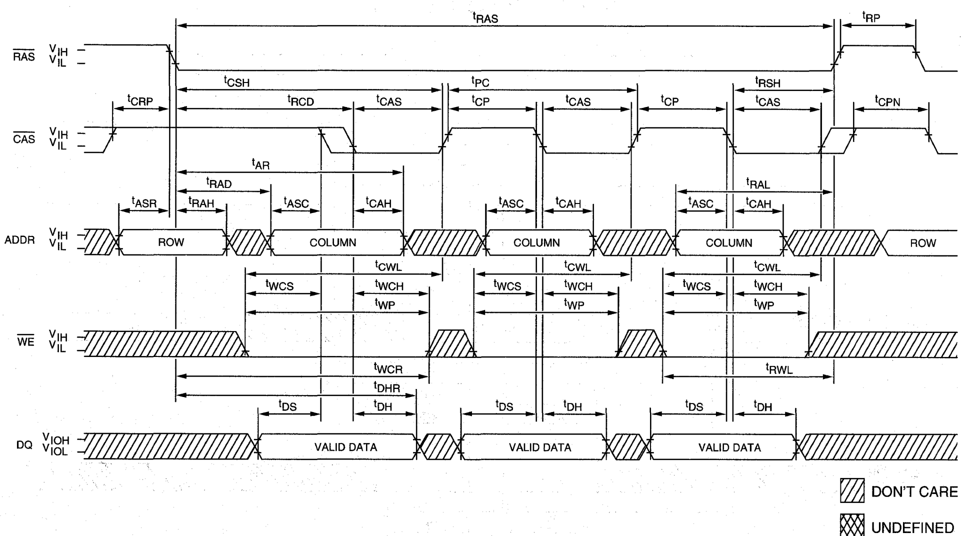
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



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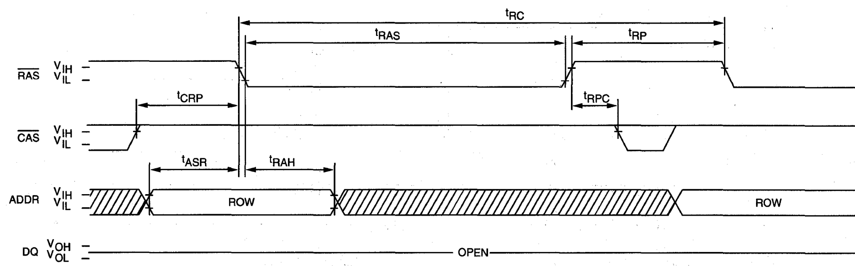
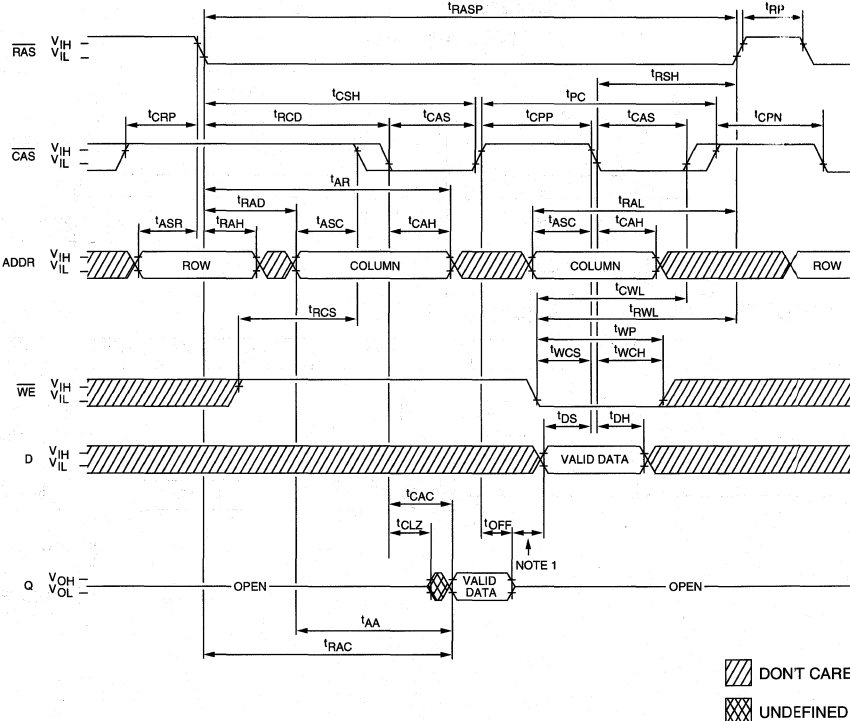
RAS ONLY REFRESH CYCLE
(ADDR = A0-A9; A10 and WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: ^{t}CPP(MIN) or ^{t}CP(whichever is greater) + ^{t}DS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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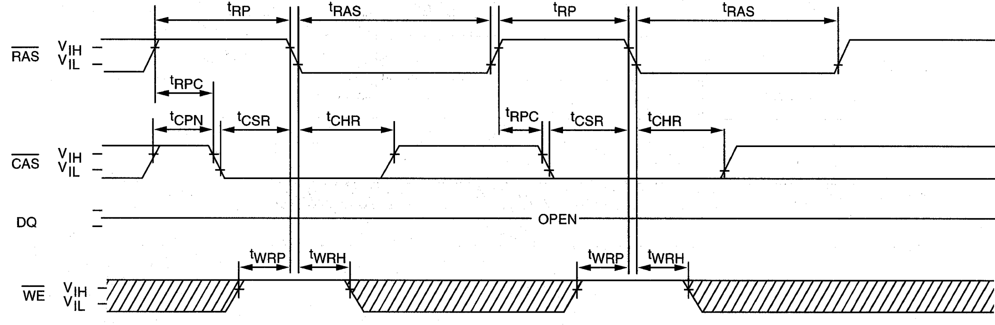
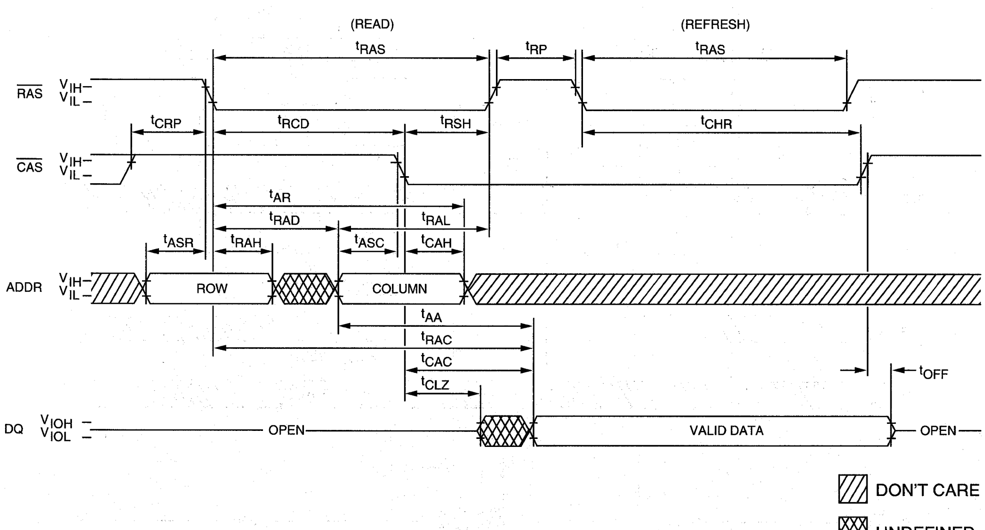
CBR REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [22]
(WE = HIGH)



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DRAM MODULE

1 MEG x 9 DRAM

FAST PAGE MODE

FEATURES

- Industry-standard pinout in a 30-pin single-in-line memory module
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 9mW standby; 625mW active, typical
- All device pins are TTL-compatible
- FAST PAGE MODE access cycle
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Low profile
- 1,024-cycle refresh distributed across 16ms

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Leadless 30-pin SIMM	M

- Part Number Example: MT3D19M-6

PIN ASSIGNMENT (Top View)

30-Pin SIMM
(DE-2)

Signal	Pin
Vcc	1
CAS	2
DQ1	3
A0	4
A1	5
DQ2	6
A2	7
A3	8
Vss	9
DQ3	10
A4	11
A5	12
DQ4	13
A6	14
A7	15
DQ5	16
A8	17
A9	18
NC	19
DQ6	20
WE	21
Vss	22
DQ7	23
NC	24
DQ8	25
Q9	26
RAS	27
CAS9	28
D9	29
Vcc	30

MT3D19M

GENERAL DESCRIPTION

The MT3D19 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, and the output pins remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms regardless of sequence.

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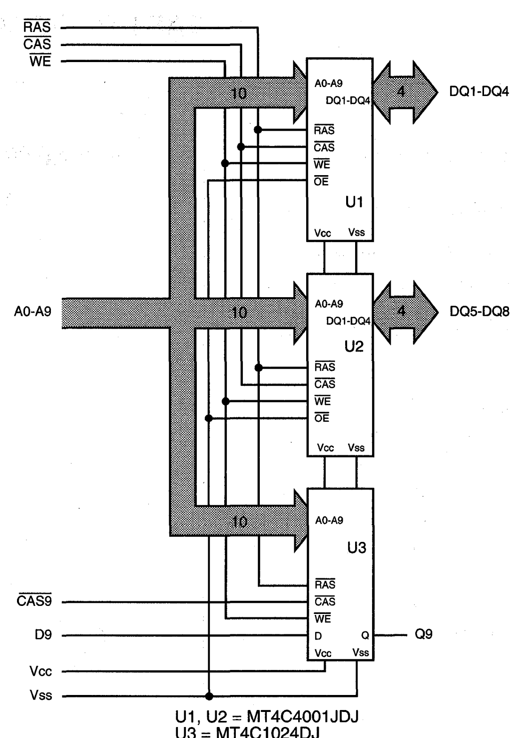
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

FUNCTION		RAS	CAS	CAS9	WE	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ8, D9, Q9
Standby		H	H→X	H→X	X	X	X	High-Z
READ		L	L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data-In
RAS ONLY REFRESH		L	H	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	L	H	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature .... -55°C to +125°C
Power Dissipation 3W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6, 7, 25) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	D9, $\overline{\text{CAS9}}$	II	-2	2	µA	
	A0-A9, $\overline{\text{RAS}}$, $\overline{\text{WE}}$	II	-6	6	µA	
OUTPUT LEAKAGE (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	DQ1-DQ8, Q9	IOZ	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low (Logic 0) Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = VIH)	ICC1	6	6	6	mA	
STANDBY CURRENT: (CMOS) ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = Vcc -0.2V)	ICC2	3	3	3	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address Cycling: tRC = tRC [MIN])	ICC3	310	280	250	mA	2, 25, 28
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{\text{RAS}}$ = VIL, $\overline{\text{CAS}}$, Address Cycling: tPC = tPC [MIN])	ICC4	230	200	170	mA	2, 25, 28
REFRESH CURRENT: $\overline{\text{RAS}}$ ONLY Average power supply current ($\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}}$ = VIH: tRC = tRC [MIN])	ICC5	310	280	250	mA	2, 28
REFRESH CURRENT: CBR Average power supply current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address Cycling: tRC = tRC [MIN])	ICC6	310	280	250	mA	2, 19

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		19	pF	17
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		25	pF	17
Input Capacitance: D9	C_{I3}		10	pF	17
Input/Output Capacitance: DQ1-DQ8	$C_{I/O}$		10	pF	17
Output Capacitance: Q9	C_O		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		n/a	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	9
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	22
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	^tRCH	0		0		0		ns	24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	24
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^tOFF	3	15	3	20	3	20	ns	12, 27
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	19
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	23
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	23
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	23
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	23

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NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ᵗREF refresh requirement is exceeded.
4. AC characteristics assume ᵗT = 5ns.
5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that ᵗRCD < ᵗRCD (MAX). If ᵗRCD is greater than the maximum recommended value shown in this table, ᵗRAC will increase by the amount that ᵗRCD exceeds the value shown.
9. Assumes that ᵗRCD ≥ ᵗRCD (MAX).
10. If $\overline{CAS}$ = VIH, data output is High-Z.
11. If $\overline{CAS}$ = VIL, data output may contain data from the last valid READ cycle.
12. ᵗOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the ᵗRCD (MAX) limit ensures that ᵗRAC (MAX) can be met. ᵗRCD (MAX) is specified as a reference point only; if ᵗRCD is greater than the specified ᵗRCD (MAX) limit, then access time is controlled exclusively by ᵗCAC.
14. Either ᵗRCH or ᵗRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ᵗCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1 and U2.
22. Operation within the ᵗRAD (MAX) limit ensures that ᵗRCD (MAX) can be met. ᵗRAD (MAX) is specified as a reference point only; if ᵗRAD is greater than the specified ᵗRAD (MAX) limit, then access time is controlled exclusively by ᵗAA.
23. ᵗWTS and ᵗWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ᵗWRP and ᵗWRH in the CBR REFRESH cycle.
24. Either ᵗRCH or ᵗRRH must be satisfied for a READ cycle.
25. Icc is dependent on cycle rates.
26. All other inputs at Vcc - 0.2V.
27. The 3ns minimum is a parameter guaranteed by design.
28. Column-address changed once each cycle.

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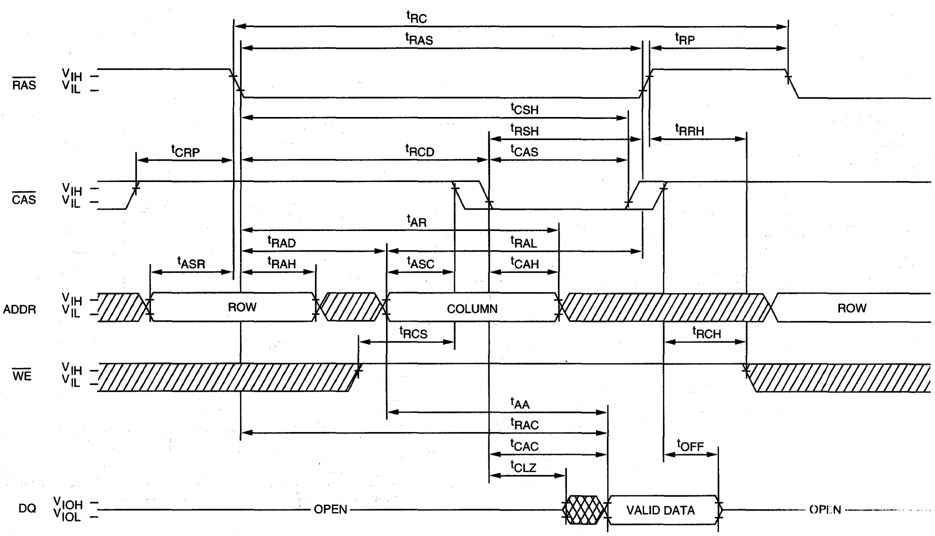
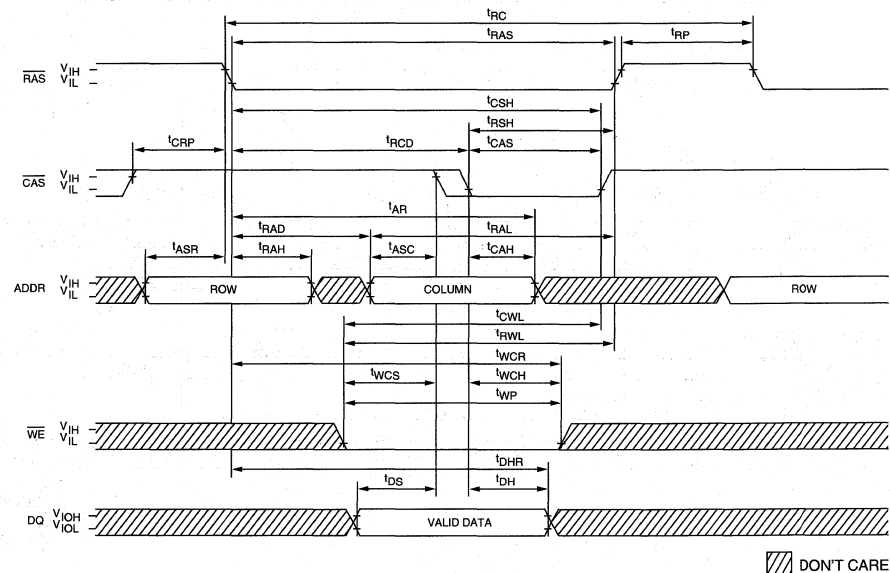
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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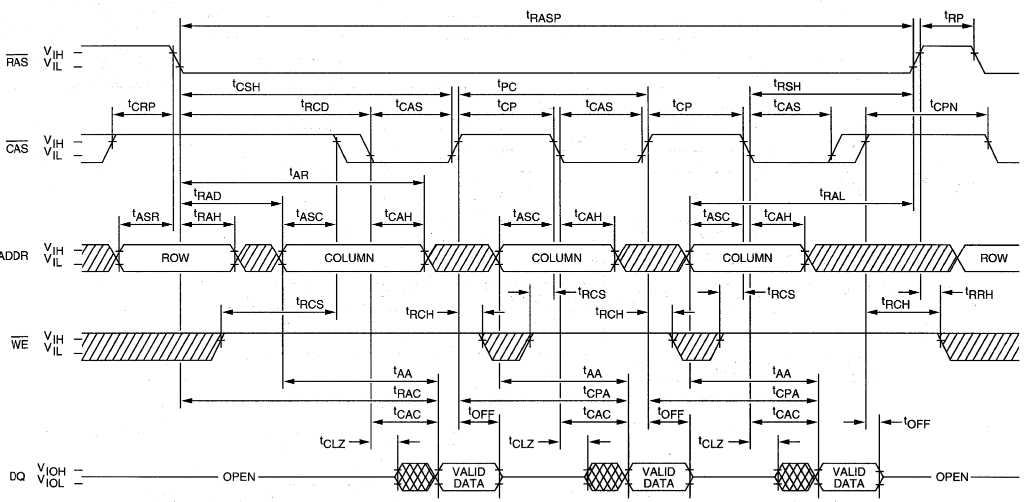
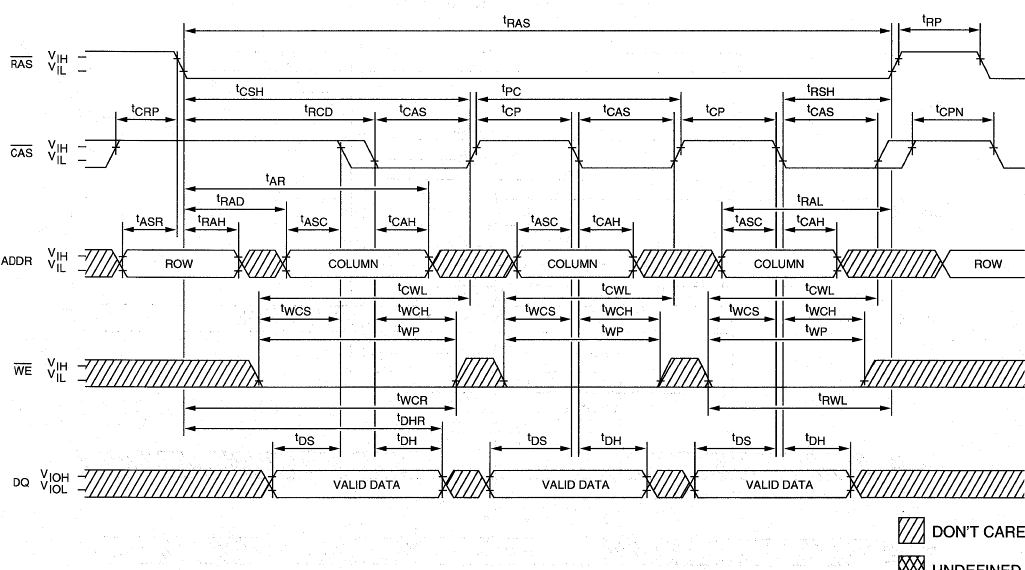
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



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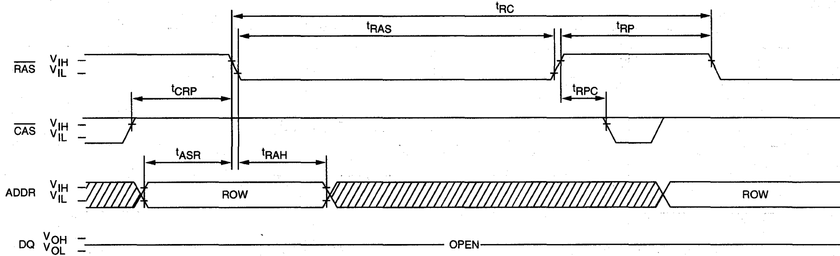
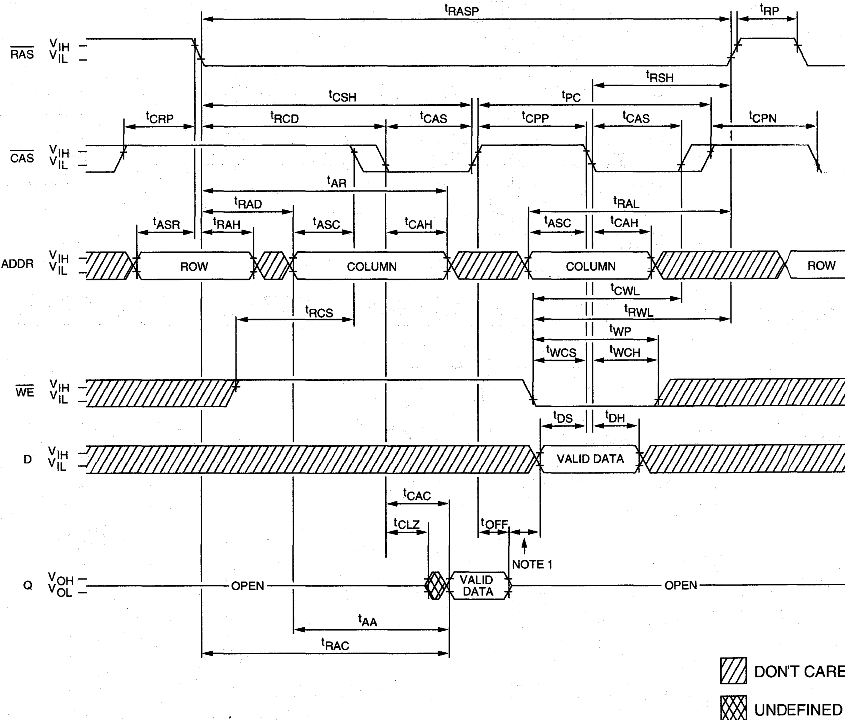
RAS ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

DRAM MODULE

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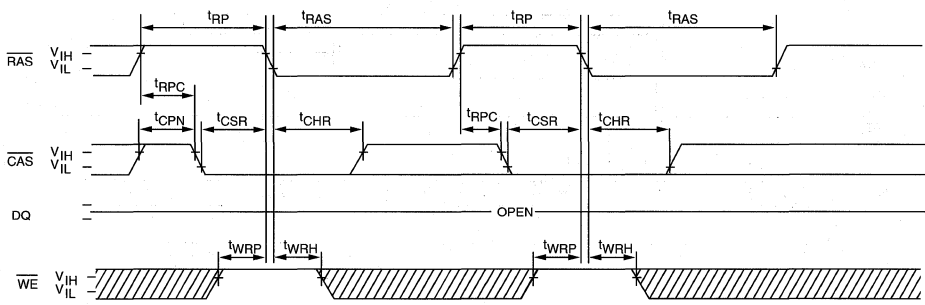
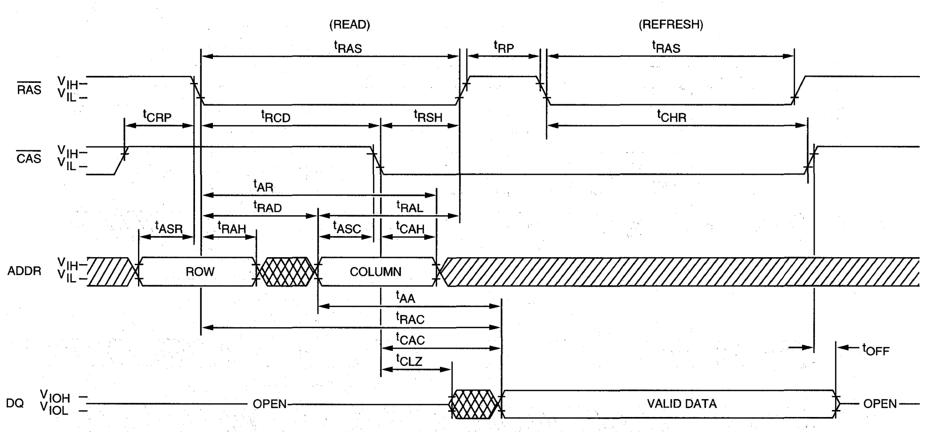
CBR REFRESH CYCLE
(A0-A9 = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



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DRAM MODULE

4 MEG x 9 DRAM

FAST PAGE MODE

FEATURES

- Industry-standard pinout in a 30-pin, single-in-line memory module
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 9mW standby; 575mW active, typical
- All device pins are TTL-compatible
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- Low profile

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
- Packages
  - Leadless 30-pin SIMM — M
- Part Number Example: MT3D49M-6

PIN ASSIGNMENT (Top View)

30-Pin SIMM
(DE-6)

Pin	Signal
1	Vcc
2	$\overline{\text{CAS}}$
3	DQ1
4	A0
5	A1
6	DQ2
7	A2
8	A3
9	Vss
10	DQ3
11	A4
12	A5
13	DQ4
14	A6
15	A7
16	DQ5
17	A8
18	A9
19	A10
20	DQ6
21	$\overline{\text{WE}}$
22	Vss
23	DQ7
24	NC
25	DQ8
26	Q9
27	$\overline{\text{RAS}}$
28	$\overline{\text{CAS9}}$
29	D9
30	Vcc

MT3D49M

GENERAL DESCRIPTION

The MT3D49 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through 22 address bits, which are entered 11 bits (A0-A10) at a time. $\overline{\text{RAS}}$ is used to latch the first 11 bits and $\overline{\text{CAS}}$ the latter 11 bits. READ or WRITE cycles are selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{CAS}}$. Since $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pins remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{\text{RAS}}$ followed by a column-address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the FAST PAGE MODE operations.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE) or $\overline{\text{RAS}}$ REFRESH cycle ($\overline{\text{RAS}}$ ONLY, CBR or HIDDEN) so that all 2,048 combinations of $\overline{\text{RAS}}$ addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{\text{RAS}}$ addressing.

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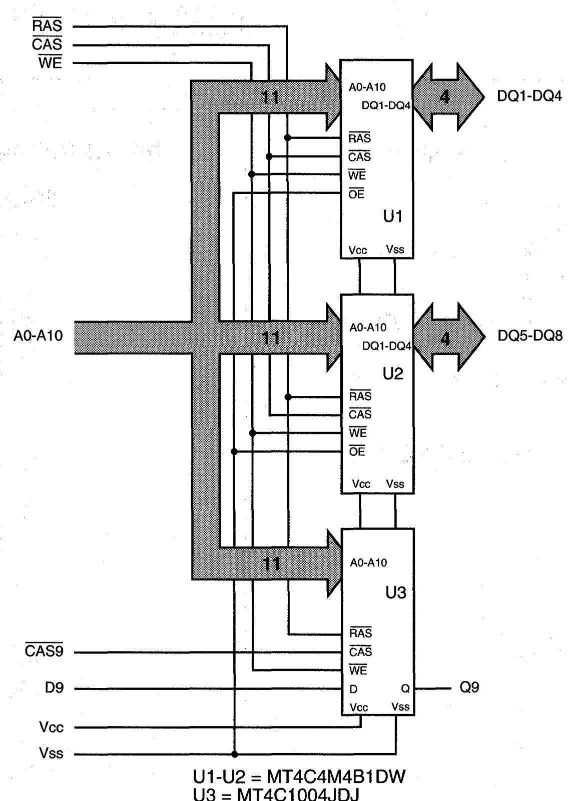
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{CAS9}$	$\overline{WE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ8, D9, Q9
Standby		H	H→X	H→X	X	X	X	High-Z
READ		L	L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	L	H	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature .... -55°C to +125°C
Power Dissipation 3W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	D9, CAS9	II	-2	2	µA	
	A0-A10, RAS, WE	II	-6	6	µA	
OUTPUT LEAKAGE (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	DQ1-DQ8, Q9	IOZ	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low (Logic 0) Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	6	6	mA	
STANDBY CURRENT: (CMOS) Average power supply current (RAS = CAS = 'Other Inputs = Vcc -0.2V)	ICC2	3	3	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS and CAS = Cycling; tRC = tRC [MIN])	ICC3	290	260	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL; CAS = Cycling; tPC = tPC [MIN])	ICC4	220	190	mA	3, 4, 26
REFRESH CURRENT: RAS ONLY (RAS = Cycling; CAS = VIH; tRC = tRC [MIN])	ICC5	290	260	mA	3, 26
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling = tRC = tRC [MIN])	ICC6	290	260	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		19	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		25	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}		10	pF	2
Input Capacitance: DQ9	C_{I3}		10	pF	2
Output Capacitance: Q9	C_O		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		ns	22
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15
Access time from column-address	^tAA		30		35	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	25
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 25
$\overline{WE}$ command setup time	^tWCS	0		0		ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
Write command pulse width	^tWP	10		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in setup time	^tDS	0		0		ns	21
Data-in hold time	^tDH	10		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	^tREF		32		32	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		ns	24

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, V_{CC} = 5V, DC bias = 2.4V at 15mV RMS).
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
22. $\overline{OE}$ is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not possible.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.

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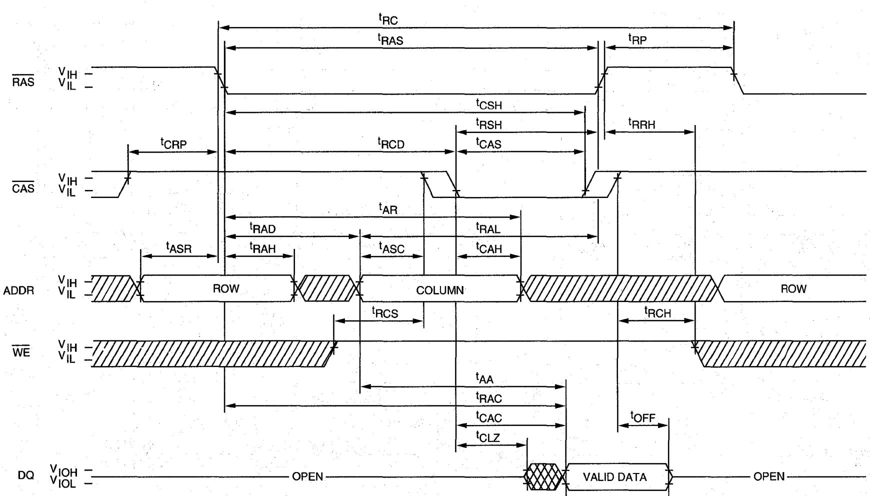
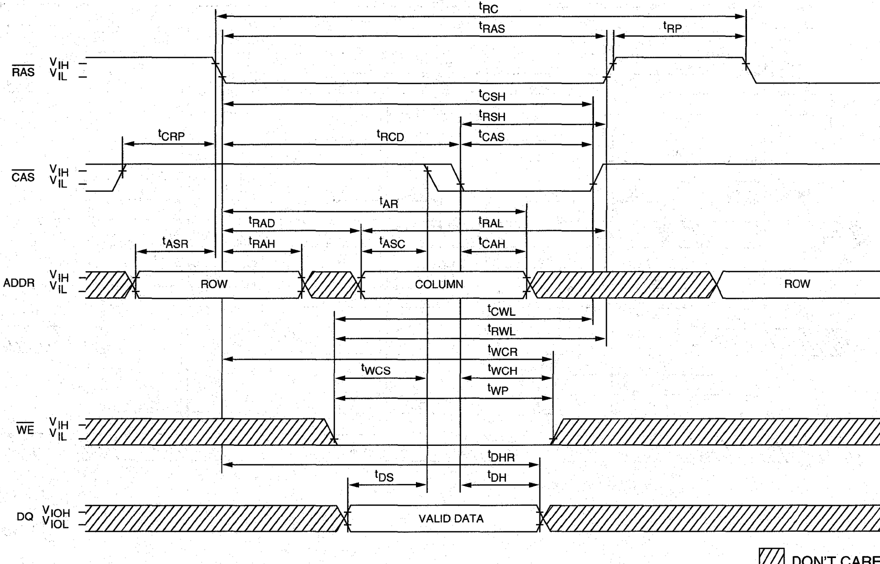
READ CYCLE



EARLY WRITE CYCLE



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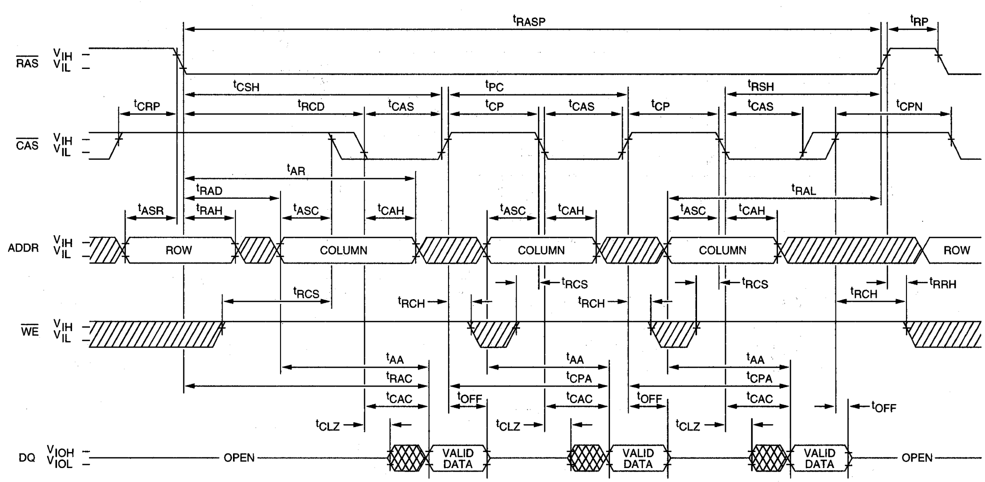
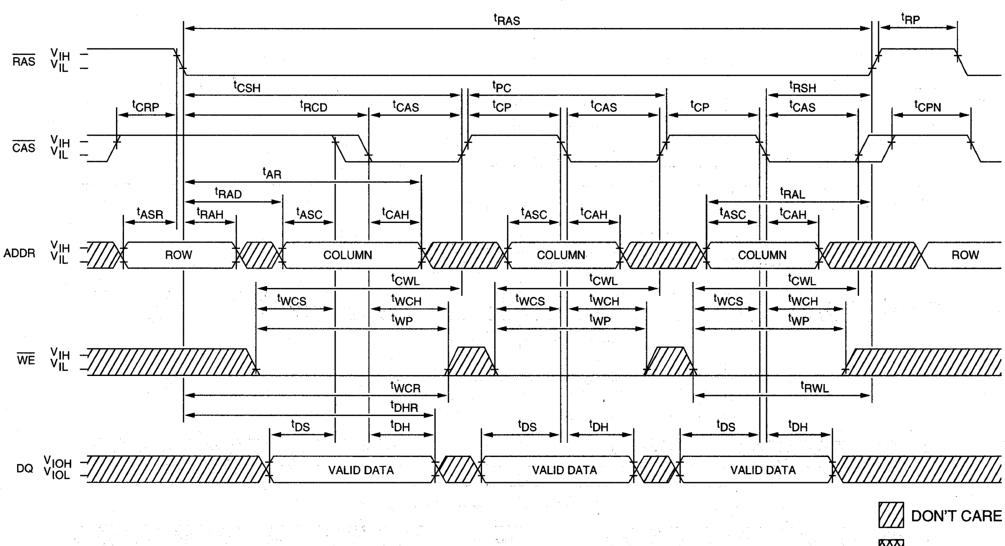
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

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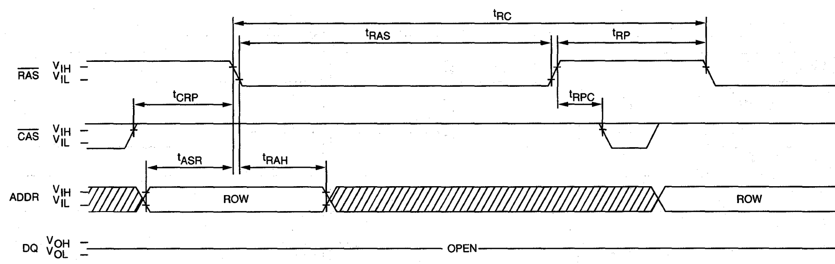
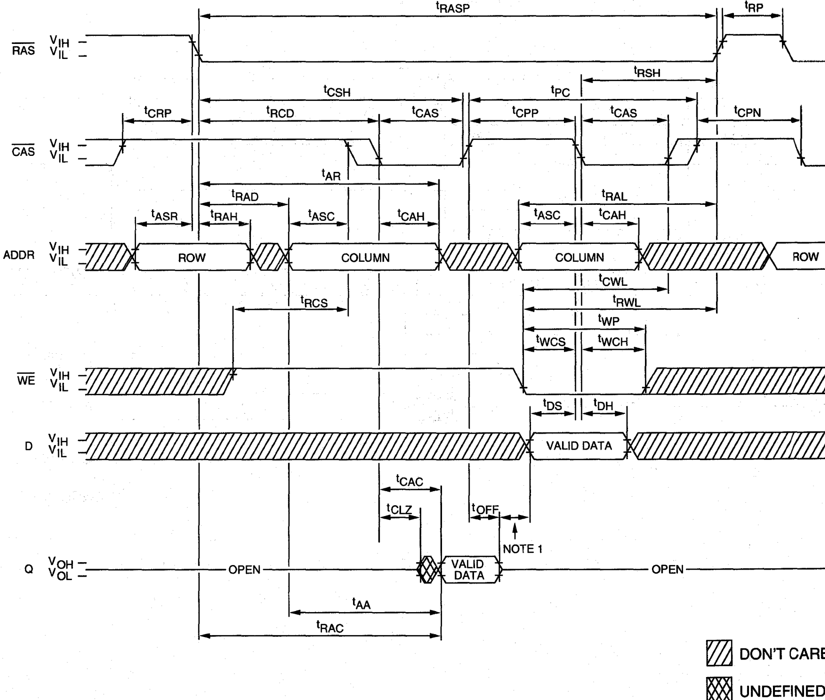
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A0-A10; $\overline{WE}$ = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: ᵗCPP(MIN) or ᵗCP(whichever is greater) + ᵗDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

DRAM MODULE

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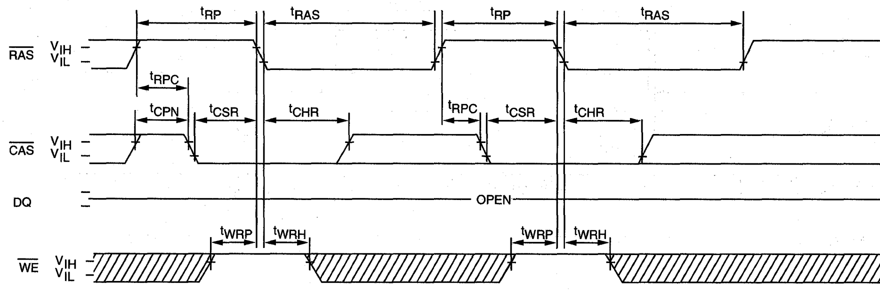
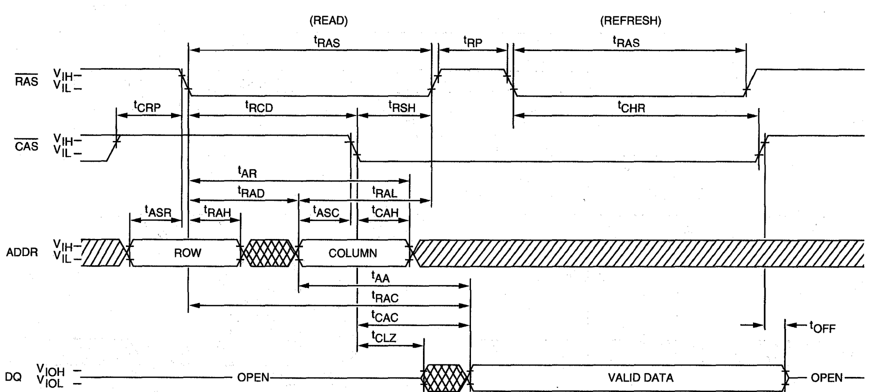
CBR REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
(WE = HIGH)



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DRAM MODULE

4 MEG x 9 DRAM
FAST PAGE MODE

FEATURES
- Industry-standard pinout in a 30-pin single-in-line package
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 27mW standby; 2,025mW active, typical
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- FAST PAGE MODE access cycle

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Leadless 30-pin SIMM	M

- Part Number Example: MT9D49M-6

PIN ASSIGNMENT (Top View)

30-Pin SIMM
(DE-4)

MT9D49M

Pin	Name	Pin	Name	Pin	Name
1	Vcc	11	A4	21	WE
2	CAS	12	A5	22	Vss
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	Q9
7	A2	17	A8	27	RAS
8	A3	18	A9	28	CAS9
9	Vss	19	*A10	29	D9
10	DQ3	20	DQ6	30	Vcc

*Address not used for RAS ONLY REFRESH

GENERAL DESCRIPTION

The MT9D49 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x9 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, and the ouput remains open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms regardless of sequence.

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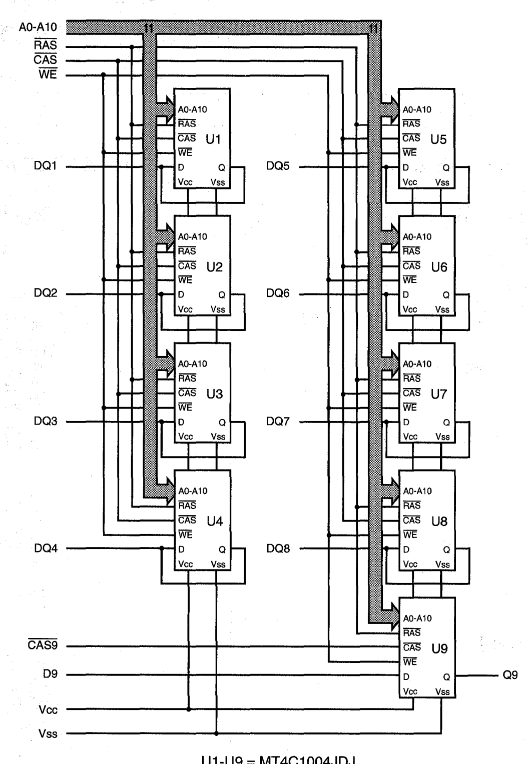
FUNCTIONAL BLOCK DIAGRAM



U1-U9 = MT4C1004JDJ

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{CAS9}$	$\overline{WE}$	ADDRESSES		DATA-IN/OUT
						${}^tR$	${}^tC$	DQ1-DQ8, D9, Q9
Standby		H	H→X	H→X	X	X	X	High-Z
READ		L	L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	L	H	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	D9, CAS9	II	-2	2	µA	
	A0-A10, WE, CAS, RAS	II	-18	18	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	Q9	IOZ	-10	10	µA	
	DQ1-DQ8	IOZ	-12	12	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	18	18	18	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	ICC2	9	9	9	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	990	900	810	mA	3, 4, 27
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])	ICC4	720	630	540	mA	3, 4, 27
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])	ICC5	990	900	810	mA	3, 27
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC6	990	900	810	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		55	pF	2
Input Capacitance: $\overline{\text{RAS}}$, $\overline{\text{WE}}$, $\overline{\text{CAS}}$	C_{I2}		73	pF	2
Input Capacitance: D9, $\overline{\text{CAS9}}$	C_{I3}		10	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}		15	pF	2
Output Capacitance: Q9	C_O		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
READ WRITE cycle time	^{t}RWC	n/a		n/a		n/a		n/a	23
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	n/a		n/a		n/a		n/a	23
Access time from $\overline{\text{RAS}}$	^{t}RAC		60		70		80	ns	14
Access time from $\overline{\text{CAS}}$	^{t}CAC		15		20		20	ns	15
Access time from column-address	^{t}AA		30		35		40	ns	
Access time from $\overline{\text{CAS}}$ precharge	^{t}CPA		35		40		45	ns	
$\overline{\text{RAS}}$ pulse width	^{t}RAS	60	100,000	70	100,000	80	100,000	ns	26
$\overline{\text{RAS}}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	26
$\overline{\text{RAS}}$ hold time	^{t}RSH	15		20		20		ns	
$\overline{\text{RAS}}$ precharge time	^{t}RP	40		50		60		ns	
$\overline{\text{CAS}}$ pulse width	^{t}CAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{\text{CAS}}$ hold time	^{t}CSH	60		70		80		ns	
$\overline{\text{CAS}}$ precharge time	^{t}CPN	10		10		10		ns	16
$\overline{\text{CAS}}$ precharge time (FAST PAGE MODE)	^{t}CP	10		10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	^{t}RCD	20	45	20	50	20	60	ns	17
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	^{t}CRP	10		10		10		ns	
Row-address setup time	^{t}ASR	0		0		0		ns	
Row-address hold time	^{t}RAH	10		10		10		ns	
$\overline{\text{RAS}}$ to column-address delay time	^{t}RAD	15	30	15	35	15	40	ns	18
Column-address setup time	^{t}ASC	0		0		0		ns	
Column-address hold time	^{t}CAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{\text{RAS}}$)	^{t}AR	45		50		55		ns	
Column-address to $\overline{\text{RAS}}$ lead time	^{t}RAL	30		35		40		ns	
Read command setup time	^{t}RCS	0		0		0		ns	
Read command hold time (referenced to $\overline{\text{CAS}}$)	^{t}RCH	0		0		0		ns	19

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	3	15	3	20	3	20	ns	20, 25
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	10		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	24

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DRAM MODULE

NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ᵗREF refresh requirement is exceeded.
8. AC characteristics assume ᵗT = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If CAS = VIH, data output is High-Z.
12. If CAS = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ᵗRCD < ᵗRCD (MAX). If ᵗRCD is greater than the maximum recommended value shown in this table, ᵗRAC will increase by the amount that ᵗRCD exceeds the value shown.
15. Assumes that ᵗRCD ≥ ᵗRCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ᵗCPN.
17. Operation within the ᵗRCD (MAX) limit ensures that ᵗRAC (MAX) can be met. ᵗRCD (MAX) is specified as a reference point only; if ᵗRCD is greater than the specified ᵗRCD (MAX) limit, then access time is controlled exclusively by ᵗCAC.
18. Operation within the ᵗRAD (MAX) limit ensures that ᵗRAC (MIN) and ᵗCAC (MIN) can be met. ᵗRAD (MAX) is specified as a reference point only; if ᵗRAD is greater than the specified ᵗRAD (MAX) limit, then access time is controlled exclusively by ᵗAA.
19. Either ᵗRCH or ᵗRRH must be satisfied for a READ cycle.
20. ᵗOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
21. These parameters are referenced to CAS leading edge in EARLY WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
23. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
24. ᵗWTS and ᵗWTH are set up and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ᵗWRP and ᵗWRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Extended refresh current is reduced as ᵗRAS is reduced from its maximum specification during the extended refresh cycle.
27. Column-address changed once each cycle.

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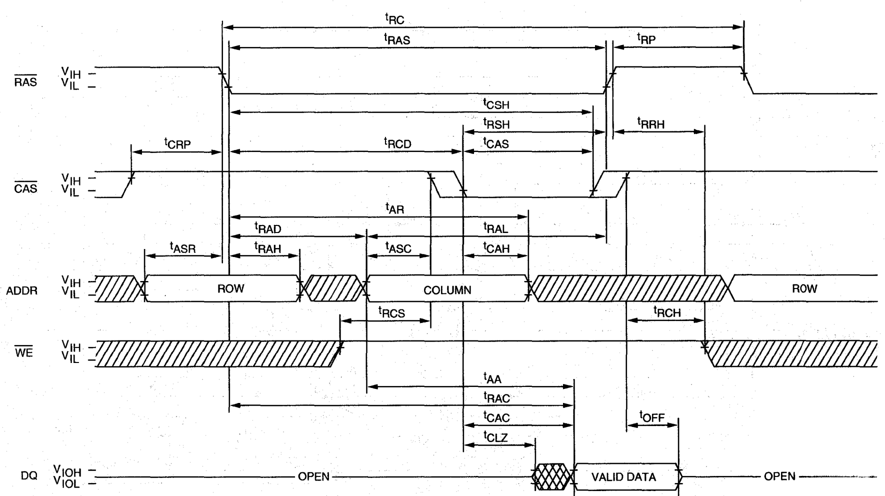
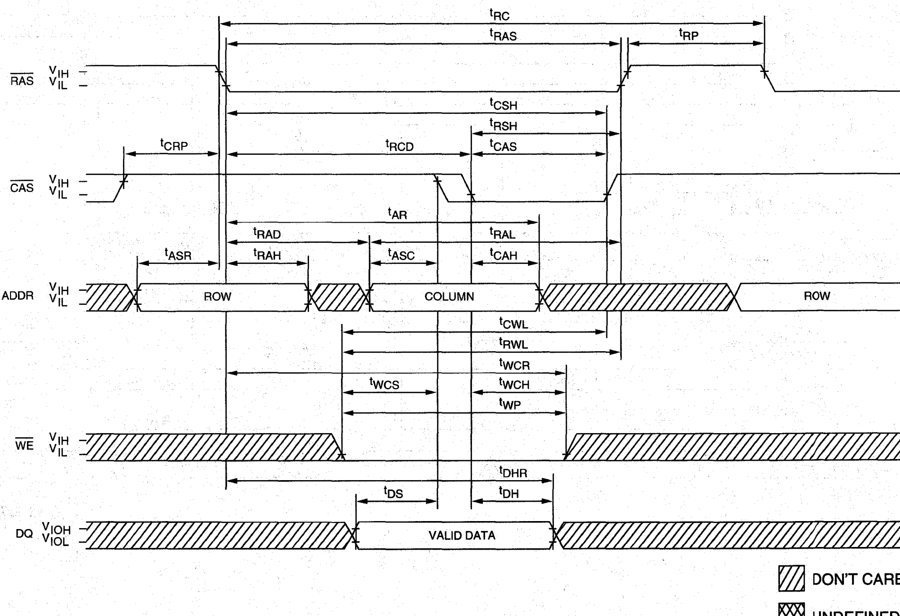
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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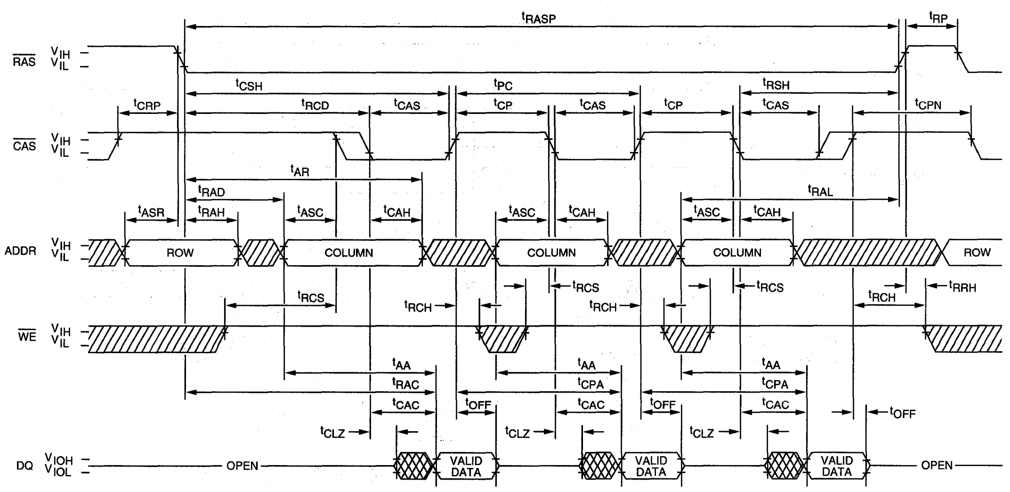
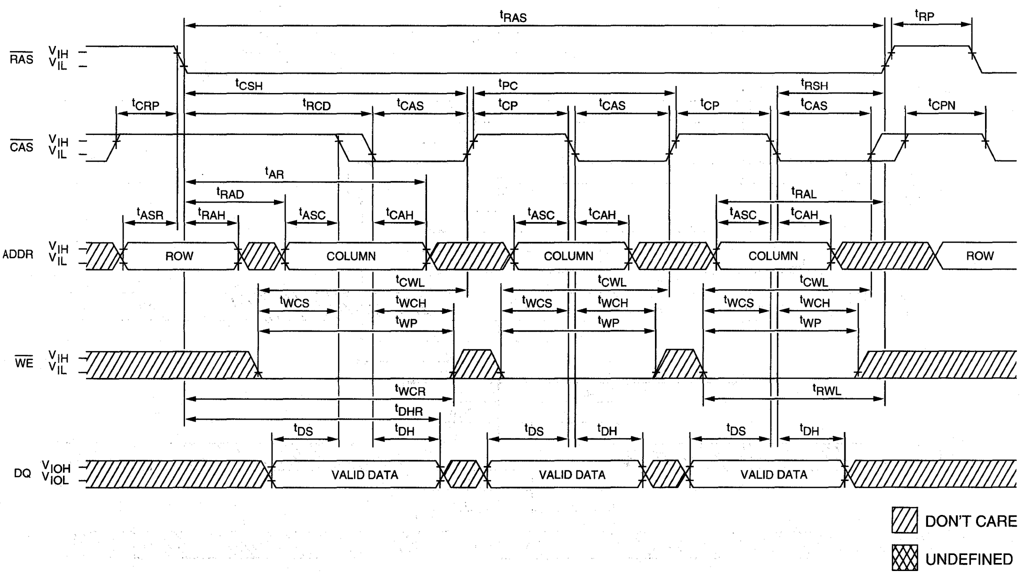
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

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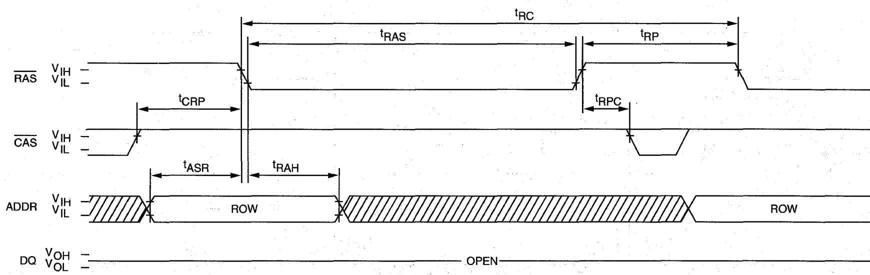
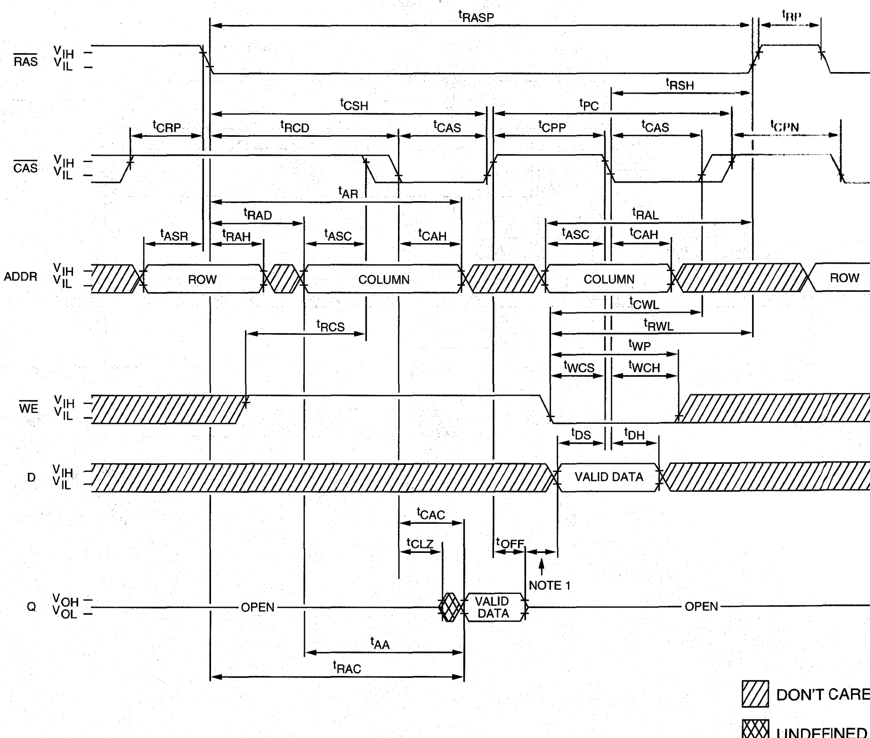
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE
(ADDR = A0-A9; A10 and $\overline{\text{WE}}$ = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

DRAM MODULE

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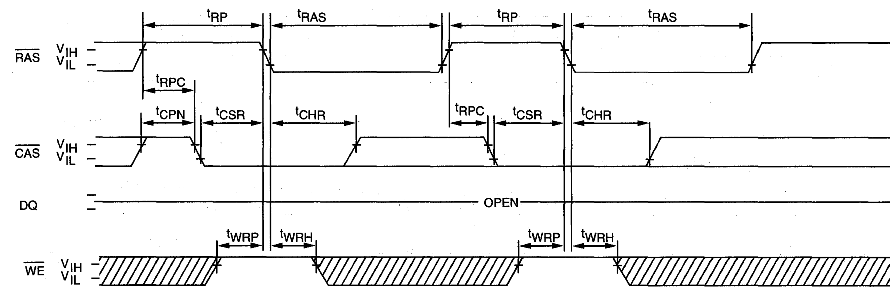
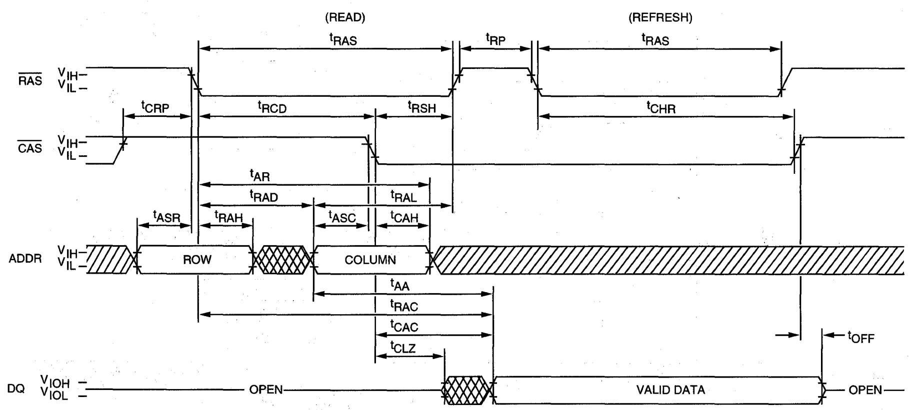
CBR REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [22]
($\overline{WE}$ = HIGH)



DON'T CARE

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DRAM MODULE

1 MEG x 32, 2 MEG x 16

FAST PAGE MODE (MT8D132)
LOW POWER, EXTENDED REFRESH (MT8D132 L)

FEATURES

- Industry-standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 24mW (6.4mW L-version) standby; 1,800mW active, typical
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR), HIDDEN; optional Extended
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE access cycle

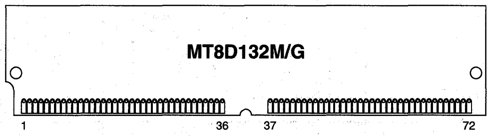
OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (gold)	G
• Power/Refresh	
Normal Power/16ms	Blank
Low Power/128ms	L

- Part Number Example: MT8D132G-6 L

PIN ASSIGNMENT (Top View)

72-Pin SIMM (DE-7)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{\text{CAS0}}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{\text{CAS2}}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{\text{CAS3}}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{\text{CAS1}}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{\text{RAS0}}$	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

GENERAL DESCRIPTION

The MT8D132 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{\text{RAS}}$ is used to latch the first 10 bits and $\overline{\text{CAS}}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{\text{RAS}}$ followed by a column-address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE) or $\overline{\text{RAS}}$ REFRESH cycle ($\overline{\text{RAS}}$ ONLY, CBR or HIDDEN) so that all 1,024 combinations of $\overline{\text{RAS}}$ addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

For x16 applications, the corresponding DQ and $\overline{\text{CAS}}$ pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and $\overline{\text{CAS0}}$ to $\overline{\text{CAS2}}$ and $\overline{\text{CAS1}}$ to $\overline{\text{CAS3}}$). Each $\overline{\text{RAS}}$ is then a bank select for the x16 memory organization.

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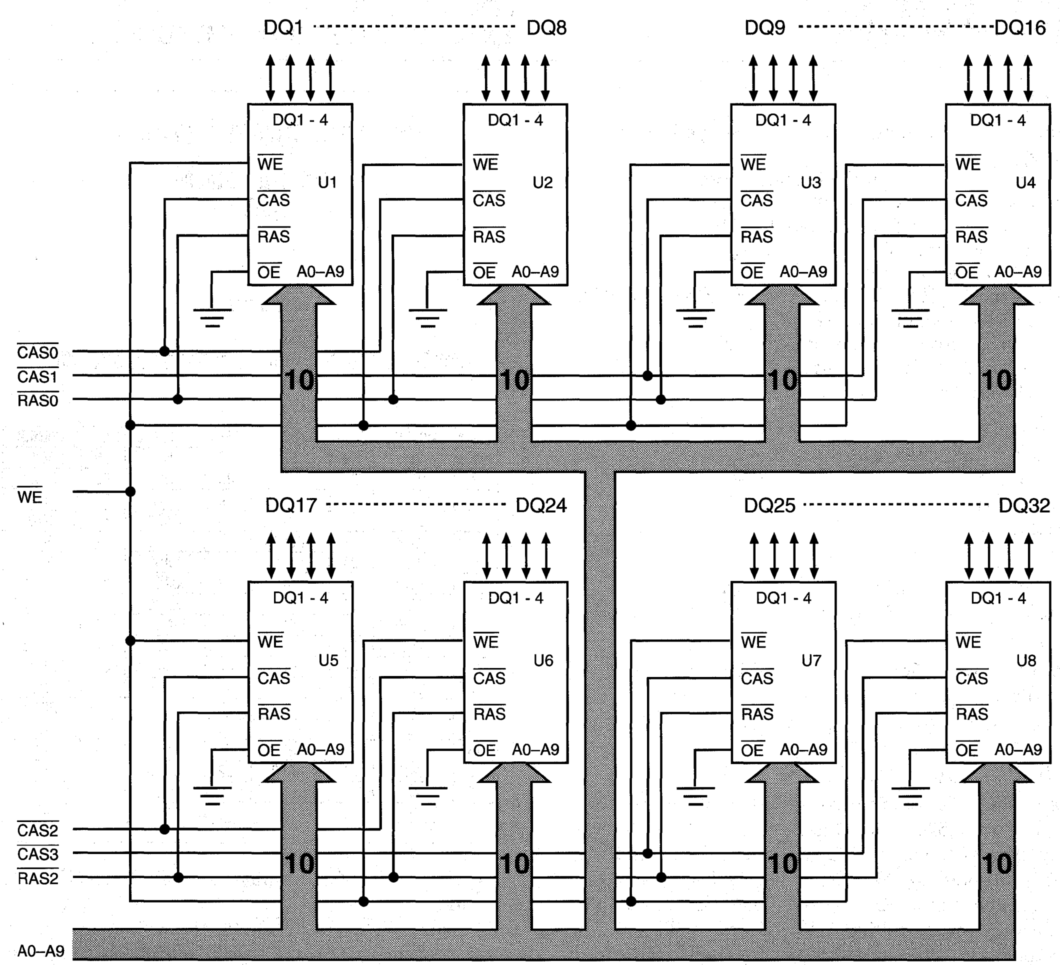
FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4001JDJ
U1-U8 = MT4C4001JDJ S (L-version)

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES		DATA-IN/OUT
					^tR	^tC	DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
Extended CBR REFRESH (L-version)		H→L	L	H	X	X	High-Z

PRESENCE-DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

DRAM MODULE

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6, 22) (V_{CC} = 5V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{RAS0}$, $\overline{RAS2}$	I_{I1}	-8	8	µA	
Any input 0V ≤ V_{IN} ≤ 6.5V	A0-A9, $\overline{WE}$	I_{I2}	-16	16	µA	
(All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS3}$	I_{I3}	-4	4	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ1-DQ32	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16	16	16	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	8	8	8	mA	
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		1.6	1.6	1.6	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	880	800	720	mA	2, 22, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	640	560	480	mA	2, 22, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	880	800	720	mA	22, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	880	800	720	mA	19, 22
REFRESH CURRENT: Extended CBR Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	2.4	2.4	2.4	mA	19, 22, 24

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		51	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		67	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		32	pF	17
Input Capacitance: $\overline{CAS1}$, $\overline{CAS0}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		16	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
READ WRITE cycle time	^{t}RWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^{t}RAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^{t}CAC		15		20		20	ns	9
Access time from column-address	^{t}AA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^{t}RSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^{t}RP	40		50		60		ns	
$\overline{CAS}$ pulse width	^{t}CAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^{t}CSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^{t}CPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^{t}CP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	10		10		10		ns	
Row-address setup time	^{t}ASR	0		0		0		ns	
Row-address hold time	^{t}RAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	30	15	35	15	40	ns	23
Column-address setup time	^{t}ASC	0		0		0		ns	
Column-address hold time	^{t}CAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	45		50		55		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		40		ns	
Read command setup time	^{t}RCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		0		ns	14

DRAM MODULE

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	tOFF	3	15	3	20	3	20	ns	12, 25
WE command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	tREF		16/128*		16/128*		16/128*	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CBR REFRESH)	tCSR	10		10		10		ns	19
CAS hold time (CBR REFRESH)	tCHR	10		10		10		ns	19
WE hold time (CBR REFRESH)	tWRH	10		10		10		ns	27
WE setup time (CBR REFRESH)	tWRP	10		10		10		ns	27
WE hold time (WCBR test cycle)	tWTH	10		10		10		ns	27
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	27

*L-version only

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NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U8.
22. I_{CC} is dependent on cycle rates.
23. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
24. Applies to L-version only.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.
27. Extended refresh current is reduced as ^{t}RAS is reduced from its maximum specification during the extended refresh cycle.

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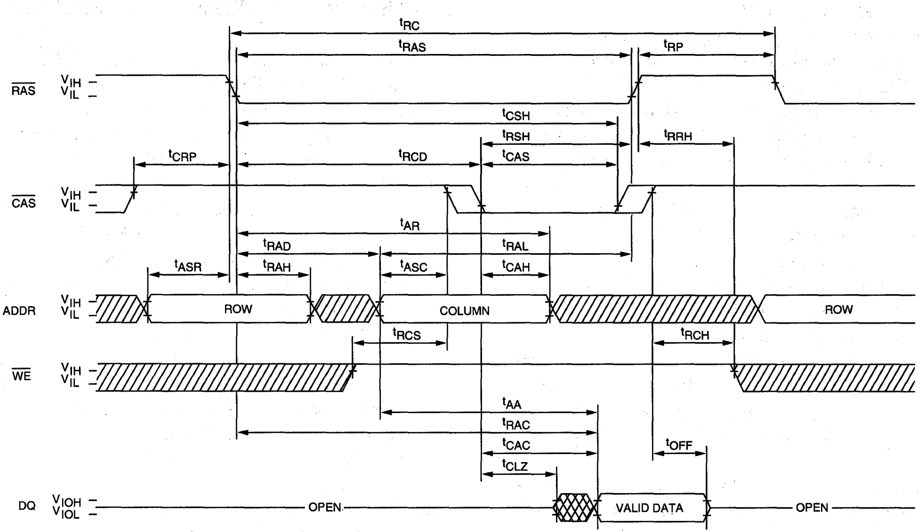
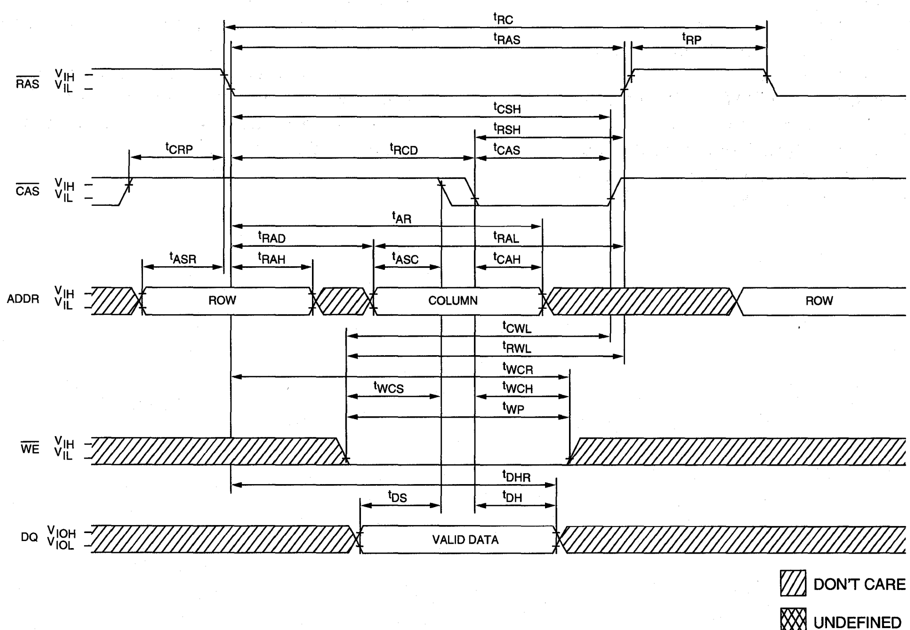
READ CYCLE



EARLY WRITE CYCLE



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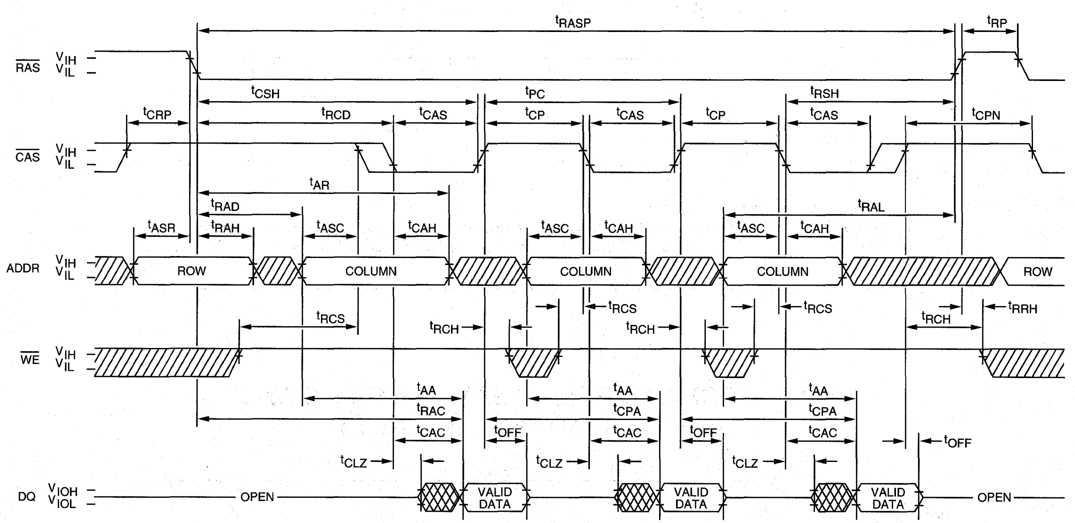
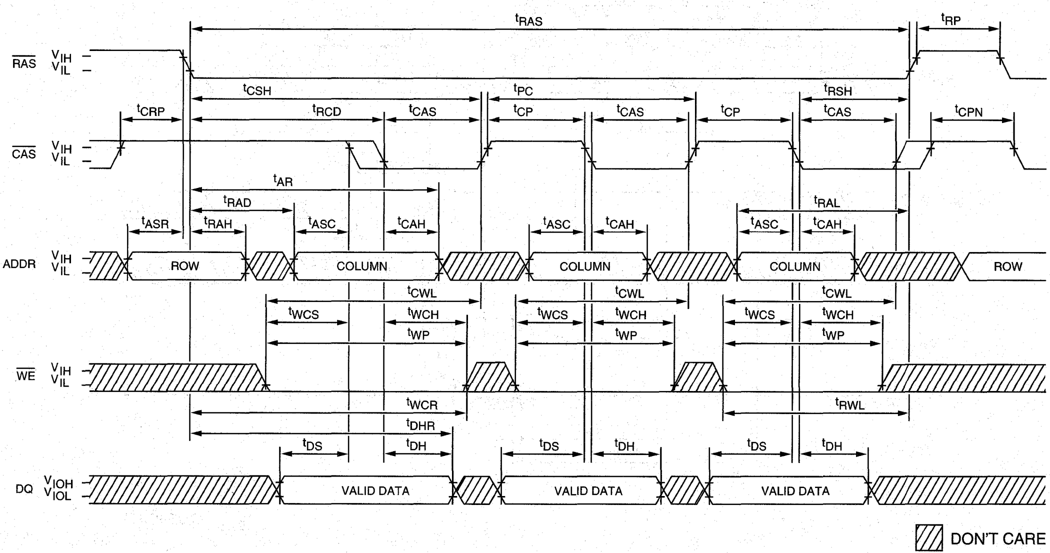
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



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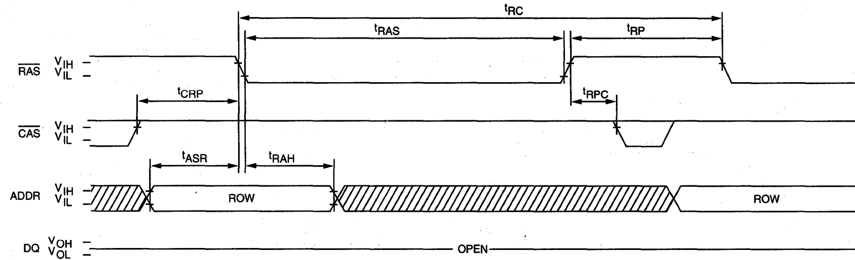
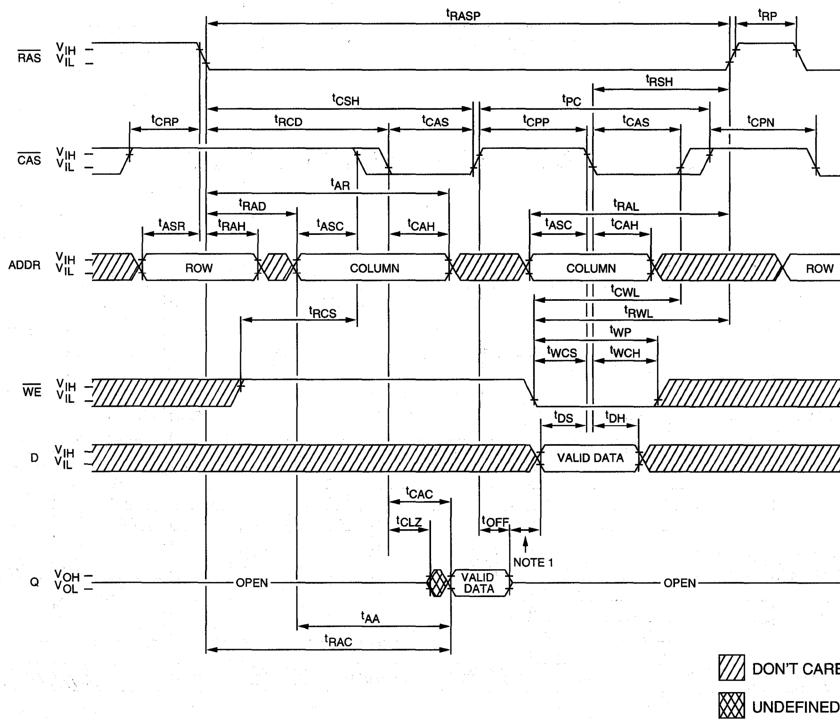
RAS ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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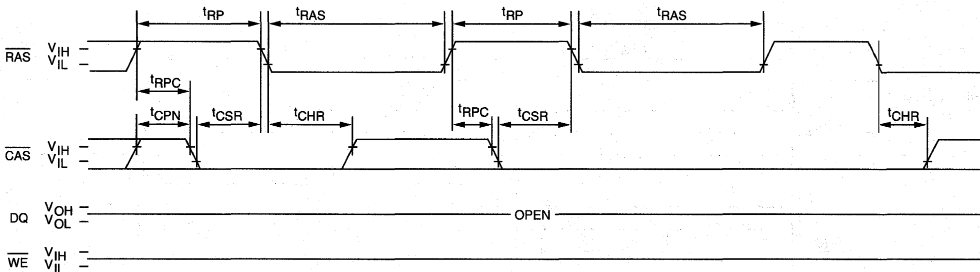
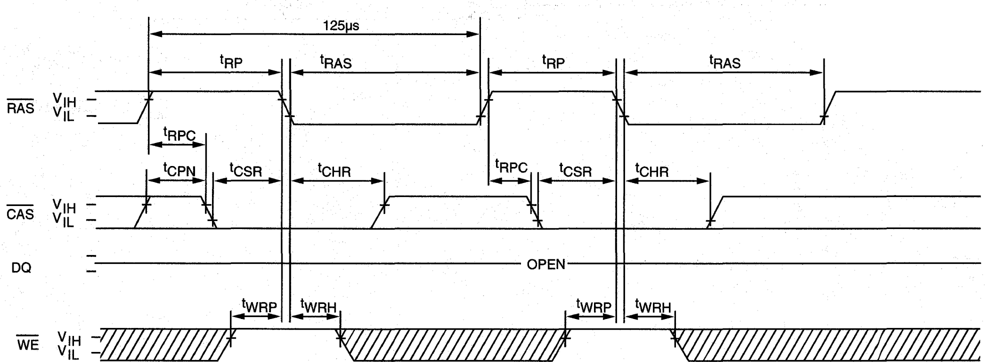
CBR REFRESH CYCLE
(A0-A9 = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [24]
(A0-A9 = DON'T CARE)



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DRAM MODULE

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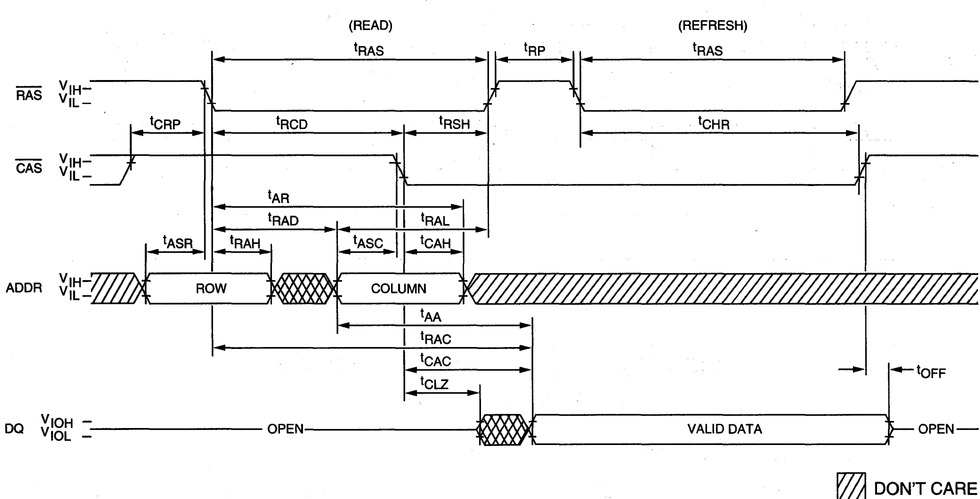
DRAM MODULE

HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



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DRAM MODULE

1 MEG, 2 MEG x 32

4, 8 MEGABYTE, 3.3V, FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- Industry-standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon-gate process
- Single +3.3V ±.3V power supply
- All device pins are TTL-compatible
- Low power, 1.6mW standby; 1,440mW active, typical
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN; optional Extended and SELF REFRESH modes
- Multiple RAS lines allow x16 or x32 width
- 1,024-cycle Extended Refresh distributed across 16ms or 128ms
- FAST PAGE MODE access cycle

OPTIONS MARKING

- Timing
  - 60ns access -6
  - 70ns access -7
  - 80ns access -8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (gold) G
- Refresh
  - Standard Blank
  - Low-power Extended Refresh, SELF REFRESH S
- Part Number Example: MT16LD232G-6 S

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(DE-7) 1 Meg x 32
(DE-8) 2 Meg x 32

1 36 37 72

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	NC*/RAS1	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC*/RAS3	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

*4MB version only

GENERAL DESCRIPTION

The MT8LD132(S) and MT16LD232(S) are randomly accessed 4MB and 8MB solid-state memories organized in a x32 configuration. They are specially processed to operate from 3.0V to 3.6V for low voltage memory systems. The modules have optional FAST PAGE MODE, which allows faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary.

The wider voltage range on these modules allows them to be used in 3.3V ±.3V memory designs. The refresh period is also extended from the standard 16ms to 128ms to provide maximum power savings. An optional SELF REFRESH cycle allows the module to perform the extended refresh by itself. This eliminates the need to toggle the RAS clock during a sleep mode.

During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS latches the first 10 bits and CAS latches the latter 10 bits.

READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) with lower power consumption within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address

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strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on "S" option), regardless of sequence. The CBR and SELF REFRESH cycles will invoke the internal refresh counter for automatic RAS addressing.

An additional SELF REFRESH mode is also available. The "S" option allows the user the option of a fully static low power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms. The module's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding RAS LOW for the specified ^tRASS. Additionally, the "S" option allows for an extended refresh period of 128ms, or 125ms per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum ^tRPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

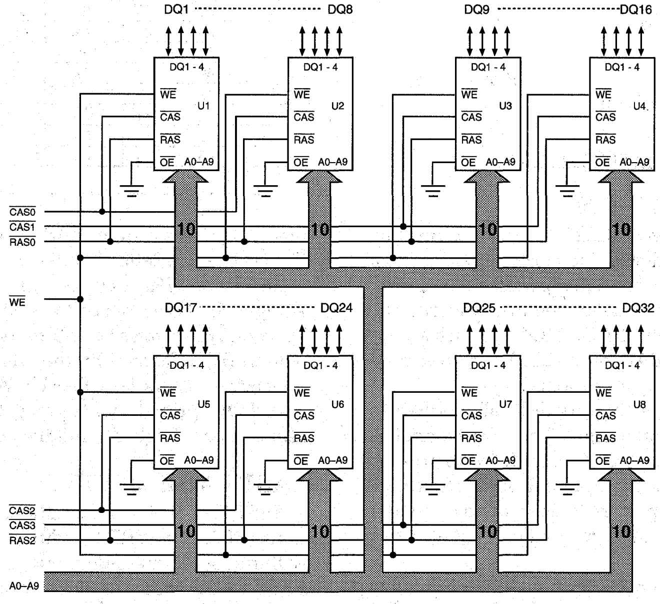
STANDBY

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time.

x16 OPERATION

For x16 applications, the corresponding DQ and CAS pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x16 memory organization.

FUNCTIONAL BLOCK DIAGRAM
4MB



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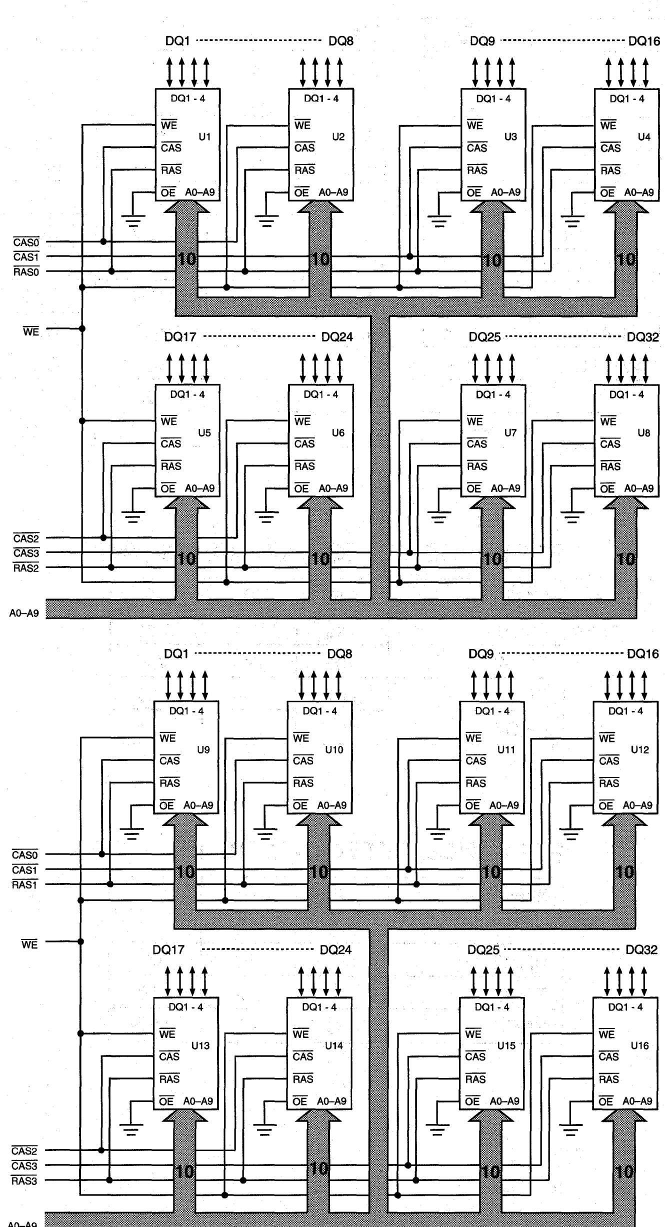
FUNCTIONAL BLOCK DIAGRAM
8MB



U1-U16 = MT4LC4001J (S)

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TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES ᵗR	ADDRESSES ᵗC	DATA-IN/OUT DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	High-Z

PRESENCE-DETECT - MT8LD132 (4MB)

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

PRESENCE-DETECT - MT16LD232 (8MB)

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (Vcc = +3.0V to 3.6V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	II1	-8	8	µA	
Any input 0V ≤ VIN ≤ Vcc+0.5V	A0-A9, $\overline{WE}$	II2	-32	32	µA	
(All other pins not under test = 0V) for each package input	$\overline{RAS0}$-$\overline{RAS3}$	II3	-8	8	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ Vcc+0.5V) for each package input	DQ1-DQ32	IOZ	-20	20	µA	
TTL OUTPUT LEVELS High Voltage (IOUT = -2mA)		VOH	2.4		V	
Low Voltage (IOUT = 2mA)		VOL		0.4	V	

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NEW DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 22) (0°C ≤ T_A ≤ 70°C; Vcc = 3.0V to 3.6V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	4MB 8MB	8 16	8 16	8 16	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = Vcc -0.2V)	I_{CC2}	4MB 8MB	4 8	4 8	4 8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	4MB 8MB	640 648	560 568	480 488	mA	2, 22, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	4MB 8MB	480 488	400 408	320 328	mA	2, 22, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	4MB 8MB	640 648	560 568	480 488	mA	22, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	4MB 8MB	640 648	560 568	480 488	mA	22, 19
REFRESH CURRENT: Extended (S only) Average power supply current $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$, A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	4MB 8MB	1.2 2.0	1.2 2.0	1.2 2.0	mA	2, 19 22, 25
REFRESH CURRENT: SELF (S only) Average power supply current during SELF REFRESH: CBR cycle with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc -0.2V; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	4MB 8MB	1.2 2.0	1.2 2.0	1.2 2.0	mA	19

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CAPACITANCE

PARAMETER	SYMBOL	MAX 4MB	MAX 8MB	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	48	95	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}	64	127	pF	17
Input Capacitance: $\overline{RAS0}$-$\overline{RAS3}$	C_{I3}	32	32	pF	17
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$	C_{I4}	16	32	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}	10	10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (V_{CC} = 3.0 to 3.6V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		45		ns	
Access time from $\overline{RAS}$	^{t}RAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^{t}CAC		15		20		20	ns	9
Access time from column-address	^{t}AA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^{t}RSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^{t}RP	40		50		60		ns	
$\overline{CAS}$ pulse width	^{t}CAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^{t}CSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^{t}CPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^{t}CP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	10		10		10		ns	
Row-address setup time	^{t}ASR	0		0		0		ns	
Row-address hold time	^{t}RAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	30	15	35	15	40	ns	23
Column-address setup time	^{t}ASC	0		0		0		ns	
Column-address hold time	^{t}CAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	45		50		55		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		40		ns	
Read command setup time	^{t}RCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		0		ns	14
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	3		3		3		ns	

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NEW ■ DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = 3.0V to 3.6V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	tOFF	3	15	3	20	3	20	ns	12, 24
WE command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	tREF		16/128*		16/128*		16/128*	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CBR REFRESH)	tCSR	10		10		10		ns	19
CAS hold time (CBR REFRESH)	tCHR	10		10		10		ns	19
WE hold time (CBR REFRESH)	tWRH	10		10		10		ns	28
WE setup time (CBR REFRESH)	tWRP	10		10		10		ns	28
WE hold time (WCBR test cycle)	tWTH	10		10		10		ns	28
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	28
RAS pulse width during SELF REFRESH cycle	tRASS	100		100		100		ms	27
RAS precharge time during SELF REFRESH cycle	tRPS	110		130		150		ns	27
RAS LOW to "don't care" during SELF REFRESH cycle	tCHD	10		10		10		ns	27

*S-version only

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NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF. Output reference voltages are 0.8V for a low level and 2.0V for a high level.
8. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
10. If $\overline{CAS}$ = VIH, data output is High-Z.
11. If $\overline{CAS}$ = VIL, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
17. This parameter is sampled. Vcc = 3.0V ±0.3V; f = 1 MHz.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U16.
22. Icc is dependent on cycle rates.
23. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
24. The 3ns minimum is a parameter guaranteed by design.
25. Refresh current increases if ^{t}RAS is extended beyond its minimum specification.
26. Column-address changed once each cycle.
27. If the DRAM controller uses a BURST REFRESH, a BURST REFRESH of all rows must be executed upon exiting SELF REFRESH.
28. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.

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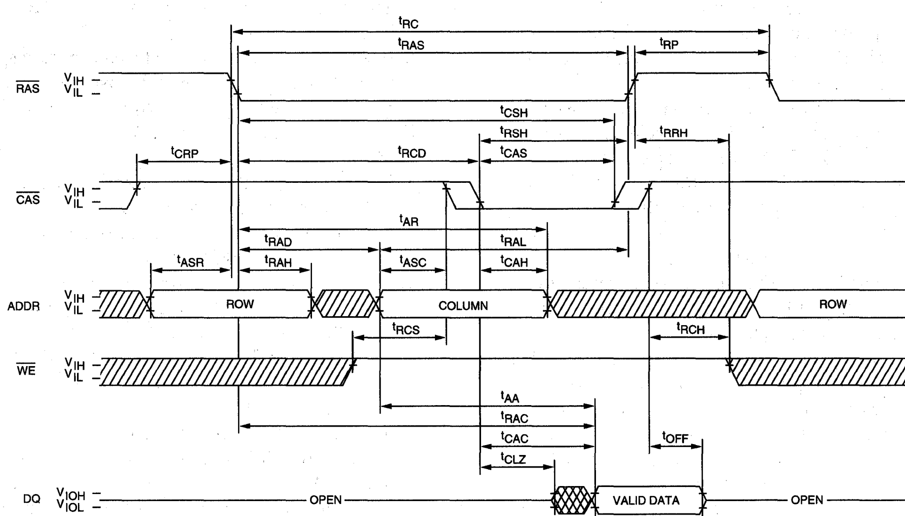
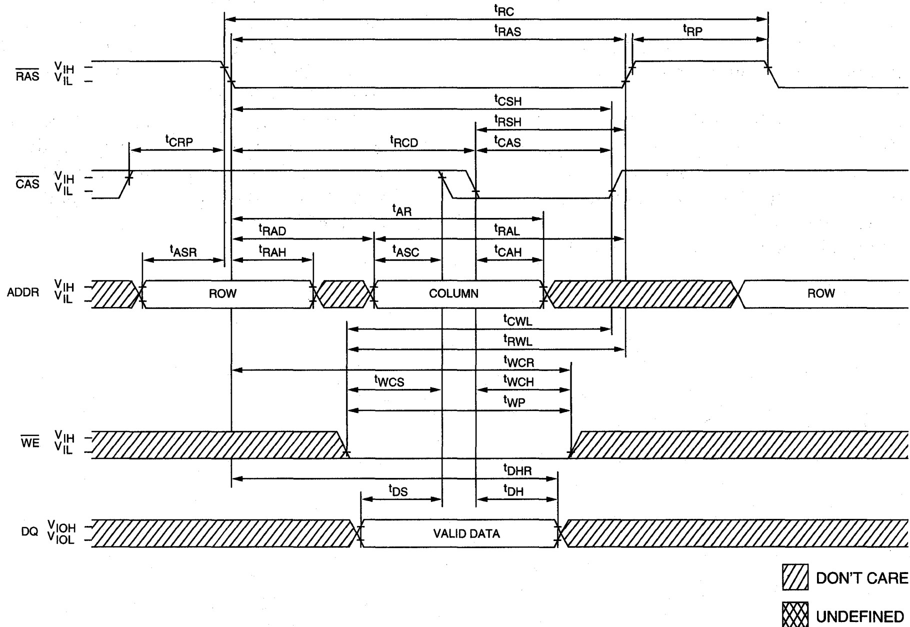
READ CYCLE



EARLY WRITE CYCLE



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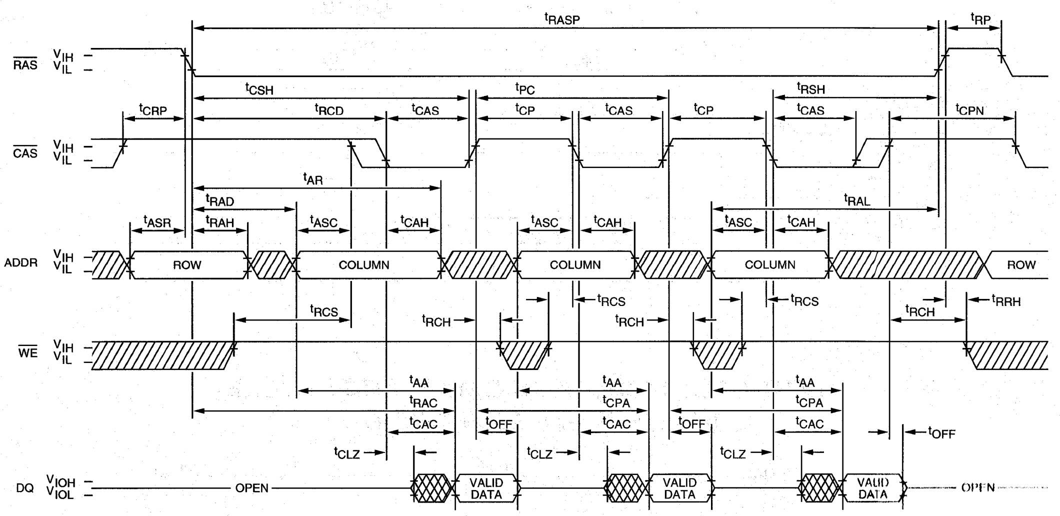
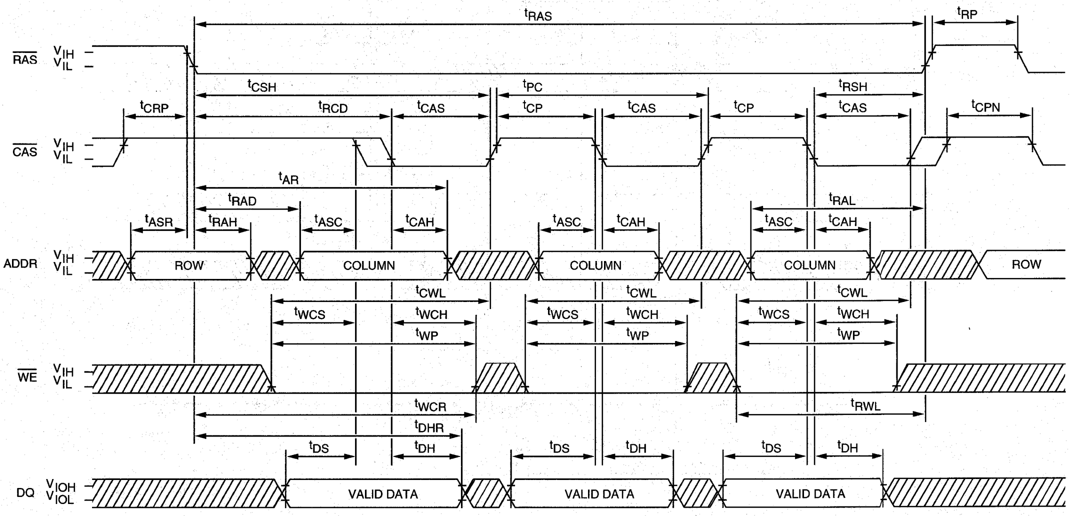
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



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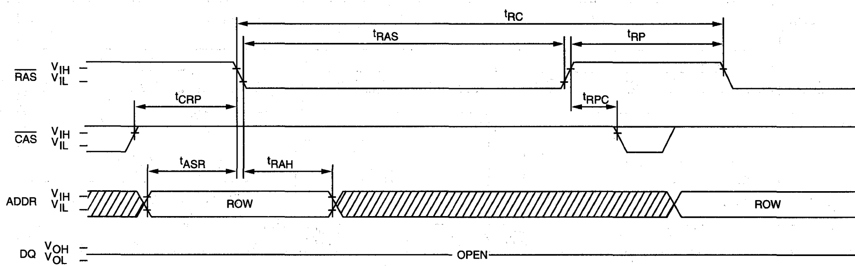
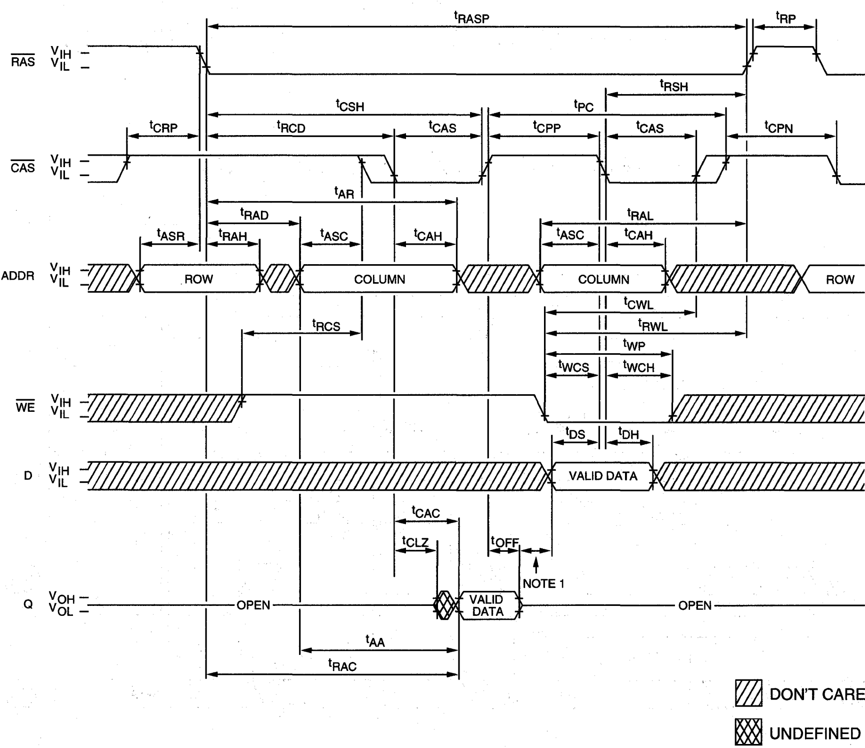
RAS ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: ^{t}CPP(MIN) or ^{t}CP(whichever is greater) + ^{t}DS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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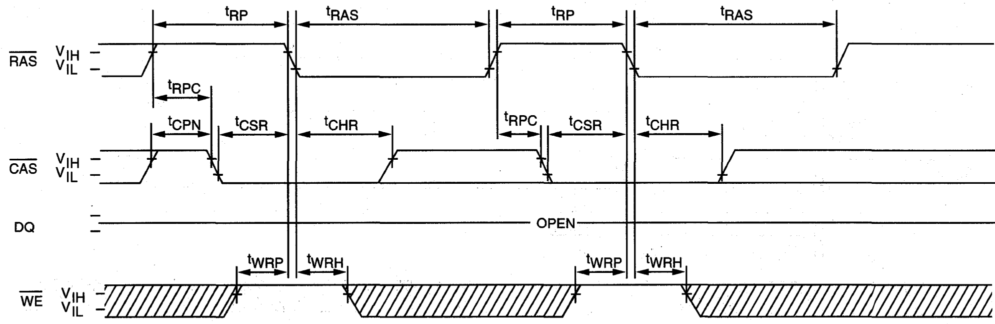
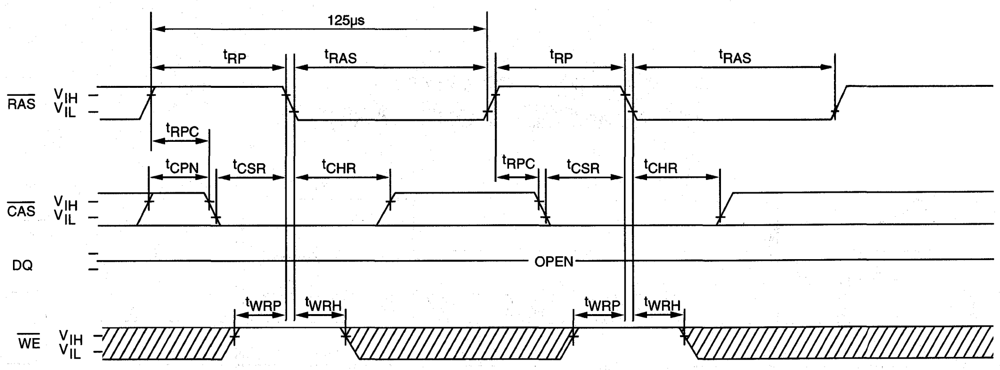
CBR REFRESH CYCLE
(A0-A9 = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [24]
(A0-A9 = DON'T CARE)



DON'T CARE

UNDEFINED

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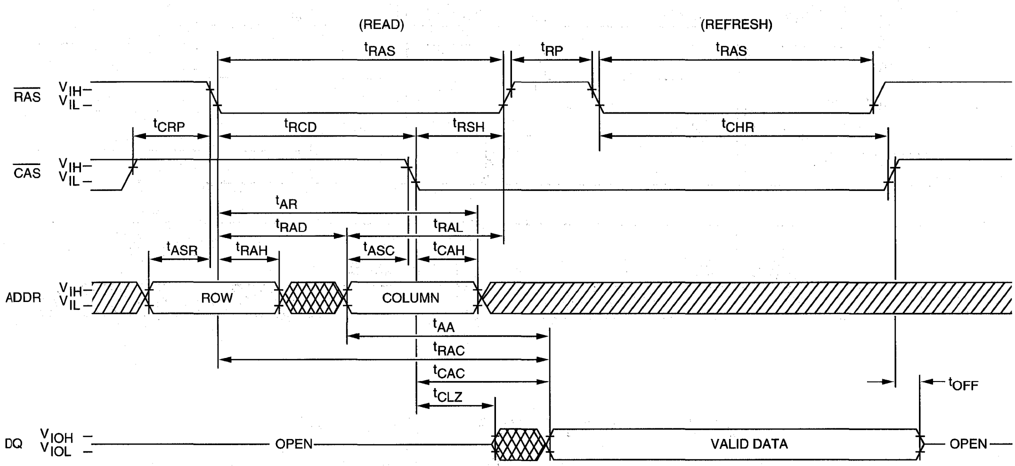
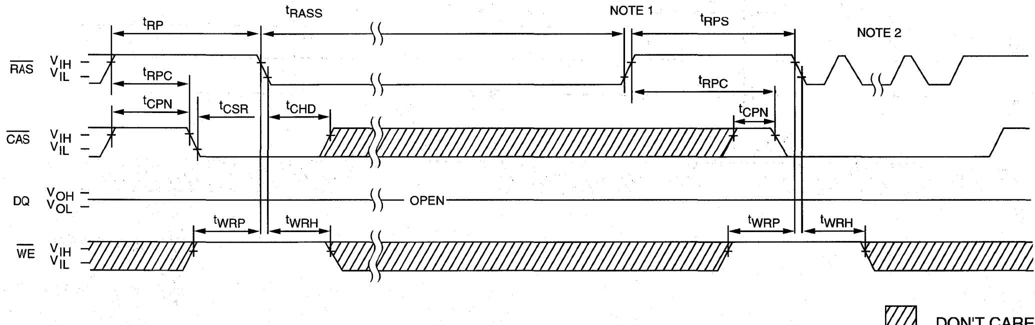
HIDDEN REFRESH CYCLE [20]

(WE = HIGH)



SELF REFRESH CYCLE

(A0-A9 and OE = DON'T CARE)



NOTE:
1. Once tRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a compete burst of all rows should be executed.

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DRAM MODULE

2 MEG x 32, 4 MEG x 16

FAST PAGE MODE (MT16D(T)232)
LOW POWER,
EXTENDED REFRESH (MT16D(T)232 L)

FEATURES

- Industry-standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 48mW (13mW L-version) standby; 1,824mW active, typical
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN; optional Extended Refresh mode
- Multiple RAS lines allow x16 or x32 width
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Thin outline using TSOP version

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Components	
SOJ	D
TSOP	DT
• Packages	
Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (gold)	G
• Power/Refresh	
Normal Power/16ms	Blank
Low Power/128ms	L

- Part Number Example: MT16DT232G-6 L

GENERAL DESCRIPTION

The MT16D(T)232 is a randomly accessed solid-state memory containing 2,097,152 words organized in a x32 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last.

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(DE-8) SOJ Version
(DE-20) TSOP Version

MT16D(T)232M/G

1 36 37 72

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	RAS1	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	RAS3	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its

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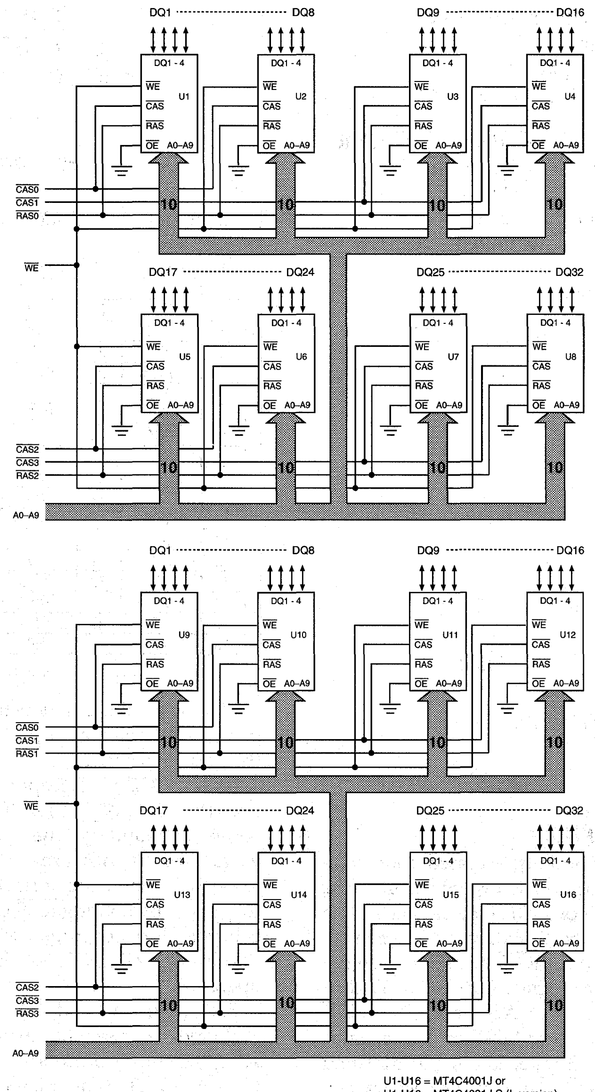
correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE) or $\overline{\text{RAS}}$ REFRESH cycle ($\overline{\text{RAS}}$ ONLY, CBR or HIDDEN) so that all 1,024 combination of $\overline{\text{RAS}}$ addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

For x16 applications, the corresponding DQ and $\overline{\text{CAS}}$ pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and $\overline{\text{CAS0}}$ to $\overline{\text{CAS2}}$ and $\overline{\text{CAS1}}$ to $\overline{\text{CAS3}}$). Each $\overline{\text{RAS}}$ is then a bank select for the x16 memory organization.

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4001J or
U1-U16 = MT4C4001J S (L-version)

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ${}^tR$	ADDRESSES ${}^tC$	DATA-IN/OUT DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
Extended CBR REFRESH (L-version)		H→L	L	H	X	X	High-Z

DRAM MODULE

PRESENCE-DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	II1	-8	8	µA	
Any input 0V ≤ VIN ≤ 6.5V	A0-A9, $\overline{WE}$	II2	-32	32	µA	
(All other pins not under test = 0V) for each package input	$\overline{RAS0}$-$\overline{RAS3}$	II3	-8	8	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ32	IOZ	-20	20	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	32	32	32	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	16	16	16	mA	
		3.2	3.2	3.2	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC = {}^tRC$ [MIN])	ICC3	896	816	736	mA	2, 22, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: $^tPC = {}^tPC$ [MIN])	ICC4	656	576	496	mA	2, 22, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = VIH: $^tRC = {}^tRC$ [MIN])	ICC5	896	816	736	mA	22, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC = {}^tRC$ [MIN])	ICC6	896	816	736	mA	19, 22
REFRESH CURRENT: Extended CBR Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = Vcc -0.2V; A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	ICC7	4.0	4.0	4.0	mA	19, 22, 24, 27

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		95	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		127	pF	17
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$, $\overline{RAS0}$-$\overline{RAS3}$	C_{I4}		32	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	23
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	3	15	3	20	3	20	ns	12, 25
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	^tREF		16/128*		16/128*		16/128*	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	19
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	28
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	28
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	28
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	28

*L-version only

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NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U16.
22. Icc is dependent on cycle rates.
23. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
24. Applies to L-version only.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.
27. Extended refresh current is reduced as ^{t}RAS is reduced from its maximum specification during the extended refresh cycle.
28. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.

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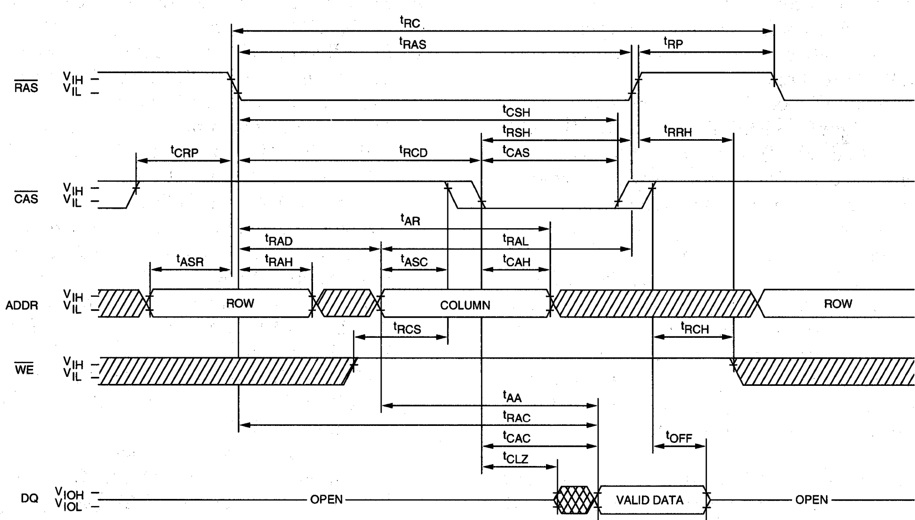
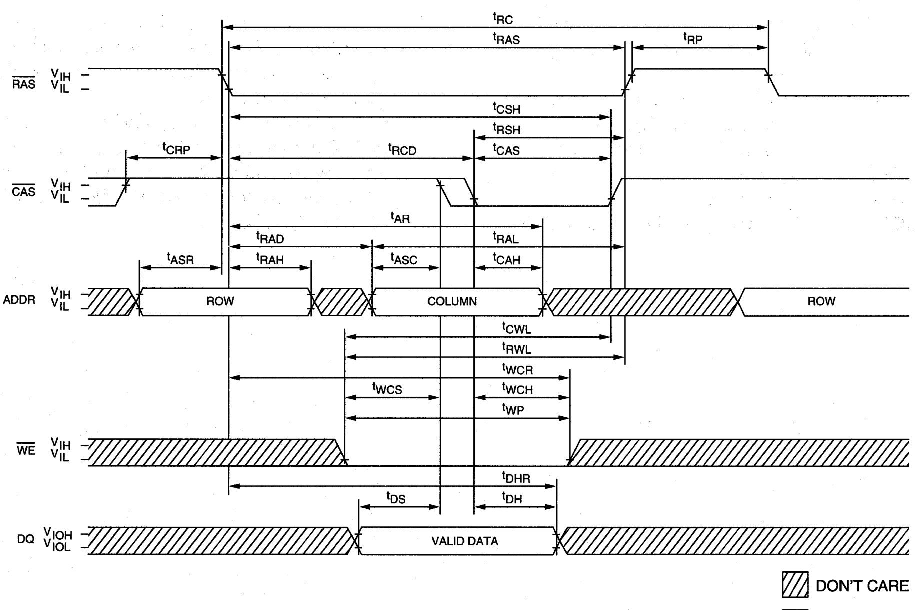
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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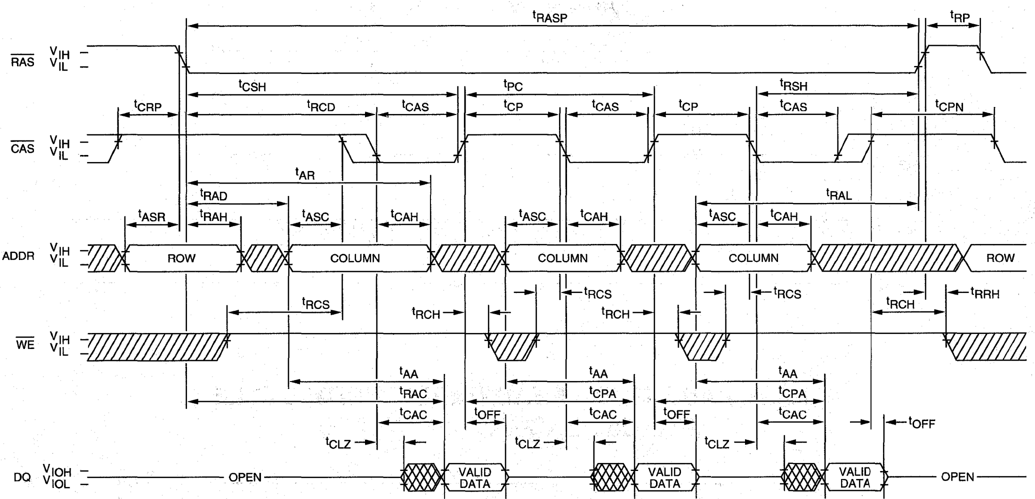
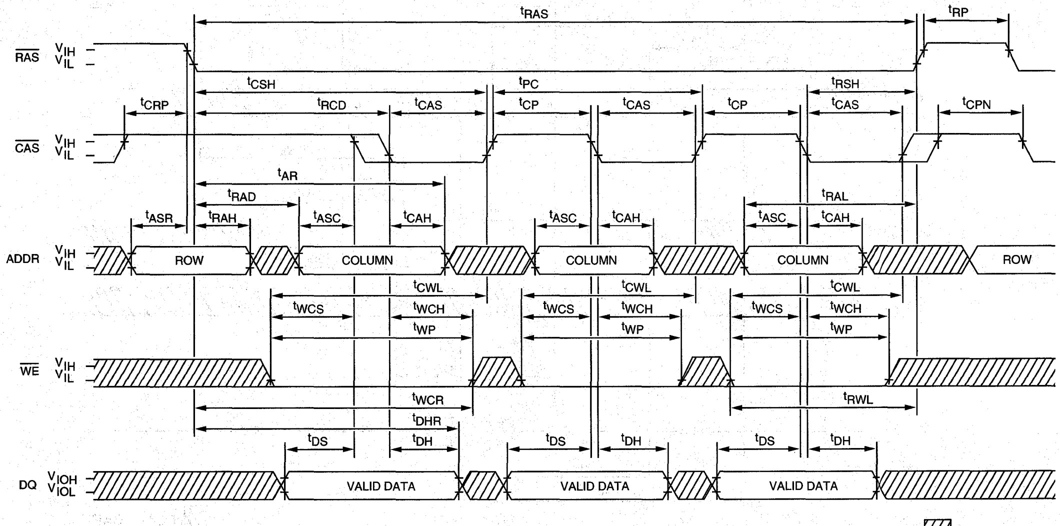
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

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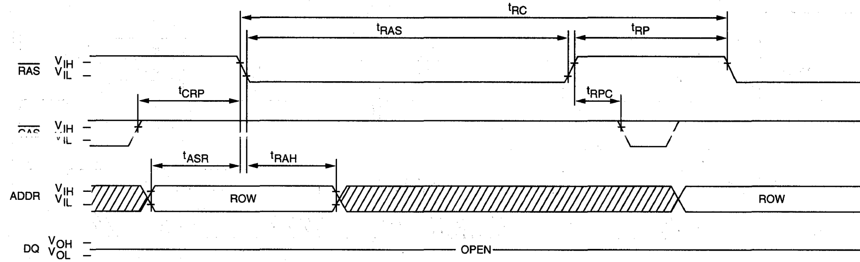
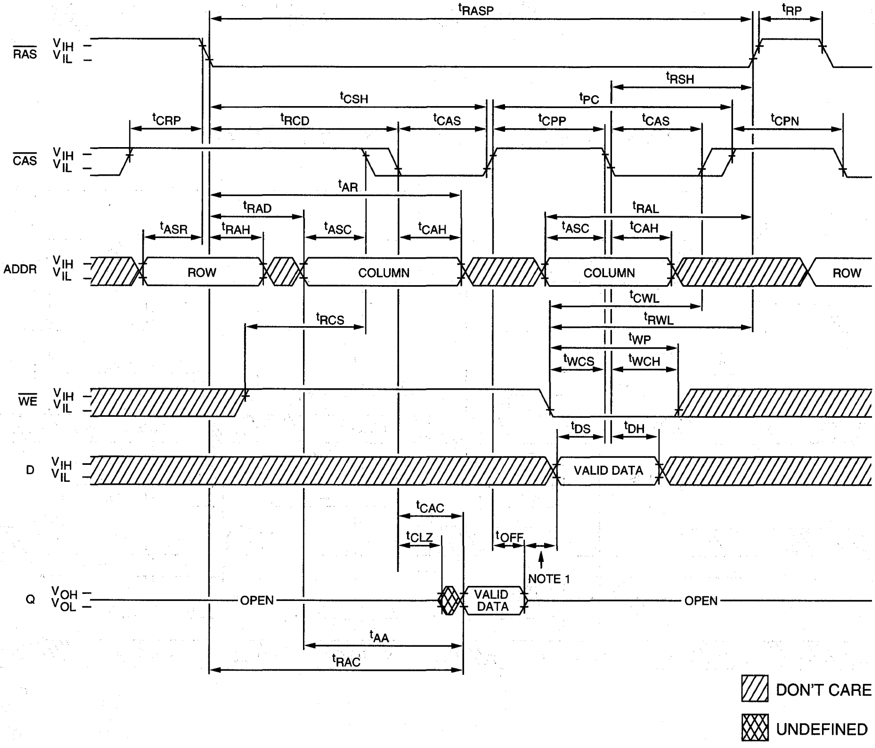
RAS ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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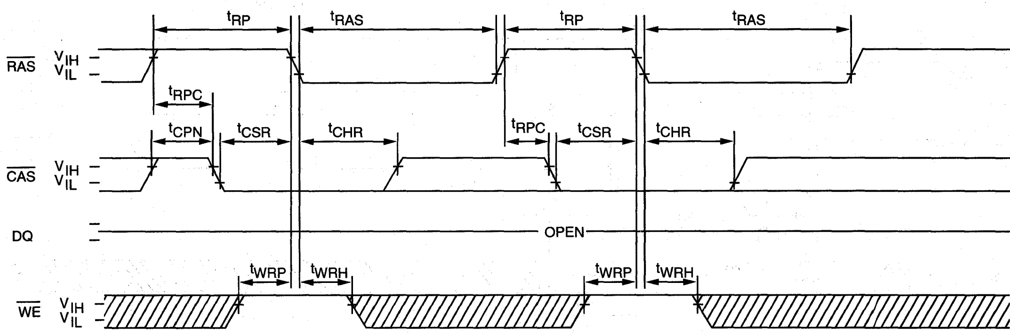
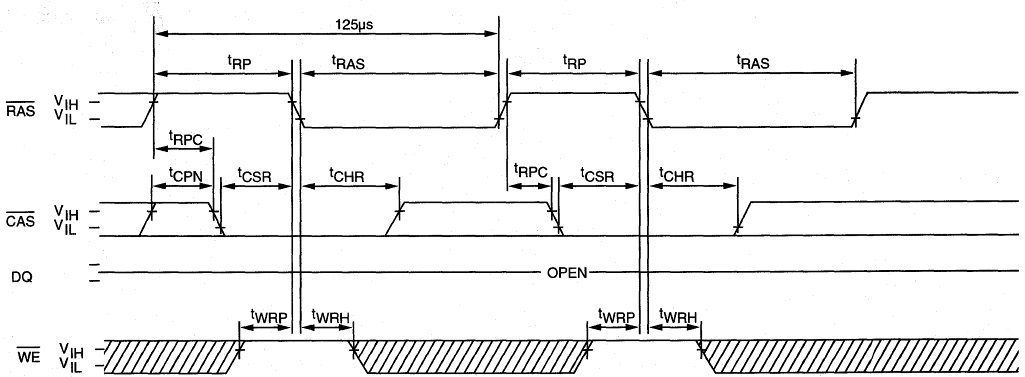
CBR REFRESH CYCLE
(A0-A9 = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [24]
(A0-A9 = DON'T CARE)



DON'T CARE

UNDEFINED

DRAM MODULE

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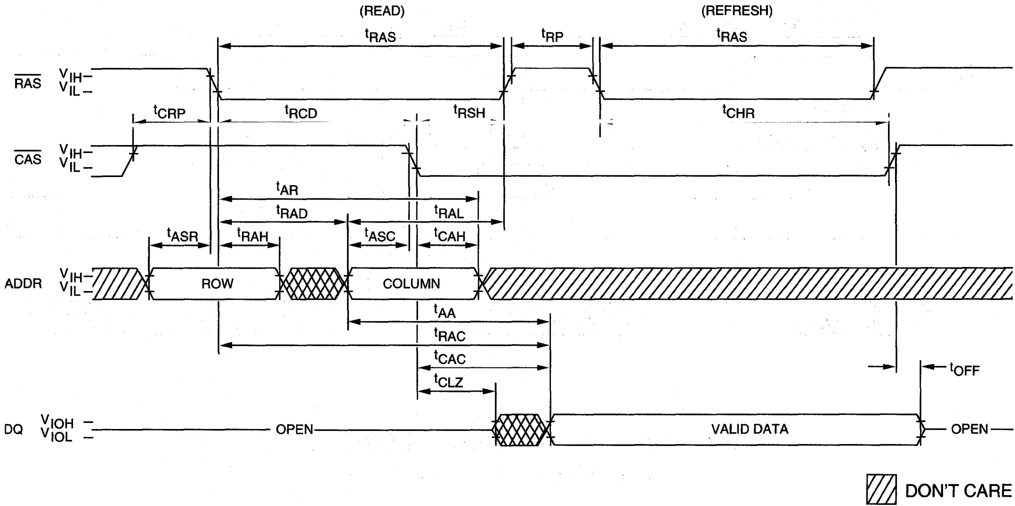
HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



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DRAM MODULE

4 MEG x 32, 8 MEG x 16
FAST PAGE MODE

FEATURES

- Industry-standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL-compatible
- Low power, 24mW standby; 1,600mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Multiple $\overline{RAS}$ lines allow x16 or x32 width
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE access cycle

OPTIONS — MARKING

- Timing
  - 60ns access: -6
  - 70ns access: -7
- Packages
  - Leadless 72-pin SIMM: M
  - Leadless 72-pin SIMM (gold): G
- Part Number Example: MT8D432G-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(DE-19)

MT8D432M/G

1 36 37 72

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

GENERAL DESCRIPTION

The MT8D432 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x32 configuration. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{CAS}$. Since $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all 2,048 combinations of $\overline{RAS}$ addresses are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

For x16 applications, the corresponding DQ and $\overline{CAS}$ pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the x16 memory organization.

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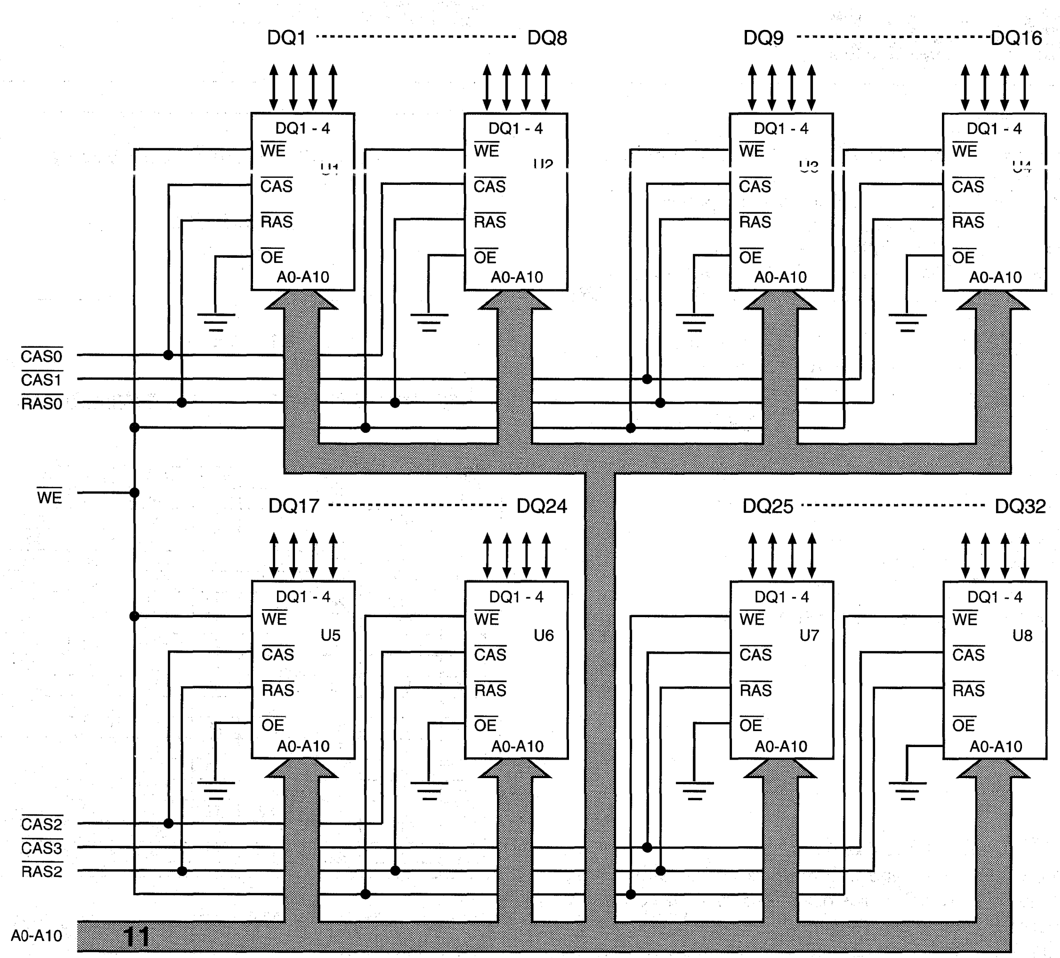
FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4M4B1DJ (2,048-cycle)

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TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA-IN/OUT
					tR	tC	DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

PRESENCE-DETECT

SYMBOL	-6	-7
PRD1	Vss	Vss
PRD2	NC	NC
PRD3	NC	Vss
PRD4	NC	NC

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	RAS0, RAS2	II1	-8	8	µA	
Any input 0V ≤ VIN ≤ 6.5V	A0-A10, WE	II2	-16	16	µA	
(All other pins not under test = 0V) for each package input	CAS0-CAS3	II3	-4	4	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ32	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = 5V ±10%) 2,048-cycle refresh

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16	16	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	8	8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	960	800	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	640	560	mA	3, 4, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	960	800	mA	3, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	960	800	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		51	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		67	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		32	pF	2
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		16	pF	2
Input/Output Capacitance: DQ1-DQ32	C_{IO}		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		ns	22
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15
Access time from column-address	^tAA		30		35	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time	^tRCH	0		0		ns	19

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	25
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 25
$\overline{WE}$ command setup time	^tWCS	0		0		ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
Write command pulse width	^tWP	10		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in setup time	^tDS	0		0		ns	21
Data-in hold time	^tDH	10		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	^tREF		32		32	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR test cycle)	^tCSR	5		5		ns	5
$\overline{CAS}$ hold time (CBR test cycle)	^tCHR	15		15		ns	5
$\overline{WE}$ hold time (CBR test cycle)	^tWRH	10		10		ns	24
$\overline{WE}$ setup time (CBR test cycle)	^tWRP	10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		ns	24

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS)
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ${}^tREF$ refresh requirement is exceeded.
8. AC characteristics assume ${}^tT$ = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ${}^tRCD < {}^tRCD$ (MAX). If ${}^tRCD$ is greater than the maximum recommended value shown in this table, ${}^tRAC$ will increase by the amount that ${}^tRCD$ exceeds the value shown.
15. Assumes that ${}^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ${}^tCPN$.
17. Operation within the ${}^tRCD$ (MAX) limit ensures that ${}^tRAC$ (MAX) can be met. ${}^tRCD$ (MAX) is specified as a reference point only; if ${}^tRCD$ is greater than the specified ${}^tRCD$ (MAX) limit, then access time is controlled exclusively by ${}^tCAC$.
18. Operation within the ${}^tRAD$ (MAX) limit ensures that ${}^tRCD$ (MAX) can be met. ${}^tRAD$ (MAX) is specified as a reference point only; if ${}^tRAD$ is greater than the specified ${}^tRAD$ (MAX) limit, then access time is controlled exclusively by ${}^tAA$.
19. Either ${}^tRCH$ or ${}^tRRH$ must be satisfied for a READ cycle.
20. ${}^tOFF$ (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
22. $\overline{OE}$ is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not possible.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. ${}^tWTS$ and ${}^tWTH$ are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ${}^tWRP$ and ${}^tWRH$ in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.

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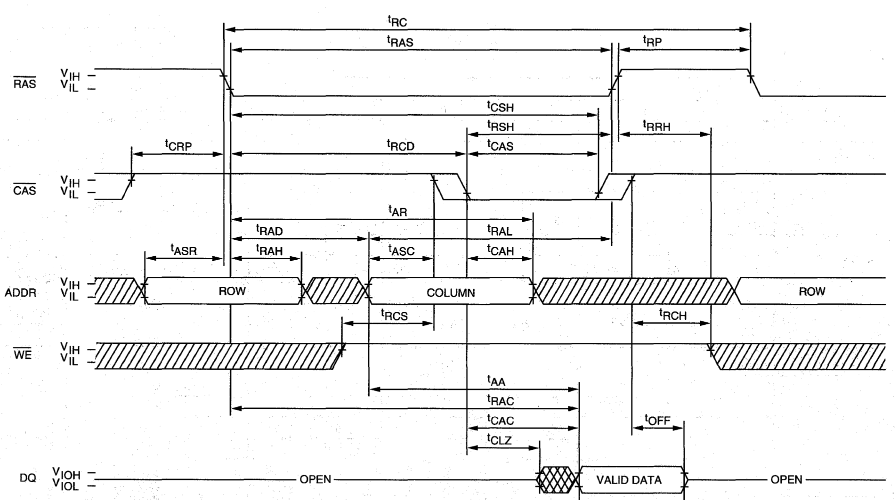
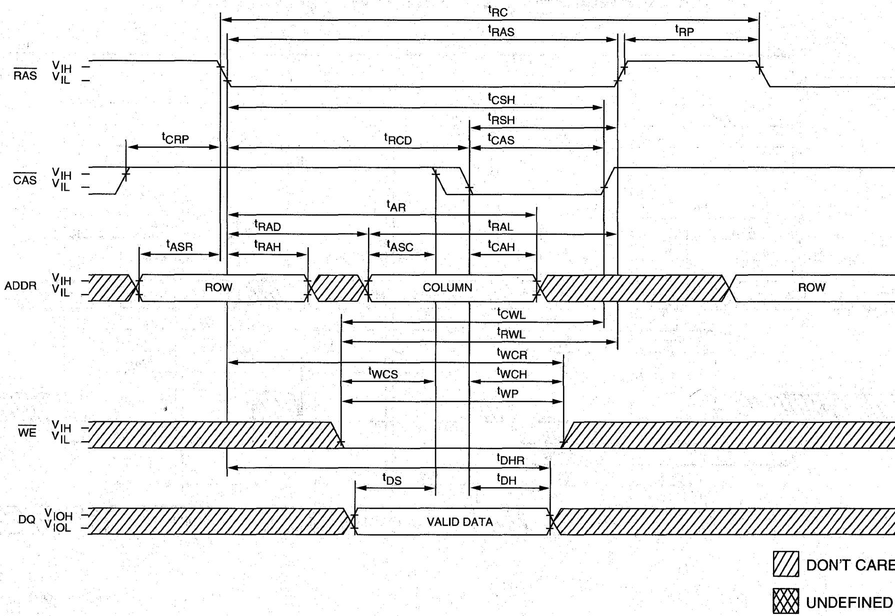
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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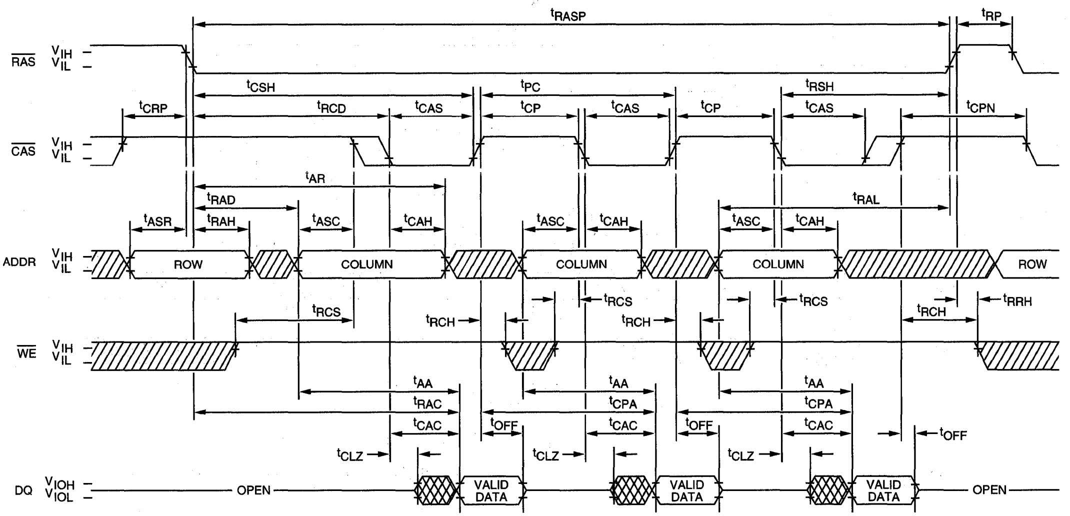
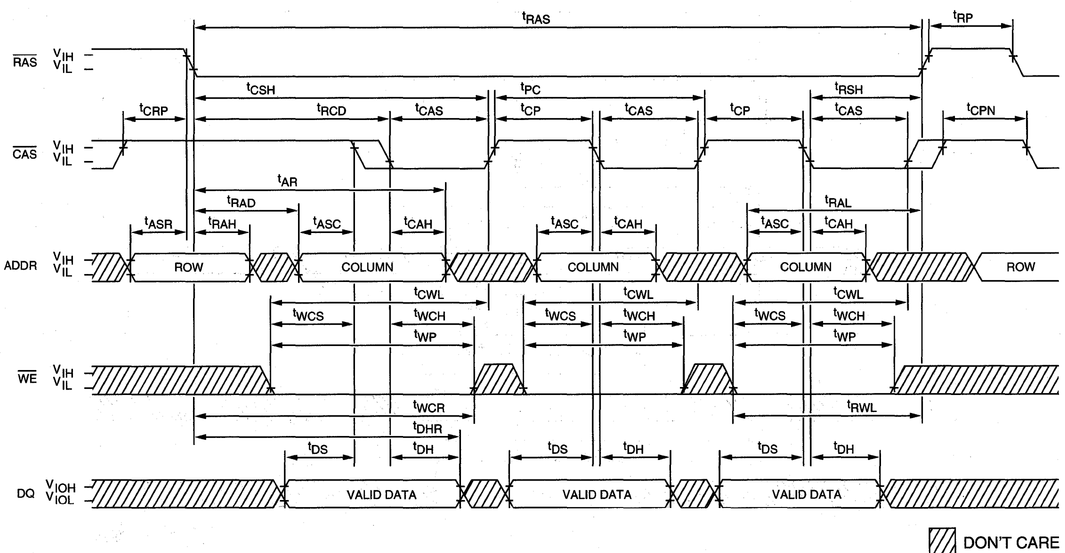
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

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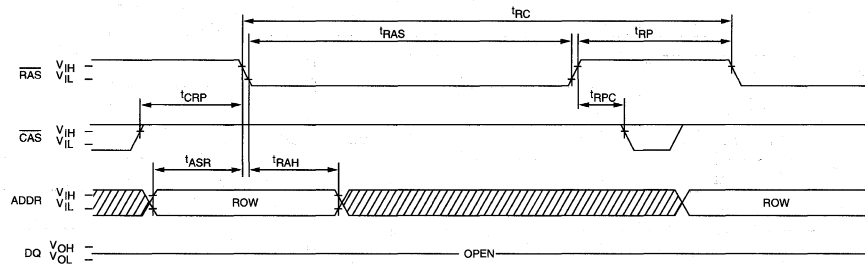
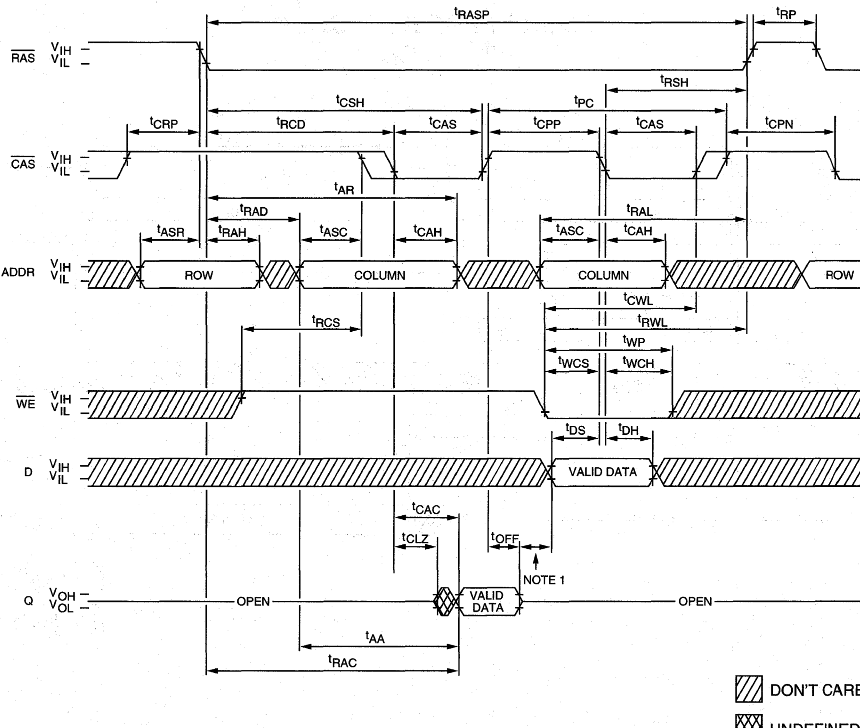
RAS ONLY REFRESH CYCLE
(ADDR = A0-A10; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

DRAM MODULE

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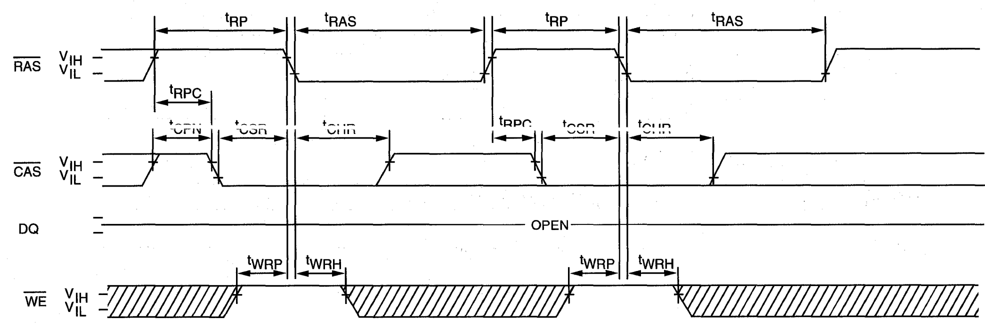
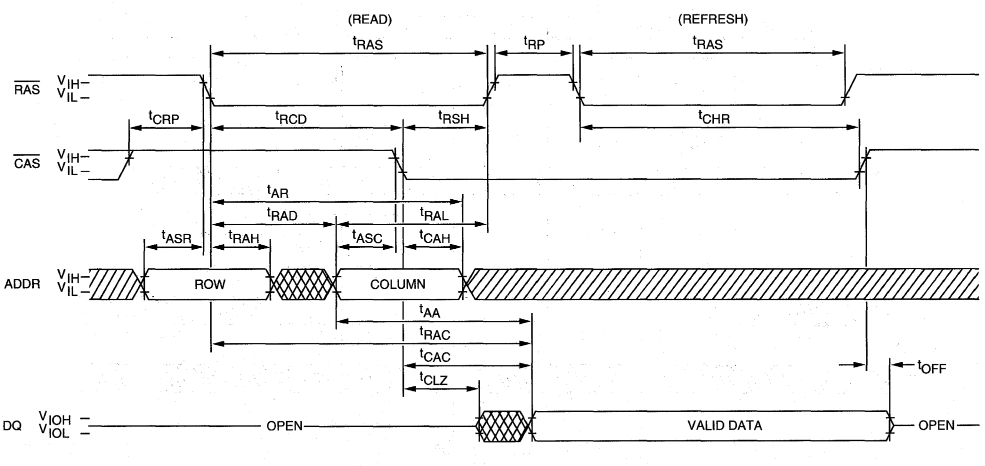
CBR REFRESH CYCLE
(ADDRESSES = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
(WE = HIGH)



DON'T CARE

UNDEFINED

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DRAM MODULE

4 MEG, 8 MEG x 32

3.3V 16, 32 MEGABYTES
OPTIONAL SELF REFRESH

FEATURES

- Industry-standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 16mW standby; 1,440mW active, typical
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR), HIDDEN and SELF
- Multiple $\overline{\text{RAS}}$ lines allow x16 or x32 width
- 2,048-cycle refresh distributed across 32ms or 2,048-cycle extended refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Optional SELF REFRESH mode, Extended Refresh rate

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (gold)	G
• Refresh	
Standard	Blank
Self refresh	S

- Part Number Example: MT16LD832G-6 S

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(DE-19) 4 Meg x 32
(DE-11) 8 Meg x 32

MT16D832M/G S

1 36 37 72

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{\text{CAS0}}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{\text{CAS2}}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{\text{CAS3}}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{\text{CAS1}}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{\text{RAS0}}$	62	DQ31
9	DQ20	27	DQ24	45	NC*/$\overline{\text{RAS1}}$	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC*/$\overline{\text{RAS3}}$	51	DQ10	69	PRD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

*16MB version only

GENERAL DESCRIPTION

The MT8LD432(S) and MT16LD832(S) are randomly accessed 16MB and 32MB solid-state memories organized in a x32 configuration. They are specially processed to operate from 3.0V to 3.6V for low voltage memory systems. The modules have optional FAST PAGE MODE, which allows faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary.

During READ or WRITE cycles each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. $\overline{\text{RAS}}$ latches the first 11 bits and $\overline{\text{CAS}}$ latches the latter 11 bits.

READ and WRITE cycles are selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. EARLY WRITE occurs when $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) with lower power consumption within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{\text{RAS}}$ followed by a column-address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the FAST PAGE MODE operation.

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REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms (128ms "S" option), regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

An optional SELF REFRESH mode is also available. The "S" option allows the user the option of a fully static low power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms, four times longer than the standard 32ms specifications. The module's SELF REFRESH mode is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" option allows for an extended refresh rate of 62.5µs per row if using distributed CBR refresh. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ^{t}RPS ($\approx ^{t}$RCns). This delay allows for the completion of any internal refresh cycles that may be in process at the time of RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS only or BURST REFRESH sequence, all 2,048 rows must be refreshed within 300µs, prior to the resumption of normal operation.

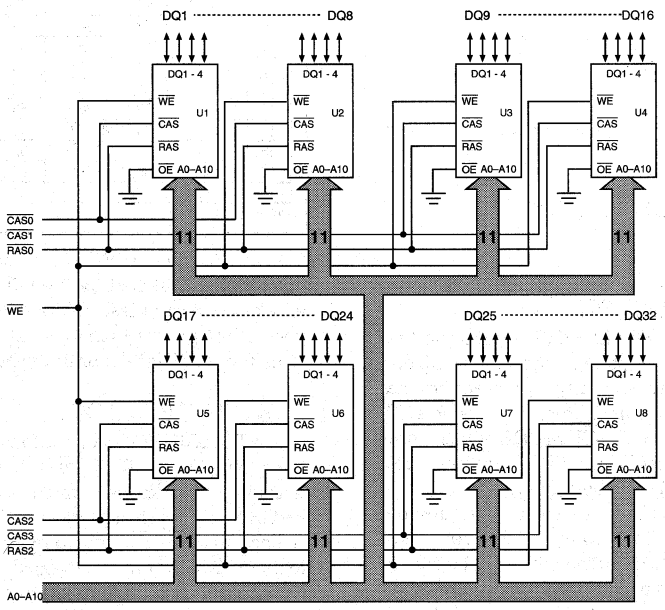
STANDBY

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time.

x16 OPERATION

For x16 applications, the corresponding DQ and CAS pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x16 memory organization.

FUNCTIONAL BLOCK DIAGRAM 16MB



U1-U8 = MT4LC4M4B1SJ or
U1-U8 = MT4LC4M4B1SJ S ("S" option)

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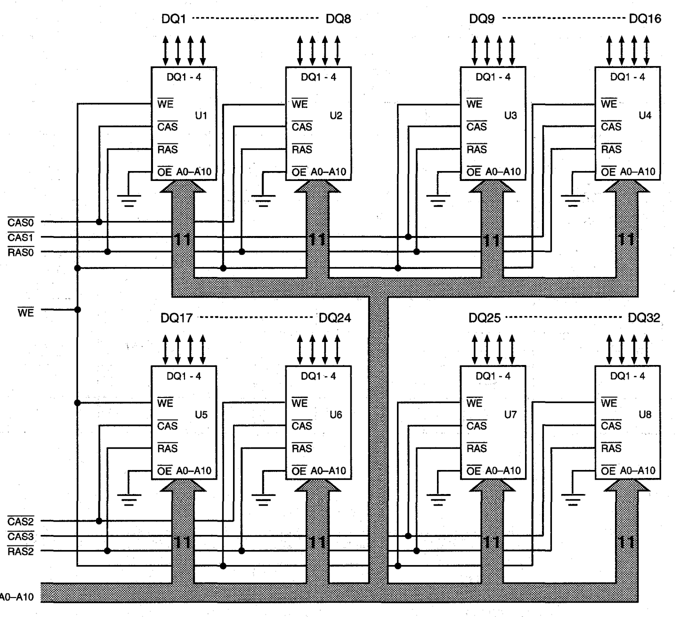
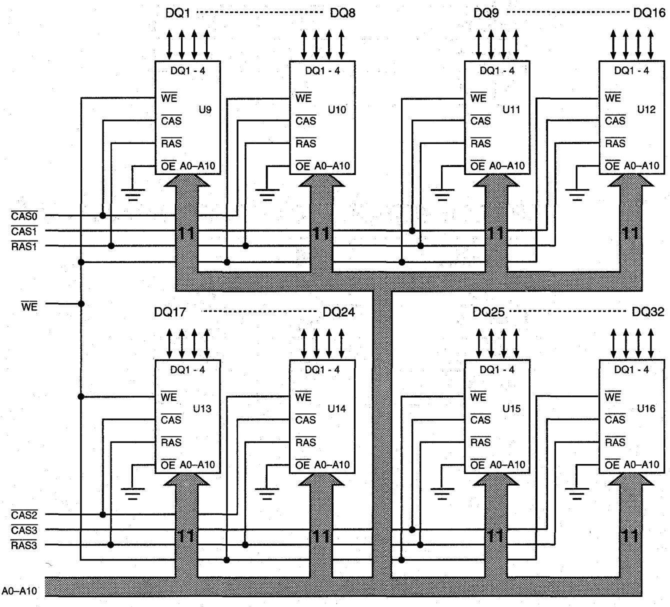
NEW DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM
32MB





U1-U16 = MT4LC4M4B1SJ or
U1-U16 = MT4LC4M4B1SJ S ("S" option)

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES		DATA-IN/OUT
					${}^tR$	${}^tC$	DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	High-Z

PRESENCE-DETECT - MT8LD432 (16MB)

SYMBOL	-6	-7
PRD1	Vss	Vss
PRD2	NC	NC
PRD3	NC	Vss
PRD4	NC	NC

PRESENCE-DETECT - MT16LD832 (32MB)

SYMBOL	-6	-7
PRD1	NC	NC
PRD2	Vss	Vss
PRD3	NC	Vss
PRD4	NC	NC

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +4.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (Vcc = 3.0V to 3.6V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	I_{I1}	-8	8	µA	28
Any input 0V ≤ V_{IN} ≤ 3.6V	A0-A9, $\overline{WE}$	I_{I2}	-32	32	µA	28
(All other pins not under test = 0V) for each package input	$\overline{RAS0}$-$\overline{RAS3}$	I_{I3}	-8	8	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 3.6V) for each package input	DQ1-DQ32	I_{OZ}	-20	20	µA	28
TTL OUTPUT LEVELS High Voltage (I_{OUT} = -2mA)		V_{OH}	2.4		V	
Low Voltage (I_{OUT} = 2mA)		V_{OL}		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6, 22) (V_{CC} = 3.0V to 3.6V)

PARAMETER/CONDITION		SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = V_{IH})		I_{CC1}	16MB 32MB	8 16	8 16	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = V_{CC} -0.2V)	STD	I_{CC2}	16MB 32MB	4 8	4 8	mA	
	S	I_{CC2}	16MB 32MB	1.2 2.4	1.2 2.4	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ${}^tRC = {}^tRC$ [MIN])		I_{CC3}	16MB 32MB	960 968	880 888	mA	2, 22, 25
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V_{IL}, CAS, Address Cycling: ${}^tPC = {}^tPC$ [MIN])		I_{CC4}	16MB 32MB	720 728	640 648	mA	2, 22, 25
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = V_{IH}: ${}^tRC = {}^tRC$ [MIN])		I_{CC5}	16MB 32MB	960 968	880 888	mA	22, 25
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: ${}^tRC = {}^tRC$ [MIN])		I_{CC6}	16MB 32MB	960 968	880 888	mA	22, 19
REFRESH CURRENT: Extended (S only) Average power supply current CAS = 0.2V or CBR cycling; RAS = ${}^tRAS$ (MIN); WE = Vcc -0.2V; A0-A10 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ${}^tRC$ = 62.5µs		I_{CC7}	16MB 32MB	2.4 3.6	2.4 3.6	mA	19, 22
REFRESH CURRENT: SELF (S only) Average power supply current during SELF REFRESH: CBR cycle with RAS ≥ ${}^tRASS$ (MIN) and CAS held LOW; WE = Vcc -0.2V; A0-A10 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open)		I_{CC8}	16MB 32MB	2.4 3.6	2.4 3.6	mA	19

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CAPACITANCE

PARAMETER	SYMBOL	MAX 16MB	MAX 32MB	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	48	95	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}	64	127	pF	17
Input Capacitance: $\overline{RAS0}$-$\overline{RAS3}$	C_{I3}	32	32	pF	17
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$	C_{I4}	16	32	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}	10	16	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
Access time from $\overline{RAS}$	^tRAC		60		70	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20	ns	9
Access time from column-address	^tAA		30		35	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ precharge time (CBR REFRESH)	^tCPN	10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	23
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	14
Read command hold time (referenced to $\overline{CAS}$)	^tRRH	0		0		ns	14
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	24
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	12, 24

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{WE}$ command setup time	^tWCS	0		0		ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
Write command pulse width	^tWP	10		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in setup time	^tDS	0		0		ns	15
Data-in hold time	^tDH	10		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	5, 16
Refresh period (2,048 cycles)	^tREF		32		32	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		ns	19
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		ns	19
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	27
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	27
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		ns	27
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		ns	27
$\overline{RAS}$ pulse width entering SELF REFRESH	^tRASS	100		100		µs	26
$\overline{RAS}$ precharge time entering SELF REFRESH	^tRPS	110		130		ns	26
$\overline{CAS}$ hold time entering SELF REFRESH	^tCHD	15		15		ns	26

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NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. Measured with a load equivalent to two TTL gates and 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
8. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Vcc = 3.3V; f = 1 MHz.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U16.
22. I_{CC} is dependent on cycle rates.
23. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
24. The 3ns minimum is a parameter guaranteed by design.
25. Column-address changed once each cycle.
26. Refresh must be completed within the time of three external refresh rate periods prior to active use of the module (provided distributed CBR REFRESH is used when in active mode). Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the module if anything other than distributed CBR REFRESH is used in the active mode.
27. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
28. 16MB module values will be half of those shown.

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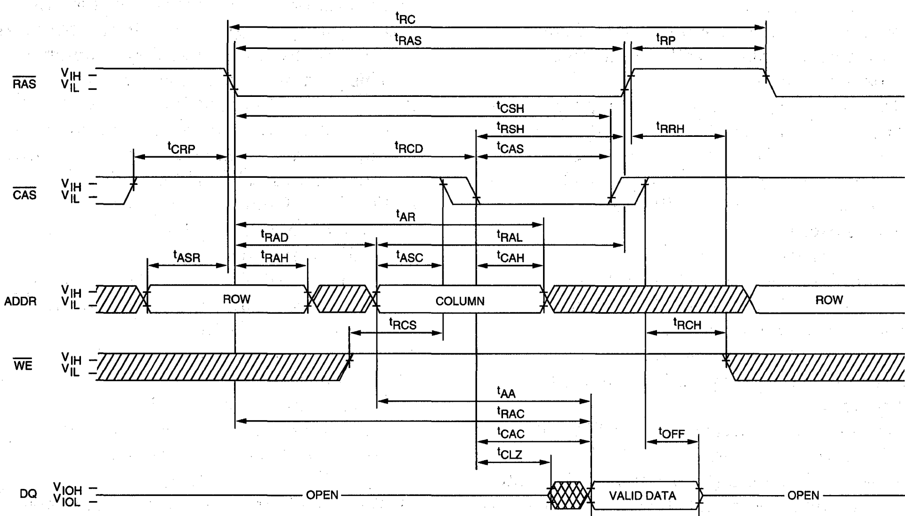
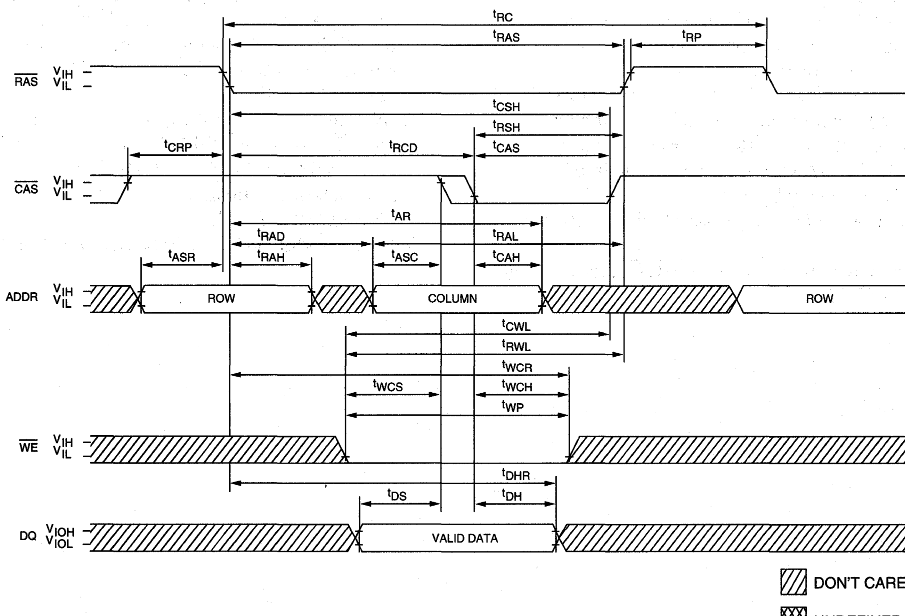
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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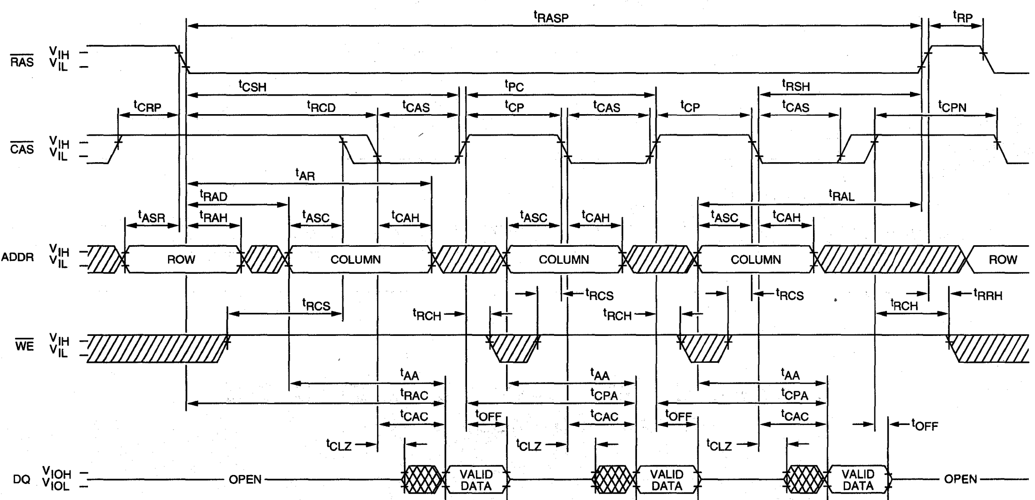
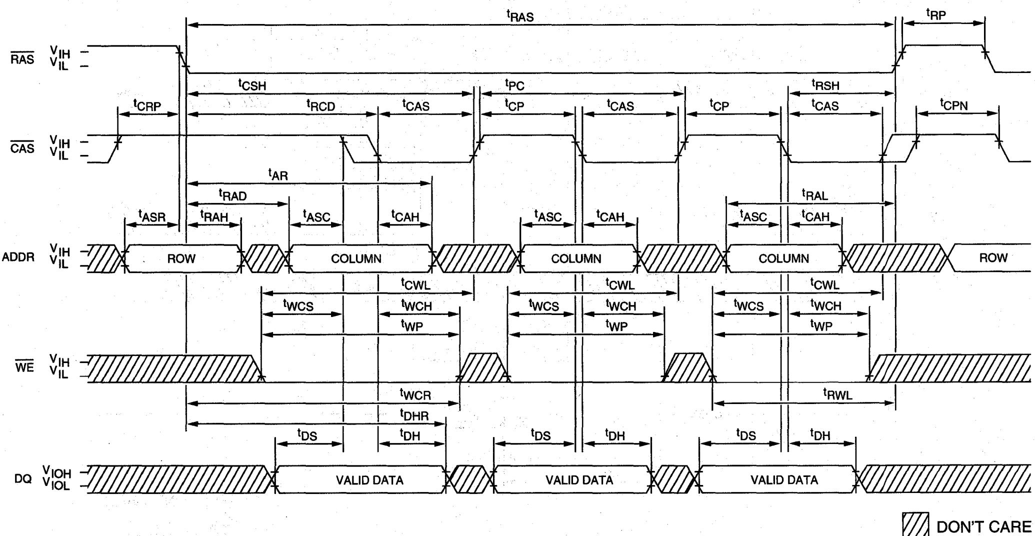
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

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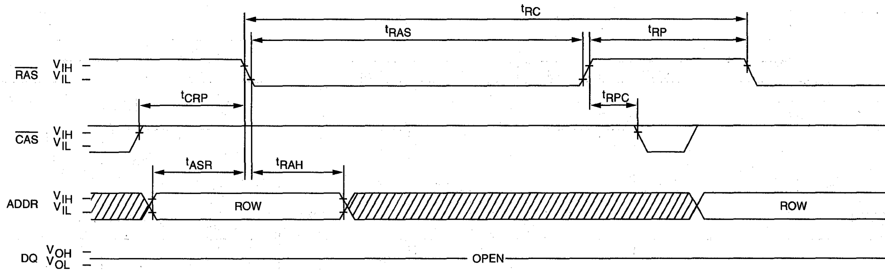
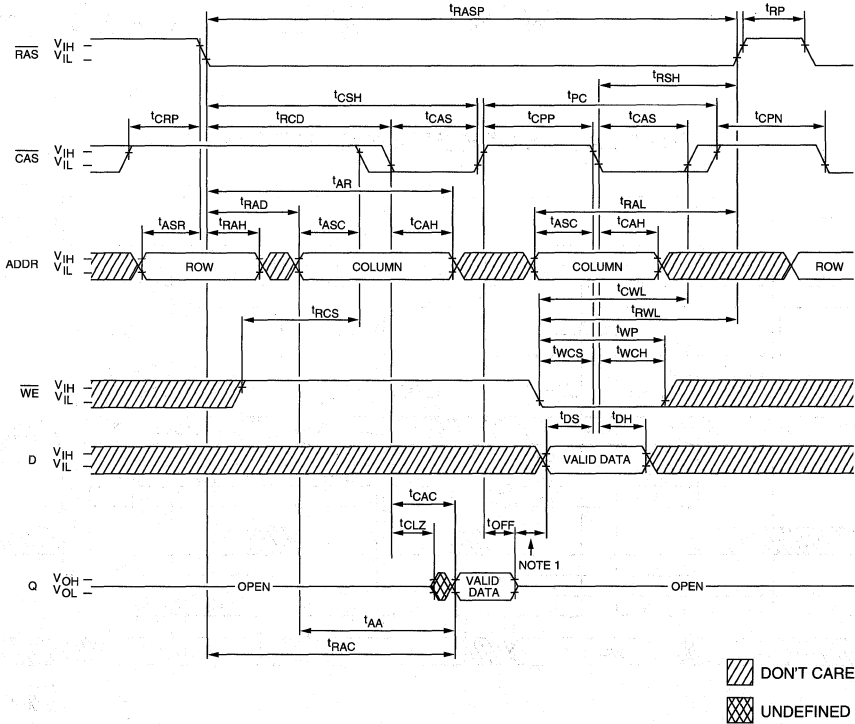
RAS ONLY REFRESH CYCLE

(ADDR = A0-A10; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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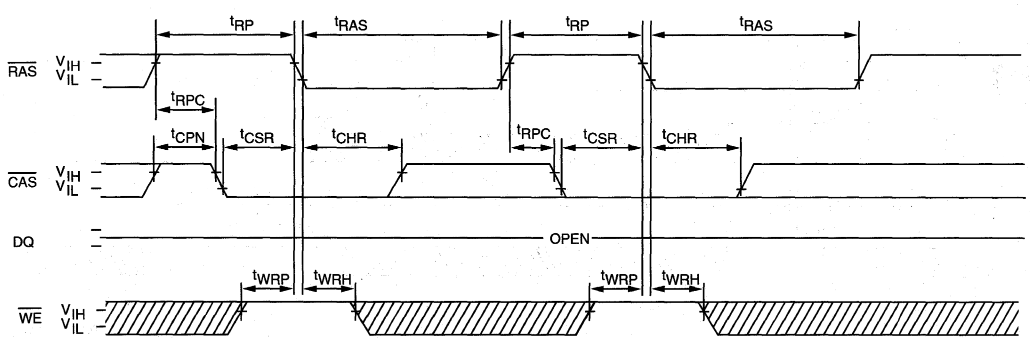
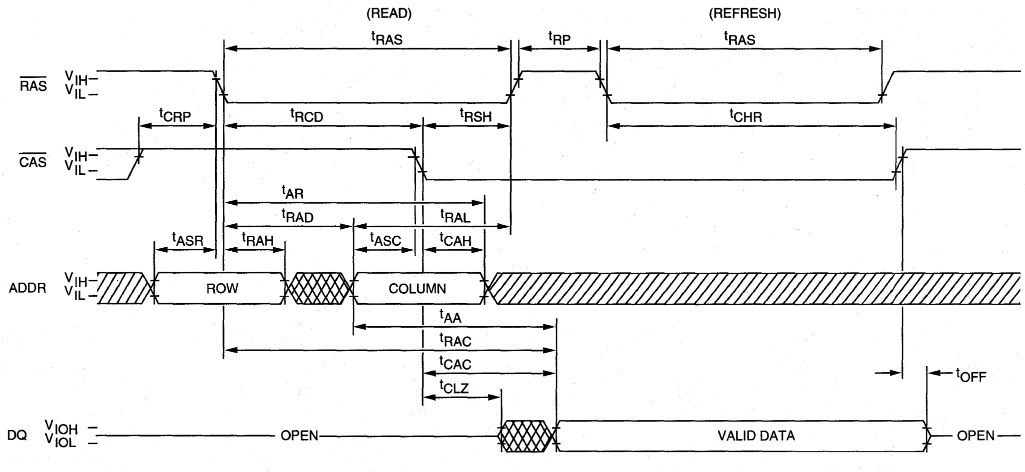
CBR REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
(WE = HIGH)



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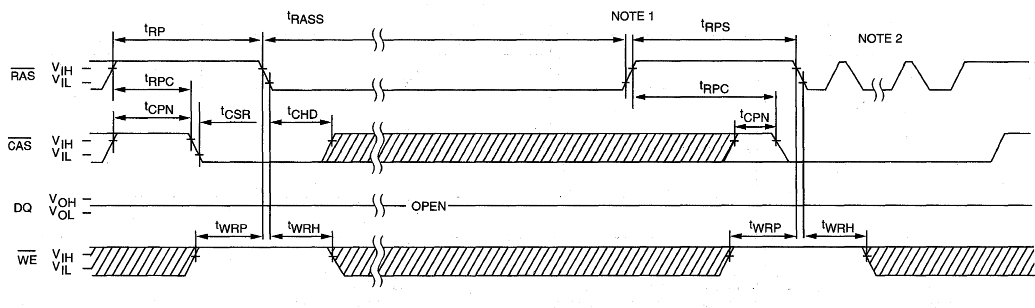
SELF REFRESH CYCLE
(A0-A10 = DON'T CARE)



NOTE: 1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a compete burst of all rows should be executed.

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DRAM MODULE

4 MEG x 32 DRAM

FAST PAGE MODE (MT32D432) LOW POWER, EXTENDED REFRESH (MT32D432 L)

FEATURES

- Industry-standard pinout in a 72-pin small-outline-single in-line package
- High-performance CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 96mW (26mW L-version) standby; 7,200mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional Extended Refresh
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE access cycle

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
72-pin SIMM	M
72-pin SIMM (gold)	G
• Power/Refresh	
Normal Power/16ms	Blank
Low Power/128ms	L

- Part Number Example: MT32D432M-6 L

PIN ASSIGNMENT (Top View)

72-Pin SIMM (DE-21)

MT32D432

1 36 37 72

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

GENERAL DESCRIPTION

The MT32D432 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

REFRESH

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

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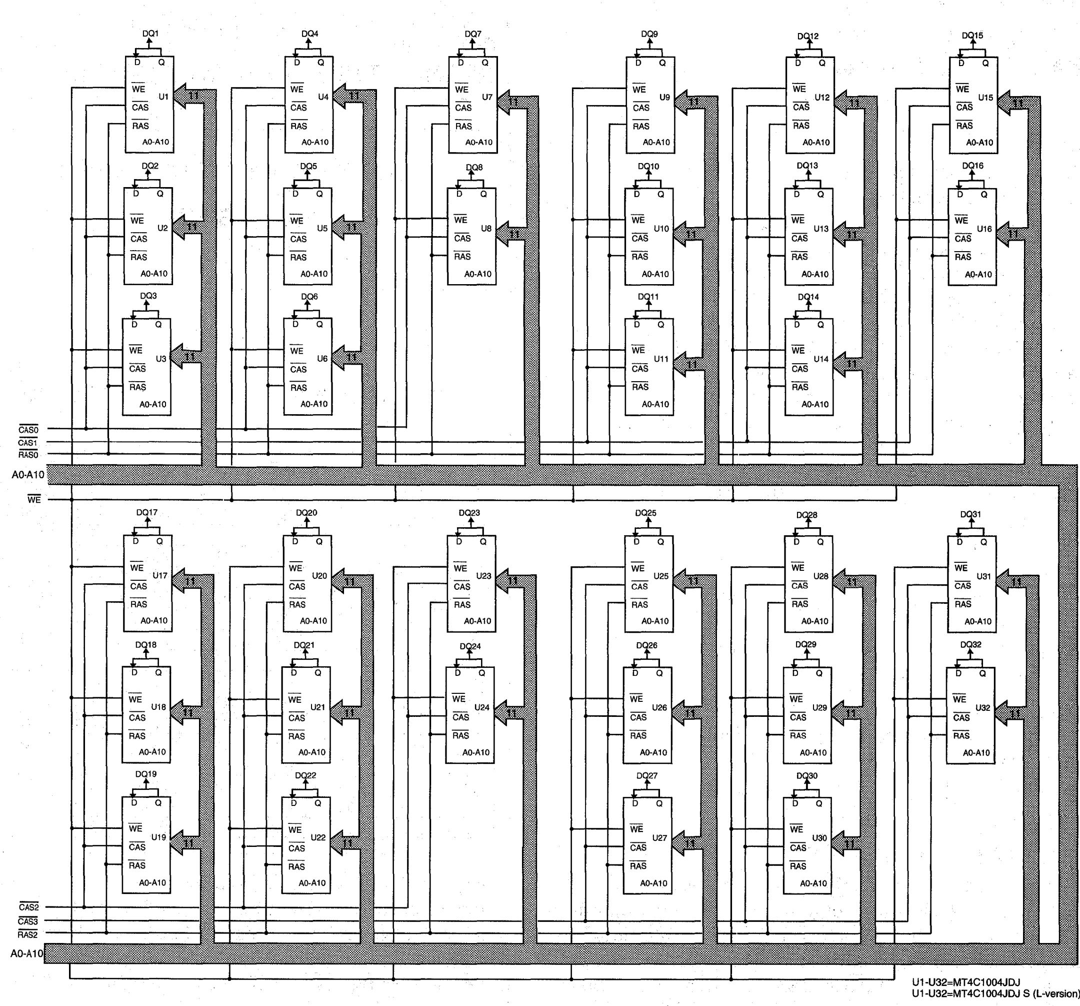
FUNCTIONAL BLOCK DIAGRAM



U1-U32=MT4C1004JDJ
U1-U32=MT4C1004JDJ S (L-version)

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
Extended CBR REFRESH (L-version)		H→L	L	H	X	X	High-Z

PRESENCE-DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

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NEW DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 32W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (Vcc = +5V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	RAS0, RAS2	II1	-32	32	µA	
Any input 0V ≤ VIN ≤ 6.5V	A0-A10, WE	II2	-64	64	µA	
(All other pins not under test = 0V) for each package input	CAS0-CAS3	II3	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ32	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	64	64	64	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	ICC2	32	32	32	mA	
		6.4	6.4	6.4	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	3,520	3,200	2,880	mA	2, 22, 27
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])	ICC4	2,560	2,240	1,920	mA	2, 22, 27
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])	ICC5	3,520	3,200	2,880	mA	2, 27
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC6	3,520	3,200	2,880	mA	19, 22
REFRESH CURRENT: Extended CBR (L-version only) Average power supply current during extended refresh: CAS = 0.2V or CBR cycling; RAS = tRAS (MIN); WE = Vcc -0.2V; A0-A10 and DIN = Vcc -0.2V or 0.2V (DIN may be left open); tRC = 125µs (1,024 rows at 125µs = 128ms)	ICC7	9.6	9.6	9.6	mA	2, 4 19, 24, 26

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	180	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}	244	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}	122	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}	61	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}	14	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	23
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		ns	14
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	tOFF	3	15	3	20	3	20	ns	12, 25
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	tREF		16/128*		16/128*		16/128*	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time (CBR REFRESH)	tCHR	10		10		10		ns	19
$\overline{WE}$ hold time (CBR REFRESH)	tWRH	10		10		10		ns	28
$\overline{WE}$ setup time (CBR REFRESH)	tWRP	10		10		10		ns	28
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	10		10		10		ns	28
$\overline{WE}$ setup time (WCBR test cycle)	tWTS	10		10		10		ns	28

*L-version only

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NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight RAS REFRESH cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ᵗREF refresh requirement is exceeded.
4. AC characteristics assume ᵗT = 5ns.
5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that ᵗRCD < ᵗRCD (MAX). If ᵗRCD is greater than the maximum recommended value shown in this table, ᵗRAC will increase by the amount that ᵗRCD exceeds the value shown.
9. Assumes that ᵗRCD ≥ ᵗRCD (MAX).
10. If CAS = VIH, data output is High-Z.
11. If CAS = VIL, data output may contain data from the last valid READ cycle.
12. ᵗOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the ᵗRCD (MAX) limit ensures that ᵗRAC (MAX) can be met. ᵗRCD (MAX) is specified as a reference point only; if ᵗRCD is greater than the specified ᵗRCD (MAX) limit, then access time is controlled exclusively by ᵗCAC.
14. Either ᵗRCH or ᵗRRH must be satisfied for a READ cycle.
15. These parameters are referenced to CAS leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ᵗCPN.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to OE being grounded on U1-U32.
22. Icc is dependent on cycle rates.
23. Operation within the ᵗRAD (MAX) limit ensures that ᵗRCD (MAX) can be met. ᵗRAD (MAX) is specified as a reference point only; if ᵗRAD is greater than the specified ᵗRAD (MAX) limit, then access time is controlled exclusively by ᵗAA.
24. Applies to L-version only.
25. The 3ns minimum is a parameter guaranteed by design.
26. Extended refresh current is reduced as ᵗRAS is reduced from its maximum specification during the extended refresh cycle.
27. Column-address changed once each cycle.
28. ᵗWTS and ᵗWTH are set up and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ᵗWRP and ᵗWRH in the CBR REFRESH cycle.

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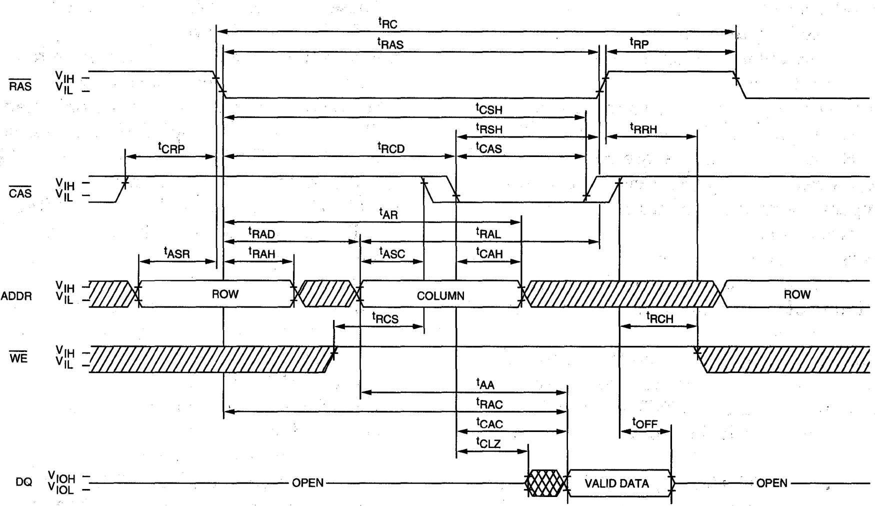
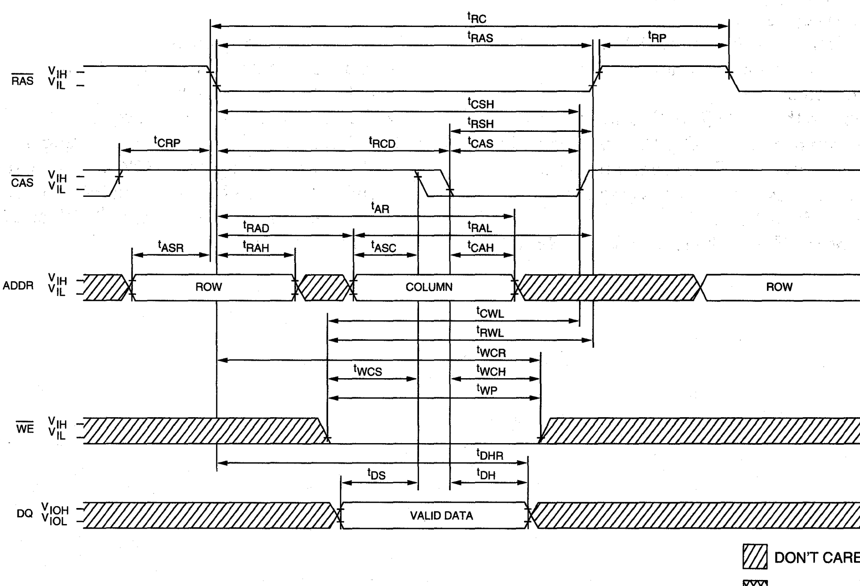
READ CYCLE



EARLY WRITE CYCLE



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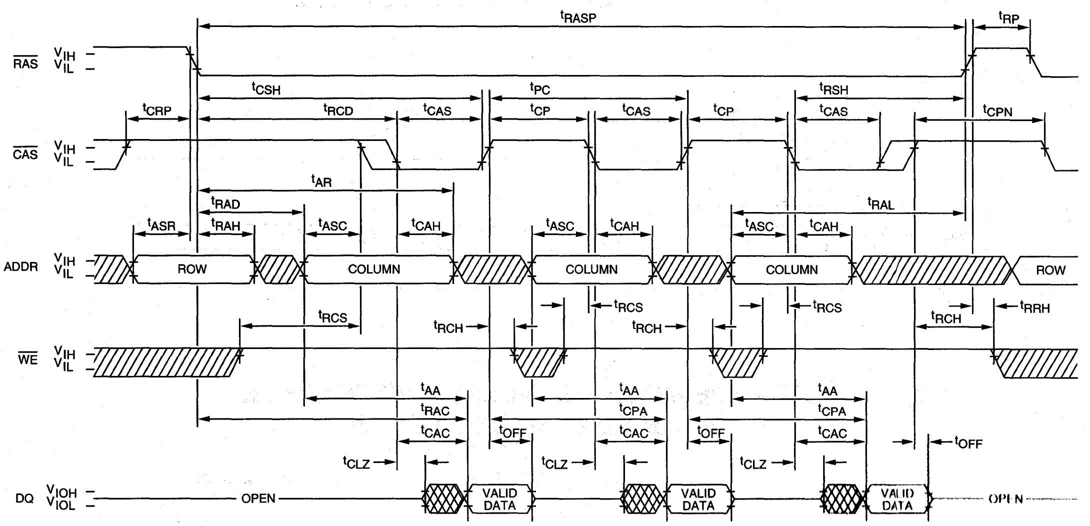
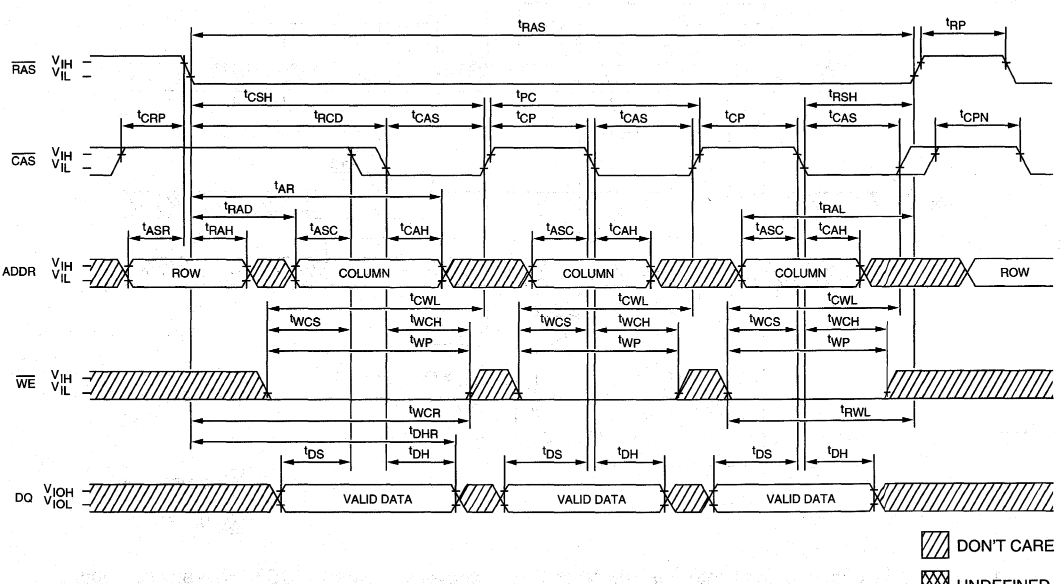
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



NEW DRAM MODULE

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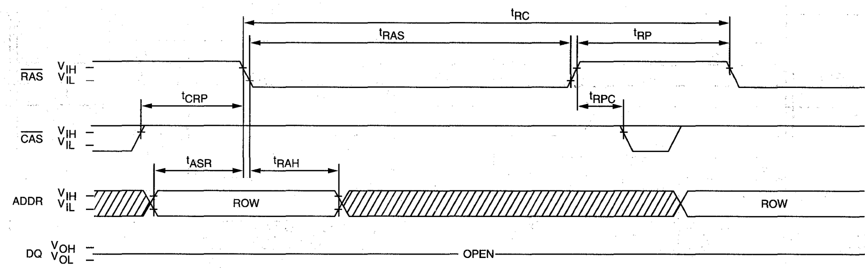
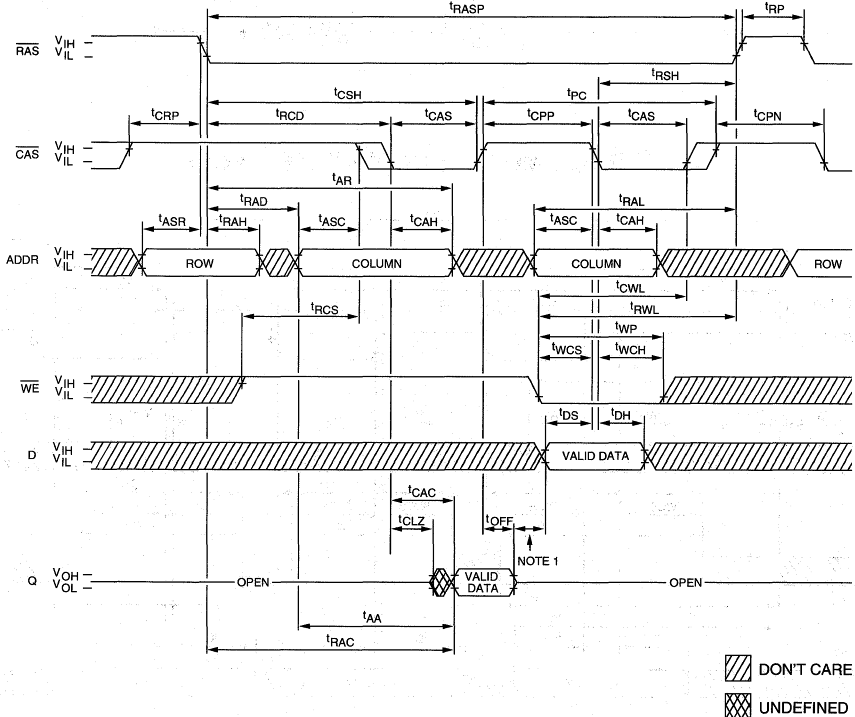
RAS ONLY REFRESH CYCLE
(ADDR = A0-A9; A10 and WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE:
1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

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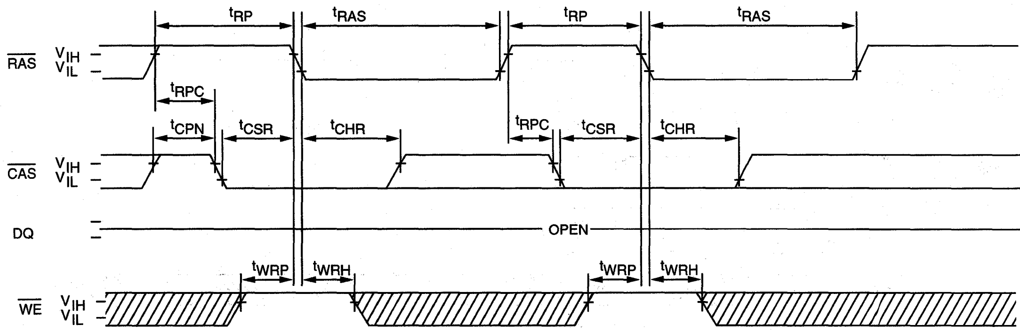
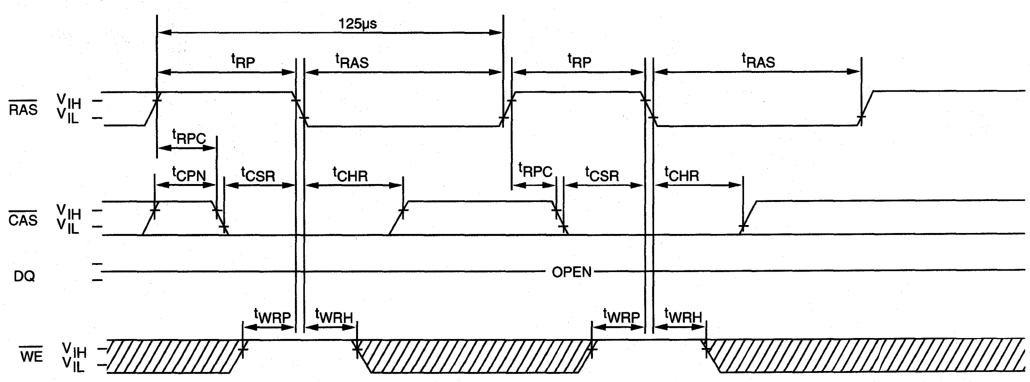
CBR REFRESH CYCLE
(A0-A10 = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [24]
(A0-A10 = DON'T CARE)



DON'T CARE
UNDEFINED

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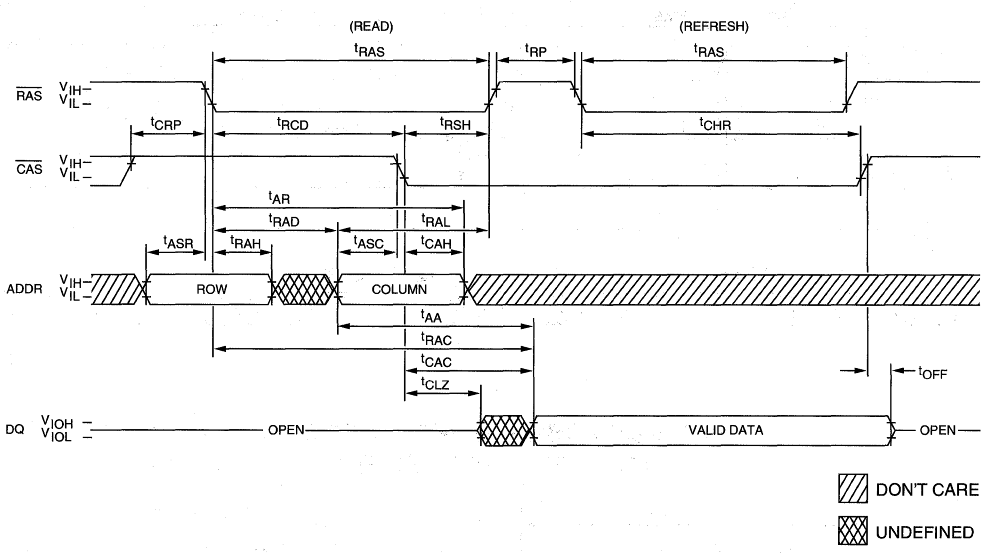
HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



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DRAM MODULE

8 MEG x 32,16 MEG x16

FAST PAGE MODE

FEATURES

- Industry-standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 48mW standby; 1,624mW active, typical
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE access cycle
- Multiple RAS lines allow x16 or x32 width

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
- Packages
  - Leadless 72-pin SIMM — M
  - Leadless 72-pin SIMM (gold) — G
- Part Number Example: MT16D832G-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(DE-11)

MT16D832M/G

1 36 37 72

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	RAS1	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	RAS3	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

GENERAL DESCRIPTION

The MT16D832 is a randomly accessed solid-state memory containing 8,388,608 words organized in a x32 configuration. RAS is used to latch the first 11 bits and CAS the latter 11 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

For x16 applications, the corresponding DQ and CAS pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x16 memory organization.

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FUNCTIONAL BLOCK DIAGRAM

U1-U16 = MT4C4MB1DJ (2,048-cycle)

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES		DATA-IN/OUT
					tR	tC	DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

PRESENCE-DETECT

SYMBOL	-6	-7
PRD1	NC	NC
PRD2	Vss	Vss
PRD3	NC	Vss
PRD4	NC	NC

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{RAS0}$-$\overline{RAS3}$	II1	-8	8	µA	
Any input 0V ≤ VIN ≤ 6.5V	A0-A10, $\overline{WE}$	II2	-32	32	µA	
(All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS3}$	II3	-8	8	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ32	IOZ	-20	20	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = 5V ±10%) 2,048-cycle refresh

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	32	32	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	16	16	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	976	816	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	656	576	mA	3, 4, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	976	816	mA	3, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	976	816	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		95	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		127	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		32	pF	2
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		32	pF	2
Input/Output Capacitance: DQ1-DQ32	C_{IO}		18	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
READ WRITE cycle time	^{t}RWC	n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	n/a		n/a		ns	22
Access time from $\overline{RAS}$	^{t}RAC		60		70	ns	14
Access time from $\overline{CAS}$	^{t}CAC		15		20	ns	15
Access time from column-address	^{t}AA		30		35	ns	
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40	ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	^{t}RSH	15		20		ns	
$\overline{RAS}$ precharge time	^{t}RP	40		50		ns	
$\overline{CAS}$ pulse width	^{t}CAS	15	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^{t}CSH	60		70		ns	
$\overline{CAS}$ precharge time	^{t}CPN	10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^{t}CP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	45	20	50	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	5		5		ns	
Row-address setup time	^{t}ASR	0		0		ns	
Row-address hold time	^{t}RAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	30	15	35	ns	18
Column-address setup time	^{t}ASC	0		0		ns	
Column-address hold time	^{t}CAH	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	50		55		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		ns	
Read command setup time	^{t}RCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	3		3		ns	25

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	${}^tOFF$	3	15	3	20	ns	20, 25
$\overline{WE}$ command setup time	${}^tWCS$	0		0		ns	
Write command hold time	${}^tWCH$	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	${}^tWCR$	45		55		ns	
Write command pulse width	${}^tWP$	10		15		ns	
Write command to $\overline{RAS}$ lead time	${}^tRWL$	15		20		ns	
Write command to $\overline{CAS}$ lead time	${}^tCWL$	15		20		ns	
Data-in setup time	${}^tDS$	0		0		ns	21
Data-in hold time	${}^tDH$	10		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	${}^tDHR$	45		55		ns	
Transition time (rise or fall)	${}^tT$	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	${}^tREF$		32		32	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	${}^tRPC$	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	${}^tCSR$	5		5		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	${}^tCHR$	15		15		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	${}^tWRH$	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	${}^tWRP$	10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	${}^tWTH$	10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	${}^tWTS$	10		10		ns	24

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS)
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
22. $\overline{OE}$ is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not possible.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.

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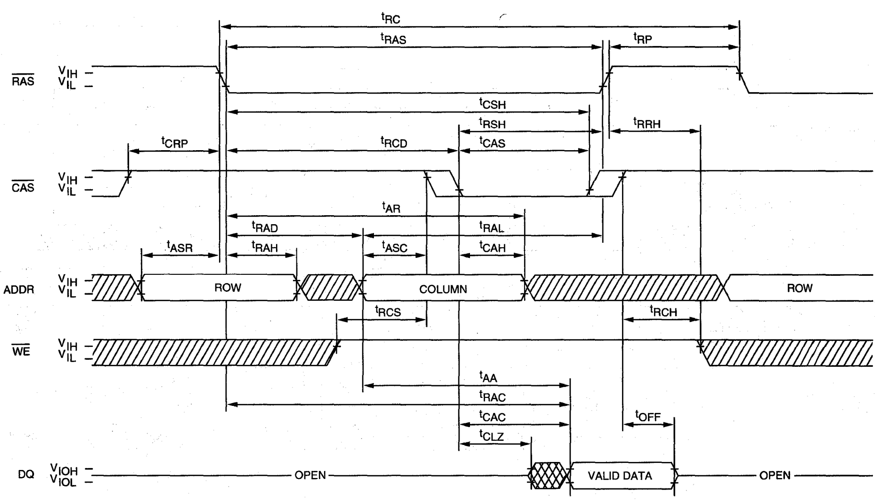
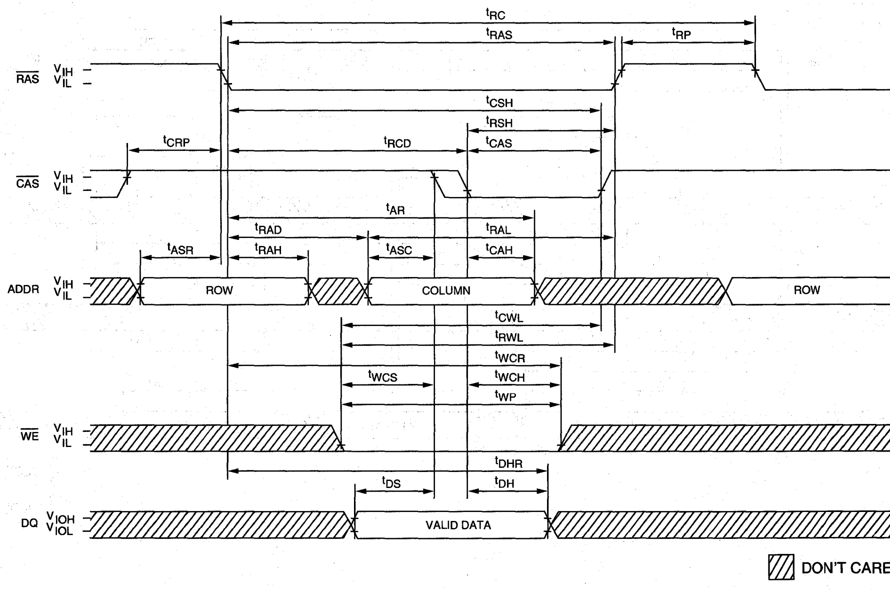
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

DRAM MODULE

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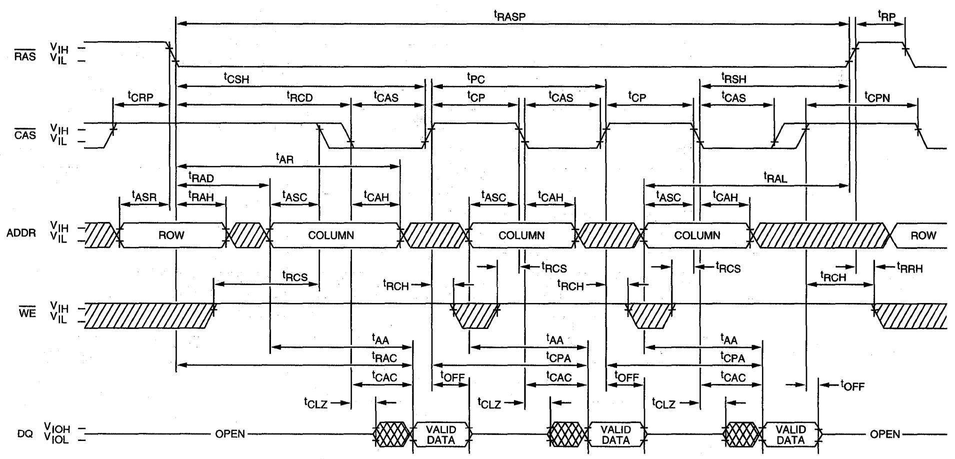
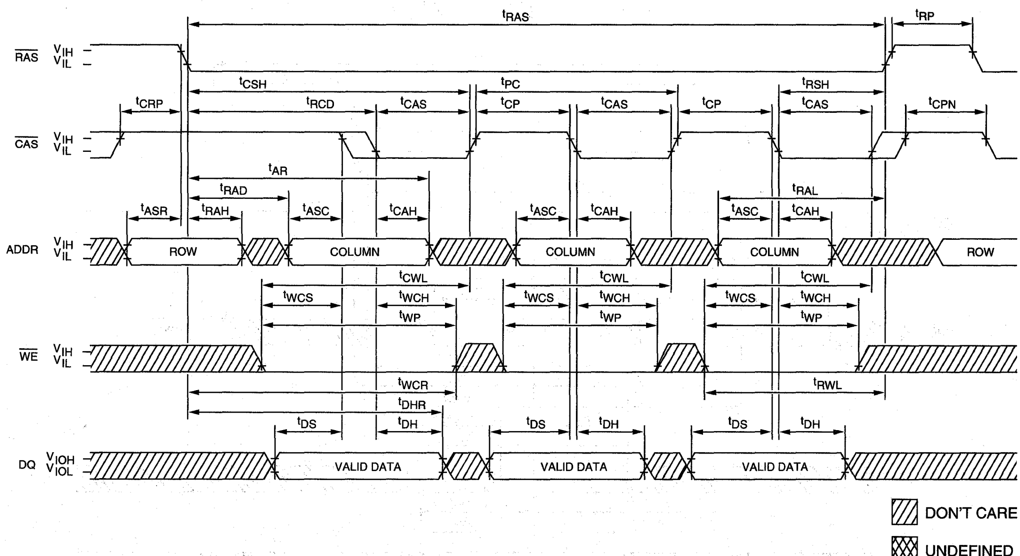
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



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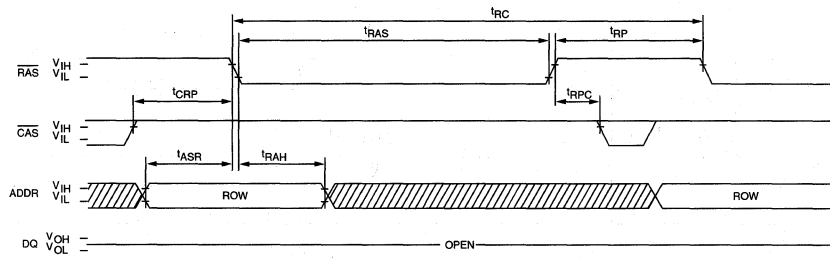
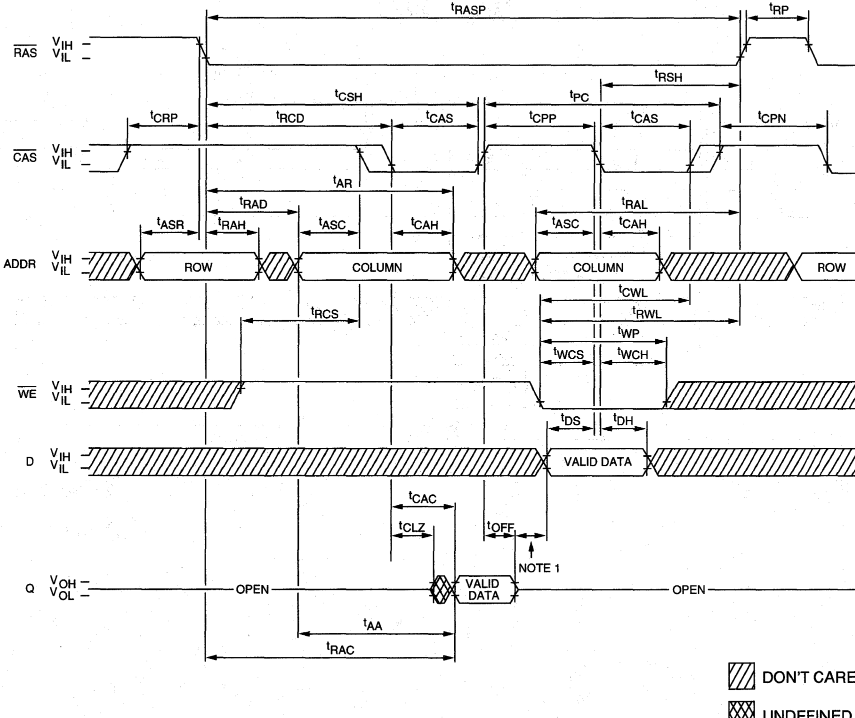
RAS ONLY REFRESH CYCLE
(ADDR = A0-A10; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

DRAM MODULE

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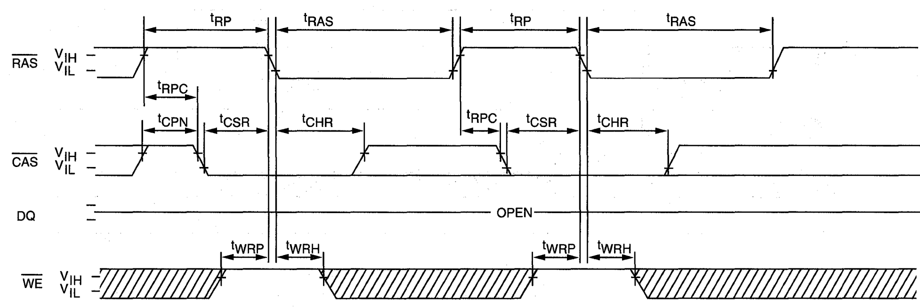
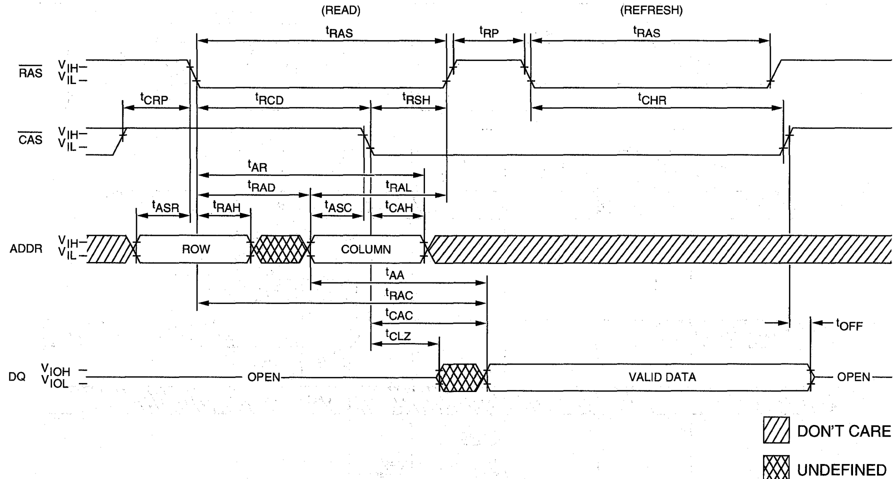
CBR REFRESH CYCLE
(ADDRESSES = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)



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DRAM MODULE

1 MEG x 36, 2 MEG x 18

FAST PAGE MODE (MT12D136)
LOW POWER,
EXTENDED REFRESH (MT12D136 L)

FEATURES

- Industry-standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 36mW (9.2mW L-version) standby; 2,500mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional Extended Refresh
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Multiple $\overline{RAS}$ lines allow x18 or x36 width

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Leadless 72-pin SIMM — M
  - Leadless 72-pin SIMM (gold) — G
  - Leadless 72-pin SIMM low profile — DM
  - Leadless 72-pin SIMM (gold) low profile — DG
- Power/Refresh
  - Normal Power/16ms — Blank
  - Low Power/128ms — L
- Part Number Example: MT12D136G-6 L

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(DE-12)
(DE-18)

MT12D136M/G

1 36 37 72

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

GENERAL DESCRIPTION

The MT12D136 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its

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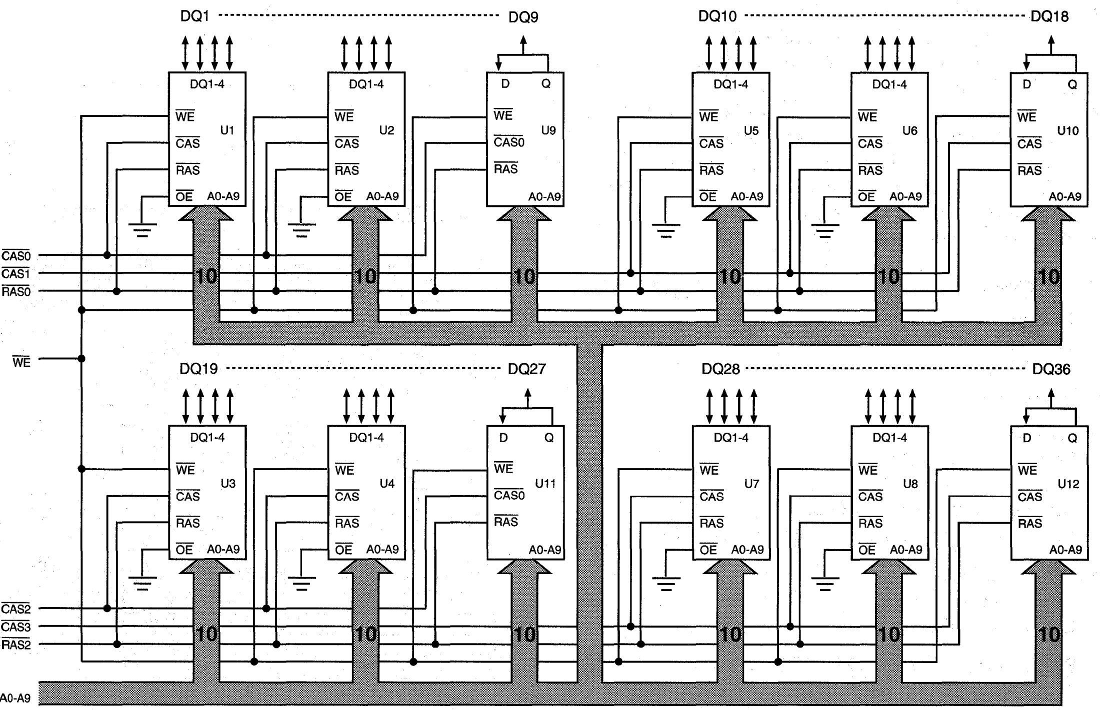
correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

For x18 applications, the corresponding DQ and CAS pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x16 memory organization.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4001JDJ
U9-U12 = MT4C1024DJ
or
U1-U8 = MT4C4001JDJ S (L-version)
U9-U12 = MT4C1024DJ L (L-version)

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TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
EXTENDED CBR REFRESH (L-version)		H→L	L	H	X	X	High-Z

DRAM MODULE

PRESENCE-DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 12W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6, 22) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	I_{I1}	-6	6	µA	
Any input 0V ≤ V_{IN} ≤ 6.5V	A0-A9, $\overline{WE}$	I_{I2}	-24	24	µA	
(All other pins not under test = 0V) for each package input	$\overline{RAS0}$, $\overline{RAS2}$	I_{I3}	-12	12	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ1-DQ36	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	24	24	24	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	12	12	12	mA	
		2.4	2.4	2.4	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	1240	1120	1000	mA	2, 22 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	920	800	680	mA	2, 22 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	1240	1120	1000	mA	22, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	1240	1120	1000	mA	19, 22
REFRESH CURRENT: Extended CBR (L-version only) Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = V_{CC} -0.2; A0-A9 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	3.2	3.2	3.2	mA	19, 22, 24, 27

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		70	pF	17
Input Capacitance: $\overline{\text{WE}}$	C_{I2}		94	pF	17
Input Capacitance: $\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$	C_{I3}		50	pF	17
Input Capacitance: $\overline{\text{CAS0}}$, $\overline{\text{CAS1}}$, $\overline{\text{CAS2}}$, $\overline{\text{CAS3}}$	C_{I4}		25	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{\text{RAS}}$	^tRAC		60		70		80	ns	8
Access time from $\overline{\text{CAS}}$	^tCAC		15		20		20	ns	9
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{\text{CAS}}$ precharge	^tCPA		35		40		45	ns	
$\overline{\text{RAS}}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ hold time	^tRSH	15		20		20		ns	
$\overline{\text{RAS}}$ precharge time	^tRP	40		50		60		ns	
$\overline{\text{CAS}}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{\text{CAS}}$ hold time	^tCSH	60		70		80		ns	
$\overline{\text{CAS}}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{\text{CAS}}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	^tRCD	20	45	20	50	20	60	ns	13
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{\text{RAS}}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	23
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{\text{RAS}}$)	^tAR	45		50		55		ns	
Column-address to $\overline{\text{RAS}}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{\text{CAS}}$)	^tRCH	0		0		0		ns	14

DRAM MODULE

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	14
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	tOFF	3	20	3	20	3	20	ns	12, 25
WE command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	tREF		16/128*		16/128*		16/128*	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CBR REFRESH)	tCSR	10		10		10		ns	19
CAS hold time (CBR REFRESH)	tCHR	10		15		15		ns	19
WE hold time (CBR REFRESH)	tWRH	10		10		10		ns	28
WE setup time (CBR REFRESH)	tWRP	10		10		10		ns	28
WE hold time (WCBR test cycle)	tWTH	10		10		10		ns	28
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	28

*L-version only

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NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on all 4 Meg DRAMs.
22. I_{CC} is dependent on cycle rates.
23. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
24. Applies to L-version only.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.
27. Extended refresh current is reduced as ^tRAS is reduced from its maximum specification during the extended refresh cycle.
28. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.

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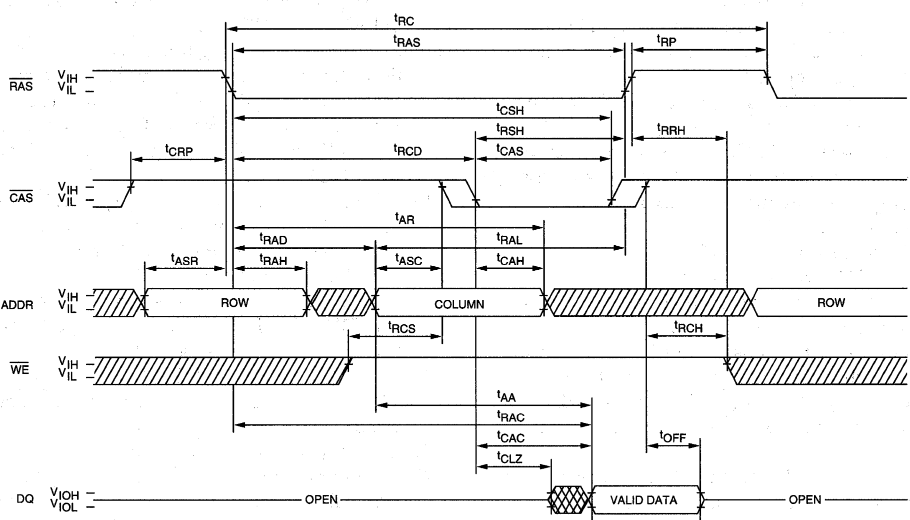
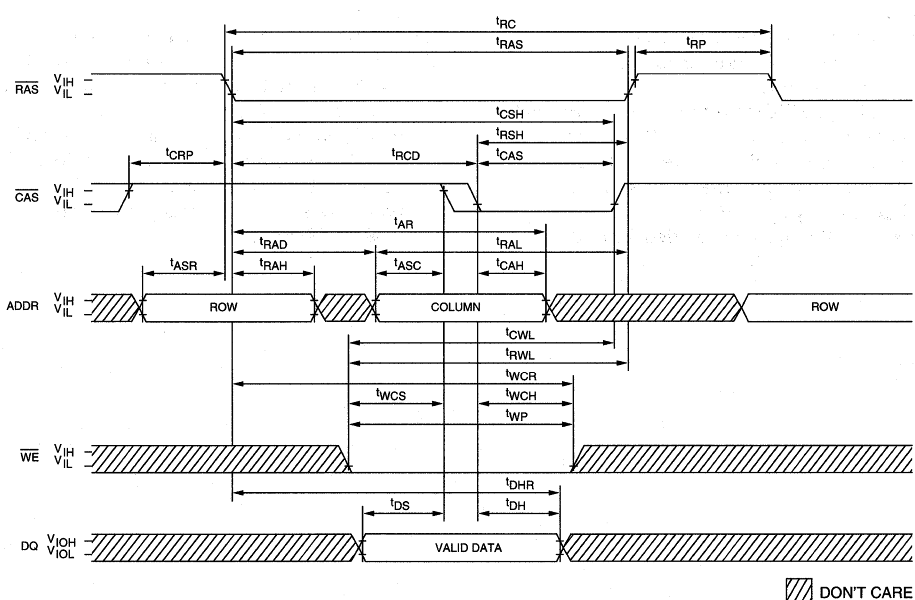
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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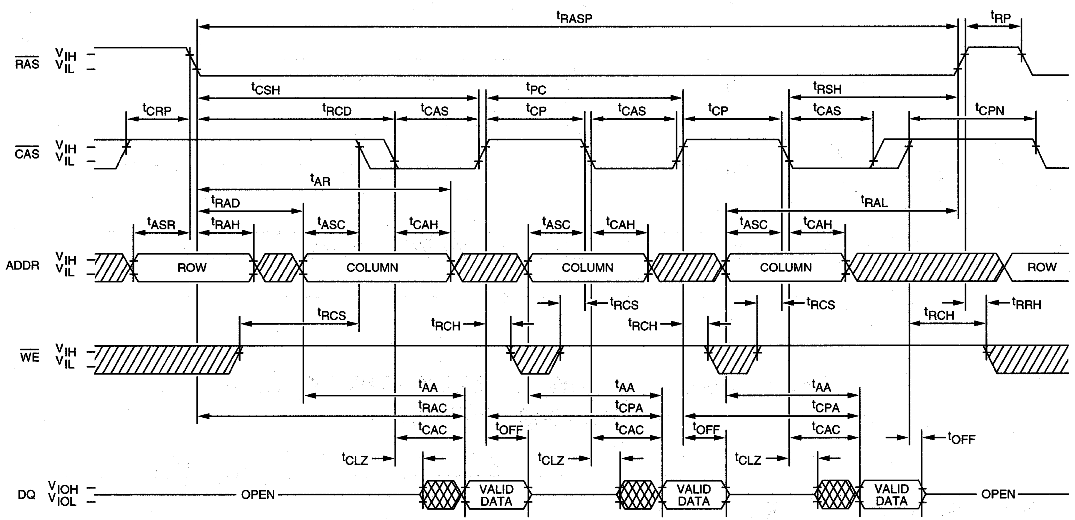
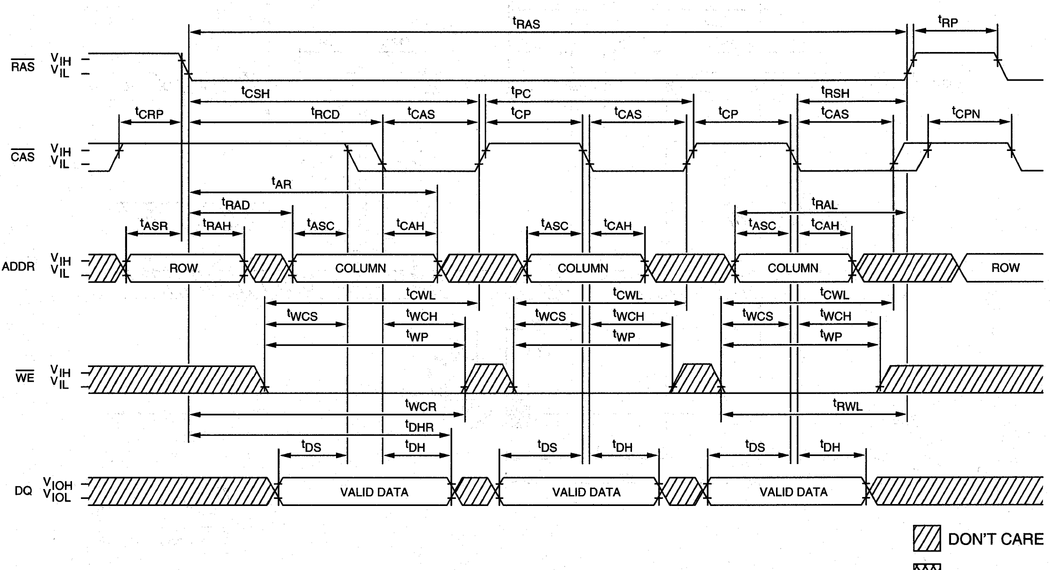
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

DRAM MODULE

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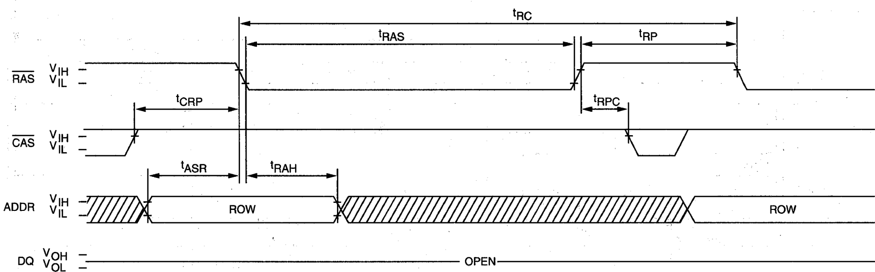
DRAM MODULE

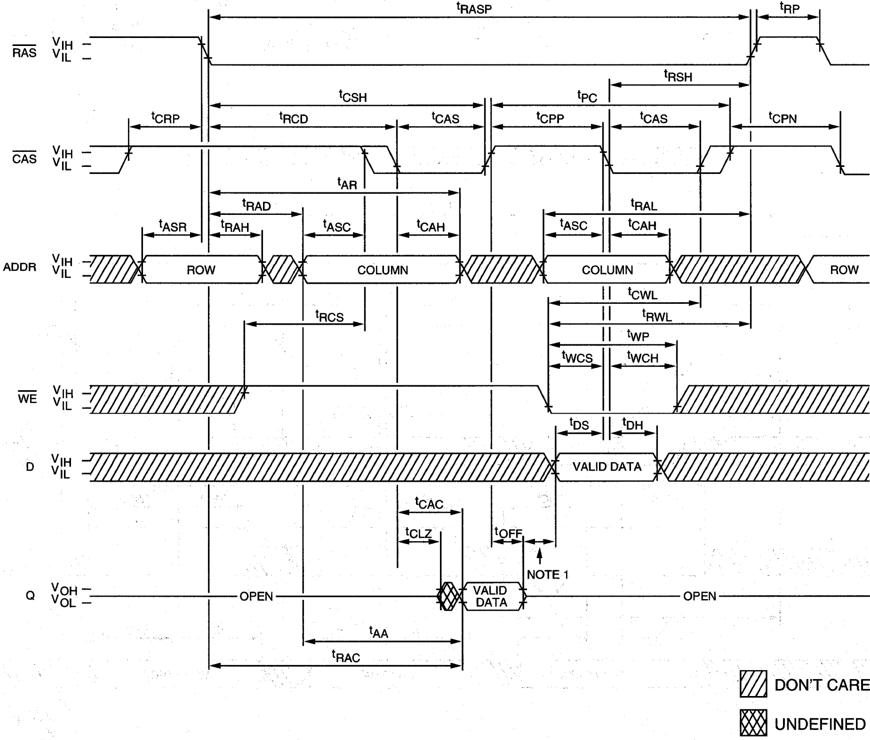
RAS ONLY REFRESH CYCLE

(ADDR = A0-A9; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE:
1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

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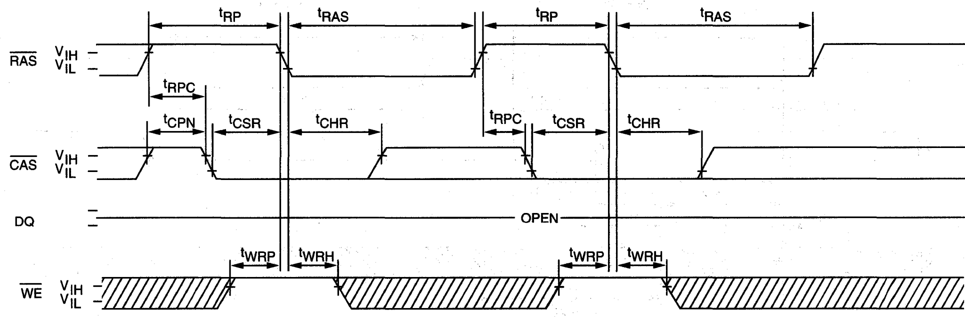
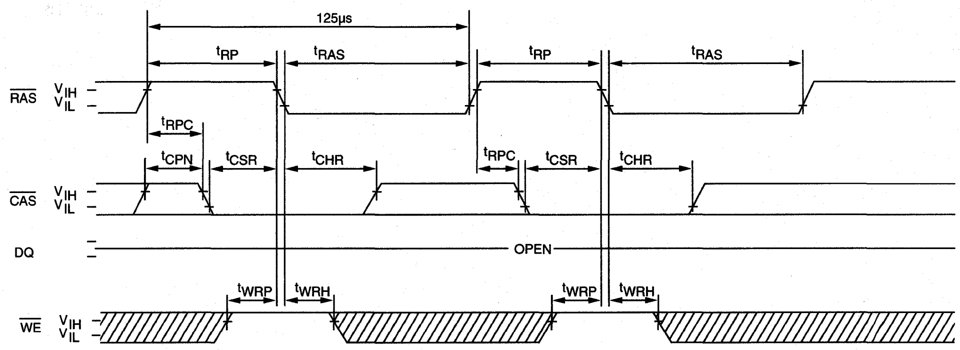
CBR REFRESH CYCLE
(A0-A9 = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [24]
(A0-A9 = DON'T CARE)



DON'T CARE

UNDEFINED

DRAM MODULE

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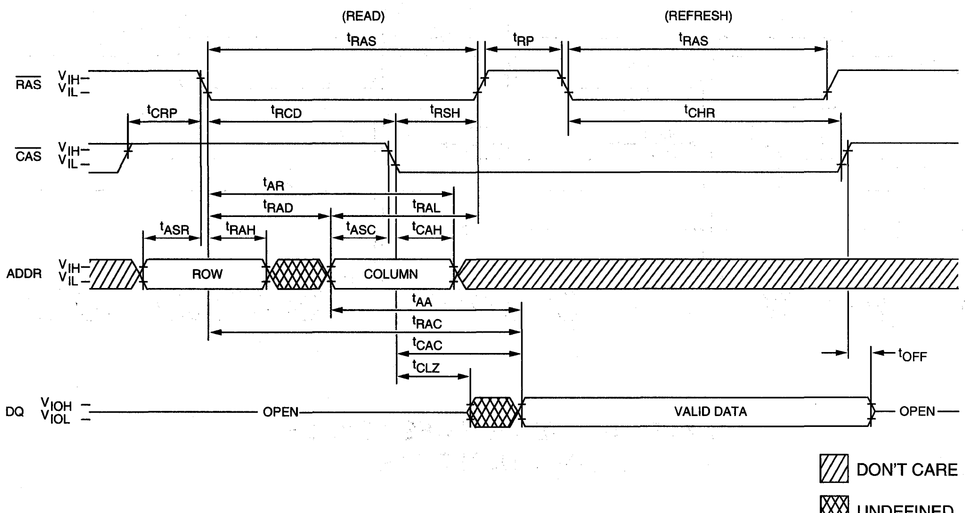
HIDDEN REFRESH CYCLE [20]

(WE = HIGH)



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DRAM MODULE

2 MEG x 36, 4 MEG x 18

FAST PAGE MODE (MT24D236)
LOW POWER,
EXTENDED REFRESH (MT24D236 L)

FEATURES

- Industry-standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 72mW (18.4mW L-version) standby; 2,536mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional Extended Refresh
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Multiple $\overline{RAS}$ lines allow x18 or x36 width

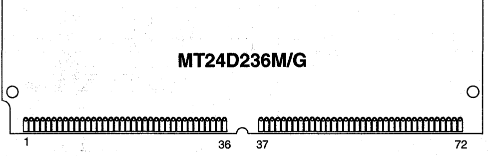
OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (gold)	G
• Power/Refresh	
Normal Power/16ms	Blank
Low Power/128ms	L

- Part Number Example: MT24D236G-6 L

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(DE-13)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	$\overline{RAS1}$	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	$\overline{RAS3}$	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

DRAM MODULE

GENERAL DESCRIPTION

The MT24D236 is a randomly accessed solid-state memory containing 2,097,152 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its

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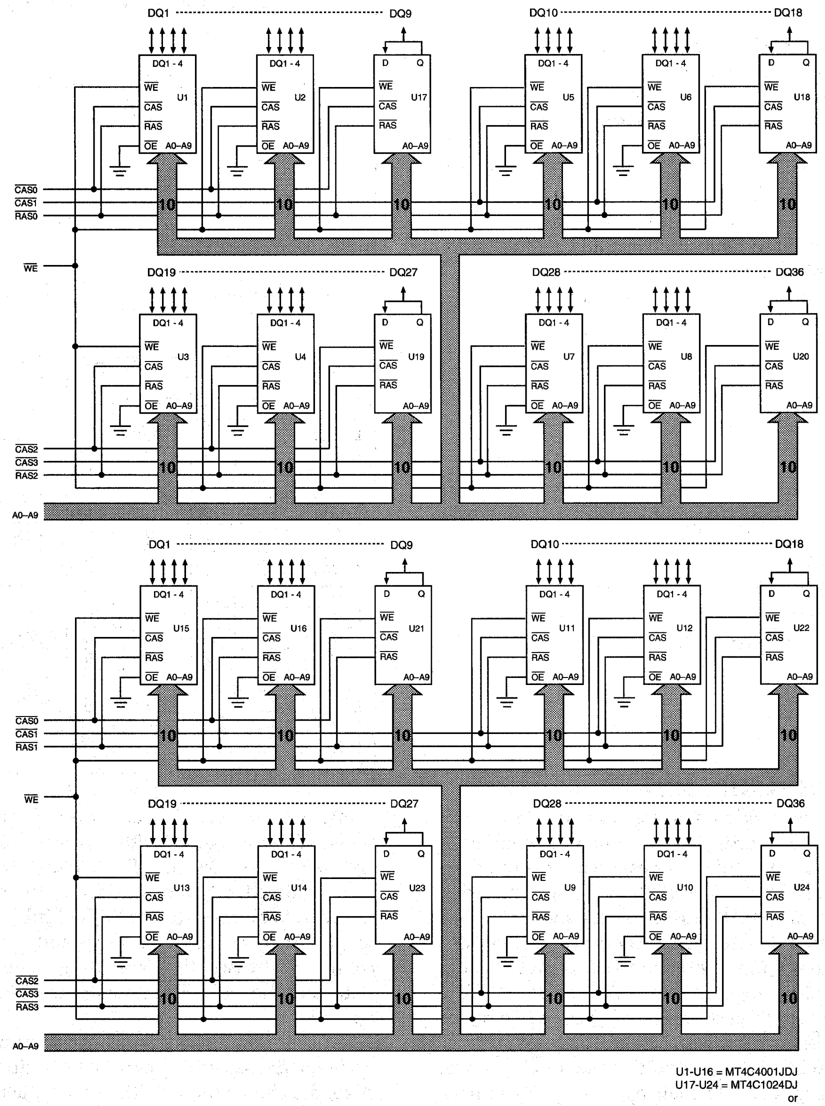
correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE) or $\overline{\text{RAS}}$ REFRESH cycle ($\overline{\text{RAS}}$ ONLY, CBR or HIDDEN) so that all 1,024 combinations of $\overline{\text{RAS}}$ addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

For x18 applications, the corresponding DQ and $\overline{\text{CAS}}$ pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and $\overline{\text{CAS0}}$ to $\overline{\text{CAS2}}$ and $\overline{\text{CAS1}}$ to $\overline{\text{CAS3}}$). Each $\overline{\text{RAS}}$ is then a bank select for the x18 memory organization.

FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ${}^tR$	ADDRESSES ${}^tC$	DATA-IN/OUT DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
Extended CBR REFRESH (L-version)		H→L	L	H	X	X	High-Z

DRAM MODULE

PRESENCE-DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 24W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6, 22) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	CAS0-CAS3	II1	-12	12	µA	
Any input 0V ≤ VIN ≤ 6.5V	A0-A9, WE	II2	-48	48	µA	
(All other pins not under test = 0V) for each package input	RAS0-RAS3	II3	-12	12	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ36	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	48	48	48	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	ICC2	24	24	24	mA	
		4.8	4.8	4.8	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ᵗRC = ᵗRC [MIN])	ICC3	1264	1144	1024	mA	2, 22, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ᵗPC = ᵗPC [MIN])	ICC4	944	824	704	mA	2, 22, 26
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: ᵗRC = ᵗRC [MIN])	ICC5	1264	1144	1024	mA	22, 26
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: ᵗRC = ᵗRC [MIN])	ICC6	1264	1144	1024	mA	19, 22
REFRESH CURRENT: Extended CBR Average power supply current during Extended Refresh: CAS = 0.2V or CBR cycling; RAS = ᵗRAS (MIN) WE =Vcc -0.2V; A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left open); ᵗRC = 125µs (1,024 rows at 125µs = 128ms)	ICC7	6.4	6.4	6.4	mA	19, 22, 24, 27

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		140	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		188	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		50	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		50	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}		18	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
READ WRITE cycle time	^{t}RWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^{t}RAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^{t}CAC		15		20		20	ns	9
Access time from column-address	^{t}AA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^{t}RSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^{t}RP	40		50		60		ns	
$\overline{CAS}$ pulse width	^{t}CAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^{t}CSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^{t}CPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^{t}CP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	10		10		10		ns	
Row-address setup time	^{t}ASR	0		0		0		ns	
Row-address hold time	^{t}RAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	30	15	35	15	40	ns	23
Column-address setup time	^{t}ASC	0		0		0		ns	
Column-address hold time	^{t}CAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	45		50		55		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		40		ns	
Read command setup time	^{t}RCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		0		ns	14

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	3	20	3	20	3	20	ns	12, 25
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	^tREF		16/128*		16/128*		16/128*	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		15		ns	19
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	28
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	28
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	28
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	28

*L-version only

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NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100μs is required after power-up followed by any eight RAS REFRESH cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
10. If CAS = VIH, data output is High-Z.
11. If CAS = VIL, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to CAS leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to OE being grounded on all 4 Meg DRAMs.
22. Icc is dependent on cycle rates.
23. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
24. Applies to L-version only.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.
27. Extended refresh current is reduced as ^{t}RAS is reduced from its maximum specification during the extended refresh cycle.
28. ^{t}WTS and ^{t}WTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.

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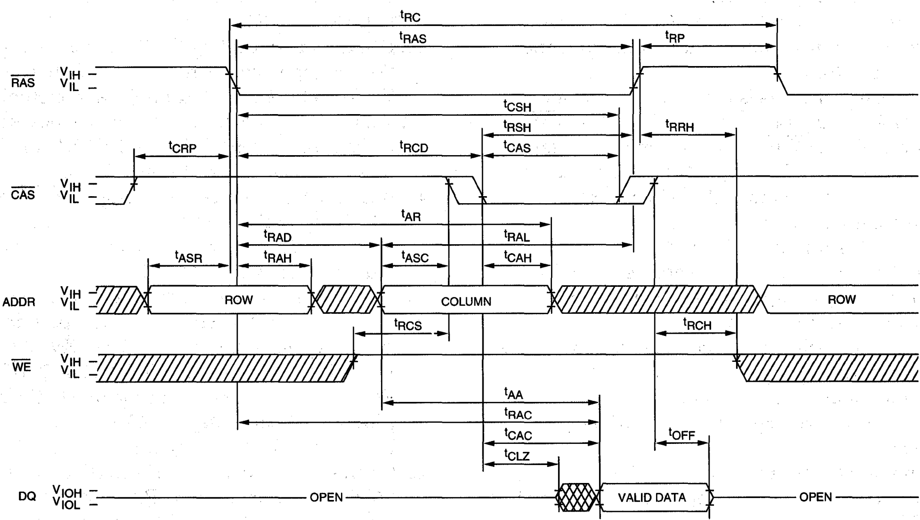
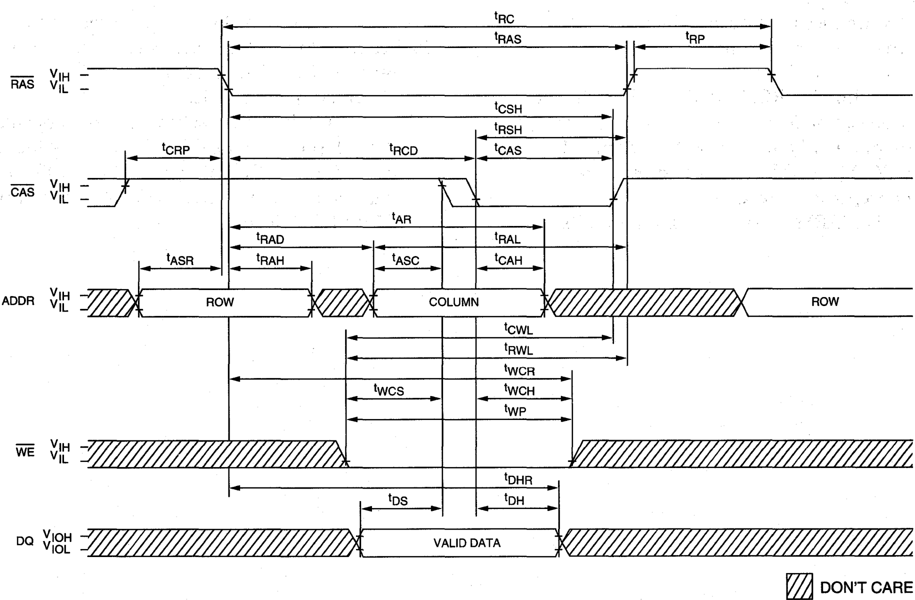
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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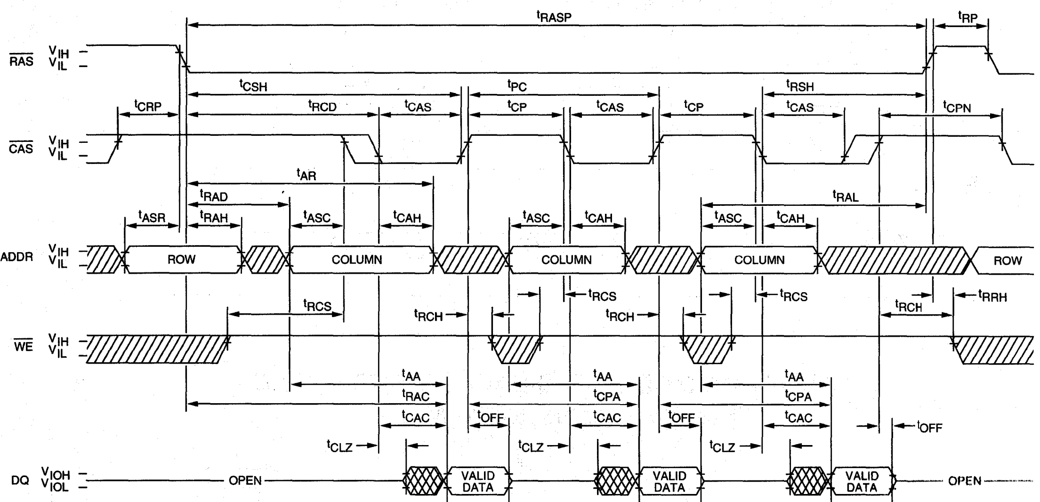
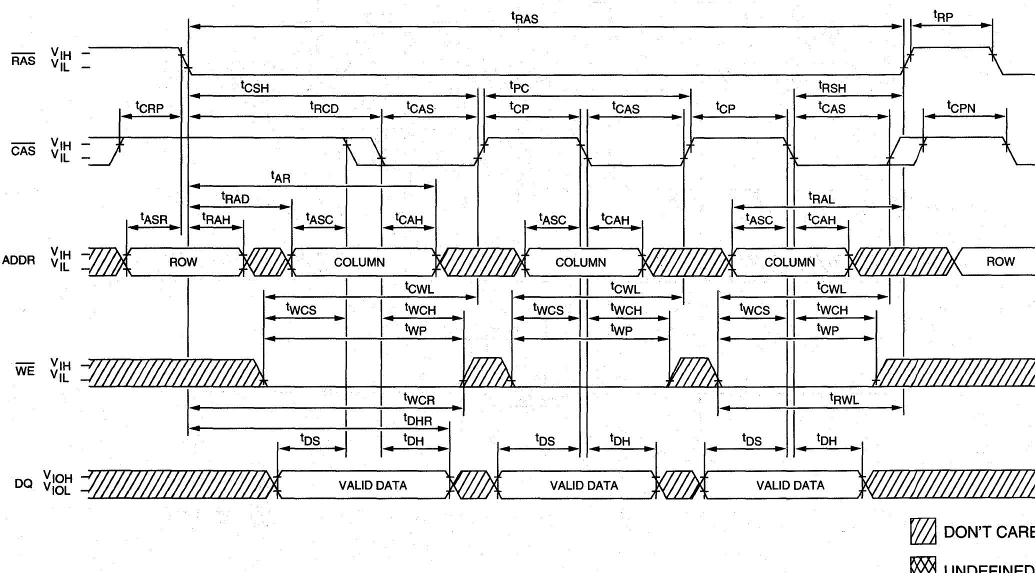
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

DRAM MODULE

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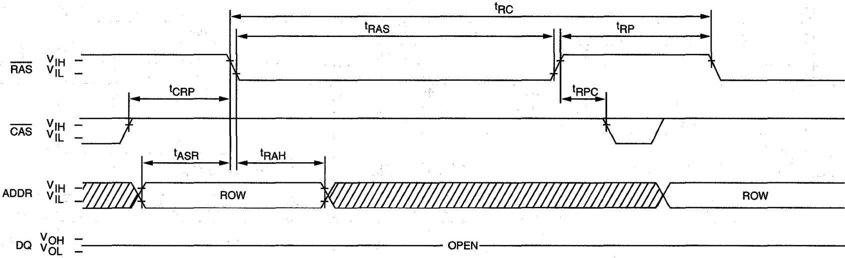
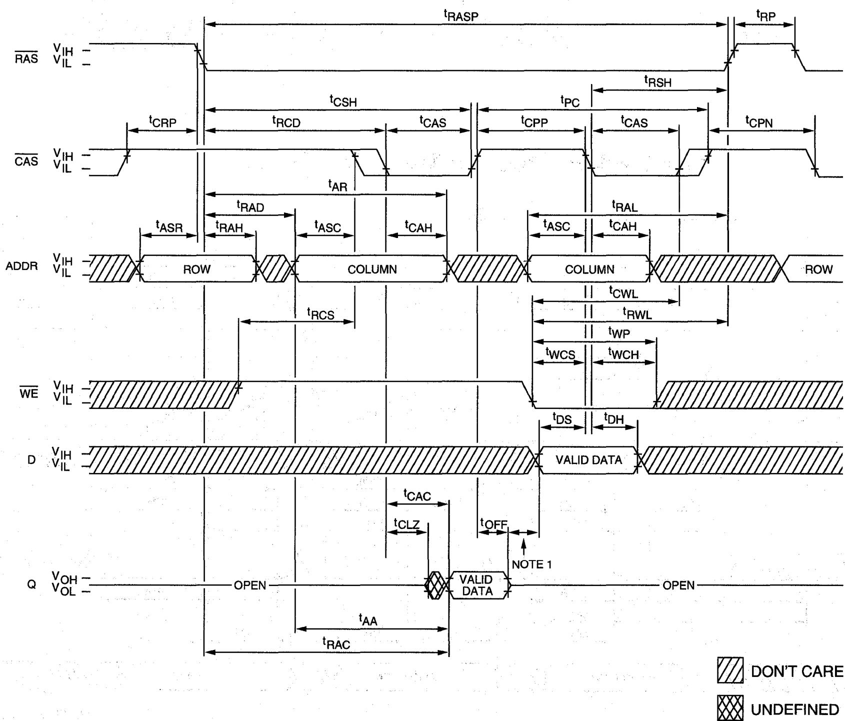
DRAM MODULE

RAS ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE:
1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

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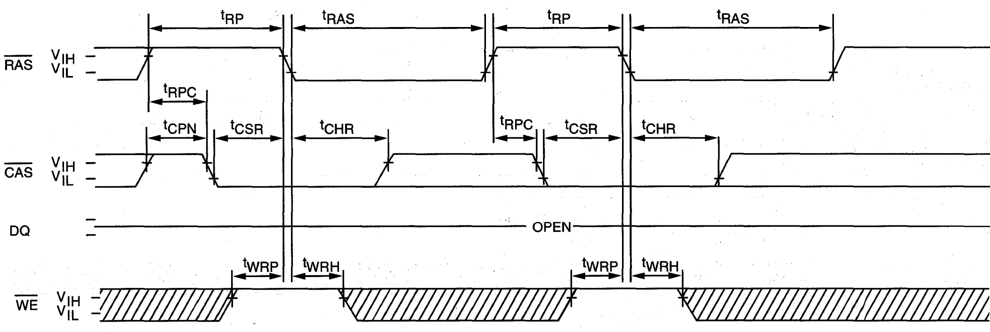
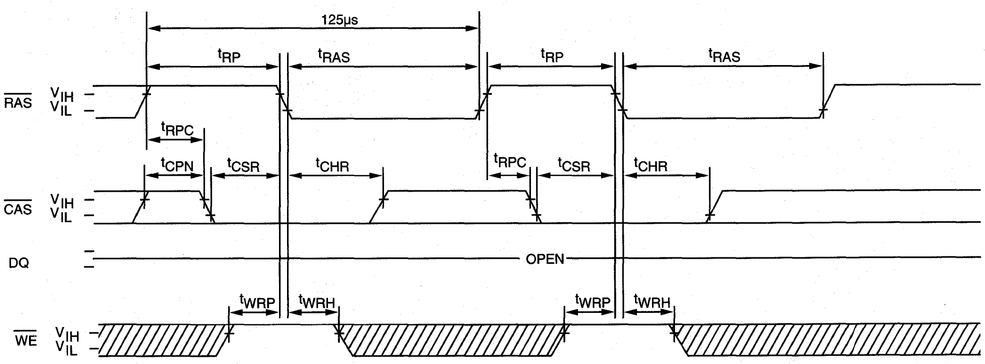
CBR REFRESH CYCLE
(A0-A9 = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [24]
(A0-A9 = DON'T CARE)



DON'T CARE

UNDEFINED

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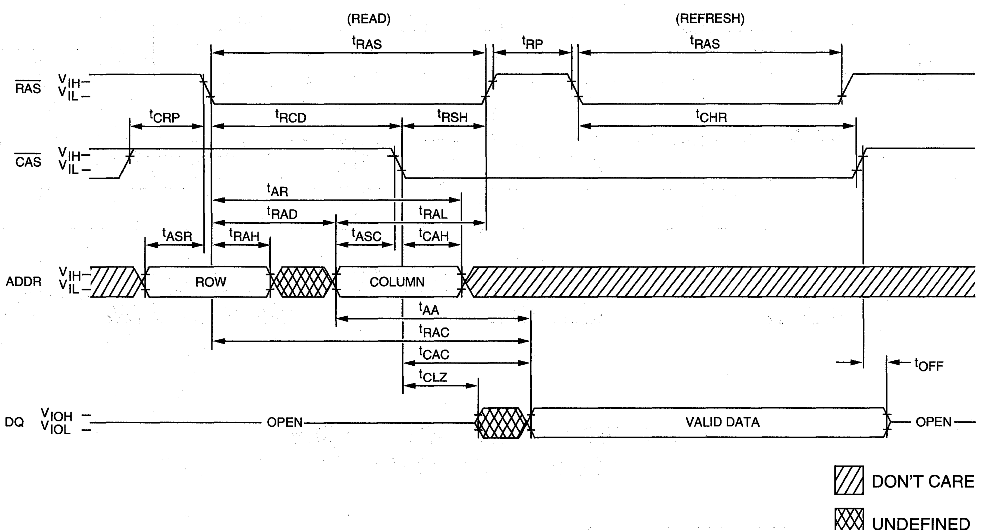
HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



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DRAM MODULE

4 MEG x 36, 8 MEG x 18

FAST PAGE MODE

FEATURES

- Industry-standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon-gate process
- Low profile (1.00" height) DM and DG packages only
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 36mW standby; 2,500mW active, typical
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE access cycle
- Multiple RAS lines allow x18 or x36 width

OPTIONS — MARKING

- Timing
  - 60ns access: -6
  - 70ns access: -7
- Packages
  - Leadless 72-pin SIMM: M
  - Leadless 72-pin SIMM (gold): G
  - Leadless 72-pin SIMM low profile: DM
  - Leadless 72-pin SIMM (gold) low profile: DG
- Part Number Example: MT12D436DG-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(DE-14)
(DE-18)

MT12D436DM/G

1 36 37 72

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CAS0	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	RAS2	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

GENERAL DESCRIPTION

The MT12D436 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

For x18 applications, the corresponding DQ and CAS pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x18 memory organization.

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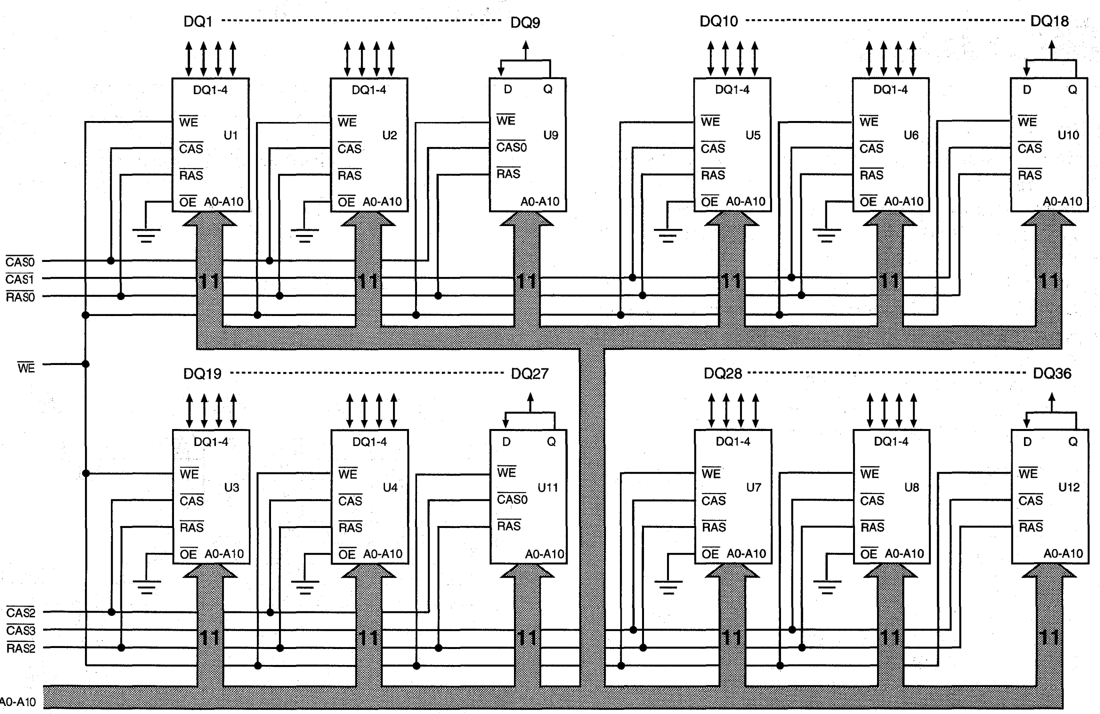
FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4M4B1
U9-U12 = MT4C1004J

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ${}^tR$	ADDRESSES ${}^tC$	DATA-IN/OUT DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

DRAM MODULE

PRESENCE-DETECT

SYMBOL	-6	-7
PRD1	Vss	Vss
PRD2	NC	NC
PRD3	NC	Vss
PRD4	NC	NC

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 12W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	RAS0, RAS2	II1	-12	12	µA	
Any input 0V ≤ VIN ≤ 6.5V	A0-A10, WE	II2	-24	24	µA	
(All other pins not under test = 0V) for each package input	CAS0-CAS3	II3	-6	6	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ36	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	24	24	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	ICC2	12	12	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	1400	1200	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])	ICC4	960	840	mA	3, 4, 26
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])	ICC5	1400	1200	mA	3, 26
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC6	1400	1200	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		70	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		94	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		50	pF	2
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		25	pF	2
Input/Output Capacitance: DQ1-DQ36	C_{IO}		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		ns	22
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15
Access time from column-address	^tAA		30		35	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		ns	
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 25
$\overline{WE}$ command setup time	^tWCS	0		0		ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
Write command pulse width	^tWP	10		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in setup time	^tDS	0		0		ns	21
Data-in hold time	^tDH	10		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	^tREF		32		32	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		ns	24

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
22. $\overline{OE}$ is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not possible.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.

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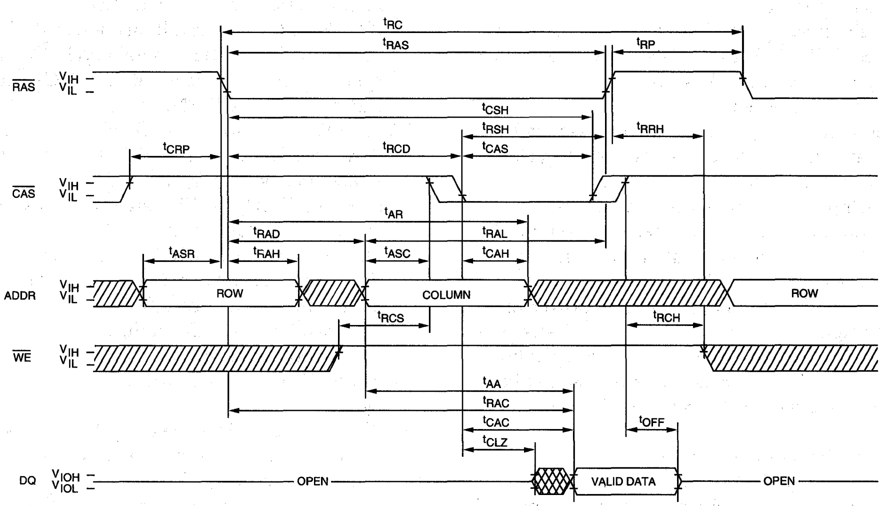
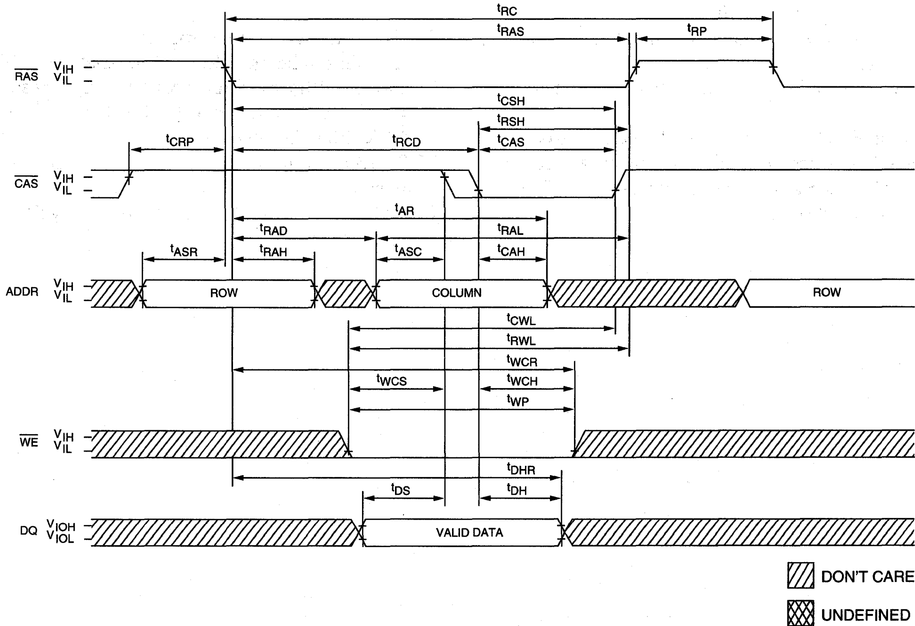
DRAM MODULE

READ CYCLE



EARLY WRITE CYCLE



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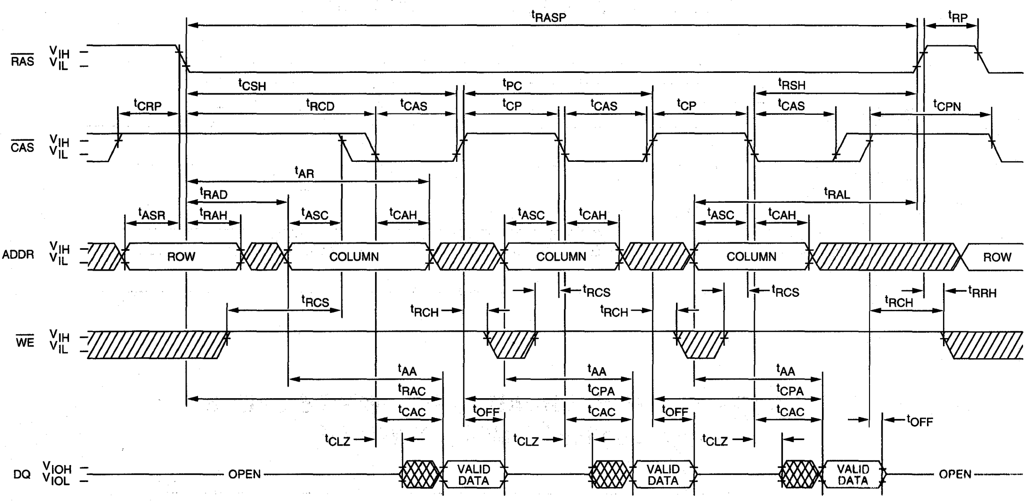
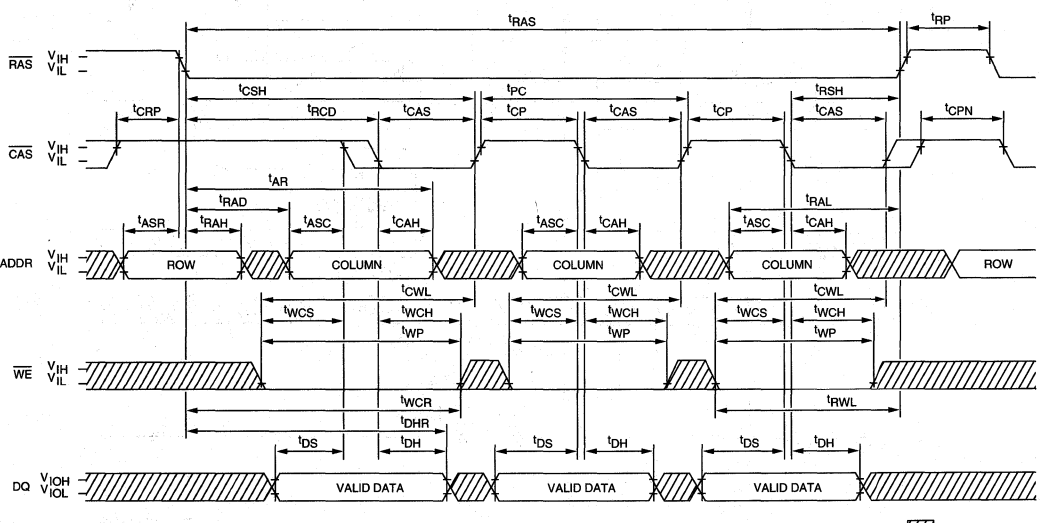
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

DRAM MODULE

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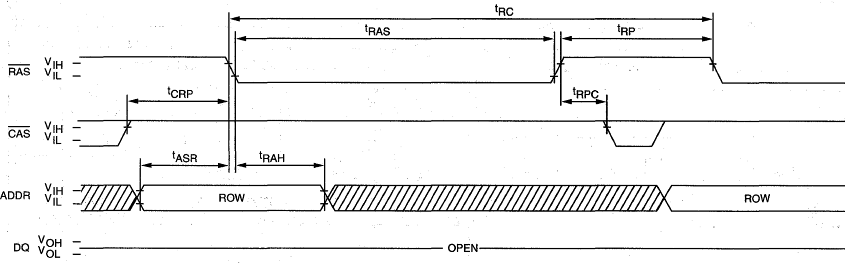
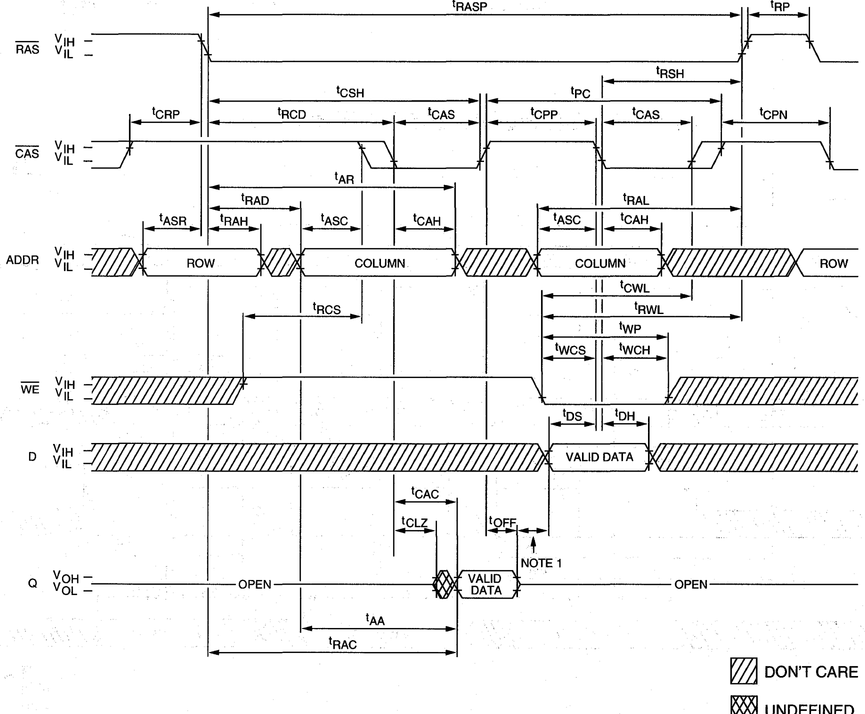
RAS ONLY REFRESH CYCLE
(ADDR = A0-A10; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE:
1. Do not drive data prior to tristate: ^{t}CPP(MIN) or ^{t}CP(whichever is greater) + ^{t}DS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

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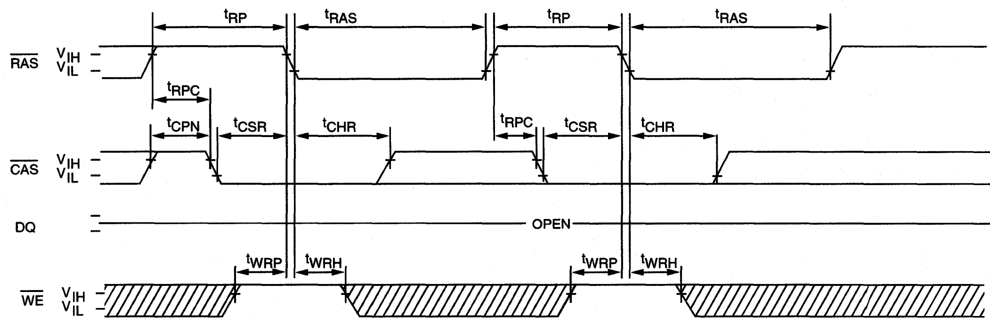
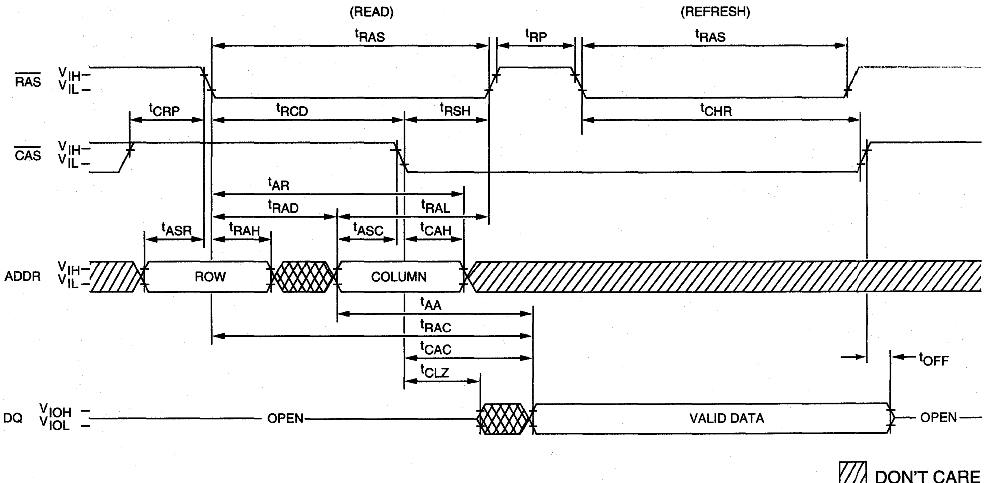
CBR REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE 23
($\overline{WE}$ = HIGH)



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DRAM MODULE

4 MEG x 36 DRAM

FAST PAGE MODE (MT36D436)
LOW POWER,
EXTENDED REFRESH (MT36D436 L)

FEATURES

- Industry-standard pinout in a 72-pin small-outline-single in-line package
- High-performance CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 108mW (29mW L-version) standby; 8,100mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional Extended Refresh
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE access cycle

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
72-pin SIMM	M
72-pin SIMM (gold)	G
• Power/Refresh	
Normal Power/16ms	Blank
Low Power/128ms	L

- Part Number Example: MT36D436M-6 L

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(DE-21)

MT36D436

1 36 37 72

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

GENERAL DESCRIPTION

The MT36D436 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

REFRESH

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

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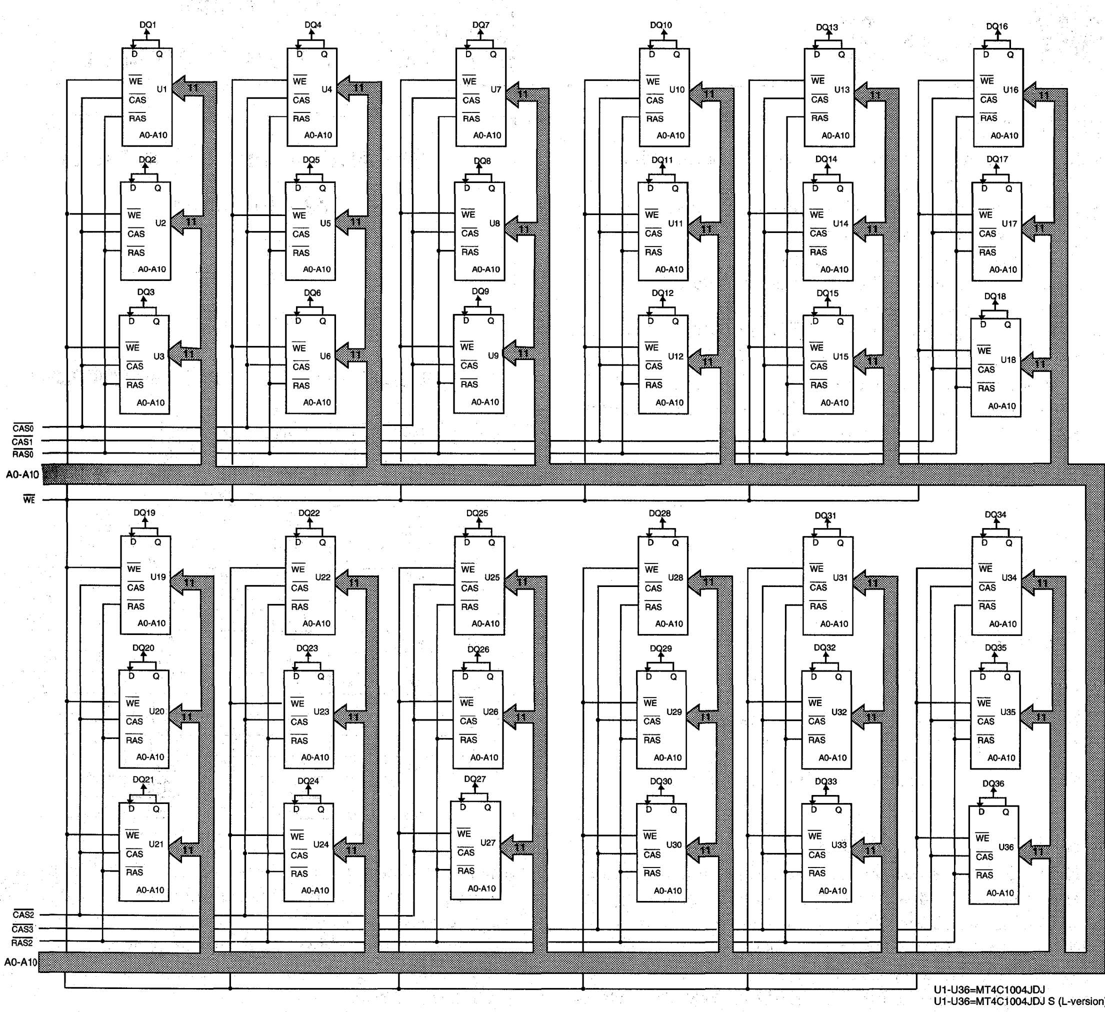
FUNCTIONAL BLOCK DIAGRAM



U1-U36=MT4C1004JDJ
U1-U36=MT4C1004JDJ S (L-version)

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ${}^tR$	ADDRESSES ${}^tC$	DATA-IN/OUT DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
Extended CBR REFRESH (L-version)		H→L	L	H	X	X	High-Z

NEW DRAM MODULE

PRESENCE-DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 36W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6, 22) (V_{CC} = 5V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{RAS0}$, $\overline{RAS2}$	I_{I1}	-36	36	µA	
Any input 0V ≤ V_{IN} ≤ 6.5V	A0-A10, $\overline{WE}$	I_{I2}	-72	72	µA	
(All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS3}$	I_{I3}	-18	18	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ1-DQ36	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	72	72	72	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	36	36	36	mA	
		7.2	7.2	7.2	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC3}	3,960	3,600	3,240	mA	2, 22, 27
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ${}^tPC$ = ${}^tPC$ [MIN])	I_{CC4}	2,880	2,520	2,160	mA	2, 22, 27
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC5}	3,960	3,600	3,240	mA	2, 27
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC6}	3,960	3,600	3,240	mA	2, 19
REFRESH CURRENT: Extended CBR (L-version only) Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ${}^tRAS$ (MIN); $\overline{WE}$ = Vcc -0.2V; A0-A10 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ${}^tRC$ = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	10.8	10.8	10.8	mA	2, 4, 19, 24, 26

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	200	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}	272	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}	132	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}	66	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}	14	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	23
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14

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NEW DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	3	15	3	20	3	20	ns	12, 25
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	^tREF		16/128*		16/128*		16/128*	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	19
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	28
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	28
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	28
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	28

*L-version only

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NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
10. If $\overline{CAS}$ = VIH, data output is High-Z.
11. If $\overline{CAS}$ = VIL, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available.
22. Icc is dependent on cycle rates.
23. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
24. Applies to L-version only.
25. The 3ns minimum is a parameter guaranteed by design.
26. Extended refresh current is reduced as ^{t}RAS is reduced from its maximum specification during the extended refresh cycle.
27. Column-address changed once each cycle.
28. Extended refresh current is reduced as ^{t}RAS is reduced from its maximum specification during the extended refresh cycle.

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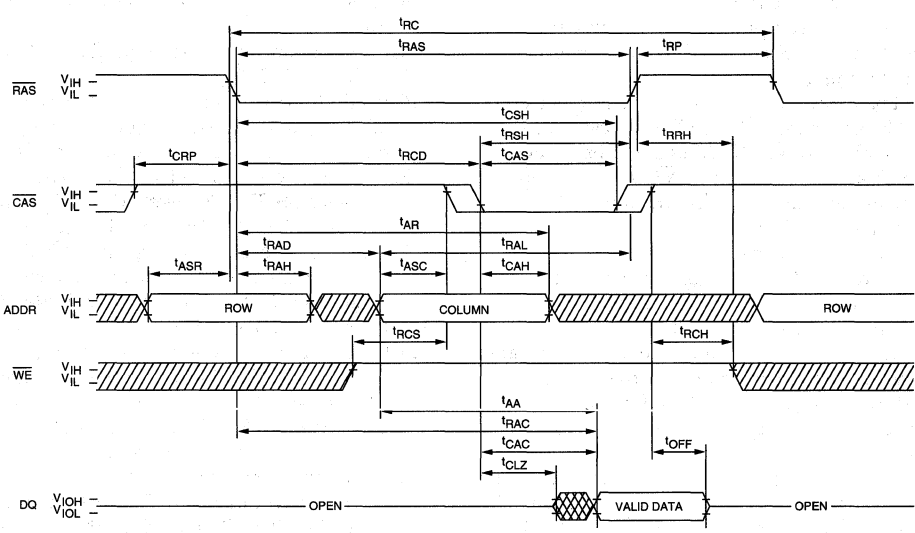
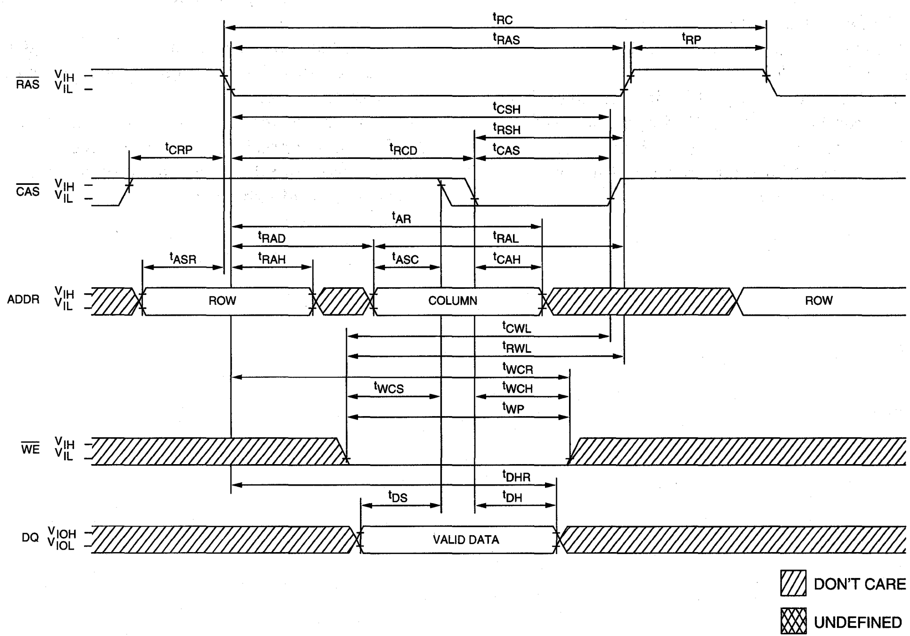
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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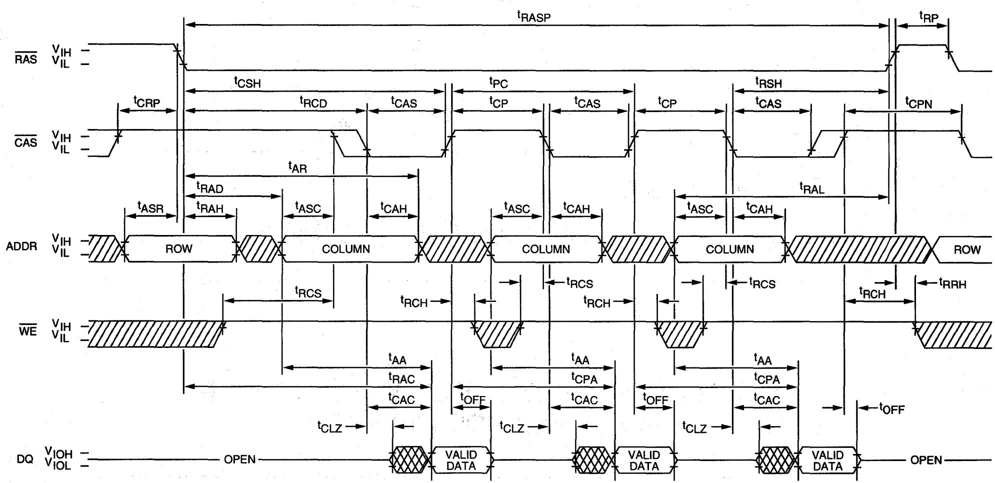
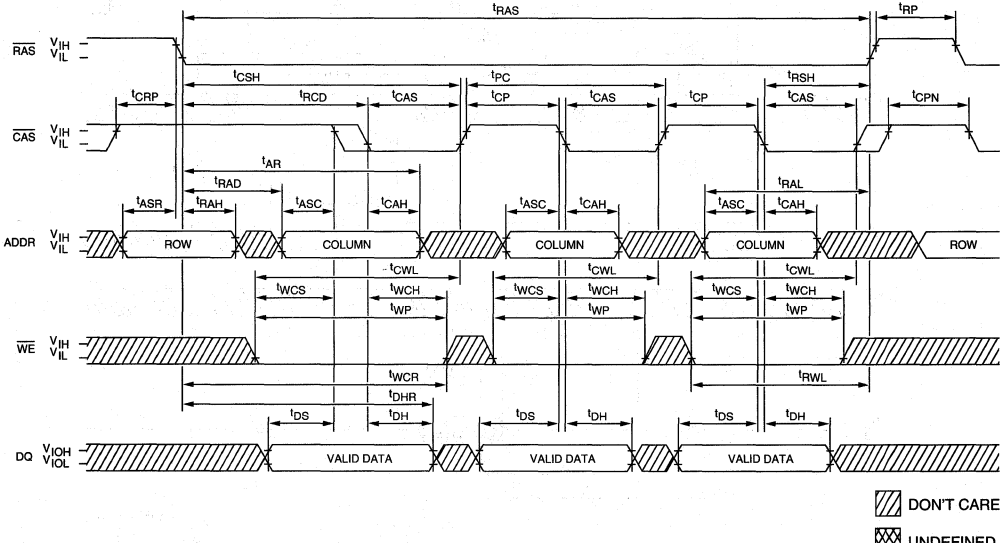
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



NEW DRAM MODULE

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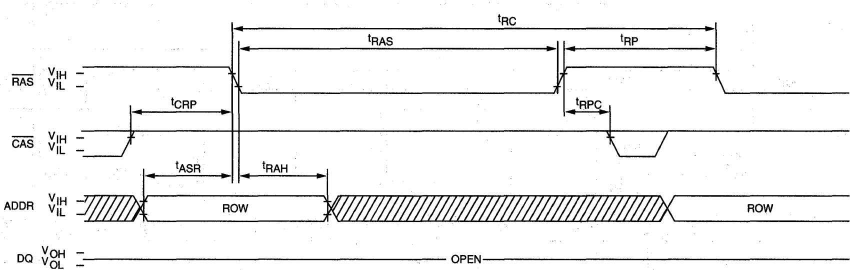
NEW DRAM MODULE

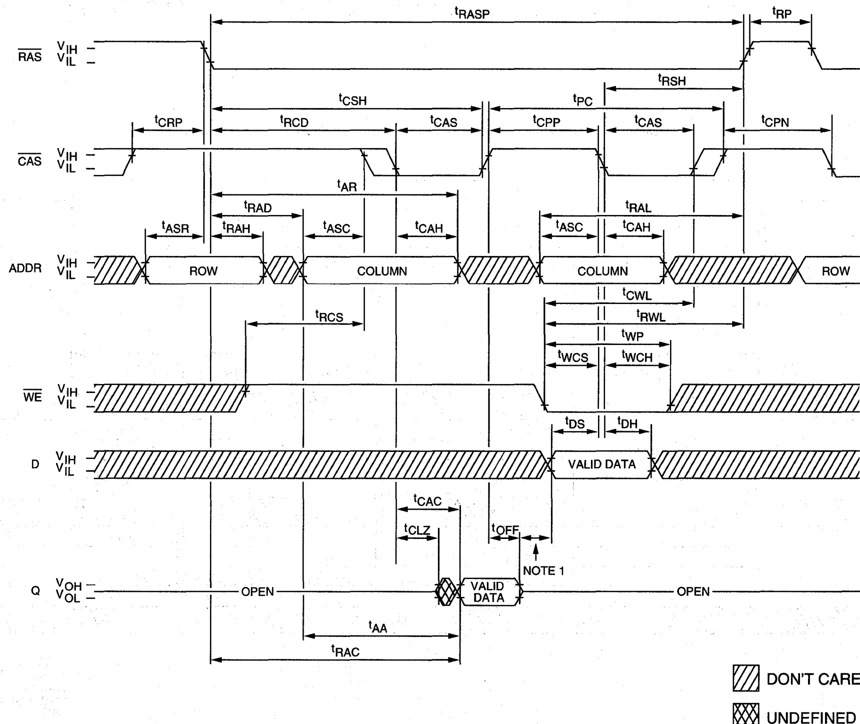
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A0-A9; A10 and $\overline{WE}$ = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE:
1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

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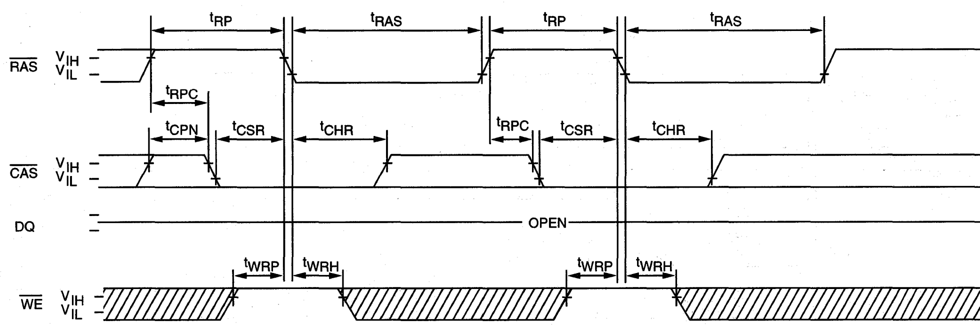
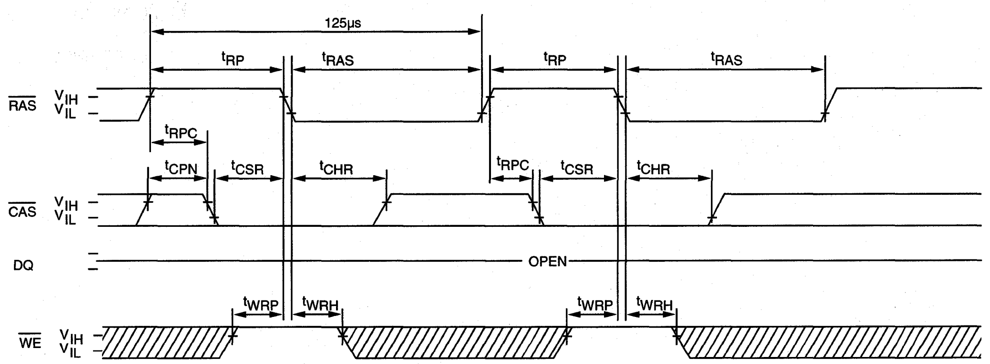
CBR REFRESH CYCLE
(A0-A10 = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [24]
(A0-A10 = DON'T CARE)



DON'T CARE

UNDEFINED

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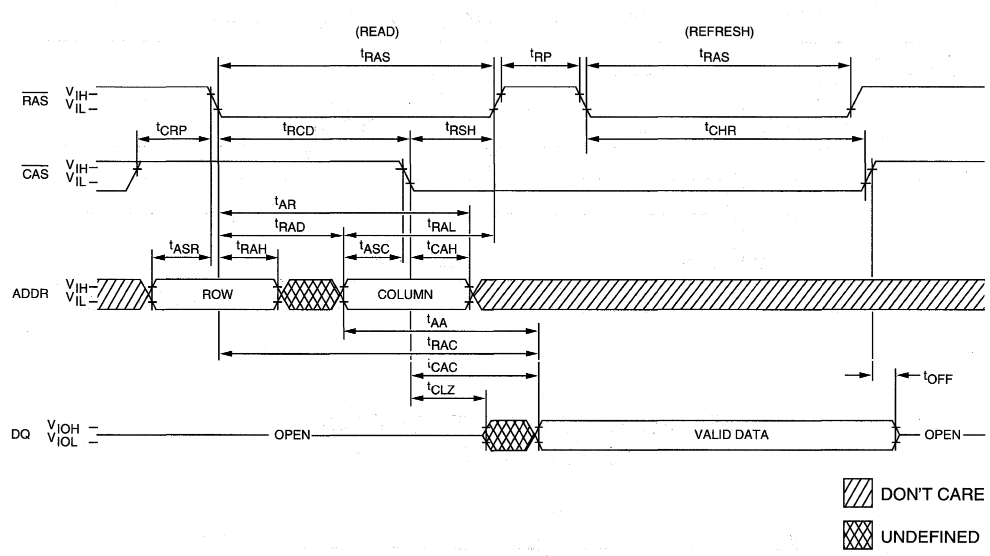
HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



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DRAM MODULE

8 MEG x 36,16 MEG x18
FAST PAGE MODE

FEATURES

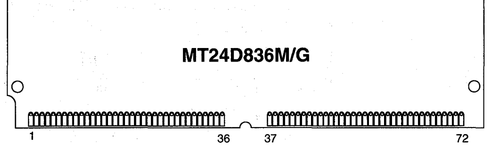
- Industry-standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 72mW standby; 2,536mW active, typical
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE access cycle
- Multiple RAS lines allow x18 or x36 widths

OPTIONS — MARKING

- Timing
  - 60ns access: -6
  - 70ns access: -7
- Packages
  - Leadless 72-pin SIMM: M
  - Leadless 72-pin SIMM (gold): G
- Part Number Example: MT24D836G-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(DE-15)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CAS0	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	RAS1	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	RAS3	51	DQ11	69	PRD3
16	A4	34	RAS2	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

GENERAL DESCRIPTION

The MT24D836 is a randomly accessed solid-state memory containing 8,388,608 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

For x18 applications, the corresponding DQ and CAS pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x18 memory organization.

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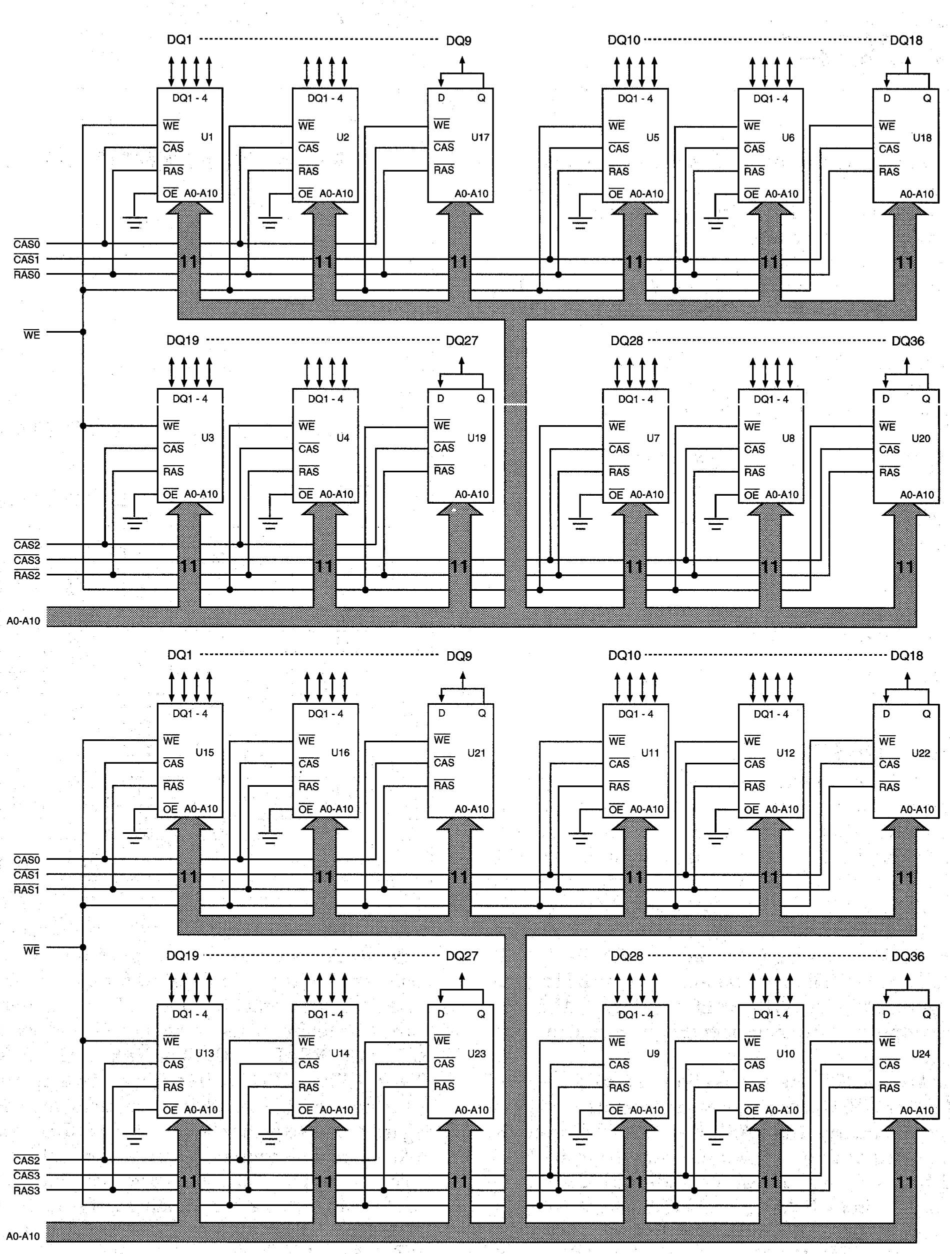
DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

PRESENCE-DETECT

SYMBOL	-6	-7
PRD1	NC	NC
PRD2	Vss	Vss
PRD3	NC	Vss
PRD4	NC	NC

DRAM MODULE

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 24W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	RAS0-RAS3	II1	-12	12	µA	
Any input 0V ≤ VIN ≤ 6.5V	A0-A10, WE	II2	-48	48	µA	
(All other pins not under test = 0V) for each package input	CAS0-CAS3	II3	-12	12	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ36	IOZ	-20	20	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	48	48	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	ICC2	24	24	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^{t}RC = ^{t}RC [MIN])	ICC3	1424	1224	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^{t}PC = ^{t}PC [MIN])	ICC4	984	864	mA	3, 4, 26
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: ^{t}RC = ^{t}RC [MIN])	ICC5	1424	1224	mA	3, 26
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: ^{t}RC = ^{t}RC [MIN])	ICC6	1424	1224	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		140	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		188	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		50	pF	2
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		50	pF	2
Input/Output Capacitance: DQ1-DQ36	C_{IO}		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
READ WRITE cycle time	^{t}RWC	n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	$^{t}PRWC$	n/a		n/a		ns	22
Access time from $\overline{RAS}$	^{t}RAC		60		70	ns	14
Access time from $\overline{CAS}$	^{t}CAC		15		20	ns	15
Access time from column-address	^{t}AA		30		35	ns	
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40	ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	$^{t}RASP$	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	^{t}RSH	15		20		ns	
$\overline{RAS}$ precharge time	^{t}RP	40		50		ns	
$\overline{CAS}$ pulse width	^{t}CAS	15	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^{t}CSH	60		70		ns	
$\overline{CAS}$ precharge time	^{t}CPN	10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^{t}CP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	45	20	50	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	10		10		ns	
Row-address setup time	^{t}ASR	0		0		ns	
Row-address hold time	^{t}RAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	30	15	35	ns	18
Column-address setup time	^{t}ASC	0		0		ns	
Column-address hold time	^{t}CAH	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	50		55		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		ns	
Read command setup time	^{t}RCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	3		3		ns	25

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	tOFF	3	15	3	20	ns	20, 25
WE command setup time	tWCS	0		0		ns	
Write command hold time	tWCH	10		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		ns	
Write command pulse width	tWP	10		15		ns	
Write command to RAS lead time	tRWL	15		20		ns	
Write command to CAS lead time	tCWL	15		20		ns	
Data-in setup time	tDS	0		0		ns	21
Data-in hold time	tDH	10		15		ns	21
Data-in hold time (referenced to RAS)	tDHR	45		55		ns	
Transition time (rise or fall)	tT	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	tREF		32		32	ms	
RAS to CAS precharge time	tRPC	0		0		ns	
CAS setup time (CBR test cycle)	tCSR	10		10		ns	5
CAS hold time (CBR test cycle)	tCHR	15		15		ns	5
WE hold time (CBR test cycle)	tWRH	10		10		ns	24
WE setup time (CBR test cycle)	tWRP	10		10		ns	24
WE hold time (WCBR test cycle)	tWTH	10		10		ns	24
WE setup time (WCBR test cycle)	tWTS	10		10		ns	24

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS)
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
22. $\overline{OE}$ is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not possible.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
24. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.

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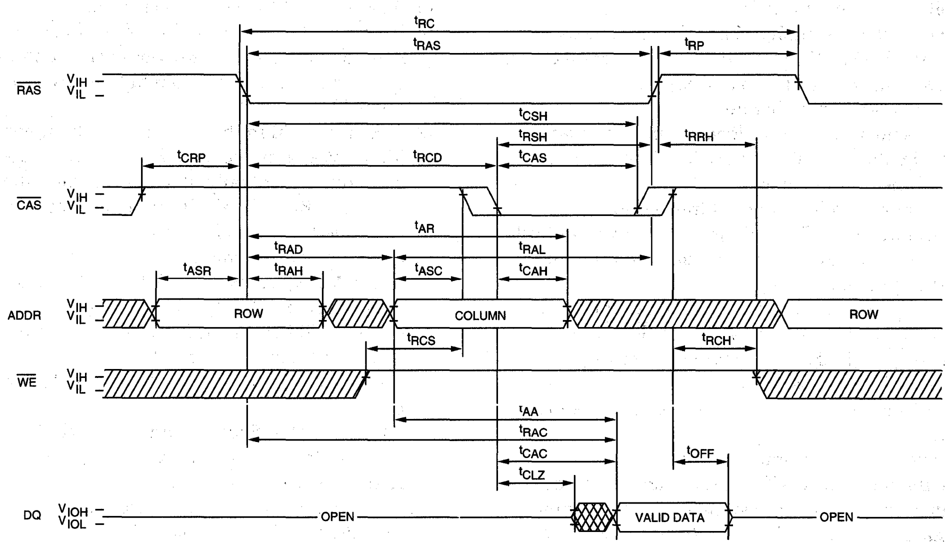
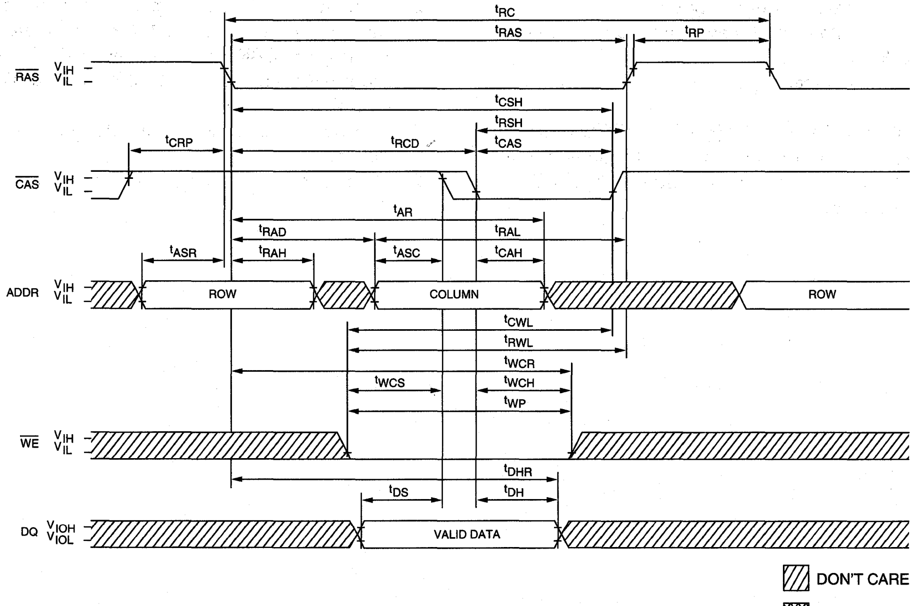
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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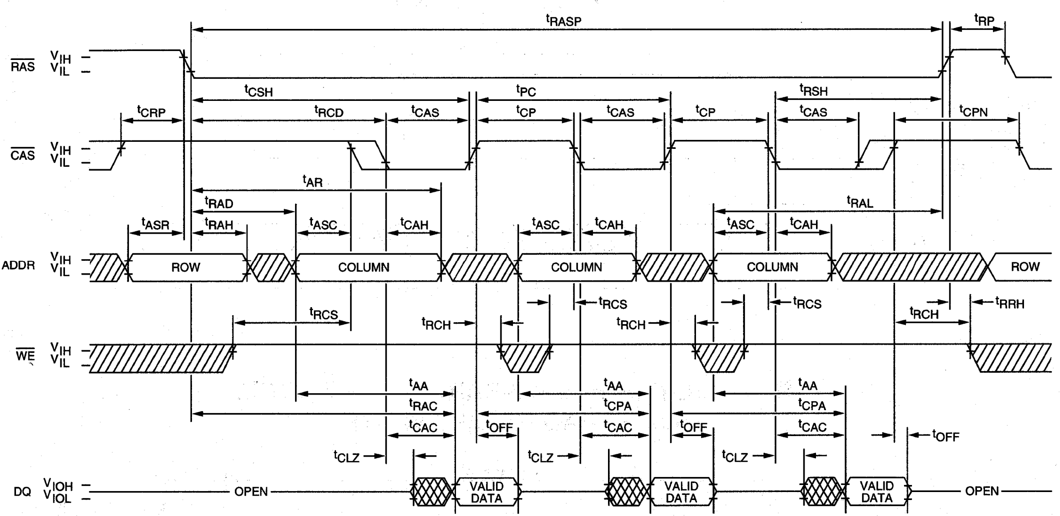
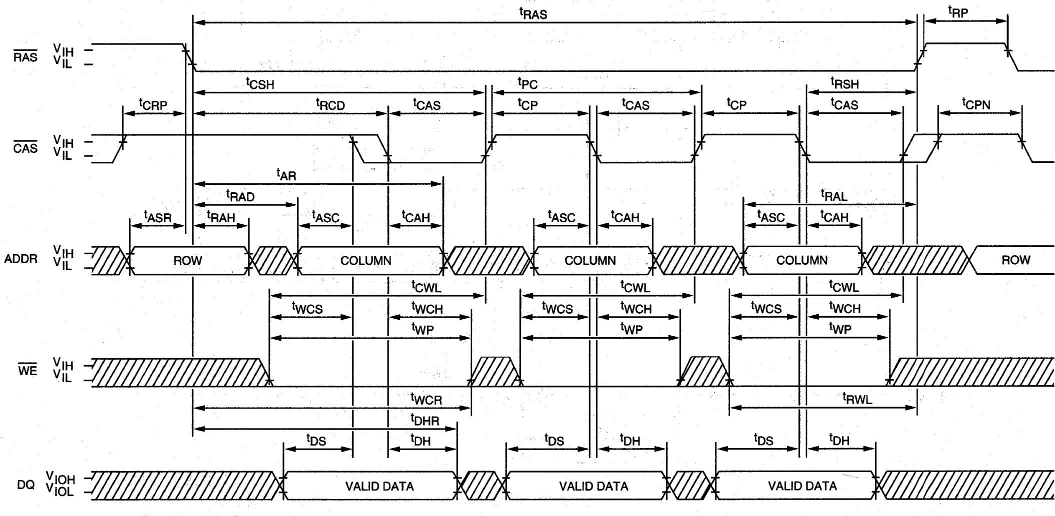
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DRAM MODULE

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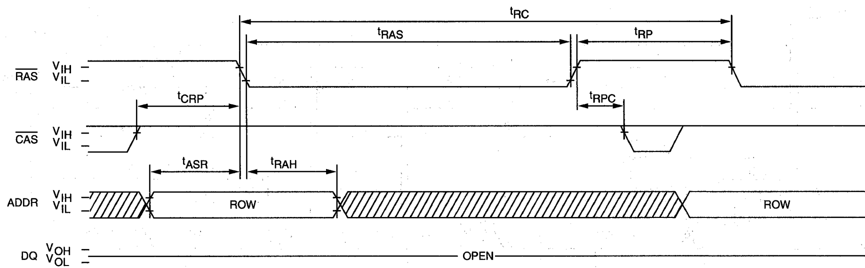
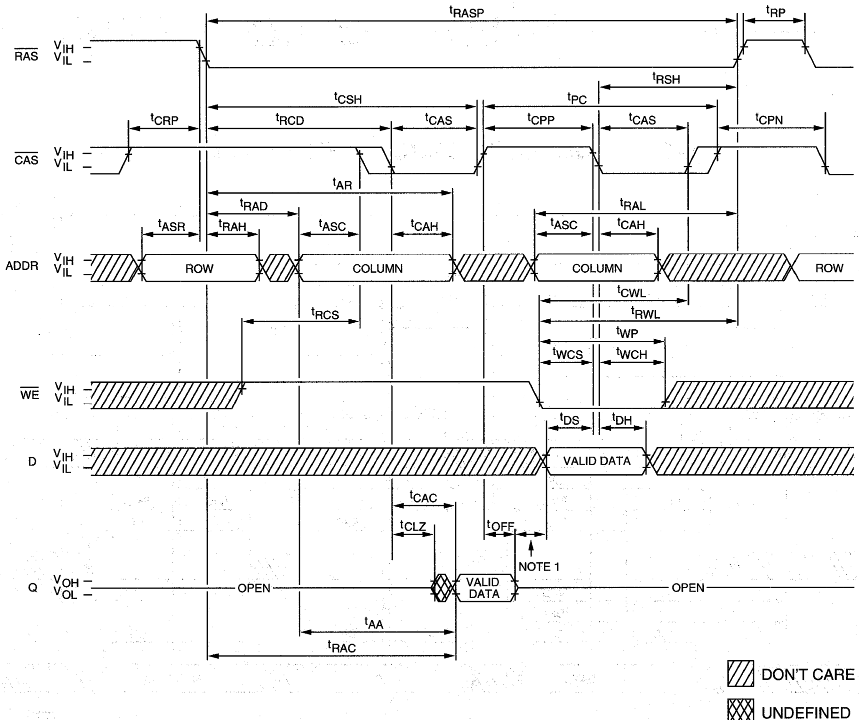
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE
(ADDR = A0-A10; $\overline{\text{WE}}$ = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE:
1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

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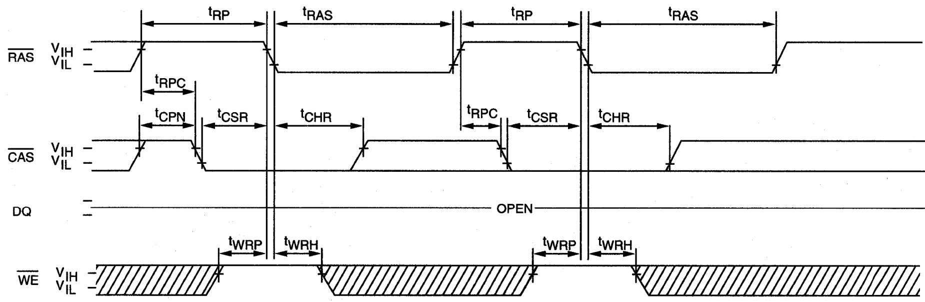
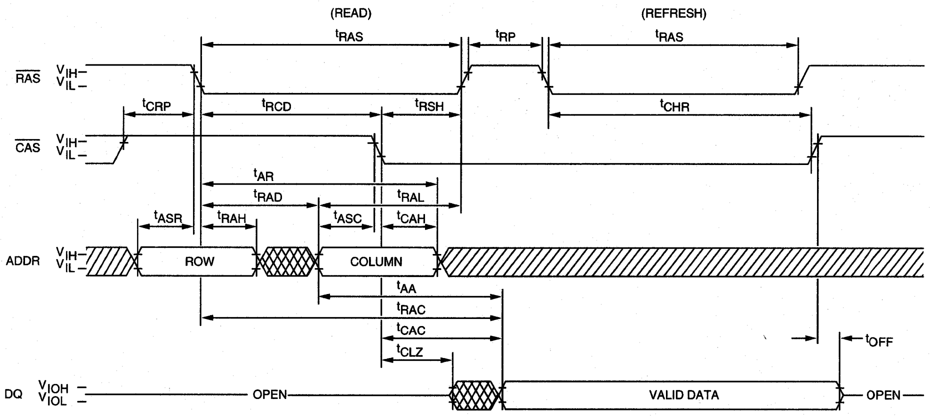
CBR REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)



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DRAM MODULE

1 MEG x 40 DRAM

FAST PAGE MODE (MT10D140)
LOW POWER, EXTENDED REFRESH (MT10D140 L)

FEATURES

- 72-pin single-in-line package
- High-performance CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 30mW (8mW L-version) standby; 2,250mW active, typical
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional Extended Refresh
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms

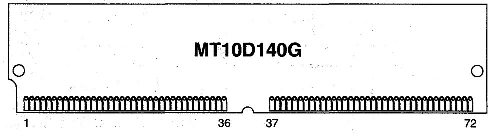
OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Leadless 72-pin SIMM (gold)	G
• Power/Refresh	
Normal power/16ms	Blank
Low power/128ms	L

- Part Number Example: MT10D140G-6 L

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(DE-9)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	$\overline{OE}$	37	DQ34	55	DQ12
2	DQ1	20	DQ5	38	DQ36	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	NC	59	Vcc
6	DQ3	24	DQ7	42	NC	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	DQ38	64	DQ32
11	NC	29	DQ37	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	Vss	66	DQ39
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	NC	52	DQ26	70	PRD4
17	A5	35	DQ35	53	DQ11	71	DQ40
18	A6	36	DQ33	54	DQ27	72	Vss

GENERAL DESCRIPTION

The MT10D140 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x40 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW; the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

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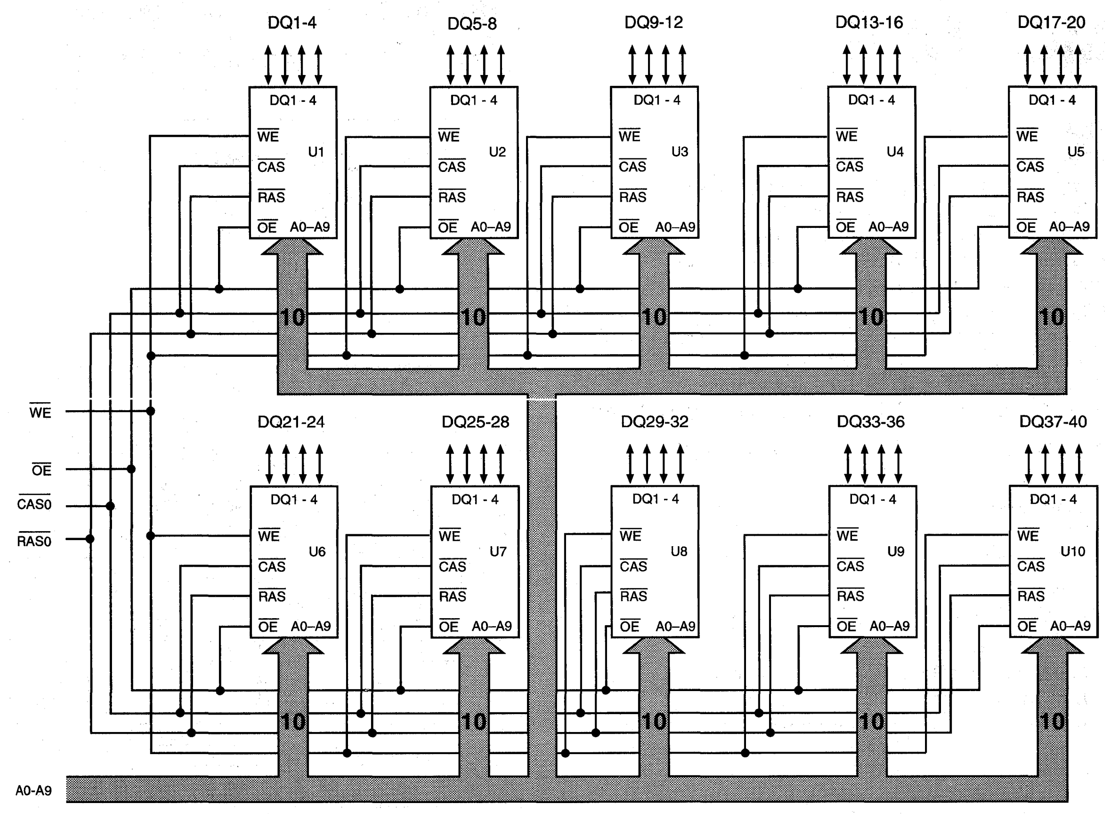
DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U10 = MT4C4001JDJ
U1-U10 = MT4C4001JDJ S (L-version)

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ40	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY WRITE		L	L	L	X	ROW	COL	Data-In	
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	
$\overline{RAS}$ ONLY REFRESH		H	X	X	X	ROW	n/a	High-Z	
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	
CBR REFRESH		H→L	L	H	X	X	X	High-Z	
Extended CBR REFRESH		H→L	L	H	X	X	X	High-Z	22

PRESENCE-DETECT–INDUSTRY STANDARD

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 10W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6, 26) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V) for each package input	A0-A9, $\overline{WE}$, $\overline{OE}$	II	-20	20	µA	
	$\overline{RAS0}$, $\overline{CAS0}$	II2	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ40	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	Icc3	20	20	20	mA	
STANDBY CURRENT: (CMOS) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V) (All other inputs at Vcc -0.2V)	Icc4	10	10	10	mA	
		2	2	2	mA	22
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	Icc1	1100	1000	900	mA	2, 25, 28
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$ = Cycling: ${}^tPC$ = ${}^tPC$ [MIN])	Icc2	800	700	600	mA	2, 25, 28
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = VIH)	Icc5	1100	1000	900	mA	25, 28
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	Icc6	1100	1000	900	mA	19, 25
REFRESH CURRENT: Extended CBR (L-version only) Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ${}^tRAS$ (MIN); $\overline{WE}$, A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open); ${}^tRC$ = 125µs (1024 rows at 125µs = 128ms)	Icc7	3	3	3	mA	19, 22, 25

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		60	pF	17
Input Capacitance: $\overline{WE}$, $\overline{OE}$, $\overline{RAS0}$, $\overline{CAS0}$	C_{I2}		80	pF	17
Input/Output Capacitance: DQ1-DQ40	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		100		105		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	45		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	21
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14

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DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	3	15	3	20	3	20	ns	12, 23, 27
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	24
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		110		ns	24
Column-address to $\overline{WE}$ delay time	^tAWD	55		65		70		ns	24
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		50		50		ns	24
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1024 cycles)	^tREF		16/128*		16/128*		16/128*	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	19
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	19
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	20
Output disable	^tOD		15		20		20	ns	23
Output enable	^tOE	15		20		20		ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	25
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	29
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	29
$\overline{WE}$ hold time (WCBR Test Cycle)	^tWTH	10		10		10		ns	29
$\overline{WE}$ setup time (WCBR Test Cycle)	^tWTS	10		10		10		ns	29

*L-version only

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NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the 16ms (128ms L version) refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C $\leq T_A \leq$ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
21. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
22. L-version only.
23. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
24. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
25. I_{CC} is dependent on cycle rates.
26. All other inputs at V_{CC} -0.2V.
27. The 3ns minimum is a parameter guaranteed by design.
28. Column-address changed once each cycle.
29. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.

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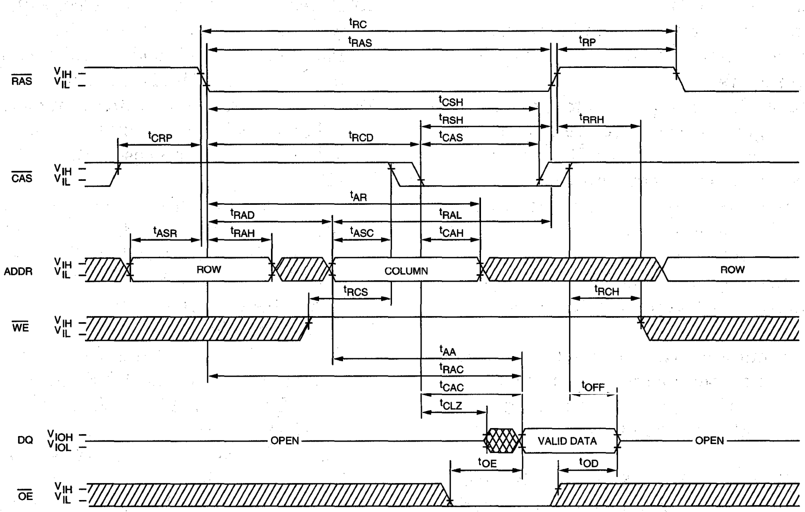
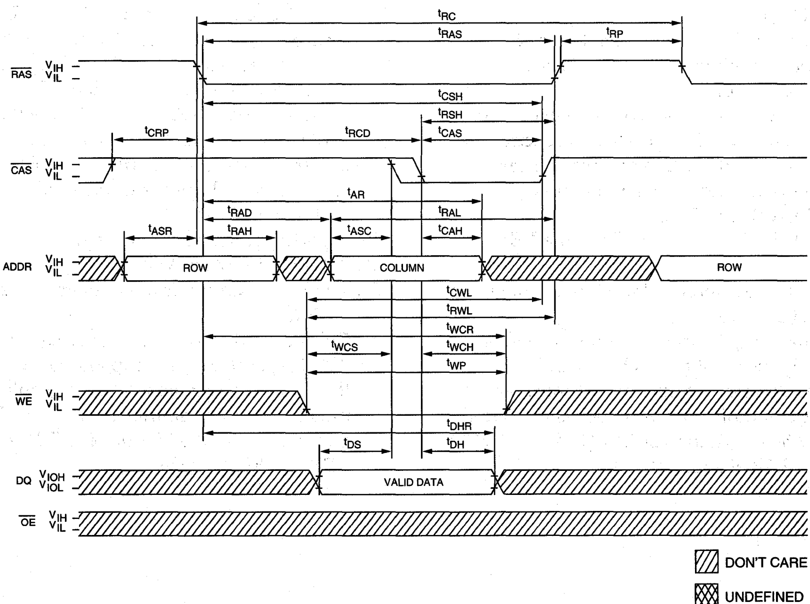
READ CYCLE



EARLY WRITE CYCLE



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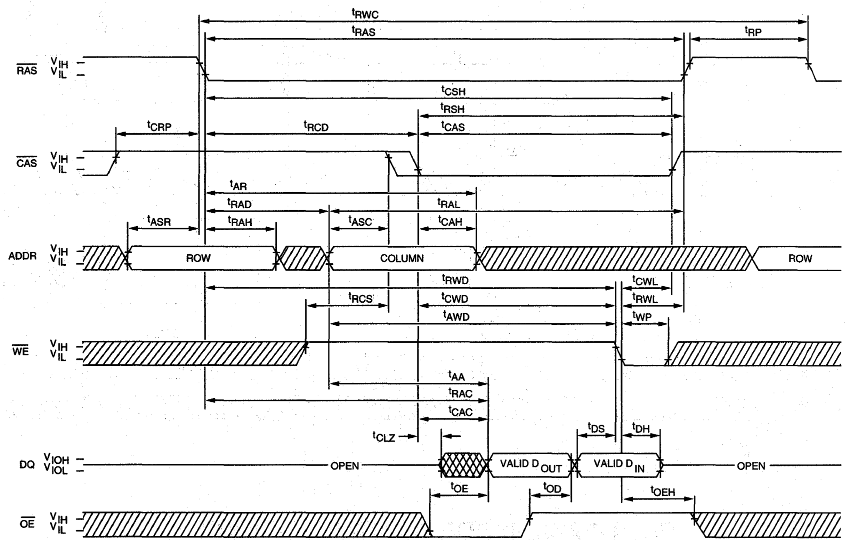
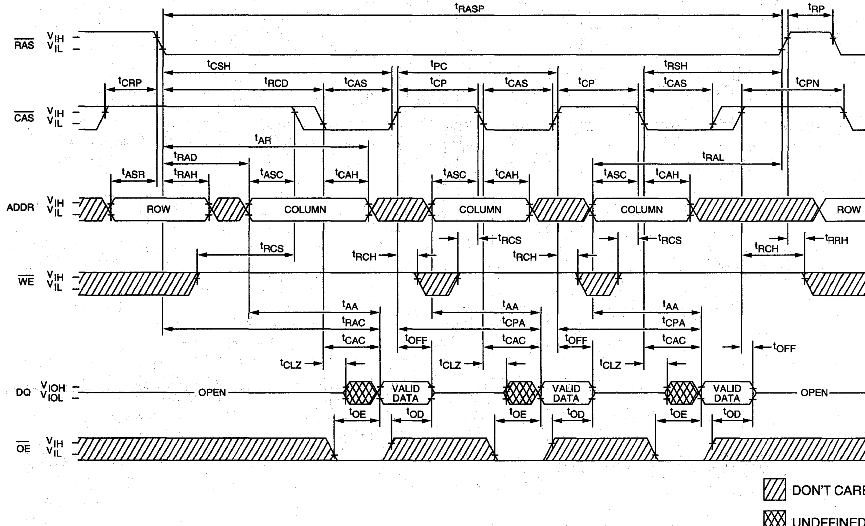
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

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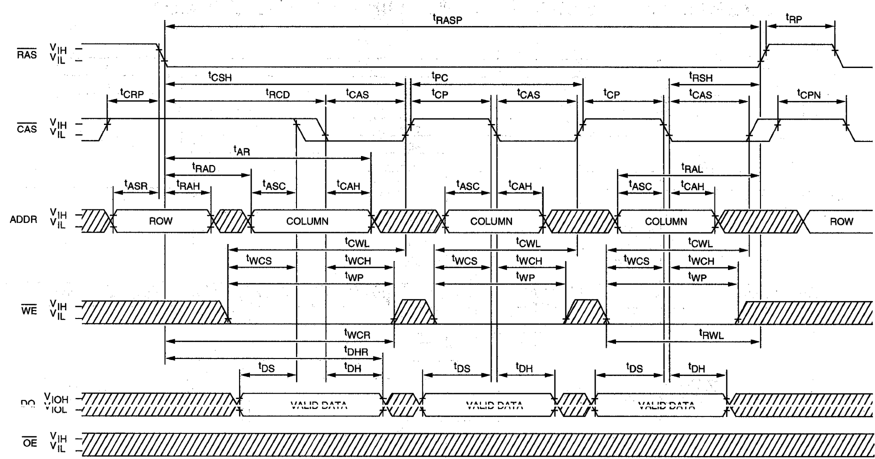
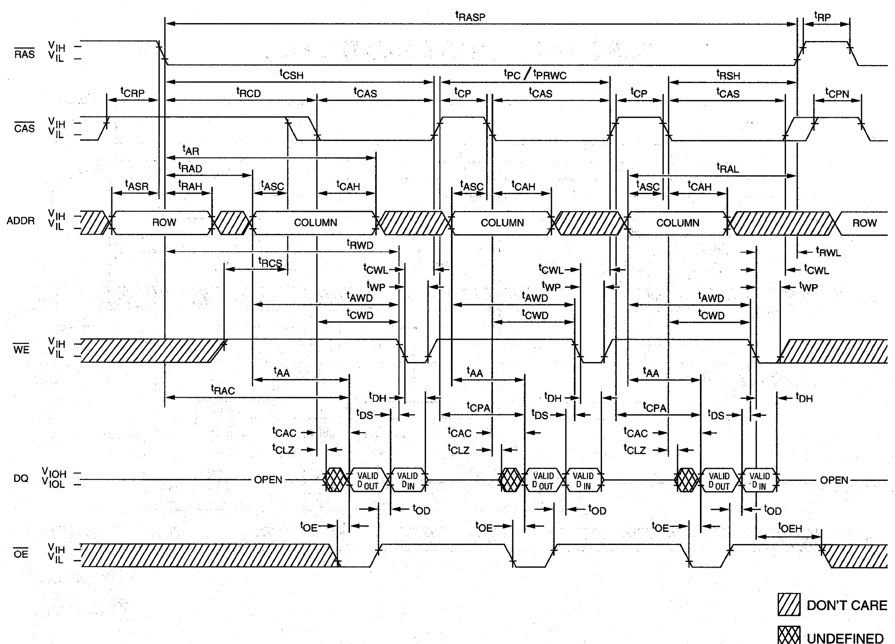
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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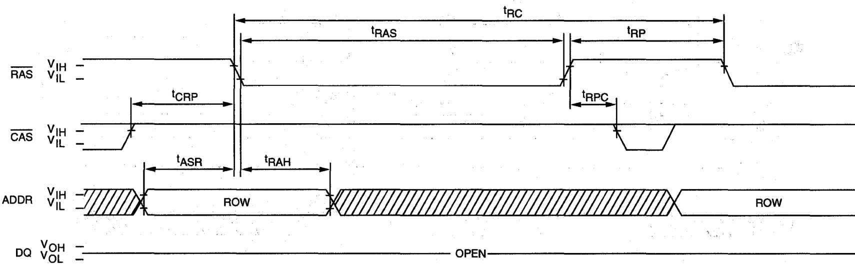
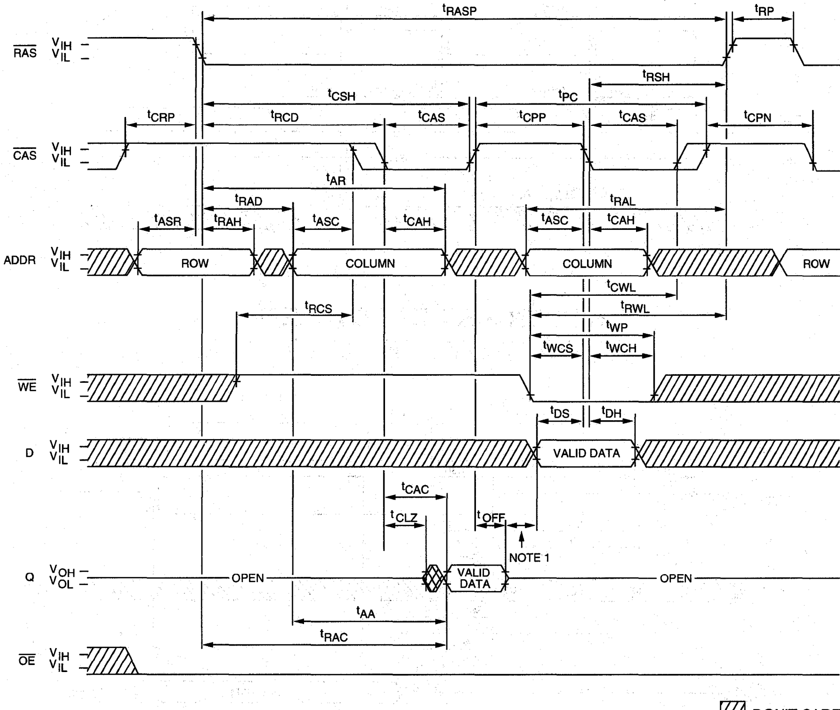
RAS ONLY REFRESH CYCLE
(ADDR = A0-A9; and WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

DRAM MODULE

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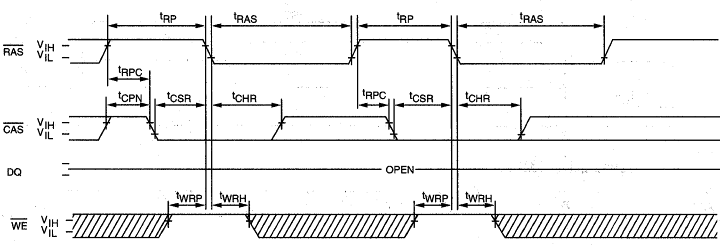
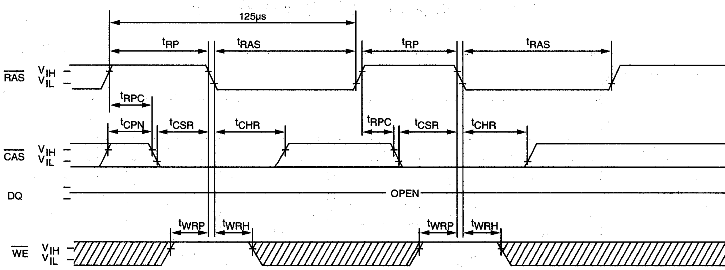
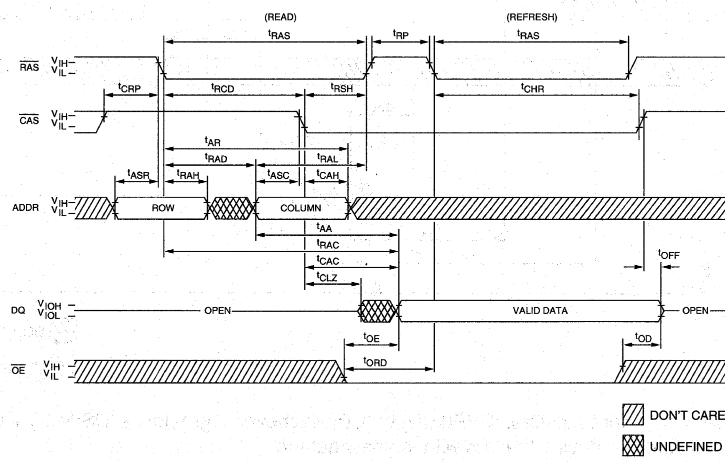
CBR REFRESH CYCLE
(A0-A9, $\overline{OE}$ = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [22]
(A0-A9, $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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DRAM MODULE

2 MEG x 40 DRAM

FAST PAGE MODE (MT20D240)
LOW POWER, EXTENDED REFRESH (MT20D240 L)

FEATURES

- 72-pin single-in-line package
- High-performance CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 60mW (16mW L-version) standby; 2,280mW active, typical
- FAST PAGE MODE access cycle
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN; optional Extended Refresh
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms (L-version)

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Leadless 72-pin SIMM (gold)	G
• Power/Refresh	
Normal power/16ms	Blank
Low power/128ms	L

- Part Number Example: MT20D240G-6 L

PIN ASSIGNMENT (Top View)

72-Pin SIMM (DE-10)

MT20D240G

1 36 37 72

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	OE	37	DQ34	55	DQ12
2	DQ1	20	DQ5	38	DQ36	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	NC	59	Vcc
6	DQ3	24	DQ7	42	NC	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	RAS1	63	DQ15
10	Vcc	28	A7	46	DQ38	64	DQ32
11	NC	29	DQ37	47	WE	65	DQ16
12	A0	30	Vcc	48	Vss	66	DQ39
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	NC	52	DQ26	70	PRD4
17	A5	35	DQ35	53	DQ11	71	DQ40
18	A6	36	DQ33	54	DQ27	72	Vss

GENERAL DESCRIPTION

The MT20D240 is a randomly accessed solid-state memory containing 2,097,152 words organized in a x40 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW; the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

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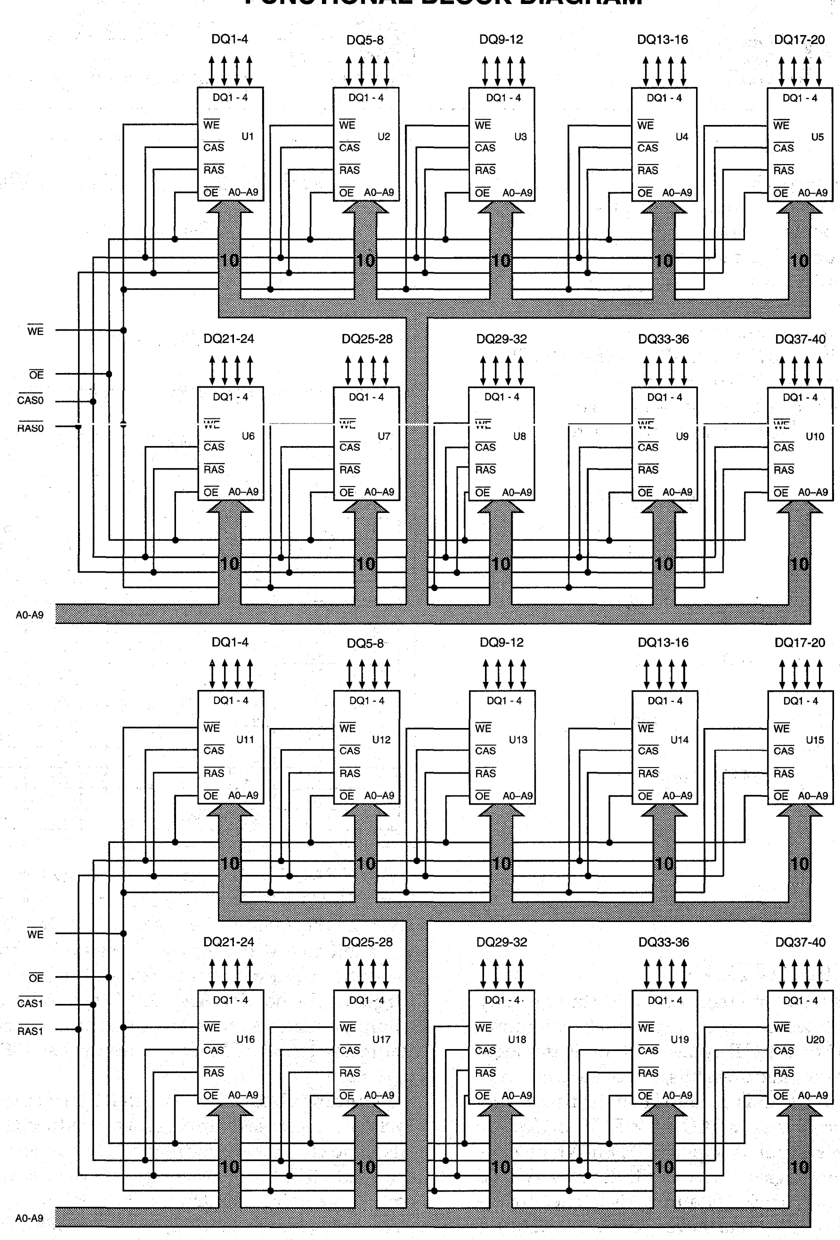
FUNCTIONAL BLOCK DIAGRAM



U1-U20 = MT4C4001JDJ
or U1-U20 = MT4C4001JDJ S (L-version)

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DATA-IN/OUT	NOTES
						^tR	^tC	DQ1-DQ40	
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY WRITE		L	L	L	X	ROW	COL	Data-In	
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	
$\overline{RAS}$ ONLY REFRESH		H	X	X	X	ROW	n/a	High-Z	
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	
CBR REFRESH		H→L	L	H	X	X	X	High-Z	
Extended CBR REFRESH		H→L	L	H	X	X	X	High-Z	22

DRAM MODULE

PRESENCE-DETECT–INDUSTRY STANDARD

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 20W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6, 26) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V) for each package input	A0-A9, W̅E̅, O̅E̅	II	-40	40	µA	
	R̅A̅S̅0-1, C̅A̅S̅0-1	II2	-20	20	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ40	IOZ	-20	20	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (R̅A̅S̅ = C̅A̅S̅ = VIH)	ICC3	40	40	40	mA	
STANDBY CURRENT: (CMOS) (R̅A̅S̅ = C̅A̅S̅ = Vcc -0.2V)	ICC4	20	20	20	mA	
(All other inputs at Vcc -0.2V)		4	4	4	mA	22
OPERATING CURRENT: Random READ/WRITE Average power supply current (R̅A̅S̅ and C̅A̅S̅ = Cycling: tRC = tRC [MIN])	ICC1	1120	1020	920	mA	2, 25, 28
OPERATING CURRENT: FAST PAGE MODE Average power supply current (R̅A̅S̅ = VIL, C̅A̅S̅ = Cycling: tPC = tPC [MIN])	ICC2	820	720	620	mA	2, 25, 28
REFRESH CURRENT: R̅A̅S̅ ONLY Average power supply current (R̅A̅S̅ = Cycling: C̅A̅S̅ = VIH)	ICC5	1120	1020	920	mA	25, 28
REFRESH CURRENT: CBR Average power supply current (R̅A̅S̅ and C̅A̅S̅ = Cycling)	ICC6	1120	1020	920	mA	19, 25
REFRESH CURRENT: Extended CBR (L-version only) Average power supply current during Extended Refresh: C̅A̅S̅ = 0.2V or CBR cycling; R̅A̅S̅ = tRAS (MIN); W̅E̅, A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open); tRC = 125µs (1,024 rows at 125µs = 128ms)	ICC7	6	6	6	mA	19, 22, 25

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		120	pF	17
Input Capacitance: $\overline{WE}$, $\overline{OE}$	C_{I2}		160	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS0}$, $\overline{CAS1}$	C_{I3}		84	pF	17
Input/Output Capacitance: DQ1-DQ40	C_{IO}		18	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		100		105		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	45		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	21
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14

DRAM MODULE

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	14
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	tOFF	3	15	3	20	3	20	ns	12, 23, 27
WE command setup time	tWCS	0		0		0		ns	24
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
RAS to WE delay time	tRWD	90		100		110		ns	24
Column-address to WE delay time	tAWD	55		65		70		ns	24
CAS to WE delay time	tCWD	40		50		50		ns	24
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	tREF		16/128*		16/128*		16/128*	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	19
CAS setup time (CBR REFRESH)	tCSR	10		10		10		ns	19
CAS hold time (CBR REFRESH)	tCHR	10		10		10		ns	19
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		0		ns	20
Output disable	tOD		15		20		20	ns	23
Output enable	tOE	15		20		20		ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		20		20		ns	25
WE hold time (CBR REFRESH)	tWRH	10		10		10		ns	29
WE setup time (CBR REFRESH)	tWRP	10		10		10		ns	29
WE hold time (WCBR REFRESH)	tWTH	10		10		10		ns	29
WE setup time (WCBR REFRESH)	tWTS	10		10		10		ns	29

*L-version only

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NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the 16ms (128ms L version) refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IH} and V_{IL}).
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
21. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
22. L-version only.
23. ^tWCS, ^tRWD, ^tAWD and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY WRITE cycles. ^tRWD, ^tAWD and ^tCWD apply to READ-MODIFY-WRITE cycles. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE WRITE cycle.
24. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
25. I_{CC} is dependent on cycle rates.
26. All other inputs at V_{CC} -0.2V.
27. The 3ns minimum is a parameter guaranteed by design.
28. Column-address changed once each cycle.
29. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.

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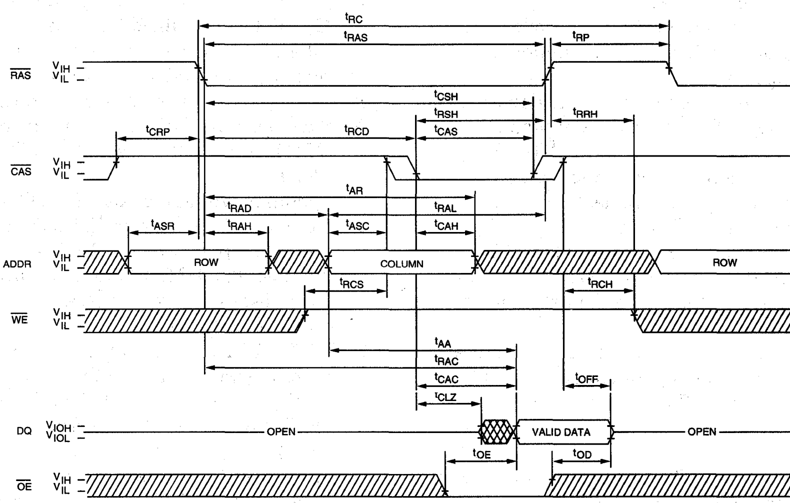
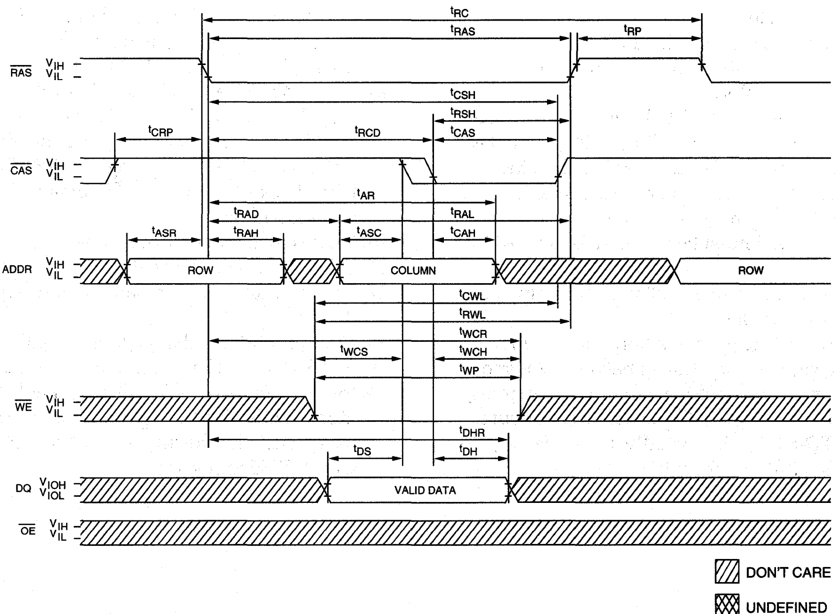
READ CYCLE



EARLY WRITE CYCLE



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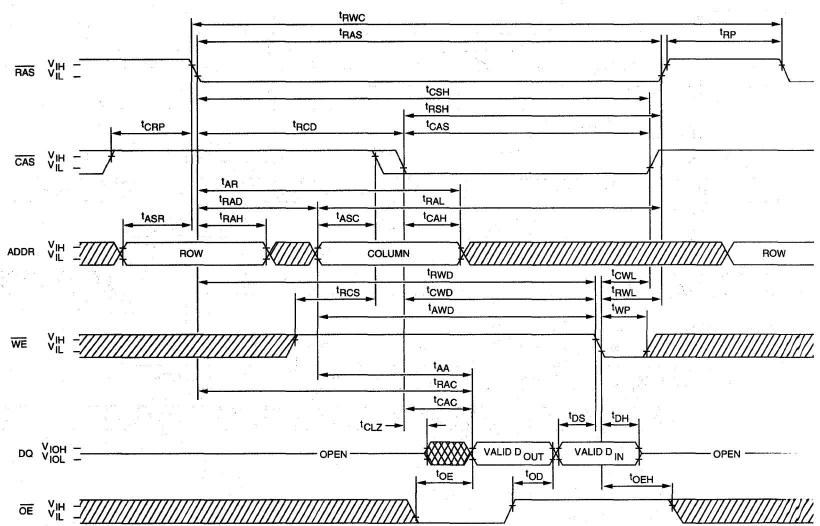
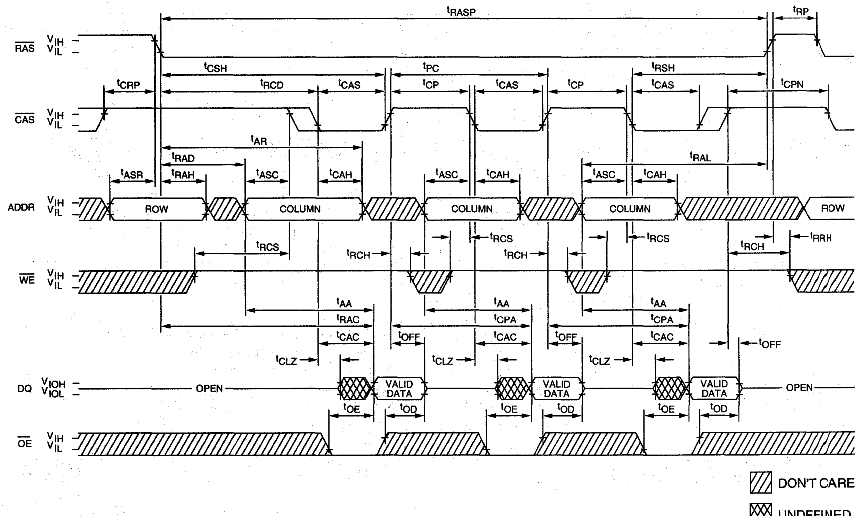
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

DRAM MODULE

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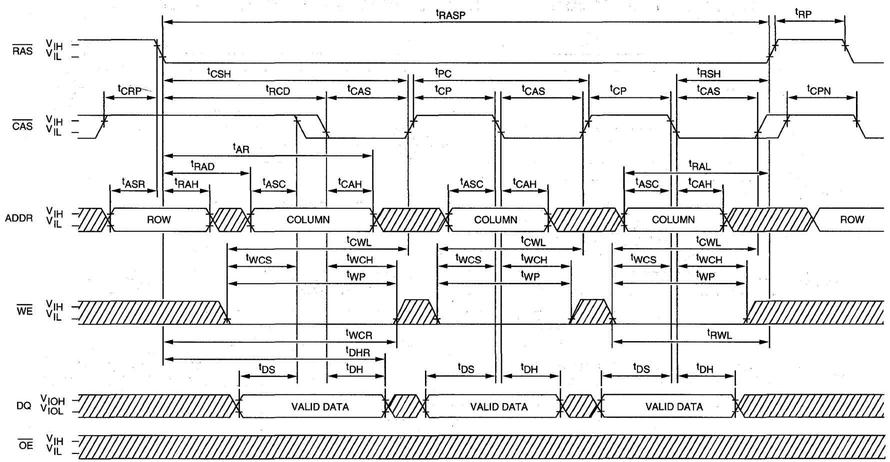
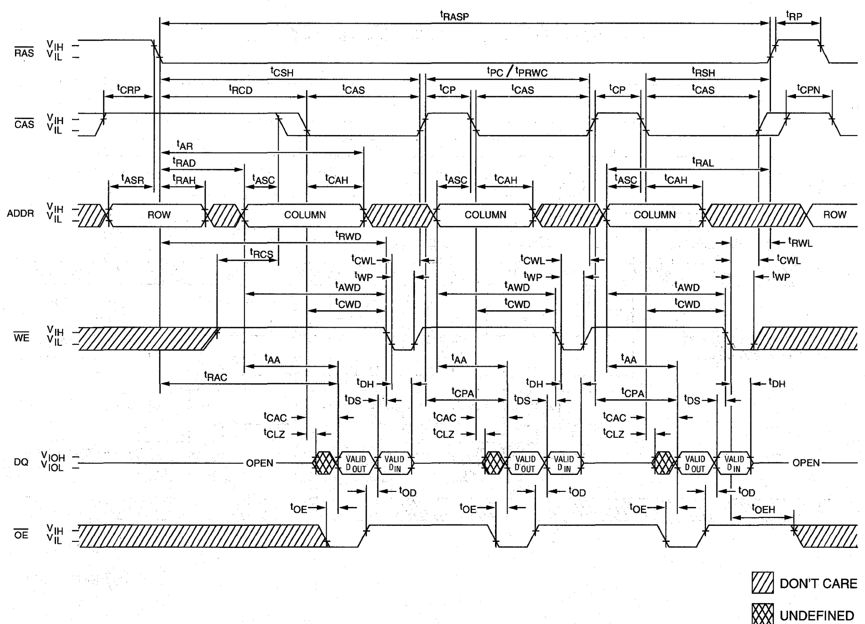
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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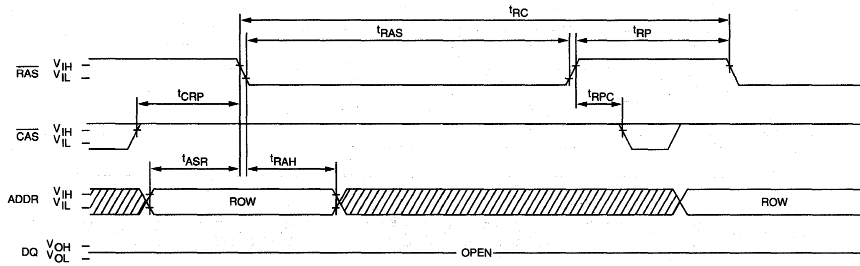
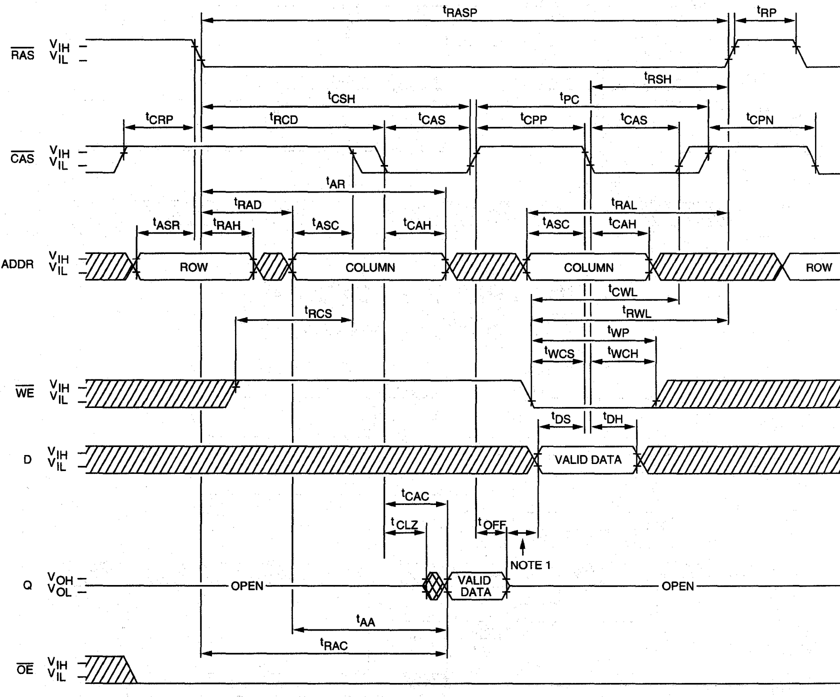
RAS ONLY REFRESH CYCLE
(ADDR = A0-A9; and WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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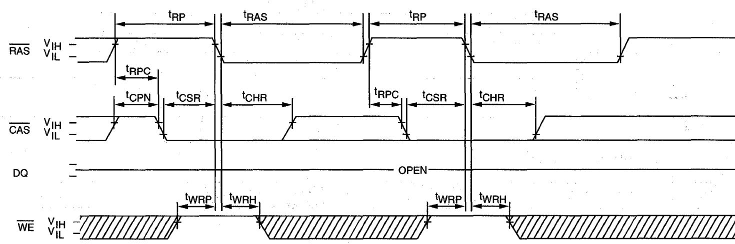
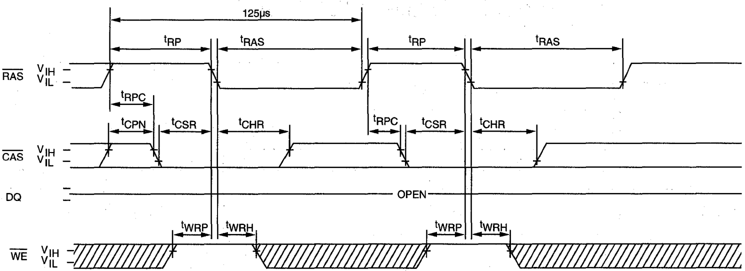
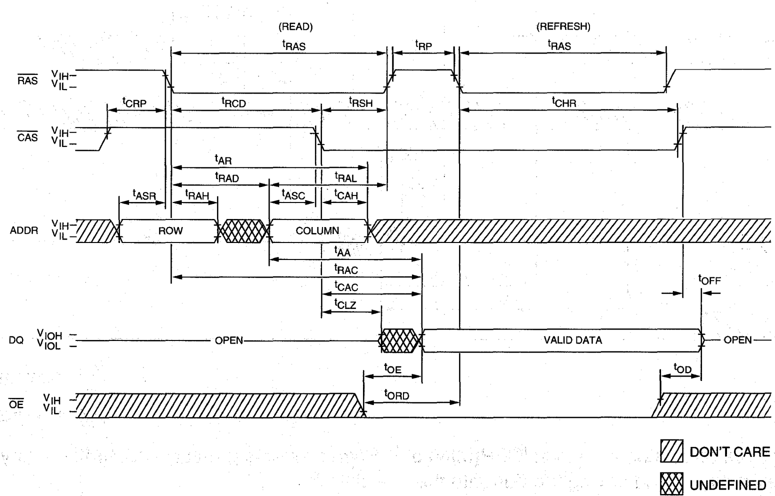
CBR REFRESH CYCLE
(A0-A9, $\overline{OE}$ = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [22]
(A0-A9, $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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DRAM MODULE

4 MEG x 40 DRAM

FAST PAGE MODE

FEATURES

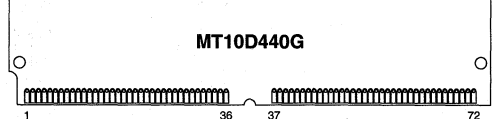
- Industry-standard 72-pin single in-line package
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins TTL-compatible
- Low power, 30mW standby; 2,000mW active, typical (4K refresh)
- FAST PAGE MODE access cycle
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms or 4,096-cycle refresh distributed across 64ms

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
- Packages
  - Leadless 72-pin SIMM (gold) — G
- Refresh period
  - 2,048 cycles at 32ms, 11 row-addresses — blank
  - 4,096 cycles at 64ms, 12 row-addresses — B
- Part Number Example: MT10D440G-6 B

PIN ASSIGNMENT (Top View)

72-Pin SIMM (DE-17)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	OE	37	DQ20	55	DQ29
2	DQ1	20	DQ9	38	DQ21	56	DQ30
3	DQ2	21	DQ10	39	Vss	57	DQ31
4	DQ3	22	DQ11	40	CAS0	58	DQ32
5	DQ4	23	DQ12	41	A10	59	Vcc
6	DQ5	24	DQ13	42	A11*/NC	60	DQ33
7	DQ6	25	DQ14	43	NC	61	DQ34
8	DQ7	26	DQ15	44	RAS0	62	DQ35
9	DQ8	27	DQ16	45	NC	63	DQ36
10	Vcc	28	A7	46	DQ22	64	DQ37
11	PRD5	29	DQ17	47	WE	65	DQ38
12	A0	30	Vcc	48	Vss	66	DQ39
13	A1	31	A8	49	DQ23	67	PRD1
14	A2	32	A9	50	DQ24	68	PRD2
15	A3	33	NC	51	DQ25	69	PRD3
16	A4	34	NC	52	DQ26	70	PRD4
17	A5	35	DQ18	53	DQ27	71	DQ40
18	A6	36	DQ19	54	DQ28	72	Vss

*B-version only

GENERAL DESCRIPTION

The MT10D440/B are randomly accessed solid-state memories containing 4,194,304 words organized in a x40 bit configuration. The MT10D440 and MT10D440 B are the same DRAM module versions except that the MT10D440 B has a 4,096-cycle refresh instead of a 2,048-cycle refresh. All further references made for the MT10D440G also apply to the MT10D440 B unless specifically stated otherwise. For the module with a 2,048-cycle refresh, RAS is used to latch the first 11 bits and CAS the latter 11 bits. For a module with a 4,096-cycle refresh, RAS is used to latch the first 12 bits and CAS the latter 10 bits (A10 and A11 are "don't care" bits). READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ MODE while a logic LOW on WE dictates WRITE MODE. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW after data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE and OE.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9/A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory

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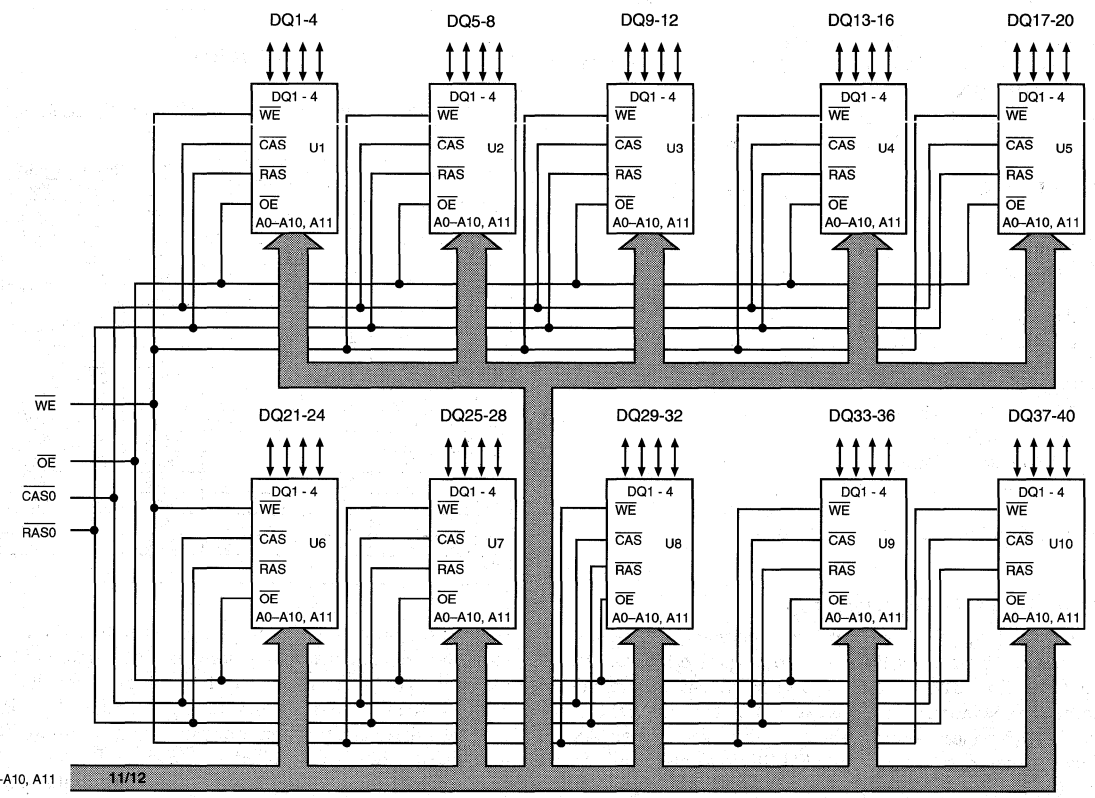
cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all 2,048/4,096 combinations of $\overline{RAS}$ addresses (A0-A10/A11) are executed at least every 32ms/64ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

If CBR REFRESH is used, the number of cycles is a "don't care."

FUNCTIONAL BLOCK DIAGRAM



U1-U10 = MT4C4M4B1DJ (2,048-cycle)
or U1-U10 = MT4C4M4A1DJ (4,096-cycle)

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DATA-IN/OUT	NOTES
						${}^tR$	${}^tC$	DQ1-DQ40	
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY WRITE		L	L	L	X	ROW	COL	Data-In	
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	
$\overline{RAS}$ ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	
CBR REFRESH		H→L	L	H	X	X	X	High-Z	

PRESENCE-DETECT–INDUSTRY STANDARD

SYMBOL	-6	-7
PRD1	Vss	Vss
PRD2	NC	NC
PRD3	NC	Vss
PRD4	NC	NC
PRD5	Vss	Vss

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 10W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V	A0-A10, A11 $\overline{WE}$, $\overline{OE}$	II	-20	20	µA	
(All other pins not under test = 0V) for each package input	$\overline{RAS0}$, $\overline{CAS0}$	II2	-20	20	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ40	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = 5V ±10%), 4,096-cycle refresh (B-version only)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	20	20	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	ICC2	10	10	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	900	800	mA	3, 4, 28, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])	ICC4	700	600	mA	3, 4, 28, 30
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])	ICC5	900	800	mA	3, 28, 30
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC6	900	800	mA	3, 5, 28

(Notes: 1, 6, 7) (Vcc = 5V ±10%), 2,048-cycle refresh

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	20	20	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	ICC2	10	10	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	1200	1100	mA	3, 4, 27, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])	ICC4	900	800	mA	3, 4, 27, 30
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])	ICC5	1200	1100	mA	3, 27, 30
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC6	1200	1100	mA	3, 5, 27

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, A11	C_{I1}		64	pF	2
Input Capacitance: $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{RAS0}}$, $\overline{\text{CAS0}}$	C_{I2}		84	pF	2
Input/Output Capacitance: DQ1-DQ40	C_{IO}		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +5V±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	
READ WRITE cycle time	^tRWC	150		180		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		ns	
Access time from $\overline{\text{RAS}}$	^tRAC		60		70	ns	14
Access time from $\overline{\text{CAS}}$	^tCAC		15		20	ns	15
Output Enable	^tOE		15		20	ns	23
Access time from column-address	^tAA		30		35	ns	
Access time from $\overline{\text{CAS}}$ precharge	^tCPA		35		40	ns	
$\overline{\text{RAS}}$ pulse width	^tRAS	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ hold time	^tRSH	15		20		ns	
$\overline{\text{RAS}}$ precharge time	^tRP	40		50		ns	
$\overline{\text{CAS}}$ pulse width	^tCAS	15	100,000	20	100,000	ns	
$\overline{\text{CAS}}$ hold time	^tCSH	60		70		ns	
$\overline{\text{CAS}}$ precharge time	^tCPN	10		10		ns	16
$\overline{\text{CAS}}$ precharge time (FAST PAGE MODE)	^tCP	10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	^tRCD	20	45	20	50	ns	17
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	^tCRP	5		5		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{\text{RAS}}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	10		15		ns	
Column-address hold time (referenced to $\overline{\text{RAS}}$)	^tAR	50		55		ns	
Column-address to $\overline{\text{RAS}}$ lead time	^tRAL	30		35		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{\text{CAS}}$)	^tRCH	0		0		ns	19

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	3		3		ns	29
Output buffer turn-off delay	^{t}OFF	3	15	3	20	ns	20, 29
$\overline{WE}$ command setup time	^{t}WCS	0		0		ns	21, 27
Write command hold time	^{t}WCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	45		55		ns	
Write command pulse width	^{t}WP	10		15		ns	
Write command to $\overline{RAS}$ lead time	^{t}RWL	15		20		ns	
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		ns	
Data-in setup time	^{t}DS	0		0		ns	22
Data-in hold time	^{t}DH	10		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	85		95		ns	21
Column-address to $\overline{WE}$ delay time	^{t}AWD	55		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	40		45		ns	21
Transition time (rise or fall)	^{t}T	3	50	3	50	ns	9, 10
Refresh period (2,048 & 4,096 cycles)	^{t}REF		32/64*		32/64*	ms	26
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	5		5		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	15		15		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	10		10		ns	25
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	^{t}WTH	10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	^{t}WTS	10		10		ns	25
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		ns	
Output disable	^{t}OD	3	15	3	20	ns	29
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^{t}OEH	15		15		ns	

*B-version only

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, V_{CC} = 5V, DC bias = 2.4V at 15mV RMS).
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY-WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$ controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. 32ms is a 2048-row refresh, 64ms is a 4096-row refresh.
27. 2048-row refresh.
28. 4096-row refresh.
29. The 3ns minimum is a parameter guaranteed by design.
30. Column-address changed once each cycle.

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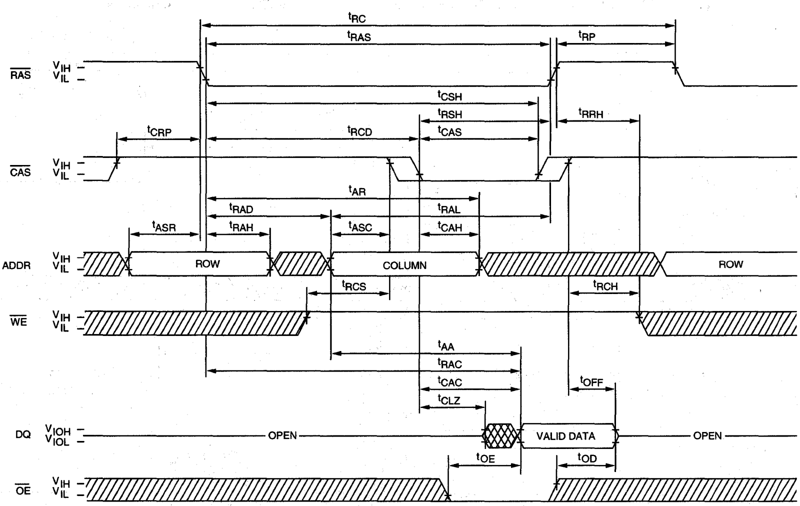
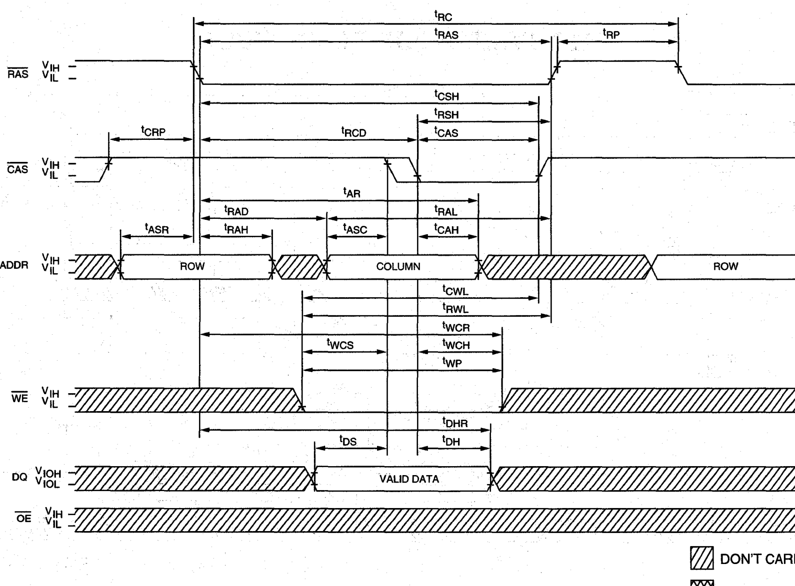
READ CYCLE



EARLY WRITE CYCLE



DRAM MODULE

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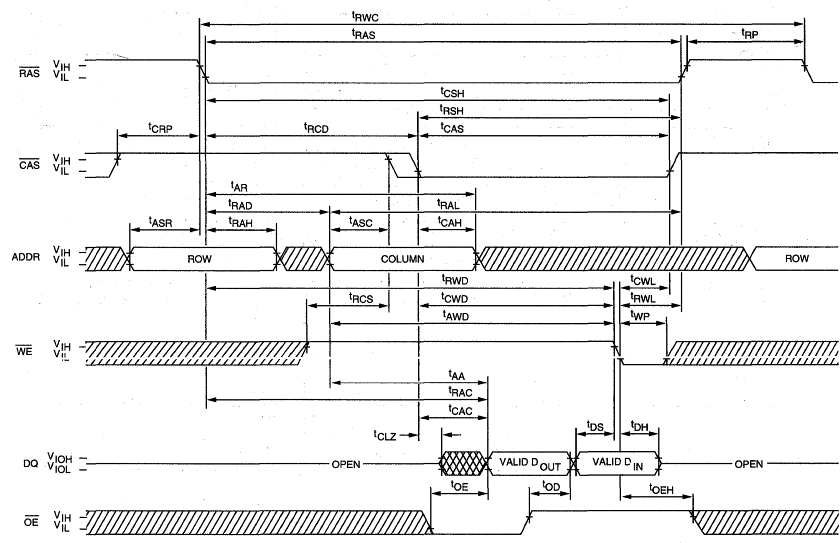
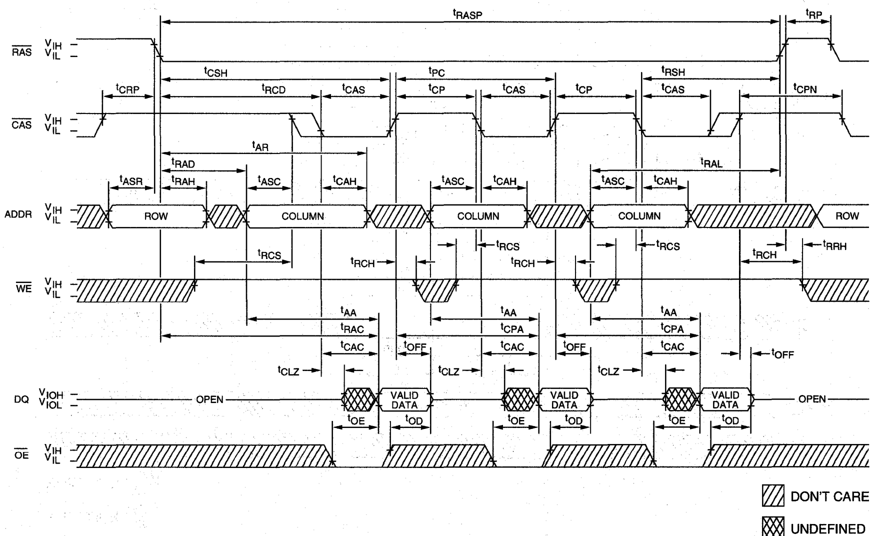
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



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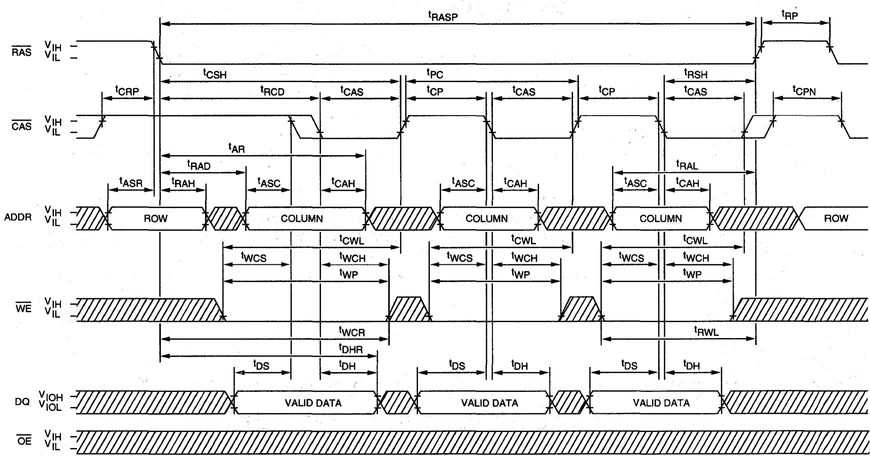
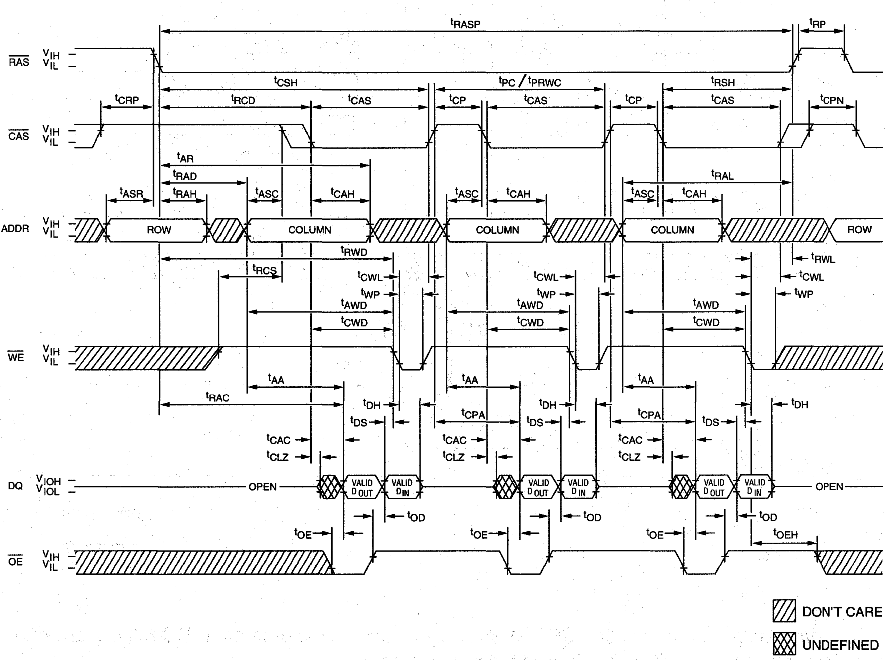
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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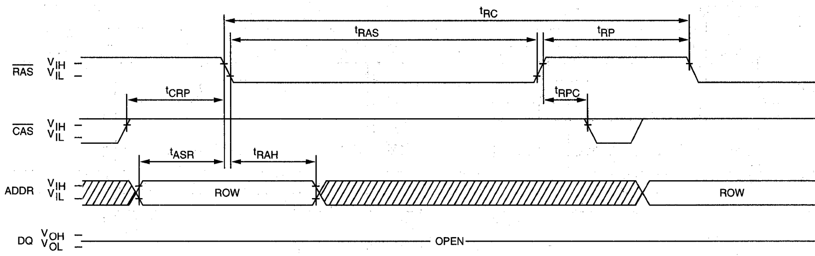
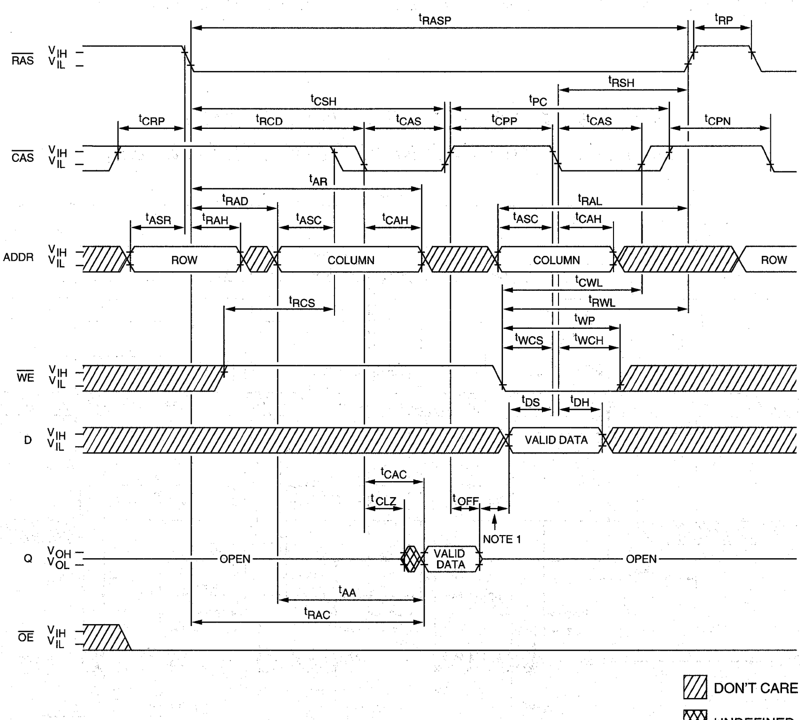
RAS ONLY REFRESH CYCLE

(ADDR = A0-A10, A11; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: ^{t}CPP(MIN) or ^{t}CP(whichever is greater) + ^{t}DS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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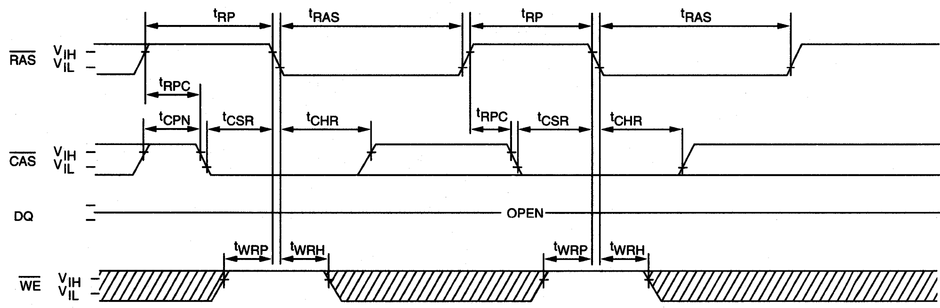
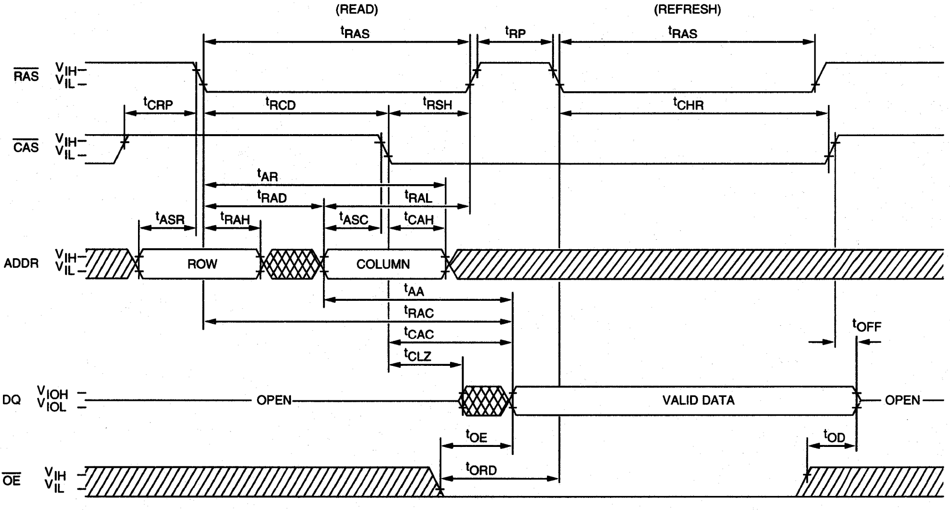
CBR REFRESH CYCLE
(ADDRESSES, $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



DON'T CARE

UNDEFINED

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DRAM MODULE

8 MEG x 40 DRAM

FAST PAGE MODE

FEATURES

- Industry-standard 72-pin single in-line package
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 60mW standby; 2,030mW active, typical (4K refresh)
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms or 4,096-cycle refresh distributed across 64ms

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Leadless 72-pin SIMM (gold)	G
• Refresh period	
2,048 cycles at 32ms, 11 row-addresses	blank
4,096 cycles at 64ms, 12 row-addresses	B

- Part Number Example: MT20D840G-6 B

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(DE-16)

MT20D840G

1 36 37 72

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	$\overline{OE}$	37	DQ20	55	DQ29
2	DQ1	20	DQ9	38	DQ21	56	DQ30
3	DQ2	21	DQ10	39	Vss	57	DQ31
4	DQ3	22	DQ11	40	$\overline{CAS0}$	58	DQ32
5	DQ4	23	DQ12	41	A10	59	Vcc
6	DQ5	24	DQ13	42	A11*/NC	60	DQ33
7	DQ6	25	DQ14	43	$\overline{CAS1}$	61	DQ34
8	DQ7	26	DQ15	44	$\overline{RAS0}$	62	DQ35
9	DQ8	27	DQ16	45	$\overline{RAS1}$	63	DQ36
10	Vcc	28	A7	46	DQ22	64	DQ37
11	PRD5	29	DQ17	47	$\overline{WE}$	65	DQ38
12	A0	30	Vcc	48	Vss	66	DQ39
13	A1	31	A8	49	DQ23	67	PRD1
14	A2	32	A9	50	DQ24	68	PRD2
15	A3	33	NC	51	DQ25	69	PRD3
16	A4	34	NC	52	DQ26	70	PRD4
17	A5	35	DQ18	53	DQ27	71	DQ40
18	A6	36	DQ19	54	DQ28	72	Vss

*B-version only

GENERAL DESCRIPTION

The MT20D840/B are randomly accessed solid-state memories containing 8,388,608 words organized in a x40 bit configuration. The MT20D840 and MT20D840 B are the same DRAM module versions except that the MT20D840 B has a 4,096-cycle refresh instead of a 2,048-cycle refresh. All further references made for the MT20D840 also apply to the MT20D840 B unless specifically stated otherwise. For the module with a 2,048-cycle refresh, $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. For a module with a 4,096-cycle refresh, $\overline{RAS}$ is used to latch the first 12 bits and $\overline{CAS}$ the latter 10 bits (A10 and A11 are "don't care" bits). READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW after data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9/A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

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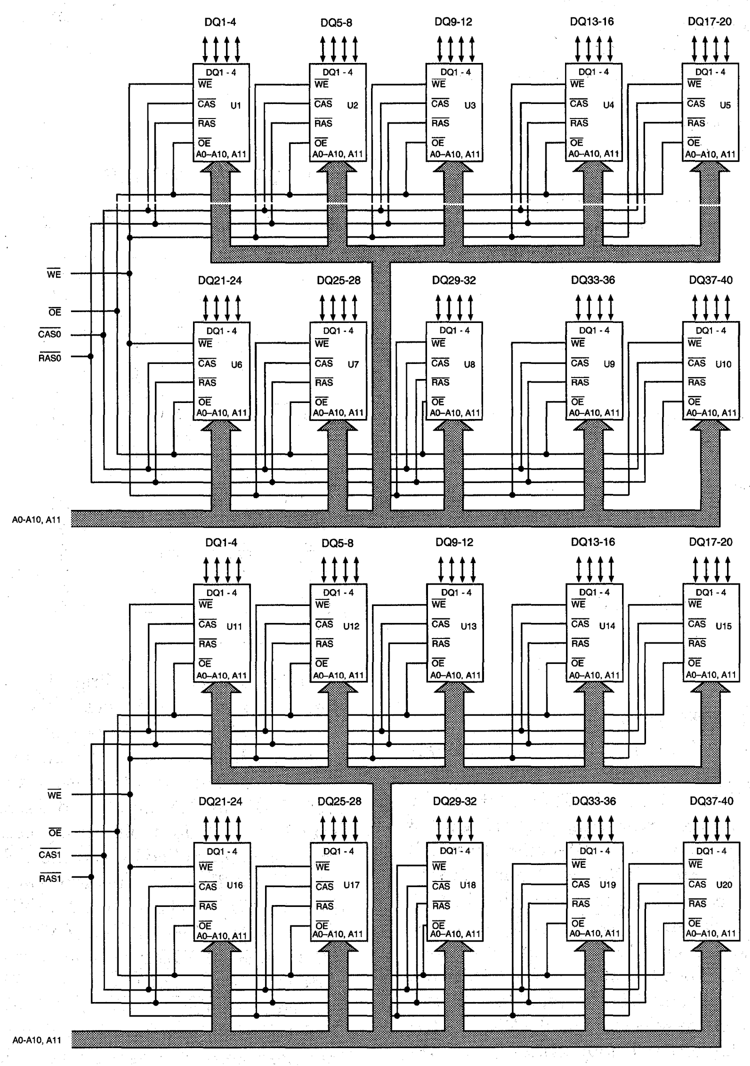
Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048/4,096 combinations of RAS addresses (A0-A10/A11) are executed at least every 32ms/64ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

If CBR REFRESH is used, the number of cycles is a "don't care."

FUNCTIONAL BLOCK DIAGRAM



U1-U20 = MT4C4M4B1DJ (2,048-cycle)
or U1-U20 = MT4C4M4A1DJ (4,096-cycle)

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DATA-IN/OUT	NOTES
						^tR	^tC	DQ1-DQ40	
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY WRITE		L	L	L	X	ROW	COL	Data-In	
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	
$\overline{RAS}$ ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	
CBR REFRESH		H→L	L	H	X	X	X	High-Z	

PRESENCE-DETECT–INDUSTRY STANDARD

SYMBOL	-6	-7
PRD1	NC	NC
PRD2	Vss	Vss
PRD3	NC	Vss
PRD4	NC	NC
PRD5	Vss	Vss

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 20W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V	A0-A10, A11 $\overline{\text{WE}}$, $\overline{\text{OE}}$	II	-40	40	µA	
(All other pins not under test = 0V) for each package input	$\overline{\text{RAS}}$0-1, $\overline{\text{CAS}}$0-1	II2	-20	20	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ40	IOZ	-20	20	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = 5V ±10%), 4,096-cycle refresh (B-version only)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	40	40	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	20	20	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	920	820	mA	3, 4, 28, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	720	620	mA	3, 4, 28, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	920	820	mA	3, 28, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	920	820	mA	3, 5, 28

(Notes: 1, 6, 7) (V_{CC} = 5V ±10%), 2,048-cycle refresh

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	40	40	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	20	20	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	1,220	1,120	mA	3, 4, 27, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	920	820	mA	3, 4, 27, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	1,220	1,120	mA	3, 27, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	1,220	1,120	mA	3, 5, 27

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DRAM MODULE

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, A11	C_{I1}		110	pF	2
Input Capacitance: $\overline{WE}$, $\overline{OE}$	C_{I2}		150	pF	2
Input Capacitance: $\overline{RAS0-RAS1}$, $\overline{CAS0-CAS1}$	C_{I2}		80	pF	2
Input/Output Capacitance: DQ1-DQ40	C_{IO}		16	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V ± 10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	
READ WRITE cycle time	^tRWC	150		180		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		ns	
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15
Output Enable	^tOE		15		20	ns	23
Access time from column-address	^tAA		30		35	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V ± 10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		ns	29
Output buffer turn-off delay	tOFF	3	15	3	20	ns	20, 29
$\overline{WE}$ command setup time	tWCS	0		0		ns	21, 27
Write command hold time	tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		ns	
Write command pulse width	tWP	10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		20		ns	
Data-in setup time	tDS	0		0		ns	22
Data-in hold time	tDH	10		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	85		95		ns	21
Column-address to $\overline{WE}$ delay time	tAWD	55		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	40		45		ns	21
Transition time (rise or fall)	tT	3	50	3	50	ns	9, 10
Refresh period (2,048 & 4,096 cycles)	tREF		32/64*		32/64*	ms	26
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	tCSR	5		5		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	tCHR	15		15		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	tWRH	10		10		ns	25
$\overline{WE}$ setup time (CBR REFRESH)	tWRP	10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	tWTS	10		10		ns	25
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		ns	
Output disable	tOD	3	15	3	20	ns	29
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	15		15		ns	

*B-version only

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, V_{CC} = 5V, DC bias = 2.4V at 15mV RMS).
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$ controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. 32ms is a 2048-row refresh, 64ms is a 4096-row refresh.
27. 2048-row refresh.
28. 4096-row refresh.
29. The 3ns minimum is a parameter guaranteed by design.
30. Column-address changed once each cycle.

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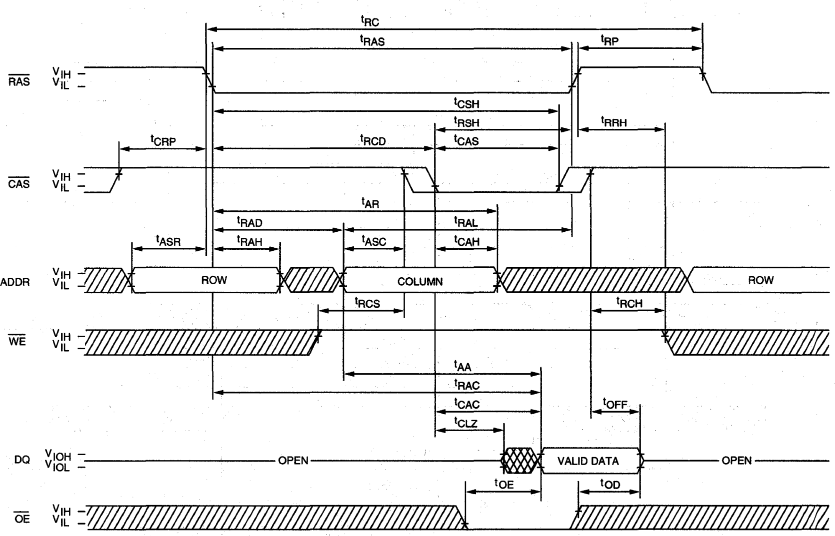
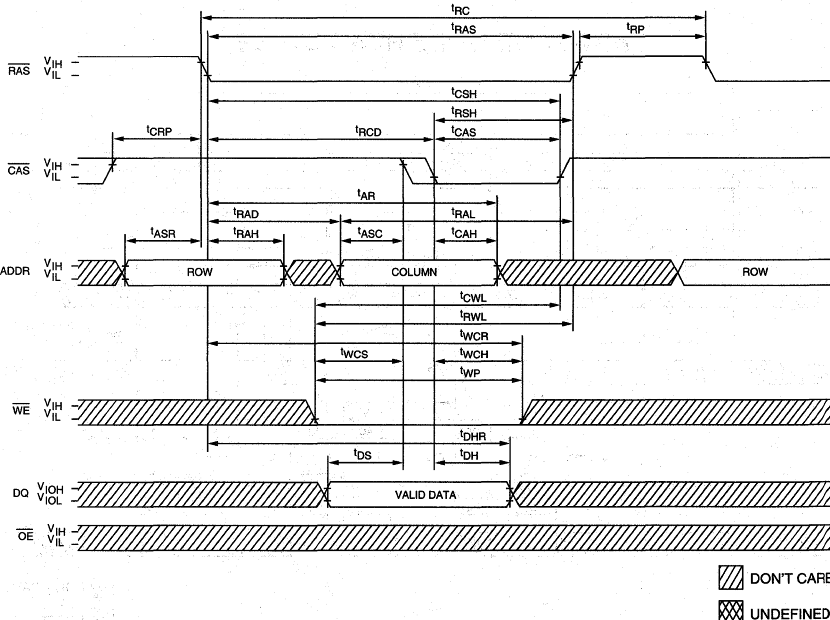
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

DRAM MODULE

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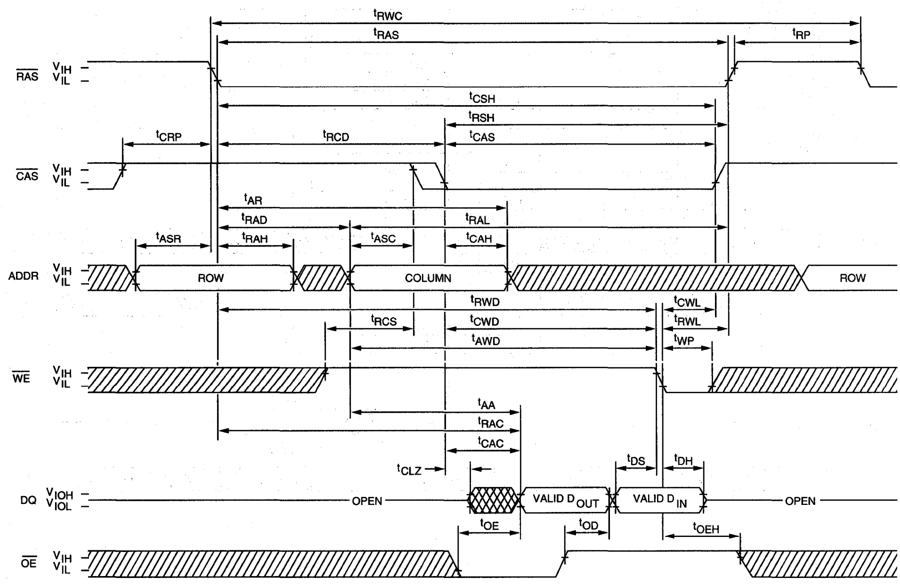
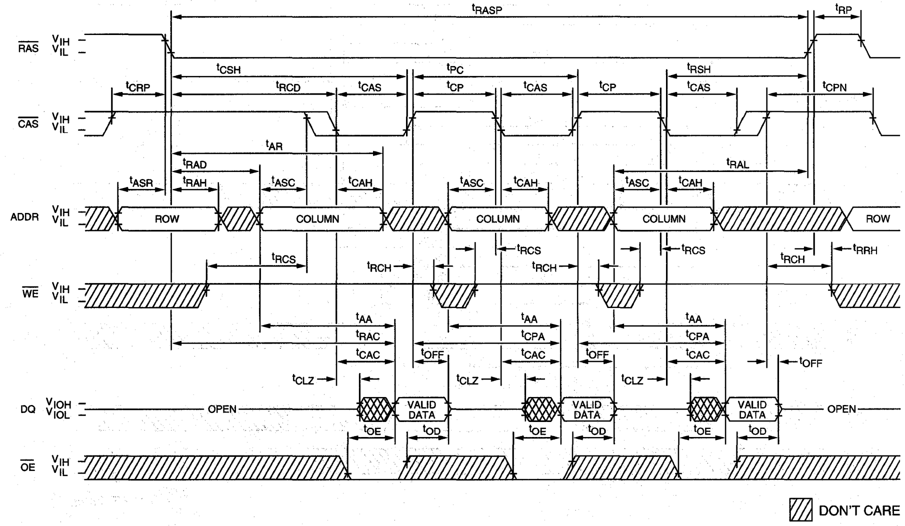
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

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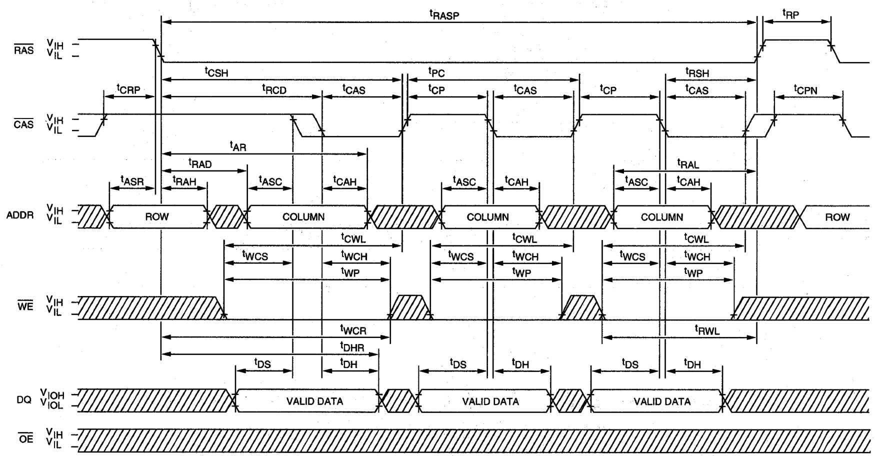
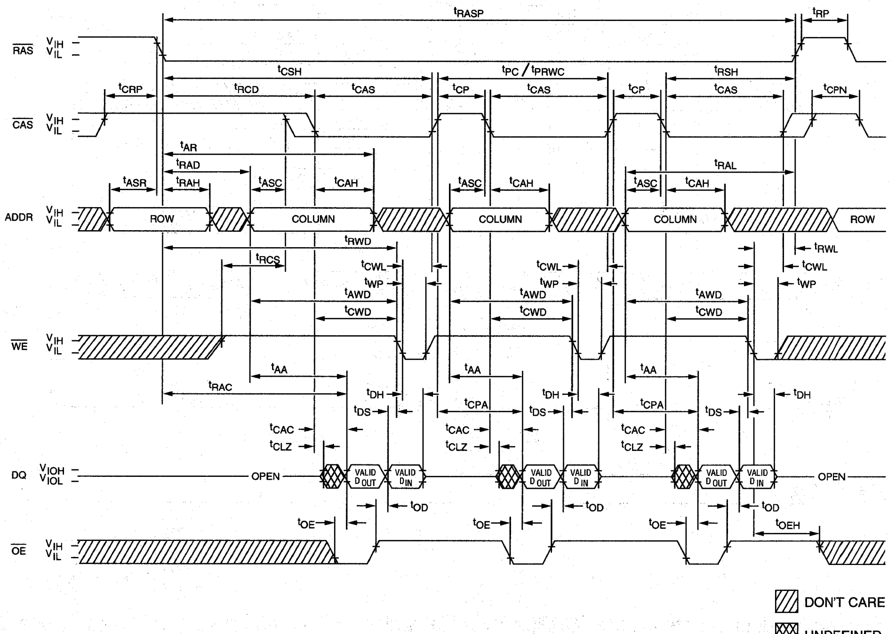
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



DON'T CARE

UNDEFINED

DRAM MODULE

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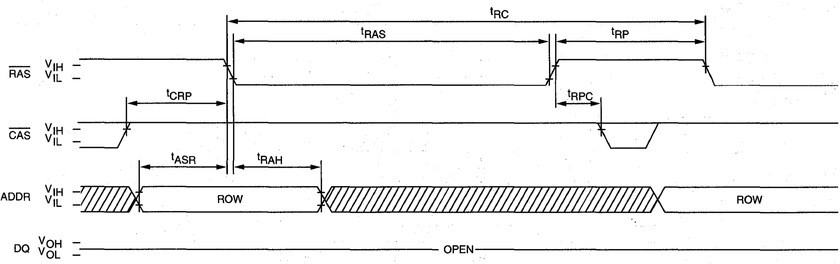
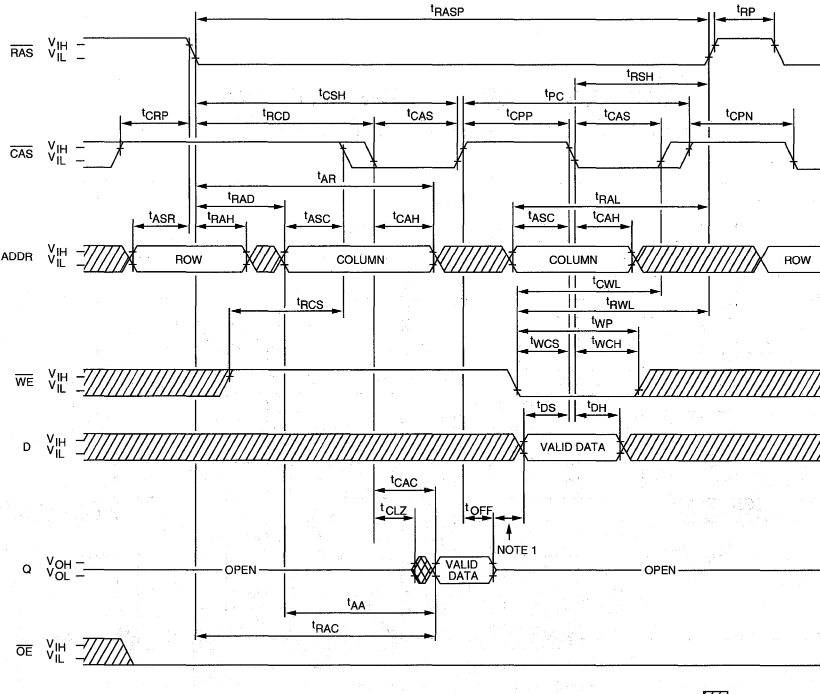
RAS ONLY REFRESH CYCLE
(ADDR = A0-A10, A11; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: ^{t}CPP(MIN) or ^{t}CP(whichever is greater) + ^{t}DS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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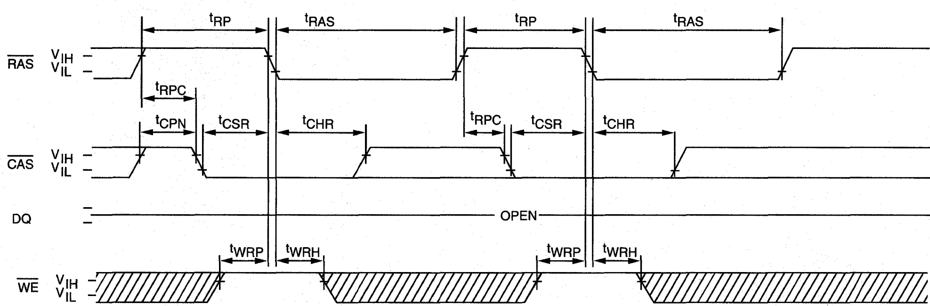
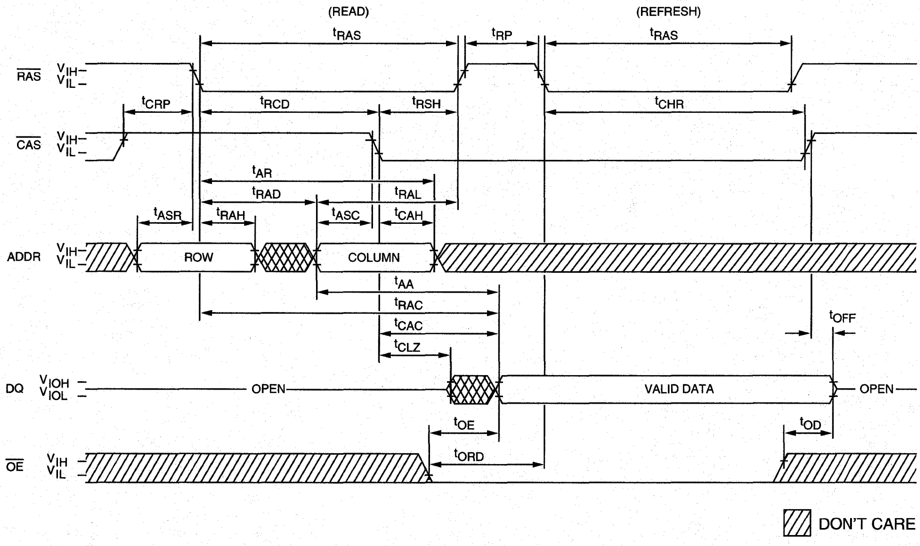
CBR REFRESH CYCLE
(ADDRESSES, $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



DRAM MODULE

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DRAM MODULE

1 MEG x 64 DRAM

FAST PAGE MODE (MT16D(T)164)
LOW POWER,
EXTENDED REFRESH (MT16D(T)164 L)

FEATURES

- Industry-standard pinout in a 168-pin, dual read-out, single in-line package
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 48mW (13mW L-version) standby; 3,600mW active, typical
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN; optional Extended Refresh
- All inputs are buffered except $\overline{\text{RAS}}$
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE access cycle

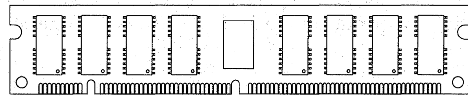
OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Components
  - SOJ — D
  - TSOP — DT
- Packages
  - Leadless 168-pin, dual read-out DIMM — M
  - Leadless 168-pin, dual read-out DIMM (gold) — G
- Refresh
  - Standard — Blank
  - Low-power Extended Refresh — L
- Part Number Example: MT16DT164M-6 L

PIN ASSIGNMENT (Top View)

168-Pin, Dual Read-out DIMM

(DE-22) SOJ version
(DE-23) TSOP version



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{\text{OE2}}$	86	DQ32	128	RFU
3	DQ1	45	$\overline{\text{RAS2}}$	87	DQ33	129	NC
4	DQ2	46	$\overline{\text{CAS4}}$	88	DQ34	130	$\overline{\text{CAS5}}$
5	DQ3	47	$\overline{\text{CAS6}}$	89	DQ35	131	$\overline{\text{CAS7}}$
6	Vcc	48	$\overline{\text{WE2}}$	90	Vcc	132	$\overline{\text{PDE}}$
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	NC	53	DQ17	95	NC	137	DQ49
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	Vcc	101	DQ44	143	Vcc
18	Vcc	60	DQ22	102	Vcc	144	DQ54
19	DQ13	61	RFU	103	DQ45	145	RFU
20	DQ14	62	RFU	104	DQ46	146	RFU
21	DQ15	63	RFU	105	DQ47	147	RFU
22	NC	64	RFU	106	NC	148	RFU
23	Vss	65	DQ23	107	Vss	149	DQ55
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ24	109	NC	151	DQ56
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{\text{WE0}}$	69	DQ25	111	RFU	153	DQ57
28	$\overline{\text{CAS0}}$	70	DQ26	112	$\overline{\text{CAS1}}$	154	DQ58
29	$\overline{\text{CAS2}}$	71	DQ27	113	$\overline{\text{CAS3}}$	155	DQ59
30	$\overline{\text{RAS0}}$	72	DQ28	11	NC	156	DQ60
31	$\overline{\text{OE0}}$	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ29	116	Vss	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	NC	119	A5	161	NC
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	NC	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

GENERAL DESCRIPTION

The MT16D(T)164 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x64 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0 /B0-A9) at a time. A0 is connected to DQ0-DQ31, while B0 is connected to DQ32-DQ63. $\overline{\text{RAS}}$ is used to latch the first 10 bits and $\overline{\text{CAS}}$ the latter 10 bits. READ and WRITE cycles are selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, which-

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ever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, and the output pin(s) remain open (High-Z) until the next CAS cycle.

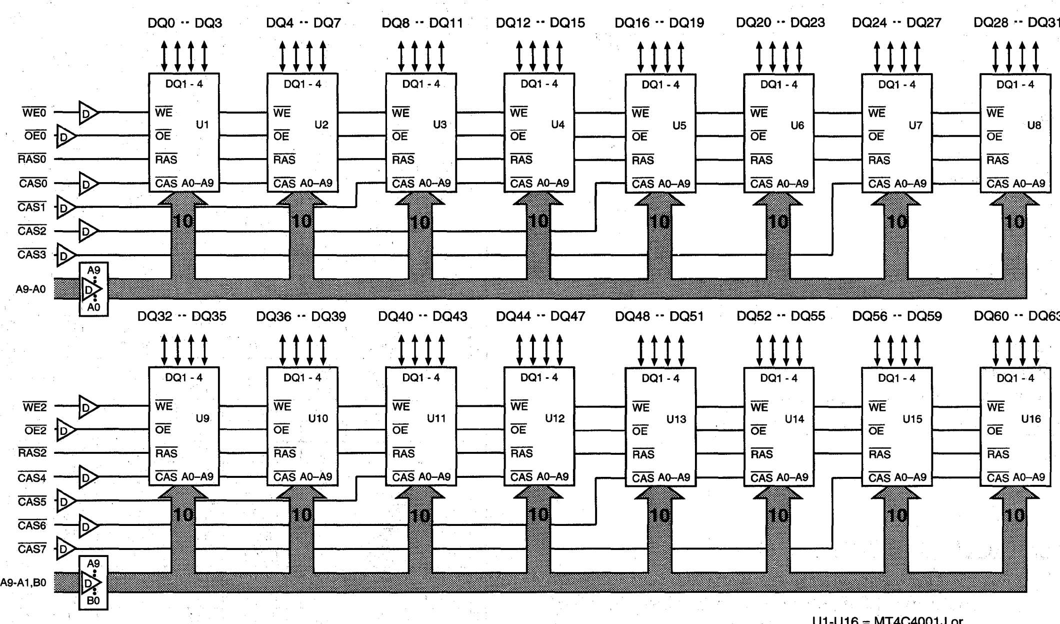
FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

REFRESH

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS addresses (A0/B0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. All inputs with the exception of RAS are redriven.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the ten row-address bits. Two $\overline{RAS}$ inputs allow for one x64 bank or two x32 banks.
28, 29, 46, 47, 112, 113, 130, 131	$\overline{CAS0}$-7	Buffered Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
27, 48	$\overline{WE0}$, $\overline{WE2}$	Buffered Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. $\overline{WE0}$ controls DQ0-DQ31. $\overline{WE2}$ controls DQ32-DQ63. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	$\overline{OE0}$, $\overline{OE2}$	Buffered Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. This signal may be driven, allowing LATE WRITE cycles.
33-37, 117-121, 126	A0-A9, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-5, 7-10, 13-17, 19-21, 52-53, 55-58, 60, 65, 67, 69-72, 74-76, 86-89, 91-94, 97-101, 103-105, 136-137, 139-142, 144, 149,151,153-156,158-160	DQ0-DQ63	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x64 mode only). For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	-	Presence-Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
41-42, 61-64, 111, 115, 125, 128, 145-148	RFU	-	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	Vcc	Supply	Power Supply: +5V ± 10%
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	Vss	Supply	Ground
83, 167	ID0, ID1	-	ID bit
132	$\overline{PDE}$	-	PD enable
11, 22, 24-25, 38-39, 50-51, 66, 77, 95, 106, 108-109, 114, 122-123, 129, 134-135, 150,161	NC	-	No connect.

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DATA-IN/OUT	NOTES
						^tR	^tC	DQ0-63	
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY WRITE		L	L	L	X	ROW	COL	Data-In	
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	
RAS ONLY REFRESH		H	X	X	X	ROW	n/a	High-Z	
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	
CBR REFRESH		H→L	L	H	X	X	X	High-Z	

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			NC	NC	NC	NC	NC			
2MB	256K x 64/72	9/9			Vss	Vss	Vss	Vss	Vss			
4MB	512K x 64/72	9/9			NC	Vss	Vss	Vss	Vss			
4MB	512K x 64/72/80	10/9			Vss	NC	Vss	Vss	Vss			
8MB	1 Meg x 64/72/80	10/9			NC	NC	Vss	Vss	Vss			
• 8MB	1 Meg x 64/72/80	10/10			Vss	Vss	NC	Vss	Vss			
16MB	2 Meg x 64/72/80	10/10			NC	Vss	NC	Vss	Vss			
16MB	2 Meg x 64/72/80	11/10			NC	Vss	Vss	NC	Vss			
32MB	4 Meg x 64/72/80	11/10			Vss	NC	Vss	NC	Vss			
32MB	4 Meg x 64/72/80	12/10			NC	NC	Vss	NC	Vss			
64MB	8 Meg x 64/72/80	12/10			Vss	Vss	NC	Vss	Vss			
Access Timing		80ns								NC	Vss	
		70ns								Vss	NC	
		60ns								NC	NC	
		50ns								Vss	Vss	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, No Parity	Vss									NC
		x72, Parity	NC									NC
		x72, ECC	Vss									Vss
		x80, ECC	NC									Vss

NOTE: Vss = ground.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	3.5	V_{CC}+0.5	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-0.5	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS7}$ A0-A9, B0 $\overline{WE0,2}$,$\overline{OE0,2}$	I_{I1}	-2	2	µA	
	$\overline{RAS0,2}$	I_{I2}	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ0-DQ63	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	8MB	32	32	32	mA	29
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	8MB	16	16	16	mA	29
			3.2	3.2	3.2	mA	29, 31
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	8MB	1,760	1,600	1,440	mA	3, 4, 29, 34
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	8MB	1,280	1,120	960	mA	3, 4, 29, 34
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	8MB	1,760	1,600	1,440	mA	3, 29, 34
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	8MB	1,760	1,600	1,440	mA	3, 5, 29
REFRESH CURRENT: Extended CBR (L-version only) Average power supply current, $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = Vcc -0.2V; A0/B0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	8MB	4.8	4.8	4.8	mA	3, 5, 7, 29, 34

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, B0	CI1		9	pF	2
Input Capacitance: WE0, WE2, OE0, OE2	CI2		9	pF	2
Input Capacitance: RAS0, RAS2	CI3		40	pF	2
Input Capacitance: CAS0 - CAS7	CI4		9	pF	2
Input/Output Capacitance: DQ0-DQ63	CIO		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	23
Access time from RAS	tRAC		60		70		80	ns	14, 23
Access time from CAS	tCAC		22		27		27	ns	15, 26
Access time from column-address	tAA		37		42		47	ns	26
Access time from CAS precharge	tCPA		42		47		52	ns	26
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	23
RAS hold time	tRSH	22		27		27		ns	26
RAS precharge time	tRP	45		50		60		ns	23
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	23
CAS hold time	tCSH	58		68		78		ns	25
CAS precharge time	tCPN	10		10		10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	23
RAS to CAS delay time	tRCD	18	38	18	43	18	53	ns	17, 27
CAS to RAS precharge time	tCRP	17		17		17		ns	26
Row-address setup time	tASR	7		7		7		ns	26
Row-address hold time	tRAH	8		8		8		ns	25
RAS to column-address delay time	tRAD	13	23	13	28	13	33	ns	18, 27
Column-address setup time	tASC	2		2		2		ns	24
Column-address hold time	tCAH	10		15		15		ns	23

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Column-address hold time (referenced to $\overline{RAS}$)	${}^tAR$	43		48		53		ns	25
Column-address to $\overline{RAS}$ lead time	${}^tRAL$	37		42		47		ns	26
Read command setup time	${}^tRCS$	2		2		2		ns	24
Read command hold time (referenced to $\overline{CAS}$)	${}^tRCH$	2		2		2		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	${}^tRRH$	0		0		0		ns	19, 23
$\overline{CAS}$ to output in Low-Z	${}^tCLZ$	2		2		2		ns	24
Output buffer turn-off delay	${}^tOFF$	5	22	5	27	5	27	ns	20, 28
$\overline{WE}$ command setup time	${}^tWCS$	2		2		2		ns	24
Write command hold time	${}^tWCH$	10		15		15		ns	23
Write command hold time (referenced to $\overline{RAS}$)	${}^tWCR$	43		53		58		ns	25
Write command pulse width	${}^tWP$	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	${}^tRWL$	22		27		27		ns	26
Write command to $\overline{CAS}$ lead time	${}^tCWL$	15		20		20		ns	23
Data-in setup time	${}^tDS$	2		2		2		ns	24, 30
Data-in hold time	${}^tDH$	17		22		22		ns	26, 30
Data-in hold time (referenced to $\overline{RAS}$)	${}^tDHR$	45		55		60		ns	23
Transition time (rise or fall)	${}^tT$	3	50	3	50	3	50	ns	9, 10, 23
Refresh period (1,024 cycles)	${}^tREF$		16/128*		16/128*		16/128*	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	${}^tRPC$	0		0		0		ns	23
$\overline{CAS}$ setup time (CBR REFRESH)	${}^tCSR$	12		12		12		ns	5, 24
$\overline{CAS}$ hold time (CBR REFRESH)	${}^tCHR$	8		8		8		ns	5, 25
$\overline{WE}$ hold time (CBR REFRESH)	${}^tWRH$	8		8		8		ns	22, 25
$\overline{WE}$ setup time (CBR REFRESH)	${}^tWRP$	12		12		12		ns	22, 24
$\overline{WE}$ hold time (WCBR test cycle)	${}^tWTH$	8		8		8		ns	22, 25
$\overline{WE}$ setup time	${}^tWTS$	12		12		12		ns	22, 24
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	${}^tORD$	0		0		0		ns	20
Output disable	${}^tOD$		15		20		20	ns	23
Output enable	${}^tOE$	15		20		20		ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	${}^tOEH$	15		20		20		ns	25
$\overline{RAS}$ to $\overline{WE}$ delay time	${}^tRWD$	90		100		110		ns	24, 32
Column-address to $\overline{WE}$ delay time	${}^tAWD$	55		65		70		ns	24, 32
$\overline{CAS}$ to $\overline{WE}$ delay time	${}^tCWD$	40		50		50		ns	24, 32

*L-version only.

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
23. Timing between the DRAMs and the module did not change with the addition of the line drivers.
24. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
26. A +7ns timing skew from the DRAM to the module resulted from the addition of line drivers.
27. A -2ns (MIN) and a -7ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
28. A +2ns (MIN) and a +7ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
29. The maximum current ratings are based with the memory operating or being refreshed in the x64 mode. The stated maximums may be reduced by approximately one-half when used in the x32 mode.
30. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
31. L-version only.
32. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
33. Refresh current increases if ^{t}RAS is extended beyond its minimum specification.
34. Column-address changed once each cycle.

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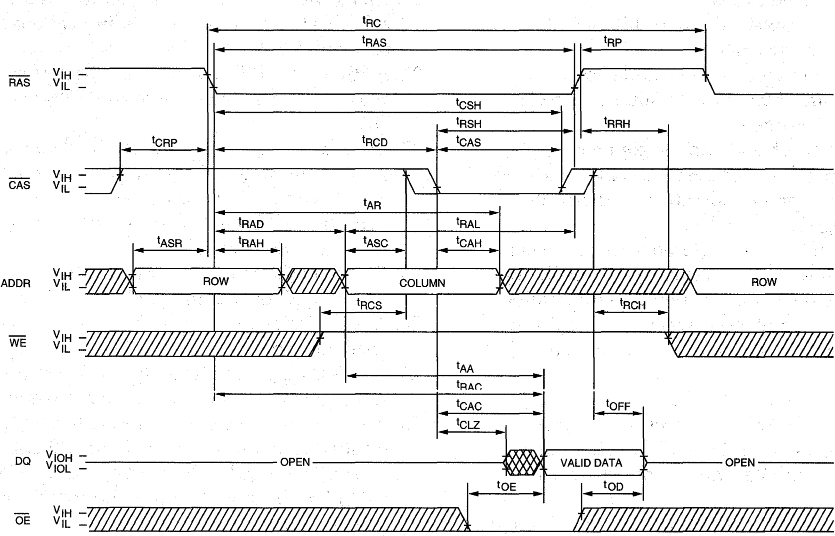
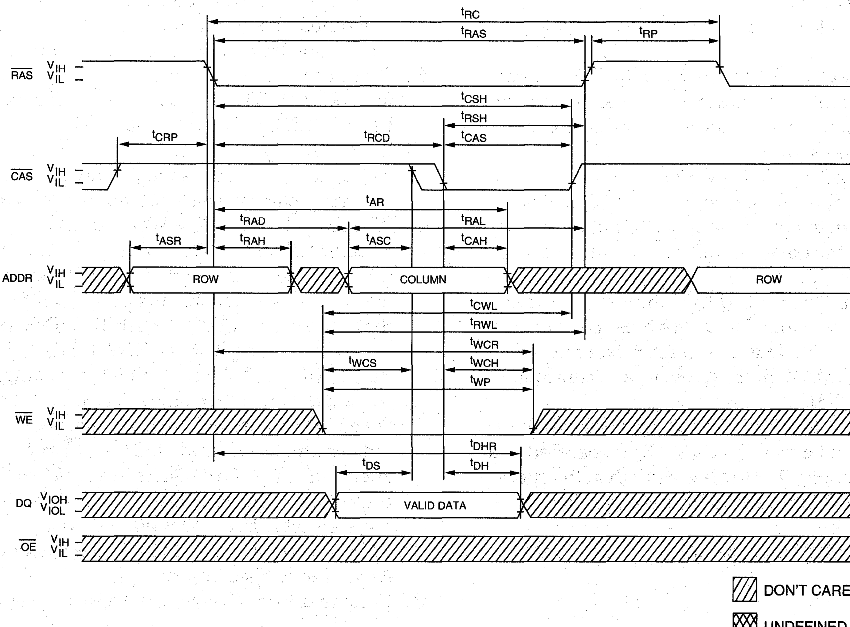
NEW ■ DRAM MODULE

READ CYCLE



EARLY WRITE CYCLE



DON'T CARE
UNDEFINED

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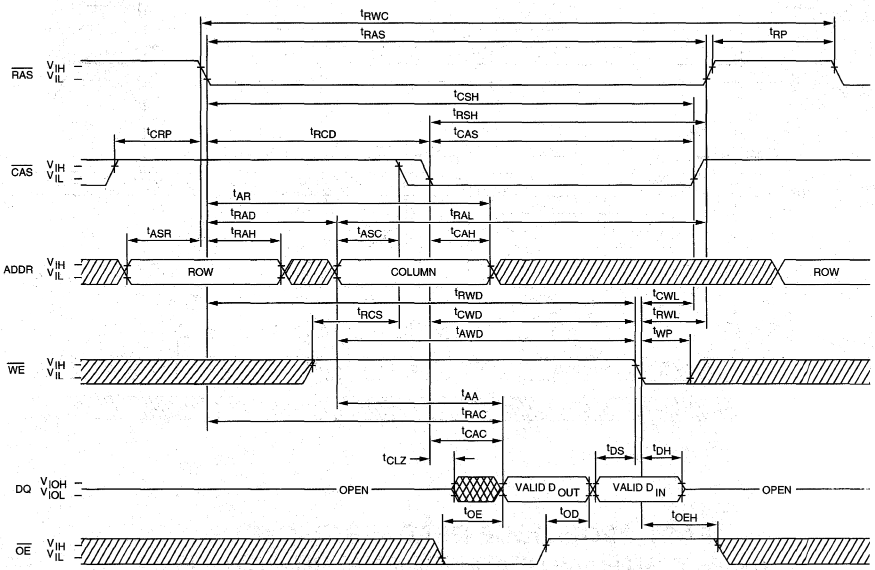
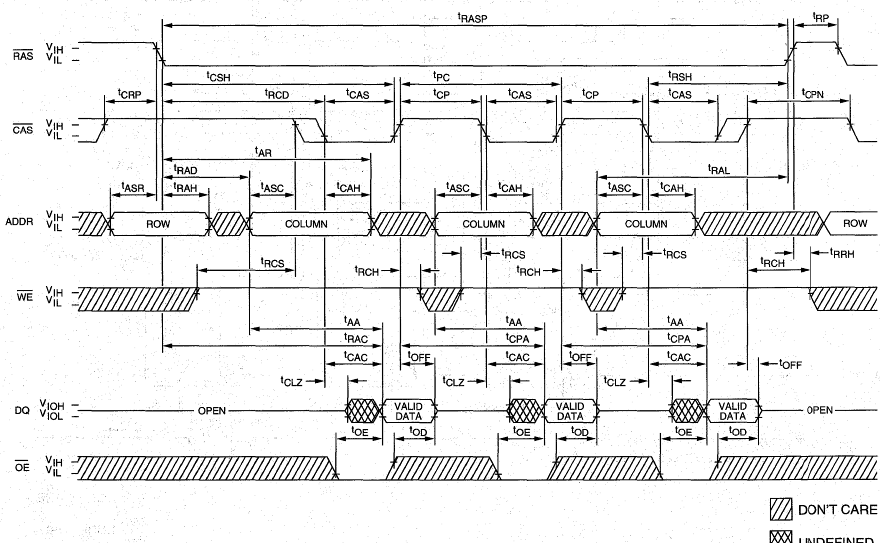
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



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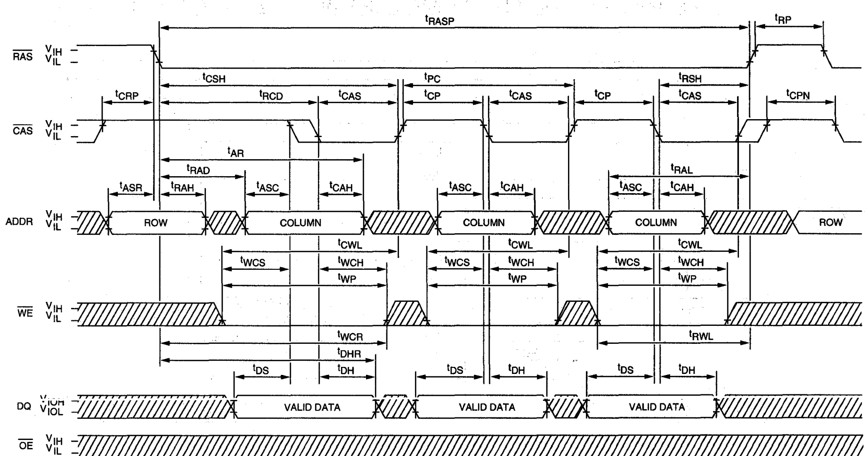
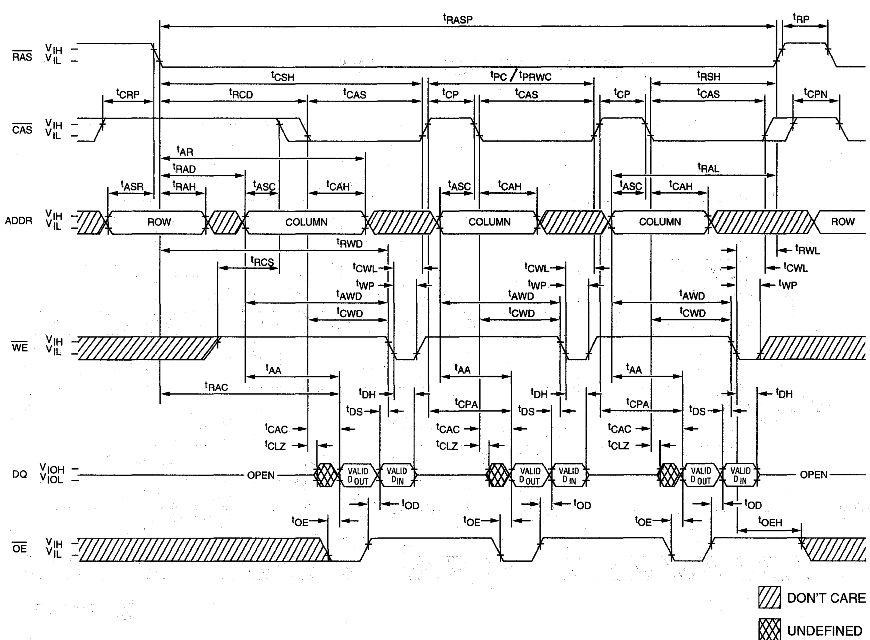
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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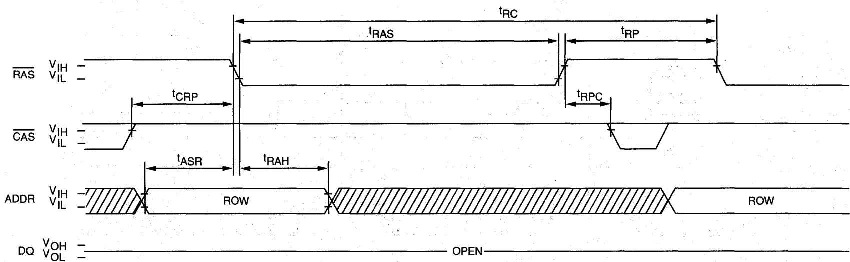
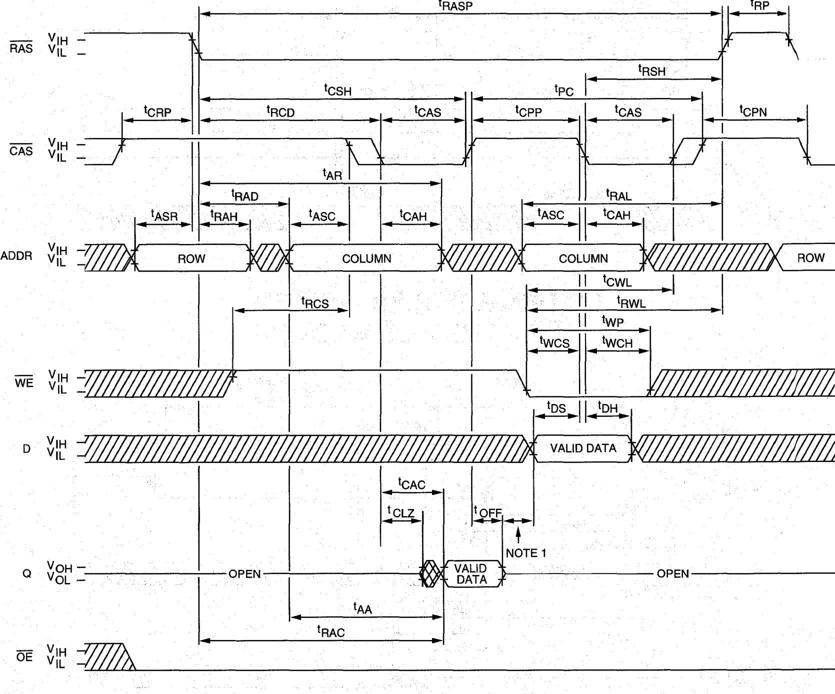
RAS ONLY REFRESH CYCLE
(ADDR = A0/B0-A9; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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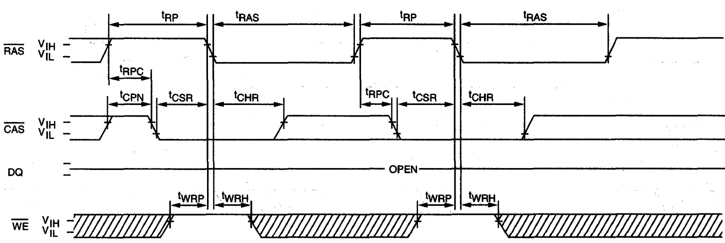
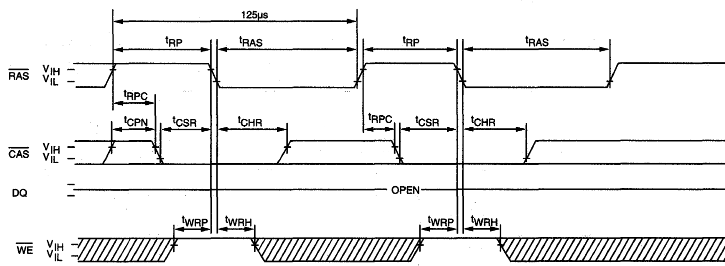
NEW DRAM MODULE

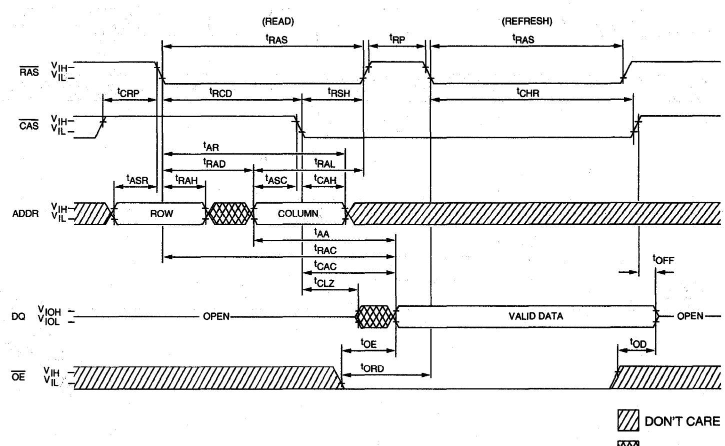
CBR REFRESH CYCLE
(A0/B0-A9, $\overline{OE}$ = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [31]
(A0/B0-A9, $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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DRAM MODULE

1 MEG x 64 DRAM

3.3V, OPTIONAL EXTENDED REFRESH, SELF REFRESH

FEATURES

- Industry-standard pinout in a 168-pin, dual read-out, single-in-line package
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 2.0mW standby; 1,200mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional Extended and SELF REFRESH modes
- 1,024-cycle refresh distributed across 16ms or 128ms
- FAST PAGE MODE access cycle

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Components
  - SOJ — D
  - TSOP — DT
- Packages
  - Leadless 168-pin, dual read-out DIMM — M
  - Leadless 168-pin, dual read-out DIMM (gold) — G
- Refresh
  - Standard — Blank
  - Low-power Extended Refresh, SELF REFRESH — S
- Part Number Example: MT16LDT164M-6 S

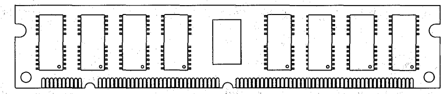
GENERAL DESCRIPTION

The MT16LD(T)164(S) is a randomly accessed solid-state memory containing 1,048,576 words organized in a x64 configuration. It is specially processed to operate from 3.0V to 3.6V for low voltage memory systems. The module has optional FAST PAGE MODE, which allows faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary.

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits.

READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$,

PIN ASSIGNMENT (Top View)
168-Pin, Dual Read-out DIMM
(DE-24) SOJ version
(DE-25) TSOP version



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{OE2}$	86	DQ32	128	RFU
3	DQ1	45	$\overline{RAS2}$	87	DQ33	129	NC
4	DQ2	46	$\overline{CAS4}$	88	DQ34	130	$\overline{CAS5}$
5	DQ3	47	$\overline{CAS6}$	89	DQ35	131	$\overline{CAS7}$
6	Vcc	48	$\overline{WE2}$	90	Vcc	132	PDE
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	NC	53	DQ17	95	NC	137	DQ49
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	Vcc	101	DQ44	143	Vcc
18	Vcc	60	DQ22	102	Vcc	144	DQ54
19	DQ13	61	RFU	103	DQ45	145	RFU
20	DQ14	62	RFU	104	DQ46	146	RFU
21	DQ15	63	RFU	105	DQ47	147	RFU
22	NC	64	RFU	106	NC	148	RFU
23	Vss	65	DQ23	107	Vss	149	DQ55
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ24	109	NC	151	DQ56
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{WE0}$	69	DQ25	111	RFU	153	DQ57
28	$\overline{CAS0}$	70	DQ26	112	$\overline{CAS1}$	154	DQ58
29	$\overline{CAS2}$	71	DQ27	113	$\overline{CAS3}$	155	DQ59
30	$\overline{RAS0}$	72	DQ28	11	NC	156	DQ60
31	$\overline{OE0}$	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ29	116	Vss	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	NC	119	A5	161	NC
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	NC	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

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whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

REFRESH

Preserve correct memory cell data by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms (128ms on S-version), regardless of sequence. The CBR and Extended CBR REFRESH cycles will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

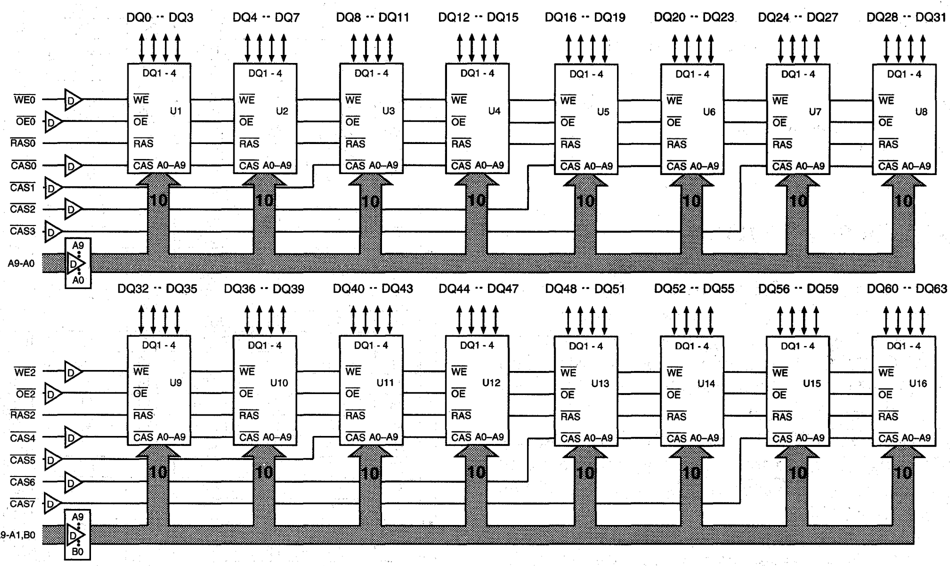
An optional SELF REFRESH mode is also available. The S-version allows the user the option of a fully static, low-power, data-retention mode, or a dynamic refresh mode at the extended refresh period. The module's SELF REFRESH mode is initiated by performing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified ^{t}RASS.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of ^{t}RPS ($\approx$ ^{t}RCns). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF refresh mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or burst refresh sequence, all rows must be refreshed within the average interal refresh rate, prior to the resumption of normal operation.

STANDBY

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. All inputs, with the exception of $\overline{RAS}$, are redriven.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits. Two $\overline{RAS}$ inputs allow for one x64 bank or two x32 banks.
28, 29, 46, 47, 112, 113, 130, 131	$\overline{CAS0}$-7	Buffered Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
27, 48	$\overline{WE0}$, $\overline{WE2}$	Buffered Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. $\overline{WE0}$ controls DQ0-DQ31. $\overline{WE2}$ controls DQ32-DQ63. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	$\overline{OE0}$, $\overline{OE2}$	Buffered Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE0}$ controls DQ0-DQ31. $\overline{OE2}$ controls DQ32-DQ63. These signals may be driven, allowing LATE WRITE cycles.
33-37, 117-121, 126	A0-A9, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-5, 7-10, 13-17, 19-21, 52-53, 55-58, 60, 65, 67, 69-72, 74-76, 86-89, 91-94, 97-101, 103-105, 136-137, 139-142, 144, 149,151,153-156,158-160	DQ0-DQ63	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x64 mode only). For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	-	Presence-Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
41-42, 61-64, 111, 115, 125, 128, 145-148	RFU	-	RFU: These pins should be left unconnected (reserved for future use).
6,18,26,40,49,59,73,84, 90,102,110,124,133,143, 157,168	Vcc	Supply	Power Supply: +3.3V ± 0.3V
1,12,23,32,43,54,68,78, 85,96,107,116,127,138, 152,162	Vss	Supply	Ground
83, 167	ID0, ID1	-	ID bit
132	$\overline{PDE}$	-	PD enable
11,22,24-25,38-39,50-51, 66,77,95,106,108-109, 114,122-123,129, 134-135,150,161	NC	-	No connect.

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DATA-IN/OUT	NOTES
						^tR	^tC	DQ0-63	
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY WRITE		L	L	L	X	ROW	COL	Data-In	
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	
$\overline{RAS}$ ONLY REFRESH		H	X	X	X	ROW	n/a	High-Z	
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	
CBR REFRESH		H→L	L	H	X	X	X	High-Z	
SELF REFRESH		H→L	L	H	X	X	X	High-Z	

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			NC	NC	NC	NC	NC			
2MB	256K x 64/72	9/9			Vss	Vss	Vss	Vss	Vss			
4MB	512K x 64/72	9/9			NC	Vss	Vss	Vss	Vss			
4MB	512K x 64/72/80	10/9			Vss	NC	Vss	Vss	Vss			
8MB	1 Meg x 64/72/80	10/9			NC	NC	Vss	Vss	Vss			
• 8MB	1 Meg x 64/72/80	10/10			Vss	Vss	NC	Vss	Vss			
16MB	2 Meg x 64/72/80	10/10			NC	Vss	NC	Vss	Vss			
16MB	2 Meg x 64/72/80	11/10			NC	Vss	Vss	NC	Vss			
32MB	4 Meg x 64/72/80	11/10			Vss	NC	Vss	NC	Vss			
32MB	4 Meg x 64/72/80	12/10			NC	NC	Vss	NC	Vss			
64MB	8 Meg x 64/72/80	12/10			Vss	Vss	NC	Vss	Vss			
Access Timing		80ns								NC	Vss	
		70ns								Vss	NC	
		60ns								NC	NC	
		50ns								Vss	Vss	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, Parity	Vss									NC
		x72, Parity	NC									NC
		x72, ECC	Vss									Vss
		x80, ECC	NC									Vss

NOTE: Vss = ground.

NEW DRAM MODULE

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = 3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC}+0.5V (All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS7}$ A0-A9, B0 $\overline{WE0,2}$,$\overline{OE0,2}$	I_{I1}	-2	2	µA	
	$\overline{RAS0}$,RAS2	I_{I2}	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ V_{CC}+0.5V) for each package input	DQ0-DQ63	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION		SYMBOL	SIZE	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC1}	8MB	16	16	16	mA	29
STANDBY CURRENT: (CMOS)		I_{CC2}	8MB	8	8	8	mA	29
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	S-version	I_{CC2}	8MB	1.6	1.6	1.6		
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC3}	8MB	1,280	1,120	960	mA	3, 4, 29, 35
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])		I_{CC4}	8MB	960	800	640	mA	3, 4, 29, 35
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])		I_{CC5}	8MB	1,280	1,120	960	mA	3, 29, 35
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC6}	8MB	1,280	1,120	960	mA	3, 5, 29
REFRESH CURRENT: Extended CBR (S-only) Average power supply current, $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = Vcc -0.2V; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)		I_{CC7}	8MB	2.4	2.4	2.4	mA	3, 5, 7, 29, 34
REFRESH CURRENT: SELF (S-only) Average power supply current during SELF REFRESH: CBR cycle with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc -0.2V; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open)		I_{CC8}	8MB	2.4	2.4	2.4	mA	5,29

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, B0	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$	C_{I2}		9	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		40	pF	2
Input Capacitance: $\overline{CAS0}$ - $\overline{CAS7}$	C_{I4}		9	pF	2
Input/Output Capacitance: DQ0-DQ63	C_{IO}		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	${}^tRC$	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	${}^tPC$	35		40		45		ns	23
Access time from $\overline{RAS}$	${}^tRAC$		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	${}^tCAC$		22		27		27	ns	15, 26
Access time from column-address	${}^tAA$		37		42		47	ns	26
Access time from $\overline{CAS}$ precharge	${}^tCPA$		42		47		52	ns	26
$\overline{RAS}$ pulse width	${}^tRAS$	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	${}^tRASP$	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	${}^tRSH$	22		27		27		ns	26
$\overline{RAS}$ precharge time	${}^tRP$	45		50		60		ns	23
$\overline{CAS}$ pulse width	${}^tCAS$	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	${}^tCSH$	58		68		78		ns	25
$\overline{CAS}$ precharge time	${}^tCPN$	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	${}^tCP$	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	${}^tRCD$	18	38	18	43	18	53	ns	17, 27
$\overline{CAS}$ to $\overline{RAS}$ precharge time	${}^tCRP$	17		17		17		ns	26
Row-address setup time	${}^tASR$	7		7		7		ns	26
Row-address hold time	${}^tRAH$	8		8		8		ns	25
$\overline{RAS}$ to column-address delay time	${}^tRAD$	13	23	13	28	13	33	ns	18, 27
Column-address setup time	${}^tASC$	2		2		2		ns	24
Column-address hold time	${}^tCAH$	10		15		15		ns	23
Column-address hold time (referenced to $\overline{RAS}$)	${}^tAR$	43		48		53		ns	25
Column-address to $\overline{RAS}$ lead time	${}^tRAL$	37		42		47		ns	26

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read command setup time	^{t}RCS	2		2		2		ns	24
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	2		2		2		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		0		ns	19, 23
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	2		2		2		ns	24
Output buffer turn-off delay	^{t}OFF	5	22	5	27	5	27	ns	20, 28
$\overline{WE}$ command setup time	^{t}WCS	2		2		2		ns	24, 36
Write command hold time	^{t}WCH	10		15		15		ns	23
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	43		53		58		ns	25
Write command pulse width	^{t}WP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	^{t}RWL	22		27		27		ns	26
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		20		ns	23
Data-in setup time	^{t}DS	2		2		2		ns	24, 30
Data-in hold time	^{t}DH	17		22		22		ns	26, 30
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		60		ns	23
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	9, 10, 23
Refresh period (1,024 cycles)	^{t}REF		16/128*		16/128*		16/128*	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	23
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	12		12		12		ns	5, 24
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	8		8		8		ns	5, 25
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	8		8		8		ns	22, 25
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	12		12		12		ns	22, 24
$\overline{WE}$ hold time (WCBR test cycle)	^{t}WTH	8		8		8		ns	22, 25
$\overline{WE}$ setup time	^{t}WTS	12		12		12		ns	22, 24
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	20
Output disable	^{t}OD		15		20		20	ns	23, 36
Output enable	^{t}OE	15		20		20		ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^{t}OEH	15		20		20		ns	25
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	90		100		110		ns	24, 32
Column-address to $\overline{WE}$ delay time	^{t}AWD	55		65		70		ns	24, 32
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	40		50		50		ns	24, 32
$\overline{RAS}$ pulse width entering SELF REFRESH	^{t}RASS	100		100		100		µs	33
$\overline{RAS}$ precharge time entering SELF REFRESH	^{t}RPS	110		130		150		ns	33
$\overline{CAS}$ hold time entering SELF REFRESH	^{t}CHD	10		10		10		ns	33

*S-version only

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 3.3V ±10%; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW AND $\overline{OE}$ = HIGH.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
23. Timing between the DRAMs and the module did not change with the addition of the line drivers.
24. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
26. A +7ns timing skew from the DRAM to the module resulted from the addition of line drivers.
27. A -2ns (MIN) and a -7ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
28. A +2ns (MIN) and a +7ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
29. The maximum current ratings are based with the memory operating or being refreshed in the x64 mode. The stated maximums may be reduced by approximately one-half when used in the x32 mode.
30. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
31. L-version only.
32. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY-WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
33. If the DRAM controller uses a BURST REFRESH, a BURST REFRESH of all rows must be executed upon exiting SELF REFRESH.

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NOTES (continued)

34. Refresh current increases if ^{t}RAS is extended beyond its minimum specification.
35. Column-address changed once each cycle.
36. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.

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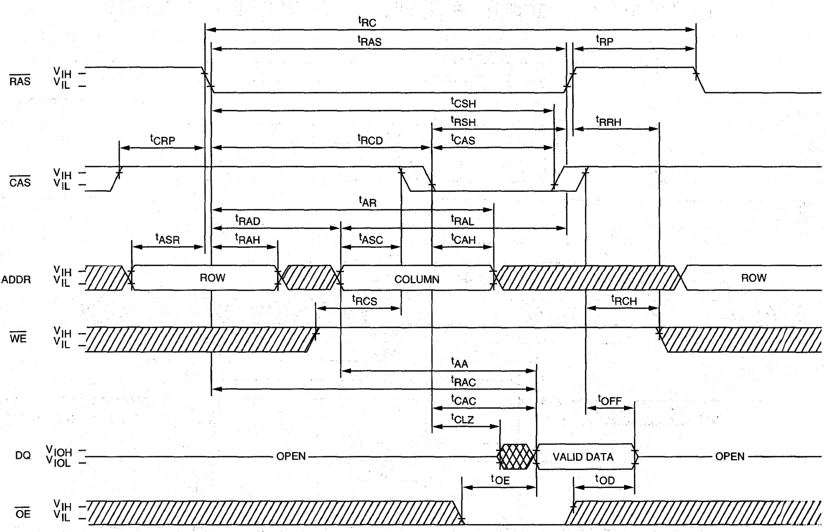
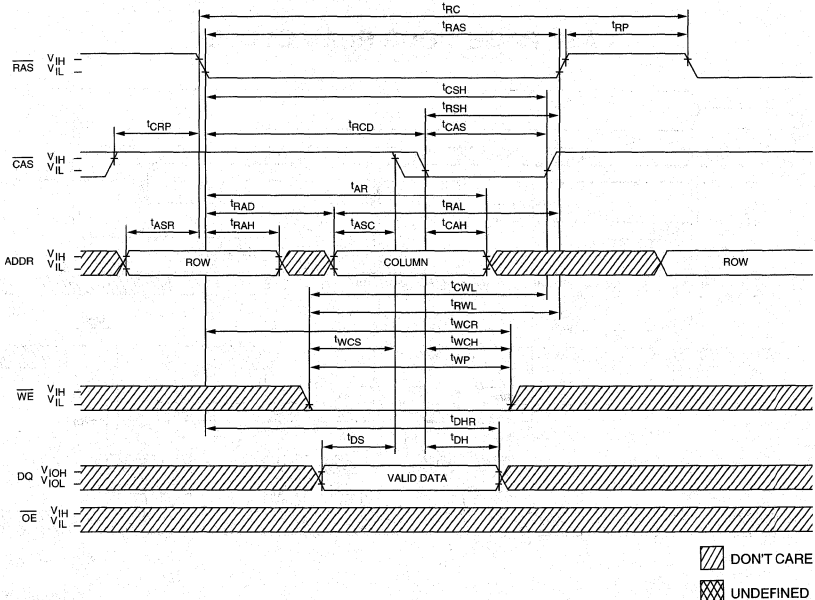
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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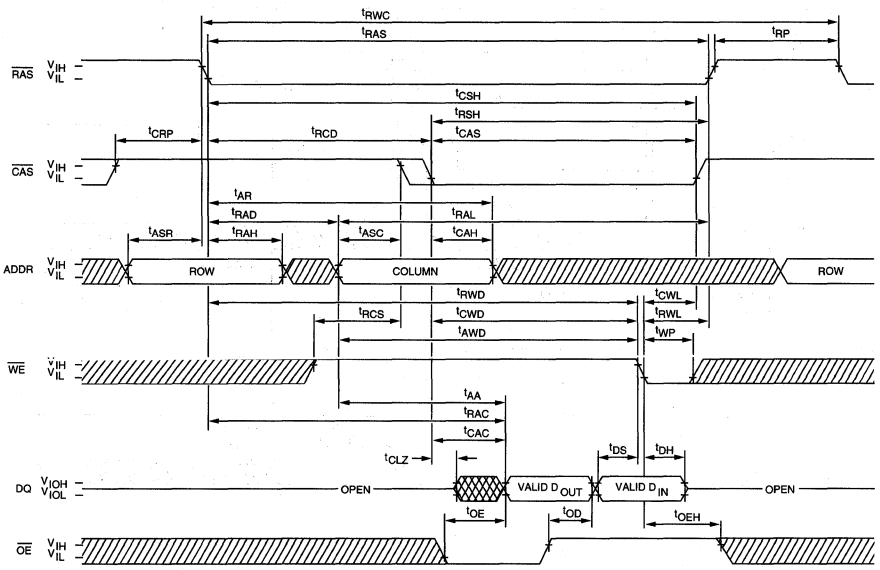
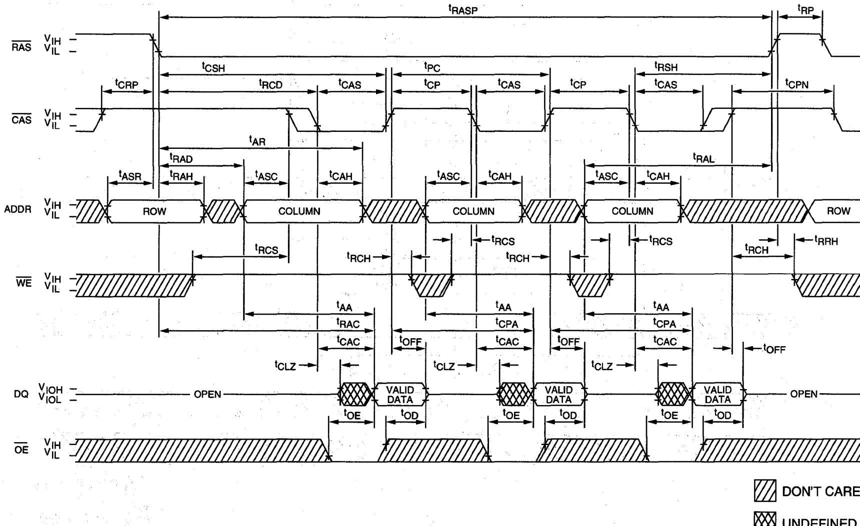
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST PAGE MODE READ CYCLE



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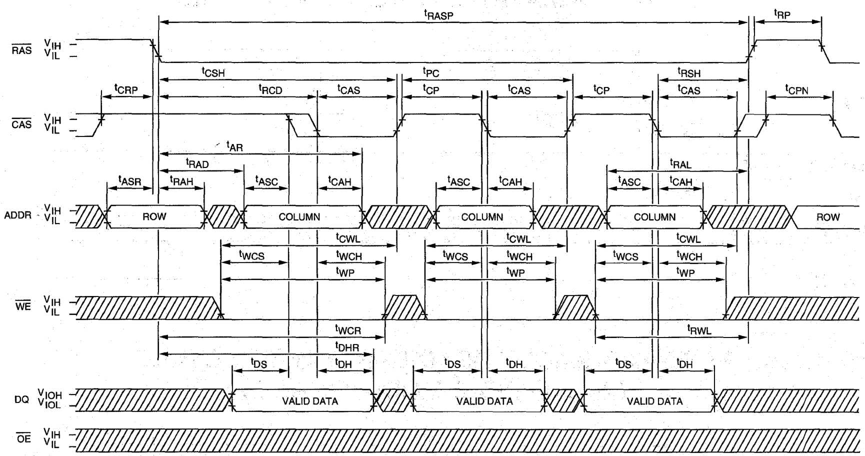
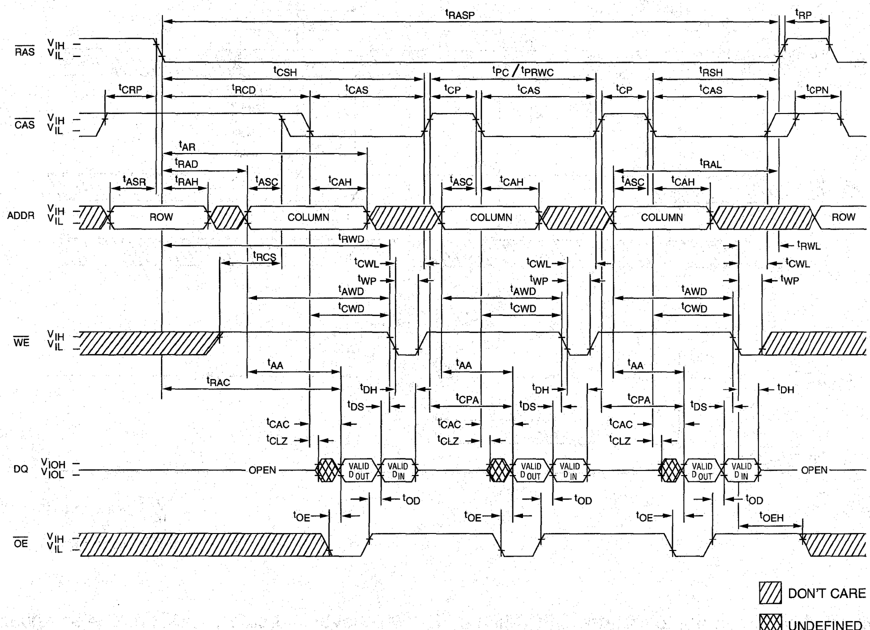
FAST-PAGE-MODE EARLY WRITE CYCLE



FAST-PAGE-MODE READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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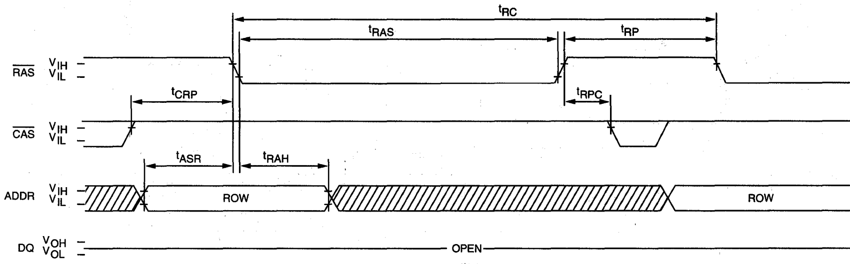
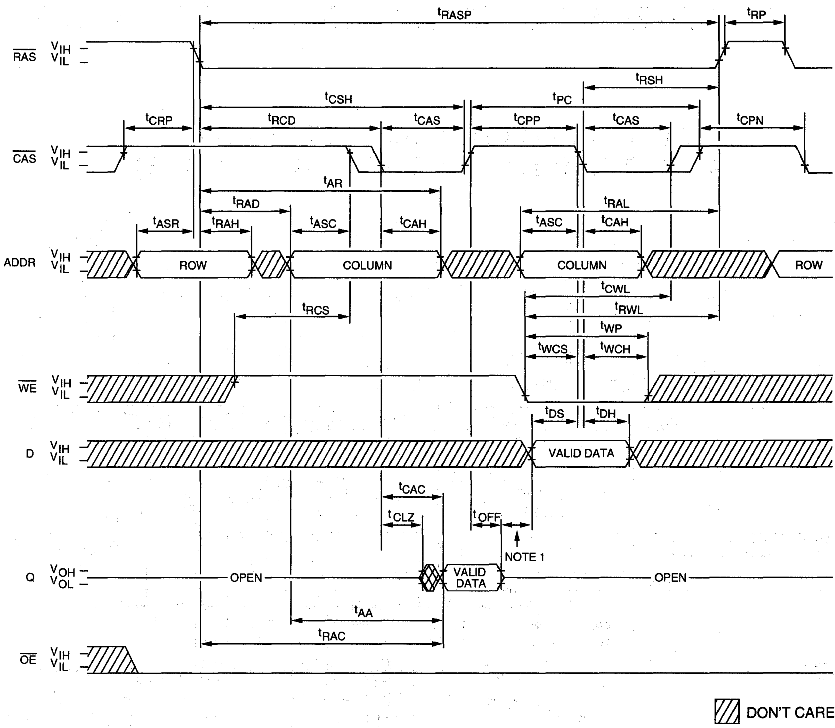
RAS ONLY REFRESH CYCLE
(ADDR = A0/B0-A9; and WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: ^{t}CPP(MIN) or ^{t}CP(whichever is greater) + ^{t}DS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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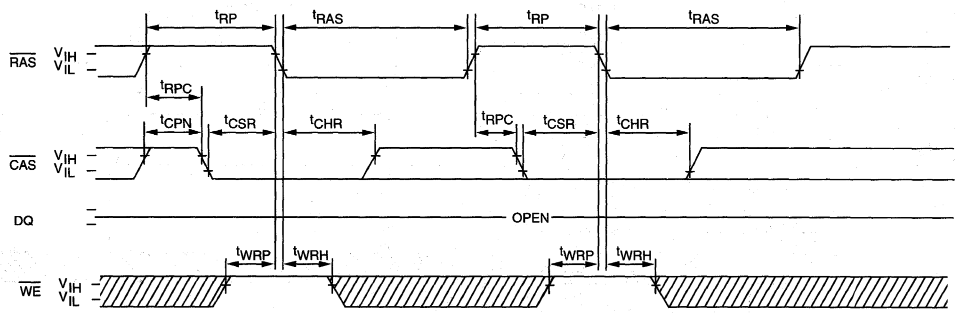
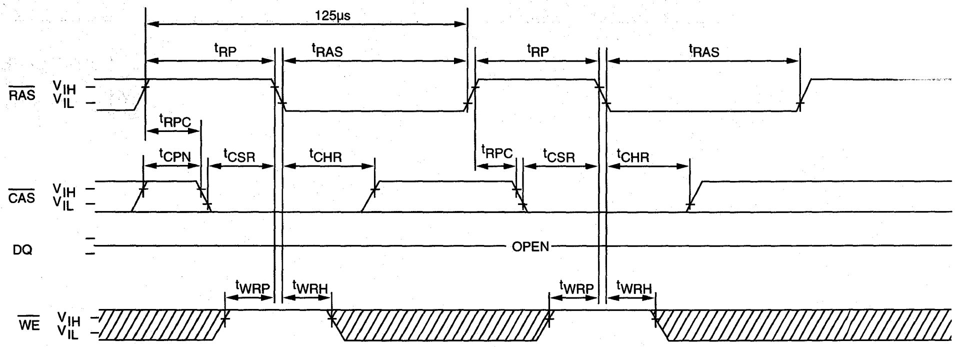
CBR REFRESH CYCLE
(A0/B0-A9, $\overline{OE}$ = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [31]
(A0/B0-A9, $\overline{OE}$ = DON'T CARE)



DON'T CARE

UNDEFINED

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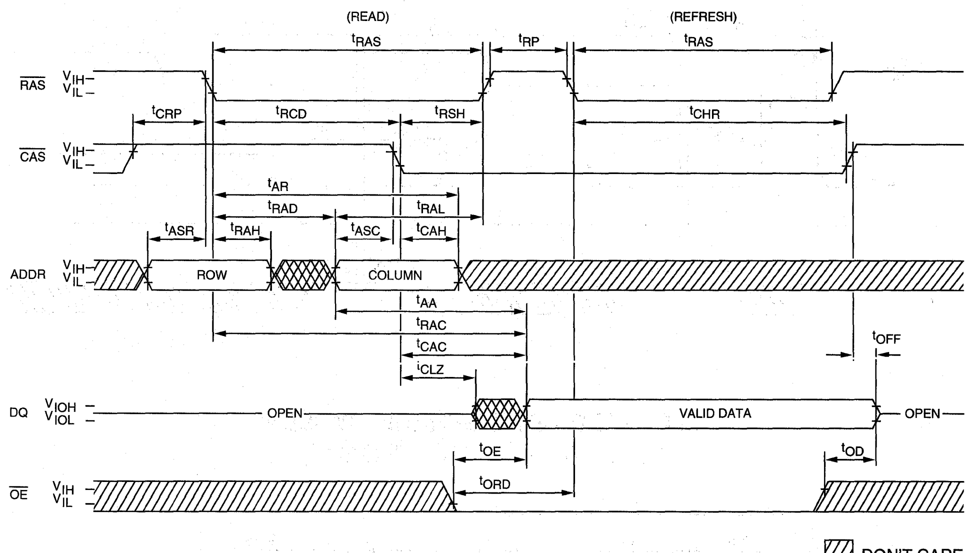
NEW DRAM MODULE

HIDDEN REFRESH CYCLE [21]
(WE = HIGH; OE = LOW)



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DRAM MODULE

4 MEG x 64 DRAM

5.0V FAST PAGE MODE

FEATURES

- Industry-standard pinout in a 168-pin, dual read-out, single in-line package
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 48mW standby; 3,200mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- All inputs are buffered except $\overline{RAS}$
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE access cycle

OPTIONS — MARKING

- Timing
  - 60ns access: -6
  - 70ns access: -7
- Components
  - SOJ: D
  - TSOP: DT
- Packages
  - Leadless 168-pin, dual read-out DIMM: M
  - Leadless 168-pin, dual read-out DIMM (gold): G
- Part Number Example: MT16DT464M-6

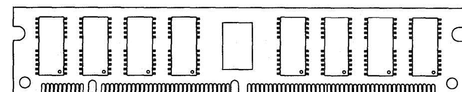
GENERAL DESCRIPTION

The MT16D(T)464 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x64 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0 /B0-A10) at a time. A0 is connected to DQ0-DQ31, while B0 is connected to DQ32-DQ63. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

PIN ASSIGNMENT (Top View)

168-Pin, Dual Read-out DIMM

(DE-22) SOJ version
(DE-23) TSOP version



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{OE2}$	86	DQ32	128	RFU
3	DQ1	45	$\overline{RAS2}$	87	DQ33	129	NC
4	DQ2	46	$\overline{CAS4}$	88	DQ34	130	$\overline{CAS5}$
5	DQ3	47	$\overline{CAS6}$	89	DQ35	131	$\overline{CAS7}$
6	Vcc	48	$\overline{WE2}$	90	Vcc	132	$\overline{PDE}$
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	NC	53	DQ17	95	NC	137	DQ49
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	Vcc	101	DQ44	143	Vcc
18	Vcc	60	DQ22	102	Vcc	144	DQ54
19	DQ13	61	RFU	103	DQ45	145	RFU
20	DQ14	62	RFU	104	DQ46	146	RFU
21	DQ15	63	RFU	105	DQ47	147	RFU
22	NC	64	RFU	106	NC	148	RFU
23	Vss	65	DQ23	107	Vss	149	DQ55
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ24	109	NC	151	DQ56
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{WE0}$	69	DQ25	111	RFU	153	DQ57
28	$\overline{CAS0}$	70	DQ26	112	$\overline{CAS1}$	154	DQ58
29	$\overline{CAS2}$	71	DQ27	113	$\overline{CAS3}$	155	DQ59
30	$\overline{RAS0}$	72	DQ28	11	NC	156	DQ60
31	$\overline{OE0}$	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ29	116	Vss	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	NC	119	A5	161	NC
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

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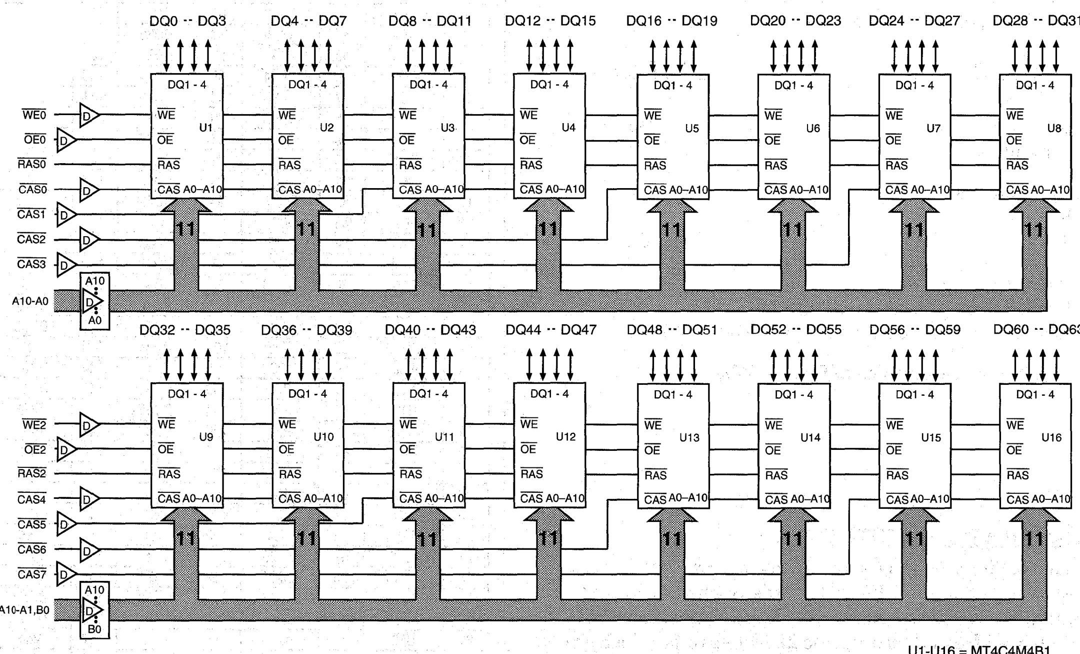
FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

REFRESH

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. All inputs with the exception of RAS are redriven.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the ten row-address bits. Two $\overline{RAS}$ inputs allow for one x64 bank or two x32 banks.
28, 29, 46, 47, 112, 113, 130, 131	$\overline{CAS0-7}$	Buffered Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the ten column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
27, 48	$\overline{WE0}$, $\overline{WE2}$	Buffered Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. $\overline{WE0}$ controls DQ0-DQ31. $\overline{WE2}$ controls DQ32-DQ63. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	$\overline{OE0}$, $\overline{OE2}$	Buffered Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE0}$ controls DQ0-DQ31. $\overline{OE2}$ controls DQ32-DQ63. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121, 126	A0-A10, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-5, 7-10, 13-17, 19-21, 52-53, 55-58, 60, 65, 67, 69-72, 74-76, 86-89, 91-94, 97-101, 103-105, 136-137, 139-142, 144, 149,151,153-156,158-160	DQ0-DQ63	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x64 mode only). For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	-	Presence-Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
41-42, 61-64, 111, 115, 125, 128, 145-148	RFU	-	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157,168	Vcc	Supply	Power Supply: +5V ± 10%
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	Vss	Supply	Ground
83, 167	ID0, ID1	-	ID bit
132	$\overline{PDE}$	-	PD enable
11, 22, 24-25, 38-39, 50-51, 66, 77, 95, 106, 108-109, 114, 122-123, 129, 134-135, 150, 161	NC	-	No connect.

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ0-63	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY WRITE		L	L	L	X	ROW	COL	Data-In	
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	
$\overline{RAS}$ ONLY REFRESH		H	X	X	X	ROW	n/a	High-Z	
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	
CBR REFRESH		H→L	L	H	X	X	X	High-Z	

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			NC	NC	NC	NC	NC			
2MB	256K x 64/72	9/9			Vss	Vss	Vss	Vss	Vss			
4MB	512K x 64/72	9/9			NC	Vss	Vss	Vss	Vss			
4MB	512K x 64/72/80	10/9			Vss	NC	Vss	Vss	Vss			
8MB	1 Meg x 64/72/80	10/9			NC	NC	Vss	Vss	Vss			
8MB	1 Meg x 64/72/80	10/10			Vss	Vss	NC	Vss	Vss			
16MB	2 Meg x 64/72/80	10/10			NC	Vss	NC	Vss	Vss			
16MB	2 Meg x 64/72/80	11/10			NC	Vss	Vss	NC	Vss			
• 32MB	4 Meg x 64/72/80	11/10			Vss	NC	Vss	NC	Vss			
32MB	4 Meg x 64/72/80	12/10			NC	NC	Vss	NC	Vss			
64MB	8 Meg x 64/72/80	12/10			Vss	Vss	NC	Vss	Vss			
Access Timing		80ns								NC	Vss	
		70ns								Vss	NC	
		60ns								NC	NC	
		50ns								Vss	Vss	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, No Parity	Vss									NC
		x72, Parity	NC									NC
		x72, ECC	Vss									Vss
		x80, ECC	NC									Vss

NOTE: Vss = ground.

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NEW DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	3.5	V_{CC}+1.5	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-0.5	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS7}$ A0-A9, B0 $\overline{WE0,2}$,$\overline{OE0,2}$	I_{I1}	-2	2	µA	
	$\overline{RAS0,2}$	I_{I2}	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ0-DQ63	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	32MB	32	32	mA	29
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	32MB	16	16	mA	29
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	32MB	1,920	1,760	mA	3, 4, 29, 34
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	32MB	1,440	1,280	mA	3, 4, 29, 34
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	32MB	1,920	1,760	mA	3, 29, 34
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	32MB	1,920	1,760	mA	3, 5, 29

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, B0	CI1		9	pF	2
Input Capacitance: WE0, WE2, OE0, OE2	CI2		9	pF	2
Input Capacitance: RAS0, RAS2	CI3		40	pF	2
Input Capacitance: CAS0 - CAS7	CI4		9	pF	2
Input/Output Capacitance: DQ0-DQ63	CIO		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		ns	23
Access time from RAS	tRAC	60		70		ns	14, 23
Access time from CAS	tCAC		22		27	ns	15, 26
Access time from column-address	tAA		37		42	ns	26
Access time from CAS precharge	tCPA		42		47	ns	26
RAS pulse width	tRAS	60	100,000	70	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	ns	23
RAS hold time	tRSH	22		27		ns	26
RAS precharge time	tRP	40		50		ns	23
CAS pulse width	tCAS	15	100,000	20	100,000	ns	23
CAS hold time	tCSH	58		68		ns	25
CAS precharge time	tCPN	10		10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	tCP	10		10		ns	23
RAS to CAS delay time	tRCD	18	38	18	43	ns	17, 27
CAS to RAS precharge time	tCRP	12		12		ns	26
Row-address setup time	tASR	7		7		ns	26
Row-address hold time	tRAH	8		8		ns	25
RAS to column-address delay time	tRAD	13	23	13	28	ns	18, 27
Column-address setup time	tASC	2		2		ns	24
Column-address hold time	tCAH	10		15		ns	23

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Column-address hold time (referenced to RAS)	^{t}AR	48		53		ns	25
Column-address to RAS lead time	^{t}RAL	37		42		ns	26
Read command setup time	^{t}RCS	2		2		ns	24
Read command hold time (referenced to CAS)	^{t}RCH	2		2		ns	19, 24
Read command hold time (referenced to RAS)	^{t}RRH	0		0		ns	19, 23
CAS to output in Low-Z	^{t}CLZ	2		2		ns	24
Output buffer turn-off delay	^{t}OFF	5	22	5	27	ns	20, 28
WE command setup time	^{t}WCS	2		2		ns	24
Write command hold time	^{t}WCH	10		15		ns	23
Write command hold time (referenced to RAS)	^{t}WCR	43		53		ns	25
Write command pulse width	^{t}WP	10		15		ns	23
Write command to RAS lead time	^{t}RWL	22		27		ns	26
Write command to CAS lead time	^{t}CWL	15		20		ns	23
Data-in setup time	^{t}DS	2		2		ns	24, 30
Data-in hold time	^{t}DH	17		22		ns	26, 30
Data-in hold time (referenced to RAS)	^{t}DHR	45		55		ns	23
Transition time (rise or fall)	^{t}T	3	50	3	50	ns	9, 10, 23
Refresh period (2,048 cycles)	^{t}REF		32		32	ms	
RAS to CAS precharge time	^{t}RPC	0		0		ns	23
CAS setup time (CBR REFRESH)	^{t}CSR	7		7		ns	5, 24
CAS hold time (CBR REFRESH)	^{t}CHR	13		13		ns	5, 25
WE hold time (CBR REFRESH)	^{t}WRH	8		8		ns	22, 25
WE setup time (CBR REFRESH)	^{t}WRP	12		12		ns	22, 24
WE hold time (WCBR test cycle)	^{t}WTH	8		8		ns	22, 25
WE setup time	^{t}WTS	12		12		ns	22, 24
OE setup prior to RAS during HIDDEN REFRESH cycle	^{t}ORD	0		0		ns	20
Output disable	^{t}OD		15		20	ns	23
Output enable	^{t}OE	15		20		ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	^{t}OEH	15		15		ns	25
RAS to WE delay time	^{t}RWD	85		95		ns	24, 32
Column-address to WE delay time	^{t}AWD	55		60		ns	24, 32
CAS to WE delay time	^{t}CWD	40		45		ns	24, 32

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 5V ±10%; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ᵗREF refresh requirement is exceeded.
8. AC characteristics assume ᵗT = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If CAS = VIH, data output is High-Z.
12. If CAS = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ᵗRCD < ᵗRCD (MAX). If ᵗRCD is greater than the maximum recommended value shown in this table, ᵗRAC will increase by the amount that ᵗRCD exceeds the value shown.
15. Assumes that ᵗRCD ≥ ᵗRCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ᵗCPN.
17. Operation within the ᵗRCD (MAX) limit ensures that ᵗRAC (MAX) can be met. ᵗRCD (MAX) is specified as a reference point only; if ᵗRCD is greater than the specified ᵗRCD (MAX) limit, access time is controlled exclusively by ᵗCAC.
18. Operation within the ᵗRAD (MAX) limit ensures that ᵗRAC (MIN) and ᵗCAC (MIN) can be met. ᵗRAD (MAX) is specified as a reference point only; if ᵗRAD is greater than the specified ᵗRAD (MAX) limit, access time is controlled exclusively by ᵗAA.
19. Either ᵗRCH or ᵗRRH must be satisfied for a READ cycle.
20. ᵗOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
22. ᵗWTS and ᵗWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ᵗWRP and ᵗWRH in the CBR REFRESH cycle.
23. Timing between the DRAMs and the module did not change with the addition of the line drivers.
24. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
26. A +7ns timing skew from the DRAM to the module resulted from the addition of line drivers.
27. A -2ns (MIN) and a -7ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
28. A +2ns (MIN) and a +7ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
29. The maximum current ratings are based with the memory operating or being refreshed in the x64 mode. The stated maximums may be reduced by approximately one-half when used in the x32 mode.
30. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
31. L-version only.
32. ᵗWCS, ᵗRWD, ᵗAWD and ᵗCWD are not restrictive operating parameters. ᵗWCS applies to EARLY WRITE cycles. ᵗRWD, ᵗAWD and ᵗCWD apply to READ-MODIFY-WRITE cycles. If ᵗWCS ≥ ᵗWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ᵗRWD ≥ ᵗRWD (MIN), ᵗAWD ≥ ᵗAWD (MIN) and ᵗCWD ≥ ᵗCWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE WRITE (OE-controlled) cycle. ᵗWCS, ᵗRWD, ᵗCWD and ᵗAWD are not applicable in a LATE WRITE cycle.
33. Refresh current increases if ᵗRAS is extended beyond its minimum specification.
34. Column-address changed once each cycle.

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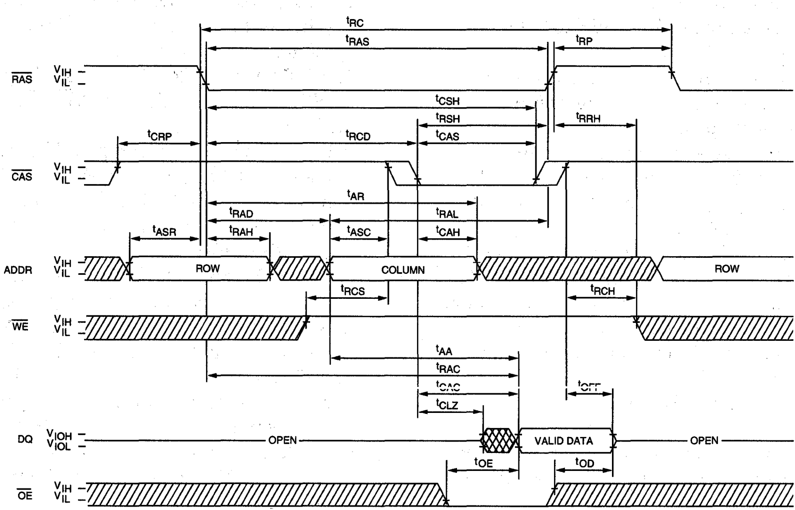
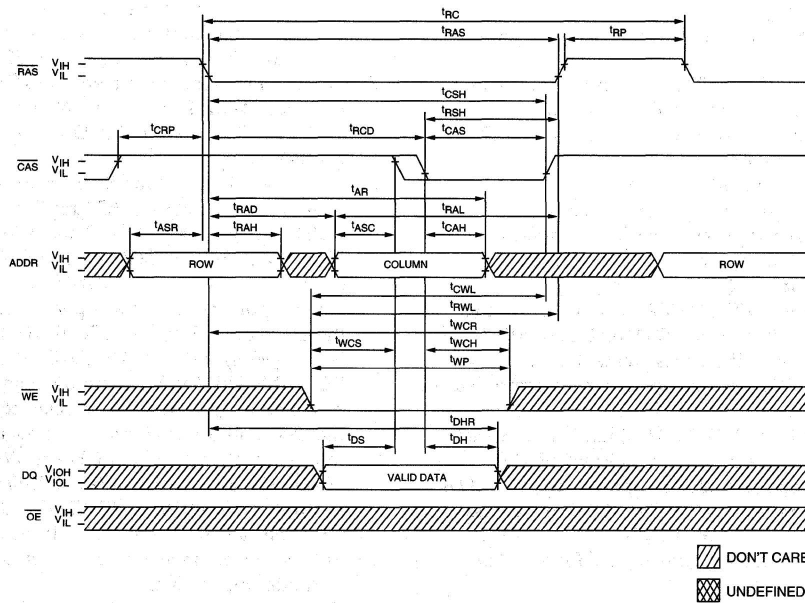
READ CYCLE



EARLY WRITE CYCLE



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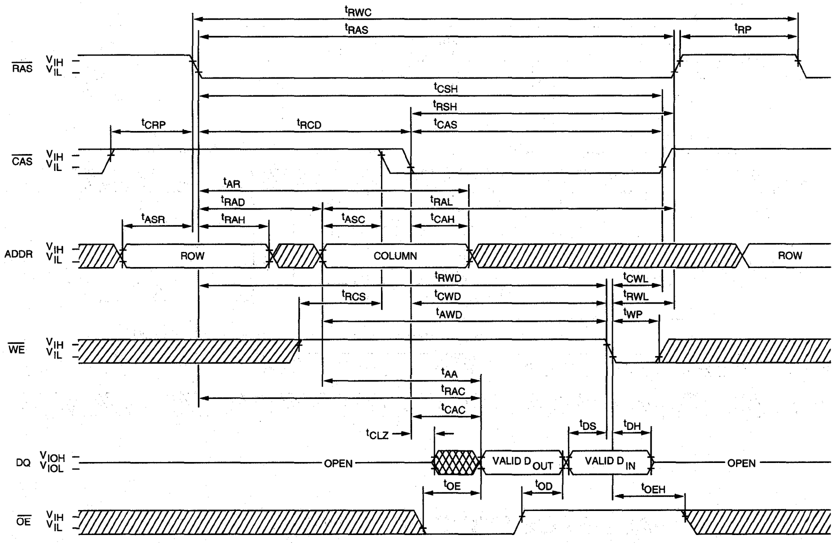
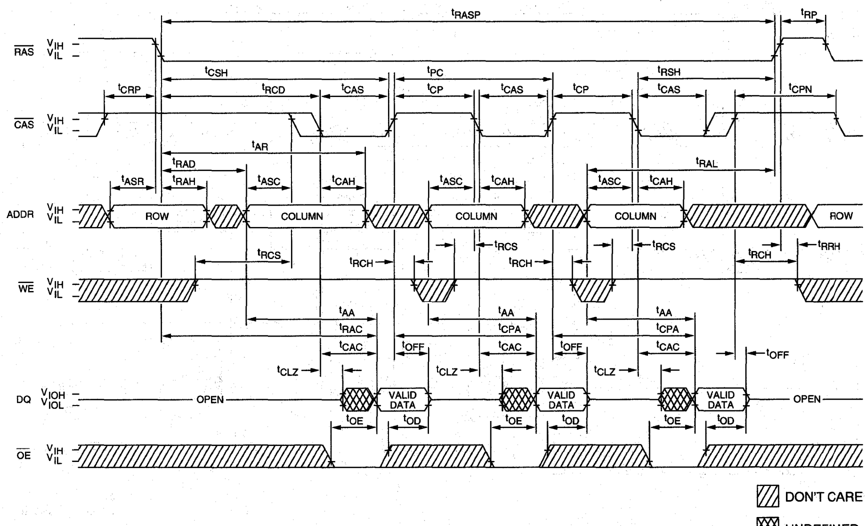
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



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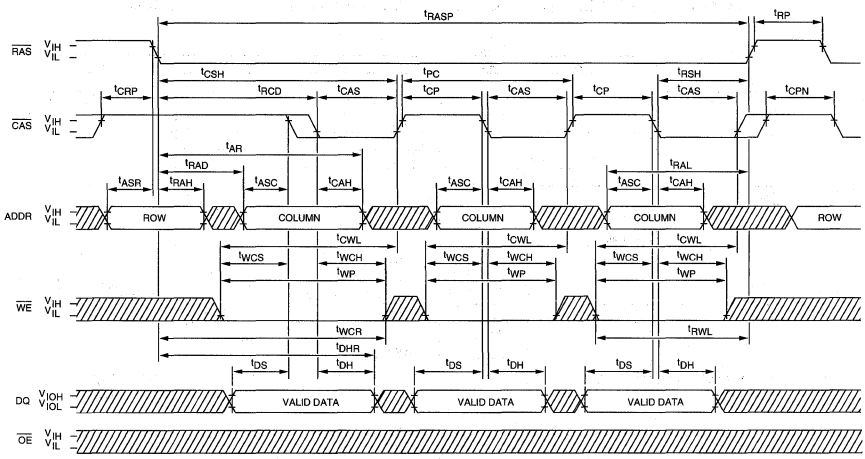
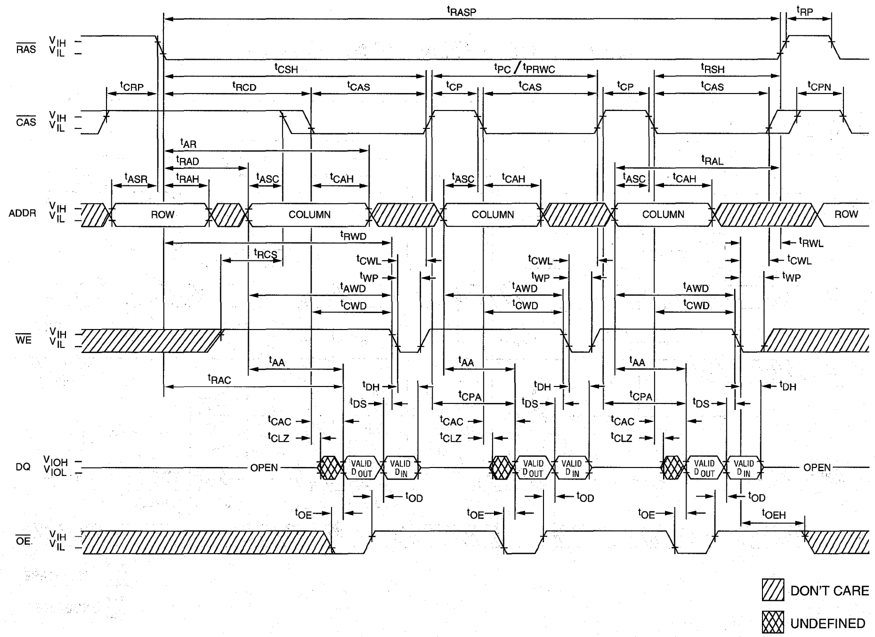
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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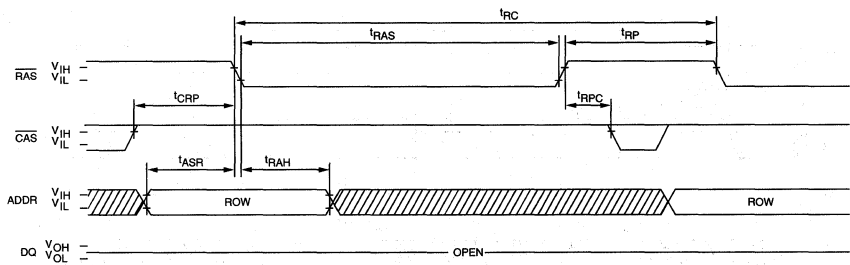
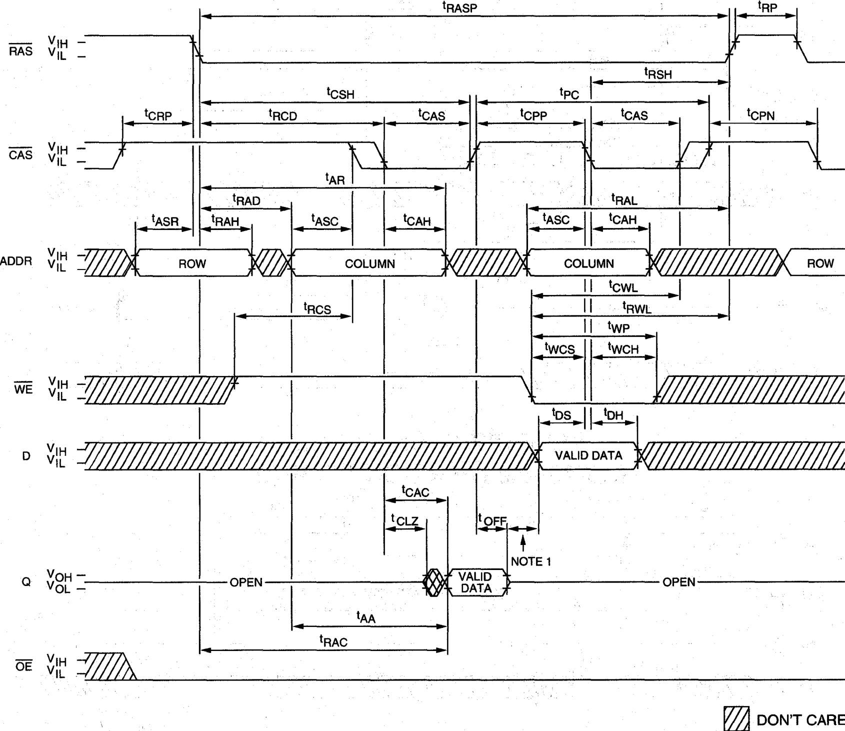
RAS ONLY REFRESH CYCLE

(ADDR = A0/B0-A10; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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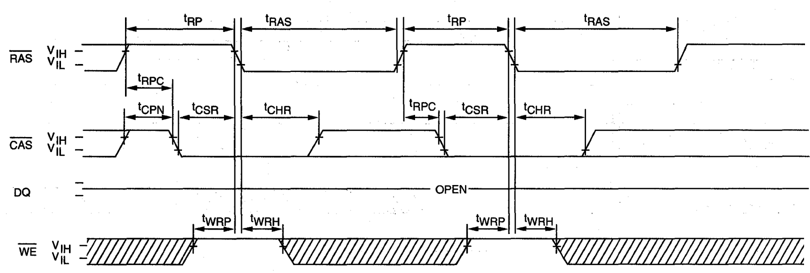
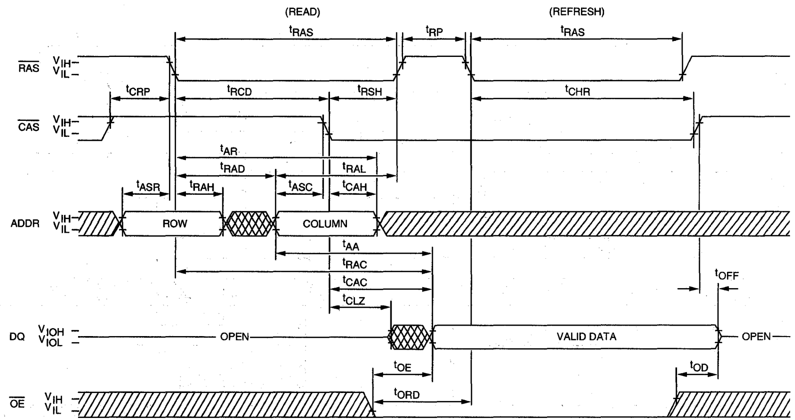
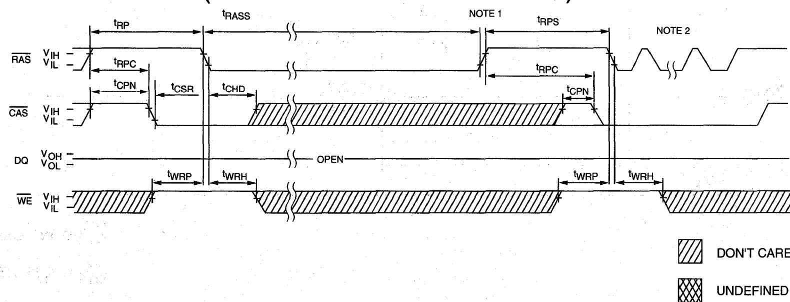
CBR REFRESH CYCLE
(A0/B0-A10, $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



SELF REFRESH CYCLE
(A0-A9 and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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DRAM MODULE

4 MEG x 64 DRAM

3.3V, OPTIONAL SELF REFRESH

FEATURES

- Industry-standard pinout in a 168-pin, dual read-out, single-in-line package
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 16mW standby; 2,400mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and SELF
- 2,048-cycle refresh distributed across 32ms or 2,048-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Optional SELF REFRESH mode, with Extended Refresh

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Components	
SOJ	D
TSOP	DT
• Packages	
Leadless 168-pin, dual read-out DIMM	M
Leadless 168-pin, dual read-out DIMM (gold)	G
• Refresh	
Standard	Blank
Low-power SELF REFRESH	S

- Part Number Example: MT16LDT464G-6 S

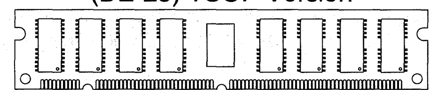
GENERAL DESCRIPTION

The MT16LD(T)464(S) is a randomly accessed solid-state memory containing 4,194,304 words organized in a x64 configuration. It is specially processed to operate from 3.0V to 3.6V for low voltage memory systems. The module has optional FAST PAGE MODE, which allows faster data operations (READ or WRITE) within a row-address-defined page boundary.

During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0 / B0-A10) at a time. A0 is connected to DQ0-DQ31, while B0 is connected to DQ32-DQ63. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits.

READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle,

PIN ASSIGNMENT (Top View)
168-Pin, Dual Read-out DIMM
(DE-24) SOJ Version
(DE-25) TSOP Version



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{OE2}$	86	DQ32	128	RFU
3	DQ1	45	$\overline{RAS2}$	87	DQ33	129	NC
4	DQ2	46	$\overline{CAS4}$	88	DQ34	130	$\overline{CAS5}$
5	DQ3	47	$\overline{CAS6}$	89	DQ35	131	$\overline{CAS7}$
6	Vcc	48	$\overline{WE2}$	90	Vcc	132	$\overline{PDE}$
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	NC	53	DQ17	95	NC	137	DQ49
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	Vcc	101	DQ44	143	Vcc
18	Vcc	60	DQ22	102	Vcc	144	DQ54
19	DQ13	61	RFU	103	DQ45	145	RFU
20	DQ14	62	RFU	104	DQ46	146	RFU
21	DQ15	63	RFU	105	DQ47	147	RFU
22	NC	64	RFU	106	NC	148	RFU
23	Vss	65	DQ23	107	Vss	149	DQ55
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ24	109	NC	151	DQ56
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{WE0}$	69	DQ25	111	RFU	153	DQ57
28	$\overline{CAS0}$	70	DQ26	112	$\overline{CAS1}$	154	DQ58
29	$\overline{CAS2}$	71	DQ27	113	$\overline{CAS3}$	155	DQ59
30	$\overline{RAS0}$	72	DQ28	11	NC	156	DQ60
31	$\overline{OE0}$	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ29	116	Vss	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	NC	119	A5	161	NC
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

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data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, and the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS-ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms (128ms "S" option), regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

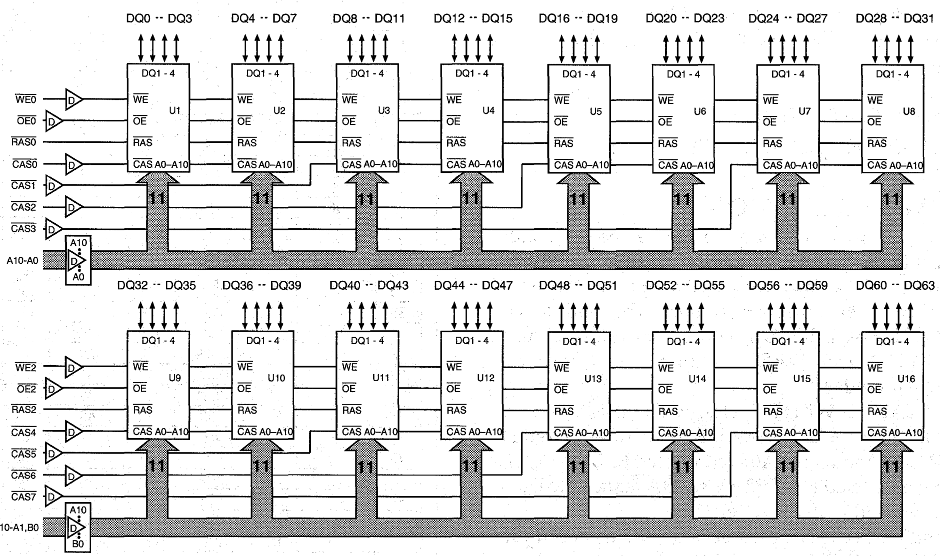
An optional SELF REFRESH mode is also available. The "S" option allows the user the option of a fully static, low-power, data-retention mode, or a dynamic refresh mode at the extended refresh period of 128ms, four times longer than the standard 32ms specifications. The module's SELF REFRESH mode is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" option allows for extended refresh rate of 62.5µs per row if using distributed CBR refresh. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum of an operation cycle, ^{t}RPS ($\approx^{t}$RCns). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS only or burst refresh sequence, all 2,048 rows must be refreshed within 300µs prior to the resumption of normal operation.

STANDBY

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. All inputs with the exception of RAS are redriven.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits. Two $\overline{RAS}$ inputs allow for one x64 bank or two x32 banks.
28, 29, 46, 47, 112, 113, 130, 131	$\overline{CAS0-7}$	Buffered Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
27, 48	$\overline{WE0}$, $\overline{WE2}$	Buffered Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. $\overline{WE0}$ controls DQ0-DQ31. $\overline{WE2}$ controls DQ32-DQ63. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	$\overline{OE0}$, $\overline{OE2}$	Buffered Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE0}$ controls DQ0-DQ31. $\overline{OE2}$ controls DQ32-DQ63. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121, 126	A0-A10, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-5, 7-10, 13-17, 19-21, 52-53, 55-58, 60, 65, 67, 69-72, 74-76, 86-89, 91-94, 97-101, 103-105, 136-137, 139-142, 144, 149,151,153-156,158-160	DQ0-DQ63	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x64 mode only). For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	-	Presence-Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
41-42, 61-64, 111, 115, 125, 128, 145-148	RFU	-	RFU: These pins should be left unconnected (reserved for future use).
6,18,26,40,49,59,73,84, 90,102,110,124,133,143, 157,168	Vcc	Supply	Power Supply: +3.3V ± 0.3V
1,12,23,32,43,54,68,78, 85,96,107,116,127,138, 152,162	Vss	Supply	Ground
83, 167	ID0, ID1	-	ID bit
132	$\overline{PDE}$	-	PD enable
11,22,24-25,38-39,50-51, 66,77,95,106,108-109, 114,122-123,129, 134-135,150,161	NC	-	No connect

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ᵗR	ADDRESSES ᵗC	DATA-IN/OUT DQ0-63	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY WRITE		L	L	L	X	ROW	COL	Data-In	
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	
$\overline{RAS}$ ONLY REFRESH		H	X	X	X	ROW	n/a	High-Z	
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	
CBR REFRESH		H→L	L	H	X	X	X	High-Z	
SELF REFRESH		H→L	L	H	X	X	X	High-Z	

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			NC	NC	NC	NC	NC			
2MB 4MB	256K x 64/72 512K x 64/72	9/9 9/9			Vss NC	Vss Vss	Vss Vss	Vss Vss	Vss Vss			
4MB 8MB	512K x 64/72/80 1 Meg x 64/72/80	10/9 10/9			Vss NC	NC NC	Vss Vss	Vss Vss	Vss Vss			
8MB 16MB	1 Meg x 64/72/80 2 Meg x 64/72/80	10/10 10/10			Vss NC	Vss Vss	NC NC	Vss Vss	Vss Vss			
16MB	2 Meg x 64/72/80	11/10			NC	Vss	Vss	NC	Vss			
• 32MB	4 Meg x 64/72/80	11/10			Vss	NC	Vss	NC	Vss			
32MB 64MB	4 Meg x 64/72/80 8 Meg x 64/72/80	12/10 12/10			NC Vss	NC Vss	Vss NC	NC Vss	Vss Vss			
Access Timing		80ns								NC	Vss	
		70ns								Vss	NC	
		60ns								NC	NC	
		50ns								Vss	Vss	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, Parity	Vss									NC
		x72, Parity	NC									NC
		x72, ECC	Vss									Vss
		x80, ECC	NC									Vss

NOTE: Vss = ground.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 4, 6, 7) (V_{CC} = 3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 3.6V (All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS7}$ A0-A9, B0 $\overline{WE0}$,2,$\overline{OE0}$,2	I_{I1}	-2	2	µA	
	$\overline{RAS0}$,2	I_{I2}	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 3.6V) for each package input	DQ0-DQ63	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION		SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC1}	32MB	16	16	mA	29
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	STD	I_{CC2}	32MB	8	8	mA	29
	S	I_{CC2}	32MB	2.4	2.4	mA	29
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC3}	32MB	1,920	1,760	mA	3, 4, 29, 34
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])		I_{CC4}	32MB	1,440	1,280	mA	3, 4, 29, 34
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])		I_{CC5}	32MB	1,920	1,760	mA	22, 26, 29
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC6}	32MB	1,920	1,760	mA	19, 22, 29
REFRESH CURRENT: Extended CBR (S only) Average power supply current, $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = Vcc -0.2V; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)		I_{CC7}	32MB	4.8	4.8	mA	3, 19, 22, 25, 29
REFRESH CURRENT: SELF (S only) Average power supply current during SELF REFRESH: CBR cycle with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc -0.2V; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open)		I_{CC8}	32MB	4.8	4.8	mA	19, 29

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +4.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, B0	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$	C_{I2}		9	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		40	pF	2
Input Capacitance: $\overline{CAS0}$ - $\overline{CAS7}$	C_{I4}		9	pF	2
Input/Output Capacitance: DQ0-DQ63	C_{IO}		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	23
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14, 23
Access time from $\overline{CAS}$	^tCAC		22		27	ns	15, 26
Access time from column-address	^tAA		37		42	ns	26
Access time from $\overline{CAS}$ precharge	^tCPA		42		47	ns	26
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	23
$\overline{RAS}$ hold time	^tRSH	22		27		ns	26
$\overline{RAS}$ precharge time	^tRP	45		50		ns	23
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	^tCSH	58		68		ns	25
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	18	38	18	43	ns	17, 27
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	17		17		ns	26
Row-address setup time	^tASR	7		7		ns	26
Row-address hold time	^tRAH	8		8		ns	25
$\overline{RAS}$ to column-address delay time	^tRAD	13	23	13	28	ns	18, 27
Column-address setup time	^tASC	2		2		ns	24
Column-address hold time	^tCAH	10		15		ns	23

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NEW DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Column-address hold time (referenced to RAS)	^tAR	48		53		ns	25
Column-address to RAS lead time	^tRAL	37		42		ns	26
Read command setup time	^tRCS	2		2		ns	24
Read command hold time (referenced to CAS)	^tRCH	2		2		ns	19, 24
Read command hold time (referenced to RAS)	^tRRH	0		0		ns	19, 23
CAS to output in Low-Z	^tCLZ	5		5		ns	24, 35
Output buffer turn-off delay	^tOFF	5	22	5	27	ns	20, 28
WE command setup time	^tWCS	2		2		ns	24
Write command hold time	^tWCH	10		15		ns	23
Write command hold time (referenced to RAS)	^tWCR	43		53		ns	25
Write command pulse width	^tWP	10		15		ns	23
Write command to RAS lead time	^tRWL	22		27		ns	26
Write command to CAS lead time	^tCWL	15		20		ns	23
Data-in setup time	^tDS	2		2		ns	24, 30
Data-in hold time	^tDH	17		22		ns	26, 30
Data-in hold time (referenced to RAS)	^tDHR	45		55		ns	23
Transition time (rise or fall)	^tT	3	50	3	50	ns	9, 10, 23
Refresh period (2,048 cycles)	^tREF		32/128*		32/128*	ms	
RAS to CAS precharge time	^tRPC	0		0		ns	23
CAS setup time (CBR REFRESH)	^tCSR	12		12		ns	5, 24
CAS hold time (CBR REFRESH)	^tCHR	8		8		ns	5, 25
WE hold time (CBR REFRESH)	^tWRH	8		8		ns	22, 25
WE setup time (CBR REFRESH)	^tWRP	12		12		ns	22, 24
WE hold time (WCBR test cycle)	^tWTH	8		8		ns	22, 25
WE setup time	^tWTS	12		12		ns	22, 24
OE setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		ns	20
Output disable	^tOD		15		20	ns	23
Output enable	^tOE	15		20		ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	^tOEH	15		20		ns	25
RAS to WE delay time	^tRWD	90		100		ns	24, 32
Column-address to WE delay time	^tAWD	55		65		ns	24, 32
CAS to WE delay time	^tCWD	40		50		ns	24, 32
RAS pulse width entering SELF REFRESH	^tRASS	100		100		µs	33
RAS precharge time entering SELF REFRESH	^tRPS	110		130		ns	33
CAS hold time entering SELF REFRESH	^tCHD	15		15		ns	33

*S-version only

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than thespecified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW AND $\overline{OE}$ = HIGH.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
23. Timing between the DRAMs and the module did not change with the addition of the line drivers.
24. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
26. A +7ns timing skew from the DRAM to the module resulted from the addition of line drivers.
27. A -2ns (MIN) and a -7ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
28. A +2ns (MIN) and a +7ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
29. The maximum current ratings are based with the memory operating or being refreshed in the x64 mode. The stated maximums may be reduced by one-half when used in the x32 mode.
30. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
31. L-version only.

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NOTES(continued)

32. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If $^t\text{WCS} \geq {}^t\text{WCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^t\text{RWD} \geq {}^t\text{RWD}$ (MIN), $^t\text{AWD} \geq {}^t\text{AWD}$ (MIN) and $^t\text{CWD} \geq {}^t\text{CWD}$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE WRITE ($\overline{\text{OE}}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
33. Refresh must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in the active mode.) Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.
34. Column-address changed once each cycle.
35. The 3ns minimum is a parameter guaranteed by design.

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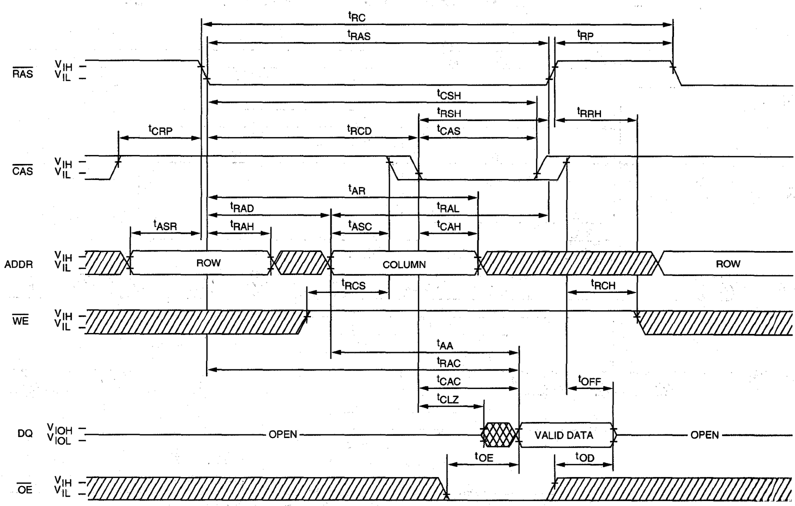
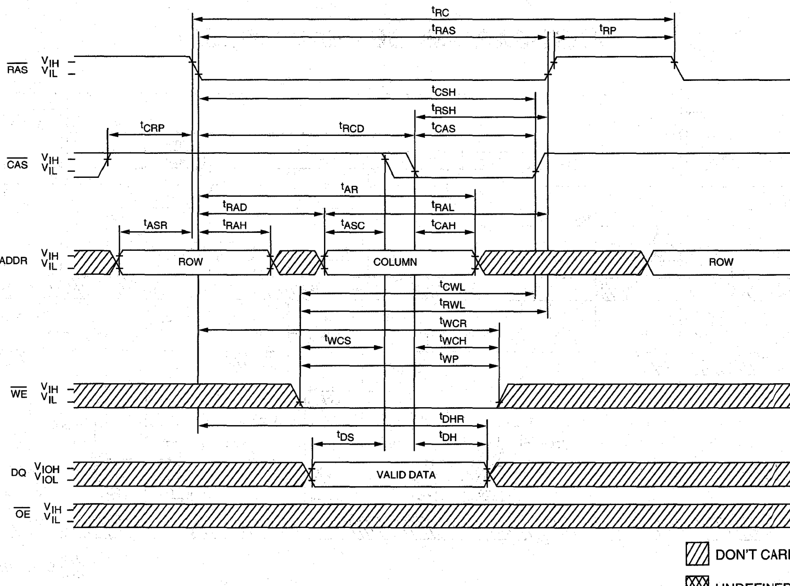
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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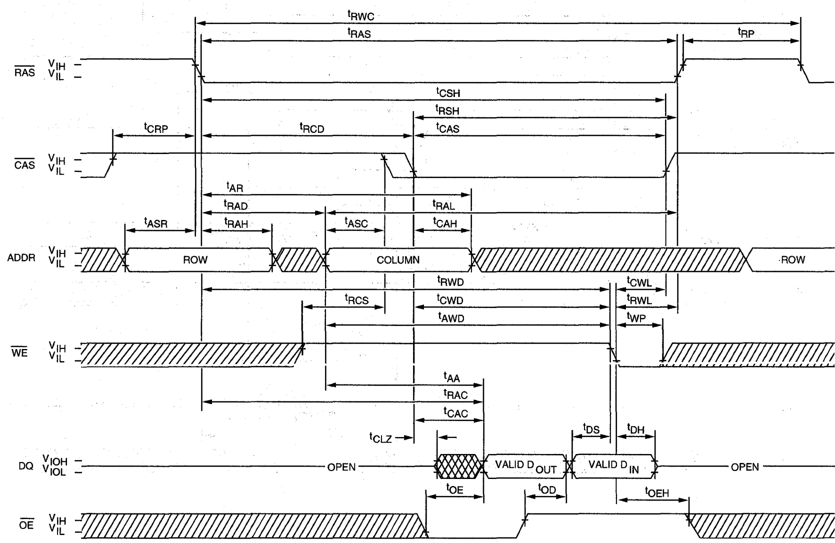
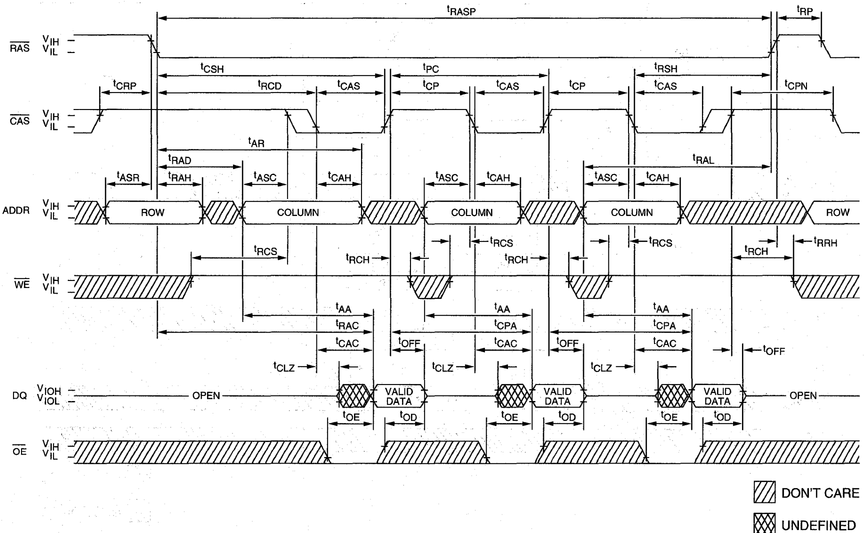
NEW DRAM MODULE

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



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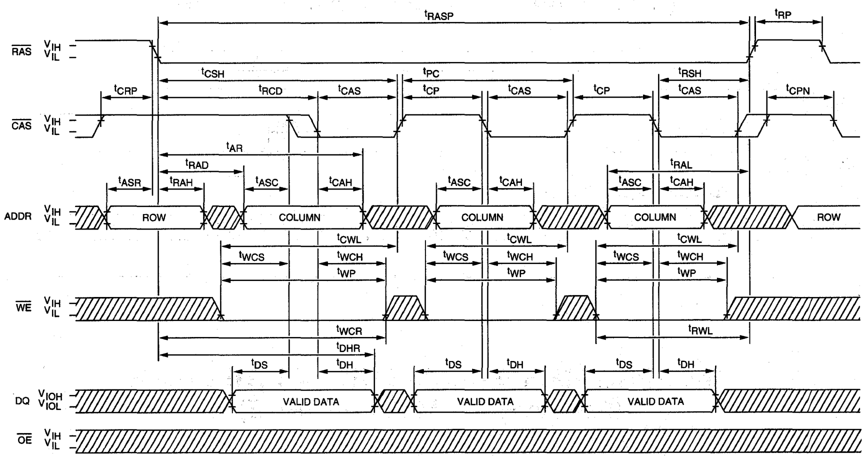
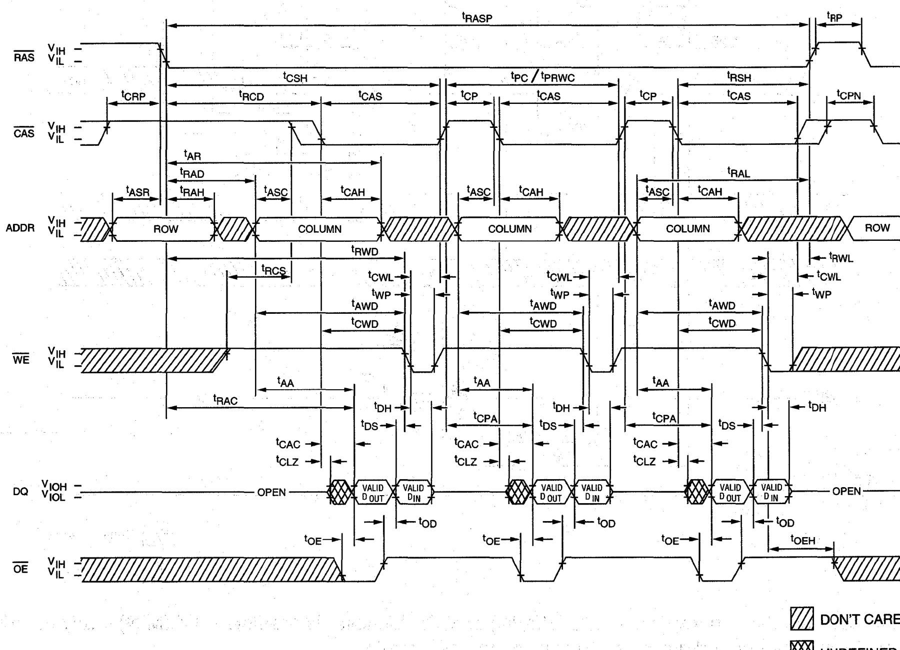
FAST-PAGE-MODE EARLY WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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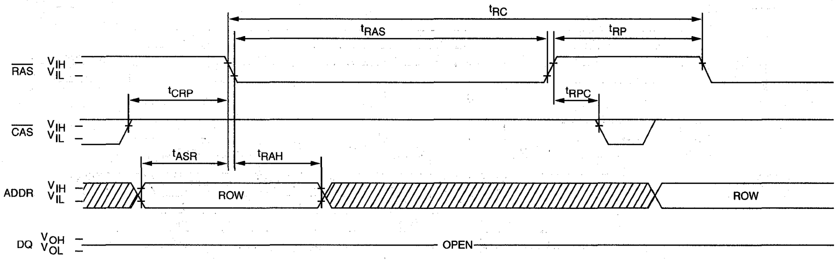
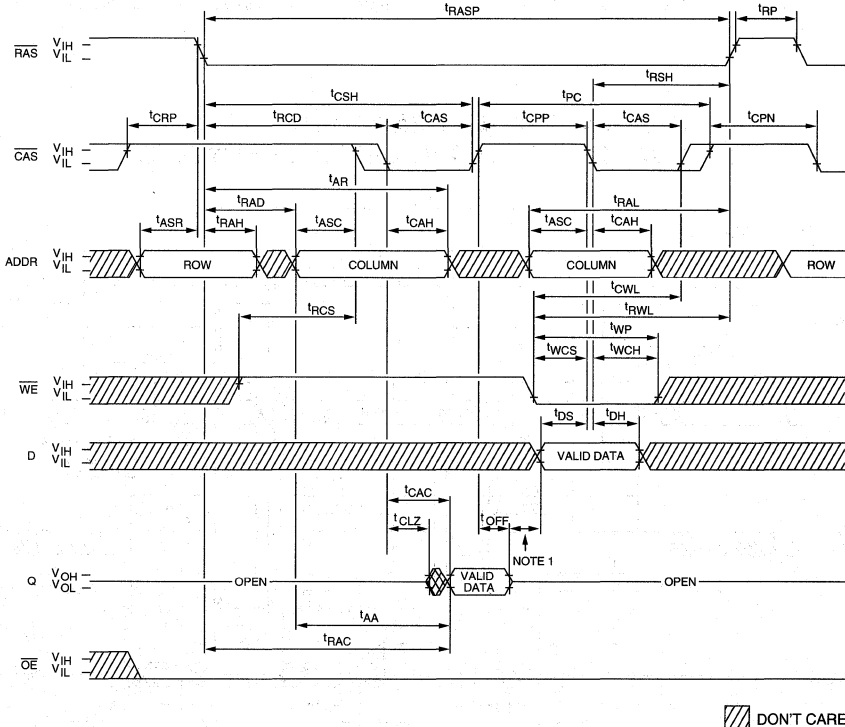
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

(ADDR = A0/B0-A10; $\overline{\text{WE}}$ = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: ^{t}CPP(MIN) or ^{t}CP(whichever is greater) + ^{t}DS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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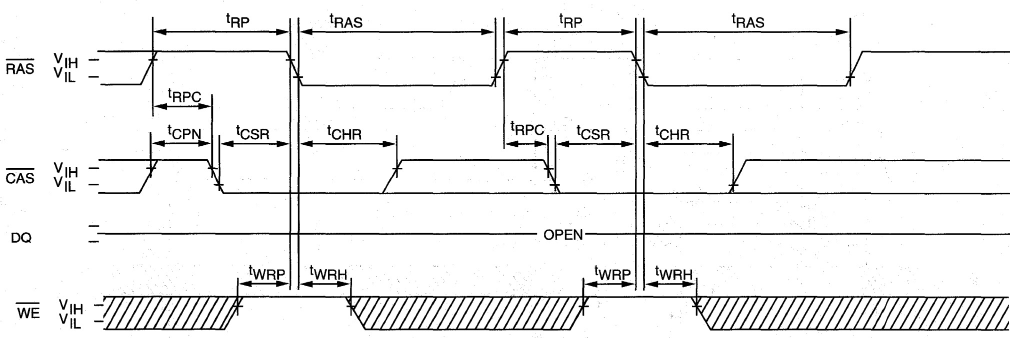
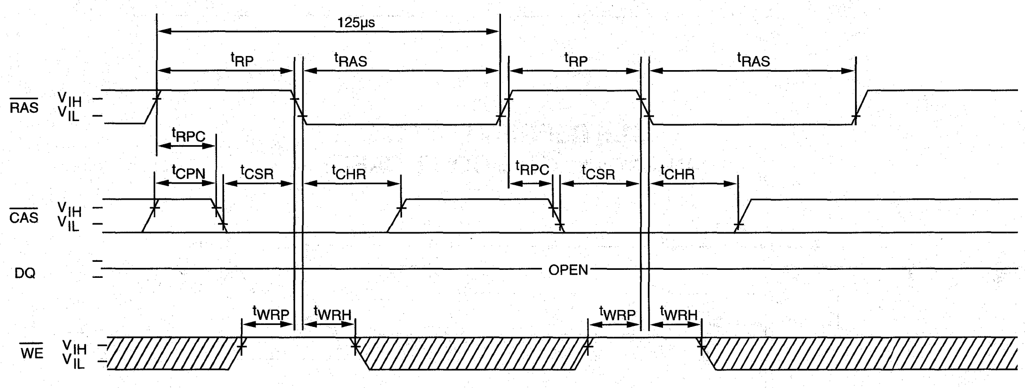
CBR REFRESH CYCLE
(A0/B0-A10, $\overline{OE}$ = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [31]
(A0/B0-A10, $\overline{OE}$ = DON'T CARE)



DON'T CARE

UNDEFINED

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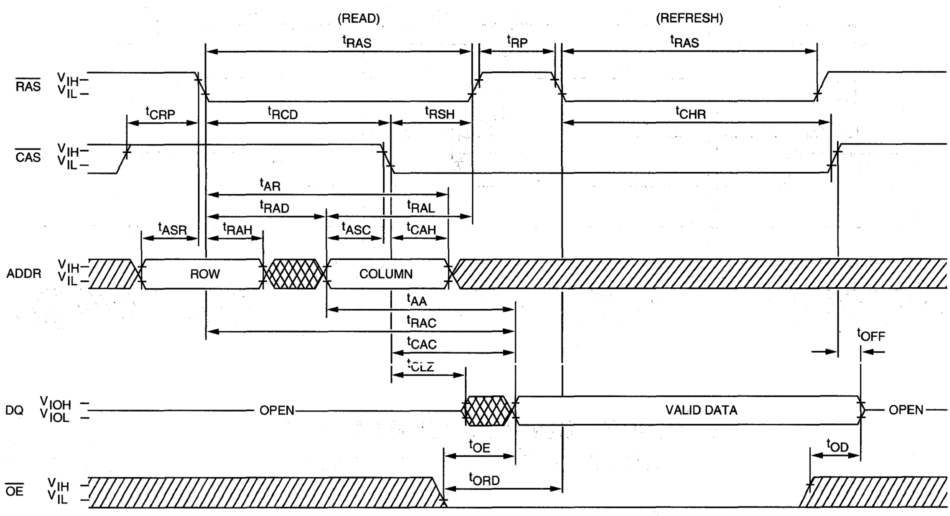
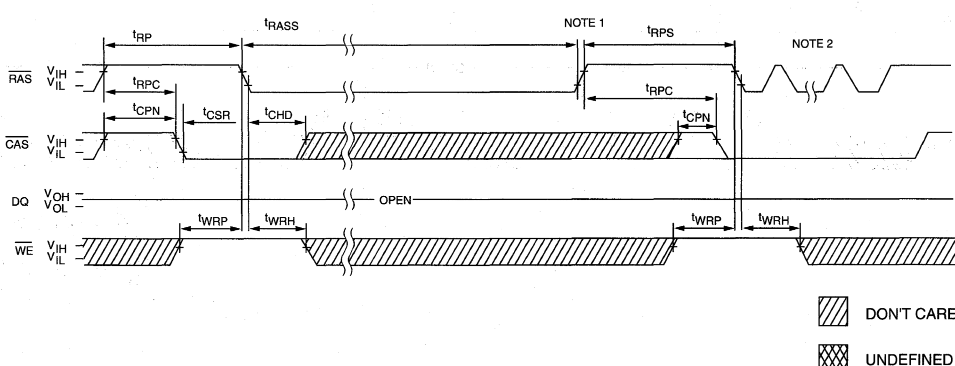
HIDDEN REFRESH CYCLE[21]

(WE = HIGH; OE = LOW)



SELF REFRESH CYCLE

(A0-A11 and OE = DON'T CARE)



NOTE:
1. Once tRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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DRAM MODULE

4 MEG x 72 DRAM

5.0V FAST PAGE MODE

FEATURES

- Industry-standard pinout in a 168-pin, dual read-out, single in-line package
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 56mW standby; 5,000mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- All inputs are buffered except $\overline{RAS}$
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE access cycle

OPTIONS — MARKING

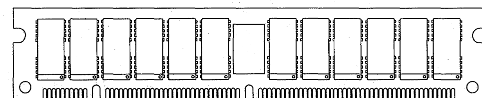
OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Components	
SOJ	D
TSOP	DT
• Packages	
Leadless 168-pin, dual read-out DIMM	M
Leadless 168-pin, dual read-out DIMM (gold)	G

- Part Number Example: MT24DT472M-6

PIN ASSIGNMENT (Top View)

168-Pin, Dual Read-out DIMM

(DE-26) SOJ version
(DE-27) TSOP version



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{OE2}$	86	DQ32	128	RFU
3	DQ1	45	$\overline{RAS2}$	87	DQ33	129	NC
4	DQ2	46	$\overline{CAS4}$	88	DQ34	130	$\overline{CAS5}$
5	DQ3	47	$\overline{CAS6}$	89	DQ35	131	$\overline{CAS7}$
6	Vcc	48	$\overline{WE2}$	90	Vcc	132	$\overline{PDE}$
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	PDQ0	53	DQ17	95	PDQ4	137	DQ49
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	Vcc	101	DQ44	143	Vcc
18	Vcc	60	DQ22	102	Vcc	144	DQ54
19	DQ13	61	RFU	103	DQ45	145	RFU
20	DQ14	62	RFU	104	DQ46	146	RFU
21	DQ15	63	RFU	105	DQ47	147	RFU
22	PDQ1	64	RFU	106	PDQ5	148	RFU
23	Vss	65	DQ23	107	Vss	149	DQ55
24	NC	66	PDQ2	108	NC	150	PDQ6
25	NC	67	DQ25	109	NC	151	DQ56
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{WE0}$	69	DQ25	111	RFU	153	DQ57
28	$\overline{CAS0}$	70	DQ26	112	$\overline{CAS1}$	154	DQ58
29	$\overline{CAS2}$	71	DQ27	113	$\overline{CAS3}$	155	DQ59
30	$\overline{RAS0}$	72	DQ28	11	NC	156	DQ60
31	$\overline{OE0}$	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ29	116	Vss	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	PDQ3	119	A5	161	PDQ7
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

GENERAL DESCRIPTION

The MT24D(T)472 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x72 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0 /B0-A10) at a time. A0 is connected to DQ0-DQ31 and PDQ0-PDQ3, while B0 is connected to DQ32-DQ63 and PDQ4-PDQ7. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

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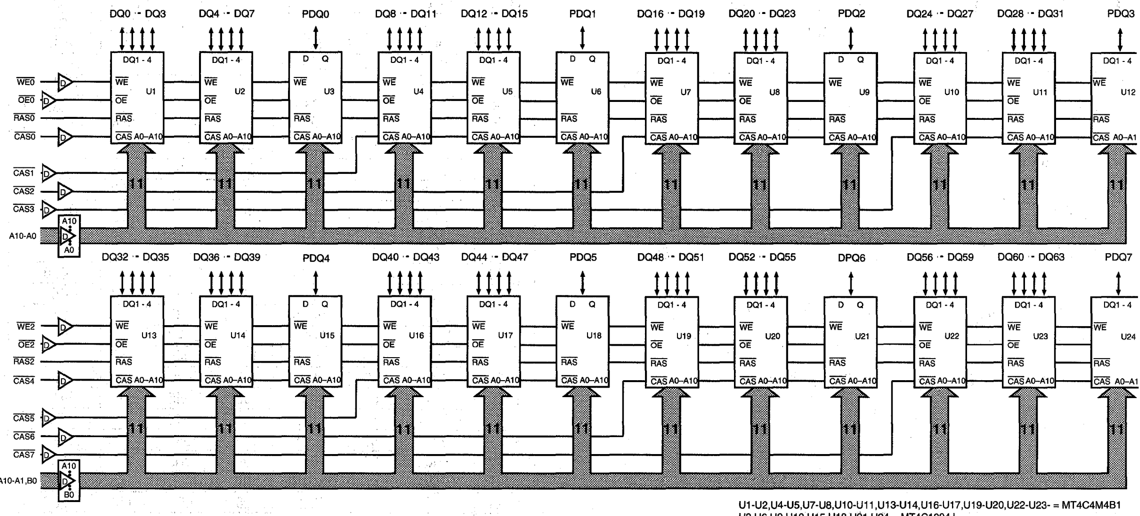
FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

REFRESH

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses (A0/B0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. All inputs with the exception of RAS are redriven.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the ten row-address bits. Two $\overline{RAS}$ inputs allow for one x72 bank or two x36 banks.
28, 29, 46, 47, 112, 113, 130, 131	$\overline{CAS0-7}$	Buffered Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the ten column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
27, 48	$\overline{WE0}$, $\overline{WE2}$	Buffered Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. $\overline{WE0}$ controls DQ0-DQ31 and PDQ0-PDQ3. $\overline{WE2}$ controls DQ32-DQ63 and PDQ4-PDQ7. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	$\overline{OE0}$, $\overline{OE2}$	Buffered Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE0}$ controls DQ0-DQ31 and PDQ0-PDQ3. $\overline{OE2}$ controls DQ32-DQ63 and PDQ4-PDQ7. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121, 126	A0-A10, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
11, 22, 66, 77, 95 106, 150, 161	PDQ0-PDQ7	Input/ Output	Parity Data I/O: Additional storage location provided per byte (as controlled by $\overline{CAS0-7}$) for parity purposes.
2-5, 7-10, 13-17, 19-21, 52-53, 55-58, 60, 65, 67, 69-72, 74-76, 86-89, 91-94, 97-101, 103-105, 136-137, 139-142, 144, 149,151,153-156,158-160	DQ0-DQ63	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x72 mode only). For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	-	Presence-Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
41-42, 61-64, 111, 115, 125, 128, 145-148	RFU	-	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133,143, 157, 168	Vcc	Supply	Power Supply: +5V ± 10%

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PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	Vss	Supply	Ground
83, 167	ID0, ID1	-	ID bit
132	$\overline{PDE}$	-	PD enable
11, 22, 24-25, 38-39, 50-51, 66, 77, 95, 106, 108-109, 114, 122-123, 129, 134-135, 150, 161	NC	-	No connect.

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ᵗR	ADDRESSES ᵗC	DATA-IN/OUT DQ0-63, PDQ0-7	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY WRITE		L	L	L	X	ROW	COL	Data-In	
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	
$\overline{RAS}$ ONLY REFRESH		H	X	X	X	ROW	n/a	High-Z	
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	
CBR REFRESH		H→L	L	H	X	X	X	High-Z	

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			NC	NC	NC	NC	NC			
2MB 4MB	256K x 64/72 512K x 64/72	9/9 9/9			Vss NC	Vss Vss	Vss Vss	Vss Vss	Vss Vss			
4MB 8MB	512K x 64/72/80 1 Meg x 64/72/80	10/9 10/9			Vss NC	NC NC	Vss Vss	Vss Vss	Vss Vss			
8MB 16MB	1 Meg x 64/72/80 2 Meg x 64/72/80	10/10 10/10			Vss NC	Vss Vss	NC NC	Vss Vss	Vss Vss			
16MB	2 Meg x 64/72/80	11/10			NC	Vss	Vss	NC	Vss			
• 32MB	4 Meg x 64/72/80	11/10			Vss	NC	Vss	NC	Vss			
32MB 64MB	4 Meg x 64/72/80 8 Meg x 64/72/80	12/10 12/10			NC Vss	NC Vss	Vss NC	NC Vss	Vss Vss			
Access Timing		80ns								NC	Vss	
		70ns								Vss	NC	
		60ns								NC	NC	
		50ns								Vss	Vss	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, No Parity	Vss									NC
		x72, Parity	NC									NC
		x72, ECC	Vss									Vss
		x80, ECC	NC									Vss

NOTE: Vss = ground.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	3.5	V_{CC}+0.5	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-0.5	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS7}$ A0-A10, B0 $\overline{WE0}$,2,$\overline{OE0}$,2	I_{I1}	-2	2	µA	
	$\overline{RAS0}$, 2	I_{I2}	-24	24	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ0-DQ63, PDQ0-PDQ7	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	32MB	48	48	mA	29
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	32MB	24	24	mA	29
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	32MB	2,800	2,560	mA	3, 4, 29, 34
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	32MB	2,080	1,840	mA	3, 4, 29, 34
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	32MB	2,800	2,560	mA	3, 29 34
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	32MB	2,800	2,560	mA	3, 5, 29

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 24W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, B0	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$	C_{I2}		9	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		40	pF	2
Input Capacitance: $\overline{CAS0}$ - $\overline{CAS7}$	C_{I4}		9	pF	2
Input/Output Capacitance: DQ0-DQ63, PDQ0-PDQ7	C_{IO}		15	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		ns	23
Access time from $\overline{RAS}$	tRAC	60		70		ns	14, 23
Access time from $\overline{CAS}$	tCAC		22		27	ns	15, 26
Access time from column-address	tAA		37		42	ns	26
Access time from $\overline{CAS}$ precharge	tCPA		42		47	ns	26
$\overline{RAS}$ pulse width	tRAS	60	100,000	70	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	ns	23
$\overline{RAS}$ hold time	tRSH	22		27		ns	26
$\overline{RAS}$ precharge time	tRP	40		50		ns	23
$\overline{CAS}$ pulse width	tCAS	15	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	tCSH	58		68		ns	25
$\overline{CAS}$ precharge time	tCPN	10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	tCP	10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	18	38	18	43	ns	17, 27
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	12		12		ns	26
Row-address setup time	tASR	7		7		ns	26
Row-address hold time	tRAH	8		8		ns	25
$\overline{RAS}$ to column-address delay time	tRAD	13	23	13	28	ns	18, 27
Column-address setup time	tASC	2		2		ns	24
Column-address hold time	tCAH	10		15		ns	23

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Column-address hold time (referenced to RAS)	tAR	48		53		ns	25
Column-address to RAS lead time	tRAL	37		42		ns	26
Read command setup time	tRCS	2		2		ns	24
Read command hold time (referenced to CAS)	tRCH	2		2		ns	19, 24
Read command hold time (referenced to RAS)	tRRH	0		0		ns	19, 23
CAS to output in Low-Z	tCLZ	2		2		ns	24
Output buffer turn-off delay	tOFF	5	22	5	27	ns	20, 28
WE command setup time	tWCS	2		2		ns	24
Write command hold time	tWCH	10		15		ns	23
Write command hold time (referenced to RAS)	tWCR	43		53		ns	25
Write command pulse width	tWP	10		15		ns	23
Write command to RAS lead time	tRWL	22		27		ns	26
Write command to CAS lead time	tCWL	15		20		ns	23
Data-in setup time	tDS	2		2		ns	24, 30
Data-in hold time	tDH	17		22		ns	26, 30
Data-in hold time (referenced to RAS)	tDHR	45		55		ns	23
Transition time (rise or fall)	tT	3	50	3	50	ns	9, 10, 23
Refresh period (2,048 cycles)	tREF		32		32	ms	
RAS to CAS precharge time	tRPC	0		0		ns	23
CAS setup time (CBR REFRESH)	tCSR	7		7		ns	5, 24
CAS hold time (CBR REFRESH)	tCHR	13		13		ns	5, 25
WE hold time (CBR REFRESH)	tWRH	8		8		ns	22, 25
WE setup time (CBR REFRESH)	tWRP	12		12		ns	22, 24
WE hold time (WCBR test cycle)	tWTH	8		8		ns	22, 25
WE setup time	tWTS	12		12		ns	22, 24
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		ns	20
Output disable	tOD		15		20	ns	23
Output enable	tOE	15		20		ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		15		ns	25
RAS to WE delay time	tRWD	85		95		ns	24, 32
Column-address to WE delay time	tAWD	55		60		ns	24, 32
CAS to WE delay time	tCWD	40		45		ns	24, 32

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 5V ±10%; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
22. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^tWRP and ^tWRH in the CBR REFRESH cycle.
23. Timing between the DRAMs and the module did not change with the addition of the line drivers.
24. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
26. A +7ns timing skew from the DRAM to the module resulted from the addition of line drivers.
27. A -2ns (MIN) and a -7ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
28. A +2ns (MIN) and a +7ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
29. The maximum current ratings are based with the memory operating or being refreshed in the x72 mode. The stated maximums may be reduced by approximately one-half when used in the x36 mode.
30. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
31. L-version only.
32. ^tWCS, ^tRWD, ^tAWD and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY WRITE cycles. ^tRWD, ^tAWD and ^tCWD apply to READ-MODIFY-WRITE cycles. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE WRITE cycle.
33. Refresh current increases if ^tRAS is extended beyond its minimum specification.
34. Column-address changed once each cycle.

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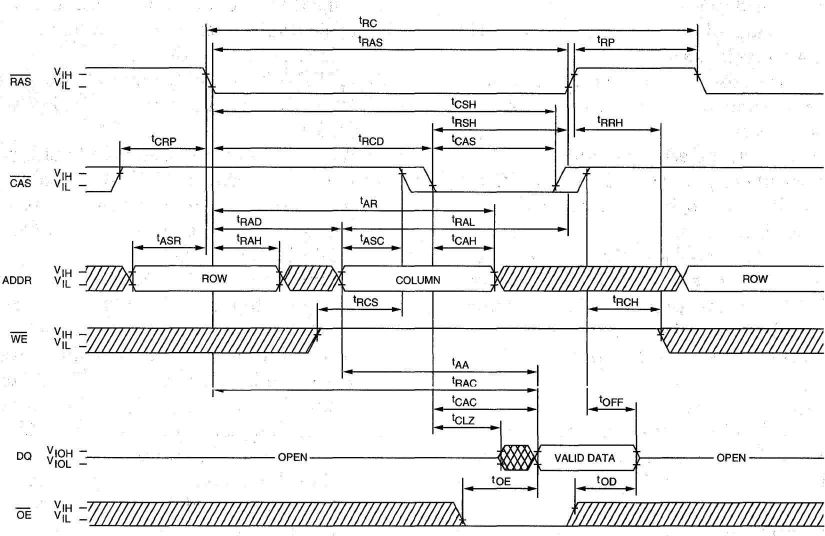
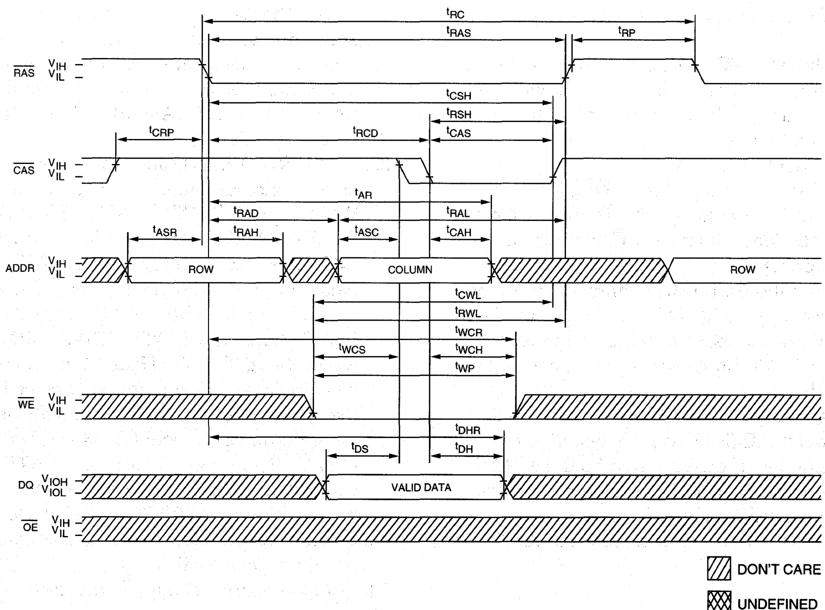
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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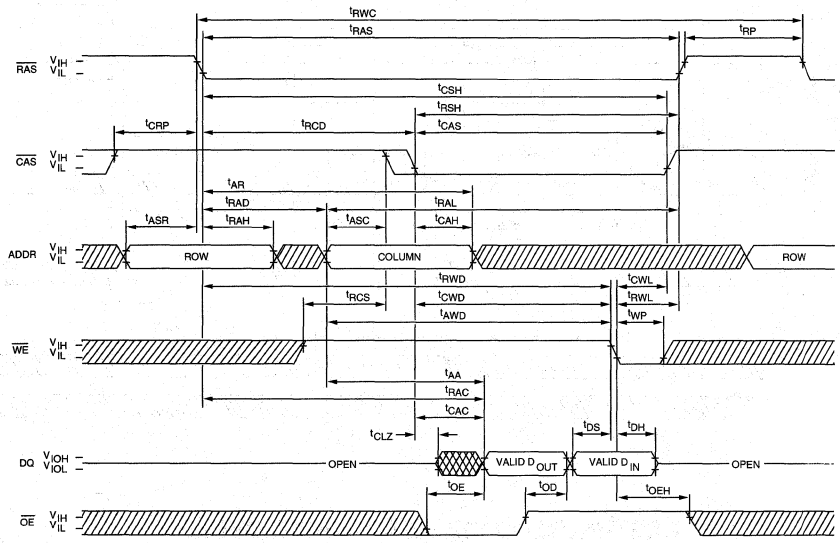
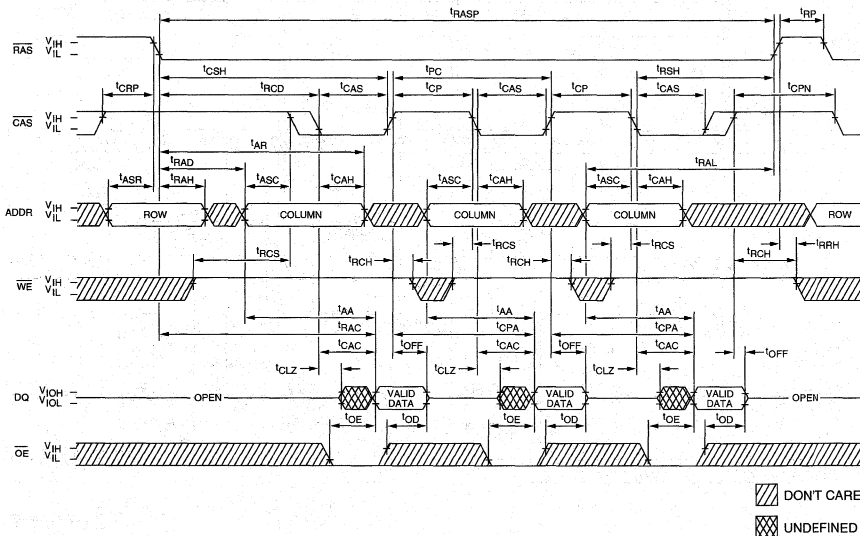
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



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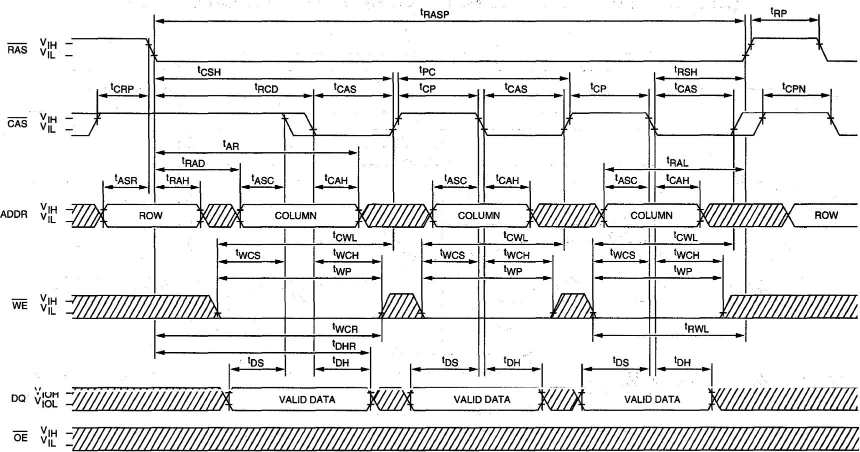
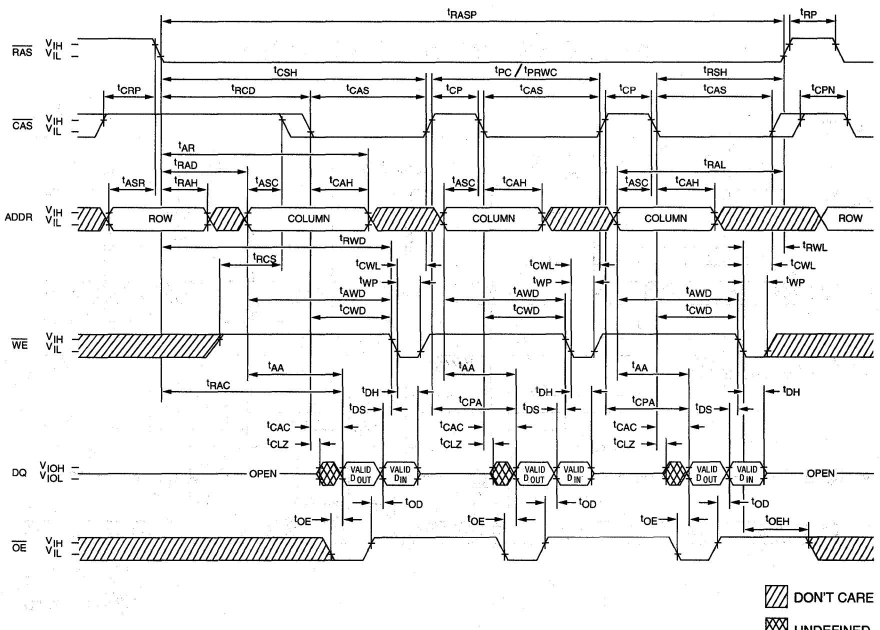
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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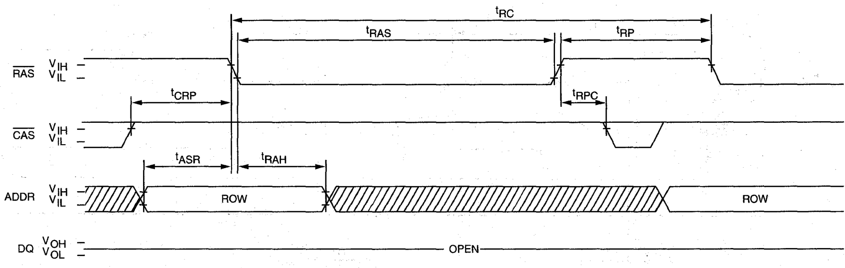
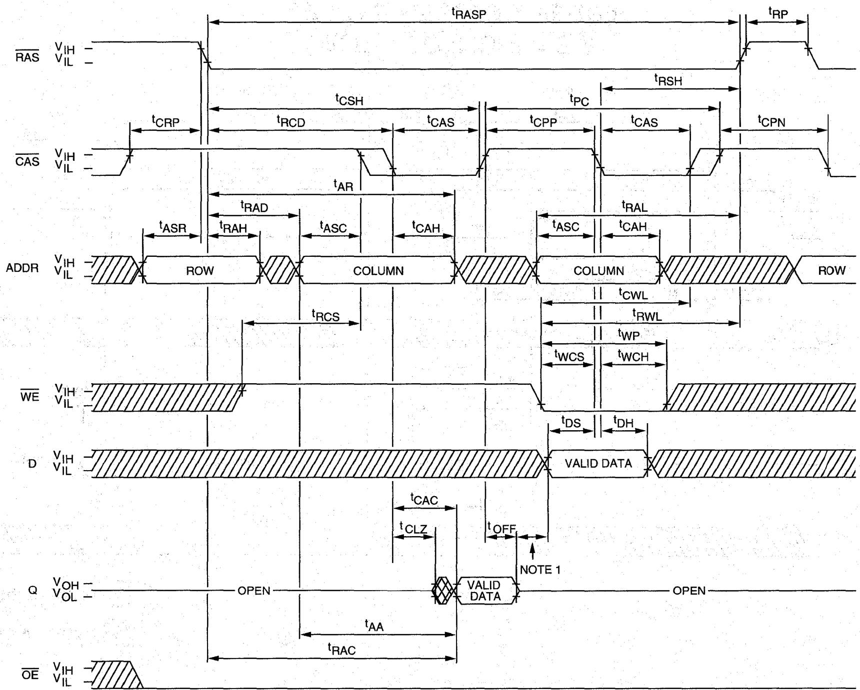
RAS ONLY REFRESH CYCLE
(ADDR = A0/B0-A10; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE:
1. Do not drive data prior to tristate: ${}^tCPP(MIN)$ or ${}^tCP$(whichever is greater) + ${}^tDS(MIN)$ + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

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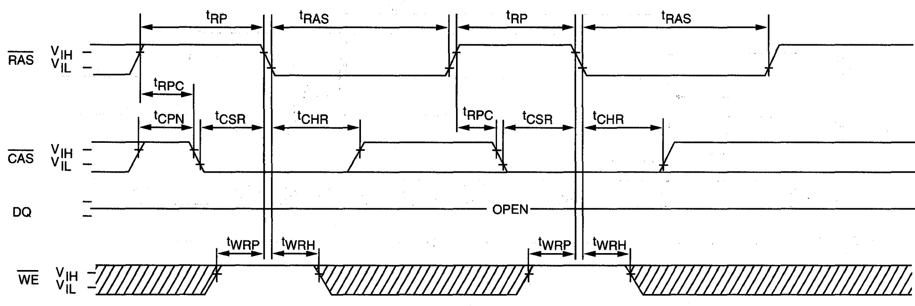
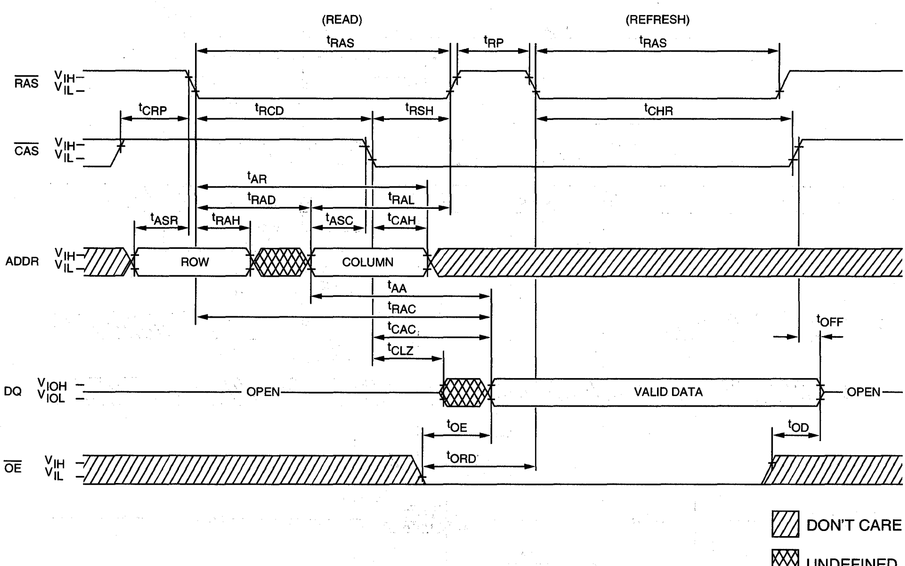
CBR REFRESH CYCLE
(A0/B0-A10, OE = DON'T CARE)



HIDDEN REFRESH CYCLE[21]
(WE = HIGH; OE = LOW)



DON'T CARE

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DRAM MODULE

4 MEG x 72 DRAM

3.3V FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- Industry-standard pinout in a 168-pin, dual read-out, single in-line package
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 56mW standby; 3,400mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and SELF
- All inputs are buffered except $\overline{RAS}$
- 2,048-cycle refresh distributed across 32ms or 2,048-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Optional SELF REFRESH mode

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Components	
SOJ	D
TSOP	DT
• Packages	
Leadless 168-pin, dual read-out DIMM	M
Leadless 168-pin, dual read-out DIMM (gold)	G
• Refresh	
Standard	Blank
Low-power extended SELF REFRESH	S

- Part Number Example: MT24LDT472G-6 S

GENERAL DESCRIPTION

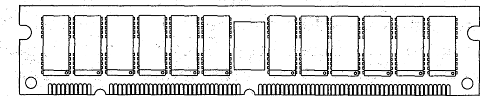
The MT24LD(T)472(S) is a randomly accessed solid-state memory containing 4,194,304 words organized in a x72 configuration. It is specially processed to operate from 3.0V to 3.6V for low-voltage memory systems. The module has optional FAST PAGE MODE, which allows faster data operations (READ or WRITE) within a row-address-defined (A0/B0-A10) page boundary. A0 is connected to DQ0-DQ31 and PDQ0-PDQ3 while B0 is connected to DQ32-DQ63 and PDQ4-PDQ7.

During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0 /B0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits.

PIN ASSIGNMENT (Top View)

168-Pin, Dual Read-out DIMM

(DE-28) SOJ version
(DE-29) TSOP version



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{OE2}$	86	DQ32	128	RFU
3	DQ1	45	$\overline{RAS2}$	87	DQ33	129	NC
4	DQ2	46	$\overline{CAS4}$	88	DQ34	130	$\overline{CAS5}$
5	DQ3	47	$\overline{CAS6}$	89	DQ35	131	$\overline{CAS7}$
6	Vcc	48	$\overline{WE2}$	90	Vcc	132	$\overline{PDE}$
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	PDQ0	53	DQ17	95	PDQ4	137	DQ49
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	Vcc	101	DQ44	143	Vcc
18	Vcc	60	DQ22	102	Vcc	144	DQ54
19	DQ13	61	RFU	103	DQ45	145	RFU
20	DQ14	62	RFU	104	DQ46	146	RFU
21	DQ15	63	RFU	105	DQ47	147	RFU
22	PDQ1	64	RFU	106	PDQ5	148	RFU
23	Vss	65	DQ23	107	Vss	149	DQ55
24	NC	66	PDQ2	108	NC	150	PDQ6
25	NC	67	DQ25	109	NC	151	DQ56
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{WE0}$	69	DQ25	111	RFU	153	DQ57
28	$\overline{CAS0}$	70	DQ26	112	$\overline{CAS1}$	154	DQ58
29	$\overline{CAS2}$	71	DQ27	113	$\overline{CAS3}$	155	DQ59
30	$\overline{RAS0}$	72	DQ28	11	NC	156	DQ60
31	$\overline{OE0}$	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ29	116	Vss	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	PDQ3	119	A5	161	PDQ7
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

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READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, and the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses (A0/B0-A10) are executed at least every 32ms (128ms "S" option), regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

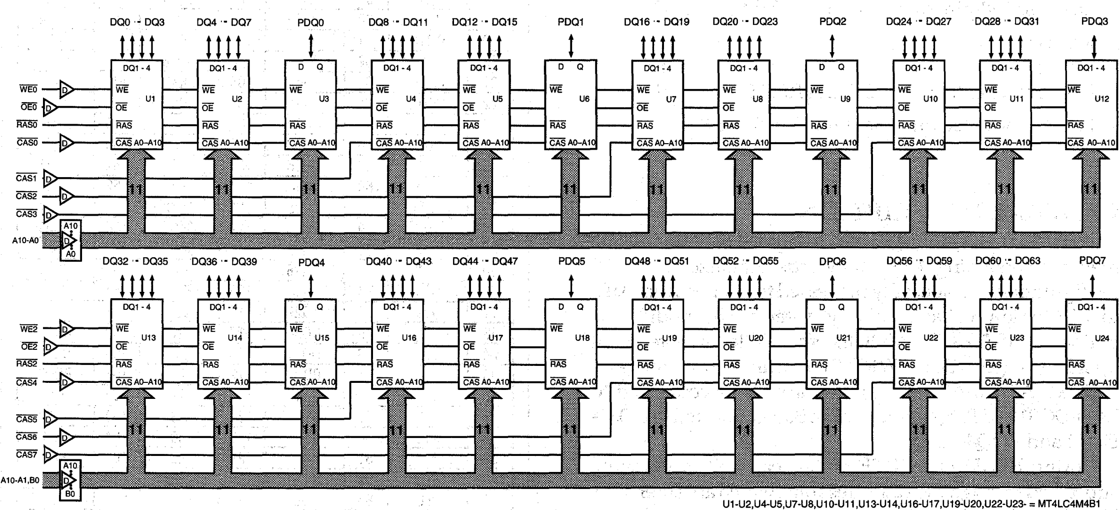
An optional SELF REFRESH mode is also available. The "S" option allows the user the option of a fully static, low-power, data-retention mode, or a dynamic refresh mode at the extended refresh period of 128ms, four times longer than the standard 32ms specifications. The module's SELF REFRESH mode is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified ^tRASS. Additionally, the "S" option allows for extended refresh rate of 62.5µs per row if using distributed CBR refresh. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum of ^tRPS ($\approx {}^tRCns$). This delay allows for the completion of any internal refresh cycles that may be in process at the time of RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 2,048 rows must be refreshed within 300µs, prior to the resumption of normal operation.

STANDBY

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. All inputs with the exception of RAS are redriven.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	RAS0, RAS2	Input	Row-Address Strobe: RAS is used to clock-in the ten row-address bits. Two RAS inputs allow for one x72 bank or two x36 banks.
28, 29, 46, 47, 112, 113, 130, 131	CAS0-7	Buffered Input	Column-Address Strobe: CAS is used to clock-in the ten column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight CAS inputs allow byte access control for any memory bank configuration.
27, 48	WE0, WE2	Buffered Input	Write Enable: WE is the READ/WRITE control for the DQ pins. WE0 controls DQ0-DQ31 and PDQ0-PDQ3. WE2 controls DQ32-DQ63 and PDQ4-PDQ7. If WE is LOW prior to CAS going LOW, the access is an EARLY WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle, provided OE is also LOW. If WE goes LOW after CAS goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	OE0, OE2	Buffered Input	Output Enable: OE is the input/output control for the DQ pins. OE0 controls DQ0-DQ31 and PDQ0-PDQ3. OE2 controls DQ32-DQ63 PDQ4-PDQ7. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121, 126	A0-A10, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.
11, 22, 66, 77, 95 106, 150, 161	PDQ0-PDQ7	Input/ Output	Parity Data I/O: Additional storage location provided per byte (as controlled by CAS0-7) for parity purposes.
2-5, 7-10, 13-17, 19-21, 52-53, 55-58, 60, 65, 67, 69-72, 74-76, 86-89, 91-94, 97-101, 103-105, 136-137, 139-142, 144, 149,151,153-156,158-160	DQ0-DQ63	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS select (x72 mode only). For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	-	Presence-Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
41-42, 61-64, 111, 115, 125, 128, 145-148	RFU	-	RFU: These pins should be left unconnected (reserved for future use).

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PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	Vcc	Supply	Power Supply: +3.3V ± 0.3V
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	Vss	Supply	Ground
83, 167	ID0, ID1	-	ID bit
132	$\overline{PDE}$	-	PD enable
11, 22, 24-25, 38-39, 50-51, 66, 77, 95, 106, 108-109, 114, 122-123, 129, 134-135, 150, 161	NC	-	No connect.

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DATA-IN/OUT	NOTES
						tR	tC	DQ0-63, PDQ0-7	
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY WRITE		L	L	L	X	ROW	COL	Data-In	
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	
$\overline{RAS}$ ONLY REFRESH		H	X	X	X	ROW	n/a	High-Z	
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	
CBR REFRESH		H→L	L	H	X	X	X	High-Z	

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			NC	NC	NC	NC	NC			
2MB	256K x 64/72	9/9			Vss	Vss	Vss	Vss	Vss			
4MB	512K x 64/72	9/9			NC	Vss	Vss	Vss	Vss			
4MB	512K x 64/72/80	10/9			Vss	NC	Vss	Vss	Vss			
8MB	1 Meg x 64/72/80	10/9			NC	NC	Vss	Vss	Vss			
8MB	1 Meg x 64/72/80	10/10			Vss	Vss	NC	Vss	Vss			
16MB	2 Meg x 64/72/80	10/10			NC	Vss	NC	Vss	Vss			
16MB	2 Meg x 64/72/80	11/10			NC	Vss	Vss	NC	Vss			
• 32MB	4 Meg x 64/72/80	11/10			Vss	NC	Vss	NC	Vss			
32MB	4 Meg x 64/72/80	12/10			NC	NC	Vss	NC	Vss			
64MB	8 Meg x 64/72/80	12/10			Vss	Vss	NC	Vss	Vss			
Access Timing		80ns								NC	Vss	
		70ns								Vss	NC	
		60ns								NC	NC	
		50ns								Vss	Vss	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, No Parity	Vss									NC
		x72, Parity	NC									NC
		x72, ECC	Vss									Vss
		x80, ECC	NC									Vss

NOTE: Vss = ground.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = 3.3V ± 0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.1	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 3.6V (All other pins not under test = 0V) for each package input	CAS0-CAS7 A1-A9, A0, B0 WE0,2,OE0,2	I_{I1} I_{I2} I_{I3}	-2	2	µA	
	RAS0,2		-24	24	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 3.6V) for each package input	DQ0-DQ63, PDQ0-PDQ7	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION		SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = V_{IH})		I_{CC1}	32MB	24	24	mA	29
STANDBY CURRENT: (CMOS)	STD	I_{CC2}	32MB	12	12	mA	29
(RAS = CAS = V_{CC} -0.2V)	S	I_{CC2}	32MB	3.6	3.6	mA	29
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC3}	32MB	2,800	2,560	mA	3, 4, 29, 34
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V_{IL}, CAS, Address Cycling: ^tPC = ^tPC [MIN])		I_{CC4}	32MB	2,080	1,840	mA	3, 4, 29, 34
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = V_{IH}: ^tRC = ^tRC [MIN])		I_{CC5}	32MB	2,800	2,560	mA	3, 29, 34
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC6}	32MB	2,800	2,560	mA	3, 5, 29
REFRESH CURRENT: Extended (S-only) Average power supply current, CAS = 0.2V or CBR cycling; RAS = ^tRAS (MIN); WE = Vcc -0.2V; A0/B0-A10 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 62.5µs (2,048 rows at 62.5µs = 128ms)		I_{CC7}	32MB	7.2	7.2	mA	3, 5 29, 31 33
REFRESH CURRENT: SELF (S-only) Average power supply current during SELF REFRESH: CBR cycle with RAS ≥ ^tRASS (MIN) and CAS held LOW; WE = Vcc -0.2V; A0/B0-A10 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open)		I_{CC8}	32MB	7.2	7.2	mA	5, 29, 31

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +4.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 24W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, B0	C_{I1}		9	pF	2
Input Capacitance: WE0, WE2, OE0, OE2	C_{I2}		9	pF	2
Input Capacitance: RAS0, RAS2	C_{I3}		40	pF	2
Input Capacitance: CAS0 - CAS7	C_{I4}		9	pF	2
Input/Output Capacitance: DQ0-DQ63, PDQ0-PDQ7	C_{IO}		15	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		ns	23
Access time from RAS	tRAC	60		70		ns	14, 23
Access time from CAS	tCAC		22		27	ns	15, 26
Access time from column-address	tAA		37		42	ns	26
Access time from CAS precharge	tCPA		42		47	ns	26
RAS pulse width	tRAS	60	100,000	70	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	ns	23
RAS hold time	tRSH	22		27		ns	26
RAS precharge time	tRP	40		50		ns	23
CAS pulse width	tCAS	15	100,000	20	100,000	ns	23
CAS hold time	tCSH	58		68		ns	25
CAS precharge time	tCPN	10		10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	tCP	10		10		ns	23
RAS to CAS delay time	tRCD	18	38	18	43	ns	17, 27
CAS to RAS precharge time	tCRP	12		12		ns	26
Row-address setup time	tASR	7		7		ns	26
Row-address hold time	tRAH	8		8		ns	25
RAS to column-address delay time	tRAD	13	23	13	28	ns	18, 27
Column-address setup time	tASC	2		2		ns	24
Column-address hold time	tCAH	10		15		ns	23

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Column-address hold time (referenced to RAS)	tAR	48		53		ns	25
Column-address to RAS lead time	tRAL	37		42		ns	26
Read command setup time	tRCS	2		2		ns	24
Read command hold time (referenced to CAS)	tRCH	2		2		ns	19, 24
Read command hold time (referenced to RAS)	tRRH	0		0		ns	19, 23
CAS to output in Low-Z	tCLZ	2		2		ns	24
Output buffer turn-off delay	tOFF	5	22	5	27	ns	20, 28
WE command setup time	tWCS	2		2		ns	24
Write command hold time	tWCH	10		15		ns	23
Write command hold time (referenced to RAS)	tWCR	43		53		ns	25
Write command pulse width	tWP	10		15		ns	23
Write command to RAS lead time	tRWL	22		27		ns	26
Write command to CAS lead time	tCWL	15		20		ns	23
Data-in setup time	tDS	2		2		ns	24, 30
Data-in hold time	tDH	17		22		ns	26, 30
Data-in hold time (referenced to RAS)	tDHR	45		55		ns	23
Transition time (rise or fall)	tT	3	50	3	50	ns	9, 10, 23
Refresh period (2,048 cycles)	tREF		32/128*		32/128*	ms	
RAS to CAS precharge time	tRPC	0		0		ns	23
CAS setup time (CBR REFRESH)	tCSR	7		7		ns	5, 24
CAS hold time (CBR REFRESH)	tCHR	13		13		ns	5, 25
WE hold time (CBR REFRESH)	tWRH	8		8		ns	22, 25
WE setup time (CBR REFRESH)	tWRP	12		12		ns	22, 24
WE hold time (WCBR test cycle)	tWTH	8		8		ns	22, 25
WE setup time	tWTS	12		12		ns	22, 24
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		ns	20
Output disable	tOD		15		20	ns	23
Output enable	tOE	15		20		ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		15		ns	25
RAS to WE delay time	tRWD	85		95		ns	24, 32
Column-address to WE delay time	tAWD	55		60		ns	24, 32
CAS to WE delay time	tCWD	40		45		ns	24, 32

*S-version only.

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 3.3V ±0.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OH} = 2.0V and V_{OL} = 0.8V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
23. Timing between the DRAMs and the module did not change with the addition of the line drivers.
24. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
26. A +7ns timing skew from the DRAM to the module resulted from the addition of line drivers.
27. A -2ns (MIN) and a -7ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
28. A +2ns (MIN) and a +7ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
29. The maximum current ratings are based with the memory operating or being refreshed in the x72 mode. The stated maximums may be reduced by approximately one-half when used in the x36 mode.
30. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
31. S-version only.
32. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
33. Refresh current increases if ^{t}RAS is extended beyond its minimum specification.
34. Column-address changed once each cycle.

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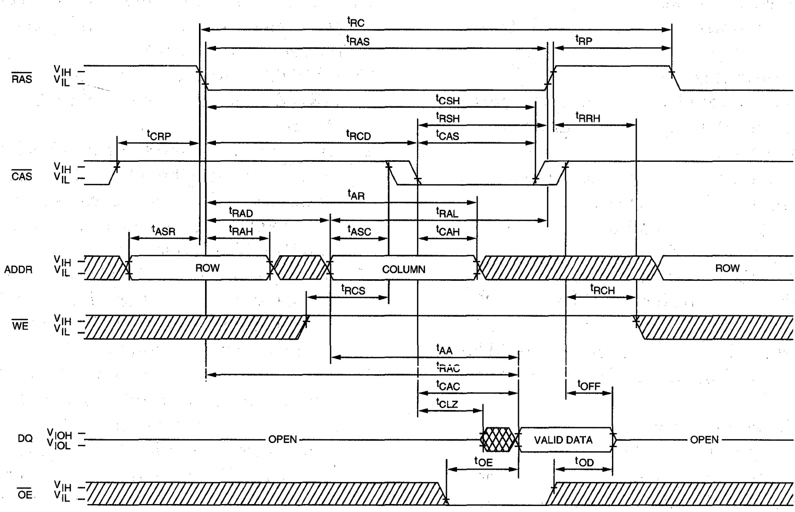
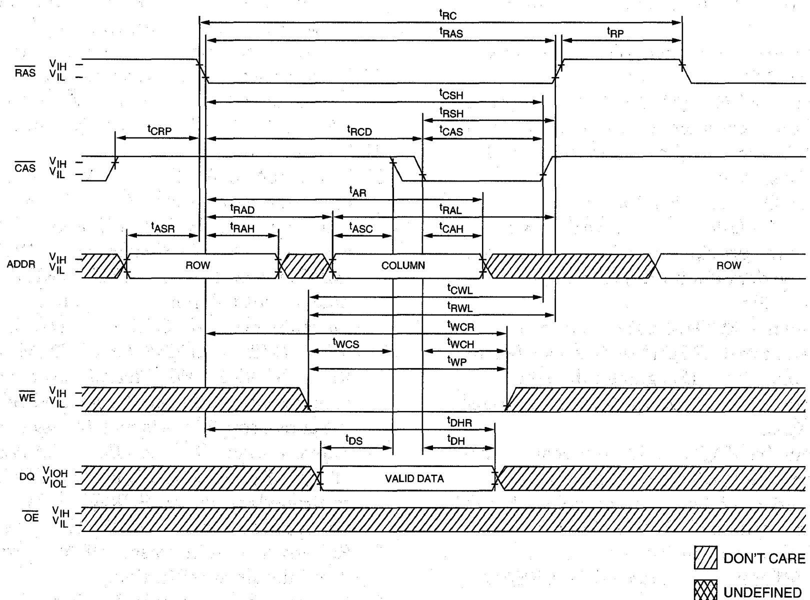
NEW DRAM MODULE

READ CYCLE



EARLY WRITE CYCLE



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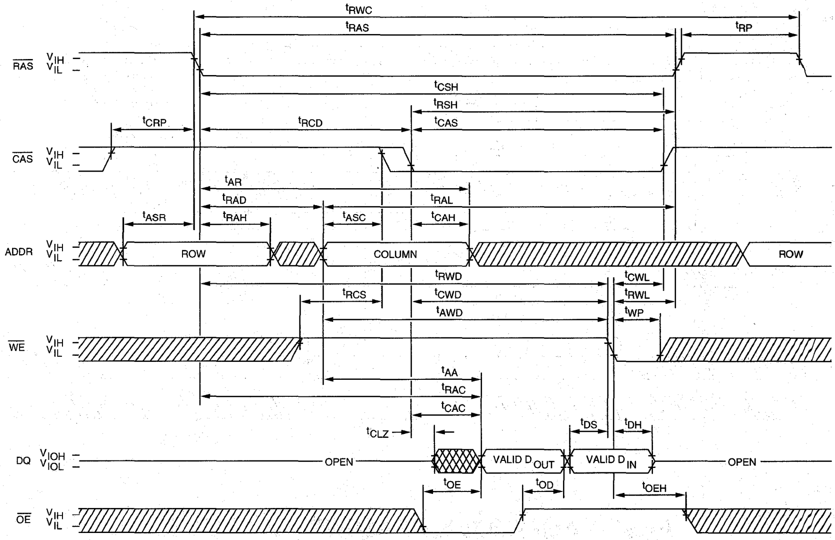
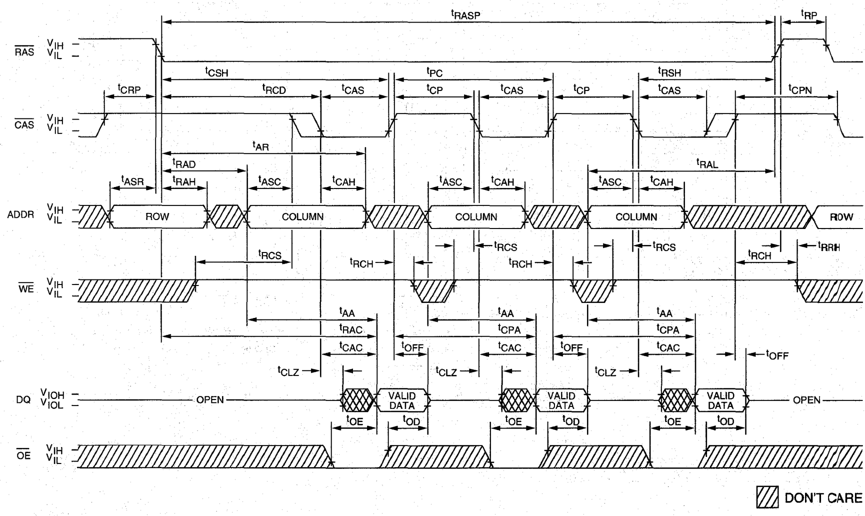
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

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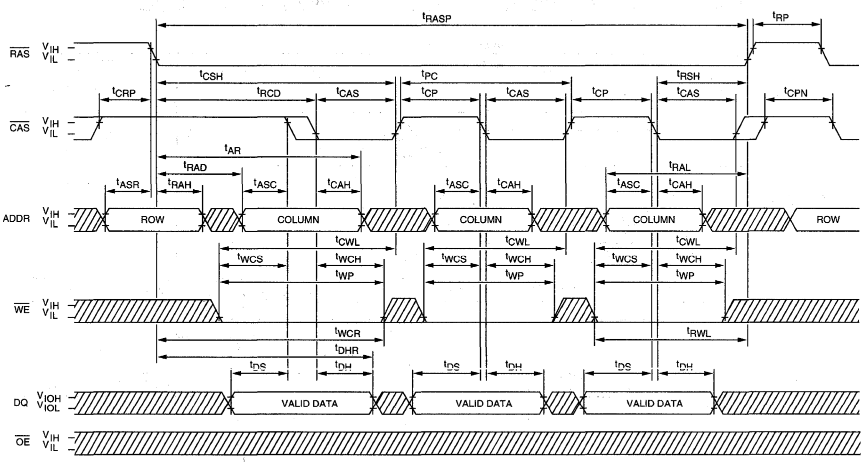
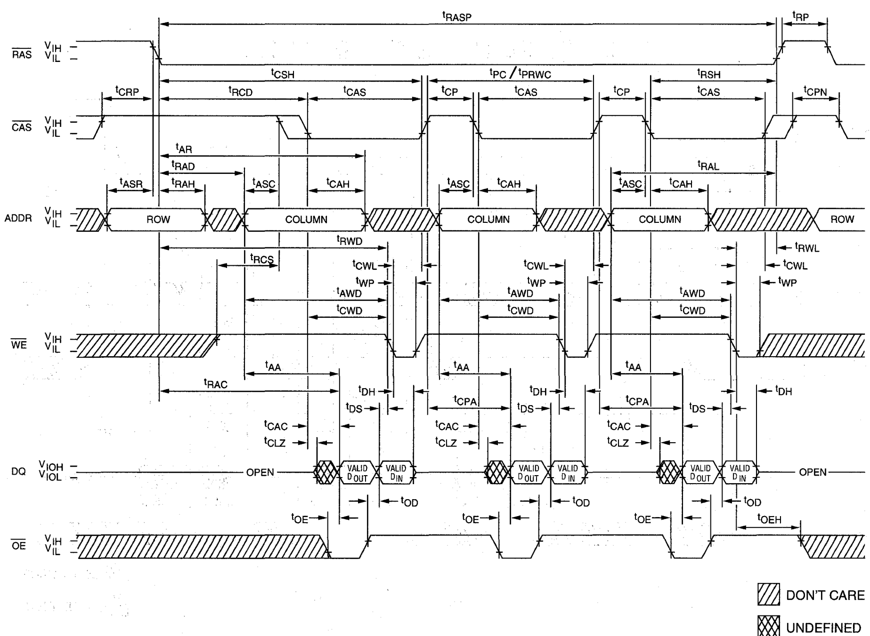
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



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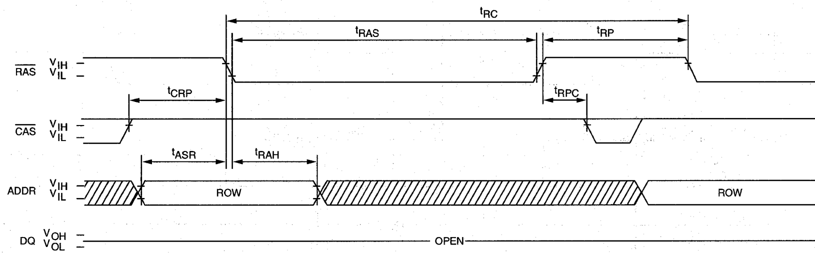
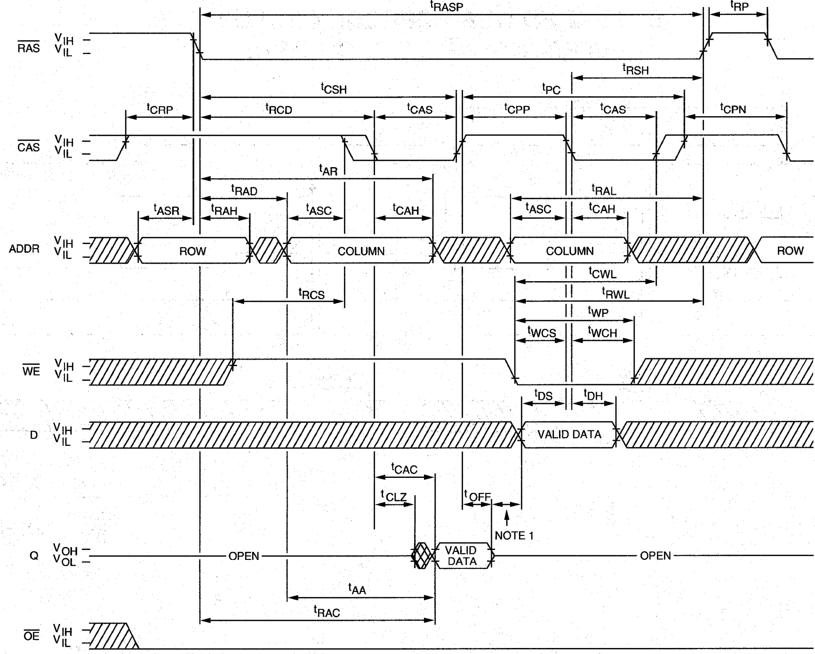
RAS ONLY REFRESH CYCLE
(ADDR = A0/B0-A10; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE:
1. Do not drive data prior to tristate: ^{t}CPP(MIN) or ^{t}CP(whichever is greater) + ^{t}DS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

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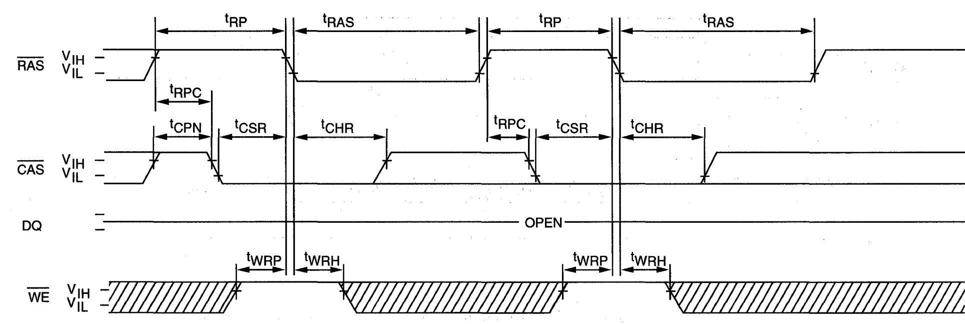
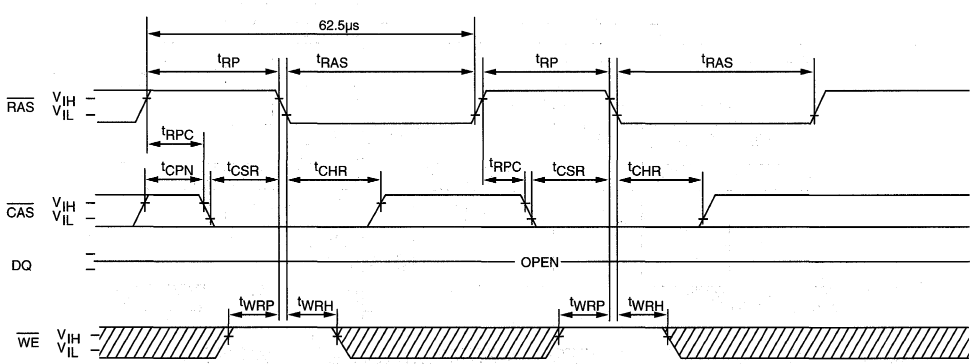
CBR REFRESH CYCLE
(A0/B0-A10, $\overline{OE}$ = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [31]
(A0/B0-A10, $\overline{OE}$ = DON'T CARE)



DON'T CARE

UNDEFINED

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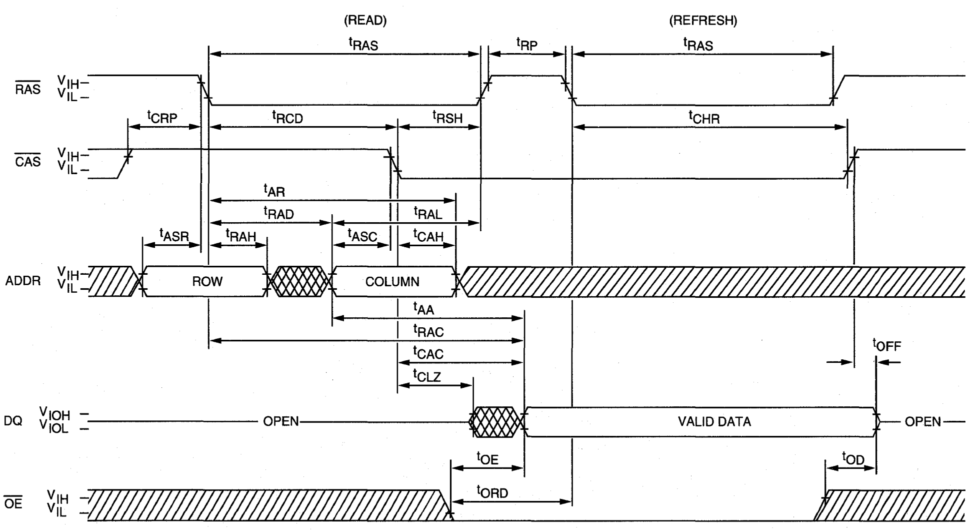
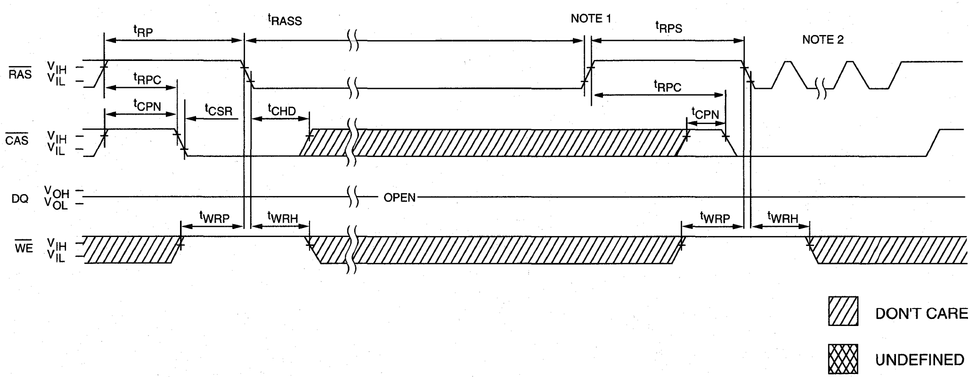
HIDDEN REFRESH CYCLE[21]

($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



SELF REFRESH CYCLE

(A0/B0-A10, $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.

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DRAM CARD PRODUCT SELECTION GUIDE

Memory Configuration		Part Number	Access Time (ns)	Number of Pins Card	Page
1 Meg x 32	4 Megabytes	MT8D88C132(S)	60, 70, 80	88	4-1
1 Meg x 32	4 Megabytes	MT8D88C132H(S)	60, 70, 80	88	4-17
1 Meg x 32	4 Megabytes	MT8D88C132V(S)	60, 70, 80	88	4-33
1 Meg x 32	4 Megabytes	MT8D88C132VH(S)	60, 70, 80	88	4-49
2 Meg x 32	8 Megabytes	MT16D88C232(S)	60, 70, 80	88	4-1
2 Meg x 32	8 Megabytes	MT16D88C232H(S)	60, 70, 80	88	4-17
2 Meg x 32	8 Megabytes	MT16D88C232V(S)	60, 70, 80	88	4-33
2 Meg x 32	8 Megabytes	MT16D88C232VH(S)	60, 70, 80	88	4-49
4 Meg x 32	16 Megabytes	MT8D88C432(S)	60, 70, 80	88	4-1
4 Meg x 32	16 Megabytes	MT8D88C432H(S)	60, 70, 80	88	4-17
4 Meg x 32	16 Megabytes	MT8D88C432V(S)	60, 70, 80	88	4-33
4 Meg x 32	16 Megabytes	MT8D88C432VH(S)	60, 70, 80	88	4-49
8 Meg x 32	32 Megabytes	MT16D88C832(S)	60, 70, 80	88	4-1
8 Meg x 32	32 Megabytes	MT16D88C832H(S)	60, 70, 80	88	4-17
8 Meg x 32	32 Megabytes	MT16D88C832V(S)	60, 70, 80	88	4-33
8 Meg x 32	32 Megabytes	MT16D88C832VH(S)	60, 70, 80	88	4-49

DRAM CARD

4, 8, 16, 32 MEGABYTES

1 MEG, 2 MEG, 4 MEG, 8 MEG x 32;
5.0V FAST PAGE MODE,
OPTIONAL SELF REFRESH

FEATURES

- Low power
- JEDEC-standard 88-pin DRAM card pinout
- Polarized receptacle connector
- Industry-standard DRAM FAST PAGE MODE operation
- High reliability, gold-plated connector
- All outputs fully TTL-compatible
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional SELF REFRESH mode
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Extended Refresh

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Refresh	
Extended Refresh	Blank
SELF REFRESH	S

- Part Number Example: MT8D88C432-6 S

GENERAL DESCRIPTION

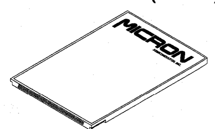
The MT8D88C132/432(S) and MT16D88C232/832(S) comprise a family of JEDEC standard DRAM cards organized in x32-bit memory arrays. The cards may also be configured as x16-bit memory arrays, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented. Four separate $\overline{CAS}$ inputs allow byte accesses.

These cards are designed for low-power operation using low-power, extended refresh DRAMs. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32 organization, the memory is a single array that may be divided into four separate bytes. In the x16 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence-detect pins may be read by the host to identify the card's organization, number of banks, access time and refresh operation. These extensive presence-detect functions allow systems to take full advantage of the

PIN ASSIGNMENT (End View)
88-Pin Card (DF-1)



44 ... 1
88 ... 45

PIN #	4MB	8MB	16MB	32MB	PIN #	4MB	8MB	16MB	32MB
1	Vss	→	→	→	45	Vss	→	→	→
2	DQ0	→	→	→	46	DQ16	→	→	→
3	DQ1	→	→	→	47	DQ17	→	→	→
4	DQ2	→	→	→	48	DQ18	→	→	→
5	DQ3	→	→	→	49	DQ19	→	→	→
6	DQ4	→	→	→	50	DQ20	→	→	→
7	DQ5	→	→	→	51	DQ21	→	→	→
8	DQ6	→	→	→	52	DQ22	→	→	→
9	Vcc	→	→	→	53	DQ23	→	→	→
10	DQ7	→	→	→	54	NC	→	→	→
11	NC	→	→	→	55	NC	→	→	→
12	NC	→	→	→	56	Vss	→	→	→
13	A0	→	→	→	57	A1	→	→	→
14	A2	→	→	→	58	A3	→	→	→
15	Vcc	→	→	→	59	A5	→	→	→
16	A4	→	→	→	60	A7	→	→	→
17	NC	→	→	→	61	A9	→	→	→
18	A6	→	→	→	62	NC	→	→	→
19	A8	→	→	→	63	Vss	→	→	→
20	NC	→	A10	→	64	NC	→	→	→
21	NC	→	→	→	65	NC	$\overline{RAS1}$	NC	$\overline{RAS1}$
22	$\overline{RAS0}$	→	→	→	66	$\overline{CAS2}$	→	→	→
23	$\overline{CAS0}$	→	→	→	67	Vss	→	→	→
24	$\overline{CAS1}$	→	→	→	68	$\overline{CAS3}$	→	→	→
25	NC	→	→	→	69	NC	$\overline{RAS3}$	NC	$\overline{RAS3}$
26	$\overline{RAS2}$	→	→	→	70	$\overline{WE}$	→	→	→
27	Vcc	→	→	→	71	PD1	→	→	→
28	PD2	→	→	→	72	PD3	→	→	→
29	PD4	→	→	→	73	Vss	→	→	→
30	PD6	→	→	→	74	PD5	→	→	→
31	NC	→	→	→	75	PD7	→	→	→
32	NC	→	→	→	76	PD8	→	→	→
33	NC	→	→	→	77	NC	→	→	→
34	DQ8	→	→	→	78	NC	→	→	→
35	NC	→	→	→	79	NC	→	→	→
36	DQ9	→	→	→	80	DQ24	→	→	→
37	Vcc	→	→	→	81	DQ25	→	→	→
38	DQ10	→	→	→	82	DQ26	→	→	→
39	DQ11	→	→	→	83	DQ27	→	→	→
40	DQ12	→	→	→	84	DQ28	→	→	→
41	DQ13	→	→	→	85	DQ29	→	→	→
42	DQ14	→	→	→	86	DQ30	→	→	→
43	DQ15	→	→	→	87	DQ31	→	→	→
44	Vss	→	→	→	88	Vss	→	→	→

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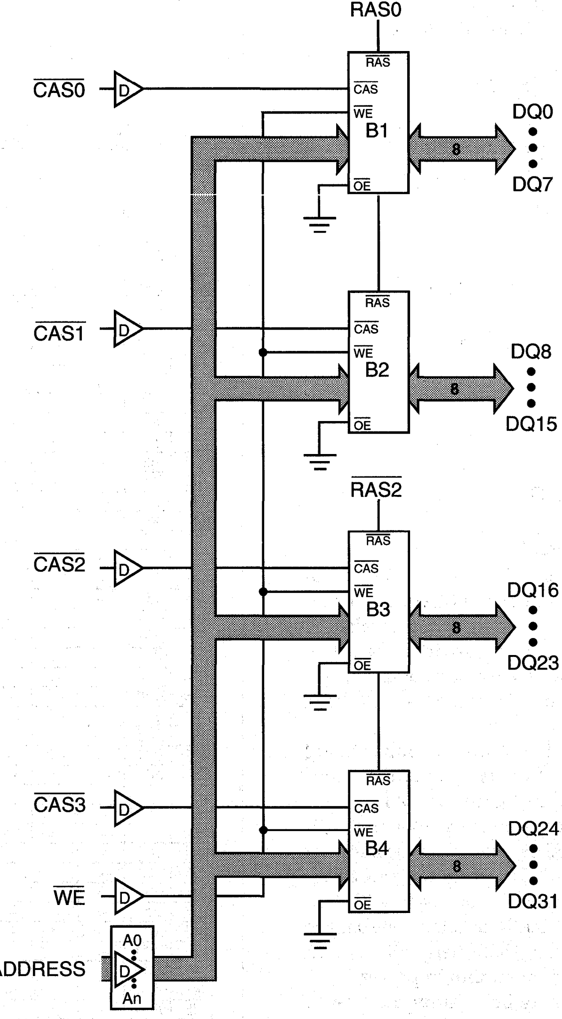
card's advanced power-saving features.

These Micron DRAM cards are built with 3.370-inch-long static dissipative plastic frames covered by metal panels. Packages containing 88-pin receptacle connectors are keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM
(4MB - MT8D88C132, 16MB - MT8D88C432)



NOTE: 1. B1 through B4 = x8 memory blocks.
2. D = 74AC11244 line drivers.

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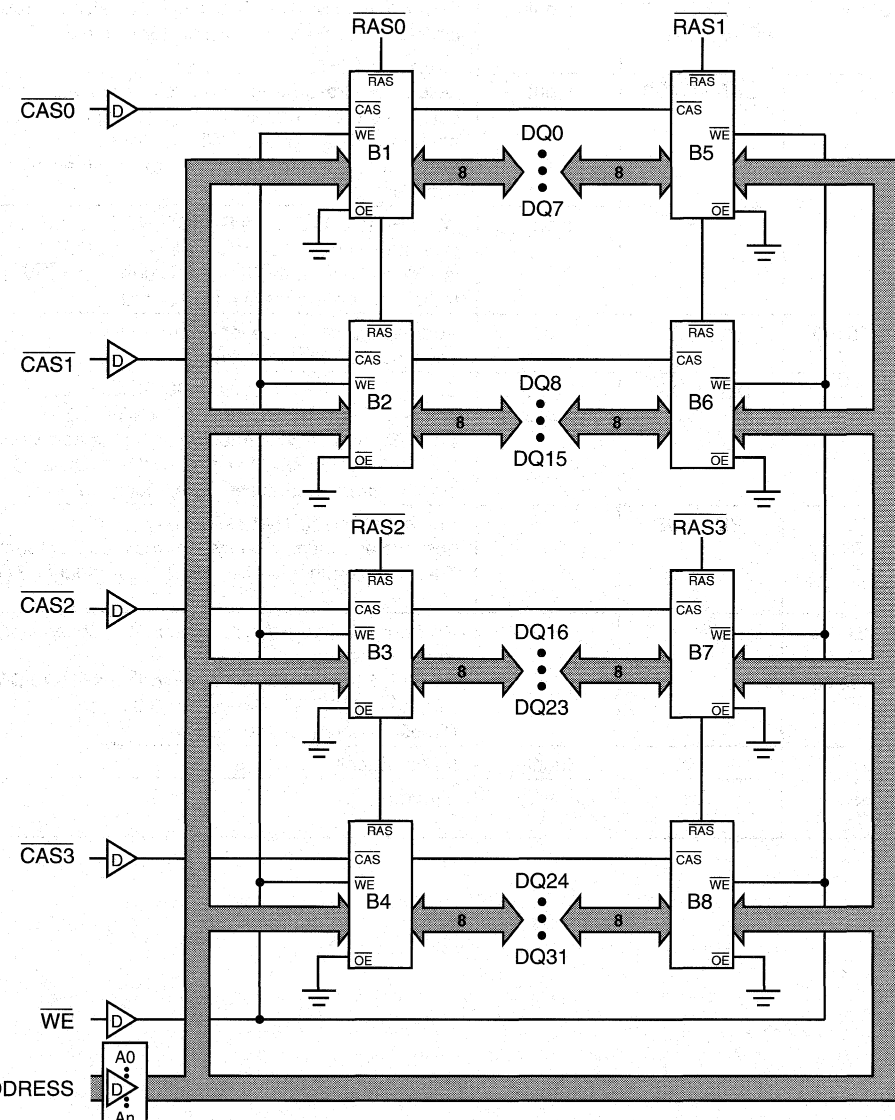
FUNCTIONAL BLOCK DIAGRAM
(8MB - MT16D88C232, 32MB - MT16D88C832)



NOTE: 1. B1 through B8 = x8 memory blocks.
2. D = 74AC11244 line drivers.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	$\overline{RAS0}$, $\overline{RAS2}$ $\overline{RAS1}$, $\overline{RAS3}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch the row-address. Two $\overline{RAS}$ inputs allow for a single x32 bank or two x16 banks.
23, 24, 66, 68	$\overline{CAS0-CAS3}$	Input	Column-Address Strobe: $\overline{CAS}$ is used to latch the column-address, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is a WRITE cycle. If $\overline{WE}$ is HIGH during the $\overline{CAS}$ LOW transition, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61, 20	A0-A10	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ31	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ31 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ31 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or grounded (Vss).
11, 12, 17, 20, 21, 25, 31, 32, 33, 35, 54, 55, 62, 64, 65, 69, 77, 78, 79	NC	-	No Connect: These pins should be left unconnected (reserved for future use). Pins 12, 31-33, 54, 77-79 reserved for x36/x40 DQs. PIns 11, 17, 25, 35 reserved for 3.3V Vcc. Pin 55 reserved for x40 $\overline{OE}$.
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

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MT8D88C132/432(S), MT16D88C232/832(S) 4MB, 8MB, 16MB, 32MB DRAM CARDS

FUNCTIONAL DESCRIPTION

The MT8D88C132/432(S) and MT16D88C232/832(S) comprise a family of DRAM cards organized in x32- bit memory arrays (RAS0 = RAS2). They also may be configured as x16-bit memory arrays provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both RAS lines.

Most x32-bit applications use the same signal to control the CAS inputs. RAS0 and RAS1 control the lower 16 bits and RAS2 and RAS3 control the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQ and CAS pins must be connected (DQ0 to DQ15, DQ1 to DQ16 and so forth, CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x16 memory organizations.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR, extended CBR or HIDDEN) so that all combinations of RAS addresses (A0-A9/A10) are executed at least every tREF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

The implied method of choice for refreshing the memory card is the extended CBR cycle. This is a very low-current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common to standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the extended CBR REFRESH cycle. However, the memory card will draw more current in the standby mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20/22 address bits, which are entered 10/11 bits (A0-A9/A10) at a time. RAS is used to latch the first 10/11 bits, and CAS latches the latter 10/11 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. WE must fall prior to CAS (EARLY WRITE). The data inputs and data outputs are routed through pins using common I/O and pin direction is controlled by WE.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row-address-defined (A0 - A9/A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation. Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time.

REFRESH

An optional SELF REFRESH mode is also available. The "S" option allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" option allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ^{t}RPS ($\approx^{t}$RC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or BURST REFRESH sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

PHYSICAL DESIGN

These Micron DRAM cards are constructed with a 3.370-inch-long static dissipative plastic frame covered by metal panels. Inside, thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high-insertion, 88-pin receptacle connector. The package is keyed to prevent improper installation, including insertion into other types of IC card sockets. The DRAM cards operate reliably up to 55°C.

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NEW DRAM CARD

MEMORY TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ0-DQ31
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
READ WRITE		L	L	H→L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Data-Out
RAS ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH (S-version only)		H→L	L	H	X	X	High-Z

PRESENCE-DETECT TRUTH TABLE

Card Density	DRAM Organizations	# of Address	RAS Address	CAS Address	Page Depth	PDx 1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC			
1MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	NC			
2MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	Vss			
2MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	NC			
4MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	Vss			
•4MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	NC			
•8MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	Vss			
8MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	NC			
16MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	Vss			
•16MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	NC			
•32MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	Vss			
Access Timing tRAC Max	100ns										Vss	Vss	
	80ns										NC	Vss	
	70ns										Vss	NC	
	60ns										NC	NC	
	50ns										Vss	Vss	
Refresh Control	Extended												NC
	SELF, Extended												Vss

NOTE: Vss = ground.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1.0V to +7V
Operating Temperature T_A (ambient) .... 0°C to 55°C
Storage Temperature .... -40°C to +70°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Card Insertions (connector's life cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

NEW DRAM CARD

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ± 5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input: 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V) for each package input	$\overline{RAS0-RAS3}$	I_{I1}	-8	8	µA	
	Buffered	I_{I2}	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ0-DQ31	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5 mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2 mA)		V_{OL}		0.4	V	

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NEW DRAM CARD

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ± 5%)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC1}	4MB 8MB 16MB 32MB	880 896 960 976	800 816 880 896	720 736 800 816	mA	3, 4, 31
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	4MB 8MB 16MB 32MB	16 32 16 32	16 32 16 32	16 32 16 32	mA	
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC3}	4MB 8MB 16MB 32MB	640 656 720 736	560 576 640 656	480 496 560 576	mA	3, 4, 31
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = Vcc -0.2V)	I_{CC4}	4MB 8MB 16MB 32MB	1.6 3.2 1.6 3.2	1.6 3.2 1.6 3.2	1.6 3.2 1.6 3.2	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	4MB 8MB 16MB 32MB	880 896 960 976	800 816 880 896	720 736 800 816	mA	3, 31
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	4MB 8MB 16MB 32MB	880 960 896 976	800 880 816 896	720 800 736 816	mA	3, 5
REFRESH CURRENT: Extended CBR Average power supply current during extended CBR: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); ^tRC = 125µs; $\overline{WE}$, A0-A10 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	I_{CC7}	4MB 8MB 16MB 32MB	2.4 4.8 2.4 4.8	2.4 4.8 2.4 4.8	2.4 4.8 2.4 4.8	mA	3, 5
REFRESH CURRENT: SELF (S-version only) Average power supply current, CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc-0.2V; A0-A11 and D_{IN} = Vcc - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	4MB 8MB 16MB 32MB	2.4 4.8 2.4 4.8	2.4 4.8 2.4 4.8	2.4 4.8 2.4 4.8	mA	5, 32

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CAPACITANCE

PARAMETER	SYMBOL	MAX 4,16MB	MAX 8, 32MB	UNITS	NOTES
Input Capacitance: $\overline{\text{CAS0-CAS3}}$	C_{I1}	9	9	pF	2
Input Capacitance: $\overline{\text{WE}}$	C_{I2}	13	13	pF	2
Input Capacitance: $\overline{\text{RAS0-RAS3}}$	C_{I3}	34	34	pF	2
Input/Output Capacitance: DQ0-DQ31	C_{IO}	10	18	pF	2
Input Capacitance: Addressess	C_{I3}	9	9	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le 55°C$; V_{CC} = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		45		ns	23
Access time from $\overline{\text{RAS}}$	^{t}RAC		60		70		80	ns	14, 23
Access time from $\overline{\text{CAS}}$	^{t}CAC		22		27		27	ns	15, 26
Access time from column-address	^{t}AA		37		42		47	ns	26
Access time from $\overline{\text{CAS}}$ precharge	^{t}CPA		42		47		52	ns	26
$\overline{\text{RAS}}$ pulse width	^{t}RAS	60	100,000	70	100,000	80	100,000	ns	23
$\overline{\text{RAS}}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	23
$\overline{\text{RAS}}$ hold time	^{t}RSH	22		27		27		ns	26
$\overline{\text{RAS}}$ precharge time	^{t}RP	45		50		60		ns	23
$\overline{\text{CAS}}$ pulse width	^{t}CAS	15	100,000	20	100,000	20	100,000	ns	23
$\overline{\text{CAS}}$ hold time	^{t}CSH	58		68		78		ns	25
$\overline{\text{CAS}}$ precharge time	^{t}CPN	10		10		10		ns	16, 23
$\overline{\text{CAS}}$ precharge time (FAST PAGE MODE)	^{t}CP	10		10		10		ns	23
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	^{t}RCD	18	38	18	43	18	53	ns	17, 27
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	^{t}CRP	17		17		17		ns	26
Row-address setup time	^{t}ASR	7		7		7		ns	26
Row-address hold time	^{t}RAH	8		8		8		ns	25
$\overline{\text{RAS}}$ to column-address delay time	^{t}RAD	13	23	13	28	13	33	ns	18, 27
Column-address setup time	^{t}ASC	2		2		2		ns	24
Column-address hold time	^{t}CAH	10		15		15		ns	23
Column-address hold time (referenced to $\overline{\text{RAS}}$)	^{t}AR	48		53		58		ns	25
Column-address to $\overline{\text{RAS}}$ lead time	^{t}RAL	37		42		47		ns	26
Read command setup time	^{t}RCS	2		2		2		ns	24
Read command hold time (referenced to $\overline{\text{CAS}}$)	^{t}RCH	2		2		2		ns	19, 24
Read command hold time (referenced to $\overline{\text{RAS}}$)	^{t}RRH	0		0		0		ns	19, 23

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	5		5		5		ns	24, 33
Output buffer turn-off delay	^{t}OFF	5	22	5	27	5	27	ns	20, 28
$\overline{WE}$ command setup time	^{t}WCS	2		2		2		ns	24
Write command hold time	^{t}WCH	10		15		15		ns	23
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	43		53		58		ns	25
Write command pulse width	^{t}WP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	^{t}RWL	22		27		27		ns	26
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		20		ns	23
Data-in setup time	^{t}DS	2		2		2		ns	24
Data-in hold time	^{t}DH	17		22		22		ns	26
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		60		ns	23
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	9, 10, 23
Refresh period (1,024 cycles)	^{t}REF		128		128		128	ms	35
Refresh period (2,048 cycles)	^{t}REF		128		128		128	ms	34
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	23
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	12		12		12		ns	5, 24
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	8		8		8		ns	5, 25
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	8		8		8		ns	22, 25
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	12		12		12		ns	22, 24
$\overline{WE}$ hold time (WCBR test cycle)	^{t}WTH	8		8		8		ns	22, 25
$\overline{WE}$ setup time	^{t}WTS	12		12		12		ns	22, 24
$\overline{RAS}$ pulse width entering SELF REFRESH	^{t}RASS	100		100		100		µs	23, 32
$\overline{RAS}$ precharge time exiting SELF REFRESH	^{t}RPS	110		130		150		ns	23, 32
$\overline{CAS}$ hold time entering SELF REFRESH	^{t}CHD	15		15		15		ns	25, 32

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 5V ±10%; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^tWRP and ^tWRH in the CBR REFRESH cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +2ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -2ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +7ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -2ns (MIN) and a -7ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A +2ns (MIN) and a +7ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. The maximum current ratings are based on one of the two banks operating or being refreshed in a x32 mode. The stated maximums may be reduced by one-half when used in the x16 mode.
30. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
31. Column-address changed once each cycle.
32. If the DRAM controller uses a BURST REFRESH, a BURST REFRESH of all rows must be executed upon exiting SELF REFRESH.
33. The 3ns minimum is a parameter guaranteed by design.
34. 16MB and 32MB versions.
35. 4MB and 8MB versions.

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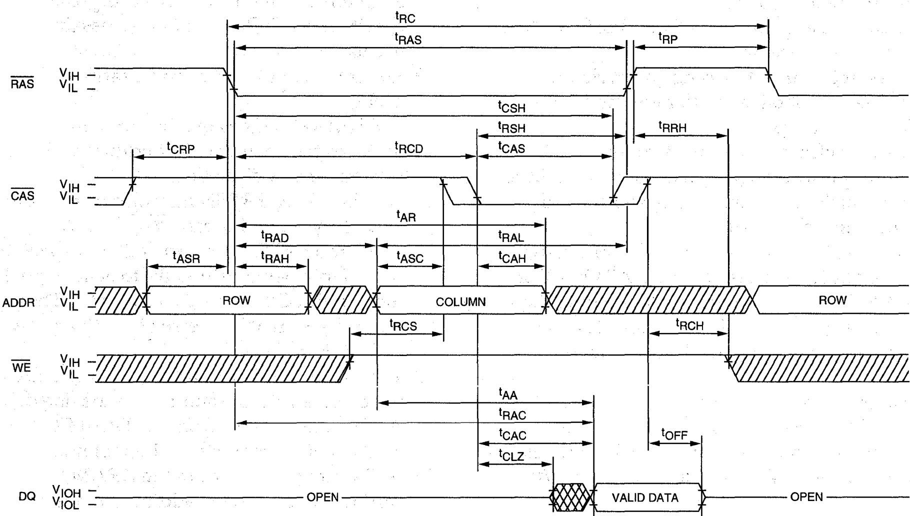
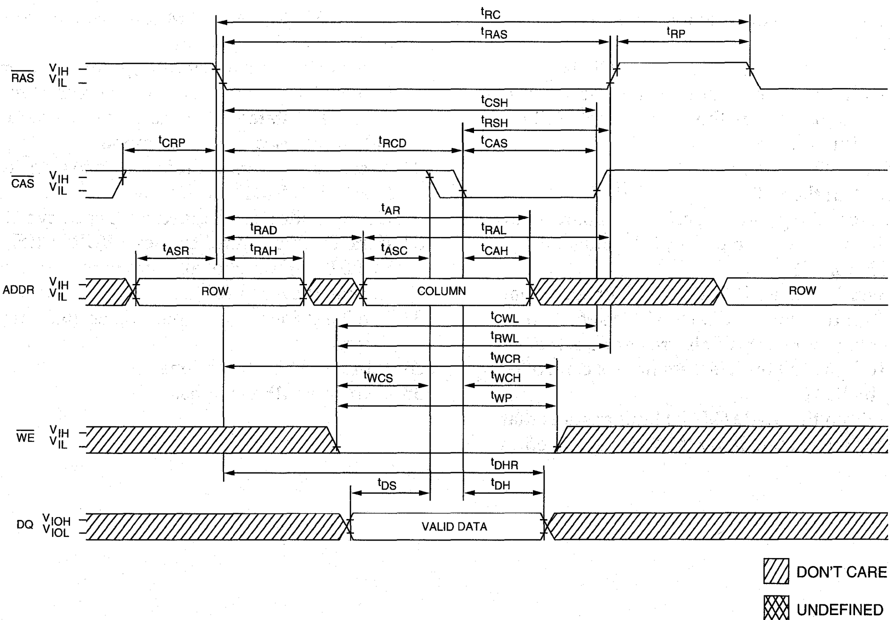
NEW DRAM CARD

READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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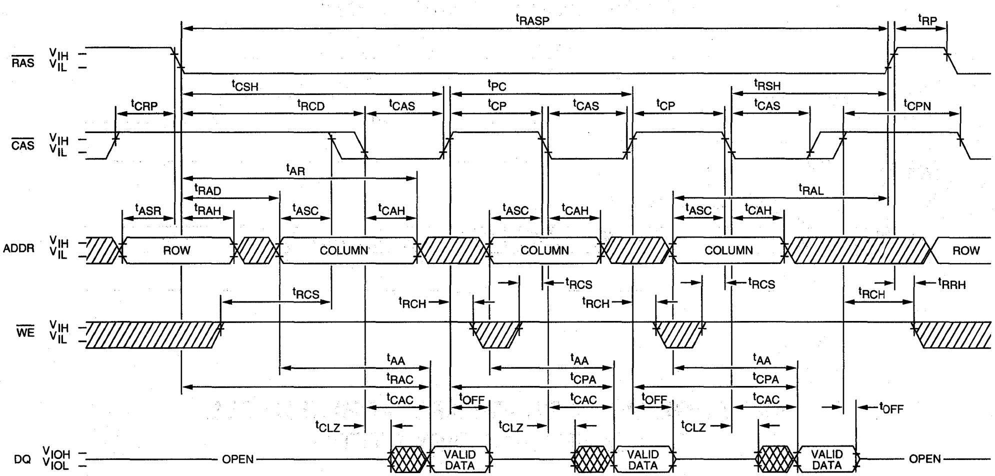
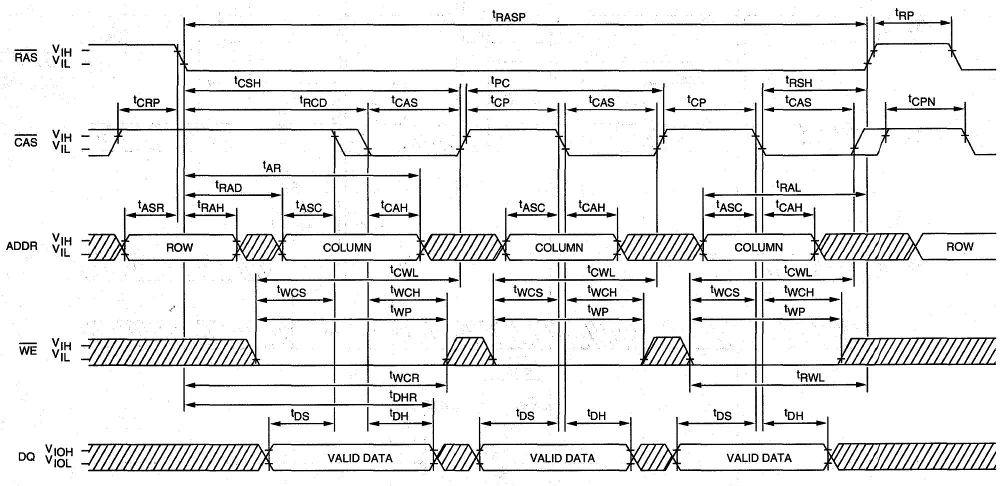
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



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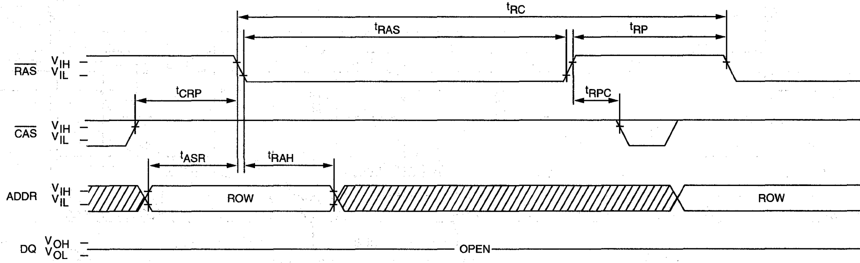
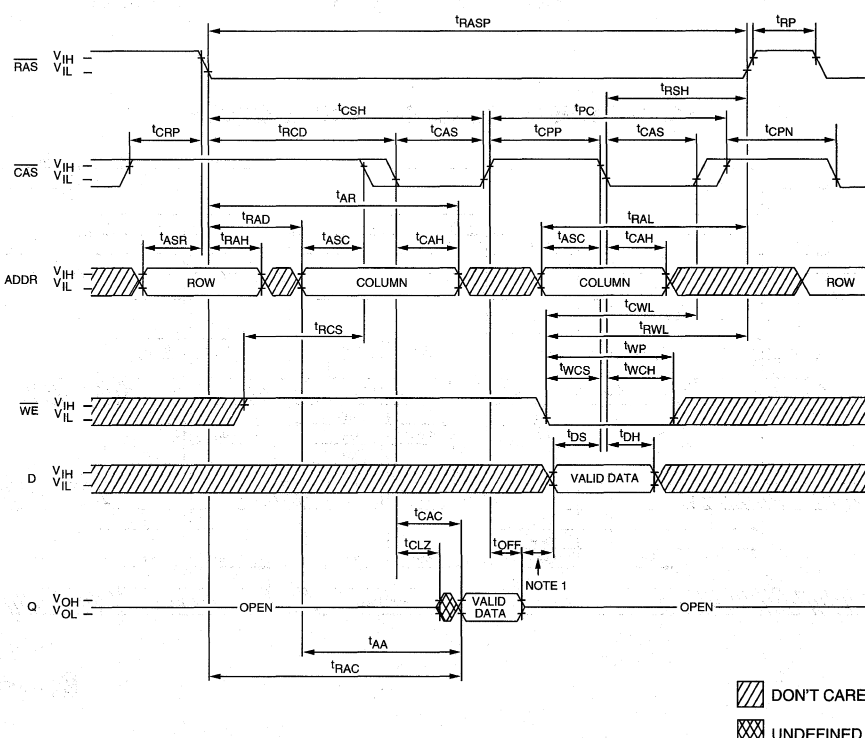
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

(ADDRESS; $\overline{\text{WE}}$ = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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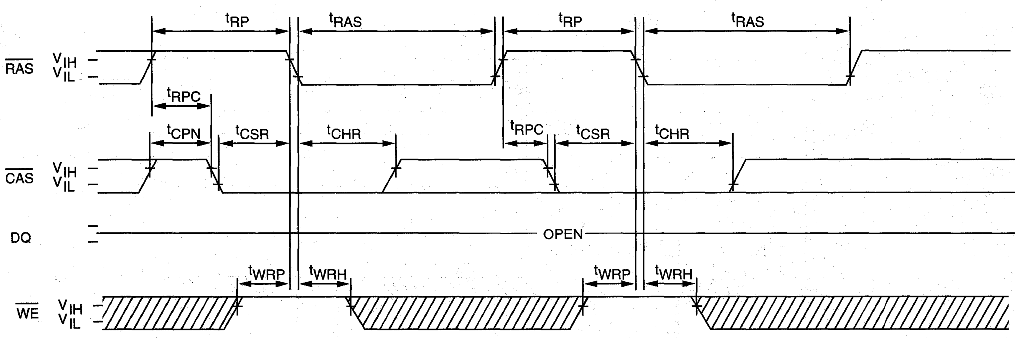
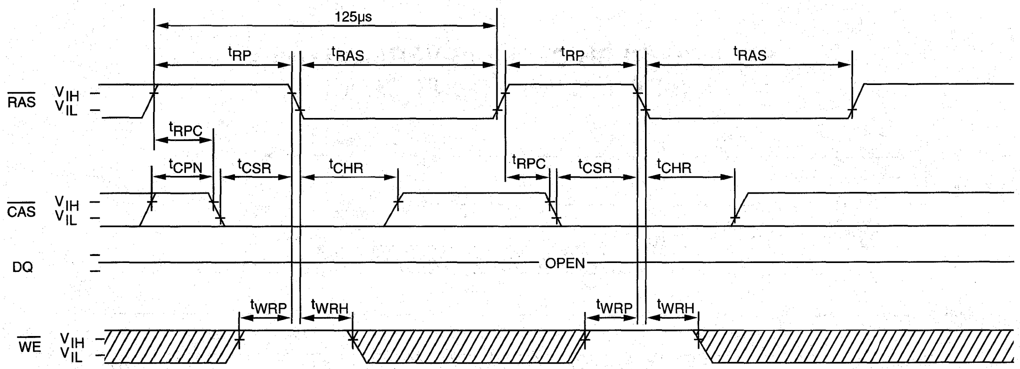
CBR REFRESH CYCLE
(ADDRESS = DON'T CARE)



EXTENDED CBR REFRESH CYCLE
(ADDRESS = DON'T CARE)



DON'T CARE

UNDEFINED

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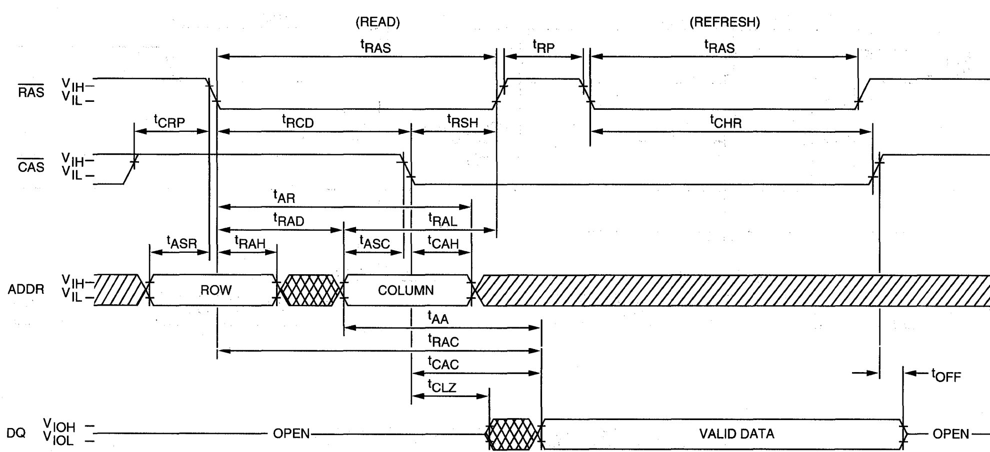
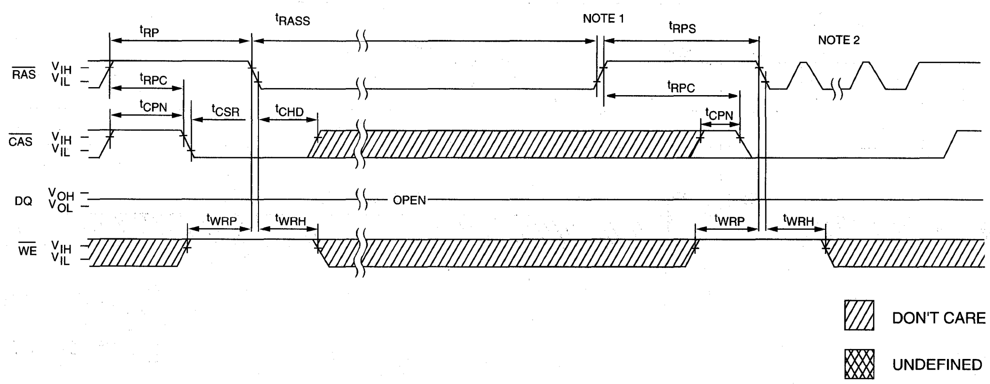
HIDDEN REFRESH CYCLE [21]

(WE = HIGH)



SELF REFRESH CYCLE (S-VERSION ONLY)

(ADDRESSES = DON'T CARE)



NOTE: 1. Once tRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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DRAM MINICARD

4, 8,16, 32 MEGABYTES

1 MEG, 2 MEG, 4 MEG, 8 MEG x 32;
5.0V FAST PAGE MODE,
OPTIONAL SELF REFRESH

FEATURES

- Low power
- JEDEC-standard 88-pin DRAM card pinout
- 2-inch (50.8mm)-long nonbuffered DRAM cards
- Polarized receptacle connector
- Industry-standard DRAM FAST PAGE MODE operation
- High reliability, gold-plated connector
- All outputs fully TTL-compatible
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional SELF REFRESH mode
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Extended Refresh

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Refresh	
Extended Refresh	Blank
SELF REFRESH	S

- Part Number Example: MT8D88C432H-6 S

GENERAL DESCRIPTION

The MT8D88C132H/432H(S) and MT16D88C232H/832H(S) comprise a family of DRAM cards organized in x32-bit memory arrays. These DRAM cards are 2-inch-long bufferless versions of the JEDEC-standard 3.37-inch (85.6mm), 88-pin x32 DRAM cards. Buffers are not included on these cards, so the on-board timing delays have been eliminated. Redrive circuitry may be implemented on the system board.

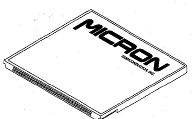
These cards may also be configured as a x16-bit memory arrays, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented. Four separate $\overline{CAS}$ inputs allow byte accesses.

These MiniCards are designed for low-power operation using low-power, extended refresh DRAMs. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32 organization, the memory is a single array that may be divided into four separate bytes. In the x16 organization, up to two banks, each with two

PIN ASSIGNMENT (End View)

88-Pin Card (DF-4)



PIN #	4MB	8MB	16MB	32MB	PIN #	4MB	8MB	16MB	32MB
1	Vss	→	→	→	45	Vss	→	→	→
2	DQ0	→	→	→	46	DQ16	→	→	→
3	DQ1	→	→	→	47	DQ17	→	→	→
4	DQ2	→	→	→	48	DQ18	→	→	→
5	DQ3	→	→	→	49	DQ19	→	→	→
6	DQ4	→	→	→	50	DQ20	→	→	→
7	DQ5	→	→	→	51	DQ21	→	→	→
8	DQ6	→	→	→	52	DQ22	→	→	→
9	NC	→	→	→	53	DQ23	→	→	→
10	DQ7	→	→	→	54	NC	→	→	→
11	3.3V Vcc	→	→	→	55	NC	→	→	→
12	NC	→	→	→	56	Vss	→	→	→
13	A0	→	→	→	57	A1	→	→	→
14	A2	→	→	→	58	A3	→	→	→
15	NC	→	→	→	59	A5	→	→	→
16	A4	→	→	→	60	A7	→	→	→
17	3.3V Vcc	→	→	→	61	A9	→	→	→
18	A6	→	→	→	62	NC	→	→	→
19	A8	→	→	→	63	Vss	→	→	→
20	NC	→	A10	→	64	NC	→	→	→
21	NC	→	→	→	65	NC	$\overline{RAS1}$	NC	$\overline{RAS1}$
22	$\overline{RAS0}$	→	→	→	66	$\overline{CAS2}$	→	→	→
23	$\overline{CAS0}$	→	→	→	67	Vss	→	→	→
24	$\overline{CAS1}$	→	→	→	68	$\overline{CAS3}$	→	→	→
25	3.3V Vcc	→	→	→	69	NC	$\overline{RAS3}$	NC	$\overline{RAS3}$
26	$\overline{RAS2}$	→	→	→	70	$\overline{WE}$	→	→	→
27	NC	→	→	→	71	PD1	→	→	→
28	PD2	→	→	→	72	PD3	→	→	→
29	PD4	→	→	→	73	Vss	→	→	→
30	PD6	→	→	→	74	PD5	→	→	→
31	NC	→	→	→	75	PD7	→	→	→
32	NC	→	→	→	76	PD8	→	→	→
33	NC	→	→	→	77	NC	→	→	→
34	DQ8	→	→	→	78	NC	→	→	→
35	3.3V Vcc	→	→	→	79	NC	→	→	→
36	DQ9	→	→	→	80	DQ24	→	→	→
37	NC	→	→	→	81	DQ25	→	→	→
38	DQ10	→	→	→	82	DQ26	→	→	→
39	DQ11	→	→	→	83	DQ27	→	→	→
40	DQ12	→	→	→	84	DQ28	→	→	→
41	DQ13	→	→	→	85	DQ29	→	→	→
42	DQ14	→	→	→	86	DQ30	→	→	→
43	DQ15	→	→	→	87	DQ31	→	→	→
44	Vss	→	→	→	88	Vss	→	→	→

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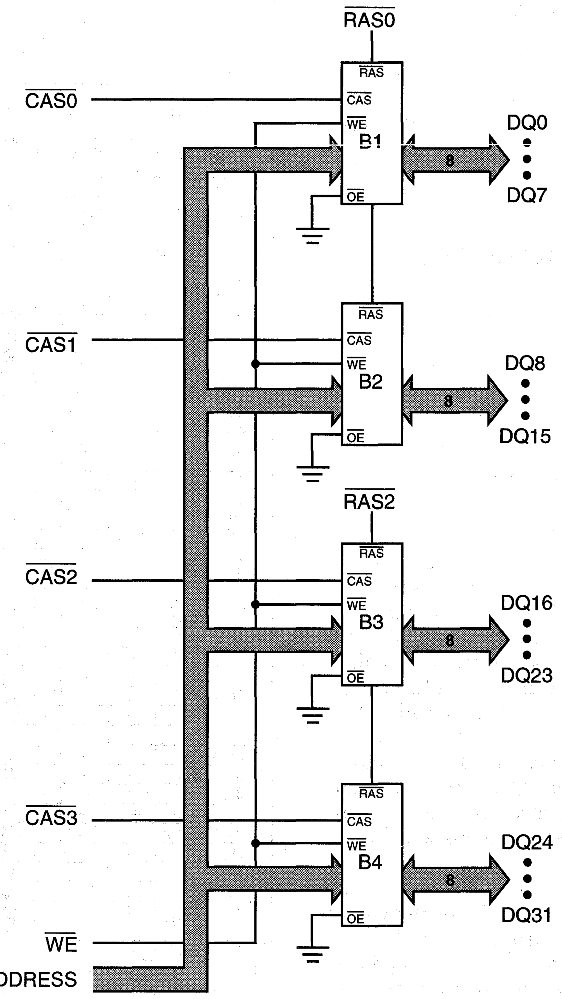
separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence-detect pins may be read by the host to identify the card's organization, number of banks, access time and refresh operation. These extensive presence-detect functions allow systems to take full advantage of the advanced power-saving features.

These Micron DRAM cards are built with 2-inch-long static dissipative plastic frames covered by metal panels. Packages containing 88-pin receptacle connectors are keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM
(4MB - MT8D88C132H, 16MB - MT8D88C432H)



NOTE: 1. B1 through B4 = x8 memory blocks.

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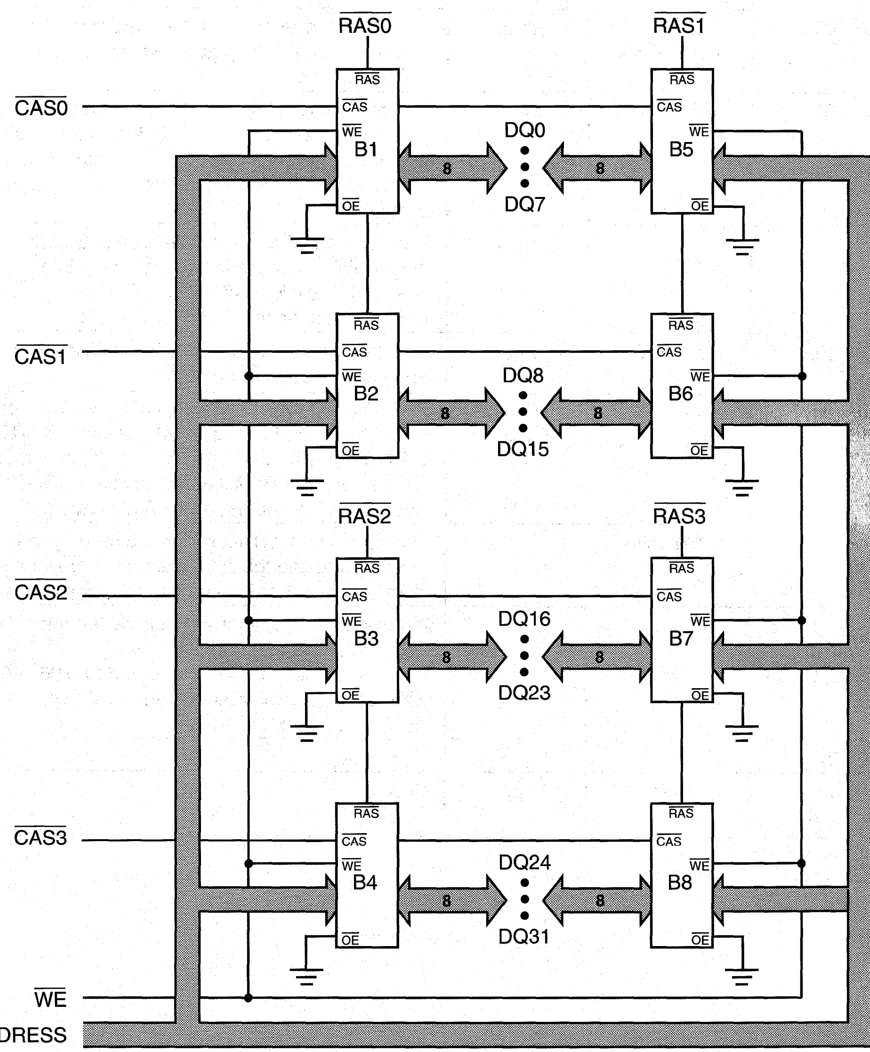
FUNCTIONAL BLOCK DIAGRAM

(8MB - MT16D88C232H, 32MB - MT16D88C832H)



NOTE: 1. B1 through B8 = x8 memory blocks.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	$\overline{RAS0}$, $\overline{RAS2}$ $\overline{RAS1}$, $\overline{RAS3}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch the row-address. Two $\overline{RAS}$ inputs allow for a single x32 bank or two x16 banks.
23, 24, 66, 68	$\overline{CAS0\text{-}CAS3}$	Input	Column-Address Strobe: $\overline{CAS}$ is used to latch the column-address, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is a WRITE cycle. If $\overline{WE}$ is HIGH during the $\overline{CAS}$ LOW transition, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61, 20	A0-A10	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ31	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ31 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ31 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or grounded (Vss).
9, 11, 12, 15, 17, 20, 21, 25, 27, 31, 32, 33, 35, 37, 54, 55, 62, 64, 65, 69, 77, 78, 79	NC	-	No Connect: These pins should be left unconnected (reserved for future use). Pins 12, 31-33, 54, 77-79 reserved for x36/x40 DQs. PIns 11, 17, 25, 35 reserved for 3.3V Vcc. Pin 55 reserved for x40 $\overline{OE}$.
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

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FUNCTIONAL DESCRIPTION

The MT8D88C132H/432H(S) and MT16D88C232H/832H(S) comprise a family of DRAM cards organized in x32-bit memory arrays (RAS0 = RAS2). They also may be configured as x16-bit memory arrays provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both RAS lines.

Most x32-bit applications use the same signal to control the CAS inputs. RAS0 and RAS1 control the lower 16 bits and RAS2 and RAS3 control the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQ and CAS pins must be connected (DQ0 to DQ15, DQ1 to DQ16 and so forth, CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x16 memory organizations.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR, extended CBR or HIDDEN) so that all combinations of RAS addresses (A0-A9/A10) are executed at least every tREF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

The implied method of choice for refreshing the memory card is the extended CBR cycle. This is a very low-current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common to standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the extended CBR REFRESH cycle. However, the memory card will draw more current in the standby mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20/22 address bits, which are entered 10/11 bits (A0-A9/A10) at a time. RAS is used to latch the first 10/11 bits, and CAS latches the latter 10/11 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. WE must fall prior to CAS (EARLY WRITE). The data inputs and data outputs are routed through pins using common I/O and pin direction is controlled by WE.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row-address-defined (A0-A9/A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation. Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time.

REFRESH

An optional SELF REFRESH mode is also available. The "S" option allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" option allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ^{t}RPS ($\approx^{t}$RC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or BURST REFRESH sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

PHYSICAL DESIGN

These Micron DRAM MiniCards are constructed with a 2-inch-long static dissipative plastic frame covered by metal panels. Inside, thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high-insertion, 88-pin receptacle connector. The package is keyed to prevent improper installation, including insertion into other types of IC card sockets. The DRAM cards operate reliably up to 55°C.

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MEMORY TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDRESSES ^{t}R	ADDRESSES ^{t}C	DATA IN/OUT DQ0-DQ31
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
READ WRITE		L	L	H→L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Data-Out
$\overline{\text{RAS}}$ ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH (S-version only)		H→L	L	H	X	X	High-Z

PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS						PRESENCE-DETECT PIN (PDx)							
Card Density	DRAM Organizations	# of Address	$\overline{\text{RAS}}$ Address	$\overline{\text{CAS}}$ Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC			
1MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	NC			
2MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	Vss			
2MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	NC			
4MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	Vss			
•4MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	NC			
•8MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	Vss			
8MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	NC			
16MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	Vss			
•16MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	NC			
•32MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	Vss			
Access Timing ^{t}RAC Max		100ns									Vss	Vss	
		80ns									NC	Vss	
		70ns									Vss	NC	
		60ns									NC	NC	
		50ns									Vss	Vss	
Refresh Control		Extended											NC
		SELF, Extended											Vss

NOTE: Vss = ground.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1.0V to +7V
Operating Temperature T_A (ambient) .... 0°C to 55°C
Storage Temperature .... -40°C to +70°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Card Insertions (connector's life cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ± 5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.75	5.25	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	RAS0-RAS3	II1	-8	8	µA	
Any input: 0V ≤ VIN ≤ 6.5V	A0-A10, WE	II2	-10	10	µA	
(All other pins not under test = 0V) for each package input	CAS0-CAS3	II3	-8	8	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ VOUT ≤ 5.5V) for each package input	DQ0-DQ31	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5 mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2 mA)		VOL		0.4	V	

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NEW DRAM CARD

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ± 5%)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC1}	4MB	880	800	720	mA	3, 4, 27
		8MB	896	816	736		
		16MB	960	880	800		
		32MB	976	896	816		
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	4MB	16	16	16	mA	
		8MB	32	32	32		
		16MB	16	16	16		
		32MB	32	32	32		
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ${}^tPC$ = ${}^tPC$ [MIN])	I_{CC3}	4MB	640	560	480	mA	3, 4, 27
		8MB	656	576	496		
		16MB	720	640	560		
		32MB	736	656	576		
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = Vcc -0.2V)	I_{CC4}	4MB	1.6	1.6	1.6	mA	
		8MB	3.2	3.2	3.2		
		16MB	1.6	1.6	1.6		
		32MB	3.2	3.2	3.2		
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC5}	4MB	880	800	720	mA	3, 27
		8MB	896	816	736		
		16MB	960	880	800		
		32MB	976	896	816		
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC6}	4MB	880	800	720	mA	3, 5
		8MB	896	816	736		
		16MB	960	880	800		
		32MB	976	896	816		
REFRESH CURRENT: Extended CBR Average power supply current during extended CBR: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ${}^tRAS$ (MIN); ${}^tRC$ = 125µs; $\overline{WE}$, A0-A10 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	I_{CC7}	4MB	2.4	2.4	2.4	mA	3, 5
		8MB	4.8	4.8	4.8		
		16MB	2.4	2.4	2.4		
		32MB	4.8	4.8	4.8		
REFRESH CURRENT: SELF (S-version only) Average power supply current, CBR cycling with $\overline{RAS}$ ≥ ${}^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc-0.2V; A0-A11 and D_{IN} = Vcc - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	4MB	2.4	2.4	2.4	mA	5, 29
		8MB	4.8	4.8	4.8		
		16MB	2.4	2.4	2.4		
		32MB	4.8	4.8	4.8		

CAPACITANCE

PARAMETER	SYMBOL	MAX 4,16MB	MAX 8, 32MB	UNITS	NOTES
Input Capacitance: $\overline{CAS0\text{-}CAS3}$	C_{I1}	17	32	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}	66	66	pF	2
Input Capacitance: $\overline{RAS0\text{-}RAS3}$	C_{I3}	34	34	pF	2
Input/Output Capacitance: DQ0-DQ31	C_{IO}	10	18	pF	2
Input Capacitance: Addresses	C_{I3}	51	90	pF	2

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	
Access time from RAS	tRAC		60		70		80	ns	14
Access time from CAS	tCAC		15		20		20	ns	15
Access time from column-address	tAA		30		35		40	ns	
Access time from CAS precharge	tCPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	tCPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row-address setup time	tASR	0		0		0		ns	
Row-address hold time	tRAH	10		10		10		ns	
RAS to column-address delay time	tRAD	15	30	15	35	20	40	ns	18
Column-address setup time	tASC	0		0		0		ns	
Column-address hold time	tCAH	10		15		15		ns	
Column-address hold time (referenced to RAS)	tAR	50		55		60		ns	
Column-address to RAS lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	tRCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	19
CAS to output in Low-Z	tCLZ	3		3		3		ns	26
Output buffer turn-off delay	tOFF	3	15	3	20	3	20	ns	20, 26
WE command setup time	tWCS	0		0		0		ns	

NEW DRAM CARD

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to RAS lead time	^tRWL	15		20		20		ns	
Write command to CAS lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	24
Data-in hold time	^tDH	10		15		15		ns	24
Data-in hold time (referenced to RAS)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		128		128		128	ms	30
Refresh period (2,048 cycles)	^tREF		128		128		128	ms	29
RAS to CAS precharge time	^tRPC	0		0		0		ns	
CAS setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
CAS hold time (CBR REFRESH)	^tCHR	15		15		15		ns	5
WE hold time (CBR REFRESH)	^tWRH	10		10		10		ns	22
WE setup time (CBR REFRESH)	^tWRP	10		10		10		ns	22
WE hold time (WCBR test cycle)	^tWTH	10		10		10		ns	22
WE setup time	^tWTS	10		10		10		ns	22
RAS pulse width entering SELF REFRESH	^tRASS	100		100		100		µs	28
RAS precharge time exiting SELF REFRESH	^tRPS	110		130		150		ns	28
CAS hold time entering SELF REFRESH	^tCHD	15		15		15		ns	28

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1. Vcc = 5V ±5%; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If CAS = VIH, data output is High-Z.
12. If CAS = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
23. The maximum current ratings are based on the memory operating or being refreshed in the x32 mode. The stated maximums may be reduced by one-half when used in the x16 mode.
24. These parameters are referenced to CAS leading edge in EARLY WRITE cycles.
25. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to OE being tied permanently LOW on all 4 Meg DRAMs.
26. The 3ns minimum is a parameter guaranteed by design.
27. Column-address changed once each cycle.
28. If the DRAM controller uses a BURST REFRESH, a BURST REFRESH of all rows must be executed upon exiting SELF REFRESH.
29. 16MB and 32MB versions only.
30. 4MB and 8MB versions only.

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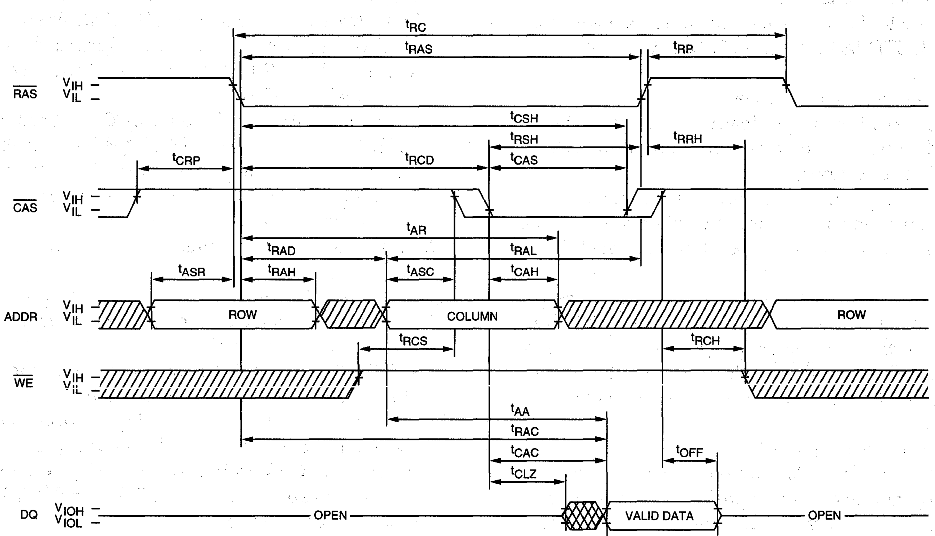
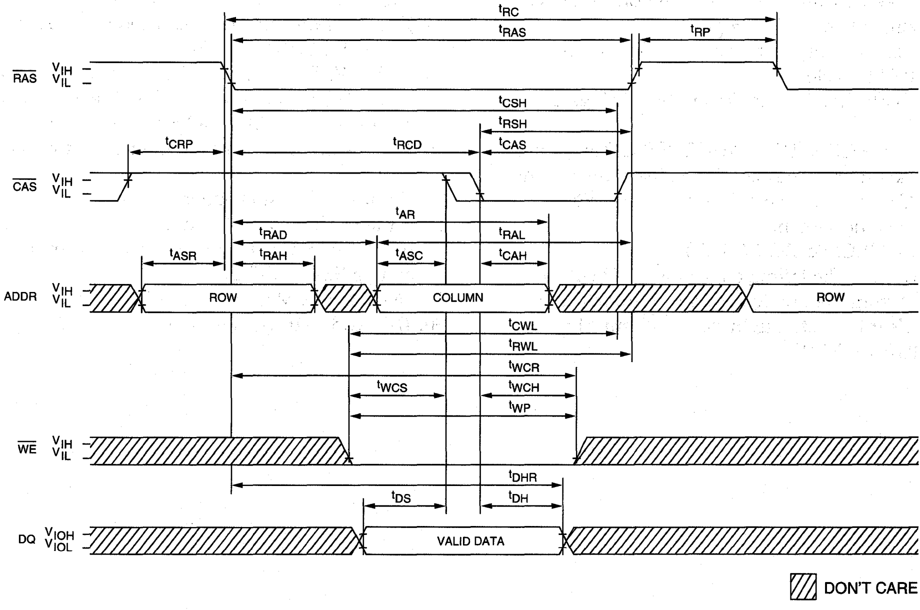
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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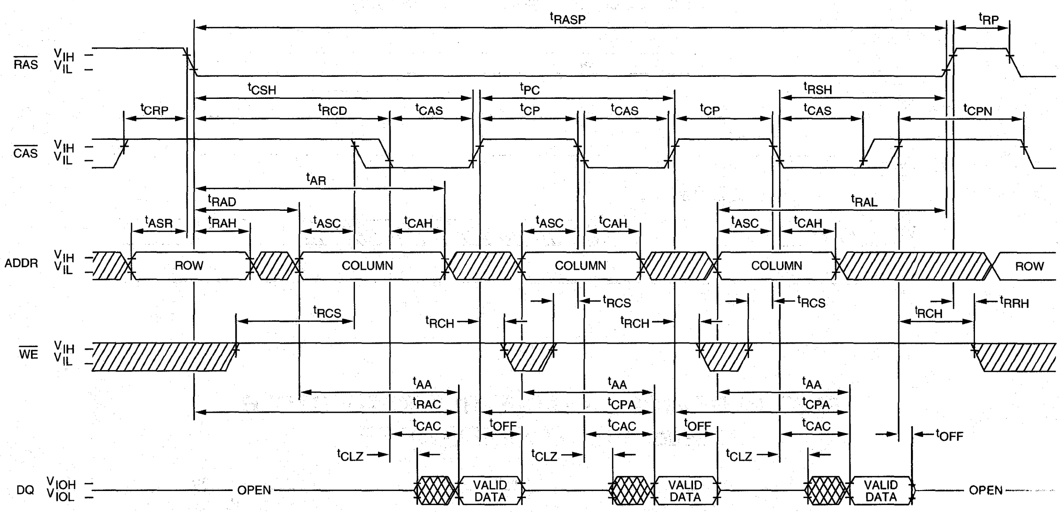
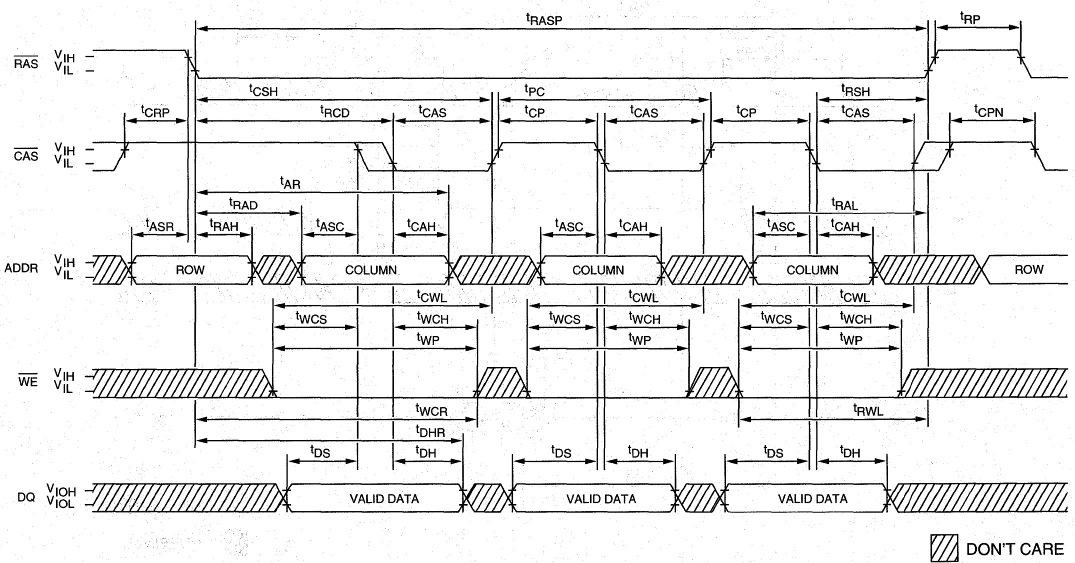
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

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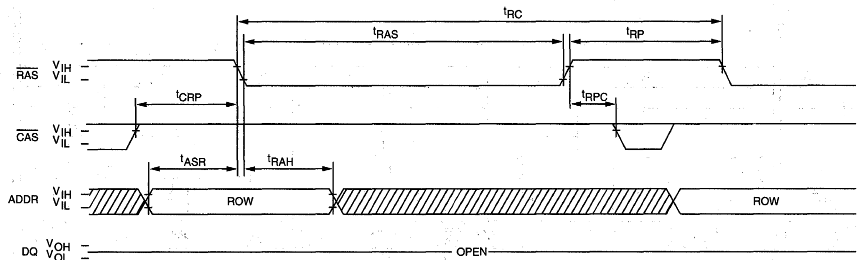
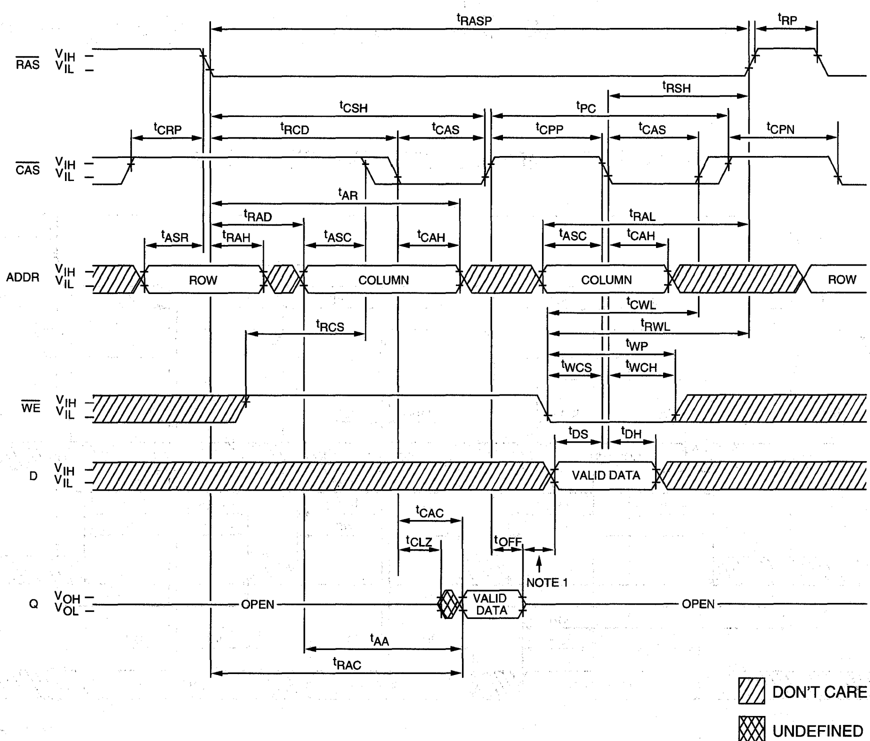
NEW DRAM CARD

RAS ONLY REFRESH CYCLE
(ADDRESS; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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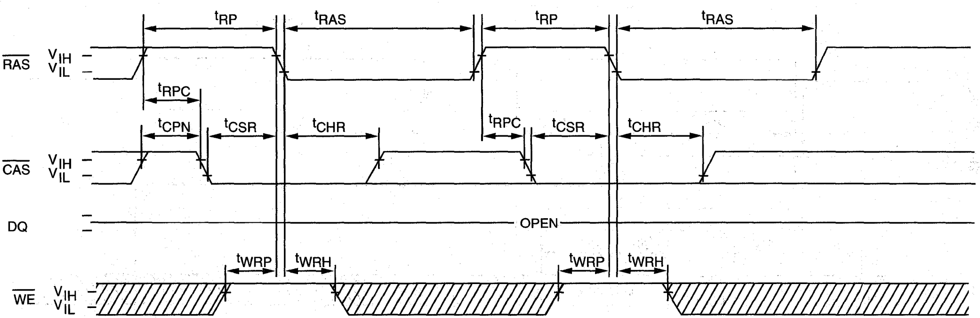
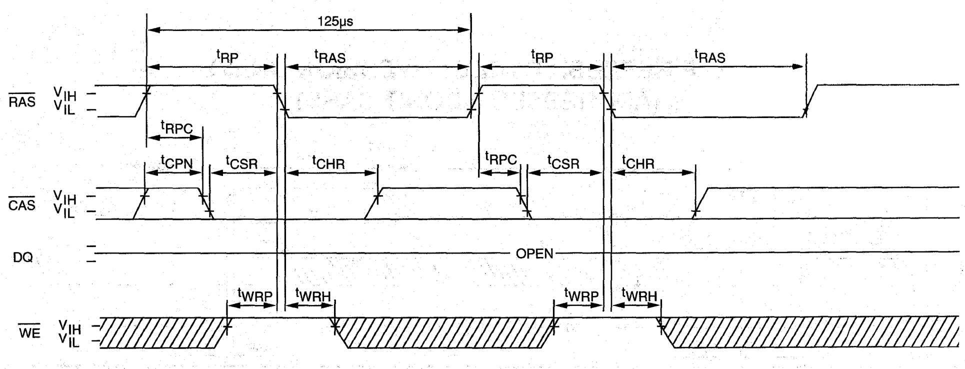
CBR REFRESH CYCLE
(ADDRESS = DON'T CARE)



EXTENDED CBR REFRESH CYCLE
(ADDRESS = DON'T CARE)



DON'T CARE

UNDEFINED

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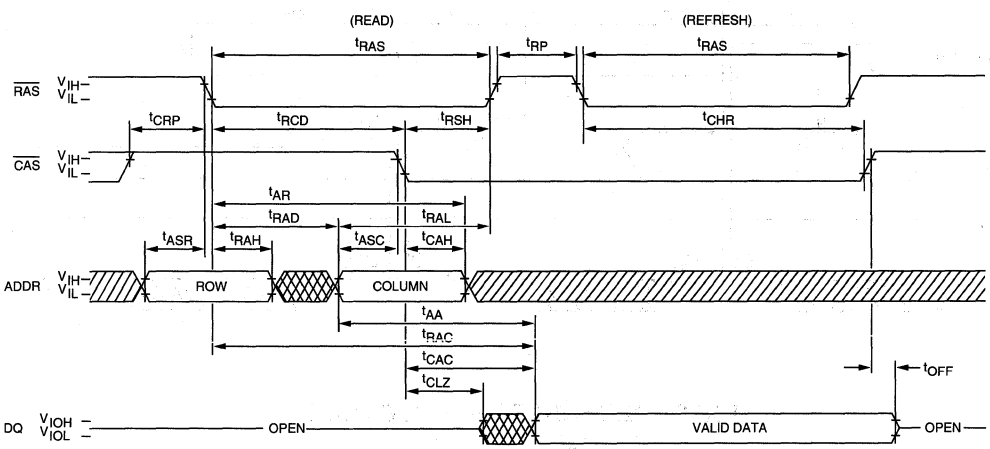
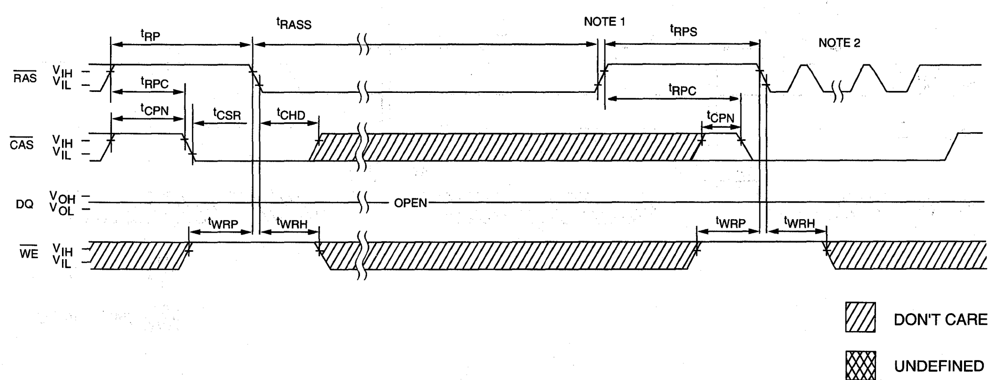
HIDDEN REFRESH CYCLE [21]
(WE = HIGH)



SELF REFRESH CYCLE (S-VERSION ONLY)
(ADDRESSES = DON'T CARE)



NOTE:
1. Once tRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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DRAM CARD

4, 8,16, 32 MEGABYTES

1 MEG, 2 MEG, 4 MEG, 8 MEG x 32;
3.3V FAST PAGE MODE,
OPTIONAL SELF REFRESH

FEATURES

- JEDEC-standard 88-pin DRAM card
- Polarized receptacle connector
- Industry-standard DRAM FAST PAGE MODE operation
- High reliability, gold-plated connector
- All outputs fully TTL-compatible
- All inputs buffered except RAS inputs
- Multiple RAS inputs for x16 or x32 selectability
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN; optional SELF REFRESH mode
- FAST PAGE MODE access cycle
- Single +3.3V ±0.3V power supply
- Low power
- Extended Refresh

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Refresh
  - Extended Refresh — Blank
  - SELF REFRESH — S
- Part Number Example: MT8D88C432V-7 S

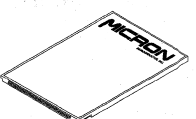
GENERAL DESCRIPTION

The MT8D88C132V/432V(S) and MT16D88C232V/832V(S) comprise a family of JEDEC-standard DRAM cards organized in x32-bit memory arrays. The cards may also be configured as x16-bit memory arrays, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented. Four separate CAS inputs allow byte accesses.

These 3.3V cards are designed for low-power operation using 3.3V, low-power, extended refresh DRAMs. Standard component DRAM refresh modes are supported as well.

Multiple RAS inputs conserve power by allowing individual bank selection. In the x32 organization, the memory is a single array that may be divided into four separate bytes. In the x16 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each RAS selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View)
88-Pin Card (DF-3)



44 ... 1
88 ... 45

PIN #	4MB	8MB	16MB	32MB	PIN #	4MB	8MB	16MB	32MB
1	Vss	→	→	→	45	Vss	→	→	→
2	DQ0	→	→	→	46	DQ16	→	→	→
3	DQ1	→	→	→	47	DQ17	→	→	→
4	DQ2	→	→	→	48	DQ18	→	→	→
5	DQ3	→	→	→	49	DQ19	→	→	→
6	DQ4	→	→	→	50	DQ20	→	→	→
7	DQ5	→	→	→	51	DQ21	→	→	→
8	DQ6	→	→	→	52	DQ22	→	→	→
9	NC	→	→	→	53	DQ23	→	→	→
10	DQ7	→	→	→	54	NC	→	→	→
11	3.3V Vcc	→	→	→	55	NC	→	→	→
12	NC	→	→	→	56	Vss	→	→	→
13	A0	→	→	→	57	A1	→	→	→
14	A2	→	→	→	58	A3	→	→	→
15	NC	→	→	→	59	A5	→	→	→
16	A4	→	→	→	60	A7	→	→	→
17	3.3V Vcc	→	→	→	61	A9	→	→	→
18	A6	→	→	→	62	NC	→	→	→
19	A8	→	→	→	63	Vss	→	→	→
20	NC	→	A10	→	64	NC	→	→	→
21	NC	→	→	→	65	NC	RAS1	NC	RAS1
22	RAS0	→	→	→	66	CAS2	→	→	→
23	CAS0	→	→	→	67	Vss	→	→	→
24	CAS1	→	→	→	68	CAS3	→	→	→
25	3.3V Vcc	→	→	→	69	NC	RAS3	NC	RAS3
26	RAS2	→	→	→	70	WE	→	→	→
27	NC	→	→	→	71	PD1	→	→	→
28	PD2	→	→	→	72	PD3	→	→	→
29	PD4	→	→	→	73	Vss	→	→	→
30	PD6	→	→	→	74	PD5	→	→	→
31	NC	→	→	→	75	PD7	→	→	→
32	NC	→	→	→	76	PD8	→	→	→
33	NC	→	→	→	77	NC	→	→	→
34	DQ8	→	→	→	78	NC	→	→	→
35	3.3V Vcc	→	→	→	79	NC	→	→	→
36	DQ9	→	→	→	80	DQ24	→	→	→
37	NC	→	→	→	81	DQ25	→	→	→
38	DQ10	→	→	→	82	DQ26	→	→	→
39	DQ11	→	→	→	83	DQ27	→	→	→
40	DQ12	→	→	→	84	DQ28	→	→	→
41	DQ13	→	→	→	85	DQ29	→	→	→
42	DQ14	→	→	→	86	DQ30	→	→	→
43	DQ15	→	→	→	87	DQ31	→	→	→
44	Vss	→	→	→	88	Vss	→	→	→

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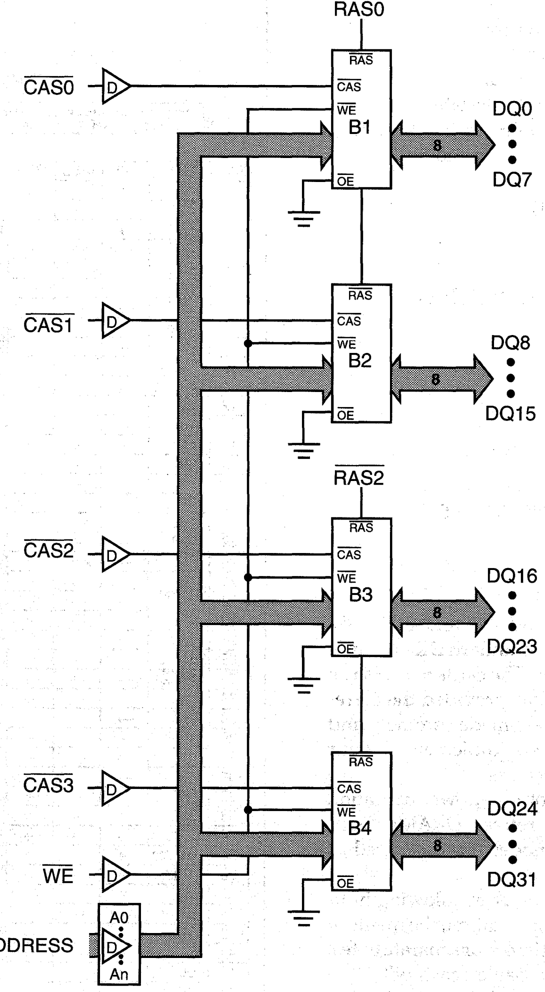
Eight presence-detect pins may be read by the host to identify the card's organization, number of banks, access time and refresh operation. These extensive presence-detect functions allow systems to take full advantage of the advanced power-saving features.

These Micron DRAM cards are built with 3.370-inch-long static dissipative plastic frames covered by metal panels. Packages containing 88-pin receptacle connectors are keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM
(4MB - MT8D88C132V, 16MB - MT8D88C432V)



NOTE: 1. B1 through B4 = x8 memory blocks.
2. D = 74AC11244 line drivers.

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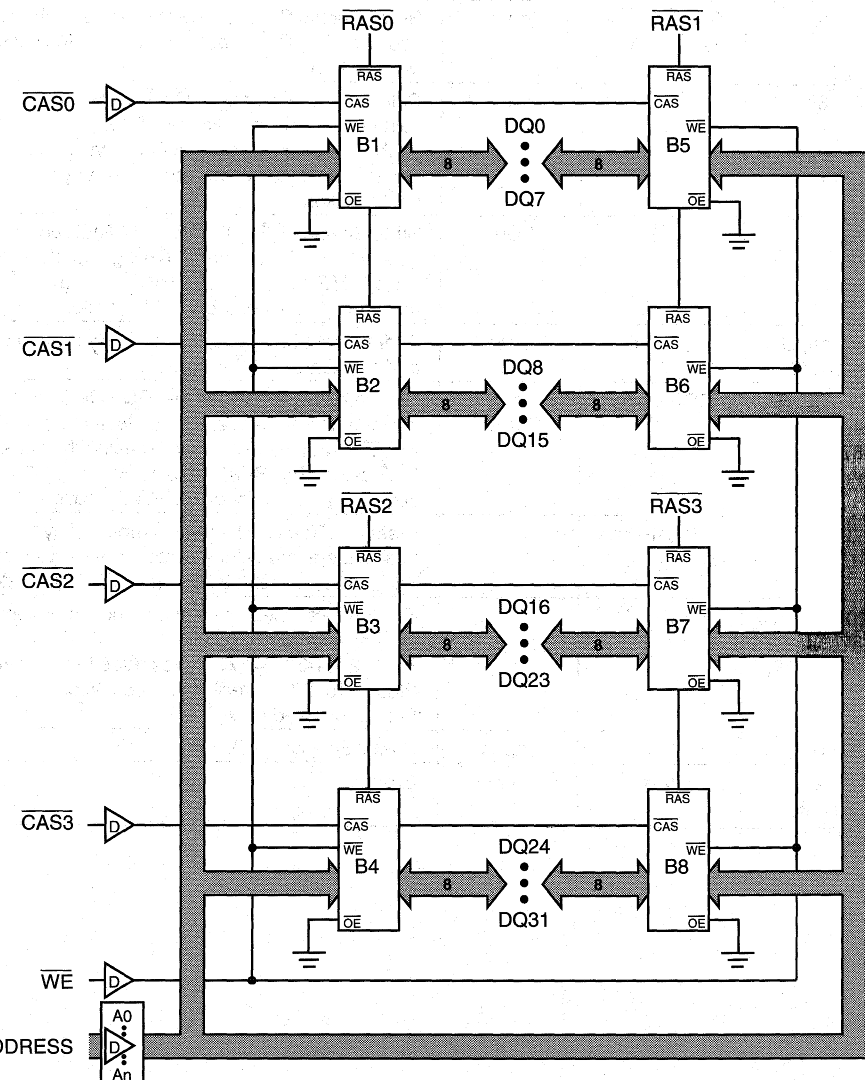
FUNCTIONAL BLOCK DIAGRAM
(8MB - MT16D88C232V, 32MB - MT16D88C832V)



NOTE: 1. B1 through B8 = x8 memory blocks.
2. D = 74AC11244 line drivers.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	$\overline{RAS0}$, $\overline{RAS2}$ $\overline{RAS1}$, $\overline{RAS3}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch the row-address. Two $\overline{RAS}$ inputs allow for a single x32 bank or two x16 banks.
23, 24, 66, 68	$\overline{CAS0\text{-}CAS3}$	Input	Column-Address Strobe: $\overline{CAS}$ is used to latch the column-address, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is a WRITE cycle. If $\overline{WE}$ is HIGH during the $\overline{CAS}$ LOW transition, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61, 20	A0-A10	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ31	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ31 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ31 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or grounded (Vss).
9, 12, 15, 20, 21, 27, 31, 32, 33, 37, 54, 55, 62, 64, 65, 69, 77, 78, 79	NC	-	No Connect: These pins should be left unconnected (reserved for future use). Pins 12, 31-33, 54, 77-79 reserved for x36/x40 DQs. PIns 9, 15, 27, 37 reserved for 5V Vcc. Pin 55 reserved for x40 $\overline{OE}$.
11, 17, 25, 35	Vcc	Supply	Power Supply: +3.3V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

NEW DRAM CARD

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FUNCTIONAL DESCRIPTION

The MT8D88C132V/432V(S) and MT16D88C232V/832V(S) comprise a family of DRAM cards organized in x32-bit memory arrays ($\overline{RAS0}$ = $\overline{RAS2}$). They also may be configured as x16-bit memory arrays provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both $\overline{RAS}$ lines.

Most x32-bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ and $\overline{RAS1}$ control the lower 16 bits and $\overline{RAS2}$ and $\overline{RAS3}$ control the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQ and $\overline{CAS}$ pins must be connected (DQ0 to DQ15, DQ1 to DQ16 and so forth, $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the x16 memory organizations.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, extended CBR or HIDDEN) so that all combinations of $\overline{RAS}$ addresses (A0-A9/A10) are executed at least every tREF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

The implied method of choice for refreshing the memory card is the extended CBR cycle. This is a very low-current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common to standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the extended CBR REFRESH cycle. However, the memory card will draw more current in the standby mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20/22 address bits, which are entered 10/11 bits (A0-A9/A10) at a time. $\overline{RAS}$ is used to latch the first 10/11 bits, and $\overline{CAS}$ latches the latter 10/11 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE). The data inputs and data outputs are routed through pins using common I/O and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row-address-defined (A0-A9/A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time.

REFRESH

An optional SELF REFRESH mode is also available. The "S" option allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified ^{t}RASS. Additionally, the "S" option allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of ^{t}RPS (≈^{t}RC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or BURST REFRESH sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

PHYSICAL DESIGN

These Micron 3.3V DRAM cards are constructed with a 3.370-inch long static dissipative plastic frame covered by metal panels. Inside, thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high-insertion, 88-pin receptacle connector. The package is keyed to prevent improper installation, including insertion into other types of IC card sockets. The DRAM cards operate reliably up to 55°C.

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MEMORY TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDRESSES ${}^tR$	ADDRESSES ${}^tC$	DATA IN/OUT DQ0-DQ31
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
READ WRITE		L	L	H→L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Data-Out
$\overline{\text{RAS}}$ ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH (S-version only)		H→L	L	H	X	X	High-Z

PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS						PRESENCE-DETECT PIN (PDx)							
Card Density	DRAM Organizations	# of Address	$\overline{\text{RAS}}$ Address	$\overline{\text{CAS}}$ Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC			
1MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	NC			
2MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	Vss			
2MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	NC			
4MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	Vss			
•4MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	NC			
•8MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	Vss			
8MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	NC			
16MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	Vss			
•16MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	NC			
•32MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	Vss			
Access Timing ${}^tRAC$ Max		100ns									Vss	Vss	
		80ns									NC	Vss	
		70ns									Vss	NC	
		60ns									NC	NC	
		50ns									Vss	Vss	
Refresh Control		Extended											NC
		SELF, Extended											Vss

NOTE: Vss = ground.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1.0V to +4.5V
Operating Temperature T_A (ambient) .... 0°C to 55°C
Storage Temperature .... -40°C to +70°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Card Insertions (connector's life cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; Vcc = 3.3V ± 5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	3.15	3.45	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.1	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input: 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V) for each package input	$\overline{RAS0}$-$\overline{RAS3}$	II1	-8	8	µA	
	Buffered	II2	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ VOUT ≤ Vcc) for each package input	DQ0-DQ31	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2.0 mA)		VOH	2.0		V	
Output Low Voltage (IOUT = 2.0 mA)		VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; Vcc = 3.3V ± 5%)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX			UNITS	NOTES
			-6	-7	-8		
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC1}	4MB 8MB 16MB 32MB	640 648 960 968	560 568 880 888	480 488 - -	mA	3, 4, 31
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	4MB 8MB 16MB 32MB	8 16 8 16	8 16 8 16	8 16 - -	mA	
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC3}	4MB 8MB 16MB 32MB	480 488 720 728	400 408 640 648	320 328 - -	mA	3, 4, 31
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = Vcc -0.2V)	I_{CC4}	4MB 8MB 16MB 32MB	4 8 4 8	4 8 4 8	4 8 - -	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	4MB 8MB 16MB 32MB	640 648 960 968	560 568 880 888	480 488 - -	mA	3, 31
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	4MB 8MB 16MB 32MB	640 648 960 968	560 568 880 888	480 488 - -	mA	3, 5
REFRESH CURRENT: Extended CBR Average power supply current during extended CBR: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); ^tRC = 125µs; $\overline{WE}$, A0-A10 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	I_{CC7}	4MB 8MB 16MB 32MB	1.2 2.4 2.4 4.8	1.2 2.4 2.4 4.8	1.2 2.4 2.4 4.8	mA	3, 5
REFRESH CURRENT: SELF (S-version only) Average power supply current, CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc-0.2V; A0-A11 and D_{IN} = Vcc - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	4MB 8MB 16MB 32MB	1.2 2.4 2.4 4.8	1.2 2.4 2.4 4.8	1.2 2.4 2.4 4.8	mA	5, 32

CAPACITANCE

PARAMETER	SYMBOL	MAX		UNITS	NOTES
		4,16MB	8, 32MB		
Input Capacitance: $\overline{CAS0-CAS3}$	C_{I1}	9	9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}	13	13	pF	2
Input Capacitance: $\overline{RAS0-RAS3}$	C_{I3}	34	34	pF	2
Input/Output Capacitance: DQ0-DQ31	C_{IO}	10	18	pF	2
Input Capacitance: Addresses	C_{I3}	9	9	pF	2

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 3.3V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	23
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	^tCAC		26		31		31	ns	15, 26
Access time from column-address	^tAA		41		46		51	ns	26
Access time from $\overline{CAS}$ precharge	^tCPA		46		51		56	ns	26
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	^tRSH	26		31		31		ns	26
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	23
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	^tCSH	58		68		78		ns	25
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	18	34	18	39	18	49	ns	17, 27
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	21		21		21		ns	26
Row-address setup time	^tASR	11		11		11		ns	26
Row-address hold time	^tRAH	8		8		8		ns	25
$\overline{RAS}$ to column-address delay time	^tRAD	13	19	13	24	13	29	ns	18, 27
Column-address setup time	^tASC	2		2		2		ns	24
Column-address hold time	^tCAH	10		15		15		ns	23
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	48		53		53		ns	25
Column-address to $\overline{RAS}$ lead time	^tRAL	41		46		51		ns	26
Read command setup time	^tRCS	2		2		2		ns	24
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	2		2		2		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		5		ns	24, 33
Output buffer turn-off delay	^tOFF	5	26	5	31	5	31	ns	20, 28, 33
$\overline{WE}$ command setup time	^tWCS	2		2		2		ns	24

NEW DRAM CARD

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NEW DRAM CARD

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 3.3V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	^tWCH	10		15		15		ns	23
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	43		53		58		ns	25
Write command pulse width	^tWP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	^tRWL	26		31		31		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	26		31		31		ns	23
Data-in setup time	^tDS	2		2		2		ns	24
Data-in hold time	^tDH	21		26		26		ns	26
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	23
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10, 23
Refresh period (1,024 cycles)	^tREF		128		128		128	ms	35
Refresh period (2,048 cycles)	^tREF		128		128		128	ms	34
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	23
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	12		12		12		ns	5, 24
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	13		13		13		ns	5, 25
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	8		8		8		ns	22, 25
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	12		12		12		ns	22, 24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	8		8		8		ns	22, 25
$\overline{WE}$ setup time	^tWTS	12		12		12		ns	22, 24
$\overline{RAS}$ pulse width entering SELF REFRESH	^tRASS	100		100		100		µs	23, 32
$\overline{RAS}$ precharge time exiting SELF REFRESH	^tRPS	110		130		150		ns	23, 32
$\overline{CAS}$ hold time entering SELF REFRESH	^tCHD	13		13		13		ns	23, 32

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 3.3V ±10%; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {^tRCD}$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {^tRCD}$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^tWRP and ^tWRH in the CBR REFRESH cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +2ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -2ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +11ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -2ns (MIN) and a -11ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A +2ns (MIN) and a +11ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. The maximum current ratings are based on the memory operating or being refreshed in the x32 mode. The stated maximums may be reduced by one-half when used in the x16 mode.
30. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
31. Column-address changed once each cycle.
32. If the DRAM controller uses a BURST REFRESH, a BURST REFRESH of all rows must be executed upon exiting SELF REFRESH.
33. The 3ns minimum is a parameter guaranteed by design.
34. 16MB and 32MB only.
35. 4MB and 8MB only.

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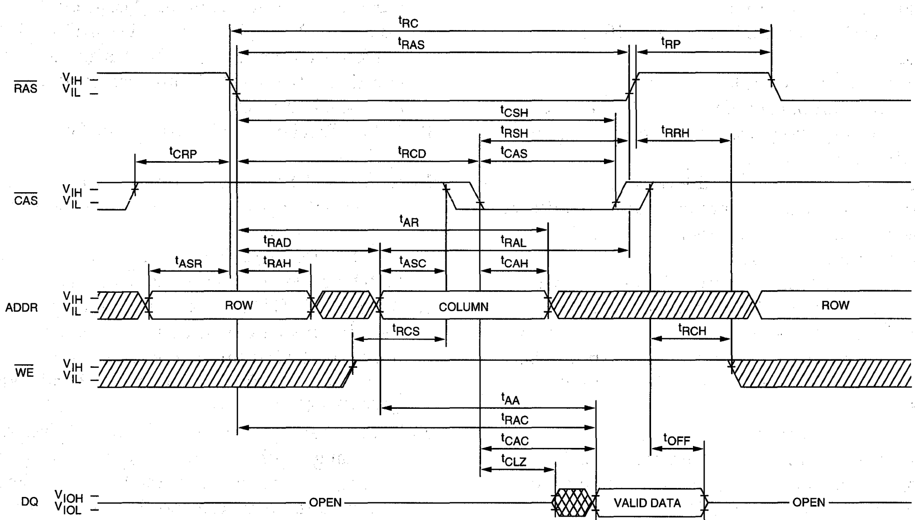
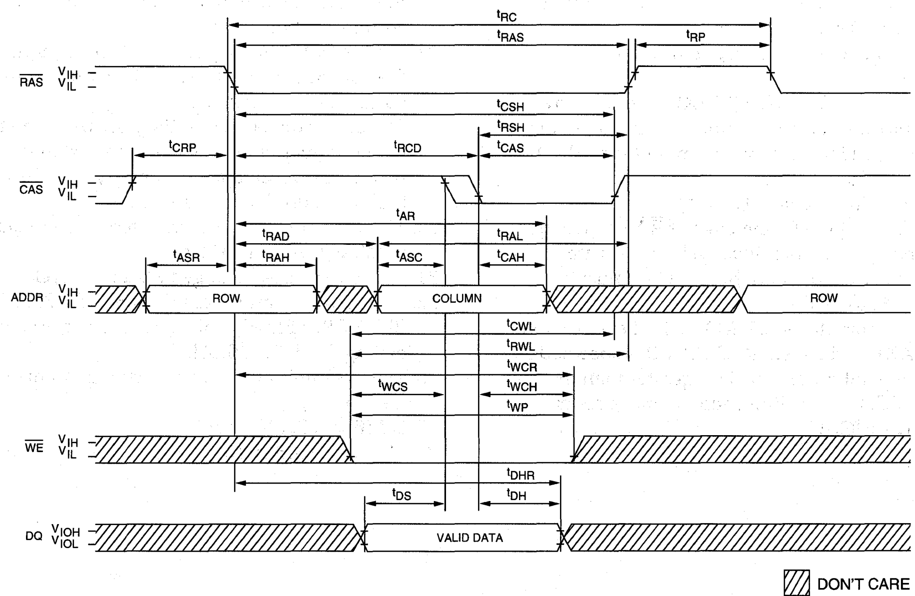
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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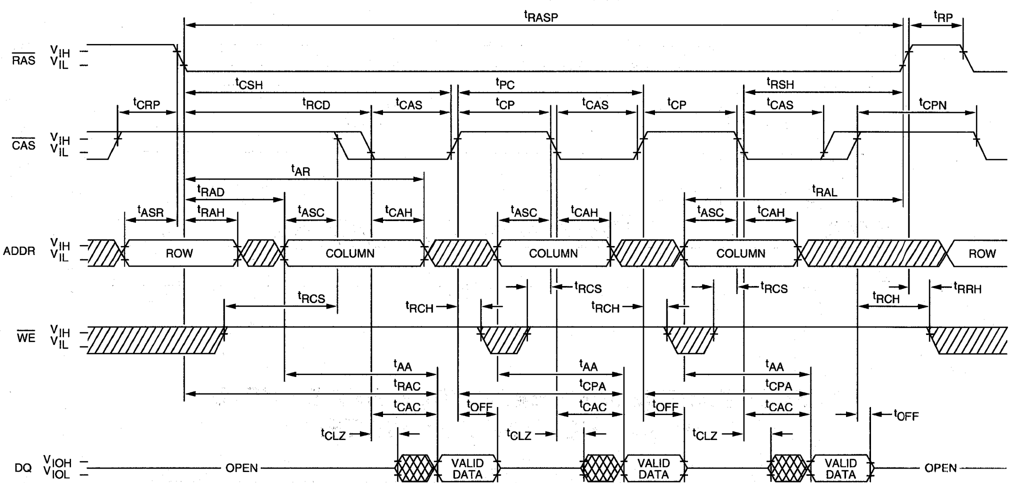
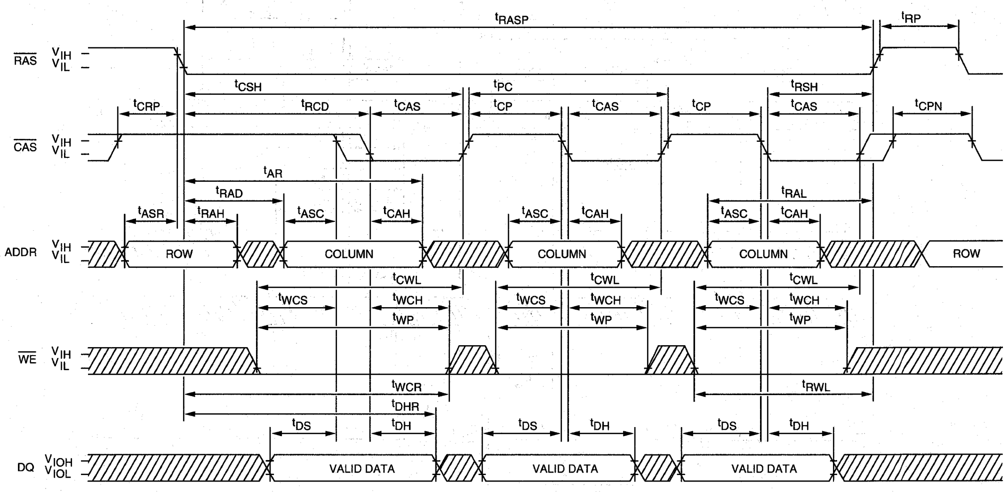
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

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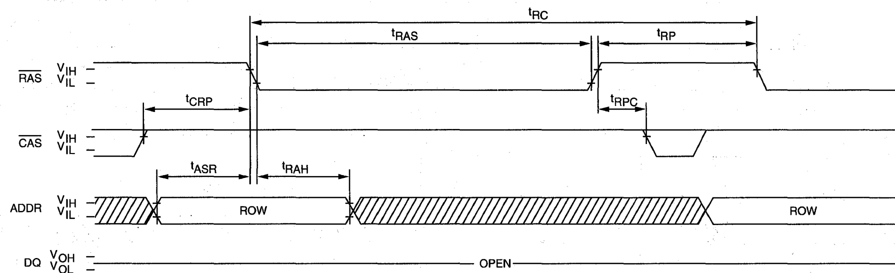
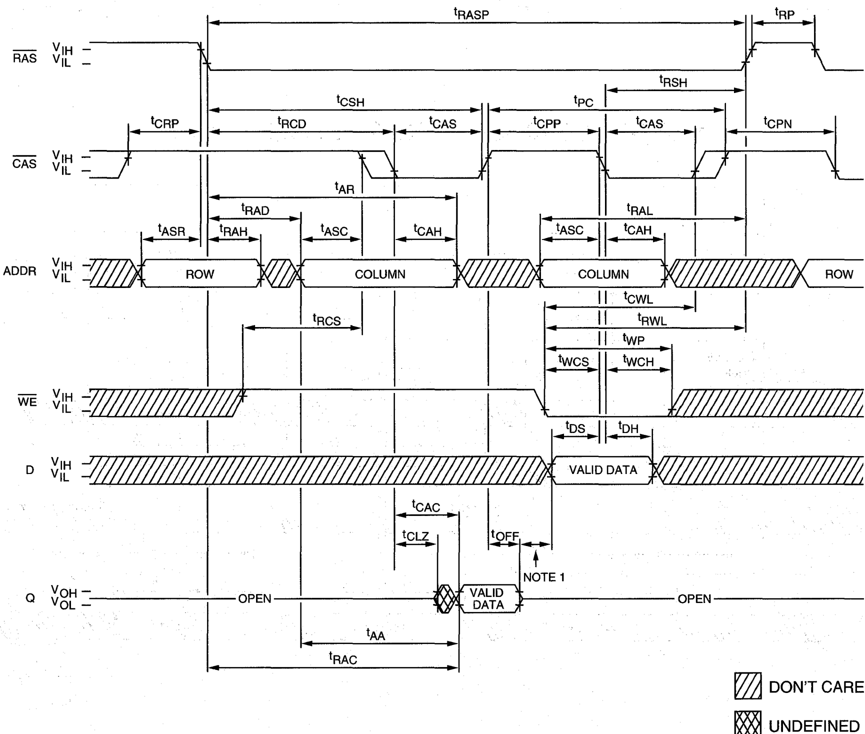
RAS ONLY REFRESH CYCLE
(ADDRESS; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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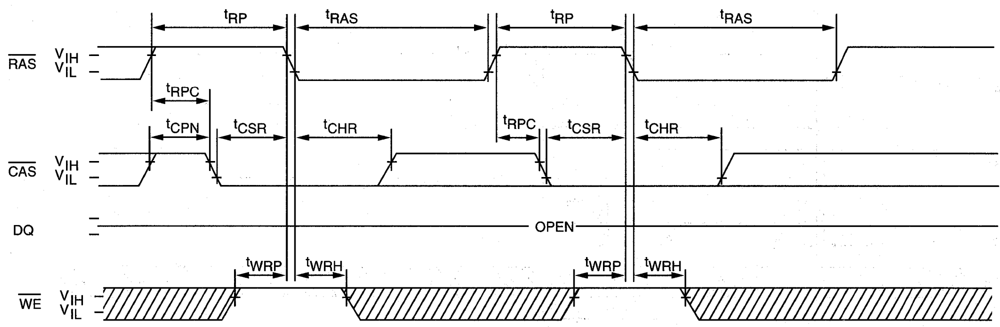
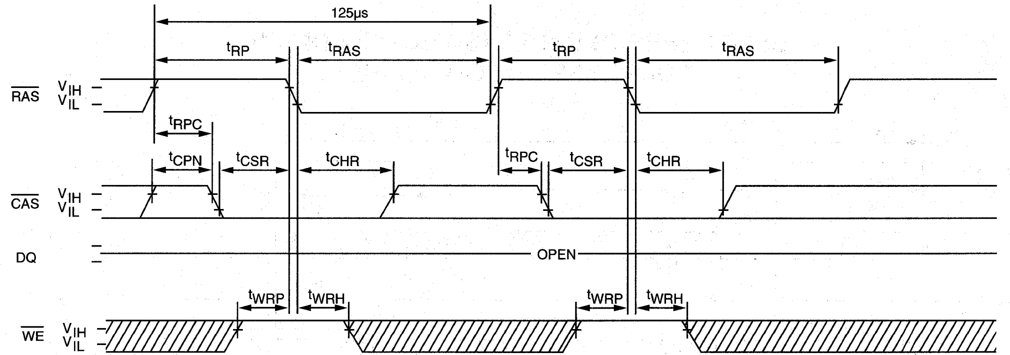
CBR REFRESH CYCLE
(ADDRESS = DON'T CARE)



EXTENDED CBR REFRESH CYCLE
(ADDRESS = DON'T CARE)



DON'T CARE

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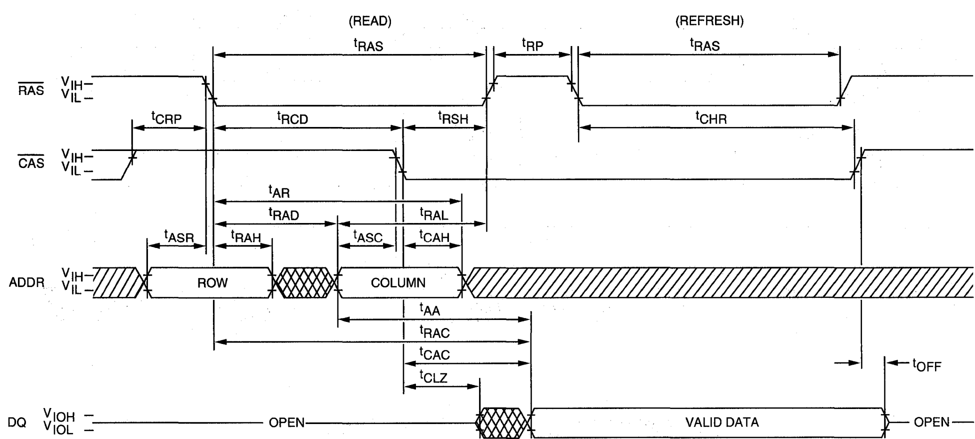
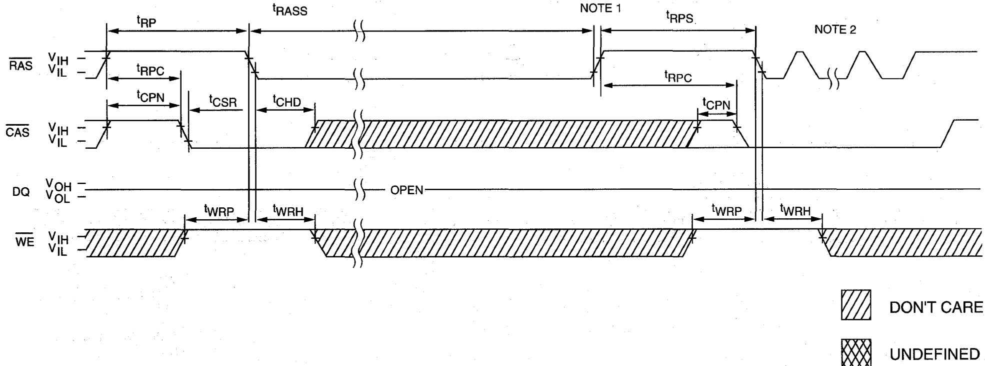
HIDDEN REFRESH CYCLE [21]
(WE = HIGH)



SELF REFRESH CYCLE (S-VERSION ONLY)
(ADDRESSES = DON'T CARE)



DON'T CARE

UNDEFINED

NOTE: 1. Once tRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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DRAM MINICARD

4, 8, 16, 32 MEGABYTES

1 MEG, 2 MEG, 4 MEG, 8 MEG x 32;
3.3V FAST PAGE MODE,
OPTIONAL SELF REFRESH

FEATURES

- JEDEC-standard 88-pin DRAM card pinout
- 2-inch (50.8mm)-long nonbuffered DRAM cards
- Polarized receptacle connector
- Industry-standard DRAM FAST PAGE MODE operation
- High reliability, gold-plated connector
- All outputs fully TTL-compatible
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional SELF REFRESH
- FAST PAGE MODE access cycle
- Single +3.3V ±5% power supply
- Low power
- Extended Refresh

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Refresh	
Extended Refresh	Blank
SELF REFRESH	S

- Part Number Example: MT8D88C432VH-7 S

GENERAL DESCRIPTION

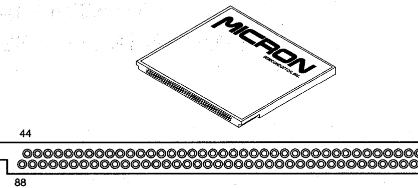
The MT8D88C132VH/432VH(S), MT16D88C232VH/832VH(S) comprise a family of DRAM cards organized in x32-bit memory arrays. These DRAM cards are 2-inch-long bufferless versions of the JEDEC-standard 3.37-inch (85.6mm), 88-pin x32 DRAM cards. Buffers are not included on these cards, so the on-board timing delays have been eliminated. Redrive circuitry may be implemented on the system board.

The cards may also be configured as x16-bit memory arrays, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented. Four separate $\overline{CAS}$ inputs allow byte accesses.

These 3.3V MiniCards are designed for low-power operation using 3.3V, low-power, extended refresh DRAMs. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32 organization, the memory

PIN ASSIGNMENT (End View)
88-Pin Card (DF-2)



44 — 1
88 — 45

PIN #	4MB	8MB	16MB	32MB	PIN #	4MB	8MB	16MB	32MB
1	Vss	→	→	→	45	Vss	→	→	→
2	DQ0	→	→	→	46	DQ16	→	→	→
3	DQ1	→	→	→	47	DQ17	→	→	→
4	DQ2	→	→	→	48	DQ18	→	→	→
5	DQ3	→	→	→	49	DQ19	→	→	→
6	DQ4	→	→	→	50	DQ20	→	→	→
7	DQ5	→	→	→	51	DQ21	→	→	→
8	DQ6	→	→	→	52	DQ22	→	→	→
9	NC	→	→	→	53	DQ23	→	→	→
10	DQ7	→	→	→	54	NC	→	→	→
11	3.3V Vcc	→	→	→	55	NC	→	→	→
12	NC	→	→	→	56	Vss	→	→	→
13	A0	→	→	→	57	A1	→	→	→
14	A2	→	→	→	58	A3	→	→	→
15	NC	→	→	→	59	A5	→	→	→
16	A4	→	→	→	60	A7	→	→	→
17	3.3V Vcc	→	→	→	61	A9	→	→	→
18	A6	→	→	→	62	NC	→	→	→
19	A8	→	→	→	63	Vss	→	→	→
20	NC	→	A10	→	64	NC	→	→	→
21	NC	→	→	→	65	NC	$\overline{RAS1}$	NC	$\overline{RAS1}$
22	$\overline{RAS0}$	→	→	→	66	$\overline{CAS2}$	→	→	→
23	$\overline{CAS0}$	→	→	→	67	Vss	→	→	→
24	$\overline{CAS1}$	→	→	→	68	$\overline{CAS3}$	→	→	→
25	3.3V Vcc	→	→	→	69	NC	$\overline{RAS3}$	NC	$\overline{RAS3}$
26	$\overline{RAS2}$	→	→	→	70	$\overline{WE}$	→	→	→
27	NC	→	→	→	71	PD1	→	→	→
28	PD2	→	→	→	72	PD3	→	→	→
29	PD4	→	→	→	73	Vss	→	→	→
30	PD6	→	→	→	74	PD5	→	→	→
31	NC	→	→	→	75	PD7	→	→	→
32	NC	→	→	→	76	PD8	→	→	→
33	NC	→	→	→	77	NC	→	→	→
34	DQ8	→	→	→	78	NC	→	→	→
35	3.3V Vcc	→	→	→	79	NC	→	→	→
36	DQ9	→	→	→	80	DQ24	→	→	→
37	NC	→	→	→	81	DQ25	→	→	→
38	DQ10	→	→	→	82	DQ26	→	→	→
39	DQ11	→	→	→	83	DQ27	→	→	→
40	DQ12	→	→	→	84	DQ28	→	→	→
41	DQ13	→	→	→	85	DQ29	→	→	→
42	DQ14	→	→	→	86	DQ30	→	→	→
43	DQ15	→	→	→	87	DQ31	→	→	→
44	Vss	→	→	→	88	Vss	→	→	→

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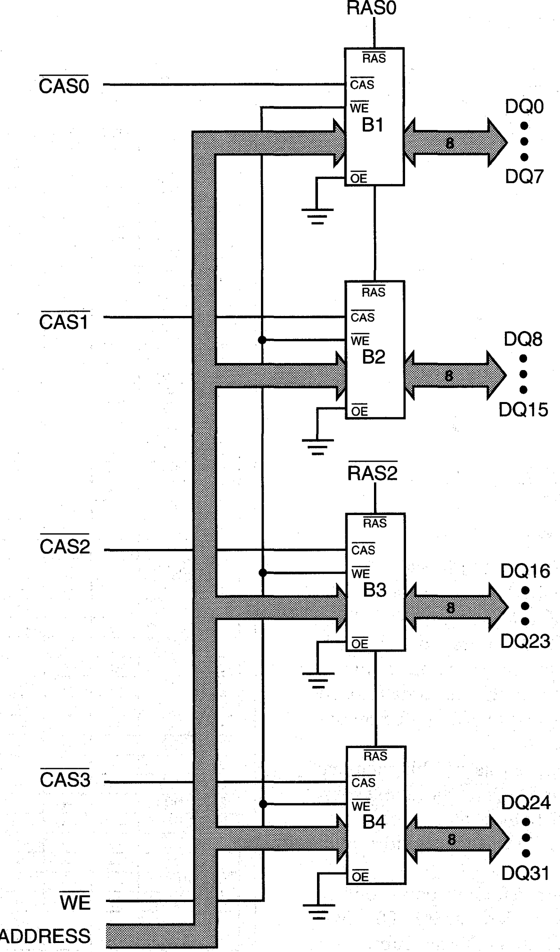
is a single array that may be divided into four separate bytes. In the x16 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each RAS selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence-detect pins may be read by the host to identify the card's organization, number of banks, access time and refresh operation. These extensive presence-detect functions allow systems to take full advantage of the advanced power-saving features.

These Micron DRAM cards are built with 3.370-inch-long static dissipative plastic frames covered by metal panels. Packages containing 88-pin receptacle connectors are keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM
(4MB - MT8D88C132VH, 16MB - MT8D88C432VH)



NOTE: 1. B1 through B4 = x8 memory blocks.

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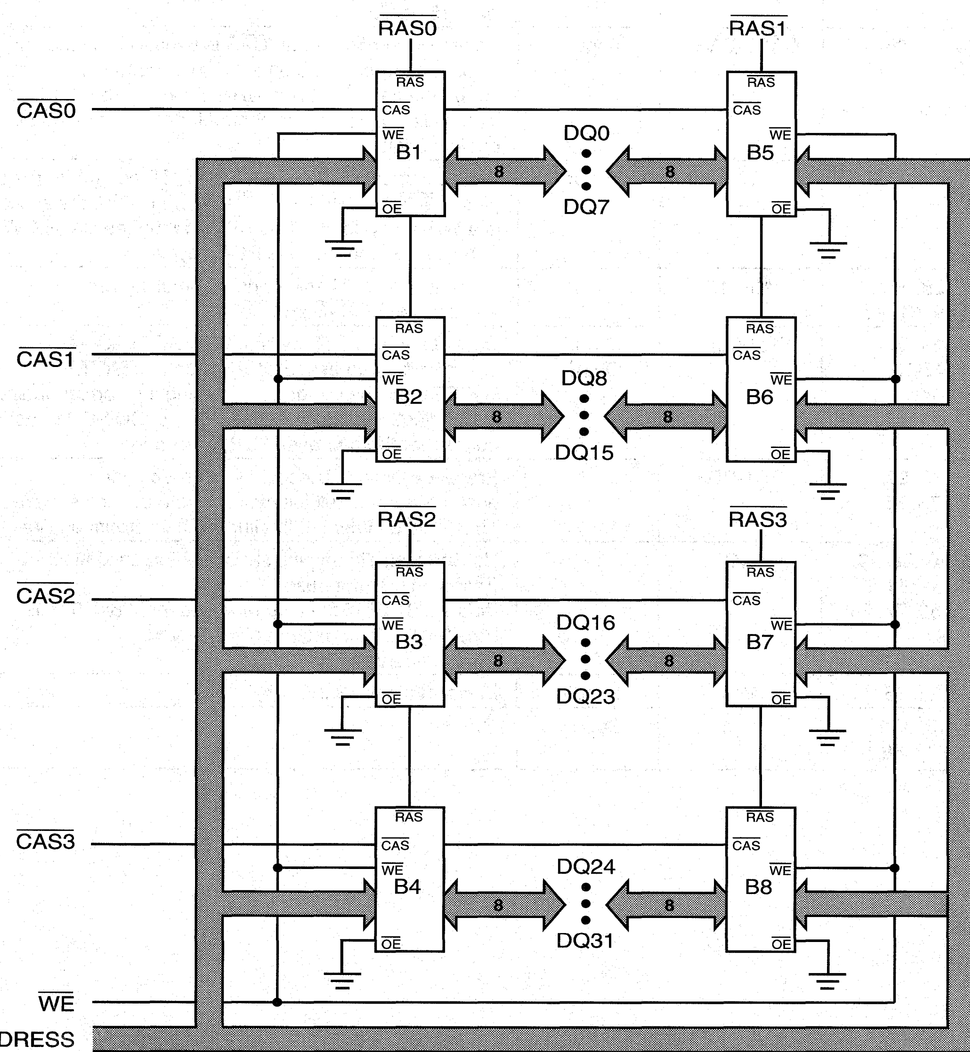
FUNCTIONAL BLOCK DIAGRAM
(8MB - MT16D88C232VH, 32MB - MT16D88C832VH)



NOTE: 1. B1 through B8 = x8 memory blocks.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	$\overline{RAS0}$, $\overline{RAS2}$ $\overline{RAS1}$, $\overline{RAS3}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch the row-address. Two $\overline{RAS}$ inputs allow for a single x32 bank or two x16 banks.
23, 24, 66, 68	$\overline{CAS0\text{-}CAS3}$	Input	Column-Address Strobe: $\overline{CAS}$ is used to latch the column-address, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is a WRITE cycle. If $\overline{WE}$ is HIGH during the $\overline{CAS}$ LOW transition, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61, 20	A0-A10	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ31	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ31 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ31 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or grounded (Vss).
9, 12, 15, 20, 21, 27, 31, 32, 33, 37, 54, 55, 62, 64, 65, 69, 77, 78 79	NC	-	No Connect: These pins should be left unconnected (reserved for future use). Pins 12, 31-33, 54, 77-79 reserved for x36/x40 DQs. PIns 9, 15, 27, 37 reserved for 5V Vcc. Pin 55 reserved for x40 $\overline{OE}$.
11, 17, 25, 35	Vcc	Supply	Power Supply: +3.3V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

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FUNCTIONAL DESCRIPTION

The MT8D88C132VH/432VH(S), MT16D88C232VH/832VH(S) comprise a family of DRAM cards organized in x32-bit memory arrays ($\overline{RAS0}$ = $\overline{RAS2}$). They also may be configured as x16-bit memory arrays provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both $\overline{RAS}$ lines.

Most x32-bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ and $\overline{RAS1}$ control the lower 16 bits and $\overline{RAS2}$ and $\overline{RAS3}$ control the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQ and $\overline{CAS}$ pins must be connected (DQ0 to DQ15, DQ1 to DQ16 and so forth, $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the x16 memory organizations.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, extended CBR or HIDDEN) so that all combinations of $\overline{RAS}$ addresses (A0-A9, A10) are executed at least every tREF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

The implied method of choice for refreshing the memory card is the extended CBR cycle. This is a very low-current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common to standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the extended CBR REFRESH cycle. However, the memory card will draw more current in the standby mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20/22 address bits, which are entered 10/11 bits (A0-A9/A10) at a time. $\overline{RAS}$ is used to latch the first 10/11 bits, and $\overline{CAS}$ latches the latter 10/11 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE). The data inputs and data outputs are routed through pins using common I/O and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row-address-defined (A0-A9/A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time.

REFRESH

An optional SELF REFRESH mode is also available. The "S" option allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified ${}^tRASS$. Additionally, the "S" option allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of ${}^tRPS$ ($\approx {}^tRC$). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or BURST REFRESH sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

PHYSICAL DESIGN

These Micron DRAM MiniCards are constructed with a 2-inch-long static dissipative plastic frame covered by metal panels. Inside, thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high-insertion, 88-pin receptacle connector. The package is keyed to prevent improper installation, including insertion into other types of IC card sockets. The DRAM cards operate reliably up to 55°C.

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MEMORY TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA IN/OUT DQ0-DQ31
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
READ WRITE		L	L	H→L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Data-Out
$\overline{\text{RAS}}$ ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH (S-version only)		H→L	L	H	X	X	High-Z

PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS						PRESENCE-DETECT PIN (PDx)							
Card Density	DRAM Organizations	# of Address	$\overline{\text{RAS}}$ Address	$\overline{\text{CAS}}$ Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC			
1MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	NC			
2MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	Vss			
2MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	NC			
4MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	Vss			
•4MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	NC			
•8MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	Vss			
8MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	NC			
16MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	Vss			
•16MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	NC			
•32MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	Vss			
Access Timing ^tRAC Max		100ns									Vss	Vss	
		80ns									NC	Vss	
		70ns									Vss	NC	
		60ns									NC	NC	
		50ns									Vss	Vss	
Refresh Control		Extended											NC
		SELF, Extended											Vss

NOTE: Vss = ground.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss........ -1.0V to +4.5V
Operating Temperature T_A (ambient) .... 0°C to 55°C
Storage Temperature .... -40°C to +70°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Card Insertions (connector's life cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; Vcc = 3.3V ± 5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	3.15	3.45	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{RAS0-RAS3}$	II1	-8	8	µA	
Any input: 0V ≤ VIN ≤ Vcc	A0-A10, $\overline{WE}$	II2	-10	10	µA	
(All other pins not under test = 0V) for each package input	$\overline{CAS0-CAS3}$	II3	-8	8	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ VOUT ≤ Vcc) for each package input	DQ0-DQ31	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2.0 mA)		VOH	2.0		V	
Output Low Voltage (IOUT = 2.0 mA)		VOL		0.4	V	

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NEW DRAM CARD

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; Vcc = 3.3V ± 5%)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ${}^tRC = {}^tRC$ [MIN])	Icc1	4MB	640	560	480	mA	3, 4, 31
		8MB	648	568	488		
		16MB	960	880	-		
		32MB	968	888	-		
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	Icc2	4MB	8	8	8	mA	
		8MB	16	16	16		
		16MB	8	8	-		
		32MB	16	16	-		
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ${}^tPC = {}^tPC$ [MIN])	Icc3	4MB	480	400	320	mA	3, 4, 31
		8MB	488	408	328		
		16MB	720	640	-		
		32MB	728	648	-		
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	Icc4	4MB	4	4	4	µA	
		8MB	8	8	8	µA	
		16MB	4	4	-	mA	
		32MB	8	8	-		
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: ${}^tRC = {}^tRC$ [MIN])	Icc5	4MB	640	560	480	mA	3, 31
		8MB	648	568	488		
		16MB	960	880	-		
		32MB	968	888	-		
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: ${}^tRC = {}^tRC$ [MIN])	Icc6	4MB	640	560	480	mA	3, 5
		8MB	648	568	488		
		16MB	960	880	-		
		32MB	968	888	-		
REFRESH CURRENT: Extended CBR Average power supply current during extended CBR: CAS = 0.2V or CBR cycling; RAS = ${}^tRAS$ (MIN); ${}^tRC$ = 125µs; WE, A0-A10 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	Icc7	4MB	1.2	1.2	1.2	mA	3, 5
		8MB	2.4	2.4	2.4		
		16MB	2.4	2.4	2.4		
		32MB	4.8	4.8	4.8		
REFRESH CURRENT: SELF (S-version only) Average power supply current, CBR cycling with RAS ≥ ${}^tRASS$ (MIN) and CAS held LOW; WE = Vcc-0.2V; A0-A11 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)	Icc8	4MB	1.2	1.2	1.2	mA	5, 32
		8MB	2.4	2.4	2.4		
		16MB	2.4	2.4	2.4		
		32MB	4.8	4.8	4.8		

CAPACITANCE

PARAMETER	SYMBOL	MAX 4,16MB	MAX 8, 32MB	UNITS	NOTES
Input Capacitance: CAS0-CAS3	CI1	17	34	pF	2
Input Capacitance: WE	CI2	66	66	pF	2
Input Capacitance: RAS0-RAS3	CI3	34	34	pF	2
Input/Output Capacitance: DQ0-DQ31	CIO	10	18	pF	2
Input Capacitance: Addresses	CI3	51	90	pF	2

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 3.3V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45		50	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	10		15		20		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	26
Output buffer turn-off delay	^tOFF	3	15	3	20	3	20	ns	20, 26
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	

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NEW DRAM CARD

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	24
Data-in hold time	^tDH	10		15		15		ns	24
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		128		128		128	ms	30
Refresh period (2,048 cycles)	^tREF		128		128		128	ms	29
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	22
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	22
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	22
$\overline{WE}$ setup time	^tWTS	10		10		10		ns	22
$\overline{RAS}$ pulse width entering SELF REFRESH	^tRASS	100		100		100		µs	28
$\overline{RAS}$ precharge time exiting SELF REFRESH	^tRPS	110		130		150		ns	28
$\overline{CAS}$ hold time entering SELF REFRESH	^tCHD	15		15		15		ns	28

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1. V_{CC} = 3.3V ±5%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
23. The maximum current ratings are based on the memory operating or being refreshed in the x32 mode. The stated maximums may be reduced by one-half when used in the x16 mode.
24. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
25. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being tied permanently LOW on all 4 Meg DRAMs.
26. The 3ns minimum is a parameter guaranteed by design.
27. Column-address changed once each cycle.
28. If the DRAM controller uses a BURST REFRESH, a BURST REFRESH of all rows must be executed upon exiting SELF REFRESH.
29. 16MB and 32MB versions only.
30. 4MB and 8MB versions only.

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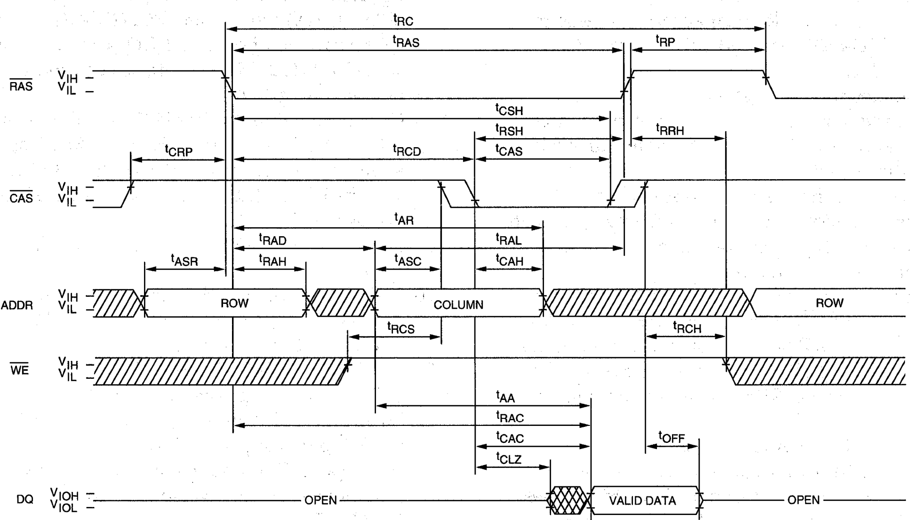
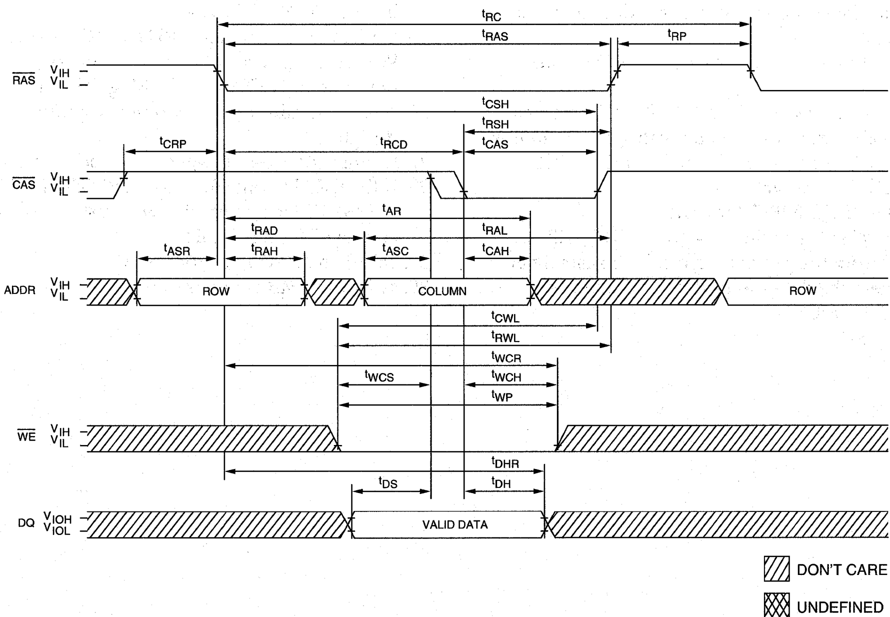
NEW DRAM CARD

READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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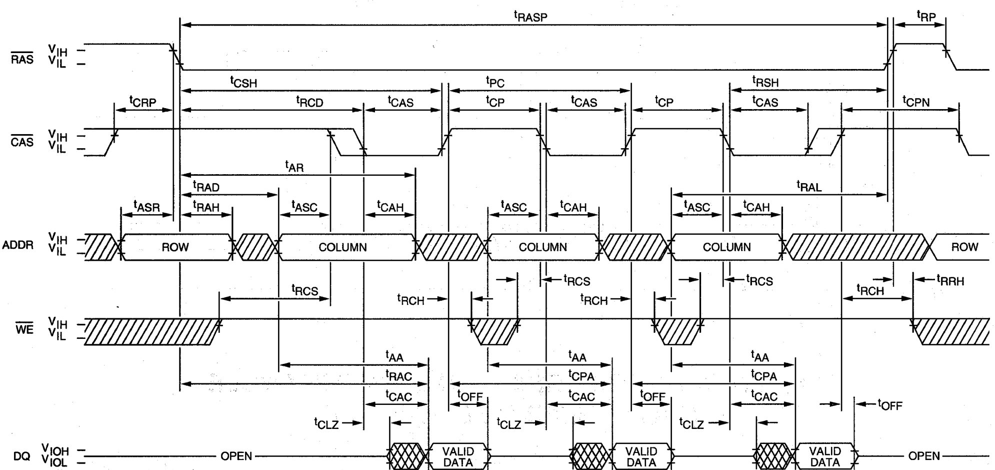
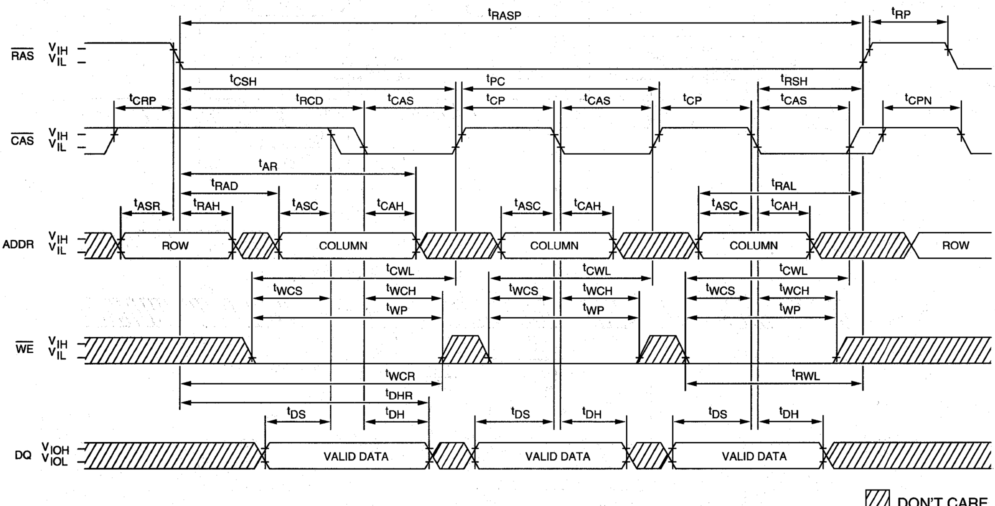
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

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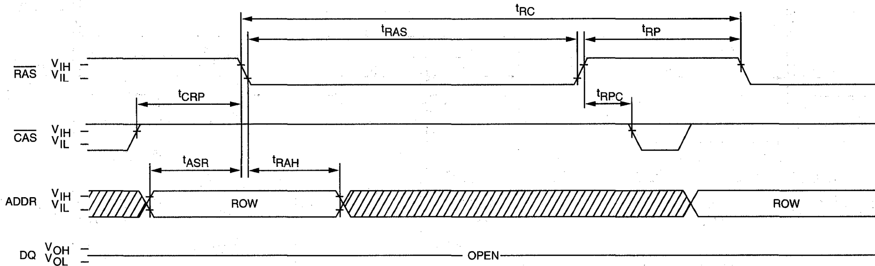
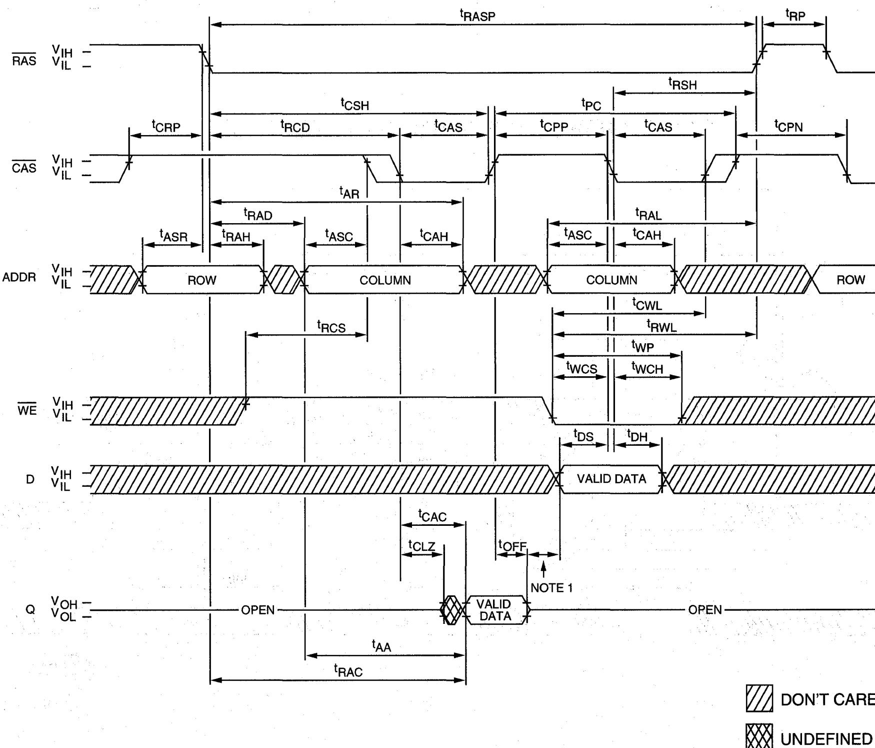
NEW DRAM CARD

RAS ONLY REFRESH CYCLE
(ADDRESS; WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: ^{t}CPP(MIN) or ^{t}CP(whichever is greater) + ^{t}DS(MIN) + any guardband between data-out and driving the bus with the new data-in.

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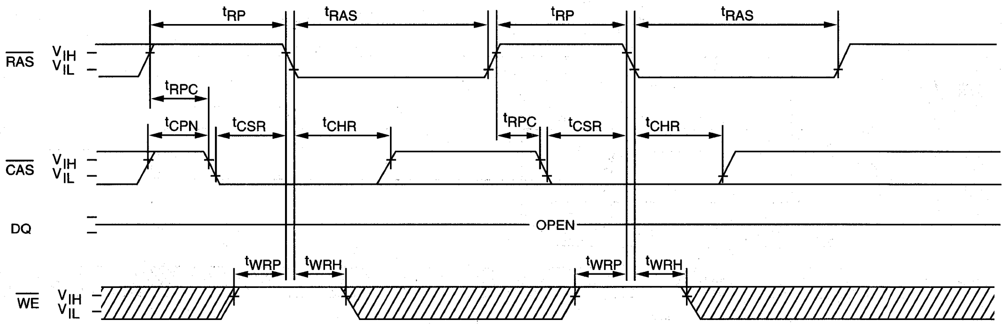
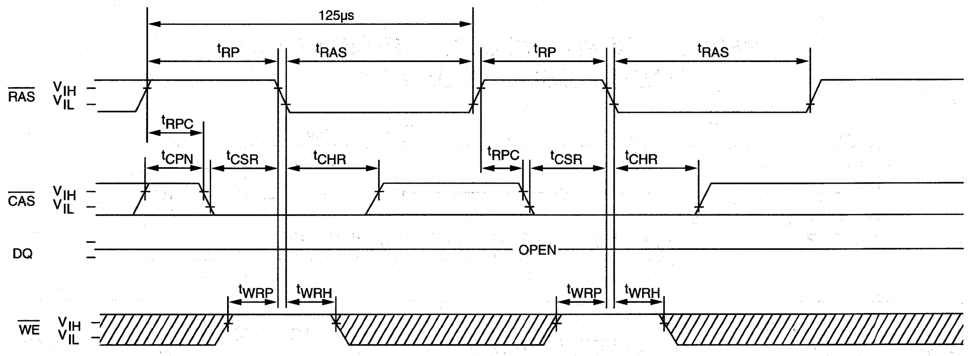
CBR REFRESH CYCLE
(ADDRESS = DON'T CARE)



EXTENDED CBR REFRESH CYCLE
(ADDRESS = DON'T CARE)



DON'T CARE

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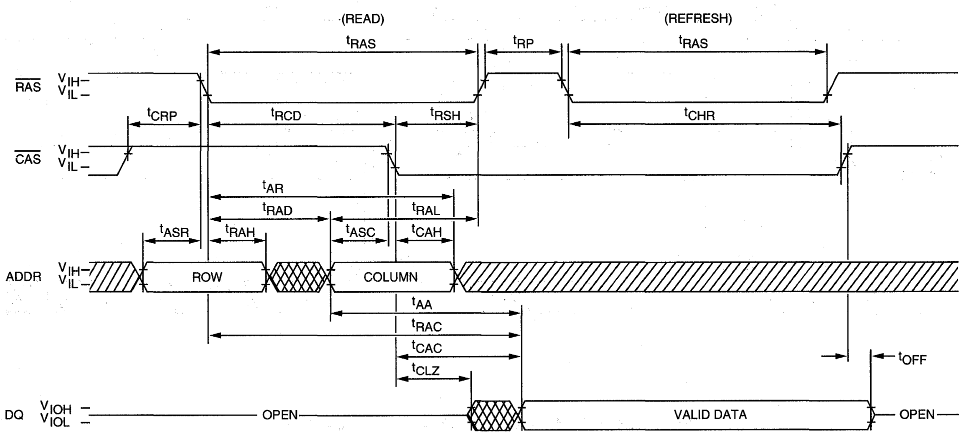
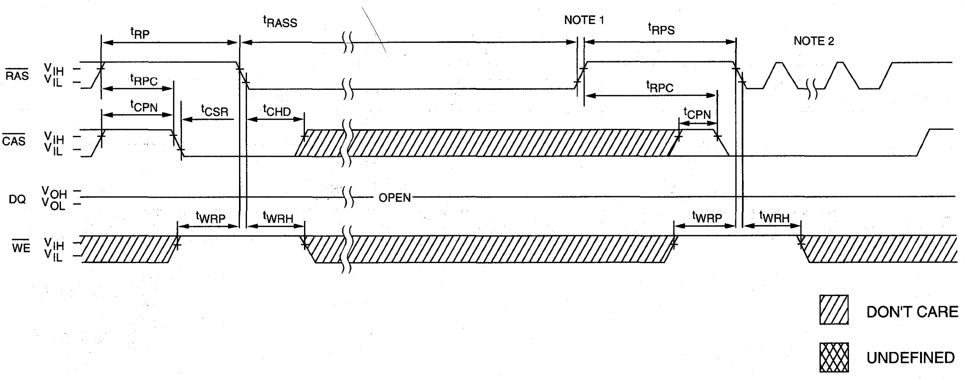
HIDDEN REFRESH CYCLE [21]
(WE = HIGH)



SELF REFRESH CYCLE (S-VERSION ONLY)
(ADDRESSES = DON'T CARE)



NOTE: 1. Once tRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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TECHNICAL NOTE

MOISTURE ABSORPTION IN PLASTIC PACKAGES

NTRODUCTION

All plastic integrated-circuit packages have a tendency to bsorb moisture. During surface-mount assembly, this noisture can vaporize when subjected to the heat associated vith solder reflow operations. Vaporization creates internal tresses that can cause the plastic molding compound to rack. Cracks in the package allow contamination to enetrate to the die and potentially reduce the reliability of he semiconductor device. The cracking process associated vith surface-mountable devices is commonly referred to as he "popcorn effect."

Cracks in the plastic pose several reliability concerns. The noisture path to the die is shortened, allowing ion migration r corrosion to occur more readily. Minor cracks which night not be harmful initially could propagate with time, esulting in a longer-term functional failure.

Since plastic packages absorb moisture, care must be aken to prevent exposure for any long period prior to urface-mounting the devices on the printed circuit board. f exposed to excessive moisture, the devices should be aked to remove moisture prior to solder reflow operations.

This technical note describes the shipping procedures hat ensure Micron's customers will receive memory devices hat do not exhibit the popcorn effect. It also discusses Micron's recommendations for baking the devices if they re exposed to excessive moisture.

ABSORPTION CHARACTERISTICS

Micron's extensive testing empirically characterizes the noisture absorption characteristics of plastic packages. As he plastic takes on moisture, the weight of the device ncreases. Micron employs a standard procedure for veighing the device before and after it is exposed to noisture. We calculate the percentage of weight gain to letermine the relative efficiency of different packaging echniques used for shipping devices.

MICRON PROCEDURES

Micron has eliminated any chance of having popcorn ailures with surface-mount packages by shipping all urface-mount devices in sealed bags containing a desiccant. Devices stored in these bags show no measurable weight gain when subjected to a high-humidity environment for ong time periods.

DEVICE STORAGE

To prevent device failure due to the popcorn effect, store plastic surface-mount packages carefully before PCB assembly. Micron has run tests on devices that have been exposed to 50 percent humidity outside of their shipping containers for time intervals from six months to one year, and no failures have been recorded.

Any concerns about the moisture absorption can be eliminated by storing the devices in Micron's shipping bags. We designed these containers to prevent the passage of water vapor for long periods of time.

DEVICE BAKING

If devices have been removed from their shipping containers and exposed to high levels of moisture, Micron recommends a device bake-out procedure before surface mounting. This bake-out may be accomplished by placing the parts in a tray and baking them in an oven for 160 hours at 40° C. Any moisture is driven out of the devices during the exposure to the heat.

Moisture may be removed faster by baking at 100° C for 24 hours.

SUMMARY

1. All plastic packages absorb moisture when exposed to high levels of humidity for long time intervals.
2. Micron devices have not exhibited any popcorn effect when exposed to 50 percent humidity for long time periods.
3. Micron ships all surface-mount packages in containers that prevent absorption of moisture.
4. If devices have been removed from their shipping containers and exposed to excessive moisture, they should be baked before being surface-mounted.

REFERENCES

"Moisture Absorption and Mechanical Performance of Surface Mountable Plastic Packages": Bhattacharyya, B. K., et al. : 1988 Proceedings of the 38th Electronics Components Conference.

"Analysis of Package Cracking During Reflow Soldering Process": Kitano, M., et al. : 26th Annual Proceeding, Reliability Physics, 1988.

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TECHNICAL NOTE

TAPE-AND-REEL PROCEDURES

GENERAL DESCRIPTION

Tape-and-reel is becoming the packaging and shipment method of choice for Micron's surface-mounted memory devices. Tape-and-reel minimizes the handling of components by directly interfacing with automatic pick-and-place machines.

Micron supports the Electronic Industries Association's (EIA) standardization of tape-and-reel specifications number 481A. The intent of this technical note is to describe Micron's status in support of the EIA standard.

Table 1*
MICRON TAPE SIZES AND DEVICES PER REEL

COMPONENT	TAPE WIDTH (W) mm	PITCH (P) mm	DEVICES PER 13-INCH REEL
PLCC			
18 Pin	24	12	1,000
32 Pin	24	16	500
52 Pin	32	24	500
SOJ (300 mil)			
20/26 Pin	24	12	1,000
24 Pin	24	12	1,000
28 Pin	24	12	1,000
32 Pin	32	12	1,000
SOJ (400 mil)			
28 Pin	32	16	500
32 Pin	44	16	500
40 Pin	44	16	500
TSOP (300 mil)			
20/26 Pin	24	12	1,000
TSOP (400 mil)			
40/44 Pin	32	16	1,000

*These are examples of tape-and-reel sizes available. Please contact Micron for all available options.

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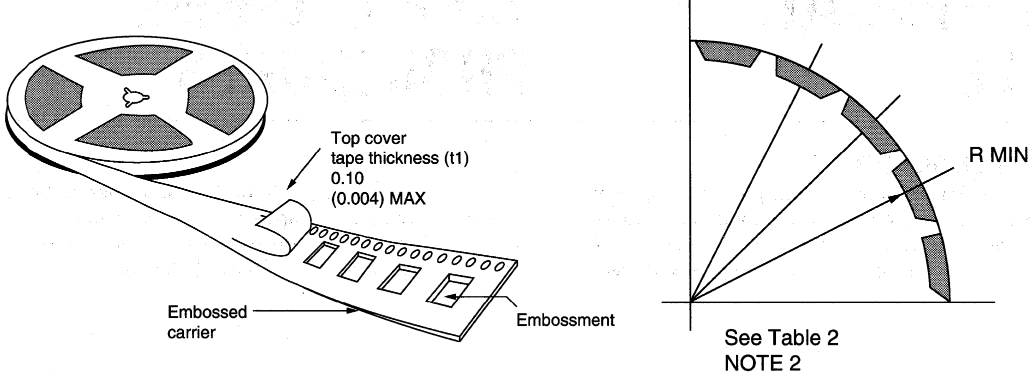
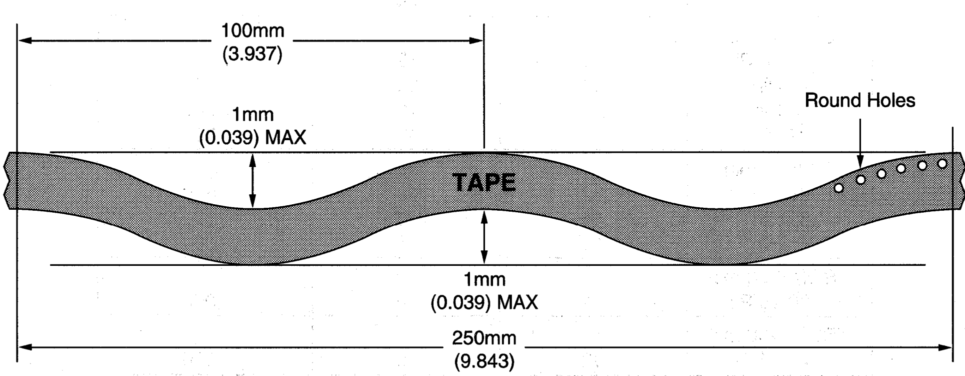


Figure 1
REEL

Figure 2
BENDING RADIUS



Allowable camber to be 1mm/100mm nonaccumulative over 250mm.

Figure 3
CAMBER
(top view)

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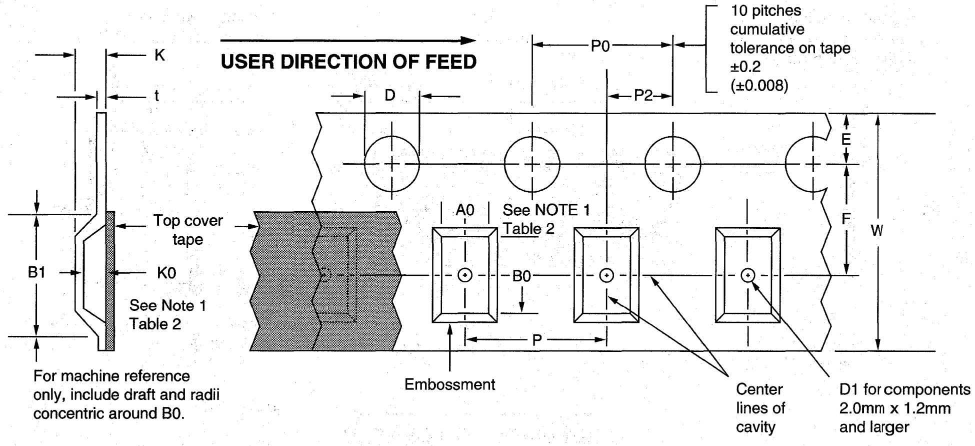

Figure 4
EMBOSSED CARRIER DIMENSIONS
(24mm tape only)

Table 2
24mm EMBOSSED TAPE DIMENSIONS [3]

TAPE SIZE	D	E	P0	t (MAX)	A0, B0, K0
24mm	1.5 $^{+0.10}_{-0.00}$ (0.59) $^{+0.004}_{-0.000}$	1.75 (0.069 ±0.004)	4 (0.157 ±0.004)	0.400 (0.16)	Note 1

TAPE SIZE	B1 (MAX)	D1 (MIN)	F	K (MAX)	P2	R (MIN)	W
24mm	20.1 (0.791)	1.5 (0.059)	11.5 ±0.10 (0.453 ±0.004)	6.5 (0.256)	2 ±0.10 (0.079 ±0.004)	50 (1.969)	24 ±0.30 (0.945 ±0.012)

TAPE SIZE	P					
	4 ±0.10 (0.157 ±0.004)	8 ±0.10 (0.315 ±0.004)	12 ±0.10 (0.472 ±0.004)	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)
24mm			x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters, (inches).

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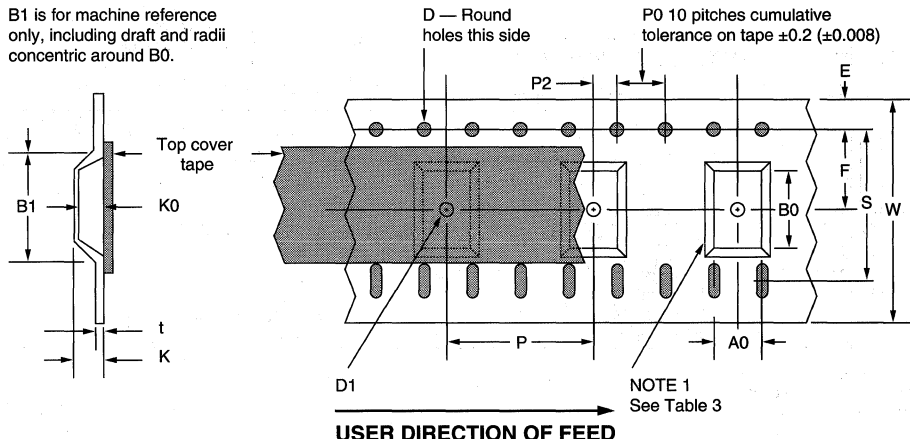

Figure 5
EMBOSSED CARRIER DIMENSIONS
(32 and 44mm tape only)

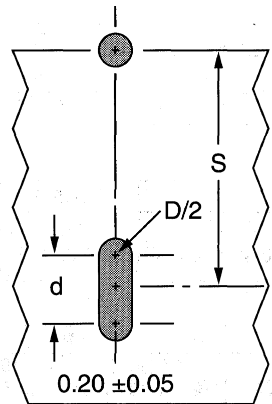

Figure 6
DETAIL ELONGATED HOLE

TECHNICAL NOTE

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Table 3
32 AND 44mm EMBOSSED TAPE [3]

TAPE SIZE	D	D1 (MIN)	E	K (MAX)	P0	t (MAX)	A0, B0, K0
32 and 44mm	1.5 $^{+0.10}_{+0.00}$ (0.059) $^{+0.004}_{+0.000}$	2 (0.079)	1.75 ±0.10 (0.069 ±0.004)	10 (0.394)	4 ±0.10 (0.156 ±0.004)	0.500 (0.20)	NOTE 1

TAPE SIZE	B1 (MAX)	F	P2	S	W	R (MIN)
32mm	23 (0.906)	14.2 ±0.10 (0.559 ±0.004)	2 ±0.10 (0.079 ±0.004)	28.4 ±0.10 (1.118 ±0.004)	32 ±0.30 (1.26 ±0.012)	50 (1.973)
44mm	35 (1.378)	20.2 ±0.15 (0.795 ±0.006)	2 ±0.15 (0.079 ±0.006)	40.4 ±0.10 (1.591 ±0.004)	44.8 ±0.30 (1.732 ±0.12)	50 (1.973)

TAPE SIZE	P							
	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)	28 ±0.10 (1.102 ±0.004)	32 ±0.10 (1.26 ±0.004)	36 ±0.10 (1.417 ±0.004)	40 ±0.10 (1.575 ±0.004)	44 ±0.10 (1.732 ±0.004)
32mm	x	x	x	x	x			
44mm			x	x	x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius “R” without damage.
3. All dimensions in millimeters (inches).

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TECHNICAL NOTE

DRAM POWER-UP AND REFRESH CONSTRAINTS

INTRODUCTION

The JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding and addressing these incompatibilities and providing for them will offer designers and system users greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CAS-BEFORE-RAS (CBR) REFRESH cycle. The CBR for the 1 Meg specifies the WE pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the WE pin held at a voltage HIGH level.

A CBR cycle with WE LOW will put the 4 Meg into the JEDEC-specified test mode (WCBR). In contrast, the 1 Meg test mode is entered by applying a HIGH signal to the test pin (pin 4 on DIPs, pin 5 on SOJs and pin 8 on ZIPs). This HIGH signal is usually a "super voltage" (Vin ≥ 7.5V), so normal TTL or CMOS HIGH levels will not cause the part to enter TEST MODE.

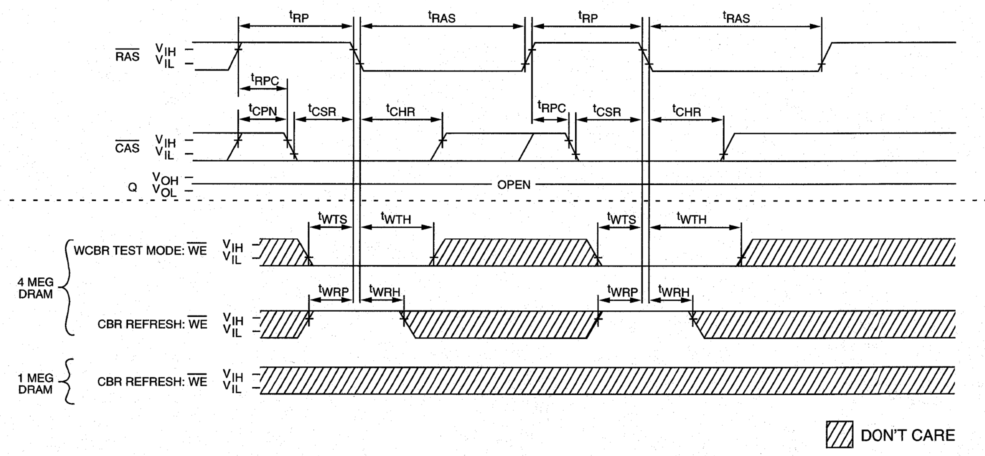
POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight RAS cycles. The 4 Meg POWER-UP cycle is more restrictive in that eight RAS ONLY or CBR REFRESH (WE held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC-specified test mode and must exit out of the TEST MODE. The only way to exit the 4 Meg JEDEC TEST MODE is with either a RAS ONLY or a CBR REFRESH cycle (WE held HIGH).

SUMMARY

The 1 Meg and 4 Meg are compatible, with the following exceptions:

1. For standard TEST MODE, the 1 Meg requires a valid HIGH on the test pin while the 4 Meg requires a CBR cycle with WE LOW.
2. The 1 Meg CBR REFRESH allows the WE pin to be a "don't care" while the 4 Meg CBR requires WE to be HIGH.
3. The eight RAS wake-up cycles on the 1 Meg may be any valid RAS cycle while the 4 Meg may only use RAS ONLY or CBR REFRESH cycles (WE held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

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TECHNICAL NOTE

OE-CONTROLLED/LATE WRITE CYCLES (DRAM)

INTRODUCTION

There are three cycles available to write to a DRAM: EARLY WRITE cycles, READ-MODIFY-WRITE cycles and LATE WRITE cycles. The industry-standard definitions for DRAM WRITE cycles are fairly consistent for both the EARLY WRITE and READ-MODIFY-WRITE cycles. An exception exists for the LATE WRITE cycle.

COMMON DQ DRAM (x4, x8, etc.)

A LATE WRITE cycle is a READ-MODIFY-WRITE (see Figure 1) except that the READ portion is not utilized. This is accomplished by keeping the output enable pin (OE) HIGH throughout the cycle. The timing parameters ᵗRWD, ᵗAWD and ᵗCWD no longer apply since OE is HIGH.

This condition may be viewed as an EARLY WRITE with ᵗWCS "sliding" past the CAS time and violating the 0ns setup time (WE going LOW prior to CAS going LOW). However, since the output buffers are not being used (OE is HIGH), ᵗWCS and ᵗCWD are no longer required.

If WE transitions LOW after CAS transitions LOW, do not bring OE LOW (a noise spike may occur), because the output buffers could turn on and cause contention with the data bus, which could corrupt input data.

The term used for such a WRITE cycle varies throughout the industry. The use of "OE-controlled WRITE," "delayed WRITE" and "LATE WRITE" all signify the same WRITE cycle described.

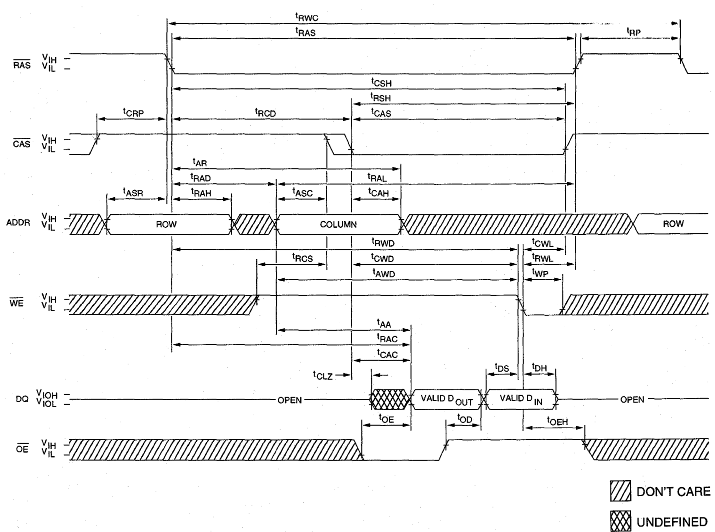

Figure 1
READ-MODIFY-WRITE (MULTIPLE DQ) TIMING

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SPLIT D AND Q DRAM (x1)

A LATE-WRITE cycle is a READ-MODIFY-WRITE, except the READ portion is not guaranteed and the D and Q pins are separate paths (D and Q cannot be connected). This is accomplished by ignoring the timing parameters ^tRWD, ^tAWD and ^tCWD.

This condition can be viewed as an EARLY WRITE with ^tWCS "sliding" past the $\overline{CAS}$ time and violating the 0ns setup time (WE going LOW prior to $\overline{CAS}$ going LOW). However, since the output buffers are "don't care," ^tWCS and ^tCWD are no longer required.

This cycle is not available on applications that have the D and Q connected together, because the output will contend with the input.

SUMMARY

A LATE WRITE cycle is most useful on common DQ DRAMs. Use caution to ensure that the output enable pin is properly controlled.

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TECHNICAL NOTE

DRAM TIMING PARAMETERS

INTRODUCTION

A DRAM has many timing parameters which are specified to help the memory designers define memory system timing. These parameters may be separated into several groups. This note separates these parameters as core parameters (COP) or calculated parameters (CAP).

The calculated parameters are tested by Micron prior to shipment. In cases where the summation of COP parameters is larger than the CAP parameter specification, the CAP parameter overrides the summation of COP parameters. Additionally, if an incoming test is required, the testing of the COP parameter is typically sufficient since CAP parameters are simply combinations of COP parameters.

The CAP parameters are listed below, showing how they are calculated. This will aid the memory designer's understanding of the parameters affected when a COP parameter is altered. Additionally, during testing of the COP parameters, the CAP parameters are also tested by default.

^tRC	=	$^tRAS + {}^tRP + 2{}^tT$
^tPC	=	^tCPA
^tAR	=	^tRCD (MAX) + ^tCAH
^tRSH	≈	^tCAS
^tCSH	=	^tCAS + ^tRCD (MAX)
^tCPA	=	$^tAA + {}^tT$
^tAA	≈	$^tRAS/2$
^tDHR	=	^tRCD (MAX) + ^tDH
^tWCH	=	$^tWP - {}^tWCS - {}^tT$
^tWCR	=	^tRCD (MAX) + ^tWCH
^tRAD (MIN)	=	$^tRAH + {}^tT$
^tRAD (MAX)	=	$^tRAC - {}^tAA$
^tRCD (MIN)	=	$^tRAD + {}^tASC + {}^tT = {}^tRAH + {}^tASC + 2{}^tT$
^tRCD (MAX)	=	$^tRAS - {}^tCAC$
^tRWD (x1)	=	^tRAC
^tRWD (x4)	=	$^tRAC + {}^tOD + 3{}^tT + {}^tDS$
^tCWD (x1)	=	^tCAC
^tCWD (x4)	=	$^tCAC + {}^tOD + 2{}^tT + {}^tDS$
^tAWD (x1)	=	^tAA
^tAWD (x4)	=	$^tAA + {}^tOD + 2{}^tT$
^tRWC (x1)	=	$^tRWD + {}^tRWL + {}^tRP + 3{}^tT$
^tRWC (x4)	=	$^tRAC + {}^tRWL + {}^tRP + 4{}^tT + {}^tOD + {}^tDS$
^tPRWC (x1)	=	$^tCPA + {}^tCWL + 2{}^tT + {}^tDS$
^tPRWC (x4)	=	$^tCPA + {}^tCWL + 4{}^tT + {}^tOD + {}^tDS$

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TECHNICAL NOTE

LPDRAM EXTENDED REFRESH CURRENT vs $\overline{RAS}$ ACTIVE TIME (1 MEG)

INTRODUCTION

One of the most significant features of the low power, extended refresh DRAM (LPDRAM) is its cycle. Extended refresh is essentially a $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) REFRESH at an extended refresh rate of 125µs per cycle.

$\overline{RAS}$ pulse width (^tRAS) affects the extended refresh current and should be considered when designing a low-power system. The longer $\overline{RAS}$ is held LOW, the more current an LPDRAM will consume while in the extended refresh mode. Therefore, keeping ^tRAS at a minimum will maximize power savings.

Figure 1 shows a typical curve of Micron's 1 Meg LPDRAM (MT4C4256L and MT4C1024L) showing the relationship between its extended refresh standby current and the width of ^tRAS. The 25°C curve has a slope of 4.8µA increase for every additional 1µs $\overline{RAS}$ is held LOW. The 70°C curve has a slope of 4µA increase for every additional 1µs $\overline{RAS}$ is held LOW.

SUMMARY

The ^tRAS time should be kept as short as possible when the memory array is being designed. This will result in lower standby currents, especially with the extended refresh cycle.

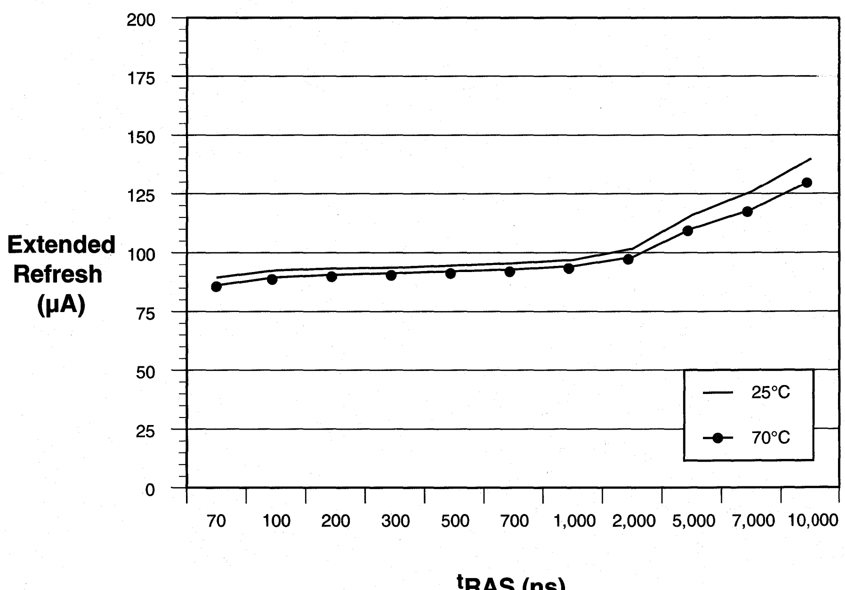

Figure 1
TYPICAL EXTENDED REFRESH CURRENT AS A FUNCTION OF ^tRAS

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TECHNICAL NOTE

LPDRAM EXTENDED REFRESH CURRENT vs $\overline{\text{RAS}}$ ACTIVE TIME (4 MEG)

INTRODUCTION

One of the most significant features of the low-power extended refresh DRAM (LPDRAM) is its cycle. Extended refresh is essentially a $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) REFRESH at an extended refresh rate of 125µs per cycle.

$\overline{\text{RAS}}$ pulse width (^{t}RAS) affects the extended refresh current and should be considered when designing a low-power system. The longer $\overline{\text{RAS}}$ is held LOW, the more current an LPDRAM will consume while in the extended refresh mode. Therefore, keeping ^{t}RAS at a minimum will maximize power savings.

Figure 1, a typical curve of Micron's 4 Meg LPDRAM (MT4C4001J S and MT4C1004J S), shows the relationship between its extended refresh standby current and the width of ^{t}RAS.

SUMMARY

The ^{t}RAS time should be kept as short as possible when designing memory array timing. This will result in lower standby currents, especially for the extended refresh cycle.

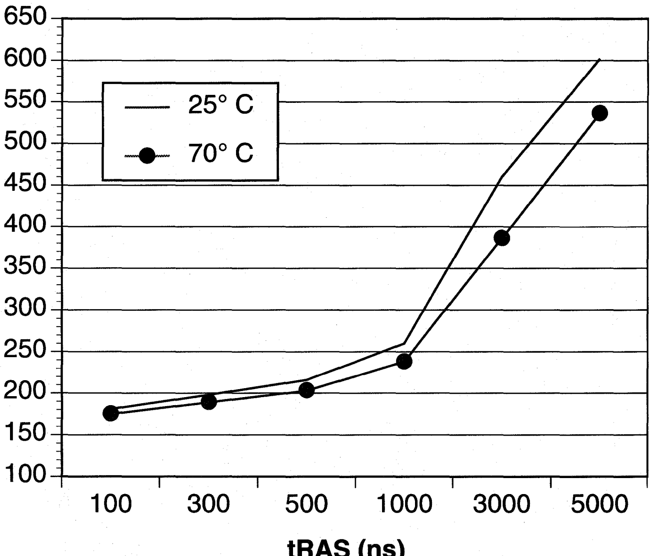

Figure 1
TYPICAL EXTENDED REFRESH CURRENT AS A FUNCTION OF ^{t}RAS

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TECHNICAL NOTE

DRAM CONSIDERATIONS FOR PC MEMORY DESIGN

INTRODUCTION

The demand for DRAM memory in personal computers (PCs) has been mainly for desktop personal computers. When designing main memory, PC designers have primarily focused on three requirements: availability, cost and speed.

The new and growing field of laptop and notebook personal computers has introduced seven additional issues:

- Parity
- Lower power (Extended Refresh)
- SELF REFRESH
- Package size
- Operating current
- 3.3V operating voltage
- DRAM cards (88-pin)

The first three issues (availability, cost and speed) are well understood. This technical note discusses the remaining issues in order to help memory designers choose the best solution for their portable or desktop system designs.

OFFERINGS

To design main memory, four basic offerings of DRAM are or will be available in the near future:

256K x 4	(plus 256K x 1 for parity)
1 Meg x 4	(plus 1 Meg x 1 for parity)
512K x 8	(512K x 9 for parity)
256K x 16	(256K x 18 for parity)

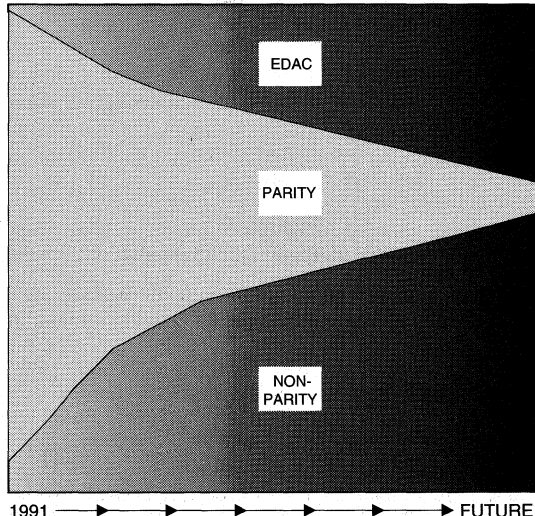
The first two offerings are referred to as "standard DRAMs," and the second two are referred to as "wide DRAMs." Generally, standard DRAMs are more readily available and have more sources. Wide DRAM development is usually a generation behind the standard DRAM and is not expected to catch up until the third generation of 16 Meg DRAMs and the first generation of 64 Meg DRAMs.

PARITY (OR NO PARITY)

There is a growing trend to build laptop, notebook and low-end desktop PCs without parity. Within a few years, all parity-based systems may switch to either nonparity-based systems (as in most PCs) or error detection and correction (EDAC) based systems (high-end PCs).

Some of the reasons for this trend away from parity are listed below:

1. Parity does not significantly improve reliability.
2. DRAMs from a quality manufacturer now have very low soft error rates (SERs).
3. Parity increases memory costs 10 to 15 percent.
4. Some chipsets allow turning off the parity bit.
5. Parity requires extra board space as well as previous generation devices or less available parity chips.
6. Some software does not use parity.



Past, Present and Future Trends

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The most important of these factors is the memory system's reliability. In the early days of semiconductor DRAM memories, the high SER of 4K and 16K DRAMs, coupled with the high cost of implementing EDAC (8-bit buses), made implementing parity critical. DRAM manufacturers, however, have significantly reduced SER during the last five generations (Fig. 1). For example, the SER on a 16K DRAM was approximately 1 to 5 FITs per bit, whereas the SER on a 4 Meg DRAM is closer to 0.0002 to 0.0004 FITs per bit—a 10,000x improvement. (FIT is a failure in time, where time is 1 billion device hours.)

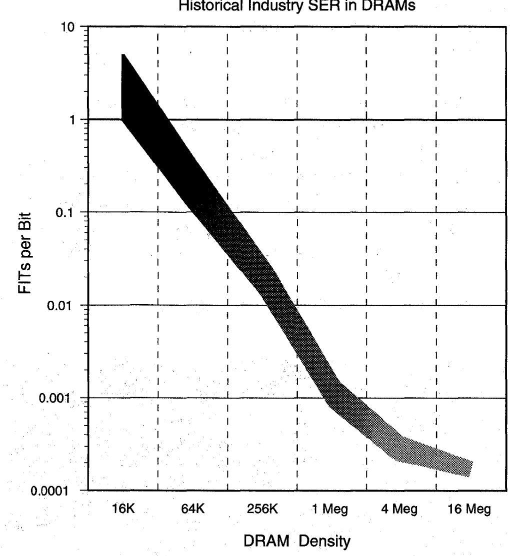

Figure 1
HISTORICAL DRAM SER

By taking these industry SER averages and applying them to a 2MB, 16-bit wide memory system, meaningful benchmarks for PCs can be obtained. Most systems measure errors in mean time between failures (MTBF). Applying the SER numbers from the previous figure, the improvement in MTBF for a typical 2MB, 16-bit wide memory system can be demonstrated (Fig. 2).

It is obvious why parity was instituted in the 16K DRAM days. A memory system made of 16K DRAMs would experience a SER hit every 60 to 70 hours. Because of this, it has been standard operating procedure to design in parity. But changes are ahead. System designers are starting to ask, "Why?" Using today's high-quality 4 Meg DRAMs rather than yesterday's 16K DRAMs extends the MTBF from approximately 60 hours to an MTBF of 30 to 35 years on a 2MB by 16-bit wide memory system.

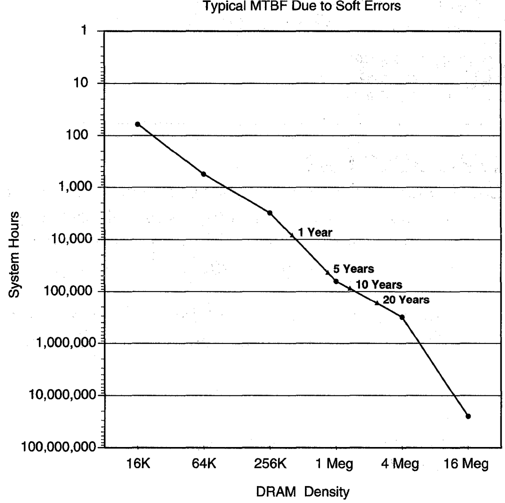

Figure 2
MTBF for 2MB Memory System

Another way to look at this same data is to calculate the number of SER hits a user would see after ten years of continuous use (Fig. 3). As expected, the SER is negligible after ten years of continuous use when using today's high-quality DRAMs.

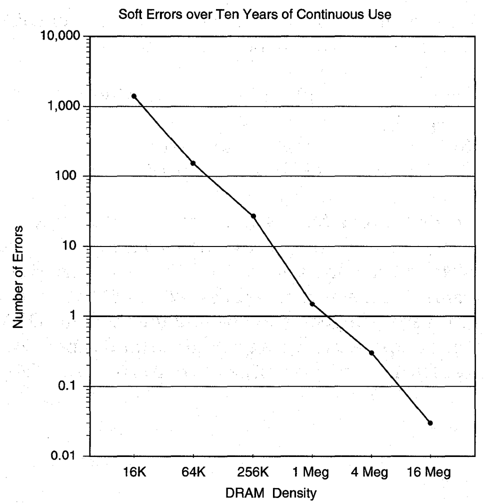

Figure 3
2MB MEMORY SYSTEM SER

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It is important to note that the SER and MTBF must be carefully calculated for any given system and its application. The DRAM's SER is dependent on Vcc (power supply voltage), operating speed (cycle rate) and memory configuration. By taking the previous 2MB example and doubling it to 4MB, the SER will either increase slightly or double. If the width of the memory system is increased to 32 bits, the SER would double since all DRAM bits are active. If, on the other hand, the memory is interleaved and the bus remains 16 bits wide, the SER increases only slightly. This is because the bank not being accessed is in standby mode and is much less susceptible to SER hits. (The faster the cycle rate, the more susceptible a DRAM is to SER.)

Although the need for parity would appear to be greater for wider buses, the additional cost to implement EDAC, rather than parity, decreases substantially as the bus width increases. In fact, the DRAM memory cost is the same for a 64-bit wide bus (Table 1). Besides detecting two errors for a given word, EDAC will also correct any single bit error.

Table 1
Parity and EDAC Overhead

	EXTRA BITS REQUIRED		BUS WIDTH INCREASE	
BUS SIZE (BITS)	PARITY	EDAC	PARITY	EDAC
8	1	5	12.5%	62.5%
16	2	6	12.5%	37.5%
32	4	8	12.5%	25%
64	8	8	12.5%	12.5%

Most applications with buses no more than 32 bits wide do not require parity, whereas applications using bus widths of 32 bits or more generally require some kind of bit-checking for errors. The choice is usually EDAC rather than parity.

Table 2
Selection for Error Checking

ERROR CHECKING	BUS SIZE (BITS)			
	8	16	32	64
Nonparity	1 Meg x 4	1 Meg x 4	1 Meg x 4	512K x 8
Parity	512K x 9	1 Meg x 4	1 Meg x 4	512K x 8
EDAC	n/a	n/a	1 Meg x 4	512K x 8

Table 2 summarizes which DRAM would be the optimum choice, considering price, performance and space. It takes into account the typical PC which ships with a minimum of 4MB of memory. A 256K x 16 or 512K x 8 DRAM could be a better alternative than a 1 Meg x 4 DRAM, should the memory system's depth be equal to or less than 512K bits deep. This is typically the case with wider buses. The 64-bit bus choice of 512K x 8 DRAMs would change to 1 Meg x 4 should the total memory size increase from 4MB to 8MB.

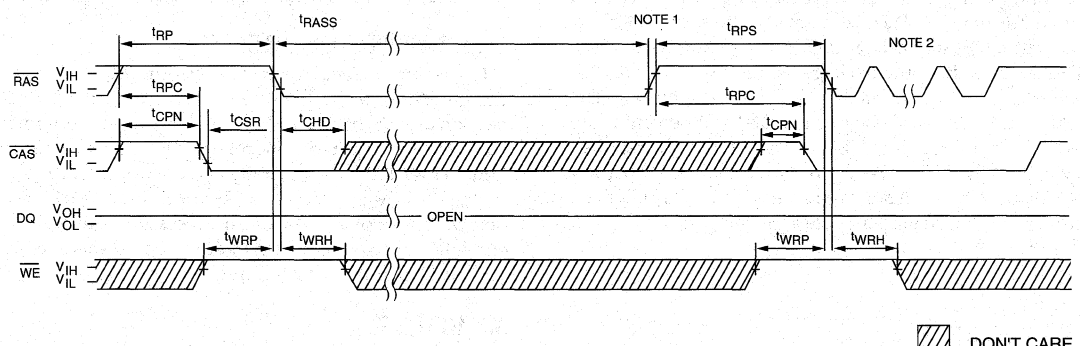

Figure 4
SELF REFRESH OPERATION

NOTE:
1. Once ^{t}RASSmin is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a complete burst refresh of all rows should be executed. Distributed refreshes at the specified refresh rate are acceptable, provided CBR refreshes are utilized.

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LOW-POWER, EXTENDED REFRESH

A low-power, extended refresh DRAM (LPDRAM) has a reduced CMOS standby current limit (typically from 1mA to 200µA) and refresh interval eight times longer (from 15µs per row to 125µs per row). The extended refresh offers an extended mode, which is a low-current, data-retention cycle. Each of the four DRAM options in this technical note have low power, extended refresh versions available.

On a per-bit basis, the 1 Meg x 4 generally offers the best standby and refresh power savings compared to the other three DRAM organizations. The DRAM standby current is important in battery-operated systems, since DRAMs usually draw a large percentage (50 to 70 percent) of the total system current when the system is in sleep or suspend mode.

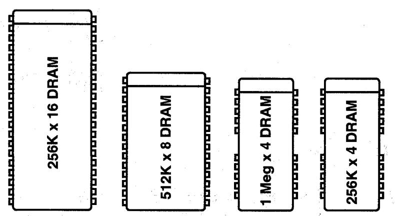
SELF REFRESH

The SELF REFRESH feature built into some DRAMs is usually indicated by an LL or S suffix. This feature performs an extended refresh mode, with the exception that no external clocking is required; that is, the DRAM will refresh itself via its own internal refresh clock (Fig. 4).

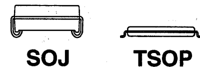
Control of SELF REFRESH is defined by JEDEC and the following defacto standard timing specifications: $^{t}RASS$ = 100µs, $^{t}RPS \approx {}^{t}RC$, ^{t}CHD = 10ns.

PACKAGE SIZE

Conserving board space is always an important design consideration, especially for laptop and notebook computers. Functionally, DRAMs require more board space than most other devices. The size between the four options in small outline J-lead package (SOJ) vary greatly. The 256K x 4 DRAM uses the same package as the 1 Meg x 4 DRAM; however, four times as many devices are required. The 512K x 8 DRAM requires approximately 50 percent more area than a 1 Meg x 4 DRAM. The 256K x 16 requires approximately 110 percent more area than a 1 Meg x 4 DRAM and 44 percent more area than a 512K x 8. Full-sized outlines are shown here for comparison:



These are also available in a thin, small-outline, gull-lead package (TSOP). The length and width of a TSOP are the same as the corresponding SOJ package (same board area) except that the x16 width TSOP is reduced because of a smaller lead pitch (50mil to 32mil). The TSOP's key attraction is that it is one-third the thickness of the SOJ (47 mils compared to 142 mils), as illustrated below:



Laptop, notebooks and other compact designs which have height or layout restrictions can usually justify the current cost premium required to use TSOPs. However, any price premium associated with TSOPs will be short-lived and is expected to disappear by mid-1993. Additionally, in TSOP, the x16 does not impose as severe a board space penalty, as does a x8 TSOP. Table 3 lists the dimensions (length and width) for the various packages.

Table 3
PACKAGE DIMENSIONS (in mils)

	SOJ		TSOP	
Device Type	Width	Length	Width	Length
1 Meg x 4	340	679	367	677
512K x 8	445	729	467	727
256K x 16	445	1029	467	727

OPERATING CURRENT

Operating current is usually of less importance in system design. When a PC is in the active mode, the DRAM's portion of current draw is minimal (typically from four to six percent) compared to the total system current consumption. Wider DRAMs generally offer lower operating currents (10 to 20 percent) in most applications, since fewer devices are active for a given access, but generally not enough to outweigh the cost increase, board space increase and performance reduction they impose.

3.3 VOLTS

Laptop and notebook personal computers and BBU systems are also starting to employ 3.3V DRAMs. A low-voltage (3.3V) DRAM consumes approximately half the power of a 5V version. The choice of whether to use 5V or 3.3V DRAMs is dictated by the voltage platform selected, which is determined by the CPU and chipset specifications. Once the voltage range is selected, the considerations discussed in this technical note apply for either 5V or 3.3V DRAMs.

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FUTURE FEATURES

Many new features will be available in the near future. Some of the more important features may be extended data-out (EDO) and synchronous DRAMs. The EDO DRAM is a FAST PAGE DRAM with the exception that the data outputs (DQ) are not tristated by $\overline{CAS}$.

The key advantage with EDO is a PAGE-MODE READ cycle up to 30 percent faster. Since $\overline{CAS}$ does not tristate the DQs, ^tCAS can be minimized and $\overline{CAS}$ precharge can occur while the output data is being latched. EDO is considered a possible bridge for performance increase until synchronous DRAMs are a reality.

The synchronous DRAM is a radical change from the standard DRAM. Rather than being dependent on time delays, the synchronous DRAM's inputs will all be clocked-in on the positive edge of the system clock. The synchronous DRAM is expected to provide the speed performance required for 66, 75 and 100 MHz systems. Future synchronous DRAMs will achieve speeds beyond 100 MHz.

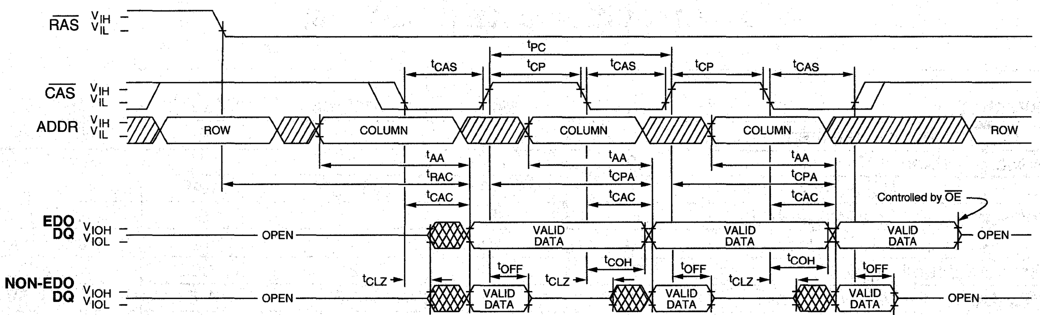

Figure 5
EDO vs NON-EDO (FAST PAGE MODE) DRAMS

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SUMMARY

The 1 Meg x 4 DRAM is today's best choice for main memory in laptop, notebook and desktop personal computers. Table 3 summarizes and compares the issues involved in selecting DRAMs for PC memories.

Wider DRAMs are best suited to systems which require shallow and wide arrays. The 256K x 16 is a good choice for high-end video graphics and printer buffers requiring up to 256K bits deep and 16 or more bits wide. The 512K x 8 is usually a good choice for 8-bit systems requiring more than 256KB but less than 1 Meg of memory, such as high-end disk drives.

Most PC systems do not require the burden of parity when using 1 or 4 Meg DRAMs. High-end systems should use EDAC for the best reliability.

Table 3
2 MEGABYTE MODULE (1 MEG x 16)

PARAMETERS		1 MEG x 4	256K x 4	512K x 8	256K x 16	UNITS
Number of Devices Required		4	16	4	4	Devices
Availability (Market Volume)		20	160	2	1	Relative to
	Base Price	1.0	1.0	1.15[1]	1.2[2]	1 Meg x 4
Costs	Low Power Adder	5	5	5	5	% of Base
	TSOP Adder	10	40	10	10	% of Base
Minimum Speed (Typical)		70	70	80	80	ns @ 5V
BBU ICC[3]	Maximum Spec	1.2	4.8	1.6	1.6	mA @ 5V
	Typical	0.6	1.3	1.2	1.2	mA @ 5V
Minimum Board Space Used		6	24	9	13	cm^2
Active ICC[3]	Maximum Spec	340	260	200	140	mA @ 5V
	Typical	200	160	170	120	mA @ 5V

NOTE:
1. A parity version (x9) would be 1.3 times a 1 Meg x 4.
2. A parity version (x18) would be 1.35 times a 1 Meg x 4.
3. Parity versions (x9/x18) typically have currents approximately ten percent higher.

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TECHNICAL NOTE

16 MEG DRAM—2K vs 4K REFRESH COMPARISON

INTRODUCTION

Micron Semiconductor, Inc., offers its 4 Meg x 4 DRAM in two JEDEC-approved versions. The MT4C4M4A1 requires 12 row-address bits and 10 column-address bits for 4,096 (4K) cycle refresh in 64ms. The MT4C4M4B1 requires 11 row-address bits and 11 column-address bits for 2,048 (2K) cycle refresh in 32ms. Excluding this difference, the timing and performance of the two devices are identical.

Industry demand for decreased power consumption led JEDEC to approve 4K refresh in addition to 2K refresh at the 16 Meg level. At minimum random cycle time (^tRC = 110ns), A 4 Meg x 4 device with 4K refresh draws ≈30mA less operating current than a device with 2K refresh. The current is decreased by increasing the number of rows and decreasing the number of columns in the DRAM array. A 4 Meg x 4 with 4K refresh has 4,096 rows and 1,024 columns, whereas one with 2K refresh has 2,048 rows and 2,048 columns. The number of columns defines the "depth" of a page. The drawing below shows how 2K and 4K refresh devices are different. Notice that the 2K device has a page depth of 2,048, while the 4K device has a page depth of 1,024, or half the page depth of the 2K device.

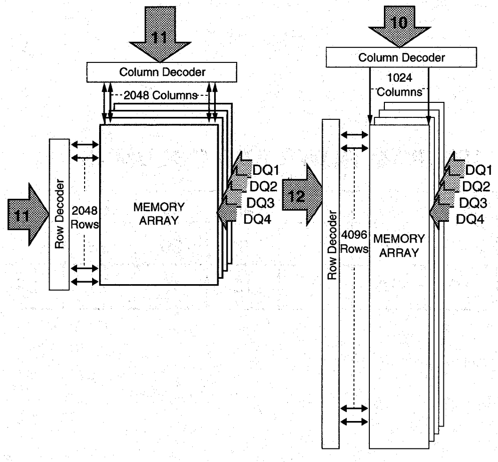

Figure 1

CHOOSING 2K OR 4K REFRESH

There are several factors to consider when deciding which refresh standard is best for an application:

1. Addressing supported by your DRAM controller—11 row/11 column, 12 row/12 column, or both?
2. Frequency and length of page accesses
3. Average cycle rates

Some DRAM controllers have only 11 address drivers, so they are limited to 2K refresh. Many newer DRAM controllers, including some of the 3.3V controllers, are being designed to support both standards, so this limitation should be short-lived.

Your choice of 2K or 4K refresh will probably be based on the importance of power consumption versus page depth. A system requiring frequent page accesses may not benefit by sacrificing page depth in exchange for the power savings of a 4K refresh. In a portable system, the benefits of 20mA less current may easily override concerns about decreased page depth.

Additionally, the difference in power consumption decreases with longer cycle times. If the DRAMs spend much of their time idle, as in systems using SRAM caches, the power savings may be negligible. See Figure 2.

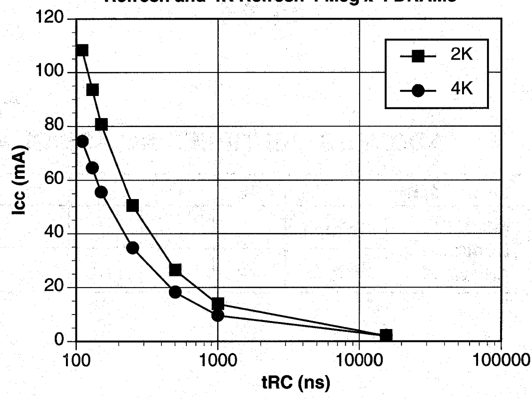

Figure 2

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MODULES

Modules may use both 2K and 4K refresh depending on whether or not they have twelve address inputs. If a module uses parity, such as the 4 Meg x 9 or the 4 Meg x 36, it probably mixes 4 Meg x 4 and 4 Meg x 1 DRAMs on the same module. Because the 4 Meg x 1 DRAM requires symmetric addressing (11 row-addresses and 11 column-addresses), using a 4K refresh 4 Meg x 4 DRAM requires that the DRAM controller support both addressing decodes simultaneously. This is possible using "redundant addressing," whereby one of the address bits is duplicated as both a row-address and as a column-address. Most modules that have parity will simply use the 2K refresh 4 Meg x 4 DRAM in order to avoid changes to existing controllers. As shown in Figure 3, when a 4 Meg x 4 with 2K refresh is employed, the numbers of rows and columns match the 4 Meg x 1, allowing use of the 4 Meg x 1 for parity.

If the 4 Meg x 4 with 4K rows is implemented, redundant addressing must be employed, or use of the 4 Meg x 1 for parity becomes impossible because the number of rows and columns does not match. The shaded areas shown in Figure 4 are the portions of the DRAM that can't be used because of the difference in the number of rows and columns. Table 1 shows an example of redundant addressing. If bit 23 is set to equal bit 22, it can serve as both the 12th row-address on the 16 Meg and the 11th column-address on the 4 Meg.

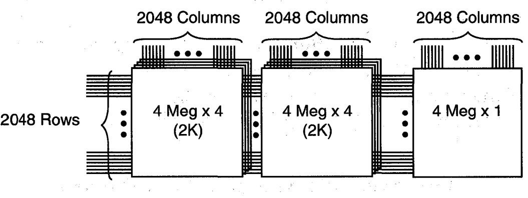

Figure 3

SUMMARY

1. JEDEC has approved two refresh standards at the 16 Meg level, 2K and 4K.
2. 2K refresh is 2,048 cycles in 32ms; 4K refresh is 4,096 cycles in 64ms.
3. Devices with 4K refresh cut current consumption by 20mA under worst-case operating conditions.
4. Devices with 4K refresh have half the page depth of a 2K device.
5. Existing 5V standard modules generally will use the 2K refresh standard DRAM.

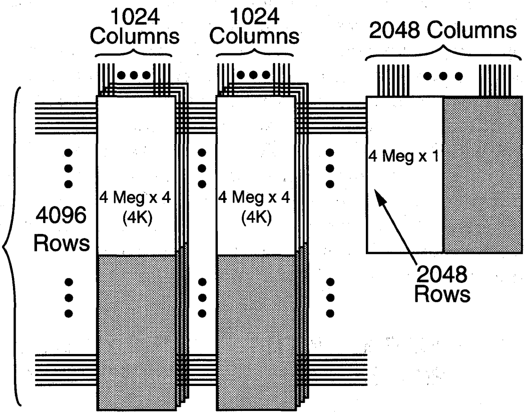

Figure 4

Table 1
ADDRESS MULTIPLEXING ASSIGNMENT FOR DRAM ROWS AND COLUMNS

DRAM Adress		A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11
Memory Controller Address	Column	1	2	3	4	5	6	7	8	9	20	23	
	Row	10	11	12	13	14	15	16	17	18	19	21	22

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TECHNICAL NOTE

256K x 16 DRAM VARIATIONS

INTRODUCTION

Micron Semiconductor, Inc., offers its 256K x 16 DRAM in a number of JEDEC-approved versions. BYTE WRITE control and symmetrical or asymmetrical addressing are available. The timing and performance of the devices are similar, with the few differences described here.

WORD OR BYTE WRITE CONTROL

Many systems require the ability to write one byte at a time. To accommodate this need, Micron supplies the x16 devices with either two $\overline{CAS}$ signals or two $\overline{WE}$ signals. One of the signals is used to select the upper byte and one is used to select the lower byte.

Controllers exist that support either version, so choosing dual $\overline{CAS}$ or dual $\overline{WE}$ depends on the controller you wish to use. Often, systems that are upgraded from 256K X 4 DRAMs will use the dual $\overline{CAS}$ version because the controllers are already set up for that version. The dual $\overline{CAS}$ allows the user to do byte reads or byte writes, whereas the dual $\overline{WE}$ does not have the capability to perform byte reads. Many graphics controllers prefer the dual $\overline{WE}$ version, because some data processing may take place during the first part of a cycle and the dual $\overline{WE}$ allows a LATE WRITE, giving more time for data manipulation. The timing diagram in Figure 1 illustrates the WORD and BYTE WRITE cycles using dual $\overline{CAS}$ signals.

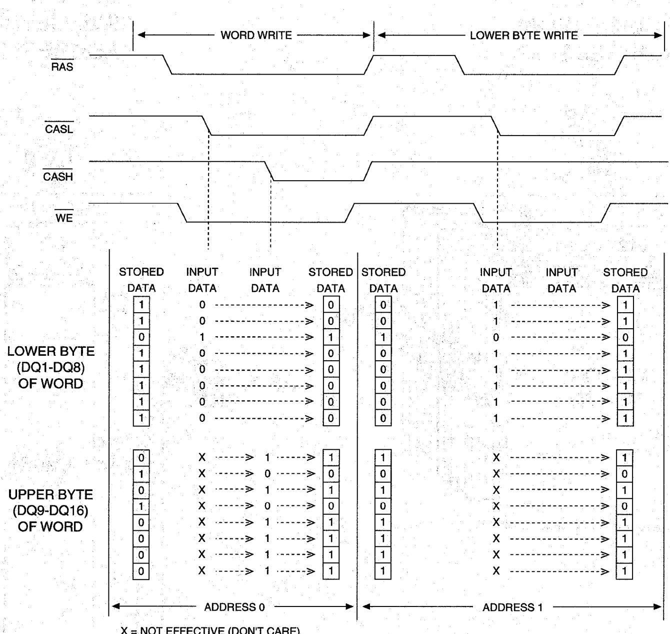

Figure 1
WORD AND BYTE WRITE EXAMPLE USING DUAL $\overline{CAS}$ VERSION

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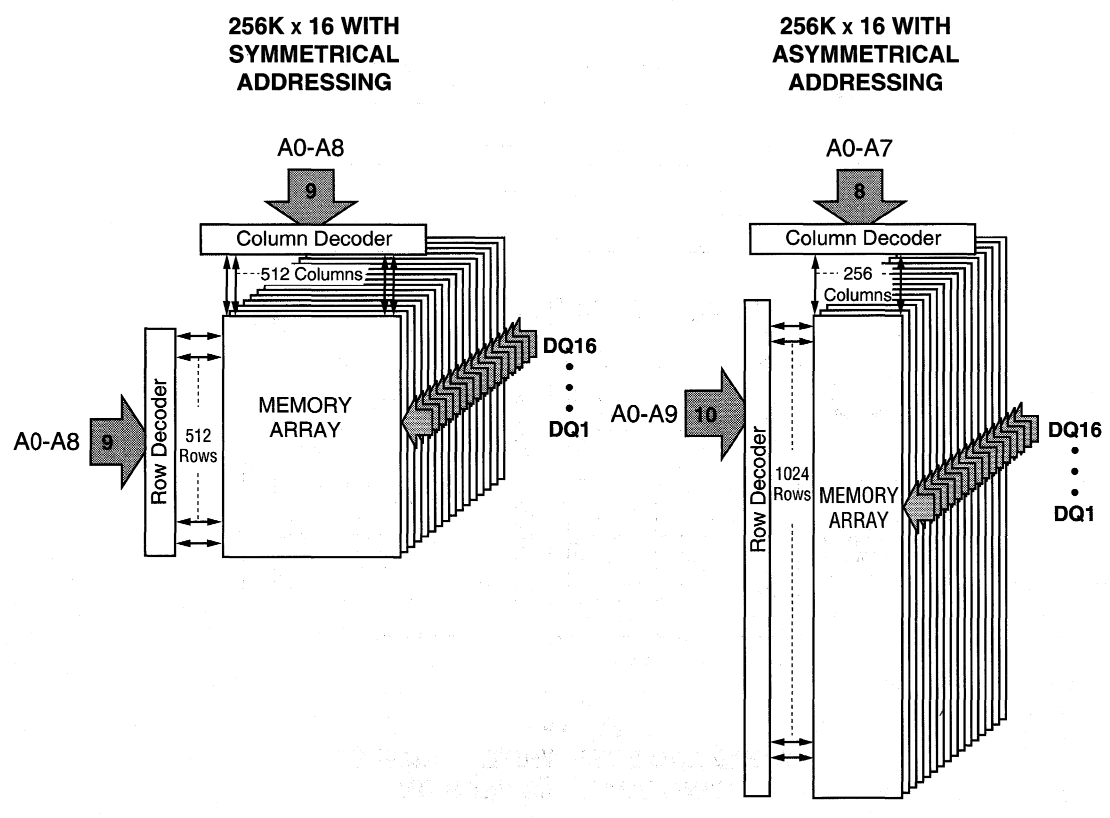
SYMMETRICAL AND ASYMMETRICAL ADDRESSING

In the past, the addressing of DRAMs has been simple. The number of row-address lines was equal to the number of column-address lines. This is known as "symmetrical addressing." For the x16 devices, JEDEC has approved a slightly different type of addressing called "asymmetrical," in addition to the symmetrical version. Asymmetrical addressing has more row-address lines than column-address lines. With the increased number of rows and decreased number of columns, there is a potential for power savings at the chip level (one-half the number of sense amplifiers activated in any one cycle).

A 256K x 16 DRAM with symmetrical addressing has 512 rows and 512 columns, whereas one with asymmetrical addressing has 1,024 rows and 256 columns. The number of columns defines the "depth" of a page. The illustrations below show how the symmetrical and asymmetrical devices differ. Note that the symmetrical device has a page depth of 512, while the asymmetrical device has a page depth of 256, or half the page depth of the symmetrical device. The symmetrical 256K x 16 requires a 512-cycle refresh in 8ms, while the asymmetrical requires a 1,024-cycle refresh in 16ms.

SUMMARY

1. x16 wide devices will be available with word or byte write capability. Byte write capability can be implemented with dual $\overline{CAS}$ or dual $\overline{WE}$.
2. JEDEC has approved asymmetrical and symmetrical addressing for the 256K x 16 DRAM.
3. Symmetrical 256K x 16 requires a 512-cycle refresh in 8ms; asymmetrical requires a 1,024-cycle refresh in 16ms.



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TECHNICAL NOTE

LOW-POWER DRAMS vs SLOW SRAMS FOR MAIN MEMORY

INTRODUCTION

The market for portable computers such as notebooks, laptops and palmtops is extremely competitive and fast-paced. Designers of these systems are continually trying to minimize power, cost and size without compromising performance. One of the most challenging areas is memory design. To meet their design constraints, manufacturers are using either low-power DRAMs or slow SRAMs for memory. This technical note discusses memory design and the trade-offs associated with each of these types of memory.

LPDRAMs AND SLOW SRAMs

Users of portable devices want long battery life. Reducing power consumption to meet this need is critical. This is why portables use low-power extended refresh DRAMs (LPDRAMs) instead of standard DRAMs. A standard DRAM has standby currents of 3mA at a $15\mu s$ refresh cycle. LPDRAMs have standby currents ranging from 1mA to $200\mu A$, and a refresh interval of $125\mu s$ (extended refresh).

LPDRAMs offer a very low-power standby power mode called BATTERY BACKUP (BBU) mode. BBU is the lowest DRAM power mode possible that still retains data. It consists of a $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH cycle at the slowest possible cycle rate.

Some designers have used slow SRAMs in their designs since they offer low standby currents. Slow SRAMs are usually defined as SRAMs with a cycle speed of 80ns or slower. They have low standby currents when compared to standard DRAMs.

A standard memory configuration was chosen in order to compare the two types of memory. In portables, a 2MB memory in a x16 configuration is quite common. Memory will typically be a 4 Meg DRAM (x4 or x8) or a 1 Meg SRAM (x8). These memory arrays are compared in the following paragraphs and in Table 1 on the next page.

COST

In the highly competitive notebook market, reduction of cost is crucial. Because an SRAM bit cell uses four times as many transistors as a DRAM, the amount of silicon area used is much larger. Cost is proportional to silicon area, so for a given amount of memory the SRAM takes up more area and costs more. This is clearly seen in the marketplace since 256K SRAMs are more expensive than 256K DRAMs, 1 Meg SRAMs are more expensive than 1 Meg DRAMs, etc.

Of course, the size of a chip can be increased only so far before yield drops. When 4 Meg DRAMs were the highest density DRAM being manufactured, only 1 Meg SRAMs were available. A designer would only need one-fourth the number of 4 Meg DRAM parts over 1 Meg SRAMs. Table 1 compares the relative cost of several arrays; DRAMs always have the cost advantage.

SIZE AND WEIGHT

Typically, DRAMs are a generation ahead of SRAMs and are thus a factor of four ahead in density. This is because SRAMs take up much more silicon die area for a given memory density. For a typical memory size, SRAMs require four times as many devices and four times the board area (see Table 1).

DRAMs use multiplexed row and column addressing whereas SRAMs use unmultiplexed addressing. For an identical size of memory, DRAM packages use less pins and are smaller. This contributes to their effectiveness in minimizing space.

A designer should be cautious in choosing a slow SRAM for a portable application due to the board space required to implement the memory system. Similarly, the increased number of devices will make the portable heavier.

POWER

One of the main problems with notebook computers today is that the battery life is too short. Even with the large batteries used today, battery life can be less than two hours–users are demanding eight hours or more.

Slow SRAMs have an advantage in standby and active currents (typical). As you can see from Table 1, slow SRAM standby current can be much lower than that of DRAMs. This is because only a portion of the memory is accessed at any given time, so much of the memory is in standby mode.

SUMMARY

The portable market is so competitive that cost is usually the overriding consideration. Even if battery time can be extended slightly with slow SRAMs, cost and increased board space usually prohibit their use. DRAMs have been and will likely continue to be the part of choice in portable applications.

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Table 1
2MB, 16-BIT-WIDE MEMORY

PART TYPES		1 MEG x 4 DRAMS	512K x 8 DRAMS	128K x 8 SLOW SRAM[4]	128K x 8 SLOW SRAM[5]	UNITS
Number of Devices Required		4	4	16	16	No. of Devices
Total Cost[1]		1.0	1.1	4.3	4.3	Relative Cost
Minimum Speed		70	70	85	85	ns
Standby/BBU Current[2]	(MAX)	1.2	1.2	1.6	0.8	mA
	(Typical)	600	600	32	32	µA
Active Icc Current[2, 3]	(MAX)	240	160	140	140	mA
	(Typical)	141	94	90	90	mA
Minimum Board Space Used		0.9	1.3	7.4	7.4	(TSOP) in^2
Weight[6]		1.0	1.4	5.8	5.8	Relative Weight

NOTE:
1. Costs are relative to the 1 Meg x 4 DRAM.
2. Assumes an 80ns part in FAST PAGE MODE for DRAMs, 85ns part for SRAMs.
3. For the x8 devices, only a portion of the array is active at any one time.
4. Standard slow SRAMs
5. Low-power slow SRAMs
6. Weight is relative to the 1 Meg x 4 DRAM.
7. The rest are in standby.

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TECHNICAL NOTE

SELF REFRESH DRAMS

INTRODUCTION

DRAM memories targeted for the low-power, portable market are providing several new features to help maximize power savings. One of these new features is the SELF REFRESH mode. DRAMs having this new feature are referred to as SELF REFRESH DRAMs and provide the user with a very low-current, data-retention mode.

This mode has been approved by JEDEC and is quickly becoming an industry-standard feature. Most 3.3V DRAMs will be offered with this feature, as will many future 5V DRAMs.

SELF REFRESH DRAMs vs LPDRAMs

Low-power, extended-refresh DRAMs (LPDRAMs) have the same functionality as a standard DRAM, except they have been tested to meet the lower CMOS standby current and the extended refresh specifications. SELF REFRESH DRAMs, on the other hand, require additional circuitry be added to the standard DRAM to perform the SELF REFRESH function.

SELF REFRESH MODE

SELF REFRESH mode provides the DRAM with the ability to refresh itself while in an extended standby mode (sleep or suspend). It is similar to the extended refresh mode of an LPDRAM except the SELF REFRESH DRAM utilizes an internally generated refresh clock while in the SELF REFRESH mode.

During a system's suspend mode, the internally generated refresh clock on the DRAM replaces the DRAM controller refresh signals. Therefore, it is no longer necessary to power-up the DRAM controller while the system is in the suspend mode. Consulting the devices' data sheets will determine the power savings achieved.

USING SELF REFRESH

SELF REFRESH introduces the new parameters ᵗRASS, ᵗCHD and ᵗRPS. These new parameters are shown in Figure 1. The DRAM's SELF REFRESH mode is initiated by executing a $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) REFRESH cycle and holding both $\overline{RAS}$ and $\overline{CAS}$ LOW for a specified period. The industry standard for this value is 100µs minimum (ᵗRASS). The DRAM will remain in the SELF REFRESH mode while $\overline{RAS}$ and $\overline{CAS}$ remain LOW. Once $\overline{CAS}$ has been held LOW for ᵗCHD, $\overline{CAS}$ is no longer required to remain LOW and becomes a "don't care."

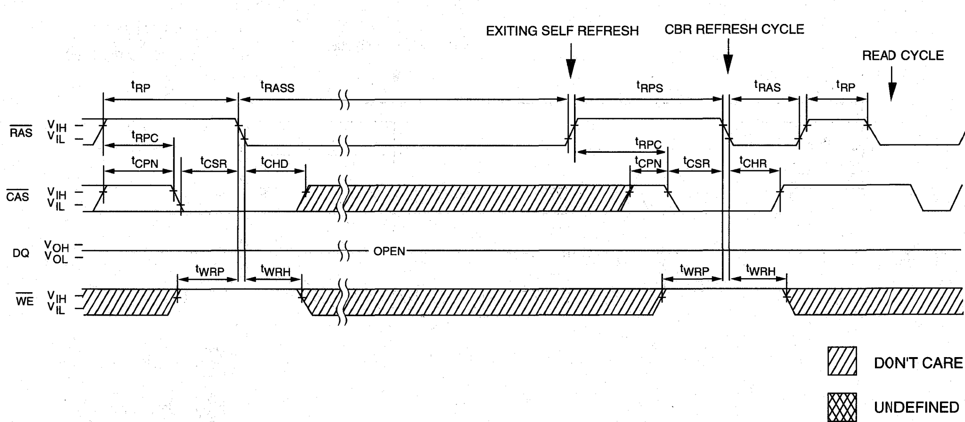

Figure 1
SELF REFRESH CYCLE UTILIZING DISTRIBUTED CBR REFRESH

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The SELF REFRESH mode is terminated by taking $\overline{RAS}$ HIGH for ^tRPS (the minimum time of an operation cycle). Once the SELF REFRESH mode has been terminated, the user can access the DRAM normally.

HOW IS SELF-REFRESH DONE?

SELF REFRESH can be implemented on the device in two ways. One method utilizes a distributed method and the second uses a wait and burst method. Micron devices use the distributed method.

Devices that utilize the distributed method will refresh the rows at a regular rate, utilizing the CBR REFRESH counter to turn on rows. In a system that utilizes distributed CBR REFRESH as the standard refresh, accesses to the DRAM can begin as soon as SELF REFRESH is exited. The first CBR pulse should occur within the time of the external refresh rate prior to active use of the DRAM to ensure maximum data integrity and must be executed within three external refresh rate periods. Since CBR REFRESH is commonly implemented as the standard refresh, this ability to access the DRAM immediately after exiting SELF REFRESH is a big benefit over the burst scheme described later. If anything other than CBR REFRESH is used as the standard refresh, a burst of all rows needs to be executed when exiting SELF REFRESH. This is because the CBR counter and the DRAM controller counter will not likely be at the same count. If they're not at the same count and both are being used in the distributed method, then refresh will be violated and data will eventually be lost.

An alternative way to implement SELF REFRESH is to use an internal burst refresh scheme. Instead of turning on a row at regular intervals, a circuit would sense when the array needs to be refreshed and then sequence through the rows until all had been refreshed. When exiting a burst type SELF REFRESH, the entire array must be refreshed before any accesses are allowed, regardless of the type of refresh used (see Figure 2). This full burst is necessary because you may have exited SELF REFRESH just before the entire array was going to be refreshed. If the burst is not performed when exiting this type of SELF REFRESH, you may violate refresh requirements and lose data.

Micron's devices allow you to access the DRAM as soon as SELF REFRESH is exited, while other manufacturers' devices may require a full burst when exiting, regardless of the refresh used. To prevent possible compatibility problems, you may want to design the controller to perform the burst when exiting SELF REFRESH.

SUMMARY

1. SELF REFRESH mode allows additional power savings for portable applications since the DRAM controller is no longer required to remain powered-up while the system is in the suspend mode.
2. The mode is initiated by executing a CBR REFRESH with $\overline{RAS}$ and $\overline{CAS}$ remaining LOW for at least 100us.
3. The SELF REFRESH mode remains active until $\overline{RAS}$ is taken HIGH.
4. You may access the DRAM as soon as SELF REFRESH has been exited, provided you use distributed CBR REFRESH as the standard refresh.

TECHNICAL NOTE

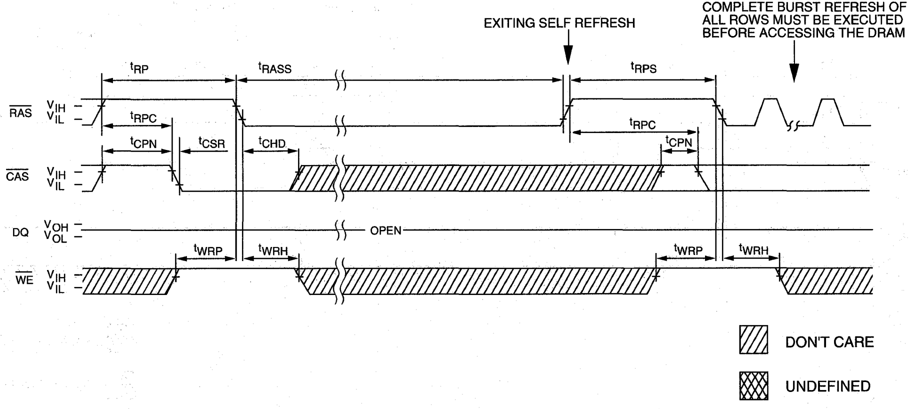

Figure 2
SELF REFRESH CYCLE UTILIZING BURST REFRESH SCHEME

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TECHNICAL NOTE

REDUCE DRAM CYCLE TIMES WITH EXTENDED DATA-OUT

INTRODUCTION

As system speeds increase, DRAM manufacturers are developing methods to decrease the cycle times of DRAMs. The most common version of DRAM is FAST PAGE (FP) but the addition of a feature known as extended data-out (EDO) may become more common because it allows shorter page cycle times with only a minor functional change from FP. Because the device with EDO doesn't turn off the output drivers when CAS goes HIGH, it can have a shorter cycle time than FP.

EDO OFFERS ADVANTAGES

- It has a shorter PAGE READ cycle time than either FP or SC devices.
- Data is valid on the falling edge of CAS, so the designer can use that edge to strobe data.
- A 70ns EDO device has the same PAGE READ cycle time as a 40ns FP DRAM.
- Implementing EDO in place of FP devices in a system can be as easy as knowing when the bus needs to be deactivated and using OE or WE instead of CAS to accomplish it.

This article first covers some basic differences between FP and EDO during a PAGE READ cycle. Then a comparison of cycle times between FP and EDO is done, followed by a few examples under different address setup conditions. When moving from a PAGE READ into a PAGE WRITE, the timing differs slightly between FP and EDO; this difference is discussed. Finally, the issues involved when replacing an FP device with an EDO device are addressed.

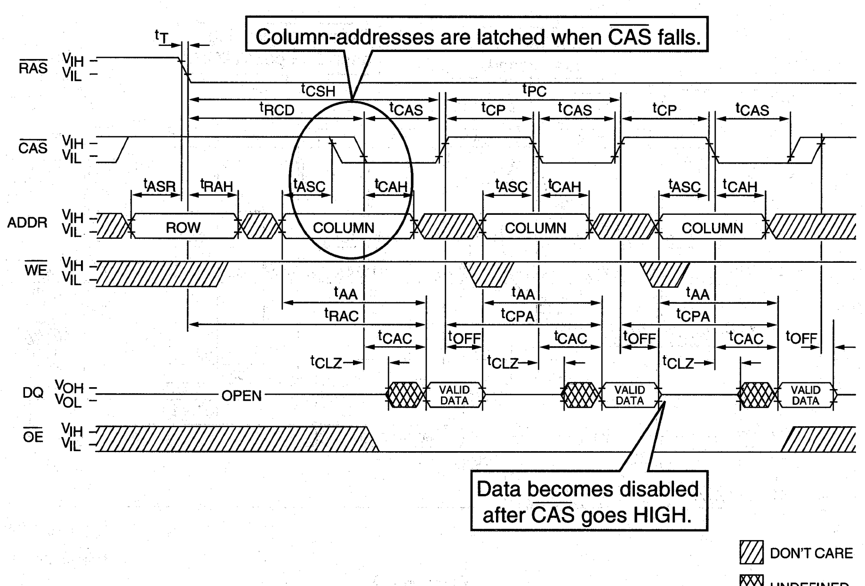

Figure 1
FP READ CYCLE

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BASIC DESCRIPTION

FP and EDO allow fast data operations within a row. The differences are in the deactivation of data-out when CAS goes HIGH and the operation of OE and WE. The following section highlights differences between the fP and EDO when reading within a page.

FP MODE

Characteristics:

- The column-address is latched when CAS falls.
- The output drivers are turned off when CAS goes HIGH.
- Minimum FP READ cycle time is $^tPC = {}^tCPA + {}^tT$, $({}^tCPA = {}^tAA + {}^tT)$

The cycle begins with RAS strobing-in a row address, followed by CAS strobing-in a column-address. To continue to access columns within that row, CAS is toggled as addresses change.

Figure 1 shows a typical FP READ cycle. The column-address is latched into the part when CAS falls, so column-address setup and hold times are referenced to the falling edge of CAS. Notice ^tOFF; this specification tells you that CAS going HIGH turns off the output drivers.

EDO

Characteristics:

- The column-address is latched when CAS falls.
- The output drivers are not turned off when CAS goes HIGH.
- Minimum EDO read cycle time is determined by the greater of the two equations below.

Equation 1: $^tPC = {}^tCAS + {}^tCP + 2{}^tT$
Equation 2: $^tPC = {}^tCPA - ({}^tCP + {}^tT)$

- OE and CAS work together to enable and disable the outputs.
- WE can disable the outputs.

EDO allows fast access within a row and uses CAS to latch the column-address, as does FP, but does not turn off the output when CAS goes HIGH. This last feature allows EDO to cycle faster than FP because the user does not have to wait for valid data to appear before starting the next access. In other words, data can appear after CAS has been pulled HIGH, and it will stay valid for 5ns after CAS transitions LOW again (^tCOH), as shown in Figure 2. The output will deactivate when both RAS and CAS are

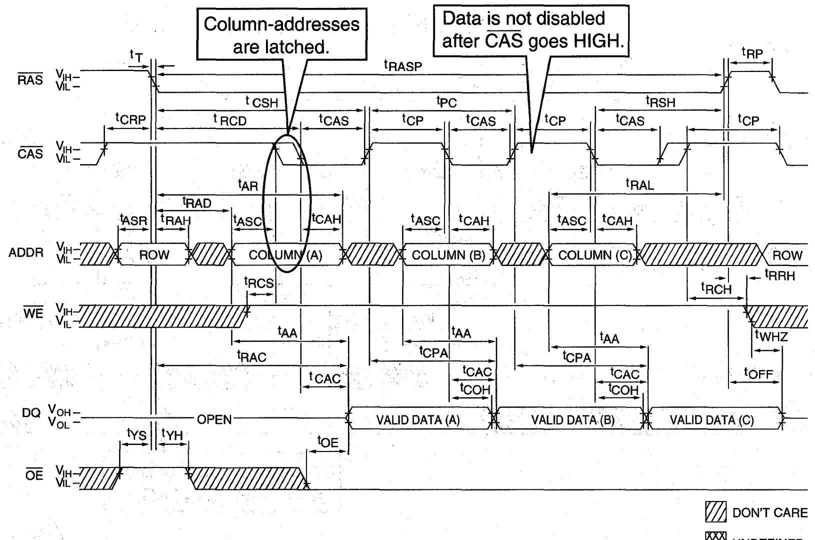

Figure 2
FP READ WITH EDO

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HIGH, so ^{t}OFF will now be referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last. $\overline{OE}$ will also deactivate the outputs, as shown in Figure 3. In order to accomodate systems where $\overline{OE}$ is tied LOW, $\overline{WE}$ now has the ability to turn off the output drivers as well (see Figure 4).

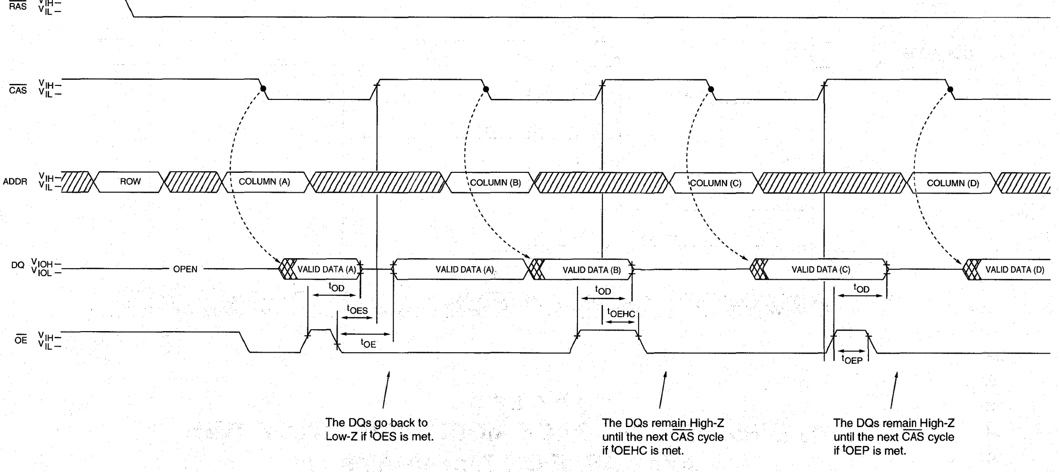

Figure 3
OUTPUT ENABLE AND DISABLE USING $\overline{OE}$

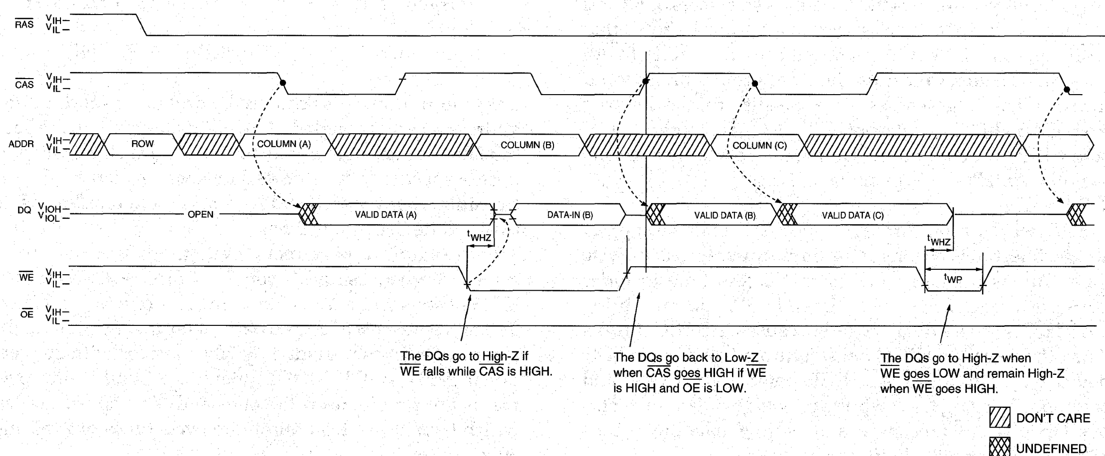

Figure 4
OUTPUT DISABLE USING $\overline{WE}$

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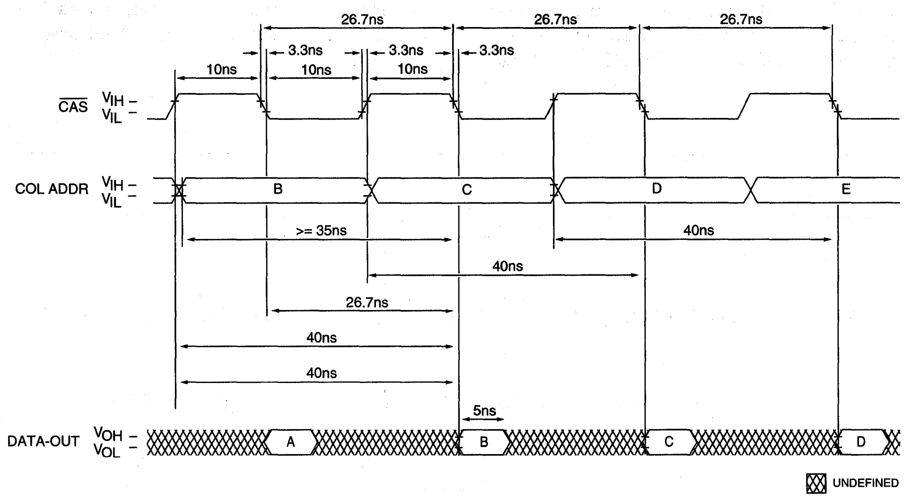

Figure 5
EDO MINIMUM FAST-PAGE-MODE READ CYCLE TIME AVAILABLE ON 70ns VRAMs

PAGE READ CYCLE TIMES

This section examines the different cycle times of FP and EDO to see how they are generated. Figure 1 shows that $\overline{CAS}$ must stay LOW until data-out becomes valid (if $\overline{CAS}$ goes HIGH before valid data, then the output buffers would turn off). The longest access time specified for the device is from $\overline{CAS}$ HIGH to data-out (^tCPA). $\overline{CAS}$ can't go HIGH before ^tCPA, or data-out will not fire. Add a transition time to pull $\overline{CAS}$ HIGH and you have the cycle time $^tPC_{FPM} = {}^tCPA + {}^tT$.

EDO works a bit differently. ^tCPA is still the longest access time, but is no longer the limiting parameter in cycle time. This is because some of this access time includes $\overline{CAS}$ precharge ($\overline{CAS}$ HIGH time). In FP, you can't bring $\overline{CAS}$ HIGH before data is valid because $\overline{CAS}$ HIGH turns data off. Since $\overline{CAS}$ HIGH doesn't turn off data in the EDO device, you can bring $\overline{CAS}$ HIGH before data is valid and begin precharging $\overline{CAS}$ while you wait for data-out. This overlap of $\overline{CAS}$ precharge and getting data-out means ^tCPA is no longer the limiting parameter.

The theoretical minimum page-mode cycle time is determined by one of the two equations below, whichever is greater (see Figure 2).

Equation 1: $^tPC = {}^tCAS + {}^tCP + {}^tLH + {}^tHL$

Equation 2: $^tPC = {}^tCPA - ({}^tCP + {}^tHL)$

The minimum cycle is achieved by providing valid column addresses early enough that ^tAA is not limiting. In the past, transition times were assumed to be 5ns each for the purpose of specifying cycle times. However, in many cases, the transitions between 0.8 and 2.4 volts do not require 5ns, so the EDO devices allow 2.5ns.

For example, a page-mode cycle time of 26.7ns can be achieved when using Micron 70ns EDO VRAMs with a ^tCPA of 40ns when transitions are 3.3ns or less (see Figure 5). This represents a 33 to 40 percent improvement over the same cycle times provided by 70ns devices with conventional FAST PAGE MODE operation. Similar improvements are provided on the 60ns and 80ns speed grades, which have theoretical minimum cycle times of 24ns and 30ns, respectively.

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EXAMPLES: EDO AND FP

The table below compares page READ cycles of FP and EDO under two different conditions: minimum column-address setup and maximum column-address setup time. The timing diagrams for the following examples assume that RAS is already LOW, WE is HIGH and OE is LOW. A 70ns DRAM is used with the following timing:

DESCRIPTION	FP	EDO
ᵗPC (MIN)	45	30
ᵗCAS (MIN)	20	12
ᵗCLZ (MIN)	0	0
ᵗOFF	0-20	0-20
ᵗT	5	5

Figures 6 and 7 show FP and EDO cycles with plenty of address setup time. On an FP device with plenty of address setup time, we can operate at ᵗPC = 45ns (the minimum allowed), and data is valid for 5ns.

EDO under the same address setup time looks different (see Figure 5). Now the minimum cycle time is 32ns. Notice that data doesn't appear on the bus until you are already into the second access (8ns of CAS precharge for the next cycle is already completed when data appears). This is the overlap that allows the shorter cycle time. ᵗPC is 32ns and data is valid for 12ns.

Under these conditions, EDO cuts the cycle time over a FP device by 29 percent (45ns to 32ns). In addition, even with the shorter cycle time, data-out is valid for 12ns on the EDO as opposed to only 5ns on the FP device. We could get more

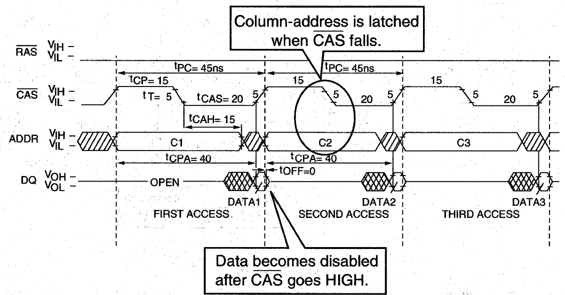

Figure 6
FP PAGE READ CYCLE WITH MAXIMUM ADDRESS SETUP
ᵗPC = 45ns; DATA VALID FOR 5ns

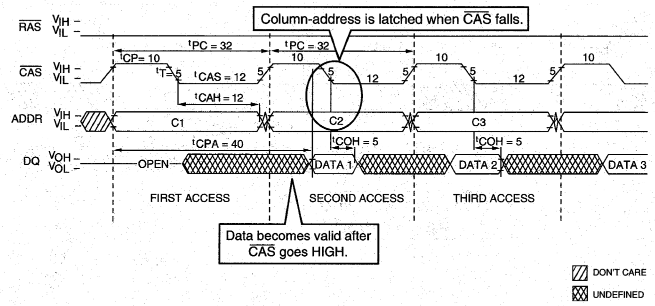

Figure 7
EDO-PAGE READ CYCLE WITH MAXIMUM ADDRESS SETUP
ᵗPC = 32ns; DATA VALID FOR 12ns

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performance by using shorter transition times on the EDO device, but we used 5ns to make the comparison between FP and EDO easily understandable.

Figures 8 and 9 show FP and EDO cycles with minimum address setup time. In this case, the address becomes valid coincident with CAS falling. For FP, data won't be valid for ^{t}AA(35ns), so CAS must be held LOW until that time (see Figure 8). Since the minimum CAS HIGH time is 10ns, the cycle time is 50ns (^{t}AA + ^{t}CP + ^{t}T). Data-out is valid for 5ns.

Looking at EDO under the same conditions, (Figure 9) it still takes ^{t}AA (35ns) after the addresses are valid to get valid data-out, but now you don't have to wait before pulling CAS HIGH. Notice that CAS has been pulled HIGH and precharge has been completed for the next cycle, before Data 1 appears on the bus. Just before data becomes valid, CAS drops and the second address is latched. Again, there is an overlap of starting one cycle and finishing the other. Now ^{t}PC = 32ns, and data-out is valid for 7ns.

In this case, EDO cycle time (32ns) is 36 percent less than the FP cycle time (50ns); EDO data is valid 2ns longer.

These examples should point out another big advantage of EDO. Not only can you operate at a shorter cycle time, but data is available longer for the system to sample. Since data is guaranteed to be valid as CAS falls, that edge may be used to sample data.

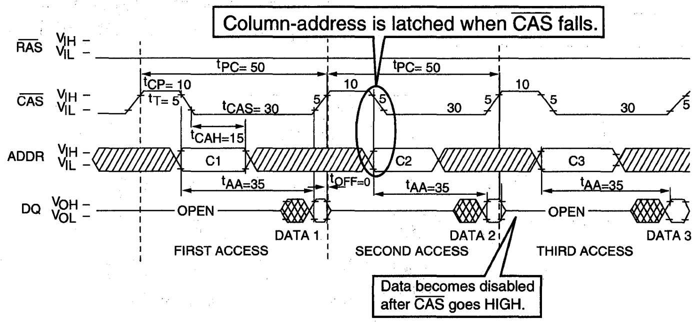

Figure 8
PAGE READ WITH MINIMUM ADDRESS SETUP
^{t}PC = 50ns; DATA VALID FOR 5ns

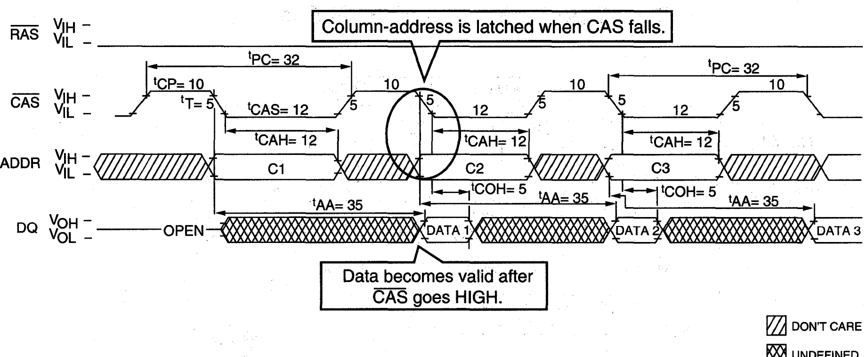

Figure 9
EDO-PAGE READ CYCLE WITH MINIMUM ADDRESS SETUP
^{t}PC = 32ns; DATA VALID FOR 7ns

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70ns EDO INSTEAD OF 40ns DRAMs

EDO can provide the FP READ speed of a 40ns DRAM. Even though a 40ns DRAM has a 40ns ^{t}RAC, the FP READ cycle time is 30-35ns, which is the same page READ cycle time as that of a 70ns EDO device.

EASY TO IMPLEMENT

An additional benefit of EDO is the ease of implementation. PAGE READ or WRITE cycle time is cut but the major difference between FP and EDO is that the FP device will stop driving data-out when $\overline{CAS}$ goes HIGH and the EDO device must have the correct combination of $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$ and $\overline{WE}$ to deactivate the output. This means that any time the designer is counting on $\overline{CAS}$ by itself to turn off the output drivers, bus contention may occur if something else tries to drive the bus. This may occur in the following situations:

- PAGE interleave memory banks
- Moving from PAGE READ directly into a PAGE WRITE (within the same page)
- Whenever anything other than the DRAM is driving the bus, and $\overline{OE}$ and $\overline{RAS}$ are LOW while $\overline{CAS}$ is HIGH

(This last case is uncommon and should not mandate a change for most systems.) Interleaved memory need only make use of $\overline{OE}$ or $\overline{WE}$ instead of $\overline{CAS}$ when turning off the output drivers; then EDO can be used in place of FP DRAMS.

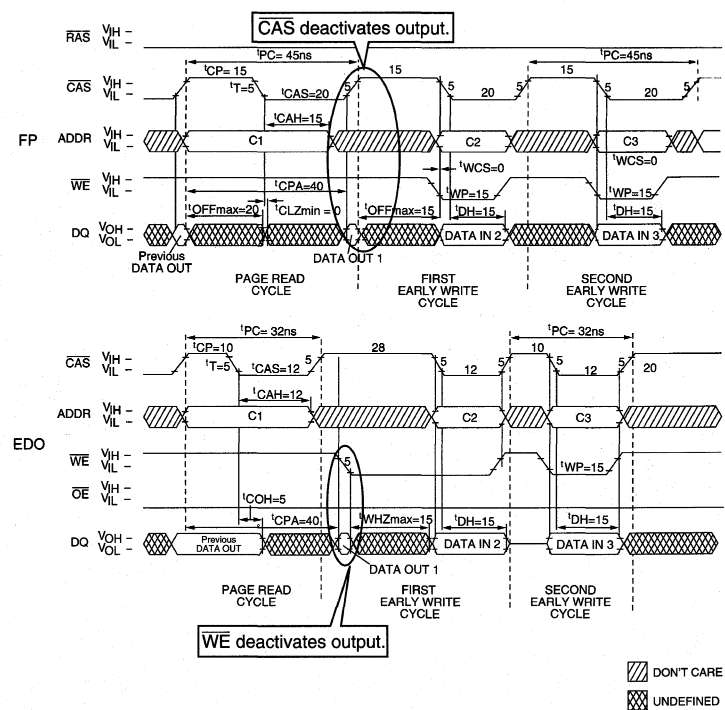

Figure 10
EXAMPLE FP AND EDO READ TO WRITE CYCLES
^{t}PC = 45ns

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READ TO WRITE CYCLES

Since $\overline{CAS}$ doesn't turn off the output devices on an EDO device, caution should be used when turning the bus around on a shared IO device. To demonstrate the difference, Figure 8 shows the transition from a PAGE READ to a PAGE EARLY WRITE on the same page. When using the FP version, $\overline{OE}$ can be tied LOW and $\overline{CAS}$ can be used to deactivate the output. Notice that $\overline{OE}$ is also tied low on the EDO device and this cycle is still possible.

SUMMARY

EDO is simply a modified FP MODE cycle and can be used in systems to increase performance. It allows system designers to improve their cycle times and system performance since data is present for a much longer time, even during short cycle times. Because each generation device has different timing limitations, be sure to consult the data sheet for exact timing.

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TECHNICAL NOTE

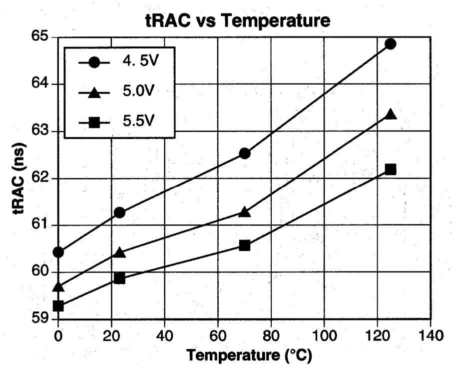
256K x 16/512K x 8 DRAM TYPICAL OPERATING CURVES

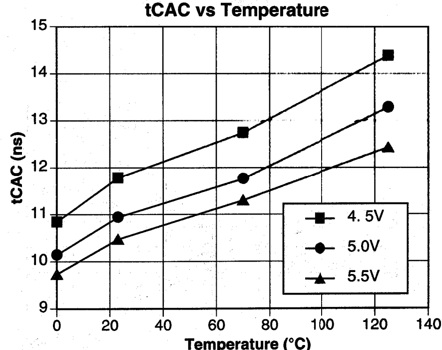
INTRODUCTION

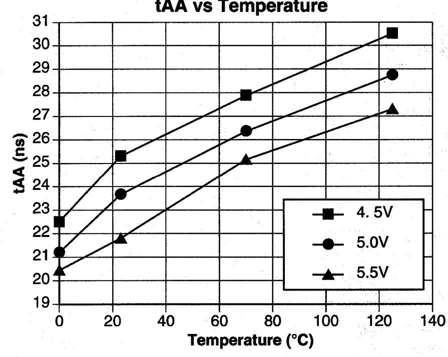
These curves represent the typical operating characteristics of Micron's 70ns 256K x 16 and 512K x 8 DRAMs. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets.

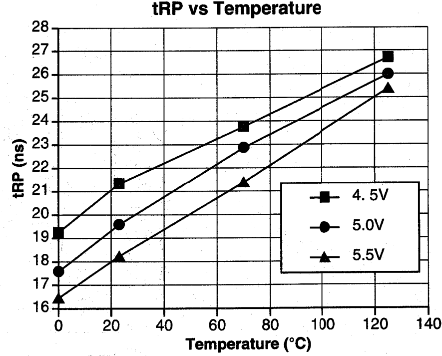
NEW TECHNICAL NOTE

256K x 16 OPERATING CURVES









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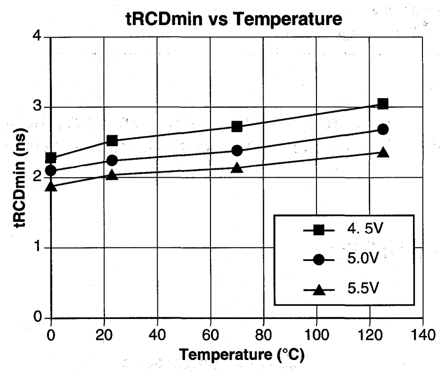
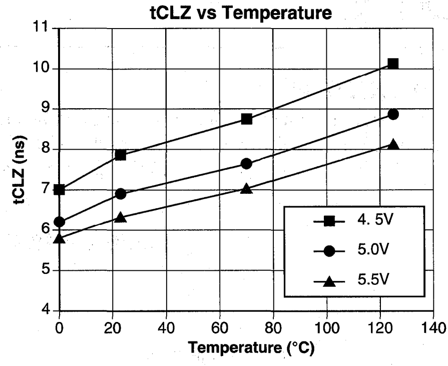
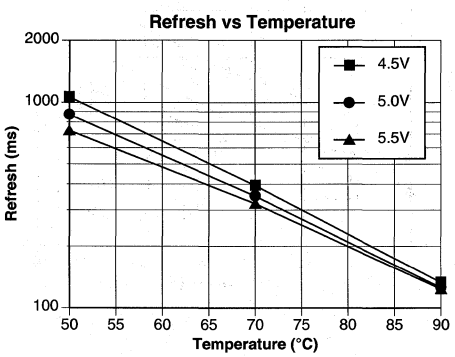
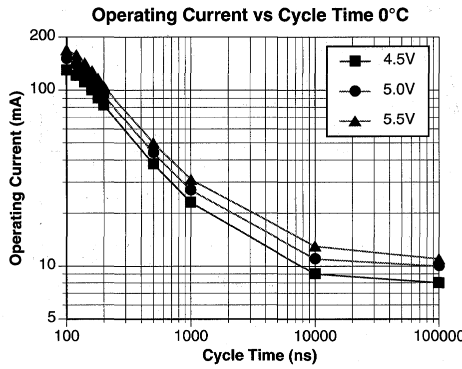
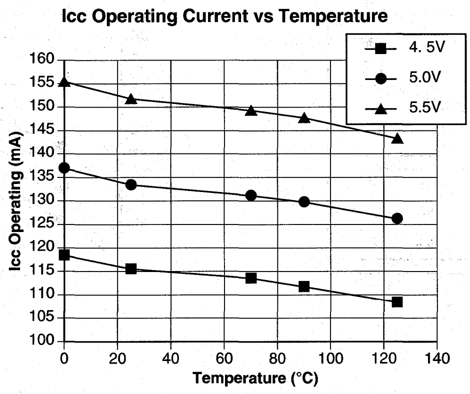
256K x 16 OPERATING CURVES (continued)











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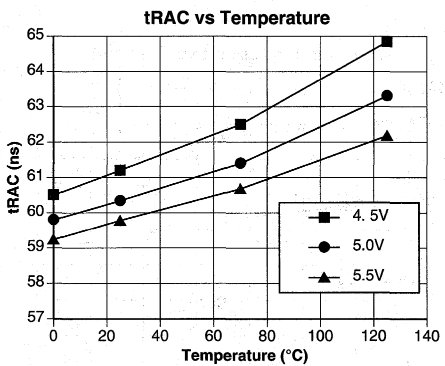
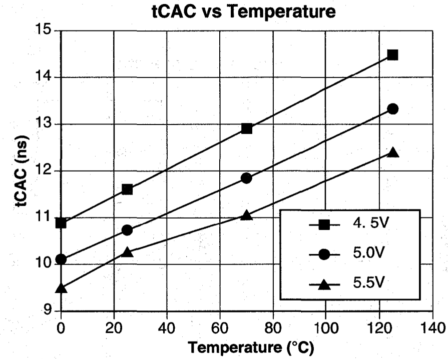
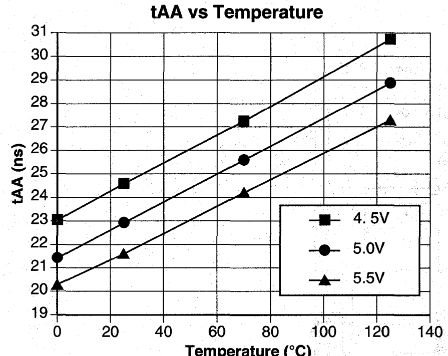
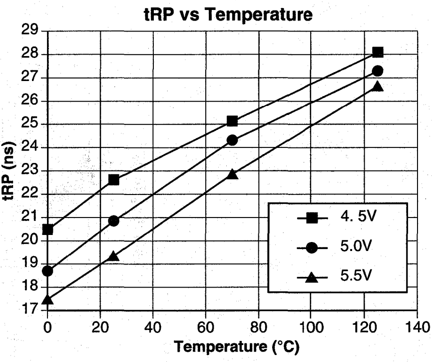
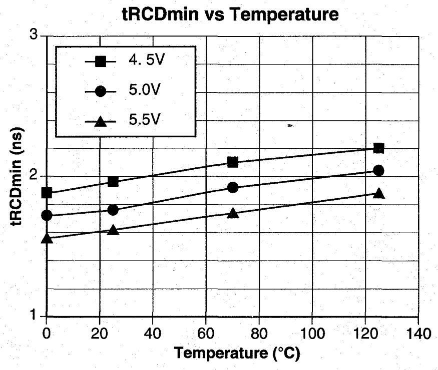
512K x 8 OPERATING CURVES

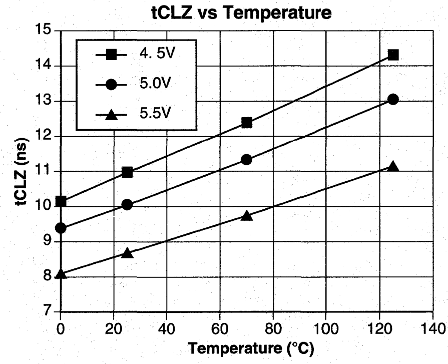












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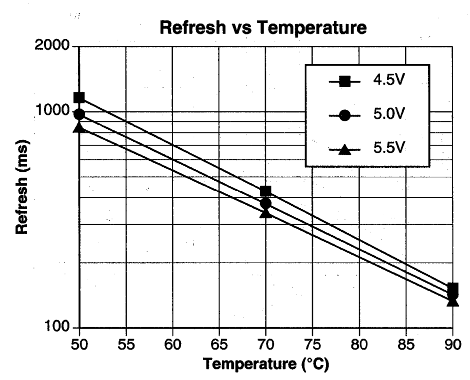
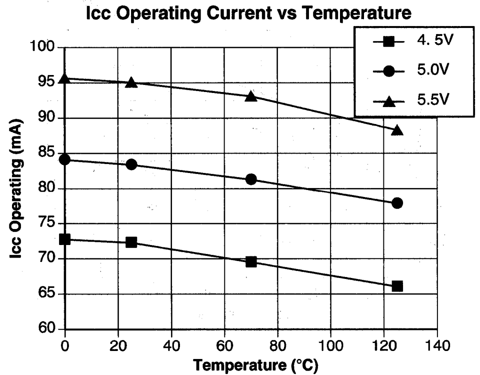
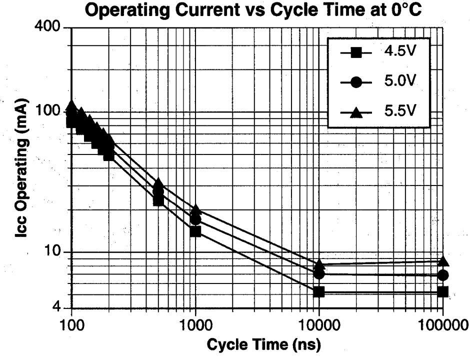
512K x 8 OPERATING CURVES (continued)







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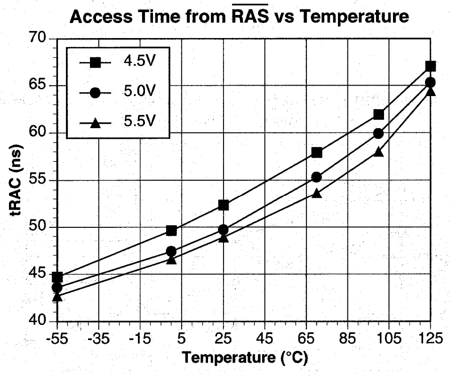
TECHNICAL NOTE

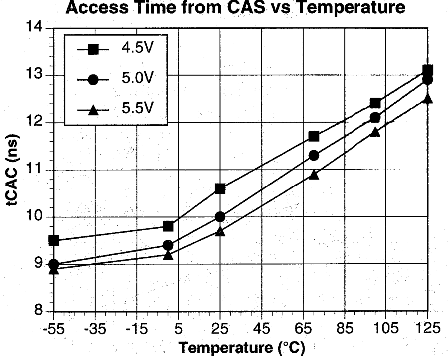
4 MEG DRAM TYPICAL OPERATING CURVES

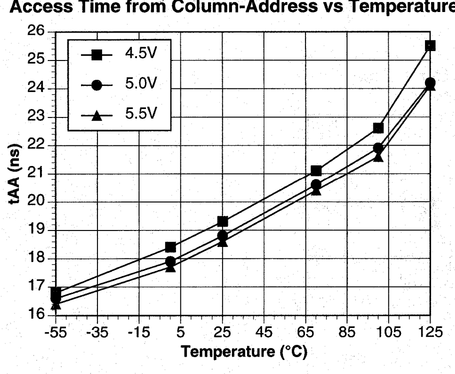
INTRODUCTION

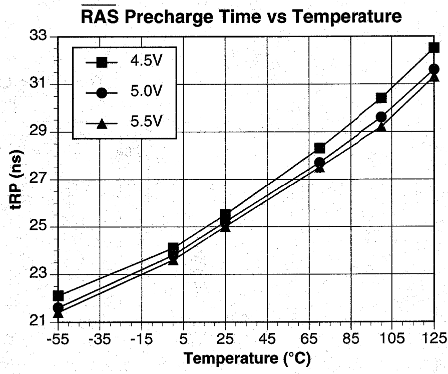
These curves represent the typical operating characteristics of Micron's 70ns 4 Meg DRAMs. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets.

5-VOLT PRODUCT DC AND AC PARAMETER PERFORMANCE









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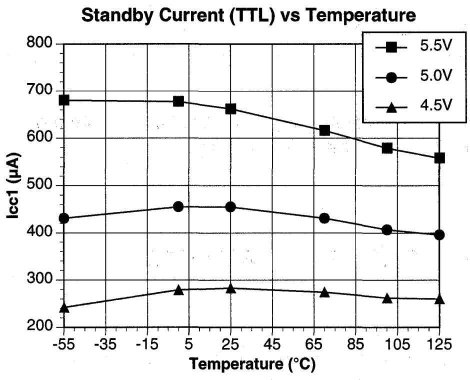
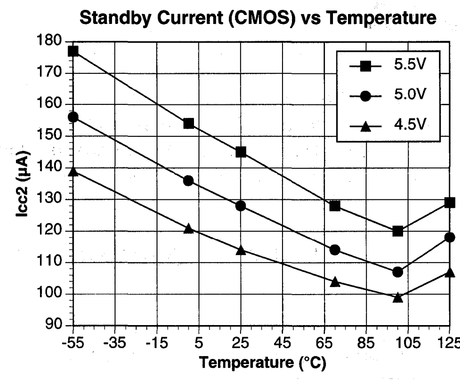
5-VOLT PRODUCT DC AND AC PARAMETER PERFORMANCE (continued)

Standby Current (TTL) vs Temperature

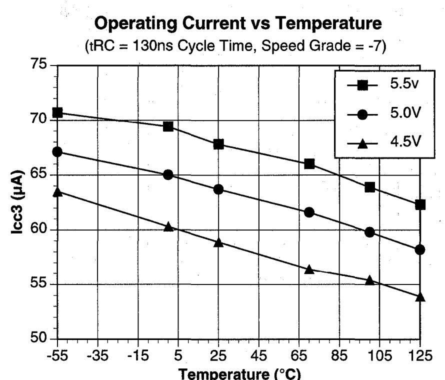


Standby Current (CMOS) vs Temperature



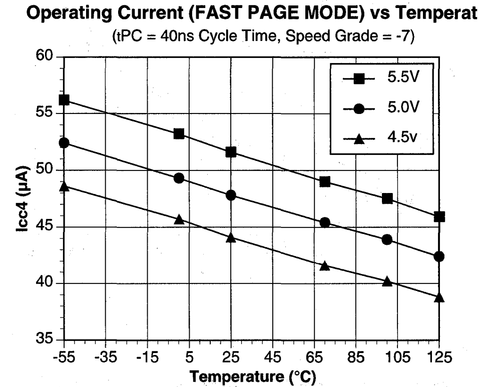
Operating Current vs Temperature

(tRC = 130ns Cycle Time, Speed Grade = -7)



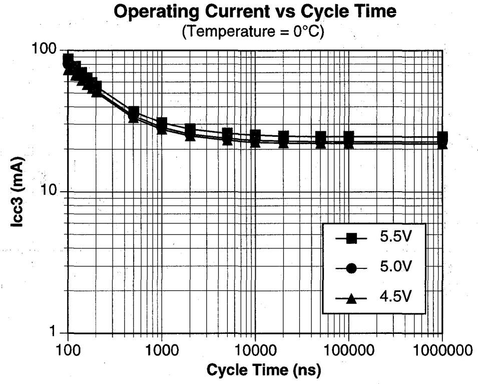
Operating Current (FAST PAGE MODE) vs Temperature

(tPC = 40ns Cycle Time, Speed Grade = -7)



Operating Current vs Cycle Time

(Temperature = 0°C)



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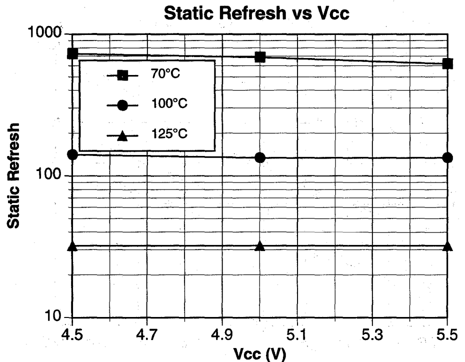
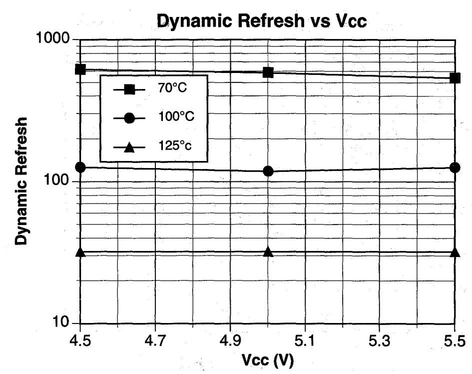
5-VOLT PRODUCT DC AND AC PARAMETER PERFORMANCE (continued)





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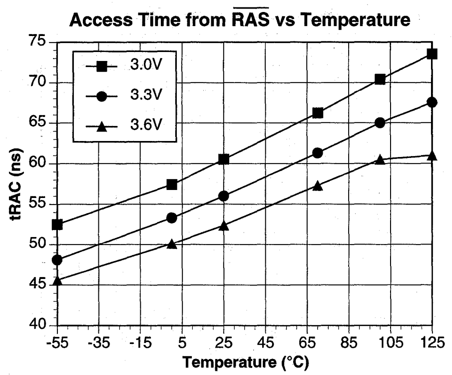
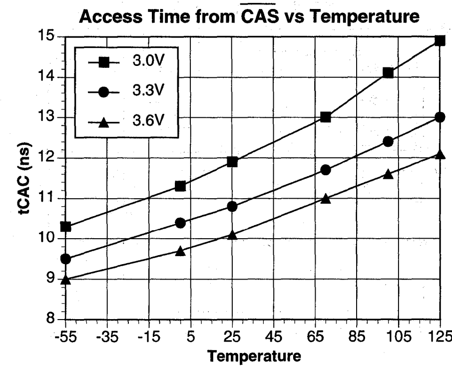
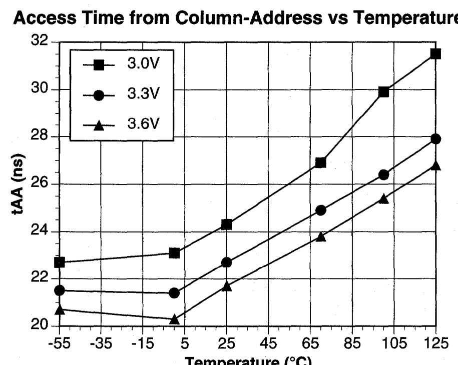
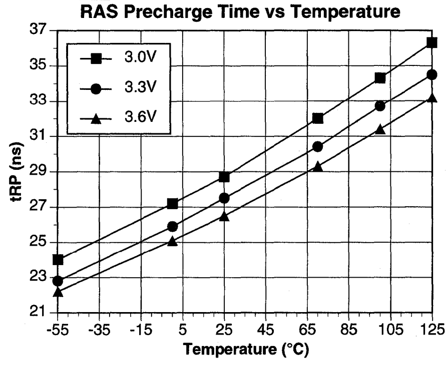
NEW TECHNICAL NOTE

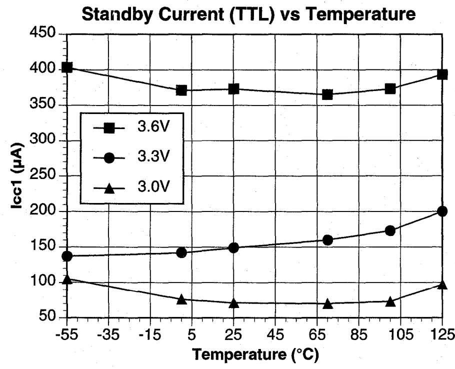
3.3-VOLT PRODUCT DC AND AC PARAMETER PERFORMANCE

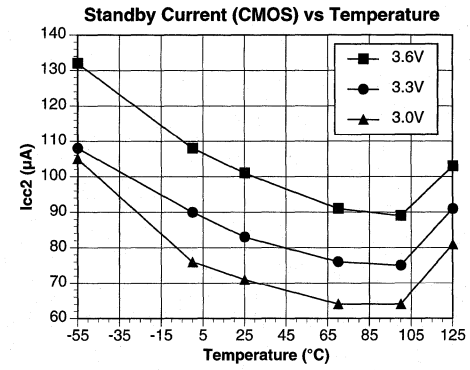












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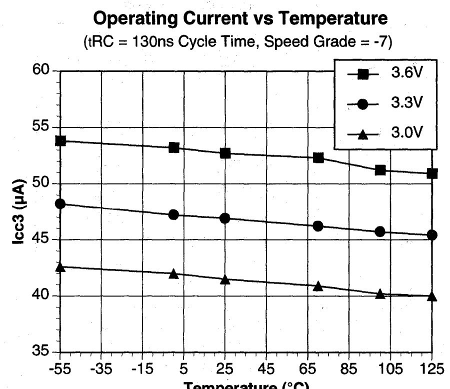
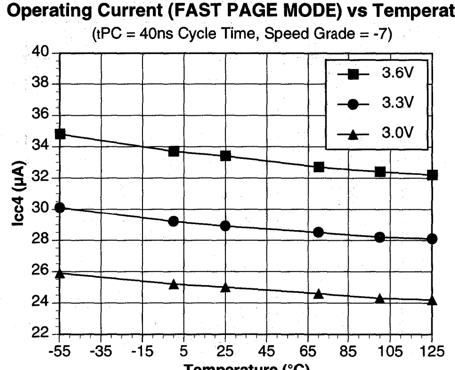
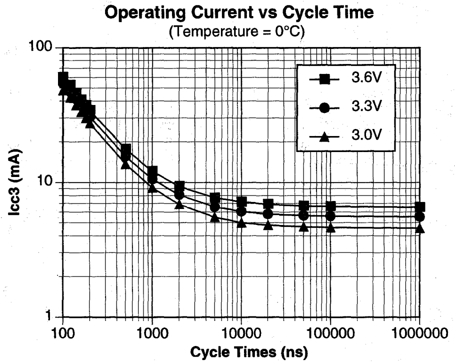
3.3-VOLT PRODUCT DC AND AC PARAMETER PERFORMANCE (continued)







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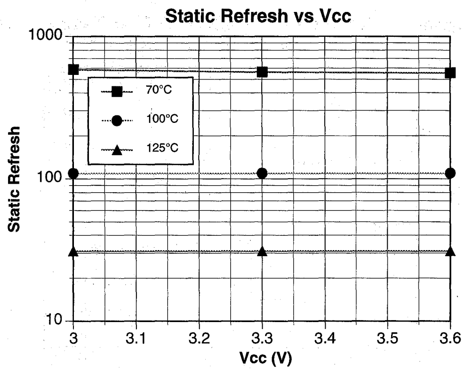
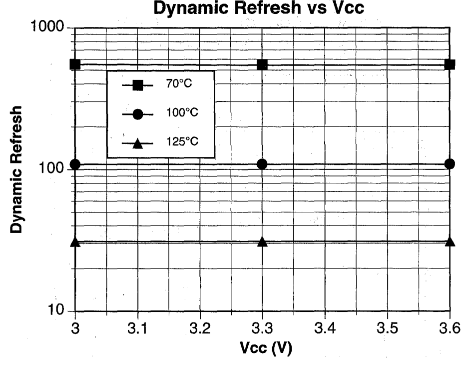
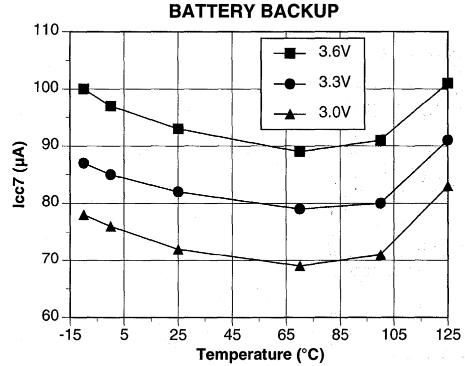
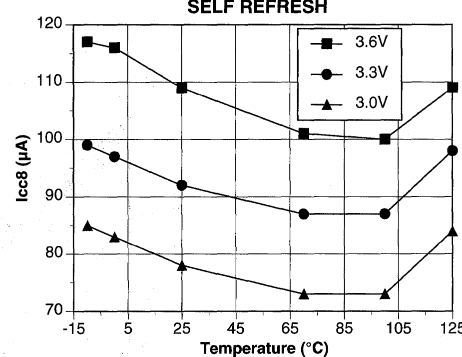
3.3-VOLT PRODUCT DC AND AC PARAMETER PERFORMANCE (continued)









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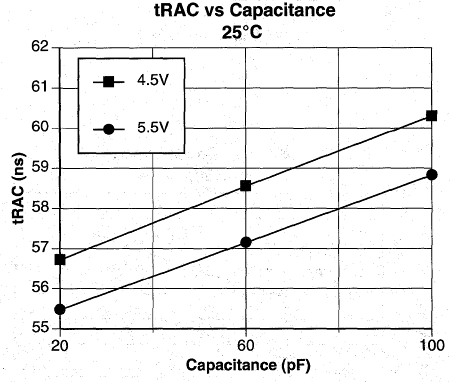
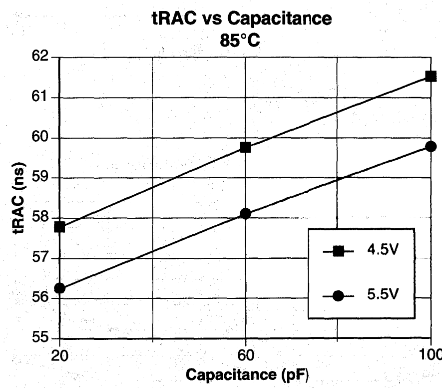
TECHNICAL NOTE

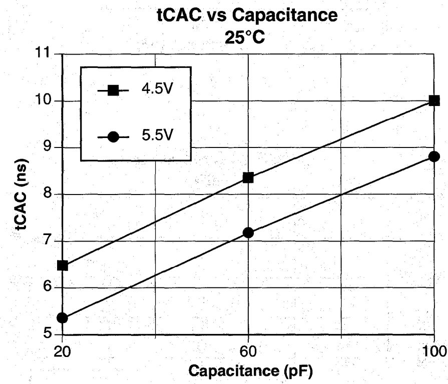
4 MEG DRAM—ACCESS TIME vs CAPACITANCE

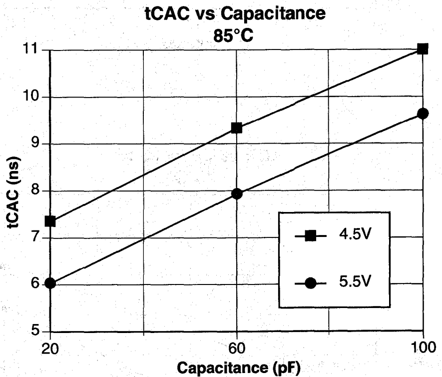
INTRODUCTION

These curves for the 4 Meg DRAM show typical access times with different capacitive loading. For worst-case design limits, the system designer should refer to the individual data sheets.









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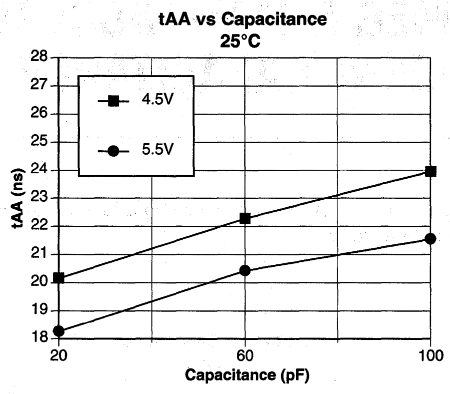

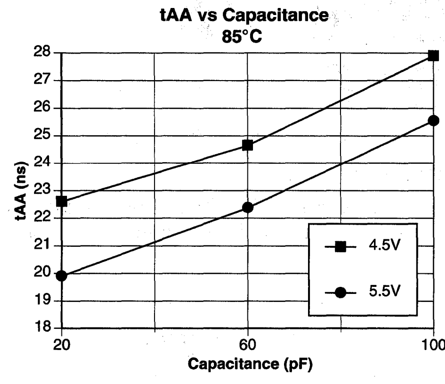

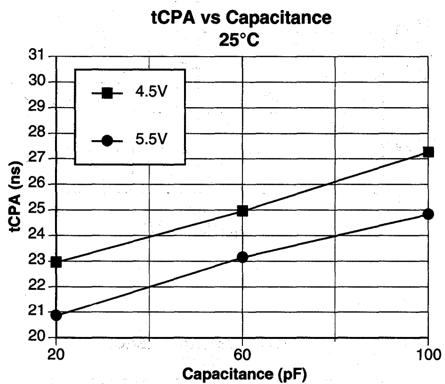

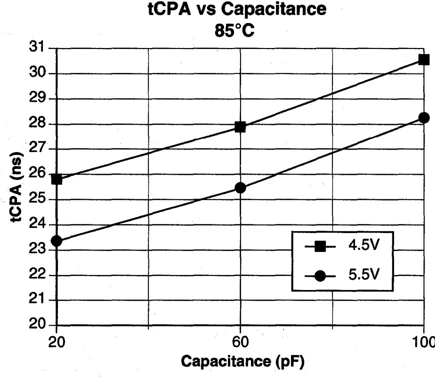

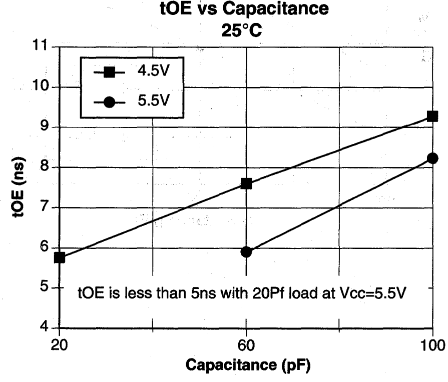

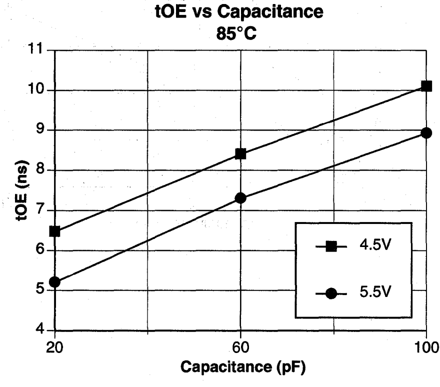

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TECHNICAL NOTE

MT3D19 AND MT9D19 COMPATIBILITIES

INTRODUCTION

Converting from the nine-chip 1 Meg x 9 memory module (MT9D19) to the three-chip 1 Meg x 9 memory module (MT3D19), introduces four potential system incompatibilities. The incompatibilities involve CAS-BEFORE-RAS (CBR) REFRESH, test mode entry, power-up and refresh addressing. Understanding and providing for these incompatibilities will offer designers and system users better compatibility between these two versions of the 1 Meg x 9, 30-pin memory module.

REFRESH

The most commonly used refresh mode of the MT9D19 is the CBR REFRESH cycle. The CBR for the MT9D19 specifies the WE pin as a "don't care" (Figure 1). The MT3D19, on the other hand, specifies the CBR REFRESH mode with the WE pin held at a voltage HIGH level (Figure 2). A CBR cycle with WE LOW will put the MT3D19 into the JEDEC-specified test mode (WCBR). Therefore, existing systems looking at migrating from the MT9D19 to the MT3D19 should insure that WE is HIGH for CBR REFRESH operation (Figure 3).

TEST MODE

A CBR cycle with WE LOW will put the MT3D19 into the JEDEC standard test mode. Since the edge connector of the MT9D19 does not supply the required connection to the Test Function pin of the DRAMs, the MT9D19 cannot be placed into test mode.

POWER-UP

The MT3D19 JEDEC test mode constraint may introduce another problem. The MT9D19 POWER-UP cycle requires a 100µs delay followed by any eight RAS cycles. The MT3D19 POWER-UP cycle is more restrictive in that eight RAS ONLY or CBR REFRESH (WE held HIGH) cycles must be used. The restriction is needed since the MT3D19 may power-up in the JEDEC-specified test mode and must exit out of the TEST MODE. The only way to exit the JEDEC TEST MODE is with either a RAS ONLY or a CBR REFRESH cycle (WE held HIGH). Hence those designs that plan to use both modules need to execute eight RAS ONLY or CBR (WE held HIGH) REFRESH cycles after the required 100µs delay from power on.

REFRESH ADDRESSING

To retain memory cell data in its correct state, the MT9D19 requires executing any RAS REFRESH cycle (READ, WRITE, RAS ONLY, CBR, OR HIDDEN) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence. Compare this to the MT3D19, which requires executing any RAS REFRESH cycle (READ, WRITE, RAS ONLY, CBR, OR HIDDEN) so that all 1,024 combinations of RAS addresses A0-A9 are executed at least every 16ms, regardless of sequence. The MT3D19 must have RAS addresses A0-A9 as part of the memory cell data refreshing scheme, whereas the MT9D19 requires only RAS addresses A0-A8. This requires that those designs planning to use both the MT9D19 and MT3D19 modules must be able to refresh all combinations of 1,024 addresses (A0-A9) at least every 16ms.

SUMMARY

In summary, a system that is compatible with both the MT3D19 and MT9D19 modules must support the following:

- The CBR REFRESH must require WE to be HIGH.
- The eight RAS wake-up cycles must be either RAS ONLY or CBR REFRESH cycles (WE held HIGH).
- To retain memory cell data in its correct state, the system must have RAS addresses A0-A9 as part of the memory cell data refreshing scheme over the 16ms period (i.e. 15.6µs address to address refresh rate).

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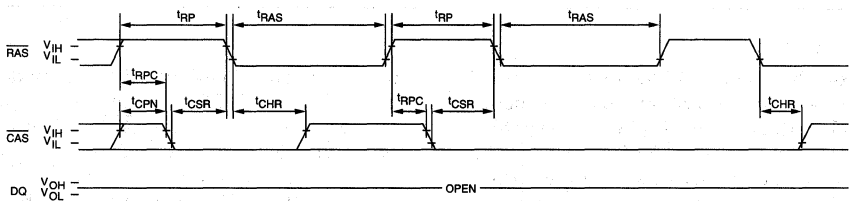
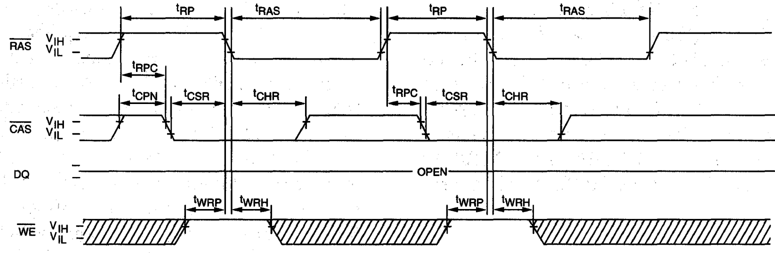
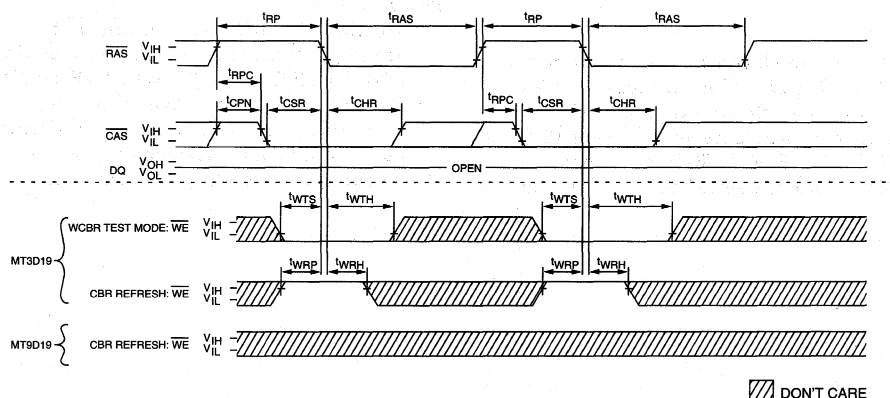
MT9D19
CBR REFRESH CYCLE
(WE = DON'T CARE)



MT3D19
CBR REFRESH CYCLE



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR



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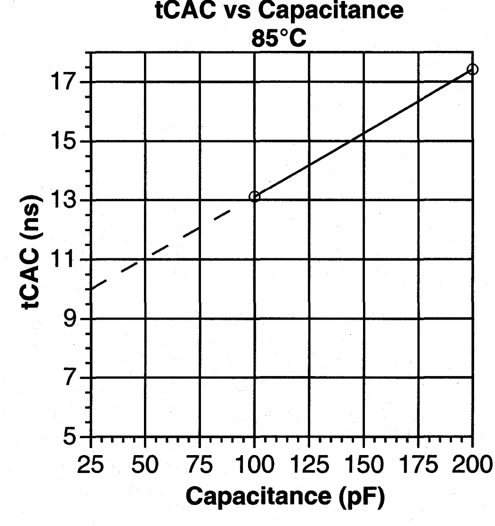
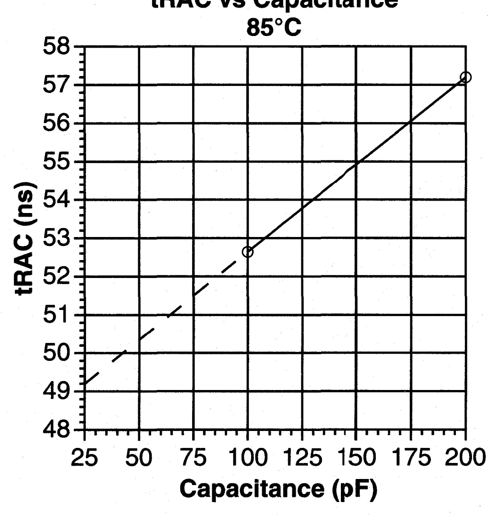
TECHNICAL NOTE

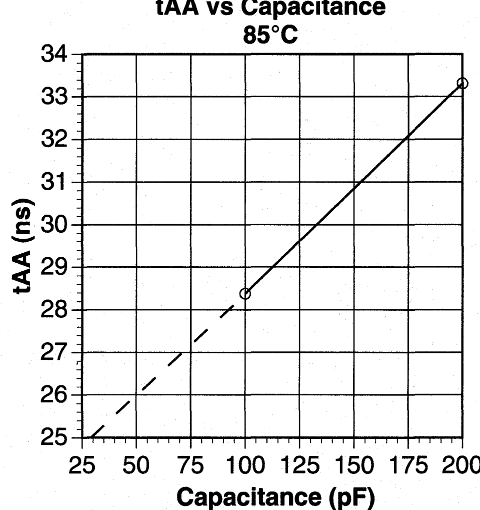
256K x 16/512K x 8—ACCESS TIME vs CAPACITANCE

INTRODUCTION

These curves for the 256K x 16 DRAM show typical access times at Vcc = 4.5V with different capactive loading. For worst-case design limits, the system designer should refer to the individual data sheets.







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TECHNICAL NOTE

CONTROLLER SUPPORT FOR EXTENDED DATA-OUT DRAMs

INTRODUCTION

The advent of extended data-out (EDO) DRAMs has given system designers the possibility of greatly improving the performance of the memory subsystem. EDO functionality provides faster PAGE MODE cycle times by allowing data to remain or appear on the outputs after $\overline{CAS}$ has gone HIGH (please refer to technical note TN-04-21, "Reduce DRAM Cycle Times with Extended Data-Out"). A variety of controller manufacturers are planning to support EDO DRAMs in their graphics controllers and PC chip sets. This technical note lists a few manufacturers of controllers or chip sets who plan to support the EDO feature on DRAM products.

MICRON DEVICES

Micron has a full range of EDO DRAMs slated to support EDO requirements.

MICRON DEVICES

PART NUMBER	CONFIGURATION	VCC	FEATURES
MT4C16270	256K x 16	5V	2 CAS, Symmetrical Addressing
MT4LC16270	256K x 16	3.3V	2 CAS, Symmetrical Addressing
MT4LC4007	1 Meg x 4	3.3V	Standard or SELF REFRESH versions
MT4LC4M4E9	4 Meg x 4	3.3V	4K rows, standard or SELF REFRESH versions, 300mil
MT4LC2M8E7	2 Meg x 8	3.3V	2K rows, standard or SELF REFRESH versions, 300mil

CONTROLLERS

Several controller manufacturers have already committed support or plan to support EDO DRAMs and have provided the information listed below. Call Micron DataFax at 208-368-5800 for revised lists of companies that have been identified and confirmed.

CONTROLLER MANUFACTURERS

COMPANY	PART NUMBER	NOTES	PHONE NUMBER
• Chips & Technologies	C & T is currently supporting EDO DRAMs, as well as planning support in future products.		408-434-0600 ext. 4232
• Cirrus Logic	GD5429	EDO DRAM support up to 2MB of memory Support for 256K x 16 EDO 32-bit DRAM bus interface Samples 1Q94	510-623-8300
	GD5430	EDO DRAM support up to 2MB of memory Support for 256K x 16 EDO 64-bit DRAM bus interface Samples 1Q94	

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CONTROLLER MANUFACTURERS (continued)

COMPANY	PART NUMBER	NOTES	PHONE NUMBER
• S3	Vision864	EDO DRAM support up to 4MB of memory Support for 256K x 16 EDO DRAM 64-bit DRAM bus interface PCI and local bus support Samples 4Q93, Product 1Q94	408-980-5401
• VLSI	VLSI has plans to support EDO DRAMs with future products.		
• Xtechnology	Xtechnology has plans to support EDO DRAMs in 1994.	EDO DRAM support 64-bit DRAM bus interface	408-986-5000

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TECHNICAL NOTE

88-PIN DRAM CARDS

INTRODUCTION

Just as SIMMs began a new period in memory placement and packaging in the 1980s, the 88-pin DRAM card promises to have an equal impact on the industry in the 1990s. The 88-pin DRAM card combines the architecture of a SIMM with an memory card form factor to create a high density, easy-to-use memory device. No longer do end-users have to disassemble their systems and risk ESD damage to add more SIMM modules or memory boards. Finally, a sensible approach to memory packaging has arrived.

For engineers, Micron's 88-pin DRAM cards offer a significant improvement in the way system designers manage main and add-in memory. DRAM memory cards require less system interface logic, they pack more memory into a given area than SIMM modules and they are better able to withstand more use and abuse than contemporary memory upgrade schemes. All this functionality is contained in a convenient, portable and standardized package.

Standards for the 88-pin DRAM card have been jointly ratified by the three major standard-setting bodies: PCMCIA, JEDIA and JEDEC. As a companion to the 68-pin memory card, or by itself, the 88-pin DRAM card will enhance your product design or offerings.

DRAM cards provide a rigid and durable enclosure for the printed circuit board and memory devices contained within. The card's physical dimensions are 2.126 ±0.004 inches wide by 3.37 ±0.004 inches long by 0.129 ±0.004 inches thick, which is about the same dimension as a credit card, though three times its thickness.

Once assembled, the strength of the DRAM card surpasses that of SIMM modules. Moreover, since the card's components are not subjected to direct physical contact by the user, it can withstand casual, even abusive, handling much better than a SIMM module. When a SIMM module is installed, removed or transported, there is a risk of inflicting damage due to ESD. The card is made with a conductive plastic that allows static charges to be safely dissipated to the ground pins via a High-Z path.

DRAM cards are designed to ease facilitation. Though the DRAM cards appear to function like 72-pin SIMM modules, significant differences favor the DRAM card. For example, the DRAM card provides its own buffering for its control lines, relieving the system board. Furthermore, buffering enhances system performance, both from noise reduction and reduced capacitive loading of the control lines.

The DRAM cards are preferable to SIMMs in small profile notebook and palmtop computers, because the cards offer a twofold improvement in board area usage. Proper choice of receptacle connector for the system board provides the ability for hot insertion or removal, which is impossible for a SIMM module. And the DRAM card's size and ruggedness make it ideal for mainframe or industrial applications.

Table 1
MEMORY ADDRESS RANGE

DRAM ADDRESS SPACE PER BANK	MEMORY ADDRESS RANGE					
	PRESENCE-DETECT BITS					TOTAL MEMORY SIZE
	PD1	PD2	PD3	PD4	PD5 = 0	PD5 = 1
no card installed	1	1	1	1	n/a	n/a
256K	0	0	0	0	1MB	2MB
512K	1	0	0	0	2MB	4MB
1 Meg	0	1	0	0	4MB	8MB
2 Meg	1	1	0	0	8MB	16MB
4 Meg	0	0	1	0	16MB	32MB
8 Meg	1	0	1	0	32MB	64MB
16 Meg	0	1	1	0	64MB	128MB

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PRESENCE-DETECT DEFINITIONS FOR THE 88-PIN DRAM CARD

It is necessary to clarify the presence-detect definitions for the 88-pin DRAM cards. The eight presence-detect pins are divided into four groups, consisting of memory size (four bits), number of DRAM banks (1 bit), DRAM access timing (two bits) and refresh control (1 bit). As shown in Table 1, presence-detect bits are defined as 0 = ground, 1 = open.

Presence-detect bits PD1, PD2, PD3 and PD4 relate to the byte size of the card or its memory address range. The PD5 presence-detect indicates the number of memory banks present on the card. The card will be provided with either one or two banks (32- and 36-bit versions) or two or four banks (16- and 18-bit versions).

For 32- and 36-bit applications, PD5's definition relates to whether one or two banks are present. Each bank is defined by two $\overline{\text{RAS}}$ lines. In other words, both $\overline{\text{RAS}}$ lines should be activated simultaneously for a 32- and 36-bit word access. When PD5 = 0, there is one bank present, activated by $\overline{\text{RAS0}}$ and $\overline{\text{RAS2}}$. When PD5 = 1, there are two banks present. Bank 1 is activated by $\overline{\text{RAS0}}$ and $\overline{\text{RAS2}}$ while Bank 2 is activated by $\overline{\text{RAS1}}$ and $\overline{\text{RAS3}}$.

For 16- or 18-bit applications, PD5's definition relates to whether two or four banks are present. Each bank is defined by a single $\overline{\text{RAS}}$ lines. When PD5 = 0, two banks are present, activated by $\overline{\text{RAS0}}$ and $\overline{\text{RAS2}}$. When PD5 = 1, two additional banks are present, activated by $\overline{\text{RAS1}}$ and $\overline{\text{RAS3}}$. A logical progression within the system's address space would be $\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$, $\overline{\text{RAS1}}$ and $\overline{\text{RAS3}}$ in that order. For a 36-bit data bank interpreted as an 18-bit card, $\overline{\text{RAS}}$ relates to the data bus as shown in Table 2.

The PD6 and PD7 presence-detects indicate the access time of the card from $\overline{\text{RAS}}$ true to data-out. They are defined in Table 3.

The PD8 presence-detect is related to the refresh type of the card, either SELF REFRESH when PD8 = 0, or an extended refresh when PD8 = 1. Presently, all DRAM cards will leave PD8 open, indicating that the system should provide refreshing, preferably a $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ type of refresh. This allows an address-independent refresh, which allows interchangeability among different card types.

Table 2
$\overline{\text{RAS}}$ RELATION TO DATA BUS

$\overline{\text{RAS0}}$	D0-D17	Bank 1
$\overline{\text{RAS1}}$	D18-D36	Bank 2
$\overline{\text{RAS2}}$	D0-D17	Bank 3
$\overline{\text{RAS3}}$	D18-D36	Bank 4

Table 3
DATA-OUT ACCESS TIME

ACCESS TIME	PD7	PD6
100ns (or 50ns for future cards)	0	0
80ns	0	1
70ns	1	0
60ns	1	1

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Table 4
32-BIT PRODUCT OFFERINGS

PRODUCT NUMBER (32-BIT SERIES)	MEMORY SIZE (MB)	WORD LENGTH (BITS)	POWER SUPPLY	SPEED
MT8D88C132-xx	4	16, 32	5V	60-80ns
MT8D88C132V-xx	4	16, 32	3.3V	70-100ns
MT16D88C232-xx	8	16, 32	5V	60-80ns
MT16D88C232V-xx	8	16, 32	3.3V	70-100ns
MT8D88C432-xx	16	16, 32	5V	60-80ns
MT8D88C432V-xx	16	16, 32	3.3V	60-80ns
MT16D88C832-xx	32	16, 32	5V	60-80ns
MT16D88C832V-xx	32	16, 32	3.3V	60-80ns

PRODUCT OFFERING

DRAM cards are offered through Micron. The current product spectrum provides memory sizes from 4 MB to 32 MB with x16/x32 data path, and both 5V and 3.3V operation. Micron's product offering is shown in Table 4. The series is provided with speed grades from 80ns to 60ns. This is specified with a -8, -7 or -6 suffix to the part number where "xx" is shown. The cards use low-power, extended-refresh DRAMs. Cards using a 3.3V supply have their part number appended with a "V" option.

In addition, all versions of the standard DRAM card are available in a two-inch-long, bufferless version. Contact Micron for further details

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SERVICES

Micron stands ready to help customers who wish to enter the IC DRAM card market with proprietary solutions. Our staff engineers are well-versed in the design of boards for the entire PCMCIA/JEDEC/JEIDA arena. If one of our standard products does not meet your current needs, we are ready and able to design a custom solution for you.

For customers desiring a standard product under private label, Micron can supply current products labeled and marked in virtually any manner the customer wishes. Simply supply us with the desired artwork and markings—Micron will do the rest.

Often overlooked by companies considering entrance into the DRAM card market are the mechanical considerations. Micron has invested considerable time and effort into developing superior card frames, covers and components. Our custom design services break down the significant entry barriers to this burgeoning market and will get your product to market on time and on budget. Design services include:

- Design from concept
- Schematic capture
- Board layout
- Enclosure design
- Thermal and signal noise analysis
- Custom marking
- Comprehensive testing
- Connector redesign
- ASIC solutions
- Packaging solutions

Applications engineering assistance is also available from 8 a.m. to 5 p.m. Mountain Time by calling 208-368-3900.

The DRAM card arena is very fast-paced. Product development and introduction will quickly outdate current information. When contemplating a design in this arena, please call us for the latest product datasheets and design guidelines.

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OVERVIEW

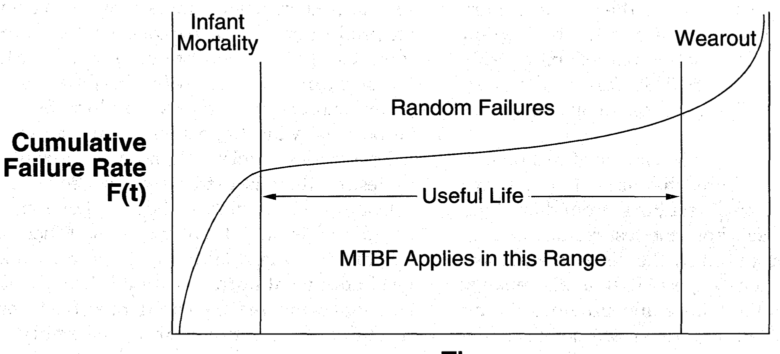
Product reliability is a product's ability to function within given performance limits, under specified operating conditions over time. This section contains a brief overview of some of the issues that affect the reliability of IC devices and briefly describes Micron's reliability program.

For a more in-depth discussion of reliability, please refer to Micron's Quality/Reliability literature.

RELIABILITY GOALS

When we discuss reliability goals of semiconductor ICs, we typically refer to the traditional reliability curve of component life. The reliability curve, or "bathtub curve," appears below, where h(t) is the hazard rate or the probability of a component failing at t_0+1 in time if it has survived at time t_0.

The reliability curve in Figure 1 is divided into three segments: infant mortality, random failures and wearout. The term "infant mortality" refers to those ICs that would fail early in their lives due to manufacturing defects. To screen out such failures, Micron evaluates all our products using intelligent burn-in. This unique AMBYX® intelligent burn-in/test system developed by Micron is described in the following section.



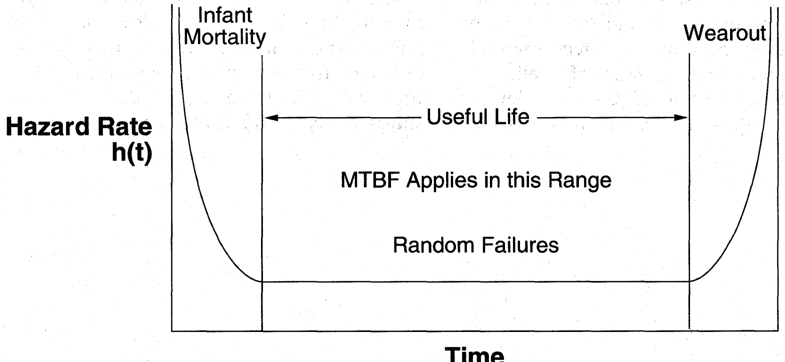


Figure 1
RELIABILITY CURVE

RELIABILITY

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MICRON'S AMBYX® INTELLIGENT BURN-IN AND TEST SYSTEM

Burn-in refers to the process of accelerating failures that occur during the infant mortality phase of component life to remove the inherently weaker devices. The process has been regarded as critical for ensuring product reliability since the beginning of the semiconductor industry. To effectively screen out infant mortalities, Micron believes it is critical to functionally test devices several times during the burn-in cycle without removing them from the burn-in oven. In 1986, when we were unable to find a system that met our requirements, we introduced the concept of "intelligent" burn-in and developed the AMBYX® intelligent burn-in and test system. Today, we use AMBYX to test every component product we make.

With AMBYX, we can determine if the failure rate curves of individual product lots reach the random failure region of the bathtub curve by the end of the burn-in cycle. We subject product lots that do not exhibit a stable failure rate to additional burn-in. This burn-in flow also brings to our attention the slightest variation in a product's failure rate.

Since AMBYX allows us to test devices for functionality without removing them from the burn-in oven, we effectively eliminate failures resulting from handling, thereby minimizing "noise" from the test results. During the test phase, output produced by the devices under test is compared to the pattern expected. If a discrepancy occurs, AMBYX records the failure and provides the bit address, device address, board address, temperature, Vcc voltage, test pattern and time set.

During the burn-in cycle itself, devices are functionally tested in four intervals. The first test begins at room temperature. Then we ramp up the oven to 85°C for more functional testing. This enables us to detect thermal intermittent failures, another unique feature of intelligent burn-in. We conduct the next test at 125°C — any device that does not pass this sequence is eliminated. As the burn-in process continues, the devices are dynamically stressed at high temperature and voltage for a given number of hours. At the end of this period, we functionally test all devices again, followed by another burn-in cycle and further tests. This sequence is repeated four times on every device in every production lot.

These test results allow us to identify individual failures after each burn-in cycle. Figure 2 illustrates how the four burn-in and test cycles flow. The typical test results shown make up the first portion of the bathtub curve of component reliability.

There are two important reasons why Micron conducts the last two burn-in and test periods (or "quarters") at lower Vcc than the first two portions. First, we want the several million device hours that we accumulate weekly on production lots to be conducted at stress conditions identical to the conditions for the extended high-temperature-operating-life (HTOL) test used by IC manufacturers to compute random field failure rates. Second, we want to be sure we are not introducing new failure modes unrelated to normal wearout, such as VOS, by testing them at extremely elevated conditions.

Control charts, such as the one shown in Figure 3, alert us to trends in lot failure rates. When we detect an upward trend in a failure rate, we correlate the lots that need additional burn-in with all the variables that might be influencing the increased rate. Such variables could include fabrication and assembly equipment, manufacturing shifts and time frames when the lots were processed through specific steps.

The overall benefits of intelligent burn-in are wide ranging. Intelligent burn-in allows us to identify early-life failures and failure mechanisms as they would actually occur in customer applications. It also allows us to identify problem lots that, if undetected, could contribute substantially to infant mortalities.

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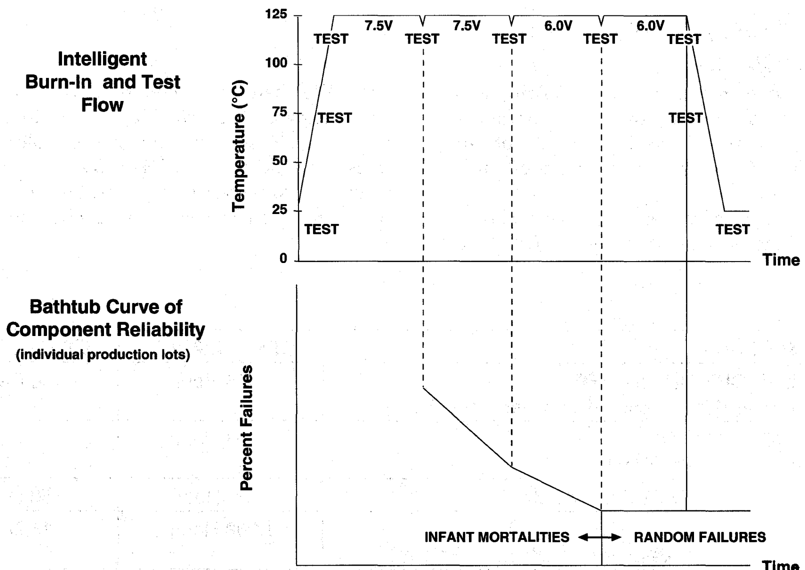

Figure 2
AMBYX BURN-IN/TEST FLOW AND TEST RESULTS

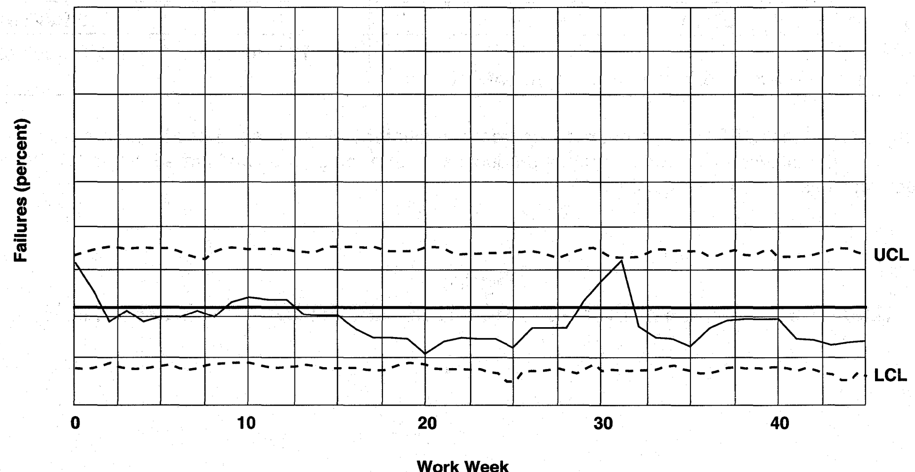

Figure 3
AMBYX FOURTH QUARTER FAILURES

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ENVIRONMENTAL PROCESS MONITOR PROGRAM

Micron's environmental process monitor (EPM) program is designed to ensure the reliability of our standard products. Under this program, we subject weekly samples of our various product and package types to a battery of stress tests.

During these tests, we stress the devices for many hours under conditions designed to simulate years of normal field use. We then apply equations derived from intricate engineering models to the data collected from the accelerated tests. From these calculations, we are able to predict failure rates under normal use. Figure 3 shows the conditions for these tests, known as environmental stress tests. The EPM program described in Figure 4 is for Micron's 4 Meg DRAM.

TEST NAME AND DESCRIPTION	TEST DURATION	BIWEEKLY SAMPLE SIZE
HIGH TEMPERATURE OPERATING LIFE (125°C, 6V, Checkerboard/Checkerboard Complement Pattern)	1,008 Hours	150 Devices
TEMPERATURE AND HUMIDITY (85°C, 85% RH, 5.5V, Alternating Bias)	1,008 Hours	150 Devices
AUTOCLAVE (121°C, 100% RH, 15 PSI, No Bias)	96 Hours	50 Devices
LOW TEMPERATURE LIFE (-25°C, 7V, Checkerboard/Checkerboard Complement Pattern)	1,008 Hours	15 Devices
TEMPERATURE CYCLE (0°C for 15 min., +125°C for 15 min, air to air)	1,000 Cycles	50 Devices
THERMAL SHOCK (-55°C for 5 min., +125°C for 5 min., liquid to liquid)	700 Cycles	50 Devices
HIGH TEMPERATURE STORAGE (150°C, No Bias)	1,008 Hours	50 Devices
ELECTROSTATIC DISCHARGE (+ and -)	MIL-STD-3015.7	40 Devices
Vcc LATCH-UP (MIN voltage, 25°C)	—	10 Devices
SYSTEM SOFT ERROR (4.5V, 0.3ms, Checkerboard/Checkerboard Complement Patterns)	168 Hours	2,010 Devices

NOTE: Samples used in the EPM program are taken from five different lots at finished goods. Before being subjected to environmental testing, all surface-mount products are run twice through an infrared (IR) reflow furnace, reaching a peak temperature of 240°C.

Figure 4
SAMPLE ENVIRONMENTAL PROCESS MONITOR – 4 MEG DRAM

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FAILURE RATE CALCULATION

The failure rate during the useful life of a device is expressed as percent failures per thousand device hours or as FITs (failures in time, per billion device hours). Using Micron's 4 Meg DRAM as an example, the failure rate is calculated as follows:

$$\text{Failure Rate} = \frac{Pn}{\text{Device hours} \times AF}$$

where: Pn = Poisson Statistic (at a given confidence level). In our example given seven device failure, Pn = 8.390 at 60 percent confidence level.

Device hours = sample size multiplied by test time (in hours) In our example, device hours equal 7.803×10^6 in an accelerated environment.

AF = acceleration factor between the stress environment and typical use conditions. For the 4 Meg DRAM, the acceleration factor between 125°C, 6V (HTOL stress conditions) and 50°C, 5V (typical operating conditions) equals 56. (Calculation of this acceleration factor is described in the following section.)

Thus, the failure rate of the Micron 4 Meg DRAM family is computed as follows:

$$\text{Failure Rate} = \frac{8.390}{(7.803 \text{ X } 10^6)(56)} = 19.200 \text{ X } 10^{-9}$$

where: total device hours at test conditions = 7.803×10^6. Equivalent device hours at typical use conditions (50°C, 5V Vcc) using an acceleration factor of 56 equals 56 $(7.803 \times 10^6) = 437 \times 10^6$.

To translate this failure rate into percent failures per thousand device hours, we multiply the failure rate obtained from the equation above by 10^5:

Failure Rate = $(19.200 \times 10^{-9}) \times 10^5$ = 0.0019202% or 0.0019% per 1K device hours

To state the failure rate in FITs, we multiply the failure rate obtained from the equation above by 10^9:

Failure Rate = $19.202 \times 10^{-9}) \times 10^9$ = 19.202 or 19 FITs.

RELIABILITY

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ACCELERATION FACTOR CALCULATION

Again, using the 4 Meg DRAM as our example, the acceleration factor between high temperature operating life stress conditions (125°C, 6V) and typical operating conditions (50°C, 5V) is computed using the following models:

ACCELERATION FACTOR DUE TO TEMPERATURE STRESS

The acceleration factor due to temperature stress is computed using the Arrhenius equation, which is stated as follows:

$$AF_T = e^{\frac{E_a}{k}\left[\frac{1}{T_O} - \frac{1}{T_S}\right]}$$

where: k = Boltzmann's constant , which is equal to 8.617×10^{-5} eV/K.

T_O and T_S = typical operating and stress temperatures, respectively, in kelvins.

E = activation energy in eV. (For oxide defects, which is the most common failure mechanism for the 4 Meg DRAM used in our example. The activation energy is determined to be 0.3eV.)

Using these values, the temperature acceleration factor between 125°C and 50°C is computed to be 7.62.

ACCELERATION FACTOR DUE TO VOLTAGE STRESS

The acceleration factor due to voltage stress is computed using the following model:

$$AF_V = e^{\beta (V_S - V_O)}$$

where:

v_S and v_O = stress voltage and typical operating voltage, respectively, in volts

β = constant, the value of which was derived experimentally by running several sessions of Micron's intelligent burn-in test sequence at different voltages on large numbers of the device. (For the 4 Meg DRAM used in our example, ß equals 2).

Thus, the voltage acceleration factor for the 4 Meg DRAM between 6V (stress condition) and 5V (typical operating condition) is computed to be 7.39.

Finally, the overall acceleration factor due to temperature and voltage stress is calculated as the product of the two respective acceleration factors or:

$$AF_{overall} = AF_{temperature} \times AF_{voltage}$$
$$= 7.62 \times 7.39$$
$$= 56$$

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OUTGOING PRODUCT QUALITY

Before being sent to our finished goods area, where products are prepared for shipping, a special unit within the quality assurance department takes a sample from each production lot. These samples are subjected to visual and electrical testing to measure the acceptable quality level (AQL) of all outgoing product. Test flows for new products that have not met required production volume and ppm levels are more comprehensive than for mature products. Over a period of time, as a product matures, the objective is to eliminate those tests which devices never fail. AQL testing, although it is performed on only a small percentage of each product, is much more exhaustive. Conducted at spec conditions without guardband for every known timing, pattern and background, it is a sanity check on the production test flow. Its purpose is to detect subtle shifts in defect mechanisms which the production test flow may not catch.

Visual testing for mechanical defects consists of visual inspection of the sample devices for any physical irregularities that could negatively affect device performance. If a sample device is found to have, for example, a bent lead, a package irregularity or excess solder, the entire lot is returned to our test area for a 100 percent visual inspection.

Electrical testing of the sample devices is performed using automatic test equipment (ATE) systems. Testing is conducted at 0°C, or room temperature (~25°C) and at 70°C. Should an electrical failure occur, a quality assurance engineer further evaluates the failing device. After completing this analysis, the quality assurance engineer determines which production monitor/test should have caught the failure, and the devices are retested beginning at that point in the test flow. These are important steps to preserve the integrity of our test process.

AUTOMATED DATA CAPTURE AND ANALYSIS

Micron has developed a sophisticated data capture and analysis system with a computer network tailored to the needs of quality IC manufacturing. Figure 5 shows the various functional areas that provide the input to our VAX data bases.

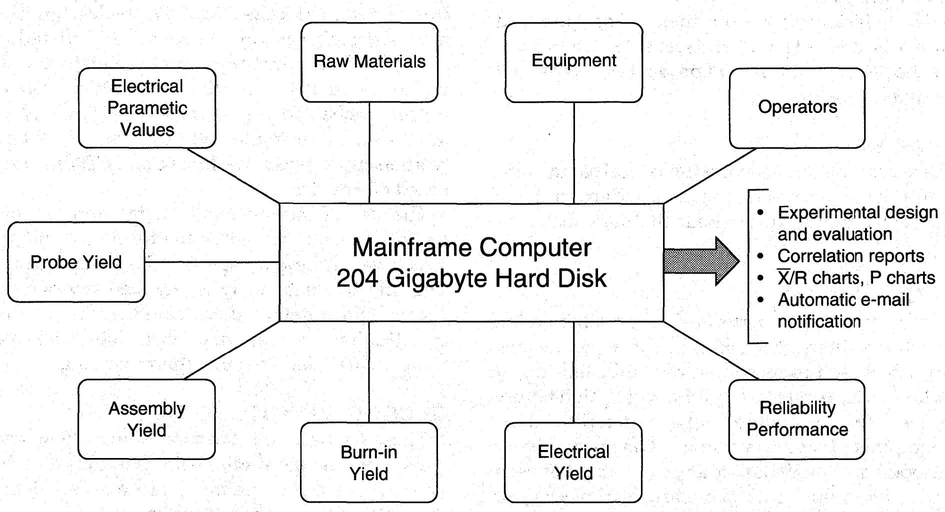

Figure 7
STATISTICAL CORRELATION

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DATA CAPTURE

Automated, real-time data capture makes real-time charting ($\overline{X}$ and R charts, etc.) of all critical operations and processes possible and ensures that appropriate personnel know of any unexpected variation on a timely basis. As production lots move through each manufacturing step, detailed information (including step number, lot number, machine number, date/time, and operator number) is entered into the production data base. Automated, highly-programmable measurement systems capture a host of parameters associated with equipment, on-line process material and environmental variables.

STATISTICAL TECHNIQUES AND TOOLS

By using highly flexible, on-line data extraction programs, system users can tap this vast data base and design their own correlation and trend analyses. Because we can correlate process variables to product performance, we can make on-line projections of the quality of our finished product for a given lot or process run. In addition, we can estimate the impact of process improvements on quality well in advance and can make the impact of process deviations more visible to our engineers. This approach allows us to model yield and quality parameters based on on-line parameters. We then use this model to predict the final product results through the following means:

GROUP SUMMARIES

Summaries, which provide the means and standard deviations of user-defined parametrics, enable system users to compare the parametric values of production lots as well as special engineering lots.

TREND ANALYSIS

Trend charts are routinely generated for critical parameters. System users can plot the means and ranges of any probe or parametric data captured throughout the manufacturing process.

CORRELATION ANALYSIS

Correlation analysis can be performed on any combination of factors, such as equipment, masks or electrical parameters. One report, regularly produced and disseminated to key personnel, takes two groups of lots (one with a high failure rate, the other with a low failure rate) and identifies all the pieces of equipment that are common to one or the other group. The report quickly alerts us to any correlation between a lot with a high failure rate and particular piece(s) of equipment in the wafer fabrication or assembly areas.

Another regularly produced report analyzes a user-selected set of database parametrics against an index, such as manufacturing yield. Lots are divided into three subgroups (upper yielding, middle yielding and lower yielding). The report then correlates the yields with all electrical parametric values taken on individual lots at wafer sort. It helps us determine which processing step may have caused the yields to vary among the three subgroups.

STATISTICAL PROCESS CONTROL (SPC) CHARTS

Micron employs SPC control charts throughout the company to monitor and evaluate critical process parameters, such as critical dimensions (CDs), oxide thickness, chemical vapor depositions (CVDs), particle counts, temperature and humidity, and many other critical process and product quality parameters.

OVERLAYS OR WAFER MAPS

Maps, which are produced for all wafers during probe, show various parameters as a function of position on the wafer and are very useful for problem isolation. Maps may be analyzed individually or in groups. For example, wafers from an entire lot may be analyzed in relation to one particular parameter.

RS/1 DISCOVER/EXPLORE/MULREG

This analysis software is used for experimental design and evaluation of results. The statistical approach supported by this software (*t* tests, ANOVA tables, multiregression analysis, etc.) has proven invaluable in reducing time expended for product development and trouble-shooting. It is also used to determine the relationships between process output, probe and parametric data. Using multiregression analysis, for example, we are able to determine the relationship between L effective and CD dimensions to the speed of a device.

The use of automation in data capture, analysis and feedback greatly enhances the flexibility and speed with which we can view all aspects of the manufacturing process. This effective data analysis and feedback system helps to reduce parametric deviations, improve margin to specifications, increase manufacturing yields and provide more accurate fabrication output planning.

GAUGE CAPABILITY STUDIES

These studies are performed on both new and existing equipment. Gauge studies help us understand the cause of variation in a measurement process and determine the amount of variation in the system.

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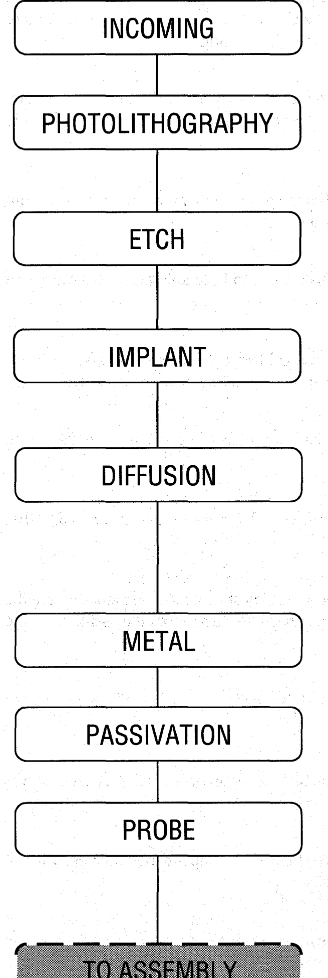
FABRICATION*



Incoming
Verification that the starting material is clean, uniform and compliant with all requirements. Each wafer receives an individual laser scribe for total product traceability.

Photolithography
Wafers are coated with a layer of light-sensitive photoresist. Specified sections of the wafer are exposed by projecting ultraviolet light onto the wafer through a mask. The exposed photoresist hardens and becomes impervious to etchants.

Etch
The areas of the wafer not protected by the exposed photoresist are removed by either plasma (dry etch) or acid (wet etch). The photoresist is then cleaned ("stripped") off of the wafer, leaving a pattern in the exact design of the mask.

Implant
Wafers are bombarded with positively or negatively charged dopant ions, which are implanted into the silicon. This process changes electrical characteristics in selective areas of the silicon. This is called "doping" and forms conductive regions on the wafer.

Diffusion
Silicon dioxide, nitrite and polysilicon layers are formed on the wafer during a number of high-temperature furnace processes. The wafers are exposed to various gases which either react with the silicon, causing it to oxidize and form an SiO_2 layer or react with each other, forming poly and nitrite deposits. These layers are patterned using photolithography and form the layers of the diodes, transistors and capacitors of the circuit. High temperature furnaces are also used to introduce and diffuse dopants into the wafers.

Metal
A thin layer of aluminum or other metal is deposited and patterned, forming interconnections between various regions of the die.

Passivation
The fabrication process is completed by forming a final glass layer on the wafer. This layer protects the circuits from contamination or damage through the testing and packaging process flows.

Probe
When the fabrication process is complete, each wafer consists of many die. Each individual die on the wafer is taken through a series of tests. A computer attached to a probe card tests the die and produces a "wafer map," storing data on each functioning (good) die. All data is collected and stored for each die. Wafermaps are used in assembly to ensure that only good die are packaged.

Assembly (see next page)

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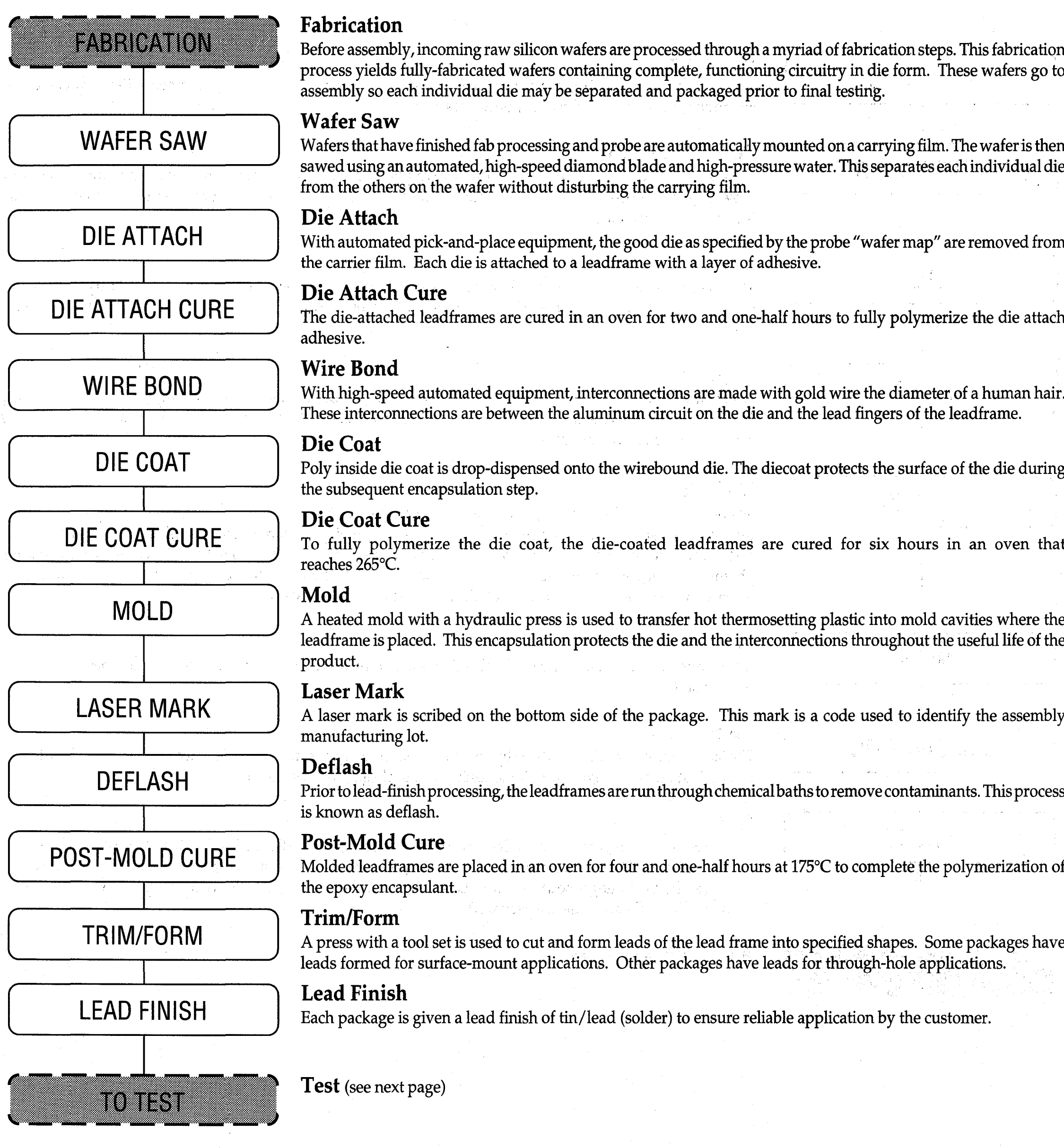
ASSEMBLY*



Fabrication
Before assembly, incoming raw silicon wafers are processed through a myriad of fabrication steps. This fabrication process yields fully-fabricated wafers containing complete, functioning circuitry in die form. These wafers go to assembly so each individual die may be separated and packaged prior to final testing.

Wafer Saw
Wafers that have finished fab processing and probe are automatically mounted on a carrying film. The wafer is then sawed using an automated, high-speed diamond blade and high-pressure water. This separates each individual die from the others on the wafer without disturbing the carrying film.

Die Attach
With automated pick-and-place equipment, the good die as specified by the probe "wafer map" are removed from the carrier film. Each die is attached to a leadframe with a layer of adhesive.

Die Attach Cure
The die-attached leadframes are cured in an oven for two and one-half hours to fully polymerize the die attach adhesive.

Wire Bond
With high-speed automated equipment, interconnections are made with gold wire the diameter of a human hair. These interconnections are between the aluminum circuit on the die and the lead fingers of the leadframe.

Die Coat
Poly inside die coat is drop-dispensed onto the wirebound die. The diecoat protects the surface of the die during the subsequent encapsulation step.

Die Coat Cure
To fully polymerize the die coat, the die-coated leadframes are cured for six hours in an oven that reaches 265°C.

Mold
A heated mold with a hydraulic press is used to transfer hot thermosetting plastic into mold cavities where the leadframe is placed. This encapsulation protects the die and the interconnections throughout the useful life of the product.

Laser Mark
A laser mark is scribed on the bottom side of the package. This mark is a code used to identify the assembly manufacturing lot.

Deflash
Prior to lead-finish processing, the leadframes are run through chemical baths to remove contaminants. This process is known as deflash.

Post-Mold Cure
Molded leadframes are placed in an oven for four and one-half hours at 175°C to complete the polymerization of the epoxy encapsulant.

Trim/Form
A press with a tool set is used to cut and form leads of the lead frame into specified shapes. Some packages have leads formed for surface-mount applications. Other packages have leads for through-hole applications.

Lead Finish
Each package is given a lead finish of tin/lead (solder) to ensure reliable application by the customer.

Test (see next page)

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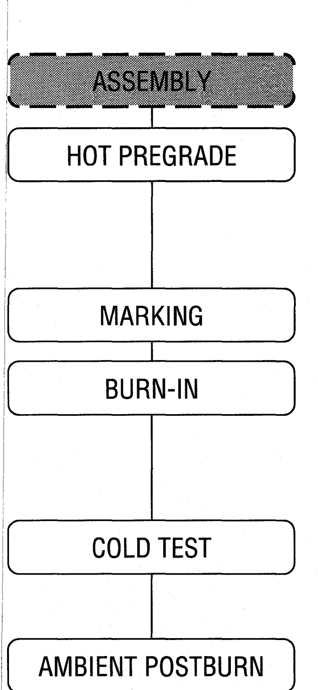
TEST*



Assembly
Fully fabricated silicon wafers reach assembly after each die has been probed to screen out failures. Passing chips are then carried through a number of steps to become individual units in leaded packages.

Hot Pregrade
All testing (including speed sorting, parametric and functional testing) is conducted at 85°C; parts are tested for speed grade and functionality. Parametric tests are performed to detect opens, shorts, input/output leakage, input/output high and low levels and standby current. Functional tests include low and high Vcc margin, Vcc bump, speed sorting, dynamic and static refresh, long tRAS and tCAS lows, and a full range of algorithms and data backgrounds to verify AC parameters. Specific tests and temperatures are incorporated as applicable for specific products.

Marking
Devices are marked with ink with the following information: year, special process designator, part type, package type and speed grade.

Burn-in
Micron uses its exclusive AMBYX® intelligent burn-in and test system to screen out infant mortalities. Devices are dynamically burned-in, using checkerboard/checkerboard complement patterns in four intervals under the following conditions: 125°C, 7V Vcc for the first three intervals and 125°C, 6V Vcc for the final interval. Functional testing is performed at 85°C and back to 25°C AMBYX tests for thermal intermittent opens. Devices are also functionally tested at burn-in conditions (125°C, 7V) at the beginning of the burn-in cycle to verify that the devices under test are being properly exercised.

Cold Test
Micron also uses its AMBYX test system to perform functional pattern tests at ambient, cold and hot temperatures. Low and high Vcc margin, dynamic (distibuted only) and static refresh, long ^{t}RAS and a full range of algorithms and data backgrounds are performed at temperatures ranging from -10°C to 90°C. To insure wire-bond integrity, testing is performed while temperature are ramped from 25°C to -10°C and back to 25°C.

Ambient Postburn
Parametric and functional tests are conducted at 25°C. Parametric tests are performed to detect opens, shorts, and input/output leakage, and to determine whether input/output high and low levels and standby and operating currents are within specified limits. Functional tests include low and high Vcc margin, Vcc bump, speed verification, dynamic (distributed and disturbed) and static refresh, long ^{t}RAS and ^{t}CASlows, and a full range of algorithms and data backgrounds to verify AC parameters.

Hot Final
All testing (including speed grade verification and parametric and functional testing) is conducted at 78°C. Parametric tests are performed to detect opens, shorts, and input/output leakage and to determine whether input/output high and low levels, and standby and operating currents are within specified limits. Functional tests include low and high Vcc margin, Vcc bump, speed verification, dynamic (distributed and disturbed) and static refresh, long ^{t}RAS and ^{t}CAS lows, and a full range of algorithms and data backgrounds to verify AC parameters.

Scanner
Devices are optically scanned by an automated scanning machine for bent leads, incorrect splay, coplanarity failures and tweeze failures. Passing and failing parts are then sorted into appropriate bins.

Visual Inspection
All devices determined functional are visually inspected for cosmetic defects such as bent leads, poor marks, broken packages and poor solder. Defective products are removed and repaired, if possible. Data on the type of defects found is carefully recorded and used for improving the manufacturing processes in both assembly and test.

AQL
A quality assurance monitoring program overseas the electrical and environmental performance of all production lots. New products which have not met required production volume and ppm levels are held at this stage until it is confirmed that electrical and environmental test results meet Micron's requirements.

Packaging
Devices are prepared for shipping. They may remain in tubes or they may be mechanically placed in tape-and-reel packages, ready for application in automatic pick-and-place machines. Products will be either dry-packed in vacuum sealed bags, or placed in black antistatic bags.

Finished Goods
Devices are shipped through a system that maintains lot identity.

*This flow is general and is based on DRAM and VRAM products.

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SYNCHRONOUS DRAMs 2

DRAM MODULES 3

DRAM CARDS 4

TECHNICAL NOTES 5

PRODUCT RELIABILITY 6

PACKAGE INFORMATION 7

SALES INFORMATION 8

PACKAGE TYPE	PIN COUNT	PAGE
PLASTIC DIP	18	7-2
	20	7-3
PLASTIC ZIP	20	7-4
PLASTIC SOJ	20/26	7-6
	24/26	7-7
	24/28	7-8
	28	7-9
	32	7-11
	40	7-12
	42	7-13
TSOP	20/26	7-14
	24/26	7-15
	28	7-16
	40/44	7-17
	44/50	7-18
	44	7-19
MODULE SIMM	30	7-20
	72	7-23
MODULE DIMM	168	7-32
DRAM CARD	88	7-40

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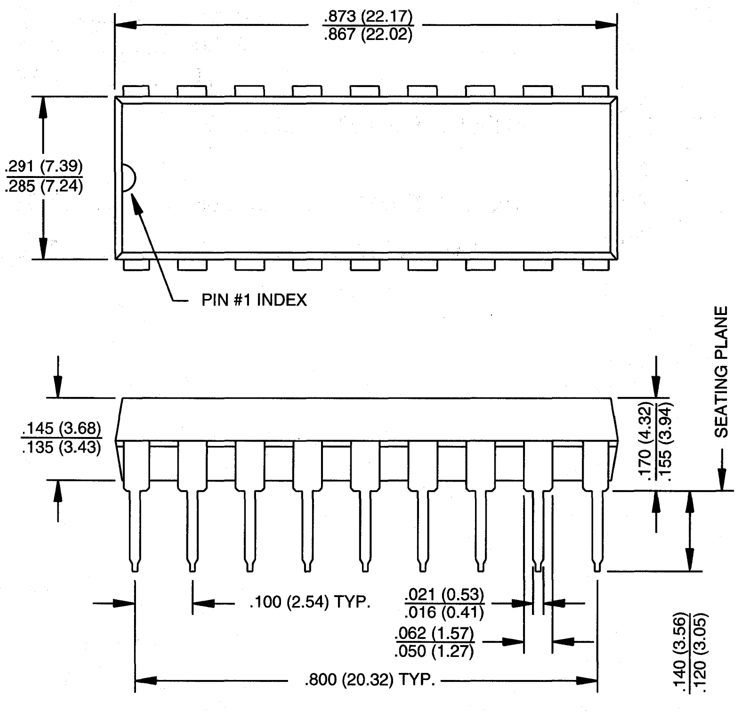
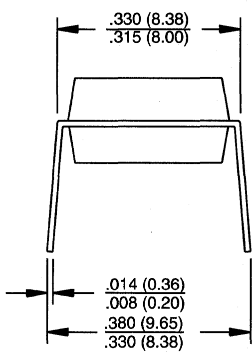
18-PIN PLASTIC DIP (300 mil)

DA-1





NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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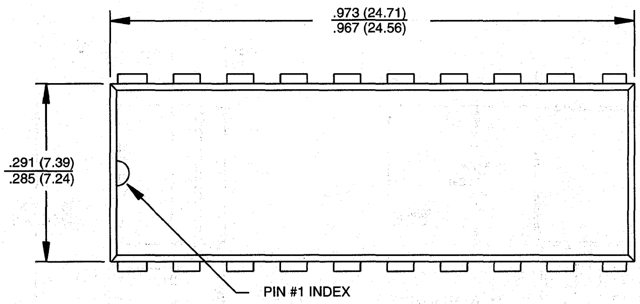
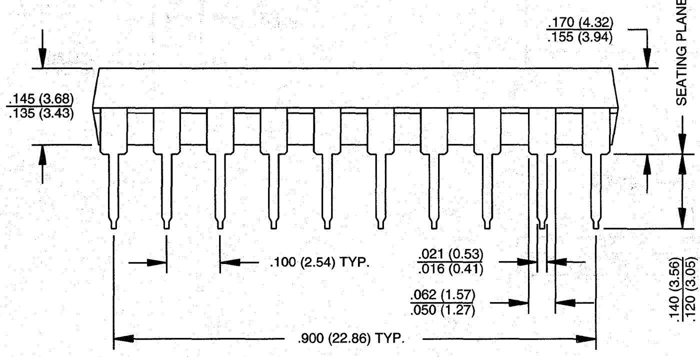
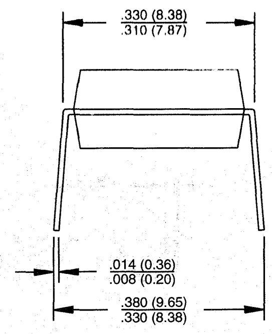
20-PIN PLASTIC DIP (300 mil)

DA-2







NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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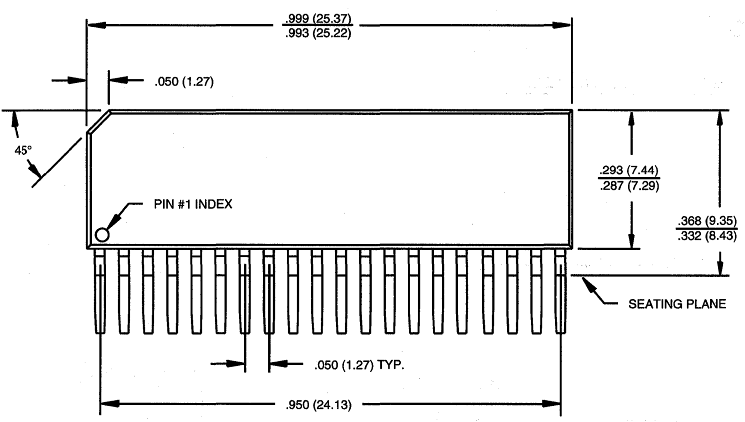
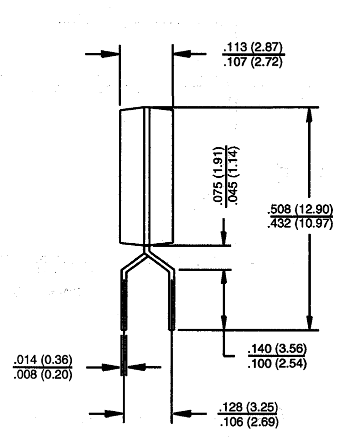
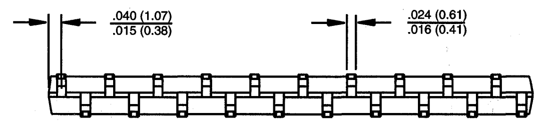
20-PIN PLASTIC ZIP (350 mil)

DB-1







NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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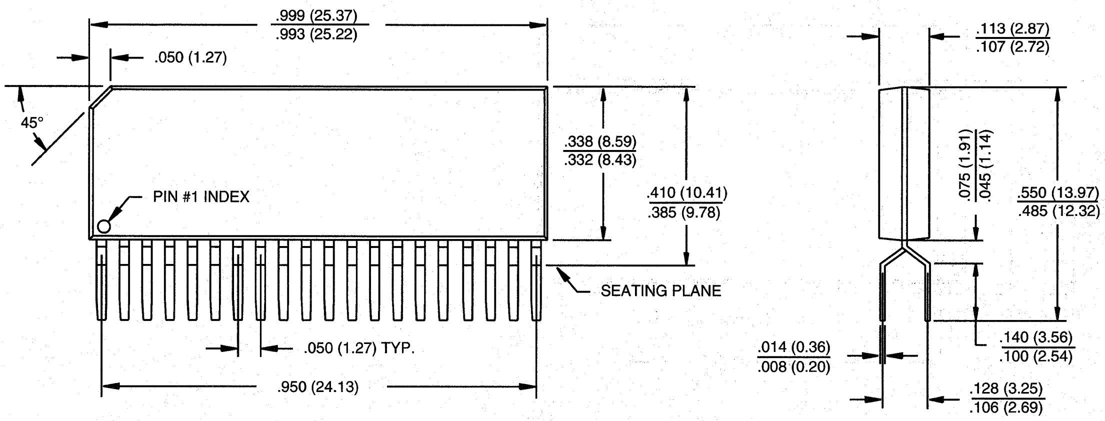
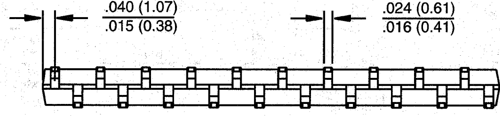
20-PIN PLASTIC ZIP (400 mil)

DB-2





PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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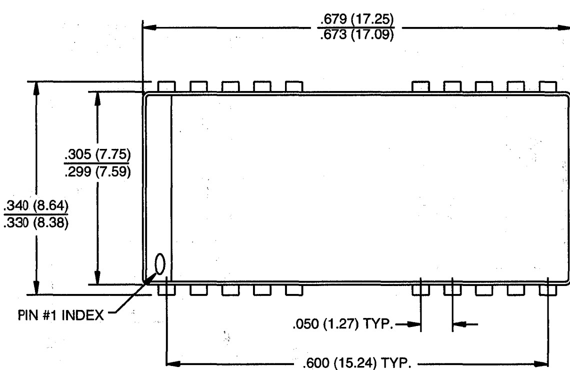
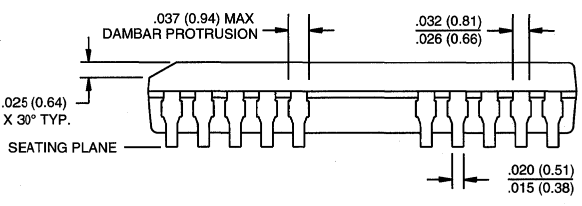
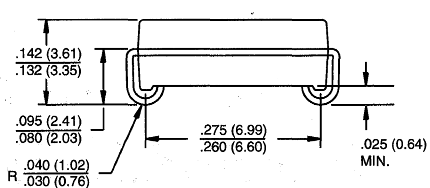
20/26-PIN PLASTIC SOJ (300 mil)

DC-1







PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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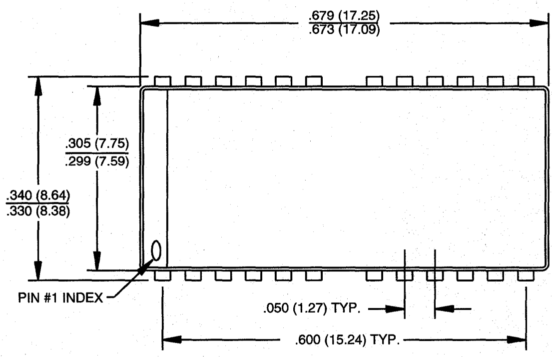
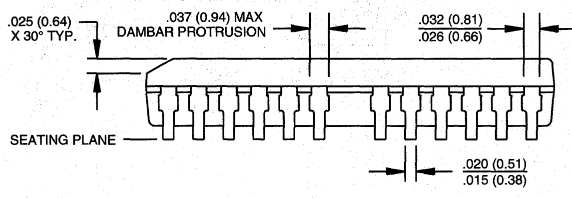
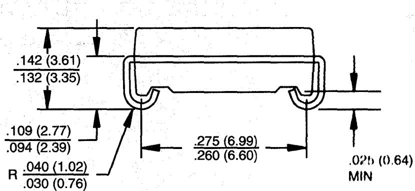
24/26-PIN PLASTIC SOJ (300 mil)

DC-2







PACKAGE INFORMATION

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2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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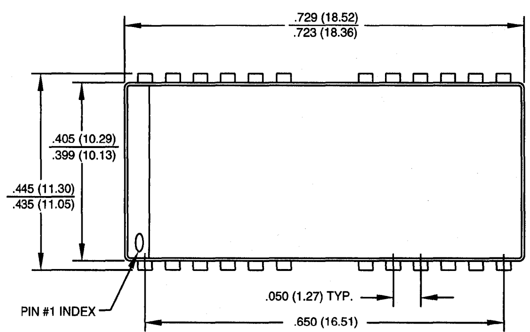
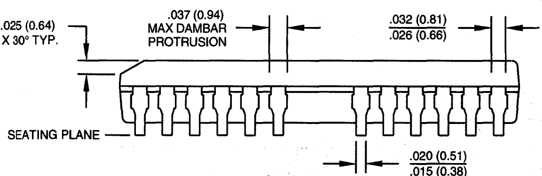
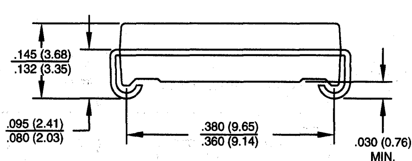
24/28-PIN PLASTIC SOJ (400 mil)

DC-3







PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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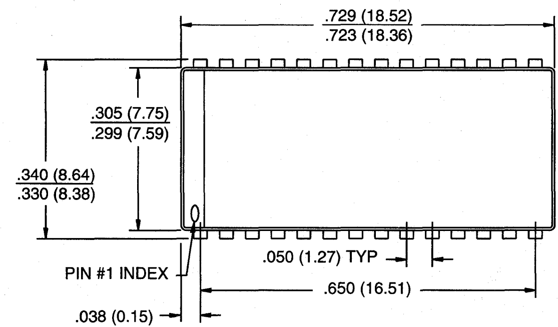
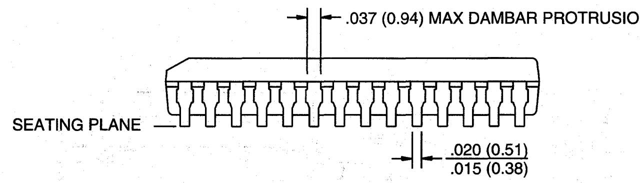
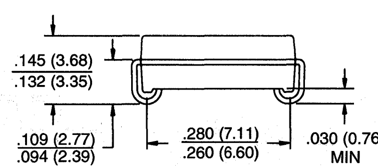
28-PIN PLASTIC SOJ (300 mil)

DC-8







PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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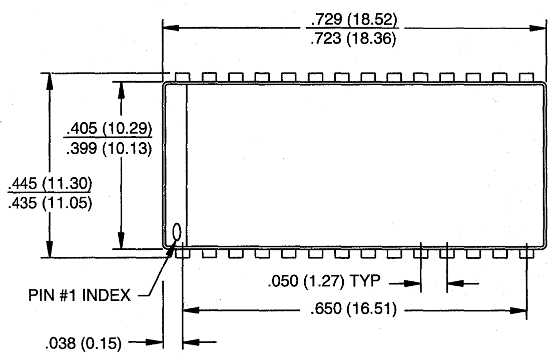
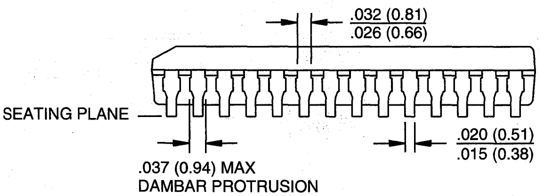
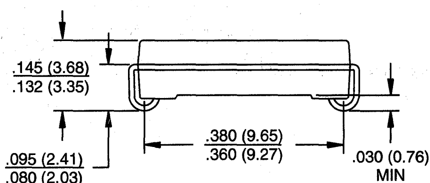
28-PIN PLASTIC SOJ (400 mil)

DC-4







PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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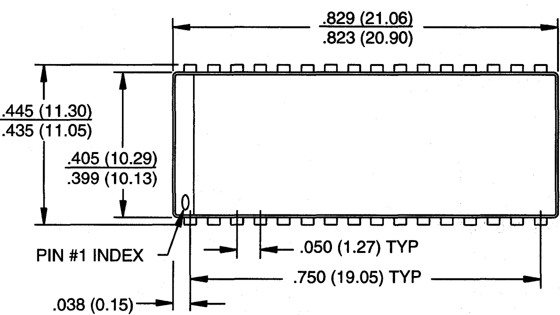
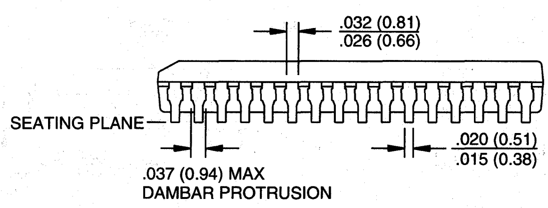
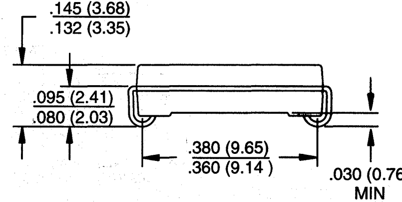
32-PIN PLASTIC SOJ (400 mil)

DC-5







PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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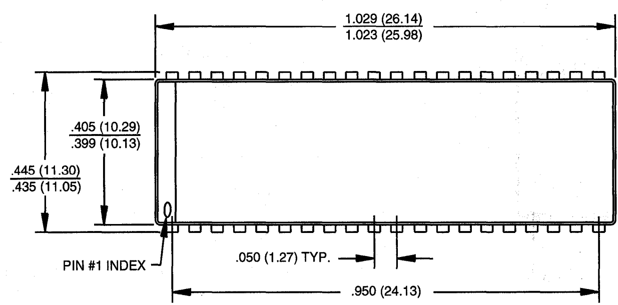
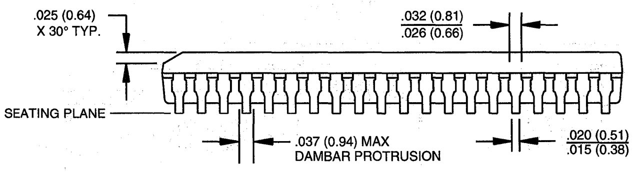
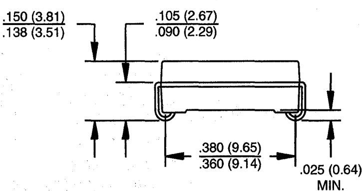
40-PIN PLASTIC SOJ (400 mil)

DC-6







PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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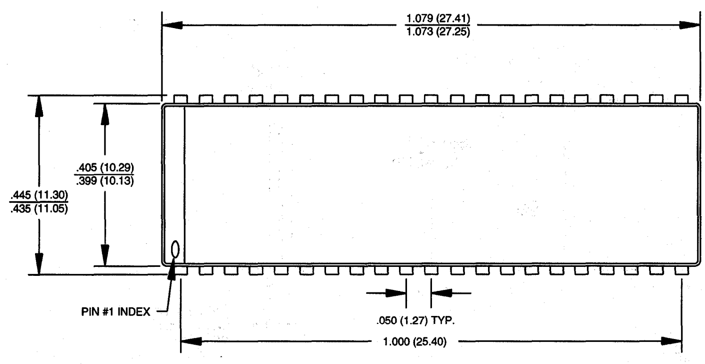
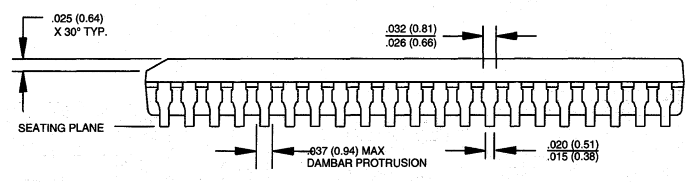
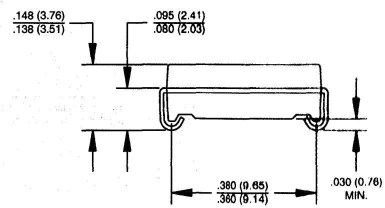
42-PIN PLASTIC SOJ (400 mil)

DC-7







NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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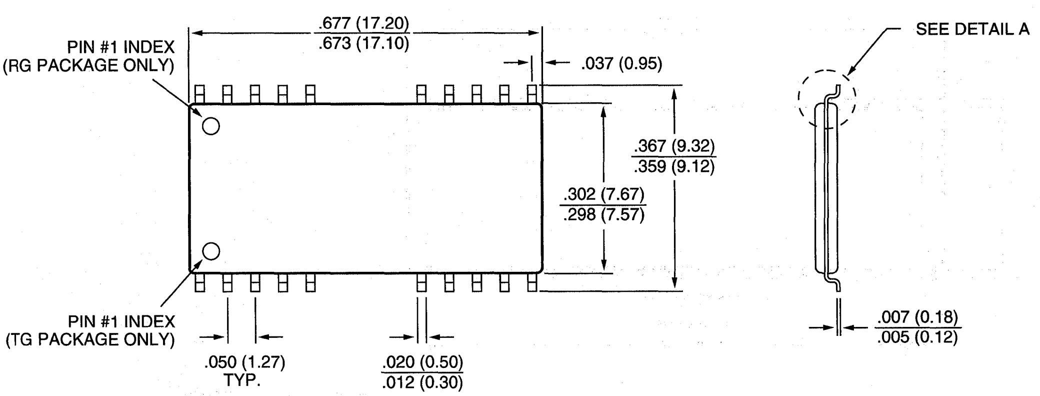
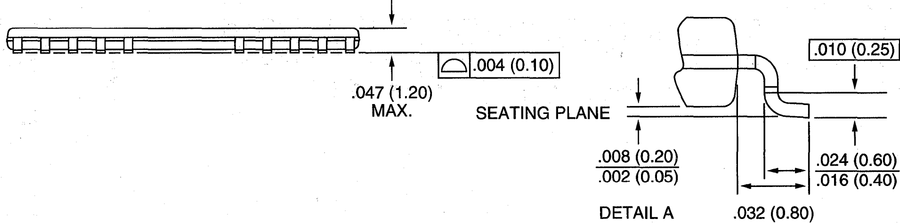
20/26-PIN PLASTIC TSOP (300 mil)

DD-1





PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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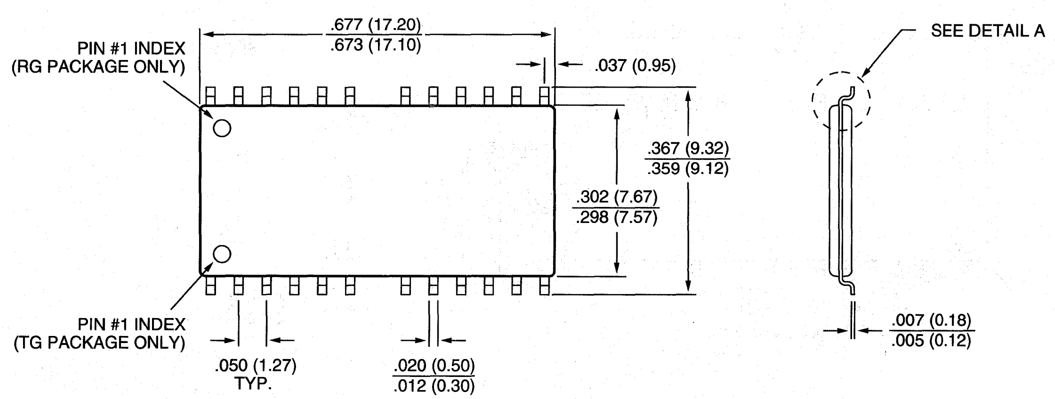
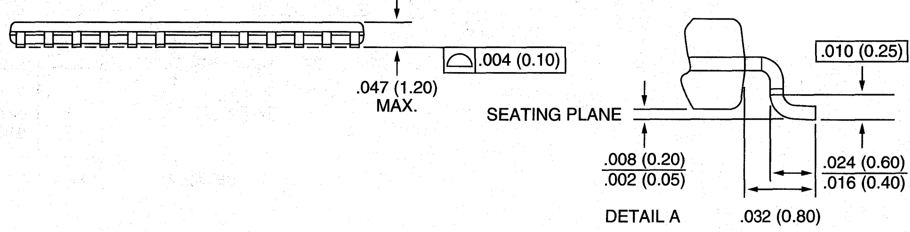
24/26-PIN PLASTIC TSOP (300 mil)

DD-2





PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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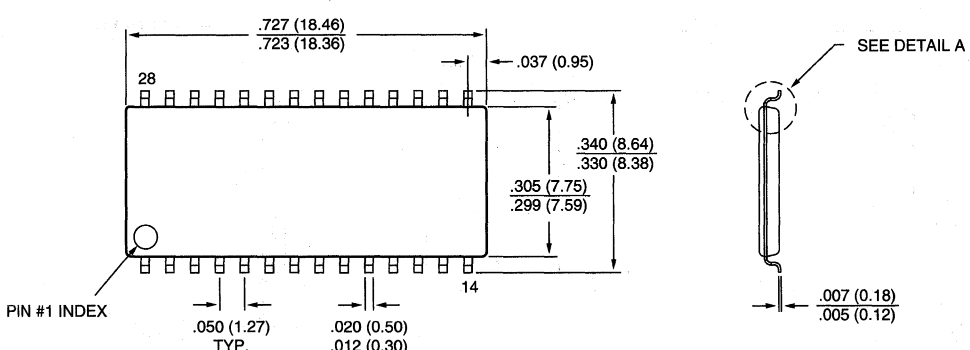
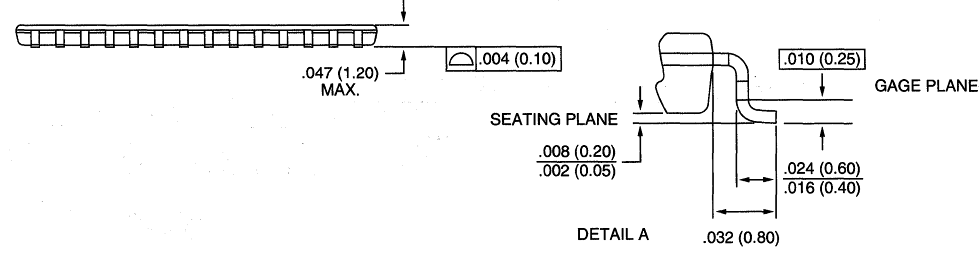
28-PIN PLASTIC TSOP (300 mil)

DD-3





PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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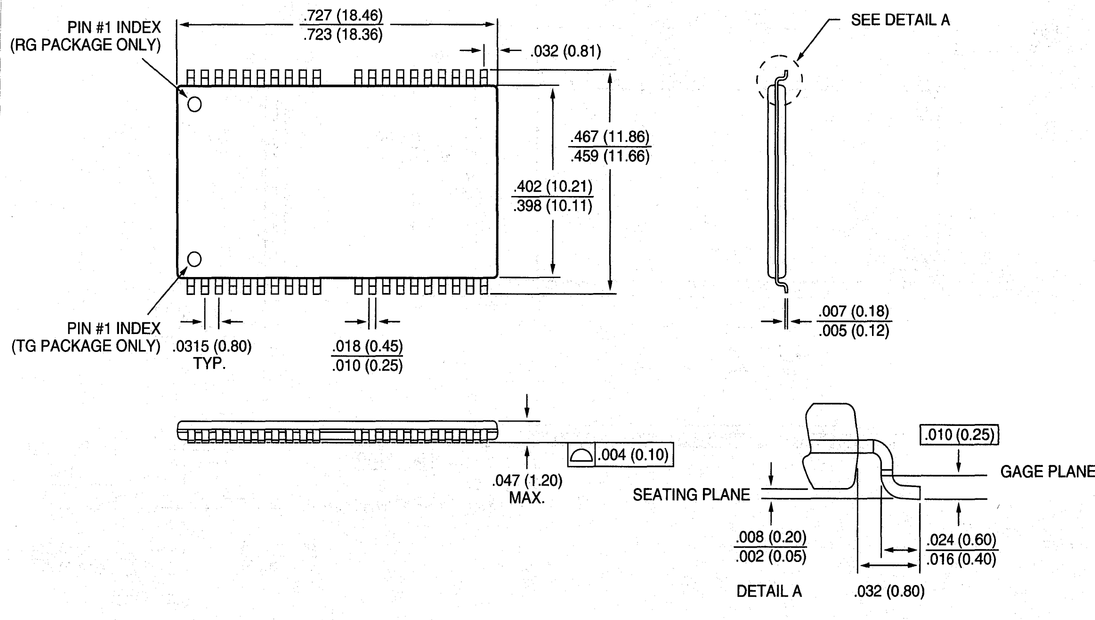
40/44-PIN PLASTIC TSOP (400 mil)

DD-5



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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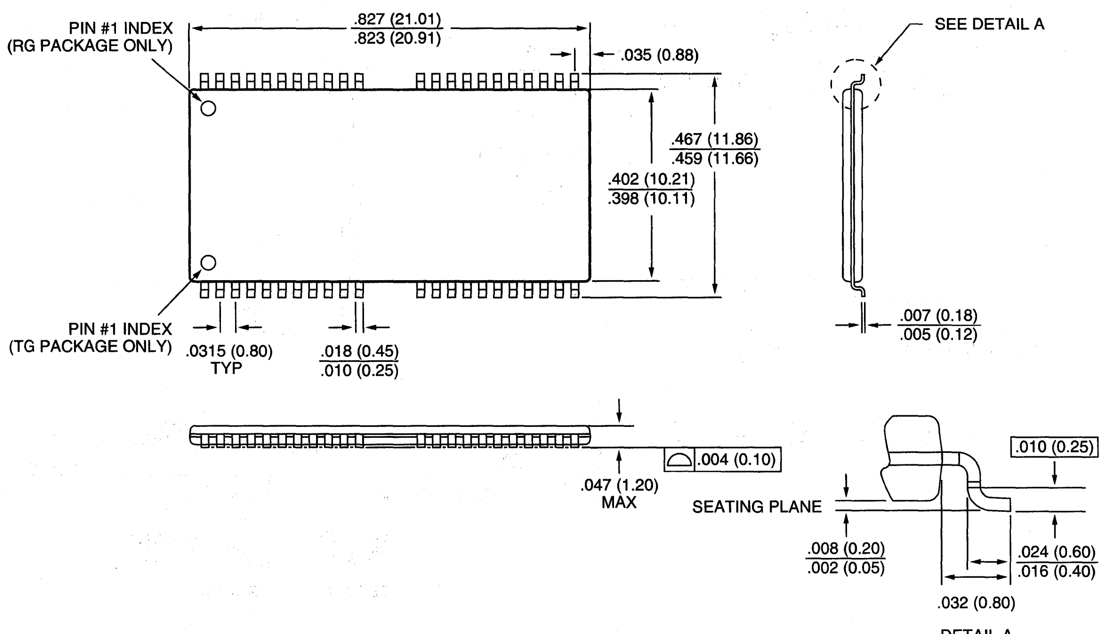
44/50-PIN PLASTIC TSOP (400 mil)

DD-6



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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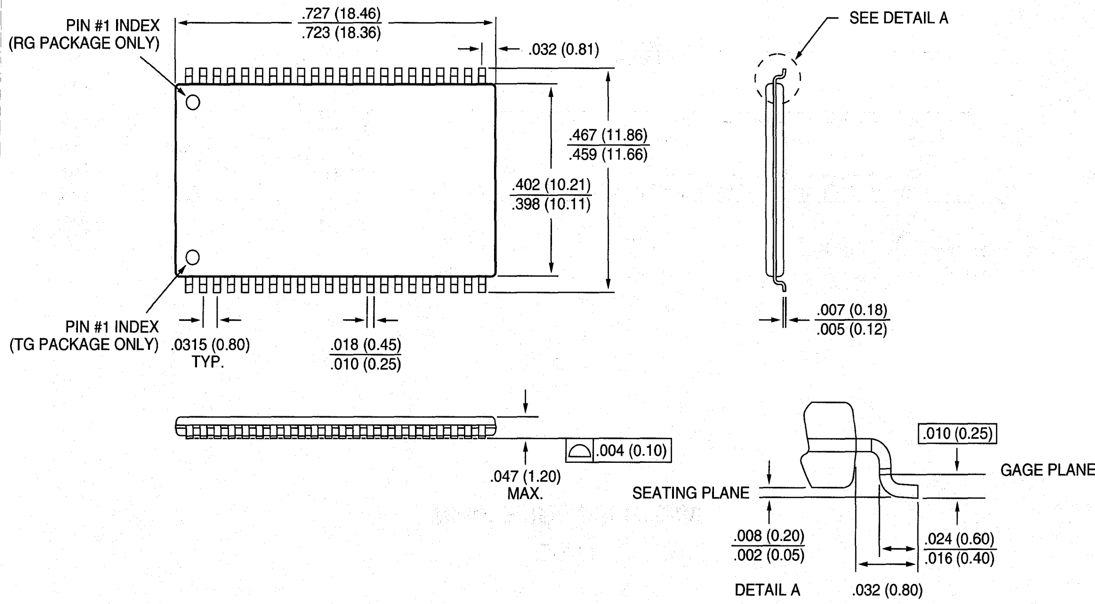
44-PIN PLASTIC TSOP (400 mil)

DD-7



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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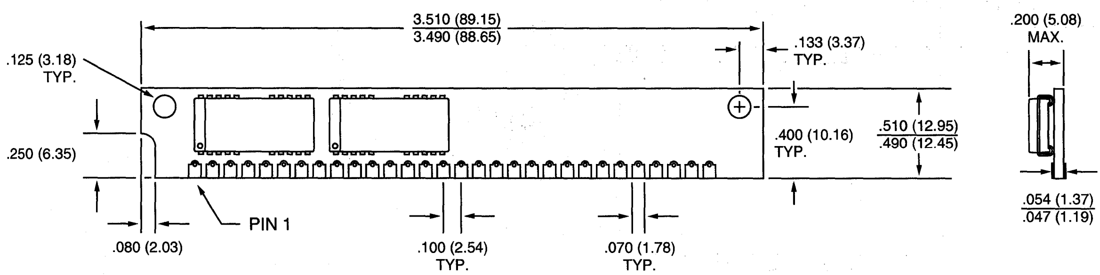
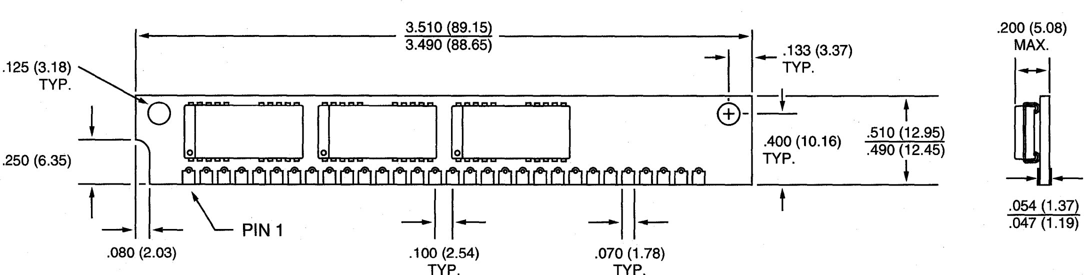
30-PIN MODULE SIMM

DE-1



30-PIN MODULE SIMM

DE-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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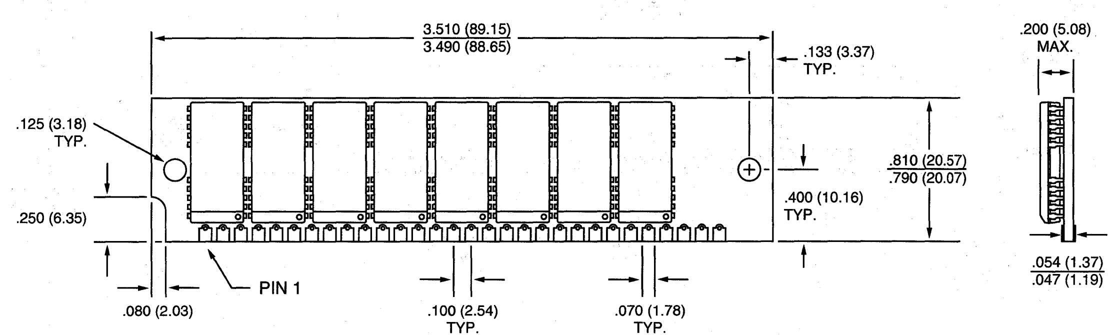
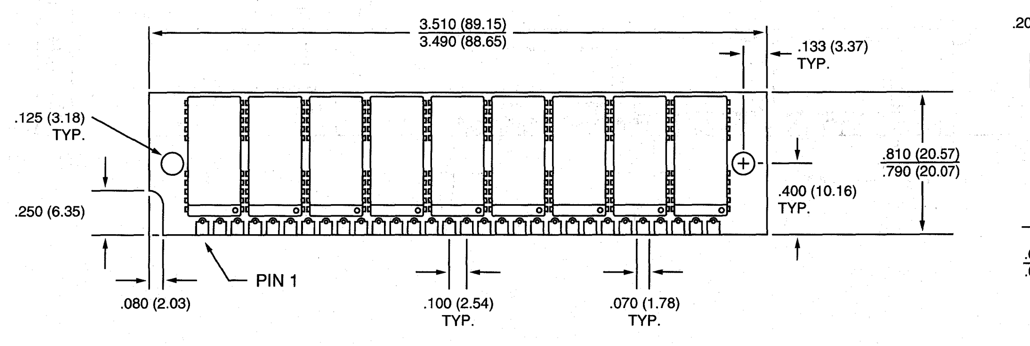
30-PIN MODULE SIMM

DE-3



30-PIN MODULE SIMM

DE-4



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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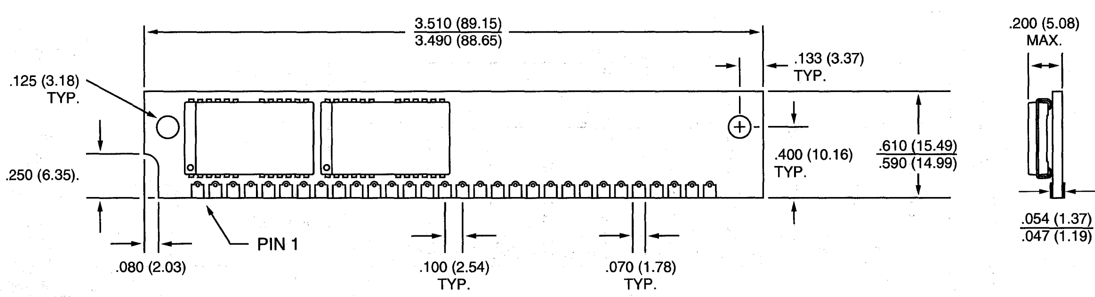
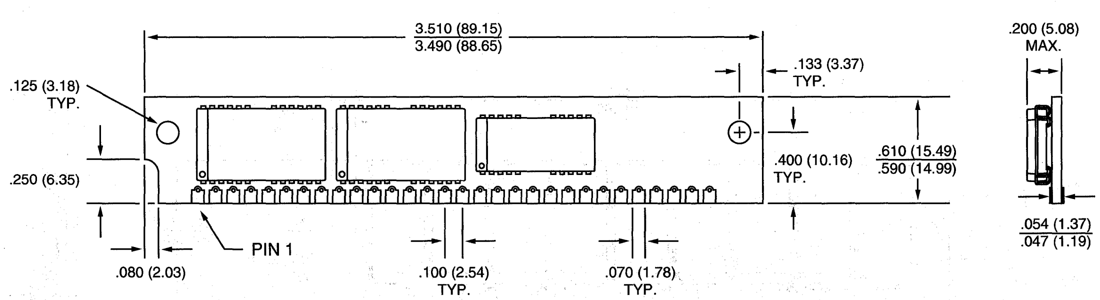
30-PIN MODULE SIMM

DE-5



30-PIN MODULE SIMM

DE-6



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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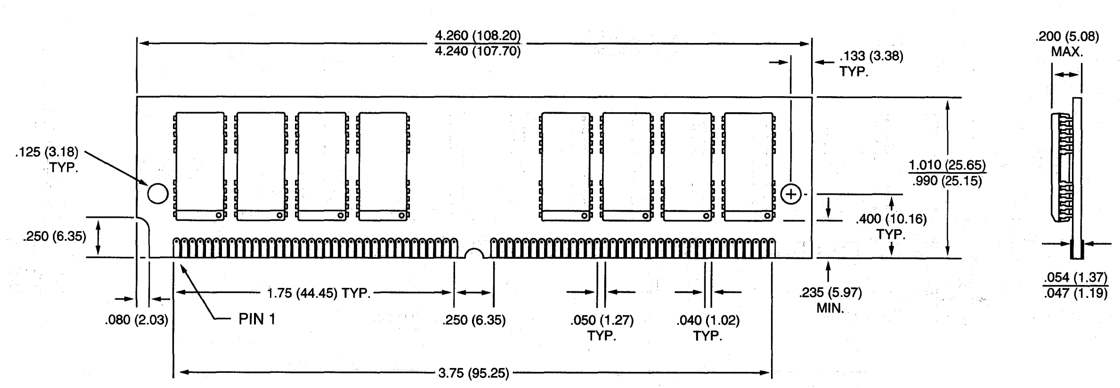
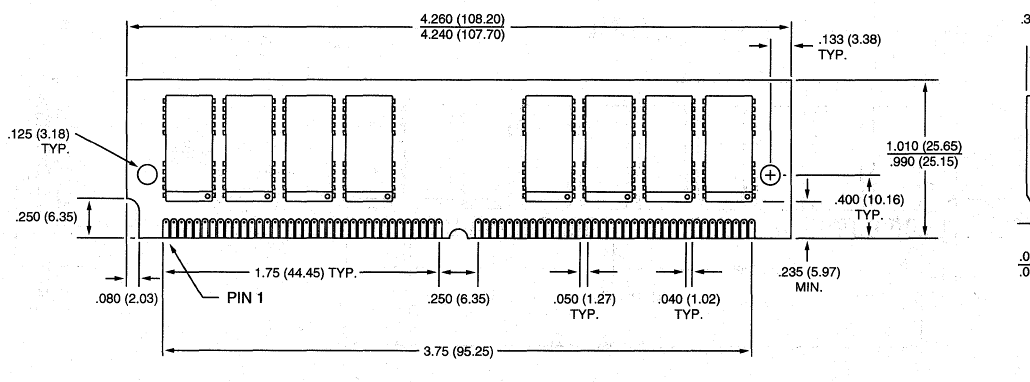
72-PIN MODULE SIMM
DE-7



72-PIN MODULE SIMM
DE-8



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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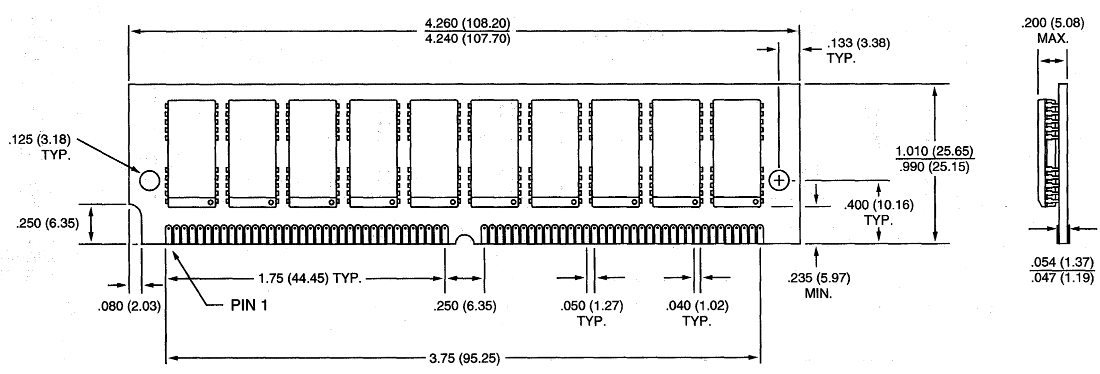
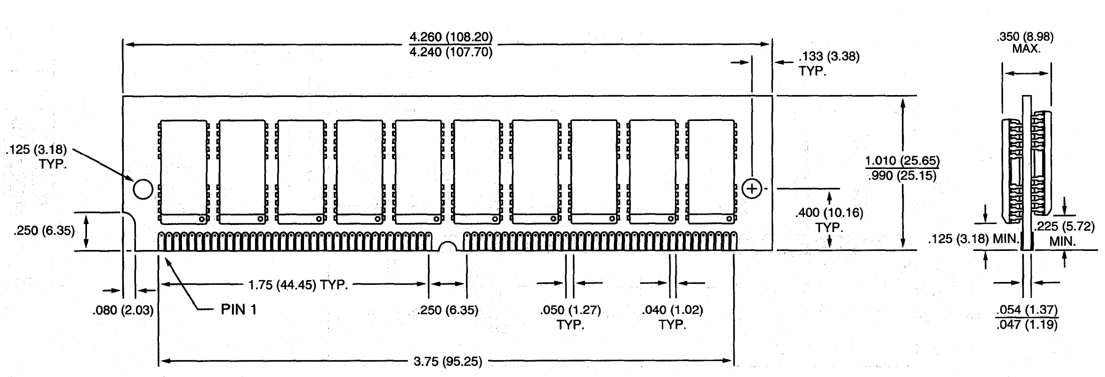
72-PIN MODULE SIMM
DE-9



72-PIN MODULE SIMM
DE-10



PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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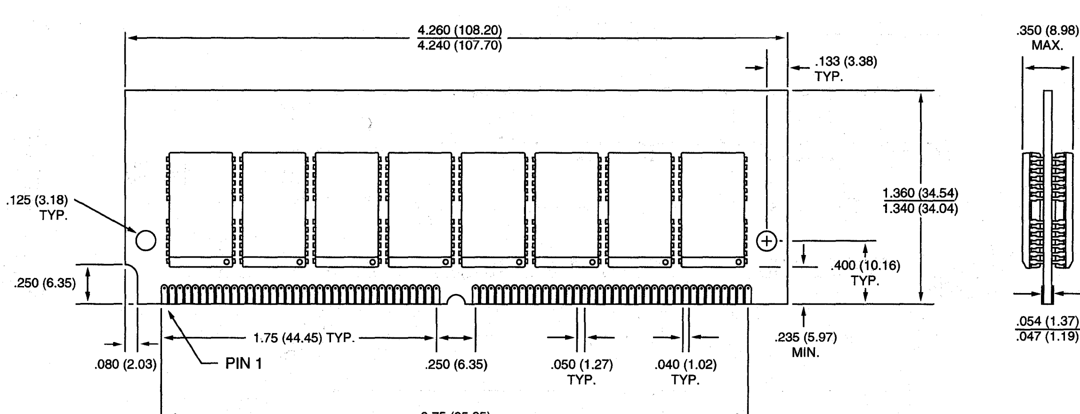
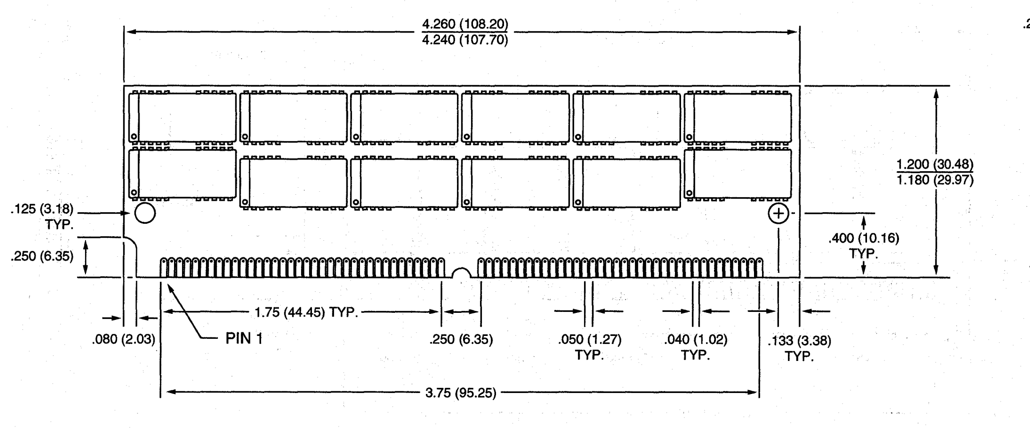
72-PIN MODULE SIMM
DE-11



72-PIN MODULE SIMM
DE-12



PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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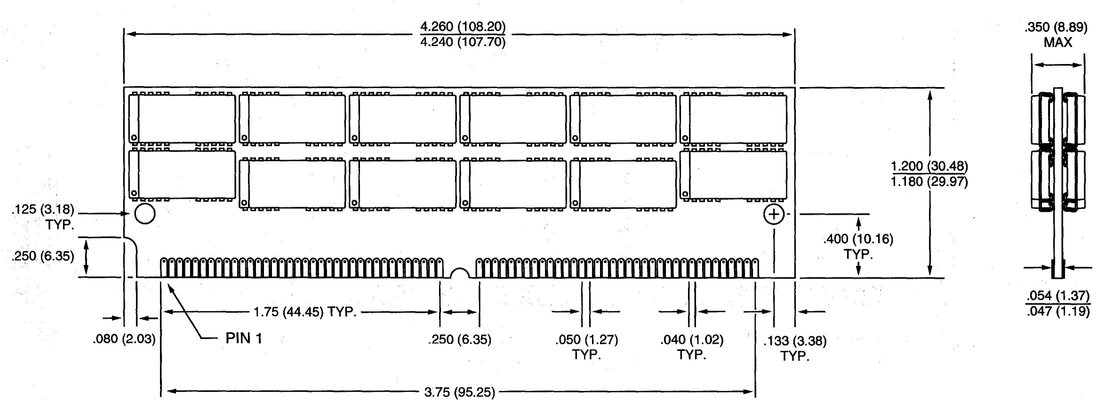
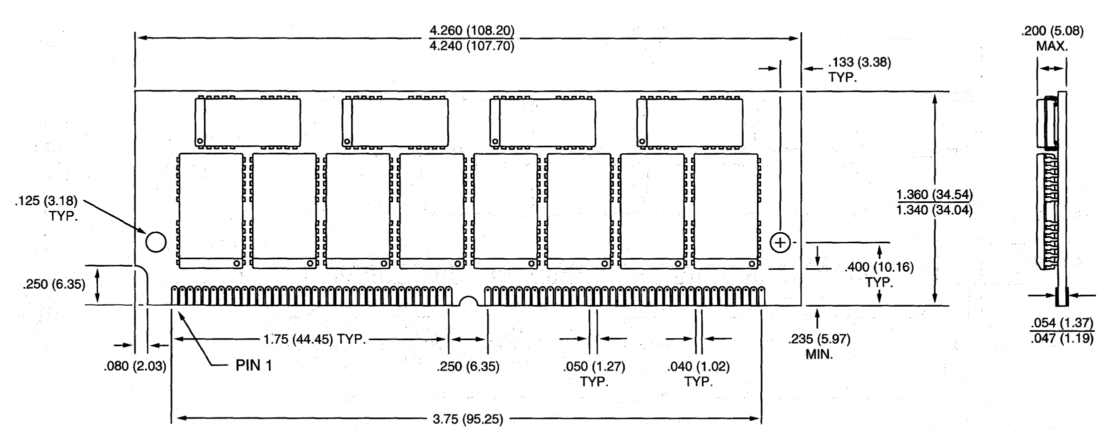
72-PIN MODULE SIMM

DE-13



72-PIN MODULE SIMM

DE-14



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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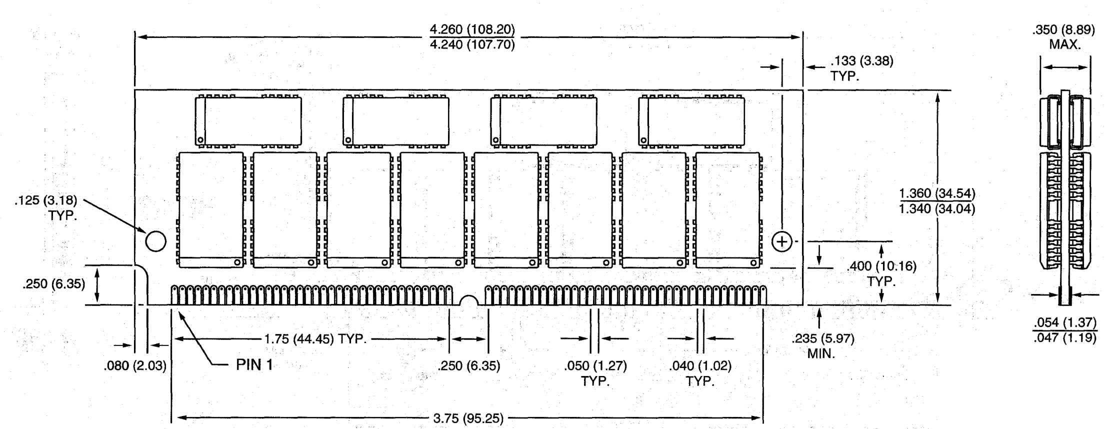
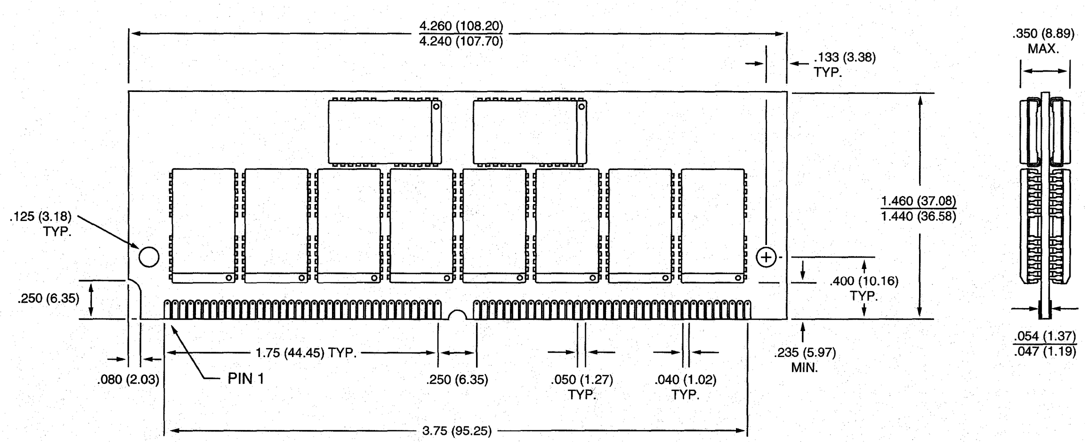
72-PIN MODULE SIMM
DE-15



72-PIN MODULE SIMM
DE-16



PACKAGE INFORMATION

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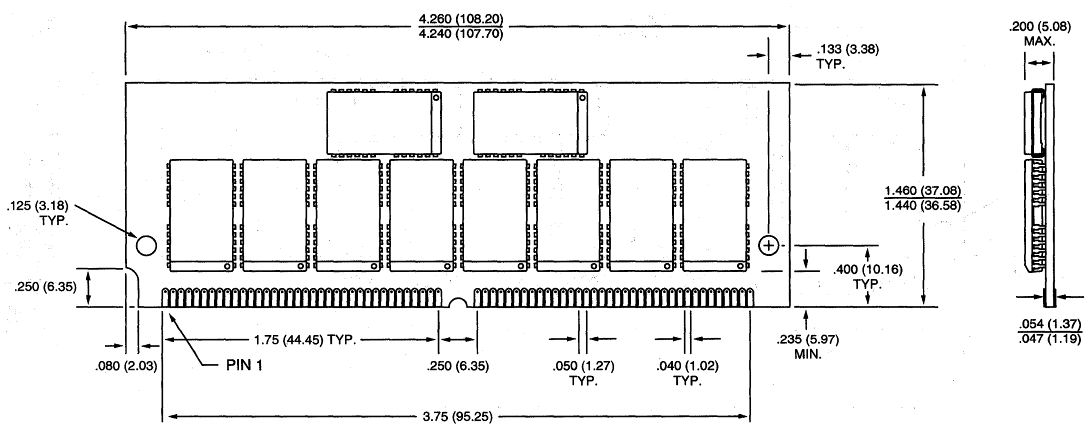
72-PIN MODULE SIMM

DE-17



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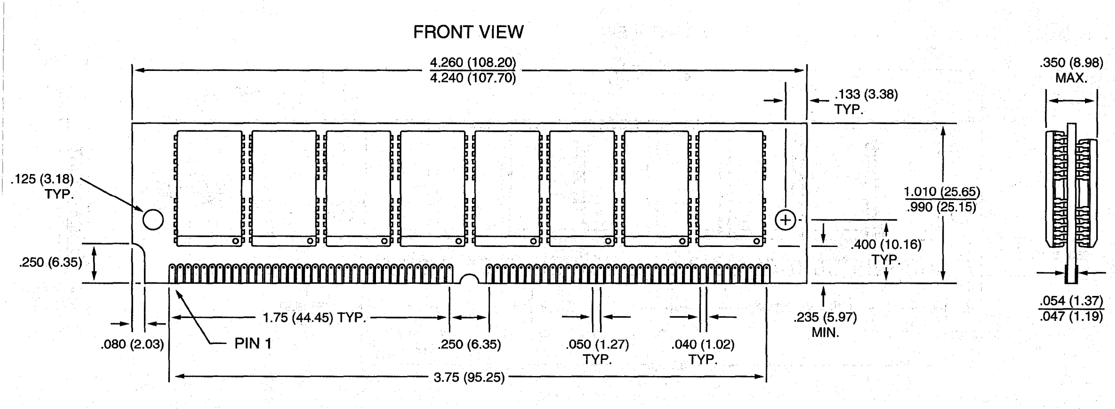
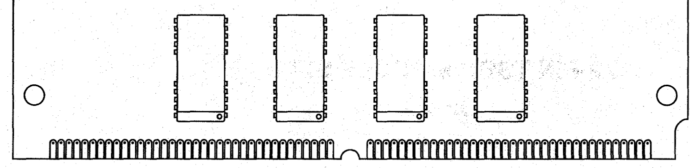
72-PIN MODULE SIMM

DE-18

FRONT VIEW



BACK VIEW



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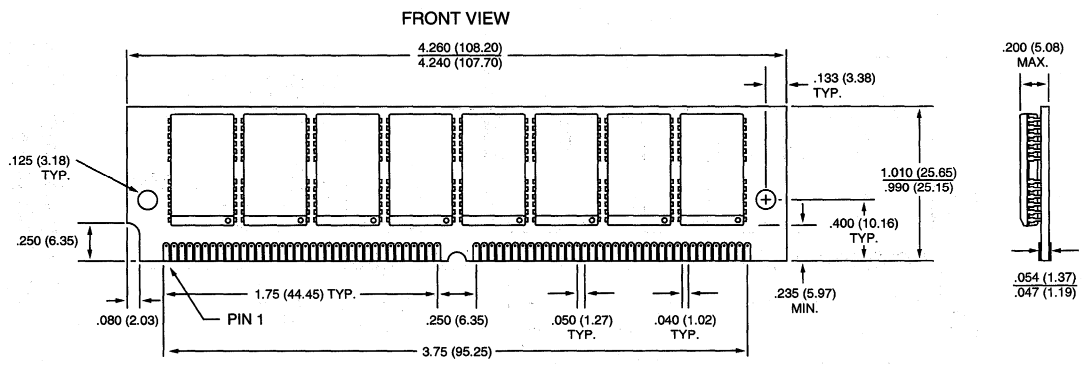
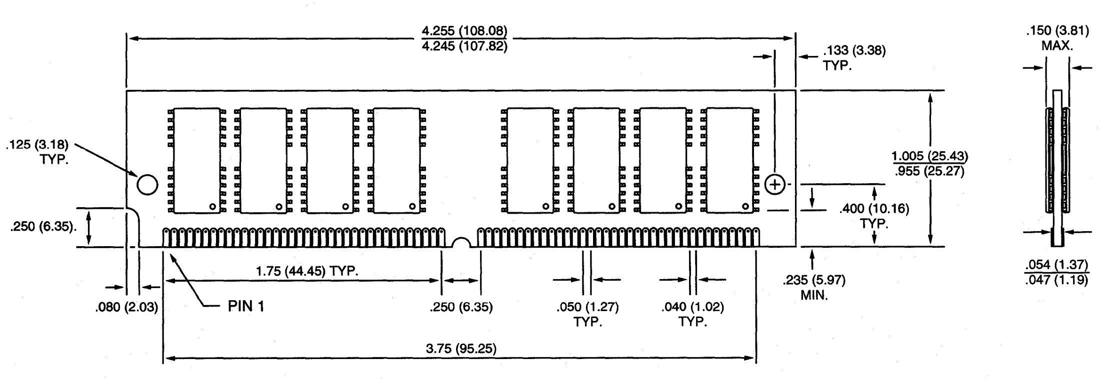
72-PIN MODULE SIMM
DE-19



72-PIN TSOP MODULE SIMM
DE-20



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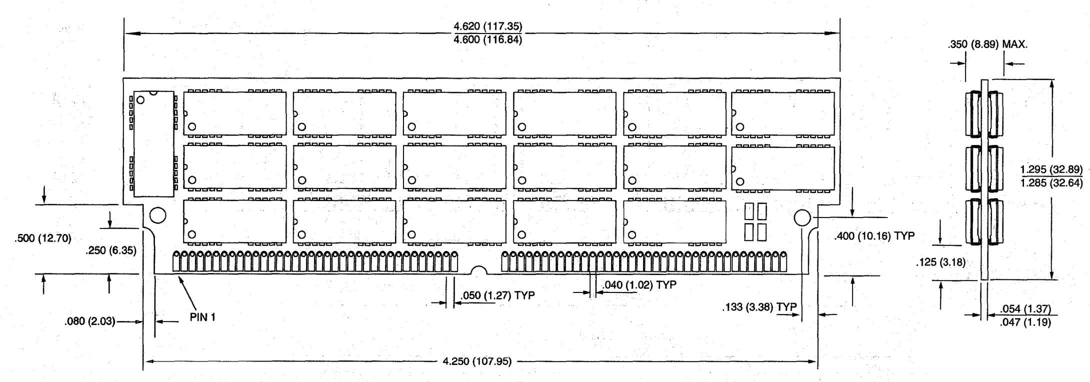
72-PIN MODULE SIMM

DE-21



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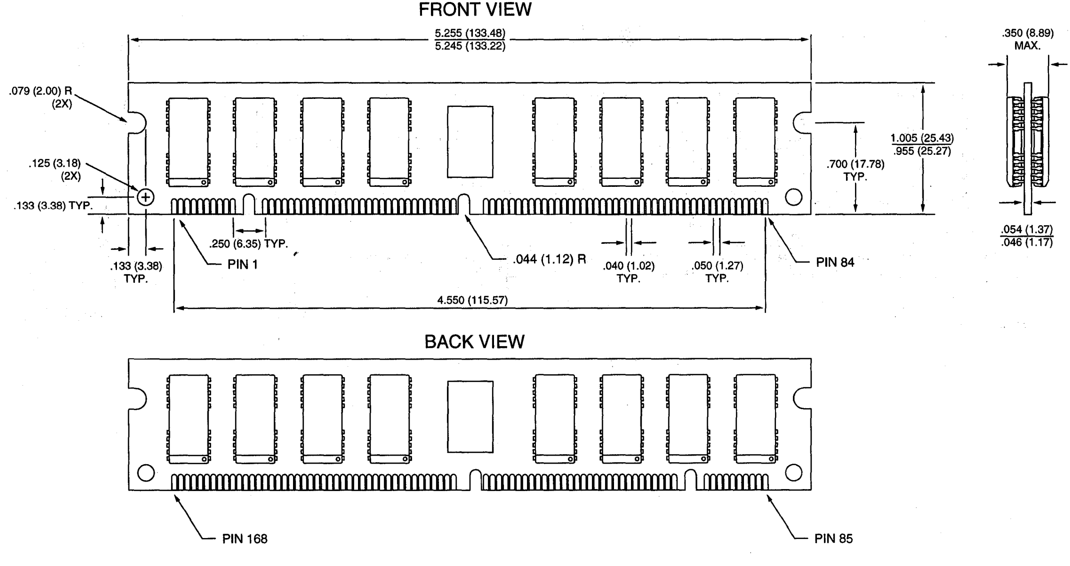
168-PIN TSOP MODULE DIMM

DE-22



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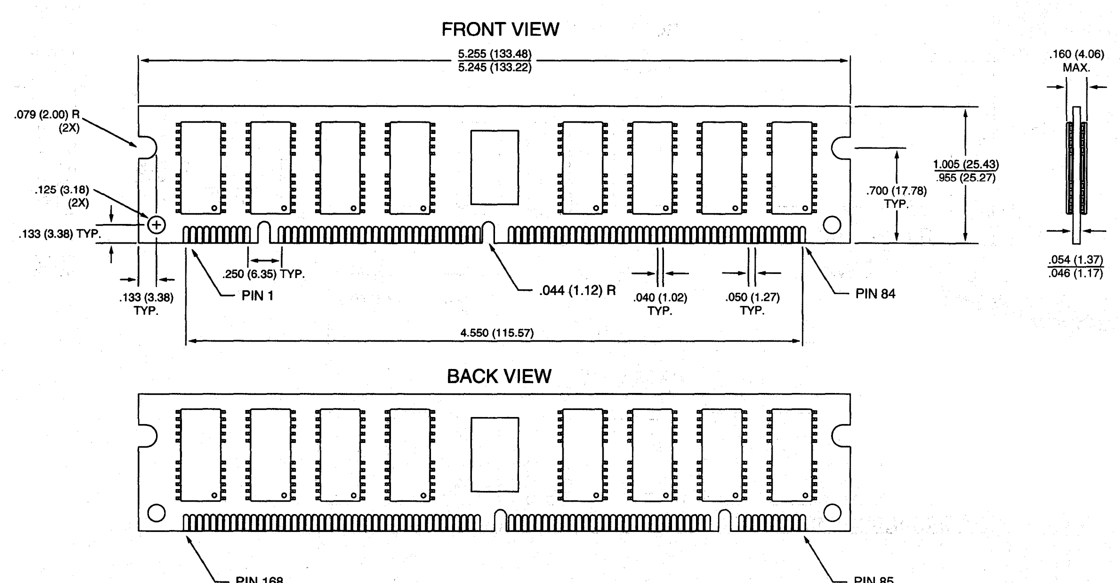
168-PIN MODULE DIMM

DE-23



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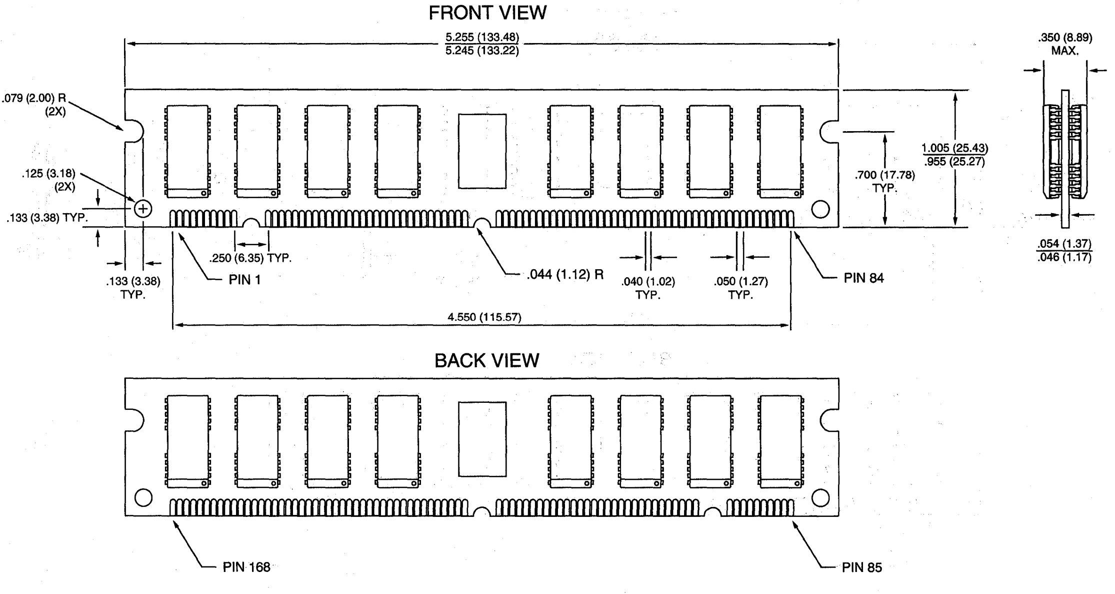
168-PIN MODULE DIMM

DE-24



PACKAGE INFORMATION

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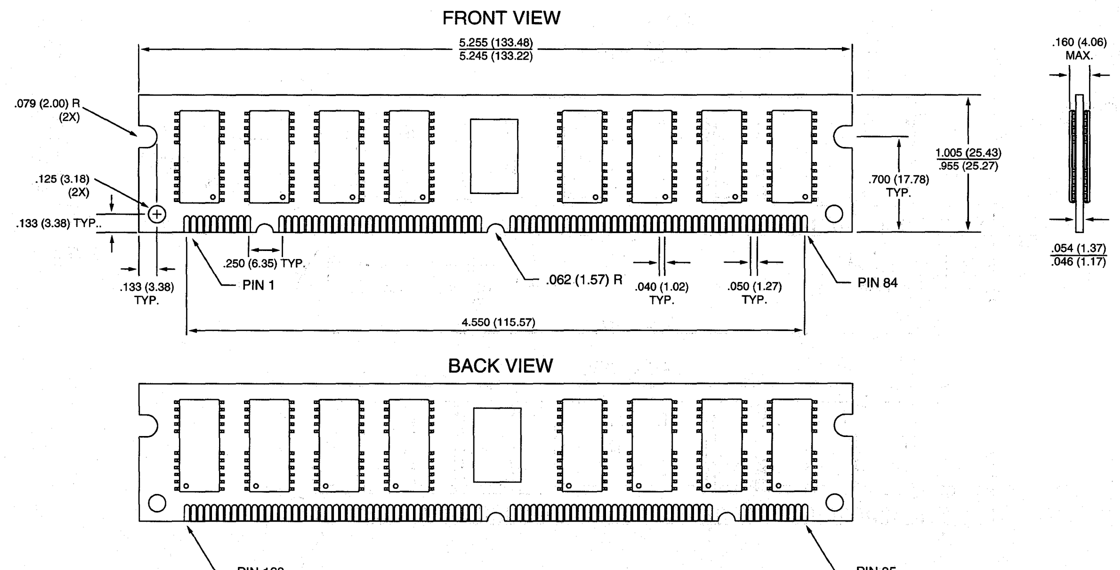
168-PIN MODULE DIMM

DE-25



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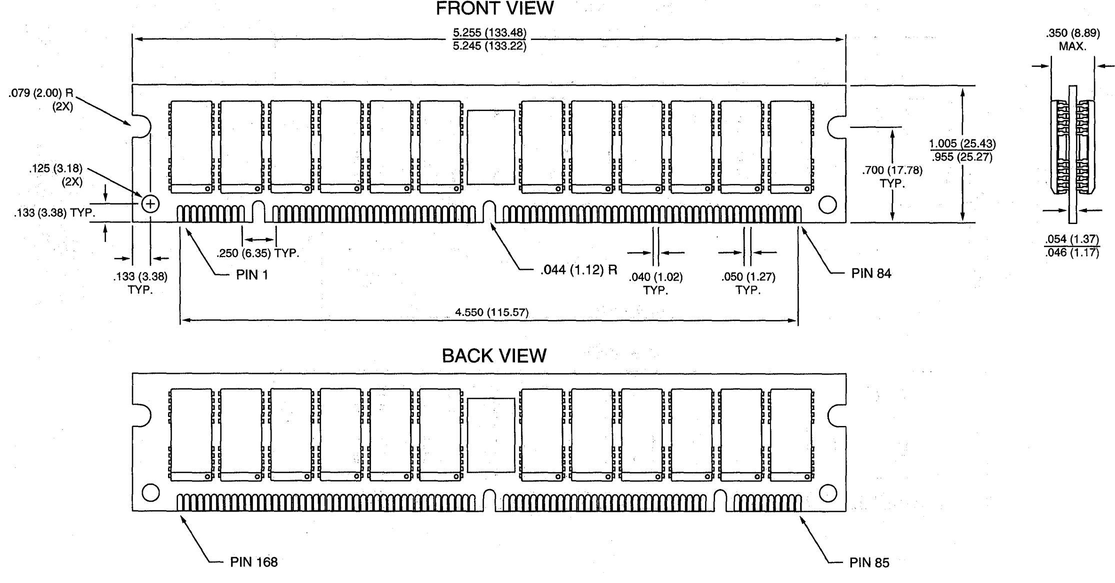
168-PIN MODULE DIMM

DE-26



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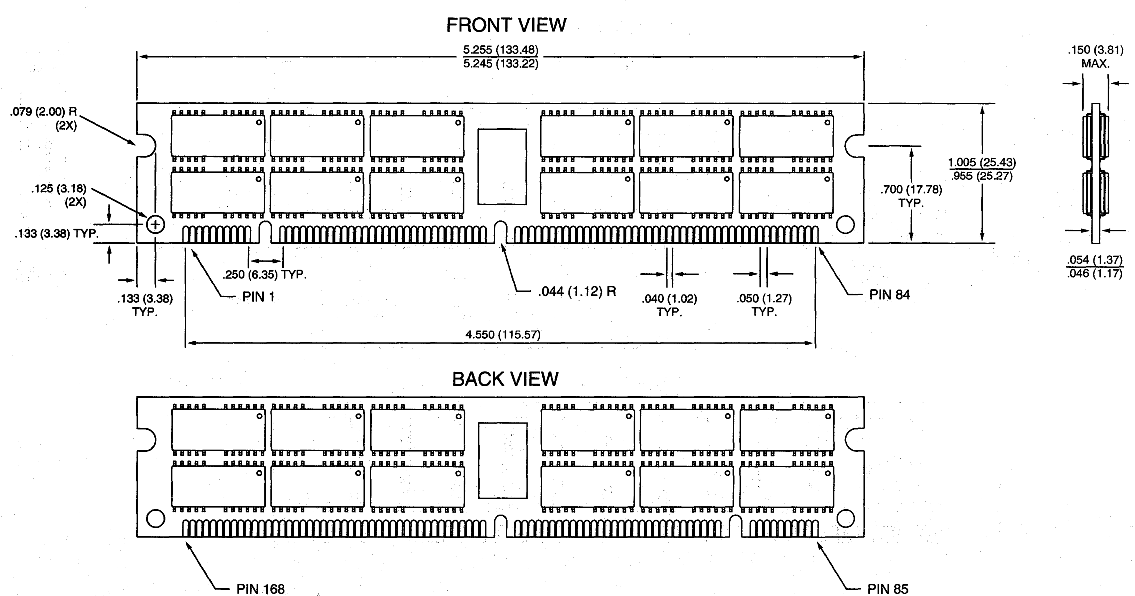
168-PIN MODULE DIMM

DE-27



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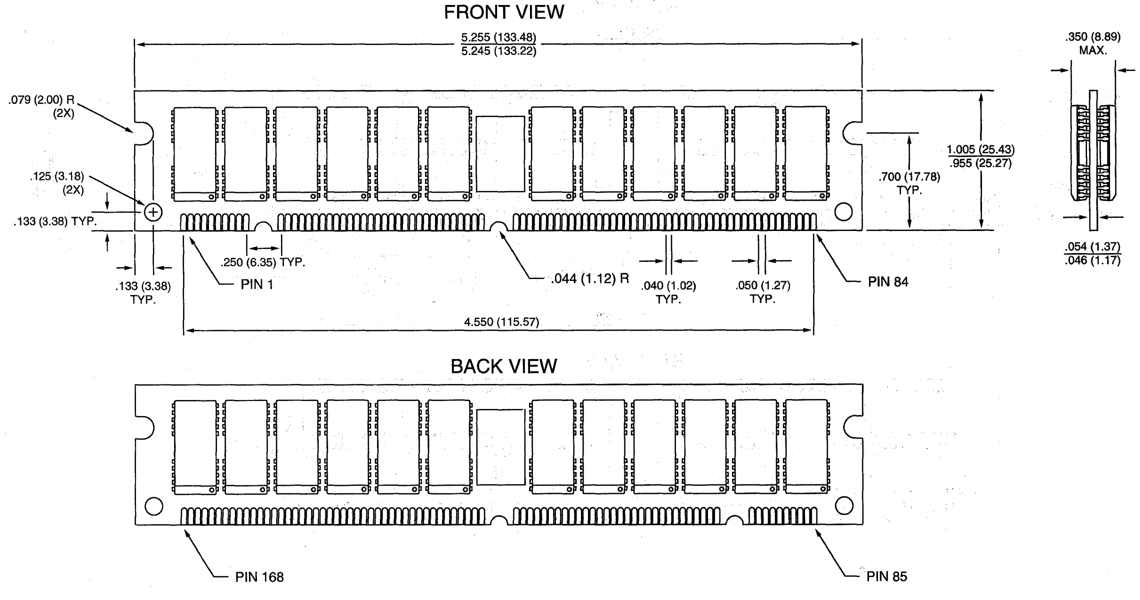
168-PIN MODULE DIMM

DE-28



PACKAGE INFORMATION

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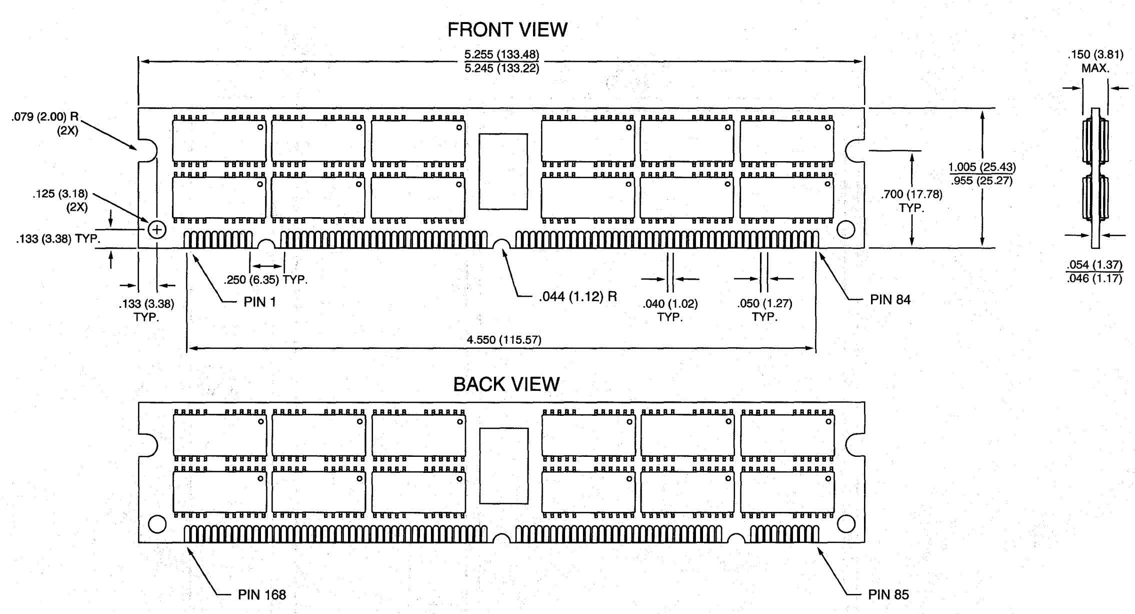
168-PIN MODULE DIMM

DE-29



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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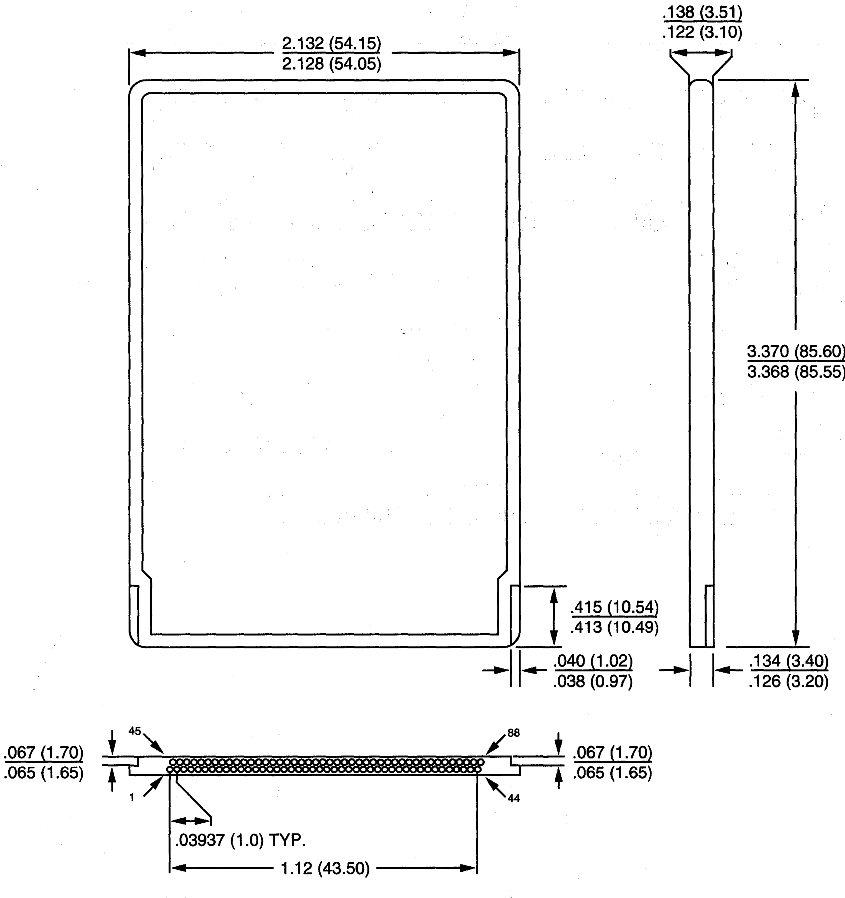
88-PIN DRAM CARD

DF-1



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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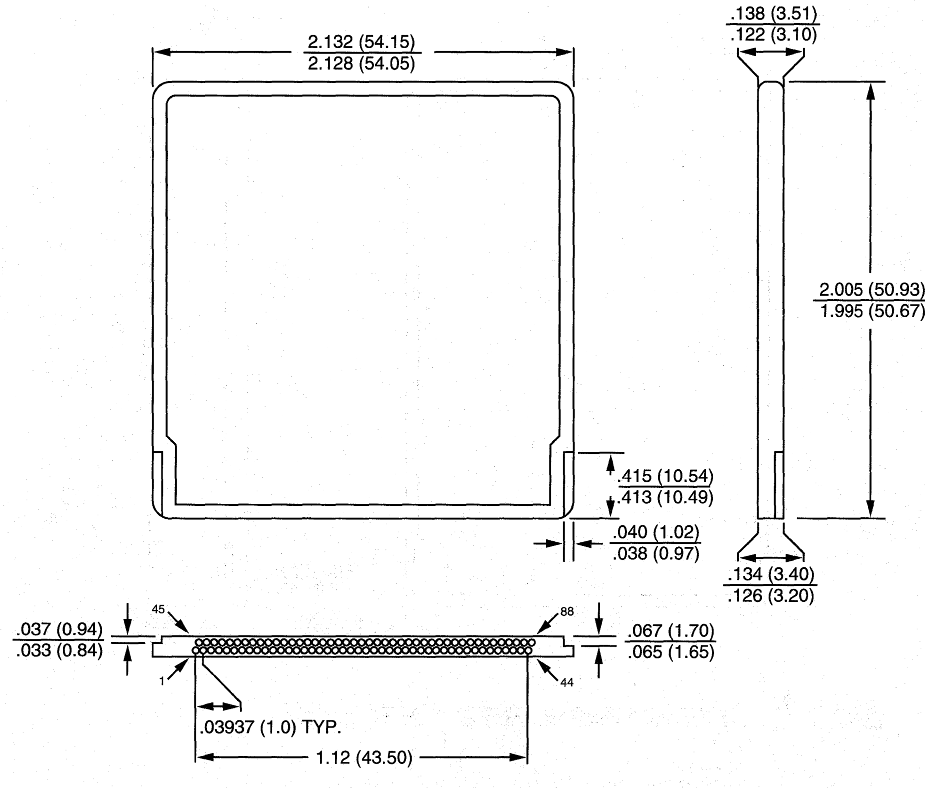
88-PIN REDUCED-LENGTH DRAM CARD

DF-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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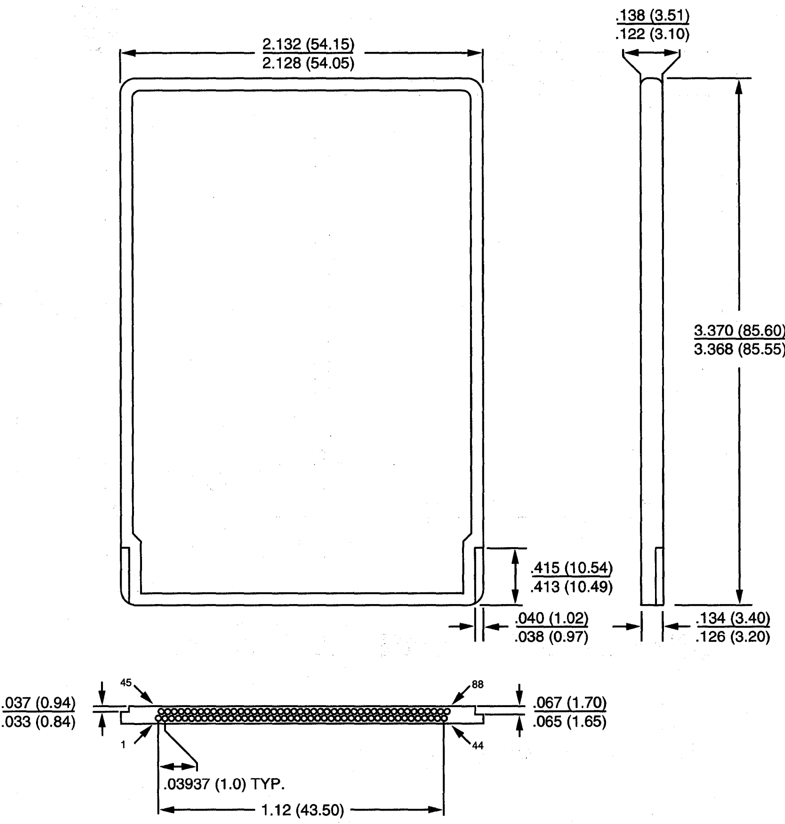
88-PIN DRAM CARD
DF-3



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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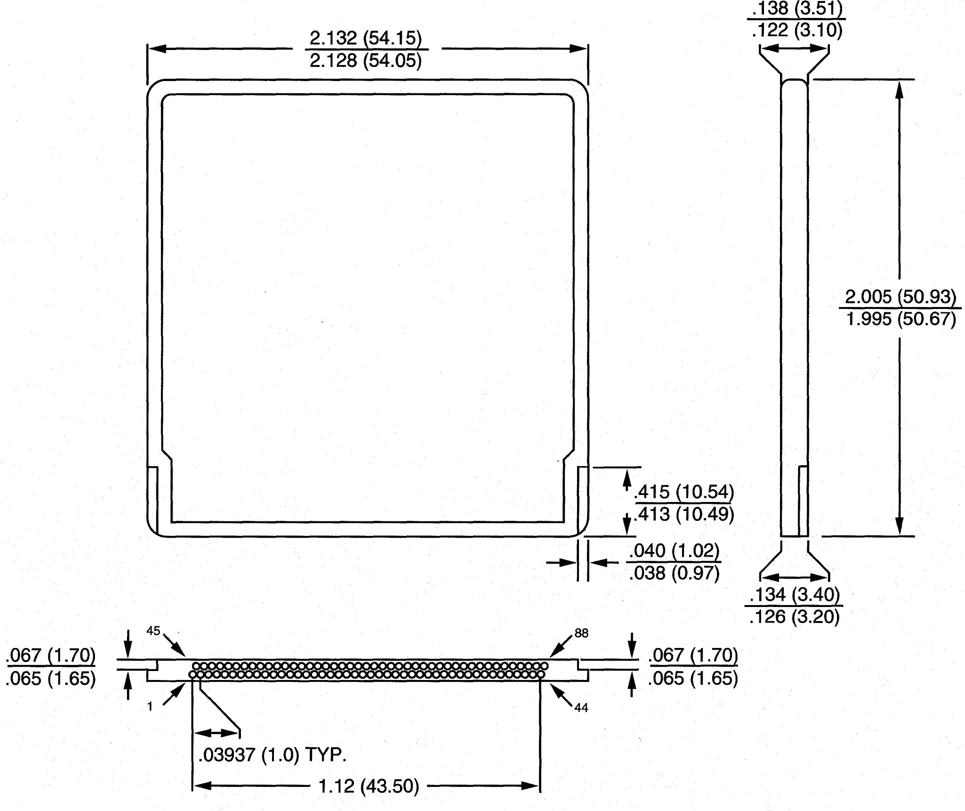
88-PIN REDUCED-LENGTH DRAM CARD

DF-4



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MICRON
SEMICONDUCTOR, INC.

CUSTOMER SERVICE NOTE

STANDARD SHIPPING BAR CODE LABELS

INTRODUCTION

Micron Semiconductor, Inc., has implemented standard bar coding labels that will accompany all shipments. These labels conform to EIA Standard 556.

Samples and tape-and-reel boxes will have their own individual bar code labels (see CSN-02). The bar code labels will allow customers to scan individual Micron containers for quick order verification. Figure 1 shows an example of the standard bar coding label.

BAR CODE INFORMATION

The information provided on the label is:

(S) — Serial: Individual box serial number

(13Q) — Special: Individual box number and total number of boxes in the shipment (example: 2 of 10)

(Q) — Quantity: Total quantity of parts in the box

(K) — Trans ID: Customer purchase order number

(P) — Customer Product ID: Customer part number

If a customer part number is not designated, the Micron part number will be printed.

ADDITIONAL SALES INFORMATION

Ship-to-Name: Customer's name and ship-to address
Ship-From-Name: Micron name and address
Lot Date Code: Indicates date of oldest lot in the box

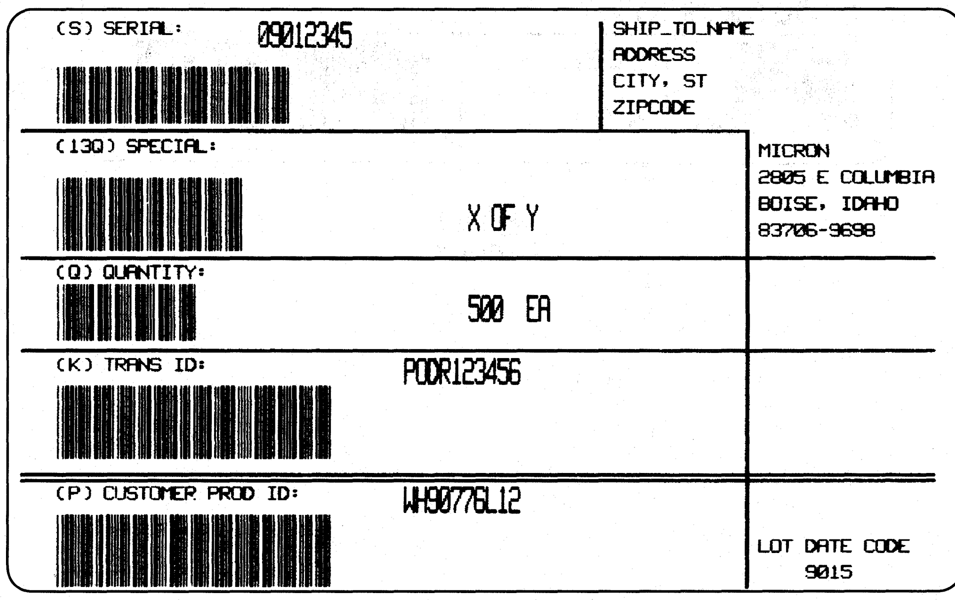

Figure 1
STANDARD BAR CODE LABEL

SALES INFORMATION

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CUSTOMER SERVICE NOTE

TAPE-AND-REEL/SAMPLE BAR CODE LABELS

INTRODUCTION

Micron Semiconductor, Inc., provides a standard bar code label on each individual sample and tape-and-reel box. The standard bar code label allows scanning of Micron shipping containers at a receiving dock for quick order verification.

Figure 1 shows an example of the standard bar code label.

BAR CODE INFORMATION

The information provided on the label is:

Label 1: Individual box number (in a multibox shipment)
Actual box number printed
Micron part number/speed/customer code
Part type/rev/quantity/date code of oldest lot*

Figure 1
LABEL 1

*Indicates that more than one date code is contained on the reel.

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CUSTOMER SERVICE NOTE

SURFACE-MOUNT PRODUCTS' SPC LABELS

INTRODUCTION

Micron Semiconductor, Inc., provides an SPC label on all surface-mount products. The label is attached to the static-proof bag for products packaged in tape-and-reel as well as tubes.

Figure 1 shows an example of the standard SPC label, while Figures 2 and 3 show the difference between the labels for tubed and tape-and-reel packaged products.

DATE INFORMATION

The SPC label includes the date on which the tube or reel was hermetically sealed in drypack. It also lists the ID number of the operator who sealed the product.

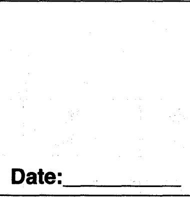

Figure 1
SURFACE-MOUNT PRODUCT SPC LABEL

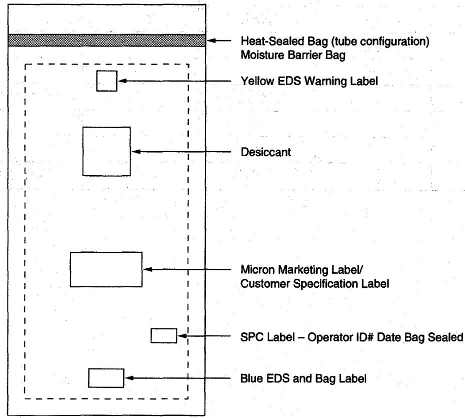

Figure 2
TUBED PRODUCT LABEL

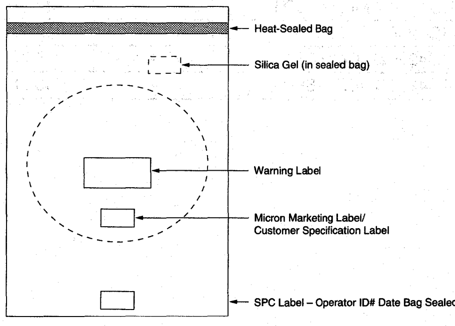

Figure 3
TAPE-AND-REEL PACKAGED PRODUCT LABEL

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CUSTOMER SERVICE NOTE

BOX AND TAPE-AND-REEL QUANTITY AND WEIGHT CHART

INTRODUCTION

Micron encourages customers to place orders in increments of standard box, tray and reel quantities whenever possible. The chart below will help determine order quantities.

ADDITIONAL SALES INFORMATION

Benefits to Micron's customers by ordering in standard quantities:

1. Cost Savings—it is less expensive to send a shipment containing full boxes.
2. Process Control—Micron's production tracking system automatically checks speeds, revs, customer codes and quantities. When standard box quantities are ordered, manual errors are eliminated, thus ensuring error-free shipments.
3. Lot Integrity—lot integrity is kept in tact when box quantities are not broken up.
4. Fewer returns—fewer errors equal fewer complaints and returns.

Part Type	Quantity Per Tray	Quantity Per Box	Lbs Per Box	Quantity Per Tube	Tape-and-Reel Quantity	Lbs Per Reel	Tape Size
DRAMs							
MT4C4MB1DW-4C4M4A1DW	—	2000	—	25	500	—	
MT4C1004DJ-4C1006DJ	—	4000	13.2	25	1000	4.1	24mm x 12mm
MT4C4001DJ-4C4003DJ	—	4000	13.2	25	1000	4.1	24mm x 12mm
MT4C1004JZ-4C4001JZ	—	2500	13.1	20	—	—	
4C4003JZ	—	2500	13.1	20	—	—	
MT4C1004TG-4C4001TG	84	1000	8.0	—	1000	2.7	24mm x 12mm
4LC4001DJ	—	4000	13.2	25	1000	4.1	24mm x 12mm
4LC4001TG	84	1000	8.0	—	1000	2.7	24mm x 12mm
MT4C1024-4C1026	—	2000	10.6	20	—	—	
MT4C1024Z-4C1026Z	—	2500	12.7	20	—	—	
MT4C1024DJ-4C1026DJ	—	4000	13.1	25	1000	4.1	24mm x 12mm
MT4C4256-4C4258	—	1800	10.7	18	—	—	
MT4C4256Z-4C4258Z	—	2500	12.7	20	—	—	
MT4C4256DJ-4C4258DJ	—	4000	13.1	25	1000	4.1	24mm x 12mm

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CUSTOMER SERVICE NOTE

ENVIRONMENTAL PROGRAMS

INTRODUCTION

Environmental issues such as the depletion of the ozone layer by chlorofluorocarbons (CFCs) affect everyone. Micron Semiconductor, Inc., takes a proactive approach to eliminating hazardous and polluting chemicals by educating and involving our workforce in their removal. We have eliminated ozone-depleting chemicals (ODCs) from the manufacturing process. Micron is in full compliance with Section 611 of the Clean Air Act and does not have to label any product to the contrary. We believe a proactive approach to environmental responsibility is not only environmentally advantageous, but gives the company a long-term competitive advantage.

COMPLETED TEAM PROJECTS

WET SIDE ECONOMIZER

This system, developed by Micron engineers in 1987, saves the company $150,000 annually. The Wet Side Economizer uses cold air rather than refrigeration to cool the manufacturing complex. This system reduces kwh consumption by 15.1 million, which translates into a 11,174-ton reduction in CO^2 emissions, a 121-ton reduction in SO^2 emissions, and a 53-ton cut in NO_X emissions. The system earned Micron a Certificate of Recognition for Energy Consciousness from the state of Idaho and an award for Energy Innovation from the federal Department of Energy in 1991.

AQUEOUS CLEANING

Micron's Custom Manufacturing Services group researched the possibility of switching from solvent-based CFC cleaners to aqueous (water only) cleaning in early 1990. The group eliminated all CFC-based solvents in October 1991 and discovered that the new aqueous cleaning process proved more effective and cheaper than the solvent-based process.

REFRIGERANTS

Micron's Plant Operations group has installed high-efficiency purge pumps that exceed EPA specifications on refrigeration units in order to eliminate the discharge of refrigerants into the atmosphere. In addition, portable refrigerant reclaim units are used to recover and recycle refrigerants during maintenance or when equipment is retired.

FIRE EXTINGUISHERS

Micron eliminated the use of all halon fire extinguishers in 1993. They were replaced with more environmentally safe units according to their application. The quick elimination of ozone-depleting chemicals such as halon saves the company money because the price of these chemicals goes up as manufacturers discontinue their production.

WATER TREATMENT FACILITY

During the past year, Micron has allocated $10 million for the first phase of a new industrial waste water pretreatment facility. The facility is designed to reclaim process waste waters and reduce ground water usage by 50 percent in the first phase. The final $5 million phase, scheduled for completion in 1997, will reduce ground water use by 80 percent.

RECYCLING

Several Micron teams have developed systems to recycle items for sale to outside customers or reuse within the manufacturing process. These items include sulfuric acid, gold, various solvents and alcohols, scrap metal, wire, aluminum and steel cans, buckets and barrels, pallets, plastic, and cardboard and paper products.

GLYCOL ETHER ELIMINATION

Micron has instituted a program to eliminate glycol ethers, which have been implicated as reproductive toxins.

ONGOING TEAM PROJECTS

VOLATILE ORGANIC COMPOUNDS (VOCS)

The goal of this team project is to reduce VOC emissions by 90 percent within one year.

HAZARDOUS AIR POLLUTANTS

This project focuses on reducing the use of MEK, acetone, toluene and methanol by 90 percent by the spring of 1994.

HAZARDOUS WASTE REDUCTION

This ongoing team focuses on reducing all hazardous wastes. Chemical usage is screened and chemicals containing toxic substances are included on a "hit list." The team works to reduce or eliminate the use of these hit list chemicals. If the chemical cannot be immediately eliminated,

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team members work with lab staff, plant operations, and production engineering to find substitutes for the chemicals that contain the toxic substances.

POLLUTION ABATEMENT

Micron is working with a start-up company on a new approach to abating organic compounds. Our chemistry group also continuously reviews existing abatement technologies.

ENVIRONMENTAL BENCHMARKING

The benchmarking team reviews environmental programs that are successful in other semiconductor facilities and develops a shared network of information.

SUPPLIER ASSISTANCE

Micron offers assistance to suppliers to help eliminate toxic substances in chemicals or products they provide. A Micron team is currently working with suppliers to eliminate perfluorinated compounds that contribute to global warming.

COMMUNITY ASSISTANCE

Micron volunteers lab resources and provides consultation to local companies and community organizations, such as the Peregrine Fund, to help resolve industrial hygiene and environmental issues. Micron team members are active in local environmental and safety organizations and in the Community Emergency Planning Committee. They also periodically host training classes (such as Hazardous Gas Bottle Handling and Disposal) for local professional organizations.

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CUSTOMER SERVICE NOTE

ELECTRONIC DATA INTERCHANGE

INTRODUCTION

Electronic Data Interchange (EDI) has become an important data transmission element in today's marketplace. Micron is ready to serve your EDI needs and encourages customer participation.

STANDARDS SUPPORTED

X.12

Micron supports versions 002000 through 003020 for all implemented transaction sets. The addition of new versions is an automated process which drives off of the standard diskettes available through Data Interchange Standards Association.

EDIFACT

Micron supports EDIFACT under the 90.1 EDIFICE guidelines for the Purchase Order (PO), PO Acknowledgment, PO Change and PO Change Acknowledgment messages.

TRANSACTION SETS

Inbound	Outbound
850 - PO	855 - PO Acknowledgment
860 - PO Change	865 - PO Change Acknowledgment
840 - Request For Quote (RFQ)	843 - Response to RFQ
830 - Forecast	856 - Advanced Ship Notice
846 - Inventory Inquiry/ Advice	810 - Invoice
867 - Product Transfer & Resale	
844 - Product Transfer Account Adjustment (PTAA)	849 - Response to PTAA
997 - Functional Acknowledgment	

VALUE ADDED NETWORKS

A T & T

A T & T allows our partners to transmit EDI documents via standard protocol or X.400 (e-mail protocol).

Advantis

Advantis is the result of a merger between the Sears and IBM networks.

TRANSMISSION TIMES

Transmission times are 2 a.m., 10 a.m., 1 p.m., 3 p.m. and 8 p.m. MST weekdays and 1 p.m. MST on weekends. Additional transmission times can be added easily as circumstances warrant.

MICRON EDI CONTACTS

EDI Project Leader	EDI Software Development
Becka Shirrod	Tony Holden
208-368-3338	208-368-3855

STEPS TO IMPLEMENTATION

The following are typical steps taken as Micron begins exchanging EDI data with a new trading partner:

- Micron receives an implementation guide from a trading partner
- Micron's EDI team contacts the trading partner's EDI coordinator to set up a trading partnership and coordinate the transmission and receipt of test documents
- Micron receives a test EDI document from the partner's VAN and responds with the necessary acknowledgments
- Once both parties agree everything is working properly, parallel testing with EDI and paper documents begins
- Micron insures an EDI agreement has been signed and returned to the trading partner
- Paper documents are replaced with EDI documents (full production).

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CUSTOMER SERVICE NOTE

RETURN MATERIAL AUTHORIZATION (RMA) PROCEDURES

HOW TO RETURN PRODUCT TO MICRON

- Obtain an RMA number (see "How to Obtain an RMA" below).
- Package product taking all antistatic precautions.
- Write RMA number on outside of box for proper routing.
- Ship package prepaid to:
  Micron Semiconductor, Inc.
  Attn.: RMA Area
  2805 East Columbia Road
  Boise, ID 83706
- If RMA is being shipped from outside of the United States, please note that Boise, Idaho, is a customs port city; reference Port City Code 2907.

HOW TO OBTAIN AN RMA

NONFAILURE-RELATED RETURNS:

- If you buy direct, contact your Micron sales rep at 1-208-368-3900.
- If you buy through a Micron rep, contact that rep.
- If you buy through Distribution, contact the distributor.

Provide the Following Information:
- Micron part number, including speed and package
- Reason for return
- One of the following: PO number, invoice number, or sales order number
- One of the following: replacement parts, credit only, or refund

FAILURE-RELATED RETURNS AND/OR APPLICATION PROBLEMS:

- Contact Micron Application Engineering Department at 1-208-368-3900

Provide the Following Information:
- Micron part number, including speed and package
- Type of failure
- Name of engineer who witnessed failure or requested failure analysis report
- One of the following: PO number, invoice number, or sales order number
- One of the following: replacement parts, credit only, or refund

FAILURE ANALYSIS STANDARDS FOR RETURN MATERIAL AUTHORIZATIONS:

- Upon receipt of an RMA for failure analysis, Micron's Quality Assurance Department will provide an initial response within 48 hours.
- Micron's Quality Assurance Department will issue a completed failure analysis report within three weeks of receiving an RMA.

MICRON ACCOUNTING PROCEDURES FOR RETURN MATERIAL AUTHORIZATIONS

- Replacements: Replacement parts are shipped after receipt of the RMA parts. The credit memo will be applied directly to the replacement invoice. A new invoice will be sent when the replacement amount is greater than the returned amount. If this is not compatible with your accounts payable procedures, please advise your sales rep upon RMA request.
- Credit: A credit memo is sent out for the amount of the return upon arrival of the RMA parts. This credit memo number should be referenced when sending in payment information if intended to be used.
- Refund: A check request is submitted to Micron Accounts Payable upon receipt of RMA parts. A refund check is sent upon completion of the check request approval process.

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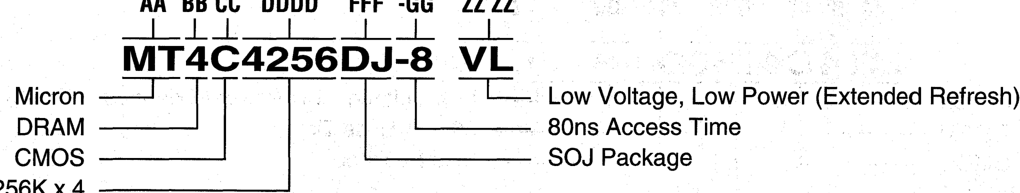
EXPANDED COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product ..... MT

BB – PRODUCT FAMILY

DRAM 4
DPDRAM (VRAM) 42
TPDRAM 43
SRAM 5
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

DRAM ..... Width, Density
DPDRAM (VRAM) ..... Width, Density
TPDRAM ..... Width, Density
SRAM ..... Total Bits, Width
Synchronous SRAM ..... Density, Width

E – DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required.)

JEDEC Test Mode (4 Meg DRAM) ..... J
Errata on Base Part ..... Q

FFF – PACKAGE CODES

PLASTIC

DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG
QFP ..... LG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL

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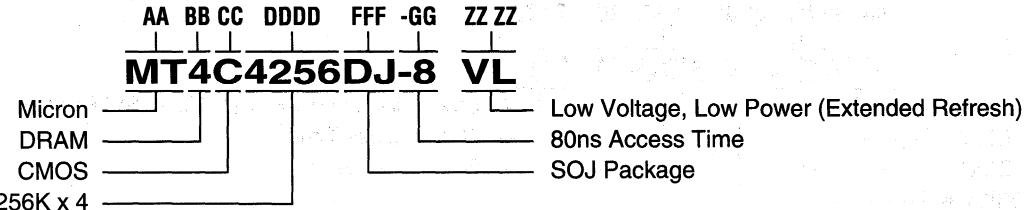
EXPANDED COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

Code	Access Time
-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-50 (SRAM only)	50ns
-53	53ns
-55	55ns
-70 (SRAM only)	70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

Processing	Code
Interim	I
Low Voltage	V

ZZ ZZ – PROCESSING CODES (continued)

Processing	Code
DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh)	S
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

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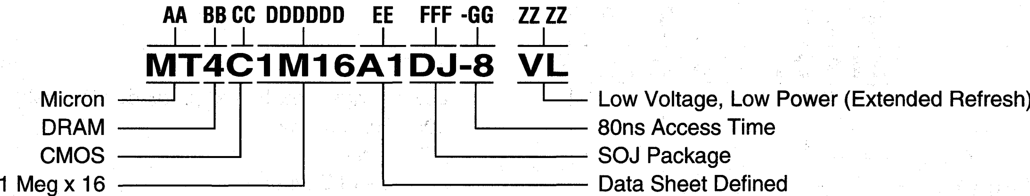
NEW COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product .... MT

BB – PRODUCT FAMILY

DRAM 4
DPDRAM (VRAM) 42
TPDRAM 43
Synchronous DRAM 48
SRAM 5
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC
BiCMOS .... B
Low Voltage BiCMOS .... LB

DDDDDD – DEVICE NUMBER

Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter .... Bits
K .... Kilobits
M .... Megabits
G .... Gigabits

EE – DEVICE VERSIONS

(The first character is an alphabetic character only; the second character is a numeric character only.)
Specified by individual data sheet.

FFF – PACKAGE CODES

Plastic

DIP .... Blank
DIP (Wide Body) .... W
ZIP .... Z
LCC .... EJ
SOP/SOIC .... SG
QFP .... LG
TSOP (Type II) .... TG
TSOP (Reversed) .... RG
TSOP (Longer) .... TL
SOJ .... DJ
SOJ (Wide) .... DW
SOJ (Reversed) .... DR
SOJ (Longer) .... DL

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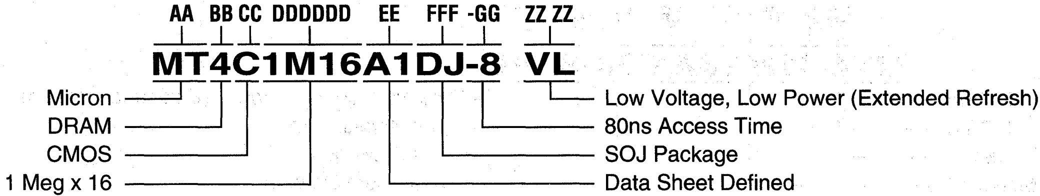
NEW COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

Code	Access Time
-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-9	9ns or 90ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-53	53ns
-55	55ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

Code	
Interim	I
Low Voltage	V

ZZ ZZ – PROCESSING CODES (continued)

	Code
DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh)	S
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Volt Data Retention, Low Power	LP
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

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MODULE NUMBERING SYSTEM

AA BB C DDD EEE FFF GG HH JJ KK

MT12LD136xxG-7 L

- Micron (MT)
- 12 Components (12)
- 3.3 Volt (L)
- DRAM Module (D)
- 1 Meg (1)
- x36 (36)
- Device Version (xx)
- Gold Plating (G)
- 70ns Access Time (-7)
- DRAM Low Power (L)

AA – PRODUCT LINE IDENTIFIER

Micron Semiconductor Product .... MT

BB – NUMBER OF MEMORY COMPONENTS

C – PROCESS TECHNOLOGY

LOW VOLTAGE (3.3V) L

DDD – RAM FAMILY

DRAM .... D
DRAM TSOP .... DT
SRAM .... S
SRAM TSOP .... ST
SYNCHRONOUS SRAM .... SY
SYNCHRONOUS SRAM TQFP .... SYT
VRAM V

EEE – DEPTH

FFF – WIDTH

GG – DEVICE VERSIONS

Specified by individual data sheet (Synchronous SRAM only)

HH – PACKAGE CODE

Gold Plated SIMM/DIMM .... G
ZIP .... Z
SIP .... N
SIMM/DIMM .... M
Small Outline DIMM .... H
Small Outline Gold DIMM .... HG
Double-Sided SIMM (1 or 4 Meg x 36 Only) .... DM
Double-Sided SIMM (Gold 1 or 4 Meg x 36 Only) .... DG

JJ – ACCESS TIME

-10 .... 10ns or 100ns
-12 .... 12ns
-15 .... 15ns
-17 .... 17ns
-20 .... 20ns
-25 .... 25ns
-35 .... 35ns
-6 .... 60ns
-7 .... 70ns
-8 .... 80ns

KK – MODULE SPECIAL DESIGNATOR

SRAM
- 2V data retention L
- Low Power .... P
- Low Power, 2V data retention .... LP

DRAM
- Low Power (Extended Refresh) L
- ECC C
- Extended Data Out X
- Self Refresh .... S
- 16 Meg DRAM 4,096 Refresh .... B

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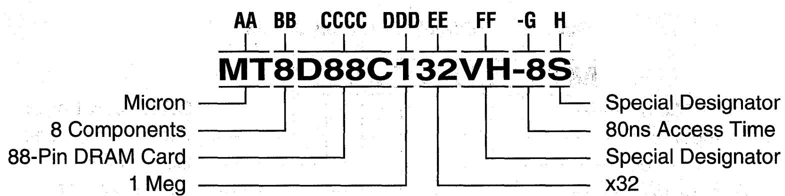
DRAM CARD NUMBERING SYSTEM



AA – Product Line Identifier
Micron Product .... MT

BB – NUMBER OF MEMORY COMPONENTS

CCCC – DRAM CARD DESIGNATOR AND PIN COUNT
88-Pin DRAM Card D88C

DDD – DEPTH

EE – WIDTH

FF – SPECIAL DESIGNATOR
3.3 Volts V
Reduced length (2") .... H

G – ACCESS TIME
-5 .... 50ns
-6 .... 60ns
-7 .... 70ns
-8 .... 80ns

H– SPECIAL DESIGNATOR
Self Refresh .... S

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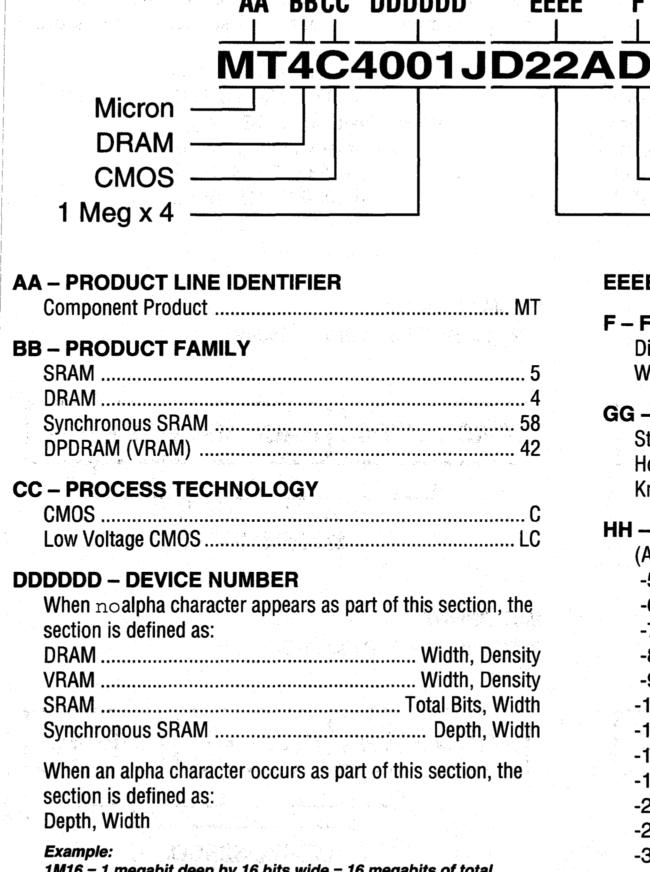
DIE PRODUCT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Component Product .... MT

BB – PRODUCT FAMILY

SRAM 5
DRAM 4
Synchronous SRAM 58
DPDRAM (VRAM) 42

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC

DDDDDD – DEVICE NUMBER

When no alpha character appears as part of this section, the section is defined as:

DRAM .... Width, Density
VRAM .... Width, Density
SRAM .... Total Bits, Width
Synchronous SRAM .... Depth, Width

When an alpha character occurs as part of this section, the section is defined as:
Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter .... Bits
K .... Kilobits
M .... Megabits
G .... Gigabits

EEEE – DIE DATA BASE REVISION

F – FORM

Die Form .... D
Wafer Form (6" Wafer) .... W

GG – TESTING LEVELS

Standard Probe (0° to 70°C) C1
Hot Speed Probe (0° to 70°C) C2
Known Good Die (0° to 70°C) C3

HH – ACCESS TIME

(Applicable for C2 and C3 only)

-5 .... 5ns or 50ns
-6 .... 6ns or 60ns
-7 .... 7ns or 70ns
-8 .... 8ns or 80ns
-9 .... 9ns or 90ns
-10 .... 10ns or 100ns
-12 .... 12ns or 120ns
-15 .... 15ns or 150ns
-17 .... 17ns
-20 .... 20ns
-25 .... 25ns
-35 .... 35ns
-45 .... 45ns
-50 (SRAM only) 50ns

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ORDER INFORMATION*

Each Micron component family is manufactured and quality controlled in the U.S.A. at our modern Boise, Idaho, facility employing Micron's low-power, high-performance CMOS silicon-gate process. Micron products are functionally equivalent to other manufacturers' products meeting JEDEC standards. Device functionality is consistently assured over a wider power supply, temperature range and refresh range than specified. Each unit receives continuous system-level testing during many hours of accelerated burn-in prior to final test and shipment. This testing is performed with Micron's exclusive AMBYX intelligent burn-in and test system.

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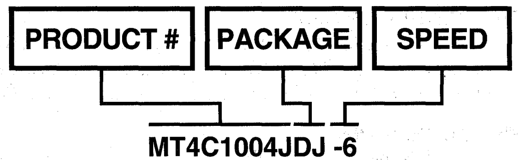
Fax: 208-368-4431
Micron DataFax: 208-368-5802
Customer Comment Line:
800-932-4992 (U.S.A.)
01-208-368-3410 (Intl.)

ORDER EXAMPLES

DRAM

4 Meg x 1, 60ns in Plastic SOJ



DRAM MODULE

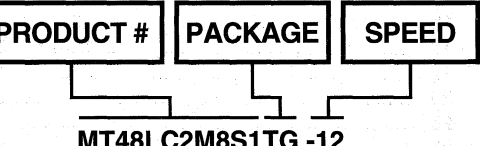
4 Meg x 32, 70ns in SIMM Module

PRODUCT # PACKAGE SPEED

MT8D432M -7

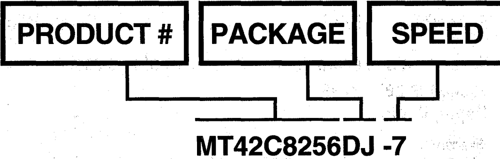
SYNCHRONOUS DRAM

2 Meg x 8, 12ns in Plastic TSOP



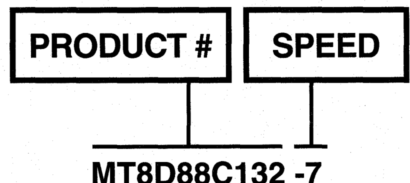
MULTIPORT

256K x 8, 70ns in Plastic SOJ



DRAM CARD

1 Meg x 32, 70ns DRAM Card



*For more detailed information, refer to the product numbering charts on pages 8-9 through 8-15.

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