High Speed Programmable Array Logic Family

PAL® Series 20AP With Programmable Output Polarity

U.S. Patent 4124899

Features/Benefits

- **15 ns typical propagation delay**
- **Programmable output polarity**
- **Power-up reset for all registers**
- **Preload feature during testing**
- **Programmable replacement for TTL logic**
- **Reduces chip count by greater than 4 to 1**
- **Expedites prototyping and board layout**
- **Programmed on standard PAL/PROM programmers**
- **Programmable three-state outputs**
- **Last fuse prevents duplication on a PAL/PROM programmer**

Functional Description

The PAL Series 20AP represents an enhancement of existing PAL architectures which provides greater design flexibility and improved testability. Several new features have been incorporated into the family, including programmable output polarity, power-up reset, and register preload.

The programmable output polarity feature allows the user to program individual outputs either active high or active low. This feature eliminates any possible need for inversion of signals outside the device.

The registered members of the Series 20AP have been designed to reset during system power-up. Upon application of power, all registers are initialized to a logic 0 state, setting all outputs to a logic 1.

The testability of the registered devices has been increased through the use of the preload feature. During testing, registers can be loaded with any arbitrary state value, thereby allowing full logical verification.

General Description

The PAL Series utilitizes Monolithic Memories advanced self-aligned washed-emitter high-speed bipolar process and the bipolar PROM fusible-link technology to provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from the PC board and are placed on silicon where they can be easily modified during prototype check-out or production.

PART NUMBER	PKG	GATE ARRAY DESCRIPTION
PAL16P8A	N,J,F,L	Octal 16 input And-Or
PAL16RP8A	N,J,F,L	Octal 16 input Registered And-Or
PAL16RP6A	N,J,F,L	Hex 16 input registered And-Or
PAL16RP4A	N,J,F,L	Quad 16 input registered And-Or

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition the PAL provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D-type flip-flops which are loaded on the low-to-high transition of the clock. The registers power up with high (V_{OH}) at the output pin, regardless of the polarity fuse. PAL Logic Diagrams are shown with all fuses blown, enabling the designer to use the diagrams as coding sheets.

The entire PAL family is programmed on inexpensive conventional PAL/PROM programmers with appropriate personality and socket adapter modules. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

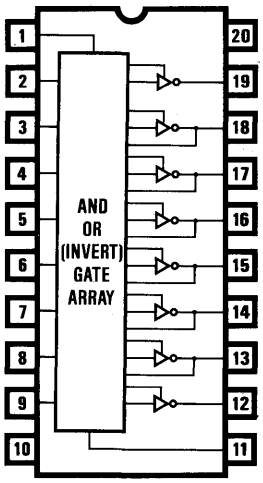
Ordering Information

PAL 16 RP 8 A C J 883B

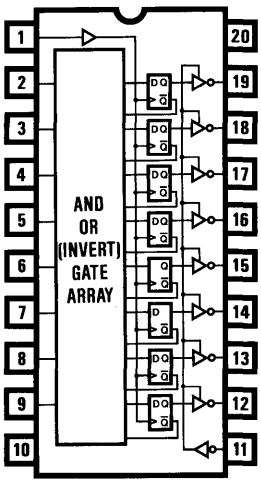
- **PAL** — PROGRAMMABLE ARRAY LOGIC FAMILY
- **16** — NUMBER OF ARRAY INPUTS
- **RP** — OUTPUT TYPE
  - R = Registered
  - P = Programmable output polarity
- **8** — NUMBER OF OUTPUTS
- **A** — SPEED/POWER
  - A = High speed
- **C** — TEMPERATURE RANGE
  - C = 0°C to +75°C
  - M = -55°C to +125°C (case temperature)
- **J** — PACKAGE
  - N = Plastic dip
  - J = Ceramic dip
  - F = Flat pack
  - L = Leadless chip carrier
- **883B** — OPTIONAL HI-REL PROCESSING
  - 883B = Mil-Std-883 Method 5004 and 5005 Level B
  - 883C = Mil-Std-883 Method 5004 and 5005 Level C
  - B = Mil-Std-883 Method 5004 equivalent

2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

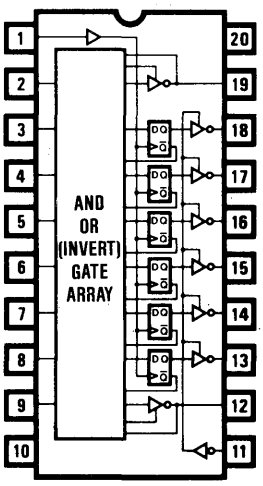
PAL16P8A



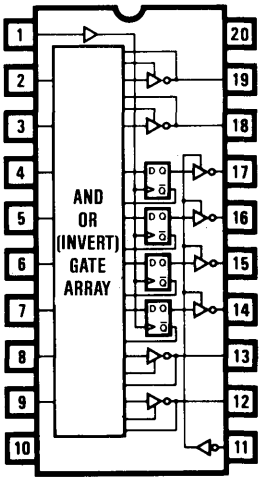
PAL16RP8A



PAL16RP6A



PAL16RP4A



Operating Conditions

SYMBOL	PARAMETER			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
t_w	Width of Clock	Low		25	14		20	14		ns
		High		15	6		10	6		
t_{su}	Set up time from input or feedback to clock	16RP8A 16RP6A 16RP4A	Polarity fuse intact	30	15		25†	15		ns
			Polarity fuse blown	35	20		30	20		
t_h	Hold time			0	−10		0	−10		ns
T_A	Operating free-air temperature			−55			0		75	°C
T_C	Operating case temperature					125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}	Low-level input current††	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}	High-level input current††	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL I_{OL} = 12 mA		0.3	0.5	V
			COM I_{OL} = 24 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = −2 mA	2.4	2.8		V
			COM I_{OH} = −3.2 mA				
I_{OZL}	Off-state output current††	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}			V_O = 2.4 V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5 V	V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

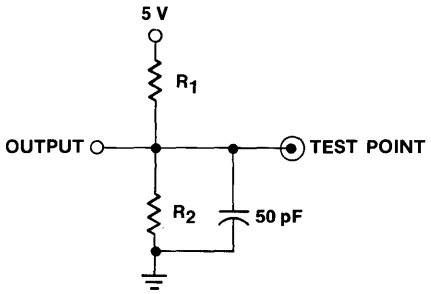
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	16RP8A, 16RP6A, 16RP4A Input or feedback to output	Polarity fuse intact	R_1 = 200 Ω, R_2 = 390 Ω		15	30		15	25	ns
		Polarity fuse blown			20	35		20	30	
t_{CLK}	Clock to output or feedback				10	20		10	15	ns
t_{PZX}	Pin 11 to output enable except 16P8A				10	25		10	20	ns
t_{PXZ}	Pin 11 to output disable except 16P8A				11	25		11	20	ns
t_{PZX}	Input to output enable	16RP6A, 16RP4A, and 16RP8A			10	30		10	25	ns
t_{PZX}	Input to output disable	16RP6A, 16RP4A, and 16RP8A			13	30		13	25	ns
f_{MAX}	16RP8A, 16RP6A, 16RP4A Maximum frequency	Polarity fuse intact		20	40		28.5	40		MHz
		Polarity fuse blown		18.5	33		25	33		

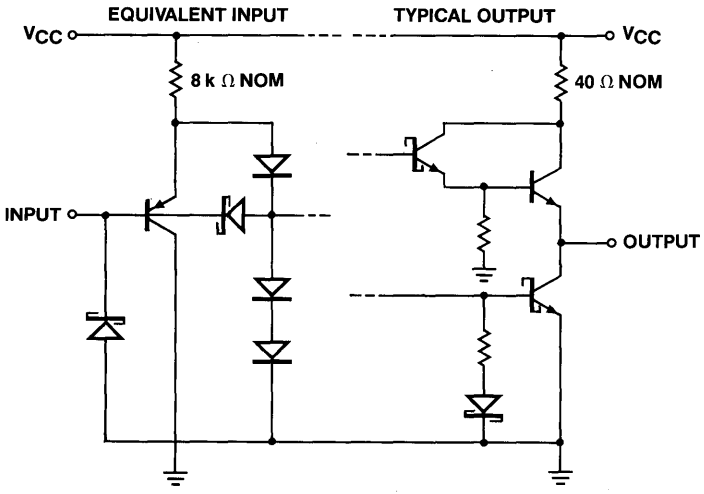
Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 to 7.0 V	-0.5 to 12.0 V
Input voltage	-1.5 to 5.5 V	-1.0 to 22 V
Off-state output voltage	5.5 V	12.0 V
Storage temperature	-65 to +150° C	

Test Load



Schematic of Inputs and Outputs



Typical notes for all the previous specifications

NOTES: Apply to electrical and switching characteristics

† Can select 20 ns upon customer request.

††I/O pin leakage is the worst case of I_{OZX} or I_{IX}, i.e. I_{IL} and I_{OZH}.

* These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

* * Only one output shorted at a time.

Output Register PRELOAD

The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing which would otherwise require a state sequencer for test coverage. The procedure for PRELOAD is as follows:

1 Raise V_{CC} to 4.5 V.

2 Disable output registers by setting pin 11 to V_{IH}.

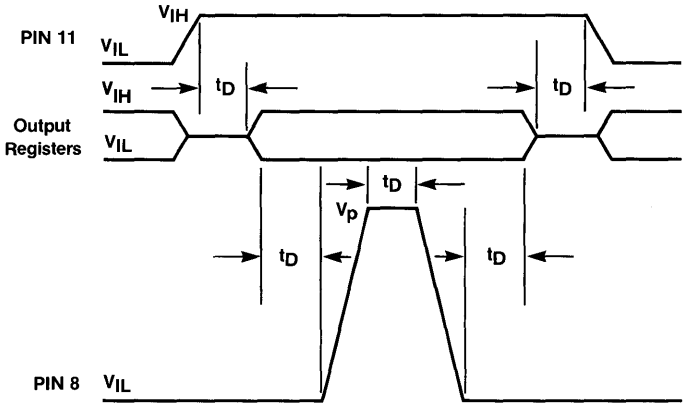
3 Apply V_{IL}/V_{IH} to all output registers.

4 Pulse pin 8 to V_p. Then back to 0 V.

5 Remove V_{IL}/V_{IH} from all output registers.

6 Lower pin 11 to V_{IL} to enable the output registers.

7 Verify for V_{OL}/V_{OH} at all output registers.



PAL Legend

Constants

LOW (L)	NEGATIVE (N)	ZERO (0)	GND	FALSE	×	FUSE NOT BLOWN
HIGH (H)	POSITIVE (P)	ONE (1)	V_{CC}	TRUE	–	FUSE BLOWN

Operators (IN HIERARCHY OF EVALUATION)

```
;   COMMENT FOLLOWS
/   COMPLEMENT, PREFIX TO A PIN NAME
*   AND (PRODUCT)
+   OR (SUM)
:+: XOR (EXCLUSIVE OR)
:*: XNOR (EXCLUSIVE NOR)
( ) CONDITIONAL THREE-STATE (IF STATEMENT) OR FIXED SYMBOL
=   EQUALITY
:=  REPLACED BY AFTER THE LOW TO HIGH TRANSITION OF THE CLOCK
```

Equations

Standard $O'_1 = I_1 \overline{I_2} + \overline{I_1} I_2$

PALASM `O1 = I1*/I2 + /I1*I2`

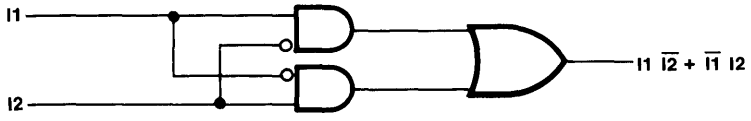
Function Table States

```
H = HIGH LEVEL                C = TRANSITION FROM LOW TO HIGH
L = LOW LEVEL                 Z = OFF (HIGH IMPEDANCE)
X = IRRELEVANT
```

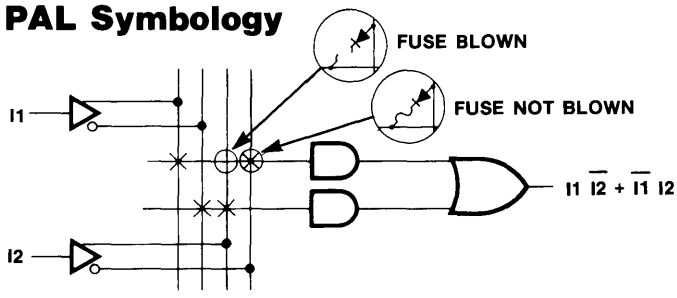
Test Conditions

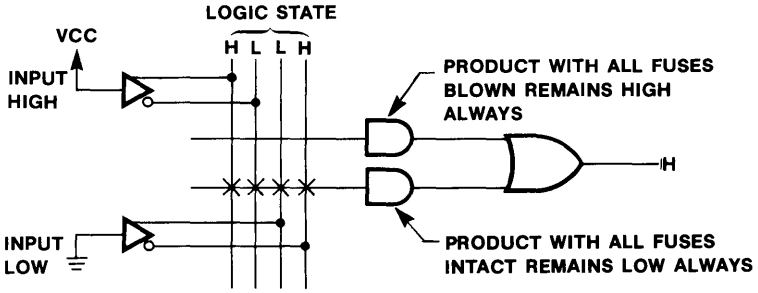
```
H = TEST HIGH     1 = DRIVE HIGH     C = DRIVE INPUT FROM LOW TO HIGH
L = TEST LOW      0 = DRIVE LOW      Z = TEST FOR HIGH IMPEDANCE
X = IRRELEVANT
```

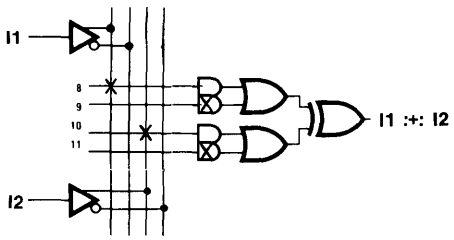
Conventional Symbology

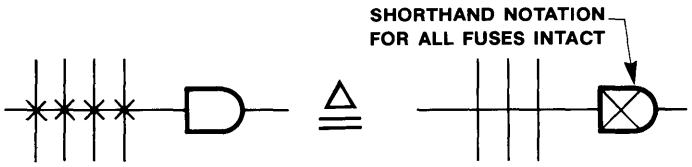


PAL Symbology

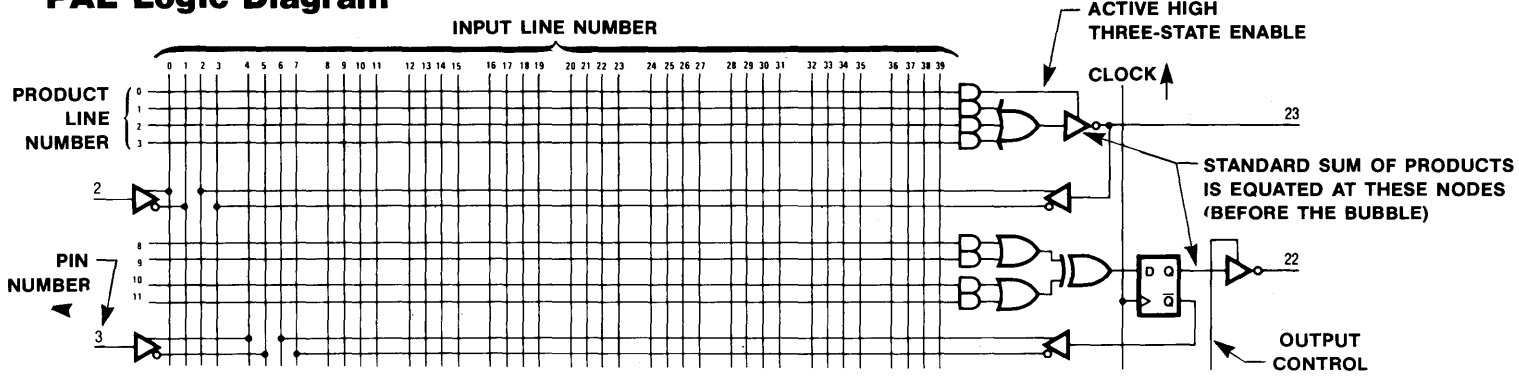






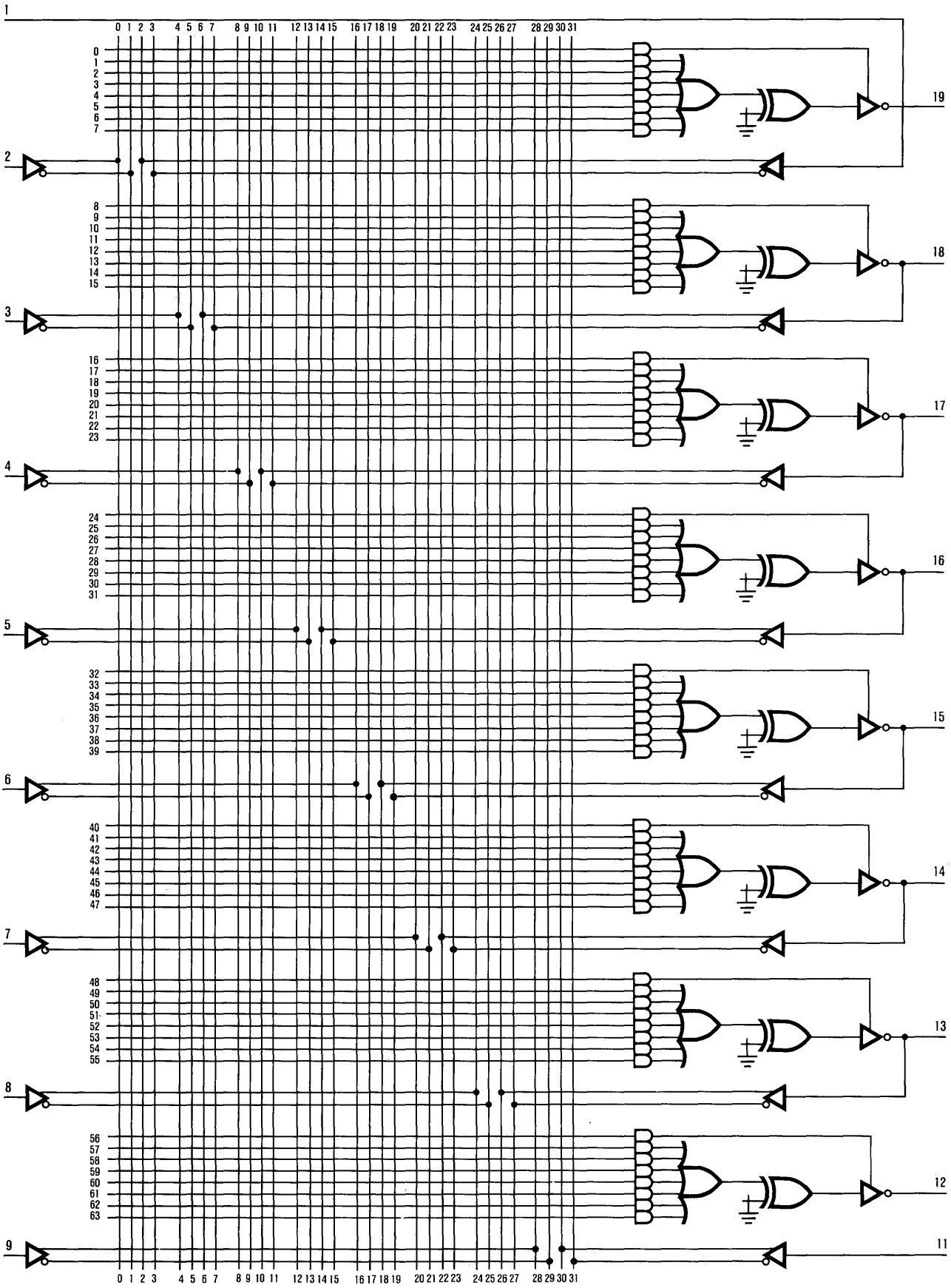


PAL Logic Diagram



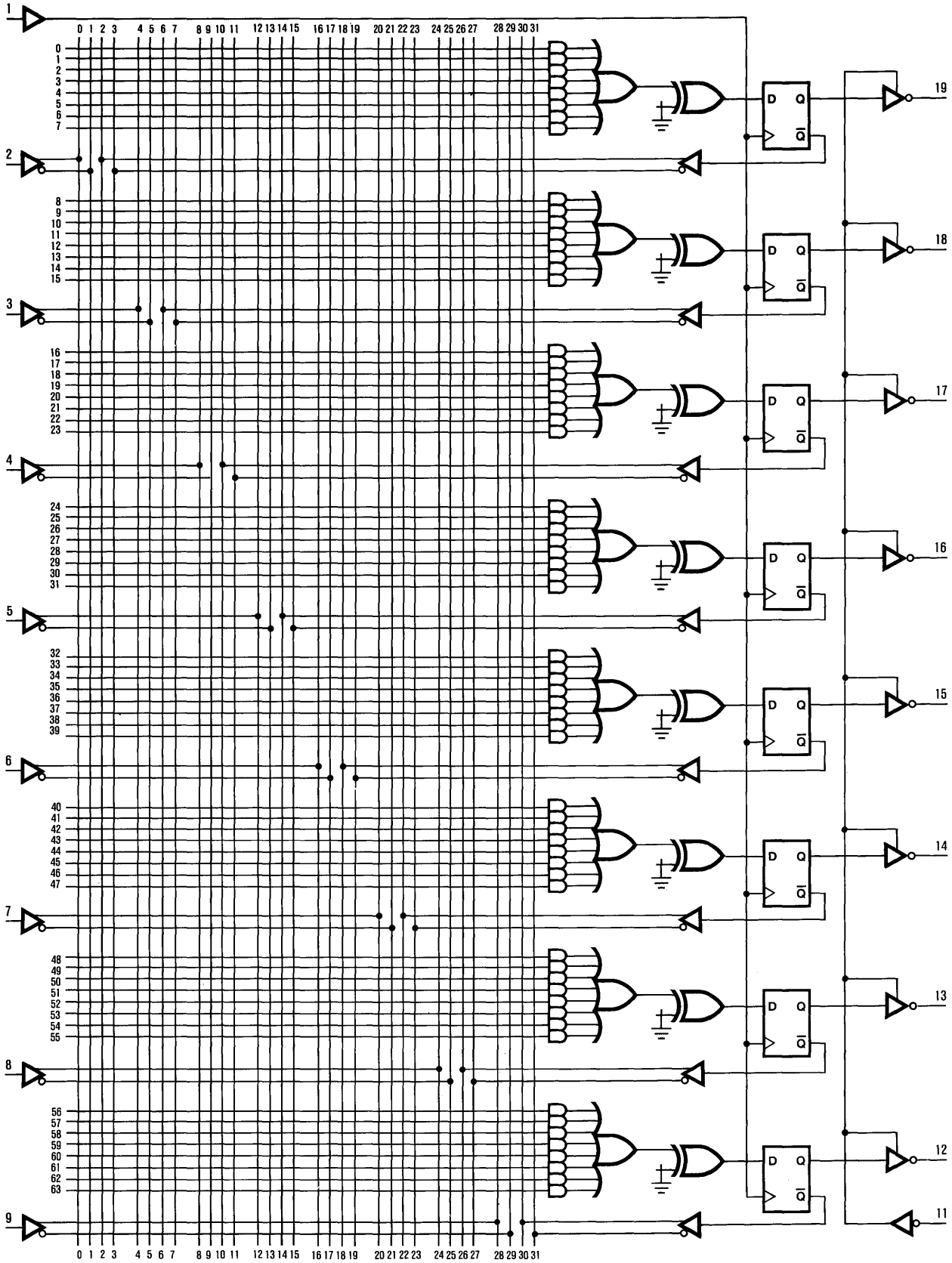
Logic Diagram

16P8A



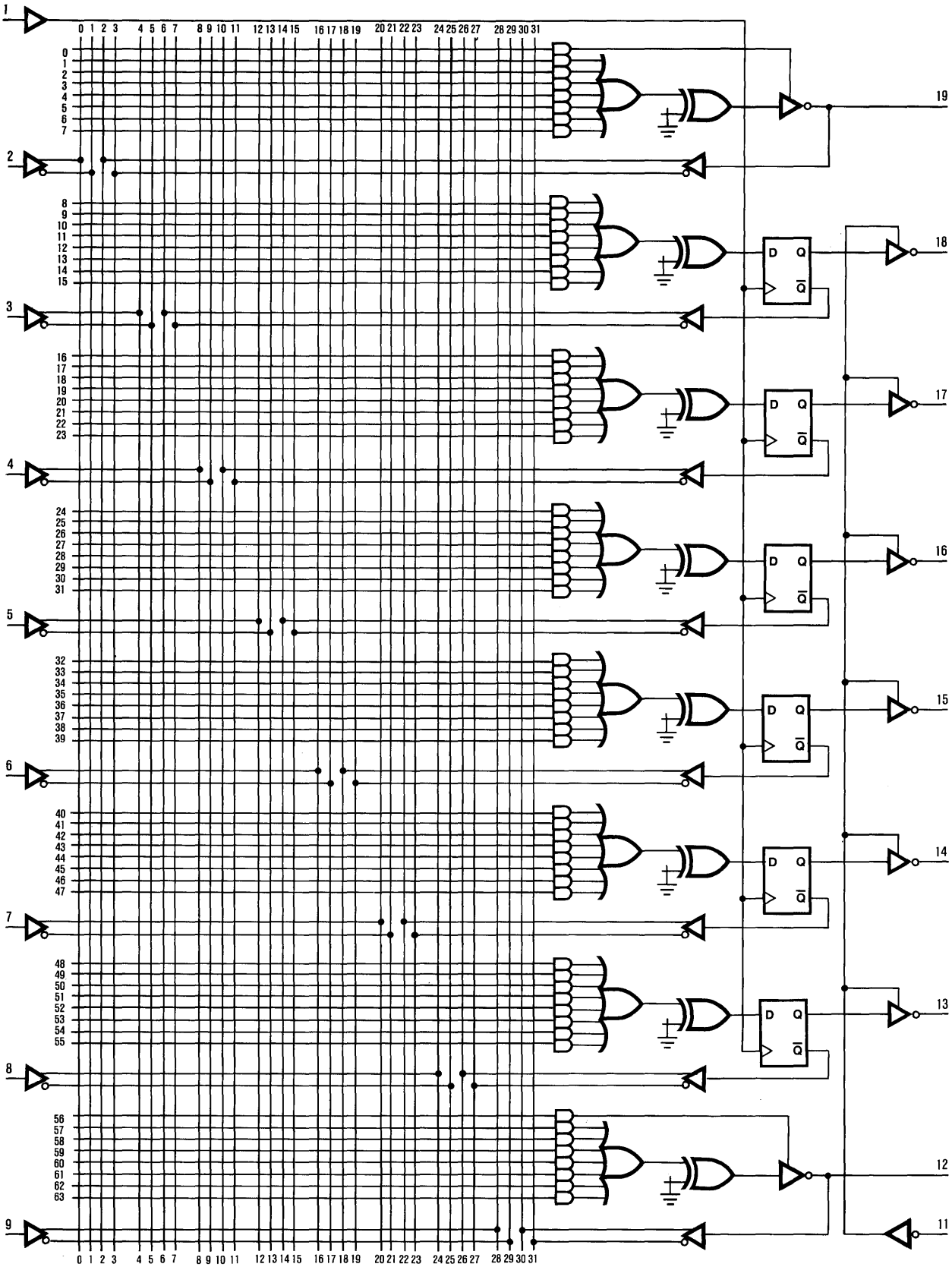
Logic Diagram

16RP8A



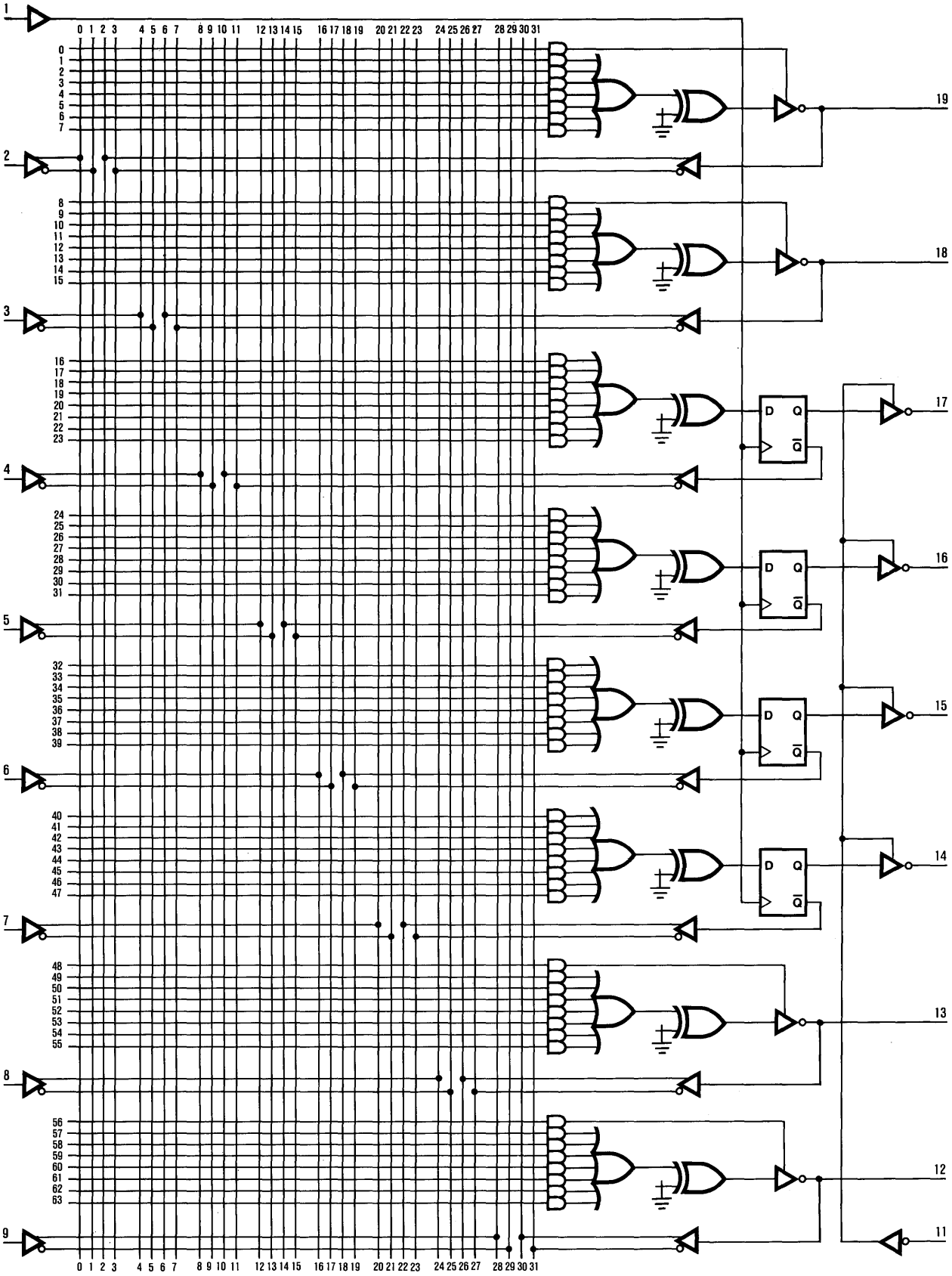
Logic Diagram

16RP6A



Logic Diagram

16RP4A



Programming/Verifying Procedure

NOTES: For programming purposes many PAL pins have double functions.

As long as Pin 1 is at V_{IHH}, Pin 11 is at ground, and Pin 12 is either at V_{IH} or Z (as defined in Table 1) — Pins 16, 17, 18 and 19 are outputs. The other pin functions are: I0 (Pin 2) through I7 (Pin 9) plus Pin 12 address the proper row; A0 (Pin 15), A1 (Pin 14), and A2 (Pin 13) address the proper product lines.

When Pin 11 is at V_{IH}, Pin 1 is at ground and Pin 19 is either at V_{IH} or Z — Pins 12, 13, 14, and 15 are outputs. The other pin functions are: I0 (Pin 2) through I7 (Pin 9) plus Pin 19 address the proper row; A0 (now Pin 18), A1 (now Pin 17), and A2 (now Pin 16) address the proper product lines.

5.1 Pre-verification

5.1.1. Pre-verification-Security-Fuses

5.1.1.1 Raise Pin 2 to VP

5.1.1.2 Place a 2k resistor to ground on Pin 1 and measure voltage across it.
— Reject part if measured voltage is less than 1.5 V

5.1.1.3 Place a 2k resistor to ground on Pin 11 and measure voltage across it.
— Reject part if measured voltage is less than 1.5 V

5.1.2 Pre-verification — Array

5.1.2.1 Raise V_{CC} to 5.0 V

5.1.2.2 Raise output disable, OD, to VIHH.

5.1.2.3 Select an input line by specifying inputs and L/R as shown in Table 1.

5.1.2.4 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table 2.

5.1.2.5 Pulse the CLOCK pin and verify (with CLOCK at VIL) that the output pin, O is TTL high.
— For TTL high, continue procedure
— For TTL low, stop procedure and reject part.

5.1.3 Pre-verification — Programmable Polarity Fuses (METHOD 1)

5.1.3.1 Raise V_{CC} to 5.0 V

5.1.3.2 Raise Pin 3 to VP.

5.1.3.3 Raise Pin 4 to VP.

5.1.3.4 Pulse the CLOCK pin and test (with CLOCK at VIL) the state of the output pin, O.
— For unblown polarity fuse the output will be at logic 0.
— For blown polarity fuse the output will be at logic 1.

5.1.4 Pre-verification — Programmable Polarity Fuses (METHOD 2)

5.1.4.1 Raise Vcc to 5.0 V

5.1.4.2 For any input condition determine the state of each output.

5.1.4.3 Raise Pin 7 to VP.

5.1.4.4 Compare the output states now with their states at 5.1.4.2.
— If the state of the output has changed, then the output polarity fuse is unblown.
— If the state of the output is unchanged, then the output polarity fuse is blown.

5.1.5 Pre-verification — Programmable Polarity Fuses (METHOD 3)

5.1.5.1 Raise V_{CC} to 5.0 V

5.1.5.2 Raise all inputs to VIHH.

5.1.5.3 Raise Pin 11 to VIHH.

5.1.5.4 Pulse the CLOCK pin and verify (with CLOCK at VIL) the state of the output pin.
— If output is at logic 0, then the output polarity fuse is unblown.
— If output is at logic 1, then the output polarity fuse is blown.

Programming Algorithm

5.2.1 Raise Output Disable pin, OD, to VIHH

5.2.2 Programming pass. For all fuses to be blown:

5.2.2.1 Lower CLOCK pin to ground.

5.2.2.2 Select an input line by specifying inputs and L/R as shown in Table 1

5.2.2.3 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table 2.

5.2.2.4 Raise V_{CC} to VIHH.

5.2.2.5 Program the fuse by pulsing the output pins of the selected product group one at a time to VIHH.

5.2.2.6 Lower V_{CC} to 5.0 V

5.2.2.7 Repeat this procedure from 5.2.2.2 until pattern is complete.

5.2.3 First verification pass. For all fuse locations:

5.2.3.1 Select an input line by specifying inputs and L/R as shown in Table 1.

5.2.3.2 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table 2.

5.2.3.3 Pulse the CLOCK pin and verify (with CLOCK at VIL) that the output pin, O is in the correct state.
— For verify output state, continue procedure
— For overblow condition, stop procedure and reject part.
— For underblow condition, reexecute steps 5.2.2.4 through 5.2.2.6 and 5.2.2.3. If successful, continue procedure. After three attempts to blow fuse without success, reject part.

5.2.3.4 Repeat this procedure from 5.2.3.1 until the entire array is exercised.

5.2.4 High Voltage Verify. For all fuse locations:

5.2.4.1 Raise V_{CC} to 5.5 V

5.2.4.2 Select an input line by specifying inputs and L/R as shown in Table 1.

5.2.4.3 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table 2.

5.2.4.4 Pulse the CLOCK pin and verify (with CLOCK at VIL) that the output pin, O is in the correct state.
— For verified output state, continue procedure
— For invalid output state, stop procedure and reject part.

5.2.4.5 Repeat this procedure from 5.2.4.2 until the entire array is exercised.

5.2.5 Low Voltage Verify. For all fuse locations:

5.2.5.1 Lower V_{CC} to 4.5 V

5.2.5.2 Select an input line by specifying inputs and L/R as shown in Table 1

5.2.5.3 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table 2.

5.2.5.4 Pulse the CLOCK pin and verify (with CLOCK at VIL) that the output pin, O, is in the correct state.
— For verified output state, continue procedure.
— For invalid output state, continue procedure and reject part.

5.2.5.5 Repeat this procedure from 5.2.5.2 until entire array is exercised.

Programming the Security Fuses

5.3.1 Verify per Section 5.2.4 and 5.2.5.

5.3.2 Raise V_{CC} to 5.5

5.3.3 — Program the first fuse by pulsing Pin 1 to VP. (From 1 to 5 pulses are acceptable.)
— Program the second fuse by pulsing Pin 11 to VP. (From 1 to 5 pulses are acceptable.)

5.3.4 Verify per Section 5.1.
— A device is "secured" if it verifies as blank per section 5.1.

Programming the Output Polarity Fuses.

5.4.1 Initial Programming Pass.

5.4.1.1 Raise V_{CC} to 5.5 V.

5.4.1.2 Set all inputs and output pins to Z

5.4.1.3 Raise output disable, OD, to V_{IHH} to disable the selected outputs.

5.4.1.4 Raise Polarity Enable, POLE to VP.

5.4.1.5 Program the fuse by pulsing the desired output to VIHH.

5.4.1.6 Lower POLE to VIH

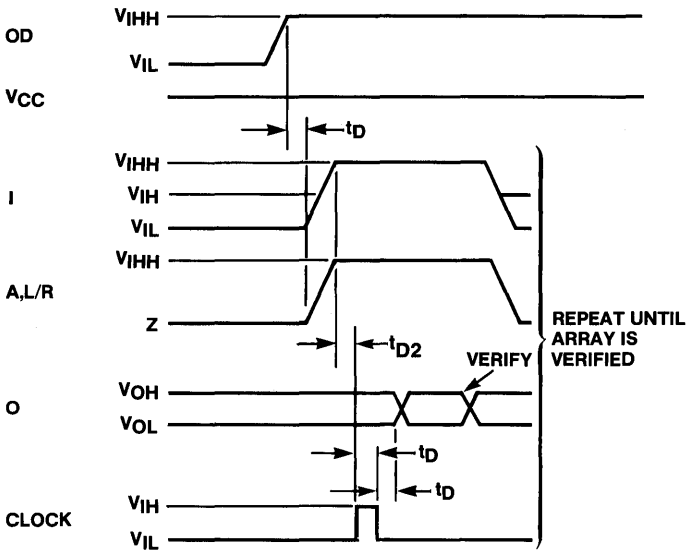
5.4.1.7 Lower OD to VIL.

5.4.1.8 Repeat this procedure from 5.4.1.3 to 5.4.1.7 until all desired outputs are programmed.

Programming Parameters

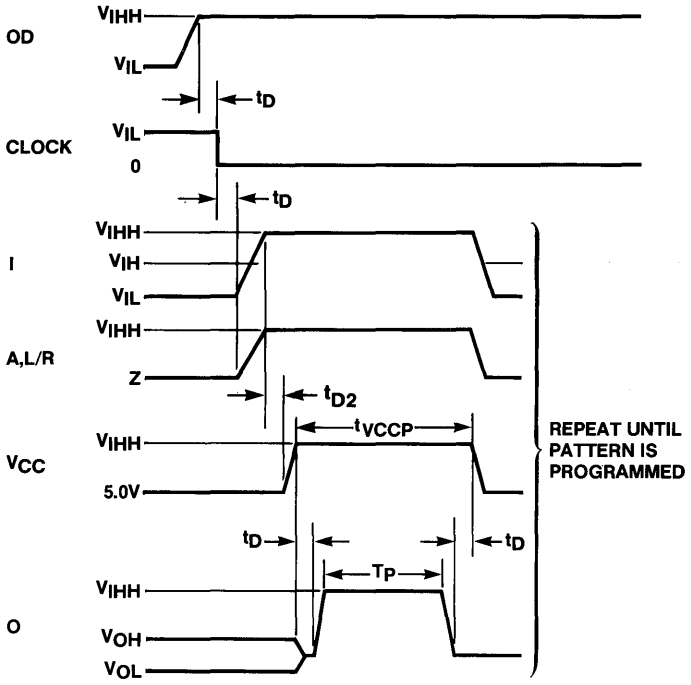
SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNIT
V_{IHH}	Program-level input voltage		11.5	11.75	12	V
I_{IHH}	Program-level input current	Output Program Pulse			50	mA
		OD, L/R			50	
		All other inputs			15	
I_{CCH}	Program Supply Current				900	mA
t_{VCCP}	Pulse Width of V_{CC} @ V_{IHH}				60	μS
T_P	Program Pulse Width		10	20	50	μS
t_D	Delay Time		100			ns
t_{D2}	Delay Time after L/R Pin		10			μS
	V_{CCP} Duty Cycle				20	%
V_P	Output Polarity and Security Fuse Programming Voltage		19.5	20	20.5	V
I_{P1}	Security Fuse Programming Supply Current				400	mA
I_{P2}	Output Polarity Programming Supply Current				200	mA
T_{PP}	Output Polarity and Security Fuse Programming Pulse Width		10	40	70	μS
	Output Polarity and Security Fuse Programming Duty Cycle				50	%
t_{RP}	Rise time of output programming and address pulses		1	1.5	10	V/μS
t_{RP}	Rise Time of security fuse programming pulses		1	1.5	10	V/μS
V_{CCOP}	V_{CC} value during output polarity programming		5.25	5.5	5.25	V
V_{CCPP}	V_{CC} value during security fuse programming		5.25	5.5	5.75	V
	V_{CC} value for first verify		4.75	5.0	5.25	
	V_{CC} value for High V_{CC} verify		5.4	5.5	5.6	
	V_{CC} value for Low V_{CC} verify		4.4	4.5	4.6	

Array Verify

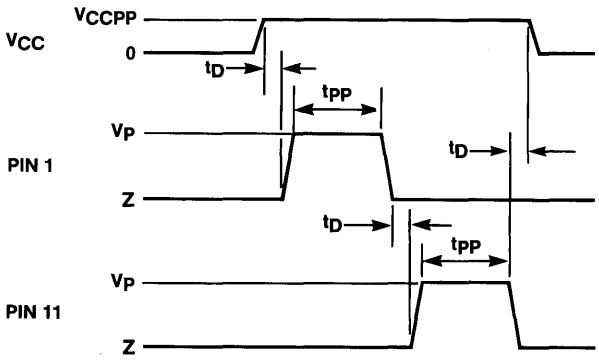


V_{CC} (Low Voltage Verify) = 4.5 volts
V_{CC} (High Volatge Verify) = 5.5 volts
V_{CC} (First Verify) = 5.0 volts
A Delay (t_{D2}) must always precede the Positive Clock Transition. (e.g. see section 5.2.3.3 for underblow condition)

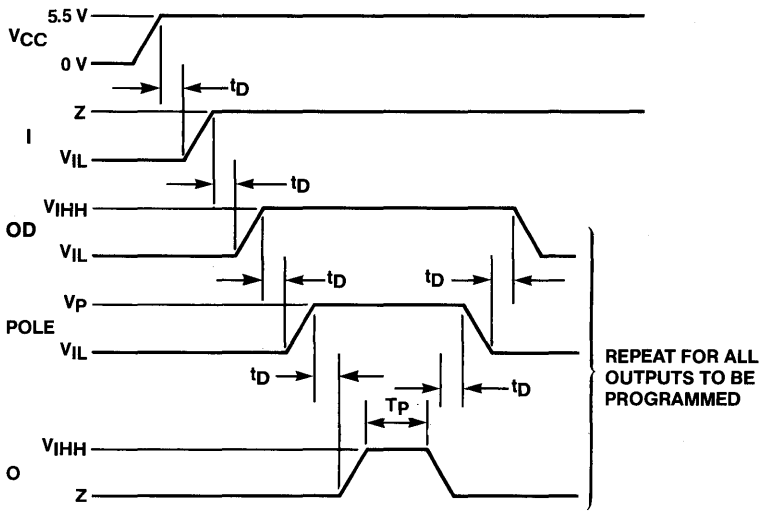
Array Programming



Security Fuse Programming



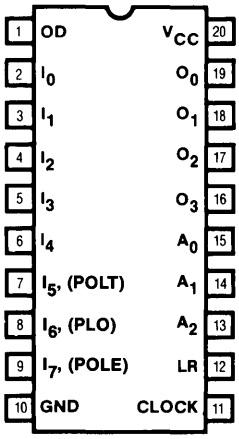
Output Polarity Programming



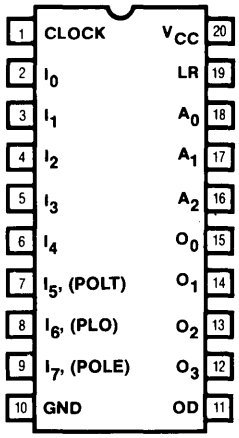
Programming Pin Configurations

POLT = Polarity Test
PLO = Register Preload
POLE = Polarity Programming Enable

PRODUCTS 0 THRU 31



PRODUCTS 32 THRU 63



Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
Z = High impedance (e.g., 10kΩ to 5.0V)

INPUT LINE NUMBER	PIN IDENTIFICATION								
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

Table 1 Input Line Select

PRODUCT LINE NUMBER	PIN IDENTIFICATION						
	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

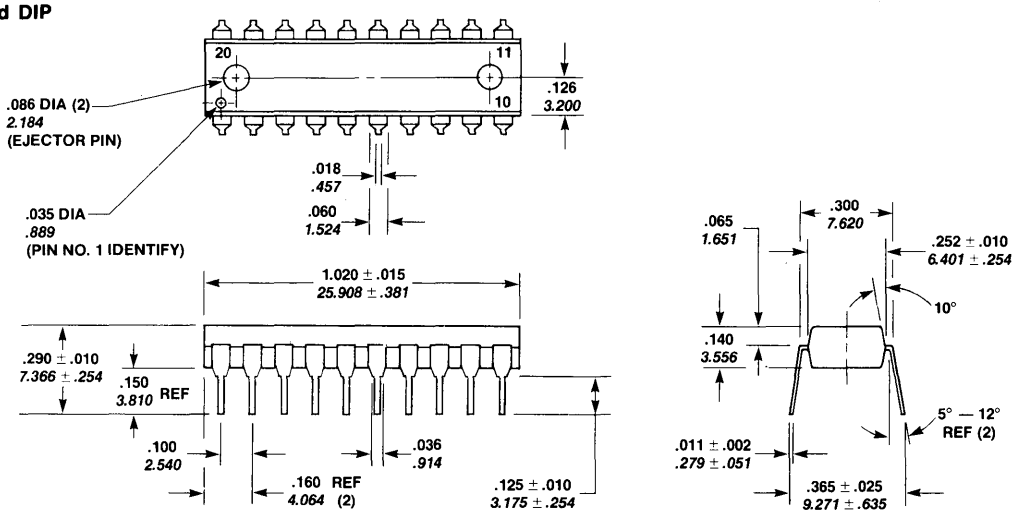
Table 2 Product Line Select

Programmer/Development System

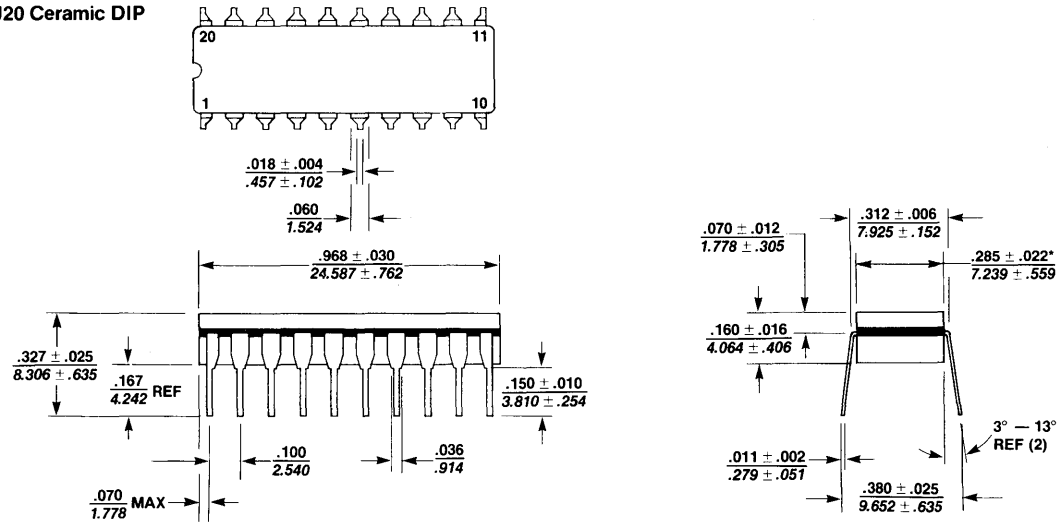
VENDOR	PAL20AP	PAL20	PAL24 (STD)	PAL24 (FAST)
Data I/O	- Logic PAK	- Logic PAK	- Logic PAK	- Logic PAK
Structured Design	- SD 1000	- SD 20/24 - SD 1000	- SD 20/24 - SD 1000	- SD 20/24 - SD 1000
Stag	- ZL 30	- PM 202 (rev 3) - Stag ZL 30	- PM 202 (rev 3) - Stag ZL 30	- PM 202 (rev 3) - Stag ZL 30
Digelec		- UP 803 (FAM 51) or (FAM 52)	- UP 803 (FAM 51) or (FAM 52)	- UP 803 (FAM 51) or (FAM 52)
Kontron		- MPP 80S MOD 21	- MPP 80S MOD 21	
Varix		- Omni programmer	- Omni programmer	

Package Drawings

N20 Molded DIP



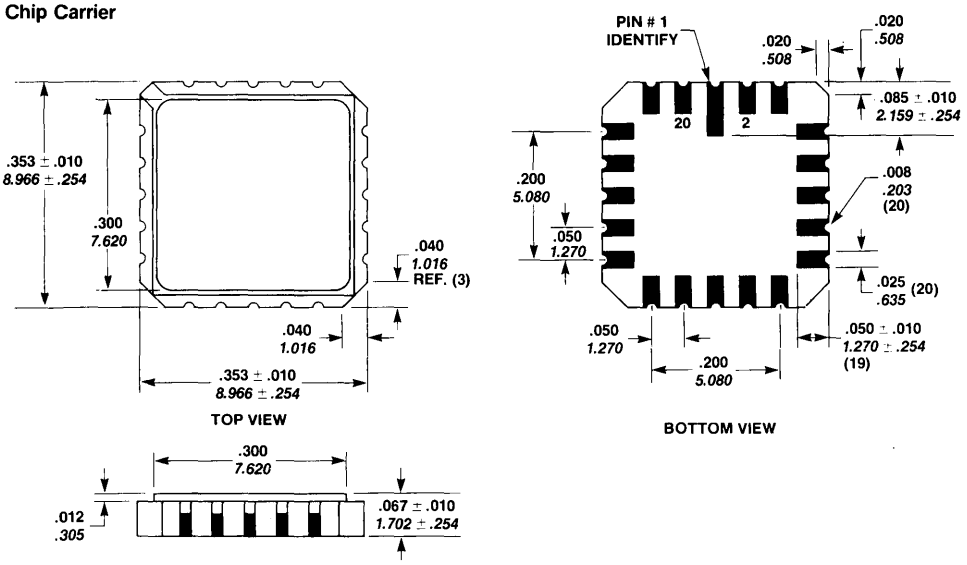
J20 Ceramic DIP



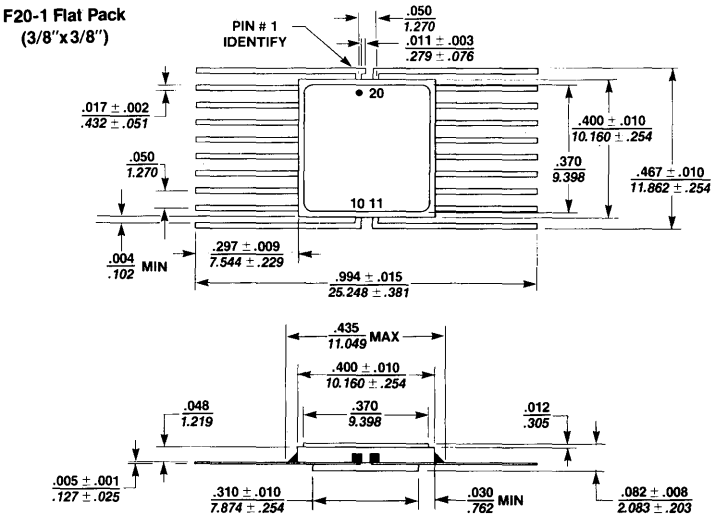
Package Drawings

UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS

L20 Leadless Chip Carrier



F20-1 Flat Pack
(3/8"x3/8")



Monolithic MMI Memories

Americas
Monolithic Memories
2175 Mission College Blvd.
Santa Clara, CA 95050
Phone (408) 970-9700
Telex (910) 338-2374
Telex (910) 338-2376
Fax (408) 980-0675

France
Monolithic Memories France S.A.R.L.
Silic 463
F 94613 Rungis Cedex
France
Phone 1-6874500
Telex 202146
Fax 1-6876825

Japan
Monolithic Memories Japan KK
5-17-9 Shinjuku
Shinjuku
Tokyo 160
Japan
Phone 3-207-3131
Telex 232-3390 MMIKKJ
Fax 3-207-3139

United Kingdom
Monolithic Memories, Ltd.
Lynwood House
1 Camp Road
Farnborough, Hampshire
England GU146EN
Phone 9-011-44-252-517431
Telex 858051 MONO UKG
Fax (0252) 43724

Germany
Monolithic Memories, GmbH
Mauerkircherstr 4
D 8000 Munich 80
West Germany
Phone 89-984961
Telex 524385
Fax 89-983162

Monolithic Memories reserves the right to make changes in order to improve circuitry and supply the best product possible.

Monolithic Memories cannot assume responsibility for the use of any circuitry described other than circuitry entirely embodied in their product. No other circuit patent licenses are implied.

Printed in U.S.A.