AN-513
Application Note

A HIGH GAIN INTEGRATED CIRCUIT RF-IF AMPLIFIER WITH WIDE RANGE AGC

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This note describes the operation and application of the MC1590G, a monolithic RF-IF amplifier. Included are several applications for IF amplifiers, a mixer, video amplifiers, single and two-stage RF amplifiers.

MOTOROLA Semiconductor Products Inc.

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INTRODUCTION

The MC1590G is a direct coupled, high gain, monolithic amplifier intended primarily for use in IF amplifiers with operating frequencies up to 150 MHz. The MC1590G comes in a TO-99, 8 pin, metal package and is characterized for the full -55°C to +125°C temperature range. In addition to the extremely high gain capability, the MC1590 incorporates a highly efficient automatic gain control feature. Besides IF amplifier applications, the MC1590G also serves well as an oscillator and as a mixer over the same IF frequency range. The high gain, wide bandwidth, and AGC capability also make this circuit attractive for use in video amplifier applications. This application note will describe the operation and pertinent device characteristics of the MC1590G. Also included are several applications including IF amplifiers, a mixer, and a video amplifier.

OPERATION

The circuit, shown schematically in Figure 1, consists of a common-emitter differential amplifier input stage (Q1, 2) which drives a pair of common-base differential amplifiers (Q3, 4 and Q5, 6). The output of the common-base stage is fed into a common-collector (Q7, 10), common-emitter (Q8, 9) cascaded, differential pair. The unnumbered transistors shown on the schematic are for dc biasing.

A simplified schematic of the transistor configuration for the signal path is shown in Figure 2. The cascode arrangement of the first two stages provides good gain. The common emitter output stage yields high power gain when the

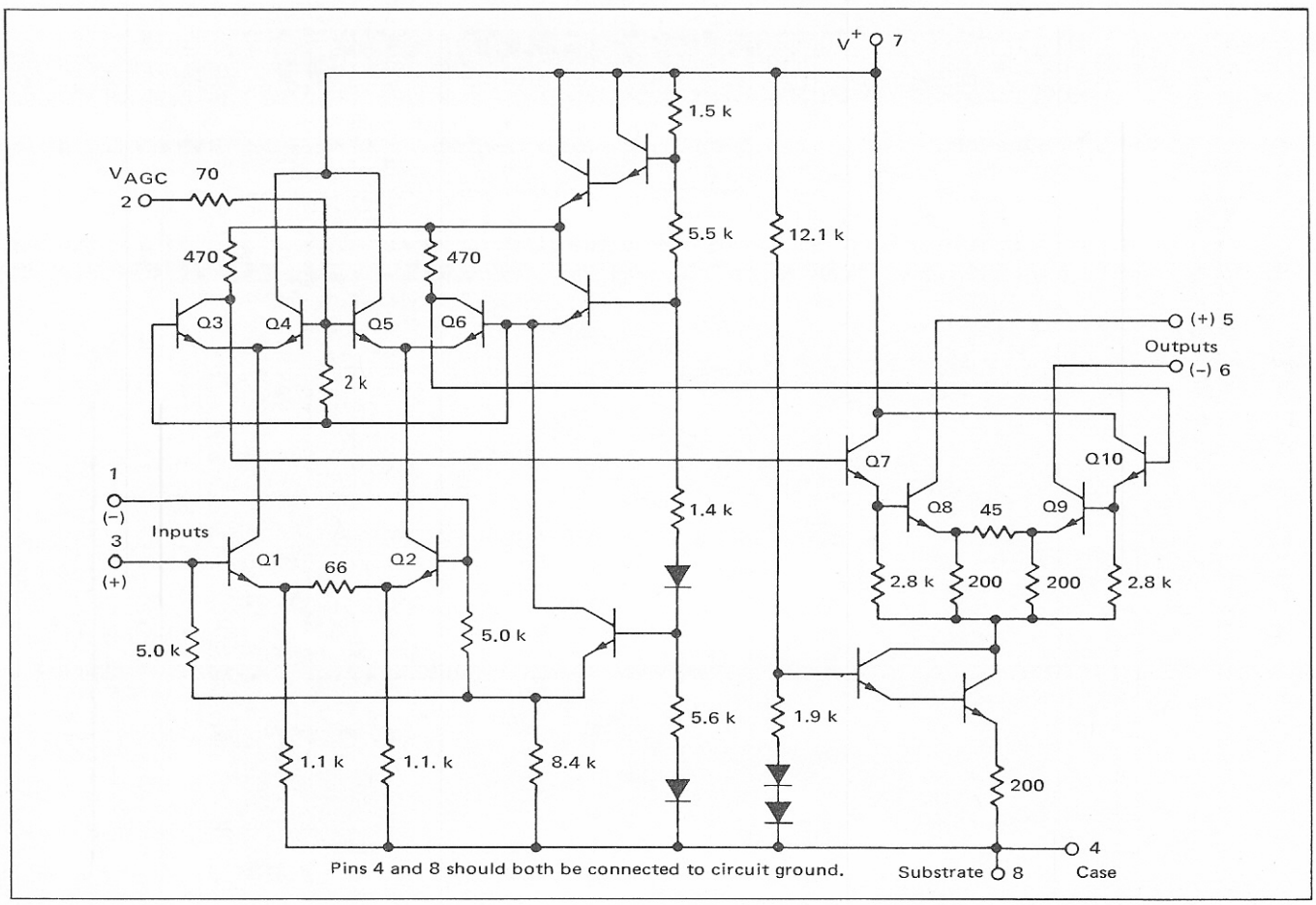


FIGURE 1 – MC1590G Circuit Schematic

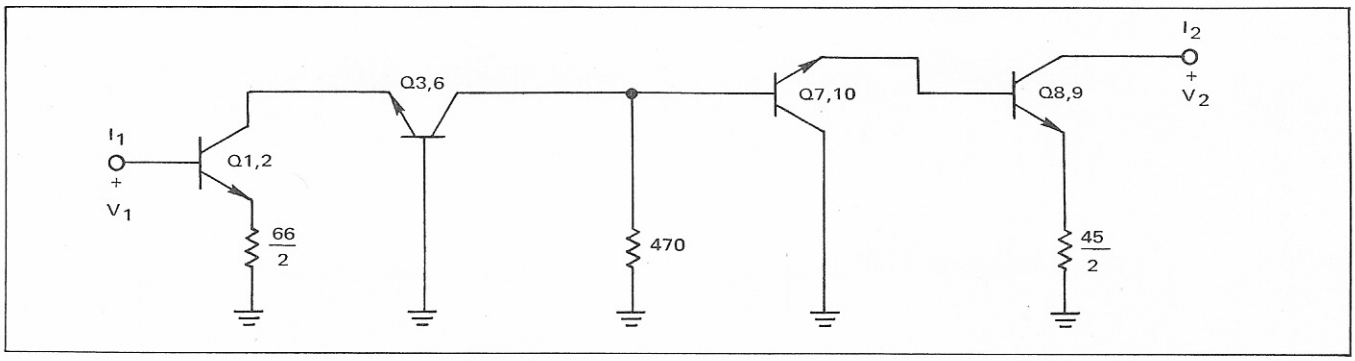


FIGURE 2 – Signal Path for 1/2 MC1590G

proper collector impedance is provided. The emitter followers, Q7, 10, separating the input and output stages, improve the amplifier's bandwidth. The reason for this is that when the gain of the output stage is high, the Miller capacitance reflected into the bases of the output transistors, Q8, 9 is also high. If the emitter followers were absent, this capacitance would shunt the 470 Ω load impedances of the previous stage thereby severely limiting broadband performance. A detailed derivation of the y-parameters, based on the model of Figure 2, is given in the literature along with other considerations involved in integrated circuit design of the MC1590G.

In the typical amplifier configuration, the input signal is applied between pins 1 and 3 (Figure 1) in either a single-ended or a differentially coupled mode. In the single-ended mode the signal is applied to either pin 1 or pin 3, while the unused pin is ac coupled to ground. It is important to note that connections made at the signal input pins should not be dc coupled to ground. Care should also be taken in direct coupling the input to the driving source to prevent upsetting the dc bias condition established on the bases of the input transistors. Output coupling can also be in either the single-ended or the differential-coupled mode. Two distinct improvements result when differential coupling is used: (1) amplifier power gain is increased by 6 dB over the single-ended case and (2) the available level of output signal swing, before clipping occurs, is also doubled.

Automatic gain control of the amplifier is accomplished by an increase in the dc voltage on pin 2 above a nominal voltage of 5 Vdc (assuming +12 Vdc power supply). As the voltage on pin 2 is raised above 5 Vdc, transistors Q4 and Q5 which are normally off, begin to turn on. With transistors Q4 and Q5 on, a portion of the signal current is diverted from Q3 and Q6 and the output signal is reduced accordingly. This method of gain control offers important advantages over other methods of AGC. For example, the fixed gain input and output stages of the amplifier eliminate input and output admittance variations that accompany conventional AGC techniques. This helps alleviate detuning, bandwidth variations, and changes in signal handling capability during AGC. Another advantage is that the common-mode nature of the AGC signal permits dc variations produced by the AGC signal to be cancelled by the output differential amplifier. This absence of dc offset with AGC voltage applied permits the addition of a direct coupled stage at the output. Two bias bleeders have been included in the circuit to prevent signal feedthrough in the bias circuitry under high levels of gain reduction.

Y PARAMETERS

Admittance parameter versus frequency data for the MC1590G is shown in Figures 3 to 6. All admittance measurements excepting Y_{12} were made on a General Radio Transfer Function and Immittance Bridge and are for a single-ended input and output. Output admittance for the differential output configuration is one-half that of the single ended output admittance while the input admittance is approximately the same for both single-ended and differentially-coupled inputs. Due to the extremely small value of reverse transfer admittance, a special test circuit was required to measure its value. This admittance is primarily due to package parasitics and may vary depending upon the method of component mounting. In a practical circuit, stray capacitance or unwanted inductive coupling between input and output coils will probably be the major contribution to the total reverse transfer admittance. The value for Y_{12} plotted in Figure 6 reflects the reverse transfer admittance of the device plus that of the test circuit used in the measurement and represents a total feedback capacitance of 0.025 pF. This value of feedback capacitance is

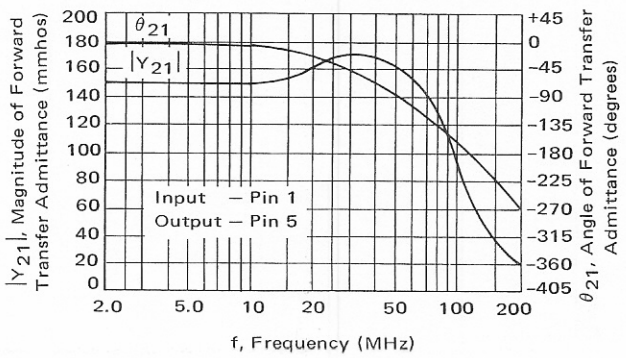


FIGURE 3 – Y_{21}, Forward Transfer Admittance, Polar Form

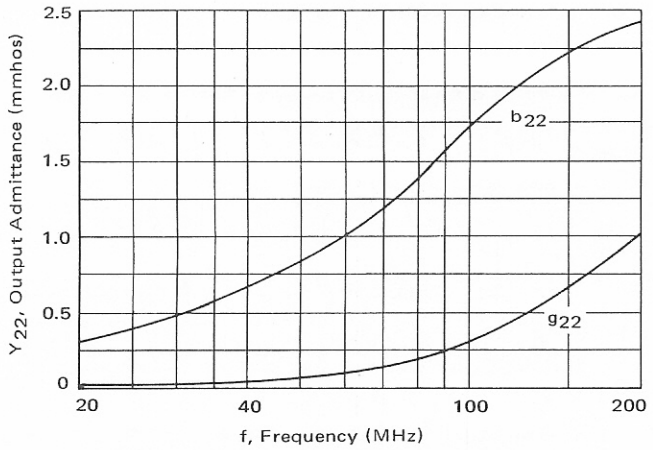


FIGURE 4 – Single-Ended Output Admittance

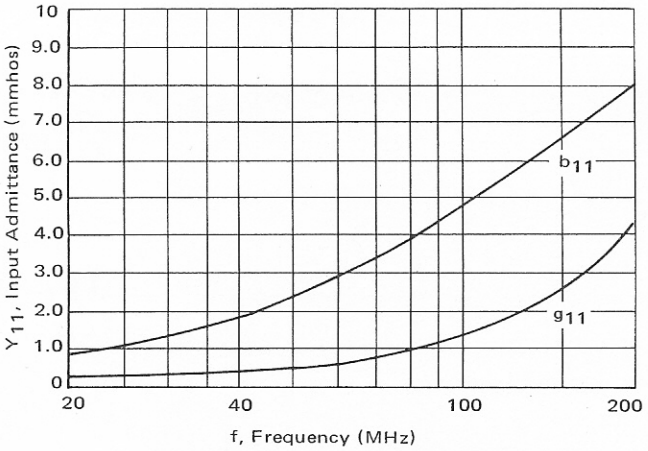


FIGURE 5 – Single-ended Input Admittance

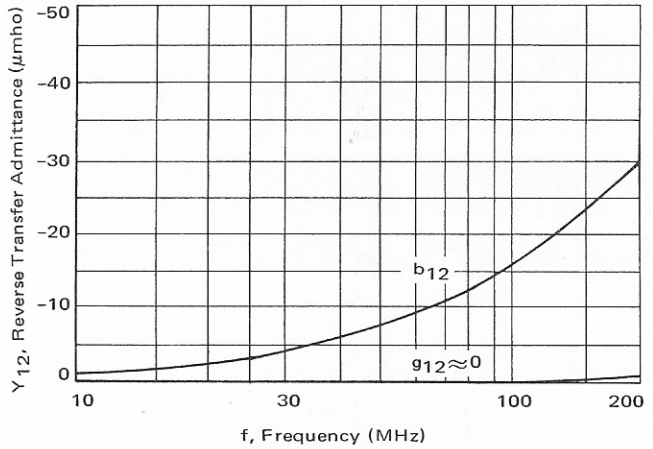


FIGURE 6 – Reverse Transfer Admittance versus Frequency

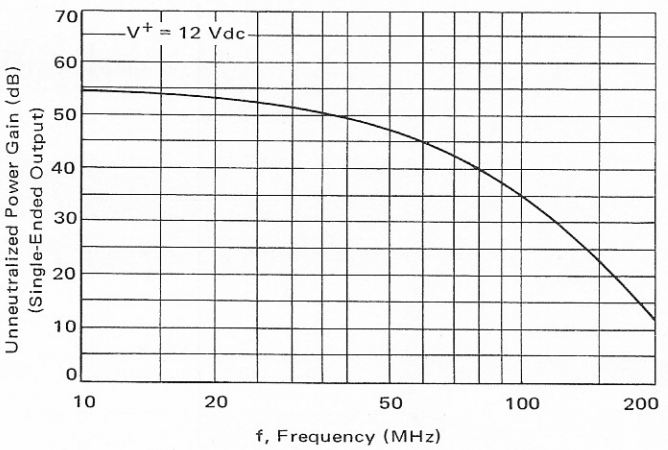


FIGURE 7 – Unneutralized Power Gain versus Frequency

considered to be a more practical value for design calculations than the internal feedback of the device alone. The transadmittance,

$$Y_{21} = \frac{I_2}{E_1}\Bigg|_{E_2 = 0},$$

shown in Figure 3 is for the input applied at pin 1 and the output taken at pin 5, with pins 3 and 6 ac coupled to ground through a capacitor. The low frequency phase shift of Y_{21} between these 2 pins is seen to be 0^o. When the output is taken off pin 6 and pin 5 is ac grounded the low frequency phase shift of Y_{21} is -180^o and exhibits an increasing lag with frequency (assuming the input is again applied at pin 1).

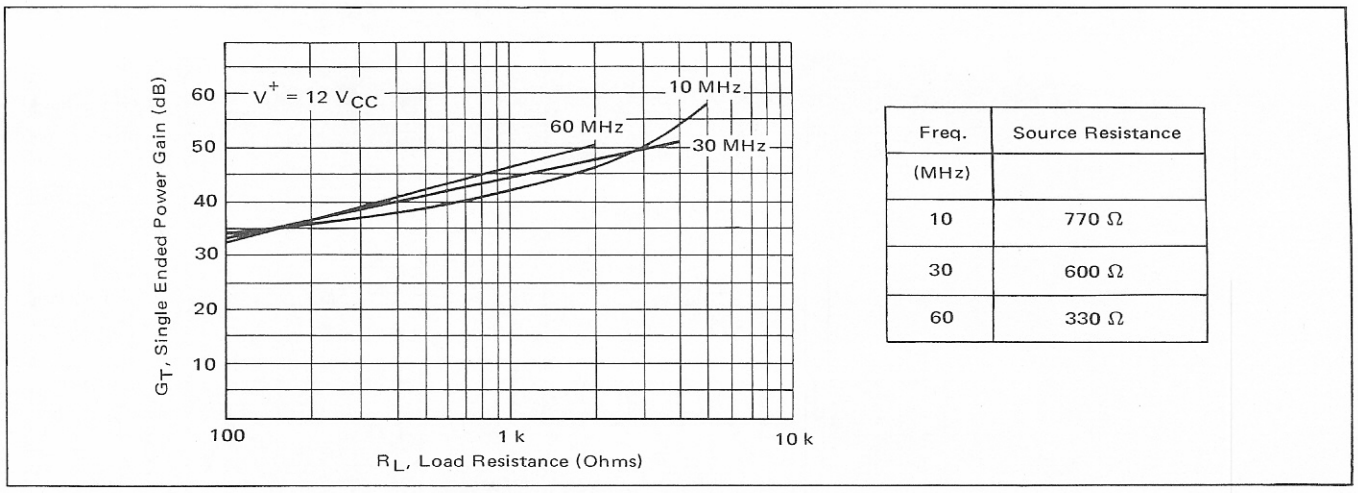
STABILITY AND POWER GAIN

Calculations using the admittance data indicate that for frequencies less than 100 MHz oscillation may occur for certain combinations of load and source impedance. The criterion used to determine device stability was the open circuit or Linvill stability factor C,

$$C = \frac{|Y_{12}Y_{21}|}{2g_{11}g_{22} - R_e(_{12}Y_{21})}.$$

When the absolute magnitude of C is greater than 1.0 the device is potentially unstable. When this condition exists ($<$ 100 MHz, for the MC1590) either mismatching or neutralization must be used to insure circuit stability. The literature[3] provides a detailed discussion of the stability factors referred to in this note and also presents various methods for achieving a stable circuit design. All the amplifiers to be described in this report used mismatching to achieve stability when necessary.

The unneutralized power gain capability versus frequency is shown in Figure 7. The curve shown is the calculated power gain based on the admittance parameters just discussed and is for a circuit stability factor (Stern's Stability Factor, K)[3] of 4.0. A circuit stability factor of 4.0 was chosen to provide a satisfactory compromise between good gain and reasonable stability. The power gain curve represents single ended output operation and has been experimentally verified with test circuits at several different frequencies. These test circuits were carefully laid out and



Freq. (MHz)	Source Resistance
10	770 Ω
30	600 Ω
60	330 Ω

FIGURE 8 – Power Gain versus Load Resistance

shielding was used to isolate the input and output networks. For those amplifiers operating at frequencies less than 100 MHz, mismatching was used to achieve the desired circuit stability. Circuit values for several of these tuned amplifiers are presented in a following section.

Experimental results for unneutralized power gain versus load impedance is given in Figure 8. This data was obtained using amplifiers with single-ended coupling and having tuned circuits at both input and output ports. The load impedance, R_L, in this case is defined as the real part of the RF impedance presented to the collector of the output transistor (Pin 5 or Pin 6). The value of the source impedance, R_S, used at each frequency is also given in Figure 8, and represents the R_S required to achieve the minimum noise figure at that particular frequency.

It is emphasized that the curves shown represent the range of RF load impedances consistent with stable amplifier operation. The designer should recognize that for a given frequency the increased gain achieved by increasing the load impedance is accompanied by a decrease in the relative circuit stability (i.e., a decrease in K factor). When values of R_L greater than those shown are used, some degree of regeneration may result. Increasingly higher-valued load impedances will eventually produce oscillation in amplifiers with operating frequencies less than 100 MHz.

Although these curves are valid only for the specified source impedance they can be adjusted to give an approximate indication of the gain and relative stability for other values of R_S. If the product of R_S and R_L is held constant approximately the same gain and circuit stability will result. For example at 30 MHz, the power gain is 45 dB for a load and source impedance of 1 kΩ and 600 Ω, respectively. If the same gain and stability is desired using a source impedance of R_S = 1200 Ω, then the load impedance should be

$$\frac{1\ k\ \Omega}{2} = 500\ \Omega.$$

Due to the increased gain-per-stage capability of the MC1590G, the layout of the physical circuit is especially important in obtaining optimum performance. Care should be taken to minimize stray feedback between the input and output circuits and parasitic coupling between stages. Toroidal cores can be used to reduce magnetic coupling between input and output coils. When printed circuit boards are used, added input-output isolation can be achieved by placing a ground plane between pins 4 and 8 as shown in Figure 9.

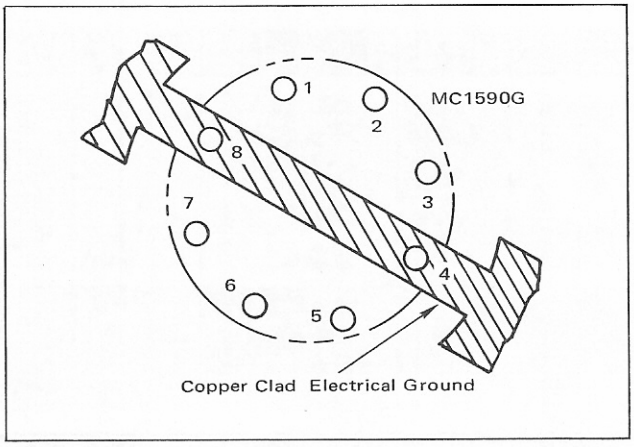


FIGURE 9 – View of Copper Clad Side of Printed Circuit Board

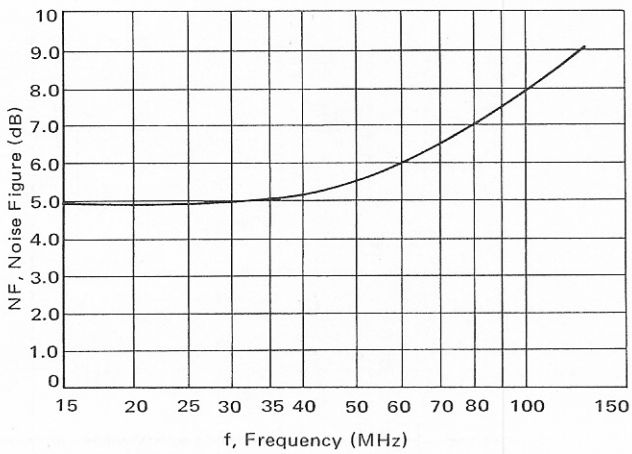


FIGURE 10 – Noise Figure versus Frequency

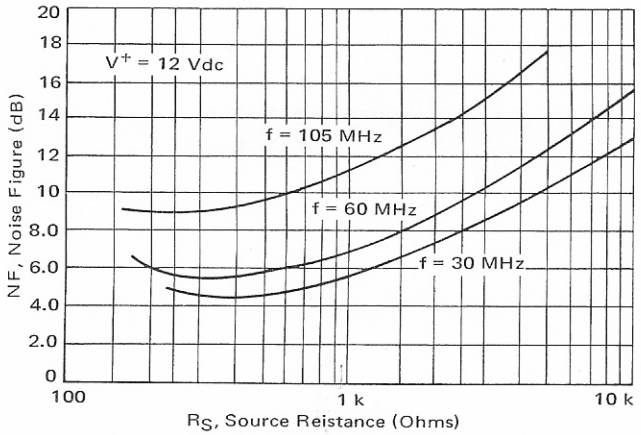
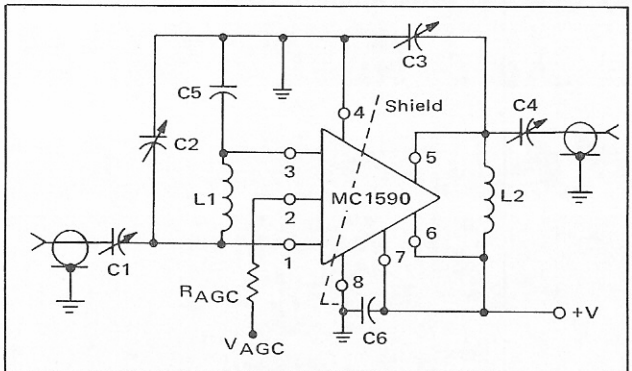


FIGURE 11 – Noise Figure versus Source Resistance



Parameter	30 MHz	60 MHz	100 MHz
Power Gain (dB)	50.8–54	44.2–46.7	31.6–35.7
BW (MHz)	0.7–1.4	1.9–2.4	7.8–9.2
C1 pF	38	1–30	1–30
C2 pF	1–30	1–30	1–10
C3 pF	1–10	1–30	1–15
C4 pF	1–30	1–10	1–10
C5 μF	0.002	0.001	470
C6 μF	0.002	0.001	470
L1 μH	0.6	0.17	0.07
L2 μH	1.35	0.28	0.13
V+ Vdc	12	12	12

FIGURE 12 – Single-Stage Tuned Amplifier

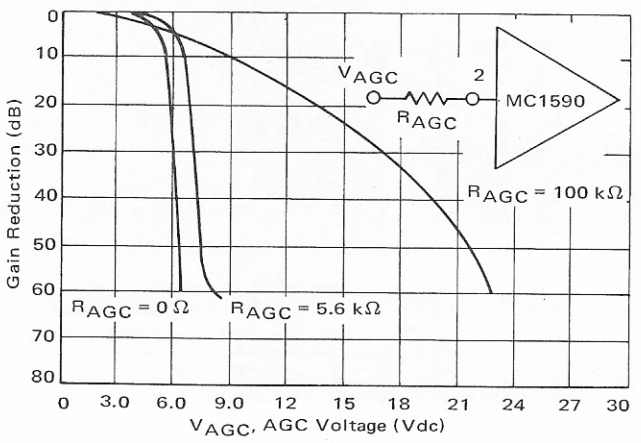


FIGURE 13 – Typical Gain Reduction versus AGC Voltage

NOISE FIGURE

Optimum noise figure versus frequency for the MC1590 is shown in Figure 10. The data was emperically obtained on a Hewlett-Packard 342A noise figure meter at frequencies of 30, 45, 60 and 105 MHz. Although this noise figure is not adequate for the first RF stage of sensitive RF receivers it is sufficient for most IF applications where 20 to 40 dB of RF gain precedes the IF amplifier. Since the noise figure shown in Figure 10 can only be obtained with the optimum source resistance, it is important to know the variation of noise figure with other values of source impedance. This dependence, given in Figure 11, shows that for best noise figure the range of source impedance, R_S, should be more than 200 Ω and less than 1 kΩ. However, this may not always be possible. A particular case being the first stage of an IF amplifier with a crystal filter at the input. Since these filters often require load impedances of several thousand ohms, a noise figure trade-off may be required in achieving good filter characteristics.

SINGLE STAGE TUNED AMPLIFIERS

The circuit schematic for a single stage tuned amplifier configuration is shown in Figure 12. A table of circuit element values is included for amplifiers with center frequencies at 30, 60 and 100 MHz. The performance of these amplifiers, all laboratory built and tested, is also included in the table.

The input for this configuration is applied in a single-ended manner at pin 1 with pin 3 ac grounded through C5. Likewise the output is taken single-endedly off pin 5 while pin 6 is ac grounded through C6. Single-ended coupling has been used to eliminate the need for transformer connections which are usually required when differential coupling is used. In addition to dc blocking, the input and output coupling capacitors, C1 and C4, are used to adjust the effective source and load impedance presented to the amplifier. They can also be used to adjust the gain and relative stability of the amplifier over a wide range of values. Capacitors C2 and C3 are used to tune the input and output networks to resonance. Note that the power gain performance shown in the table represents stable operation with no apparent regeneration as evidenced by an agreement of the design and measured bandwidths. As C1 and C4 are adjusted to reflect higher and higher source and load impedances to the tuned amplifier (i.e. reduced in value) regeneration may occur, resulting in much higher power gains. This regeneration is always accompanied by a narrowing of the amplifier bandwidth.

AUTOMATIC GAIN CONTROL

The typical gain reduction versus V_{AGC} (gain control voltage applied at pin 2) characteristic is shown in Figure 13. Curves are shown for three different values of series resistors, R_{AGC}. This dependence on R_{AGC} is a result of the AGC being a current-controlled rather than a voltage-controlled process. Figure 14, valid over a wide range of R_{AGC} values, shows gain reduction versus I_{AGC} (dc current into pin #2). For a given V_{AGC}, then, the lower series resistance, the larger the available base current drive to Q4 and

Q5 and therefore the greater the gain reduction.

Since the gain reduction is accomplished in the second stage, input and output admittance variations during AGC are held to a minimum. This fact is demonstrated in Figure 15 by the stability of the center frequency and bandwidth at various levels of applied gain reduction. This bandpass characteristic was measured on a 60 MHz amplifier (shown in Figure 12) and an R_{AGC} of 5.6 kΩ. Input and output admittance stability under AGC conditions is quite important in many IF amplifier applications, especially those incorporating crystal filters requiring constant impedance terminations.

GAIN VARIATIONS WITH POWER SUPPLY

Since many integrated circuit applications require operation with power supply voltages less than 12 Vdc, Figure 16 is provided to show the relative gain capability of the MC1590 as a function of power supply voltage. The 60 MHz tuned amplifier was again used as the test fixture with the circuit retuned for maximum gain at each voltage level. The MC1590, by inspection of the data, provides excellent power gain for power supply voltages down to 5 volts. Below this voltage current sources "dry up" and the gain falls off rapidly.

Supply current (I^+) versus power supply voltage (V^+) is also shown in Figure 16. For some applications (e.g., battery powered units) the 15 mA typical drain current required for 12 Vdc may be excessive. However with V^+ = 6 V, the dc supply current is reduced to approximately that which would be required for a discrete, 2-stage IF amplifier. For those applications requiring reduced current drain, the dropping resistor shown in Figure 17 can be used. The proper value for R is chosen by first selecting the V^+ that corresponds to the desired current drain and then computing

$$R = \frac{V_{SUP} - V+}{I^+} \text{ where,}$$

V_{SUP} = available power supply voltage

I^+ = desired current into MC1590

V^+ = bias voltage applied to MC1590 corresponding to I^+ in Figure 16.

In this manner, good single-ended power gains (≈40dB) can be achieved at reduced bias currents.

60 MHz 2-STAGE IF AMPLIFIER

Figure 18 shows the circuit diagram for a 2-stage 60 MHz tuned IF amplifier designed for a nominal 80 dB unneutralized power gain. To achieve maximum gain and output signal swing capability, differential mode coupling is used for the interstage and output networks. For simplicity of design and ease in tuning the input coupling capacitor is a

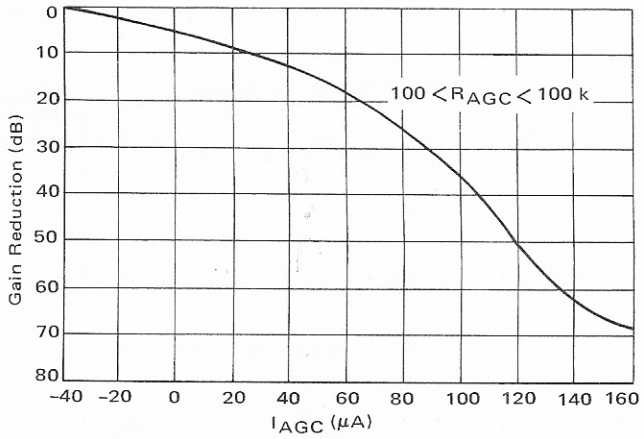


FIGURE 14 – Typical Gain Reduction versus I_{AGC}

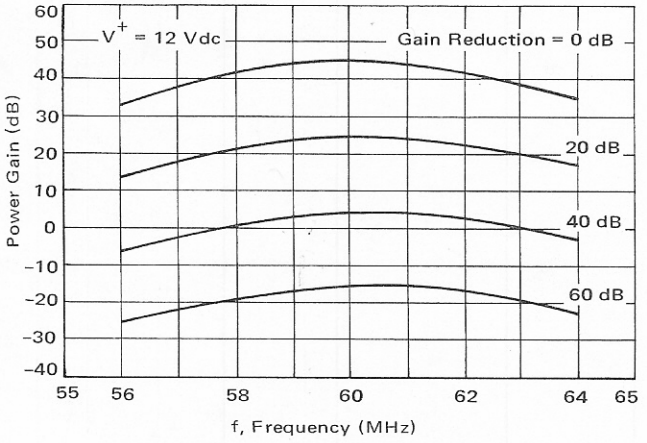


FIGURE 15 – Power Bandwidth versus AGC

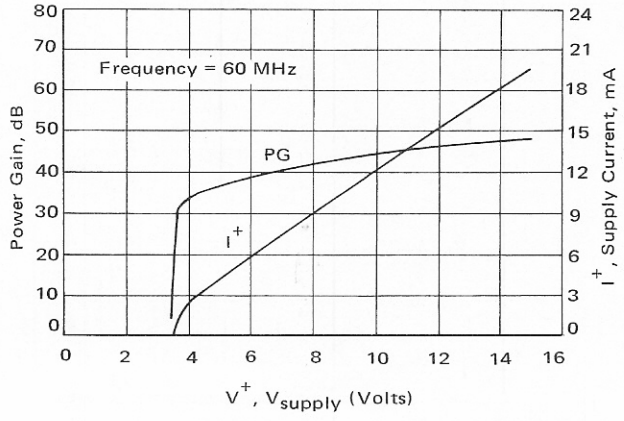


FIGURE 16 – Typical Power Gain versus V_{supply}

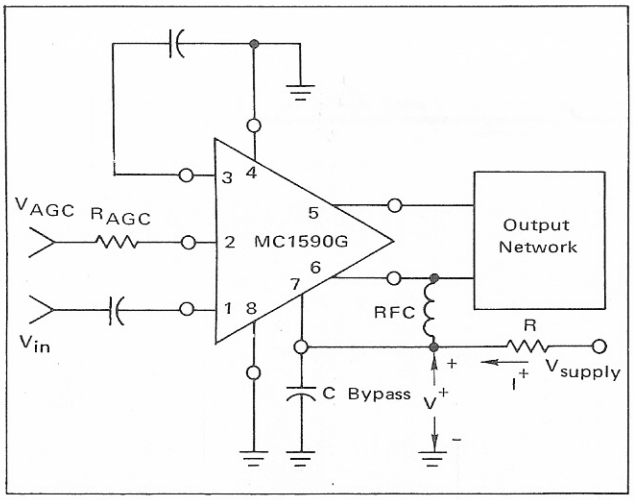
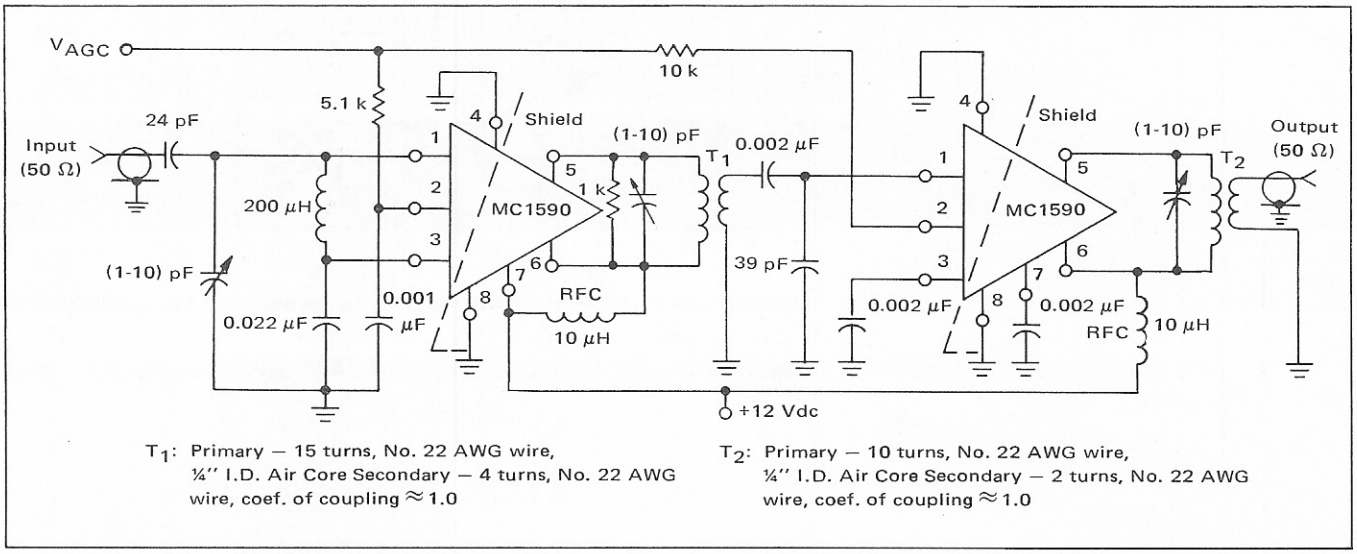


FIGURE 17 – Circuit For Adjusting Supply Current, I^+

fixed value and the interstage network has only one tuning element. The 1 kΩ load resistor across the primary of the interstage transformer is to provide loading sufficient to insure stable operation. With an overall bandwidth of 1.5 MHz the sensitivity for a 10 dB signal to noise ratio was 6 μV. For narrow band IF strips using commerical filters this sensitivity can be somewhat improved.

The values of the 5.1 k and 10 k resistors in series with the AGC pins (Pin 2 of the first and second stages respectively) were chosen to produce a more efficient AGC action. The reason for this is that when large signal levels appear at the input, causing the AGC voltage at pin 2 to rise, it is important that the gain reduction produced by the first stage is sufficient to prevent overloading at the input of the second stage. Recalling Figure 13, the 5.1 kΩ/10 kΩ resistor ratio causes the first stage to AGC faster than the



T_1: Primary – 15 turns, No. 22 AWG wire, ¼" I.D. Air Core Secondary – 4 turns, No. 22 AWG wire, coef. of coupling ≈ 1.0

T_2: Primary – 10 turns, No. 22 AWG wire, ¼" I.D. Air Core Secondary – 2 turns, No. 22 AWG wire, coef. of coupling ≈ 1.0

FIGURE 18 – Two Stage 60 MHz If Amplifier With Power Gain ≈80 dB, and BW ≈1.5 MHz

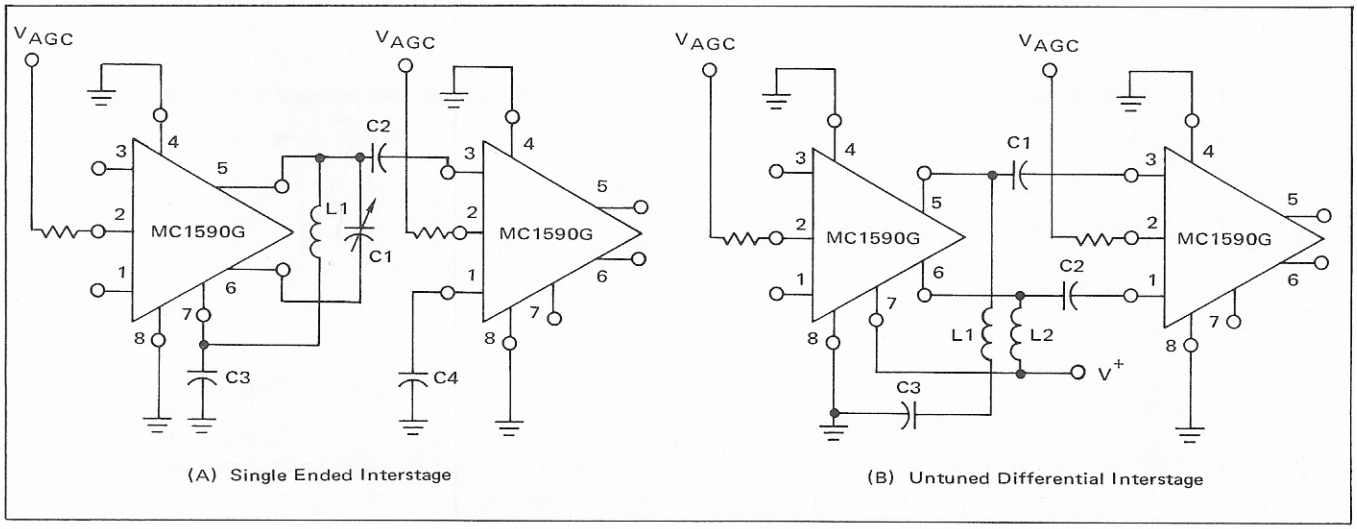


FIGURE 19 – Cascaded MC1590 Schemes

second stage, thereby preventing overloading of the input to the second stage. A two-stage amplifier built and tested with the component values shown exhibited 80 dB power gain and had a bandwidth of 1.0 MHz.

The additional schemes for interconnecting the two MC1590G circuits are shown in Figure 19. The configuration in (A) is for a single-ended tuned interstage connection. Capacitor C2 is for dc blocking and like C3 and C4 should provide a very low RF impedance to the signal. C1 and L1 are used to tune the interstage network to resonance.

A simplified yet effective method for differentially coupling two MC1590G stages is shown in Figure 19 (B). Although some of the available power gain is sacrificed (due to untuned interstage reactances), a 75 dB two-stage power gain at 60 MHz has been achieved with this approach. In this 60 MHz design, inexpensive molded chokes (5.6 μH) were used for L1 and L2 while C1, C2 and C3 were each 0.001 μF ceramic disc capacitors.

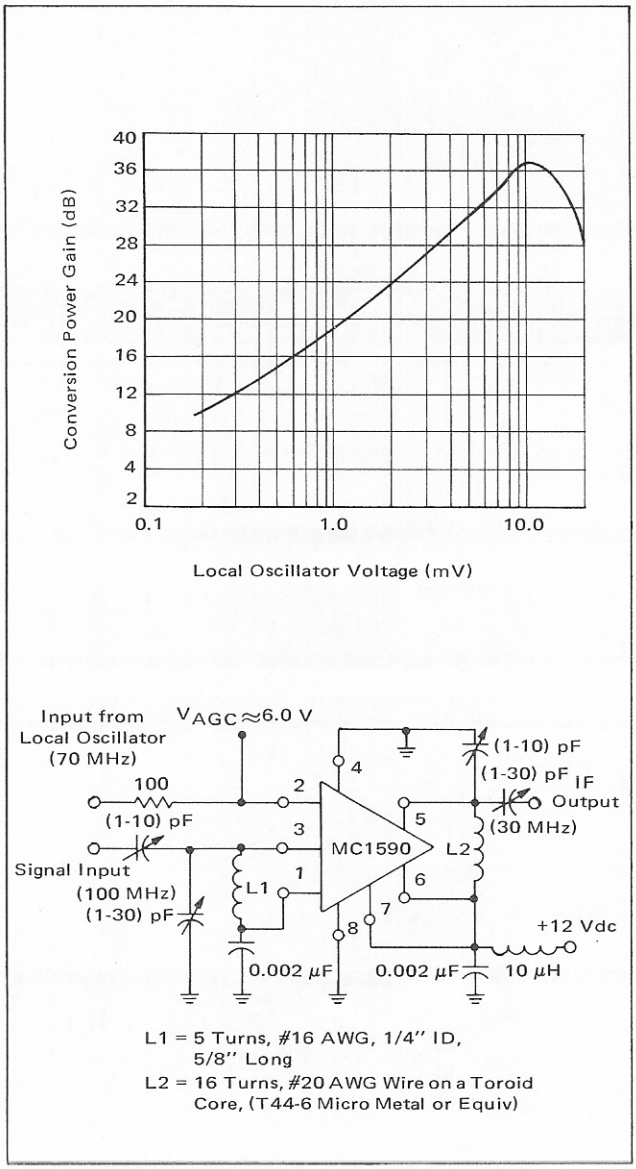


FIGURE 20 – A 100 MHz Mixer

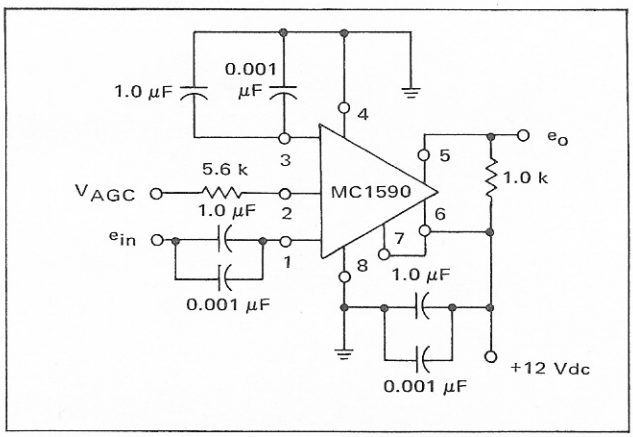


FIGURE 21 – Video Amplifier

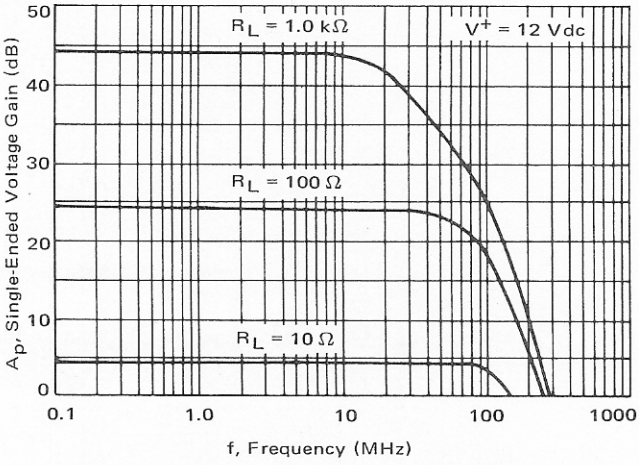


Figure 22 – Voltage Gain versus Frequency

100 MHz MIXER

When pin 2 is biased near the center of the linear portion of the AGC characteristic, the MC1590G can also be used as a frequency converter. When the local oscillator signal is applied to the AGC pin and the signal is applied between the input pins, the familiar sum and difference frequencies are produced at the output. Figure 20 shows the schematic for a mixer of this type with a signal frequency of 100 MHz and a local oscillator frequency of 70 MHz. The 30 MHz difference frequency is filtered at the output. Also shown in the figure is the mixer conversion gain versus local oscillator voltage for the test circuit. In addition to the exceptionally high conversion gain the circuit also provides excellent isolation of the signal source from the local oscillator. With this frequency conversion capacity it is possible to construct a 2 stage mixer-IF amplifier combination with a total power gain of 70 dB. Although this combination has not been experimentally tested it should exhibit good stability and would also have AGC capabilities.

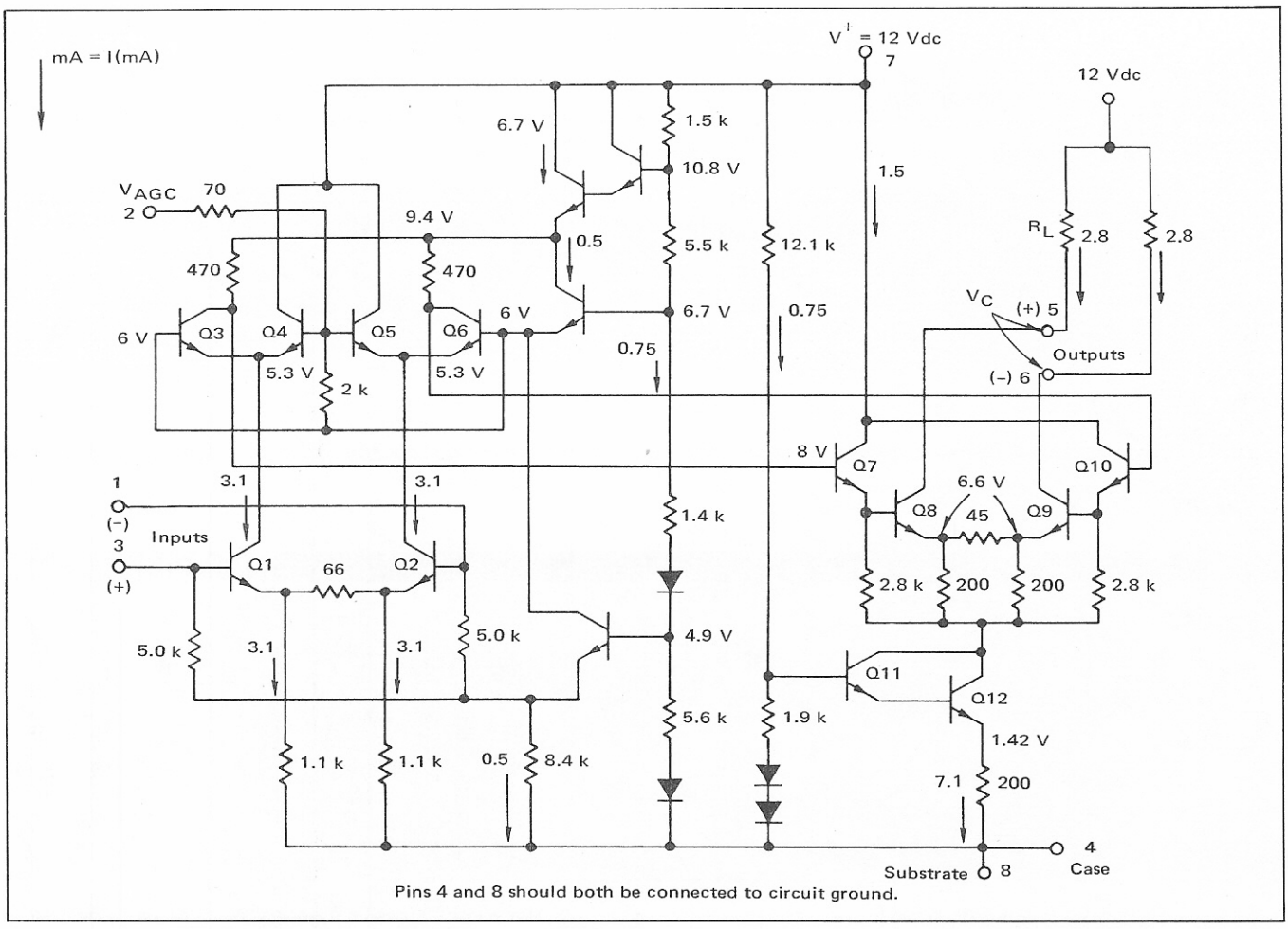


FIGURE 23 – MC1590G Bias Voltages and Currents

VIDEO AMPLIFIER

By replacing the output tuned circuit with the proper valued load resistor, the MC1590G can also be used as a wide band video amplifier (Figure 21). In addition to its high gain, the AGC capability makes the MC1590 quite attractive for video amplifier applications. Voltage gain versus frequency for several values of load resistance is shown in Figure 22. Several MC1590G icrcuits can be cascaded to increase the gain. To cascade two MC1590G circuits, the two input pins need only be capacitively coupled to the output pins of the previous stage.

DISTORTION CHARACTERISTICS

When discrete series resistors are used for collector loads as in the video amplifier circuits, an upper limit is imposed on the value of the load resistor. Figure 23 shows the quiescent current and voltages for $V^+ = 12\ V_{DC}$ and no AGC applied. The constant current source Q11-Q12 produces 2.8 mA (typ) quiescent collector current in Q8 and Q9. For the maximum linear output voltage swing, R_L should be such that the quiescent collector voltage (V_C) is midway between V^+ and the emitter voltage (V_E) of Q8 and Q9, i.e.,

$$R_L = \frac{V^+ - V_E}{2I_C} = \frac{12 - 6.6}{2(0.0028)} = \frac{5.4}{5.6 \times 10^{-3}} \approx 1\ k\Omega$$

When values of R_L greater than 1 k are used V_C approaches V_E and the output signal swing is reduced. The maximum differential output voltage swing for $V^+ = 12$ Vdc and $R_L =$ 1 k is approximately twice the single ended output voltage swing and is,

$$V_{max} = 2\ [V_{CE} - V_{CE(sat)}] \quad 2(5.4 - 0.3) \quad 10.2\ V_{pp}$$

However at this signal level the waveshape is quite distorted. Figure 24 shows a more practical value of output signal swing. The figure shows the level of output signal swing at which 5% THD in the output waveshape occurs. It is important to note that the amplifier used for this test was a video amplifier with load resistors of 1 kΩ. The signal frequency was 50 kHz with a single-ended input and differentially coupled output. When AGC is applied, the available level of output voltage swing is reduced. This reduction in output signal swing with applied AGC is due to an attendent increase in the emitter voltage, V_E, of the output tran-

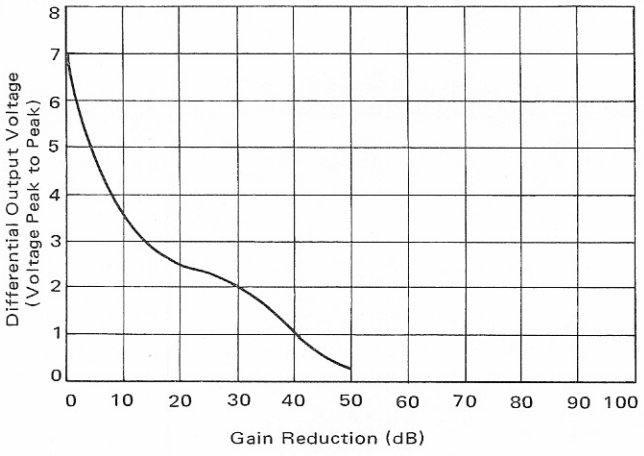


FIGURE 24 – Differential Output Voltage @ 5% THD

sistors. As AGC is applied and bias current is switched from Q3 and Q6 to Q4 and Q5 the voltage at the collectors of Q3 and Q6 rises and therefore V_E rises. Under conditions of maximum gain reduction V_E rises to approximately 8.2 Vdc, reducing V_{CE} of the output transistors accordingly. The reduced output voltage swing capability for gain reductions greater than 30 dB is no longer due to a decrease in the output transistors V_{CE}. Above 30 dB of AGC the input signal level becomes excessive (>200 mV.) and the major contribution to distortion is overdrive of the input transistor's base emitter junction.

The curve in Figure 24 cannot be used to provide a valid indication of the performance of high frequency tuned amplifiers. This is in part due to ringing in the tank circuit and rejection of harmonics out of the pass band. With V^+ = 12 Vdc, the maximum tuned circuit differential output voltage is approximately

$$V_{O(max)} = 4\,[V^+ - V_E - V_{CE(sat)}]$$

$$= 4\,(12 - 6.6 - 0.3) \mid 20.4\ V_{pp}$$

It is important to realize that maximum output voltage excursions can be achieved only if current limiting is avoided. Due to the constant current available to the output transistors, the output voltage swing at either collector is current limited to,

$$V_{out} = I_O R_L \mid$$

$I_O = I_{C1} + I_{C2}$ = constant current

R_L = real part of RF load.

For example, if V^+ = 12 Vdc then I_O = 5.6 mA. With R_L = 500 Ω the single-ended output voltage is limited to 0.0056(500) = 2.8 V_{pp}. For a differential output the collector voltages add and the maximum output voltage is current limited to 5.6 V_{pp}.

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