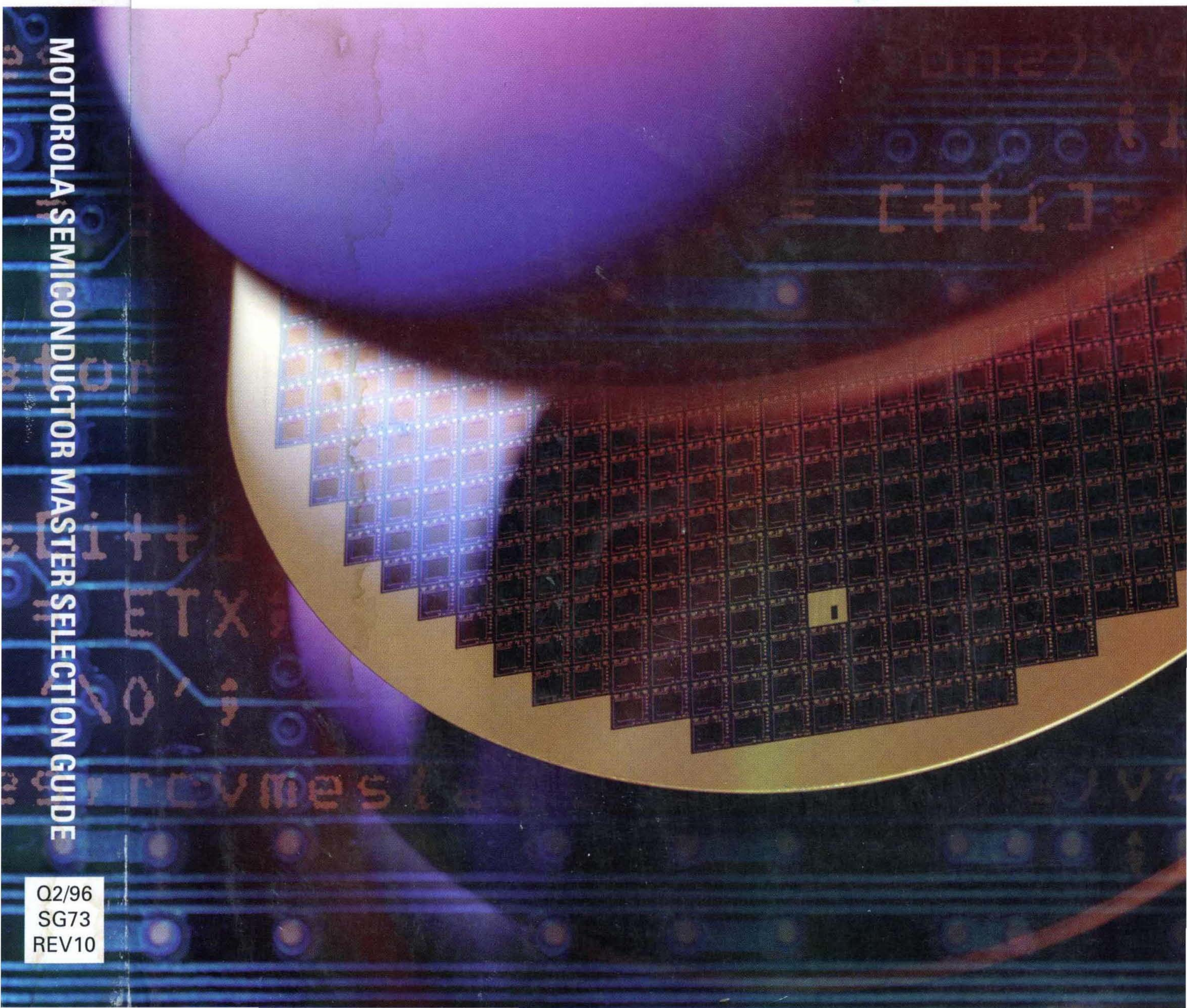
MOTOROLA

SG73/D
REV 10

MOTOROLA SEMICONDUCTOR
MASTER SELECTION GUIDE



MOTOROLA

Master Selection Guide

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Master Selection Guide

Where We Stand. . .

Total Customer Success

Service, speed and facility of response, product quality and reliability are the goals to which we are dedicated. Our commitment to progress such as Six Sigma performance and Cycle Time Reduction are symbolic of a culture in which Total Customer Success is, overwhelmingly, our primary objective.

In today's highly competitive market, selecting the most effective semiconductor components for a given application poses a significant challenge. The range of available functions and the sheer number of components within each unique product line is staggering. Add to this the number of vendors capable of satisfying a portion of the overall system demands and the selection of a cost–effective component complement can be as time consuming as the design of the system itself.

This is where Motorola occupies a unique position among semiconductor manufacturers – one that can significantly shorten the product selection cycle. Please consider these facts:

As a manufacturer of semiconductors since the very beginning of the technology, Motorola has emerged as a leading supplier of such components to the world market.

Motorola's product line is the *broadest* in the industry, capable of filling 75–80% of the many applications for semiconductor devices.

In each of its various product categories, Motorola is a recognized leader, with leading edge products as well as commodity products for mass applications.

Motorola's vast network of sales offices and distributors, augmented by manufacturing centers throughout the world, not only ensures easy communications, cost–effective pricing and rapid service, but guarantees a continuing stream of state–of–the–art products based on world–wide experience and demand.

How To Use This Guide. . .

This Selection guide is arranged to provide three–way assistance to engineers and technicians in making a first–order selection of components best suited for a specific circuit or system design.

If you have a device number that needs identification or if you want to know if Motorola manufactures a particular device type:

1. Turn to the Device Index for a complete listing of Motorola products, and the page numbers where more detailed information is given for these products.

If you have a device name or acronym and wish to know if Motorola makes such a device:

2. Look for it in the Subject Index.

If you want an overview of Motorola products for a specific product category:

3. Refer to the quick–reference product line guide located at the front of this publication or use the table of contents located at the front of each section.

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Semicustom Application Specific Integrated Circuits

In Brief . . .

Motorola supports strategic programs and co–development partnerships to accelerate the availability of advanced processes (CMOS, BiCMOS, Bipolar), packaging and CAD technology. Extensive research, manufacturing and financial resources are focused to develop and maintain leading edge capabilities.

ASIC Preview

Bipolar

ECL & ETL Series Arrays

Motorola's MOSAIC III™ technology features modified transistor structures to reduce series base resistance and collector–base junction capacitance. The result is enhanced switching speed. Mixed ECL/TTL interface compatibility and high frequency (over 2.5 GHz) operation highlights the ETL Series.

CMOS

1.0 Micron HDC Series
Sub–Micron H4C & H4CPlus Series

High density CMOS arrays (HDC Series) are built on 1.0 micron drawn, triple–layer–metal CMOS process. By utilizing three layers of metal for signal routing, designers can achieve greater utilization on a channelless architecture.

The sub–micron ($0.7\mu L_{eff}$) H4C Series enables densities over 300 K gates with 365 picosecond typical gate delay performance. It's available in Custom Defined Architecture (CDA).

Motorola's highest performance 0.6 micron CMOS arrays, the H4CPlus Series, are targeted for mixed 3.3 V and 5 V applications. The H4CPlus arrays range in density from 28,400 to 178,000 available gates with packages ranging from 128 QFP to 313 OMPAC.

Design Automation Software (OACS™)

Motorola's Open Architecture CAD System (OACS) provides a complete ASIC development environment using industry–standard workstations and leading third–party design and verification tools. The OACS system integrates sophisticated ASIC design software tools to handle high performance designs and has the required flexibility to support future technology advances.

Advanced Packaging

OMPAC: (Over–Molded Pad Array Carrier), a surface mount plastic package with solder bumps instead of traditional pins for interfacing to printed circuit boards.

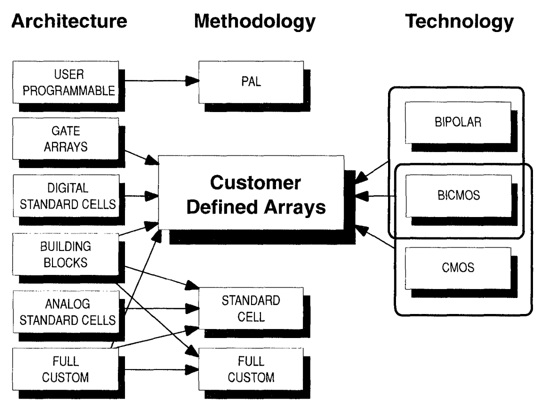
QFP–MCR: Quad Flat Package in lead counts from 64 to 304 in optional Molded Carrier Ring which provides coplanarity and lead protection during manufacturing, testing and shipping.

MicroCool QFP: A new QFP–compatible plastic package with heat slug attached for improved heat dissipation capacity.

Architecture for the 90's CDA™ (Customer Defined Arrays)

Performance, density and power dissipation are critical issues for next generation ASIC designs. The integration of large diffused blocks and embedded memory enhances intra–chip communication and saves board area. The Customer Defined Array (CDA) concept lets designers combine array–based, cell based, and full custom logic with diffused memory blocks on a die. The concept equally supports Bipolar and CMOS, each with the capability to incorporate BiCMOS modules.

CDA — The Architecture of the '90s



Benefits

- **Time–to–market through integration of functional building blocks and ASIC design methodology.**
- **Customers can create application specific arrays.**
- **Diffused RAM optimized for performance and density.**
- **Fixed die sizes for ease of manufacturing.**

Bipolar
ECL & ETL Series Arrays

Third Generation

ETL Series Arrays
Extend Design Flexibility

The ETL Series is flexible enough to simplify translation between high speed logic families.

Three base arrays:
MCA750ETL, MCA3200ETL, MCA6200ETL

- 848 to 6915 Equivalent Gates
- Channelled Architecture for up to 100% Utilization
- Input and Internal ECL Gate Delays – 0.20 ns (Typical)
- TTL Input/Translation Cell Delay – 0.55 ns (Typical)
- Up to 168 Universal I/O Signal Ports
- Bidirectional ECL and TTL I/O Macros
- ECL 100 K, Pseudo ECL and TTL Logic Interfaces
- Programmable Speed/Power Levels
- Three–Level Series Gated Macros
- MCA2 and MCA3 ECL Series Library Compatible

Motorola's MOSAIC III bipolar process offers unexcelled mixed TTL/ECL interface capability in a high performance, mature technology.

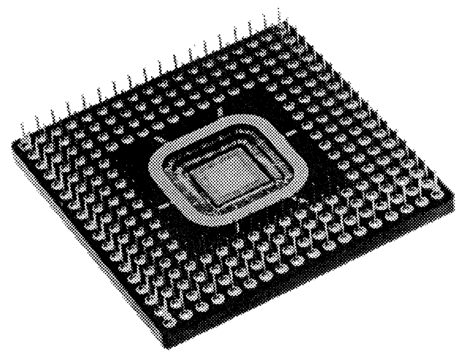


Figure 1. MCA6200ETL in Multi–Layer Ceramic 224 Pin–Grid–Array Designed for High Frequency, Mixed–Mode Applications

ETL Series Features
Mixed ECL–TTL Interface

The ETL Series offers mixed ECL, PECL (pseudo ECL) and TTL compatible interfaces. The Series combines 200 ps typical gate delays with 2500 MHz operating frequencies. Any signal pin can be programmed for input, output, or bidirectional signals in ECL, TTL or PECL logic. MOSAIC III process technology, combined with innovative design, extensive macrocell library and versatile I/O structure adds up to superior performance and flexibility.

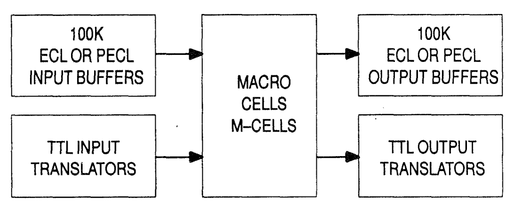


Figure 2. ETL Series Block Diagram

Table 1. ECL & ETL Series Features

Array / Features	MCA 2200ECL	MCA 10000ECL	MCA 750ETL	MCA 3200ETL	MCA 6200ETL
Technology	MOSAIC III				
Equivalent Gates	2412	12402	848	3570	6915
Internal (Major) Cells	68	414	24	110	225
I/O Signals	108	256	Universal I/O Ports		
Input/Interface Cells	96	224	42	120	168
Output (O) Cells	96	200			
Max Gate Delay (ns)	0.175	0.175	0.2	0.2	0.2
Max I/O Frequency (MHz)	1500	1200	2500	2500	2500
Typical Power Dissipation (W)	3–6	10–30	1–2	4–7	7–12

CMOS

1.0 Micron CMOS HDC™ Series

Triple–Layer Metal

Built on a 1.0 micron, triple–layer metal CMOS process, the HDC Series represents a significant advancement in microchip technology. By utilizing three layers of metal for signal routing and power distribution, designers can achieve maximum utilization on a channelless architecture having minimum chip dimensions. The result is high performance combined with I/O flexibility and density.

The HDC Series is available in a wide variety of plastic surface mount packages. The diversity of package style and pin count lets the designer best match system size, cost and performance requirements.

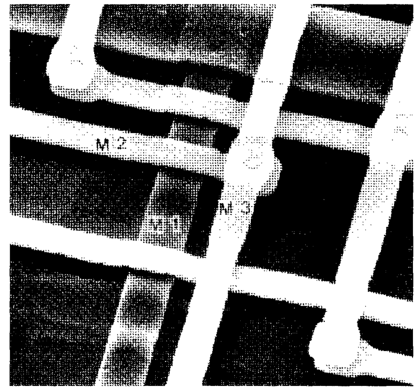


Figure 3. Triple–Layer Metal Signal Routing Enhances Utilization

Features

- 3,000 to 49,000 available gates
- Up to 70% utilization
- Channelless Sea–Of–Gates architecture
- 1.0 micron drawn gate length (0.8 μL_{eff})
- Triple layer metal routing and power distribution
- Eight transistor, fully utilizable, oxide isolated primary cell
- 475 picosecond typical gate delay (2–input NAND)
- Fixed RAM blocks (single, dual and quad)
- 5 V CMOS and TTL compatible I/O options
- Low power consumption of 6 µW/gate /MHz
- I/O cells can be paralleled on–chip for 48 mA drive
- Pin functions are 100% programmable as I/O or power on plastic packages
- 1000 V ESD protection, latchup immunity to 100 mA
- Comprehensive workstation based CAD support

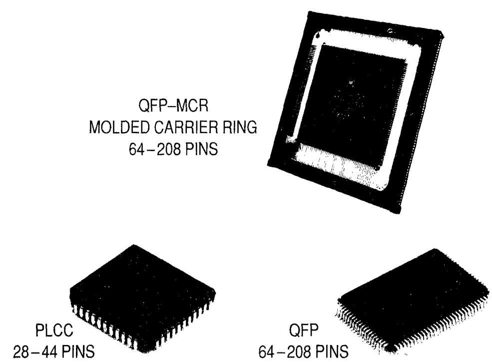


Figure 4. Typical HDC Series Packages

Table 2. HDC Series Features

Array	Available Gates	# of Die Pads (Wirebond)	Available I/O Cells	Die Size (mils square)	Package Pins
HDC003	3,036	76	88	136	28–68
HDC006	5,670	96	120	168	28–84
HDC008	8,208	108	144	182	28–100
HDC011	11,208	120	168	202	28–100
HDC016	16,416	136	204	232	68–128
HDC027	27,270	168	264	282	84–160
HDC031	31,290	180	280	295	68–160
HDC049	49,368	216	352	354	160–208

Sub–Micron CMOS H4C™ Series

CDA Architecture

The H4C Series of CMOS Customer Defined Arrays™ (CDA) provides a new generation of ASICs to capture the functionality of the sub–micron process. The new fabrication process of the H4C Series supports speed requirements of 60 MHz processors with a power dissipation of only 3 µW/MHz/gate.

The CDA architecture offers the versatility and efficiency of system design on a single chip by providing large, fully–diffused architectural blocks such as user configurable SRAMs. Additionally, to ensure high quality ASIC system designs, several design–for–test implementations and clock skew management schemes are available.

Features

- 18,080 to 317,968 available gates
- Compatible channelless, Sea–Of–Gates and CDA architectures
- 0.7 micron effective gate length
- Triple–layer–metal signal routing and power distribution
- Up to 70% gate utilization (smaller arrays)
- 365 picosecond typical gate delay (2–input NAND)
- User configurable, fully diffused SRAM blocks up to 256K bits
- Low power consumption – 3 µw/MHz/gate
- 3.3 V and 5.0 V CMOS and TTL compatible I/O cells
- BIST, JTAG (IEEE 1149.1) and LSSD/ESSD scan supported
- Digital PLL to manage clock skew
- Boundary scan embedded in periphery
- Extended workstation–based CAD support for embedded functions
- Clock tree synthesis and clock skew management

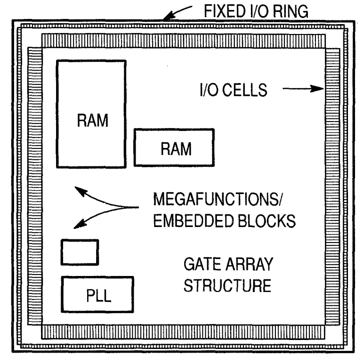


Figure 5. The CDA Concept: Megafunctions and Embedded Blocks Within a Gate Array

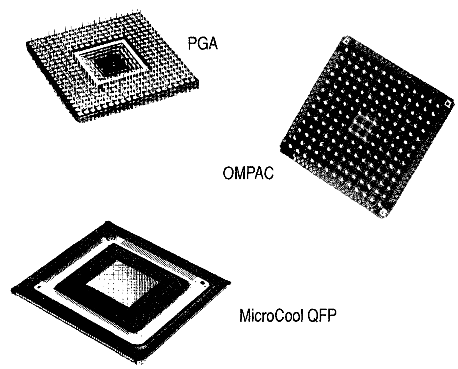


Figure 6. Typical H4C Series Packages

Table 3. H4C Series Features

Array	Available Gates	# of Die Pads	I/O Cells	Package Pins
H4C018	18,080	136	160	80–120
H4C027	27,048	160	196	80–128
H4C035	35,392	176	224	80–160
H4C057	57,368	216	284	80–225
H4C086	85,956	256	344	120–225
H4C123	123,136	304	416	160–313
H4C161	161,364	344	476	160–313
H4C195	195,452	376	524	160–375
H4C267	266,832	432	612	447
H4C318	317,968	468	668	447

Product Preview

Sub–Micron CMOS H4Plus™ Series Mixed 3.3 V/5.0 V Levels

The new sub–micron CMOS H4CPlus Series is targeted for mixed 3.3 V and 5 V applications, as well as low–power 3.3 V systems. The H4CPlus arrays range in density from 28,400 to 178,000 available gates with packages initially ranging from 128 QFP to 313 OMPAC.

A key feature of this family is a powerful I/O buffer aimed at meeting the requirement for GTL I/O levels and capable of driving backplanes of 50 Ω transmission lines in today's high–performance RISC/CISC microprocessor–based systems.

For the highest possible chip–to–chip operating frequencies, the H4CPlus family introduces Current Mode Transceiver Logic™ (CMTL™) buffers. This new self–terminating I/O method permits CMOS chip–to–chip interface speeds (using typical differential or single–ended inputs) to 250 MHz, at low power dissipation. It also provides a differential interface directly to industry standard ECLinPS™ logic when used with a +5 V rail.

Features:

- 0.6 micron effective gate length
- Typical gate delay of 280 ps for a NAN2, FO = 2 at 5 V
- Power dissipation of 1 µW/gate/MHz at 3.3 V
- Standard 5 V high performance or 2.7 V to 3.6 V low power configurations, with mixed 3.3 V and 5 V combinations
- Single I/O site, 2 mA to 24 mA drive, TTL and CMOS output macros
- PECL input buffer macros supporting inputs to 250 MHz Typical
- Current Mode Transceiver Logic I/O buffer for self–terminated, high–speed differential or single–ended interfacing to 250 MHz
- Separate 5 V and 3.3 V power bussing
- Embedded analog PLL* macros for up to 125 MHz clocks
- Industry standard JTAG boundary scan built into I/O macros
- DFT methodology support (JTAG, BIST, LSSD, ESSD)

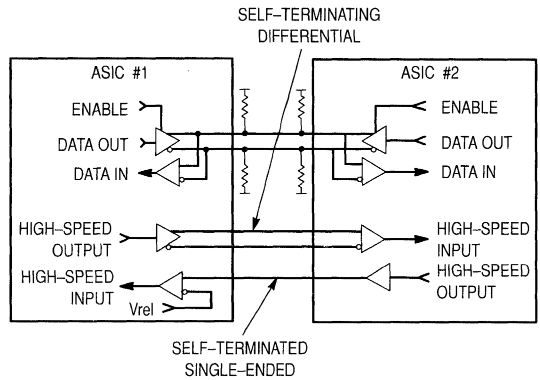


Figure 7. Interfacing H4CPlus Series with Current Mode Transceiver Logic

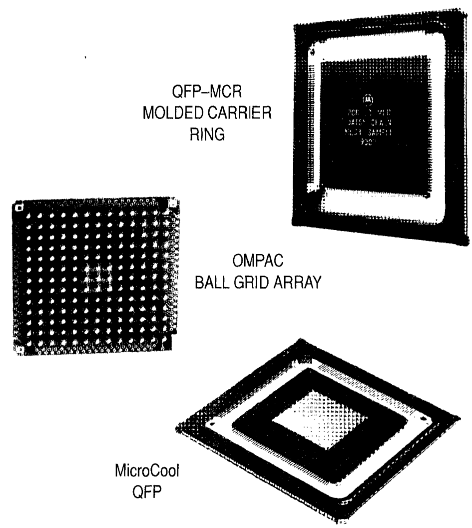


Figure 8. Typical H4CPlus Series Packages

Table 4. H4CPlus Series Features

Array Name	Available Gates	Die Size (mils/side)	Die Pads Wirebond	I/O Cells	Package Pins
H4CP028	28,400	239	176	160	128–169
H4CP048	48,100	287	216	208	128–225
H4CP075	74,520	337	256	256	128–225
H4CP109	109,368	391	304	312	160–313
H4CP146	145,544	438	344	360	160–313
H4CP178	178,000	476	376	400	160–313

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Design Automation Software

Motorola has worked closely with several leading CAD/CAE vendors to integrate the best design tools in the industry into one system. In many cases, Motorola has been instrumental in the definition and refining of key third–party design tools.

To satisfy specific CAD requirements, Motorola has developed several design tools to perform netlisting and translation, rule checking, delay and timing calculation, fault grading and automatic test pattern generation, floorplanning, test vector analysis and processing.

The OACS 2.2 and 3.1M features chart briefly describes Motorola's OACS™ ASIC design system options.

OACS™

Open Architecture CAD System

The Open Architecture CAD System™

The Open Architecture CAD System (OACS) offers a highly versatile and powerful design environment for the design of Motorola's H4CPlus, HC4 Series, and HDC Series CMOS arrays. The OACS integrates several of the industry's most powerful design tools with Motorola's high–performance tools into a standard EDIF based CAD environment. The release of this Design Reference Guide corresponds to the release of two major versions of OACS: OACS 2.2 and OACS 3.1M.

OACS 2.2 is Motorola's point tool CAE solution based on Cadence's Concept™ schematic editor, Synopsys' synthesis tools, and Cadence's Verilog™ logic simulator.

OACS 3.1M is Motorola's framework based CAE solution using Mentor's Falcon Framework™. This solution provides support of Mentor's design entry tools and QuickSim II logic simulation.

OACS™ 2.2 and 3.1M Features:

- EDIF 2.0.0 backplane approach to providing an open design environment
- Supports the following third–party design tools:
  - Synopsys' Design Compiler™, HDL Compiler™, Test Compiler™ (optional) and Design Wave™
  - Cadence's Concept™ schematic capture (2.2)
  - Cadence's Verilog XL™ simulator and Veritime™ static timing analysis (2.2)
  - Quad Design's MOTIVE® static timing analysis (optional) (2.2)
  - Mentor Graphics' Falcon Framework™ (3.1M)
  - Mentor Graphics' QuickSim II™ simulator and QuickPath™ static timing analysis (3.1M)
  - Mentor Graphics' AutoLogic™ design synthesis tool
  - Cadence's Gate Ensemble™ and Dracula™ physical layout and verification tools (factory only)
- Motorola design tools:
  - Memorist™ diffused SRAM compiler (optional)
  - Mustang™ automatic test pattern generation (optional)
  - TestPAS™ test vector validation and extraction
  - ERC and MARV comprehensive electrical and manufacturing rules checking
  - PrediX™ floorplanning (optional)
- Testability support: ESSD/LSSD scan, JTAG boundary scan, BIST, and scan synthesis
- Sophisticated delay and timing limits calculations for accurate simulation and timing analysis
  - Estimated and actual (back–annotated) wire capacitances
  - Includes intrinsic, rise/fall time, output pin loading and distributed RC delays
  - Continuous process, temperature, and voltage variation
- Clock skew management: clock–tree synthesis, PLL, timing driven layout
- Supports multiple technologies: HDCMOS, H4C, H4C–CDA–1C, H4CPlus
- Supported on HP9000/7XX and SUN–4 SPARC® workstations

Advanced Packaging

Low cost, high performance systems require excellence in ASIC packaging technology. MicroCool, QFP–MCR (Quad Flat Pack in an optional Molded Carrier Ring), and Over–Molded Pad Array Carrier (OMPAC) packages illustrate cost effective manufacturing solutions for high lead count, high frequency applications.

Quad Flat Pack Molded Carrier Ring (MCR–QFP)

Motorola currently offers the popular EIAJ standard Plastic Quad Flat Package (QFP) in lead counts from 64 to 240 pins. The Molded Carrier Ring (MCR) is a coplanarity and lead protection device for QFP packages. The ring provides lead protection during manufacturing/testing and shipping.

Standard ring sizes simplify manufacturing across the range of packages and improve component testability.

MicroCool™ Quad Flat Pack

The MicroCool QFP is a new QFP compatible plastic package with improved heat dissipation capacity. It has a heat slug attached to a printed circuit board which supports a copper lead frame. The package incorporates a molded carrier ring to maintain pin coplanarity. Lead counts range from 64 to 304 points. MicroCool packaging is cost–effective and capable of meeting high power dissipation (up to 5 W, depending on temperature and ambient conditions).

Features:

- Thermally improved footprint compatible version of MCR–QFP package
- Constructed using PCB with attached leadframe and heat slug. The die is attached to the slug which is exposed on the package top surface
- Coplanarity less than 4 mils using MCR techniques–(PCB material aids good coplanarity by cutting bowing of plastic)

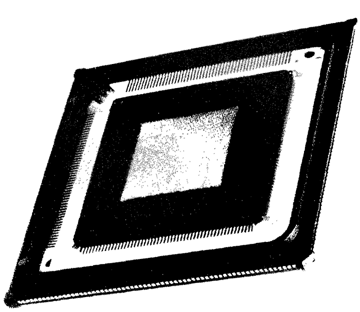


Figure 9. MicroCool Quad Flat–Pack in Molded Carrier Ring Lowers Board Cost and Improves Thermal Performance

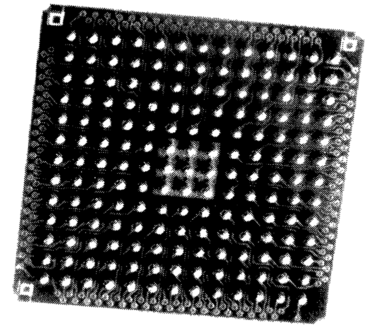


Figure 10. 169–lead OverMolded Pad Array Carrier (OMPAC) Saves Board Space and Improves Manufacturing Yields

Over–Molded Pad Array Carrier (OMPAC™)

OMPAC consists of a thin double metal printed circuit board, overmolded with plastic. The integrated circuit is attached to a gold–plated die flag on the substrate with a silver–filled epoxy. Electrical connections to the integrated circuits are made using conventional gold ball bonding techniques.

Primary Advantages Over QFP

- Eliminates concerns with lead coplanarity
- Improved electrical performance
- Comparable or better thermal performance
- Requires less costly PCB pitch
- Smaller size
- No risk of lead damage
- Improved manufacturing yields
- Competitive pricing

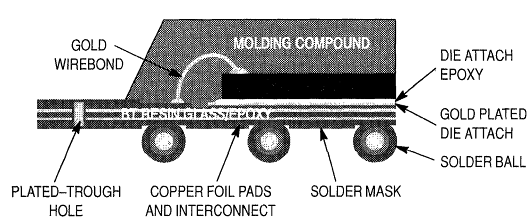


Figure 11. Simplified Cross–Sectional View of OMPAC

Literature

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Order Number	Description
Design Manuals	
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H4CPDM/D	H4CPlus Series CMOS Arrays
HDCDM/D	HDC Series CMOS Arrays
MCA3ECL/D	MCA3 ECL Series Arrays
MCA3ETLDM/D	MCA3 ETL Series Arrays
MC92005UM/D	SBus Interface Controller
Data Sheets	
ETL/D	MCA3 ETL Series Macrocell Arrays
H4C/D	Sub–micron H4C Series CMOS Arrays
H4CP/D	H4CPlus Series CMOS Arrays
HDC/D	HDC Series CMOS Arrays
MCA2200ECL/D	MCA2200ECL Macrocell Array
MCA10000ECL/D	MCA10000ECL Macrocell Array
MC92005/D	Slave Interface Controller
Brochures/Selector Guides/Misc.	
SG367/D	ASIC Product Overview
BR916/D	Packaging Manual for ASIC Arrays
BR931/D	Symbols to Silicon (C_LAN)
BR1400/D	Open Architecture CAD System — OACS 2.x
BR1417/D	Open Architecture CAD System — OACS 3.xM

Order Number	Description
Application Notes/Article Reprints	
AN1093/D	Delay and Timing Methods for CMOS ASICs
AN1095/D	Clock Distribution
AN1096/D	Guidelines for Using the Mustang™ ATPG System
AN1099/D	Test Methodology for HDC Series Arrays
AN1500	JTAG Boundary Scan for H4C/H4CPlus Arrays
AN1502/D	Embedded RAM/BIST
AN1508/D	High Frequency Design Techs & Guidelines for Bipolar Gate Arrays
AN1509/D	ASIC Clock Distribution Using PLL
AN1512/D	TestPAS Primer
AN1514/D	H4CPlus Series 3.3 V/5 V Design Considerations
AR518/D	Gate Arrays Simplify Translation between High Speed Logic Families
AR522/D	Ranking of Gate Array Vendors
AR524/D	ASIC Package Selection

ASIC Regional Design Centers — United States

California, San Jose
(408) 749–0510

Illinois, Chicago
(708) 490–9500

Massachusetts, Marlborough
(508) 481–8100

ASIC Regional Design Centers — International

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France, Velizy
(01) 34635900

Holland, Eindhoven
(04998) 61211

Hong Kong, Silicon Harbour, Tai Po
(852) 666–8333

Japan, Tokyo
(03) 440–3311

Sweden, Stockholm
(08) 734–8800

Italy, Milan
(02) 82201

Microcomputer Components

In Brief . . .

Motorola continues to be a leading supplier of components for microcomputer systems. The product portfolio includes digital signal processors; CISC and RISC and PowerPC advanced microprocessors and complementary full–function peripherals; a comprehensive selection of high–performance microcontrollers; VLSI functions for Local Operating Network applications; and a broad range of fast static RAM and dynamic RAM chips and modules.

Our commitment is to provide state–of–the–art devices as well as continuing support of established products, with six–sigma quality and total customer satisfaction.

Digital Signal Processors

In Brief . . .

Drawing on both design excellence and expertise in manufacturing, Motorola has created a range of architecturally compatible Digital Signal Processing chips. The philosophy behind the DSP families has been to create compatibility between products as well as conformance to international standards.

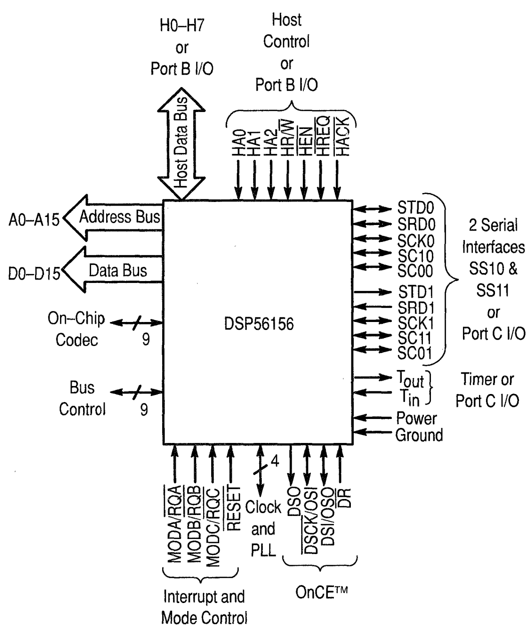
Motorola offers a complete portfolio of 16– and 24–bit fixed point and 32–bit floating point DSPs.

In addition, we offer a comprehensive array of development tools to give the designer access to the full power and versatility of the DSPs with minimum fuss. All the tools were designed for ease of use and functionality. They provide a low–cost means of evaluation and greatly simplify the design and development phase of a DSP project.

16–/24–/32–Bit Families —Your Complete DSP Solution

DSP56100 — 16–Bit Digital Signal Processors

The DSP56100 family of HCMOS, low–power, 16–bit fixed–point general–purpose digital signal processors (DSP) is ideal for high end speech coding, telecommunications and control applications. The first DSP56100 family member, the DSP56156, combines the high–speed core with 8K bytes RAM, two serial ports, one parallel port, codec, phase–locked loop (PLL) and On–Chip Emulation (OnCE™). The DSP56166, the second member of the DSP56100 family, has identical package and pinout to the DSP56156 with different memory configuration and peripherals.



PART NUMBERS

Part	Description
XC56156FV40	40 MHz in TQFP
XC56156FV50	50 MHz in TQFP
XC56156FE60	60 MHz in CQFP
XC56166FV60	60 MHz in TQFP

DSP56156 BENCHMARKS

Benchmark	Instruction Cycles
Real FIR Filter with Data Shift	1 per Tap
LMS Adaptive Real FIR Filter	2 per Tap
Double Integration Sinewave Generation	2 per Sample
Complex FIR Filter with Data Shift	4 per Tap
General Lattice Filter	4 per Tap
Real Cascaded IIR Biquad Filter Sections (4 coeff.)	5 per Section
PID Loop	5
Double Precision Multiply	6
[1×3][3×3] Matrix Multiplication	21

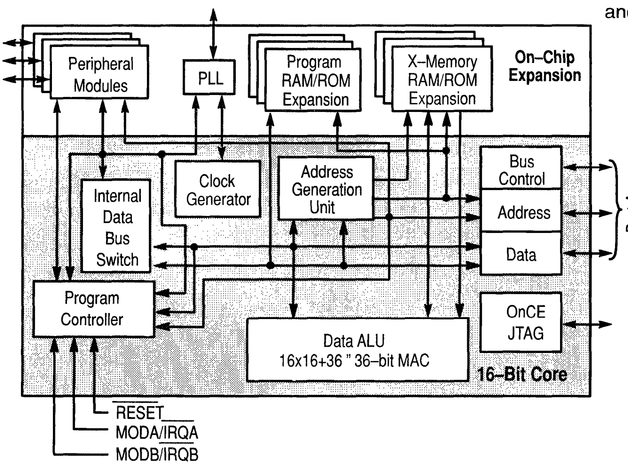
DSP56100 Features

- Up to 30 Million Instructions per Second (MIPS) at 60 MHz – 33.3 ns Instruction cycle
- Single–cycle 16 x 16–bit parallel Multiply–Accumulate
- 2 x 40–bit accumulators with extension byte
- Fractional and integer arithmetic with support for multiprecision arithmetic
- Highly parallel instruction set with unique DSP addressing modes
- Nested hardware DO loops including infinite loops and DO zero loop
- Two instruction LMS adaptive filter loop
- Fast auto–return interrupts
- Three external interrupt request pins
- Three 16–bit internal data and three 16–bit internal address buses
- Individual programmable wait states on the external bus for program, data, and peripheral memory spaces
- Off–chip memory–mapped peripheral space with programmable access time and separate peripheral enable pin
- On–chip memory–mapped peripheral registers
- Low Power Wait and Stop modes
- On–Chip Emulation(OnCE) for unobtrusive, processor speed independent debugging
- Operating frequency down to DC
- 5 V single power supply
- Low Power (HCMOS)

DSP56800 — 16–Bit Digital Signal Processors

The DSP56800 core family is the first architecture designed to enable digital signal processing and embedded microcontroller functionality. This multi–functional approach supports applications requiring both signal processing and control functionality, such as wireless messaging, digital answering machines, feature phones and low–cost wireline modems.

The first two DSP56800 family members, the DSP56L811 and DSP56L812 are identical except for memory configuration. The DSP56L811 contains 1K of program RAM and 2K of data RAM. The DSP56L812 features 22K of program ROM, 2K of data ROM and 2K of data RAM.



DSP56800 Features

- 20 MIPS at 40 MHz
- 3.3 Volts
- Three 16–bit Timers
- Two Serial Peripheral Interfaces (SPIs)
- Serial Synchronous Interface (SSI)
- JTAG OnCE™ Port
- Phase–Locked Loop
- 16 – 32 general purpose input/output pins. (16 dedicated and 16 shared with peripherals)
- External bus interface to allow for additional memory
- Support for high–level C and C++ programming languages
- Streamlined instruction set featuring frequently used DSP and microcontroller codes, as well as control extensions

PART NUMBERS (4Q '96 Availability)

Part	Description
XC56L811BU40	40 MHz in TQFP
XC56L812BU40	40 MHz in TQFP

DSP56000 — 24–Bit Digital Signal Processors

The DSP56000 Family of 24–bit, fixed–point, general–purpose digital signal processors is Motorola's original DSP family and has set the standard for high end DSP devices with its triple Harvard architecture of seven internal buses and three parallel execution units — Data ALU, Address Generation Unit, and Program Controller. Motorola has retained architectural compatibility with the 24–bit family into the 16–bit DSP56100 and 32–bit DSP96002 products helping to preserve our customer software investment.

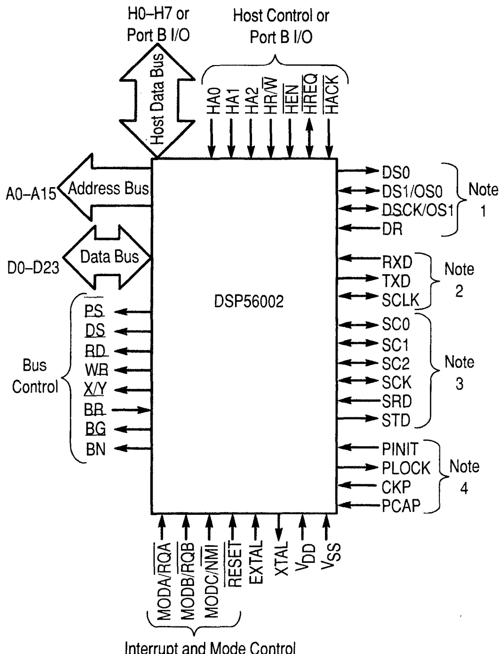
The DSP56000 Family of HCMOS, 24–bit DSP devices consists of the DSP56002, DSP56L002, DSP56004, DSP56005, DSP56007, DSP56L007, DSP56009 and the transitional DSP56001A. All these products are source code compatible and are used extensively in telecommunications, control and audio applications. The DSP56000 Family's unique 24–bit architecture has made these products the industry standard for CD–quality digital audio processing.

The DSP56L002 and DSP56L007 low–voltage devices operate at 3.3 volts which effectively extends the battery life of portable applications up to three times longer than 5 volt systems.

DSP56002 BENCHMARKS

Benchmark	Instruction Cycles
Real FIR Filter with Data Shift	1 per Tap
Two Dimensional Convolution (3×3 coeff. mask)	1 per Output
LMS Adaptive Real FIR Filter	3 per Tap
Real Cascaded IIR Biquad Filter Sections (4 coeff.)	4 per Section
Complex FIR Filter with Data Shift	4 per Tap
[1×3][3×3] Matrix Multiplication	17
Division	28
Leroux–Gueguen LPC Analysis: 8th Order 10th Order 16th Order	 473 622 1203

DSP56000 — 24–Bit Digital Signal Processors (continued)



NOTES:
1. On–Chip Emulator Port (OnCE™)
2. SCI Serial or Port C I/O
3. SSI Serial or Port C I/O
4. Phase–Locked Loop

DSP56000 Family Features

- On–chip Harvard architecture permitting simultaneous accesses to program and two data memories
- Two 56–bit accumulators including extension byte
- Parallel 24 x 24–bit multiply–accumulate in 1 instruction cycle (2 clock cycles)
- Double precision 48 x 48–bit multiply with 96–bit result in 6 instruction cycles
- 56–bit addition/subtraction in 1 instruction cycle
- Fractional arithmetic with support for multiprecision arithmetic
- Hardware support for block–floating point FFT
- Hardware nested DO loops
- Zero–overhead fast interrupts (2 instruction cycles)
- On–Chip Emulation (OnCE) port for unobtrusive, processor speed–independent debugging
- Software–programmable, Phase–Locked Loop (PLL) based frequency synthesizer for the core clock
- On–chip peripheral registers memory mapped in data memory space
- Double buffered peripherals
- Power–saving Wait and Stop modes

DSP56002 Features

- 512 x 24–bit on–chip program RAM and 64 x 24–bit bootstrap ROM
- Two 256 x 24–bit on–chip data RAMs
- Two 256 x 24–bit on–chip data ROMs containing sine, A–law, and μ–law tables
- External memory expansion with 16–bit address and 24–bit data buses
- Bootstrap loading from external data bus, Host Interface, or Serial Communications Interface
- Byte–wide Host Interface (HI) with Direct Memory Access (DMA) support
- Synchronous Serial Interface (SSI) to communicate with codecs and synchronous serial devices
  — 8–, 12–, 16–, 24–bit word sizes
  — Up to 32 software–selectable time slots in network mode
  — Serial Communication Interface (SCI) for full–duplex asynchronous communications
  — 24–bit Timer/Event Counter also generates and measures digital waveforms
  — Up to 25 general–purpose I/O (GPIO) pins
  — Three external interrupt request pins; one non–maskable
  — 3.3 V (DSP56L002) and 5 V (DSP56002) power supply options

DSP56004/DSP56007 Features

- Serial Audio Interface (SAI) includes 2 receivers and 3 transmitters, master or slave capability, and implementation of I²S, Sony, and Matshushita audio protocols; two sets of SAI interrupt vectors
- Serial Host Interface (SHI) features single master capability, 10–word receive FIFO, and support for 8–, 16–, and 24–bit words
- External Memory Interface (EMI) peripheral providing glueless connection to DRAM, SRAM, and/or EPROM for audio delay buffering
- Four dedicated, independent, programmable General Purpose I/O (GPIO) lines
- DSP56004 memory: 512 words PRAM, 2 x 256 words data RAM, 2 x 256 words data ROM
- DSP56007 memory: 6400 words PROM, 3200 words data RAM, 1024 words data ROM
- 3.3 V power supply option available (DSP56L007)
- Bootstrap loading via I²C, SPI, or byte–wide memory modes available
- Up to 25 general–purpose I/O (GPIO) pins

DSP56000 — 24–Bit Digital Signal Processors (continued)

DSP56005 Features

- Five Pulse Width Modulators (PWM)
- 24–bit timer/event counter also generates and measures digital waveforms
  - Three with alternate outputs; two with open drain or TTL outputs
  - 9–bit to 16–bit data width
  - Alternate outputs independently selectable as active high or active low
- 16–bit Watchdog timer
- 4608 x 24–bit on–chip program RAM and 96 x 24–bit bootstrap ROM
- Two 256 x 24–bit on–chip data RAMs
- Two 256 x 24–bit on–chip data ROMs containing sine and arc–tangent tables
- External memory expansion with 16–bit address and 24–bit data buses
- Bootstrap loading from external data bus, Host Interface, or Serial Communications Interface

DSP56009 Features

The memory configurations available differentiate this DSP from the other family members. The DSP core is fed by a large program ROM, two independent data RAMs, two data ROMs, a Serial Audio Interface, Serial Host Interface, External Memory Interface, dedicated I/O lines, on–chip Phase–Locked Loop (PLL), and On–Chip Emulation (OnCE™) port.

- Completely pin compatible with DSP56004 and DSP56007 for easy upgrades
- 5 V power supply
- On–chip Harvard architecture permitting simultaneous accesses to program and two data memories
- 10240 x 24–bit on–chip program ROM*
- 4608 x 24–bit on–chip X–data RAM and 3072 x 24–bit on–chip X–data ROM*
- 4352 x 24–bit on–chip Y–data RAM and 1792 x 24–bit on–chip Y–data ROM*
- 512 x 24–bit on–chip program RAM and 64 x 24–bit bootstrap ROM
- Up to 2304 x 24–bit from X and Y data RAM can be switched to program RAM giving a total of 2816 x 24–bits of program RAM
- Bootstrap loading from Serial Host Interface or External Memory Interface

*These ROMs may be factory programmed with data/program provided by the application developer.

PART NUMBERS

Part	Description
XC56001ARC27	Transitional Device. DSP56002 recommended for new designs
XC56001ARC33	Transitional Device. DSP56002 recommended for new designs
XC56001AFE27	Transitional Device. DSP56002 recommended for new designs
XC56001AFE33	Transitional Device. DSP56002 recommended for new designs
XC56001AFC27	Transitional Device. DSP56002 recommended for new designs
XC56001AFC33	Transitional Device. DSP56002 recommended for new designs
DSP56002RC40	40 MHz RAM–based in 132–pin PGA
DSP56002FC40	40 MHz RAM–based in 132–pin PQFP
DSP56002FC66	66 MHz RAM–based in 132–pin PQFP
XC56002PV40	40 MHz RAM–based in 144–pin TQFP
XC56002PV66	66 MHz RAM–based in 144–pin TQFP
XCP56002PV80	80 MHz RAM–based in 144–pin TQFP
DSP56L002FC40	Low power 40 MHz RAM–based in 132–pin PQFP
XC56L002PV40	Low power 40 MHz RAM–based in 144–pin TQFP
XC56004FJ50	50 MHz RAM–based in 80–pin QFP
XC56004FJ66	66 MHz RAM–based in 80–pin QFP
XC56005PV50	50 MHz RAM–based in 144–pin TQFP
XC56007FJ50	50 MHz ROM–based in 80–pin QFP
XC56007FJ66	66 MHz ROM–based in 80–pin QFP
XC56L007FJ40	Low–power 40 MHz ROM–based in 80–pin QFP
XC56009PV80	80 MHz ROM–based in 80–pin QFP

DSP56300 — 24–Bit Digital Signal Processors

The first programmable Motorola DSP product to provide a true single clock–cycle execution, the DSP56300 core effectively doubles the number of instructions executed without increasing clock speed, providing 80 MIPS of performance at 80 MHz while retaining code compatibility with the rest of the Motorola DSP offerings. The DSP56300 family offers a new level of performance in MIPS, a rich instruction set and low power dissipation, enabling a new generation of products in wireless, telecommunications, and multimedia.

Several significant architectural enhancements include a barrel shifter, 24–bit addressing, instruction cache and DMA functionality. The DSP56301 offers 66/80 MIPS using an internal 66/80 MHz clock at 3.0 – 3.6 V.

DSP56301 Features

- 66/80 MIPS with a 66/80 MHz internal clock at 3.0 – 3.6 volts
- Single clock per instruction execution
- Code compatible with the DSP56000 family

- Fully–static logic with operation to DC
- Wait, stop and intelligent power control circuitry powers down unused memories, peripherals and core logic on each individual instruction

DSP56300 — 24–Bit Digital Signal Processors (continued)

- OnCE with added JTAG support for system debugging and testing
- On–chip PLL
- ALU Enhancements over DSP56000
  - — Fully pipelined barrel shifter supports bit stream parsing and generation
  - — Conditional ALU instruction
  - — 16–bit arithmetic supports cellular and videotelephony standards
- Address Generation Unit Enhancements over DSP56000
  - — 24–bit addressing provides 16M word addressing for Program, X and Y memories
  - — Program Counter relative addressing improves operating system and compiler efficiency
  - — Immediate offset addressing
- Program Controller Enhancements over DSP56000
  - — Hard stack extension in data memory allows unlimited stack depth without programmer overhead
  - — Support for instruction code
- Direct Memory Access Unit
  - — 6 channel fully concurrent DMA supports 120 Mbytes/sec transfers at 80 MHz
  - — Dedicated address and data buses support concurrent memory accesses
  - — Supports peripheral interrupts, internal and external memory reads/writes

DSP56301 Peripherals/External Buses

- Modular peripheral and memory design
- Glueless interface to PCI, ISA, and other DSP56301 buses
- One Serial Communication Interface module
- Two Enhanced Serial Synchronous Interface modules
- Three independent Timer modules
- Glueless interface to SRAM, Synchronous SRAM, DRAM and memory mapped peripherals
- Off–chip expansion to 224 words for program, X, and Y memory

DSP56301 On–Chip Memories

- On–chip 2048 x 24–bit X data RAM
- On–chip 2048 x 24–bit Y data RAM
- On–chip 3072 x 24–bit Program RAM
- On–chip 1024 x 24–bit Instruction Cache/Program RAM
- On–chip 192 x 24 bit Bootstrap ROM

DSP56302 Features

- 8–bit parallel host port
- 34K words on–chip RAM
- 144–pin QFP

DSP56303 Features

- Cost effective version of 56301
- 8–bit parallel host port
- 144–pin QFP

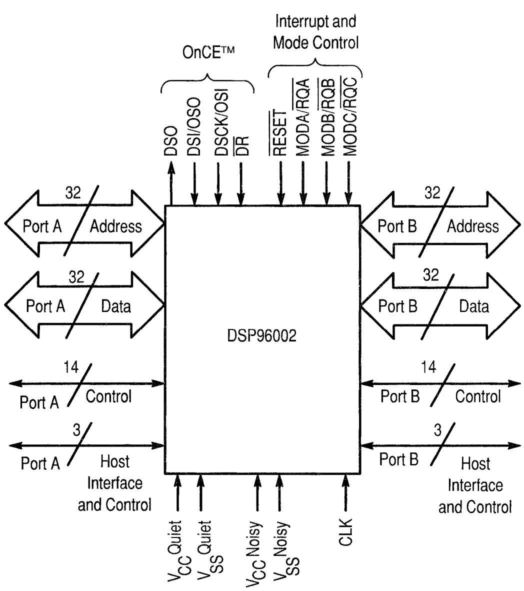
PART NUMBERS

Part	Description
XC56301PW66	66 MHz in 208 TQFP
XC56302PV60	60 MHz in 144–pin QFP
XC56303PV66	66 MHz in 144–pin QFP

DSP96002 — 32–Bit Digital Signal Processors

The DSP96002 has full architecture compatibility with the 16–bit DSP56100 and 24–bit DSP56000 Families. The DSP96002 is the first in a family of 32–bit IEEE floating–point DSP devices. The DSP96002 has two identical memory expansion ports simplifying network configurations for multiprocessor and DSP96002 communications. These ports interface to SRAM, DRAM (operating in their fast access modes), video RAM or directly to other processors with host interface logic.

Although designed primarily for image processing, other proven applications include communications, spectrum analysis, instrumentation, speech processing and pattern recognition.



PART NUMBERS

Part	Description
XC96002RC33	33 MHz in PGA
XC96002RC40	40 MHz in PGA

DSP96002 BENCHMARKS

Benchmark	Instruction Cycles
Real	
FIR Filter with Data Shift	1 per Tap
V = V*S + V	2
Lattice Filter with Data Shift	3 per Tap
Cascaded IIR Biquad Filter Sections (4 coeff.)	4 per Section
1024–point FFT and bit reversal	12880
Complex	
V = V*V + V	4
FIR Filter with Data Shift	4 per Tap
1024–point FFT and bit reversal	20931
Graphics/Image Processing	
Divide (32–bit accuracy)	7
Square Root (32–bit accuracy)	12
Bezier Cubic Evaluation for Font Compilation	13
[4×4][4×4] = [4×4]	67

DSP96002 Features

- DSP96000 family architecture
  - — Full IEEE Standard 754 compatible for 32–bit (SP) and 44–bit (SEP) arithmetic
  - — 20 MIPS, 50 ns instruction cycle at 40 MHz
  - — 60 million floating–point operations per second (MFLOPS) at 40 MHz
  - — Single cycle 32 x 32 → 96–bit multiply/accumulate
  - — Ten 96–bit general–purpose data registers
  - — Zero–overhead nested DO loops
  - — Two instruction–cycle fast interrupts
  - — Low–power Wait and Stop Modes
  - — On–Chip Emulation for unobtrusive, full–speed debugging
  - — 4K byte instruction cache
  - — Integer mode available
  - — Single precision mode available
  - — Timer/Event Counter
- DSP96002 peripherals
  - — Two 32–bit address and data host ports
  - — Dual channel DMA controller
- DSP96002 memories
  - — 1024 x 32 program RAM
  - — 2 x 512 x 32 data RAM
  - — 2 x 512 x 32 data ROM (sine and cosine tables)

DSP56ADC16 — The Analog–To–Digital Converter

The DSP56ADC16 is a single–chip, linear analog–to–digital (A/D) converter. It is an ideal choice for high–performance digital audio systems, voice–bandwidth communication and control applications. It does not require antialiasing filters and sample–and–hold circuitry because they are an inherent part of the sigma–delta technology. The DSP56ADC16 can be easily interfaced to the DSP56001 and other host processors using its flexible serial interface.

Key Features

- 16–bit output resolution at 100 kHz from FIR filter
- 12–bit output resolution at 400 kHz from Comb filter
- 96–dB dynamic range
- 90–dB signal–to–THD ratio
- 90–dB signal–to–noise ratio
- In–band ripple: <0.001 dB
- Maximum output sample rates:
  - — FIR filter — 100 kHz
  - — Comb filter — 400 kHz
- Maximum input sample rate is 6.4 MHz
- Maximum internal clock rate is 12.8 MHz
- DC stability is 10–bits
- Supply voltage is single +5V (±10%)
- Supply current is <100 mA
- Linear–phase analog front end and internal digital filters
- Simple serial interface to host microprocessors
- Fully differential inputs

PART NUMBERS

Part	Description
DSP56ADC16S	16–bit in Ceramic DIP

DSP Development Tools

Application Development Systems

Every member of the Motorola Family of 16–, 24– and 32–bit DSPs is supported by a multi–component Application Development System (ADS) which acts as a tool for designing, debugging and evaluating real–time DSP target system equipment. The ADS simplifies evaluation of the user's prototype hardware/software product by making all of the essential timing and I/O circuitry easily accessible. Using an IBM PC™, Macintosh™ II, a Sun–4™, or Hewlett–Packard Series 700 as a medium between the user and the DSP hardware significantly reduces the overall complexity and cost of development while increasing the capabilities of the system. With the ADS, DSP programs can be executed in real–time, single instruction traced or multiple instruction stepped with registers and/or memory block contents displayed. The ADS is fully compatible with the CLAS design–in software package for each product and may act as an accelerator for testing DSP algorithms.

All Application Development Systems offer an On–Chip Emulation (OnCE™) circuit for unobtrusive, processor speed independent debugging. The ADS takes full advantage of this circuit to allow the user non–intrusive control of the target.

General ADS Features

Software —

- Single/multiple stepping through DSP object programs
- Conditional/unconditional software and hardware breakpoints
- Program patching using a single–line assembler/disassembler
- Session and/or command logging for later reference
- Loading and saving of files to/from ADM memory
- Macro command definition and execution
- Display enable/disable of registers and memory
- Debug commands which support multiple DSP development
- Hexadecimal/decimal/binary calculator
- Multiple input/output file access from DSP object programs
- On–line help screens for each command and register

Hardware —

- Full speed operation
- Multiple ADM support with programmable ADM addressing
- Stand–alone operation of ADM after initial development

DSP56156ADS Features

- System commands from within ADS user interface program
- 16K words of configurable static RAM expandable to 64K words

DSP56002ADS Features

- Host operating system commands from within ADS user interface program
- 8K/32K words of configurable RAM for DSP56002 code development
- 96–pin euro–card connector for accessing all DSP56000/1 pins
- 1K words of monitor ROM expandable to 4K words
- Separate connectors for accessing serial or host/DMA ports

DSP96000ADS Features

- System commands from within ADS user interface program
- 128K words of configurable static RAM expandable to 512K words
- 2K words of EPROM with sockets expandable to 64K words
- Full support of multiple data memory maps

- Two sets of 96–pin connectors provide access to all DSP96002 pins
- 2K words of EPROM with sockets expandable to 16K words

DSP Development Tools (continued)

PART NUMBERS

Development Systems	Host Machine
DSP56100ADSA *	IBM PC
DSP56100ADSB	Macintosh II
DSP56100ADSF *	Sun–4
DSP56100ADSH *	Hewlett–Packard Series 700
DSP96000ADSA *	IBM PC
DSP96000ADSB	Macintosh II
DSP96000ADSF *	Sun–4
DSP96000ADSH *	Hewlett–Packard Series 700
DSP56002ADSA *	IBM PC
DSP56002ADSB	Macintosh II
DSP56002ADSF *	Sun–4
DSP56002ADSH *	Hewlett–Packard Series 700
DSP56004ADSA *	IBM PC
DSP56004ADSB	Macintosh II
DSP56004ADSF *	Sun–4
DSP56004ADSH *	Hewlett–Packard Series 700
DSP56005ADSA *	IBM PC
DSP56005ADSB	Macintosh II
DSP56005ADSF *	Sun–4
DSP56005ADSH *	Hewlett–Packard Series 700
DSP56005ADPTR	Adapter Board
DSP56301ADSA *	IBM PC
DSP56301ADSF *	Sun–4
DSP56301ADSH *	Hewlett–Packard Series 700
DSP56002ADM	ADM Board for 56002
DSP56004ADM	ADM Board for 56004
DSP56156ADM	ADM Board for 56156
DSP56166ADM	ADM Board for 56166
DSP96000ADM	ADM Board for 96000
DSPPCHOST *	PC compatible host board and interface software
DSPMACHOST	Macintosh II host board and interface software
DSPSUN4HOST *	Sun–4 host board and interface software
DSPCOMMAND	16–, 24–, 32–bit Command Converter board and software
DSP56002EVM	Evaluation board and software for DSP56002
DSP56007EVM	Evaluation board and software for DSP56007
DSP56009EVM	Evaluation board and software for DSP56009

— *Supported by Graphical User Interface

Graphical User Interface

For DSP Application Development Systems and Simulators

A number of Motorola's DSP development systems and simulators come with graphical user interface software to ease working on applications based on our product families.

User Friendly

- GUI works native to three operation systems
  - — SunOS
  - — Windows 3.1
  - — HPUX
- Multiple overlapping windows for the display of debugging information, command input registers, memory, and programs
- Pull down menus for ease of use
  - — Dialog boxes for selecting options of complex commands
  - — Tool bar will provide fast access to commonly performed actions
  - — Keyboard accelerators will be defined for commonly executed commands
  - — Help viewer will be provided for viewing pre–defined help on selected topics

Debugging Capabilities for C Language and Assembly

- Assembly language symbolic or C Language source code debugging capabilities

DSP Development Software

Design–In Software Packages

The Simulator/Macro–Assembler/Linker/Librarian software package is a development system support tool. The Simulator program imitates the operation of the DSP on a clock–cycle by clock–cycle basis and gives an accurate measurement of code execution time. All on–chip peripheral operations, memory and register updates and exception processing activities may be functionally simulated.

The full–featured Macro Cross Assembler translates one or more source files containing instruction mnemonics, operands, and assembler directives into a Common Object File Format (COFF) file which is directly loadable by the Simulator. It supports the full instruction set, memory spaces, and parallel transfer fields of the DSP.

The Linker relocates and links relocatable COFF object modules from the Assembler to create an absolute load file which can be loaded directly into the Simulator. The Librarian utility will merge separate, relocatable object modules into a single file allowing frequently used modules to be grouped for convenient linking and storing.

The assembler and linker now provide support for assembly language source–level debugging via the simulator. Global symbols, symbols local to sections, and even underscore labels may be referenced with all scoping constructs intact. In addition, the assembler generates information about included files and macros. The assembler and linker also support numbered counters ranging from 0 to 65535.

PART NUMBERS

Simulator/Assembler/ Linker/Library	Host Machine
DSP56100CLASA *	IBM PC
DSP56100CLASB	Macintosh II (consult factory)
DSP56100CLASF *	Sun–4
DSP56100CLASH *	Hewlett–Packard Series 700
DSP56000CLASA *	IBM PC
DSP56000CLASB	Macintosh II (consult factory)
DSP56000CLASF *	Sun–4
DSP56000CLASH *	Hewlett–Packard Series 700
DSP56300CLASA *	IBM PC
DSP56300CLASF *	Sun–4
DSP56300CLASH *	Hewlett–Packard Series 700
DSP96000CLASA *	IBM PC
DSP96000CLASB	Macintosh II (consult factory)
DSP96000CLASF *	Sun–4
DSP96000CLASH *	Hewlett–Packard Series 700

— *Supported by Graphical User Interface

C–Compiler Packages

A full ANSI C compliant compiler, based on GNU technology, provides higher efficiency and implements more than 20 major optimization techniques. It has improved in–line assembly capability and an ANSI C preprocessor. The package includes the C Compiler, a new COFF Assembler, Linker, complete ANSI C Libraries, and a new C source level debugger as well as expanded user's reference manual. The software package is available for various host computers listed.

PART NUMBERS

GNU C Compiler	Host Machine
DSP56100 Family	
DSP561CCCA	IBM PC
DSP561CCCF	Sun–4
DSP561CCCH	Hewlett–Packard Series 700
DSP56000 Family	
DSP56KCCA	IBM PC
DSP56KCCF	Sun–4
DSP56KCCH	Hewlett–Packard Series 700
DSP53000 Family	
DSP563CCA	IBM PC
DSP563CCF	Sun–4
DSP563CCH	Hewlett–Packard Series 700
DSP96000 Family	
DSP96KCCA	IBM PC
DSP96KCCF	Sun–4
DSP96KCCH	Hewlett–Packard Series 700

C–Compiler Upgrades

Registered users of the earlier versions of the Motorola DSP C compiler can upgrade to the latest GNU C compiler for $120. To order, contact a Motorola sales representative or distributor. Have your registration number ready.

PART NUMBERS

GNU C Compiler	Host Machine
DSP56000 Family	
DSP56KCCAJ	IBM PC
DSP56KCCFJ	Sun–4

The M68000 Family

. . . the Upward Compatible 8–/16–/32–Bit Microprocessor Family

In Brief . . .

An MPU For All Functions

To designers of the most advanced microcomputer systems, the Motorola M68000 Family of microprocessors needs no introduction. Products based on its members have become the standard for systems utilizing the UNIX operating system and for CAD/CAM engineering workstations. They are invading the next generation designs of personal computers and color graphics systems, and they find widespread implementation in multi–user/multi–tasking applications and in small business systems. M68000 MPUs are found in the leading products in fault–tolerant systems requiring high performance and parallel processing, and they are the preferred components for artificial intelligence engines requiring large linear addressing capabilities. Control applications include graphics, numerical controllers, robotics, telecommunications switching and PBX voice/data transmission.

Upward Compatibility

The M68000 MPU Family consists of a line of processors based on a 32–bit flexible register set, a large linear address space, a simple yet powerful instruction set and flexible addressing modes. The internal architecture of the 8–, 16–, and 32–bit MPU versions, and the common instruction set, provide software compatibility and offer an easy upward migration path for products requiring increasing levels of processing power.

A Host of Peripherals

A large selection of full–function peripheral chips complements the processor family. Compatible LSI and VLSI chips for memory management, data communications, DMA control, network control, system interfacing, general I/O and graphics, all simplify system design and reduce design and manufacturing cost while improving system performance.

Microprocessors

The 68K Family of Microprocessors has revolutionized virtually every segment of the electronic industry. They have set the standard for performance while still maintaining binary software compatibility from generation to generation. The combination of low cost and high performance (measured in $/system MIPS) makes every member of the Family a price performance leader. The M68000 Family provides the widest range of price and performance with choices from 1.6 MIPS to over 100 MIPS.

Table 1.

	68000	68020	68030	68040	68060
MIPS	1.6	5.5	12	35	100
MFLOPS	–	0.25	0.5	3.5	15
Address Range	16M Byte	4G Byte	4G Byte	4G Byte	4G Byte
Data Bus	16 bit	32 bit	32 bit	32 bit	32 bit
Clock Speed (MHz)	8–16	16–33	16–50	25–40	50–66
Instruction Cache	–	256 Byte	256 Byte	4K Byte	8K
Data Cache	–	–	256 Byte	4K Byte	8K
Burst Mode	–	–	16 Byte R	16 Byte R/W	16 Byte R/W
General Purpose Registers	16	16	16	16	16
Address Modes	14	18	18	18	18
On–Chip MMU	No	No	Yes	Yes*	Yes*
Floating–Point Solution	68881	68882	68882	On–Chip	On–Chip

*Separate Instruction/Data

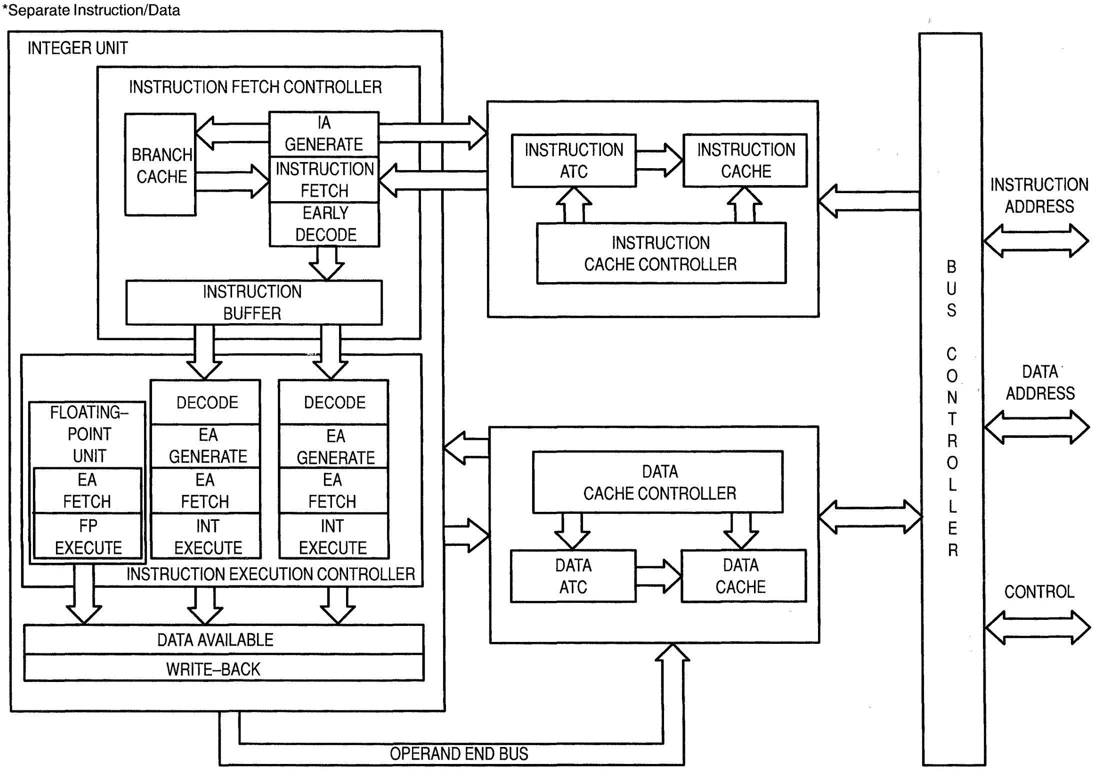


Figure 1. MC68060 Block Diagram

MC68060
Superscalar 32–Bit Microprocessor

The MC68060 is fully compatible with all previous members of the M68000 family. The MC68060 features dual on–chip caches, fully independent demand–paged memory management units (MMUs) for both instructions and data, dual integer execution pipelines, on–chip floating–point unit (FPU) and a branch target cache. A high degree of instruction execution parallelism is achieved through the use of a full internal Harvard architecture, multiple internal buses, independent execution units, and dual instruction issue within the instruction controller. Power management is also a key part of the MC68060 architecture. The MC68060 offers a low–power mode of operation that is accessed through the LPSTOP instruction, allowing for full power–down capability. The MC68060 design is fully static so that when circuits are not in use, they do not draw power. Each unit can be disabled so that power is used only when the unit is enabled and executing an instruction.

Complete code compatibility with the M68000 family allows the designer to draw on existing code and past experience to bring products to market quickly. There is also a broad base of established development tools, including real–time kernels, operating systems, languages and applications, to assist in product design. The functionality provided by the MC68060 makes it the ideal choice for a range of high–performance computing applications as well as many portable applications that require low power and high performance.

MC68040
Third–Generation 32–Bit Microprocessor

The MC68040 is Motorola's third generation of M68000–compatible, high–performance, 32–bit microprocessors. The MC68040 is a virtual memory microprocessor employing multiple, concurrent execution units and a highly integrated architecture to provide very high performance in a monolithic HCMOS device. On a single chip, the MC68040 integrates an MC68030–compatible integer unit, an IEEE 754–compatible floating–point unit (FPU), and fully independent instruction and data demand–paged memory management units (MMUs), including independent 4K–byte instruction and data caches. A high degree of instruction execution parallelism is achieved through the use of multiple independent execution pipelines, multiple internal buses, and a full internal Harvard architecture, including separate physical caches for both instruction and data accesses. The MC68040 also directly supports cache coherency in multimaster applications with dedicated on–chip bus snooping logic.

The MC68040 is an enhanced, 32–bit, HCMOS microprocessor that combines the integer unit processing capabilities of the MC68030 microprocessor with independent 4K–byte data and instruction caches and an on–chip FPU. The MC68040 maintains the 32–bit registers available with the entire M68000 Family as well as the 32–bit address and data paths, rich instruction set, and versatile addressing modes. Instruction execution proceeds in parallel with accesses to the internal caches, MMU operations, and bus controller activity. Additionally, the integer unit is optimized for high–level language environments. The MC68040 is user–object–code compatible with previous members of the M68000 Family and is specifically optimized to reduce the execution time of compiler–generated code. The MC68040 is implemented in Motorola's latest HCMOS technology, providing an ideal balance between speed, power, and physical device size.

Instruction execution is pipelined in both the integer unit and FPU. Independent data and instruction MMUs control the main caches and the address translation caches (ATCs). The ATCs speed up logical–to–physical address translations by storing recently used translations. The bus snooper circuit ensures cache coherency in multimaster and multiprocessing applications. The MC68040 FPU is user–object–code compatible with the MC68882 floating–point coprocessor. The FPU has been optimized to execute the most commonly used subset of the MC68882 instruction set, and includes additional instruction formats for single– and double–precision rounding of results.

The MMUs support multiprocessing, virtual memory systems by translating logical addresses to physical addresses using translation tables stored in memory. Each MMU has two transparent translation registers available that define a one–to–one mapping for address space segments ranging in size from 16 Mbytes to 4 Gbytes each. The instruction and data caches operate independently from the rest of the machine, storing information for fast access by the execution units. Each cache resides on its own internal address bus and internal data bus, allowing simultaneous access to both. The data cache provides writethrough or copyback write modes that can be configured on a page–by–page basis.

The MC68040 bus controller supports a high–speed, nonmultiplexed, synchronous external bus interface, which allows the following transfer sizes: byte, word (2 bytes), long word (4 bytes), and line (16 bytes). Line accesses are performed using burst transfers for both reads and writes to provide high data transfer rates.

MC68030
The Second Generation 32–Bit MPU

The 030 started with a high performance 020 core and added many performance improvement features including increased internal parallelism, dual on–chip caches with a burst fillable mode, dual internal data and address buses, improved bus interface, and on–chip paged memory management unit.

Two independent 32–bit address buses and two 32–bit data buses allow the CPU, caches, MMU, and the bus controller to operate in parallel, so the 030 can, for example, simultaneously access an instruction from the instruction cache, data from the data cache and instruction/data from external memory.

Performance is further enhanced by on–chip instruction and data caches. Separate 256–byte data and instruction caches reduce the access time and increase CPU throughput by providing data and instructions on–chip.

Overall bus requirements are reduced and multiple processors can run more efficiently thanks to increased bandwidth of the 030 bus, achieved by the enhanced bus controller allowing high speed fills of both data and instruction caches.

The on–chip paged memory management unit translates logical address to the corresponding physical address in 1/2 the time required by the 020 and MC68851 Paged Memory Management Unit. Pipelining permits this translation to be performed in parallel with other functions so that no translation time is added to any bus cycle.

MC68020

The Original 32–Bit Performance Standard

The MC68020, oh twenty, is the industry's leading 32–bit microprocessor because of high performance, architecture, ease of design–in, and long–range compatible growth path.

The 020 has a full 32–bit internal and 32–bit external, regular, symmetrical architecture designed with the customer in mind. It offers all the functionality of the other M68000 Family MPUs, and maintains software user–code compatibility which controls the expense of your product migration.

Programmers appreciate the large general purpose register set, simple yet powerful instruction set and the many flexible M68000 addressing modes. The unique on–chip instruction cache helps provide burst–mode operation to 12.5 MIPS.

The 020 is the proven leader in high performance systems in office automation, engineering workstations, fault tolerant computers, parallel processors, telephone switching systems, and intelligent controllers.

MC68010

A Virtual Memory Enhancement

The MC68010 offers the advantage of Virtual Memory. A high–speed loop mode operation executes tight software loops faster to enhance performance. Its instruction continuation feature has made it the choice for fault–tolerant and parallel processing systems. The MC68010 can support a governing operating system which handles the supervisory chores of any number of subordinate operating systems.

MC68HC000

A Micropower Alternative

HCMOS design gives the MC68HC000 all the functions and performance of its MC68000 predecessors . . . at one–tenth of the operating power requirements. With a maximum power dissipation of only 0.175 watts, the MC68HC000 is ideal for high–performance computer peripherals, industrial controllers, instrumentation and communications equipment.

MC68HC001

Low Power HCMOS 8–/16–/32–Bit Microprocessor

The MC68HC001 provides a functional extension of the MC68HC000 HCMOS 16–/32–bit microprocessor with the addition of statically selectable 8– or 16–bit data bus operation. The MC68HC001 is object–code compatible with the MC68HC000, and code written for the MC68HC001 can be migrated without modification to any member of the M68000 Family. This is possible because the user programming model is identical for all members of the M68000 Family and the instruction sets are proper subsets for the complete architecture.

MC68000

The 16–Bit Foundations

As the first member of the M68000 family, the state–of–the–art technology and advance circuit design concepts of the MC68000 16–bit MPU started a new trend in microprocessor architecture. Its seventeen 32–bit data and address registers permit rapid internal execution of its powerful yet simple instruction set. It is designed for large multiprocessing systems and realtime applications with vectored interrupts, seven priority levels and a 16 megabyte linear addressing space. It offers mainframe–like performance, supporting high–level languages and sophisticated operating systems.

The MC68000 MPU has been joined by more advanced products with even greater capabilities, yet it satisfies a large segment of the existing applications. It is extremely cost competitive and it remains one of the major growth products in the entire MPU line.

MC68008

An 8–Bit Compatible Competitor

With an 8–bit data bus and 32–bit internal architecture, the MC68008 offers performance that competes with a number of 16–bit MPUs. It has the same register set, same instructions, and the same functionality as the MC68000 with extensive exception processing. Large modular programs can be developed and executed efficiently because of the large, 1–megabit non–segmented, linear address space. It is the choice for high performance, cost effective, 8–bit designs, particularly those requiring a migration path to 16–bit or full 32–bit operation.

Embedded Controllers

The principle elements of this popular microprocessor family have now been redesigned specifically for embedded applications. The new 68EC0x0 family including the 68EC000, EC020, EC030 and EC040 MPUs are all optimized for cost–sensitive embedded control designs. The 68EC0x0 family offers the high performance of the 680x0 family, yet streamlines the feature sets for embedded applications. The 68EC0x0 family completes the triad forming the M68000 family of compatible products: the 680x0 family of computer–class central processing units; the 68300 family of integrated processors; and now, the 68EC0x0 family of embedded microprocessors.

Table 2.

	68EC000	68EC020	68EC030	68EC040
MIPS	2.5	6.5	10.7	29
Address Range	16M Byte	16M Byte	4G Byte	4G Byte
Data Bus	16 bit	32 bit	32 bit	32 bit
Clock Speeds	8, 10, 12, 16 MHz	16, 25 MHz	25, 40 MHz	20, 25, 33* MHz
Instruction Cache	–	256 Byte	256 Byte	4K Byte
Data Cache	–	–	256 Byte	4K Byte
Burst Fill Caches	–	–	16 Bytes	16 Bytes
General Purpose Registers	16	16	16	16
Address Modes	14	18	18	18
Floating Point Hardware	68881/68882	68881/68882	68881/68882	68040
Packages	PLCC	PPGA, PQFP	PPGA, CQFP	PGA, CQFP*

* Available in the future

MC68EC040

32–Bit High–Performance Embedded Controller

The 68EC040 is the newest addition to Motorola's embedded microprocessor family. It is the performance leader for top–of–the–line embedded applications. The EC040 is capable of delivering 29 MIPS of sustained performance at 1.2 cycles per instruction with a system cost that is unattainable by competing architectures.

This impressive performance is a result of a six–level pipelined integer unit, independent four–way set–associative instruction and data caches, and a very high level of on–chip parallelism. The EC040 also supports multimaster and multiprocessor systems with bus snooping.

By integrating all these features into the EC040, the microprocessor is able to perform the vast majority of work on–chip, limiting external memory accesses to allow for higher system performance with less expensive DRAMs. The result is virtual immunity to the effects of memory wait states.

MC68EC030

32–Bit Enhanced Embedded Controller

The MC68EC030 is a 32–bit embedded controller that streamlines the functionality of an MC68030 for the requirements of embedded control applications. The MC68EC030 is optimized to maintain performance while using cost–effective memory subsystems. The rich instruction set and addressing mode capabilities of the MC68020, MC68030, and MC68040 have been maintained, allowing a clear migration path for M68000 systems. The MC68EC030 is object–code compatible with the MC68020, MC68030, and earlier M68000 microprocessors. Burst–mode bus interface is provided for efficient DRAM access.

The MC68EC030 has an on–chip data cache and on–chip instruction cache with 256 bytes each. Dynamic bus sizing is available for direct interfacing to 8–, 16–, and 32–Bit Devices. The MC68EC030 includes 32–bit nonmultiplexed address and data buses, sixteen 32–bit general–purpose data and address registers, and two 32–bit supervisor stack pointers and eight special–purpose control registers. The EC030 provides complete support for coprocessors with the M68000 coprocessor interface. There are two access control registers that allow blocks to be defined for cacheability protection. The pipelined architecture, along with increased parallelism, allows internal caches accesses in parallel with bus transfers and overlapped instruction execution. The enhanced bus controller supports asynchronous bus cycles (three clocks minimum), synchronous bus cycles (two clocks minimum), and burst data transfers (one clock).

MC68EC020

32–Bit Embedded Controller

The 68EC020, with a complete 32–bit internal implementation, has a 32–bit data bus and an on–chip instruction cache to provide dramatically increased performance over 8– and 16–bit microprocessors. In addition, upward migration to the EC020 is made simple with dynamic bus sizing, allowing 8, 16 and 32–bit peripherals to communicate with the microprocessor.

Other performance features include advanced bit manipulation capabilities that provide multiple bit shift operations in a single instruction cycle. This capability greatly simplifies and accelerates the bit operations required in graphics processing and optical recognition applications.

MC68EC000

Low–Powered HCMOS Embedded Controller

The 68EC000 is a low–power HCMOS derivative of the 68000 optimized for cost–effective embedded processing. The EC000 has a flexible data bus that can operate in either 8– or 16–bit modes and a 24–bit address bus that provides 16 Mbytes of memory addressing capability. Electrical characteristics of the 68EC000 have been optimized to ensure easy access to low–cost memories.

The 68EC000 represents the lowest cost entry point to any 32–bit architecture. Coupled with efficient support for high–level languages and real–time operating systems, the 68EC000 provides unparalleled compatible migration paths to higher performance.

Integrated Processors

Powerful solutions to cost–, space–, and power–sensitive embedded applications are provided by the 68300 family of integrated microprocessors and microcontrollers. The 68300 family combines two of Motorola's greatest strengths — the 32–bit microprocessor architecture of the 68000 family and a proliferation of peripheral circuits offering a growing family of integrated solutions.

The 68000 family is based on a proven, expandable architecture that spans the performance range from 1 to over 29 MIPS. This architecture offers the industry's highest level of compatibility for both hardware and software. Motorola's single–chip microcomputers and microcontrollers provide the industry's broadest selection of peripheral combinations, insurance that one will fit the need of practically any application. The 683000 family embraces both of these concepts.

Each member of the 68300 family contains a core processor based on the 68000 family, a System Integration Module (SIM), an on–chip bus and various peripheral modules. The SIMs include support circuitry such a clock generation, external chip selects, system protection, timers and JTAG. The on–chip intermodule bus (IMB) on the CPU–based 68300s creates a standard interface over which the CPU and each of the modules communicate. The peripheral modules include specialized processors, system controllers, traditional peripherals and memory. Because the peripheral modules are independent from each other, they can appear in multiple 68300 devices. With so many major features incorporated into a single 68300 device, a system designer can realize improved reliability along with significant savings in design time, power consumption, cost, board space, pin count and program development. In a 68300 device, the major functions and glue logic are all properly connected, internally timed with the same fast clock, fully tested and consistently documented.

Table 3.

	68302	68306	68330	68331	68332	68333	68334	68340
Core Processor	68000	680EC00	CPU32	CPU32	CPU32	CPU32	CPU32	CPU32
Speeds (MHz)	16, 20	16	16, 25	16	16	16	16	16, 25
DMA	Yes	–	–	–	–	–	–	Yes
Serial Processor	Yes	–	–	–	–	–	–	–
Time Processor Unit	–	–	–	–	Yes	Yes	Yes	–
Flash EEPROM	–	–	–	–	–	64K	–	–
Serial I/O	Yes	Yes	–	Yes	Yes	Yes	–	Yes
Timers	1	–	–	1	–	–	–	2
A/D Converter	–	–	–	–	–	Yes	Yes	–
SRAM	1K	–	–	–	2K	4K	1K	–
DRAM Controller	–	Yes	–	–	–	–	–	–
Glue Logic (SIM)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
3.3 Volts Available	–	–	–	–	–	–	–	Yes

MC68302

Integrated Multiprotocol Processor

The MC68302 integrated multiprotocol processor (IMP) is a very large–scale integration (VLSI) device incorporating the main building blocks needed for the design of a wide variety of controllers used in the communications industry. The IMP is the first device to offer the benefits of a closely coupled, industry–standard M68000/MC68008 microprocessor core and a flexible communications architecture. The three–channel communications device may be configured to support a number of popular industry interfaces, including those for the Integrated Services Digital Network (ISDN) basic rate and terminal adaptor applications. Through a combination of architectural and programmable features concurrent operation of different protocols (HDLC/SDLC™, UART, BISYNC, DDCMP™, or transparent modes) can easily be achieved. Data concentrators, modems, line cards, bridges, and gateways are examples of suitable applications for this device.

The IMP is a Complementary Metal–Oxide Semiconductor (CMOS) device consisting of an M68000/MC68008 microprocessor core, a system integration block (SIB), and a Communications Processor (CP). By integrating the microprocessor core with the serial ports (in the CP) and the system peripherals (in the SIB), the IMP is capable of handling complex tasks such as all ISDN basic rate (2B+D) access tasks.

MC68306

Integrated 68EC00 Processor

The 68306 integrated EC000 processor includes many of the features commonly found in 68000–based designs. The 68306 includes a 68EC000 core processor, a 68681 Dual Universal Asynchronous Receiver Transmitter (DUART), system integration functions, and a DRAM controller. The on–chip DRAM controller gives the 68306 the family's simplest interface to DRAM–based designs. The DRAM controller easily accommodates 64 Mbytes of memory. The 68306 saves time in the design cycle by providing valuable 68000 system components pre–packaged in one chip.

MC68330

Integrated CPU32 Processor

The 68330 is ideal for applications requiring 32–bit microprocessor performance without the additional expense inherent in 32–bit memory systems. The 68330 is the simplest and lowest priced member of the CPU32–based 68300 family. The 68330 allows the designer access to the high performance of the CPU32 along with minimized external glue logic, while allowing the greatest freedom in selecting needed peripherals, ASICs or gate arrays.

MC68331

32–Bit Microcontroller

The 68331 is well suited to applications requiring simple serial communications and general timing needs. The 68331 contains the CPU32, a SIM, a General Purpose Timer (GPT) and a Queued Serial Module (QSM). The general purpose timer is a simple yet flexible timer that provides four modes of operation with multiple channels for some operations. The QSM provides two modes of communication: an asynchronous channel that provides up to 524–Kbits per second transfer rate and a serial peripheral interface with separate 16–word receive/transmit queues.

MC68332

32–Bit Microcontroller

The 68332 is especially suited for high–performance timing applications such as automotive engine control, precision motor control and industrial robotics. The powerful Time Processor Unit (TPU) distinguishes the 68332 providing optimum performance in controlling time–related activity. It drastically reduces the need for CPU intervention with its dedicated execution unit, tri–level prioritized scheduler, data storage RAM and dual time bases. In addition to the TPU and CPU32, the 68332 features the QSM, a SIM and 2–Kbytes of standby static RAM.

MC68F333

32–Bit Microcontroller

The 68F333 provides the highest level of integration available to high–performance timing applications such as avionics and automotive engine control. The 68F333 contains the CPU32, the TPU and the QSM. It also adds two banks of flash EEPROM totaling 64–Kbytes, a total of 4–Kbytes of SRAM (512 bytes separately powered) and an 8–channel, 10–bit analog–to–digital converter. The Single–Chip Integration Module (SCIM) allows 18 of the external address and data pins to be converted to I/O pins, resulting in a single–chip solution suitable for many applications.

MC68334

32–Bit Microcontroller

The 68334 is a streamlined version of the 68332, taking advantage of the powerful TPU. The 68334 includes the CPU32 core processor, the TPU, a SIM, 1–Kbyte of SRAM, a 10–bit analog–to–digital converter and up to 47 discrete I/O lines.

MC68340

Integrated Multiprotocol Processor with DMA

The 68340 is excellent for applications requiring high–speed or block data transfers, such as disk drives and navigation systems. The combination of general peripherals and the extremely low power consumption possibilities of the 68340 make it ideal for many battery powered, portable applications such as hand held computers and data acquisition systems.

The most distinguishing 68340 feature is the high speed two channel, 32–bit Direct Memory Access (DMA) controller. Incorporating the CPU32 and DMA on the same chip eliminates the usual bus arbitration and synchronization delays, maximizing data throughout (25–Mbytes per second on a 16–bit bus).

In addition to the CPU32, a SIM and the DMA, the 68340 contains a 68681/2681–compatible DUART. The 68340 also has two identical, versatile counter/timers, each with a 16–bit counter and an 8–bit prescaler with 80 ns resolution.

Coprocessors

MC68851

Paged Memory Management Unit, PMMU

The PMMU is a 32–bit memory manager which provides full support for a demand paged virtual environment with the 68010 or MC68020. It supports a 4–gigabyte addressing space when used as a coprocessor with the MC68020. An on–chip address translation cache minimizes translation delays and maximizes system performance.

MC68881

A Floating Point Coprocessor

Designed specifically for arithmetic expansion of the MC68020 MPUI, this powerful coprocessor can also be used as a peripheral to all other M68000 family members, and with non–M68000 processors as well. It performs floating point math calculations in strict conformance to a full implementation of the IEEE Standard for Binary Floating Point Arithmetic (754) and, in addition to the basic add, subtract, multiply, and divide functions, it handles full selection of transcendental and non–transcendental operations. These operations include root values, trigonometric functions, exponentials, hyperbolics, and logs. All functions are calculated to 80 bits of extended precision in hardware.

MC68882

Enhanced Floating Point Coprocessor

The MC68882 is pin–to–pin hardware and software compatible with the MC68881 Floating Point Coprocessor and implements a variety of performance enhancements including dual–ported registers and an advanced pipeline. Additional circuitry allows execution of multiple instructions in parallel for more than twice the Floating Point performance of the trail–blazing MC68881. Where higher performance requirements indicate, the MC68882 is a drop–in replacement for the MC68881.

DMA Controllers

MC68450

DMA Controller, DMAC

The DMAC maintains high–performance data movement for complex M68000 MPU–based systems. While pin compatible with the MC68440 DDMA, the DMAC offers four completely independent DMA channels. In addition to all the features of the DDMA, the DMAC also provides very sophisticated manipulation of data through sequential and linked array–chained addressing capabilities.

MC68440

Dual Direct Memory Access Controller, DDMA

The DDMA complements the performance capabilities of M68000 microprocessors by moving blocks of data in a quick, efficient manner with a minimum of intervention from the MPU. The DDMA performs memory–to–memory, peripheral–to–memory, and memory–to–peripheral transfers through each of two completely independent DMA channels. The DDMA also offers two interrupt vectors per channel and supports both 8–bit and 16–bit data transfers.

Network Devices

MC68824

Token Bus Controller, TBC

The TBC is the industry's first single–chip VLSI device to implement the IEEE 802.4 Media Access Control Sublayer of the ISO Data Link Layer, as specified by General Motors Manufacturing Automation Protocol, MAP. The TBC supports serial data rates of 1, 5, and 10 Mbps and relieves the host processor of the frame formatting and token management functions. For efficient transfer of data frames, to and from memory, the TBC features an on–chip four–channel DMA with bus master capability, a 32–bit address range, an 8– or 16–bit data bus, and a 40–byte FIFO. The MC68824 also offers support options for network bridges, real–time support and network monitoring services.

MC68184

Broadband Interface Controller

The MC68184 Broadband Interface Controller (BIC) is a high–performance interface device for use with the MC68824 Token Bus Controller (TBC) to implement the digital portion of the physical layer of a broadband IEEE 802.4 token bus node. The BIC manipulates both data and control for RF transmitter circuitry and RF receiver circuitry. The CMOS BIC supports data rates up to 10 Mbps using a duo–binary modulation technique and provides 20 lines for receiver/transmitter control with 13 user–defined outputs.

The BIC performs the digital functions of the physical layer when implementing a broadband token bus node. The modem side of the BIC provides data and control for the RF transmitter/receiver circuitry. A standard serial interface is used to connect the BIC to the MC68824 TBC. The TBC performs the media access control (MAC) function. The MC68184 has the ability to scramble and descramble data.

MC68185

Twisted–Pair Modem

The MC68185 Twisted–Pair Modem (TPM) is used in conjunction with a MC68824 Token Bus Controller (TBC), an RS485 transceiver, and a twisted–pair media to implement a low–cost area network (LAN). The MC68824 TBC implements the layer 2 media access control (MAC) portion of the IEEE 802.4 LAN station and receiver portion for the IEEE 802.2 logical link control (LLC) type 3 as well as providing support for LLC type 1 and type 2. The TPM interfaces directly to the TBC, providing physical layer management, including MAC symbol encoding/decoding at data rates up to 2 Mbps.

The TPM contains an 32 kHz to 20 MHz on–chip crystal oscillator that generates a transmit clock without external circuitry. The physical layer management includes local loopback mode, transmitter enable, and reset. An on–chip digital filter provides for noise reduction of received data.

MC68194

Carrierband Modem

The bipolar LSI MC68194 Carrierband Modem (CBM), when combined with the MC68824 Token Bus Controller (TBC), provides an IEEE 802.4 single–channel, phase–coherent carrierband, Local Area Network (LAN) connection. The CBM performs the physical layer function, including symbol encoding/decoding, signal transmission and reception, and physical management.

The CBM provides the three basic functions of the physical layer: data transmission to the coaxial cable, data reception from the cable, and management of the physical layer. For standard data mode (also called MAC mode), the CBM receives a serial transmit data stream from the TBC (called symbols or atomic symbols), encodes, modulates the carrier, and transmits the signal to the coaxial cable. Also in the data mode, the CBM receives a signal from the cable, demodulates the signal, recovers the data, and sends the received data symbols to the TBC. End–of–transmission receiver blanking as required by IEEE 802.4 is supported. Communication between the TBC and CBM is through a standardized serial interface consistent with the IEEE 802.4 DTE–DCE interface.

MC68195

Local Talk Adaptor

The MC68195 LocalTalk adaptor (LA) is used in conjunction with the MC68302 Integrated Multiprotocol Processor (IMP) to build a network interface to LocalTalk™, also known as AppleTalk™. LocalTalk refers to the 230.4–kbps Local Area Network (LAN) that connects multiple MacIntosh™ computers and printers.

The LA provides LocalTalk support for any two of the three IMP serial channels. Combinations of multiple LA and/or IMP devices may be used to support additional LocalTalk channels. Non–LocalTalk applications can use the LA device with the IMP to build proprietary HDLC–based LANs at up to 2.5 Mbps using bi–phase space (FMO) encoding.

MC68605

X.25 Protocol Controller, XPC

The XPC implements the 1984 CCITT X.25 Recommendation Data Link Procedure (level 2) LAPB. In addition to handling the lower level communications functions (HDLC framing, CRC generation/checking, and zero insertion/deletion), the XPC also independently handles higher level communications functions (frame sequencing, retransmission, flow control, retries limit and timeout conditions). This allows the host to operate almost totally isolated from the task of ensuring error–free transmission and reception of data.

MC68606

Multi–Link LAPD Controller CCITT Q.920/Q.921, LAPD

The MC68606 Multi–link LAPD (MLAPD) Protocol Controller fully implements CCITT Recommendation Q.920/Q.921 Link Layer Access Procedure (LAPD) protocol for ISDN networks. The MLAPD is designed to handle both signalling and data links in high–performance ISDN primary rate applications.

This VLSI device provides a cost–effective solution to ISDN link–level processing with simultaneous support for up to 8K logical links. The MC68606 is an intelligent communications protocol controller compatible with AT&T specifications for ISDN devices and features low power consumption and high performance, with an aggregate data rate in excess of 2.048 Mbps.

Data Communication Devices

MC68681
MC2681

Dual Universal Asynchronous Receiver/Transmitter, DUART

The MC68681 features two completely independent full–duplex asynchronous receiver/transmitter channels that interface directly to the M68000 microprocessor bus. Receiver data registers are quadruple buffered and transmitter data registers are double buffered for minimum MPU intervention. Each has its own independently selectable baud rate. Multifunction 6–bit input port and 8–bit output port, a 16–bit programmable counter/timer, interrupt handling capabilities, and a maximum one–megabyte per second transfer rate make the DUART an extremely powerful device for complex data communication applications. Full device functionality with an M6800 bus interface is provided by the MC2681.

General Purpose I/O

MC68230

Parallel Interface/Timer, PI/T

The PI/T provides versatile double–buffered parallel interfaces and a system–oriented timer for M68000 systems. The parallel interfaces operate either in a unidirectional or bidirectional mode, either 8– or 16–bit wide. The timer is 24 bits with full programmability and a 5–bit prescaler. The PI/T has a complete M68000 bus interface and is fully compatible with the MC68450 DMAC.

MC68901

Multifunction Peripheral, MFP

The MFP provides basic microcomputer function requirements as a single companion chip to the M68000 Family of Microprocessors. Features provided via a direct M68000 system bus interface include a full–function, single–channel Universal Serial Asynchronous Receiver/Transmitter (USART) for data communication, an 8–source interrupt controller, eight parallel I/O lines, and four 8–bit timers.

Fiber Distributed Data Interface

Fiber Distributed Data Interface (FDDI) is defined as a dual fiber–optic token ring LAN (Local Area Network) that can support rates up to 100 Mbps. It can accommodate rings with 1,000 stations. Two kilometers between stations, and up to 200 kilometers in total length. This technology is driven by the need to support high performance distributed computer systems which are becoming faster and more powerful, thus imposing a greater need for network speed and bandwidth. Other uses for FDDI include backbone networks connecting Ethernet, Token Bus, and Token Ring segments and back end networks connecting high–speed peripherals. FDDI is an American National Standards Institute (ANSI) standard. Motorola's FDDI chip set includes the MC68836, MC68837, MC68838, and MC68839.

MC68836

FDDI Clock Generator

The MC68836 FDDI Clock Generator (FCG) implements part of the Physical Layer (PHY) functions of the FDDI standard including clock recovery, data recovery, and NRZI conversions. The FCG also does a five–bit parallel to serial conversion during transmission, and a serial to five–bit parallel conversion during reception. The FCG uses the five–bit parallel interface to communicate with the MC68837 device. The FCG directly connects to fiber optic modules through differential driver/receiver pins. Features include full duplex operations, 125 MHz clock recovery from incoming serial NRZI data stream, and 125 MHz transmit clock generation.

MC68837

Elasticity Buffer and Link Manager

The Elasticity Buffer and Link Manager (ELM) implements the remaining of the PHY functions of the FDDI standard including data framing, elasticity buffer, encoding, decoding, smoothing, line state detection, and repeat filter. The ELM also implements some Station Management (SMT) functions such as the Connection Management (CMT), Physical Connection Management (PCM), Physical Connection Insertion (PCI), and Link Error Monitor (LEM).

MC68838

Media Access Controller

The Media Access Controller (MAC) implements the MAC portion of the FDDI standard. The MAC protocol is the lower sub–layer of the ISO OSI data link layer and provides for fair and deterministic sharing of the physical medium, address recognition, frame check sequence generation and verification, frame insertion, frame repetition, frame removal, token generation, and certain error recovery procedures. Features on the MC68838 include independent receive and transmit data paths and state machines, bridging support including a bit order reversal option, a count and void frame bridge stripping algorithm, and CRC appendage on a per frame basis. The MAC also contains an interface to Content Addressable Memory (CAM) for individual and multicast address recognition.

MC68839

FDDI System Interface

The FDDI System Interface (FSI) is a high performance interface device which can easily connect to any bus including high speed processors, little– and big–endian busses, and multiplexed/non–multiplexed address data busses. Its primary purpose is to interface the FDDI protocol devices to the user system bus. FSI features include support for a ring buffer structure, addressing flexibility, programmable partitioned 8K bytes internal RAM for temporary data storage, two 32–bit ports, the ability to sustain up to 250 μs bus latencies, support for synchronous and asynchronous frames, and the ability to chain multiple buffers per frame.

Development Tools

Application Development System

The M68302ADS is a stand–alone board developed by Motorola that includes software modules (driver code, LAPB, LAPD, and X.25), a real–time kernel, and a monitor/debugger. The board consists of the MC68302, memory (512K bytes of RAM expandable to 1M bytes, 256 bytes of EPROM and EEPROM), and an MC68681 DUART (to allow all MC68302 serial ports to be available to the user). It is an inexpensive, ideal platform for software development and testing.

M68EC0x0IDP

Evaluation Boards for Embedded Controllers

The M68000 family IDP is a board set designed to provide a low–cost evaluation platform, yet flexible environment for developing both software and hardware for the family products. The platform provides the means for M68000 microprocessor and tool evaluation which enables users to properly select the microprocessor and associated tools for their next application. Because the turnkey development system requires the user to do very little to power up the system and begin development, significant time savings is realized by reducing the overall time that the product takes to get to market.

The IDP consists of an M68000 Family microprocessor–based CPU module as well as a generic IDP motherboard designed to support each CPU module. The IDP also includes two software debug monitor programs: Integrated Systems' ROM68K™ and Intermetrics' SmartROM™. This configuration allows the user to take advantage of an entire suite of features, including tracing, assembling, disassembling and downloading, that are offered by the monitors. Optional software is available to expand the development environment of the IDP by allowing the user to design, debug and evaluate the M68000 microprocessor–based applications in real–time and non–real–time operating system environments. The IDP also functions as a tool for final test or fault analysis of user target systems.

The IDP only requires a user–supplied power supply and an RS–332 ASCII terminal or host computer with an RS–232 serial port. Although the IDP will function using a terminal, the preferred communication device is a host computer. Operating the IDP with a host computer allows the user to develop, compile and debug code using one of many optional software tools. Once code is developed, the program can be saved and downloaded to the IDP from the host computer.

M68340EVS

Evaluation System

The M68340EVS is an inexpensive three–board evaluation and development system which allows the user to design, debug and evaluate 68340–based applications. It interfaces easily to traditional emulation tools and includes its own software debugger.

Support Software

M68KESW–PC1

This Intermetrics software package is for the 68K Family (68000, 68008, 68HC001, 68010, 68020, 68030, 68EC030, 68040, 683xx). The M68KESW InterTools package includes C compiler, assembler/linker, run–time libraries, and one year of support from Intermetrics.

M68040FPSP

This software provides 68040 floating point emulation of unimplemented 68881/68882 functions. Contact factory for license agreement.

Table 4. Selector Guide

Device Number	Package	Speeds	Device Type
MC68000	64–Lead L*, P 68–Lead R, RC*, FN	8, 10, 12, 12F* 8, 10, 12, 12F*	Microprocessor
MC68EC000	68–Lead FN	8, 10, 12, 16	Embedded Controller
MC68HC000	64–Lead P 68–Lead R, RC*, FN 68–Lead FC	8, 10, 12, 12F*, 16 8, 10, 12, 16 8, 10, 12, 16	Microprocessor
MC68HC001	68–Lead R, RC*, FN	8, 10, 12, 16	
MC68008	48–Lead P 52–Lead FN	8, 10 8, 10	Microprocessor
MC68010	64–Lead P 68–Lead R, RC*, FN	8, 10, 12 8, 10, 12	Microprocessor

* Not recommended for new design
All package/speed combinations may not be valid – consult factory to verify

Table 4. Selector Guide (continued)

Device Number	Package	Speeds	Device Type
MC68020	114–Lead RC 132–Lead FE* 114–Lead RP 132–Lead FC	12, 16, 20, 25, 33 16, 20, 25 16, 20, 25 16, 20, 25	Microprocessor
MC68EC020	100–Lead FG, RP	16, 25	Embedded Controller
MC68030	128–Lead RC 124–Lead RP 132–Lead FE	16, 20, 25, 33, 40, 50 16, 20, 25, 33 16, 20, 25, 33	Microprocessor
MC68EC030	124–Lead RP 132–Lead FE	25, 40 25, 40	Embedded Controller
MC68040	179–Lead RC	25, 33, 40	Microprocessor
MC68EC040	179–Lead RC 184–Lead FE	20, 25, 33 20, 25	Embedded Controller
MC68LC040	179–Lead RC 184–Lead FE	20, 25, 33 20, 25	Microprocessor
MC68040V	184–Lead FE	25, 33	Microprocessor
MC68060	223–Lead RC TBD–Lead FE	50, 66 50, 66	Microprocessor
MC68184	40–Lead P, L	–	Network
MC68185	44–Lead FN 68–Lead RC	– –	Network
MC68194	52–Lead FJ	–	Network
MC68195	44–Lead FN	–	Network
MC68230	48–Lead P 52–Lead FN	8, 10 8, 10	General Purpose I/O
MC68302	132–Lead RC, FE, FC, FD	16, 20	Integrated Processor
MC68306	128–Lead FC 132–Lead FG	16 16	Integrated Processor
MC68330	132–Lead FC	16, 25 8, 16 @ 3.3 V	Integrated Processor
MC68331	132–Lead FC	16	Integrated Processor
MC68332	132–Lead FC	16	Integrated Processor
MC68340	144–Lead FE 145–Lead RP	16, 25 16, 25	Integrated Processor
MC68340V	144–Lead FE 145–Lead RP	8, 16 @ 3.3 V 8, 16 @ 3.3 V	Integrated Processor
MC68360	240–Lead FC 241–Lead RC	0 – 25 0 – 25	Integrated Communication Controller
MC68440	68–Lead L, P 68–Lead R, FN	8, 10 8, 10	DMA Controller
MC68450	68–Lead L, P 68–Lead R, FN	8, 10 8, 10	DMA Controller
MC68605	84–Lead R, RC 84–Lead FN	10, 12, 16 10, 12, 16	Network
MC68606	84–Lead RC 84–Lead FN	12, 16 12, 16	Network

* Not recommended for new design
All package/speed combinations may not be valid – consult factory to verify

Table 4. Selector Guide (continued)

Device Number	Package	Speeds	Device Type
MC2681	40–Lead P, L* 44–Lead FN	– –	Data Communication
MC68681	40–Lead P, L* 44–Lead FN	– –	Data Communication
MC68824	84–Lead R, RC 84–Lead FN	10, 12, 16 10, 12, 16	Network
MC68836	52–Lead FN	– –	Fiber Distributed Data Interface
MC68837	120–Lead KB 120–Lead FC	– –	Fiber Distributed Data Interface
MC68838	120–Lead KB 120–Lead FC	– –	Fiber Distributed Data Interface
MC68839	184–Lead RC 184–Lead FE	– –	Fiber Distributed Data Interface
MC68851*	132–Lead RC	12, 16, 20	CoProcessor
MC68881	68–Lead RC, FN	12, 16, 20	CoProcessor
MC68882	68–Lead RC 68–Lead RN	16, 20, 25, 33, 40, 50 16, 20, 25, 33, 40	CoProcessor
MC68901	48–Lead P 52–Lead FN	– –	General Purpose I/O

FC = Plastic Quad (Gull Wing)	FN = Plastic Quad Pack (PLCC)	P = Plastic DIP
FD = Plastic Quad w/Molded Carrier Ring	KB = Ceramic PGA w/Ceramic Lid	R = Pin Grid Array, Solder Lead Finish
FE = Ceramic Quad (Gull Wing)	L = Ceramic DIP	RC = Ceramic PGA, Gold Lead Finish
FG = Plastic Quad Flat Pack (PQFP)	LC = Ceramic DIP, Gold Lead Finish	RP = Plastic Pin Grid Array

* Not recommended for new design
All package/speed combinations may not be valid – consult factory to verify

The M88000 RISC Family

In Brief . . .

Motorola's 88000 Family comes from the only company committed to long–term upward software compatibility through such features as hardware interlocked and protected pipelines. Our goal is to make sure each generation of the 88000 RISC family delivers a high performance level while maintaining software compatibility.

Motorola's 88000 RISC Microprocessors

. . . a performance architecture

Architecture, Performance, and Software Compatibility

The 88000 RISC was designed from the start for superscaler implementations. In fact, the design of the second generation 88110 microprocessor is a unique superscaler implementation called Symmetric Superscalar™. The Symmetric Superscaler design allows you to execute multiple instructions in a single clock cycle without any restrictions on instruction ordering. So there are no wait states or performance penalties because of out of order instructions.

Also, while other RISC microprocessors may be limited in the instructions they can execute in a single clock cycle, members of the 88000 are able to execute multiple instructions per clock cycle, thus providing the performance edge required for next generation system designs.

Performance Plus Software Compatibility

Although high performance is recognized as a key feature for systems design, software compatibility is also important. Motorola's 88000 Family comes from the only company committed to long term upward software compatibility through such features as hardware interlocked and protected pipelines. Our goal is to make sure each generation of the 88000 RISC family delivers a high performance level while maintaining software compatibility. This gives the opportunity for designing one of the industry's highest performance systems, while leveraging your largest dollar investment in new systems, your software.

Software compatibility is also promoted through standards to provide an open systems environment benefitting system companies, software developers, and end users because 88000 based systems from different vendors will run all of the same software.

Microprocessors

MC88100RC
32–Bit RISC Microprocessor

The MC88100 is the first processor in the 88000 Family of RISC (reduced instruction set computer) microprocessors. Implemented with Motorola's HCMOS technology, the MC88100 incorporates 32–bit registers, data paths, and addresses. In designing the MC88100, Motorola has incorporated a high degree of fine–grain parallelism; four independent execution units maintain separate, fully concurrent execution pipelines. Most instructions operate in one machine cycle or effective concurrent execution can be accomplished through internal pipelines in one machine cycle. A common register file provides data sharing and synchronization control among the execution units through register scoreboarding.

The MC88100 addresses a variety of applications requiring high operational speeds and efficient, fast–execution architectures. All data manipulation instructions are nondestructive register to register or register with immediate operations, allowing both fast operand access and operand reuse. IEEE 754 floating–point arithmetic is supported in the processor. Instruction and data memory space are accessed through separate memory ports, allowing simultaneous access to dedicated memory areas. The 88000 Family includes the MC88200 CMMU (cache/memory management unit), which adds high–speed memory caching, two–level, demand–paged memory management, and support for shared–memory multiprocessing. The 88000 Family also includes a full line of highly optimizing compilers, operating systems, development boards, and development tools.

MC88110RC
32–Bit RISC Microprocessor

The MC88110 is the second implementation of the 88000 family of reduced instruction set computer (RISC) microprocessors. The MC88110 is a Symmetric Superscalar machine capable of issuing and retiring two instructions per clock without any special alignment, ordering, or type restrictions on the instruction stream. Instructions are issued to multiple execution units, execute in parallel, and can complete out of order, with the machine automatically keeping results in the correct program sequence. The Symmetric Superscalar design allows sustained performance to approach the peak performance capability.

The MC88110 uses dual instruction issue and simple instructions with extremely rapid execution times to yield maximum efficiency and throughput for 88000 systems. Instructions either execute in one clock cycle, or effective one clock cycle execution is achieved through internal pipelining. Ten independent execution units communicate with a general register file and an extended register file through multiple 80–bit internal buses. Each of the register files has sufficient bandwidth to supply four operands and receive two results per clock cycle. Each of the pipelined execution units, including those that execute floating–point and data movement instructions, can accept a new instruction and retire a previous instruction on every clock cycle.

In a single chip implementation, the MC88110 integrates the central processing unit, floating point unit, graphics processing unit, virtual memory address translation, instruction cache, and data cache. The MC88110 maintains compatibility with MC88100 user application software.

Cache/Memory Management Units

MC88200RC

16–Kilobyte Cache/Memory Management Unit (CMMU)

The MC88200 CMMU is a high–performance, HCMOS VLSI device providing zero–wait–state memory management and data caching. The MMU (memory management unit) efficiently supports a demand–paged virtual memory environment with two logical address ranges (user/supervisor) of 4 gigabytes each. Translated addresses are provided by one of two ATCs (address translation caches), providing address translation in one clock cycle for most memory accesses. The PATC (page address translation cache) is a 56–entry, fully associative cache containing recently used translations for 4–kilobyte memory pages and is maintained by MC88200 hardware. The BATC (block address translation cache) is a 10–entry cache, loaded by software, containing translations for 512–kilobyte memory blocks. The BATC translations are used for operating system software or for other memory–resident instructions and data. In addition, the MMU provides access control for the two logical address spaces. The CMMU data cache is a 16–kilobyte, four–way, set–associative cache for instruction or data storage. The cache incorporates memory–update policies and cache–coherency mechanisms that support multiprocessor applications. The MC88200 CMMU also includes an MC88100–compatible P bus (processor bus) interface and an M bus (memory bus) interface. A processor may use two or more CMMUs for increased data cache and ATC sizes.

MC88204RC

64K–Byte Cache/Memory Management Unit (CMMU)

The MC88204 CMMU is a high–performance, HCMOS VLSI device providing zero–wait–state memory management and data caching. The memory management unit (MMU) efficiently supports a demand–paged virtual memory environment with two logical address ranges (user/supervisor) of 4 Gbytes each. Translated addresses are provided by one of two address translation caches (ATCs), providing address translation in one clock cycle for most memory accesses. The page address translation cache (PATC) is a 56–entry, fully associative cache containing recently used translations for 4K–byte memory pages and is maintained by MC88204 hardware. The block address translation cache (BATC) is a 10–entry cache, loaded by software, containing translations for 512K–byte memory blocks. The BATC translations are used for operating system software or for other memory–resident instructions and data. In addition, the MMU provides access control for the two logical address spaces. The CMMU data cache is a 64K–byte, four–way set–associative cache for instruction or data storage. The cache incorporates memory–update policies and cache–coherency mechanisms that support multiprocessor applications. The MC88204 CMMU also includes an MC88100–compatible processor bus (P bus) interface and memory bus (M bus) interface.

The MC88204 CMMU is completely software and pin–level compatible with the MC88200 16K–byte CMMU. The functionality of the MC88204 is identical to that of the MC88200. With board layout constraints in mind, a central processing unit (CPU) may use up to two MC88204 CMMUs on the data P bus and up to two MC88204 CMMUs on the instruction P bus to increase data cache and ATC sizes.

MC88410

Secondary Cache Controller

The MC88410 is a highly integrated secondary cache controller for the MC88110 microprocessor that reduces memory latency and extends multiprocessing capability for those seeking the highest level of system performance. Used with the MCM62110 Fast Static RAM, it provides a functionally complete secondary cache solution for both uniprocessor and multiprocessor environments. The MC88410 provides tag, control and buffering for 1/4, 1/2, and 1 Mbyte secondary cache configurations, all in a single chip cache controller. The MC88410 eliminates external logic between the processor and the secondary cache, provides bus arbitration for the MC88110, and requires no external programming.

The MC88410 and MCM62110 are optimized to provide low latency memory access to the MC88110 processor. Initial accesses incur only one wait state. Subsequent transactions in a burst incur zero wait states. Data streaming to the processor reduces the penalty on secondary cache misses.

The MC88410 expands the MC88110's system flexibility by providing a choice of secondary cache line size, burst byte ordering, and system clock frequency. The MC88410 extends the MC88110 multiprocessing capability by significantly reducing system bandwidth consumption. This increased available bandwidth, along with the MC88410's hardware enforced cache coherency protocol, enable the implementation of dual bus systems and scalable shared–bus multiprocessing systems.

The PowerPC™ RISC Family Microprocessors

In Brief . . .

The PowerPC architecture is derived from the IBM Performance Optimized with Enhanced RISC (POWER) architecture. The PowerPC architecture shares all of the benefits of the POWER architecture but is optimized for single–chip implementations. The architecture design emphasizes parallel instruction execution and high throughput and allows for exceptional floating–point performance. The PowerPC architecture is powerful today and is scalable from palmtops to mainframes.

Page

PowerPC™ RISC Microprocessors

The PowerPC Architecture™, developed jointly by Motorola, IBM, and Apple, is based on the POWER Architecture™ implemented by the RISC System/6000™ family of computers. The PowerPC architecture takes advantage of recent technological advances in such areas as process technology, compiler design, and RISC (reduced instruction set computer) microprocessor design to provide software compatibility across a diverse family of implementations, primarily single–chip microprocessors, intended for a wide range of systems, including battery–powered personal computers, embedded controllers, high–end scientific and graphics workstations, and multiprocessing, microprocessor–based mainframes.

To provide a single architecture for such a broad assortment of processor environments, the PowerPC architecture is both flexible and scalable.

The flexibility of the PowerPC architecture offers many price/performance options. Designers can choose whether to implement architecturally–defined features in hardware or in software. For example, a processor designed for a high–end workstation has greater need for the performance gained from implementing floating–point normalization and denormalization in hardware than a battery–powered, general–purpose computer might.

The PowerPC architecture is scalable to take advantage of continuing technological advances — for example, the continued miniaturization of transistors makes it more feasible to implement more execution units and a richer set of optimizing features without being constrained by the architecture.

The PowerPC architecture defines the following features:

- Separate 32–entry register files for integer and floating–point instructions. The general–purpose registers (GPRs) hold source and target data for integer arithmetic instructions, and the floating–point registers (FPRs) hold source and target data for floating–point arithmetic instructions.
- Instructions for loading and storing data between the memory system and either the FPRs or GPRs.
- Uniform–length instructions to allow simplified instruction pipelining and parallel processing instruction dispatch mechanisms.
- Nondestructive use of registers for arithmetic instructions in which the second, third, and sometimes the fourth operand, typically specify source registers for calculations whose results are typically stored in the target register specified by the first operand.
- A precise exception model (with the option of treating floating–point exceptions imprecisely).
- Floating–point support that includes IEEE–754 floating–point operations.
- The ability to perform both single– and double–precision floating–point operations.
- A flexible architecture definition that allows certain features to be performed in either hardware or with assistance from implementation–specific software depending on the needs of the processor design.
- User–level instructions for explicitly storing, flushing, and invalidating data in the on–chip caches. The architecture also defines special instructions (cache block touch instructions) for speculatively loading data before it is needed, potentially reducing the effect of memory latency.
- Definition of a memory model that allows weakly–ordered memory accesses. This allows bus operations to be reordered dynamically, which improves overall performance and in particular reduces the effect of memory latency on instruction throughput.
- Support for separate instruction and data caches (Harvard architecture) and for unified caches.
- Support for both big– and little–endian addressing modes.
- Support for 64–bit addressing. The architecture supports both 32–bit or 64–bit implementations. This document typically describes the architecture in terms of the 64–bit implementations in those cases where the 32–bit subset can be easily deduced.

MPC601 RISC Microprocessor

The MPC601 is the first implementation of the PowerPC architecture. The MPC601 implements the 32–bit portion of the PowerPC architecture, which provides 32–bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating–point data types of 32 and 64 bits. For 64–bit PowerPC implementations, the PowerPC architecture provides 64–bit integer data types, 64–bit addressing, and other features required to complete the 64–bit architecture.

The MPC601 is a superscalar processor capable of issuing and retiring three instructions per clock, one to each of three execution units. Instructions can complete out of order for increased performance; however, the MPC601 makes execution appear sequential.

The MPC601 integrates three execution units — an integer unit (IU), a branch processing unit (BPU), and a floating–point unit (FPU). The ability to execute three instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for MPC601–based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single–precision multiply–add instruction can be issued every clock cycle.

The MPC601 includes an on–chip, 32–Kbyte, eight–way set–associative, physically addressed, unified instruction and data cache and an on–chip memory management unit (MMU). The MMU contains a 256–entry, two–way set–associative, unified translation look–aside buffer (UTLB) and provides support for demand paged virtual memory address translation and variable–sized block translation. Both the UTLB and the cache use least recently used (LRU) replacement algorithms.

The MPC601 has a 64–bit data bus and a 32–bit address bus. The MPC601 interface protocol allows multiple masters to compete for system resources through a central external arbiter. Additionally, on–chip snooping logic maintains cache coherency in multiprocessor applications. The MPC601 supports single–beat and burst data transfers for memory accesses; it also supports both memory–mapped I/O and I/O controller interface addressing.

The MPC601 uses an advanced, 3.6–volts (601) or 2.5 volts (601v) CMOS process technology and maintains full interface compatibility with TTL devices.

Block Diagram

Figure 1 provides a block diagram of the MPC601 that illustrates how the execution units — IU, FPU, and BPU — operate independently and in parallel.

MPC602 RISC Microprocessor

The MPC602 is a low–cost, low–power implementation of the PowerPC RISC architecture. The MPC602 implements the 32–bit portion of the PowerPC architecture, which provides 32–bit effective addresses, integer data types of 8, 16, and 32 bits, and floating–point data types of 32 and 64 bits. Floating–point operations involving either 32– or 64–bit data types in single–precision format are supported; however, floating–point operations involving 64–bit data types in double–precision format are not implemented in hardware and are instead trapped for emulation in software.

The MPC602 has four execution units—an integer unit (IU), a floating–point unit (FPU), a branch processing unit (BPU), and a load/store unit (LSU). The ability to execute four instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for MPC602–based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined such that typically when the FPU pipeline is full, a single–precision instruction can complete every clock cycle.

The MPC602 provides dynamic and static power–saving modes. The three static modes — nap, doze, and sleep — progressively reduce the amount of power dissipated by the processor.

The MPC602 provides independent on–chip, 4–Kbyte, two–way set–associative, physically addressed caches for instructions and data and on–chip instruction and data memory management units (MMUs). The MPC602 MMUs contain 32–entry, two–way set–associative, data and instruction translation lookaside buffers (DTLB and ITLB). The MPC602 provides an additional memory protection mechanism not defined by the PowerPC architecture. The 602's protection–only mode can control whether instructions can be fetched from 4–Kbyte instruction pages and whether data can be written to 4–Kbyte data pages.

The MPC602 has a single bus interface used for transferring both 32–bit addresses and either 32– or 64–bit data. This bus is time–multiplexed. The MPC602 interface protocol allows multiple masters to compete for system resources through a central external arbiter. The MPC602 provides a three–state coherency protocol that supports the modified, exclusive, and invalid (MEI) cache states. This protocol is a compatible subset of the MESI (modified/exclusive/shared/invalid) four–state protocol and operates coherently in systems that contain four–state caches.

The MPC602 uses an advanced, 3.3–V CMOS process technology and maintains full interface compatibility with TTL devices.

Block Diagram

The MPC602 block diagram in Figure 2 illustrates how the execution units — IU, FPU, BPU, and LSU — operate independently and in parallel.

MPC603 RISC Microprocessor

The MPC603 is the first low–power implementation of the PowerPC architecture. The MPC603 implements the 32–bit portion of the PowerPC architecture, which provides 32–bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating–point data types of 32 and 64 bits. For 64–bit PowerPC implementations, the PowerPC architecture provides 64–bit integer data types, 64–bit addressing, and other features required to complete the 64–bit architecture.

The MPC603 provides four software controllable power–saving modes. Three of the modes (the nap, doze, and sleep modes) are static in nature, and progressively reduce the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the MPC603 to automatically enter a low–power mode when the functional units are idle without affecting operational performance, software execution or any external hardware.

The MPC603 is a superscalar processor capable of issuing and retiring a maximum of three instructions per clock. Instructions can execute out of order for increased performance; however, the MPC603 makes completion appear sequential.

The MPC603 integrates five execution units — an integer unit (IU), a floating–point unit (FPU), a branch processing unit (BPU), a load/store unit (LSU) and a system register unit (SRU). The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for MPC603–based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single–precision multiply–add instruction can be issued every clock cycle.

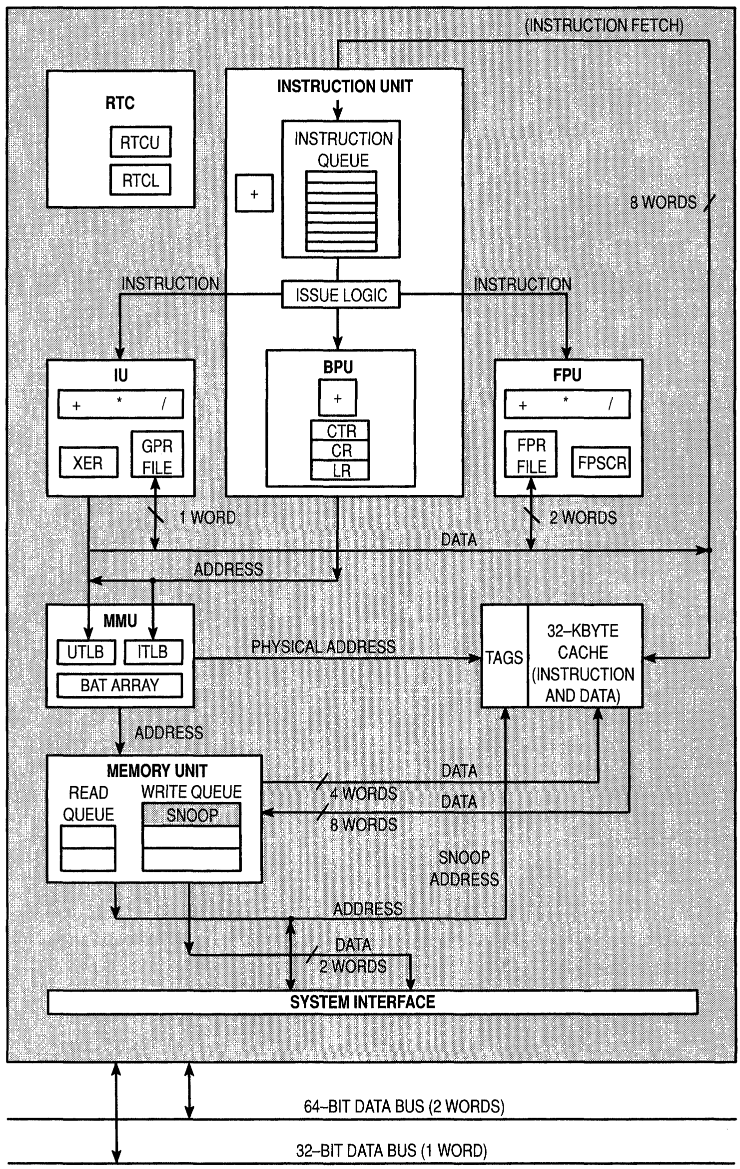


Figure 1. MPC601 Block Diagram

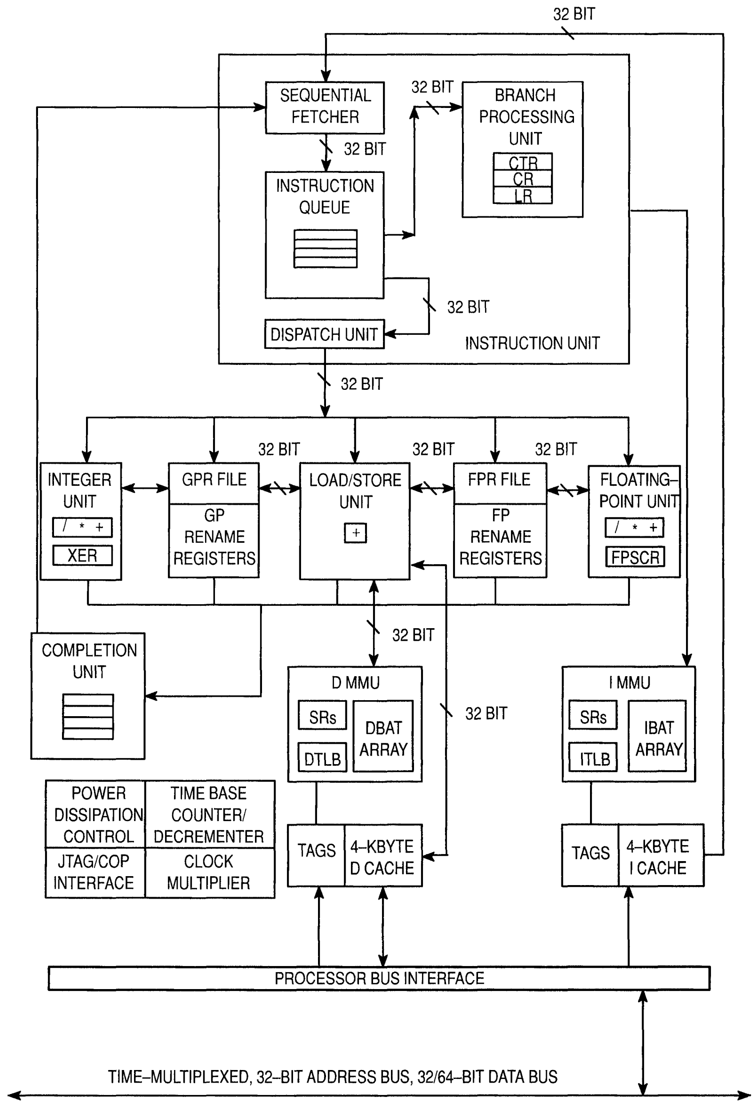


Figure 2. MPC602 Block Diagram

The MPC603 provides independent on–chip, 8–Kbyte, two–way set–associative, physically addressed caches for instructions and data and on–chip instruction and data memory management units (MMUs). The MMUs contain 64–entry, two–way set–associative, data and instruction translation lookaside buffers (DTLB and ITLB) that provide support for demand–paged virtual memory address translation and variable–sized block translation.

The MPC603 has a selectable 32– or 64–bit data bus and a 32–bit address bus. The MPC603 interface protocol allows multiple masters to compete for system resources through a central external arbiter. The MPC603 provides a three–state coherency protocol that supports the Exclusive, Modified, and Invalid cache states. This protocol is a compatible subset of the MESI four–state protocol and operates coherently in systems that contain four–state caches. The MPC603 supports single–beat and burst data transfers for memory accesses; it also supports both memory–mapped I/O and I/O controller interface addressing.

The MPC603 uses an advanced, 3.3–V CMOS process technology and maintains full interface compatibility with TTL devices.

Block Diagram

Figure 3 provides a block diagram of the MPC603 that illustrates how the execution units — IU, FPU, BPU, LSU, and SRU — operate independently and in parallel.

The MPC603 provides address translation and protection facilities, including an ITLB, DTLB, and instruction and data BAT arrays. Instruction fetching and issuing is handled in the instruction unit. Translation of addresses for cache or external memory accesses are handled by the MMUs.

MPC603e RISC Microprocessor

The MPC603e is a low–power implementation of the PowerPC RISC architecture. The MPC603e implements the 32–bit portion of the PowerPC architecture, which provides 32–bit effective addresses, integer data types of 8, 16, and 32 bits, and floating–point data types of 32 and 64 bits.

The MPC603e provides four software controllable power–saving modes. Three of the modes (the nap, doze, and sleep modes) are static in nature, and progressively reduce the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the MPC603e to automatically enter a low–power mode when the functional units are idle without affecting operational performance, software execution, or any external hardware.

The MPC603e is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can execute out of order for increased performance; however, the MPC603e makes completion appear sequential.

The MPC603e integrates five execution units — an integer unit (IU), a floating–point unit (FPU), a branch processing unit (BPU), a load/store unit (LSU), and a system register unit (SRU). The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for MPC603e–based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single–precision multiply–add instruction can be issued every clock cycle.

The MPC603e provides independent on–chip, 16–Kbyte, four–way set–associative, physically addressed caches for instructions and data and on–chip instruction and data memory management units (MMUs). The MMUs contain 64–entry, two–way set–associative, data and instruction translation lookaside buffers (DTLB and ITLB) that provide support for demand–paged virtual memory address translation and variable–sized block translation.

The MPC603e has a selectable 32– or 64–bit data bus and a 32–bit address bus. The MPC603e interface protocol allows multiple masters to compete for system resources through a central external arbiter. The MPC603e provides a three–state coherency protocol that supports the exclusive, modified, and invalid cache states. This protocol is a compatible subset of the MESI (modified/exclusive/shared/invalid) four–state protocol and operates coherently in systems that contain four–state caches. The MPC603e supports single–beat and burst data transfers for memory accesses, and supports memory–mapped I/O accesses.

The MPC603e uses an advanced CMOS process technology and maintains full interface compatibility with TTL devices. The MPC603e is implemented in both a 2.5–V version (PID7V–603e) and a 3.3–V version (PID6–603e).

Block Diagram

Figure 4 provides a block diagram of the MPC603e that illustrates how the execution units — IU, FPU, BPU, LSU, and SRU — operate independently and in parallel.

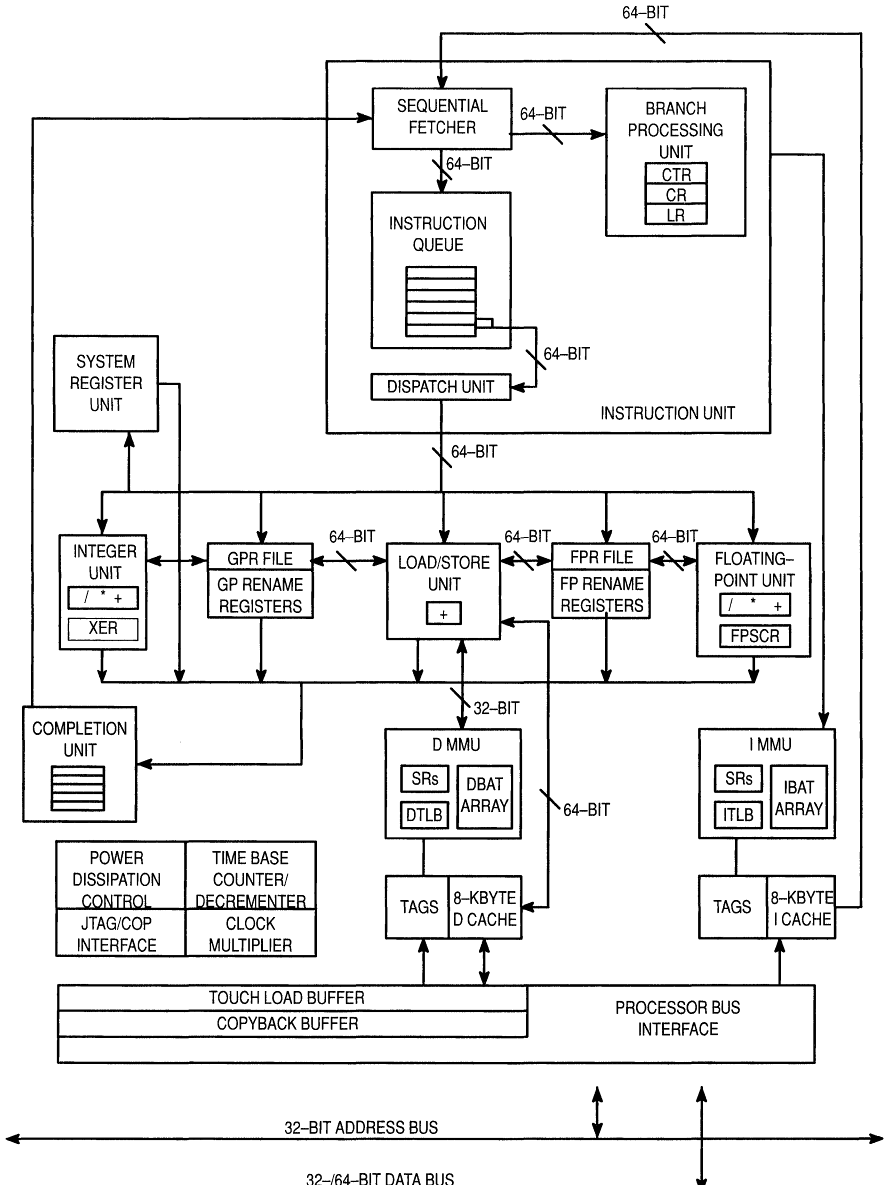


Figure 3. MPC603 Block Diagram

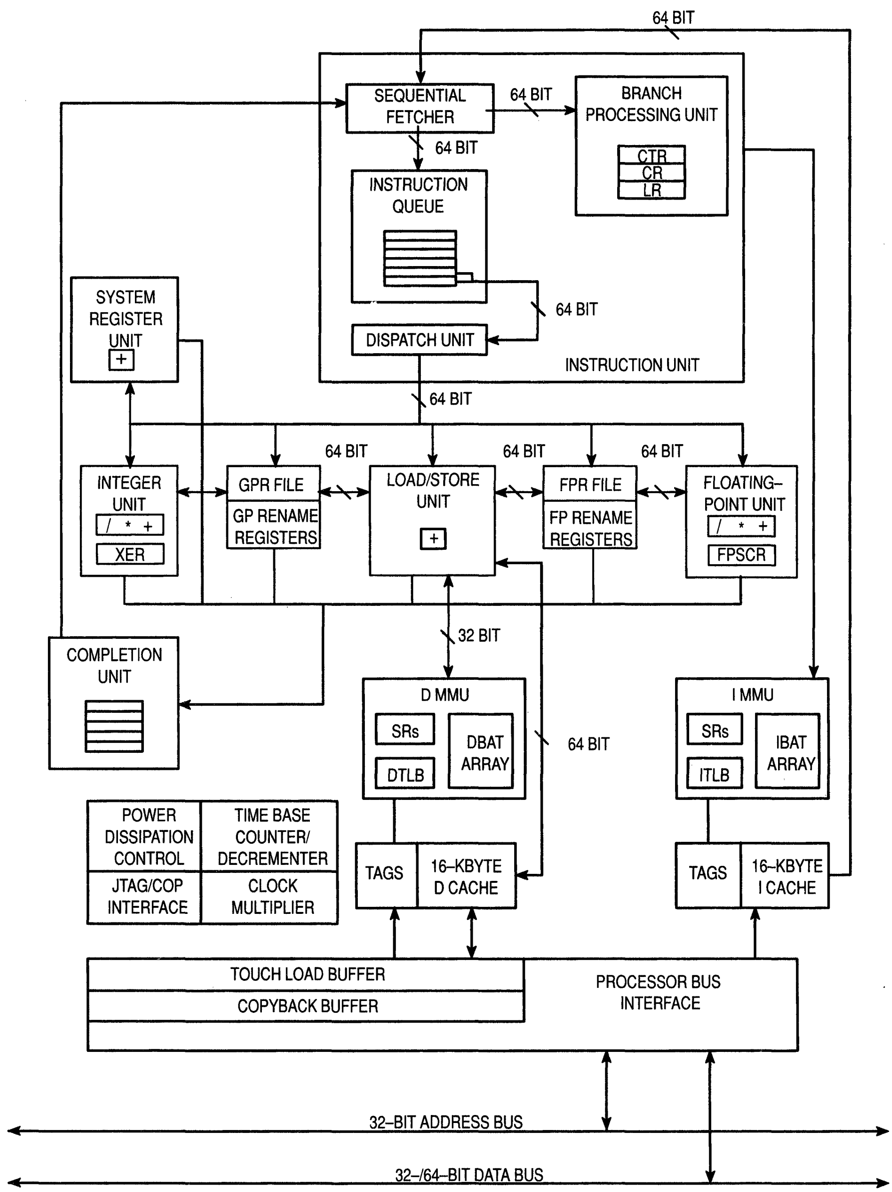


Figure 4. MPC603e Block Diagram

MPC604 RISC Microprocessor

The MPC604 is an implementation of the PowerPC family of RISC microprocessors. The MPC604 implements the PowerPC architecture as it is specified for 32–bit addressing, which provides 32–bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating–point data types of 32 and 64 bits (single–precision and double–precision). For 64–bit PowerPC implementations, the PowerPC architecture provides additional 64–bit integer data types, 64–bit addressing, and related features.

The MPC604 is a superscalar processor capable of issuing four instructions simultaneously. As many as six instructions can finish execution in parallel. The MPC604 has six execution units that can operate in parallel—floating–point unit (FPU), branch processing unit (BPU), load/store unit (LSU), two single–cycle integer units (SCIUs), and one multiple–cycle integer unit (MCIU).

This parallel design, combined with the PowerPC architecture's specification of uniform instructions that allows for rapid execution times, yields high efficiency and throughput. The MPC604's rename buffers, reservation stations, dynamic branch prediction, and completion unit increase instruction throughput, guarantee in–order completion, and ensure a precise exception model. (Note that the PowerPC architecture specification refers to all exceptions as interrupts.)

The MPC604 has separate memory management units (MMUs) and separate 16–Kbyte on–chip caches for instructions and data. The MPC604 implements two 128–entry, two–way set (64–entry per set) associative translation lookaside buffers (TLBs), one for instructions and one for data, and provides support for demand–paged virtual memory address translation and variable–sized block translation. The TLBs and the cache use least–recently used (LRU) replacement algorithms.

The MPC604 has a 64–bit external data bus and a 32–bit address bus. The MPC604 interface protocol allows multiple masters to compete for system resources through a central external arbiter. Additionally, on–chip snooping logic maintains data cache coherency for multiprocessor applications. The MPC604 supports single–beat and burst data transfers for memory accesses and memory–mapped I/O accesses.

The MPC604 uses an advanced, 3.3–V CMOS process technology and is fully compatible with TTL devices.

Block Diagram

Figure 5 provides a block diagram showing features of the MPC604. Note that this is a conceptual block diagram intended to show the basic features rather than an attempt to show how these features are physically implemented on the chip.

MPC604e RISC Microprocessor

The MPC604e is an implementation of the PowerPC family of RISC microprocessors. The MPC604e implements the PowerPC architecture as it is specified for 32–bit addressing, which provides 32–bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating–point data types of 32 and 64 bits (single–precision and double–precision). For 64–bit PowerPC implementations, the PowerPC architecture provides additional 64–bit integer data types, 64–bit addressing, and related features.

The MPC604e is a superscalar processor capable of issuing four instructions simultaneously. As many as seven instructions can finish execution in parallel. The MPC604e has seven execution units that can operate in parallel — floating–point unit (FPU), branch processing unit (BPU), condition register unit (CRU), load/store unit (LSU), two single–cycle integer units (SCIUs), and one multiple–cycle integer unit (MCIU).

This parallel design, combined with the PowerPC architecture's specification of uniform instructions that allows for rapid execution times, yields high efficiency and throughput. The MPC604e's rename buffers, reservation stations, dynamic branch prediction, and completion unit increase instruction throughput, guarantee in–order completion, and ensure a precise exception model. (Note that the PowerPC architecture specification refers to all exceptions as interrupts.)

The MPC604e has separate memory management units (MMUs) and separate 32–Kbyte on–chip caches for instructions and data. The MPC604e implements two 128–entry, two–way set associative translation lookaside buffers (TLBs), one for instructions and one for data, and provides support for demand–paged virtual memory address translation and variable–sized block translation. The TLBs and the cache use least–recently used (LRU) replacement algorithms.

The MPC604e has a 64–bit external data bus and a 32–bit address bus. The MPC604e interface protocol allows multiple masters to compete for system resources through a central external arbiter. Additionally, on–chip snooping logic maintains data cache coherency for multiprocessor applications. The MPC604e supports single–beat and burst data transfers for memory accesses and memory–mapped I/O accesses.

The MPC604e uses an advanced, 2.5–V CMOS process technology and is fully compatible with TTL devices.

Block diagram

Figure 6 provides a block diagram of the MPC604e.

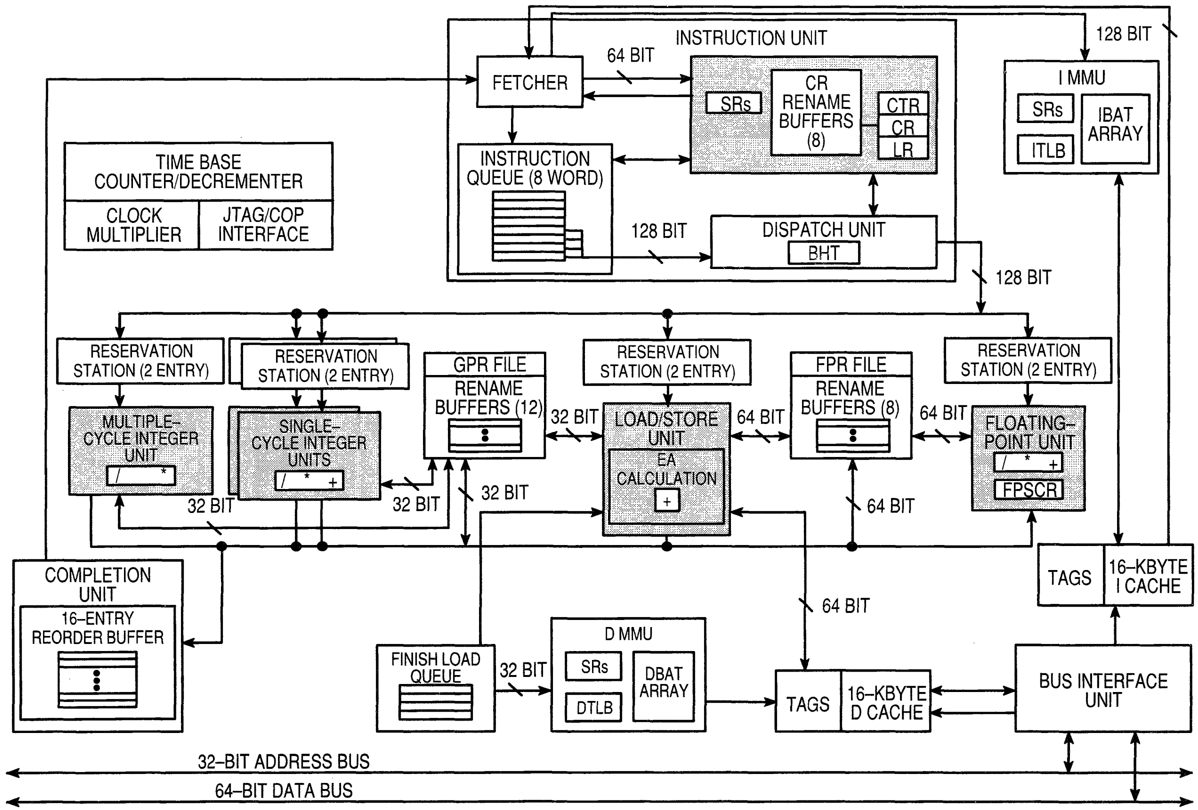


Figure 5. MPC604 Block Diagram

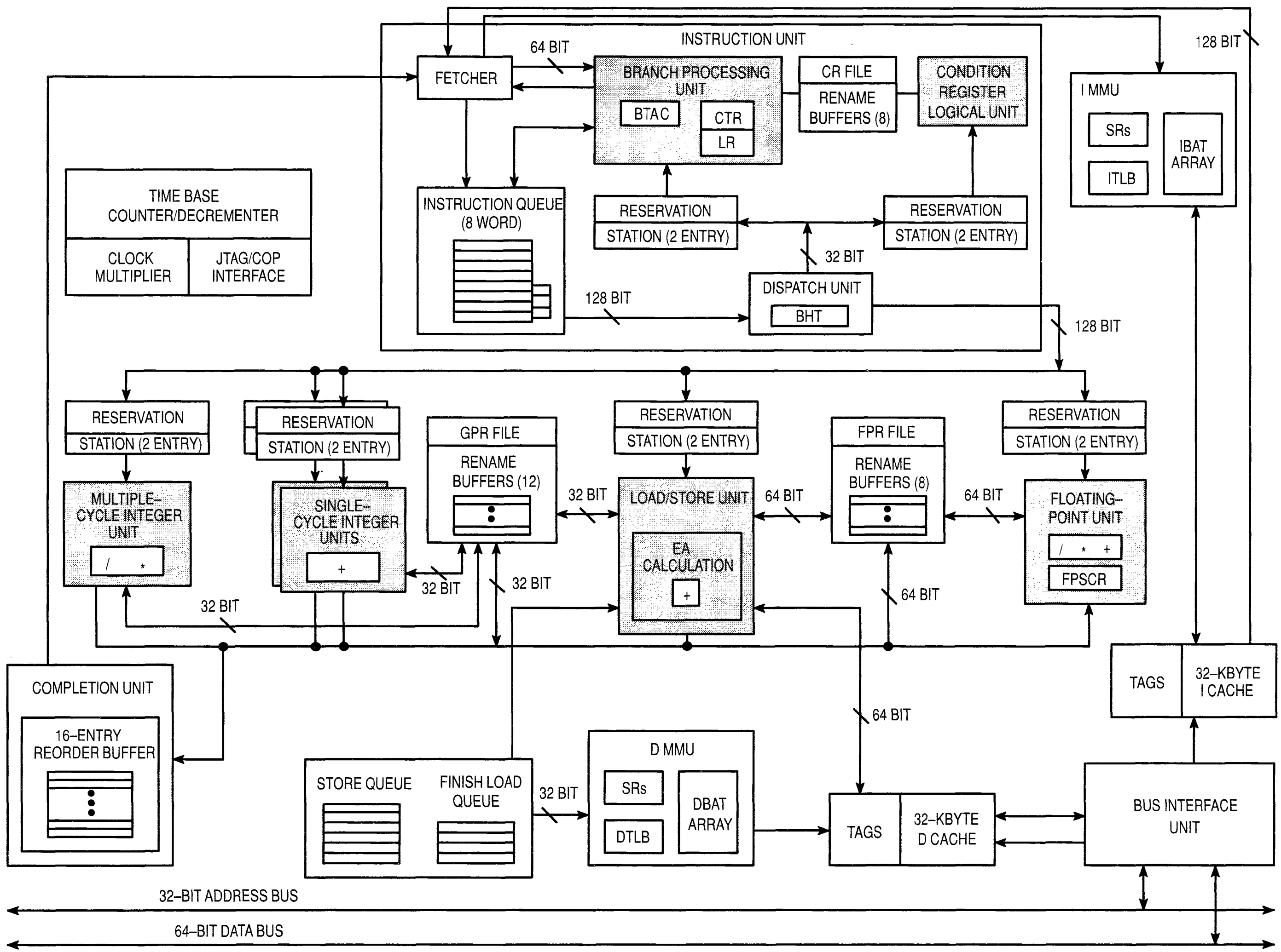


Figure 6. MPC604e Block Diagram

New Features of the MPC604e

Features of the MPC604e that are not implemented in the MPC604 are as follows:

- Additional special–purpose registers
  - HID1 provides four read–only PLL_CFG bits for indicating the processor/bus clock ratio.
  - Three additional registers support the performance monitor—MMCR1 is a second control register that includes bits to support the use of two additional counter registers, PMC3 and PMC4.
- Instruction execution
  - Separate units for branch and condition register (CR) instructions. The BPU is now split into a CR logical unit and a branch unit, which makes it possible for branch instructions to execute and resolve before preceding CR logical instructions. The MPC604e can still only dispatch one CR logical or branch instruction per cycle, but it can execute both branch and CR logical instructions at the same time.
  - Branch correction in decode stage. Branch correction in the decode stage can now predict branches whose target is taken from the count or link registers if no updates of the count and link register are pending. This saves at least one cycle on branch correction when the **mtspr** instruction can be sufficiently separated from the branch that uses the SPR as a target address.
  - Ability to disable the branch target address cache (BTAC)—HID0[30] has been defined to allow the BTAC to be disabled. When HID0[30] is set, the BTAC contents are invalidated and the BTAC behaves as if it were empty. New entries cannot be added until the BTAC is enabled.
- Improvements to cache implementation
  - 32–Kbyte split data and instruction caches. Like the 604, both caches are four–way set associative; however, each cache has twice as many sets, logically separated into 128 sets of odd lines and 128 sets of even lines.
  - Data cache line–fill buffer forwarding. In the 604 only the critical double word of a burst operation was made available to the requesting unit at the time it was burst into the line–fill buffer. Subsequent data was unavailable until the cache block was filled. On the MPC604e, subsequent data is also made available as it arrives in the line–fill buffer.
  - Additional cache copyback buffers. The MPC604e implements three copyback write buffers (as opposed to one in the 604). Having multiple copyback buffers provides the ability for certain instructions to take fuller advantage of the pipelined system bus to provide more efficient handling of cache copyback, block invalidate operations caused by the data cache block flush (**dcbf**) instruction, and cache block clean operations resulting from the data cache block store (**dcbst**) instruction.
  - Coherency support for instruction fetching. Instruction fetching coherency is controlled by HID0[23]. In the default mode, HID0[23] is 0, GBL is not asserted for instruction accesses, as is the case with the 604. If the bit is set, and instruction translation is enabled (MSR[IR] = 1), the GBL signal is set to reflect the M bit for this page or block. If instruction translation is disabled (MSR[IR] = 0), the GBL signal is asserted.
- System interface operation
  - The MPC604e has the same pin configuration as the MPC604; however, on the MPC604e V_{DD} and AV_{DD} must be connected to 2.5 Vdc and OV_{DD} must be connected to 3.3 Vdc. The MPC604e uses split voltage planes, and for replacement compatibility, MPC604/MPC604e designs should provide both 2.5–V and 3.3–V planes and the ability to connect those two planes together and disable the 2.5–V plane for operation with an MPC604.
  - Support for additional processor/bus clock ratios (5:2 and 4:1). Configuration of the processor/bus clock ratios is displayed through a new MPC604e–specific register, HID1.
  - To support the changes in the clocking configuration, different precharge timings for the ABB, DBB, ARTRY, and SHD signals are implemented internally by the processor. The precharge timings for ARTRY and SHD can be disabled by setting HID0[7].
  - No–DRTRY mode. In addition to the normal and fast L2 modes implemented on the 604, a no–DRTRY mode is implemented on the MPC604e that improves performance on read operations for systems that do not use the DRTRY signal. No–DRTRY mode makes read data available to the processor one bus clock cycle sooner than in normal mode. In no–DRTRY mode, the DRTRY signal is no longer sampled as part of a qualified bus grant.
- Full hardware support for little–endian accesses. Little–endian accesses take alignment exceptions for only the same set of causes as big–endian accesses. Accesses that cross a word boundary require two accesses with the lower–addressed word accessed first.
- Additional enhancements to the performance monitor.

MPC620 RISC Microprocessor

The MPC620 is an implementation of the PowerPC™ family of RISC microprocessors. The MPC620 implements the PowerPC architecture as it is specified for 64–bit addressing, which provides 64–bit effective (logical) addresses, integer data types of 8, 16, 32, and 64 bits, and floating–point data types of 32 and 64 bits (single–precision and double–precision). The MPC620 is software compatible with the 32–bit versions of the PowerPC microprocessor family.

The MPC620 is a superscalar processor capable of issuing four instructions simultaneously. As many as six instructions can finish execution in parallel. The MPC620 has six execution units that can operate in parallel — floating–point unit (FPU), branch processing unit (BPU), load/store unit (LSU), two single–cycle integer units (SCIUs), and one multiple–cycle integer unit (MCIU).

This parallel design, combined with the PowerPC architecture's specification of uniform instructions that allows for rapid execution times, yields high efficiency and throughput. The MPC620's rename buffers, reservation stations, dynamic branch prediction, and completion unit increase instruction throughput, guarantee in–order completion, and ensure a precise exception model.

The MPC620 has separate memory management units (MMUs) and separate 32–Kbyte on–chip caches for instructions and data. The MPC620 implements a 128–entry, two–way set–associative translation lookaside buffer (TLB) for instructions and data, and provides support for demand–paged virtual memory address translation and variable–sized block translation. The TLB and the cache use least–recently used (LRU) replacement algorithms.

The MPC620 has a 40–bit address bus, and can be configured with either a 64– or 128–bit data bus. The MPC620 interface protocol allows multiple masters to compete for system resources through a central external arbiter. Additionally, on–chip snooping logic maintains data cache coherency for multiprocessor applications. The MPC620 supports single–beat and burst data transfers for memory accesses and memory–mapped I/O accesses.

The MPC620 uses an advanced, 3.3–V CMOS process technology and is compatible with 3.3–V CMOS devices.

Block Diagram

Figure 7 provides a block diagram showing features of the MPC620. Note that this is a conceptual block diagram intended to show the basic features rather than an attempt to show how these features are physically implemented on the chip.

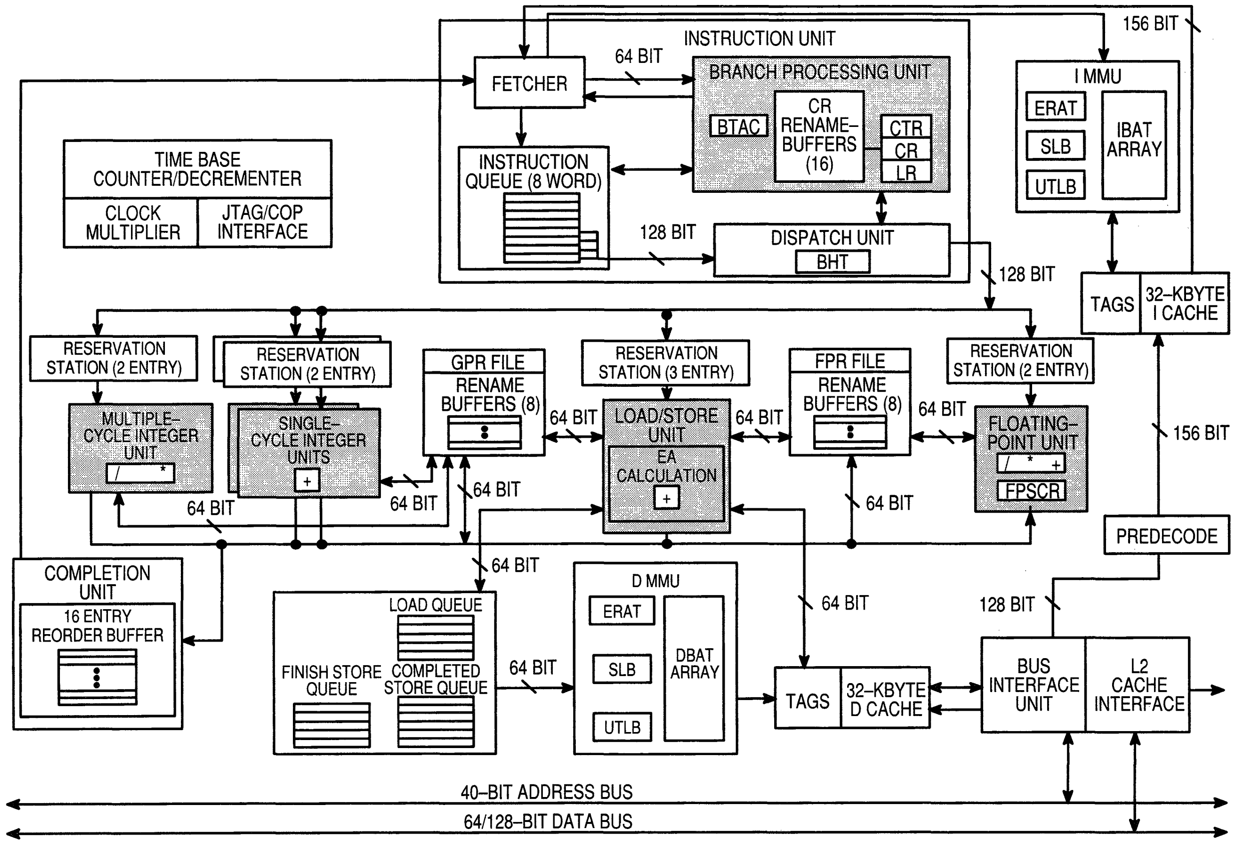


Figure 7. MPC620 Block Diagram

MPC105 PCI Bridge/Memory Controller

The MPC105 PCI bridge/memory controller (PCIB/MC) provides a PowerPC reference platform–compliant bridge between the PowerPC microprocessor family and the peripheral component interconnect (PCI) bus. PCI support allows system designers to rapidly design systems using peripherals already designed for PCI and the other standard interfaces available in the personal computer hardware environment. The MPC105 integrates secondary cache control and a high–performance memory controller that supports DRAM, SDRAM, ROM, and Flash ROM. The MPC105 uses an advanced, 3.3–V CMOS process technology and is fully compatible with TTL devices.

The MPC105 provides an integrated high bandwidth, high performance, TTL–compatible interface between a 60x processor, a secondary (L2) cache or secondary 60x processor, the PCI bus, and main memory.

The MPC105 supports a programmable interface to a variety of PowerPC microprocessors operating at various bus speeds. The 60x processor interface uses a subset of the 60x bus protocol, which enables the interface between the processor and MPC105 to be optimized for performance. The MPC105's 60x interface allows for a variety of system configurations by providing support for either a direct–mapped, lookaside, L2 cache or a secondary 60x processor. The L2 cache interface generates the arbitration and support signals necessary to maintain a write–through or write–back L2 cache. The L2 cache interface supports either burst SRAMs or asynchronous SRAMs, and L2 data a per–byte basis. The MPC105 features on–chip byte decoding for L2 data write enables or can be configured to use external logic for data write enable generation.

The PCI interface connects the processor and memory buses to the PCI bus, to which I/O components are connected, without the need for "glue" logic. This interface acts as both a master and slave device.

The memory interface controls processor and PCI interactions to main memory. It is capable of supporting a variety of DRAM or SDRAM, and ROM or Flash ROM configurations as main memory. The maximum supported memory size is 1 Gbyte of DRAM or SDRAM, with 16 Mbytes of ROM or 1 Mbyte of Flash ROM.

The MPC105 provides hardware support for four levels of power reduction; the doze, nap, and sleep modes are invoked by register programming, and the suspend mode is invoked by assertion of an external signal. The design of the MPC105 is fully static, allowing internal logic states to be preserved during all power saving modes. The following sections describe the programmable power modes provided by the MPC105.

Block Diagram

Figure 8 shows the MPC105 in a typical system implementation. The major functional units within the MPC105 are also shown in Figure 1. Note that this is a conceptual block diagram intended to show the basic features rather than an attempt to show how these features are physically implemented on the device.

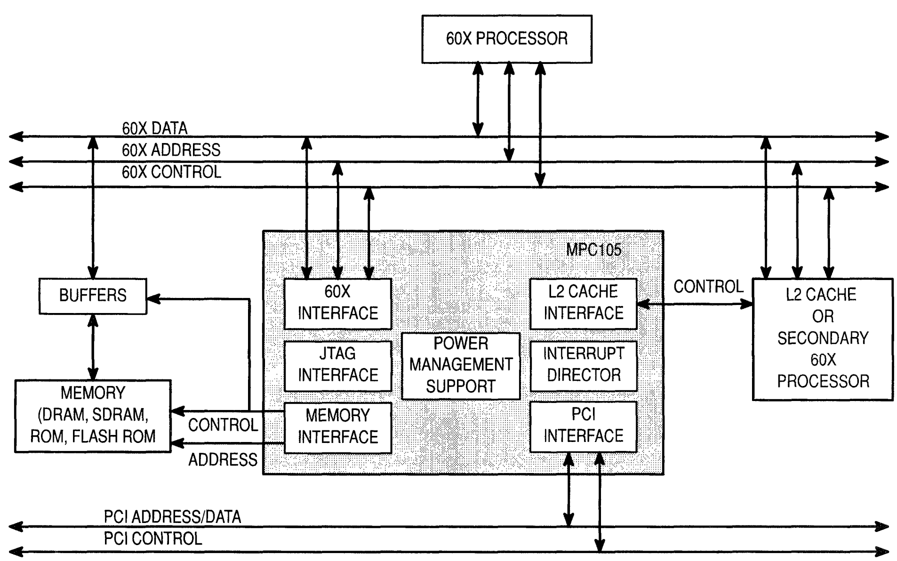


Figure 8. System Implementation and Block Diagram

MPC106 PCI Bridge/Memory Controller

The MPC106 provides a PowerPC common hardware reference platform (CHRP) compliant bridge between the PowerPC microprocessor family and the Peripheral Component Interconnect (PCI) bus. PCI support allows system designers to rapidly design systems using peripherals already designed for PCI and the other standard interfaces available in the personal computer hardware environment. The MPC106 integrates secondary cache control and a high–performance memory controller. The MPC106 uses an advanced, 3.3–V CMOS process technology and is fully compatible with TTL devices.

The MPC106 provides an integrated high–bandwidth, high–performance, TTL–compatible interface between a 60x processor, a secondary (L2) cache or secondary 60x processor, the PCI bus, and main memory.

60x Processor Interface

The MPC106 supports a programmable interface to a variety of PowerPC microprocessors operating at select bus speeds. The 60x processor interface of the MPC106 uses a subset of the 60x bus protocol, supporting single–beat and burst data transfers. The address bus is 32 bits wide and the data bus is 64 bits wide. The address and data buses are decoupled to support pipelined transactions. PCI bus accesses to system memory space are passed to the 60x processor bus for snooping purposes. Two signals on the MPC106, LBCLAIM, and DBGLB, are provided for an optional local bus slave. The local bus slave must be capable of generating AACK and TA signals to interact with the 60x processor(s). Depending on the system implementation, the processor(s) may operate at the PCI bus clock rate, or at two or three times the PCI bus clock rate. The bus is synchronous, with all timing relative to the rising edge of the bus clock.

L2 Cache/Multiple Processor Interface

The MPC106 provides support for the following configurations of 60x processors and L2 cache:

- A single 60x processor with no L2 cache
- A single 60x processor plus a direct–mapped, lookaside, L2 cache
- A single 60x processor plus an external L2 cache controller or integrated L2 cache module such as the Motorola MPC2604GA integrated L2 lookaside cache
- Two 60x processors with no L2 cache
- Two 60x processors plus an external L2 cache controller or integrated L2 cache module such as the Motorola MPC2604GA integrated L2 lookaside cache

The internal L2 cache controller generates the arbitration and support signals necessary to maintain a write–through or write–back L2 cache. The internal L2 cache controller supports either asynchronous SRAMs, pipelined burst SRAMs, or synchronous burst SRAMs, using byte parity for data error detection. When a second 60x processor is used, three signals of the L2 interface (BR1, BG1, and DBG1) change their functions to allow for arbitration between the 60x processors. All 60x interface signals of the MPC106, except the bus request, bus grant, and data bus grant signals, are shared by the 60x processors. When an external L2 controller (or integrated L2 cache module) is used, three signals of the L2 interface (BRL2, BGL2, and DBGL2) change their functions to allow the MPC106 to arbitrate between the external cache and the 60x processor(s).

Memory Interface

The memory interface controls processor and PCI interactions to main memory and is capable of supporting a variety of DRAM, or extended data–out (EDO) DRAM and ROM or Flash ROM configurations as main memory. The maximum supported memory size is 1 Gbyte of DRAM or EDO DRAM, with 16 Mbytes of ROM or Flash ROM. The memory controller of the MPC106 supports the various memory sizes through software initialization of on–chip configuration registers. Parity or ECC is provided for error detection.

PCI Interface

The MPC106's PCI interface is compliant with the PCI *Local Bus Specification, Revision 2.1,* and follows the guidelines in the *PCI System Design Guide, Revision 1.0* for host bridge architecture. The PCI interface connects the processor and memory buses to the PCI bus, to which I/O components are connected. The PCI bus uses a 32–bit multiplexed address/data bus, plus various control and error signals.

Figure 9 shows the major functional units within the MPC106. Note that this is a conceptual block diagram intended to show the basic features rather than an attempt to show how these features are physically implemented on the device.

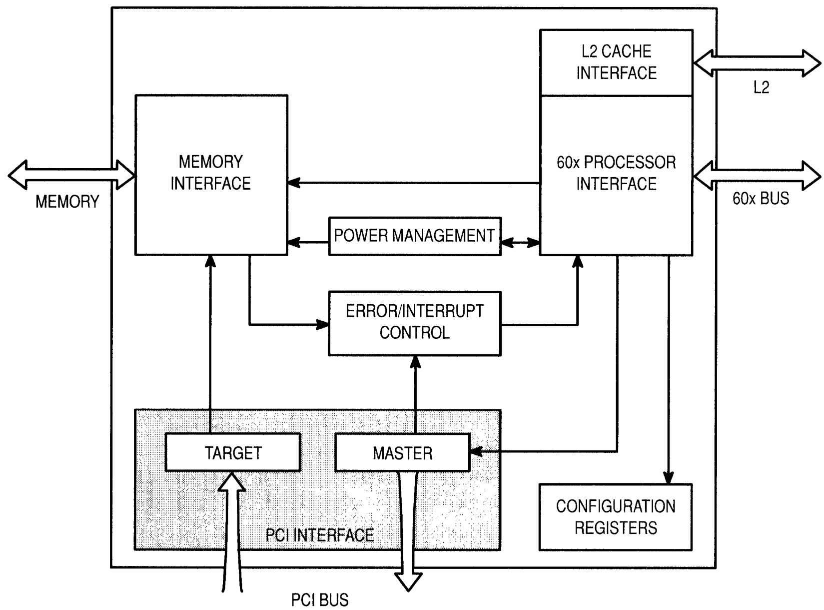


Figure 9. MPC106 Block Diagram

Single–Chip Microcontrollers (CSIC)

In Brief . . .

Motorola offers the most comprehensive selection of high–performance single–chip control systems available from a single source. Microcontroller device families range from industry–standard 8–bit controllers to state–of–the–art 16– and 32–bit modular controllers. Within the price and performance categories of each family, there are a variety of on–chip capabilities to match specific applications.

Motorola device families are structured so that upward migration need not involve complete code development. The M68HC11 Family is upward code compatible with M6800 and M6801 software, while the M68HC16 family is source–code compatible with the M68HC11 family. Motorola's newest 8–bit MCU product line, the M68HC08 family, is fully upward object code compatible with the M68HC05 and M6805 families. In addition, M68300 and M68HC16 devices share standard internal modules and bus configurations.

M68HC05 CSIC Family

It all started with the 68HC05 Family, and Motorola's CSIC (Customer–Specified Integrated Circuits) approach to microcontroller design. Today, customers can select from over 70 mask ROM 68HC05 devices and over 30 one–time programmable (OTP) 68HC705 devices — and that number is growing all the time, as Motorola continues to develop derivatives of the 68HC05 based on customer demand.

With so many standard 68HC05 microcontrollers from which to choose, most customers will find the right device for an application among these existing devices. For some high–volume applications, however, a customer may opt for Motorola to develop a new derivative to meet an application's precise requirements. The result is a new microcontroller which can then be added to the selection of standard devices.

M68HC05 Industry Solutions

Motorola's 68HC05 and 68HC08 Families consist of a variety of microcontroller designs to meet the requirements of a broad range of applications. The 68HC05 Family, already over 100 devices strong, offers a wide range of standard products from which to choose, while the flagship 68HC08 offers a large library of modules from which derivatives can be developed.

68HC05 General–Purpose Microcontrollers

68HC05 C–Family. These flexible, general–purpose devices feature a wide variety of memory options capable of handling complex programs. On–chip SCI provides asynchronous communications, with software–selectable baud rates from 75 Hz to 131 kHz. The high–speed, synchronous 4–wire serial system SPI is ideal for driving off–chip displays and peripherals.

All C–Family devices include a powerful 16–bit free–running programmable counter in conjunction with input capture and output compare functions for simultaneous input waveform measurement and output waveform generation. A watchdog timer guards against runaway software in noisy environments.

The high–packing density of Motorola's HCMOS process allows standard devices to run at bus frequencies up to 2.1 MHz. Motorola also offers high–speed versions which run at frequencies up to 4.2 MHz from an 8.4 MHz crystal or external clock. Low–voltage versions are available for applications requiring extremely low power consumption to extend battery life or minimize heat dissipation.

68HC05 J–Family. This 20–pin family provides a low–cost, low pin count, 8–bit upgrade for existing 4–bit applications. It combines a powerful 68HC05 CPU with a flexible, 15–stage multifunction timer and real–time interrupt capability.

68HC05 K–Family. Our lowest–cost family offers a 16–pin count and is appropriate for logic replacement.

68HC05 P–Family. Born out of the CSIC design concept, this family offers an extremely cost–competitive 28–lead family of microcontrollers with a variety of ROM sizes and special features such as Serial Input/Output Port (SIOP) to control display drivers and communicate with other peripherals. Other options include A/D input and on–chip EEPROM for non–volatile data storage. Low–voltage and high–speed versions are also available.

The flagship 68HC(7)08XL36 OTP and ROM versions are the first two devices in the 68HC08 Family and are intended for general purpose uses.

Low–Voltage Microcontrollers

The 68HC05 Family has been capable of 3.0 V operation since 1980 and includes some 2.2 V selections. Recently, Motorola announced several 68HC05 microcontrollers capable of 1.8 Vdc and 500 kHz operation. This new low–voltage capability affords a greater than threefold power savings over 3.0 V versions of the same chips, a significant design consideration for any portable electronic application. The new devices are collectively designated 68HCL05 and include the following versions: 68HCL05C4, C8, C12, J1A, K0, P1, and P4. They are designed to provide lower–power control technology to accommodate trends in portable applications toward compactness, lightweight design, and extended battery life.

Automotive

68HC05 B–Family. EEPROM memory in these devices makes it possible to store information that must be retained after the power is removed. Applications include electric seat control (storage of seat positions) and audio systems (storage of radio stations).

68HC05 C– and D–Families. These general–purpose microcontrollers are used for cruise control, ignition systems, and in–car entertainment systems.

68HC05 J–, K–, and P–Families. With their low pin count and low cost, these devices are ideal for automotive applications such as car alarms, power windows, keyless entry, and air bags.

68HC05 V– and X–Families. Both these groups contain integrated automotive multiplex interfaces that allow them to talk to other electronic modules within a vehicle. The V series adds an on–chip voltage regulator.

Computer

68HC05 BD–Family. These devices are ideal for computer monitor applications. They include a horizontal and vertical sync processor as well as 16 channels of pulse–width modulation.

68HC05 C–Family. These are general purpose devices for keyboard and monitor control.

68HC05 J–, P–, and E–Families. These low–cost, low pin count devices are appropriate for applications like a cordless PC mouse and trackball.

Consumer

68HC05 C– and D–Families. The multiple communication lines (I/O ports, SCI and SPI) and free–running timer in this group of devices make it possible to execute several tasks in parallel. These features are used in consumer products like CD players, automotive entertainment systems, and remote controls.

68HC05 J–, K–, and P–Families. The free–running timer in these cost–effective microcontrollers allows multitasking in applications such as washing machines, oven controls, and remote controls.

68HC05 L–Family. These low–power, small–footprint devices can drive large LCD displays, making them ideal for hand–held consumer products like portable CD players.

Industrial

68HC05 B–Family. On–chip features include EEPROM; 8–channel, 8–bit A/D converter; and Pulse Length Modulated outputs. Typical industrial applications include Programmable Logic Controllers (PLC) and data acquisition systems.

68HC05 C– and D–Families. These general–purpose devices can be used in applications such as process control systems where multiple I/O lines and LED outputs are required.

68HC05 J– and P–Families. These devices are popular in low–cost industrial applications such as smoke detectors, security devices, thermostats, and furnace ignition systems.

68HC05 L–Family. Multi–port controllers with LCD driver, 16–bit timer and watchdog timer on board. Excellent for display panels requiring tone output and low power consumption such as thermostats and alarms.

68HC705MC4. This device is intended for use in industrial motor control and power supply applications.

68HC05 X–Family. These devices have Controlled Area Network (CAN) controllers with 4K thru 32K ROM for integrated messaging on factory automation, sensor, and switch applications.

Telecommunications

68HC05 B–Family. These devices can store user–programmable telephone numbers in 256 bytes of non–volatile EEPROM memory. They can also communicate with analog inputs like battery life in hand–held equipment, using the A/D module. The D/A module can be used to control analog outputs such as telephone volume and line cards.

68HC05 C–Family. This group of microcontrollers has proven useful as a general–purpose device for communications applications.

68HC05 E–Family. Like the 68HC05 B–Series devices, E–Series devices are ideal for number storage and keyboard interrupt applications.

68HC05 F–Family. These devices — except for the F5, which features an integrated DTMF receiver — include an on–chip Dual–Tone Multi–Frequency Generator (DTMG) for digital transmission and reception, as well as an LED drive for user information. These features make the F–Family suitable for a number of telecommunications applications, including auto dialing, number storage, and display control.

68HC05 J– and P–Families. These low pin count, low–cost microcontrollers have a variety of telecommunications uses, with features ranging from EEPROM to multifunction timers.

68HC05 L–Family. With its large LCD driving capability and low power consumption, this series is well–suited to applications in hand–held communication equipment. The on–chip tone generator and display functions can be used in pager systems to alert users to incoming messages.

Television and Video

68HC05 B–Family. These devices are ideal for EEPROM storage, with 256 bytes of EEPROM to store TV or satellite channel frequencies and preset volume or brightness levels. Features include Analog–to–Digital (A/D) conversion and PWM.

68HC05 C– and D–Families. With up to 32K of user ROM, these devices can be used in the television and video market as general–purpose microcontrollers.

68HC05 CC–Family. Evolved from the T–Series, CC–Series devices feature closed–caption Data Slicer (DSL) and enhanced OSD features for decoding and displaying closed captions.

68HC05CO. This device has no on–chip user ROM, but is capable of addressing up to 64K of external memory, making it ideal for applications that require large amounts of operating code, like televisions. The I^2C bus module and 4 MHz internal bus speed also allow interconnection with standard TV peripherals.

68HC05 K– and RC–Families. These devices are used in remote control applications.

68HC05 T–Family. All T–Family devices have On Screen Display (OSD) modules that can overlay graphical images onto television screens. They also contain D/A converters that can drive analog outputs like volume control, and A/D converters that can be used to automatically adjust the fine tuning. Some members of the T–Series have I^2C interfaces that can communicate with industry–standard TV peripherals.

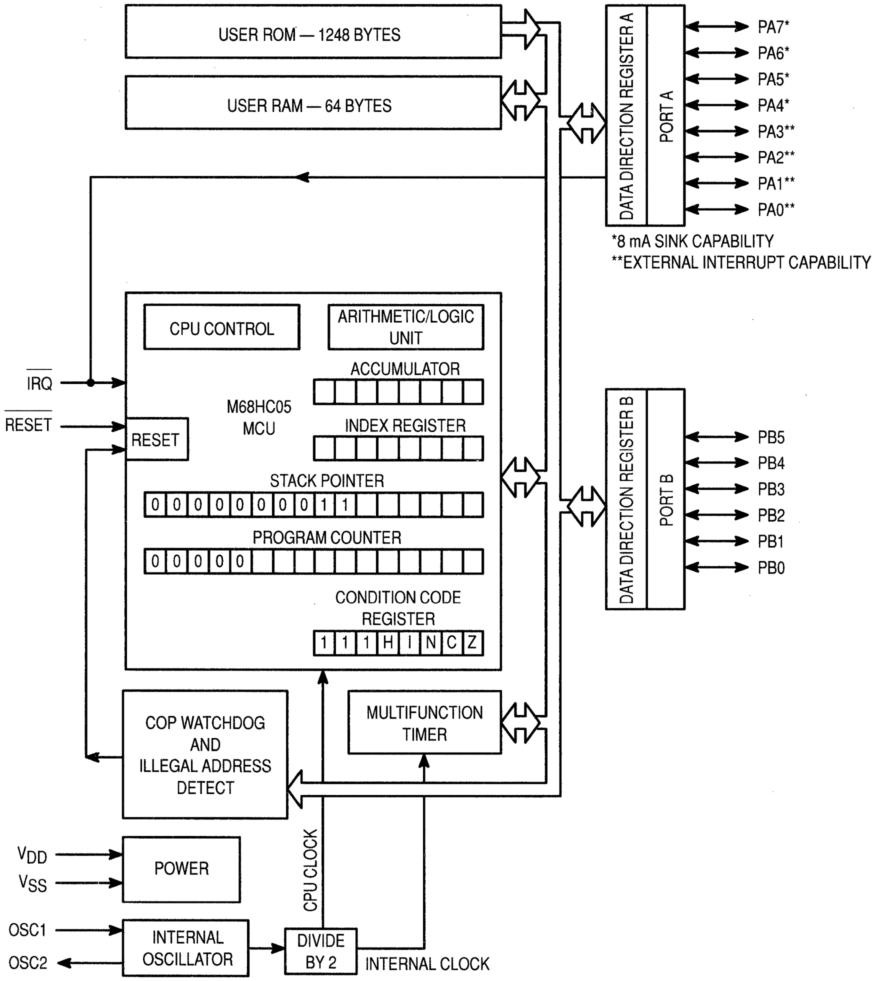


Figure 1. MC68HC05J1A Block Diagram

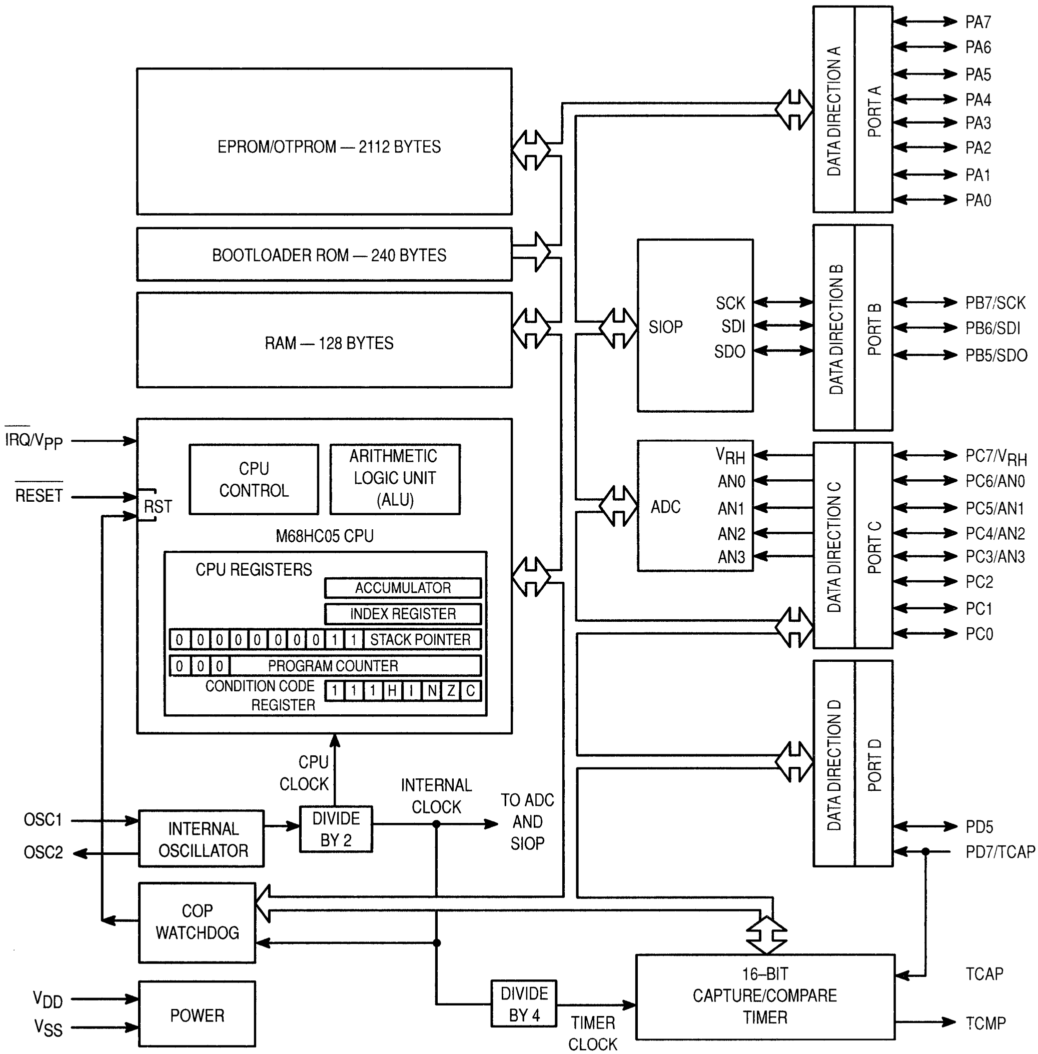


Figure 2. MC68HC705P9 Block Diagram

68HC05 MICROCONTROLLERS

All 68HC05 products have a standard operating voltage range from 3 V to 5.5 V unless noted in Comments.
All 68HC05 products have a standard operating temperature range from 0 – 70°C.
Contact a Motorola Sales Office for availability of extended temperature versions.

Table 5. 68HC05 Microcontrollers

Motorola Part Number	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	Serial	A/D	PWM	Display Drive	I/O	COP	Comments	Packages
MC68HC05B4	4K	176		16–bit: (2IC, 2OC)	SCI+	8 ch (8–bit)	2 ch (8–bit)		24 i/o 8 i 2 o	✔		56 SDIP – B 52 PLCC – FN 64 QFP – FU
MC68HC05B6	6K	176	256	16–bit: (2IC, 2OC)	SCI+	8 ch (8–bit)	2 ch (8–bit)		24 i/o 8 i 2 o	✔	On–Chip Charge Pump EEPROM Write Protect	56 SDIP – B 52 PLCC – FN 64 QFP – FU
MC68HC05B8	7.25K	176	256	16–bit: (2IC, 2OC)	SCI+	8 ch (8–bit)	2 ch (8–bit)		24 i/o 8 i 2 o	✔	On–Chip Charge Pump EEPROM Write Protect	56 SDIP – B 52 PLCC – FN 64 QFP – FU
MC68HC05B16	15K	352	256	16–bit: (2IC, 2OC)	SCI+	8 ch (8–bit)	2 ch (8–bit)		24 i/o 8 i 2 o	✔	On–Chip Charge Pump EEPROM Write Protect	56 SDIP – B 52 PLCC – FN 64 QFP – FU
MC68HC05BD3	3.75K	128		MFT, RTI	I^{2}C		16 ch (8–bit)		24 i/o	✔	Horizontal and Vertical Sync Signal Processor	40 DIP – P 42 SDIP – B
MC68HC05C4A	4K	176		16–bit: (1IC, 1OC)	SPI SCI				24 i/o 7 i	✔	KBI (8 pins) 1 High Current Pin (5 mA sink) Mask Option Pullups High Speed Option (HSC05C4A) Low Power Option (HCL05C4A) (1.8 V minimum)	40 DIP – P 44 PLCC – FN 44 QFP – FB 42 SDIP – B
MC68HC05C5	5K	176	128	16–bit: (1IC, 1OC)	SIOP				32 i/o	✔	8 High Current Pins (10 mA sink) LVPI, On–Chip Charge Pump	40 DIP – P 44 PLCC – FN
MC68HC05C8A	8K	176		16–bit: (1IC, 1OC)	SPI SCI				24 i/o 7 i	✔	KBI (8 pins) 1 High Current Pin (5 mA sink) Mask Option Pullups High Speed Option (HSC05C8A) Low Power Option (HCL05C8A) (1.8 V minimum)	40 DIP – P 44 PLCC – FN 44 QFP – FB 42 SDIP – B
MC68HC05C9A	16K	352		16–bit: (1IC, 1OC)	SPI SCI				24 i/o 7 i	✔	KBI (8 pins) 1 High Current Pin (5 mA sink) Mask Option Pullups High Speed Option (HSC05C9A) Low Power Option (HCL05C9A)	40 DIP – P 44 PLCC – FN 44 QFP – FB 42 SDIP – B
MC68HC05C12	12K	176		16–bit: (1IC, 1OC)	SCI SPI				24 i/o 7 i	✔	1 High Current Pin (20 mA sink) KBI (8 pins) Mask Option Pullups (8 pins) High Speed Option (HSC05C12) Low Power Option (HCL05C12): (1.8 V minimum)	40 DIP – P 44 PLCC – FN 44 QFP – FB 42 SDIP – B
MC68HC05CC1	16K	544		8–bit: Pulse Accum, MFT	I^{2}C	1 ch (5–bit)	8 ch (6–bit)	OSD (127 Char ROM)	31 i/o		Closed Caption Television NTSC Data Slicer w/int Sync Sep 28 MHz PLL 8 Open Drain I/O Pins, 5 V Only	40 DIP – P 42 SDIP – B
MC68HC05CC2	31.5K	928		8–bit: Pulse Accum, MFT	I^{2}C	1 ch (5–bit)	8 ch (6–bit)	OSD (127 Char ROM)	31 i/o		Closed Caption Television NTSC Data Slicer w/int Sync Sep 32 MHz PLL 8 Open Drain I/O Pins, 5 V Only	42 SDIP – B 40 DIP – P
MC68HC05CJ4	4K	224		16–bit: (1IC, 1OC) MFT	SPI SCI I^{2}C				24 i/o	✔	I^{2}C (Slave Only)	44 QFP – FB
MC68HC05D9	16K	352		16–bit: (1IC, 1OC)	SCI		5 ch (6–bit)		31 i/o	✔	8 High Current Pins (25 mA sink) 30 kHz PWM	40 DIP – P 44 PLCC – FN
MC68HC05D24	24K	352		16–bit: (1IC, 1OC)	SCI		5 ch (6–bit)		31 i/o	✔	8 High Current Pins (24 mA sink) 30 kHz PWM	40 DIP – P 44 PLCC – FN
XC68HC05D32	32K	352		16–bit: (1IC, 1OC)	SCI		5 ch (6–bit)		31 i/o	✔	8 High Current Pins (24 mA sink) 30 kHz PWM	40 DIP – P 44 PLCC – FN
MC68HC05E1	4K	368		MFT, RTI					20 i/o	✔	32 kHz PLL Clock Synthesizer	28 DIP – P 28 SOIC – DW
MC68HC05E6	6K	128	160	16–bit: (1IC, 1OC) MFT, RTI		4 ch (8–bit)			32 i/o 4 i	✔	KBI (8 pins) Pin for External LVI	44 QFP – FB 28 SOIC – DW

Table 5. 68HC05 Microcontrollers (continued)

Motorola Part Number	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	Serial	A/D	PWM	Display Drive	I/O	COP	Comments	Packages
MC68HC05F5	5K	224		MFT, RTI					30 i/o 1 i	✔	DTMF Receiver Mask IRQ	40 DIP – P 44 PLCC – FN
MC68HC05F6	4K	320		16–bit: (1IC, 1OC)	SPI				26 i/o 4 i 2 o		DTMF Generator 8 High Current Pins (10 mA sink) KBI (6 pins)	42 SDIP – B 44 QFP – FB
MC68HC05F8	8K	320		16–bit: (1IC, 1OC) 16–bit: auto	SPI				50 i/o 2 o	✔	DTMF Generator KBI (8 pins) Manchester Encoder/Decoder 8 High Current Pins (10 mA sink)	64 QFP – FU
MC68HC05G1	8K	176		16–bit: (1IC, 1OC) RTC	SPI	4 ch (8–bit)			40 i/o 8 i	✔	32 kHz PLL – Standby modes	56 SDIP – B 64 QFP – FU
MC68HC05G3	24K	768		16–bit: (1IC, 1OC) 8–bit: Event Cntr	Dual SPI	8 ch (8–bit)	4 ch (8–bit)		48 i/o 16 i 4 o	✔	KBI (8 pins) Dual Oscillators – Selectable Clock Dual IRQ	80 QFP – FU
MC68HC05J1A	1.2K	64		MFT, RTI					14 i/o	✔	KBI (4 pins) 4 High Current Pins (8 mA sink) Mask Option Pulldowns (14 pins) High Speed Version (HSC05J1A) Low Power Version (HCL05J1A): (1.8 V minimum)	20 DIP – P 20 SOIC – DW
MC68HC05J3	2K	128		16–bit: (1IC, 1OC) MFT, RTI					14 i/o	✔	14 High Current Pins (8 mA sink) KBI (4 pins)	20 DIP – P 20 SOIC – DW
MC68HC05K0	0.5K	32		MFT, RTI					10 i/o	✔	4 High Current Pins (8 mA sink) Programmable Pulldowns (10 pins) Low Voltage Reset Mask Option Low power version (HCL05K0): (1.8 V minimum)	16 DIP – P 16 SOIC – DW
MC68HC05K1	0.5K	32		MFT, RTI					10 i/o	✔	4 High Current Pins (8 mA sink) PEP (64 bits) Programmable Pulldowns (10 pins) Low Voltage Reset Mask Option	16 DIP – P 16 SOIC – DW
XC68HC05K3	920	64	16 PEEP	MFT, RTI					10 i/o	✔	KBI (4 pins), Programmable Pulldowns (10 pins) 4 High Current Pins (8 mA sink) On–Chip Charge Pump 1.8 V Operating Voltage	16 DIP – P 16 SOIC – DW
MC68HC05L1	4K	128		16–bit: (2IC, 2OC)		6 ch (8–bit)		64 Segment LCD: (3/4 x 12/16)	17 i/o 15 i 2 o			56 SDIP – B 64 QFP – FU
MC68HC05L2	2K	96		16–bit: (1IC, IOC) MFT, RTI		1 ch (8–bit)		45 Segment LCD: (3 x 15)	13 i/o	✔	Programmable Pullups (13 pins)	42 SDIP – B
MC68HC05L5	8K	256		16–bit: (1IC, 1OC) RTI 8–bit: (1IC, 1OC)	SIOP			156 Segment LCD: (1–4 x 27–39)	14 i/o 10 i 15 o	✔	KBI (8 pins), Dual Oscillators 8 High Current Pins (10 mA sink) Programmable Pullups (24 pins), Open Drain (31 pins), 2.2 V	80 QFP – FU
MC68HC05L7	6K	176		16–bit: (1IC, 1OC) RTC	SCI			960 Segment LCD: (8/16 x 60)	15 i/o		Mux EBI (13–bit Address), 32 kHz PLL, KBI (8 pins), LVI Tone Generator	128 QFP – FT Die
MC68HC05L9	6K	176		16–bit: (1IC, 1OC) RTC	SCI			640 Segment LCD: (8/16 x 40)	27 i/o 2 i		Mux EBI (16–bit Address), 32 kHz PLL, KBI (8 pins), LVI Expand LCD to 3K Segments w/68HC68L9, Tone Generator	128 QFP – FT Die
MC68HC05L10	13K	352		16–bit: (1IC, 1OC) RTC	SPI SCI			5K–20K Pixel LCD	28 i/o		Mux EBI w/MMU (20–bit Address) 4 Chip Selects, KBI (8 pins) Tone Generator/DTMF, 32 kHz PLL LCD Expansion w/MC141511	128 QFP – FT Die

Table 5. 68HC05 Microcontrollers (continued)

Motorola Part Number	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	Serial	A/D	PWM	Display Drive	I/O	COP	Comments	Packages
MC68HC05L11	3K	448		16–bit: (1IC, 1OC) RTC	SPI SCI			Up to 40K Pixel LCD	38 i/o		Mux EBI w/MMU (23–bit Address) 4 Chip Selects, KBI (8 pins) Tone Generator/DTMF, 32 kHz PLL LCD Expansion with MC141512 + MC141514	100 QFP – FU
MC68HC05L16	16K	512		16–bit: (1IC, 1OC) RTI 8–bit: (1IC, 1OC)	SIOP			156 Segment LCD: (1–4 x 27–39)	16 i/o 8 i 15 o	✔	KBI (8 pins), Dual Oscillators 8 High Current Pins (10 mA sink) Programmable Pullups (24 pins) Open Drain (31 pins), 2.2 V Operation	80 QFP – FU
MC68HC05M4	4K	128		16–bit: (1IC, 1OC) 8–bit Modulo		6 ch (8–bit)		VFD (24 lines)	32 i/o 8 i	✔	5 V Only	52 PLCC – FN
MC68HC05P1A	2K	128		16–bit: (1IC, 1OC)					20 i/o 1 i	✔	KBI (8 pins) Mask Option Pullups (8 pins) 2 High Current Pins (20 mA)	28 DIP – P 28 SOIC – DW
MC68HC05P3	3K	128	128	16–bit: (1IC, 1OC) MFT, RTI					22 i/o	✔	KBI (6 pins) On–Chip Charge Pump	28 DIP – P 28 SOIC – DW
MC68HC05P4	4K	176		16–bit: (1IC, 1OC)	SIOP				20 i/o 1 i	✔	High Speed Option (68HSC05P4) Low Power Option (68HCL05P4): (1.8 V minimum)	28 DIP – P 28 SOIC – DW
MC68HC05P6	4.5K	176		16–bit: (1IC, 1OC)	SIOP	4 ch (8–bit)			20 i/o 1 i	✔		28 DIP – P 28 SOIC – DW
MC68HC05P7	2K	128		16–bit: (1IC, 1OC)	SIOP				20 i/o 1 i	✔		28 DIP – P 28 SOIC – DW
MC68HC05P8	2K	112	32	MFT, RTI		4 ch (8–bit)			16 i/o 4 i	✔	LVPI Option on EEPROM On–Chip Charge Pump	28 DIP – P 28 SOIC – DW
MC68HC05P9	2K	128		16–bit: (1IC, 1OC)	SIOP	4 ch (8–bit)			20 i/o 1 i	✔		28 DIP – P 28 SOIC – DW
MC68HC05PE0	2K	128		16–bit: (1IC, 1OC)					20 i/o	✔	1 High Current Pin (20 mA sink) PEP (64 bits), KBI (8 pins) Mask Option Pulldowns (8 pins) RC Oscillator Option	28 DIP – P 28 SOIC – DW
XC68HC05RC16	16K	350		Infrared Timer					12 i/o	✔	Mask Option Pullups (12 pins) KBI (12 pins), Low Power Stop Pin	28 DIP – P 28 SOIC – DW
MC68HC05SC11	6K	128							5 i/o		Security Features, 8K EPROM Smartcard Applications, 5 V Only	Die 16 DIP – P 20 SOIC – DW
MC68HC05SC21	6K	128	3K						5 i/o		Security Features On–Chip Charge Pump Smartcard Applications	Die 16 DIP – P 20 SOIC – DW
MC68HC05SC24	3K	128	1K						5 i/o		Security Features On–Chip Charge Pump Smartcard Applications	Die 16 DIP – P 20 SOIC – DW
MC68HC05SC27	16K	240	3K						5 i/o	✔	Security Features On–Chip Charge Pump Smartcard Applications High Speed Option	Die 16 DIP – P 20 SOIC – DW
XC68HC05SC28	12K	256	8K						5 i/o	✔	Security Features, On–Chip Charge Pump Smartcard Applications High Speed Option	Die 44 PLCC – FN
MC68HC05T1	8K	320		16–bit: (1IC, 1OC)	SIOP	1 ch (6–bit)	9 ch (6–bit)	OSD (64 Char ROM)	29 i/o 1 i	✔	Open Drain PWM Outputs 5 V Only	40 DIP – P 42 SDIP – B
XC68HC05T2	15K	320		16–bit: (1IC, 1OC)	SIOP	1 ch (6–bit)	9 ch (6–bit)	OSD (64 Char ROM)	29 i/o 1 i	✔	Open Drain PWM Outputs 5 V Only	40 DIP – P 42 SDIP – B
MC68HC05T10	12K	320		16–bit: (1IC, 1OC) RTC	I^2C	1 ch (8–bit)	8 ch (6–bit) 1 ch (14–bit)	OSD (64 Char ROM)	20 i/o 4 i		Open Drain PWM Outputs KBI (8 pins) 5 V Only	56 SDIP – B

Table 5. 68HC05 Microcontrollers (continued)

Motorola Part Number	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	Serial	A/D	PWM	Display Drive	I/O	COP	Comments	Packages
MC68HC05T16	24K	320		16–bit: (1IC, 2OC) 8–bit PAC	I^2C	2 ch (5–bit)	9 ch (7–bit) 1 ch (14–bit)	OSD (128 Char EPROM)	40 i/o	✔	12 V Open Drain I/O lines (up to 22) 4 row OSD buffer Timer output compare functions do not have output pins	56 SDIP – B
MC68HC05X1	12K	336		16–bit: (1IC, 2OC) MFT, RTI	SSI				24 i/o	✔	KBI (8 pins) SAE J1850 Serial Mux Interface 5 V Operation Only	44 PLCC – FN
MC68HC05X4	4K	176		16–bit: (1IC, 1OC) MFT, RTI					16 i/o	✔	CAN (Controller Area Network) KBI (16 pins)	28 SOIC – DW
MC68HC05X16	15K	352	255	16–bit: (2IC, 2OC)	SCI+	8 ch (8–bit)	2 ch (8–bit)		32 i/o	✔	CAN (Controller Area Network) KBI (8 pins) EEPROM Write Protect On–Chip Charge Pump	64 QFP – FU
MC68HC05X32	32K	528	255	16–bit: (2IC, 2OC)	SCI+	8 ch (8–bit)	2 ch (8–bit)		32 i/o	✔	CAN (Controller Area Network) KBI (8 pins) EEPROM Write Protect On–Chip Charge Pump	64 QFP – FU

ONE–TIME PROGRAMMABLE (OTP) / EMULATOR MCUs

All 68HC705 products have a standard operating voltage range from 3 V to 5.5 V unless noted in Comments.
All 68HC705 products have a standard operating temperature range from 0 – 70°C.
Contact a Motorola Sales Office for availability of extended temperature versions.

Table 6. One–Time Programmable (OTP)/Emulator MCUs

Motorola Part Number	EPROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	Serial	A/D	PWM	Display Drive	I/O	COP	Comments	Packages
MC68HC705B5	6K	176		16–bit: (2IC, 2OC)	SCI+	8 ch (8–bit)	2 ch (8–bit)		24 i/o 8 i 2 o	✔	Programmable Pulldowns (16 pins) EPROM Write Protect	56 SDIP – B 52 PLCC – FN
MC68HC705B16	15K	352	255	16–bit: (2IC, 2OC)	SCI+	8 ch (8–bit)	2 ch (8–bit)		32 i/o 2 o	✔	On–Chip Charge Pump EEPROM Write Protect	52 PLCC – FN *52 Cerquad–FS 64 QFP – FU
XC68HC705B32	32K	528	255	16–bit: (2IC, 2OC)	SCI+	8 ch (8–bit)	2 ch (8–bit)		32 i/o	✔	On–Chip Charge Pump EEPROM Write Protect	52 PLCC – FN 56 SDIP – B 64 QFP – FU
MC68HC705BD3	7.75K	256		MFT, RTI	I^2C		16 ch (8–bit)		24 i/o	✔	Horizontal and Vertical Sync Signal Processor	42 SDIP – B *42 Cersdip – K 40 DIP – P *40 Cerdip – S
MC68HC705C4A	4K	176		16–bit: (1IC, 1OC)	SPI SCI				24 i/o 7 i	✔	Mask Option Register Pullups (8 pins) KBI (8 pins) 1 High Current Pin (20 mA sink) EPROM Security	40 DIP – P 44 PLCC – FN 42 SDIP – B 44 QFP – FB
MC68HC705C8A	8K	304		16–bit: (1IC, 1OC)	SPI SCI				24 i/o 7 i	✔	Mask Option Pullups (8 pins) KBI (8 pins) 1 High Current Pin (20 mA sink) High Speed Option (HSC705C8A) Superset of ROM C8A with more RAM EPROM Security	40 DIP – P 44 PLCC – FN *40 Cerdip – S 42 SDIP – B 44 QFP – FB *44 Cerquad – FS
MC68HC705C9A	16K	352		16–bit: (1IC, 1OC)	SPI SCI				31 i/o	✔	Mask Option Pullups (8 pins) KBI (8 pins) 1 High Current Pin (20 mA sink) EPROM Security	40 DIP – P *40 Cerdip – S *44 Cerquad–FS 44 PLCC – FN 42 SDIP – B 44 QFP – FB
MC68HC705CJ4	4K	224		16–bit: (1IC, 1OC) MFT	SPI SCI I^2C				29 i/o 3 i	✔	8 High Current Pins (10 mA sink) I^2C (Slave Only)	44 QFP – FB
XC68HC705D9	16K	352		16–bit: (1IC, 1OC)	SCI		5 ch (6–bit)		31 i/o	✔	8 High Current Pins (25 mA sink) 30 kHz PWM	40 DIP – P *44 Cerquad–FS 44 PLCC – FN
MC68HC705E1	4K	368		MFT, RTC RTI					20 i/o	✔	32 kHz PLL Clock Synthesizer	*28 Cerdip – S 28 DIP – P 28 SOIC – DW
XC68HC705F6	4K	320		16–bit: (1IC, 1OC)	SPI				26 i/o 4 i		DTMF Generator 8 High Current Pins (10 mA sink) KBI (6 pins)	42 SDIP – B *42 Cersdip – K 64 QFP – FU *64 CQFP – FZ
MC68HC705F8	8K	320		16–bit: (1IC, 1OC) 16–bit: auto	SPI				50 i/o 2 o	✔	DTMF Generator KBI (8 pins) 8 High Current Pins (10 mA sink) Manchester Encoder/Decoder	64 QFP – FU *64 CQFP – FZ
MC68HC705G1	12K	176		16–bit: (1IC, 1OC) RTC	SPI	4 ch (8–bit)			40 i/o 8 i	✔	32 kHz PLL	56 SDIP – B *56 Cersdip – K 64 QFP – FU *64 CQFP – FZ
MC68HC705G4	32K	1024		16–bit: (1IC, 1OC) 8–bit: Event Cntr	Dual SPI	8 ch (8–bit)	4 ch (8–bit)		48 i/o 16 i 4 o	✔	KBI (8 pins) Dual IRQ Dual Oscillators, Selectable Clock	80 QFP – FU *80 CQFP – FZ
MC68HC705J1A	1.2K	64		MFT, RTI					14 i/o	✔	KBI (4 pins), EPROM Security Feature 4 High Current Pins (8 mA sink) Mask Option Pulldowns (14 pins)	20 DIP – P 20 SOIC – DW *20 Cerdip – S
MC68HC705J2	2K	112		MFT, RTI					14 i/o	✔		20 DIP – P 20 SOIC – DW *20 Cerdip – S

Table 6. One–Time Programmable (OTP)/Emulator MCUs (continued)

Motorola Part Number	EPROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	Serial	A/D	PWM	Display Drive	I/O	COP	Comments	Packages
MC68HC705K1	0.5K	32		MFT, RTI					10 i/o	✔	4 High Current Pins (8 mA sink) PEP (64 bits) Programmable Pulldowns (10 pins) Low Voltage Reset Mask Option	16 DIP – P 16 SOIC – DW *16 Cerdip – S
XC68HC705L1	6K	128		16–bit: (2IC, 2OC)		6 ch (8–bit)		64 Segment LCD: (3/4 x 12/16)	17 i/o 15 i 2 o			56 SDIP – B 64 QFP – FU *64 CQFP – FZ *56 Cersdip – K
MC68HC705L5	8K	256		16–bit: (1IC, 1OC) RTI 8–bit: (1IC, 1OC)	SIOP			156 Segment LCD: (1–4 x 27–39)	14 i/o 10 i 15 o		KBI (8 pins), Dual Oscillators 8 High Current Pins (10 mA sink) Programmable Pullups (24 pins) Open Drain (31 pins)	80 QFP – FU *80 CQFP – FZ
MC68HC705L16	16K	512		16–bit: (1IC, 1OC) RTI 8–bit: (1IC, 1OC)	SIOP			156 Segment LCD: (1–4 x 27–39)	16 i/o 8 i 15 o	✔	KBI (8 pins), Dual Oscillators 8 High Current Pins (10 mA sink) Programmable Pullups (24 pins) Open Drain (31 pins)	80 QFP – FU *80 CQFP – FZ
MC68HC705P6	4.5K	176		16–bit: (1IC, 1OC)	SIOP	4 ch (8–bit)			20 i/o 1 i	✔		28 DIP – P 28 SOIC – DW *28 Cerdip – S
MC68HC705P9	2K	128		16–bit: (1IC, 1OC)	SIOP	4 ch (8–bit)			20 i/o 1 i	✔		28 DIP – P 28 SOIC – DW *28 Cerdip – S
MC68HC705T10	12K	320		16–bit: (1IC, 1OC) RTC	I^2C	1 ch (8–bit)	8 ch (6–bit) 1 ch (14–bit)	OSD (64 Char EPROM)	20 i/o 4 i		Open Drain PWM Outputs KBI (8 pins) 5 V Only	56 SDIP – B *56 Cersdip – K
MC68HC705T16	24K	320		16–bit: (1IC, 2OC) 8–bit PAC	I^2C	2 ch (5–bit)	9 ch (7–bit) 1 ch (14–bit)	OSD (128 Char EPROM)	40 i/o	✔	12 V Open Drain I/O Lines (Up to 22) 4 Row OSD Buffer Timer output compare functions do not have output pins	56 SDIP – B *56 Cersdip – K
XC68HC705V8	12K	512	128	16–bit: (1IC, 1OC) MFT, RTI	SPI	8 ch (8–bit)	1 ch (6–bit)		22 i/o	✔	LVR, On Chip Charge Pump, MDLC (Message Datalink Control) 5 V Regulator, KBI (16 pins)	56 SDIP – B 68 PLCC – FN 68 CLCC – FS 56 Cersdip – K
XC68HC705X4	4K	176		16–bit: (1IC, 1OC) MFT, RTI					16 i/o	✔	CAN (Controller Area Network) KBI (16 pins)	28 SOIC – DW

*Windowed packages available only in sample quantities.

Definitions

- CAN – Controller Area Network
- CCTV – Closed Caption Television
- COP – Computer Operating Properly (Watch Dog Timer)
- DTMF – Dual–Tone Multi–Frequency
- EBI – External Bus Interface
- IC – Input Capture
- I^2C – Inter–Integrated Circuit
- IDE – Integrated Device Electronics (IBM PC/AT Type)
- i/o – Bidirectional Input and Output Port Pins
- i – Input Only Port Pins
- KBI – Key Board Interrupt
- LCD – Liquid Crystal Display
- LVI – Low Voltage Interrupt
- LVPI – Low Voltage Program Inhibit
- LVR – Low Voltage Reset
- MDLC – Message Data Link Controller (J1850)
- MFT – Multi Function Timer
- o – Output Only Port Pins
- OC – Output Compare
- OSD – On–Screen Display
- PEEP – Personality EEPROM
- PEP – Personality EPROM
- PIO – Parallel Input Output (IBM PC/AT Type)
- PLL – Phase–Lock Loop
- PWM – Pulse–Width Modulation
- RTC – Real–Time Clock
- RTI – Real–Time Interrupt
- SCI – Serial Communications Interface (asynchronous)
- SCI+ – Serial Communications Interface (async. and sync.)
- SIO – Serial Input Output (IBM PC/AT Type)
- SIOP – Simple Serial I/O Port
- SPI – Serial Peripheral Interface
- VFD – Vacuum Fluorescent Display
- VREG – Voltage Regulator
- WDOG – Watch Dog Timer

Package Definitions

- B – Shrink DIP (70 mil spacing)
- DW – Small Outline (Wide–Body SOIC)
- FA – 7 x 7 mm Quad Flat Pack (QFP)
- FB – 10 x 10 mm Quad Flat Pack (QFP)
- FE – CQFP (windowed) – Samples Only
- FN – Plastic Quad (PLCC)
- FS – CLCC (windowed) – Samples Only
- FT – 28 x 28 mm Quad Flat Pack (QFP)
- FU – 14 x 14 mm Quad Flat Pack (QFP)
- FZ – CQFP (windowed) – Samples Only
- K – Cersdip (windowed) – Samples Only
- L – Ceramic Sidebraze
- P – Dual–in–Line Plastic
- S – Cerdip (windowed) – Samples Only

MCU NEW PRODUCTS

All 68HC05 and 68HC705 products have a standard operating voltage range from 3 V to 5.5 V unless noted in Comments.
All 68HC05 and 68HC705 products have a standard operating temperature range from 0 to 70°C.
Contact a Motorola Sales Office for availability of the following MCUs:

Table 7. MCU New Products

Motorola Part Number	ROM/ EPROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	Serial	A/D	PWM	Display Drive	I/O	COP	Comments	Packages
68HC05B32	32K	528	256	16–bit: (2IC, 2OC)	SCI+	8 ch (8–bit)	2 ch (8–bit)		32 i/o	✔	On–Chip Charge Pump EEPROM Write Protect	52 PLCC – FN 56 SDIP – B 64 QFP – FU
68HC05BD5	7.75K	256		MFT, RTI	I^2C		16 ch (8–bit)		24 i/o	✔	Horizontal and Vertical Sync Signal Processor	40 DIP – P 42 SDIP – B
68HC05C0	0	512		16–bit: (1IC, 1OC) MFT	SCI+				18 i/o	✔	Mux or Non–Mux EBI (16–bit) 3 Chip Selects, KBI (8 pins) Programmable Pullups (8 pins) 1 High Current Pin (20 mA sink)	44 PLCC – FN 40 DIP – P 42 SDIP – B
68HC05E16	16K	352	320	16–bit: (2IC, 2OC) MFT, RTI	Dual I^2C	4 ch (8–bit)			47 i/o 2 i	✔	KBI (8 pins) LVI 32 kHz Programmable PLL Perodic Interrupt (0.25, 0.5, 1 s)	44 QFP – FB 64 QFP – FU 56 SDIP – B
68HC805K3		64	920 16PEEP	MFT, RTI					10 i/o	✔	KBI (4 pins), Programmable Pulldowns (10 pins), 4 High Current Pins (8 mA sink), On–Chip Charge Pump, 1.8 V EE Read	16 DIP – P 16 SOIC – DW
68HC05P7A	2K	128		16–bit: (1IC, 1OC)	SIOP				20 i/o	✔	KBI (8 pins) 2 High Current Pins (15 mA sink)	28 DIP – P 28 SOIC – DW
68HC05P9A	2K	128		16–bit: (1IC, 1OC)	SIOP	4 ch (8–bit)			20 i/o	✔	KBI (8 pins) 2 High Current Pins (15 mA sink)	28 DIP – P 28 SOIC – DW
68HC05SC26	6K	224	1024						5 i/o	✔	Smartcard Security Features On–Chip Charge Pump High Speed Option	die 44 PLCC – FN
68HC05V7	10K	384	128	16–bit: (1IC, 1OC) MFT, RTI	SPI	8 ch (8–bit)	1 ch (6–bit)		22 i/o 16 i	✔	MDLC (Message Datalink Control) 5 V Power Regulator KBI (16 pins) LVR	56 SDIP – B 68 PLCC – FN
68HC705E5	5K	384		MFT, RTI	I^2C				20 i/o	✔	32 kHz PLL Clock Synthesizer	28 DIP – P *28 Cerdip – S 28 SOIC – DW
68HC705MC4	3.5K	176		16–bit: (2IC or 1IC, 1OC) MFT, RTI	SCI	6 ch (8–bit)	2 hi sp (8–bit 24 kHz Max)		22 i/o	✔	1 8–Bit High Current Port (10 mA Source Pin, 20 mA Max/Port) 1 High Sink Current Pin (10 mA) Low EMI Pinout Commutation Mux for PWM Industrial Motor Control	28 DIP – P *28 Cerdip – S 28 SOIC – DW
68HC705RC16	16K	350		Infrared Timer					12 i/o	✔	Mask Option Pullups (12 pins) KBI (12 pins)	28 DIP – P *28 Cerdip – S 28 SOIC – DW
68HC705RC17	16K	350		Infrared Timer					12 i/o	✔	Mask Option Pullups (12 pins) KBI (12 pins) Phase–Locked Loop (PLL)	28 DIP – P *28 Cerdip – S 28 SOIC – DW
68HC705SR3	4K	192		8–bit Timer (7–bit prescaler)		4 ch (8–bit)			24 i/o		Mask Option Pullups (24 pins) KBI (8 pins), LED Drive (8 pins), LVR	40 DIP – P *40 Cerdip – S 42 SDIP – B 44 QFP – FB
68HC705X32	32K	528	255	16–bit: (21C, 2OC)	SCI+	8 ch (8–bit)	2 ch (8–bit)		32 i/o	✔	CAN (Controller Area Network)	64 QFP – FU
68HC08XL36	36K	1K		4 ch 16–bit: (IC, OC, or PWM)	SCI SPI				43 i/o	✔	8 MHz Internal Bus (5 V) Direct Memory Access Module (3 ch) Programmable PLL, LVI/LVR KBI (8 pins), Programmable Pullups (8 pins)	56 SDIP – B 64 QFP – FU
68HC708XL36	36K	1K		4 ch 16–bit: (IC, OC, or PWM)	SCI SPI				43 i/o	✔	8 MHz Internal Bus (5 V) Direct Memory Access Module (3 ch) Programmable PLL, LVI/LVR KBI (8 pins), Programmable Pullups (8 pins)	56 SDIP – B *56 Cersdip – K 64 QFP – FU *64 CQFP – FE

M68HC08 Family

The M68HC08 Family offers a unique combination of high–speed, low–power, enhanced processing performance for cost–sensitive 8–bit applications. Full upward object code compatibility with the world's leading 8–bit microcontroller allows current M68HC05 users to leverage their resource and time investment. M68HC08 modular design utilizes a growing library of on–chip peripherals. The flagship 68HC(7)08X36 OTP and ROM versions for general purpose use are the first two devices in the family.

Features

- Architecturally Enhanced 8–Bit CPU
  - 8 MHz bus speed yields 125 ns minimum instruction cycle
  - 16–bit stack with stack pointer operations and addressing modes
  - 16–bit index register
  - 78 new instructions including advanced looping control
  - Eight new addressing modes
- Fully upward object code compatible with the M68HC05 and M6805 families
- Direct Memory Access Module
  - Memory–to–memory transfer
  - Peripheral–to–memory and memory–to–peripheral transfer
- Timing Interface Module
  - Four independently programmable channels
  - Input capture, output compare, buffered, and unbuffered PWM configurations
- Interface Modules
  - Serial Communications Interface (UART)
  - Serial Peripheral Interface
  - System Interface Module
- System Control Modules
  - Low Voltage Inhibit, PLL, COP, and System Integration Module
- Clock Generator Module
  - Generates two different clock signals from a user–selected source

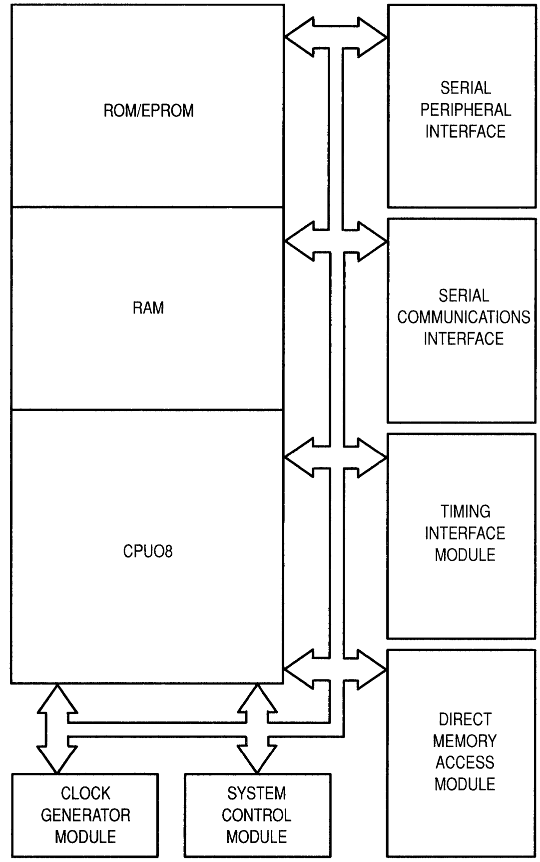


Figure 3. Block Diagram of Typical M68HC08 MCU

M68HC05 Microcontroller Development Tools

Motorola now offers two fully modular development system choices: the new Motorola Modular Evaluation System (MMEVS) and our popular, high–performance Motorola Modular Development System (MMDS). You can now build a customized MMEVS or MMDS to emulate the MCU in your target design in four simple steps. First, order the MMEVS or MMDS system platform (M68MMPFB0508 or M68MMDS05). Second, select and order the emulation module (EM) that contains circuitry specific to emulating the particular HC05/08 MCU in your target application. Third, complete the system by ordering target cable accessories to connect the MMEVS or MMDS to your target MCU socket. Finally, select the appropriate parallel programmer to program your prototype devices.

Choosing Between the MMEVS and MMDS

Build an economical MMEVS system to perform traditional debugging activities such as executing code in run or step mode; setting breakpoints; monitoring or modifying CPU registers, memory and application variables; and creating log or script files to record test results or automate the testing process. Or, create an MMDS system to add high–performance, advanced emulation features such as real–time, dual–ported memory and a real–time bus state analyzer with an 8K trace buffer. In addition, the MMDS includes a built–in power supply and is fully enclosed in a metal case. Both the MMEVS and MMDS include a host–based Integrated Development Environment (IDE) comprised of an editor, assembler, and hardware debugger.

Modular Architecture Benefits

The MMEVS replaces Motorola's older–style EVS and EVM development tool products. A proper subset of the MMDS architecture, the new MMEVS is fully compatible with all EM products supported by the MMDS. The MMEVS extends the emulation performance beyond that of the EVS and EVM by supporting full, real–time, non–intrusive, in–circuit emulation for the new high–speed devices (68HSC05) in the HC05 Family and the new HC08 architecture. The MMEVS also extends emulation support to all low–voltage HC05/HC08 derivatives. The common hardware, firmware, and software design of the MMEVS and MMDS also provide greater flexibility in mixing and matching Motorola hardware tools with the ever–increasing variety of C compilers, assemblers, and integrated development environment product offerings from Motorola's third party developer companies.

CONFIGURATION AND ORDER INFORMATION FOR MMDS/MMEVS

Table 8. Configuration and Order Information for MMDS/MMEVS

Devices	Platform	Emulation Modules	Package Type	In–Circuit Target Cable		
				Low Noise Flexcable	Target Head Adapter	Surface Mount Adapter
68HC05A16 68HC705A24	M68MMPFB0508 OR M68MMDS05	M68EM05A24	56 SDIP – B	M68CBL05B	M68TB05A24B56	
68HC05B4/B6/B8/B16/B32 68HC705B5/B16/B32	M68MMPFB0508 OR M68MMDS05	M68EM05B32	56 SDIP – B	M68CBL05B	M68TB05B32B56	
			64 QFP – FU	M68CBL05C	M68TC05B32FU64	M68TQS064SAG1† M68TQP064SA1†
			52 PLCC – FN	M68CBL05C	M68TC05B32FN52	
68HC05BD3/BD5 68HC705BD3/BD5	M68MMPFB0508 OR M68MMDS05	M68EM05BD3	40 DIP – P	M68CBL05B	M68TB05BD3P40	
			42 SDIP – B	M68CBL05B	M68TB05BD3B42	
68HC05BS8 68HC705BS8	M68MMPFB0508 OR M68MMDS05	M68EM05BS8	44 QFP – FB	M68CBL05C	M68TC05BS8FB44	M68TQS044SAG1† M68TQP044SAMO1†
			52 PLCC – FN	M68CBL05B	M68TB05BS8FN52	
68HC05C0	M68MMPFB0508 OR M68MMDS05	M68EM05C0	40 DIP – P	M68CBL05B	M68TB05C0P40	
			42 SDIP – B	M68CBL05B	M68TB05C0B42	
			44 PLCC – FN	M68CBL05	M68TC05C0FN44	
			44 QFP – FB	M68CBL05C	M68TC05C0FB44	M68TQS044SAG1† M68TQP044SAMO1†
68HC05C5 68HC705C5	Refer to the Configuration and Order Information for Other Motorola Development Tools Section to select a development tool for the 68HC05C5/68HC705C5.					

Table 8. Configuration and Order Information for MMDS/MMEVS (continued)

				In–Circuit Target Cable		
Devices	**Platform**	**Emulation Modules**	**Package Type**	**Low Noise Flexcable**	**Target Head Adapter**	**Surface Mount Adapter**
68HC05C4/C4A/C8A/C12A 68HC705C4A/705C8A	M68MMPFB0508 OR M68MMDS05	M68EM05C9	40 DIP – P	M68CBL05B	M68TB05C9P40	
			44 PLCC – FN	M68CBL05C	M68TC05C4FN44	
			44 QFP – FB	M68CBL05C	M68TC05C9FB44	M68TQS044SAG1† M68TQP044SAMO1†
			42 SDIP – B	M68CBL05B	M68TB05C9B42	
68HC05C9/C9A 68HC705C9	M68MMPFB0508 OR M68MMDS05	M68EM05C9	40 DIP – P	M68CBL05B	M68TB05C9P40	
			44 PLCC – FN	M68CBL05C	M68TC05C9FN44	
			42 SDIP – B	M68CBL05B	M68TB05C9B42	
			44 QFP – FB	M68CBL05C	M68TC05C9FB44	M68TQS044SAG1† M68TQP044SAMO1†
68HC05CCV 68HC705CCV	Refer to the Configuration and Order Information for Other Motorola Development Tools Section to select a development tool for the 68HC05CCV/68HC705CCV.					
68HC05CJ4 68HC705CJ4	M68MMPFB0508 OR M68MMDS05	M68EM05CJ4	44 QFP – FB	M68CBL05C	M68TC05CJ4FB44	M68TQS044SAG1† M68TQP044SAMO1†
68HC05D9/D24/D32 68HC705D9	M68MMPFB0508 OR M68MMDS05	M68HC05D32EM	40 DIP – P	M68CBL05B	M68TB05C9P40	
			44 PLCC – FN	M68CBL05C	M68TC05C9FN44	
			44 QFP – FB	M68CBL05C	M68TC05C9FB44	M68TQS044SAG1† M68TQP044SAMO1†
68HC05E6 68HC705E6	M68MMPFB0508 OR M68MMDS05	M68EM05E6	28 SOIC – DW	M68CBL05C	M68TC05E6P28	M68DIP28SOIC
			44 QFP – FB	M68CBL05C	M68TC05E6FB44	M68TQS044SAG1† M68TQP044SAMO1†
68HC05F4 68HC705F4	M68MMPFB0508 OR M68MMDS05	M68EM05F4	28 DIP – P	M68CBL05C	M68TC05E6P28	
			28 SOIC – DW	M68CBL05C	M68TC05E6P28	M68DIP28SOIC
			44 QFP – FB	M68CBL05C	M68TC05E6FB44	M68TQS044SAG1 M68TQP044SAMO1†
68HC05F6 68HC705F6	M68MMPFB0508 OR M68MMDS05	M68EM05F6	42 SDIP – B	M68CBL05B	M68TB05F6B42	
			44 QFP – FB	M68CBL05C	M68TC05F6FB44	M68TQS044SAG1† M68TQP044SAMO1†
			64 QFP – FU	M68CBL05C	M68TC05F6FU64	M68TQS064SAG1† M68TQP064SAMO1†
68HC05F8 68HC705F8	Refer to the Configuration and Order Information for Other Motorola Development Tools Section to select a development tool for the 68HC05F8/68HC705F8.					
68HC05G1 68HC705G1	M68MMPFB0508 OR M68MMDS05	M68EM05G1	56 SDIP – B	M68CBL05B	M68TB05G1B56	
			64 QFP – FU	M68CBL05C	M68TC05G1FU64	M68TQS064SAG1† M68TQP064SAMO1†
68HC05G3 68HC705G4	M68MMPFB0508 OR M68MMDS05	M68EM05G4	80 QFP – FU	M68CBL05E	M68TE05G4FU80	M68TQS080SBG1† M68TQP080SBMO1†
68HC05J1 68HC705J2	M68MMPFB0508 OR M68MMDS05	M68HC05JPEM	20 DIP – P	M68CBL05A	M68TA05J2P20	
			20 SOIC – DW	M68CBL05A	M68TA05J2P20	M68DIP20SOIC
68HC05J1A 68HC705J1A	M68MMPFB0508 OR M68MMDS05	M68EM05J1A	20 DIP – P	M68CBL05A	M68TA05J2P20	
			20 SOIC – DW	M68CBL05A	M68TA05J2P20	M68DIP20SOIC
68HC05J3 68HC705J3	M68MMPFB0508 OR M68MMDS05	M68EM05J3	20 DIP – P	M68CBL05A	M68TA05J2P20	M68DIP20SOIC
			20 SOIC – DW	M68CBL05A	M68TA05J2P20	
68HC05K0/K1/K3 68HC705K1	M68MMPFB0508 OR M68MMDS05	M68EM05K3	16 DIP – P	M68CBL05A	M68TA05K1P16	
			16 SOIC – DW	M68CBL05A	M68TA05K1P16	M68DIP16SOIC
68HC05L1 68HC705L1	M68MMPFB0508 OR M68MMDS05	M68EM05L1	56 SDIP – B	M68CBL05B	M68TB05L1B56	M68TQS064SAG1†
			64 QFP – FU	M68CBL05C	M68TC05L1FU64	M68TQP064SAMO1†
68HC05L2 68HC705L2	M68MMPFB0508 OR M68MMDS05	M68HC05L2EM	42 SDIP – B	42–SDIP ribbon cable assembly included with M68HC05L2EM.		

Table 8. Configuration and Order Information for MMDS/MMEVS (continued)

Devices	Platform	Emulation Modules	Package Type	In-Circuit Target Cable: Low Noise Flexcable	In-Circuit Target Cable: Target Head Adapter	In-Circuit Target Cable: Surface Mount Adapter
68HC05L5/L16 68HC705L5/L16	M68MMPFB0508 OR M68MMDS05	M68EML05L16	80 QFP – FU	M68CBL05E	M68TE05L16FU80	M68TQS080SBG1† M68TQP080SBMO1†
68HC05L7/L9 68HC705L10 68HC05L11 68HC05M4	Refer to the Configuration and Order Information for Other Motorola Development Tools Section to select a development tool for the 68HC05L7/L9, 68HC05L10, 68HC05L11, or 68HC05M4.					
68HC05P3	M68MMPFB0508 OR M68MMDS05	M68EM05P3	28 DIP – P	M68CBL05A	M68TA05X4P28	
			28 SOIC – DW	M68CBL05A	M68TA05X4P28	M68DIP28SOIC
68HC05P8	M68MMPFB0508	M68HC05JPEM	28 DIP – P	M68CBL05A	M68TA05P8P28	
			28 SOIC – DW	M68CBL05A	M68TA05P8P28	M68DIP28SOIC
68HC05P1/P4/P6/P7/P9 68HC705P6/705P9	M68MMPFB0508 OR M68MMDS05	M68HC05P9EM (Included with MMDS)	28 DIP – P	M68CBL05A	M68TA05P9P28	
			28 SOIC – DW	M68CBL05A	M68TA05P9P28	M68DIP28SOIC
68HC05RC16 68HC705RC16	M68MMPFB0508 OR M68MMDS05	M68EM05RC16	28 DIP – P	M68CBL05A	M68TA05RC16P28	
			28 SOIC – DW	M68CBL05A	M68TA05RC16P28	M68DIP28SOIC
68HC05SC11/SC21/SC24/ SC27		CONTACT SALES OFFICE	die/card	ISO Adapter Included w/EM.		
68HC05SR3 68HC705SR3	M68MMPFB0508 OR M68MMDS05	M68EM05SR3	40 DIP – P	M68CBL05B	M68TB05SR3P40	
			44 QFP – FB	M68CBL05C	M68TC05SR3FB44	M68TQS044SAG1† M68TQP044SAMO1†
			42 SDIP – B	M68CBL05B	M68TB05SR3B42	
68HC05T1/T2	Refer to the Configuration and Order Information for Other Motorola Development Tools Section to select a development tool for the 68HC05T1/T2.					
68HC05T10 68HC705T10	M68MMPFB0508 OR M68MMDS05	M68EM05T7	56 SDIP – B	M68CBL05B	M68TB05T7B56	
68HC05V7 68HC705V8	M68MMPFB0508 OR M68MMDS05	M68EM05V8	56 SDIP – B	M68CBL05B	M68TB05V8B56	
			68 PLCC – FN	M68CBL05B	M68TB05V8FN68	
68HC05X4 68HC705X4	M68MMPFB0508 OR M68MMDS05	M68EM05X4	28 DIP – P	M68CBL05A	M68TA05X4P28	
			28 SOIC – DW	M68CBL05A	M68TA05X4P28	M68DIP28SOIC
68HC05X16/X32 68HC705X32	M68MMPFB0508 OR M68MMDS05	M68EML05X32	64 QFP – FU	M68CBL05E	M68TE05X32FU64	M68TQS064SAG1† M68TQP064SA1†

* Development tools that are scheduled for availability during 1Q96.
† To support more than one QFP target system, separate purchase of additional TQPACKs is required. Contact your Motorola representative for details.
Each QFP target head includes one TQSOCKET with guides (M68TQS0xxSyG1) and one TQPACK disposable surface mount adapter (M68TQP0xxSy1 (1.2 mm lead length) or M68TQP0xxSyMO1 (1.6 mm lead length)). Order additional TQSOCKETs and TQPACKs using part numbers referenced in the Surface Mount Adapters column to support multiple target systems. Contact your Motorola representative for details.

CONFIGURATION AND ORDER INFORMATION FOR OTHER MOTOROLA DEVELOPMENT TOOLS (EVM/EVS/ICS)

Table 9. Configuration and Order Information for Other Motorola Development Tools (EVM/EVS/ICS)

Devices	Development Tool	Package Type	In–Circuit Target Cable			Comments
			Low Noise Flexcable	Target Head Adapter	Surface Mount Adapter	
68HC05C5 68HC705C5	M68HC05C5EVS	40 DIP – P	Not Available			For DIP package user must supply a ribbon cable assembly to interface to user's target system.
		44 PLCC – P	Not Available			For PLCC package, user has the option to order 44PLCC05M, which is the old–style ribbon cable assembly with PLCC target adapter.
68HC05CCV 68HC705CCV	Order M68HC05CCVEM and M68HC05PFB	42 SDIP – B	M68CBL05B	M68TB05CCVB42		
		44 QFP – FB	M68CBL05C	M68TC05CCVFB44	M68TQS044SAG1† M68TQP044SAMO1†	
68HC05J1A 68HC705J1A	M68HC705JICS	20 DIP – P	20 DIP Ribbon Cable Assembly Included With M68HC705JICS			M68HC705KICS In–Circuit Simulator
		20 SOIC – DW	See Above		M68DIP20SOIC	For the SOIC package, user may order M68DIP20SOIC, which is a 20–pin DIP to SOIC adapter.
68HC05K0/K1 68HC705K1	M68HC705KICS	16 DIP – P	16 DIP Ribbon Cable Assembly Included With M68HC705KICS			M68HC705KICS In–Circuit Simulator
		16 SOIC – DW	See Above		M68DIP16SOIC	For the SOIC package, user may order M68DIP16SOIC, which is a 16 pin DIP to SOIC adapter.
68HC05L7/L9	M68HC05L9EVM2	128 QFP – FT	Not Available			
68HC05L10	M68HC05L10EVM	128 QFP – FT	Not Available			
68HC05L11	M68HC05L11EVM	100 QFP – FU	Not Available			
68HC05M4	M68HC05M4EVM	52 PLCC – FN	Not Available			For PLCC package, user has the option to order 52PLCCU, which is the old–style ribbon cable assembly with PLCC target adapter.
68HC05T1/T2	M68HC05T2EVS	40 DIP – P	Not Available			For DIP/SDIP package, user must supply a ribbon cable assembly to interface to user's target system.
		42 SDIP – B	Not Available			
		44 PLCC – FN	Not Available			For PLCC package, user has the option to order 44PLCC05M, which is the old–style ribbon cable assembly with PLCC target adapter.

CONFIGURATION AND ORDER INFORMATION FOR PROGRAMMERS

Table 10. Configuration and Order Information for Programmers

Devices	Packages Supported	Programmer Boards	Comments
68HC705B5/B16/B32	52 PLCC – FN 56 SDIP – B	M68HC05BPGMR	For QFP package, order M68HC705X32PGMR.
68HC705BD3	40 DIP – P 42 SDIP – B	M68HC705UPGMR	M68HC705UPGMR requires package adapter. For 40 DIP – P, order M68UPA05BD3P40. For 42 SDIP – B, order M68UPA05BD3B42.
68HC705C4A/C5/C8/C8A/C9	40 DIP – P/S 44 PLCC – FN/FS	M68HC05PGMR–2	Order M68ADT05P40FB44 adapter to program 44 QFP – FB.
68HC705D9	40 DIP – P/S 44 PLCC – FN/FS	M68HC05PGMR–2	Order M68ADT05P40FB44 adapter to program 44 QFP – FB.
68HC705E6	44 QFP – FB 28 SOIC – DW	M68HC705E6PGMR	
68HC705F6	64 QFP – FU/FZ 42 SDIP – B/K	M68HC705F6PGMR64	
68HC705F8	64 QFP – FU/FZ	M68HC705F8PGMR	
68HC705G1	56 SDIP – B 64 QFP – FU	M68HC705G1PGMR	
68HC705J1A	20 DIP – P	M68HC705JICS	M68HC705JICS In–circuit simulator. SOIC requires user supplied socket or adapter. (Available from Yamaichi, part number IC51–0282–334–1)
68HC705J2/J3	20 DIP – P/S	M68HC705J2PGMR	SOIC requires user supplied socket or adapter. (Available from Yamaichi, part number IC51–0282–334–1)
68HC705K1	16 DIP – P/S	M68HC705KICS M68HC705K1GANG	M68HC705K1GANG Programs up to 8 68HC705K1S or P.
	16 SOIC – DW**	M68HC705K1GANGY	M68HC705K1GANGY Programs up to 8 68HC705K1S, P, or DW.
68HC705L1	56 SDIP – B/K 64 QFP – FU/FZ	M68HC705L1PGMR	
68HC705L5/L16	80 QFP – FU/FZ	M68HC705L5PGMR	
68HC705P3	28 DIP – P 28 SOIC – DW	M68HC705E6PGMR	
68HC705P6/P9	28 DIP – P/S	M68HC705P9PGMR	SOIC requires user supplied socket or adapter.
68HC705SR3	40 DIP – P 42 SDIP – B 44 QFP – FB	M68HC05SR3PGMRSG	M68HC05SR3PGMRSG requires package adapter. For 40 DIP – P, order M68HC05SR3PAP40. For 42 SDIP – B, order M68HC05SR3PAB42. For 44 QFP – FB, order M68HC05SR3PAFB44.
68HC705T10	56 SDIP – B/K	M68HC705T10PGMR	
68HC705X4	28 DIP – P/S 28 SOIC – DW	M68HC705X4PGMR	
68HC705V8	56 SDIP – B 68 PLCC – FN	M68HC705V8PGMR	
68HC705X32	64 QFP – FU 68 PLCC – FN	M68HC705X32PGMR	

*Development tools that are scheduled for availability during 1Q96.
**SOIC on M68HC705K1GANGY only.

THIRD PARTY DEVELOPERS FOR 68HC05 AND 68HC705 FAMILY MCUs

Table 11. Third Party Developers for 68HC05 and 68HC705 Family MCUs

Programmers		
Advin Systems Inc.	USA	(408) 243–7000 (800) 627–2456
	Canada:	
	Eastern	(514) 337–0723
	Western	(604) 986–1286
	France	+33 13961–1414
	Germany	+49 7459–1271
	UK	+44 1332–32651
	Hong Kong	(852) 833–5188
Ascend Systems Inc.	USA	(510) 606–2000 (800) 541–3526
	Austria/ Germany	+43 2772–54581
	France	+33 148619528
BP Microsystems	USA	(800) 225–2102 (713) 688–4600
	Canada	(905) 602–8550
	UK	+44 1280–700262
	France	+33 16941–2801
	Germany	+49–8856–932616
	Hong Kong	852–234–166–11
	Tokyo	81–3–3817–4980
Bytek	USA	(407) 994–3520
	Netherlands, UK, Belgium	+31 16248–0100
	France	+33 16930–2880
	Germany	49 6181–75041
	Hong Kong	852 29198282
Circuit Equipment Corporation	USA	(216) 951–8840
	UK	+44 1734–575666
	France	+33 6185–5767
Data I/O	USA	(206) 881–6444 (800) 426–1045
	Canada	(905) 678–0761
	France	+35 80502–3300
	Germany	+33–31956–8131
	Hong Kong	49–89–858–580
	Japan	81–3–3779–2151
	Netherlands	+31–402–582–911
	UK	+44–1734–440011
E.E. Tools Inc.	USA	(408) 734–8184
	Canada	
	Mexico	52–5–705–7422
	France	+33 16930–2880
	Germany	+49 89834–3047
	Japan	81–538–322822
Emulation Technology, Inc.	France	+33 16941–2801
	USA	(408) 982–0660
	UK	+44 1234 266455 +44 1962–733140
	Germany	+49 89–4602071 +49 81–047044
Logical Devices	USA	(800) 331–7766
Nash Electronics	USA	(501) 289–6111
Needham's Electronics	USA	(916) 924–8037
Sunrise Electronics	USA	(909) 595–7774
System General Corporation	USA	(800) 967–4776 (408) 263–6667
	Japan	81–3–3441–1510
	France	+33 2015–1133
	Germany	+41 1982–2050
TECI (The Engineers Collaborative Inc.)	USA	(800)–336–8321 (802) 525–3458
Tribal Microsystems, Inc.	USA	(510) 623–8859
	Asia	886–2–764–0215
Vel Electronic	Germany	+49 851–751427

ICE/Evaluation Boards		
American Arium	USA	(714) 731–1661
Ashling Microsystems	USA	(508) 366–3220 (Eastern Systems)
	UK	+44 1628–773070
	France	+33 14666–2750
	Germany	+49 8233–32681
Dr. Krohn & Stiller	Germany	+49 896100–0022
	UK	+44 1235–861461
	USA	(320) 617–9400
Emulation Technology, Inc.	France	+33 16941–2801
	USA	(408) 982–0660
	UK	+44 1234–266455 +44 1962–733140
	Germany	+49 89460–2071 +49 8104–7044
iSystem GmbH	Germany	+49 8131–25083
	USA	(408) 982–0660 (Emulation Technology Inc)
	France	+33 62–072–954 (ISIT Societe)
MetaLink Corporation	USA	(602) 926–0797
	UK	+44 1491–455907
	Canada	(613) 226–2365
	Hong Kong	896–2–501–6699
	Germany	+49 8091–55950
	France	+33 1–39–3956–8131
Orion Instruments	USA	(408) 747–0440
	Canada	(416) 609–8396 (Multitest Elect. Inc.)
	France	+33 1–30–54–2222 (BSO France S.A.)
Pentica Systems	USA	(800) PENTICA (617) 275–4419
	UK	+44 0734–792101
	Germany	+49 7147–3085
Sophia Systems	Japan	(044) 989–7000
	USA	(800) 824–9294
Vel Electronic	Germany	+49 85175–1427
Yokogawa Digital Computer Corp	Japan	81–422–56–9101
	USA	(408) 747–0400 (Orion Instruments)

Assemblers/Linkers/Debuggers		
2500 Software Inc.	USA	(719) 395–8683
	France	+33 7443–8045 (CK Electronique) +33 6185–1914 (Societe L.S.I.T.)
	UK	+44 1364–654100 (Greymatter) +44 17183–31022 (System Science)
American Arium	USA	(714) 731–1661
Archimedes Software, Inc.	USA	(206) 822–6300
Avocet Systems, Inc.	USA	(207) 236–9055 (800) 448–8500
BSO Tasking	USA	(617) 894–7800 (800) 458–8276
	France	+33 1–3054–2222
	UK	+44 1252–510014
	Germany	+49 71–5222090
Byte Craft Ltd.	USA	(519) 888–6511
Cosmic Software	USA	(617) 932–2556
	Europe/Intnl	+33 143–995390
	UK	+44 1734–880241
HIWARE	USA	(206) 827–4832 (Archimedes)
	France	+33 16013–3668 (CK Electronique Avnet Group)
	Germany	+41 61331–7151 (HIWARE) +49 7031–2895–38 (Diessner)
	UK	+44 1734–792101 (Pentica) +44 1962–733140 (Nohau)
	Japan	81 3–3293–4716 (Lifeboat)
IAR Systems	USA/ Canada	(415)–765–5500
	Germany	+49 89470–6022
	UK	+44 171924–3334
	France	+1–39–61–14–14
	Hong Kong	2687–1931
	Japan	03–293–4711 (Lifeboat)
Introl Corp.	USA	(414) 327–7171 (800) 327–7171
	UK	+44 171–8331022 (System Science)
	France	+33 7443–8045 (CK Electronique) +33 14622–9988 (Micro Sigma S.A.)
	Japan	(81) 3 256 5881 (Soft Mart Inc.)
	Germany	+49 8104–9074 (Lauterbach GmbH)
P & E Microcomputer Systems, Inc	USA	(617) 353–9206
PseudoCorp	USA	(541) 683–9173
Software Development Systems (SDS)	USA	(708) 368–0400
	UK	+44 1442–876065
	Japan	+81 (0) 3 3493 7981
	Asia–Pac.	+61 (0) 3 720 5344
	Germany	+49 2534–800170 (H S P GmbH)
TECI (The Engineers Collaborative Inc.)	USA	(802) 525–3458 (800) 336–8321

Compiler/Real–Time Kernel		
Archimedes Software, Inc.	USA	(206) 822–6300
Avocet Systems, Inc.	USA	(207) 236–9055 (800) 448–8500
BSO Tasking	USA	(617) 894–7800 (800) 458–8276
	France	+33 1–30542222
	UK	+44 1252–510014
	Germany	+49 71–5222090
Byte Craft Ltd.	USA	(519) 888–6511
Cosmic Software	USA	(617) 932–2556
	Europe/Intnl	+33 143–995390
	UK	+44 1734–880241
Embedded System Products, Inc.	USA	(713) 728–9688
	Europe	+33–143–995–390 (Cosmic Software)
Hi–Tech (distributed by Avocet in USA)	UK	+44–0734–792–101 (Pentica)
	Germany	+49–7147–3085 (Pentica)
HIWARE	USA	(206) 827–4832 (Archimedes)
	France	+33 16013–3668 (CK Electronique Avnet Group)
	Germany	+41 61331–7151 (HIWARE) +49 7031–2895–38 (Diessner)
	UK	+44 1734–792101 (Pentica) +44 1962–733140 (Nohau)
	Japan	81 33293–4716 (Lifeboat)

Miscellaneous Software and Hardware Support		
AMP Incorporated (sockets)	USA	(717) 564–0100
		(800) 522–6752
	Canada	(905) 475–6222
	Mexico	(525) 729–0400
	Europe	+44 1753–676–800
	Asia/Pacific	(81) 44–813–8502
Aptronix (fuzzy logic dev.)	USA	(408) 428–1888
McKenzie (now part of Berg Electronics) (adapters, sockets)	USA	(510) 6512700
	Germany	+49 89150–1001 (Infratron GmbH)
	France	+33 14594–1424 (Green Components)
	UK	+44 1295–271777 (Toby Electronics)
		+44 1501–44434 (Neltronic Ltd.)
Emulation Technology, Inc. (adapters)	France	+33 16941–2801
	USA	(408) 982–0660
	UK	+44 1234 266455
		+44 1962–733140
	Germany	+49 89–4602071
		+49 81–047044
USAR Incorporated (keyboard encoders)	USA	(212) 226–2042
Yamaichi Elec. Inc. (sockets)	USA	(408) 456–0797

On–Line Help

CSIC Microcontroller Division World Wide Web Site

http://design–net.com/csic/CSIC_home.html

The CSIC WWW pages provide a direct line to the latest information and software for 68HC05 and 68HC08 microcontrollers. The web site provides access to:

The Latest News and Press Releases

Product, Market, and Development Tool Overviews

On–Line MCU and Development Tool Selector Guides

On–Line Datasheets and Application Notes

Development Tool Software Upgrades

Free Development Software

Applications Software

3rd Party Development Tool Information

On–Line Technical Support

Freeware Bulletin Board

The Freeware Data Services are now mirrored on the CSIC WWW site for easy access. Customers unable to access the Internet can still access the Freeware development software and applications software by dial–up modem at 2400 to 9600 baud. To log in:

1. Make sure to set character format to 8–bits, no parity, 1 stop bit
2. Dial (512) 891–FREE (512–891–3733)
3. Follow directions from the system

The Freeware files are also accessible by anonymous FTP server:

freeware.aus.mot.com
(use email address for password)

Single–Chip Microcontrollers (AMCU)

In Brief . . .

Motorola offers the most comprehensive selection of high–performance single–chip control systems available from a single source. Microcontroller device families range from industry–standard 8–bit controllers to state–of–the–art 16– and 32–bit modular controllers. Within the price and performance categories of each family, there are a variety of on–chip capabilities to match specific applications.

Motorola device families are structured so that upward migration need not involve complete code development. The M68HC11 Family is upward code compatible with M6800 and M6801 software, while the M68HC16 family is source–code compatible with the M68HC11 family. Motorola's newest 8–bit MCU product line, the M68HC08 family, is fully upward object code compatible with the M68HC05 and M6805 families. In addition, M68300 and M68HC16 devices share standard internal modules and bus configurations.

M68HC11 Family

The M68HC11 Family incorporates a flexible central processing unit and a large number of control–oriented on–chip peripherals. M68HC11 MCU are upward code compatible with M6800, M6801, and M68HC05 software.

Central Processing Unit

The M68HC11 CPU is optimized for low power consumption and high–performance operation at bus frequencies up to 4 MHz. Key features include:

- Two 8–bit or one 16–bit accumulator
- Two 16–bit index registers
- Powerful bit–manipulation instructions
- Six powerful addressing modes
  - Immediate, Extended, Direct, Indexed, Inherent, and Relative
- Power saving STOP and WAIT modes
- Memory mapped I/O and special functions
- 16x16 Integer and Fractional Divides
- 8x8 Multiply

Timer

M68HC11 timer architecture is based on a 16–bit free running counter driven through a software–programmable prescaler. Features include multiple Input Captures, Output Compares, Real–Time Interrupt, Pulse Accumulator, and Watchdog functions.

On–Chip Memory

Since its introduction, the M68HC11 Family has provided versatile combinations of popular memory technologies, including the first EEPROM on a CMOS microcontroller. The family has a memory option to fit virtually any application.

- ROM sizes range from 0 to 32K bytes. ROM is typically factory programmed to contain custom software. ROMless versions of most M68HC11 Family members are also available.
- RAM sizes range from 192 bytes to 1.25K bytes. M68HC11 RAM utilizes a fully static design, and all devices feature a standby power supply pin for battery back–up of RAM contents.
- EPROM sizes range from 4K to 32K bytes. EPROM is especially suited to prototype development and small production runs. EPROM versions are available in both windowed and OTP packaging.
- EEPROM sizes range from 0 to 2K bytes. EEPROM is ideal for storage of calibration, diagnostic, data logging, and security information. Each M68HC11 device with EEPROM includes an on–chip charge pump to facilitate single–supply programming and erasing.

Digital–to–Analog Conversion

The M68HC11 Family provides powerful, on–chip, multi–channel A/D converter systems. Multi–conversion and multi–channel options allow single or continuous conversion on single or multiple channels. M68HC11 A/D systems have eight input channels, and most offer 8–bit resolution, although some provide 10–bit resolution. A 2 channel, 8–bit D/A is also available.

Pulse–Width Modulation

Some M68HC11 Family members have up to six channels of 8–bit PWM. At a 4 MHz bus frequency, signals can be produced from 40 KHz to less than 10 Hz. PWM signals with a period greater than one minute are possible in the 16–bit mode.

Serial Communication

All members of the M68HC11 Family include a Serial Peripheral Interface (SPI) and a Serial Communications Interface (SCI). These on–chip peripherals are designed to minimize CPU intervention during data transfer.

- The SCI is a full duplex UART–type asynchronous system that uses standard Non–Return–to–Zero (NRZ) data format. An on–chip Baud rate generator derives standard rates from the microcontroller oscillator. Both transmitter and receiver are double buffered.
- The SPI is a four–wire synchronous communications interface used for high–speed communication with specialized peripheral devices and other microcontrollers. Data is transmitted and received simultaneously; the Baud rate is software programmable.

Digital I/O and Special Functions

M68HC11 Family I/O is extremely flexible, allowing pins to be configured to match application requirements. Most I/O lines are controlled by bits in a Data Direction Register (DDR) which can configure pins for either input or output. Most lines have a dedicated port data latch.

Some M68HC11 Family members include a 4–channel Direct Memory Access (DMA) and a Memory Management Unit (MMU). The DMA provides fast data transfer between memories and registers, and includes externally mapped memory in the expanded mode. The MMU allows up to 1 megabyte of address space in a physical 64 kbyte allocation. Integrated chip selects help to reduce glue logic.

Several members of the M68HC11 Family also include programmable chip select circuits. These circuits can be used to enable external peripherals whenever an access to a predefined block of memory addresses is made. These circuits help to reduce external logic requirements.

Math Coprocessor

New M68HC11 Family members offer a 16–bit on–chip math coprocessor that accelerates multiply and divide operations by as much as 10 times. The coprocessor functions independently of the CPU and requires no special instructions. The coprocessor is well–suited to low–bandwidth DSP functions such as closed loop control, servo positioning, and signal conditioning.

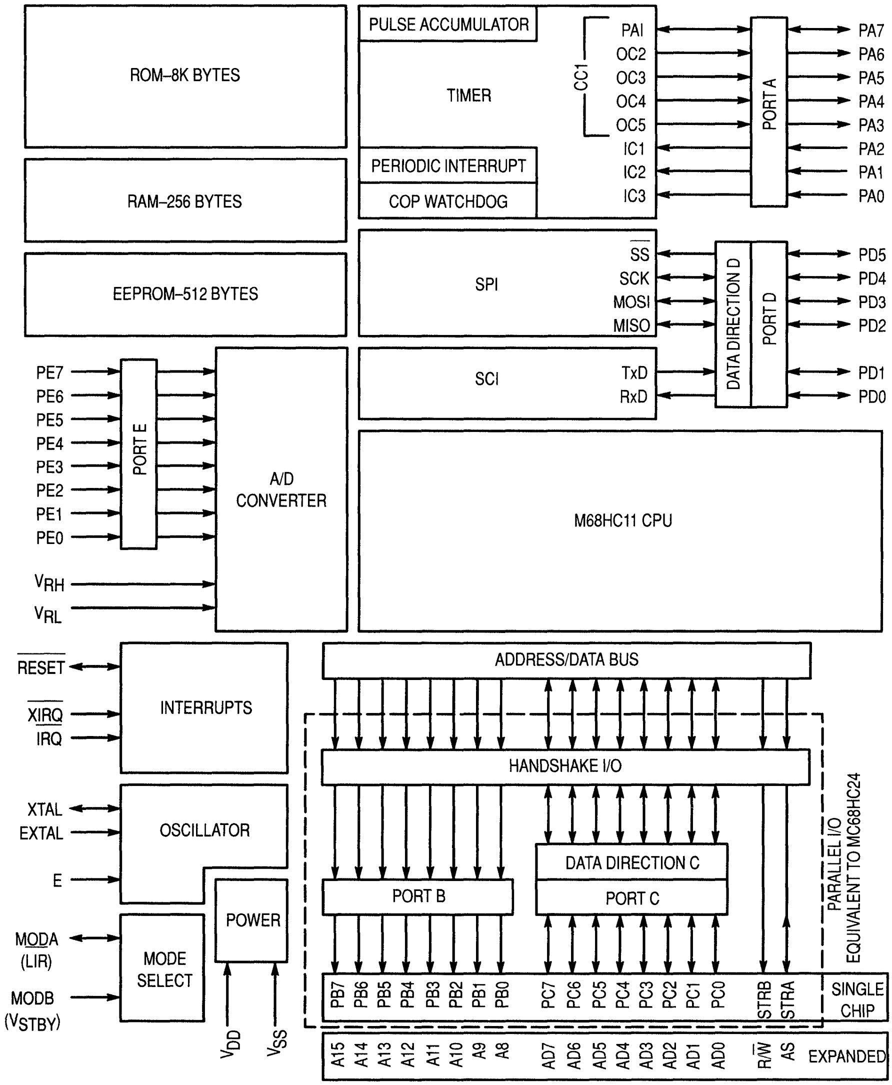


Figure 4. MC68HC11A8 Block Diagram

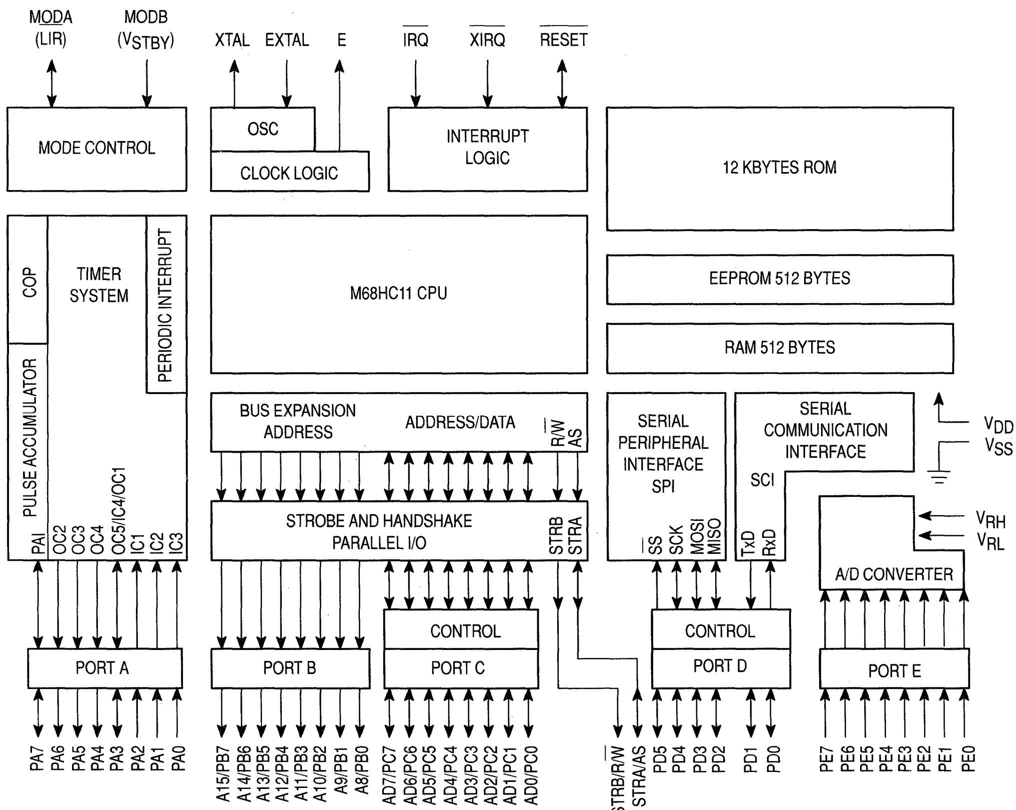


Figure 5. MC68HC11E9 Block Diagram

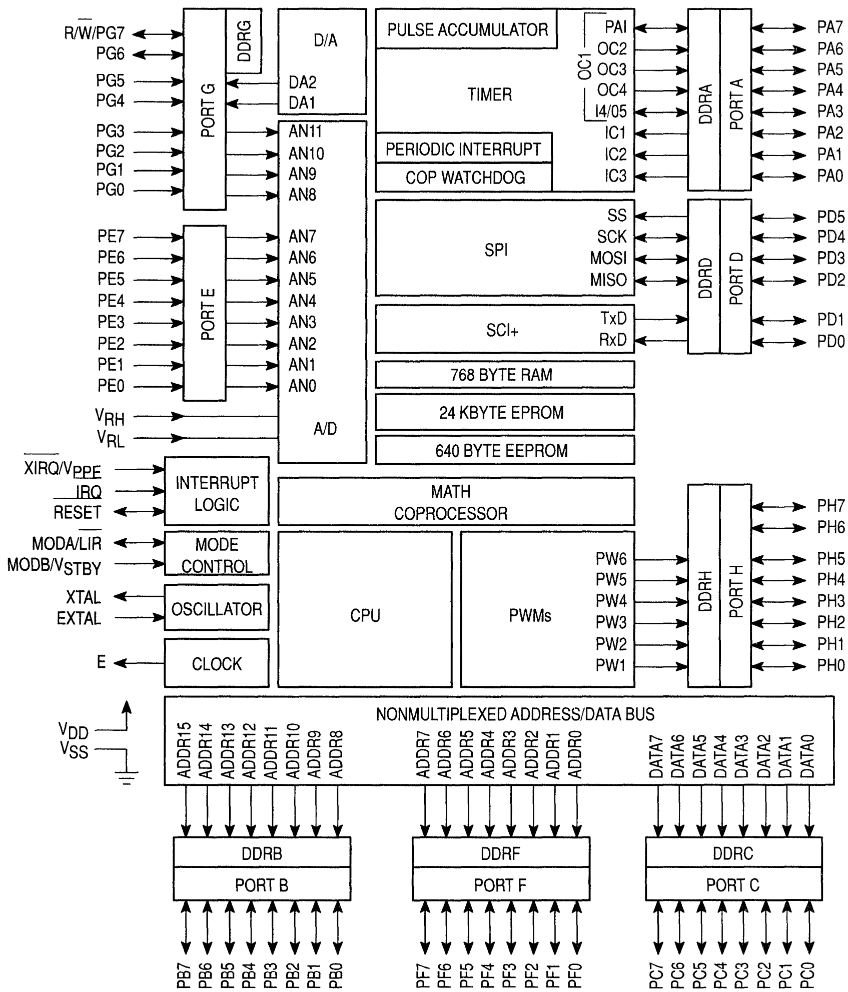


Figure 6. MC68HC711N4 Block Diagram

Table 12. M68HC11 Family Microcontrollers

Part Number	EPROM	RAM	EEPROM	Timer	I/O	Serial	A/D	PWM	Package	Comments
MC68HC11A0	–	256	–	16–Bit – 3 IC, 5 OC, RTI, WDOG Pulse Accumulator	22	SPI, SCI	8 Ch, 8–Bit	–	52–FN 64–FU 48–P	64K External Address Bus, 68HC24 PRU, 3.0 V Version Available
MC68HC11A1	–	256	512	16–Bit – 3 IC, 5 OC, RTI, WDOG Pulse Accumulator	22	SPI, SCI	8 Ch, 8–Bit	–	52–FN 64–FU 48–P	64K External Address Bus, 68HC24 PRU, 3.0 V Version Available
MC68HC11A7	8K	256	–	16–Bit – 3 IC, 5 OC, RTI, WDOG, Pulse Accumulator	38	SPI, SCI	8 Ch, 8–Bit	–	52–FN 64–FU 48–P	3 MHz Version Available, 64K External Address Bus, 68HC24 PRU, 3.0 V Version Available
MC68HC11A8	8K	256	512	16–Bit – 3 IC, 5 OC, RTI, WDOG, Pulse Accumulator	38	SPI, SCI	8 Ch, 8–Bit	–	52–FN 48–P	3 MHz Version Available, Low Voltage Version (3.0–5.5V) at 2 MHz, 64KExternal Address Bus, 68HC24 PRU
XC68HC11C0	–	256	512	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	36	SPI, SCI	4 Ch, 8–Bit	2 Ch, 8–Bit	68–FN 64–FU	256K Extemed Memory, 6 Chip Selects
MC68HC11D0	–	192	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	14	SPI, SCI	–	–	44–FB 44–FN 40–P	64K External Address Bus, 68HC27 PRU, 3.0V Version Available
MC68HC11D3	4K	192	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	32	SPI, SCI	–	–	44–FB 44–FN 40–P	3 MHz Version Available, Low Voltage Version (3.0–5.5V) at 2 MHz, 64K External Address Bus, 68HC27 PRU
MC68HC11ED0	–	512	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	30	SPI, SCI	–	–	44–FB 44–FN 40–P	Pin Compatible with 68HC11D3
MC68HC11E0	–	512	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	22 SCI	SPI, 8–Bit	8 Ch,	–	52–FN	64K External Address Bus, 68HC24 PRU, 3.0 V Version Available
MC68HC11E1	–	512	512	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	22	SPI, SCI	8 Ch, 8–Bit	–	52–FN 64–FU	64K External Address Bus, EEPROM Block Protect, 68HC24 PRU, 3.0 V Version Available
MC68HC11E8	12K	512	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	38 SCI	SPI, 8–Bit	8 Ch,	–	52–FN	3 MHz Version Available, 64K External Address Bus, 3.0 V Version Available
MC68HC11E9	12K	512	512	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	38	SPI, SCI	8 Ch, 8–Bit	–	52–FN 64–FU	EEPROM Block Protect, 3 MHz Version Available, Low Voltage Version (3.0–5.5V) at 2 MHz, 64K External Address Bus
XC68HC11E20	20K	768	512	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	38	SPI, SCI	8 Ch, 8–Bit	–	52–FN 64–FU	3 MHz Mux Bus
MC68HC811E2	–	256	2048	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	38	SPI, SCI	8 Ch, 8–Bit	–	52–FN	EEPROM Block Protect, 64K External Address Bus, 68HC24 PRU
MC68HC11F1	–	1K	512	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	54	SPI, SCI	8 Ch, 8–Bit	–	68–FN 80–FU	Programmable Chip Selects, EEPROM Block Protect, 64K External Address Bus, 68HC27 PRU, 4 MHz Non–Mux Address/Data Bus

Table 12. M68HC11 Family Microcontrollers (continued)

Part Number	EPROM	RAM	EEPROM	Timer	I/O	Serial	A/D	PWM	Package	Comments
PC68HC11G0	–	–	512	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	38	SPI, SCI	8 Ch, 10–Bit	4 Ch, 8–Bit	84–FN 80–FU	
PC68HC11G5	16K	512	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	66	SPI, SCI	8 Ch, 10–Bit	4 Ch, 8–Bit	84–FN 80–FU	
PC68HC11G7	24K	512	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	66	SPI, SCI	8 Ch, 10–Bit	4 Ch, 8–Bit	84–FN 80–FU	
PC68HC11J6	16K	–	512	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	29	SPI, SCI	8 Ch, 8–Bit	4 Ch, 8–Bit	84–FN 80–FU	
MC68HC11K0	–	768	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	37	SPI, SCI	8 Ch, 8–Bit	4 Ch, 8–Bit	84–FN 80–FU	4 MHz Non–Mux Address/Data Bus, Chip Selects, Extended Memory Map, 68HC27 PRU, 3.0 V Version Available
MC68HC11KA0	–	768	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	26	SPI, SCI	8 Ch, 8–Bit	4 Ch, 8–Bit	68–FN 64–FU	4 MHz Non–Mux Address/Data Bus, Chip Selects, Extended Memory Map, 68HC27 PRU
MC68HC11K1	–	768	640	16–Bit – 3/4 IC, 4/5 OC, RTI,WDOG, Pulse Accumulator	37	SPI, SCI	8 Ch, 8–Bit	4 Ch, 8–Bit	84–FN 80–FU	4 MHz Non–MuxBus,Chip Selects, EEPROM Block Protect, Extended Memory Map, 68HC27 PRU, 3.0 V Version Available
MC68HC11KA1	–	768	640	16–Bit – 3/4 IC, 4/5 OC, RTI,WDOG, Pulse Accumulator	26	SPI, SCI	8 Ch, 8–Bit	4 Ch, 8–Bit	68–FN 64–FU	4 MHz Non–Mux Address/Data Bus, Chip Selects,EEPROM Block Protect, Extended Memory Map, 68HC27 PRU
MC68HC11K3	24K	768	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	62	SPI, SCI	8 Ch, 8–Bit	4 Ch, 8–Bit	84–FN 80–FU	4 MHz Non–Mux Address/Data Bus, Chip Selects, Extended Memory Map, 68HC27 PRU, 3.0V Version Available
MC68HC11KA3	24K	768	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	51	SPI, SCI	8 Ch, 8–Bit	4 Ch, 8–Bit	68–FN 64–FU	4 MHz Non–Mux Address/Data Bus, Chip Selects, Extended Memory Map, 68HC27 PRU
MC68HC11K4	24K	768	640	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	62	SPI, SCI	8 Ch, 8–Bit	4 Ch, 8–Bit	84–FN 80–FU	4 MHz Non–Mux Bus, Low Voltage Version (3.0–5.5V) at 3 MHz, Chip Selects, EEPROM Block Protect, Extended Memory Map, 68HC27 PRU
MC68HC11KA4	24K	768	640	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	51	SPI, SCI	8 Ch, 8–Bit	4 Ch, 8–Bit	68–FN 64–FU	4 MHz Non–Mux Address/Data Bus, Chip Selects, EEPROM Block Protect
MC68HC11L0	–	512	–	16–Bit – 3/4 IC, 4/5 OC,RTI, WDOG, Pulse Accumulator	30	SPI, SCI	8 Ch, 8–Bit	–	68–FN 64–FU	64K External Address Bus, 68HC24 PRU, 3.0 V Version Available
MC68HC11L1	–	512	512	16–Bit – 3/4 IC, 4/5 OC,RTI, WDOG, Pulse Accumulator	46	SPI, SCI	8 Ch, 8–Bit	–	68–FN 64–FU	64K External Address Bus, EEPROM Block Protect, 68HC24 PRU, 3.0 V Version Available
MC68HC11L5	16K	512	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	46	SPI, SCI	8 Ch, 8–Bit	–	68–FN 64–FU	64K External Address Bus, 68HC24 PRU, 3.0 V Version Available

Table 12. M68HC11 Family Microcontrollers (continued)

Part Number	EPROM	RAM	EEPROM	Timer	I/O	Serial	A/D	PWM	Package	Comments
MC68HC11L6	16K	512	512	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	46	SPI, SCI	8 Ch, 8–Bit	–	68–FN 64–FU	3 MHz Version Available, Low Voltage Version (3.0–5.5V) at 2 MHz, 64K External Address Bus, 68HC24 PRU
MC68HC11M2	32K	1.25K	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	62	SPI, 2–SCI	8 Ch, 8–Bit	4 Ch, 8–Bit	84–FN 80–FU	16–Bit Math Coprocessor, 4 MHz Non–Mux Bus, 4 Ch DMA Controller
XC68HC11N4	24K	768	640	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	62	SPI, SCI	12 Ch, 8–Bit	6 Ch, 8–Bit	84–FN 80–QFP	16–Bit Math Coprocessor, 4 MHz Non–Mux Bus, 2 Ch 8–Bit D/A
XC68HC11P2	32K	1K	640	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	62	SPI, 3–SCI	8 Ch, 8–Bit	4 Ch, 8–Bit	84–FN 80–FU	PLL Clock Option

Table 13. M68HC11 One–Time Programmable/Emulator Microcontrollers

Part Number	EPROM	RAM	EEPROM	Timer	I/O	Serial	A/D	PWM	Package	Comments
PC68HC711D3	4K	192	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	32	SPI, SCI	–	–	44–FB 44–FN 40–P	64K External Address Bus
PC68HC711E9	12K	512	512	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	38	SPI, SCI	8 Ch, 8–Bit	–	52–FN 64–FU	EEPROM Block Protect, 64K External Address Bus
PC68HC711E20	20K	768	512	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	38	SPI, SCI	8 Ch, 8–Bit	–	52–FN 52–FS 64–FU	EEPROM Block Protect, 64K External Address Bus
PC68HC711G5	16K	512	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	66	SPI, SCI	8 Ch, 10–Bit	4 Ch, 8–Bit	84–FN 84–FS	
PC68HC711J6	16K	512	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	54	SPI, SCI	–	–	68–FN 68–FS	1 Chip Select
PC68HC711K4	24K	768	640	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	62	SPI, SCI	8 Ch, 8–Bit	4 Ch, 8–Bit	84–FN 84–FS 80–FU	4 MHz Non–Mux Bus, EEPROM Block Protect, Chip Selects, Extended Memory Map
PC68HC711L6	16K	512	512	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	46	SPI, SCI	8 Ch, 8–Bit	–	68–FN 68–FS 64–FU	EEPROM Block Protect, 64K External Address Bus
PC68HC711M2	32K	1.25K	–	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	62	SPI, SCI	8 Ch, 8–Bit	–	84–FN 84–FS 80–FU	16–Bit Math Coprocessor, 4 MHz Non–Mux Bus, 4 Ch DMA Controller
PC68HC711N4	24K	768	640	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	62	SPI, SCI	12 Ch, 8–Bit	6 Ch, 8–Bit	84–FN 84–FS	16–Bit Math Coprocessor, 4 MHz Non–Mux Bus, 2 Ch 8–Bit D/A
XC68HC711P2	32K	1K	640	16–Bit – 3/4 IC, 4/5 OC, RTI, WDOG, Pulse Accumulator	62	SPI, SCI	8 Ch, 8–Bit	4 Ch, 8–Bit	84–FN 84–FS 88–FU	PLL Clock

Definitions for Tables 3 and 4

General Definitions

ADC	Analog to Digital Converter Module
A/D	Analog to Digital Converter
CPU16	16 bit Central Processing Unit
CPU32	32 bit Central Processing Unit
D/A	Digital to Analog Converter
DMA	Direct Memory Access
GPT	General–Purpose Timer
IC	Input Capture
IIC	Inter–Integrated Circuit
MCCI	Multi–Channel Communication Interface
PLL	Phase Lock Loop
OC	Output Capture
POQ	Preferred Order Quantity Multiple
PWM	Pulse Width Modulation
QSM	Queued Serial Module
RPSCIM	Reduced Pin Count SCIM
RTC	Real–Time Clock
RTI	Real–Time Interrupt
SCI	Serial Communication Interface
SCIM	Single Chip Integration Module
SIM	System Integration Module
SPI	Serial Peripheral Interface
TPU	Time Processing Unit
UART	Universal Asynchronous Receiver/Transmitter
WDOG	Watch Dog Timer

Package Definitions

FB	10x10 mm Quad Flat Pack (QFP)
FC	Fine Pitch Plastic Quad Flat Pack (PQFP)
FD	Plastic Quad Flat Pack in Molded Carrier Ring
FE	Ceramic Quad Flat Pack (CQFP)
FM	Molded Carrier Flat Pack (CQFP)
FN	Plastic Leaded Chip Carrier (PLCC)
FS	Windowed Cerquad (Ceramic LCC)
FT	28x28 mm Quad Flat Pack (QFP)
FU	14x14 mm Quad Flat Pack (QFP)
FV	20x20 mm Quad Flat Pack (QFP)
L	Ceramic
P	Dual–in–Line Plastic
PB	Thin Quad Flat Pack (TQFP) 10x10 mm
PU	Thin Quad Flat Pack (TQFP) 14x14 mm
PV	Thin Quad Flat Pack (TQFP) 20x20mm
S	Cerdip (windowed or non–windowed)
TH	16x16 mm Quad Flat Pack (QFP)

M6800 Series Microprocessors and Peripherals

These devices are a testament to the staying power of Motorola microtechnology. The original MC6800 was Introduced in 1975, and is still in demand today. Quality M6801, M6804 and M6805 systems have been performing reliably in automotive, industrial, and office equipment applications for years. Each of these devices can be combined with various peripherals to meet the requirements of a microcontroller design.

Table 14. M6801 and M6803 (HMOS)

Part Number	ROM	RAM	EEPROM	Timer	Serial	A/D	I/O	Bus Speed, MHz	Package	Comments
MC6801	2048	192	0	16 bit: 1 IC, 1 OC	SCI	No	29	0.5–2.0	40 P	
MC68701	0	128	2048	16 bit: 1 IC, 1 OC	SCI	No	29	0.5–2.0	40 P	
MC6803	0	192	0	16 bit: 1 IC, 1 OC	SCI	No	13	0.5–2.0	40 P	
MC6801U4	4096	256	0	16 bit: 2 IC, 3 OC	SCI	No	29	0.5–1.25	40 P	
MC68701U4	0	128	4096	16 bit: 2 IC, 3 OC	SCI	No	29	0.5–1.25	40 P	
MC6803U4	0	256	0	16 bit: 2 IC, 3 OC	SCI	No	13	0.5–1.25	40 P	

Table 15. 8–Bit MPU/Peripherals

Device	Pins	Package	Part Description	Speed
MC68B00	40	P	8 Bit MPU, Addresses 64K Memory, 1 or 2 MHz Versions	2 MHz
MC6802	40	P	MC6800 + Int. Clock Oscillator; 128 Bytes RAM	1 MHz
MC68B09	40	P	High Performance MPU, 10 Powerful Addressing Modes	2 MHz
MC68B09E	40	P	MC6809 With External Clock Input for External Sync.	2 MHz
MC68B21	40	P	Peripheral Interface Adapter	2 MHz
MC68B40	40	P	Programmable Timer Module Contains 3 16–Bit Timers	2 MHz
MC6845	40	P	CRT Ctrl, Refresh Memory Addressing; 2nd Source HD6845R	1 MHz
MC68B50	40	P	Asynchronous Communication Interface Adaptor	2 MHz
MC68HC24	40, 44	P, FN	MC68HC11 Port Replacement (Expanded Mode) for A8, E9	2 MHz
MC68HC27	46, 68	FU, FN	Port Replacement for D3, K4, F1	2 MHz
MC68HCB34	40	P, FN	256 Byte Dual Port RAM, 6 Semaphore Registers	2 MHz
MC68B10	24	P	128 x 8 Random Access Memory	2 MHz
MC68B44	40	P	Direct Memory Access Controller	2 MHz
MC68B488	40	P	General Purpose Interface Adapter	2 MHz
MC68B52	24	P	Synchronous Serial Data Adapter	2 MHz
MC68B54	28	P	Advanced Data Link Controller	2 MHz

Table 16. M6805 (HMOS) Microprocessors

Part Number	ROM	RAM	EEPROM	Timer	Serial	A/D	I/O	Bus Speed, MHz	Package	EPROM or EEPROM Version	Comments
MC6805P2	1K	64	0	8–Bit	–	No	20	0.1–1.0	28–P 28–FN	705P3	LVI Option
MC6805P6	2K	64	0	8–Bit	–	No	20	0.1–1.0	28–P	705P3	LVI Option
MC6805R2	2K	64	0	8–Bit	–	Yes	32	0.1–1.0	40–P 44–FN	705R3	LVI Option, Prog. Prescaler Option
MC6805R3	4K	112	0	8–Bit	–	Yes	32	0.1–1.0	40–P 44–FN	705R3	7–Bit Prescaler, LVI Option
MC6805R6	4K	112	0	8–Bit, WDOG	–	Yes	32	0.1–1.0	40–P 44–FN	705R3	7–Bit Prescaler, LVI Option
MC6805S2	1K	64	0	16–Bit, 8–Bit	SPI	Yes	16	0.1–1.0	28–P	705S3	15–Bit Prescaler, LVI
MC6805S3	4K	104	0	2 8–Bit, 16–Bit	SPI	Yes	21	0.1–1.0	28–P	705S3	1 Extra 8–Bit Timer
MC6805U2	2K	64	0	8–Bit	–	No	32	0.1–1.0	40–P 44–FN	705U3	LVI Option
MC6805U3	4K	112	0	8–Bit	–	No	32	0.1–1.0	40–P 44–FN	705U3	7–Bit Prescaler, LVI Option

Table 17. 8–Bit MPU/Peripherals

Device	Pins	Package	Part Description
MC14618	24	P	Real Time Clock, 50 Bytes RAM, Programmable Square Wave
MC146818A	24, 28	P, FN	Enhanced Version of the MC146818
MC146823	40, 44	P, FN	Three 8–Bit Ports, Handshake Control Logic
MC146805E2	40, 44	P, FN	CMOS 8–Bit Microprocessor
MC68HC68L9	80	FU	LCD Expansion to the MC05L9

Modular Microcontrollers

Modular microcontrollers are another of the innovations that make Motorola a leader in single–chip control systems. Modular controllers are built up from standard modules that interface via a common intermodule bus (IMB). The modular concept allows rapid design and manufacture of controllers tailored for specific applications.

Intermodule Bus Peripherals

Each modular microcontroller incorporates a state–of–the art pipelined CPU module, a sophisticated integration module, and a number of special–purpose modules. The rapidly–growing library of special–purpose modules includes programmable timers, serial communication interfaces, analog–to–digital converters, and a variety of memory modules.

Central Processing Units

CPU16

- 16–Bit Architecture
- Full Set of 16–Bit Instructions
- Three 16–Bit Index Registers
- Two 16–Bit Accumulators
- One Megabyte of Program Memory and One Megabyte of Data Memory
- Source code compatible with the M68HC11 CPU
- Control–Oriented Digital Signal Processing Capability
- High–Level Language Support
- Fast Interrupt Response Time
- Fully Static Implementation
- Low Power Stop Operation
- Background Debugging Mode
- Hardware Breakpoint Signal

CPU32

- 32–Bit Internal Data Path and Arithmetic Hardware
- 32–Bit Internal Address Bus – 24–Bit External Address Bus
- Eight 32–Bit General–Purpose Data Registers
- Seven 32–Bit General–Purpose Address Registers
- Separate User and Supervisor Stack Pointers and Address Spaces
- Separate Program and Data Address Spaces
- Virtual Memory Implementation
- Enhanced Addressing Modes
- Object Code Compatible with M68000 Family
- Improved Exception Handling for Controller Applications
- Rich Instruction Set
- Fully Static Implementation
- Low Power Stop Operation
- Background Debugging Mode
- Hardware and Software Breakpoints
- Trace on Change of Flow

Integration Modules

System Integration Module (SIM)

- Manages controller internal and external bus interfaces
- Provides device interrupt arbitration
- Spurious interrupt monitor
- Twelve programmable chip–select outputs
- Watchdog timer, clock monitor, and bus monitor
- PLL clock synthesizer

Single–Chip Integration Module (SCIM)

- Manages controller internal and external bus interfaces
- Provides device interrupt arbitration
- Spurious interrupt monitor
- Single–chip operation with address and data bus pins configured as I/O ports
- Optional Fully or Partially–expanded bus operation
- Nine general–purpose chip select outputs
- Emulation mode chip–select outputs can be used to address a port replacement unit and external emulation RAM
- Watchdog timer, clock monitor, and bus monitor
- PLL clock synthesizer
- Interrupt request inputs can be configured for edge or level detection
- Reduced pin SCIM (RPSCIM) available with 5 chip selects

Timers

Time Processor Unit (TPU)

- On–chip microengine dedicated to high–speed timing tasks
- Two independent 16–bit counters used as basis for timing tasks
- Real–time task scheduler
- Executes a programmed series of functions to perform complex tasks
- Each of 16 orthogonal channels can perform available time functions
- Functions contained in dedicated control store or in MCU RAM
- TPU communicates to CPU via dual port RAM

General Purpose Timer (GPT)

- Two 16–bit free–running counters
- Three input capture channels
- Four output compare channels
- One input capture/output compare channel
- One pulse accumulator/event counter input
- Two pulse–width modulation outputs
- Pulse accumulator input

Configurable Timer Module (CTM)

- Modular timer system combining different configurations of timer submodules:
- CPSM–6 TAP counter prescaler
- FCSM–16–bit free running up counter
- MCSM–16–bit modulus up counter
- SASM–(Single Action) two I/O pins for 16–bit input capture or output compare functions
- DASM–(Dual Action) one I/O pin for 16–bit I/C, O/C, PWM, or output function

Timer Module (TM)

- 16–bit free–running counter with 8–bit prescaler
- Two TM can be externally cascaded to increase count width
- Software selected input capture, output compare, pulse accumulation, event counting, or pulse–width modulation functions

Communication Modules

Queued Serial Module (QSM)

- Queued full–duplex, synchronous three–line SPI with dedicated RAM
- Standard, asynchronous NRZ–format SCI
- Polled and interrupt–driven operation
- Pins can be configured as a parallel I/O port

Multi–Channel Communications Interface (MCCI)

- One full–duplex synchronous three–line SPI
- Two independent standard, asynchronous NRZ–format SCI
- Polled and interrupt–driven operation
- Pins can be configured as a parallel I/O port

Dual Universal Asynchronous/ Synchronous Receiver Transmitter (DUART)

- Dual NRZ Serial RS–232C channels
- Independently programmable TxD and Receiver Transmitter (DUART)
- RxD Baud rates for each channel up to 76.8K Baud
- Optional external input pins provide baud clock
- Transmit operations are double buffered, and receive operations are quadruple buffered
- RTS and CTS signals are directly supported

Analog–to–Digital Conversion Modules

Analog–to–Digital Converter (ADC)

- 8 or 10 bits of resolution
- Eight input channels
- Eight result registers
- Three result alignment formats
- Eight automated conversion modes
- Programmable sample and hold times are provided
- Three result alignment modes

Queued Analog–to–Digital Converter (QADC)

- 10 bits of resolution
- 16 analog input channels (up to 27 if multiplexed externally)
- Two independent conversion queues
- 32 result registers (16 per queue)
- Three result alignment formats
- Queued conversions can be performed continuously or can be retriggered by software or the QADC module periodic interval timer and external trigger
- Programmable sample and hold times
- Alternate voltage references

Specialized Control Modules

Direct Memory Access (DMA)

- Provides low–latency transfer to external peripheral or for memory–memory data transfer
- Two independent DMA channels with full programmability

Memory Modules

Standby RAM (SRAM)

- Fast Static RAM maintained by voltage from standby voltage pin
- Available in 1K, 1.5K, 2K, 3.5K, and 4K blocks
- Fast (2 clock) access speed
- Byte, word, and long–word operations supported

Standby RAM with TPU Emulation (TPURAM)

- Fast Static RAM maintained by voltage from standby voltage pin
- Available in 1K, 1.5K, 2K, 3.5K, and 4K blocks
- Fast termination (2 clock) access speed
- Supports TPU microcode ROM emulation
- Byte, word, and long–word operations supported

Masked ROM (MRM)

- Custom–masked non–volatile 16–bit wide memory
- Available in 4K increments from 8K to 48K bytes
- Fast (2 clock) access speed
- Byte, word, and long–word operations supported
- Boot ROM capability

Flash EEPROM (FLASH)

- Word programmable, bulk erasable non–volatile 16–bit wide memory
- Available in 8K increments from 8K to 64K bytes
- Fast (2 clock) access speed
- Byte, word, and long–word operations supported
- Boot ROM capability
- External 12 volt programming/erasure source required

Block Erasable Flash EEPROM (BEFLASH)

- Available in 8K increments from 8K to 64K bytes
- Eight independently–erasable blocks
- Fast termination (2 clock) access speed
- Byte, word, and long–word operations supported
- Byte/Word programming with 12 volt external input

The M68HC16 Family

The M68HC16 family is designed for embedded control applications. Each M68HC16 MCU incorporates a true 16–bit CPU module (CPU16) that is upwardly code–compatible with the M68HC11 CPU, a sophisticated integration module, and a number of special–purpose modules. M68HC16 devices can be placed in low–power stop mode to minimize power consumption during periods of inactivity. The M68HC16 family provides the flexibility and features of the M68300 family, and also provides a convenient way for users of M68HC11 devices to move up to 16–bit performance.

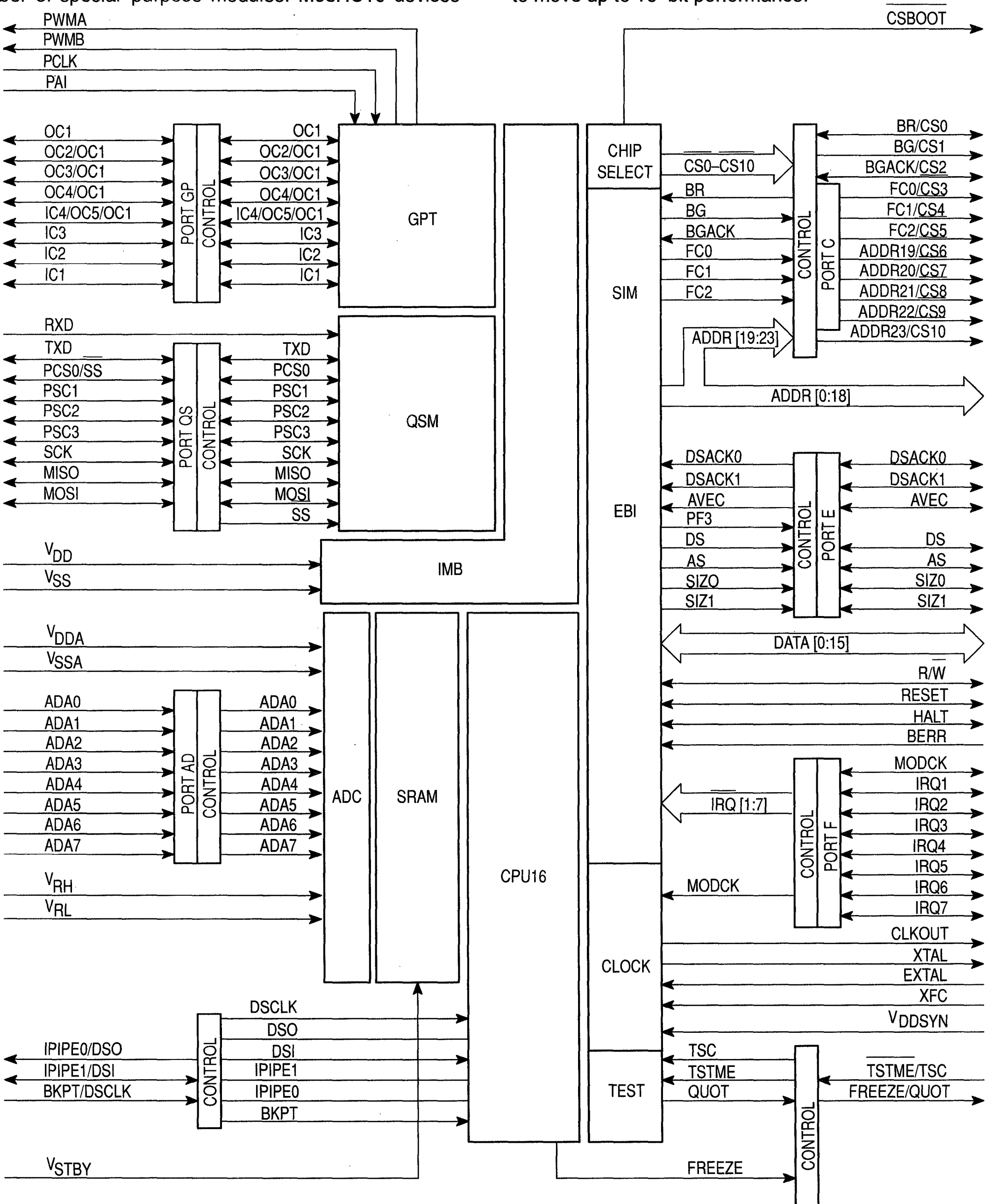


Figure 7. MC68HC16Z1 Block Diagram

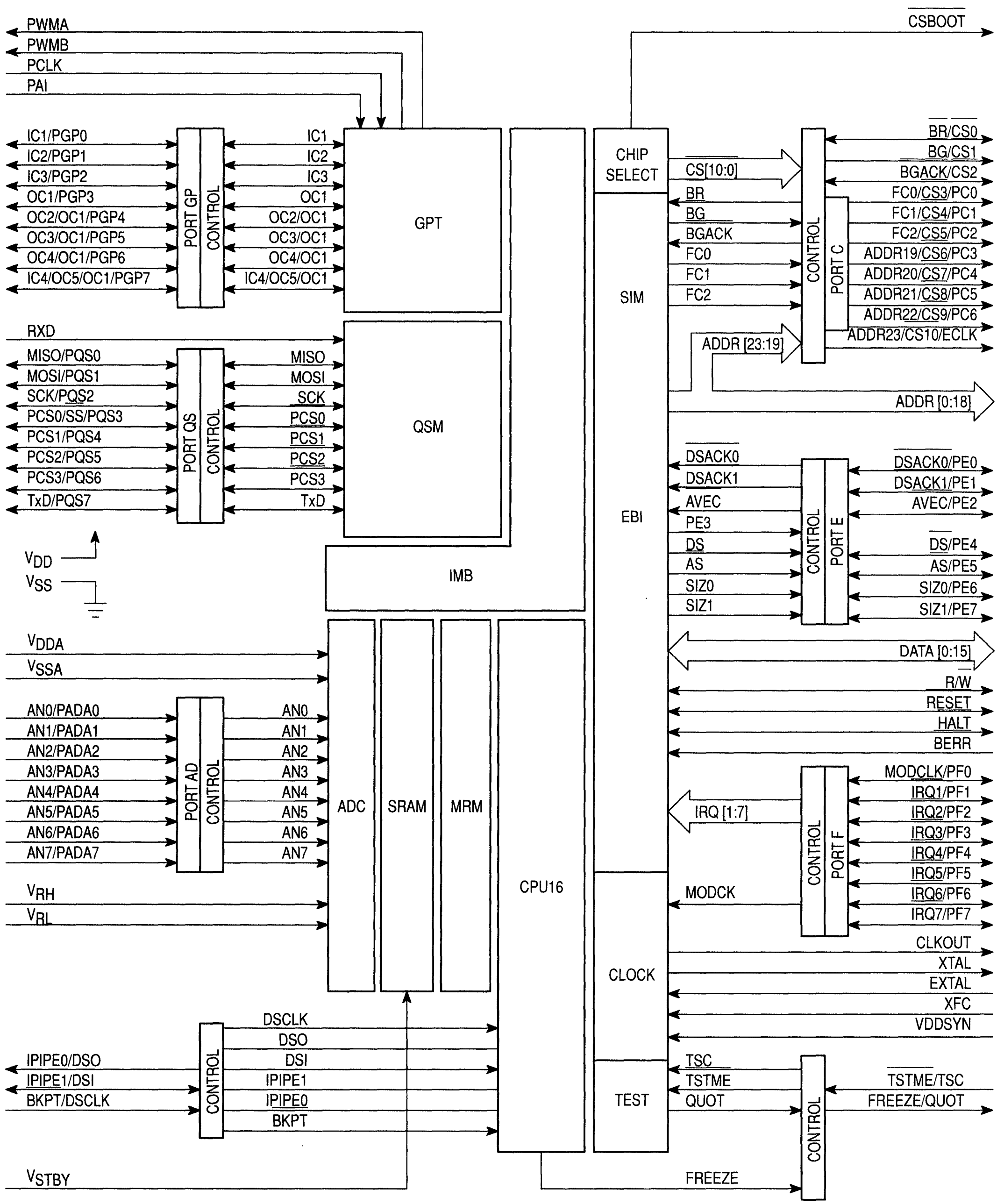


Figure 8. MC68HC16Z2 Block Diagram

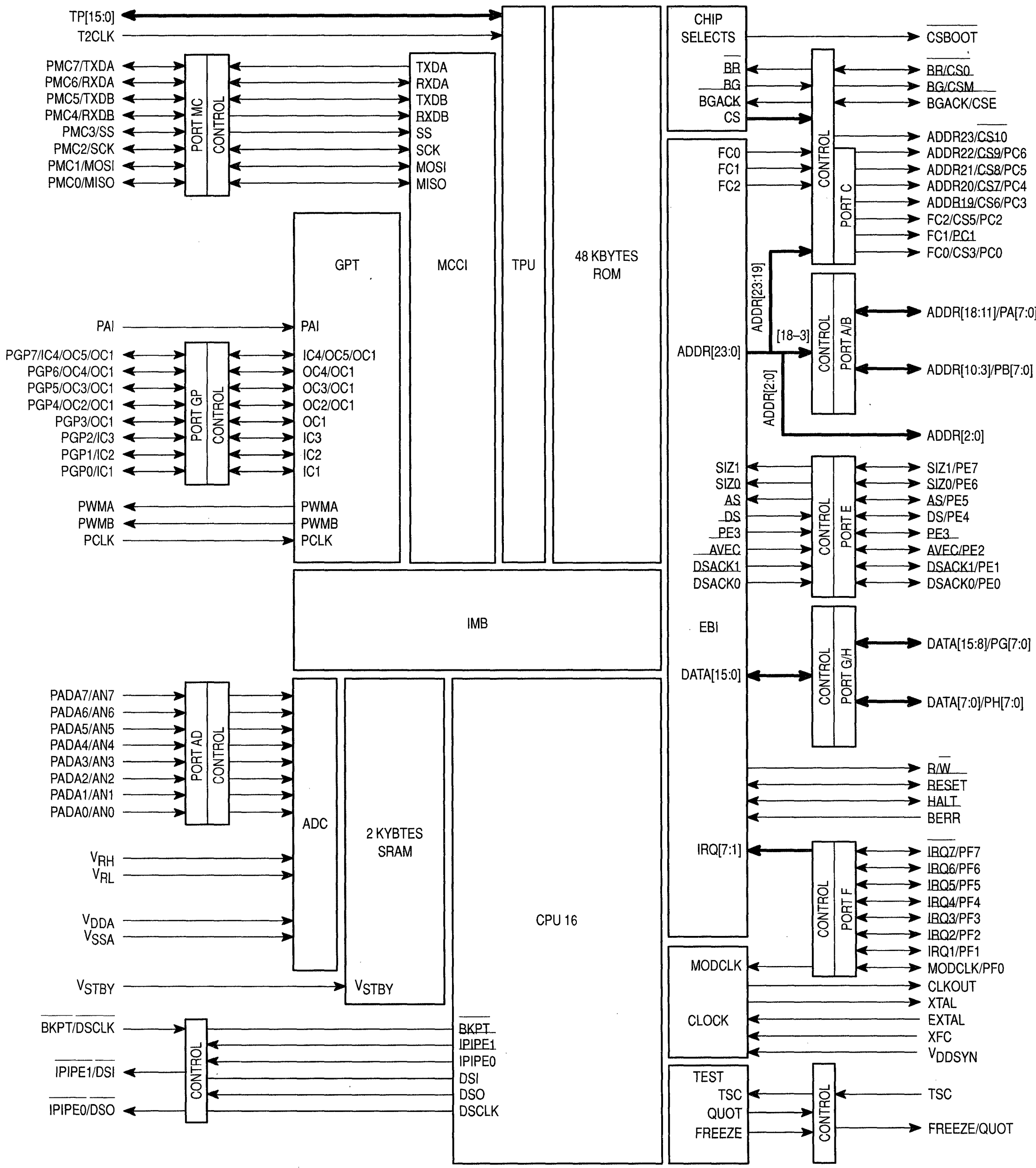


Figure 9. MC68HC16Y1 Block Diagram

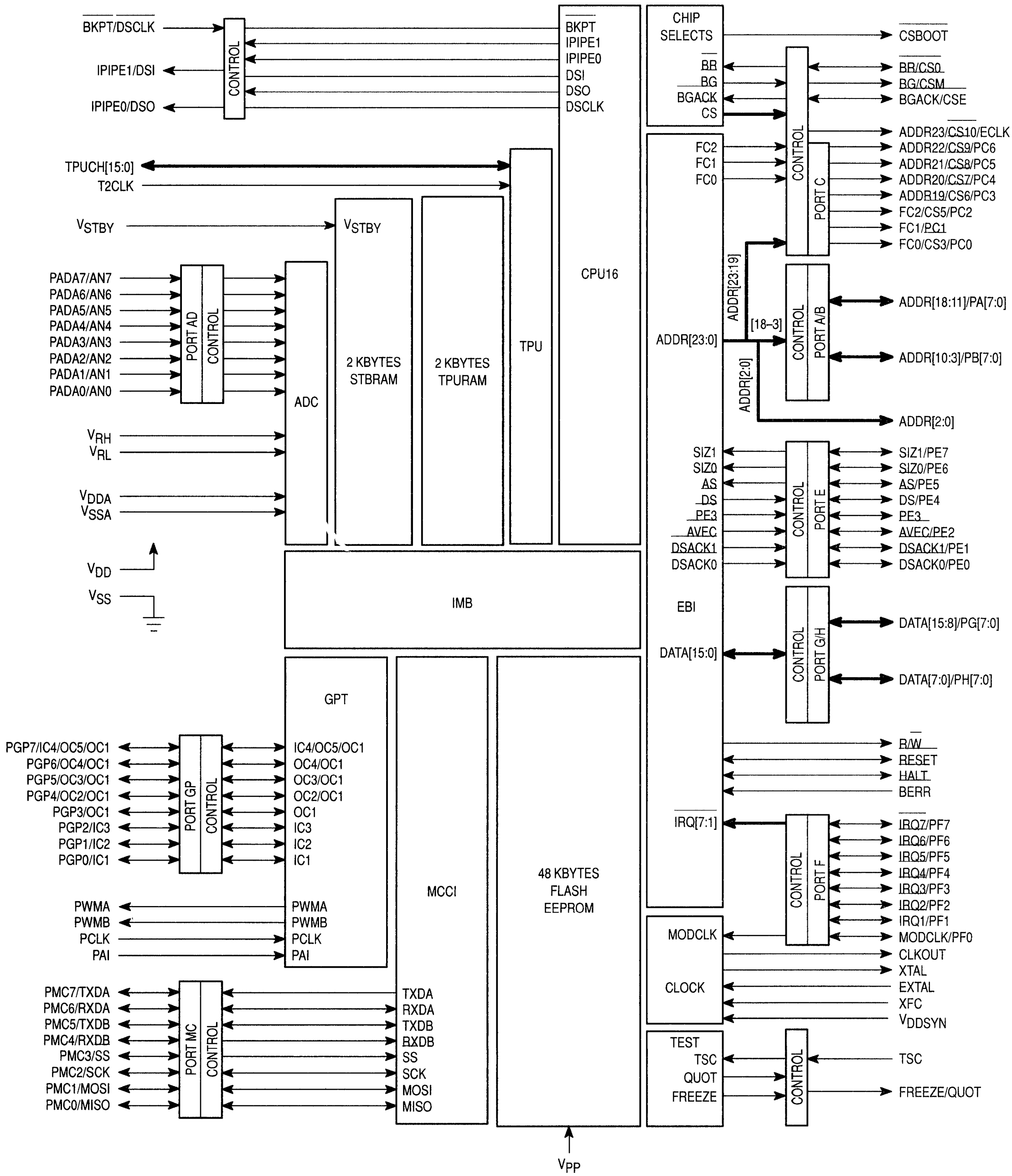


Figure 10. MC68HC916Y1 Block Diagram

Table 18. M68HC16 Family Modular Microcontrollers

Part Number	ROM	SRAM	EEPROM	Timer	I/O	Serial	ADC	Integration Module	Package	Comments
MC68HC16Z1	–	1K	–	GPT	46	QSM	8 Ch, 10–Bit	SIM	132–FC 132–FD 144–FM 144–FV	20 Address Lines, 12 Chip Selects, Synthesized Clock
MC68HC16Z2	8K	2K	–	GPT	46	QSM	8 Ch, 10–Bit	SIM	132–FC 132–FD	20 Address Lines, 12 Chip Selects, Synthesized Clock
MC68HC16Y1	48K	2K	–	TPU + GPT	95	MCCI	8 Ch, 10–Bit	SCIM	160–FT 160–FM	20 Address Lines, 9 Chip Selects, Single Chip or Expanded Mode
XC68HC916X1		1K	2K BEFlash 48K Flash	GPT	70	QSM	8 Ch, 10–Bit	RPSCIM	120–TH	20 Address Lines, 5 Chip Selects, Single Chip or Expanded Mode
XC68HC916Y1	–	4K	48K Flash	TPU + GPT	95	MCCI	8 Ch, 10–Bit	SCIM	160–FT 160–FM	20 Address Lines, 9 Chip Selects, Single Chip or Expanded Mode

The M68300 Family

The high–performance M68300 family is designed for embedded control applications. Each M68300 MCU incorporates a 32–bit M68000–based CPU module (CPU32), a sophisticated integration module, and a number of dedicated special–purpose modules. In addition to utilizing a bus protocol similar to that of the M68020, the system integration module generates external bus–control signals for M6800 devices, and provides a variety of programmable chip–select functions. M68300 devices can be placed in low–power stop mode to minimize power consumption during periods of inactivity. The M68300 family provides great design flexibility, performance, and compatibility with exiting hardware and software.

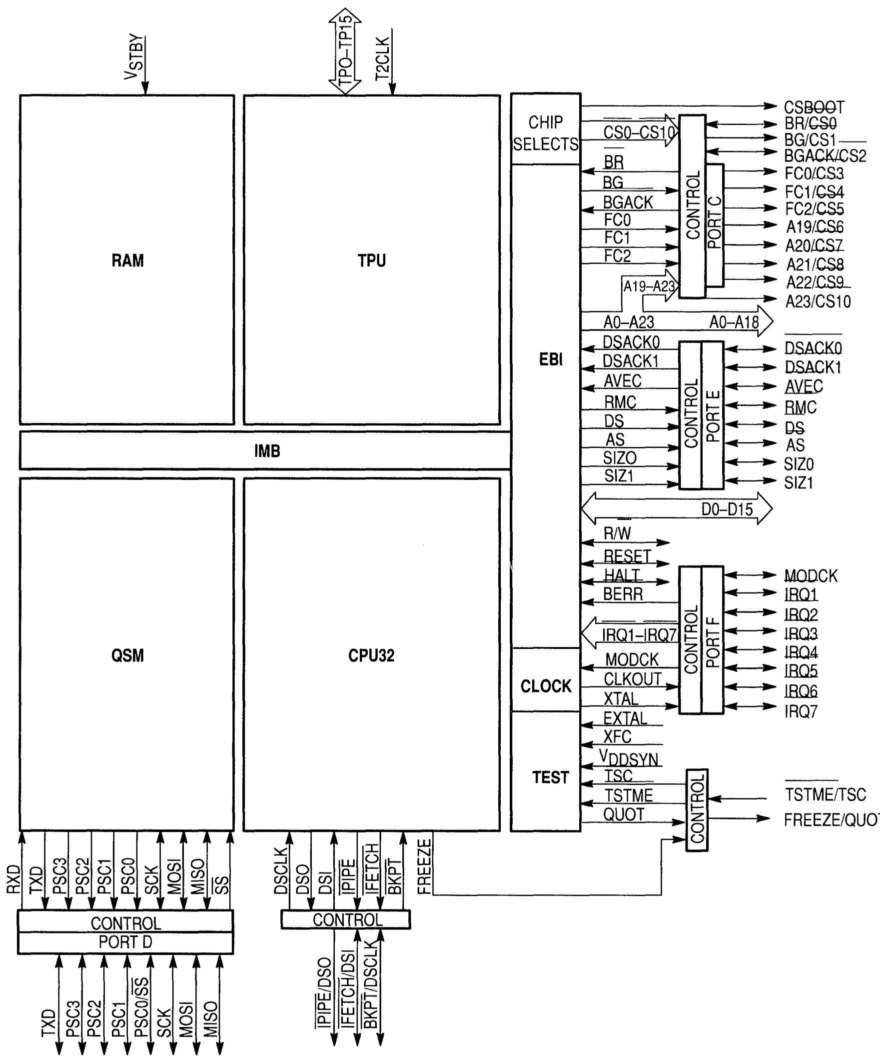


Figure 11. MC68332 Block Diagram

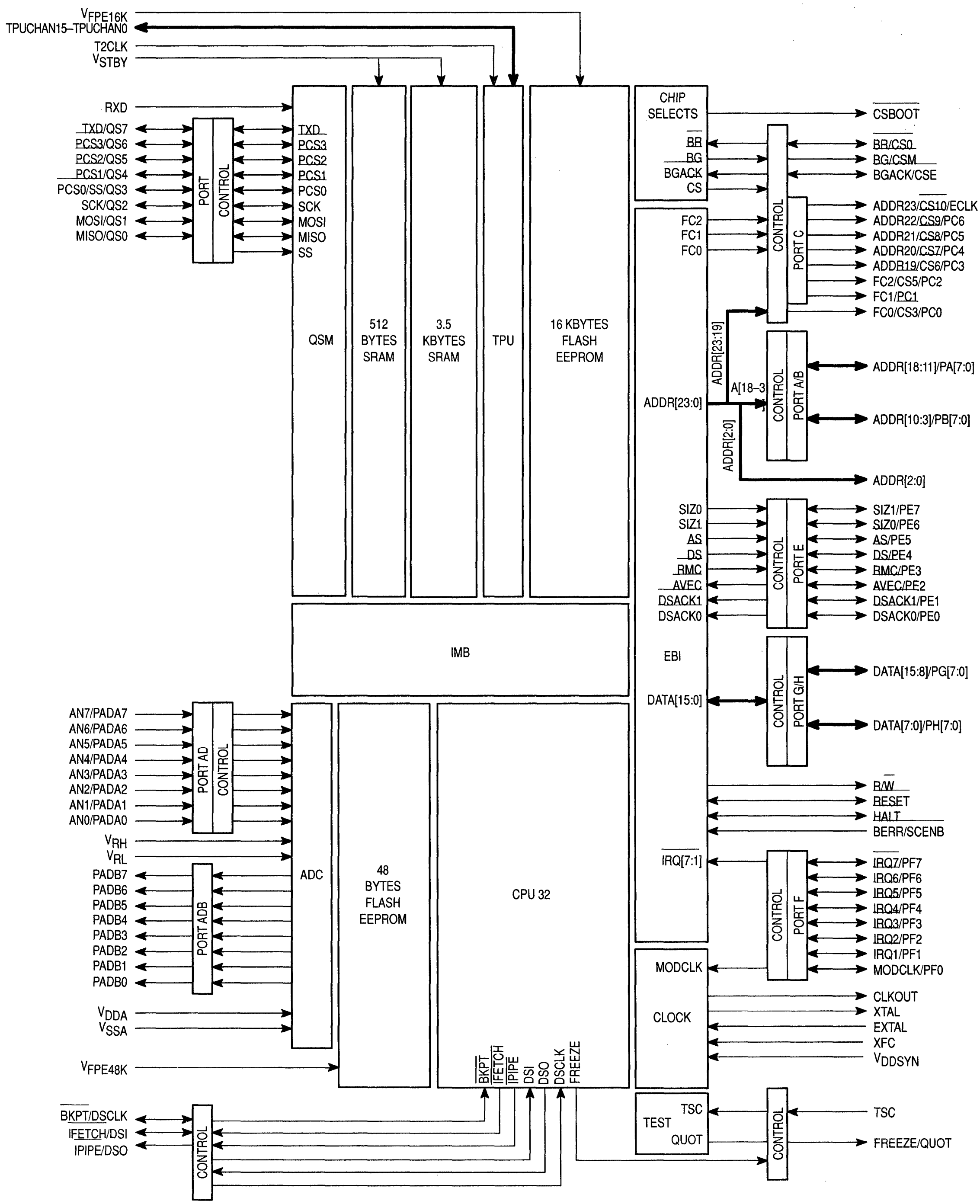


Figure 12. MC68F333 Block Diagram

Table 19. M68300 Family Modular Microcontrollers

Part Number	ROM	SRAM	EEPROM	Timer	I/O	Serial	ADC	Integration Module	Package	Comments
MC68331	–	–	–	GPT	43	QSM	–	SIM	132–FC, 132–FD 144–FM, 144–FV	12 Chip Selects, Synthesized Clock
MC68332	–	2K	–	TPU	47	QSM	–	SIM	132–FC, 132–FD 144–FM, 144–FV	12 Chip Selects, Synthesized Clock
PC68F333	–	4K	16K Flash, 48K Flash Emulator	TPU	96	QSM	8 Ch, 10–Bit	SCIM	160–FT, 160–FM	9 Chip Selects, Synthesized Clock
XC68334	–	1K	–	TPU	47	–	8 Ch, 10–Bit	SIM	132–FC, 132–FD	12 Chip Selects, Synthesized Clock, Single Chip or Expanded Mode

Definitions for Tables 9 and 10

General Definitions

ADC	Analog to Digital Converter Module
A/D	Analog to Digital Converter
CPU16	16 bit Central Processing Unit
CPU32	32 bit Central Processing Unit
D/A	Digital to Analog Converter
DMA	Direct Memory Access
GPT	General–Purpose Timer
IC	Input Capture
IIC	Inter–Integrated Circuit
MCCI	Multi–Channel Communication Interface
PLL	Phase Lock Loop
OC	Output Capture
POQ	Preferred Order Quantity Multiple
PWM	Pulse Width Modulation
QSM	Queued Serial Module
RPSCIM	Reduced Pin Count SCIM
RTC	Real–Time Clock
RTI	Real–Time Interrupt
SCI	Serial Communication Interface
SCIM	Single Chip Integration Module
SIM	System Integration Module
SPI	Serial Peripheral Interface
TPU	Time Processing Unit
UART	Universal Asynchronous Receiver/Transmitter
WDOG	Watch Dog Timer

Package Definitions

FB	10x10 mm Quad Flat Pack (QFP)
FC	Fine Pitch Plastic Quad Flat Pack (PQFP)
FD	Plastic Quad Flat Pack in Molded Carrier Ring
FE	Ceramic Quad Flat Pack (CQFP)
FM	Molded Carrier Flat Pack (CQFP)
FN	Plastic Leaded Chip Carrier (PLCC)
FS	Windowed Cerquad (Ceramic LCC)
FT	28x28 mm Quad Flat Pack (QFP)
FU	14x14 mm Quad Flat Pack (QFP)
FV	20x20 mm Quad Flat Pack (QFP)
L	Ceramic
P	Dual–in–Line Plastic
PB	Thin Quad Flat Pack (TQFP) 10x10 mm
PU	Thin Quad Flat Pack (TQFP) 14x14 mm
PV	Thin Quad Flat Pack (TQFP) 20x20mm
S	Cerdip (windowed or non–windowed)
TH	16x16 mm Quad Flat Pack (QFP)

Microcontroller Development Tools

M68HC05 Family

The M68HC05 Family is supported by a variety of development tools including Evaluation Modules (EVM) and Evaluation Systems (EVS). Both provide an economical means of designing, debugging, and evaluating M68HC05 microcontrollers in a target system environment.

Many new M68HC05 CSIC devices are supported by an MCU–specific EVS. The EVS is a two–board system consisting of a 68HC05 Platform Board (PFB) and an Emulator Module (EM) which contains the emulating microcontroller, and control circuits.

The M68HC05 Family is also supported by the Compact Development System (CDS) for 8–bit microcontrollers (M68CDS8HC05), a powerful, portable, full–featured emulator for debugging hardware and software operations. The CDS8HC05 features high–speed, non–invasive, in–circuit emulation with real–time trace, and a powerful bus state analyzer. Commands are entered from an MS–DOS® host computer.

The Motorola Modular Development System for the M68HC05 Family, MMDS05, allows the use of Emulation Modules (EM) that are compatible with the existing EVS product line. The MMDS05 provides an upgrade for CDS8HC05 customers. The MMDS05 has all of the features of the CDS8HC05, and includes a notable enhancement. A dual–port RAM "memory window" allows a user to to modify memory while a program is running at full speed. An internal power supply and totally shielded enclosure assure compliance with FCC and EC92 regulations. The development software provided with the MMDS05 is an enhancement of the EVM05/EVM11 front end — it provides an integrated development environment with true Source Level Debug (SLD).

M68HC11 Family

The M68HC11 Family is supported by a variety of economical development tools. These include Evaluation Boards (EVB), Evaluation Modules (EVM), and Evaluation Systems (EVS).

An EVB allows a user to debug code under the BUFFALO (Bit User Fast Friendly Aid to Logical Operations) monitor/debugging program contained in the microcontroller ROM. The EVB emulates only the single–chip mode of operation and has no EPROM programmer. The EVBU, a "universal" version of the EVB, includes a wire–wrap area for custom interfacing.

EVM are low–cost tools for designing, debugging, and evaluating M68HC11 devices in a target system. An EVM provides essential microcontroller signals and timing, and on–board monitor/debugging firmware contains extensive commands for controlling I/O and debug operations.

An EVS is a two–board system consisting of a 68HC11 Platform Board (PFB) and an Emulator Module (EM). The EM contains control circuits and a 68HC11 MCU for the part or series of parts being emulated. An EVS provides expanded, multiplexed, special test, and single–chip mode emulation, a dual 64 kbyte memory map with 64 kbytes of emulation RAM, and an RS–232 port.

In addition, the Intermetrics Whitesmiths 68HC11 C Compiler/Assembler (M68S11CCAB) and 68HC11 Simulator Debugger (M68S11SIMAB) are now available through Motorola.

Modular Microcontroller Families

In–circuit debuggers for modular microcontroller families (M68ICD32 and M68ICD16) are economical development and debugging environments. ICD make use of the non–intrusive Background Debug Mode (BDM) interface, and provide sophisticated software debugging functions. The ICD consist of debugger and assembler development software, a small interconnect board, and target system cable. The IASM32 and IASM16 assemblers provide a single development environment that includes an editor and cross–assembler programs. ICD source–level debugger software uses easy–to–read screen windows to display register information for the CPU, the instruction pointer, breakpoints, program memory, and data memory.

The MC68331 and MC68332 are supported by evaluation kits (EVK). These multi–board systems include a common platform board, a Business Card Computer (BCC) that contains the MCU being emulated, and the CPU32BUG debug monitor program. The EVK is a cost–effective system for designing, debugging, and evaluating target system software and hardware. The MC68340 is supported by an evaluation system (EVS) similar to the EVK with the addition of a development interface board for a comprehensive development environment.

The M68HC16Z1 Evaluation Board (EVB) is an inexpensive tool for designing, debugging, and evaluating the MC68HC16Z1. Features include background–mode operation, an integrated assembly/editing/emulation environment, and logic analyzer pod connectors.

Modular evaluation boards (MEVB) for each modular family member are under development. The MEVB system is a multi–board evaluation system that consists of a common platform board (PFB) and interchangeable MCU personality boards (MPB). The MEVB system provides an economical development environment for downloading and debugging software generated with IASM16 and IASM32.

Motorola also sells the Intermetrics Whitesmiths 68HC16 C Compiler/Assembler (M68S16CCAB) and 68HC16 Simulator Debugger (M68S16SIMAB) for the M68HC16 Family. In addition, the Intermetrics InterTools™ 683XX C Compiler/Assembler (M68S32CCAB) and 683XX ROM Monitor Debugger (M68S32ROMAB) for the M68300 Family are now available through Motorola.

Table 20. Development Tools

Devices	Evaluation Modules*	Programmer Boards	Evaluation Systems/Kits
M6800 Development Tools			
MC6801		M68701EVM	
MC6801U4		M68701EVM	
MC68701		M68701EVM	
MC68701U4		M68701EVM	
MC6803		M68701EVM	
MC6803U4		M68701EVM	
M68HC05 Development Tools			
MC68HC05B4/B6/B8/B16 MC68HC705B5 MC68HC705B16	M68HC05X16EVS M68HC05X16EVS M68HC05X16EVS	 M68HC05BPGMR M68HC05BPGMR	52PLCCU: 52 Pin PLCC Target Cable Use M68HC05X16PGMR for 64 QFP
MC68HC05C5 XC68HC705C5	M68HC05C5EVS M68HC05C5EVS		44 PLCC05M: 44 Pin PLCC Target Cable
MC68HC05C4/C4A/C8/C9/C12 XC68HC05C4 MC68HC705C8 XC68HC705C	M68HC05C9EVS M68HC05C9EVS	 M68HC05PGMR–2	44 PLCC05M: 44 Pin PLCC Target Cable
MC68HC05D9/D24 XC68HC05D32 MC68HC705D9	 M68HC05D32EVS M68HC05D32EVS	 M68HC05PGMR–2	44 PLCC05M: 44 Pin PLCC Target Cable
MC68HC05E1 MC68HC705E1	M68HC05E1EVS M68HC05E1EVS		
XC68HC05F2 XC68HC05F6	M68HC05F6EVM		42 SDIP Target Cable Included
XC68HC05F8 XC68HC705F8	M68HC05F8EVM M68HC05F8EVM	 M68HC705F8PGMR	
MC68HC05G1 MC8HC705G1	M68HC05G1EVM M68HC05G1EVM	 M68HC705G1PGMR	
XC68HC05G9 XC68HC705G9	M68HC05G9EVM M68HC05G9EVM	 M68HC705G9PGMR	
XC68HC05G10 XC68HC705G10	M68HC05G10EVM M68HC05G10EVM		
XC68HC05H2	M68HC05H2EVS		
XC68HC05I8 XC68HC705I8	M68HC05I8EVS M68HC05I8EVS	 M68HC705L4PGMR	
MC68HC05J1 MC68HC705J2	M68HC05P8EVS M68HC05P8EVS	 M68HC705J2PGMR	
XC68HC05J3 XC68HC705J3	M68HC05J3EVS M68HC05J3EVS	 M68HC705J2PGMR	
XC68HC05K0/K1 XC68HC705K1		M68HC705KIGANG** Use M68HC705KICS	M68HC705KICS In–Circuit Simulator M68HC705KICS In–Circuit Simulator

* EVSs and EVMs include an Integrated Development Environment (IDE) which contains an editor, assembler and hardware debugger.
* EVSs and EVMs do not include target cables or OTP/EPROM programming capability unless noted in comment section.
** Development tools that are scheduled for availability during 1Q94.

Table 20. Development Tools (continued)

Devices	Evaluation Modules*	Programmer Boards	Evaluation Systems/Kits
M68HC05 Development Tools (continued)			
XC68HC05L1 XC68HC705L1	M68HC05L1EVM M68HC05L1EVM		56 SDIP Target Cable Included
XC68HC05L2 XC68HC705L2	M68HC05L2EVS M68HC05L2EVS	 M68HC705L2PGMR	
XC68HC05L4 XC68HC705L4	M68HC05L4EVS M68HC05L4EVS	 M68HC705L4PGMR	M68SDIP64: 64 Pin SDIP Target Cable
MC68HC05L5 MC68HC705L5	M68HC05L5EVS M68HC05L5EVS	 M68HC705L5PGMR	80QFPUKIT: 80 Pin QFP Target Cable
MC68HC05L7/L9	M68HC05L9EVM2		
MC68HC05L10	M68HC05L10EVM		
XC68HC05L11	M68HC05L11EVM		
XC68HC05M4	M68HC05M4EVM		
XC68HC05P3	M68HC05P3EVS		
MC68HC05P1/P4/P6/P7/P9 XC68HC705P9	M68HC05P9EVS M68HC05P9EVS	 M68HC705P9PGMR	XMDS05 Hi–Performance In–Circuit Emulator 68HC705P6 is required for P6 EVS Capability
MC68HC05P8	M68HC05P8EVS		
XC68HC05SC11/SC21/SC24/SC27	M68HC05SCEVS		ISO Adaptor Included with M68HC05SCEVS
MC68HC05T1 XC68HC05T2/T3	M68HC05T2EVS		
XC68HC05T4	M68HC05T4EVM		
MC68HC05T7/T10 XC68HC705T10	M68HC05T7EVM M68HC05T7EVM	 M68HC705T10PGMR	
XC68HC05T12 XC68HC705T12	M68HC05T12EVM M68HC05T12EVM	 M68HC705T12PGMR	
XC68HC05X4 XC68HC705X4	M68HC05X4EVS M68HC05X4EVS	 M68HC705X4PGMR	
XC68HC05X16 MC68HC705X16	M68HC05X16EVS M68HC05X16EVS	 M68HC705X16PGMR	68 PLCCU: 68 Pin PLCC Target Cable
M68HC11 Development Tools			
MC68HC11A0/A1/A8	M68HC11EVB M68HC11EVB2 M68HC11EVBU	M68HC11EVM	
MC68HC11D0/D3		M68HC11EVM	M68HC11D3EVS
MC68HC711D3	M68HC711D3EVB	M68HC11EVM	M68HC11D3EVS
MC68HC11E0/E1/E2/E9	M68HC11EVB M68HC11EVBU	M68HC11EVM	
MC68HC711E9	M68HC11EVBU	M68HC11EVM	
MC68HC811A8/E2	M68HC11EVB M68HC11EVBU	M68HC11EVM	

* EVSs and EVMs include an Integrated Development Environment (IDE) which contains an editor, assembler and hardware debugger.
* EVSs and EVMs do not include target cables or OTP/EPROM programming capability unless noted in comment section.
** Development tools that are scheduled for availability during 1Q94.

Table 20. Development Tools (continued)

Devices	Evaluation Modules*	Programmer Boards	Evaluation Systems/Kits
M68HC11 Development Tools (continued)			
MC68HC11F1			M68HC11F1EVS
MC68HC11G5/G7 MC68HC711G5			M68HC11G7EVS
MC68HC11KA4			M68HC11KA4EVS
MC68HC11K0/K1/K4 MC68HC711K4			M68HC11K4EVS
MC68HC11L0/L1/L6 MC68HC711L6			M68HC11L6EVS
MC68HC11M2 MC68HC711M2			M68HC11KMNPEVS
MC68HC11N4 MC68HC711N4			M68HC11KMNPEVS
MC68HC11P2 MC68HC711P2			M68HC11KMNPEVS
M68HC16 Development Tools			
MC68HC16Y1	MG8MEVB16Y1		
MC68HC16Z1	M68MEVB16Z1		
MC68HC16Z2	M68MEVB16Z1		
M68300 Development Tools			
MC68331	M68MEVB333		M68331EVK
MC68332	M68MEVB16Z1		M68332EVS/M68332EVK
MC68F333 MC6805R2/R3	M68MEVB333		

* EVSs and EVMs include an Integrated Development Environment (IDE) which contains an editor, assembler and hardware debugger.
* EVSs and EVMs do not include target cables or OTP/EPROM programming capability unless noted in comment section.
** Development tools that are scheduled for availability during 1Q94.

Fuzzy Logic

Fuzzy logic replaces conventional programming techniques with a simpler approach to control algorithms. Fuzzy logic uses a series of case statements to create sophisticated features that do not require additional memory or excessive processing time.

Motorola's portfolio of fuzzy logic products is geared for every level of user. The fuzzy logic educational kit (part number FLEDKT00) includes everything needed to learn how to use fuzzy logic with M68HC05 and M68HC11 microcontrollers.

- An easy–to–follow PC–based tutorial
  - Explains fuzzy logic fundamentals, basic concepts and terminology
  - Methodology section teaches a five–step sequence or principles and procedures for designing a fuzzy logic system. These include defining the control system, writing rules and membership functions, tuning and debugging and optimizing the design.
  - Advanced topics section covers areas such as stability, adaptability, ambiguity, noise, alpha–cuts and contribution weights
- A Knowledge Base Generator (KBG)
  - Uses natural language inputs to generate a knowledge base (rules and membership functions)
  - Inference Engines for the M68HC11 and M68HC05 families implement the fuzzy logic in software ready to embed in your Motorola microcontroller application
  - Runs a software simulation of the inference engine and displays a two–dimensional plot of the control surface
  - Generates real–time code for the standard M68HC05 or M68HC11 microcontroller families which can be downloaded to an evaluation module (EVM) for in–circuit emulation
- Demonstration–version of Aptronix's Fuzzy Inference Development Environment (FIDE) software
  - Features powerful, time–saving debug functions to help determine the correct membership functions and rules for any application
  - Demonstrates easy–to–use graphical interface for designing and debugging integrated systems

Aptronix's Fuzzy Inference Development Environment (FIDE™) is a powerful software tool that allows users to easily edit, simulate, debug, and tune the membership functions and rules of a fuzzy logic application. FIDE offers graphical and natural language editing of source files. The user–friendly debug tools allow time domain simulations, three–dimensional surface displays of input–to–output relationships, and linkage of fuzzy and non–fuzzy modules. FIDE also generates assembler code that implements fuzzy logic on Motorola microcontrollers.

On–Line Help

Microcontroller Electronic Bulletin Board

Freeware Data Service provides a direct line to the latest information and software for Motorola microcontrollers. The Freeware bulletin board provides access to:

- Development Software for PC and Macintosh Computers
  - Cross Assemblers
  - Small C Compiler for 68HC11
  - EVM and EVB Monitor/Debugger Object Code
- Development software
  - Floating Point Routines
  - Fast Fourier Transform Routines
  - 16–Bit Math Packages
  - Utility Programs
  - User Group Library Routines and User–Donated Programs
  - Kermit File Transfer Program
  - Terminal Emulation Program
- Masked ROM information
- MCU literature listings
- Updates/Erratas to existing literature
- Press releases and updates concerning new and phase–out products
- Contests, promotions and seminars
- Electronic mail service

How to Access Freeware

You can access Freeware from anywhere in the world. To log on, you'll need the following equipment:

1. 2400/1200/300 baud modem
2. Terminal, MS–DOS personal computer or Macintosh computer
3. Telephone line

This equipment will allow the user to read files and post questions. However, with a file transfer program such as XMODEM, YMODEM or Kermit, all information can be downloaded to your terminal or PC.

To log on:

1. Dial (512) 891–FREE (891–3733). Be sure to set the character format to 8 data, no parity, 1 stop bit.
2. Follow directions from the system.
3. Read log–on messages, then follow the directions on the screen display. A log–on session is limited to 120 minutes.

Third–Party Support

Development support for Motorola microcontrollers is available from a variety of independent suppliers.

Third–Party Development Tools

Table 21. Software Products

M68HC05 Family	M68HC11 Family	M68HC16 Family	M68300 Family
Simulators			
Byte Craft Ltd.	Avocet Systems, Inc.	P&E Microcomputer Systems, Inc.	Software Environments Ltd.
P&E Microcomputer Systems, Inc.	Nohau Corp.		
PseudoCorp.	P&E Microcomputer Systems, Inc.		
TECi			
Assemblers			
2500AD Software, Inc.	2500AD Software, Inc.	2500AD Software, Inc.	Avocet Systems, Inc.
American Arium	Archimedes Software, Inc.	Byte Craft Ltd.	Eyring Systems Software Division
Byte Craft Ltd.	Avocet Systems, Inc.	Eris Systems, Inc.	Introl Corp.
Computer Systems Consultants, Inc.	Computer Systems Consultants, Inc	Introl Corp.	Micro Dialects, Inc.
Eris Systems, Inc.	Eris Systems, Inc.	Micro Dialects, Inc.	Microtec Research, Inc.
Introl Corp.	Introl Corp.	P&E Microcomputer Systems, Inc.	Oasys, Inc.
Lloyd I/O, Inc.	Lloyd I/O, Inc.		
LOGISOFT	LOGISOFT		
Micro Dialects, Inc.	Micro Dialects, Inc.		
Onset Computer Corp.			
P&E Microcomputer Systems, Inc.			
PseudoCorp.			
TECi			
Symbolic Debuggers			
2500AD Software, Inc.	2500AD Software, Inc.	Byte Craft Ltd.	Eyring Systems Software Division
Byte Craft Ltd.	Microtec Research, Inc.		Integrated Systems, Inc.
P&E Microcomputer Systems, Inc.	P&E Microcomputer Systems, Inc.		JMI Software Consultants, Inc.
TECi	TECi		
Wytec Company			
Compilers			
American Arium	2500AD Software, Inc.	Byte Craft Ltd.	Eyring Systems Software Division
Byte Craft Ltd.	Archimedes Software, Inc.	Intermetrics Microsystems Software, Inc.	Forth, Inc.
	Avocet Systems, Inc.	Introl Corp.	Integrated Systems, Inc.
	Forth, Inc.	Software Environments Ltd.	Intermetrics Microsystems Software, Inc.
	Intermetrics Microsystems Software, Inc.		Introl Corp.
	Introl Corp.		Laboratory Microsystems Inc.
	Laboratory Microsystems Inc.		Microtec Research, Inc.
	New Micros, Inc.		Microware Systems Corp.
	Software Environments Ltd.		RAVEN Computer Systems
	SYNGEN Industrial Control		Sierra Systems

Table 21. Software Products (continued)

M68HC05 Family	M68HC11 Family	M68HC16 Family	M68300 Family
Source Level Debuggers			
Byte Craft Ltd.	Huntsville Microsystems, Inc.	Huntsville Microsystems, Inc.	Embedded Support Tools Corp.
Yokogawa Digital Computer Corp.	Intermetrics Microsystems Software, Inc.	Intermetrics Microsystems Software, Inc.	Eyring Systems Software Division
	Introl Corp.	Introl Corp.	GreenSpring Computers, Inc.
	Yokogawa Digital Computer Corp.	Yokogawa Digital Computer Corp.	Huntsville Microsystems, Inc.
			Integrated Systems, Inc.
			Intermetrics Microsystems Software, Inc.
Introl Corp.			
			Microtec Research, Inc.
			Sierra Systems
			Yokogawa Digital Computer Corp.
Real–Time Executives			
	Accelerated Technology, Inc.	A. T. Barrett & Associates	Accelerated Technology, Inc.
	A. T. Barrett & Associates	U S Software Corporation	A. T. Barrett & Associates
	U S Software Corporation		Eyring Systems Software Division
			GreenSpring Computers, Inc.
			Integrated Systems, Inc.
			JMI Software Consultants, Inc.
			Microware Systems Corp.
			Ready Systems
			U S Software Corporation
Other			
PsuedoCorp	Logic Automation Inc.	Momentum Data Systems, Inc.	Avocet Systems, Inc.
	LOGISOFT	U S Software Corporation	CARDtools Systems Corp.
	PsuedoCorp		Eyring Systems Software Division
	U S Software Corporation		GreenSpring Computers, Inc.
			Integrated Systems, Inc.
			JMI Software Consultants, Inc.
			Logic Automation Inc.
			Microware Systems Corp.
			U S Software Corporation

Table 22. Hardware Products

M68HC05 Family	M68HC11 Family	M68HC16 Family	M68300 Family
Logic Analyzers			
	American Arium Hewlett–Packard Step Engineering Tektronix, Inc.	Hewlett–Packard Tektronix, Inc.	Hewlett–Packard
Emulators			
American Arium Orion Instruments, Inc. Pentica Systems Inc. Sophia Systems & Technology TECi Thorson Engineering Co. Trace Technology Ltd. Yokogawa Digital Computer Corp.	Advance Electronic Diagnostics, Inc. American Arium Huntsville Microsystems, Inc. MetaLink Corp. Nohau Corp. Orion Instruments, Inc. Pentica Systems Inc. Sophia Systems & Technology TECi Thorson Engineering Co. Wytec Company Yokogawa Digital Computer Corp.	Embedded Support Tools Corp. Huntsville Microsystems, Inc. Nohau Corp. Pentica Systems, Inc. Yokogawa Digital Computer Corp.	Advance Electronic Diagnostics, Inc. Applied Microsystems Embedded Support Tools Corp. Hewlett–Packard Huntsville Microsystems, Inc. Microtek International Nohau Corp. Pentica Systems Inc. Yokogawa Digital Computer Corp.
Evaluation Boards			
Elan Digital Systems	Elan Digital Systems Mosaic Industries, Inc. New Micros, Inc.	New Micros, Inc.	GreenSpring Computers, Inc. New Micros, Inc.
Other			
3M Electronic Products Division AMP Inc. EE Tools Co. Elan Digital Systems Pentica Systems Inc. TECi	3M Electronic Products Division AMP Inc. Elan Digital Systems Emulation Technology, Inc. Pentica Systems Inc. SYNGEN Industrial Control	AMP Inc. P&E Microcomputer Systems, Inc.	Emulation Technology, Inc Pentica Systems Inc.

Table 23. Contact List

Company	Phone
3M Electronic Products Division	(512) 984–3441
2500AD Software, Inc.	(719) 395–8683
A. T. Barrett & Associates	(713) 728–9688
Accelerated Technology, Inc.	(205) 450–0707
Advance Electronic Diagnostics, Inc.	(602) 861–9359
American Arium	(714) 731–1661
AMP Inc.	(800) 52AMP52
Applied Microsystems	(800) 426–3925
Archimedes Software, Inc.	(415) 567–4010
Avocet Systems, Inc.	(800) 448–8500
Byte Craft Ltd.	(519) 888–6911
CARDtools Systems Corp.	(408) 559–4240
Computer Systems Consultants, Inc	(404) 483–4570
EE Tools Co.	(716) 346–6973
Elan Digital Systems	(4489) 579799
Embedded Support Tools Corp.	(617) 828–5588
Emulation Technology, Inc.	(408) 982–0660
Eris Systems, Inc.	(612) 374–2967
Eyring Systems Software Division	(801) 375–2434
Forth, Inc.	(213) 372–8493
GreenSpring Computers, Inc.	(415) 327–1200
Hewlett–Packard	(800) 447–3282
Huntsville Microsystems, Inc.	(205) 881–6005
Integrated Systems, Inc.	(408) 980–1500
Intermetrics Microsystems Software, Inc.	(617) 661–0072
Introl Corp.	(414) 327–7171
JMI Software Consultants, Inc.	(215) 628–0840
Laboratory Microsystems Inc.	(310) 306–7412
Lloyd I/O, Inc.	(503) 222–0702
Logic Automation Inc.	(503) 690–6900
LOGISOFT	(408) 773–8465
MetaLink Corp.	(602) 926–0797
Micro Dialects, Inc.	(513) 271–9100
Microtec Research, Inc.	(408) 980–1300
Microtek International	(503) 645–7333
Microware Systems Corp.	(515) 224–1929
Momentum Data Systems, Inc.	(714) 577–6894
Mosaic Industries, Inc.	(415) 790–1255
New Micros, Inc.	(214) 339–2204
Nohau Corp.	(408) 866–1820
Oasys, Inc.	(617) 862–2002

Table 23. Contact List (continued)

Company	Phone
Onset Computer Corp.	(508) 563–9000
Orion Instruments, Inc.	(800) 729–7700
P&E Microcomputer Systems, Inc.	(617) 944–7585
Pentica Systems Inc.	(617) 275–4419
PseudoCorp.	(804) 873–1947
RAVEN Computer Systems	(612) 636–0365
Ready Systems	(800) 228–1249
Sierra Systems	(510) 339–8200
Software Environments Ltd.	(714) 588–9685
Sophia Systems & Technology	(800) 824–9294
Step Engineering	(408) 733–7837
SYNGEN Industrial Control	(403) 986–1203
TECi	(802) 525–3458
Tektronix, Inc.	(503) 629–1773
Thorson Engineering Co.	(206) 334–4214
Trace Technology Ltd.	0234 266 455
U S Software Corporation	(503) 641–8446
Wytec Company	(708) 894–1440
Yokogawa Digital Computer Corp.	(415) 570–7050

LonWorks™ Neuron IC Products

In Brief . . .

Motorola's Neuron® Chip processors are sophisticated VLSI devices that make it possible to implement low–cost Local Operating Network applications. The unique combination of hardware and firmware provides all the key functions necessary to process inputs from sensors and control devices intelligently, and propagate control information across a variety of network media.

Used in conjunction with the LonBuilder™ Developer's Workbench or the NodeBuilder™ Development Tool, the Neuron Chips make available to a system designer an object–oriented, high–level environment providing for the easy implementation of distributed sense and control networks, flexible reconfiguration capability after network installation, and management of LonTalk™ protocol messages on the network.

Applications include distributed sense and control systems, instrumentation, machine automation, processor control, diagnostic equipment, environmental monitoring and control, power distribution and control, production control, lighting control, building automation and control, security systems, data collection/acquisition, robotics, home automation, consumer electronics, and automotive electronics.

NEURON CHIPS

Motorola's NEURON CHIPS, the MC143120 and MC143150, are the brains behind LONWORKS technology. These VLSI devices are specifically designed for distributed systems where sensing, processing, control, and communication are paramount. With LONWORKS development tools and software, they form a complete system solution that provides easy development of Local Operating Networks.

The power of both chips lies in their three respective on-board CPUs, high-speed serial communications ports (up to 1.25 MBps), and LONTALK communications protocol which is based on the OSI reference model. The difference between the two integrated circuits lies in the type and size of memory configuration; the MC143120 is targeted for cost-sensitive designs with small application programs running in internal EEPROM; the MC143150 is for larger systems with expanded memory requirements.

MC143120 Features

The MC143120B1DW/MC143120E2DW is a complete system-on-a-chip that integrates 10K ROM, 1K/2K RAM, and 512 bytes EEPROM. The ROM is used for storing LONTALK protocol, operating system, and 24 I/O models that can be accessed by the application program. An additional 10 I/O models are loaded into EEPROM if needed. Application program data is stored in RAM or the internal EEPROM. The application program and system configuration data reside in the MC143120's internal EEPROM. The MC143120 is available in a 32-pin SOG.

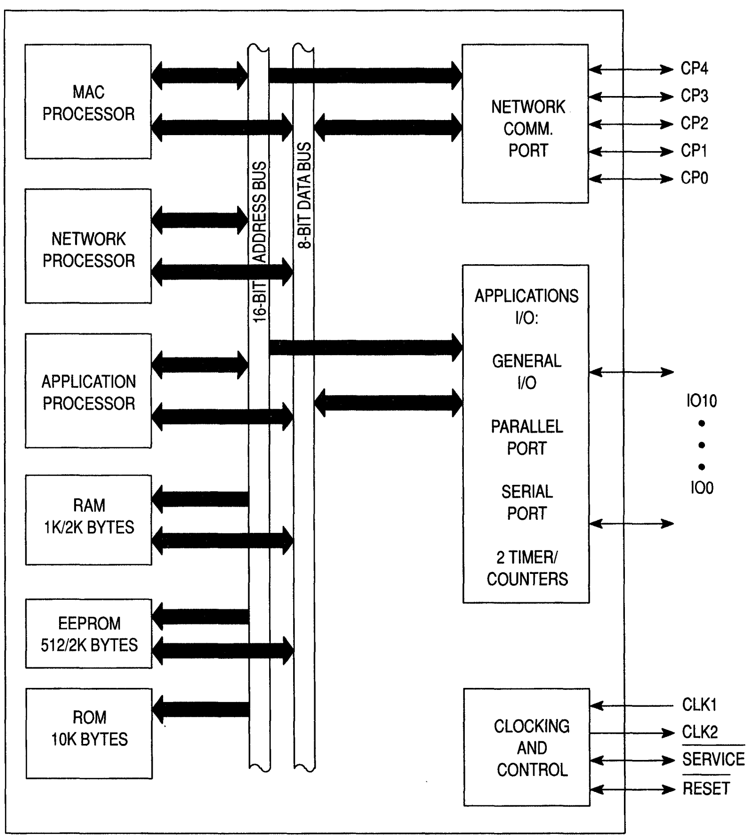


Figure 13. MC143120 (32–Lead SOG)

MC143150 Features

The MC143150 contains an additional 1K of on–chip RAM (2K total) but no on–board ROM. An external memory interface allows the system designer to use 42K of the available 64K of address space for application program storage. The remaining address space is reserved for LONTALK communications protocol, operation system, and up to 34 I/O models which are supplied with the LONBUILDER Developer's Workbench or NODEBUILDER Development Tool. The protocol and application code can be located in external ROM, EEPROM, NVRAM, or battery–backup static RAM. The MC143150 is available in a 64–pin QFP.

Shared Strengths

Of the three processors on–board each NEURON CHIP, two (MAC and Network processors) implement a communication subsystem, enabling the automatic transfer of information from node to node. The remaining processor handles the application program. The NEURON IC supports a maximum clock rate of 10 MHz.

Both NEURON CHIPS have eleven I/O pins (IO.0 — IO.10) to provide flexible interfacing to external hardware and access to two internal timers/counters. IO.4 — IO.7 have optional pull–up resistors. Pins IO.0 — IO.3 have high current sink capability (20 mA @ 0.8 V) while the others have a standard sink capability of 1.4 mA @ 0.4 V. All I/O pins have TTL–level inputs with hysteresis.

There are two versions of the MC143150 NEURON IC that offer different cost and technical advantages. The MC143150FU operates up to a maximum clock rate of 10 MHz over a temperature range of −40 to +85°C. The MC143150FU1 is a lower cost device that operates up to 5 MHz over the same temperature range and consumes less power. The key difference between the two ICs is in the cost saving gained by using an external 200 ns EPROM memory device with the MC143150FU1 as opposed to a 90 ns memory device for a 10 MHz clock rate with the MC143150FU.

Integrated Circuits

Motorola Part No.	Description	Leads–Package	Samples	Production	Document#
MC143120DW	NEURON IC 1K RAM/512 EEPROM/10K ROM, 10 MHz, 1.2 µm	32–SOG	Phase Out	Phase Out	BR1134/D DL159/D
MC143120B1DW	NEURON IC 1K RAM/512 EEPROM/10K ROM, 10 MHz, 0.8 µm	32–SOG	Now	Now	
MC143150FU	NEURON IC 2K RAM/512 EEPROM, 10 MHz, 1.2 µm	64–PQFP	Phase Out	Phase Out	
MC143150FU1	NEURON IC 2K RAM/512 EEPROM, 5 MHz, 1.2 µm	64–PQFP	Now	Now	
MC143150B1FU	NEURON IC 2K RAM/512 EEPROM, 10 MHz, 0.8 µm	64–PQFP	Phase Out	Phase Out	
MC143150B1FU1	NEURON IC 2K RAM/512 EEPROM, 10 MHz, 0.8 µm	32–SOG	1Q95	1Q95	
MC143120E2DW	NEURON IC 2K RAM/2K EEPROM, 10 MHz, 0.71 µm	32–SOG	4Q95	1Q96	

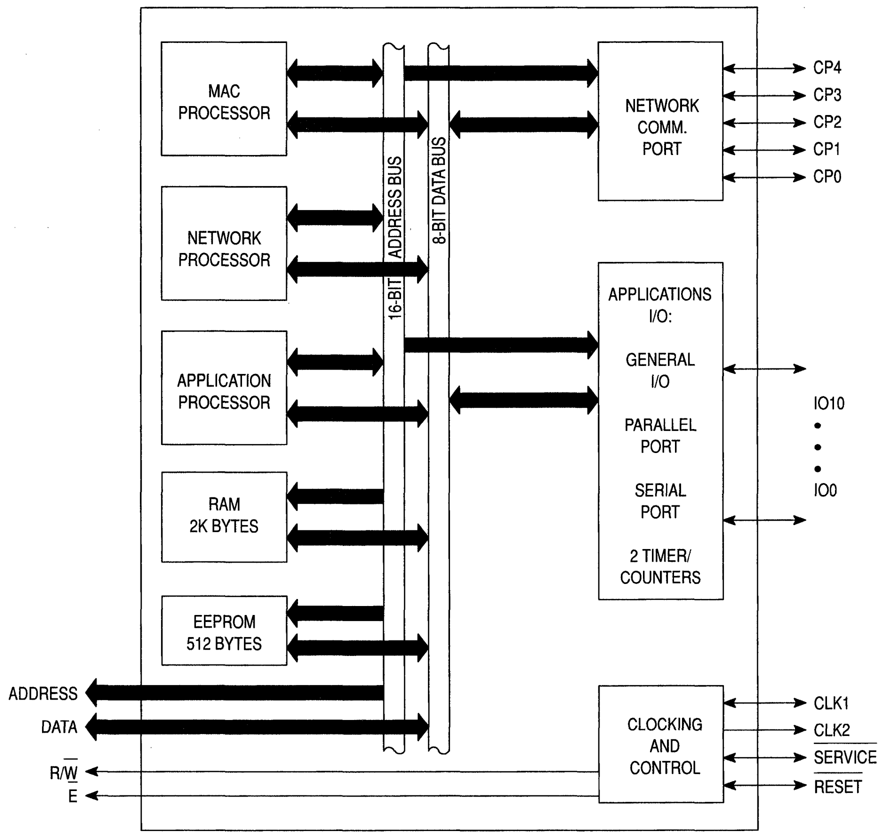


Figure 14. MC143150 (64–Lead PQFP)

LonWorks Technology Overview and Architecture

LonWorks technology is a complete solution for implementing distributed control networks. These networks consist of nodes that communicate with one another over a variety of communications media using LonTalk protocol, a common, message–based communications protocol. In a LonWorks application, nodes sense, monitor, count, measure time, manage switches and relays, and respond to conditions reported by other smart nodes.

LonWorks technology includes all of the hardware and firmware functions needed to process data within nodes and to communicate information among nodes through a variety of network physical layers. In one convenient package, designers can now access all the elements required to design, install, and support control networks. Those elements include: the MC143150 and MC143120 Neuron Chips, LonWorks transceivers, the LonBuilder Developer's Workbench, and LonTalk protocol.

LonTalk protocol features seven layers, each optimized for control networks, and is based on the OSI reference model. LonTalk protocol is embedded within the firmware of Motorola's Neuron Chips and is the foundation of the LonWorks technology networking solution.

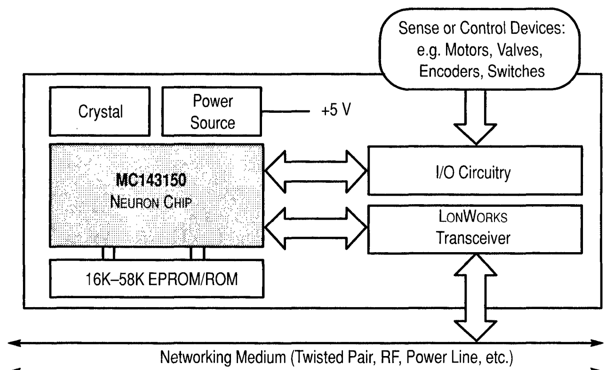


Figure 15. MC143150 in a Typical Node Block Diagram

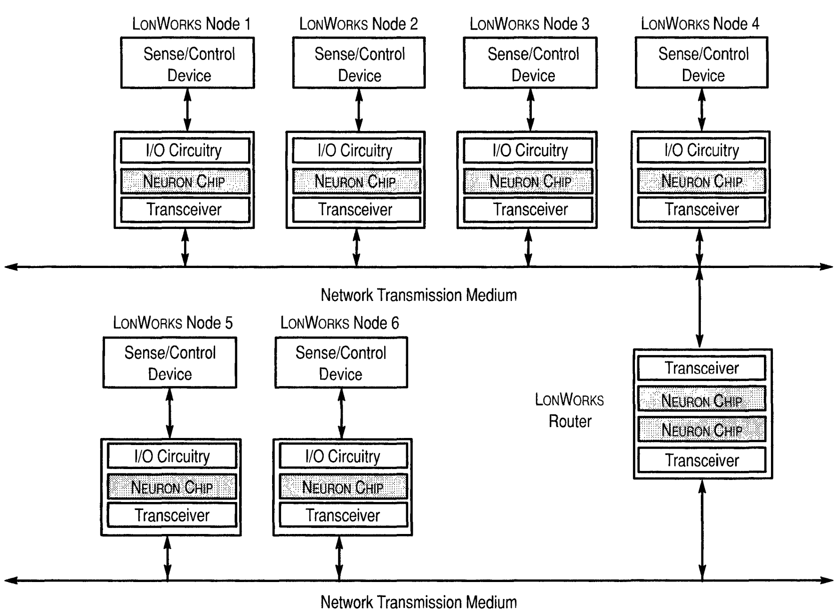


Figure 16. The MC143150 or MC143120 in a LonWorks Network

LonBuilder Developer's Workbench(1)

Thanks to Echelon's LonBuilder and NodeBuilder tools, as well as Motorola's extensive technical support network, both system and device manufacturers can now develop control networks quickly and inexpensively. These tools provide developers with everything needed to begin building LonWorks–based products immediately. The NodeBuilder Development Tool is used to design individual LonWorks products while the LonBuilder Developer's Workbench features the tools required to develop systems consisting of multiple LonWorks nodes. Best of all, technical support for LonWorks technology is available worldwide through Motorola's 30 LonWorks design centers.

LonBuilder Developer's Workbench combines three development tools — a multi–node development system, a network manager, and a protocol analyzer — into an integrated hardware and software development environment. This development system provides the tools to create software applications and prototype hardware on a network ranging from two to hundreds of nodes. The network manager installs and configures nodes during development, making them easy to connect, define, and build. The protocol analyzer monitors the network and interprets its activity.

The LonBuilder Developer's Workbench includes two PC interface cards, two LonWorks transceivers, an expandable development station with two Neuron Chip emulator cards, DOS–based software for compiling, loading, integrating and testing LonWorks applications, and Windows–based software for monitoring and controlling a LonWorks application.

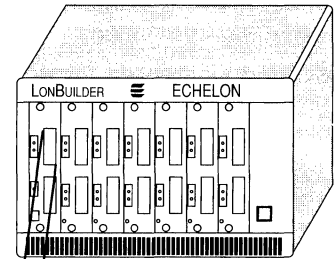
The LonWorks NodeBuilder Development Tool is used to design LonWorks nodes. The NodeBuilder tool does not include the system integration and test tools incorporated into the LonBuilder Developer's Workbench, but does include all the tools required to compile, load, and test code for a LonWorks node. NodeBuilder includes Windows–based software, a PC interface card, a prototype LonWorks node, and two LonWorks transceivers that are used to develop and test LonWorks nodes.

The LonBuilder development tool requires a PC with an available 8– or 16–bit slot, DOS 3.3 or higher, 64K bytes of RAM, mouse, and a hard disk with 10M bytes of available storage. The NodeBuilder tool requires a Microsoft® Windows–compatible PC with an available 16–bit slot, 8M bytes of RAM, mouse, and a hard disk.

(1) Motorola supports these tools, but they should be purchased through Echelon Corporation (1–800–258–4566).

LonWorks Support Tools

Motorola's LonBuilder support tools offer the user a quick and flexible means to demonstrate or test a LonWorks based product which was developed and debugged on the LonBuilder Developer's Workbench. The family of tools consist of Neuron Chip based development boards, I/O application boards, a Differential Direct Connect Transceiver Board (for the LonBuilder Developer's Workbench), and a



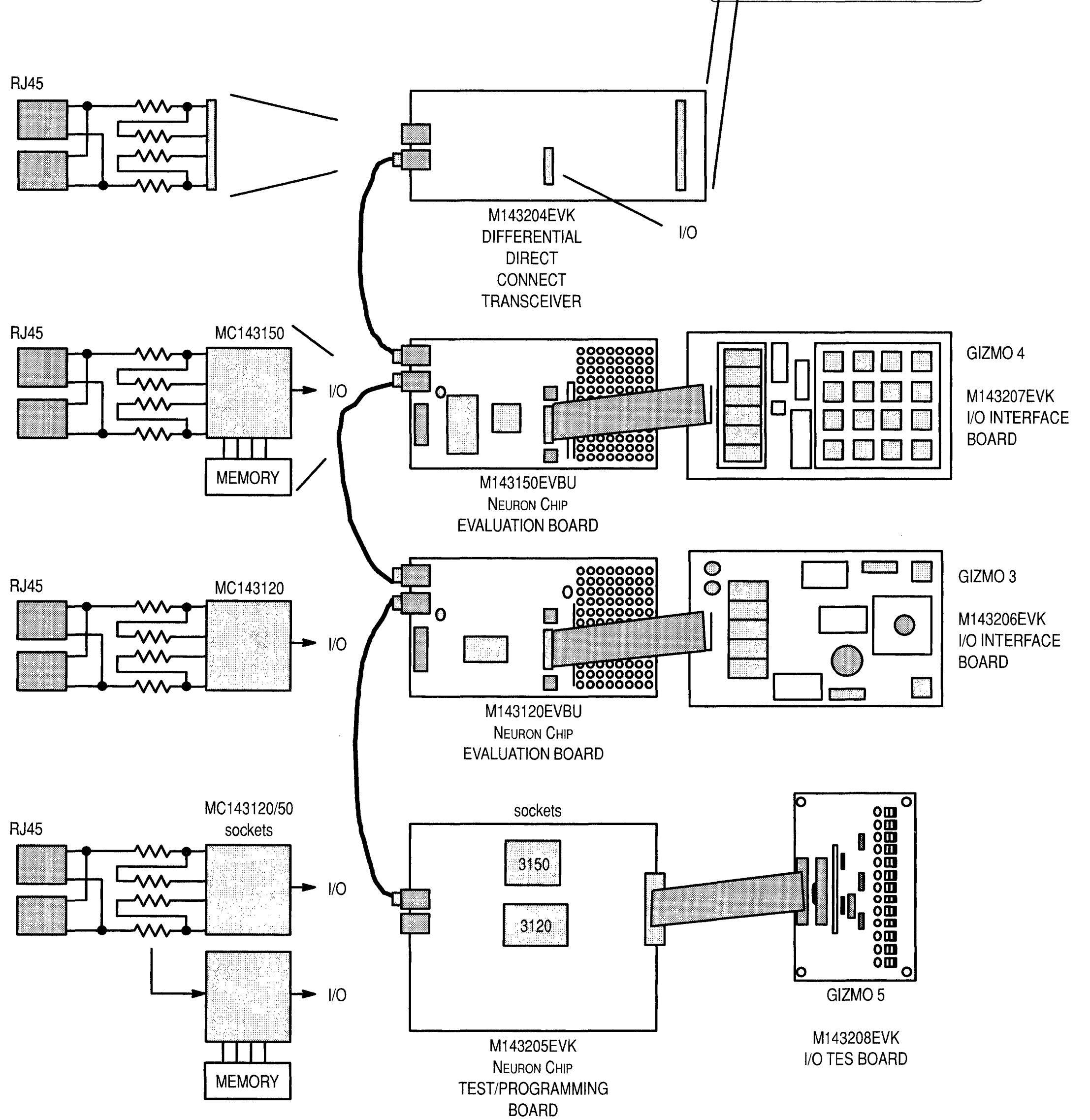


Figure 17. Evaluation and I/O Interface Boards

NEURON CHIP Test/Programming Board. The unique advantages that these tools offer are:

- The boards all have RJ45 connectors allowing ease of connectivity.
- The NEURON CHIP boards contain a 5 volt regulator allowing for a wider range of power supply voltages.
- A common 2 x 10 connector for interface to the NEURON CHIP I/O pins.
- A library of application functions are available from Motorola.
- An inexpensive means of demonstrating LONWORKS based products.

This document covers a brief detail on each of the boards. For further information, contact Motorola's LONWORKS applications support team in Austin, Texas at 512–505–8330 or FAX 512–505–8312.

Motorola Support Tools for LONWORKS

Motorola Part No.	Description	Production	Document#
M143120EVK	143120 NEURON IC Custom Node Development Board with Socket, Supports all MC143120 NEURON Chips		BR1139
M143120B1EVBU	MC143120B1DW NEURON IC Custom Node Development Board		
M143150EVK	MC143150FU NEURON IC Custom Node Development Board		
M143150B1EVBU	MC143150B1FU NEURON IC Custom Node Development Board		
M143204EVK	Direct Connect Transceiver Board		
M143206EVK	NEURON IC I/O Interface Board (Gizmo 3)		
M143207EVK	NEURON IC I/O Interface Board (Gizmo 4)		
M143208EVK	NEURON IC I/O Interface Test Board (Gizmo 5)		
M143213EVK5	NEURON IC RF Radio with EIA–232 Interface (US Version)		
M143213EVK6	NEURON IC RF Radio with EIA–232 Interface (European Version)		
M143214EVK5	NEURON IC RF Radio with I/O Interface (US Version)		
M143214EVK6	NEURON IC RF Radio with I/O Interface (European Version)		
M143215EVK5	RF Radio for Router Interface (US Version)		
M143215EVK6	RF Radio for Router Interface (European Version)		
M143221EVK	EIA–232 EVBU Interface Board		
M143222EVK	Intelligent Neuron IC Cards (5 Cards, to be used with M143223EVK Card Reader)		
M143223EVK	NEURON Chip Card Reader Board (to be used with M143222EVK Cards)		
M143226EVK	Intelligent NEURON IC Kit with UART Port		
M143232EVK	ADPCM Voice Application Kit		

LonWorks Literature

Motorola Document No.	Echelon No.	Description
DL159/D		LonWorks Technology Device Data
BR1134/D		Neuron Chip Product Overview
BR1139/D		LonWorks Support Tools

Current versions (Q4/95) of the following Engineering Bulletins and Application Notes are incorporated into Motorola publication DL159/D, *LonWorks Technology Device Data*.

AN1208/D		Parallel I/O Interface to the Neuron Chip
AN1211/D		Interfacing DACs and ADCs to the Neuron IC
AN1216/D		Setback Thermostat Design Using the Neuron IC
AN1225/D		Fuzzy Logic and the Neuron Chip
AN1247/D		MC683XX to Neuron Chip Parallel I/O Interface
AN1248/D		Interfacing the PSD3XX to the MC143150
AN1250/D		Low–Cost PC Interface to LonWorks Based Nodes
AN1251/D		Programming the MC143120 Neuron Chip
AN1252/D		MIP Guidelines and Design Issues
EB146/D	005–0003–01A	Neuron Chip Quadrature Input Function Interface
EB147/D	005–0006–01B	LonWorks Installation Overview
EB148/D	005–0001–01B	Enhanced Media Access Control with Echelon's LonTalk Protocol
EB149/D	005–0011–01A	Optimizing LonTalk Response Time
EB150/D	005–0009–01A	Neuron Chip EIA–485 Transceiver
EB151/D	005–0004–01A	Scanning a Keypad with the Neuron Chip
EB152/D	005–0002–01A	How to Use SNVTs in LonWorks Applications
EB153/D	005–0014–01B	Driving a Seven–Segment Display with the Neuron Chip
EB155/D	005–0019–01B	Analog–to–Digital Conversion with the Neuron Chip
EB157/D	005–0016–01B	Creating Applications with the LonBuilder Multi–Function I/O Kit
EB159/D	005–0022–01B	Neuron Chip–Based Installation of LonWorks Networks
EB161/D	005–0017–01B	LonTalk Protocol
EB167/D	005–0043–01A	A Hybrid System for Fast Synchronized Response
EB168/D	005–0008–01C	EIA–232C Serial Interfacing with the Neuron Chip
EB169/D	005–0032–01C	LonWorks 78 kbps Self–Healing Ring Architecture
EB170/D	005–0010–01A	LonTalk Response Time Measurements
EB171/D	005–0013–01B	Neuron 3150 Chip External Memory Interface
EB172/D	005–0024–01A	LonWorks Custom Node Development
EB173/D	005–0027–01F	The SNVT Master List and Programmer's Guide
EB174/D	005–0023–01A	Junction Box and Wiring Guidelines for Twisted Pair LonWorks Networks
EB175/D	005–007–01G	Neuron C Extended Arithmetic Support

The following documents can be ordered from Echelon Corporation.

078–0001–01A	LonBuilder User's Guide
078–0002–01	Neuron C Programmer's Guide
078–0140–01	Neuron C Reference Guide

Contact Motorola or Echelon (415–855–7400) for additional documentation.

Memory Products

In Brief . . .

Motorola's memory product portfolio has been expanded to support a broad range of engineering applications. Included in this portfolio are asynchronous devices with access times of 6 ns at 256K–bit density, 6 ns at 5 V 1 Megabit density, 8 ns at 3.3 V 1 Megabit density, as well as synchronous FSRAMs with access times as fast as 6 ns and 8.5 ns.

Motorola's Fast Static RAM Division goal is simple: speed. All of our SRAMs are designed to provide the highest performance, cost efficient solutions available.

The Dynamic Memory Products Division utilizes alliances as a vehicle for global customer support in the DRAM and memory module markets. The product portfolio consists of high–density DRAMs, standard and custom memory modules, and PCMCIA Flash cards.

Page

Fast Static RAMs

Introduction

Motorola is designing the fastest, most technologically advanced fast SRAMs. From 0.8 µm to 0.5 µm with access times as fast as 5 V 6 ns 256K, 6 ns 1M, 13ns 4M, and 8 ns 3.3 V 1M, these devices are progressively smaller, faster, and lower cost. These SRAMs are designed to provide the highest performance, cost efficient solutions available. Selected fast SRAMs are also available on 2M and 8M memory modules.

Application specific memories are designed for high–performance microprocessors that require more specialization from memory cache than is available from standard devices. Products include those for use with digital signal processors as well as a variety of popular microprocessors.

SYNCHRONOUS

APPLICATION SPECIFIC FAST STATIC RAMs (5 to 35 ns)

3.3 V Supply

Description	Organi–zation	Motorola Part Number	Pin Count	Packaging	Access Time (ns Max)	Tech–nology	Pro–duction	Comments
BurstRAMs™	32Kx32	MCM63P532	100	(TQ) TQFP	7/8/9	HCMOS	1Q96	Pipelined BurstRAM for PowerPC™ /Pentium™ MPUs.
	32Kx36	MCM69F536A	100	(TQ) TQFP	8.5/9/10/12	BiCMOS	Now	Flow–through BurstRAM for PowerPC/Pentium MPUs.
		MCM69P536A	100	(TQ) TQFP	5/6/7	BiCMOS	Now	Pipelined BurstRAM for PowerPC/Pentium MPUs.
	64Kx18	MCM69F618A	100	(TQ) TQFP	8.5/9/10/12	BiCMOS	Now	Flow–through BurstRAM for PowerPC/Pentium MPUs.
		MCM69P618A	100	(TQ) TQFP	5/6/7	BiCMOS	Now	Pipelined BurstRAM for PowerPC/Pentium MPUs.
Tag RAM	64Kx18	MCM69T618	119	(ZP) PBGA	5/6/7	BiCMOS	2Q96	100 MHz Cache Tag RAM.

5 V Supply

Description	Organi–zation	Motorola Part Number	Pin Count	Packaging	Access Time (ns Max)	Tech–nology	Pro–duction	Comments
Integrated Cache Solutions	32Kx36	MPC2604GA	357	(ZP) PBGA	66 MHz	BiCMOS	1Q96	Integrated L2 cache for PowerPC processors.Two components for 256KB solution, and four for 512KB.
BurstRAMs	64Kx18	MCM67B618A	52	(FN) PLCC	9/10/12	BiCMOS	Now	BurstRAM (flow–through) for 486/Pentium. 3.3 V output levels.
		MCM67C618A	52	(FN) PLCC	5/7	BiCMOS	Now	BurstRAM (pipelined) for 486/Pentium. 3.3 V output levels.
		MCM67H618A	52	(FN) PLCC	9/10/12	BiCMOS	Now	Supports Pentium pipelined address mode.
		MCM67J618A	52	(FN) PLCC	5/7	BiCMOS	Now	Supports Pentium pipelined address mode.
		MCM67M618A	52	(FN) PLCC	9/10/12	BiCMOS	Now	BurstRAM (flow–through) for PowerPC. 3.3 V output levels.
	32Kx18	MCM67B518	52	(FN) PLCC	9/10/12	BiCMOS	Now	BurstRAM (flow–through) for 486/Pentium. 3.3 V output levels. Not recommended for new designs.
		MCM67C518	52	(FN) PLCC	6/7/9	BiCMOS	Now	BurstRAM (pipelined) for 486/Pentium. 3.3 V output levels. Not recommended for new designs.
		MCM67H518	52	(FN) PLCC	9/10/12	BiCMOS	Now	Supports Pentium pipelined address mode. Not recommended for new designs.
		MCM67J518	52	(FN) PLCC	6/7/9	BiCMOS	Now	Supports Pentium pipelined address mode. Not recommended for new designs.
		MCM67M518	52	(FN) PLCC	9/11/14	BiCMOS	Now	BurstRAM (flow–through) for PowerPC. 3.3 V output levels. Not recommended for new designs.
DSPRAM™	8Kx24	MCM56824A	52	(FN) PLCC	20/25/35	HCMOS	Now	Designed for DSP56001 applications, replaces 3 8Kx8's.
General Synchronous	128Kx9	MCM67Q709	86	(ZP) PBGA	5/6	BiCMOS	Now	General synchronous separate I/O with write pass through. 3.3 V output levels.
	256Kx4	MCM67Q804	36	400 (WJ) SOJ	5/6	BiCMOS	Now	Graphics; general RISC. Register to register. Revolutionary pinout. 3.3 V output levels. Write pass through. Separate I/O.
	16Kx16	MCM62990A	52	(FN) PLCC	12/15/20/25	HCMOS	Now	Designed for advanced RISC–CSIC cache applications
		MPC27T416	80	(TQ) TQFP	9/10/12	BiCMOS	2Q96	14 tag bits, 2 status bits. Sampling 2Q96.
	8Kx8	MCM62X308	28	300 (J) SOJ	15/17	HCMOS	Now	Line buffer for processing digital data.
	4Kx12	MCM62973A	44	(FN) PLCC	18/20	HCMOS	Now	Pipelined SRAM with chip select.
		MCM62974A	44	(FN) PLCC	18/20	HCMOS	Now	Pipelined SRAM with output enable.
		MCM62975A	44	(FN) PLCC	25/30	HCMOS	Now	Output enable.

ASYNCHRONOUS

6 to 15 ns FAST STATIC RAMS

3.3 V Supply

Density	Organi–zation	Motorola Part Number	Pin Count	Packaging Package width in mils	Access Time (ns Max)	Tech–nology	Pro–duction	Comments
1M	128Kx8	MCM6926	32	400 (WJ) SOJ	8/10/12/15	BiCMOS	1Q96	Revolutionary pinout.
	256Kx4	MCM6929	32	400 (WJ) SOJ	8/10/12/15	BiCMOS	1Q96	Revolutionary pinout.

5 V Supply

Density	Organi–zation	Motorola Part Number	Pin Count	Packaging Package width in mils	Access Time (ns Max)	Tech–nology	Pro–duction	Comments
1M	64Kx18	MCM67A618A	52	(FN) PLCC	10/12/15	BiCMOS	Now	General asynchronous, latched address and data.
	128Kx8	MCM6726B	32	400 (WJ) SOJ	8/10/12	BiCMOS	Now	Use for new quals and design. Revolutionary pinout.
		MCM6726C	32	400 (WJ) SOJ	6/7	BiCMOS	Now	Revolutionary pinout.
	256Kx4	MCM6729B	32	400 (WJ) SOJ	8/10/12	BiCMOS	Now	Use for new quals and design. With output enable. Revolutionary pinout.
		MCM6729C	32	400 (WJ) SOJ	6/7	BiCMOS	Now	Revolutionary pinout.
256K	32Kx8	MCM6706B	28	300 (J) SOJ	8/10	BiCMOS	Now	Not recommended for new designs. Potential substitute MCM6706BR.
		MCM6706BR	32	300 (J) SOJ	6/7/8	BiCMOS	Now	Revolutionary pinout.

12 to 35 ns FAST STATIC RAMS

3.3 V Supply

Density	Organi–zation	Motorola Part Number	Pin Count	Packaging Package width in mils	Access Time (ns Max)	Tech–nology	Pro–duction	Comments
1M	64Kx16	MCM6323	44	400 (J) SOJ	12/15	HCMOS	2Q96	Revolutionary pinout. Samples 1Q96.
	128Kx8	MCM6326	32	400 (J) SOJ	12/15	HCMOS	3Q96	Revolutionary pinout. Samples 2Q96.
256K	32Kx8	MCM6306D	28	300 (J) SOJ	15/20/25	HCMOS	Now	3.3 V Fast SRAM

5 V Supply

Density	Organi–zation	Motorola Part Number	Pin Count	Packaging Package width in mils	Access Time (ns Max)	Tech–nology	Pro–duction	Comments
4M	512Kx8	MCM6246	36	400 (WJ) SOJ	20/25/35	HCMOS	Now	Output enable. Revolutionary pinout.
	1Mx4	MCM6249	32	400 (WJ) SOJ	20/25/35	HCMOS	Now	Output enable. Revolutionary pinout.
1M	64Kx16	MCM6223	44	400 (J) SOJ	12/15	HCMOS	2Q96	Revolutionary pinout. Samples 1Q96. 3.3 V I/Os.
	128Kx8	MCM6226B	32	400 (WJ) SOJ	15/17/20/25	HCMOS	Now	Not for new designs. Suggest MCM6226BB.
		MCM6226BA	32	400 (WJ) SOJ	17/20/25	HCMOS	Now	Not for new designs. Suggest MCM6226BB.
		MCM6226BB	32	300 (J), 400 (WJ) SOJ	15/17/20/25	HCMOS	1Q96	Samples 4Q95.
		MCM6326	32	400 (J) SOJ	12/15	HCMOS	3Q96	Revolutionary pinout. Samples 2Q96. 3.3 V I/Os.
	256Kx4	MCM6229B	28	400 (WJ) SOJ	15/17/20/25	HCMOS	Now	Not for new designs. Suggest MCM6229BB.
		MCM6229BA	28	400 (WJ) SOJ	17/20/25	HCMOS	Now	Not for new designs. Suggest MCM6229BB.
		MCM6229BB	28	300 (J), 400 (WJ) SOJ	15/17/20/25	HCMOS	1Q96	Samples 4Q95.
	1Mx1	MCM6227B	28	300 (J), 400 (WJ) SOJ	15/17/20/25	HCMOS	Now	Separate I/O. Replaces 6227A.
256K	16Kx16	MCM62996	52	(FN) PLCC	12/15/20/25	HCMOS	Now	Choice of 5 V or 3.3 V power supplies for output buffers. For wide bus applications.
		MCM62995A	52	(FN) PLCC	12/15/20/25	HCMOS	Now	DSP96000 and RISC applications. Latched address inputs.
	32Kx8	MCM6206BA	28	300 (J) SOJ	12/15/20/25	HCMOS	Now	Replaces MCM6206D.
	32Kx9	MCM6205D	32	300 (J) SOJ	15/20/25	HCMOS	Now	

DEVICE/PART NUMBER DESIGNATORS

ASYNCHRONOUS DEVICE

MC M 67 0 6 B R J 8

Motorola Component
- MC = Qualified
- SC = Special

Memory

62 = 5 V CMOS
63 = 3.3 V CMOS
67 = 5 V BiCMOS
69 = 3.3 V BiCMOS

Density:
- 0 = 256K
- 2 = 1M
- 4 = 4M
- 6 = 16K
- 8 = 64K

Width:
- 5 = x 9
- 6 = x 8
- 7 = x 1
- 8 = x 4
- 9 = x 4 with OE

Die Revision*
- Blank = First qualified Motorola device
- A = First die size change/spec change
- B = Second die size change/spec change
- BA = First qualified foundry device

Revolutionary Pinout*

Package* (WJ = Wide SOJ, J = SOJ, FN = PLCC, TB = TAB)

Speed (ns)

NOTE: There are some exceptions to these device numbering schemes, i.e., MCM62990A is a CMOS 16K x 16 and NOT a 512K x 90 device. MPC designates devices designed to work with PowerPC microprocessors and support chips.

* These designators apply to current products – future products will not necessarily follow this scheme.

SYNCHRONOUS DEVICE

MC M 67 B 6 18 A FN 12

Motorola Component (Qualified)

Memory

62 = 5 V CMOS
63 = 3.3 V CMOS
67 = 5 V BiCMOS
69 = 3.3 V BiCMOS

- A = Async w/Address and Data Latch
- B = x86 Burst Count
- C = x86 Burst Count and Output Register
- D = Dual I/O
- F = Flow–Through BurstRAM
- H = x86 Burst Count with Address Disable
- J = x86 Burst Count with Address Disable and Output Register
- M = Motorola (PowerPC) Burst Count
- P = Pipelined BurstRAM
- Q = Sep. I/O
- T = Cache Tag
- X = Line Buffer

Depth:
- 3 = 8K Address Depth
- 4 = 16K Address Depth
- 5 = 32K Address Depth
- 6 = 64K Address Depth
- 7 = 128K Address Depth
- 8 = 256K Address Depth

Width:
- 04 = x 4
- 08 = x 8
- 09 = x 9
- 16 = x 16
- 18 = x 18
- 24 = x 24
- 32 = x 32
- 36 = x 36

Die Revision

Package (WJ = Wide SOJ, FN = PLCC, J = SOJ, ZP = PBGA, TQ = TQFP)

Speed (ns)

FAST STATIC RAM MODULES (Contact Fast Static RAM Marketing for Custom Fast SRAM Modules)

PowerPC Processor Applications

Description	Chip Set	Functionality	Cache Size	Access Time (Max)	Pro–duction	Packaging	Motorola Part Number
PowerPC™ Cache Modules	Motorola MPC105, Motorola MPC106	Flow–Through Burst	512KB Cache	66 MHz	1Q96	136 Pin DIMM (SG)	MPC2103
		Asynchronous	256KB Cache	15 ns	1Q96		MPC2101
PowerPC Cache Modules with 16K x 15 CacheTag	Motorola MPC105, Motorola MPC106	Flow–Through Burst	256KB Cache	66 MHz	TBD	182 Pin Card Edge (SG)	MPC2104
		Flow–Through Burst	512KB Cache	66 MHz	1Q96		MPC2105
		Flow–Through Burst	1MB	66 MHz	1Q96		MPC2106
		Asynchronous	256KB Cache	15 ns	TBD		MPC2107

Pentium and other x86 Processor Applications

Description	Chip Set	Functionality	Cache Size	Access Time (Max)	Pro–duction	Packaging	Motorola Part Number
Pentium™ L2 Cache Modules	Intel 82430 FX Triton chip set	Piped Burst	512KB Cache	66 MHz	Now	160 Pin Card Edge (SG)	MCM72JG64
			256KB Cache	66 MHz	Now		MCM64PA32
		Asynchronous	256KB Cache	15 ns	Now	160 Pin Card Edge (SG)	MCM64AF32
	Intel 82430 PCI chip set	Flow–Through Burst	512KB Cache	60/66 MHz	Now	136 Pin DIMM Form Factor. (SG)	MCM72BA64
			256KB Cache	60/66 MHz	Now		MCM72BA32
		Flow–Through Burst	512KB Cache	60/66 MHz	Now	160 Pin Card Edge (SG)	MCM72BF64
	VLSI 82C590	Asynchronous	256KB Cache	15 ns	Now	160 Pin Card Edge (SG)	MCM64AG32
	Corollary, Ross Computer	Piped Burst	512KB Cache	66 MHz	Now	160 Pin Card Edge (SG)	MCM72CB64

RISC Processor Applications

Description	Cache Size	Access Time (Max)	Production	Packaging	Comments	Motorola Part Number
R4000 Secondary Cache Modules	4MB	12/15/17 ns	Now	80 Pin SIMM (SG)	4MB cache using 4 modules, all Tag options available.	MCM44256 Series
	1MB	12/15/17 ns	Now	80 Pin SIMM (SG)	1MB cache using 4 modules, all Tag options available.	MCM4464 Series

Networking and Buffer Applications

Description	Organization	Access Time (Max)	Production	Packaging	Comments	Motorola Part Number
Standard FSRAM Modules	1M x 32	20/25 ns	Now	72 Pin SIMM (SG)	Uses eight 4M SRAMs	MCM321024
	512K x 32	20/25 ns	Now	72 Pin SIMM (SG)	Uses four 4M SRAMs	MCM32515

Dynamic RAMs

Introduction

DRAMs offer the lowest cost per bit of any memory. Because of this, they are popular for a wide range of applications, particularly in the computing environment. Motorola's Dynamic Memory Products include DRAM components, memory modules, and PCMCIA Flash cards. The 4 and 16 MByte DRAM components are offered in various organizations and surface mount packaging. Motorola's DRAM Memory Modules include densities up to 64 MByte in both standard and custom configurations.

All devices are fabricated using HCMOS technology and operate in a 5–volt power supply. However, specific DRAM products are designed for use in either a 3.3 Volt or 5–Volt power supply.
The 68–pin Flash ATA card is fully PCMCIA compatible. It is available in capacities from 1.8 MBytes to 40 MBytes and capacities can be doubled using data compression software.

DRAM MODULES (Contact DRAM Marketing for Custom DRAM Modules)

Organi–zation	Byte Density	Motorola Part Number	Pin Count	Packaging	Access Time (ns Max)	Operating Current (mA Max)	Pro–duction	Comments
1Mx8	1MB	MCM81430	30	(S)	60/70	240/200	Now	30–pad SIMM package; 2–chip version
4Mx8	4MB	MCM84000	30	(AS)	60/70	960/800	Now	30–pad SIMM package
		MCM84430	30	(S)	50/60/70	260/220/190	Now	30–pad SIMM package; 2–chip version
		MCM84T430	30	(S)	50/60/70	260/220/190	Now	30–pad SIMM package; 2–chip TSOP version
1Mx9	1MB	MCM91430	30	(S), (SC)	60/70	330/280	Now	30–pad SIMM package for parity application; 3–chip version PHASE OUT
4Mx9	4MB	MCM94000	30	(AS), (SC)	60/70	1080/900	Now	30–pad SIMM package for parity application
		MCM94430	30	(S)	60/70	340/290	Now	30–pad SIMM package; 3–chip version
		MCM94T430	30	(S)	60/70	340/290	Now	30–pad SIMM package; 3–chip TSOP version
1Mx18	2MB	MCM18100	72	(AS), (ASG)	60/70	240/220	Now	72–pad SIMM package for 16 bit parity application PHASE OUT
2Mx18	4MB	MCM18200	72	(S), (SG)	60/70	672/572	Now	72–pad SIMM package for 16 bit parity application PHASE OUT
4Mx18	8MB	MCM18400	72	(AS), (ASG)	60/70	680/580	Now	72–pad SIMM package for 16 bit parity application
8Mx18	16MB	MCM18800	72	(AS), (ASG)	60/70	692/592	Now	72–pad SIMM package for 16 bit parity application
1M x 32	4MB	MCM32100	72	(DG)	60/70	960/800	Now	Small outline DIMM package, 5 V – TSOP
		MCM32103	72	(DG)	80	480	Now	Small outline DIMM package, 3.3 V – TSOP
		MCM32L103	72	(DG)	80	480	Now	Small outline DIMM package, 3.3 V Low power TSOP
		MCM32116	72	(S), (SG)	60/70	370/310	Now	72–pad SIMM package; Uses 1M x 16 SOJ DRAM
		MCM32T116	72	(SH)	60/70	370/310	Now	72–pad SIMM package; Uses 1M x 16 TSOP DRAM
		MCM32130	72	(SH), (SHG), (SSH)	60/70	960/800	Now	72–pad SIMM package; SOJ version
		MCM32T100	72	(S), (SG)	60/70	960/800	Now	72–pad SIMM package; TSOP version
2Mx32	8MB	MCM32216	72	(S), (SG)	60/70	374/314	Now	72–pad SIMM package; Uses 1M x 16 SOJ DRAM
		MCM32T216	72	(SH)	60/70	374/314	Now	72–pad SIMM package; Uses 1M x 16 TSOP DRAM
		MCM32230	72	(SH), (SHG)	60/70	976/816	Now	72–pad SIMM package; SOJ version
		MCM32T200	72	(S), (SG)	60/70	976/816	Now	72–pad SIMM package; TSOP version
4Mx32	16MB	MCM32400	72	(ASH), (ASHG)	50/60/70	1040/880/760	Now	72–pad SIMM package; SOJ version
4Mx32	16MB	MCM32410	72	(S), (SG)	60/70	3840/3200	Now	Double–sided module using 4M DRAM PHASE OUT
4Mx32	16MB	MCM32420	72	(ADG)	50/60/70	1040/880/760	Now	MCM32400 small outline package, 5.0 V – TSOP
		MCM32423	72	(ADG)	60/70	880/760	Now	MCM32400 small outline package, 3.3 V – TSOP
8Mx32	32MB	MCM32800	72	(ASH), (ASHG)	50/60/70	1056/896/776	Now	72–pad SIMM package; SOJ version
		MCM32T800	72	(ASH), (ASHG)	50/60/70	1056/896/776	Now	72–pad SIMM package; TSOP version
1Mx36	4MB	MCM36100	72	(AS), (ASG), (ASH), (ASHG)	60/70	1320/1120	Now	72–pad SIMM package for parity application PHASE OUT
1Mx36	4MB	MCM36104	72	(S), (SG)	60/70	1080/900	Now	72–pad SIMM package for ECC, and parity application; SOJ version
2Mx36	8MB	MCM36200	72	(AS), (ASG)	60/70	1344/1144	Now	72–pad SIMM package for parity application PHASE OUT
2Mx36	8MB	MCM36204	72	(S), (SG)	60/70	1098/918	Now	72–pad SIMM package for ECC pinout parity application; SOJ version
4Mx36	16MB	MCM36400	72	(AS), (ASG), (ASH), (ASHG)	60/70	1360/1160	Now	72–pad SIMM package for parity application; SOJ version
		MCM36404	72	(ASH), (ASHG)	50/60/70	1170/990/855	Now	ECC pinouts, for parity application; SOJ version
8Mx36	32MB	MCM36800	72	(AS), (ASG)	60/70	1384/1184	Now	72–pad SIMM package for parity application; SOJ version
		MCM36804	72	(ASH), (ASHG)	50/60/70	1188/1008/873	Now	ECC pinouts, for parity application; SOJ version
1Mx40	4MB for EDC	MCM40100	72	(AS), (ASG)	60/70	1200/1000	Now	72–pad SIMM package for ECC application; SOJ version
2Mx40	8MB for EDC	MCM40200	72	(AS), (ASG)	60/70	1220/1020	Now	72–pad SIMM package for ECC application; SOJ version
4Mx40	16MB for EDC	MCM40400	72	(SH), (SHG)	50/60/70	1300/1100/900	Now	Replaces MCM40420; SOJ version
	16MB for EDC	MCM40420	72	(S), (SG)	60/70	1200/1000	Now	72–pad SIMM for ECC application PHASE OUT
8Mx40	32MB for EDC	MCM40800	72	(SH), (SHG)	50/60/70	1320/1120/970	Now	72–pad SIMM for ECC application; SOJ version
1Mx64	8MB	MCM64100	168	(DG)	60/70	2050/1715	Now	168–pad DIMM package; SOJ version
		MCM64T100	168	(ADG)	60/70	828/700	Now	168–pad DIMM package; Using 16M DRAM

Organi–zation	Byte Density	Motorola Part Number	Pin Count	Packaging	Access Time (ns Max)	Operating Current (mA Max)	Pro–duction	Comments
		MCM64T116	168	(DG)	60/70	828/700	4Q95	168–pad DIMM package; Uses 1M x 16 TSOP DRAM
2Mx64	16MB	MCM64T216	168	(DG)	60/70	TBD	4Q95	168–pad DIMM package; Uses 1M x 16 TSOP DRAM
4Mx64	32M	MCM64400	168	(DG)	60/70	2050/1715	1H96	168–pad DIMM package

NOTE: Package suffixes are enclosed by ( ) in packaging column

AD/ADG = DIMM/Gold Pad DIMM (Board Rev.)
AS = SIMM (Board Revision)
ASG = Gold Pad SIMM (Board Revision)
ASH = Low Profile SIMM
ASHG = Low Profile Gold Pad SIMM
D/DG = Dual Inline Module/Dual Inline Gold Pad Module
S = SIMM
SC = Industrial Temperature SIMM
SG = Gold Pad SIMM
SH = Short Height SIMM
SSH = Super Short Height SIMM
SHG = Short Height Gold Pad SIMM

DYNAMIC RAMs (HCMOS) (Contact DRAM Marketing)

Density	Organi–zation	Motorola Part Number	Pin Count	Packaging Package width in mils	Access Time (ns Max)	Operating Current (mA Max)	Pro–duction	Comments
1M	1Mx1	MCM511000A	18, 20, 20/26	300 (P)DIP, 100 (Z)IP	70/80	80/70	Now	No new customers. No orders after June 93
		MCM51L1000A	18, 20, 20/26	300 SO(J)	70/80	80/70	Now	No new customers. Orders limited after Sept 93
	256Kx4	MCM514256A	18, 20, 20/26	300 (P)DIP, 100 (Z)IP	70/80	80/70	Now	No new customers. No orders after June 93
		MCM51L4256A	18, 20, 20/26	300 SO(J)	70/80	80/70	Now	No new customers. Orders limited after Sept 93
4M	4Mx1	MCM44100B	20/26	300 SO(N)	60/70	110/100	Now	Fast page mode cycle time = 40/45 ns
		MCM4L4100B	20/26	300 SO(N)	60/70	110/100	Now	Low power
4M	4Mx1	MCM44100C	20/26	300 SO(N)	60/70	110/100	1Q96	Fast page mode cycle time = 40/45 ns
		MCM4L4100C	20/26	300 SO(N)	60/70	110/100	1Q96	Low power
		MCM54100A	20/26	300 SO(N), 300 (T)SOP	60/70	120/100	Now	Fast page mode cycle time = 45/45 ns
		MCM5L4100A	20/26	300 SO(N), 300 (T)SOP	60/70	120/100	Now	Low power
		MCM54100A–C	20/26	300 SOJ(N), 300 (T)SOP	70/80	100/85	Now	3.3 V Fast page mode cycle time = 45/50 ns
		MCM54100A–V	20/26	300 SOJ(N), 300 (T)SOP	70/80	70/60	Now	3.3 V Fast page mode cycle time = 45/50 ns
		MCM5L4100A–V	20/26	300 SOJ(N), 300 (T)SOP	70/80	70/60	Now	Low power, 3.3 V
	1Mx4	MCM44400B	20/26	300 SO(N)	60/70	110/100	Now	Fast page mode cycle time = 40/45 ns
		MCM4L4400B	20/26	300 SO(N)	60/70	110/100	Now	Low power
		MCM54400A	20/26	300 SOJ(N), 300 (T)SOP	60/70	120/100	Now	Fast page mode cycle time = 45/45 ns
		MCM5L4400A	20/26	300 SOJ(N), 300 (T)SOP	60/70	120/100	Now	Low power
		MCM54400A–C	20/26	300 SO(N)	70/80	100/85	Now	Industrial temp range (– 40 to + 85°C)
		MCM5L4400A–C	20/26	300 SOJ(N), 300 (T)SOP	70	100	Now	Low power, industrial temp range (–40 to + 85°C)
		MCM54400A–V	20/26	300 SOJ(N), 300 (T)SOP	70/80	70/60	Now	3.3 V Fast page mode cycle time = 45/50 ns
		MCM5L4400A–V	20/26	300 SOJ(N), 300 (T)SOP	70/80	70/60	Now	Low power, 3.3 V
4M	512Kx8	MCM54800A	28	400 SO(J), 400 (T)SOP	70/80	105/90	Now	Fast page mode cycle time = 45/50/60 ns
		MCM5L4800A	28	400 SO(J), 400 (T)SOP	70/80	105/90	Now	Low power
		MCM5V4800A	28	400 SO(J), 400 (T)SOP	70/80	105/90	Now	Low power, self refresh
	256Kx16	MCM54260B	40, 40/44	400 SO(J), 400 (T)SOP	70/80	100/85	Now	Fast page mode, 2 CAS, 1 W, 512 refresh
		MCM5L4260B	40, 40/44	400 SO(J), 400 (T)SOP	70/80	100/85	Now	Low power
		MCM5S4260B	40, 40/44	400 SO(J), 400 (T)SOP	70/80	100/85	Now	Low power, self refresh
		MCM54260D	40, 40/44	400 SO(J), 400 (T)SOP	50/60	135	2Q96	Fast page mode, 2 CAS, 1 W, 512 refresh
		MCM54265D	40, 40/44	400 SO(J), 400 (T)SOP	50/60	120	2Q96	Extended Data Out, 2 CAS, 1W, 512refresh
16M	4Mx4	MCM417400	24/26	300 SO(J)	60/70	110/100	Now	2K refresh, 11 row, 11 column
		MCM516400B	24/26	300 SO(J), 300 (T)SOP	50/60/70	100/80/70	Now	4K refresh, 12 row, 10 column
		MCM517400B	24/26	300 SO(J), 300 (T)SOP	50/60/70	130/110/95	Now	2K refresh, 11 row, 11 column
		MCM517400C	24/26	300 SO(J), 300 (T)SOP	60/70	110/95	3Q96	2K refresh, FPM, 11 row, 11 column
		MCM517400CV	24/26	300 SO(J), 300 (T)SOP	60/70	75/65	3Q96	3.3 version of MCM517400C
		MCM517405C	24/26	300 SO(J), 300 (T)SOP	60/70	110/95	3Q96	2K refresh, EDO, 11 row, 11 column
		MCM517405CV	24/26	300 SO(J), 300 (T)SOP	60/70	75/65	3Q96	3.3 version of MCM517405C
16M	1Mx16	MCM518160A	42	400 SO(J)	60/70	185/155	Now	1K refresh, 10 row, 10 column
		MCM518160A	44/50	400 (T)SOP	60/70	185/155	Now	1K refresh, 10 row, 10 column
16M	1Mx16	MCM518160B	42	400 (J)SOJ	60/70	180/150	2Q96	1K refresh, FPM, 10 row, 10 column
		MCM518160B	44/50	400 (T)SOP	60/70	180/150	2Q96	1K refresh, FPM, 10 row, 10 column
		MCM518165B	44/50	400 (T)SOP	60/70	180/150	2Q96	1K refresh, EDO, 10 row, 10 column
		MCM518165BV	42	400 (J)SOJ	70/80	145/120	3Q96	3.3 V version of MCM518165B
		MCM518165BV	44/50	400 (T)SOP	70/80	145/120	3Q96	3.3 V version of MCM518165B

Logic: Standard, Special and Programmable

In Brief . . .

This selector guide is a quick reference to Motorola's vast offering of standard logic integrated circuits. In TTL, popular due to its ease of use, low cost, medium–to–high speed operation and good output drive capability, Motorola offers both LS and FAST. Motorola's CMOS portfolio includes MC14000B standard CMOS series devices, High–Speed CMOS consisting of a full line of products that are pinout–compatible with many LSTTL and MC14000B standard CMOS logic devices which offers designers a solution to the long–standing combined barrier — high speed and low power. Motorola's Emitter Coupled Logic (MECL) is a non–saturated form of digital logic which eliminates transistor storage time permitting very high speed operation. Motorola offers five versions of MECL: MECL 10K, MECL 10H, MECL III, and the recently introduced families ECLinPS (ECL in picoseconds) and ECLinPS Lite. Also included are timing solution products such as clock drivers, clock generators and programmable delay chips, high performance and communications products such as VCO's, prescalers, and synthesizers, and a wide variety of translators, low–voltage bus interface and serial data transmission devices. Field programmable logic and in particular, field programmable arrays, have become the solution of choice for logic design implementation in applications where time to market is a critical product development factor. In addition, reconfigurable arrays have been used to enhance Customer product flexibility in ways that no other technology can match.

The Logic I.C. Division publishes a New Product Calendar quarterly that reflects any recent device releases and the approximate dates new devices are expected to be released. This New Product Calendar, BR1332/D, can be ordered from your nearest Motorola Sales Office or from the Motorola Literature Distribution Center.

Motorola Logic Families, Which Is Best for You?

By Gary Tharalson, Motorola, Chandler, AZ

Introduction

When a logic designer is faced with developing a new product requiring performance significantly different from the past, it might be well to examine various logic family alternatives. Selecting a logic family for a new design from today's rapidly changing semiconductor technologies can be a perilous task. With the many choices available, it is easy to under–kill or over–kill an application with inadequate or excessive capabilities.

By selecting the family whose parameters most closely fit your needs, you can save many future headaches. Obviously, before selecting a specific device, a detailed review of the vendor's data sheet specifications is recommended.

Family Comparison

Table 24. compares some typical characteristics of several popular logic families available in the market today. The following sections provide brief explanations of the various parameters.

Table 24. Logic Family Comparison

Typical Commercial Parameters (0° to +70°C)	Logic Families												
	TTL/ABT				CMOS					ECL			
	LS	ALS	ABT	FAST	MG	HC	FACT	LVC	LCX	10KH	100K	ECLinPS[3]	E–Lite
Speed													
OR Gate Prop Delay (t_{PLH}) ns	9	7	2.7	3	25	8	5	3.3	3.5	1	0.75	0.33	0.22
D Flip–Flop Toggle Rate MHz	33	45	200	125	4	45	160	200	200	330	400	1000	2800
Output Edge Rate ns	6	3	3	2	100	4	2	3.7	3.6	1	0.70	0.50	0.25
Power Consumption (Per Gate)													
Quiescent mW	5	1.2	0.005	12.5	0.0006	0.003	0.003	0.0001	1E–04	25	50	25	73
Operating (1MHz) mW	5	1.2	1.0	12.5	0.04	0.6	0.8	0.6	0.3	25	50	25	73
Supply Voltage V	+4.5 to 5.5	+4.5 to 5.5	+4.5 to 5.5	+4.5 to 5.5	+3 to 18	+2 to 6	+2 to 6	+1.2 to3.6	+2 to 3.6	–4.5 to –5.5	–4.2 to –4.8	–4.2 to –5.5	–4.5 to –5.5
Output Drive mA	8	8	32/64	20	1	4	24	24	24	50Ω Load	50Ω Load	50Ω Load	50Ω Load
5V Tolerant													
Inputs	N/A	N/A	N/A	N/A	N/A	N/A	N/A	YES	YES	N/A	N/A	N/A	N/A
Outputs	N/A	N/A	N/A	N/A	N/A	N/A	N/A	NO	YES	N/A	N/A	N/A	N/A
DC Noise Margin[1]													
High Input %	22	22	22	22	30	30	30	30	30	28	41	28/41	33
Low Input %	10	10	10	10	30	30	30	30	30	31	31	31/31	33
Packaging[4]													
DIP	YES	YES	YES	YES	YES	YES	YES	NO	NO	YES	YES	NO	NO
SO	YES	YES	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO	YES
LCC	NO	YES	NO	YES	NO	NO	YES	NO	NO	YES	NO	YES	NO
SSOP	NO	YES	YES	YES	NO	YES	YES	YES	YES	NO	NO	NO	NO
TSSOP	NO	NO	NO	NO	YES	YES	YES	YES	YES	NO	NO	NO	NO
Functional Device Types	190	210	50	110	125	103	80	35	27[2]	64	44	48	40
Relative 1–25 Price/Gate	0.9	1	1.6	1	0.9	0.9	1.4	1.8	1.8	2	10	25	32

NOTES:
1. Typical noise margin expressed as a percentage of typical output voltage swing.
2. Announced plans for Motorola offering.
3. ECLinPS is Available in both 10KH and 100K compatible versions.
4. A "YES" may not include all devices within a family.

VENDORS REFERENCED (DATA BOOK):

LS	Motorola Low power Schottky TTL (DL121)
ALS	Texas Instruments Advanced Low power Schottky TTL (SDAD001B)
ABT	Philips Semiconductor (IC23)
FAST	Motorola Advanced Schottky TTL (DL121)
MG	Motorola 14000 Series Metal Gate CMOS (DL131)
HC	Motorola High–Speed Silicon Gate CMOS (DL129)
FACT	Motorola Advanced CMOS (DL138)
LCX	Motorola Low–Voltage CMOS (BR1339)
LVC	Philips Low–Voltage CMOS (IC24)
10KH	Motorola 10KH Series ECL (DL122)
100K	National 100K Series ECL (F100K)
ECLinPS	Motorola Advanced ECL (DL140)
E–Lite	Motorola (ECLinPS Lite) Advanced ECL (DL140)

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Logic Families

Although there are many family technologies available, they can be divided into roughly three broad categories: Transistor–Transistor Logic (TTL), Complementary Metal–Oxide Semiconductor logic (CMOS), and Emitter–Coupled Logic (ECL). TTL and ECL are bipolar technologies differing in implementation techniques, while CMOS (an MOS technology) differs in fundamental transistor structure and operation.

TTL

The designation "bipolar" essentially refers to the basic component utilized to build this family of integrated circuits, the bipolar transistor. By employing a bipolar transistor in a logic function's output driver as well as the input buffer, it results in a Transistor–to–Transistor (TTL) direct connection. Older technologies were interconnected via passive components such as resistors or diodes.

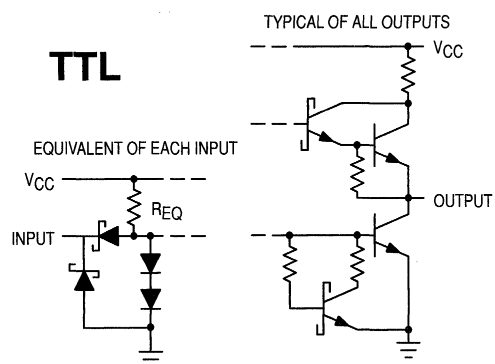
Since the original TTL design, several enhancements have been employed to reduce power and increase speed. Common to these has been the use of Schottky diodes which, ironically, no longer result in strictly TTL connections. Consequently, the two names, Schottky and TTL, are used in combination: LS (Low power Schottky), ALS (Advanced Low power Schottky), and FAST™ (Advanced Schottky) TTL.

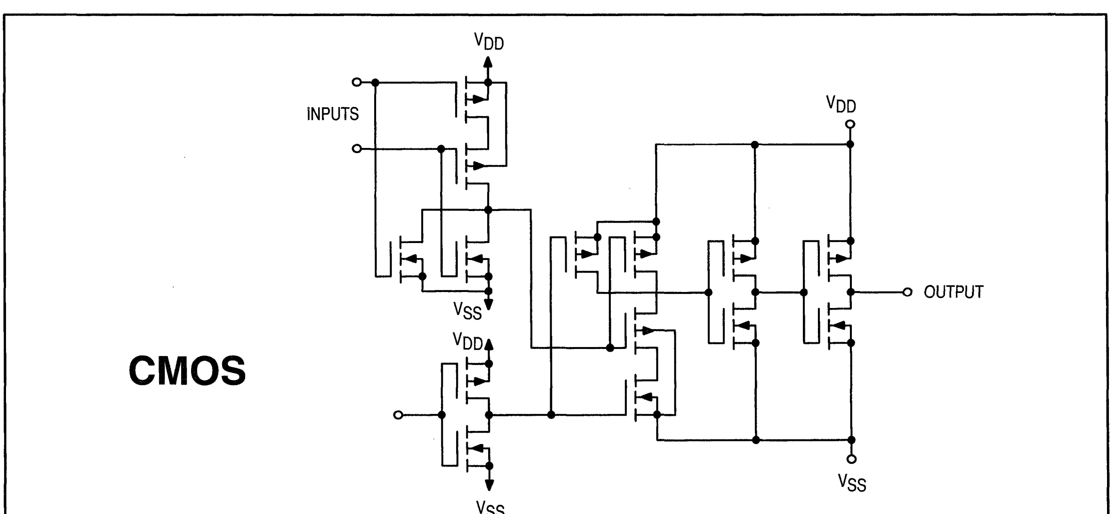
The superior characteristics of TTL compared to CMOS, in the past, have been its relatively high speed and high output drive; these advantages are rapidly diminishing as described in the next section. One family of devices, ABT (Advanced BiCMOS Technology), utilizes TTL circuitry at the inputs and outputs, and CMOS technology in between—attempting to combine the advantages of both bipolar and CMOS.

CMOS

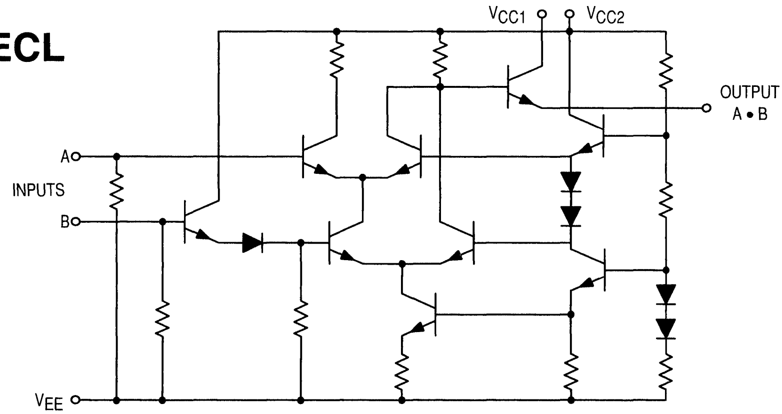
Complementary Metal–Oxide Semiconductor (CMOS) field–effect transistors differ from bipolar both in structure and operation. The primary advantages of CMOS are its low power dissipation and small physical geometry. Advances in design and fabrication have brought CMOS devices into the same speed and output drive capability as TTL. Again, enhancements have resulted in the evolvement of additional classifications: MG (Metal–Gate CMOS), HC (High–speed silicon–gate CMOS), and FACT™ (Advanced CMOS).

The most recent evolution in CMOS logic has been in reducing supply voltage without sacrificing performance. The new LCX family is one outgrowth of this trend. This family results from the joint efforts of a triumvirate of companies including Motorola, National, and Toshiba. Although each company has done its own design and fabrication, they have mutually agreed to provide identical performance specifications. In addition to the 3V operating voltage, LCX inputs and outputs are tolerant of interfacing with 5V devices.





ECL



ECL

Emitter–coupled logic (ECL) derives its name from the differential–amplifier configuration in which one side of the diff–amp consists of multiple–input bipolar transistors with their emitters tied together. An input bias on the opposite side of the diff–amp causes the amplifier to operate continuously in the active mode. Consequently, ECL consumes a relatively substantial amount of power in both states (one or zero) but also results in the fastest switching speeds of all logic families. An inherent benefit of ECL is the narrow switching level swing between devices (approximately 800 mV) which helps to reduce noise generation.

There have also been many evolutionary advancements in ECL, the following being some of the most prominent: 100K (1975), 10KH (1981), and ECLinPS™ (1987). Of most recent vintage is the ECLinPS Lite™ family of single function devices. By focusing on simplicity, this family achieves very high performance, while at the same time reducing package size.

Speed

Speed is typically the first parameter at which a designer looks, and when design engineers are asked what features of a logic family they would like enhanced, usually they want more speed. But increased speed often brings along many potential problems such as: increased noise generation, higher power consumption, increased component and system cost, more difficult board layout, etc. An assessment of the other family parameters is usually required before a final selection is possible.

In Table 24. , family speed is compared for three parameters using typical values: propagation delay through a simple OR gate, flip–flop toggle frequency, and output switching time. Typical values can be misleading as they are frequently specified according to different vendor's criteria, but they are usually close to an average of min and max values. For final assessment of a particular component's performance, the min/max spec's provided in most vendor's data sheets should be examined. Furthermore, switching (edge) rate is highly load dependent, and again, data sheet specifics must be compared.

Power Consumption

The amount of power an application consumes (and the subsequent heat generated) is frequently of prime importance. One of the major differences between the three families, the power parameter may also limit the designer's choices.

TTL consumes a moderate amount of power and is nearly constant over operating frequencies up to about 10 MHz; above 10 MHz it begins to climb rapidly. Although only a few milliwatts are consumed by each device, in a complete system a substantial amount of power may be used.

CMOS power consumption, on the other hand, is highly frequency dependent. In quiescent mode (zero frequency), it consumes almost no power at all, being measured in microwatts/device. However, its consumption grows almost linearly with frequency so that at maximum operating frequency it may be several milliwatts/device. The great power reduction advantage of CMOS derives from the fact, that in most applications, the percentage of the total number of devices operating at high frequencies at any given time is small; consequently, the average total power consumed by the system is greatly diminished.

Since power consumption is proportional to the square of supply voltage, simply reducing the operating voltage will have desirable effects. Unfortunately, speed generally falls off as well. By designing the LCX family specifically for a lower supply voltage, it was possible to maintain high overall performance. The LCX family is also designed to interface with five volt devices, being tolerant of the differences in I/O levels.

Because of its inherent design, ECL is the highest power consumer at frequencies below approximately 50 MHz; however, at higher frequencies, TTL and CMOS power consumption can exceed ECL. The amount of power used by ECL is fairly constant over its entire operating frequency range. Designers of large, high performance ECL systems may have to employ somewhat more complex cooling and power distribution techniques.

Supply Voltage

The power supply voltage required for TTL and ECL is restricted to fixed values; only a narrow voltage variation is allowed for the device to remain within specifications. Since these families also consume substantial amounts of power, there is a large current flow through the power lines. To avoid unacceptable voltage fluctuation, various preventive measures may be necessary such as remote sensing by the supply regulator, beefing up power buses and filters, and utilizing multi–layer PC boards with separate power and ground planes. Typically, a high–speed energy storage capacitor is required near each logic device; this capacitor maintains the correct device voltage during high–current switching.

An important advantage of CMOS is the large range of supply voltage over which operation is specified. By allowing systems to be operated at voltages as low as 2V, not only is power consumption lowered, but noise generation from fast signal switching is reduced. It must be noted, however, that operating speed drops off rapidly as the voltage is reduced. As mentioned previously, this was a significant reason for developing the LCX family.

Output Drive

An important characteristic of a logic device is its ability to drive relatively large loads without significant speed degradation. The older families within TTL, and especially CMOS, had only limited drive capability (below 10 mA). All advanced logic family versions have significantly increased drive capacity, and several (FACT, LCX and all ECL) are capable of driving 50 ohm transmission lines directly. Furthermore, because of the symmetrical sink/source capability of FACT and LCX, their rise and fall times are nearly equal, resulting in balanced delay times.

5V Tolerant Input/Output

Because of the limited number of functions available in the new low voltage CMOS families, a designer might might have to mix 3V and 5V devices, each operating from 3V and 5V rails, respectively. Unless the 3V device was specifically designed with proper protection to tolerate 5V at its input or output, it may not survive.

Noise Margin

Noise immunity refers to the resistance of a logic device to undesired switching. Depending on the input level, a noise glitch that causes a transient across the input switch point from either a high or low level can result in erroneous operation. Clearly, the more voltage difference there is between the switch point and the normal input high and low levels, the more immunity a logic family has to erroneous switching. In Table 24. , these differences are expressed as a percentage of the swing between typical output high and low voltage logic levels. High input noise margin is calculated from the formula:

$$HNM = \frac{V_{OH} - V_{IH}}{V_{OH} - V_{OL}},$$ and for low input noise margin,

$$LNM = \frac{V_{IL} - V_{OL}}{V_{OH} - V_{OL}}.$$

Packaging

The venerable Dual–Inline package (DIP) is rapidly being replaced by Small Outline (SO), Shrink Small Outline (SSOP), Thin Shrink Small Outline (TSSOP), and Leadless Chip Carrier (LCC) packages for surface mounting. Savings in footprint area of up to 90% are possible with these newer packages.

Device Types

In general, the older the family the larger the quantity of different functional devices available. This is only natural since it takes time (and substantial resource investment) to design and reliably manufacture increasingly more complex devices. The newer TTL and CMOS families will undoubtedly grow, but because of competition from higher integrated devices, will be more limited in scope.

Cost

Here again, the age of a family has a substantial bearing on its relative selling price. The older families have benefited longer from manufacturing learning and volume curve cost reductions. Newer technologies, because of their inherently more complex process requirements, increased performance improvements, and higher cost of production, are priced higher but should decline over time.

Mix and Match

Many designers have found that the best approach to achieving their particular application performance goal is to combine devices from several families. The obvious advantage of this is to optimize the requirements of selected portions of a design, whether it is for speed, power consumption, output drive, cost, etc. Some disadvantages are that devices must be analyzed and tested for compatibility, inventories may increase, and some performance parameters may be compromised.

Conclusion

The diversity of logic families available to today's logic designer may be likened to a bad news/good news scenario. The bad news is that you have huge ratios between the highest and lowest performance values—speeds of 500:1, power at 100,000:1, output drive at 24:1, etc. The good news is that you have lots of choices—it wasn't too many years ago that there were very few. By examining and comparing each family's parameters, an optimal selection can result.

A few potential users of standard logic devices may worry, that because of the trends towards higher–integration chips, some vendors will abandon the older product lines. This may *eventually* happen; however, the current demand, projected for at least the next decade, indicates that these families have a very solid future. The diverse applications that keep arising for semiconductor products that are inexpensive and reliable continue to mount. Until some totally revolutionary development should occur, these "oldies, but goodies" will be around for a long time to come.

INTRODUCTION TO MOTOROLA PROGRAMMABLE ARRAYS

Field programmable logic and in particular, field programmable arrays, have become the solution of choice for logic design implementation in applications where time to market is a critical product development factor. In addition, reconfigurable arrays have been used to enhance Customer product flexibility in ways that no other technology can match.

Microprocessors have traditionally been used to satisfy time to market and end product flexibility needs. This solution may not meet performance constraints and lacks the concurrency possible in an unconstrained hardware design. Typical design processes, therefore, reach a point where the overall design is partitioned into hardware and software components. An interface is defined and the design process continues along two parallel paths. Sometime later, the software and hardware components must be integrated. Problems usually develop at this point because of interface misinterpretation or partitioning that cannot meet design requirements. This impacts the hardware, the software and the schedule. If the hardware design is realized in programmable logic, the hardware can be manipulated as easily as the software.

Products which adapt to the end users particular requirements through self directed or end user directed reconfiguration are becoming more prevalent. As the number of modes of operation increases, mode specific hardware becomes a less cost effective solution. In the case where the end user is truly directing the adaptation, predetermined hardware solutions become untenable. Reconfigurable logic enables design solutions where dynamic hardware–software repartitioning is possible.

Programmable logic not only vastly improves the time necessary to implement a static design, but significant time to market and product feature benefits can be realized when hardware can be dynamically altered as easily as software.

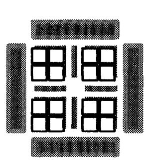
To reduce design cycles, designers have also turned towards high level design languages and logic synthesis tools. Many programmable logic solutions are poorly suited to this design methodology, however. An incompatibility exists between logic synthesis algorithms originally developed for gate level design and the block–like structures found on many programmable logic devices. This can result in significant under utilization or degraded performance. In either case a more expensive device is required. Real gate level programmable devices are ideally suited to this design methodology.

When schematic based design methods are used, some programmable logic solutions impose significant constraints on design implementation to insure satisfactory results. This imposition tends to bind the design to a particular programmable device and requires a significant learning investment. Any design specification changes which impact design decisions made to fit this imposed structure can have disastrous effects on utilization and performance and potentially require a more expensive device or even a costly redesign. Gate level programmable devices coupled with sophisticated, timing driven, implementation tools minimize device specific optimization.

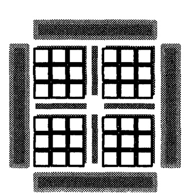
Any design process includes a significant amount of learning. Usually engineers spend most of this time learning about product requirements or prototyping critical portions of the design to prove implementation feasibility. Many programmable logic solutions are not push button; time must be spent learning programmable device architecture or implementation tool quirks. Worse yet, the design may require modification or manual component placement to meet design targets. The cost? Time to market.

The reconfigurable Motorola Programmable Array (MPA) and MPA design system maximize application flexibility and minimize time to market by delivering a gate level, push button, programmable logic solution.

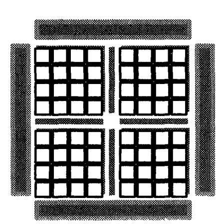
MPA1016



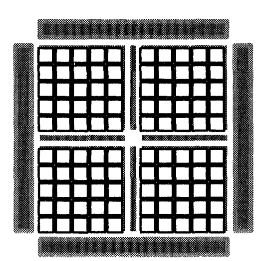
MPA1036



MPA1064



MPA1100



MPA1000 Programmable Arrays

MPA1016
MPA1036
MPA1064
MPA1100

PROGRAMMABLE ARRAY
3,500 to 22,000 GATES

Motorola Programmable Array (MPA) products are a high density, high performance, low cost, solution for your reconfigurable logic needs. When used with our automatic high performance design tools, MPA delivers custom logic solutions in minutes rather than weeks. And the low cost keeps those solutions competitive throughout the product lifecycle.

The MPA architecture has solved the historical problems associated with fine grain devices without sacrificing re–programmability, reliability, or cost. MPA1000 devices are reprogrammable SRAM based products manufactured on a standard 0.5µ Leff CMOS process with logic capacities from 3,500 to more than 22,000 equivalent FPGA gates. MPA Logic resources hold a single gate or storage element providing a highly efficient, adaptable, design implementation medium. Gate level logic resources, abundant hierarchical interconnection resources and automatic, timing driven, tools work together to quickly provide design implementations that meet timing constraints without sacrificing device utilization.

Staying focused on end product design rather than implementation tools or device architecture gets the design done faster and, unlike other programmable solutions, without programmable logic device specificity to impede future design migration efforts. The combination of automatic tools and gate level architecture is ideal for traditional schematic driven or high level language based design methodologies. In fact, logic synthesis tools were originally designed for and produce the most efficient results when targeting gate level devices.

High MPA1000 register count and controlled clock skew is ideal for designs employing pipelining techniques such as communications. The unique set of MPA1000 I/O programming options make these devices suitable for industrial and computer Interfacing circuits.

- Multiple I/O from 80–200 I/O Pins
- Programmable 3V/5V I/O at Any Site
- Multiple Packaging Options
- Fine Grain Structure Is Optimized for Logic Synthesis
- Programmable Output Drive, 6/12mA @ 5.0V
- High Register Count, with 560–2,900 Flip–Flops
- IEEE 1149.1 JTAG Boundary Scan
- Eight Low–Skew (<1ns) Clocks

MPA1000 Family Members

FPGA Gates	Part No.	Logic Cells	Internal Flip–Flops	I/O Cell Flip–Flops	Signal I/O Pads Max.	Packages	Availability
3500	MPA1016FN MPA1016DD	1600	400	160	80	84–Pin PLCC 128–Pin PQFP	April 1996 April 1996
8000	MPA1036FN MPA1036DD MPA1036DH MPA1036HI	3600	900	240	120	84–Pin PLCC 128–Pin PQFP 160–Pin PQFP 181–Pin PGA	NOW April 1996 NOW NOW
14200	MPA1064DH MPA1064DK MPA1064KE	6400	1600	320	160	160–Pin PQFP 208–Pin PQFP 224–Pin PGA	April 1996 2Q96 1Q96
22000	MPA1100DK MPA1100HV	10000	2500	400	200	208–Pin PQFP 299–Pin PGA	3Q96 3Q96

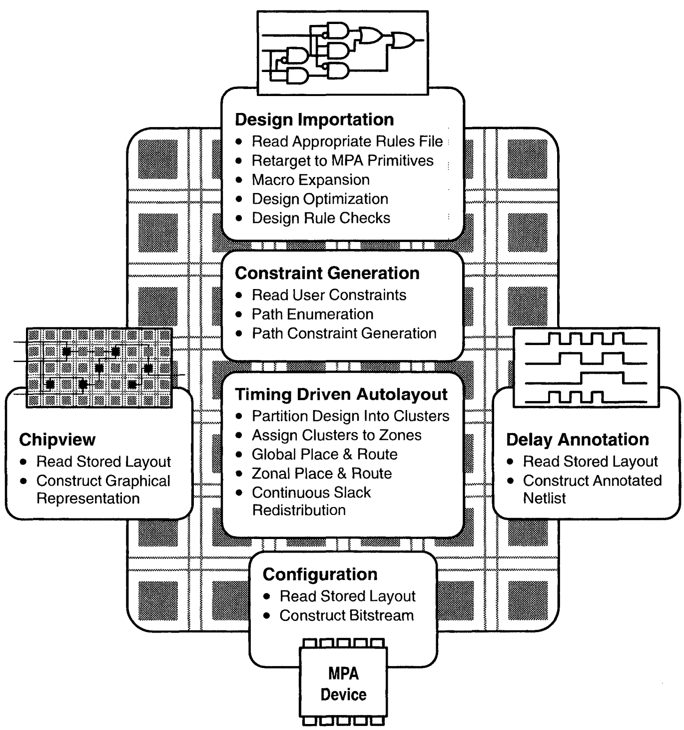
MPA1000 Design System Product Description

Overview

The Motorola Programmable Array (MPA) design system is a bridge between a design capture environment and Motorola field programmable arrays. The MPA design system automatically transforms designs into device configurations which, when loaded into an MPA device, realize a design. A design is automatically analyzed, optimized, transformed into MPA cells, partitioned, placed and routed based on timing constraints for every path in the design. MPA design tools understand and optimally utilize the MPA device architecture; this eliminates the need to learn a new set of rules and makes these tools ideally suited for use with logic synthesis. Full incremental design support reduces design implementation time and powerful library retargeting capabilities allow you to reuse designs which may have been implemented on less capable devices. The MPA design system operates on existing hardware platforms and supports design capture and simulation tools from more than 10 vendors. All these features plus on–line, hypermedia, help make the MPA design system a powerful yet extremely easy to use design implementation engine.

Features

- Push Button Implementation
- Optimal Use of MPA Device Resources
- Optimal Results with Gate Level Design Input
- Library of Common MSI Functions
- Design Flow Manager
- Design Retargeter
- Timing Driven with Integrated Static Timing Analysis
- Layout Delay extraction for post layout simulation
- Layout viewer
- Incremental design support
- On–line, hypermedia, documentation
- Supports all popular design capture and simulation tools
- Lowest cost FPGA development systems.
- Instant access; Downloading via the internet (WWW, ftp).



Push Button Design Implementation

The MPA design system minimizes training investment and automatically generates design implementations which meet timing constraints.

The gate level logic and abundant hierarchical routing resources of the MPA device present a rich implementation media for design implementation. MPA design tools understand and optimally utilize the MPA device resources so there are no elaborate rules to learn or design modifications required to begin design capture. Staying focused on end product design rather than implementation tools or device architecture gets the design done faster and, unlike other programmable solutions, without programmable logic device specificity to impede future design migration efforts. The combination of automatic tools and gate level architecture is ideal for traditional schematic driven or high level language based design capture methods. In fact, logic synthesis tools were originally designed for and produce the most efficient results for targeting gate level devices.

A design is analyzed, optimized, transformed into MPA cells, partitioned, placed and routed based on timing constraints for all paths in the design – automatically. A netlist from one of the popular design capture systems or an existing XNF or LPM netlist is imported into the MPA design system. The logic is mapped to a series of MPA cells and the entire resulting netlist is optimized and checked. Based on a simple clock specification, the MPA design system generates timing constraints for all paths in the design. During automatic partitioning, placement and routing path slack time is constantly redistributed insuring only the resources required to meet timing requirements are consumed. Because MPA tools implement the design according to constraints, tool induced design iterations are virtually eliminated. Completed layouts can be transformed into device configurations, as well as annotated simulation netlists. A layout browser is also available.

The MPA design system also includes complete on–line, hypermedia, help covers the device, the design system and the integration kits. Integration kits for Viewlogic, Exemplar, VHDL (1076), Verilog (OVI) and OrCAD are included (contact your vendor for additional kits).All these features add up to a powerful yet extremely easy to use design implementation engine for the MPA product family.

Design Importation

Designs can be captured using schematics, a high level language, or a combination of these entry methods using commercially available design capture and logic synthesis software and the appropriate interface kit. Alternatively, existing designs can be retargeted from other programmable logic devices to the MPA device using commercial logic synthesis tools or the powerful retargetting capabilities provided with MPA design system.

Design importation begins with a netlist and an optional clock specification file. The clock specification file provides a mechanism for the user or design capture tools to document system level timing requirements. In addition, a rich set of attributes can be attached to specific components or nets within the design to specify timing and design pinout constraints.

A retargetting rules file is read and the input netlist is transformed into a series of MPA cells and associated interconnections. Rules files provide a mechanism to perform attribute mapping, cell mapping and macro expansion. By creating custom rule files, the user can extend the importation process from arbitrary sources. The MPA design system comes with rules for it's native library/EDIF. The resulting netlist is optimized to clip unused logic and remove redundant logic. For example: each MPA cell has programmable input inversion capability. All Inverters or non–inverting buffers can be removed from the netlist and replaced with signal sense information attached to each input.

A series of design rule checks are performed to insure design integrity before the layout process begins.

Constraint Generation

Timing constraints, the optimized MPA netlist and static timing analysis is used to generate path slack constraints for all paths in the design. Each unique signal pathway between a register output and a register input throughout the design are enumerated. The total logic and estimated or real wire delays along the path are summed. The time between the active upstream register clock edge and the next active downstream clock edge minus the downstream register setup time is subtracted from the total path delay. This difference is called path slack. If any path in the design has a negative slack value, the implementation will not function at the required clock rate(s).

Path constraints are utilized throughout the layout process to insure that a design implementation which meets timing constraints is automatically generated. If no clock or timing specifications are provided, the MPA design system uses the fastest possible clock based on very small net delay estimates to generate the path constraints. This usually results in the best possible implementation, but may take longer than the time required to generate a satisfactory rather than best possible result.

Contrast this to other programmable logic design tools which only provide manual net constraint annotation or net criticality assignment. In these cases significant effort is necessary to generate constraints and many costly iterations are required to tune these constraints for a given design. If any changes are made to the design, another costly round of iterations is required.

Autolayout

The autolayout process makes use of the hierarchical organization of the MPA device to minimize run time and deliver implementations that meet timing requirements. Designs which have diverse timing requirements are ideally implemented because path slack estimates are refined throughout the autolayout process insuring only the resources required to meet timing requirements are consumed.

The process begins by flattening the design and partitioning it into small component groups of approximately the same size called clusters. A cluster boundary delay estimation is applied to pull the most tightly constrained paths into a minimum number of clusters. The clusters are then assigned to zones talking into account zonal boundary delay cost and relative zone placement delay costs. Other costs like total number of port connections per zone and are also considered. As assignment proceeds, cluster and zone boundary delay costs are added to each path and slack is recomputed.

Next global placement and routing is done. Global routes begin and end on either I/O cells or port cells. Intrazone placement and routing is deferred to a later phase. During global routing all the port cell and I/O cell locations are fixed and the connections between them established. High fanout nets are constructed in a highly regular manner to insure efficient resource utilization. As in partitioning, slack estimates are refined throughout global routing.

Finally the intrazonal placement and routing is done. Cells assigned to a particular zone are placed and routed to other zone cells or zone port cells. Port cells and core cells are constructed to allow port swapping. Core cells can be routed through if necessary. Allowing core cells to act as routing cells allows dynamic adjustment of routing resources within the zone. Dynamic resource adjustment is a powerful design specific adaptation mechanism.

This process produces a layout from which device configurations, delay back annotations, and chipviews can be generated.

Incremental Design Support

When specification changes necessitate design iterations, simply push the button again. Constraints are automatically recalculated and autolayout only reworks those portions of the design which have changed. Full incremental design support means simple design changes to facilitate design verification can be made quickly and easily.

Delay Back Annotation

Designs can be verified through numerous methods. One particularly useful method is the annotation of device and implementation specific delays back into the original simulation environment to improve system or device level simulation accuracy. A MPA device layout can be transformed into an appropriately formatted delay annotation file or annotated netlist quickly and easily. The annotated delay information represents the worst case delays for a given device speed grade.

Chipview

While the MPA design system provides a rich set of reports describing the implementation of a design, a graphical view of the implementation can be indispensable for reviewing overall layout quality. Chipview provides a graphical view of a completed layout. Chipview can be useful during initial design iterations to visually verify I/O pin placements before commencing PCB layout, for example.

Configuration

A layout can be transformed into a device configuration which, when loaded into the appropriate MPA device, produces a physical design realization. Many formatting options are available. The MPA download pod can be used to emulate a serial PROM. Using the pod, device configuration files can be downloaded to a device directly from the PC or workstation development environment.

Integration Kits

The MPA design system can be used with a large number of commercial electronic design automation software. Figure X–X shows the currently supported vendors and tools. For each supported vendor, an integration kit is provided which facilitates MPA design within that vendors' environment. Many of these kits are available from Motorola and included at no charge on the MPA design system CD–ROM. Other kits can be acquired directly from the vendor. Refer to the MPA Design System Product List for more information.

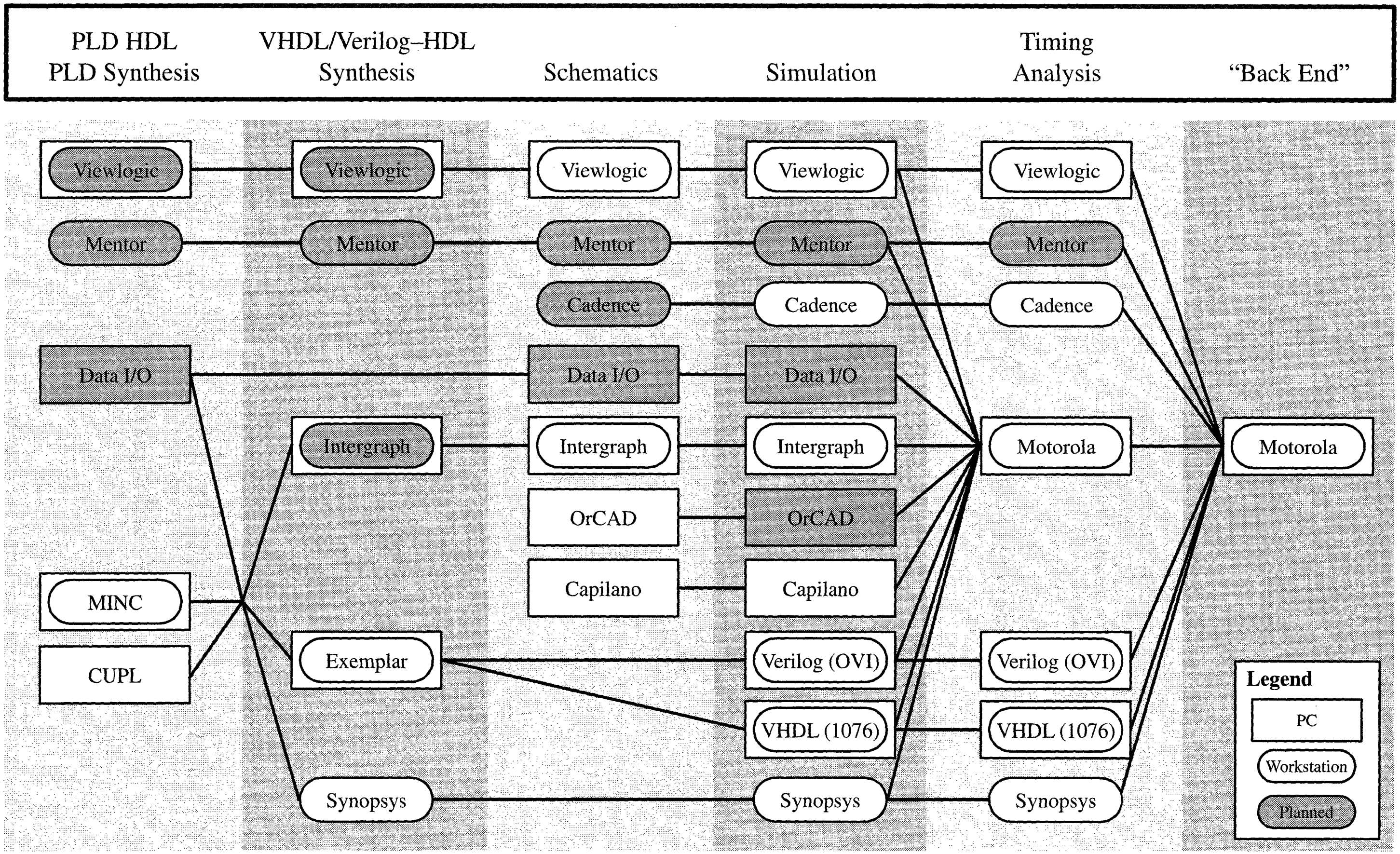
Low Cost, Easy Access

MPA Design systems are easy to use, competitively priced and widely available. Copies of MPA design system software supporting up to 8000 gates can be downloaded from the World Wide Web (WWW) @ http://Design–NET.com/fpga. Complete kits including download pod, evaluation board, MPA device, CD–ROM and documentation can be ordered from your local authorized Motorola distributor or Motorola sales representative (see appendix Z).

Fast, Efficient Design Implentation With Minimal Investment.

That's MPA!

SOFTWARE FLOWS – WORKSTATION and PC



Design System Product List

MPA Design Kits and Options

Part Number	Description
MPA1E/P MPA1E/W	Entry Level PC with 6 Months Maintenance Entry Level Workstation with 6 Months Maintenance
MPA1S/P MPA1S/W	Standard Level PC with 6 Months Maintenance Standard Level Workstation with 6 Months Maintenance
MPA1M12/P MPA1M12/W	12 Months Maintenance PC 12 Months Maintenance Workstation
MPA1CD/P MPA1CD/W	MPA Design System CDROM PC MPA Design System CDROM Workstation (Requires License)
MPA1/POD	Configuration Download POD
MPA1/BRD	Evaluation Board with MPA Device

Schematic Capture and Simulation

Part Number	Description
MPA1/SCH/P MPA1/SCH/W MPA1/SCH/WF	Schematic Capture PC Schematic Capture Workstation, Node Locked Schematic Capture Workstation, Floating
MPA1/SSM/P MPA1/SSM/W MPA1/SSM/WF	Schematic Capture and 20K Simulation PC Schematic Capture and 20K Simulation Workstation, Node Locked Schematic Capture and 20K Simulation Workstation, Floating
MPA1/SSU/P MPA1/SSU/W MPA1/SSU/WF	Schematic and Simulation UPGRADE** PC Schematic and Simulation UPGRADE** Workstation Node Locked Schematic and Simulation UPGRADE** Workstation Floating
MPA1M12/SCH/P MPA1M12/SCH/W MPA1M12/SSM/P MPA1M12/SSM/W	Schematic Maintenance, 12 Months, PC Schematic Maintenance, 12 Months, Workstation Schematic & Simulation Maintenance, 12 Months, PC Schematic & Simulation Maintenance, 12 Months, Workstation

** Upgrades existing vendor locked Viewlogic for MPA support.

MPA Design Kit Description

- MPA Design System Software on CDROM
  - Design Import and Retargeting
  - Timing Driven Placement and Routing
  - Layout Viewer
  - Layout Delay Extraction (Annotation)
  - Incremental Design
  - On–Line MPA Device and Design Kit Help
- MPA Device Support
  - Entry Level: MPA1016, MPA1036
  - Standard Level: All MPA1000 Devices
- Evaluation Board with MPA Device (MPA1/BRD)
- Download POD (MPA1/POD)
- 6 Months Maintenance
- All Integration Kits*

*The MPA Design System CDROM contains integration kits for Viewlogic, Exemplar, Synopsys, VHDL (1076), Verilog (OVI), and OrCAD. For other integration kits, contact your EDA vendor.

MPA Design System Maintenance

- Support Line Access 1–800–521–6274
- Upgrades

MPA Design System Download POD

- RS232 Connection to Host Computer
- Emulates Serial PROM
- Loads MPA Device via Host Computer

MPA Design System Evaluation Board

- MPA Device
- Simple PCB Facillitating MPA Evaluation

Platform Requirements

- PC Platform – 33MHz 486, 16Mb RAM, 32Mb Swap, 40MB Free Disk Space, Serial Port, Windows 3.1 or Later, Windows/NT
- Sun Platform Requirements: Sun SPARC Compatible, 32Mb RAM, 40Mb Swap, 60Mb Free Disk Space, SunOS 4.1.3, Solaris 2.3, Windows Manager: OSF/MOTIF 1.2 X11r5

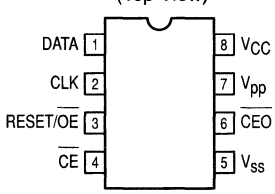
MPA17000 Serial EPROMs

The MPA17128, MPA1765 serial OTP EPROMs provide a compact, low pin count, non–volatile configuration store for MPA1000 devices.

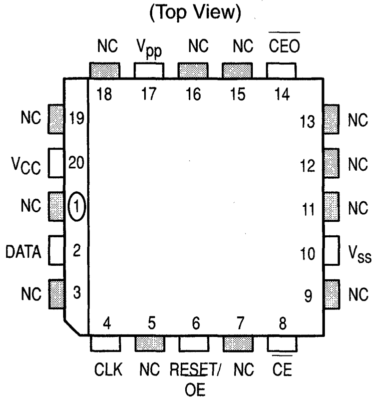
MPA17000 devices can be cascaded for increased memory capacity when needed. They are available in the standard 8–pin plastic DIP (N suffix), 8–pin SOIC (D suffix) and 20–pin PLCC (FN suffix) packages.

- Configuration EPROM for MPA1000 Devices
- Voltage Range — 4.5 to 6.0V
- Maximum Read Current of 10mA
- Standby Current of 10µA, Typical
- Industry Standard Synchronous Serial Interface
- Full Static Operation
- 10MHz Maximum Clock Rate at 5.0V
- Programmable Polarity on Hardware Reset
- Programs With Industry Standard Programmers
- Electrostatic Discharge Protection > 2000 Volts
- 8–Pin PDIP and SOIC; 20–Pin PLCC Packages
- Commercial (0 to +70°C) and Industrial (–40 to +85°C)

8–Lead Pinouts
(Top View)

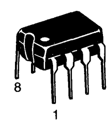


20–Lead Pinout
(Top View)

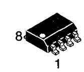


MPA17128
MPA1765

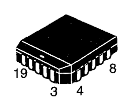
128K, 64K SERIAL EPROM



P SUFFIX
PLASTIC PACKAGE
CASE 626–05



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–05



FN SUFFIX
PLCC PACKAGE
CASE 775–02

PIN NAMES

Pins	Function
DATA	Data I/O
CLK	Clock
RESET/$\overline{\text{OE}}$	Reset Input and Output Enable
$\overline{\text{CE}}$	Chip Enable Input
V_{SS}	Ground
$\overline{\text{CEO}}$	Chip Enable Output
V_{PP}	Programming Voltage Supply
V_{CC}	+4.5 to 6.0V Power Supply
NC	Not Connected

Selection by Function

In order to better serve our customers, we have made some modifications to the Selection by Function portion of the Logic Selector Guide. For easy selection of Logic's newer, more complex functions, as well as standard family functions, refer to the subject index below. Within the Selection by Function tables on the next 23 pages, you will find functions sorted by these broad subjects, and then broken down alphabetically into more precise functions.

Logic Functions

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
ARITHMETIC OPERATORS						
4–Bit Arithmetic Logic Unit	TTL	MC74F181	—	24	N	DW
	TTL	MC74F381	—	20	N	DW
	TTL	MC74F382	—	20	N	DW
	TTL	SN54LS181	SN74LS181	24	N,J	DW
4–Bit Arithmetic Logic Unit/Function Generator	ECL	MC10H181	—	24	P,L, PW, LW	FN
	ECL	MC10181	—	24	P,L	
4–Bit Binary Full Adder With Fast Carry	TTL	MC74F283	—	16	N	D
	TTL	SN54LS83A	SN74LS83A	14	N,J	D
	TTL	SN54LS283	SN74LS283	16	N,J	D
4–Bit Full Adder	CMOS	MC14008B	—	16	P,L	D
9's Complementer	CMOS	MC14561B	—	14	P	D
BCD Rate Multiplier	CMOS	MC14527B	—	16	P	DW
Carry Lookahead Generator	TTL	MC74F182	—	16	N	D
Dual 2–Bit Adder/Subtractor	ECL	MC10H180	—	16	P,L	FN
	ECL	MC10180	—	16	P,L	
Look Ahead Carry Block	ECL	MC10H179	—	16	P,L	FN
NBCD Adder	CMOS	MC14560B	—	16	P,L	D
Triple Serial Adder (Negative Logic)	CMOS	MC14038B	—	16	L	
BOUNCE ELIMINATOR						
Hex Contact Bounce Eliminator	CMOS	MC14490	—	16	P,L	DW
BUFFERS						
1:2 Differential Fanout Buffer	ECL	MC100LVEL11	—	8		D
2:8 Differential Fanout Buffer	ECL	MC100LVE310	MC100E310	28		FN
Dual 1:3 Fanout Buffer	ECL	MC100LVEL13	MC100EL13	20		DW
Expandable Buffer	DTL	MC832	—	14	P,L	
Low Voltage Dual 1:4, 1:5 Differential Fanout Buffer, ECL/PECL Compatible	ECL	MC100LVE210	MC100E210	28		FN
BUFFERS, 3–STATE						
Low–Voltage CMOS Octal Buffer, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX244	—	20		DW,M, DT
Low–Voltage CMOS Octal Buffer, 3–State, Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX240	—	20		DW,M, DT
Low–Voltage CMOS Octal Buffer Flow Through Pinout, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX541	—	20		DW,M, DT
Low–Voltage CMOS Octal Buffer Flow Through Pinout, 3–State, Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX540	—	20		DW,M, DT
Low–Voltage Quiet CMOS Octal Buffer	CMOS	MC74LVQ541	—	20		D,M, SD,DT
Low–Voltage Quiet CMOS Octal Buffer, 3–State, Non–Inverting	CMOS	MC74LVQ244	—	20		DW,M, SD,DT
Low–Voltage Quiet CMOS Octal Buffer, 3–State, Inverting	CMOS	MC74LVQ240	—	20		DW,M, SD,DT
Low–Voltage Quiet CMOS Quad Buffer, 3–State, Non–Inverting	CMOS	MC74LVQ125	—	14		D,M, SD,DT
BUS INTERFACE						
10–Bit Buffer/Line Driver (Inverting), With 3–State Outputs	TTL	MC74F828	—	24	N	DW
10–Bit Buffer/Line Driver (Non–Inverting), With 3–State Outputs	TTL	MC74F827	—	24	N	DW
3–Bit Registered Bus Transceiver, 25Ω Cutoff Outputs	ECL	MC10E336	MC100E336	28		FN

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
BUS INTERFACE						
3–Bit Scannable Registered Bus Transceiver	ECL	MC10E337	MC100E337	28		FN
32–Bit to 32/16/8–Bit Dynamic READ/WRITE Bus Sizer	CMOS	MC68150*33	—	68		FN
	CMOS	MC68150*40	—	68		FN
9–Bit Bus Interface, NINV, 3 State Outputs	TTL	MC74F823	—	24	N	DW
Bus Driver	ECL	MC10128	—	16	L	
Dual Bus Driver/Receiver With 4–to–1 Output Multiplexer (25Ω)	ECL	MC10H332	—	20	P,L	FN
Hex 3–State Non–Inverting Buffer With Separate 2–Bit and 4–Bit Sections	CMOS	MC54HC367	MC74HC367	16	N,J	
Hex Buffer 4/2–Bit/Inverting With 3–State Outputs	TTL	SN54LS368A	SN74LS368A	16	N,J	D
Hex Buffer 4/2–Bit/Non–Inverting With 3–State Outputs	TTL	SN54LS367A	SN74LS367A	16	N,J	D
Hex Buffer Driver, 4+2–Bit, Inverting, With 3–State Outputs	TTL	MC74F368	—	16	N	D
Hex Buffer Gated Enable Inverting With 3–State Outputs	TTL	SN54LS366A	SN74LS366A	16	N,J	D
Hex Buffer Gated Enable Non–Inverting With 3–State Outputs	TTL	SN54LS365A	SN74LS365A	16	N,J	D
Hex Buffer/Driver Gated Enable Inverting, With 3–State Outputs	TTL	MC74F366	—	16	N	D
Hex Buffer/Driver Gated Enable Non–Inverting, With 3–State Outputs	TTL	MC74F365	—	16	N	D
Hex Buffer/Driver, 4+2–Bit, Non–Inverting, With 3–State Outputs	TTL	MC74F367	—	16	N	D
Hex With 3–State Outputs Buffer (Non–Inverting)	CMOS	MC14503B	—	16	P,L	D
Hex With 3–State Outputs Inverting Buffer With Common Enables	CMOS	MC54HC366	MC74HC366	16	N,J	
Hex With 3–State Outputs Inverting Buffer With Separate 2–Bit and 4–Bit Sections	CMOS	MC74HC368	—	16	N	
Hex With 3–State Outputs Non–Inverting Buffer With Separate 2–Bit/4–Bit Sections	CMOS	MC54HC365	MC74HC365	16	N,J	DT
Octal 3–State Non–Inverting Bus Transceiver With LSTTL Compatible Inputs	CMOS	MC54HCT245A	MC74HCT245A	20	N,J	DW, SD,DT
Octal Bidirectional Transceiver With 3–State Inputs/Outputs	CMOS	MC74AC245	—	20	N	DW
	CMOS	MC74ACT245	—	20	N	DW
Octal Bidirectional Transceiver With 3–State Outputs	CMOS	MC74AC620	—	20	N	DW
	CMOS	MC74ACT620	—	20	N	DW
	CMOS	MC74AC623	—	20	N	DW
	CMOS	MC74ACT623	—	20	N	DW
	CMOS	MC74AC640	—	20	N	DW
	CMOS	MC74ACT640	—	20	N	DW
	CMOS	MC74AC643	—	20	N	DW
	CMOS	MC74ACT643	—	20	N	DW
	TTL	MC74F245	—	20	N	DW
Octal Bidirectional Transceiver With 8–Bit Parity Generator Checker, With 3–State Outputs	TTL	MC74F657A	—	24	N	DW
	TTL	MC74F657B	—	24	N	DW
Octal Bidirectional Transceiver, With 3–State Inputs/Outputs	TTL	MC74F1245	—	20	N	DW
Octal Buffer With 3–State Outputs (81LS95)	TTL	SN54LS795	SN74LS795	20	N,J	DW
(81LS96)	TTL	SN54LS796	SN74LS796	20	N,J	DW
(81LS97)	TTL	SN54LS797	SN74LS797	20	N,J	DW
(81LS98)	TTL	SN54LS798	SN74LS798	20	N,J	DW
Octal Buffer/Line Driver With 3–State Outputs	TTL	SN54LS244	SN74LS244	20	N,J	DW
	TTL	MC74F240	—	20	N	DW
	TTL	MC74F241	—	20	N	DW
	TTL	MC74F244	—	20	N	DW
	TTL	SN54LS240	SN74LS240	20	N,J	DW
	TTL	SN54LS241	SN74LS241	20	N,J	DW

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
BUS INTERFACE						
Octal Buffer/Line Driver With 3–State Outputs	TTL	SN54LS540	SN74LS540	20	N,J	DW
	TTL	SN54LS541	SN74LS541	20	N,J	DW
	CMOS	MC74AC241	—	20	N	DW
	CMOS	MC74AC244	—	20	N	DW
	CMOS	MC74ACT244	—	20	N	DW
	CMOS	MC74AC540	—	20	N	DW
	CMOS	MC74ACT540	—	20	N	DW
	CMOS	MC74AC541	—	20	N	DW
	CMOS	MC74ACT541	—	20	N	DW
	CMOS	MC74AC240	—	20	N	DW
	CMOS	MC74ACT240	—	20	N	DW
	CMOS	MC74ACT241	—	20	N	DW
Octal Bus Transceiver	TTL	SN54LS245	SN74LS245	20	N,J	DW
	TTL	SN54LS623	SN74LS623	20	N,J	DW
Octal Bus Transceiver, With 3–State Outputs	TTL	MC74F623	—	20	N	DW
Octal Bus Transceiver/Inverting With 3–State Outputs	TTL	SN54LS640	SN74LS640	20	N,J	DW
	TTL	MC74F620	—	20	N	DW
	TTL	MC74F640	—	20	N	DW
Octal Bus Transceiver/Non–Inverting With 3–State Outputs	TTL	SN54LS645	SN74LS645	20	N,J	DW
Octal Bus Transceiver/Register With 3–State Outputs Non–Inverting	CMOS	MC74AC652	—	24	N	DW
	CMOS	MC74ACT652	—	24	N	DW
Octal Registered Transceiver Inverting, With 3–State Outputs	TTL	MC74F544	—	24	N	DW
Octal Registered Transceiver Non–Inverting, With 3–State Outputs	TTL	MC74F543	—	24	N	DW
Octal Transceiver/Register With 3–State Outputs Non–Inverting	CMOS	MC74AC646	—	24	N	DW
	CMOS	MC74ACT646	—	24	N	DW
Octal Transceiver/Register With 3–State Outputs Inverting	CMOS	MC74AC648	—	24	N	DW
	CMOS	MC74ACT648	—	24	N	DW
Octal Transceiver/Register, With 3–State Outputs	TTL	MC74F646	—	24	N	DW
Octal With 3–State Non–Inverting Buffer/Line Driver/Line Receiver	CMOS	MC54HC241A	MC74HC241A	20	N,J	DW
Octal With 3–State Non–Inverting Buffer/Line Driver/Line Receiver With LSTTL Compatible Inputs	CMOS	MC54HCT241A	MC74HCT241A	20	N,J	DW
	CMOS	MC54HCT244A	MC74HCT244A	20	N,J	DW, SD,DT
Octal With 3–State Outputs Inverting Buffer/Line Driver/Line Receiver	CMOS	MC54HC240A	MC74HC240A	20	N,J	DW, DT
	CMOS	MC54HC540A	MC74HC540A	20	N,J	DW
Octal With 3–State Outputs Inverting Buffer/Line Driver/Line Receiver With LSTTL Compatible Inputs	CMOS	MC74HCT240A	—	20	N	DW, SD,DT
Octal With 3–State Outputs Inverting Bus Transceiver	CMOS	MC54HC640A	MC74HC640A	20	N,J	DW
Octal With 3–State Outputs Non–Inverting Buffer/Line Driver/Line Receiver	CMOS	MC54HC541A	MC74HC541A	20	N,J	DW
Octal With 3–State Outputs Non–Inverting Buffer/Line Driver/Line Receiver With LSTTL Compatible Inputs	CMOS	MC74HCT541A	—	20	N	DW
Octal With 3–State Outputs Non–Inverting Buffer/Line Driver/Line Receiver	CMOS	MC54HC244A	MC74HC244A	20	N,J	DW, SD,DT
Octal With 3–State Outputs Non–Inverting Bus Transceiver	CMOS	MC54HC245A	MC74HC245A	20	N,J	DW
Octal With 3–State Outputs Non–Inverting Bus Transceiver & D Flip–Flop	CMOS	MC54HC646	MC74HC646	24	N,J	DW
Quad Buffers With 3–State Outputs	TTL	SN54LS125A	SN74LS125A	14	N,J	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
BUS INTERFACE						
Quad 3–State Non–Inverting Buffers	CMOS	MC74HC125A	—	14	N	D
	CMOS	MC74HC126A	—	14	N	D
Quad Buffer With 3–State Outputs	CMOS	MC74AC125	—	14	N	D
	CMOS	MC74ACT125	—	14	N	D
	CMOS	MC74AC126	—	14	N	D
	CMOS	MC74ACT126	—	14	N	D
	TTL	MC74F125	—	14	N	D
	TTL	MC74F126	—	14	N	D
	TTL	SN54LS126A	SN74LS126A	14	N,J	D
Quad Bus Driver	ECL	MC10192	—	16	P,L	FN
Quad Bus Driver/Receiver With 2–to–1 Output Multiplexer (25Ω)	ECL	MC10H330	—	24	P,L	FN
Quad Bus Driver/Receiver With Transmit & Receiver Latches (25Ω)	ECL	MC10H334	—	20	P,L	FN
Quad Bus Transceiver/Inverting With 3–State Outputs	TTL	SN54LS242	SN74LS242	14	N,J	D
Quad Bus Transceiver/Non–Inverting With 3–State Outputs	TTL	SN54LS243	SN74LS243	14	N,J	D
Quad Bus Transceivers With 3–State Outputs	TTL	MC74F242	—	14	N	D
	TTL	MC74F243	—	14	N	D
Quad With 3–State Outputs Inverting Bus Transceiver	CMOS	MC74HC242	—	14	N	
Triple 3–Input Bus Driver With Enable (25Ω)	ECL	MC10H423	—	16	P,L	FN
Triple 4–3–3 Input Bus Driver (25Ω)	ECL	MC10H123	—	16	P,L	FN
	ECL	MC10123	—	16	P,L	FN
CBM						
CBM – Carrier Band Modem	SXLG	MC68194	—	52		*FJ
CLOCK DISTRIBUTION CHIPS						
1:4 Clock Distribution Chip	ECL	MC10EL15	MC100EL15	16		D
1:5 Clock Distribution Chip	ECL	MC100LVEL14	MC100EL14	20		DW
1:6 Differential Clock Distribution Chip	ECL	MC10E211	MC100E211	28		FN
Low Voltage 1:12 Clock Distribution Chip	SXLG	MPC948	—	32		FA
Low Voltage 1:9 Clock Distribution Chip	SXLG	MPC947	—	32		FA
Low Voltage 1:9 ECL/PECL Clock Distribution Chip	ECL	MC100LVE111	—	28		FN
CLOCK DRIVERS						
1:2 Differential Clock Driver	ECL	MC10EL11	MC100EL11	8		D
1:6 PCI Clock Generator/Fanout Buffer	SXLG	MPC903	—	16		D
	SXLG	MPC904	—	16		D
1:9 Differential Clock Driver With Low Skew, Enable, Vbb	ECL	MC10E111	MC100E111	28		FN
1:9 Differential ECL/PECL RAMBus Clock Buffer	ECL	MC10E411	—	28		FN
1:9 TTL/TTL Clock Distribution Chip	ECL	MC10H645	—	28		FN
50 MHz Low Skew CMOS PLL Clock Driver With µP Power Down	CMOS	MC88920	—	20		DW
66 MHz Low Skew CMOS PLL Clock Driver With µP Power–Down/Power–Up Feature	CMOS	MC88921	—	20		DW
68030/040 PECL/TTL Clock Driver	ECL	MC10H640	MC100H640	28		FN
	ECL	MC10H642	MC100H642	28		FN
	ECL	MC10H644	MC100H644	20		FN
Clock Driver Quad D–Type Flip–Flop w/ Matched Propagation Delays	TTL	MC74F1803	—	14	N	D
	TTL	MC74F803	—	14	N	D
CMOS PLL Clock Driver Programmable Frequency, Low Skew, High Fan–Out	CMOS	MC88PL117	—	52		FN

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
CLOCK DRIVERS						
Dual Supply ECL/TTL 1:8 Clock Driver	ECL	MC10H643	MC100H643	28		FN
High Frequency PLL Clock Generator		MC12429	—	28		FN
		MC12439	—	28		FN
Low Skew CMOS Clock Driver	CMOS	MC88913	—	14	N	D
Low Skew CMOS Clock Driver With Reset	CMOS	MC88914	—	14	N	D
Low Skew CMOS PLL 68060 Clock Driver	CMOS	MC88LV926	—	20		DW
Low Skew CMOS PLL Clock Driver	CMOS	MC88915*55	—	28		FN
	CMOS	MC88915*70	—	28		FN
Low Skew CMOS PLL Clock Driver With Processor Reset	CMOS	MC88916*70	—	20		DW
	CMOS	MC88916*80	—	20		DW
Low Skew CMOS PLL Clock Driver 160 MHz Version	CMOS	MC88915T*160	—	28		FN
133 MHz Version	CMOS	MC88915T*133	—	28		FN
100 MHz Version	CMOS	MC88915T*100	—	28		FN
70 MHz Version	CMOS	MC88915T*70	—	28		FN
55 MHz Version	CMOS	MC88915T*55	—	28		FN
Low Voltage PLL Clock Driver	SXGL	MPC930	MPC931	32		FA
Low Voltage PLL Clock Driver	SXGL	MPC950	MPC951	32		FA
Low Voltage PLL Clock Driver	SXGL	MPC956	—	32		FA
Low Voltage PLL Clock Driver	SXGL	MPC970	—	32		FA
PECL/TTL to TTL 1: 8 Clock Distribution Chip	ECL	MC10H646	MC100H646	28		FN
Single Supply PECL/TTL 1:9 Clock Distribution Chip	ECL	MC10H641	MC100H641	28		FN
÷2, ÷4/6 Clock Generation Chip (3.3V)	ECL	MC100LVEL38	MC100EL38	20		DW
÷2/4, ÷4/6 Clock Generation Chip	ECL	MC100LVEL39	MC100EL39	20		DW
÷2,4,8 Differential Clock Driver	ECL	MC10EL34	MC100EL34	16		D
COAX CABLE DRIVERS						
Fibre Channel Coaxial Cable Driver and Loop Resiliency Circuit	SDX	MC10SX1189	—	16		D
300 MBit/s LED Driver for FDDI and Fibre Channel	SDX	MC10SX1130	—	16		D
COMPARATORS						
4–Bit Magnitude Comparator	TTL	MC74F85	—	16	N	D
	CMOS	MC74HC85	—	16	N	DT
	TTL	SN54LS85	SN74LS85	16	N,J	D
	CMOS	MC14585B	—	16	P,L	D
5–Bit Magnitude Comparator	ECL	MC10H166	—	16	P,L	FN
	ECL	MC10166	—	16	P,L	FN
8–Bit Equality Comparator	CMOS	MC54HC688	MC74HC688	20	N,J	DW
8–Bit Identity Comparator	CMOS	MC74ACT521	—	20	N	
	TTL	MC74F521	—	20	N	DW
8–Bit Magnitude Comparator	TTL	SN54LS682	SN74LS682	20	N,J	DW
	TTL	SN54LS684	SN74LS684	20	N,J	DW
	TTL	SN54LS688	SN74LS688	20	N,J	DW
9–Bit Magnitude Comparator	ECL	MC10E166	MC100E166	28		FN
Dual Analog Comparator With Latch	ECL	MC10E1651	—	16,20	L	FN
Dual Analog Comparator With Latch (Hi–Perf MC1651)	ECL	MC10E1652	—	16,20	L	FN

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
CONVERTERS						
4–Bit Parallel to Serial Converter	ECL	MC10E446	MC100E446	28		FN
4–Bit Serial to Parallel Converter	ECL	MC10E445	MC100E445	28		FN
Dual A/D Converter	ECL	MC1650	—	16	L	
	ECL	MC1651	—	16	L	
COUNTERS						
12–Bit Binary Counter	CMOS	MC14040B	—	16	P,L	D
12–Stage Binary Ripple Counter	CMOS	MC54HC4040A	MC74HC4040A	16	N,J	D,DT
	CMOS	MC74AC4040	—	16	N	D
14–Bit Binary Counter	CMOS	MC14020B	—	16	P,L	D
14–Bit Binary Counter and Oscillator	CMOS	MC14060B	—	16	P,L	D
14–Stage Binary Ripple Counter	CMOS	MC74HC4020A	—	16	N	D,DT
	CMOS	MC74AC4020	—	16	N	D
14–Stage Binary Ripple Counter With Oscillator	CMOS	MC54HC4060	MC74HC4060	16	N,J	DT
	CMOS	MC54HC4060A	MC74HC4060A	16	N,J	D,DT
3–Digit BCD Counter	CMOS	MC14553B	—	16	P	DW
4–Bit BCD Decade Counter, Asynchronous Reset	TTL	SN54LS160A	SN74LS160A	16	N,J	D
	TTL	SN54LS162A	SN74LS162A	16	N,J	D
4–Bit Bidirectional Binary Counter, With 3–State Outputs	TTL	MC74F569	—	20	N	DW
4–Bit Bidirectional Decade Counter, With 3–State Outputs	TTL	MC74F568	—	20	N	DW
4–Bit Binary Counter	TTL	SN54LS93	SN74LS93	14	N,J	D
	TTL	SN54LS293	SN74LS293	14	N,J	D
	ECL	MC10H16	—	16	P,L	FN
4–Bit Binary Counter, Synchronous Presettable	CMOS	MC14161B	—	16	P	D
	CMOS	MC14163B	—	16	P	D
4–Bit Binary Counter, Synchronous Reset	TTL	SN54LS161A	SN74LS161A	16	N,J	D
	TTL	SN54LS163A	SN74LS163A	16	N,J	D
4–Bit Up/Down Counter With 3–State Outputs	TTL	SN54LS569A	SN74LS569A	20	N,J	DW
4–Stage Presettable Ripple Counters	TTL	SN54LS196	SN74LS196	14	N,J	D
	TTL	SN54LS197	SN74LS197	14	N,J	D
4–Stage Synchronous Bidirectional Counter	TTL	MC74F168	—	16	N	D
	TTL	MC74F169	—	16	N	D
5 Cascaded BCD Counters	CMOS	MC14534B	—	24	P,L	DW
6–Bit Universal Counter, (Lookahead Carry)	ECL	MC10E136	MC100E136	28		FN
7–Stage Ripple Counter	CMOS	MC14024B	—	14	P,L	D
8–Bit Bidirectional Binary Counter	TTL	MC74F269	—	24	N	DW
8–Bit Bidirectional Binary Counter, With 3–State Outputs	TTL	MC74F579	—	20	N	DW
	TTL	MC74F779	—	16	N	D
8–Bit Ripple Counter	ECL	MC10E137	MC100E137	28		FN
8–Bit Synchronous Binary Up Counter	ECL	MC10E016	MC100E016	28		FN
BCD Decade Counter, Synchronous Presettable	TTL	MC74F160A	—	16	N	D
	TTL	MC74F162A	—	16	N	D
BCD Decade Synchronous Bidirectional Counter	TTL	SN54LS168	SN74LS168	16	N,J	D
Bi–Quinary Counter	ECL	MC10138	—	16	P,L	FN
Binary Counter	ECL	MC10154	—	16	P,L	
	ECL	MC10178	—	16	P,L	FN
Binary Counter, Synchronous Presettable, 4–Bit	TTL	MC74F161A	—	16	N	D
	TTL	MC74F163A	—	16	N	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
COUNTERS						
Counter Control Logic	ECL	MC12014	—	16	P,L	
Decade Counter	TTL	SN54LS90	SN74LS90	14	N,J	D
	TTL	SN54LS290	SN74LS290	14	N,J	D
	CMOS	MC14017B	—	16	P,L	D
	CMOS	MC74HC4017	—	16	N	D
Divide By 12 Counter	TTL	SN54LS92	SN74LS92	14	N,J	D
Dual 4–Stage Binary Counter	TTL	SN54LS393	SN74LS393	16	N,J	D
Dual 4–Stage Binary Ripple Counter	CMOS	MC54HC393	MC74HC393	14	N,J	D
Dual 4–Stage Binary Ripple Counter W ÷2, ÷5 Sections	CMOS	MC54HC390	MC74HC390	16	N,J	D
Dual BCD Up Counter	CMOS	MC14518B	—	16	P,L	DW
Dual Binary Up Counter	CMOS	MC14520B	—	16	P,L	DW
Dual Decade Counter	TTL	SN54LS390	SN74LS390	16	N,J	D
	TTL	SN54LS490	SN74LS490	16	N,J	D
Industrial Time Base Generator	CMOS	MC14566B	—	16	P	D
Modulo 16 Binary Synchronous Bidirectional Counter	TTL	SN54LS169	SN74LS169	16	N,J	D
Octal Counter	CMOS	MC14022B	—	16	P,L	D
Phase Comparator and Programmable Counter	CMOS	MC14568B	—	16	P,L	D
Presettable 4–Bit BCD Down Counter	CMOS	MC14522B	—	16	P	DW
Presettable 4–Bit Binary Down Counter	CMOS	MC14526B	—	16	P,L	DW
Presettable 4–Bit Binary Up/Down Counter	TTL	SN54LS191	SN74LS191	16	N,J	D
	TTL	SN54LS193	SN74LS193	16	N,J	D
Presettable BCD Up/Down Counter	CMOS	MC14510B	—	16	P	D
Presettable BCD/Decade Up/Down Counter	TTL	SN54LS190	SN74LS190	16	N,J	D
	TTL	SN54LS192	SN74LS192	16	N,J	D
Presettable Binary Up/Down Counter	CMOS	MC14516B	—	16	P,L	D
Presettable Binary/BCD Up/Down Counter	CMOS	MC14029B	—	16	P,L	D
Presettable Counter	CMOS	MC54HC160	MC74HC160	16	N,J	D
	CMOS	MC54HC161A	MC74HC161A	16	N,J	D
	CMOS	MC54HCT161A	MC74HCT161A	16	N,J	D
	CMOS	MC54HC162	MC74HC162	16	N,J	D
	CMOS	MC54HC163A	MC74HC163	16	N,J	D
	CMOS	MC54HCT163A	MC74HCT163A	16	N,J	D
Presettable Divide–by–N Counter	CMOS	MC14018B	—	16	P	D
Programmable Dual Binary/BCD Counter	CMOS	MC14569B	—	16	P,L	DW
Programmable Modulo–N Counters (N=0–9)	ECL	MC4016	—	16	P,L	
	ECL	MC4018	—	16	P,L	
	ECL	MC4316	—	16	P,L	
Synchronous 4–Bit Up/Down Counter	TTL	SN54LS669	SN74LS669	16	N,J	D
Synchronous Presettable Binary Counter	CMOS	MC74AC161	—	16	N	D
	CMOS	MC74ACT161	—	16	N	D
	CMOS	MC74AC163	—	16	N	D
	CMOS	MC74ACT163	—	16	N	D
Synchronous Presettable Binary–Coded–Decimal Decade Counter	CMOS	MC74AC160	—	16	N	D
	CMOS	MC74ACT160	—	16	N	D
	CMOS	MC74AC162	—	16	N	D
	CMOS	MC74ACT162	—	16	N	D
Universal Decade Counter	ECL	MC10137	—	16	P,L	

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
COUNTERS						
Universal Hexadecimal Counter	ECL	MC10H136	—	16	P,L	FN
	ECL	MC10136	—	16	P,L	FN
Up/Down Counter With Preset and Ripple Clock	CMOS	MC74AC190	—	16	N	D
DECODER/DEMULTIPLEXERS						
1–of–10 Decoder	CMOS	MC74HC42	—	16	N	D
	TTL	SN54LS42	SN74LS42	16	N,J	D
1–of–10 Decoder/Driver Open–Collector	TTL	SN54LS145	SN74LS145	16	N,J	D
1–of–10 Decoder, With 3–State Outputs	TTL	MC74F537	—	20	N	DW
1–of–16 Decoder/Demultiplexer	CMOS	MC54HC154	MC74HC154	24	N,J	DW
1–of–16 Decoder/Demultiplexer With Address Latch	CMOS	MC74HC4514	—	24	N	DW
1–of–4 Decoder, With 3–State Outputs	TTL	MC74F539	—	20	N	DW
1–of–8 Decoder, With 3–State Outputs	TTL	MC74F538	—	20	N	DW
1–of–8 Decoder/Demultiplexer	CMOS	MC74AC138	—	16	N	D
	CMOS	MC74ACT138	—	16	N	D
	TTL	MC74F138	—	16	N	D
	CMOS	MC54HC138A	MC74HC138A	16	N,J	D
	CMOS	MC74HCT138A	—	16	N	D,DT
	TTL	SN54LS138	SN74LS138	16	N,J	D
1–of–8 Decoder/Demultiplexer With Address Latch	CMOS	MC74HC137	—	16	N	D
	CMOS	MC74HC237	—	16	N	D
3–Line to 8–Line Decoders/Demultiplexers With Address Latches	TTL	SN54LS137	SN74LS137	16	N,J	D
4–Bit Transparent Latch/4–to–16 Line Decoder (High)	CMOS	MC14514B	—	24	P,L	DW
4–Bit Transparent Latch/4–to–16 Line Decoder (Low)	CMOS	MC14515B	—	24	P,L	DW
8–Bit Addressable Latch/1–of–8 Decoder	CMOS	MC54HC259	MC74HC259	16	N,J	D
BCD–to–Decimal Decoder/Binary–to–Octal Decoder	CMOS	MC14028B	—	16	P,L	D
Binary to 1–4 Decoder (Low)	ECL	MC10171	—	16	P,L	FN
Binary to 1–8 Decoder, (High)	ECL	MC10H162	—	16	P,L	FN
	ECL	MC10162	—	16	P,L	FN
Binary to 1–8 Decoder, (Low)	ECL	MC10H161	—	16	P,L	FN
	ECL	MC10161	—	16	P,L	FN
Dual 1–of–4 Decoder	TTL	SN54LS155	SN74LS155	16	N,J	D
Dual 1–of–4 Decoder Open–Collector	TTL	SN54LS156	SN74LS156	16	N,J	D
Dual 1–of–4 Decoder/Demultiplexer	CMOS	MC74AC139	—	16	N	D
	CMOS	MC74ACT139	—	16	N	D
	TTL	MC74F139	—	16	N	D
Dual 1–of–4 Decoder/Demultiplexer	CMOS	MC54HC139A	MC74HC139A	16	N,J	D
	TTL	SN54LS139	SN74LS139	16	N,J	D
Dual Binary to 1–4 Decoder (High)	ECL	MC10H172	—	16	P,L	FN
	ECL	MC10172	—	16	P,L	FN
Dual Binary to 1–4 Decoder (Low)	ECL	MC10H171	—	16	P,L	FN
Dual Binary to 1–of–4 Decoder (Active High Outputs)	CMOS	MC14555B	—	16	P	D
Dual Binary to 1–of–4 Decoder (Active Low Outputs)	CMOS	MC14556B	—	16	P	D
Low–Voltage Quiet CMOS 1–of–8 Decoder/Demultiplexer	CMOS	MC74LVQ138	—	16		D,M, SD,DT
DETECTORS						
Analog Mixer	ECL	MC12002	—	14	P,L	
Phase–Frequency Detector	ECL	MC4044	—	14	P,L	D
	ECL	MC4344	—	14	P,L	

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
DETECTORS						
Phase–Frequency Detector	ECL	MC12040	—	14	P,L	FN
	ECL	MCH12140	MCK12140	8		D
DISPLAY DECODE DRIVERS						
BCD–to–Seven Segment Decoder	TTL	SN54LS48	SN74LS48	16	N,J	D
	CMOS	MC14558B	—	16	P,L	D
BCD–to–Seven Segment Decoder/Driver	TTL	SN54LS47	SN74LS47	16	N,J	D
	TTL	SN54LS247	SN74LS247	16	N,J	D
	TTL	SN54LS248	SN74LS248	16	N,J	D
	TTL	SN54LS249	SN74LS249	16	N,J	D
BCD–to–Seven Segment Latch/Decoder/Display Driver	CMOS	MC74HC4511	—	16	N	D
BCD–to–Seven Segment Latch/Decoder/Driver	CMOS	MC14511B	—	16	P,L	D,DW
BCD–to–Seven Segment Latch/Decoder/Driver for Liquid Crystals	CMOS	MC14543B	—	16	P,L	D
BCD–to–Seven Segment Latch/Decoder/Driver With Ripple Blanking	CMOS	MC14544B	—	18	P,L	
	CMOS	MC14513B	—	18	P	
High Current BCD–to–Seven Segment Decoder/Driver	CMOS	MC14547B	—	16	P,L	DW
DIVIDERS						
÷ 2 Divider	ECL	MC10EL32	MC100EL32	8		D
÷ 4 Divider	ECL	MC10EL33	MC100EL33	8		D
DRIVER						
Coaxial Cable Driver	ECL	MC10EL89	—	8		D
300MBit/s LED Driver for FDDI and Fibre Channel	ECL	MC10SX1130	—	16		D
EDACs						
Error Detection–Correction Circuit (IBM Code)	ECL	MC10163	—	16	P,L	
Error Detection–Correction Circuit (Motorola Code)	ECL	MC10193	—	16	P,L	
ENCODERS						
10–Line to 4–Line Priority Encoder	TTL	SN54LS147	SN74LS147	16	N,J	D
8–Bit Priority Encoder	CMOS	MC14532B	—	16	P,L	D
8–Input Priority Encoder	TTL	SN54LS348	SN74LS348	16	N,J	D
	ECL	MC10H165	—	16	P,L	FN
	ECL	MC10165	—	16	P,L	FN
8–Input Priority Encoder (Glitchless)	TTL	SN54LS848	SN74LS848	16	N,J	D
8–Line to 3–Line Priority Encoder	TTL	MC74F148	—	16	N	D
	TTL	SN54LS148	SN74LS148	16	N,J	D
	TTL	SN54LS748	SN74LS748	16	N,J	D
Decimal–to–BCD Encoder	CMOS	MC74HC147	—	16	N	D
ENCODER/DECODERS						
CMI Encoder/Decoder	ECL	MC100SX1230	—	28		FN
EXPANDERS						
Dual 4–Iput Expander	HTL	MC669	—	14	P,L	
Expandable Dual 4–Input Gate (Active Pullup)	HTL	MC660	—	14	P,L	
Expandable Dual 4–Input Gate (Passive Pullup)	HTL	MC661	—	14	P,L	
Expandable Dual 4–Input Line Driver	HTL	MC662	—	14	P,L	
Expandable Dual Power Gate	DTL	MC844	—	14	P,L	
	DTL	MC944	—	14	P,L	

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
FLIP-FLOPS						
3–Bit Differential Flip–Flop	ECL	MC10E431	MC100E431	28		FN
4–Bit D Flip–Flop Individual Clock, Reset Differential Output	ECL	MC10E131	MC100E131	28		FN
4–Bit D Flip–Flop With Enable	TTL	SN54LS379	SN74LS379	16	N,J	D
4–Bit D–Type Register With With 3–State Outputs	TTL	SN54LS173A	SN74LS173A	16	N,J	D
5–Bit Differential Register	ECL	MC10E452	MC100E452	28		FN
6–Bit 2:1 Mux–Register With Common Clock, Asynchronous Master Reset Single Ended	ECL	MC10E167	MC100E167	28		FN
6–Bit D Register With Common Clock, Asynchronous Master Reset, Differential Outputs	ECL	MC10E151	MC100E151	28		FN
6–Bit D Register, With Differential Inputs, (Data & Clock) , VBB, Common Reset	ECL	MC10E451	MC100E451	28		FN
6–Bit Parallel D Register With Enable	CMOS	MC74AC378	—	16	N	D
	CMOS	MC74ACT378	—	16	N	D
9–Bit Hold Register, 700MHz, With Asynchronous Master Reset	ECL	MC10E143	MC100E143	28		FN
Clocked Flip–Flop	DTL	MC845	—	14	P,L	
Clocked Flip–Flop	DTL	MC945	—	14	P,L	
D Flip–Flop With Set & Reset	ECL	MC10EL31	MC100EL31	8		D
Differential Clock D Flip–Flop	ECL	MC10EL51	MC100EL51	8		D
Differential Data & Clock D Flip–Flop	ECL	MC10EL52	MC100EL52	8		D
Dual D Flip–Flop	CMOS	MC74AC74	—	14	N	D
	CMOS	MC74ACT74	—	14	N	D
	CMOS	MC14013B	—	14	P,L	D
Dual D Flip–Flop With Set and Reset	CMOS	MC54HC74A	MC74HC74A	14	N,J	D,DT
Dual D Flip–Flop With Set and Reset With LSTTL Compatible Inputs	CMOS	MC74HCT74A	—	14	N	D
Dual D–Type Positive Edge–Triggered Flip–Flop	TTL	MC74F74	—	14	N	D
	TTL	SN54LS74A	SN74LS74A	16	N,J	D
Dual Differential Data and Clock D Flip–Flop With Set and Reset	ECL	MC100LVEL29	MC100EL29	20		DW
Dual J–K Negative Edge–Triggered Flip–Flop	TTL	SN54LS112A	SN74LS112A	16	N,J	D
	TTL	SN54LS113A	SN74LS113A	14	N,J	D
	TTL	SN54LS114A	SN74LS114A	14	N,J	D
Dual J–K Positive Edge–Triggered Flip–Flop	TTL	SN54LS109A	SN74LS109A	16	N,J	D
Dual J–K Flip–Flop	HTL	MC663	—	14	P,L	
	TTL	SN54LS107A	SN74LS107A	14	N,J	D
Dual J–K Flip–Flop (Common Clock and CD Separate SD)	DTL	MC952	—	14	P,L	
Dual J–K Flip–Flop (Separate Clock and SD, No CD)	DTL	MC953	—	14	P,L	
Dual J–K Flip–Flop Negative Edge Trigger	CMOS	MC74AC112	—	16	N	D
	CMOS	MC74ACT112	—	16	N	D
Dual J–K Flip–Flop Negative Edge Trigger	CMOS	MC74AC113	—	14	N	D
	CMOS	MC74ACT113	—	14	N	D
Dual J–K Flip–Flop With Set and Clear	TTL	SN54LS76A	SN74LS76A	16	N,J	D
Dual J–K Flip–Flop With Set and Reset	CMOS	MC74HC112	—	16	N	D,DT
Dual J–K Flip–Flop	CMOS	MC14027B	—	16	P,L	D
Dual J–K Flip–Flop With Reset	CMOS	MC74HC73	—	14	N	D
	CMOS	MC74HC107	—	14	N	D
Dual J–K Flip–Flop With Set and Reset	CMOS	MC74HC76	—	16	N	D
Dual J–K Master–Slave Flip–Flop	ECL	MC10135	—	16	P,L	FN
	ECL	MC10H135	—	16	P,L	FN

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
FLIP–FLOPS						
Dual J–K Negative Edge–Triggered Flip–Flop	TTL	MC74F112	—	16	N	D
	TTL	SN54LS73A	SN74LS73A	14	N,J	D
Dual J–K Positive Edge–Triggered Flip–Flop With Set & Clear	CMOS	MC74AC109	—	16	N	D
	CMOS	MC74ACT109	—	16	N	D
Dual J–K Flip–Flop With Set and Reset	CMOS	MC74HC109	—	16	N	D
Dual J–K Positive Edge–Triggered Flip–Flop	TTL	MC74F109	—	16	N	D
Dual Type–D Master–Slave Flip–Flop	ECL	MC10131	—	16	P,L	FN
	ECL	MC10H131	—	16	P,L	FN
Hex D Flip–Flop	TTL	SN54LS174	SN74LS174	16	N,J	D
Hex D Flip–Flop With Enable	TTL	SN54LS378	SN74LS378	16	N,J	D
Hex D Flip–Flop With Master Reset	CMOS	MC74AC174	—	16	N	D
	TTL	MC74F174	—	16	N	D
	CMOS	MC74ACT174	—	16	N	D
Hex D Flip–Flop	CMOS	MC14174B	—	16	P,L	D
Hex D Flip–Flop With Common Clock & Reset	CMOS	MC54HC174A	MC74HC174A	16	N,J	D
Hex D Flip–Flop With Common Clock & Reset	CMOS	MC74HCT174A	—	16	N	D
Hex D Master–Slave Flip–Flop	ECL	MC10H176	—	16	P,L	FN
Hex D Master–Slave Flip–Flop With Reset	ECL	MC10H186	—	16	P,L	FN
	ECL	MC10186	—	16	P,L	FN
Hex D Master–Slave Flip–Flop	ECL	MC10176	—	16	P,L	FN
High Speed Dual D Master–Slave Flip–Flop	ECL	MC10231	—	16	P,L	FN
J–K Flip–Flop	ECL	MC10EL35	MC100EL35	8		D
Low–Voltage CMOS Octal D–Type Flip–Flop, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX374	—	20		DW,M, DT
Low–Voltage CMOS Octal D–Type Flip–Flop Flow Through Pinout, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX574	—	20		DW,M, DT
Low–Voltage Quiet CMOS Octal D–Type Flip–Flop	CMOS	MC74LVQ374	—	20		DW,M, SD,DT
Low–Voltage Quiet CMOS Octal D–Type Flip–Flop Flow Through Pinout	CMOS	MC74LVQ574	—	20		DW,M, SD,DT
Master–Slave Flip–Flop	ECL	MC1670	—	16	L	
Master–Slave R–S Flip–Flop	HTL	MC664	—	14	P,L	
Octal 3–State Inverting D Flip–Flop	CMOS	MC54HC534A	MC74HC534A	20	N,J	DW
Octal 3–State Non–Inverting D Flip–Flop With LSTTL Compatible Inputs	CMOS	MC54HCT374A	MC74HCT374A	20	N,J	DW
Octal D Flip Flop, With 3–State Outputs	TTL	MC74F374	—	20	N	DW
Octal D Flip–Flop	CMOS	MC74AC273	—	20	N	DW
	CMOS	MC74ACT273	—	20	N	DW
Octal D Flip–Flop With 3–State Outputs/Broadside Pinout, F374	TTL	MC74F574	—	20	N	DW
Octal D Flip–Flop With Clear	TTL	SN54LS273	SN74LS273	20	N,J	DW
Octal D Flip–Flop With Clock Enable	CMOS	MC74AC377	—	20	N	DW
	CMOS	MC74ACT377	—	20	N	DW
Octal D Flip–Flop With Common Clock & Reset	CMOS	MC54HC273A	MC74HC273A	20	N,J	DW, DT
Octal D Flip–Flop With Common Clock and Reset With LSTTL Compatible Inputs	CMOS	MC74HCT273A	—	20	N	DW
Octal D Flip–Flop With Enable	TTL	MC74F377	—	20	N	DW
Octal D Flip–Flop With Enable/ Non–Inverting	TTL	SN54LS377	SN74LS377	20	N,J	DW
Octal D Type Flip–Flop With 3–State Outputs	CMOS	MC74AC374	—	20	N	DW

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
FLIP–FLOPS						
Octal D Type Flip–Flop With 3–State Outputs	CMOS	MC74ACT374	—	20	N	DW
	TTL	MC74F534	—	20	N	DW
	TTL	SN54LS374	SN74LS374	20	N,J	DW
	CMOS	MC74AC534	—	20	N	DW
Octal D–Type Flip–Flop With 3–State Outputs	CMOS	MC74ACT534	—	20	N	DW
Octal D–Type Latch With 3–State Outputs	CMOS	MC74AC564	—	20	N	DW
	CMOS	MC74ACT564	—	20	N	DW
	CMOS	MC74AC574	—	20	N	DW
	CMOS	MC74ACT574	—	20	N	DW
Octal With 3–State Outputs Inverting D Flip–Flop	CMOS	MC74HC564	—	20	N	DW
Octal With 3–State Outputs Non–Inverting D Flip–Flop	CMOS	MC54HC374A	MC74HC374A	20	N,J	DW, SD,DT
	CMOS	MC54HC574A	MC74HC574A	20	N,J	DW
Octal With 3–State Outputs Non–Inverting D Flip–Flop With LSTTL Compatible Inputs	CMOS	MC54HCT574A	MC74HCT574A	20	N,J	DW
Quad D Flip–Flop	CMOS	MC74AC175	—	16	N	D
	CMOS	MC74ACT175	—	16	N	D
	TTL	MC74F175	—	16	N	D
	TTL	SN54LS175	SN74LS175	16	N,J	D
	CMOS	MC14175B	—	16	P,L	D
Quad D Flip–Flop With Common Clock & Reset	CMOS	MC54HC175	MC74HC175	16	N,J	D
	CMOS	MC54HC175A	MC74HC175A	16	N,J	D,SD
Quad D–Type Register With 3–State Outputs	CMOS	MC14076B	—	16	P,L	D
Quad Parallel Register With Enable	TTL	MC74F379	—	16	N	D
Quad With 3–State Outputs D Flip–Flop With Common Clock & Reset	CMOS	MC74HC173	—	16	N	D
Triple D Flip–Flop With Set and Reset	ECL	MC100LVEL30	MC100EL30	20		DW
GATES, AND/NAND						
13–Input NAND Gate	CMOS	MC74HC133	—	16	N	D
	TTL	SN54LS133	SN74LS133	16	N,J	D
8–Input NAND Gate	CMOS	MC74HC30	—	14	N	D
	TTL	SN54LS30	SN74LS30	14	N,J	D
	CMOS	MC14068B	—	14	P	D
Dual 4–Input AND Gate	TTL	MC74F21	—	14	N	D
	TTL	SN54LS21	SN74LS21	14	N,J	D
	CMOS	MC14082B	—	14	P,L	D
Dual 4–Input NAND Buffer	TTL	MC74F40	—	14	N	D
	TTL	SN54LS40	SN74LS40	14	N,J	D
Dual 4–Input NAND Gate	CMOS	MC74AC20	—	14	N	D
	CMOS	MC74ACT20	—	14	N	D
	TTL	MC74F20	—	14	N	D
	CMOS	MC74HC20	—	14	N	D
	TTL	SN54LS20	SN74LS20	14	N,J	D
	TTL	SN54LS22	SN74LS22	14	N,J	D
	CMOS	MC14012B	—	14	P,L	D
Dual 4–Input NAND Gate (Unbuffered)	CMOS	MC14012UB	—	14	P,L	D
Expandable NAND Gate	DTL	MC830	—	14	P,L	
Hex AND Gate	ECL	MC10197	—	16	P,L	FN

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
GATES, AND/NAND						
Low–Voltage CMOS Quad 2–Input AND Gate, 5V–Tolerant Inputs	CMOS	MC74LCX08	—	14		D,DT
Low–Voltage CMOS Quad 2–Input NAND Gate, 5V–Tolerant Inputs	CMOS	MC74LCX00	—	14		D,DT
Low–Voltage Quiet CMOS Quad 2–Input NAND Gate	CMOS	MC74LVQ00	—	14		D,M, DT,SD
Quad 2–Input AND Gate	CMOS	MC74AC08	—	14	N	D
	CMOS	MC74ACT08	—	14	N	D
	TTL	MC74F08	—	14	N	D
	CMOS	MC54HC08A	MC74HC08A	14	N,J	D,DT
	TTL	SN54LS08	SN74LS08	14	N,J	D
	TTL	SN54LS09	SN74LS09	14	N,J	D
	ECL	MC10H104	—	16	P,L	FN
Quad 2–Input AND Gate	ECL	MC10104	—	16	P,L	FN
	CMOS	MC14081B	—	14	P,L	D
Quad 2–Input AND Gate With LSTTL–Compatible Inputs	CMOS	MC54HCT08A	MC74HCT08A	14	N,J	D
Quad 2–Input NAND Buffer	TTL	MC74F37	—	14	N	D
	TTL	SN54LS26	SN74LS26	14	N,J	D
	TTL	SN54LS37	SN74LS37	14	N,J	D
Quad 2–Input NAND Buffer Open–Collector	TTL	MC74F38	—	14	N	D
Quad 2–Input NAND Buffer Open–Collector	TTL	SN54LS38	SN74LS38	14	N,J	D
Quad 2–Input NAND Gate	DTL	MC846	—	14	P,L	
	DTL	MC849	—	14	P,L	
	DTL	MC946	—	14	P,L	
	CMOS	MC74AC00	—	14	N	D
Quad 2–Input NAND Gate	CMOS	MC74ACT00	—	14	N	D
	TTL	MC74F00	—	14	N	D
	CMOS	MC54HC00A	MC74HC00A	14	N,J	D,DT
	TTL	SN54LS00	SN74LS00	14	N,J	D
	TTL	SN54LS01	SN74LS01	14	N,J	D
	TTL	SN54LS03	SN74LS03	14	N,J	D
	CMOS	MC14011B	—	14	P,L	D
Quad 2–Input NAND Gate (Unbuffered)	CMOS	MC14011UB	—	14	P,L	D
Quad 2–Input NAND Gate With LSTTL–Compatible Inputs	CMOS	MC54HCT00A	MC74HCT00A	14	N,J	D
Quad 2–Input NAND Gate With Open–Drain Outputs	CMOS	MC74HC03A	—	14	N	D,DT
Triple 3–Input AND Gate	CMOS	MC74AC11	—	14	N	D
	CMOS	MC74ACT11	—	14	N	D
	TTL	MC74F11	—	14	N	D
	CMOS	MC74HC11	—	14	N	D
	TTL	SN54LS11	SN74LS11	14	N,J	D
	TTL	SN54LS15	SN74LS15	14	N,J	D
	CMOS	MC14073B	—	14	P,L	D
Triple 3–Input NAND Gate	CMOS	MC74AC10	—	14	N	D
	CMOS	MC74ACT10	—	14	N	D
	TTL	MC74F10	—	14	N	D
	CMOS	MC74HC10	—	14	N	D
	TTL	SN54LS10	SN74LS10	14	N,J	D
	TTL	SN54LS12	SN74LS12	14	N,J	D
	CMOS	MC14023B	—	14	P,L	D
Triple 3–Input NAND Gate (Unbuffered)	CMOS	MC14023UB	—	14	P,L	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
GATES, COMPLEX						
2–Input AND/NAND Gate	ECL	MC10EL04	MC100EL04	8		D
2–Input Differential AND/NAND Gate	ECL	MC10EL05	MC100EL05	8		D
2–Input XOR/NOR Gate	ECL	MC10EL07	MC100EL07	8		D
2–Wide, 2–Input/2–Wide, 3–Input AND–NOR Gate	CMOS	MC74HC51	—	14	N	D
2–Wide, 2–Input/2–Wide, 3–Input AND–OR Gate	CMOS	MC74HC58	—	14	N	D
2–Wide, 4–Input AND/OR Invert Gate	TTL	SN54LS55	SN74LS55	14	N,J	D
3–2–2–3–Input AND/OR Invert Gate	TTL	SN54LS54	SN74LS54	14	N,J	D
4–2–3–2 Input AND–OR–Invert Gate	TTL	MC74F64	—	14	N	D
4–Bit AND/OR Selector	CMOS	MC14519B	—	16	P	D
4–Input OR/NOR Gate	ECL	MC10EL01	MC100EL01	8		D
4–Wide 4–3–3–3 Input OR–AND Gate	ECL	MC10H119	—	16	P,L	FN
4–Wide 4–3–3–3 Input OR–AND Gate	ECL	MC10119	—	16	P,L	FN
4–Wide OR–AND/OR–AND–Invert Gate	ECL	MC10H121	—	16	P,L	FN
4–Wide OR–AND/OR–AND–Invert Gate	ECL	MC10121	—	16	P,L	FN
8–Input NOR/OR Gate	CMOS	MC74HC4078	—	14	N	D
Dual 2 Wide 2–Input/3–Input AND/OR Invert Gate	TTL	SN54LS51	SN74LS51	14	N,J	D
Dual 2–Wide 2–3–Input OR–AND/OR–AND–Invert Gate	ECL	MC10117	—	16	P,L	FN
	ECL	MC10H117	—	16	P,L	FN
Dual 2–Wide 2–Input, 2–Wide 3–Input AND–OR–Invert Gate	TTL	MC74F51	—	14	N	D
Dual 2–Wide 3–Input OR–AND Gate	ECL	MC10H118	—	16	P,L	FN
	ECL	MC10118	—	16	P,L	FN
Dual 4–5 Input OR/NOR Gate	ECL	MC10H109	—	16	P,L	FN
	ECL	MC10109	—	16	P,L	FN
	ECL	MC10H209	—	16	P,L	FN
Dual 4–Input NAND, 2–Input NOR/OR, 8–Input AND/NAND Gate (Unbuffered)	CMOS	MC14501UB	—	16	P	D
Dual 4–Input OR/NOR Gate	ECL	MC1660	—	16	L	
Dual 5–Input Majority Logic Gate	CMOS	MC14530B	—	16	P	D
Dual Expandable AND OR Invert Gate (Unbuffered)	CMOS	MC14506UB	—	16	L	
Hex NAND/NOR/Invert Gate (Unbuffered)	CMOS	MC14572UB	—	16	P	D
High Speed Dual 3–Input 3–Output OR/NOR Gate	ECL	MC10212	—	16	P	
Quad 4–Input OR/NOR Gate	ECL	MC10E101	MC100E101	28		FN
Quad Differential AND/NAND Gate	ECL	MC10E404	MC100E404	28		FN
Quad OR/NOR Gate	ECL	MC10H101	—	16	P,L	FN
	ECL	MC10101	—	16	P,L	FN
Quint 2–Input AND/NAND Gate	ECL	MC10E104	MC100E104	28		FN
Quint 2–Input XOR/XNOR Gate	ECL	MC10E107	MC100E107	28		FN
Triple 2–3–2 Input OR/NOR Gate	ECL	MC10H105	—	16	P,L	FN
	ECL	MC10105	—	16	P,L	FN
Triple 2–Input Exclusive OR/Exclusive NOR Gate	ECL	MC10H107	—	16	P,L	FN
	ECL	MC10107	—	16	P,L	FN
GATES, EXCLUSIVE OR/EXCLUSIVE NOR						
Quad 2–Input Exclusive NOR Gate	CMOS	MC74AC810	—	14	N	DW
	CMOS	MC74ACT810	—	14	N	DW
	CMOS	MC74HC7266	—	14	N	D
	TTL	SN54LS266	SN74LS266	14	N,J	D
Quad Exclusive NOR Gate	CMOS	MC14077B	—	14	P,L	D
Quad 2–Input Exclusive OR Gate	CMOS	MC74AC86	—	14	N	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
GATES, EXCLUSIVE OR/EXCLUSIVE NOR						
Quad 2–Input Exclusive OR Gate	CMOS	MC74ACT86	—	14	N	D
	TTL	MC74F86	—	14	N	D
	CMOS	MC54HC86	MC74HC86	14	N,J	D
	TTL	SN74LS136	—	14	N,J	D
	TTL	SN54LS386	SN74LS386	14	N,J	D
Quad Exclusive OR Gate	TTL	SN54LS86	SN74LS86	14	N,J	D
	ECL	MC10H113	—	16	P,L	FN
	ECL	MC10113	—	16	P,L	FN
	CMOS	MC14070B	—	14	P,L	D
Triple 2–Input Exclusive–OR Gate	ECL	MC1672	—	16	L	
GATES, NOR						
8–Input NOR Gate	CMOS	MC14078B	—	14	P	D
Dual 3–Input 3–Output NOR Gate	ECL	MC10111	—	16	P,L	FN
Dual 3–Input NOR Gate + Inverter (Unbuffered)	CMOS	MC14000UB	—	14	P,L	D
Dual 3–Input, 3–Output NOR Gate	ECL	MC10H211	—	16	P,L	FN
Dual 3–Input, 3–Output NOR Gate	ECL	MC10211	—	16	P,L	FN
Dual 4–Input NOR Gate	CMOS	MC74HC4002	—	14	N	D
	CMOS	MC14002B	—	14	P,L	D
Dual 4–Input NOR Gate (Unbuffered)	CMOS	MC14002UB	—	14	P,L	D
Dual 5–Input NOR Gate	TTL	SN54LS260	SN74LS260	14	N,J	D
Low–Voltage CMOS Quad 2–Input NOR Gate, 5V–Tolerant Inputs	CMOS	MC74LCX02	—	14		D,DT
Quad 2–Input NOR Buffer	TTL	SN54LS28	SN74LS28	14	N,J	D
Quad 2–Input NOR Buffer	TTL	SN54LS33	SN74LS33	14	N,J	D
Quad 2–Input NOR Gate	CMOS	MC74AC02	—	14	N	D
	CMOS	MC74ACT02	—	14	N	D
	TTL	MC74F02	—	14	N	D
	CMOS	MC54HC02A	MC74HC02A	14	N,J	D,DT
	TTL	SN54LS02	SN74LS02	14	N,J	D
	ECL	MC10H102	—	16	P,L	FN
	ECL	MC10102	—	16	P,L	FN
	ECL	MC1662	—	16	L	
Quad 2–Input NOR Gate	CMOS	MC14001B	—	14	P,L	D
Quad 2–Input NOR Gate (Unbuffered)	CMOS	MC14001UB	—	14	P,L	D
Quad 2–Input NOR Gate With strobe	ECL	MC10H100	—	16	P,L	FN
	ECL	MC10100	—	16	P,L	FN
Triple 3–Input NOR Gate	CMOS	MC54HC27	MC74HC27	14	N,J	D
	TTL	SN54LS27	SN74LS27	14	N,J	D
	CMOS	MC14025B	—	14	P,L	D
Triple 3–Input NOR Gate (Unbuffered)	CMOS	MC14025UB	—	14	P,L	D
Triple 4–3–3 Input NOR Gate	ECL	MC10H106	—	16	P,L	FN
	ECL	MC10106	—	16	P,L	FN
GATES, OR						
Dual 3–Input 3–Output OR Gate	ECL	MC10110	—	16	P,L	FN
	ECL	MC10H210	—	16	P,L	FN
	ECL	MC10210	—	16	P,L	FN
Dual 4–Input OR Gate	CMOS	MC14072B	—	14	P	D
Low–Voltage CMOS Quad 2–Input OR Gate, 5V–Tolerant Inputs	CMOS	MC74LCX32	—	14		D,DT

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
GATES, OR						
Quad 2–Input OR Gate	CMOS	MC74AC32	—	14	N	D
	CMOS	MC74ACT32	—	14	N	D
	TTL	MC74F32	—	14	N	D
	CMOS	MC54HC32A	MC74HC32A	14	N,J	D,DT
	CMOS	MC54HCT32A	MC74HCT32A	14	N,J	D
	TTL	SN54LS32	SN74LS32	14	N,J	D
	ECL	MC10H103	—	16	P,L	FN
	ECL	MC10103	—	16	P,L	FN
	CMOS	MC14071B	—	14	P,L	D
Triple 3–Input OR Gate	CMOS	MC74HC4075	—	14	N	D
	CMOS	MC14075B	—	14	P,L	D
INDUSTRIAL CONTROL UNIT						
Industrial Control Unit	CMOS	MC14500B	—	16	P	DW
INVERTERS						
Hex Inverter	DTL	MC836	—	14	P,L	
	DTL	MC837	—	14	P,L	
Hex Inverter	DTL	MC936	—	14	P,L	
	DTL	MC937	—	14	P,L	
Hex Inverter (Without Input Diodes)	DTL	MC840	—	14	P,L	
INVERTER/BUFFERS, 2–STATE						
9–Bit Buffer	ECL	MC10E122	MC100E122	28		FN
Driver	ECL	MC10EL12	MC100EL12	8		D
Dual Complementary Pair Plus Inverter (Unbuffered)	CMOS	MC14007UB	—	14	P	D
Hex Buffer With Enable	ECL	MC10H188	—	16	P,L	FN
	ECL	MC10188	—	16	P,L	FN
Hex Buffer/Non–Inverting	CMOS	MC14050B	—	16	P,L	D
Hex Inverter	CMOS	MC74AC04	—	14	N	D
	CMOS	MC74ACT04	—	14	N	D
	TTL	MC74F04	—	14	N	D
	CMOS	MC54HC04A	MC74HC04A	14	N,J	D,SD, DT
	TTL	SN54LS04	SN74LS04	14	N,J	D
	TTL	SN54LS05	SN74LS05	14	N,J	D
Hex Inverter Gate (Unbuffered)	CMOS	MC14069UB	—	14	P,L	D
Hex Inverter With Enable	ECL	MC10H189	—	16	P,L	FN
	ECL	MC10189	—	16	P,L	FN
Hex Inverter With LSTTL Compatible Inputs	CMOS	MC74HCT04A	—	14	N	D,DT
Hex Inverter With open Drain Outputs	CMOS	MC74AC05	—	14	N	D
	CMOS	MC74ACT05	—	14	N	D
Hex Inverter With Strobe (Active Pullup)	HTL	MC677	—	14	P,L	
Hex Inverter With Strobe (Without Output Resistors)	HTL	MC678	—	14	P,L	
Hex Inverter/Buffer	ECL	MC10195	—	16	P,L	FN
	CMOS	MC14049B	—	16	P	D
Hex Inverter/Buffer (Unbuffered)	CMOS	MC14049UB	—	16	P,L	D
Hex Inverting Buffer/Logic–Level Down Converter	CMOS	MC54HC4049	MC74HC4049	16	N,J	D
Hex Non–Inverting Buffer/Logic–Level Down Converter	CMOS	MC54HC4050	MC74HC4050	16	N,J	D
Hex Unbuffered Inverter	CMOS	MC74HCU04	—	14	N	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
INVERTER/BUFFERS, 2–STATE						
Low–Voltage CMOS Hex Inverter, With 5V–Tolerant Inputs	CMOS	MC74LCX04	—	14		D,DT
Low–Voltage Quiet CMOS Hex Inverter	CMOS	MC74LVQ04	—	14		D,M, SD,DT
Quad 2–Input Gate (Active Pullup)	HTL	MC672	—	14	P,L	
Quad 2–Input Gate (Passive Pullup)	HTL	MC668	—	14	P,L	
Quad Driver	ECL	MC10E112	MC100E112	28		FN
Strobed Hex Inverter/Buffer	CMOS	MC14502B	—	16	P,L	DW
Triple 3–Input Gate (Active Pullup)	HTL	MC671	—	14	P,L	
Triple 3–Input Gate (Passive Pullup)	HTL	MC670	—	14	P,L	
LATCHES						
3–Bit 4:1 Mux–Latch (Integrated E156 & E171)	ECL	MC10E256	MC100E256	28		FN
3–Bit 4:1 Mux–Latch, With Common Enable, Asynchronous Master Reset, Differential Output	ECL	MC10E156	MC100E156	28		FN
4–Bit D Latch	TTL	SN54LS75	SN74LS75	16	N,J	D
	TTL	SN54LS77	SN74LS77	14	N,J	D
	TTL	SN54LS375	SN74LS375	16	N,J	D
5–Bit 2:1 Mux–Latch, With Common Enable, Asynchronous Master Reset Differential Output	ECL	MC10E154	MC100E154	28		FN
6–Bit 2:1 Mux–Latch, With Common Enable, Asynchronous Master Reset Single Ended	ECL	MC10E155	MC100E155	28		FN
6–Bit D Latch	ECL	MC10E150	MC100E150	28		FN
8–Bit Addressable Latch	CMOS	MC74AC259	—	16	N	D
	CMOS	MC74ACT259	—	16	N	D
	TTL	MC74F259	—	16	N	D
	TTL	SN54LS259	SN74LS259	16	N,J	D
8–Bit Addressable Latch	CMOS	MC14099B	—	16	P	DW
	CMOS	MC14599B	—	18	P	
8–Bit Bus Compatible Addressable Latch	CMOS	MC14598B	—	18	P,L	
9–Bit Latch, With Parity	ECL	MC10E175	MC100E175	28		FN
Dual Latch	ECL	MC10H130	—	16	P,L	FN
Dual 2–Bit Transparent Latch	CMOS	MC74HC75	—	16	N	D
Dual 4–Bit Addressable Latch	CMOS	MC74AC256	—	16	N	DW
	CMOS	MC74ACT256	—	16	N	DW
	TTL	MC74F256	—	16	N	D
	TTL	SN54LS256	—	16	N,J	D
Dual 4–Bit Latch	CMOS	MC14508B	—	24	P,L	DW
Dual Latch	ECL	MC10130	—	16	P,L	FN
Low–Voltage CMOS Octal Transparent Latch, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX373	—	20		DW,M, DT
Low–Voltage CMOS Octal Transparent Latch Flow Through Pinout, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX573	—	20		DW,M, SD,DT
Low–Voltage Quiet CMOS Octal Transparent Latch	CMOS	MC74LVQ373	—	20		DW,M, SD,DT
Low–Voltage Quiet CMOS Octal Transparent Latch Flow Through Pinout	CMOS	MC74LVQ573	—	20		DW,M, SD,DT
Octal 3–State Non–Inverting Transparent Latch With LSTTL Compatible Inputs	CMOS	MC54HCT373A	MC74HCT373A	20	N,J	DW, SD,DT
Octal D Latch With 3–State Outputs	CMOS	MC74AC563	—	20	N	DW
	CMOS	MC74ACT563	—	20	N	DW
	CMOS	MC74AC573	—	20	N	DW

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
LATCHES						
Octal D Latch With 3–State Outputs	CMOS	MC74ACT573	—	20	N	DW
Octal Transparent Latch With 3–State Outputs	CMOS	MC74AC373	—	20	N	DW
	CMOS	MC74ACT373	—	20	N	DW
	TTL	SN54LS373	SN74LS373	20	N,J	DW
	TTL	MC74F373	—	20	N	DW
	TTL	MC74F533	—	20	N	DW
	CMOS	MC74AC533	—	20	N	DW
	CMOS	MC74ACT533	—	20	N	DW
Octal With 3–State Outputs Inverting Transparent Latch	CMOS	MC54HC533A	MC74HC533A	20	N,J	DW
	CMOS	MC54HC563	MC74HC563	20	N,J	DW
Octal With 3–State Outputs Non–Inverting Transparent Latch	CMOS	MC54HC373A	MC74HC373A	20	N,J	DW
	CMOS	MC54HC573A	MC74HC573A	20	N,J	DW
Octal With 3–State Outputs Non–Inverting Transparent Latch With LSTTL Compatible Inputs	CMOS	MC74HCT573A	—	20	N	DW
Quad Latch	ECL	MC10133	—	16	P,L	FN
	ECL	MC10153	—	16	P,L	FN
	ECL	MC10168	—	16	P	
Quad NAND R–S Latch	CMOS	MC14044B	—	16	P	D
Quad NOR R–S Latch	CMOS	MC14043B	—	16	P,L	D
Quad Set/Reset Latch	TTL	SN54LS279	SN74LS279	16	N,J	D
Quad Transparent Latch	CMOS	MC14042B	—	16	P,L	D
Quint Latch	ECL	MC10H175	—	16	P,L	FN
	ECL	MC10175	—	16	P,L	FN
MEMORY SUPPORT						
4–Bit ECL–TTL Load Reducing DRAM Driver	ECL	MC10H660	MC100H660	28		FN
MISCELLANEOUS						
Data Separator	ECL	MC10E197	—	28		FN
MULTIPLEXER/DATA SELECTORS						
1–of–8 Decoder/Demultiplexer	CMOS	MC74AC151	—	16	N	D
	CMOS	MC74ACT151	—	16	N	D
16–Channel Analog Multiplexer/Demultiplexer	CMOS	MC14067B	—	24	P	DW
16:1 Multiplexer	ECL	MC10E164	MC100E164	28		FN
2–Bit 8:1 Multiplexer	ECL	MC10E163	MC100E163	28		FN
2:1 Multiplexer	ECL	MC10EL58	MC100EL58	8		D
3–Bit 4:1 Multiplexer, With Split Select Differential Output	ECL	MC10E171	MC100E171	28		FN
4:1 Differential Multiplexer	ECL	MC10EL57	MC100EL57	16		D
5–Bit 2:1 Multiplexer, With Differential Output	ECL	MC10E158	MC100E158	28		FN
8–Channel Analog Multiplexer/Demultiplexer With Address Latch	CMOS	MC54HC4351	MC74HC4351	20	N,J	DW
8–Channel Analog Multiplexer/Demultiplexer	CMOS	MC54HC4051	MC74HC4051	16	N,J	D, DW ,DT
	CMOS	MC14051B	—	16	P,L	D
8–Channel Data Selector	CMOS	MC14512B	—	16	P,L	D
8–Input Data Selector/Multiplexer	CMOS	MC74HC151	—	16	N	D
8–Input Data Selector/Multiplexer With 3–State Outputs	CMOS	MC54HC251	MC74HC251	16	N,J	D
8–Input Multiplexer	TTL	MC74F151	—	16	N	D
	TTL	SN54LS151	SN74LS151	16	N,J	D
8–Input Multiplexer With 3–State Outputs	TTL	SN54LS251	SN74LS251	16	N,J	D
	TTL	MC74F251	—	16	N	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
MULTIPLEXER/DATA SELECTORS						
8–Input Multiplexer With 3–State Outputs	CMOS	MC74AC251	—	16	N	D
	CMOS	MC74ACT251	—	16	N	D
8–Input Data Selector/Multiplexer With Data and Address Latches and With 3–State Outputs	CMOS	MC54HC354	MC74HC354	20	N,J	DW
8–Line Multiplexer	ECL	MC10H164	—	16	P,L	FN
	ECL	MC10164	—	16	P,L	FN
Dual 4–Channel Analog Data Selector	CMOS	MC14529B	—	16	P	D
Dual 4–Channel Analog Multiplexer/Demultiplexer	CMOS	MC74HC4052	—	16	N	D, DW
	CMOS	MC14052B	—	16	P,L	D
Dual 4–Channel Data Selector/Multiplexer	CMOS	MC14539B	—	16	P	D
Dual 4–Input Data Selector/Multiplexer	CMOS	MC74HC153	—	16	N	D
Dual 4–Input Data Selector/Multiplexer With 3–State Outputs	CMOS	MC74HC253	—	16	N	D
Dual 4–Input Multiplexer	CMOS	MC74AC153	—	16	N	D
	CMOS	MC74ACT153	—	16	N	D
	CMOS	MC74AC352	—	16	N	DW
	CMOS	MC74ACT352	—	16	N	DW
	TTL	MC74F153	—	16	N	D
	TTL	MC74F352	—	16	N	D
	TTL	SN54LS153	SN74LS153	16	N,J	D
	TTL	SN54LS352	SN74LS352	16	N,J	D
Dual 4–Input Multiplexer With 3–State Outputs	CMOS	MC74AC253	—	16	N	DW
	CMOS	MC74ACT253	—	16	N	DW
	CMOS	MC74AC353	—	16	N	D
	CMOS	MC74ACT353	—	16	N	D
	TTL	SN54LS253	SN74LS253	16	N,J	D
	TTL	SN54LS353	SN74LS353	16	N,J	D
Dual 4–Input Multiplexer With 3–State Outputs	TTL	MC74F253	—	16	N	D
	TTL	MC74F353	—	16	N	D
Dual 4–to–1 Multiplexer	ECL	MC10H174	—	16	P,L	FN
	ECL	MC10174	—	16	P,L	FN
Dual Differential 2:1 Multiplexer (3.3V)	ECL	MC100LVEL56	MC100EL56	20		DW
Dual Multiplexer With Latch	ECL	MC10134	—	16	P,L	FN
Dual Multiplexer With Latch and Common Reset	ECL	MC10132	—	16	P,L	FN
Low Voltage 16:1 Multiplexer	ECL	MC100LVE164	—	32		FA
Quad 2–Input Multiplexer With Latch	ECL	MC10H173	—	16	P,L	FN
Quad 2–Channel Analog Multiplexer/Demultiplexer	CMOS	MC14551B	—	16	P	D
Quad 2–Input Data Selector/Multiplexer	CMOS	MC54HC158	MC74HC158	16	N,J	D
Quad 2–Input Data Selector/Multiplexer With 3–State Outputs	CMOS	MC74HC257	—	16	N	D
Quad 2–Input Data Selector/Multiplexer With LSTTL Compatible Inputs	CMOS	MC74HCT157A	—	16	N	D
Quad 2–Input Data Selectors/Multiplexers	CMOS	MC54HC157A	MC74HC157A	16	N,J	D,DT
Quad 2–Input Multiplexer	TTL	MC74F157A	—	16	N	D
	TTL	MC74F158A	—	16	N	D
	TTL	SN54LS157	SN74LS157	16	N,J	D
	TTL	SN54LS158	SN74LS158	16	N,J	D
Quad 2–Input Multiplexer (Inverting)	ECL	MC10159	—	16	P,L	FN
Quad 2–Input Multiplexer (Non–Inverting)	ECL	MC10158	—	16	P,L	FN

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
MULTIPLEXER/DATA SELECTORS						
Quad 2–Input Multiplexer Inverting With 3–State Outputs	CMOS	MC74AC258	—	16	N	DW
	CMOS	MC74ACT258	—	16	N	DW
Quad 2–Input Multiplexer Non–Inverting With 3–State Outputs	CMOS	MC74ACT257	—	16	N	D
	CMOS	MC74AC257	—	16	N	D
Quad 2–Input Multiplexer With 3–State Outputs	TTL	SN54LS257B	SN74LS257B	16	N,J	D
Quad 2–Input Multiplexer With Storage	TTL	SN54LS298	SN74LS298	16	N,J	D
Quad 2–Input Multiplexer, Inverting	CMOS	MC74AC158	—	16	N	D
	CMOS	MC74ACT158	—	16	N	D
Quad 2–Input Multiplexer, Inverting Output	ECL	MC10H159	—	16	P,L	FN
Quad 2–Input Multiplexer, Inverting, With 3–State Outputs	TTL	SN54LS258B	SN74LS258B	16	N,J	D
Quad 2–Input Multiplexer, Non–Inverting	CMOS	MC74AC157	—	16	N	D
	CMOS	MC74ACT157	—	16	N	D
Quad 2–Input Multiplexer, Non–Inverting Output	ECL	MC10H158	—	16	P,L	FN
Quad 2–Input Multiplexer, With 3–State Outputs	TTL	MC74F257A	—	16	N	D
	TTL	MC74F258A	—	16	N	D
Quad 2–Input Multiplexer/Latch	ECL	MC10173	—	16	P,L	FN
Quad 2–Port Register	TTL	MC74F398	—	20	N	DW
	TTL	MC74F399	—	16	N	D
	TTL	SN54LS398	SN74LS398	20	N,J	DW
	TTL	SN54LS399	SN74LS399	16	N,J	D
Quad 2:1 Mux, Individual–Select	ECL	MC10E157	MC100E157	28		FN
Quad Analog Switch/Multiplexer	CMOS	MC14016B	—	14	P,L	D
	CMOS	MC14066B	—	14	P,L	D
Quad Analog Switch/Multiplexer/Demultiplexer	CMOS	MC54HC4016	MC74HC4016	14	N,J	D
	CMOS	MC54HC4066	MC74HC4066	14	N,J	D,DT
Quad Analog Switch/Multiplexer/Demultiplexer With Separate Analog/Digital Power Supplies	CMOS	MC74HC4316	—	16	N	D
Triple 2–Channel Analog Multiplexer/Demultiplexer	CMOS	MC54HC4053	MC74HC4053	16	N,J	D, DW
	CMOS	MC14053B	—	16	P,L	D
Triple 2–Channel Analog Multiplexer/Demultiplexer With Address Latch	CMOS	MC54HC4353	MC74HC4353	20	N,J	DW
Triple 2:1 Multiplexer	ECL	MC100EL59	—	20		DW
Triple 2:1 Multiplexer (3.3V)	ECL	MC100LVEL59	—	20		DW
Triple Differential 2:1 Multiplexer	ECL	MC100E457	—	28		FN
	ECL	MC10E457	—	28		FN
MULTIVIBRATORS						
130MHz Voltage Controlled Multivibrator	ECL	MC12101	—	20	P	FN
200 MHz Voltage Controlled Multivibrator	ECL	MC12100	—	20	P	FN
Dual Monostable Multivibrator	HTL	MC667	—	14	P,L	
	CMOS	MC14528B	—	16	P,L	D
Dual Monstable Multivibrators With Schmitt Trigger Inputs	TTL	SN54LS221	SN74LS221	16	N,J	D
Dual Precision Monostable Multivibrator Retriggerable, Resettable)	CMOS	MC54HC4538A	MC74HC4538A	16	N,J	D
Dual Precision Monostable Multivibrator	CMOS	MC14538B	—	16	P,L	D, DW
Dual Voltage–Controlled Multivibrator	ECL	MC4024	—	14	P,L	
Monostable Multivibrator	DTL	MC951	—	14	P,L	
	ECL	MC10198	—	16	P,L	FN
Retriggerable Monostable Multivibrators	TTL	SN54LS122	SN74LS122	14	N,J	D
	TTL	SN54LS123	SN74LS123	14	N,J	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
MULTIVIBRATORS						
Voltage Controlled Multivibrator	ECL	MC1658	—	16	P,L	D,FN
OSCILLATORS						
7–Stage Binary Ripple Counter	CMOS	MC74HC4024	—	14	N	D
Crystal Oscillator	ECL	MC12061	—	16	P,L	
Dual Voltage–Controlled Multivibrator	ECL	MC4324	—	14	P,L	
Low Power Voltage Controlled Oscillator	ECL	MC12148	—	8		D,SD
Voltage Controlled Oscillator	ECL	MC1648	—	14	P,L	D,FN
OSCILLATOR/TIMERS						
24–Stage Frequency Divider	CMOS	MC14521B	—	16	P,L	D
Programmable Oscillator Timer	CMOS	MC14541B	—	14	P,L	D
Programmable Timer	CMOS	MC14536B	—	16	P,L	DW
Quad Precision Timer/Driver	CMOS	MC14415	—	16	P,L	DW
PARITY CHECKERS						
12–Bit Parity Generator/Checker	ECL	MC10H160	—	16	P,L	FN
	ECL	MC10160	—	16	P,L	FN
12–Bit Parity Generator/Checker, Register–Shiftable, Diff Output	ECL	MC10E160	MC100E160	28		FN
12–Bit Parity Tree	CMOS	MC14531B	—	16	P	D
9 + 2–Bit Parity Generator–Checker	ECL	MC10170	—	16	P,L	FN
9–Bit Odd/Even Parity Generator/Checker	CMOS	MC74HC280	—	14	N	D
	TTL	SN54LS280	SN74LS280	14	N,J	D
9–Bit Parity Generator/Checker	TTL	MC74F280	—	14	N	D
Error Detection and Correction Circuit	ECL	MC10E193	MC100E193	28		FN
PHASE–LOCKED LOOP						
Phase–Locked Loop	CMOS	MC14046B	—	16	P,L	DW
PRESCALERS						
1.1GHz ÷10/20/40/80 Prescaler	ECL	MC12080	—	8	P	D
1.1GHz ÷126/128, ÷254/256 Low Power Dual Modulus Prescaler	ECL	MC12058	—	8		D,SD
1.1GHz ÷127/128, ÷255/256 Low Power Dual Modulus Prescaler	ECL	MC12038A	—	8	P	D
1.1GHz ÷8/9, ÷16/17 Dual Modulus Prescaler	ECL	MC12026A	—	8	P	D
	ECL	MC12026B	—	8	P	D
1.1GHz ÷2 Low Power Prescaler With Stand–By Mode	ECL	MC12083	—	8	P	D
1.1GHz ÷2/4/8 Low Power Prescaler With Stand–By Mode	ECL	MC12093	—	8	P	D,SD
1.1GHz ÷256 Prescaler	ECL	MC12074	—	8	P	D
1.1GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	ECL	MC12028A	—	8	P	D
1.1GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	ECL	MC12028B	—	8	P	D
1.1GHz ÷64 Prescaler	ECL	MC12073	—	8	P	D
1.1GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	ECL	MC12022A	—	8	P	D
	ECL	MC12022B	—	8	P	D
	ECL	MC12022SLA	—	8	P	D
	ECL	MC12022SLB	—	8	P	D
	ECL	MC12022TSA	—	8	P	D
	ECL	MC12022TSB	—	8	P	D
1.1GHz ÷64/65, ÷128/129 Dual Modulus Prescaler With Stand–By Mode	ECL	MC12036A	—	8	P	D
	ECL	MC12036B	—	8	P	D
1.1GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	ECL	MC12022LVA	—	8	P	D
	ECL	MC12022LVB	—	8	P	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
PRESCALERS						
1.1GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	ECL	MC12022TVA	—	8	P	D
	ECL	MC12022TVB	—	8	P	D
1.1GHz ÷64/65, ÷128/129 Super Low Power Dual Modulus Prescaler	ECL	MC12052A	—	8		D,SD
1.1GHz ÷64/65, ÷128/129 Super Low Power Dual Modulus Prescaler With Stand–By Mode	ECL	MC12053A	—	8		D,SD
1.3GHz ÷64 Prescaler	ECL	MC12075	—	8	P	D
1.3GHz ÷256 Prescaler	ECL	MC12076	—	8	P	D
	ECL	MC12078	—	8	P	D
2.0GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	ECL	MC12034A	—	8	P	D
	ECL	MC12034B	—	8	P	D
2.0GHz ÷32/33, ÷64/65 Low Voltage Dual Modulus Prescaler	ECL	MC12033A	—	8	P	D
	ECL	MC12033B	—	8	P	D
2.0GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	ECL	MC12032A	—	8	P	D
	ECL	MC12032B	—	8	P	D
2.0GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	ECL	MC12031A	—	8	P	D
	ECL	MC12031B	—	8	P	D
2.0GHz ÷64/65, ÷128/129 Super Low Power Dual Modulus Prescaler	ECL	MC12054A	—	8		D,SD
2.5GHz ÷2, ÷4 Low Power Prescaler With Satnd–By Mode	ECL	MC12095	—	8		D,SD
2.8GHz ÷64/128/256 Prescaler	ECL	MC12079	—	8	P	D
	ECL	MC12089	—	8	P	D
225MHz ÷20/21 Dual Modulus Prescaler	ECL	MC12019	—	8	P,L	D
225MHz ÷32/33 Dual Modulus Prescaler	ECL	MC12015	—	8	P,L	D
225MHz ÷40/41 Dual Modulus Prescaler	ECL	MC12016	—	8	P,L	D
225MHz ÷64 Prescaler	ECL	MC12023	—	8	P	D
225MHz ÷64/65 Dual Modulus Prescaler	ECL	MC12017	—	8	P,L	D
480MHz ÷5/6 Dual Modulus Prescaler	ECL	MC12009	—	16	P,L	
520MHz ÷128/129 Dual Modulus Prescaler	ECL	MC12018	—	8	P,L	D
520MHz ÷64/65 Dual Modulus Prescaler	ECL	MC12025	—	8	P	D
550MHz ÷10/11 Dual Modulus Prescaler	ECL	MC12013	—	16	P,L	
550MHz ÷8/9 Dual Modulus Prescaler	ECL	MC12011	—	16	P,L	
750MHz ÷2 UHF Prescaler	ECL	MC12090	—	16	P,L	
PROGRAMMABLE DELAY CHIPS						
Programmable Delay Chip (Dig 80ps Anal. 1.6 Ps/mv)	ECL	MC10E196	MC100E196	28		FN
Programmable Delay Chip (Digitally Selectable 20ps Res)	ECL	MC10E195	MC100E195	28		FN
PROMs						
1024–Bit Programmable Read Only Memory	ECL	MCM10149*25	—	16	L	
32 X 8–Bit Programmable Read Only Memory	ECL	MCM10139	—	16	L	
RAMs						
1024 X 1–Bit Random Access Memory	ECL	MCM10146	—	16	L	
256 X 1–Bit Random Access Memory	ECL	MCM10152	—	16	L	
RECEIVERS						
Differential Receiver	ECL	MC10EL16	MC100EL16	8		D
High Speed Triple Line Receiver	ECL	MC10216	—	16	P,L	FN
Low–Voltage Quad Differential Line Receiver	ECL	MC100LVEL17	MC100EL17	20		DW
Quad Bus Receiver	ECL	MC10129	—	16	L	

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
RECEIVERS						
Quad Line Receiver	ECL	MC10H115	—	16	P,L	FN
	ECL	MC10115	—	16	P,L	FN
	ECL	MC1692	—	16	L	
Quint Differential Line Receiver	ECL	MC10E116	MC100E116	28		FN
	ECL	MC10E416	MC100E416	28		FN
Triple Line Receiver	ECL	MC10H116	—	16	P,L	D,FN
	ECL	MC10114	—	16	P,L	FN
	ECL	MC10116	—	16	P,L	FN
REGISTERS						
4 X 4 Multiport Register	CMOS	MC14580B	—	24	P,L	D
Hex Parallel D Register With Enable	TTL	MC74F378	—	16	N	D
REGISTER FILES						
16 X 4–Bit Register File (RAM)	ECL	MC10H145	—	16	P,L	FN
4 X 4 Register File Open Collector	TTL	SN54LS170	SN74LS170	16	N,J	D
4 X 4 Register File With 3–State Outputs	TTL	SN54LS670	SN74LS670	16	N,J	D
64–Bit Register File (RAM)	ECL	MCM10145	—	16	L	
8 X 2 Multiport Register File (RAM)	ECL	MCM10143	—	24	L	
SCHMITT TRIGGERS						
Dual 4–Input NAND Schmitt Trigger	TTL	MC74F13	—	14	N	D
	TTL	SN54LS13	SN74LS13	14	N,J	D
Dual Schmitt Trigger	CMOS	MC14583B	—	16	P	D
Hex Inverter Schmitt Trigger	CMOS	MC74AC14	—	14	N	D
	CMOS	MC74ACT14	—	14	N	D
	TTL	MC74F14	—	14	N	D
	TTL	SN54LS14	SN74LS14	14	N,J	D
Hex Schmitt Trigger	CMOS	MC14106B	—	14	P,L	D
	CMOS	MC14584B	—	14	P,L	D
Hex Schmitt Trigger Inverter	CMOS	MC54HC14A	MC74HC14A	14	N,J	D,DT
	CMOS	MC54HCT14A	MC74HCT14A	14	N,J	D
Quad 2–Input NAND Gate With Schmitt Trigger Inputs	CMOS	MC54HC132A	MC74HC132A	14	N,J	D
Quad 2–Input NAND Schmitt Trigger	CMOS	MC74AC132	—	14	N	D
	CMOS	MC74ACT132	—	14	N	D
	TTL	MC74F132	—	14	N	D
	CMOS	MC14093B	—	14	P,L	D
Quad 2–Input Schmitt Trigger NAND Gate	TTL	SN54LS132	SN74LS132	14	N,J	D
SCSI BUS TERMINATORS						
18–Bit Active SCSI Bus Terminator (*Also Available in 32–Pin QFP Package)	CMOS	MCCS142235	—	24,32		DW,*FA
9–Bit Switchable SCSI Bus Term (110Ω: Active)	CMOS	MCCS142234	—	16		D
9–Bit Switchable SCSI Bus Term (220Ω & 330Ω: Passive)	CMOS	MCCS142233	—	20		FN
9–Bit Switchable Active SCSI–2 Bus Term (110Ω) with Volt Reg	CMOS	MCCS142237	—	16,20		DW, DT
SHIFT REGISTERS						
1–to–64–Bit Variable Length Shift Register	CMOS	MC14557B	—	16	P,L	DW
128–Bit Static Shift Register	CMOS	MC14562B	—	14	P,L	
18–Bit Static Shift Register	CMOS	MC14006B	—	14	P,L	D
3–Bit Scannable Registered Address Driver, ECL	ECL	MC10E212	MC100E212	28		FN

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
SHIFT REGISTERS						
4–Bit Bidirectional Universal Shift Register	CMOS	MC74AC194	—	16	N	D
	CMOS	MC74ACT194	—	16	N	D
	TTL	MC74F194	—	16	N	D
	CMOS	MC74HC194	—	16	N	
	TTL	SN54LS194A	SN74LS194A	16	N,J	D
4–Bit Shift Register	TTL	MC74F195	—	16	N	D
	TTL	SN54LS95B	SN74LS95B	14	N,J	D
	CMOS	MC14035B	—	16	P,L	D
4–Bit Shift Register With 3–State Outputs	TTL	SN74LS395	—	16	N,J	D
4–Bit Shifter With 3–State	CMOS	MC74AC350	—	16	N	D
	CMOS	MC74ACT350	—	16	N	D
4–Bit Shifter, With 3–State Outputs	TTL	MC74F350	—	16	N	D
4–Bit Universal Shift Register	CMOS	MC74HC195	—	16	N	
	ECL	MC10H141	—	16	P,L	FN
	ECL	MC10141	—	16	P,L	FN
	CMOS	MC14194B	—	16	P,L	D
8–Bit Bidirectional Universal Shift Register With parallel I/O	CMOS	MC74HC299	—	20	N	DW
8–Bit Parallel–to–Serial Shift Register	TTL	SN54LS165	SN74LS165	16	N,J	D
8–Bit Scannable Register	ECL	MC10E241	MC100E241	28		FN
8–Bit Serial In–Serial Out Shift Register	TTL	MC74F164	—	14	N	D
8–Bit Serial or Parallel–Input/Serial–Output Shift Register	CMOS	MC54HC165	MC74HC165	16	N,J	D
8–Bit Serial or Parallel–Input/Serial–Output Shift Register With 3–State Outputs	CMOS	MC54HC589	MC74HC589	16	N,J	D
8–Bit Serial or Parallel–Input/Serial–Output Shift Register With Input Latch	CMOS	MC54HC597	MC74HC597	16	N,J	D
8–Bit Serial–In/Parallel–Out Shift Register	TTL	SN54LS164	SN74LS164	14	N,J	D
8–Bit Serial–Input/Parallel–Output Shift Register	CMOS	MC54HC164	MC74HC164	14	N,J	D
8–Bit Serial–Input/Serial or Parallel–Output Shift Register With Latched 3–State Outputs	CMOS	MC54HC595A	MC74HC595A	16	N,J	D,DT
8–Bit Shift Register	ECL	MC10E141	MC100E141	28		FN
	TTL	SN54LS166	SN74LS166	16	N,J	D
8–Bit Shift Registers With Sign Extend	TTL	SN54LS322A	SN74LS322A	20	N,J	DW
8–Bit Shift/Storage Register With 3–State Outputs	TTL	SN54LS299	SN74LS299	20	N,J	DW
	TTL	SN54LS323	SN74LS323	20	N,J	DW
8–Bit Static Shift Register	CMOS	MC14014B	—	16	P,L	D
	CMOS	MC14021B	—	16	P,L	D
8–Input Shift/Storage Register W/Synchronous Reset and Common I/O Pins	TTL	MC74F323	—	20	N	DW
8–Input Universal Shift/Storage Register With Common Parallel I/O Pins: With 3–State Outputs	CMOS	MC74AC299	—	20	N	DW
	CMOS	MC74ACT299	—	20	N	DW
8–Input Universal Shift/Storage Register With Syn Reset/Common Parallel I/O Pins: With 3–State Outputs	CMOS	MC74AC323	—	20	N	DW
	CMOS	MC74ACT323	—	20	N	DW
8–Input Universal Shift/Storage Register, W/Common Parallel I/O Pins	TTL	MC74F299	—	20	N	DW
8–Stage Shift/Store Register With 3–State Outputs	CMOS	MC14094B	—	16	P,L	D
9–Bit Shift Register, 700MHz, With Asynchronous Master Reset	ECL	MC10E142	MC100E142	28		FN
Dual 5–Bit Shift Register	CMOS	MC14015B	—	16	P,L	D
Dual 64–Bit Static Shift Register	CMOS	MC14517B	—	16	P	DW

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
SHIFT REGISTERS						
Successive Approximation Register	CMOS	MC14549B	—	16	P,L	DW
	CMOS	MC14559B	—	16	P,L	DW
Universal 4–Bit Shift Register	TTL	SN54LS195A	SN74LS195A	16	N,J	D
SYNTHESIZERS						
1.1GHz Serial Input Synthesizer With ÷64/65, ÷128/129 Prescaler	ECL	MC12202	—	16,20		D,M, DT
2.0GHz Serial Input Synthesizer With ÷64/65, ÷128/129 Prescaler	ECL	MC12206	—	16,20		D,DT
2.5GHz Serial Input Synthesizer With ÷32/33, ÷64/65 Prescaler	ECL	MC12210	—	16,20		D,DT
2.7GHz Frequency Synthesizer	ECL	MC12179	—	8		D
TRANSCEIVERS						
4–Bit Differential ECL Bus/TTL Bus Transceiver	ECL	MC10H680	MC100H680	28		FN
ECL/TTL Inverting Bidirectional Transceivers With Latch (4–Bit)	ECL	MC10804	—	16	L	
ECL/TTL Inverting Bidirectional Transceivers With Latch (5–Bit)	ECL	MC10805	—	20	L	
Hex ECL/TTL Transceiver With Latches	ECL	MC10H681	MC100H681	28		FN
Low–Voltage CMOS Octal Transceiver, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX245	—	20		M,DW, DT
Low–Voltage Quiet CMOS Octal Transceiver, 3–State, Non–Inverting	CMOS	MC74LVQ245	—	20		M,DW, SD,DT
Low–Voltage Quiet CMOS Octal Transceiver/Registered Transceiver	CMOS	MC74LVQ646	—	24		DW, SD,DT
Low–Voltage Quiet CMOS Octal Transceiver/Registered Transceiver	CMOS	MC74LVQ652	—	24		DW, SD,DT
Octal Bus Transceiver/Inverting With Open Collector	TTL	SN54LS642	SN74LS642	20	N,J	DW
Octal Bus Transceiver/Non–Inverting With Open Collector	TTL	SN54LS641	SN74LS641	20	N,J	DW
Quad Futurebus Backplane Transceiver, With 3–State Outputs and Open Collector	TTL	MC74F3893A	—	20		FN
TRANSLATORS						
9–Bit ECL/TTL Translator	ECL	MC10H601	MC100H601	28		FN
9–Bit Latch ECL/TTL Translator	ECL	MC10H603	MC100H603	28		FN
9–Bit Latch TTL/ECL Translator	ECL	MC10H602	MC100H602	28		FN
9–Bit TTL/ECL Translator	ECL	MC10H600	MC100H600	28		FN
Differential ECL/TTL Translator	ECL	MC10ELT25	MC100ELT25	8		D
Differential PECL/TTL Translator	ECL	MC10ELT21	MC100ELT21	8		D
Dual Differential PECL/TTL Translator	ECL	MC100ELT23	—	8		D
Dual TTL/Differential PECL Translator	ECL	MC10ELT22	MC100ELT22	8		D
ECL/TTL Translator (Single P.S. @+ 5.0V)	ECL	MC10H350	—	16	P,L	FN
Hex ECL/MST Translator	ECL	MC10191	—	16	P,L	
Hex TTL OR CMOS/CMOS Hex Level Shifter	CMOS	MC14504B	—	16	P,L	D
Quad CMOS/ECL Translator (Single P.S. @+ 5.0V)	ECL	MC10H352	—	20	P,L	FN
Quad MECL/TTL Translator	ECL	MC10H125	—	16	P,L	FN
	ECL	MC10125	—	16	P,L	FN
Quad MST/ECL Translator	ECL	MC10190	—	16	P	
Quad TTL/ECL Translator (ECL Strobe)	ECL	MC10H424	—	16	P,L	FN
Quad TTL/MECL Translator	ECL	MC10124	—	16	P,L	FN
Quad TTL/MECL Translator, With TTL Strobe Input	ECL	MC10H124	—	16	P,L	FN
Quad TTL/NMOS–to–PECL Translator (Single P.S. @+ 5.0V)	ECL	MC10H351	—	20	P,L	FN
Registered Hex ECL/TTL Translator	ECL	MC10H605	MC100H605	28		FN
Registered Hex PECL/TTL Translator	ECL	MC10H607	MC100H607	28		FN
Registered Hex TTL/ECL Translator	ECL	MC10H604	MC100H604	28		FN

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
TRANSLATORS						
Registered Hex TTL/PECL Translator	ECL	MC10H606	MC100H606	28		FN
Triple MECL/NMOS Translator	ECL	MC10177	—	16	L	
Triple ECL to PECL Translator	ECL	MC100LVEL90	MC100EL90	20		DW
Triple PECL to LVPECL Translator	ECL	MC100LVEL92	—	20		DW
TTL/Differential ECL Translator	ECL	MC10ELT24	MC100ELT24	8		D
TTL/Differential PECL Translator	ECL	MC10ELT20	MC100ELT20	8		D
TTL to Differential PECL/Differential PECL to TTL Translator	ECL	MC10ELT28	MC100ELT28	8		D
VCO						
Phase–Locked–Loop With VCO	CMOS	MC74HC4046A	—	16	N	D
Low Power Voltage Controlled Oscillator Buffer	CMOS	MC12147	—	8		D,SD
Low Power Voltage Controlled Oscillator Buffer	CMOS	MC12149	—	8		D,SD

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Ordering Information
Device Nomenclatures

LS – Low Power Schottky

SN VV WW XXXX Y

Standard Prefix — SN

Temperature Range — VV
- 74 Series (0 to +70°C)
- 54 Series (–55 to +125°C)

Family — WW
- LS = Low Power Schottky

Function Type — XXXX

Package Type — Y
- N for Plastic (74 Series Only)
- J for Ceramic
- D for 150 mil Plastic SOIC (74 Series Only)
- DW for 300 mil Plastic SOIC (74 Series Only)

FAST

MC VV W XXXX Y

Motorola Circuit Identifier — MC

Temperature Range — VV
- 74 Series (0 to +70°C)

Family — W
- F = FAST

Function Type — XXXX

Package Type — Y
- N for Plastic (74 Series Only)
- D for 150 mil Plastic SOIC (74 Series Only)
- DW for 300 mil Plastic SOIC (74 Series Only)

MECL 10K, MECL 10H/100H

MC WWW XXX YY

Motorola Circuit Identifier — MC

Temperature Range — WWW
- 10 = 10K (–30 to +85°C)
- 10H = 10H (0 to +75°C)
- 100H = 100K Compatible (0 to +85°C)

Function Type — XXX

Package Type — YY
- P for Plastic
- L for Ceramic
- FN for PLCC

ECLinPS, ECLinPS Lite

MC WWW XXX YYY ZZ

Motorola Circuit Identifier (MC)
- MC = Fully Qualified Circuit
- XC = Non Reliability Qualified

Compatibility Identifier (WWW)
- 10 = 10H Compatible (0 to +85°C)
- 100 = 100K Compatible (0 to +85°C)

Package Type (ZZ)
- FN = PLCC
- D = Plastic SOIC
- L = Ceramic DIP
- P = Plastic DIP

Function Type (YYY)
- YYY = 3-Digits for ECLinPS
- YY= 2-Digits for ECLinPS Lite

ECLinPS Family Identifier (XXX)
- E = ECLinPS
- EL = ECLinPS Lite
- ELT = ECLinPS Lite Translator
- LVE = Low Voltage ECLinPS
- LVEL = Low Voltage ECLinPS Lite

Metal Gate 14000 Series CMOS

MC 14XXX YY ZZ

Motorola Circuit Identifier (MC)

Function Type (14XXX)

Identifier (per JEDEC Standard) (YY)
- B (or Blank)= Buffered Outputs
- UB = Unbuffered Outputs

Package and Temperature Range (ZZ)
- CL for Ceramic –55 to +125°C
- CP for Plastic –55 to +125°C
- D/DW for Small Outline Package (Plastic) –55 to +125°C

High–Speed CMOS

MC VV WWW XXXX Y

Motorola Circuit Identifier (MC)

Temperature Range (VV)
- 74 Series (–55 to +125°C)
- 54 Series (–55 to +125°C)

High–Speed CMOS Specification Identifier (WWW)
- HC = Buffered High–Speed CMOS
- HCU = Unbuffered High–Speed CMOS*
- HCT = High–Speed CMOS TTL Compatible

Package Type (Y)
- N for Plastic (74 Series Only)
- J for Ceramic (54 Series Only)
- D for 150 mil Plastic SOIC (74 Series Only)
- DW for 300 mil Plastic SOIC (74 Series Only)

Function Type (XXXX)
- XX(X) Same Function and Pin Configuration as LSTTL
- 4XXX Same Function and Pin Configuration as CMOS 14000
- 7XX(X) Variation of LSTTL or CMOS 14000 Device

***Not Available On All Devices**

FACT

MC WWWWW XXX YY

Motorola Circuit Identifier (MC)

Temperature Range Family (WWWWW)
- 74AC = FACT (–40 to +85°C)
- 74ACT = TTL Compatible (–40 to +85°C)

Package Type (YY)
- N for Plastic
- D for Narrow SOIC
- DW for Wide SOIC

Function Type (XXX)

Other Logic Circuits

MC/MCCS WWWWWW X YY ZZ

Motorola Circuit Identifier
- MC = Standard Circuit Identifier
- MCCS = Circuit Chip–Set Identifier

Function Type

Option Suffix Indicator

Package Type
- N for Plastic
- D for Narrow SOIC
- FN for PLCC
- FJ for CLCC

Option Type

MECL III/HTL/DTL

MC XXXX Y

Motorola Circuit Identifier

Package Type
- P for Plastic
- L for Ceramic
- D for Narrow SOIC
- FN for PLCC

Function Type

LCX Products

MC 74 LCX YYYY ZZ

Motorola Circuit Identifier

Temperature Range
- 74 = –40 to +85°C

Family Identifier
- LCX = 5V–Tolerant Low–Voltage CMOS

Package Type
- D for Plastic Narrow JEDEC SOIC
- DW for Plastic Wide JEDEC SOIC
- M for Plastic EIAJ SOIC
- SD for Plastic SSOP
- DT for Plastic TSSOP

Function Type

LVQ Products

MC 74 LVQ YYYY ZZ

Motorola Circuit Identifier

Temperature Range
- 74 = –40 to +85°C

Family Identifier
- LVQ =Low–Voltage Quiet CMOS

Package Type
- D for Plastic Narrow JEDEC SOIC
- DW for Plastic Wide JEDEC SOIC
- M for Plastic EIAJ SOIC
- SD for Plastic SSOP
- DT for Plastic TSSOP

Function Type

Motorola Programmable Arrays (MPA)

MPA 1XXXX YY Z –I

MPA — **Motorola Programmable Array Circuit Identifier**

1XXXX — **Family Identifier**
- 1XXX = 1000 Series Programmable Array
- 17XXX = 17000 Series Serial EPROM

YY — **Package Types**
- P = 8–Pin DIP
- D = 8–Pin SOIC
- FN = 20–Pin PLCC
- FN = 84–Pin PLCC
- DD = 128–Pin PQFP
- DH = 160–Pin PQFP
- DK = 208–Pin PQFP
- HI = 181–Pin PGA
- KE = 224–Pin PGA
- HV = 299–Pin PGA

Z — **Speed Grade**
- Consult Factory

–I — **Temperature Range**
- Blank = 0 to +70°C
- –I = –40 to +85°C (Planned)

MPA Design System Configuration Numbering

MPA X / Y

MPA — **Motorola Programmable Array Circuit Identifier**

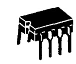
X — **Development System Identifier**
- E = Entry Series (Includes Full MPA1016/1036 Device Support)
- S = Standard Series (Includes All MPA1000 Family Support)

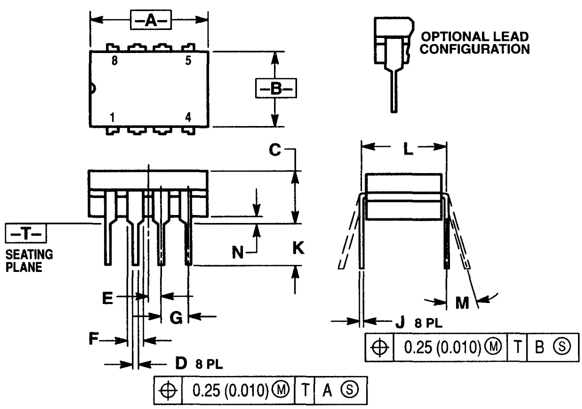
Y — **Temperature Range**
- P = PC
- W = Workstation

Case Outlines

8–Pin Packages

L SUFFIX
CERAMIC DIP PACKAGE
CASE 693–03
ISSUE C

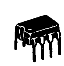


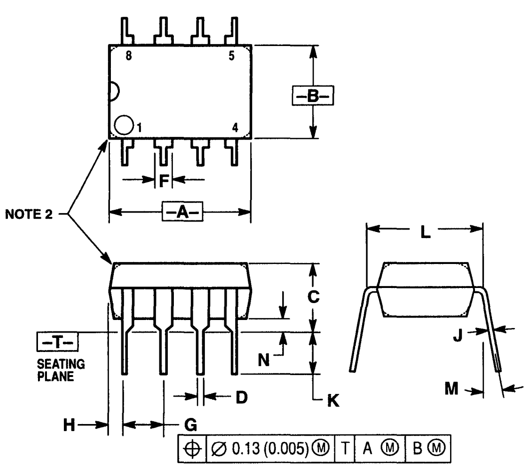


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS AT LEAD POSITIONS 1, 4, 5, AND 8.
5. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.390	0.430	9.91	10.92
B	0.245	0.275	6.22	6.98
C	0.170	0.200	4.32	5.08
D	0.016	0.020	0.41	0.51
E	0.050 BSC		1.27 BSC	
F	0.050	0.065	1.27	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.20	0.38
K	0.125	0.160	3.18	4.06
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

P SUFFIX
PLASTIC DIP PACKAGE
CASE 626–05
ISSUE K



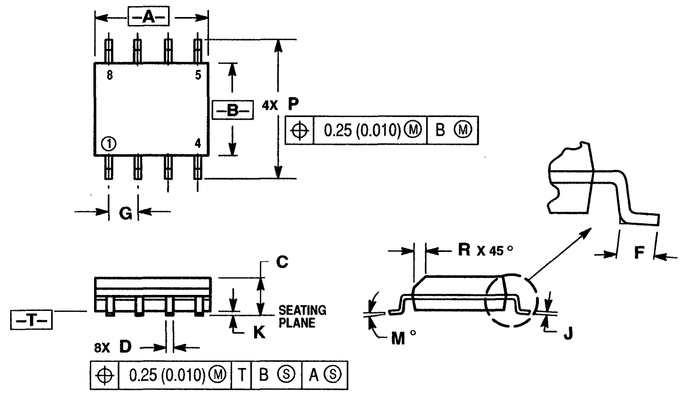


NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

8–Pin Packages

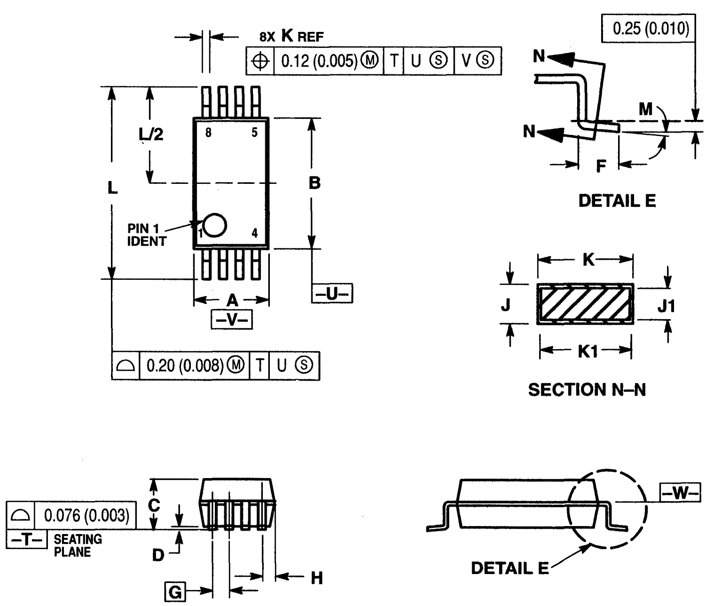
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–05
ISSUE N



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940–03
ISSUE B

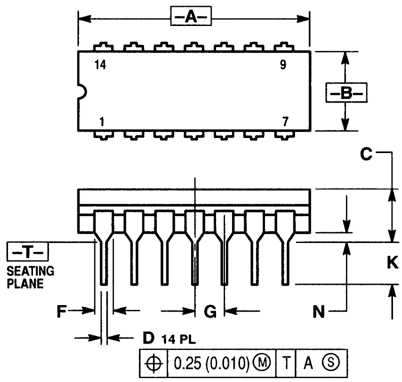


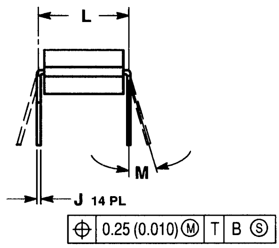
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.87	3.13	0.113	0.123
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.44	0.60	0.017	0.023
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

14–Pin Packages

L,J SUFFIX
CERAMIC DIP PACKAGE
CASE 632–08
ISSUE Y

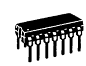


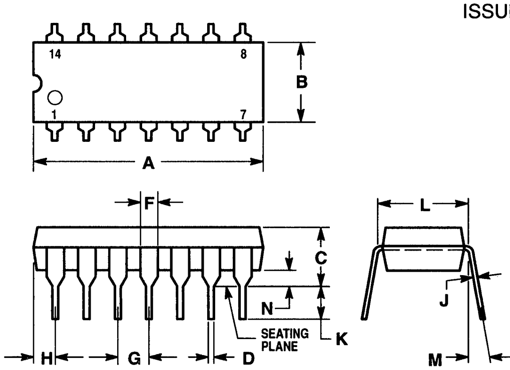


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P,N SUFFIX
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE L

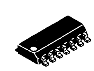


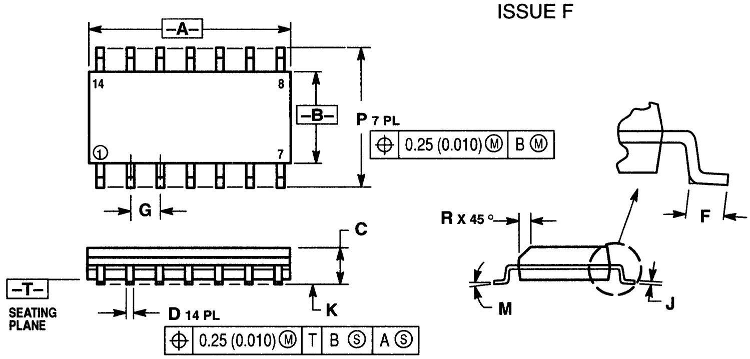


NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F



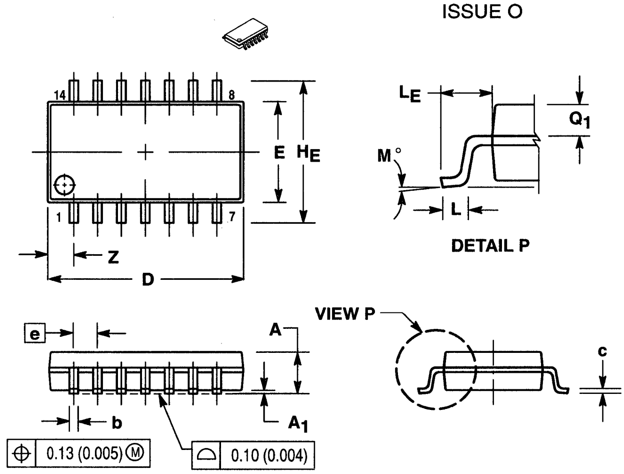


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

14–Pin Packages

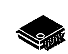
M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 965–01
ISSUE O

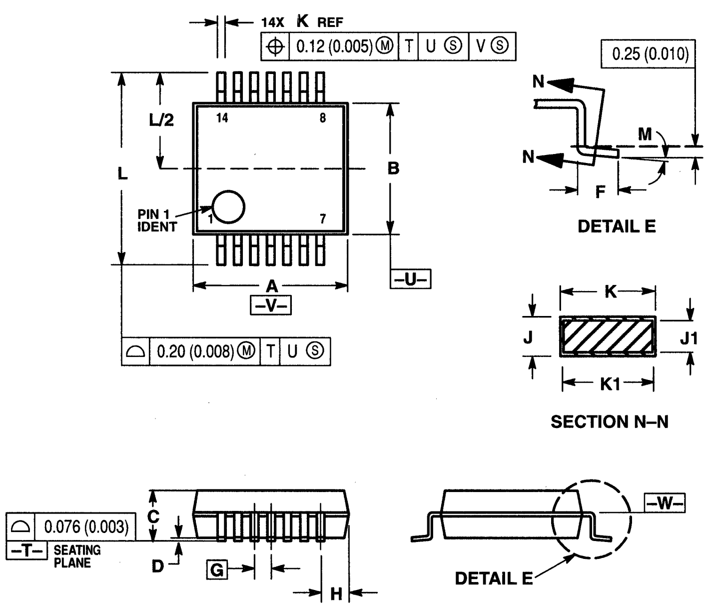


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	1.42	—	0.056

SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940A–03
ISSUE B



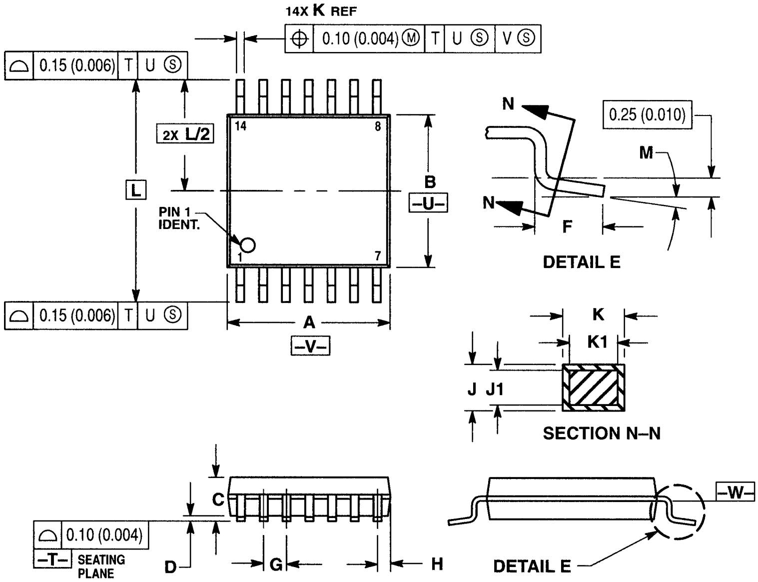


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.07	6.33	0.238	0.249
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	1.08	1.22	0.042	0.048
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

14–Pin Packages

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948G–01
ISSUE O

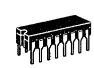


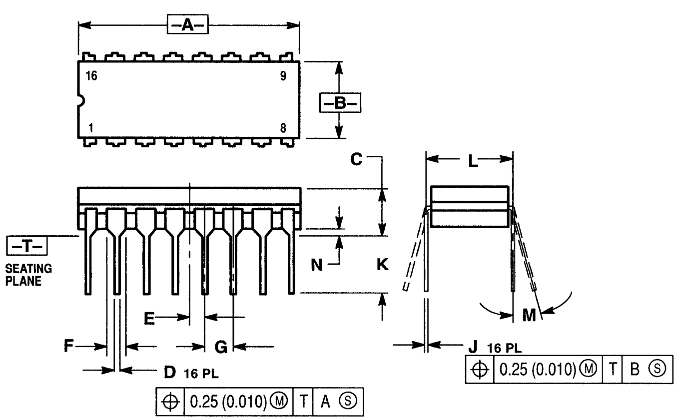
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

16–Pin Packages

L,J SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



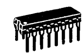


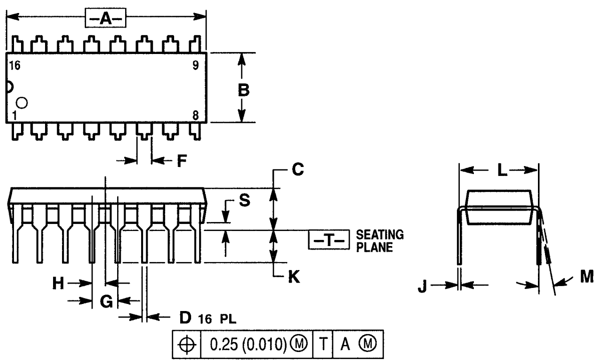
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

16–Pin Packages

P,N SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

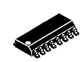


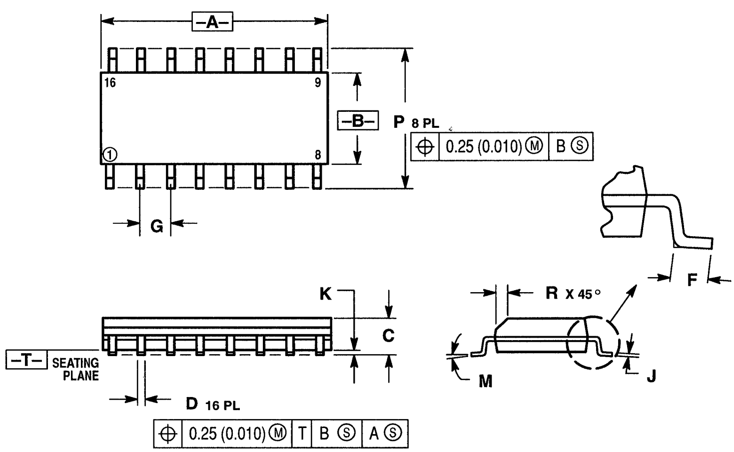


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



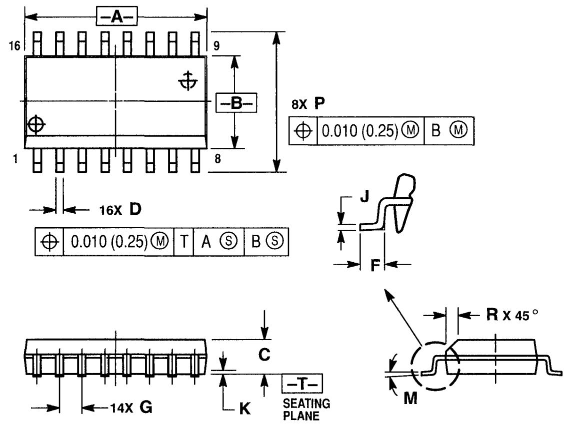


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

16–Pin Packages

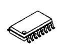
DW SUFFIX
PLASTIC WIDE SOIC PACKAGE
CASE 751G–02
ISSUE A

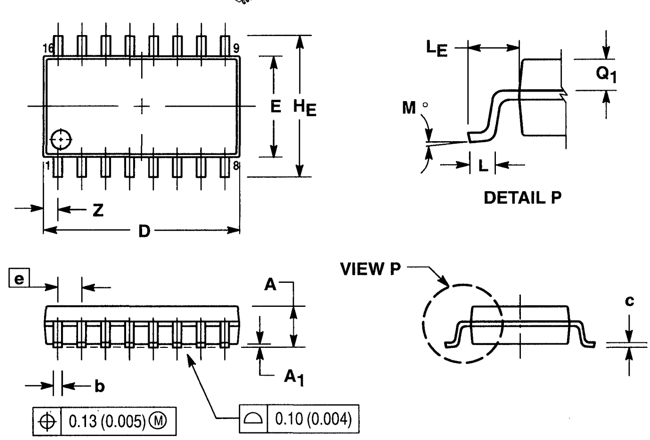


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSIOM D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 966–01
ISSUE O



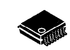


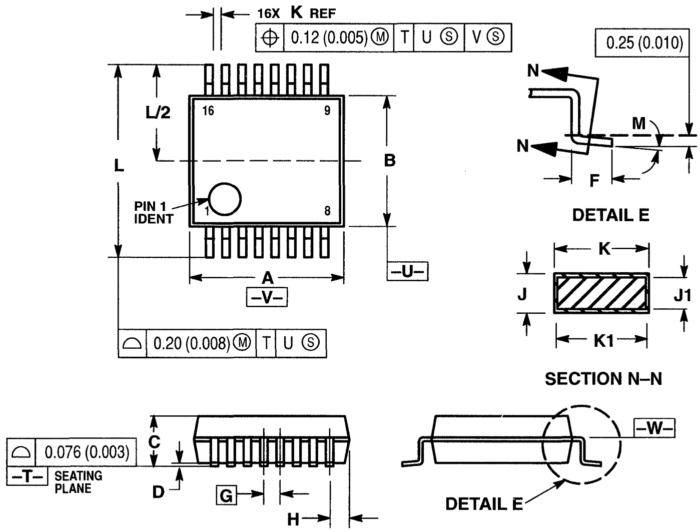
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q_1	0.70	0.90	0.028	0.035
Z	—	0.78	—	0.031

16–Pin Packages

SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940B–03
ISSUE B

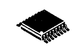


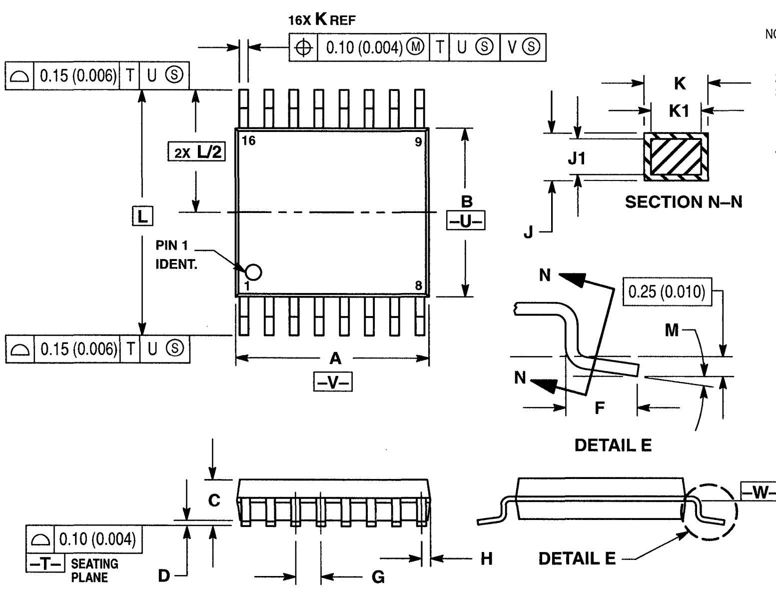


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.07	6.33	0.238	0.249
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.73	0.90	0.028	0.035
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F–01
ISSUE O



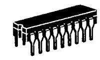


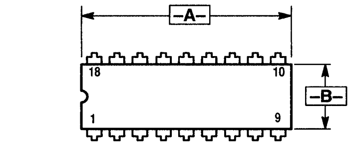
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

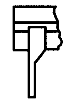
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

18–Pin Packages

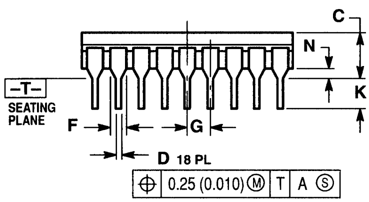
L,J SUFFIX
CERAMIC DIP PACKAGE
CASE 726–04
ISSUE G

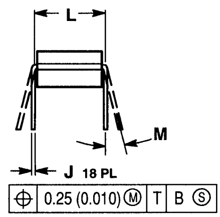






OPTIONAL LEAD
CONFIGURATION (1, 9, 10, 18)

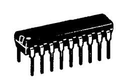


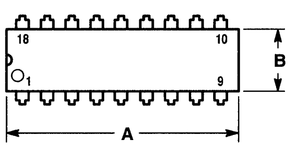


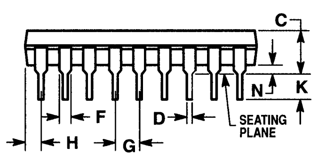
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

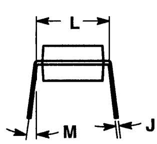
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.880	0.910	22.35	23.11
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.021	0.38	0.53
F	0.055	0.070	1.40	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.20	0.30
K	0.125	0.170	3.18	4.32
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

P,N SUFFIX
PLASTIC DIP PACKAGE
CASE 707–02
ISSUE C







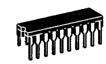


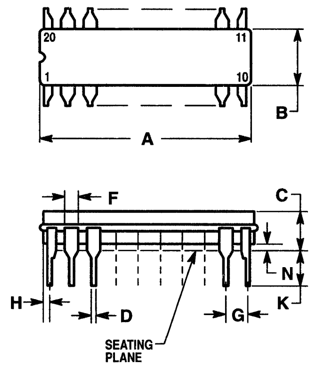
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

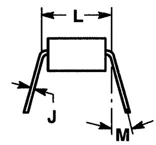
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

20–Pin Packages

L,J SUFFIX
CERAMIC DIP PACKAGE
CASE 732–03
ISSUE E



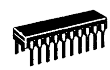


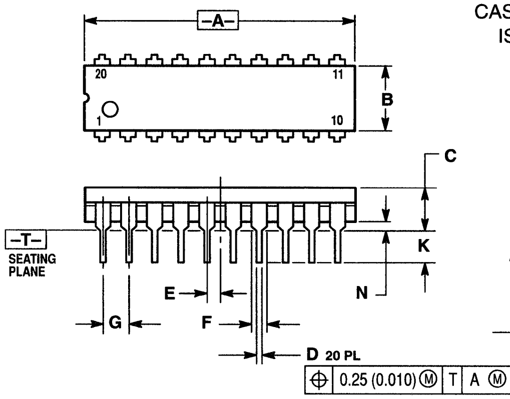


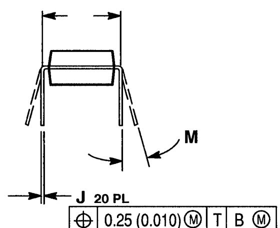
NOTES:
1. LEADS WITHIN 0.25 (0.010) DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS A AND B INCLUDE MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

P,N SUFFIX
PLASTICC DIP PACKAGE
CASE 738–03
ISSUE E



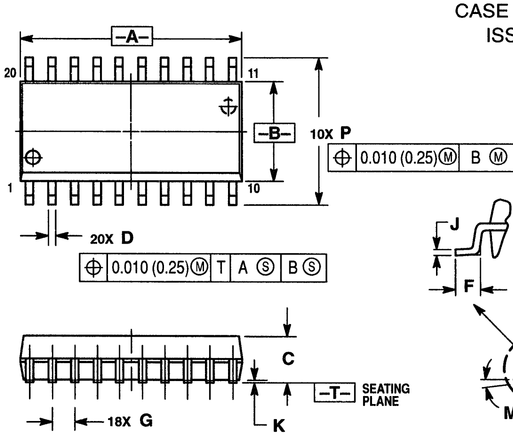


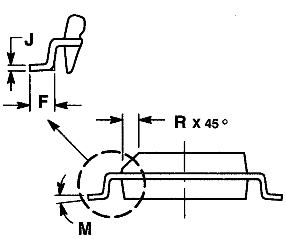


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04
ISSUE E



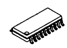


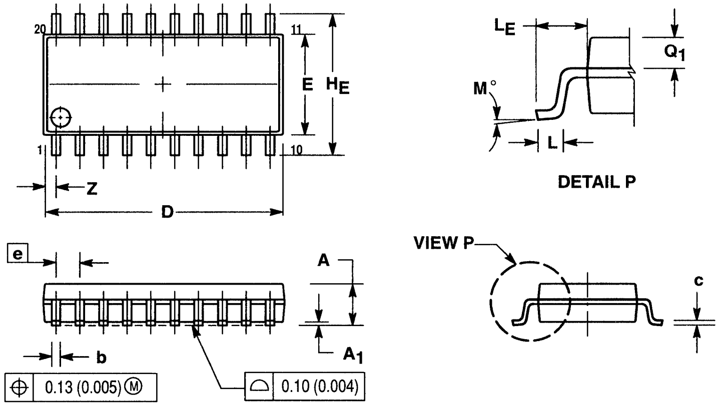
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

20–Pin Packages

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 967–01
ISSUE O

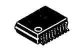


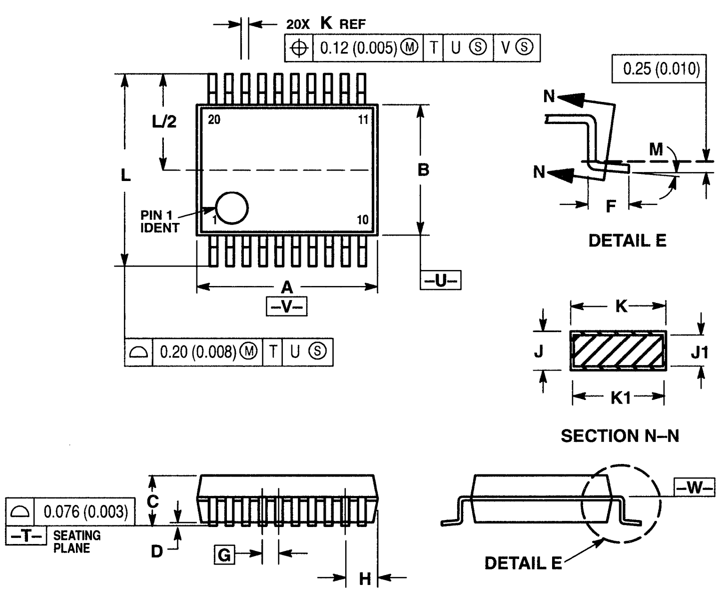


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	0.81	—	0.032

SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940C–03
ISSUE B



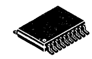


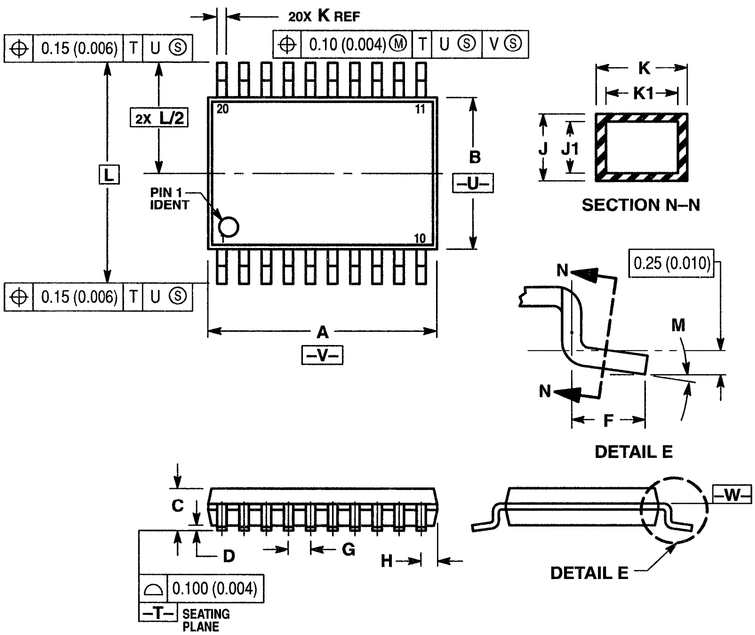
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.07	7.33	0.278	0.288
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.59	0.75	0.023	0.030
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

20–Pin Packages

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A



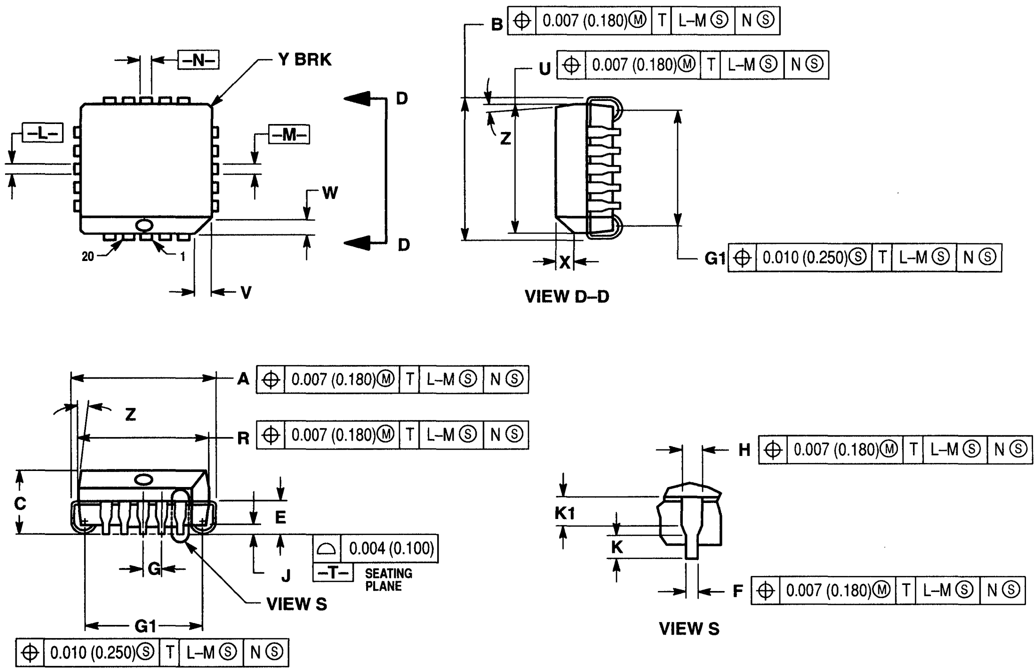


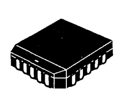
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

20–Pin Packages

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C



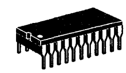


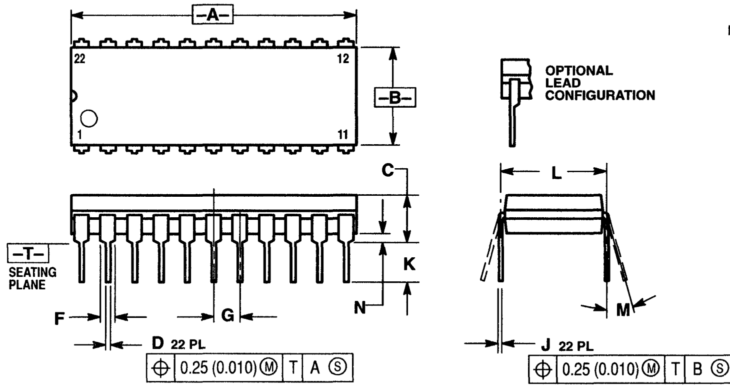
NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

22–Pin Packages

J SUFFIX
CERAMIC DIP PACKAGE
CASE 736–05
ISSUE E

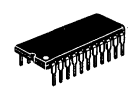


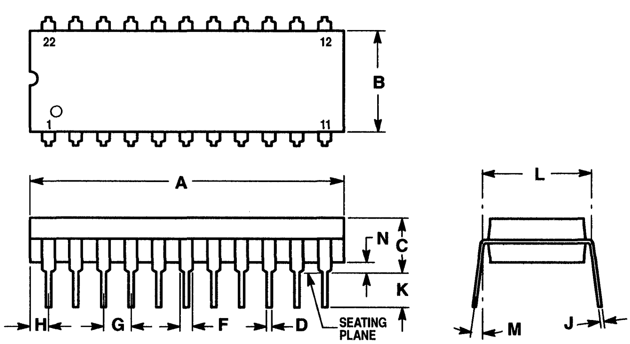


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 11, 12, AND 22.
5. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.060	1.095	26.93	27.81
B	0.360	0.390	9.15	9.90
C	0.150	0.215	3.81	5.46
D	0.015	0.021	0.39	0.53
F	0.050	0.065	1.27	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.20	0.39
K	0.125	0.170	3.18	4.31
L	0.400 BSC		10.16 BSC	
M	0°	15°	0°	15°
N	0.020	0.050	0.51	1.27

N SUFFIX
PLASTIC DIP PACKAGE
CASE 708–04
ISSUE D



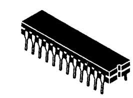


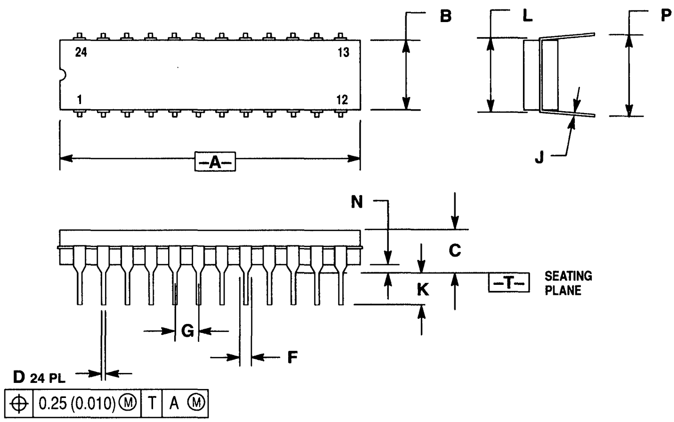
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

24–Pin Packages

J SUFFIX
CERAMIC DIP PACKAGE
CASE 758–02
ISSUE A

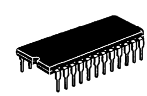


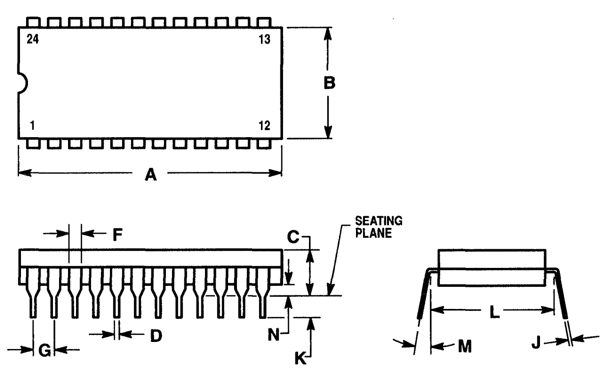


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.240	1.285	31.50	32.64
B	0.285	0.305	7.24	7.75
C	0.160	0.200	4.07	5.08
D	0.015	0.021	0.38	0.53
F	0.045	0.062	1.14	1.57
G	0.100 BSC		2.54 BSC	
J	0.008	0.013	0.20	0.33
K	0.100	0.165	2.54	4.19
L	0.300	0.310	7.62	7.87
N	0.020	0.050	0.51	1.27
P	0.360	0.400	9.14	10.16

L,J,JW SUFFIX
CERAMIC DIP PACKAGE
CASE 623–05
ISSUE M



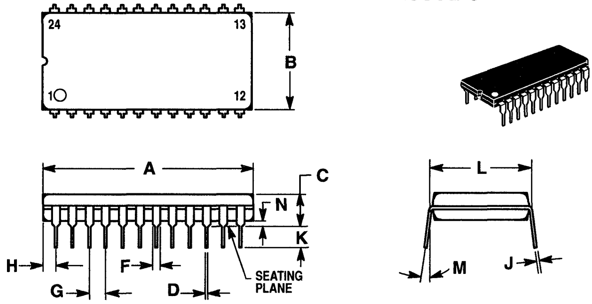


NOTES:
1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED PARALLEL).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

24–Pin Packages

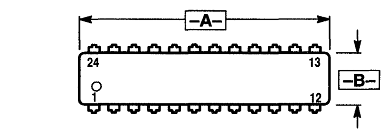
N SUFFIX
PLASTIC DIP PACKAGE
CASE 709–02
ISSUE C

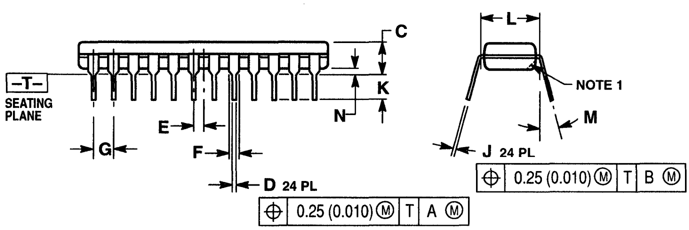


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

P,N SUFFIX
PLASTIC DIP PACKAGE
CASE 724–03
ISSUE D

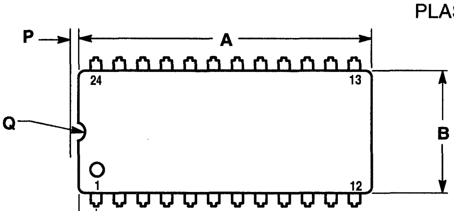


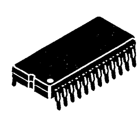


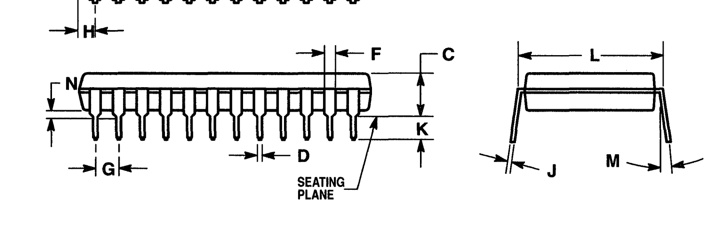
NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P,N,PW SUFFIX
PLASTIC DIP PACKAGE
CASE 649–03
ISSUE D





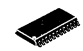


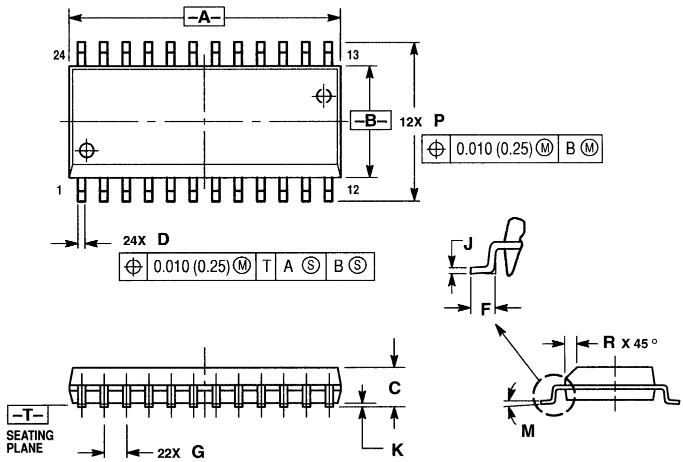
NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

24–Pin Packages

DW SUFFIX
PLASTIC WIDE SOIC PACKAGE
CASE 751E–04
ISSUE E

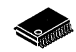


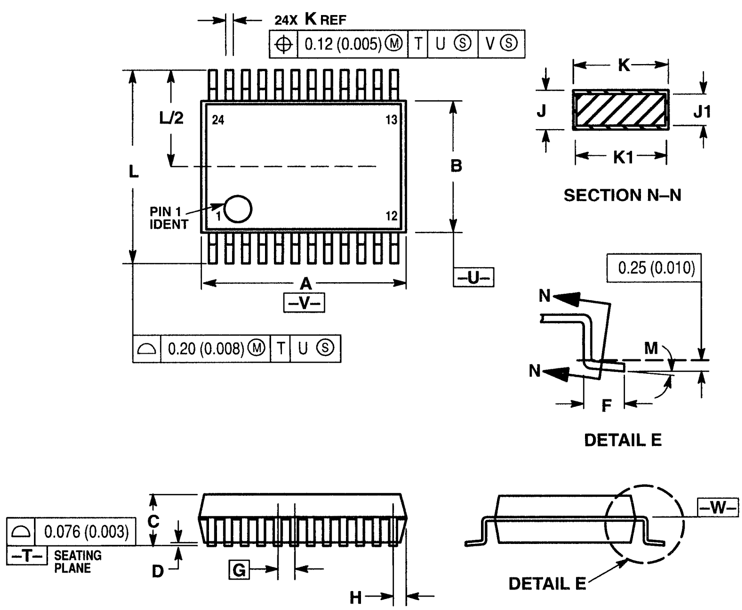


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940D–03
ISSUE B



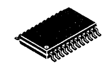


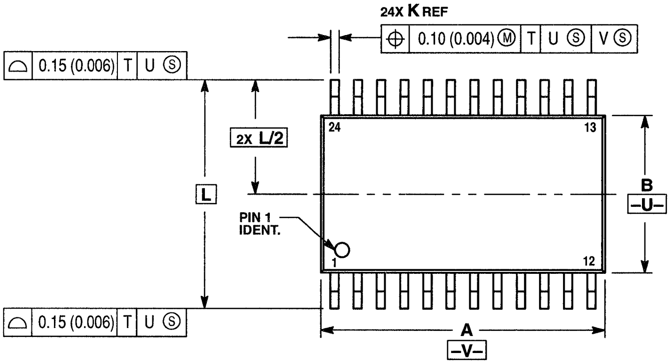
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

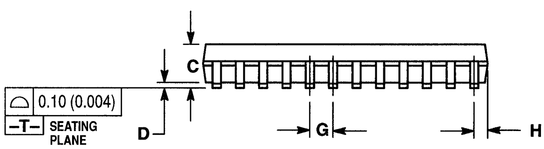
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.07	8.33	0.317	0.328
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.44	0.60	0.017	0.024
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

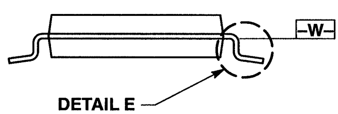
24–Pin Packages

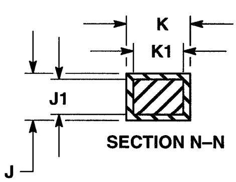
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948H–01
ISSUE O



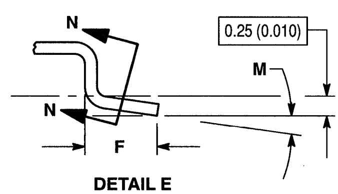








SECTION N–N



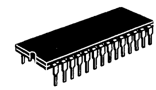
DETAIL E

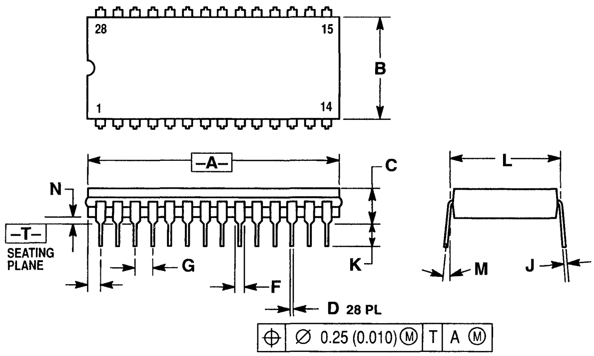
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

28–Pin Packages

J SUFFIX
CERAMIC DIP PACKAGE
CASE 733–04
ISSUE C

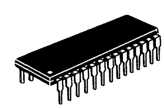


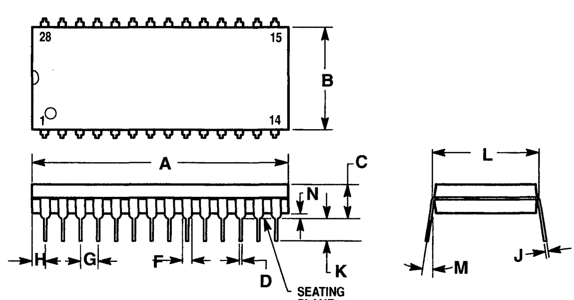


NOTES:
1. DIMENSIONS A AND B INCLUDES MENISCUS.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.490	36.45	37.84
B	0.500	0.605	12.70	15.36
C	0.160	0.230	4.06	5.84
D	0.015	0.022	0.38	0.55
F	0.050	0.065	1.27	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.20	0.30
K	0.125	0.160	3.18	4.06
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.050	0.51	1.27

N SUFFIX
PLASTIC DIP PACKAGE
CASE 710–02
ISSUE B



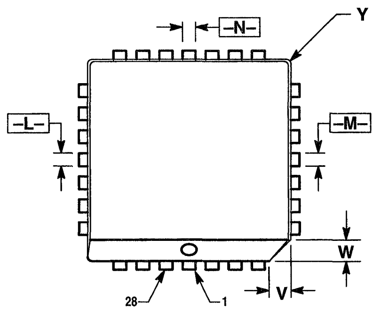


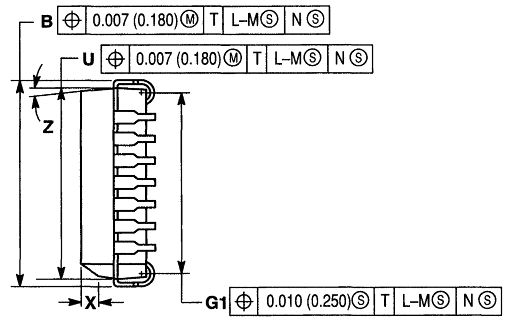
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

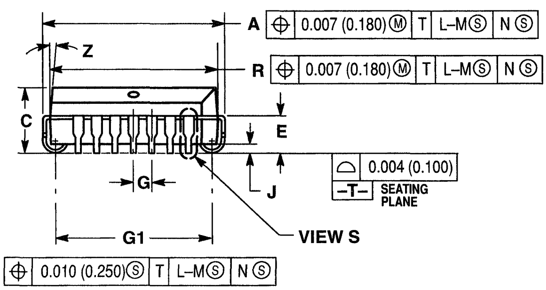
28–Pin Packages

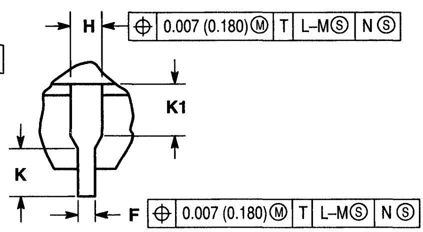
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE D



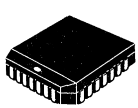


VIEW D–D





VIEW S

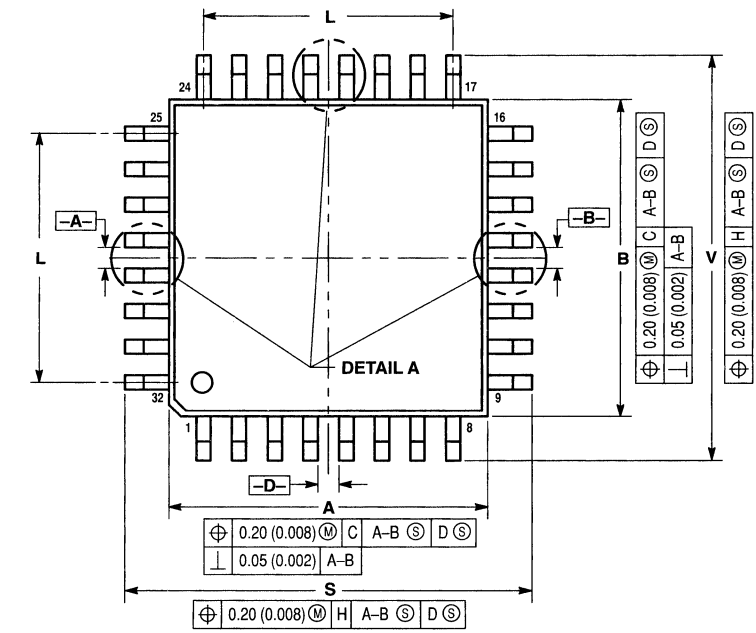


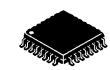
NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

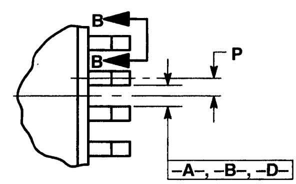
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

32–Pin Package

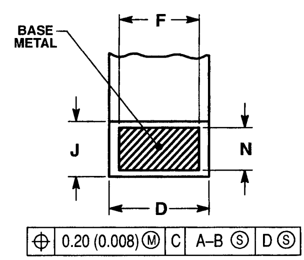
FA SUFFIX
PLASTIC TQFP PACKAGE
CASE 873–01
ISSUE A



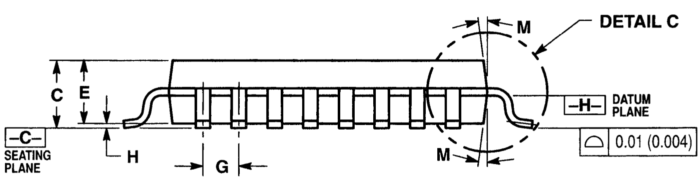


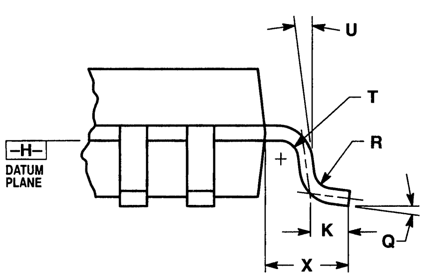


DETAIL A



SECTION B–B
VIEW ROTATED 90° CLOCKWISE





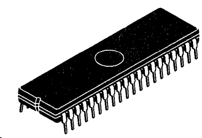
DETAIL C

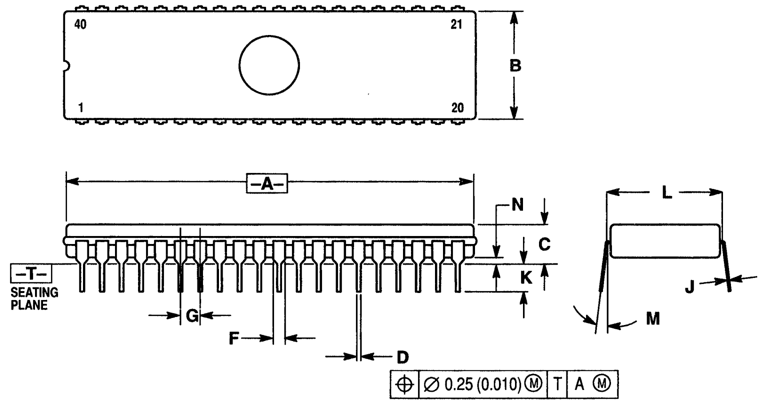
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC		0.031 BSC	
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.00 REF		0.039 REF	

40–Pin Packages

J SUFFIX
CERAMIC DIP PACKAGE
CASE 734–04
ISSUE D

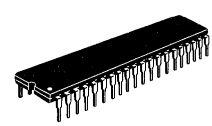


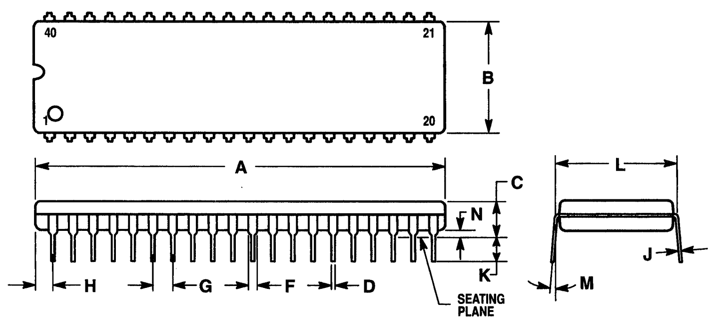


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B INCLUDE MENISCUS.
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

N SUFFIX
PLASTIC DIP PACKAGE
CASE 711–03
ISSUE C



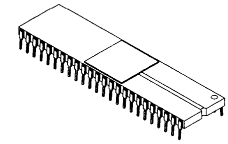


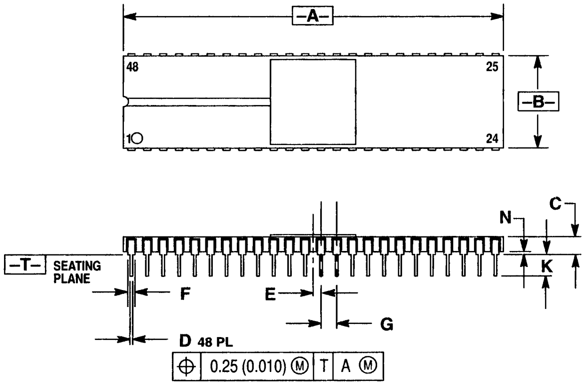
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

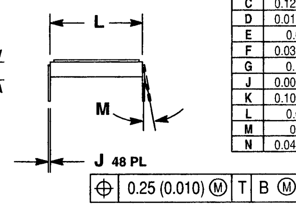
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

48–Pin Packages

J SUFFIX
CERAMIC DIP PACKAGE
CASE 740–03
ISSUE B



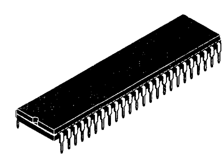


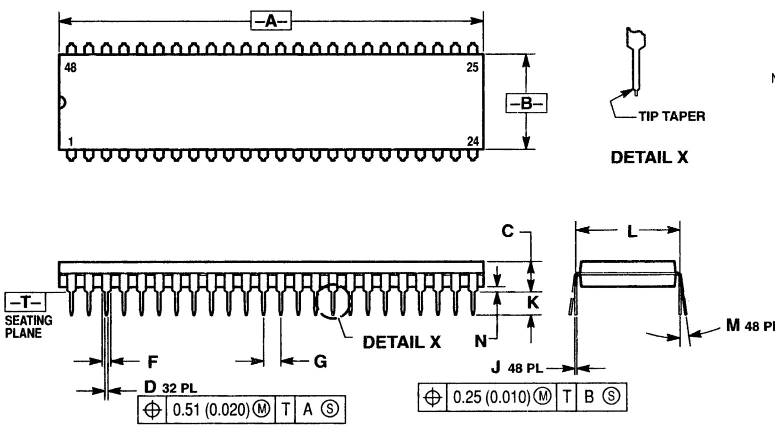


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	2.376	2.424	60.36	61.56
B	0.576	0.604	14.64	15.34
C	0.120	0.127	3.05	4.31
D	0.015	0.021	0.381	0.533
E	0.050 BSC		1.27 BSC	
F	0.030	0.055	0.762	1.397
G	0.100 BSC		2.54 BSC	
J	0.008	0.013	0.204	0.330
K	0.100	0.165	2.54	4.19
L	0.600 BSC		15.24 BSC	
M	0°	10°	0°	10°
N	0.040	0.060	1.016	1.524

N SUFFIX
PLASTIC DIP PACKAGE
CASE 767–02
ISSUE B



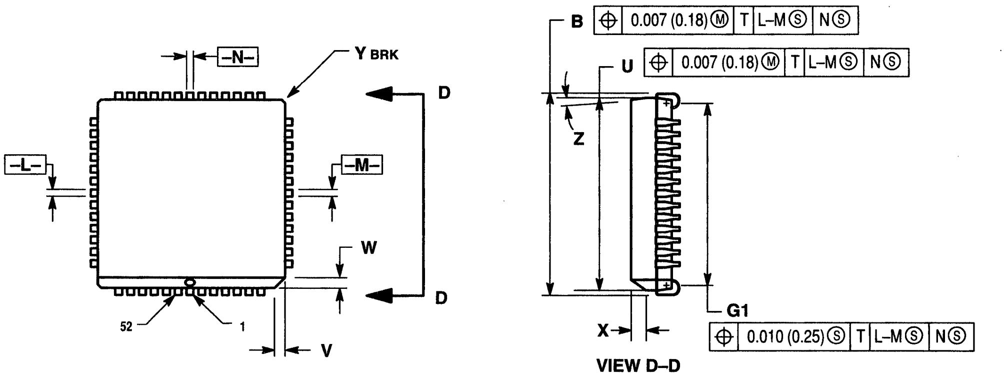


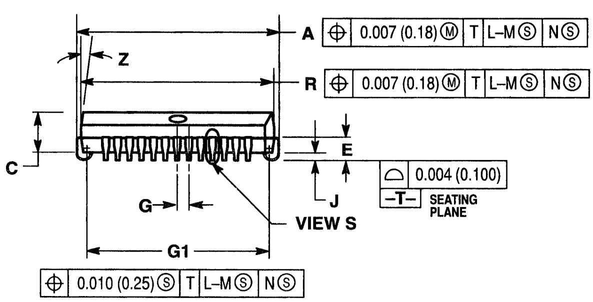
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

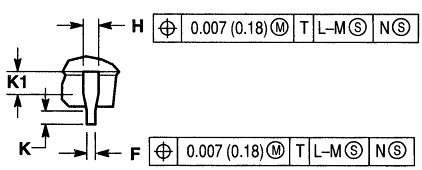
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	2.415	2.445	61.34	62.10
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.55
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.070 BSC		1.79 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.150	2.92	3.81
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

52–Pin Packages

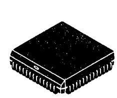
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 778–02
ISSUE C







VIEW S

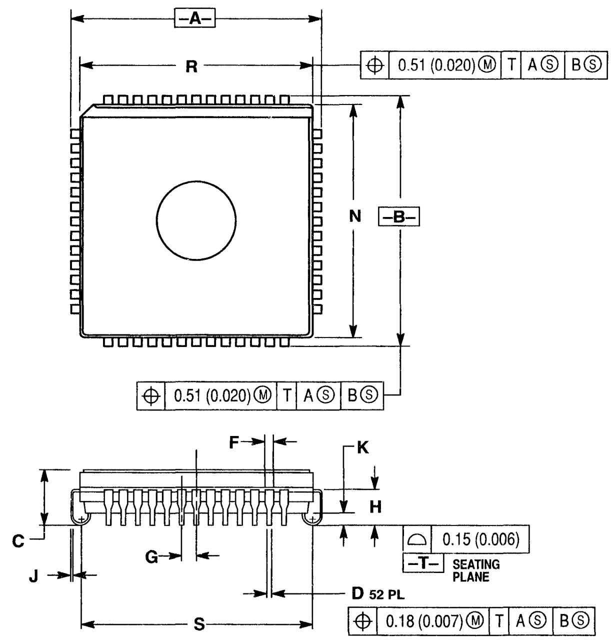


NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.710	0.730	18.04	18.54
K1	0.040	—	1.02	—

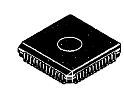
52–Pin Packages

FJ SUFFIX
PLASTIC PLCC PACKAGE
CASE 778B–01
ISSUE O



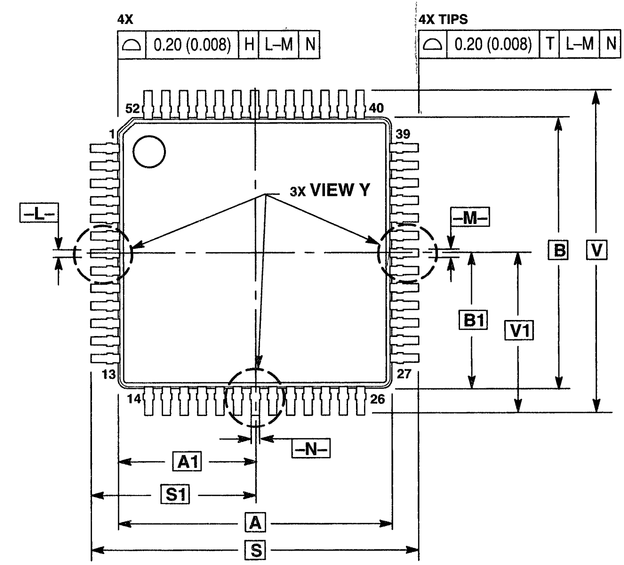
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R AND N DO NOT INCLUDE GLASS PROTRUSION. GLASS PROTRUSION TO BE 0.25 (0.010) MAXIMUM.
4. ALL DIMENSIONS AND TOLERANCES INCLUDE LEAD TRIM OFFSET AND LEAD FINISH.

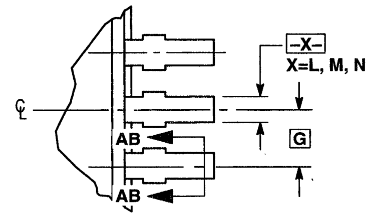
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.200	4.20	5.08
D	0.017	0.021	0.44	0.53
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
H	0.090	0.130	2.29	3.30
J	0.006	0.010	0.16	0.25
K	0.035	0.045	0.89	1.14
N	0.735	0.756	18.67	19.20
R	0.735	0.756	18.67	19.20
S	0.690	0.730	17.53	18.54



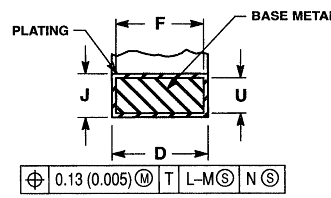
52–Pin Packages

FA SUFFIX
PLASTIC TQFP PACKAGE
CASE 848D–03
ISSUE C

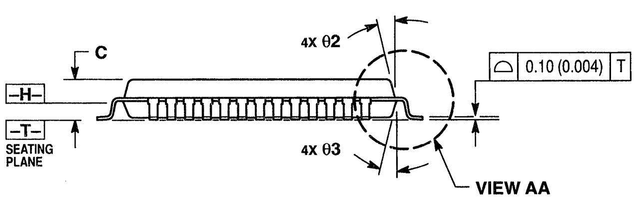


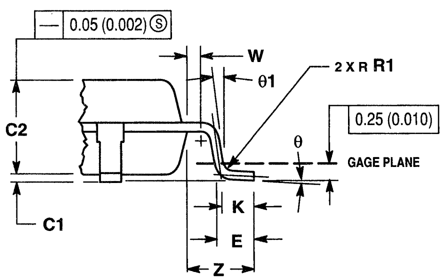


VIEW Y

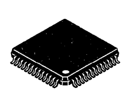


SECTION AB–AB
ROTATED 90° CLOCKWISE





VIEW AA

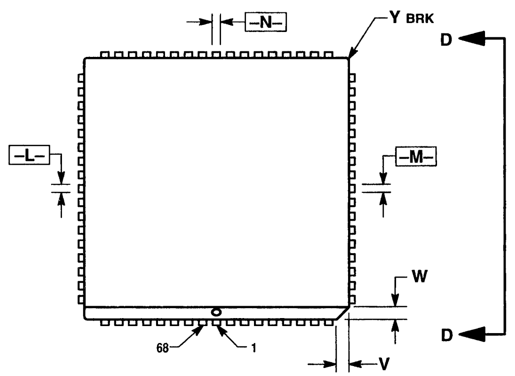


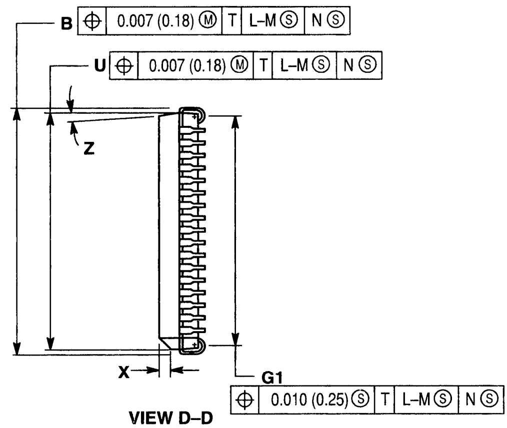
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

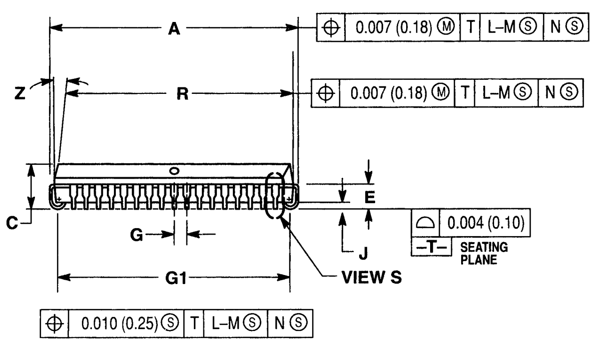
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.70	—	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	5°	13°	5°	13°

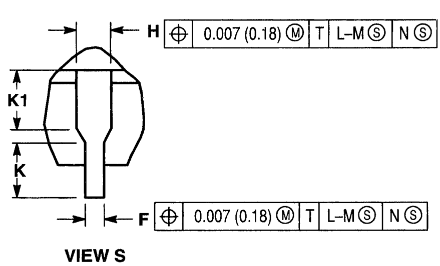
68–Pin Package

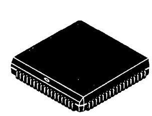
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 779–02
ISSUE C











NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.985	0.995	25.02	25.27
B	0.985	0.995	25.02	25.27
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.950	0.956	24.13	24.28
U	0.950	0.956	24.13	24.28
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.910	0.930	23.12	23.62
K1	0.040	—	1.02	—

Programmable Array
84–Pin Package

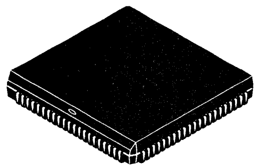
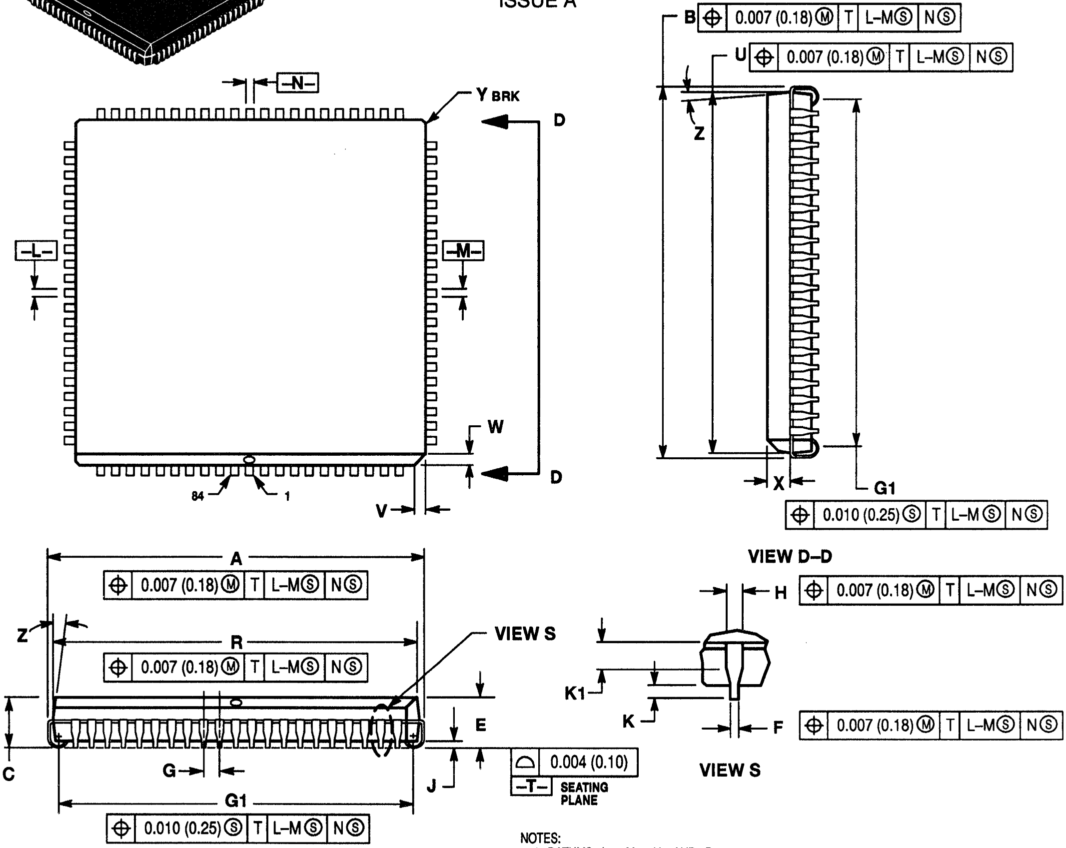


Figure 18. FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 780-01
ISSUE A



NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PACKAGE BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.94). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.185	1.195	30.10	30.35
B	1.185	1.195	30.10	30.35
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	1.150	1.156	29.21	29.36
U	1.150	1.156	29.21	29.36
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	1.110	1.130	28.20	28.70
K1	0.040	—	1.02	—

Programmable Array
128–Pin Package

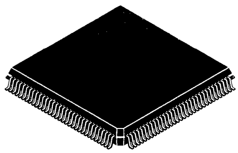
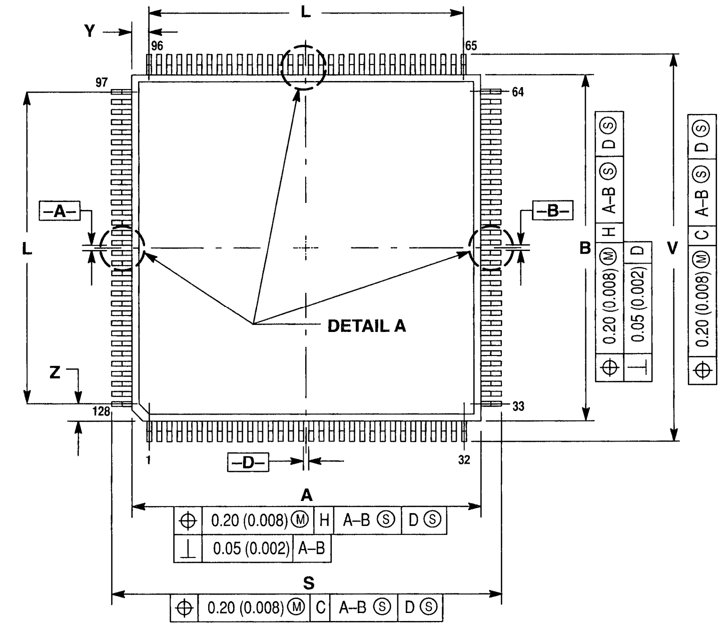
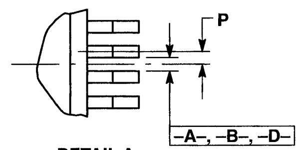


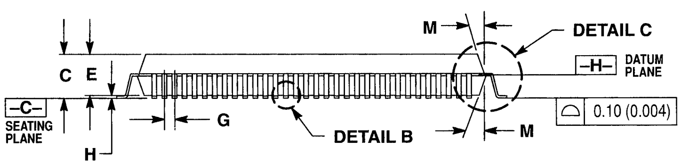
Figure 19. DD SUFFIX
PLASTIC QFP PACKAGE
CASE 862A-02
ISSUE B



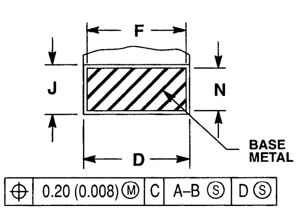


DETAIL A

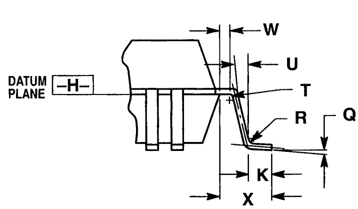
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D-TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	—	4.07	—	0.160
D	0.30	0.45	0.012	0.018
E	3.17	3.67	0.125	0.144
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.032 BSC	
H	0.25	0.35	0.010	0.014
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	24.80 REF		0.976 REF	
M	5°	16°	5°	16°
N	0.13	0.17	0.005	0.007
P	0.40 BSC		0.016 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	30.95	31.45	1.219	1.238
T	0.13	—	0.005	—
U	0°	—	0°	—
V	30.95	31.45	1.219	1.238
W	0.40	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.60 REF		0.063 REF	
Z	1.60 REF		0.063 REF	



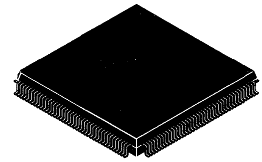
DETAIL B

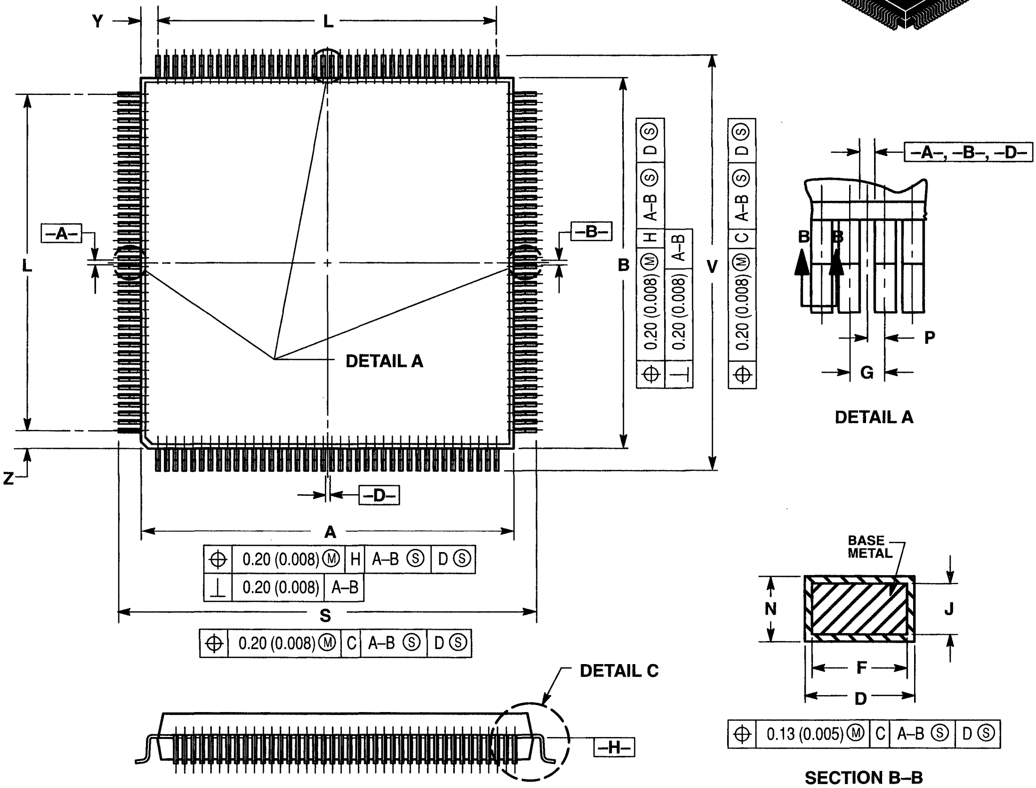


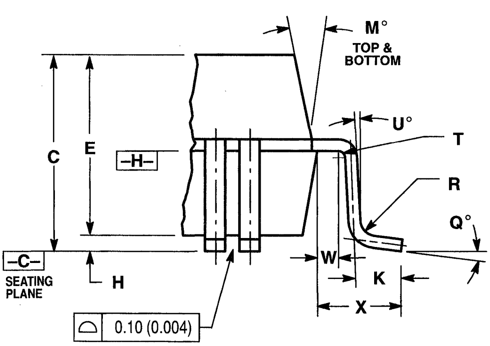
DETAIL C

Programmable Array
160–Pin Package

Figure 20. DH SUFFIX
PLASTIC QFP PACKAGE
CASE 864A-03
ISSUE C







DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.35	3.85	0.132	0.152
D	0.22	0.38	0.009	0.015
E	3.20	3.50	0.126	0.138
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 REF	
H	0.25	0.35	0.010	0.014
J	0.11	0.23	0.004	0.009
K	0.70	0.90	0.028	0.035
L	25.35 REF		0.998 REF	
M	5°	16°	5°	16°
N	0.11	0.19	0.004	0.007
P	0.325 BSC		0.013 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	—	0.005	—
U	0°	—	0°	—
V	31.00	31.40	1.220	1.236
W	0.40	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	

Programmable Array
181–Pin Package

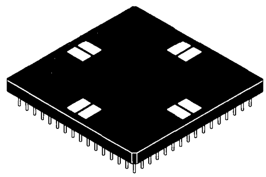
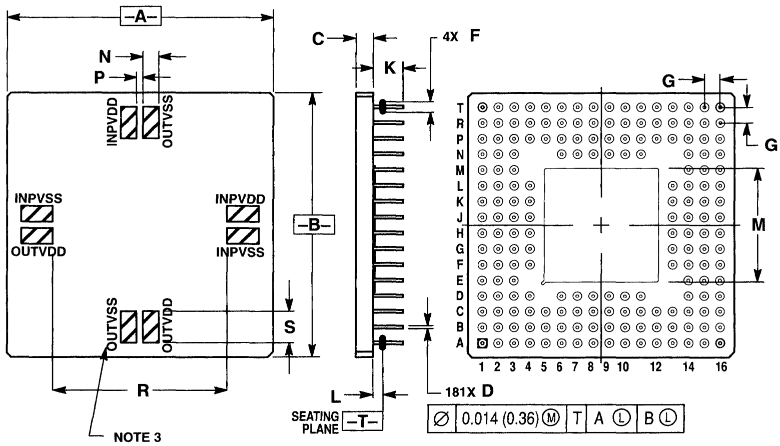


Figure 21. HI SUFFIX
PIN GRID ARRAY PACKAGE
CASE 795A–02
ISSUE A

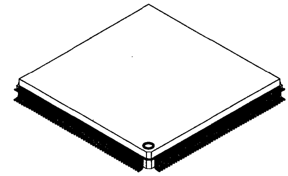


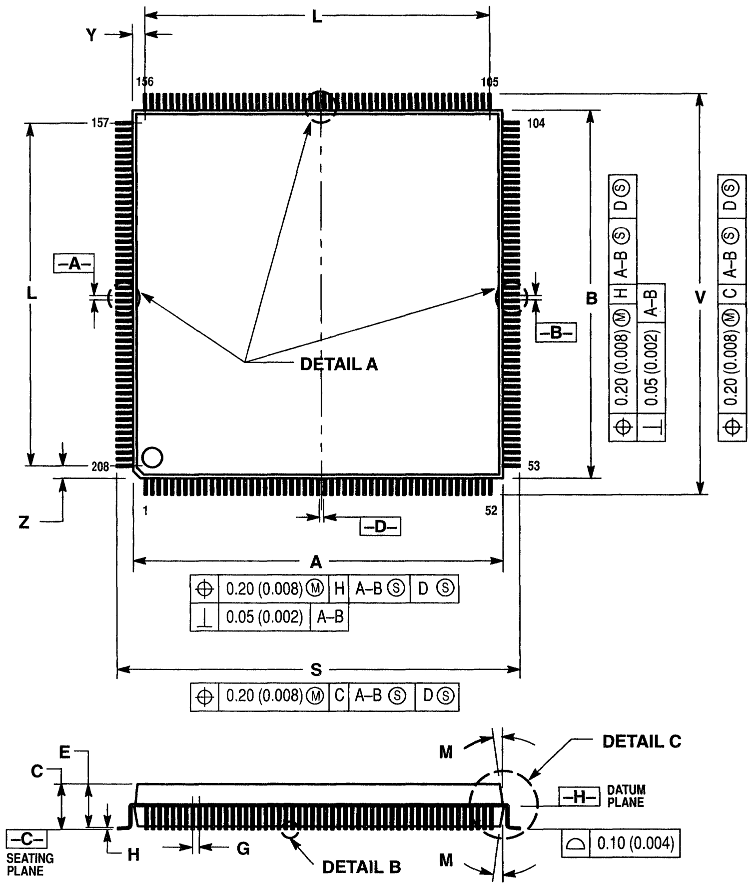
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MARKING SHOWN FOR INFORMATION ONLY, NOT ON ACTUAL PART.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.640	1.680	41.66	42.67
B	1.640	1.680	41.66	42.67
C	0.088	0.112	2.24	2.84
D	0.017	0.019	0.43	0.48
F	0.043	0.057	1.09	1.45
G	0.100 BSC		2.54 BSC	
K	0.163	0.197	4.14	5.00
L	0.025	0.039	0.64	0.99
M	0.700	0.720	17.78	18.29
N	0.095	0.105	2.41	2.67
P	0.035	0.045	0.89	2.41
R	1.095	1.105	27.81	28.07
S	0.195	0.205	4.95	5.21

Programmable Array
208–Pin Package

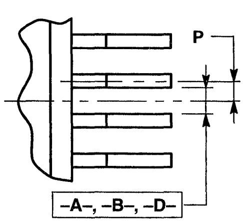
Figure 22. DK SUFFIX
PLASTIC QFP PACKAGE
CASE 872A-01
ISSUE O



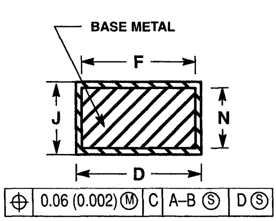


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.38 (0.015).

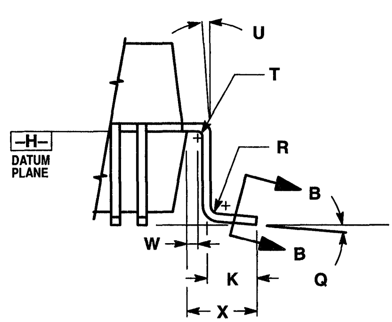
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.45	4.10	0.136	0.161
D	0.14	0.30	0.005	0.012
E	3.20	3.60	1.126	0.142
F	0.14	0.26	0.005	0.010
G	0.50 BSC		0.020 BSC	
H	0.25	0.35	0.010	0.014
J	0.09	0.20	0.003	0.008
K	0.70	0.90	0.027	0.036
L	25.50 REF		1.004 REF	
M	5°	9°	5°	9°
N	0.09	0.18	0.003	0.007
P	0.25 BSC		0.010 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	—	0.005	—
U	0°	—	0°	—
V	31.00	31.40	1.220	1.236
W	0.40	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.25 REF		0.049 REF	
Z	1.25 REF		0.049 REF	



DETAIL A



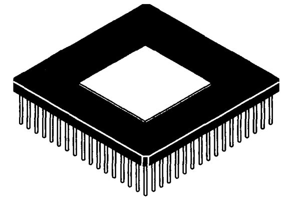
DETAIL B
SECTION B–B
ROTATED 7° CCW

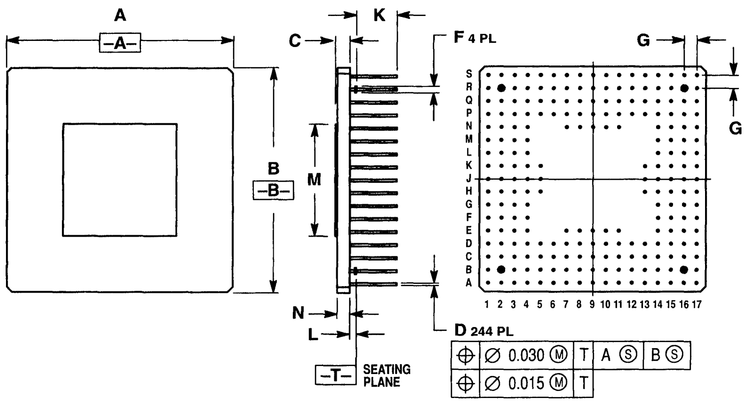


DETAIL C

Programmable Array
224–Pin Package

Figure 23. KE SUFFIX
PIN GRID ARRAY PACKAGE
CASE 823B–01
ISSUE O





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.726	1.744	43.84	44.30
B	1.726	1.744	43.84	44.30
C	0.095	0.120	2.41	3.05
D	0.018		0.46	
F	0.050		1.27	
G	0.100 BSC		2.54 BSC	
K	0.283	0.339	7.19	8.61
L	0.043	0.057	1.09	1.45
M	0.865	0.885	21.97	22.48
N	0.080	0.100	2.03	2.54

Programmable Array
299–Pin Package

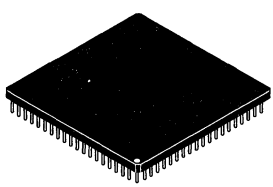
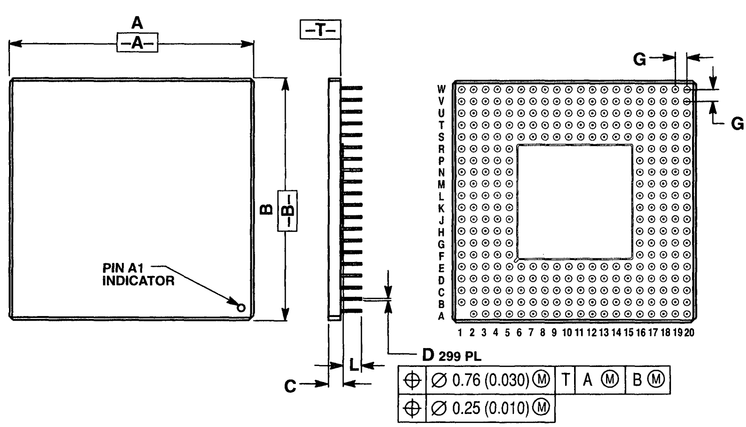


Figure 24. HV SUFFIX
PIN GRID ARRAY PACKAGE
CASE 861A–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	2.040	2.080	51.82	52.83
B	2.040	2.080	51.82	52.83
C	0.110	0.140	2.80	3.55
D	0.017	0.019	0.43	0.48
G	0.100 BSC		2.54 BSC	
L	0.150	0.170	3.81	4.31

Packaging Information

Surface Mount

Why Surface Mount?

Surface Mount Technology is utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the state–of–the–art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contributes significantly to lower PC board prices.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and/or offer increased functions with the same size product.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Pin Conversion Tables

Dual–in–Line Package to PLCC Pin Conversion Data

The following table gives the equivalent I/O pinouts of Dual–In–Line Package (DIP) configuration and Plastic Leaded Chip Carrier (PLCC) packages.*

Conversion Tables

8 PIN DIP	1	2	3	4	5	6	7	8
20 PIN PLCC	2	5	7	10	12	15	17	20

14 PIN DIP	1	2	3	4	5	6	7	8	9	10	11	12	13	14
20 PIN PLCC	2	3	4	6	8	9	10	12	13	14	16	18	19	20

16 PIN DIP	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
20 PIN PLCC	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

20 PIN DIP	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
20 PIN PLCC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

24 PIN DIP	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
28 PIN PLCC	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28

* The MC1648 has a Non–Standard Conversion Table. For more information, refer to the Motorola MECL Data Book, DL122/D.

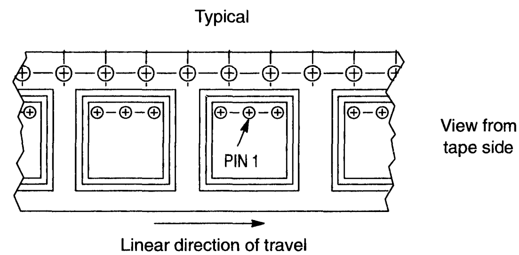
Tape and Reel

Logic Integrated Circuits

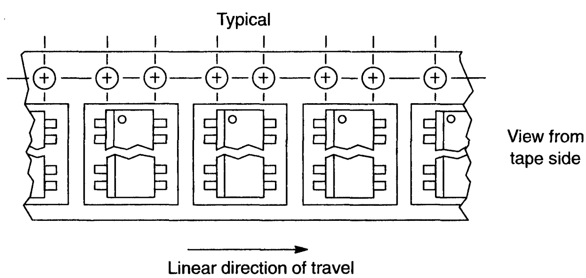
Motorola's tape and reel packaging fully conforms to the latest EIA RS–481A specification. The antistatic embossed tape provides a secure cavity sealed with a peel–back cover tape.

Mechanical Polarization

PLCC Devices



SOIC Devices



General Information

— Reel Size	13 inch (330 mm) Suffix: R2	— Units/Reel	500 to 5000 (see table)
— Tape Width	12 mm to 24 mm (see table)		

Ordering Information

To order devices which are to be delivered in Tape and Reel, add the suffix R2 to the device number being ordered.

Tape and Reel Data

Device Type	Tape Width (mm)	Device/Reel	Reel Size (inch)	Min Lot Size Per Part No. Tape and Reel
PLCC–20	16	1,000	13	3,000
PLCC–28	24	500	13	500
SO–8	12	2,500	13	5,000
SO–14	16	2,500	13	5,000
SO–16	16	2,500	13	5,000
SO–16 Wide	16	1,000	13	5,000
SO–20 Wide	24	1,000	13	5,000

Logic Literature Listing

For additional information, refer to the following Motorola Logic Documents, available through the Literature Distribution Center.

LOGIC NEW PRODUCT CALENDAR

BR1332/D	Logic Quarterly New Product Calendar

DATA BOOKS

BR1333/D	Timing Solutions
BR1334/D	High Performance Frequency Control Products
BR1335/D	Low Voltage Logic
BR1339/D	LCX Data
DL121/D	FAST and LS TTL Data
DL122/D	MECL Data
DL129/D	High–Speed CMOS Data
DL131/D	CMOS Logic Data
DL138/D	FACT Data
DL140/D	High Performance ECL Data – ECLinPS and ECLinPS Lite
DL201/D	MPA – Motorola Programmable Arrays

DESIGN HANDBOOKS

HB205/D	MECL Systems Design Handbook

APPLICATION NOTES

AN1091/D	Low Skew Clock Drivers and Their System Design Considerations
AN1092/D	Driving High Capacitance DRAMs in an ECL System
AN1400/D	H64x Clock Driver I/O SPICE Modelling Kit
AN1401/D	Using SPICE to Analyze the Effects of Board Layout on System Skew When Designing With the MC10/100640 Family of Clock Drivers
AN1402/D	MC10/100H600 Translator Family I/O SPICE Modelling Kit
AN1403/D	FACT™ I/O Model Kit
AN1404/D	ECLinPS™ Circuit Performance at Non–Standard VIH Levels
AN1405/D	ECL Clock Distribution Techniques
AN1406/D	Designing With PECL (ECL at +5.0V)
AN1407/D	Performance Testing With the ALExIS™ Mini–Evaluation Boards
AN1408/D	Power Dissipation for Active SCSI Terminators
AN1410/D	Configuring and Applying the MC54/74HC4046A Phase–Locked Loop
AN1503/D	ECLinPS™ I/O SPICE Modelling Kit
AN1504/D	Metastability and the ECLinPS™ Family

OTHER DOCUMENTATION

SG365/D	Timing Solutions Folder Selector Guide
BR1341/D	Motorola Programmable Array Update Folder

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MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

Analog and Interface Integrated Circuits

In Brief . . .

Motorola Analog and Interface Integrated Circuits cover a much broader range of products than the traditional op amps/regulators/consumer–image associated with Analog suppliers. Analog circuit technology currently influences the design and architecture of equipment for all major markets. As with other integrated circuit technologies, Analog circuit design techniques and processes have been continually refined and updated to meet the needs of these diversified markets.

Operational amplifiers have utilized JFET inputs for improved performance, plus innovative design and trimming concepts have evolved for improved high performance and precision characteristics. In analog power ICs, basic voltage regulators have been refined to include higher current and voltage levels, low dropout regulators, and more precise three–terminal fixed and adjustable voltages. The power area continues to expand into switching regulators, power supply control and supervisory circuits, motor controllers, and battery charging controllers.

Analog designs also offer a wide array of line drivers, receivers and transceivers for many of the EIA, European, IEEE and IBM interface standards. Peripheral drivers for a variety of devices are also offered. In addition to these key interface functions, hard disk drive read channel circuits, 10BASE–T and Ethernet circuits are also available.

In Data Conversion, a high performance video speed flash converter is available, as well as a variety of CMOS and Sigma–Delta converters. Analog circuit technology has also provided precision low–voltage references for use in Data Conversion and other low temperature drift applications.

A host of special purpose analog devices have also been developed. These circuits find applications in telecommunications, radio, television, automotive, RF communications, and data transmission. These products have reduced the cost of RF communications, and have provided capabilities in telecommunications which make the telephone line convenient for both voice and data communications. Analog developments have also reduced the many discrete components formerly required for consumer functions to a few IC packages and have made significant contributions to the rapidly growing market for electronics in automotive applications.

The table of contents provides a perspective of the many markets served by Analog/Interface ICs and of Motorola's involvement in these areas.

Amplifiers and Comparators

In Brief . . .

For over two decades, Motorola has continually refined and updated integrated circuit technologies, analog circuit design techniques and processes in response to the needs of the marketplace. The enhanced performance of newer operational amplifiers and comparators has come through innovative application of these technologies, designs and processes. Some early designs are still available but are giving way to the new, higher performance operational amplifier and comparator circuits. Motorola has pioneered in JFET inputs, low temperature coefficient input stages, Miller loop compensation, all NPN output stages, dual–doublet frequency compensation and analog "in–the–package" trimming of resistors to produce superior high performance operational amplifiers and comparators, operating in many cases from a single supply with low input offset, low noise, low power, high output swing, high slew rate and high gain–bandwidth product at reasonable cost to the customer.

Present day operational amplifiers and comparators find applications in all market segments including motor controls, instrumentation, aerospace, automotive, telecommunications, medical, and consumer products.

Operational Amplifiers

Motorola offers a broad line of bipolar operational amplifiers to meet a wide range of applications. From low–cost industry–standard types to high precision circuits, the span encompasses a large range of performance capabilities. These Analog integrated circuits are available as single, dual and quad monolithic devices in a variety of temperature ranges and package styles. Most devices may be obtained in unencapsulated "chip" form as well. For price and delivery information on chips, please contact your Motorola Sales Representative or Distributor.

Table 1. Single Operational Amplifiers

Device	I_{IB} (µA) Max	V_{IO} (mV) Max	TC_{VIO} (µV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/µs) Typ	Supply Voltage (V) Min	Supply Voltage (V) Max	Description	Suffix/ Package
Noncompensated											
Commercial Temperature Range (0°C to +70°C)											
LM301A	0.25	7.5	10	50	25	1.0	0.5	±3.0	±18	General Purpose	N/626, D/751
LM308A	7.0	0.5	5.0	1.0	80	1.0	0.3	±3.0	±18	Precision	N/626, D/751
Industrial Temperature Range (–25°C to +85°C)											
LM201A	0.075	2.0	10	10	50	1.0	0.5	±3.0	±22	General Purpose	N/626, D/751
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF351	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/626, D/751
LF411C	200 pA	2.0	10	100 pA	25	8.0	25	+5.0	±22	JFET Input, Low Offset, Low Drift	N/626, D/751
LF441C	100 pA	5.0	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power, JFET Input	N/626, D/751
LM11C	100 pA	0.6	2.0	10 pA	250	1.0	0.3	±3.0	±20	Precision	N/626
LM11CL	200 pA	5.0	3.0	25 pA	50	1.0	0.3	±3.0	±20	Precision	N/626
MC1436, C	0.04	10	12	10	70	1.0	2.0	±15	±34	High Voltage	P1/626, D/751
MC1741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	General Purpose	P1/626, D/751
MC1776C	0.003	6.0	15	3.0	100	1.0	0.2	±1.2	±18	µPower, Programmable	P1/626, D/751
MC3476	0.05	6.0	15	25	50	1.0	0.2	±1.5	±18	Low Cost, µPower, Programmable	P1/626
MC34001	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
MC34001B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, D/751
MC34071	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/626, D/751
MC34071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, D/751
MC34080B	200 pA	1.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/626, D/751
MC34081B	200 pA	1.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, D/751
MC34181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/626
TL071AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, D/751
TL071C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, D/751
TL081AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, D/751
TL081C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
Automotive Temperature Range (–40°C to +85°C)											
MC33071	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/626, D/751
MC33071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, D/751
MC33171	0.1	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/626, D/751
MC33181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/626, D/751
Extended Automotive Temperature Range (–40°C to +105°C)											
MC33201	250 nA	9.0	2.0	100	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail™	P/626, D/751
Military Temperature Range (–55°C to +125°C)											
MC33201	400 nA	9.0	2.0	200	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail™	P/626, D/751

Table 2. Dual Operational Amplifiers

Device	I_{IB} (µA) Max	V_{IO} (mV) Max	TC_{VIO} (µV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/µs) Typ	Supply Voltage (V) Min	Max	Description	Suffix/ Package
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF353	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/626, D/751
LF412C	200 pA	3.0	10	100 pA	25	4.0	13	+5.0	±18	JFET Input, Low Offset, Low Drift	N/626, D/751
LF442C	100 pA	5.0	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power, JFET Input	N/626
LM358	0.25	6.0	7.0	50	25	1.0	0.6	±1.5 +3.0	±18 +36	Single Supply, Low Power Consumption	N/626, D/751
LM833	1.0	5.0	2.0	200	31.6	15	7.0	+2.5	±18	Low Noise, Audio	N/626, D/751
MC/MCT1458	0.5	6.0	10	200	20	1.1	0.8	±3.0	±18	Dual MC1741	P1/626, D/751
MC1458C	0.7	10	10	300	20	1.1	0.8	±3.0	±18	General Purpose	P1/626, D/751
MC3458	0.5	10	7.0	50	20	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies, Single Supply, Low Crossover Distortion	P1/626, D/751
MC4558AC	0.5	5.0	10	200	50	2.8	1.6	±3.0	±22	High Frequency	P1/626
MC/MCT4558C	0.5	6.0	10	200	20	2.8	1.6	±3.0	±18	High Frequency	P1/626, D/751
MC34002	100 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
MC34002B	100 pA	5.0	10	70 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
MC34072	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/626, D/751
MC34072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, D/751
MC34082	200 pA	3.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/626
MC34083B	200 pA	3.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/626
MC34182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/626, D/751
TL062AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	P/626, D/751
TL062C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	P/626, D/751
TL072AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, D/751
TL072C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, D/751
TL082AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, D/751
TL082C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
Industrial Temperature Range (–25°C to +85°C)											
LM258	0.15	5.0	10	30	50	1.0	0.6	±1.5 +3.0	±18 +36	Split or Single Supply Op Amp	N/626, D/751
Automotive Temperature Range (–40°C to +85°C)											
LM2904	0.25	7.0	7.0	50	100 typ	1.0	0.6	±1.5 +3.0	±13 +26	Split or Single Supply	N/626, D/751
MC3358	5.0	8.0	10	75	20	1.0	0.6	±1.5 +3.0	±18 +36	Split or Single Supply	P1/626
MC33072	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/626, D/751
MC33072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, D/751
MC33076	0.5	4.0	2.0	70	25	7.4	2.6	±2.0	±18	High Output Current	P1/626, P2/648C, D/751
MC33077	1.0	1.0	2.0	180	150	37	11	±2.5	±18	Low Noise	P/626, D/751
MC33078	750 nA	2.0	2.0	150	31.6	16	7.0	±5.0	±18	Low Noise	N/626, D/751
MC33102											P/626, D/751
(Awake)	600 nA	3.0	1.0	60	25	4.6	1.7	±2.5	±18	Sleepmode™	
(Sleep)	60 nA	3.0	1.0	6.0	15	0.3	0.1	±2.5	±18	Micropower	
MC33172	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/626, D/751
MC33178	0.5	3.0	2.0	50	50	5.0	2.0	±2.0	±18	High Output Current	P/626, D/751
MC33182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/626, D/751
MC33272A	650 nA	1.0	0.56	25 nA	31.6	5.5	11.5	±1.5	±18	High Performance	P/626, D/751
MC33282	100 pA	200 µV	5.0	50 pA	50	30	12	±2.5	±18	Low Input, Offset JFET	P/626, D/751
TL062V	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	P/626, D/751

Table 2. Dual Operational Amplifiers (continued)

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V) Min	Max	Description	Suffix/ Package
Extended Automotive Temperature Range (−40°C to +105°C)											
MC33202 MC33206	250 nA	11	2.0	100	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail™ Rail–to–Rail™ with Enable	P/626, D/751 P/646, D/751A
Extended Automotive Temperature Range (−40°C to +125°C)											
TCA0372	500 nA	15	20	50	30	1.1	1.4	+5.0	+36	Power Op Amp, Single Supply	DP2/648, DW/751G
Military Temperature Range (−55°C to +125°C)											
MC33202	400 pA	11	2.0	200 pA	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail™	P/626, D/751

Table 3. Quad Operational Amplifiers

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V) Min	Max	Description	Suffix/ Package
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF347	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/646
LF347B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	N/646
LF444C	100 pA	10	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power, JFET Input	N/646, D/751A
LM324, A	0.25	6.0	7.0	50	25	1.0	0.6	±1.5 +3.0	±16 +32	Low Power Consumption	N/646, D/751A
LM348 LM3900	0.2	6.0	–	50	25	1.0	0.5	±3.0 +3.0	±18 +36	Quad MC1741	N/646, D/751A
MC3403	0.5	10	7.0	50	20	1.0	0.6	±1.5 +3.0	±18 +36	No Crossover Distortion	P/646, D/751A
MC4741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	Quad MC1741	P/646, D/751A
MC34004	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	P/646
MC34004B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/646
MC34074	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/646, D/751A
MC34074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/646, D/751A
MC34084	200 pA	12	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/646, DW/751G
MC34085B	200 pA	12	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/646, DW/751G
MC34184	0.1 nA	10	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/646, D/751A
TL064AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	N/646, D/751A
TL064C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	N/646, D/751A
TL074AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	N/646
TL074C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	N/646
TL084AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	N/646
TL084C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	N/646
Industrial Temperature Range (−25°C to +85°C)											
LM224, A	0.15	5.0	7.0	30	50	1.0	0.6	±1.5 +3.0	±16 +32	Split Supplies or Single Supply	N/646, D/751A
Automotive Temperature Range (−40°C to +85°C)											
LM2902	0.5	10	–	50	–	1.0	0.6	±1.5 +3.0	±13 +26	Differential Low Power	N/646, D/751A
MC3301/ LM2900	0.3	–	–	–	1.0	4.0	0.6	±2.0 +4.0	±15 +28	Norton Input	P/646 N/646
MC3303	0.5	8.0	10	75	20	1.0	0.6	±1.5 +3.0	±18 +36	Differential General Purpose	P/646, D/751A
MC33074	0.5	4.5	10	75	25	4.5	10	+3.0	+44	High Performance, Single Supply	P/646, D/751A
MC33074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	High Performance	P/646, D/751A

Table 3. Quad Operational Amplifiers (continued)

Device	I_{IB} (µA) Max	V_{IO} (mV) Max	TC_{VIO} (µV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/µs) Typ	Supply Voltage (V) Min	Supply Voltage (V) Max	Description	Suffix/ Package
MC33079	750 nA	2.5	2.0	150	31.6	9.0	7.0	±5.0	±18	Low Noise	N/646, D/751A
MC33174	0.1	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/646, D/751A
MC33179	0.5	3.0	2.0	50	50	5.0	2.0	±2.0	±18	High Output Current	P/646, D/751A
MC33184	0.1 nA	10	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/646, D/751A
MC33274A	650 nA	1.0	0.56	25 nA	31.6	5.5	11.5	±1.5	±18	High Performance	P/646, D/751A
MC33284	100 pA	2.0	5.0	50 pA	50	30	12	±2.5	±18	Low Input, Offset JFET	P/646, D/751A
TL064V	200 pA	9.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	N/646, D/751A
Extended Automotive Temperature Range (–40°C to +105°C)											
MC33204	250 nA	13	2.0	100	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail™	P/646, D/751A
MC33207					50	2.2		±0.9	±6.0	Rail–to–Rail™ with Enable	P/648, D/751B
MC33304					25	3.0		+1.8	+12	Sleepmode, Rail–to–Rail™	P/646, D/751A
Military Temperature Range (–55°C to +125°C)											
MC33204	400 pA	13	2.0	200 pA	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail™	P/646, D/751A

High Frequency Amplifiers

A variety of high frequency circuits with features ranging from low cost simplicity to multifunction versatility marks Motorola's line of integrated amplifiers. Devices described here are intended for industrial and communications applications. For devices especially dedicated to consumer products, i.e., TV and entertainment radio. (See the Consumer Electronics Circuits section.)

AGC Amplifiers

MC1490/MC1350 Family Wideband General Purpose Amplifiers

The MC1490 and MC1350 family are basic building blocks – AGC (Automatic Gain Controlled) RF/Video Amplifiers. These parts are recommended for applications up through 70 MHz. The best high frequency performance may be obtained by using the physically smaller SOIC version (shorter leads) – MC1350D. There are currently no other RF ICs like these, because other manufacturers have dropped their copies. Applications include variable gain video and instrumentation amplifiers, IF (Intermediate Frequency) amplifiers for radio and TV receivers, and transmitter power output control. Many uses will be found in medical instrumentation, remote monitoring, video/graphics processing, and a variety of communications equipment. The family of parts using the same basic die (identical circuit with slightly different test parameters) is listed in the following table.

Table 4. High Frequency Amplifier Specifications

Operating Temperature Range		A_V (dB)	Bandwidth @ MHz	V_{CC}/V_{EE} (Vdc)		Suffix/ Package
–40° to +85°C	0° to +70°C	Typical		Minimum	Maximum	
–	MC1350	50	45	+6.0	+18	P/626, D/751
MC1490	–	50	10			P/626
		45	60			
		35	100			

Miscellaneous Amplifiers

Motorola provides several Bipolar and CMOS special purpose amplifiers which fill specific needs. These devices range from low power CMOS programmable amplifiers and comparators to variable–gain bipolar power amplifiers.

MC3405
Dual Operational Amplifier and Dual Voltage Comparator

This device contains two Differential Input Operational Amplifiers and two Comparators; each set capable of single supply operation. This operational amplifier–comparator circuit will find its applications as a general purpose product for automotive circuits and as an industrial "building block."

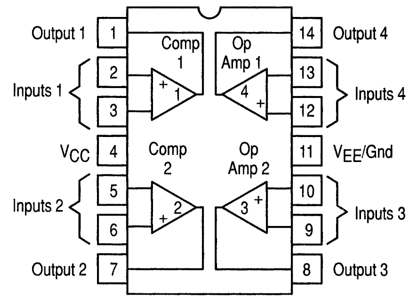


Table 5. Bipolar

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	I_{IO} (nA) Max	A_{vol} (V/mV) Min	Response (μs) Typ	Supply Voltage Single	Supply Voltage Dual	Suffix/ Package
MC3405	0.5	10	50	20	1.3	3.0 to 36	±1.5 to ±18	P/646

MC14573
Quad Programmable Operational Amplifier
MC14575
Dual Programmable Operational Amplifier and Dual Programmable Comparator
MC14576B/MC14577B
Dual Video Amplifiers

Table 6. CMOS

Function	Quantity Per Package	Single Supply Voltage Range	Dual Supply Voltage Range	Frequency Range	Device	Suffix/ Package
Operational Amplifiers	4	3.0 to 15 V	±1.5 to ±7.5 V	DC to 1.0 MHz	MC14573	P/648, D/751B
Operational Amplifiers and Comparators	2 and 2	3.0 to 15 V	±1.5 to ±7.5 V	DC to 1.0 MHz	MC14575	P/648, D/751B
Video Amplifiers	2	5.0 to 12 V(1)	±2.5 to ±6.0 V(2)	Up to 10 MHz	MC14576C MC14577C	P/626, F/904

(1) 5.0 to 10 V for surface mount package.
(2) ±2.5 to ±5.0 V for surface mount package.

Comparators

Table 7. Single Comparators

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	I_{IO} (μA) Max	A_V (V/V) Typ	I_{IO} (mA) Min	Response Time (ns)	Supply Voltage (V)	Description	Temperature Range (°C)	Suffix/ Package
Bipolar										
LM211	0.1	3.0	0.01	200 k	8.0	200	+15, –15	With strobe, will operate from single supply	–25 to +85	D/751
LM311	0.25	7.5	0.05						0 to +70	N/626, D/751
CMOS										
MC14578	1.0 pA	50	–	–	1.1	–	3.5 to 14	Requires only 10 μA from single–ended supply	–30 to +70	P/648, D/751B

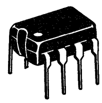
Table 8. Dual Comparators

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	I_{IO} (μA) Max	A_V (V/V) Typ	I_{IO} (mA) Min	Response Time (ns)	Supply Voltage (V)	Description	Temperature Range (°C)	Suffix/ Package
Bipolar										
LM293	0.25	5.0	0.05	200 k	6.0	1300	±1.5 to ±18 or 3.0 to 36	Designed for single or split supply operation, input common mode includes ground (negative supply)	–25 to +85	N/626, D/751
LM393		5.0				1300			0 to +70	
LM393A		2.0				1300			0 to +70	
LM2903		7.0				1500			–40 to +105	
MC3405	0.5	10	0.05	200 k	6.0	1300	±1.5 to ±7.5 or 3.0 to 15	This device contains 2 op amps and 2 comparators in a single package	0 to +70	P/646
CMOS										
MC14575	0.001	30	0.0001	2.0 k	3.0	1000	±1.5 to ±7.5 or 3.0 to 15	This device contains 2 op amps and 2 comparators in a single package	–40 to +85	P/648, D/751B

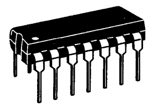
Table 9. Quad Comparators

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	I_{IO} (μA) Max	A_V (V/V) Typ	I_{IO} (mA) Min	Response Time (ns)	Supply Voltage (V)	Description	Temperature Range (°C)	Suffix/ Package
Bipolar										
LM239	0.25	5.0	0.05	200 k	6.0	1300	±1.5 to ±18 or 3.0 to 36	Designed for single or split supply operation, input common mode includes ground (negative supply)	–25 to +85	N/646, D/751A
LM239A		2.0		200 k					–25 to +85	
LM339		5.0		200 k					0 to +70	
LM339A		2.0		200 k					0 to +70	
LM2901		7.0		100 k					–40 to +85	
MC3302	0.5	20	0.5	30 k					–40 to +85	P/646
MC3430	40	6.0	1.0 Typ	1.2 k	16	33	+5.0, –5.0	High speed comparator/ sense amplifier	0 to +70	P/648
MC3431		10				33				
MC3432		6.0				40				
MC3433		10				40				
CMOS										
MC14574	0.001	30	0.0001	2.0 k	3.0	1000	±1.5 to ±7.5 or 3.0 to 15	Externally programmable power dissipation with 1 or 2 resistors	–40 to +85	P/648, D/751B

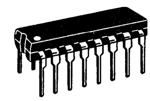
Amplifiers and Comparators Package Overview



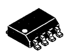
CASE 626
N, P, P1 SUFFIX



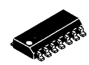
CASE 646
N, P SUFFIX



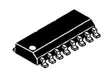
CASE 648, 648C
DP2, P, P2 SUFFIX



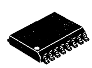
CASE 751
D SUFFIX



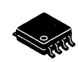
CASE 751A
D SUFFIX



CASE 751B
D SUFFIX



CASE 751G
DW SUFFIX



CASE 904
F SUFFIX

Power Supply Circuits

In Brief . . .

In most electronic systems, some form of voltage regulation is required. In the past, the task of voltage regulator design was tediously accomplished with discrete devices, and the results were quite often complex and costly. Today, with bipolar monolithic regulators, this task has been significantly simplified. The designer now has a wide choice of fixed, low V_{Diff} and adjustable type voltage regulators. These devices incorporate many built–in protection features, making them virtually immune to the catastrophic failures encountered in older discrete designs.

The switching power supply continues to increase in popularity and is one of the fastest growing markets in the world of power conversion. They offer the designer several important advantages over linear series–pass regulators. These advantages include significant advancements in the areas of size and weight reduction, improved efficiency, and the ability to perform voltage step–up, step–down, and voltage–inverting functions. Motorola offers a diverse portfolio of full featured switching regulator control circuits which meet the needs of today's modern compact electronic equipment.

Power supplies, MPU/MCU–based systems, industrial controls, computer systems and many other product applications are requiring power supervisory functions which monitor voltages to ensure proper system operation. Motorola offers a wide range of power supervisory circuits that fulfill these needs in a cost effective and efficient manner. MOSFET drivers are also provided to enhance the drive capabilities of first generation switching regulators or systems designed with CMOS/TTL logic devices. These drivers can also be used in dc–to–dc converters, motor controllers or virtually any other application requiring high speed operation of power MOSFETs.

Page

Linear Voltage Regulators

Fixed Output

These low cost monolithic circuits provide positive and/or negative regulation at currents from 100 mA to 3.0 A. They are ideal for on–card regulation employing current limiting and thermal shutdown. Low V_{Diff} devices are offered for battery powered systems.

Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Table 1. Linear Voltage Regulators

Device	V_{out}	25°C Tol. ±%	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out}) / °C	Suffix/ Package
Fixed Voltage, 3–Terminal Regulators, 0.1 Amperes								
LM2931*/A–5.0*	5.0	5.0/3.8	40	0.16	0.6	1.0	0.2	D/751, D2T/936, DT, DT–1, T/221A, Z
LP2950C*/AC*	3.0	0.5	30	0.38	0.2/0.1	0.2/0.1	0.04	DT–3.0, Z–3.0
	3.3							DT–3.3, Z–3.3
	5.0							DT–5.0, Z–5.0
MC78LXXC/AC/AB*	5.0, 8.0, 9.0	8.0/4.0	30	1.7	4.0/3.0	1.2	0.2	D/751, P/29
MC78LXXC/AC/AB*	12, 15, 18	8.0/4.0	35	1.7	2.0	1.0	0.2	D/751, P/29
MC78L24C/AC/AB*	24	8.0/4.0	40	1.7	2.0	1.0	0.2	D/751, P/29
MC79L05C/AC/AB*	–5.0	8.0/4.0	30	1.7	4.0/3.0	1.2	0.2	D/751, P/29
MC79LXXC/AC/AB*	–(12, 15, 18)	8.0/4.0	35	1.7	2.0	1.0	0.2	D/751, P/29
MC79L24C/AC/AB*	–24	8.0/4.0	40	1.7	2.0	1.0	0.2	D/751, P/29
MC33160**	5.0	5.0	40	2.0	0.8	1.0	–	P/626
Fixed Voltage, 3–Terminal Regulators, 0.5 Amperes								
MC78MXXB*/C	5.0, 6.0, 8.0, 12	4.0	35	2.0	1.0	2.0	±0.04	DT, DT–1, T/221A
MC78MXXB*/C	15, 18	4.0	35	2.0	1.0	2.0	±0.04	DT, DT–1, T/221A
MC78MXXB*/C	20, 24	4.0	40	2.0	0.25	2.0	±0.04	DT, DT–1, T/221A
MC79MXXB*/C	–(5.0, 8.0, 12, 15)	4.0	35	1.1	1.0	2.0	–0.07 to ±0.04	DT, DT–1, T/221A
MC33267*	5.05	2.0	40	0.58	1.0	1.0	–	D2T/936A, T/314D, TV
Fixed Voltage, 3–Terminal Medium Dropout Regulators, 0.8 Amperes								
MC33269–XX*	3.3, 5.0, 12	1.0	20	1.0	0.3	1.0	–	D/751, DT, T/221A
MC34268	2.85	1.0	15	0.95	0.3	1.0	–	D/751, DT

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C
** T_A = –40° to +85°C

Table 1. Linear Voltage Regulators (continued)

Device	V_{out}	25°C Tol. ±%	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out})/°C	Suffix/ Package
Fixed Voltage, 3–Terminal Regulators, 1.0 Amperes								
MC78XXB*/C/AC	5.0, 6.0, 8.0, 12, 18	4.0/2.0	35	2.0	2.0/1.0	2.0	–0.06 to –0.22	D2T/936, T/221A
MC7824B*/C/AC	24	4.0/2.0	40	2.0	2.0/1.0	2.0/0.4	0.125	D2T/936, T/221A
MC79XXC/AC	–(5.0, 5.2, 6.0)	4.0/2.0	35	2.0	2.0/1.0	2.0	–0.2	D2T/936, T/221A
MC79XXC/AC	–(8.0, 12, 15, 18)	4.0/2.0	35	2.0	2.0/1.0	2.0/1.25	–0.12 to –0.06	D2T/936, T/221A
MC7924C	–24	4.0	40	2.0	1.0	2.0	–0.04	D2T/936, T/221A
LM340/A–XX	5.0, 6.0, 12, 15, 18	4.0/2.0	35	1.7	1.0/0.2	1.0/0.5	±0.12	T/221A
LM340–24	24	4.0	40	1.7	1.0	1.0	±0.12	T/221S
TL780–XXC	5.0, 12, 15	1.0	35	2.0	0.10	0.5	0.012	KC
Fixed Voltage, 3–Terminal Regulators, 3.0 Amperes								
MC78TXXC/AC	5.0, 8.0, 12	4.0/2.0	35	2.5	0.5	0.6	0.04	T/221A
MC78T15C/AC	15	4.0/2.0	40	2.5	0.5	0.6	0.04	T/221A
LM323/A	5.0	4.0/2.0	20	2.3	0.5/0.3	2.0/1.0	±0.2	T/221A

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C
** T_A = –40° to +85°C

Table 2. Fixed Voltage Medium and Low Dropout Regulators

Device	V_{out}	25°C Tol. ±%	I_O (mA) Max	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out})/°C	Suffix/ Package
Fixed Voltage, Medium Dropout Regulators									
MC33267*	5.05	2.0	500	40	0.58	1.0	1.0	–	D2T/936A, T/314D, TV
MC34268	2.85	1.0	800	15	0.95	0.3	1.0		D/751, DT
MC33269–XX*	3.3, 5.0, 12			20	1.0				D/751, DT, T/221A
Fixed Voltage, Low Dropout Regulators									
LM2931*/A*	5.0	5.0/3.8	100	37	0.16	1.12	1.0	±2.5	D/751, D2T/936A, DT, DT–1, T/221A, Z

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C

Table 2. Fixed Voltage Medium and Low Dropout Regulators (continued)

Device	V_{out}	25°C Tol. ±%	I_O (mA) Max	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out})/°C	Suffix/ Package
Fixed Voltage, Low Dropout Regulators									
LP2950C*/AC*	3.0	1.0/0.5	100	30	0.38	0.2/0.1	0.2/0.1	0.2	DT–3.0, Z–3.0
	3.3								DT–3.3, Z–3.3
	5.0								DT–5.0, Z–5.0
LP2951C*/AC*	3.0	1.0/0.5	100	28.75	0.38	0.04/0.02	0.04/0.02	±1.0	D–3.0/751, N–3.0/626
	3.3								D–3.3/751, N–3.3/626
	5.0								D/751, N/626
LM2935*	5.0/5.0	5.0/5.0	500/10	60	0.45/0.55	1.0	1.0	–	D2T/936A, T/314D, TH, TV

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C

Adjustable Output

Motorola offers a broad line of adjustable output voltage regulators with a variety of output current capabilities. Adjustable voltage regulators provide users the capability of stocking a single integrated circuit offering a wide range of output voltages for industrial and communications applications. The three–terminal devices require only two external resistors to set the output voltage.

Table 3. Adjustable Output Regulators

Device	V_{out}	I_O (mA) Max	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out})/°C	Suffix/ Package
Adjustable Regulators								
LM317L/B*	2.0–37	100	40	1.9	0.07	1.5	±0.35	D/751, Z
LM2931C*	3.0–24	100	37	0.16	1.12	1.0	±2.5	D/751, D2T/936A, T/314D, TH, TV
LP2951C*/AC*	1.25–29	100	28.75	0.38	0.04/0.02	0.04/0.02	±1.0	D–3.0/751, N–3.0/626
								D–3.3/751, N–3.3/626
								D/751, N/626
MC1723C#	2.0–37	150	38	2.5	0.5	0.2	±0.033	D/751, P/646

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C
\# T_A = 0° to +70°C

Table 3. Adjustable Output Regulators (continued)

Device	V_{out}	I_O (mA) Max	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out}) / °C	Suffix/ Package
Adjustable Regulators								
LM317M/B*	1.2–37	500	40	2.1	0.04	0.5	±0.35	DT, DT–1, T/221A
LM337M/B*	–(1.2–37)	500	40	1.9	0.07	1.5	±0.3	T/221A
MC33269*	1.25–19	800	18.75	1.0	0.3	0.5	±0.4	D/751, DT, T/221A
LM317/B*	1.2–37	1500	40	2.25	0.07	1.5	±0.35	D2T/936, T/221A
LM337/B*	–(1.2–37)	1500	40	2.3	0.07	1.5	±0.3	D2T/936, T/221A
LM350/B*	1.2–33	3000	35	2.7	0.07	1.5	±0.5	T/221A

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C
\# T_A = 0° to +70°C

Special Regulators

Voltage Regulator/Supervisory

Table 4. Voltage Regulator/Supervisory

Device	V_{out} (V) Min	V_{out} (V) Max	I_O (mA) Max	V_{in} (V) Min	V_{in} (V) Max	Reg_{line} (mV) Max	Reg_{load} (mV) Max	T_A (°C)	Suffix/ Package
MC33128*	2.9	3.1	35	3.2	7.0	n/a	30	–30 to +60	D/751B
	2.9	3.1	60				40		
	2.9	3.1	20				25		
	–2.65	–2.35	1.0				20		
MC34160	4.75	5.25	100	7.0	40	40	50	0 to +70	P/648C, DW/751G
MC33160								–40 to +85	
MC33267	4.9	5.2	500	6.0	26	50	50	–40 to +105	T/314D, TH, TV
MC33169*	4.7	6.4	–	2.7	9.5	–	–	–40 to +85	DTB/948B
	6.4	7.0							
	–2.35	–2.65							

* These ICs are intended for powering cellular phone GaAs power amplifiers and can be used for other portable applications as well.

Microprocessor Voltage Regulator and Supervisory Circuit

MC34160P, DW

T_A = 0° to +70°C, Case 648C, 751G

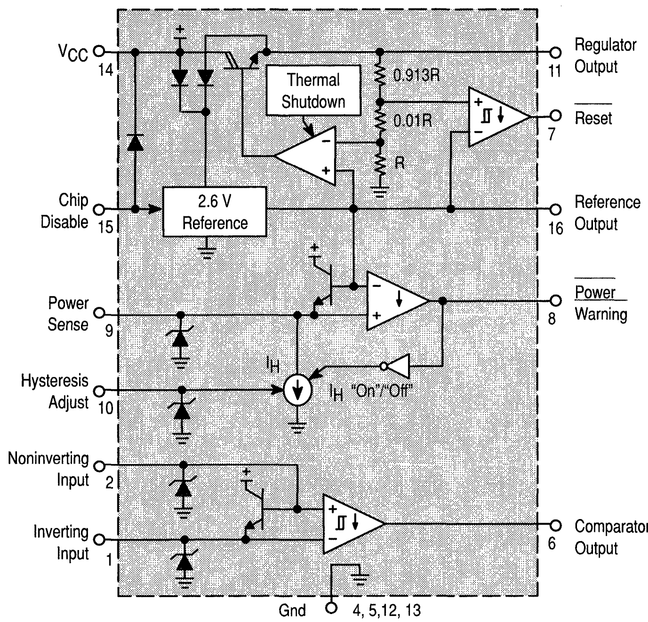
MC33160P, DW

T_A = –40° to +85°C, Case 648C, 751G

The MC34160 series is a voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a 5.0 V, 100 mA regulator with short circuit current limiting, pinned out 2.6 V bandgap reference, low voltage reset comparator, power warning comparator with programmable hysteresis, and an uncommitted comparator ideally suited for microprocessor line synchronization.

Additional features include a chip disable input for low standby current, and internal thermal shutdown for over temperature protection.

These devices are contained in a 16 pin dual–in–line heat tab plastic package for improved thermal conduction.



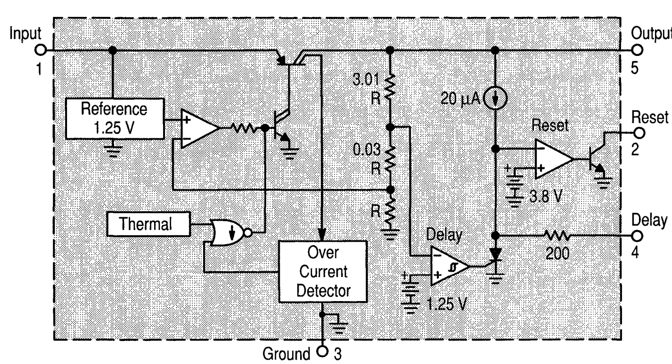
Low Dropout Regulator

MC33267T, TV

T_J = –40° to +105°C, Case 314D, 314B

The MC33267 is a positive fixed 5.0 V regulator that is specifically designed to maintain proper voltage regulation with an extremely low input–to–output voltage differential. This device is capable of supplying output currents in excess of 500 mA and contains internal current limiting and thermal shutdown protection. Also featured is an on–chip power–up reset circuit that is ideally suited for use in microprocessor based systems. Whenever the regulator output voltage is below nominal, the reset output is held low. A programmable time delay is initiated after the regulator has reached its nominal level and upon timeout, the reset output is released.

Due to the low dropout voltage specifications, the MC33267 is ideally suited for use in battery powered industrial and consumer equipment where an extension of useful battery life is desirable. This device is contained in an economical five lead TO–220 type package.



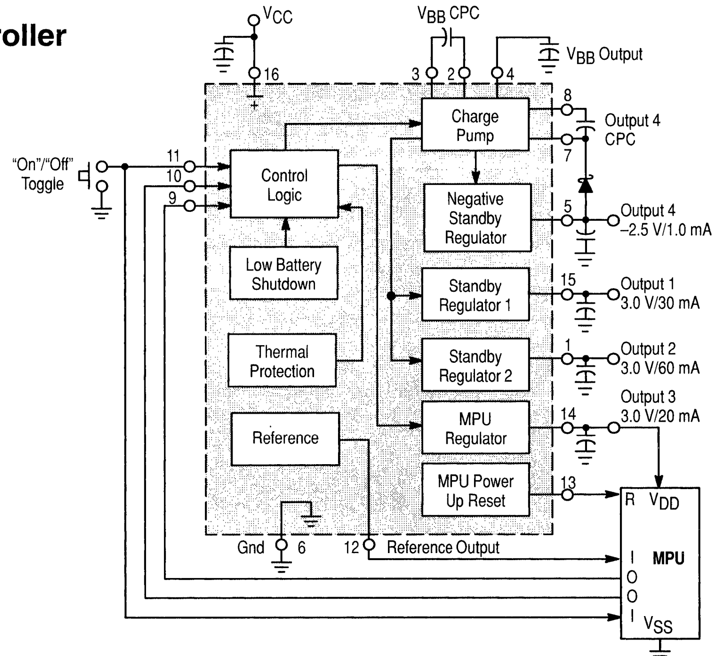
Power Management Controller

MC33128D

T_A = –30° to +60°C, Case 751B

The MC33128 is a power management controller specifically designed for use in battery powered cellular telephone and pager applications. This device contains all of the active functions required to interface the user to the system electronics via a microprocessor. This integrated circuit consists of a low dropout voltage regulator with power–up reset for MPU power, two low dropout voltage regulators for independant powering of analog and digital circuitry, and a negative charge pump voltage regulator for full depletion of gallium arsenide MESFETs.

Also included are protective system shutdown features consisting of a battery latch that is activated upon battery insertion, low battery voltage shutdown, and a thermal over temperature detector. This device is available in a 16–pin narrow body surface mount plastic package.



GaAs Amplifier Supervisory Circuit

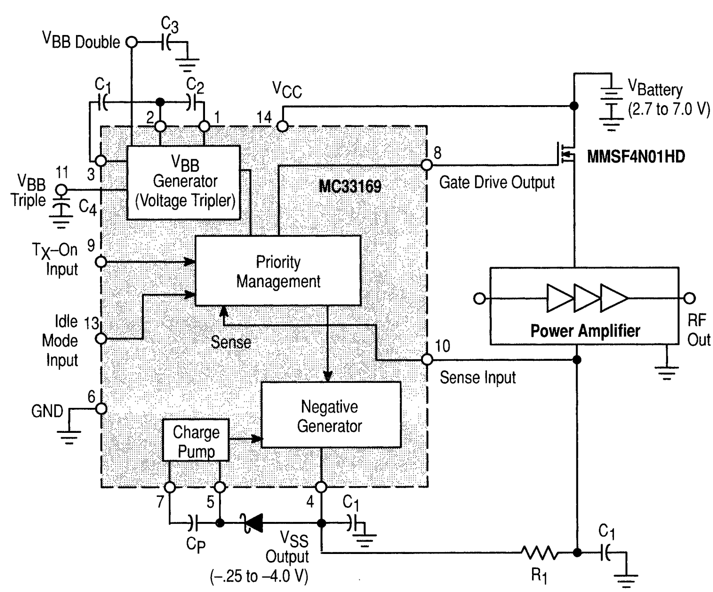
MC33169DTB

T_A = –40° to +85°C, Case 948B

The MC33169 is a support IC for GaAs Power Amplifier Enhanced FETs used in hand portable telephones such as GSM, PCN, DECT. This device provides negative voltages for full depletion of Enhanced MESFETs as well as a priority management system of drain switching, ensuring that the negative voltage is always present before turning "on" the power amplifier. Additional features include an idle mode input and a direct drive of the N–Channel drain switch transistor.

This product is available in two versions, –2.5 V and –4.0 V. The –4.0 V version is intended for supplying RF modules for GSM and DCS1800 application whereas the –2.5 V version is dedicated for DECT and PHS systems.

- Negative Regulated Output for Full Depletion of GaAs MESFETs
- Drain Switch Priority Management Circuit
- CMOS Compatible Inputs
- Idle Mode Input (Standby Mode) for Very Low Current Consumption
- Output Signal Directly Drives N–Channel FET
- Low Startup and Operating Current



SCSI Regulator

Table 5. SCSI Regulator

Device	V_{out} (V)		I_{sink} (mA)	V_{in} (V)		Reg_{line} (%)	Reg_{load} (%)	T_J (°C)	Suffix/ Package
	Min	Max		Min	Max				
MC34268	2.81	2.89	800	3.9	20	0.3	0.5	150	D/751, DT

SCSI–2 Active Terminator Regulator

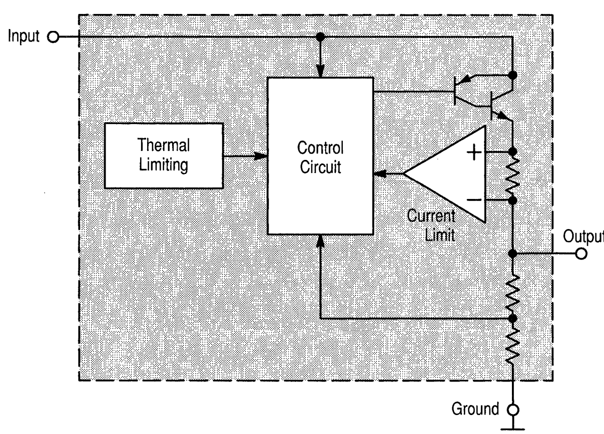
MC34268D, DT

T_J = 0° to +125°C, Case 751, 369A

The MC34268 is a medium current, low dropout positive voltage regulator specifically designed for use in SCSI–2 active termination circuits. This device offers the circuit designer an economical solution for precision voltage regulation, while keeping power losses to a minimum. The regulator consists of a 1.0 V dropout composite PNP/NPN pass transistor, current limiting, and thermal limiting. These devices are packaged in the 8–pin SOP–8 and 3–pin DPAK surface mount power packages.

Applications include active SCSI–2 terminators and post regulation of switching power supplies.

- 2.85 V Output Voltage for SCSI–2 Active Termination
- 1.0 V Dropout
- Output Current in Excess of 800 mA
- Thermal Protection
- Short Circuit Protection
- Output Trimmed to 1.4% Tolerance
- No Minimum Load Required
- Space Saving DPAK and SOP–8 Surface Mount Power Packages



Switching Regulator Control Circuits

These devices contain the primary building blocks which are required to implement a variety of switching power supplies. The product offerings fall into three major categories consisting of single–ended and double–ended controllers, plus single–ended ICs with on–chip power switch transistors. These circuits operate in voltage, current or resonant modes and are designed to drive many of the standard switching topologies. The single–ended configurations include buck, boost, flyback and forward converters. The double–ended devices control push–pull, half bridge and full bridge configurations.

Table 6. Single–Ended Controllers

These single–ended voltage and current mode controllers are designed for use in buck, boost, flyback, and forward converters. They are cost effective in applications that range from 0.1 to 200 W power output.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
500 (Uncommitted Drive Output)	7.0 to 40	Voltage	5.0 ± 1.5%	200	MC34060A	0 to +70	D/751A
							P/646
					MC33060A	–40 to +85	D/751A
							P/646
1000 (Totem Pole MOSFET Drive Output)	4.2 to 12	Current	1.25 ± 2.0%	300	MC34129	0 to +70	D/751A
							P/646
					MC33129	–40 to +85	D/751A
							P/646
	11.5 to 30		5.0 ± 2.0%	500	UC3842A	0 to +70	D/751A
							N/626
	11 to 30		5.0 ± 1.0%		UC2842A	–25 to +85	D/751A
							N/626
	8.2 to 30		5.0 ± 2.0%		UC3843A	0 to +70	D/751A
							N/626
			5.0 ± 1.0%		UC2843A	–25 to +85	D/751A
							N/626
	11.5 to 30		5.0 ± 2.0%	500 (50% Duty Cycle Limit)	UC3844	0 to +70	D/751A
							N/626
	11 to 30		5.0 ± 1.0%		UC2844	–25 to +85	D/751A
							N/626
	8.2 to 30		5.0 ± 2.0%		UC3845	0 to +70	D/751A
							N/626
			5.0 ± 1.0%		UC2845	–25 to +85	D/751A
							N/626
	11.5 to 30		5.0 ± 2.0%	500 (Improved Oscillator Specifications with Frequency Guaranteed at 250 kHz)	UC3842B	0 to +70	D/751A
							D1/751
							N/626
					UC3842BV	–40 to +105	D/751A
							D1/751
							N/626

Table 6. Single–Ended Controllers (continued)

These single–ended voltage and current mode controllers are designed for use in buck, boost, flyback, and forward converters. They are cost effective in applications that range from 0.1 to 200 W power output.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
1000 (Totem Pole MOSFET Drive Output)	11 to 30	Current	5.0 ± 1.0%	500 (Improved Oscillator Specifications with Frequency Guaranteed at 250 kHz)	UC2842B	–25 to +85	D/751A
							D1/751
							N/626
	8.2 to 30		5.0 ± 2.0%		UC3843B	0 to +70	D/751A
							D1/751
							N/626
					UC3843BV	–40 to +105	D/751A
							D1/751
							N/626
			5.0 ± 1.0%		UC2843B	–25 to +85	D/751A
							D1/751
							N/626
	11.5 to 30		5.0 ± 2.0%	500 (50% Duty Cycle Limit)	UC3844B	0 to +70	D/751A
							D1/751
							N/626
					UC3844BV	–40 to +105	D/751A
							D1/751
							N/626
	11 to 30		5.0 ± 1.0%		UC2844B	–25 to +85	D/751A
							D1/751
							N/626
	8.2 to 30		5.0 ± 2.0%		UC3845B	0 to +70	D/751A
							D1/751
							N/626
					UC3845BV	–40 to +105	D/751A
							D1/751
							N/626
			5.0 ± 1.0%		UC2845B	–25 to +85	D/751A
							D1/751
							N/626
1000 Source 1500 Sink (Split Totem Pole Bipolar Drive Output)	11 to 18		5.0 ± 6.0%		MC44602		P2/648C
2000 (Totem Pole MOSFET Drive Output)	9.2 to 30	Current or Voltage	5.1 ± 1.0%	1000	MC34023	0 to +70	DW/751G
							FN/775
							P/648
					MC33023	–40 to +105	DW/751G
							FN/775
							P/648

Table 7. Single–Ended Controllers with On–Chip Power Switch

These monolithic power switching regulators contain all the active functions required to implement standard dc–to–dc converter configurations with a minimum number of external components.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
1500 (Uncommitted Power Switch)	2.5 to 40	Voltage	1.25 ± 5.2%(1)	100	μA78S40	0 to +70	PC/648
						–40 to +85	PV/648
			1.25 ± 2.0%		MC34063A	0 to +70	D/751
							P1/626
					MC33063A	–40 to +85	D/751
							P1/626
3400 (Uncommitted Power Switch)	2.5 to 40		1.25 ± 2.0% and 5.05 ± 3.0 %		MC34163	0 to +70	P/648C, DW/751G
					MC33163	–40 to +85	
3400(2) (Dedicated Emitter Power Switch)	7.5 to 40		5.05 ± 2.0%	72 ± 12% Internally Fixed	MC34166	0 to +70	D2T/936A, TH, TV, T/314D
					MC33166	–40 to +85	
5500(3) (Dedicated Emitter Power Switch)					MC34167	0 to +70	
					MC33167	–40 to +85	

(1) Tolerance applies over the specified operating temperature range.
(2) Guaranteed minimum, typically 4300 mA.
(3) Guaranteed minimum, typically 6500 mA.

Table 8. Very High Voltage Single–Ended Controller with On–Chip Power Switch

This monolithic high voltage switching regulator is specifically designed to operate from a rectified ac line voltage source. Included are an on–chip high voltage power switch, active off–line startup circuitry and a full featured PWM controller with fault protection.

Power Switch Maximum Rating		Startup Input Max (V)	Operating Mode	Feedback Threshold (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
V_{DS} (V)	I_{DS} (mA)							
500	2000	250	Voltage	2.6 ± 3.1%	1000	MC33362	–25 to +125	DW/751N

Table 9. Double–Ended Controllers

These double–ended voltage, current and resonant mode controllers are designed for use in push–pull, half–bridge, and full–bridge converters. They are cost effective in applications that range from 100 to 2000 watts power output.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
500 (Uncommitted Drive Outputs)	7.0 to 40	Voltage	5.0 ± 5.0%[1]	200	TL494	0 to +70	CN/648
						–25 to +85	IN/648
			5.0 ± 1.5%	300	TL594	0 to +70	CN/648
						–25 to +85	IN/648
± 500 (Totem Pole MOSFET Drive Outputs)	8.0 to 40		5.1 ± 2.0%	400	SG3525A	0 to +70	N/648
					SG3527A		N/648
± 200 (Totem Pole MOSFET Drive Outputs)			5.0 ± 2.0%		SG3526	0 to +125[2]	N/707
±1500 (Totem Pole MOSFET Drive Outputs)	9.6 to 20	Resonant (Zero Current)	5.1 ± 2.0%	1000	MC34066	0 to +70	DW/751G
							P/648
					MC33066	–40 to +85	DW/751G
							P/648
		Resonant (Zero Voltage)		2000	MC34067	0 to +70	DW/751G
							P/648
					MC33067	–40 to +85	DW/751G
							P/648
2000 (Totem Pole MOSFET Drive Outputs)	9.2 to 30	Current or Voltage	5.1 ± 1.0%	1000	MC34025	0 to +70	DW/751G
							FN/775
							P/648
					MC33025	–40 to +105	DW/751G
							FN/775
							P/648

(1) Tolerance applies over the specified operating temperature range.
(2) Junction Temperature Range.

High Voltage Switching Regulator

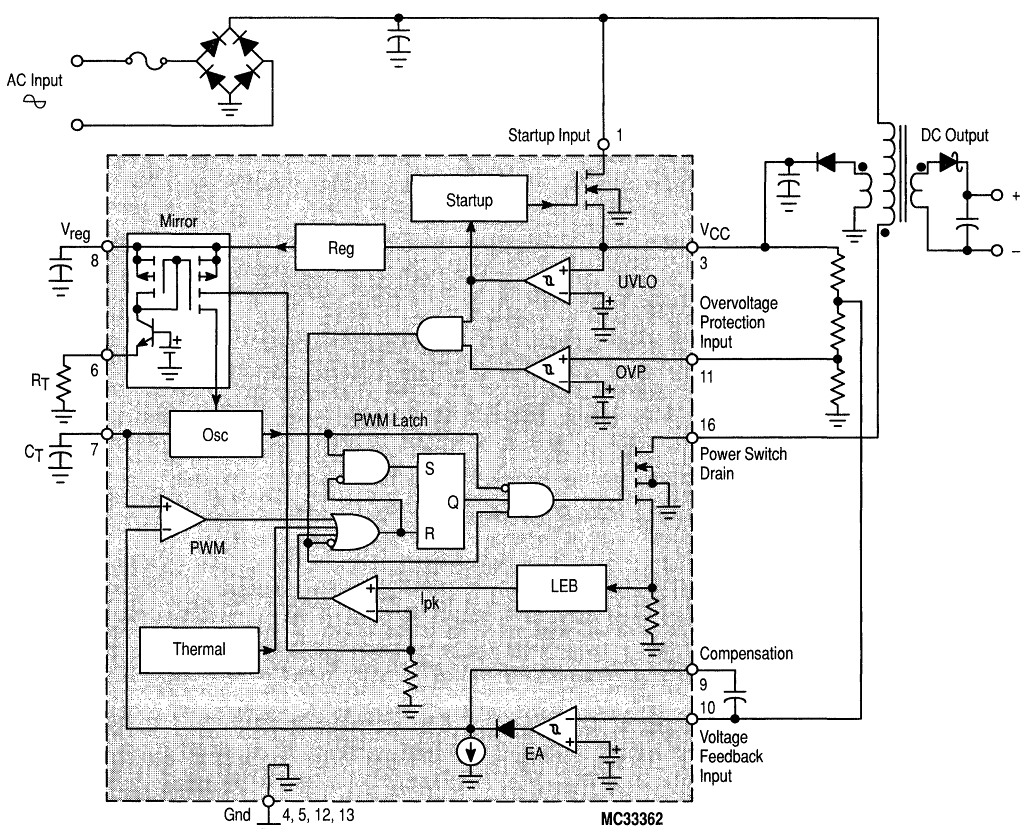
MC33362DW

T_J = –25° to +125°C, Case 751N

The MC33362 is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 120 Vac line source. This integrated circuit features an on–chip 500 V/2.0 A SenseFET power switch, 250 V active off–line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle–by–cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16 lead wide body surface mount package.

- On–Chip 500 V, 2.0 A SenseFET Power Switch
- Rectified 120 Vac Line Source Operation
- On–Chip 250 V Active Off–Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle–By–Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed 1.0% Internal Bandgap Reference
- Internal Thermal Shutdown

20 W Off–Line Converter



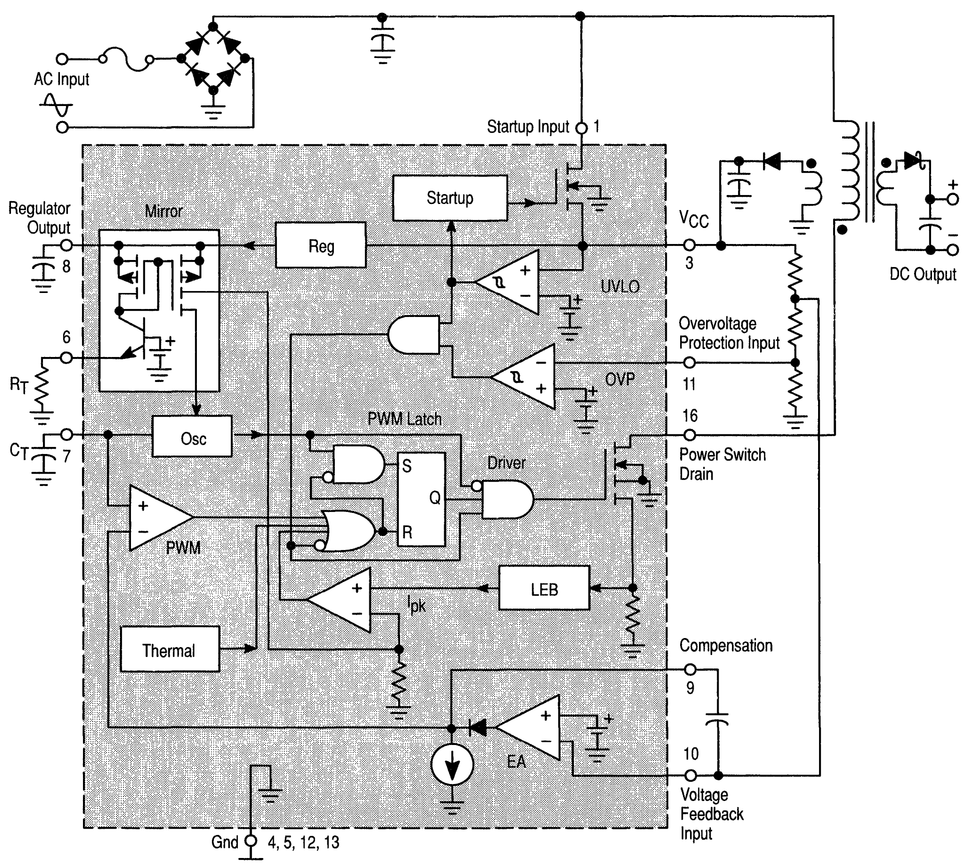
High Voltage Switching Regulator

MC33363DW

T_J = –25° to +125°C, Case 751N

The MC33363 is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 240 Vac line source. This integrated circuit features an on–chip 700 V/1.0 A SenseFET power switch, 450 V active off–line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle–by–cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16–lead wide body surface mount package.

- On–Chip 700 V, 1.0 A SenseFET Power Switch
- Rectified 240 Vac Line Source Operation
- On–Chip 450 V Active Off–Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle–By–Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown



Special Switching Regulator Controllers

These high performance dual channel controllers are optimized for off–line, ac–to–dc power supplies and dc–to–dc converters in the flyback topology. They also have undervoltage lockout voltages which are optimized for off–line and lower voltage dc–to–dc converters, respectively. Applications include desktop computers, peripherals, televisions, games, and various consumer appliances.

Table 10. Dual Channel Controllers

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
500	4.0	Voltage	1.25 ± 2.0%	700	MC34270	0 to +70	FB/873A
					MC34271		
±1000 (Totem Pole MOSFET Drive Outputs)	11 to 20	Current	5.0 ± 2.6%	500	MC34065	0 to +70	DW–H/751G
							P–H/648
					MC33065	–40 to +85	DW–H/751G
							P–H/648
	8.2 to 20				MC34065	0 to +70	DW–L/751G
							P–L/648
					MC33065	–40 to +85	DW–L/751G
							P–L/648

Table 11. Universal Microprocessor Power Supply Controllers

A versatile power supply control circuit for microprocessor–based systems, this device is mainly intended for automotive applications and battery powered instruments. The circuit provides a power–on reset delay and a Watchdog feature for orderly microprocessor operation.

Regulated Outputs	Output Current (mA)	V_{CC} (V) Min	Max	Reference (V)	Key Supervisory Features	Device	T_A (°C)	Package
E^2PROM Programmable Output: 24 V (Write Mode) 5.0 V (Read Mode)	150 peak	6.0	35	2.5 ± 3.2%	MPU Reset and Watchdog Circuit	TCF5600 TCA5600	–40 to +85	707

Table 12. Power Factor Controllers

I_O (mA) Max	Minimum Operating Voltage Range (V)	Maximum Startup Voltage (V)	Reference (V)	Features	Device	T_A (°C)	Suffix/ Package
± 500 (Totem Pole MOSFET Drive Outputs)	9.0 to 30	30	2.5 ± 1.4%	Undervoltage Lockout, Internal Startup Timer	MC34261	0 to +70	D/751
							P/626
					MC33261	–40 to +85	D/751
							P/626
				Overvoltage Comparator, Undervoltage Lockout, Internal Startup Timer	MC34262	0 to +85	D/751
							P/626
					MC33262	–40 to +105	D/751
							P/626
1500 (CMOS Totem Pole MOSFET Drive Outputs)	9.0 to 16	500	5.0 ± 1.5%	Off–Line High Voltage Startup Overvoltage Comparator, Undervoltage Lockout, Timer, Low Load Detect	MC33368	–25 to +125	D/751

Power Factor Controllers

MC34262D, P

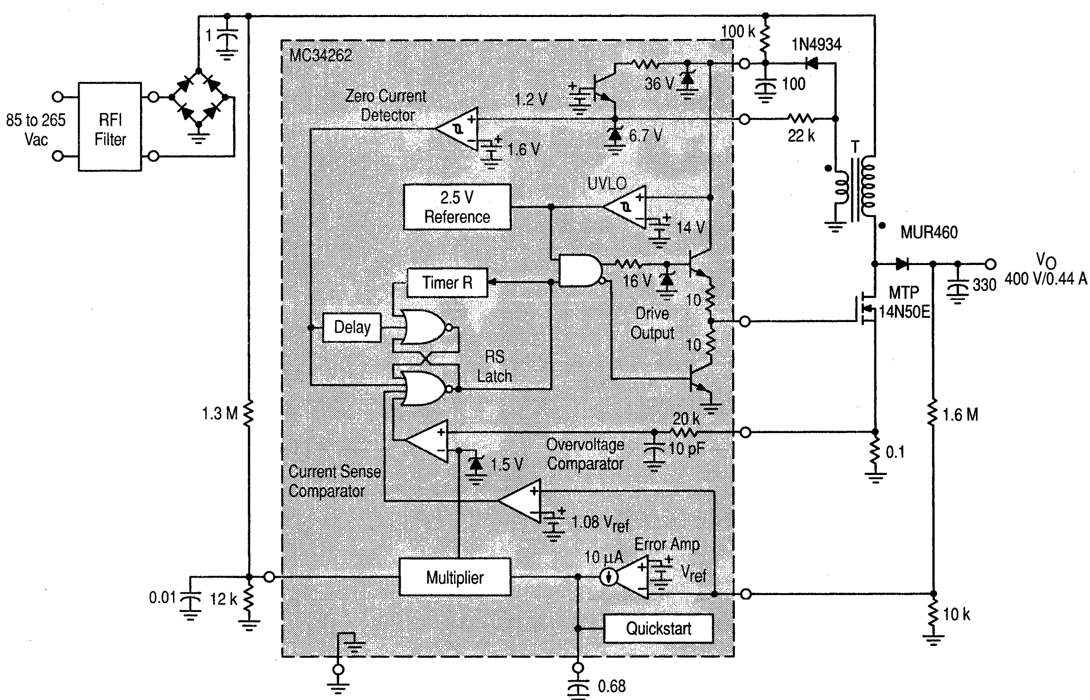
T_A = 0° to +85°C, Case 751, 626

MC33262D, P

T_A = –40° to +105°C, Case 751, 626

The MC34262, MC33262 series are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off–line power converter applications. These integrated circuits feature an internal startup timer for stand alone applications, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, transconductance error amplifier, quickstart circuit for enhanced startup, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of an overvoltage comparator to eliminate runaway output voltage due to load removal, input undervoltage lockout with hysteresis, cycle–by–cycle current limiting, multiplier output clamp that limits maximum peak switch current, an RS latch for single pulse metering, and a drive output high state clamp for MOSFET gate protection. These devices are available in dual–in–line and surface mount plastic packages.



Power Factor Controllers (continued)

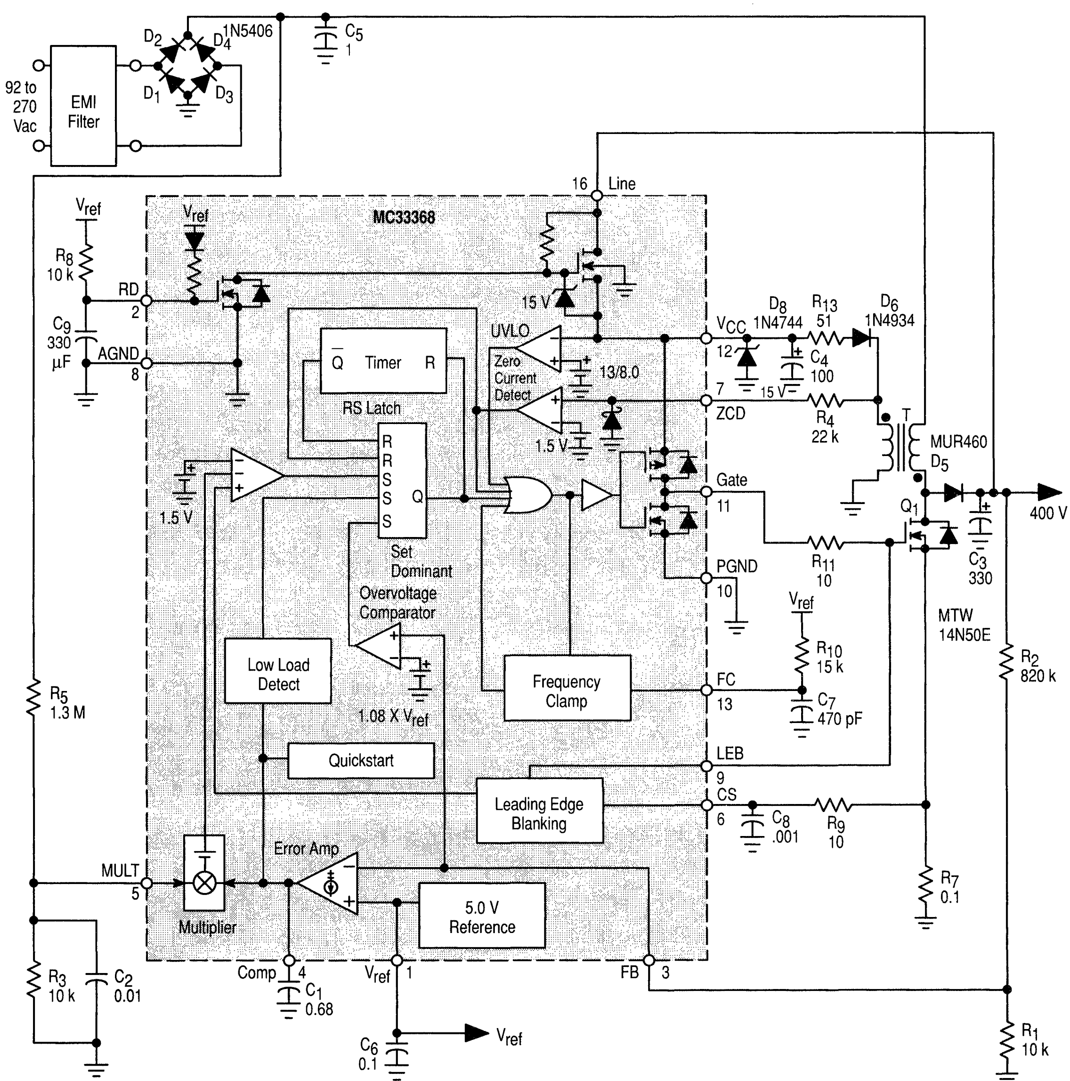
MC33368D

T_J = –25° to +125°C, Case 751K

The MC33368 is an active power factor controller that functions as a boost preconverter in off–line power supply applications. MC33368 is optimized for low power, high density power supplies requiring minimum board area, reduced component count, and low power dissipation. The narrow body SOIC package provides a small footprint. Integration of the high voltage startup saves approximately 0.7 W of power compared to resistor bootstrapped circuits.

The MC33368 features a watchdog timer to initiate output switching, a one quadrant multiplier to force the line current to follow the instantaneous line voltage, a zero current detector to ensure critical conduction operation, a transconductance error amplifier, a current sensing comparator, a 5.0 V reference, an undervoltage lockout (UVLO) circuit which monitors the V_{CC} supply voltage, and a CMOS driver for driving MOSFETs. The MC33368 also includes a programmable output switching frequency clamp. Protection features include an output overvoltage comparator to minimize overshoot, a restart delay timer, and cycle–by–cycle current limiting.

- Lossless Off–Line Startup
- Output Overvoltage Comparator
- Leading Edge Blanking (LEB) for Noise Immunity
- Watchdog Timer to Initiate Switching
- Restart Delay Timer



Supervisory Circuits

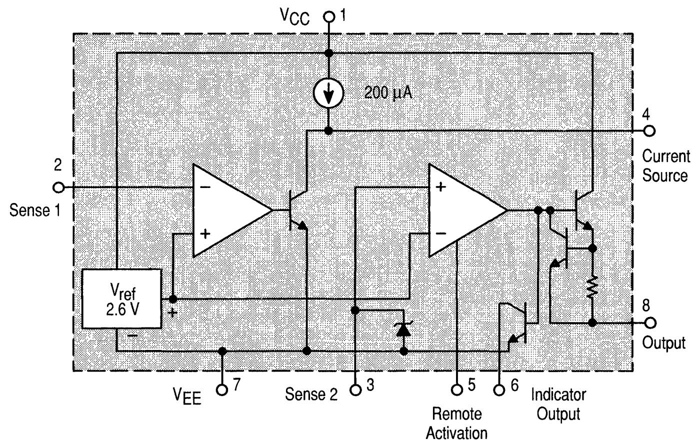
A variety of Power Supervisory Circuits are offered. Overvoltage sensing circuits which drive "Crowbar" SCRs are provided in several configurations from a low cost three–terminal version to 8–pin devices which provide pin–programmable trip voltages or additional features, such as an indicator output drive and remote activation capability. An over/undervoltage protection circuit is also offered.

Overvoltage Crowbar Sensing Circuit

MC3423P1, D

T_A = 0° to +70°C, Case 626, 751

This device can protect sensitive circuitry from power supply transients or regulator failure when used with an external "Crowbar" SCR. The device senses voltage and compares it to an internal 2.6 V reference. Overvoltage trip is adjustable by means of an external resistive voltage divider. A minimum duration before trip is programmable with an external capacitor. Other features include a 300 mA high current output for driving the gate of a "Crowbar" SCR, an open–collector indicator output and remote activation capability.

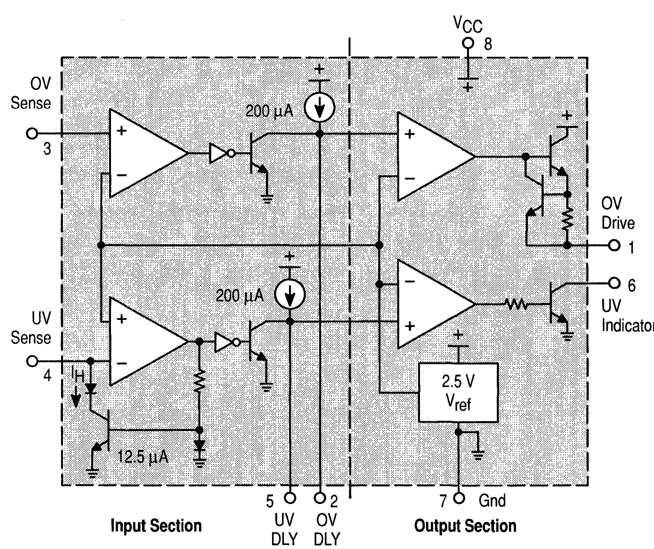


Over/Undervoltage Protection Circuit

MC3425P1

T_A = 0° to +70°C, Case 626

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. This device features dedicated over and undervoltage sensing channels with independently programmable time delays. The overvoltage channel has a high current drive output for use in conjunction with an external SCR "Crowbar" for shutdown. The undervoltage channel input comparator has hysteresis which is externally programmable, and an open–collector output for fault indication.



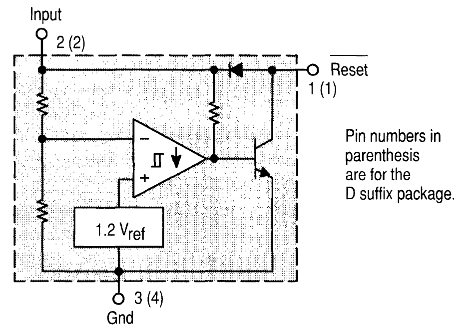
Undervoltage Sensing Circuit

MC34064P–5, D–5
T_A = 0° to +70°C, Case 29, 751

MC33064P–5, D–5
T_A = –40° to +85°C, Case 29, 751

MC34164P–3, P–5, D–3, D–5
T_A = 0° to +70°C, Case 29, 751

MC33164P–3, P–5, D–3, D–5
T_A = –40° to +85°C, Case 29, 751



The MC34064 and MC34164 are two families of undervoltage sensing circuits specifically designed for use as reset controllers in microprocessor–based systems. They offer the designer an economical solution for low voltage detection with a single external resistor. Both parts feature a trimmed bandgap reference, and a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation.

The two families of undervoltage sensing circuits taken together, cover the needs of the most commonly specified power supplies used in MCU/MPU systems. Key parameter specifications of the MC34164 family were chosen to complement the MC34064 series. The table summarizes critical parameters of both families. The MC34064 fulfills the needs of a 5.0 V ± 5% system and features a tighter hysteresis specification. The MC34164 series covers 5.0 V ± 10% and 3.0 V ± 5% power supplies with significantly lower power consumption, making them ideal for applications where extended battery life is required such as consumer products or hand held equipment.

Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.

The MC34164 is specifically designed for battery powered applications where low bias current (1/25th of the MC34064's) is an important characteristic.

Table 13. Undervoltage Sense/Reset Controller Features

MC34X64 devices are specified to operate from 0° to +70°C, and MC33X64 devices operate from –40° to +85°C.

Device	Standard Power Supply Supported	Typical Threshold Voltage (V)	Typical Hysteresis Voltage (V)	Minimum Output Sink Current (mA)	Power Supply Input Voltage Range (V)	Maximum Quiescent Input Current	Suffix/ Package
MC34064/MC33064	5.0 V ± 5%	4.6	0.02	10	1.0 to 10	500 μA @ V_{in} = 5.0 V	P–5/29 D–5/751
MC34164/MC33164	5.0 V ± 10%	4.3	0.09	7.0	1.0 to 12	20 μA @ V_{in} = 5.0 V	P–5/29 D–5/751
	3.0 V ± 5%	2.7	0.06	6.0	1.0 to 12	15 μA @ V_{in} = 3.0 V	P–3/29 D–3/751

Supervisory Circuits (continued)

Universal Voltage Monitor

MC34161P, D

T_A = 0° to +70°C, Case 626, 751

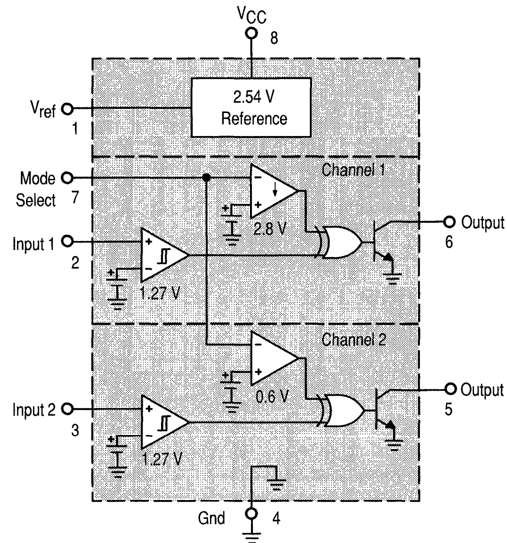
MC33161P, D

T_A = –40° to +85°C, Case 626, 751

The MC34161, MC33161 series are universal voltage monitors intended for use in a wide variety of voltage sensing applications. These devices offer the circuit designer an economical solution for positive and negative voltage detection. The circuit consists of two comparator channels each with hysteresis, a unique Mode Select Input for channel programming, a pinned out 2.54 V reference, and two open collector outputs capable of sinking in excess of 10 mA. Each comparator channel can be configured as either inverting or noninverting by the Mode Select Input. This allows over, under, and window detection of positive and negative voltages. The minimum supply voltage needed for these devices to be fully functional is 2.0 V for positive voltage sensing and 4.0 V for negative voltage sensing.

Applications include direct monitoring of positive and negative voltages used in appliance, automotive, consumer, and industrial equipment.

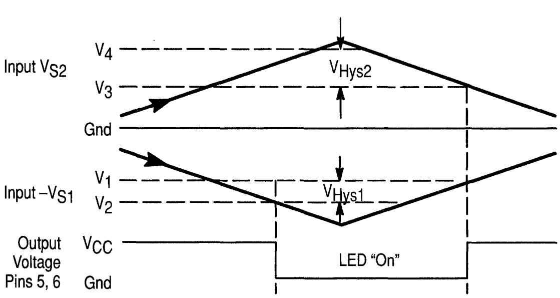
- Unique Mode Select Input Allows Channel Programming
- Over, Under, and Window Voltage Detection
- Positive and Negative Voltage Detection
- Fully Functional at 2.0 V for Positive Voltage Sensing and 4.0 V for Negative Voltage Sensing
- Pinned Out 2.54 V Reference with Current Limit Protection
- Low Standby Current
- Open Collector Outputs for Enhanced Device Flexibility

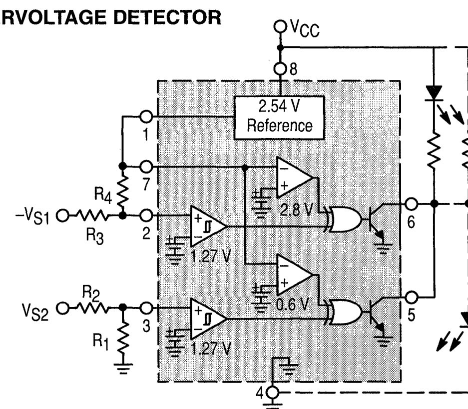


TRUTH TABLE

Mode Select Pin 7	Input 1 Pin 2	Output 1 Pin 6	Input 2 Pin 3	Output 2 Pin 5	Comments
GND	0 1	0 1	0 1	0 1	Channels 1 & 2: Noninverting
V_{ref}	0 1	0 1	0 1	1 0	Channel 1: Noninverting Channel 2: Inverting
V_{CC} (>2.0 V)	0 1	1 0	0 1	1 0	Channels 1 & 2: Inverting

POSITIVE AND NEGATIVE OVERVOLTAGE DETECTOR





Battery Management Circuits

Battery Charger ICs

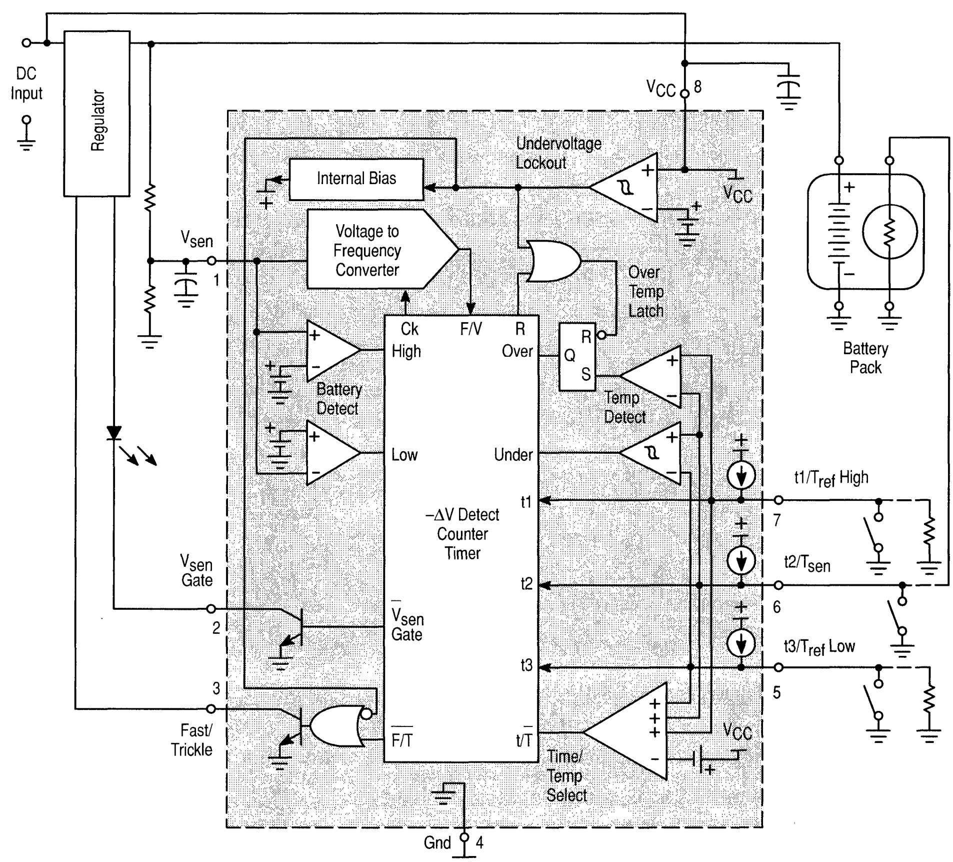
Battery Fast Charge Controller

MC33340D

T_A = –25° to +85°C, Case 751

The MC33340 is a monolithic control IC that is specifically designed as a fast charge controller for Nickel Cadmium (NiCd) and Nickel Metal Hydride (NiMH) batteries. This device features negative slope voltage detection as the primary means for fast charge termination. Accurate detection is ensured by an output that momentarily interrupts the charge current for precise voltage sampling. An additional secondary backup termination method can be selected that consists of either a programmable time or temperature limit. Protective features include battery over– and undervoltage detection, latched over temperature detection, and power supply input undervoltage lockout with hysteresis. Provisions for entering a rapid test mode are available for enhanced end product testing. This device is available in an economical 8 lead surface mount package.

- Negative Slope Voltage Detection
- Accurate Zero Current Battery Voltage Sensing
- Programmable 1 to 4 Hour Fast Charge Time Limit
- Programmable Over/Under Temperature Detection
- Battery Over– and Undervoltage Fast Charge Protection
- Rapid System Test Mode
- Power Supply Input Undervoltage Lockout with Hysteresis
- Operating Voltage Range of 3.0 V to 18 V



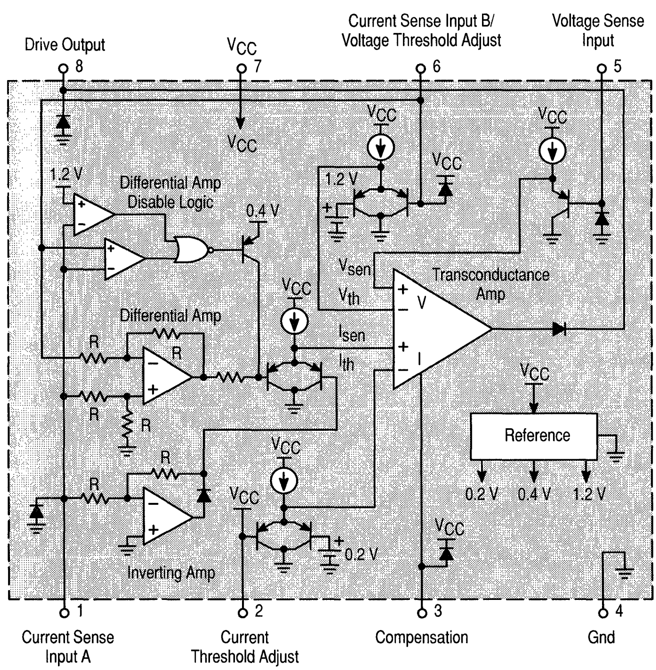
Power Supply Battery Charger Regulation Control Circuit

MC33341P, D

T_A = –40° to +85°C, Case 626, 751

The MC33341 is a monolithic regulation control circuit that is specifically designed to close the voltage and current feedback loops in power supply and battery charger applications. This device features the unique ability to perform source high–side, load high–side, source low–side, and load low–side current sensing, each with either an internally fixed or externally adjustable threshold. The various current sensing modes are accomplished by a means of selectively using the internal differential amplifier, inverting amplifier, or a direct input path. Positive voltage sensing is performed by an internal voltage amplifier. The voltage amplifier threshold is internally fixed and can be externally adjusted in all low–side current sensing applications. An active high drive output is provided to directly interface with economical optoisolators for isolated output power systems. This device is available in 8 lead dual–in–line and surface mount packages.

- Differential Amplifier for High–Side Source and Load Current Sensing
- Inverting Amplifier for Source Return Low–Side Current Sensing
- Noninverting Input Path for Load Low–Side Current Sensing
- Fixed or Adjustable Current Threshold in all Current Sensing Modes
- Positive Voltage Sensing in all Current Sensing Modes
- Fixed Voltage Threshold in all Current Sensing Modes
- Adjustable Voltage Threshold in all Low–Side Current Sensing Modes
- Output Driver Directly Interfaces with Economical Optoisolators
- Operating Voltage Range of 2.3 V to 18 V



Battery Pack ICs

1 to 4 Cells Lithium Battery Safety IC

MC33344DW

T_A = –40° to +85°C, Case 751D

The MC33344 is a Lithium Battery Safety Integrated Circuit designed to control the charge and discharge voltage safety limits of one to four lithium–ion or lithium polymer rechargeable cells. This device is designed to be placed inside the battery pack together with the cells and other external components, to form a smart battery pack. Its main purpose is to ensure safe battery pack charging and discharging.

The circuit also protects the integrity of the Li–ion cells. In effect, it avoids the degradation of the cells in case of overdischarge by causing the battery pack to go in a zero current SLEEPMODE™ state. This state interrupts any further leakage of the cells.

Integrated into the MC33344 are two seriesed N–FETs designed to interrupt the battery charge or discharge current.

Charge Control:

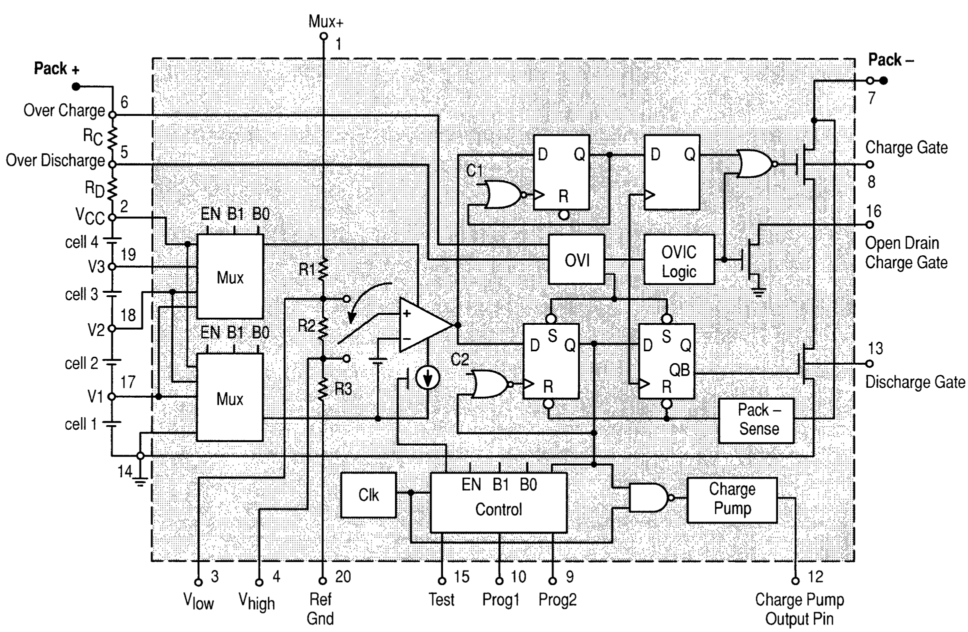
- Fully programmable for 1 to 4 Lithium–Ion (Li–ion) or Lithium–Polymer Rechargeable Cells
- Precision Cell Voltage Measurement with an Accuracy of 1.0%
- Programmable Voltage and Current Limits
- Automatic Cell Balancing for Optimization of the Charge of each Cell

Protection Features:

- Zero Current Sleepmode in Order to Avoid the Degradation of a Cell in the Event of an Undervoltage Condition
- Overvoltage and Undervoltage Cell Protection
- Overcurrent Protection during Charge and Discharge

Designed for Smart Battery Pack Integration:

- Surface Mount 20 Pin Package
- On–Chip Series N–FETs capable of up to 1.5 A Load Current



1 to 4 Cells Lithium Battery Safety IC

MC33345DTB

T_A = –40° to +85°C, Case 948E

The MC33345 is a Lithium Battery Safety Integrated Circuit designed to control the charge and discharge voltage safety limits of one to four lithium–ion or lithium polymer rechargeable cells. This device is designed to be placed inside the battery pack together with the cells and other external components, to form a smart battery pack. Its main purpose is to ensure safe battery pack charging and discharging.

The circuit also protects the integrity of the Li–ion cells. In effect, it avoids the degradation of the cells in case of overdischarge by causing the battery pack to go in a zero current SLEEPMODE™ state. This state interrupts any further leakage of the cells.

Charge Control:

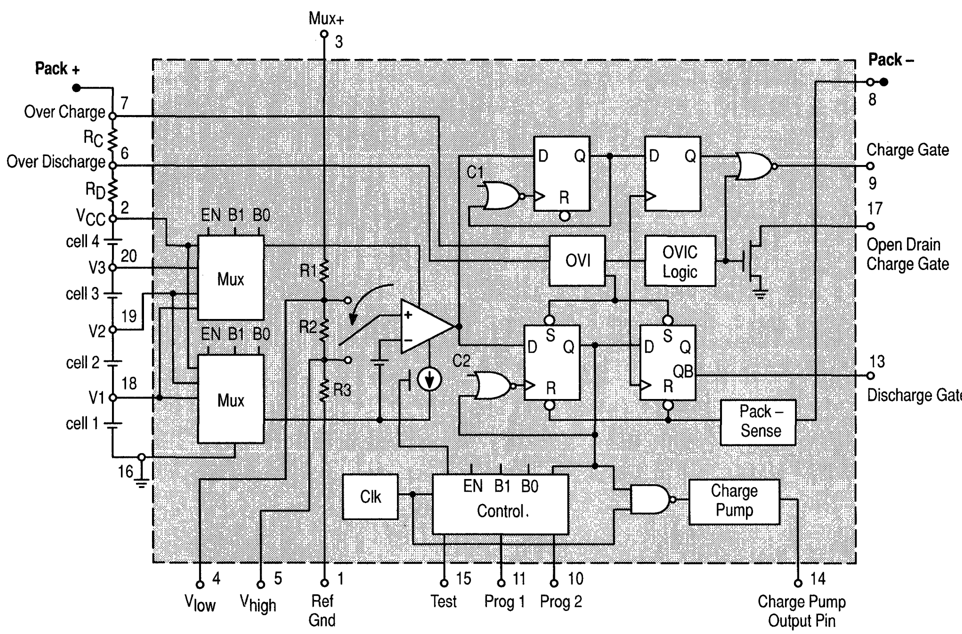
- Fully programmable for 1 to 4 Lithium–Ion (Li–ion) or Lithium–Polymer Rechargeable Cells
- Precision Cell Voltage Measurement with an Accuracy of 1.0%
- Programmable Voltage and Current Limits
- Automatic Cell Balancing for Optimization of the Charge of each Cell

Protection Features:

- Zero Current Sleepmode in Order to Avoid the Degradation of a Cell in the Event of an Undervoltage Condition
- Overvoltage and Undervoltage Cell Protection
- Overcurrent Protection during Charge and Discharge

Designed for Smart Battery Pack Integration:

- Low Profile 20 Pin Surface Mount Package



MOSFET/IGBT Drivers

High Speed Dual Drivers

(Inverting)

MC34151P, D

T_A = 0° to +70°C, Case 626, 751

MC33151P, D

T_A = –40° to +85°C, Case 626, 751

(Noninverting)

MC34152P, D

T_A = 0° to +70°C, Case 626, 751

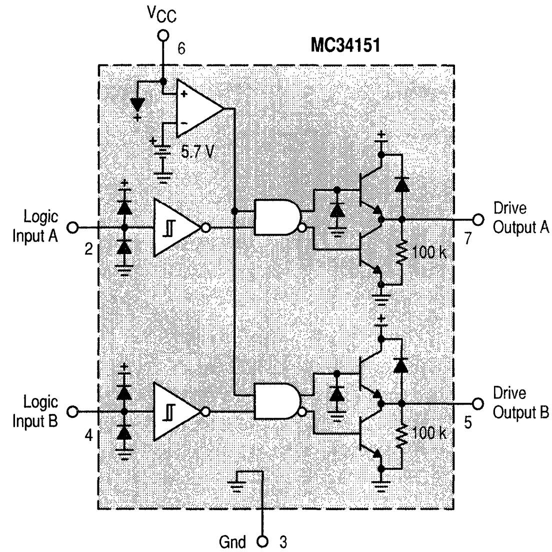
MC33152P, D

T_A = –40° to +85°C, Case 626, 751

These two series of high speed dual MOSFET driver ICs are specifically designed for applications requiring low current digital circuitry to drive large capacitive loads at high slew rates. Both series feature a unique undervoltage lockout function which puts the outputs in a defined low state in an undervoltage condition. In addition, the low "on" state resistance of these bipolar drivers allows significantly higher output currents at lower supply voltages than with competing drivers using CMOS technology.

The MC34151 series is pin–compatible with the MMH0026 and DS0026 dual MOS clock drivers, and can be used as drop–in replacements to upgrade system performance. The MC34152 noninverting series is a mirror image of the inverting MC34151 series.

These devices can enhance the drive capabilities of first generation switching regulators or systems designed with CMOS/TTL logic devices. They can be used in dc–to–dc converters, motor controllers, capacitor charge pump converters, or virtually any other application requiring high speed operation of power MOSFETs.



Single IGBT Driver

MC33153P, D

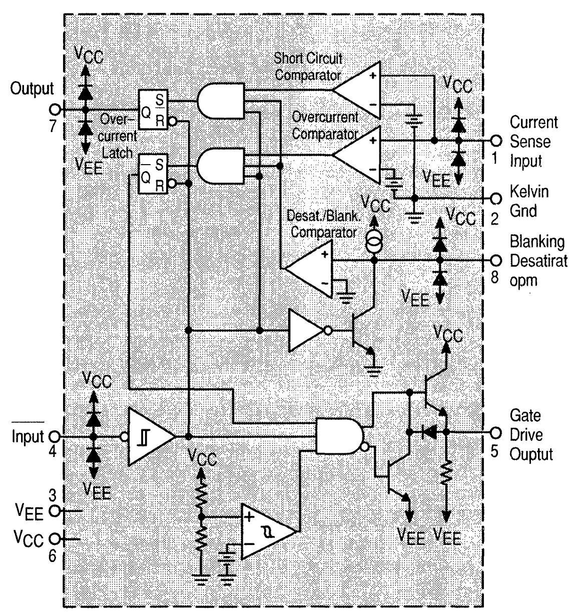
T_A = –40° to +105°C, Case 626, 751

The MC33153 is specifically designed to drive the gate of an IGBT used for ac induction motors. It can be used with discrete IGBTs and IBGT modules up to 100 A.

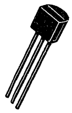
Typical applications are ac induction motor control, brushless dc motor control, and uninterruptable power supplies.

These devices are available in dual–in–line and surface mount packages and include the following features:

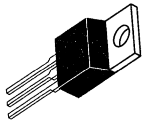
- High Current Output Stage : 1.0 A Source – 2.0 A Sink
- Protection Circuits for Both Conventional and SenseIGBTs
- Current Source for Blanking Timing
- Protection Against Overcurrent and Short Circuit
- Undervoltage Lockout Optimized for IGBT's
- Negative Gate Drive Capability



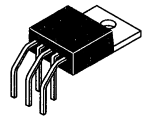
Power Supply Circuits Package Overview



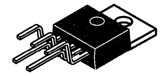
CASE 29
P, Z SUFFIX



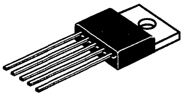
CASE 221A
T, KC SUFFIX



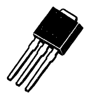
CASE 314A
TH SUFFIX



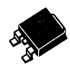
CASE 314B
TV SUFFIX



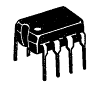
CASE 314D
T SUFFIX



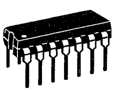
CASE 369
DT–1 SUFFIX



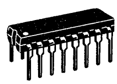
CASE 369A
DT SUFFIX



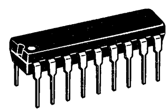
CASE 626
N, P, P1 SUFFIX



CASE 646
P SUFFIX

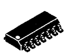


CASES 648, 648C
N, P, P2 SUFFIX



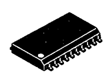
CASE 707
N SUFFIX

CASE 751
D, D1 SUFFIX

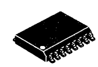


CASE 751A
D SUFFIX

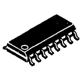
CASE 751B
D SUFFIX



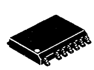
CASE 751D
DW SUFFIX



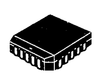
CASE 751G
DW SUFFIX



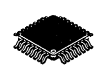
CASE 751K
D SUFFIX



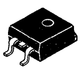
CASE 751N
DW SUFFIX



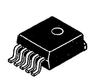
CASE 775
FN SUFFIX



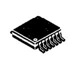
CASE 873A
FB SUFFIX



CASE 936
D2T SUFFIX



CASE 936A
D2T SUFFIX



CASE 948B
DTB SUFFIX

CASE 948E
DTB SUFFIX

Power/Motor Control Circuits

In Brief . . .

With the expansion of electronics into more and more mechanical systems, there comes an increasing demand for simple but intelligent circuits that can blend these two technologies. In the past, the task of power/motor control was once accomplished with discrete devices. But today this task is being performed by bipolar IC technology due to cost, size, and reliability constraints. Motorola offers integrated circuits designed to anticipate the requirements for both simple and sophisticated control systems, while providing cost effective solutions to meet the needs of the applications.

Page

Power Controllers

An assortment of battery and ac line–operated control ICs for specific applications are shown. They are designed to enhance system performance and reduce complexity in a wide variety of control applications.

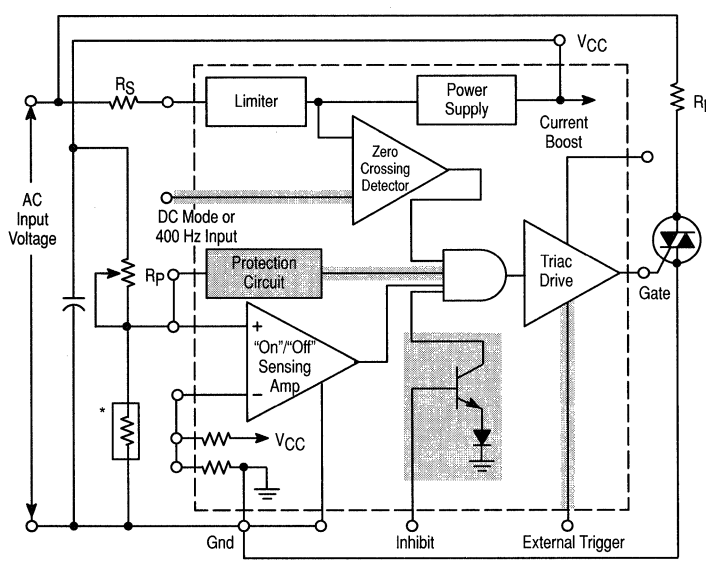
Zero Voltage Switch

CA3059

T_A = –40° to +85°C, Case 646

This device is designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 227 V @ 50/60 Hz.

- **Limiter–Power Supply** – Allows operation directly from an ac line.
- **Differential "On"/"Off" Sensing Amplifier** – Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented.
- **Zero–Crossing Detector** – Synchronizes the output pulses to the zero voltage point of the ac cycle. Eliminates RFI when used with resistive loads.
- **Triac Drive** – Supplies high current pulses to the external power controlling thyristor.
- **Protection Circuit** (CA3059 only) – A built–in circuit may be actuated, if the sensor opens or shorts, to remove the drive circuit from the external triac.
- **Inhibit Capability** (CA3059 only) – Thyristor firing may be inhibited by the action of an internal diode gate.
- **High Power DC Comparator Operation** (CA3059 only) – Operation in this mode is accomplished by connecting Pin 7 to 12 (thus overriding the action of the zero–crossing detector).



*NTC Sensor
NOTE: Shaded Area Not Included with CA3079.

Power Controllers (continued)

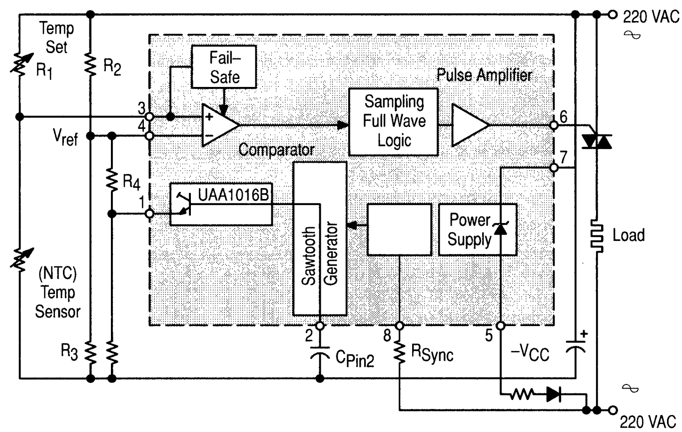
Zero Voltage Controller

UAA1016B

T_A = –20° to +100°C, Case 626

This device is designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. They provide the following features:

- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- Sensor Fail–Safe
- No DC Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (Triacs Quadrants 2 and 3)
- Direct AC Line Operation
- Low External Components Count



Zero Voltage Controller

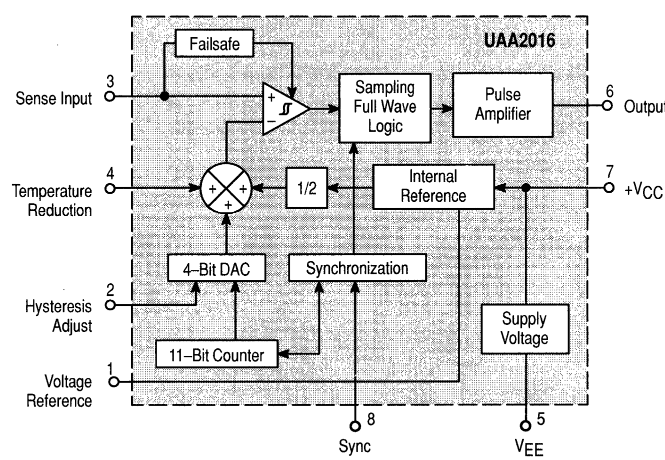
UAA2016P, D

T_A = –20° to +85°C, Case 626, 751

The UAA2016 is designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. Operating directly on the ac power line, its main application is the precision regulation of electrical heating systems such as panel heaters or irons.

A built–in digital sawtooth waveform permits proportional temperature regulation action over a ±1°C band around the set point. For energy savings there is a programmable temperature reduction function, and for security, a sensor failsafe inhibits output pulses when the sensor connection is broken. Preset temperature (i.e., defrost) application is also possible. In applications where high hysteresis is needed, its value can be adjusted up to 5°C around the set point. All these features are implemented with a very low external component count.

- Zero Voltage Switch for Triacs, up to 2.0 kW (MAC212A8)
- Direct AC Line Operation
- Proportional Regulation of Temperature over a 1°C Band
- Programmable Temperature Reduction
- Preset Temperature (i.e., Defrost)
- Sensor Failsafe
- Adjustable Hysteresis
- Low External Component Count



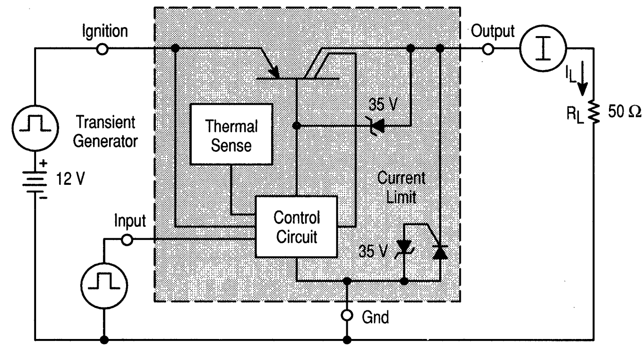
High–Side Driver Switch

MC3399T, DW

T_J = –40° to +150°C, Case 314D, 751G

The MC3399T is a high side driver switch that is designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the "on" state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive or negative–going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.

The MC3399T is fabricated on a Power BiMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.



Motor Controllers

This section contains integrated circuits designed for cost effective control of specific motor families. Included are controllers for brushless, dc servo, stepper, and universal type motors.

Brushless DC Motor Controllers

Advances in magnetic materials technology and integrated circuits have contributed to the unprecedented rise in popularity of brushless dc motors. Analog control ICs are making the many features and advantages of brushless motors available at a much more economical price. Motorola offers a family of monolithic integrated brushless dc motor controllers. These ICs provide a choice of control functions which allow many system features to be easily implemented at a fraction of the cost of discrete solutions. The following table summarizes and compares the features of Motorola's brushless motor controllers.

Table 1. Features Summary for Motorola Brushless DC Motor Controllers

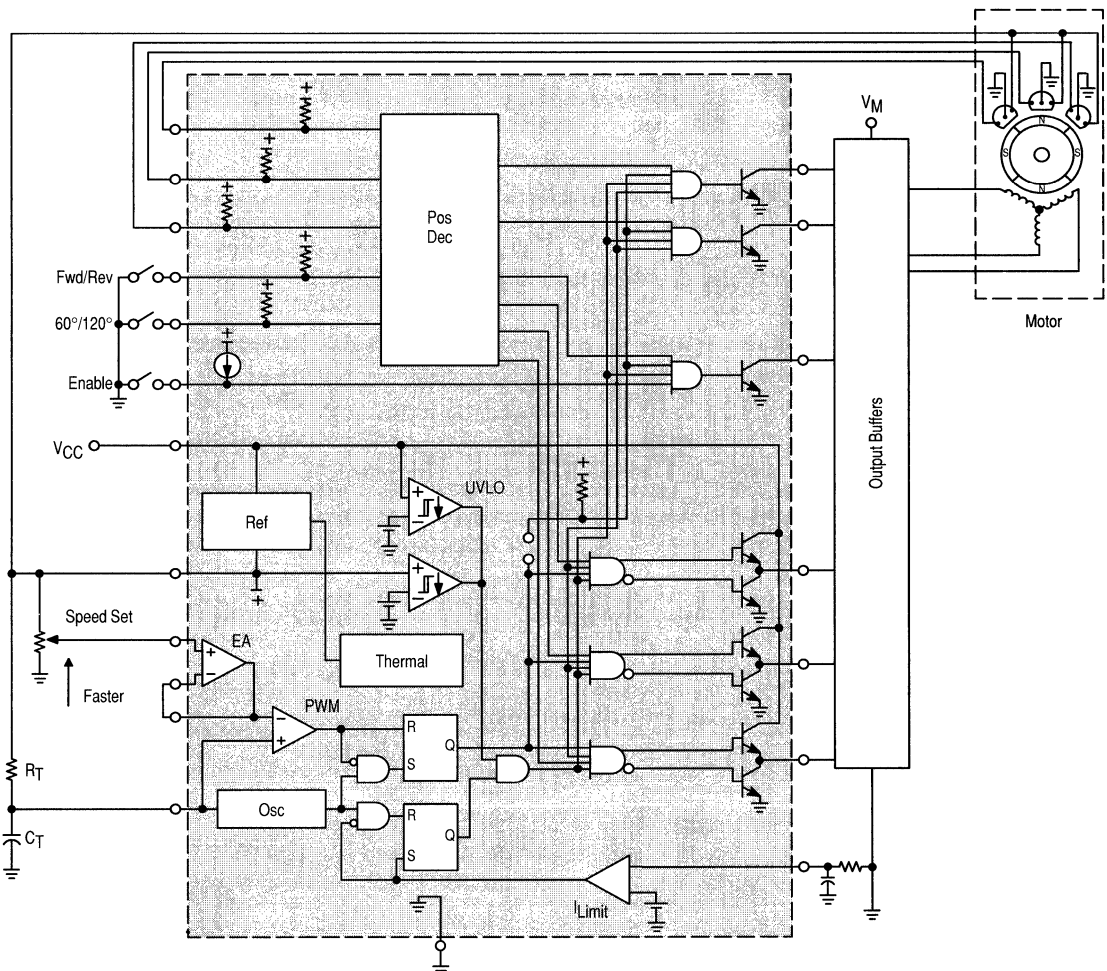
Device	Operating Voltage Range (V)		Undervoltage Lockout	Internal Thermal Shutdown	Fwd/Rev Control	Sensor Electrical Phasing	Output Enable	Output Drivers		6.25 V Reference Output	Current Sense Comparator Input(s)	Error Amplifier	FAULT Output	Separate Drive V_C	Brake Input	Suffix/ Package
	V_{CC}	V_C						Totem Pole (Bottom)	Open Collector (Top)							
MC33033	10–30	–	✓	✓	✓	60°/300° and 120°/240°	✓	✓	✓	✓	Noninv. Only	✓	–	–	–	P/738, DW/751D
MC33035	10–40	10–30	✓	✓	✓		✓	✓	✓	✓	Noninv. and Inv.	✓	✓	✓	✓	P/724, DW/751E

MC33033P, DW

T_A = –40° to +85°C, Case 738, 751D

The MC33033 is a lower cost second generation brushless dc motor controller which has evolved from the full featured MC33034 and MC33035 controllers. The MC33033 contains all of the active functions needed to implement a low cost open loop motor control system. This IC has all of the key control and protection functions of the two full featured devices with the following secondary features deleted: separate drive–circuit supply and ground pins, the brake input, and the fault output signal. Like its MC33035 predecessor, the MC33033 has a control pin which allows the user to select 60°/300° or 120°/240° sensor electrical phasings.

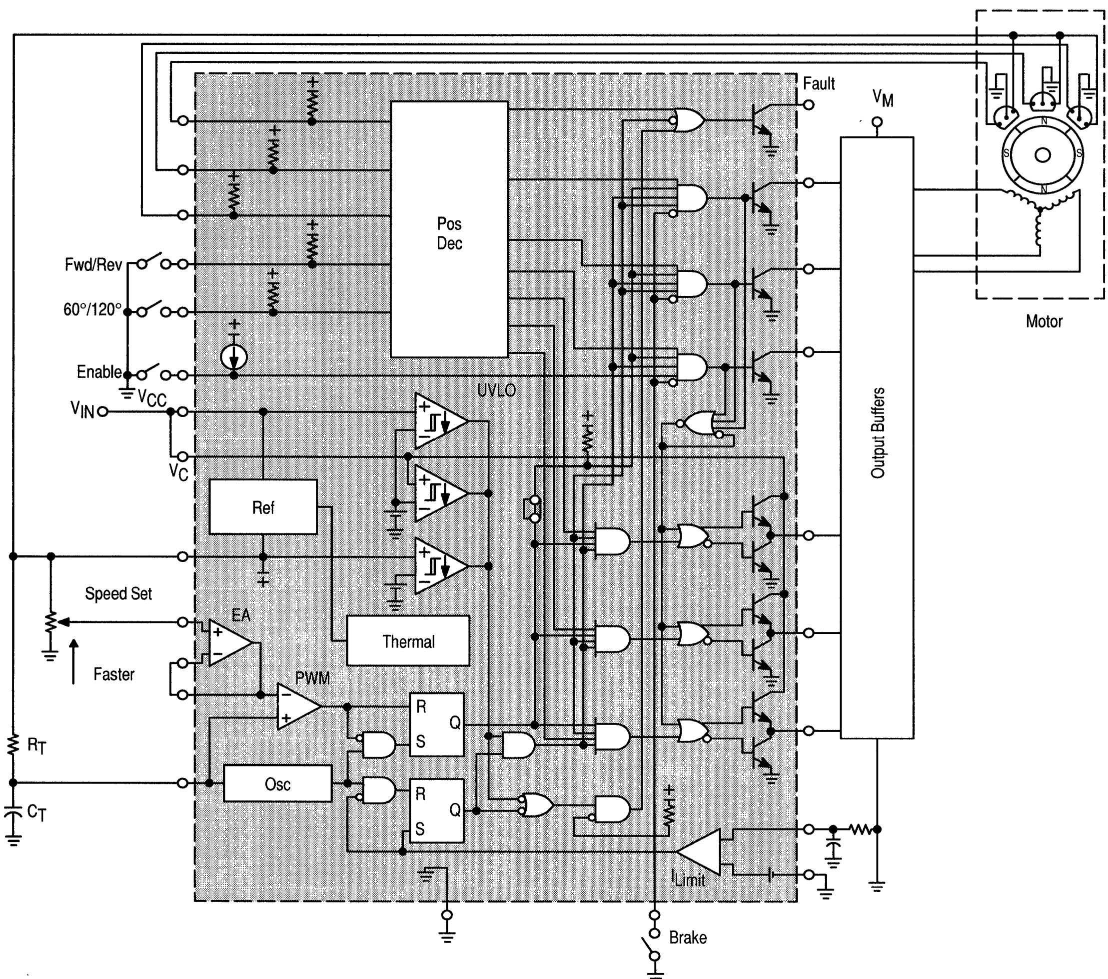
Because of its low cost, the MC33033 can efficiently be used to control brush dc motors as well as brushless. A brush dc motor can be driven using two of the three drive output phases provided in the MC33033, while the Hall sensor input pins are selectively tied to V_{ref} or ground. Other features such as forward/reverse, output enable, speed control, current limiting, undervoltage lockout and internal thermal shutdown will still remain functional.



MC33035P, DW

T_A = –40° to +85°C, Case 724, 751E

The MC33035 is a second generation high performance brushless dc motor controller which contains all of the active functions required to implement a full featured open loop motor control system. While being pin–compatible with its MC33034 predecessor, the MC33035 offers additional features at a lower price. The two additional features provided by the MC33035 are a pin which allows the user to select 60°/300° or 120°/240° sensor electrical phasings, and access to both inverting and noninverting inputs of the current sense comparator. The earlier devices had two part numbers which were needed to support the different sensor phasings, and the inverting input to the current sense comparator was internally grounded. All of the control and protection features of the MC33034 are also provided in the MC33035.

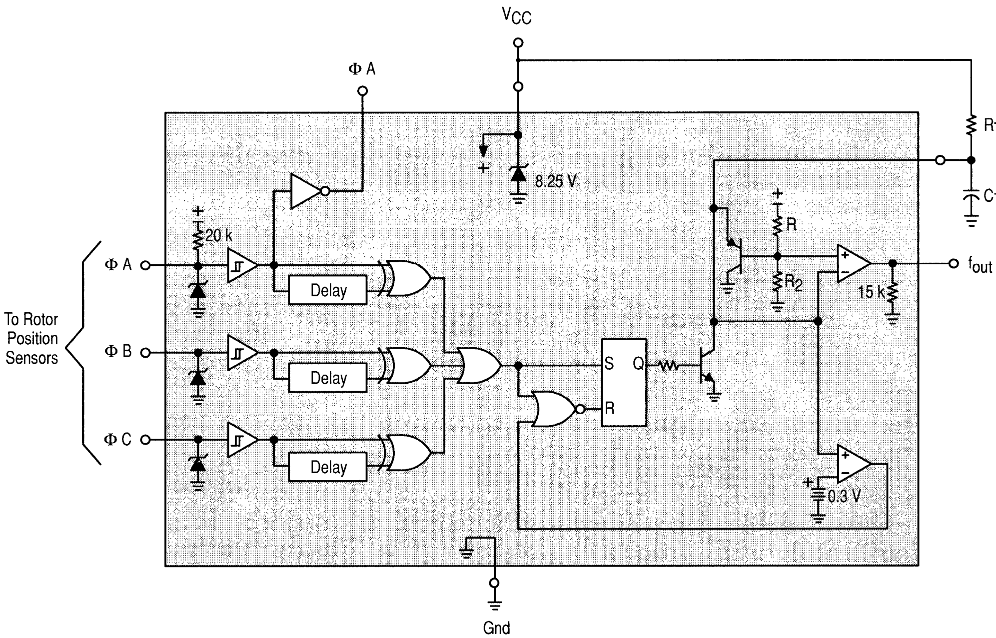


Closed Loop Brushless Motor Adapter

MC33039P, D

T_A = –40° to +85°C, Case 626, 751

The MC33039 is a high performance close loop speed control adapter specifically designed for use in brushless dc motor control systems. Implementation will allow precise speed regulation without the need for a magnetic or optical tachometer. These devices contain three input buffers each with hysteresis for noise immunity, three digital edge detectors, a programmable monostable, and an internal shunt regulator. Also included is an inverter output for use in systems that require conversion of sensor phasing. Although this device is primarily intended for use with the MC33033/35 brushless motor controllers, it can be used cost effectively in many other closed loop speed control applications.

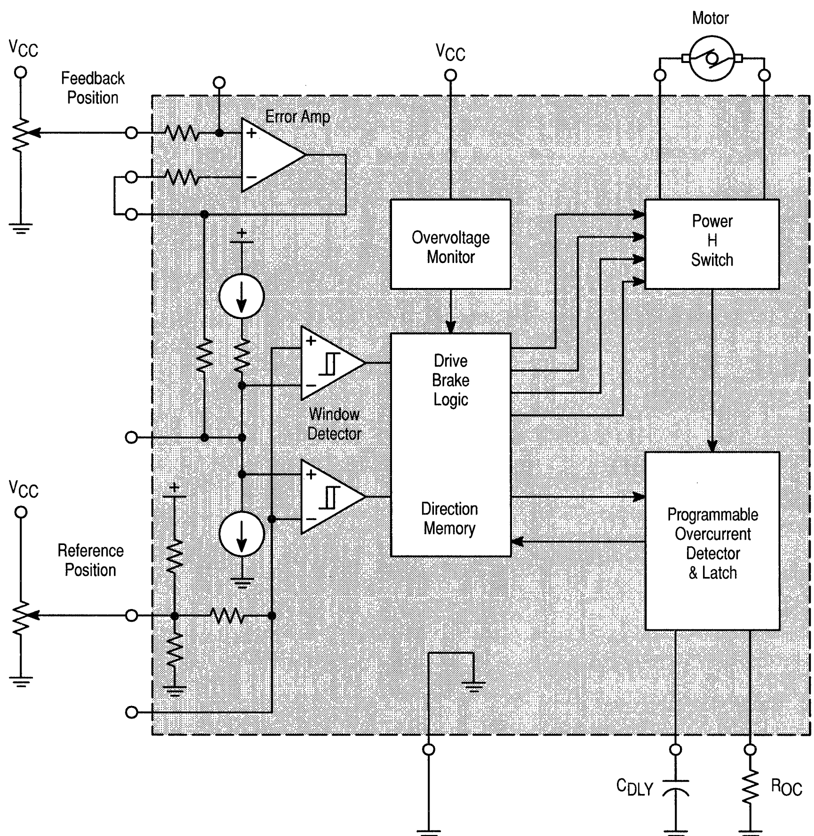


DC Servo Motor Controller/Driver

MC33030P, DW

T_A = –40° to +85°C, Case 648C, 751G

A monolithic dc servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on–chip op amp and window comparator with wide input common mode range, drive and brake logic with direction memory, a power H switch driver capable of 1.0 A, independently programmable over current monitor and shutdown delay, and over voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.



Stepper Motor Driver

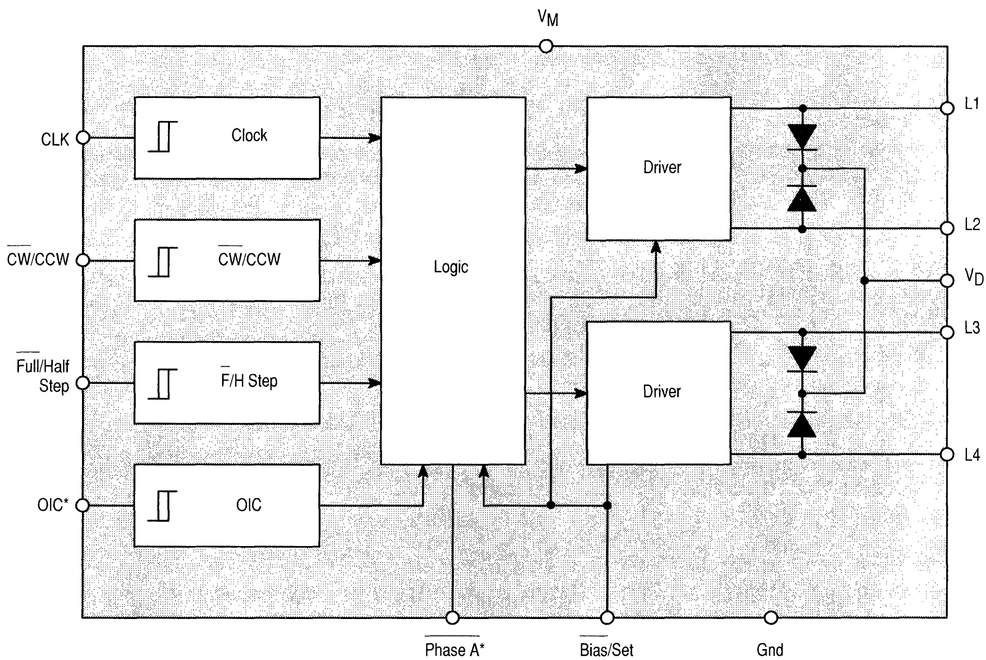
MC3479P, FN

T_A = 0° to +70°C, Case 648C, 775

SAA1042AV

T_A = –30° to +125°C, Case 648C

These Stepper Motor Drivers provide up to 500 mA of drive per coil for two phase 6.0 V to 24 V stepper motors. Control logic is provided to accept commands for clockwise, counter clockwise and half or full step operation. The MC3479 has an added Output Impedance Control (OIC) and a Phase A drive state indicator (not available on SAA1042 devices).



* MC3479 Only

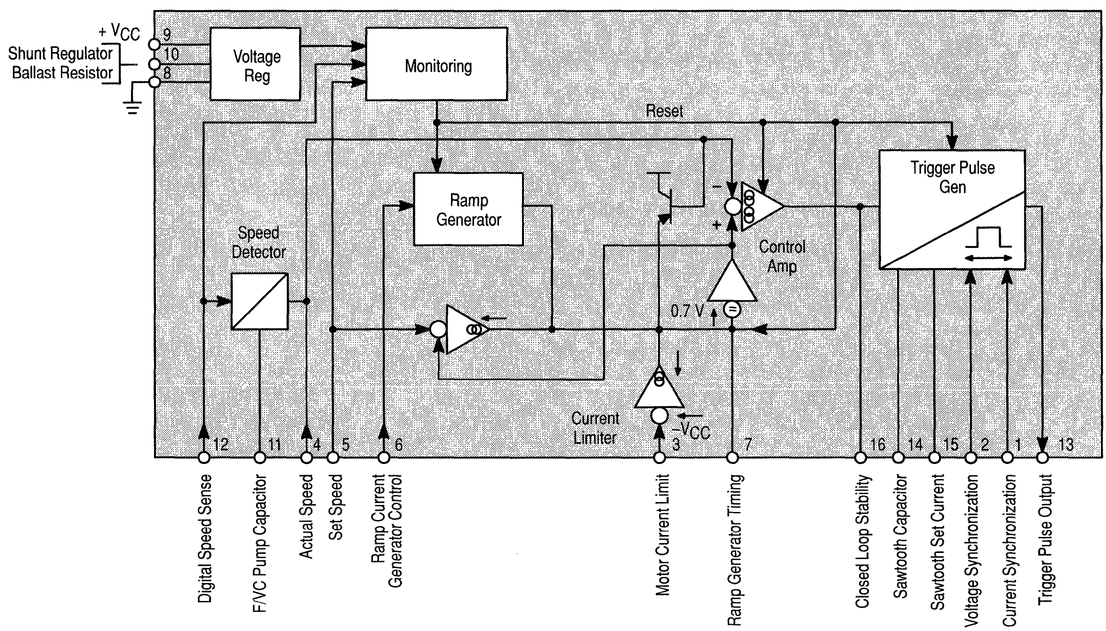
Universal Motor Speed Controller

TDA1085C, CD

T_A = –10° to +120°C, Case 648, 751B

The TDA1085C is a phase angle triac controller having all the necessary functions for universal motor speed control in washing machines. It operates in closed loop configuration and provides two ramp possibilities.

- On-Chip Frequency to Voltage Converter
- On-Chip Ramps Generator
- Soft Start
- Load Current Limitation
- Tachogenerator Circuit Sensing
- Direct Supply from AC Line
- Security Functions Peformed by Monitor



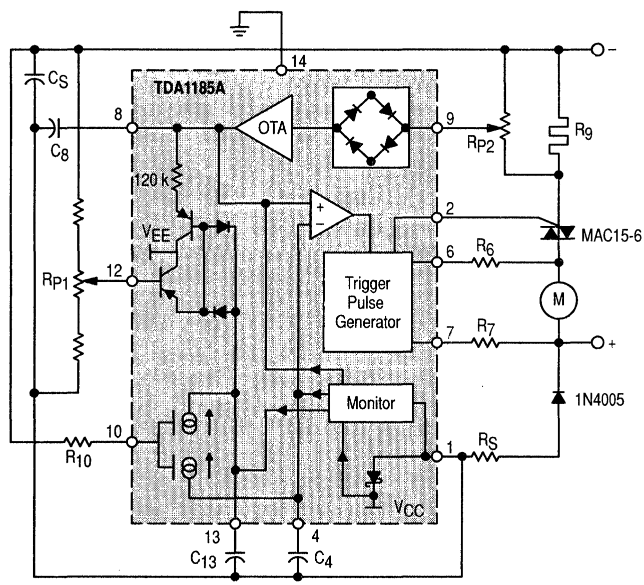
Triac Phase Angle Controller

TDA1185A

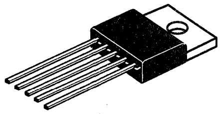
T_A = 0° to +70°C, Case 646

This device generates controlled triac triggering pulses and allows tachless speed stabilization of universal motors by an integrated positive feedback function.

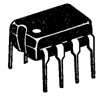
- Low Cost External Components Count
- Optimum Triac Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses when Triac Current is Interrupted by Motor Brush Bounce
- Triac Current Sensed to Allow Inductive Loads
- Soft–Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 1.0 mA



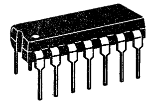
Power/Motor Control Circuits Package Overview



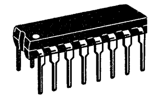
CASE 314D
T SUFFIX



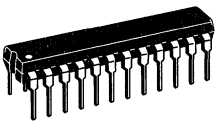
CASE 626
B, P SUFFIX



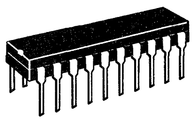
CASE 646



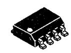
CASE 648, 648C
P, V SUFFIX



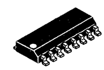
CASE 724
P SUFFIX



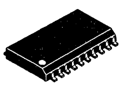
CASE 738
P SUFFIX



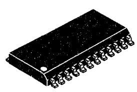
CASE 751
D SUFFIX



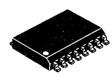
CASE 751B
D SUFFIX



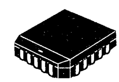
CASE 751D
DW SUFFIX



CASE 751E
DW SUFFIX



CASE 751G
DW SUFFIX



CASE 775
FN SUFFIX

Voltage References

In Brief . . .

Motorola's line of precision voltage references is designed for applications requiring high initial accuracy, low temperature drift, and long term stability. Initial accuracies of ±1.0%, and ±2.0% mean production line adjustments can be eliminated. Temperature coefficients of 25 ppm/°C max (typically 10 ppm/°C) provide excellent stability. Uses for the references include D/A converters, A/D converters, precision power supplies, voltmeter systems, temperature monitors, and many others.

Page

Precision Low Voltage References

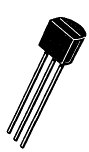
A family of precision low voltage bandgap reference devices designed for applications requiring low temperature drift.

Table 1. Precision Low Voltage References

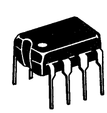
V_{out} (V) Typ	I_O (mA) Max	V_{out}/T ppm/°C Max	Device 0° to +70°C	Device –40° to +85°C	Reg_{line} (mV) Max	Reg_{load} (mV) Max	Package
1.235 ± 12 mV 1.235 ± 25 mV	20	80 Typ	LM385BZ–1.2 LM385Z–1.2	LM285Z–1.2	(Note 1)	1.0 (Note 2)	Z, D
2.5 ± 38 mV 2.5 ± 75 mV			LM385BZ–2.5 LM385Z–2.5	LM285Z–2.5		2.0 (Note 3)	
2.5 ± 25 mV	10	25	MC1403A	–	3.0/4.5 (Note 4)	10 (Note 5)	D
		40	MC1403				
5.0 ± 50 mV		40	MC1404P5	–	6.0 (Note 6)		P
6.25 ± 60 mV		40	MC1404P6	–			
10 ± 100 mV		40	MC1404P10	–			
2.5 to 37	100	50 Typ	TL431C, AC, BC	TL431I, AI, BI	Shunt Reference Dynamic Impedance (z) ≤ 0.5 Ω		LP, P, D

Notes: 1. Micropower Reference Diode Dynamic Impedance (z) ≤ 1.0 Ω at I_R = 100 µA.
2. 10 µA ≤ I_R ≤ 1.0 mA.
3. 20 µA ≤ I_R ≤ 1.0 mA.
4. 4.5 V ≤ V_{in} ≤ 15 V/15 V ≤ V_{in} ≤ 40 V.
5. 0 mA ≤ I_L ≤ 10 mA.
6. (V_{out} + 2.5 V) ≤ V_{in} ≤ 40 V.

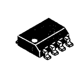
Voltage References Package Overview



CASE 29
LP, Z SUFFIX



CASE 626
P SUFFIX



CASE 751
D SUFFIX

Data Conversion

In Brief . . .

Motorola's line of digital–to–analog and analog–to–digital converters include several well established industry standards.

The A/D converters have 7 and 8–bit flash converters suitable for NTSC and PAL systems, CMOS has 8 to 10–bit converters, as well as other high speed digitizing applications.

The D/A converters have 6 and 8–bit devices, video speed (for NTSC and PAL) devices, and triple video DAC with on–board color palette for color graphics applications.

Data Conversion

The line of data conversion products which Motorola offers spans a wide spectrum of speed and resolution/accuracy. Features, including bus compatibility, minimize external parts count and provide easy interface to microprocessor systems. Various technologies, such as Bipolar and CMOS, are utilized to achieve functional capability, accuracy and production repeatability. Bipolar technology generally results in higher speed, while CMOS devices offer greatly reduced power consumption.

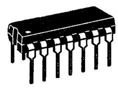
Table 1. A–D Converters

Resolution (Bits)	Device	Nonlinearity Max	Conversion Time/Rate	Input Voltage Range	Supplies (V)	Temperature Range (°C)	Suffix/ Package	Comments
CMOS								
8	MC145040	±1/2 LSB	10 µs	0 to V_{DD}	+5.0 ±10%	–40 to +125	P/738, DW/751D	Requires External Clock, 11–Ch MUX
	MC145041		20 µs					Includes Internal Clock, 11–Ch MUX
	MC14549B/ MC14559B	Successive Approximation Registers			+3.0 to +18	–40 to +85	P/648	Compatible with MC1408 S.A.R. 8–bit D–A Converter
Triple 8–Bit	MC44251	1 LSB	18 MHz	1.6 to 4.6 V	+5.0 ±10%	–40 to +85	FN/777	3 Separate Video Channels
10	MC145050	±1 LSB	21 µs	0 to V_{DD}	+5.0 ±10%	–40 to +125	P/738, DW/751D	Requires External Clock, 11–Ch MUX
	MC145051		44 µs					Includes Internal Clock, 11–Ch MUX
	MC145053						P/646, D/751A	Includes Internal Clock, 5–Ch MUX
8–10	MC14443/ MC14447	±0.5% Full Scale	300 µs	Variable w/Supply	+5.0 to +18	–40 to +85	P/648, DW/751G	µP Compatible, Single Slope, 6–Ch MUX
3–1/2 Digit	MC14433	±0.05% ±1 Count	40 ms	±2.0 V ±200 mV	+5.0 to +8.0 –2.8 to –8.0		P/709, DW/751E	Dual Slope
Bipolar								
8	MC10319	±1 LSB	25 MHz	0 to 2.0 Vpp Max	+5.0 and –3.0 to –6.0	0 to +70	P/709, DW/751F Die Form	Video Speed Flash Converter, Internal Gray Code TTL Outputs
Sigma–Delta								
16	MC145073	±1 LSB	48 kHz	1.9 Vpp	4.5 to 5.5	–40 to +85	DW/751E	Dual Channel, Sigma–Delta architecture

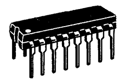
Table 2. D–A Converters

Resolution (Bits)	Device	Accuracy @ 25°C Max	Max Settling Time (± 1/2 LSB)	Supplies (V)	Temperature Range (°C)	Suffix/ Package	Comments
CMOS							
6	MC144110	–	–	+5.0 to +15	0 to +85	P/707, DW/751D	Serial input, Hex DAC, 6 outputs
	MC144111	–	–			P/646, DW/751G	Serial input, Quad DAC, 4 outputs
	MC144112	–	–	+2.5 to +5.5	–40 to +85	P/646, D/751A	Serial input, Quad DAC, 4 outputs
Triple 8–Bit	MC44200	±1/2 LSB	30 ns	+5.0 ±10%	–40 to +85	FU/824A	Triple Video DAC, 55 MHz, TTL
Sigma–Delta							
16, 18, 20	MC145074	See data sheet	6.0 ns	4.5 to 5.5	–40 to +85	D/751B	Dual Channel, Sigma–Delta architecture, MC145076 FIR Filter available
–	MC145076	See data sheet	–	+5.0	–40 to +85	D/751B	Dual Channel Bit Stream, 144 tap FIR Filter

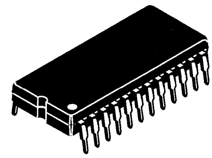
Data Conversion Package Overview



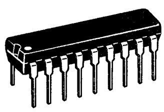
CASE 646
P SUFFIX



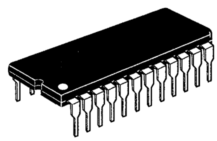
CASE 648
P SUFFIX



CASE 649
P SUFFIX



CASE 707
P SUFFIX



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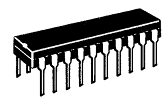
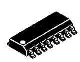
P SUFFIX

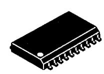


CASE 738
P SUFFIX

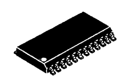
CASE 751A
D SUFFIX



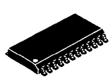
CASE 751B
D SUFFIX



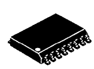
CASE 751D
DW SUFFIX



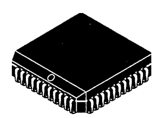
CASE 751E
DW SUFFIX



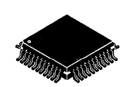
CASE 751F
DW SUFFIX



CASE 751G
DW SUFFIX



CASE 777
FN SUFFIX



CASE 824A
FU SUFFIX

Interface Circuits

In Brief . . .

Described in this section is Motorola's line of interface circuits, which provide the means for interfacing with microprocessor or digital systems and the external world, or to other systems.

Also included are devices which allow a microprocessor to communicate with its own array of memory and peripheral I/O circuits.

The line drivers, receivers, and transceivers permit communication between systems over cables of several thousand feet in length, and at data rates of up to several megahertz. The common EIA data transmission standards, several European standards, IEEE–488, and IBM 360/370 are addressed by these devices.

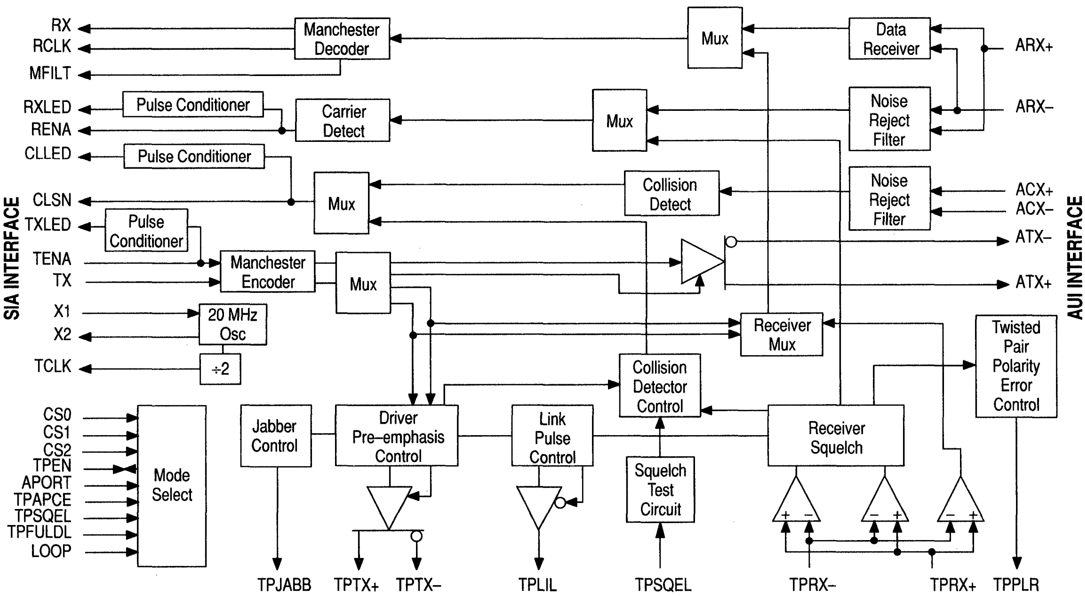
The peripheral drivers are designed to handle high current loads such as relay coils, lamps, stepper motors, and others. Input levels to these drivers can be TTL, CMOS, high voltage MOS, or other user defined levels. The display drivers are designed for LCD or LED displays, and provide various forms of decoding.

Enhanced Ethernet Transceiver

MC68160FB

T_A = 0° to +70°C, Case 848D

The MC68160 Enhanced Ethernet Interface Circuit is a BiCMOS device which supports both IEEE 802.3 Access Unit Interface (AUI) and 10BASE–T Twisted Pair (TP) Interface media connections through external isolation transformers. It encodes NRZ data to Manchester data and supplies the signals which are required for data communication via 10BASE–T or AUI interfaces. The MC68160 gluelessly interfaces to the Ethernet controller contained in the MC68360 Quad Integrated Communications Controller (QUICC) device. The MC68160 also interfaces easily to most other industry–standard IEEE 802.3 LAN controllers. Prior to twisted pair data reception, Smart Squelch circuitry qualifies input signals for correct amplitude, pulse width, and sequence requirements.



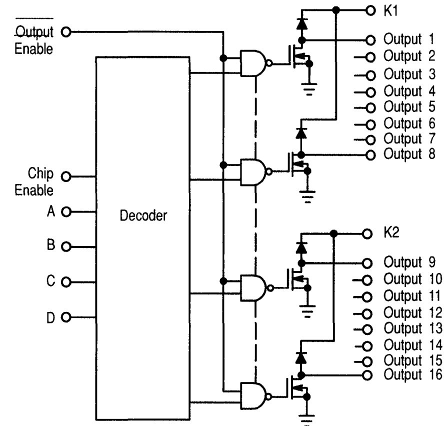
High Performance Decoder Driver/Sink Driver

MC34142DW, FN

T_A = 0° to +70°C, Case 751F, 776

The MC34142 is a high performance 4 to 16 multiplexed driver. This integrated circuit features a 4 to 16 decoder, 16 open drain N–channel MOS output devices with clamp diodes. The outputs are controlled by 4 address inputs, an output enable, and a chip enable.

Typical applications include solenoid drivers, LED drivers, lamp drivers, and relay drivers.

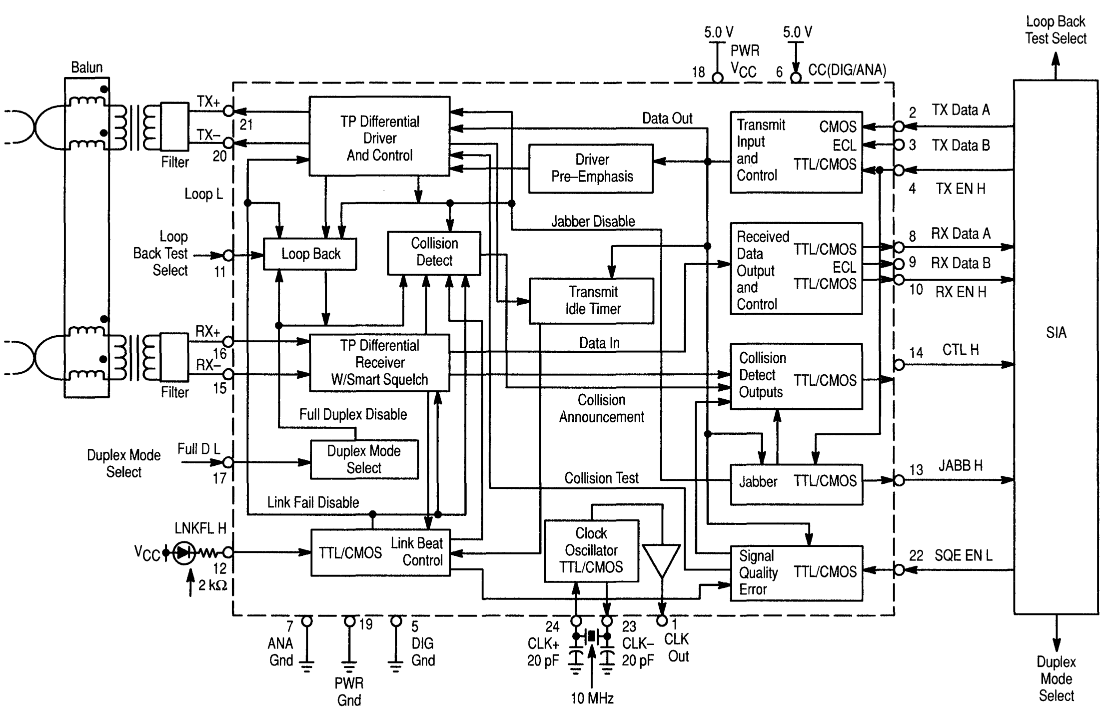


ISO 8802–3[IEEE 802.3] 10BASE–T Transceiver

MC34055DW

T_A = 0° to +70°C, Case 751E

The Motorola 10BASE–T transceiver, designed to comply with the ISO 8802–3[IEEE 802.3] 10BASE–T specification, will support a Medium Dependent Interface (MDI) in an embedded Media Attachment Unit (MAU). The interface supporting the Data Terminal Equipment (DTE) is TTL, CMOS, and raised ECL compatible, and the interface to the Twisted Pair (TP) media is supported through standard 10BASE–T filters and transformers. Differential data intended for the TP media is provided a 50 ns pre–emphasis and data at the TP receiver, is screened by Smart Squelch circuitry for specific threshold, pulse width, and sequence requirements.



Hex EIA–485 Transceiver with Three–State Outputs

MC34058/59FTA

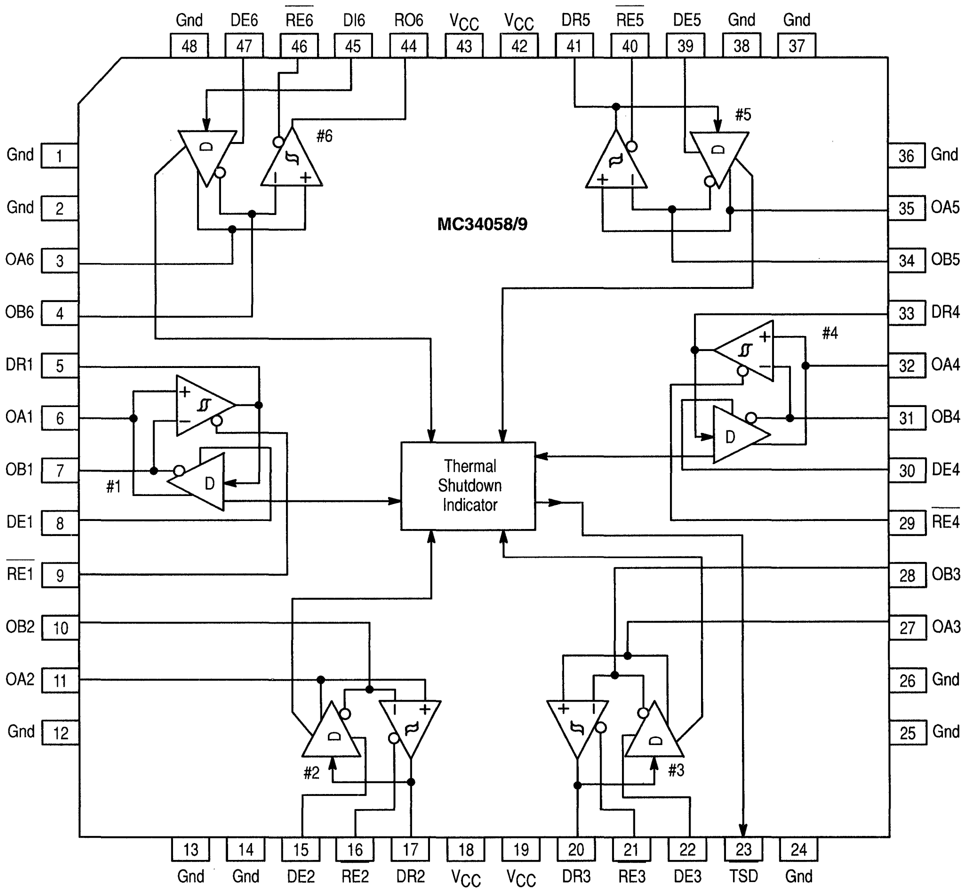
T_A = 0° to +70°C, Case 932

The Motorola MC34058/9 Hex Transceiver is composed of six driver/receiver combinations designed to comply with the EIA–485 standard. Features include three–state outputs, thermal shutdown for each driver, and current limiting in both directions. This device also complies with EIA–422 and CCITT Recommendations V.11 and X.27.

The devices are optimized for balanced multipoint bus transmission at rates to 20 MBPS (MC34059). The driver outputs/receiver inputs feature a wide common mode voltage range, allowing for their use in noisy environments. The current limit and thermal shutdown features protect the devices from line fault conditions.

The MC34058/9 is available in a space saving 7.0 mm 48 lead surface mount quad package designed for optimal heat dissipation.

- Meets EIA–485 Standard for Party Line Operation
- Meets EIA–422A and CCITT Recommendations V.11 and X.27
- Operating Ambient Temperature: 0°C to +70°C
- Common Mode Driver Output/Receiver Input Range: –7.0 to +12 V
- Positive and Negative Current Limiting
- Transmission Rates to 14 MBPS (MC34058) and 20 MBPS (MC34059)
- Driver Thermal Shutdown at 150°C Junction Temperature
- Thermal Shutdown Active Low Output
- Single +5.0 V Supply, ±10%
- Low Supply Current
- Compact 7.0 mm 48 Lead TQFP Plastic Package
- Skew Specified for MC34059



5.0 V, 200 M–Bit/Sec PR–IV Hard Disk Drive Read Channel

MC34250FTA

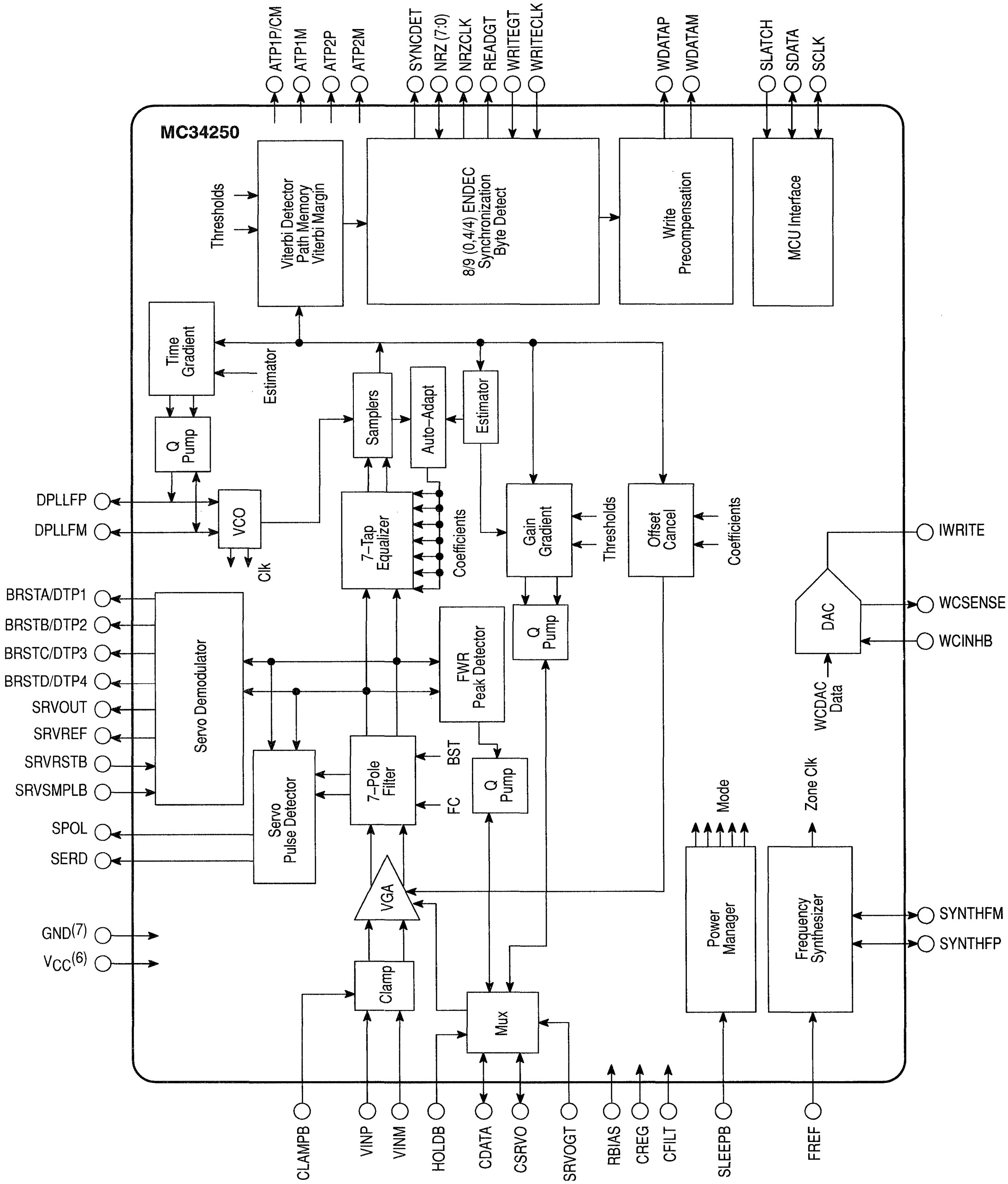
T_A = 0° to +70°C, Case 840F

The Motorola MC34250 is a fully integrated partial response maximum likelihood disk drive read/write channel for use in zoned recording applications. This device integrates the AGC, active filter, 7 tap equalizer, Viterbi detector, frequency synthesizer, servo demodulator, 8/9 rate (0,4/4) Encoder/Decoder with write precompensation and power management in a single 64 pin 10 mm x 10 mm TQFP package.

FEATURES:

- 50 to 200 MBPS Programmable Data Rate
- 800 mW at 200 MBPS and 5.0 V
- Channel Monitor Output
- Programmable AGC Charge Pump Currents with Different Values for Data and Servo Envelope Modes and Gain Gradient Mode
- Programmable AGC Peak Detector Droop Currents with Different Values for Data and Servo Envelope Modes
- Separate AGC Charge Pump Outputs for Data and Servo Modes
- Programmable Dual Threshold Qualifier or Hysteresis Comparator Type Pulse Detector for Servo Data Detection.
- ERD and Polarity Outputs for Servo Timing and Raw Encoded Data
- Integrated 7 pole 0.05° Equiripple Linear Phase Filter with Programmable Bandwidth from 5.0 MHz to 80 MHz and Different Values for Both Data and Servo Modes
- Programmable Symmetrical Boost from 0 to 10 dB and Different Values for Data and Servo Modes
- Programmable Asymmetrical Boost of Up to ±40% of Nominal Filter Group Delay in Both Data and Servo Modes
- 7 Tap Continuous Time Transversal Equalizer with 8 Bit Programmable Tap Weights and Integrated Decision Directed Sign–Sign Least Mean Squared Adaptation
- Internal Offset Cancellation Loops
- Fast Acquisition Data Phase Locked Loop with Zero Phase Restart
- Programmable Data Phase Locked Loop Charge Pump Current
- Integrated Soft Decision Viterbi Detectors with Programmable Merge References
- Integrated 8/9 Rate (0,4/4) Encoder and Decoder with Code Scrambler and Descrambler
- Programmable 2/4/8 Bit NRZ Data Interface
- Programmable Write Precompensation Delays Locked to the Frequency Synthesizer
- Differential PECL Write Data Outputs
- External Write Data Path for DC Erase or Other Non–Encoded Data
- Integrated Write Current DAC
- Programmable Power Management
- Bi–Directional Serial Microprocessor Interface
- Various Test Modes Controlled Via the Serial Microprocessor Interface

5.0 V, 200 M–Bit/Sec PR–IV Hard Disk Drive Read Channel (continued)



Line Receivers

Table 1. EIA Standard

S = Single Ended D = Differential	Type of Output	t_{prop} Delay Time Max (ns)	Party Line Operation	Strobe or Enable	Power Supplies (V)	Device	Suffix/ Package	Receivers Per Package	Companion Drivers	Comments
S	TP	4000	–	–	+5.0	MC14C89B, AB	P/646, D/751A	4	MC1488 MC14C88B	EIA–232–D/ EIA–562
	R(1)	85	–	–		MC1489 MC1489A				EIA–232–D
S, D	TP	30	✓	✓		AM26LS32	PC/648		AM26LS31	EIA–422/423
						MC3486	P/648, D/751B		MC3487	
		35				SN75173 SN75175	N/648, D/751B		MC75174B	EIA–422/423/ 485

(1) R = Resistor Pull–up, TP = Totem–pole output.

Line Drivers

Table 2. EIA Standard

Output Current Capa–bility (mA)	t_{prop} Delay Time Max (ns)	S = Single Ended D = Differential	Party Line Operation	Strobe or Enable	Power Supplies (V)	Device	Suffix/ Package	Drivers Per Package	Companion Receivers	Comments
85	35	D	✓	✓	+5.0	MC75174B	P/648	4	SN75173 SN75175	EIA–485
48	20					MC3487	P/648, D/751B		MC3486 AM26LS32	EIA–422 with 3–state outputs
						AM26LS31	PC/648			
						MC26LS31	D/751B			
15	3500	S	–		±7.0 to ±12	MC14C88B	P/646, D/751A		MC14C89B MC14C89AB	EIA–232–D/ EIA–562
10	350				±9.0 to ±12	MC1488			MC1489 MC1489A	EIA–232–D
60	300	S/D		EIA–422 ✓ EIA–423 –	±5.0	AM26LS30	PC/648	2 (422) 4 (423)	AM26LS32 MC3486	EIA–422 or EIA–423 Switchable
						MC26LS30	D/751B			

Table 3. Line Transceivers

Driver Prop Delay (Max ns)	Receiver Prop Delay Max (ns)	DE = Driver Enable RE = Receiver Enable	Party Line Operation	Power Supplies (V)	Device	Suffix/ Package	Drivers Per Package	Receivers Per Package	EIA Standard
20	30	DE, RE	✓	+5.0	MC34050	D/751B, P/648	2	2	EIA–422/423
		DE			MC34051				
23	23	DE, RE			MC34058	FTA/932	6	6	EIA–485 to 14 MBPS
					MC34059	FTA/932	6	6	EIA–485 to 20 MBPS

Table 4. EIA–232–E/V.28 CMOS Drivers/Receivers

Device	Suffix/ Package	Pins	Drivers	Receivers	Power Supplies (V)	Features
MC145403	P/738, DW/751D	20	3	5	±5.0 to ±12	
MC145404			4	4		
MC145405			5	3		
MC145406	P/648, DW/751G, SD/940B	16	3			
MC145407	P/738, DW/751D	20			+5.0	Charge Pump
MC145408	P/724, DW/751E, SD/940B	24	5	5	±5.0 to ±12	
MC145583	DW/751F, VF/940J	28	3	5	+3.3 to +5.0	On–board ring monitor circuit; charge pump, power down
MC145705	P/738, DW/751D	20	2	3	+5.0	Charge Pump, Power Down
MC145706			3	2		
MC145707	P/724, DW/751E	24		3		

Table 5. Peripheral Drivers

Output Current Capability (mA)	Input Capability	Propagation Delay Time Max (μs)	Output Clamp Diode	Off State Voltage Max (V)	Device	Drivers Per Package	Suffix/ Package	Logic Function
500	TTL, CMOS	1.0	✓	50	ULN2803	8	A/707	Invert
	6.0 V to 15 V MOS				ULN2804			
	TTL, 5.0 V CMOS				MC1413, B (ULN2003A)	7	P/648, D/751B	
	8.0 V to 18 V MOS				MC1416, B (ULN2004A)			

Table 6. IEEE 802.3 Transceivers

Device	Power Supply	10 BaseT	NRZ	IEEE	Comments	Suffix/ Package
MC34055	+5.0 Vdc	Transmit and Receive over 4 Pins	Raised ECL, CMOS	802.3 Type 10BaseT	Transceiver with non–return to zero (NRZ) interface. Intended for but not restricted to concentrators and repeator applications.	DW/751E
MC68160			TTL, CMOS	802.3 Type 10BaseT/ AUI/NRZ	Interfaces gluelessly to Motorola's MC68360 communications controller.	FB/848D

Read/Write Channel

Table 7. Hard Disk Drive Read Channel

Device	Power Supply	Comments	T_A (°C)	Suffix/ Package
MC34250	5.0 V	200 Mbps fully integrated partial response maximum likelihood hard disk drive read/write channel which equalizes to a PR–IV shape and uses 8/9 rate (0, 4/4) coding.	0 to +70	FTA/840F

CMOS Display Drivers

These CMOS devices include digit as well as matrix drivers for LEDs, LCDs, and VFDs. They find applications over a wide range of end equipment such as instruments, automotive dashboards, home computers, appliances, radios and clocks.

Table 8. Display Drivers

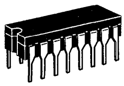
Display Type	Input Format	Drive Capability Per Package	On–Chip Latch	Display Control	Segment Drive Current	Device
LCD (Direct Drive)	Parallel BCD	7 Segments	✓	Blank	≈ 1.0 mA	MC14543B
				Blank, Ripple Blank		MC14544B
	Serial Binary [Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs]	33 Segments or Dots			20 μA	MC145453
Muxed LCD (1/4 Mux)		48 Segments or Dots			≈ 200 μA	MC145000
		44 Segments or Dots				MC145001
LED, Incandescent, Fluorescent[1]	Parallel BCD	7 Segments		Blank, Lamp Test	25 mA	MC14511B
				Blank, Ripple Blank, Lamp Test		MC14513B
			–	Blank	65 mA	MC14547B
Muxed LED (1/4 Mux)	Serial Binary [Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs]	4 Digits + Decimals	✓	Oscillator (Scanner)	50 mA (Peak)	MC14499
Muxed LED (1/5 Mux)		5 Characters + Decimals or 25 Lamps		Oscillator (Scanner), Low Power Mode, Dimming	0 to 35 mA (Peak) Adjustable	MC14489
LED (Direct Drive)	Parallel Hex	7 Segments + A thru F Indicator			10 mA[2]	MC14495–1
(Interfaces to Display Drivers)	Parallel BCD	7 Segments	–	Ripple Blank, Enable	–	MC14558B

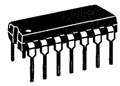
(1) Absolute maximum working voltage = 18 V.
(2) On–chip current–limiting resistor.

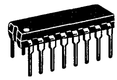
Table 9. Functions

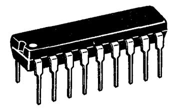
Device	Function	Package
MC14489	Multi–Character LED Display/Lamp Driver	738, 751D
MC14495–1	Hexadecimal–to–7 Segment Latch/Decoder ROM/Driver	648, 751G
MC14499	4–Digit 7–Segment LED Display Decoder/Driver with Serial Interface	707, 751D
MC14511B	BCD–to–7–Segment Latch/Decoder/Driver	648, 751G
MC14513B	BCD–to–7–Segment Latch/Decoder/Driver with Ripple Blanking	726, 707
MC14543B	BCD–to–7–Segment Latch/Decoder/Driver for Liquid Crystals	620, 648
MC14544B	BCD–to–7–Segment Latch/Decoder/Driver with Ripple Blanking	726, 707
MC14547B	High–Current BCD–to–7–Segment Decoder/Driver	620, 648
MC14558B	BCD–to–7–Segment Decoder	620, 648
MC145000	48–Segment Serial Input Multiplexed LCD Driver (Master)	709, 776
MC145001	44–Segment Serial Input Multiplexed LCD Driver (Slave)	707, 776
MC145453	33–Segment, Non–Multiplexed LCD Driver with Serial Interface	711, 777

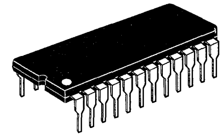
Interface Circuits Package Overview

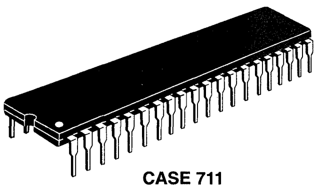

CASE 620


CASE 646
P SUFFIX


CASE 648
N, P, PC SUFFIX


CASE 707
A SUFFIX


CASE 709
P SUFFIX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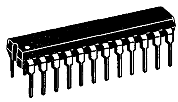
P SUFFIX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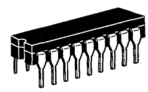
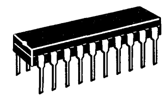
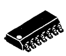
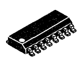
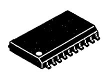
P SUFFIX

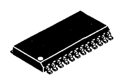

CASE 726

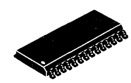

CASE 738
P SUFFIX

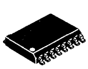

CASE 751A
D SUFFIX

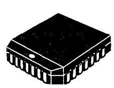

CASE 751B
D SUFFIX

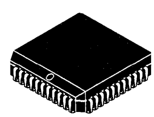

CASE 751D
DW SUFFIX

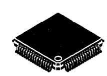

CASE 751E
DW SUFFIX

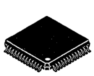

CASE 751F
DW SUFFIX


CASE 751G
DW SUFFIX

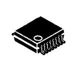

CASE 776
FN SUFFIX

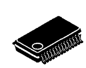

CASE 777
FN SUFFIX


CASE 840F
FTA SUFFIX


CASE 848D
FB SUFFIX


CASE 932
FTA SUFFIX


CASE 940B
SD SUFFIX


CASE 940J
VF SUFFIX

Communication Circuits

In Brief . . .

RF

Radio communication has greatly expanded its scope in the past several years. Once dominated by public safety radio, the 30 to 1000 MHz spectrum is now packed with personal and low cost business radio systems. The vast majority of this equipment uses FM or FSK modulation and is targeted at short range applications. From mobile phones and VHF marine radios to garage door openers and radio controlled toys, these new systems have become a part of our lifestyle. Motorola Analog has focused on this technology, adding a wide array of new products including complete receivers processed in our exclusive 3.0 GHz MOSAIC® 1.5 process. New surface mount packages for high density assembly are available for all of these products, as well as a growing family of supporting application notes and development kits.

Telephone & Voice/Data

Traditionally, an office environment has utilized two distinctly separate wired communications systems: telecommunications and data communications. Each had its individual hardware components complement, and each required its own independent transmission line system: twisted wire pairs for Telecom and relatively high priced coaxial cable for Datacom. But times have changed. Today, Telecom and Datacom coexist comfortably on inexpensive twisted wire pairs and use a significant number of components in common. This has led to the development and enhancement of PBX (Private Branch Exchanges) to the point where the long heralded "office of the future," with simultaneous voice and data communications capability at each station, is no longer of the future at all. The capability is here today!

Motorola Semiconductor serves a wide range of requirements for the voice/data marketplace. We offer both CMOS and Analog technologies, each to its best advantage, to upgrade the conventional analog voice systems and establish new capabilities in digital communications. Early products, such as the solid–state single–chip crosspoint switch, the more recent monolithic Subscriber–Loop–Interface Circuit (SLIC), a single–chip Codec/Filter (Mono–Circuit), the Universal Digital Loop Transceivers (UDLT), basic rate ISDN (Integrated Services Digital Network), and single–chip telephone circuits are just a few examples of Motorola leadership in the voice/data area.

RF Communications

Table 1. Wideband (FM/FSK) IFs

Device	V_{CC}	I_{CC}	Sensitivity (Typ)	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Package
MC13055	3–12 V	25 mA	20 µV	40 MHz	✓	✓	2.0 Mb	Wideband Data IF, includes data shaper	P/648, D/751B
MC13155	3–6 V	7.0 mA	100 µV	250 MHz	–		10 Mb	Video Speed FM IF	D/751B

Table 2. Wideband Single Conversion Receivers – VHF

Device	V_{CC}	I_{CC}	Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Package
MC3356	3–9 V	25 mA	30 µV	200 MHz	10.7 MHz	✓	✓	500 kb	Includes front end mixer/L.O.	P/738, DW/751D
MC13156	2–6 V	5.0 mA	2.0 µV	500 MHz	21.4 MHz	–			CT–2 FM/Demodulator	DW/751E, FB/873
MC13158	2–6 V	6.0 mA						>1.2 Mb	FM IF/Demodulator with split IF for DECT	FTB/873

Table 3. Narrowband Single Conversion Receivers – VHF

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Package
MC3357	4–8 V	5.0 mA	5.0 µV	45 MHz	455 kHz	✓	–	>4.8 kb	Ceramic Quad Detector/Resonator	P/648, D/751B
MC3359	4–9 V	7.0 mA	2.0 µV						Scan output option	P/707, DW/751D
MC3361C	2–8 V	6.0 mA		60 MHz				>2.4 kb	Lowest cost receiver	P648, D/751B
MC3371							✓	>4.8 kb	RSSI	P/648, D/751B
MC3372, A									RSSI, Ceramic Quad Detector/Resonator	
MC13150	3–6 V	1.8 mA	1.0 µV	500 MHz			✓ 110 dB	>9.6 kb	Coilless Detector with Adjustable Bandwidth	FTB/873, FTA/977

RF Communications (continued)

Table 4. Narrowband Dual Conversion Receivers – FM/FSK – VHF

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	RF Input	IF1	IF2 (Limiter In)	Mute	RSSI	Data Rate	Notes	Suffix/ Package
MC3362	2–7 V	3.0 mA	0.7 μV	180 MHz	10.7 MHz	455 kHz	–	✓	> 4.8 kb	Includes buffered VCO output	P/724, DW/751E
MC3363		4.0 mA	0.4 μV				✓			Includes RF amp/mute	DW/751F
MC3335			0.7 μV							Low cost version	DW/751D, P/738
MC13135			1.0 μV				–			Voltage buffered RSSI, LC Quad Detector	DW/751E, P/724
MC13136										Voltage Buffered RSSI, Ceramic Quad Detector	

Table 5. Universal Cordless Phone Subsystem ICs

Device	V_{CC}	I_{CC}	Dual Conversion Receiver	Universal Dual PLL	Compander and Audio Interface	Voice Scrambler	Low Battery Detect	Programmable R_X, T_X Trim Gain and LBD Voltage Reference	Suffix/ Package
MC13109	2.0–5.5 V	Active Mode 6.7 mA Inactive Mode 40 μA	✓	✓	✓	–	1	–	FB/848B, FTA/932
MC13110	2.7–5.5 V	Active Mode 8.2 mA Inactive Mode 60 μA	✓	✓	✓	✓	2	✓	FB/848B
MC13111	2.7–5.5 V	Active Mode 8.2 mA Inactive Mode 60 μA	✓	✓	✓	–	2	✓	FB/848B

Table 6. Transmitters – AM/FM/FSK

Device	V_{CC}	I_{CC}	P_{out}	Max RF Freq Out	Max Mod Freq	Notes	Suffix/ Package
MC2833	3–8 V	10 mA	–30 dBm to +10 dBm	150 MHz	50 kHz	FM transmitter. Includes two frequency multiplier/amplifier transistors	P/648, D/751B
MC13175	2–5 V	40 mA	8.0 dBm	500 MHz	5.0 MHz	AM/FM transmitter. Single frequency PLL $f_{out} = 8 \times f_{ref}$, includes power down function	D/751B
MC13176				1.0 GHz		$f_{out} = 32 \times f_{ref}$, includes power down function	

Table 7. Balanced Modulator/Demodulator

Device	V_{CC}	I_{CC}	Function	Suffix/ Package
MC1496	3–5 V	10 mA	General purpose balanced modulator/demodulator for AM, SSB, FM detection with Carrier Balance >50 dB	P/646, D/751A

Table 8. Infrared Transceiver

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	Max IF Freq	Carr Det	RSSI	Data Rate	Notes	Suffix/ Package
MC13173	3–5 V	6.5 mA	5.0 μV	10.7 MHz	✓	✓	200 kb	Includes Single Frequency PLL for T_X Carrier and R_X L_O	FTB/873

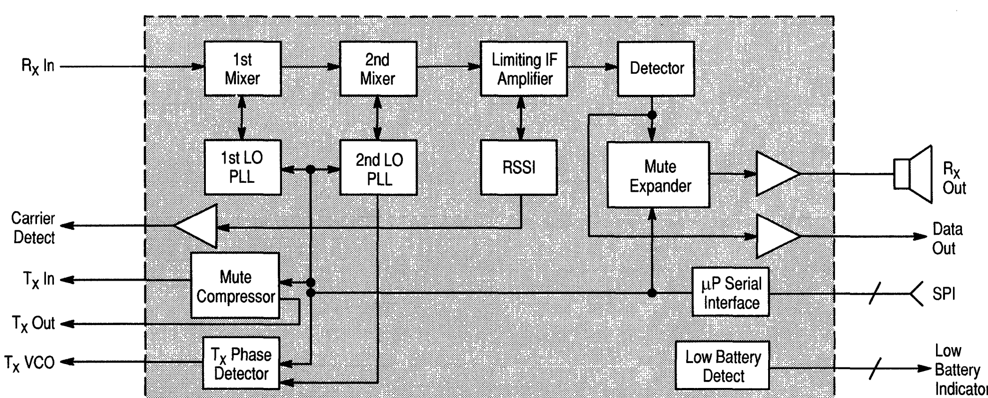
Universal Cordless Telephone Subsystem IC

MC13109FB, FTA

T_A = –40° to +85°C, Case 848B, 932

The MC13109 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna Input to Audio Output 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expandor Includes Mute, Digital Volume Control and Speaker Driver
  - Compressor Includes Mute, ALC and Limiter
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Output Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Externally Adjustable Trip Point
- 2.0 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices



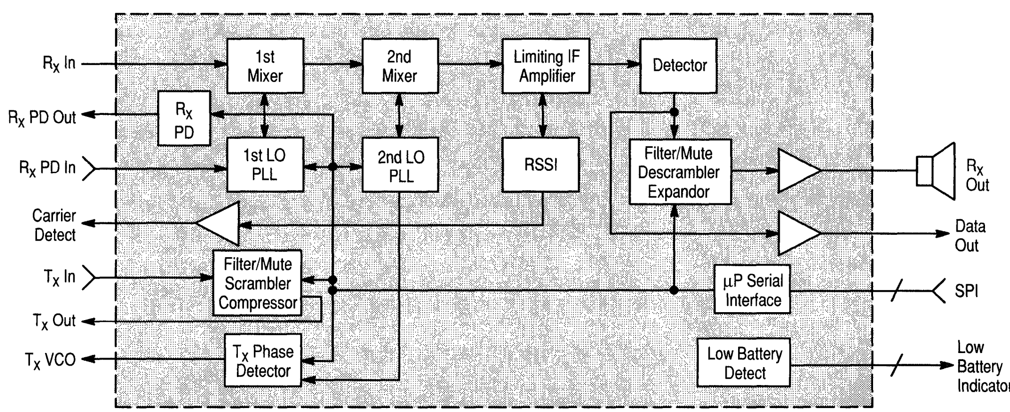
Universal Cordless Telephone Subsystem IC with Scrambler

MC13110FB

T_A = –40° to +85°C, Case 848B

The MC13110 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna In to Audio Out 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expandor Includes Mute, Digital Volume Control, Speaker Driver, 3.5 kHz Low Pass Filter, and Programmable Gain Block
  - Compressor Includes Mute, 3.5 kHz Low Pass Filter, Limiter, and Programmable Gain Block
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with New External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Outputs Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Provides Two Levels of Monitoring with Separate Outputs
  - Separate, Adjustable Trip Points
- Frequency Inversion Scrambler/Descrambler
  - Can Be Enabled/Disabled Via MPU Interface
  - Programmable Carrier Modulation Frequency
- 2.7 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices



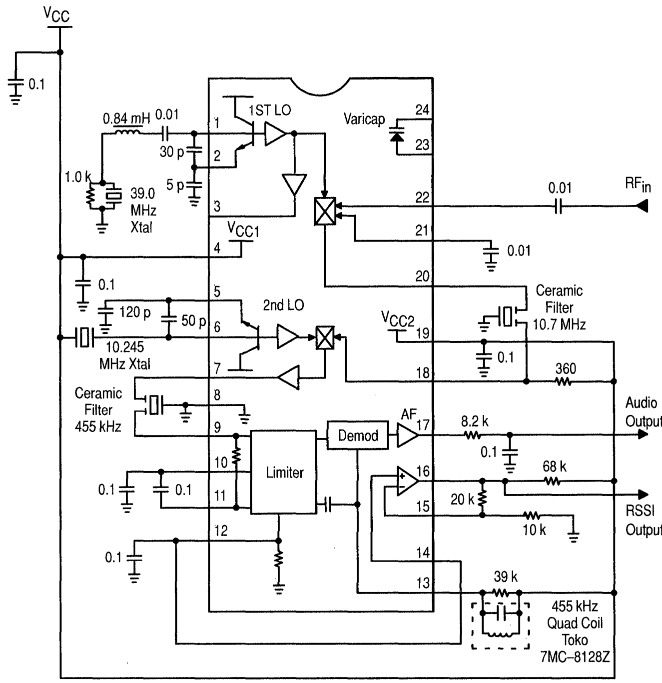
Narrowband FM Receiver

MC13135/136P, DW

T_A = –40° to +85°C, Case 724, 751E

The MC13135 is a full dual conversion receiver with oscillators, mixers, Limiting IF Amplifier, Quadrature Discriminator, and RSSI circuitry. It is designed for use in security systems, cordless phones, and VHF mobile and portable radios. Its wide operating supply voltage range and low current make it ideal for battery applications. The Received Signal Strength Indicator (RSSI) has 65 dB of dynamic range with a voltage output, and an operational amplifier is included for a dc buffered output. Also, an improved mixer third order intercept enables the MC13135 to accommodate larger input signal levels.

- Complete Dual Conversion Circuitry
- Low Voltage: 2.0 to 6.0 Vdc
- RSSI with Op Amp: 65 dB Range
- Low Drain Current: 3.5 mA Typical
- Improved First and Second Mixer 3rd Order Intercept
- Detector Output Impedance: 25 Ω Typically



Narrowband FM Coilless Detector IF Subsystem

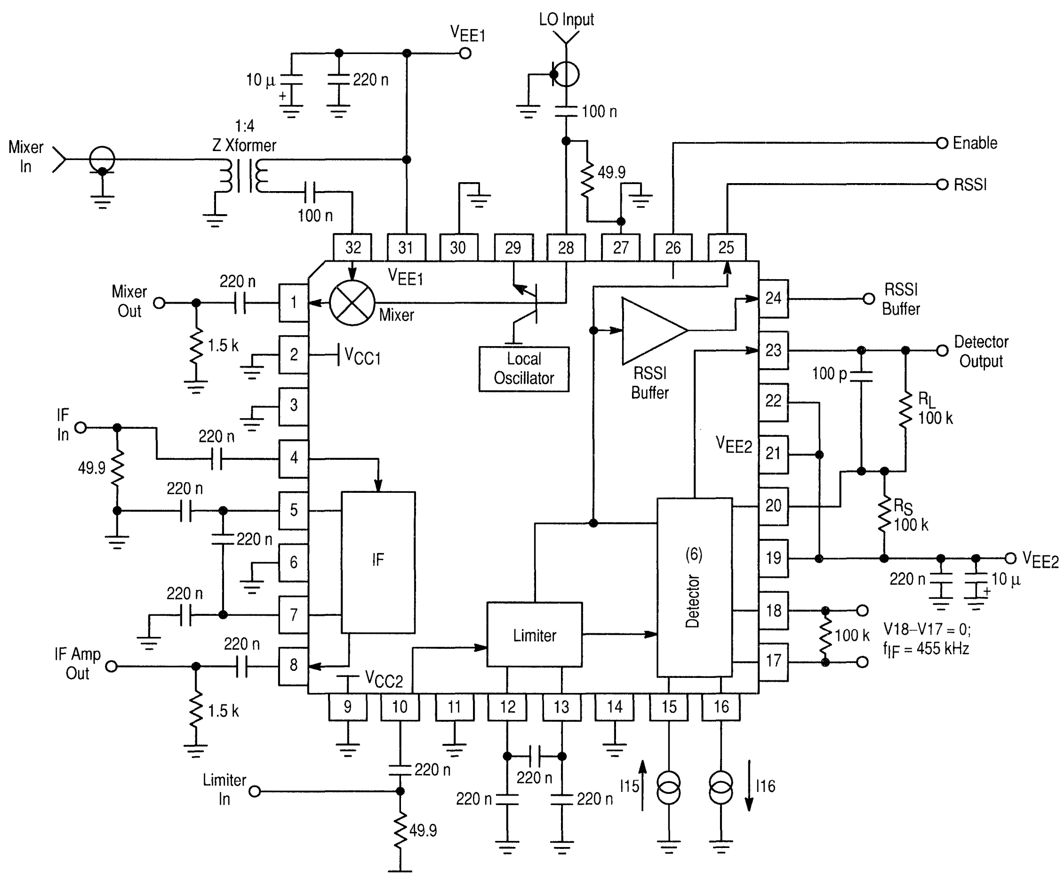
MC13150FTA, FTB

T_A = –40° to +85°C, Case 977, 873

The MC13150 is a narrowband FM IF subsystem targeted at cellular and other analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13150 has an onboard Colpitts VCO for Crystal controlled second LO in dual conversion receivers. The mixer is a double balanced configuration with excellent third order intercept. It is useful to beyond 200 MHz. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. The quadrature detector is a unique design eliminating the conventional tunable quadrature coil.

Applications for the MC13150 include cellular, CT–1 900 MHz cordless telephone, data links and other radio systems utilizing narrowband FM modulation.

- Linear Coilless Detector
- Adjustable Demodulator Bandwidth
- 2.5 to 6.0 Vdc Operation
- Low Drain Current: < 2.0 mA
- Typical Sensitivity of 2.0 μV for 12 dB SINAD
- IIP3, Input Third Order Intercept Point of 0 dBm
- RSSI Range of Greater Than 100 dB
- Internal 1.4 kΩ Terminations for 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range



Wideband FM IF System

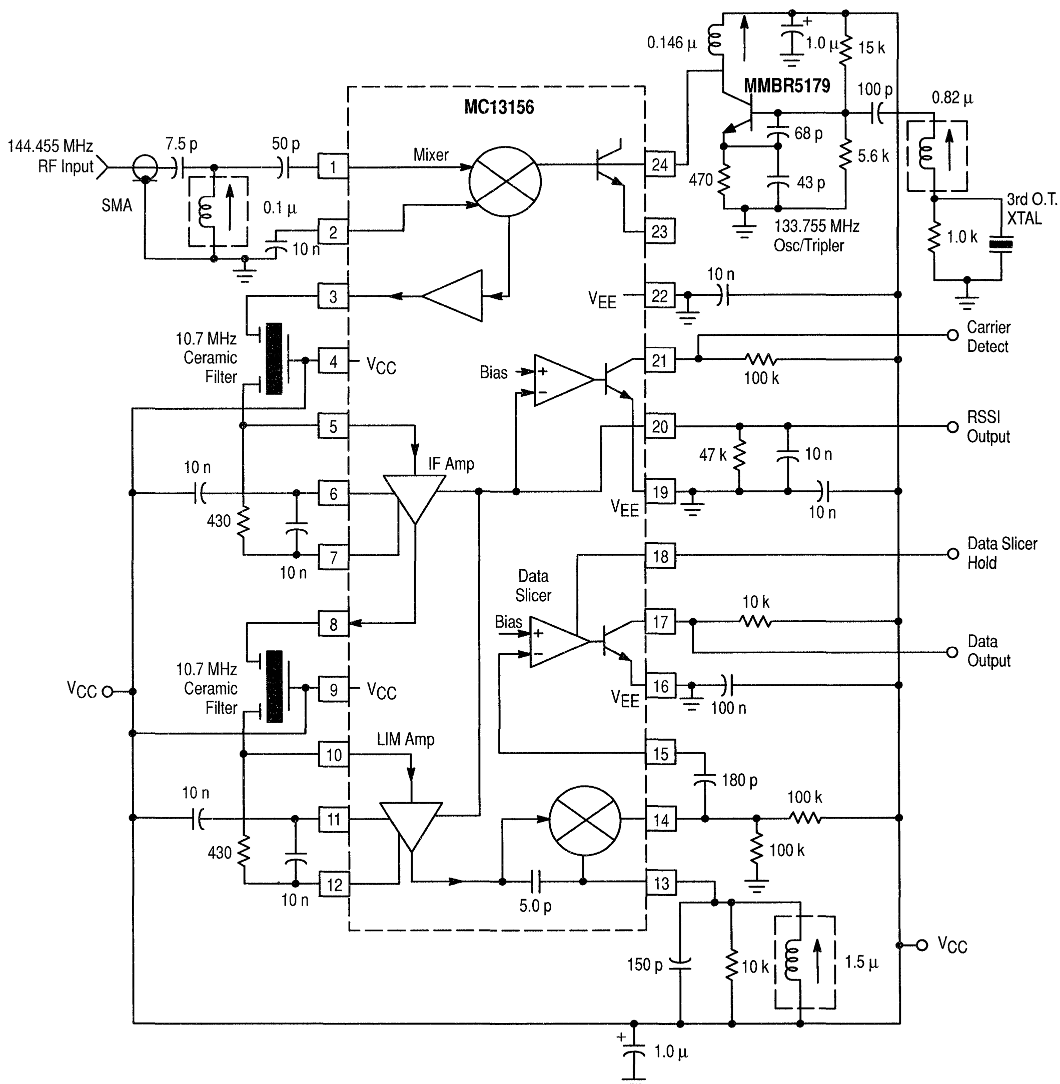
MC13156DW, FB

T_A = –40° to +85°C, Case 751E, 873

The MC13156 is a wideband FM IF subsystem targeted at high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13156 has an onboard Colpitts VCO for PLL controlled multichannel operation. The mixer is useful to beyond 200 MHz and may be used in a differential, balanced, or single–ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has a hold function to preset the shaper for fast recovery of new data.

Applications for the MC13156 include CT–2, wideband data links, and other radio systems utilizing GMSK, FSK or FM modulation.

- 2.0 to 6.0 Vdc Operation
- Typical Sensitivity of 6.0 µV for 12 dB SINAD
- RSSI Dynamic Range Typically 80 dB
- High Performance Data Shaper for Enhanced CT–2 Operation
- Internal 300 Ω and 1.4 kΩ Terminations for 10.7 MHz and 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range



Wideband FM IF Subsystem

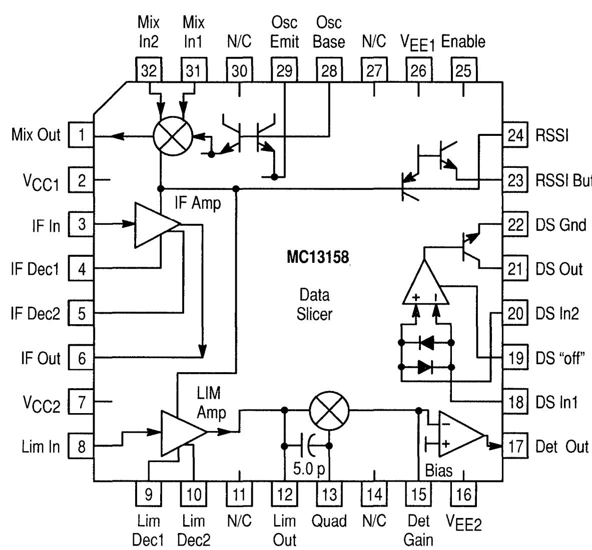
MC13158FTB

T_A = –40° to +85°C, Case 873

The MC13158 is a wideband IF subsystem that is designed for high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through the use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13158 has an on–board grounded collector VCO transistor that may be used with a fundamental or overtone crystal in single channel operation or with a PLL in multi–channel operation. The mixer is useful to 500 MHz and may be used in a balanced differential or single ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has an Off function to shut the output "off" to save current. An enable control is provided to power down the IC for power management in battery operated applications.

Applications include DECT, wideband wireless data links for personal and portable laptop computers and other battery operated radio systems which utilize GFSK, FSK or FM modulation.

- Designed for DECT Applications
- 1.8 to 6.0 Vdc Operating Voltage
- Low Power Consumption in Active and Standby Mode
- Greater than 600 kHz Detector Bandwidth
- Data Slicer with Special Off Function
- Enable Function for Power Down of Battery Operated Systems
- RSSI Dynamic Range of 80 dB Minimum
- Low External Component Count



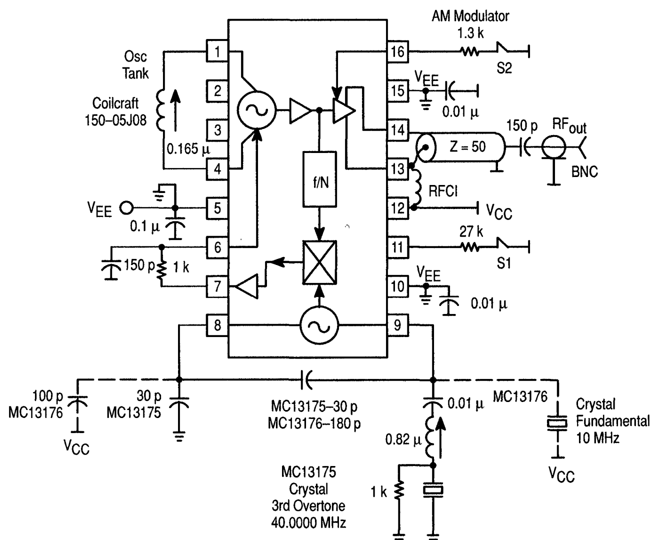
UHF, FM/AM Transmitter

MC13175/176D

T_A = 0° to +70°C, Case 751B

The MC13175 and MC13176 are one chip FM/AM transmitter subsystems designed for AM/FM communication systems operating in the 260 to 470 MHz band covered by FCC Title 47; Part 15. They include a Colpitts crystal reference oscillator, UHF oscillator, ÷8 (MC13175) or ÷32 (MC13176) prescaler, and phase detector forming a versatile PLL system. Another application is as a local oscillator in a UHF or 900 MHz receiver. MC13175/176 offer the following features:

- UHF Current Controlled Oscillator
- Use Easily Available 3rd Overtone or Fundamental Crystals for Reference
- Low Number of External Parts Required
- Low Operating Supply Voltage (1.8–5 Vdc)
- Low Supply Drain Currents
- Power Output Adjustable (Up to +10 dBm)
- Differential Output for Loop Antenna or Balun Transformer Networks
- Power Down Feature
- ASK Modulated by Switching Output "On"/"Off"
- MC13175 – $f_o = 8 \times f_{ref}$
- MC13176 – $f_o = 32 \times f_{ref}$



Telecommunications

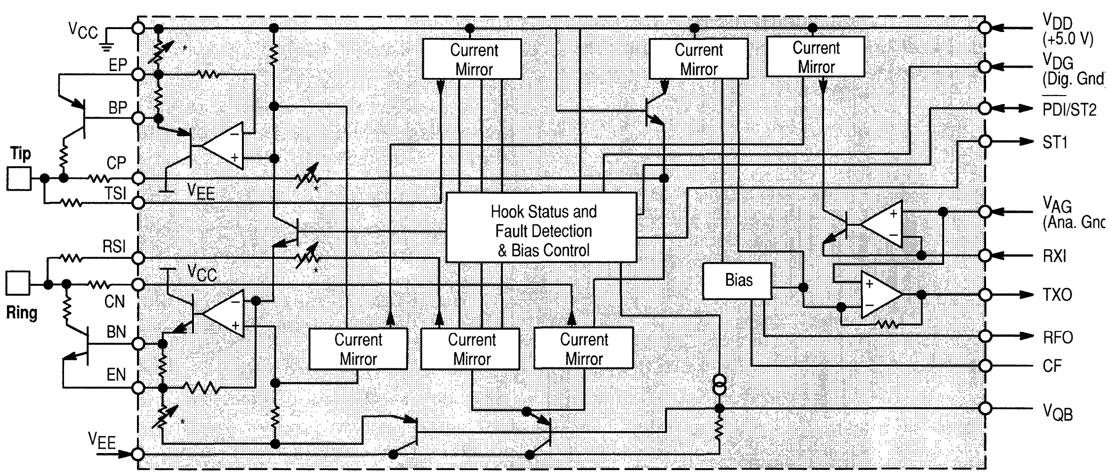
Subscriber Loop Interface Circuit (SLIC)

MC33120/1P, FN

T_A = –40° to +85°C, Case 738, 776

With a guaranteed minimum longitudinal balance of 58 dB, the MC33120/1 is ideally suited for Central Office applications, as well as PBXs, and other related equipment. Protection and sensing components on the two–wire side can be non–precision while achieving required system performance. Most BORSHT functions are provided while maintaining low power consumption, and a cost effective design. Size and weight reduction over conventional transformer designs permit a higher density system.

- All Key Parameters Externally Programmable with Resistors:
  - Transmit and Receive Gains
  - Transhybrid Loss
  - Return Loss
  - DC Loop Current Limit and Battery Feed Resistance
  - Longitudinal Impedance
- Single and Double Fault Sensing and Protection
- Minimum 58 dB Longitudinal Balance (2–wire and 4–wire) Guaranteed
- Digital Hook Status and Fault Outputs
- Power Down Input
- Loop Start or Ground Start Operation
- Size & Weight Reduction Over Conventional Approaches
- Available in 20 Pin DIP and 28 Pin PLCC Packages
- Battery Voltage: –42 to –58 V (for MC33120), –21.6 to –42 V (for MC33121)



(Battery)
* Indicates Trimmed Resistor

PBX Architecture (Analog Transmission)

PCM Mono–Circuits Codec–Filters (CMOS LSI)

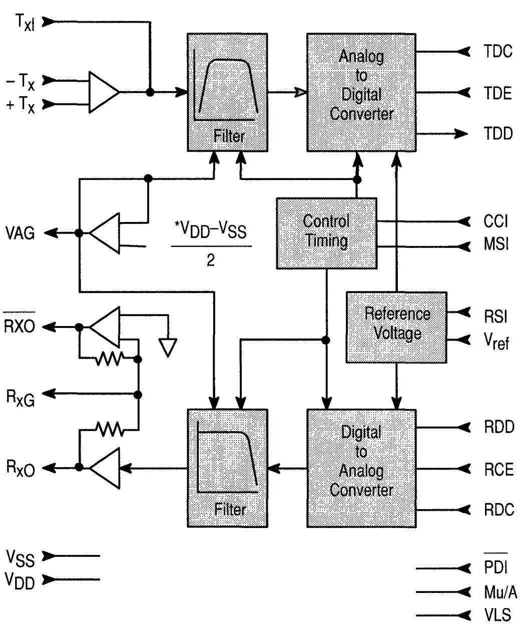
MC145500 Series

Case 648, 708, 751G, 776

The Mono–circuits perform the digitizing and restoration of the analog signals. In addition to these important functions, Motorola's family of pulse–code modulation mono–circuits also provides the band–limiting filter functions – all on a single monolithic CMOS chip with extremely low power dissipation.

The Mono–circuits require no external components. They incorporate the bandpass filter required for antialiasing and 60 Hz rejection, the A/D–D/A conversion functions for either U.S. Mu–Law or European A–Law companding formats, the low–pass filter required for reconstruction smoothing, an on–board precision voltage reference, and a variety of options that lend flexibility to circuit implementations. Unique features of Motorola's Mono–circuit family include wide power supply range (6.0 to 13 V), selectable on–board voltage reference (2.5, 3.1, or 3.8 V), and TTL or CMOS I/O interface.

Motorola supplies three versions in this series. The MC145503 and MC145505 are general–purpose devices in 16 pin packages designed to operate in digital telephone or line card applications. The MC145502 is the full–feature device that presents all of the options available on the chip. This device is packaged in a 22 pin DIP and 28 pin chip carrier package.



MC145554/57/64/67

Case 648, 751D, 751G, 738

These per channel PCM Codec–Filters perform the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. They are designed to operate in both synchronous and asynchronous applications and contain an on–chip precision voltage reference. The MC145554 (Mu–Law) and MC145557 (A–Law) are general purpose devices that are offered in 16 pin packages. The MC145564 (Mu–Law) and MC145567 (A–Law), offered in 20 pin packages, add the capability of analog loop–back and push–pull power amplifiers with adjustable gain.

All four devices include the transmit bandpass and receive lowpass filters on–chip, as well as active RC pre–filtering and post–filtering. Fully differential analog circuit design assures lowest noise. Performance is specified over the extended temperature range of –40° to +85°C.

These PCM Codec–Filters accept both industry standard clock formats. They also maintain compatibility with Motorola's family of MC3419/MC33120 SLIC products.

MC145480P, DW, SD

Case 738, 751D, 940C

This 5.0 V, general purpose per channel PCM Codec–Filter offers selectable Mu–Law or A–Law companding in 20 pin DIP, SOG and SSOP packages. It performs the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. It is designed to operate in both synchronous and asynchronous applications and contains an on–chip precision reference voltage (1.575 V).

The transmit bandpass and receive lowpass filters, and the active RC pre–filtering and post–filtering are incorporated, as well as fully differential analog circuit design for lowest noise. Push–pull 300 Ω power drivers with external gain adjust are also included.

The MC145480 PCM Codec–Filter accepts a variety of clock formats, including short–frame sync, long–frame sync, IDL, and GCI timing environments. This device also maintains compatibility with Motorola's family of Telecom products, including the MC145472 U–Interface Transceiver, MC145474/75 S/T–Interface Transceiver, MC145532 ADPCM Transcoder, MC145422/26 UDLT–I, MC145421/25 UDLT–II, and MC3419/MC33120 SLIC.

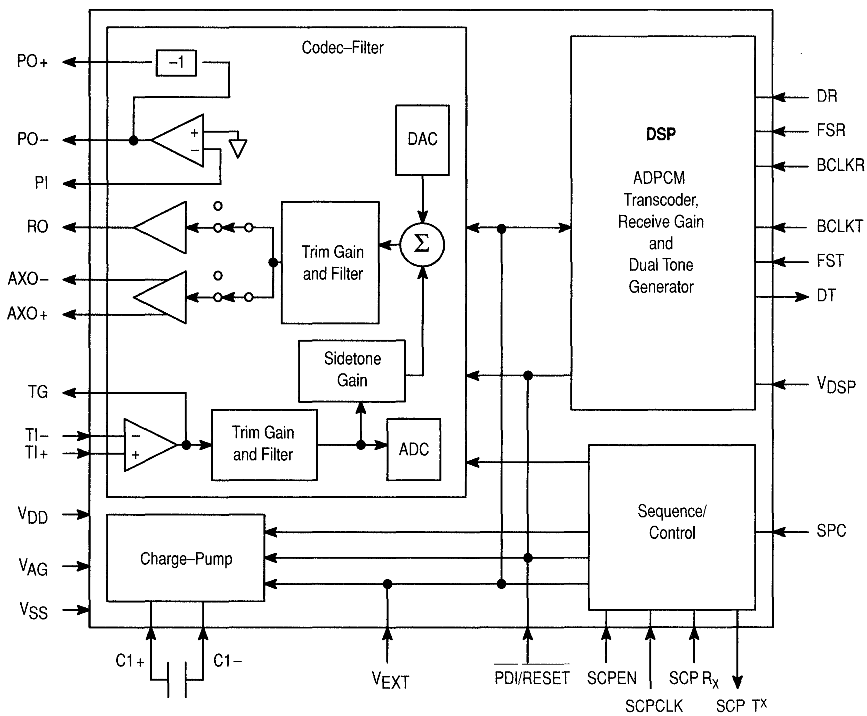
MC14LC5540P, DW, FU

Case 710, 751F, 873

The MC14LC5540 ADPCM Codec is a single chip implementation of a PCM Codec–Filter and an ADPCM encoder/decoder, and therefore provides an efficient solution for applications requiring the digitization and compression of voiceband signals. This device is designed to operate over a wide voltage range, 2.7 V to 5.25 V, and as such is ideal for battery powered as well as ac powered applications. The MC14LC5540 ADPCM Codec also includes a serial control port and internal control and status registers that permit a microcomputer to exercise many built–in features.

The ADPCM Codec is designed to meet the 32 kbps ADPCM conformance requirements of CCITT Recommendation G.721 (1988) and ANSI T1.301 (1987). It also meets ANSI T1.303 and CCITT Recommendation G.723 for 24 kbps ADPCM operation, and the 16 kbps ADPCM standard, CCITT Recommendation G.726. This device also meets the PCM conformance specification of the CCITT G.714 Recommendation.

Figure 25. MC14LC5540 ADPCM Codec Block Diagram



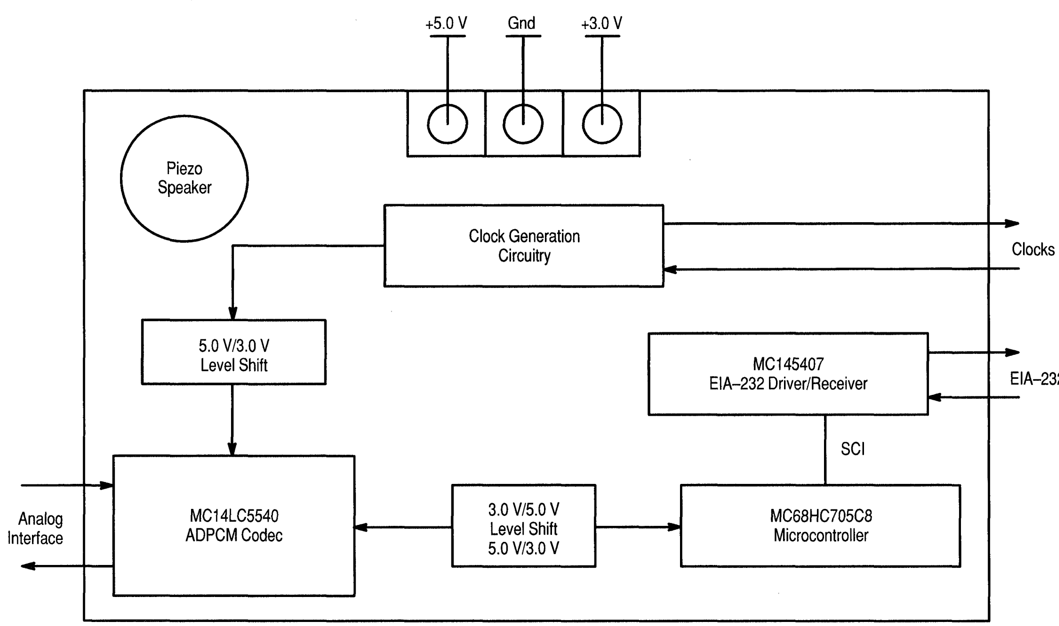
MC145537EVK

ADPCM Codec Evaluation Kit

The MC145537EVK is the primary tool for evaluation and demonstration of the MC14LC5540 ADPCM Codec. It provides the necessary hardware and software interface to access the many features and operational modes of the MC14LC5540 ADPCM Codec.

- Provides Stand Alone Evaluation on Single Board
- The kit provides Analog–to–Analog, Analog–to–Digital or Digital–to–Analog Connections – with Digital Connections being 64 kbps PCM, 32 or 24 kbps ADPCM, or 16 kbps CCITT G.726 or Motorola Proprietary ADPCM
- +5.0 V Only Power Supply, or 5.0 V Plus 2.7 to 5.25 V Supply
- Easily Interfaced to Test Equipment, Customer System, Second MC145537EVK or MC145536EVK (5.0 V Only) for Full Duplex Operation
- Convenient Access to Key Signals
- Piezo Loudspeaker
- EIA–232 Serial Computer Terminal Interface for Control of the MC14LC5540 ADPCM Codec Features
- Compatible Handset Provided
- Schematics, Data Sheets, and User's Manual Included

Figure 26. MC145537EVK Block Diagram

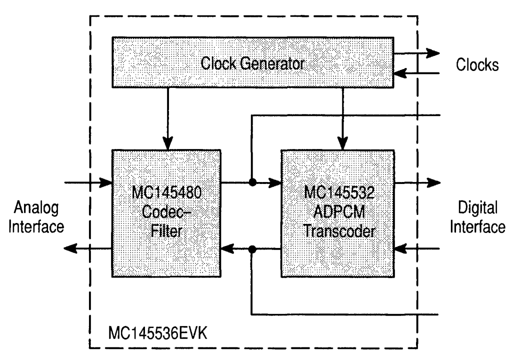


MC145536EVK

Codec–Filter/ADPCM Transcoder Evaluation Kit

The MC145536EVK is the primary tool for evaluation and demonstration of the MC145480 Single +5.0 V supply PCM Codec–Filter and the MC145532 ADPCM Transcoder (see "Telephone Accessory Circuits"). The MC145536EVK provides the necessary hardware needed to evaluate the many separate operating modes under which the MC145480 and MC145532 are intended to operate.

- Provides Stand Alone Evaluation on a Single Board
- Easily Interfaced to Test Equipment, Customer System, or Second MC145536EVK
- Convenient Access to Key Signals
- Generous Wire–Wrap Area for Application Development
- The kit provides Analog–to–Analog, Analog–to–Digital, or Digital–to–Analog Connections – with Digital Connections Being 64 kbps PCM; 32, 24, or 16 kbps Motorola Proprietary ADPCM
- Compatible Handset Included
- Schematics, Data Sheets, and User's Manual included



Dual Tone Multiple Frequency Receiver

MC145436AP, DW

Case 646, 751G

This device contains the filter and decoder for detection of a pair of tones conforming to the DTMF standard with outputs in hexadecimal. Switched capacitor filter technology is used together with digital circuitry for the timing control and output circuits. The MC145436A provides excellent power–line noise and dial tone rejection.

Replaces MC145436P, DW.

ISDN Voice/Data Circuits

Integrated Services Digital Network

ISDN is the revolutionary concept of converting the present analog telephone networks to an end–to–end global digital network. ISDN standards make possible a wide variety of services and capabilities that are revolutionizing communications in virtually every industry.

Motorola's ISDN product family includes the MC14LC5472 and MC145572 U–Interface Transceivers, the MC145474/75 and MC145574 S/T–Interface Transceivers, MC145488 Dual Data Link Controller, and the MC68302 Integrated Multi–Protocol Processor. These are supported by a host of related devices including the MC145480 +5.0 V PCM Codec–Filter, MC145532 ADPCM Transcoder, MC14LC5540 ADPCM Codec, MC145500 family of single–chip codec/filters, MC145436A DTMF Decoder, MC33120 Subscriber Loop Interface Circuit, MC34129 Switching Power Supply Controller, and the MC145406/07 CMOS EIA 232–E Driver/ Receiver family.

Motorola's key ISDN devices fit into four ISDN network applications: a digital subscriber line card, an NT1 network termination, an ISDN terminal adapter, and an ISDN terminal. Digital subscriber line cards are used in central offices, remote concentrators, channel banks, T1 multiplexers, and other switching equipment. The NT1 network termination block illustrates the simplicity of remote U– to S/T–interface conversion. The ISDN terminal adapter and ISDN terminal block show how Motorola ICs are used to combine voice and data in PC compatible boards, digital telephones, and other terminal equipment. Expanded applications such as a PBX may include these and other Motorola ISDN circuits. Many "non–ISDN" uses, such as pairgain applications, are appropriate for Motorola's ISDN devices as well.

Second Generation U–Interface Transceivers

MC145572PB

Case 842D

MC145572FN

Case 777

The MC145572 fully conforms to ANSI T1.601–1992, the North American standard for ISDN Basic Access on a single twisted–wire pair. The transceiver achieves a remarkable 10^{-7} bit error rate performance on all ANSI specified test loops with worst–case impairments present. The state–of–the–art 0.65 micron single–chip solution uses advanced design techniques to combine precision analog signal processing elements with three digital signal coprocessors to build an adaptively equalized echo cancelling receiver.

Two modes of handling U–interface maintenance functions are provided on the MC145572. In the automatic maintenance mode the U–interface transceiver handles all ANSI specified maintenance and channel procedures internally to minimize your software development effort. Automatic procedures include generating and monitoring the cyclic redundancy check, reporting and counting far end block errors (near end block errors too), handling the ACT and DEA bits, as well as monitoring and appropriately responding to embedded operations channel messages.

The MC145572 has 275 mW maximum power dissipation. It also has an enhanced TDM interface that supports an on–chip timeslot assigner, GCI and IDL modes of operation.

The optional manual maintenance mode lets you choose an inexpensive microcontroller, such as a member of Motorola's MC68HC05 family, to control and augment the standard maintenance channel functions. This flexible feature also allows for easy implementation of proprietary maintenance functions.

Second Generation S/T–Interface Transceivers

MC145574PB

Case 736B

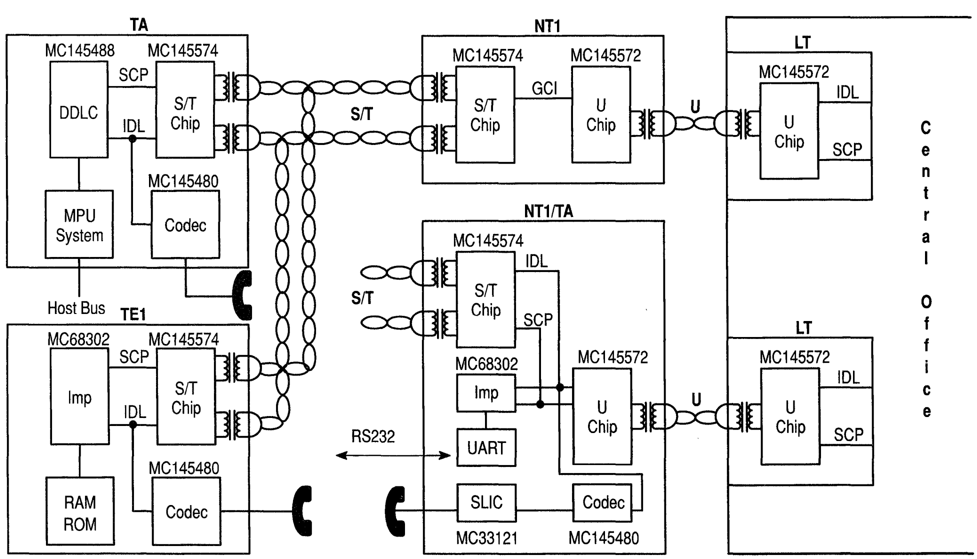
MC145574DW

Case 837A

The MC145574 S/T–Interface Transceivers provide a CCITT I.430 compatible interface for use in line card, network termination, and ISDN terminal equipment applications. Manufactured with Motorola's advanced 0.65 micron CMOS mixed analog and digital process technology, the MC145574 is a physical layer device capable of operating in point–to–point or point–to–multipoint passive bus arrangements. In addition, the MC145574 implements the optional NT1 Star topology, NT terminal mode and TE slave mode.

This device features outstanding transmission performance. It reliably transmits over 1 kilometer in a point–to–point application. Comparable performance is achieved in all other topologies as well. Other features include pin selectable terminal or network operating modes, industry standard microprocessor serial control port, full support of the multiframing S and Q channels, a full range of loopbacks, and low power CMOS operation, with a maximum power consumption of 90 mW.

The MC145574 has an enhanced TDM interface that supports GCI, IDL and an on–chip timeslot assigner.



Dual Data Link Controller

MC145488FN
Case 779

The MC145488 features two full–duplex serial HDLC channels with an on–chip Direct Memory Access (DMA) controller. The DMA controller minimizes the number of microprocessor interrupts from the communications channels, freeing the microprocessor's resources for other tasks. The DMA controller can access up to 64 kbytes of memory, and transfers either 8–bit bytes or 16–bit words to or from memory. The MC145488 DDLC is compatible with Motorola's MC68000 and other microprocessors.

In a typical ISDN terminal application, one DDLC communications channel supports the D–channel (LAPD) while the other supports the B–channel (LAPB). While the DDLC is ideally suited for ISDN applications, it can support many other HDLC protocol applications as well.

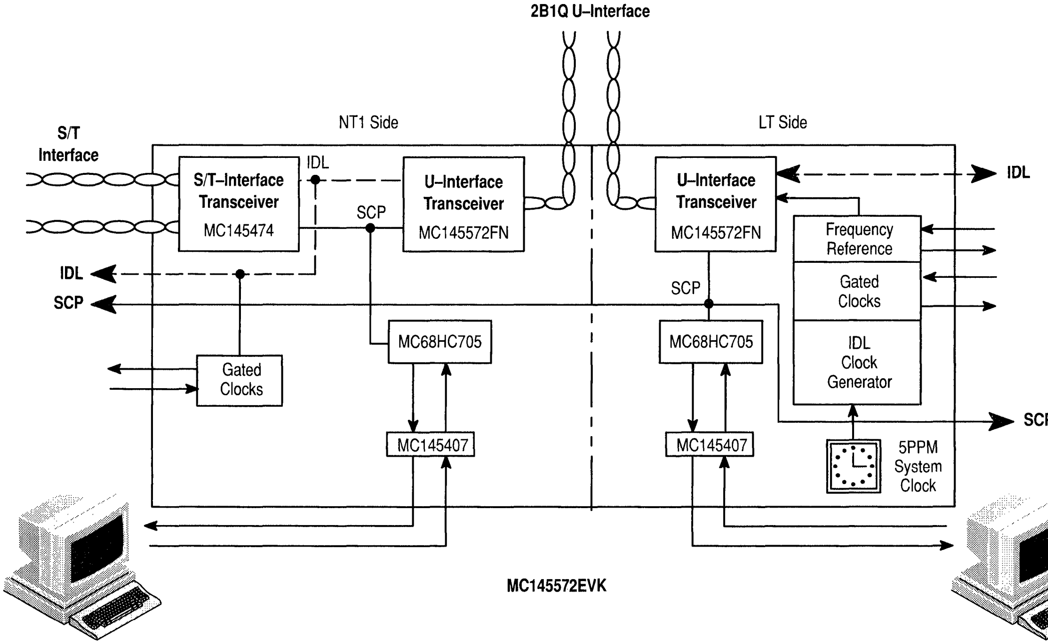
Some of the powerful extras found on the DDLC include automatic abort and retransmit of D–channel collisions in S/T–interface applications, address recognition, automatic recovery mechanisms for faulty frame correction, and several system test modes. Address recognition provides a reduction in the host microprocessor load by filtering data frames not addressed to the host. The DDLC can compare either SAPI or TEI fields of LAPD frames. For LAPD (Q.921) applications, both A and B addresses may be checked.

MC14LC5494EVK
U–Interface Transceiver Evaluation Kit discontinued

MC145572EVK
U–Interface Transceiver Evaluation Kit

This kit provides the hardware and software to evaluate the many configurations under which the MC145572EVK is able to operate. Used as a whole, it operates as both ends of the two–wire U interface that extends from the customer premises (NT1) to the switch line card (LT). The two halves of the board can be physically and functionally separated, providing independent NT1 and LT evaluation capability.

The kit provides the ability to interactively manipulate status registers in the MC145572EVK U–Interface transceiver or in the MC145474/75 S/T–Interface transceiver with the aid of an external terminal. The device can also be controlled using the MC68302 Integrated Multiprotocol Processor application development system to complete a total Basic Rate ISDN evaluation solution.



MC145572EVK

Voice/Data Communication (Digital Transmission)

2–Wire Universal Digital Loop Transceiver (UDLT)

MC145422P, DW Master Station

Case 708, 751E

MC145426P, DW Slave Station

Case 708, 751E

The UDLT family of transceivers allows the use of existing twisted–pair telephone lines (between conventional telephones and a PBX) for the transmission of digital data. With the UDLT, every voice–only telephone station in a PBX system can be upgraded to a digital telephone station that handles the complex voice/data communications with no increase in cabling costs.

In implementing a UDLT–based system the A/D to D/A conversion function associated with each telset is relocated from the PBX directly to the telset. The SLIC (or its equivalent circuit) is eliminated since its signaling information is transmitted digitally between two UDLTs.

The UDLT master–slave system incorporates the modulation/demodulation functions that permit data communications over a distance up to 2 kilometers. It also provides the sequence control that governs the exchange of information between master and slave. Specifically, the master resides on the PBX line card where it transmits and receives data over the wire pair to the telset. The slave is located in the telset and interfaces the mono–circuit to the wire pair. Data transfer occurs in 10–bit bursts (8 bits of data and 2 signaling bits), with the master transmitting first, and the slave responding in a synchronized half–duplex transmission format.

UDLTs utilize a 256 kilobaud Modified Differential Phase Shift Keyed (MDPSK) burst modulation technique for transmission to minimize radio frequency, electromagnetic, and crosstalk interference. Implementation through CMOS technology takes advantage of low–power operation, increased reliability, and the proven capabilities to perform complex telecommunications functions.

Functional Features

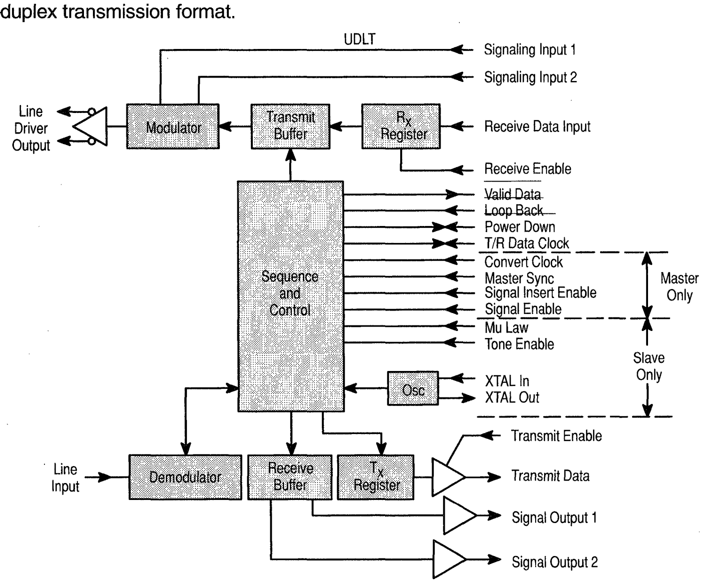
- Provides Synchronous Duplex 64 kbits/Second Voice/Data Channel and Two 8 kbits/Second Signaling Data Channels Over One 26 AWG Wire Pair Up to 2 km.
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signaling Schemes
- Automatic Detection Threshold Adjustment for Optimum Performance Over Varying Signal Attenuations
- Protocol Independent
- Single 5.0 V to 8.0 V Power Supply

MC145422 Master UDLT

- 2.048 MHz Master Clock
- Pin Controlled Power–Down and Loop–Back Features
- Variable Data Clock – 64 kHz to 2.56 MHz
- Pin Controlled Insertion/Extraction of 8 kbits/Seconds Channel into LSB of 64 kbits/Second Channel for Simultaneous Routing of Voice and Data Through PCM Voice Path of Telephone Switch

MC145426 Slave UDLT

- Compatible with MC145500 Series and Later PCM Mono–Circuits
- Automatic Power–Up/Down Feature
- On–Chip Data Clock Recovery and Generation
- Pin Controlled 500 Hz D3 or CCITT Format PCM Tone Generator for Audible Feedback Applications



2–Wire ISDN Universal Digital Loop Transceiver II (UDLT II)

MC145421P, DW Master
Case 709, 751E

MC145425P, DW Slave
Case 709, 751E

Similar to the MC145422/26 UDLT, but provide synchronous full duplex 160 kbps voice and data communication in a 2B + 2D format for ISDN compatibility on a single twisted pair up to 1 km. Single 5.0 V power supply, protocol independent.

Electronic Telephone

The Complete Electronic Telephone Circuit

MC34010P, FN

T_A = –20° to +60°C, Case 711, 777

The conventional transformer–driven telephone handset is undergoing major innovations. The bulky transformer is disappearing. So are many of its discrete components, including the familiar telephone bell. They are being replaced with integrated circuits that perform all the major handset functions simply, reliably and inexpensively . . . functions such as 2–to–4 wire conversion, DTMF dialing, tone ringing, and a variety of related activities.

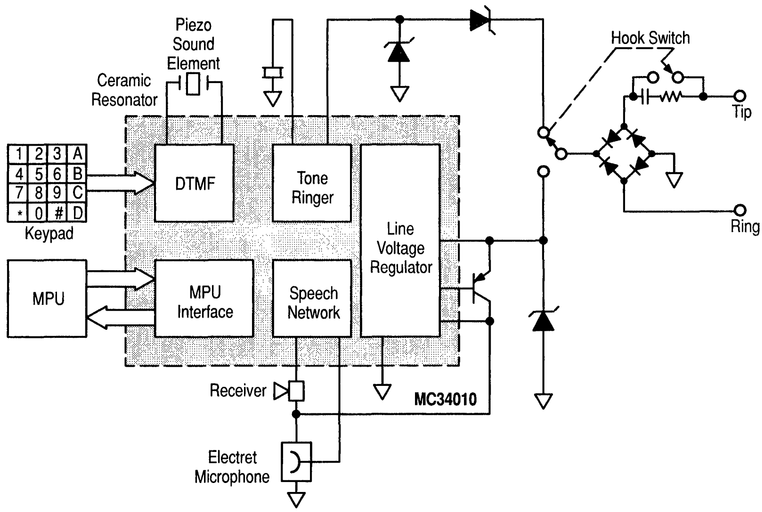
The culmination of these capabilities is the Electronic Telephone Circuit, the MC34010. These ICs place all of the above mentioned functions on a single monolithic chip.

These telephone circuits utilize advanced bipolar analog (I^2L) technology and provide all the necessary elements of a modern tone–dialing telephone. The MC34010 even incorporates an MPU interface circuit for the inclusion of automatic dialing in the final system.

- Provides all basic telephone functions, including DTMF dialer, tone ringer, speech network and line voltage regulator
- DTMF generator uses low cost ceramic resonator with accurate frequency synthesis technique
- Tone ringer drives piezoelectric transducer and satisfies EIA–470 requirements
- Speech network provides 2–to–4 wire conversion with adjustable sidetone utilizing an electret transmitter
- On–chip regulator insures stable operation over wide range of loop lengths
- I^2L technology provides low 1.4 V operation and high static discharge immunity
- Microprocessor interface port for automatic dialing features

Also Available

A broad line of additional telephone components for customizing systems design.



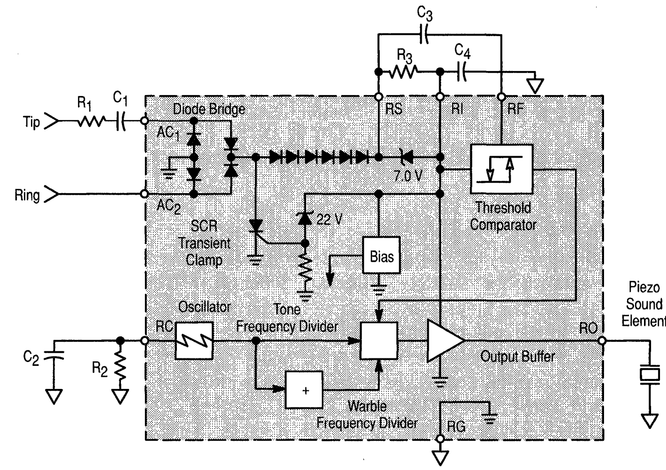
Tone Ringers

The MC34012, MC34017, and MC34117 Tone Ringers are designed to replace the bulky bell assembly of a telephone, while providing the same function and performance under a variety of conditions. The operational requirements spelled out by the FCC and EIA–470, simply stated, are that a ringer circuit MUST function when a ringing signal is provided, and MUST NOT ring when other signals (speech, dialing, noise) are on the line. The tone ringers described below were designed to meet those requirements with a minimum of external components.

MC34012P, D

T_A = –20° to +60°C, Case 626, 751

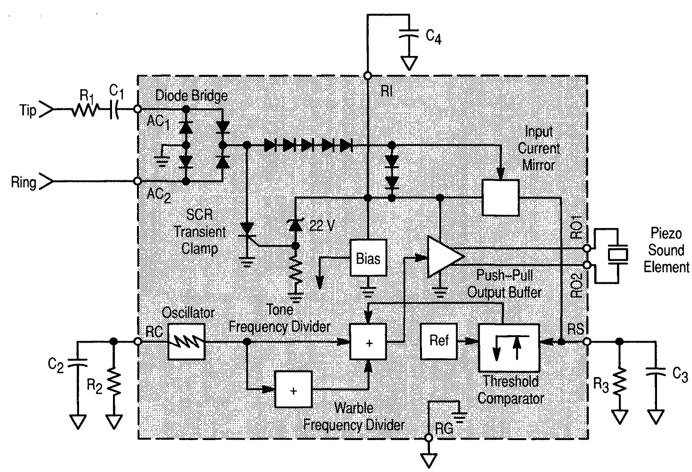
- Complete Telephone Bell Replacement
- On–Chip Diode Bridge and Transient Protection
- Single–Ended Output to Piezo Transducer
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial and Hook Switch Transients
- Adjustable Base Frequencies
- Output Frequency to Warble Ratio –
  - MC34012–1:80
  - MC34012–2:160
  - MC34012–3:40



MC34017P, D

T_A = –20° to +60°C, Case 626, 751

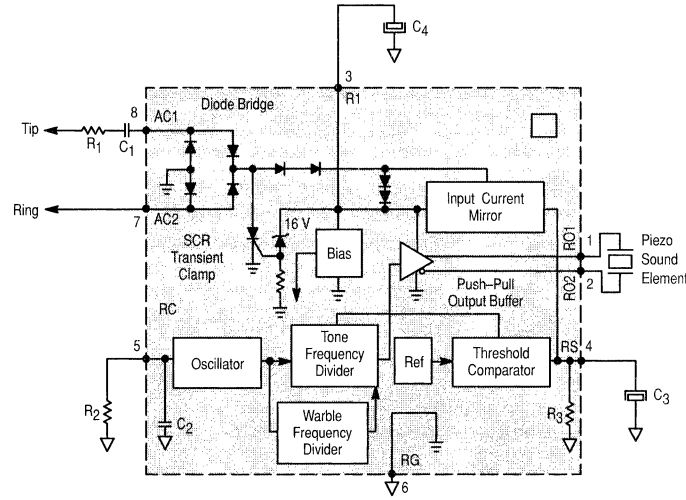
- Complete Telephone Bell Replacement
- On–Chip Diode Bridge and Transient Protection
- Differential Output to Piezo Transducer for Louder Sound
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial and Hook Switch Transients
- Output Frequency to Warble Ratio –
  - MC34017–1:80
  - MC34017–2:160
  - MC34017–3:40



MC34217P, D

T_A = –20° to +60°C, Case 626, 751

- Complete Telephone Bell Replacement
- On–Chip Diode Bridge
- Internal Transient Protection
- Differential Output to Piezo Transducer for Louder Sound
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial and Hook Switch Transients
- Base Frequency and Warble Frequencies are Independently Adjustable
- Adjustable Base Frequency
- Reduced Number of Externals



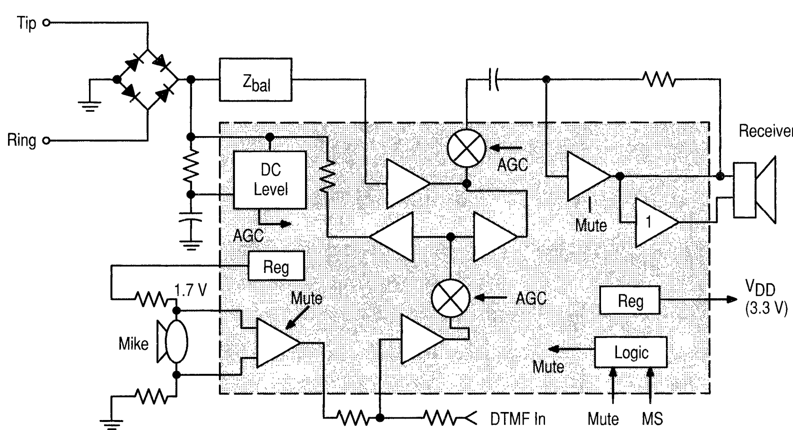
Speech Networks

Telephone Speech Network with Dialer Interface

MC34114P, DW

T_A = –20° to +70°C, Case 707, 751D

- Operation Down to 1.2 V
- Adjustable Transmit, Receive, and Sidetone Gains by External Resistors
- Differential Microphone Amplifier Input Minimizes RFI
- Transmit, Receive, and Sidetone Equalization on both Voice and DTMF Signals
- Regulated 1.7 V Output for Biasing Microphone
- Regulated 3.3 V Output for Powering External Dialer
- Microphone and Receive Amplifiers Muted During Dialing
- Differential Receive Amplifier Output Eliminates Coupling Capacitor
- Operates with Receiver Impedances of 150 Ω and Higher



Cordless Universal Telephone Interface

MC34016DW, P

T_A = –20° to +70°C, Case 751D, 738

The MC34016 is a telephone line interface meant for use in cordless telephone base stations for CT0, CT1, CT2 and DECT. The circuit forms the interface towards the telephone line and performs all speech and line interface functions like dc and ac line termination, 2–4 wire conversion, automatic gain control and hookswitch control. Adjustment of transmission parameters is accomplished by two 8 bit registers accessible via the integrated serial bus interface and by external components.

- DC Masks for Voltage and Current Regulation
- Supports Passive or Active AC Set Impedance Applications
- Double Wheatstone Bridge Sidetone Architecture
- Symmetrical Inputs and Outputs with Large Signal Swing Capability
- Gain Setting and Mute Function for T_X and R_X Amplifiers
- Very Low Noise Performance
- Serial Bus Interface SPI Compatible
- Operation from 3.0 V to 5.5 V

FEATURES

Line Driver Architecture

- Two DC Masks for Voltage Regulation
- Two DC Masks for Current Regulation
- Passive or Active Set Impedance Adjustment
- Double Wheatstone Bridge Architecture
- Automatic Gain Control Function

Transmit Channel

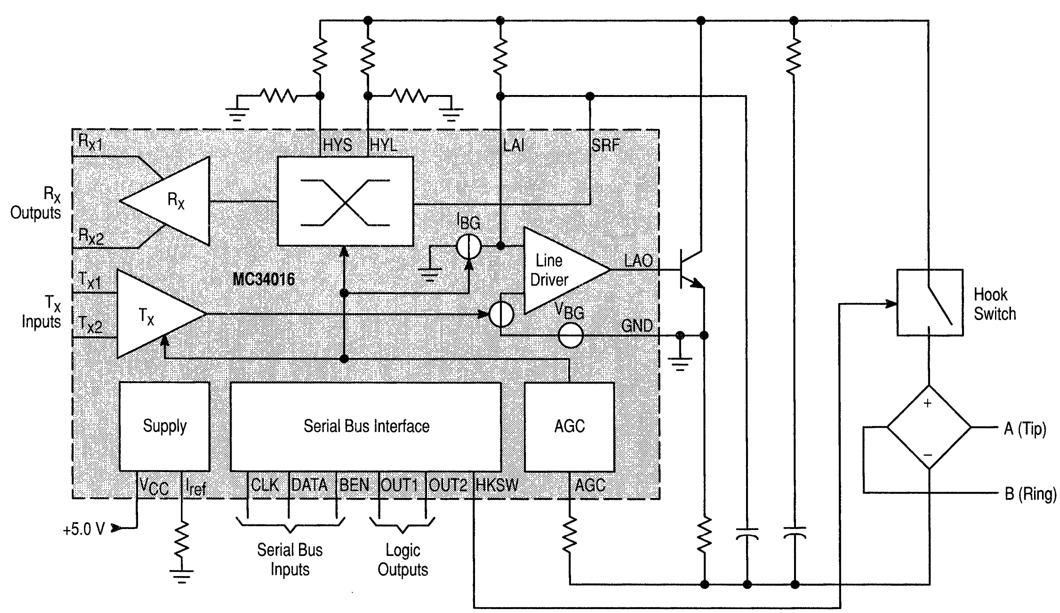
- Symmetrical Inputs Capable of Handling Large Voltage Swing
- Gain Select Option via Serial Bus Interface
- Transmit Mute Function, Programmable via Bus
- Large Voltage Swing Capability at the Telephone Line

Receive Channel

- Double Sidetone Architecture for Optimum Line Matching
- Symmetrical Outputs Capable of Producing High Voltage Swing
- Gain Select Option via Serial Bus Interface
- Receive Mute Function, Programmable via Serial Bus

Serial Bus Interface

- 3–Wire Connection to Microcontroller
- One Programmable Output Meant for Driving a Hookswitch
- Two Programmable Outputs Capable of Driving Low Ohmic Loads
- Two Eight Bit Registers for Parameter Adjustment



Programmable Telephone Line Interface Circuit with Loudspeaker Amplifier

MC34216DW

T_A = 0° to +70°C, Case 751F

The MC34216 is developed for use in telephone applications where besides the standard telephone functions also the group listening–in feature is required. In cooperation with a microcontroller, the circuit performs all basic telephone functions including DTMF generation and pulse–dialing. The listening–in part includes a loudspeaker amplifier, an anti–howling circuit and a strong supply. In combination with the TCA3385, the ringing is performed via the loudspeaker.

FEATURES

Line Driver and Supply

- DC and AC Termination of the Line
- Selectable Masks: France, U.K., Low Voltage
- Current Protection
- Adjustable Set Impedance for Resistive and Complex Termination
- Efficient Supply Point for Loudspeaker Amplifier and Peripherals

Handset Operation

- Transmit and Receive Amplifiers
- Adjustable Sidetone Network
- Line Length AGC
- Microphone and Earpiece Mute
- Earpiece Gain Increase Switch
- Microphone Squelch Function
- Transmit Amplifier Soft Clipping

Dialing and Ringing

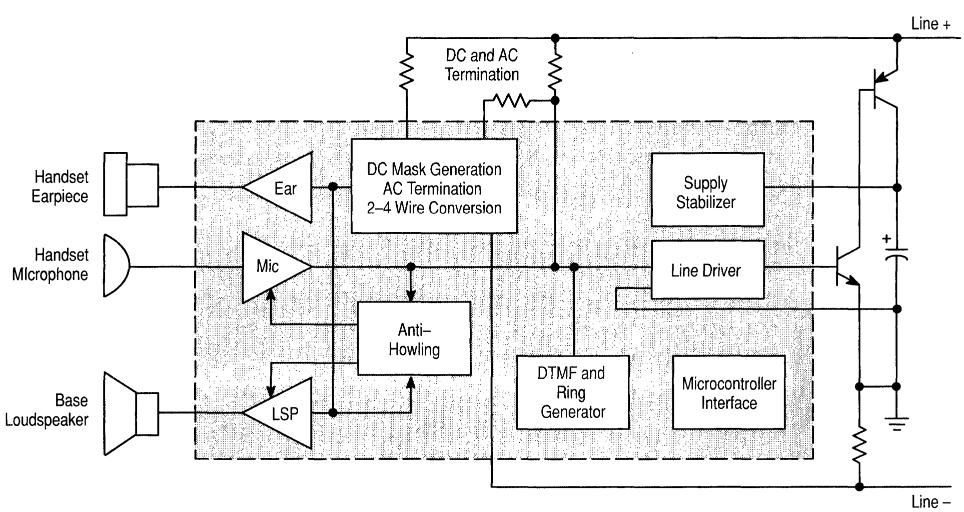
- Generates DTMF, Pilot Tones and Ring Signal
- Interrupter Driver for Pulse–Dialing
- Low Current While Pulse–Dialing
- Optimized for Ringing via Loudspeaker
- Programmable Ring Melodies
- Uses Inexpensive 500 kHz Resonator

Loudspeaking Facility

- Integrated Loudspeaker Amplifier
- Peak–to–Peak Limiter Prevents Distortion
- Programmable Volume
- Anti–Howling Circuitry for Group Listening–In
- Interfacing for Handsfree Conversation

Application Areas

- Corded Telephony with Group Listening–In
- Cordless Telephony Base Station with Group Listening–In
- Telephones with Answering Machines
- Fax, Intercom, Modem



Telephone Line Interface

TCA3388DP, FP

T_A = 0° to +70°C, Case 738, 751D

The TCA3388 is a telephone line interface circuit which performs the basic functions of a telephone set in combination with a microcontroller and a ringer. It includes dc and ac line termination, the hybrid function with 2 adjustable sidetone networks, handset connections and an efficient supply point.

FEATURES

Line Driver and Supply

- DC and AC Termination of the Telephone Line
- Selectable DC Mask: France, U.K., Low Voltage
- Current Protection
- Adjustable Set Impedance for Resistive and Complex Termination
- Efficient Supply Point for Peripherals
- Hook Status Detection

Handset Operation

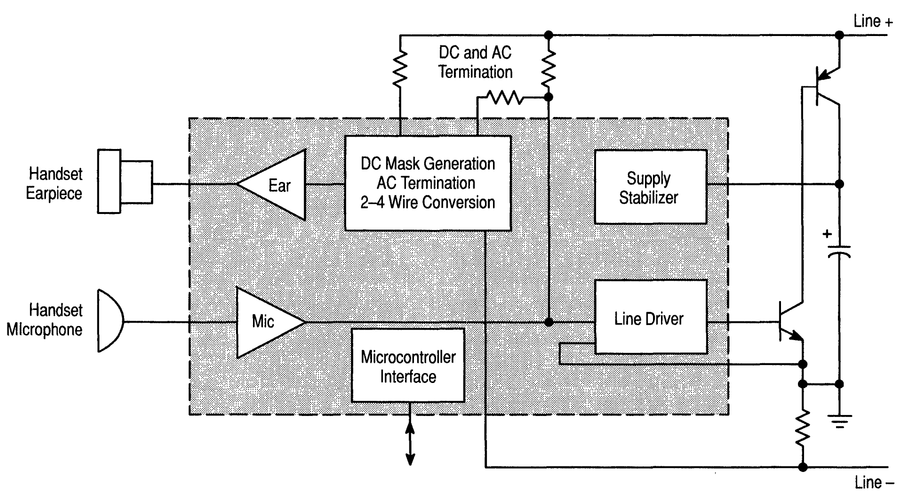
- Transmit and Receive Amplifiers
- Double Anti–Sidetone Network
- Line Length AGC
- Microphone and Earpiece Mute
- Transmit Amplifier Soft Clipping

Dialing and Ringing

- Interrupter Driver for Pulse–Dialing
- Reduced Current Consumption During Pulse–Dialing
- DTMF Interfacing
- Ringing via External Ringer

Application Areas

- Corded Telephony
- Cordless Telephony Base Station
- Answering Machines
- Fax
- Intercom
- Modem



Speakerphones

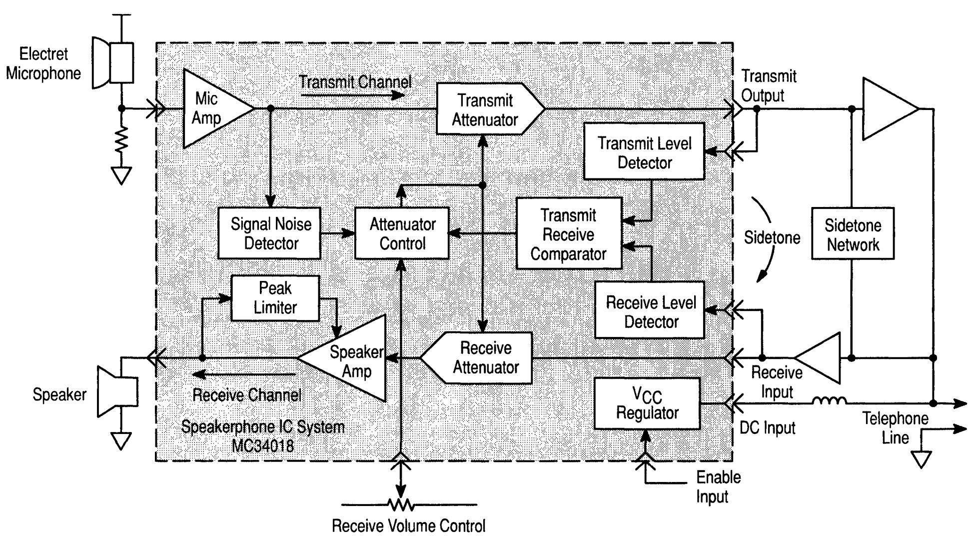
Voice Switched Speakerphone Circuit

MC34018P, DW

T_A = –20° to +60°C, Case 710, 751F

The MC34018 Speakerphone integrated circuit incorporates the necessary amplifiers, attenuators, and control functions to produce a high quality hands–free speakerphone system. Included are a microphone amplifier, a power audio amplifier for the speaker, transmit and receive attenuators, a monitoring system for background sound level, and an attenuation control system which responds to the relative transmit and receive levels as well as the background level. Also included are all necessary regulated voltages for both internal and external circuitry, allowing line–powered operation (no additional power supplies required). A Chip Select pin allows the chip to be powered down when not in use. A volume control function may be implemented with an external potentiometer. MC34018 applications include speakerphones for household and business uses, intercom systems, automotive telephones, and others.

- All Necessary Level Detection and Attenuation Controls for a Hands–Free Telephone in a Single Integrated Circuit
- Background Noise Level Monitoring with Long Time Constant
- Wide Operating Dynamic Range Through Signal Compression
- On–Chip Supply and Reference Voltage Regulation
- Typical 100 mW Output Power (into 25 Ω) with Peak Limiting to Minimize Distortion
- Chip Select Pin for Active/Standby Operation
- Linear Volume Control Function



Voice Switched Speakerphone Circuit

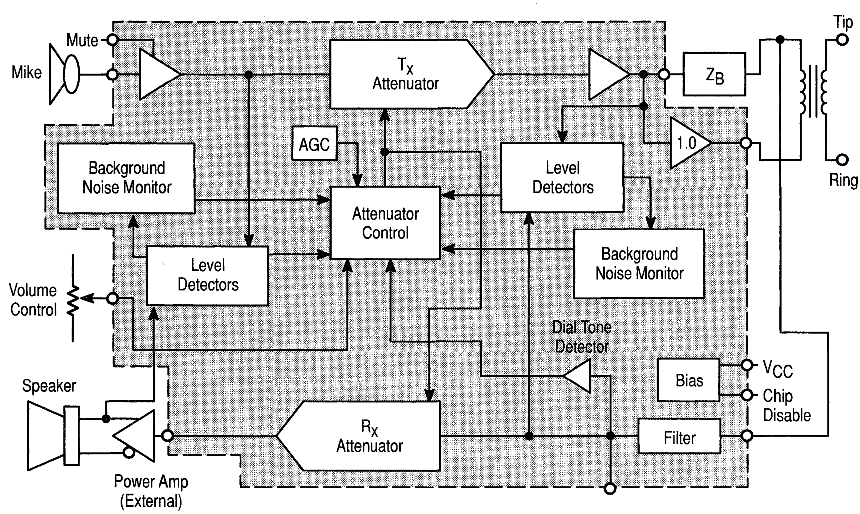
MC34118P, DW

T_A = –20° to +60°C, Case 710, 751F

The MC34118 Voice Switched Speakerphone circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands–free speakerphone system. Included are a microphone amplifier with adjustable gain and mute control, Transmit and Receive attenuators which operate in a complementary manner, level detectors at input and output of both attenuators,and background noise monitors for both the transmit and receive channels. A dial tone detector prevents the dial tone from being attenuated by the Receive background noise monitor circuit. Also included are two line driver amplifiers which can be used to form a hybrid network in conjunction with an external coupling transformer. A high–pass filter can be used to filter out 60 Hz noise in the receive channel, or for other filtering functions. A Chip Disable pin permits powering down the entire circuit to conserve power on long loops where loop current is at a minimum.

The MC34118 may be operated from a power supply, or it can be powered from the telephone line, requiring typically 5.0 mA. The MC34118 can be interfaced directly to Tip and Ring (through a coupling transformer) for stand–alone operation, or it can be used in conjunction with a handset speech network and/or other features of a featurephone.

- Improved Attenuator Gain Range: 52 dB Between Transmit and Receive
- Low Voltage Operation for Line–Powered Applications (3.0 to 6.5 V)
- 4–Point Signal Sensing for Improved Sensitivity
- Background Noise Monitors for Both Transmit and Receive Paths
- Microphone Amplifier Gain Set by External Resistors – Mute Function Included
- Chip Disable for Active/Standby Operation
- On Board Filter Pinned–Out for User Defined Function
- Dial Tone Detector Inhibits Receive Idle Mode During Dial Tone Presence
- Compatible with MC34119 Speaker Amplifier



Voice Switched Speakerphone with μProcessor Interface

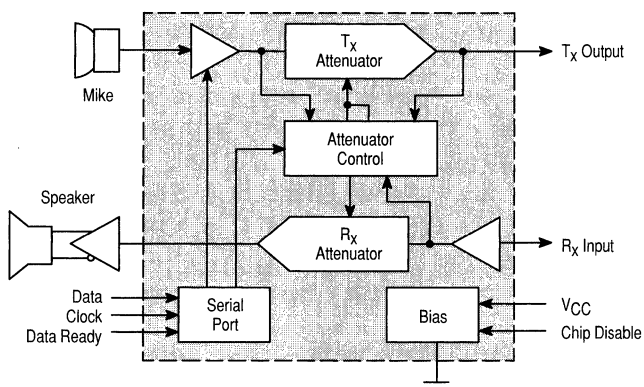
MC33218AP, DW

T_A = –40° to +85°C, Case 724, 751E

The MC33218A, Voice Switched Speakerphone circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands–free speakerphone system. Included are a microphone amplifier with adjustable gain, and mute control, transmit and receive attenuators which operate in a complementary manner, and level detectors and background noise monitors for both paths. A dial tone detector prevents dial tone from being attenuated by the receive background noise monitor. A Chip Disable pin permits powering down the entire circuit to conserve power.

Also included is an 8–bit serial μprocessor port for controlling the receive volume, microphone mute, attenuator gain, and operation mode (force to transmit, force to receive, etc.). Data rate can be up to 1.0 MHz. The MC33218A can be operated from a power supply, or from the telephone line, requiring typically 3.8 mA. It can also be used in intercoms and other voice–activated applications.

- Low Voltage Operation: 2.5 to 6.0 V
- 2–Point Sensing, Background Noise Monitor in Each Path
- Chip Disable Pin for Active/Standby Operation
- Microphone Amplifier Gain Set by External Resistors – Mute Function Included
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence
- Microprocessor port for controlling:
  - Receive Volume Level (16 Steps)
  - Attenuator Range (26 or 52 dB, Selectable)
  - Microphone Mute
  - Force to Transmit, Receive, Idle or Normal Voice Switched Operation
- Compatible with MC34119 Speaker Amplifier



Voice Switched Speakerphone Circuit

MC33219AP, ADW

T_A = –40° to +85°C, Case 724, 751E

The MC33219A Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands–free speakerphone system. Included are a microphone amplifier with adjustable gain, and mute control, transmit and receive attenuators which operate in a complementary manner, and level detectors and background noise monitors. A dial tone detector prevents dial tone from being attenuated by the receive background noise monitor. A Chip Disable pin permits powering down the entire circuit to conserve power.

The MC33219A may be operated from a power supply, or it can be powered from the telephone line requiring typically 4.0 mA. The MC33219A can be interfaced directly to Tip and Ring (through a coupling transformer for stand–alone operation, or it can be used in conjuction with a handset speech network and/or other features of a featurephone.

- Low Voltage Operation: 2.7 to 6.0 V
- 2–Point Sensing, Background Noise Monitor in Each Path
- Chip Disable Pin for Active/Standby Operation
- Microphone Amplifier Gain Set by External Resistors – Mute Function Included
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence
- Volume Control Range: 34 dB
- Compatible with MC34119 Speaker Amplifier

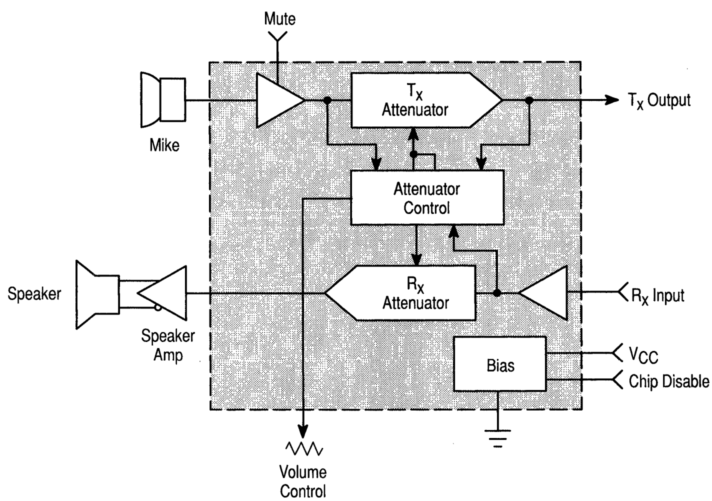


Table 9. The Motorola Family of Speakerphone Integrated Circuits

MC34018	MC34118	MC33218A	MC33219A
Two point sensing with slow idle, background noise monitor in T_X path only	Four point sensing with both fast and slow idle modes, background noise monitors in both R_X and T_X paths	Two point sensing with slow idle, background noise monitors in both R_X and T_X paths	Two point sensing with slow idle, background noise monitors in both R_X and T_X paths
No dial tone detector in receive path	Receive path has dial tone detector	Receive path has dial tone detector	Receive path has dial tone detector
Attenuator Characteristics: • Range: 44 dB • Tolerance: ±4.0 dB • Gain tracking not specified • White noise is constant	Attenuator Characteristics: • Range: 52 dB • Tolerance: ±2.0 dB • Gain Tracking: <1.0 dB • White noise reduces with volume	Attenuator Characteristics: • Range: 52 or 26 dB (selectable) • Tolerance: ±3.0 dB • Gain Tracking: <1.0 dB • White noise reduces with volume	Attenuator Characteristics: • Range: 52 dB • Tolerance: ±3.0 dB • Gain Tracking: <1.0 dB • White noise reduces with volume
External hybrid required	Hybrid amplifiers on board	External hybrid required	External hybrid required
Speaker amplifier is on board (34 dB, 100 mW)	External speaker amplifier required (MC34119)	External speaker amplifier required (MC34119)	External speaker amplifier required (MC34119)
Filtering is external	Configurable filter on board	Filtering is external	Filtering is external
Microphone amplifier has fixed gain and no muting	Microphone amplifier has adjustable gain and mute input	Microphone amplifier has adjustable gain, and can be muted through µP port	Microphone amplifier has adjustable gain and a mute input
Supply Voltage: 4.0 V to 11 V	Supply Voltage: 2.8 V to 6.5 V	Supply Voltage: 2.5 V to 6.5 V	Supply Voltage: 2.7 V to 6.5 V
Supply Current: 6.5 mA typ., 9.0 mA max	Supply Current: 5.5 mA typ., 8.0 mA max	Supply Current: 4.0 mA typ., 5.0 mA max	Supply Current: 3.0 mA typ., 5.0 mA max
Speaker amplifier reduces gain to prevent clipping	Receive gain is reduced as supply voltage falls to prevent clipping	Receive gain is reduced as supply voltage falls to prevent clipping	Receive gain is reduced as supply voltage falls to prevent clipping
Volume control is linear. Cannot override voice switched operation except through additional circuitry. Attenuator gain is fixed at 44 dB (slightly variable). No microphone mute.	Volume control is linear, and microphone mute has separate pin. Cannot override voice switched operation except through additional circuitry. Attenuator gain is fixed at 52 dB.	8–bit µP serial port controls: • Volume control (16 steps) • Microphone mute • Range selection (26 dB or 52 dB) • Force to transmit, idle, receive, or normal voice switched operation	Volume control is linear, and microphone mute has separate pin. Attenuator range fixed at 52 dB. Cannot override voice switched operation except through additional circuitry.
28 Pin DIP and SOIC packages	28 Pin DIP and SOIC packages	24 Pin narrow DIP and SOIC packages	24 Pin narrow DIP and SOIC packages
External Required: • 12 Resistors • 11 Capacitors (≤1.0 µF) • 8 Capacitors (>1.0 µF)	External Required: • 14 Resistors • 12 Capacitors (≤1.0 µF) • 9 Capacitors (>1.0 µF)	External Required: • 12 Resistors • 11 Capacitors (≤1.0 µF) • 4 Capacitors (>1.0 µF)	External Required: • 12 Resistors • 11 Capacitors (≤1.0 µF) • 4 Capacitors (>1.0 µF)
Temperature Range: –20° to +60°C	Temperature Range: –20° to +60°C	Temperature Range: –40° to +85°C	Temperature Range: –40° to +85°C

Telephone Accessory Circuits

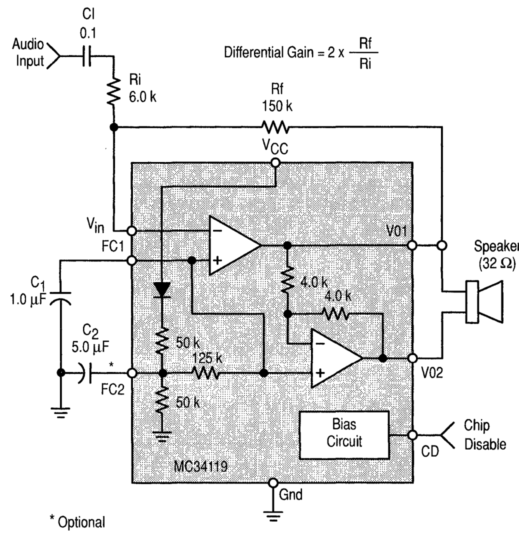
Audio Amplifier

MC34119P, D

T_A = 0° to +70°C, Case 626, 751

A low power audio amplifier circuit intended (primarily) for telephone applications, such as speakerphones. Provides differential speaker outputs to maximize output swing at low supply voltages (2.0 V min.). Coupling capacitors to the speaker, and snubbers, are not required. Overall gain is externally adjustable from 0 to 46 dB. A Chip Disable pin permits powering–down to mute the audio signal and reduce power consumption.

- Drives a Wide Range of Speaker Loads (16 to 100 Ω)
- Output Power Exceeds 250 mW with 32 Ω Speaker
- Low Distortion (THD = 0.4% Typical)
- Wide Operating Supply Voltage (2.0 V to 16 V) – Allows Telephone Line Powered Applications.
- Low Quiescent Supply Current (2.5 mA Typical)
- Low Power–Down Quiescent Current (60 µA Typical)



* Optional

Current Mode Switching Regulator

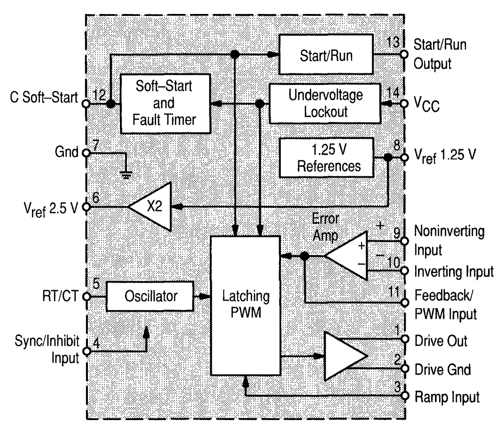
MC34129P, D

T_A = 0° to +70°C, Case 646, 751A

High performance current mode switching regulator for low–power digital telephones. Unique internal fault timer provides automatic restart for overload recovery. A start/run comparator is included to implement bootstrapped operation of V_{CC}.

Although primarily intended for digital telephone systems, these devices can be used cost effectively in many other applications. On–chip functions and features include:

- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–By–Cycle Current Limiting
- Latched–Off or Continuous Retry after Fault Timeout
- Soft–Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- Input Undervoltage Lockout



300 Baud FSK Modems

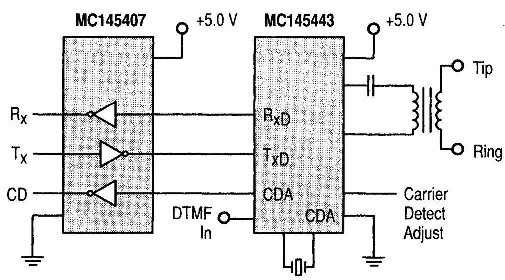
MC145442P, DW Modem – CCITT V.21
Case 738, 751D

MC145443P, DW Modem – Bell 103
Case 738, 751D

This powerful modem combines a complete FSK modulator/demodulator and an accompanying transmit/receive filter system on a single silicon chip. Designed for bidirectional transmission over the telephone network, the modem operates at 300 baud and can be obtained for compatibility with CCITT V.21 and Bell 103 specifications.

The modem contains an on–board carrier–detect circuit that allows direct operation on a telephone line (through a simple transformer), providing simplex, half–duplex, and full–duplex data communications. A built–in power amplifier is capable of driving –9.0 dBm onto a 600 Ω line in the transmit mode.

CMOS processing keeps power dissipation to a very low 45 mW, with a power–down dissipation of only 1.0 mW . . . from a single 5.0 V power supply. Available in a 20 pin dual–in–line P suffix, and a wide body surface mount DW suffix.



3.579545 MHz

MC145444H, DW – CCITT V.21
Case 804, 751D

MC145446AFW – CCITT V.21
Case 751M

This device includes the DTMF generator and call progress tone detector (CPTD) as well as the other circuitry needed for full–duplex, half–duplex, or simplex 300 baud data communication over a pair of telephone lines. It is intended for use with telemeter system or remote control system applications.

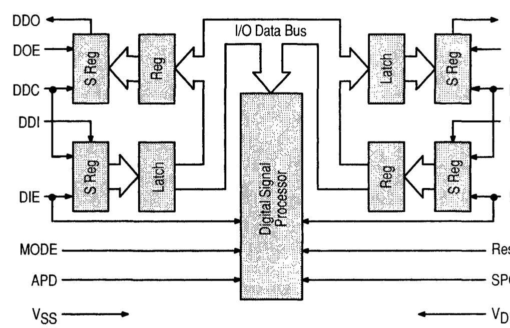
The differential line driver is capable of driving 0 dBm into a 600 Ω load. The transmit attenuator is programmable in 1.0 dB steps.

ADPCM Transcoder

MC145532DW, L
Case 751G, 620

The MC145532 Adaptive Differential Pulse Code Modulation (ADPCM) Transcoder provides a low cost, full–duplex, single–channel transcoder to (from) a 64 kbps PCM channel from (to) either a 16 kbps, 24 kbps, 32 kbps, or 64 kbps channel.

- Complies with CCITT Recommendation G.721 (1988)
- Complies with the American National Standard (T1.301–1987)
- Full–Duplex, Single–Channel Operation
- Mu–Law or A–Law Coding is Pin Selectable
- Synchronous or Asynchronous Operation
- Easily Interfaces with any Member of Motorola's PCM Codec–Filter Mono–Circuit Family or Other Industry Standard Codecs
- Serial PCM and ADPCM Data Transfer Rate from 64 kbps to 5.12 Mbps
- Power Down Capability for Low Cost Consumption
- The Reset State is Automatically Initiated when the Reset Pin is Released.
- Simple Time Slot Assignment Timing for Transcoder Applications
- Single 5.0 V Power Supply
- Evaluation Kit MC145536 EVK Supports the MC145532 as well as the MC145480 PCM Codec–Filter. (See PBX Architecture Pages for More Information.)



Calling Line Identification (CLID) Receiver with Ring Detector

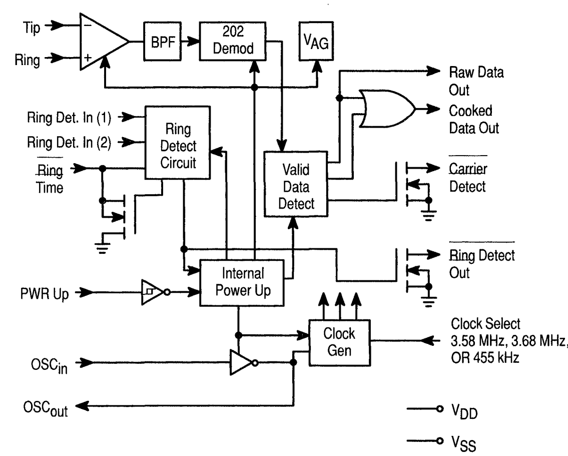
MC145447P, DW

Case 648, 751G

The MC145447 is designed to demodulate Bell 202 1200 baud FSK asynchronous data. Its primary application is in products that will be used to receive and display the calling number, or the message waiting indicator sent to subscribers from participating central office facilities of the public switched telephone network. The device also contains a carrier detect circuit and telephone ring detector which may be used to power up the device.

Applications include adjunct boxes, answering machines, feature phones, fax machines, and computer interface products.

- Ring Detector On–Chip
- Ring Detect Output for MCU Interrupt
- Power–Down Mode Less Than 1.0 μA
- Single Supply: 3.5 V to 6.0 V
- Pin Selectable Clock Frequencies: 3.68 MHz, 3.58 MHz, or 455 kHz
- Two–Stage Power–Up for Power Management Control

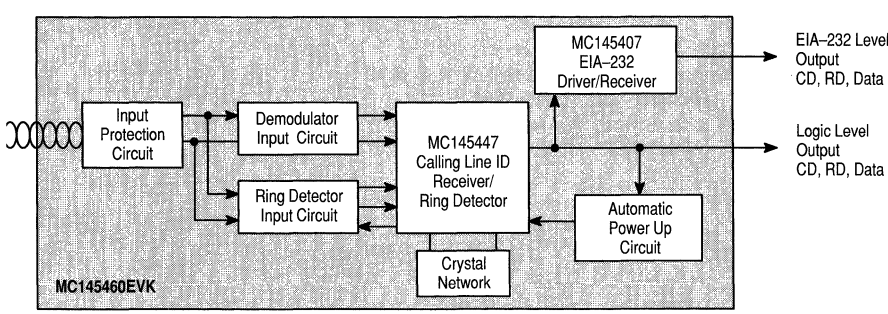


Calling Line ID Receiver Evaluation Kit

MC145460EVK

The MC145460EVK is a low cost evaluation platform for the MC145447. The MC145460EVK facilitates development and testing of products that support the Bellcore customer premises equipment (CPE) data interface, which enables services such as Calling Number Delivery (CND). The MC145447 can be easily incorporated into any telephone, FAX, PBX, key system, answering machine, CND adjunct box or other telephone equipment with the help of the MC145460EVK development kit.

- Easy Clip–On Access to Key MC145447 Signals
- Generous Prototype Area
- Configurable for MC145447 Automatic or External Power Up Control
- EIA–232 and Logic Level Ports for Connection to any PC or MCU Development Platform
- Carrier Detect, Ring Detect and Data Status LEDs
- Optional Tip and Ring Input Protection Network
- MC145460EVK User Guide, MC145447 Data Sheet, and Additional MC145447 Sample Included



Continuously Variable Slope Delta (CVSD) Modulator/Demodulator

MC34115P, DW
T_A = 0° to +70°C, Case 648, 751G

MC3418P, DW
T_A = 0° to +70°C, Case 648, 751G

Provides the A/D–D/A function of voice communications by digital transmission. Designed for speech synthesis and commercial telephone applications. A single IC provides both encoding and decoding.

- Encode and Decode Functions on the Same Chip with a Digital Input
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable (V_{CC}/2 reference provided on Chip)
- MC34115 Has a 3–Bit Algorithm (General Communications)
- MC3418 Has a 4–Bit Algorithm (Commercial Telephone)

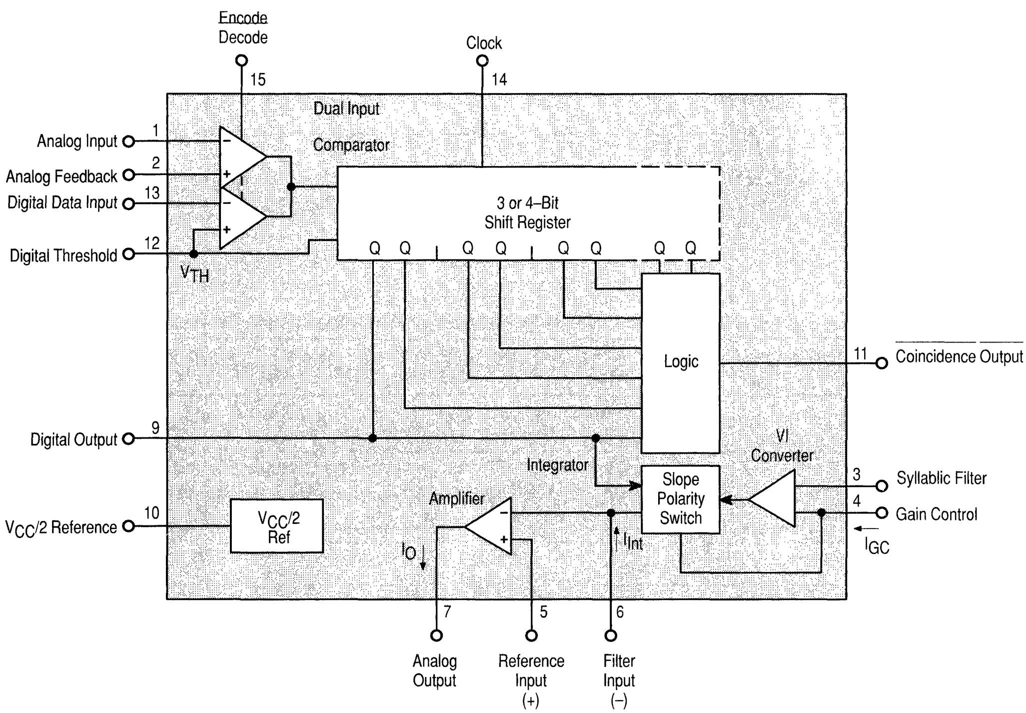


Table 10. Summary of Bipolar Telecommunication Circuits

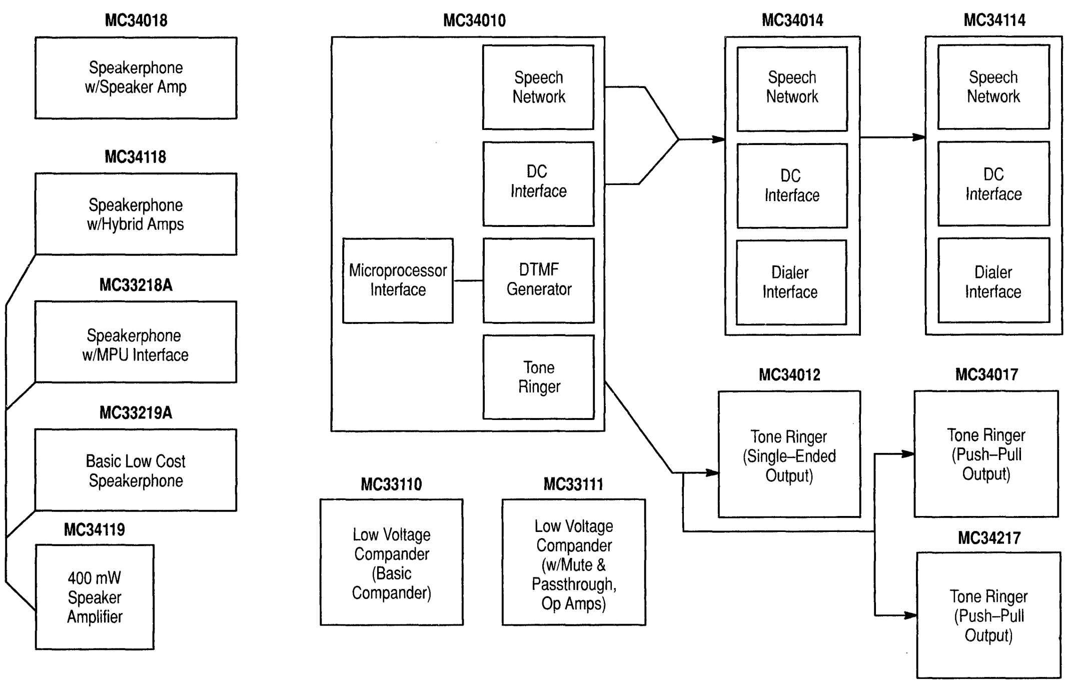
Function	Features	Suffix/ Package	Device
Subscriber Loop Interface Circuits (SLICs)			
PBX Applications	All gains externally programmable, most BORSHT functions, current limit adjustable to 100 mA.	L/726	MC3419–1
Central Office, Remote Terminals, PBX Applications	All gains externally programmable, most BORSHT functions, current limit adjustable to 50 mA, 58 dB Longitudinal Balance, –21.6 V to –42 V.	P/738, FN/776	MC33121
Central Office, Remote Terminals, PBX Applications	All gains externally programmable, most BORSHT functions, current limit adjustable to 50 mA, 58 dB Longitudinal Balance, –42 V to –58 V.	P/738, FN/776	MC33120
Complete Telephone Circuit			
POTS Circuit + MPU Dialing	Speech network, tone ringer, dc loop current interface, DTMF dialer with serial port control.	P/711, FN/777	MC34010
Tone Ringers			
Adjustable Tone Ringer	Single–ended output, meets FCC requirements, adjustable REN, different warble rates.	P/626, D/751	MC34012–1, 2, 3
Adjustable Tone Ringer	Differential output, meets FCC requirements, adjustable REN, different warble rates.	P/626, D/751	MC34017–1, 2, 3
Adjustable Tone Ringer	Differential output, meets FCC requirements, adjustable REN, single warble rates.	P/626, D/751	MC34217
Speech Networks			
Basic Phone Line Interface	Loop current interface, speech network, line length compensation, speech/dialing modes, Bell System compliant.	P/707, DW/751D	MC34014
Cordless Universal Telephone Interface	Designed for digital cordless phones, SPI interface, double sidetone network, low noise and distortion.	P/738, DW/751D	MC34016
Basic Phone Line Interface	Loop current interface, speech network, line length compensation, speech/dialing modes, Bell System and foreign countries.	P/707, DW/751D	MC34114
Programmable Telephone Line Interface Circuit with Loudspeaker Amplifier	Group listening–in, DTMF and tones generator, ring generator, country programmable, SPI interface.	DW/751F	MC34216
Telephone Line Interface	Country programmable, double sidetone network, provides strong supply point.	DP/738, FP/751D	TCA3388
Speakerphone Circuits			
Complete Speaker Phone with Speaker Amplifier	All level detection (2 pt.), attenuators, and switching controls, mike and speaker amp.	P/710, DW/751F	MC34018
Complete Speaker Phone with Hybrid, Filter	All level detection (4 pt.), attenuators, and switching controls, mike amp with mute, hybrid, and filter.	P/710, DW/751F	MC34118
Complete Speaker Phone with MPU Interface	All level detection, attenuators, and switching controls, mike amp, MPU interface for: volume control, mode selection, mike mute.	P/724, DW/751E	MC33218A
Basic Low Cost Speakerphone	All level detection, attenuators and switching controls, Mike amplifier with Mute, low voltage operation.	P/724, DW/751E	MC33219A
Audio Amplifiers			
1 Watt Audio Amp	1.0 W output power into 16 Ω, 35 V maximum.	D/751	MC13060
Low Voltage Audio Amp	400 mW, 8.0 to 100 Ω, 2.0 to 16 V, differential outputs, chip–disable input pin.	P/626, D/751	MC34119

Telephone Accessory Circuits (continued)

Summary of Bipolar Telecommunications Circuits (continued)

Function	Features	Suffix/ Package	Device
Companders			
Basic Compander	2.1 V to 7.0 V, no precision externals, 80 dB range, –40° to +85°C, independent compressor and expander.	P/646, D/751A	MC33110
Compander with Features	3.0 V to 7.0 V, no precision externals, 80 dB range, –40° to +85°C, independent compressor and expander, pass through and mute functions, two op amps.	P/648, D/751B	MC33111
Switching Regulator			
Current Mode Regulator	For phone line power applications, soft–start, current limiting, 2% accuracy.	P/646, D/751A	MC34129
Voice Encoder/Decoders			
Continuously Variable Slope Modulator/Demodulator (CVSD)	Telephone quality voice encoding/decoding, variable clock rate, 3–bit coding, for secure communications, voice storage/retrieval, answering machines, 0° to 70°C.	P/738, DW/751G	MC34115
	Same as above except 4–bit coding.	P/738, DW751G	MC3418

Figure 27. The Motorola Family of Handset Telecom Integrated Circuits



Phase–Locked Loop Components

Motorola offers a choice of phase–locked loop components ranging from complete functional frequency synthesizers for dedicated applications to a wide selection of general purpose PLL circuit elements. Technologies include CMOS for lowest power consumption and bipolar for high speed operation. Typical applications include TV, CATV, radios, scanners, cordless telephones plus home and personal computers.

Table 11. PLL Frequency Synthesizers

Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Phase Detector	Standby	Interface	Device	Suffix/ Case
4.0 @ 5.0 V	4.5 to 12	6.0 @ 5.0 V	Single–ended 3–state	No	Parallel	MC145106	P/707, DW/751D
15 @ 5.0 V	3.0 to 9.0	–	Two single–ended 3–state		Serial	MC145149*	P/738, DW/751D
		7.5 @ 5.0 V	Analog			MC145159–1	P/738, DW/751D
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5.0 V	Single–ended 3–state, double–ended		4–Bit	MC145145–2	P/707, DW/751D
						MC145146–2	P/738, DW/751D
					Parallel	MC145151–2	P/710, DW/751F
			Double–ended			MC145152–2	P/710, DW/751F
			Single–ended 3–state, double–ended		Serial	MC145155–2	P/707, DW/751D
						MC145156–2	P/707, DW/751D
						MC145157–2	P/648, DW/751G
						MC145158–2	P/648, DW/751G
60 @ 3.0 V	2.5 to 5.5	3.0 @ 3.0 V	Two single–ended 3–state	Yes		MC145162*	P/648, DW/751G
60 @ 2.0 V	1.8 to 3.6	1.5 @ 1.8 V				MC145165*	P/648, D/751B
60 @ 3.0 V	2.5 to 5.5	3.0 @ 3.0 V			Parallel	MC145166*	P/648, DW/751G
					Serial	MC145167*	P/648, DW/751G
					Parallel	MC145168*	
					Serial	MC145169*	
85 @ 3.0 V	2.5 to 5.5	3.0 @ 3.0 V				MC145162–1*	P/648, DW/751G
40/130 @ 5.0 V	4.5 to 5.5	9.0 @ 5.0 V	Single–ended 3–state, Current source/sink			MC145173	DW/751E
100 @ 3.0 V 185 @ 5.0 V	2.5 to 5.5	2.0 @ 3.0 V 6.0 @ 5.0 V		No		MC145170–1	P/648, D/751B

* Dual PLL

Phase–Locked Loop Components (continued)

PLL Frequency Synthesizers (continued)

Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Phase Detector	Standby	Interface	Device	Suffix/ Case
1100 @ 5.0 V	4.5 to 5.5	7.0 @ 5.0 V	Current source/sink, double–ended	Yes	Serial	MC145190	F/751J, DT/948D
						MC145191	F/751J, DT/948D
1100 @ 3.0 V	2.7 to 5.0	6.0 @ 2.7 V				MC145192	F/751J, DT/948D
1100 @ 3.0 V	2.7 to 5.5	12	Two current source/sink, double–ended			MC145220*	F/803C, DT/948D
2000 @ 5.0 V	4.5 to 5.5	12 @ 5.0 V	Current source/sink, double–ended			MC145200	F/751J, DT/948D
2000 @ 5.0 V	4.5 to 5.5	12 @ 5.0 V				MC145201	F/751J, DT/948D
2000 @ 3.0 V	2.7 to 5.5	4.0 @ 3.0 V				MC145202	F/751J, DT/948D

* Dual PLL

Table 12. Phase–Locked Loop Functions

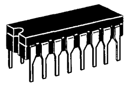
Device	Function	Pins	DIP	SM
MC4016	Programmable Modulo–N Counters (N=0–9)	16	P,L	
MC4018	Programmable Modulo–N Counters (N=0–9)	16	P,L	
MC4024	Dual Voltage–Controlled Multivibrator	14	P,L	
MC4044	Phase–Frequency Detector	14	P,L	D
MC4316	Programmable Modulo–N Counters (N=0–9)	16	P,L	
MC4324	Dual Voltage–Controlled Multivibrator	14	P,L	
MC4344	Phase–Frequency Detector	14	P,L	
MC12002	Analog Mixer	14	P,L	
MC12009	480 MHz ÷5/6 Dual Modulus Prescaler	16	P,L	
MC12011	550 MHz ÷8/9 Dual Modulus Prescaler	16	P,L	
MC12013	550 MHz ÷10/11 Dual Modulus Prescaler	16	P,L	
MC12014	Counter Control Logic	16	P,L	
MC12015	225 MHz ÷32/33 Dual Modulus Prescaler	8	P,L	D
MC12016	225 MHz ÷40/41 Dual Modulus Prescaler	8	P,L	D
MC12017	225 MHz ÷64/65 Dual Modulus Prescaler	8	P,L	D
MC12018	520 MHz ÷128/129 Dual Modulus Prescaler	8	P,L	D
MC12019	225 MHz ÷20/21 Dual Modulus Prescaler	8	P,L	D
MC12022A	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D
MC12022B	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D

Phase–Locked Loop Components (continued)

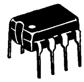
Phase–Locked Loop Functions (continued)

Device	Function	Pins	DIP	SM
MC12022LVA	1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12022LVB	1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12022SLA	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D
MC12022SLB	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D
MC12022TSA	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D
MC12022TSB	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D
MC12022TVA	1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12022TVB	1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12023	225 MHz ÷64 Prescaler	8	P	D
MC12025	520 MHz ÷64/65 Dual Modulus Prescaler	8	P	D
MC12026A	1.1 GHz ÷8/9, ÷16/17 Dual Modulus Prescaler	8	P	D
MC12026B	1.1 GHz ÷8/9, ÷16/17 Dual Modulus Prescaler	8	P	D
MC12028A	1.1 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12028B	1.1 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12031A	2.0 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12031B	2.0 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12032A	2.0 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D
MC12032B	2.0 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D
MC12033A	2.0 GHz ÷32/33, ÷64/65 Low Voltage Dual Modulus Prescaler	8	P	D
MC12033B	2.0 GHz ÷32/33, ÷64/65 Low Voltage Dual Modulus Prescaler	8	P	D
MC12034A	2.0 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12034B	2.0 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12036A	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler with Stand–By Mode	8	P	D
MC12036B	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler with Stand–By Mode	8	P	D
MC12040	Phase–Frequency Detector	14	P,L	FN
MC12061	Crystal Oscillator	16	P,L	
MC12073	1.1 GHz ÷64 Prescaler	8	P	D
MC12074	1.1 GHz ÷256 Prescaler	8	P	D
MC12076	1.3 GHz ÷256 Prescaler	8	P	D
MC12078	1.3 GHz ÷256 Prescaler	8	P	D
MC12079	2.8 GHz ÷64/128/256 Prescaler	8	P	D
MC12080	1.1 GHz ÷10/20/40/80 Prescaler	8	P	D
MC12083	1.1 GHz ÷2 Low Power Prescaler with Stand–By Mode	8	P	D
MC12089	2.8 GHz ÷64/128/256 Low Power Prescaler	8	P	D
MC12090	750 MHz ÷2 UHF Prescaler	16	P,L	
MC12100	200 MHz Voltage Controlled Multivibrator	20	P	FN
MC12101	130 MHz Voltage Controlled Multivibrator	20	P	FN
MCH12140	Phase–Frequency Detector	8		D
MCK12140	Phase–Frequency Detector	8		D
MC12148	Low Power Voltage Controlled Oscillator	8		D,SD

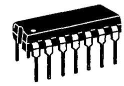
Communications Circuits Package Overview



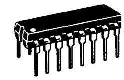
CASE 620
L SUFFIX



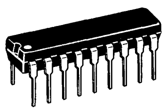
CASE 626
P SUFFIX



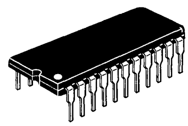
CASE 646
P SUFFIX



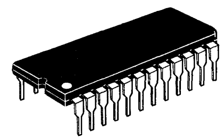
CASE 648
P SUFFIX



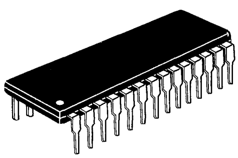
CASE 707
P SUFFIX



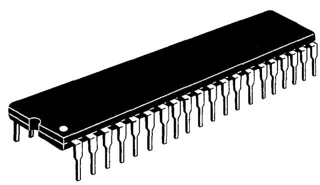
CASE 708
P SUFFIX



CASE 709
P SUFFIX



CASE 710
P SUFFIX



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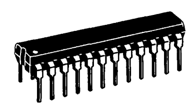
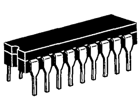
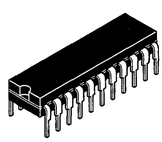
P SUFFIX



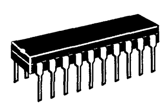
CASE 724
P SUFFIX



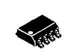
CASE 726
L SUFFIX



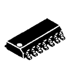
CASE 736B
PB SUFFIX



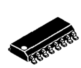
CASE 738
DP, P SUFFIX



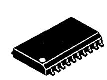
CASE 751
D SUFFIX



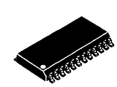
CASE 751A
D SUFFIX



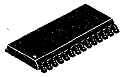
CASE 751B
D SUFFIX



CASE 751D
DW, FP SUFFIX



CASE 751E
DW SUFFIX



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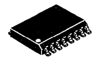
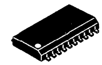
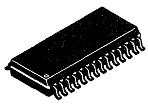
DW SUFFIX



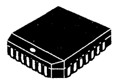
CASE 751G
DW SUFFIX



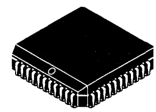
CASE 751J
F SUFFIX



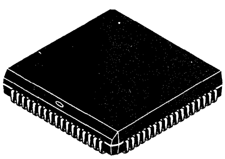
CASE 751M
FW SUFFIX



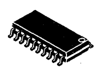
CASE 776
FN SUFFIX



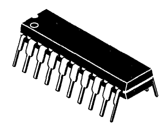
CASE 777
FN SUFFIX



CASE 779
FN SUFFIX

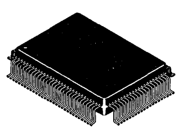


CASE 803C
F SUFFIX

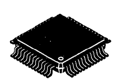


CASE 804
H SUFFIX

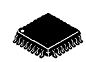
CASE 837A
DW SUFFIX



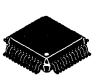
CASE 842D
PB SUFFIX



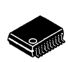
CASE 848B
FB SUFFIX



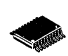
CASE 873
FB, FTB, FU SUFFIX



CASE 932
FTA SUFFIX



CASE 940C
SD SUFFIX



CASE 948D
DT SUFFIX

CASE 977
FTA SUFFIX

Consumer Electronic Circuits

In Brief . . .

These integrated circuits reflect Motorola's continuing commitment to semiconductor products necessary for consumer system designs. This tabulation is arranged to simplify selection of consumer integrated circuit devices that satisfy the primary functions for home entertainment products, including television, hi–fi audio and AM/FM radio.

Page

Entertainment Radio Receiver Circuits

Table 1. Entertainment Receiver RF/IF

Function	Features	Suffix/ Package	Device
E.T.R. Front End	Mixer/VCO/AGC for Electronically Tuned AM Stereo Receivers	P/648, D/751B	MC13025
AMAX Front End	Mixer/VCO/AGC with RF and Audio Noise Blanking	DW/751D	MC13027
Dual Conversion AM Receiver	1st Mixer/OSC, 2nd Mixer/OSC, High Gain IF, AGC, Detector	DW/751F	MC13030

Table 2. C–Quam® AM Stereo Decoders

Function	Features	Suffix/ Package	Device
Basic AM Stereo Decoder	Monaural/Stereo AM Detector/Indicator, 6.0 to 10 V Operation	P/738	MC13020
Advanced AM Stereo Decoder	Medium Voltage 6.0 to 10 V, Decoder and IF Amp	P/710, DW/751F	MC13022A
Low V AM Stereo Receiver	IF/Decoder for Advanced C–Quam Receivers	P/648, D/751B	MC13028A
Medium V AM Stereo Decoder	IF/Decoder for Advanced C–Quam Receivers with AM/FM Switch	DW/751D, H/738	MC13029A
AM/FM Stereo Decoder	AM Stereo Tuner IC with FM Stereo Decoder	DW/751D	MC13035
AM/FM Stereo Decoder	AM and FM Stereo Decoder, 4.0 to 12 V Operation	P/648	MC13037
AMAX Stereo Decoder	Am Stereo Decoder with Audio Noise Blanker	DW/751F	MC13122

Table 3. Audio Amplifiers

Function	P_O (Watts)	V_{CC} Vdc Max	V_{in} @ Rated P_O mV Typ	I_D mA Typ	R_L (Ohms)	Suffix/ Package	Device
Mini Watt SOIC Audio Amp	1.0 W	35	80	11	16	D/751	MC13060
Low Power Audio Amp	500 mW	16	–	2.5 mA	8 – ∞	D/751, P/626	MC34119

Video Circuits

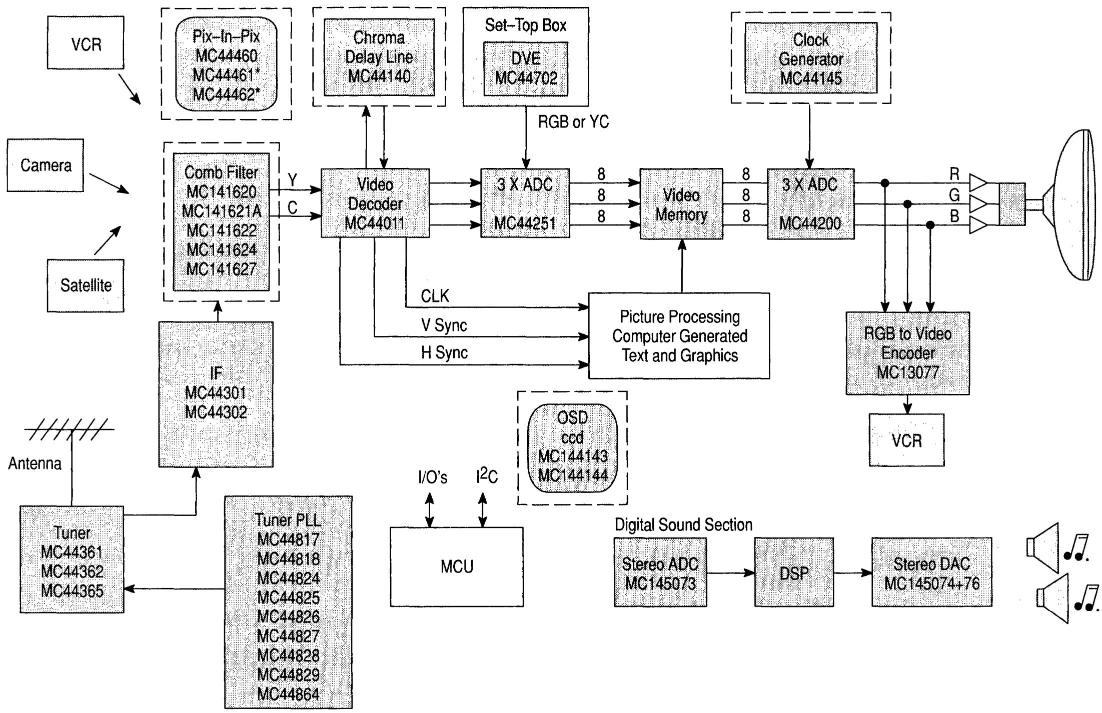
Table 4. Video Circuits

Function	Features	Suffix/ Package	Device
Encoders			
RGB to PAL/NTSC Encoder	RGB and Sync inputs, Composite Video out; PAL/NTSC selectable.	P/738, DW/751D	MC1377
Video Overlay Synchronizer	Complete Color TV Video Overlay Synchronizer, remote or local system control and RGB encoder.	P/711, FN/777	MC1378
Advanced RGB to PAL/NTSC Encoder	RGB and Sync inputs, Composite Video and S–VHS out; PAL/NTSC selectable; subcarrier from crystal or external source.	P/738, DW/751D	MC13077
TV Decoder			
Chroma 4 Multistandard Decoder (TV set)	PAL/NTSC/S–VHS input, RGB outputs; horizontal and vertical timing outputs; all digital internal filters, no external tank; μP and crystal controlled.	P/711	MC44002
Video Capture Chip Sets			
Chroma 4 Multistandard Video Processor (Multimedia)	PAL/NTSC/S–VHS input, RGB/YUV outputs; horizontal and vertical timing outputs; all digital internal filters, no external tanks; μP and crystal controlled.	FN/777, FB/824E	MC44011
PAL Digital Delay Line	For PAL applications of the MC44011 and MC44001.	P/648, DW/751G	MC44140
Pixel Clock PLL/Sync Sep.	PAL/NTSC sync separator, 6.0–40 MHz pixel clock PLL.	D/751A	MC44145
Triple 8–Bit Video DAC	TTL inputs, 75 Ω drive outputs.	FB/824A	MC44200
Triple 8–Bit Video A/D	Video clamps for RGB/YUV, 18 MHz, High Z TTL outputs.	FN/777	MC44251
TV Picture–in–Picture			
Picture–in–Picture (PIP) Controller	Complete PIP function on one chip: two NTSC composite inputs (reversible); encoder, decoder, logic, memory, video amplifier. Uses I^2C bus control to select 1/16 or 1/9 PIP size, contrast and color parameters.	B/859	MC44460
Comb Filters			
Enhanced Comb Filter	Fast 8–Bit A/D Converter, Two 8–Bit D/A Converters, Two Line–Delay Memories, utilizes NTSC Subcarrier Frequency clock, CMOS Technology.	FU/898	MC141620
Advanced Comb Filter (ACF)	Composite Video input; YC outputs in digital and analog form; all digital internal filters.	FU/898	MC141621A
Advanced Comb Filter – II (ACF–II)	Composite Video input; YC outputs in digital and analog form; all digital internal filters; vertical enhancer circuit.	P/898	MC141622
Advanced Comb Filter – I (ACF–I)	Low cost Ih filter.	FU/873 SP/TBD	MC141624
Advanced PAL/NTSC Comb Filter	Composite Video input; YC outputs in digital and analog form; all digital internal filters.	FB/898	MC141627
Deflection			
Horizontal Processor	Linear balanced phase detector, oscillator and predriver, adjustable DC loop gain and duty cycle.	P/626	MC1391
TV IF Circuits			
Advanced Video IF	Complete video IF system for high performance analog TV receivers.	P/724, DW/751F	MC44301
Advanced Multi–Standard TV Video/Sound IF	Complete video/sound IF system for all standard modulation techniques including NTSC, PAL, SECAM and AM D2MAC.	P/710, DW/751F	MC44302
IF Amplifier	1st and 2nd video IF amplifiers, 50 dB gain at 45 MHz, 60 dB AGC range.	D/751, P/626	MC1350

Table 4. Video Circuits (continued)

Function	Features	Suffix/ Package	Device
Tuner PLL Circuits			
PLL Tuning Circuits	1.3 GHz, 10 mV sensitivity selectable prescaler (MC44817), op amp, 4 band buffers, 3–wire bus interface, lock detect.	D/751B	MC44817, B
	1.3 GHz, 10 mV sensitivity prescaler, op amp, 4 band buffers, I^2C interface, lock detect.	D/751B	MC44818
	1.3 GHz, 10 mV sensitivity prescaler, 3 band buffers, I^2C interface, replacement for Siemens MPG3002.	D/751, D/751B	MC44824, MC44825
	Similar to MC44817, with lower power consumption, push–pull lock detector output, no divide–by–8 bypass, in a TSSOP package.	DTB/948F	MC44827
	Similar to MC44818, with lower power consumption, push–pull lock detector output, in a TSSOP package.	DTB/948F	MC44828
	1.3 GHz prescaler, 10 mV sensitivity 50 to 950 MHz, op amp, 3 band buffers, Mixer/Osc Decoder and I^2C Bus.	D/751A	MC44829
	1.3 GHz, 10 mV sensitivity selectable prescaler, op amp, 4 band buffers, I^2C interface, 3 DACs for automatic tuner alignment.	DW/751D	MC44864
Modulator			
Color TV Modulator with Sound	RF oscillator/modulator, and FM sound oscillator/modulator.	P/646	MC1374
Video Data Converters			
Single Channel A/D	8–Bit, 25 MHz, 2.0 V input range, ±5.0 V supplies, TTL output, no pipeline delay.	P/709, DW/751E	MC10319
Triple 8–Bit Video A/D	Video clamps for RGB/YUV, 18 MHz conversion, high Z outputs.	FN/777	MC44251
Triple 8–Bit Video DAC	TTL inputs, 75 Ω drive outputs.	FB/824	MC44200
Monitor Subsystem			
Multimode Color Monitor Processor	Triple video amplifiers, horizontal PLLs and deflection timing, vertical ramp generator.	B/859	MC13081X
Sound			
Sound IF Detector	Interchangeable with ULN2111A.	P/646, D/751A	MC1357
Miscellaneous			
Subcarrier Reference Generator	Provides continuous subcarrier sine wave and 4x subcarrier, locked to incoming burst.	P/626, D/751	MC44144
Closed Caption Decoder	Conforms to FCC, NTSC standards, underline and italics control.	P/707	MC144143
Enhanced Closed Caption Decoder	Conforms to FCC, NTSC, XDS standards, underline, italics and OSC.	P/707	MC144144
Sync Separator/Pixel Clock PLL	PAL/NTSC sync separator with vertical and composite sync output, 6 to 40 MHz pixel clock PLL.	D/751	MC44145
Dual Video Amplifiers	Gain @ 4.43 MHz = 6.0 dB ±1.0 dB, fixed gain, internally compensated, CMOS Technology.	P/626, F/904	MC14576C
	Gain @ 5.0 MHz = 10 dB max, 10 MHz = 6.0 dB max, adjustable gain, internally compensated, CMOS Technology.	P/626, F/904	MC14577C
Transistor Array	One differential pair and 3 isolated transistors, 15 V, 50 mA.	P/646, D/751A	MC3346
General Purpose Transistor Array	One differential pair and 3 isolated transistors, 130 V, 50 mA.	D/751A	CA3146

Video Capture Block Diagram



* In Development

Digitally Controlled Video Processor for Multimedia Applications

MC44011FN, FB

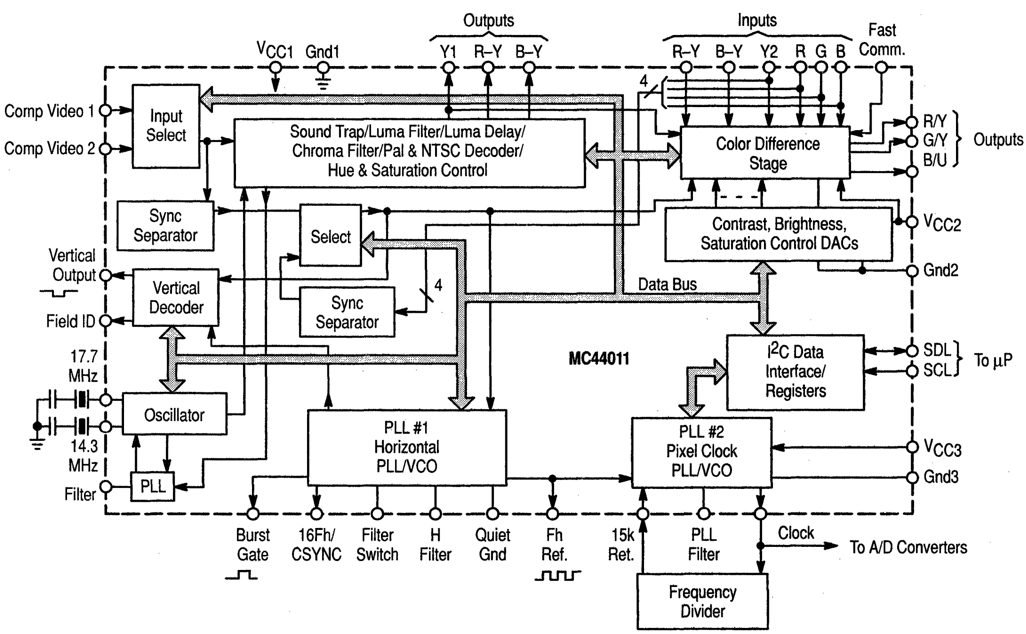
Case 777, 824E

The MC44011, a member of the MC44000 Chroma 4 family, is designed to provide RGB or YUV outputs from a variety of inputs. The inputs may be either PAL or NTSC composite video (two inputs), S–VHS, RGB, and color difference (R–Y, B–Y).

The MC44011 provides a sampling clock output for use by a subsequent analog to digital converter. The sampling clock (6.0 to 40 MHz) is phase–locked to the horizontal frequency. Additional outputs include composite sync, vertical sync, field identification, luminance, burst gate, and horizontal frequency.

Control of the MC44011, and reading of status flags is accomplished via an I^{2}C bus.

- Multistandard Decoder, Accepts NTSC and PAL Composite Video
- Dual Composite Video or S–VHS Inputs
- All Chroma and Luma Channel Filtering, and Luma Delay Line are Integrated Using Sampled Data Filters Requiring no External components
- Digitally Controlled via I^{2}C Bus
- Auxiliary Y, R–Y, B–Y Inputs
- Switched RGB Inputs with Separate Saturation Control
- Line–Locked Sampling Clock for Digitizing Video Signals
- Burst Gate Pulse Output for External Clamping
- Vertical Sync and Field Ident Outputs
- Software Selectable YUV or RGB Outputs Able to Drive A/D Converters



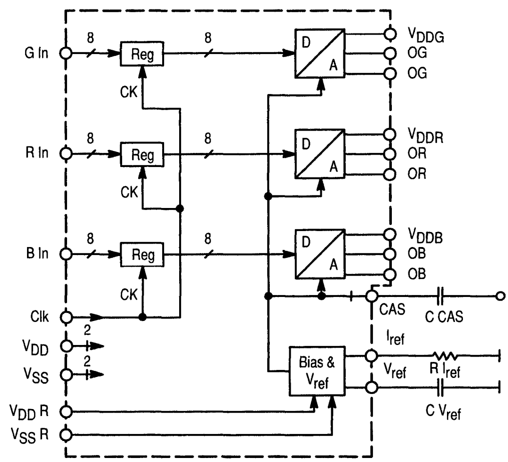
Triple 8–Bit D/A Converter

MC44200FB

Case 824A

The MC44200 is a monolithic digital to analog converter for three independent channels fabricated in CMOS technology. The part is specifically designed for video applications. Differential outputs are provided, allowing for a large output voltage range.

- 8–Bit Resolution
- Differential Outputs
- 55 msps Conversion Speed
- Large Output Voltage Range
- Low Current Mode
- Single 5.0 V Power Supply
- TTL Compatible Inputs
- Integrated Reference Voltage



Triple 8–Bit A/D Converter

MC44251FN

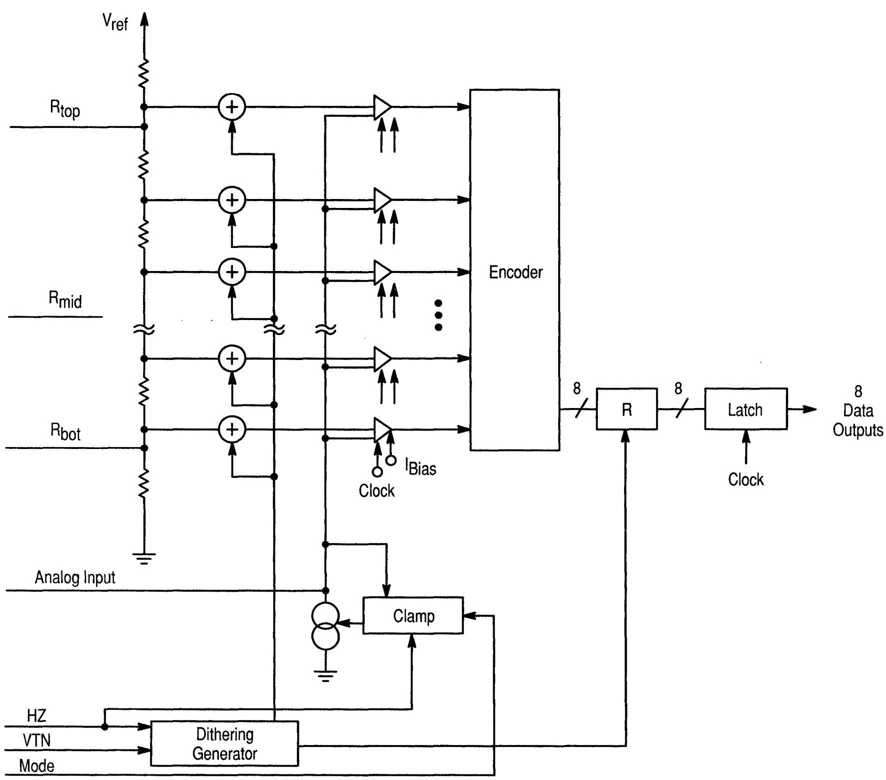
Case 777

The MC44251 contains three independent parallel analog to digital converters. Each ADC consists of 256 latching comparators and an encoder. Input clamps allow for AC coupling of the input signals, and dc coupling is also allowed. For video processing performance enhancements, a dither generator with subsequent digital correction is provided to each ADC. The outputs of the MC44251 can be set to a high impedance state.

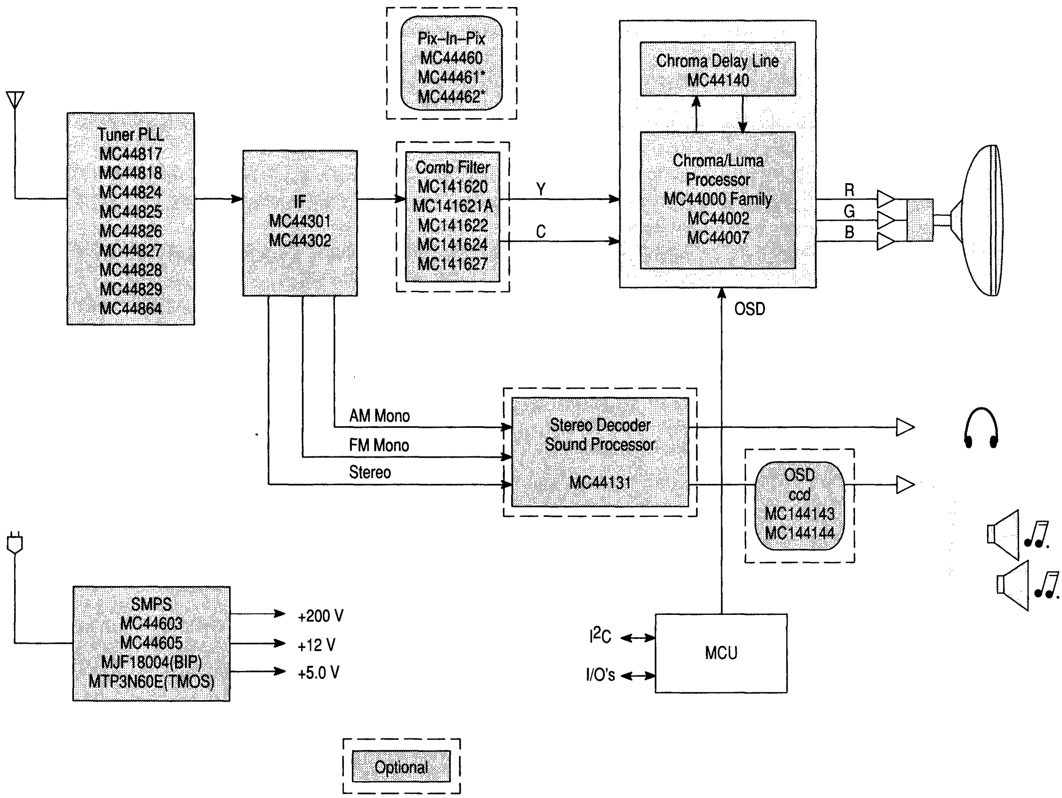
These A/Ds are especially suitable as front end converters in TV picture processing.

- 18 MHz Maximum Conversion Speed (MC44251)
- Input Clamps Suitable for RGB and YUV Applications
- Built–in Dither Generator with Subsequent Digital Correction
- Single 5.0 V Power Supply

Simplified Diagram of One of the ADCs



Color TV Block Diagram



* In Development

Advanced Multistandard TV Video/Sound IF

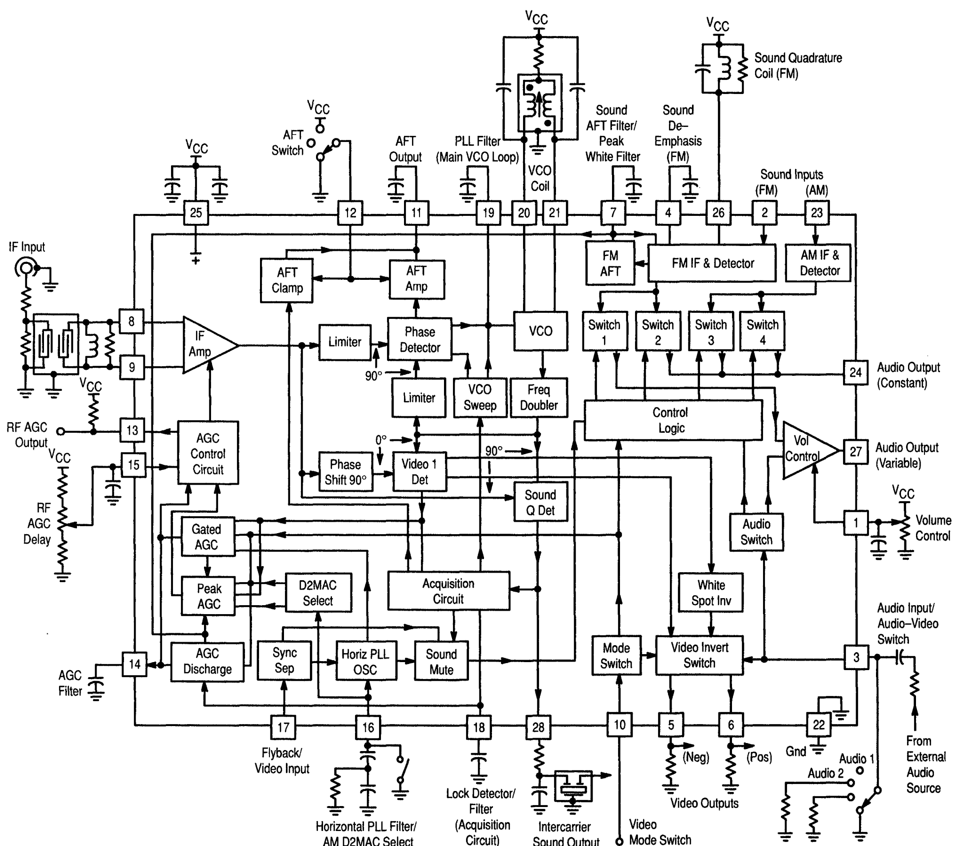
MC44302P, DW

Case 710, 751F

The MC44302 is a multistandard single channel TV Video/Sound IF and PLL detector system specifically designed for use with all standard modulation techniques including NTSC, PAL, SECAM, and AM D2MAC. This device enables the designer to produce a high quality IF system with a minimum number of external components.

The MC44302 contains a high gain video IF with an AGC range of 80 dB, enhanced phase locked loop carrier regenerator for low static phase error, doubly balanced full wave synchronous video demodulator featuring wide bandwidth positive and negative video outputs with extremely low differential gain and phase distortion, video AFT amplifier, multistage sound IF limiter with FM quadrature detector and AFT for self tuning, AM sound detector, constant and variable audio outputs, dc volume control for reduced hum and noise pickup, unique signal acquisition circuit that prevents false PLL lockup and AFT push out, sound mute, horizontal gating system with sync separator and phase locked loop circuitry for self–contained RF/IF AGC operation, RF AGC delay circuitry, and programmable control logic that allows operation in NTSC, PAL SECAM and AM D2MAC systems. This device is available in wide body 28 pin dual–in–line and surface mount plastic packages.

- Multi–Standard Detector System for NTSC, PAL, SECAM, and AM D2MAC
- High Gain Video IF Amplifier with 80 dB AGC Range
- Enhanced PLL Carrier Regenerator for Low Static Phase Error
- Synchronous Video Demodulator with Positive and Negative Video Outputs
- Sound IF with Self Tuning FM Quadrature Detector
- AM Sound Detector
- DC Volume Control
- Unique Signal Acquisition Circuit Prevents False PLL Lockup
- Horizontal Gating System for Self Contained RF/IF AGC Operation
- RF AGC Delay Circuitry



Picture–in–Picture (PIP) Controller

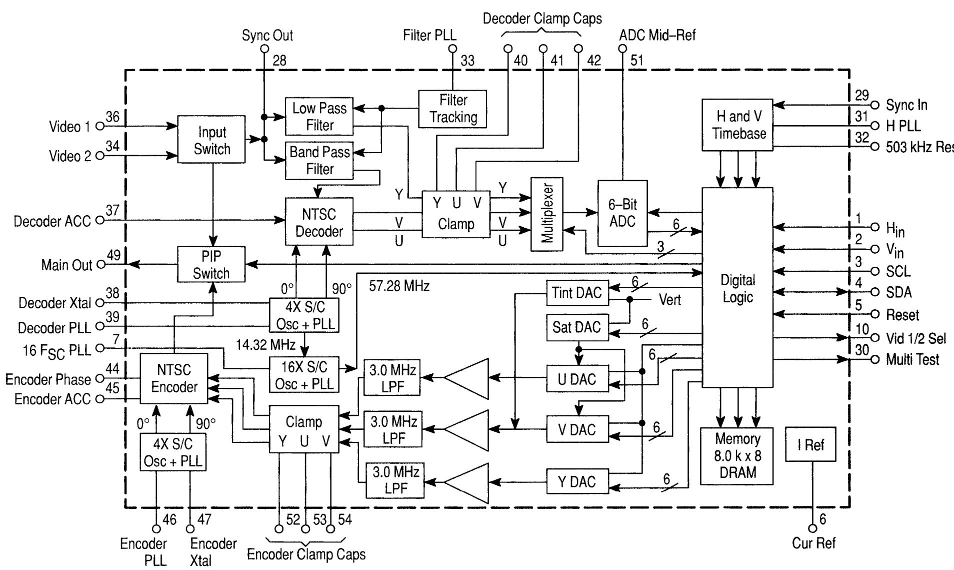
MC44460B

Case 859

The MC44460 Picture–in–Picture (PIP) controller is a low cost member of a family of high performance PIP controllers and video signal processors for television. It is NTSC compatible and contains all the analog signal processing, control logic and memory necessary to provide for the overlay of a small picture from a second non synchronized source onto the main picture of a television. All control and setup of the MC44460 is via a standard two pin I^2C bus interface. The device is fabricated using BICMOS technology. It is available in a 56–pin shrink dip (SDIP) package.

The main features of the MC44460 are:

- Two NTSC CVBS Inputs
- Switchable Main and PIP Video Signals
- Single NTSC CVBS Output Allows Simple TV Chassis Integration
- Two PIP Sizes; 1/16 and 1/9 Screen Area
- Freeze Field Feature
- Variable PIP Position in 64–X by 64–Y Steps
- PIP Border with Programmable Color
- Programmable PIP Tint and Saturation Control
- Automatic Main to PIP Contrast Balance
- Vertical Filter
- Integrated 64 k Bit DRAM Memory Resulting in Minimal RFI
- Minimal RFI Allows Simple Low Cost Application into TV
- I^2C Bus Control – No External Variable Adjustments Needed
- Operates from a Single 5.0 V Supply
- Economical 56–Pin Shrink DIP Package



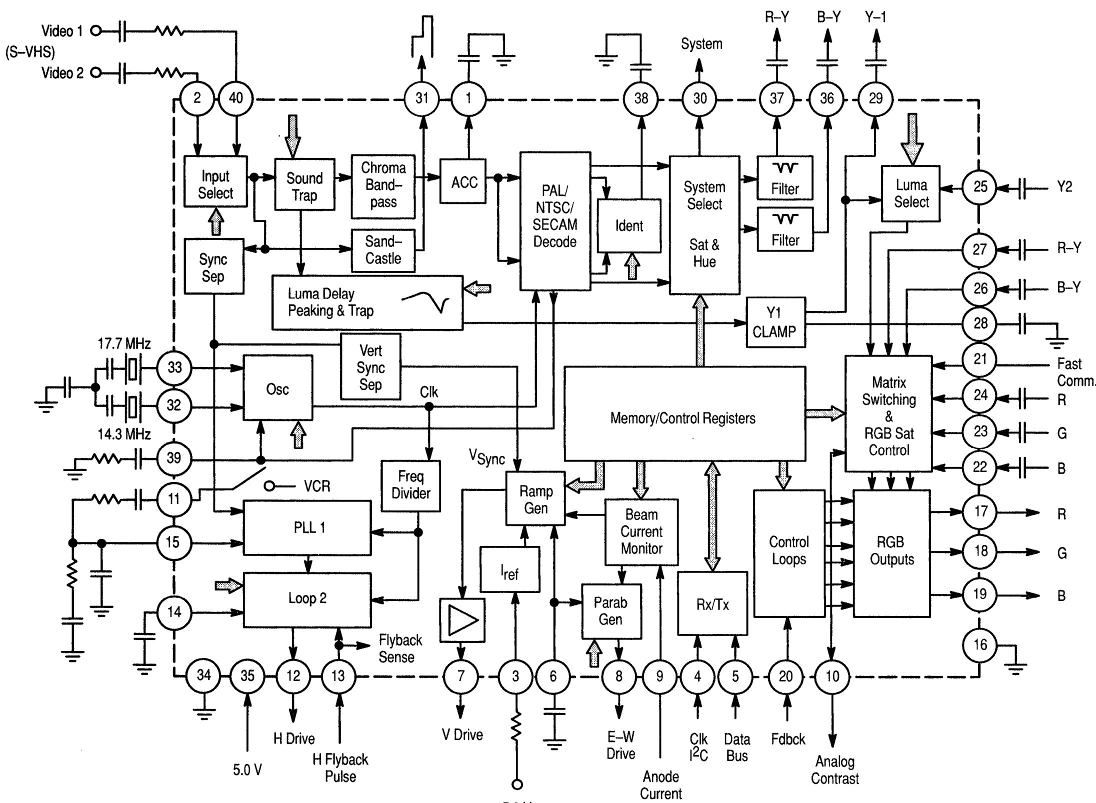
Multistandard Video/Timebase Processor

MC44002P

Case 711

The MC44002 is a highly advanced circuit which performs most of the basic functions required for a color TV. All of its advanced features are under processor control via an I^2C bus, enabling potentiometer controls to be removed completely. In this way the component count may be reduced dramatically to allow significant cost savings and the possibility of implementing sophisticated automatic test routines. Using the MC44002, TV manufacturers will be able to build a standard chassis for anywhere in the world.

- Operation from a Single 5.0 V Supply; Typical Current Consumption Only 120 mA
- Full PAL/SECAM/NTSC Capability
- Dual Composite Video or S–VHS Inputs
- All Chroma/Luma Channel Filtering, and Luma Delay Line are Integrated Using Sampled Data Filters Requiring No External Components
- Filters Automatically Commutate with Change of Standard
- Chroma Delay Line is Realized with Companion Device (MC44140)
- RGB Drives Incorporate Contrast and Brightness Controls and Auto Gray Scale
- Switched RGB Inputs with Saturation Control
- Auxiliary Y, R–Y, B–Y Inputs
- Line Timebase Featuring H–Phase Control and Switchable Phase Detector Gain and Time Constant
- Vertical Timebase Incorporating the Vertical Geometry Corrections
- E–W Parabola Drive Incorporating the Horizontal Geometry Corrections
- Beam Current Monitor with Breathing Compensation
- 16:9 Display Mode Capability

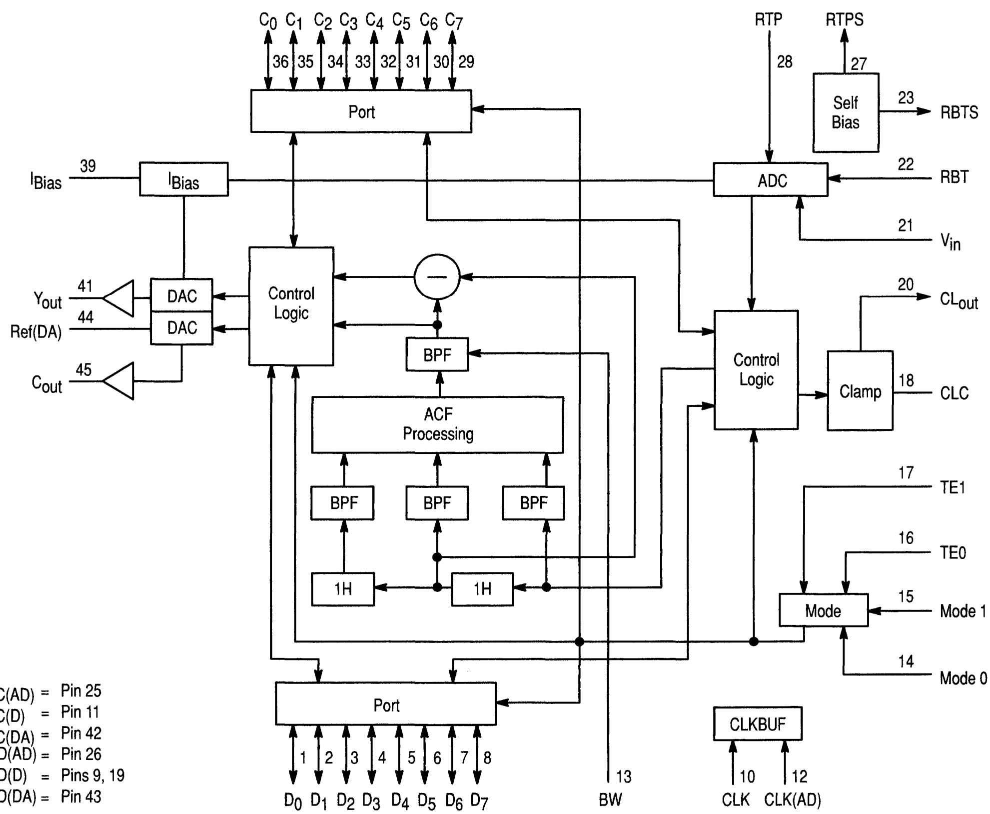


Advanced NTSC Comb Filter

MC141621FB
Case 898

The MC141621 is an advanced NTSC comb filter for VCR and TV applications. It separates the luminance (Y) and chrominance (C) signals from the NTSC composite video signal by using digital signal processing techniques. This filter allows a video signal input of an extended frequency bandwidth by using a 4.0 F_{SC} clock. In addition, the filter minimizes dot crawl and cross color effects. The built-in A/D and D/A converters allow easy connections to analog video circuits.

- Built–in High Speed 8–Bit A/D Converter
- Two Line Memories (1820 Bytes)
- Advanced Combing Process
- Two 8–Bit D/A Converters
- Built–in Clamp Circuit
- On–Chip Reference Voltage Regulator for ADC
- Digital Interface Mode



$V_{CC(AD)}$	=	Pin 25
$V_{CC(D)}$	=	Pin 11
$V_{CC(DA)}$	=	Pin 42
GND(AD)	=	Pin 26
GND(D)	=	Pins 9, 19
GND(DA)	=	Pin 43

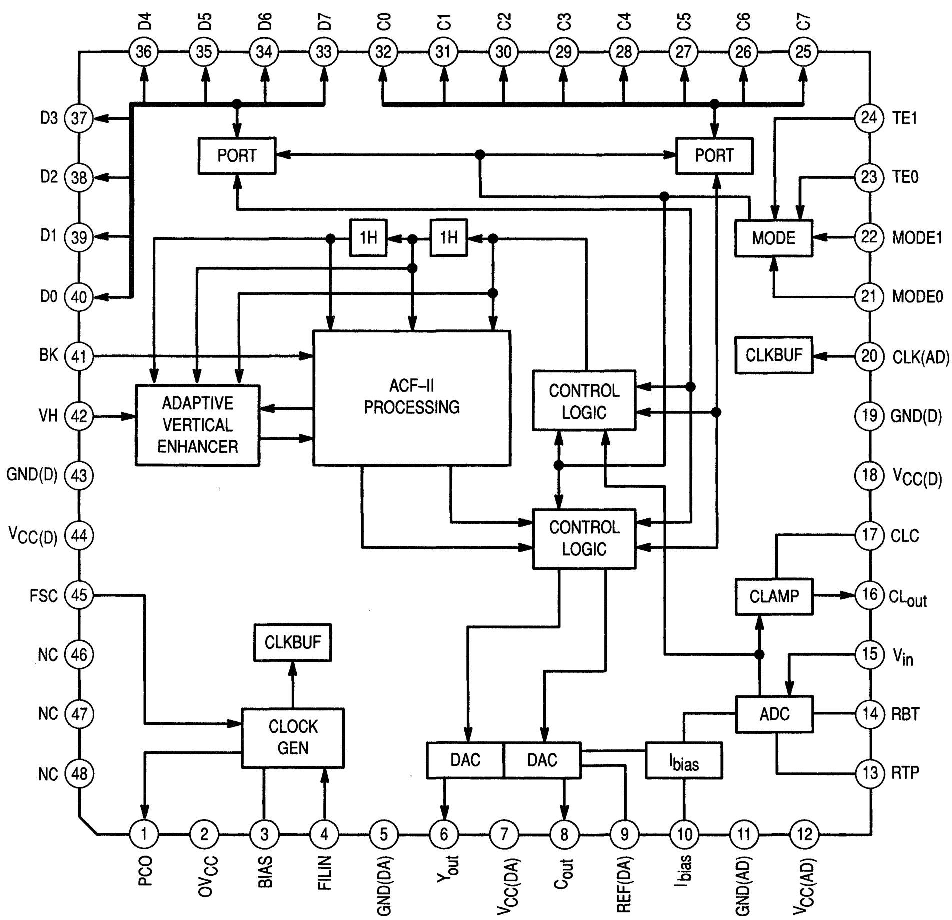
Advanced Comb Filter–II (ACF–II)

MC141622FU

Case 898

The Advanced Comb Filter–II is a video signal processor for VCRs and TVs. It's function is to separate the Luminance Y and Chrominance C signals from the NTSC composite video signal. The ACF–II minimizes dot–crawl and cross–color. A built–in PLL provides a 4xfsc clock from either an NTSC subcarrier signal or a 4xfsc input. This allows a video signal input of an extended frequency bandwidth. The built–in vertical enhancer circuit improves the quality of the Luminance Y signal. The built–in A/D and D/A converters allow easy connection to analog video circuits.

- Built–in High Speed 8–Bit A/D Converter
- Two Line Memories (1820 Bytes)
- Advanced Comb–II Process
- Vertical Enhancer Circuit
- Two High Speed 8–Bit D/A Converters
- 4xfsc PLL Circuit
- Built–in Clamp Circuit
- Digital Interface Mode
- On–Chip Reference Voltage Regulator for A/D Converter

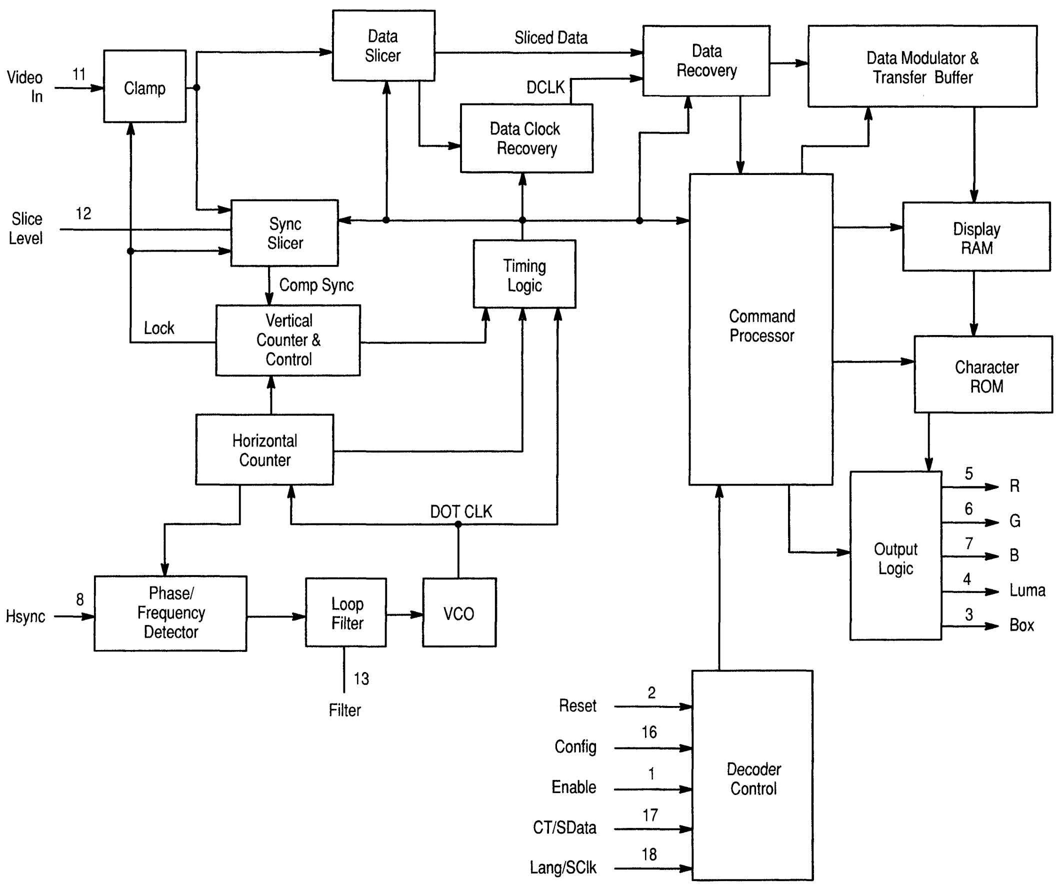


Closed–Caption Decoder

MC144143P
Case 707

The MC144143 is a Line 21 closed–caption decoder for use in television receivers or set top decoders conforming to the NTSC broadcast standard. Capability for processing and displaying all of the latest standard Line 21 closed–caption format transmissions is included. The device requires a closed–caption encoded composite video signal, a horizontal sync signal, and an external keyer to produce captioned video. RGB outputs are provided, along with a luminance and a box signal, allowing simple interface to both color and black and white receivers.

- Conforms to the FCC Report and Order as Amended by the Petition for Reconsideration on Gen. Doc. 91–1
- Supports Four Different Data Channels, Time Multiplexed within the Line 21 Data Stream: Captions Utilizing Languages 1 & 2, Plus Text Utilizing Languages 1 & 2
- Output Logic Provides Hardware Underline Control and Italics Slant Generation
- Single Supply Operating Voltage Range: 4.75 to 5.25 V
- Composite Video Input Range: 0.7 to 1.4 V_{pp}
- Horizontal Sync Input Polarity can be either Positive or Negative
- Internal Timing/Sync Signals Derived from On–Chip VCO



Enhanced Closed–Caption Decoder

MC144144P
Case 707

The MC144144 is a Line 21 closed–caption decoder for use in television receivers or set–top decoders conforming to the NTSC standard. Capability for processing and displaying all of the latest standard Line 21 closed–caption format transmissions is included. The device requires a closed–caption encoded composite video signal, a horizontal sync signal, and an external keyer to produce captioned video. RGB and box signal outputs are provided, which along with the mode select, allow simple interfacing to either color or black–and–white TV receivers.

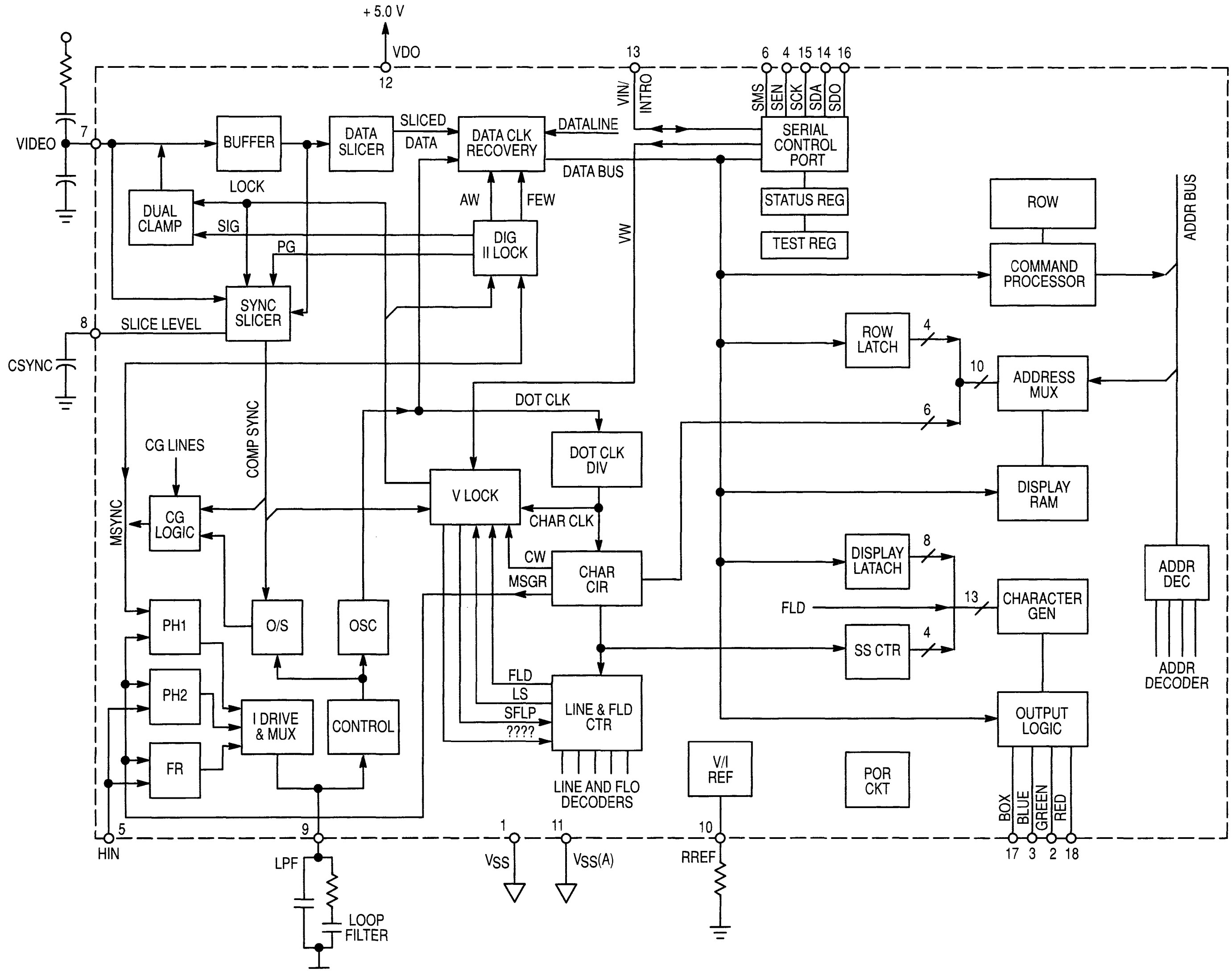
Display storage is accomplished with an on–chip RAM. A modified ASCII character set, which includes several non–English characters, is decoded by an on–chip ROM. An on–screen character appears as a white or colored dot matrix on a black background.

Captions (video–related information) can be up to four rows appearing anywhere on the screen and can be displayed in two modes: roll–up, paint–on, or pop–on. With rollup captions, the row scrolls up and new information appears at the bottom row each time a carriage return is received. Pop–on captions work with two memories. One memory is displayed while the other is used to accumulate new data. A special command causes the information to be exchanged in the two memories, thus causing the entire caption to appear at once.

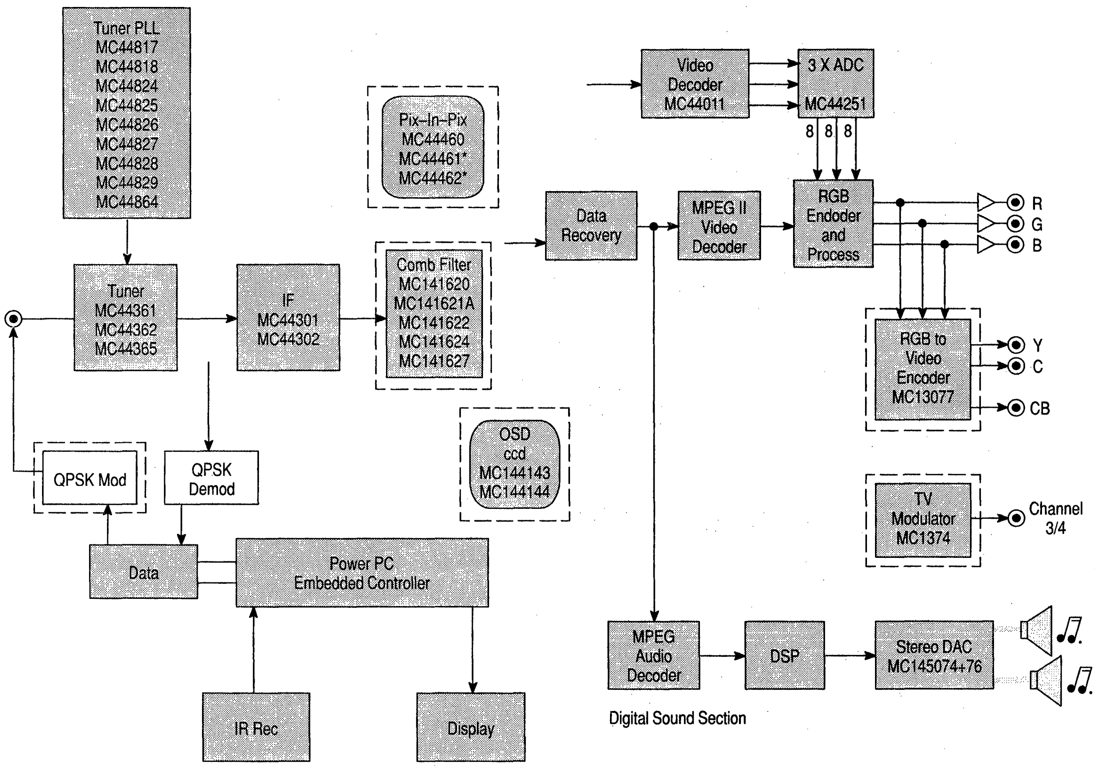
When text (non–video related information) is displayed, the rows contain a maximum of 32 characters over a black box which overwrites the screen. Fifteen rows of characters are displayed in the text mode.

An on–chip processor controls the manipulation of data for storage and display. Also controlled are the loading, addressing, and clearing of the display RAM. The processor transfers the data received to the RAM during scan lines 21 through 42. The operation of the display RAM, character ROM, and output logic circuits are controlled during scan lines 43 through 237. The functions of the MC144144 are controlled via a serial port which may be configured to be either I^2C or SPI.

- Conforms to FCC Report and Order as Amended by the Petition for Reconsideration on Gen. Doc. 91–1
- Conforms to EIA–608 for XDS Data Structure
- Supports Four Different Data Channels for Field 1 and Five Different Data Channels for Field 2, Time Multiplexed within the Line 21 Data Stream: Captions Utilizing Languages 1 and 2, Text Utilizing Languages 1 and 2 and XDS Support
- Output Logic Provides Hardware Underline Control and Italics Slant Generation
- Single Supply, Operating Voltage Range: 4.75 to 5.25 V
- Supply Current: 20 mA (Preliminary)
- Operating Temperature Range: 0 to 70°C
- Composite Video Input Range: 0.7 to 1.4 V_{pp}
- Horizontal Input Polarity: Either Positive or Negative
- Internal Timing and Sync Signals Derived from On–Chip VCO


+ 5.0 V
VDO
12
13
VIN/ INTRO
6 4 15 14 16
SMS SEN SCK SDA SDO
VIDEO
7
BUFFER
DATA SLICER
SLICED
DATA
DATA CLK RECOVERY
DATALINE
SERIAL CONTROL PORT
DATA BUS
STATUS REG
TEST REG
DUAL CLAMP
LOCK
SIG
PG
AW
FEW
DIG II LOCK
VW
ROW
COMMAND PROCESSOR
ADDR BUS
8
SLICE LEVEL
SYNC SLICER
CSYNC
ROW LATCH
4
10
ADDRESS MUX
6
DOT CLK
COMP SYNC
CG LINES
DOT CLK DIV
V LOCK
CHAR CLK
DISPLAY RAM
MSYNC
CG LOGIC
CW
MSGR
CHAR CIR
DISPLAY LATACH
8
13
CHARACTER GEN
ADDR DEC
FLD
PH1
O/S
OSC
SS CTR
4
ADDR DECODER
PH2
I DRIVE & MUX
CONTROL
FLD
LS
SFLP
????
LINE & FLD CTR
OUTPUT LOGIC
FR
LINE AND FLD DECODERS
V/I REF
POR CKT
BOX BLUE GREEN RED
5
9
1
11
10
HIN
LPF
VSS
VSS(A)
RREF
17 3 2 18
LOOP FILTER

Set–Top Block Diagram



* In Development

PLL Tuning Circuits with 3–Wire Bus

MC44817BD, D

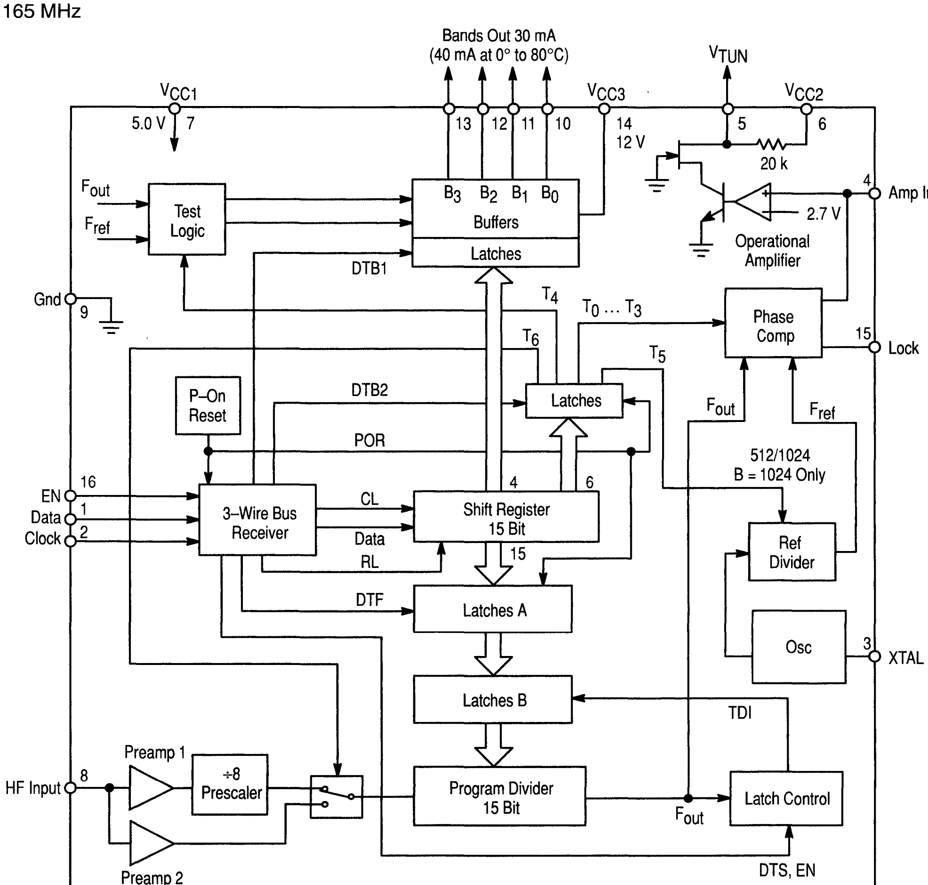
Case 751B

The MC44817/17B are tuning circuits for TV and VCR tuner applications. They contain on one chip all the functions required for PLL control of a VCO. The integrated circuits also contain a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44817 has programmable 512/1024 reference dividers while the MC44817B has a fixed reference divider of 1024.

The MC44817/17B are manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (3–Wire Bus). Data and Clock Inputs are IIC Bus Compatible
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider Accepts Input Frequencies up to 165 MHz
- Reference Divider: Programmable for Division Ratios 512 and 1024. The MC44817B has a Fixed 1024 Reference Divider
- 3–State Phase/Frequency Comparator
- Operational Amplifier for Direct Tuning Voltage Output (30 V)
- Four Integrated PNP Band Buffers for 40 mA (V_{CC1} to 14.4 V)
- Output Options for the Reference Frequency and the Programmable Divider
- Bus Protocol for 18 or 19 Bit Transmission
- Extra Protocol for 34 Bit for Test and Further Features
- High Sensitivity Preamplifier
- Circuit to Detect Phase Lock
- Fully ESD Protected



PLL Tuning Circuit with I²C Bus

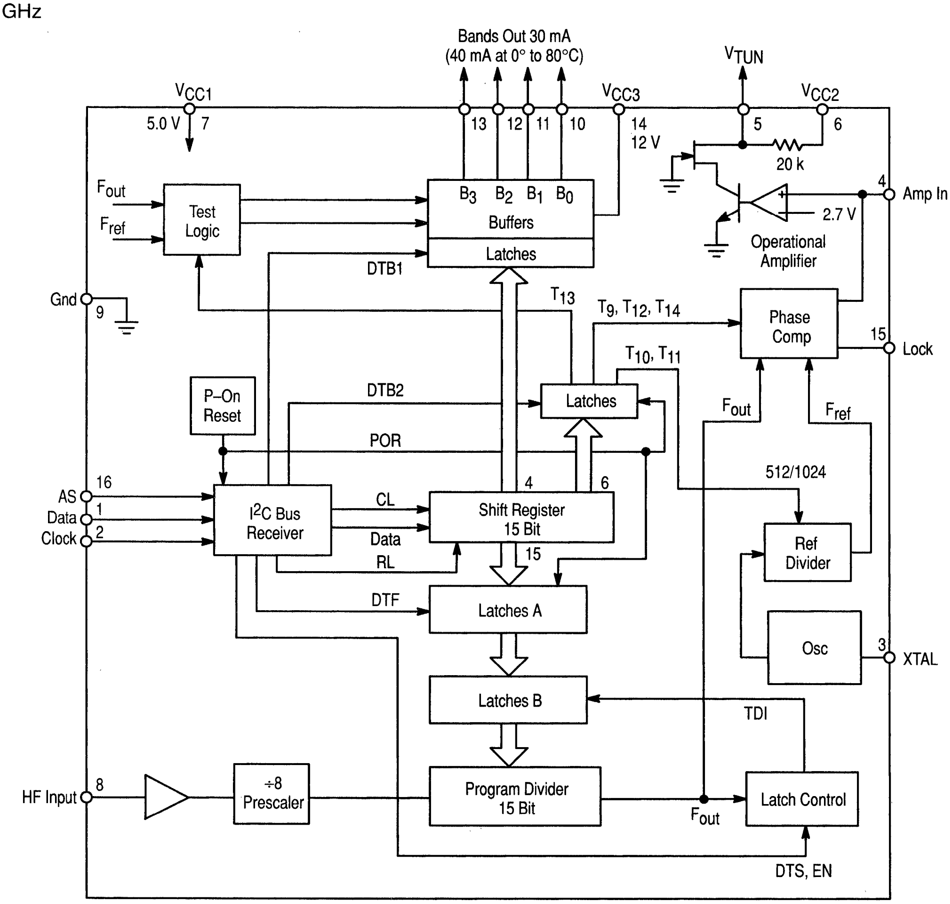
MC44818D

Case 751B

The MC44818 is a tuning circuit for TV and VCR tuner applications. It contains, on one chip, all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz. The MC44818 is a pin compatible drop–in replacement for the MC44817, where the only difference is the MC44818 has a fixed divide–by–8 prescaler (cannot be bypassed) and the MC44817 uses the three wire bus.

The MC44818 has programmable 512/1024 reference dividers and is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (I²C Bus). Data and Clock Inputs are 3–Wire Bus Compatible
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider Accepts Input Frequencies up to 165 MHz
- Reference Divider: Programmable for Division Ratios 512 and 1024.
- 3–State Phase/Frequency Comparator
- Operational Amplifier for Direct Tuning Voltage Output (30 V)
- Four Integrated PNP Band Buffers for 40 mA (V_{CC1} to 14.4 V)
- Output Options for the Reference Frequency and the Programmable Divider
- High Sensitivity Preamplifier
- Circuit to Detect Phase Lock
- Fully ESD Protected



PLL Tuning Circuits with I²C Bus

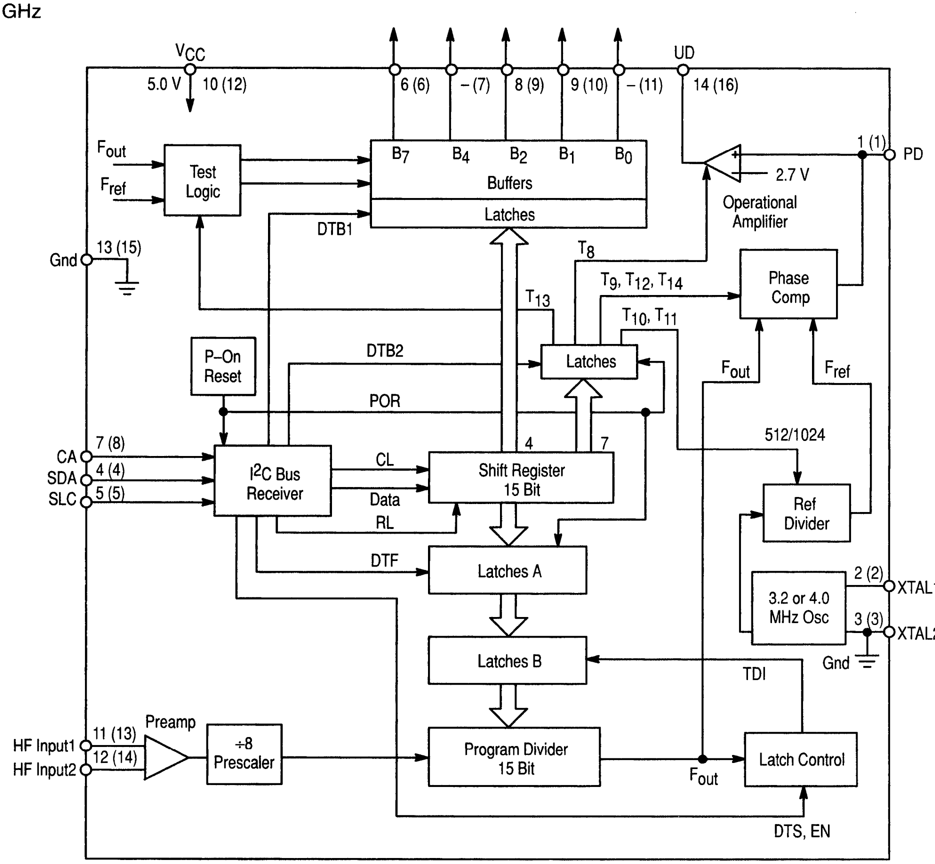
MC44824/25D

Case 751A, 751B

The MC44824/25 are tuning circuits for TV and VCR tuner applications. They contain on one chip all the functions required for PLL control of a VCO. The integrated circuits also contain a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44824/25 are manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (I²C Bus). Data and Clock Inputs are 3–Wire Bus Compatible
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider
- Reference Divider: Programmable for Division Ratios 512 and 1024
- 3–State Phase/Frequency Comparator
- 4 Programmable Chip Addresses
- 3 Output Buffers (MC44824) respectively; 5 Output Buffers (MC44825) for 10 mA/15 V
- Operational Amplifier for use with External NPN Transistor
- SO–14 Package for MC44824 and SO–16 for MC44825
- High Sensitivity Preamplifier
- Fully ESD Protected



MC44825 Pin Numbers ( )

PLL Tuning Circuit with 3–Wire Bus

MC44827DTB

Case 948F

The MC44827 is a tuning circuit for TV and VCR tuner applications. This device contains on one chip all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44827 is controlled by a 3–wire bus. It has the same function as the MC44828 which is I^2C bus controlled. The MC44827 and MC44828 can replace each other to allow conversion between 3–wire bus and I^2C bus control.

The MC44827 is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

The MC44827 has the same features as MC44817 with the following differences:

- Lower Power Consumption, 200 mW Typical
- Improved Prescaler with Higher Margins for Sensitivity and Temperature Range. (A typical device is functional in a temperature range greater than –40 to 100°C.)
- Lock Detector with Push–Pull Output
- No Bypass of Divide–by–8 Prescaler
- TSSOP Package

PLL Tuning Circuit with I^2C Bus

MC44828DTB

Case 948F

The MC44828 is a tuning circuit for TV and VCR tuner applications. This device contains on one chip all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44828 is controlled by an I^2C bus. It has the same function as the MC44827 which is 3–wire bus controlled. The MC44827 and MC44828 can replace each other to allow conversion between 3–wire bus and I^2C bus control.

The MC44828 is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

The MC44828 has the same features as MC44818 with the following differences:

- Lower Power Consumption, 200 mW Typical
- Improved Prescaler with Higher Margins for Sensitivity and Temperature Range. (A typical device is functional in a temperature range greater than –40 to 100°C.)
- Lock Detector with Push–Pull Output
- TSSOP Package

PLL Tuning Circuit with I²C Bus

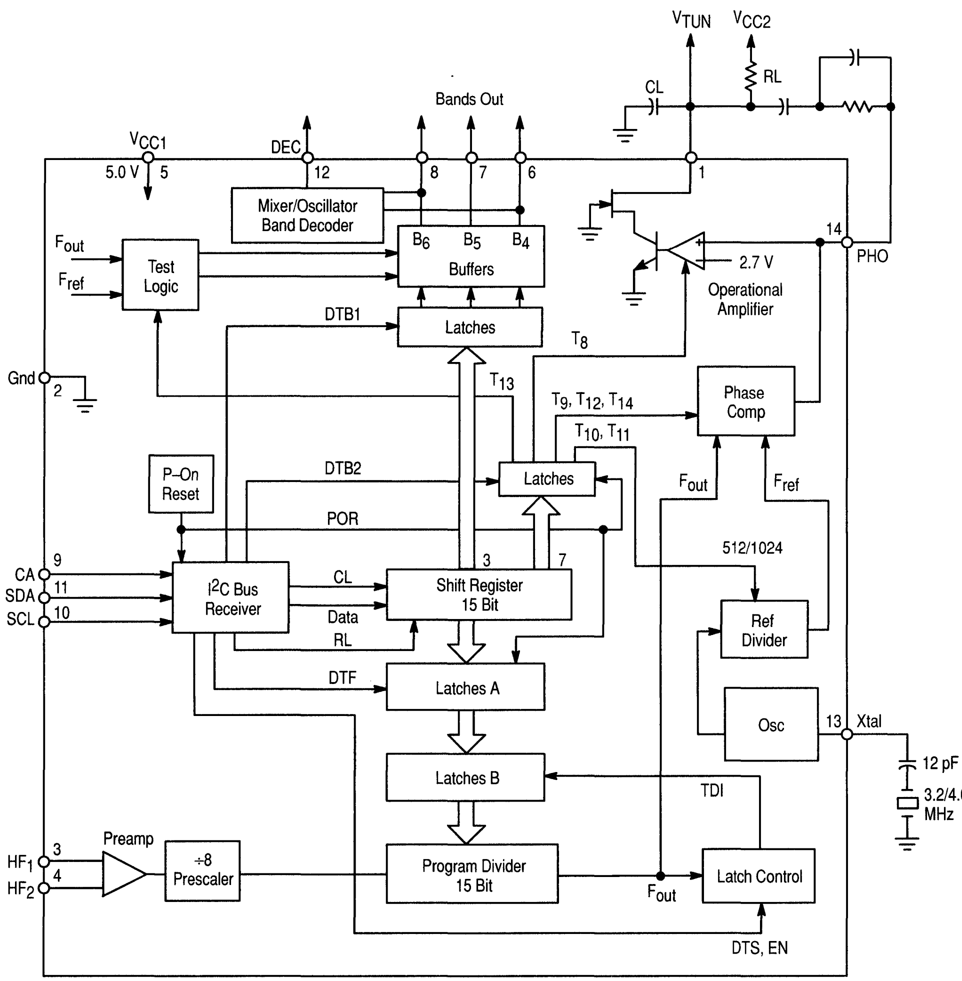
MC44829D

Case 751A

The MC44829 is a tuning circuit for TV and VCR tuner applications. It contains, on one chip, all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz. The circuit has a band decoder that provides the band switching signal for the mixer/oscillator circuit. The decoder is controlled by the buffer bits.

The MC44829 has programmable 512/1024 reference dividers and is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (I²C Bus)
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider
- Reference Divider: Programmable for Division Ratios 512 and 1024
- 3–State Phase/Frequency Comparator
- Operational Amplifier for Direct Tuning Voltage Output (30 V)
- Four Programmable Chip Addresses
- Integrated Band Decoder for the Mixer/Oscillator Circuit
- Band Buffers with Low "On" Voltage (0.4 V Maximum at 5.0 mA)
- Fully ESD Protected to MIL–STD–883C, Method 3015.7 (2000 V, 1.5 kΩ, 150 pF)



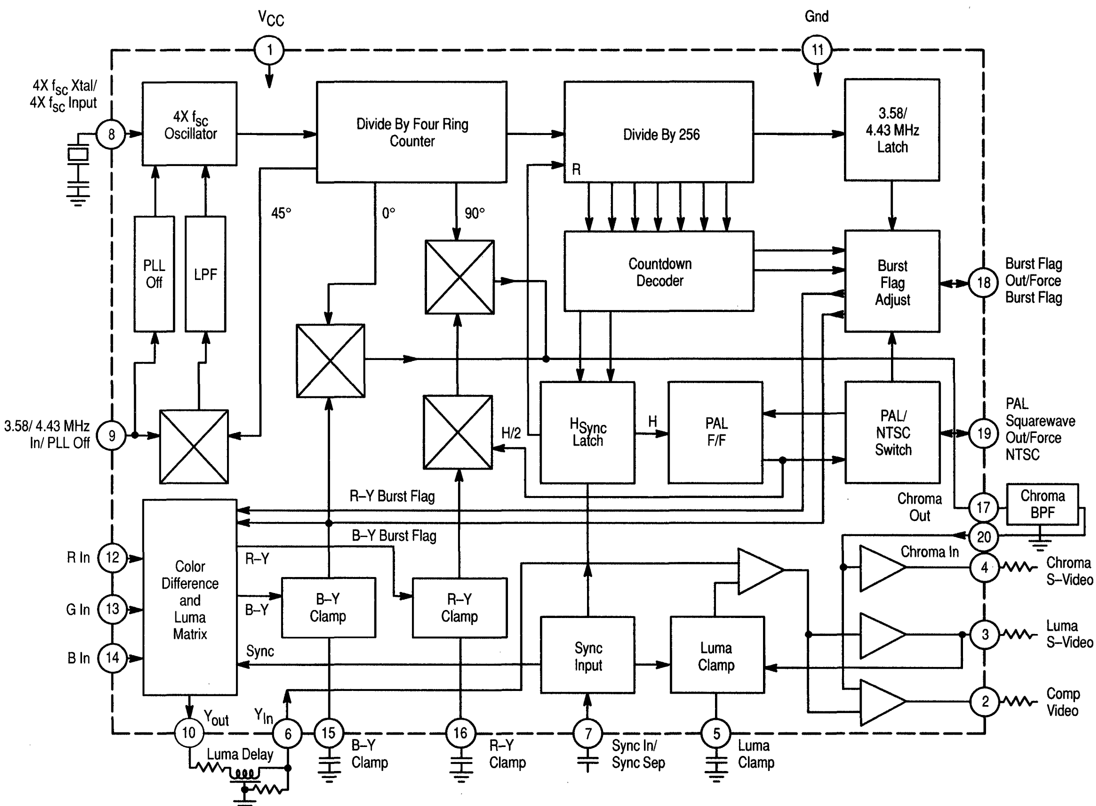
Advanced PAL/NTSC Encoder

MC13077P, DW

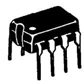
Case 738, 751D

The MC13077 is an economical, high quality, RGB encoder for PAL or NTSC applications. It accepts red, green, blue and composite sync inputs and delivers either composite PAL or NTSC video, and S–Video Chroma and Luma outputs. The MC13077 is manufactured using Motorola's high density, bipolar MOSAIC® process.

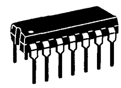
- Single 5.0 V Supply
- Composite Output
- S–Video Outputs
- PAL/NTSC Switchable
- PAL Squarewave Output
- PAL Sequence Resettable
- Internal/External Burst Flag
- Modulator Angles Accurate to 90°
- Burst Position/Duration Determined Digitally
- Subcarrier Reference from a Crystal or External Source



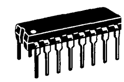
Consumer Electronic Circuits Package Overview



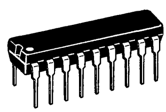
CASE 626
P SUFFIX



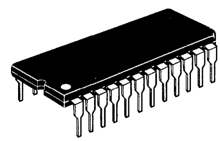
CASE 646
P SUFFIX



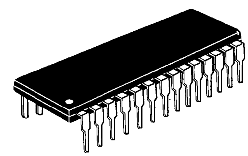
CASE 648
P SUFFIX



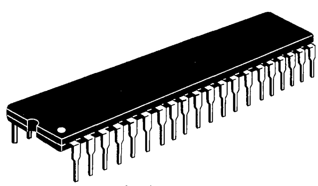
CASE 707
P SUFFIX



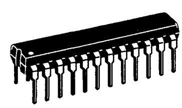
CASE 709
P SUFFIX



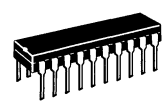
CASE 710
P SUFFIX



CASE 711
P SUFFIX

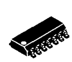


CASE 724
P SUFFIX

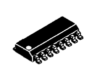


CASE 738
H, P SUFFIX

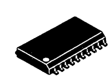
CASE 751
D SUFFIX



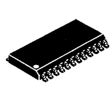
CASE 751A
D SUFFIX



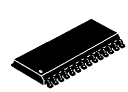
CASE 751B
D SUFFIX



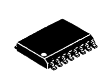
CASE 751D
DW SUFFIX



CASE 751E
DW SUFFIX

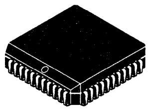


CASE 751F
DW SUFFIX

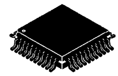


CASE 751G
DW SUFFIX

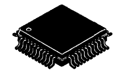
Consumer Electronic Circuits Package Overview (continued)



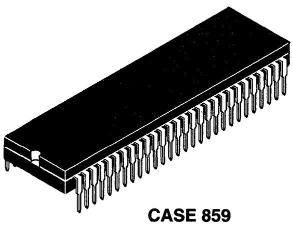
CASE 777
FN SUFFIX



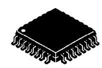
CASE 824, 824A
FB SUFFIX



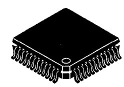
CASE 824E
FB SUFFIX



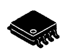
CASE 859
B SUFFIX



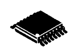
CASE 873
FU SUFFIX



CASE 898
FB, FU, P SUFFIX



CASE 904
F SUFFIX



CASE 948F
DTB SUFFIX

Automotive Electronic Circuits

In Brief . . .

Motorola Analog has established itself as a global leader in custom integrated circuits for the automotive market. With multiple design centers located on four continents, global process and assembly sites, and strategically located supply centers, Motorola serves the global automotive market needs. These products are key elements in the rapidly growing engine control, body, navigation, entertainment, and communication electronics portions of modern automobiles. Though Motorola is most active in supplying automotive custom designs, many of yesterday's proprietary custom devices have become standard products of today, available to the broad base manufacturers who support this industry. Today, based on new technologies, Motorola offers a wide array of standard products ranging from rugged high current "smart" fuel injector drivers which control and protect the fuel management system through the rigors of the underhood environment, to the latest SMARTMOS™ switches and series transient protectors. Several devices are targeted to support microprocessor housekeeping and data line protection. A wide range of packaging is available including die, flip–chip, and SOICs for high density layouts, to low thermal resistance multi–pin, single–in–line types for high power control ICs.

Automotive Electronic Circuits

Table 1. Voltage Regulators

Function	Features	Suffix/ Package	Device
Low Dropout Voltage Regulator	Positive fixed and adjustable output voltage regulators which maintain regulation with very low input to output voltage differential.	Z/29, T/221A, T/314D, TH/314A, TV/314B, DT/369A, DT–1/369, D2T/936, D2T/936A, D/751	LM2931, C
Low Dropout Dual Regulator	Positive low voltage differential regulator which features dual 5.0 V outputs, with currents in excess of 750 mA (switched) and 10 mA standby, and quiescent current less than 3.0 mA.	T/314D, TH/314A, TV/314B, D2T/936A	LM2935
Automotive Voltage Regulator	Provides load response control, duty cycle limiting, under/overvoltage and phase detection, high side MOSFET field control, voltage regulation in 12 V alternator systems.	DW/751D	MC33092
Low Dropout Voltage Regulator	Positive 5.0 V, 500 mA regulator having on–chip power–up–reset circuit with programmable delay, current limit, and thermal shutdown.	T/314D, TV/314B	MC33267
Low Dropout Voltage Regulator	Positive 3.3 V, 5.0 V, 12 V, 800 mA regulator.	D/751, DT/369A	MC33269

Table 2. Electronic Ignition

Function	Features	Suffix/ Package	Device
Electronic Ignition Circuit	Used in high energy variable dwell electronic ignition systems with variable reluctance sensors. Dwell and spark energy are externally adjustable. “Bumped” die for inverted mounting to substrate.	P/626, D/751, Flip–Chip	MC3334, MCCF3334
Electronic Ignition Circuit	Used in high energy electronic ignition systems requiring differential Hall Sensor control. “Bumped” die for inverted mounting to substrate.	DW/751G, Flip–Chip	MC33093, MCCF33093
Electronic Ignition Circuit	Used in high energy electronic ignition systems requiring single Hall Sensor control. “Bumped” die for inverted mounting to substrate.	DW/751G, Flip–Chip	MC33094, MCCF33094
Electronic Ignition Circuit	Used in high energy electronic ignition systems requiring single Hall Sensor control. Dwell feedback for coil variation. “Bumped” die for inverted mounting to substrate.	DW/751G, Flip–Chip	MC79076, MCCF79076

Table 3. Special Functions

Function	Features	Suffix/ Package	Device
Low Side Protected Switch	Single automotive low side switch having CMOS compatible input, 1.0 A maximum rating, with overcurrent, overvoltage and thermal protection.	T/221A, T–1/314D, DW/751G	MC3392
Low Current High–Side Switch	Drives loads from positive side of power supply and protects against high–voltage transients.	T/314D, DW/751G	MC3399
High–Side TMOS Driver	Designed to drive and protect N–channel power MOSFETs used in high side switching applications. Has internal charge pump, externally programmed timer and fault reporting.	P/626, D/751	MC33091A
MI–Bus Interface Stepper Motor Controller	High noise immunity serial communication using MI–Bus protocol to control relay drivers and motors in harsh environments. Four phase signals drive two phase motors in either half or full–step modes.	DW/751G	MC33192
Quad Fuel Injector Driver	Four low side switches with parallel CMOS compatible input control, $\leq$7.0 mA quiescent current, 0.25 Ω $r_{DS(on)}$ at 25°C independent outputs with 3.0 A current limiting and internal 65 V clamps.	T/821D, TV/821C	MC33293
Octal Serial Output Switch	Eight low side switches having 8–bit serial CMOS compatible input control, serial fault reporting, $\leq$4.0 mA quiescent current, independent 0.45 Ω $r_{DS(on)}$ at 25°C outputs with 3.0 A minimum current limiting and internal 55 V clamps.	P/738, DW/751E	MC33298
Integral Alternator Regulator	Control device used in conjunction with a Darlington device to monitor and control the field current in alternator charging systems. "Bumped" die for inverted mounting to substrate.	D/751A, Flip–Chip	MC33095 MCCF33095
Peripheral Clamping Array	Protects up to six MPU I/O lines against voltage transients.	*/626, D/751	TCF6000
Automotive Direction Indicator	Detects defective lamps and protects against overvoltage in automotive turn–signal applications. Replaces UAA1041B in most applications.	D/751, P/626	MC33193
Automotive Wash Wiper Timer	Standard wiper timer control device that drives a wiper motor relay and can perform the intermittent, afterwash and continuous wiper timer functions.	D/751, P/626	MC33197
Automotive ISO 9141 Serial Link Driver	Interface between the two–wire asynchronous serial communication interface (SCI) of a microcontroller and a special one–wire care diagnosis system (DIA).	D/751A	MC33199

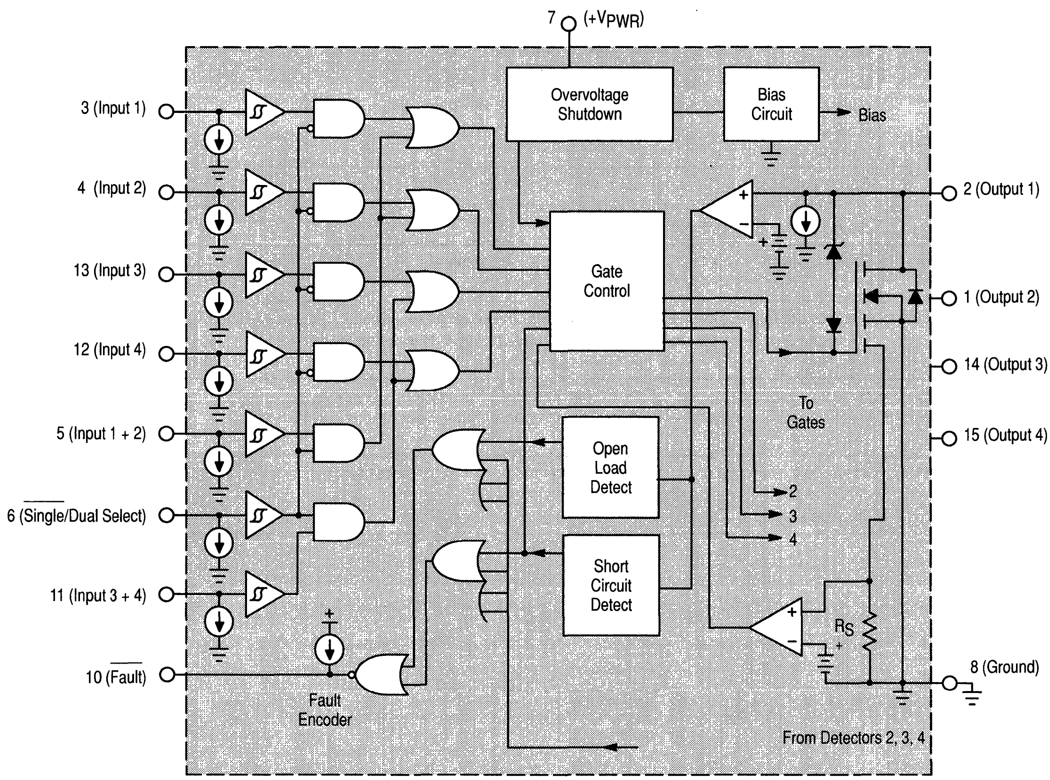
* No Suffix

Quad Fuel Injector Driver

MC33293T, MC33293TV

T_J = –40° to +150°C, Case 821D, C

The MC33293T is a monolithic quad low–side switching device having CMOS logic, bipolar/ CMOS analog circuitry, and DMOS power FETs. All inputs are CMOS compatible. Each independent output is internally clamped to 65 V, current limited to ≥ 3.0 A, and has an $r_{DS(on)}$ of ≤ 0.25 Ω with V_{PWR} ≥ 9.0 V and may be paralleled to lower $r_{DS(on)}$. Fault output reports existence of open loads (outputs "On" or "Off"), shorted loads, and over temperature condition of outputs. A shorted load condition will shut off only the specific output involved while allowing other outputs to operate normally. An overvoltage condition will shut off all outputs for the overvoltage duration. A single/dual mode select pin allows either independent input/output operation or paired output operation.

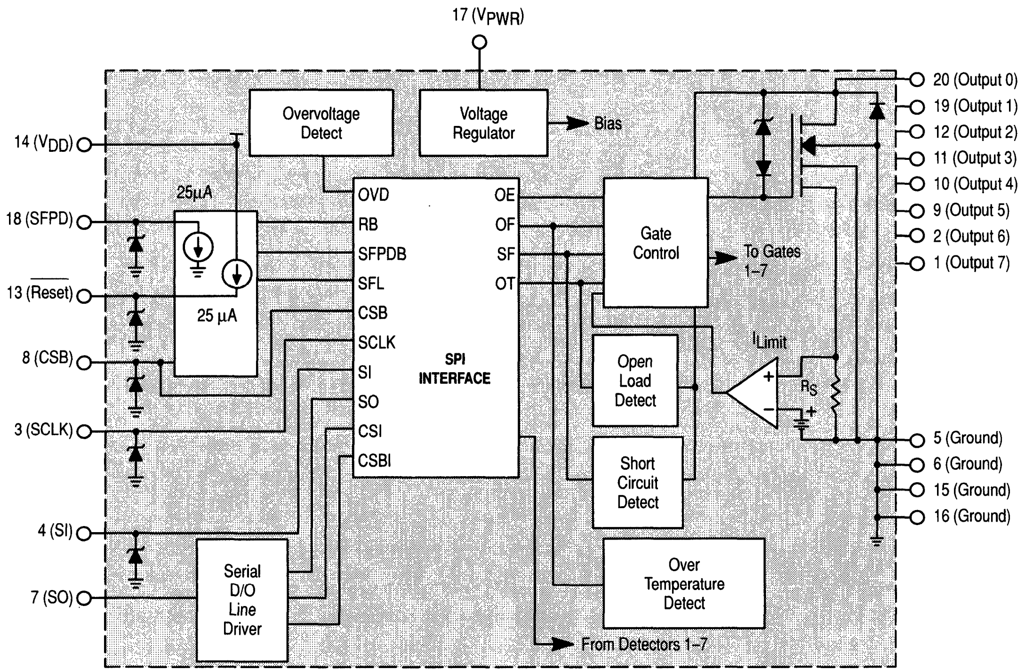


Octal Serial Switch

MC33298P, MC33298DW

T_J = –40° to +150°C, Case 738, 751E

The MC33298 is a monolithic eight output low–side switch with 8–bit serial input control. Incorporates CMOS logic, bipolar/CMOS analog circuitry, and DMOS power FETs. All inputs are CMOS compatible. It is designed to interface to a microcontroller and switch inductive or incandescent loads. Each independent output is internally clamped to 55 V, current limited to ≥ 3.0 A, and has an $r_{DS(on)}$ of ≤ 0.45 Ω with V_{PWR} ≥ 9.0 V. This device has low standby current, cascadable fault status reporting, output diagnostics, and shutdown for each output.

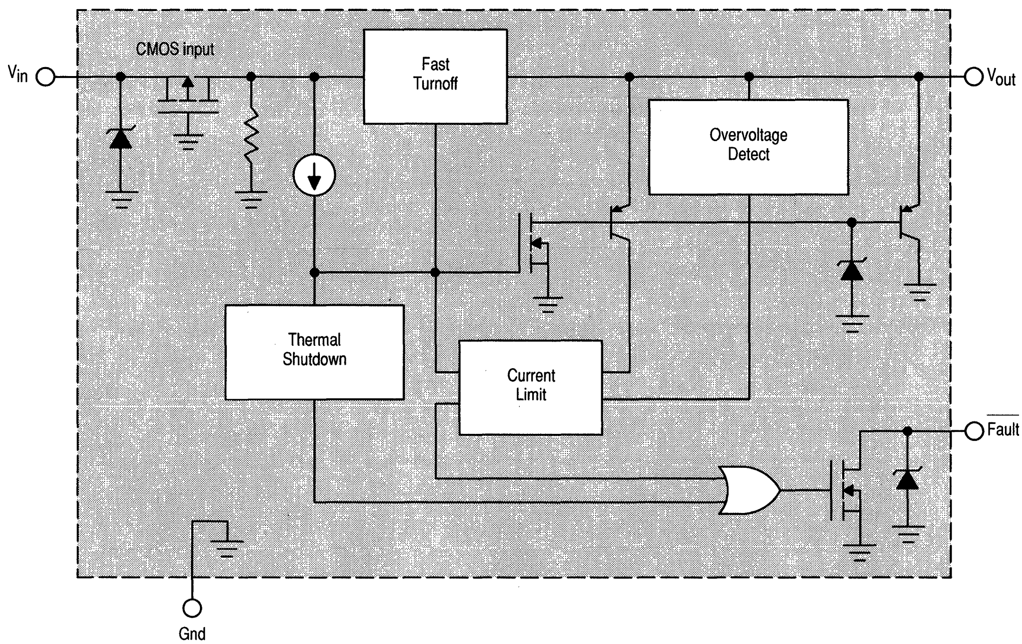


Low Side Protected Switch

MC3392T, T–1, DW

T_J = –40° to +150°C,
Case 221A, 314D, 751G

Single low side protected switch with fault reporting capability. Input is CMOS compatible. Output is short circuit protected to 1.0 A minimum with a unique current fold–back feature. Device has internal output clamp for driving inductive loads with overcurrent, overvoltage, and thermal protection. When driving a moderate load, the MC3392 performs as an extremely high gain, low saturation Darlington transistor having a CMOS input characteristic with added protection features. In some applications, the three terminal version can replace industry standard TIP100/101 NPN power Darlington transistors.

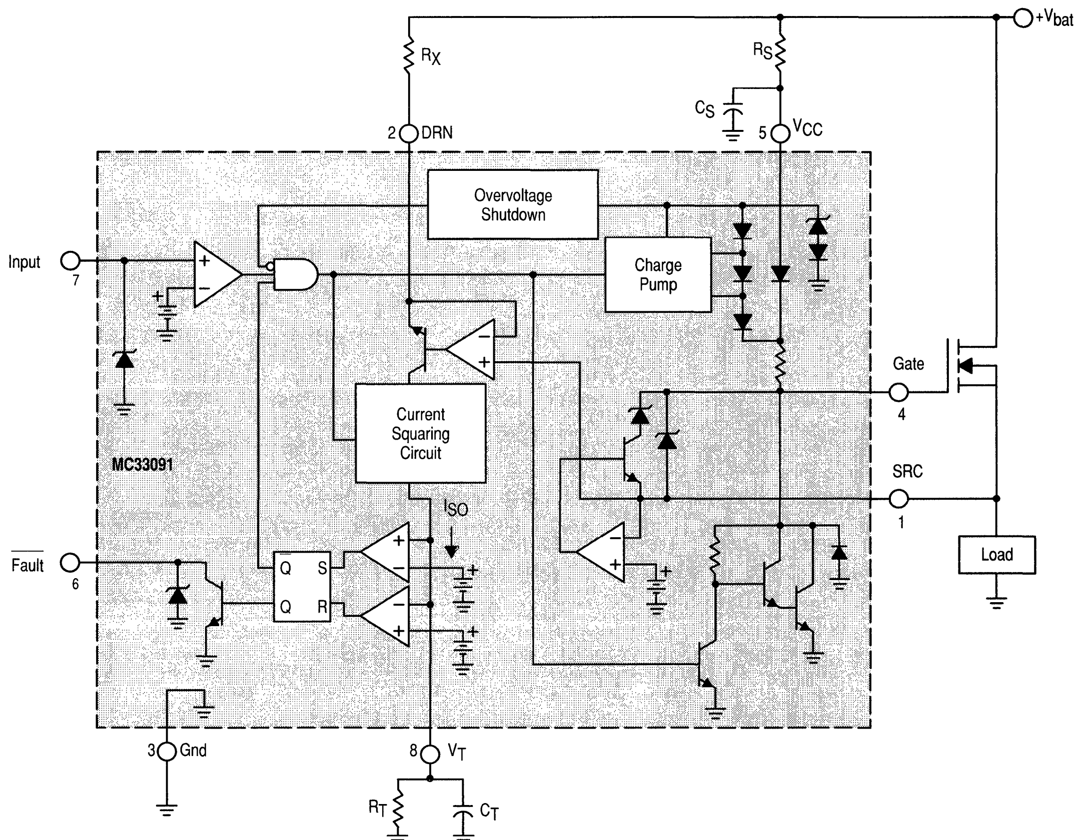


High Side TMOS Driver

MC33091AP, AD

T_J = –40° to +150°C, Case 626, 751

Offers an economical solution to drive and protect N–channel power TMOS devices used in high side switching configurations. Unique device monitors load resulting V_{DS}. TMOS voltage to produce a proportional current used to drive an externally programmed over current timer circuit to protect the TMOS device from shorted load conditions. Timer can be programmed to accommodate driving incandescent loads. Few external components required to drive a wide variety of N–channel TMOS devices. A Fault output is made available through the use of an open collector NPN transistor requiring a single pull–up resistor for operation. Input is CMOS compatible. Device uses ≤ 3.0 μA standby current and has an internal charge pump requiring no external components for operation.

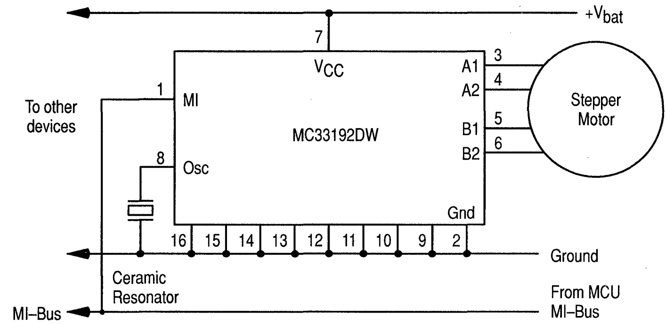


MI–Bus Interface Stepper Motor Controller

MC33192DW

T_J = –40° to +100°C, Case 751G

Intended to control loads in harsh automotive environments using a serial communication bus. Can provide satisfactory real time control of up to eight stepper motors using MI–Bus protocol. Use of MI–Bus offers a noise immune system solution for difficult applications involving relays and motors. The stepper motor controller provides four phase signals to drive two phase motors in either half of full–step modes. Designed to interface to a microprocessor with minimal amount of wiring, affording an economical and versatile system.



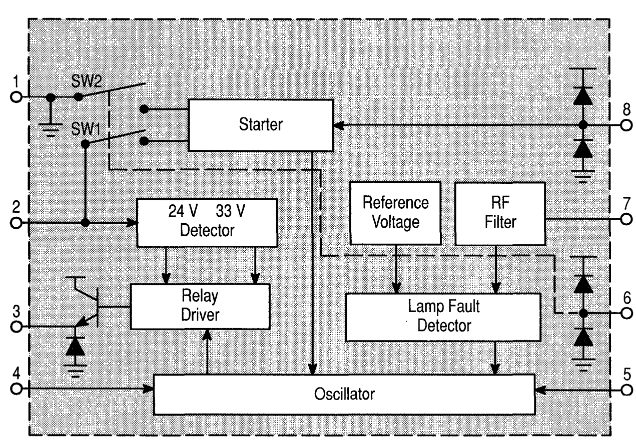
Automotive Direction Indicator

MC33193P, D

T_A = –40° to +125°C, Case 626, 751

The MC33193 is a new generation industry standard UAA1041 "Flasher". It has been developed for enhanced EMI sensitivity, system reliability, and improved wiring simplification. The MC33193 is pin compatible with the UAA1041 and UAA1041B in the standard application configuration as shown in Figure 9, without lamp short circuit detection and using a 20 mΩ shunt resistor. The MC33193 has a standby mode of operation requiring very low standby supply current and can be directly connected to the vehicle's battery. It includes a RF filter on the Fault detection pin (Pin 7) for EMI purposes. Fault detection thresholds are reduced relative to those of the UAA1041 allowing a lower shunt resistance value (20 mΩ) to be use.

- Pin Compatible with the UAA1041
- Defective Lamp Detection Threshold
- RF Filter for EMI Purposes
- Load Dump Protection
- Double Battery Capability for Jump Start Protection
- Internal Free Wheeling Diode Protection
- Low Standby Current Mode



Automotive Wash Wiper Timer

MC33197D

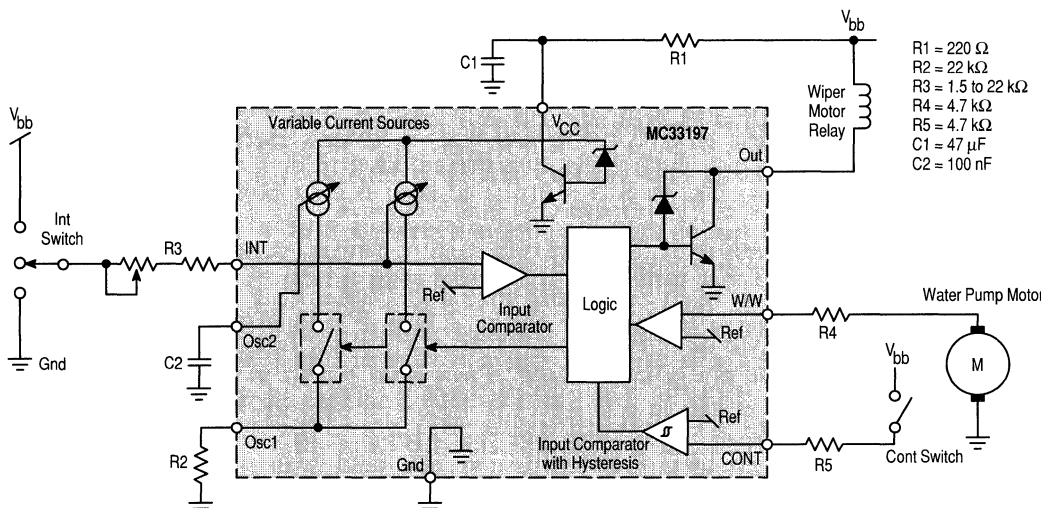
T_A = –40° to +105°C, Case 751

MC33197P

T_A = –40° to +125°C, Case 626

The MC33197 is a standard wiper timer control device designed for harsh automotive applications. The device can perform the intermittent, after wash, and continuous wiper timer functions. It is designed to directly drive a wiper motor relay. The MC33197 requires very few external components for full system implementation. The intermittent control pin can be switched to ground or V_{bat} to meet a large variety of possible applications. The intermittent timing can be fixed or adjustable via an external resistor. The MC33197 is built using bipolar technology and parametrically specified over the automotive ambient temperature range and 8.0 to 16 V supply voltage. The MC33197 can operate in both front and rear wiper applications.

- Adjustable Time Interval of Less Than 500 ms to More Than 30 s
- Intermittent Control Pin Can Be Switched to Ground or V_{bat}
- Adjustable After Wipe Time
- Priority to Continuous Wipe
- Minimum Number of Timing Components
- Integrated Relay Driver With Free Wheeling Protection Diode
- Operating Voltage Range From 8.0 to 16 V
- For Front Wiper and Rear Wiper Window Applications



Automotive ISO 9141 Serial Link Driver

MC33199D

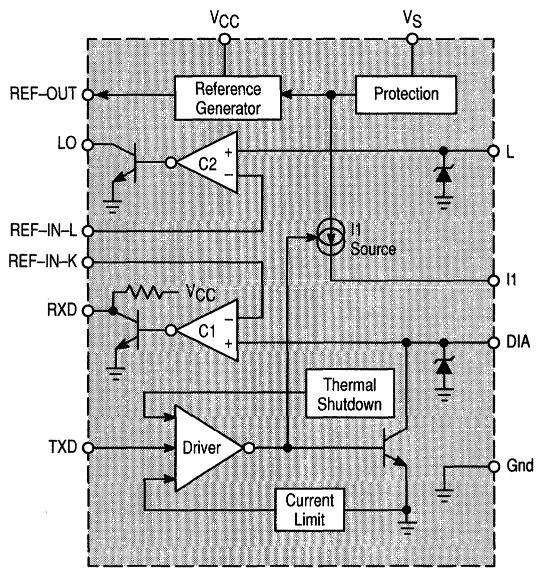
T_A = –40° to +125°C, Case 751A

The MC33199D is a serial interface circuit used in diagnostic applications. It is the interface between the microcontroller and the special K and L Lines of the ISO diagnostic port. The MC33199D has been designed to meet the “Diagnosis System ISO 9141” specification.

The device has a bi–directional bus K Line driver, fully protected against short circuits and over temperature. It also includes the L Line receiver, used during the wake up sequence in the ISO transmission.

The MC33199 has a unique feature which allows transmission baud rate up to 200 k baud.

- Electrically Compatible with Specification “Diagnosis System ISO 9141”
- Transmission Speed Up to 200 k Baud
- Internal Voltage Reference Generator for Line Comparator Thresholds
- TXD, RXD and LO Pins are 5.0 V CMOS Compatible
- High Current Capability of DIA Pin (K Line)
- Short Circuit Protection for the K Line Input
- Over Temperature Shutdown with Hysteresis
- Large Operating Range of Driver Supply Voltage
- Full Operating Temperature Range
- ESD Protected Pins

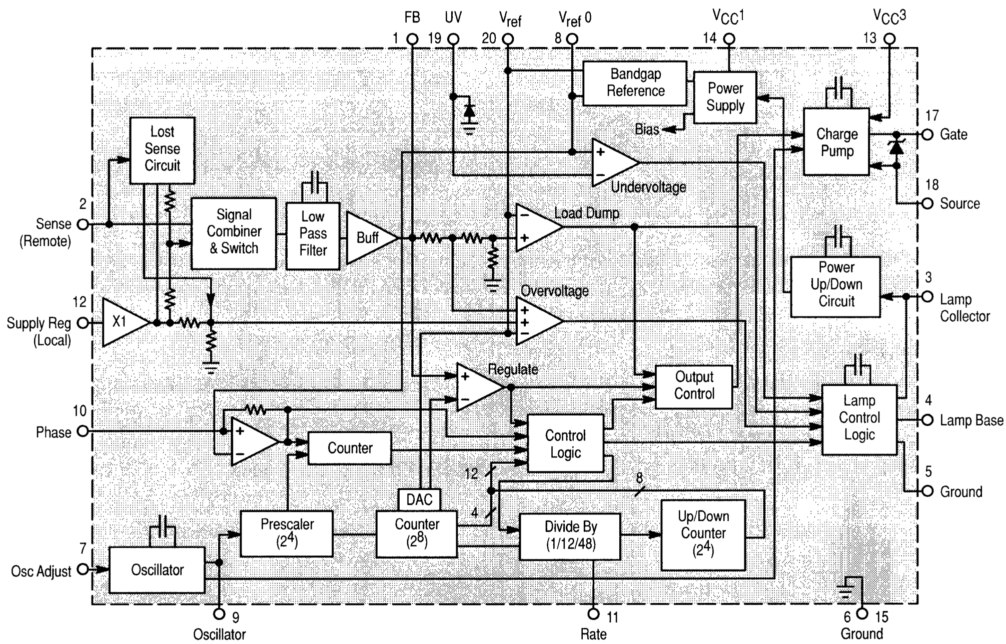


Alternator Voltage Regulator

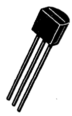
MC33092DW

T_J = –40° to +125°C, Case 751D

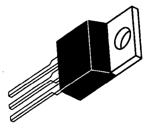
Provides voltage regulation and load response control in diode rectified 12 V alternator charging systems. Provides externally programmed load response control of the alternator output current to eliminate engine speed hunting and vibration due to sudden electrical loads. Monitors and compares the system battery voltage to an externally programmed set point value and pulse width modulates an N–channel MOSFET transistor to control the average alternator field current. In addition, has duty cycle limiting, under/overvoltage and phase detection (broken belt) protective features.



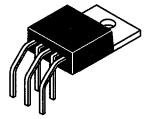
Automotive Electronic Circuits Package Overview



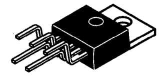
CASE 29
Z SUFFIX



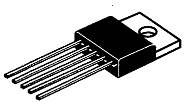
CASE 221A
T SUFFIX



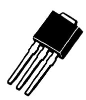
CASE 314A
TH SUFFIX



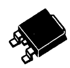
CASE 314B
TV SUFFIX



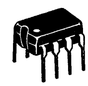
CASE 314D
T, T–1 SUFFIX



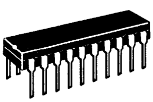
CASE 369
DT–1 SUFFIX



CASE 369A
DT SUFFIX

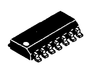


CASE 626
P, NO SUFFIX

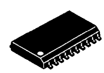


CASE 738
P SUFFIX

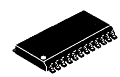
CASE 751
D SUFFIX



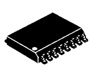
CASE 751A
D SUFFIX



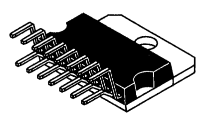
CASE 751D
DW SUFFIX



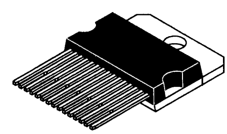
CASE 751E
DW SUFFIX



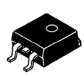
CASE 751G
DW SUFFIX



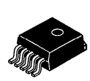
CASE 821C
TV SUFFIX



CASE 821D
T SUFFIX



CASE 936
D2T SUFFIX



CASE 936A
D2T SUFFIX

Other Analog Circuits

In Brief . . .

A variety of other analog circuits are provided for special applications with both bipolar and CMOS technologies. These circuits range from the industry standard analog timing circuits and multipliers to specialized CMOS smoke detectors. These products provide key functions in a wide range of applications, including data transmission, commercial smoke detectors, and various industrial controls.

Timing Circuits

These highly stable timers are capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free–running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The output structure can source or sink up to 200 mA or drive TTL circuits. Timing intervals from microseconds through hours can be obtained. Additional terminals are provided for triggering or resetting if desired.

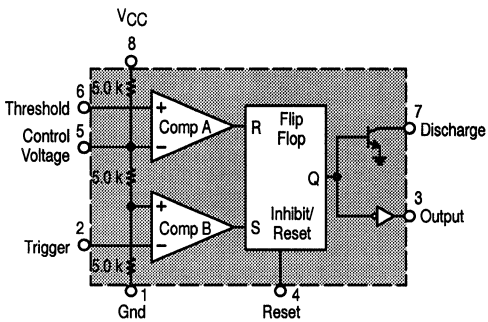
Singles

MC1455P1, D

T_A = 0° to +70°C, Case 626, 751

MC1455BP1, D

T_A = −40° to +85°C, Case 626, 751



Duals

MC3456P

T_A = 0° to +70°C, Case 646

NE556N, D

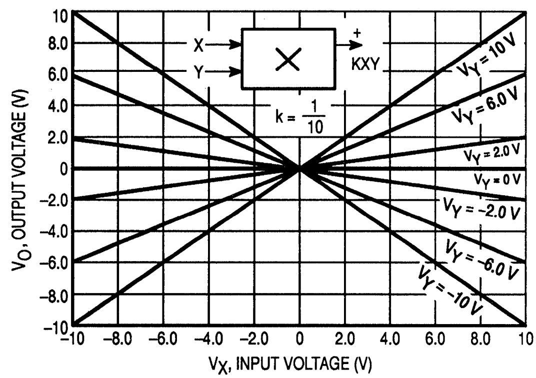
T_A = 0° to +70°C, Case 646, 751A

Multipliers

Linear Four–Quadrant Multipliers

Multipliers are designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square, root–mean–square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

Multiplier Transfer Characteristics



MC1494P

T_A = 0° to +70°C, Case 648

This device has all the necessary internal regulation and references. The single–ended output is referenced to ground.

MC1495D, P

T_A = 0° to +70°C, Case 751A, 646

Maximum versatility is assured by allowing the user to select the level shift method.

MC1495BP

T_A = −40° to +125°C, Case 646

Linearity and offset are actually tested over temperature. This is an improved specification over previous versions.

Smoke Detectors (CMOS)

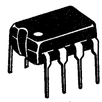
These smoke detector ICs require a minimum number of external components. When smoke is sensed, or a low battery voltage is detected, an alarm is sounded via an external piezoelectric transducer. All devices are designed to comply with UL specifications.

Table 1. Smoke Detectors (CMOS)

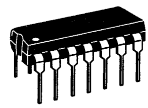
Function	Recommended Power Source	Unique Feature	Low Battery Detector	Piezoelectric Horn Driver	Complies with UL217 and UL268	Device Number	Suffix/ Package
Ionization–Type Smoke Detector	Battery	High Input Impedance FET Comparator	✓	✓	✓	MC14467–1	P1/646
	Line		–	–	✓	MC14578	P/648
Ionization–Type Smoke Detector with Interconnect	Battery		✓	✓	✓	MC14468	
	Line		–	✓	✓	MC14470	
Photoelectric–Type Smoke Detector with Interconnect	Battery	Photo Amplifier	✓	✓	✓	MC145010	P/648, DW/751G
	Line		(1)	✓	✓	MC145011	
	Battery	Photo Amplifier Temporal Pattern	✓	✓	✓	MC145012	
	Line		(1)	✓	✓	MC145013	
Ionization–Type Smoke Detector	Battery	High Input Impedance FET Comparator Temporal Pattern	✓	✓	✓	MC145017	P/648
Ionization–Type Smoke Detector with Interconnect	Battery		✓	✓	✓	MC145018	

(1) Low–supply detector.

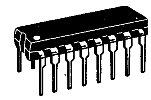
Other Analog Circuits Package Overview



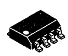
CASE 626
P1 SUFFIX



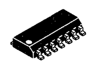
CASE 646
N, P, P1 SUFFIX



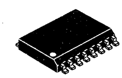
CASE 648
P SUFFIX



CASE 751
D SUFFIX



CASE 751A
D SUFFIX



CASE 751G
DW SUFFIX

Tape and Reel Options

In Brief . . .

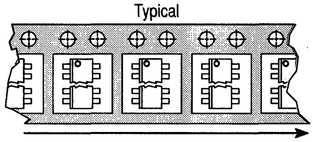
Motorola offers the convenience of Tape and Reel packaging for our growing family of standard integrated circuit products. Reels are available to support the requirements of both first and second generation pick–and–place equipment. The packaging fully conforms to the latest EIA–481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel–back cover tape.

Tape and Reel

Mechanical Polarization

SOIC DEVICES

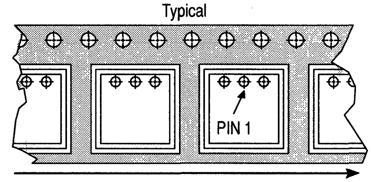
Typical



User Direction of Feed

PLCC DEVICES

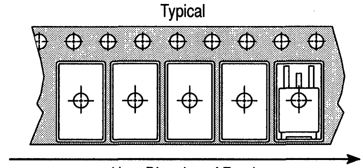
Typical



User Direction of Feed

DPAK DEVICES

Typical



User Direction of Feed

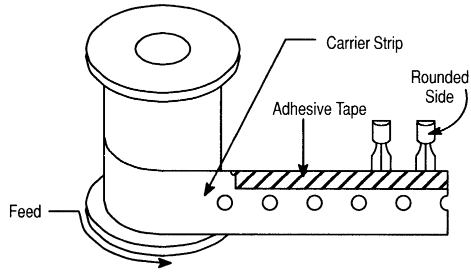
Package	Tape Width (mm)	Device[1] per Reel	Reel Size (inch)	Device Suffix
SO–8, SOP–8	12	2,500	13	R2
SO–14	16	2,500	13	R2
SO–16	16	2,500	13	R2
SO–16L, SO–8+8L WIDE	16	1,000	13	R2
SO–20L WIDE	24	1,000	13	R2
SO–24L WIDE	24	1,000	13	R2
SO–28L WIDE	24	1,000	13	R2
SO–28L WIDE	32	1,000	13	R3
PLCC–20	16	1,000	13	R2
PLCC–28	24	500	13	R2
PLCC–44	32	500	13	R2
PLCC–52	32	500	13	R2
PLCC–68	44	250	13	R2
PLCC–84	44	250	13	R2
TO–226AA (TO–92)[2]	18	2,000	13	RA, RE, RP, or RM (Ammo Pack) only
DPAK	16	2,500	13	RK

(1) Minimum order quantity is 1 reel. Distributors/OEM customers may break lots or reels at their option, however broken reels may not be returned.
(2) Integrated circuits in TO–226AA packages are available in Styes A and E only, with optional "Ammo Pack" (Suffix RP or RM). The RA and RP configurations are preferred. For ordering information please contact your local Motorola Semiconductor Sales Office.

Tape and Reel (continued)

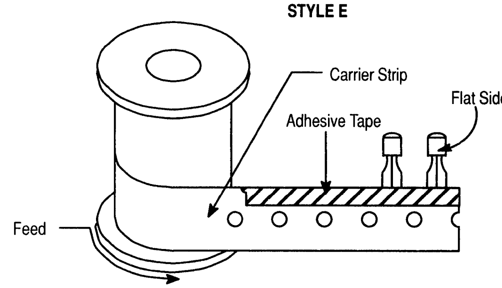
TO–92 Reel Styles

STYLE A
(Preferred)



Rounded side of transistor and adhesive tape visible.

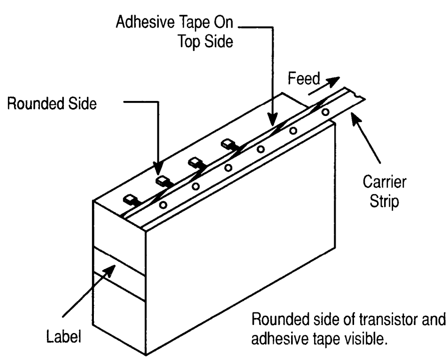
STYLE E



Flat side of transistor and adhesive tape visible.

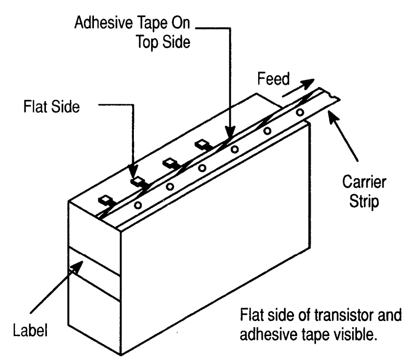
TO–92 Ammo Pack Styles

STYLE P
(Preferred)



Style P ammo pack is equivalent to Styles A and B of reel pack dependent on feed orientation from box.

STYLE M



Style M ammo pack is equivalent to Style E of reel pack dependent on feed orientation from box.

Analog MPQ Table

Tape/Reel and Ammo Pack

Package Type	Package Code	MPQ
PLCC		
Case 775	0802	1000/reel
Case 776	0804	500/reel
Case 777	0801	500/reel
SOIC		
Case 751	0095	2500/reel
Case 751A	0096	2500/reel
Case 751B	0097	2500/reel
Case 751G	2003	1000/reel
Case 751D	2005	1000/reel
Case 751E	2008	1000/reel
Case 751F	2009	1000/reel
TO–92		
Case 29	0031	2000/reel
Case 29	0031	2000/Ammo Pack

Communications, Power and Signal Technologies Group Products

In Brief . . .

Many leading semiconductor manufacturers have either de–emphasized or eliminated discrete components from their product portfolio. At Motorola, exceptional long–term growth and outstanding customer acceptance of our portfolio are the most significant effects of Motorola's superiority in providing bipolar and MOS transistors, diodes, thyristors, zeners, opto, RF, rectifier, and sensor devices.

Consistent, ongoing improvements in product development and packaging processing continue to ensure Motorola's position as the most broad–based discrete supplier in the world. The increased use of automatic placement equipment has driven the trend towards surface mount packaging.

Motorola continues to expand upon a broad offering of discrete surface mount packages which continue to advance state–of–the–art designs that cannot be accomplished with insertion technology. Surface mount technology is cost effective, allowing users the opportunity to utilize smaller units and increased functions with less board space. In many electronic applications, complex integrated solutions with a multitude of functions can replace several active and passive components.

SMARTDISCRETES, RF hybrid amplifiers and modules and RF monolithic integrated circuits, pressure and temperature sensors, optoelectronics and hybrid power modules are a few of the exciting new products which provide more reliable, intelligent discrete devices. Key initiatives to raise products and services to a Six Sigma standard (99.9997% defect–free), reduce total cycle time in all activities, and provide leadership in the areas of product and manufacturing ensure that Motorola will continue to be the manufacturer of choice for all your discrete semiconductor requirements.

Page

Small Signal Transistors, FETs and Diodes

In Brief . . .

New in this revision is Motorola's GreenLine™ portfolio of devices. They feature energy–conserving traits superior to those of our existing line of standard parts for the same usage. GreenLine devices can actually help reduce the power demands of your products.

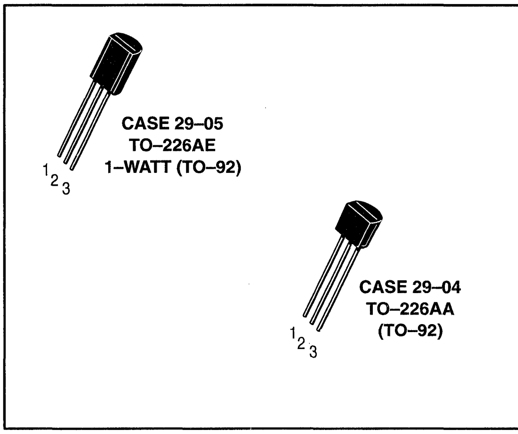
Also, this section highlights semiconductors that are the most popular and have a history of high usage for the most applications.

It covers a wide range of Small Signal plastic and metal–can semiconductors.

A large selection of encapsulated plastic transistors, FETs and diodes are available for surface mount and insertion assembly technology. Plastic packages include TO–92 (TO–226AA), 1 Watt TO–92 (TO–226AE), SOT–23, SC–59, SC–70/SOT–323 and SOT–223. Plastic multiples are available in 14–pin and 16–pin dual in–line packages for insertion applications: SO–8, SO–14, and SO–16 for surface mount applications.

Metal–can packages are available for applications requiring higher power dissipation or having hermetic requirements in TO–18 (TO–206AA) and TO–39 (TO–205AD).

Bipolar Transistors



Plastic–Encapsulated Transistors

Motorola's Small Signal TO–226 plastic transistors encompass hundreds of devices with a wide variety of characteristics for general–purpose, amplifier and switching applications. The popular high–volume package combines proven reliability, performance, economy and convenience to provide the perfect solution for industrial and consumer design problems. All devices are laser marked for ease of identification and shipped in antistatic containers, as part of Motorola's ongoing practice of maintaining the highest standards of quality and reliability.

Table 1. Plastic–Encapsulated General–Purpose Transistors

These general–purpose transistors are designed for small–signal amplification from dc to low ratio frequencies. They are also useful as oscillators and general–purpose switches. Complementary devices shown where available (Tables 1–4).

NPN	PNP	$V_{(BR)CEO}$ Volts Min	f_T @ I_C MHz Min	f_T @ I_C mA	I_C mA Max	h_{FE} @ I_C Min	h_{FE} @ I_C Max	h_{FE} @ I_C mA	NF dB Max	Style
Case 29–04 — TO–226AA (TO–92)										
MPS8099	***MPS8599***	80	150	10	500	100	300	1.0	—	1
MPSA06	***MPSA56***	80	100	10	500	100	—	100	—	1
2N4410	—	80	60	10	250	60	400	10	—	1
BC546	BC556	65	150	10	100	120	450	2.0	10	17
BC546A	—	65	150	10	100	120	220	2.0	10	17
BC546B	BC556B	65	150	10	100	180	450	2.0	10	17
MPSA05	MPSA55	60	100	10	500	100	—	100	—	1
—	***MPS2907A***	60	200	50	600	100	300	150	—	1
BC182	BC212	50	200(1)	10	100	120	500	2.0	10	14
BC237B	BC307B	45	150	10	100	200	460	2.0	10	17
BC337	BC327	45	210(1)	10	800	100	630	100	—	17
BC547	BC557	45	150	10	100	120	800	2.0	10	17
BC547A	BC557A	45	150	10	100	120	220	2.0	10	17
BC547B	BC557B	45	150	10	100	180	450	2.0	10	17
BC547C	BC557C	45	150	10	100	380	800	2.0	10	17
MPSA20	MPSA70	40	125	5.0	100	40	400	5.0	—	1
MPS2222A	—	40	300	20	600	100	300	150	—	1
2N4401	***2N4403***	40	200	20	600	100	300	150	—	1
2N4400	2N4402	40	150	20	600	50	150	150	—	1
MPS6602	***MPS6652***	40	100	50	1000	50	—	500	—	1
2N3903	2N3905	40	200	10	200	50	150	10	6.0	1
2N3904	***2N3906***	40	250	10	200	100	300	10	5.0	1
BC548	—	30	300(1)	10	100	110	800	2.0	10	17
BC548A	—	30	300(1)	10	100	120	220	2.0	10	17
BC548B	BC558B	30	300(1)	10	100	200	450	2.0	10	17
BC548C	—	30	300	10	100	420	800	2.0	10	17
2N4123	2N4125	30	200	10	200	50	150	2.0	6.0	1
2N4124	2N4126	25	250	10	200	120	360	2.0	4.0	1
BC338	BC328	25	210(1)	10	800	100	630	100	—	17

(1) Typical

Devices listed in bold, italic are Motorola preferred devices.

Plastic–Encapsulated Transistors (continued)

Table 1. Plastic–Encapsulated General–Purpose Transistors (continued)

NPN	PNP	$V_{(BR)CEO}$ Volts Min	f_T @ I_C MHz Min	mA	I_C A Max	h_{FE} @ I_C Min	Max	mA	$V_{CE(sat)}$ @ I_C @ I_B Volts Max	mA	mA	Style
Case 29–05 — TO–226AE (1–WATT TO–92)												
	BDB02D	100	50	200	0.5	40	400	100	0.7	1000	100	1
BDC01D	BDC02D	100	50	200	0.5	40	400	100	0.7	1000	100	14
BDB01C	BDB02C	80	50	200	0.5	40	400	100	0.7	1000	100	1
MPS6717		80	50	200	0.5	80	—	50	0.5	250	10	1
MPSW06	***MPSW56***	80	50	200	0.5	80	—	50	0.4	250	10	1

Table 2. Plastic–Encapsulated Low–Noise and Good h_{FE} Linearity

These devices are designed to use on applications where good h_{FE} linearity and low–noise characteristics are required: Instrumentation, hi–fi preamplifier.

NPN	PNP	$V_{(BR)CEO}$ Volts	h_{FE} @ I_C Min	Max	mA	V_T(4) mV Typ	NF(5) dB Max	f_T MHz Typ	Style
Case 29–04 — TO–226AA (TO–92)									
—	***2N5087***	50	250	800	0.1	—	2.0	40(2)	1
—	2N5086	50	150	500	0.1	—	3.0	40(2)	1
MPS6428	—	50	250	650	0.1	7.0(7)	3.5(8)	100(2)	1
BC239	—	45	120	800	2.0	9.5	2.0(1)	280	17
BC550B	BC560B	45	180	450	2.0	—	2.5	250	17
BC550C	BC560C	45	380	800	2.0	—	2.5	250	17
MPSA18	—	45	500	—	1.0	6.5(1)	—	160	1
MPS3904	MPS3906	40	100	300	10	—	5.0	200(2)	1
—	MPS4250	40	250	—	10	—	2.0	—	1
BC549B	BC559B	30	200	450	2.0	—	2.5	250	17
BC549C	BC559C	30	380	800	2.0	—	2.5	250	17
2N5088	—	30	350	—	1.0	—	3.0	50	1
2N5089(6)	—	25	450	—	1.0	—	2.0	50	1
MPS6521	MPS6523	25	300	600	2.0	—	3.0	—	1

(1) Typical
(2) Min
(4) V_T: Total Input Noise Voltage (see BC413/BC414 and BC415/BC416 Data Sheets) at R_S = 2.0 kΩ, I_C = 200 µA, V_{CE} = 5.0 Volts.
(5) N_F: Noise Figure at R_S = 2.0 kΩ, I_C = 200 µA, V_{CE} = 5.0 Volts. f = 30 Hz to 15 kHz.
(7) R_S = 10 kΩ, BW = 1.0 Hz, f = 100 MHz
(8) R_S = 500 Ω, BW = 1.0 Hz, f = 10 MHz

Devices listed in bold, italic are Motorola preferred devices.

Plastic–Encapsulated Transistors (continued)

Table 3. Plastic–Encapsulated Darlington Transistors

Darlington amplifiers are cascade transistors used in applications requiring very high–gain and input impedance. These devices have monolithic construction.

NPN	PNP	$V_{(BR)CEO}$ Volts	I_C Max	h_{FE} @ I_C Min	Max	mA	$V_{CE(sat)}$ @ I_C & I_B Volts Max	mA	mA	f_T @ I_C Min	mA	Style
Case 29–05 — TO–226AE (1–WATT TO–92)												
MPSW45A	—	50	1000	25K	150K	200	1.5	1000	2.0	100	200	1
—	***MPSW64***	30	1000	20K	—	100	1.5	100	0.1	125	10	1
Case 29–04 — TO–226AA (TO–92)												
MPSA29	—	100	500	10K	—	100	1.5	100	0.1	125	10	1
BC373	—	80	1000	10K	160K	100	1.1	250	0.25	100	100	1
MPSA27	MPSA77	60	500	10K	—	100	1.5	100	0.1	—	—	1
BC618	—	55	1000	10K	50K	200	1.1	200	0.2	150	500	17
—	MPSA75	40	500	10K	—	100	1.5	100	0.1	—	—	1
2N6427	—	40	500	20K	200K	100	1.5	500	0.5	—	—	1
2N6426	—	40	500	30K	300K	100	1.5	500	0.5	125	10	1
MPSA14	***MPSA64***	30	500	20K	—	100	1.5	100	0.1	125	10	1
MPSA13	MPSA63	30	500	10K	—	100	1.5	100	0.1	125	10	1
BC517	—	30	1000	30K	—	20	1.0	100	0.1	200(1)	10	17

Table 4. Plastic–Encapsulated High–Current Transistors

The following table is a listing of devices that are capable of handling a higher current range for small–signal transistors.

NPN	PNP	$V_{(BR)CEO}$ Volts Min	f_T @ I_C MHz Min	mA	I_C mA Max	h_{FE} @ I_C Min	Max	mA	$V_{CE(sat)}$ @ I_C & I_B Volts Max	mA	mA	Style
Case 29–05 — TO–226AE (1–WATT TO–92)												
MPS6715	MPS6727	40	—	—	1000	50	—	1000	0.5	1000	100	1
MPSW01A	***MPSW51A***	40	50	50	1000	50	—	1000	0.5/0.7	1000	100	1
Case 29–04 — TO–226AA (TO–92)												
BC489	BC490	80	200/150(1)	50	1000	60	400	100	0.3/0.5	1000	100	17
BC639	BC640	80	60	10	500	40	160	150	0.5	500	50	14
MPS651	***MPS751***	60	75	50	2000	75	—	1000	0.5	2000	200	1
MPS650	MPS750	40	75	50	2000	75	—	1000	0.5	2000	200	1
BC368	BC369	20	65	10	1000	60	—	1000	0.5	1000	100	1

(1) Typical

Devices listed in bold, italic are Motorola preferred devices.

Table 5. Plastic–Encapsulated High–Voltage Amplifier Transistors

These high–voltage transistors are designed for driving neon bulbs and indicator tubes, for direct line operation, and for other applications requiring high–voltage capability at relatively low collector current. These devices are listed in order of decreasing breakdown voltage ($V_{(BR)CEO}$).

Device Type	$V_{(BR)CEO}$ Volts Min	I_C Amp Max	h_{FE} @ I_C Min	mA	$V_{CE(sat)}$ @ I_C & I_B Volts Max	mA	mA	f_T @ I_C MHz Min	mA	Style
Case 29–05 — TO–226AE (1–WATT TO–92) — NPN										
BDC05	300	0.5	40	25	2.0	20	2.0	60	10	14
MPSW42	300	0.5	40	30	0.5	20	2.0	50	10	1
Case 29–05 — TO–226AE (1–WATT TO–92) — PNP										
MPSW92	300	0.5	25	30	0.5	20	2.0	50	10	1
Case 29–04 — TO–226AA (TO–92) — NPN										
BF844	400	0.3	50	10	0.5	10	1.0	—	—	1
MPSA44	400	0.3	40	100	0.75	50	5.0	—	—	1
2N6517	350	0.5	30	30	0.3	10	1.0	40	10	1
BF393	300	0.5	40	10	0.2	20	2.0	50	10	1
MPSA42	300	0.5	40	10	0.5	20	2.0	50	10	1
2N5551	160	0.6	80	10	0.15	10	1.0	100	10	1
Case 29–04 — TO–226AA (TO–92) — PNP										
BF493S	350	0.5	40	10	20	20	2.0	50	10	1
2N6520	350	0.5	30	30	0.3	10	1.0	40	10	1
MPSA92	300	0.5	40	10	0.5	20	2.0	50	10	1
2N6519	300	0.5	45	30	0.3	10	1.0	40	10	1
2N5401	150	0.6	60	10	0.2	10	1.0	100	10	1

Case 29–04 — TO–226AA (TO–92)

NPN	PNP	$V_{(BR)CEO}$ Volts Min	I_C Amp Cont	h_{FE} @ I_C Min	mA	$V_{CE(sat)}$ @ I_C & I_B Volts Max	mA	mA	f_T @ I_C MHz Min	mA	Style
BF420	BF421	300	0.5	50	25	2.0	20	2.0	60	10	14
BF422	BF423	250	0.5	50	25	2.0	20	2.0	60	10	14

Devices listed in bold, italic are Motorola preferred devices.

Plastic–Encapsulated Transistors (continued)

Table 6. Plastic–Encapsulated RF Transistors

The RF transistors are designed for small–signal amplification from RF to VHF/UHF frequencies. They are also used as mixers and oscillators in the same frequency ranges.

Device Type	$V_{(BR)CEO}$ Volts Min	I_C mA Max	h_{FE} @ I_C Min	mA	V_{CE} V	f_T MHz Typ	CRE/CRB pF Max	NF dB Typ	f MHz	Style
Case 29–04 — TO–226AA (TO–92) — NPN										
BF224	30	50	30	7.0	10	600	0.28	2.5	100	21
MPSH24	30	50	30	8.0	10	400(2)	0.36	—	—	2
MPSH20	30	100	25	4.0	10	400(2)	0.65	—	—	2
MPSH07A(9)	30	25	20	3.0	10	400(2)	0.3	3.2(3)	100	1
MPS3866	30	400	10	50	5.0	500(2)	—	—	—	1
MPSH11	25	—	60	4.0	10	650(2)	0.9	—	—	2
MPSH10	25	—	60	4.0	10	650(2)	0.65	—	—	2
BF199	25	100	40	7.0	10	750	0.35	2.5	35	21
BF959	20	100	40	20	10	600(2)	0.65	3.0	200	21
MPSH17	15	—	25	5.0	10	800(2)	0.9	6.0(3)	200	2
MPS918	15	50	20	8.0	10	600(2)	1.7	6.0(3)	60	1
MPS5179	12	50	25	3.0	1.0	2000(3)	—	5.0(3)	200	1
MPS3563	12	50	20	8.0	10	800	1.7	6.0(3)	60	1
MPS6595	12	50	25	10	5.0	1200(2)	1.3	—	—	1
Case 29–04 — TO–266AA (TO–92) — PNP										
MPSH81	20	50	60	5.0	10	600(2)	0.85	—	—	2
MPSH69	15	50	30	10	10	2000(2)	0.3	—	—	1

Table 7. Plastic–Encapsulated High–Speed Saturated Switching Transistors

Device Type	t_{on} & t_{off} @ I_C ns Max	ns Max	mA	$V_{(BR)CEO}$ Volts Min	h_{FE} @ I_C Min	mA	$V_{CE(sat)}$ @ I_C & I_B Volts Max	mA	mA	f_T @ I_C MHz Min	mA	Style
Case 29–04 — TO–226AA (TO–92) — NPN												
2N4264	25	35	10	15	40	10	0.22	10	1.0	300	10	1
2N4265	25	35	10	12	100	10	0.22	10	1.0	300	10	1
MPS3646	18	28	300	15	30	30	0.2	30	3.0	350	30	1
MPS2369A	12	18	10	15	40	10	0.2	10	1.0	—	—	1
Case 29–04 — TO–226AA (TO–92) — PNP												
MPS4258	15	20	10	12	30	50	0.15	10	1.0	700	10	1

(2) Min
(3) Max
(9) AGC Capable

Devices listed in bold, italic are Motorola preferred devices.

Plastic–Encapsulated Transistors (continued)

Table 8. Plastic–Encapsulated Choppers

Devices are listed in decreasing $V_{(BR)EBO}$.

Device Type	$V_{(BR)EBO}$ Volts Min	I_C Amp(1) Max	h_{FE} @ I_C Min	mA	$V_{CE(sat)}$ @ I_C & I_B Volts Max	mA	mA	f_T @ I_C MHz Min	mA	Style
Case 29–04 — TO–226AA (TO–92) — NPN										
MPSA17	15	100	200	5.0	0.25	10	1.0	80	5.0	1
MPSA16	12	100	200	5.0	0.25	10	1.0	100	5.0	1
Case 29–04 — TO–266AA (TO–92) — PNP										
MPS404A	–25	–150	30	–12	–0.2	–24	1.0	—	—	1

Table 9. Plastic–Encapsulated Telecom Transistors

These devices are special product ranges intended for use in telecom applications.

Device Type	$V_{(BR)CEO}$ Volts	P_D mW 25°C Amb	I_C mA Cont	h_{FE} @ I_C @ V_{CE} Min	Max	mA	Volts	f_T MHz Min	Style
Case 29–04 — TO–226AA (TO–92) — NPN									
P2N2222A	40	625	600	75	—	10	10	300	17
PBF259,S(10)	300	625	500	25	—	1.0	10	40	1
Case 29–04 — TO–226AA (TO–92) — PNP									
P2N2907A	60	625	600	100	—	10	10	200	17
PBF493,S(11)	300	625	500	40	—	1.0	10	40	1

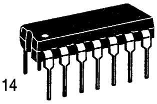
(1) Typical
(10) "S" version, h_{FE} Min 60 @ I_C = 20 mA, V_{CE} = 10 V.
(11) "S" version, h_{FE} Min 40 @ I_C = 0.1 mA, V_{CE} = 1.0 V.

Devices listed in bold, italic are Motorola preferred devices.

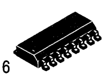
Plastic–Encapsulated Multiple Transistors

The manufacturing trend has been toward printed circuit board design with requirements for smaller packages with more functions. In the case of discrete components the use of the multiple device package helps to reduce board space requirements and assembly costs.

Many of the most popular devices are offered in the standard plastic DIP and surface mount IC packages. This includes small–signal NPN and PNP bipolar transistors, N–channel and P–channel FETs, as well as diode arrays.



14
1
CASE 646–06
(TO–116)
STYLE 1



16
1

CASE 751B–05
SO–16
STYLE 4

Specification Tables

The following short form specifications include Quad and Dual transistors listed in alphanumeric order. Some columns denote two different types of data indicated by either **bold** or *italic* typeface. See key and headings for proper identification. This applies to Table 10 and 11 of this section only.

KEY

TYPE NO.	ID	Ref. Point P_D Watts One Die Only	Subscript V_{CE} Volts	I_C Amp Max	Unit h_{FE} Min @ I_C	f_T MHz Min	C_{ob} pF Max	h_{FE1}/h_{FE2} — *t_{on} ns Max*	ΔV_{BE} mV Max — *t_{off} ns Max*	G_p dB Min — *$V_{CE(sat)}$ Volts Max*	NF dB Max — *I_C/I_B*	@ f — & I_C Unit

Alphanumeric listing type numbers

Identification Code

First Letter: Polarity
C — both types in multiple device
N — NPN
P — PNP
Second Letter: Use
A — General Purpose Amplifier
E — Low Noise Audio Amplifier
F — Low Noise RF Amplifier
G — General Purpose Amplifier and Switch
H — Tuned RF/IF Amplifier
M — Differential Amplifier
S — High Speed Switch
D — Darlington

Common–emitter DC Current Gain.

Units for test Current:
A — ampere
m — mA
u — µA

Current–Gain–Bandwidth Product

Continuous (DC) Collector Current

G_p — Power Gain
NF — Noise Figure
f — Test Frequency
AUD — 10–15 kHz
Frequency Units:
H — Hertz M — MHz
K — kHz G — GHz

$V_{CE(sat)}$ — Collector–Emitter Saturation Voltage
IC — Test Current
Current Units: u — µA
m — mA
A — Amp

h_{FE1}/h_{FE2} — Current Gain Ratio
V_{BE} — Differential Base Voltage $|V_{BE1} - V_{BE2}|$.
Differential Amplifiers
t_{on} — turn–on time
t_{off} — turn–off time

Power Dissipation specified at 25°C. Single die rating.
Ref. Point: A — Ambient Temperature
C — Case Temperature

Rated Minimum Collector–Emitter Voltage
Subscript letter identifies base termination listed below in order of preference.
SUBSCRIPT:
0 — V_{CEO}, open

Output Capacitance, common–base. Shown without distinction:
C_{cb} — Collector–Base Capacitance
C_{re} — Common–Emitter Reverse Transfer Capacitance

Plastic–Encapsulated Multiple Transistors (continued)

Table 10. Plastic–Encapsulated Multiple Transistors — Quad

The following table is a listing of the most popular multiple devices available in the plastic DIP package. These devices are available in NPN, PNP, and NPN/PNP configurations. (See note.)

Device	ID	P_D Watts One Die Only	V_{CEO} Volts	I_C Amp Max	h_{FE} Min	@ I_C	f_T MHz Min	C_{ob} pF Max	h_{FE1}/h_{FE2} / *t_{on} ns Max*	ΔV_{BE} mV Max / t_{off} ns Max	G_p dB Min / $V_{CE(sat)}$ Volts Max	**NF dB Max Typ(1)** / @ I_C/I_B	@ f / I_C
Case 646–06 — TO–116													
MPQ2222A	**NA**	0.65	40	0.5	100	150 m	200	8.0	35(1)	285(1)	0.3	10	150 m
MPQ2369	**NS**	0.5	15	0.5	40	10 m	450	4.0	9.0(1)	15(1)	0.25	10	10 m
MPQ2483	**NA**	0.625	40	0.05	150	1.0 m	50					**3.0(1)**	**AUD**
MPQ2484	**NA**	0.625	40	0.05	300	1.0 m	50					**2.0(1)**	**AUD**
MPQ2907A	**PA**	0.65	60	0.6	100	150 m	200	8.0	45(1)	180(1)	0.4	10	150 m
MPQ3467	**PS**	0.75	40	1.0	20	500 m	125	25	40	90	0.5	10	500 m
MPQ3725	**NS**	1.0	40	1.0	25	500 m	250	10	35	60	0.45	10	500 m
MPQ3762	**PS**	0.75	40	1.5	35	150 m	150	15	50	120	0.55	10	500 m
MPQ3798	**PA**	0.625	40	0.05	150	0.1 m	60	4.0				**3.0(1)**	**AUD**
MPQ3799	**PA**	0.625	60	0.05	300	0.1 m	60	4.0				**2.0(1)**	**AUD**
MPQ3904	**NG**	0.5	40	0.2	75	10 m	250	4.0	37(1)	136(1)	0.2	10	10 m
MPQ3906	**PG**	0.5	40	0.2	75	10 m	200	4.5	43(1)	155(1)	0.25	10	10 m
MPQ6001	**CG**	0.65	30	0.5	40	150 m	200	8.0	30(1)	225(1)	0.4	10	150 m
MPQ6002	**CG**	0.65	30	0.5	100	150 m	200	8.0	30(1)	225(1)	0.4	10	150 m
MPQ6100A	**CA**	0.5	45	0.05	150	1.0 m	50	4.0				**4.0(1)**	**AUD**
MPQ6426	**ND**	0.5	30	0.5	10K	100 m	125	8.0	—	—	1.5	10	100 m
MPQ6501	**CG**	0.65	30	0.5	40	150 m	200	8.0	30(1)	225(1)	0.4	10	150 m
MPQ6502	**CG**	0.65	30	0.5	100	150 m	200	8.0	30(1)	225(1)	0.4	10	150 m
MPQ6600A1	**CA**	0.5	45	0.05	150	1.0 m	50	4.0	0.8	20	0.25	10	1.0 m
MPQ6700	**CA**	0.5	40	0.2	70	10 m	200	4.5			0.25	10	1.0 m
MPQ6842	**CA**	0.75	40	0.5	70	10 m	300	4.5	45	150	0.15	10	0.5 m
MPQ7043	**NA**	0.75	250	0.5	25	1.0 m	50	5.0			0.5	10	20 m
MPQ7042	**NA**	0.75	200	0.5	25	1.0 m	50	5.0			0.5	10	20 m
MPQ7051	**CG**	0.75	150	0.5	25	1.0 m	50	6.0			0.7	10	20 m
MPQ7093	**PA**	0.75	250	0.5	25	1.0 m	50	5.0			0.5	10	20 m

Table 11. Plastic–Encapsulated Multiple Transistors — Quad Surface Mount

The following table is a listing of the most popular multiple devices available in the plastic SOIC surface mount package. These devices are available in NPN, PNP, and NPN/PNP configurations.

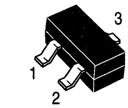
Device	$V_{(BR)CEO}$	$V_{(BR)CBO}$	h_{FE} @ I_C Min	h_{FE} @ I_C mA	f_T @ I_C MHz Min	f_T @ I_C mA
Case 751B–05 — SO–16						
MMPQ2222A	40	75	40	500	200	20
MMPQ2369	15	40	20	100	450	10
MMPQ2907A	50	60	50	500	200	50
MMPQ3467	40	40	20	500	125	50
MMPQ3725	40	60	25	500	250	50
MMPQ3799	60	60	300	0.5	60	1.0
MMPQ3904	40	60	75	10	250	10
MMPQ3906	40	40	75	10	200	10
MMPQ6700(12)	40	40	70	10	200	10

(1) Typical
(12) NPN/PNP
NOTE: Some columns show 2 different types of data indicated by either **bold** or *italic* typefaces. See key and headings.

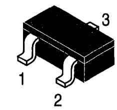
Devices listed in bold, italic are Motorola preferred devices.

Plastic–Encapsulated Surface Mount Transistors

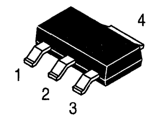
This section of the selector guide lists the small–signal plastic devices that are available for surface mount applications. These devices are encapsulated with the latest state–of–the–art mold compounds that enhance reliability and exhibit excellent performance in high temperature and high humidity environments. This package offers higher power dissipation capability for small–signal applications.



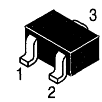
CASE 318–08
TO–236AB
SOT–23



CASE 318D–03
SC–59



CASE 318E–04
SOT–223



CASE 419–02
SC–70/SOT–323

Table 12. Plastic–Encapsulated Surface Mount General–Purpose Transistors

The following tables are a listing of small–signal general–purpose transistors in the SOT–23 and SC–59 surface mount packages. These devices are intended for small–signal amplification for DC, audio, and lower RF frequencies. They also have applications as oscillators and general–purpose, low voltage switches.

Pinout: 1–Base, 2–Emitter, 3–Collector

Devices are listed in order of descending breakdown voltage.

Device	Marking	$V_{(BR)CEO}$	h_{FE} @ I_C			f_T
			Min	Max	mA	MHz Min
Case 318–08 — TO–236AB (SOT–23) — NPN						
BC846ALT1	1A	65	110	220	2.0	100
BC846BLT1	1B	65	200	450	2.0	100
BC817–16LT1	6A	45	100	250	100	200
BC817–25LT1	6B	45	160	400	100	200
BC817–40LT1	6C	45	250	600	100	200
BC847ALT1	1E	45	110	220	2.0	100
BC847BLT1	1F	45	200	450	2.0	100
BC847CLT1	1G	45	420	800	2.0	100
MMBT2222ALT1	1P	40	100	300	150	200
MMBT3904LT1	1AM	40	100	300	10	200
MMBT4401LT1	2X	40	100	300	150	250
BC848ALT1	1J	30	110	220	2.0	100
BC848BLT1	1K	30	200	450	2.0	100
BC848CLT1	1L	30	420	800	2.0	100
Case 318–08 — TO–236AB (SOT–23) — PNP						
MMBT8599LT1	2W	80	100	300	1.0	150
BC856ALT1	3A	65	125	250	2.0	100
BC856BLT1	3B	65	220	475	2.0	100
MMBT2907ALT1	2F	60	100	300	150	200
BC807–16LT1	5A	45	100	250	100	200

Devices listed in bold, italic are Motorola preferred devices.

Plastic–Encapsulated Surface Mount Transistors (continued)

Table 12. Plastic–Encapsulated Surface Mount General–Purpose Transistors (continued)
Pinout: 1–Base, 2–Emitter, 3–Collector
Devices are listed in order of descending breakdown voltage.

Device	Marking	$V_{(BR)CEO}$	h_{FE} @ I_C Min	Max	mA	f_T MHz Min
Case 318–08 — TO–236AB (SOT–23) — PNP						
BC807–25LT1	5B	45	160	400	100	200
BC807–40LT1	5C	45	250	600	100	200
BC857ALT1	3E	45	125	250	2.0	100
BC857BLT1	3F	45	220	475	2.0	100
MMBT3906LT1	2A	40	100	300	10	250
MMBT4403LT1	2T	40	100	300	150	200
BC858ALT1	3J	30	125	250	2.0	100
BC858BLT1	3K	30	220	475	2.0	100
BC858CLT1	3L	30	420	800	2.0	100
Case 318D–03 — SC–59 — NPN						
MSD601–RT1	YR	25	210	340	2.0	150(1)
MSD601–ST1	YS	25	290	460	2.0	150(1)
MSD602–RT1	WR	25	120	240	150	200(1)
MSD1328–RT1	1DR	20	200	350	500	200(1)
Case 318D–03 — SC–59 — PNP						
MSB709–RT1	AR	25	210	340	2.0	100(1)
MSB709–ST1	AS	25	290	460	2.0	100(1)
MSB710–QT1	CQ	25	85	170	150	200(1)
MSB710–RT1	CR	25	120	240	150	200(1)
Case 419–02 — SC–70/SOT–323 —NPN						
BC846AWT1	1A	65	110	220	2.0	100
BC846BWT1	1B	65	200	450	2.0	100
BC847AWT1	1E	45	110	220	2.0	100
BC847BWT1	1F	45	200	450	2.0	100
BC847CWT1	1G	45	420	800	2.0	100
BC848AWT1	1J	30	110	220	2.0	100
BC848BWT1	1K	30	200	450	2.0	100
BC848CWT1	1L	30	420	800	2.0	100
MMBT3904WT1	AM	40	100	300	10	300
MSC3930–BT1	VB	20	70	140	1.0	150
MSD1819A–RT1	ZR	50	210	340	2.0	—
Case 419–02 — SC–70/SOT–323 —PNP						
BC856AWT1	3A	65	125	250	2.0	100
BC856BWT1	3B	65	220	475	2.0	100
BC857AWT1	3E	45	125	250	2.0	100
BC857BWT1	3F	45	220	475	2.0	100
BC858AWT1	3J	30	110	220	2.0	100
BC858BWT1	3K	30	200	450	2.0	100
BC858CWT1	3L	30	420	800	2.0	100
MMBT3906WT1	2A	40	100	300	10	250
MSB1218A–RT1	BR	45	210	340	2.0	—

(1) Typical

Devices listed in bold, italic are Motorola preferred devices.

Plastic–Encapsulated Surface Mount Transistors (continued)

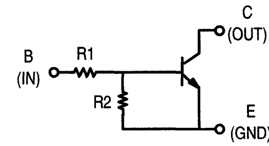


Table 13. Plastic–Encapsulated Surface Mount Bias Resistor Transistors for General Purpose Applications

Pinout: 1–Base, 2–Emitter, 3–Collector

These devices include bias resistors on the semiconductor chip with the transistor. See the BRT diagram for orientation of resistors.

Device		Marking		$V_{(BR)CEO}$ Volts (Min)	h_{FE} @ I_C		I_C mA Max	R_1 Ohm	R_2 Ohm
NPN	PNP	NPN	PNP		Min	mA			
Case 318D–03 — SC–59									
MUN2211T1	***MUN2111T1***	8A	6A	50	35	5.0	100	10K	10K
MUN2212T1	***MUN2112T1***	8B	6B	50	60	5.0	100	22K	22K
MUN2213T1	***MUN2113T1***	8C	6C	50	80	5.0	100	47K	47K
MUN2214T1	***MUN2114T1***	8D	6D	50	80	5.0	100	10K	47K
MUN2215T1	***MUN2115T1***	8E	6E	50	160	5.0	100	10K	∞
MUN2216T1	***MUN2116T1***	8F	6F	50	160	5.0	100	4.7K	∞
MUN2230T1	***MUN2130T1***	8G	6G	50	3.0	5.0	100	1.0K	1.0K
MUN2231T1	***MUN2131T1***	8H	6H	50	8.0	5.0	100	2.2K	2.2K
MUN2232T1	***MUN2132T1***	8J	6J	50	15	5.0	100	4.7K	4.7K
MUN2233T1	***MUN2133T1***	8K	6K	50	80	5.0	100	4.7K	47K
MUN2234T1	***MUN2134T1***	8L	6L	50	80	5.0	100	22K	47K
Case 318–08 — TO–236AB (SOT–23)									
MMUN2211LT1	***MMUN2111LT1***	A8A	A6A	50	35	5.0	100	10K	10K
MMUN2212LT1	***MMUN2112LT1***	A8B	A6B	50	60	5.0	100	22K	22K
MMUN2213LT1	***MMUN2113LT1***	A8C	A6C	50	80	5.0	100	47K	47K
MMUN2214LT1	***MMUN2114LT1***	A8D	A6D	50	80	5.0	100	10K	47K
MMUN2215LT1	***MMUN2115LT1***	A8E	A6E	50	160	5.0	100	10K	∞
MMUN2216LT1	***MMUN2116LT1***	A8F	A6F	50	160	5.0	100	4.7K	∞
MMUN2230LT1	***MMUN2130LT1***	A8G	A6G	50	3.0	5.0	100	1.0K	1.0K
MMUN2231LT1	***MMUN2131LT1***	A8H	A6H	50	8.0	5.0	100	2.2K	2.2K
MMUN2232LT1	***MMUN2132LT1***	A8J	A6J	50	15	5.0	100	4.7K	4.7K
MMUN2233LT1	***MMUN2133LT1***	A8K	A6K	50	80	5.0	100	4.7K	47K
MMUN2234LT1	***MMUN2134LT1***	A8L	A6L	50	80	5.0	100	22K	47K
Case 419–02 — SC–70/SOT–323									
MUN5211T1	***MUN5111T1***	8A	6A	50	35	5.0	50	10K	10K
MUN5212T1	***MUN5112T1***	8B	6B	50	60	5.0	50	22K	22K
MUN5213T1	***MUN5113T1***	8C	6C	50	80	5.0	50	47K	47K
MUN5214T1	***MUN5114T1***	8D	6D	50	80	5.0	50	10K	47K
MUN5215T1	***MUN5115T1***	8E	6E	50	160	5.0	50	10K	∞
MUN5216T1	***MUN5116T1***	8F	6F	50	160	5.0	50	4.7K	∞
MUN5230T1	***MUN5130T1***	8G	6G	50	3.0	5.0	50	1.0K	1.0K
MUN5231T1	***MUN5131T1***	8H	6H	50	8.0	5.0	50	2.2K	2.2K
MUN5232T1	***MUN5132T1***	8J	6J	50	15	5.0	50	4.7K	4.7K
MUN5233T1	***MUN5133T1***	8K	6K	50	80	5.0	50	4.7K	47K
MUN5234T1	***MUN5134T1***	8L	6L	50	80	5.0	50	22K	47K

Devices listed in bold, italic are Motorola preferred devices.

Plastic–Encapsulated Surface Mount Transistors (continued)

Table 14. Plastic–Encapsulated Surface Mount Switching Transistors

The following tables are a listing of devices intended for high–speed, low saturation voltage, switching applications. These devices have very fast switching times and low output capacitance for optimized switching performance.

Pinout: 1–Base, 2–Emitter, 3–Collector

Device	Marking	Switching Time (ns)		$V_{(BR)CEO}$	h_{FE} @ I_C			f_T MHz Min
		t_{on}	t_{off}		Min	Max	mA	
Case 318–08 — TO-236AB (SOT–23) — NPN								
MMBT2369LT1	M1J	12	18	15	20	—	100	—
MMBT2369ALT1	1JA	12	18	15	20	—	100	—
BSV52LT1	B2	12	18	12	40	120	10	400
Case 318–08 — TO-236AB (SOT–23) — PNP								
MMBT3640LT1	2J	25	35	12	20	—	50	500
Pinout: 1–Emitter, 2–Base, 3–Collector								
Case 318D–03 — SC–59 — NPN								
MSC1621T1	RB	20	40	20	40	180	1.0	200

Table 15. Plastic–Encapsulated Surface Mount VHF/UHF Amplifiers, Mixers, Oscillators

The following table is a listing of devices intended for small–signal RF amplifier applications to VHF/UHF frequencies. These devices may also be used as VHF/UHF oscillators and mixers.

Pinout: 1–Base, 2–Emitter, 3–Collector

Device	Marking	$V_{(BR)CEO}$	C_{cb}(13) pF Max	f_T @ I_C	
				GHz Min	mA
Case 318–08 — TO-236AB (SOT–23) — NPN					
MMBTH10LT1	3EM	25	0.7	0.65	4.0
MMBT918LT1	M3B	15	1.7(14)	0.6	4.0
MMBTH24LT1	M3A	30	0.45	0.4	8.0
Case 318–08 — TO-236AB (SOT–23) — PNP					
MMBTH81LT1	3D	20	0.85	0.6	5.0
MMBTH69LT1	M3J	15	0.35(13)	2.0	10
Pinout: 1–Emitter, 2–Base, 3–Collector					
Case 318D–03 — SC–59 — NPN					
MSC2295–BT1	VB	20	1.5(13)	0.15	1.0
MSC2295–CT1	VC	20	1.5(13)	0.15	1.0
MSC2404–CT1	UC	20	1.0(13)	0.45	1.0
MSC3130T1	1S	10	—	1.4	5.0
Case 318D–03 — SC–59 — PNP					
MSA1022–BT1	EB	20	2.0(13)	0.15	1.0
MSA1022–CT1	EC	20	2.0(13)	0.15	1.0
Case 419–02 — SC–70/SOT–323 — PNP					
MSB81T1	J3D	20	0.85(13)	0.6	5.0

(13) C_{re}
(14) C_{ob}

Devices listed in bold, italic are Motorola preferred devices.

Table 16. Plastic–Encapsulated Surface Mount Choppers

The following table is a listing of small–signal devices intended for chopper applications where a higher than normal $V_{(BR)CEO}$ is required in the circuit application.

Pinout: 1–Base, 2–Emitter, 3–Collector

Device	Marking	$V_{(BR)CEO}$	$V_{(BR)EBO}$	h_{FE} @ I_C Min	Max	mA
Case 318–08 — TO–236AB (SOT–23) — PNP						
MMBT404ALT1	2N	35	25	30	400	12

Table 17. Plastic–Encapsulated Surface Mount Darlingtons

The following table is a listing of small–signal devices that have very high h_{FE} and input impedance characteristics. These devices utilize monolithic, cascade transistor construction.

Pinout: 1–Base, 2–Emitter, 3–Collector

Devices are listed in order of descending h_{FE}.

Device	Marking	$V_{(BR)CES}$	$V_{CE(sat)}$ Volts Max	h_{FE} @ I_C Min	Max	mA
Case 318–08 — TO–236AB (SOT–23) — NPN						
MMBTA14LT1	1N	30	1.5	20K	—	100
MMBTA13LT1	1M	30	1.5	10K	—	100
Case 318–08 — TO–236AB (SOT–23) — PNP						
MMBTA64LT1	2V	30	1.5	20K	—	100

Table 18. Plastic–Encapsulated Surface Mount Low–Noise Transistors

The following table is a listing of small–signal devices intended for low noise applications in the audio range. These devices exhibit good linearity and are candidates for hi–fi and instrumentation equipment.

Pinout: 1–Base, 2–Emitter, 3–Collector

Devices are listed in order of ascending NF.

Device	Marking	NF dB Typ	$V_{(BR)CEO}$	h_{FE}@ I_C Min	Max	mA	f_T MHz Min
Case 318–08 — TO–236AB (SOT–23) — NPN							
MMBT5089LT1	1R	2.0(15)	25	400	—	10	50
MMBT2484LT1	1U	3.0(15)	60	—	800	10	—
MMBT6428LT1	1KM	3.0	50	250	—	10	100
MMBT6429LT1	1L	3.0	45	500	—	10	100
Case 318–08 — TO–236AB (SOT–23) — PNP							
MMBT5087LT1	2Q	2.0(15)	50	250	—	10	40

(15) Max

Devices listed in bold, italic are Motorola preferred devices.

Plastic–Encapsulated Surface Mount Transistors (continued)

Table 19. Plastic–Encapsulated Surface Mount High–Voltage Transistors

The following table is a listing of small–signal high–voltage devices designed for direct line operation requiring high voltage breakdown and relatively low current capability.

Pinout: 1–Base, 2–Emitter, 3–Collector

Devices are listed in order of descending breakdown voltage.

Device	Marking	$V_{(BR)CEO}$	h_{FE} @ I_C Min	Max	mA	f_T MHz Min
Case 318–08 — TO–236AB (SOT–23) — NPN						
MMBT6517LT1	1Z	350	15	—	100	40
MMBTA42LT1	1D	300	40	—	30	50
MMBT5551LT1	G1	160	30	—	50	100
Case 318–08 — TO–236AB (SOT–23) — PNP						
MMBT6520LT1	2Z	350	15	—	100	40
MMBTA92LT1	2D	300	25	—	30	50
MMBT5401LT1	2L	150	50	—	50	100

Table 20. Plastic–Encapsulated Surface Mount Drivers

The following is a listing of small–signal devices intended for medium voltage driver applications at fairly high current levels.

Pinout: 1–Base, 2–Emitter, 3–Collector

Device	Marking	$V_{(BR)CEO}$	$V_{CE(sat)}$	$V_{BE(sat)}$	h_{FE} @ I_C Min	Max	mA
Case 318–08 — TO–236AB (SOT–23) — NPN							
MMBTA06LT1	1GM	80	0.25	—	100	—	100
BSS64LT1	AM	80	0.15	—	20	—	10
Case 318–08 — TO–236AB (SOT–23) — PNP							
BSS63LT1	T1	100	−0.25	−0.90	30	—	25
MMBTA56LT1	2GM	80	−0.25	—	100	—	100
The following devices are designed to conserve energy. They offer ultra–low collector saturation voltage.							
Case 318–08 — TO–236AB (SOT–23) — PNP							
MMBT1010LT1	GLP	15	0.1	1.1	300	600	100
Case 318–03 — SC–59 — PNP							
MSD1010T1	GLP	15	0.1	1.1	300	600	100

Table 21. Plastic–Encapsulated Surface Mount General Purpose Amplifiers

Pinout: 1–Base, 2–Collector, 3–Emitter, 4–Collector

Device	Marking	$V_{(BR)CEO}$	h_{FE} @ I_C Min	Max	mA
Case 318E–04 — SOT–223 — NPN					
BCP56T1	BH	80	40	250	150
Case 318E–04 — SOT–223 — PNP					
Pinout: 1–Gate, 2–Drain, 3–Source, 4–Drain					
BCP53T1	AH	80	40	25	150

Devices listed in bold, italic are Motorola preferred devices.

Plastic–Encapsulated Surface Mount Transistors (continued)

Table 22. Plastic–Encapsulated Surface Mount Switching Transistors
Pinout: 1–Base, 2–Collector, 3–Emitter, 4–Collector

Device	Marking	t_{on}	t_{off}	$V_{(BR)CEO}$	h_{FE} Min	h_{FE} Max	f_T @ I_C (mA)	f_T Min (MHz)
Case 318E–04 — SOT–223 — NPN								
PZT2222AT1	P1F	35	285	40	100	300	20	300
Case 318E–04 — SOT–223 — PNP								
PZT2907AT1	P2F	45	100	60	100	300	50	200

Table 23. Plastic–Encapsulated Surface Mount Darlingtons
Pinout: 1–Base, 2–Collector, 3–Emitter, 4–Collector

Device	Marking	$V_{(BR)CER}$	$V_{CE(sat)}$ Max (V)	h_{FE} Min	h_{FE} Max	@ I_C (mA)
Case 318E–04 — SOT–223 — NPN						
BSP52T1	AS3	80	1.3	2000	—	500
PZTA14T1	P1N	30	1.5	20k	—	100
Case 318E–04 — SOT–223 — PNP						
BSP62T1	BS3	90	1.3	2000	—	500
PZTA64T1	P2V	30	1.5	20k	—	100

Table 24. Plastic–Encapsulated Surface Mount High–Voltage Transistors
Pinout: 1–Base, 2–Collector, 3–Emitter, 4–Collector

Device	Marking	$V_{(BR)CEO}$	h_{FE} Min	h_{FE} Max	f_T @ I_C (mA)	f_T Min (MHz)
Case 318E–04 — SOT–223 — NPN						
BSP19AT1	SP19A	350	40	—	20	70
PZTA42T1	P1D	300	40	—	10	50
BF720T1	BF720	250	50	—	10	60
BSP20AT1	SP20A	250	40	—	20	70
Case 318E–04 — SOT–223 — PNP						
PZTA96T1	ZTA96	450	50	150	10	50
PZTA92T1	P2D	300	40	—	10	50
BSP16T1	BSP16	300	30	150	10	15
BF721T1	BF721	250	50	—	10	60

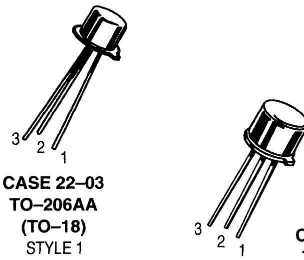
Table 25. Plastic–Encapsulated Surface Mount High Current Transistors
Pinout: 1–Base, 2–Collector, 3–Emitter, 4–Collector

Device	Marking	$V_{(BR)CEO}$	$V_{CE(sat)}$ Volts	h_{FE}@ I_C Min	h_{FE}@ I_C Max	h_{FE}@ I_C mA
Case 318E–04 — SOT–223 — NPN						
PZT651T1	651	60	0.5	75	—	1000
BCP68T1	CA	20	0.5	60	—	1000
Case 318E–04 — SOT–223 — PNP						
PZT751T1	ZT751	60	0.5	75	—	1000
BCP69T1	CE	20	0.5	60	—	1000

Devices listed in bold, italic are Motorola preferred devices.

Metal–Can Transistors

Metal–can packages are intended for use in industrial applications where harsh environmental conditions are encountered. These packages enhance reliability of the end products due to their resistance to varying humidity and extreme temperature ranges.



CASE 22–03
TO–206AA
(TO–18)
STYLE 1

CASE 79–04
TO–205AD
(TO–39)
STYLE 1

Table 26. Metal–Can General–Purpose Transistors

These transistors are designed for DC to VHF amplifier applications, general–purpose switching applications, and complementary circuitry. Devices are listed in decreasing order of $V_{(BR)CEO}$ within each package group.

Device Type	$V_{(BR)CEO}$ Volts Min	f_T @ I_C MHz Min	f_T @ I_C mA	I_C mA Max	h_{FE} @ I_C Min	h_{FE} @ I_C Max	h_{FE} @ I_C mA
Case 22–03 — TO–206AA (TO–18) — NPN							
2N3700	80	80	50	1000	50	—	500
BC107	45	150	10	200	110	450	2.0
BC107B	45	150	10	200	200	450	2.0
2N2222A	40	300	20	800	100	300	150
BC109C	25	150	10	200	420	800	2.0
Case 22–03 — TO–206AA (TO–18) — PNP							
2N2906A	60	200	50	600	40	120	150
2N2907A	60	200	50	600	100	300	150
2N3251A	60	300	10	200	100	300	10
BC177B	45	200	10	200	180	460	2.0
Case 79–04 — TO–205AD (TO–39) — NPN							
2N3019	80	100	50	1000	100	300	150
2N3020	80	80	50	1000	40	120	150
2N1893	80	50	50	500	40	120	150
2N2219A	40	300	20	800	100	300	150
Case 79–04 — TO–205AD (TO–39) — PNP							
2N4033	80	—	—	1000	25	—	1000
2N4036	65	60	50	1000	40	140	150
2N2904A	60	200	50	600	40	120	150
2N2905A	60	200	50	600	100	300	150
2N4032	60	—	—	1000	40	—	1000

Devices listed in bold, italic are Motorola preferred devices.

Metal–Can Transistors (continued)

Table 27. Metal–Can High–Gain/Low–Noise Transistors

These transistors are characterized for high–gain and low–noise applications. Devices are listed in decreasing order of NF.

Device Type	NF Wideband dB Typ Max	$V_{(BR)CEO}$ Volts Min	I_C mA Max	h_{FE} @ I_C Min	Max	µA mA	f_T @ I_C MHz Min	mA
Case 22–03 — TO–206AA (TO–18) — NPN								
2N2484	8.0(1)	60	50	100	500	10	15	0.05
2N930A	3.0	45	30	—	600	10	45	0.5
2N930	3.0	45	30	—	600	10	30	0.5
Case 22–03 — TO–206AA (TO–18) — PNP								
2N3964	4.0	45	200	250	600	1.0(24)	50	0.5
2N3799	2.5	60	50	300	900	500	30	0.5

Table 28. Metal–Can High–Voltage/High–Current Transistors

The following table lists Motorola standard devices that have high collector–emitter breakdown voltage. Devices are listed in decreasing order of $V_{(BR)CEO}$ within each package type.

Device Type	$V_{(BR)CEO}$ Volts Min	I_C mA Max	h_{FE} @ I_C Min	mA	$V_{CE(sat)}$ @ I_C & I_B Volts Max	mA	mA	f_T @ I_C MHz Min	mA
Case 22–03 — TO–206AA (TO–18) — NPN									
2N6431	300	50	50	30	0.5	20	2.0	50	10
BSS73	300	500	40	30	1.0	50	5.0	50	20
Case 22–03 — TO–206AA (TO–18) — PNP									
BSS76	300	500	35	30	0.5	50	5.0	50	20
Case 79–04 — TO–205AD (TO–39) — PNP									
2N3637	175	1000	100	50	0.5	50	5.0	200	30

(1) Typical
(24) $T_A = 25°C$

Table 29. Metal–Can Switching Transistors

The following devices are intended for use in general–purpose switching and amplifier applications. Within each package group shown, the devices are listed in order of decreasing turn–on time (t_{on}).

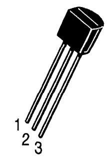
Device Type	t_{on} & t_{off} @ I_C ns Max	ns Max	mA	$V_{(BR)CEO}$ Volts Min	I_C mA Max	h_{FE} @ I_C Min	mA	$V_{CE(sat)}$ @ I_C @ I_B Volts Max	mA	mA	f_T MHz Min	I_C mA
Case 22–03 — TO–206AA (TO–18) — NPN												
2N2369A	12	18	10	15	200	40	10	0.2	10	1.0	500	10
BSX20	7.0	21	100	15	500	20	10	0.25	10	1.0	500	10
Case 79–04 — TO–205AD (TO–39) — PNP												
2N3467	40	90	500	40	1000	40	500	0.5	500	50	175	50

Devices listed in bold, italic are Motorola preferred devices.

Field–Effect Transistors

JFETs

JFETs operate in the depletion mode. They are available in both P– and N–channel and are offered in both Through–hole and Surface Mount packages. Applications include general–purpose amplifiers, switches and choppers, and RF amplifiers and mixers. These devices are economical and very rugged. The drain and source are interchangeable on many typical FETs.



CASE 29–04
TO–226AA
(TO–92)

Table 30. JFET Low–Frequency/Low–Noise

The following table is a listing of small–signal JFETs intended for low–noise applications in the audio range. These devices exhibit good linearity and are candidates for hi–fi and instrumentation equipment.

Device	$R_e\lvert Y_{fs}\rvert$ @ f mmho Min	kHz	$R_e\lvert Y_{os}\rvert$ @ f µmho Max	kHz	C_{iss} pF Max	C_{rss} pF Max	$V_{(BR)GSS}$ $V_{(BR)GDO}$ Volts Min	$V_{GS(off)}$ Volts Min	Max	I_{DSS} mA Min	Max	Style
Case 29–04 — TO–226AA (TO–92) — N–Channel												
J202	—	—	—	—	—	—	40	0.8	4.0	0.9	4.5	5
2N5458	1.5	1.0	50	1.0	7.0	3.0	25	1.0	7.0	2.0	9.0	5
MPF3821	1.5	1.0	10	1.0	6.0	3.0	50	—	4.0	0.5	2.5	5
2N5457	1.0	1.0	50	1.0	7.0	3.0	25	0.5	6.0	1.0	5.0	5
2N5459	2.0	1.0	50	1.0	7.0	3.0	25	2.0	8.0	4.0	16	5
Case 29–04 — TO–226AA (TO–92) — P–Channel												
2N5460	1.0	1.0	75	1.0	7.0	2.0	40	0.75	6.0	1.0	5.0	7
2N5461	1.5	1.0	75	1.0	7.0	2.0	40	1.0	7.5	2.0	9.0	7
2N5462	2.0	1.0	75	1.0	7.0	2.0	40	1.8	9.0	4.0	16	7

Table 31. JFET High–Frequency Amplifiers

The following is a listing of small–signal JFETs that are intended for hi–frequency applications. These are candidates for VHF/UHF oscillators, mixers and front–end amplifiers.

Device	$R_e\lvert Y_{fs}\rvert$ @ f mmho Min	MHz	$R_e\lvert Y_{os}\rvert$ @ f µmho Max	MHz	C_{iss} pF Max	C_{rss} pF Max	NF @ R_G = 1K dB Max	f MHz	$V_{(BR)GSS}$ $V_{(BR)GDO}$ Volts Min	$V_{GS(off)}$ Volts Min	Max	I_{DSS} mA Min	Max	Style
Case 29–04 — TO–226AA (TO–92) — N–Channel														
MPF102	1.6	100	200	100	7.0	3.0	—	—	25	—	8.0	2.0	20	5
2N5668	1.0	100	50	100	7.0	3.0	2.5	100	25	0.2	4.0	1.0	5.0	5
2N5484	2.5	100	75	100	5.0	1.0	3.0	100	25	0.3	3.0	1.0	5.0	5
2N5485	3.0	400	100	400	5.0	1.0	4.0	400	25	0.5	4.0	4.0	10	5
2N5486	3.5	400	100	400	5.0	1.0	4.0	400	25	2.0	6.0	8.0	20	5
J308	12(1)	100	250(1)	100	7.5	2.5	1.5(1)	100	25	1.0	6.5	12	60	5
J309	12(1)	100	250(1)	100	7.5	2.5	1.5(1)	100	25	1.0	4.0	12	30	5
J310	12(1)	100	250(1)	100	7.5	2.5	1.5(1)	100	25	2.0	6.5	24	60	5

(1) Typical

Devices listed in bold, italic are Motorola preferred devices.

Table 32. JFET Switches and Choppers

The following is a listing of JFETs intended for switching and chopper applications.

Device	$R_{DS(on)}$ @ I_D		$V_{GS(off)}$ Volts		I_{DSS} mA		$V_{(BR)GSS}$ $V_{(BR)GDO}$ Volts	C_{iss} pF	C_{rss} pF	t_{on} ns	t_{off} ns	Style
	Ω Max	mA	Min	Max	Min	Max	Min	Max	Max	Max	Max	
Case 29–04 — TO-226AA (TO-92) — N-Channel												
MPF4856	25	—	4.0	10	50	—	40	18	8.0	9.0	25	5
MPF4859	25	—	4.0	10	50	—	30	18	8.0	9.0	25	5
J111	30	—	3.0	10	20	—	35	28	5.0	—	—	5
MPF4857	40	—	2.0	6.0	20	100	40	18	8.0	10	50	5
MPF4860	40	—	2.0	6.0	20	100	30	18	8.0	10	50	5
J112	50	—	1.0	5.0	5.0	—	35	28	5.0	—	—	5
MPF4392	60	—	—	—	25	75	30	10	3.5	15	35	5
2N5639	60	1.0	—	(8.0)(1)	25	—	30	10	4.0	—	—	5
MPF4861	60	—	0.8	4.0	8.0	80	30	18	8.0	20	100	5
MPF4393	100	—	—	(12)(1)	5.0	30	30	10	3.5	15	55	5
2N5640	100	1.0	—	(6.0)(1)	5.0	—	30	10	4.0	18	45	5
J113	100	—	0.5	3.0	2.0	—	35	28	5.0	—	—	5
2N5555	150	—	—	1.0(16)	15	—	25	5.0	1.2	10	25	5
BF246A	35(1)	1.0	0.6	14	30	80	25	—	—	—	—	22
BF246B	50(1)	1.0	0.6	14	60	140	25	—	—	—	—	22
J110	18	—	0.5	4.0	10	—	25	—	—	—	—	5
Case 29–04 — TO-226AA (TO-92) — P-Channel												
MPF970	100	1.0	5.0	12	15	100	30	12	5.0	8.0	25	5
MPF971	250	1.0	1.0	7.0	2.0	50	30	12	5.0	10	120	5

(1) Typical
(16) $V_{GS(f)}$

Devices listed in bold, italic are Motorola preferred devices.

TMOS FETs

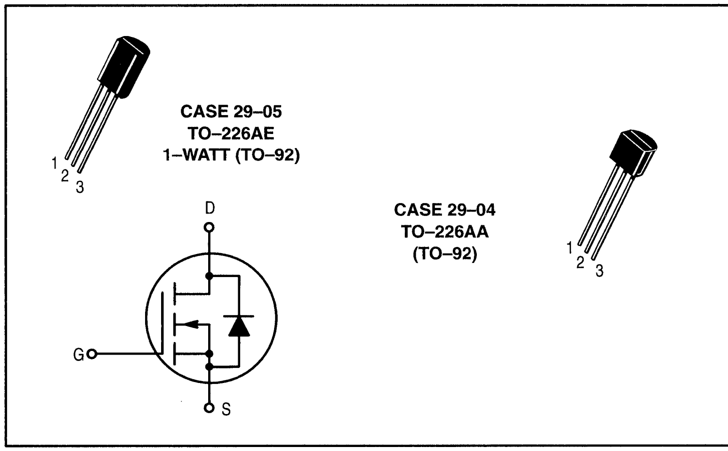


Table 33. TMOS Switches and Choppers

The following is a listing of small–signal TMOS devices that are intended for switching and chopper applications. These devices offer low $R_{DS(on)}$ characteristics.

Device	$R_{DS(on)}$ @ I_D Ω Max	$R_{DS(on)}$ @ I_D A	$V_{GS(th)}$ Volts Min	$V_{GS(th)}$ Volts Max	$V_{(BR)DSS}$ Volts Min	C_{iss} pF Max	C_{rss} pF Max	t_{on} ns Max	t_{off} ns Max	Style
Case 29–05 — TO–226AE (1–WATT TO–92) — N–Channel										
MPF930	1.4	1.0	1.0	3.5	35	70(1)	20(1)	15	15	22
MPF960	1.7	1.0	1.0	3.5	60	70(1)	20(1)	15	15	22
MPF6659	1.8	1.0	0.8	2.0	35	30(1)	4(1)	5.0	5.0	22
MPF990	2.0	1.0	1.0	3.5	90	70(1)	20(1)	15	15	22
MPF6660	3.0	1.0	0.8	2.0	60	30(1)	4(1)	5.0	5.0	22
MPF6661	4.0	1.0	0.8	2.0	90	30(1)	4(1)	5.0	5.0	22
MPF910	5.0	0.5	0.3	2.5	60	—	—	—	—	22
VN10LM	5.0	0.5	0.8	2.5	60	60	5.0	10	10	22
Case 29–04 — TO–226AA (TO–92) — N–Channel										
VN0300L	1.2	1.0	0.8	2.5	60	100	25	30	30	22
2N7000	5.0	0.5	0.8	3.0	60	60	5.0	10	10	22
BS170	5.0	0.2	0.8	3.0	60	25(1)	3.0(1)	10	10	30
VN0610LL	5.0	0.5	0.8	2.5	60	60	5.0	10	10	22
VN1706L	6.0	0.5	0.8	2.0	170	125	20	8.0	18	22
VN2406L	6.0	0.5	0.8	2.0	240	125	20	8.0	23	22
BSS89	6.0	0.30	1.0	2.7	200	72(1)	3.0(1)	6.0(1)	12(1)	7
BS107A	6.4	0.25	1.0	3.0	200	60(1)	6.0(1)	15	15	30
2N7008	7.5	0.5	1.0	2.5	60	50	5.0	20	20	22
VN2222LL	7.5	0.5	0.6	2.5	60	60	5.0	10	10	22
VN2410L	10	0.5	0.8	2.0	240	125	20	8.0	23	22
BS107	14	0.2	1.0	3.0	200	60(1)	6.0(1)	15	15	30

(1) Typical

Devices listed in bold, italic are Motorola preferred devices.

Surface Mount FETs

This section contains the FET plastic packages available for surface mount applications. Most of these devices are the most popular metal–can and insertion type parts carried over to the new surface mount packages.

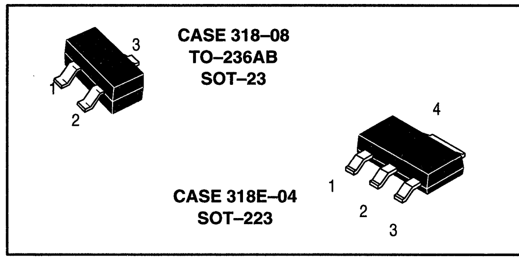


Table 34. Surface Mount RF JFETs

The following is a list of surface mount FETs which are intended for VHF/UHF RF amplifier applications.

Pinout: 1–Drain, 2–Source, 3–Gate

		NF		Y_{fs} @ V_{DS}				
Device	**Marking**	**dB Typ**	**f MHz**	**mmhos Min**	**mmhos Max**	**Volts**	**$V_{(BR)GSS}$**	**Style**
Case 318–08 — TO–236AB (SOT–23) — N–Channel								
MMBFJ309LT1	6U	1.5	450	10	20	10	25	10
MMBFJ310LT1	6T	1.5	450	8.0	18	10	25	10
MMBFU310LT1	M6C	1.5	450	10	18	10	25	10
MMBF4416LT1	M6A	2(3)	100	4.5	7.5	15	30	10
MMBF5484LT1	M6B	2.0	100	3.0	6.0	15	25	10
MMBF5486LT1	6H	2.0	100	4.0	8.0	15	25	10

(3) Max

Table 35. Surface Mount General–Purpose JFETs

The following table is a listing of surface mount small–signal general purpose FETs. These devices are intended for small–signal amplification for DC, audio, and lower RF frequencies. They also have applications as oscillators and general–purpose, low–voltage switches.

Pinout: 1–Drain, 2–Source, 3–Gate

			Y_{fs} @ V_{DS}			I_{DSS}		
Device	**Marking**	**$V_{(BR)GSS}$**	**mmhos Min**	**mmhos Max**	**Volts**	**mA Min**	**mA Max**	**Style**
Case 318–08 — TO–236AB (SOT–23) — N–Channel								
MMBF5457LT1	6D	25	1.0	5.0	15	1.0	5.0	10
MMBF5459LT1	6L	25	2.0	6.0	15	4.0	16	10
Case 318–08 — TO–236AB (SOT–23) — P–Channel								
MMBF5460LT1	M6E	40	1.0	4.0	15	1.0	5.0	10

(3) Max

Devices listed in bold, italic are Motorola preferred devices.

Surface Mount FETs (continued)

Table 36. Surface Mount Choppers/Switches JFETs

The following is a listing of small–signal surface mount JFET devices intended for switching and chopper applications.

Pinout: 1–Drain, 2–Source, 3–Gate

Device	Marking	$R_{DS(on)}$ Ohms Max	t_{off} ns Max	$V_{(BR)GSS}$	$V_{GS(off)}$ Volts Min	$V_{GS(off)}$ Volts Max	I_{DSS} mA Min	I_{DSS} mA Max	Style
Case 318–08 — TO–236AB (SOT–23) — N–Channel									
MMBF4856LT1	AAA	25	25	40	–4.0	–10	50	—	10
MMBF4391LT1	6J	30	20	30	–4.0	–10	50	150	10
MMBF4860LT1	6F	40	50	30	–2.0	–6.0	20	100	10
MMBF4392LT1	6K	60	35	30	–2.0	–5.0	25	75	10
MMBF4393LT1	6G	100	50	30	–0.5	–3.0	5.0	30	10
Case 318–08 — TO–236AB (SOT–23) — P–Channel									
MMBFJ175LT1	6W	125	—	30	3.0	6.0	7.0	60	10
MMBFJ177LT1	6Y	300	—	30	0.8	2.5	1.5	20	10

Table 37. TMOS FETs

The following is a listing of small–signal surface mount TMOS FETs which exhibit low $R_{DS(on)}$ characteristics.

Pinout: 1–Gate, 2–Source, 3–Drain

Device	Marking	$R_{DS(on)}$ @ I_D Ohm	$R_{DS(on)}$ @ I_D mA	V_{DSS}	$V_{GS(th)}$ Volts Min	$V_{GS(th)}$ Volts Max	Switching Time t_{on} ns	Switching Time t_{off} ns	Style
Case 318–08 — TO–236AB (SOT–23) — N–Channel									
MMBF170LT1	6Z	5.0	200	60	0.8	3.0	10	10	21
BSS123LT1	SA	6.0	100	100	0.8	2.8	20	40	21
2N7002LT1	702	7.5	500	60	1.0	2.5	20	20	21
MMBF0201NLT1	N1	1.0	300	20	1.0	2.4	2.5	15	21
Case 318–08 — TO–236 (SOT–23) — P–Channel									
MMBF0202PLT1	P3	1.4	200	20	1.0	2.4	2.5	16	21

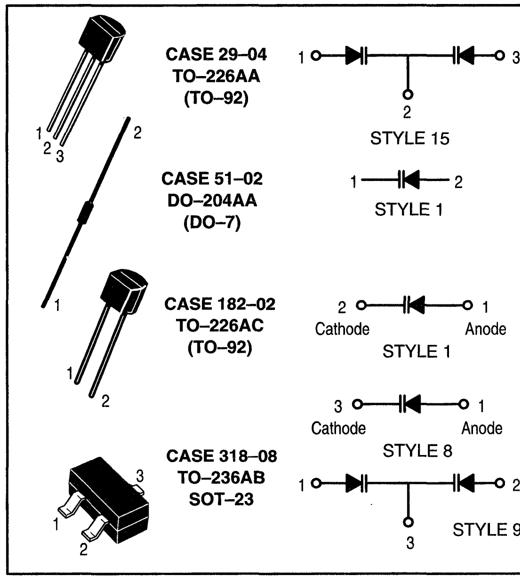
Pinout: 1–Gate, 2–Drain, 3–Source, 4–Drain

Device	Marking	$R_{DS(on)}$ Ohm	$R_{DS(on)}$ mA	V_{DSS}	$V_{GS(th)}$ Volts Min	$V_{GS(th)}$ Volts Max	Switching Time t_{on} ns	Switching Time t_{off} ns	Style
Case 318E–04— SOT–223 — N–Channel									
MMFT960T1	FT960	1.7	1000	60	1.0	3.5	15	15	3
MMFT6661T1	T6661	4.0	1000	90	0.8	2.0	5.0	5.0	3
MMFT2406T1	T2406	10	200	240	0.8	2.0	—	—	3
MMFT107T1	FT107	14	200	200	1.0	3.0	15	15	3

Devices listed in bold, italic are Motorola preferred devices.

Tuning and Switching Diodes

Tuning Diodes — Abrupt Junction



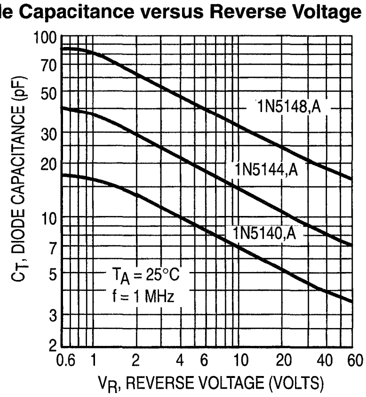
Motorola supplies voltage–variable capacitance diodes serving the entire range of frequencies from HF through UHF. Used in RF receivers and transmitters, they have a variety of applications, including:

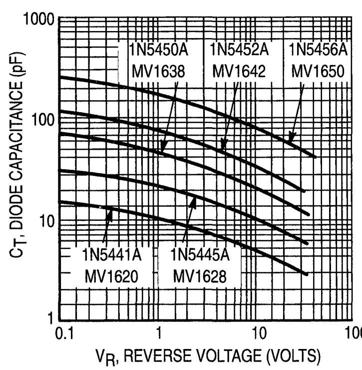
- Phase–locked loop tuning systems
- Local oscillator tuning
- Tuned RF preselectors
- RF filters
- RF phase shifters
- RF amplifiers
- Automatic frequency control
- Video filters and delay lines
- Harmonic generators
- FM modulators

Two families of devices are available: Abrupt Junction and Hyper Abrupt Junction. The Abrupt Junction family includes devices suitable for virtually all tuned–circuit and narrow–range tuning applications throughout the spectrum.

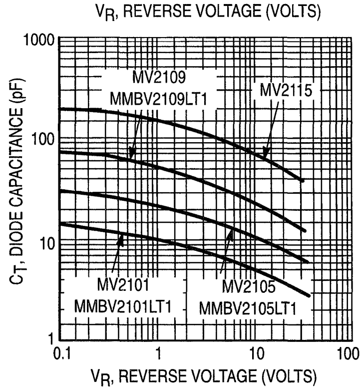
Typical Characteristics

Diode Capacitance versus Reverse Voltage

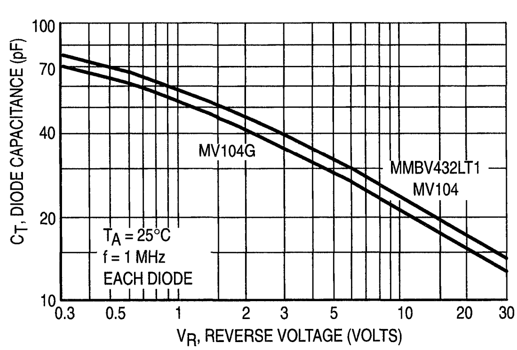




(See Tables 38 Thru 40)



(See Tables 41 and 42)



(See Table 43)

Tuning Diodes — Abrupt Junction (continued)

Table 38. General–Purpose Glass Abrupt Tuning Diodes
High Q Capacitance Ratio @ 4.0 Volts/60 Volts

The following is a listing of axial leaded, general–purpose, abrupt tuning diodes. These devices exhibit high Q characteristics.

Device[19]	C_T @ V_R = 4.0 V, 1.0 MHz pF Min	pF Nominal	pF Max	$V_{(BR)R}$ Volts	Cap Ratio C4/C60 Min	Q 4.0 V, 50 MHz Min
Case 51–02 — DO-204AA (DO–7)						
1N5139	6.1	6.8	7.5	60	2.7	350
1N5140	9.0	10	11	60	2.8	300
1N5143	16.2	18	19.8	60	2.8	250
1N5144	19.8	22	24.2	60	3.2	200
1N5145	24.3	27	29.7	60	3.2	200
1N5148	42.3	47	51.7	60	3.2	200

Table 39. General–Purpose Glass Abrupt Tuning Diodes
High Q Capacitance Ratio @ 2.0 Volts/30 Volts

The following is a listing of axial leaded, general–purpose, abrupt tuning diodes. These devices exhibit very high Q characteristics.

Device[20]	C_T @ V_R = 4.0 V, 1.0 MHz pF Min	pF Nominal	pF Max	$V_{R(BR)R}$ Volts	Cap Ratio C2/C30 Min	Q 4.0 V, 50 MHz Min
Case 51–02 — DO-204AA (DO–7)						
1N5441A	6.1	6.8	7.5	30	2.5	450
1N5444A	10.8	12	13.2	30	2.6	400
1N5446A	16.2	18	19.8	30	2.6	350
1N5448A	19.8	22	24.2	30	2.6	350
1N5449A	24.3	27	29.7	30	2.6	350
1N5450A	29.7	33	36.3	30	2.6	350
1N5451A	35.1	39	42.9	30	2.6	300
1N5452A	42.3	47	51.7	30	2.6	250
1N5453A	50.4	56	61.6	30	2.6	200
1N5455A	73.8	82	90.2	30	2.7	175
1N5456A	90	100	110	30	2.7	175

(19)Suffix A = 5.0%
(20)Suffix B = 5.0%

Tuning Diodes — Abrupt Junction (continued)

Table 40. General–Purpose Glass Abrupt Tuning Diodes
Capacitance Ratio @ 2.0 Volts/20 Volts

The following is a listing of axial leaded, general–purpose, abrupt tuning diodes. These devices exhibit high Q characteristics.

Device	C_T @ V_R = 4.0 V, 1.0 MHz pF Min	pF Nominal	pF Max	$V_{(BR)R}$ Volts	Cap Ratio C2/C20 Min	Q 4.0 V, 50 MHz Typ
Case 51–02 — DO–204AA (DO–7)						
MV1620	6.1	6.8	7.5	20	2.0	300
MV1624	9.0	10	11	20	2.0	300
MV1626	10.8	12	13.2	20	2.0	300
MV1628	13.5	15	16.5	20	2.0	250
MV1630	16.2	18	19.8	20	2.0	250
MV1634	19.8	22	24.2	20	2.0	250
MV1636	24.3	27	29.7	20	2.0	200
MV1638	29.7	33	36.3	20	2.0	200
MV1640	35.1	39	42.9	20	2.0	200
MV1642	42.3	47	51.7	20	2.0	200
MV1644	50.4	56	61.6	20	2.0	150
MV1648	73.8	82	90.2	20	2.0	150
MV1650	90	100	110	20	2.0	150

Table 41. General–Purpose Plastic Abrupt Tuning Diodes
Capacitance Ratio @ 2.0 Volts/30 Volts

The following is a listing of plastic package, general–purpose, abrupt tuning diodes. These devices exhibit high Q characteristics.

Device	C_T @ V_R = 4.0 V, 1.0 MHz pF Min	pF Nominal	pF Max	$V_{R(BR)R}$ Volts	Cap Ratio C4/C30 Min	Q 4.0 V, 50 MHz Typ
Case 182–02 — TO–226AC (TO–92) — 2–Lead						
MV2101	6.1	6.8	7.5	30	2.5	400
MV2103	9.0	10	11	30	2.5	350
MV2104	10.8	12	13.2	30	2.5	350
MV2105	13.5	15	16.5	30	2.5	350
MV2107	19.8	22	24.2	30	2.5	300
MV2108	24.3	27	29.7	30	2.5	250
MV2109	29.7	33	36.3	30	2.5	200
MV2111	42.3	47	51.7	30	2.5	150
MV2113	61.2	68	74.8	30	2.5	150
MV2114	73.8	82	90.2	30	2.5	100
MV2115	90	100	110	30	2.6	100

Devices listed in bold, italic are Motorola preferred devices.

Tuning Diodes — Abrupt Junction (continued)

Table 42. Surface Mount Abrupt Tuning Diodes
Capacitance Ratio @ 2.0 Volts/30 Volts

The following is a listing of surface mount abrupt junction tuning diodes intended for general–purpose variable capacitance circuit applications.

Device	C_T @ V_R = 4.0 V, 1.0 MHz pF Min	pF Nominal	pF Max	$V_{R(BR)R}$ Volts	Cap Ratio C2/C30 Min	Q 4.0 V, 50 MHz Typ
Case 318–08 — DO–236AB (SOT–23)						
MMBV2101LT1	6.1	6.8	7.5	30	2.5	400
MMBV2103LT1	9.0	10	11	30	2.5	350
MMBV2104LT1	10.8	12	13.2	30	2.5	350
MMBV2105LT1	13.5	15	16.5	30	2.5	350
MMBV2107LT1	19.8	22	24.2	30	2.5	300
MMBV2108LT1	24.3	27	29.7	30	2.5	250
MMBV2109LT1	29.7	33	36.3	30	2.5	200

Table 43. Abrupt Tuning Diodes for FM Radio — Dual

The following is a listing of abrupt tuning diodes that are available as dual units in a single package.

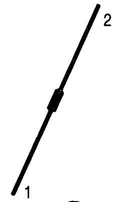
Device	C_T @ V_R(22) pF Min	pF Max	Volts	Cap Ratio C3/C30 Min	Q 3.0 V, 50 MHz Min	$V_{(BR)R}$ Volts	Device Marking	Style
Case 29–04 — TO–226AA (TO–92)								
MV104	37	42	3.0	2.5	100	32	—	15
Case 318–08 — TO–236AB (SOT–23)								
MMBV432LT1	43	48.1	2.0	1.5(21)	100	14	M4B	9

(21)C2/C8
(22)Each Diode

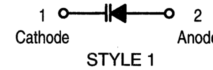
Devices listed in bold, italic are Motorola preferred devices.

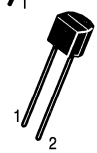
Tuning Diodes — Hyper–Abrupt Junction

The Hyper–Abrupt family exhibits higher capacitance, and a much larger capacitance ratio. It is particularly well suited for wider–range applications such as AM/FM radio and TV tuning.

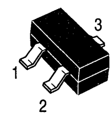


CASE 51–02
DO–204AA
(DO–7)

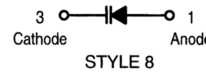


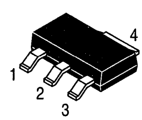


CASE 182–02
TO–226AC
(TO–92)



CASE 318–08
TO–236AB
SOT–23





CASE 318E–04
SOT–223

Typical Characteristics

Diode Capacitance versus Reverse Voltage

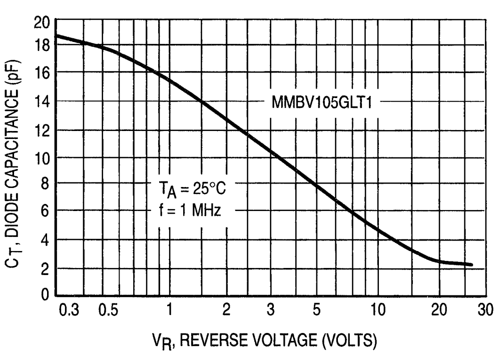


Figure 1. Diode Capacitance

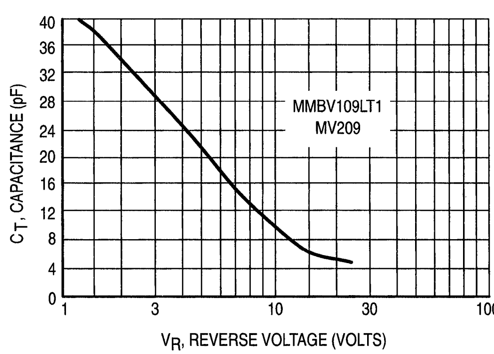


Figure 2. Diode Capacitance

Tuning Diodes — Hyper–Abrupt Junction (continued)

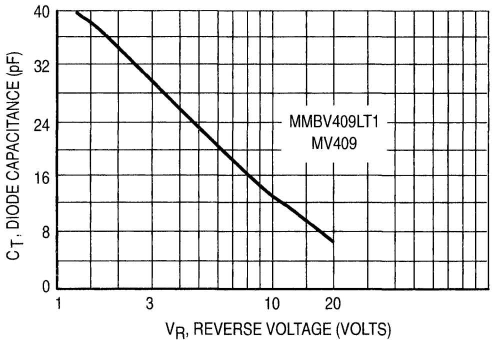


Figure 3. Diode Capacitance

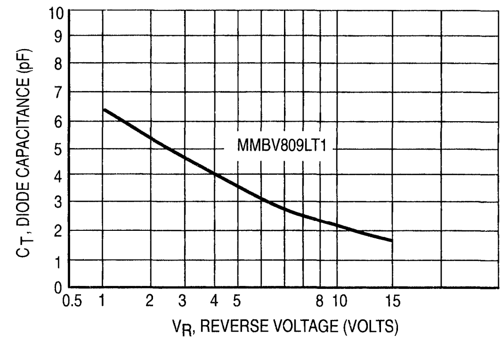


Figure 4. Diode Capacitance

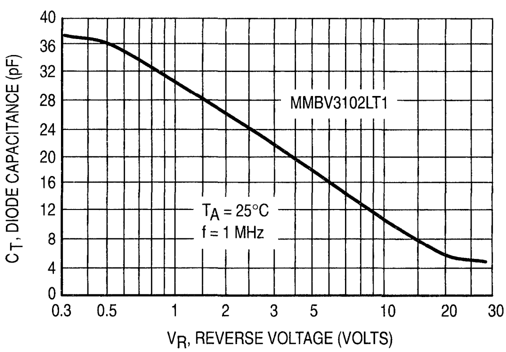


Figure 5. Diode Capacitance

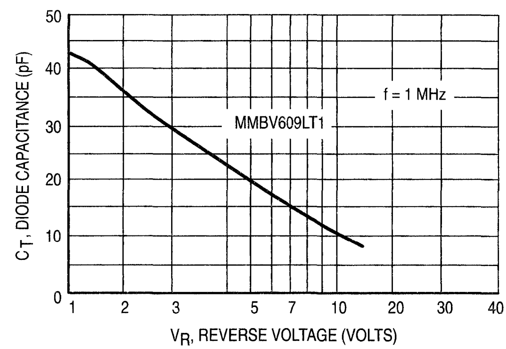


Figure 6. Diode Capacitance Each Die

MVAM108

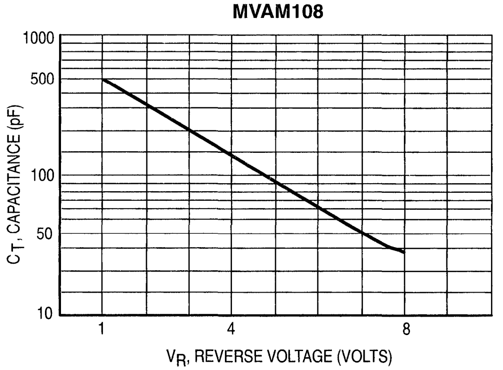


Figure 7. Capacitance versus Reverse Voltage

MVAM109/MV7005T1

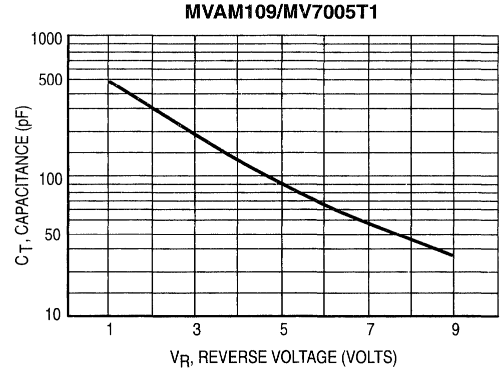


Figure 8. Capacitance versus Reverse Voltage

Tuning Diodes — Hyper–Abrupt Junction (continued)

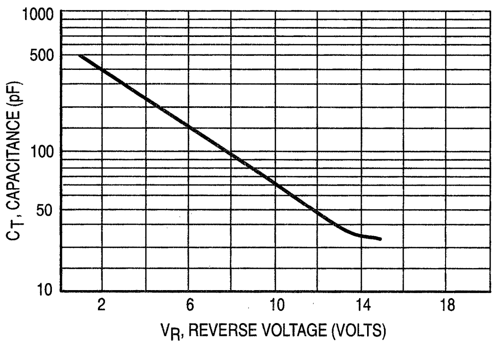


Figure 9. Capacitance versus Reverse Voltage

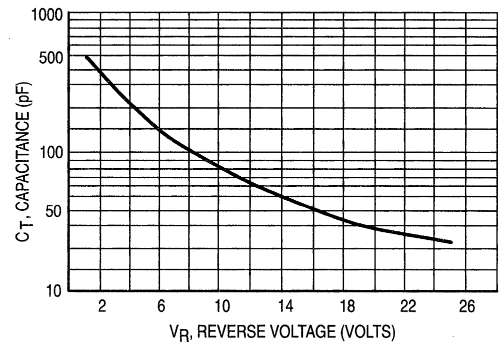


Figure 10. Capacitance versus Reverse Voltage

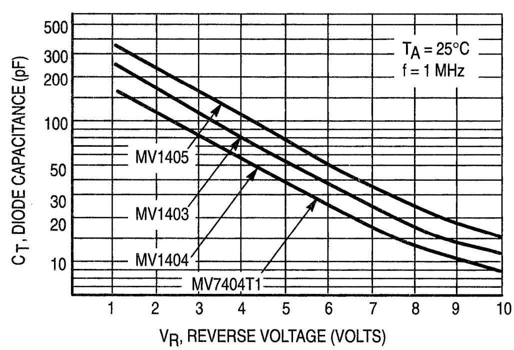


Figure 11. Diode Capacitance versus Reverse Voltage

Table 44. Hyper–Abrupt Tuning Diodes for Telecommunications — Single

The following is a listing of hyper–abrupt tuning diodes intended for high frequency, FM radio, and TV tuner applications.

Device	C_T @ V_R (f = 1.0 MHz) pF Min	pF Max	Volts	Cap Ratio @ V_R Min	Max	Volts	Q 3.0 V Min	50 MHz Max	$V_{(BR)R}$ Volts	Device Marking	Case Style	CV Curve Fig
Case 182–02 — TO–226AC (TO–92)												
MV209	26	32	3.0	5.0	6.5	3/25	200	—	30	—	1	2
MV409	26	32	3.0	1.5	2.0	3/8	200	—	20	—	1	3
Case 318–08 — TO–236AB (SOT–23)												
MMBV105GLT1	1.5	2.8	25	4.0	6.5	3/25	200	—	30	M4E	8	1
MMBV109LT1	26	32	3.0	5.0	6.5	3/25	200	—	30	M4A	8	2
MMBV409LT1	26	32	3.0	1.5	1.9	3/8	200	—	20	X5	8	3
MMBV809LT1	4.5	6.1	2.0	1.8	2.6	2/8	300	—	20	5K	8	4
MMBV3102LT1	20	25	3.0	4.5	—	3/25	200	—	30	M4C	8	5
Case 419–02 — SC–70/SOT–323												
MBV109T1	26	32	3.0	5.0	6.5	3/25	200	—	30	M4A	8	—

Devices listed in bold, italic are Motorola preferred devices.

Tuning Diodes — Hyper–Abrupt Junction (continued)

Table 45. Hyper–Abrupt Tuning Diodes for Communications — Dual

Device	C_T @ V_R (f = 1.0 MHz) pF Min	pF Max	Volts	Cap Ratio @ V_R Min	Max	Volts	Q 3.0 V Min	50 MHz Max	$V_{(BR)R}$ Volts	Device Marking	Case Style	CV Curve Fig
Case 318–08 — TO–236AB (SOT–23)												
MMBV609LT1	26	32	3.0	1.8	2.4	3/8	250	—	20	5L	9	6

Table 46. Hyper–Abrupt Tuning Diodes for Low Frequency Applications — Single

The following is a listing of AM, hyper–abrupt tuning diodes that have a large capacity range and are designed for low frequency circuit applications.

Device	C_T @ 1.0 MHz pF Min	pF Max	Volts	Cap Ratio @ V_R Min	Volts	$V_{(BR)R}$ Volts	Style	CV Curve Figure
Case 182–02— TO–226AC (TO–92)								
MVAM108	440	560	1.0	15	1.0/8.0	12	1	7
MVAM109	400	520	1.0	12	1.0/9.0	15	1	8
MVAM115	440	560	1.0	15	1.0/15	18	1	9
MVAM125	440	560	1.0	15	1.0/25	28	1	10

Table 47. Hyper–Abrupt High Capacitance Voltage Variable Diode — Surface Mount

The following are high capacitance voltage variable diodes intended for low frequency applications and circuits requiring large tuning capacitance.

Device	$V_{(BR)R}$ Volts	I_R nA	C_T @ f = 1.0 MHz Min pF	Max pF	Cap Ratio Min	Q Min	Style	CV Curve Figure
Case 318E–04— SOT–223								
Pinout: 1–Anode, 2, 4–Cathode, 3–NC								
MV7005T1	15	100	400	520	12(26)	150(28)	2	8
MV7404T1	12	100	96	144	10(27)	200(29)	2	11

Table 48. Hyper–Abrupt High Capacitance Tuning Diodes — Axial Lead Glass Package

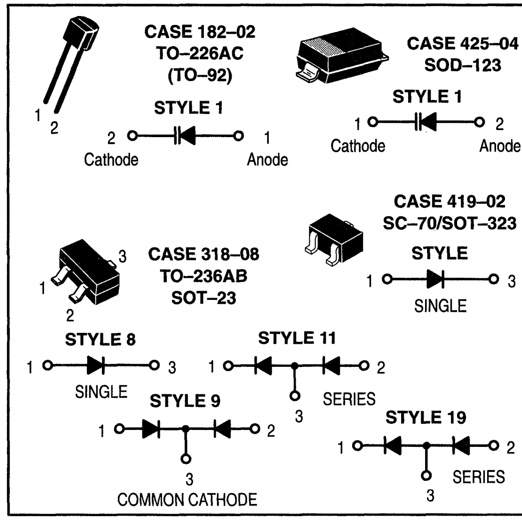
Device	C_T @ V_R pF Min	pF Max	Volts	Cap Ratio C2/C10 Min	Q 2.0 V, 1.0 MHz Min	$V_{(BR)R}$ Volts	Style	CV Curve Figure
Case 51–02 — DO–204AA (DO–7)								
MV1404	96	144	2.0	10	200	12	1	11
MV1403	140	210	2.0	10	200	12	1	11
MV1405	200	300	2.0	10	200	12	1	11

(26) V_R = 1.0 V/V_R = 9.0 V
(27) V_R = 2.0 V/V_R = 10 V
(28) V_R = 1.0 V, f = 1.0 MHz
(29) V_R = 2.0 V, f = 1.0 MHz

Devices listed in bold, italic are Motorola preferred devices.

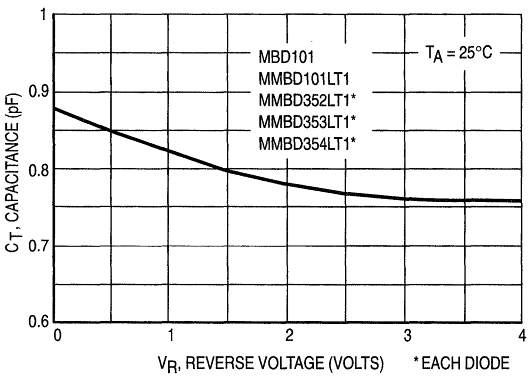
Hot–Carrier (Schottky) Diodes

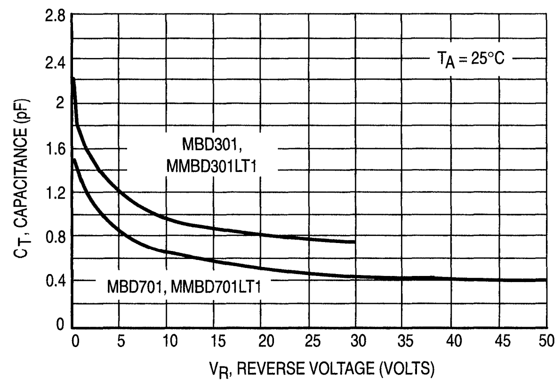
Hot–Carrier diodes are ideal for VHF and UHF mixer and detector applications as well as many higher frequency applications. They provide stable electrical characteristics by eliminating the point–contact diode presently used in many applications.



Typical Characteristics

Capacitance versus Reverse Voltage





(See Table 49)

Table 49. Hot–Carrier (Schottky) Diodes

The following is a listing of hot carrier (Schottky) diodes that exhibit low forward voltage drop for improved circuit efficiency.

Device	$V_{(BR)R}$ Volts	C_T @ V_R pF Max	V_F @ 10 mA Volts Max	I_R @ V_R nA Max	Minority Lifetime pS (TYP)	Device Marking	Style
Case 182–02 — TO–226AC (TO–92)							
MBD701	70	1.0 @ 20 V	1.0	200 @ 35 V	15	—	1
MBD301	30	1.5 @ 15 V	0.6	200 @ 25 V	15	—	1
MBD101	7.0	1.0 @ 0 V	0.6	250 @ 3.0 V	—	—	1
Case 318–08 — TO–236AB (SOT–23)							
MMBD701LT1	70	1.0 @ 20 V	1.0	200 @ 35 V	15	5H	8
MMBD301LT1	30	1.5 @ 15 V	0.6	200 @ 25 V	15	4T	8
MMBD101LT1	7.0	1.0 @ 0 V	0.6	250 @ 3.0 V	15	4M	8
MMBD352LT1 (23)	7.0	1.0 @ 0 V	0.6	250 @ 3.0 V	15	M5G	11
MMBD353LT1 (23)	7.0	1.0 @ 0 V	0.6	250 @ 3.0 V	15	M4F	19
MMBD354LT1 (23)	7.0	1.0 @ 0 V	0.6	250 @ 3.0 V	15	M6H	9

(23) Dual Diodes

Devices listed in bold, italic are Motorola preferred devices.

Table 49. Hot–Carrier (Schottky) Diodes

The following is a listing of hot carrier (Schottky) diodes that exhibit low forward voltage drop for improved circuit efficiency.

Device	$V_{(BR)R}$ Volts	C_T @ V_R pF Max	V_F @ 10 mA Volts Max	I_R @ V_R nA Max	Minority Lifetime pS (TYP)	Device Marking	Style
Case 425–04 — (SOD–123)							
MMSD701T1	70	1.0 @ 20 V	1.2	0.2 @ 35 V	15	5H	1
MMSD301T1	30	1.5 @ 15 V	0.6	0.2 @ 25 V	15	4T	1
MMSD101T1	4	1.0 @ 0 V	0.6	0.25 @ 3 V	15	4M	1
Case 419–02 – (SC–70/SOT–323)							
MMBD330T1	30	1.5 @ 15 V	0.6	0.2 @ 25 V	—	4T	2
MMBD770T1	70	1.0 @ 20 V	1.0	0.2 @ 35 V	—	5H	2

(23) Dual Diodes

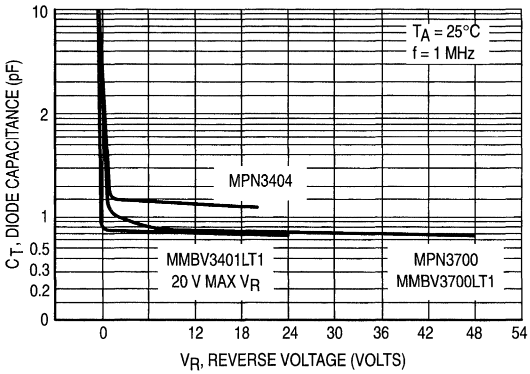
Devices listed in bold, italic are Motorola preferred devices.

Switching Diodes

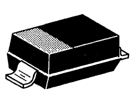
Small–signal switching diodes are intended for low current switching and steering applications. Hot–Carrier, PIN and general–purpose diodes allow a wide selection for specific application requirements.

Typical Characteristics

Capacitance versus Reverse Voltage



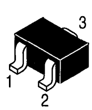
(See Table 50)



STYLE 1

CASE 425–04
SOD–123

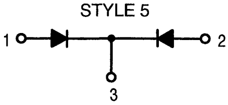
CASE 419–02
SC–70/SOT–323



STYLE 2

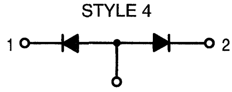
SINGLE

STYLE 5

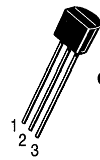


COMMON CATHODE

STYLE 4

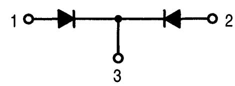


COMMON ANODE

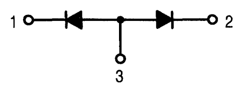


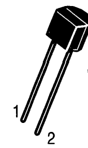
CASE 29–04
TO–226AA
(TO–92)

STYLE 3



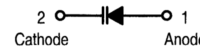
STYLE 4

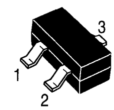




CASE 182–02
TO–226AC
(TO–92)

STYLE 1



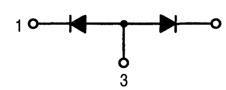


CASE 318–08
TO–236AB
SOT–23

STYLE 8

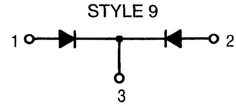
SINGLE

STYLE 12



COMMON ANODE

STYLE 9

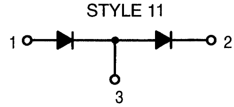


COMMON CATHODE

STYLE 18

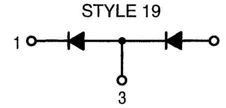
SINGLE

STYLE 11



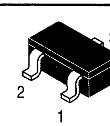
SERIES

STYLE 19



SERIES

CASE 318D–03
SC–59



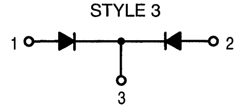
STYLE 2

SINGLE

STYLE 4

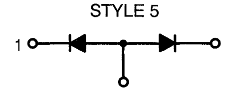
SINGLE

STYLE 3



COMMON CATHODE

STYLE 5



COMMON ANODE

Switching Diodes (continued)

Table 50. PIN Switching Diodes

The following PIN diodes are designed for VHF band switching and general–purpose low current switching applications.

Device	$V_{(BR)R}$ Volts Min	C_T @ V_R @ 1.0 MHz pF Max	Volts	I_R @ V_R nA Max	Series Resistance Ohm Max	Device Marking	Style
Case 182–02 — TO–226AC (TO–92)							
MPN3700	200	1.0	20	0.1 @ 150	1.0 @ 10 mA	—	1
MPN3404	20	2.0	15	0.1 @ 25 V	0.85 @ 10 mA	—	1
Case 318–08 — TO–236AB (SOT–23)							
MMBV3700LT1	200	1.0	20	0.1 @ 150	1.0 @ 10 mA	4R	8
MMBV3401LT1	35	1.0	20	0.1 @ 25 V	0.7 @ 10 mA	4D	8

Table 51. General–Purpose Signal and Switching Diodes — Single

The following is a listing of small–signal switching diodes in surface mount packages. These diodes are intended for low current switching and signal steering applications.

Device	Marking	$V_{(BR)R}$ Min Volts	@ I_{BR} (μA)	I_R Max (μA)	@ V_R Volts	V_F Min Volts	Max Volts	@ I_F (mA)	C_T(30) Max (pF)	t_{rr} Max (ns)	Case Style
Case 318–08 — TO–236AB (SOT–23)											
BAS21LT1	JS	250	100	0.1	200	—	1.0	100	5.0	50	8
MMBD914LT1	5D	100	100	5.0	75	—	1.0	10	4.0	4.0	8
BAS16LT1	A6	75	100	1.0	75	—	1.0	50	2.0	6.0	8
MMBD6050LT1	5A	70	100	0.1	50	0.85	1.1	100	2.5	4.0	8
BAL99LT1	JF	70	100	2.5	70	—	1.0	50	1.5	6.0	18
Case 318D–03 — SC–59											
M1MA151AT1	MA	40	100	0.1	35	—	1.2	100	2.0	3.0	4
M1MA151KT1	MH	40	100	0.1	35	—	1.2	100	2.0	3.0	2
Case 419–02 — SC–70/SOT–323											
BAS16WT1	A6	75	1.0	0.02	20	—	1.25	150	2.0	6.0	2
M1MA141KT1	MH	40	100	0.1	35	—	1.2	100	2.0	3.0	2
M1MA142KT1	MI	80	100	0.1	75	—	1.2	100	2.0	3.0	2
M1MA174T1	J6	100	100	5.0	75	—	1.0	10	4.0	4.0	2
Case 425–04— SOD–123											
MMSD914T1	5D	100	100	5.0	75	—	1.0	10	4.0	4.0	1

(30) V_R = 0 V, f = 1.0 MHz

Devices listed in bold, italic are Motorola preferred devices.

Switching Diodes (continued)

Table 52. General–Purpose Signal and Switching Diodes — Dual

The following is a listing of small–signal switching diodes in surface mount packages. These diodes are intended for low current switching and signal steering applications.

Device	Marking	$V_{(BR)R}$ Min Volts	$V_{(BR)R}$ @ I_{BR} (µA)	I_R Max (µA)	I_R @ V_R Volts	V_F Min Volts	V_F Max Volts	V_F @ I_F (mA)	C_T(30) Max (pF)	t_{rr} Max (ns)	Case Style
Case 318–08 — TO–236AB (SOT–23)											
MMBD7000LT1	M5C	100	100	1.0	50	0.75	1.1	100	1.5	4.0	11
MMBD2836LT1	A2	75	100	0.1	50	—	1.0	10	4.0	4.0	12
MMBD2838LT1	A6	75	100	0.1	50	—	1.0	10	4.0	4.0	9
BAV70LT1	A4	70	100	5.0	70	—	1.0	50	1.5	6.0	9
BAV99LT1	A7	70	100	2.5	70	—	1.0	50	1.5	4.0	11
BAW56LT1	A1	70	100	2.5	70	—	1.0	50	2.0	6.0	12
MMBD6100LT1	5BM	70	100	0.1	50	0.85	1.1	100	2.5	4.0	9
BAV74LT1	JA	50	5.0	0.1	50	—	1.0	100	2.0	4.0	9
MMBD2835LT1	A3	35	100	0.1	30	—	1.0	10	4.0	4.0	12
MMBD2837LT1	A5	35	100	0.1	30	—	1.0	10	4.0	4.0	9
Case 318D–03 — SC–59											
M1MA151WAT1	MN	40	100	0.1	35	—	1.2	100	15	10	5
M1MA151WKT1	MT	40	100	0.1	35	—	1.2	100	2.0	3.0	3
Case 419–02 — SC–70/SOT–323											
M1MA142WKT1	MU	80	100	0.1	75	—	1.2	100	2.0	3.0	5
M1MA142WAT1	MO	80	100	0.1	75	—	1.2	100	15	10	4
BAW56WT1	A1	70	100	2.5	70	—	1.0	50	2.0	6.0	4
BAV70WT1	A4	70	100	5.0	70	—	1.0	50	1.5	6.0	5
M1MA141WKT1	MT	40	100	0.1	35	—	1.2	100	2.0	3.0	5
M1MA141WAT1	MN	40	100	0.1	35	—	1.2	100	15	10	4

Table 53. Low–Leakage Medium Speed Switching Diodes — Single

Device	Marking	$V_{(BR)R}$ Min Volts	$V_{(BR)R}$ @ I_{BR} (µA)	I_R Max (nA)	I_R @ V_R Volts	V_F Min Volts	V_F Max Volts	V_F @ I_F (mA)	C_T(30) Max (pF)	t_{rr} Max (ns)	Case Style
Case 318–08 — TO–236AB (SOT–23)											
BAS116LT1	JV	75	100	5.0	75	—	1.0	10	2.0	3000	8
MMBD1000LT1	AY	30	100	0.5	30	—	0.95	10	2.0	3000	6
Case 419–02 — (SOT–323)/(SC–70)											
MMBD2000T1	DH	30	100	0.5	30	—	0.95	10	2.0	3000	2
Case 318D–03 — (SC–59)											
MMBD3000T1	XP	30	100	0.5	30	—	0.95	10	2.0	3000	2
Case 425–04 — (SOD–123)											
MMSD1000T1	4K	30	100	0.5	30	—	0.95	10	2.0	3000	1

Devices listed in bold, italic are Motorola preferred devices.

Switching Diodes (continued)

Table 54. Low–Leakage Medium Speed Switching Diodes — Dual

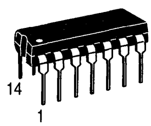
Device	Marking	$V_{(BR)R}$ Min Volts	$V_{(BR)R}$ @ I_{BR} (μA)	I_R Max (nA)	I_R @ V_R Volts	V_F Min Volts	V_F Max Volts	V_F @ I_F (mA)	C_T(30) Max (pF)	t_{rr} Max (ns)	Case Style
Case 318–08 — TO–236AB (SOT–23)											
BAV170LT1	JX	70	100	5.0	70	—	1.0	10	2.0	3000	9
BAV199LT1	JY	70	100	5.0	70	—	1.0	10	2.0	3000	11
BAW156LT1	JZ	70	100	5.0	70	—	1.0	10	2.0	3000	12
MMBD1005LT1	A3	30	100	0.5	30	—	0.95	10	2.0	3000	12
MMBD1010LT1	A5	30	100	0.5	30	—	0.95	10	2.0	3000	9
Case 419–02 — (SOT–323)/(SC–70) — DUAL											
MMBD2005T1	DI	30	100	0.5	30	—	0.95	10	2.0	3000	4
MMBD2010T1	DP	30	100	0.5	30	—	0.95	10	2.0	3000	5
Case 318D–03 — (SC–59) — DUAL											
MMBD3005T1	XQ	30	100	0.5	30	—	0.95	10	2.0	3000	5
MMBD3010T1	XS	30	100	0.5	30	—	0.95	10	2.0	3000	3

(30) V_R = 0 V, f = 1.0 MHz

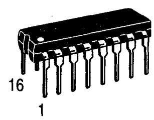
Devices listed in bold, italic are Motorola preferred devices.

Multiple Switching Diodes

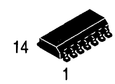
Multiple diode configurations utilize monolithic structures fabricated by the planar process. They are designed to satisfy fast switching requirements as in core driver and encoding/decoding applications where their monolithic configurations offer lower cost, higher reliability and space savings.



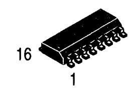
CASE 646–06
PIN DIP
PLASTIC



CASE 648–08
PIN DIP
PLASTIC



CASE 751A–03
SO–14
PLASTIC

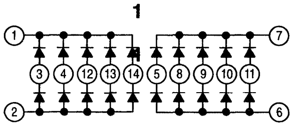


CASE 751B–05
SO–16
PLASTIC

Diode Array Diagrams

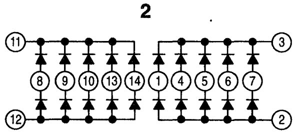
1

Dual 10 Diode Array



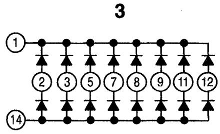
2

Dual 10 Diode Array



3

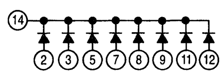
16 Diode Array



NC Pin 4,6,10,13

4

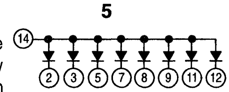
8 Diode Array (Common Cathode)



NC Pin 1, 4, 6, 10, 13

5

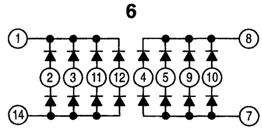
8 Diode Array (Common Anode)



NC Pin 1, 4, 6, 10, 13

6

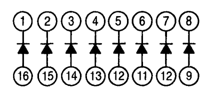
Dual 8 Diode Array



NC Pin 6, 13

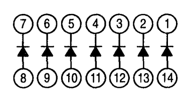
7

Isolated 8 Diode Array



8

Isolated 7 Diode Array



Multiple Switching Diodes (continued)

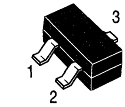
Table 55. Diode Arrays

Case 646 — TO–116

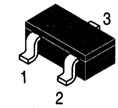
Device	Function	Pin Connections Diagram Number
MAD130P	Dual 10 Diode Array	1
MAD1103P	16 Diode Array	3
MAD1107P	Dual 8 Diode Array	6
MAD1109P	7 Isolated Diode Array	8
Case 648–08		
MAD1108P	8 Isolated Diode Array	7
Case 751A–03— SO–14		
MMAD130	Dual 10 Diode Array	2
MMAD1103	16 Diode Array	3
MMAD1105	8 Diode Common Cathode Array	4
MMAD1106	8 Diode Common Anode Array	5
MMAD1107	Dual 8 Diode Array	6
MMAD1109	7 Isolated Diode Array	8
Case 751B–05 — SO–16		
MMAD1108	8 Isolated Diode Array	7

Devices listed in bold, italic are Motorola preferred devices.

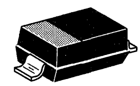
GREEN LINE™



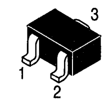
CASE 318–08
TO–236AB
SOT–23



CASE 318D–03
SC–59



CASE 425–04
SOD–123



CASE 419–02
SC–70/SOT–323

Plastic–Encapsulated Surface Mount Devices

Energy. It's something Motorola is putting a lot of energy into helping save. That's why we're introducing our GreenLine™ portfolio of devices, featuring energy–conserving traits superior to those of our existing line of standard parts for the same usage. GreenLine devices can actually help reduce the power demands of your products.

Wide Range of Applications

Currently, our portfolio consists of three families.

- **Low–Leakage Switching Diodes:** With reverse leakage specifications guaranteed to 500 pA, they help extend battery life, making them ideal for small battery–operated systems in which standby power is essential. Applications include ESD protection, reverse voltage protection, and steering logic.
- **Bipolar Output Driver Transistors:** Offering ultra–low collector saturation voltage, they deliver more energy to the intended load with less power wasted through dissipation loss. They are especially effective in today's lower voltage battery–powered applications, and prolong battery life in portable and hand–held communications and personal digital equipment.
- **Small Signal HDTMOS™:** These devices provide our lowest ever drain–source resistance versus package size. Lower $r_{DS(on)}$ means less wasted energy through dissipation loss, making them especially effective for low–current applications where energy conservation is crucial, such as low current switchmode power supplies, uninterruptable power supplies (UPS), power management systems, and bias switching. This makes them ideal for portable computer–type products or any system where the combination of power management and energy conservation is key.

Save Energy — Save Money

In an increasingly power–hungry world, Motorola's GreenLine portfolio makes powerful sense. So much sense that we plan to continue adding devices to the portfolio. Chances are, there are Motorola GreenLine devices applicable to one or more of your products — ones that can help save energy, dollars — and the environment.

Table 56. Bipolar Driver Transistor — PNP

These offer ultra–low collector saturation voltage.

Pinout: 1–Base, 2–Emitter, 3–Collector

Device Type	Marking	Case	$V_{(BR)CEO}$	$V_{CE(sat)}$	$V_{BE(sat)}$	h_{FE} @ I_C Min	Max	mA
MMBT1010LT1	GLP	SOT–23	15	0.1	1.1	300	600	100
MSD1010T1	GLP	SC–59	15	0.1	1.1	300	600	100

Devices listed in bold, italic are Motorola preferred devices.

GreenLine (continued)

Table 57. Low Leakage Switching Diodes

These offer reverse leakage specifications guaranteed to 500 pA. Versions available in single and dual.

Device Type	Marking	Case	Style	$V_{(BR)R}$ Min Volts	$V_{(BR)R}$ @ I_{BR} (μA)	I_R Max (nA)	I_R @ V_R Volts
MMBD1000LT1	AY	SOT–23	Single	30	100	0.5	30
MMBD1005LT1	A3	SOT–23	Dual Anode	30	100	0.5	30
MMBD1010LT1	A5	SOT–23	Dual Cathode	30	100	0.5	30
MMBD2000T1	DH	SC–70	Single	30	100	0.5	30
MMBD2005T1	DI	SC–70	Dual Anode	30	100	0.5	30
MMBD2010T1	DP	SC–70	Dual Cathode	30	100	0.5	30
MMBD3000T1	XP	SC–59	Single	30	100	0.5	30
MMBD3005T1	XQ	SC–59	Dual Anode	30	100	0.5	30
MMBD3010T1	XS	SC–59	Dual Cathode	30	100	0.5	30
MMSD1000T1	4K	SOD–123	Single	30	100	0.5	30

Table 58. Small Signal HDTMOS™

These provide the lowest drain–source resistance versus package size.

Device Type	Marking	Channel	$R_{DS(on)}$ Ohm	$R_{DS(on)}$ mA	V_{DSS}	$V_{GS(th)}$ Volts Min	$V_{GS(th)}$ Volts Max	Switching Time $t_{(on)}$ ns	Switching Time $t_{(off)}$ ns	Style
Case 318–08 — TO–236AB (SOT–23) — P–Channel and N–Channel										
MMBF0201NLT1	N1	N	1.0	300	20	1.0	2.4	2.5	15	21
MMBF0202PLT1	P3	P	1.4	200	20	1.0	2.4	2.5	16	21

Devices listed in bold, italic are Motorola preferred devices.

Devices listed in bold, italic are Motorola preferred devices.

TVS/Zeners
Transient Voltage Suppressors
Zener Regulator and Reference Diodes

In Brief . . .

Motorola's standard TVS (Transient Voltage Suppressors) and Zener diodes comprise the largest inventoried line in the industry. Continuous development of improved manufacturing techniques have resulted in computerized diffusion and test, as well as critical process controls learned from surface–sensitive MOS fabrication. Resultant high yields lower factory costs. Check the following features for application to your specific requirements:

- Wide selection of package materials and styles:
  - — Plastic (Surmetic) for low cost, mechanical ruggedness
  - — Glass for high reliability, low cost
  - — Surface Mount packages for state of the art designs
- Power Ratings from 0.25 to 5.0 Watts
- Breakdown voltages from 1.8 to 400 Volts in approximately 10% steps
- TVS from 24 to 1500 Watts and from 6.2 to 250 Volts
- ESD protection devices
- Available tolerances from 5% (low cost) to as tight as 1% (critical applications)
- Special selection of electrical characteristics available at low cost due to high–volume lines (check your Motorola sales representative for special quotations)
- UL Recognition on many TVS device types
- Tape and Reel options available on all axial leaded and surface mount types

Page

Note: Any TVS/Zener device not listed in this Master Selection Guide may be available with a special order. Please contact your Motorola representative for details.

TVS (Transient Voltage Suppressors)

General–Purpose

Transient Voltage Suppressors are designed for applications requiring protection of voltage sensitive electronic devices in danger of destruction by high energy voltage transients. Many of the zener voltage regulator diodes listed in the previous charts are in fact used in circuits as transient voltage suppressors. The purpose of this section is to present the families of Motorola Zeners that are specified with the key transient voltage suppressor parameters and limits, e.g., maximum clamping voltage at maximum surge current rating and working peak reverse (stand–off) voltage.

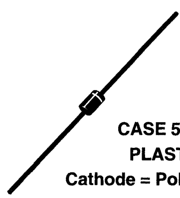
Selection sequence:

1. Package type (axial or surface mount)
2. Peak surge power expected for the application
3. Working peak reverse stand–off voltage (or the breakdown voltage)
4. Maximum reverse clamping voltage

Consult the factory for special electrical selections if there is no standard device type available to fit the application.

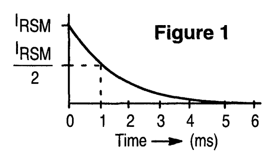
Axial Leaded for Through–hole Designs

Table 1. Peak Power Dissipation(1) (*500 Watts* @ 1 ms Surge – Figure 1)
Case 59–04 — Mini Mosorb



CASE 59-04 (Mini Mosorb™)
PLASTIC
Cathode = Polarity Band

Figure 1



Surge Current Characteristics

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) V_F = 3.5 V Max, I_F = 35 A Pulse (except bidirectional devices).

Working Peak Reverse Voltage V_{RWM} (Volts)	Device(2)	Breakdown Voltage V_{BR} (Volts) Min	Breakdown Voltage V_{BR} (Volts) Max	@ I_T Pulse (mA)	Maximum Reverse Leakage @ V_{RWM} I_R (μA)	Maximum Reverse Surge Current I_{RSM} Figure 1 (Amps)	Maximum Reverse Voltage @ I_{RSM} (Clamping Voltage) V_{RSM} (Volts)
5	***SA5.0A***	6.4	7	10	600	54.3	9.2
6	***SA6.0A***	6.67	7.37	10	600	48.5	10.3
7	SA7.0A	7.78	8.6	10	150	41.7	12
8	SA8.0A	8.89	9.83	1	25	36.7	13.6
11	***SA11A***	12.2	13.5	1	1	27.4	18.2
12	***SA12A***	13.3	14.7	1	1	25.1	19.9
13	SA13A	14.4	15.9	1	1	23.2	21.5
14	SA14A	15.6	17.2	1	1	21.5	23.2
15	***SA15A***	16.7	18.5	1	1	20.6	24.4
16	SA16A	17.8	19.7	1	1	19.2	26
17	SA17A	18.9	20.9	1	1	18.1	27.6

(1) Steady state power dissipation = 3 watt max rating
(2) For bidirectional types use CA suffix, ***SA6.5CA, SA12CA, SA13CA and SA15CA*** are Motorola preferred devices. Have cathode polarity band on each end. (Consult factory for availability).

Devices listed in bold, italic are Motorola preferred devices.

TVS
Axial Leaded for Through–hole Designs (continued)

Table 1. Peak Power Dissipation(1) (*500 Watts* @ 1 ms Surge – Figure 1)
Case 59–04 — Mini Mosorb (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) V_F = 3.5 V Max, I_F = 35 A Pulse (except bidirectional devices).

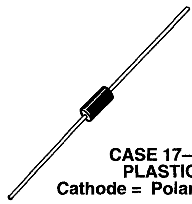
Working Peak Reverse Voltage V_{RWM} (Volts)	Device(2)	Breakdown Voltage V_{BR} (Volts) Min	Breakdown Voltage V_{BR} (Volts) Max	@ I_T Pulse (mA)	Maximum Reverse Leakage @ V_{RWM} I_R (µA)	Maximum Reverse Surge Current I_{RSM} Figure 1 (Amps)	Maximum Reverse Voltage @ I_{RSM} (Clamping Voltage) V_{RSM} (Volts)
20	SA20A	22.2	24.5	1	1	15.4	32.4
24	SA24A	26.7	29.5	1	1	12.8	38.9
26	SA26A	28.9	31.9	1	1	11.9	42.1
28	SA28A	31.1	34.4	1	1	11	45.4
30	SA30A	33.3	36.8	1	1	10.3	48.4
36	SA36A	40	44.2	1	1	8.6	58.1
51	SA51A	56.7	62.7	1	1	6.1	82.4
58	SA58A	64.4	71.2	1	1	5.3	93.6
60	SA60A	66.7	73.7	1	1	5.2	96.8
75	SA75A	83.3	92.1	1	1	4.1	121
78	SA78A	86.7	95.8	1	1	4	126
90	***SA90A***	100	111	1	1	3.4	146
110	SA110A	122	135	1	1	2.8	177
130	SA130A	144	159	1	1	2.4	209
160	SA160A	178	197	1	1	1.9	259
170	SA170A	189	209	1	1	1.8	275

(1) Steady state power dissipation = 3 watt max rating
(2) For bidirectional types, use CA suffix.
Have cathode polarity band on each end. (Consult factory for availability).

Devices listed in bold, italic are Motorola preferred devices.

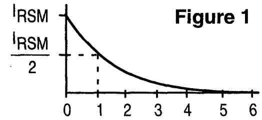
TVS
Axial Leaded for Through–hole Designs (continued)

Table 2. Peak Power Dissipation(2) (*600 Watts* @ 1 ms Surge – Figure 1)
Case 17–02 — Surmetic 40



CASE 17–02
PLASTIC
Cathode = Polarity Band

Figure 1



Surge Current Characteristics

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) V_F = 3.5 V Max, I_F = 50 A Pulse (except bidirectional devices).

Breakdown Voltage(3) V_{BR} (Volts) Nom	@ I_T Pulse (mA)	Device(1, 4)	Working Peak Reverse Voltage V_{RWM} (Volts)	Maximum Reverse Leakage @ V_{RWM} I_R (μA)	Maximum Reverse Surge Current I_{RSM} Figure 1 (Amps)	Maximum Reverse Voltage @ I_{RSM} (Clamping Voltage) V_{RSM} (Volts)
6.8	10	***P6KE6.8A***	5.8	1000	57	10.5
7.5	10	P6KE7.5A	6.4	500	53	11.3
8.2	10	P6KE8.2A	7.02	200	50	12.1
9.1	1	P6KE9.1A	7.78	50	45	13.4
10	1	P6KE10A	8.55	10	41	14.5
11	1	P6KE11A	9.4	5	38	15.6
12	1	P6KE12A	10.2	5	36	16.7
13	1	P6KE13A	11.1	5	33	18.2
15	1	***P6KE15A***	12.8	5	28	21.2
16	1	P6KE16A	13.6	5	27	22.5
18	1	P6KE18A	15.3	5	24	25.2
20	1	P6KE20A	17.1	5	22	27.7
22	1	P6KE22A	18.8	5	20	30.6
24	1	P6KE24A	20.5	5	18	33.2
27	1	P6KE27A	23.1	5	16	37.5
30	1	P6KE30A	25.6	5	14.4	41.4
33	1	P6KE33A	28.2	5	13.2	45.7
36	1	P6KE36A	30.8	5	12	49.9
39	1	P6KE39A	33.3	5	11.2	53.9
43	1	P6KE43A	36.8	5	10.1	59.3
47	1	P6KE47A	40.2	5	9.3	64.8
51	1	P6KE51A	43.6	5	8.6	70.1
56	1	P6KE56A	47.8	5	7.8	77
62	1	P6KE62A	53	5	7.1	85
68	1	P6KE68A	58.1	5	6.5	92
75	1	P6KE75A	64.1	5	5.8	103
82	1	P6KE82A	70.1	5	5.3	113
91	1	P6KE91A	77.8	5	4.8	125
120	1	P6KE120A	102	5	3.6	165

(1) For bidirectional types use CA suffix, ***P6KE7.5CA*** and ***P6KE11CA*** are Motorola preferred devices. Have cathode polarity band on each end. (Consult factory for availability).
(2) Steady state power dissipation = 5 watt max rating.
(3) Breakdown voltage tolerance is ±5% for A suffix.
(4) UL recognition for classification of protectors (QVGV2) under the UL standard for safety 497B and file #E116110 for entire series including CA suffixes.

Devices listed in bold, italic are Motorola preferred devices.

Table 2. Peak Power Dissipation(2) (*600 Watts* @ 1 ms Surge – Figure 1)
Case 17–02 — Surmetic 40 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) V_F = 3.5 V Max, I_F = 50 A Pulse (except bidirectional devices).

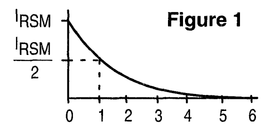
Breakdown Voltage(3) V_{BR} (Volts) Nom	@ I_T Pulse (mA)	Device(1, 4)	Working Peak Reverse Voltage V_{RWM} (Volts)	Maximum Reverse Leakage @ V_{RWM} I_R (μA)	Maximum Reverse Surge Current I_{RSM} Figure 1 (Amps)	Maximum Reverse Voltage @ I_{RSM} (Clamping Voltage) V_{RSM} (Volts)
130	1	P6KE130A	111	5	3.3	179
150	1	P6KE150A	128	5	2.9	207
160	1	P6KE160A	136	5	2.7	219
180	1	P6KE180A	154	5	2.4	246
200	1	P6KE200A	171	5	2.2	274

(1) For bidirectional types use CA suffix. Have cathode polarity band on each end. (Consult factory for availability).
(2) Steady state power dissipation = 5 watt max rating.
(3) Breakdown voltage tolerance is ±5% for A suffix.
(4) UL recognition for classification of protectors (QVGV2) under the UL standard for safety 497B and file #E116110 for entire series including CA suffixes.

Table 3. Peak Power Dissipation(1) (*1500 WATTS* @ 1 ms Surge – Figure 1)
Case 41A–02 — Mosorb

CASE 41A–02
PLASTIC
Cathode = Polarity Band

Figure 1



Time ⟶ (ms)
Surge Current Characteristics

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) V_F = 3.5 V Max, I_F = 100 A Pulse)
(C suffix denotes standard back to back bidirectional versions. Test both polarities)

Maximum Reverse Stand–Off Voltage V_{RWM} (Volts)	JEDEC(2) Device	Device(2)	Breakdown Voltage V_{BR} Volts Min	Breakdown Voltage @ I_T Pulse (mA)	Maximum Reverse Leakage @ V_{RWM} I_R (μA)	Maximum Reverse Surge Current Figure 1 I_{RSM} (Volts)	Maximum Reverse Voltage @ I_{RSM} (Clamping Voltage) V_{RSM} (Volts)	Clamping Voltage(3) Peak Pulse Current @ I_{pp1} = 1 A Figure 1 V_{C1} (Volts max)	Clamping Voltage(3) Peak Pulse Current @ I_{pp2} = 10 A Figure 1 V_{C2} (Volts max)
5	**1N5908**		6	1	300	120	8.5	7.6 @ 30 A	8 @ 60 A
5	**1N6373**	***ICTE–5***/MPTE–5	6	1	300	160	9.4	7.1	7.5
8	1N6374	ICTE–8/MPTE–8	9.4	1	25	100	15	11.3	11.5
8	1N6382	ICTE–8C/MPTE–8C	9.4	1	25	100	15	11.4	11.6
10	1N6375	ICTE–10/MPTE–10	11.7	1	2	90	16.7	13.7	14.1
10	1N6383	ICTE–10C/MPTE–10C	11.7	1	2	90	16.7	14.1	14.5
12	1N6376	ICTE–12/MPTE–12	14.1	1	2	70	21.2	16.1	16.5
12	1N6384	ICTE–12C/MPTE–12C	14.1	1	2	70	21.2	16.7	17.1
15	1N6377	ICTE–15/MPTE–15	17.6	1	2	60	25	20.1	20.6
15	1N6385	ICTE–15C/MPTE–15C	17.6	1	2	60	25	20.8	21.4
18	1N6378	ICTE–18/MPTE–18	21.2	1	2	50	30	24.2	25.2
18	1N6386	ICTE–18C/MPTE–18C	21.2	1	2	50	30	24.8	25.5
22	1N6379	ICTE–22/MPTE–22	25.9	1	2	40	37.5	29.8	32
36	1N6380	ICTE–36/MPTE–36	42.4	1	2	23	65.2	50.6	54.3
36	1N6388	ICTE–36C/MPTE–36C	42.4	1	2	23	65.2	50.6	54.3
45	1N6381	ICTE–45/MPTE–45	52.9	1	2	19	78.9	63.3	70
45	1N6389	ICTE–45C/MPTE–45C	52.9	1	2	19	78.9	63.3	70

(1) Steady state power dissipation = 5 watts max rating.
(2) 1N6382 thru 1N6389 and C suffix ICTE/MPTE device types are bidirectional. Have cathode polarity band on each end. All other device types are unidirectional only. (Consult factory for availability)
(3) Clamping voltage peak pulse currents for 1N5908 are 30 Amps and 60 Amps.

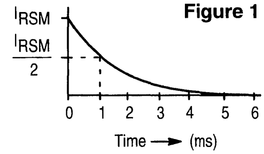
Devices listed in bold, italic are Motorola preferred devices.

TVS
Axial Leaded for Through–hole Designs (continued)

Table 4. Peak Power Dissipation(1) ***(1500 Watts*** **@ 1 ms Surge – Figure 1)**
Case 41A–02 – Mosorb

CASE 41A–02
PLASTIC
Cathode = Polarity Band

Figure 1



Surge Current Characteristics

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) V_F = 3.5 V Max, I_F = 100 A Pulse

Breakdown Voltage(2) V_{BR} Volts Nom	Breakdown Voltage(2) @ I_T Pulse (mA)	JEDEC Device	Device(3, 4)	Working Peak Reverse Voltage V_{RWM} (Volts)	Maximum Reverse Leakage @ V_{RWM} I_R (µA)	Maximum Reverse Surge Current Figure 1 I_{RSM} (Amps)	Maximum Reverse Voltage @ I_{RSM} (Clamping Voltage) V_{RSM} (Volts)
6.8	10	***1N6267A***	1.5KE6.8A	5.8	1000	143	10.5
7.5	10	1N6268A	1.5KE7.5A	6.4	500	132	11.3
8.2	10	1N6269A	1.5KE8.2A	7.02	200	124	12.1
10	1	1N6271A	1.5KE10A	8.55	10	103	14.5
11	1	1N6272A	1.5KE11A	9.4	5	96	15.6
12	1	1N6273A	1.5KE12A	10.2	5	90	16.7
13	1	1N6274A	1.5KE13A	11.1	5	82	18.2
15	1	***1N6275A***	1.5KE15A	12.8	5	71	21.2
16	1	1N6276A	1.5KE16A	13.6	5	67	22.5
18	1	1N6277A	1.5KE18A	15.3	5	59.5	25.2
20	1	1N6278A	1.5KE20A	17.1	5	54	27.7
22	1	1N6279A	***1.5KE22A***	18.8	5	49	30.6
24	1	***1N6280A***	1.5KE24A	20.5	5	45	33.2
27	1	***1N6281A***	1.5KE27A	23.1	5	40	37.5
30	1	***1N6282A***	1.5KE30A	25.6	5	36	41.4
33	1	***1N6283A***	1.5KE33A	28.2	5	33	45.7
36	1	1N6284A	1.5KE36A	30.8	5	30	49.9
39	1	***1N6285A***	***1.5KE39A***	33.3	5	28	53.9
43	1	1N6286A	1.5KE43A	36.8	5	25.3	59.3
47	1	1N6287A	1.5KE47A	40.2	5	23.2	64.8
51	1	***1N6288A***	1.5KE51A	43.6	5	21.4	70.1
56	1	1N6289A	1.5KE56A	47.8	5	19.5	77
62	1	1N6290A	1.5KE62A	53	5	17.7	85
68	1	1N6291A	1.5KE68A	58.1	5	16.3	92
75	1	1N6292A	1.5KE75A	64.1	5	14.6	103
82	1	1N6293A	1.5KE82A	70.1	5	13.3	113
91	1	1N6294A	1.5KE91A	77.8	5	12	125
100	1	1N6295A	1.5KE100A	85.5	5	11	137
110	1	1N6296A	1.5KE110A	94	5	9.9	152
120	1	1N6297A	1.5KE120A	102	5	9.1	165
130	1	1N6298A	1.5KE130A	111	5	8.4	179

(1) Steady state power dissipation = 5 watts max rating.
(2) Breakdown voltage tolerance is ±5% for A suffix.
(3) For bidirectional types use CA suffix on 1.5KE series only. Have cathode polarity band on each end. (Consult factory for availability)
1N6267–6303A series do not have CA option since the CA is not included in EIA Registration.
(4) UL recognition for classification of protectors (QVGV2) under the UL standard for safety 497B and file #E116110 for 1.5KE6.8A,CA thru 1.5KE250A,CA.

Devices listed in bold, italic are Motorola preferred devices.

TVS
Axial Leaded for Through–hole Designs (continued)

Table 4. Peak Power Dissipation(1) ***(1500 Watts*** **@ 1 ms Surge – Figure 1)**
Case 41A–02 – Mosorb (continued)

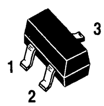
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) V_F = 3.5 V Max, I_F = 100 A Pulse

Breakdown Voltage(2)							
V_{BR} Volts Nom	@ I_T Pulse (mA)	JEDEC Device	Device(3, 4)	Working Peak Reverse Voltage V_{RWM} (Volts)	Maximum Reverse Leakage @ V_{RWM} I_R (μA)	Maximum Reverse Surge Current Figure 1 I_{RSM} (Amps)	Maximum Reverse Voltage @ I_{RSM} (Clamping Voltage) V_{RSM} (Volts)
150	1	1N6299A	1.5KE150A	128	5	7.2	207
160	1	1N6300A	1.5KE160A	136	5	6.8	219
170	1	1N6301A	1.5KE170A	145	5	6.4	234
180	1	1N6302A	1.5KE180A	154	5	6.1	246
200	1	1N6303A	1.5KE200A	171	5	5.5	274
220	1		1.5KE220A	185	5	4.6	328
250	1		1.5KE250A	214	5	5	344

(1) Steady state power dissipation = 5 watts max rating.
(2) Breakdown voltage tolerance is ±5% for A suffix.
(3) For bidirectional types use CA suffix. Have cathode polarity band on each end. (Consult factory for availability).
1N6267–6303A series do not have CA option since the CA is not included in EIA Registration.
(4) UL recognition for classification of protectors (QVGV2) under the UL standard for safety 497B and file #E116110 for 1.5KE6.8A,CA thru 1.5KE250A,CA.

Surface Mount Packages

Table 5. Peak Power Dissipation (*40 Watts* @ 1 ms Surge – Figure 1)(1)
Case 318–08 — Common Cathode
***MMBZ15VDLT1, MMBZ27VCLT1*(2) — SOT–23 Dual Monolithic Common Cathode Bipolar Zener (for ESD protection)**



CASE 318-08, STYLE 9
TO-236AB
LOW PROFILE SOT-23
PLASTIC

Pinout: TERMINAL 1 — ANODE
TERMINAL 2 — ANODE
TERMINAL 3 — COMMON CATHODE

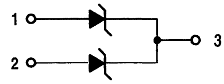
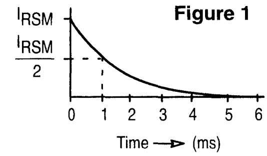


Figure 1

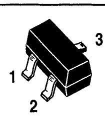


Surge Current Characteristics

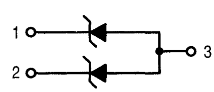
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)
BIDIRECTIONAL (Circuit tied to pins 1 and 2)

Breakdown Voltage V_{BR}(3) (Volts) Min	Nom	Max	@ I_T (mA)	Working Peak Reverse Voltage V_{RWM} (Volts)	Maximum Reverse Leakage Current I_{RWM} I_R (nA)	Maximum Reverse Surge Current I_{RSM} (Amps)	Maximum Reverse Voltage @ I_{RMS} (Clamping Voltage) V_{RSM} (Volts)	Maximum Temperature Coefficient of V_{BR} (mV/°C)
14.3	15	15.8	1.0	12.8	100	1.9	21.2	12
25.65	27	28.35	1.0	22	50	1.0	38	26

Table 6. Peak Power Dissipation (*24 Watts* @ 1 ms Surge – Figure 1)(1)
Case 318–08 — Common Anode
***MMBZ5V6ALT1, MMBZ6V2ALT1, MMBZ15ALT1,MMBZ20ALT1*(2) — SOT–23 Dual Monolithic Common Anode Zener (for ESD Protection)**

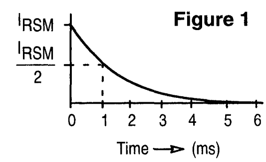


CASE 318-08, STYLE 12
TO-236AB
LOW PROFILE SOT-23
PLASTIC



PIN 1. CATHODE
2. CATHODE
3. COMMON ANODE

Figure 1



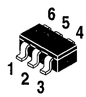
Surge Current Characteristics

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)
UNIDIRECTIONAL (Circuit tied to pins 1 and 3 or Pins 2 and 3) (V_F = 0.9 V Max @ I_F = 10 mA)

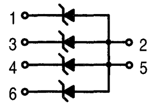
Breakdown Voltage				Max Reverse Leakage Current		Max Zener Impedance(4)			Max Reverse Surge Current	Max Reverse Voltage @ I_{RSM} (Clamping Voltage)	Maximum Temperature Coefficient of V_{BR}
V_{BR}(3) (Volts) Min	Nom	Max	@ I_T (mA)	I_R (µA)	@ V_R (V)	Z_{ZT} @ I_T (ΩA) (mA)	Z_{ZK} (Ω)	@ I_{ZK} (mA)	I_{RSM} (A)	V_{RSM}(V)	(mV/°C)
5.32	5.6	5.88	20	5.0	3.0	11	1600	0.25	3.0	8.0	1.26
5.89	6.2	6.51	1.0	0.5	3.0	220			2.76	8.7	2.80
14.25	15	15.75	1.0	0.05	12	100			1.9	21	12.3
19	20	21	1.0	0.05	17	100			1.4	28	17

(1) **Other voltages may be available upon request. Contact your Motorola representative.**
(2) T1 suffix designates tape and reel of 3000 units.
(3) V_{BR} measured at pulse test current I_T at an ambient temperature of 25°C.
(4) Z_{ZT} and Z_{ZK} are measured by dividing the AC voltage drop across the device by the AC current supplied.
The specified limits are $I_{Z(AC)} = 0.1\ I_{Z(DC)}$, with AC frequency = 1 kHz.

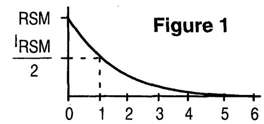
Table 7. Peak Power Dissipation (*24 Watts* @ 1 ms Surge – Figure 1)
Case 318F–01—Monolithic 4–Function Device (Available 1st Quarter 1996)
MMQA5V6T1, MMQA20VT1(1) **— SC–59 Quad Transient Voltage Suppressor (for ESD Protection)**



CASE 318F–02
SC–59
PLASTIC



PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

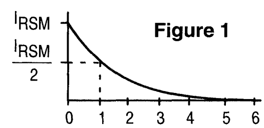
UNIDIRECTIONAL (Circuit tied to pins 1, 2, and 5; Pins 2, 3, and 5; Pins 2, 4, and 5; or Pins 2, 5, and 6) (V_F = 0.9 V Max @ I_F = 10 mA)

Breakdown Voltage V_{ZT}(2) (Volts) Min	Nom	Max	@ I_{ZT} (mA) 1	Max Reverse Leakage Current I_R (µA)	@ V_R (V)	Max Zener Impedance(3) Z_{ZT} (Ω) @ I_{ZT} (mA)	Z_{ZK} (Ω)	@ I_{ZK} (mA)	Max Reverse Surge Current I_{RSM} (A)	Max Reverse Voltage @ I_{RSM} (Clamping Voltage) V_{RSM}(V)	Maximum Temperature Coefficient of V_Z (mV/°C)
5.32	5.6	5.88	1.0	5.0	3.0	11	1600	0.25	3.0	8.0	1.26
19	20	21	1.0	0.1	15	125	600	0.25	0.84	28.6	20.07

(1) T1 suffix designates tape and reel of 3000 units.
(2) V_{BR} and V_Z are measured at pulse test current I_T at an ambient temperature of 25°C.
(3) Z_{ZT} and Z_{ZK} are measured by dividing the AC voltage drop across the device by the AC current supplied.
The specified limits are $I_{Z(AC)}$ = 0.1 $I_{Z(DC)}$, with AC frequency = 1 kHz.

Table 8. Peak Power Dissipation (*600 Watts* @ 1 ms Surge – Figure 1) Case 403A–03

SMB
CASE 403A–03
PLASTIC
Cathode = Notch



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Reverse Stand–Off V_R(Volts)(1)	Device(2, 3)	Breakdown Voltage V_{BR} @ I_T Volts Min	Pulse mA	Maximum Clamping Voltage V_C @ I_{pp} Volts	Peak Pulse Current (See Figure 1) I_{pp} Amps	Maximum Reverse Leakage @ V_R I_R µA	Device Marking
5	***1SMB5.0AT3***	6.4	10	9.2	65.2	800	KE
6	***1SMB6.0AT3***	6.67	10	10.3	58.3	800	KG
6.5	1SMB6.5AT3	7.22	10	11.2	53.6	500	KK
7	1SMB7.0AT3	7.78	10	12	50	200	KM
7.5	1SMB7.5AT3	8.33	1	12.9	46.5	100	KP
8	1SMB8.0AT3	8.89	1	13.6	44.1	50	KR

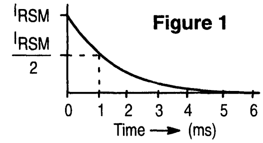
(1) A transient suppressor is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.
(2) T3 suffix designates tape and reel of 2500 units.
(3) Bidirectional version available for 1SMB10AT3 thru 1SMB78AT3, electrical characteristics apply in both directions except for V_F. Use CAT3 suffix.

Devices listed in bold, italic are Motorola preferred devices.

Table 8. Peak Power Dissipation (*600 Watts* @ 1 ms Surge – Figure 1) Case 403A–03 (continued)

SMB
CASE 403A–03
PLASTIC
Cathode = Notch

Figure 1



Surge Current Characteristics

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Reverse Stand–Off V_R(Volts)(1)	Device(2, 3)	Breakdown Voltage V_{BR} @ I_T Volts Min	Breakdown Voltage V_{BR} @ I_T Pulse mA	Maximum Clamping Voltage V_C @ I_{pp} Volts	Peak Pulse Current (See Figure 1) I_{pp} Amps	Maximum Reverse Leakage @ V_R I_R µA	Device Marking
8.5	1SMB8.5AT3	9.44	1	14.4	41.7	10	KT
9	1SMB9.0AT3	10	1	15.4	39	5	KV
10	1SMB10AT3	11.1	1	17	35.3	5	KX
11	1SMB11AT3	12.2	1	18.2	33	5	KZ
12	1SMB12AT3	13.3	1	19.9	30.2	5	LE
13	1SMB13AT3	14.4	1	21.5	27.9	5	LG
14	1SMB14AT3	15.6	1	23.2	25.8	5	LK
15	1SMB15AT3	16.7	1	24.4	24	5	LM
16	1SMB16AT3	17.8	1	26	23.1	5	LP
18	1SMB18AT3	20	1	29.2	20.5	5	LT
20	1SMB20AT3	22.2	1	32.4	18.5	5	LV
22	***1SMB22AT3***	24.4	1	35.5	16.9	5	LX
24	1SMB24AT3	26.7	1	38.9	15.4	5	LZ
26	1SMB26AT3	28.9	1	42.1	14.2	5	ME
28	1SMB28AT3	31.1	1	45.4	13.2	5	MG
30	1SMB30AT3	33.3	1	48.4	12.4	5	MK
36	1SMB36AT3	40	1	58.1	10.3	5	MP
40	1SMB40AT3	44.4	1	64.5	9.3	5	MR
43	1SMB43AT3	47.8	1	69.4	8.6	5	MT
45	1SMB45AT3	50	1	72.7	8.3	5	MV
48	1SMB48AT3	53.3	1	77.4	7.7	5	MX
51	1SMB51AT3	56.7	1	82.4	7.3	5	MZ
54	1SMB54AT3	60	1	87.1	6.9	5	NE
58	***1SMB58AT3***	64.4	1	93.6	6.4	5	NG
60	1SMB60AT3	66.7	1	96.8	6.2	5	NK
64	1SMB64AT3	71.1	1	103	5.8	5	NM
70	1SMB70AT3	77.8	1	113	5.3	5	NP
75	1SMB75AT3	83.3	1	121	4.9	5	NR
78	1SMB78AT3	86.7	1	126	4.7	5	NT
85	1SMB85AT3	94.4	1	137	4.4	5	NV
90	1SMB90AT3	100	1	146	4.1	5	NX
100	1SMB100AT3	111	1	162	3.7	5	NZ
110	1SMB110AT3	122	1	177	3.4	5	PE
120	1SMB120AT3	133	1	193	3.1	5	PG
130	1SMB130AT3	144	1	209	2.9	5	PK
150	1SMB150AT3	167	1	243	2.5	5	PM
160	1SMB160AT3	178	1	259	2.3	5	PP
170	1SMB170AT3	189	1	275	2.2	5	PR

(1) A transient suppressor is normally selected according to the reverse “Stand Off Voltage” (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.
(2) T3 suffix designates tape and reel of 2500 units.
(3) Bidirectional version available for 1SMB10AT3 thru 1SMB78AT3, electrical characteristics apply in both directions except for V_F. Use CAT3 suffix.

Devices listed in bold, italic are Motorola preferred devices.

Table 9. Peak Power Dissipation (*600 Watts* @ 1 ms Surge – Figure 1) Case 403A–03

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) V_F = 3.5 V Max, I_F[5] = 100 A for all types.

	V_{BR} @ I_T Volts				Working Peak Reverse Voltage V_{RWM} Volts	Maximum Reverse Leakage @ V_{RWM} I_R µA	Maximum Reverse Surge Current I_{RSM} Amps	Maximum Reverse Voltage @ I_{RSM} (Clamping Voltage) V_{RSM} Volts	Maximum Temperature Coefficient of V_{BR} %/°C	Device Marking
Device[3, 4]	Min	Nom	Max	mA						
P6SMB6.8AT3	***6.45***	***6.8***	***7.14***	***10***	***5.8***	***1000***	***57***	***10.5***	***0.057***	***6V8A***
P6SMB7.5AT3	***7.13***	***7.5***	***7.88***	***10***	***6.4***	***500***	***53***	***11.3***	***0.061***	***7V5A***
P6SMB9.1AT3	8.65	9.1	9.55	1	7.78	50	45	13.4	0.068	9V1A
P6SMB10AT3	***9.5***	***10***	***10.5***	***1***	***8.55***	***10***	***41***	***14.5***	***0.073***	***10A***
P6SMB12AT3	11.4	12	12.6	1	10.2	5	36	16.7	0.078	12A
P6SMB13AT3	***12.4***	***13***	***13.7***	***1***	***11.1***	***5***	***33***	***18.2***	***0.081***	***13A***
P6SMB15AT3	***14.3***	***15***	***15.8***	***1***	***12.8***	***5***	***28***	***21.2***	***0.084***	***15A***
P6SMB16AT3	***15.2***	***16***	***16.8***	***1***	***13.6***	***5***	***27***	***22.5***	***0.086***	***16A***
P6SMB18AT3	***17.1***	***18***	***18.9***	***1***	***15.3***	***5***	***24***	***25.2***	***0.088***	***18A***
P6SMB20AT3	***19***	***20***	***21***	***1***	***17.1***	***5***	***22***	***27.7***	***0.09***	***20A***
P6SMB22AT3	***20.9***	***22***	***23.1***	***1***	***18.8***	***5***	***20***	***30.6***	***0.092***	***22A***
P6SMB24AT3	22.8	24	25.2	1	20.5	5	18	33.2	0.094	24A
P6SMB27AT3	***25.7***	***27***	***28.4***	***1***	***23.1***	***5***	***16***	***37.5***	***0.096***	***27A***
P6SMB30AT3	***28.5***	***30***	***31.5***	***1***	***25.6***	***5***	***14.4***	***41.4***	***0.097***	***30A***
P6SMB33AT3	31.4	33	34.7	1	28.2	5	13.2	45.7	0.098	33A
P6SMB36AT3	***34.2***	***36***	***37.8***	***1***	***30.8***	***5***	***12***	***49.9***	***0.099***	***36A***
P6SMB39AT3	***37.1***	***39***	***41***	***1***	***33.3***	***5***	***11.2***	***53.9***	***0.1***	***39A***
P6SMB47AT3	44.7	47	49.4	1	40.2	5	9.3	64.8	0.101	47A
P6SMB51AT3	***48.5***	***51***	***53.6***	***1***	***43.6***	***5***	***8.6***	***70.1***	***0.102***	***51A***
P6SMB56AT3	***37.1***	***39***	***41***	***1***	***33.3***	***5***	***11.2***	***53.9***	***0.1***	***39A***
P6SMB62AT3	58.9	62	65.1	1	53	5	7.1	85	0.104	62A
P6SMB68AT3	64.6	68	71.4	1	58.1	5	6.5	92	0.104	68A
P6SMB82AT3	77.9	82	86.1	1	70.1	5	5.3	113	0.105	82A
P6SMB91AT3	86.5	91	95.5	1	77.8	5	4.8	125	0.106	91A
P6SMB100AT3	95	100	105	1	85.5	5	4.4	137	0.106	100A
P6SMB110AT3	105	110	116	1	94	5	4	152	0.107	110A
P6SMB120AT3	114	120	126	1	102		3	165	0.107	120A
P6SMB150AT3	143	150	158	1	128	5	2.9	207	0.108	150A
P6SMB160AT3	***152***	***160***	***168***	***1***	***136***	***5***	***2.7***	***219***	***0.108***	***160A***
P6SMB170AT3	162	170	179	1	145	5	2.6	234	0.108	170A
P6SMB180AT3	171	180	189	1	154	5	2.4	246	0.108	180A
P6SMB200AT3	190	200	210	1	171	5	2.2	274	0.108	200A

(1) Breakdown voltage tolerance is ±5% for A suffix.
(2) V_{BR} measured at pulse test current I_T at an ambient temperaure of 25°C.
(3) T3 suffix designates tape and reel of 2500 units.
(4) Bidirectional version available for P6SMB12AT3 thru P6SMB91AT3. Electrical characteristics apply in both directional except for V_F. Use CAT3 suffix.
(5) 1/2 sine wave (or equivalent square wave), PW = 8.3 ms, duty cycle = 4 pulses per minute maximum.

Devices listed in bold, italic are Motorola preferred devices.

TVS
Surface Mount Packages (continued)

Table 10. Peak Power Dissipation (*1500 Watts* @ 1 ms Surge – Figure 1) Case 403–03

SMC
CASE 403–03
PLASTIC
Cathode = Notch

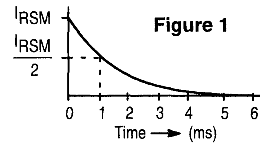


Figure 1

Surge Current Characteristics

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Device(1)	Reverse Stand-Off Voltage V_R Volts(2)	Breakdown Voltage(3) V_{BR} @ I_T Volts Min	mA	Maximum Clamping Voltage V_C @ I_{pp} Volts	Peak Pulse Current (See Figure 1) I_{pp} Amps	Maximum Reverse Leakage @ V_R I_R µA	Device Marking
1SMC5.0AT3	5.0	6.40	10	9.2	163.0	1000	GDE
1SMC6.0AT3	6.0	6.67	10	10.3	145.6	1000	GDG
1SMC6.5AT3	6.5	7.22	10	11.2	133.9	500	GDK
1SMC7.0AT3	7.0	7.78	10	12.0	125.0	200	GDM
1SMC7.5AT3	7.5	8.33	1.0	12.9	116.3	100	GDP
1SMC8.0AT3	8.0	8.89	1.0	13.6	110.3	50	GDR
1SMC8.5AT3	8.5	9.44	1.0	14.4	104.2	20	GDT
1SMC9.0AT3	9.0	10.0	1.0	15.4	97.4	10	GDV
1SMC10AT3	10	11.1	1.0	17.0	88.2	5.0	GDX
1SMC11AT3	11	12.2	1.0	18.2	82.4	5.0	GDZ
1SMC12AT3	12	13.3	1.0	19.9	75.3	5.0	GEE
1SMC13AT3	13	14.4	1.0	21.5	69.7	5.0	GEG
1SMC14AT3	14	15.6	1.0	23.2	64.7	5.0	GEK
1SMC15AT3	15	16.7	1.0	24.4	61.5	5.0	GEM
1SMC16AT3	16	17.8	1.0	26.0	57.7	5.0	GEP
1SMC17AT3	17	18.9	1.0	27.6	53.3	5.0	GER
1SMC18AT3	18	20.0	1.0	29.2	51.4	5.0	GET
1SMC20AT3	20	22.2	1.0	32.4	46.3	5.0	GEV
1SMC22AT3	22	24.4	1.0	35.5	42.2	5.0	GEX
1SMC24AT3	24	26.7	1.0	38.9	38.6	5.0	GEZ
1SMC26AT3	26	28.9	1.0	42.1	35.6	5.0	GFE
1SMC28AT3	28	31.1	1.0	45.4	33.0	5.0	GFG
1SMC30AT3	30	33.3	1.0	48.4	31.0	5.0	GFK
1SMC33AT3	33	36.7	1.0	53.3	28.1	5.0	GFM
1SMC36AT3	36	40.0	1.0	58.1	25.8	5.0	GFP
1SMC40AT3	40	44.4	1.0	64.5	23.2	5.0	GFR
1SMC43AT3	43	47.8	1.0	69.4	21.6	5.0	GFT
1SMC45AT3	45	50.0	1.0	72.7	20.6	5.0	GFV
1SMC48AT3	48	53.3	1.0	77.4	19.4	5.0	GFX
1SMC51AT3	51	56.7	1.0	82.4	18.2	5.0	GFZ
1SMC54AT3	54	60.0	1.0	87.1	17.2	5.0	GGE
1SMC58AT3	***58***	***64.4***	***1.0***	***93.6***	***16.0***	***5.0***	***GGG***
1SMC60AT3	60	66.7	1.0	96.8	15.5	5.0	GGK
1SMC64AT3	64	71.1	1.0	103	14.6	5.0	GGM
1SMC70AT3	70	77.8	1.0	113	13.3	5.0	GGP
1SMC75AT3	75	83.3	1.0	121	12.4	5.0	GGR
1SMC78AT3	78	86.7	1.0	126	11.4	5.0	GGT

(1) T3 suffix designates tape and reel of 2500 units.
(2) A transient suppressor is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.
(3) V_{BR} measured at pulse test current I_T at an ambient temperaure of 25°C.

Devices listed in bold, italic are Motorola preferred devices.

Table 11. Peak Power Dissipation (*1500 Watts* @ 1 ms Surge – Figure 1) Case 403–03

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) V_F = 3.5 V Max, I_F(3) = 100 A for all types.

Device(1)	Breakdown Voltage(2) V_{BR} @ I_T Volts Min	Nom	Max	mA	Working Peak Reverse Voltage V_{RWM} Volts	Maximum Reverse Leakage @ V_{RWM} I_R μA	Maximum Reverse Surge Current I_{RSM} Amps	Maximum Reverse Voltage @ I_{RSM} (Clamping Voltage) V_{RSM} Volts	Maximum Temperature Coefficient of V_{BR} %/°C	Device Marking
1.5SMC6.8AT3	6.45	6.8	7.14	10	5.8	1000	143	10.5	0.057	6V8A
1.5SMC8.2AT3	7.79	8.2	8.61	10	7.02	200	124	12.1	0.065	8V2A
1.5SMC9.1AT3	8.65	9.1	9.55	1	7.78	50	112	13.4	0.068	9V1A
1.5SMC10AT3	9.5	10	10.5	1	8.55	10	103	14.5	0.073	10A
1.5SMC11AT3	10.5	11	11.6	1	9.4	5	96	15.6	0.075	11A
1.5SMC12AT3	11.4	12	12.6	1	10.2	5	90	16.7	0.078	12A
1.5SMC13AT3	12.4	13	13.7	1	11.1	5	82	18.2	0.081	13A
1.5SMC15AT3	***14.3***	***15***	***15.8***	***1***	***12.8***	***5***	***71***	***21.2***	***0.084***	***15A***
1.5SMC18AT3	17.1	18	18.9	1	15.3	5	59.5	25.2	0.088	18A
1.5SMC22AT3	20.9	22	23.1	1	18.8	5	49	30.6	0.092	22A
1.5SMC24AT3	***22.8***	***24***	***25.2***	***1***	***20.5***	***5***	***45***	***33.2***	***0.094***	***24A***
1.5SMC27AT3	25.7	27	28.4	1	23.1	5	40	37.5	0.096	27A
1.5SMC30AT3	28.5	30	31.5	1	25.6	5	36	41.4	0.097	30A
1.5SMC33AT3	***31.4***	***33***	***34.7***	***1***	***28.2***	***5***	***33***	***45.7***	***0.098***	***33A***
1.5SMC36AT3	***34.2***	***36***	***37.8***	***1***	***30.8***	***5***	***30***	***49.9***	***0.099***	***36A***
1.5SMC39AT3	***37.1***	***39***	***41***	***1***	***33.3***	***5***	***28***	***53.9***	***0.1***	***39A***
1.5SMC43AT3	***40.9***	***43***	***45.2***	***1***	***36.8***	***5***	***25.3***	***59.3***	***0.101***	***43A***
1.5SMC47AT3	***44.7***	***47***	***49.4***	***1***	***40.2***	***5***	***23.2***	***64.8***	***0.101***	***47A***
1.5SMC51AT3	48.5	51	53.6	1	43.6	5	21.4	70.1	0.102	51A
1.5SMC56AT3	53.2	56	58.8	1	47.8	5	19.5	77	0.103	56A
1.5SMC62AT3	58.9	62	65.1	1	53	5	17.7	85	0.104	62A
1.5SMC68AT3	64.6	68	71.4	1	58.1	5	16.3	92	0.104	68A
1.5SMC75AT3	***71.3***	***75***	***78.8***	***1***	***64.1***	***5***	***14.6***	***103***	***0.105***	***75A***
1.5SMC82AT3	77.9	82	86.1	1	70.1	5	13.3	113	0.105	82A
1.5SMC91AT3	86.5	91	95.5	1	77.8	5	12	125	0.106	91A

(1) T3 suffix designates tape and reel of 2500 units.
(2) V_{BR} measured at pulse test current I_T at an ambient temperaure of 25°C.
(3) 1/2 sine wave (or equivalent square wave), PW = 8.3 ms, duty cycle = 4 pulses per minute maximum.

Devices listed in bold, italic are Motorola preferred devices.

TVS
Overvoltage Transient Suppressors

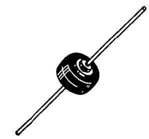
Table 12. Overvoltage Transient Suppressors

Overvoltage transient suppressors are designed for protection against over–voltage conditions in the auto electrical system including the "LOAD DUMP" phenomenon that occurs when the battery open circuits while the car is running.

OVERVOLTAGE TRANSIENT SUPPRESSOR	
	CASE 194–04 *MR2535L*
V_{RRM} (Volts)	20
I_O (Amp)	35
$V_{(BR)}$ (Volts)	24–32
I_{RSM}(30) (Amp)	110
T_C @ Rated I_O (°C)	150
T (°C)	175

(30) Time constant = 10 ms, duty cycle ≤ 1%, T_C = 25°C.
Note: MR2535L is considered part of the rectifier product portfolio.

CASE 194–04

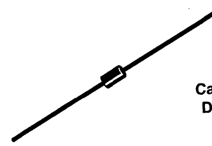


Devices listed in bold, italic are Motorola preferred devices.

Zener Diodes

Voltage Regulator Diodes

Table 13. Axial Leaded for Through–hole Designs – 500 mW

Nominal Zener Breakdown Voltage	500 mW Cathode = Polarity Band	500 mW Low Level Cathode = Polarity Band	500 mW Cathode = Polarity Band					500 mW Low Level Cathode = Polarity Band	500 mW Cathode = Polarity Band	
(*Note 1)	(*Note 2)	(*Note 3)	(*Note 4)	(*Note 5)	(*Note 6)	(*Note 7)	(*Note 8)	(*Note 9)	(*Note 10)	(*Note 8)
Volts	 Glass Case 299–02 DO–204AH (DO–35)									
1.8		1N4678						MZ4614		
2.0		1N4679						MZ4615		
2.2								MZ4616		
2.4	1N4370A	1N4681	1N5221B	1N5985B	BZX55C2V4RL	BZX79C2V4RL		MZ4617		
2.5			1N5222B							
2.7	1N4371A	1N4682	1N5223B		BZX55C2V7RL	BZX79C2V7RL		MZ4618		ZPD2.7RL
2.8										
3.0	1N4372A	1N4683	1N5225B	1N5987B	BZX55C3V0RL	BZX79C3V0RL		MZ4619		
3.3	***1N746A***	1N4684	***1N5226B***	1N5988B	BZX55C3V3RL	BZX79C3V3RL	BZX83C3V3RL	MZ4620		
3.6	1N747A	1N4685	1N5227B	1N5989B	BZX55C3V6RL	BZX79C3V6RL	BZX83C3V6RL			ZPD3.6RL
3.9	1N748A	1N4686	***1N5228B***	1N5990B	BZX55C3V9RL			MZ4622	MZ5520B	
4.3	1N749A	1N4687	1N5229B	1N5991B	BZX55C4V3RL	BZX79C4V3RL		MZ4623	MZ5521B	
4.7	1N750A	***1N4688***	1N5230B	1N5992B	BZX55C4V7RL	BZX79C4V7RL	BZX83C4V7RL	MZ4624		ZPD4.7RL
5.1	***1N751A***	1N4689	***1N5231B***	***1N5993B***	BZX55C5V1RL	BZX79C5V1RL	BZX83C5V1RL	MZ4625	MZ5523B	ZPD5.1RL
5.6	***1N752A***	1N4690	***1N5232B***	***1N5994B***	BZX55C5V6RL	BZX79C5V6RL		MZ4626	MZ5524B	
6.0			1N5233B							
6.2	***1N753A***	1N4691	***1N5234B***	1N5995B	BZX55C6V2RL	BZX79C6V2RL	BZX83C6V2RL	MZ4627	MZ5525B	ZPD6.2RL
6.8	1N754A 1N957B	1N4692	***1N5235B***	1N5996B	BZX55C6V8RL	BZX79C6V8RL		MZ4099		
7.5	1N755A	1N4693	1N5236B	1N5997B	BZX55C7V5RL				MZ5527B	
8.2	1N756A 1N959B	1N4694	***1N5237B***	***1N5998B***	BZX55C8V2RL	BZX79C8V2RL		MZ4101		
8.7		1N4695								
9.1	1N757A	1N4696	1N5239B	1N5999B	BZX55C9V1RL				MZ5529B	
10	1N758A 1N961B	1N4697	***1N5240B***	1N6000B	BZX55C10RL			MZ4104		
11	1N962B	1N4698	1N5241B		BZX55C11RL					
12	1N759A 1N963B	1N4699	***1N5242B***	1N6002B	BZX55C12RL	BZX79C12RL	BZX83C12RL			
13	1N964B	1N4700	1N5243B	1N6003B	BZX55C13RL					
14			1N5244B							
15	1N965B	1N4702	***1N5245B***	1N6004B	BZX55C15RL	BZX79C15RL				
16	1N966B	1N4703	***1N5246B***		BZX55C16RL	BZX79C16RL				
17		1N4704	1N5247B							
18	1N967B	1N4705	1N5248B							

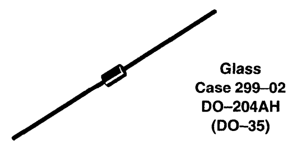
*See Notes on page 5.2–20.

Devices listed in bold, italic are Motorola preferred devices.

Zener Diodes
Voltage Regulator Diodes (continued)

Table 13. Axial Leaded for Through–hole Designs – 500 mW (continued)

Nominal Zener Breakdown Voltage	500 mW Cathode = Polarity Band	500 mW Low Level Cathode = Polarity Band	500 mW Cathode = Polarity Band					500 mW Low Level Cathode = Polarity Band	500 mW Cathode = Polarity Band	
(*Note 1)	(*Note 2)	(*Note 3)	(*Note 4)	(*Note 5)	(*Note 6)	(*Note 7)	(*Note 8)	(*Note 9)	(*Note 10)	(*Note 8)
Volts										
19			1N5249B							
20	1N968B	1N4707	***1N5250B***	1N6007B	BZX55C20RL					
22	1N969B	1N4708	1N5251B							
24	1N970B		1N5252B							
25										
27	1N971B		1N5254B		BZX55C27RL					ZPD27RL
28			1N5255B							
30	1N972B		1N5256B							ZPD30RL
33	1N973B		1N5257B			BZX79C33RL				
36	1N974B		1N5258B							
39	1N975B		1N5259B							
43	1N976B		1N5260B							
47	1N977B		1N5261B							
51	1N978B		1N5262B		BZX55C51RL					
56			1N5263B			BZX79C56RL				
60			1N5264B							
62	1N980B		1N5265B							
68	1N981B		1N5266B		BZX55C68RL					
75	1N982B		1N5267B		BZX55C75RL					
82					BZX55C82RL					
87										
91			1N5270B	1N6023B	BZX55C91RL					
100	1N985B		1N5271B			BZX79C100RL				
110	1N986B		1N5272B							
120	1N987B		1N5273B							
130	1N988B		1N5274B							
140			1N5275B							
150	1N989B		1N5276B							
160										
170										
180	1N991B		1N5279B							
190										
200	1N992B		1N5281B							
220										
240										
270										
300										
330										
360										
400										

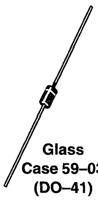
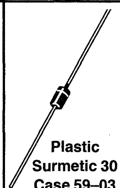
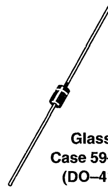
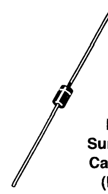
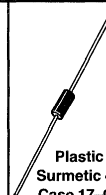


*See Notes on page 5.2–20.

Devices listed in bold, italic are Motorola preferred devices.

Zener Diodes
Voltage Regulator Diodes (continued)

Table 14. Axial Leaded for Through–hole Designs – 1, 1.3, 1.5, 3 and 5 Watt

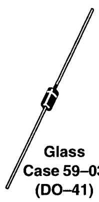
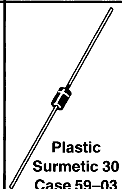
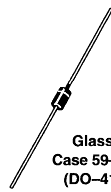
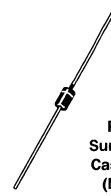
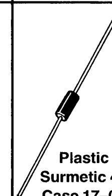
Nominal Zener Breakdown Voltage	1 Watt Cathode = Polarity Band		1.3 Watt Cathode = Polarity Band			1.5 Watt Cathode = Polarity Band	3 Watt Cathode = Polarity Band	5 Watt Cathode = Polarity Band
(*Note 1)	(*Note 11)	(*Note 12)	(*Note 13)	(*Note 14)	(*Note 15)	(*Note 16)	(*Note 17)	(*Note 18)
Volts	 Glass Case 59–03 (DO–41)	 Plastic Surmetic 30 Case 59–03 (DO–41)	 Glass Case 59–03 (DO–41)			 Plastic Surmetic 30 Case 59–03 (DO–41)		 Plastic Surmetic 40 Case 17–02
3.3	1N4728A	MZP4728A	BZX85C3V3RL			1N5913B		1N5333B
3.6	1N4729A	MZP4729A	***BZX85C3V6RL***					1N5334B
3.9	1N4730A		BZX85C3V9RL	MZPY3.9RL	MZD3.9RL			1N5335B
4.3	1N4731A				MZD4.3RL		***3EZ4.3D5***	1N5336B
4.7	1N4732A				MZD4.7RL	1N5917B		1N5337B
5.1	***1N4733A***		BZX85C5V1RL	MZPY5.1RL	MZD5.1RL			1N5338B
5.6	***1N4734A***	MZP4734A	BZX85C5V6RL	MZPY5.6RL	MZD5.6RL			1N5339B
6.0								1N5340B
6.2	***1N4735A***	MZP4735A			MZD6.2RL	***1N5920B***		1N5341B
6.8	***1N4736A***		BZX85C6V8RL	MZPY6.8RL	MZD6.8RL	1N5921B		1N5342B
7.5	1N4737A	MZP4737A	BZX85C7V5RL	MZPY7.5RL	MZD7.5RL	1N5922B	3EZ7.5D5	1N5343B
8.2	***1N4738A***	MZP4738A	BZX85C8V2RL	MZPY8.2RL	MZD8.2RL		3EZ8.2D5	1N5344B
8.7								
9.1	1N4739A				MZD9.1RL	1N5924B	3EZ9.1D5	1N5346B
10	***1N4740A***	MZP4740A	BZX85C10RL	MZPY10RL	MZD10RL	1N5925B	3EZ10D5	1N5347B
11	***1N4741A***	MZP4741A		MZPY11RL	MZD11RL		3EZ11D5	1N5348B
12	***1N4742A***		BZX85C12RL	MZPY12RL	MZD12RL	1N5927B		1N5349B
13	1N4743A				MZD13RL		3EZ13D5	1N5350B
14							3EZ14D5	1N5351B
15	***1N4744A***	MZP4744A	BZX85C15RL	MZPY15RL	MZD15RL	***1N5929 B***		1N5352B
16	***1N4745A***	MZP4745A			MZD16RL	1N5930B		1N5353B
17								1N5354B
18	***1N4746A***	***MZP4746A***	BZX85C18RL	MZPY18RL	***MZD18RL***	1N5931B		1N5355B
19							3EZ19D5	1N5356B
20	***1N4747A***				MZD20RL			1N5357B
22	***1N4748A***		***BZX85C22RL***	MZPY22RL	MZD22RL	1N5933B	3EZ22D5	1N5358B
24	***1N4749A***	***MZP4749A***	***BZX85C24RL***	MZPY24RL	MZD24RL			1N5359B
25								1N5360B
27	***1N4750A***	MZP4750A	BZX85C27RL	MZPY27RL	MZD27RL	1N5935B	3EZ27D5	1N5361B
28							3EZ28D5	1N5362B
30	***1N4751A***	***MZP4751A***	BZX85C30RL		MZD30RL			1N5363B
33	***1N4752A***	MZP4752A	BZX85C33RL		MZD33RL		3EZ33D5	1N5364B
36	1N4753A	MZP4753A			MZD36RL	1N5938B	3EZ36D5	1N5365B
39	1N4754A				MZD39RL	1N5939B		1N5366B
43	1N4755A		BZX85C43RL	MZPY43RL	MZD43RL		3EZ43D5	1N5367B
47	1N4756A		BZX85C47RL	MZPY47RL	MZD47RL	1N5941B	3EZ47D5	1N5368B
51	1N4757A				MZD51			1N5369B
56	1N4758A				MZD56	1N5943B	3EZ56D5	1N5370B
60								1N5371B
62	1N4759A				MZD62			1N5372B
68	1N4760A				MZD68		3EZ68D5	1N5373B

*See Notes on page 5.2–20.

Devices listed in bold, italic are Motorola preferred devices.

Zener Diodes
Voltage Regulator Diodes (continued)

Table 14. Axial Leaded for Through–hole Designs – 1, 1.3, 1.5, 3 and 5 Watt (continued)

Nominal Zener Breakdown Voltage	1 Watt Cathode = Polarity Band		1.3 Watt Cathode = Polarity Band			1.5 Watt Cathode = Polarity Band	3 Watt Cathode = Polarity Band	5 Watt Cathode = Polarity Band
(*Note 1)	(*Note 11)	(*Note 12)	(*Note 13)	(*Note 14)	(*Note 15)	(*Note 16)	(*Note 17)	(*Note 18)
Volts	 Glass Case 59–03 (DO–41)	 Plastic Surmetic 30 Case 59–03 (DO–41)	 Glass Case 59–03 (DO–41)		 Plastic Surmetic 30 Case 59–03 (DO–41)			 Plastic Surmetic 40 Case 17–02
75	1N4761A		BZX85C75RL		MZD75	1N5946B	3EZ75D5	1N5374B
82	1N4762A			MZPY82RL	MZD82			1N5375B
87								
91	1N4763A				MZD91		3EZ91D5	1N5377B
100	1N4764A		BZX85C100RL	MZPY100RL	MZD100			1N5378B
110					MZD110		3EZ110D5	
120					MZD120	1N5951B	3EZ120D5	1N5380B
130					MZD130		3EZ130D5	1N5381B
140							3EZ140D5	
150						1N5953B		1N5383B
160						1N5954B	3EZ160D5	1N5384B
170								
180					MZD180	***1N5955B***		1N5386B
190							3EZ190D5	
200						1N5956B	3EZ200D5	1N5388B
220							3EZ220D5	
240							3EZ240D5	
270								
300								
330							3EZ330D5	
360								
400							3EZ400D5	

*See Notes on page 5.2–20.

Devices listed in bold, italic are Motorola preferred devices.

Notes — Axial Leaded Chart

1. Zener Voltage is the key parameter for each device type. It is specified at a particular test current applied at either thermal equilibrium (T.E.) or pulse test condition. The voltage tolerance for the device types listed is, in general, ±5%; however, for some series, the voltage tolerance varies from device type to device type over a range of ±(5 to 8.5)%. Consult the complete data sheet to determine the exact test conditions and minimum/maximum limits for the zener voltage. Consult Application Note AN924 regarding measurement of Zener Voltage (pulse versus thermal equilibrium).

Power Ratings represent the capability of the case size listed as supplied by Motorola. These ratings may be higher than the JEDEC registration and/or the same device types supplied by other manufacturers. (On tight tolerance devices, please consult factory on availability.)

V_Z Test Conditions And Tolerances

2. 1N4370A/1N746A Series
   I_{ZT} = 20 mA (T.E.).
   A suffix = ±5%.
   C suffix = ±2%.
   D suffix = ±1%.

   1N957B Series
   I_{ZT} @ approximately 125 mW point (T.E.).
   B suffix = ±5%.
   C suffix = ±2%.
   D suffix = ±1%.

3. 1N4678 Series I_{ZT} = 50 µA (T.E.).
   No suffix = ±5%.
   C suffix = ±2%.
   D suffix = ±1%.
   Also has delta V_Z parameter and limit.

4. 1N5221B–42B I_{ZT} = 20 mA (T.E.).
   1N5243B–81B I_{ZT} @ approximately 125 mW point (T.E.).
   B suffix = ±5%.
   C suffix = ±2%.
   D suffix = ±1%.

5. 1N5985B–6013B I_{ZT} = 5 mA (T.E.).
   1N6017B–23B I_{ZT} = 2 mA (T.E.).
   B suffix = ±5%.
   C suffix = ±2%.
   D suffix = ±1%.

6. BZX55C2V4–C27RL I_{ZT} = 5 mA (T.E.).
   BZX55C51–C82RL I_{ZT} = 2.5 mA (T.E.).
   BZX55C91RL I_{ZT} = 1 mA (T.E.).
   C indicates ±(5 to 8.5)% depending on type number.
   Replace C with B for ±2%.

7. BZX79C2V4–C16RL I_{ZT} = 5 mA (pulse).
   BZX79C33–C56RL I_{ZT} = 2 mA (pulse).
   BZX79C100 I_{ZT} = 1 mA (pulse).
   C indicates ±(5 to 8.5)% depending on type number.
   Replace C with B for ±2%.
   Replace C with A for ±1%.

8. BZX83C3V3–C12RL I_{ZT} = 5 mA (pulse).
   ZPD2.7–30RL I_{ZT} = 5 mA (pulse).
   Tolerance is ±(5 to 8.5)% depending on type number.

9. MZ4614–27 I_{ZT} = 250 µA (T.E.).
   MZ4099–4104 I_{ZT} = 250 µA (T.E.).
   Tolerance is ±5%.

10. MZ5520B–21B I_{ZT} = 20 mA (T.E.).
    MZ5523B I_{ZT} = 5 mA (T.E.).
    MZ5524B I_{ZT} = 3 mA (T.E.).
    MZ5525B–29B I_{ZT} = 1 mA (T.E.).
    Tolerance is ±5%.
    Also has delta V_Z parameter and limit.

11. 1N4728A–64A
    I_{ZT} @ approximately 250 mW point (T.E.).
    A suffix = ±5%.
    C suffix = ±2%.
    D suffix = ±1%.

12. MZP4728A–53A
    I_{ZT} @ approximately 250 mW point (T.E.).
    MZP Series A suffix = ±5%.

13. BZX85C3V3–C100RL
    I_{ZT} varies from 185 mW to 300 mW point depending on type number (pulse).
    C indicates ±(5 to 8.5)% depending on type number.
    Replace C with B for ±2%.

14. MZPY3.9–8.2RL I_{ZT} = 100 mA (pulse).
    MZPY10–15RL I_{ZT} = 50 mA (pulse).
    MZPY18–27RL I_{ZT} = 25 mA (pulse).
    MZPY43–82RL I_{ZT} = 10 mA (pulse).
    MZPY100RL I_{ZT} = 5 mA (pulse).
    No suffix tolerance is approximately ±(5 to 8.5)% depending on type number.
    C suffix = ±2%.
    D suffix = ±1%.

15. MZD3.9–8.2 I_{ZT} = 100 mA (pulse).
    MZD9.1–15 I_{ZT} = 50 mA (pulse).
    MZD16–33 I_{ZT} = 25 mA (pulse).
    MZD36–82 I_{ZT} = 10 mA (pulse).
    MZD91–180 I_{ZT} = 5 mA (pulse).
    Tolerance is ±(5 to 8.5)% depending on type number.

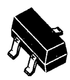
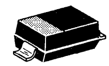
16. 1N5913B–56B
    I_{ZT} @ approximately 375 mW point (T.E.).
    B suffix = ±5%.

17. 3EZ4.3D5–400D5
    I_{ZT} @ approximately 750 mW point (pulse).
    Suffix 5 = ±5%.

18. 1N5333B–88B
    I_{ZT} varies from 0.9 to 1.5 W point depending on type number (pulse)
    B suffix = ±5%.
    Also has delta V_Z parameter and limit.

Zener Diodes
Voltage Regulator Diodes (continued)

Table 15. Surface Mount Packages

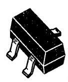
Nominal Zener Breakdown Voltage	225 mW Surface Mount SOT-23		500 mW Surface Mount SOD-123	500 mW Low Level Surface Mount SOD-123	500 mW Surface Mount SOD-123	1.5 Watt Surface Mount SMA	3 Watt Surface Mount SMB
(*Note 1)	(*Note 2)	(*Note 3)	(*Note 4)	(*Note 5)	(*Note 6)	(*Note 7)	(*Note 8)
Volts	Anode  Cathode, No Connection Plastic Case 318–08 TO-236AB			Plastic Case 425–04, Style 1		 Plastic Case 403B–01	 Plastic Case 403A–03 Cathode = Notch
1.8				MMSZ4678T1			
2.0				MMSZ4679T1			
2.2				***MMSZ4680T1***			
2.4	BZX84C2V4LT1	MMBZ5221BLT1	MMSZ2V4T1	MMSZ4681T1	***MMSZ5221BT1***		
2.5		MMBZ5222BLT1			***MMSZ5222BT1***		
2.7	BZX84C2V7LT1		MMSZ2V7T1	MMSZ4682T1	MMSZ5223BT1		
2.8					MMSZ5224BT1		
3.0	BZX84C3V0LT1	MMBZ5225BLT1	MMSZ3V0T1	MMSZ4683T1	***MMSZ5225BT1***		
3.3	BZX84C3V3LT1	MMBZ5226BLT1	MMSZ3V3T1	MMSZ4684T1	MMSZ5226BT1	1SMA5913BT3	1SMB5913BT3
3.6	BZX84C3V6LT1		MMSZ3V6T1	***MMSZ4685T1***	MMSZ5227BT1	1SMA5914BT3	
3.9	BZX84C3V9LT1	***MMBZ5228BLT1***	MMSZ3V9T1	MMSZ4686T1	MMSZ5228BT1	1SMA5915BT3	1SMB5915BT3
4.3	BZX84C4V3LT1	MMBZ5229BLT1	MMSZ4V3T1	MMSZ4687T1	***MMSZ5229BT1***	1SMA5916BT3	1SMB5916BT3
4.7	***BZX84C4V7LT1***	MMBZ5230BLT1	MMSZ4V7T1	***MMSZ4688T1***	***MMSZ5230BT1***	1SMA5917BT3	1SMB5917BT3
5.1	***BZX84C5V1LT1***	***MMBZ5231BLT1***	***MMSZ5V1T1***	***MMSZ4689T1***	***MMSZ5231BT1***	1SMA5918BT3	1SMB5918BT3
5.6	***BZX84C5V6LT1***	***MMBZ5232BLT1***	***MMSZ5V6T1***	***MMSZ4690T1***	***MMSZ5232BT1***	1SMA5919BT3	1SMB5919BT3
6.0		MMBZ5233BLT1			MMSZ5233BT1		
6.2	***BZX84C6V2LT1***	***MMBZ5234BLT1***	***MMSZ6V2T1***	MMSZ4691T1	***MMSZ5234BT1***	1SMA5920BT3	1SMB5920BT3
6.8	BZX84C6V8LT1	***MMBZ5235BLT1***	MMSZ6V8T1	MMSZ4692T1	***MMSZ5235BT1***	1SMA5921BT3	1SMB5921BT3
7.5	BZX84C7V5LT1	MMBZ5236BLT1	MMSZ7V5T1	MMSZ4693T1	MMSZ5236BT1	1SMA5922BT3	1SMB5922BT3
8.2	BZX84C8V2LT1	MMBZ5237BLT1	MMSZ8V2T1	MMSZ4694T1	MMSZ5237BT1	1SMA5923BT3	1SMB5923BT3
8.7				MMSZ4695T1	MMSZ5238BT1		
9.1	BZX84C9V1LT1	MMBZ5239BLT1	MMSZ9V1T1	MMSZ4696T1	MMSZ5239BT1	1SMA5924BT3	1SMB5924BT3
10	BZX84C10LT1	***MMBZ5240BLT1***	MMSZ10T1	MMSZ4697T1	***MMSZ5240BT1***	1SMA5925BT3	1SMB5925BT3
11	BZX84C11LT1	MMBZ5241BLT1	MMSZ11T1	MMSZ4698T1	MMSZ5241BT1	1SMA5926BT3	1SMB5926BT3
12	***BZX84C12LT1***	***MMBZ5242BL***T1	MMSZ12T1	MMSZ4699T1	***MMSZ5242BT1***	1SMA5927BT3	1SMB5927BT3
13	BZX84C13LT1	MMBZ5243BLT1	MMSZ13T1	MMSZ4700T1	MMSZ5243BT1	1SMA5928BT3	1SMB5928BT3
14		MMBZ5244BLT1		MMSZ4701T1	MMSZ5244BT1		
15	BZX84C15LT1	***MMBZ5245BLT1***	MMSZ15T1	MMSZ4702T1	***MMSZ5245BT1***	1SMA5929BT3	1SMB5929BT3
16	BZX84C16LT1	MMBZ5246BLT1	MMSZ16T1	MMSZ4703T1	***MMSZ5246BT1***	1SMA5930BT3	1SMB5930BT3
17		MMBZ5247BLT1		MMSZ4704T1	MMSZ5247BT1		
18	***BZX84C18LT1***	***MMBZ5248BLT1***	***MMSZ18T1***	MMSZ4705T1	***MMSZ5248BT1***	1SMA5931BT3	1SMB5931BT3
19		MMBZ5249BLT1		MMSZ4706T1	MMSZ5249BT1		
20	BZX84C20LT1	***MMBZ5250BLT1***	MMSZ20T1	MMSZ4707T1	***MMSZ5250BT1***	1SMA5932BT3	1SMB5932BT3
22	BZX84C22LT1	MMBZ5251BLT1	MMSZ22T1	MMSZ4708T1	MMSZ5251BT1	1SMA5933BT3	
24	BZX84C24LT1	MMBZ5252BLT1	MMSZ24T1	MMSZ4709T1	***MMSZ5252BT1***	1SMA5934BT3	1SMB5934BT3
25				MMSZ4710T1	MMSZ5253BT1		
27	BZX84C27LT1	***MMBZ5254BLT1***	MMSZ27T1	MMSZ4711T1	MMSZ5254BT1	1SMA5935BT3	1SMB5935BT3

*See Notes page 5.2–23.

Devices listed in bold, italic are Motorola preferred devices.

Zener Diodes
Voltage Regulator Diodes (continued)

Table 15. Surface Mount Packages (continued)

Nominal Zener Breakdown Voltage	225 mW Surface Mount SOT–23		500 mW Surface Mount SOD–123	500 mW Low Level Surface Mount SOD–123	500 mW Surface Mount SOD–123	1.5 Watt Surface Mount SMA	3 Watt Surface Mount SMB
(*Note 1)	(*Note 2)	(*Note 3)	(*Note 4)	(*Note 5)	(*Note 6)	(*Note 7)	(*Note 8)
Volts	Anode  Cathode No Connection Plastic Case 318–08 TO–236AB		 Plastic Case 425–04, Style 1			 Plastic Case 403B–01	 Plastic Case 403A–03 Cathode = Notch
28		MMBZ5255BLT1		MMSZ4712T1	MMSZ5255BT1		
30	BZX84C30LT1	MMBZ5256BLT1	MMSZ30T1	MMSZ4713T1	***MMSZ5256BT1***	1SMA5936BT3	1SMB5936BT3
33	BZX84C33LT1	***MMBZ5257BLT1***	MMSZ33T1	MMSZ4714T1	MMSZ5257BT1	1SMA5937BT3	1SMB5937BT3
36	BZX84C36LT1	MMBZ5258BLT1	MMSZ36T1	MMSZ4715T1	MMSZ5258BT1	1SMA5938BT3	1SMB5938BT3
39	BZX84C39LT1	MMBZ5259BLT1	***MMSZ39T1***	MMSZ4716T1	MMSZ5259BT1	1SMA5939BT3	1SMB5939BT3
43	BZX84C43LT1		MMSZ43T1	MMSZ4717T1	MMSZ5260BT1	1SMA5940BT3	1SMB5940BT3
47	BZX84C47LT1	MMBZ5261BLT1	MMSZ47T1		***MMSZ5261BT1***	1SMA5941BT3	1SMB5941BT3
51	BZX84C51LT1	MMBZ5262BLT1	MMSZ51T1		MMSZ5262BT1	1SMA5942BT3	1SMB5942BT3
56	BZX84C56LT1	MMBZ5263BLT1	MMSZ56T1		MMSZ5263BT1	1SMA5943BT3	1SMB5943BT3
60					MMSZ5264BT1		
62	BZX84C62LT1	MMBZ5265BLT1	MMSZ62T1		MMSZ5265BT1	1SMA5944BT3	1SMB5944BT3
68	BZX84C68LT1	MMBZ5266BLT1	MMSZ68T1		MMSZ5266BT1	1SMA5945BT3	1SMB5945BT3
75	BZX84C75LT1		MMSZ75T1		MMSZ5267BT1		1SMB5946BT3
82		MMBZ5268BLT1			MMSZ5268BT1		1SMB5947BT3
87		MMBZ5269BLT1			MMSZ5269BT1		
91		MMBZ5270BLT1			MMSZ5270BT1		
100					MMSZ5271BT1		1SMB5949BT3
110							1SMB5950BT3
120							1SMB5951BT3
130							1SMB5952BT3
150							1SMB5953BT3
160							1SMB5954BT3
170							
180							
200							

*See Notes on page 5.2–23.

Devices listed in bold, italic are Motorola preferred devices.

Zener Diodes

Notes — Surface Mount Chart

1. *Zener Voltage* is the key parameter for each device type. It is specified at a particular test current applied at either thermal equilibrium (T.E.) or pulse test condition. The voltage tolerance for the device types listed is, in general ±5%; however, for some series, the voltage tolerance varies from device type to device type over a range of ±(5 to 8.5)%. Consult the complete data sheet to determine the exact test conditions and minimum/maximum limits for the zener voltage.

   Power Ratings represent the capability of the case size listed as supplied by Motorola. These ratings may be higher than the same device types supplied by other manufacturers.

V_Z TEST CONDITIONS AND TOLERANCES

2. *BZX84C2V4L–C24LT1* I_{ZT} = 5 mA (pulse).
   BZX84C27L–C75LT1
   I_{ZT} = 2 mA (pulse).

   Tolerance is ±(5 to 8.5)% depending on type number. Each device type also has other V_Z min/max limits at two other I_{ZT} pulse current values.

3. *MMBZ5221BL–42BLT1* I_{ZT} = 20 mA (pulse).
   MMBZ5243BL–70BLT1
   I_{ZT} @ approximately 125 mW point (pulse).
   BL suffix = ±5%.

4. MMSZ2V4–24T1 I_{ZT} = 5 mA (pulse).
   MMSZ27–56T1 I_{ZT} = 2 mA (pulse).

   Tolerance is ±(5 to 8.5)% depending on type number. Each device type also has other V_Z min/max limits at two other I_{ZT} pulse current values.

5. *MMSZ4678T1 Series* I_{ZT} = 50 µA (T.E.).
   No suffix = ±5%.

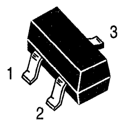
6. *MMSZ5221B–42BT1* I_{ZT} = 20 mA (T.E.).
   MMSZ5243B–63BT1
   I_{ZT} @ approximately 125 mW point (T.E.).
   A suffix = ±10%.
   B suffix = ±5%.

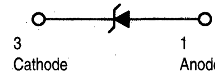
7. *1SMA5913BT3 Series*
   I_{ZT} @ approximately 375 mW point (T.E.).
   BT3 suffix = ±5%.
   T3 suffix designates tape and reel of 2500 units.

8. *1SMB5913BT3 Series*
   I_{ZT} @ approximately 750 mW point (T.E.).
   BT3 suffix = ±5%.
   T3 suffix designates tape and reel of 2500 units.

Zener Diodes

Table 16. 225 mW Rating on FR–5 Board – Case 318–08 – SOT–23





CASE 318–08, STYLE 8
SOT–23 (TO–236AB)
PLASTIC

ELECTRICAL CHARACTERISTICS (Pinout: 1–Anode, 2–NC, 3–Cathode) (V_F = 0.9 V Max @ I_F = 10 mA for all types)

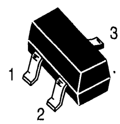
Type Number	Marking	Zener Voltage V_{Z1} (Volts) @ I_{ZT1} = 5 mA (1) Nom	Min	Max	Max Zener Impedance Z_{ZT1} (Ohms) @ I_{ZT1} = 5 mA	Max Reverse Leakage Current I_R mA	@ V_R Volts	Zener Voltage V_{Z2} (Volts) @ I_{ZT2} = 1 mA (1) Min	Max	Max Zener Impedance Z_{ZT2} (Ohms) @ I_{ZT12} = 1 mA	Zener Voltage V_{Z3} (Volts) @ I_{ZT3} = 20 mA (1) Min	Max	Max Zener Impedance Z_{ZT3} (Ohms) @ I_{ZT3} = 20 mA	d_{VZ}/dt (mV/k) @ I_{ZT1} = 5 mA Min	Max	C_{pF} Max @ V_R = 0 f = 1 MHz
BZX84C2V4LT1	Z11	2.4	2.2	2.6	100	50	1	1.7	2.1	600	2.6	3.2	50	–3.5	0	450
BZX84C2V7LT1	Z12	2.7	2.5	2.9	100	20	1	1.9	2.4	600	3	3.6	50	–3.5	0	450
BZX84C3V0LT1	Z13	3	2.8	3.2	95	10	1	2.1	2.7	600	3.3	3.9	50	–3.5	0	450
BZX84C3V3LT1	Z14	3.3	3.1	3.5	95	5	1	2.3	2.9	600	3.6	4.2	40	–3.5	0	450
BZX84C3V6LT1	Z15	3.6	3.4	3.8	90	5	1	2.7	3.3	600	3.9	4.5	40	–3.5	0	450
BZX84C3V9LT1	Z16	3.9	3.7	4.1	90	3	1	2.9	3.5	600	4.1	4.7	30	–3.5	–2.5	450
BZX84C4V3LT1	W9	4.3	4	4.6	90	3	1	3.3	4	600	4.4	5.1	30	–3.5	0	450
BZX84C4V7LT1	Z1	4.7	4.4	5	80	3	2	3.7	4.7	500	4.5	5.4	15	–3.5	0.2	260
BZX84C5V1LT1	Z2	5.1	4.8	5.4	60	2	2	4.2	5.3	480	5	5.9	15	–2.7	1.2	225
BZX84C5V6LT1	Z3	5.6	5.2	6	40	1	2	4.8	6	400	5.2	6.3	10	–2.0	2.5	200
BZX84C6V2LT1	Z4	6.2	5.8	6.6	10	3	4	5.6	6.6	150	5.8	6.8	6	0.4	3.7	185
BZX84C6V8LT1	Z5	6.8	6.4	7.2	15	2	4	6.3	7.2	80	6.4	7.4	6	1.2	4.5	155
BZX84C7V5LT1	Z6	7.5	7	7.9	15	1	5	6.9	7.9	80	7	8	6	2.5	5.3	140
BZX84C8V2LT1	Z7	8.2	7.7	8.7	15	0.7	5	7.6	8.7	80	7.7	8.8	6	3.2	6.2	135
BZX84C9V1LT1	Z8	9.1	8.5	9.6	15	0.5	6	8.4	9.6	100	8.5	9.7	8	3.8	7.0	130
BZX84C10LT1	Z9	10	9.4	10.6	20	0.2	7	9.3	10.6	150	9.4	10.7	10	4.5	8.0	130
BZX84C11LT1	Y1	11	10.4	11.6	20	0.1	8	10.2	11.6	150	10.4	11.8	10	5.4	9.0	130
BZX84C12LT1	Y2	12	11.4	12.7	25	0.1	8	11.2	12.7	150	11.4	12.9	10	6.0	10.0	130
BZX84C13LT1	Y3	13	12.4	14.1	30	0.1	8	12.3	14	170	12.5	14.2	15	7.0	11.0	120
BZX84C15LT1	Y4	15	13.8	15.6	30	0.05	10.5	13.7	15.5	200	13.9	15.7	20	9.2	13.0	110
BZX84C16LT1	Y5	16	15.3	17.1	40	0.05	11.2	15.2	17	200	15.4	17.2	20	10.4	14.0	105
BZX84C18LT1	Y6	18	16.8	19.1	45	0.05	12.6	16.7	19	225	16.9	19.2	20	12.4	16.0	100
BZX84C20LT1	Y7	20	18.8	21.2	55	0.05	14	18.7	21.1	225	18.9	21.4	20	14.4	18.0	85
BZX84C22LT1	Y8	22	20.8	23.3	55	0.05	15.4	20.7	23.2	250	20.9	23.4	25	16.4	20.0	85
BZX84C24LT1	Y9	24	22.8	25.6	70	0.05	16.8	22.7	25.5	250	22.9	25.7	25	18.4	22.0	80
		V_{Z1} Below @ I_{ZT1} = 2 mA			Z_{ZT1} Below @ I_{ZT1} = 2 mA			V_{Z2} Below @ I_{ZT2} = 0.1 mA		Z_{ZT2} Below @ I_{ZT4} = 0.5 mA (2)	V_{Z3} Below @ I_{ZT3} = 10 mA		Z_{ZT3} Below @ I_{ZT3} = 10 mA	d_{VZ}/dt (mV/k) Below @ I_{ZT1} = 2 mA		
BZX84C27LT1	Y10	27	25.1	28.9	80	0.05	18.9	25	28.9	300	25.2	29.3	45	21.4	25.3	70
BZX84C30LT1	Y11	30	28	32	80	0.05	21	27.8	32	300	28.1	32.4	50	24.4	29.4	70
BZX84C33LT1	Y12	33	31	35	80	0.05	23.1	30.8	35	325	31.1	35.4	55	27.4	33.4	70
BZX84C36LT1	Y13	36	34	38	90	0.05	25.2	33.8	38	350	34.1	38.4	60	30.4	37.4	70
BZX84C39LT1	Y14	39	37	41	130	0.05	27.3	36.7	41	350	37.1	41.5	70	33.4	41.2	45
BZX84C43LT1	Y15	43	40	46	150	0.05	30.1	39.7	46	375	40.1	46.5	80	37.6	46.6	40
BZX84C47LT1	Y16	47	44	50	170	0.05	32.9	43.7	50	375	44.1	50.5	90	42.0	51.8	40
BZX84C51LT1	Y17	51	48	54	180	0.05	35.7	47.6	54	400	48.1	54.6	100	46.6	57.2	40
BZX84C56LT1	Y18	56	52	60	200	0.05	39.2	51.5	60	425	52.1	60.8	110	52.2	63.8	40
BZX84C62LT1	Y19	62	58	66	215	0.05	43.4	57.4	66	450	58.2	67	120	58.8	71.6	35
BZX84C68LT1	Y20	68	64	72	240	0.05	47.6	63.4	72	475	64.2	73.2	130	65.6	79.8	35
BZX84C75LT1	Y21	75	70	79	255	0.05	52.5	69.4	79	500	70.3	80.2	140	73.4	88.6	35

(1) V_Z is measured with a pulse test current (I_{ZT}) applied at an ambient temperature of 25°C.
(2) The zener impedance, Z_{ZT2}, for the 27 through 75 volt types is tested at 0.5 mA rather than the test current of 0.1 mA used for V_{Z2}.

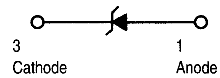
Devices listed in bold, italic are Motorola preferred devices.

Zener Diodes

Table 17. 225 mW Rating on FR–5 Board – Case 318–08 – SOT–23



CASE 318–08, STYLE 8
SOT–23 (TO–236AB)
PLASTIC



ELECTRICAL CHARACTERISTICS (Pinout: 1–Anode, 2–NC, 3–Cathode) (V_F = 0.9 V Max @ I_F = 10 mA for all types.)

Device	Marking	Test Current I_{ZT} mA	Zener Voltage V_Z (±5%) Nominal(1)	Z_{ZK} I_Z = 0.25 mA Ω Max	Z_{ZT} $I_Z = I_{ZT}$ @ 10% Mode Ω Max	Max I_R @ µA	V_R V
MMBZ5221BLT1	18A	20	2.4	1200	30	100	1
MMBZ5222BLT1	18B	20	2.5	1250	30	100	1
MMBZ5225BLT1	18E	20	3	1600	29	50	1
MMBZ5226BLT1	8A	20	3.3	1600	28	25	1
MMBZ5228BLT1	8C	20	3.9	1900	23	10	1
MMBZ5229BLT1	8D	20	4.3	2000	22	5	1
MMBZ5230BLT1	8E	20	4.7	1900	19	5	2
MMBZ5231BLT1	8F	20	5.1	1600	17	5	2
MMBZ5232BLT1	8G	20	5.6	1600	11	5	3
MMBZ5233BLT1	8H	20	6	1600	7	5	3.5
MMBZ5234BLT1	8J	20	6.2	1000	7	5	4
MMBZ5235BLT1	8K	20	6.8	750	5	3	5
MMBZ5236BLT1	8L	20	7.5	500	6	3	6
MMBZ5237BLT1	8M	20	8.2	500	8	3	6.5
MMBZ5239BLT1	8P	20	9.1	600	10	3	7
MMBZ5240BLT1	8Q	20	10	600	17	3	8
MMBZ5241BLT1	8R	20	11	600	22	2	8.4
MMBZ5242BLT1	8S	20	12	600	30	1	9.1
MMBZ5243BLT1	8T	9.5	13	600	13	0.5	9.9
MMBZ5244BLT1	8U	9	14	600	15	0.1	10
MMBZ5245BLT1	8V	8.5	15	600	16	0.1	11
MMBZ5246BLT1	8W	7.8	16	600	17	0.1	12
MMBZ5247BLT1	8X	7.4	17	600	19	0.1	13
MMBZ5248BLT1	8Y	7	18	600	21	0.1	14
MMBZ5249BLT1	8Z	6.6	19	600	23	0.1	14
MMBZ5250BLT1	81A	6.2	20	600	25	0.1	15
MMBZ5251BLT1	81B	5.6	22	600	29	0.1	17
MMBZ5252BLT1	81C	5.2	24	600	33	0.1	18
MMBZ5254BLT1	81E	4.6	27	600	41	0.1	21
MMBZ5255BLT1	81F	4.5	28	600	44	0.1	21
MMBZ5256BLT1	81G	4.2	30	600	49	0.1	23
MMBZ5257BLT1	81H	3.8	33	700	58	0.1	25
MMBZ5258BLT1	81J	3.4	36	700	70	0.1	27
MMBZ5259BLT1	81K	3.2	39	800	80	0.1	30

(1) V_Z is measured at pulse test current (I_{ZT}) at an ambient temperature of 25°C.

Devices listed in bold, italic are Motorola preferred devices.

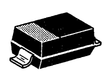
Table 17. 225 mW Rating on FR–5 Board – Case 318–08 – SOT–23 (continued)

ELECTRICAL CHARACTERISTICS (Pinout: 1–Anode, 2–NC, 3–Cathode) (V_F = 0.9 V Max @ I_F = 10 mA for all types.)

Device	Marking	Test Current I_{ZT} mA	Zener Voltage V_Z (±5%) Nominal(1)	Z_{ZK} I_Z = 0.25 mA Ω Max	Z_{ZT} $I_Z = I_{ZT}$ @ 10% Mode Ω Max	Max I_R @ µA	V_R V
MMBZ5261BLT1	81M	2.7	47	1000	105	0.1	36
MMBZ5262BLT1	81N	2.5	51	1100	125	0.1	39
MMBZ5263BLT1	81P	2.2	56	1300	150	0.1	43
MMBZ5265BLT1	81R	2	62	1400	185	0.1	47
MMBZ5266BLT1	81S	1.8	68	1600	230	0.1	52
MMBZ5268BLT1	81U	1.5	82	2000	330	0.1	62
MMBZ5269BLT1	81V	1.4	87	2200	370	0.1	68
MMBZ5270BLT1	81W	1.4	91	2300	400	0.1	69

(1) V_Z is measured at pulse test current (I_{ZT}) at an ambient temperature of 25°C.

Table 18. 500 mW Rating on FR–4 or FR–5 Board – Case 425–04 – SOD–123



CASE 425–04, STYLE 1
SOD–123
PLASTIC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted(1), (V_F = 0.9 V Max. @ I_F = 10 mA for all types)

Type Number	Marking	Zener Voltage V_Z @ I_{ZT} Volts(1,2, 3)			Test Voltage V_R	Max Zener Impedance(4)		Max Reverse Leakage Current I_R @ V_R	Test Voltage V_R
		Nom	Min	Max	Volts	Z_{ZT} @ $I_Z = I_{ZT}$ Ω	Z_{ZK} @ I_{ZK} = 0.25 mA Ω	µA	Volts
MMSZ5221BT1	C1	2.4	2.28	2.52	20	30	1200	100	1
MMSZ5222BT1	C2	2.5	2.38	2.63	20	30	1250	100	1
MMSZ5223BT1	C3	2.7	2.57	2.84	20	30	1300	75	1
MMSZ5224BT1	C4	2.8	2.66	2.94	20	30	1400	75	1
MMSZ5225BT1	C5	3.0	2.85	3.15	20	30	1600	50	1
MMSZ5226BT1	D1	3.3	3.14	3.47	20	28	1600	25	1
MMSZ5227BT1	D2	3.6	3.42	3.78	20	24	1700	15	1
MMSZ5228BT1	D3	3.9	3.71	4.10	20	23	1900	10	1
MMSZ5229BT1	D4	4.3	4.09	4.52	20	22	2000	5	1
MMSZ5230BT1	D5	4.7	4.47	4.94	20	19	1900	5	2

(1) Nominal zener voltage is measured with the device junction in thermal equilibrium at T_L = 30°C ± 1°C.
(2) All part numbers shown indicate a V_Z tolerance of ±5%.
(3) V_Z is measured at pulse test current (I_{ZT}) at an ambient temperature of 25°C.
(4) Z_{ZT} and Z_{ZK} are measured by dividing the AC voltage drop across the device by the AC current applied. The specified limits are for $I_{Z(AC)} = 0.1\ I_{Z(DC)}$, with the AC frequency = 1 kHz.

Devices listed in bold, italic are Motorola preferred devices.

Table 18. 500 mW Rating on FR–4 or FR–5 Board – Case 425–04 – SOD–123 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted(1), (V_F = 0.9 V Max. @ I_F = 10 mA for all types)

Type Number	Marking	Zener Voltage V_Z @ I_{ZT} Volts(1,2,3) Nom	Min	Max	Test Voltage V_R Volts	Max Zener Impedance(4) Z_{ZT} @ $I_Z = I_{ZT}$ Ω	Z_{ZK} @ I_{ZK} = 0.25 mA Ω	Max Reverse Leakage Current I_R @ V_R µA	Test Voltage V_R Volts
MMSZ5231BT1	E1	5.1	4.85	5.36	20	17	1600	5	2
MMSZ5232BT1	E2	5.6	5.32	5.88	20	11	1600	5	3
MMSZ5233BT1	E3	6.0	5.70	6.30	20	7	1600	5	3.5
MMSZ5234BT1	E4	6.2	5.89	6.51	20	7	1000	5	4
MMSZ5235BT1	E5	6.8	6.46	7.14	20	5	750	3	5
MMSZ5236BT1	F1	7.5	7.13	7.88	20	6	500	3	6
MMSZ5237BT1	F2	8.2	7.79	8.61	20	8	500	3	6.5
MMSZ5238BT1	F3	8.7	8.27	9.14	20	8	600	3	6.5
MMSZ5239BT1	F4	9.1	8.65	9.56	20	10	600	3	7
MMSZ5240BT1	F5	10	9.50	10.50	20	17	600	3	8
MMSZ5241BT1	H1	11	10.45	11.55	20	22	600	2	8.4
MMSZ5242BT1	H2	12	11.40	12.60	20	30	600	1	9.1
MMSZ5243BT1	H3	13	12.35	13.65	9.5	13	600	0.5	9.9
MMSZ5244BT1	H4	14	13.30	14.70	9.0	15	600	0.1	10
MMSZ5245BT1	H5	15	14.25	15.75	8.5	16	600	0.1	11
MMSZ5246BT1	J1	16	15.20	16.80	7.8	17	600	0.1	12
MMSZ5247BT1	J2	17	16.15	17.85	7.4	19	600	0.1	13
MMSZ5248BT1	J3	18	17.10	18.90	7.0	21	600	0.1	14
MMSZ5249BT1	J4	19	18.05	19.95	6.6	23	600	0.1	14
MMSZ5250BT1	J5	20	19.00	21.00	6.2	25	600	0.1	15
MMSZ5251BT1	K1	22	20.90	23.10	5.6	29	600	0.1	17
MMSZ5252BT1	K2	24	22.80	25.20	5.2	33	600	0.1	18
MMSZ5253BT1	K3	25	23.75	26.25	5.0	35	600	0.1	19
MMSZ5254BT1	K4	27	25.65	28.35	4.6	41	600	0.1	21
MMSZ5255BT1	K5	28	26.60	29.40	4.5	44	600	0.1	21
MMSZ5256BT1	M1	30	28.50	31.50	4.2	49	600	0.1	23
MMSZ5257BT1	M2	33	31.35	34.65	3.8	58	700	0.1	25
MMSZ5258BT1	M3	36	34.20	37.80	3.4	70	700	0.1	27
MMSZ5259BT1	M4	39	37.05	40.95	3.2	80	800	0.1	30
MMSZ5260BT1	M5	43	40.85	45.15	3.0	93	900	0.1	33
MMSZ5261BT1	N1	47	44.65	49.35	2.7	105	1000	0.1	36
MMSZ5262BT1	N2	51	48.45	53.55	2.5	125	1100	0.1	39
MMSZ5263BT1	N3	56	53.20	58.80	2.2	150	1300	0.1	43
MMSZ5264BT1	N4	60	57.00	63.00	2.1	170	1400	0.1	46
MMSZ5265BT1	N5	62	58.90	65.10	2.0	185	1400	0.1	47
MMSZ5266BT1	P1	68	64.60	71.40	1.8	230	1600	0.1	52
MMSZ5267BT1	P2	75	71.25	78.75	1.7	270	1700	0.1	56
MMSZ5268BT1	P3	82	77.90	86.10	1.5	330	2000	0.1	62
MMSZ5269BT1	P4	87	82.65	91.35	1.4	370	2200	0.1	68
MMSZ5270BT1	P5	91	86.45	95.55	1.4	400	2300	0.1	69

(1) Nominal zener voltage is measured with the device junction in thermal equilibrium at T_L = 30°C ± 1°C.
(2) All part numbers shown indicate a V_Z tolerance of ±5%.
(3) V_Z is measured at pulse test current (I_{ZT}) at an ambient temperature of 25°C.
(4) Z_{ZT} and Z_{ZK} are measured by dividing the AC voltage drop across the device by the AC current applied. The specified limits are for $I_{Z(AC)} = 0.1\ I_{Z(DC)}$, with the AC frequency = 1 kHz.

Devices listed in bold, italic are Motorola preferred devices.

Zener Diodes

Table 19. 500 mW Rating on FR–4 or FR–5 Board – Case 425–04 – SOD–123

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted[1]), (V_F = 0.9 V Max. @ I_F = 10 mA for all types)

Type Number	Marking	Zener Voltage V_Z @ I_{ZT} = 50 μA Volts[1, 2] Nom	Min	Max	Max Reverse Leakage Current I_R @ V_R μA	Test Voltage V_R Volts
MMSZ4678T1	CC	1.8	1.71	1.89	7.5	1
MMSZ4679T1	CD	2.0	1.90	2.10	5	1
MMSZ4680T1	CE	2.2	2.09	2.31	4	1
MMSZ4681T1	CF	2.4	2.28	2.52	2	1
MMSZ4682T1	CH	2.7	2.57	2.84	1	1
MMSZ4683T1	CJ	3.0	2.85	3.15	0.8	1
MMSZ4684T1	CK	3.3	3.14	3.47	7.5	1.5
MMSZ4685T1	CM	3.6	3.42	3.78	7.5	2
MMSZ4686T1	CN	3.9	3.71	4.10	5	2
MMSZ4687T1	CP	4.3	4.09	4.52	4	2
MMSZ4688T1	CT	4.7	4.47	4.94	10	3
MMSZ4689T1	CU	5.1	4.85	5.36	10	3
MMSZ4690T1	CV	5.6	5.32	5.88	10	4
MMSZ4691T1	CA	6.2	5.89	6.51	10	5
MMSZ4692T1	CX	6.8	6.46	7.14	10	5.1
MMSZ4693T1	CY	7.5	7.13	7.88	10	5.7
MMSZ4694T1	CZ	8.2	7.79	8.61	1	6.2
MMSZ4695T1	DC	8.7	8.27	9.14	1	6.6
MMSZ4696T1	DD	9.1	8.65	9.56	1	6.9
MMSZ4697T1	DE	10	9.50	10.50	1	7.6
MMSZ4698T1	DF	11	10.45	11.55	0.05	8.4
MMSZ4699T1	DH	12	11.40	12.60	0.05	9.1
MMSZ4700T1	DJ	13	12.35	13.65	0.05	9.8
MMSZ4701T1	DK	14	13.30	14.70	0.05	10.6
MMSZ4702T1	DM	15	14.25	15.75	0.05	11.4
MMSZ4703T1	DN	16	15.20	16.80	0.05	12.1
MMSZ4704T1	DP	17	16.15	17.85	0.05	12.9
MMSZ4705T1	DT	18	17.10	18.90	0.05	13.6
MMSZ4706T1	DU	19	18.05	19.95	0.05	14.4
MMSZ4707T1	DV	20	19.00	21.00	0.01	15.2
MMSZ4708T1	DA	22	20.90	23.10	0.01	16.7
MMSZ4709T1	DZ	24	22.80	25.20	0.01	18.2
MMSZ4710T1	DY	25	23.75	26.25	0.01	19.00
MMSZ4711T1	EA	27	25.65	28.35	0.01	20.4
MMSZ4712T1	EC	28	26.60	29.40	0.01	21.2
MMSZ4713T1	ED	30	28.50	31.50	0.01	22.8
MMSZ4714T1	EE	33	31.35	34.65	0.01	25.0
MMSZ4715T1	EF	36	34.20	37.80	0.01	27.3
MMSZ4716T1	EH	39	37.05	40.95	0.01	29.6
MMSZ4717T1	EJ	43	40.85	45.15	0.01	32.6

(1) Nominal zener voltage is measured with the device junction in thermal equilibrium at T_L = 30°C ± 1°C.
(2) All part numbers shown indicate a V_Z tolerance of ±5%.

Devices listed in bold, italic are Motorola preferred devices.

Zener Diodes

Table 20. 500 mW Rating on FR–4 or FR–5 Board — Case 425–04 — SOD–123

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted[1], (V_F = 0.9 V Max. @ I_F = 10 mA for all types)

Type Number	Marking	Zener Voltage V_{Z1} (Volts) @ I_{ZT1} = 5 mA (2, 3) Nom	Min	Max	Max Zener Impedance Z_{ZT1} @ I_{ZT1} = 5 mA (21) Ω	Max Reverse Leakage Current I_R μA	@ V_R Volts	Zener Voltage V_{Z2} (Volts) @ I_{ZT2} = 1 mA (3) Min	Max	Max Zener Impedance Z_{ZT2} @ I_{ZT1} = 1 mA (4) Ω
MMSZ2V4T1	T1	2.4	2.28	2.52	100	50	1	1.7	2.1	600
MMSZ2V7T1	T2	2.7	2.57	2.84	100	20	1	1.9	2.4	600
MMSZ3V0T1	T3	3.0	2.85	3.15	95	10	1	2.1	2.7	600
MMSZ3V3T1	T4	3.3	3.14	3.47	95	5	1	2.3	2.9	600
MMSZ3V6T1	T5	3.6	3.42	3.78	90	5	1	2.7	3.3	600
MMSZ3V9T1	U1	3.9	3.71	4.10	90	3	1	2.9	3.5	600
MMSZ4V3T1	U2	4.3	4.09	4.52	90	3	1	3.3	4.0	600
MMSZ4V7T1	U3	4.7	4.47	4.94	80	3	2	3.7	4.7	500
MMSZ5V1T1	U4	5.1	4.85	5.36	60	2	2	4.2	5.3	480
MMSZ5V6T1	U5	5.6	5.32	5.88	40	1	2	4.8	6.0	400
MMSZ6V2T1	V1	6.2	5.89	6.51	10	3	4	5.6	6.6	150
MMSZ6V8T1	V2	6.8	6.46	7.14	15	2	4	6.3	7.2	80
MMSZ7V5T1	V3	7.5	7.13	7.88	15	1	5	6.9	7.9	80
MMSZ8V2T1	V4	8.2	7.79	8.61	15	0.7	5	7.6	8.7	80
MMSZ9V1T1	V5	9.1	8.65	9.56	15	0.5	6	8.4	9.6	100
MMSZ10T1	A1	10	9.50	10.50	20	0.2	7	9.3	10.6	150
MMSZ11T1	A2	11	10.45	11.55	20	0.1	8	10.2	11.6	150
MMSZ12T1	A3	12	11.40	12.60	25	0.1	8	11.2	12.7	150
MMSZ13T1	A4	13	12.35	13.65	30	0.1	8	12.3	14.0	170
MMSZ15T1	A5	15	14.25	15.75	30	0.05	10.5	13.7	15.5	200
MMSZ16T1	X1	16	15.20	16.80	40	0.05	11.2	15.2	17.0	200
MMSZ18T1	X2	18	17.10	18.90	45	0.05	12.6	16.7	19.0	225
MMSZ20T1	X3	20	19.00	21.00	55	0.05	14	18.7	21.1	225
MMSZ22T1	X4	22	20.80	23.10	55	0.05	15.4	20.7	23.2	250
MMSZ24T1	X5	24	22.80	25.20	70	0.05	16.8	22.7	25.5	250

(1) Nominal zener voltage is measured with the device junction in thermal equilibrium at T_L = 30°C ± 1°C.
(2) All part numbers shown indicate a V_Z tolerance of ±5%.
(3) Zener voltage is measured with the zener current applied for PW = 1.0 ms.
(4) Z_{ZT} and Z_{ZK} are measured by dividing the AC voltage drop across the device by the AC current applied. The specified limits are for $I_{Z(AC)} = 0.1\ I_{Z(DC)}$, with the AC frequency = 1 kHz.

Devices listed in bold, italic are Motorola preferred devices.

Table 20. 500 mW Rating on FR–4 or FR–5 Board — Case 425–04 — SOD–123 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted(1), (V_F = 0.9 V Max. @ I_F = 10 mA for all types)

Type Number	Marking	Zener Voltage V_{Z1} (Volts) @ I_{ZT1} = 2 mA (2, 3) Nom	Min	Max	Max Zener Impedance Z_{ZT1} @ I_{ZT1} = 2 mA (4) Ω	Max Reverse Leakage Current I_R µA	@ V_R Volts	Zener Voltage V_{Z2} (Volts) @ I_{ZT2} = 0.1 mA (3) Min	Max	Max Zener Impedance Z_{ZT2} @ I_{ZT1} = 0.5 mA (4, 5) Ω
MMSZ27T1	Y1	27	25.65	28.35	80	0.05	18.9	25	28.9	300
MMSZ30T1	Y2	30	28.50	31.50	80	0.05	21	27.8	32	300
MMSZ33T1	Y3	33	31.35	34.65	80	0.05	23.1	30.8	35	325
MMSZ36T1	Y4	36	34.20	37.80	90	0.05	25.2	33.8	38	350
MMSZ39T1	Y5	39	37.05	40.95	130	0.05	27.3	36.7	41	350
MMSZ43T1	Z1	43	40.85	45.15	150	0.05	30.1	39.7	46	375
MMSZ47T1	Z2	47	44.65	49.35	170	0.05	32.9	43.7	50	375
MMSZ51T1	Z3	51	48.45	53.55	180	0.05	35.7	47.6	54	400
MMSZ56T1	Z4	56	53.20	58.80	200	0.05	39.2	51.5	60	425
MMSZ62T1	Z5	62	58.90	65.10	215	0.05	43.4	57.4	66	450
MMSZ68T1	Z6	68	64.60	71.40	240	0.05	47.6	63.4	72	475
MMSZ75T1	Z7	75	71.25	78.75	255	0.05	52.5	69.4	79	500

(1) Nominal zener voltage is measured with the device junction in thermal equilibrium at T_L = 30°C ± 1°C.
(2) All part numbers shown indicate a V_Z tolerance of ±5%
(3) Zener voltage is measured with the zener current applied for PW = 1.0 ms.
(4) Z_{ZT} and Z_{ZK} are measured by dividing the AC voltage drop across the device by the AC current applied. The specified (imits are for $I_{Z(AC)} = 0.1\ I_{Z(DC)}$, with the AC frequency = 1 kHz
(5) The zener impedance, Z_{ZT2}, for the 27 through 75 volt types is tested at 0.5 mA rather than the test current of 0.1 mA used for V_{Z2}.

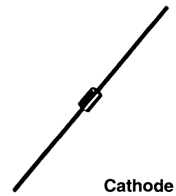
Devices listed in bold, italic are Motorola preferred devices.

Zener Diodes

Voltage Reference Diodes

Temperature Compensated Reference Devices

For applications where output voltage must remain within narrow limits during changes in input voltage, load resistance and temperature. Motorola guarantees all reference devices to fall within the specified maximum voltage variations, ΔV_Z, at the specifically indicated test temperatures and test current (JEDEC Standard #5). Temperature coefficient is also specified but should be considered as a reference only — not a maximum rating.
Devices in this table are hermetically sealed structures.



Glass
CASE 299–02
DO–204AH
(DO–35)

Cathode = Polarity Band

Table 21. Temperature Compensated Reference Devices

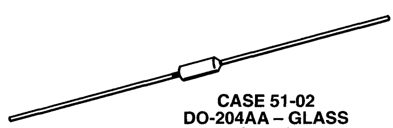
			AVERAGE TEMPERATURE COEFFICIENT OVER THE OPERATING RANGE									
			0.01 %/°C		0.005 %/°C		0.002 %/°C		0.001 %/°C		0.0005 %/°C	
V_Z Volts	Test Current mAdc	Test(2) Temp Points	Device Type	ΔV_Z Max Volts	Device Type	ΔV_Z Max Volts	Device Type	ΔV_Z Max Volts	Device Type	ΔV_Z Max Volts	Device Type	ΔV_Z Max Volts
6.2(1)	7.5	A	***1N821***	0.096	***1N823***	0.048	***1N825***	0.019	1N827	0.009	1N829	0.005
6.2(1)	7.5	A	***1N821A***	0.096	***1N823A***	0.048	***1N825A***	0.019	1N827A	0.009	1N829A	0.005

(1) Non–suffix — Z_{ZT} = 15 ohms, "A" Suffix — Z_{ZT} = 10 ohms
(2) Test Temperature Points °C: A = −55, 0, +25, +75, +100

Current Regulator Diodes

High impedance diodes whose "constant current source" characteristic complements the "constant voltage" of the zener line. Currents are available from 0.22 to 4.7 mA, with usable voltage range from a minimum limit of 1.0 to 2.5 Volts, up to a voltage compliance of 100 Volts, for the 1N5283 series.

Table 22. Current Regulator Diodes



CASE 51-02
DO-204AA – GLASS
(DO-7)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Type No.	Regulator Current I_P (mA) @ V_T = 25 V Nom	Min	Max	Minimum Dynamic Impedance @ V_T = 25 V Z_T (MΩ)	Minimum Knee Impedance @ V_K = 6.0 V Z_K (MΩ)	Maximum Limiting Voltage @ I_L = 0.8 I_P (min) V_L (Volts)
1N5283	0.22	0.198	0.242	25.0	2.75	1.00
1N5287	0.33	0.297	0.363	6.6	1.35	1.00
1N5297	1.00	0.900	1.100	0.800	0.205	1.35
1N5298	1.00	0.900	1.210	0.700	0.180	1.40
1N5305	2.00	1.80	2.20	0.395	0.061	1.85
1N5309	3.00	2.70	3.30	0.300	0.029	2.25
1N5310	3.30	2.97	3.63	0.280	0.024	2.35
1N5311	3.60	3.24	3.96	0.265	0.020	2.50
1N5312	3.90	3.51	4.29	0.255	0.017	2.60
1N5313	4.30	3.87	4.73	0.245	0.014	2.75
1N5314	4.70	4.23	5.17	0.235	0.012	2.90

Devices listed in bold, italic are Motorola preferred devices.

Devices listed in bold, italic are Motorola preferred devices.

Hybrid Power Module Operation

In Brief . . .

The Motorola Semiconductor Products Sector is proud to announce the formation of a new group: Hybrid Power Modules. Our operation has been in existence since August of 1992, and we're chartering new ground to become the world's fastest supplier of intelligent, energy efficient power modules for motor drive and uninterruptable power supply applications.

It's an exciting market, with 50 million motors being manufactured per year, and fewer than 5% of those using electronically controlled drives. Motorola Hybrid Power Modules will play a major role in supplying those power modules.

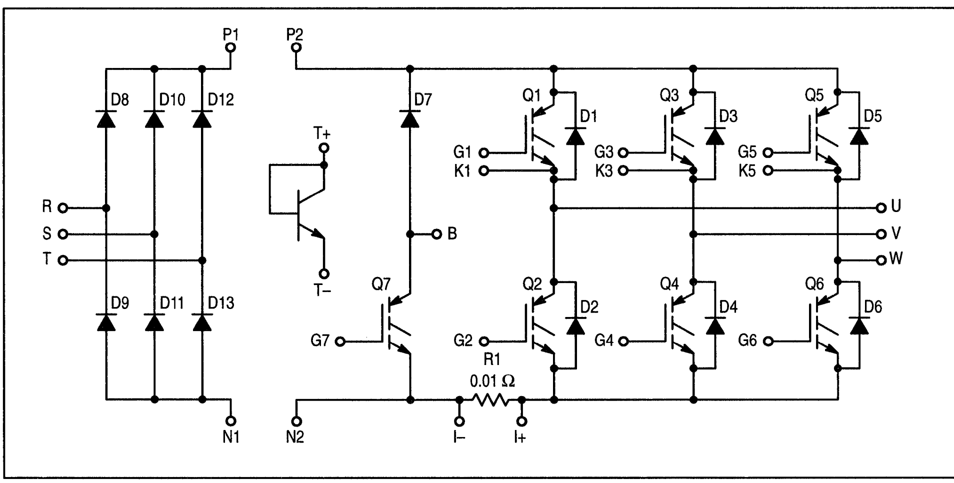
With Motorola's technology broadth, we're well positioned to develop highly integrated, intelligent IGBT (insulated gate bipolar transistor) power modules. The IGBT technology combines high current handling capability with low input current requirements in a smaller form factor which enables the design of more compact inverters. We have the capabilities to support custom modules (based on annual volume requirements) and offer the fastest possible time to market. Present integrated IGBT modules range from 5 to 30 amps, 600 and 1200 volts are also in our product portfolio. Our plans for the future include a family of advanced modules for applications in higher current and higher voltage devices and control networks.

To summarize, we believe that we offer the leading edge technology combined with a state–of–the–art flexible manufacturing line and rapid cycle time that can give you the unique ability to differentiate your products in this highly competitive market.

Table 1. Integrated Power Stage IGBT

V_{CES} (V)	Maximum Ratings				
	I_C (A)				
	5	10	15	20–25	30
600			***MHPM7A15A60A*** 6/94	***MHPM7A20A60A*** 10/94	***MHPM7A30A60B*** 5/95
1200	***MHPM7A8A120A*** 7/94	***MHPM7A12A120A*** 1/95	***MHPM7A16A120B*** 5/95	***MHPM7A25A120B*** 9/95	

CIRCUIT



Includes sense resistor and temperature sensor.

Benefits of Motorola Integrated Power Stage

- combines a 3–phase input rectifier bridge, output inverter and brake transistor in one package
- utilizes Motorola's advanced 600 & 1200 V IGBTs with matched soft free–wheeling diodes
- positive and negative bus access to designer
- temperature and current sense integrated in module

Devices listed in bold, italic are Motorola preferred devices.

TMOS Power MOSFETs Products

In Brief . . .

Motorola continues to build a world class portfolio of TMOS Power MOSFETs with new advances in silicon and packaging technology. The following new advances have been made in the area of silicon technology.

- New high voltage devices with voltages up to 1200 volts.
- New High Cell Density (HDTMOS) family of standard and Logic Level devices in both N and P–channel are available in DPAK, D^2PAK, TO–220 and SO–8 surface mount packages and in the industry standard TO–220 package.
- New TMOS V fifth generation of Motorola Power MOSFET technology. This is a new processing technique that more than doubles the present cell density of our MOSFET devices.
- New Micro8 package is the smallest power MOSFET surface mount package.
- New EZFET™ surface mount power MOSFETs incorporate back to back zener diodes across the gate–to–source to enhance ESD protection.
- New IGBTs with high short circuit capability in TO–220, TO–247 and TO–264 packages.

The following new advances have been made in the area of packaging technology.

- New SO–8 (MiniMOS) and SOT–223 packages to the surface mount portfolio.
- New High Power packages capable of housing very large die and higher power dissipation are now available in the TO–264 (formerly TO–3PBL) and SOT–227B (Isotop) packages.
- New D^3PAK package allows the highest power dissipation of any standard, plastic surface–mount power semiconductor.

TMOS
Power MOSFETs

TMOS Power MOSFETs Numbering System

Wherever possible, Motorola has used the following numbering systems for TMOS power MOSFET products.

MTP75N06HD

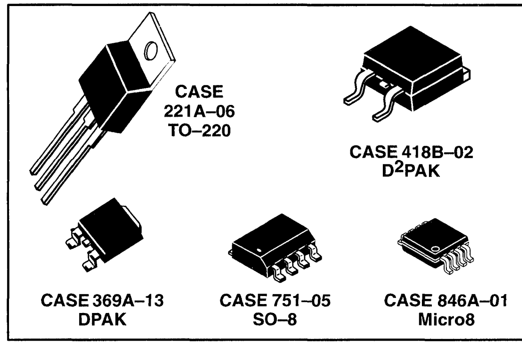
- **MOTOROLA**
  - X FOR ENGINEERING SAMPLES
- **TMOS**
  - T FOR TMOS
  - L FOR SMARTDISCRETES
  - G FOR IGBT
- **PACKAGE TYPE**
  - P FOR PLASTIC TO–220
  - D FOR DPAK
  - A FOR TO–220 ISOLATED
  - W FOR TO–247
  - B FOR D^2PAK
  - Y FOR TO–264
  - E FOR SOT–227B
  - V FOR D^3PAK
- **CURRENT**
- **CHANNEL POLARITY, N OR P**
- **VOLTAGE RATING DIVIDED BY 10**
- **OPTIONAL SUFFIX:**
  - L FOR LOGIC LEVEL
  - E FOR ENERGY RATED
  - T4 FOR TAPE & REEL (DPAK/D^2PAK)
  - RL FOR TAPE & REEL (DPAK)
  - HD FOR HIGH CELL DENSITY
  - V FOR TMOS V (FIVE)

Example of exceptions: MTD/MTP3055E
MTD/MTP2955E

SO–8 (MiniMOS)™, Micro8™ and SOT–223 Power MOSFETs

MMSF4P01HDR1

- **MOTOROLA**
- **TMOS**
  - M FOR MINIATURE
- **PACKAGE TYPE**
  - DF — DUAL FET (SO–8)
  - SF — SINGLE FET (SO–8)
  - FT — FET TRANSISTOR (SOT–223)
  - MTSF — SINGLE FET (Micro8)
  - MTDF — DUAL FET (Micro8)
- **CURRENT**
- **CHANNEL POLARITY, N OR P**
  - C FOR COMPLEMENTARY
- **VOLTAGE RATING DIVIDED BY 10**
- **OPTIONAL SUFFIX:**
  - E FOR ENERGY RATED
  - HD FOR HIGH CELL DENSITY
  - L FOR LOGIC LEVEL
  - V FOR TMOS V (FIVE)
  - Z FOR ESD
- **R1 AND R2 FOR TAPE & REEL**
  - MiniMOS
- **T1 AND T3 FOR TAPE & REEL**
  - SOT–223



HDTMOS Power MOSFETs N and P–Channel

HDTMOS Technology is a design technique that reduces the on–resistance contribution in virtually every portion of the power FET. The aggressive six million cells per square inch design is easily manufactured using wafer fabrication techniques that Motorola has used for several years to manufacture highly successful 8–bit microcontrollers.

HDTMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

Table 1. High Power

$V_{(BR)DSS}$	$R_{DS(on)}$ @ V_{GS}			I_D	Motorola Part Number	Package Type
(V)	10 V (mΩ)	5 V (mΩ)	2.7 V (mΩ)	(A)		
60	45	—	—	20	***MTD20N06HD***[4]	DPAK
	—	45	—	20	***MTD20N06HDL***[4]	DPAK
	—	150	—	15	***MTD20P06HDL***[4][5]	DPAK
	10	—	—	75	***MTB75N06HD***[4]	D^{2}PAK
	14	—	—	60	***MTB60N06HD***[4]	D^{2}PAK
	10	—	—	75	***MTP75N06HD***	TO–220
	14	—	—	60	***MTP60N06HD***	TO–220
50	9.50	—	—	75	***MTP75N05HD***	TO–220
	9.50	—	—	75	***MTB75N05HD***[4]	D^{2}PAK
30	—	35	—	20	***MTD20N03HDL***[4]	DPAK
	—	99	—	19	***MTD20P03HDL***[4][5]	DPAK
	6.0	7.5	—	75	***MTB75N03HDL***[4]	D^{2}PAK
	—	30	—	50	***MTB50P03HDL***[4][5]	D^{2}PAK
	6.0	7.5	—	75	***MTP75N03HDL***	TO–220
	—	30	—	50	***MTP50P03HDL***[5]	TO–220

[4] Available in tape and reel — add T4 suffix to part number.
[5] Indicates P–Channel

Devices listed in bold, italic are Motorola preferred devices.

HDTMOS Power MOSFETs (continued)

Table 2. SOIC — COMPLEMENTARY, N and P–Channel

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ V_{GS} 10 V (mΩ)	4.5 V (mΩ)	2.7 V (mΩ)	I_D (A)	Device[5]	Package Type	P_D[3] (Watts) Max
50	300	500	—	1.5	***MMDF1N05E***	SO-8	1.5
30	200	300	—	2	***MMDF2P03HD***	SO-8	1.5
	100	110	—	3	***MMSF3P03HD***	SO-8	1.5
	70/200[11]	75/300[11]	—	2	***MMDF2C03HD***	SO-8	1.5
	70	75	—	2.8	***MMDF3N03HD***	SO-8	1.5
	40	50	—	5	***MMSF5N03HD***	SO-8	1.5
20	250	400	—	2	***MMSF2P02E***	SO-8	1.5
	250	400	—	2	***MMDF2P02E***	SO-8	1.5
	160	180	—	2	***MMDF2P02HD***	SO-8	1.5
	100/250[11]	200/400[11]	—	2	***MMDF2C02E***	SO-8	1.5
	100	200	—	2	***MMDF2N02E***	SO-8	1.5
	90/160[11]	100/180[11]	—	2	***MMDF2C02HD***	SO-8	1.5
	90	100	—	3	***MMDF3N02HD***	SO-8	1.5
	75	95	—	3	***MMSF3P02HD***	SO-8	1.5
	25	40	—	5	***MMSF5N02HD***	SO-8	1.5
12	—	180	220	2	***MMDF2P01HD***	SO-8	1.5
	—	100	110	4	***MMSF4P01HD***	SO-8	1.5
	—	45/180[11]	55/220[11]	2	***MMDF2C01HD***	SO-8	1.5
	—	45	55	4	***MMDF4N01HD***	SO-8	1.5

(3) Power rating when mounted on an FR-4 glass epoxy printed circuit board with the minimum recommended footprint.
(5) Available in tape and reel only — R1 suffix = 500/reel, R2 suffix = 2500/reel.
(11) N–Channel/P–Channel $R_{DS(on)}$

Table 3. EZFET

$V_{(BR)DSS}$ (Volts) Min	Device	Description	$R_{DS(on)}$ (mΩ) Max	@ V_{GS} (Volts)	I_D (cont) Amps	V_{GS} (Volts) Max	Package
20	***MMSF3P02Z***	Single P–Channel	75 90	10 4.5	3	±15	SO–8
	MMSF4P01Z		70 90	4.5 2.7	4	±8	
	MMSF6N01Z	Single N–Channel	25 30	4.5 2.7	6		
	MMDF4N01Z	Dual N–Channel	45 55	4.5 2.7	4		
30	***MMSF5N03Z***	Single P–Channel	30 40	10 4.5	5	±15	

Table 4. Micro8

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (mΩ) Max	V_{GS} (Volts)	I_D (cont) Amps	Device	Product Description
20	190	2.7	2	***MTSF1P02HD***	Single P–Channel
20	200	2.7	1.5	***MTDF1N02HD***	Dual N–Channel
30	75	4.5	3	***MTSF3N03HD***	Single N–Channel
30	225	4.5	1.5	***MTDF1N03HD***	Dual N–CHannel

Devices listed in bold, italic are Motorola preferred devices.

TMOS V

TMOS V

Motorola Introduces Fifth Generation TMOS Technology

Power Products Division introduces a new technology in the low voltage TMOS transistor family. This new generation technology is currently referred to as TMOS V. It is revolutionary rather than evolutionary.

The TMOS V technology will more than double the present cell density of our TMOS Power MOSFETs. This new technology will result in a tighter overall distribution of electrical parameters and optimizes the performance of our 50 and 60 volt portfolio.

This is a high cell density process of the future that will produce a new line of industry standard devices. Power transistors can now be built with the same high resolution/small geometry MOS fabrication technology that is standard in Motorola's ASIC, microprocessor and Memory Wafer Fabs.

Table 1. TMOS V — DPAK N–Channel

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device	I_D (cont) Amps	P_D (Watts) Max
60	0.150	6	***MTD3055V***(4)	12	1.75(3)
	0.180	6	***MTD3055VL***(2)(4)	12	1.75(3)
	0.120	7.5	***MTD15N06V***(4)	15	1.75(3)
	0.120	7.5	***MTD15N06VL***(2)(4)	15	1.75(3)
	0.100	10	***MTD20N06V***(4)	20	1.75(3)

Table 2. TMOS V — TO–220AB N–Channel

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device	I_D (cont) Amps	P_D (Watts) Max
60	0.150	6	***MTP3055V***	12	48(1)
	0.180	6	***MTP3055VL***(2)	12	48(1)
	0.120	7.5	***MTP15N06V***	15	55(1)
	0.120	7.5	***MTP15N06VL***(2)	15	65(1)
	0.100	10	***MTP20N06V***	20	65(1)
	0.040	16	***MTP36N06V***	32	90(1)
	0.050	15	***MTP30N06VL***(2)	30	90(1)
	0.028	21	***MTP50N06V***	42	125(1)
	0.032	21	***MTP50N06VL***(2)	42	125(1)
	0.024	26	***MTP52N06V***	52	135(1)
	0.028	26	***MTP52N06VL***(2)	52	135(1)

(1) $T_C = 25°C$
(2) Indicates logic level
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) Available in tape and reel — add T4 suffix to part number.

Devices listed in bold, italic are Motorola preferred devices.

TMOS V (continued)

Table 3. TMOS V — D^2PAK N–Channel

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D (Watts) Max
60	0.120	7.5	***MTB15N06V***(4)	15	3.0(3)
	0.120	7.5	***MTB15N06VL***(2)(4)	15	3.0(3)
	0.100	10	***MTB20N06V***(4)	20	3.0(3)
	0.040	16	***MTB36N06V***(4)	32	3.0(3)
	0.050	15	***MTB30N06VL***(2)(4)	30	3.0(3)
	0.028	21	***MTB50N06V***(4)	42	3.0(3)
	0.032	21	***MTB50N06VL***(2)(4)	42	3.0(3)
	0.024	26	***MTB52N06V***(4)	52	3.0(3)
	0.028	26	***MTB52N06VL***(2)(4)	52	3.0(3)

Table 4. TMOS V — SOIC–8

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D (Watts) Max
60	0.150	0.85	***MMDF3055V***(4)	1.7	1.8(3)
	0.180	0.75	***MMDF3055VL***(2)(4)	1.5	1.8(3)

Table 5. TMOS V — SOT–223

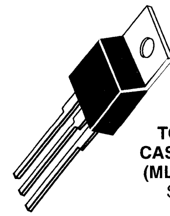
$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D (Watts) Max
60	0.150	0.85	***MMFT3055V***(4)	1.7	0.96(3)
	0.180	0.75	***MMFT3055VL***(2)(4)	1.5	0.96(3)

Table 6. TMOS V — P–Channel

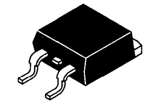
$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D (Watts) Max
60	0.450	2.5	***MTD5P06V***(4)	5	1.75(3)
	0.450	2.5	***MTP5P06V***	5	40(1)
	0.300	6	***MTD2955V***(4)	12	1.75(3)
	0.300	6	***MTP2955V***	12	55(1)
	0.120	11.5	***MTB23P06V***(4)	23	3.0(3)
	0.120	11.5	***MTP23P06V***	23	90(1)
	0.080	15	***MTP30P06V***	30	125(1)
	0.080	15	***MTB30P06V***(4)	30	3.0(3)

(1) $T_C = 25°C$
(2) Indicates logic level
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) Available in tape and reel — add T4 suffix to part number.

Devices listed in bold, italic are Motorola preferred devices.



TO–220AB
CASE 221A–06
(MLP PREFIX)
STYLE 5



CASE 418B–02
STYLE 2

SMARTDISCRETES Products

From a standard power MOSFET process, several active and passive elements can be obtained that provide on–chip protection to the basic power device. Such elements require only a small increase in silicon area and/or the addition of one masking layer to the process. The resulting device exhibits significant improvements in ruggedness and reliability and a system cost reduction. These SMARTDISCRETES™ functions can now provide an economical alternative to smart power ICs for power applications requiring low on–resistance, high voltage and high current.

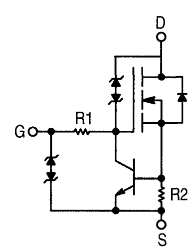
These devices make up a series of "smart" power devices that automatically clamp spikes in automotive ignition systems and guard against ESD. The devices feature a logic level IGBT (Insulated Gate Bipolar Transistor) with integral active collector clamp and ESD gate protection and are designed primarily as ignition coil drivers to withstand high current in a pulsed mode without latching.

Table 1. Ignition IGBTs

BV_{CES} (Volts) Clamped	$V_{CE(on)}$ @ 10 A	Device	P_D[1] (Watts) Max	Package
140 V	1.8	***MGP20N14CL***	150	TO–220AB
350 V	1.8	***MGP20N35CL*** ***MGB20N35CL***	150 2.5[3][4]	TO–220AB D^2PAK
400 V	1.8	***MGP20N40CL*** ***MGB20N40CL***	150 2.5[3][4]	TO–220AB D^2PAK

(1) T_C = 25°C
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) DPAK and D^2PAK packages available in tape and reel — add T4 suffix to part number.

The MLP1N06CL is a SMARTDISCRETES device that has integrated on–chip current limit capability, drain–to–source voltage clamping and gate voltage protection. The logic level processing allows operation of this device at half of the gate–to–source (5 volts) voltage of the conventional MOSFETs and can now be driven directly from CMOS or TTL logic drivers. This integration of technologies results in an intelligent, monolithic power circuit that offers a reduced parts count and improved reliability by replacing resistors, diodes, a bipolar transistor and a MOSFET with one device all of which are packaged in a TO–220AB package.



MLP1N06CL

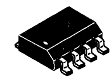
Table 2. TO–220AB — MLP1N06CL

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	I_D (Amps)	Device	I_D (cont) Amps	P_D[1] (Watts) Max
60 Clamped Voltage	0.75	1	***MLP1N06CL***	Current Limited	40
62 Clamped Voltage	0.4	2	MLP2N06CL	Current Limited	40

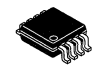
(1) T_C = 25°C
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.

Devices listed in bold, italic are Motorola preferred devices.

TMOS V



CASE 751–05
SO–8
STYLE 11, STYLE 13



CASE 846A–01
Micro8

N–Channel

SO–8 MiniMOS™ and Micro8 Surface Mount Products

MiniMOS devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance.

MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

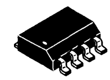
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, with Soft Recovery
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Avalanche Energy Specified

Table 1. SO–8 Products — N–Channel

$V_{(BR)DSS}$	$R_{DS(on)}$ @ V_{GS}			I_D			
(V)	10 V (mΩ)	4.5 V (mΩ)	2.7 V (mΩ)	(A)	Device(5)	Package Type	P_D(3) (Watts) Max
50	300	500	—	1.5	***MMDF1N05E***	SO-8	1.5
30	40	50	—	5	***MMSF5N03HD***	SO-8	1.5
	70	75	—	2.8	***MMDF3N03HD***	SO-8	1.5
	70/200(11)	75/300	—	2	***MMDF2C03HD***	SO-8	1.5
20	25	40	—	5	***MMSF5N02HD***	SO-8	1.5
	90	100	—	3	***MMDF3N02HD***	SO-8	1.5
	100	200	—	2	***MMDF2N02E***	SO-8	1.5
	90/160(11)	100/180(11)	—	2	***MMDF2C02HD***	SO-8	1.5
	100/250(11)	200/400(11)	—	2	***MMDF2C02E***	SO-8	1.5
12	—	45	55	4	***MMDF4N01HD***	SO-8	1.5
	—	45/180(11)	55/220(11)	2	***MMDF2C01HD***	SO-8	1.5

(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(5) Available in tape and reel only — R1 suffix = 500/reel, R2 suffix = 2500/reel.
(11) N–Channel/P–Channel $R_{DS(on)}$

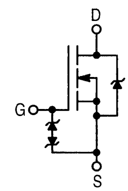
Devices listed in bold, italic are Motorola preferred devices.



CASE 751–05
SO–8
STYLE 11, STYLE 13

N–Channel

SO–8 EZFET™ — Power MOSFETs with Zener Gate Protection



N–Channel

- New Family of Low $R_{DS(on)}$ MOSFETs with monolithic back–to–back zener diodes across the gate to source.
- HDTMOS™ Technology (High Cell Density TMOS)
- Extremely Low $R_{DS(on)}$ provides higher efficiency and increased battery life in portable applications

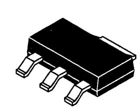
Table 2. EZFET

$V_{(BR)DSS}$ (Volts) Min	Device	Description	$R_{DS(on)}$ (mΩ) Max	@ V_{GS} (Volts)	I_D (cont) Amps	V_{GS} (Volts) Max	Package
20	***MMSF6N01Z***	Single N–Channel	25 30	4.5 2.7	6	±8	SO–8
	MMDF4N01Z	Dual N–Channel	45 55	4.5 2.7	4		

Table 3. Micro8

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (mΩ) Max	@ V_{GS} (Volts)	I_D (cont) Amps	Device	Product Description
20	200	2.7	1.5	***MTDF1N02HD***	Dual N–Channel
30	75	4.5	3	***MTSF3N03HD***	Single N–Channel
30	225	4.5	1.5	***MTDF1N03HD***	Dual N–CHannel

SOT–223 Medium Power MOSFETs Surface Mount Products



CASE 318E–04
SOT–223
STYLE 3

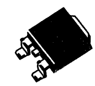
Table 4. SOT–223 Medium Power TMOS FETs — N–Channel

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device(12)	I_D (cont) Amps	P_D(1) (Watts) Max	Applications
100	0.30	0.5	***MMFT1N10E***	1	0.8(3)	dc-dc Converters Power Supplies Motor Controls, Disk Drives
60	0.18	0.75	***MMFT3055EL***(2)	1.5		
	0.15	0.85	***MMFT3055E***	1.7		
20	0.15	1	***MMFT2N02EL***(2)	2		

(1) $T_C = 25°C$
(2) Indicates logic level
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(12) Available in tape and reel only — T1 suffix = 1000/reel, T3 suffix = 4000/reel.

Devices listed in bold, italic are Motorola preferred devices.

N–Channel (continued)



CASE 369A–13
TO–252
STYLE 2

N–Channel

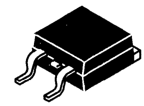
DPAK Surface Mount Products

Table 5. DPAK — N–Channel

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device (4)	I_D (cont) Amps	P_D (1) (Watts) Max
800	12	0.5	***MTD1N80E***	1	1.75(3)
600	8	0.5	***MTD1N60E***	1	
500	5	0.5	***MTD1N50E***	1	
	3.60	1	***MTD2N50E***	2	
400	3.50	1	***MTD2N40E***	2	
250	1.40	1.5	***MTD3N25E***	3	
	1	2.5	***MTD5N25E***	5	
200	1.20	2	***MTD4N20E***	4	
	0.70	3	***MTD6N20E***	6	
150	0.30	3	MTD6N15	6	
100	0.60	2.5	***MTD5N10E***	5	
	0.40	3	***MTD6N10E***	6	
	0.25	4.5	***MTD9N10E***	9	
	0.22	5	***MTD10N10EL***(2)	10	
60	0.18	6	***MTD3055VL***(2)	12	
	0.15	6	***MTD3055V***	12	
	0.12	4	***MTD8N06E***	8	
	0.12	7.5	***MTD15N06V***	15	
	0.045	10	***MTD20N06HD***	20	
	0.045	10	***MTD20N06HDL***(2)	20	
50	0.10	5	***MTD10N05E***	10	
30	0.035	10	***MTD20N03HDL***(2)	20	

(1) $T_C = 25°C$
(2) Indicates logic level
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) Available in tape and reel — add T4 suffix to part number.

Devices listed in bold, italic are Motorola preferred devices.



CASE 418B–02
STYLE 2

N–Channel

D2PAK Surface Mount Products

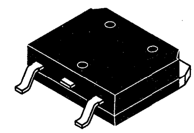
Table 6. D2PAK — N–Channel

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device(4)	I_D (cont) Amps	P_D(1) (Watts) Max
1200	5	1.5	***MTB3N120E***	3	2.5(3)
1000	9	0.5	***MTB1N100E***	1	
	4	1.5	***MTB3N100E***	3	
800	3	2	***MTB4N80E***	4	
600	1.20	3	***MTB6N60E***	6	
500	0.80	4	***MTB8N50E***	8	
400	0.55	5	***MTB10N40E***	10	
250	0.50	4.5	***MTB9N25E***	9	
	0.25	8	***MTB16N25E***	16	
200	0.16	10	***MTB20N20E***	20	
100	0.060	16.5	***MTB33N10E***	33	
60	—	—	***MTB15N06V***	—	
	0.05	15	***MTB30N06EL***(2)	30	
	0.04	16	***MTB36N06V***	36	
	0.032	21	***MTB50N06VL***	42	
	0.028	21	***MTB50N06V***	42	
	0.014	30	***MTB60N06HD***	60	
	0.01	37.5	***MTB75N06HD***	75	
50	0.0095	37.5	***MTB75N05HD***	75	
30	0.0075	37.5	***MTB75N03HDL***(2)	75	

(1) $T_C = 25°C$
(2) Indicates logic level
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) Available in tape and reel — add T4 suffix to part number.

Devices listed in bold, italic are Motorola preferred devices.

TMOS®



CASE 433–01
TO–286
STYLE 2

N–Channel

D3PAK

- D3PAK is a high power surface mount package designed to accommodate die which is too large for a D2PAK.
  - Utilized for Size 5, Size 6 or larger MOSFET and IGBT.
  - Used for dual die IGBT and diode combination.
- 24 mm Tape and Reel, 500 units per 13' reel.
- D3PAK is thermal characterized for use on FR–4 and IMS board materials.

- Applications:
  - Surface mount motor drives
  - Power supplies both AC/DC and DC/DC

Table 7. D3PAK — N–Channel

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device(4)	I_D (cont) Amps	P_D(1) (Watts) Max
1000	1.50	3	***MTV6N100E***	6	178
	1.30	5	***MTV10N100E***	10	250
500	0.320	8	***MTV16N50E***	16	250
	0.240	10	***MTV20N50E***	20	250
	0.200	12.5	***MTV25N50E***	25	250
250	0.065	16	***MTV32N05E***	32	250
200	0.075	16	***MTV32N20E***	32	180

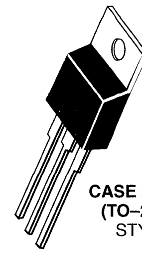
(1) $T_C = 25°C$
(4) Available in tape and reel — add RL suffix to part number.

Devices listed in bold, italic are Motorola preferred devices.

N–Channel (continued)

N–Channel

TO–220AB



CASE 221A–06
(TO–220AB)
STYLE 5

Table 8. TO–220AB — N–Channel

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D(1) (Watts) Max
1200	5.0	1.5	***MTP3N120E***	3	125
1000	9	0.5	***MTP1N100E***	1	75
	4.0	1.5	***MTP3N100E***	3	125
800	3	2	***MTP4N80E***	4	
600	8	0.5	***MTP1N60E***	1	50
	3.80	1	***MTP2N60E***	2	
	2.20	1.5	***MTP3N60E***	3	75
	1.20	3	***MTP6N60E***	6	125
500	5	0.5	***MTP1N50E***	1	50
	3.60	1	***MTP2N50E***	2	75
	3	1.5	***MTP3N50E***	3	50
	1.50	2	***MTP4N50E***	4	75
	0.80	4	***MTP8N50E***	8	125
400	3.50	1	***MTP2N40E***	2	50
	1.80	2	***MTP4N40E***	4	50
	1	2.5	***MTP5N40E***	5	75
	0.55	5	***MTP10N40E***	10	125
250	1.4	1	***MTP3N25E***	3	40
	0.5	4.5	***MTP9N25E***	9	75
	0.25	8	***MTP16N25E***	16	125
200	0.70	3.5	***MTP7N20E***	7	75
	0.16	10	***MTP20N20E***	20	125
100	0.25	5	***MTP10N10E***	10	75
	0.22	5	MTP10N10EL	10	40
	0.16	6	***MTP12N10E***	12	75
	0.070	13.5	***MTP27N10E***	27	125
	0.060	16.5	***MTP33N10E***	33	150

(1) $T_C = 25°C$

Devices listed in bold, italic are Motorola preferred devices.

N–Channel (continued)

Table 8. TO–220AB — N–Channel (continued)

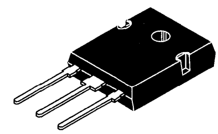
$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D(1) (Watts) Max
60	0.18	6	***MTP3055VL***(2)	12	48
	0.15	6	***MTP3055V***	12	
	0.12	7.5	***MTP15N06V***	15	60
	0.12	7.5	***MTP15N06VL***	15	65
	0.10	10	***MTP20N06V***	20	
	0.05	15	***MTP30N06VL***(2)	30	90
	0.04	18	***MTP36N06V***	32	
	0.032	25	***MTP50N06VL***(2)	50	150
	0.028	25	***MTP50N06V***	50	
	0.028	26	***MTP52N06VL***	52	135
	0.024	26	***MTP52N06V***	52	
	0.014	30	***MTP60N06HD***	60	150
	0.01	37.5	***MTP75N06HD***	75	
50	0.10	7.5	***MTP15N05EL***(2)	15	75
	0.0095	37.5	***MTP75N05HD***	75	150
25	0.0075	37.5	***MTP75N03HDL***(2)	75	

(1) $T_C = 25°C$
(2) Indicates logic level

Devices listed in bold, italic are Motorola preferred devices.

TMOS

N–Channel



CASE 340F–03
TO–247AE
(MTW PREFIX)
STYLE 1

TO–247 Isolated Mounting Hole

The Motorola portfolio of TO–247 devices has new on–resistance specifications on many industry standard devices with $R_{DS(on)}$ reductions up to 25%.

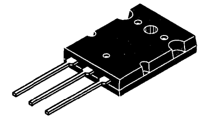
Table 9. TO–247 — N–Channel

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device	I_D (cont) Amps	P_D(1) (Watts) Max
1000	1.50	3	***MTW6N100E***	6	180
	1.30	5	***MTW10N100E***	10	250
800	1	3.5	***MTW7N80E***	7	180
600	0.50	4	***MTW8N60E***	8	180
500	0.32	7	***MTW14N50E***	14	180
	0.24	10	***MTW20N50E***	20	250
400	0.24	8	***MTW16N40E***	16	180
	0.16	12	***MTW24N40E***	24	250
250	0.10	16	***MTW32N25E***	32	250
200	0.075	16	***MTW32N20E***	32	180
150	0.065	17.5	***MTW35N15E***	35	180
100	0.035	22.5	***MTW45N10E***	45	180

(1) $T_C = 25°C$

Devices listed in bold, italic are Motorola preferred devices.

N–Channel



CASE 340G–02
TO–264

TO–264 High Power Products

The TO–264 package is a new addition to the Motorola portfolio of high power packages. This package is capable of a power dissipation of 300 Watts and it achieves a low on–resistance with a single die. Lead spacing is compatible to the TO–247 package.

Table 10. TO–264 High Power Products — N–Channel

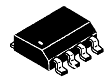
$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device	I_D (cont) Amps	P_D(1) (Watts) Max
600	0.21	12.5	***MTY25N60E***	25	300
500	0.26	10	***MTY20N50E***	20	
	0.15	15	***MTY30N50E***	30	
200	0.028	27.5	***MTY55N20E***	55	
100	0.011	50	***MTY100N10E***	100	

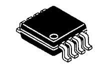
(1) $T_C = 25°C$

Devices listed in bold, italic are Motorola preferred devices.

TMOS

TMOS





CASE 751–05
SO–8
STYLE 11, STYLE 13

CASE 846A–01
Micro8

P–Channel

SO–8 (MiniMOS) and Micro8 Surface Mount Products

Multiple Chip TMOS Products in SOIC Surface Mount Packages

MiniMOS devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance.

MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

Table 1. SO–8 Products — P–Channel

$V_{(BR)DSS}$	$R_{DS(on)}$ @ V_{GS}			I_D			P_D(3)
(V)	10 V (mΩ)	4.5 V (mΩ)	2.7 V (mΩ)	(A)	Device(5)	Package Type	(Watts) Max
30	100	110	—	3	***MMSF3P03HD***	SO-8	1.5
	200	300	—	2	***MMDF2P03HD***	SO-8	1.5
20	75	95	—	3	***MMSF3P02HD***	SO-8	1.5
	160	180	—	2	***MMDF2P02HD***	SO-8	1.5
	250	400	—	2	***MMDF2P02E***	SO-8	1.5
	250	400	—	2	***MMSF2P02E***	SO-8	1.5
12	—	100	110	4	***MMSF4P01HD***	SO-8	1.5
	—	180	220	2	***MMDF2P01HD***	SO-8	1.5

(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(5) Available in tape and reel only — R1 suffix = 500/reel, R2 suffix = 2500/reel.

Table 2. Micro8

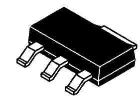
$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (mΩ) Max @	V_{GS} (Volts)	I_D (cont) Amps	Device	Product Description
20	190	2.7	2	***MTSF1P02HD***	Single P–Channel

Table 3. EZFET

$V_{(BR)DSS}$ (Volts) Min	Device	Description	$R_{DS(on)}$ (mΩ) Max	V_{GS} (Volts)	I_D (cont) Amps	V_{GS} (Volts) Max	Package
20	***MMSF3P02Z***	Single P–Channel	75 90	10 4.5	3	±15	SO–8
	MMSF4P01Z		70 90	4.5 2.7	4	±8	

Devices listed in bold, italic are Motorola preferred devices.

P–Channel



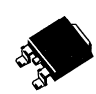
CASE 318E–04
SOT–223
STYLE 3

SOT–223 Medium Power MOSFETs Surface Mount Products

Table 4. SOT–223 Medium Power TMOS FETs — P–Channel

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) @ Max	I_D (Amps)	Device(12)	I_D (cont) Amps	P_D(1) (Watts) Max	Application
60	0.30	0.6	***MMFT2955E***	1.2	0.8(3)	dc-dc Converters Power Supplies Motor Controls, Disk Drives

(1) $T_C = 25°C$
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(12) Available in tape and reel only — T1 suffix = 1000/reel, T3 suffix = 4000/reel.



CASE 369A–13
TO–252
STYLE 2

DPAK Surface Mount Products

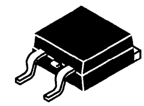
Table 5. DPAK — P–Channel

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) @ Max	I_D (Amps)	Device(4)	I_D (cont) Amps	P_D(1) (Watts) Max
500	15.0	0.5	***MTD1P50E***	1	1.75(3)
100	0.66	3	***MTD6P10E***	6	
60	0.55	2.5	***MTD5P06E***	5	
	—	—	***MTD5P06V***	—	
	0.15	10	***MTD20P06HDL***(2)	20	
30	0.099	10	***MTD20P03HDL***(2)	19	

(1) $T_C = 25°C$
(2) Indicates logic level
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) Available in tape and reel — add T4 suffix to part number.

Devices listed in bold, italic are Motorola preferred devices.

P–Channel



CASE 418B–02
STYLE 2

D2PAK Surface Mount Products

Table 6. D2PAK — P–Channel

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device(4)	I_D (cont) Amps	P_D(1) (Watts) Max
500	6	1	***MTB2P50E***	2	2.5(3)
60	0.12	11.5	***MTB23P06E***	23	
30	0.025	25	***MTB50P03HDL***(2)	50	

(1) $T_C = 25°C$
(2) Indicates logic level
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) Available in tape and reel — add T4 suffix to part number.

CASE 221A–06
(TO–220AB)
STYLE 5

TO–220AB

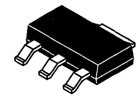
Table 7. TO–220AB — P–Channel

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device	I_D (cont) Amps	P_D(1) (Watts) Max
500	6	1	***MTP2P50E***	2	75
200	1	3	***MTP6P20E***	6	
100	0.30	6	***MTP12P10***	12	88
60	0.45	2.5	***MTP5P06V***	5	40
	0.30	6	***MTP2955V***	12	60
	0.12	11.5	***MTP23P06V***	23	125
	0.08	15	***MTD30P06V***	30	125
30	0.025	25	***MTP50P03HDL***(2)	50	150

(1) $T_C = 25°C$
(2) Indicates logic level

Devices listed in bold, italic are Motorola preferred devices.

TMOS
TMOS V



CASE 318E–04
SOT–223
STYLE 3

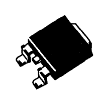
Logic Level — N–Channel

SOT–223 Medium Power MOSFETs Surface Mount Products

Table 1. SOT–223 Medium Power TMOS FETs — Logic Level

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device[12]	I_D (cont) Amps	P_D[1] (Watts) Max	Application
60	0.18	0.75	***MMFT3055EL***	1.5	0.8[3]	dc–dc Converters Power Supplies Motor Controls, Disk Drives
20	0.15	1	***MMFT2N02EL***	2		

(1) T_C = 25°C
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(12) Available in tape and reel only — T1 suffix = 1000/reel, T3 suffix = 4000/reel.



CASE 369A–13
TO–252
STYLE 2

DPAK — N and P–Channel Surface Mount Products

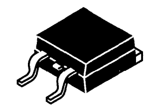
Table 2. DPAK — Logic Level

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device[4]	I_D (cont) Amps	P_D[1] (Watts) Max
100	0.22	5	***MTD10N10EL***	10	1.75[3]
60	0.12	7.5	***MTD15N06V***	15	
	0.18	6	***MTD3055VL***	12	
	0.15	10	***MTD20P06HDL***[5]	20	
	0.045	10	***MTD20N06HDL***	20	
30	0.099	10	***MTD20P03HDL***[5]	19	
	0.035	10	***MTD20N03HDL***	20	

(1) T_C = 25°C
(2) Indicates logic level
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) Available in tape and reel — add T4 suffix to part number.
(5) Indicates P–Channel

Devices listed in bold, italic are Motorola preferred devices.

Logic Level (continued)



CASE 418B–02
STYLE 2

Logic Level

D^2PAK — N and P–Channel Surface Mount Products

Table 3. D^2PAK — Logic Level

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device(4)	I_D (cont) Amps	P_D(1) (Watts) Max
60	0.05	15	***MTB30N06VL***	30	2.5(3)
	0.032	21	***MTB50N06VL***	42	
30	0.025	25	***MTB50P03HDL***(5)	50	
	0.0075	37.5	***MTB75N03HDL***	75	

(1) $T_C = 25°C$
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) Available in tape and reel — add T4 suffix to part number.
(5) Indicates P–Channel

CASE 221A–06
(TO–220AB)
STYLE 5

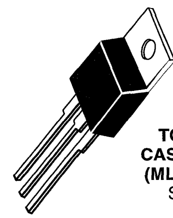
TO–220AB — N and P–Channel

Table 4. TO–220AB — Logic Level

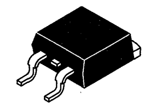
$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device	I_D (cont) Amps	P_D(1) (Watts) Max
100	0.22	5	***MTP10N10EL***	10	75
60	0.18	6	***MTP3055EL***	12	48
	0.18	6	***MTP3055VL***	12	
	0.05	15	***MTP30N06EL***	30	75
	0.05	15	***MTP30N06VL***	30	90
	0.028	25	***MTP50N06EL***	50	150
	0.032	21	***MTP50N06VL***	42	125
	0.028	26	***MTP52N06VL***	50	135
50	0.12	7.5	***MTP15N06VL***	15	65
	0.10	7.5	***MTP15N05EL***	15	150
	0.032	25	***MTP50N05EL***	50	
30	0.025	25	***MTP50P03HDL***(2)	50	
	0.0075	37.5	***MTP75N03HDL***	75	

(1) $T_C = 25°C$
(2) Indicates P–Channel

Devices listed in bold, italic are Motorola preferred devices.



TO–220AB
CASE 221A–06
(MLP PREFIX)
STYLE 5



CASE 418B–02
STYLE 2

N–Channel

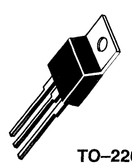
Insulated Gate Bipolar Transistors (IGBTs)

These devices make up a series of “smart” power devices that automatically clamp spikes in automotive ignition systems and guard against ESD. The devices feature a logic level IGBT (Insulated Gate Bipolar Transistor) with integral active collector clamp and ESD gate protection and are designed primarily as ignition coil drivers to withstand high current in a pulsed mode without latching.

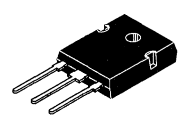
Table 1. N–Channel Ignition IGBTs

BV_{CES} (Volts) Clamped	$V_{CE(on)}$ @ 10 A	Device	P_D(1) (Watts) Max	Package
140 V	1.8	***MGP20N14CL***	150	TO–220AB
350 V	1.8	***MGP20N35CL*** ***MGB20N35CL***	150 2.5(3)(4)	TO–220AB D^2PAK
400 V	1.8	***MGP20N40CL*** ***MGB20N40CL***	150 2.5(3)(4)	TO–220AB D^2PAK

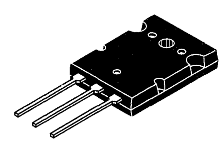
(1) $T_C = 25°C$
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) DPAK and D^2PAK packages available in tape and reel — add T4 suffix to part number.



TO–220
CASE 221A–06



TO–247AE
CASE 340F–03



TO–264
CASE 340G–02

Table 2. N–Channel, Standard and Copackaged IGBTs

Device	BV_{CES} (Volts)	I_C @ 90°C (A)	$V_{CE(on)}$ @ I_C (Volts) Max	P_D(1) Watts	Package
MGP5N60E	600	5	2.06 A @ 1.5 A	62	TO–220
MGP20N60		20	2.9 V @ 10 A	142	TO–220
MGW20N60D					TO–247
MGW30N60		30	2.9 V @ 15 A	202	TO–247
MGY30N60D					TO–264
MGY40N60		40	2.8 V @ 20 A	260	TO–264
MGY40N60D					TO–264
MGW12N120	1200	12	3.37 V @ 5 A	123	TO–247
MGW12N120D					TO–247
MGY25N120		25	3.24 V @ 12.5 A	212	TO–264

(1) $T_C = 25°C$

Devices listed in bold, italic are Motorola preferred devices.

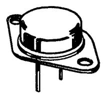
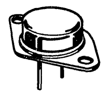
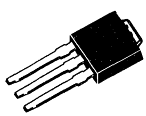
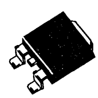
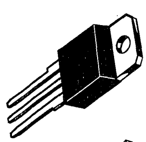
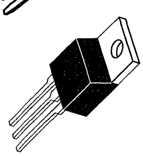
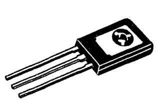
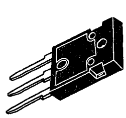
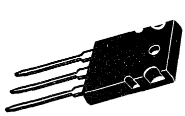
Bipolar Power Transistors

In Brief . . .

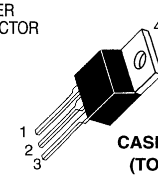
Motorola's broad line of Bipolar Power Transistors includes discrete and Darlington transistors in a variety of packages from the popular surface mount DPAK at 1.75 watts to the 250 watt TO-3 and TO–264. New products include the MJE/MJF 18000 series for lamp ballast and power supplies, MJW16212 — a new 1500 V deflection transistor for video monitor applications, and high performance audio output devices in the TO–264 package. We have the broadest line of Bipolar Power Transistors in the industry and the Motorola commitment to quality and total customer satisfaction to go with them.

Page

Bipolar Power Transistors
Selection by Package

Package		I_C Range (Amps)	V_{CE} Range (Volts)	P_D (Watts)	Page #
	**TO–204AA (TO–3) CASE 1–07**	4–30	40–1500	90–250	5.5–11
	**TO–204AE CASE 197A**	50–80	60–1000	150–300	5.5–11
	**DPAK CASE 369**	0.5–10	40–400	12.5–20	5.5–10
	**DPAK CASE 369A**	0.5–10	40–400	12.5–20	5.5–10
	**TO–218 TYPE CASE 340D**	5.0–25	60–1500	80–150	5.5–6
	**TO–220AB CASE 221A–06**	0.5–15	30–1800	30–125	5.5–3
	**TO–225AA (TO–126 TYPE) CASE 77**	0.3–5.0	25–400	12.5–40	5.5–8
	**TO–247 TYPE CASE 340F**	10–30	400–1500	125–180	5.5–7
	**TO–264 CASE 340G**	15–16	200–650	250	5.5–8

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



CASE 221A–06
(TO–220AB)

Table 1. Plastic TO–220AB

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min[8]	Device Type NPN	PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
0.5	350	MJE2360T		15 min	0.1				10 typ	30
		MJE2361T		40 min	0.1				10 typ	30
1	100	TIP29C	TIP30C	15/75	1	0.6 typ	0.3 typ	1	3	30
	250	TIP47		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	300	TIP48	MJE5730	30/150	0.3	2 typ	0.18 typ	0.3	10	40
	350	***TIP49***	***MJE5731***	30/150	0.3	2 typ	0.18 typ	0.3	10	40
	400	***TIP50***	***MJE5731A***[7]	30/150	0.3	2 typ	0.18 typ	0.3	10	40
2	100	***TIP112***[2]	***TIP117***[2]	500 min	2	1.7 typ	1.3 typ	2	25[1]	50
	400/700	***BUL44***		14/36	0.4	2.75[3]	0.175[3]	1	13 typ	50
	450/1000	***BUX85***		30	0.1	3.5	1.4	1	4	50
	450/1000	***MJE18002***		14/34	0.2	3[3]	0.17[3]	1	12 typ	40
	900/1800	***MJE1320***		3 min	1	4 typ	0.8 typ	1		80
3	80	BD241B	BD242B	25 min	1				3	40
	100	BD241C	BD242C	25 min	1				3	40
		TIP31C	***TIP32C***	25 min	1	0.6 typ	0.3 typ	1	3	40
	150		***MJE9780***	50/200	0.5				5 typ	40

[1] $|h_{FE}|$ @ 1 MHz
[2] Darlington
[3] Switching tests performed w/special application simulator circuit. See data sheet for details.
[7] V_{CEO} = 375 V
[8] When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

Devices listed in bold, italic are Motorola preferred devices.

Table 1. Plastic TO–220AB (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type NPN	PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
4	40		***MJE1123***	45/100	4				5	75
	60	***MJE800***(2)	***MJE700***(2)	750 min	1.5				1(1)	40
	80	***D44C12***	***D45C12***	40/120	0.2			1	40 typ	30
	400/700	***MJE13005***		6/30	3	3	0.7	3	4	60
5	100	***TIP122***(2)	***TIP127***(2)	1k min	3	1.5 typ	1.5 typ	4	4(1)	75
	250	2N6497		10/75	2.5	1.8	0.8	2.5	5	80
	300	***2N6498***		10/75	2.5	1.8	0.8	2.5	5	80
	400/700	***BUL45***		14/34	0.3	1.7(3)	0.15(3)	1	12 typ	75
	450/1000	MJE16002		5 min	5	3	0.3	3		80
	450/850	***MJE16004***		7 min	5	2.7	0.35	3		80
	450/1000	***MJE18004***		14/34	0.3	1.7	0.15	1.0	13	75
	550/1200	***MJE18204***		18/35	0.5	2.75(3)	0.2(3)	2	12	75
6	80	***BD243B***	***BD244B***	15 min	3	0.4 typ	0.15 typ	3	3	65
	100	***BD243C***	***BD244C***	15 min	3	0.4 typ	0.15 typ	3	3	65
		TIP41C	***TIP42C***	15/75	3	0.4 typ	0.15 typ	3	3	65
	250/550	***MJE16204***		5 min	6	1.5(2)	0.15(2)	1	10	80
	400/700	***BUL146***		14/34	0.5	1.75(3)	0.15(3)	3	14 typ	100
	450/1000	***MJE18006***		14/34	0.5	3.2(3)	0.13(3)	3	14 typ	100
7	30	2N6288	2N6111	30/150	3	0.4 typ	0.15 typ	3	4	40
	50		2N6109	30/150	2.5	0.4 typ	0.15 typ	3	4	40
	70	***2N6292***	***2N6107***	30/150	2	0.4 typ	0.15 typ	3	4	40
	100	***BD801***	***BD802***	15 min	3				3	65
	150	BU407		30 min	1.5		0.75	5	10	60
	200	***BU406***		30 min	1.5		0.75	5	10	60
	450	***BU522B***(2)		250 min	2.5				7.5	75

(1)$|h_{FE}|$ @ 1 MHz
(2)Darlington
(3)Switching tests performed w/special application simulator circuit. See data sheet for details.
(7)V_{CEO} = 375 V
(8)When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

Devices listed in bold, italic are Motorola preferred devices.

Table 1. Plastic TO–220AB (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
8	60	2N6043(2)	2N6040(2)	1k/10k	4	1.5 typ	1.5 typ	3	4(1)	75
	80	***2N6044***(2)	***2N6041***(2)	1k/10k	4	1.5 typ	1.5 typ	3	4(1)	75
		BDX53B(2)	***BDX54B***(2)	750 min	3				4(1)	60
	100	***2N6045***(2)	***2N6042***(2)	1k/10k	3	1.5 typ	1.5 typ	3	4(1)	75
		BDX53C(2)	***BDX54C***(2)	750 min	3					
		TIP102(2)	***TIP107***(2)	1k/20k	3	1.5 typ	1.5 typ	3	4(1)	80
	120	MJE15028	MJE15029	20 min	4				30	50
	150	***MJE15030***	***MJE15031***	20 min	4				30	50
	200	***BU806***(2)		100 min	5	0.55 typ	0.2 typ	5		60
	300/600	MJE5740(2)		200 min	4	8 typ	2 typ	6	4	80
			MJE5850	15 min	2	2	0.5	4		80
	350	***MJE5741***(2)		200 min	4	8 typ	2 typ	6		80
			MJE5851	15 min	2	2	0.5	4		80
		MJE5742(2)		200 min	4	8 typ	2 typ	6		80
		MJE13007		5/30	5	3	0.7	5		80
			MJE5852	15 min	2	2	0.5	4		80
	400/650	***MJE16106***		6/22	8	2 typ	0.1 typ	5		100
	400/700	***BUL147***		14/34	1	2.5(3)	0.18(3)	2	14 typ	125
	450/1000	***MJE18008***		16/34	1	2.75(3)	0.18(3)	2	13 typ	125
10	20		***BD808***	15 min	4				1.5	90
	60	D44H8	D45H8	40 min	4					50
		MJE3055T	***MJE2955T***	20/70	4					75
		2N6387(2)	***2N6667***(2)	1k/20k	5				20(1)	65
	80	***BDX33B***(2)	***BDX34B***(2)	750 min	3				3	70
		BD809	***BD810***	15 min	4				1.5	90
		2N6388(2)	***2N6668***(2)	1k/20k	5				20(1)	65
		D44H10	D45H10	20 min	4	0.5 typ	0.14 typ	5	50 typ	50
		D44H11	***D45H11***	40 min	4	0.5 typ	0.14 typ	5	50 typ	50

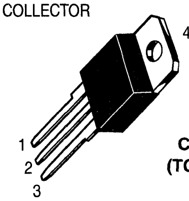
(1)$|h_{FE}|$ @ 1 MHz
(2)Darlington
(3)Switching tests performed w/special application simulator circuit. See data sheet for details.
(7)V_{CEO} = 375 V
(8)When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.
(9)Self protected Darlington

Devices listed in bold, italic are Motorola preferred devices.

Table 1. Plastic TO–220AB (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
10	100	***BDX33C***(2)	***BDX34C***(2)	750 min	3				3	70
	450/1000	***MJE18009***		14/34	1.5	2.75(3)	0.2(3)	3	12	150
12	400/700	***MJE13009***		6/30	8	3	0.7	8	4	100
15	80	***2N6488***	***2N6491***	20/150	5	0.6 typ	0.3 typ	5	5	75
		D44VH10	***D45VH10***	20 min	4	0.5	0.09	8	50 typ	83
	100	***BDW42***(2)	***BDW47***(2)	1k min	5	1 typ	1.5 typ	5	4	85

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



CASE 340D
(TO–218 Type,
SOT–93)

Table 2. Plastic TO–218 Type

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
8	500/1000	***MJH16006A***		5 min	8	2.5	0.25	5		125
10	60	TIP140(2)	TIP145(2)	500 min	10	2.5 typ	2.5 typ	5	4(1)	125
		TIP141(2)	TIP146(2)	500 min	10	2.5 typ	2.5 typ	5	4(1)	125
	100	***BDV65B***(2)	***BDV64B***(2)	1k min	5					125
		TIP33C	TIP34C	20/100	3				3	80
		TIP142(2)	***TIP147***(2)	500 min	10	2.5 typ	2.5 typ	5	4(1)	125
	400	***BU323AP***(2)		150/100	6	15	15	6		125
		MJH10012(2)		100/2k	6	15	15	6		118

(1)$|h_{FE}|$ @ 1 MHz
(2)Darlington
(8)When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

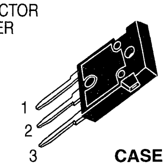
Devices listed in bold, italic are Motorola preferred devices.

Table 2. Plastic TO–218 Type (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
15	60	***TIP3055***	***TIP2955***	5 min	10				2.5	80
	150	MJH11018(2)	MJH11017(2)	400/15k	10				3	150
	200	MJH11020(2)	MJH11019(2)	400/15k	10				3	150
	250	***MJH11022***(2)	***MJH11021***(2)	400/15k	10				3	150
	400	BUV48		8 min	10	2	0.4	10		150
	450	***BUV48A***		8 min	8	2	0.4	10		150
16	140	MJE4342	MJE4352	15 min	8	1.2 typ	1.2 typ	8	1	125
	160	***MJE4343***	***MJE4353***	15 min	8	1.2 typ	1.2 typ	8	1	125
20	60	MJH6282(2)	MJH6285(2)	750/18k	10				4	125
	100	***MJH6284***(2)	***MJH6287***(2)	750/18k	10				4	125
25	80	TIP35A	TIP36A	15/75	15	0.6 typ	0.3 typ	10	3	125
	100	***BD249C***	***BD250C***	10 min	15				3	125
		TIP35C	***TIP36C***	15/75	15	0.6 typ	0.3 typ	10	3	125

(2)Darlington
(8)When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER



CASE 340F
(TO–247 Type)

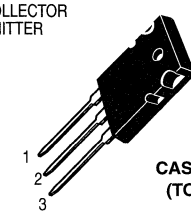
Table 3. Isolated Mounting Hole — Plastic TO–247 Type

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
10	650	1500	***MJW16212***		4/10	10	4(3)	0.5(3)	5.5		150
	800	1500	***MJW16018***		4 min	5	4.5 typ	0.2 typ	5	3 typ	150
12	500	1200	***MJW16206***		5/13	10	2.25	0.25	6.5	3 typ	150
15	450	850	***MJW16010***		5 min	15	1.2 typ	0.2 typ	10		150
		850	***MJW16012***		7 min	15	0.9 typ	0.15 typ	10		150
	500	1000	***MJW16010A***		5 min	15	3	0.4	10		150

(3)Switching tests performed w/special application simulator circuit. See data sheet for details.
(10)Tested in Applications simulator: see Data Sheet.

Devices listed in bold, italic are Motorola preferred devices.

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER



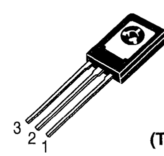
CASE 340G
(TO–264)

Table 4. Large Plastic TO–264

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	PNP	hFE Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
15	200	***MJL3281A***	***MJL1302A***	60/175	0.1				30 typ	200
	650/1500	***MJL16218***		4/11	12				2.5 typ	170
16	250	***MJL21194***	***MJL21193***	25/75	8				4	200

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER



CASE 77
(TO–225AA)

Table 5. Plastic TO–225AA Type (Formerly TO–126 Type)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
0.3	350	***MJE3439***		40/160	0.02				15	15
0.5	150	MJE341		25/200	0.05				15	20.8
	200	***MJE344***		30/300	0.05				15	20.8
	250	2N5655		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
		BD157		30/240	0.05					20
	300	***BD158***		30/240	0.05					20
		MJE340	***MJE350***	30/240	0.05					20.8
		2N5656		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20

Devices listed in bold, italic are Motorola preferred devices.

Table 5. Plastic TO–225AA Type (Formerly TO–126 Type) (continued)

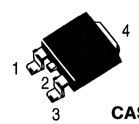
I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
0.5	350	***2N5657***		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
		BD159		30/240	0.05					20
1	40	2N4921	2N4918	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
	60	2N4922	2N4919	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
	80	***2N4923***	***2N4920***	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
1.5	45	***BD165***	***BD166***	15 min	0.5				6	20
		BD135	BD136	40/250	0.15					12.5
	60	BD137	BD138	40/250	0.15					12.5
	80	***BD169***		15 min	0.5				6	20
		BD139	***BD140***	40/250	0.15					12.5
			BD140–10	63/160	0.15					12.5
	300	MJE13002(11)		5/25	1	4	0.7	1	5	40
	400	***MJE13003***(11)		5/25	1	4	0.7	1	5	40
2	80	***BD237***	***BD238***	25 min	1				3	25
	100	***MJE270***(2)(11)	***MJE271***(2)(11)	1.5k min	0.12				6	15
3	60	MJE181	MJE171	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	80	***BD179***	***BD180***	40/250	0.15				3	30
		MJE182	***MJE172***	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	200	***BUY49P***		30 min	0.5				25	20
4	40	***MJE521***	***MJE371***	40 min	1					40
	45	***BD437***	***BD438***	40 min	2				3	36
			BD776(2)	750 min	2				20	15
	60		***BD440***	25 min	2				3	36
		BD677(2)	***BD678***(2)	750 min	1.5					40
		BD677A(2)	***BD678A***(2)	750 min	2					40
		BD787	***BD788***	20 min	2				50	15
		BD777(2)	***BD778***(2)	750 min	2				20	15
		2N5191	***2N5194***	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
		MJE800(2)	***MJE700***(2)	750 min	1.5				1(1)	40
		2N6038(2)	***2N6035***(2)	750/18k	2	1.7 typ	1.2 typ	2	25	40
	80	***2N5192***	***2N5195***	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
		BD441	***BD442***	15 min	2				3	36
		BD679(2)	***BD680***(2)	750 min	1.5					40
		BD679A(2)	***BD680A***(2)	750 min	2					40
		BD789	***BD790***	10 min	2				40	15

(1) $|h_{FE}|$ @ 1 MHz
(2) Darlington
(11) Case 77, Style 3

Devices listed in bold, italic are Motorola preferred devices.

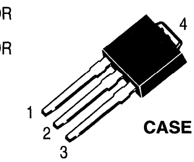
Table 5. Plastic TO–225AA Type (Formerly TO–126 Type) (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
4	80	***BD779***[2]	***BD780***[2]	750 min	2				20	15
		MJE802[2]	MJE702[2]	750 min	1.5				1[1]	40
		MJE803[2]	***MJE703***[2]	750 min	2				1[1]	40
		2N6039[2]	***2N6036***[2]	750/18k	2	1.7 typ	1.2 typ	2	25	40
	100	***BD681***[2]	***BD682***[2]	750 min	1.5					40
		BD791	***BD792***	10 min	2				40	15
		MJE243	***MJE253***	40/120	0.2	0.15 typ	0.07 typ	2	40	15
5	25	***MJE200***	***MJE210***	45/180	2	0.13 typ	0.035 typ	2	65	15



CASE 369A[13]

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



CASE 369[12]

Table 6. DPAK – Surface Mount Power Packages

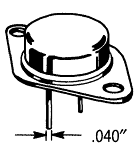
I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
0.5	300	***MJD340***	***MJD350***	30/240	0.05					15
1	250	MJD47		30/150	0.3	2	0.2	0.3	10	15
	375		***MJD5731***	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	400	***MJD50***		30/150	0.3	2	0.2	0.3	10	15
1.5	400	***MJD13003***		5/25	1	4	0.7	1	4	15

(1) $|h_{FE}|$ @ 1 MHz
(2) Darlington
(12) Case 369–07 may be ordered by adding –1 suffix to part number.
(13) Case 369A–13 may be ordered as tape and reel by adding a "T4" suffix; 2500 units/reel.

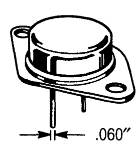
Devices listed in bold, italic are Motorola preferred devices.

Table 6. DPAK – Surface Mount Power Packages (continued)

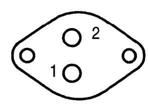
I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
2	100	***MJD112***[2]	***MJD117***[2]	1000 min	2	1.7	1.3	2	25[1]	20
3	40	MJD31	MJD32	10 min	1	0.6	0.3	1	3	15
	100	***MJD31C***	***MJD32C***	10 min	1	0.6	0.3	1	3	15
4	80	***MJD6039***[2]	***MJD6036***[2]	1k/12k	2	1.7	1.2	2	25	20
	100	***MJD243***	***MJD253***	40/180	0.2	0.16	0.04	1	40	12.5
5	25	***MJD200***	***MJD210***	45/180	2	0.15	0.04	2	65	12.5
6	100	***MJD41C***	***MJD42C***	15/75	3	0.4	0.15	3	3	20
8	80	***MJD44H11***	***MJD45H11***	40 min	4	0.5	0.14	5	50 typ	20
	100	***MJD122***[2]	***MJD127***[2]	1k/12k	4	1.5	2	4	4[1]	20
10	60	***MJD3055***	***MJD2955***	20/100	4	1.5	1.5	3	2	20
	80	***MJD44E3***[2]		1k min	5	2	0.5	10		20



CASE 1–07
TO–204AA



CASE 197A TO–204AE
(Used for high current types at end of table. See types w/footnote(16).)



STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

Table 7. Metal TO–204AA (Formerly TO–3), TO–204AE

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min[8]	Device Type NPN	PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
4	200	MJ15018		30 min	1				20	150
	250	***MJ15020***	***MJ15021***	30 min	1				20	150
5	700/1500	***BU208A***		2.5 min	4.5	8 typ	0.4 typ	4.5	4 typ	90
8	60	MJ1000[2]		1k min	3					90
		2N6055[2]		750/18k	4	1.5 typ	1.5 typ	4	4[1]	100
	80	***MJ1001***[2]		1k min	3					90
		2N6056[2]		750/18k	4	1.5 typ	1.5 typ	4	4[1]	100

(1) $|h_{FE}|$ @ 1 MHz
(2) Darlington
(8) When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.
(12) Case 369 may be ordered by adding –1 suffix to part number.
(13) Case 369A may be ordered as tape and reel by adding a "T4" suffix; 2500 units/reel.

Devices listed in bold, italic are Motorola preferred devices.

Table 7. Metal TO–204AA (Formerly TO–3), TO–204AE (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min[8]	Device Type NPN	PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
10	60	2N3715	2N3791	30 min	3	0.3 typ	0.4 typ	5	4	150
		MJ3000[2]	MJ2500[2]	1k min	5					150
	80	2N3716	2N3792	30 min	3	0.3 typ	0.4 typ	5	4	150
		2N5878		20/100	4	1	0.8	4	4	150
		MJ3001[2]	***MJ2501***[2]	1k min	5					150
	140	2N3442		20/70	4					117
	250	***MJ15011***	***MJ15012***	20/100	2					200
	325	***MJ413***		20/80	0.5				2.5	125
		MJ423		30/90	1				2.5	125
	400	***BU323A***[2]		150 min	6	7.5 typ	5.2 typ	6		175
		MJ10007[2]		30/300	5	1.5	0.5	5	10[1]	150
		MJ10012[2]		100/2k	6	15	15	6		175
12	60	2N6057[2]	2N6050[2]	750/18k	6	1.6 typ	1.5 typ	6	4[1]	150
	80	2N6058[2]	2N6051[2]	750/18k	6	1.6 typ	1.5 typ	6	4[1]	150
	100	***2N6059***[2]	***2N6052***[2]	750/18k	6	1.6 typ	1.5 typ	6	4[1]	150
15	60	***2N3055***	***MJ2955***	20/70	4	0.7 typ	0.3 typ	4	2.5	115
		2N3055A	***MJ2955A***	20/70	4				0.8	115
		2N6576[2]		2k/20k	4	2	7	10	10–200[1]	120
		2N5881	2N5879	20/100	6	1	0.8	6	4	160
	80	***2N5882***	***2N5880***	20/100	6	1	0.8	6	4	160
	90	2N6577[2]		2k/20k	4	2	7	10	10–200[1]	120
	120	***MJ15015***	***MJ15016***	20/70	4	0.7 typ	0.3 typ	4	1	180
		2N6578[2]		2k/20k	4	2	7	10	10–200[1]	120
	140	MJ15001	MJ15002	25/150	4				2	200
	150	MJ11018[2]	MJ11017[2]	100 min	15				3[1]	175
	200	MJ11020[2]		100 min	15				3[1]	175
		MJ3281A	***MJ1302A***	60/175	0.1				30 typ	250
	250	***MJ11022***[2]	MJ11019[2]	100 min	15				3[1]	175
			MJ11021[2]	6/30	10	4	0.7	10	6 to 24	175
	400/850	***BUX48***		8 min	10	2	0.4	10		175
		2N6547		6/30	10	4	0.7	10	6 to 24	175
	400/650	***MJ16110***		6/20	15	0.8 typ	0.1 typ	10		175
	450/1000	***BUX48A***		8 min	8	2	0.4	10		175

[1] $|h_{FE}|$ @ 1 MHz
[2] Darlington
[8] When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

Devices listed in bold, italic are Motorola preferred devices.

Table 7. Metal TO–204AA (Formerly TO–3), TO–204AE (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
15	450/850	MJ16010		5 min	15	1.2 typ	0.2 typ	10		175
		MJ16012		7 min	15	0.9 typ	0.15 typ	10		175
16	140	***2N3773***	2N6609	15/60	8	1.1 typ	1.5 typ	8	4	150
		2N5631	2N6031	15/60	8	1.2 typ	1.2 typ	8	1	200
	200	MJ15022	MJ15023	15/60	8				5	250
	250	***MJ15024***	***MJ15025***	15/60	8				5	250
		MJ21194	***MJ21193***	25/75	8				4	250
20	60	***2N3772***		15/60	10				2	150
		2N6282(2)	2N6285(2)	750/18k	10	2.5 typ	2.5 typ	10	4(1)	160
	75	2N5039		20/100	10	1.5	0.5	10	60	140
	80	***2N6283***(2)	2N6286(2)	750/18k	10	2.5 typ	2.5 typ	10	4(1)	160
	90	2N5038		20/100	12	1.5	0.5	12	60	140
	100	***2N6284***(2)	***2N6287***(2)	750/18k	10	2.5 typ	2.5 typ	10	4(1)	160
	140	***MJ15003***	***MJ15004***	25/150	5				2	250
	200	***BUV11***		10 min	12	1.8	0.4	12	8	150
	350	***MJ10000***(2)		40/400	10	3	1.8	10	10(1)	175
	400	***MJ10005***(2)		40/400	10	1.5	0.5	10	10(1)	175
		MJ13333		10/60	5	4	0.7	10		175
	500	***MJ10009***(2)		30/300	10	2	0.6	10	8(1)	175
25	60	2N5885	2N5883	20/100	10	1	0.8	10	4	200
	80	***2N5886***	***2N5884***	20/100	10	1	0.8	10	4	200
			2N6436	30/120	10	1	0.25	10	40	200
	100	2N6338	2N6437	30/120	10	1	0.25	10	40	200
	120	2N6339	***2N6438***	30/120	10	1	0.25	10	40	200
	140	2N6340		30/120	10	1	0.25	10	40	200
	150	***2N6341***		30/120	10	1	0.25	10	40	200
30	40	***2N3771***		15/60	15				2	150
		2N5301	2N4398	15/60	15	2	1	10	2	200
	60	2N5302	2N4399	15/60	15	2	1	10	2	200
		MJ11012(2)	MJ11011(2)	1k min	20				4(1)	200
	90	***MJ11014***(2)	***MJ11013***(2)	1k min	20				4(1)	200
	100	2N6328		6/30	30				3	200
		MJ802	***MJ4502***	25/100	7.5				2	200
	120	***MJ11016***(2)	***MJ11015***(2)	1k min	20				4(1)	200

(1)$|h_{FE}|$ @ 1 MHz
(2)Darlington
(8)When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

Devices listed in bold, italic are Motorola preferred devices.

Table 7. Metal TO–204AA (Formerly TO–3), TO–204AE (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min[8]	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
30	325	***BUV23***		8 min	16	1.8	0.4	16	8	250
	400/1000	***BUS98***		8 min	20	2.3	0.4	20		250
		BUX98		8 min	20	3	0.8	20		250
	450/850	MJ16020[16]		5 min	30	1.8	0.2	20		250
		MJ16022[16]		7 min	30	1.5	0.15	20		250
	450/1000	***BUS98A***		8 min	16	2.3	0.4	16		250
		BUX98A		8 min	16	3	0.8	16		250
40	200	BUV21[16]		10 min	25	1.8	0.4	25	8	150
	250	***BUV22***[16]		10 min	20	1.1	0.35	20	8	250
	350	MJ10022[2][16]		50/600	10	2.5	0.9	20		250
	400	***MJ10023***[2][16]		50/600	10	2.5	0.9	20		250
50	60	2N5685[16]		15/60	25	0.5 typ	0.3 typ	25	2	300
	80	***2N5686***[16]	***2N5684***[16]	15/60	25	0.5 typ	0.3 typ	25	2	300
	90	***MJ11030***[2][16]	***MJ11031***[2][16]	400 min	50					300
	100	2N6274[16]		30/120	20	0.8	0.25	20	30	250
	120	2N6275[16]	***2N6379***[16]	30/120	20	0.8	0.25	20	30	250
		MJ11032[2][16]	***MJ11033***[2][16]	400 min	50					300
	125	***BUV20***[16]		10 min	50	1.2	0.25	50	8	250
		BUV60[16]		10 min	80	1.1	0.25	80		250
	150	***2N6277***[16]		30/120	20	0.8	0.25	20	30	250
	400	***MJ10015***[2][16]		10 min	40	2.5	1	20		250
	500	***BUT34***[2][16]		15 min	32	3	1.5	32		250
		MJ10016[2][16]		10 min	40	2.5	1	20		250
56	400	***BUT33***[2][16]		20 min	36	3.3	1.6	36		250
60	60		MJ14001[16]	15/100	50					300
	80	***MJ14002***[16]	***MJ14003***[16]	15/100	50					300
	200	MJ10020[2][16]		75 min	15	3.5	0.5	30		250
	250	***MJ10021***[2][16]		75 min	15	3.5	0.5	30		250
70	125	***BUS50***[16]		15 min	50	1.5	0.3	70		350
80	100	***BUV18A***[16]		10 min	80	1.1	0.25	80		250

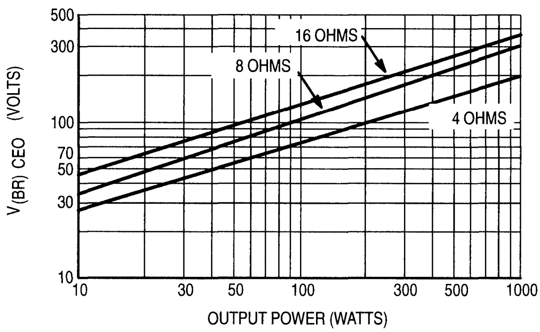
[1] $|h_{FE}|$ @ 1 MHz
[2] Darlington
[8] When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.
[16] Case 197A–03 (TO–204AE)

Devices listed in bold, italic are Motorola preferred devices.

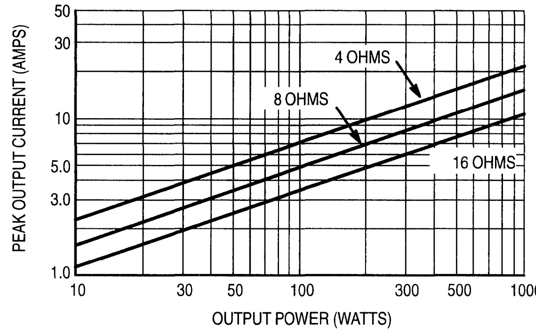
Audio

GENERAL DESIGN CURVES FOR POWER AUDIO OUTPUT STAGES

$V_{(BR)CEO}$ Required on Output and Driver Transistor versus Output Power for 4, 8 and 18 Ohm Loads



Output Transistor Peak Collector Current versus Output Power for 4, 8 and 16 Ohm Loads



Another important parameter that must be considered before selecting the output transistors is the safe–operating area these devices must withstand. For a complete discussion see Application Note AN485.

Table 8. Recommended Power Transistors for Audio/Servo Loads

RMS Power Output	NPN	PNP	Case	P_D Watts @ 25°C	V_{CEO}	h_{FE} @ Min/Max	I_C Amps	f_T MHz Typ	ISB Volts/Amps
To 25W	MJE15030	MJE15031	TO–220	50	150	20 min	4	30	14/3.6
	MJE15032	MJE15033	TO–220	50	250	50 min	1	40	50/1
25 to 50W	2N3055A	MJ2955A	TO–204	120	120	20/70	4	3	60/2
	MJ15001	MJ15002	TO–204	200	140	25/150	4	3	40/5
50 to 100W	MJ15015	MJ15016	TO–204	180	120	20/70	4	3	60/3
	MJ15003	MJ15004	TO–204	250	140	25/150	5	3	100/1
	MJ15020	MJ15021	TO–204	150	250	30 min	1	20	50/3
Over 100W	MJ15024	MJ15025	TO–204	250	250	15/60	8	8	80/2.2
	MJ3281A	MJ1302A	TO–204	250	200	60/175	7	30	50/4
	MJL3281A	MJL1302A	340G–01	150	200	60/175	7	30	40/4
	MJ21194	MJ21193	TO–204	250	250	25/75	8	7	100/2
	MJL21194	MJL21193	340G–01	200	200	25/75	8	7	100/2

The Power Transistors shown are provided for reference only and show device capability. The final choice of the Power Transistors used is left to the circuit designer and depends upon the particular safe–operating area required and the mounting and heat sinking configuration used.

Electronic Lamp Ballasts

As in many other areas of its semiconductor activity, Motorola is an industry leader in the fast growing market of Electronic Ballast Semiconductors. We introduced the first dedicated devices for this market in 1988. Today, devices based on advanced technologies such as H2BIP (High Gain, High Frequency Bipolar) and ZPCMOS (Zero Power Control MOS) are leading the way in providing benefits for ballast manufacturers, consumers and the environment.

Two factors make the Electronic Lamp Ballast market grow at an ever increasing rate — Economics and the Environment.

Lamps based on Electronic Ballasts have long lifetimes and very low power consumption, so contributing to the efficient use of energy and to preservation of the environment. Motorola designs silicon solutions specifically for these applications.

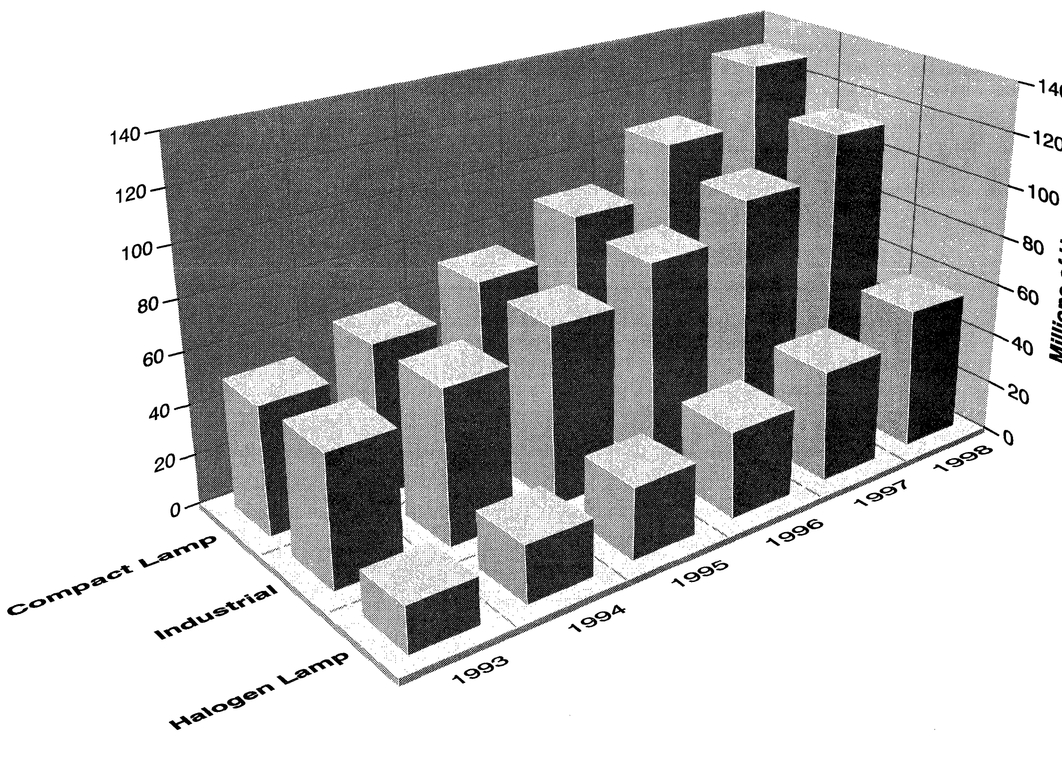
For this growing ballast market Motorola offers optimized devices such as Power MOSFETs, Bipolar Transistors, Linear drive ICs, custom Start–Stop ICs, Diodes and Silicon Bilateral Switches.

Even more important are our efforts to develop the technology for tomorrow in close cooperation with the world's leading manufacturers of Electronic Transformers and Lamp Ballasts, as well as assisting them today in their choice of technology.

This capability is driven from our centre of competence based in Toulouse, France. An important team of Applications, Design, Product, Manufacturing and Marketing Engineers drives our worldwide dedication to this market.

The intention of this section is to provide you with a 'snapshot' of our bipolar transistor products and capabilities. It is a document showing Motorola's professionalism in this area, and illustrating some of the expertise available to *you* — the Electronic Lamp Ballast manufacturer.

World Lamp Ballast Market



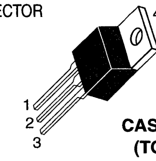
Cross Reference Transistors for Electronic Lamp Ballasts

Industry Part Number	Motorola Direct Replacement	Motorola Nearest Replacement
2SC4053		MJE18004
2SC4546		BUL146F
2SC4630		MJF18004
2SC4820		MJF18002
BU1706A		MJE18604D2
BU1708A		MJE18604D2
BUD43B–1	BUD43B–1	
BUF610		MJE18004D2
BUF654		BUL146
BUH100	BUH100	
BUH150	BUH150	
BUH50	BUH50	
BUH51	BUH51	
BUL146	BUL146	
BUL146F	BUL146F	
BUL147	BUL147	
BUL147F	BUL147F	
BUL213		MJE18204
BUL216		MJE18206
BUL381		BUL45
BUL38D		BUL45D2
BUL410		MJE18006
BUL416		MJE18604D2
BUL43B	BUL43B	
BUL44	BUL44	
BUL44D2	BUL44D2	
BUL44F	BUL44F	
BUL45	BUL45	
BUL45D2	BUL45D2	
BUL45F	BUL45F	
BUL48		MJE18004D2
BUL510		MJE18004D2
BUL57		BUL147
BUL67		BUL147
BUL810		BUV48A
BUL87		BUL147
BULD215		BUL45D2

Industry Part Number	Motorola Direct Replacement	Motorola Nearest Replacement
BULD50		BUL44D2
BULD85		BUL45D2
BUT11AF		MJF18004
BUT18		BUH100
BUT93		BUL45
BUT93D		BUL44D2
BUV46		MJE18006
KSC5021F		MJE18004
KSC5027F		MJE18604D2
MJD13003–1	MJE13003–1	
MJE13003	MJE13003	
MJE13005	MJE13005	
MJE13007	MJE13007	
MJE13009	MJE13009	
MJE18002	MJE18002	
MJE18004	MJE18004	
MJE18004D2	MJE18004D2	
MJE18006	MJE18006	
MJE18008	MJE18008	
MJE18009	MJE18009	
MJE18204	MJE18204	
MJE18206	MJE18206	
MJE18604D2	MJE18604D2	
MJF18002	MJF18002	
MJF18004	MJF18004	
MJF18006	MJF18006	
MJF18008	MJF18008	
MJF18009	MJF18009	
MJF18204	MJF18204	
MJF18206	MJF18206	
TD13003		MJD13003–1
TD13004		BUF43B–1
TEO13005D		BUL44D2–1
TEO13007	MJE13007	
TEO13003	MJE13003	
TEO13005	MJE13005	
TEO13009	MJE13009	

Cross Reference Transistors for Electronic Lamp Ballasts

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



CASE 221A–06
(TO–220AB)

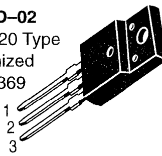
Table 9. TO–220AB Bipolar Transistors

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1 V	Inductive Switching @ I_C Operating T_{si} Min/Max (μs)	P_D (Case) Watts @ 25°C
2	350	650	BUL43B	0.8	9	1.8 / 3.3	40
	400	700	BUL44	0.8	10	2.6 / 3.8	50
	400	700	BUL44D2*	0.8	20	2.05 / 2.35	50
	450	1000	MJE18002	1	6	/ 2.75	50
4	500	800	BUH50	2	8 typ	/ 2.5	50
5	400	700	BUL45	2	7	2.6 / 3.8	75
	400	700	BUL45D2*	2	10	1.95 / 2.25	75
	450	1000	MJE18004	2	6	/ 2.5	75
	450	1000	MJE18004D2*	2	6	2.1 / 2.4	75
	550	1200	MJE18204	2	5	/ 2.75	75
	600	1600	MJE18604D2*	0.5	15	/ 1.0	75
6	400	700	BUL146	3	8	2.6 / 3.8	100
	450	1000	MJE18006	3	6	/ 3.2	100
8	400	700	BUL147	4.5	8	2.6 / 3.8	125
	450	1000	MJE18008	4.5	6	/ 3.2	125
	550	1200	MJE18206	3	5	/ 2.75	100
10	400	700	BUH100	5	10 typ	/ 3.0	100
	450	1000	MJE18009	7	8	/ 2.75	150
15	400	700	BUH150	10	8 typ	/ 2.75	150

BUHXXX Series are specified for Halogen applications.
* D2 suffix indicates transistor with built in C–E freewheeling diode and antisaturation network.

Cross Reference Transistors for Electronic Lamp Ballasts

CASE 221D–02
Isolated TO–220 Type
UL Recognized
File #E69369

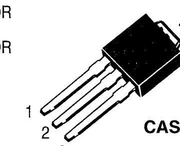


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

Table 10. Isolated TO–220 Bipolar Transistors

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1 V	Inductive Switching @ I_C Operating T_{si} Min/Max (μs)	P_D (Case) Watts @ 25°C
2	400	700	BUL44F	0.8	10	2.6 / 3.8	25
	450	1000	MJF18002	1	6	/ 2.75	25
5	400	700	BUL45F	2	7	2.6 / 3.8	35
	450	1000	MJF18004	2	6	/ 2.5	35
	550	1200	MJF18204	2	5	/ 2.75	40
6	400	700	BUL146F	3	8	2.6 / 3.8	40
	450	1000	MJF18006	3	6	/ 3.2	40
8	400	700	BUL147F	4.5	8	2.6 / 3.8	45
	450	1000	MJF18008	4.5	6	/ 3.2	45
	550	1200	MJF18206	5	6	/ 2.75	45
10	450	1000	MJF18009	7	8	/ 2.75	50

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



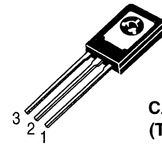
CASE 369–07

Table 11. DPAK Bipolar Transistors

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1 V	Inductive Switching @ I_C Operating T_{si} Min/Max (μs)	P_D (Case) Watts @ 25°C
2	350	650	BUD43B–1	0.8	9 typ	1.8 / 3.3	25
	400	700	BUD44D2–1*	0.8	20 typ	2.05 / 2.35	25

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER



CASE 77–08
(TO–225AA)

Table 12. Case 77 (TO–225) Bipolar Transistors

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1 V	Inductive Switching @ I_C Operating T_{si} Min/Max (μs)	P_D (Case) Watts @ 25°C
1.5	400	700	MJE13003	1	6 typ	/ 3.0	40
4	400	700	BUH51	1	8	/ 3.75	50

BUHXXX Series are specified for Halogen applications.
* D2 suffix indicates transistor with built in C–E freewheeling diode and antisaturation network.

Rectifiers

In Brief . . .

Continuing investment in research and development for discrete products has created a rectifier manufacturing facility that matches the precision and versatility of the most advanced integrated circuits. As a result, Motorola's silicon rectifiers span all high tech applications with quality levels capable of passing the most stringent environmental tests . . . including those for automotive under–hood applications. Additionally, the introduction of Motorola's first generation GaAs power devices is pushing the limits of today's rectifier technology.

Product Highlights:

- GaAs Rectifiers Power Manager™ with incredibly soft and hyperfast (<15 ns) reverse recovery are ideally suited for high frequency power supplies, free wheeling diodes, and as polarity protection diodes.
- Surface Mount Devices — A major thrust has been the development and introduction of a broad range of power rectifiers, Schottky and Ultrafast, 1/2 amp to 25 amp, 15 to 600 volts.
- Application Specific Rectifiers —
  - — MEGAHERTZ™ series for high frequency power supplies and power factor correction.
  - — Schottky rectifiers having lower forward voltage drop (0.3 to 0.6 volts) for use in low voltage SMPS outputs and as "OR"ing diodes.
  - — Automotive transient suppressors.
- Ultrafast rectifiers having reverse recovery times as low as 25 ns to complement the Schottky devices for higher voltage requirements in high frequency applications.
- A wide variety of package options to match virtually any potential requirement.

The rectifier selector section that follows has generally been arranged by package and technology. The individual tables have been sorted by voltage and current with the package types for the devices listed shown above each table. The Application Specific Rectifiers are also included in their respective tables.

Motorola's commitment to Six–Sigma is showing its worth. Refined processes no longer produce fallout as such and therefore only **Motorola Preferred Devices** are listed in the tables. The non–preferred devices will continue to be offered, but customers are encouraged to begin designing using the preferred types.

RECTIFIER NUMBERING SYSTEM

PART NUMBER KEY XXX X XX XX XX X

PREFIX (TYPE DESIGNATOR) — XXX

X:
F = FULLY ISOLATED
S = SURFACE MT (SMB/SMC)
D = DPAK
B = D^2PAK
H = MEGAHERTZ
V = D^3PAK

XX: I_O

XX: V_R (X10 EXCEPT SCHOTTKY)

XX: SUFFIX (DUAL DESIGNATOR)

X:
R = REVERSE
L = LOW V_F
E = ENERGY

PREFIX KEY

MUR = MOTOROLA ULTRA FAST RECTIFIER
MBR = MOTOROLA (SCHOTTKY) BARRIER RECTIFIER
MGR = MOTOROLA GaAs RECTIFIER
MR = MOTOROLA STANDARD & FAST RECOVERY

SUFFIX KEY

CT = CENTER TAP (DUAL) TO–220, TO–3, POWERTAP II
PT = CENTER TAP (DUAL) TO–218 PACKAGE
WT = CENTER TAP (DUAL) TO–247 / TO–3P

EXAMPLE:	MUR	30	20	WT
	MOTOROLA ULTRAFAST	30 AMP	200 V	CENTER TAP (DUAL) TO–247
EXAMPLE:	MBR	30	45	WT
	MOTOROLA SCHOTTKY	30 AMP	45 V	CENTER TAP (DUAL) TO–247

Application Specific Rectifiers

The focus for Rectifier Products continues to be on Schottky and Ultrafast technologies, with process and packaging improvements to achieve greater efficiency in high frequency switching power supplies, and high current mainframe supplies. Our new product thrust is intended to be more "application specific" than in the past, while continuing to strive for broad market acceptance.

Table 1. Low V_F Schottky Rectifiers

State of the art geometry is used in low V_F Schottky devices for improved efficiency in low voltage, high frequency switching power supplies, free–wheeling diodes, polarity protection diodes and "OR"ing diodes.

Device	I_O Amps	V_{RRM} (Volts)	V_F @ Rated I_O and Temperature Volts (Max)	I_R @ Rated V_{RRM} mAmps (Max)	Package
MBR0520LT1	0.5	20	0.33	0.25	SOD–123
MBRS130LT3	1	30	0.395	1	SMB
MBRD835L	8	35	0.41	1.4	DPAK
MBRD1035CTL	10	35	0.41	6	DPAK
MBR2030CTL	20	30	0.48	5	TO–220
MBRB2535CTL	25	35	0.41	10	D^2PAK
MBR2535CTL	25	35	0.41	5	TO–220
MBRB2515L	25	15	0.42	15	D^2PAK
MBR2515L	25	15	0.42	15	TO–220
MBRB3030CTL	30	30	0.58	5	D^2PAK
MBR4015LWT	40	15	0.42	5	TO–247
MBR5025L	50	25	0.58	0.5	TO–218
MBRP20030CTL	200	30	0.39	5	POWERTAP II
MBRP60035CTL	600	35	0.50	10	POWERTAP II

Table 2. MEGAHERTZ Rectifiers

MEGAHERTZ Series — This group of ultrafast rectifiers is designed to provide improved efficiency in very high frequency switching power supplies and for use in power factor correction circuits.

			Maximum		
Device	I_O Amps	V_{RRM} (Volts)	V_F @ Rated I_O and Temp. (Volts)	I_R @ Rated V_{RRM} (mAmps)	t_{rr} (Nanosecond)
MURH840CT/MURHB840CT	8	400	1.7	0.01	28
MURH860CT	8	600	2.0	0.01	28

Table 3. SCANSWITCH Rectifiers

These ultrafast rectifiers are designed for improved performance in very high resolution monitors and work stations where forward recovery time (t_{fr}) and high voltage (1200–1500 volts) are primary considerations.

			Maximum		
Device	I_O Amps	V_{RRM} (Volts)	t_{fr} (Nanoseconds)	t_{rr} (Nanoseconds)	V_{RFM} (6) (Volts)
MUR880E	8	800	—	75	—
MUR10120E	10	1200	175	175	14
MUR10150E	10	1500	175	175	16

Table 4. Automotive Transient Suppressors

Automotive transient suppressors are designed for protection against over–voltage conditions in the auto electrical system including the "LOAD DUMP" phenomenon that occurs when the battery open circuits while the car is running.

Device	I_O Amps	V_{RRM} (Volts)	$V_{(BR)}$ (Volts)	I_{RSM}(7) (Amps)	T (°C)
MR2535L/MR2535S	35	20	24–32	110	175

(6) V_{RFM} = Maximum Transient Overshoot Voltage.
(7) Time constant = 10 ms, Duty Cycle ≤ 1%, T_C = 25°C.

Devices listed in bold, italic are Motorola preferred devices.

SWITCHMODE™ Rectifiers

Schottky power rectifiers with the high speed and low forward voltage drop characteristic of Schottky's metal/silicon junctions are produced with ruggedness and temperature performance comparable to silicon–junction rectifiers. Ideal for use in low–voltage, high–frequency power supplies, and as very fast clamping diodes, these devices feature switching times less than 10 ns, and are offered in current ranges from 0.5 to 600 amperes, and reverse voltages to 200 volts.

In some current ranges, devices are available with junction temperature specifications of 125°C, 150°C and 175°C. Devices with higher T_J ratings can have significantly lower leakage currents, but higher forward–voltage specifications. These parameter tradeoffs should be considered when selecting devices for applications that can be satisfied by more than one device type number.

All devices are connected cathode–to–case or cathode–to–heatsink, where applicable. Contact your Motorola representative for more information.

There are many other standard features in Motorola Schottky rectifiers that give added performance and reliability.

1. GUARDRINGS were pioneered by Motorola and are included in all Schottky die for reverse voltage stress protection from high rates of dv/dt to virtually eliminate the need for snubber networks. The guardring also operates like a zener and avalanches when subjected to voltage transients.
2. MOLYBDENUM DISCS on both sides of the die minimize fatigue from power cycling in all metal products. Plastic encapsulated devices have a special solder formulation for the same purpose.
3. QUALITY CONTROL monitors all critical fabrication operations and performs selected stress tests to assure constant processes. Motorola's commitment to six sigma has provided significant quality improvement.

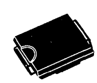
Case 425
SOD–123

Cathode = Band

Case 403B–01
SMA

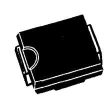
Cathode = Notch

Case 403A
SMB



Cathode = Notch

Case 403
SMC



Cathode = Notch

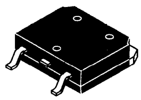
Table 5. Surface Mount Schottky Rectifiers

V_{RRM} (Volts)	I_O(1) (Amperes)	I_O Rating Condition	Device	Max V_F @ i_F T_C = 25°C (Volts)	I_{FSM} (Amperes)	T_J Max (°C)	Package
20	0.5	T_L = 105°C	***MBR0520LT1*** ★	0.310 @ 0.1 A 0.385 @ 0.5 A	5	125	SOD–123
30	0.5	T_L = 105°C	***MBR0530T1*** ★	0.375 @ 0.1 A 0.430 @ 0.5 A	5	125	SOD–123
40	0.5	T_L = 110°C	***MBR0540T1*** ★	0.53 @ 0.5 A	20	150	SOD–123
30	1	T_L = 100°C	***MBRA130LT3*** ★	0.395 @ 1.0 A	—	125	SMA
40	1	T_L = 100°C	***MBRA140T3*** ★	0.55 @ 1.0 A	—	125	SMA
30	1	T_L = 120°C	***MBRS130LT3***	0.395 @ 1.0 A	40	125	SMB
40	1	T_L = 115°C	***MBRS140T3***	0.6 @ 1.0 A	40	125	SMB
100	1	T_L = 120°C	***MBRS1100T3***	0.75 @ 1.0 A	40	150	SMB
40	3	T_L = 100°C	***MBRS340T3***	0.525 @ 3.0 A	80	125	SMC
60	3	T_L = 100°C	***MBRS360T3*** ★	0.74 @ 3.0 A	80	125	SMC

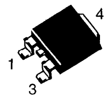
(1) I_O is total device current capability.
★ New Product

Devices listed in bold, italic are Motorola preferred devices.

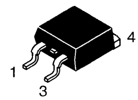
Case 433–01
D^3PAK



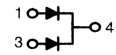
Case 369A
DPAK
Style 3



Case 418B
D^2PAK
Style 3



"CT" Suffix:



Non–"CT" Suffix:

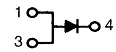


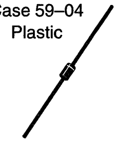
Table 5. Surface Mount Schottky Rectifiers (continued)

V_{RRM} (Volts)	I_O(1) (Amperes)	I_O Rating Condition	Device	Max V_F @ i_F $T_C = 25°C$ (Volts)	I_{FSM} (Amperes)	T_J Max (°C)	Package
40	3	$T_C = 125°C$	***MBRD340***	0.60 @ 3.0 A	75	150	DPAK
60	3	$T_C = 125°C$	***MBRD360***	0.60 @ 3.0 A	75	150	DPAK
40	6	$T_C = 130°C$	***MBRD640CT***	0.70 @ 3.0 A	75	150	DPAK
60	6	$T_C = 130°C$	***MBRD660CT***	0.70 @ 3.0 A	75	150	DPAK
35	8	$T_C = 100°C$	***MBRD835L*** ★	0.40 @ 3.0 A 0.51 @ 8.0 A	100	125	DPAK
35	10	$T_C = 90°C$	***MBRD1035CTL***★	0.49 @ 10 A	100	125	DPAK
45	15	$T_C = 105°C$	***MBRB1545CT***	0.84 @ 15 A	150	150	D^2PAK
60	20	$T_C = 110°C$	***MBRB2060CT***	0.95 @ 20 A	150	150	D^2PAK
100	20	$T_C = 110°C$	***MBRB20100CT***	0.85 @ 10 A 0.95 @ 20 A	150	150	D^2PAK
200	20	$T_C = 125°C$	***MBRB20200CT***★	1.0 @ 20 A	150	150	D^2PAK
15	25	$T_C = 90°C$	***MBRB2515L***★	0.45 @ 25 A	150	100	D^2PAK
35	25	$T_C = 110°C$	***MBRB2535CTL***	0.47 @ 12.5 A 0.55 @ 25 A	150	125	D^2PAK
45	25	$T_C = 130°C$	***MBRB2545CT***	0.82 @ 30 A	150	150	D^2PAK
30	30	$T_C = 115°C$	***MBRB3030CT***★	0.51 @ 15 A 0.62 @ 30 A	300	150	D^2PAK
30	30	$T_C = 95°C$	***MBRB3030CTL***★	0.45 @ 15 A 0.51 @ 30 A	150	125	D^2PAK
30	40	$T_C = 110°C$	***MBRB4030***★	0.46 @ 20 A 0.55 @ 40 A	300	150	D^2PAK
30	70	$T_C = 90°C$	***MBRV7030CTL***★	0.5 @ 35 A 0.62 @ 70 A	500	150	D^3PAK

(1) I_O is total device current capability.
★ New Product

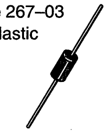
Devices listed in bold, italic are Motorola preferred devices.

Case 59–04
Plastic



Cathode = Polarity Band

Case 267–03
Plastic



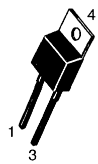
Cathode = Polarity Band

Table 6. Axial Lead Schottky Rectifiers

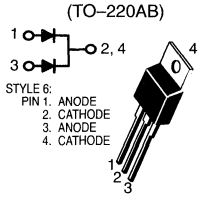
V_{RRM} (Volts)	I_O (Amperes)	I_O Rating Condition	Device	Max V_F @ i_F T_C = 25°C (Volts)	I_{FSM} (Amperes)	T_J Max (°C)	Case
20	1	T_A = 55°C $R_{\theta JA}$ = 80°C/W	***1N5817***	0.45 @ 1.0 A	25	125	59–04
30	1	T_A = 55°C $R_{\theta JA}$ = 80°C/W	***1N5818***	0.55 @ 1.0 A	25	125	59–04
40	1	T_A = 55°C $R_{\theta JA}$ = 80°C/W	***1N5819***	0.60 @ 1.0 A	25	125	59–04
60	1	T_A = 55°C $R_{\theta JA}$ = 80°C/W	***MBR160***	0.75 @ 1.0 A	25	150	59–04
100	1	T_A = 120°C $R_{\theta JA}$ = 50°C/W	***MBR1100***	0.79 @ 1.0 A	50	150	59–04
20	3	T_A = 76°C $R_{\theta JA}$ = 28°C/W	***1N5820***	0.457 @ 3.0 A	80	125	267–03
30	3	T_A = 71°C $R_{\theta JA}$ = 28°C/W	***1N5821***	0.500 @ 3.0 A	80	125	267–03
40	3	T_A = 61°C $R_{\theta JA}$ = 28°C/W	***1N5822***	0.525 @ 3.0 A	80	125	267–03
40	3	T_A = 65°C $R_{\theta JA}$ = 28°C/W	***MBR340***	0.600 @ 3.0 A	80	150	267–03
60	3	T_A = 65°C $R_{\theta JA}$ = 28°C/W	***MBR360***	0.740 @ 3.0 A	80	150	267–03
100	3	T_A = 100°C $R_{\theta JA}$ = 28°C/W	***MBR3100***	0.79 @ 3.0 A	150	150	267–03

Devices listed in bold, italic are Motorola preferred devices.

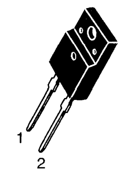
Case 221B
(TO–220AC)



Case 221A–06
(TO–220AB)



Case 221E



Case 221D

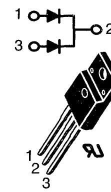


Table 7. TO–220 Type Schottky Rectifiers

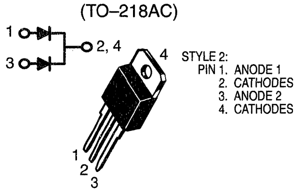
V_{RRM} (Volts)	I_O (Amperes)	I_O Rating Condition	Device	Max V_F @ i_F T_C = 25°C (Volts)	I_{FSM} (Amperes)	T_J Max (°C)	Case
45	15	T_C = 105°C	***MBR1545CT***	0.84 @ 15 A	150	150	221A–06
30	20	T_C = 137°C	***MBR2030CTL***★	0.52 @ 10 A 0.58 @ 20 A	150	150	221A–06
45	20	T_C = 135°C	***MBR2045CT***	0.84 @ 20 A	150	150	221A–06
60	20	T_C = 133°C	***MBR2060CT***	0.85 @ 10 A 0.95 @ 20 A	150	150	221A–06
100	20	T_C = 133°C	***MBR20100CT***	0.85 @ 10 A 0.95 @ 20 A	150	150	221A–06
200	20	T_C = 125°C	***MBR20200CT***	1.0 @ 20 A	150	150	221A–06
15	25	T_C = 90°C	***MBR2515L***★	0.45 @ 25 A	150	100	221A–06
35	25	T_C = 95°C	***MBR2535CTL***★	0.55 @ 25 A	150	125	221A–06
45	25	T_C = 130°C	***MBR2545CT***	0.82 @ 30 A	150	150	221A–06
45	30	T_C = 130°C	***MBR3045ST***★	0.76 @ 30 A	150	150	221A–06
45	7.5	T_C = 105°C	***MBR745***	0.84 @ 15 A	150	150	221B
45	10	T_C = 135°C	***MBR1045***	0.84 @ 20 A	150	150	221B
60	10	T_C = 133°C	***MBR1060***	0.80 @ 10 A	150	150	221B
100	10	T_C = 133°C	***MBR10100***	0.80 @ 10 A	150	150	221B
45	16	T_C = 125°C	***MBR1645***	0.63 @ 16 A	150	150	221B
45	15	T_C = 105°C	UL ***MBRF1545CT***	0.84 @ 15 A	150	150	ISOLATED 221D
45	20	T_C = 135°C	UL ***MBRF2045CT***	0.84 @ 20 A	150	150	ISOLATED 221D
60	20	T_C = 133°C	UL ***MBRF2060CT***	0.95 @ 20 A	150	150	ISOLATED 221D
100	20	T_C = 133°C	UL ***MBRF20100CT***	0.95 @ 20 A	150	150	ISOLATED 221D
200	20	T_C = 125°C	UL ***MBRF20200CT***	1.0 @ 20 A	150	150	ISOLATED 221D
45	25	T_C = 125°C	UL ***MBRF2545CT***	0.82 @ 25 A	150	150	ISOLATED 221D
45	7.5	T_C = 105°C	***MBRF745***★	0.84 @ 15 A	150	150	ISOLATED 221E
45	10	T_C = 135°C	***MBRF1045***★	0.84 @ 20 A	150	150	ISOLATED 221E

UL Indicates UL Recognized — File #E69369

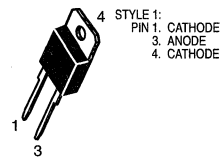
★ New Product

Devices listed in bold, italic are Motorola preferred devices.

Case 340D
(TO–218AC)



Case 340E
(TO–218)



Case 340F
(TO–247)

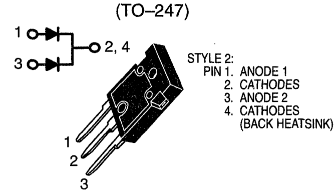


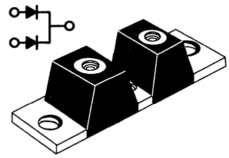
Table 8. TO–218 Types and TO–247 Schottky Rectifiers

V_{RRM} (Volts)	I_O (Amperes)	I_O Rating Condition	Device	Max V_F @ i_F T_C = 25°C (Volts)	I_{FSM} (Amperes)	T_J Max (°C)	Case
45	30	T_C = 105°C	***MBR3045PT***	0.76 @ 30 A	200	150	340D
45	40	T_C = 125°C	***MBR4045PT***	0.70 @ 20 A 0.80 @ 40 A	400	150	340D
45	60	T_C = 125°C	***MBR6045PT***★	0.62 @ 30 A 0.75 @ 60 A	500	150	340D
25	50	T_C = 125°C	***MBR5025L***★	0.54 @ 30 A 0.62 @ 50 A	300	150	340E
45	30	T_C = 105°C	***MBR3045WT***	0.76 @ 30 A	200	150	340F
15	40	T_C = 125°C	***MBR4015LWT***	0.42 @ 20 A 0.50 @ 40 A	400	150	340F
45	40	T_C = 125°C	***MBR4045WT***	0.70 @ 20 A 0.80 @ 40 A	400	150	340F
45	60	T_C = 125°C	***MBR6045WT***	0.62 @ 30 A 0.75 @ 60 A	500	150	340F
30	70	T_C = 135°C	***MBR7030WT***	0.55 @ 35 A 0.72 @ 70 A	400	150	340F

★ New Product

Devices listed in bold, italic are Motorola preferred devices.

Case 357C
POWERTAP™



Cathode = Mounting Plate
Anode = Terminal

Table 9. POWERTAP II

V_{RRM} (Volts)	I_O(1) (Amperes)	I_O Rating Condition	Device	Max V_F @ i_F T_C = 25°C (Volts)	I_{FSM} (Amperes)	T_J Max (°C)	Case
30	200	T_C = 125°C	***MBRP20030CTL*** ★	0.52 @ 100 A 0.60 @ 200 A	1500	150	357C
45	200	T_C = 125°C	***MBRP20045CT*** ★	0.78 @ 100 A	1500	175	357C
60	200	T_C = 125°C	***MBRP20060CT*** ★	0.800 @ 100 A	1500	175	357C
45	300	T_C = 120°C	***MBRP30045CT*** ★	0.70 @ 150 A 0.82 @ 300 A	2500	175	357C
60	300	T_C = 120°C	***MBRP30060CT*** ★	0.79 @ 150 A 0.89 @ 300 A	2500	175	357C
35	600	T_C = 100°C	***MBRP60035CTL*** ★	0.57 @ 300 A	4000	150	357C

(1) I_O is total device current capability.

All POWERTAP devices were converted to the new, more rugged, POWERTAP II configuration beginning January 1994. Contact your Motorola representative for more details.

★ New Product

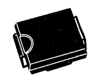
Devices listed in bold, italic are Motorola preferred devices.

Ultrafast Rectifiers

Case 403A
SMB

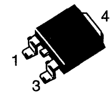
Cathode = Notch

Case 403
SMC

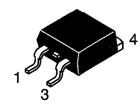


Cathode = Notch

Case 369A
DPAK
Style 3



Case 418B
D^2PAK
Style 3



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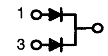


Non–"CT" Suffix:

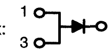
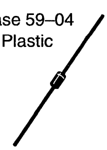


Table 10. Surface Mount Ultrafast Rectifiers

V_{RRM} (Volts)	I_O(1) (Amperes)	I_O Rating Condition	Device	Max t_{rr} (ns)	Max V_F @ i_F T_C = 25°C (Volts)	I_{FSM} (Amperes)	T_J Max (°C)	Package
200	1	T_L = 155°C	***MURS120T3***	35	0.875 @ 1.0 A	40	175	SMB
600	1	T_L = 150°C	***MURS160T3***	75	1.25 @ 1.0 A	35	175	SMB
200	3	T_L = 140°C	***MURS320T3***	35	0.875 @ 3.0 A	75	175	SMC
600	3	T_L = 130°C	***MURS360T3***	75	1.25 @ 3.0 A	75	175	SMC
200	3	T_L = 158°C	***MURD320***	35	0.95 @ 3.0 A	75	175	DPAK
200	6	T_L = 145°C	***MURD620CT***	35	1.0 @ 3.0 A	63	175	DPAK
400	8	T_L = 120°C	***MURHB840CT***★	28	2.2 @ 4.0 A	100	175	D^2PAK
200	16	T_L = 150°C	***MURB1620CT***	35	0.975 @ 8.0 A	100	175	D^2PAK
600	16	T_L = 150°C	***MURB1660CT***	60	1.5 @ 8.0 A	100	175	D^2PAK

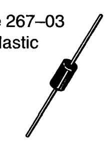
(1) I_O is total device current capability.
★ New Product

Case 59–04
Plastic



Cathode = Polarity Band

Case 267–03
Plastic



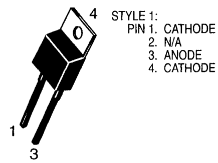
Cathode = Polarity Band

Table 11. Axial Lead Ultrafast Rectifiers

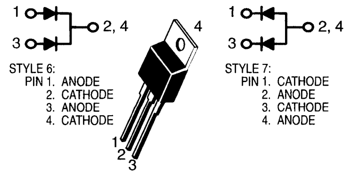
V_{RRM} (Volts)	I_O (Amperes)	I_O Rating Condition	Device	Max t_{rr} (ns)	Max V_F @ i_F T_C = 25°C (Volts)	I_{FSM} (Amperes)	T_J Max (°C)	Case
200	1	T_A = 130°C $R_{\theta JA}$ = 50°C/W	***MUR120***	25	0.875 @ 1.0 A	35	175	59–04
600	1	T_A = 120°C $R_{\theta JA}$ = 50°C/W	***MUR160***	50	1.25 @ 1.0 A	35	175	59–04
1000	1	T_A = 95°C $R_{\theta JA}$ = 50°C/W	***MUR1100E***	75	1.75 @ 1.0 A	35	175	59–04
200	4	T_A = 80°C $R_{\theta JA}$ = 28°C/W	***MUR420***	25	0.875 @ 3.0 A	125	175	267–03
600	4	T_A = 40°C $R_{\theta JA}$ = 28°C/W	***MUR460***	50	1.25 @ 3.0 A	70	175	267–03
1000	4	T_A = 35°C $R_{\theta JA}$ = 28°C/W	***MUR4100E***	75	1.75 @ 3.0 A	70	175	267–03

Devices listed in bold, italic are Motorola preferred devices.

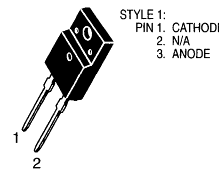
Case 221B
(TO–220AC)



Case 221A–06
(TO–220AB)



Case 221E



Case 221D

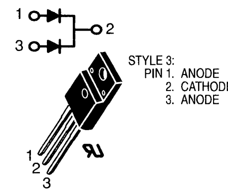


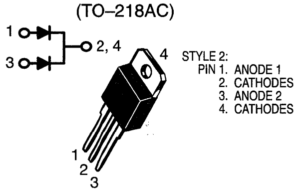
Table 12. TO–220 Type Ultrafast Rectifiers

V_{RRM} (Volts)	I_O (Amperes)	I_O Rating Condition	Device	Max t_{rr} (ns)	Max V_F @ i_F T_C = 25°C (Volts)	I_{FSM} (Amperes)	T_J Max (°C)	Case
200	6	T_C = 130°C	***MUR620CT***	35	0.975 @ 3.0 A	75	175	221A–06
400	8	T_C = 120°C	***MURH840CT***	28	2.0 @ 4.0 A	100	175	221A–06
600	8	T_C = 120°C	***MURH860CT***	35	2.8 @ 4.0 A	100	175	221A–06
200	16	T_C = 150°C	***MUR1620CT***	35	0.975 @ 8.0 A	100	175	221A–06
200	16	T_C = 160°C	***MUR1620CTR***	85	1.2 @ 8.0 A	100	175	221A–06
400	16	T_C = 150°C	***MUR1640CT***	60	1.30 @ 8.0 A	100	175	221A–06
600	16	T_C = 150°C	***MUR1660CT***	60	1.5 @ 8.0 A	100	175	221A–06
200	8	T_C = 150°C	***MUR820***	35	0.975 @ 8.0 A	100	175	221B
400	8	T_C = 150°C	***MUR840***★	50	1.30 @ 8.0 A	100	175	221B
600	8	T_C = 150°C	***MUR860***★	50	1.50 @ 8.0 A	100	175	221B
800	8	T_C = 175°C	***MUR880E***	75	1.80 @ 8.0 A	100	175	221B
1000	8	T_C = 150°C	***MUR8100E***	75	1.80 @ 8.0 A	100	175	221B
1200	10	T_C = 125°C	***MUR10120E***	175	2.2 @ 6.5 A	100	125	221B
1500	10	T_C = 125°C	***MUR10150E***	175	2.4 @ 6.5 A	100	125	221B
200	15	T_C = 150°C	***MUR1520***	35	1.05 @ 15 A	200	175	221B
400	15	T_C = 150°C	***MUR1540***	60	1.25 @ 15 A	150	175	221B
600	15	T_C = 145°C	***MUR1560***	60	1.50 @ 15 A	150	175	221B
200	8	T_C = 150°C	***MURF820***★	25	0.975 @ 8.0 A	100	150	ISOLATED 221E
200	16	T_C = 150°C	UL ***MURF1620CT***★	25	0.975 @ 8.0 A	100	150	ISOLATED 221D
600	16	T_C = 150°C	UL ***MURF1660CT***★	50	1.50 @ 8.0 A	100	150	ISOLATED 221D

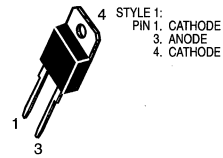
UL Indicates UL Recognized — File #E69369
★ New Product

Devices listed in bold, italic are Motorola preferred devices.

Case 340D
(TO–218AC)



Case 340E
(TO–218)



Case 340F
(TO–247)

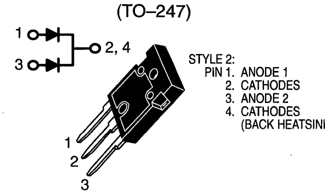
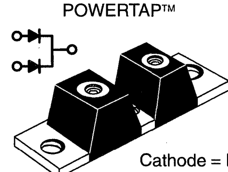


Table 13. TO–218 Types and TO–247 Ultrafast Rectifiers

V_{RRM} (Volts)	I_O (Amperes)	I_O Rating Condition	Device	Max t_{rr} (ns)	Max V_F @ i_F $T_C = 25°C$ (Volts)	I_{FSM} (Amperes)	T_J Max (°C)	Case
200	30	T_C = 145°C	***MUR3020WT***	35	1.05 @ 15 A	150	175	340F
400	30	T_C = 145°C	***MUR3040WT***	60	1.25 @ 15 A	150	175	340F
600	30	T_C = 145°C	***MUR3060WT***	60	1.70 @ 15 A	150	175	340F
200	30	T_C = 150°C	***MUR3020PT***	35	1.12 @ 15 A	200	175	340D
400	30	T_C = 150°C	***MUR3040PT***	60	1.12 @ 15 A	150	175	340D
600	30	T_C = 145°C	***MUR3060PT***	60	1.20 @ 15 A	150	175	340D
400	30	T_C = 70°C	***MUR3040***★	100	1.5 @ 30 A	300	175	340E
800	30	T_C = 70°C	***MUR3080***★	110	1.90 @ 30 A	300	175	340E
400	60	T_C = 70°C	***MUR6040***	100	1.50 @ 60 A	600	175	340E

★ New Product

Case 357C
POWERTAP™



Cathode = Mounting Plate
Anode = Terminal

Table 14. POWERTAP II

V_{RRM} (Volts)	I_O(1) (Amperes)	I_O Rating Condition	Device	Max t_{rr} (ns)	Max V_F @ i_F $T_C = 25°C$ (Volts)	I_{FSM} (Amperes)	T_J Max (°C)	Case
200	200	T_C = 130°C	***MURP20020CT***★	50	1.00 @ 100 A	800	175	357C
400	200	T_C = 100°C	***MURP20040CT***★	50	1.30 @ 100 A	800	175	357C

(1) I_O is total device current capability.

All POWERTAP devices were converted to the new, more rugged, POWERTAP II configuration beginning January 1994. Contact your Motorola representative for more details.

UL Indicates UL Recognized — File #E69369

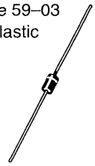
★ New Product

Devices listed in bold, italic are Motorola preferred devices.

Fast Recovery Rectifiers/General–Purpose Rectifiers

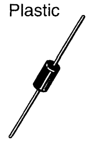
Axial lead Fast Recovery Rectifiers having maximum switching times of 200 ns and low cost general purpose rectifiers are listed in the table below.

Case 59–03
Plastic



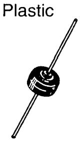
Cathode = Polarity Band

Case 267–03
Plastic



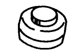
Cathode = Polarity Band

Case 194–04
Plastic



Cathode indicated by diode symbol

Case 193–04
Plastic(10)



Cathode = Polarity Band

Case 403B–01
SMA

Case 421A–01

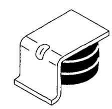


Table 15. Fast Recovery Rectifiers/General Purpose Rectifiers

V_{RRM} (Volts)	I_O (Amperes)	I_O Rating Condition	Device	Max V_F @ i_F T_J = 25°C (Volts)	Max t_{rr} (ns)	I_{FSM} (Amperes)	T_J Max (°C)	Case
200	1	T_C = 100°C	***MRA4003***	1.1 @ 1.0 A	—	30	150	
400	1	T_C = 100°C	***MRA4004***	1.1 @ 1.0 A	—	30	150	
600	1	T_C =100°C	***MRA4005***	1.1 @ 1.0 A	—	30	150	403B–01
800	1	T_C = 100°C	***MRA4006***	1.1 @ 1.0 A	—	30	150	
1000	1	T_C = 100°C	***MRA4007***	1.1 @ 1.0 A	—	30	150	
400	1	T_A = 75°C	***1N4004***	1.1 @ 1.0 A	—	30	150	
1000	1	T_A = 75°C	***1N4007***	1.1 @ 1.0 A	—	30	150	
200	1	T_A = 75°C	***1N4935***	1.2 @ 3.14 A T_J = 125°C	200	30	150	59–03(9)
600	1	T_A = 75°C	***1N4937***	1.2 @ 3.14 A T_J = 125°C	200	30	150	
400	3	T_L = 105°C	***1N5404***	1.2 @ 9.4 A	—	200	150	
600	3	T_L = 105°C	***1N5406***	1.2 @ 9.4 A	—	200	150	267–03
200	3	T_A = 80°C(10)	***MR852***	1.25 @ 3.0 A	200	100	150	
600	3	T_A = 80°C(10)	***MR856***	1.25 @ 3.0 A	200	100	150	
400	6	T_A = 60°C $R_{\theta JA}$ = 25°C/W	***MR754***	1.25 @ 100 A	—	400	175	194–04
1000	6	T_A = 60°C $R_{\theta JA}$ = 25°C/W	***MR760***	1.25 @ 100 A	—	400	175	
400	25	T_C = 150°C	***MR2504***	1.18 @ 78.5 A	—	400	175	193–04
1000	25	T_C = 150°C	***MR2510***	1.18 @ 78.5 A	—	400	175	
20	35	T_C = 150°C	***MR2535S***	1.1 @ 100 A	—	400	175	421A–01
20	35	T_C = 150°C	***MR2535L***(11)	1.1 @ 100 A	—	400	175	194–04
200	1	T_L = 100°C	***MRA4935T3***	1.1 @ 1.0 A	200	30	150	
400	1	T_L = 100°C	***MRA4936T3***	1.1 @ 1.0 A	200	30	150	403B–01
600	1	T_L = 100°C	***MRA4937T3***	1.1 @ 1.0 A	200	30	150	

(2) V_{RRM} unless noted
(3) V_{RRM}, T_J = 100°C unless noted
(9) Package Size: 0.120" max diameter by 0.260" length.
(10) Must be derated for reverse power dissipation. See data sheet.
(11) Overvoltage Transient Suppressor: 24–32 volts avalanche voltage.

Devices listed in bold, italic are Motorola preferred devices.

GaAs Rectifiers Power Manager™

For use in state–of–the–art high power density DC–DC converters and high frequency power supplies, GaAs power rectifiers have several unique characteristics that make them superior to Si–based devices. In particular, GaAs devices are acclaimed for their hyperfast and soft reverse recovery characteristics with low stored charge. Also, the device parameters are stable over a wide temperature range.

GaAs devices as drop–in replacements for Si may eliminate the need for a snubber network or allow for a significant reduction in network size. Performance improvements can therefore be achieved while reducing circuit size (increasing power density), decreasing EMI, and enhancing overall system efficiency.

Table 16. TO–220 and D²PAK GaAs Rectifiers Power Manager™

V_{RRM} (Volts)	I_{DC}(12)	I_{DC} Rating Condition	Device	Max V_F @ 10 A T_C = 25°C (Volts)	Max t_{rr} (ns)	Case
180	10	T_C = 110°C	***MGR1018★***	1.4	15	221A–06
180	10	T_C = 110°C	***MGRB1018★***	1.4	15	418B
180	20	T_C = 130°C	***MGR2018CT★***	1.4	15	221A–06
180	20	T_C = 130°C	***MGRB2018CT★***	1.4	15	418B
250	20	T_C = 95°C	***MGR2025CT★***	2.2	15	221A–06
250	20	T_C = 95°C	***MGRB2025CT★***	2.2	15	418B

(12) I_{DC} is total device current capability.
★ New Product
Case 418B available in reel of 800 "T4".

Devices listed in bold, italic are Motorola preferred devices.

Thyristors and Triggers

In Brief . . .

Motorola's broad line of Thyristors includes. . . .

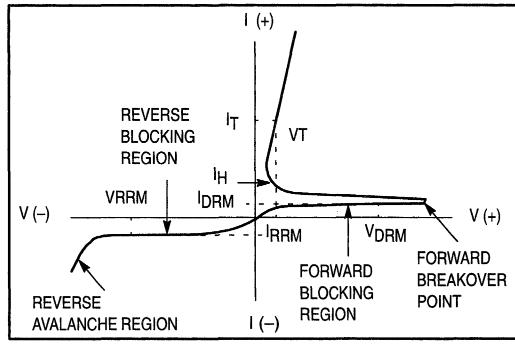
- A full line of TRIACs and SCRs covering a forward current range from 0.5 to 55 amperes and blocking voltages from 15 to 800 volts.
- Plastic package for lowest cost which includes the fully insulated plastic Case 221C (TO–220 Isolated).
- An extensive line of trigger devices that includes SIDACs, PUTs and SBS.

Then there are the special applications devices for Ignition circuits and Crowbar applications. Also included are isolated packaged devices for appliances and surface mount packages for surface mounting in space–saving requirements.

Finally, there is the continued Motorola investment in discrete–product R & D producing new capabilities such as transient SIDACs for use in circuits sensitive to high voltage transients.

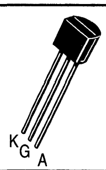
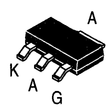
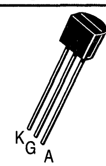
Page

SCRs



Silicon Controlled Rectifiers

Table 1. SCRs — General Purpose Plastic Packages
0.8 to 55 Amperes RMS, 25 to 800 Volts

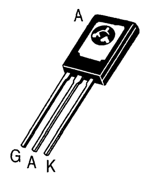
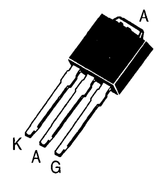
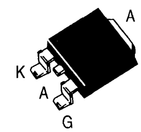
On–State (RMS) Current			V_{DRM} V_{RRM} (Volts)
0.8 AMP		**1.5 AMPS**	
T_C = 58°C	**T_C = 80°C**	**T_C = 50°C**	
			
Sensitive Gate			
Case 29–04 TO–226AA (TO–92) Style 10	**Case 318E SOT–223 STYLE 10**	**Case 29–04 TO–226AA (TO–92) Style 10**	
			25
			50
			100
	MCR08BT1		**200**
MCR100–6	***MCR08DT1***	***MCR22–6***	**400**
			500
MCR100–8	***MCR08MT1***	***MCR22–8***	**600**
Maximum Electrical Characteristics			
10	10	15 150(3)	**I_{TSM} (Amps) 60 Hz**
0.2			**I_{GT} (mA)**
0.8			**V_{GT} (V)**
–65 to +110	–40 to +110	–40 to +125	**T_J Operating Range (°C)**

(3) Exponential decay 2 μs wide at 5 time constants, f = 12 Hz.

Devices listed in bold, italic are Motorola preferred devices.

SCRs (continued)

Table 1. SCRs — General Purpose Plastic Packages (continued)

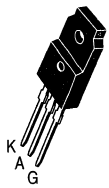
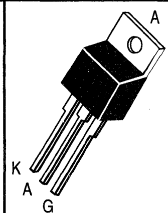
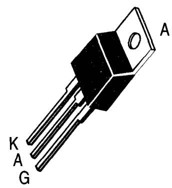
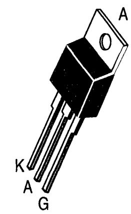
	On–State (RMS) Current			
	4 AMPS			
	T_C = 93°C	**T_C = 30°C**		
				
	Sensitive Gate			**Surface Mount**
V_{DRM} V_{RRM} (Volts)	**Case 77 TO–225AA (TO–126) Style 2**		**Case 369 Style 4**	**Case 369A Style 4**
50	***MCR106–2*** ***2N6237***	***C106F***		
100	MCR106–3 ***2N6238***	***C106A***		
200	***MCR106–4*** ***2N6239***	***C106B***		
400	***MCR106–6*** ***2N6240***	***C106D***	MCR716–1	MCR716
600	***MCR106–8*** ***2N6241***	***C106M***	MCR718–1	MCR718
800				
Maximum Electrical Characteristics				
I_{TSM} (Amps) 60 Hz	25	20	25	
I_{GT} (mA)	0.2		0.075	
V_{GT} (V)	1	0.8	1	
T_J Operating Range (°C)	−40 to +110			

UL Indicates UL Recognized — File #E69369

Devices listed in bold, italic are Motorola preferred devices.

SCRs (continued)

Table 1. SCRs — General Purpose Plastic Packages (continued)

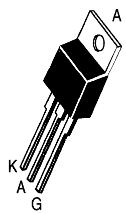
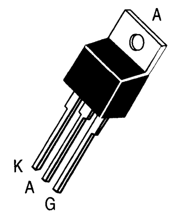
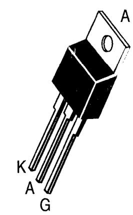
On–State (RMS) Current					
8 AMPS				10 AMPS	
T_C = 70°C	T_C = 83°C	T_C = 80°C		T_C = 75°C	
		 High Performance			
Isolated ꭐ	**Sensitive Gate**		**Sensitive Gate**		
Case 221C–02 Style 2	**Case 221A–04 TO–220AB Style 3**	**Case 221A–06 TO–220AB Style 3**		**Case 221A–04 TO–220AB Style 3**	**V_{DRM} V_{RRM} (Volts)**
	MCR72–2				**50**
	MCR72–3			MCR310–3	**100**
MCR218–4FP	MCR72–4			MCR310–4	**200**
MCR218–6FP	MCR72–6	***MCR8D***	***MCR8SD***	MCR310–6	**400**
MCR218–8FP	MCR72–8	***MCR8M***	***MCR8SM***	MCR310–8	**600**
MCR218–10FP	MCR72–10	***MCR8N***	***MCR8SN***	MCR310–10	**800**
Maximum Electrical Characteristics					
80	100	80		100	**I_{TSM} (Amps) 60 Hz**
25	0.2	15	0.2		**I_{GT} (mA)**
1.5		1		1.5	**V_{GT} (V)**
		Min. 50	**Min.** 2		**DV/DT V/µsec**
−40 to +125	−40 to +110	−40 to +125	−40 to +110		**T_J Operating Range (°C)**

ꭐ Indicates UL Recognized — File #E69369

Devices listed in bold, italic are Motorola preferred devices.

SCRs (continued)

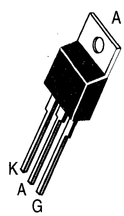
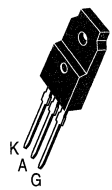
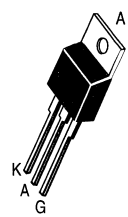
Table 1. SCRs — General Purpose Plastic Packages (continued)

V_{DRM} V_{RRM} (Volts)	On–State (RMS) Current				
	10 AMPS	**12 AMPS**	**16 AMPS**	**25 AMPS**	
	T_C = 75°C	**T_C = 80°C**			**T_C = 85°C**
					
	Sensitive Gate	**High Performance**			
	Case 221A–04 TO–220AB Style 3	**Case 221A–06 TO–220AB Style 3**			**Case 221A–04 TO–220AB Style 3**
50					2N6504
100					2N6505
200					2N6506
400	MCR12LD	***MCR12D***	***MCR16D***	***MCR25D***	2N6507
600	MCR12LM	***MCR12M***	***MCR16M***	***MCR25M***	2N6508
800	MCR12LN	***MCR12N***	***MCR16N***	***MCR25N***	2N6509
Maximum Electrical Characteristics					
I_{TSM} (Amps) 60 Hz	100		150	300	
I_{GT} (mA)	8	20		30	40
V_{GT} (V)	1.5	2.2	1.7	1	1.5
DV/DT V/µsec	**Min.** 50	**Min.** 50	**Min.** 50	**Min.** 50	
T_J Operating Range (°C)	−40 to +100	−40 to +125			

Devices listed in bold, italic are Motorola preferred devices.

SCRs (continued)

Table 1. SCRs — General Purpose Plastic Packages (continued)

On–State (RMS) Current				
25 AMPS		**40 AMPS**	**55 AMPS**	
T_C = 85°C		**T_C = 80°C**	**T_C = 70°C**	
	 **Isolated ®**			
Case 221A–04 TO–220AB Style 3	**Case 221C–02 Style 2**	**Case 221A–04 TO–220AB Style 3**		**V_{DRM} V_{RRM} (Volts)**
MCR69–2	MCR225–2FP			**50**
MCR69–3				**100**
	MCR225–4FP	***MCR264–4***	***MCR265–4***	**200**
MCR69–6	MCR225–6FP	***MCR264–6***	***MCR265–6***	**400**
	MCR225–8FP	***MCR264–8***	***MCR265–8***	**600**
	MCR225–10FP	***MCR264–10***	***MCR265–10***	**800**
Maximum Electrical Characteristics				
750(2)	300	400	550	**I_{TSM} (Amps) 60 Hz**
30	40	50		**I_{GT} (mA)**
1.5				**V_{GT} (V)**
−40 to +125				**T_J Operating Range (°C)**

(2) Peak capacitor discharge current for t_W = 1 ms. t_W is defined as five time constants of an exponentially decaying current pulse (crowbar applications).

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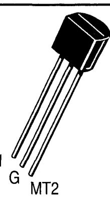
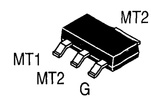
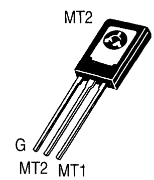
Devices listed in bold, italic are Motorola preferred devices.

TRIACs

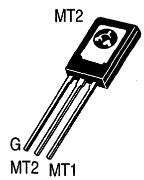
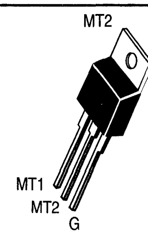
Table 2. TRIACs — General Purpose Plastic Packages
0.6 to 40 Amperes, 200 to 800 Volts

	On–State (RMS) Current			
	0.6 AMP		**0.8 AMPS**	**2.5 AMPS**
	T_C = 50°C		T_C = 80°C	T_C = 70°C
				
	Sensitive Gate			
V_{DRM} (Volts)	**Case 29–04 TO–226AA (TO–92) Style 12**		**Case 318E Style 11 SOT–223**	**Case 77 TO–225AA (TO–126) Style 5**
200			***MAC08BT1***	***T2322B***
400	***MAC97–6***	***MAC97A6***	***MAC08DT1***	***T2322D***
600	***MAC97–8***	***MAC97A8***	***MAC08MT1***	***T2322M***
Maximum Electrical Characteristics				
I_{TSM} (Amps)	8		10	25
I_{GT} @ 25°C (mA)				
MT2(+)G(+)	10	5	10	10
MT2(+)G(–)	10	5	10	10
MT2(–)G(–)	10	5	10	10
MT2(–)G(+)	10	7	10	10
V_{GT} @ 25°C (V)			0.8	
MT2(+)G(+)	2		2	2.2
MT2(+)G(–)	2		2	2.2
MT2(–)G(–)	2		2	2.2
MT2(–)G(+)	2.5		2	2.2
T_J Operating Range (°C)	–40 to +110			

Devices listed in bold, italic are Motorola preferred devices.

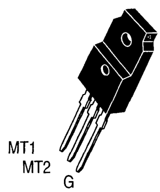
TRIACs (continued)

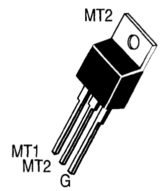
Table 2. TRIACs (continued)

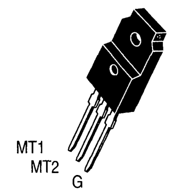
On–State (RMS) Current					
2.5 AMPS	**4 AMPS**			**6 AMPS**	
T_C = 70°C	**T_C = 85°C**			**T_C = 80°C**	
		**Sensitive Gate**			
Case 77 TO–225AA (TO–126) Style 5				**Case 221A–04 TO–220AB Style 4**	**V_{DRM} (Volts)**
T2323B	***2N6071***	***2N6071A***	***2N6071B***	T2500B	**200**
T2323D	***2N6073***	***2N6073A***	***2N6073B***	T2500D	**400**
T2323M	***2N6075***	***2N6075A***	***2N6075B***	T2500M	**600**
				T2500N	**800**
Maximum Electrical Characteristics					
25	30			60	**I_{TSM} (Amps)**
25 40 25 40	30 — 30 —	5 5 5 10	3 3 3 5	25 60 25 60	**I_{GT} @ 25°C (mA) MT2(+)G(+) MT2(+)G(–) MT2(–)G(–) MT2(–)G(+)**
2.2 2.2 2.2 2.2	@ –40°C 2.5 — 2.5 —	@ –40°C 2.5 2.5 2.5 2.5		2.5 2.5 2.5 2.5	**V_{GT} @ 25°C (V) MT2(+)G(+) MT2(+)G(–) MT2(–)G(–) MT2(–)G(+)**
–40 to +110		–40 to +100			**T_J Operating Range (°C)**

Devices listed in bold, italic are Motorola preferred devices.

Table 2. TRIACs (continued)







	On-State (RMS) Current						
	6 AMPS	8 AMPS					
	T_C = 80°C	T_C = 80°C	T_C = 70°C		T_C = 80°C		
			Sensitive Gate				
	Isolated		High Performance				Isolated
V_{DRM} (Volts)	Case 221C–02 Style 3	Case 221A–04 TO–220AB Style 4	Case 221A–06 TO–220AB Style 4				Case 221C–02 Style 3
200	T2500BFP	MAC218A4					MAC218A4FP
400	T2500DFP	MAC218A6	***MAC8SD***		***MAC8D***	***MAC9D***	MAC218A6FP
600	T2500MFP	MAC218A8	***MAC8SM***		***MAC8M***	***MAC9M***	MAC218A8FP
800	T2500NFP	MAC218A10	***MAC8SN***		***MAC8N***	***MAC9N***	MAC218A10FP
Maximum Electrical Characteristics							
I_{TSM} (Amps)	100		70		80		100
I_{GT} @ 25°C (mA)			Min.	Max.			
MT2(+)G(+)	25	50	0.8	5.0	35	50	50
MT2(+)G(–)	60	50	0.8	5.0	35	50	50
MT2(–)G(–)	25	50	0.8	5.0	35	50	50
MT2(–)G(+)	60	75(1)	—	—	—	—	75(1)
V_{GT} @ 25°C (V)							
MT2(+)G(+)	2.5	2	0.45	1.5	1.5		2
MT2(+)G(–)	2.5	2	0.45	1.5	1.5		2
MT2(–)G(–)	2.5	2	0.45	1.5	1.5		2
MT2(–)G(+)	2.5	2.5(1)	—	—	—		2.5(1)
			Min.		Min.	Min.	
DV/DT V/µsec			25		250	500	
T_J Operating Range (°C)	–40 to +100	–40 to +125	–40 to +110		–40 to +125		

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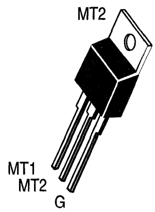
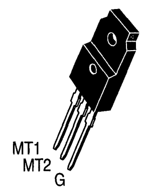
Devices listed in bold, italic are Motorola preferred devices.

TRIACs (continued)

Table 2. TRIACs (continued)

On–State (RMS) Current				
8 AMPS				
T_C = 80°C				
				
			Isolated UL	
		Sensitive Gate		
Case 221A–04 TO–220AB Style 4			**Case 221C–02 Style 3**	**V_{DRM} (Volts)**
2N6342 2N6346	T2800B	MAC228A4	MAC228A4FP	**200**
2N6343 2N6347	T2800D	MAC228A6	MAC228A6FP	**400**
2N6344 2N6348	T2800M	MAC228A8	MAC228A8FP	**600**
2N6345 2N6349		MAC228A10	MAC228A10FP	**800**
Maximum Electrical Characteristics				
100		80		**I_{TSM} (Amps)**
50 75(6) 50 75(6)	25 60 25 60	5 5 5 10(1)	5 5 5 10(1)	**I_{GT} @ 25°C (mA) MT2(+)G(+) MT2(+)G(–) MT2(–)G(–) MT2(–)G(+)**
2 2.5(6) 2.5 2.5(6)	2.5 2.5 2.5 2.5	2 2 2 2.5(1)		**V_{GT} @ 25°C (V) MT2(+)G(+) MT2(+)G(–) MT2(–)G(–) MT2(–)G(+)**
–40 to +125	–40 to +100	–40 to +110		**T_J Operating Range (°C)**

(6) Denotes 2N6346–49 Series only.

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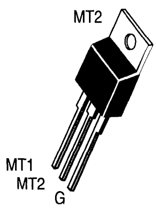
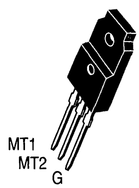
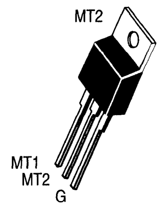
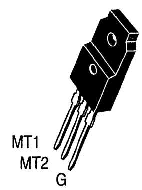
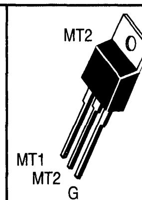
Table 2. TRIACs (continued)

	On–State (RMS) Current				
	10 AMPS			12 AMPS	
	T_C = 70°C		T_C = 75°C	T_C = 85°C	
		 Isolated ꓤL	 Sensitive Gate	 Isolated ꓤL	
V_{DRM} (Volts)	**Case 221A–04 TO–220AB Style 4**	**Case 221C–02 Style 3**	**Case 221A–04 TO–220AB Style 4**	**Case 221C–02 Style 3**	**Case 221A–04 TO–220AB Style 4**
200	MAC210A4	MAC210A4FP	MAC310A4	MAC212A4FP	MAC212A4
400	MAC210A6	MAC210A6FP	MAC310A6	MAC212A6FP	MAC212A6
600	MAC210A8	MAC210A8FP	MAC310A8	MAC212A8FP	MAC212A8
800	MAC210A10	MAC210A10FP	MAC310A10	MAC212A10FP	MAC212A10
	Maximum Electrical Characteristics				
I_{TSM} **(Amps)**	100				
I_{GT} **@ 25°C (mA)**					
MT2(+)G(+)	50		5	50	
MT2(+)G(–)	50		5	50	
MT2(–)G(–)	50		5	50	
MT2(–)G(+)	75(1)		10(1)	75(1)	
V_{GT} **@ 25°C (V)**					
MT2(+)G(+)	2				
MT2(+)G(–)	2				
MT2(–)G(–)	2				
MT2(–)G(+)	2.5(1)				
T_J **Operating Range (°C)**	–40 to +125				

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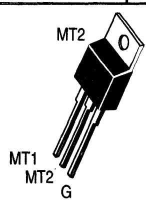
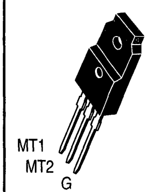
TRIACs (continued)

Table 2. TRIACs (continued)

On–State (RMS) Current							
12 AMPS		15 AMPS					
T_C = 80°C			T_C = 70°C	T_C = 90°C	T_C = 80°C	T_C = 90°C	
			Sensitive Gate				
	High Performance				High Performance	Isolated (UL)	
Case 221A–04 TO–220AB Style 4	Case 221A–06 TO–220AB Style 4			Case 221A–04 TO–220AB Style 4	Case 221A–06 TO–220AB Style 4	Case 221C–02 Style 3	V_{DRM} (Volts)
2N6346A				MAC15A4		MAC15A4FP	**200**
2N6347A	***MAC12D***	***MAC15D***	***MAC15SD***	MAC15A6	***MAC16D***	MAC15A6FP	**400**
2N6348A	***MAC12M***	***MAC15M***	***MAC15SM***	MAC15A8	***MAC16M***	MAC15A8FP	**600**
2N6349A	***MAC12N***	***MAC15N***	***MAC15SN***	MAC15A10	***MAC16N***	MAC15A10FP	**800**
Maximum Electrical Characteristics							
120		150	120	150			I_{TSM} (Amps)
			Min. / Max.				**I_{GT} @ 25°C (mA)**
50		35	0.8 / 5.0	50	50	50	**MT2(+)G(+)**
75		35	0.8 / 5.0	50	50	50	**MT2(+)G(–)**
50		35	0.8 / 5.0	50	50	50	**MT2(–)G(–)**
75		—	— / —	75(1)	—	75(1)	**MT2(–)G(+)**
							V_{GT} @ 25°C (V)
2	1.5		0.45 / 1.5	2	1.5	2	**MT2(+)G(+)**
2.5	1.5		0.45 / 1.5	2	1.5	2	**MT2(+)G(–)**
2	1.5		0.45 / 1.5	2	1.5	2	**MT2(–)G(–)**
2.5	—		— / —	2.5(1)	—	2.5(1)	**MT2(–)G(+)**
	Min.	Min.	Min.		Min.		
	250	250	25		500		**DV/DT V/μsec**
–40 to +125			–40 to +110	–40 to +125			**T_J Operating Range (°C)**





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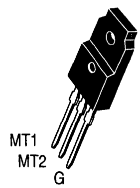
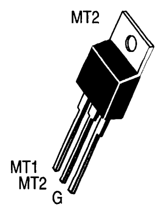
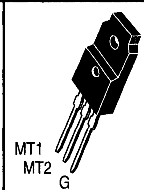
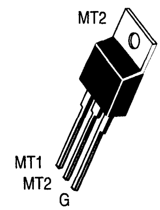
Devices listed in bold, italic are Motorola preferred devices.

TRIACs (continued)

Table 2. TRIACs (continued)

<table>
<tr><td rowspan="5">V_{DRM}
(Volts)</td><td colspan="6">On–State (RMS) Current</td></tr>
<tr><td colspan="2">20 AMPS</td><td colspan="3">25 AMPS</td><td>40 AMPS</td></tr>
<tr><td colspan="3">T_C = 75°C</td><td colspan="2">T_C = 80°C</td><td>T_C = 75°C</td></tr>
<tr><td>
Isolated UL</td><td colspan="2"></td><td>
Isolated UL</td><td colspan="2"></td></tr>
<tr><td>Case 221C–02
Style 3</td><td colspan="2">Case 221A–04
TO–220AB
Style 4</td><td>Case 221C–02
Style 3</td><td colspan="2">Case 221A–04
TO–220AB
Style 4</td></tr>
<tr><td>200</td><td>MAC320A4FP</td><td>MAC320A4</td><td>MAC321–4</td><td>MAC223A4FP</td><td>MAC223A4</td><td>MAC224A4</td></tr>
<tr><td>400</td><td>MAC320A6FP</td><td>MAC320A6</td><td>MAC321–6</td><td>MAC223A6FP</td><td>MAC223A6</td><td>MAC224A6</td></tr>
<tr><td>600</td><td>MAC320A8FP</td><td>MAC320A8</td><td>MAC321–8</td><td>MAC223A8FP</td><td>MAC223A8</td><td>MAC224A8</td></tr>
<tr><td>800</td><td>MAC320A10FP</td><td>MAC320A10</td><td>MAC321–10</td><td>MAC223A10FP</td><td>MAC223A10</td><td>MAC224A10</td></tr>
<tr><td colspan="7">Maximum Electrical Characteristics</td></tr>
<tr><td>I_{TSM} (Amps)</td><td colspan="3">150</td><td colspan="2">250</td><td>350</td></tr>
<tr><td>I_{GT} @ 25°C (mA)
MT2(+)G(+)
MT2(+)G(–)
MT2(–)G(–)
MT2(–)G(+)</td><td colspan="2">
50
50
50
75(1)</td><td>
100
100
100
—</td><td colspan="3">
50
50
50
75(1)</td></tr>
<tr><td>V_{GT} @ 25°C (V)
MT2(+)G(+)
MT2(+)G(–)
MT2(–)G(–)
MT2(–)G(+)</td><td colspan="2">
2
2
2
2.5(1)</td><td>
2
2
2
—</td><td colspan="3">
2
2
2
2.5(1)</td></tr>
<tr><td>T_J Operating
Range (°C)</td><td colspan="6">–40 to
+125</td></tr>
</table>

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Devices listed in bold, italic are Motorola preferred devices.

Thyristor Triggers

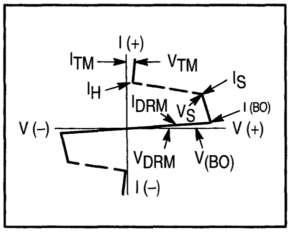


Table 3. SIDACs

High voltage trigger devices similar in operation to a Triac. Upon reaching the breakover voltage in either direction, the device switches to a low–voltage on–state.

Device Type	I_{TSM} Amps	V_{BO} Volts Min	V_{BO} Volts Max
Case 267–03/1			
MKP3V110	20	100	120
MKP3V120	20	110	130
MKP3V130	20	120	140
Case 59–04/1			
MKP1V120	4	110	130
MKP1V130	4	120	140

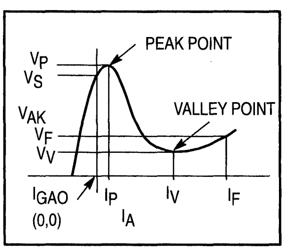


Table 4. Programmable Unijunction Transistor — PUT

Similar to UJTs, except that I_V, I_P and intrinsic standoff voltage are programmable (adjustable) by means of external voltage divider. This stabilizes circuit performance for variations in device parameters. General operating frequency range is from 0.01 Hz to 10 kHz, making them suitable for long–duration timer circuits.

Device Type	I_P R_G = 10 kΩ	I_P R_G = 1 MΩ	I_{GAO} @ 40 V nA Max	I_V R_G = 10 kΩ	I_V R_G = 1 MΩ
	μA Max	μA Max		μA Min	μA Max
Plastic TO–92 (Case 29–04/16)					
2N6027	5	2	10	70	50
2N6028	1	0.15	10	25	25

Devices listed in bold, italic are Motorola preferred devices.

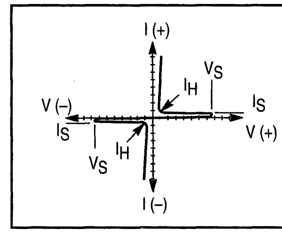


Table 5. Silicon Bidirectional Switch (SBS)

This versatile trigger device exhibits highly symmetrical bi-directional switching characteristics which can be modified by means of a gate lead. Requires a gate trigger current of only 250 μAdc for triggering.

Device Type	V_S Volts Min	V_S Volts Max	I_S μA Max	I_H mA Max
Plastic TO–92/TO–226AA (Case 29–04/12)				
MBS4991	6	10	500	1.5
MBS4992	7.5	9	120	0.5
MBS4993	7.5	9	250	0.75

Table 6. High Voltage Bidirectional TVS Devices Primary Protection

Transient Voltage Suppression (TVS) devices are break-over–triggered crowbar protectors. Turn–off occurs when the surge current falls below the holding current value.

Device Type	I_{TSM} Amps	V_{BR} Volts (Min)	V_{BO} Volts (Max)
Case 416A–01			
MMT10V275	100	200	275
MMT10V400	100	265	400

Thyristor Surge Suppressors–Secondary Protection

Package SO–8

MGSS150–1	30 AMP, 150 mA I_h, Programmable Bidirectional Surge Suppressor

Package 8 Pin PDIP

MGSS150–2	30 AMP, 150 mA I_h, Programmable Bidirectional Surge Suppressor

- Telecom Line Card Protection
- Dual Line Protection in a Single Package
- 2 Package Choices
- Bidirectional Capability
- 30 AMP Surge
- 150 mA I_h
- Low Gate Trigger Current

Optoelectronic Devices

In Brief . . .

Motorola's families of optoelectronic components encompass red and infrared GaAs emitters and silicon detectors that are well matched for a variety of applications.

Optoisolators

Motorola's "Global" 6–Pin Dual In–line Package (DIP) devices use infrared emitting diodes that are optically coupled to a wide selection of output (Transistor, Darlington, Triac, and Schmitt trigger) silicon detectors. These devices are guaranteed to provide at least 7500 volts of isolation between the input and output and are 100% VISO tested. The entire line of Motorola 6–pin DIP packages are recognized by all major safety regulatories including UL and VDE. This extensive line of regulatory approvals attest to their suitability for use under the most stringent conditions. Motorola also offers a line of SOIC–8 small outline, surface mount devices that are UL approved and ideally suited for high density applications.

POWER OPTO™ Isolators

The MOC2A40 and MOC2A60 series are the first members of the POWER OPTO™ Isolator family from Motorola. The MOC2A40/60 are 2 Amp @ 40°C/400 or 600 Vac[pk]/Zero–Crossing/Optically Coupled Triacs. These isolated AC output devices are ruggedized to survive the harsh operating environments inherent in Industrial Controller applications. Additionally, their thermally optimized SIP package profile allows for high density stacking on 0.200″ centers and can handle 2 Amps @ 40°C (Free–Air Rating) *without the need for heatsinks, thermal grease, etc.*

Page

Safety Regulatory Approvals for Motorola's "Global" Optoisolators

Motorola's entire line of 6–pin optoisolators are approved by all major safety regulatories.

Safety Standard Approvals for 6–Pin Optoisolators

GlobalOptoisolator™	VDE	UL	CSA	SETI	SEMKO	DEMKO	NEMKO	BABT
MOCXXXX	* (1)	*	*	*	*	*	*	*
SOCXXXX	* (1)	*	*	*	*	*	*	*
4NXXXXXX	* (1)	*	*	*	*	*	*	*
H1XXXXXX	* (1)	*	*	*	*	*	*	*
MCXXXXXX	* (1)	*	*	*	*	*	*	*
TIXXXXXX	* (1)	*	*	*	*	*	*	*
CNXXXXXX	* (1)	*	*	*	*	*	*	*

* = Approved

Regulatory Approval Certification Index

Regulatory Agency	Certificate File Number
VDE(0883)	41853 (expired 12/31/91)
VDE(0884)(1)	62054 (replaces VDE0883)
UL (isolation)	E54915
UL (flammability)	E–8436
CSA	CA93952
FIMKO	41990
SEMKO	9313138
DEMKO	Approved per SEMKO
NEMKO	A99177
BABT	CR/0117
AUSTEL	03 887 0711

Note: Motorola's 8–pin surface mount optocouplers are approved by UL only and have a guaranteed isolation voltage of 3000 Vac(rms).

All Motorola 6–pin optocouplers are 100% tested for isolation voltage and are guaranteed to 7500 Vac(peak).

UL Flammability Rating = 94VO (File number E–8436) for all optocouplers.

(1) VDE 0884 testing is an option; the suffix letter "V" must be added to the standard part number.

VDE Approved Optoisolators

VDE has approved Motorola's entire portfolio of 6–pin DIP optoisolators against their new components standard VDE 0884 which replaces VDE 0883. The VDE 0884 components standard requires additional electrical testing to a stringent isolation partial discharge test.

The VDE 0883 specification expired 12/31/91. Motorola optoisolators can now be ordered to comply with the VDE 0884 specification.

VDE approval is based on mechanical and electrical performance of the Motorola package, shown in Figure 3. This 6–Pin DIP package incorporates specially developed materials and assembly processes optimizing thermal and moisture stability while maintaining the high level of LED life and isolation voltage. All Motorola 6–pin DIP optoisolators are made in this package, and have these approvals.

VDE 0884 Component Standard (replaces VDE 0883)

Electrical ratings in this standard are:

Input–to–Output Voltage, 1 second

V_{Pr1} = 1.6 V_{IDRM}, Partial Discharge < 5 picocouloumbs, V_{Pr1} = 1280 V(pk)

Maximum operating peak voltage, V_{IDRM} = 800 V(pk)

Isolation resistance: V_{I-O} = 500 Vdc, 10^{11} Ω, T_A = 100°C.

Note: The isolation partial discharge test V_{Pr1}, is performed after the completion of the high voltage withstand (hipot) tests.

VDE 0883 Component Standard (expired 12/31/91)

Electrical ratings in this standard were:

Isolation withstand voltages:

3750 V_{RMS}, 1 min, T_A = 100°C

5300 Vdc, 1 min, T_A = 100°C

Isolation surge withstand voltage:

10 kV per IEC 65, 50 discharges

Isolation resistance:

10^{11} Ω, 500 Vdc, T_A = 100°C

NOTE: **VDE 0884/8.87 testing is an option**; the suffix letter "V" must be added to the standard part number. (See below.)

Standard thru hole — MOC3063V

0.4″ wide spaced leadform — MOC3063TV (to satisfy 8 mm spacing requirement)

Standard–profile surface mount — MOC3063SV

Tape and Reel for surface mount — MOC3063S/SR2V

Optoisolators, a block diagram of which is shown in Figure 1, are devices which contain at least one emitter, which is optically coupled to a photo–detector through some sort of an insulating medium. This arrangement permits the passage of information from one circuit, which contains the emitter, to the other circuit containing the detector.

Because this information is passed optically across an insulating gap, the transfer is one–way; that is, the detector cannot affect the input circuit. This is important because the emitter may be driven by a low voltage circuit utilizing an MPU or logic gates, while the output photo–detector may be part of a high voltage dc or even an ac load circuit. The optical isolation prevents interaction or even damage to the input circuit to be caused by the relatively hostile output circuit.

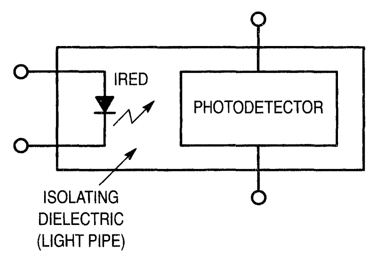


Figure 1. Block Diagram of Optoisolator

Various geometric designs have been used over the years for the internal light cavity between the emitter and detector. Motorola is the industry leader in isolation technology. All 6–pin optoisolators are guaranteed to meet or exceed 7500 Vac (pk) input–to–output isolation. See Figure 2.

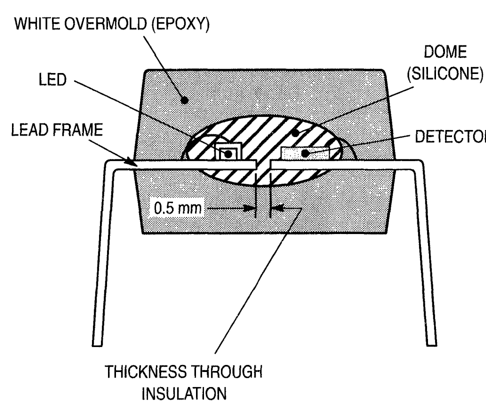


Figure 2. Geometric Design for Optoisolators

VDE Approved Optoisolators (continued)

Equipment Standards Compliance

With the approval of the Motorola package to these component standards, combined with its VDE approval ratings, a wide range of Equipment Standards are covered. The table below summarizes these Equipment Standard coverages.

Two levels of electrical interface, or insulation, are used: 1. Reinforced, or safe, insulation; 2. Basic insulation.

Reinforced Insulation (sometimes referred to as "safe" electrical isolation) is required in an optoisolator interfacing between a hazardous voltage circuit, like an ac line, and a **touchable s**afe **e**xtra **l**ow **v**oltage (SELV) circuit.

Basic Insulation is required in an optoisolator which interfaces between a hazardous voltage circuit and a **non–touchable, e**xtra **l**ow **v**oltage (ELV) circuit.

The 6–pin DIP optoisolators are suitable for both levels of electrical interface. The smaller SOIC–8 optoisolators comply with basic Insulation standards only.

Mechanical ratings are shown in the table below.

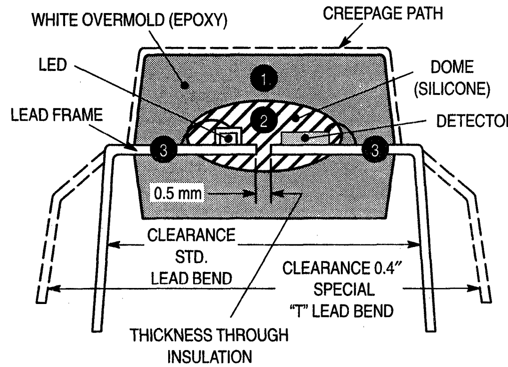


Figure 3. "DOME" Package

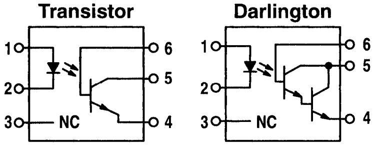
Examples for Safety Applications for Motorola VDE Approved Optoisolators

Standard (2)			Requirements for reinforced (double) or safe insulation for equipment with an operating voltage up to 250 Vrms (line voltage to ELV or SELV interfaces)				
VDE (5)	DIN IEC	Equipment	Creepage	Clearance (1)	Isolation Barrier	Dielectric Strength	Isolation Resistance
			[mm]	[mm]	[mm]	[kV RMS]	[Ω]
0806	950	Office Machines	8.0	8.0	0.5	3.75	7 x 10^6
0805	950	Data Processing	8.0	8.0	—	3.75	7 x 10^6
0804	—	Telecommunication	8.0	8.0	—	2.5	2 x 10^6
0860	65	Electrical Household	6.0	6.0	0.4	3.0 (10)*	4 x 10^6
0113	204	Industrial Controls	8.0	8.0	—	2.5	1 x 10^6
0160	—	Power Installations with Electronic Equipment	8.0	8.0	—	2.7	1 x 10^6
0832	—	Traffic Light Controls	8.0	8.0	—	2.5	4 x 10^6
0883	—	Alarm Systems	8.0	8.0	—	2.5	2 x 10^6
0831	—	Electrical Signal System for Railroads	8.0	8.0	—	2.0	2 x 10^6
0110	—	General Std. for Electrical Equipment	8.0	8.0	—	2.0	—
0883	—	Optoisolator Component Standard (obsolete 12/31/91)	8.5	8.3 (10) (1)	0.5	3.75 (10)*	10 x 10^{11}
0884(4)	—	Optoisolator Component Standard (replaces VDE0883)	>7.5	>7.5	0.5	—	10 x 10^{12}
			VDE Rating for Motorola 6–pin DIP Optoisolators				

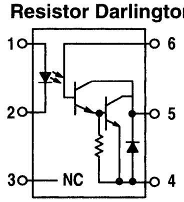
All Motorola 6–pin DIP Optoisolators meet or exceed the requirements of above listed VDE and DIN IEC Standards.
* Impulse discharge withstand voltage.
(1) To satisfy 8.0 mm creepage path on a PC board Motorola offers a special lead bend of 0.4 inch on all 6–pin dual in–line optoisolators. Order by attaching "T" to the end of the Motorola part number.
(2) VDE standards (translated into English language) and IEC standards can be ordered from the American National Standard Institute ANSI, 1430 Broadway, N.Y., N. Y. 10018, Sales Department, 212–642–4900.
(3) Creepage path distances are measured from lead to lead across the top, bottom and ends of the package body.
(4) VDE 0884 testing is an option; the suffix letter "V" must be added to the standard number.
(5) For more information regarding the use of VDE approved devices, refer to "VDE Circuit Board Layout Design Rules" in the Applications Information section.

Optoisolators 6–Pin DIP Varieties and Lead Form Options

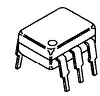
Transistor **Darlington**



Resistor Darlington



Style 1



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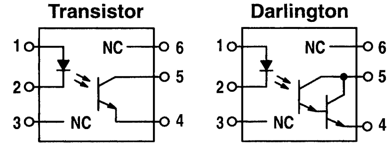
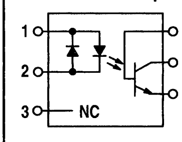
Transistor **Darlington**

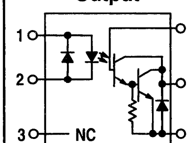


Style 3

AC Input Transistor Output

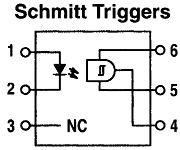


AC Input Resistor–Darlington Output



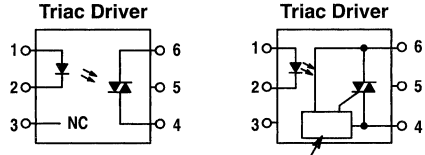
Style 8

Schmitt Triggers



Style 5

Random Phase Triac Driver **Zero Crossing Triac Driver**



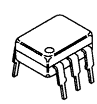
Zero Crossing Circuit

Style 6

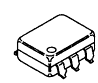
An optoisolator consists of a gallium arsenide infrared emitting diode, IRED, optically coupled to a monolithic silicon photodetector in a wide array of standard devices and encourages the use of special designs and selections for special applications. All Motorola optoisolators have V_{ISO} rating of 7500 Vac(pk), exceeding all other industry standard ratings.

Motorola offers global regulatory approvals, including UL, CSA, AUSTEL, NEMKO, BABT, SETI, SEMKO, and DEMKO. VDE(1) approved per standard 0884/8.87, with additional approvals to DIN IEC950 and IEC380/VDE 0806, IEC435/VDE 0805, IEC65/VDE 0860, VDE 110b, also covering all other standards with equal or less stringent requirements, including IEC204/VDE 0113, VDE 0160, VDE 0832, VDE 0833.

(1) VDE 0884/8.87 testing is an option; the suffix "V" must be added to the standard part number (see VDE Approved Optoisolators in Section 3).

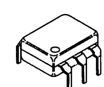


CASE 730A–04



S

(S) CASE 730C–04
Surface–mountable gull–wing option



T

(T) CASE 730D–05
Wide–spaced (0.400) lead form option

Optoisolator Lead Form Options:

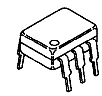
Motorola's 6–pin, dual in–line optoisolators can be ordered in either a surface–mountable, gull–wing lead form or a wide–spaced 0.400″ through–hole lead form, which is used to satisfy 8 mm PC board spacing requirements. ***Please first consult factory regarding availability for your lead form option, prior to ordering!***

- Attach "S" to any Motorola 6–pin, dual in–line part number for surface–mountable, gull–wing lead form.
- Attach "T" to any Motorola 6–pin, dual in–line part number for wide–spaced 0.400" through–hole lead form.

Tape and Reel Options:

- Attach "SR2" suffix to any Motorola 6–pin, dual in–line part number for tape and reeled, surface–mountable, gull–wing lead form.

6–Pin Dual In–Line Package



CASE 730A–04

Table 1. Transistor Output
Pinout: 1–Anode, 2–Cathode, 3–N.C., 4–Emitter, 5–Collector, 6–Base (Style 1)

Device	Current Transfer Ratio (CTR) % Min	@ I_F mA	V_{CE} Volts	$V_{CE(sat)}$ Volts Max	@ I_F mA	I_C mA	t_r/t_f or t_{on}*/t_{off}* Typ µs	@ I_C mA	V_{CC} Volts	R_L Ω	I_F mA	$V_{(BR)CEO}$ Volts Min	V_F Volts Max	@ I_F mA
TIL111	8	16	0.4	0.4	16	2	5/5	2	10	100		30	1.4	16
4N27	10	10	10	0.5	50	2	1.2/1.3	10	10	100		30	1.5	10
4N28	10	10	10	0.5	50	2	1.2/1.3	10	10	100		30	1.5	10
4N38,A	20	20	1	1	20	4	1.6/2.2	10	10	100		80	1.5	10
4N25,A	20	10	10	0.5	50	2	1.2/1.3	10	10	100		30	1.5	10
4N26	20	10	10	0.5	50	2	1.2/1.3	10	10	100		30	1.5	10
MCT2	20	10	10	0.4	16	2	1.2/1.3		5	2k	15	30	1.5	20
MCT2E	20	10	10	0.4	16	2	1.2/1.3	2	10	100		30	1.5	20
CNY17–1	40–80	10	5	0.4	10	2.5	1.6/2.3″		5	75	10	70	1.65	60
MCT271	45–90	10	10	0.4	16	2	4.9*/4.5*	2	5	100		30	1.5	20
MOC8100	50	1	5	0.5	1	0.1	3.8/5.6	2	10	100		30	1.4	1
H11A1	50	10	10	0.4	10	0.5	1.2/1.3	2	10	100		30	1.5	10
H11A550	50	10	10	0.4	20	2	5*/5*	2	10	100		30	1.5	10
TIL117	50	10	10	0.4	10	0.5	5/5	2	10	100		30	1.4	16
TIL126	50	10	10	0.4	10	1	2/2	2	10	100		30	1.4	10
SL5501	45–250	10	0.4	0.4	20	2	20*/50*		5	1k	16	30	1.3	20
CNY17–2	63–125	10	5	0.4	10	2.5	1.6/2.3		5	75	10	70	1.65	60
MCT275	70–210	10	10	0.4	16	2	4.5*/3.5*	2	5	100		80	1.5	20
MCT272	75–150	10	10	0.4	16	2	6*/5.5*	2	5	100		30	1.5	20
4N35	100	10	10	0.3	10	0.5	3.2/4.7	2	10	100		30	1.5	10
4N36	100	10	10	0.3	10	0.5	3.2/4.7	2	10	100		30	1.5	10
4N37	100	10	10	0.3	10	0.5	3.2/4.7	2	10	100		30	1.5	10
CNY17–3	100–200	10	5	0.4	10	2.5	1.6/2.3		5	75	10	70	1.65	60
H11AV1	100–300	10	10	0.4	20	2	5*/4*	2	10	100		70	1.5	10
H11AV2	50	10	10	0.4	20	2	5*/4*	2	10	100		70	1.5	10
MCT273	125–250	10	10	0.4	16	2	7.6*/6.6*	2	5	100		30	1.5	20

Table 2. Transistor Output with No Base Connection
Pinout: 1–Anode, 2–Cathode, 3–N.C., 4–Emitter, 5–Collector, 6–Base (Style 3)

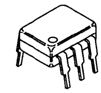
MOC8101	50–80	10	10	0.4	5	0.5	3.2/4.7	2	10	100		30	1.5	10
MOC8102	73–117	10	10	0.4	5	0.5	3.2/4.7	2	10	100		30	1.5	10
MOC8103	108–173	10	10	0.4	5	0.5	3.2/4.7	2	10	100		30	1.5	10
MOC8104	160–256	10	10	0.4	5	0.5	3.2/4.7	2	10	100		30	1.5	10
MOC8105	65–133	10	10	0.4	5	0.5	3.2/4.7	2	10	100		30	1.5	10
MOC8111	20	10	10	0.4	10	0.5	3.2/4.7	2	10	100		30	1.5	10
MOC8112	50	10	10	0.4	10	0.5	3.2/4.7	2	10	100		30	1.5	10
MOC8113	100	10	10	0.4	10	0.5	3.2/4.7	2	10	100		30	1.5	10

Table 3. AC Input – Transistor Output
Pinout: 1–LED 1 Anode/LED 2 Cathode, 2–LED 1 Cathode/LED 2 Anode, 3–N.C., 4–Emitter, 5–Collector, 6–Base (Style 8)

Device	Current Transfer Ratio (CTR) % Min	@ I_F mA	V_{CE} Volts	$V_{CE(sat)}$ Volts Max	@ I_F mA	I_C mA	t_r/t_f or t_{on}*/t_{off}* Typ µs	@ I_C mA	V_{CC} Volts	R_L Ω	I_F mA	$V_{(BR)CEO}$ Volts Min	V_F Volts Max	@ I_F mA
H11AA1	20	±10	10	0.4	±10	0.5						30	1.5	±10
H11AA2	10	±10	10	0.4	±10	0.5						30	1.8	±10
H11AA3	50	±10	10	0.4	±10	0.5						30	1.5	±10
H11AA4	100	±10	10	0.4	±10	0.5						30	1.5	±10

Devices listed in bold, italic are Motorola preferred devices.

6–Pin Dual In–Line Package (continued)



CASE 730A–04

Table 4. Darlington Output

Pinout: 1–Anode, 2–Cathode, 3–N.C., 4–Emitter, 5–Collector, 6–Base (Style 1)

	Current Transfer Ratio (CTR)			$V_{CE(sat)}$			t_r/t_f or t_{on}^*/t_{off}^* Typ					$V_{(BR)CEO}$	V_F	
Device	**% Min**	**@ I_F mA**	**V_{CE} Volts**	**Volts Max**	**@ I_F mA**	**I_C mA**	**µs**	**@ I_C mA**	**V_{CC} Volts**	**R_L Ω**	**I_F mA**	**Volts Min**	**Volts Max**	**@ I_F mA**
4N31	50	10	10	1.2	8	2	0.6*/17*	50	10		200	30	1.5	10
4N29,A	100	10	10	1	8	2	0.6*/17*	50	10		200	30	1.5	10
4N30	100	10	10	1	8	2	0.6*/17*	50	10		200	30	1.5	10
MCA231	200	1	1	1.2	10	50	80	10	10	100		30	1.5	20
TIL113	300	10	1.25	1	50	125	300	125	15	100		30	1.5	10
4N32	500	10	10	1	8	2	0.6*/45*	50	10		200	30	1.5	10
4N33	500	10	10	1	8	2	0.6*/45*	50	10		200	30	1.5	10
H11B1	500	1	5	1	1	1	1/2	10	10	100		25	1.5	10
MOC8080	500	10	5	1	1	1	1/2		10	100	5	55	1.5	10

Table 5. Darlington Output with No Base Connection

Pinout: 1–Anode, 2–Cathode, 3–N.C., 4–Emitter, 5–Collector, 6–N.C. (Style 3)

MOC119	300	10	2	1	10	10	1/2	2.5	10	100		30	1.5	10
MOC8030	300	10	1.5				1/2		50	100	10	80	2	10
MOC8020	500	10	5				1/2		50	100	10	50	2	10
MOC8050	500	10	1.5				1/2		50	100	10	80	2	10
MOC8021	1000	10	5				1/2		50	100	10	50	2	10

Table 6. Resistor Darlington Output

Pinout: 1–Anode, 2–Cathode, 3–N.C., 4–Emitter, 5–Collector, 6–Base (Style 1)

H11G1	1000	10	1	1	1	1	5*/100*		5	100	10	100	1.5	10
H11G2	1000	10	1	1	1	1	5*/100*		5	100	10	80	1.5	10
H11G3	200	1	5	1.2	50	20	5*/100*		5	100	10	55	1.5	10

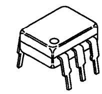
Table 7. High Voltage Transistor Output

Pinout: 1–Anode, 2–Cathode, 3–N.C., 4–Emitter, 5–Collector, 6–Base (Style 1)

MOC8204	20	10	10	0.4	10	0.5	5*/5*	2	10	100		400	1.5	10
H11D1	20	10	10	0.4	10	0.5	5*/5*	2	10	100		300	1.5	10
H11D2	20	10	10	0.4	10	0.5	5*/5*	2	10	100		300	1.5	10

Devices listed in bold, italic are Motorola preferred devices.

6–Pin Dual In–Line Package (continued)



CASE 730A–04

Table 8. Triac Driver Output
Pinout: 1–Anode, 2–Cathode, 3–N.C., 4–Main Terminal, 5–Substrate, 6–Main Terminal (Style 6)

Device	Peak Blocking Voltage Min	LED Trigger Current–I_{FT} (V_{TM} = 3 V) mA Max	Zero Crossing Inhibit Voltage (at rated I_{FT}) Volts Max	Operating Voltage Vac	dv/dt V/µs Typ
MOC3010	250	15	—	125	10
MOC3011	250	10	—	125	10
MOC3012	250	5	—	125	10
MOC3021	400	15	—	125/280	10
MOC3022	400	10	—	125/280	10
MOC3023	400	5	—	125/280	10
MOC3051*	600	15	—	125/280	2000
MOC3052*	600	10	—	125/280	2000
MOC3031	250	15	20	125	2000
MOC3032	250	10	20	125	2000
MOC3033	250	5	20	125	2000
MOC3041	400	15	20	125/280	2000
MOC3042	400	10	20	125/280	2000
MOC3043	400	5	20	125/280	2000
MOC3061	600	15	20	125/280	1500
MOC3062	600	10	20	125/280	1500
MOC3063	600	5	20	125/280	1500
MOC3162*	600	10	15	125/280	1000
MOC3163*	600	5	15	125/280	1000
MOC3081	800	15	20	125/280/320	1500
MOC3082	800	10	20	125/280/320	1500
MOC3083	800	5	20	125/280/320	1500

* New Device Offering

Table 9. Schmitt Trigger Output
Pinout: 1–Anode, 2–Cathode, 3–N.C., 4–Output, 5–Ground, 6–V_{CC} (Style 5)

Device	Threshold Current On mA Max	Threshold Current Off mA Min	$I_{F(off)}/I_{F(on)}$ Min	$I_{F(off)}/I_{F(on)}$ Max	V_{CC} Min	V_{CC} Max	t_r, t_f µs Typ
H11L1	1.6	0.3	0.5	0.9	3	16	0.1
H11L2	10	0.3	0.5	0.9	3	16	0.1
MOC5007	1.6	0.3	0.5	0.9	3	16	0.1
MOC5008	4	0.3	0.5	0.9	3	16	0.1
MOC5009	10	0.3	0.5	0.9	3	16	0.1

Devices listed in bold, italic are Motorola preferred devices.

Small Outline — Surface Mount

CASE 846–01
SO–8 DEVICES

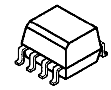


Table 10. Transistor Output
Pinout: 1–Anode, 2–Cathode, 3–N.C., 4–N.C., 5–Emitter, 6–Collector, 7–Base, 8–N.C. (Style 1)

Device	Marking	Current Transfer Ratio (CTR)			$V_{CE(sat)}$			t_r/t_f Typ				$V_{(BR)CEO}$ Volts Min	V_F	
		% Min	@ I_F mA	V_{CE} Volts	Volts Max	@ I_F mA	I_C mA	µs	@ I_C mA	V_{CC} Volts	R_L Ω		Volts Max	@ I_F mA
MOC205,R2	205	40–80	10	10	0.4	10	2	1.6	2	10	100	70	1.5	10
MOC206,R2	206	63–125	10	10	0.4	10	2	1.6	2	10	100	70	1.5	10
MOC207,R2	207	100–200	10	10	0.4	10	2	1.6	2	10	100	70	1.5	10
MOC211,R2	211	20	10	10	0.4	10	2	3.2	2	10	100	30	1.5	10
MOC212,R2	212	50	10	10	0.4	10	2	3.2	2	10	100	30	1.5	10
MOC213,R2	213	100	10	10	0.4	10	2	3.2	2	10	100	30	1.5	10
MOC215,R2	215	20	1	5	0.4	1	0.1	3.2	2	10	100	30	1.3	1
MOC216,R2	216	50	1	5	0.4	1	0.1	3.2	2	10	100	30	1.3	1
MOC217,R2	217	100	1	5	0.4	1	0.1	3.2	2	10	100	30	1.3	1

Table 11. Darlington Output
Pinout: 1–Anode, 2–Cathode, 3–N.C., 4–N.C., 5–Emitter, 6–Collector, 7–Base, 8–N.C. (Style 1)

MOC223,R2	223	500	1	5	1	1	0.5	2	5	10	100	30	1.3	1
MOC263,R2*	263	500	1	5	1	1	0.5	2	5	10	100	30	1.3	1

All devices are shipped in tape and reel format. (See Tape and Reel Specifications Section for more information.)
*No Base Connection to Pin 7

Table 12. AC Input – Transistor Output (Single Channel) (Style 2)

MOC256,R2	256	20	±10	10	0.4	±10	0.5					30	1.5	±10

Table 13. Transistor Output (Dual Channel) (Style 3)

MOCD207,R2	D207	100–200	10	10	0.4	10	2	1.6	2	10	100	70	1.5	10
MOCD208,R2	D208	45–125	10	10	0.4	10	2	1.6	2	10	100	70	1.5	10
MOCD211,R2	D211	20	10	10	0.4	10	2	3.2	2	10	100	30	1.5	10
MOCD213,R2	D213	100	10	10	0.4	10	2	3.2	2	10	100	70	1.5	10
MOCD217,R2	D217	100	1	5	0.4	1	0.1	3.2	2	10	100	30	1.5	1

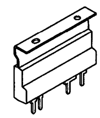
Table 14. Darlington Output (Dual Channel) (Style 3)

MOCD223,R2	D223	500	1	5	1	1	0.5	2	5	10	100	30	1.3	1

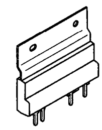
R2 devices are shipped in tape and reel format. (See Tape and Reel Specifications Section for more information.)

Devices listed in bold, italic are Motorola preferred devices.

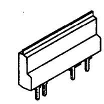
POWER OPTO™ Isolators



CASE 417-02
PLASTIC PACKAGE



CASE 417A-02
PLASTIC PACKAGE



CASE 417B-01
PLASTIC PACKAGE

Table 15. POWER OPTO Isolator 2 Amp Zero–Cross or Random Phase Triac Outputs
Pinout: (1,4,5,6,8 No Pin), 2 – LED Cathode, 3– LED Anode, 7–Main Terminal, 9–Main Terminal

Device	Peak Blocking Voltage (Volts) Min	Led Trigger Current If T (V_{TM} = 2 V) mA Max	On State Voltage V_{TM} (Rated I_{FT} I_{TM} = 2 A) (Volts) Max	Zero Crossing Inhibit Voltage (I_F = Rated I_{FT}) (Volts) Max	Operating Voltage Vac Pk (Volts)	dv/dt (static) v/µs (VIN = 200 V) (V/µs) Min
MOC2A40-5	400	5	1.3	10	125	400
MOC2A40-10	400	10	1.3	10	125	400
MOC2A60-5	600	5	1.3	10	125/220	400
MOC2A60-10	600	10	1.3	10	125/220	400

All devices are shipped in rails.
No suffix = Case 417–02/Style 2 (Standard Heat Tab),
"F" suffix = Case 417–02/Style 1 (Flush Mount Heat Tab)
"C" suffix = Case 417B–01/Style 1 (Cut Tab)

Devices listed in bold, italic are Motorola preferred devices.

Sensors

In Brief . . .

Pressure Sensors

Combining integrated circuit technology with the most advanced pressure sensor architecture now offers an unrivaled combination of performance, reliability and design adaptability in a single monolithic pressure sensing element — the Motorola MPX series of pressure transducers. Available in several versions:

- Fully signal conditioned for high–level output;
- High Impedance, temperature compensated and calibrated, for low current designs;
- Temperature compensated and calibrated, for simplified circuit design;
- Uncompensated for unlimited adaptability

This series of sensors provides both electrical and mechanical design–in options that uniquely fit the varying requirements of the system designer.

Page

Pressure Sensors

Introduction

Motorola pressure sensors combine advanced piezoresistive sensor architecture with integrated circuit technology to offer a wide range of pressure sensing devices for automotive, biomedical, consumer and industrial applications. Selection versatility includes choice of:

Pressure Ranges in PSI
0 to 1.45, 0 to 6, 0 to 7.3, 0 to 14.5, 0 to 29, 0 to 75, 0 to 100, 0 to 150

Sensing Options
Uncompensated, Temperature Compensated/Calibrated, High Impedance, and Signal Conditioned (with on–chip amplifiers)

Application Measurements
Absolute, Differential, Gauge

Package Options
Basic Element, Ported Elements for specific measurements

The Basic Structure

The Motorola pressure sensor is designed utilizing a monolithic silicon piezoresistor, which generates a changing output voltage with variations in applied pressure. The resistive element, which constitutes a strain gauge, is ion implanted on a thin silicon diaphragm.

Applying pressure to the diaphragm results in a resistance change in the strain gauge, which in turn causes a change in the output voltage in direct proportion to the applied pressure. The strain gauge is an integral part of the silicon diaphragm, hence there are no temperature effects due to differences in thermal expansion of the strain gauge and the diaphragm. The output parameters of the strain gauge itself are temperature dependent, however, requiring that the device be compensated if used over an extensive temperature range. Simple resistor networks can be used for narrow temperature ranges, i.e., 0°C to 85°C. For temperature ranges from –40°C to +125°C, more extensive compensation networks are necessary.

Motorola's Patented X–ducer™

Excitation current is passed longitudinally through the resistor (taps 1 and 3), and the pressure that stresses the diaphragm is applied at a right angle to the current flow. The stress establishes a transverse electric field in the resistor that is sensed as voltage at taps 2 and 4, which are located at the midpoint of the resistor. The single–element transverse voltage strain gauge can be viewed as the mechanical analog of a Hall effect device.

Using a single element eliminates the need to closely match the four stress and temperature sensitive resistors that form a Wheatstone bridge design. At the same time, it greatly simplifies the additional circuitry necessary to accomplish calibration and temperature compensation. The offset does not depend on matched resistors but instead on how well the transverse voltage taps are aligned. This alignment is accomplished in a single photolithographic step, making it easy to control, and is only a positive voltage, simplifying schemes to zero the offset.

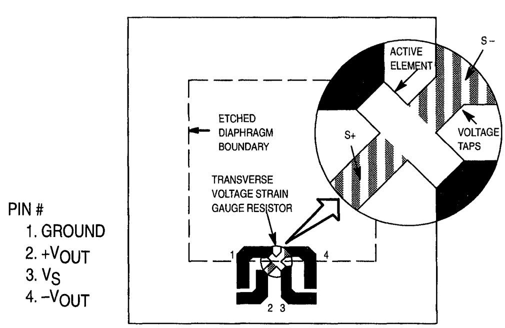


Figure 1. Basic Uncompensated Sensor Element — Top View

Linearity

Linearity refers to how well a transducer's output follows the equation: $V_{out} = V_{off}$ + sensitivity x P over the operating pressure range. There are two basic methods for calculating nonlinearity: (1) end point straight line fit (see Figure 2) or (2) a least squares best line fit. While a least squares fit gives the "best case" linearity error (lower numerical value), the calculations required are burdensome.

Conversely, an end point fit will give the "worst case" error (often more desirable in error budget calculations) and the calculations are more straightforward for the user. Motorola's specified pressure sensor linearities are based on the end point straight line method measured at the midrange pressure.

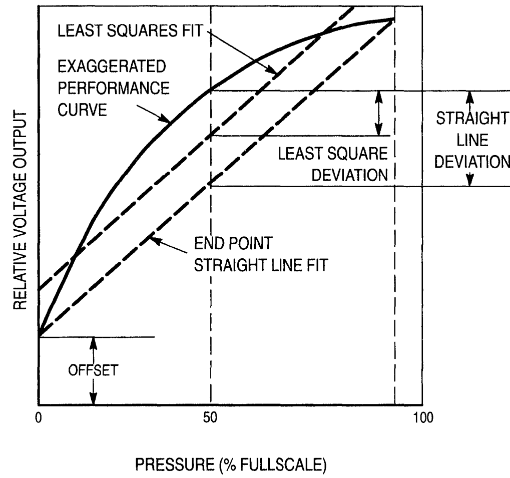


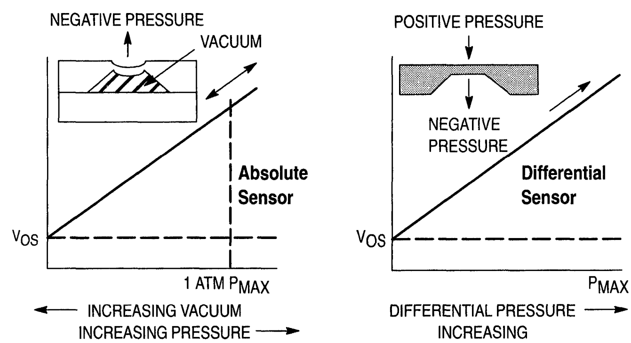
Figure 2. Linearity Specification Comparison

Operation

Motorola pressure sensors support three types of pressure measurements: Absolute Pressure, Differential Pressure and Gauge Pressure.

Absolute Pressure Sensors measure an external pressure relative to a zero–pressure reference (vacuum) sealed inside the reference chamber of the die during manufacture. This corresponds to a deflection of the diaphragm equal to approximately 14.5 psi (one atmosphere), generating a quiescent full–scale output for the MPX100A (14.5 psi) sensor, and a half–scale output for the MPX200A (29 psi) device. Measurement of external pressure is accomplished by applying a relative negative pressure to the "Pressure" side of the sensor.

Differential Pressure Sensors measure the difference between pressures applied simultaneously to opposite sides of the diaphragm. A positive pressure applied to the "Pressure" side generates the same (positive) output as an equal negative pressure applied to the "Vacuum" side.



Motorola sensing elements can withstand pressure inputs as high as four times their rated capacity, although accuracy at pressures exceeding the rated pressure will be reduced. When excessive pressure is reduced, the previous linearity will immediately be restored.

Figure 3. Pressure Measurements

Gauge Pressure readings are a special case of differential measurements in which the pressure applied to the "Pressure" side is measured against the ambient atmospheric pressure applied to the "Vacuum" side through the vent hole in the chip of the differential pressure sensor elements.

Typical Electrical Characteristic Curves

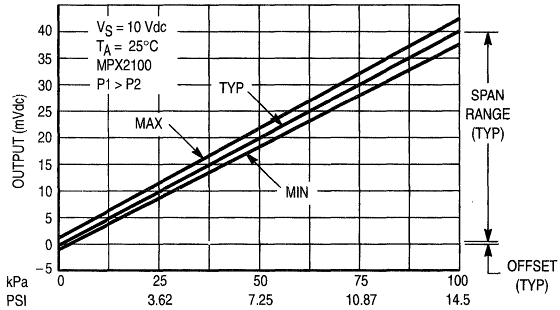


Figure 4. Output versus Pressure Differential

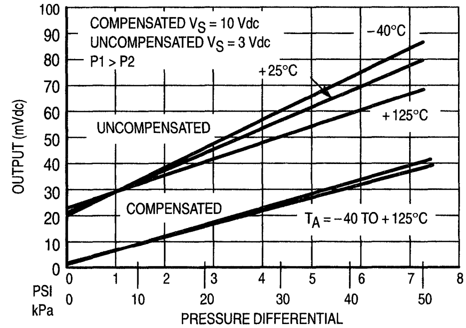


Figure 5. Typical–Output Voltage versus Pressure and Temperature for Compensated and Uncompensated Devices

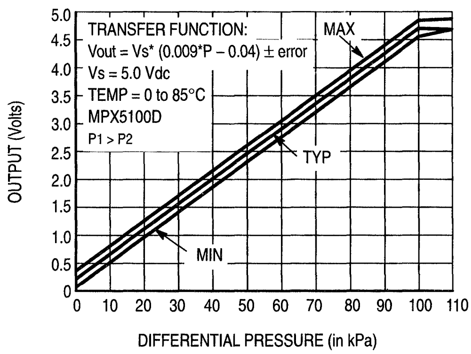


Figure 6. Signal Conditioned MPX5100

Unibody Cross–sectional Drawings

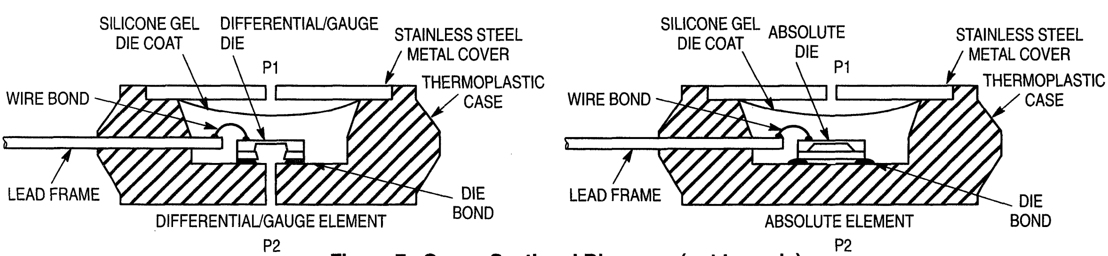


Figure 7. Cross–Sectional Diagrams (not to scale)

Figure 7 illustrates the absolute sensing configuration (right) and the differential or gauge configuration in the basic chip carrier (Case 344). A silicone gel isolates the die surface and wire bonds from harsh environments, while allowing the pressure signal to be transmitted to the silicon diaphragm.

The MPX series pressure sensor operating characteristics and internal reliability and qualification tests are based on use of dry air as the pressure media. Media other than dry air may have adverse effects on sensor performance and long term stability. Contact the factory for information regarding media compatibility in your application.

Pressure Side Identification

Motorola designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The Pressure (P1) side is the side containing the silicon gel which protects the die. The differential or gauge sensor is designed to operate with positive differential pressure applied, P1 > P2.

The absolute sensor is designed for vacuum applied to P1 side.

The Pressure (P1) side may be identified by using the table below.

Table 1. Pressure (P1) / Vacuum (P2) Side Identification

Part Number	Case Type 4 PIN	Positive Pressure Side Identifier
MPXxxxxA MPXxxxxD	344–08	Stainless Steel Cap
MPXxxxxDP	352–02	Side with Part Marking
MPXxxxxAP MPXxxxxGP	350–03	Side with Port Attached
MPXxxxxGVP	350–04	Stainless Steel Cap
MPXxxxxAS MPXxxxxGS	371–06	Side with Port Attached
MPXxxxxGVS	371–05	Stainless Steel Cap
MPXxxxxASX MPXxxxxGSX	371C–02	Side with Port Attached
MPXxxxxGVSX	371D–02	Stainless Steel Cap
Part Number	**Case Type 6 PIN**	**Positive Pressure Side Identifier**
MPXxxxxA MPXxxxxD	867–04	Stainless Steel Cap
MPXxxxxDP	867C–03	Side with Part Marking
MPXxxxxAP MPXxxxxGP	867B–03	Side with Port Attached
MPXxxxxGVP	867D–03	Stainless Steel Cap
MPXxxxxAS MPXxxxxGS	867E–02	Side with Port Attached
MPXxxxxGVS	867A–03	Stainless Steel Cap
MPXxxxxASX MPXxxxxGSX	867F–02	Side with Port Attached
MPXxxxxGVSX	867G–02	Stainless Steel Cap
MPXxxxxGVW	867H–02	Stainless Steel Cap

PRESSURE SENSOR PRODUCTS

Table 2. Uncompensated

Device Series	Max Pressure Rating psi	Max Pressure Rating kPa	Over Pressure (kPa)	Offset mV (Typ)	Full Scale Span mV (Typ)	Sensitivity (mV/kPa)	Linearity % of FSS(1) (Min)	Linearity % of FSS(1) (Max)
MPX10D	1.45	10	75	20	35	3.5	–1.0	1.0
MPX50D	7.3	50	200	20	60	1.2	–0.25	0.25
MPX100D,A	14.5	100	200	20	60	0.6	–0.25	0.25
MPX200D,A	29	200	400	20	60	0.3	–0.25	0.25
MPX700A	100	700	2800	20	60	0.086	– 1.0	1.0
MPX700D	100	700	2800	20	60	0.086	–0.50	0.50
MPX906D	**0.87**	**6**	**100**	**20**	**20**	**3.3**	**–0.50**	**2.0**

Table 3. Compensated and Calibrated (On–Chip)

Device Series	Max Pressure Rating psi	Max Pressure Rating kPa	Over Pressure (kPa)	Offset mV (Typ)	Full Scale Span mV (Typ)	Sensitivity (mV/kPa)	Linearity % of FSS(1) (Min)	Linearity % of FSS(1) (Max)
MPX2010D	1.45	10	75	±1.0	25	2.5	–1.0	1.0
MPX2050D	7.3	50	200	±1.0	40	0.8	–0.25	0.25
MPX2052D	7.3	50	200	±0.1	40	0.8	–0.55	0.25
MPX2100A	14.5	100	400	±2.0	40	0.4	–1.0	1.0
MPX2100D	14.5	100	400	±1.0	40	0.4	–0.25	0.25
MPX2200A	29	200	400	±1.0	40	0.2	–1.0	1.0
MPX2200D	29	200	400	±1.0	40	0.2	–0.25	0.25
MPX2700A	100	700	2800	±2.0	40	0.057	–1.0	1.0
MPX2700D	100	700	2800	±1.0	40	0.057	–0.5	0.5

Table 4. High Impedance (On–Chip)

Device Series	Max Pressure Rating psi	Max Pressure Rating kPa	Over Pressure (kPa)	Offset mV (Typ)	Full Scale Span mV (Typ)	Sensitivity (mV/kPa)	Linearity % of FSS(1) (Min)	Linearity % of FSS(1) (Max)
MPX7050D	7.3	50	200	±1.0	40	0.8	–0.25	0.25
MPX7100A	14.5	100	400	±2.0	40	0.4	–1.0	1.0
MPX7100D	14.5	100	400	±1.0	40	0.4	–0.25	0.25
MPX7200A	29	200	400	±2.0	40	0.2	–1.0	1.0
MPX7200D	29	200	400	±1.0	40	0.2	–0.25	0.25

Table 5. Compensated and Calibrated (On–Chip) Medical Grade

Device Series	Max Pressure Rating psi	Max Pressure Rating kPa	Supply Voltage (Vdc)	Offset mV (Max)	Sensitivity (μV/V/mmHg)	Output Impedance Ohms (Max)	Linearity % of FSS(1) (Min)	Linearity % of FSS(1) (Max)
MPX2300DT1	5.8	40	6.0	0.75	5.0	330	–2.0	2.0

(1)Based on end point straight line fit method. Best fit straight line linearity error is approximately 1/2 of listed value.

Table 6. Signal Conditioned (On–Chip)

Device Series	Max Pressure Rating psi	Max Pressure Rating kPa	Over Pressure (kPa)	Full Scale Span V (Typ)	Sensitivity (mV/kPa)	Accuracy (0–85°C) % of V_{FSS}
MPX4100A	15.2	105	400	4.59	54	±1.8
MPX4101A	14.7	102	400	4.59	54	±1.8
MPX4115A	16.6	115	400	4.59	45.9	±1.5
MPX4250A	36.2	250	400	4.69	20	±1.5
MPX5010D	1.45	10	75	4.5	450	±5.0
MPX5050D	7.3	50	200	4.5	90	±2.5
MPX5100A	16.6	115	400	4.5	45	±2.5
MPX5100D	14.5	100	400	4.5	45	±2.5
MPX5500D	72.5	500	2000	4.5	9.0	±2.5
MPX5700D	100	700	2800	4.5	6.0	±2.5
MPX5999D	150	1000	4000	4.7	5.0	±2.5

Table 7. New Products (Pressure)

Device Series	Data Sheet	Engineering Samples Available	Introduction Date	Description
MPXS4100A Series	NOW	NOW	2/96	Surface Mount, 0–105 kPa Signal–Conditioned
MPXS4115A Series	NOW	NOW	2/96	Surface Mount, 15–115 kPa Signal–Conditioned
MPXT2010G Series	NOW	NOW	2/96	Top Piston Fit, 0–10 kPa Temperature Compensated and Calibrated

Bold italic indicates product introduced in the last 12 months.

Table 8. MPX10/50/100/200/700 Series (Uncompensated)

Device Type	Measurement/Porting Options	Package Options	Pressure Range 0 to 1.45 PSI (0 to 10 kPa)	0 to 7.3 PSI (0 to 50 kPa)	0 to 14.5 PSI (0 to 100 kPa)	0 to 29 PSI (0 to 200 kPa)	0 to 100 PSI (0 to 700 kPa)
4–Pin	Absolute	Case 344–12	—	—	MPX100A	MPX200A	MPX700A
Basic Elements	Differential	Case 344–12	MPX10D	MPX50D	MPX100D	MPX200D	MPX700D
Ported Elements	Absolute Port	Case 350–05	—	—	MPX100AP	MPX200AP	MPX700AP
	Absolute Stovepipe	Case 371–07	—	—	MPX100AS	MPX200AS	MPX700AS
	Absolute Axial	Case 371C–03	—	—	MPX100ASX	MPX200ASX	MPX700ASX
	Differential Port	Case 352–03	MPX10DP	MPX50DP	MPX100DP	MPX200DP	MPX700DP
	Gauge	Case 350–05	MPX10GP	MPX50GP	MPX100GP	MPX200GP	MPX700GP
	Gauge Vacuum	Case 350–06	MPX10GVP	MPX50GVP	MPX100GVP	MPX200GVP	—
	Gauge Stovepipe	Case 371–07	MPX10GS	MPX50GS	MPX100GS	MPX200GS	MPX700GS
	Gauge Vacuum Stovepipe	Case 371–08	MPX10GVS	MPX50GVS	MPX100GVS	MPX200GVS	—
	Gauge Axial	Case 371C–03	MPX10GSX	MPX50GSX	MPX100GSX	MPX200GSX	MPX700GSX
	Gauge Vacuum Axial	Case 371D–03	MPX10GVSX	MPX50GVSX	MPX100GVSX	MPX200GVSX	—

Table 9. MPX900 Series (Uncompensated) (Water vapor and soapy water vapor tolerant)

Device Type	Measurement Options	Package Options	Pressure Range 0 to 0.87 PSI (0 to 6 kPa)
6–Pin Basic Element	Differential	Case 867–07	MPX906D
Ported Element	Gauge Axial	Case 867H–03	MPX906GVW

Table 10. MPX2000 Series (Temperature Compensated and Calibrated On–Chip)

Device Type	Measurement Options	Package Options	Pressure Range 0 to 1.45 PSI (0 to 10 kPa)	0 to 7.3 PSI (0 to 50 kPa)	0 to 14.5 PSI (0 to 100 kPa)	0 to 29 PSI (0 to 200 kPa)	0 to 100 PSI (0 to 700 kPa)
4–Pin	Absolute	Case 344–12	—	—	MPX2100A	MPX2200A	MPX2700A
Basic Elements	Differential	Case 344–12	MPX2010D	MPX2050D	MPX2100D	MPX2200D	MPX2700D
Ported Elements	Absolute Port	Case 350–05	—	—	MPX2100AP	MPX2200AP	MPX2700AP
	Absolute Stovepipe	Case 371–07	—	—	MPX2100AS	MPX2200AS	MPX2700AS
	Absolute Axial	Case 371C–03	—	—	MPX2100ASX	MPX2200ASX	MPX2700ASX
	Differential Port	Case 352–03	MPX2010DP	MPX2050DP	MPX2100DP	MPX2200DP	MPX2700DP
	Gauge	Case 350–05	MPX2010GP	MPX2050GP	MPX2100GP	MPX2200GP	MPX2700GP
	Gauge Vacuum	Case 350–06	MPX2010GVP	MPX2050GVP	MPX2100GVP	MPX2200GVP	—
	Gauge Stovepipe	Case 371–07	MPX2010GS	MPX2050GS	MPX2100GS	MPX2200GS	—
	Gauge Vacuum Stovepipe	Case 371–08	MPX2010GVS	MPX2050GVS	MPX2100GVS	MPX2200GVS	—
	Gauge Axial	Case 371C–03	MPX2010GSX	MPX2050GSX	MPX2100GSX	MPX2200GSX	MPX2700GSX
	Gauge Vacuum Axial	Case 371D–03	MPX2010GVSX	MPX2050GVSX	MPX2100GVSX	MPX2200GVSX	—

Table 11. MPX4000 Series (Signal Conditioned On–Chip)

Device Type	Measurement Options	Package Options	Pressure Range 3 to 15 PSI (20 to 105 kPa)	2.3 to 14.7 PSI (15 to 102 kPa)	2.3 to 16.6 PSI (15 to 115 kPa)	3 to 36.2 PSI (20 to 250 kPa)
6–Pin Basic Element	Absolute	Case 867–07	MPX4100A	MPX4101A	MPX4115A	MPX4250A
Ported Element	Absolute Port	Case 867E–03	MPX4100AP	MPX4101AP	MPX4115AP	MPX4250AP
	Absolute Stovepipe	Case 867F–03	MPX4100AS	MPX4101AS	MPX4115AS	MPX4250AS
	Absolute Axial	Case 867B–04	MPX4100ASX	MPX4101ASX	MPX4115ASX	MPX4250ASX

Table 12. MPX5000 Series (Signal Conditioned On–Chip)

Device Type	Measurement Options	Package Options	Pressure Range 0 to 1.45 PSI (0 to 10 kPa)	0 to 7.3 PSI (0 to 50 kPa)	0 to 14.5 PSI (0 to 100 kPa)	2.3 to 14.7 PSI (15 to 115 kPa)	0 to 75 PSI (0 to 500 kPa)	0 to 100 PSI (0 to 700 kPa)	0 to 150 PSI (0 to 1000 kPa)
6–Pin	Absolute	Case 867–07	—	—	—	MPX5100A	—	—	—
Basic Element	Differential	Case 867–07	MPX5010D	MPX5050D	MPX5100D	—	MPX5500D	MPX5700D	MPX5999D
Ported Element	Absolute Port	Case 867B–04	—	—	—	MPX5100AP	—	—	—
	Absolute Stovepipe	Case 867E–03	—	—	—	MPX5100AS	—	—	—
	Absolute Axial	Case 867F–03	—	—	—	MPX5100ASX	—	—	—
	Differential Port	Case 867C–05	MPX5010DP	MPX5050DP	MPX5100DP	—	MPX5500DP	MPX5700DP	—
	Gauge	Case 867B–04	MPX5010GP	MPX5050GP	MPX5100GP	—	MPX5500GP	MPX5700GP	—
	Gauge Vacuum	Case 867D–04	MPX5010GVP	MPX5050GVP	MPX5100GVP	—	—	—	—
	Gauge Stovepipe	Case 867E–03	MPX5010GS	MPX5050GS	MPX5100GS	—	MPX5500GS	MPX5700GS	—
	Gauge Vacuum Stovepipe	Case 867A–04	MPX5010GVS	MPX5050GVS	MPX5100GVS	—	—	—	—
	Gauge Axial	Case 867F–03	MPX5010GSX	MPX5050GSX	MPX5100GSX	—	MPX5500GSX	MPX5700GSX	—
	Gauge Vacuum Axial	Case 867G–03	MPX5010GVSX	MPX5050GVSX	MPX5100GVSX	—	—	—	—

Table 13. MPX7000 Series (Temperature Compensated and Calibrated High Impedance On–Chip)

Device Type	Measurement Options	Package Options	Pressure Range 0 to 7.3 PSI (0 to 50 kPa)	0 to 14.5 PSI (0 to 100 kPa)	0 to 29 PSI (0 to 200 kPa)
4–Pin	Absolute	Case 344–12	—	MPX7100A	MPX7200A
Basic Elements	Differential	Case 344–12	MPX7050D	MPX7100D	MPX7200D
Ported Elements	Absolute Port	Case 350–05	—	MPX7100AP	MPX7200AP
	Absolute Stovepipe	Case 371–07	—	MPX7100AS	MPX7200AS
	Absolute Axial	Case 371C–03	—	MPX7100ASX	MPX7200ASX
	Differential Port	Case 352–03	MPX7050DP	MPX7100DP	MPX7200DP
	Gauge	Case 350–05	MPX7050GP	MPX7100GP	MPX7200GP
	Gauge Vacuum	Case 350–06	MPX7050GVP	MPX7100GVP	MPX7200GVP
	Gauge Stovepipe	Case 371–07	MPX7050GS	MPX7100GS	MPX7200GS
	Gauge Vacuum Stovepipe	Case 371–08	MPX7050GVS	MPX7100GVS	MPX7200GVS
	Gauge Axial	Case 371C–03	MPX7050GSX	MPX7100GSX	MPX7200GSX
	Gauge Vacuum Axial	Case 371D–03	MPX7050GVSX	MPX7100GVSX	MPX7200GVSX

Device Numbering System for Pressure Sensors

MPX Y # # ### ZZZZ

Motorola Pressure X–Ducer

MAXIMUM RATED PRESSURE (kPa)

PACKAGE SELECTION

- **–** **Unibody**
- **B** **Backside Piston Fit**
- **D** **Dual Piston Fit**
- **S** **Surface Mount**
- **T** **Top Piston Fit**

MEDIA TOLERANT

9

FAMILY

- **–** **Basic Element**
- **2** **Temp Comp & Cal**
- **4,5** **Signal Conditioned**
- **7** **High Impedance**

MEASUREMENT TYPE/PORTING OPTION

- **A** **Absolute Element**
- **AP** **Absolute Ported**
- **AS** **Absolute Stovepipe Ported**
- **D** **Differential and Gauge Element**
- **DP** **Differential Dual Ported**
- **GP** **Gauge Ported**
- **GVP** **Gauge Vacuum Ported**
- **GS** **Gauge Stovepipe Ported**
- **GVS** **Gauge Vacuum Stovepipe**
- **GSX** **Gauge Vacuum Ported, Axial**
- **GVSX** **Gauge Vacuum Stove Ported, Axial**
- **GVW** **Gauge Vacuum, Water Tolerant**

Note: Actual device marking may be abbreviated due to space constraints but packaging label will reflect full part number.

ACCELERATION SENSOR PRODUCTS

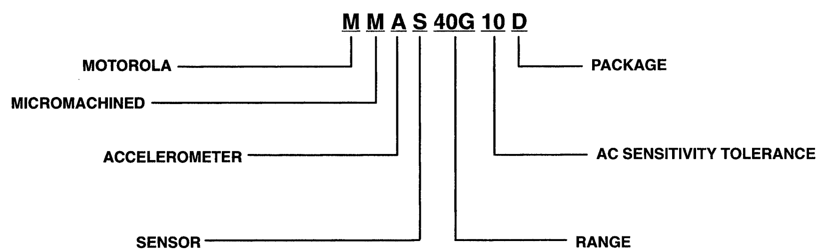
Table 14. Accelerometer Sensor

Device	Range	Sensitivity	Frequency/ Bandwidth (Hz)	Supply Current (μA)	Offset V
MMAS40G10D	±40g	40μv/g	400	5	2.9

Table 15. New Products (Accelerometer)

Device Series	Data Sheet	Engineering Samples Available	Introduction Date	Description
MMAS250G	3Q96	NOW	2Q96	+/–250 g Amplified Accelerometer

Device Numbering System for Accelerometers



EVALUATION TOOLS

Table 16. Sample Kits

Device	Max Pressure Rating psi	Max Pressure Rating kPa	Description	Order Information
MPX2010DP	1.45	10	Device w/Literature	KITNOK29/D
MPX2700DP	100	700	Device w/Literature	KITMPX2700D/D
MPX700DP	100	700	Device w/Literature	KITNOK32/D
MPX5050DP	7.3	50	Device w/Literature	KITMPX5050D/D
MPX5100DP	14.5	100	Device w/Literature	KITMPX5100D/D
MPX5100AP	14.5	100	Device w/Literature	KITMPX5100A/D
MPX7100DP	14.5	100	Device w/Literature	KITMPX7100D/D
MPX7200DP	29	200	Device w/Literature	KITMPX7200D/D

Table 17. Evaluation Kits

Order Information	Description	Device	Max Pressure Rating psi	Max Pressure Rating kPa
KITDEVB114/D	Pressure Sensor with Microprocessor	DEVB–114/AN1305/D	14.5	100
KITDEVB173/D	A Simple Sensor Interface Amplifier	DEVB–173/AN1324/D	14.5	100

Table 18. New Literature

Literature	Description
DL200/D (Rev 2)	Sensor Device Data Book
AN1516/D	Liquid Level Control Using a Motorola Pressure Sensor
AN1517/D	Pressure Switch Design with Semiconductor Pressure Sensors
AN1518/D	Using a Pulse Width Modulated Output with Semiconductor Pressure Sensors
BR3005/D	Senseon Image Brochure – Intelligent Sensor Solutions

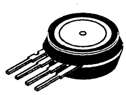
REFERENCE TABLE

Table 19. Pressure Unit Conversion Constants (Most Commonly Used — Per International Conventions)

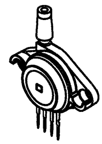
	PSI(1)	in. H_2O(2)	in. Hg(3)	K Pascal	millibar	cm H_2O(4)	mm Hg(5)
PSI(1)	1.000	27.681	2.036	6.8948	68.948	70.309	51.715
in. H_2O(2)	3.6126×10^{-2}	1.000	7.3554×10^{-2}	0.2491	2.491	2.5400	1.8683
in. Hg(3)	0.4912	13.595	1.000	3.3864	33.864	34.532	25.400
K Pascal	0.14504	4.0147	0.2953	1.000	10.000	10.1973	7.5006
millibar	0.01450	0.40147	0.02953	0.100	1.000	1.01973	0.75006
cm H_2O(4)	1.4223×10^{-2}	0.3937	2.8958×10^{-2}	0.09806	0.9806	1.000	0.7355
mm Hg(5)	1.9337×10^{-2}	0.53525	3.9370×10^{-2}	0.13332	1.3332	1.3595	1.000

PRESSURE PACKAGING OPTIONS

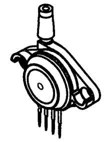
4–PIN



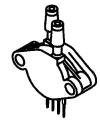
BASIC ELEMENT
CASE 344–12
SUFFIX A/D



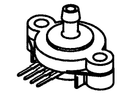
GAUGE PORT
CASE 350-05
SUFFIX AP/GP



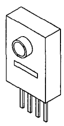
GAUGE VACUUM PORT
CASE 350-06
SUFFIX GVP



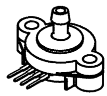
DUAL PORT
CASE 352–03
SUFFIX DP



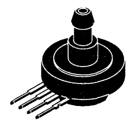
AXIAL PORT
CASE 371C–03
SUFFIX ASX/GSX



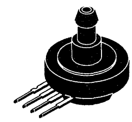
MEDICAL CHIP PACK
CASE 423–04



AXIAL VACUUM PORT
CASE 371D–03
SUFFIX GVSX

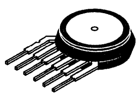


STOVEPIPE PORT
CASE 371-07
SUFFIX GVS

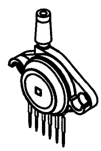


STOVEPIPE VACUUM PORT
CASE 371-08
SUFFIX AS/GS

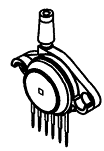
6–PIN



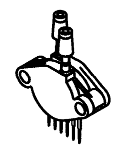
BASIC ELEMENT
CASE 867–07
SUFFIX A/D



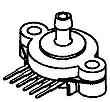
GAUGE PORT
CASE 867B–04
SUFFIX AP/GP



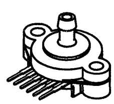
GAUGE VACUUM PORT
CASE 867D–04
SUFFIX GVP



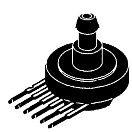
DUAL PORT
CASE 867C–05
SUFFIX DP



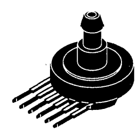
AXIAL PORT
CASE 867F–03
SUFFIX ASX/GSX



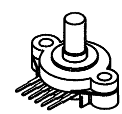
AXIAL VACUUM PORT
CASE 867G–03
SUFFIX GVSX



STOVEPIPE PORT
CASE 867E–03
SUFFIX AS/GS

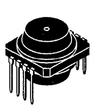


STOVEPIPE VACUUM PORT
CASE 867A–04
SUFFIX GVS

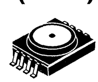


STOVEPIPE MEDIA PORT
CASE 867H–03
SUFFIX GVW

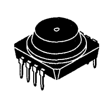
8–PIN (NEW)



DUAL PISTON FIT
CASE 434C–01

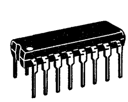


SURFACE MOUNT
CASE 432–01



TOP PISTON FIT
CASE 434A–03

ACCELEROMETER PACKAGING



DIP PACKAGE
CASE 648C–03

RF Products

In Brief . . .

While Motorola is considered to be the supermarket for semiconductor products, there is not a category in which the selection is more diverse, or more complete, than in products designed for RF system applications. From MOS, bipolar power and signal transistors to integrated circuits, Motorola's RF components cover the entire spectrum from HF to microwave to personal communications. Yet, product expansion continues — not only to keep pace with the progressive needs of the industry, but to better serve the needs of designers for a reliable and comprehensive source of supply.

How to Use This Selector Guide

This new selector guide combines the RF products of Motorola Phoenix, Motorola Toulouse (France), and Motorola Hong Kong. The products in this guide are separated FIRST into major categories such as Power FETs, Power Bipolar, Small Signal, Monolithic Integrated Circuits, and Low and High Power Amplifiers. SECOND, within each category parts are listed by frequency band, except for small signal transistors and monolithic integrated circuits, which are divided by application. Small signal transistor applications are low noise, linear amplifiers, switches, and oscillators. Monolithic integrated circuit application groupings are switching, receiver functions and transmitter functions. THIRD, within a frequency band, transistors are further grouped by operating voltage and, finally, output power.

Remember

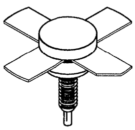
Applications assistance is only a phone call away — call the nearest Semiconductor Sales office or 1-800-521-6274.

RF Discrete Transistors

In the following pages, the reader will find the most extensive group of RF Discrete Transistors offered by any semiconductor manufacturer anywhere in the world today.

From Bipolar to FET, from Low Power to High Power, the user can choose from a variety of packages. They include plastic, metal can and ceramic that are microstrip circuit compatible or surface mountable. Many are designed for automated assembly equipment.

Major sub–headings are MOSFETs, Power Bipolar and Small Signal.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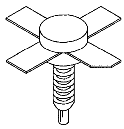
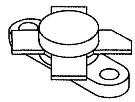
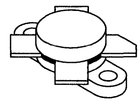
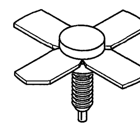
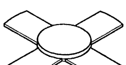
STYLE 1
(.380″ STUD)

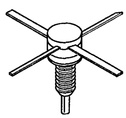

CASE 145D–02
STYLE 1
(.380″ SOE)

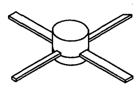

CASE 211–07
STYLE 1, 2
(.380″ FLANGE)

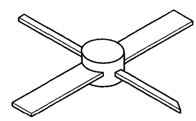

CASE 211–11
STYLE 1, 2
(.500″ FLANGE)

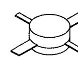

CASE 244
STYLE 1
(.280″ STUD)

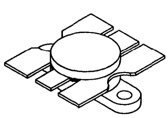

CASE 249
STYLE 1, 3
(.280″ PILL)

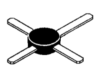

CASE 305
STYLE 1
(.204″ STUD)

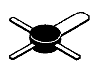

CASE 305A
STYLE 1, 2
(.204″ PILL)

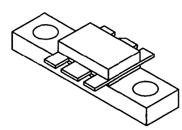

CASE 305C
STYLE 1

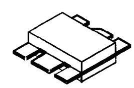

CASE 305D
STYLE 1

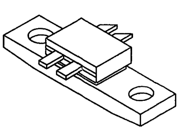

CASE 316–01
STYLE 1, 3
(.500″ CQ)

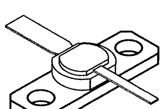

CASE 317
STYLE 1, 2
(MACRO–X)

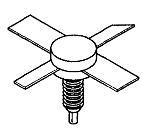

CASE 317D
STYLE 2

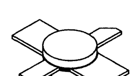

CASE 319
STYLE 1, 2, 3
(CS–12)

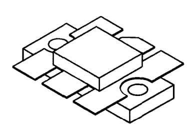

CASE 319A
STYLE 2

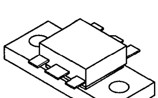

CASE 319B
STYLE 1

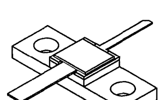

CASE 328A–03
STYLE 1

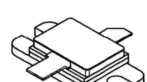

CASE 332–04
STYLE 1, 2
(.280″ STUD)

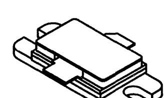

CASE 332A
STYLE 2
(.280″ PILL)

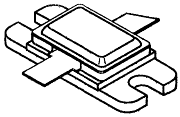

CASE 333
STYLE 1


CASE 333A
STYLE 1, 2
(MAAC PAC)

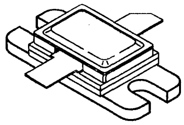

CASE 336E
STYLE 1


CASE 355C
STYLE 1

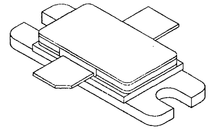

CASE 355D
STYLE 1



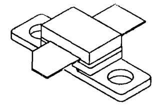
CASE 355E
STYLE 1



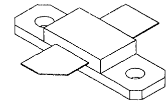
CASE 355G
STYLE 1



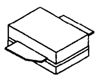
CASE 355H–01
STYLE 1



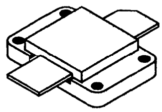
CASE 360A
STYLE 2



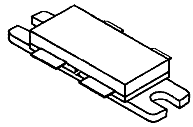
CASE 360B
STYLE 1
(Micro 250)



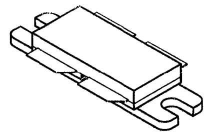
CASE 360C
STYLE 1
(Viper)



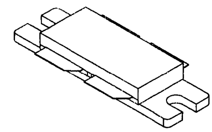
CASE 368
STYLE 2
(HOG PAC)



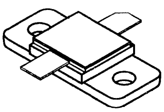
CASE 375
STYLE 2



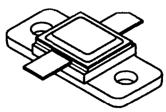
CASE 375A
STYLE 1



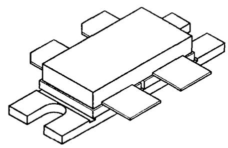
CASE 375B
STYLE 2
(Micro 860)



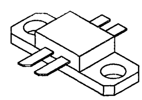
CASE 376B
STYLE 1



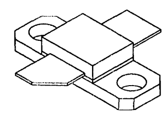
CASE 376C
STYLE 1



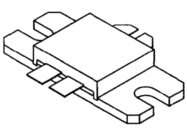
CASE 390B
STYLE 1



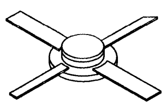
CASE 395B
STYLE 1



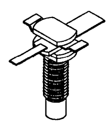
CASE 395C
STYLE 1, 2



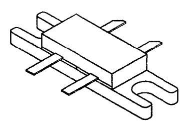
CASE 398
STYLE 1



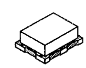
CASE 400
STYLE 1



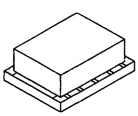
CASE 401
STYLE 1



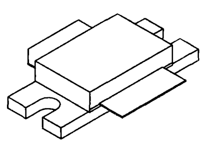
CASE 412
STYLE 1



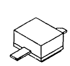
CASE 430
STYLE 2



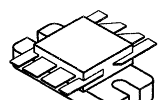
CASE 430B
STYLE 1



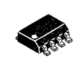
CASE 451
STYLE 1



CASE 458
STYLE 1



CASE 744A
STYLE 1, 2



CASE 751
STYLE 1
(SO–8)

RF Power MOSFETs

Motorola RF Power MOSFETs are constructed using a planar process to enhance manufacturing repeatability. They are *N–channel field effect transistors* with an oxide insulated gate which controls vertical current flow.

Compared with bipolar transistors, RF Power FETs exhibit higher gain, higher input impedance, enhanced thermal stability and lower noise. The FETs listed in this section are specified for operation in RF Power Amplifiers and are grouped by frequency range of operation and type of application. Arrangement within each group is first by order of voltage then by increasing output power.

Table 1. To 54 MHz

Designed for broadband HF & VHF commercial and industrial applications. The high gain and broadband performance of this device makes it ideal for large–signal, common–source amplifier applications in 12.5 volt mobile and base station operation.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 Volts, Class AB						
MRF255★	55	0.8	16/54	45	1.0	211–11/2

Table 2. To 150 MHz HF/SSB

For military and commercial HF/SSB fixed, mobile and marine transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} Typical Gain dB @ 30 MHz	Typical IMD d_3 dB	Typical IMD d_{11} dB	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB							
MRF138	30	0.6	17	–30	–60	1.5	211–07/2
MRF140	150	4.7	15	–30	–60	0.6	211–11/2
V_{DD} = 50 Volts, Class AB							
MRF148	30	0.5	18	–35	–60	1.5	211–07/2
MRF150	150	3	17	–32	–60	0.6	211–11/2
MRF154	600	12	17	–25	—	0.13	368/2
MRF157	600	6	20	–25	—	0.13	368/2

Table 3. To 225 MHz VHF AM/FM

For VHF military and commercial aircraft radio transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Efficiency Typical %	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB						
MRF134	5	0.2	14/150	55	10	211–07/2
MRF136	15	0.38	16/150	60	3.2	211–07/2
MRF136Y	30	1.2	14/150	54	1.8	319B/1
MRF137	30	0.75	16/150	60	1.8	211–07/2
MRF173	80	4	13/150	65	0.8	211–11/2
MRF175LV	100	4	14/225	65	0.65	333/1
MRF174	125	8.3	11.8/150	60	0.65	211–11/2
MRF141	150	15	10/175	55	0.6	211–11/2
MRF175GV	200	8	14/225	65	0.44	375/2
MRF141G	300	30	10/175	55	0.35	375/2
V_{DD} = 50 Volts, Class AB						
MRF151	150	7.5	13/175	45	0.6	211–11/2
MRF176GV	200	4	17/225	55	0.44	375/2
MRF151G	300	7.5	16/175	55	0.35	375/2

★New Product

Table 4. To 500 MHz VHF/UHF AM/FM

For VHF/UHF military and commercial aircraft radio transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB						
MRF158	2	0.02	20/400	55	13.2	305A/2
MRF160	4	0.08	17/400	50	7.2	249/3
MRF166C	20	0.4	17/400	55	2.5	319/3
MRF164W	20	0.4	16.5/400	50	1.5	412/1
MRF166W	40	2	13/400	50	1.0	412/1
MRF175LU	100	10	10/400	55	0.65	333/1
MRF177	100	6.4	12/400	60	0.65	744A/2
MRF177M	100	6.4	12/400	60	0.65	390B/1
MRF175GU	150	9.5	12/400	55	0.44	375/2
V_{DD} = 50 Volts, Class AB						
MRF176GU	150	6	14/400	50	0.44	375/2

Table 5. To 520 MHz

Designed for broadband VHF & UHF commercial and industrial applications. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 12.5 volt mobile and base station operation.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	θ_{JC} °C/W	Package/Style
V_{CC} = 7.5 Volts, Class AB						
MRF5003(18a)	3	0.27	10.5/512	50	14	430/2
MRF5007(18a) ★	7	0.5	11.5/512	55	5	430B/1
V_{CC} = 12.5 Volts, Class AB						
MRF5015	15	1.1	11.5/512	55	3.5	319/3
MRF5035	35	6.3	7.5/512	55	1.8	316–01/3

Table 6. To 1.0 GHz

For HF/VHF/UHF military and commercial radio transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB						
MRF181(46a)	4	0.15	14/1000	55	4.7	458/1
MRF182★	30	1.2	14/1000	55	1.5	360B/1
MRF182S★	30	1.2	14/1000	55	1.5	360C/1
MRF183★	45	1.8	14/1000	55	1.25	360B/1
MRF183S★	45	1.8	14/1000	55	1.25	360C/1
MRF184(46b)	60	1.9	15/1000	55	1.1	360B/1
MRF185(3,46b)	85	3.4	14/1000	55	0.7	375B/2

(3) Internal Impedance Matched Push-Pull Transistors

(18) Tape and Reel Packaging Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units.

(46) To be introduced: a) 1st half of 1996; b) 2nd half of 1996.

★ New Product

RF Power Bipolar Transistors

Motorola's broad line of bipolar RF power transistors are characterized for operation in RF power amplifiers. Typical applications are in military and commercial landmobile, avionics and marine radio transmitters. Groupings are by frequency band and type of application. Within each group, the arrangement of devices is by major supply voltage rating, then in the order of increasing output power. All devices are NPN polarity except where otherwise noted.

HF Transistors

Table 1. 1.5 – 30 MHz, HF/SSB

Designed for broadband operation, these devices feature specified Intermodulation Distortion at rated power output. Applications include mobile, marine, fixed station, and amateur HF/SSB equipment, operating from 12.5, 13.6, 28, or 50 volt supplies.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min) Gain @ 30 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 or 13.6 Volts, Class AB					
MRF421	100 PEP/CW	10	10	0.6	211–11/1
V_{CC} = 28 Volts, Class AB					
MRF426	25 PEP/CW	0.16	22	2.5	211–07/1
MRF422	150 PEP/CW	15	10	0.6	211–11/1
V_{CC} = 50 Volts, Class AB					
MRF429	150 PEP/CW	7.5	13	0.8	211–11/1
MRF448	250 PEP/CW	15.7	12	0.6	211–11/1

Table 2. 14 – 30 MHz, CB/Amateur Band

These HF transistors are designed for economical, high–volume use in CW, AM and SSB applications.

V_{CC} = 12.5 or 13.6 Volts, Class AB

MRF455	60	3	13	1	211–07/1
MRF454	80	5	12	0.7	211–11/1

Table 3. 27 – 50 MHz, Low–Band FM Band

For use in the FM "Low–Band," for Mobile communications.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min) Gain @ 50 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 or 13.6 Volts, Class AB					
MRF492	70	5.6	11	0.7	211–11/1

VHF Transistors

Table 4. 30 – 200 MHz Band

Designed for Military Radio and Commercial Aircraft VHF bands, these 28–volt devices include the all–gold metallized MRF314/16/17 high–reliability series.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class AB					
MRF314	30	3	10/150	2.2	211–07/1
MRF316(2)	80	8	10/150	0.8	316–01/1
MRF317(2)	100	12.5	9/150	0.65	316–01/1

(2)Internal Impedance Matched

Table 5. 136 – 174 MHz High Band

The "workhorse" VHF FM High–Band is served by Motorola with the broadest range of devices and package combinations in the industry.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min) Gain @ 175 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 Volts, Class C					
MRF4427(18b)	1	0.016	18(19)	125(1)	751/1
MRF553	1.5	0.11	11.5	25	317D/2
MRF2628	15	0.95	12	4	244/1
MRF1946	30	3	10	1.6	211–07/1
MRF1946A	30	3	10	1.8	145A–09/1
MRF224	40	14.3	4.5	2.2	211–07/1
MRF240	40	5	9	2.2	145A–09/1
MRF247(2)	75	15	7	0.7	316–01/1

UHF Transistors

Table 6. 100 – 400 MHz Band

Stringent requirements of the UHF Military band are met by MRF325, 326, 327, 329 and 2N6439 types, with all–gold metal systems, specified ruggedness and programmed wirebond construction, to assure consistent input impedances for internally matched parts.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min) Gain @ 400 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class C					
MRF325(2)	30	4.3	8.5	2.2	316–01/1
MRF326(2)	40	5	9	1.6	316–01/1
2N6439(2)	60	10	7.8	1.2	316–01/1
MRF327(2)	80	14.9	7.3	0.7	316–01/1
MRF329(2)	100	20	7	0.7	333/1
MRF392(3)	125	19.8	8	0.7	744A/1

Table 7. 400 – 500 MHz Band

Similar to the 100–400 MHz transistors, these devices have bandwidth capabilities operating up to 500 MHz. All have nitride passivated die, gold metal systems, specified ruggedness and controlled wirebond construction to meet the stringent requirements of military space applications.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class C					
MRF313	1	0.03	15/400	28.5	305A/1
MRF321	10	0.62	12/400	6.4	244/1
MRF323	20	2	10/400	3.2	244/1
MRF393(3)	100	18	7.5/500	0.7	744A/1

(1)$R_{\theta JA}$. Thermal Resistance Junction to Ambient.
(2)Internal Impedance Matched
(3)Internal Impedance Matched Push-Pull Transistors
(18)Tape and Reel Packaging Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units.
(19)Typical

UHF Transistors (continued)

Table 8. 470 – 512 MHz Band

Higher power output devices in this UHF power transistor series feature internally input–matched construction, are designed for broadband operation, and have guaranteed ruggedness under output mismatch and RF overdrive conditions. Devices are specified for handheld, mobile and base station operation.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min)/Freq. Power Gain dB/MHz	$θ_{JC}$ °C/W	Package/Style
V_{CC} = 12.5 Volts, Class C					
MRF581(4)	0.6	0.03	13/500	40	317/2
MRF555	1.5	0.15	10/470	25	317D/2
MRF652	5	0.5	10/512	7	244/1
MRF652S	5	0.5	10/512	7	249/1
MRF653	10	2	7/512	4	244/1
MRF653S	10	2	7/512	4	249/1
MRF641(2)	15	2.5	7.8/470	4	316–01/1
MRF654(2)	15	2.5	7.8/512	4	244/1
MRF644(2)	25	5.9	6.2/470	1.7	316–01/1
MRF650(2)	50	15.8	5.0/512	1.3	316–01/1
MRF658(2)	65	25	4.15/512	1	316–01/1

Device	P_{out} Output Power Watts	Class	P_{in} (Max) Input Power Watts	G_{PE} (Min)/Freq. Power Gain dB/MHz	$θ_{JC}$ °C/W	Package/Style
V_{CC} = 24 Volts						
TP5002S	1.5	A	0.075	13/470	21	249/1
TP5015	15	AB	1.2	11/470	7.0	319/2
TP5051	50	AB	6	9/470	1.2	333A/2

900 MHz Transistors

Table 9. 870 – 960 MHz Band

Designed specifically for the 900 MHz mobile radio band, MRF840 through MRF847 devices offer superior gain and ruggedness, using the unique CS–12 package, which minimizes common–element impedance, and thus maximizes gain and stability. Devices are listed for mobile and base station applications.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min)/Freq. Power Gain dB/MHz	$θ_{JC}$ °C/W	Package/Style
V_{CC} = 12.5 Volts — Class C — Si Bipolar					
MRF559(5)	0.5	0.08	8/870	50	317/2
MRF581(5)	0.6	0.06	10(19)/870	40	317/2
MRF837(5)	0.75	0.11	8/870	40	317/1
MRF8372(5)(18a,b)	0.75	0.11	8/870	45	751/1
MRF557(5)	1.5	0.23	8/870	25	317D/2
MRF839F(5)	3	0.46	8/870	9	319/2
MRF840(2)(6)	10	2.5	6/870	3.1	319/1
MRF842(2)(6)	20	5	6/870	1.5	319/1
MRF844(2)(6)	30	9	5.2/870	1.5	319/1
MRF847(2)(6)	45	16	4.5/870	1	319/1

(2)Internal Impedance Matched
(4)Small signal gain. P_o is Typ.
(5)Common Emitter Configuration
(6)Common Base Configuration
(18)Tape and Reel Packaging Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units.
(19)Typical

900 MHz Transistors (continued)

Table 9. 870 – 960 MHz Band (continued)

Device	P_{out} Output Power Watts	Class	P_{in}(Max) Input Power Watts	Gp (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 24 Volts — Si Bipolar						
MRF890	2	C	0.25	9/900	25	305/1
TP3007S	2	AB	0.25	9/960	21	305C/1
MRF857	2.1 (CW)	A	0.4	12.5/900	8.4	305/1
MRF857S	2.1 (CW)	A	0.4	12.5/900	8.4	305D/1
MRF896	3	AB	0.3	10/900	7	305/1
MRF858	3.6 (CW)	A	0.29	11/900	6.9	319/2
MRF858S	3.6 (CW)	A	0.29	11/900	6.9	319A/2
TP3008	4	AB	0.28	11.5/960	5	319/2
MRF891	5	AB	0.63	9/900	7	319/2
MRF891S	5	AB	0.63	9/900	7	319A/2
MRF859★	6.5 W (CW)	A	0.46	11.5/900	3.9	319/2
MRF859S★	6.5 W (CW)	A	0.46	11.5/900	3.9	319A/2
TP3021	10	AB	1.0	10/960	5.0	319/2
MRF860	13.7 (CW)	A	1.1	11/900	1.9	395B/1
MRF892(2)	14	C	2	8.5/900	3.5	319/1
MRF861	27 (CW)	A	8	9.5/900	0.92	375A/1
MRF894(2)	30	C	6	7/900	1.5	319/1
MRF897(3)	30	AB	3	10/900	1.7	395B/1
MRF897R(3)★	30	AB	3	10.5/900	1.7	395B/1
TP3034	35	AB	7	7/960	2.3	319/2
MRF862	36 (CW)	A	4.5	9/900	0.75	375A/1
MRF898(2)	60	C	12	7/900	1	333A/1
V_{CC} = 26 Volts — Si Bipolar						
MRF880(3)	90	AB	12.7	8.5/900	1.3	375A/1
TP3069	100	AB	18	7.5/960	0.7	375A/1
MRF899(3)	150	AB	24	8/900	0.8	375A/1

(2) Internal Impedance Matched

(3) Internal Impedance Matched Push-Pull Transistors

★ New Product

1.5 GHz Transistors

Table 10. 1400 – 1640 MHz Band

Device	P_{out} Output Power Watts	Class	P_{in}(Max) Input Power Watts	Gp (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
MRF16006	6	C	1.09	7.4/1600	6.8	395C/2
MRF16030	30	C	5.33	7.5/1600	1.7	395C/2

Microwave Transistors

Table 11. L–Band Pulse Power

These products are designed to operate in short pulse width, 10 µs, low duty cycle, 1%, power amplifiers operating in the 960–1215 MHz band. All devices have internal impedance matching. The prime application is avionics equipment for distance measuring (DME), area navigation (TACAN) and interrogation (IFF).

Device	P_{out} Output Power Watts	P_{in}(Max) Input Power Watts	Gp (Min) Gain @ 1090 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 18 Volts — Class A & AB Common Emitter					
MRF1000MA	0.2	0.02	10	25	332–04/2
MRF1000MB	0.2	0.02	10	25	332A/2
V_{CC} = 35 Volts — Class B & C Common Base					
MRF1004MA	4	0.4	10	25	332–04/1
V_{CC} = 50 Volts — Class C Common Base					
MRF1090MA	90	9	10	0.6	332–04/1
MRF1150MA	150	25	7.8	0.3	332–04/1
MRF1375	375	80	6.7	0.12	355G/1

Table 12. L–Band Long Pulse Power

These products are designed for pulse power amplifier applications in the 960–1215 MHz frequency range. They are capable of handling up to 10 µs pulses in long pulse trains resulting in up to a 50% duty cycle over a 3.5 millisecond interval. Overall duty cycle is limited to 25% maximum. The primary applications for devices of this type are military systems, specifically JTIDS and commercial systems, specifically Mode S. Package types are hermetic.

Device	P_{out} Output Power Watts	P_{in}(Max) Input Power Watts	G_{PB} (Min) Gain @ 1215 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts — Class C Common Base					
MRF10005	5	0.71	8.5	8	336E/1
V_{CC} = 36 Volts — Class C Common Base					
MRF10031	30	3	10	3	376B/1
MRF10120	120	19	8	0.6	355C/1

Microwave Transistors (continued)

Table 12. L–Band Long Pulse Power, Class C Common Base (continued)

Device	P_{out} Output Power Watts	P_{in}(Max) Input Power Watts	G_{PB} (Min) Gain @ 1215 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 50 Volts					
MRF10070	70	7	10(7)	0.4	376C/1
MRF10150	150	15	10(7)	0.25	376B/1
MRF10350	350	44	9(7)	0.11	355E/1
MRF10500	500	63	9(7)	0.12	355D/1
MRF10501	500	63	9(7)	0.12	355H/1

Table 13. 2 GHz Narrowband CW

The MRW2000 Series of NPN Silicon microwave power transistors are designed for common base service in amplifier or oscillator applications in the 1–2.3 GHz frequency range.

Device	P_{out} Output Power Watts	P_{in}(Max) Input Power Watts	G_{PB} (Min) Gain @ 2 GHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts — Class B & C Common Base					
MRW2001	1	0.13	9	35	328A/1
MRW2005	5	0.8	8	8.5	328A/1

Table 14. 3 GHz Narrowband CW, Class B & C Common Base

The MRW3000 Series are the industry's first 100% VSWR tolerant 3 GHz devices. They are common–base configured in hermetic packages and rated for 28 volt operation.

Device	P_{out} Output Power Watts	P_{in}(Max) Input Power Watts	G_{PB} (Min) Gain @ 3.0 GHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts					
MRW3001	1	0.2	7	35	328A/1
MRW3003	3	0.75	6	17	328A/1
MRW3005	5	1.6	5	8.5	328A/1

(7)Typical @ 1090 MHz

Linear Transistors

The following sections describe a wide variety of devices specifically characterized for linear amplification. Included are medium power and high power parts covering frequencies from 100 MHz–4 GHz.

Table 15. To 1 GHz, Class A

These devices offer a selection of performance and price for linear amplification to 1 GHz. The "MRA" prefix parts are input matched and feature high overdrive and extreme ruggedness capability.

Device	P_o @ 1 dB Comp. Point Watts	G_{SS} (Min)/Freq. Small Signal Gain dB/MHz	Bias Point (Vdc/A)	θ_{JC} °C/W	Package/Style
V_{CC} = 19 Volts					
MRA1000–7L	7	9/1000	19/1.2	4	145D–02/1
MRA1000–14L	14	8/1000	19/2.4	2.1	145D–02/1
V_{CC} = 25 Volts					
MRF1029(9)	1.5	8/1000	25/0.2	12	244/1
MRF1032(9)	6	6.5/1000	25/0.85	3.5	244/1

Table 16. To 2 GHz, Class A

These parts offer low cost alternatives to matched devices used primarily as pre–drivers to 2 GHz.

Device	P_o @ 1 dB Comp. Point Watts	G_{SS} (Min)/Freq. Small Signal Gain dB/MHz	Bias Point (Vdc/A)	θ_{JC} °C/W	Package/Style
V_{CC} = 20 Volts					
MRF3094(9)	0.5	10.5/2000	20/0.12	40	328A/2
MRF3104(9)	0.5	10.5/2000	20/0.12	40	305A/1
MRF3095(9)	0.8	9/2000	20/0.12	35	328A/2
MRF3105(9)	0.8	9/2000	20/0.12	35	305A/1
MRF3096(9)	1.6	9/2000	20/0.24	22	328A/2
MRF3106(9)	1.6	9/2000	20/0.24	22	305A/1
MRF2000–5L(10)	5	7/2000	19/0.6	10	360A/2

Table 17. UHF Ultra Linear For TV Applications

The following devices have been characterized for ultra–linear applications such as low–power TV transmitters in Band IV and Band V. Each features diffused ballast resistors and an all–gold metal system to provide enhanced reliability and ruggedness.

Device	P_{ref}(Min) Watts	Gp (Min)/Freq. Small Signal Gain dB/MHz	3 Tone IMD(8) dB	θ_{JC} °C/W	Package/Style
V_{CC} = 20 Volts, Class A					
TPV596A	0.5	11.5/860	–58	20	244/1
TPV597	1	10.5/860	–58	9	244/1
TPV598	4	7/860	–60	5	244/1
V_{CC} = 25 Volts, Class A					
TPV695A	14	9.5/860	–47	2.5	395B/1
TPV7025	25	8.5/860	–45	1.5	398/1
TPV6030	20/35(11)	9.5/860	–51/–	1.1	375A/1
V_{CC} = 26 Volts, Class AB					
MRF6414★	—	8.5/960	—	1.3	333A/2
V_{CC} = 28 Volts, Class AB					
TPV8100B	100(11)	8.5/860	—	0.7	398/1

(8)Vision Carrier: – 8 dB; Sound Carrier: – 7 dB; Sideband Carrier: – 16 dB
(9)Former Prefix was "RF"
(10)Former prefix was "MRA."
(11)Output power at 1 dB compression in Class AB
★New Product

Table 18. Microwave Linear For PCN Applications

The following devices have been developed for linear amplifiers in the 1.5–2 GHz region and have characteristics particularly suitable for PCN base station applications.

Device	P_{out} Watts	Class	Bias Point Vdc/mA	Gain (Typ)/Freq dB/MHz	θ_{JC} °C/W	Package/Style
MRF6401(12)	0.5	A	20/80	10/1880	30	305C/1
MRF6402(13)	4.5	AB	26/40	10/1880	5	319/2
MRF6404(16)	30	AB	26/150	8.5/1880	1.4	395C/1
MRF6408★	12	AB	26/100	8.8/1880	2.8	395C/1
MRF15030	30	A, AB	26/125	9/1490	1.4	395C/1
MRF15060(46b)	60	A, AB	26/200	10/1490	0.7	451/451A/1
MRF15090	90	A, AB	26/250	7.5/1490	0.7	375A/1
MRF20060(46b)	60	A, AB	26/200	9/2000	0.7	451/1

Table 19. Microwave Linear Power

Common emitter microwave devices are offered for a wide variety of uses in small and medium signal, Class A, AB and C applications up to 4 GHz. The use of all–gold metal systems, diffused ballast resistors and hermetic packaging results in devices that display excellent reliability even in a military environment.

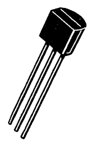
Device	G_{SS} (Min) @ Freq. Small Signal Gain dB/GHz	1 dB Comp. Watts	P_{sat} Watts	–30 dB IMD Watts	Emitter Current mA	Package/Style
V_{DD} = 20 Volts						
MRW53502	5/3	1.6	2	1.5	230	401/1
MRW53601	6/3	0.8	1	0.8	120	328A/1
MRW54001	5/4	0.5	0.8	0.5	120	400/1
MRW54601	6/4	0.5	0.8	0.5	120	328A/1

(12)Formerly known as "TP4001S"
(13)Formerly known as "TP4004"
(16)Formerly known as "TP4035"
(46)To be introduced: a)1st half of 1996; b) 2nd half of 1996.
★New Product

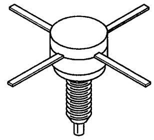
RF Small Signal Transistors

Motorola's broad line of RF Small Signal Transistors includes NPN and PNP Silicon Bipolar Transistors characterized for low noise amplifiers, mixers, oscillators, multipliers, non–saturated switches and low–power drivers.

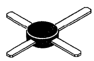
These devices are available in a wide variety of package types: plastic Macro–X and Macro–T, ceramic and surface mounted. Most of these transistors are fully characterized with s–parameters.



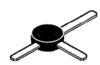
CASE 29–04
STYLE 2
(TO–226AA)



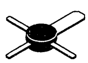
CASE 244A
STYLE 1



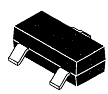
CASE 317
STYLE 2
(MACRO–X)



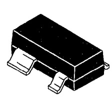
CASE 317A
STYLE 2
(MACRO–T)



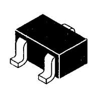
CASE 317D
STYLE 2
(POWER MACRO)



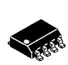
CASE 318–08
STYLE 6
(SOT–23)



CASE 318A
STYLE 1
LOW PROFILE
(SOT–143)



CASE 419
STYLE 3, 6
(SC–70/SOT–323)

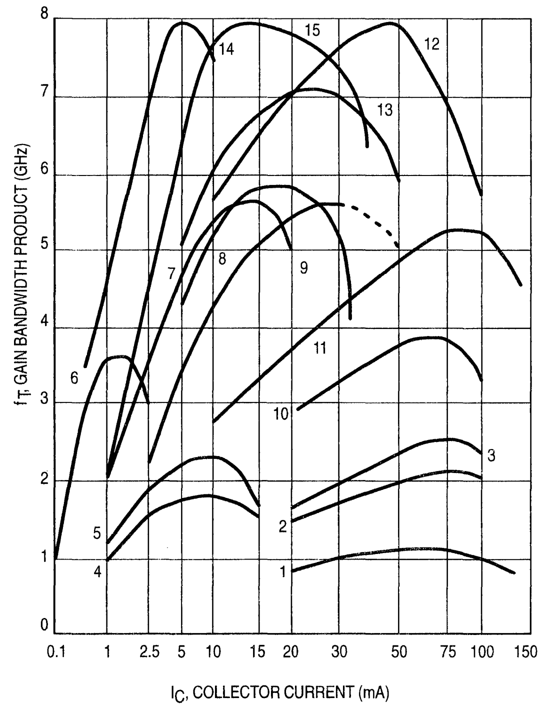


CASE 751
STYLE 1
(SO–8)

RF Small Signal Transistors

RF Small Signal Transistor Gain Characteristics

Curve numbers apply to transistors listed in the subsequent tables.

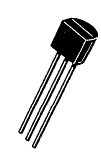


Selection by Package

In small–signal RF applications, the package style is often determined by the end application or circuit construction technique. To aid the circuit designer in device selection, the Motorola broad range of RF small–signal amplifier transistors is organized by package. Devices for other applications such as oscillators or switches are shown in the appropriate preceding tables. **These devices are NPN polarity unless otherwise designated.**

Plastic SOE Case

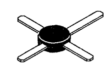
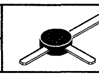
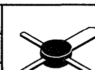
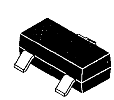
Table 1. Plastic SOE Case

Device	Gain–Bandwidth f_T Typ GHz	@ I_C mA	Curve No. Page 5.10–15	NF_{min} Typ dB	@ f MHz	Gain Typ dB	@ f MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	I_C mA	Package
Case 29–04/1,2, TO–226AA										
LP1001	5	10	—	2.7	500	12.5	1000	15	—	
LP1001A	5	10	—	3.2	1000	12.5	1000	15	—	
MPS901(29)	4.5	15	7	2.4	900	12	900	15	30	
MPS911(29)	7	30	8	1.7	500	16.5	500	12	40	
MPS571	8	50	12	2	500	14	500	10	80	
MPS3866	0.8	50	1	—	—	10	400	30	400	

(29)Packaging Options Available in Tape and Reel and Fan Fold Box

Selection by Package **(continued)**

Table 1. Plastic SOE Case (continued)

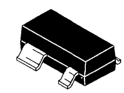
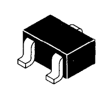
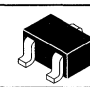
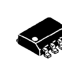
Device	Gain–Bandwidth @ f_T Typ GHz	I_C mA	Curve No. Page 5.10–15	NF_{min} @ f Typ dB	MHz	Gain @ f Typ dB	MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	I_C mA	Package
Case 317/2 — MACRO–X										
MRF901	4.5	15	7	2	1000	12	1000	15	30	
MRF941	8	15	15	2.1	2000	12.5	2000	10	50	
MRF571	8	50	12	1.5	1000	12	1000	10	70	
MRF951	8	30	—	2.1	2000	12.5	2000	10	100	
MRF559	3	100	10	—	—	13	512	18	150	
MRF581	5	75	11	2	500	15.5	500	18	200	
MRF581A	5	75	11	1.8	500	15.5	500	15	200	
MRF837	5	75	11	—	—	10	870	16	200	
Case 317A/2 — MACRO–T										
BFR90	5	14	7	2.4	500	18	500	15	30	
BFR96	4.5	50	9	2	500	14.5	500	15	100	
Case 317D/2										
MRF553	—	—	—	—	—	13	175	16	500	
MRF555	—	—	—	—	—	12.5	470	16	400	
MRF557	—	—	—	—	—	9	870	16	400	
Case 318–08/6 — SOT–23										
MMBR521LT1(17)(18c)	3.4	–35	—	1.5	500	15	500	–10	–70	
MMBR931LT1(18c)	3	1	6	4.3	1000	10	1000	5	5	
MMBR5031LT1(18c)	1	5	—	2.5	450	17	450	10	20	
BFS17LT1(18c)	1.3	25	—	—	—	—	—	15	—	
BFR92ALT1(18c)	4.5	14	—	—	—	15	—	15	25	
MMBR901LT1(18c)	4	15	7	1.9	1000	12	1000	15	30	
BFR93ALT1(18c)	3.4	30	—	2.5	30	—	—	12	35	
MMBR920LT1(18c)	4.5	14	—	2.4	500	15	500	15	35	
MMBR5179LT1(18c)	1.4	5	4	—	—	15	200	12	50	
MMBR941LT1(18c,d)	8	15	15	2.1	2000	8.5	2000	10	50	
MMBR941BLT1(18c,d)	8	15	15	2.1	2000	8.5	2000	10	50	
MMBR911LT1(18c)	6	30	8	2	500	17	500	12	60	
MMBR571LT1(18c)	8	50	12	2	500	16.5	500	10	80	
MMBR951LT1(18c)	8	30	—	2.1	2000	7.5	2000	10	100	
MMBR951ALT1(18c)	8	30	—	2.1	2000	7.5	2000	10	100	

(17)PNP

(18)Tape and Reel Packaging Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units.

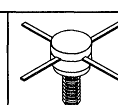
Selection by Package (continued)

Table 1. Plastic SOE Case (continued)

Device	Gain–Bandwidth @ f_T Typ GHz	I_C mA	Curve No. Page 5.10–15	NF_{min} @ f Typ dB	MHz	Gain @ f Typ dB	MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	I_C mA	Package
Case 318A/1 — SOT–143										
MRF5711LT1(18c)	8	50	12	1.6	1000	13.5	1000	10	70	
MRF5211LT1(17)(18c)	4.2	–50	—	2.8	1000	11	1000	–10	–70	
MRF9331LT1(18c)	5	1	—	2.5	1000	12.5	1000	8	2	
MRF9011LT1(18c)	3.8	15	7	2.3	1000	10.2	1000	15	30	
MRF9411LT1(18c)	8	15	15	2.1	2000	9.5	2000	10	50	
MRF9411BLT1(18c)	8	15	15	2.1	2000	9.5	2000	10	50	
MRF0211LT1(18c)	5.5	40	12	1.8	1000	9.5	1000	15	70	
MRF5811LT1 (18c) ★	5	75	11	2.0	500	18.4	500	18	200	
MRF9511LT1(18c)	8	30	—	2.1	2000	9	2000	10	100	
MRF9511ALT1(18c)	8	30	—	2.1	2000	9	2000	10	100	
Case 419/3 — SC–70/SOT–323										
MRF927T1(18c) ★	8	5	14	1.7	1000	9.8	1000	10	10	
MRF947T1(18c,d)	8	15	15	2.1	2000	10.5	1500	10	50	
MRF947AT1(18c)	8	15	15	2.1	2000	10.5	1500	10	50	
MRF947BT1(18c,d)	8	15	15	2.1	2000	10.5	1500	10	50	
MRF957T1(18c)	8	30	—	2.0	2000	9	1500	10	100	
Case 419/6 — SC–70/SOT–323										
MRF947RT3(18d)	8	15	—	2.1	2000	10.5	1500	10	50	
Case 751/1 — SO–8										
MRF5943(18a,b)	1.5	35	2	3.4	200	12	250	30	400	
MRF3866R2(18b)	0.8	50	1	—	—	10.5	400	30	400	
MRF4427(18b)	1.6	50	1	—	—	18	175	20	400	
MRF5812(18a,b)	5.5	75	11	2	500	15.5	500	15	200	
MRF8372(18a,b)	5	75	11	—	—	10	870	16	200	

Ceramic SOE Case

Table 2. Ceramic SOE Case

Device	Gain–Bandwidth @ f_T Typ GHz	I_C mA	Curve No. Page 5.10–15	N @ f Typ dB	MHz	Gain @ f Typ dB	MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	I_C mA	Package
Case 244A/1										
MRF587	5.5	90	11	3	500	13	500	15	200	

(17)PNP

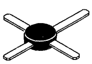
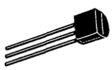
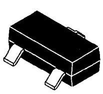
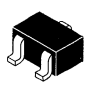
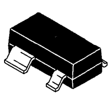
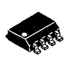
(18)Tape and Reel Packaging Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units.

★ New Product

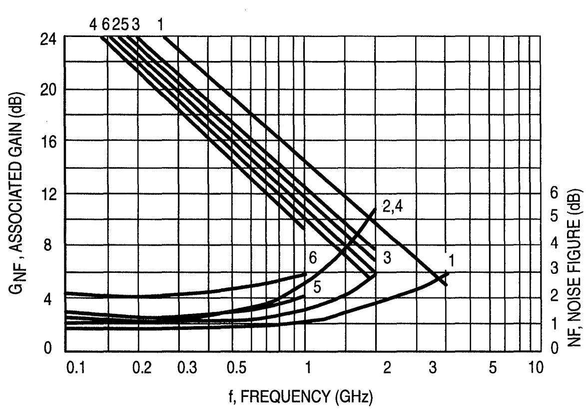
Selection by Application

Table 3. Low Noise

The Small–Signal devices listed are designed for low noise and high gain amplifier mixer, and multiplier applications. Each transistor type is available in various packages. **Polarity is NPN unless otherwise noted.**

Package	Name	Case Number	Curve Number (See figure below)					
			1	2[17]	3	4	5	6
	MACRO–X	317/2	MRF941 MRF951[20]	—	MRF571	MRF581	MRF901	—
	TO–226AA	29–04/2	—	—	MPS571	—	MPS901	MPS911
	SOT–23	318–08/6	MMBR941LT1 MMBR941BLT1 MMBR951LT1[20]	MMBR521LT1	MMBR571LT1	—	MMBR901LT1	MMBR911LT1
	SC–70/ SOT–323	419/3, 6	MRF927T1 MRF947AT1 MRF947T1 MRF947BT1 MRF947RT3 MRF957T1[20]	—	—	—	—	—
	SOT–143	318A/1	MRF9411BLT1 MRF9411LT1 MRF9511LT1[20] MRF9511ALT1	MRF5211LT1	MRF5711LT1 MRF0211LT1	MRF5811LT1	MRF9011LT1	—
	SO–8	751/1	—	—	—	MRF5812	—	—

[17]PNP
[20]Higher Current Version



Gain and Noise Figure versus Frequency

Selection by Application (continued)

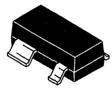
Table 4. CATV, MATV and Class A Linear

For Class A linear CATV/MATV applications. Listed according to increasing gain bandwidth (f_T).

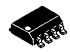
Device	Nominal Test Conditions V_{CE}/I_C Volts/mA	f_T Typ MHz	Noise Figure Typ/Freq. dB/MHz	Distortion Specifications 2nd Order IMD dBc	3rd Order IMD dBc	12 Ch. Cross–Mod. dBc	Output Level dBmV	$V_{(BR)CEO}$ V	Package/ Style
MMBR5179LT1(18c)	6/5	1500	4/450					12	318–08/6
MRF5943(18a,b)	15/50	1500	3.4/200					30	751/1
MMBR5031LT1(18c,d)	6/5	2000	1.9/450					10	318–08/6
MMBR920LT1(18c,d)	10/14	4500	2.4/500					15	318–08/6
BFR96	10/50	4500	2/500					15	317A/2
BFR90	10/14	5000	2.4/500					15	317A/2
MRF581	10/75	5000	2.7/300		−65		+50	18	317/2
MRF581A	10/75	5000	1.8/500		−65		+50	15	317/2
MRF5812(18a,b)	10/75	5000	1.8/500		−65		+50	15	751/1
LP1001		5000	2.7/500					15	29–04/2
LP1001A		5000	3.2/1000					15	29–04/2
MRF587	15/90	5500	3/500	−52	−72		+50	17	244A/1

(17)PNP

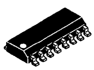
(18)Tape and Reel Packaging Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units.



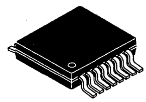
CASE 318A–05
(SOT–143)



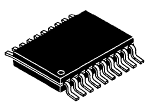
CASE 751
(SO–8)



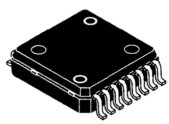
CASE 751B
(SO–16)



CASE 948C
(TSSOP–16)



CASE 948D
(TSSOP–20)



CASE 978
(PFP–16)

Monolithic Integrated Circuits

Motorola's RF monolithic integrated circuit devices provide an integrated solution for the personal communications market. These devices are available in plastic SOIC–8, SOIC–16, SOT–143, TSSOP–16, TSSOP–20 or PFP–16 packages.

Evaluation Boards

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced poduct, please contact your local Motorola Distributor or Sales Office.

RF Monolithic Integrated Circuits

Switching

Antenna Switches

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current μA (Typ)	P_{in}, 1 dB Compression dBm (Typ)	TX Insertion Loss dB (Typ)	Isolation dB (Typ)	Package	System Applicability
MRFIC2003(18b)	100–1000	2.8–6.0	<10	21	0.5	20	SO–8	CT2, ISM
MRFIC1801(18b)	1500–2500	2.7–5.5	300	29	0.6	20	SO–8	DECT, PHS, PCS, ISM
MRFIC0903(18b)★	100–2000	2.7–5.0	60	35.5	0.65	21	SO–8	AMPS, Class 4&5 GSM, DCS1800, PHS, PCS

Receiver Functions

General Purpose Integrated Circuits

General Purpose Cascode Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain @ 900 MHz dB (Typ)	Noise Figure dB (Typ)	Reverse Isolation dB (Typ)	Package	System Applicability
MRFIC0915(18c)★	100–2000	2.7–5.0	2.2	16.5	1.9	44	SOT–143	AMPS,CT1,CT2,GSM,IS–54, ISM,DECT,PHS,PCS
MRFIC0916(18c)★	100–2000	2.7–5.0	4.7	18.5	1.9	44	SOT–143	AMPS,CT1,CT2,GSM,IS–54, ISM,DECT,PHS,PCS

900 MHz Front End

LNA + Mixer

Device	RF Freq. Range MHz	IF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Conv. Gain dB (Typ)	Output Level, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC2001(18b)	500–1000	0–250	2.7–5.0	4.7	23	–10	SO–8	CT2, ISM

1.5 – 2.2 GHz Front End

Integrated LNA

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Noise Figure dB (Typ)	Reverse Isolation dB (Typ)	Package	System Applicability
MRFIC1501(18b)★	1000–2000	3–5	5.7	18	1.1	26	SO–8	DECT, PHS, PCS
MRFIC1808(18b)★	1700–2100	2.7–4.5	4.2	17	1.6	37	SO–8	DECT, PHS, PCS

(18)Tape and Reel Packaging Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units.
★New Product

Receiver Functions: 1.5 – 2.2 GHz Front End (continued)

Integrated LNA/Downconverter

Device	RF Freq. Range GHz	IF Freq. Range GHz	Supply Volt. Range Vdc	Supply Current RX Mode mA (Typ)	Mixer Conv. Gain dB (Typ)	LNA Gain dB (Typ)	LNA Noise Figure dB (Typ)	Package	System Applicability
MRFIC1804(18b)	1.8–1.925	70–325	2.7–3.3	10	4	14	2.3	SO–16	DECT,PHS,PCS
MRFIC1814(18b,46a)	1.8–2.0	70–300	2.7–4.5	10	9	17	2.5	TSSOP–16	DECT,PHS,PCS

2.4 GHz Front End

Integrated LNA/Downconverter

Device	RF Freq. Range MHz	IF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Conv. Gain dB (Typ)	LNA Noise Figure dB (Typ)	Isolation Lo to RF, Lo to IF dB (Typ)	Package	System Applicability
MRFIC2401(18b)	2400–2500	100–350	4.75–5.25	9.5	21	1.9	20	SO–16	WLAN, MMDS, ISM

Transmitter Functions

General Purpose Integrated Circuits

Quadrature Modulator

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Gain Control dB (Typ)	Lo Leakage dBm (Typ)	SSB P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC0001(18b)	50–260	2.7–5.5	10	30	–55	–10	TSSOP–20	DCS1800, GSM, NADC PDC, PHS

General Purpose Cascode Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain @ 900 MHz dB (Typ)	Noise Figure dB (Typ)	Reverse Isolation dB (Typ)	Package	System Applicability
MRFIC0915(18c)★	100–2000	2.7–5.0	2.2	16.5	1.9	44	SOT–143	AMPS,CT1,CT2,GSM,IS–54, ISM,DECT,PHS,PCS
MRFIC0916(18c)★	100–2000	2.7–5.0	4.7	18.5	1.9	44	SOT–143	AMPS,CT1,CT2,GSM,IS–54, ISM,DECT,PHS,PCS

(18)Tape and Reel Packaging Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units.
(46)To be introduced: a) 1st half of 1996; b) 2nd half of 1996.
★ New Product

Transmitter Functions (continued)

900 MHz Transmit Chain

Transmit Mixer

Device	RF Freq. Range MHz	IF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current µA (Typ)	Conv. Gain dB (Typ)	Output Level, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC2002(18b)	500–1000	0–250	2.7–5.0	5.5	0.1	10	–18	SO–8	AMPS,CT1,CT2, GSM, IS–54, ISM
MRFIC2101(18b)	800–1000	0–250	3–4.75	45	2	26.5	4.5	SO–16	AMPS,CT1,CT2, GSM, IS–54, ISM

Driver and Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	Gain Control dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC2004(18b)	800–1000	2.7–4.0	11	0.7	21.5	34	–1	SO–16	AMPS,CT1,CT2, GSM,ISM
MRFIC0904(18b)★	800–1000	2.7–5.0(47)	280	0.05	27	24.5	25.5	SO–16	AMPS,GSM,ISM

Integrated Power Amplifiers

Low Power 900 MHz Power Amplifiers

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Return Loss Input/Output dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	Semiconductor Technology
MRFIC2006(18b)	500–1000	1.8–4.0	46	23	15	15.5	SO–8	Silicon

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	Semiconductor Technology
MRFIC2101(18b)	800–1000	3 – 4.75	38	2	16	18	SO–16	Silicon

Analog Cellular

Device	Freq. Range MHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Min)	Package	Semiconductor Technology
MRFIC0910(18e,46a)	824–905	4.8	50	17.8	–40	30.8/13	PFP–16	LDMOS
MRFIC0911(18e,46a)	824–905	6.8	50	18.5	–35	31.5/13	PFP–16	LDMOS
MRFIC0912(18e,46a)	824–905	4.6(47)	55	21.8	–20	30.8/9	PFP–16	GaAs

(18)Tape and Reel Packaging Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units.
(46)To be introduced: a)1st half of 1996; b) 2nd half of 1996.
(47) Negative supply required
★ New Product

Transmitter Functions: 900 MHz Transmit Chain: Integrated Power Amplifiers (continued)

GSM Cellular

Device	Freq. Range MHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Min)	Package	Semiconductor Technology
MRFIC0913(18e,46a)	880–915	4.8(47)	50	24.5	–30	34.5/10	PFP–16	GaAs
MRFIC0917(18e,46a)	880–915	3.6(47)	50	24.5	–30	34.5/10	PFP–16	GaAs

DCS1800, PCS1900

Device	Freq. Range MHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Min)	Package	Semiconductor Technology
MRFIC1816(18e,46a)	1.5–1.9	5.8(47)	50	16.5	–30	31.5/15	PFP–16	GaAs
MRFIC1818(18e,46a)	1.7–1.9	4.8(47)	35	30	–30	33/3	PFP–16	GaAs

Two–way Paging, ISM

Device	Freq. Range MHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Typ)	Package	Semiconductor Technology
MRFIC0914(18b)★	890–950	4.8	40	28	–45	30.5/2.5	SO–16	LDMOS

1.5 – 2.2 GHz Transmit Chain

UpMixer, Exciter and LO Amp

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc	Supply Current TX Mode mA (Typ)	Standby Current µA (Typ)	Conv. Gain dB (Typ)	Recommended IF Input MHz (Typ)	P_{out}, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC1803(18b)	1.7–2.5	2.7–3.3	28	100	10	70–350	–2	SO–16	DECT,PHS, PCS
MRFIC1813(18b,46a)	1.7–2.5	2.7–4.5	24	25	15	70–350	2	TSSOP–16	DECT,PHS, PCS

PA Driver and RAMP

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc(47)	Supply Current mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	P_{out}/P_{in} dBm (Typ)	1 dB Comp. dBm (Typ)	Pkg	System Applicability
MRFIC1806(18b)	1.5–2.5	3.0–5.0	115	0.25	23	19.5/–3	+21	SO–1 6	DECT,PHS, PCS

(18)Tape and Reel Packaging Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units.
(46)To be introduced: a)1st half of 1996; b) 2nd half of 1996.
(47) Negative supply required
★New Product

Transmitter Functions: 1.5 – 2.2 GHz Transmit Chain (continued)

Power Amplifier and TX/TR Switch

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc	PA Supply Current TX Mode mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	Insertion Loss Rx Mode dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC1807(18b)	1.5–2.2	3.0–5.0	325	0.06	8	1	25	SO–16	DECT, PHS, PCS

UpMixer, Exciter and LO Amp

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc	Supply Current TX Mode mA (Typ)	Standby Current µA (Typ)	Conv. Gain dB (Typ)	Recommended IF Input MHz (Typ)	P_{out}, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC1803(18b)	1.7–2.5	2.7–3.3	28	100	10	70–350	–2	SO–16	DECT,PHS, PCS
MRFIC1813(18b,46a)	1.7–2.5	2.7–4.5	24	25	15	70–350	2	TSSOP–16	DECT,PHS, PCS

2.4 GHz Transmit Chain

Exciter Amplifier

Device	Freq. Range GHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Noise Figure dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC2404(18b)	2.0–3.0	4.75–5.25	9	17	4.3	5	SO–8	WLAN, MMDS, ISM

Power Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Power Control Range dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC2403(18b)	2200–2700	4.75–5.25	95	23	20	19	SO–16	WLAN, MMDS, ISM

UpMixer, Exciter and LO Amp

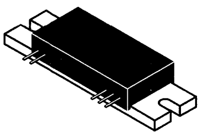
Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc	Supply Current TX Mode mA (Typ)	Standby Current µA (Typ)	Conv. Gain dB (Typ)	Recommended IF Input MHz (Typ)	P_{out}, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC1803(18b)	1.7–2.5	2.7–3.3	28	100	10	70–350	–2	SO–16	DECT,PHS, PCS
MRFIC1813(18b,46a)	1.7–2.5	2.7–4.5	24	25	15	70–350	2	TSSOP–16	DECT,PHS, PCS

(18)Tape and Reel Packaging Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units.
(46)To be introduced: a)1st half of 1996; b) 2nd half of 1996.

RF Amplifiers

Motorola's line of RF amplifiers designed and specified for use in land mobile radios, CATV distribution systems and general purpose wideband amplification applications. They feature small size, matched inputs and outputs, high stability and guaranteed performance specifications. For the user, they offer the benefits of smaller and less complex system designs in less time and at lower overall cost.

Each amplifier uses modern transistor chips which are gold metallized and have silicon nitride passivation for increased reliability and long life. Chip and wire construction features MOS capacitors and laser trimmed nichrome resistors. Circuit substrates and metallization have been selected for optimum performance cost and reliablity.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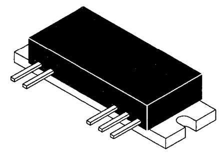
STYLE 1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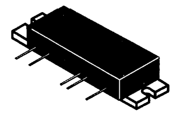
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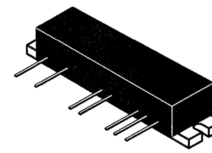
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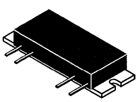
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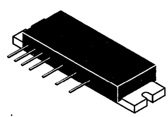
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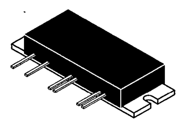
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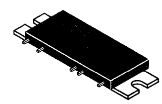
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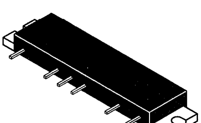
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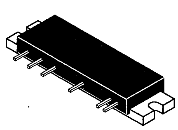
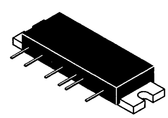

CASE 301T
STYLE 1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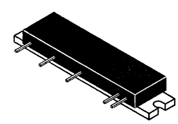
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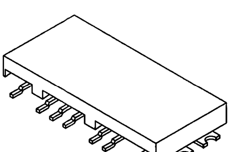
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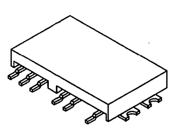
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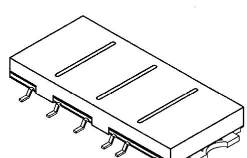
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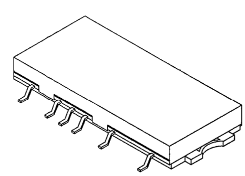
STYLE 1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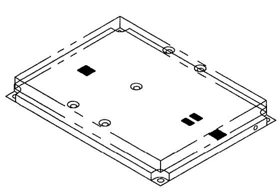
STYLE 1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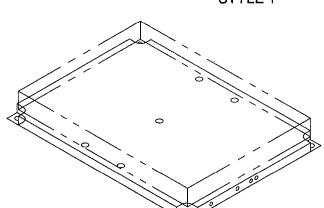
STYLE 1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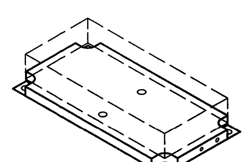
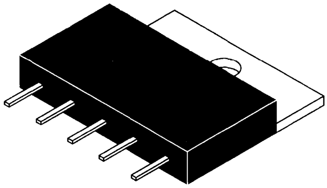
STYLE 1


CASE 429E
STYLE 1



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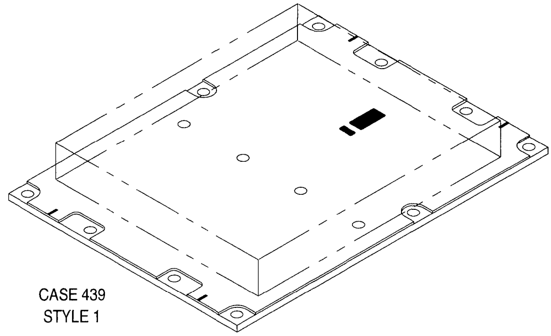
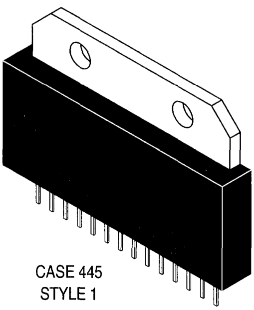
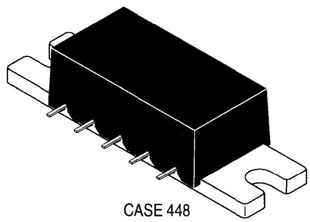


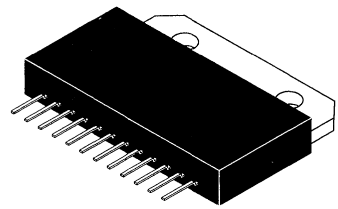
CASE 439
STYLE 1



CASE 445
STYLE 1



CASE 448
STYLE 1, 2



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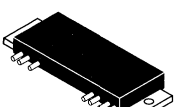

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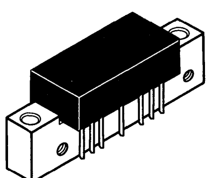

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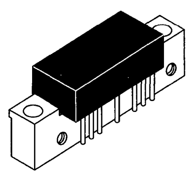

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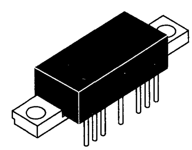
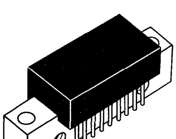
STYLE 1



CASE 714G
STYLE 1



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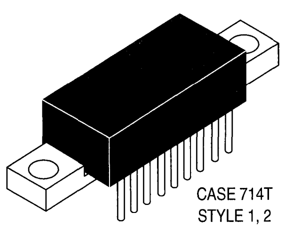
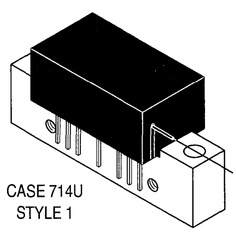
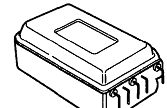
STYLE 2, 3



CASE 714T
STYLE 1, 2



CASE 714U
STYLE 1



CASE 825A
STYLE 2

RF Amplifiers

High Power

Complete amplifiers with 50 ohm in/out impedances are available for a variety of applications including land mobile radios, base stations, TV transmitters and other uses requiring large–signal amplification, both linear and Class C. Frequencies covered range from 68–1785 MHz with power levels extending to 180 watts.

Land Mobile/Portable

The advantages of small size, reproducibility and overall lower cost become more pronounced with increasing frequency of operation. These amplifiers offer a wide range in power levels and gain, with guaranteed performance specifications for bandwidth, stability and ruggedness.

Table 1. VHF/UHF, Class C

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{CC} Supply Voltage Volts	Package/Style
68–210 MHz, VHF Band — Class C (Silicon Bipolar Die)						
MHW105	5	0.001	68–88	37	7.5	301K/3
MHW607–1	7	0.001	136–150	38.4	7.5	301K/3
MHW607–2	7	0.001	146–174	38.4	7.5	301K/3
MHW607–3	7	0.001	174–195	38.4	7.5	301K/3
MHW607–4	7	0.001	184–210	38.4	7.5	301K/3
400–512 MHz, UHF Band — Class C (Silicon Bipolar Die)						
MHW704–1	3	0.001	400 – 440	34.8	6.0	301J/1
MHW704–2	3	0.001	440 – 470	34.8	6.0	301J/1
MHW707–1	7	0.001	403 – 440	38.4	7.5	301J/1
MHW707–2	7	0.001	440 – 470	38.4	7.5	301J/1
MHW707–3	7	0.001	470 – 500	38.4	7.5	301J/1
MHW707–4	7(23)	0.001	490 – 512	38.4(23)	7.5	301J/1
MHW720A1(22)	20	0.15	400 – 440	21	12.5	700/2
MHW720A2(22)	20	0.15	440 – 470	21	12.5	700/2
806–960 MHz, UHF Band — Class C (Silicon Bipolar Die)						
MHW851–1	1.6	0.001	820–850	32	6	301N/1
MHW851–2	1.6	0.001	870–905	32	6	301N/1
MHW851–3	2	0.001	890–915	33	6	301N/1
MHW851–4	1.6	0.001	915–925	32	6	301N/1
MHW803–1	2	0.001	820–850	33	7.5	301E/1
MHW803–2	2	0.001	806–870	33	7.5	301E/1
MHW803–3	2	0.001	870–905	33	7.5	301E/1
MHW804–1	4	0.001	800–870	36	7.5	301F/1
MHW806A2(22)	6	0.03	806–870	23	12.5	301H/2
MHW806A4(22)	6	0.04	870–950	21.7	12.5	301H/2
806 – 960 MHz, UHF Band — (LDMOS Die)						
MHW2821–1★	20	<0.250	806–870	19	12.5	301AB/1
MHW2821–2★	18	<0.300	890–950	17.9	12.5	301AB/1
824 – 915 MHz, UHF Band — Class C (GaAs FET Die)						
MHW9002–1(22)	1.4	0.005	824–849	24.5	5.8	420A/1
MHW9002–2(22)	1.4	0.005	870–905	24.5	5.8	420A/1
1710 – 1785 MHz, UHF Band — (GaAs FET Die)						
MHW9014★	2.1	0.001	1710–1785	33.2	6.0	420/1

(22)Designed for Wide Range P_{out} Level Control
(23)P_o @ f = 490 MHz. P_o = 6.5 W @ f = 512 MHz
★ New Product

Table 2. UHF, Linear

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{CC} Supply Voltage Volts	Package/Style
824–849 MHz, UHF Band — Class AB (Silicon Bipolar Die)						
MHW920★	0.8(24)	0.001	824–849	29	6	420U/1
MHW927B(22)	6(24)	0.001	824–849	37.8	12.5	301AA/1
880–960 MHz (for GSM) — Class AB (Silicon Bipolar Die)						
MHW953(22)	3.5	0.001	890–915	35.4	7.2	301V/1
MHW954(22)	3.5	0.1	890–915	15.4	7.2	301Y/1
880–960 MHz (for GSM) — Class AB (LDMOS Silicon FET)						
MHW913	14	0.1	880–915	21.5	12.5	301AB/1
MHW914(22)	14	0.001	890–915	41.4	12.5	301R/1
MHW916	16	0.036	925–960	26.5	26	301AB/1

TV Transmitters

Table 3. UHF Ultra Linear for TV Applications

These amplifiers are characterized for ultra–linear applications in Band IV and Band V TV transmitters.

Device	Frequency MHz	P_{ref} Watts	Gp (Min)/Freq. Power Gain dB/MHz	3 Tone(8) IMD 1 dB	3 Tone(25) IMD 2 dB	V_{CC} Volts	Class	Package/Style
MRFA2600(26)	470–860	20	10.5/860	–50	–53	26.5	A	429A/1
MRFA2602(28)	470–860	40	9/860	–50	–53	25.5	A	429C/1
RFA8090B	470–860	95(11)	8/860	—	—	28	AB	429E/1
MRFA2604★	470–860	180(11)	8/860	—	—	28	AB	439/1

(8)Vision Carrier: – 8 dB; Sound Carrier: – 7 dB; Sideband Carrier: – 16 dB
(11)Output power at 1 dB compression in Class AB
(22)Designed for Wide Range P_{out} Level Control
(24)Average Power; Peak Power is twice average power
(25)Vision Carrier: – 8 dB; Sound Carrier: – 10 dB; Sideband Carrier: – 16 dB
(26)Formerly known as “RFA6031”
(28)Formerly known as “RFA6060”
★New Product

Low Power

The following categories describe a wide range of complete amplifier assemblies both hybrid and monolithic for use in CATV distribution systems, instrumentation, communications and military equipment. A variety of power levels and frequencies of operation is offered for many applications.

CATV Distribution

Motorola Hybrids are manufactured using the latest generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels.

Table 1. 5–50 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	I_{DC} mA Max	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test(30) dB	Composite Triple Beat dB 4 CH	Cross Modulation dB 4 CH	Noise Figure @ 50 MHz dB Max	Package/ Style
Low Current Amplifiers									
MHW1184L	18	4	135	+50	–70	–73	–64	5	714/1
MHW1224L	22	4	135	+50	–70	–72	–63	5	714/1
MHW1254L	25	4	135	+50	–70	–70	–62	4.5	714/1
MHW1304L	30	4	135	+50	–70	–66	–57	4.5	714/1

Table 2. 5–200 MHz Hybrids, V_{CC} = 12 Vdc, Class A

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	Maximum Distortion Specifications: 2nd Order Test(48) dB	2nd Order Test(49) dB	2nd Order Test(50) dB	Composite Triple Beat(51) dB (Typ) 22 CH	Composite Triple Beat(51) dB (Typ) 26 CH	Triple Beat dB Typ	Noise Figure @ 200 MHz dB Max	Package/ Style
MHW1254LC(46a)	24.8	22	–68(19)	–59(19)	–57(19)	–69	–66	–71	5.0	431A/1
MHW1304LC(46a)	29.8	22	–68(19)	–59(19)	–57(19)	–71	–67	–71	5.0	431A/1

Table 3. 5–200 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test(30) dB	Composite Triple Beat dB 22 CH	Composite Triple Beat dB 26 CH	Cross Modulation dB 22 CH	Cross Modulation dB 26 CH	Noise Figure @ 175 MHz dB Max	Package/ Style
High–Split Reverse Amplifiers										
MHW1134	13	22	+50	–72	–73	–71(19)	–65	–65(19)	7	714/1
MHW1184	18	22	+50	–72	–70	–70(19)	–64	–64(19)	5.5	714/1
MHW1224	22	22	+50	–72	–69	–68.5(19)	–62	–62(19)	5.5	714/1
MHW1244	24	22	+50	–72	–68	–67.5(19)	–61	–61(19)	5	714/1

(19)Typical
(30)Channels 2 and A @ 7
(46)To be introduced: a)1st half of 1996; b) 2nd half of 1996.
(48)12 MHz and 43.25 MHz @ 55.25 MHz, V_{out} = 50 dBmV/ch
(49)54 MHz and 121.25 MHz @ 175.25 MHz, V_{out} = 50 dBmV/ch
(50)54 MHz and 145.25 MHz @ 199.25 MHz, V_{out} = 50 dBmV/ch
(51)44 dBmV/ch

Low Power: CATV Distribution (continued)

Table 4. 40–450 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 60 CH	Cross Modulation dB 60 CH	Noise Figure @ 450 MHz dB Max	Package/ Style
Conventional Hybrids								
MHW5142A	14	60	+46	–74(31)	–61	–62	7	714/1
MHW5172A	17	60	+46	–74(31)	–60	–62	7	714/1
MHW5182A	18	60	+46	–72(31)	–61	–59	6.5	714/1
MHW5222A	22	60	+46	–72(31)	–60	–59	5.5	714/1
MHW5272A	27	60	+46	–68(31)	–59	–60	6.0	714/1
MHW5342A	34	60	+46	–68(31)	–59	–59	6.0	714/1
MHW5382A	38	60	+46	–64(31)	–59	–59	5.0	714/1
Power Doubling Hybrids								
MHW5185B	18	60	+46	–67(32)	–67	–67	7.0	714/1
MHW5225	22	60	+46	–69(31)	–62	–62	6.0	714/1
Feedforward Hybrids								
MFF124B	24	60	+46	–84(31)	–79	–75	10	825A/2

Table 5. 40–550 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 77 CH	Composite Triple Beat dB 87 CH	Cross Modulation dB 77 CH	Cross Modulation dB 87 CH	Noise Figure @ 550 MHz dB Max	Package/ Style
Conventional Hybrids										
MHW6142	14	77	+44	–72(35)	–59	—	–62	—	7.5	714/1
MHW6172	17	77	+44	–72(35)	–59	—	–62	—	7	714/1
MHW6182	18	77	+44	–72(35)	–58	—	–62	—	7	714/1
MHW6222	22	77	+44	–66(35)	–57	—	–57	—	6	714/1
MHW6272	27	77	+44	–64(35)	–57	—	–57	—	6.5	714/1
MHW6342	34	77	+44	–64(35)	–57	—	–57	—	6.5	714/1
Power Doubling Hybrids										
MHW6185B	18	77	+44	–65(36)	–65	—	–68	—	7.5	714/1
MHW6205	20	77	+44	–60(36)	–64	—	–67	—	7.5	714/1
MHW6225	22	77	+44	–55(36)	–62	—	–60	—	7.0	714/1
Feedforward Hybrids										
MFF224B	24	77	+44	–86(35)	–75	—	–70	—	11	825A/2

(31)Channels 2 and M13 @ M22
(32)Composite 2nd order; V_{out} = +46 dBmV/ch
(35)Channels 2 and M30 @ M39
(36)Composite 2nd order; V_{out} = +44 dBmV/ch

Low Power: CATV Distribution (continued)

Table 6. 40–600 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 85 CH	Composite Triple Beat dB 87 CH	Cross Modulation dB 85 CH	Cross Modulation dB 87 CH	Noise Figure @ 600 MHz dB Max	Package/ Style
Conventional Hybrids										
MHW6182–6	18	87	+44	–56(36)	—	–57	—	–55	6	714/1
MHW6222–6	22	87	+44	–56(36)	—	–56	—	–56	6	714/1
MHW6272–6(46a)	27	87	+44	–63(36)	—	–57	—	–55	6.5	714/1
MHW6292–6(46a)	29	87	+44	–63(36)	—	–57	—	–55	6.5	714/1
Power Doubling Hybrids										
MHW6185–6A★	18	87	+44	–64(36)	—	–64	—	–66	7	714/1
MHW6205–6A★	20	87	+44	–63(36)	—	–63	—	–65	6.5	714/1
Feedforward Hybrids										
MFF324B	24	85	+44	–86(38)	–73	—	–68	—	12.5	825A/2

Table 7. 40–750 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 110 CH	Composite Triple Beat dB 128 CH	Cross Modulation dB 110 CH	Cross Modulation dB 128 CH	Noise Figure @ 750 MHz dB Max	Package/ Style
Conventional Hybrids										
MHW7142	14	110	+40	–60(39)	– 62	—	– 66	—	8.0	714/1
MHW7182	18	110	+40	–62(39)	– 62	—	– 64	—	6.5	714/1
MHW7222	22	110	+40	–55(39)	– 60	—	– 60	—	7	714/1
MHW7242★	24	110	+40	–60(39)	– 60	—	– 60	—	7	714/1
MHW7272★	27	110	+40	–60(39)	– 60	—	– 60	—	6.5	714/1
MHW7292★	29	110	+40	–60(39)	– 60	—	– 60	—	6.5	714/1

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 110 CH	Cross Modulation dB 110 CH	Noise Figure @ 750 MHz dB Max	Package/ Style
Power Doublers								
MHW7185A★	18.5	110	+44	–58(36)	–58	–65	8.5	714/1
MHW7205A★	20	110	+44	–56(36)	–57	–64	8.0	714/1
Feed Forward Hybrids								
MFF424B★	24	110	+44	–70(36)	–65(36)	—	13	825A/2

(36)Composite 2nd order; V_{out} = +44 dBmV/ch
(38)Channels 2 and M39 @ M48
(39)Composite 2nd order; V_{out} = +40 dBmV/ch
(46)To be introduced: a)1st half of 1996; b) 2nd half of 1996.
★New Product

Low Power: CATV Distribution (continued)

Table 8. 40–860 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 110 CH	Composite Triple Beat dB 128 CH	Cross Modulation dB 110 CH	Cross Modulation dB 128 CH	Noise Figure @ 860 MHz dB Max	Package/ Style
Conventional Hybrids										
MHW8142	14	128	+38	–60[40]	—	– 61	—	– 66	8.0	714/1
MHW8182	18	128	+38	–60[40]	—	– 60	—	– 60	7	714/1
MHW8222	22	128	+38	–60[40]	—	– 60	—	– 60	7.5	714/1
MHW8242★	24	128	+38	–60[40]	—	– 60	—	– 60	7.5	714/1
MHW8272★	27	128	+38	–60[40]	—	– 60	—	– 60	7.0	714/1
MHW8292★	29	128	+38	–56[40]	—	– 60	—	– 60	7.0	714/1
Power Doubling Hybrids										
MHW8185[46b]	18.5	128	+40	–60[39]	—	– 62	—	– 65	8.5	714/1
MHW8205[46b]	20	128	+40	–60[39]	—	– 61	—	– 65	8.5	714/1
Feedforward Hybrids										
MFF524B[46a]	24	128	+40	–70[39]	—	– 70	—	—	12.0	825A/2

Table 9. 40–860 MHz Hybrids

Device	Gain dB Typ	Frequency MHz	V_{CC} Volts	2nd Order IMD @ V_{out} = 50 dBmV/ch Max	DIN45004B @ f=860 MHz dBμV Min	Noise Figure @ 860 MHz dB Max	Package/ Style
Conventional Hybrids							
CA901	17	40 – 860	24	–60	120	8	714P/2
CA901A	17	40 – 860	24	–64	120	8	714P/2
Power Doubling Hybrids							
CA922	17	40 – 860	24	–63	123	9.5	714P/2
CA922A	17	40 – 860	24	–67	123	9.5	714P/2
Hybrid Jumper							
CATHRU	0	1 – 1000	75 Ohm Broadband Hybrid Jumper				714V

Table 10. 40/1000 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 152 CH	Cross Modulation dB 152 CH	Noise Figure @ 860 MHz dB Max	Package/ Style
Conventional Hybrids								
MHW9142	14	152	+38	–59[40]	–59	–63	8.5	714/1
MHW9182	18	152	+38	–59[40]	–59	–59	8.0	714/1
MHW9242[46a]	24	152	+38	–59[40]	–58	–59	8	714/1

(39)Composite 2nd order; V_{out} = +40 dBmV/ch

(40)Composite 2nd Order; V_{out} = +38 dBmV/ch

(46)To be introduced: a)1st half of 1996; b) 2nd half of 1996.

★ New Product

Low Power: CATV Distribution (continued)

Table 11. General Purpose Wideband Amplifiers

Device	Frequency Range MHz	Gain Min/Typ dB	Supply Voltage Vdc	Output Level 1 dB Compression MW/@ MHz	Noise Figure @ 250 MHz dB	Package/ Style
50–100 Ω Hybrids						
MHW591	1 – 250	34.5/36.5	13.6	700/100	5	714/1
MHW592	1 – 250	33.5/35	24	900/100	5	714/1
MHW593	10 – 400	33/34.5	13.6	600/200	5	714/1
MHW590	10 – 400	31.5/34	24	800/200	5	714/1

Table 12. Standard Linear Hybrids

This series of RF linear hybrid amplifiers have been optimized for wideband, 50 ohm applications. These amplifiers were designed for multi–purpose RF applications where linearity, dynamic range and wide bandwidth are of primary concern. Each amplifier is available in various package options. The MHL series utilizes a new case style that provides microstrip input and output connections.

Device	V_{CC} (Nom.) Volts	BW MHz	Gain Flatness Typ ±dB	Gain/Freq. Typ dB/MHz	P_{1dB} Typ dBm	NF/Freq. Typ dB/MHz	3rd Order Intercept Point/Freq. Typ dBm/MHz	VSWR Max 50 Ω	V_S/I_S Typ V/mA	Case/ Style
CA4812C(41)	12	10–1000	1	17.5/1000	26	7.5/1000	38/1000	2.6	12/380	714P/3
CA5815C(41)	15	10–1000	1	15.5/1000	30	8.5/1000	40.5/1000	2.6	15/700	714P/3
CA4815C(41)	15	10–1000	1	17.5/1000	26	7.5/1000	38/1000	2.6	15/380	714P/3
MHL8015★	15	10–1000	1	18.5/900	26	7.5/1000	38/1000	2.6	15/380	448/2
MHL8115★	15	10–1000	1	17.5/900	30	8.5/1000	41.5/1000	2.6	15/700	448/2
MHL9125★	15	800–960	0.5	20/900	31	7.5/960	43/879	1.5	15/700	448/2
CA2830C	24	5–200	0.5	34.5/100	29	4.7/200	46/200	2	24/300	714F/1
CA2833C	24	5–200	0.5	34.5/100	29	4.7/200	46/200	2	24/300	714G/1
CA2842C	24	10–400	0.5	22/100	32	4/100	44/300	1.5	24/230	714F/1
CA2810C	24	10–450	1.5	34/50	30	5/300	43/300	2	24/310	714F/1
CA2818C	24	10–400	0.5	18.5/50	30	5/200	45/200	2	24/205	714F/1
CA4800C(41)	24	10–1000	1	17.5/1000	26	7.5/1000	38/1000	2.6	24/220	714P/2
CA2832C	28	1–200	0.5	35.5/100	33	5/200	47/200	2	28/435	714F/1
CA5800C(41)	28	10–1000	1	15.5/1000	30	8.5/1000	40.5/1000	2.6	28/400	714P/2
CA5801(41)	28	50– 1000	1	17.5/1000	30	8.5/1000	41.5/1000	2.6	28/400	714P/2
MHL8018★	28	10–1000	1	18.5/900	26	7.5/1000	38/1000	2.6	28/400	448/1
MHL8118★	28	10–1000	1	17.5/900	30	8.5/1000	38/1000	2.6	28/200	448/1
MHL9128★	28	800–960	0.5	20/900	31	7.5/960	43/879	1.5	28/400	448/1

(41)Available in thin flange package (714T) by adding suffix "S" after part number, i.e. CA4800CS.

★New Product

CRT Drivers

Table 1. Video Amplifiers

These complete hybrid amplifiers are specifically designed for CRT driver applications requiring high frequency response and high voltage, such as high resolution color graphics video monitors. Gold metallized die and substrates are used to ensure high reliability and improved ruggedness.

Device	V_{CC}(nom) Volts	Gain(42) (Typ) V/V	t_r/t_f (Typ)(43) nsec	3 dB BW (Typ)(43) MHz	Video Clock Freq. MHz	V_{out} (Max) Volts	Load	Package/Style
CR2428	60	12	2.0	145	290	50 P–P	6 to 20 pF	431A/1
MHW2528(45)★	60	12	2.8	100	200	50 P–P	6 to 20 pF	445/1
MHW2728(45)★	60	12	3.0	100	200	50 P–P	6 to 20 pF	455/1
MHW3628(45)★	70	12	2.7	120	240	60 P–P	6 to 20 pF	455/1
CR3428	80	12	2.2	130	260	70 P–P	6 to 20 pF	431A/1
MHW3528(45)★	80	12	2.7	120	240	70 P–P	6 to 20 pF	445/1
MHW3728(45)★	80	12	2.5	120	240	70 P–P	6 to 20 pF	455/1

Fiber Optic Receivers

Table 1. 40–860 MHz Hybrids

Device	Hybrid Responsivity Min dB	Flatness dB	Maximum Distortion Specifications IMD 2(52) dB	IMD 3(52) dB	Equivalent Input Noise pA/$\sqrt{Hz}$ Max	Package/ Style
Fiber Optic Receiver Hybrids						
MHLW8000(46b)	23.5	± 0.5	–70	–80	7.5	714U/1

(42)Insertion Gain; 50 Ω Source

(43)Capacitive Load 8.5 pF, Vout = 40 V P-P

(45)Triple Video Amplifiers

(46)To be introduced: a)1st half of 1996; b) 2nd half of 1996.

(52)Two laser test with 0.5 mW optical power at 40% modulation index per lase; f1 = 373.25 MHz f2 = 415.25 MHz

★New Product

Surface Mount Information

In Brief . . .

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the state–of–the–art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that is common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

INFORMATION FOR USING SURFACE MOUNT PACKAGES

RECOMMENDED FOOTPRINTS FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain/collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For example, for a SOT–223 device, P_D is calculated as follows.

$$P_D = \frac{150°C - 25°C}{156°C/W} = 800 \text{ milliwatts}$$

The 156°C/W for the SOT–223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 800 milliwatts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain/collector pad. By increasing the area of the drain/collector pad, the power dissipation can be increased. Although the power dissipation can almost be doubled with this method, area is taken up on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figures 1, 2 and 3.

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

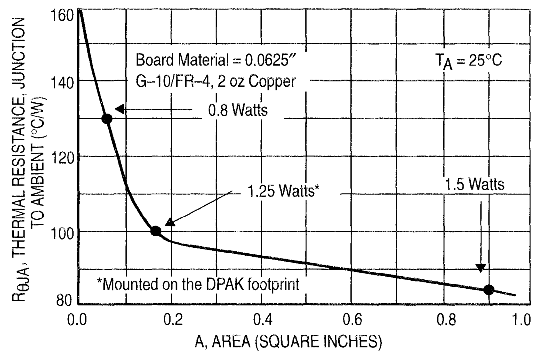


Figure 1. Thermal Resistance versus Drain Pad Area for the SOT–223 Package (Typical)

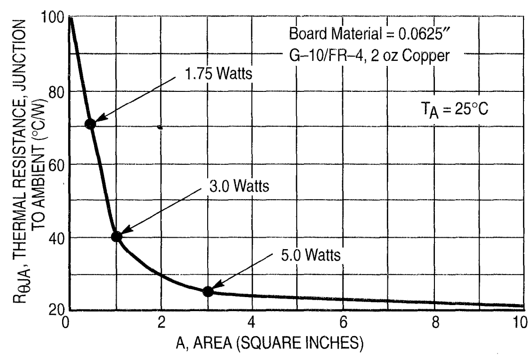


Figure 2. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)

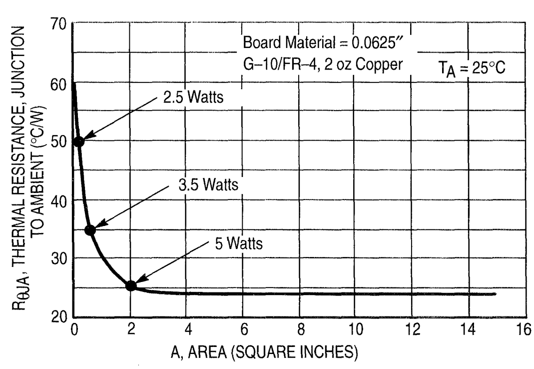


Figure 3. Thermal Resistance versus Drain Pad Area for the D^2PAK Package (Typical)

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, Micro8, and SMA/SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK, D^2PAK and D^3PAK packages. If a 1:1 opening is used to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 4 shows a typical stencil for the DPAK, D^2PAK and D^3PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

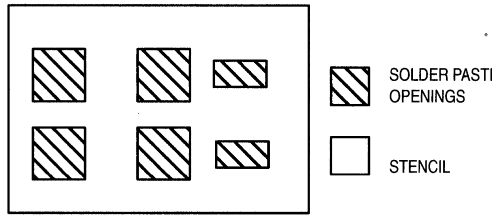


Figure 4. Typical Stencil for DPAK, D^2PAK and D^3PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used since the use of forced cooling will increase the temperature gradient and will result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^2PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 5 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

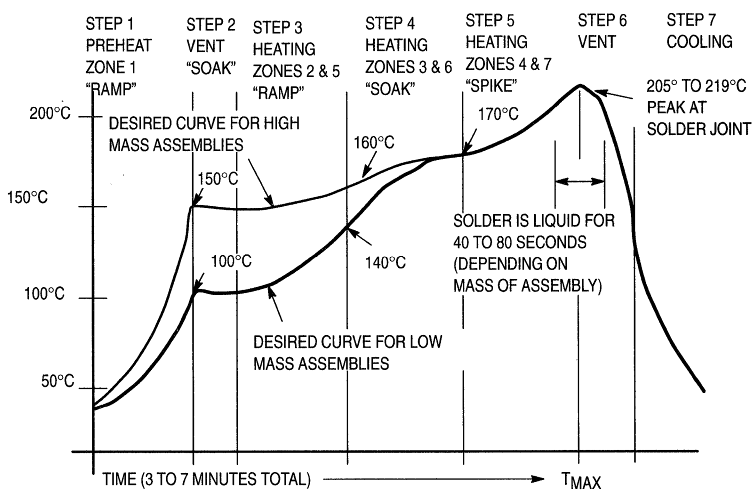
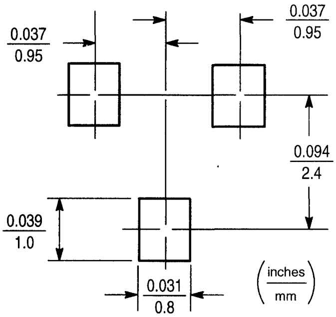
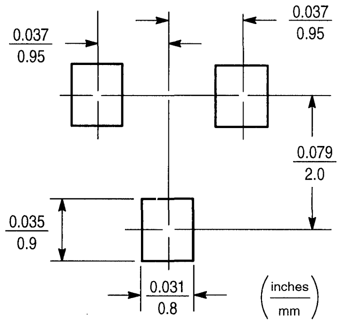


Figure 5. Typical Solder Heating Profile

Footprints for Soldering

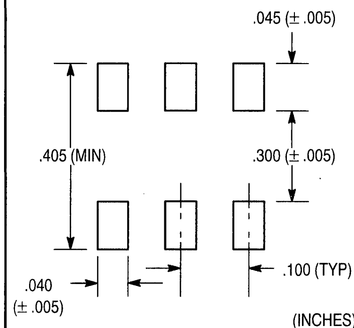


SC–59

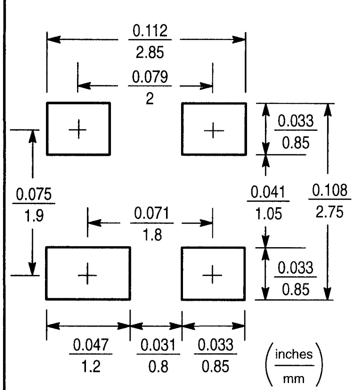


SOT–23

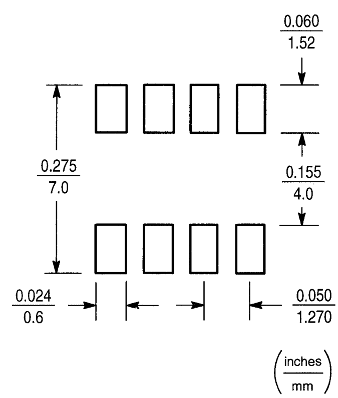
6–PIN DIP
GULL–WING



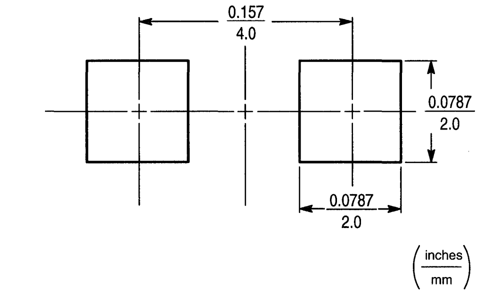
Standard "S" Option



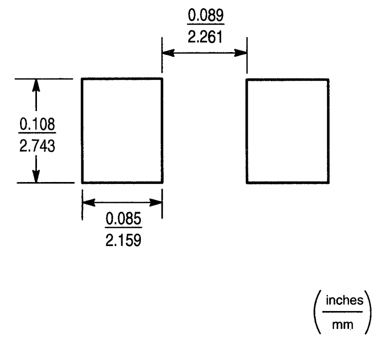
SOT–143



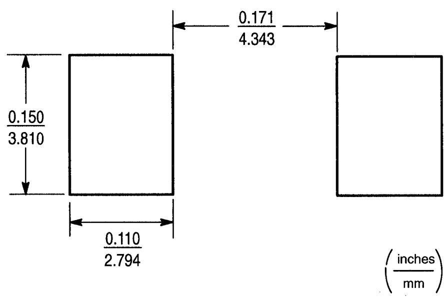
SO–8, OPTO SO–8,
SO–14, SO–16



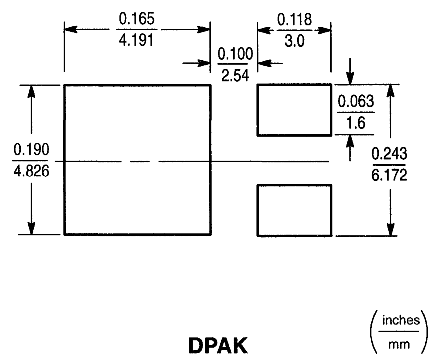
SMA



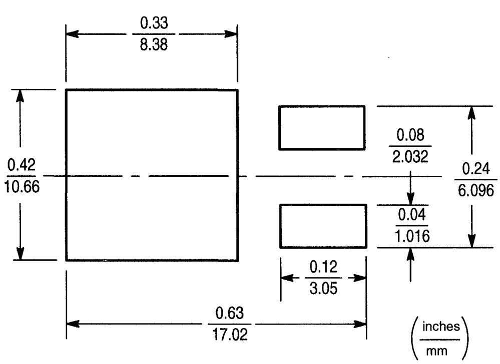
SMB



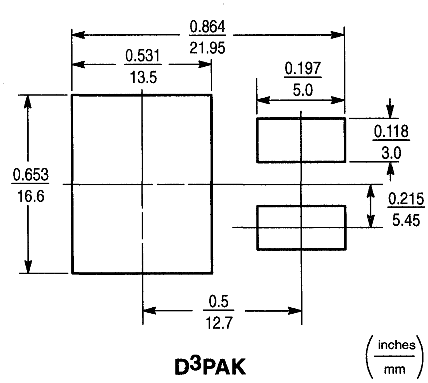
SMC



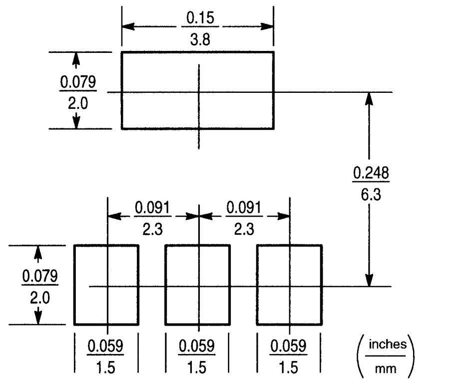
DPAK



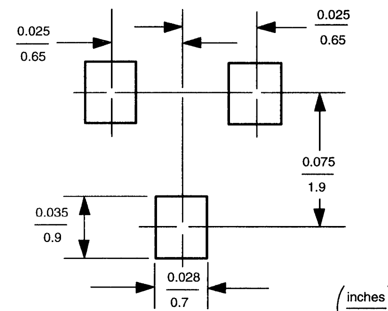
D²PAK



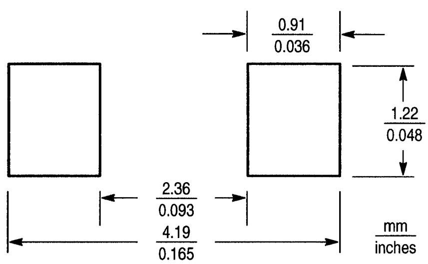
D³PAK



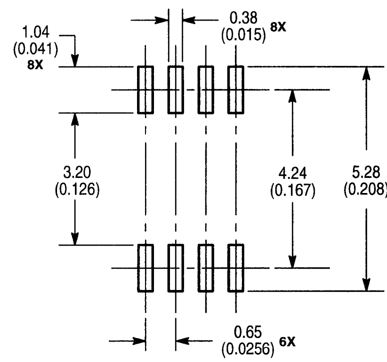
SOT–223



SC–70/SOT–323



SOD–123



MICRO8

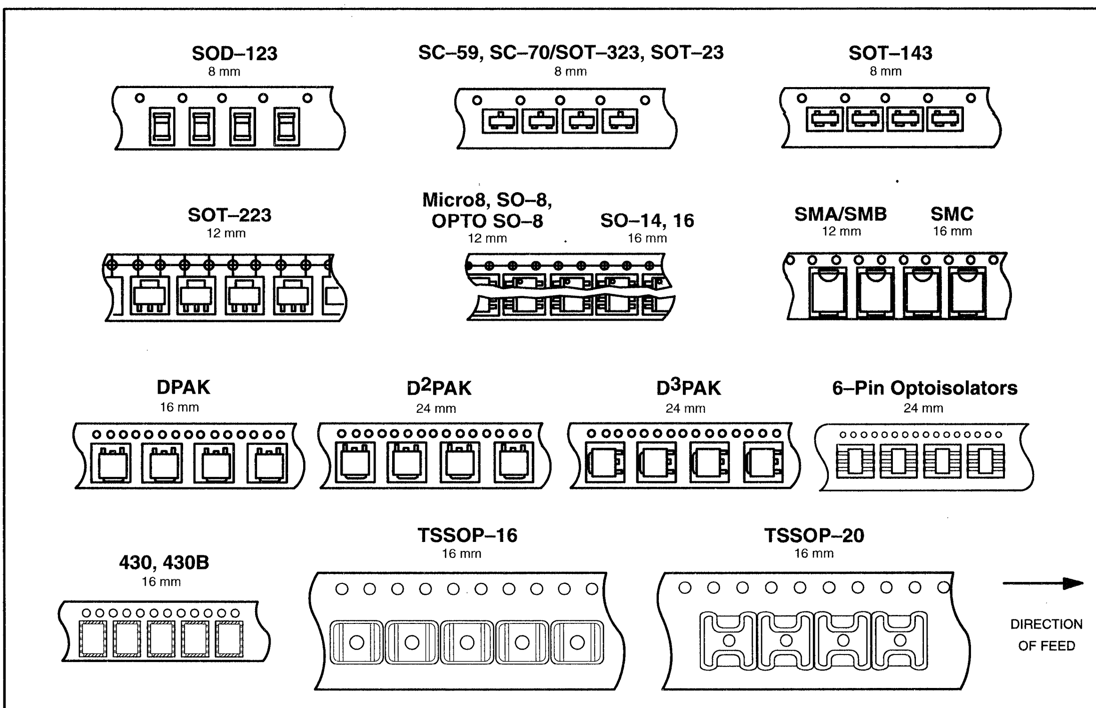
Tape and Reel Specifications and Packaging Specifications

Tape and Reel Specifications and Packaging Specifications

Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the "peel–back" cover tape.

- Two Reel Sizes Available (7″ and 13″)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, –1, –2
- SOD–123, SC–59, SC–70/SOT–323, SOT–23, SOT–143 in 8 mm Tape
- SO–8, Micro8, OPTO SO–8, SOT–223, SMA, SMB in 12 mm Tape
- DPAK, PFP–16, SO–14, SO–16, SMC, TSSOP–16, TSSOP–20, 430 and 430B in 16 mm Tape
- D^{2}PAK, D^{3}PAK, 6–Pin Optoisolators in 24 mm Tape

Use the standard device title and add the required suffix as listed in the option table on the following page. Note that the individual reels have a finite number of devices depending on the type of product contained in the tape. Also note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.

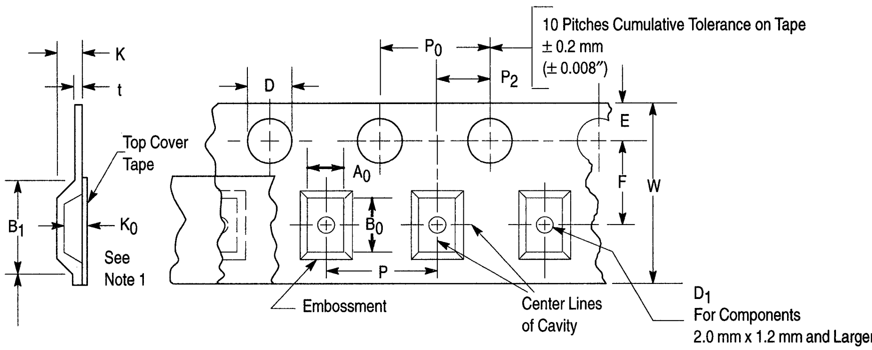


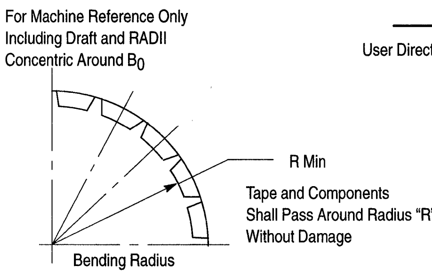
EMBOSSED TAPE AND REEL ORDERING INFORMATION

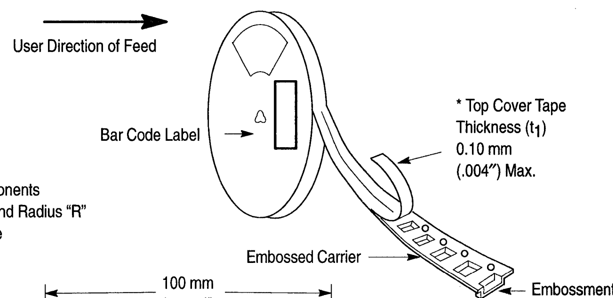
Package	Tape Width (mm)	Pitch mm (inch)	Reel Size mm (inch)	Devices Per Reel and Minimum Order Quantity	Device Suffix
DPAK	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	T4
D^2PAK	24	16.0 ± 0.1 (.630 ± .004)	330 (13)	800	T4
D^3PAK	24	24.0 ± 0.1 (.945 ± .004)	330 (13)	500	RL
SC–59	8	4.0 ± 0.1 (.157 ± .004)	178 (7)	3,000	T1
SC–70/SOT–323	8 8	4.0 ± 0.1 (.157 ± .004)	178 (7) 330 (13)	3,000 10,000	T1 T3
SMA	12	8.0 ± 0.1 (.315 ± .004)	330 (13)	5,000	T3
SMB	12	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	T3
SMC	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	T3
SO–8, OPTO SO–8	12 12	8.0 ± 0.1 (.315 ± .004)	178 (7) 330 (13)	500 2,500	R1 R2
SO–14	16 16	8.0 ± 0.1 (.315 ± .004)	178 (7) 330 (13)	500 2,500	R1 R2
SO–16	16 16	8.0 ± 0.1 (.315 ± .004)	178 (7) 330 (13)	500 2,500	R1 R2
SOD–123	8 8	4.0 ± 0.1 (.157 ± .004)	178 (7) 330 (13)	3,000 10,000	T1 T3
SOT–23	8 8	4.0 ± 0.1 (.157 ± .004)	178 (7) 330 (13)	3,000 10,000	T1 T3
SOT–143	8 8	4.0 ± 0.1 (.157 ± .004)	178 (7) 330 (13)	3,000 10,000	T1 T3
SOT–223	12 12	8.0 ± 0.1 (.315 ± .004)	178 (7) 330 (13)	1,000 4,000	T1 T3
6–Pin Optoisolators	24	12.0 ± 0.1 (.472 ± .004)	330 (13)	1000	R2
Micro8	12	8.0 ± 0.1 (.315 ± .003)	330 (13)	4000	R2
PFP–16	16	12.0 ± 0.1 (.471 ± .004)	330 (13)	1,500	R2
TSSOP–16	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
TSSOP–20	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
430, 430B	16	8.0 ± 0.1 (.315 ± .004)	178 (7)	500	R1

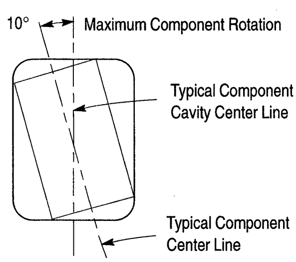
EMBOSSED TAPE AND REEL DATA FOR DISCRETES

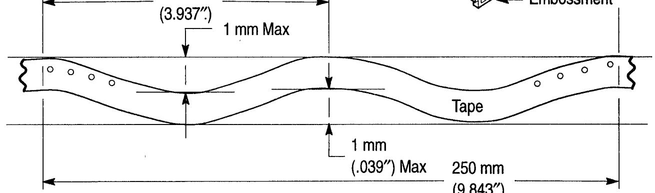
CARRIER TAPE SPECIFICATIONS











Camber (Top View)
Allowable Camber To Be 1 mm/100 mm Nonaccumulative Over 250 mm

DIMENSIONS

Tape Size	B_1 Max	D	D_1	E	F	K	P_0	P_2	R Min	T Max	W Max
8 mm	4.55 mm (.179″)	1.5 + 0.1 mm −0.0 (.059 + .004″ −0.0)	1.0 Min (.039″)	1.75 ± 0.1 mm (.069 ± .004″)	3.5 ± 0.05 mm (.138 ± .002″)	2.4 mm Max (.094″)	4.0 ± 0.1 mm (.157 ± .004″)	2.0 ± 0.1 mm (.079 ± .002″)	25 mm (.98″)	0.6 mm (.024″)	8.3 mm (.327″)
12 mm	8.2 mm (.323″)		1.5 mm Min (.060″)		5.5 ± 0.05 mm (.217 ± .002″)	6.4 mm Max (.252″)			30 mm (1.18″)		12 ± .30 mm (.470 ± .012″)
16 mm	12.1 mm (.476″)				7.5 ± 0.10 mm (.295 ± .004″)	7.9 mm Max (.311″)					16.3 mm (.642″)
24 mm	20.1 mm (.791″)				11.5 ± 0.1 mm (.453 ± .004″)	11.9 mm Max (.468″)					24.3 mm (.957″)

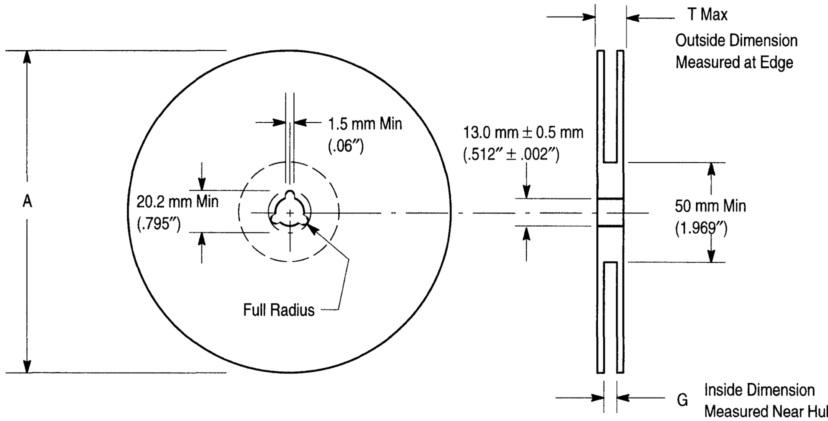
Metric dimensions govern — English are in parentheses for reference only.

NOTE 1: A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within .05 mm min. to .50 mm max., the component cannot rotate more than 10° within the determined cavity.

NOTE 2: If B_1 exceeds 4.2 mm (.165) for 8 mm embossed tape, the tape may not feed through all tape feeders.

NOTE 3: Pitch information is contained in the Embossed Tape and Reel Ordering Information on pg. 5.12–3.

EMBOSSED TAPE AND REEL DATA FOR DISCRETES



Size	A Max	G	T Max
8 mm	330 mm (12.992″)	8.4 mm + 1.5 mm, −0.0 (.33″ + .059″, −0.00)	14.4 mm (.56″)
12 mm	330 mm (12.992″)	12.4 mm + 2.0 mm, −0.0 (.49″ + .079″, −0.00)	18.4 mm (.72″)
16 mm	360 mm (14.173″)	16.4 mm + 2.0 mm, −0.0 (.646″ + .078″, −0.00)	22.4 mm (.882″)
24 mm	360 mm (14.173″)	24.4 mm + 2.0 mm, −0.0 (.961″ + .070″, −0.00)	30.4 mm (1.197″)

Reel Dimensions

Metric Dimensions Govern — English are in parentheses for reference only

LEAD TAPE PACKAGING STANDARDS FOR AXIAL–LEAD COMPONENTS

Case Type	Product Category	Device Title Suffix	MPQ Quantity Per Reel (Item 3.3.7)	Component Spacing A Dimension	Tape Spacing B Dimension	Reel Dimension C	Reel Dimension D (Max)	Max Off Alignment E
Case 17–02	Surmetic 40 & 600 Watt TVS	RL	4000	0.2 +/– 0.015	2.062 +/– 0.059	3	14	0.047
Case 41A–02	1500 Watt TVS	RL4	1500	0.4 +/– 0.02	2.062 +/– 0.059	3	14	0.047
Case 51–02	DO–7 Glass (For Reference only)	RL	3000	0.2 +/– 0.02	2.062 +/– 0.059	3	14	0.047
Case 59–03	DO–41 Glass & DO–41 Surmetic 30	RL	6000	0.2 +/– 0.015	2.062 +/– 0.059	3	14	0.047
	Rectifier							
Case 59–04	500 Watt TVS	RL	5000	0.2 +/– 0.02	2.062 +/– 0.059	3	14	0.047
	Rectifier							
Case 194–04	110 Amp TVS (Automotive)	RL	800	0.4 +/– 0.02	1.875 +/– 0.059	3	14	0.047
	Rectifier							
Case 267–02	Rectifier	RL	1500	0.4 +/– 0.02	2.062 +/– 0.059	3	14	0.047
Case 299–02	DO–35 Glass	RL	5000	0.2 +/– 0.02	2.062 +/– 0.059	3	14	0.047

Table 1. Packaging Details (all dimensions in inches)

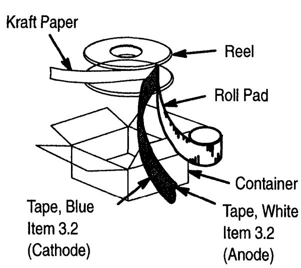


Figure 1. Reel Packing

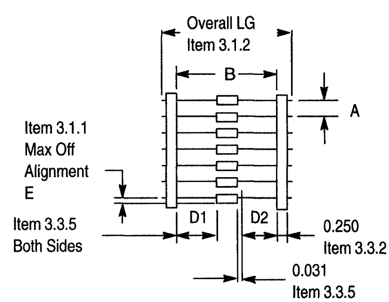


Figure 2. Component Spacing

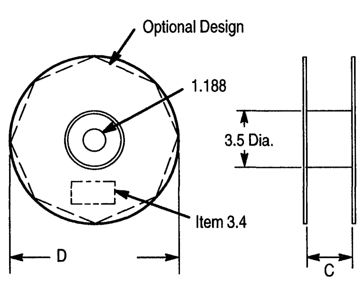


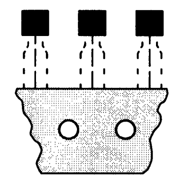
Figure 3. Reel Dimensions

TO–92 EIA, IEC, EIAJ Radial Tape in Fan Fold Box or On Reel

Radial tape in fan fold box or on reel of the reliable TO–92 package are the best methods of capturing devices for automatic insertion in printed circuit boards. These methods of taping are compatible with various equipment for active and passive component insertion.

- Available in Fan Fold Box
- Available on 365 mm Reels
- Accommodates All Standard Inserters
- Allows Flexible Circuit Board Layout
- 2.5 mm Pin Spacing for Soldering
- EIA–468, IEC 286–2, EIAJ RC1008B

TO–92 RADIAL TAPE IN FAN FOLD BOX OR ON REEL



Ordering Notes:

When ordering radial tape in fan fold box or on reel, specify the style per Figures 3 through 8. Add the suffix "RLR" and "Style" to the device title, i.e. MPS3904RLRA. This will be a standard MPS3904 radial taped and supplied on a reel per Figure 9.

Fan Fold Box Information — Minimum order quantity 1 Box/$200LL.
Order in increments of 2000.

Reel Information — Minimum order quantity 1 Reel/$200LL.
Order in increments of 2000.

US/European Suffix Conversions

US	EUROPE
RLRA	RL
RLRE	RL1
RLRM	ZL1

TO–92 EIA RADIAL TAPE IN FAN FOLD BOX OR ON REEL

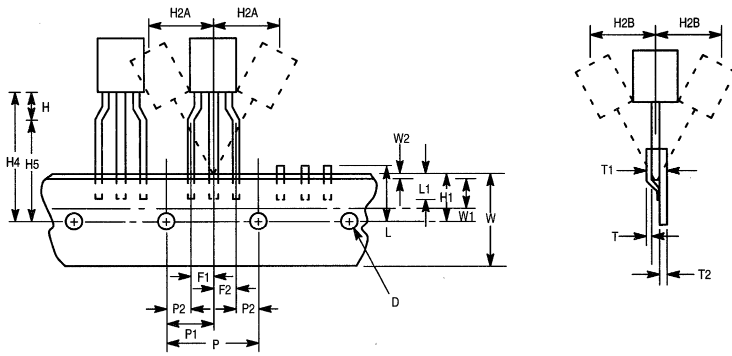


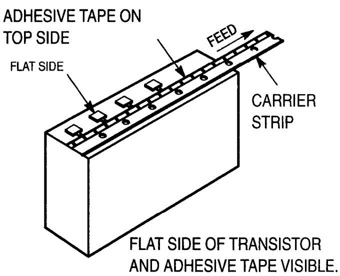
Figure 1. Device Positioning on Tape

Symbol	Item	Specification			
		Inches		Millimeter	
		Min	Max	Min	Max
D	Tape Feedhole Diameter	0.1496	0.1653	3.8	4.2
D2	Component Lead Thickness Dimension	0.015	0.020	0.38	0.51
F1, F2	Component Lead Pitch	0.0945	0.110	2.4	2.8
H	Bottom of Component to Seating Plane	.059	.156	1.5	4.0
H1	Feedhole Location	0.3346	0.3741	8.5	9.5
H2A	Deflection Left or Right	0	0.039	0	1.0
H2B	Deflection Front or Rear	0	0.051	0	1.0
H4	Feedhole to Bottom of Component	0.7086	0.768	18	19.5
H5	Feedhole to Seating Plane	0.610	0.649	15.5	16.5
L	Defective Unit Clipped Dimension	0.3346	0.433	8.5	11
L1	Lead Wire Enclosure	0.09842	—	2.5	—
P	Feedhole Pitch	0.4921	0.5079	12.5	12.9
P1	Feedhole Center to Center Lead	0.2342	0.2658	5.95	6.75
P2	First Lead Spacing Dimension	0.1397	0.1556	3.55	3.95
T	Adhesive Tape Thickness	0.06	0.08	0.15	0.20
T1	Overall Taped Package Thickness	—	0.0567	—	1.44
T2	Carrier Strip Thickness	0.014	0.027	0.35	0.65
W	Carrier Strip Width	0.6889	0.7481	17.5	19
W1	Adhesive Tape Width	0.2165	0.2841	5.5	6.3
W2	Adhesive Tape Position	.0059	0.01968	.15	0.5

NOTES:
1. Maximum alignment deviation between leads not to be greater than 0.2 mm.
2. Defective components shall be clipped from the carrier tape such that the remaining protrusion (L) does not exceed a maximum of 11 mm.
3. Component lead to tape adhesion must meet the pull test requirements established in Figures 5, 6 and 7.
4. Maximum non–cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
5. Holddown tape not to extend beyond the edge(s) of carrier tape and there shall be no exposure of adhesive.
6. No more than 1 consecutive missing component is permitted.
7. A tape trailer and leader, having at least three feed holes is required before the first and after the last component.
8. Splices will not interfere with the sprocket feed holes.

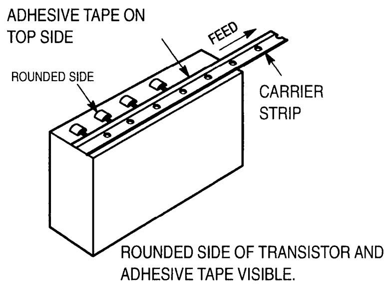
TO–92 EIA RADIAL TAPE IN FAN FOLD BOX OR ON REEL

FAN FOLD BOX STYLES



Style M fan fold box is equivalent to styles E and F of reel pack dependent on feed orientation from box.

Figure 2. Style M



Style P fan fold box is equivalent to styles A and B of reel pack dependent on feed orientation from box.

Figure 3. Style P

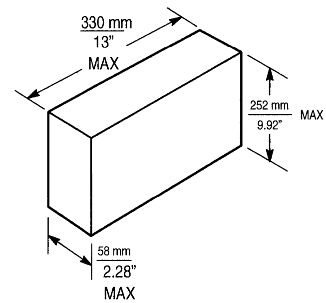
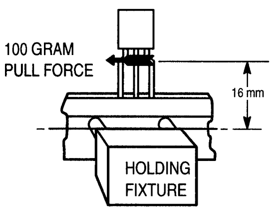


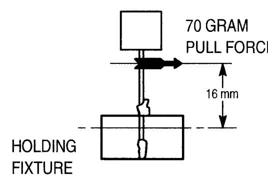
Figure 4. Fan Fold Box Dimensions

ADHESION PULL TESTS



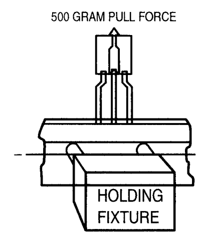
The component shall not pull free with a 300 gram load applied to the leads for 3 ± 1 second.

Figure 5. Test #1



The component shall not pull free with a 70 gram load applied to the leads for 3 ± 1 second.

Figure 6. Test #2

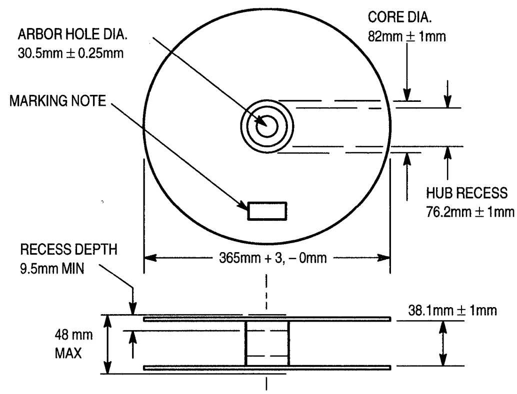


There shall be no deviation in the leads and no component leads shall be pulled free of the tape with a 500 gram load applied to the component body for 3 ± 1 second.

Figure 7. Test #3

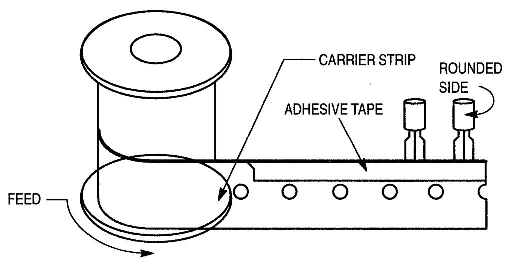
TO–92 EIA RADIAL TAPE IN FAN FOLD BOX OR ON REEL

REEL STYLES



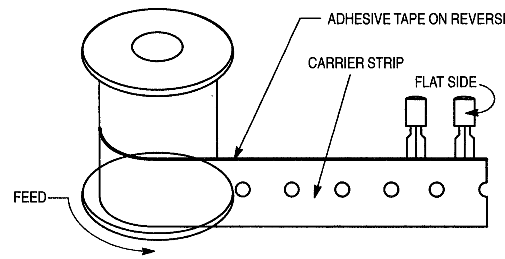
Material used must not cause deterioration of components or degrade lead solderability

Figure 8. Reel Specifications



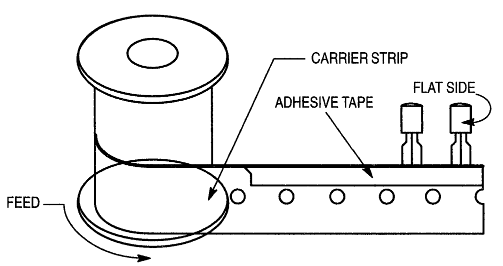
Rounded side of transistor and adhesive tape visible.

Figure 9. Style A



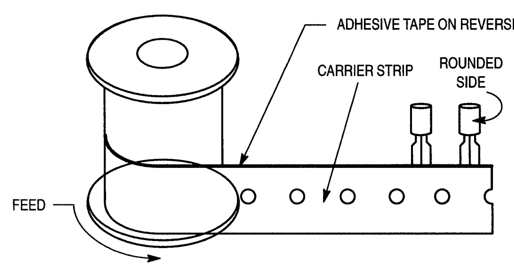
Flat side of transistor and carrier strip visible (adhesive tape on reverse side).

Figure 10. Style B



Flat side of transistor and adhesive tape visible.

Figure 11. Style E



Rounded side of transistor and carrier strip visible (adhesive tape on reverse side).

Figure 12. Style F

Product Literature and Technical Training

In Brief . . .

With the pace of new semiconductor product introductions, the task of providing an effective and up–to–date perspective of available components is beyond the means of any single document. Hence, a comprehensive Motorola Literature System has been put in place to keep semiconductor users totally informed of all aspects of the Motorola product lines — from new product introductions, to applications, to major changes in directions.

The Motorola technical literature library and associated services consist of the following:

- An extensive library of Data Books, each containing a complete selection of data sheets associated with a particular product line.
- A series of User's Manuals and Design Manuals dealing with the application of highly complex products.
- A wide range of Application Notes and Article Reprints detailing the utilization of new and significant products.
- Instructor–led Training for: Digital Signal Processing (DSP) Family; M68000 Family; Embedded Controllers (EC); MC68360 QUIC; PowerPC; Microcontroller (MCU); RISC Family; plus the MC68302, MC68332, MC68340 and the MC68HC16.

These products and services are described on the following pages. However, because of different conditions and standards, some of these may not be available outside the USA.

Technical Data Services

Motorola Semiconductor Master Selection Guide

For the identification and preliminary selection of components for circuit and system designs

For the design engineer, the Motorola Master Selection Guide is perhaps the most important single document for the identification and preliminary selection of components for circuit and system designs. Within its pages is a complete listing and description of Motorola semiconductor devices currently in general use, and those recommended for new designs. It serves two purposes:

1. It lists all standard products in the vast Motorola semiconductor inventory for rapid identification.
2. It divides this total product offering into a variety of major product categories, with sufficient technical information to permit an intelligent first–order evaluation as to the most suitable devices for a specific application.

Semiconductor Data Update Magazine

Innovative new developments from Motorola's Semiconductor Products Sector

This highly informative periodical is available to all semiconductor users on a free subscription basis. The magazine provides information on new semiconductor products and developments and provides a quick–scan insight into new–product offerings. Concise, informative articles discuss significant new product capabilities as well as newly introduced services. In short, it represents an overview of the latest and most important events at Motorola that influence the efficient implementation and most cost–effective use of semiconductor devices.

To receive Update Magazine, in the USA, please contact the Literature Distribution Center by calling 1–800–441–2447.

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Motorola SPS World Marketing Internet Server

Motorola SPS's Electronic Data Delivery organization has set up a World Wide Web Server to deliver Motorola SPS's technical data to the global Internet community.

Technical data such as the complete Master Selection Guide along with the OEM North American price book are available on the Internet server with full search capabilities. Other data on the server include abstracts of databooks, application notes, selector guides, and textbooks. All have easy text search capability. Ordering Literature from the Literature Distribution Center is available on line.

Other features of Motorola SPS's Internet server include the availability of a searchable press release database, technical training information with on–line registration capabilities, complete on–line access to the MFAX system for ordering faxes, an on–line technical support form to send technical questions and receive answers through email, information on product groups, full search capabilities of device models, a listing of the Domestic and International sales offices, and links directly to other Motorola world wide web servers.

After accessing the Internet, to locate the Motorola SPS World Marketing server, use the following URL:

http://Design–NET.com

For more information on Motorola SPS's Internet server you can request BR1307/D from MFAX or request a copy from Literature Distribution Center by calling 1–800–441–2447.

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Complete technical data for the world's most comprehensive inventory of semiconductor components

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Motorola attempts to fill the need for applications information concerning today's highly complex electronic components. Each year dozens of authors from colleges and universities, and from the industry, add their individual contributions to the collective literature. From these, Motorola has selected a number of texts which add substantially to the comprehension and applications of some of the more complex products. By buying these in large quantities and providing them to customers at lower than retail cost, Motorola hopes to foster a more comprehensive acquaintance with these products at greatly reduced prices.

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Data Books and Handbooks

BR1330/D, ECLinPS Lite Single Gate ECL Devices, Translators and PLL Support Products
BR1333/D, Timing Solutions
BR1334/D, High Performance Frequency Control Products
DL110/D, RF Device Data
DL111/D, Bipolar Power Transistor Data
DL118/D, Optoelectronics Device Data
DL121/D, FAST and LS TTL Data
DL122/D, MECL Device Data
DL126/D, Small–Signal Transistors, FETs and Diodes Device Data
DL128/D, Linear and Interface Integrated Circuits
DL129/D, High Speed CMOS Data
DL131/D, CMOS Logic Data
DL135/D, TMOS Power MOSFET Transistor Data
DL136/D, Communications Device Data
DL137/D, Thyristor Device Data
DL138/D, FACT Data
DL140/D, High Performance ECL Data – ECLinPS and ECLinPS Lite
DL150/D, TVS/Zener Device Data
DL151/D, Rectifier Device Data
DL155/D, Dynamic RAMs & Memory Modules Data
DL156/D, Fast Static RAM – Component and Module Data
DL158/D, Multimedia Device Data
DL159/D, LonWorks Technology Device Data
DL200/D, Pressure Sensor Device Data
DL201/D, FPGA Data: Field Programmable Gate Arrays

Selector Guides & Application Literature

AJ100/D, Discrete Proceedings – The Journal of CPSTG Strategic Marketing
BR128/D, Semiconductor Data 'Update' Magazine
BR135/D, Applications Literature Catalog
BR518/D, Reliability & Quality Handbook
BR724/D, 88open Sourcebook
BR729/D, Motorola 68K Source – Third Party Vendor Catalog
BR916/D, Packaging Manual for ASIC Arrays
BR923/D, Communications, Power & Signal Technologies Group – Reliability Audit Report

Selector Guides & Application Literature (continued)

BR1100/D, Microprocessor and Memory Technologies Group: Reliability and Quality Report
BR1112/D, M68HC05 & M68HC08 Family Customer Specified Integrated Circuit (CSIC) Microcontroller Unit (MCU) Literature
BR1133/D, HIPPO: High–Performance Internal Product Portfolio Overview
BR1137/D, The Motorola Explorer's Guide to the World of Embedded Control Solutions
BR1138/D, 68HC08 – Innovate, Migrate, Accelerate
BR1143/D, Fast Static RAM Cross Reference Guide
BR1202/D, Motorola Quality System Review Guidelines
BR1306/D, CATS – Customer Analysis Tracking System
BR1400/D, OACS (ASIC) – Open Architecture CAD System
BR1437/D, Multichip Module Solutions
CALCPSTG/D, Communications, Power and Signal Technologies Group: New Product Calendar
CMRQS/D, CSIC Microcontrollers: Reliability and Quality Monitor Report
CR100/D, Communications, Power and Signal Technologies Group: Through–Hole to Surface Mount Cross Reference
CR103/D, Transient Voltage Suppressors, General Instruments Cross Reference
CR104/D, General Instrument–to–Motorola Optoelectronics Cross Reference
DL408/D, 8–bit MCU Applications Manual
DL409/D, 16/32–bit Applications Manual
DL410/D, Power Applications Manual
DL411/D, Communications Applications Manual
DL412/D, Industrial Control Applications Manual
DL413/D, Radio, RF and Video Applications Manual
DL414/D, FET Applications Manual
DMRQS/D, Microcontroller Technologies Group, DSP Division: Reliability and Quality Monitor Report
DSPNEWSL/D, DSP News
HB205/D, MECL System Design Handbook
HB214/D, Rectifier Applications Handbook
HB215/D, RF Application Reports
MRQS/D, Advanced Microcontroller Division: Reliability and Quality Monitor Report

Selector Guides & Application Literature (continued)

SG46/D, RF Products Selector Guide & Cross Reference
SG73/D, Master Selection Guide
SG96/D, Analog/Interface ICs Selector Guide & Cross Reference
SG140/D, SCANSWITCH Selector Guide
SG146/D, Digital Signal Processors Update
SG162/D, Sensor Products Division
SG165/D, CSIC Microcontrollers Update
SG166/D, Advanced Microcontroller Division Update
SG167/D, High Performance Embedded Systems Fact Sheet
SG169/D, Mixed Signal Solutions from MOS Digital–Analog Integrated Circuits Division
SG171/D, Fast Static RAM Product Update
SG172/D, Dynamic Memory Update
SG173/D, CSIC Microcontrollers: Modular Development Tools
SG175/D, RISC Microprocessor Division: The PowerPC Microprocessor Family
SG265/D, Power MOSFETs Product Update
SG266/D, Bipolar Power Transistors Product Update
SG267/D, Rectifier Product Update
SG268/D, Thyristor Product Update
SG271/D, D^2PAK Surface Mount Selector Guide
SG273/D, Optoelectronic Operations Selector Guide
SG274/D, Zener Operations Selector Guide
SG275/D, Small–Signal Operations: Surface Mount Packages
SG365/D, Timing Soutions Selector Guide
SG367/D, High–Performance Gate Arrays
SG370/D, Discrete Surface Mount Selector Guide
SG372/D, Hard Disk Drive Products – Quick Reference, November
SG375/D, Silicon Solutions for Motion Control
SG417/D, Semiconductor Products for Wireless Communications
SG422/D, PowerPC Microprocessors Product Overview
SG423/D, TIGER: The Integrated Guide to European RAMs
SG424/D, EAGLES: European Analog Guide for Leading & Emerging Systems
SG425/D, Lamp Ballast Selector Guide
SG426/D, DINO: Discrete Innovation News Overview

User's Manuals

ADCRM/AD, Analog–to–Digital Converter Reference Manual
CPU08RM/AD, M68HC08 Central Processor Unit Reference Manual
CPU16RM/AD, M68HC16 Family Reference Manual
CPU32RM/AD, CPU32 Central Processor Unit Reference Manual
CTMRM/D, Configurable Timer Module Reference Manual
DLE404/D, M6804 MCU Manual

User's Manuals (continued)

DSP56KFAMUM/AD, DSP56000 Digital Signal Processor Family Manual
DSP56000UM/AD, DSP56000/DSP56001 Digital Signal Processor User's Manual
DSP56002UM/AD, DSP56002 Digital Signal Processor User's Manual
DSP56003UM/AD, DSP56003/005 Digital Signal Processor User's Manual
DSP56004UM/AD, DSP56004 Digital Signal Processor User's Manual
DSP56100FM/AD, DSP56100 Digital Signal Processor Family Manual
DSP56156UM/AD, DSP56156 Digital Signal Processor User's Manual
DSP56166UM/AD, DSP56166 Digital Signal Processor User's Manual
DSP56300FM/AD, DSP56300 24–Bit Digital Signal Processor Family Manual
DSP56301UM/AD, DSP56301 24–Bit Digital Signal Processor User's Manual
DSP96002UM/AD, DSP96002 IEEE Floating–Point Dual–Port Processor User's Manual
GPTRM/AD, Modular Microcontroller Family General Purpose Timer Reference Manual
H4CDM/D, H4C Series Design Reference Guide
H4CPDM/D, H4CPlus Series Design Reference Guide
HC711D3PGMR/AD1, M68HC711D3PGMR Programmer Board User's Manual
HDCDM/D, HDC Series Design Reference Guide
LONUG/AD, LonBuilder User's Guide
LP2/D, Portable Power: The Competitive Edge of the 68HC11 – Low Power Design Guidebook
M5CDM/D, M5C Series Design Reference Guide
M68CPU32BUG/D, CPU32BUG Debug Monitor User's Manual
M68HC05AG/AD, M68HC05 Applications Guide
M68HC08RG/AD, HC08 Family Reference Guide
M68HC11EVB/D1, M68HC11EVB Evaluation Board User's Manual
M68HC11EVBU/AD2, M68HC11EVBU Universal Evaluation Board User's Manual
M68HC11EVM/AD8, M68HC11EVM Evaluation Module User's Manual
M68HC11RM/AD, M68HC11 Reference Manual
M68PCBUG11/D2, M68HC11 PCbug11 User's Manual
M68PRM/D, M6800 Programming Reference Manual
M6809PM/AD, MC6809–MC6809E Microprocessor Programming Manual (1981)
M68000PM/AD, M68000 Family Programmer's Reference Manual
M68000UM/AD, M68000 8–/16–/32–bit Microprocessors User's Manual, Ninth Edition
M68020UM/AD, MC68020/MC68EC020 Microprocessors User's Manual

User's Manuals (continued)

M68040UM/AD, MC68040, MC68040V, MC68LC040, MC68EC040, MC68EC040V Microprocessors User's Manual
M68060UM/AD, MC68060, MC68LC060, MC68EC060 Microprocessors User's Manual
M68332EVKEM/AD1, M68332EVK Evaluation Kit Exercise Manual
MC68EC030UM/AD, MC68EC030 32–bit Embedded Controller User's Manual
MC68F333UM/AD, MC68F333 User's Manual
MC68HC05CxRG/AD, MC68HC05Cx HCMOS Single–Chip Microcontrollers Programming Reference Guide
MC68HC11A8RG/AD, MC68HC11A8 Programming Reference Guide
MC68HC11C0RG/AD, MC68HC11C0 Programming Reference Guide
MC68HC11D3RG/AD, MC68HC11D3/MC68HC711D3 Programming Reference Guide
MC68HC11ERG/AD, MC68HC11E Programming Reference Guide
MC68HC11F1RG/AD, MC68HC11F1 Programming Reference Guide
MC68HC11K4RG/AD, MC68HC11K4/MC68HC711K4 Programming Reference Guide
MC68HC11KA4RG/AD, MC68HC11KA4/MC68HC711KA4 Programming Reference Guide
MC68HC11L6RG/AD, MC68HCL6/MC68HC711L6 Programming Reference Guide
MC68HC11MRG/AD, M68HC11 M Series Programming Reference Guide
MC68HC11NRG/AD, MC68HC11N Series Programming Reference Guide
MC68HC16Y1UM/AD, MC68HC16Y1 User's Manual
MC68HC16Z1UM/AD, MC68HC16Z1 User's Manual
MC68HC16Z2UM/AD, MC68HC16Z2 User's Manual
MC68MH360RM/AD, MC68MH360 QUICC32 Quad Integrated Multichannel Controller Reference Manual
MC68030UM/AD, MC68030 Enhanced 32–bit MPU User's Manual, third edition
MC68040DH/AD, MC68040 Designer's Handbook
MC68302UM/AD, MC68302 Integrated Multiprotocol Processor User's Manual
MC68306UM/AD, MC68306 Integrated EC000 Processor User's Manual
MC68307UM/AD, MC68307 Integrated Multiple–Bus Processor User's Manual
MC68322UM/AD, Bandit: MC68322 Integrated Printer Processor User's Manual
MC68328UM/AD, MC68328 (Dragonball) Integrated Processor User's Manual
MC68330UM/AD, MC68330 Integrated CPU32 Processor Users Manual
MC68331UM/AD, MC68331 User's Manual
MC68332UM/AD, MC68332 User's Manual
MC68340UM/AD, MC68340 Integrated Processor User's Manual
MC68341UM/AD, MC68341 Integrated Processor User's Manual
MC68349UM/AD, MC68349 High Performance Integrated Processor User's Manual
MC68356UM/AD, MC68356 Signal Processing Communications Engine User's Manual
MC68360UM/AD, MC68360 Quad Integrated Communications Controller User's Manual
MC68488UM/AD, MC68488 General Purpose Interface Adapter User's Manual
MC68605UM/AD, MC68605 X.25 Protocol Controller User's Manual
MC68606UM/AD, MC68606 Multi–Link LAPD Protocol Controller User's Manual
MC68824UM/AD, MC68824 Token Bus Products User's Manual
MC68836UM/AD, MC68836 FDDI User's Manual
MC68837UM/AD, MC68837 FDDI User's Manual
MC68838UM/AD, MC68838 FDDI User's Manual
MC68839UM/AD, MC68839 FDDI System Interface User's Manual
MC68840UM/AD, MC68840 Integrated Fiber Distributed Data Interface User's Manual
MC68847UM/AD, MC68847 Quad ELM FDDI User's Manual
MC68851UM/AD, MC68851 Paged Memory Management Unit User's Manual, second edition
MC68881UM/AD, MC68881/MC68882 Floating–Point Coprocessor User's Manual, second edition
MC88100UM/AD, MC88100 RISC Microprocessor User's Manual
MC88110/410DH/AD, MC88110/MC88410 Designer's Handbook
MC88110UM/AD, MC88110 Second Generation RISC Microprocessor User's Manual
MC88200UM/AD, MC88200 Cache/Memory Management Unit User's Manual
MC88410UM/AD, MC88410 Secondary Cache Controller User's Manual
MC92005UM/D, MC92005 SBus Slave Interface Controller User's Manual
MCCIRM/AD, Multichannel Communication Interface Reference Manual
MCF5102UM/AD, MCF5102 ColdFire User's Manual
MCF5200PRM/AD, ColdFire Programmer's Reference Manual
MCUDEVTLDIR/D, Motorola Microcontroller Development Tools Directory
MPCFPE/AD, PowerPC Microprocessor Family: The Programming Environments
MPCTOOLBK/AD, PowerPC Tools – Development Tools for PowerPC Microprocessors
MPC105UM/AD, PowerPC PCI Bridge/Memory Controller User's Manual

Motorola Data and Application Literature: (continued)

User's Manuals (continued)

MPC601UM/AD, PowerPC 601 – RISC Microprocessor User's Manual
MPC603eUM/AD, PowerPC 603e RISC Microprocessor User's Manual
MPC604UM/AD, PowerPC 604 RISC Microprocessor User's Manual
QSMRM/AD, Queued Serial Module Reference Manual
RCPURM/AD, MPC500 Family: RCPU Reference Manual
SCIMRM/AD, Single–Chip Integration Module Reference Manual
SIMRM/AD, System Integration Module Reference Manual
SIURM/AD, MPC500 Family: System Integration Unit Reference Manual
TIM08RM/AD, TIM08 Timer Interface Module Reference Manual
TPURM/AD, M68300 Family Time Processor Unit Reference Manual

Textbooks

TB301/D, Basic Microprocessors and the 6800
TB304/D, Pascal Programming Structures for Motorola Microprocessors
TB309/D, Programming the 6809
TB312/D, Introduction to Integrated Circuit Layout
TB318/D, Microprocessor Systems Design: 68000 Hardware, Software and Interfacing
TB321/D, Practical Switching Power Supply Design
TB323/D, The 68000 Book

Textbooks (continued)

TB324/D, Real Time Digital Signal Processing Applications with Motorola's DSP56000 Family
TB326/D, Radio Frequency Transistors: Principles and Practical Applications
TB328/D, Programming Microcontrollers in C
TB329/D, Sensor Technology and Devices
TB330/D, PowerPC Computing
TB331/D, Power Supply Cookbook
TB332/D, Digital Signal Processing Using the Motorola DSP Family
TB333/D, Signal Processing, Image Processing and Graphics Applications with Motorola's DSP96002 Processor. Volume I: Signal Processing
TB334/D, Signal Processing, Image Processing and Graphics Applications with Motorola's DSP96002 Processor. Volume II: Image Processing and Graphics Applications
TB335/D, The PowerPC Architecture: A Specification for a New Family of RISC Processors
TB336/D, Automotive Electronics Handbook
TB337/D, PowerPC Programming for Intel Programmers

Technical Data Services

BR1307/D, Motorola SPS World Marketing Internet Server
DK105/D, Scattering Parameter Library
DK106/D, Scattering Parameter Plotting Utility
DK107/D, Impedance Matching Program
SG73/D, Master Selection Guide
SEMIVID/D, Basic Semiconductor Videos
Dr. BuB, DSP Electronic Bulletin Board Freeware Line, Microcontroller Electronic Bulletin Board

Motorola Application Literature

Semiconductors in theory and practice

Application Notes, Engineering Bulletins and Article Reprints are part of a total information system to define the characteristics and applications of semiconductor devices. Motorola's library consists of more than 300 such documents dealing with the applications of all types of semiconductors from discrete power transistors to the most complex microprocessors. All are described in an Application Note Catalog available from our Literature Distribution Center.

Individual application notes, application reports, engineering bulletins and article reprints can also be ordered from our Literature Distribution Center.

Contact the Literature Distribution Center for prices and ordering information. In addition, there may be an alternative document available in some countries, contact your local Motorola Sales Office.

For complete summaries and prices: order BR135/D from the Literature Distribution Center.

DL408/D	8–bit MCU Applications Manual	DL412/D	Industrial Control Applications Manual
DL409/D	16/32–bit Applications Manual	DL413/D	Radio, RF and Video Applications Manual
DL411/D	Communications Applications Manual	DL414/D	FET Applications Manual

Motorola Technical Training Courses

Registration & Tuition

How to register for open enrollment courses

To enroll in a Motorola Technical Training course, please call the registrar at (602) 302–8008 from 7:00 a.m to 4:00 p.m., MST, Monday through Friday. If you prefer, refer to page 7.1–10 for alternative ways to register.

For Ascent Technology offered courses call their registrar at 1–800–410–3601.

For Arnewsh Inc. offered courses call their business number at (970) 223–1616.

Plan early as classes fill up rapidly and space is limited.

Closed courses

Courses listed can be taught at your facility and can be tailored to fit your needs.

Method of payment for Motorola courses

- Customers paying by check or purchase order, please make payable to Motorola and mail to: ATTN: Technical Training, 432 N. 44th Street, Suite 200, Phoenix, AZ 85008.
- For your convenience Motorola Technical Training now accepts credit card payments; VISA, MasterCard or American Express.
- Motorola employee's department number will be internally charged.

To ensure a reserved space, payment is required two weeks prior to class start date. No refund will be given once class begins; however, the tuition may be applied to a future class. **Note:** Please contact Ascent Technology or Arnewsh, Inc. directly for their independent payment policy.

MOTOROLA COURSE PRICING

For North American class pricing contact the registrar at:

– (602) 302–8008.

For international training please contact local regional office or one of the following training departments:

– Munich, Germany, (49)–89–92103571
– Velizy Villacoublay Cedex, France, (33)–1–34635894
– Aylesbury, United Kingdom, (44)–1296–380304

TRAINING PARTNER COURSE PRICING

Please contact company directly for independent pricing information:
– Ascent Technologies, 1–800–410–3601
– Arnewsh, Inc., (970) 223–1616

Confirmation

A written notice confirming your enrollment will be sent to you prior to the class. If you have not received confirmation one week prior to the class, call our registrar at (602) 302–8008 for Motorola courses. Call Arnewsh or Ascent Technologies directly for independent confirmations.

Motorola Technical Training Courses (continued)

PowerPC™ 6xx Microprocessor

Description: The MPC6xx is primarily targeted for the desktop marketplace. The PowerPC MPC6xx course details all publicly announced MPC6xx implementations such as the MPC601, MPC602, MPC603 and MPC604. This course contains lecture, labs and exercises.
Prerequisites: The student must have advanced microprocessor and assembly language knowledge. An understanding of memory management, multi–processing/master, and cache concepts is also beneficial.

MPC505 PowerPC™ Microcontroller

Description: In this course the student learns to design with the embedded PowerPC core, system integration unit (SIU), and associated components of the MPC505. The course consists of lecture and exercises.
Prerequisites: The student must have advanced microprocessor and assembly language knowledge. PowerPC experience is not required.

DSP5600x Family Microprocessor

Description: In this course the student (with digital signal processing design experience) learns to design with the DSP5600x digital signal processor. The course consists of lecture, labs, and exercises.
Prerequisites: The student must have knowledge of at least one microprocessor and its assembly language. A prior understanding of digital signal processing theory is important for those whose applications are DSP oriented.

DSP561xx Family Microprocessor

Description: In this course the student (with digital signal processing design experience) learns to design with the DSP561xx digital signal processor. The course consists of lecture and exercises.
Prerequisites: The student must have knowledge of at least one microprocessor and its assembly language. A prior understanding of digital signal processing theory is important for those whose applications are DSP oriented.

MC68HC08 Microcontroller

Description: In this course the student learns to design with the MC68HC08 including the on–chip subsystems. Lecture, labs, and exercises are a major part of the learning process for this course.
Prerequisites: Knowledge of microprocessor fundamentals. Previous experience with either MC68HC05 or MC68HC11 is helpful. Students will be sent a self–study packet upon enrollment. The pre–work must be completed prior to the course start date.

MC68HC16 Microcontroller

Description: In this course the MC68HC16Z1 and MC68HC16Y1 are covered. In this class the student learns to design with the MC68HC16. The CPU16, general purpose timer, and analog–to–digital converter are common to both versions. The MC68HC16Z1 includes the system integration module, queued serial module, and standby RAM, while the MC68HC16Y1 includes the single–chip integration module, multi–channel communications interface, timer processor unit, and standby RAM with TPU emulation. Lecture, labs and exercises are a major part of the learning process for this course.
Prerequisites: Knowledge of microprocessor fundamentals. Previous experience with either MC68HC05 or MC68HC11 is helpful. Students will be sent a self–study packet upon enrollment. The pre–work must be completed prior to the course start date.

TPU Microcode

Description: The TPU Microcode course is a lab–intensive course in which the student learns how to write microcode functions for the TPU. The course is approximately 50% lecture and exercises and 50% lab time.
Prerequisite: The student must have advanced microprocessor experience.

MC68356 Signal Processing Communication Engine

Description: In this course the student learns to design and write programs for the various chip submodules. This includes the MC68000/MC68008 static core, communication processor (CP), system integration block (SIB), and 56002 digital signal processor. Labs are a major part of the learning process; lecture and exercises are also a part of the course.
Prerequisites: To benefit most from the course, a S/W and H/W understanding of the MC68000 microprocessor is a requirement. Also, some knowledge of the DSP56002 instructions and addressing modes will be helpful. Students who need to meet these requirements will receive a 68000 and/or 56000 pre–work packet. We highly encourage students to complete the pre–work packet before coming to class.

MC68360 QUICC–QUad Integrated Communication Controller

Description: In this course the student learns to design and write programs for the various chip submodules. This includes the CPU32+ core, communication processor module (CPM) and system integration module (SIM60). Labs are a major part of the learning process; lecture and exercises are also a part of the course.
Prerequisites: To benefit most from the course, a S/W and H/W understanding of the MC68000 microprocessor is a requirement. Students who need to meet these requirements will receive a 68000 pre–work packet. We highly encourage students to complete the pre–work packet before coming to class.

Ascent Technologies Course Information – Microcontrollers

MC68HC05 Microcontroller Family

Description: This is an introduction to the MC68HC05 microcontroller family, covering the major features of this cost–effective microcontroller. Students will understand how to program and apply all the major subsystems of the MC68HC05 including discrete I/O, timer functions, serial communication interfaces and analog to digital conversion. Many application examples are included.
Prerequisites: No familiarity with microcontrollers is assumed. Some familiarity with binary and hexadecimal numbering systems as well as fundamental electronic theory is helpful.

MC68HC11 Microcontroller Family

Description: This is an introduction to the MC68HC11 microcontroller family, covering the major features of this industry–standard microcontroller. Students will understand how to program and apply all the major subsystems of the MC68HC11 including discrete I/O, timer functions, serial communication interfaces, analog to digital conversion, and the computer operating properly (COP) watchdog timer. Many application examples are included.
Prerequisites: Students should have a basic understanding of embedded system operations and their target application.

MC68332 Embedded Controller

Description: This is an intensive introduction to the MC68332 embedded controller family. Students will understand how to program and apply all the major subsystems of the 68332, including discrete I/O, timer functions, serial communication interfaces, analog to digital conversion, computer operating properly (COP) watchdog timer. Many application examples are included.
Prerequisites: Students should have a basic understanding of embedded system operations and their target application.

Ascent Technologies, an embedded systems training and engineering services company, is located at 525 Avis Drive, Suite 15, Ann Arbor, MI 48108. For a current course schedule, course pricing, to enroll in a course, or to schedule a course at your location, please call 1–800–410–3601.

Arnewsh, Inc. Course Information – Microprocessors

MC68EC/000 Microprocessor

Description: This course covers both the software and hardware aspects of the MC68EC/000 processor. The course will cover programming model, data types, instruction set, addressing modes, exception processing, signal function and characteristics.
Prerequisites: A basic understanding of microprocessor systems, digital logic and memory concepts is required.

MC68EC/000 Family Programming

Description: This course presents the software functionality of all the MC68/EC0x0 microprocessors. The course covers the programming model, data types, instruction set, addressing modes, exception processing, and an overview of the caches and memory management unit in 020/030/040. The course consists of lecture, exercises, and labs.
Prerequisites: A basic understanding of microprocessor systems and assembly language is required.

MC68EC/040/060 Microprocessors

Description: This course covers all the hardware and system aspects of both the MC68040 and MC68060 members. The first one and a half days is used to cover the MC68040 and the common issues of the MC68060. The last half day is used to point out MC68060 differences and the new features.
Prerequisites: Students should have complete familiarity with the software aspects of the M68K family. Students who also need the software and programming background may attend the M68K family programming course offered in the same week.

MC68302 Integrated Multiprotocol Processor

Description: In this course the students learn to design and write programs for the various chip submodules. This includes the 68000 core, communication processor (CP) and system integration block (SIB). The course consists of lecture, exercises and labs.
Prerequisites: Students need the software and hardware understanding of the MC68000 processor.

MC6834x Family Integrated Processor ('330, '340, '341, '349)

Description: In this course the students will learn to design with the CPU32/CPU32+, DMA channels, timers, serial I/O modules, and system integration module. The course consists of lecture, exercises, and labs.
Prerequisites: Students need the software and hardware understanding of the M68K processor family.

DSP96002 Microprocessor

Description: This course prepares the student for designing systems which include the DSP96002.
Prerequisites: This course assumes no prior knowledge of the DSP56001 device.

CUSTOMIZED COURSES

Arnewsh, Inc. can customize these courses for presentation at your location. For scheduling and pricing information please contact Arnewsh, Inc. (970) 223–1616.

SINGLE BOARD COMPUTER SUPPLIER

Arnewsh, Inc. is also the supplier of a number of single board computer/evaluation boards which are used in Motorola lab based courses in which students are able to apply hands–on experience to their learning process. These boards include:

- SBC68K, MC68000 based board
- SBC302, MC68302 based board
- SBC306, MC68306 based board
- SBC360/SBC360EC, MC68360 (and 040) based boards
- UDLP1, Universal Design Lab Platform

For information write, call or fax to:

Arnewsh, Inc.
P.O. Box 270352
Fort Collins, CO 80527–0352
Phone: (970) 223–1616
Fax: (970) 223–9573

Motorola Technical Training Courses (continued)

Call 602–302–8008 for the latest copy
of our Technical Training Catalog and class schedule.
If you are outside of the USA, call your local Technical Training Center
or Sales Office and ask for BR348/D.

Technical Training Centers

Regional Training Centers

Detroit
41700 Six Mile Road
Nothville, MI 48167
(313) 347–6800

Phoenix
432 N 44th Street
Phoenix, AZ 85008
(602) 302–8008

International Training Centers

Munich, Germany	(49)–89–92103571
Velizy Villacoublay Cedex, France	(33)–1–34635894
Aylesbury, United Kingdom	(44)–1296–380304

Provide the following information when registering:

You can also register by:
Email: R17994@email.sps.mot.com
Internet WWWeb, URL: http://Design–NET.com

MOTOROLA
Technical Training • 432 North 44th Street • Suite 200 • Phoenix, AZ 85008
Voice: (602) 302–8008 • FAX: (602) 302–8025

ATTENTION: REGISTRAR

Contact's Name: ______________________________ Date Faxed: __________

Contact's Phone Number: ____________________ Fax Number: ______________

Company: ____

Street Address: ____

City: ____________________________ State: ______ Zip: ____________

Course Name: __________________ Date: ________ Location: __________

Note: Payment is due no later than two weeks before class start date, either by purchase order, check, or money order. If submitting a purchase order, please fax a copy with your registration to (602) 302–8025.

1. ____
Student Name(s)   Address / Phone / Fax

____
*Mail Stop   *SS#   *Dept.#   *Badge#   *Sector#

*REQUIRED BY ALL MOTOROLA EMPLOYEES ONLY

Device Index and Subject Index

In Brief . . .

Device Index

The following index lists the device numbers of the products contained in this selector guide and references the page number where each device is described in greater detail.[1] The listing is in a numeric sequence organized in a "computer sort." This means that all the devices listed herein follow a 39 character alphabet. This "new" alphabet starts with a Period, a Dash and a Slash (. – /), followed by the 26 letter alphabet (A thru Z), which is then followed by 10 numbers (0 thru 9).

The ranking or hierarchy of this 39 character alphabet is as follows:

. – / A B C D E F G H I J K L M N O P Q R S T U V W X Y Z 0 1 2 3 4 5 6 7 8 9

Therefore, if you are looking for a device starting with a letter of the alphabet like an MC1741CP, it would appear before a device starting with a number, such as 2N1132.

To find a device in this index, start with the first character of the device and find that section of the index; next move to the second character in the device number, and move to that character within the same portion of the listing; and so on until the device number is found. In other words, it is used just like a dictionary, character by character.

For example, to find the 2N6837, go to that section of the listing that begins with the number "2" (Notice that the section follows all devices that begin with a letter of the alphabet or "1"). Next, find that portion of the listing that begins with "2N" (Notice it follows those devices that begin with "2K"). Next, find that portion of the listing that begins with "2N6" (Notice it follows those devices that begin with "2N5"). Continue looking for those portions that begin with the next consecutive character until you have found the entire number.

Because of the way "Computer Sort" works it is not necessary to be concerned with the absolute value or number of characters in a part number, just move across the device part number, left to right, one character at a time until you find the number.

Subject Index

This listing is intended to simplify the identification of products where specific device numbers are not known.

(1) The device numbers contained in this index are for reference only and do not necessarily represent the complete device number necessary to order the device. Contact your local Sales Office or Authorized Distributor for complete ordering information.

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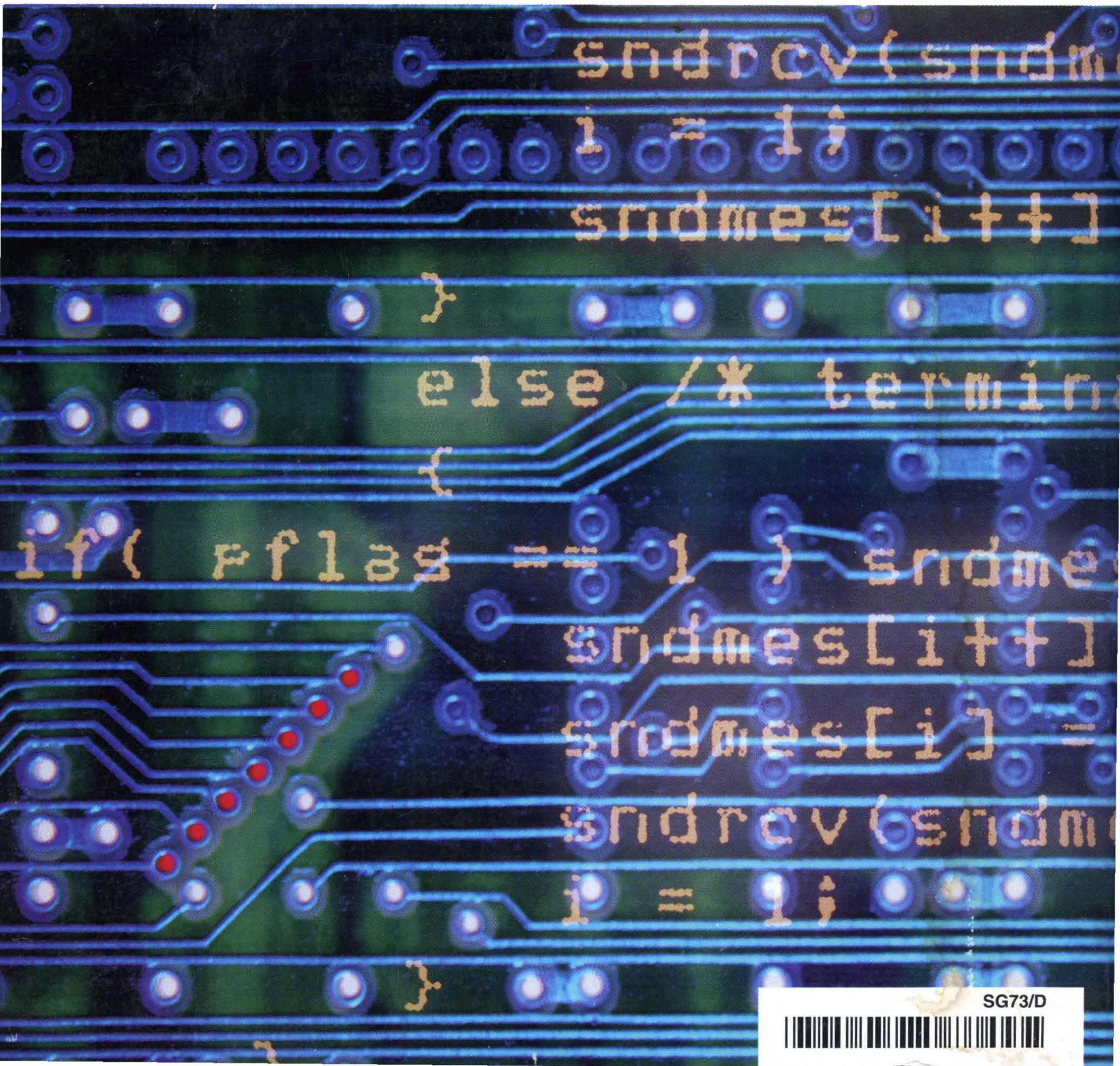

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