Volume 5 / Series B

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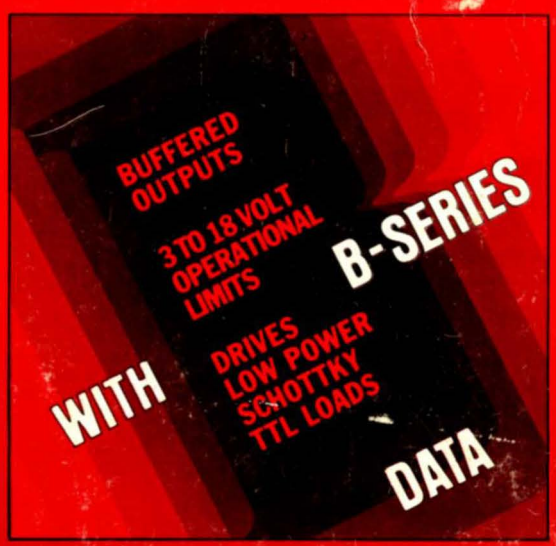

MOTOROLA Semiconductor Products Inc.

Volume 5/Series B

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CMOS INTEGRATED CIRCUITS

This book presents technical data for the broad line of McMOS integrated circuits. Complete specifications are provided in the form of data sheets.

The comprehensive specifications for the B Series reflect the industry specification developed under the auspices of EIA/JEDEC. This coordination permits multiple sources of the B Series of devices.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent right of any manufacturer.

For marketing and application information contact:
CMOS Marketing
Motorola Semiconductor Products Inc.
3501 Ed Bluestein Blvd.
Austin, Texas 78721
(512) 928-2600

Series B
Second Printing

Printed in U.S.A.

CONTENTS

NUMERICAL INDEX

Part Number	Function	Suffix*	Pins	Second Sourced	Page
MC14000	Dual 3-Input NOR Gate plus Inverter	AL,CL,CP	14	✓	5-2
MC14001	Quad 2-Input NOR Gate	AL,CL,CP	14	✓	5-5
MC14001B	Quad 2-Input NOR Gate	AL,CL,CP	14	✓	5-9
MC14002	Dual 4-Input NOR Gate	AL,CL,CP	14	✓	5-14
MC14002B	Dual 4-Input NOR Gate	AL,CL,CP	14	✓	5-14
MC14006B	18-Bit Static Shift Register	AL,CL,CP	14	✓	5-15
MC14007B	Dual Complementary Pair plus Inverter	AL,CL,CP	14	✓	5-19
MC14008B	4-Bit Full Adder	AL,CL,CP	16	✓	5-23
MC14011	Quad 2-Input NAND Gate	AL,CL,CP	14	✓	5-29
MC14011B	Quad 2-Input NAND Gate	AL,CL,CP	14	✓	5-29
MC14012	Dual 4-Input NAND Gate	AL,CL,CP	14	✓	5-30
MC14012B	Dual 4-Input NAND Gate	AL,CL,CP	14	✓	5-30
MC14013B	Dual D Flip-Flop	AL,CL,CP	14	✓	5-31
MC14014B	8-Bit Static Shift Register	AL,CL,CP	16	✓	5-35
MC14015B	Dual 4-Bit Static Shift Register	AL,CL,CP	16	✓	5-39
MC14016B	Quad Analog Switch/Quad Multiplexer	AL,CL,CP	14	✓	5-45
MC14017B	Decade Counter/Divider	AL,CL,CP	16	✓	5-51
MC14018B	Presettable Divide-by-N Counter	AL,CL,CP	16	✓	5-56
MC14020B	14-Bit Binary Counter	AL,CL,CP	16	✓	5-60
MC14021B	8-Bit Static Shift Register	AL,CL,CP	16	✓	5-35
MC14022B	Octal Counter/Divider	AL,CL,CP	16	✓	5-65
MC14023	Triple 3-Input NAND Gate	AL,CL,CP	14	✓	5-70
MC14023B	Triple 3-Input NAND Gate	AL,CL,CP	14	✓	5-70
MC14024B	Seven Stage Ripple Counter	AL,CL,CP	14	✓	5-71
MC14025	Triple 3-Input NOR Gate	AL,CL,CP	14	✓	5-76
MC14025B	Triple 3-Input NOR Gate	AL,CL,CP	14	✓	5-76
MC14027B	Dual J-K Flip-Flop	AL,CL,CP	16	✓	5-77
MC14028B	BCD-to-Decimal Decoder	AL,CL,CP	16	✓	5-81
MC14032B	Triple Serial Adder (Positive Logic)	AL,CL,CP	16	✓	5-86
MC14034B	8-Bit Universal Bus Register	AL,CL,CP	24	✓	5-91
MC14035B	4-Bit Shift Register	AL,CL,CP	16	✓	5-98
MC14038B	Triple Serial Adder (Negative Logic)	AL,CL,CP	16	✓	5-86
MC14040B	12-Bit Binary Counter	AL,CL,CP	16	✓	5-103
MC14042B	Quad Latch	AL,CL,CP	16	✓	5-107
MC14043B	Quad NOR R-S Latch	AL,CL,CP	16	✓	5-111
MC14044B	Quad NAND R-S Latch	AL,CL,CP	16	✓	5-111
MC14046B	Phase-Locked Loop	AL,CL,CP	16	✓	5-115
MC14049B	Hex Inverter/Buffer	AL,CL,CP	16	✓	5-120
MC14050B	Hex Buffer	AL,CL,CP	16	✓	5-120
MC14051B	8-Channel Analog Multiplexer	AL,CL,CP	16	✓	5-124

*Add suffix to part number on all orders.

AL	3 to 18 V, −55 to +125°C, ceramic package
CL	3 to 18 V, −40 to +85°C, ceramic package
CP	3 to 18 V, −40 to +85°C, plastic package
L	Limited voltage range, limited temperature range, ceramic package
P	Limited voltage range, limited temperature range, plastic package
EFL	3 to 18 V, −55 to +125°C, ceramic package
FL	3 to 18 V, −40 to +85°C, ceramic package
FP	3 to 18 V, −40 to +85°C, plastic package
EVL	3 to 6 V, −55 to +125°C, ceramic package
VL	3 to 6 V, −40 to +85°C, ceramic package
VP	3 to 6 V, −40 to +85°C, plastic package
Z	Limited voltage range, limited temperature range, leadless ceramic package

Chips are available for all McMOS types. Consult your Motorola Sales Office or Authorized Motorola Distributor.

NUMERICAL INDEX (continued)

Part Number	Function	Suffix*	Pins	Second Sourced	Page
MC14052B	Dual 4-Channel Analog Multiplexer	AL,CL,CP	16	✓	5-124
MC14053B	Triple 2-Channel Analog Multiplexer	AL,CL,CP	16	✓	5-124
MC14066B	Quad Analog Switch	AL,CL,CP	14	✓	5-130
MC14068B	8-Input NAND Gate	AL,CL,CP	14	✓	5-135
MC14069B	Hex Inverter	AL,CL,CP	14	✓	5-136
MC14070B	Quad Exclusive OR Gate	AL,CL,CP	14	✓	5-138
MC14071	Quad 2-Input OR Gate	AL,CL,CP	14	✓	5-140
MC14071B	Quad 2-Input OR Gate	AL,CL,CP	14	✓	5-140
MC14072B	Dual 4-Input OR Gate	AL,CL,CP	14	✓	5-141
MC14073B	Triple 3-Input AND Gate	AL,CL,CP	14	✓	5-142
MC14075B	Triple 3-Input OR Gate	AL,CL,CP	14	✓	5-143
MC14076B	Quad D-Type Register	AL,CL,CP	16	✓	5-144
MC14077B	Quad Exclusive NOR Gate	AL,CL,CP	14	✓	5-138
MC14078B	8-Input NOR Gate	AL,CL,CP	14	✓	5-149
MC14081	Quad 2-Input AND Gate	AL,CL,CP	14	✓	5-150
MC14081B	Quad 2-Input AND Gate	AL,CL,CP	14	✓	5-150
MC14082B	Dual 4-Input AND Gate	AL,CL,CP	14	✓	5-151
MC14093B	Quad 2-Input NAND Schmitt Trigger	AL,CL,CP	14	✓	5-152
MC14160B	Decade Counter (Asynchronous Clear)	AL,CL,CP	16	✓	5-155
MC14161B	Binary Counter (Asynchronous Clear)	AL,CL,CP	16	✓	5-155
MC14162B	Decade Counter (Synchronous Clear)	AL,CL,CP	16	✓	5-155
MC14163B	Binary Counter (Synchronous Clear)	AL,CL,CP	16	✓	5-155
MC14174B	Hex D Flip-Flop	AL,CL,CP	16	✓	5-163
MC14175B	Quad D Flip-Flop	AL,CL,CP	16	✓	5-167
MC14194B	4-Bit Universal Shift Register	AL,CL,CP	16	✓	5-171
MC14408	Binary-to-Phone Pulse Converter	L,P	16		5-175
MC14409	Binary-to-Phone Pulse Converter	L,P	16		5-175
MC14410	2-of-8 Tone Encoder	L,P	16		5-183
MC14411	Bit-Rate Frequency Generator	L,P	24		5-187
MC14412	Universal Low-Speed Modem	FL,VL	16		5-191
MC14415	Quad Precision Timer/Driver	EFL,FL,FP, EVL,VL,VP	16		5-196
MC14419	2-of-8 Keypad-to-Binary Encoder	L,P	16		5-201
MC14422	Remote Control Transmitter	P	16		4-2
MC14431	12-Bit A/D Converter	L,P	24		4-3
MC14433	3½ Digit A/D Converter	L,P	24		4-4
MC14435	3½ Digit A/D Logic Subsystem	EFL,FL,FP, EVL,VL,VP	16		5-205
MC14440	LCD Watch/Clock Circuit	L,Z	40,36		5-212
MC14450	Oscillator 2^{16} Divider/Buffer	L,P	6		5-216
MC14451	Oscillator/Divider/Buffer	L,P	16		5-220
MC14452	Digitally Trimmed Frequency Divider	P	14		4-5
MC14490	Hex Contact Bounce Eliminator	EFL,FL,FP, EVL,VL,VP	16		5-224
MC14501	Triple Gate	AL,CL,CP	16		5-231
MC14502B	Strobed Hex Inverter/Buffer	AL,CL,CP	16	✓	5-235
MC14503B	Hex 3-State Buffer	AL,CL,CP	16	✓	5-239
MCM14505	64 x 1-Bit Static RAM	AL,CL,CP	14		5-243
MC14506B	Dual Expandable AOI Gate	AL,CL,CP	16		5-252
MC14507	Quad Exclusive OR Gate	AL,CL,CP	14	✓	5-257
MC14508B	Dual 4-Bit Latch	AL,CL,CP	24	✓	5-258
MC14510B	BCD Up/Down Counter	AL,CL,CP	16	✓	5-263
MC14511B	BCD-to-7 Segment Latch/Decoder/Driver	AL,CL,CP	16	✓	5-269

*Suffixes defined on page ii.

NUMERICAL INDEX (continued)

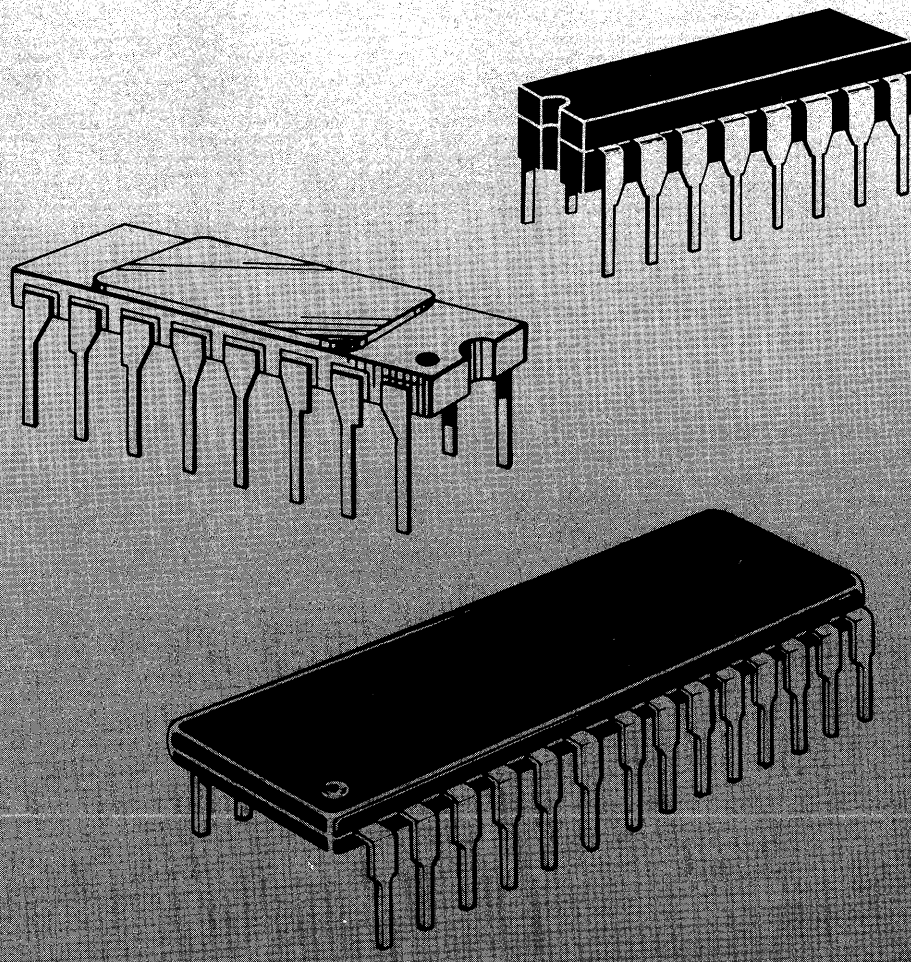
Part Number	Function	Suffix*	Pins	Second Sourced	Page
MC14512	8-Channel Data Selector	AL,CL,CP	16	✓	5-275
MC14514B	4-Bit Latch/4-to-16 Line Decoder (High)	AL,CL,CP	24	✓	5-280
MC14515B	4-Bit Latch/4-to-16 Line Decoder (Low)	AL,CL,CP	24	✓	5-280
MC14516B	Binary Up/Down Counter	AL,CL,CP	16	✓	5-286
MC14517B	Dual 64-Bit Static Shift Register	AL,CL,CP	16	✓	5-292
MC14518B	Dual BCD Up Counter	AL,CL,CP	16	✓	5-296
MC14519B	4-Bit AND/OR Selector	AL,CL,CP	16	✓	5-301
MC14520B	Dual Binary Up Counter	AL,CL,CP	16	✓	5-296
MC14521B	24-Stage Frequency Divider	AL,CL,CP	16		5-306
MC14522B	Programmable BCD Divide-by-N Counter	AL,CL,CP	16	✓	5-312
MCM14524	256 x 4-Bit Read Only Memory	AL,CL,CP	16		5-319
MC14526B	Programmable Binary Divide-by-N Counter	AL,CL,CP	16	✓	5-312
MC14527B	BCD Rate Multiplier	AL,CL,CP	16	✓	5-326
MC14528B	Dual Monostable Multivibrator	AL,CL,CP	16	✓	5-332
MC14529B	Dual 4-Channel Analog Data Selector	AL,CL,CP	16	✓	5-337
MC14530B	Dual 5-Input Majority Logic Gate	AL,CL,CP	16		5-343
MC14531B	12-Bit Parity Tree	AL,CL,CP	16	✓	5-348
MC14532B	8-Bit Priority Encoder	AL,CL,CP	16	✓	5-351
MC14534B	Real Time 5-Decade Counter	AL,CL,CP	24		5-357
MC14536B	Programmable Timer	AL,CL,CP	16		5-363
MCM14537	256 x 1-Bit Static RAM	AL,CL	16		5-370
MC14538B	Dual Precision Monostable Multivibrator	AL,CL,CP	16		5-378
MC14539B	Dual 4-Channel Data Selector/Multiplexer	AL,CL,CP	16		5-381
MC14541B	Programmable Oscillator-Timer	AL,CL,CP	14		5-385
MC14543B	BCD-to-7 Segment Latch/Decoder/Driver	AL,CL,CP	16	✓	5-391
MC14549B	Successive Approximation Register	AL,CL,CP	16		5-396
MCM14552	64 x 4-Bit Static RAM	AL,CL,CP	24		5-403
MC14553B	3-Digit BCD Counter	AL,CL,CP	16		5-410
MC14554B	2 x 2-Bit Parallel Binary Multiplier	AL,CL,CP	16		5-416
MC14555B	Dual Binary to 1-of-4 Decoder	AL,CL,CP	16	✓	5-420
MC14556B	Dual Binary to 1-of-4 Decoder (Inverting)	AL,CL,CP	16	✓	5-420
MC14557B	1-to-64-Bit Variable Length Shift Register	AL,CL,CP	16		5-423
MC14558B	BCD-to-7 Segment Decoder	AL,CL,CP	16		5-427
MC14559B	Successive Approximation Register	AL,CL,CP	16		5-396
MC14560B	NBCD Adder	AL,CL,CP	16		5-433
MC14561B	9's Complementer	AL,CL,CP	14		5-437
MC14562B	128-Bit Static Shift Register	AL,CL,CP	14		5-443
MC14566B	Industrial Time Base Generator	AL,CL,CP	16		5-447
MC14568B	Phase Comparator/Programmable Counter	AL,CL,CP	16		5-453
MC14569B	Dual Programmable BCD/Binary Counter	AL,CL,CP	16		5-461
MC14572	Hex Gate	AL,CL,CP	16		5-466
MC14580B	4 x 4 Multiport Register	AL,CL,CP	24	✓	5-469
MC14581B	4-Bit Arithmetic Logic Unit	AL,CL,CP	24	✓	5-474
MC14582B	Look-Ahead Carry Block	AL,CL,CP	16	✓	5-479
MC14583B	Dual Schmitt Trigger	AL,CL,CP	16		5-483
MC14584B	Hex Schmitt Trigger	AL,CL,CP	14		5-489
MC14585B	4-Bit Magnitude Comparator	AL,CL,CP	16	✓	5-492
MCM14505	64-Bit Static Random Access Memory	AL,CL,CP	14		5-243
MCM14524	1024-Bit Read Only Memory	AL,CL,CP	16		5-319
MCM14537	256-Bit Static Random Access Memory	AL,CL	16		5-370
MCM14552	256-Bit Static Random Access Memory	AL,CL,CP	24		5-403

NMOS Devices Designed to work with the MC14422 CMOS device:

MC6525	Remote Control Receiver	P	28		4-6
MC6526	Remote Control Receiver	P	28		4-7

*Suffixes defined on page ii.

Device Function Index/Chapter 1



1

McMOS SELECTION GUIDE BY FUNCTION

McMOS SELECTION GUIDE BY FUNCTION (continued)

1

Inverters/Buffers

Decoders/Encoders

Display Decoders

Multiplexers/Demultiplexers/Bilateral Switches

Schmitt Triggers

Flip-Flops/Latches

McMOS SELECTION GUIDE BY FUNCTION (continued)

Shift Registers

Counters

Oscillators/Timers

Phase-Locked Loops

Multivibrators

McMOS SELECTION GUIDE BY FUNCTION (continued)

Adders/Comparators

ALU Rate Multipliers

Parity Checker

Memories

Communications/Telephone Functions

A/D Converter/Logic Functions

Other Complex Functions

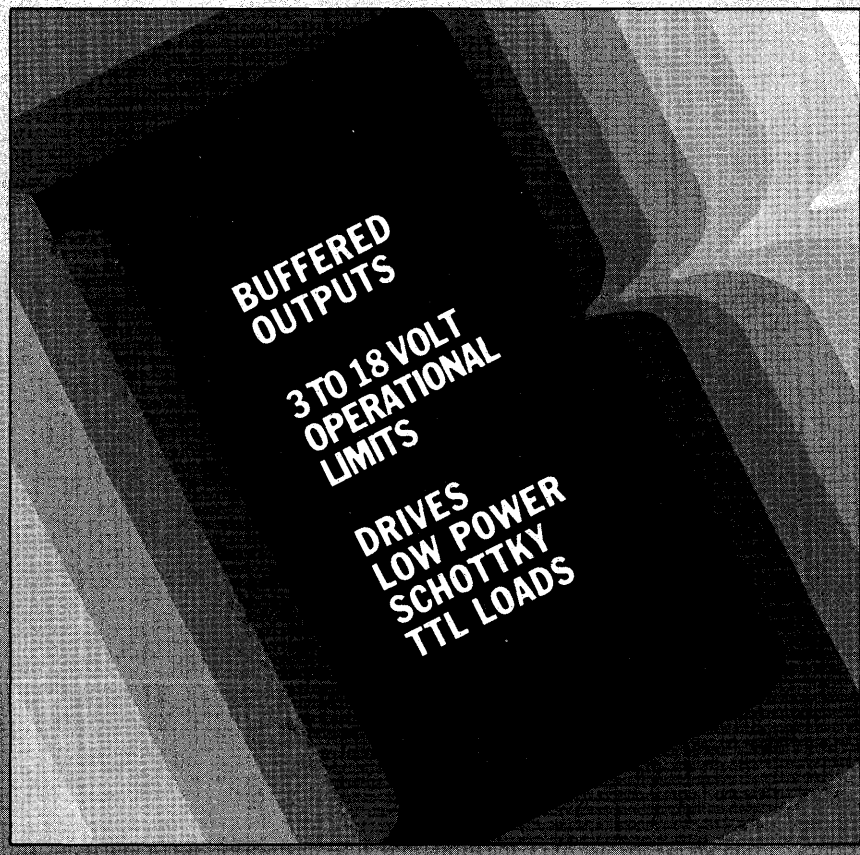
SUMMARY OF MOTOROLA CMOS LINE

Gates						Flip-Flops/ Latches	Multi-vibrators
Single-Level			Multi-Level				
NOR/NAND	OR/AND	Buffers & Inverters	Multifunction/ AOI	Decoders/ Encoders	Schmitt Triggers		
MC14000	MC14071	MC14007B	MC14070B	MC14028B	MC14093B	MC14013B	MC14528B
MC14001	MC14071B	MC14049B	MC14077B	MC14514B	MC14583B	MC14027B	MC14538B
MC14001B	MC14072B	MC14050B	MC14506B	MC14515B	MC14584B	MC14042B	
MC14002	MC14073B	MC14069B	MC14507	MC14532B		MC14043B	
MC14002B	MC14075B	MC14502B	MC14519B	MC14555B		MC14044B	
MC14011	MC14081	MC14503B	MC14530B	MC14556B		MC14076B	
MC14011B	MC14081B					MC14174B	
MC14012	MC14082B					MC14175B	
MC14012B						MC14508B	
MC14023							
MC14023B							
MC14025							
MC14025B							
MC14068B							
MC14078B							
MC14501							
MC14572							

Shift Registers	Counters			Phase-Locked Loop	Memories		
	Ripple	Synchronous	Oscillators & Timers		Multiport Register	RAMs	ROMs
MC14006B	MC14020B	MC14017B	MC14450	MC14046B	MC14580B	MCM14505	MCM14524
MC14014B	MC14024B	MC14018B	MC14451	MC14568B		MCM14537	
MC14015B	MC14040B	MC14022B	MC14452			MCM14552	
MC14021B	MC14534B	MC14160B	MC14521B				
MC14034B	MC14566B	MC14161B	MC14536B				
MC14035B		MC14162B	MC14541B				
MC14194B		MC14163B					
MC14517B		MC14510B					
MC14557B		MC14516B					
MC14562B		MC14518B					
		MC14520B					
		MC14522B					
		MC14526B					
		MC14553B					
		MC14569B					

Multiplexers/ Demultiplexers, Bilateral Switches	Display Drivers/ Encoders	Arithmetic Circuits			Communication/ Telephone	A/D Converters	Other Complex Functions
		Adders/ Comparators	ALU/Rate Multipliers	Parity Generator/ Checker			
MC14016B	MC14511B	MC14008B	MC14527B	MC14531B	MC14408	MC14431	MC14415
MC14051B	MC14543B	MC14032B	MC14554B		MC14409	MC14433	MC14422
MC14052B	MC14558B	MC14038B	MC14581B		MC14410	MC14435	MC14440
MC14053B		MC14560B			MC14411	MC14549B	MC14490
MC14066B		MC14561B			MC14412	MC14559B	
MC14512		MC14582B			MC14419		
MC14519B		MC14585B					
MC14529B							
MC14539B							

B-Series Family Data/Chapter 2



2

B-SERIES FAMILY DATA

The CMOS Devices in this volume which have a B suffix meet the minimum values for the industry-standardized* family specification for the B Series. These standardized values are shown in the Maximum Ratings and Electrical Characteristics Tables.

The B-Series devices are compatible with the other devices in the CMOS product line. Features include:

- **All buffered outputs**
- **3–18 volt operational limits**
- **Capable of driving two low-power TTL loads, one low-power Schottky TTL load, or two HTL loads over the rated temperature range**
- **Maximum input current of ±1 μA at 15 volt power supply over the temperature range**
- **Parameters specified at 5.0, 10, and 15 volt supply**
- **Noise margins of 1.0 V min @ 5.0 V supply**
  2.0 V min @ 10 V supply
  2.5 V min @ 15 V supply

For the industry-standardized B series, the maximum ratings and recommended operating range are shown at the bottom of this page. The industry-standardized limits for the static characteristics are shown in two formats: Table 1 is in the industry format and Table 2 is in the equivalent Motorola format. The Motorola format is used throughout this data book. Additional specification values are shown on the individual data sheets.

Switching characteristics for the B-series devices are specified under the following conditions:

Load Capacitance, C_L, of 50 pF

Input pulse voltage equal to $+V_{DD}$ supply voltage

Input pulse rise and fall times of 20 ns

Propagation Delay times measured from 50% point of input voltage to 50% point of output voltage

Three different supply voltages: 5, 10, and 15 V

Exceptions to the B-Series Family Specification

There are a number of devices which have a B suffix whose input and/or outputs vary somewhat from the B-Series family specification because of functional requirements. Some categories of notable exceptions are:

Inverting buffers with only one stage of buffering do not meet the input voltage specification.

Devices with specialized outputs on the chip, such as NPN emitter-follower drivers or transmission gates, do not meet output specifications.

Devices with specialized inputs, such as oscillator inputs, have unique input specifications.

Input Voltage

The input voltage specification is interpreted as the worst-case input voltage to produce an output level of "1" or "0". The "1" or "0" output level is defined as a deviation from the supply (V_{DD}) and ground (V_{SS}) levels. For a 5.0 V supply, this deviation is 0.5 V; for a 10 V supply, 1.0 V; and for 15 V, 1.5 V. As an example, in a device operating at a 5.0 V supply, the device with the input starting at ground is guaranteed to switch on or before 3.5 V and not to switch up to 1.5 V. Switching and not switching are defined as within 0.5 V of the ideal output level for the example with a 5.0 V supply. The actual switching level referred to the input is between 1.5 V and 3.5 V.

Noise Margin

The values for input voltage and the given defined output deviation lead to minimum noise margins of 1.0 V, 2.0 V, and 2.5 V for a 5.0 V, 10 V, and 15 V supply, respectively.

Output Drive Current

Devices in the B Series are capable of sinking a minimum of 0.36 mA over the temperature range with a 5.0 V supply. This value guarantees that these CMOS devices will drive Schottky low-power TTL inputs which require 0.36 mA maximum over the temperature range.

Compatibility

Other devices in the CMOS line not labeled with the B suffix also have 3.0 to 18 volt operating limits. These devices are fully compatible with B-Series devices over the full voltage range. Notable in this group is a series of eight gates available in non-buffered (numbered without the B suffix) and buffered designs (B suffix on the part number).

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING RANGE

DC Supply Voltage	V_{DD}	+3.0 to +15	Vdc

*Specifications coordinated by EIA/JEDEC Solid-State Products Council.

TABLE 1 – INDUSTRY FORMAT FOR CMOS INDUSTRY B-SERIES SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

PARAMETER		TEMP RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS							UNITS
					T_{LOW}*		+25°C			T_{HIGH}*		
					Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current											
	GATES		5			0.25			0.25		7.5	
		Mil	10	$V_{IN} = V_{SS}$ or V_{DD}		0.5			0.5		15	µAdc
			15			1.0			1.0		30	
			5	All valid input		1.0			1.0		7.5	
		Comm	10	combinations		2.0			2.0		15	µAdc
			15			4.0			4.0		30	
	BUFFERS, FLIP-FLOPS		5			1.0			1.0		30	
		Mil	10	$V_{IN} = V_{SS}$ or V_{DD}		2.0			2.0		60	µAdc
			15			4.0			4.0		120	
			5	All valid input		4			4.0		30	
		Comm	10	combinations		8			8.0		60	µAdc
			15			16			16.0		120	
	MSI		5			5			5		150	
		Mil	10	$V_{IN} = V_{SS}$ or V_{DD}		10			10		300	µAdc
			15			20			20		600	
			5	All valid input		20			20		150	
		Comm	10	combinations		40			40		300	µAdc
			15			80			80		600	
V_{OL}	Low-Level Output Voltage		5			0.05			0.05		0.05	
		All	10	$V_{IN} = V_{SS}$ or V_{DD}		0.05			0.05		0.05	Vdc
			15	$\|I_O\| < 1\mu A$		0.05			0.05		0.05	
V_{OH}	High-Level Output Voltage		5		4.95		4.95			4.95		
		All	10	$V_{IN} = V_{SS}$ or V_{DD}	9.95		9.95			9.95		Vdc
			15	$\|I_O\| < 1\mu A$	14.95		14.95			14.95		
V_{IL}	Input Low Voltage		5	$V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	
		All	10	$V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	Vdc
			15	$V_O = 1.5V$ or $13.5V$ $\|I_O\| < 1\mu A$		4.0			4.0		4.0	
V_{IH}	Input High Voltage		5	$V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		
		All	10	$V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		Vdc
			15	$V_O = 1.5V$ or 13.5 V $\|I_O\| < 1\mu A$	11.0		11.0			11.0		
I_{OL}	Output Low (Sink) Current		5	$V_O = 0.4V$, $V_{IN} = 0$ or $5V$	0.64		0.51			0.36		
		Mil	10	$V_O = 0.5V$, $V_{IN} = 0$ or $10V$	1.6		1.3			0.9		mAdc
			15	$V_O = 1.5V$, $V_{IN} = 0$ or $15V$	4.2		3.4			2.4		
			5	$V_O = 0.4V$, $V_{IN} = 0$ or $5V$	0.52		0.44			0.36		
		Com	10	$V_O = 0.5V$, $V_{IN} = 0$ or $10V$	1.3		1.1			0.9		mAdc
			15	$V_O = 1.5V$, $V_{IN} = 0$ or $15V$	3.6		3.0			2.4		
I_{OH}	Output High (Source) Current		5	$V_O = 4.6V$, $V_{IN} = 0$ or $5V$	−0.25		−0.2			−0.14		
		Mil	10	$V_O = 9.5V$, $V_{IN} = 0$ or $10V$	−0.62		−0.5			−0.35		mAdc
			15	$V_O = 13.5V$, $V_{IN} = 0$ or $15V$	−1.8		−1.5			−1.1		
			5	$V_O = 4.6V$, $V_{IN} = 0$ or $5V$	−0.2		−0.16			−0.12		
		Com	10	$V_O = 9.5V$, $V_{IN} = 0$ or $10V$	−0.5		−0.4			−0.3		mAdc
			15	$V_O = 13.5V$, $V_{IN} = 0$ or $15V$	−1.4		−1.2			−1.0		
I_{IN}	Input Current	Mil	15	$V_{IN} = 0$ or $15V$		±0.1			±0.1		±1.0	µAdc
		Comm	15	$V_{IN} = 0$ or $15V$		±0.3			±0.3		±1.0	µAdc
C_{IN}	Input Capacitance per unit load	All	–	Any Input					7.5			pF

*T_{LOW} = −55°C for Military temperature range device, −40°C for Commercial temperature range device.
T_{HIGH} = +125°C for Military temperature range device, +85°C for Commercial temperature range device.

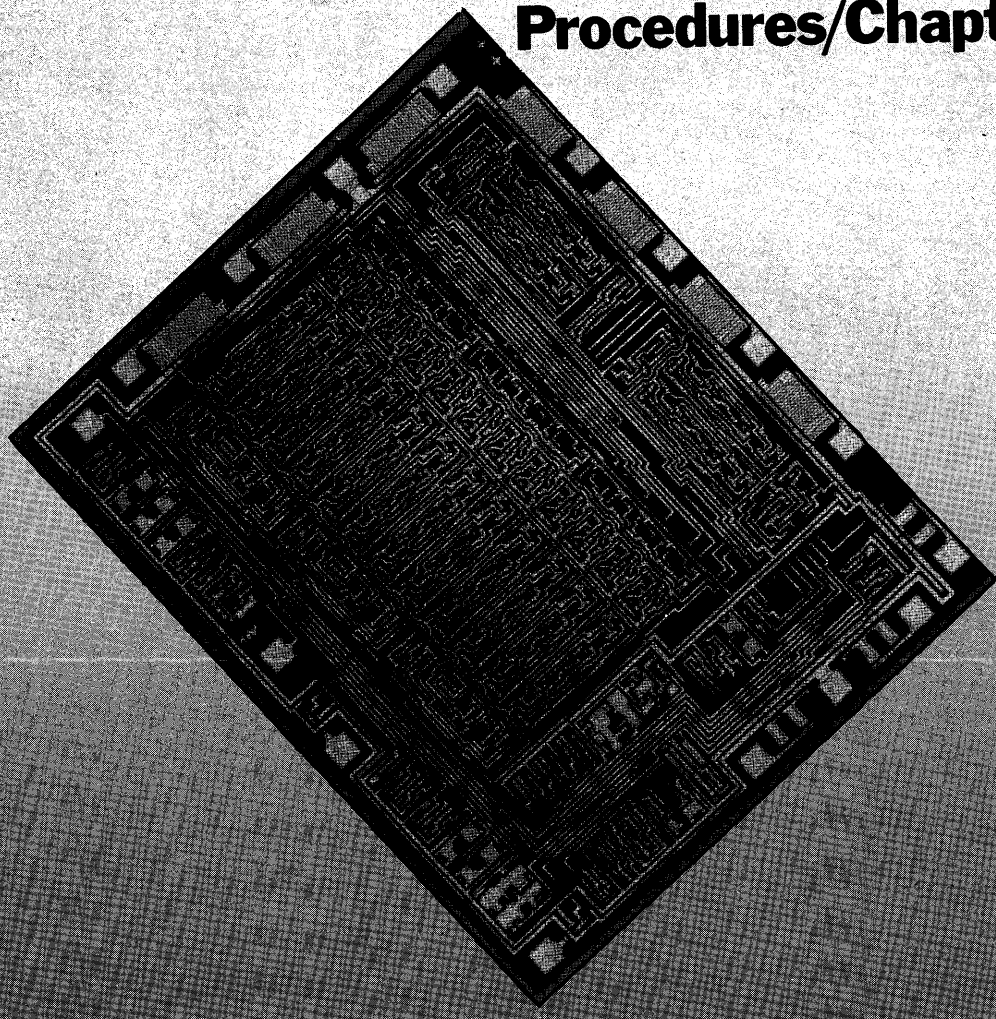
TABLE 2 – MOTOROLA FORMAT FOR CMOS INDUSTRY B-SERIES SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0.05	–	0.05	
		15	–	0.05	–	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	–	9.95	–	
		15	14.95	–	14.95	–	14.95	–	
Input Voltage # "0" Level	V_{IL}								Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	4.0	–	4.0	
"1" Level	V_{IH}								Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}								mAdc
(V_{OH} = 4.6 Vdc) Source		5.0	–0.25	–	–0.2	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}								mAdc
(V_{OH} = 4.6 Vdc) Source		5.0	–0.2	–	–0.16	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	7.5	–	–	pF
Gate Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.25	–	7.5	µAdc
		10	–	0.5	–	0.5	–	15	
		15	–	1.0	–	1.0	–	30	
(CL/CP Device)	I_{DD}	5.0	–	1.0	–	1.0	–	7.5	µAdc
		10	–	2.0	–	2.0	–	15	
		15	–	4.0	–	4.0	–	30	
Flip-Flop and Buffer Quiescent Current (Per Package) (AL Device)	I_{DD}	5.0	–	1.0	–	1.0	–	30	µAdc
		10	–	2.0	–	2.0	–	60	
		15	–	4.0	–	4.0	–	120	
(CL/CP Device)	I_{DD}	5.0	–	4.0	–	4.0	–	30	µAdc
		10	–	8.0	–	8.0	–	60	
		15	–	16	–	16	–	120	
MSI Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	5.0	–	150	µAdc
		10	–	10	–	10	–	300	
		15	–	20	–	20	–	600	
(CL/CP Device)	I_{DD}	5.0	–	20	–	20	–	150	µAdc
		10	–	40	–	40	–	300	
		15	–	80	–	80	–	600	
LSI Quiescent Current	I_{DD}	See Individual Data Sheets.							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

Reliability and Handling Procedures/Chapter 3



McMOS RELIABILITY AND DEVICE HANDLING PROCEDURES

Confident use of a family of components requires assurance of the reliability of a component under normal operating conditions and the ability of the device to survive abnormal conditions that may occur. CMOS, and specifically Motorola McMOS, has achieved the high confidence level for equipment usage that has been enjoyed by many other semiconductor products.

RELIABILITY

Figure 1 shows the composite failure rate of commercial ceramic and plastic packaged McMOS integrated circuits as a function of temperature. Note that CMOS devices dissipate little power and work nominally close to ambient temperature. This feature adds to CMOS reliability. The data shown represent over 40 million equivalent device hours and give failure rates to the factory set of test limits. This standard of failure is more severe than a catastrophic failure rate.

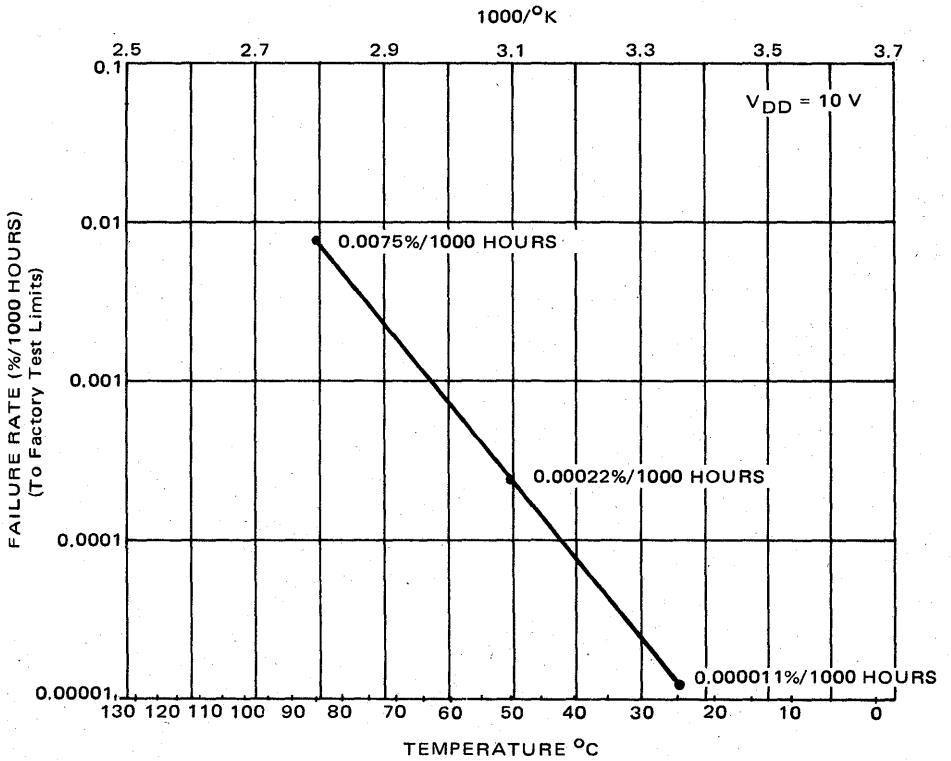
For a more detailed discussion of McMOS reliability, see Chapter 6.

HANDLING PRECAUTIONS

All McMOS devices have diode input protection against adverse electrical environments such as static discharge. The following statement is included on each data sheet:

> This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.
>
> Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – FAILURE RATE OF COMMERCIAL McMOS INTEGRATED CIRCUITS (Ceramic and Plastic Packaged Devices)



Unfortunately, there can be severe electrical environments during the process of handling. For example, static voltages generated by a person walking across a common waxed floor have been measured in the 4 to 15 kV range (depending on humidity, surface conditions, etc.). These static voltages are potentially disastrous when discharged into a CMOS input considering the energy stored in the capacity (≈300 pF) of the human body at these voltage levels.

Present McMOS gate protection structures can generally protect against overvoltages. This is usually sufficient except in the severe cases. Following are some suggested handling procedures for McMOS devices, many of which apply to most semiconductor devices.

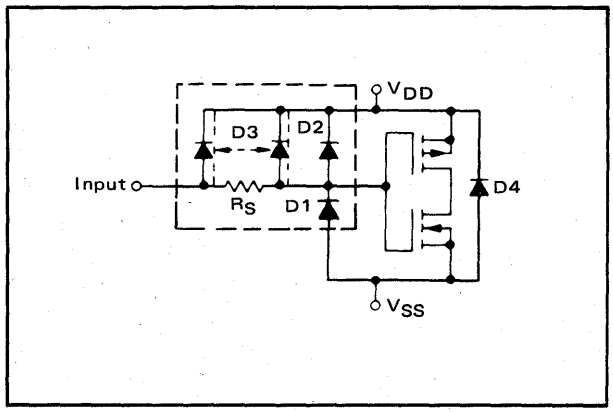
1. All MOS devices should be stored or transported in materials that are somewhat conductive. MOS devices must not be inserted into conventional plastic "snow" or plastic trays.
2. All MOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface.
3. Nylon clothing should not be worn while handling MOS circuits.
4. Do not insert or remove MOS devices from test sockets with power applied. Check all power supplies to be used for testing MOS devices to be certain there are no voltage transients present.
5. When lead straightening or hand soldering is necessary, provide ground straps for the apparatus used.
6. Do not exceed the maximum electrical voltage ratings specified by the data sheet.
7. Double check test equipment setup for proper polarity of voltage before conducting parametric or functional testing.
8. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material.
9. All unused device inputs should be connected to V_{DD} or V_{SS}.

When external connections to a PC board address only an input to a CMOS integrated circuit, it is recommended that a resistance 10 kΩ or greater be used in series with the input. This resistor will limit accidental damage if the PC board is removed and wiped across plastic, nylon carpet or inserted into statically charged plastic "snow".

The input protection circuit, while adding some delay time, provides protection by clamping positive and negative potentials to V_{DD} and V_{SS}, respectively. Figure 2 shows the internal circuitry for the diode-resistor protection.

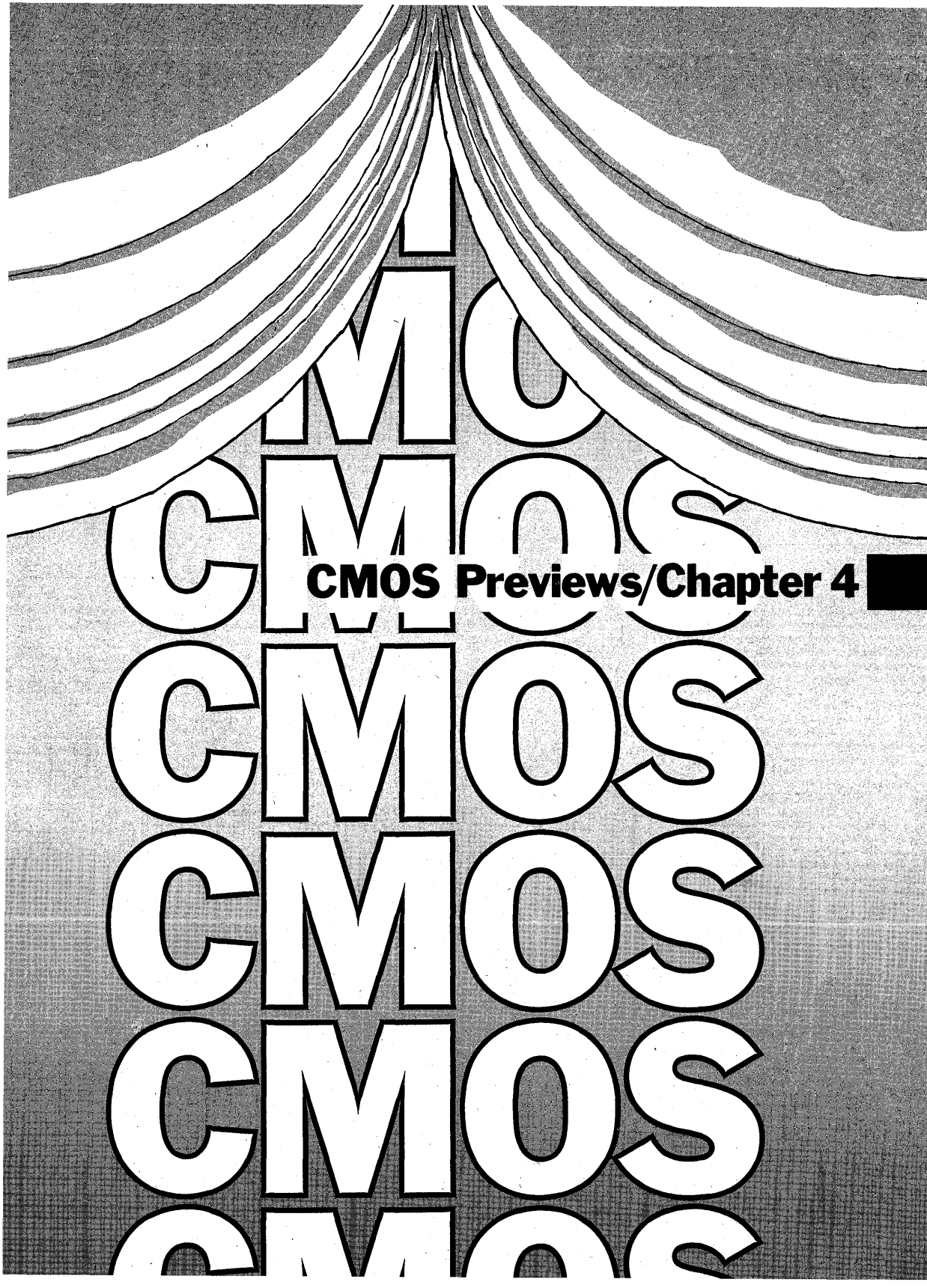
The input protection circuit consists of a series isolation resistor R_S, whose typical value is 1.5 kΩ, and diodes D1 and D2, which clamp the input voltages between the power supply pins V_{DD} and V_{SS}. Diode D3 is a distributed structure resulting from the diffusion fabrication of R_S.

FIGURE 2 – SCHEMATIC DIAGRAM, DIODE-RESISTOR INPUT PROTECTION



All present Motorola integrated circuits have the above diode protection with the exception of the MC14049 and MC14050.

3


CMOS Previews/Chapter 4

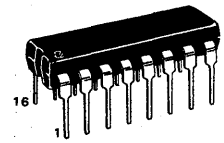
MC14422P

REMOTE CONTROL TRANSMITTER

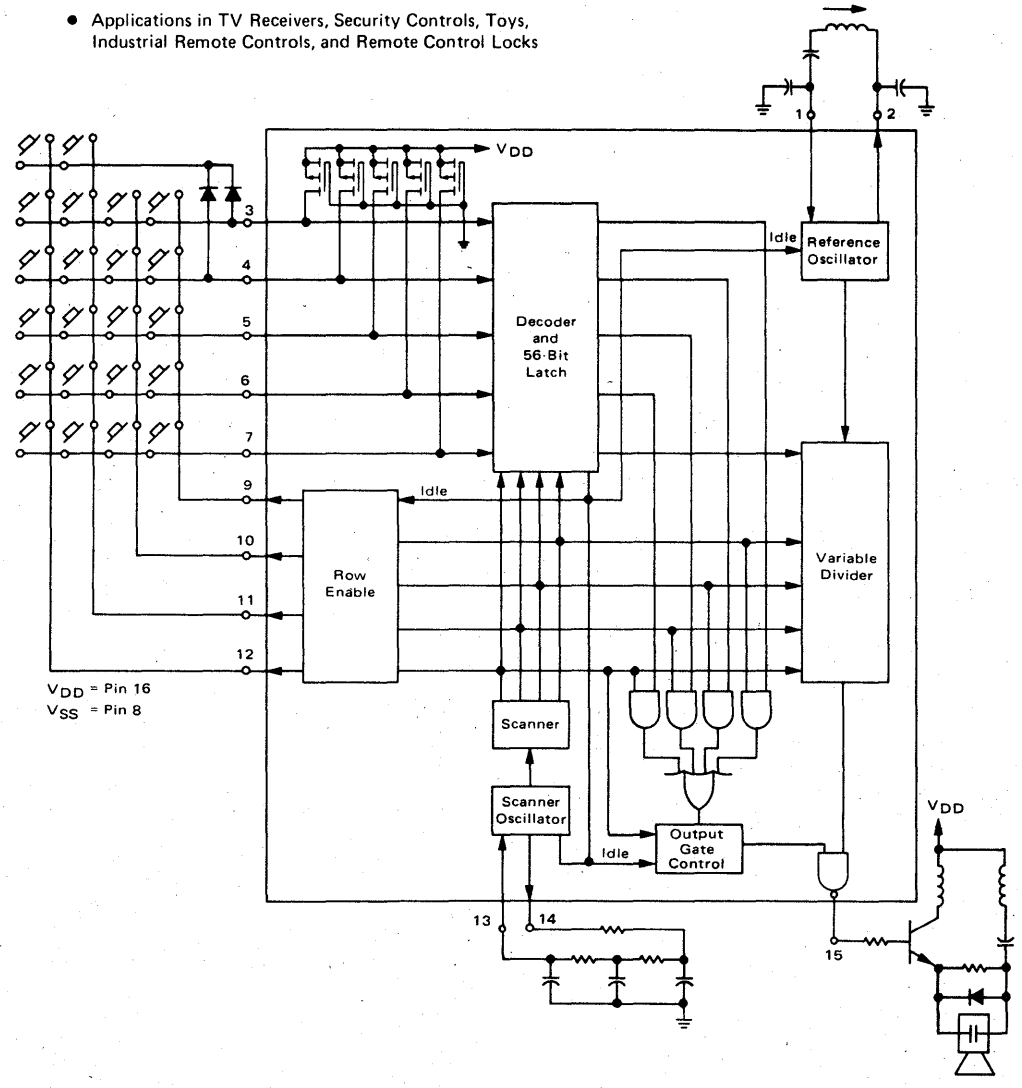
McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

- 22 Channel Capacity
- Transmission of Information Is Achieved by Time Multiplexing Five Frequencies
- No Possibility of Doppler Effect Interference
- Extremely Low External Component Count
- Low Power Consumption
- Designed for Use with the MC6525 and MC6526 Remote Control Receivers
- Applications in TV Receivers, Security Controls, Toys, Industrial Remote Controls, and Remote Control Locks



PLASTIC PACKAGE
CASE 648



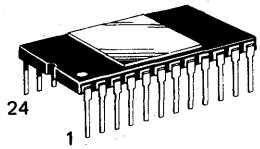
MC14431

12-BIT BINARY A/D CONVERTER DIGITAL SUBSYSTEM

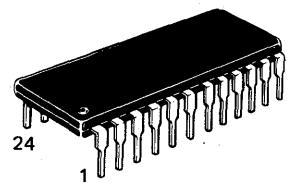
- On-Chip Clock
- Non-Multiplexed Binary Output
- System Overrange Output
- On-Chip Auto Polarity Sensor

McMOS LSI

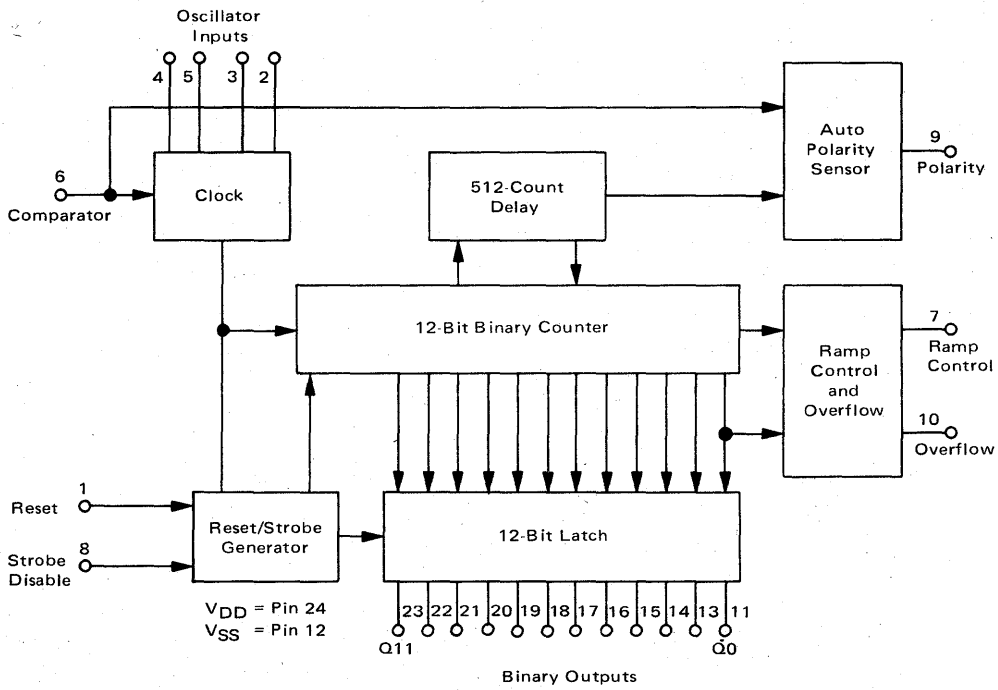
(LOW-POWER COMPLEMENTARY MOS)



L SUFFIX
CERAMIC PACKAGE
CASE 716



P SUFFIX
PLASTIC PACKAGE
CASE 709



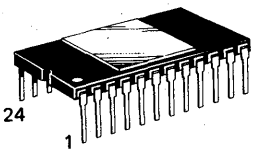
MC14433

3½ DIGIT A/D CONVERTER

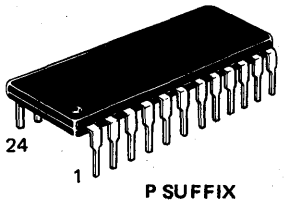
- Single Chip A/D Converter
- Auto Polarity
- Auto Zero
- $Z_{in} > 1000\ M\Omega$
- Single Positive Voltage Reference
- Low External Parts Count

McMOS LSI

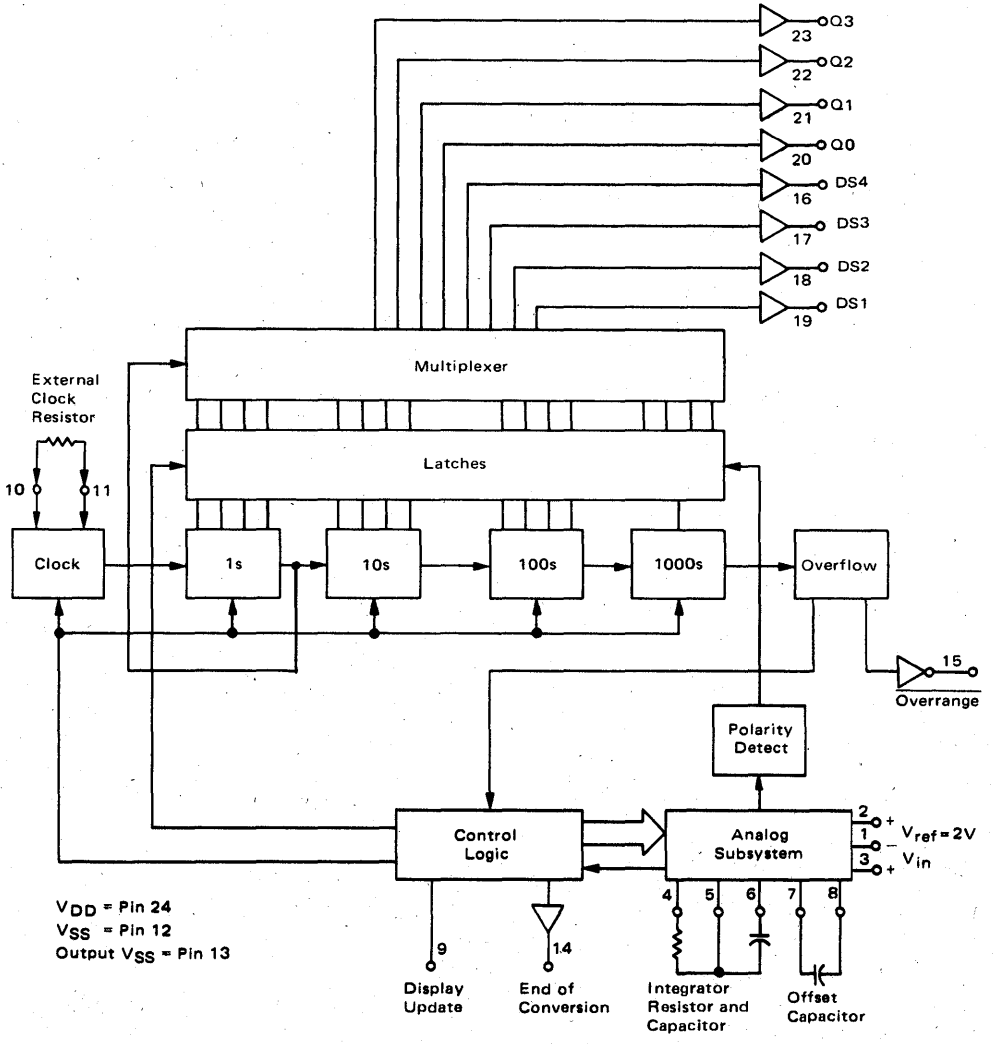
(LOW-POWER COMPLEMENTARY MOS)



L SUFFIX
CERAMIC PACKAGE
CASE 716



P SUFFIX
PLASTIC PACKAGE
CASE 709



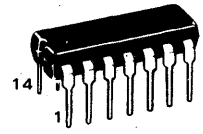
MC14452P

DIGITALLY TRIMMED FREQUENCY DIVIDER

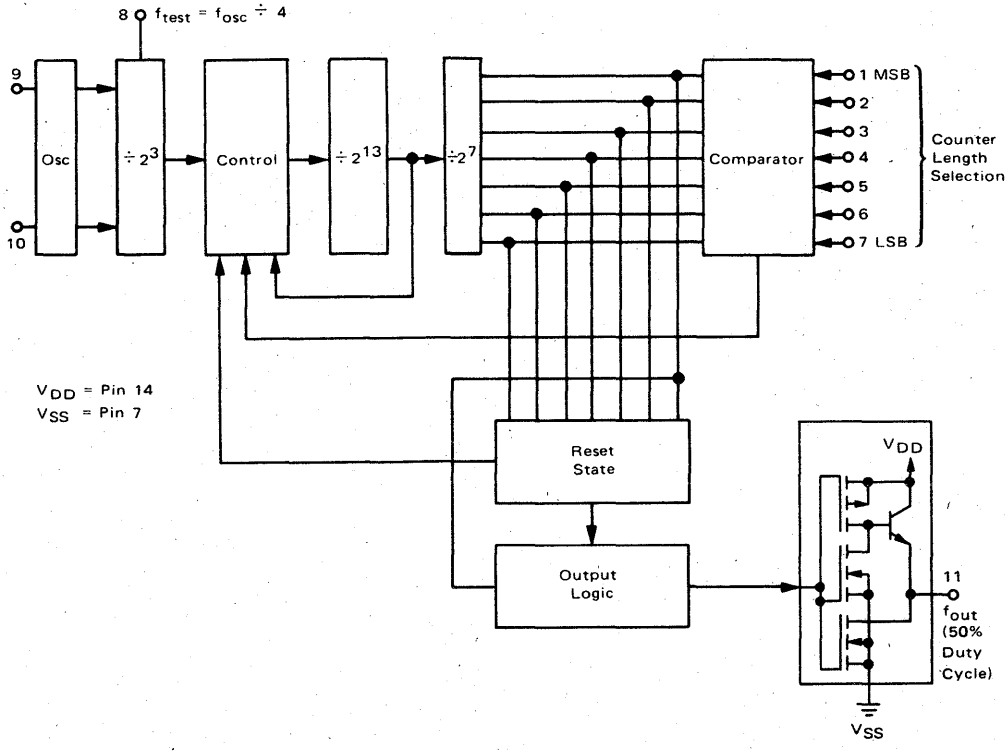
McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

- Count Range = $2^{23} - 2^{3n}$, where n = 0 to 127
- Output Drive Current = 15 mA @ V_{DD} = 6 Vdc
- For 0.5 Hz Output:
  4.194304 to 4.195320 Hz Input
  Recommended crystal frequency =
  4.194812 Hz ± 0.00012%
  Can be trimmed with MC14452 to
  ±0.0000019%



PLASTIC PACKAGE
CASE 646



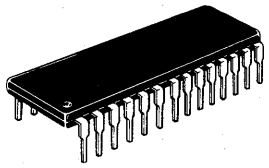
MC6525P

REMOTE CONTROL RECEIVER

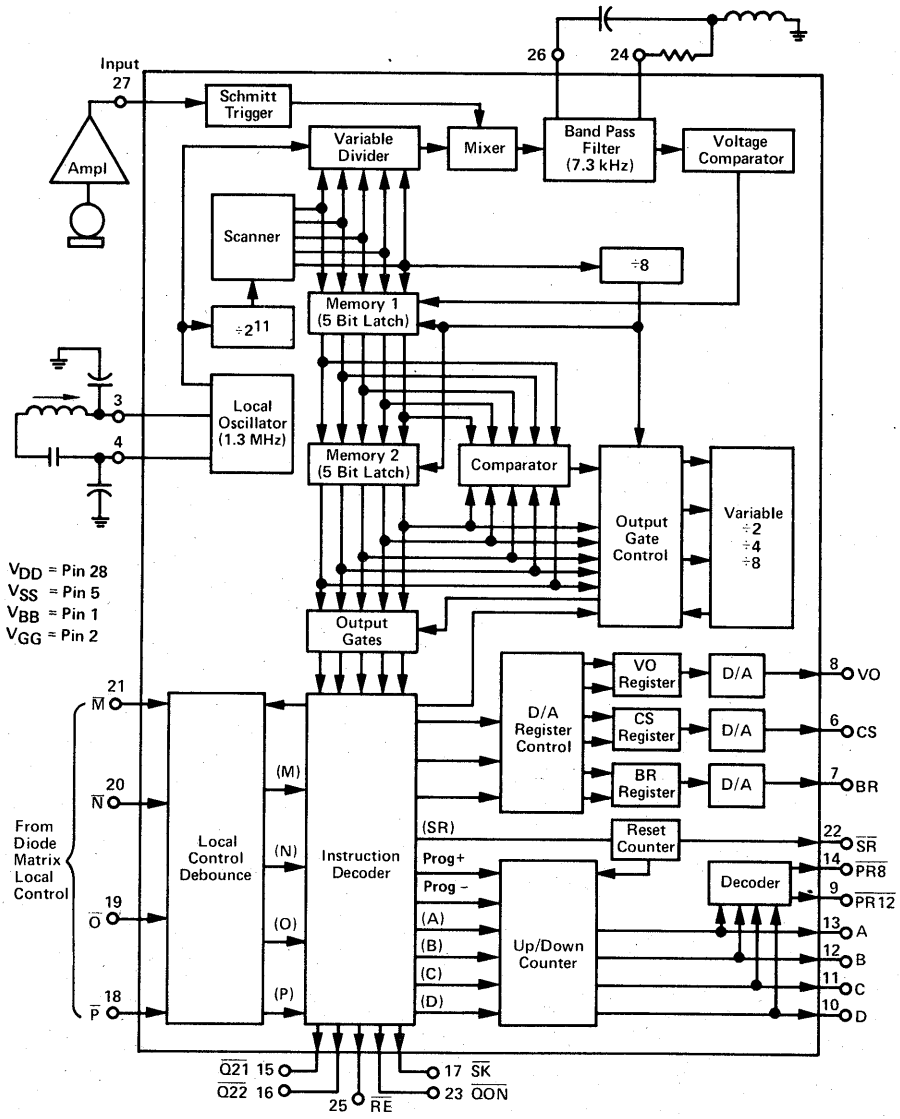
MOS

(N-CHANNEL, METAL GATE)

- Binary-Coded Output to Address 12 Programs
- High Input Sensitivity – 250 mV rms
- Good Noise Immunity — Input Multiplex Signal Read Repetitively Up to Eight Times
- Internal Up/Down Counter for Program Sequencing
- Designed for Use with the MC14422 Remote Control Transmitter



PLASTIC PACKAGE
CASE 710



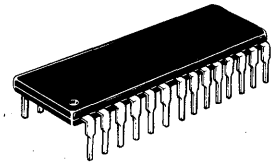
MC6526P

REMOTE CONTROL RECEIVER

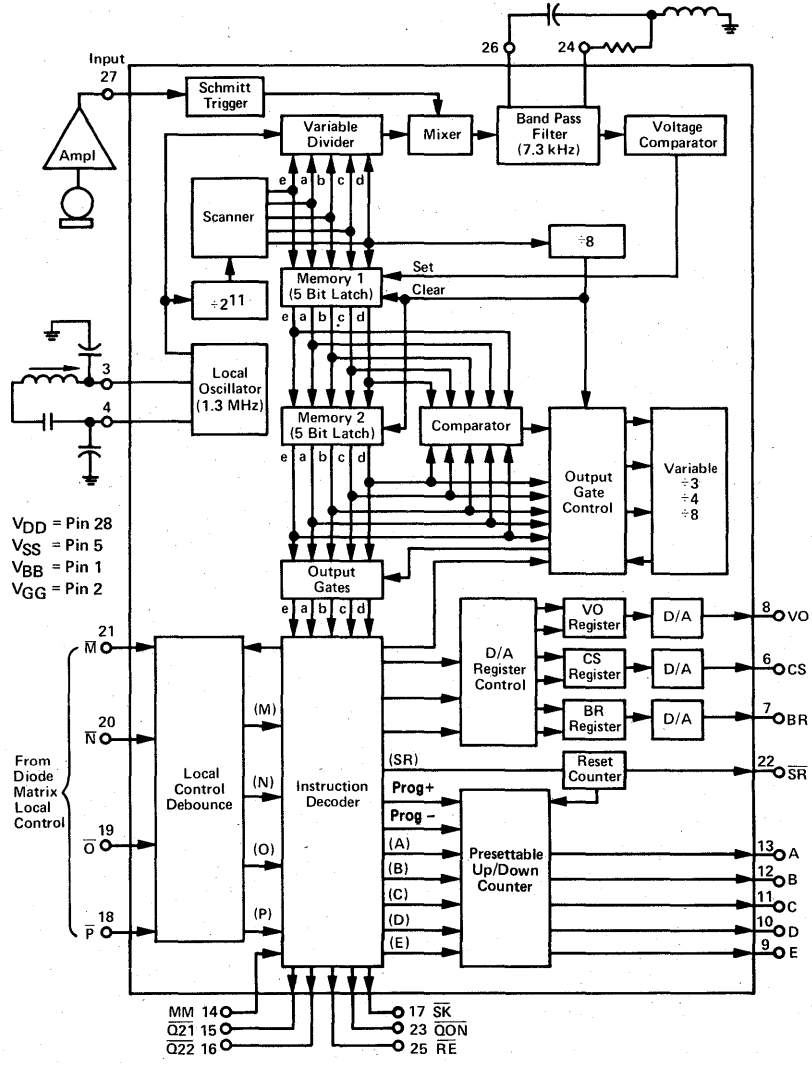
MOS

(N-CHANNEL, METAL GATE)

- Binary-Coded Output to Address 32, 16, or 8 Programs
- High Input Sensitivity—250 mV rms
- Good Noise Immunity—Input Multiplex Signal Read Repetitively up to Eight Times
- Internal Up/Down Counter for Program Sequencing
- Designed for Use with the MC14422 Remote Control Transmitter



PLASTIC PACKAGE
CASE 710



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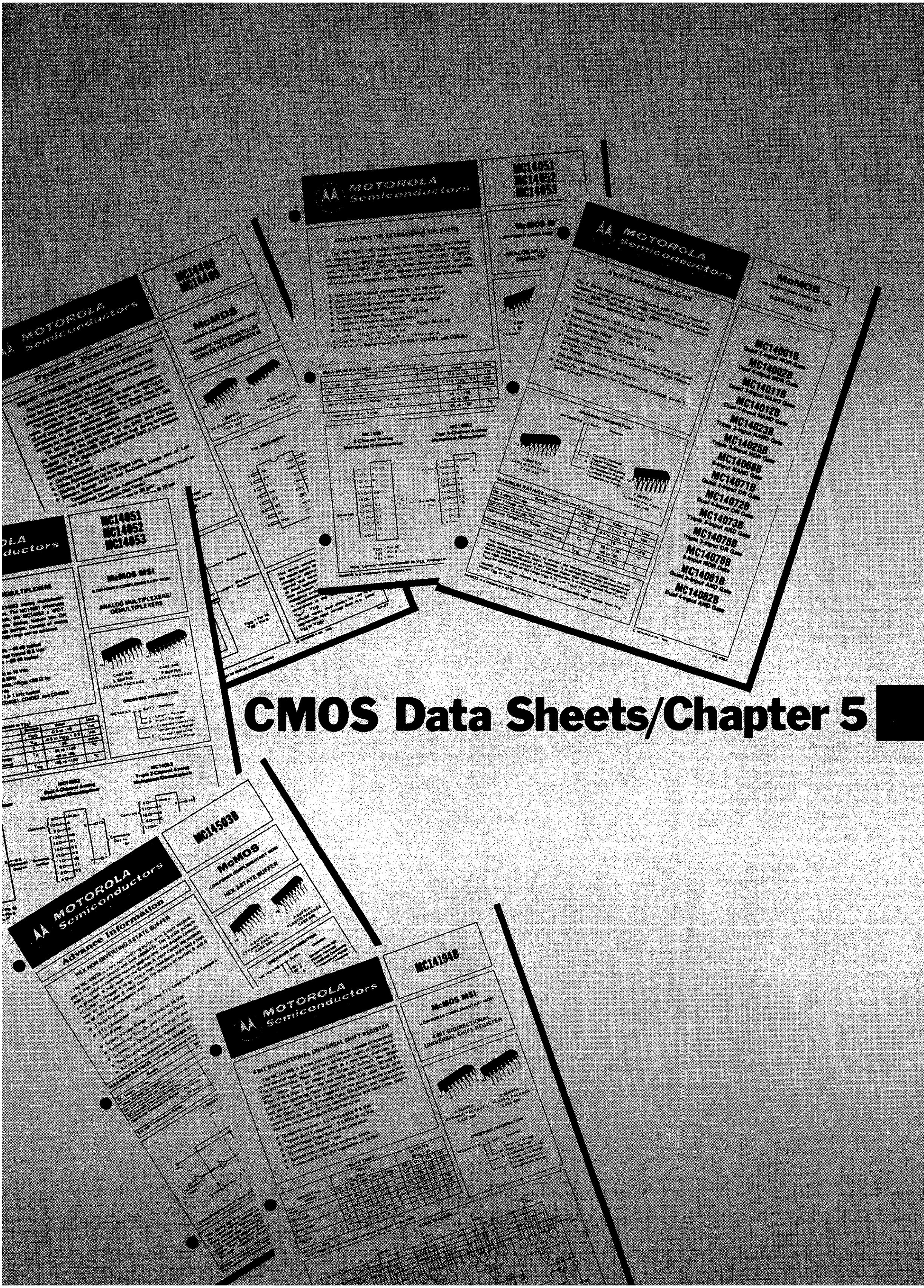


CMOS Data Sheets/Chapter 5

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14000

DUAL 3-INPUT "NOR" GATE PLUS INVERTER

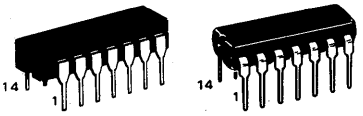
The MC14000 dual 3-input NOR gate plus inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4000

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 3-INPUT "NOR" GATE PLUS INVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

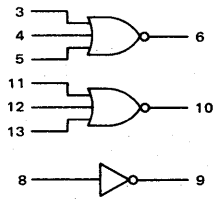
ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

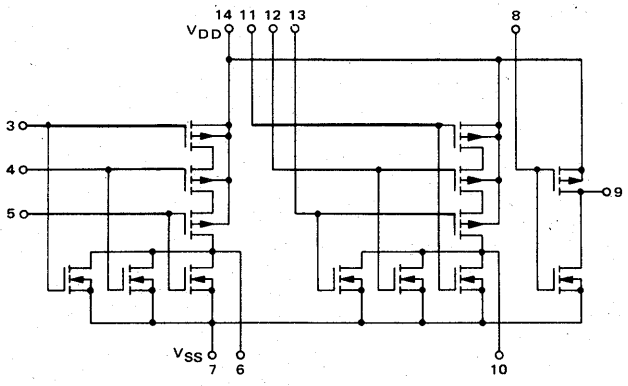
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATIC



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.4	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	2.9	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.6	
"1" Level	V_{IH}									
(V_O = 1.4 or 3.6 Vdc)		5.0	3.6	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 2.8 or 7.2 Vdc)		10	7.1	–	7.0	5.50	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.4	–	11.25	8.25	–	11.25	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−0.62	–	−0.5	−1.7	–	−0.35	–	
(V_{OH} = 9.5 Vdc)		10	−0.62	–	−0.5	−0.9	–	−0.35	–	
(V_{OH} = 13.5 Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.5	–	0.4	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.9	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−0.23	–	−0.2	−1.7	–	−0.16	–	
(V_{OH} = 9.5 Vdc)		10	−0.23	–	−0.2	−0.9	–	−0.16	–	
(V_{OH} = 13.5 Vdc)		15	−0.69	–	−0.6	−3.5	–	−0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.2	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.5	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.05	–	0.0005	0.05	–	1.5	µAdc
(Per Package)		10	–	0.10	–	0.0010	0.10	–	3.0	
		15	–	0.20	–	0.0015	0.20	–	6.0	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	0.5	–	0.0005	0.5	–	3.8	µAdc
(Per Package)		10	–	1.0	–	0.0010	1.0	–	7.5	
		15	–	2.0	–	0.0015	2.0	–	15.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.28 µA/kHz) f + I_{DD}/3							µAdc
		10	I_T = (0.55 µA/kHz) f + I_{DD}/3							
		15	I_T = (0.83 µA/kHz) f + I_{DD}/3							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns		5.0	115	165	200	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	55	95	110	
t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 15 ns		15	40	75	85	

*The formulas given are for the typical characteristics only.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

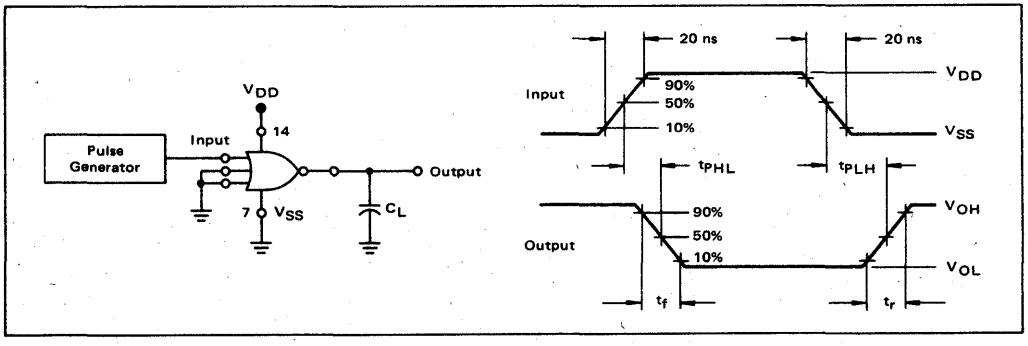


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

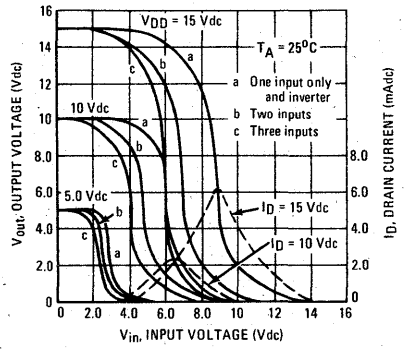
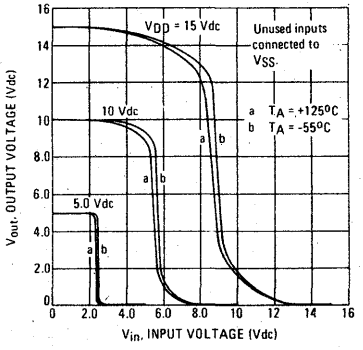


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE



MOTOROLA Semiconductors

BOX 20912 • PHOENIX, ARIZONA 85036

MC14001

QUAD 2-INPUT "NOR" GATE

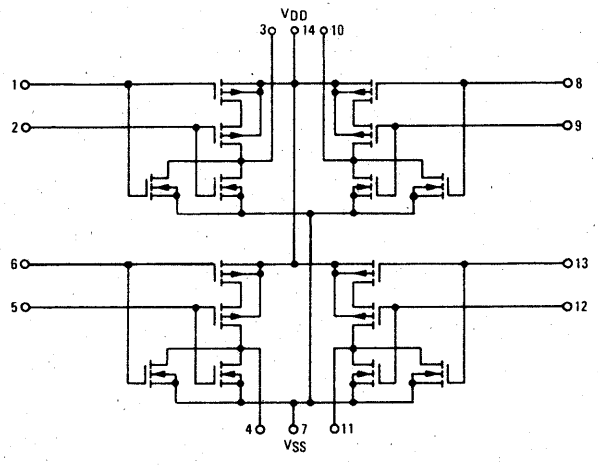
The MC14001 quad 2-Input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4001A

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	–55 to +125 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

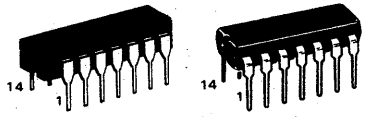
CIRCUIT SCHEMATIC



McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

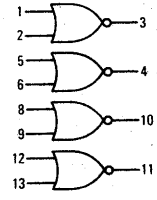
P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXX — Suffix — Denotes

- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage # "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.4	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	2.9	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.6	
"1" Level	V_{IH}									
(V_O = 1.4 or 3.6 Vdc)		5.0	3.6	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 2.8 or 7.2 Vdc)		10	7.1	–	7.0	5.50	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.4	–	11.25	8.25	–	11.25	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–0.62	–	–0.5	–1.7	–	–0.35	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.5	–	0.4	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.9	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–0.23	–	–0.2	–1.7	–	–1.16	–	
(V_{OH} = 9.5 Vdc)		10	–0.23	–	–0.2	–0.9	–	–0.16	–	
(V_{OH} = 13.5 Vdc)		15	–0.69	–	–0.6	–3.5	–	–0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.2	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.5	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.05	–	0.0005	0.05	–	1.5	µAdc
		10	–	0.10	–	0.0010	0.10	–	3.0	
		15	–	0.20	–	0.0015	0.20	–	6.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	0.5	–	0.0005	0.5	–	3.8	µAdc
		10	–	1.0	–	0.0010	1.0	–	7.5	
		15	–	2.0	–	0.0015	2.0	–	15.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	I_T = (0.28 µA/kHz) f + I_{DD}/N							µAdc
		10	I_T = (0.55 µA/kHz) f + I_{DD}/N							
		15	I_T = (0.83 µA/kHz) f + I_{DD}/N							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + N \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency and where N is number of gates per package.
**The formulas given are for the typical characteristics only at 25°C.

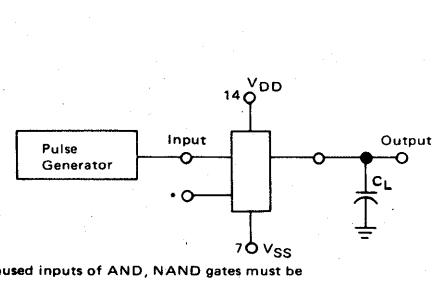
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PLH}					ns
All Inverting Non-B Series Gates						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns		5.0	115	165	200	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	55	95	110	
t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 15 ns		15	40	75	85	
Non-Inverting Non-B Series Gates (MC14071 and MC14081 only)						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 80 ns		5.0	165	275	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	75	135	185	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	50	95	130	

*The formulas given are for the typical characteristics only.

5

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.

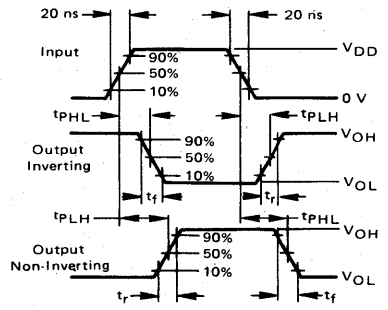


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

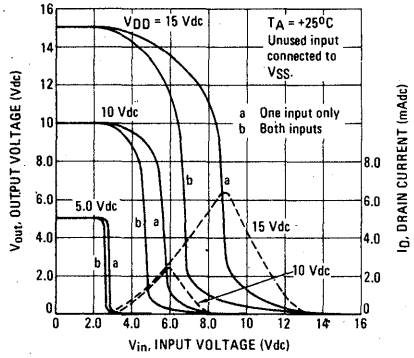


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

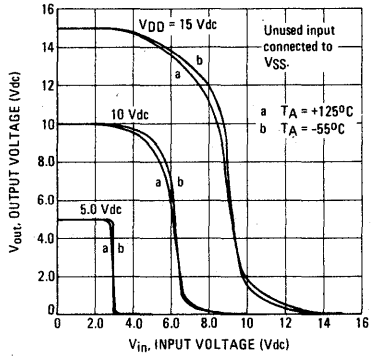


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FIGURE 4 –TYPICAL OUTPUT SOURCE CHARACTERISTICS

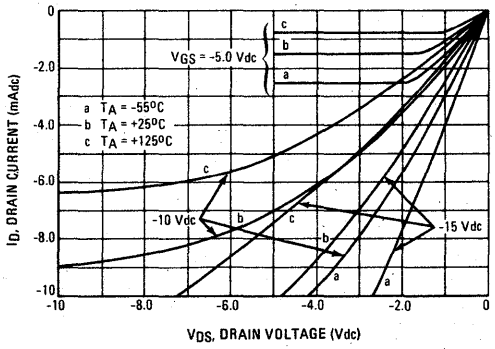
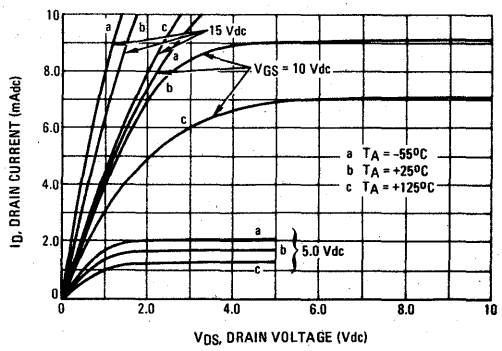


FIGURE 5 – TYPICAL OUTPUT SINK CHARACTERISTICS



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MC14001B

B-SUFFIX SERIES McMOS GATES

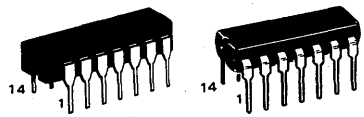
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Relpacements for CD4001B

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

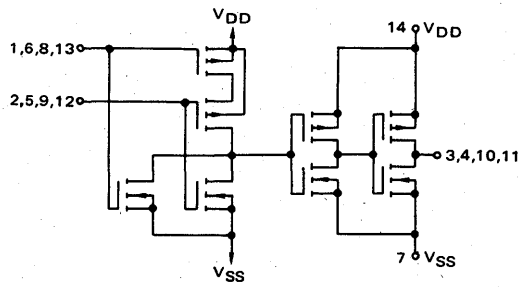
MC14XXXB — Suffix — Denotes

- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

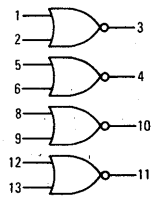
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC
(1/4 of Device Shown)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	$I_T = (0.3\ \mu A/kHz)\ f + I_{DD}/N$							μAdc
		10	$I_T = (0.6\ \mu A/kHz)\ f + I_{DD}/N$							
		15	$I_T = (0.9\ \mu A/kHz)\ f + I_{DD}/N$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + N \times 10^{-3} (C_L - 50)\ V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency and N is number of gates per package.
**The formulas given are for the typical characteristics only at 25°C.

B-SERIES GATE SWITCHING TIMES

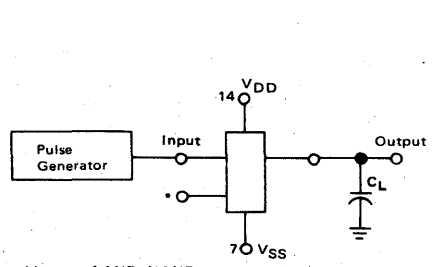
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	All Types Typ	All Types Max	Unit
Output Rise Time, All B-Series Gates	t_r					ns
t_r = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_r = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_r = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Output Fall Time, All B-Series Gates	t_f					ns
t_f = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_f = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_f = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
MC14001B, MC14011B only						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 80 ns		5.0	–	125	250	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 32 ns		10	–	50	100	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 27 ns		15	–	40	80	
All Other 2, 3, and 4 Input Gates						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 115 ns		5.0	–	160	320	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 47 ns		10	–	65	130	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns		15	–	50	100	
8-Input Gates (MC14068B, MC14078B)						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 155 ns		5.0	–	200	400	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 62 ns		10	–	80	160	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 47 ns		15	–	60	120	

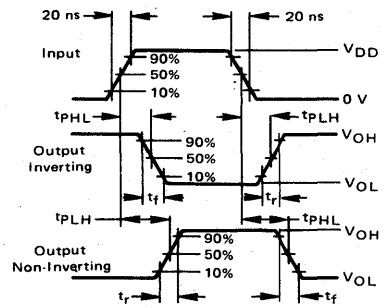
*The formulas given are for the typical characteristics only.

5

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.



TYPICAL B-SERIES GATE CHARACTERISTICS

N-CHANNEL DRAIN CURRENT

FIGURE 2 – V_{GS} = 5.0 Vdc

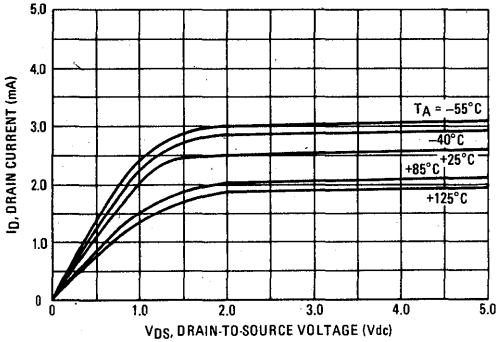


FIGURE 4 – V_{GS} = 10 Vdc

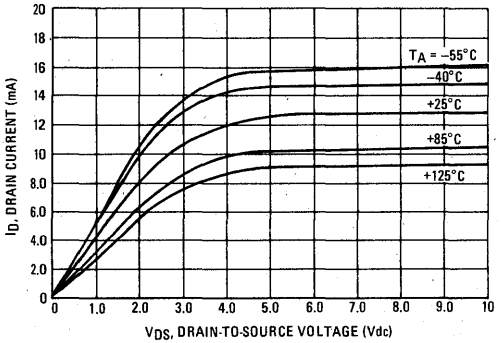
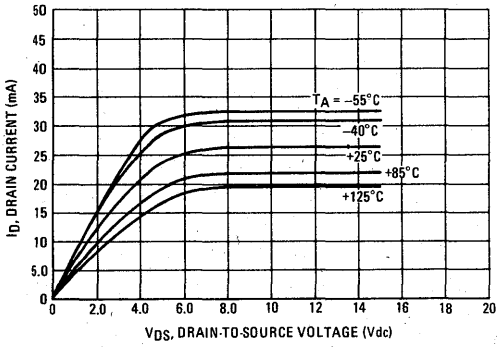


FIGURE 6 – V_{GS} = 15 Vdc



P-CHANNEL DRAIN CURRENT

FIGURE 3 – V_{GS} = −5.0 Vdc

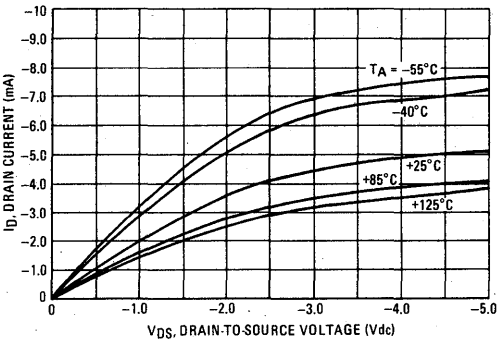


FIGURE 5 – V_{GS} = −10 Vdc

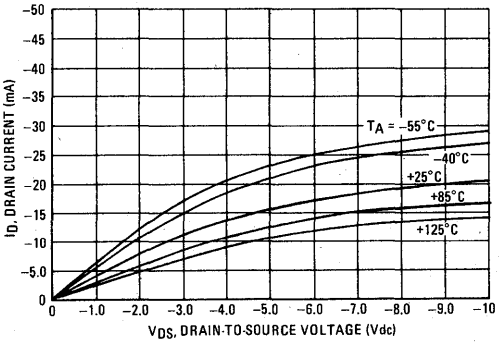
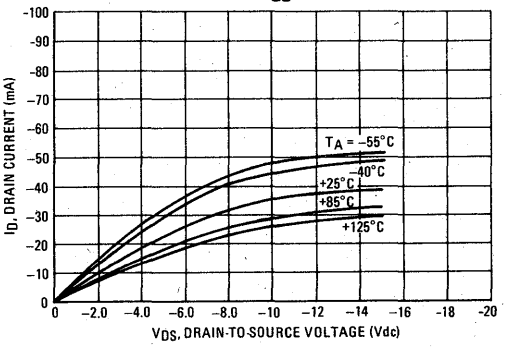


FIGURE 7 – V_{GS} = −15 Vdc



5

TYPICAL B-SERIES GATE CHARACTERISTICS (cont'd)

VOLTAGE TRANSFER CHARACTERISTICS

FIGURE 8 – V_{DD} = 5.0 Vdc

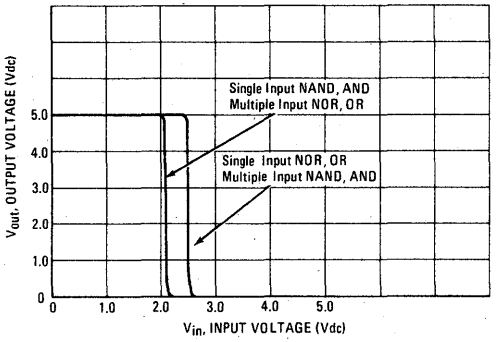


FIGURE 9 – V_{DD} = 10 Vdc

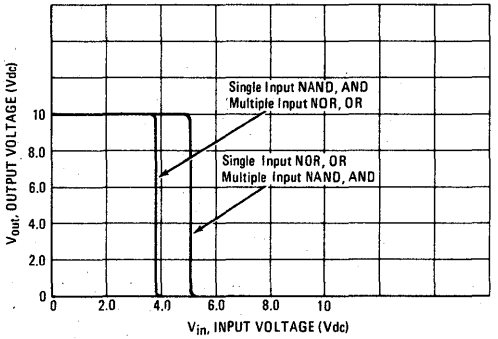
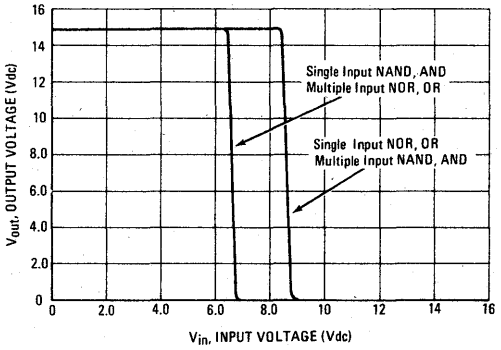


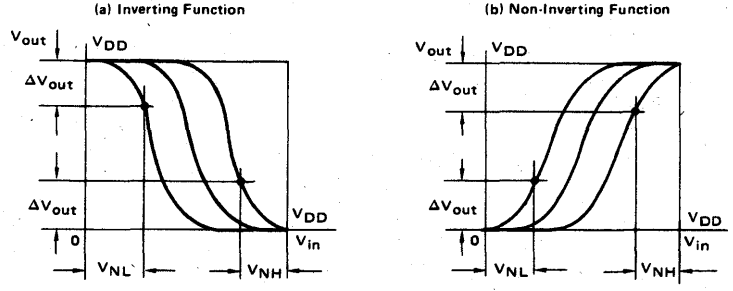
FIGURE 10 – V_{DD} = 15 Vdc



DC NOISE IMMUNITY (V_{NL} AND V_{NH})

The dc noise immunity is defined as the input voltage range from an ideal "1" or "0" input level (assuming the previous McMOS driving stage is unloaded) which does not produce output state (combination) change(s). The typical and limit values of the input ranges V_{NL} and V_{NH} for the output to stay within a range ΔV_{out} from either V_{DD} or V_{SS} are given in the Electrical Characteristics table. The definitions of V_{NL}, V_{NH}, and ΔV_{out} are illustrated in Figure 11 for inverting and non-inverting functions.

FIGURE 11 – DC NOISE IMMUNITY



V_{SS} = 0 volts dc

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MC14002
MC14002B

DUAL 4-INPUT "NOR" GATE

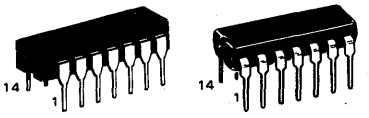
The MC14002 and MC14002B are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14002B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14002B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4002A and CD4002B

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

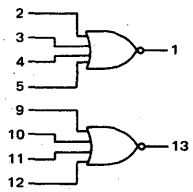
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

Delete for Non-B Device

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



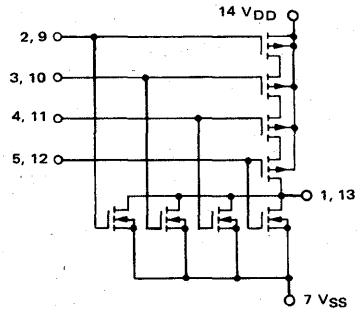
V_{DD} = Pin 14
V_{SS} = Pin 7

See the MC14001 data sheet for complete characteristics for the non-B device.

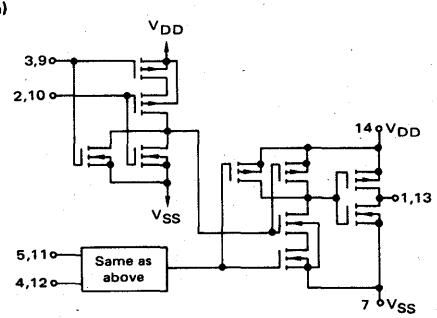
See the MC14001B data sheet for complete characteristics of the B-Series device.

CIRCUIT SCHEMATICS
(1/2 of Device Shown)

MC14002



MC14002B



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA Semiconductors
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MC14006B

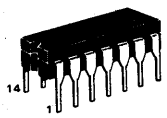
McMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

18-BIT STATIC SHIFT REGISTER

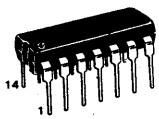
18-BIT STATIC SHIFT REGISTER

The MC14006B shift register is comprised of four separate shift register sections sharing a common clock: two sections have four stages, and two sections have five stages with an output tap on both the fourth and fifth stages. This makes it possible to obtain a shift register of 4, 5, 8, 9, 10, 12, 13, 14, 16, 17, or 18 bits by appropriate selection of inputs and outputs. This part is particularly useful in serial shift registers and time delay circuits.

- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Quiescent Current - 5nA/package typical @ 5 Vdc
- Fully Static Operation
- 8-MHz Shift Rate typical
- Can be Cascaded to Provide Longer Shift Register Lengths
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4006



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

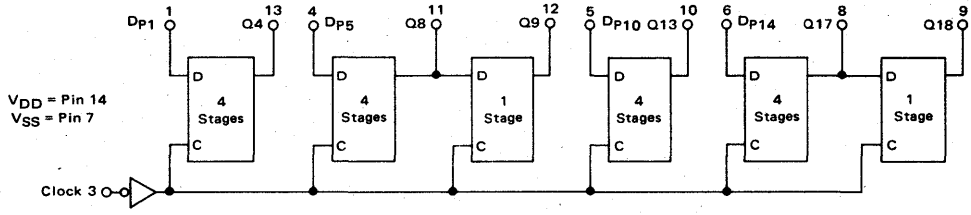
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE
(Single Stage)

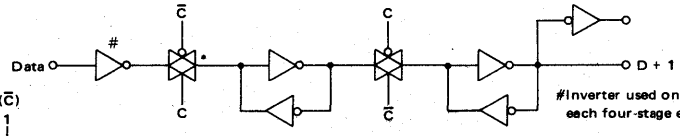
D_n	C	Q_{n+1}
0	⌐	0
1	⌐	1
X	⌐	Q_n

X = Don't Care

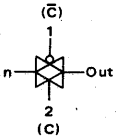
BLOCK DIAGRAM



LOGIC DIAGRAM
(ONE REGISTER STAGE)



#Inverter used only on the first stage of each four-stage element.



*Transmission Gate

Input to output is
(A) A bidirectional low impedance when control input 1 is "low" and control input 2 is "high".
(B) An open circuit when control input 1 is "high" and control input 2 is "low".

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.3 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.6 µA/kHz) f + I_{DD}							
		15	I_T = (3.9 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time	t_{PLH},							ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 220 ns	t_{PHL}	5.0	–	–	305	460	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 77 ns		10	–	–	110	165	275	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 55 ns		15	–	–	80	120	200	
Minimum Clock Pulse Width	PW_C	5.0	–	–	100	200	250	ns
		10	–	–	60	70	125	
		15	–	–	40	55	95	
Maximum Clock Pulse Frequency	PRF	5.0	2.5	2.0	5.0	–	–	MHz
		10	7.0	4.0	8.3	–	–	
		15	10	6.0	12	–	–	
Maximum Clock Pulse Rise and Fall Time#	t_r, t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
Setup Time	t_{setup}	5.0	–	–	–50	–15	0	ns
		10	–	–	–15	–5.0	0	
		15	–	–	–8.0	–3.0	0	
Hold Time	t_{hold}	5.0	–	–	75	180	220	ns
		10	–	–	25	90	110	
		15	–	–	20	75	90	

*The formula given is for the typical characteristics only at 25°C.

#When shift register sections are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the rise and fall times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitance load.

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FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

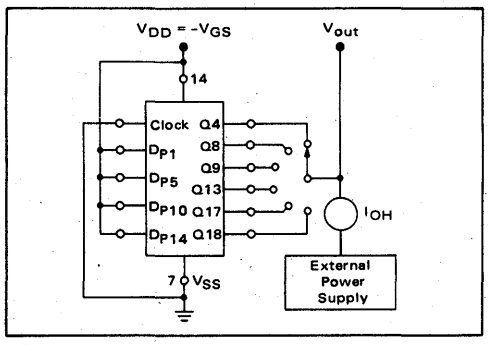


FIGURE 2 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT

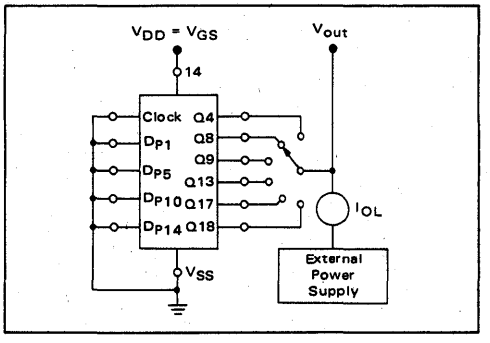


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

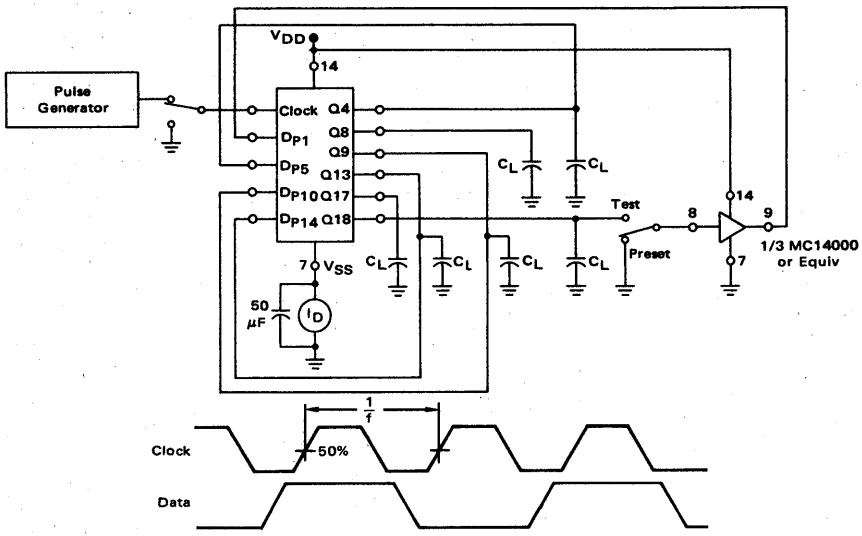
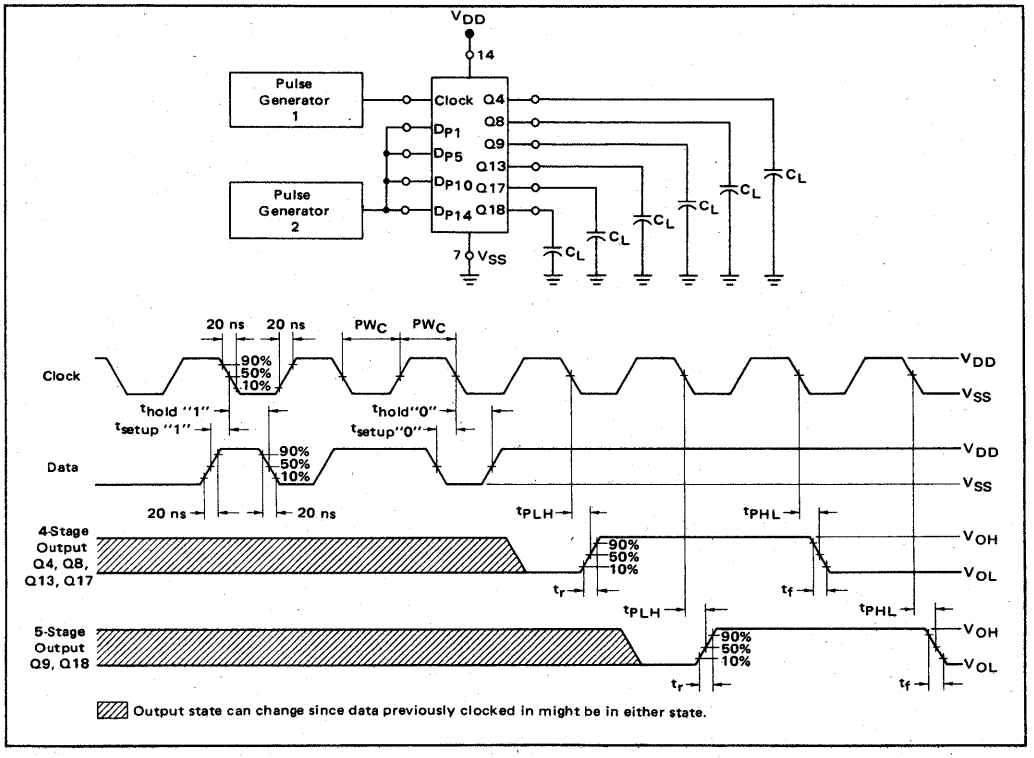


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14007B

DUAL COMPLEMENTARY PAIR PLUS INVERTER

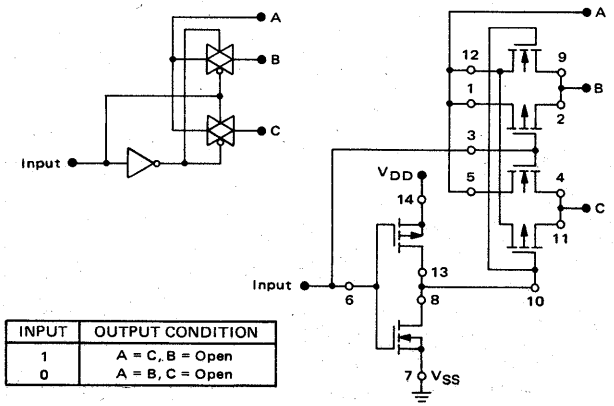
The MC14007B multi-purpose device consists of three N-channel and three P-channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse-shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation = Positive or Negative
- Symmetrical Output Impedance — 200 ohms typical @ 10 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4007

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 — TYPICAL APPLICATION: 2-INPUT ANALOG MULTIPLEXER



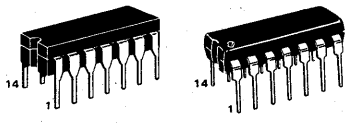
INPUT	OUTPUT CONDITION
1	A = C, B = Open
0	A = B, C = Open

Substrates of P-channel devices internally connected to V_{DD}; substrates of N-channel devices internally connected to V_{SS}.

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL COMPLEMENTARY PAIR PLUS INVERTER



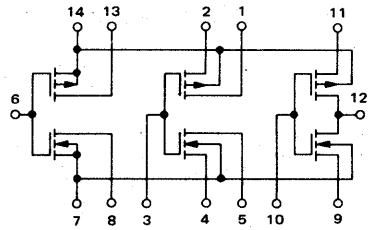
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

SCHEMATIC



V_{DD} = Pin 14
V_{SS} = Pin 7

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.4	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	2.9	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.6	
"1" Level	V_{IH}									Vdc
(V_O = 1.4 or 3.6 Vdc)		5.0	3.6	–	3.5	2.75	–	3.5	–	
(V_O = 2.8 or 7.2 Vdc)		10	7.1	–	7.0	5.50	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.4	–	11.25	8.25	–	11.25	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.75	–	–1.4	–5.0	–	–1.0	–	
(V_{OH} = 9.5 Vdc)		10	–1.35	–	–1.1	–2.5	–	–0.75	–	
(V_{OH} = 13.5 Vdc)		15	–5.0	–	–4.0	–10	–	–2.8	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.75	–	0.6	1.0	–	0.4	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.5	–	0.95	–	
(V_{OL} = 1.5 Vdc)		15	6.0	–	5.0	10	–	3.5	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.3	–	–1.1	–5.0	–	–0.9	–	
(V_{OH} = 9.5 Vdc)		10	–0.65	–	–0.55	–2.5	–	–0.45	–	
(V_{OH} = 13.5 Vdc)		15	–2.4	–	–2.0	–10	–	–1.6	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	1.0	–	0.36	–	mAdc
(V_{OL} =0.5 Vdc)		10	1.3	–	1.1	2.5	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.0	–	3.3	10	–	2.7	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	–	0.10	–	0.0010	0.10	–	3.0	
		15	–	0.20	–	0.0015	0.20	–	6.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	0.5	–	0.0005	0.5	–	3.8	μAdc
		10	–	1.0	–	0.0010	1.0	–	7.5	
		15	–	2.0	–	0.0015	2.0	–	15	
Total Supply Current**† (Dynamic plus Quiescent, Per Pachage) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.72 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.44 μA/kHz) f + I_{DD}							
		15	I_T = (2.16 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = 1.2 ns/pF) C_L + 30 ns		5.0	90	150	180	
t_r = (0.5 ns/pF) C_L + 20 ns		10	45	75	90	
t_r = (0.4 ns/pF) C_L + 15 ns		15	35	60	70	
Output Fall Time	t_f					ns
t_f = (1.2 ns/pF) C_L + 15 ns		5.0	75	125	150	
t_f = (0.5 ns/pF) C_L + 15 ns		10	40	60	80	
t_f = (0.4 ns/pF) C_L + 10 ns		15	30	50	60	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.5 ns/pF) C_L + 35 ns		5.0	60	110	130	
t_{PLH}= (0.2 ns/pF) C_L + 20 ns		10	30	60	75	
t_{PLH} = (0.15 ns/pF) C_L + 17.5 ns		15	25	45	55	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.0 ns/pF) C_L + 10 ns		5.0	60	110	130	
t_{PHL} = (0.3 ns/pF) C_L + 15 ns		10	30	60	75	
t_{PHL} = (0.2 ns/pF) C_L + 15 ns		15	25	45	55	

*The formula given is for the typical characteristics only.

FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

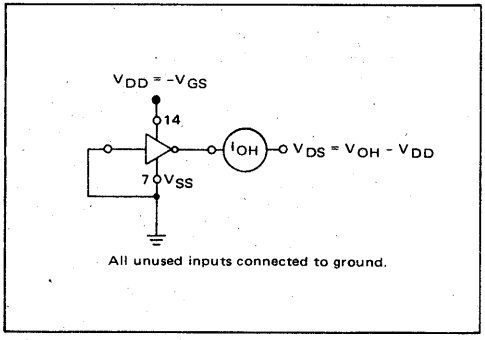
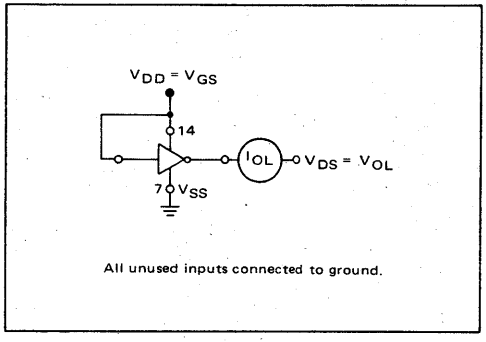
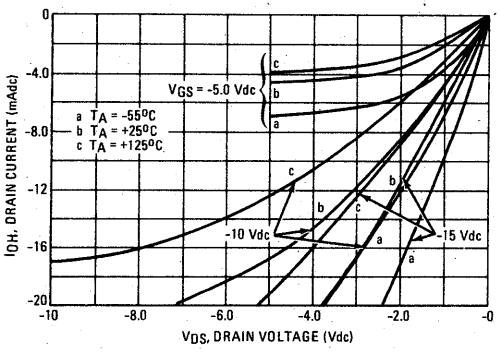
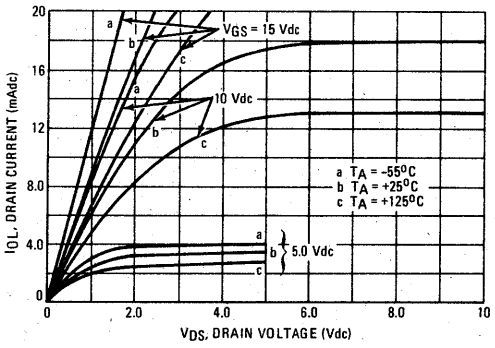


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS

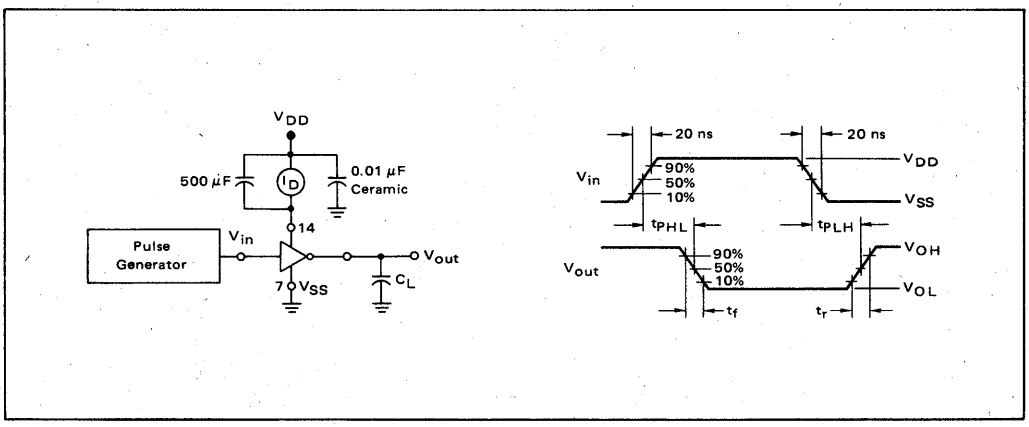






5

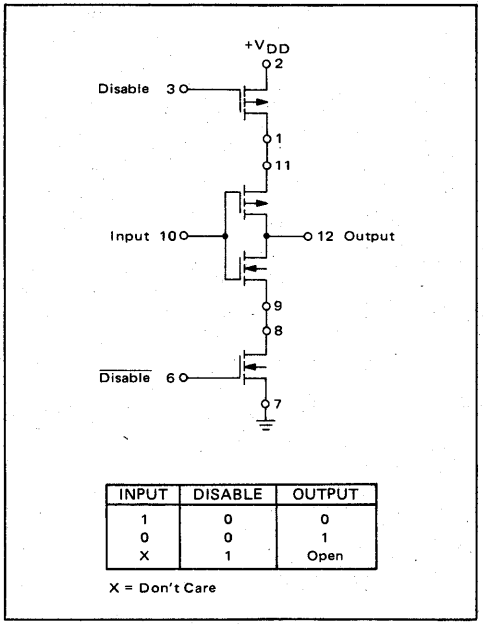
FIGURE 4 – SWITCHING TIME AND POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



APPLICATIONS

The MC14007B dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 5, and 6 are a few examples of the device flexibility.

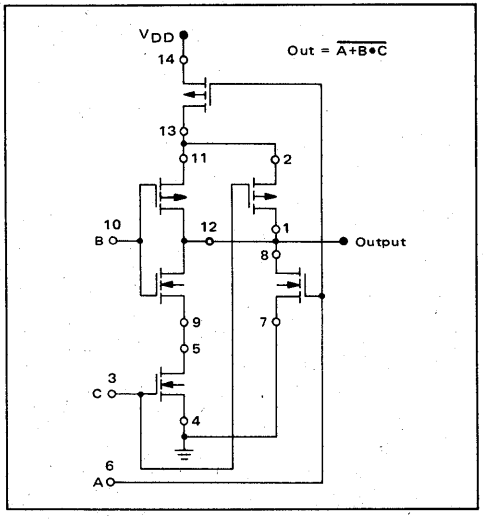
FIGURE 5 – 3-STATE BUFFER



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	Open

X = Don't Care

FIGURE 6 – AOI FUNCTIONS USING TREE LOGIC



Substrates of P-channel devices internally connected to V_{DD};
Substrates of N-channel devices internally connected to V_{SS}.

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MC14008B

4-BIT FULL ADDER

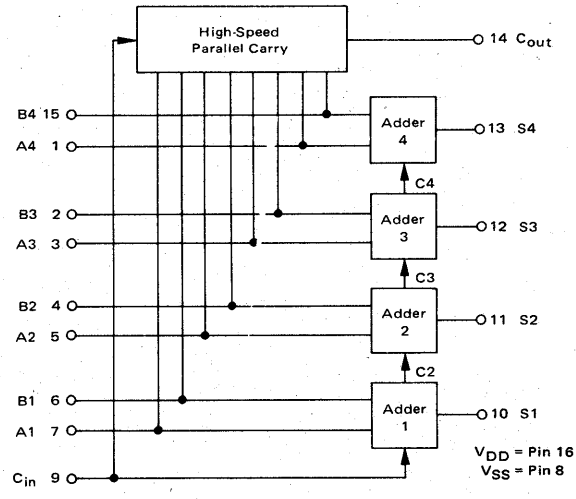
The MC14008B 4-bit full adder is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications.The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

- Look-Ahead Carry Output
- High-Speed Operation — 160 ns typical from Sum_{in} to Sum_{out}
- Quiescent Current — 5.0 nA/package typical @ 5 Vdc
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4008

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

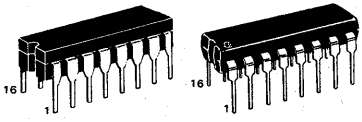
BLOCK DIAGRAM



McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT FULL ADDER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

TRUTH TABLE
(One Stage)

C_{in}	B	A	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.7 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.4 µA/kHz) f + I_{DD}							
		15	I_T = (5.0 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise Time,	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time,	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Sum In to Sum Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 127 ns		10	–	160	320	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	–	115	230	
Sum In to Carry Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 220 ns		5.0	–	305	610	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 112 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Carry In to Sum Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 290 ns		5.0	–	375	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 122 ns		10	–	155	310	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	–	115	230	
Carry In to Carry Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 85 ns		5.0	–	170	340	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 30 ns		15	–	55	110	

*The formula is for the typical characteristics only.

5

FIGURE 1 – TYPICAL SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

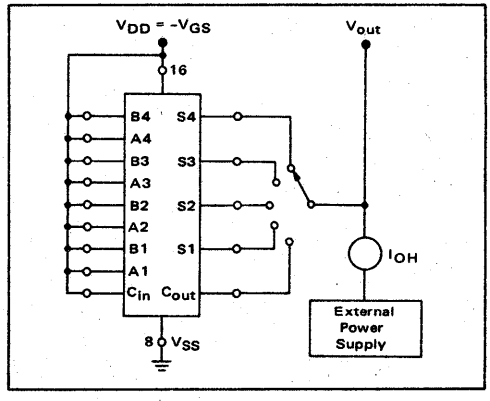


FIGURE 2 – TYPICAL SINK CURRENT CHARACTERISTICS TEST CIRCUIT

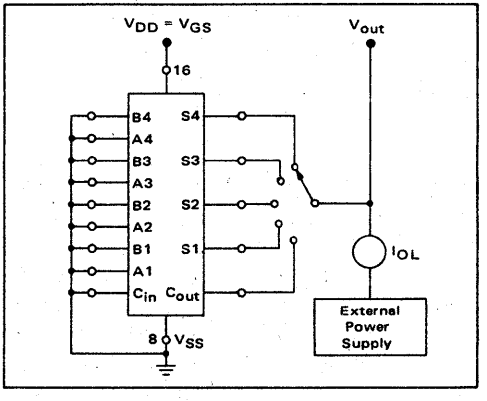


FIGURE 3 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

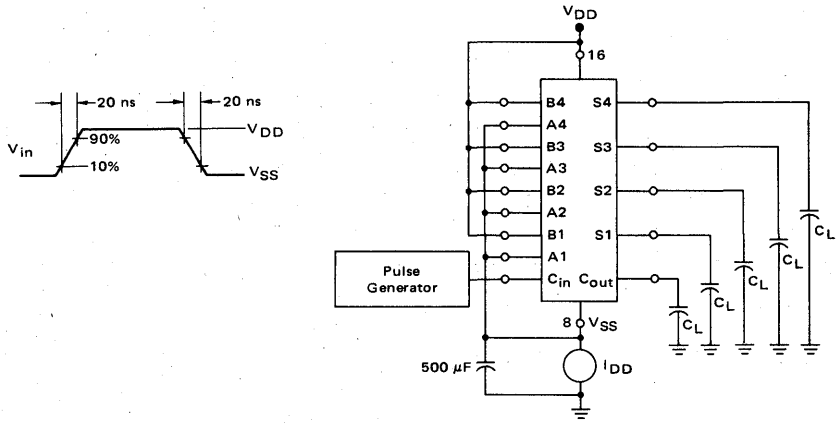


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

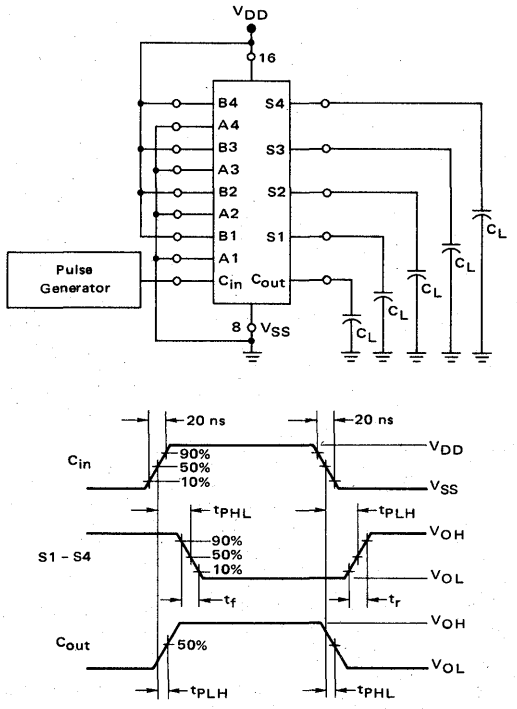
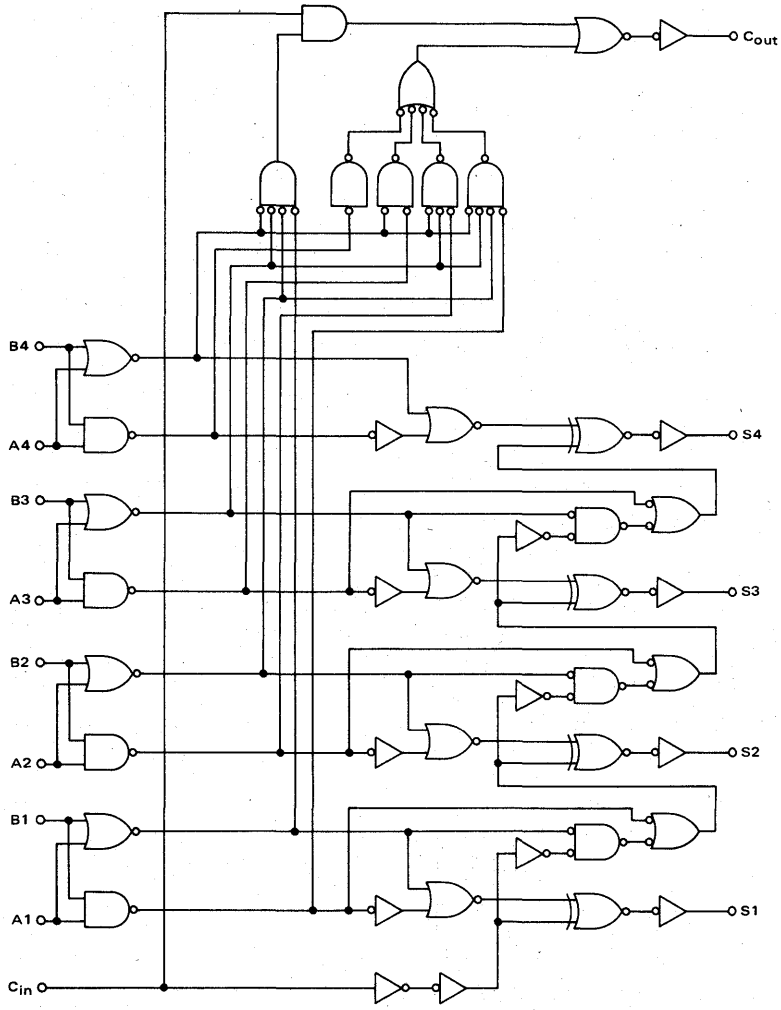
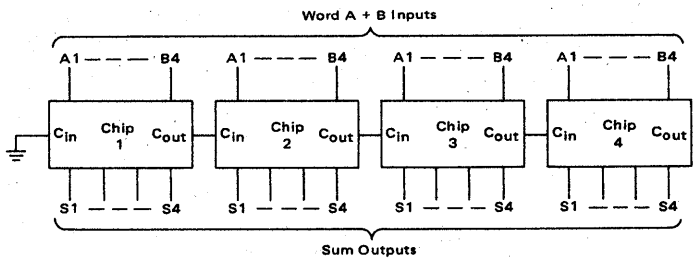


FIGURE 5 – LOGIC DIAGRAM



TYPICAL APPLICATION

FIGURE 6 – USING THE MC14008B IN A 16-BIT ADDER CONFIGURATION



Calculation of 16-bit adder speed:

t_p total = t_p (Sum to Carry) + t_p (Carry to Sum) + 2 t_p (Carry to Carry)

Typically, the overall 16-bit adder speed at 10 V is:

t_p total = 115 + 125 + 90 = 330 ns typ

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MC14011
MC14011B

QUAD 2-INPUT "NAND" GATE

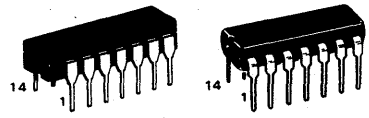
The MC14011 and MC14011B are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14011B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14011B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4011A and CD4011B

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

Delete for Non-B Device

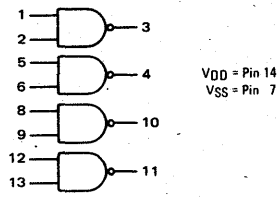
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001 data sheet for complete characteristics for the non-B device.

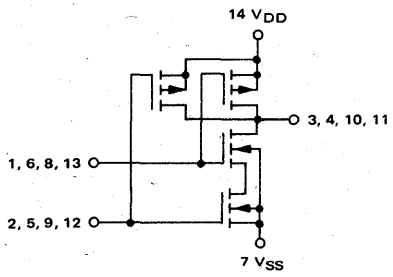
See the MC14001B data sheet for complete characteristics of the B-Series device.

LOGIC DIAGRAM

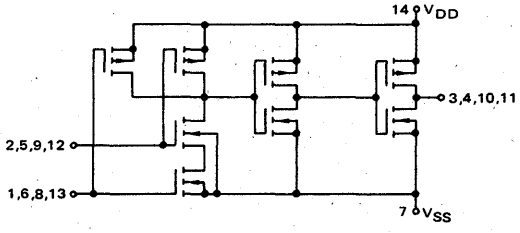


CIRCUIT SCHEMATICS
(1/4 of Device Shown)

MC14011



MC14011B



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MC14012
MC14012B

DUAL 4-INPUT "NAND" GATE

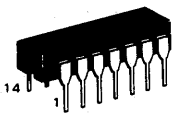
The MC14012 and MC14012B are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14012B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14012B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4012A and CD4012B

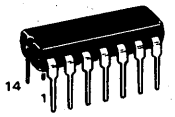
McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

Delete for Non-B Device

- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

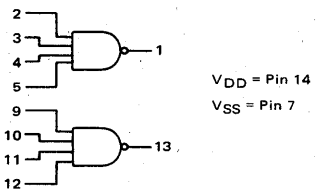
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001 data sheet for complete characteristics for the non-B device.

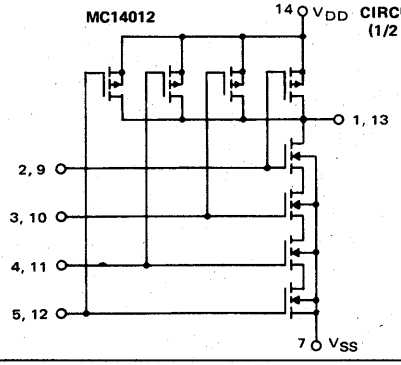
See the MC14001B data sheet for complete characteristics of the B-Series device.

LOGIC DIAGRAM

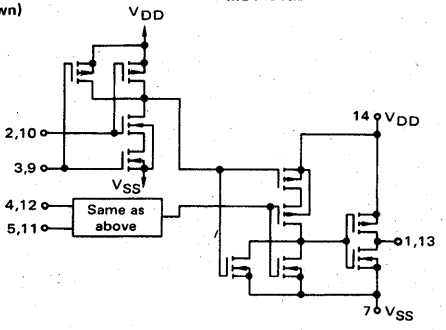


CIRCUIT SCHEMATICS
(1/2 of Device Shown)

MC14012



MC14012B



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MC14013B

DUAL TYPE D FLIP-FLOP

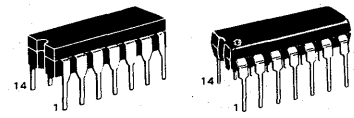
The MC14013B dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Toggle Rate = 4 MHz typical @ 5 Vdc
- Logic Edge-Clocked Flip-Flop Design – Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4013

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL TYPE D FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

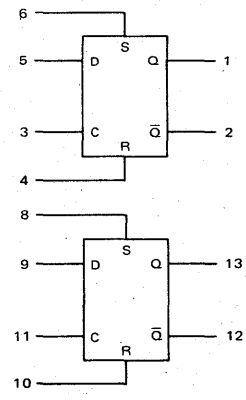
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS				OUTPUTS		
CLOCK†	DATA	RESET	SET	Q	$\overline{Q}$	
⎍	0	0	0	0	1	
⎍	1	0	0	1	0	
⎎	X	0	0	Q	$\overline{Q}$	No Change
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = Don't Care
† = Level Change

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.5 μA/kHz) f + I_{DD}							
		15	I_T = (2.3 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	360	360	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	180	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	130	130	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	200	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	100	100	
t_f = (0.55 ns/pF) C_L + 12.5 ns		15	–	–	40	80	80	
Propagation Delay Time	t_{PLH}, t_{PHL}							ns
Clock to Q								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	–	175	350	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	–	75	150	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	–	50	100	100	
Set to Q								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	–	175	350	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	–	75	150	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	–	50	100	100	
Reset to Q								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	–	350	450	450	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	–	100	200	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 50 ns		15	–	–	75	150	150	
Minimum Setup Times	$t_{setup\ H}$	5.0	–	–	20	40	40	ns
	$t_{setup\ L}$	10	–	–	10	20	20	
		15	–	–	7.5	15	15	
Minimum Clock Pulse Width	PW_{CH}, PW_{CL}	5.0	–	–	125	250	250	ns
		10	–	–	50	100	100	
		15	–	–	35	70	70	
Maximum Clock Pulse Frequency	PRF	5.0	2.0	2.0	4.0	–	–	MHz
		10	5.0	5.0	10	–	–	
		15	7.0	7.0	14	–	–	
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0	15	15	–	–	–	μs
		10	5.0	5.0	–	–	–	
		15	4.0	4.0	–	–	–	
Minimum Set and Reset Pulse Width	PW_S	5.0	–	–	125	250	250	ns
	PW_R	10	–	–	50	100	100	
		15	–	–	35	70	70	

*The formula given is for the typical characteristics only.

LOGIC DIAGRAM
(1/2 of Device Shown)

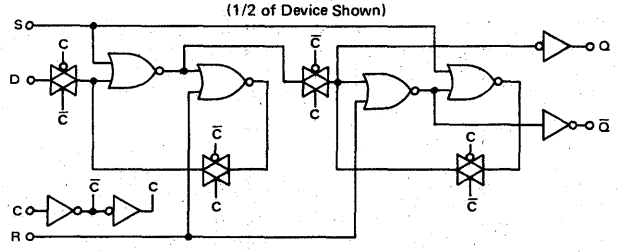


FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS
(Data, Clock, and Output)

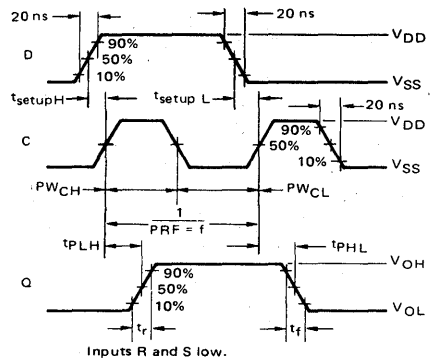
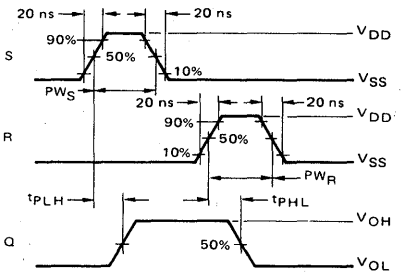
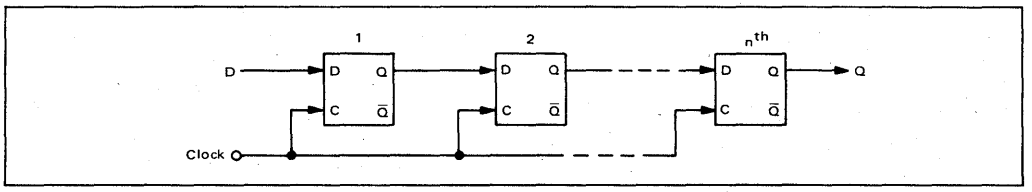


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, and Output)

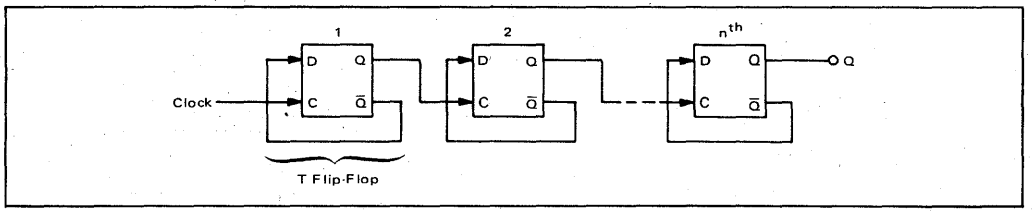


TYPICAL APPLICATIONS

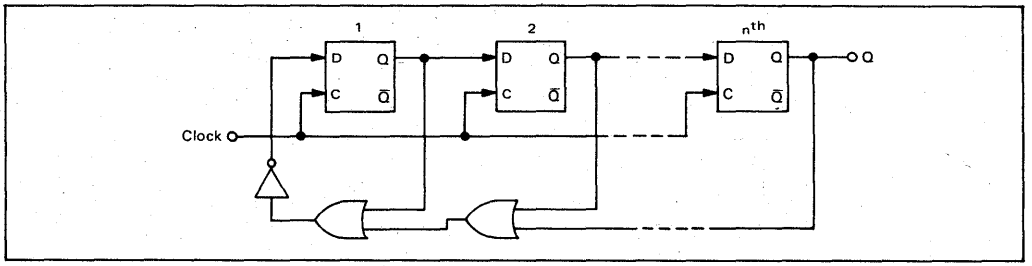
n-STAGE SHIFT REGISTER



BINARY RIPPLE UP-COUNTER (Divide-by-2^n)



MODIFIED RING COUNTER (Divide-by-(n + 1))



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Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14014B
MC14021B

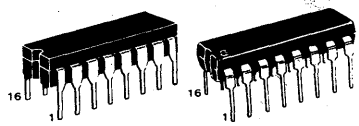
McMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER

8-BIT STATIC SHIFT REGISTER

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation from DC to 7.0 MHz
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.
- MC14014B Pin-for-Pin Replacement for CD4014
- MC14021B Pin-for-Pin Replacement for CD4021



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

SERIAL OPERATION:

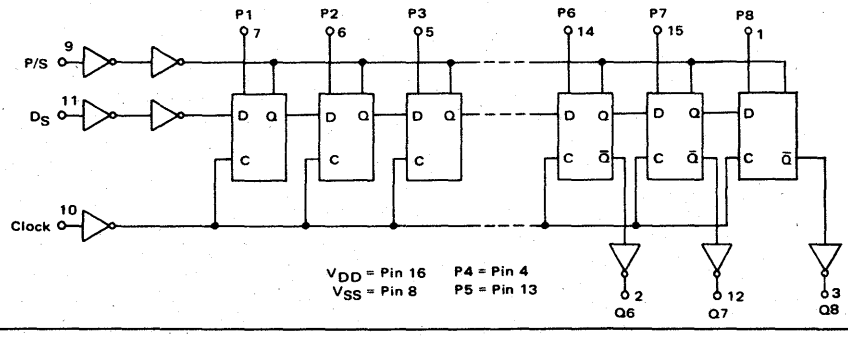
t	CLOCK	D_S	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n	⌐¬	0	0	0	?	?
n+1	⌐¬	1	0	1	0	?
n+2	⌐¬	0	0	0	1	0
n+3	⌐¬	1	0	1	0	1
	¬⌐	X	0	Q6	Q7	Q8

PARALLEL OPERATION:

CLOCK	D_S	P/S	D_m	$*Q_m$
⌐¬	X	1	0	0
	X	1	1	1

*Q6, Q7, & Q8 are available externally
X = Don't Care

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.50 μA/kHz) f + I_{DD}							
		15	I_T = (2.25 μA/kHz) f + I_{DD}							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1.5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

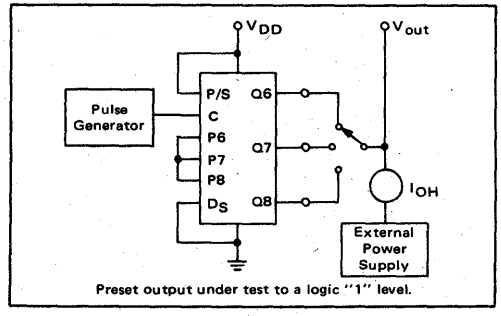
SWITCHING CHARACTERISTICS* (C_L = 50 pf, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time (Clock to Q, P/S to Q)	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	–	400	750	1000	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns		10	–	–	170	250	400	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 90 ns		15	–	–	115	170	265	
Minimum Clock Pulse Width	PW_C	5.0	–	–	150	400	500	ns
		10	–	–	75	175	200	
		15	–	–	40	135	150	
Maximum Clock Frequency	f_C	5.0	1.5	1.0	3.0	–	–	MHz
		10	3.0	2.5	6.0	–	–	
		15	4.0	3.0	8.0	–	–	
Minimum Parallel/Serial Control Pulse Width	PW(P/S)	5.0	–	–	150	400	500	ns
		10	–	–	75	175	200	
		15	–	–	40	135	150	
Minimum Setup Time	t_{setup}	5.0	–	–	150	350	500	ns
		10	–	–	50	80	100	
		15	–	–	30	60	80	
Maximum Input Clock Rise Time	t_{rC}	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	

*The formula given is for the typical characteristics only.

5

FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT



Preset output under test to a logic "1" level.

FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT

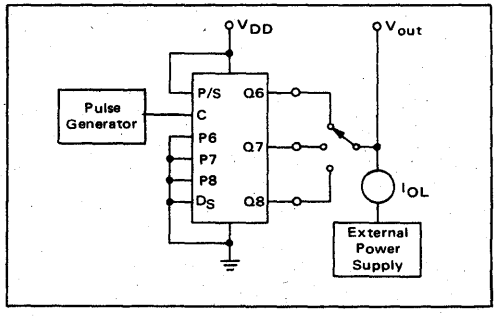


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

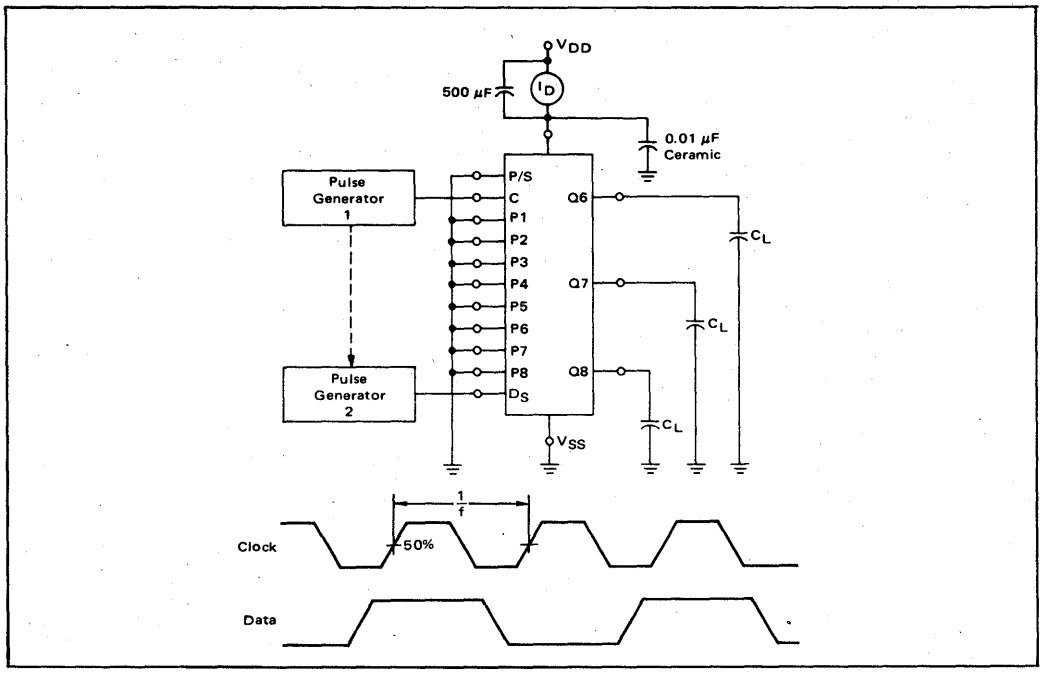
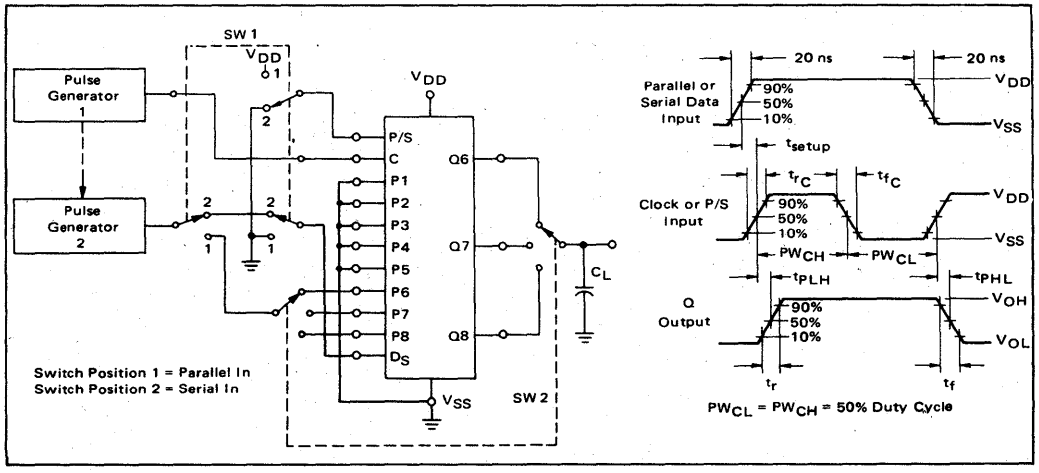


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14015B

DUAL 4-BIT STATIC SHIFT REGISTER

The MC14015B dual 4-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-state serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register states are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. There complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Low Input Capacitance – 5.0pF typical
- Logic Swing Independent of Fanout
- Toggle Rate = 6.0 MHz @ 10 Vdc
- Logic Edge-Clocked Flip-Flop Design – Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive going edge of the clock pulse.
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLES

CLOCKED OPERATION (SYNCHRONOUS)

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$Q_{n+1} = D_n$, R = 0

DIRECT OPERATION (ASYNCHRONOUS)

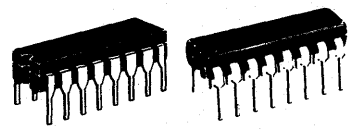
R	Q
0	Q
1	0

C = D = Don't Care

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-BIT STATIC SHIFT REGISTER



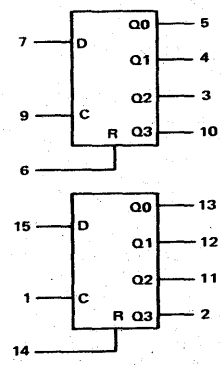
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.2 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.4 µA/kHz) f + I_{DD}							
		15	I_T = (3.6 µA/kHz) f + I_{DD}							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}							ns
Clock, Data to Q								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 225 ns		5.0	–	–	310	750	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	–	125	250	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	–	90	170	265	
Reset to Q								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 375 ns		5.0	–	–	460	750	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	–	180	250	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	–	–	120	170	265	
Minimum Clock Pulse Width	PW_C	5.0	–	–	185	400	500	ns
		10	–	–	85	175	200	
		15	–	–	55	135	150	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	2.0	–	–	MHz
		10	3.0	2.5	6.0	–	–	
		15	3.75	3.0	7.5	–	–	
Maximum Clock Pulse Rise and Fall Times	t_r,t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
Minimum Reset Pulse Width	PW_R	5.0	–	–	200	300	500	ns
		10	–	–	80	120	200	
		15	–	–	60	90	150	
Setup Time	t_{setup}	5.0	–	–	100	350	500	ns
		10	–	–	50	80	100	
		15	–	–	40	60	75	

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

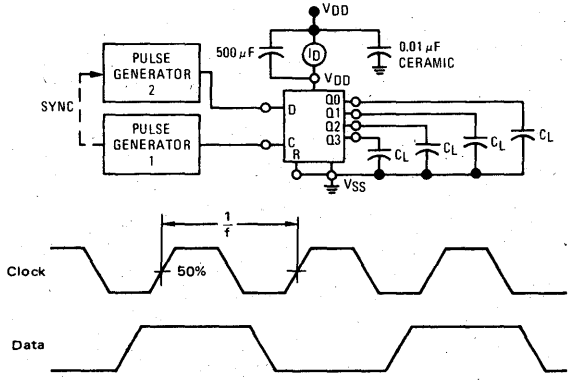


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

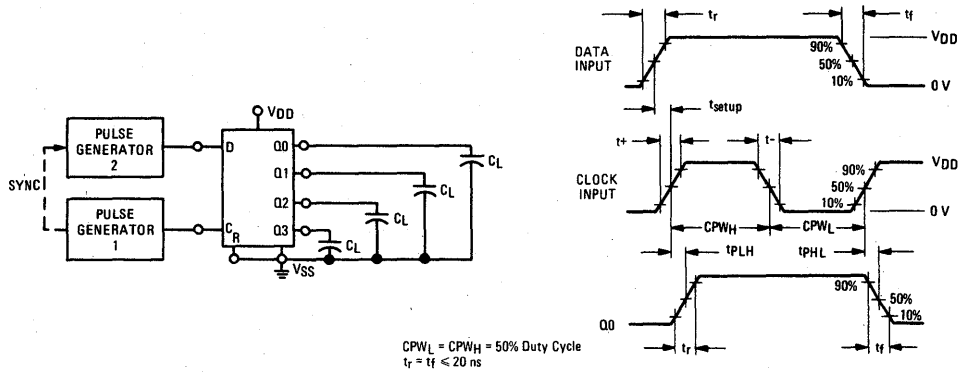
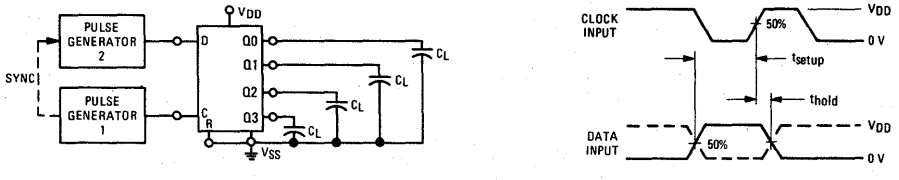
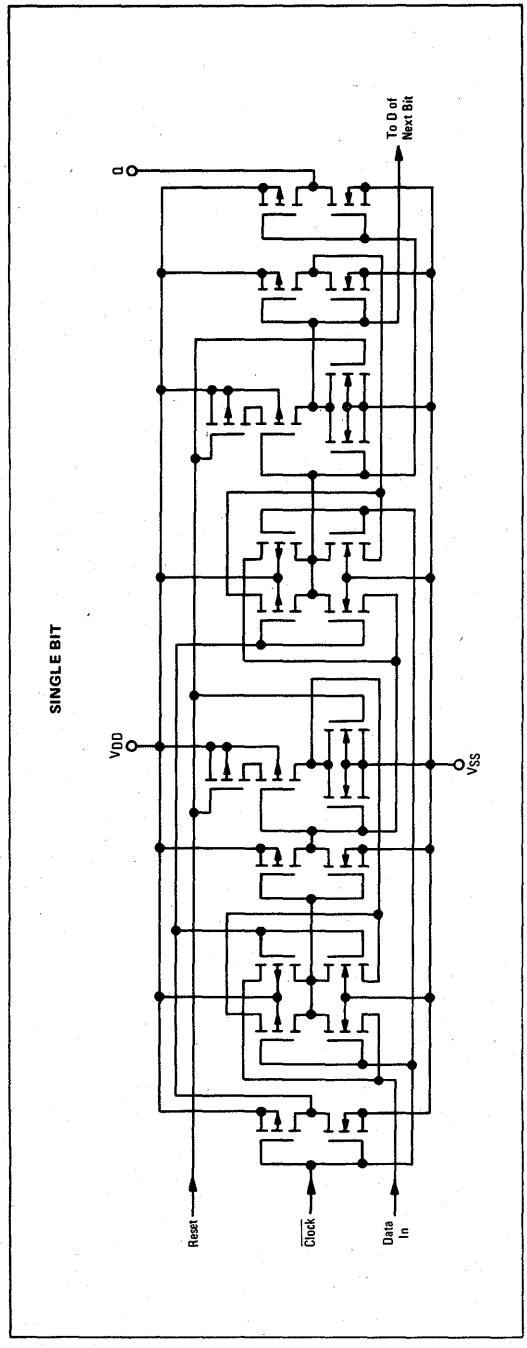
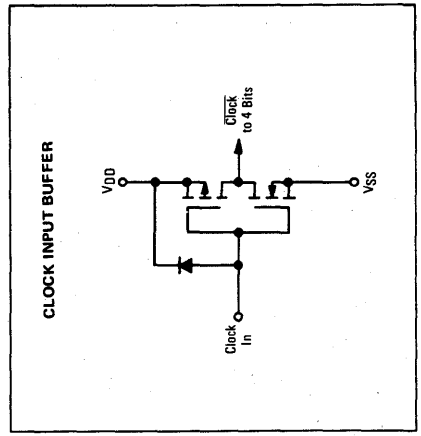


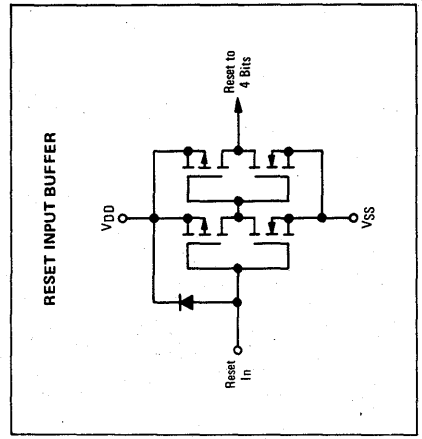
FIGURE 3 – SETUP AND HOLD TIME TEST CIRCUIT AND WAVEFORMS

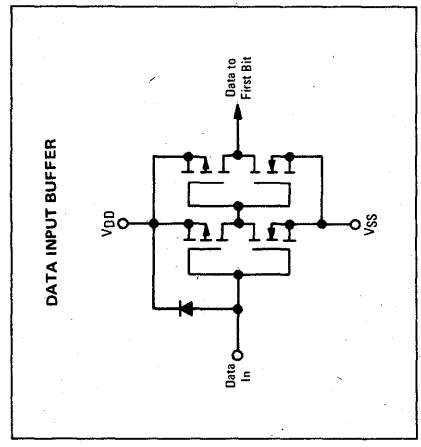


CIRCUIT SCHEMATICS









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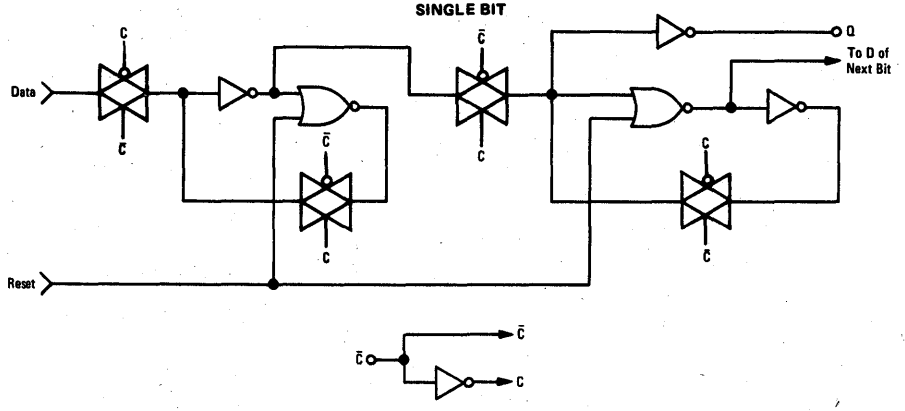
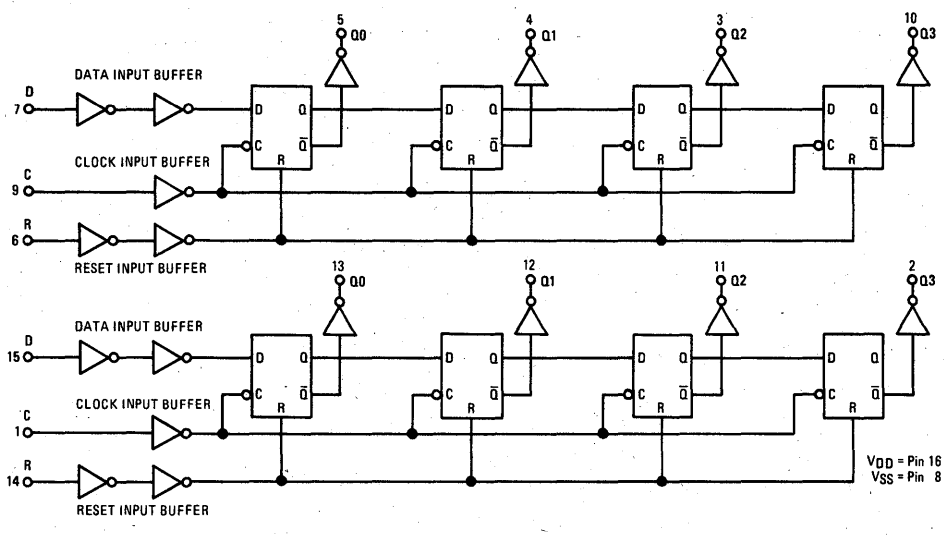
LOGIC DIAGRAMS

SINGLE BIT



COMPLETE DEVICE



MOTOROLA
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BOX 20912 • PHOENIX, ARIZONA 85036

MC14016B

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

The MC14016 quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC14016 consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

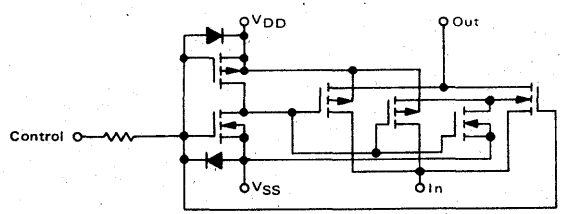
- High On/Off Output Voltage Ratio – 65 dB Typical
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches – 80 dB typical @ 1.0 MHz
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up to 54 MHz @ 5 Vdc
- Linearized Transfer Characteristics
- Low Noise – $12nV/\sqrt{Cycle}$, $f \geq 1$ kHz typical
- Pin-for-Pin Replacement for CD4016, CD4066

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the control inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} and V_{out} is not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

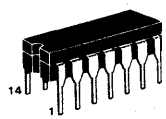
CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)



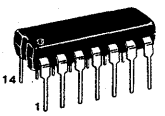
McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH
QUAD MULTIPLEXER



L SUFFIX
CERAMIC PACKAGE
CASE 632

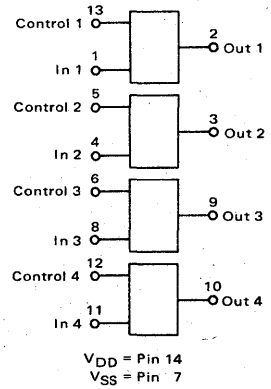


P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

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ELECTRICAL CHARACTERISTICS

Characteristics	Figure	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Voltage# Control Input	1	V_{IL}	5.0	–	–	–	1.5	0.9	–	–	Vdc
			10	–	–	–	1.5	0.9	–	–	
			15	–	–	–	1.5	0.9	–	–	
		V_{IH}	5.0	–	–	2.0	3.0	–	–	–	Vdc
			10	–	–	6.0	8.0	–	–	–	
			15	–	–	11	13	–	–	–	
Input Current (AL Device) Control	–	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device) Control	–	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance	–	C_{in}									pF
Control			–	–	–	–	5.0	–	–	–	
Switch Input			–	–	–	–	5.0	–	–	–	
Switch Output			–	–	–	–	5.0	–	–	–	
Feed Through			–	–	–	–	0.2	–	–	–	
Quiescent Current (AL Device)	2,3	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
(Per Package)			10	–	0.50	–	0.0010	0.50	–	15	
			15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	2,3	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
(Per Package)			10	–	2.0	–	0.0010	2.0	–	15	
			15	–	4.0	–	0.0015	4.0	–	30	
"ON" Resistance (AL Device)	4,5,6	R_{ON}									Ohms
($V_C = V_{DD}$, $R_L = 10\ k\Omega$)											
(V_{in} = +5.0 Vdc)			5.0	–	600	–	300	660	–	960	
(V_{in} = –5.0 Vdc) V_{SS} = –5 Vdc				–	600	–	300	660	–	960	
(V_{in} = ±0.25 Vdc)				–	600	–	280	660	–	960	
(V_{in} = +7.5 Vdc)			7.5	–	360	–	240	400	–	600	
(V_{in} = –7.5 Vdc) V_{SS} = –7.5 Vdc				–	360	–	240	400	–	600	
(V_{in} = ±0.25 Vdc)				–	360	–	180	400	–	600	
(V_{in} = +10 Vdc)			10	–	600	–	260	660	–	960	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	600	–	310	660	–	960	
(V_{in} = +5.6 Vdc)				–	600	–	310	660	–	960	
(V_{in} = +15 Vdc)			15	–	360	–	260	400	–	600	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	360	–	260	400	–	600	
(V_{in} = +9.3 Vdc)				–	360	–	300	400	–	600	
"ON" Resistance (CL/CP Device)	4,5,6	R_{ON}									Ohms
($V_C = V_{DD}$, $R_L = 10\ k\Omega$)											
(V_{in} = +5.0 Vdc)			5.0	–	610	–	300	660	–	840	
(V_{in} = –5.0 Vdc) V_{SS} = –5 Vdc				–	610	–	300	660	–	840	
(V_{in} = ±0.25 Vdc)				–	610	–	280	660	–	840	
(V_{in} = +7.5 Vdc)			7.5	–	370	–	240	400	–	520	
(V_{in} = –7.5 Vdc) V_{SS} = –7.5 Vdc				–	370	–	240	400	–	520	
(V_{in} = ±0.25 Vdc)				–	370	–	180	400	–	520	
(V_{in} = +10 Vdc)			10	–	610	–	260	660	–	840	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	610	–	260	660	–	840	
(V_{in} = +5.6 Vdc)				–	610	–	310	660	–	840	
(V_{in} = +15 Vdc)			15	–	370	–	260	400	–	520	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	370	–	260	400	–	520	
(V_{in} = +9.3 Vdc)				–	370	–	300	400	–	520	
Δ"ON" Resistance	–	ΔR_{ON}									Ohms
Between any 2 circuits in a common package											
($V_C = V_{DD}$)											
(V_{in} = ±5.0 Vdc) V_{SS} = –5 Vdc			5.0	–	–	–	15	–	–	–	
(V_{in} = ±7.5 Vdc) V_{SS} = –7.5 Vdc			7.5	–	–	–	10	–	–	–	
Input/Output Leakage Current ($V_C = V_{SS}$)	–	–									nAdc
(V_{in} = +5.0, V_{out} = –5.0 Vdc)			5.0	–	±125	–	±0.001	±125	–	–	
(V_{in} = –5.0, V_{out} = +5.0 Vdc)			5.0	–	±125	–	±0.001	±125	–	–	
(V_{in} = +7.5, V_{out} = –7.5 Vdc)			7.5	–	±250	–	±0.0015	±250	–	–	
(V_{in} = –7.5, V_{out} = +7.5 Vdc)			7.5	–	±250	–	±0.0015	±250	–	–	

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Input Voltage Specified as the voltage required at the Control Input for a 10 μA current through the transmission gate with an input-to-output stress of V_{DD}–V_{SS} for V_{IL} and V_{IH}.

NOTE: All unused control inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Propagation Delay Time (V_{SS} = 0 Vdc)	7	t_{PLH},	5.0	15	30	45	ns
V_{in} to V_{out}		t_{PHL}	10	7.0	10	15	
(V_C = V_{DD}, R_L = 1.0 kΩ)			15	6.0	7.5	12	
Control to Output	8		5.0	34	60	90	ns
(V_{in} ≤ 10 Vdc, R_L = 1.0 kΩ)			10	20	30	45	
			15	15	23	35	
Crosstalk, Control to Output (V_{SS} = 0 Vdc)	9	—	5.0	30	—	—	mV
(V_C = V_{DD}, R_{in} = 1.0 kΩ, R_{out} = 10 kΩ)			10	50	—	—	
			15	100	—	—	
Crosstalk between any two switches (V_{SS} = 0 Vdc)	—	—	5.0	−80	—	—	dB
(R_L = 1.0 kΩ, f = 1.0 MHz, crosstalk = $20 \log_{10} \frac{V_{out1}}{V_{out2}}$)							
Maximum Control Input Pulse Frequency (V_{SS} = 0 Vdc)	—	—	5.0	5.0	—	—	MHz
(R_L = 1.0 kΩ)			10	10	—	—	
			15	12	—	—	
Noise Voltage (V_{SS} = 0 Vdc)	10,11	—	5.0	24	—	—	nV/√Cycle
(V_C = V_{DD}, f = 100 Hz)			10	25	—	—	
			15	30	—	—	
(V_C = V_{DD}, f = 100 kHz)			5.0	12	—	—	
			10	12	—	—	
			15	15	—	—	
Sine Wave (Distortion) (V_{SS} = -5 Vdc)	—	—	5.0	0.16	—	—	%
(V_{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)							
Insertion Loss (V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = −5 Vdc, RMS centered = 0.0 Vdc, f = 1.0 MHz)	12	—	5.0				dB
I_{loss} = $20 \log_{10} \frac{V_{out}}{V_{in}}$							
(R_L = 1.0 kΩ)				2.3	—	—	
(R_L = 10 kΩ)				0.2	—	—	
(R_L = 100 kΩ)				0.1	—	—	
(R_L = 1.0 MΩ)				0.05	—	—	
Bandwidth (−3 dB)	12,13	BW	5.0				MHz
(V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = −5 Vdc, RMS centered @ 0.0 Vdc)							
(R_L = 1.0 kΩ)				54	—	—	
(R_L = 10 kΩ)				40	—	—	
(R_L = 100 kΩ)				38	—	—	
(R_L = 1.0 MΩ)				37	—	—	
Feedthrough (V_{SS} = −5 Vdc)	—	—	5.0				kHz
(V_C = V_{SS}, $20 \log_{10} \frac{V_{out}}{V_{in}}$ = −50 dB)							
(R_L = 1.0 kΩ)				1250	—	—	
(R_L = 10 kΩ)				140	—	—	
(R_L = 100 kΩ)				18	—	—	
(R_L = 1.0 MΩ)				2.0	—	—	

*The formula is for the typical characteristics only.

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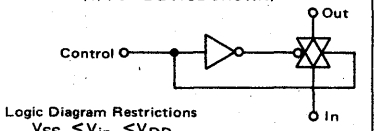
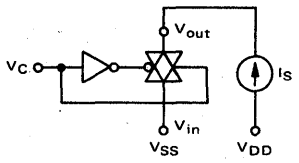
LOGIC DIAGRAM
(1/4 OF DEVICE SHOWN)



Logic Diagram Restrictions
$V_{SS} \leq V_{in} \leq V_{DD}$
$V_{SS} < V_{out} \leq V_{DD}$

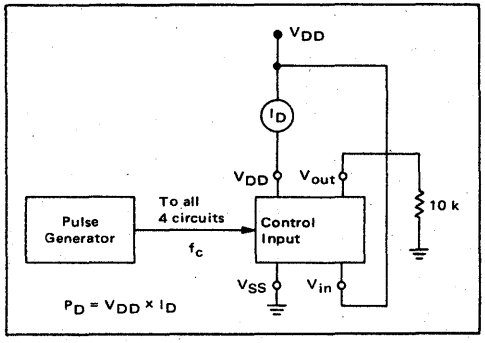
$V_{control}$	V_{in} to V_{out} Resistance
V_{SS}	$>10^9$ Ohms typ
V_{DD}	3×10^2 Ohms typ

FIGURE 1 – INPUT VOLTAGE TEST CIRCUIT



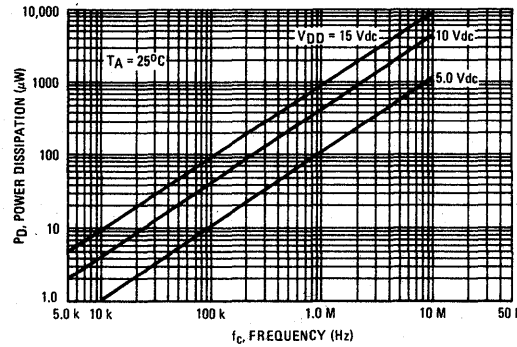
$V_{IL} = V_C$ when $I_S = 10\ \mu A$
$V_{IH} = V_{DD} - V_C$ when $I_S = 10\ \mu A$

FIGURE 2 – QUIESCENT POWER DISSIPATION TEST CIRCUIT



$P_D = V_{DD} \times I_D$

FIGURE 3 – TYPICAL POWER DISSIPATION PER CIRCUIT (1/4 OF DEVICE SHOWN)



TYPICAL R_{ON} versus INPUT VOLTAGE

FIGURE 4 – V_{SS} = –5.0 V AND –7.5 V

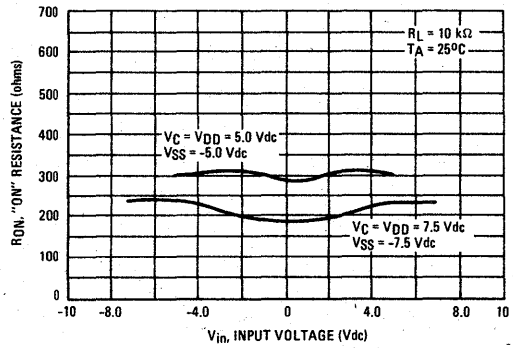


FIGURE 5 – V_{SS} = 0 V

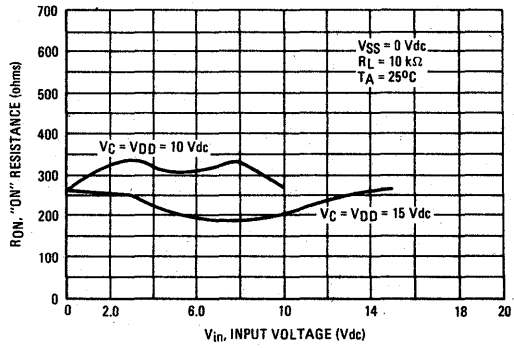


FIGURE 6 – R_{ON} CHARACTERISTICS TEST CIRCUIT

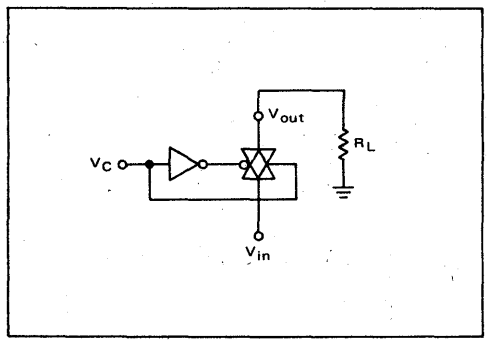


FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

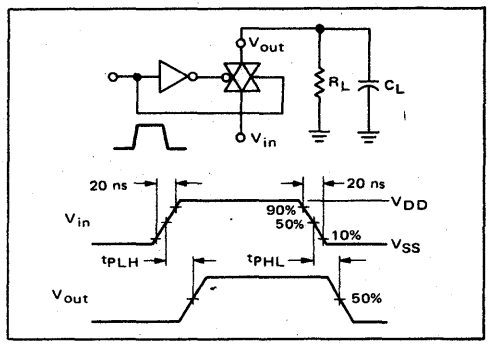


FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

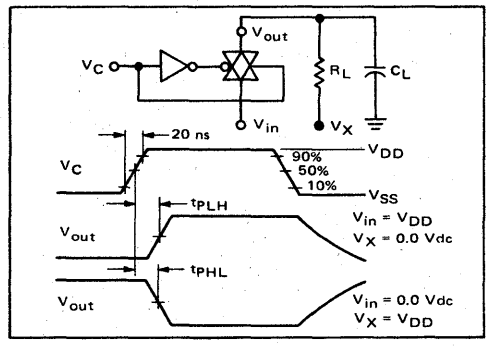


FIGURE 9 – CROSSTALK TEST CIRCUIT

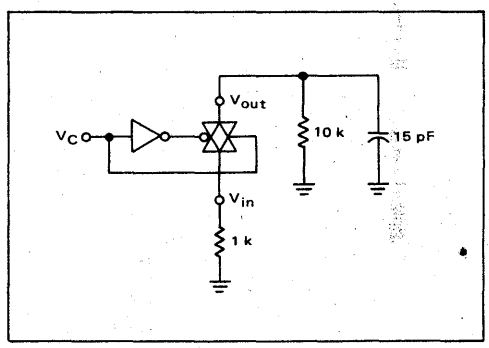


FIGURE 10 – NOISE VOLTAGE TEST CIRCUIT

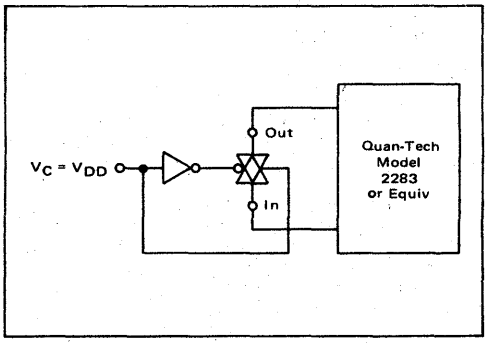


FIGURE 11 – TYPICAL NOISE CHARACTERISTICS

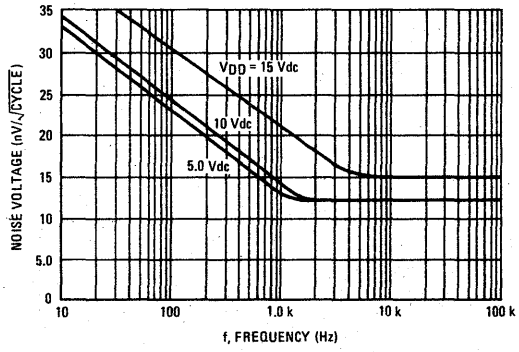


FIGURE 12 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS

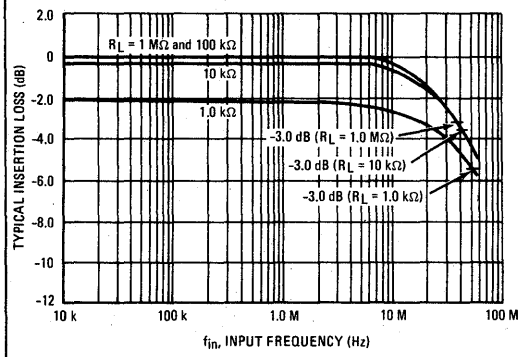
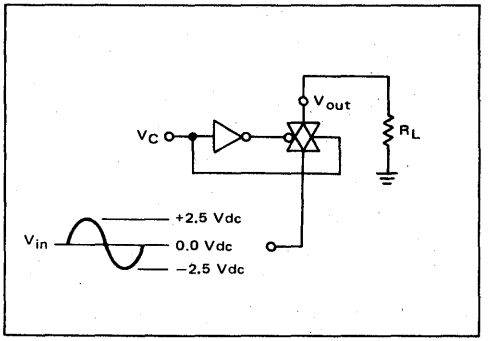


FIGURE 13 – FREQUENCY RESPONSE TEST CIRCUIT



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MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14017B

McMOS MSI

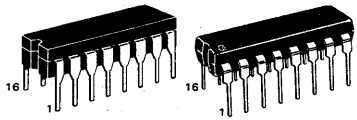
(LOW-POWER COMPLEMENTARY MOS)

DECADE COUNTER/DIVIDER

DECADE COUNTER/DIVIDER

The MC14017B is a five-stage Johnson decade counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation @ V_{DD} = 10 Vdc
- Divide-by-N Counting
- Quiescent Current = 5.0 nA/package Typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

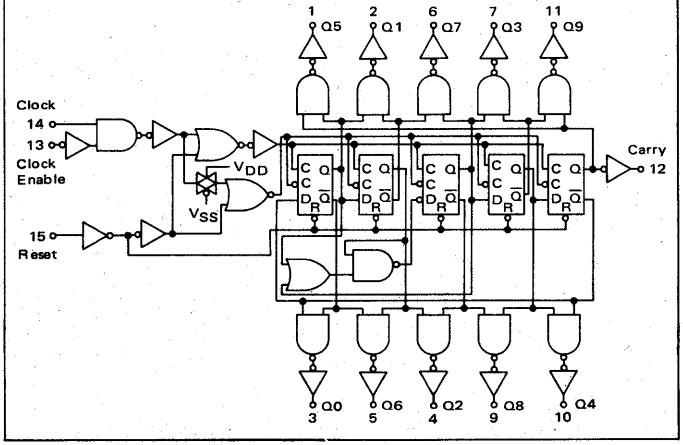
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FUNCTIONAL TRUTH TABLE
(Positive Logic)

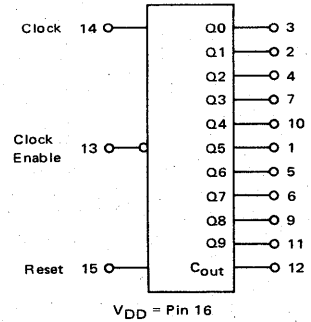
CLOCK	CLOCK ENABLE	RESET	DECODE OUTPUT = n
0	X	0	n
X	1	0	n
X	X	1	Q0
↓	0	0	n+1
↓	X	0	n
X	↓	0	n
1	↓	0	n+1

X = Don't Care If n < 5 Carry = "1", Otherwise = "0"

LOGIC DIAGRAM



BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.27 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.55 µA/kHz) f + I_{DD}							
		15	I_T = (0.83 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 1.1 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

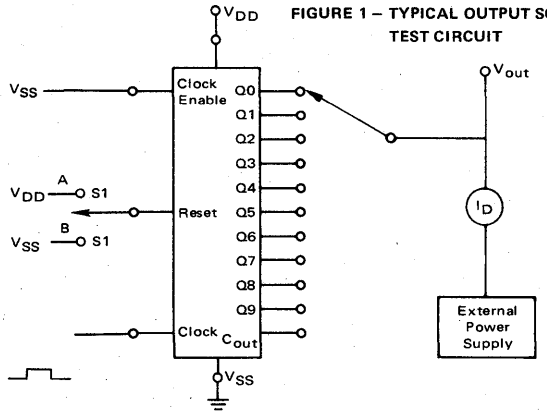
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time Reset to Decode Output	t_{PLH}, t_{PHL}							ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	–	500	750	1000	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	–	230	350	460	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 115 ns		15	–	–	140	250	350	
Propagation Delay Time Clock to C_{out}	t_{PLH}, t_{PHL}							ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	–	400	600	800	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	–	150	250	350	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	–	100	190	250	
Propagation Delay Time Clock to Decode Output	t_{PLH}, t_{PHL}							ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	–	500	750	1000	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	–	230	350	460	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 115 ns		15	–	–	140	250	350	
Turn-Off Delay Time Reset to C_{out}	t_{PLH}							ns
t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	–	400	600	800	
t_{PLH} = (0.66 ns/pF) C_L + 117 ns		10	–	–	150	250	350	
t_{PLH} = (0.5 ns/pF) C_L + 75 ns		15	–	–	100	190	250	
Minimum Clock Pulse Width	PW_C	5.0	–	–	100	200	250	ns
		10	–	–	42	70	100	
		15	–	–	30	55	75	
Maximum Clock Frequency	PRF	5.0	2.5	2.0	5.0	–	–	MHz
		10	7.0	5.0	12	–	–	
		15	9.3	6.7	16	–	–	
Minimum Reset Pulse Width	PW_R	5.0	–	–	200	330	500	ns
		10	–	–	100	165	250	
		15	–	–	75	125	190	
Reset Removal Time	t_{rem}	5.0	–	–	300	500	750	ns
		10	–	–	100	200	275	
		15	–	–	80	150	210	
Maximum Clock Input Rise and Fall Time	t_r,t_f	5.0	No Limit					–
		10						
		15						
Clock Enable Setup Time	t_{setup}	5.0	–	–	175	300	700	ns
		10	–	–	75	150	300	
		15	–	–	52	115	225	
Clock Enable Release Time	t_{rel}	5.0	–	–	260	405	700	ns
		10	–	–	100	200	300	
		15	–	–	70	150	225	

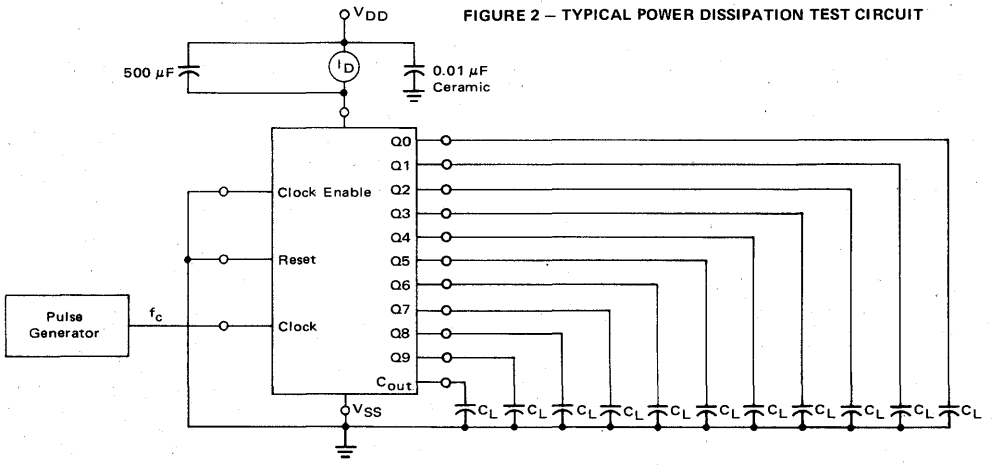
*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



	OUTPUT SINK DRIVE	OUTPUT SOURCE DRIVE
DECODE OUTPUTS	(S1 to A)	Clock to desired outputs (S1 to B)
Carry	Clock to 5 thru 9 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT



APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 3 – COUNTER EXPANSION

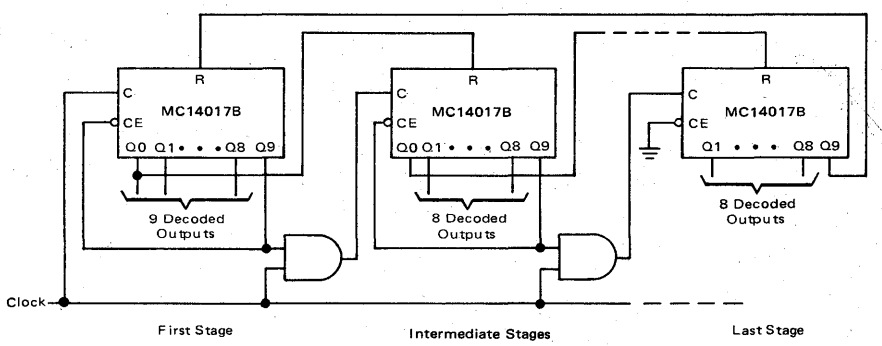
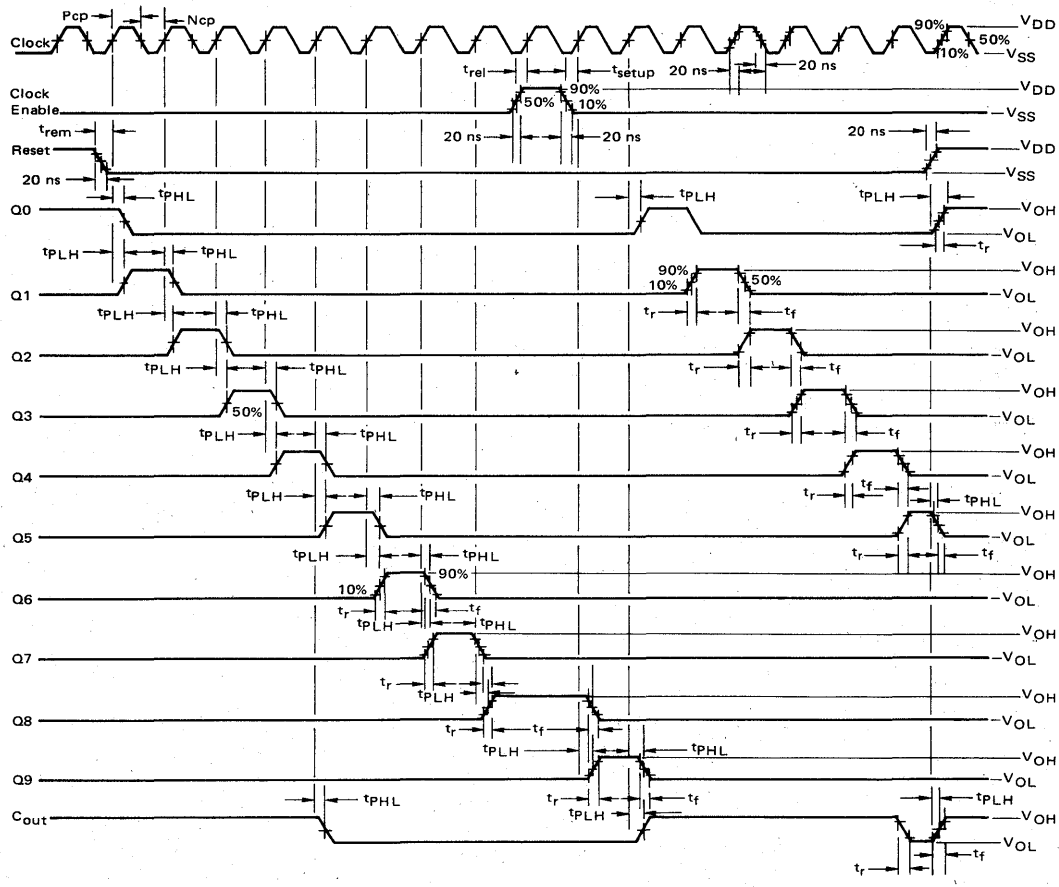


FIGURE 4 – AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14018B

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PRESETTABLE DIVIDE-BY-N COUNTER

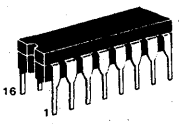
PRESETTABLE DIVIDE-BY-N COUNTER

The MC14018B contains five Johnson counter stages which are asynchronously presettable and resettable. The counters are synchronous, and increment on the positive going edge of the clock.

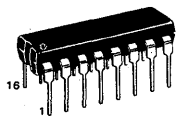
Presetting is accomplished by a logic 1 on the preset enable input. Data on the Jam inputs will then be transferred to their respective $\overline{Q}$ outputs (inverted). A logic 1 on the reset input will cause all $\overline{Q}$ outputs to go to a logic 1 state.

Division by any number from 2 to 10 can be accomplished by connecting appropriate $\overline{Q}$ outputs to the data input, as shown in the Function Selection table. Anti-lock gating is included in the MC14018B to assure proper counting sequence.

- Fully Static Operation
- Medium Speed — 6.5 MHz typical @ 10 V
- Schmitt Trigger on Clock Input
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4018



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

5

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

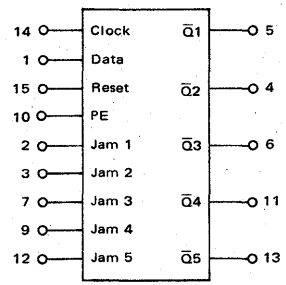
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FUNCTIONAL TRUTH TABLE

Clock	Reset	Preset Enable	Jam Input	$\overline{Q}n$
↓	0	0	X	$\overline{Q}n$
↑	0	0	X	$\overline{D}n^*$
X	0	1	0	1
X	0	1	1	0
X	1	X	X	1

*D_n is the Data input for that stage. Stage 1 has Data brought out to Pin 1.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.7 µA/kHz) f + I_{DD}							
		15	I_T = (1.0 µA/kHz) f + I_{DD}							

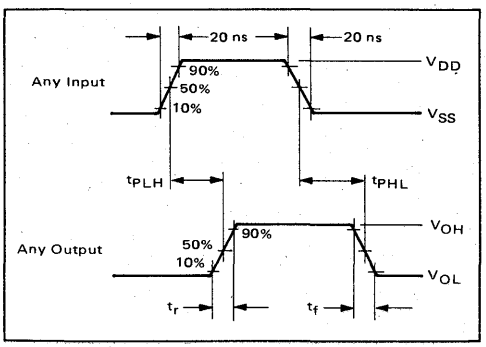
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

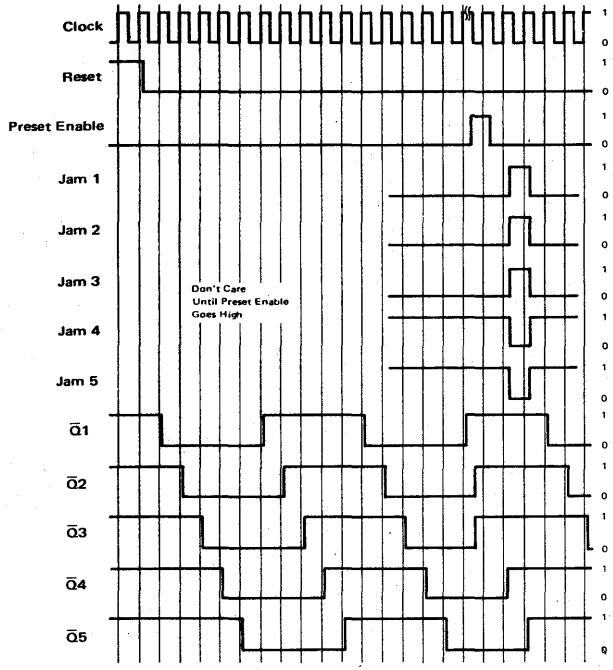
Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Output Rise and Fall Time	t_r, t_f					ns
t_r,t_f = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_r,t_f = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_r,t_f = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to $\overline{Q}$	t_{PHL}					
t_{PLH},t_{PHL} = (0.90 ns/pF) C_L + 265 ns		5.0	–	310	620	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 102 ns		10	–	120	240	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 72 ns		15	–	85	170	
Reset to $\overline{Q}$						ns
t_{PLH} = (0.90 ns/pF) C_L + 325 ns		5.0	–	370	740	
t_{PLH} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH} = (0.26 ns/pF) C_L + 81 ns		15	–	100	200	
Preset Enable to $\overline{Q}$						ns
t_{PLH},t_{PHL} = (0.90 ns/pF) C_L + 325 ns		5.0	–	370	740	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 81 ns		15	–	100	200	
Minimum Setup Time	t_{setup}					ns
Data (Pin 1) to Clock		5.0	–	0	200	
		10	–	0	100	
		15	–	0	80	
Jam Inputs to Preset Enable		5.0	–	0	200	ns
		10	–	0	100	
		15	–	0	80	
Data (Jam Inputs)-to-Preset Enable Hold Time	t_{hold}	5.0	–	270	540	ns
		10	–	250	500	
		15	–	240	480	
Minimum Clock Pulse Width	PW_C	5.0	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
Minimum Reset or Preset Enable Pulse Width	PW_R, PW_{PE}	5.0	–	145	290	ns
		10	–	65	130	
		15	–	55	110	
Maximum Clock Rise and Fall Time	t_r,t_f	5.0	No Limit			ns
		10				
		15				
Maximum Clock Pulse Frequency	PRF					MHz
		5.0	1.25	2.5	–	
		10	3.25	6.5	–	
		15	4.0	8.0	–	

*The formulas given are for the typical characteristics only.

FIGURE 1 – SWITCHING TIME WAVEFORMS



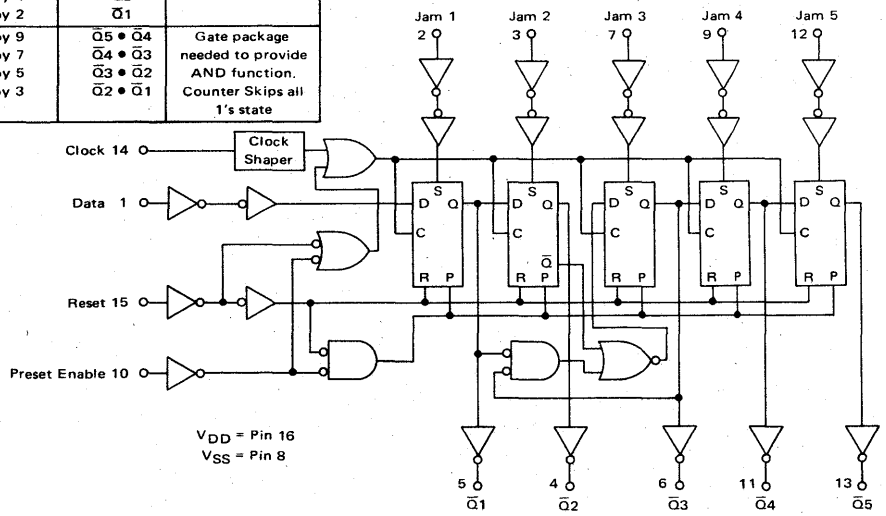
TIMING DIAGRAM
($\overline{Q5}$ Connected to Data Input)



FUNCTION SELECTION

Counter Mode	Connect Data Input (Pin 1) to:	Comments
Divide by 10	$\overline{Q5}$	No external components needed.
Divide by 8	$\overline{Q4}$	
Divide by 6	$\overline{Q3}$	
Divide by 4	$\overline{Q2}$	
Divide by 2	$\overline{Q1}$	
Divide by 9	$\overline{Q5} \bullet \overline{Q4}$	Gate package needed to provide AND function. Counter Skips all 1's state
Divide by 7	$\overline{Q4} \bullet \overline{Q3}$	
Divide by 5	$\overline{Q3} \bullet \overline{Q2}$	
Divide by 3	$\overline{Q2} \bullet \overline{Q1}$	

LOGIC DIAGRAM



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MC14020B

14-BIT BINARY COUNTER

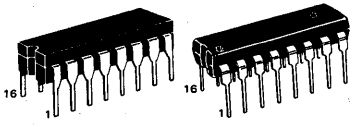
The MC14020B 14-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

- Fully Static Operation
- Quiescent Current =5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Low Input Capacitance = 5.0pF typical
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- 13 MHz Typical Counting Rate @ V_{DD} = 15V
- Pin-for-Pin Replacement for CD4020

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

14-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

5

MAXIMUM RATINGS (Voltages referenced to V_{SS})

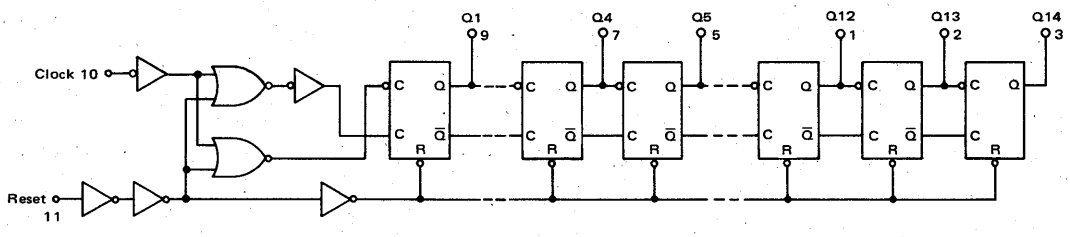
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
⎍	0	No Change
⎎	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



Q6 = Pin 4
Q7 = Pin 6
Q8 = Pin 13

Q9 = Pin 12
Q10 = Pin 14
Q11 = Pin 15

V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.42 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.85 µA/kHz) f + I_{DD}							
		15	I_T = (1.43 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L +30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L +15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L +10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L +25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L +12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L +9.5 ns		15	–	–	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}							ns
Clock to Q1								
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	–	400	600	750	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns		10	–	–	170	255	300	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 95 ns		15	–	–	120	180	230	
Clock to Q14								μs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 2715 ns		5.0	–	–	2.8	5.6	8.4	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 967 ns		10	–	–	1.0	2.0	3.0	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 575 ns		15	–	–	0.6	1.5	2.5	
Propagation-Delay Time	t_{PHL}							ns
Reset to Q_n								
t_{PHL} = (1.7 ns/pF) C_L + 510 ns		5.0	–	–	595	3000	3500	
t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	–	230	775	900	
t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	–	–	180	580	680	
Minimum Clock Pulse Width	PW_C	5.0	–	–	140	335	500	ns
		10	–	–	55	125	165	
		15	–	–	38	95	125	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	3.5	–	–	MHz
		10	4.0	3.0	9.0	–	–	
		15	5.0	4.0	13	–	–	
Maximum Clock Rise and Fall Time	t_r,t_f	5.0	No	No	–	–	–	–
		10	Limit	Limit	–	–	–	
		15			–	–	–	
Minimum Reset Pulse Width	PW_R	5.0	–	–	320	2500	3000	ns
		10	–	–	120	475	550	
		15	–	–	80	355	420	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

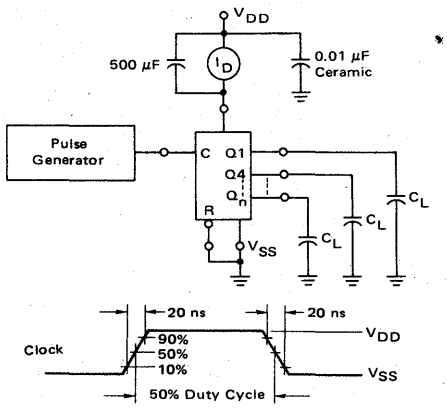


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

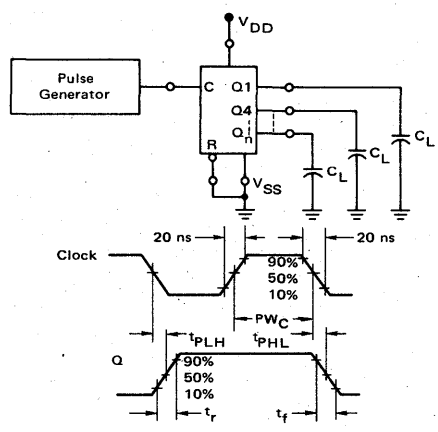
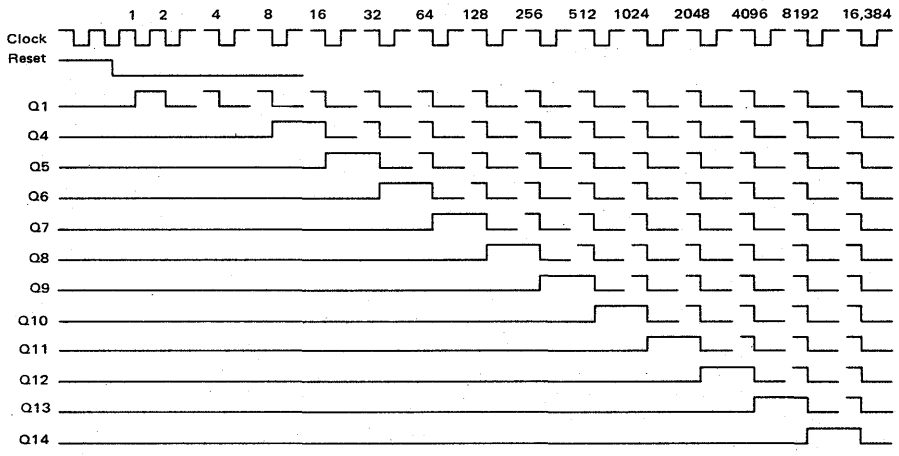


FIGURE 3 – TIMING DIAGRAM



5

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MC14021B

FOR COMPLETE DATA
SEE MC14014B

McMOS MSI

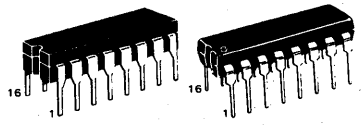
(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER

8-BIT STATIC SHIFT REGISTER

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation from DC to 7.0 MHz
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.
- MC14014B Pin-for-Pin Replacement for CD4014
- MC14021B Pin-for-Pin Replacement for CD4021



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

SERIAL OPERATION:

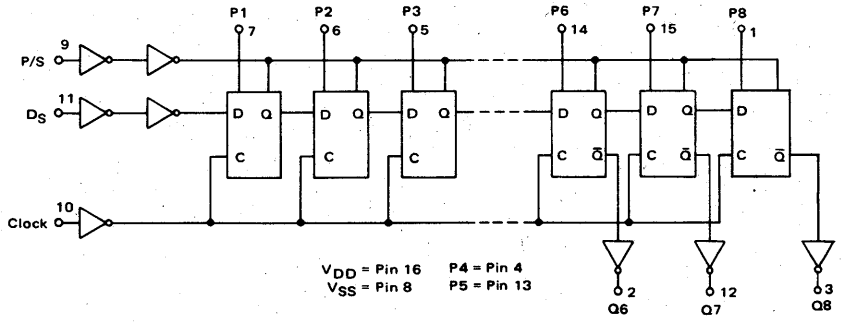
t	CLOCK	D_S	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n		0	0	0	?	?
n+1		1	0	1	0	?
n+2		0	0	0	1	0
n+3		1	0	1	0	1
		X	0	Q6	Q7	Q8

PARALLEL OPERATION:

CLOCK	D_S	P/S	D_m	$*Q_m$
	X	1	0	0
	X	1	1	1

*Q6, Q7, & Q8 are available externally
X = Don't Care

LOGIC DIAGRAM



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MC14022B

OCTAL COUNTER/DRIVER

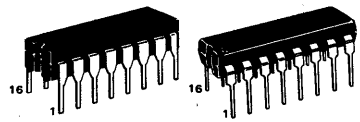
The MC14022B is a four-stage Johnson octal counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation @ V_{DD} = 10 Vdc
- Divide-by-N Counting
- Quiescent Current = 5.0 nA/package Typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4022

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

OCTAL COUNTER/DIVIDER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

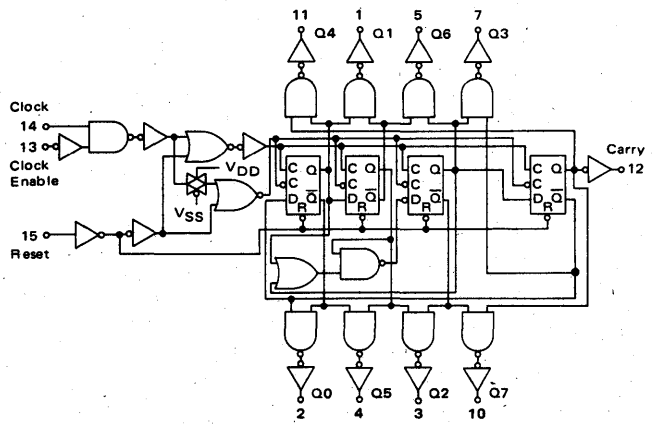
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FUNCTIONAL TRUTH TABLE
(Positive Logic)

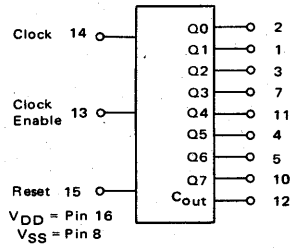
CLOCK	CLOCK ENABLE	RESET	OUTPUT = n
0	X	0	n
X	1	0	n
↓	0	0	n+1
↓	X	0	n
1	↓	0	n+1
X	↓	0	n
X	X	1	Q0

X = Don't Care If n< 4 Carry = 1, Otherwise = 0

LOGIC DIAGRAM



BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}				*					Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.28 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.56 μA/kHz) f + I_{DD}							
		15	I_T = (0.85 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 1.25 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

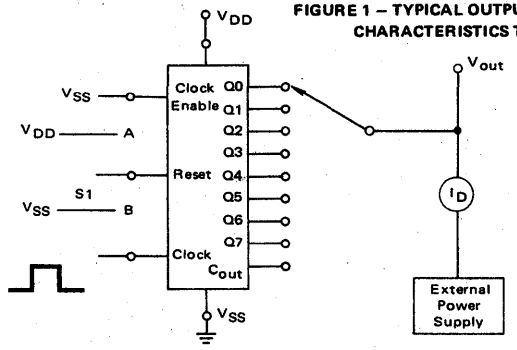
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time Reset to Decode Output	t_{PLH}, t_{PHL}							ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	–	500	750	1000	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	–	230	350	460	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 115 ns		15	–	–	140	250	350	
Propagation Delay Time Clock to C_{out}	t_{PLH}, t_{PHL}							ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	–	400	600	800	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	–	150	250	350	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	–	100	190	250	
Propagation Delay Time Clock to Decode Output	t_{PLH}, t_{PHL}							ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	–	500	750	1000	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	–	230	350	460	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 115 ns		15	–	–	140	250	350	
Turn-Off Delay Time Reset to C_{out}	t_{PLH}							ns
t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	–	400	600	800	
t_{PLH} = (0.66 ns/pF) C_L + 117 ns		10	–	–	150	250	350	
t_{PLH} = (0.5 ns/pF) C_L + 75 ns		15	–	–	100	190	250	
Minimum Clock Pulse Width	PW_C	5.0	–	–	100	200	250	ns
		10	–	–	42	70	100	
		15	–	–	30	55	75	
Maximum Clock Frequency	PRF	5.0	2.5	2.0	5.0	–	–	MHz
		10	7.0	5.0	12	–	–	
		15	9.3	6.7	16	–	–	
Minimum Reset Pulse Width	PW_R	5.0	–	–	200	330	500	ns
		10	–	–	100	165	250	
		15	–	–	75	125	190	
Reset Removal Time	t_{rem}	5.0	–	–	300	500	750	ns
		10	–	–	100	200	275	
		15	–	–	80	150	210	
Maximum Clock Input Rise and Fall Time	t_r,t_f	5.0	No Limit					–
		10						
		15						
Clock Enable Setup Time	t_{setup}	5.0	–	–	175	300	700	ns
		10	–	–	75	150	300	
		15	–	–	52	115	225	
Clock Enable Release Time	t_{rel}	5.0	–	–	260	405	700	ns
		10	–	–	100	200	300	
		15	–	–	70	150	225	

*The formula given is for the typical characteristics only.

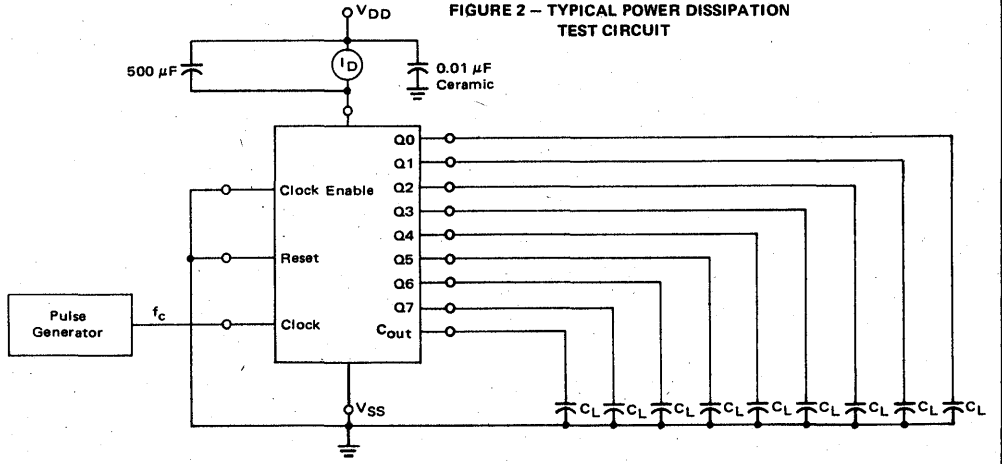
5

FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



Outputs	Output Sink Drive (S1 to A)	Output Source Drive: Clock to desired Output (S1 to B)
Carry	Clock to Q5 thru Q7 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

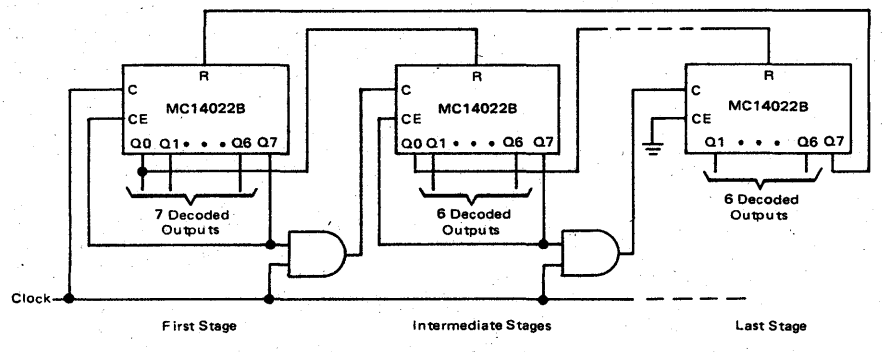
FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT



APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 3 – COUNTER EXPANSION



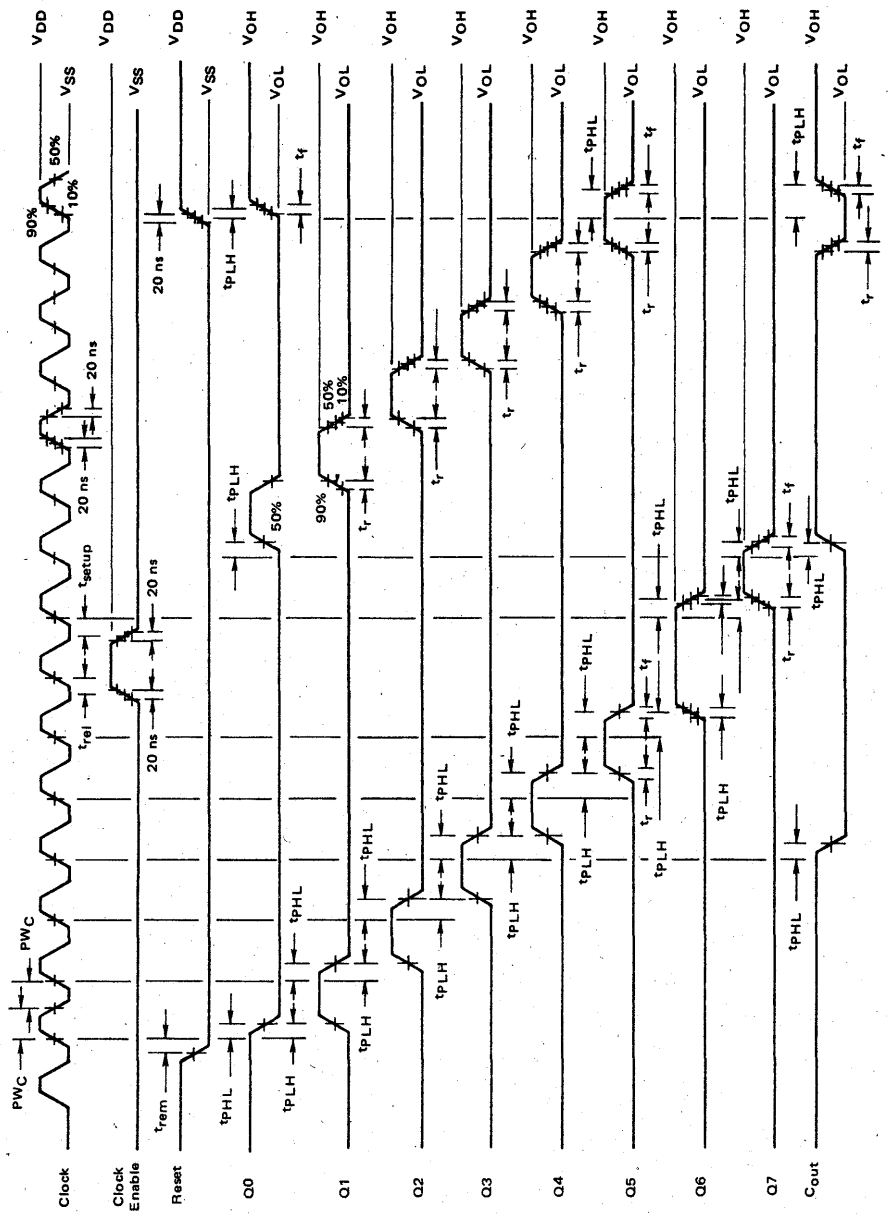


FIGURE 4 – AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS

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MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14023
MC14023B

TRIPLE 3-INPUT "NAND" GATE

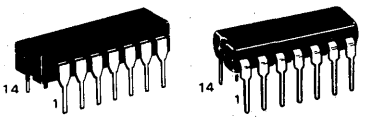
The MC14023 and MC14023B are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14023B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14023B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4023A and CD4023B

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

Delete for Non-B Device

- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

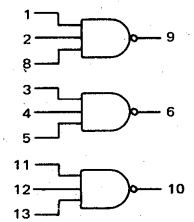
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

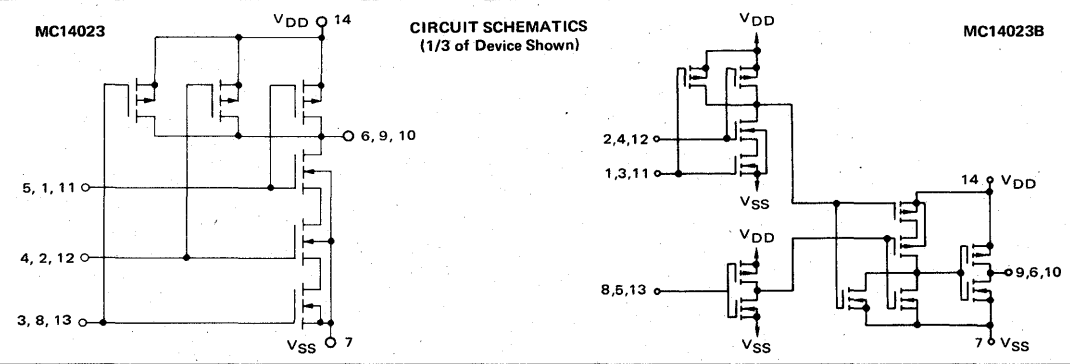
See the MC14001 data sheet for complete characteristics for the non-B device.

See the MC14001B data sheet for complete characteristics of the B-Series device.

LOGIC DIAGRAM



CIRCUIT SCHEMATICS
(1/3 of Device Shown)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14024B

McMOS SSI

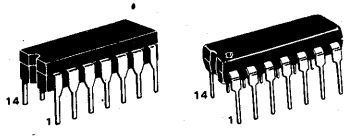
(LOW-POWER COMPLEMENTARY MOS)

SEVEN STAGE
RIPPLE COUNTER

SEVEN STAGE RIPPLE COUNTER

The MC14024B is a seven stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity (typically 45% of V_{DD}), however the Clock input has a typical noise immunity of 70% of V_{DD} with no maximum Clock input rise or fall time. The output of each counter stage is buffered.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
- 8-MHz Operation @ V_{DD} = 10 Vdc typical
- Exceedingly Slow Input Transition Rates may be Applied to the Clock Input
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4024



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

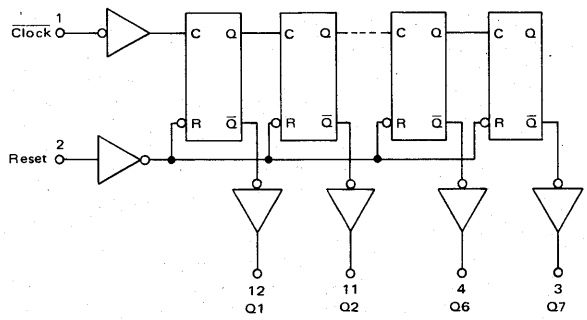
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

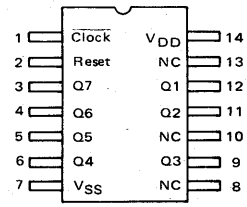
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



Q3 = Pin 9
Q4 = Pin 6
Q5 = Pin 5

PIN ASSIGNMENT



V_{DD} = Pin 14
V_{SS} = Pin 7

NC = No Connection

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.31 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.60 μA/kHz) f + I_{DD}							
		15	I_T = (0.89 μA/kHz) f + I_{DD}							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time	t_{PLH},							ns
Clock to Q1	t_{PHL}							
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 295 ns		5.0	–	–	380	490	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	–	150	195	230	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	–	110	150	175	
Clock to Q7								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 915 ns		5.0	–	–	1000	2000	3000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 367 ns		10	–	–	400	545	750	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 275 ns		15	–	–	300	410	565	
Reset to Q_n								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	–	500	700	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	–	–	250	350	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	–	–	180	260	300	
Minimum Clock Pulse Width	PW_C	5.0	–	–	200	330	500	ns
		10	–	–	60	125	165	
		15	–	–	40	95	125	
Minimum Reset Pulse Width	PW_R	5.0	–	–	375	500	600	ns
		10	–	–	200	300	350	
		15	–	–	150	225	260	
Reset Removal Time	t_{rem}	5.0	–	–	250	375	625	ns
		10	–	–	75	110	190	
		15	–	–	50	85	145	
Maximum Clock Input Rise and Fall Times	t_r, t_f	5.0	No Limit	No Limit	–	–	–	–
		10			–	–	–	
/		15			–	–	–	
Maximum Input Pulse Frequency	f_{max}	5.0	1.5	1.0	2.5	–	–	MHz
		10	4.0	3.0	8.0	–	–	
		15	5.3	4.0	12	–	–	

*The formula given is for the typical characteristics only.

TRUTH TABLE

$\overline{CLOCK}$	RESET	STATE
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
⌐	0	No Change
⌐	1	All Outputs Low
⌐	0	Advance One Count
⌐	1	All Outputs Low

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

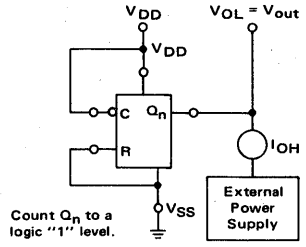


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

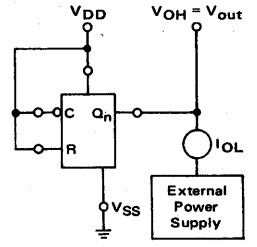


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT

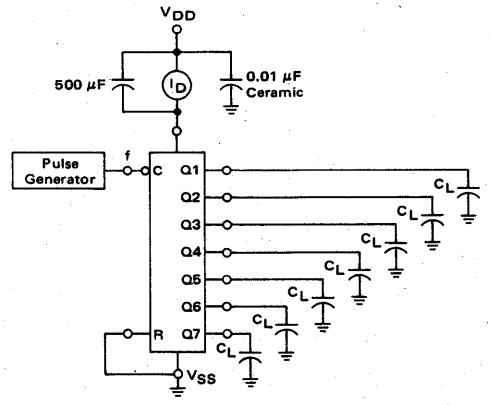


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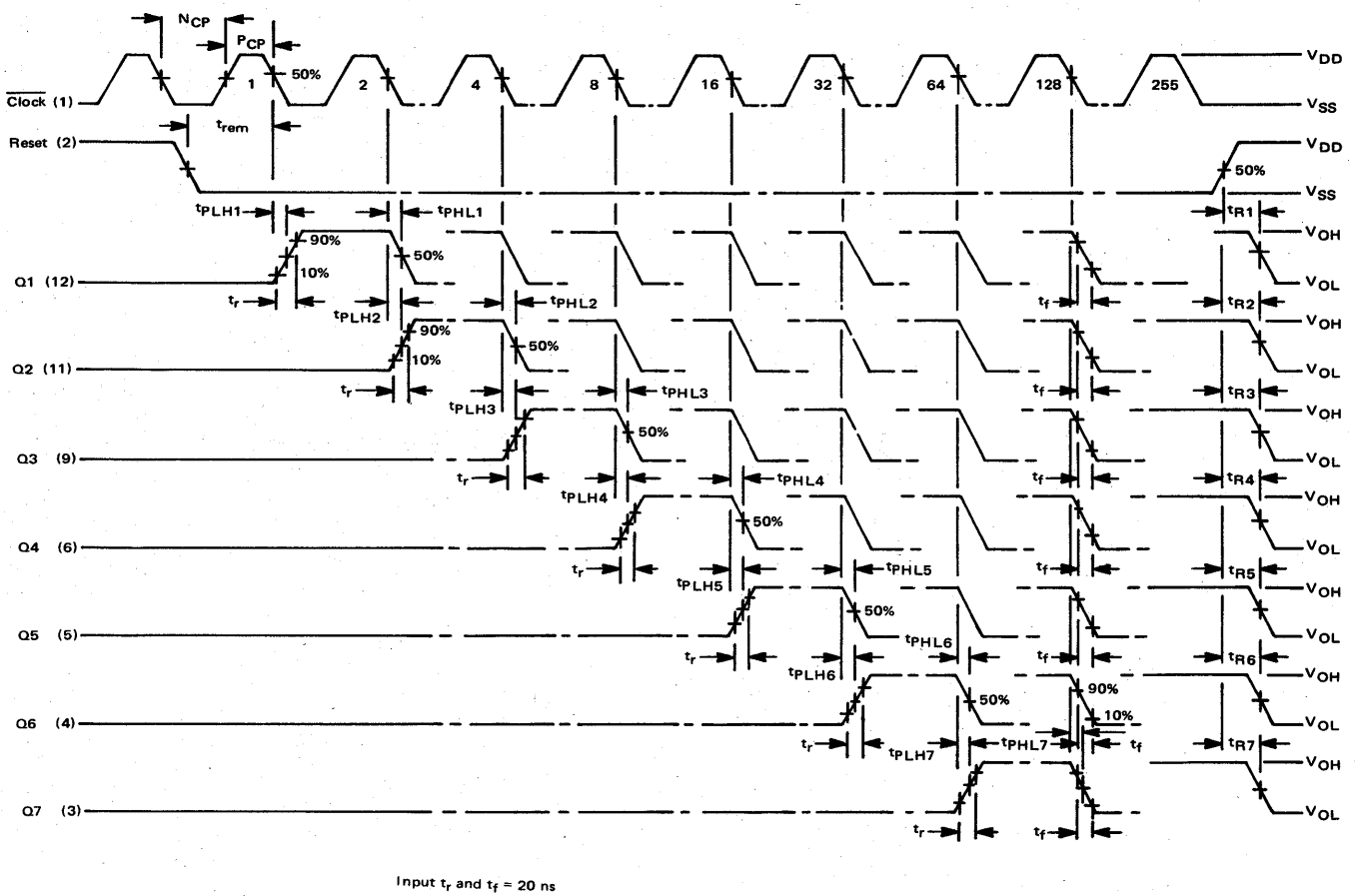
FIGURE 4 – FUNCTIONAL WAVEFORMS



Input t_r and t_f = 20 ns

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MC14025
MC14025B

TRIPLE 3-INPUT "NOR" GATE

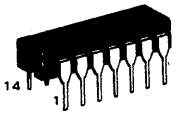
The MC14025 and MC14025B are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14025B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14025B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4025A and CD4025B

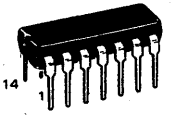
McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

Delete for Non-B Device

- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

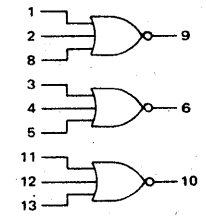
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001 data sheet for complete characteristics for the non-B device.

See the MC14001B data sheet for complete characteristics of the B-Series device.

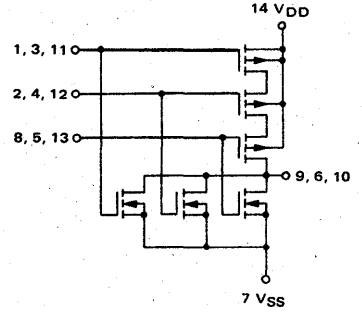
LOGIC DIAGRAM



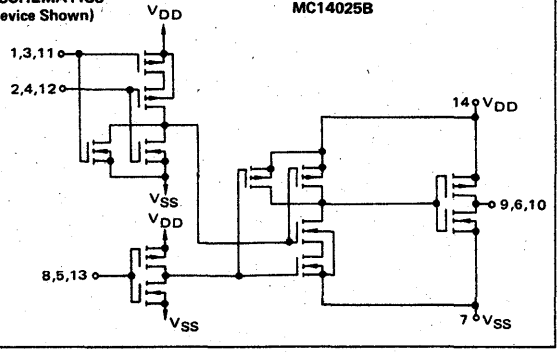
V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATICS
(1/3 of Device Shown)

MC14025



MC14025B



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MC14027B

DUAL J-K FLIP-FLOP

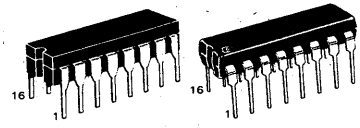
The MC14027B dual J-K flip-flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- Toggle Rate = 3.0 MHz typical @ 5 Vdc
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design – Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4027

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL J-K FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

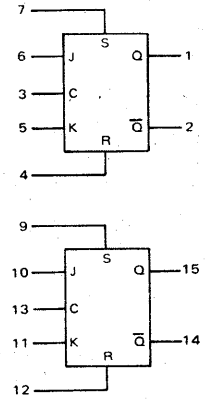
TRUTH TABLE

INPUTS						OUTPUTS*	
C†	J	K	S	R	Q_n‡	Q_{n+1}	$\overline{Q_{n+1}}$
↑	1	X	0	0	0	1	0
↑	X	0	0	0	1	1	0
↑	0	X	0	0	0	0	1
↑	X	1	0	0	1	0	1
↓	X	X	0	0	X	Q_n	$\overline{Q_n}$
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

No Change

X = Don't Care
† = Level Change
‡ = Present State
* = Next State

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.80 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.60 µA/kHz) f + I_{DD}							
		15	I_T = (2.40 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

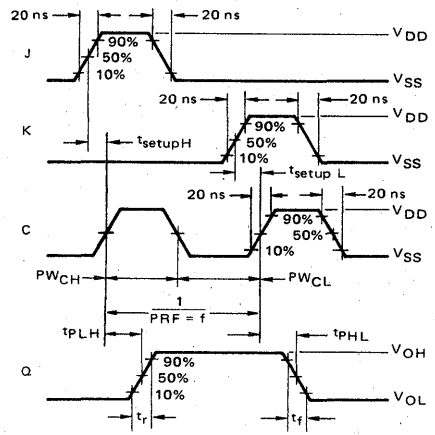
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min		Typ	Max		Unit
			AL Device	CL/CLP Device	All Types	AL Device	CL/CP Device	
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	360	360	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	180	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	130	130	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	200	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	100	100	
t_f = (0.55 ns/pF) C_L + 12.5 ns		15	–	–	40	80	80	
Propagation Delay Time	t_{PLH}, t_{PHL}							ns
Clock to Q								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	–	175	350	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	–	75	150	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	–	50	100	100	
Set to Q								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	–	175	350	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	–	75	150	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	–	50	100	100	
Reset to Q								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	–	350	450	450	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	–	100	200	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 50 ns		15	–	–	75	150	150	
Minimum Setup Times	$t_{setup\ H}$	5.0	–	–	70	140	140	ns
	$t_{setup\ L}$	10	–	–	25	50	50	
		15	–	–	17	35	35	
Minimum Clock Pulse Width	PW_{CH}, PW_{CL}	5.0	–	–	165	330	330	ns
		10	–	–	55	110	110	
		15	–	–	38	75	75	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.5	3.0	–	–	MHz
		10	4.5	4.5	9.0	–	–	
		15	6.5	6.5	13	–	–	
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0	15	15	–	–	–	μs
		10	5.0	5.0	–	–	–	
		15	4.0	4.0	–	–	–	
Minimum Set and Reset Pulse Width	PW_S, PW_R	5.0	–	–	125	250	250	ns
		10	–	–	50	100	100	
		15	–	–	35	70	70	

*The formula given is for the typical characteristics only.

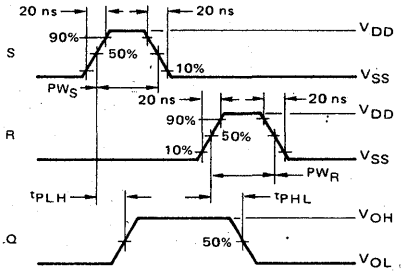
5

FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS
(J, K, Clock, and Output)



Inputs R and S low.
For the measurement of PW_C, PRF, and P_D the Inputs J and K are kept high.

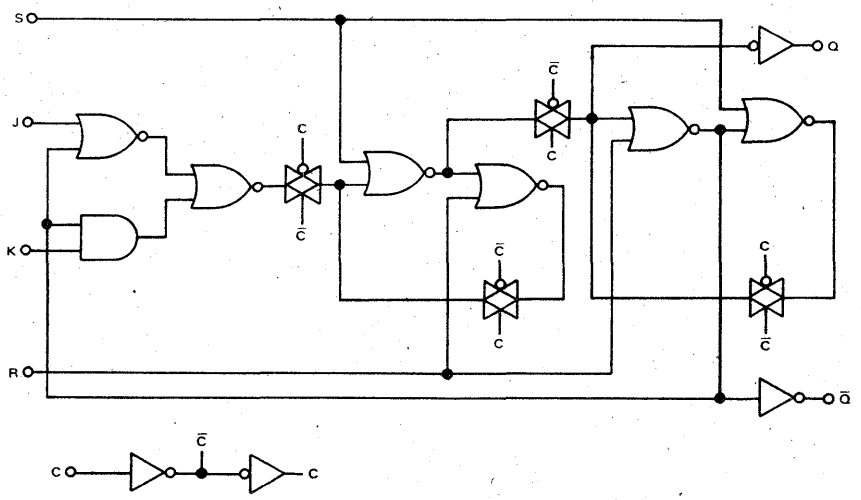
FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, and Output)



Inputs J and K low.

5

LOGIC DIAGRAM
(1/2 of Device Shown)



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14028B

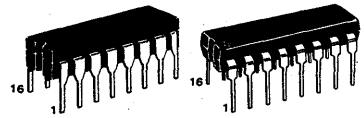
McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-DECIMAL DECODER
BINARY-TO-OCTAL DECODER

The MC14028B decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic "0". Expanded decoding such as binary-to-hexadecimal (one-of-16), etc., can be achieved by using other MC14028B devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or readout decoding.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Positive Logic Design
- Quiescent Current 5.0 nA /package typical @ 5 Vdc
- Low Outputs on All Illegal Input Combinations
- Pin-for-Pin Replacement for CD4028



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

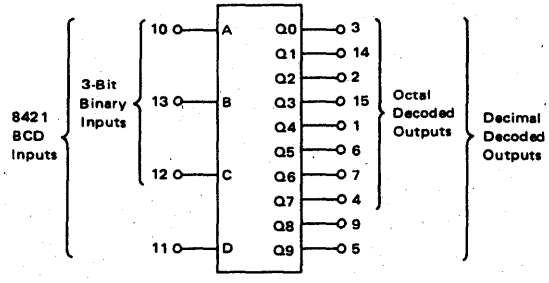
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUT				OUTPUT									
D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	0	1	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0	0	0
1	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.6 µA/kHz) f + I_{DD}							
		15	I_T = (0.9 µA/kHz) f + I_{DD}							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

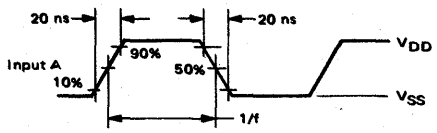
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns	t_{PHL}	5.0	300	480	700	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	130	200	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	90	140	200	

*The formula given is for the typical characteristics only.

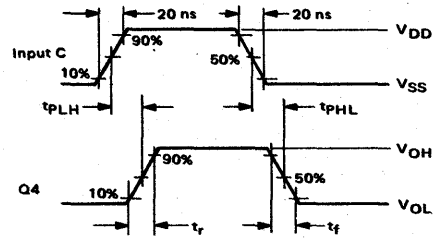
FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS

Inputs B, C, and D switching in respect to a BCD code.



All outputs connected to respective C_L loads. f in respect to a system clock.

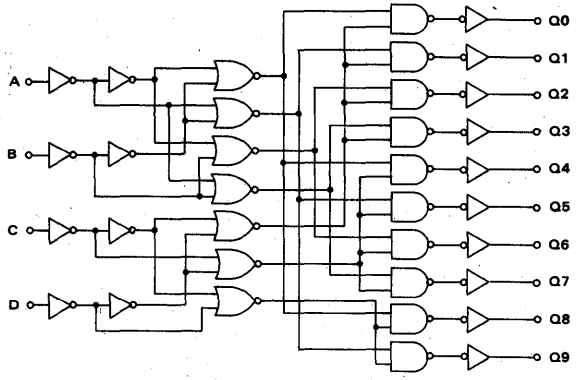
Inputs A, B, and D low.



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

LOGIC DIAGRAM

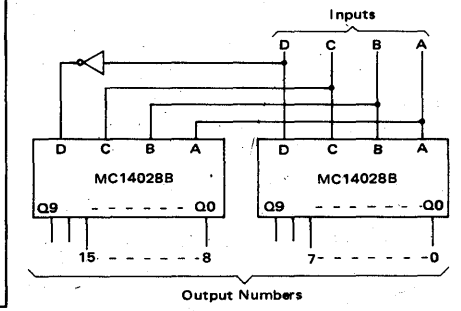


APPLICATION INFORMATION

Expanded decoding can be performed by using the MC14028B and other McMOS Integrated Circuits. The circuits in Figure 2 converts any 4-bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA = 0111 the output number 7 is redefined for the 4-bit binary, 4-bit gray, excess-3, or excess-3 gray codes as 7, 5, 4, or 2, respectively. Figure 3 shows a 6-bit binary 1-of-64 decoder using nine MC14028B circuits and two MC14069B inverters.

The MC14028B can be used in decimal digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.

FIGURE 2 – CODE CONVERSION CIRCUIT AND TRUTH TABLE



INPUTS				OUTPUT NUMBERS														CODE AND REDEFINED OUTPUT NUMBERS					
																		Hexadecimal		Decimal			
D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4-Bit Binary	4-Bit Gray	Excess-3	Excess-3 Gray	Aiken	4221
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0			0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1			1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3		0	2	2
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	3	2	0	3	3	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	4	7	1	4	4	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	5	6	2			3
0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	6	4	3	1		4
0	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	7	5	4	2		
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	8	15	5			
1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	9	14	6			5
1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	10	12	7	9		6
1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	11	13	8		5	
1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6	
1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	13	9		6	7	7
1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	14	11		8	8	8
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15	10		7	9	9

FIGURE 3 – SIX-BIT BINARY 1-OF-64 DECODER

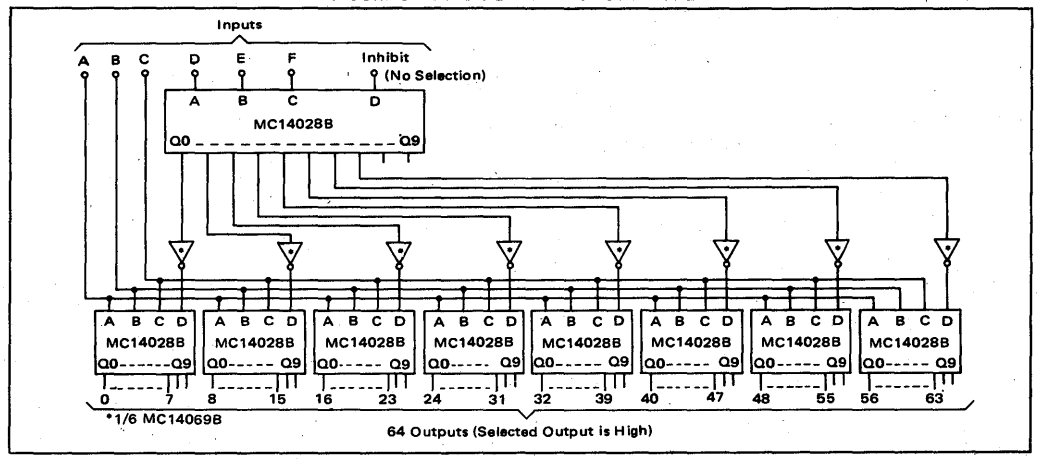
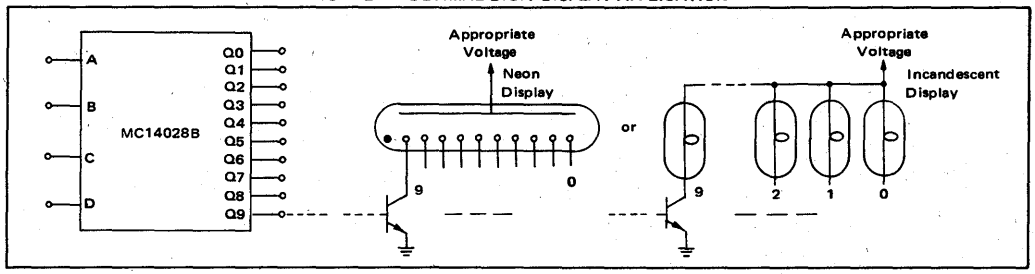


FIGURE 4 – DECIMAL DIGIT DISPLAY APPLICATION



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14032B
MC14038B

McMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

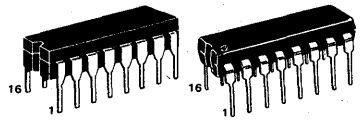
TRIPLE SERIAL ADDERS

Positive Logic — MC14032B
Negative Logic — MC14038B

TRIPLE SERIAL ADDERS

The MC14032B and MC14038B triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032B, and on the negative-going clock transition for the MC14038B. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers.

- Static Operation from dc to 5.0 MHz
- Buffered Outputs
- Single-Phase Clocking
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4032 and CD4038



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

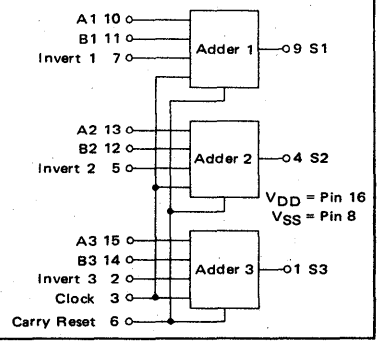
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

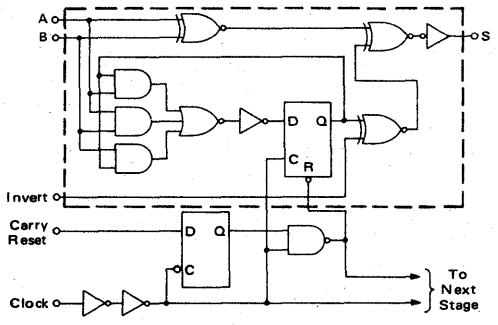
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM

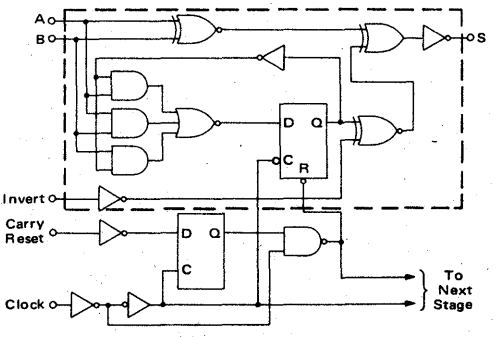


LOGIC DIAGRAMS
(ONE SECTION AND COMMON INPUTS SHOWN)

MC14032B



MC14038B



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.96 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.93 μA/kHz) f + I_{DD}							
		15	I_T = (2.8 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

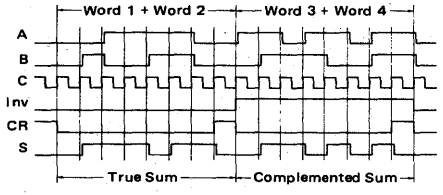
Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time	t_{PLH},							ns
A,B or Invert to Sum	t_{PHL}							
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 195 ns		5.0	–	–	280	1100	1400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns		10	–	–	120	250	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	–	90	190	230	
Clock to Sum								ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	–	500	2200	2400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	–	180	500	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 110 ns		15	–	–	135	380	450	
Input Setup Time	t_{setup}	5.0	–	–	-10	10	10	ns
		10	–	–	0	10	10	
		15	–	–	0	10	10	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	4.0	–	–	MHz
		10	3.0	2.5	10	–	–	
		15	6.0	4.0	12	–	–	
Maximum Clock Rise and Fall Times	t_r,t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	

*The formula given is for the typical characteristics only.

5

TIMING DIAGRAMS

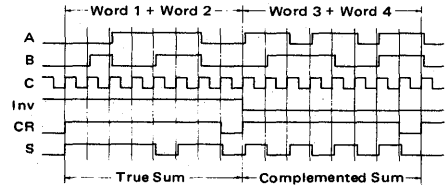
MC14032B



Word 1: 0.0111100 = +60
Word 2: 0.0110010 = +50
0.1101110 = +110

Word 3: 1.1011011 = -37
Word 4: 1.1001110 = -50
1.0101001 = -87

MC14038B



Word 1: 1.1000011 = -61
Word 2: 1.1001101 = -51
1.0010000 = -112

Word 3: 0.0100100 = +36
Word 4: 0.0110001 = +49
0.1010101 = +85

Note: Unused input pins must be connected to either V_{DD} or V_{SS}.

FIGURE 1 – TYPICAL OUTPUT SOURCE TEST CIRCUIT

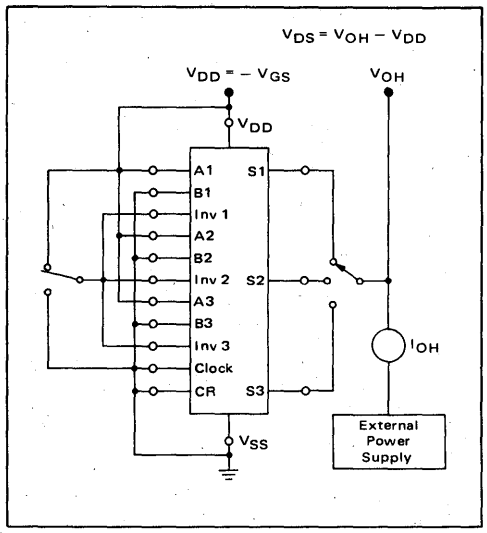


FIGURE 2 – TYPICAL OUTPUT SINK TEST CIRCUIT

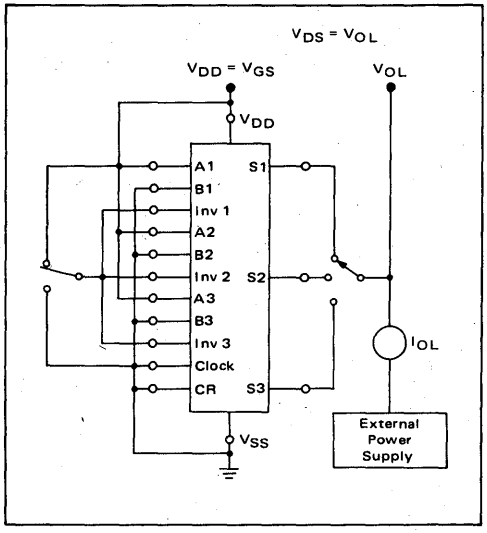


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

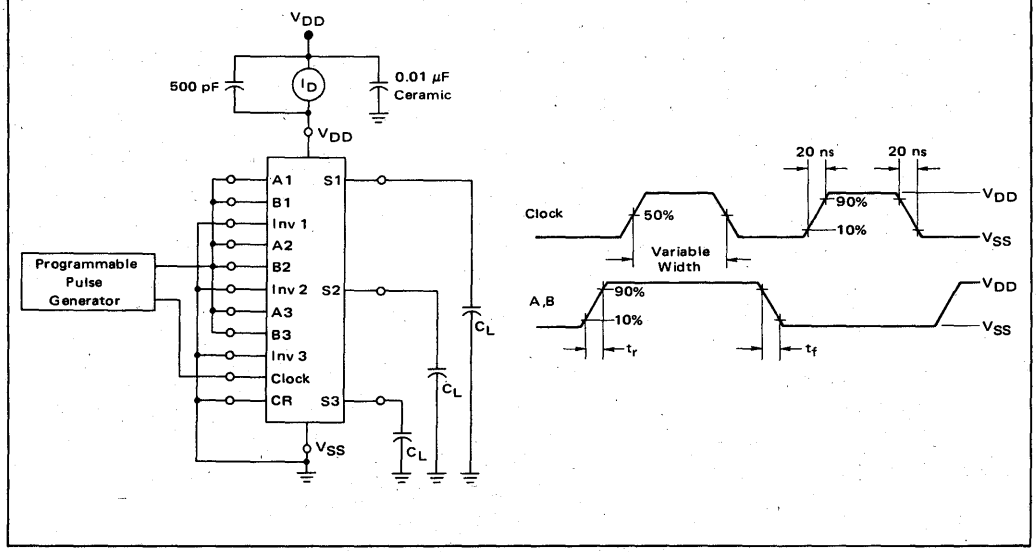


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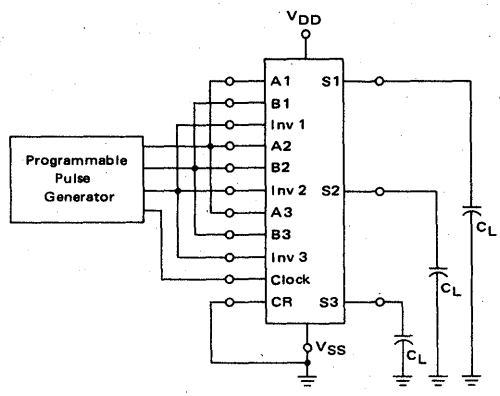
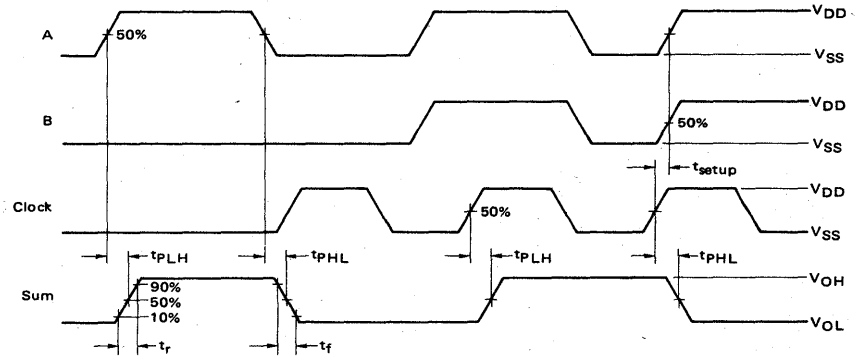
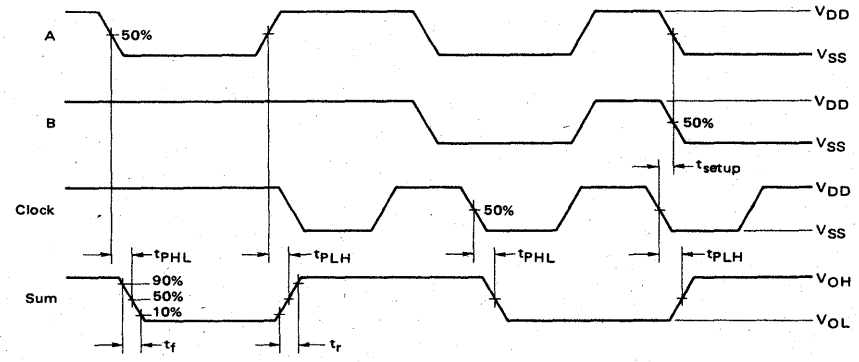
FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14032B



MC14038B



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14034B

McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

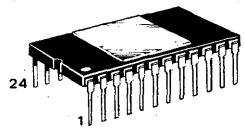
8-BIT UNIVERSAL BUS REGISTER

8-BIT UNIVERSAL BUS REGISTER

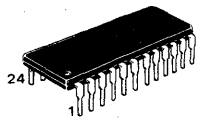
The MC14034B is a bidirectional 8-bit static parallel/serial, input/output bus register. The device contains two sets of input/output lines which allows the bidirectional transfer of data between two buses; the conversion of serial data to parallel form, or the conversion of parallel data to serial form. Additionally the serial data input allows data to be entered shift/right, while shift/left can be accompolished by hard-wiring each parallel output to the previous parallel bit input.

Other useful applications for this device include pseudo-random code generation, sample and hold register, frequency and phase-comparator, address or buffer register, and serial/parallel input/output conversions.

- Bidirectional Parallel Data Input
- Quiescent Current = 10 nA/package typical @ 5 Vdc
- Noise Immunity = 45 % of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Static Operation 0 to 5.0 MHz @ V_{DD} = 10 Vdc
- Single Supply Operation = Positive or Negative
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4034



L SUFFIX
CERAMIC PACKAGE
CASE 716



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

5

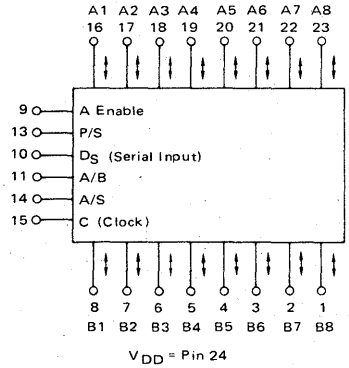
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	μAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (2.2 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (4.4 μA/kHz) f + I_{DD}							
		15	I_T = (6.6 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time A or B	t_r							ns
t_r = (3.0 ns/pF) C_L +30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L +15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L +10 ns		15	–	–	65	110	160	
Output Fall Time A or B	t_f							ns
t_f = (1.5 ns/pF) C_L +25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L +12.5 ns		10	–	–	50	75	110	
t_f = (0.55 ns/pF) C_L +9.5 ns		15	–	–	37	55	80	
Propagation Delay Time A (B) Synchronous Parallel Data Input, B (A) Parallel Data Output	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 440 ns		5.0	–	–	525	940	1300	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 172 ns		10	–	–	205	350	515	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 120 ns		15	–	–	145	270	360	
Propagation Delay Time A(B) Asynchronous Parallel Data Input B (A) Parallel Data Output	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 420 ns		5.0	–	–	505	900	1350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	–	180	300	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	–	–	130	225	340	
Minimum Clock Pulse Width	PW_C	5.0	–	–	170	340	500	
		10	–	–	70	140	200	
		15	–	–	55	100	150	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	2.5	–	–	MHz
		10	3.0	2.5	6.0	–	–	
		15	4.0	3.0	8.0	–	–	
Maximum Clock Pulse Rise and Fall Times	t_r,t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
A, B Input Setup Time	t_{setup}	5.0	–	–	35	70	100	ns
		10	–	–	15	30	45	
		15	–	–	12	25	35	
Minimum High Level AE, P/S, A/S Pulse Width	P_W	5.0	–	–	200	400	600	ns
		10	–	–	90	180	270	
		15	–	–	80	140	200	

*The formula given is for the typical characteristics only.

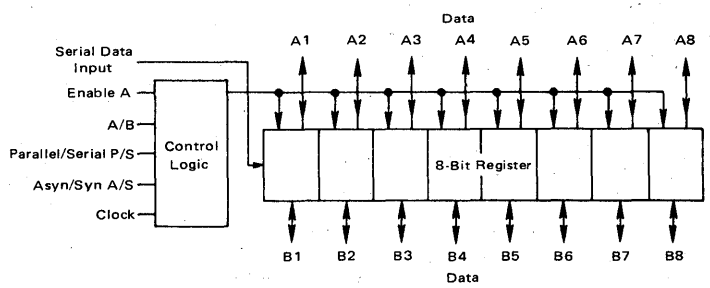
TRUTH TABLE

"A" Enable	P/S	A/B	A/S	MODE	OPERATION†
0	0	0	X	Serial	Synchronous Serial data input, A and B parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, synchronous data recirculation.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, asynchronous data recirculation.
1	0	0	X	Serial	Synchronous serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous serial data input, B-Parallel data output.
1	1	0	0	Parallel	B-Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B-Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A-Synchronous Parallel data input, B-Parallel data output.
1	1	1	1	Parallel	A-Asynchronous Parallel data input, B-Parallel data output.

X = Don't Care

†Outputs change at positive transition of clock in the serial mode and when the A/S input is low in the parallel mode. During transfer from parallel to serial operation, A/S should remain low in order to prevent D_S transfer into flip-flops.

EXPANDED BLOCK DIAGRAM



OPERATING CHARACTERISTICS

The MC14034B is composed of eight register cells connected in cascade with additional control logic. Each register cell is composed of one "D" master-slave flip-flop with separate internal clocks, and two data transfer gates allowing the data to be transferred bidirectionally from bus A to bus B and from bus B to bus A, and to be memorized. Besides the single phase clock and the serial data inputs, the control logic provides four other features:

A Enable Input – When high, this input enables the bus A data lines.

A/B Input (Data A or B) – This input controls the direction of data flow: when high, the data flows from bus A to bus B; when low, the data flows from bus B to bus A.

P/S Input (Parallel/Serial) – This input controls the data input mode (parallel or serial). When high, the data is transferred to the register in a parallel asynchronous mode or a parallel synchronous mode (positive clock transition). When low, the data is entered into the register in a serial synchronous mode (positive clock transition).

A/S Input (Asynchronous/Synchronous to the Clock) – When this input is high, the data is transferred independently from the clock rate; when low, the clock is enabled and the data is transferred synchronously.

5

LOGIC DIAGRAM

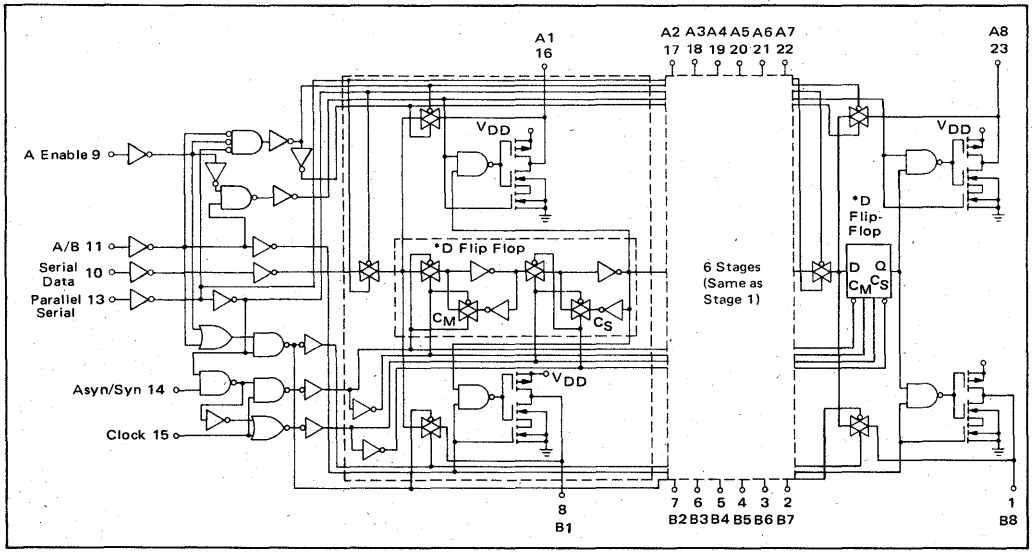
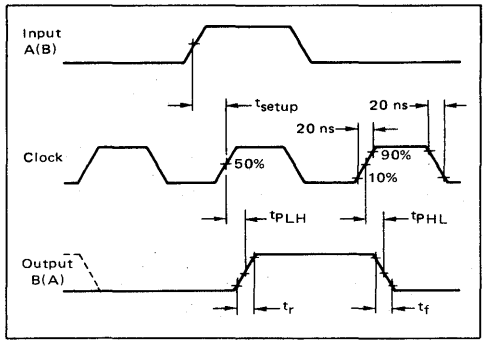


FIGURE 1 – PROPAGATION DELAY AND TRANSITION TIMES WAVEFORMS



PROPAGATION AND TRANSITION TIME TEST CIRCUITS

FIGURE 2 – A SYNCHRONOUS DATA INPUT, B PARALLEL DATA OUTPUT AND SETUP TIME

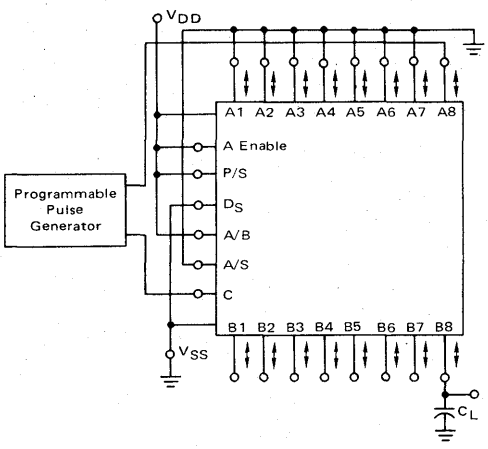


FIGURE 3 – B SYNCHRONOUS DATA INPUT, B PARALLEL DATA OUTPUT AND SETUP TIME

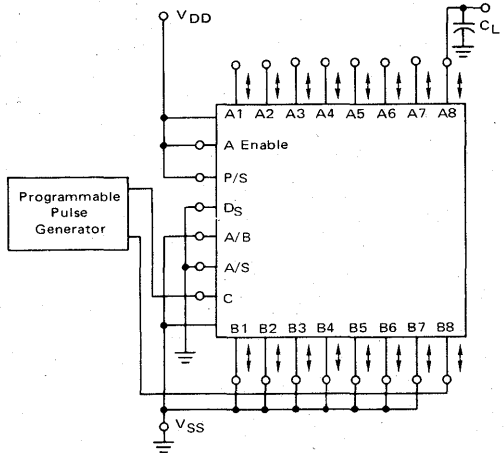


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FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

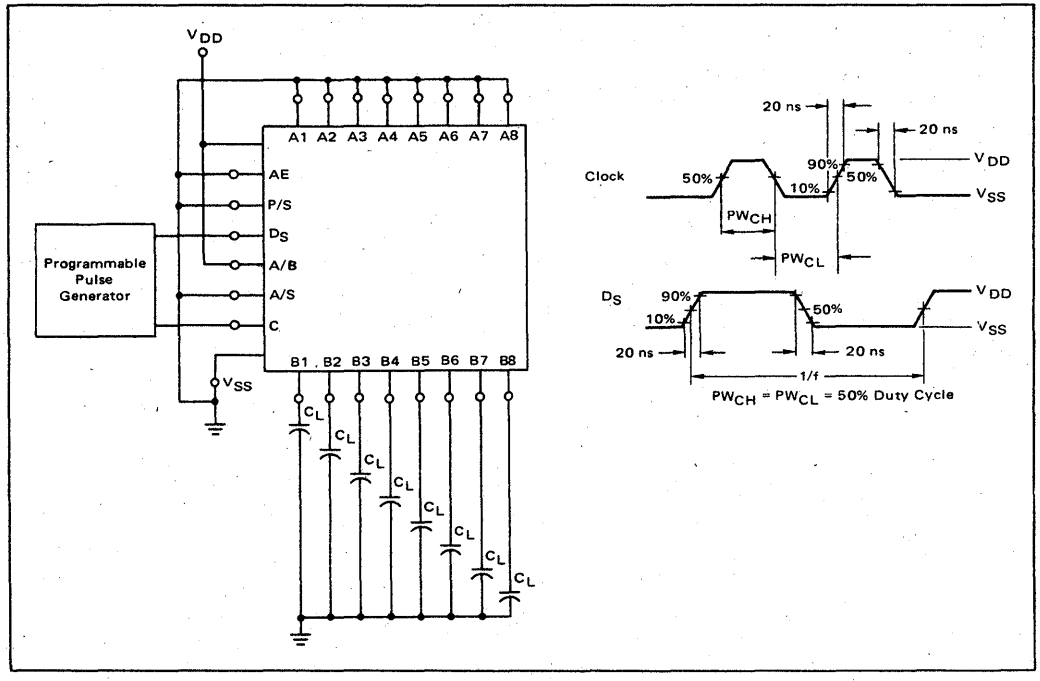


FIGURE 5 – 16-BIT PARALLEL IN/PARALLEL OUT, PARALLEL IN/SERIAL OUT, SERIAL IN/PARALLEL OUT, SERIAL IN/SERIAL OUT REGISTER

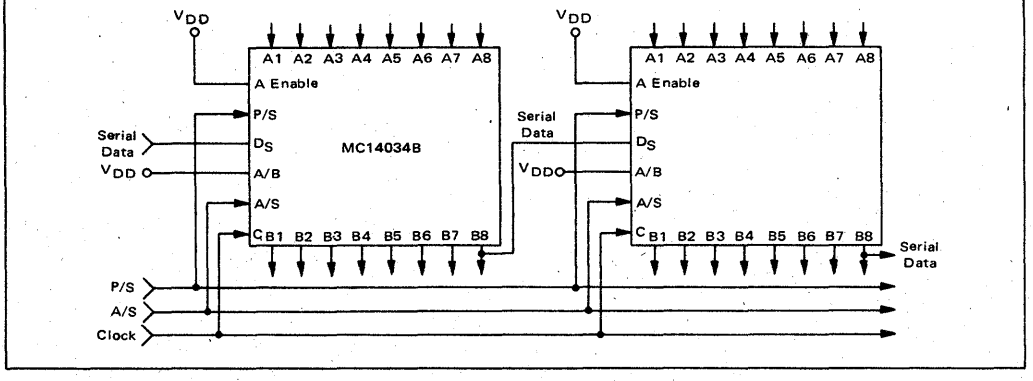
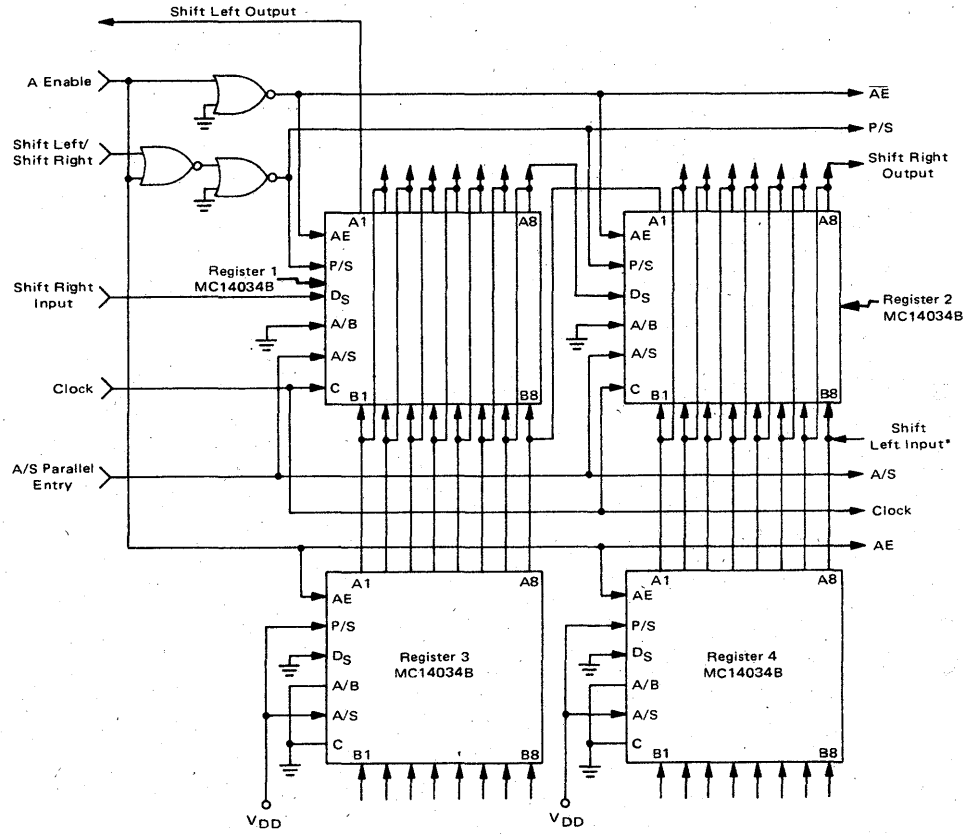


FIGURE 6 – SHIFT RIGHT/SHIFT LEFT WITH PARALLEL INPUTS



A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

*Shift left input must be disabled during parallel entry.

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MC14035B

4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER

The MC14035B 4-bit shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of a 4-stage clocked serial-shift register with synchronous parallel inputs and buffered parallel outputs. The Parallel/Serial (P/S) input allows serial-right shifting of data or synchronous parallel loading via inputs D_{P0} thru D_{P3}. The True/Complement (T/C) input determines whether the outputs display the Q or $\overline{Q}$ outputs of the flip-flop stages. J-K logic forms the serial input to the first stage. With the J and K inputs connected together they operate as a serial "D" input.

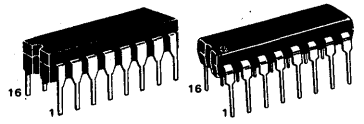
This device may be effectively used for shift-right/shift-left registers, parallel-to-serial/serial-to-parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo-random code generation, frequency and phase comparators, sample and hold registers, etc. . .

- 4-Stage Clocked Serial-Shift Operation
- Synchronous Parallel Loading of all Four Stages
- J-K Serial Inputs on First Stage
- Asynchronous True/Complement Control of all Outputs
- Fully Static Operation
- Asynchronous Master Reset
- Data Transfer Occurs on the Positive-Going Clock Transition
- No Limit on Clock Rise and Fall Times
- All Inputs are Buffered
- 6.0 MHz Operation @ V_{DD} = 10 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT
PARALLEL-IN/PARALLEL-OUT
SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

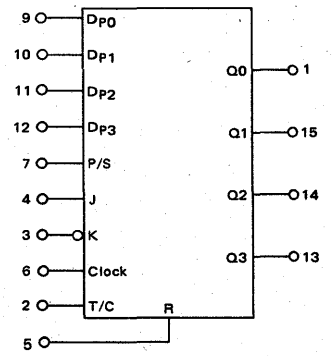
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS				t_n OUTPUT
C	J	$\overline{K}$	R	Q0
⎍	0	0	0	0
⎍	0	1	0	Q0 (n - 1)
⎍	1	0	0	$\overline{Q0}$ (n - 1)
⎍	1	1	0	1
⎎	x	x	0	Q0 (n-1)
x	x	x	1	0

x = Don't Care
P/S = 0 = Serial Mode
T/C = 1 = True Outputs

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.0 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.0 µA/kHz) f + I_{DD}							
		15	I_T = (3.0 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

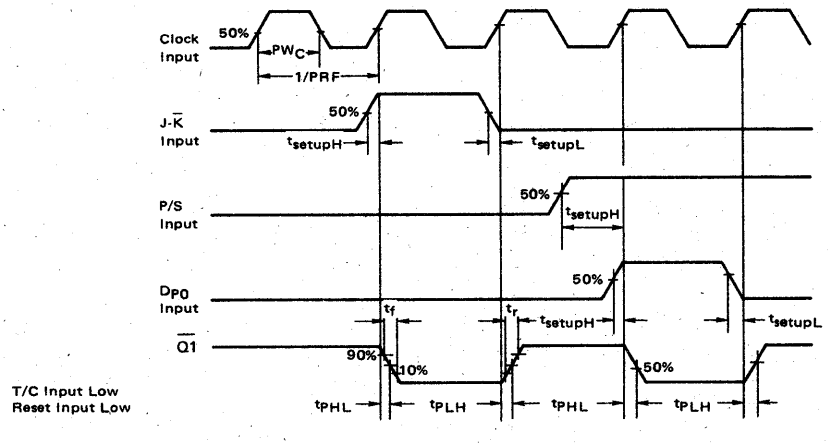
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

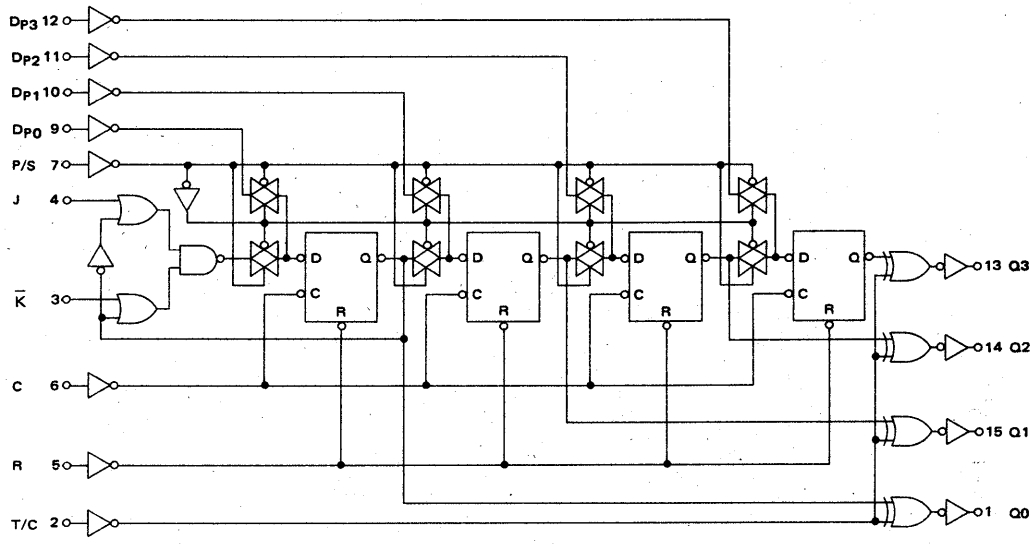
Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	37	55	80	
Propagation Delay Time, Clock or Reset to Q	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 223 ns		5.0	–	–	300	500	750	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 89 ns		10	–	–	130	200	325	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 67 ns		15	–	–	95	150	240	
Minimum Clock Pulse Width	PW_C	5.0	–	–	135	335	500	ns
		10	–	–	45	165	250	
		15	–	–	40	125	190	
Minimum Reset Pulse Width	PW_R	5.0	–	–	80	400	500	ns
		10	–	–	40	175	200	
		15	–	–	35	130	150	
Maximum Clock Pulse Rise and Fall Time	t_r,t_f	5.0	–	–	–	No	No	–
		10	–	–	–	Limit	Limit	
		15	–	–	–			
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	2.5	–	–	MHz
		10	3.0	2.0	6.0	–	–	
		15	5.0	3.0	10	–	–	
J-$\overline{K}$ Setup Time	t_{setup}	5.0	–	–	120	500	750	ns
		10	–	–	50	200	250	
		15	–	–	30	150	190	
P/S Control Setup Time	t_{setup}	5.0	–	–	25	500	750	ns
		10	–	–	10	200	250	
		15	–	–	7.5	150	190	
Parallel Input Setup Time	t_{setup}	5.0	–	–	90	500	750	ns
		10	–	–	20	200	250	
		15	–	–	15	150	190	

*The formula given is for the typical characteristics only.

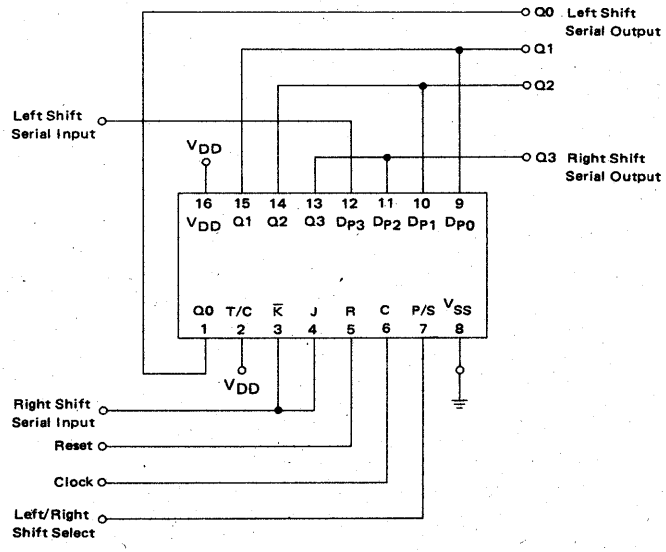
FIGURE 1 – TIMING DIAGRAM



LOGIC DIAGRAM



APPLICATION DIAGRAM
Shift Left/Shift Right Register



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MOTOROLA Semiconductors
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MC14038B

FOR COMPLETE DATA
SEE MC14032B

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

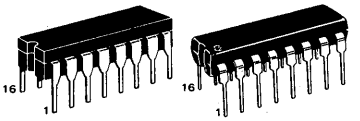
TRIPLE SERIAL ADDERS

Positive Logic — MC14032B
Negative Logic — MC14038B

TRIPLE SERIAL ADDERS

The MC14032B and MC14038B triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032B, and on the negative-going clock transition for the MC14038B. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers.

- Static Operation from dc to 5.0 MHz
- Buffered Outputs
- Single-Phase Clocking
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4032 and CD4038



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

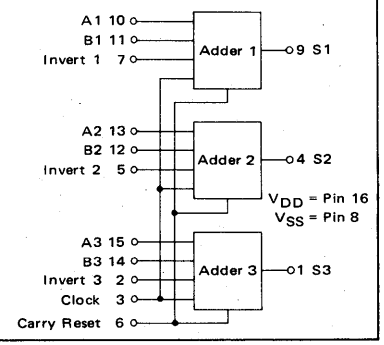
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

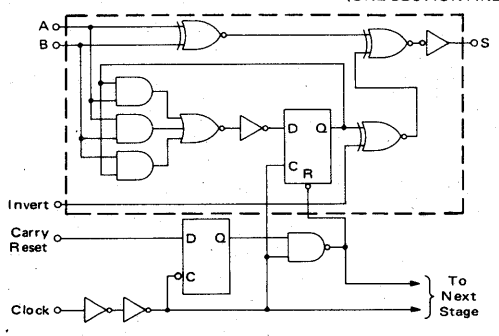
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM

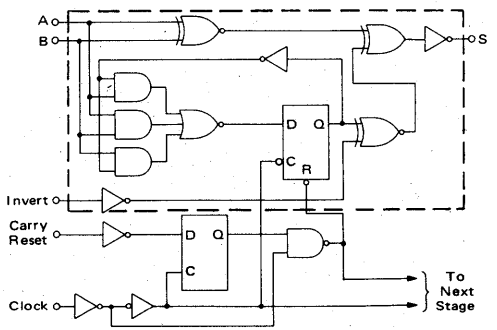


LOGIC DIAGRAMS
(ONE SECTION AND COMMON INPUTS SHOWN)

MC14032B



MC14038B



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MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14040B

12-BIT BINARY COUNTER

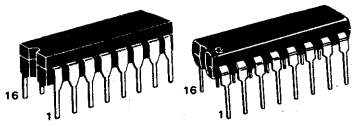
The MC14040B 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Common Reset Line
- 13 MHz Typical Counting Rate @ V_{DD} = 15 V
- Pin-for-Pin Replacement for CD4040

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

12-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

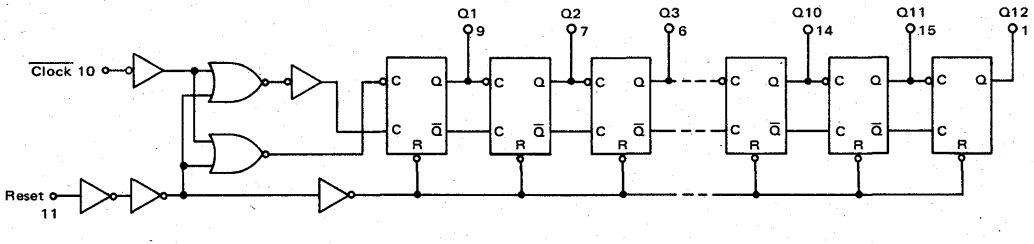
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
⌐	0	No Change
¬	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



Q4 = Pin 5 Q7 = Pin 4
Q5 = Pin 3 Q8 = Pin 13
Q6 = Pin 2 Q9 = Pin 12

V_{DD} = Pin 16
V_{SS} = Pin 8

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.42 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.85 µA/kHz) f + I_{DD}							
		15	I_T = (1.43 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time	t_{PLH},							ns
$\overline{\text{Clock}}$ to Q1	t_{PHL}							
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L +315 ns		5.0	–	–	400	700	1050	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L +137 ns		10	–	–	170	280	420	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L +95 ns		15	–	–	120	210	320	
$\overline{\text{Clock}}$ to Q12								μs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L +2415 ns		5.0	–	–	2.5	5.0	7.5	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L +867 ns		10	–	–	0.9	1.8	2.7	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L +475 ns		15	–	–	0.5	1.4	2.1	
Propagation Delay Time	t_{PHL}							ns
Reset to Q_n								
t_{PHL} = (1.7 ns/pF) C_L +485 ns		5.0	–	–	570	1080	1620	
t_{PHL} = (0.66 ns/pF) C_L +182 ns		10	–	–	215	400	600	
t_{PHL} = (0.5 ns/pF) C_L +145 ns		15	–	–	170	300	450	
Minimum Clock Pulse Width	PW_C	5.0	–	–	140	250	385	ns
		10	–	–	55	100	150	
		15	–	–	38	75	115	
Maximum Clock Pulse Frequency	PRF	5.0	2.0	1.5	3.5	–	–	MHz
		10	5.0	3.5	9.0	–	–	
		15	6.5	4.5	13	–	–	
Maximum Clock Rise and Fall Time	t_r,t_f	5.0	No	No	–	–	–	–
		10	Limit	Limit	–	–	–	
		15			–	–	–	
Minimum Reset Pulse Width	PW_R	5.0	–	–	320	640	960	ns
		10	–	–	120	240	360	
		15	–	–	80	180	270	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

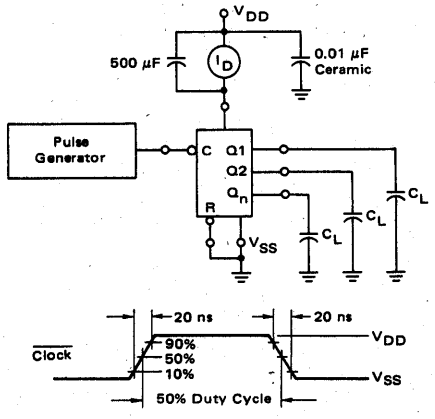


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

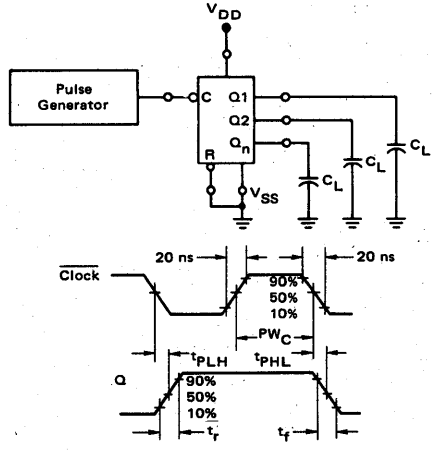
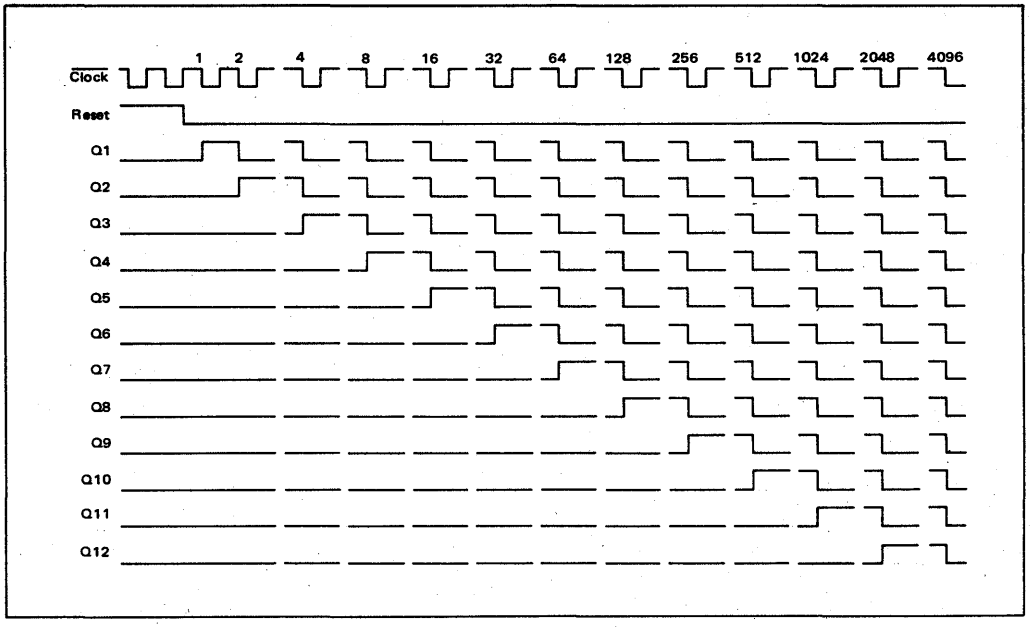


FIGURE 3 – TIMING DIAGRAM

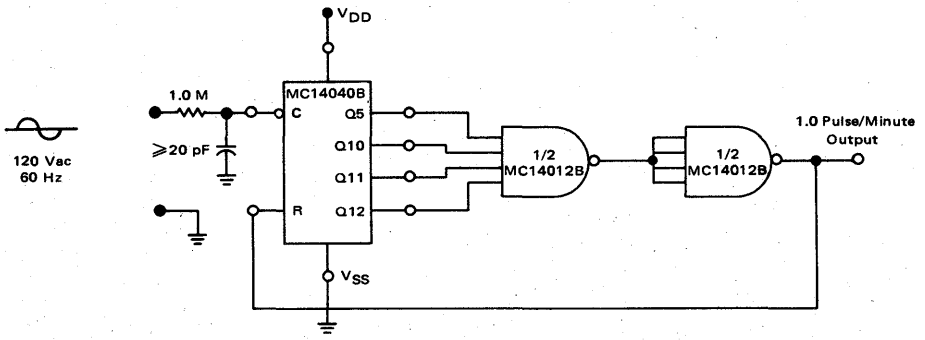


5

APPLICATIONS INFORMATION

TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14040B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



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Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14042B

QUAD LATCH

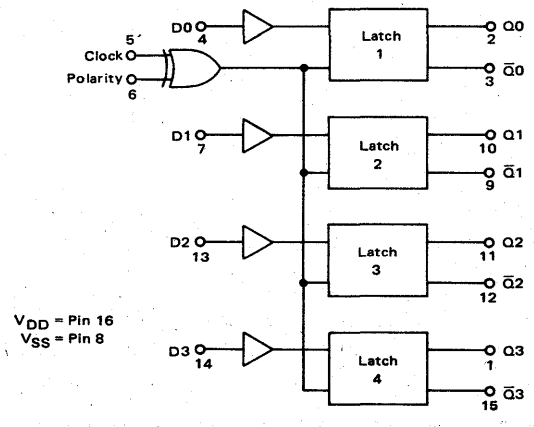
The MC14042B quad latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has a separate data input, but all four latches share a common clock. The clock polarity (high or low) used to strobe date through the latches can be reversed using the polarity input. Information present at the data input is transferred to ourputs Q and Q during the clock level which is determined by the polarity input. When the polarity input is in the logic "0" state, data is transferred during the low clock level, and when the polarity input is in the logic "1" state the transfer occurs during the high clock level.

- Buffered Data Inputs
- Common Clock
- Positive or Negative Edge Clocked
- Q and Q Outputs
- Double Diode Input Protection
- No Limit on Clock Rise or Fall Times
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

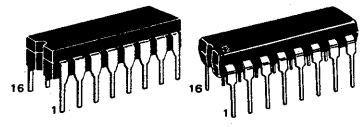
LOGIC DIAGRAM



McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD LATCH



L SUFFIX
CERAMIC PACKAGE
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PLASTIC PACKAGE
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ORDERING INFORMATION

MC14XXXB — Suffix Denotes
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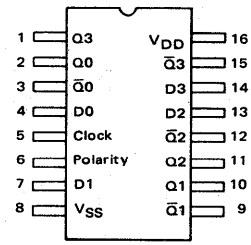
PIN ASSIGNMENT



TRUTH TABLE

CLOCK	POLARITY	Q
0	0	Data
⌐	0	Latch
1	1	Data
⌙	1	Latch

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# D Inputs "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Input Voltage C,P Inputs "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.75	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.25	–	11.25	8.25	–	11.25	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4/	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.0\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (2.0\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (3.0\ \mu A/kHz)\ f + I_{DD}$							

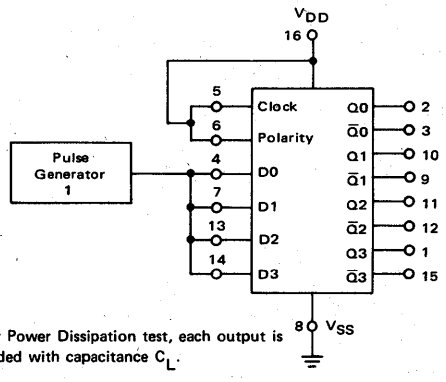
*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types		Unit
			Typical	Maximum	
Output Rise Time	t_r				ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	360	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	130	
Output Fall Time	t_f				ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	40	80	
Propagation Delay Time, D to Q, $\overline{Q}$	t_{PLH}, t_{PHL}				ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns		5.0	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	90	180	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	60	120	
Propagation Delay Time, Clock to Q, $\overline{Q}$	t_{PLH}, t_{PHL}				ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns		5.0	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	90	180	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		25	60	120	
Minimum Clock Pulse Width	PW_C				ns
		5.0	150	300	
		10	50	100	
		15	40	80	
Maximum Clock Rise Time	t_r				—
		5.0	No Limit		
		10			
		15			
Hold Time	t_{hold}				ns
		5.0	50	100	
		10	25	50	
		15	20	40	
Setup Time	t_{setup}				ns
		5.0	0	50	
		10	0	30	
		15	0	25	

*The formula given is for the typical characteristics only.

FIGURE 1 – AC AND POWER DISSIPATION TEST CIRCUIT AND TIMING DIAGRAM
(Data to Output)



For Power Dissipation test, each output is loaded with capacitance C_L.

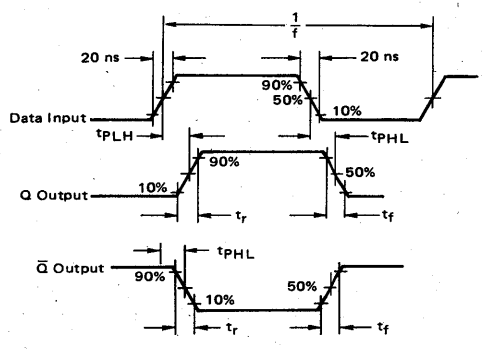
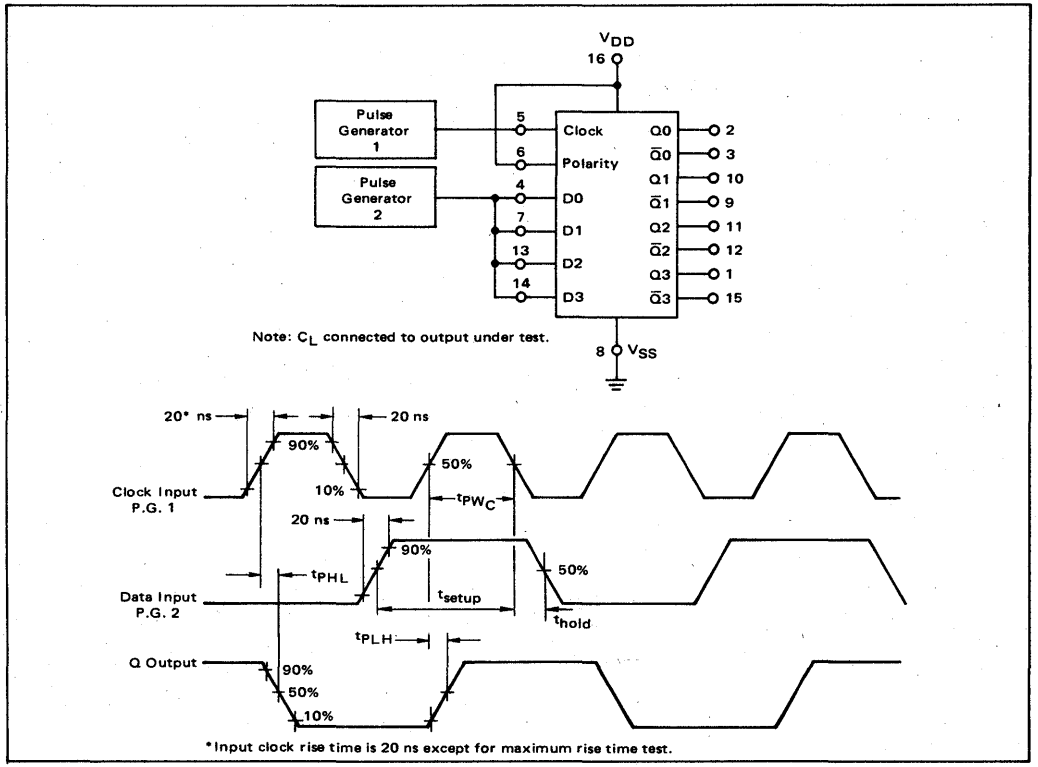


FIGURE 2 – AC TEST CIRCUIT AND TIMING DIAGRAM
(Clock to Output)



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This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

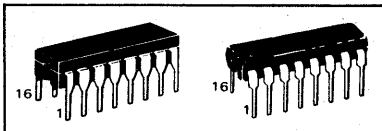
MC14043B
QUAD "NOR" R-S LATCH

MC14044B
QUAD "NAND" R-S LATCH

McMOS MSI
QUAD R-S LATCHES

The MC14043B and MC14044B quad R-S latches are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three-state buffers having a common enable input. The outputs are enabled with a logical "1" or high on the enable input; a logical "0" or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

- Quiescent Current = 4.0 nA/pkg typical @ 10 Vdc
- Double Diode Input Protection
- Three-State Outputs with Common Enable
- Outputs Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load, or Two HTL Loads Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc



L SUFFIX
CERAMIC PACKAGE
CASE 620

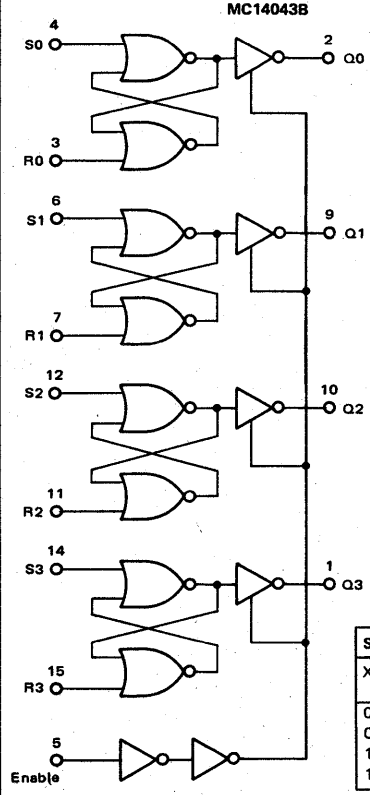
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MC14043B



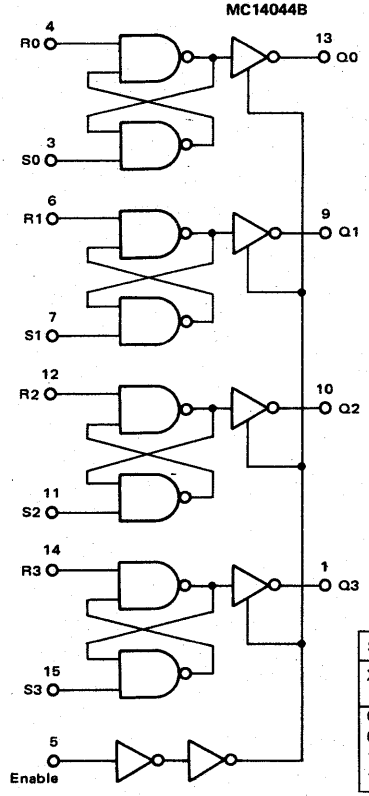
V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	No Change
0	1	1	0
1	0	1	1
1	1	1	1

X = Don't Care

MC14044B



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	No Change

X = Don't Care

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all outputs switching)	I_T	5.0	$I_T = (0.58\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (1.15\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (1.73\ \mu A/kHz)\ f + I_{DD}$							
Three-State Output Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	μAdc
Three-State Output Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.0001	±1.0	–	±7.5	μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

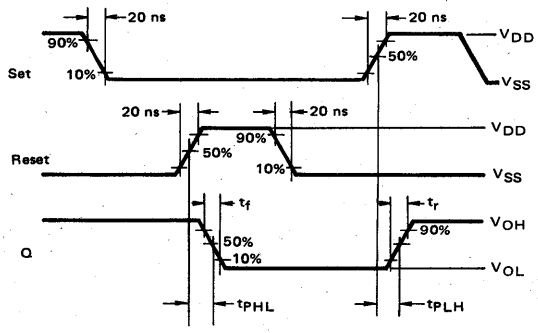
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Typ	Max	Unit
Output Rise Time	t_r				ns
t_r = (1.35 ns/pF) C_L + 32.5 ns		5.0	100	200	
t_r = (0.60 ns/pF) C_L + 20 ns		10	50	100	
t_r = (0.40 ns/pF) C_L + 20 ns		15	40	80	
Output Fall Time	t_f				ns
t_f = (1.35 ns/pF) C_L + 32.5 ns		5.0	100	200	
t_f = (0.60 ns/pF) C_L + 20 ns		10	50	100	
t_f = (0.40 ns/pF) C_L + 20 ns		15	40	80	
Propagation Delay Time	t_{PLH}				ns
t_{PLH} = (0.90 ns/pF) C_L + 130 ns		5.0	175	350	
t_{PLH} = (0.36 ns/pF) C_L + 57 ns		10	75	175	
t_{PLH} = (0.26 ns/pF) C_L + 47 ns		15	60	120	
t_{PHL} = (0.90 ns/pF) C_L + 130 ns	t_{PHL}	5.0	175	350	ns
t_{PHL} = (0.36 ns/pF) C_L + 57 ns		10	75	175	
t_{PHL} = (0.26 ns/pF) C_L + 47 ns		15	60	120	
Minimum Set Pulse Width	PW_S	5.0	80	200	ns
		10	40	100	
		15	30	70	
Minimum Reset Pulse Width	PW_R	5.0	80	200	ns
		10	40	100	
		15	30	70	
Three-State Enable/Disable Delay	t_{En}, t_{Dis}	5.0	150	300	ns
		10	80	160	
		15	55	110	

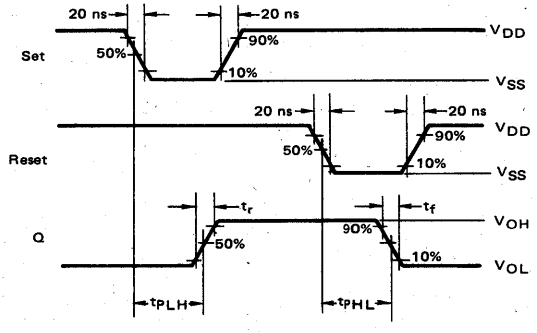
*The formulas given are for the typical characteristics only.

AC WAVEFORMS

MC14043B



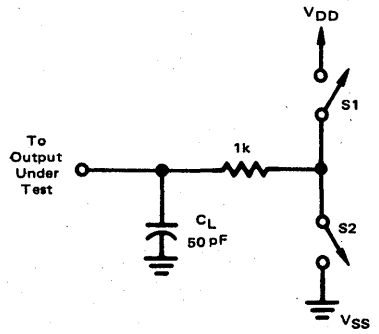
MC14044B

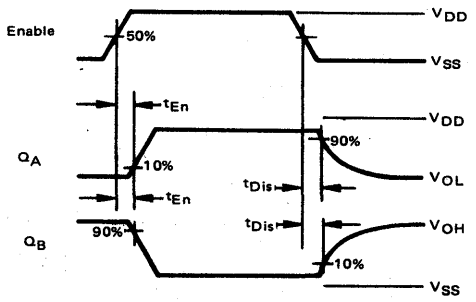


THREE-STATE ENABLE/DISABLE DELAYS

Set, Reset, and Switch Conditions for 3-State Tests.

TEST	S	R	MC14043B			MC14044B		
			S1	S2	Q	S1	S2	Q
t_{En}	V_{DD}	V_{SS}	Open	Closed	A	Closed	Open	B
t_{En}	V_{SS}	V_{DD}	Closed	Open	B	Open	Closed	A
t_{Dis}	V_{DD}	V_{SS}	Open	Closed	A	Closed	Open	B
t_{Dis}	V_{SS}	V_{DD}	Closed	Open	B	Open	Closed	A





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MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14046B

PHASE-LOCKED LOOP

The MC14046B phase-locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs. PCA_{in} and PCB_{in}. Input PCA_{in} can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal $PC1_{out}$, and maintains 90^{o} phase shift at the center frequency between PCA_{in} and PCB_{in} signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals $PC2_{out}$ and PCP_{out}, and maintains a 0^{o} phase shift between PCA_{in} and PCB_{in} signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins $C1_A$, $C1_B$, R1, and R2. The source-follower output SF_{out} with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

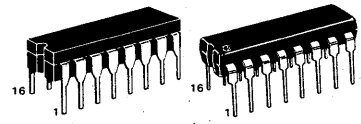
Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

- VCO Frequency = 1.4 MHz Typical @ V_{DD} = 10 Vdc
- VCO Frequency Drift with Temperature = 0.04%/°C Typical @ V_{DD} = 10 Vdc
- VCO Linearity = 1% Typical
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Dynamic Power Dissipation — 70 μW Typical @ f_0 = 10 kHz, V_{DD} = 5.0 Vdc, R1 = 1.0 MΩ, R2 = ∞, R_{SF} = ∞
- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 Vdc
- Pin-for-Pin Replacement for CD4046

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PHASE-LOCKED LOOP



L SUFFIX
CERAMIC PACKAGE
CASE 620

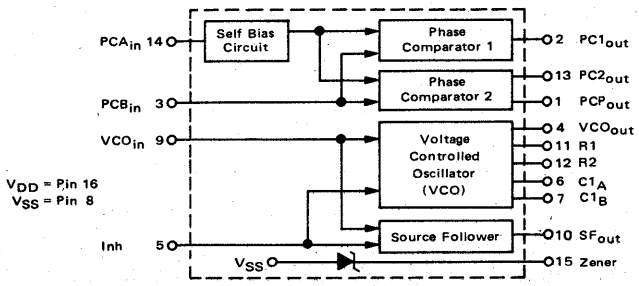
P SUFFIX
PLASTIC PACKAGE
CASE 648

5

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Pins 6, 7, 10, 11, 12, and 15 if unused must be left open.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package) (Inh = "1" and PCA = "1")	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package) (Inh = "1" and PCA = "1")	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current † (Inh = "0", f_o = 10 kHz, C_L = 50 pF, R1 = 1 MΩ, R2 = ∞, R_{SF} = ∞, and 50% Duty Cycle)	I_T	5.0	I_T = (1.46 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.91 µA/kHz) f + I_{DD}							
		15	I_T = (4.37 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To Calculate Total Current in General:

$$I_T \approx 2.2 \times V_{DD} \left(\frac{VCO_{in} - 1.65}{R1} + \frac{V_{DD} - 1.35}{R2}\right)^{3/4} + 1.6 \times \left(\frac{VCO_{in} - 1.65}{R_{SF}}\right)^{3/4} + 1 \times 10^{-3} (C_L + 9) V_{DD} f +$$
$$1 \times 10^{-1} V_{DD}^2 \left(\frac{100 - \%\ \text{Duty Cycle of PCA}_{in}}{100}\right) + I_Q$$

where: I_T in µA, C_L in pF, VCO_{in}, V_{DD} in Vdc, f in KHz, and R1, R2, R_{SF} in MΩ, C_L on VCO_{out}.

ELECTRICAL CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

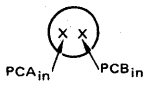
Characteristic	Symbol	V_{DD} Vdc	Minimum AL Device	Minimum CL/CP Device	Typical All Types	Maximum AL Device	Maximum CL/CP Device	Units
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
PHASE COMPARATORS 1 and 2								
Input Resistance – PCA_{in}	R_{in}	5.0	1.0	1.0	2.0	–	–	MΩ
		10	0.2	0.2	0.4	–	–	
		15	0.1	0.1	0.2	–	–	
– PCB_{in}	R_{in}	15	150	15	1500	–	–	MΩ
Minimum Input Sensitivity	V_{in}	5.0	–	–	200	300	400	mV p-p
AC Coupled – PCA_{in}		10	–	–	400	600	800	
C series = 1000 pF, f = 50 kHz		15	–	–	700	1050	1400	
DC Coupled – PCA_{in}, PCB_{in}	–	5 to 15	See Noise Immunity					
VOLTAGE CONTROLLED OSCILLATOR (VCO)								
Maximum Frequency	f_{max}	5.0	0.50	0.35	0.70	–	–	MHz
(VCO_{in} = V_{DD}, C1 = 50 pF,		10	1.0	0.7	1.4	–	–	
R1 = 5 kΩ, and R2 = ∞)		15	1.4	1.0	1.9	–	–	
Temperature – Frequency Stability	–	5.0	–	–	0.12	–	–	%/°C
(R2 = ∞)		10	–	–	0.04	–	–	
		15	–	–	0.015	–	–	
Linearity (R2 = ∞)	–							%
(VCO_{in} = 2.50 V ± 0.30 V, R1 ⩾ 10 kΩ)		5.0	–	–	1	–	–	
(VCO_{in} = 5.00 V ± 2.50 V, R1 ⩾ 400 kΩ)		10	–	–	1	–	–	
(VCO_{in} = 7.50 V ± 5.00 V, R1 ⩾ 1000 kΩ)		15	–	–	1	–	–	
Output Duty Cycle	–	5 to 15	–	–	50	–	–	%
Input Resistance – VCO_{in}	R_{in}	15	150	15	1500	–	–	MΩ
SOURCE-FOLLOWER								
Offset Voltage	–	5.0	–	–	1.65	2.2	2.5	Vdc
(VCO_{in} minus SF_{out}, R_{SF} > 50 kΩ)		10	–	–	1.65	2.2	2.5	
		15	–	–	1.65	2.2	2.5	
Linearity	–							%
(VCO_{in} = 2.50 V ± 0.30 V, R_{SF} > 50 kΩ)		5.0	–	–	0.1	–	–	
(VCO_{in} = 5.00 V ± 2.50 V, R_{SF} > 50 kΩ)		10	–	–	0.6	–	–	
(VCO_{in} = 7.50 V ± 5.00 V, R_{SF} > 50 kΩ)		15	–	–	0.8	–	–	
ZENER DIODE								
Zener Voltage (I_Z = 50 μA)	V_Z	–	6.7	6.3	7.0	7.3	7.7	Vdc
Dynamic Resistance (I_Z = 1 mA)	R_Z	–	–	–	100	–	–	Ω

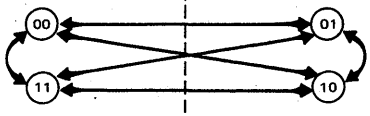
*The formula given is for the typical characteristics only.

FIGURE 1 – PHASE COMPARATORS STATE DIAGRAMS

PHASE COMPARATOR 1

Input State

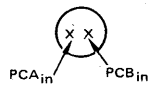


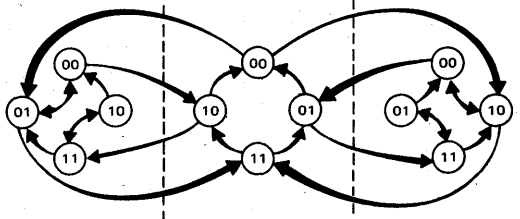


PC1$_{out}$	0	1

PHASE COMPARATOR 2

Input State





PC2$_{out}$	0	3-State Output Disconnected	1
PCP$_{out}$ (Lock Indicator)	0	1	0

Refer to Waveforms in Figure 3.

5

FIGURE 2 – DESIGN INFORMATION

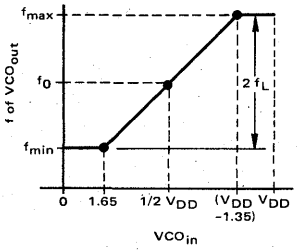
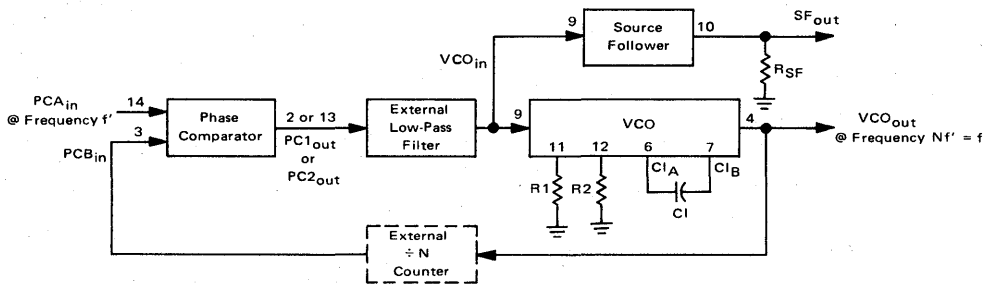
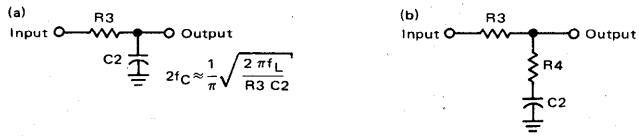
Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA$_{in}$.	VCO in PLL system adjusts to center frequency (f_0).	VCO in PLL system adjusts to minimum frequency (f_{min}).
Phase angle between PCA$_{in}$ and PCB$_{in}$.	90° at center frequency (f_0), approaching 0° and 180° at ends of lock range ($2f_L$).	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range ($2f_L$).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock. $2f_L$ = full VCO frequency range = $f_{max} - f_{min}$.	
Capture frequency range ($2f_C$).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low-pass filter characteristics (see Figure 3). $f_C \leq f_L$	$f_C = f_L$
Center frequency (f_0).	The frequency of VCO$_{out}$, when VCO$_{in}$ = 1/2 V_{DD}	
VCO output frequency (f). Note: This information is intended only to be a design guide. Some laboratory experimentation may be required for fixed designs.	$f \approx \frac{K\left[\frac{VCO_{in} - 1.65}{R1} + \frac{V_{DD} - 1.35}{R2}\right]}{(C1 + 32)(V_{DD} + 1.6)}$ MHz (at 25°C) where: V_{DD} in Vdc; 5.0 Vdc ≤ V_{DD} ≤ 15 Vdc VCO$_{in}$ in Vdc; 1.65 Vdc ≤ VCO$_{in}$ ≤ (V_{DD} -1.35 Vdc) R1 and R2 in MΩ; R1 ≥ 0.005 MΩ, R2 ≤ 10 MΩ C1 in pF; C1 ≥ 50 pF K = 0.95 @ V_{DD} = 5.0 Vdc = 0.95 @ V_{DD} = 10 Vdc = 1.08 @ V_{DD} = 15 Vdc	

FIGURE 3 – GENERAL PHASE-LOCKED LOOP CONNECTIONS AND WAVEFORMS

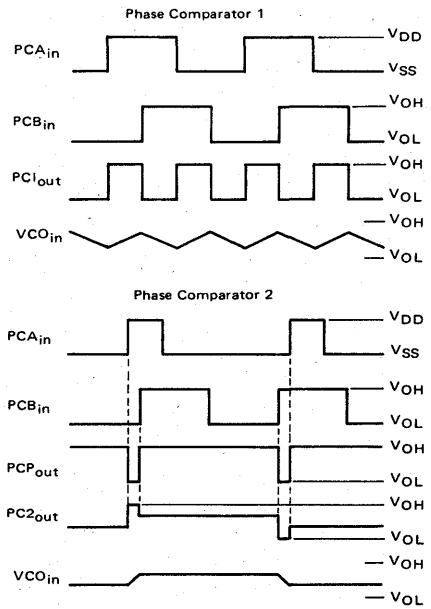


Typical Low-Pass Filters



Note: for further information, see:
(1) F. Gardner, "Phase-Lock Techniques", John Wiley and Son, New York, 1966.
(2) G. S. Moschytz, "Miniature RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

Waveforms



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MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14049B
MC14050B

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

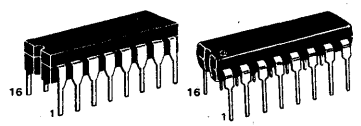
HEX BUFFERS

Inverting – MC14049B
Noninverting – MC14050B

HEX BUFFERS

The MC14049B hex inverter/buffer and MC14050B noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, V_{CC}. The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage for logic-level conversions. Two TTL/DTL Loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (V_{CC} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA). Note that pin 16 is not connected internally on these devices; consequently connections to this terminal will not affect circuit operation.

- High Source and Sink Currents
- High-to-Low Level Converter
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

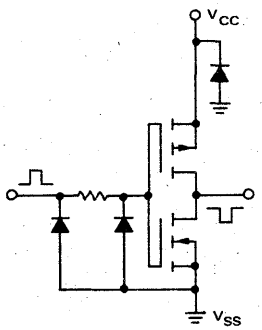
5

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

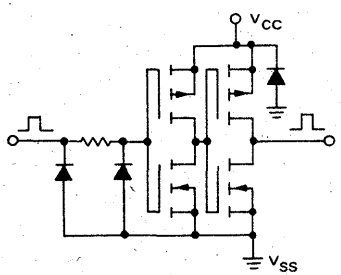
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	45	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)

MC14049B

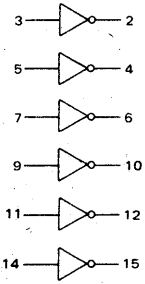


MC14050B



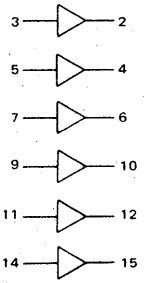
LOGIC DIAGRAMS

MC14049B



NC = Pin 13, 16
V_{SS} = Pin 8
V_{CC} = Pin 1

MC14050B



NC = Pin 13, 16
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V_{CC} = Pin 1

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.4	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	2.9	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.6	
"1" Level	V_{IH}									Vdc
(V_O = 1.4 or 3.6 Vdc)		5.0	3.6	–	3.5	2.75	–	3.5	–	
(V_O = 2.8 or 7.2 Vdc)		10	7.1	–	7.0	5.50	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.4	–	11.25	8.25	–	11.25	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)		5.0	-1.6	–	-1.25	−2.5	–	−0.9	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.25	−2.5	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.7	–	-3.75	−10	–	−2.7	–	
(V_{OL} = 0.4 Vdc)	I_{OL}	5.0	3.75	–	3.2	6.0	–	2.1	–	mAdc
(V_{OL} = 0.5 Vdc)		10	10	–	8.0	16	–	5.6	–	
(V_{OL} = 1.5 Vdc)		15	30	–	24	40	–	16.8	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)		5.0	−1.5	–	−1.25	−2.5	–	−1.0	–	
(V_{OH} = 9.5 Vdc)		10	−1.5	–	−1.25	−2.5	–	−1.0	–	
(V_{OH} = 13.5 Vdc)		15	−4.5	–	−3.75	−10	–	−3.0	–	
(V_{OL} = 0.4 Vdc)	I_{OL}	5.0	3.6	–	3.2	6.0	–	2.5	–	mAdc
(V_{OL} = 0.5 Vdc)		10	9.6	–	8.0	16	–	6.6	–	
(V_{OL} = 1.5 Vdc)		15	28	–	24	40	–	19	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	10	20	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.77 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.54 μA/kHz) f + I_{DD}							
		15	I_T = (5.31 μA/kHz) f + I_{DD}							

*T_{low} = 55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

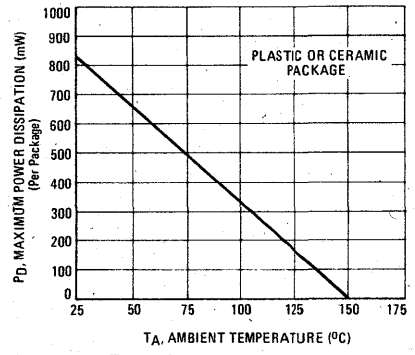
†To Calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per pachage), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

FIGURE 1 – AMBIENT TEMPERATURE POWER DERATING



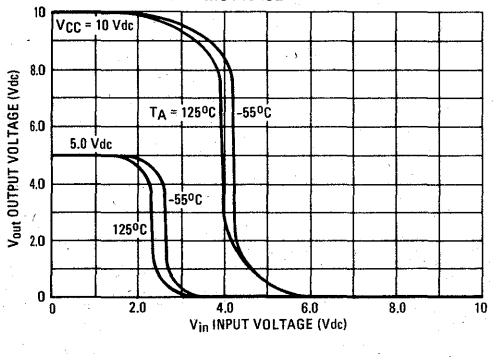
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	All Types Typ	All Types Max	Unit
MC14049B						
Output Rise Time	t_r					ns
t_r = (0.8 ns/pF) C_L + 60 ns		5.0	–	100	200	
t_r = (0.3 ns/pF) C_L + 35 ns		10	–	50	100	
t_r = (0.27 ns/pF) C_L + 26.5 ns		15	–	40	80	
Output Fall Time	t_f					ns
t_f = (0.3 ns/pF) C_L + 25 ns		5.0	–	40	80	
t_f = (0.12 ns/pF) C_L + 14 ns		10	–	20	40	
t_f = (0.1 ns/pF) C_L + 10 ns		15	–	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.38 ns/pF) C_L + 61 ns		5.0	–	80	160	
t_{PLH} = (0.20 ns/pF) C_L + 30 ns		10	–	40	80	
t_{PLH} = (0.11 ns/pF) C_L + 24.5 ns		15	–	30	60	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.38 ns/pF) C_L + 11 ns		5.0	–	30	60	
t_{PHL} = (0.12 ns/pF) C_L + 9 ns		10	–	15	30	
t_{PHL} = (0.11 ns/pF) C_L + 4.5 ns		15	–	10	20	
MC14050B						
Output Rise Time	t_r					ns
t_r = (0.7 ns/pF) C_L + 65 ns		5.0	–	100	200	
t_r = (0.25 ns/pF) C_L + 37.5 ns		10	–	50	100	
t_r = (0.2 ns/pF) C_L + 30 ns		15	–	40	80	
Output Fall Time	t_f					ns
t_f = (0.2 ns/pF) C_L + 30 ns		5.0	–	40	80	
t_f = (0.06 ns/pF) C_L +17 ns		10	–	20	40	
t_f = (0.04 ns/pF) C_L + 13 ns		15	–	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.33 ns/pF) C_L + 63.5 ns		5.0	–	80	160	
t_{PLH} = (0.19 ns/pF) C_L + 30.5 ns		10	–	40	80	
t_{PLH} = (0.06 ns/pF) C_L + 27 ns		15	–	30	60	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.2 ns/pF) C_L + 30 ns		5.0	–	40	80	
t_{PHL} = (0.1 ns/pF) C_L + 15 ns		10	–	20	40	
t_{PHL} = (0.05 ns/pF) C_L + 12.5 ns		15	–	15	30	

*The formula given is for the typical characteristics only.

FIGURE 2 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

MC14049B



MC14050B

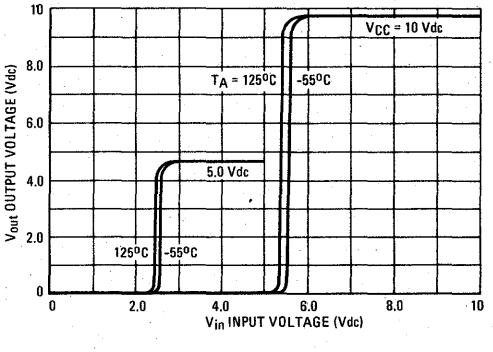


FIGURE 3 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

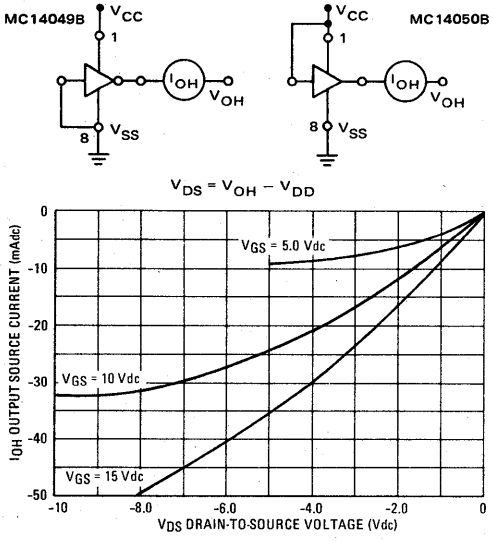


FIGURE 4 – TYPICAL OUTPUT SINK CHARACTERISTICS

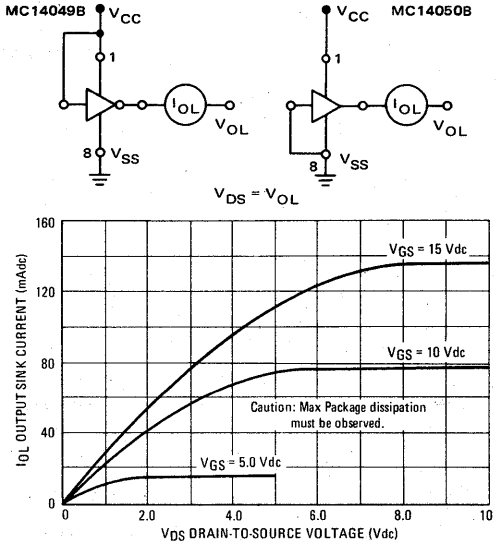
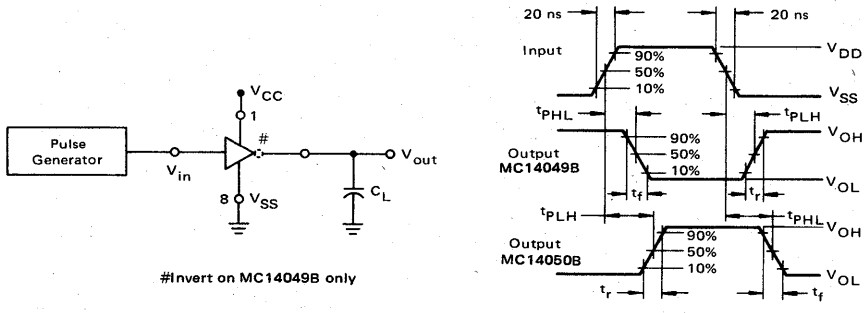


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14051B
MC14052B
MC14053B

ANALOG MULTIPLEXERS/DEMULTIPLEXERS

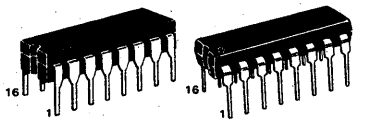
The MC14051, MC14052 and MC14053 analog multiplexers are digitally controlled analog switches. The MC14051 effectively implements an 8PST electronic switch, the MC14052 a 4PDT, and the MC14053 a DP3T. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- High On/Off Output Voltage Ratio – 65 dB typical
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches – 80 dB typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up to 65 MHz
- Linearized Transfer Characteristics, $\Delta R_{ON} < 60\ \Omega$ for $V_{in} = V_{DD}$ to V_{EE} @ 15 Vdc
- Low Noise – 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXERS/ DEMULTIPLEXERS



CASE 620
L SUFFIX
CERAMIC PACKAGE

CASE 648
P SUFFIX
PLASTIC PACKAGE

ORDERING INFORMATION

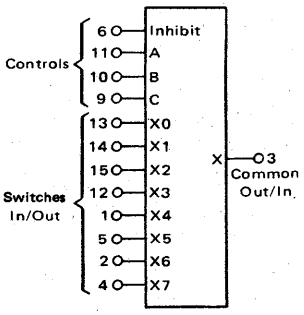
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	25	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

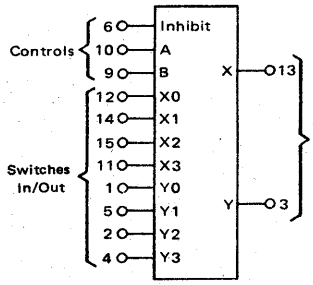
5

MC14051
8-Channel Analog Multiplexer/Demultiplexer



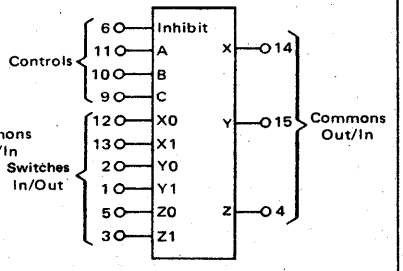
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

MC14052
Dual 4-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

MC14053
Triple 2-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

Note: Control Inputs referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be ≤ V_{SS}.

FIGURE 1 – SWITCH CIRCUIT SCHEMATIC

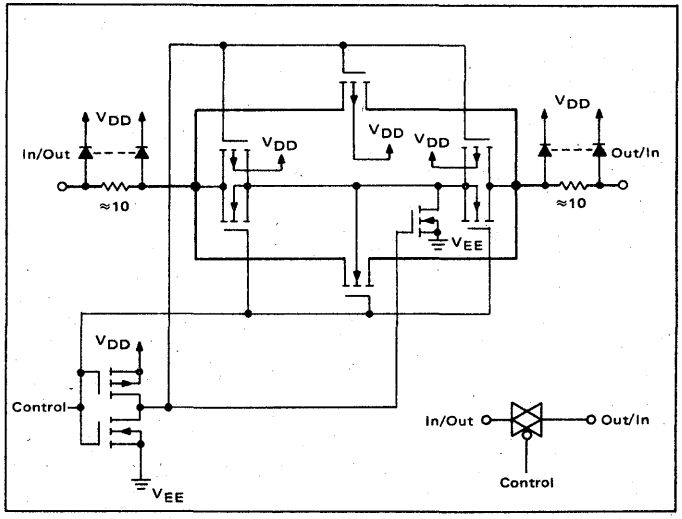
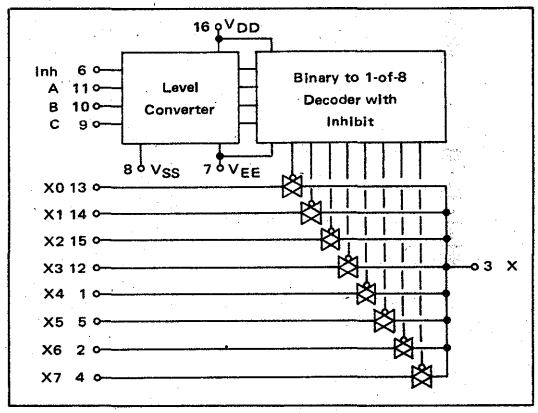


FIGURE 2 – MC14051 FUNCTIONAL DIAGRAM



TRUTH TABLE

Control Inputs				ON Switches		
	Select					
Inhibit	C*	B	A	MC14051	MC14052	MC14053
0	0	0	0	X0	Y0 X0	Z0 Y0 X0
0	0	0	1	X1	Y1 X1	Z0 Y0 X1
0	0	1	0	X2	Y2 X2	Z0 Y1 X0
0	0	1	1	X3	Y3 X3	Z0 Y1 X1
0	1	0	0	X4		Z1 Y0 X0
0	1	0	1	X5		Z1 Y0 X1
0	1	1	0	X6		Z1 Y1 X0
0	1	1	1	X7		Z1 Y1 X1
1	x	x	x	None	None	None

*Not applicable for MC14052
x = Don't Care

FIGURE 3 – MC14052 FUNCTIONAL DIAGRAM

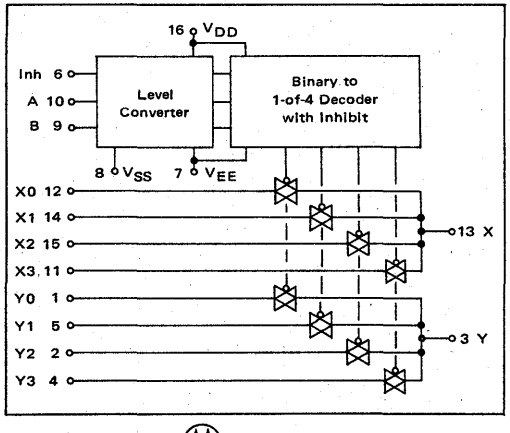
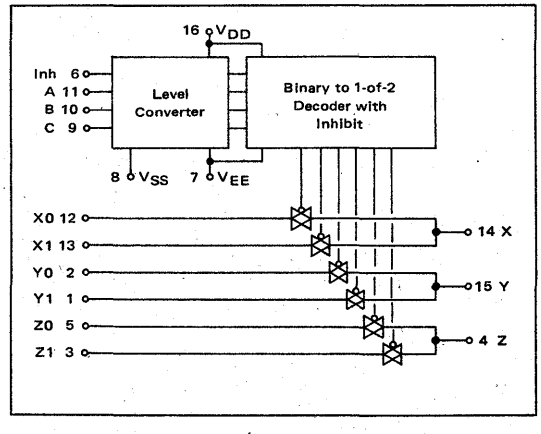


FIGURE 4 – MC14053 FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	$V_{DD}-V_{SS}$ Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{OL}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	0.01	–	0	0.01	–	0.05	
	"1" Level	V_{OH}	5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	
			15	14.99	–	14.99	15	–	14.95	–	
Input Voltage		V_{IL}									Vdc
($\Delta V_{out} \leq$ 1.5 Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq$ 3.0 Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq$4.5 Vdc)			15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq$ 1.5 Vdc)		V_{IH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq$ 3.0 Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq$ 4.5 Vdc)			15	4.4	–	4.5	6.75	–	4.5	–	
Input Current (Control, Inhibit)		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}									pF
Control, Inhibit			–	–	–	–	5.0	–	–	–	
Switch Inputs			–	–	–	–	10	–	–	–	
Output Capacitance	MC14051	C_{out}	10	–	–	–	60	–	–	–	pF
	MC14052		10	–	–	–	32	–	–	–	
	MC14053		10	–	–	–	17	–	–	–	
Feedthrough Capacitance	MC14051	C_{in-out}	10	–	–	–	0.18	–	–	–	pF
	MC14052		10	–	–	–	0.12	–	–	–	
	MC14053		10	–	–	–	0.10	–	–	–	
Quiescent Current (AL Device)		I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)			10	–	10	–	0.010	10	–	300	
			15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)		I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)			10	–	40	–	0.010	40	–	300	
			15	–	80	–	0.015	80	–	600	
Total Supply Current **†		I_T	5.0	$I_T = (0.07\ \mu A/kHz)\ f + I_{DD}$							μAdc
(Dynamic plus Quiescent,			10	$I_T = (0.20\ \mu A/kHz)\ f + I_{DD}$							
Per Package)			15	$I_T = (0.36\ \mu A/kHz)\ f + I_{DD}$							
ON Resistance (AL Device)		R_{ON}	5.0	–	800	–	250	1050	–	1300	Ω
			10	–	400	–	120	500	–	550	
			15	–	220	–	80	280	–	320	
ON Resistance (CL/CP Device)		R_{ON}	5.0	–	880	–	250	1050	–	1200	Ω
			10	–	450	–	120	500	–	520	
			15	–	250	–	80	280	–	300	
Δ ON Resistance Between Any Two Channels		ΔR_{ON}	5.0	–	–	–	25	–	–	–	Ω
			10	–	–	–	10	–	–	–	
			15	–	–	–	5.0	–	–	–	
OFF Channel Leakage Current	Any Channel	–	15	–	100	–	±0.01	100	–	–	nAdc
(AL Device)	All Channels OFF:										
	MC14051		15	–	100	–	±0.08	100	–	–	
	MC14052		15	–	100	–	±0.04	100	–	–	
	MC14053		15	–	100	–	±0.02	100	–	–	
OFF Channel Leakage Current	Any Channel	–	15	–	1000	–	±0.01	1000	–	–	nAdc
(CL/CP Device)	All Channels OFF:										
	MC14051		15	–	1000	–	±0.08	1000	–	–	
	MC14052		15	–	1000	–	±0.04	1000	–	–	
	MC14053		15	–	1000	–	±0.02	1000	–	–	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity is defined as the control input voltage coincident with the specified change, ΔV_{out}, at an output in the OFF state.
**The formulas given are for the typical characteristics only at 25°C.
†Total Supply Current, I_T, is the current drawn at device terminals V_{DD} and V_{SS} for total current through the device. The channel component, $(V_{in}-V_{out})/R_{ON}$, should not be included.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}-V_{SS} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Propagation Delay Times	t_{PLH},t_{PHL}					ns
Switch Input to Switch Output (R_L = 10 kΩ)						
MC14051						
t_{PLH},t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns		5.0	35	55	90	
t_{PLH},t_{PHL} = (0.08 ns/pF) C_L + 11 ns		10	15	25	40	
t_{PLH},t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns		15	12	18	30	
MC14052						
t_{PLH},t_{PHL} = (0.17 ns/pF) C_L + 21.5 ns		5.0	30	45	75	ns
t_{PLH},t_{PHL} = (0.08 ns/pF) C_L + 8.0 ns		10	12	18	30	
t_{PLH},t_{PHL} = (0.06 ns/pF) C_L + 7.0 ns		15	10	15	25	
MC14053						
t_{PLH},t_{PHL} = (0.17 ns/pF) C_L + 16.5 ns		5.0	25	40	65	ns
t_{PLH},t_{PHL} = (0.08 ns/pF) C_L + 4.0 ns		10	8.0	12	20	
t_{PLH},t_{PHL} = (0.06 ns/pF) C_L + 3.0 ns		15	6.0	9.0	15	
Inhibit to Output (R_L = 10 kΩ):						
Output "1" or "0" to High Impedance, or	$t_{"1"H}$,$t_{"0"H}$					ns
High Impedance to "1" or "0" Level	$t_{H"1"}$,$t_{H"0"}$					
MC14051		5.0	850	1275	2125	
		10	300	450	750	
		15	250	375	625	
MC14052		5.0	950	1425	2375	ns
		10	325	490	800	
		15	230	350	575	
MC14053		5.0	1000	1500	2500	ns
		10	350	525	875	
		15	215	325	540	
Control Input to Output (R_L = 10 kΩ)	t_{PLH},t_{PHL}					ns
MC14051		5.0	350	525	875	
		10	140	210	350	
		15	100	150	250	
MC14052		5.0	325	490	815	ns
		10	130	195	325	
		15	90	135	225	
MC14053		5.0	300	450	750	ns
		10	120	180	300	
		15	80	120	200	
Sine Wave Distortion (R_L = 1 kΩ, f = 1 kHz)	–	10	0.04	–	–	%
Bandwidth (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD} -V_{SS}) p-p, 20 $Log_{10}\frac{V_{out}}{V_{in}}$ = -3 dB)	BW					MHz
MC14051		10	20	–	–	
MC14052		10	30	–	–	
MC14053		10	55	–	–	
Feedthrough Attenuation, Input to Output	–					MHz
(R_L = 1 kΩ, 20 $Log_{10}\frac{V_{out}}{V_{in}}$ = -50 dB) MC14051		10	4.5	–	–	
MC14052		10	3.5	–	–	
MC14053		10	3.0	–	–	
Channel Separation (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD} -V_{SS}) p-p, 20 $Log_{10}\frac{V_{out(B)}}{V_{in(A)}}$ = -50 dB)	–	10	3.0	–	–	MHz
Feedthrough Control, Input to Output (R1 = 1 kΩ, R_L = 10 kΩ, Control/Inhibit t_r = t_f = 20 ns)	–	10	30	–	–	mV
Maximum Control Frequency (R_L = 1 kΩ, V_{out} = 1/2 V_{in})	–	10	10	–	–	MHz

*The formulas given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range VEE ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TEST CIRCUITS

FIGURE 5 – NOISE IMMUNITY

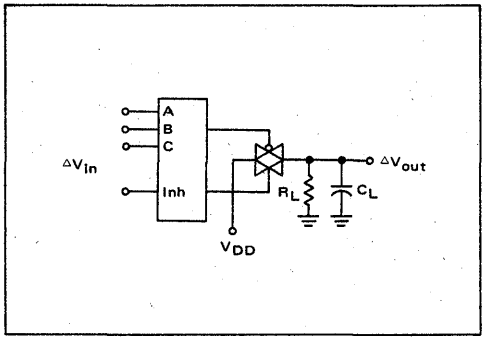


FIGURE 6 – PROPAGATION DELAY TIMES, CONTROL AND INHIBIT TO OUTPUT

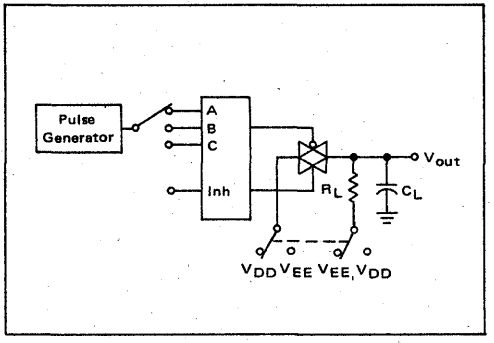


FIGURE 7 – BANDWIDTH AND FEEDTHROUGH ATTENUATION

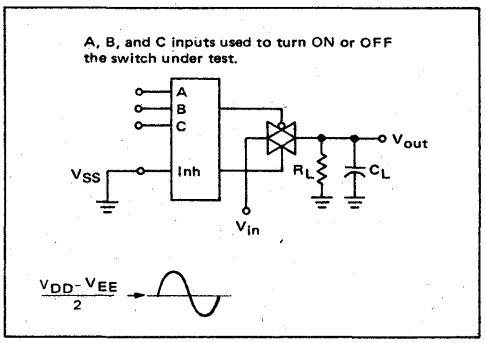


FIGURE 8 – CROSSTALK BETWEEN ANY TWO SWITCHES

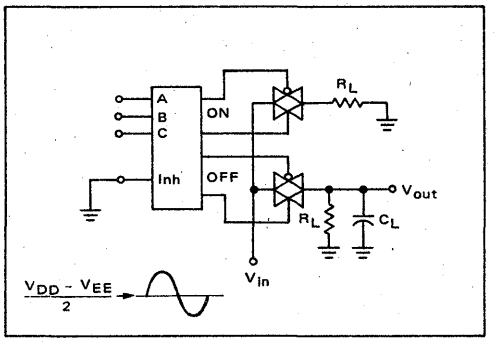


FIGURE 9 – FEEDTHROUGH, CONTROL TO SIGNAL OUTPUT

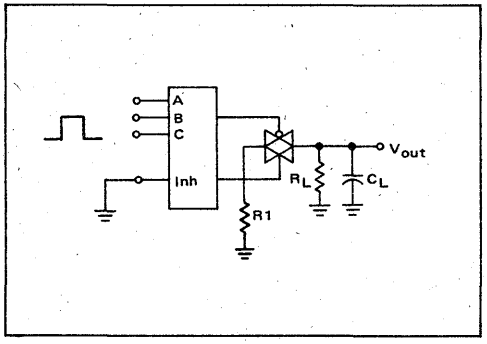


FIGURE 10 – MAXIMUM CONTROL FREQUENCY

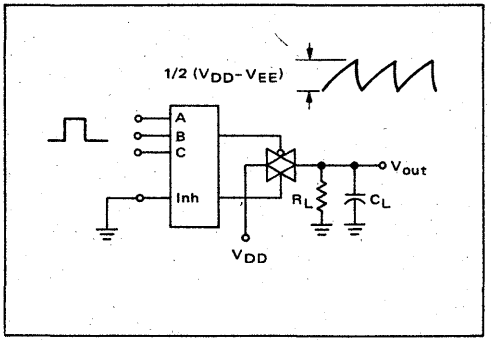
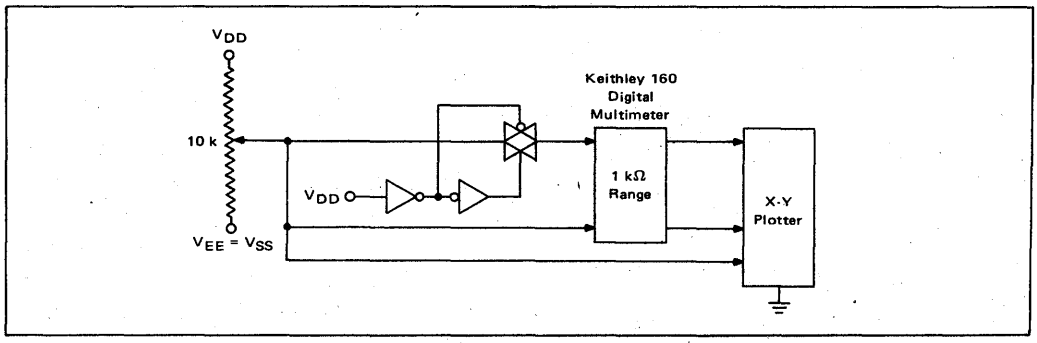


FIGURE 11 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 12 – V_{DD} = 7.5 V, V_{EE} = -7.5 V

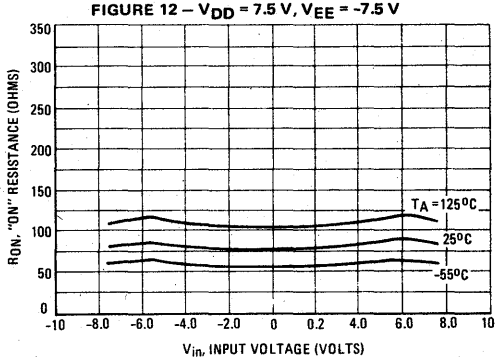


FIGURE 13 – V_{DD} = 5.0 V, V_{EE} = -5.0 V

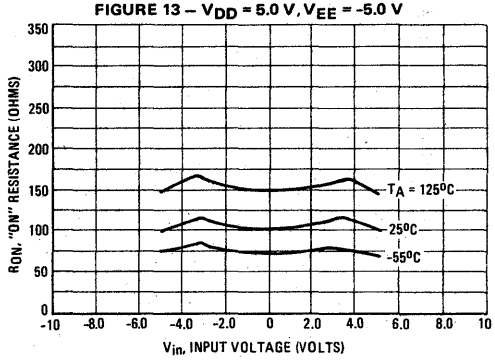


FIGURE 14 – V_{DD} = 2.5 V, V_{EE} = -2.5 V

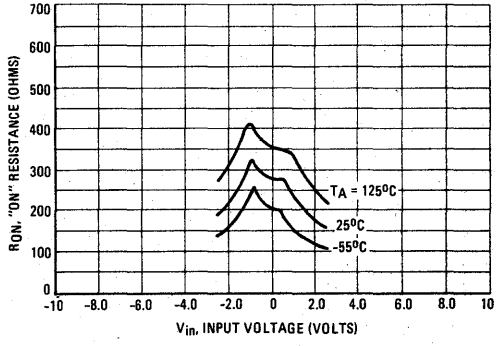
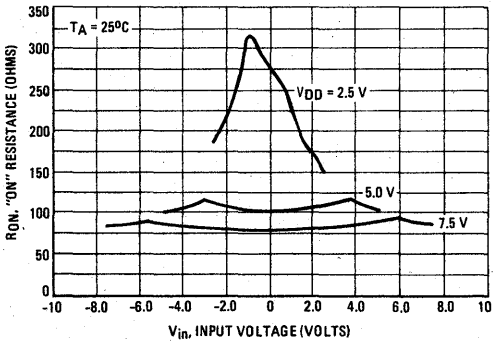


FIGURE 15 – COMPARISON AT 25°C, V_{DD} = -V_{EE}



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MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14066B

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

The MC14066 consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

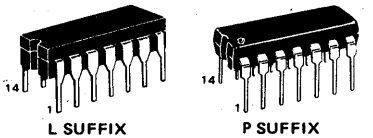
The MC14066 is designed to be pin-for-pin compatible with the MC14016, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- High On/Off Output Voltage Ratio — 65 dB typical
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches —50 dB typical @ 8 MHz
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up to 65 MHz @ 10 Vdc
- Linearized Transfer Characteristics, $\Delta R_{ON} < 60\ \Omega$ for $V_{in} = V_{DD}$ to V_{SS} (at 15V)
- Low Noise — 12 $nV/\sqrt{Cycle}$, f ⩾ 1 kHz typical
- Pin-for-Pin Replacement for CD4016, CD4066, MC14016

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH
QUAD MULTIPLEXER



L SUFFIX
CERAMIC PACKAGE
CASE 632

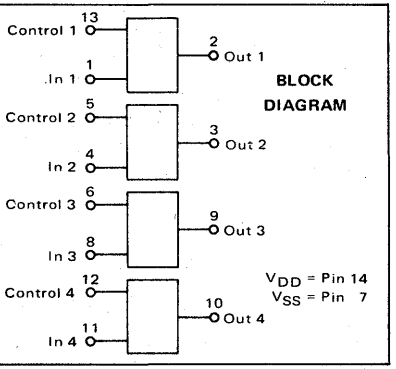
P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

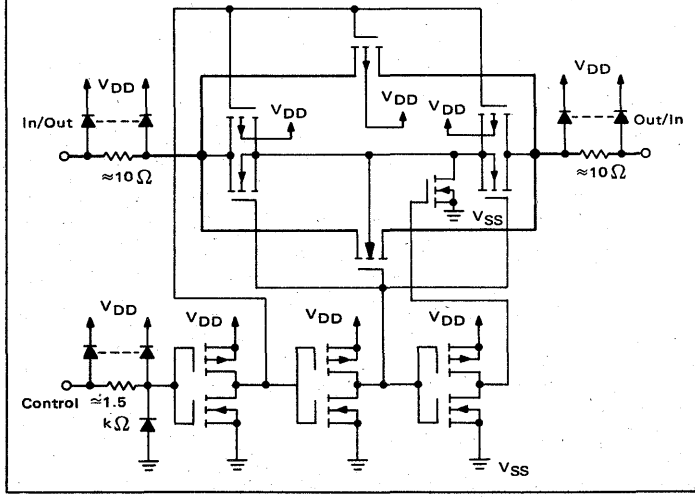
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

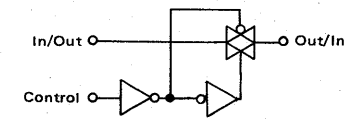
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	25	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)



LOGIC DIAGRAM AND TRUTH TABLE
(1/4 OF DEVICE SHOWN)



Control	Switch
0	OFF
1	ON

Logic Diagram Restrictions
$V_{SS} \leq V_{in} \leq V_{DD}$
$V_{SS} \leq V_{out} \leq V_{DD}$

$V_{control}$	V_{in} to V_{out} Resistance
V_{SS}	$>10^9$ Ohms typ
V_{DD}	3×10^2 Ohms typ

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Voltage (Control) "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0		1.5		2.25	1.5	--	1.5	
(V_O = 9.0 or 1.0 Vdc)		10		3.0	--	4.50	3.0	--	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	--	3.75	--	6.75	3.75	--	3.75	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	--	3.5	2.75	--	3.5	--	
(V_O = 1.0 or 9.0 Vdc)		10	7.0		7.0	5.50	--	7.0	--	
(V_O = 1.5 or 13.5 Vdc)		15	11.25		11.25	8.25	--	11.25	--	
Input Current (AL Device) Control	I_{in}	15		±0.1	--	±0.00001	±0.1	--	±1.0	µAdc
Input Current (CL/CP Device) Control	I_{in}	15		±0.3	--	±0.00001	±0.3	--	±1.0	µAdc
Input Capacitance (V_{in} 0)	C_{in}									pF
Control Input						5.0	--	--	--	
Switch Inputs		10				8.0	--	--	--	
Output Capacitance	C_{out}	10				8.0	--	--	--	pF
Feedthrough Capacitance	C_{in-out}	10				0.5	--	--	--	pF
Quiescent Current (AL Device)	I_Q	5.0		0.25		0.0005	0.25	--	7.5	µAdc
(Per Package)		10		0.50		0.0010	0.50	--	15	
		15		1.00		0.0015	1.00	--	30	
Quiescent Current (CL/CP Device)	I_Q	5.0		1.0		0.0005	1.0	--	7.5	µAdc
(Per Package)		10		2.0		0.0010	2.0	--	15	
		15		4.0		0.0015	4.0	--	30	
ON Resistance (AL Device)	R_{ON}	5.0		800		250	1050	--	1300	Ω
		10		400		120	500	--	550	
		15		220		80	280	--	320	
ON Resistance (CL/CP Device)	R_{ON}	5.0		880		250	1050	--	1200	Ω
		10		450		120	500	--	520	
		15		250		80	280	--	300	
ΔON Resistance Between Any Two of Four Switches	ΔR_{ON}	5.0				25	--	--	--	Ω
		10				10	--	--	--	
		15				5.0	--	--	--	
Input/Output Leakage Current Switch OFF (AL Device)		15		±100		±0.01	±100	--	±1000	nAdc
Input/Output Leakage Current Switch OFF (CL/CP Device)		15		±300		±0.01	±300	--	±1000	nAdc

*The formulas given are for the typical characteristics only.
T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	V_{DD} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Propagation Delay Times	V_{SS} = 0 Vdc						
Input to Output (R_L = 10 kΩ)		t_{PLH},t_{PHL}					ns
t_{PLH},t_{PHL} = (0.17 ns/pF) C_L + 15.5 ns			5.0	20	30	45	
t_{PLH},t_{PHL} = (0.08 ns/pF) C_L + 6.0 ns			10	10	15	30	
t_{PLH},t_{PHL} = (0.06 ns/pF) C_L + 4.0 ns			15	7.0	10	20	
Control to Output (R_L = 300 Ω)							
Output "1" to High Impedance		$t_{"1"H}$	5.0	35	50	100	ns
			10	30	45	90	
			15	25	38	75	
Output "0" to High Impedance		$t_{"0"H}$	5.0	30	45	90	ns
			10	25	38	75	
			15	20	30	60	
High Impedance to Output "1"		$t_{H"1"}$	5.0	60	90	180	ns
			10	20	30	60	
			15	15	22	45	
High Impedance to Output "0"		$t_{H"0"}$	5.0	60	90	180	ns
			10	16	25	50	
			15	14	20	40	
Sine Wave Distortion (V_{in} = 1.77 Vdc, RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	V_{SS} = -5 Vdc		5.0	0.1	–	–	%
Frequency Response (Switch ON) (R_L = 1 kΩ, $20 \log_{10}\frac{V_{out}}{V_{in}}$ = -3 dB)	V_{SS} = -5 Vdc		5.0	65	–	–	MHz
Feedthrough Attenuation (Switch OFF) (R_L = 1 kΩ, $20 \log_{10}\frac{V_{out}}{V_{in}}$ = -50 dB)	V_{SS} = -5 Vdc	–	5.0	1.0	–	–	MHz
Crosstalk Between Any Two Switches (R_L = 1 kΩ, $20 \log_{10}\frac{V_{out(B)}}{V_{in(A)}}$ = -50 dB, (Switch A ON, Switch B OFF)	V_{SS} = -5 Vdc	–	5.0	8.0	–	–	MHz
Crosstalk, Control Input to Signal Output	V_{SS} = -5 Vdc	–	5.0	50	–	–	mV
Maximum Control Input Frequency ($20 \log_{10}\frac{V_{out}}{V_{in}}$ = -6 dB)	V_{SS} = 0 Vdc	–	5.0	6.0	–	–	MHz
			10	8.0	–	–	
			15	8.5	–	–	

*The formulas given are for the typical characteristics only.
T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

TEST CIRCUITS

FIGURE 1 – NOISE IMMUNITY

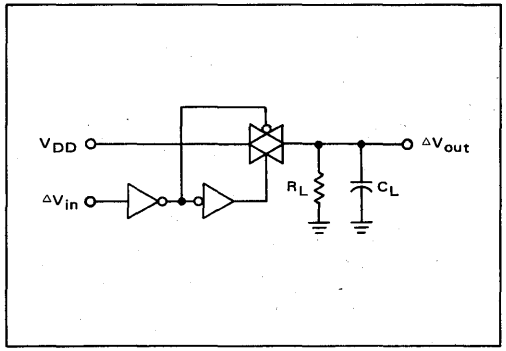

FIGURE 2 – PROPAGATION DELAY TIME, CONTROL TO OUTPUT

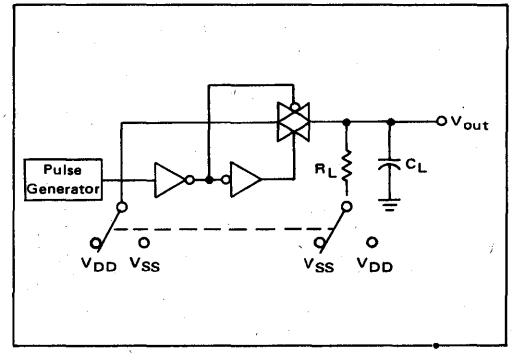

FIGURE 3 – BANDWIDTH AND FEEDTHROUGH ATTENUATION

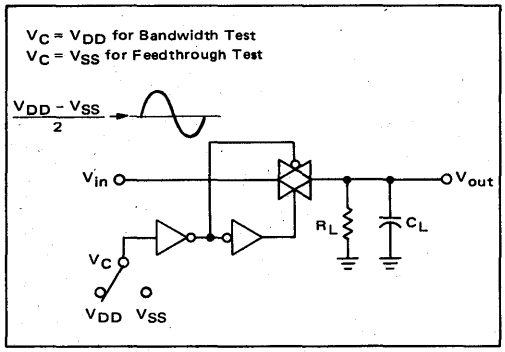

FIGURE 4 – CROSSTALK BETWEEN ANY TWO SWITCHES

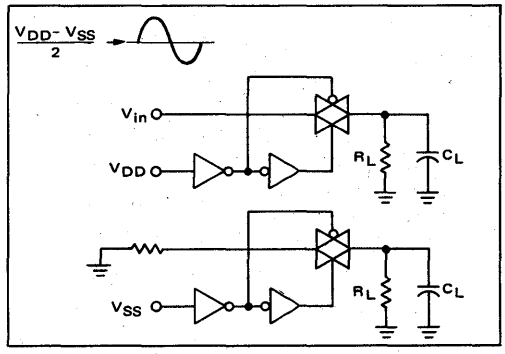

FIGURE 5 – FEEDTHROUGH, CONTROL TO OUTPUT

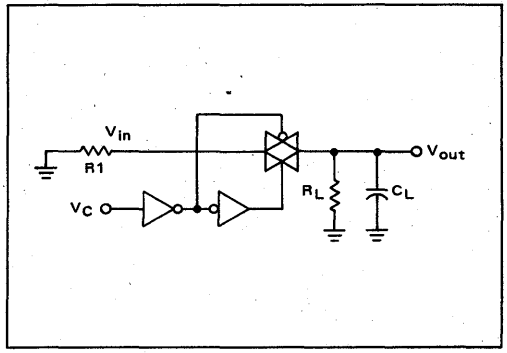

FIGURE 6 – MAXIMUM CONTROL FREQUENCY

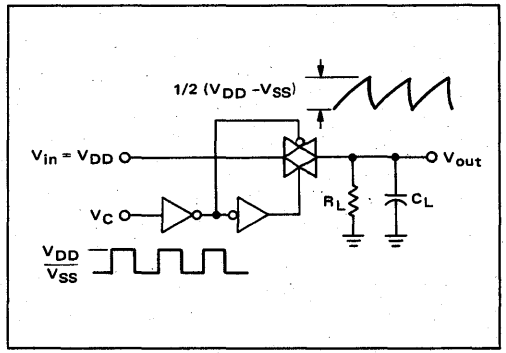

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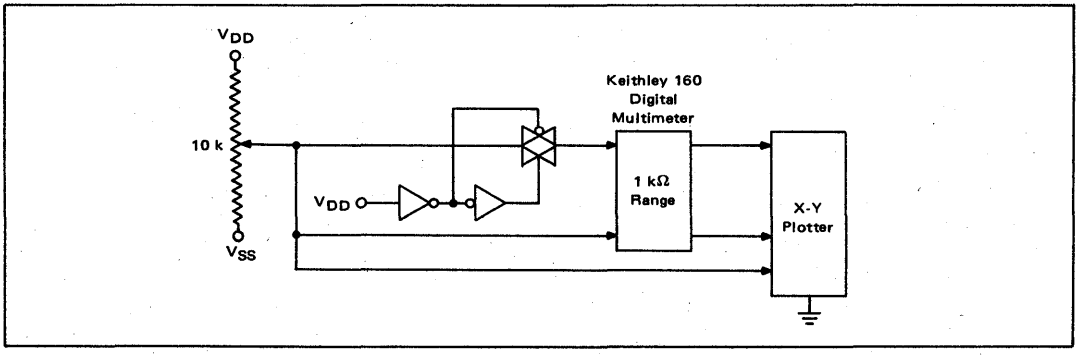
FIGURE 7 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 8 – V_{DD} = 7.5 V, V_{SS} = -7.5 V

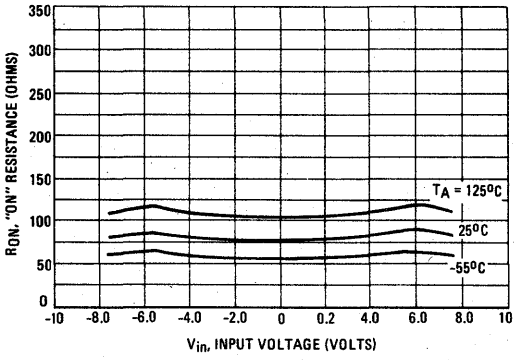


FIGURE 9 – V_{DD} = 5.0 V, V_{SS} = -5.0 V

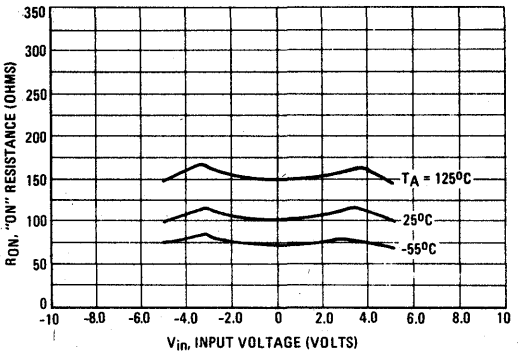


FIGURE 10 – V_{DD} = 2.5 V, V_{SS} = -2.5 V

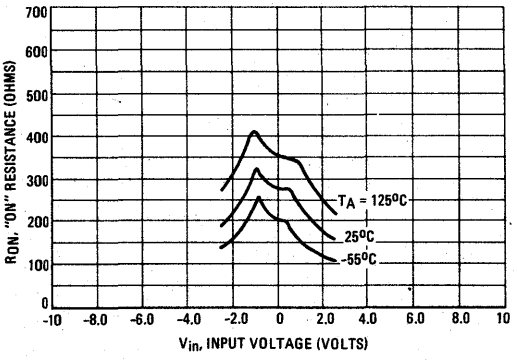
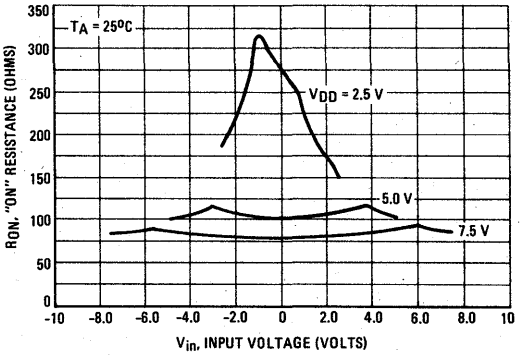


FIGURE 11 – COMPARISON AT 25°C, V_{DD} = -V_{SS}



MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14068B

B-SUFFIX SERIES McMOS GATES

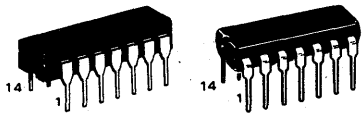
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4068B

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

8-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS})

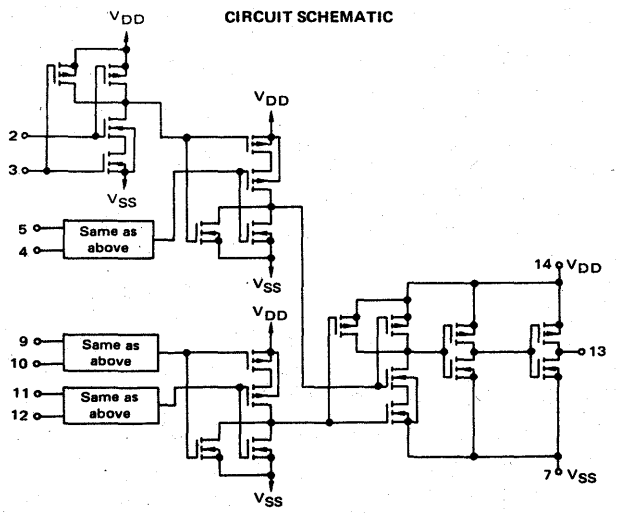
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ORDERING INFORMATION

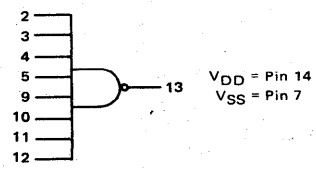
MC14XXXB — Suffix — Denotes
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

MOTOROLA Semiconductors

BOX 20912 • PHOENIX, ARIZONA 85036

MC14069B

HEX INVERTER

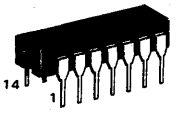
The MC14069B hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4069B

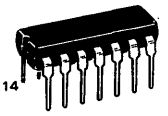
McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX INVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS})

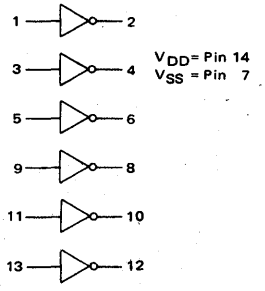
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ORDERING INFORMATION

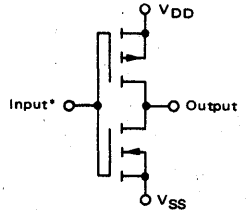
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

5

LOGIC DIAGRAM



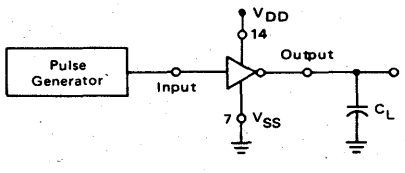
CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)

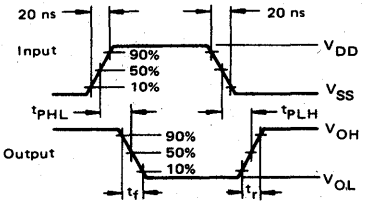


*Double diode protection on all inputs not shown.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.4	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	2.9	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.6	
"1" Level	V_{IH}									
(V_O = 1.4 or 3.6 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 2.8 or 7.2 Vdc)		10	7.1	–	7.0	5.50	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.4	–	11.25	8.25	–	11.25	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**†	I_T	5.0	I_T = (0.3 μA/kHz) f + I_{DD}/6							μAdc
(Dynamic plus Quiescent, Per Gate)		10	I_T = (0.6 μA/kHz) f + I_{DD}/6							
(C_L = 50 pF)		15	I_T = (0.9 μA/kHz) f + I_{DD}/6							
Output Rise and Fall Times**	t_r,t_f									ns
(C_L = 50 pF)										
t_r,t_f = (1.35 ns/pF) C_L + 33 ns		5.0	–	–	–	100	200	–	–	
t_r,t_f = (0.60 ns/pF) C_L + 20 ns		10	–	–	–	50	100	–	–	
t_r,t_f = (0.40 ns/pF) C_L + 20 ns		15	–	–	–	40	80	–	–	
Propagation Delay Times**	t_{PLH}, t_{PHL}									ns
(C_L = 50 pF)										
t_{PLH},t_{PHL} = (0.90 ns/pF) C_L + 20 ns		5.0	–	–	–	65	125	–	–	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 22 ns		10	–	–	–	40	80	–	–	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 17 ns		15	–	–	–	30	60	–	–	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

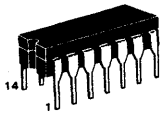
MC14070B
QUAD EXCLUSIVE "OR" GATE

MC14077B
QUAD EXCLUSIVE "NOR" GATE

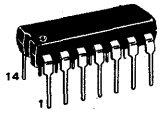
McMOS SSI
QUAD EXCLUSIVE "OR" AND "NOR" GATES

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- MC14070B – Replacement for CD4030, CD4070, and MC14507 Types
- MC14077B – Replacement for CD4077 Type



CASE 632
L SUFFIX
CERAMIC PACKAGE



CASE 646
P SUFFIX
PLASTIC PACKAGE

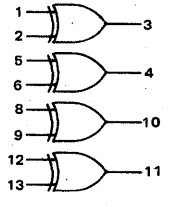
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

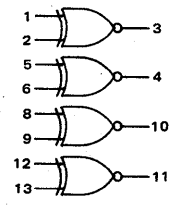
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

MC14070
Quad Exclusive OR Gate

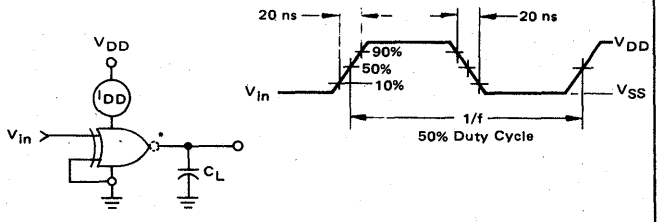


MC14077
Quad Exclusive NOR Gate



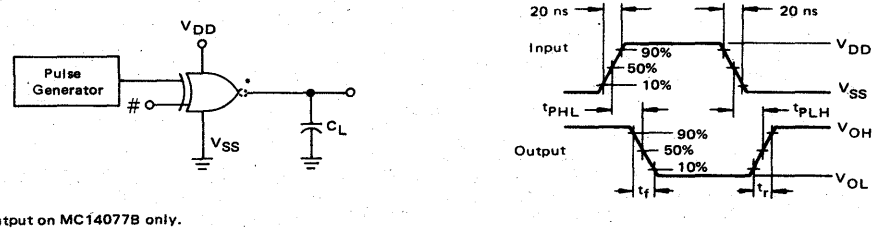
V_{DD} = Pin 14
V_{SS} = Pin 7
(Both Devices)

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



*Inverted output on MC14077B only.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



*Inverted output on MC14077B only.
#Connect unused input to V_{DD} for MC14070B, to V_{SS} for MC14077B.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.3 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.6 μA/kHz) f + I_{DD}							
		15	I_T = (0.9 μA/kHz) f + I_{DD}							
Output Rise and Fall Times** (C_L = 50 pF)	t_r,t_f									ns
t_r,t_f = (1.35 ns/pF) C_L + 33 ns		5.0	–	–	–	100	200	–	–	
t_r,t_f = (0.60 ns/pF) C_L + 20 ns		10	–	–	–	50	100	–	–	
t_r,t_f = (0.40 ns/pF) C_L + 20 ns		15	–	–	–	40	80	–	–	
Propagation Delay Times** (C_L = 50 pF)	t_{PLH}, t_{PHL}									ns
t_{PLH},t_{PHL}=(0.90 ns/pF) C_L+115 ns		5.0	–	–	–	175	350	–	–	
t_{PLH},t_{PHL}=(0.36 ns/pF) C_L+47 ns		10	–	–	–	75	150	–	–	
t_{PLH},t_{PHL}=(0.26 ns/pF) C_L+37 ns		15	–	–	–	50	100	–	–	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MC14071
MC14071B

QUAD 2-INPUT "OR" GATE

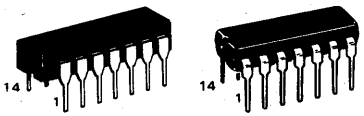
The MC14071 and MC14071B are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14071B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4071A and CD4071B

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "OR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

Delete for Non-B Device

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

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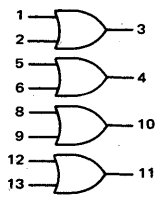
See the MC14001 data sheet for complete characteristics for the non-B device.

See the MC14001B data sheet for complete characteristics of the B-Series device.

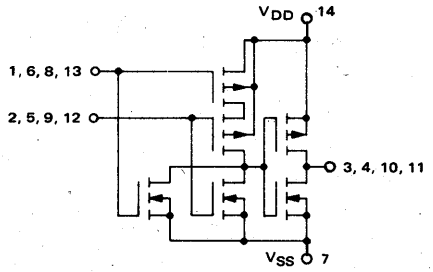
LOGIC DIAGRAM



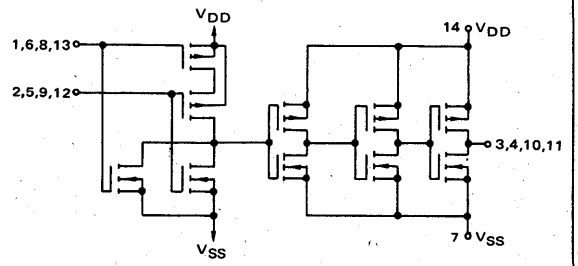
V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATICS
(1/4 of Device Shown)

MC14071



MC14071B



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MC14072B

B-SUFFIX SERIES McMOS GATES

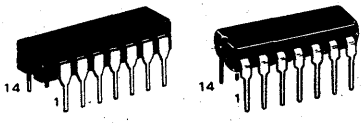
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4072B

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "OR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB ___ Suffix

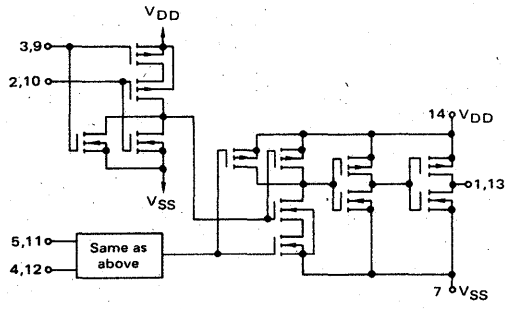
Suffix	Denotes
L	Ceramic Package
P	Plastic Package
A	Extended Operating Temperature Range
C	Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

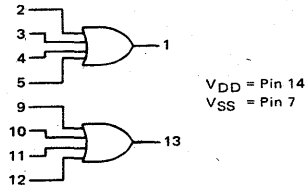
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATIC
(1/2 of Device Shown)



LOGIC DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

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MC14073B

B-SUFFIX SERIES McMOS GATES

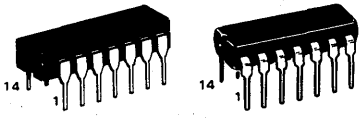
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4073B

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "AND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

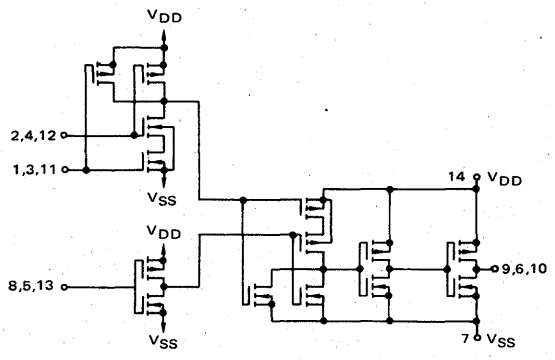
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

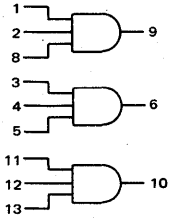
5

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATICS
(1/3 of Device Shown)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MC14075B

B-SUFFIX SERIES McMOS GATES

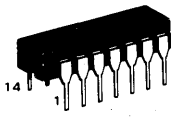
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4075B

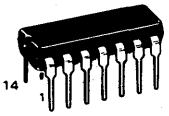
McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "OR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

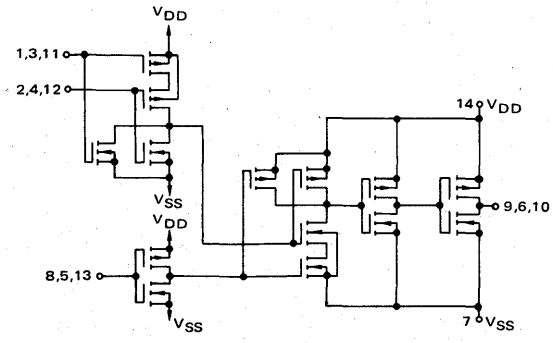
MC14XXXB — Suffix — Denotes
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

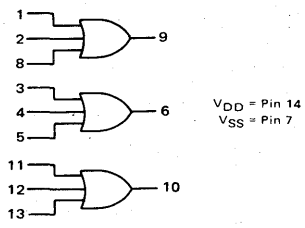
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATIC
(1/3 of Device Shown)



LOGIC DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

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MC14076B

4-BIT D-TYPE REGISTER with THREE-STATE OUTPUTS

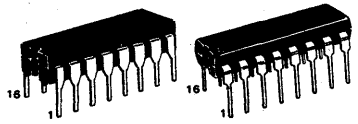
The MC14076B 4-Bit Register consists of four D-type flip-flops operating synchronously from a common clock. OR gated output-disable inputs force the outputs into a high-impedance state for use in bus organized systems. OR gated data-disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master reset is provided to clear all four flip-flops simultaneously independent of the clock or disable inputs.

- Three-State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- For Bus Buffer Registers
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD D-TYPE REGISTER with THREE STATE OUTPUTS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

5

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

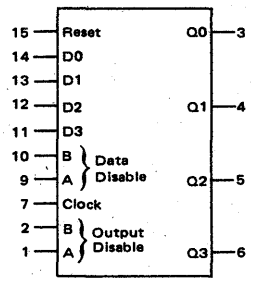
FUNCTION TABLE

INPUTS					OUTPUT
		Data Disable		Data	
Reset	Clock	A	B	D	Q
1	X	X	X	X	0
0	0	X	X	X	Q_n
0	⎍	1	X	X	Q_n
0	⎍	X	1	X	Q_n
0	⎍	0	0	0	0
0	⎍	0	0	1	1

When either output disable A or B (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

X = Don't Care.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.50 µA/kHz) f + I_{DD}							
		15	I_T = (2.25 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

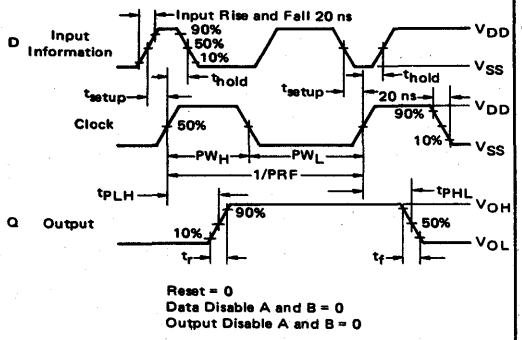
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	All Types Typ	All Types Max	Unit
Output Rise Time, All B-Series Gates	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time, All B-Series Gates	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	180	
Reset to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	180	
3-State Propagation Delay, Output "1" or "0" to High Impedance	$t_{"1"H}$, $t_{"0"H}$	5.0	–	150	300	ns
		10	–	60	120	
		15	–	45	90	
3-State Propagation Delay, High Impedance to "1" or "0" Level	$t_{H"1"}$, $t_{H"0"}$	5.0	–	200	400	ns
		10	–	80	160	
		15	–	60	120	
Minimum Clock Pulse Width	PW_C	5.0	–	130	260	ns
		10	–	55	110	
		15	–	40	80	
Minimum Reset Pulse Width	PW_R	5.0	–	185	370	ns
		10	–	75	150	
		15	–	55	110	
Data Setup Time	t_{setup}	5.0	–	15	30	ns
		10	–	5	10	
		15	–	2	4	
Data Hold Time	t_{hold}	5.0	–	65	130	ns
		10	–	30	60	
		15	–	25	50	
Data Disable Setup Time	t_{setup}	5.0	–	110	220	ns
		10	–	40	80	
		15	–	25	50	
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
Maximum Clock Pulse Frequency	PRF	5.0	1.8	3.6	–	MHz
		10	4.5	9.0	–	
		15	6.0	12	–	

*The formula given is for the typical characteristics only.

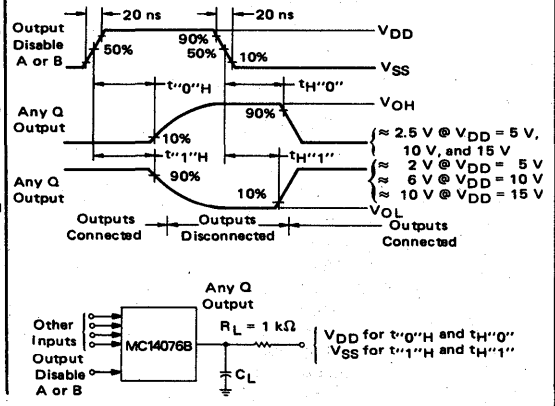
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – TIMING DIAGRAM

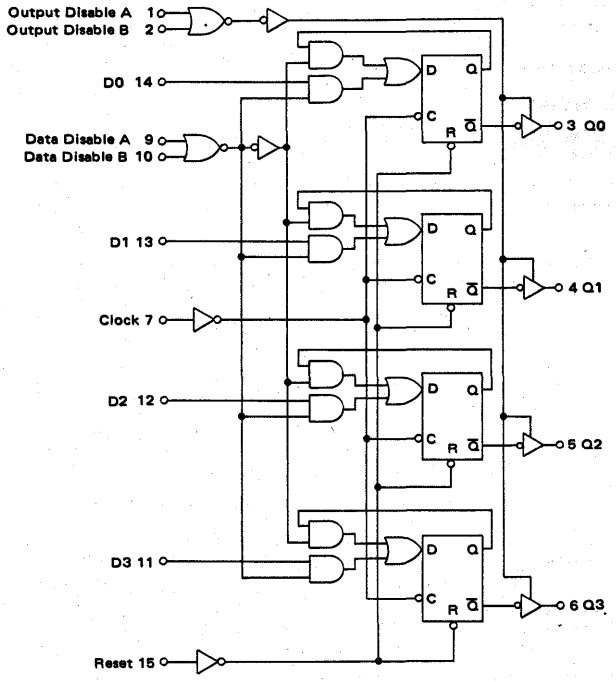


Reset = 0
Data Disable A and B = 0
Output Disable A and B = 0

FIGURE 2 – THREE-STATE PROPAGATION DELAY WAVESHAPE AND CIRCUIT



FUNCTIONAL BLOCK DIAGRAM



5

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14077B

QUAD EXCLUSIVE "NOR" GATE

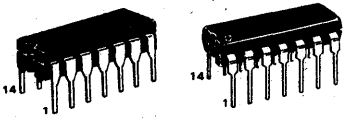
FOR COMPLETE DATA
SEE MC14070B

McMOS SSI

QUAD EXCLUSIVE "OR" AND "NOR" GATES

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- MC14070B – Replacement for CD4030, CD4070, and MC14507 Types
- MC14077B – Replacement for CD4077 Type



CASE 632
L SUFFIX
CERAMIC PACKAGE

CASE 646
P SUFFIX
PLASTIC PACKAGE

ORDERING INFORMATION

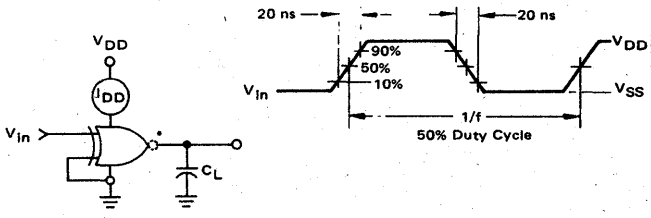
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

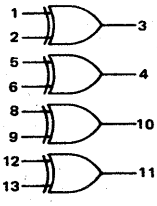
5

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

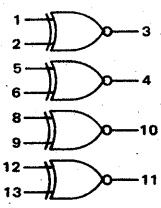


*Inverted output on MC14077B only.

MC14070
Quad Exclusive OR Gate

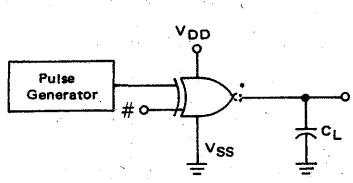


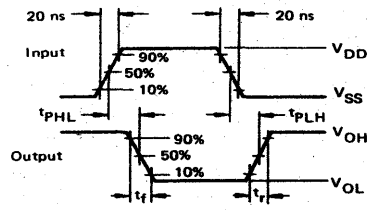
MC14077
Quad Exclusive NOR Gate



V_{DD} = Pin 14
V_{SS} = Pin 7
(Both Devices)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





*Inverted output on MC14077B only.
#Connect unused input to V_{DD} for MC14070B, to V_{SS} for MC14077B.

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MC14078B

B-SUFFIX SERIES McMOS GATES

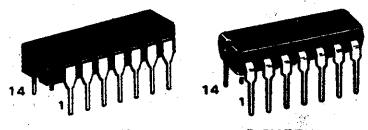
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4078B

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

8-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

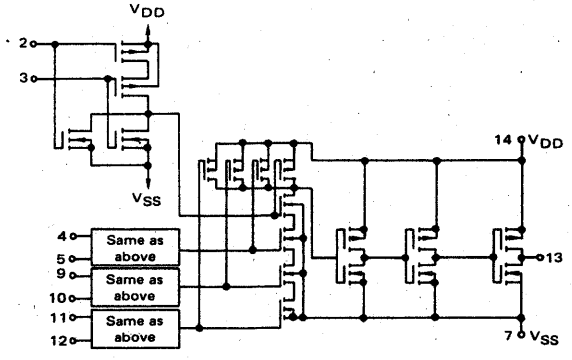
MC14XXXB — Suffix — Denotes
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

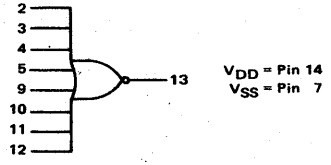
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

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MC14081
MC14081B

QUAD 2-INPUT "AND" GATE

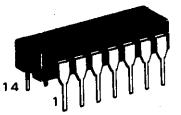
The MC14081 and MC14081B are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14081B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4081A and CD4081B

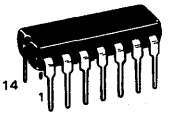
McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "AND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

Delete for Non-B Device

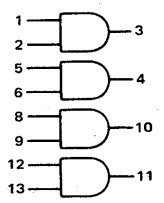
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001 data sheet for complete characteristics for the non-B device.

See the MC14001B data sheet for complete characteristics of the B-Series device.

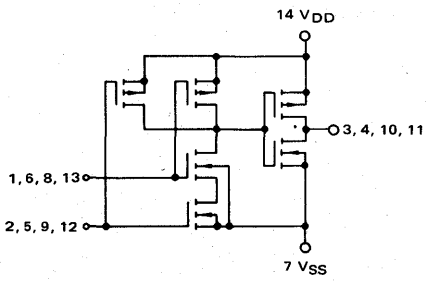
LOGIC DIAGRAM



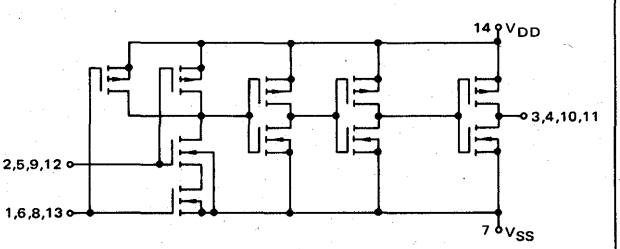
V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATICS
(1/4 of Device Shown)

MC14081



MC14081B



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MC14082B

B-SUFFIX SERIES McMOS GATES

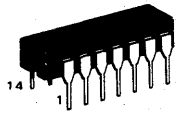
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4082B

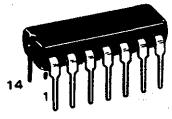
McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "AND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

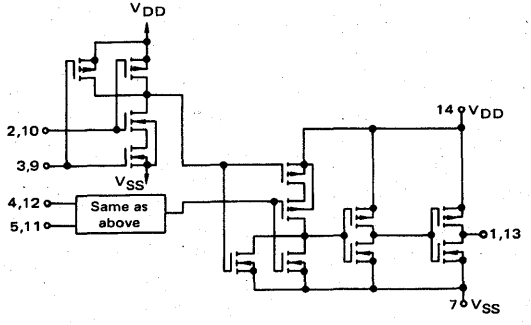
MC14XXXB — Suffix — Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

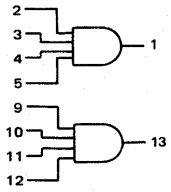
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATIC
(1/2 of Device Shown)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14093B

Advance Information

McMOS SSI

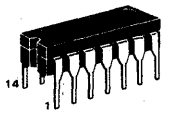
(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" SCHMITT TRIGGER

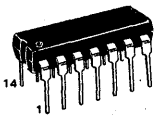
QUAD 2-INPUT "NAND" SCHMITT TRIGGER

The MC14093B Schmitt trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14093B may be used in place of the MC14011B quad 2-input NAND gate for enhanced noise immunity or to "square up" slowly changing waveforms.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Compatible with CD4093
- Can be Used to Replace MC14011B



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

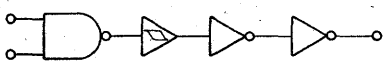
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

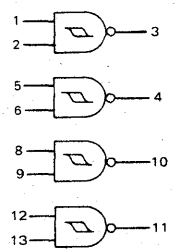
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

EQUIVALENT CIRCUIT SCHEMATIC
(1/4 OF CIRCUIT SHOWN)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This is advance information and specifications are subject to change without notice.

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
(V_{OH} = 9.5 Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	
(V_{OH} = 13.5 Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–2.5	–	–2.1	–4.2	–	–1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.52	–	–0.44	–0.88	–	–0.36	–	
(V_{OH} = 9.5 Vdc)		10	–1.3	–	–1.1	–2.25	–	–0.9	–	
(V_{OH} = 13.5 Vdc)		15	–3.6	–	–3.0	–8.8	–	–2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.2\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (2.4\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (3.6\ \mu A/kHz)\ f + I_{DD}$							
Hysteresis Voltage	V_H	5.0	–	–	–	0.3	–	–	–	Vdc
		10	–	–	–	0.4	–	–	–	
		15	–	–	–	0.7	–	–	–	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level: 1.0 Vdc min @ V_{DD} = 5.0 Vdc; 2.0 Vdc min @ V_{DD} = 10 Vdc; 2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_r	5.0 10 15		100 50 40		ns
Output Fall Time	t_f	5.0 10 15		100 50 40		ns
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0 10 15		160 65 50		ns

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVE FORMS

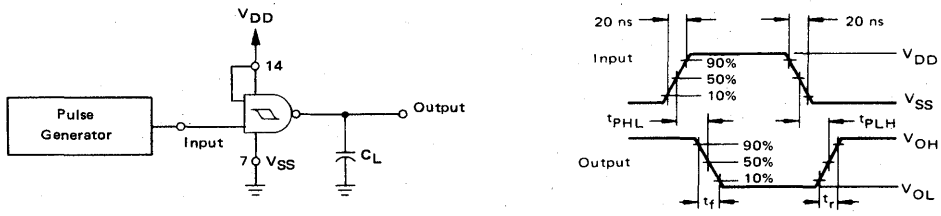
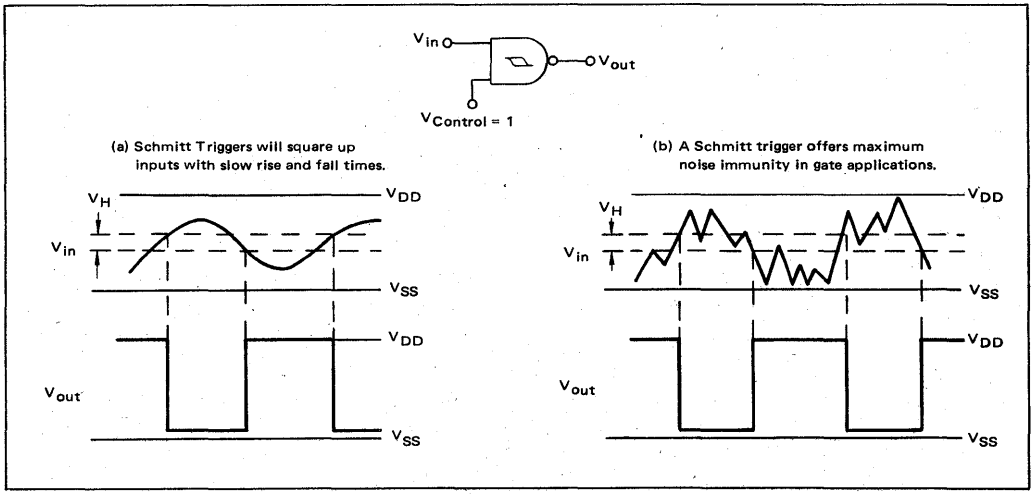


FIGURE 2 – TYPICAL SCHMITT TRIGGER APPLICATIONS



MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14160B
DECADE COUNTER
with Asynchronous Clear

MC14161B
4-BIT BINARY COUNTER
with Asynchronous Clear

MC14162B
DECADE COUNTER
with Synchronous Clear

MC14163B
4-BIT BINARY COUNTER
with Synchronous Clear

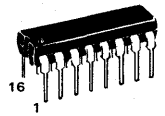
McMOS MSI

SYNCHRONOUS PROGRAMMABLE 4-BIT COUNTERS

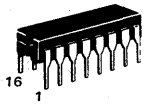
The MC14160B – MC14163B are synchronous programmable counters constructed with complementary MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These counters are functionally equivalent to the 74160–74163 TTL counters.

Two are synchronous programmable decade counters with asynchronous and synchronous clear inputs respectively (MC14160, MC14162). The other two are synchronous programmable 4-bit binary counters with the asynchronous and synchronous clear respectively (MC14161, MC14163).

- Internal Look-Ahead for Fast Counting
- Carry Output for N-Bit Cascading
- Synchronously Programmable
- Synchronous Counting
- Load Control Line
- Synchronous or Asynchronous Clear
- Positive Edge Clocked



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

ORDERING INFORMATION

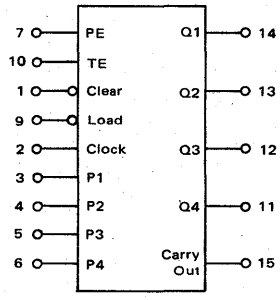
MC14xxxB — Suffix — Denotes
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.56 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.1 µA/kHz) f + I_{DD}							
		15	I_T = (1.9 µA/kHz) f + I_{DD}							

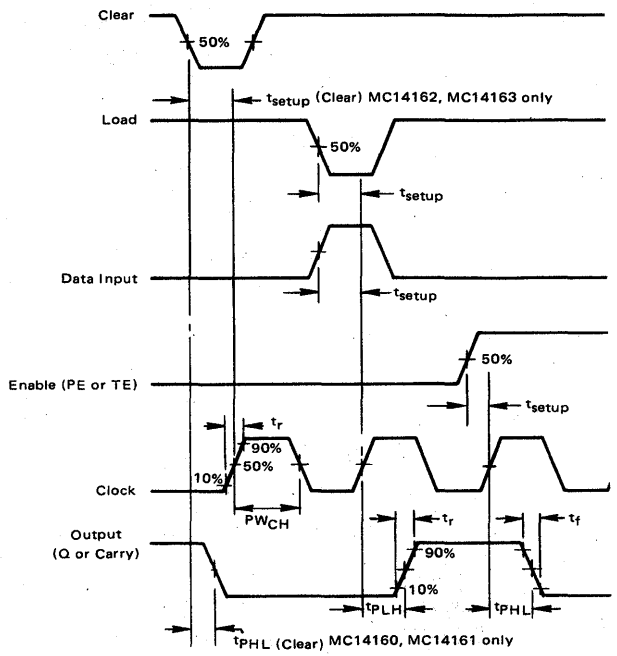
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_r					ns
t_r = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_r = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_r = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Output Fall Time	t_f					ns
t_f = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_f = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_f = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 305 ns		5.0	–	350	700	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	–	100	200	
Clock to Carry Out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 395 ns		5.0	–	440	880	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 167 ns		10	–	185	370	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 112 ns		15	–	125	250	
TE to Carry Out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 255 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 112 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 77 ns		15	–	90	180	
Clear to Q (MC14160, MC14161 only)						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 110 ns		5.0	–	155	310	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 37 ns		10	–	55	110	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 22 ns		15	–	35	70	
Minimum Setup Time						
Data to Clock	t_{setup}	5.0	–	160	320	ns
		10	–	65	130	
		15	–	45	90	
Load to Clock		5.0	–	300	600	
		10	–	130	260	
		15	–	90	180	
Enable to Clock (PE or TE)		5.0	–	210	420	
		10	–	85	170	
		15	–	60	120	
Clear to Clock (MC14162,MC14163 only)		5.0	–	155	310	
		10	–	55	110	
		15	–	35	70	
Minimum Clock Pulse Width, High	PW_{CH}	5.0	–	125	250	ns
		10	–	50	100	
		15	–	35	70	
Maximum Clock Rise Time	t_r	5	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
Maximum Clock Pulse Frequency	PRF	5.0	1.0	2.0	–	MHz
		10	2.5	5.0	–	
		15	4.0	8.0	–	

*The formula given is for the typical characteristics only.

SWITCHING WAVEFORMS



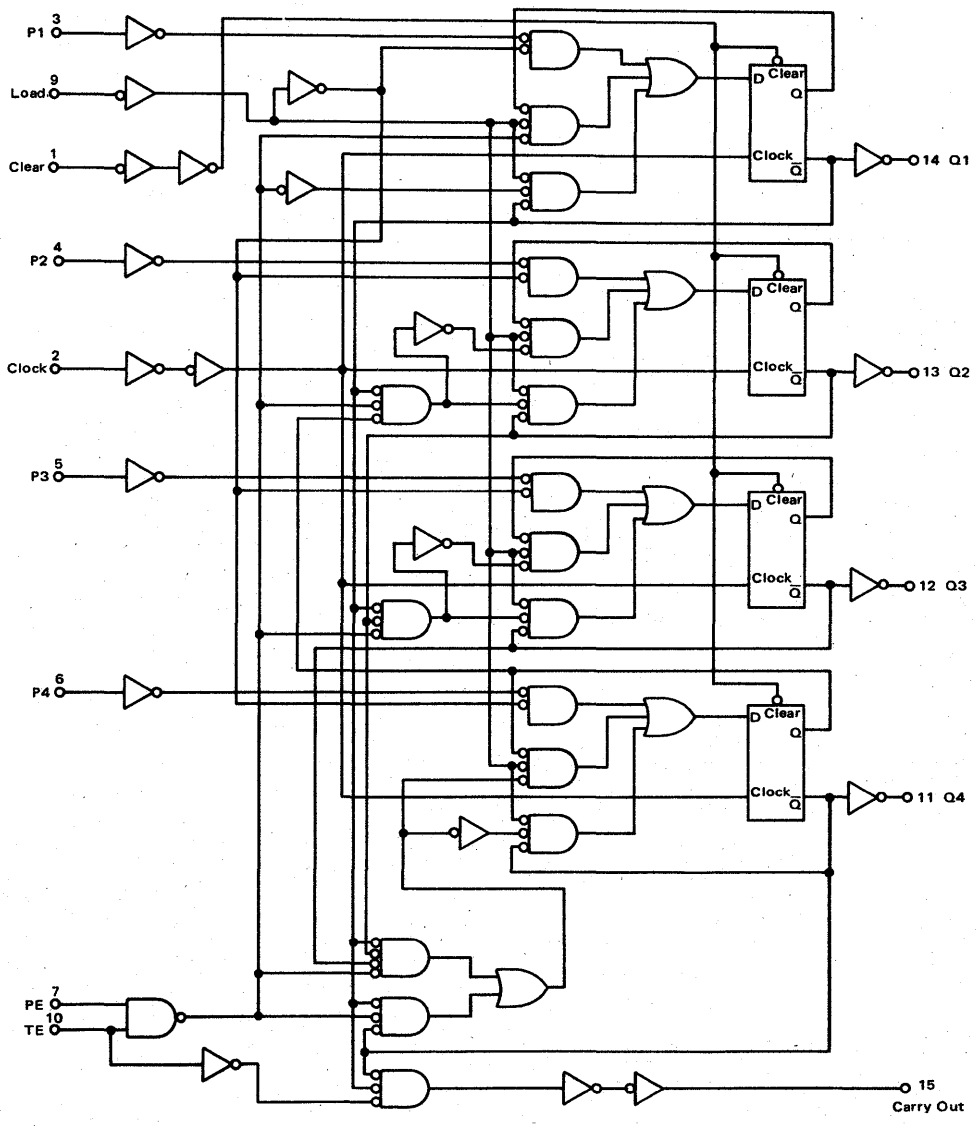
FUNCTIONAL DESCRIPTION

These counters are fully programmable; that is the outputs may be preset to either level. As presetting is synchronous, settling up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function for the MC14160, MC14161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs. The clear function for the MC14162 and MC14163 is synchronous and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily; decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (PE, TE) must be high to count, and enable input TE fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable PE or TE inputs should occur only when the clock input is high.

5

MC14160, MC14162 LOGIC DIAGRAM
(Clear is synchronous for MC14162)

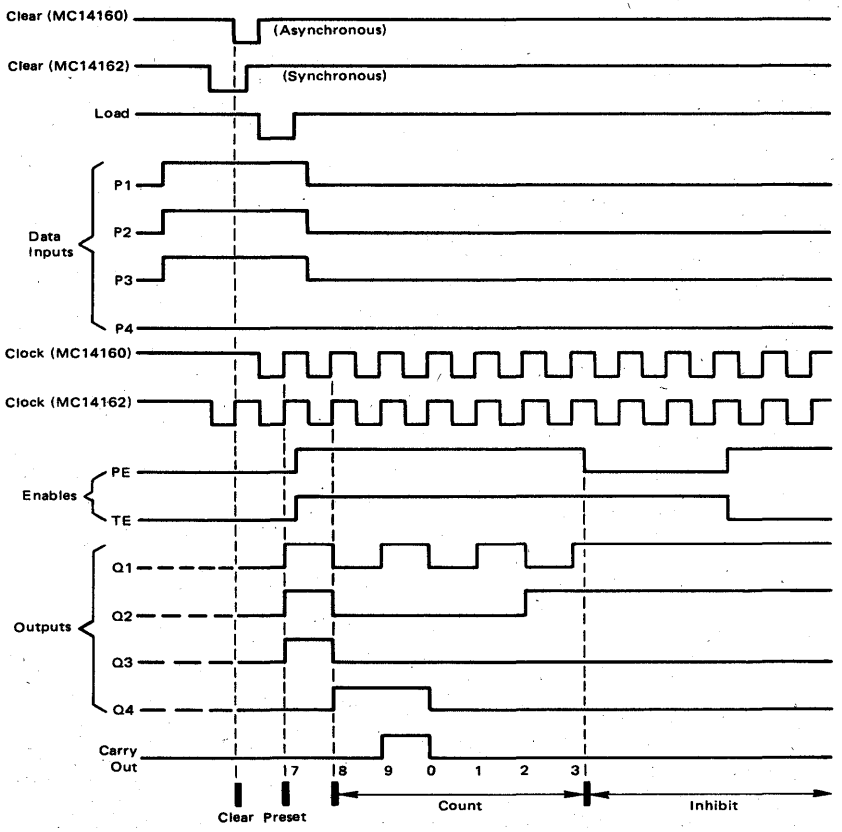


5

MC14160, MC14162 TIMING DIAGRAM

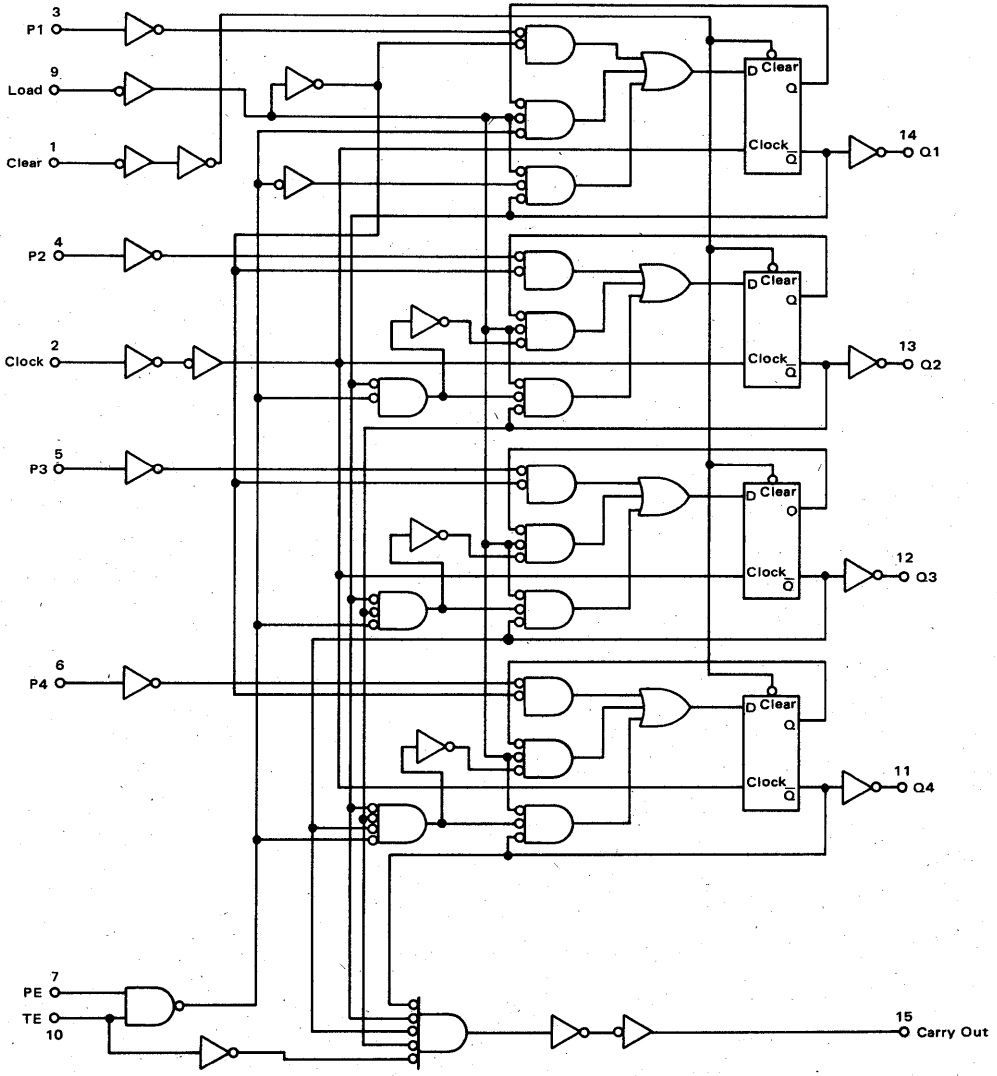
Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit



5

MC14161, MC14163 LOGIC DIAGRAM
(Clear is Synchronous for MC14163)

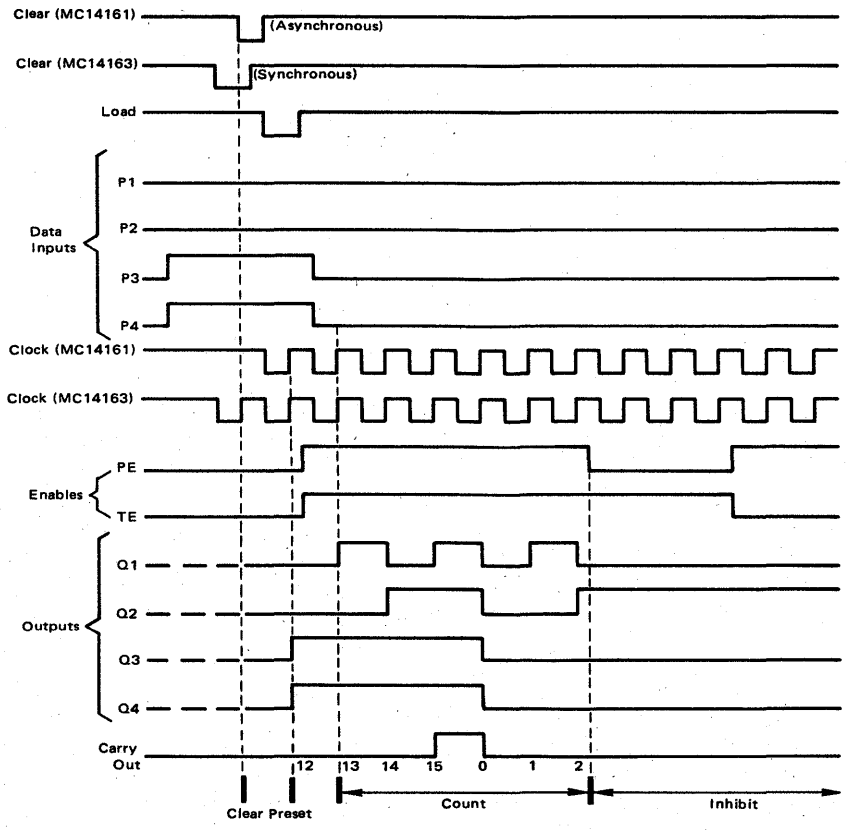


5

MC14161, MC14163 TIMING DIAGRAM

Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two,
4. Inhibit



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MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14174B

McMOS MSI

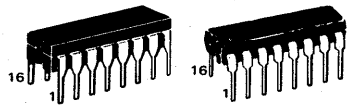
(LOW-POWER COMPLEMENTARY MOS)

HEX TYPE D FLIP-FLOP

HEX TYPE D FLIP-FLOP

The MC14174B hex type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data on the D inputs which meets the setup time requirements is transferred to the Q outputs on the positive edge of the clock pulse. All six flip-flops share common clock and reset inputs. The reset is active low, and independent of the clock.

- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Output Compatible with Two HTL Loads, Two Low-Power TTL Loads or One Low-Power Schottky TTL Load
- Functional Equivalent to TTL 74174



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

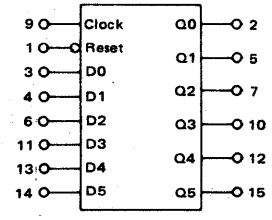
Rating *	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE
(Postive Logic)

INPUTS			OUTPUT	
Clock	Data	$\overline{\text{Reset}}$	Q	
↑	0	1	0	
↑	1	1	1	
↓	X	1	Q	No Change
X	X	0	0	

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.1 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.3 μA/kHz) f + I_{DD}							
		15	I_T = (3.7 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

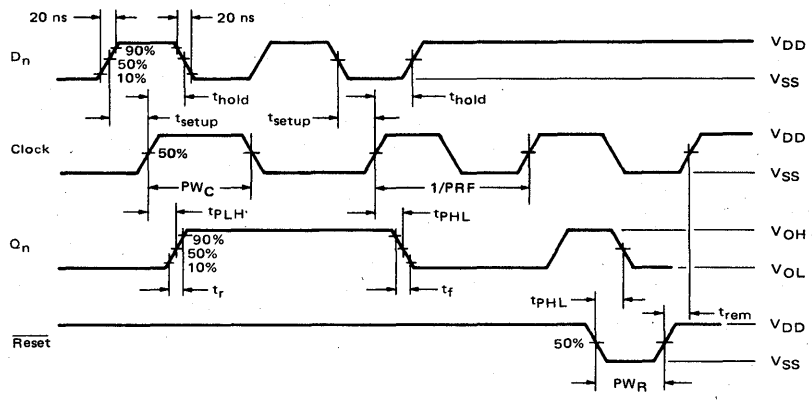
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Output Rise and Fall Time	t_r, t_f					ns
t_r, t_f = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_r, t_f = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_r, t_f = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time — Clock to Q	t_{PLH},					ns
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 165 ns	t_{PHL}	5.0	–	210	420	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 64 ns		10	–	85	170	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 52 ns		15	–	65	130	
Propagation Delay Time — $\overline{\text{Reset}}$ to Q	t_{PHL}					ns
t_{PHL} = (0.9 ns/pF) C_L + 205 ns		5.0	–	250	500	
t_{PHL} = (0.36 ns/pF) C_L + 79 ns		10	–	100	200	
t_{PHL} = (0.26 ns/pF) C_L + 62 ns		15	–	75	150	
Minimum Clock Pulse Width	PW_C	5.0	–	75	150	ns
		10	–	45	90	
		15	–	35	70	
Minimum $\overline{\text{Reset}}$ Pulse Width	PW_R	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Pulse Frequency	PRF	5.0	2.0	7.0	–	MHz
		10	5.0	12.0	–	
		15	6.5	15.5	–	
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
Data Setup Time	t_{setup}	5.0	–	20	40	ns
		10	–	10	20	
		15	–	0	15	
Data Hold Time	t_{hold}	5.0	–	40	80	ns
		10	–	20	40	
		15	–	15	30	
$\overline{\text{Reset}}$ Removal Time**	t_{rem}	5.0	–	125	250	ns
		10	–	50	100	
		15	–	40	80	

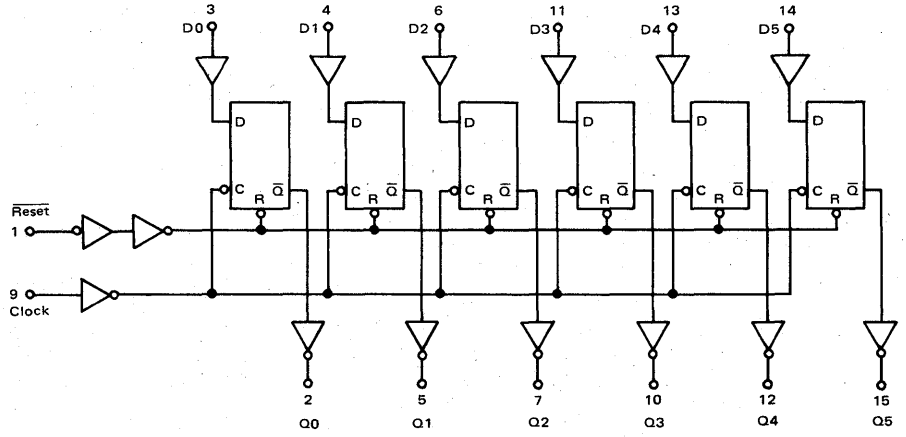
*The formulas given are for the typical characteristics only.
**The reset signal must be high prior to a positive-going transition of the clock.

5

TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14175B

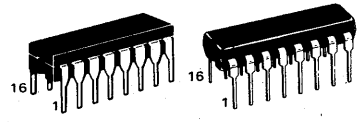
McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD TYPE D FLIP-FLOP

The MC14175B quad type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each of the four flip-flops is positive-edge triggered by a common clock input (C). An active-low reset input ($\overline{R}$) asynchronously resets all flip-flops. Each flip-flop has independent Data (D) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Complementary Outputs
- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Output Compatible with Two HTL Loads, Two Low-Power TTL Loads or One Low-Power Schottky TTL Load
- Functional Equivalent to TTL 74175



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

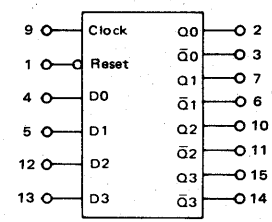
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE
(Postive Logic)

INPUTS			OUTPUTS		
Clock	Data	$\overline{Reset}$	Q	$\overline{Q}$	
↑	0	1	0	1	
↑	1	1	1	0	
↓	X	1	Q	$\overline{Q}$	No Change
X	X	0	0	1	

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.7 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.4 µA/kHz) f + I_{DD}							
		15	I_T = (5.0 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

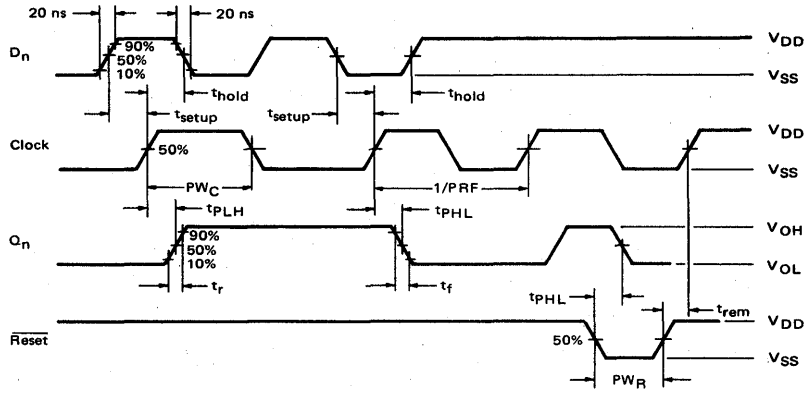
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise and Fall Time	t_r, t_f					ns
t_r, t_f = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_r, t_f = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_r, t_f = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time — Clock to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 175 ns		5.0	–	220	420	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 72 ns		10	–	90	170	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 57 ns		15	–	70	130	
Propagation Delay Time — $\overline{\text{Reset}}$ to Q	t_{PHL}					ns
t_{PHL} = (0.9 ns/pF) C_L + 280 ns		5.0	–	325	650	
t_{PHL} = (0.36 ns/pF) C_L + 112 ns		10	–	130	260	
t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	–	100	200	
Minimum Clock Width	PW_C	5.0	–	110	250	ns
		10	–	45	100	
		15	–	35	75	
Minimum $\overline{\text{Reset}}$ Pulse Width	PW_R	5.0	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
Maximum Clock Pulse Frequency	PRF	5.0	2.0	4.5	–	MHz
		10	5.0	11	–	
		15	6.5	14	–	
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
Data Setup Time	t_{setup}	5.0	–	60	120	ns
		10	–	25	50	
		15	–	20	40	
Data Hold Time	t_{hold}	5.0	–	40	80	ns
		10	–	20	40	
		15	–	15	30	
$\overline{\text{Reset}}$ Removal Time**	t_{rem}	5.0	–	125	250	ns
		10	–	50	100	
		15	–	40	80	

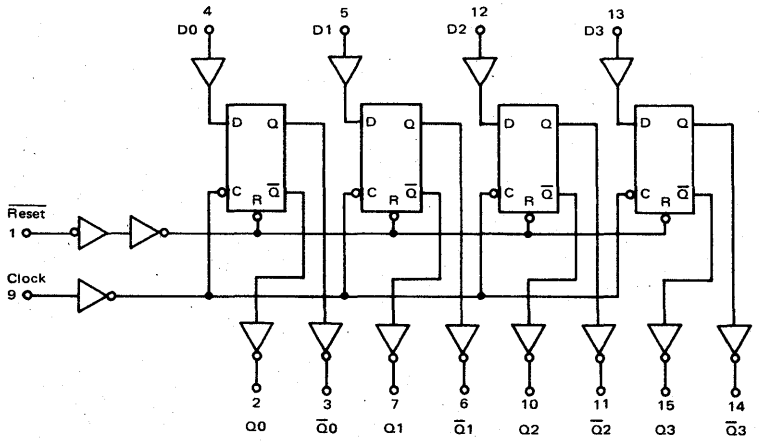
*The formulas given are for the typical characteristics only.
**The reset signal must be high prior to a positive-going transition of the clock.

5

TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



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MC14194B

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

The MC14194B is a 4-bit static shift register capable of operating in the parallel load, serial shift left, serial shift right, or hold mode. The asynchronous $\overline{\text{Reset}}$ input, when at a low level, overrides all other inputs, resets all stages, and forces all outputs low. When $\overline{\text{Reset}}$ is at a logic 1 level, the two mode control inputs, S0 and S1, control the operating mode as shown in the truth table. Both serial and parallel operation are triggered on the positive-going transition of the Clock input. The Parallel Data, Data Shift, and mode control inputs must be stable for the specified setup and hold times before and after the positive-going Clock transition.

- Quiescent Current = 5.0 nA typ/pkg @ 5 Vdc
- Typical Shift Frequency = 9.0 MHz @ 10 Vdc
- Synchronous Right/Left Serial Operation
- Synchronous Parallel Load
- Asynchronous Hold (Do Nothing) Mode
- Functional Pin for Pin Equivalent of 74194

TRUTH TABLE

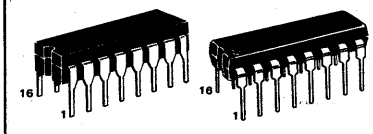
OPERATING MODE	INPUTS ($\overline{\text{Reset}}$ = 1)					OUTPUTS (@ $t_n + 1$)			
	S1	S0	DSR	DSL	D_{P0-3}	Q0	Q1	Q2	Q3
Hold	0	0	X	X	X	Q0	Q1	Q2	Q3
Shift Left	1	0	X	0	X	Q1	Q2	Q3	0
	1	0	X	1	X	Q1	Q2	Q3	1
Shift Right	0	1	0	X	X	0	Q0	Q1	Q2
	0	1	1	X	X	1	Q0	Q1	Q2
Parallel	1	1	X	X	0	0	0	0	0
	1	1	X	X	1	1	1	1	1

X = Don't Care
t_{n+1} = State after the next positive-going transition of the clock.

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER



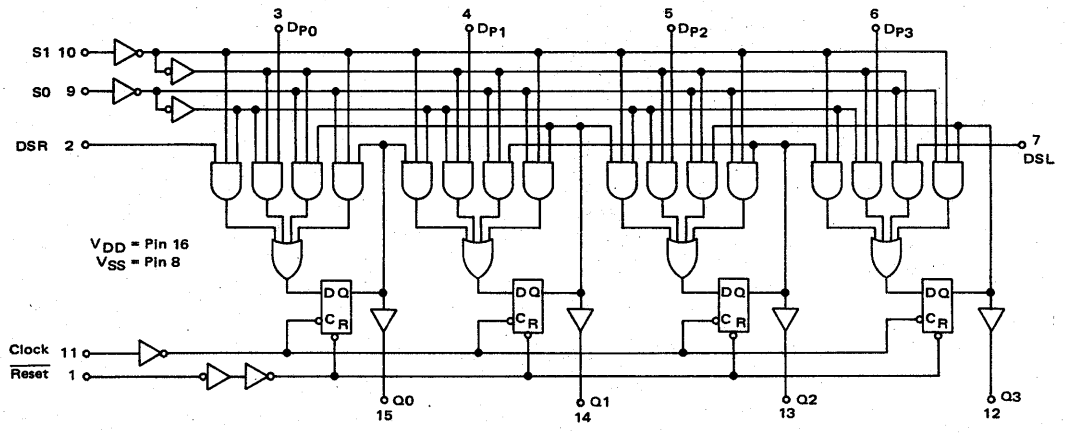
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

LOGIC DIAGRAM



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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.95\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (1.9\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (2.9\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Output Rise and Fall Time	t_r,t_f					ns
t_r,t_f = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_r,t_f = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_r,t_f = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},t_{PHL}					ns
Clock to Q						
t_{PLH},t_{PHL} = (0.9 ns/pF) C_L + 230 ns		5.0	–	275	550	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 92 ns		10	–	110	220	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 72 ns		15	–	85	170	
$\overline{\text{Reset}}$ to Q	t_{PHL}					ns
t_{PHL} = (0.9 ns/pF) C_L + 305 ns		5.0	–	350	700	
t_{PHL} = (0.36 ns/pF) C_L + 122 ns		10	–	140	280	
t_{PHL} = (0.26 ns/pF) C_L + 97 ns		15	–	110	220	
Minimum Clock Pulse Width	PW_C	5.0	–	140	280	ns
		10	–	55	110	
		15	–	40	85	
Minimum $\overline{\text{Reset}}$ Pulse Width	PW_R	5.0	–	90	180	ns
		10	–	35	70	
		15	–	26	50	
Maximum Clock Pulse Frequency	PRF	5.0	1.8	3.6	–	MHz
(Shift Right or Left Mode)		10	4.5	9.0	–	
		15	6.0	12	–	
Maximum Clock Pulse Rise and Fall Time	t_r,t_f	5.0	No Limit	–	–	μs
		10		–	–	
		15		–	–	
Setup Time	t_{setup}					ns
Data to Clock		5.0	–	-8.0	10	
		10	–	0	20	
		15	–	9.0	40	
Mode Control (S) to Clock		5.0	–	100	200	ns
		10	–	36	75	
		15	–	27	55	
Hold Time	t_{hold}					ns
Data to Clock		5.0	–	90	180	
		10	–	25	50	
		15	–	10	35	
Mode Control (S) to Clock		5.0	–	-40	0	ns
		10	–	-27	0	
		15	–	-20	0	
$\overline{\text{Reset}}$ Removal Time**	t_{rem}	5.0	–	150	300	ns
		10	–	55	110	
		15	–	40	80	

*The formulas given are for the typical characteristics only.
**The reset signal must be high prior to a positive-going transition of the clock.

FIGURE 1 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

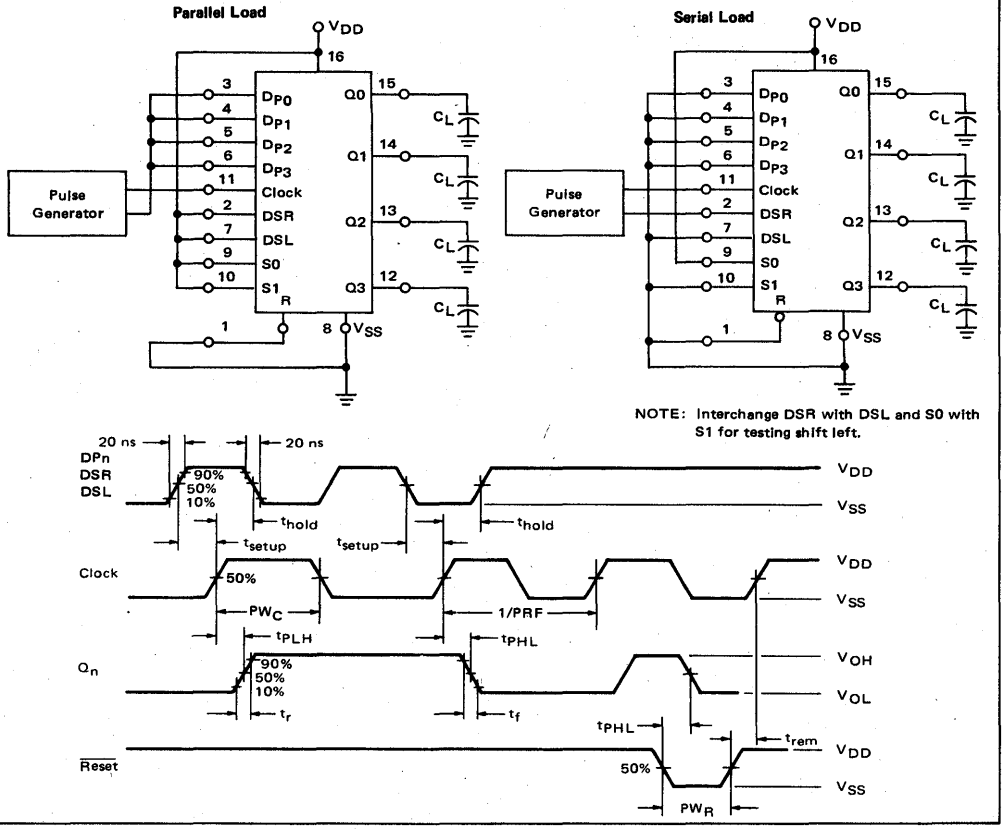
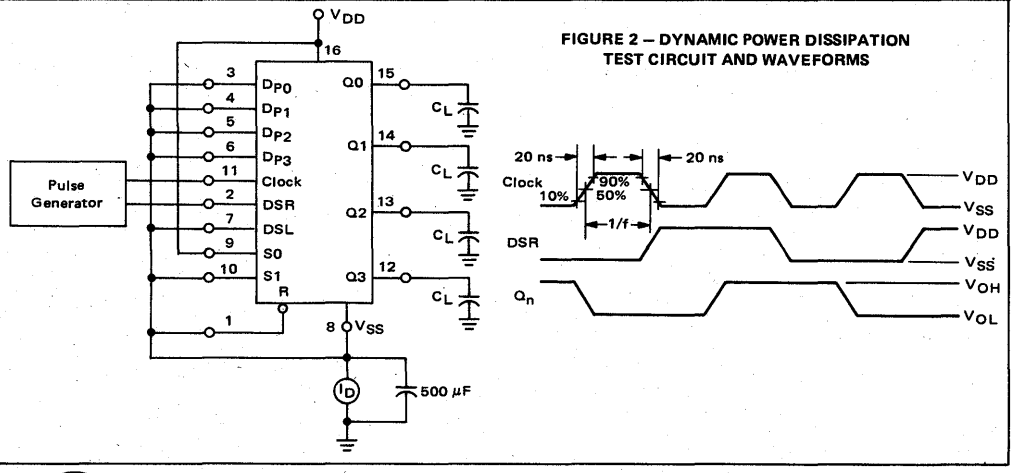


FIGURE 2 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



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MC14408
MC14409

Advance Information

BINARY TO PHONE PULSE CONVERTER SUBSYSTEM

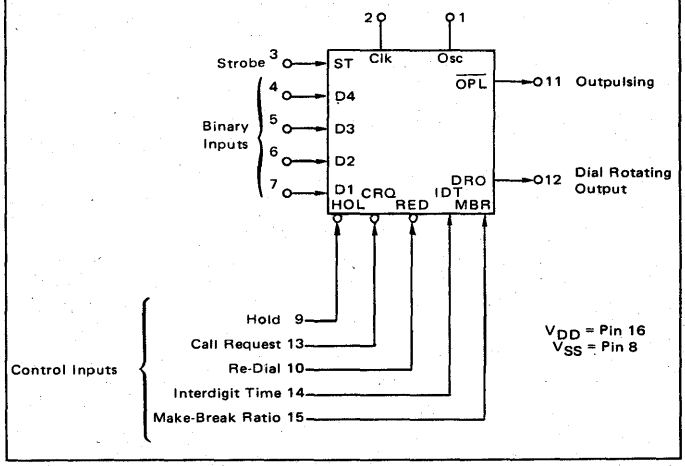
The MC14408 and the MC14409 are devices designed to convert a four bit binary input code to a number of serial output pulses corresponding to the value of the input code.

The devices can be used in telephone pulse dialing applications when combined with their companion device, the MC14419 (2-of-8 keypad-to-binary code converter). The devices have been partitioned to allow convenient addition of RAM memory and controls for repertoire dialing applications.

The MC14408 and MC14409 perform identical functions with the exception of the signal output at the DRO (Dial Rotating Output). In the MC14408, DRO remains high during continuous outpulsing of all digits and in the MC14409 DRO is low between each digit pulse burst.

- On-Chip Oscillator
- Diode Protection on All Inputs
- Dialing of Numbers Up to 16 Digits Long
- Memory Storage (FIFO) and Re-Dialing (single pin) of Last Telephone Number
- Hold Interrupt Control for Additional Interdigit Delays (such as a Wait for Intermediate Dial Tones)
- Selectable Dialing Rate (10 pps or 20 pps)
- Selectable Interdigit Time (300 or 800 ms @ 10 pps; 150 or 400 ms @ 20 pps)
- Selectable Make-Break Ratio (61% or 67%)
- Buffered Outputs Compatible with Discrete Transistor Driver Interface, One Low-power Schottky TTL Load or Two Low-power TTL Loads Over the Rated Temperature Range.
- Low Power Dissipation – I_{DD} (operating with oscillator) = 470 μA typ @ V_{DD} = 5.0 Vdc, f_{Osc} = 16 kHz, C_L = 50 pF

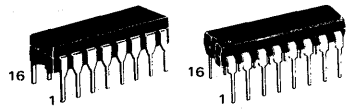
BLOCK DIAGRAM



McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

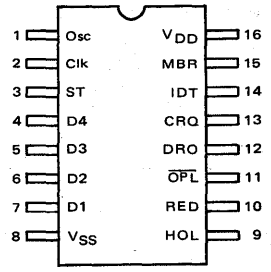
BINARY TO PHONE PULSE CONVERTER SUBSYSTEM



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.0	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	3.0	6.0	3.0	5.0	6.0	3.0	6.0	Vdc
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Noise Immunity										
($\Delta V_{out} \leq 0.5$ Vdc)	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	Vdc
($\Delta V_{out} \leq 0.5$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.80	-1.7	–	-0.60	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.20	–	-0.16	-0.36	–	-0.12	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
Input Current	I_{in}	6.0	–	–	–	±0.00001	±0.30	–	1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	12	–	5.0	12	–	12	pF
Operating Supply Current	I_{DD}	3	–	250	–	160	200	–	200	μAdc
f_{Clk} = 16 kHz (operating with Osc)		5	–	700	–	470	550	–	550	
		6	–	1250	–	740	1000	–	1000	

5

FIGURE 1 – TIMING DIAGRAM – DATA AND STROBE INPUTS

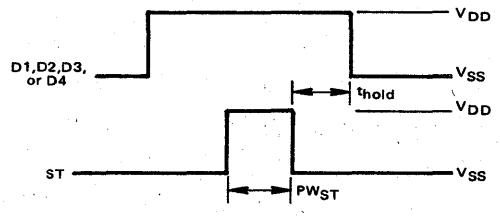
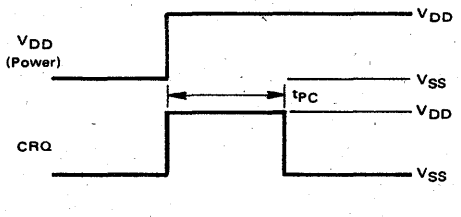


FIGURE 2 – TIMING DIAGRAM – CALL REQUEST



If power is turned off after each call, CRQ must stay high after power is applied (for a duration of t_{PC}) to ensure no spurious outpulsing. For this use the redial function is invalid.

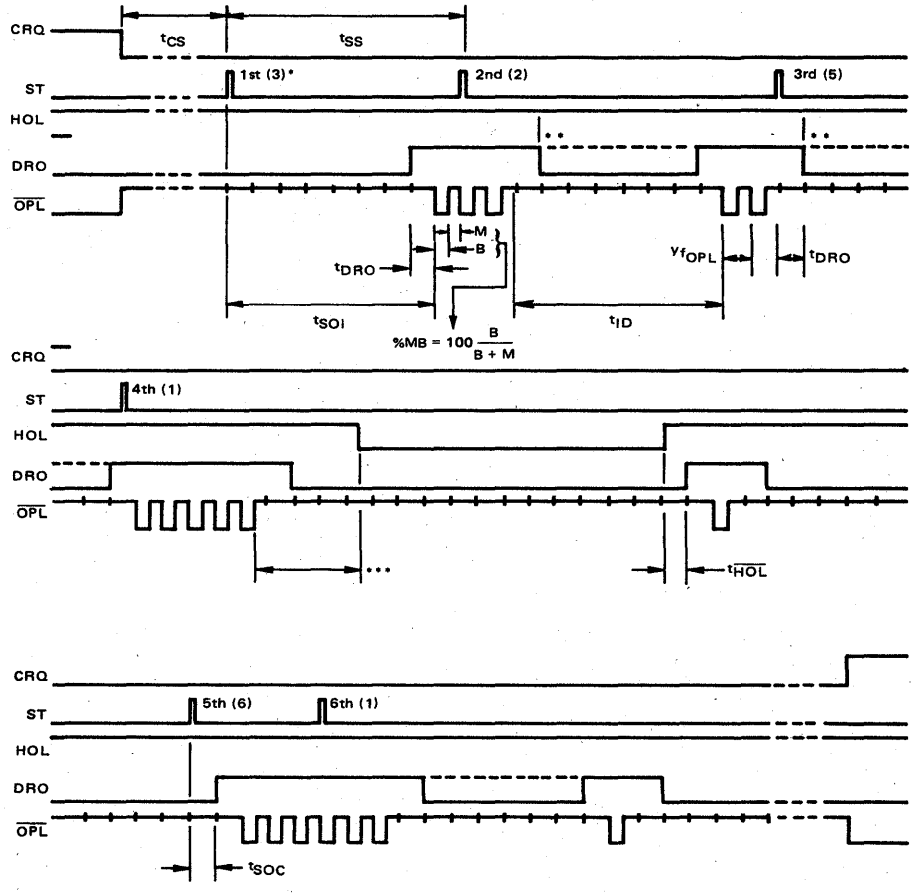
SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time** t_r = (3.0 ns/pF) C_L + 30 ns	t_r	5.0	–	180	400	ns
Output Fall Time** t_f = (1.5 ns/pF) C_L + 25 ns	t_f	5.0	–	100	200	ns
Power Up to Call Request Pause	t_{PC}	3 to 6	48/f_{Clk}*	–	–	ms
Call Request to First Strobe Pulse	t_{CS}	3 to 6	48/f_{Clk}*	–	–	ms
Strobe to Strobe Separation Time	t_{SS}	3 to 6	48/f_{Clk}*	–	–	ms
Strobe Pulse Width	PW_{ST}	3 to 6	1.0	–	–	µs
Strobe to Data Hold Time	t_{hold}	3 to 5	–	150	400	ns
Clock Frequency	f_{Clk}	3 to 6	12.5	16	100	kHz
Percent Break to Make Ratio	%MB	3 to 6				%
(MBR = 0)			–	61	–	
(MBR = 1)			–	67	–	
Outpulsing Rate (f_{OPL} = *f_{Clk}/1.6)	f_{OPL}	3 to 6				pps
f_{Clk} = 16 kHz			–	10	–	
f_{Clk} = 32 kHz			–	20	–	
Interdigit Time	t_{ID}	3 to 6				ms
t_{ID} = (5 x IDT + 3)/f_{OPL}						
IDT = 0						
f_{OPL} = 10 pps			–	300	–	
f_{OPL} = 20 pps			–	150	–	
IDT = 1						
f_{OPL} = 10 pps			–	800	–	
f_{OPL} = 20 pps			–	400	–	
Strobe to Output Time	t_{SOI}	3 to 6				ms
Initial Outpulsing Stream						
IDT = 0						
f_{OPL} = 10 pps			300	–	400	
f_{OPL} = 20 pps			150	–	200	
IDT = 1						
f_{OPL} = 10 pps			800	–	900	
f_{OPL} = 20 pps			400	–	450	
Continued Outpulsing Stream	t_{SOC}	3 to 6				ms
IDT = 0 or 1						
f_{OPL} = 10 pps			100	–	200	
f_{OPL} = 20 pps			50	–	100	
Hold to Outpulse Time	t_{HOL}	3 to 6				ms
IDT = 0 or 1						
f_{OPL} = 10 pps			100	–	200	
f_{OPL} = 20 pps			50	–	100	
Dial Rotating Overlap Time	t_{DR}	3 to 6				ms
f_{OPL} = 10 pps			–	100	–	
f_{OPL} = 20 pps			–	50	–	

*f_{Clk} in kHz
**The formula given is for the typical characteristics only.

5

FIGURE 3 – PHONE DIALER SYSTEM TIMING DIAGRAM



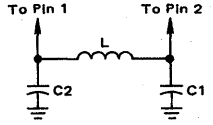
Notes:

(*)1st, 2nd, 3rd, etc., denotes Strobe pulse sequence – i.e., which digit in the phone number is being dialed. The number in parentheses denotes the numerical value of the digit being dialed. The examples define the various voltage – level and timing requirements, not a complete phone number.

(**)For the MC14408 the DRO signal will remain high provided digits remain in the memory, or a digit for continuing outpulsing is strobed in before the anticipated falling edge of the most significant digit in the memory. (i.e., [200-% MB] ms after the most significant outpulsing edge).

(***)For the HOL signal to hold a next digit (e.g. the 4th, etc.,) the HOL falling edge must not appear after [t_{ID}-%MB + 100] ms the last outpulsing edge of the previous digit.

FIGURE 4 – COMPONENT SELECTION FOR OSCILLATOR/CLOCK FREQUENCY



$$f_{Clk} = \frac{7.118}{\sqrt{LC}}$$ where f_{Clk} in kHz, L in mH, C = C1 = C2 in μF

$\%f_{Clk} = -0.5\,[\%C + \%L] \pm 3.0$ where $\%f_{Clk}$, %C, %L are the frequency capacitor, and inductor tolerances in percent. The ±3.0% accounts for supply voltage and ambient temperature variations.

EXAMPLE

L	%L	C=C1=C2	%C	f_{Clk}	$\%f_{Clk}$	OUTPULSING RATE $f_{OPL} = f_{Clk}/1.6$
5.0 mH	±5.0	0.04 μF	±5.0	≈16 kHz	±8.0	≈10 pps
5.0 mH	±5.0	0.01 μF	±5.0	≈32 kHz	±8.0	≈20 pps

FIGURE 5 – TRUTH TABLE

INPUTS						OUTPUTS	
$\overline{CRQ}$	D4 D3 D2 D1	ST	$\overline{RED}$	$\overline{HOL}$	IDT	MBR	$\overline{OPL}$	DRO †
1	X X X X	X	X	X	X	X	0	0
0	X X X X	0	1	1	X	X	1 (Steady State)	0 (Steady State)
0	X X X X (nth Digit)	⊓	1	1	X	X	Number of pulses (1,f) of nth digit = binary combination of D4, D3, D2, D1. *	1 During outpulsing 0 Otherwise
0	X X X X	0	⊓	1	X	X	Digits of number in memory re-sent.	1 During outpulsing 0 Otherwise
0	X X X X	X	1	0	X	X	1 { After conclusion of digit being outpulsed.	0 { After conclusion of digit being outpulsed
X	X X X X	X	X	X	0 1	X	300 ms Interdigit time 800 ms Interdigit time } f_{Clk} = 16 kHz	
X	X X X X	X	X	X	X	0 1	61% (≈1.6:1) Make-Break Ratio 67% (≈2:1) Make-Break Ratio	

X = Don't Care

* With the exception of 0000 which will give 10 pulses.

† Refer to timing diagram Figure 3.

DEVICE OPERATION

OSCILLATOR (Osc, Pin 1)

This pin is an input to the internal oscillator and feedback connection for the L-C π-network. An external clock signal, if desired can be applied to Osc.

CLOCK (Clk, Pin 2)

This pin is an output from the internal oscillator and feedback connection for the L-C π-network and provides the system clock for the MC14419 bounce eliminator circuitry.

STROBE INPUT (ST, Pin 3)

This Strobe input, when high (ST = V_{DD}), signifies that the data at the D1, D2, D3, and D4 inputs is valid, and enters the 4-bit number into the internal FIFO (First-In, First-Out) memory for subsequent outpulsing. The first strobe pulse after a call is requested (CRQ = low) clears the memory of any previous number and enters the first digit of the new number. Successive strobe pulses will store up to a maximum of 16 digits in the internal FIFO memory, which ignores all digits entered in excess of that amount until a new call is requested.

DATA INPUTS (D4, D3, D2, D1, Pins 4, 5, 6, 7)

These pins are the Data inputs to the internal memory. A binary coded digit number entered will result in an equivalent number of pulses at the $\overline{OPL}$ (outpulsing) output, except for the code 0000, which will outpulse 10 pulses.

NEGATIVE POWER SUPPLY (V_{SS}, Pin 8)

This pin is the negative power supply connection. Normally this pin is system ground.

HOLD (HOL, Pin 9)

When taken low (HOL = V_{SS}), the Hold input disables the outpulsing at the completion of the digit being outpulsed. When taken high, outpulsing resumes. This feature can be used in multi-dial-tone phone systems to provide longer interdigit pauses when necessary.

RE-DIAL (RED, Pin 10)

The Re-Dial input, when taken low (RED = V_{SS}) automatically outpulses the digits entered into memory after the last time a call was requested.

OUTPULSING ($\overline{OPL}$, Pin 11)

The Outpulsing output sends out bursts of pulses equivalent to the digits of the telephone number stored in the memory. The duty cycle and interdigit time of the digit pulse bursts are controlled, respectively by the MBR (Pin 16) and IDT (Pin 14).

DIAL ROTATING OUTPUT (DRO, Pin 12)

The Dial Rotating (also known as "Off Normal") Output provides a signal which indicates that digit pulse bursts are being sent. In the MC14409, DRO goes high (V_{DD}) at the beginning of the first digit pulse burst and goes low (V_{SS}) between succeeding consecutive digit pulse bursts. In the MC14408, however, DRO goes high at the beginning of the first digit pulse burst and remains high until the last digit pulse burst of the telephone number has been sent (see Timing Diagram, Figure 3).

CALL REQUEST (CRQ, Pin 13)

The Call Request input when taken low (CRQ = V_{SS}) resets internal counters and prepares the internal logic to either accept new digit inputs to be dialed, or to re-dial (see RED, Pin 10) the digits stored in the memory.

INTERDIGIT TIME (IDT, Pin 14)

The Interdigit Timing input determines the length of time between consecutive digit pulse bursts. See the Interdigit Time (t_{ID}) in the switching characteristics for the length of time.

MAKE-BREAK RATIO (MBR, Pin 15)

The Make-to-Break Ratio input controls the duty cycle of the digit pulse bursts at the $\overline{OPL}$ output. For MBR = V_{DD}, duty cycle = 67% low, 33% high; and for MBR = V_{SS}, duty cycle = 61% low, 39% high.

POSITIVE POWER SUPPLY (V_{DD}, Pin 16)

This pin is the package positive power supply pin.

FIGURE 6– KEYPAD TO PULSE DIALER FLOW DIAGRAM

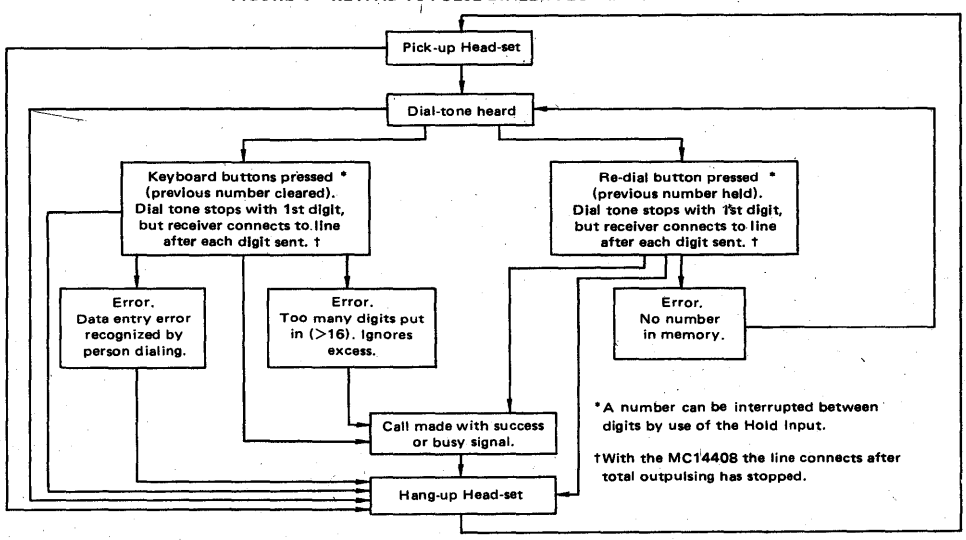


FIGURE 7– PHONE DIALER SYSTEM

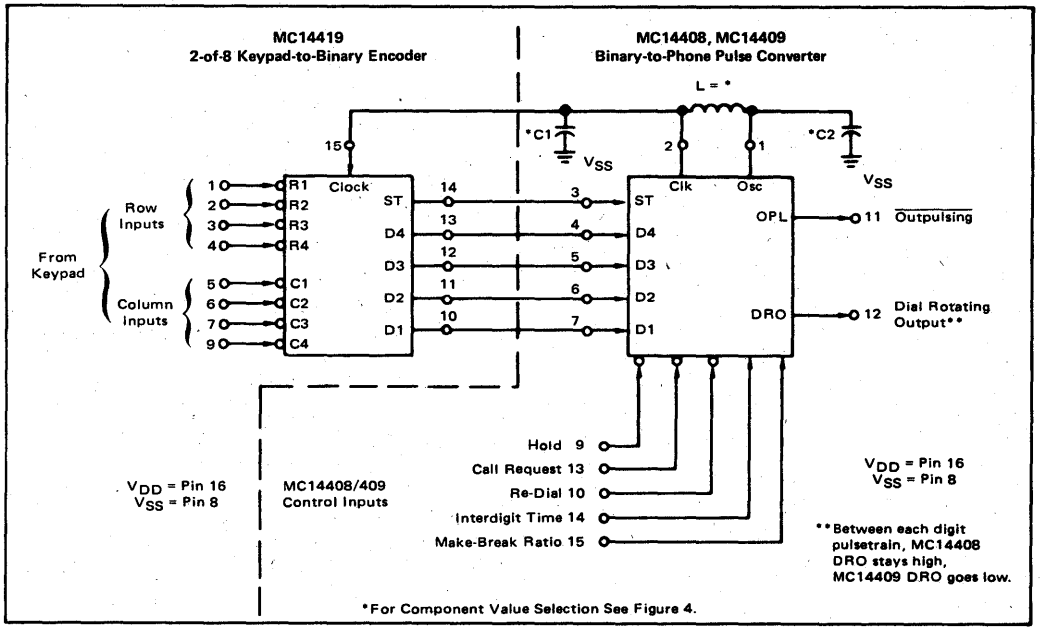


FIGURE 8 – STANDARD K-500 TELEPHONE

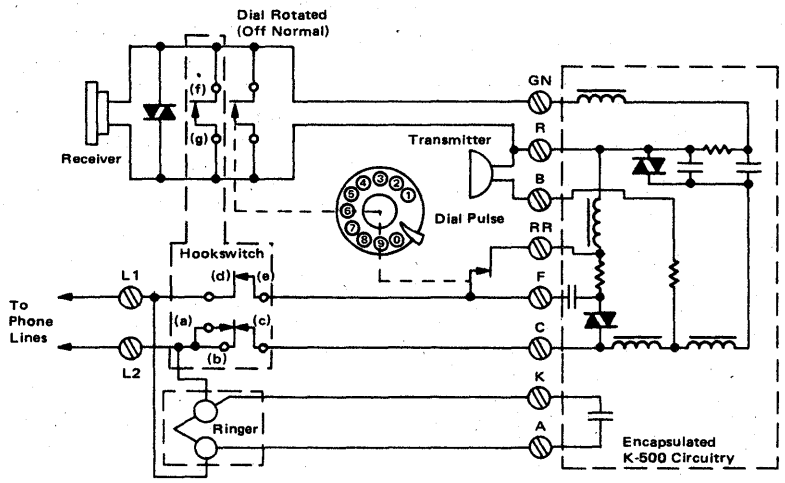
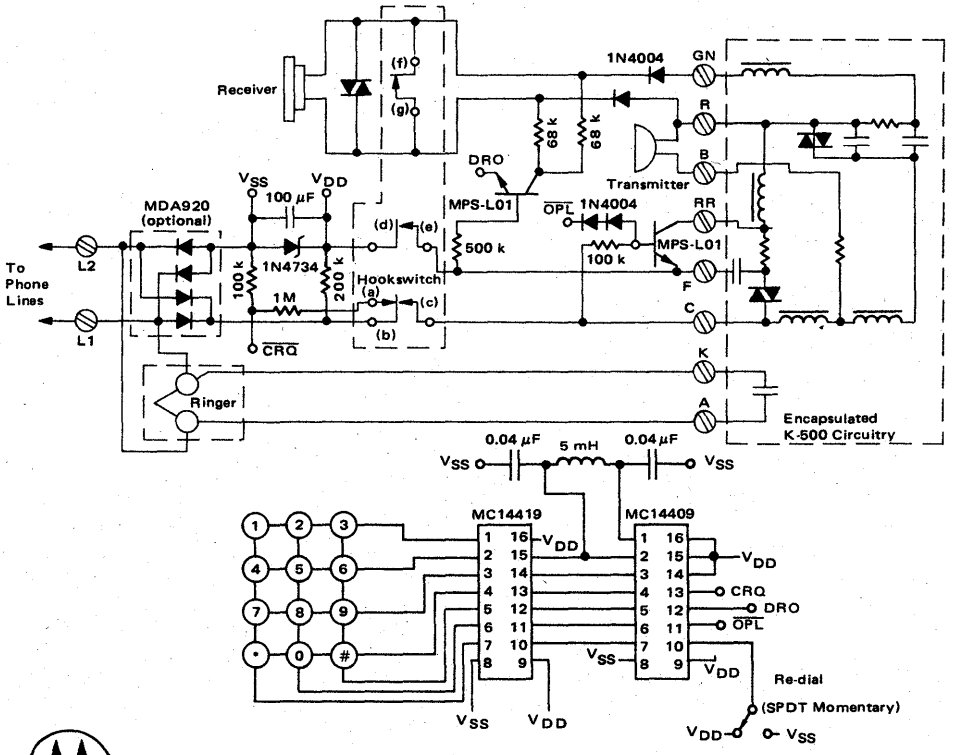


FIGURE 9 – MODIFIED K-500 TELEPHONE



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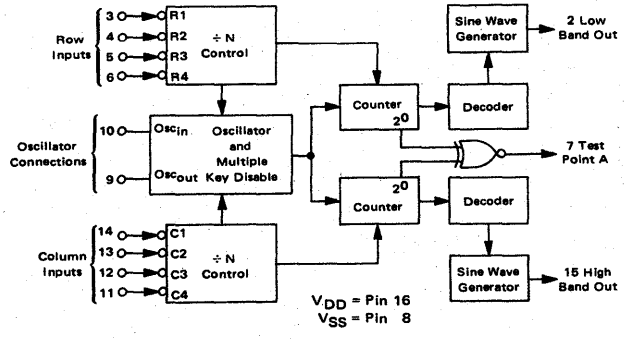
MC14410

2-OF-8 TONE ENCODER

The MC14410 2-of-8 tone encoder is constructed with complementary MOS enhancement mode devices. It is designed to accept digital inputs in a 2-of-8 code format and to digitally synthesize the high and low band sine waves specified by telephone tone dialing systems. The inputs are normally originated from a 4 x 4 matrix keypad, which generates 4 row and 4 column input signals in a 2-of-8 code format (1 row and 1 column are simultaneously connected to V_{SS}). The master clocking for the MC14410 is achieved from a crystal controlled oscillator which is included on the chip. Internal clocks, which operate the logic, are enabled only by one or more row and column signals being activated simultaneously. The two sine wave outputs have NPN bipolar structures on the same substrate which allows for low output impedance and large source currents. Applications of this device include telephone tone dialing, radio and mobile telephones, process control, point-of-sale terminals, and credit card verification terminals.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Supply Voltage Range = 4.4 Vdc to 6.0 Vdc
- On-Chip Oscillator (Crystal or External Clock Source may be applied to Pin 10)
- On-Chip Pull-Up Resistors on Row and Column Inputs
- Designed with Multiple Key Lockout (Eliminates Need for Mechanical Lockout in Keypad)
- Two Sine Wave Generators On-Chip
- Frequency Accuracy ±0.2%
- Low Harmonic Distortion
- Single Tone Capability
- Fast Oscillator Turn-On and Turn-Off Times

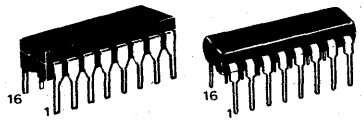
BLOCK DIAGRAM



McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

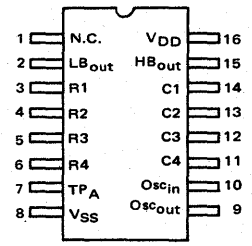
2-OF-8 TONE ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} (V_{in}$ or $V_{out}) \leq V_{DD}$.
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a peak sinewave voltage.

5

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.0	Vdc
Input Voltage, All Inputs	V_{in}	V_{SS} -0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	4.4	6.0	4.4	5.0	6.0	4.4	6.0	Vdc
Output Voltage "0" Level Pins 7 and 9	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) "0" Level	V_{IL}	5.0	1.5	–	1.5	2.25	–	1.5	–	Vdc
(V_O = 0.5 or 4.5 Vdc) "1" Level	V_{IH}	5.0	1.5	–	1.5	2.25	–	1.5	–	Vdc
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source Pin 7		5.0	-0.05	–	-0.05	-0.4	–	-0.04	–	
Pin 9			-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}									mAdc
Pin 7		5.0	0.05	–	0.05	0.20	–	0.04	–	
Pin 9			0.23	–	0.20	0.78	–	0.16	–	
Input Pull-Up Resistor Source Current (V_{in} = 0 Vdc) Pins 3-6, 11-14	I_{IL}	6.0	–	140	–	30	100	–	80	μAdc
Input Capacitance (V_{in} = 0 Vdc)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Current	I_Q									mAdc
		4.4	–	0.48	–	0.2	0.4	–	0.33	
		6.0	–	1.3	–	0.55	1.1	–	0.9	
Total Supply Current (Dynamic plus Quiescent)	I_T									mAdc
(R_L = 15 kΩ, f = 1 MHz)		4.4	–	1.7	–	0.7	1.4	–	1.15	
		6.0	–	3.5	–	1.45	2.9	–	2.4	
Low Band Output Voltage Swing Pin 2 Only	V_{Lpp}									mVpp
		4.4	400	600	500	600	700	550	750	
		6.0	800	1000	900	1000	1100	950	1150	
High Band Output Voltage Swing Pin 15 Only	V_{Hpp}									mVpp
		4.4	600	900	700	850	1000	800	1100	
		6.0	1100	1400	1200	1350	1500	1300	1600	
Low Band–High Band Voltage Differential	ΔV	5.0	–	–	–	2.5	–	–	–	dB
Low Band–High Band Pin 2,15 Output Impedance	z_o	–	–	–	–	80	–	–	–	Ω
Low Band–High Band Pin 2,15 2nd thru 14th Harmonics (R_L = 15 kΩ)	V_{2H}-V_{14H}	4.4 to 6.0	–	-20	–	-30	-25	–	-25	dB
Maximum Clock Pulse Frequency	PRF	4.4	–	–	–	1.0	–	1.1	–	MHz
Turn-on Time (Power on to oscillation)	t_{on}	5.0	–	–	–	8.0	–	–	–	ms

TABLE 1 – FUNCTIONAL TRUTH TABLE

ACTIVE LOW INPUTS		OUTPUTS	
Activated Row Lines	Activated Column Lines	Low Band Pin 2	High Band Pin 15
None	X**	dc level	dc level
X**	None	dc level	dc level
One	One	f_L*	f_H*
Two or more	One	dc level	f_H*
One	Two or more	f_L*	dc level
Two or more	Two or more	dc level	dc level

*See Table 2
**X = Don't care

TABLE 2 – OUTPUT FREQUENCY TABLE

Input Line Activated (low)	Frequency Generated**	
	f_L (Hz)	f_H (Hz)
R1	697	–
R2	770	–
R3	852	–
R4	941	–
C1	–	1209
C2	–	1336
C3	–	1477
C4	–	1633

**All frequencies are accurate to ±0.2% (crystal tolerance not included).

FIGURE 1 – TYPICAL SINE WAVE OUTPUT
(Pins 2 or 15, No External Filtering)

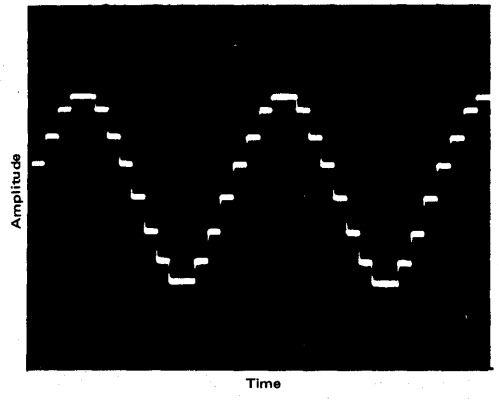


FIGURE 2 – TYPICAL FREQUENCY SPECTRUM
(Pins 2 or 15, No External Filtering)

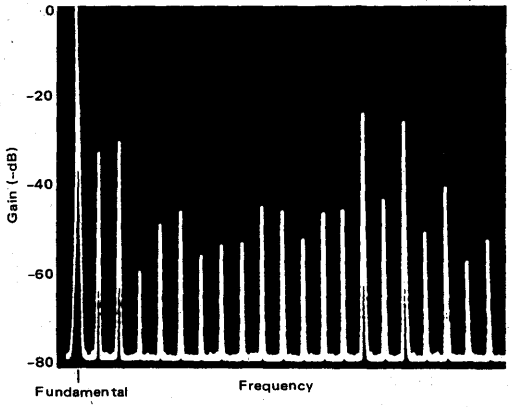


FIGURE 3 – TYPICAL CRYSTAL CIRCUIT

R_f = 15 MΩ ± 10%

CRYSTAL SPECIFICATION

Crystal Mode	Parallel
Frequency	1 MHz ± 0.1%
R_S	540Ω typ
C_0	7.0 pF typ
Temperature Range	-40°C to +85°C
Test Level	1 mW
Test Set	TS–330/TSM or Equivalent

*Suggested Suppliers: Tyco, CTS Knight and Motorola Crystal Products.

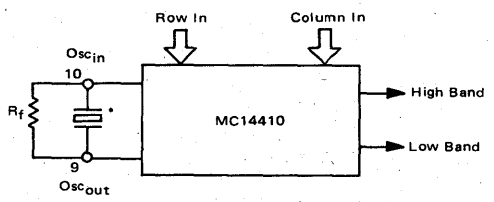


FIGURE 4 – TYPICAL TELEPHONE INTERFACE APPLICATION

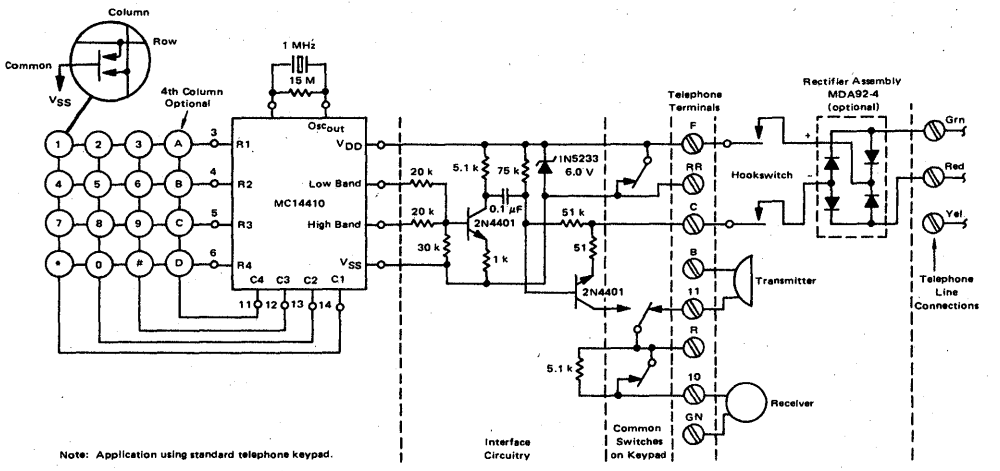


FIGURE 5 – LOW LEVEL OUTPUT TONE GENERATOR APPLICATION

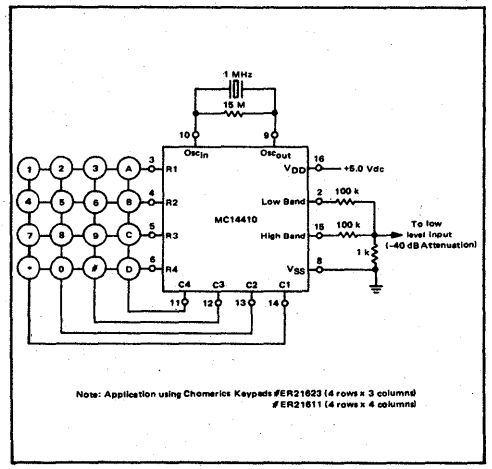
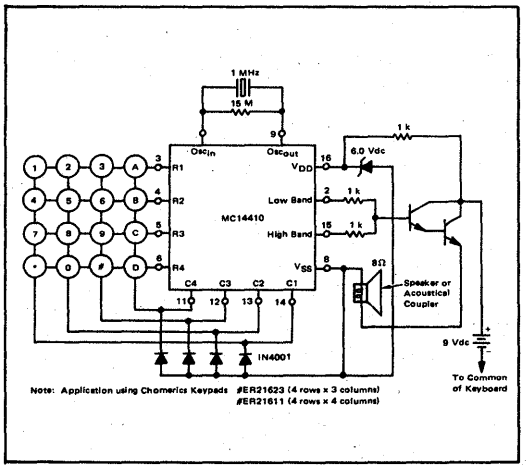


FIGURE 6 – BATTERY POWERED OPERATION (Driving Audio Speaker)



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MC14411

BIT RATE GENERATOR

The MC14411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

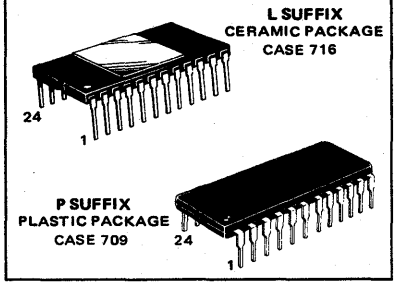
Applications include a selectable frequency source for equipment in the data communications market, such as teleprinters, printers, CRT terminals, and microprocessor systems.

- Single 5.0 Vdc (± 5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (1.8432 MHz)
- Sixteen Different Output Clock Rates
- 50% Output Duty Cycle
- Programmable Time Bases for One of Four Multiple Output Rates
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- External Clock May be Applied to Pin 21

McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

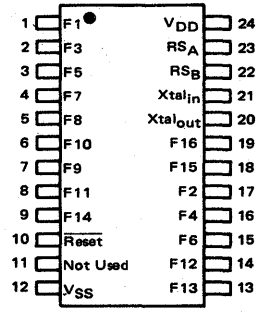
BIT RATE GENERATOR



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12.)

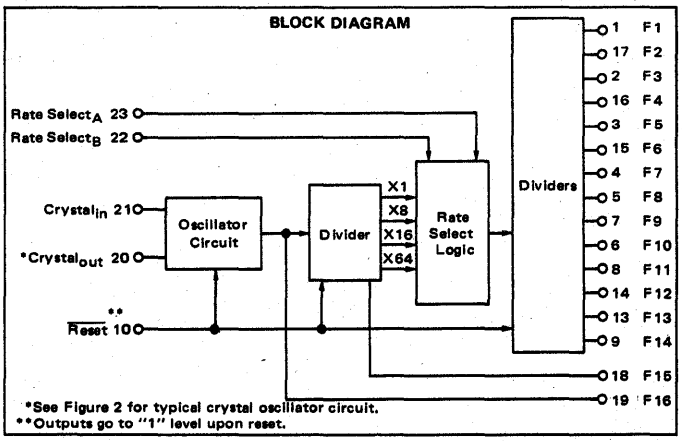
Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	5.25 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN ASSIGNMENT



V_{DD} = Pin 24
V_{SS} = Pin 12

BLOCK DIAGRAM



*See Figure 2 for typical crystal oscillator circuit.
**Outputs go to "1" level upon reset.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage		V_{DD}	–	4.75	5.25	4.75	5.0	5.25	4.75	5.25	Vdc
Output Voltage	"0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
	"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc)	"0" Level	V_{IL}	5.0	1.5	–	1.5	2.25	–	1.5	–	Vdc
(V_O = 0.5 or 4.5 Vdc)	"1" Level	V_{IH}	5.0	1.5	–	1.5	2.25	–	1.5	–	Vdc
Output Drive Current		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
Input Current		I_{in}	–	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation		P_Q	5.0	–	2.5	–	0.015	2.5	–	15	mW
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)		P_D	5.0	(P_D = (7.5 mW/MHz) f + P_Q							mW
Output Rise Time** t_r = (3.0 ns/pF) C_L + 25 ns		t_r	5.0	–	–	–	70	200	–	–	ns
Output Fall Time** t_f = (1.5 ns/pF) C_L + 47 ns		t_f	5.0	–	–	–	70	200	–	–	ns
Maximum Input Clock Frequency		f_{max}	5.0	–	–	–	1.8432	–	1.85	–	MHz

† For dissipation at different external load capacitance (C_L) refer to corresponding formula:

$P_T(C_L) = P_D + 2.6 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$

where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

**The formula given is for the typical characteristics only.

5

TABLE 1 – OUTPUT CLOCK RATES

Rate Select B	Rate Select A	Rate
0	0	X1
0	1	X8
1	0	X16
1	1	X64

Output Number	Output Rates (Hz) X64	X16	X8	X1
F1	614.4 k	153.6 k	76.8 k	9600
F2	460.8 k	115.2 k	57.6 k	7200
F3	307.2 k	76.8 k	38.4 k	4800
F4	230.4 k	57.6 k	28.8 k	3600
F5	153.6 k	38.4 k	19.2 k	2400
F6	115.2 k	28.8 k	14.4 k	1800
F7	76.8 k	19.2 k	9600	1200
F8	38.4 k	9600	4800	600
F9	19.2 k	4800	2400	300
F10	12.8 k	3200	1600	200
F11	9600	2400	1200	150
F12	8613.2	2153.3	1076.6	134.5
F13	7035.5	1758.8	879.4	109.9
F14	4800	1200	600	75
F15	921.6 k	921.6 k	921.6 k	921.6 k
F16*	1.843M	1.843M	1.843M	1.843M

*F16 is buffered oscillator output.

FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS

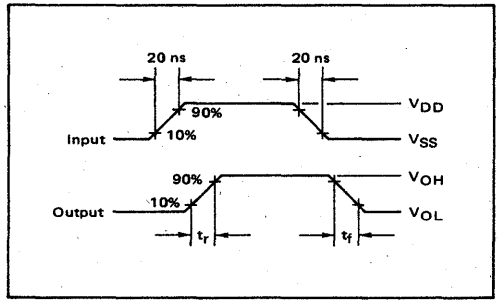
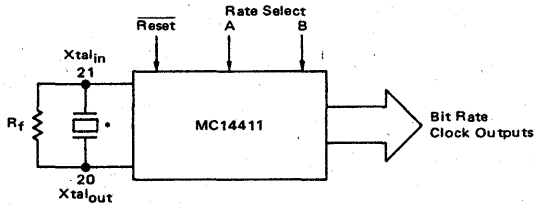


FIGURE 2 – TYPICAL CRYSTAL OSCILLATOR CIRCUIT



R_f = 15 MΩ±10%

CRYSTAL SPECIFICATION

Crystal Mode	Parallel
Frequency	1.8432 MHz ±0.05% @ 13 pF
R_S	540 Ω max
C_0	7.0 pF max
Temperature Range	0 to 70°C
Test Level	1 mW
Test Set	TS – 330/TSM or Equivalent

*Suggested Crystal Suppliers: Tyco, CTS Knight and Motorola Crystal Products.

APPLICATIONS INFORMATION

Typical applications of the Bit Rate Generator (BRG) include providing standard clock frequencies for data communications equipment, and external synchronization of a BRG output to a data source. The synchronization is accomplished by releasing the $\overline{\text{Reset}}$ input of the BRG during a data transition of the data source.

A typical data communication system is shown in Figure 3. In this example a standard frequency from the BRG is used for the clock input to the terminal transmitter and receiver (MC2257, MC2259). In a similar system the BRG, via Rate Select inputs, can provide up to 64 standard data communications frequencies for a multiple frequency system. Some examples of equipment frequency requirements are shown in Table 2.

FIGURE 3 – TYPICAL DATA COMMUNICATION TERMINAL BLOCK DIAGRAM

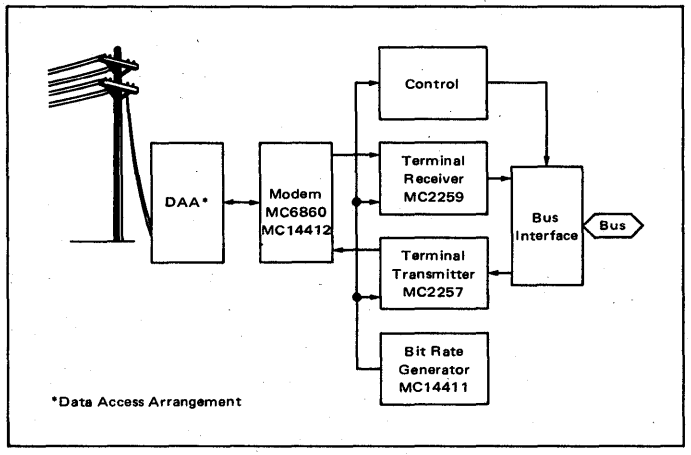


TABLE 2 – TYPICAL DATA COMMUNICATION EQUIPMENT BIT RATE FREQUENCIES

Frequency (Hz)	Use
75 110 134.49 150 200 300	Asynchronous Mode Teleprinters Printers, typewriters CRT Terminals etc.
600 1200	Asynchronous Mode (high speed) Printers CRT Terminals (i.e., Credit Card Verification, Personal Bank Checks, etc.)
2400 3600 4800 7200 9600	Synchronous Mode Such as Communication from Computer to Computer or Computer to Peripheral

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MC14412

McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

UNIVERSAL LOW SPEED (0-600 bps) MODEM

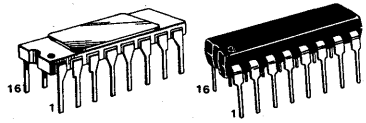
UNIVERSAL LOW SPEED MODEM (0–600 bps)

The MC14412 contains a complete FSK (Frequency-Shift Keying) modulator and demodulator compatible with both foreign (C.C.I.T.T. standards) and U.S.A. low speed (0 to 600 (bps) communication networks.

- On Chip Crystal Oscillator
- Echo Suppressor Disable Tone Generator
- Originate and Answer Modes
- Simplex, Half-Duplex, and Full Duplex Operation
- On Chip Sine Wave Generator
- Modem Self Test Mode
- Single Supply: V_{DD} = 4.75 to 15 Vdc FL, FP Suffix
  V_{DD} = 4.75 to 6.0 Vdc VL, VP Suffix
- Selectable Data Rates: 0-200, 0-300, 0-600 bps
- Post Detection Filter
- TTL or CMOS Compatible Inputs and Outputs

TYPICAL APPLICATIONS:

- Stand Alone Low-Speed Modems
- Built-In Low Speed Modems
- Remote Terminals, Acoustical Couplers
- Credit Verification
- Point of Sale
- Remote Data Collection
- Remote Process Control
- Radio Data Transmission



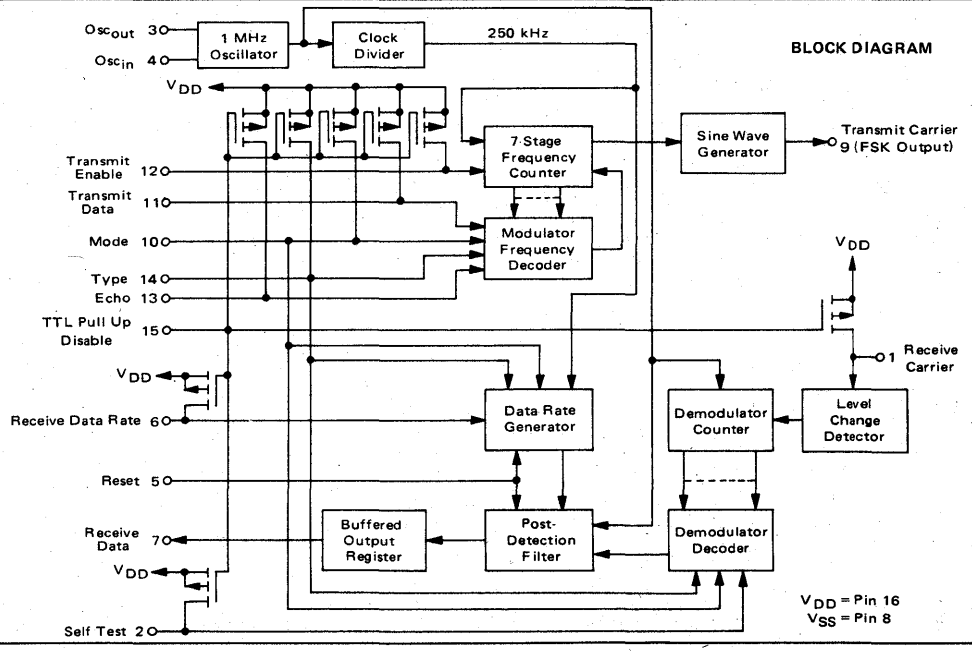
L SUFFIX
CERAMIC PACKAGE
CASE 690

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC144XX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- F Extended Operating Temperature Range
- V Limited Operating Temperature Range

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltages MC14412F MC14412V	V_{DD}	-0.5 to 15 -0.5 to 6.0	Vdc
Input Voltages, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin (except Pin 8, 7)	I	10	mAdc
DC Current Drain (Pin 8, 7)	I	35	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}** Vdc	-40°C Min	-40°C Max	+24°C Min	+24°C Typ	+24°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage* "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Pins 12,15		5 to 15	0.75	–	0.8	2.0	–	0.85	–	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5) (Pin 7)		5	-0.62	–	-0.5	-1.5	–	-0.35	–	
(V_{OH} = 9.5)		10	-0.62	–	-0.5	-1.0	–	-0.35	–	
(V_{OH} = 13.5)		15	-1.8	–	-1.5	-3.6	–	-1.1	–	
(V_{OL} = 0.4)	I_{OL}	4.75	2.3	–	2.0	4.0	–	1.6	–	mAdc
(V_{OL} = 0.5)		10	5.3	–	4.5	10	–	3.6	–	
(V_{OL} = 1.5)		15	15	–	13	35	–	10	–	
Input Current (Pin 15 = V_{DD})	I_{in}	–	–	–	–	±0.00001	±0.1	–	–	µAdc
Input Pull-Up Resistor Source Current (Pin 15 = V_{SS}, V_{in} = 2.4 Vdc) Pins 1,2,5,6,10,11,12,13,14	Ip	5	285	–	250	460	–	205	–	µAdc
Input Capacitance	C_{in}	–	–	–	–	5.0	–	–	–	pF
Total Supply Current (Pin 15 = V_{DD})	I_T	5	–	4.5	–	1.1	4.0	–	3.5	mAdc
		10	–	13	–	4.0	12	–	11	
		15	–	27	–	8.0	25	–	23	
Modulator/Demodulator Frequency Accuracy (Excluding Crystal)	ACC	5 to 15	–	–	–	0.5	–	–	–	%
Transmit Carrier Output 2nd Harmonic	V_{2H}	5 to 15	–	–	-25	-32	–	–	–	dB
Transmit Carrier Output Voltage (R_L = 100 kΩ) (Pin 9)	V_{out}	5	–	–	0.2	0.30	–	–	–	V_{RMS}
		10	–	–	0.5	0.85	–	–	–	
		15	–	–	1.0	1.5	–	–	–	

*DC Noise Immunity (V_{IL}, V_{IH}) is defined as the maximum voltage change from an ideal "0" or "1" input level, that the curcuit will withstand before accepting an erroneous input.

**Note: Only 5-Volt specifications apply to MC14412VL and MC14412VP devices.

PIN ASSIGNMENT

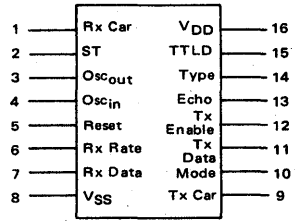


FIGURE 1 – TYPICAL LOW-SPEED MODEM APPLICATION

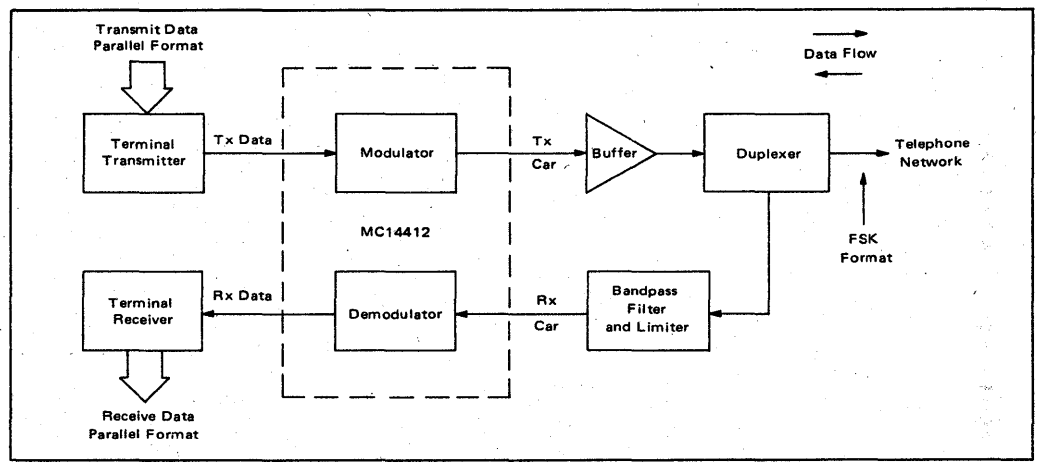
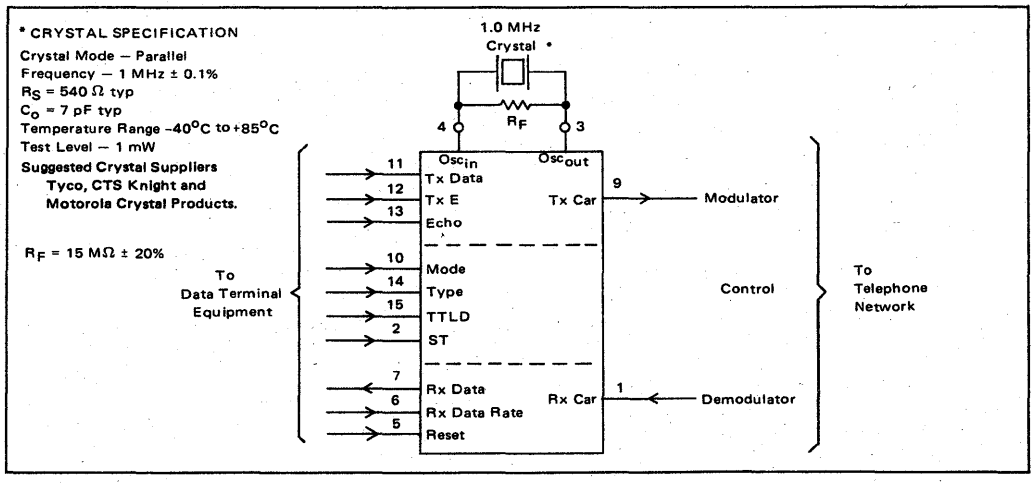


FIGURE 2 – MC14412 INPUT/OUTPUT SIGNALS



DEVICE OPERATION

GENERAL

Figure 1 shows the modem in a system application. The data to be transmitted is presented in serial format to the modulator for conversion to FSK signals for transmission over the telephone network. The modulator output is buffered/amplified before driving the 600 ohm telephone line.

The FSK signal from the remote modem is received via the telephone line and filtered to remove extraneous signals such as the local Transmit Carrier. This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interfering signal. The desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

INPUT/OUTPUT FUNCTIONS

Figure 2 shows the I/O interface for the MC14412 low-speed modem. The following is a description of each individual signal.

TYPE (Pin 14)

The Type input selects either the U.S. or C.C.I.T.T. operational frequencies for both transmitting and receiving data. When the Type input = "1", the U.S. standard is selected and when the Type input = "0", the C.C.I.T.T. standard is selected.

TRANSMIT DATA (Tx Data, Pin 11)

Transmit Data is the binary information input. Data entered for transmission is modulated using FSK techniques. When operating in the U.S. standard (Type = "1") a logic "1" input level represents a Mark or when operating in the CCITT standard (Type = "0") a logic "1" input level represents a Mark.

TRANSMIT CARRIER (Tx Car, Pin 9)

The Transmit Carrier is a digital-synthesized sine wave derived from a 1.0 MHz oscillator reference. The frequency characteristics are as follows:

United States Standard — Type = "1", Echo = "0"

Mode		Tx Data		Tx Car
Originate	"1"	Mark	"1"	1270 Hz
Originate	"1"	Space	"0"	1070 Hz
Answer	"0"	Mark	"1"	2225 Hz
Answer	"0"	Space	"0"	2025 Hz

C.C.I.T.T. Standard — Type = "0", Echo = "0"

Mode		Tx Data		Tx Car
Channel	"1"	Mark	"1"	980 Hz
No. 1	"1"	Space	"0"	1180 Hz
Channel	"0"	Mark	"1"	1650 Hz
No. 2	"0"	Space	"0"	1850 Hz

Echo Suppressor Disable Tone — Type = "0", Echo = "1"

Mode	Tx Data	Tx Car
Chan. No. 2 "0"	"1"	2100 Hz

TRANSMIT ENABLE (Tx Enable, Pin 12)

The Transmit Carrier output is enabled when the Tx Enable input = "1". No output tone can be transmitted when Tx Enable = "0".

MODE (Pin 10)

The Mode input selects the pair of transmitting and receive frequencies used during modulation and demodulation. When Mode = "1", the U.S. originate mode is selected (Type input = "1") or the C.C.I.T.T. Channel No. 1 (Type input = "0"). When mode = "0", the U.S. answer mode is selected (Type input = "1") or the C.C.I.T.T. Channel No. 2 (Type input = "0").

ECHO (Pin 13)

When the Echo input = "1" (Type = "0", Mode = "0", Tx Data = "1") the modulator will transmit a 2100 Hz tone for disabling line echo suppressors. During normal data transmission, this input should be low = "0".

RECEIVE DATA (Rx Data, Pin 7)

The Receive Data output is the digital data resulting from demodulating the Receive Carrier.

RECEIVE CARRIER (Rx Car, Pin 1)

The Receive Carrier is the FSK input to the demodulator. This input must have either a CMOS or TTL compatible logic level input (see TTL pull-up disable) at a duty cycle of 50% ± 4%, that is a square wave resulting from a signal limiter.

RECEIVE DATA RATE (Rx Rate, Pin 6)

The demodulator has been optimized for signal to noise performance at 200, 300, and 600-bps.

Data Rate	Rx Rate	Type
0 - 200 bps	"1"	"0"
0 - 300 bps	"1"	"1"
0 - 600 bps	"0"	"1"

SELF TEST (ST, Pin 2)

When a high level (ST = "1") is placed on this input, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal.

DEVICE OPERATION (continued)

RESET (Pin 5)

This input is provided to decrease the test time of the chip. In normal operation, this input may be used to disable the demodulator (Reset = "1") — otherwise it should be tied low = "0".

CRYSTAL (Osc_{in}, Osc_{out}, Pin 4, Pin 3, respectively)

A 1.0 MHz crystal is required to utilize the on chip oscillator. A 1.0 MHz square wave clock can also be applied to the Osc_{in} input to satisfy the clock requirement (see Figure 2).

When utilizing the 1.0 MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be < 9 pF at the crystal input (pin 4).

TTL PULL-UP DISABLE (TTLD, Pin 15)

To improve TTL interface compatibility, all of the inputs to the MODEM have controllable P-Channel devices which act as pull-up resistors when TTLD input is low ("0"). When the input is taken high ("1") the pull-up is disabled, thus reducing power dissipation when interfacing with CMOS.

FIGURE 3 – M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM

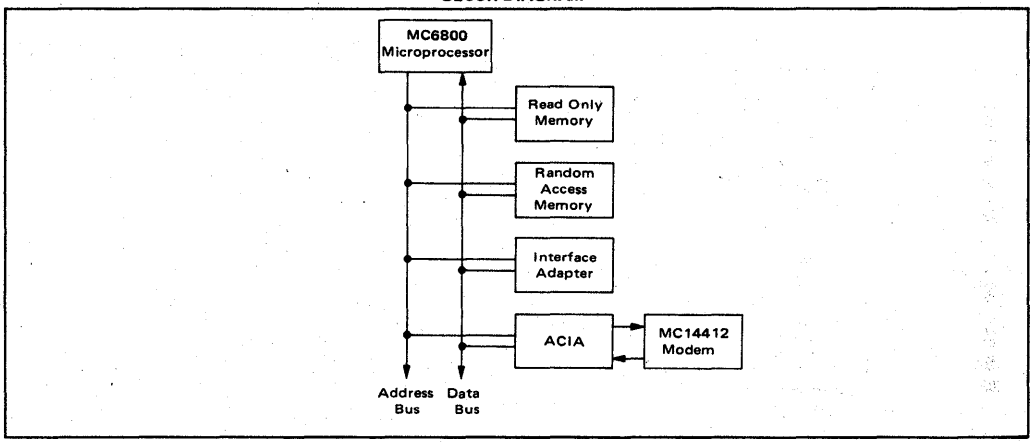


FIGURE 4 – TRANSMIT CARRIER SINEWAVE

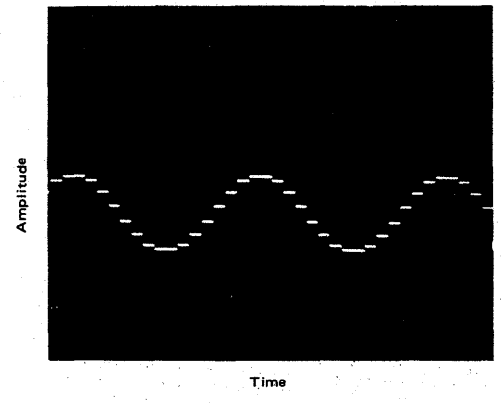
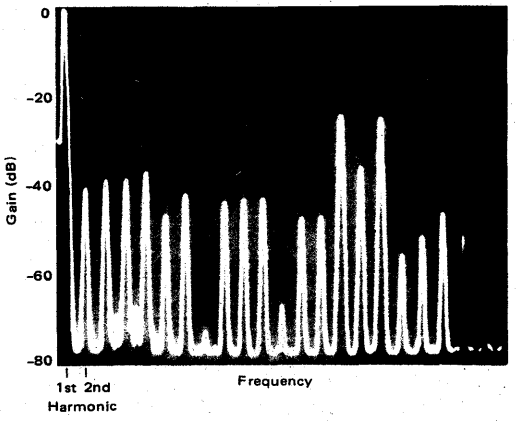


FIGURE 5 – TYPICAL TRANSMIT CARRIER FREQUENCY SPECTRUM



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MC14415

QUAD PRECISION TIMER/DRIVER

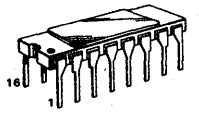
The MC14415 quad timer/driver is constructed with complementary MOS enhancement mode devices. The output pulse width of each digital timer is a function of the input clock frequency. Once the proper input sequence is detected the output buffer is set (turned on), and after 100 clock pulses are counted, the output buffer is reset (turned off).

The MC14415 was designed specifically for application in high speed line printers to provide the critical timing of the hammer drivers, but may be used in many applications requiring precision pulse widths.

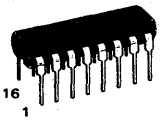
- Four Precision Digital Time Delays
- Schmitt Trigger Clock Conditioning
- NPN Bipolar Output Drivers
- Timing Disable Capability Using Inhibit Output
- Positive or Negative Edge Strobing on the Inputs
- Synchronous Polynomial Counters Used for Delay Counting
- Power Supply Operating Range
  - = 3.0 Vdc to 18 Vdc (MC14415EFL/FL/FP)
  - = 3.0 Vdc to 6.0 Vdc (MC14415EVL/VL/VP)

McMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

QUAD PRECISION TIMER/DRIVER



L SUFFIX
CERAMIC PACKAGE
CASE 690



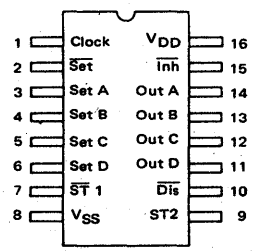
P SUFFIX
PLASTIC PACKAGE
CASE 648

5

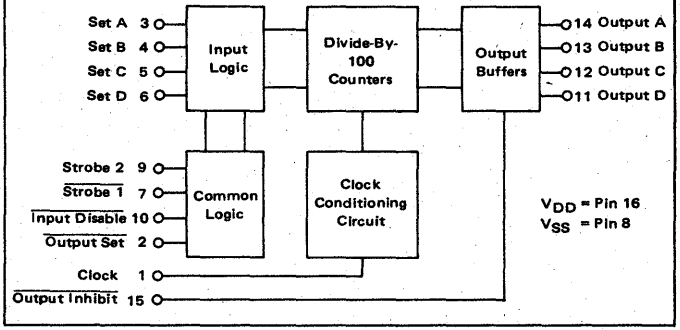
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage – MC14415EFL/FL/FP – MC14415EVL/VL/VP	V_{DD}	 +18 to -0.5 +6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Input Pin	I_{in}	10	mAdc
DC Current Drain per Output Pin	I_{out}	20	mAdc
Operating Temperature Range – MC14415EFL/EVL – MC14415FL/FP/VL/VP	T_A	 -55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN ASSIGNMENT



BLOCK DIAGRAM



ORDERING INFORMATION

MC14415 — Suffix

Suffix	Denotes
L	Ceramic Package
P	Plastic Package
F	*Extended Operating Voltage Range
V	*Limited Operating Voltage Range
Blank	**Standard Operating Temperature Range
E	**Extended Operating Temperature Range

*See Features (above, left)
**See Maximum Ratings

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage (No Load)	"0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	–	–	–	–	
	"1" Level		5.0	–	–	3.0	4.14	–	–	–	Vdc
			10	–	–	8.0	9.09	–	–	–	
			15	–	–	–	14.12	–	–	–	
Noise Immunity		V_{NL}									Vdc
($\Delta V_{out} \leq$ 1.5 Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq$ 3.0 Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq$ 4.5 Vdc)			15	–	–	–	6.75	–	–	–	
($\Delta V_{out} \leq$ 1.5 Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq$ 3.0 Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq$ 4.5 Vdc)			15	–	–	–	6.75	–	–	–	
Output Drive Voltage (NPN Driver)		V_{OH}									Vdc
(I_{OH} = 0 mA)	Source		5.0	–	–	3.0	4.14	–	–	–	
(I_{OH} = 5.0 mA)				–	–	2.7	3.44	–	–	–	
(I_{OH} = 10 mA				–	–	2.5	3.30	–	–	–	
(I_{OH} = 15 mA)				–	–	2.2	3.08	–	–	–	
(I_{OH} = 0 mA)			10	–	–	8.0	9.09	–	–	–	Vdc
(I_{OH} = 5.0 mA)				–	–	7.7	8.45	–	–	–	
(I_{OH} = 10 mA)				–	–	7.5	8.30	–	–	–	
(I_{OH} = 15 mA)				–	–	7.1	8.14	–	–	–	
(I_{OH} = 0 mA)			15	–	–	–	14.12	–	–	–	Vdc
(I_{OH} = 5.0 mA)				–	–	–	13.81	–	–	–	
(I_{OH} = 10 mA)				–	–	–	13.70	–	–	–	
(I_{OH} = 15 mA)				–	–	–	13.61	–	–	–	
Output Drive Current		I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)	Sink		5.0	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)			10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	
Input Leakage Current		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation		P_Q									mW
			5.0	–	0.25	–	0.00005	0.25	–	3.5	
			10	–	1.0	–	0.00022	1.0	–	14	
			15	–	–	–	0.00050	–	–	–	
Power Dissipation** (Dynamic plus Quiescent) (C_L = 15 pF)		P_D	5.0	$P_D = (56\ mW/MHz)\ f + P_Q$							mW
			10	$P_D = (225\ mW/MHz)\ f + P_Q$							
			15	$P_D = (510\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for MC14415EFL, EVL; -40°C for MC14415FL,FP,VL,VP
T_{high} = +125°C for MC14415EFL,EVL; +85°C for MC14415FL,FP,VL,VP

**The formula given is for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Typ	Max	Unit
Output Rise Time*	t_r				ns
t_r = (2.0 ns/pF) C_L + 10 ns		5.0	40	85	
t_r = (1.25 ns/pF) C_L + 6 ns		10	25	60	
t_r = (1.10 ns/pF) C_L + 3 ns		15	20	–	
Output Fall Time*	t_f				ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	150	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	80	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	–	
Turn-Off Delay Time*	t_{PLH}				ns
t_{PLH} = (2.7 ns/pF) C_L + 560 ns		5.0	600	1200	
t_{PLH} = (1.2 ns/pF) C_L + 282 ns		10	300	600	
t_{PLH} = (0.91 ns/pF) C_L + 286 ns		15	150	–	
Turn-On Delay Time*	t_{PHL}				ns
t_{PHL} = (2.4 ns/pF) C_L + 564 ns		5.0	600	1200	
t_{PHL} = (1.0 ns/pF) C_L + 285 ns		10	300	600	
t_{PHL} = (0.75 ns/pF) C_L + 289 ns		15	150	–	
Turn-On Delay Time ($\overline{\text{Inhibit}}$ to Output)	t_{PHLI}				ns
		5.0	300	550	
		10	225	425	
		15	110	–	
Turn-Off Delay Time ($\overline{\text{Inhibit}}$ to Output)	t_{PLHI}				ns
		5.0	300	550	
		10	225	425	
		15	110	–	
Minimum Input Pulse Coincidence (Figure 3)	PC_{min}				ns
		5.0	450	500	
		10	350	450	
		15	–	–	
Minimum Input Pulse Width (Figure 1)	PW_{min}				ns
		5.0	450	500	
		10	350	450	
		15	–	–	
Maximum Input Clock Frequency	f				MHz
		5.0	0.7	–	
		10	1.0	–	
		15	1.5	–	
Clock Input Rise and Fall Times (Figure 1)	t_{cr}, t_{cf}	5.0	–	15	μs
		10	–	5.0	
		15	–	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – SWITCHING CHARACTERISTICS – WAVEFORM RELATIONSHIPS

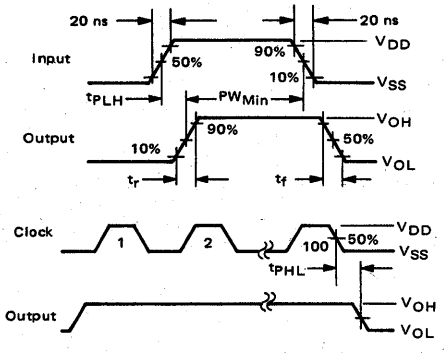


FIGURE 2 – AMBIENT TEMPERATURE POWER DERATING

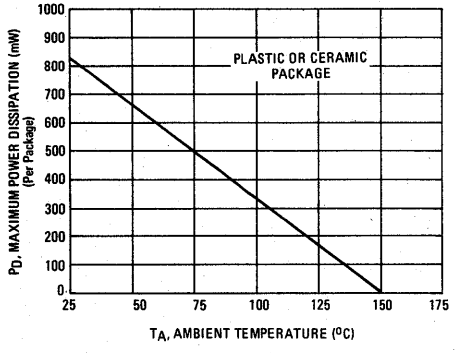
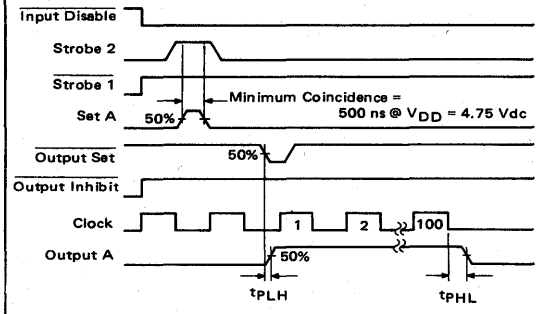
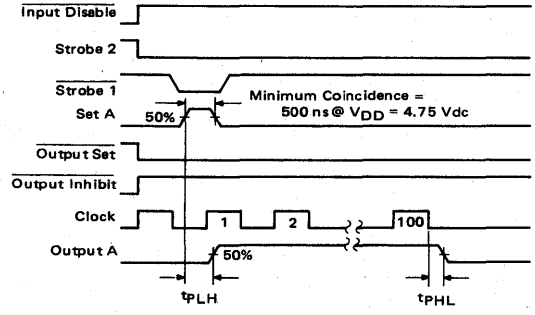


FIGURE 3 – TYPICAL OPERATION MODES AND FUNCTIONAL TIMING DIAGRAM

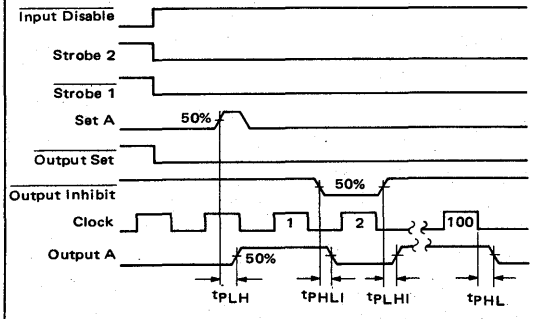
MODE 1 – $\overline{\text{OUTPUT SET}}$ INITIATES TIME DELAY



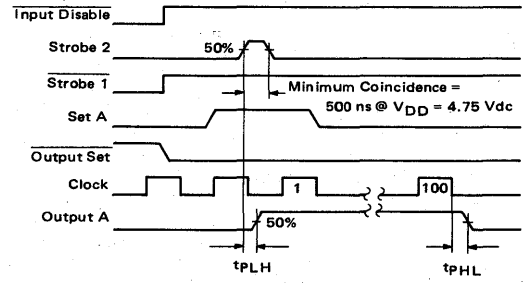
MODE 2 : SET A INITIATES TIME DELAY



MODE 3: $\overline{\text{OUTPUT INHIBIT}}$ DISABLES TIME DELAY



MODE 4: POSITIVE-EDGE STROBE (ST2) INITIATES TIME DELAY



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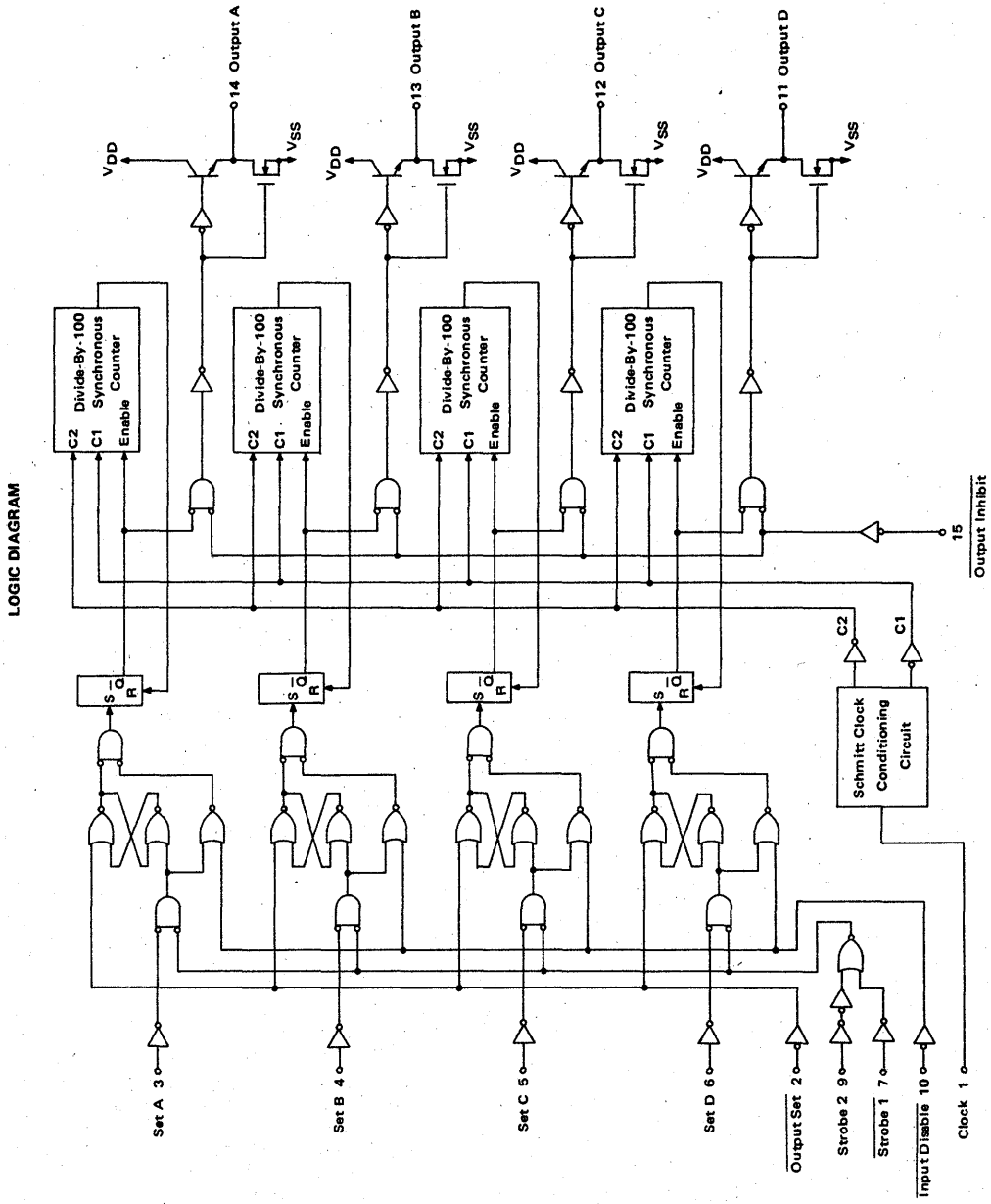
LOGIC DIAGRAM



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14419

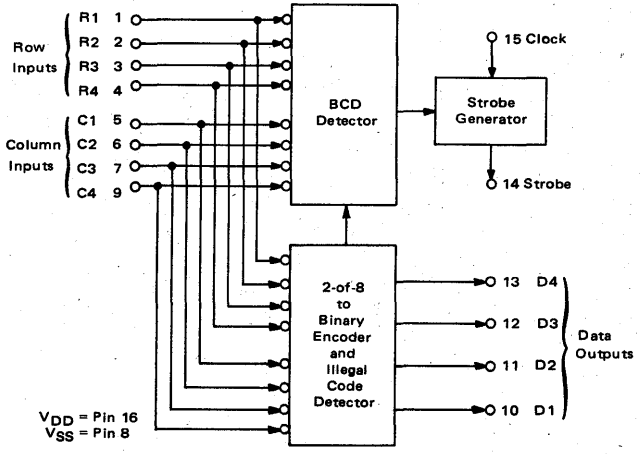
2-OF-8 KEYPAD-TO-BINARY ENCODER

The MC14419 is designed for phone dialer system applications, but finds many applications as a keypad-to-binary encoder. The device contains a 2-of-8 to binary encoder, a strobe generator, and an illegal state detector. The encoder has four row inputs and four column inputs, and is designed to accept inputs from 16 keyswitches arranged in a 4 x 4 matrix. For an output on the four data lines, one and only one row along with one and only one column input line must be activated. All other combinations are suppressed by the illegal state detector to eliminate false data output.

The strobe generator produces a strobe pulse when any of the 10 keys corresponding to numerals 0 through 9 are depressed. The strobe output can be used to eliminate erroneous data entry due to contact bounce. For a strobe output to occur, the key row and column input lines must remain stable for 80 clock pulses after activation. When the contact bounce has settled and 80 clock pulses have occurred, the output will be a single strobe pulse equal in width to that of the clock low state. The strobe generator will output one and only one pulse each time a numerical key is depressed. After the pulse has occurred, noise and bounce due to contact break will not cause another strobe pulse. With a 16 kHz input clock frequency, the pulse occurs 5 ms after the last bounce.

- Suppressed Output for Illegal Input Codes
- On-Chip Pullup Resistors for Row and Column Inputs
- Clock Input Conditioning Circuit
- Low Current Drain in Standby Mode
  5.0 μA Typical @ 5.0 Vdc
- Subsystem Complement to the MC14408/14409 Phone Pulse Converter
- Codes for Numbers 0-9 Produce a Strobe Pulse

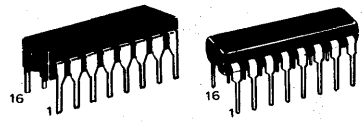
BLOCK DIAGRAM



McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

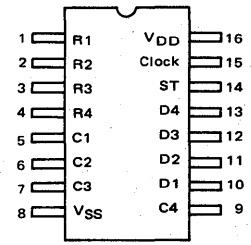
2-OF-8 KEYPAD-TO-BINARY ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

5

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage Operating Range	V_{DD}	–	3.0	6.0	3.0	5.0	6.0	3.0	6.0	Vdc
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	1.5	–	1.5	2.25	–	1.4	–	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	mAdc
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
Input Leakage Current (V_{in} = V_{DD})	I_{IH}	5.0	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Pullup Resistor Source Current (Row and Column Inputs) (V_{in} = V_{SS})	I_{IL}	5.0	265	460	190	250	330	125	215	μAdc
Input Capacitance (V_{in} = V_{SS})	C_{in}	–	–	–	–	5.0	–	–	–	pF
Standby Supply Current (f_{clock} = 16 kHz, No Keys Depressed)	I_{DDS}	3.0	–	3.0	–	1.0	3.0	–	6.0	μAdc
		5.0	–	15	–	5.0	15	–	30	
		6.0	–	60	–	20	60	–	120	
Standby Supply Current as a Function of Clock Frequency* (No Keys Depressed)	I_{DDS}	5.0	I_{DDS} = 0.09 μA/kHz + 3.0 μA							μAdc

*The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise and Fall Times, D1 thru D4 (Figure 1)	t_r,t_f	5.0	–	300	–	ns
Propagation Delay Time, Row or Column Input to Data Output (Figure 1)	t_{PLH}, t_{PHL}	5.0	–	1000	–	ns
Clock Pulse Frequency Range	PRF	3.0 to 6.0	4.0	16	80	kHz

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FIGURE 1 – SWITCHING TIME WAVEFORMS

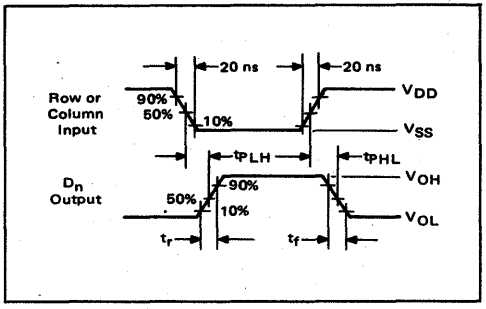
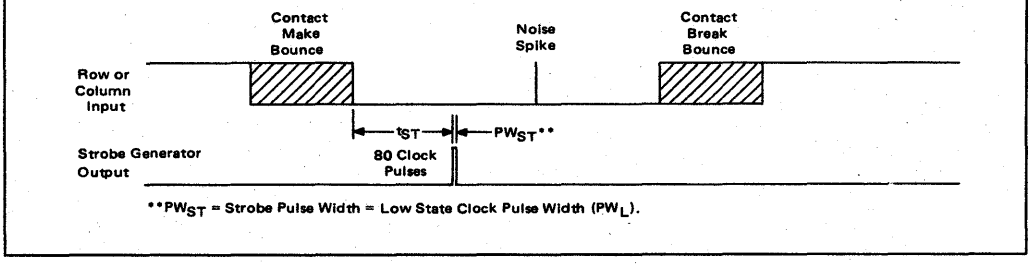


FIGURE 2 – TYPICAL STROBE PULSE DELAY TIMES

PRF Clock Frequency kHz	t_{ST}* Strobe Pulse Delay Time ms
4.0	20
8.0	10
16	5.0
32	2.5
80	1.0

*t_{ST} = (1/PRF) • 80, with PRF in kHz, t_{ST} in ms.

FIGURE 3 – STROBE GENERATOR TIMING DIAGRAM



**PW_{ST} = Strobe Pulse Width = Low State Clock Pulse Width (PW_L).

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TRUTH TABLE

	Inputs								Outputs				
	Row				Column								
Key**	R4	R3	R2	R1	C4	C3	C2	C1	D4	D3	D2	D1	Strobe
1	1	1	1	0	1	1	1	0	0	0	0	1	⎍
2	1	1	1	0	1	1	0	1	0	0	1	0	⎍
3	1	1	1	0	1	0	1	1	0	0	1	1	⎍
A	1	1	1	0	0	1	1	1	1	1	0	0	0
4	1	1	0	1	1	1	1	0	0	1	0	0	⎍
5	1	1	0	1	1	1	0	1	0	1	0	1	⎍
6	1	1	0	1	1	0	1	1	0	1	1	0	⎍
B	1	1	0	1	0	1	1	1	1	1	0	1	0
7	1	0	1	1	1	1	1	0	0	1	1	1	⎍
8	1	0	1	1	1	1	0	1	1	0	0	0	⎍
9	1	0	1	1	1	0	1	1	1	0	0	1	⎍
C	1	0	1	1	0	1	1	1	1	1	1	0	0
*	0	1	1	1	1	1	1	0	1	0	1	0	0
0	0	1	1	1	1	1	0	1	0	0	0	0	⎍
#	0	1	1	1	1	0	1	1	1	0	1	1	0
D	0	1	1	1	0	1	1	1	1	1	1	1	0
	All Other Combinations								0	0	0	0	0

**See Figure 4 for keypad designation.

FIGURE 4 – TYPICAL KEYPAD INTERFACE APPLICATION

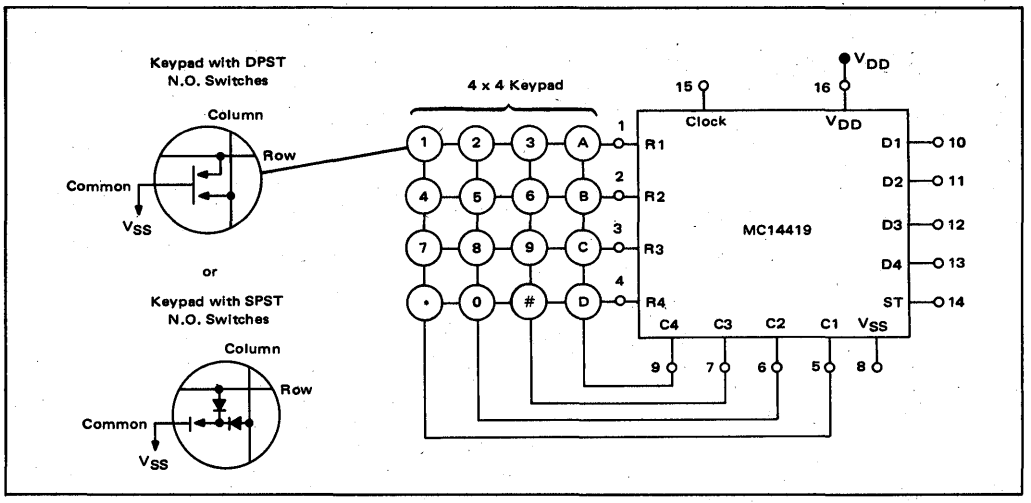
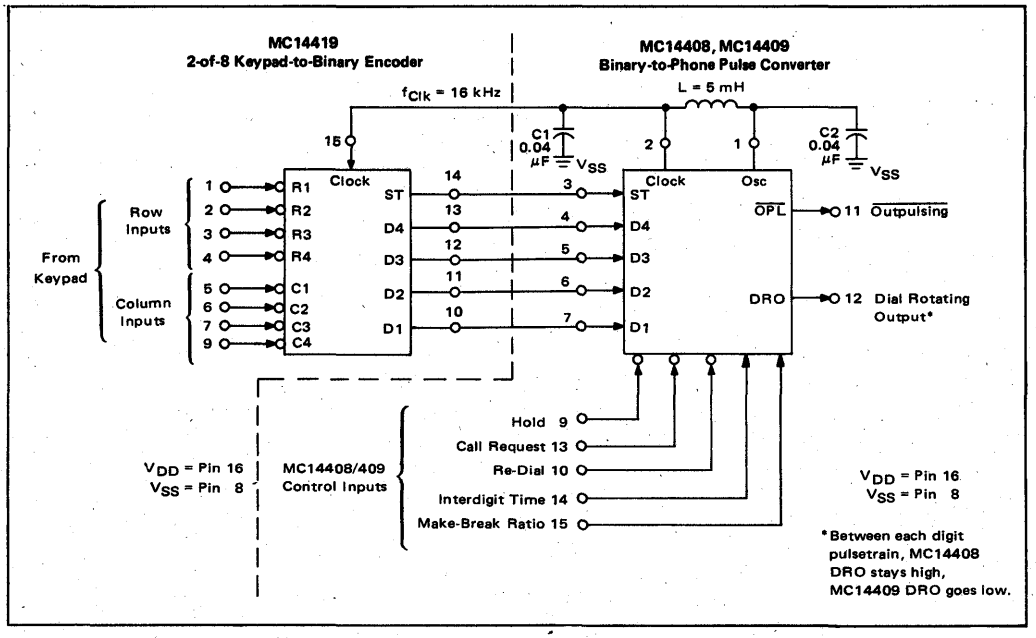


FIGURE 5 – PHONE DIALER SYSTEM



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MC14435

3-1/2 DIGIT A/D LOGIC SUBSYSTEM

The MC14435 A/D Logic is designed specifically for use in a dual-slope integration A/D converter system.

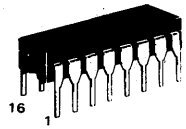
The device consists of 3-1/2 digits of BCD counters, 13 memory latches, and output multiplexing circuitry. An internal clock oscillator is provided to generate system timing and to set the output multiplexing rate. A single capacitor is required to set the oscillator frequency.

- On-Chip Clock to Control Digit Select, Multiplexing, and BCD Counters Simultaneously
- Multiplexed BCD Output
- Built-In 100-Count Delay for Accurate System Conversion of Low-Level Inputs
- System Over-Range Output
- Linear Companion Device Available From Motorola (MC1405L/1505L)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14435EFL/FL/FP)
  = 3.0 Vdc to 6.0 Vdc (MC14435EVL/VL/VP)

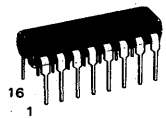
McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

3-1/2 DIGIT A/D LOGIC SUBSYSTEM



L SUFFIX
CERAMIC PACKAGE
CASE 620

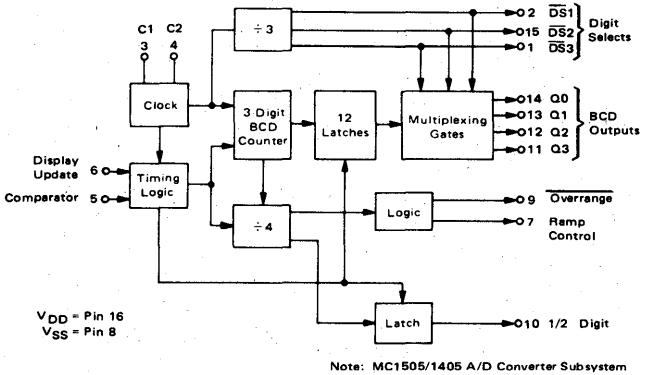


P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

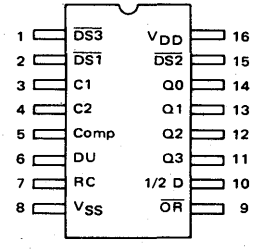
Rating	Symbol	Value	Unit
DC Supply Voltage – MC14435EFL/FL/FP – MC14435EVL/VL/VP	V_{DD}	 +18 to -0.5 +6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range MC14435EFL/EVL MC14435FL/FP/VL/VP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



Note: MC1505/1405 A/D Converter Subsystem recommended for linear front end.

PIN ASSIGNMENT



ORDERING INFORMATION

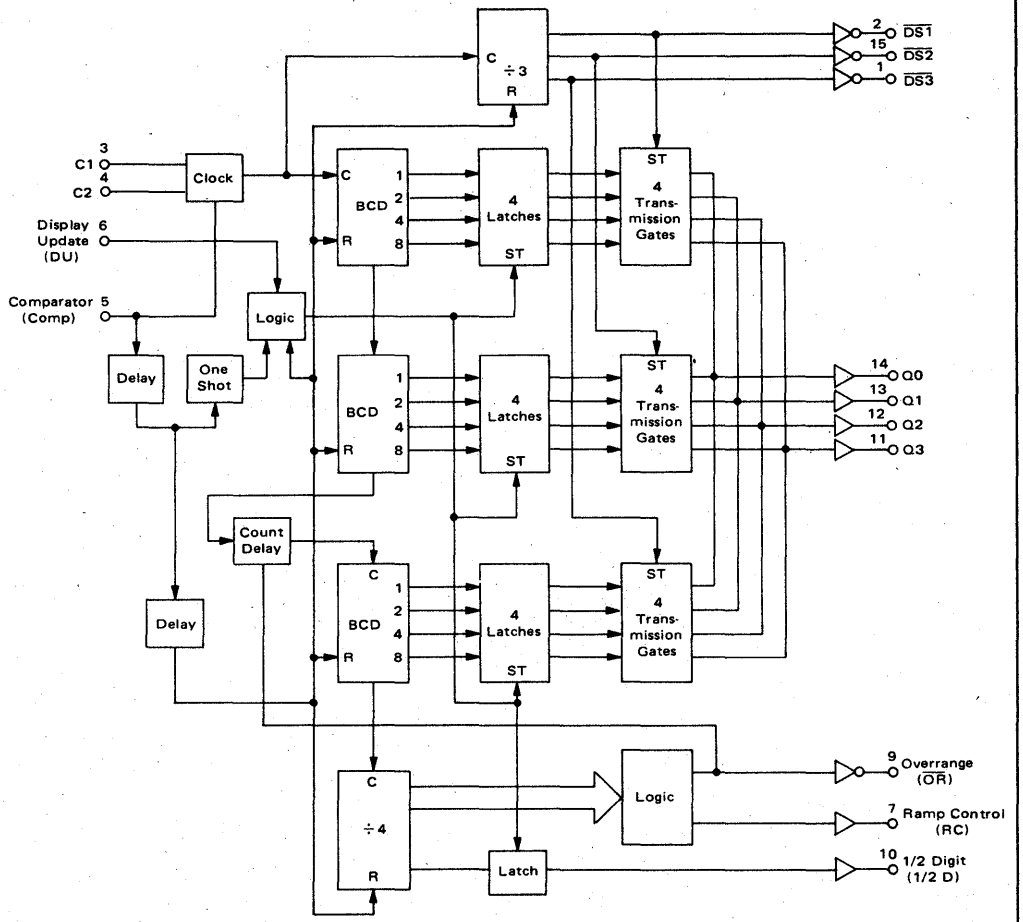
MC14435 + Suffix

Suffix	Denotes
L	Ceramic Package
P	Plastic Package
F	*Extended Operating Voltage Range
V	*Limited Operating Voltage Range
Blank	**Standard Operating Temperature Range
E	**Extended Operating Temperature Range

*See Features (above, left)
**See Maximum Ratings

5

FUNCTIONAL DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}** Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.10	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.90	–	
Noise Immunity	V_{NL}									Vdc
($\Delta V_{out} \leq 1.5$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 3.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 4.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 1.5$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 3.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 4.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current	I_{OH}									mAdc
Source – All outputs										
(V_{OH} = 2.5 Vdc)		5.0	-0.23	–	-0.20	-1.35	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.64	–	-0.14	–	
(V_{OH} = 13.5 Vdc)		15	-0.23	–	-0.20	-2.35	–	-0.14	–	
Sink – $\overline{DSI}$, $\overline{DS2}$, $\overline{DS3}$	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		5.0	1.60	–	1.60	3.45	–	1.12	–	
(V_{OL} = 0.5 Vdc)		10	2.55	–	2.15	6.50	–	1.50	–	
(V_{OL} = 1.5 Vdc)		15	8.35	–	7.0	21.0	–	4.90	–	
Sink – Q0, Q1, Q2, Q3	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		5.0	1.60	–	1.60	2.55	–	1.12	–	
(V_{OL} = 0.5 Vdc)		10	2.25	–	1.90	5.80	–	1.35	–	
(V_{OL} = 1.5 Vdc)		15	7.20	–	6.0	18.5	–	4.20	–	
Sink – 1/2D, RC, $\overline{OR}$	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		5.0	0.23	–	0.20	0.64	–	0.14	–	
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	1.57	–	0.35	–	
(V_{OL} = 1.5 Vdc)		15	2.15	–	1.8	5.5	–	1.25	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q									mW
(Comp Input Low)		5.0	–	2.15	–	0.40	1.75	–	1.75	
		10	–	8.50	–	1.60	6.85	–	6.85	
		15	–	19.50	–	3.6	15.75	–	15.75	
Dynamic Power Dissipation	P_D									mW
(Comp Input High)		5.0	–	12.4	–	2.0	10	–	10	
		10	–	62.0	–	16.7	50	–	50	
		15	–	248	–	66.7	200	–	200	

*T_{low} = -55°C for MC14435 EFL, EVL; -40°C for MC14435FL, FP, VL, VP.
T_{high} = +125°C for MC14435 EFL, EVL; +85°C for MC14435 FL, FP, VL, VP.
**Only 5 volt specifications apply to MC14435 EVL, VL, VP devices.

SWITCHING CHARACTERISTICS (C_L = 15pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Typical All Types	Unit
Output Rise and Fall Time	t_r, t_f	5.0 10 15	100 50 40	ns
Propagation Delay Time (Comp to all Outputs)	t_{PLH}, t_{PHL}	5.0 10 15	14 5.0 3.0	µs
Propagation Delay Time (Clock to RC)	t_{PLH}, t_{PHL}	5.0 10 15	2.4 1.0 0.75	µs
Propagation Delay Time (Clock to Digit Selects or Q outputs)	t_{PLH}, t_{PHL}	5.0 10 45	2.2 0.85 0.65	µs
Display Update Pulse Width	PW(DU)	5.0 10 15	230 90 65	ns
Comparator Pulse Width (Low State)	PW(Comp)	5.0 10 15	11.5 4.5 2.5	µs

5

OPERATING CHARACTERISTICS

The MC14435 contains the clock, BCD counters, latches, BCD multiplexing, and control circuitry for a 3-1/2 digit A to D converter. In conjunction with the MC1505 analog subsystem a multiplexed A to D can be implemented in three 16-pin packages as shown in Figure 5.

Two connections are required between the analog subsystem (MC1505) and the logic subsystem (MC14435). These two connections are the comparator input (Comp) and the ramp control output (RC) of the MC14435. The clock and counters operate whenever the comparator line is high. After 1000 counts from the clock, the RC output goes high, switching the integrator input from the unknown current to the reference current. When the integrator output falls below the threshold level the comparator line goes low, inhibiting the clock and ending the conversion cycle. The BCD content of the counters is then strobed into the latches, the counters reset, and the conversion cycle starts over.

After the RC line goes high, the next 100 pulses are subtracted, compensating for the offset produced by the analog subsystem. The three BCD latch outputs are multiplexed into a single 4-line output. The multiplex frequency

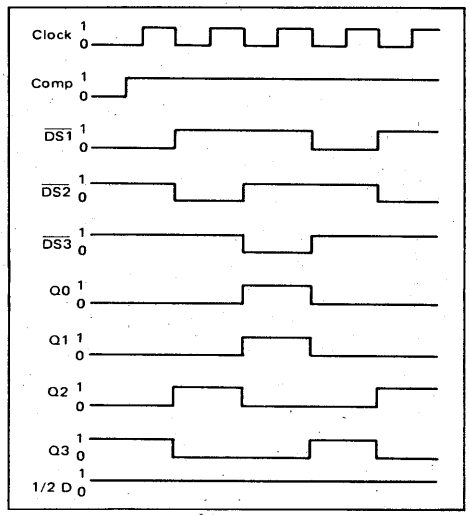
is the same as the clock frequency.

The internal oscillator requires a capacitor between pins 3 and 4. Figure 1 shows a curve of output frequency versus capacitance value for determining the desired system clock frequency. An external clock oscillator may be used by removing the clock capacitor and connecting the external signal to pin 3 (negative edge trigger), or pin 4 (positive edge trigger).

The Display Update input (DU) is used to control the rate of display of the BCD multiplexed outputs. If the DU input is held high, the system makes conversions continuously and strobes each conversion into the memory latches to be multiplexed out. If the DU input is held low, after one conversion has been entered into the latches, all other conversions will be blocked from entering. By synchronizing the DU input with the system clock, the rate of displayed output updating can be controlled.

The 3-digit multiplexed BCD pins 11, 12, 13, and 14 are low for a BCD word of "zero", while the digit select lines are normally high and go low for the individual digit selection. The half-digit output (pin 10) is in the logic "1" state whenever the input voltage is greater than 1.0 volt. When the input voltage is greater than 2.0 volts, pin 9 goes low after 2100 counts are reached during the ramp down portion of the conversion cycle, or 3100 total counts. The overrange ($\overline{OR}$) pin remains in this condition until the counters are reset and the next conversion cycle starts.

OUTPUT MULTIPLEX TIMING DIAGRAM



FUNCTIONAL TRUTH TABLE

INPUTS		
Comp	DU	FUNCTION
0	X	BCD Counter is held reset to "0". Digit Select Counter is held reset to $\overline{DS1}$. Previous count is held in latches. Clock oscillator is inhibited, RC and $\overline{OR}$ are held reset.
⌐	X	Clock oscillator starts BCD counter begins counting clock. Digit Select counter runs, operating output multiplexing. Previous count is held in latches.
⌐	1	Clock oscillator is inhibited. New count is strobed from the first BCD Counter into latches. BCD counters are reset. Digit select counter is reset to $\overline{DS1}$. RC and $\overline{OR}$ are reset.
⌐	0	The first negative edge of Comp after DU is brought low produces the same results as if DU was high. On subsequent cycles of Comp the Clock oscillator, BCD counters, and Digit Select counter operate normally, but no further latch strobes occur. RC and $\overline{OR}$ are reset.

X = Don't Care

FIGURE 1 – TYPICAL OSCILLATOR FREQUENCY versus EXTERNAL CAPACITOR VALUE

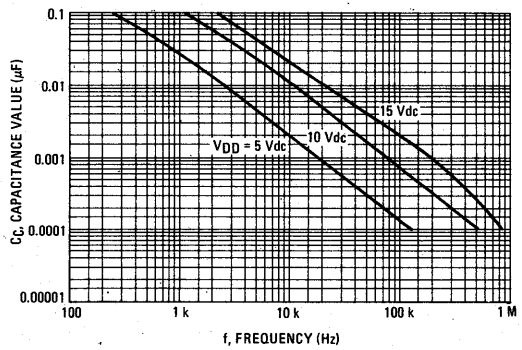
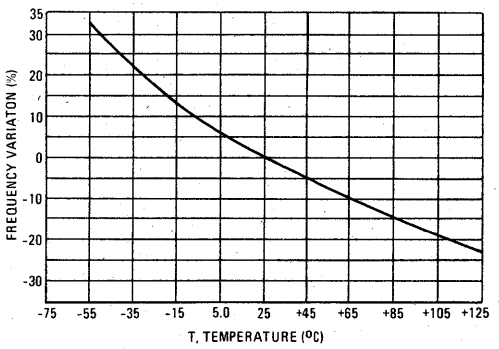


FIGURE 2 – TYPICAL OSCILLATOR FREQUENCY VARIATION versus TEMPERATURE



APPLICATION INFORMATION

The dual ramp A to D system is an integrating converter whose output is relatively independent of both clock frequency and integrator capacitor value. The timing diagram shows a typical conversion cycle for the dual ramp system. A block diagram of the basic system is shown in Figure 3 of the data sheet. The up ramp voltage is created by charging an integrator capacitor with a constant current whose value is proportional to the unknown input voltage. This time period (T1) lasts for a fixed number of clock pulses, which in the case of the MC14435 is 1000 clock pulses. The voltage on the output of the integrator at this point is proportional to the input voltage. After this fixed time period the ramp direction is reversed by switching the integrator capacitor input to a reference current which is the opposite polarity of the input current. The integrator capacitor is discharged until the output voltage reaches the comparator threshold value. This variable time period (T2) is proportional to the unknown input voltage. The unknown input voltage is the product of the reference voltage and the ratio of T2 to T1 or $T2 = T1 \frac{V_X}{V_R}$.

When the input voltage to the basic dual ramp system is zero or near zero the integrator current during the ramp up time period is zero or near zero. In this case the ramp down period would be very short. Thus any noise in the system could cause delay in the comparator line going low and cause instability in low voltage readings. The problem is eliminated by adding a fixed offset current to the unknown current and subtracting out the equivalent number of counts in the digital counters to compensate for the offset current. With this technique the A to D always has at least a minimum number of counts on the counters with a zero input voltage. In the case of the MC14435 the number of pulses subtracted out is 100 pulses; e.g., the down ramp is 100 pulses longer than T2.

For additional information consult the MC1505 (Analog Subsystem) data sheet.

FIGURE 3 – BASIC DUAL RAMP SYSTEM

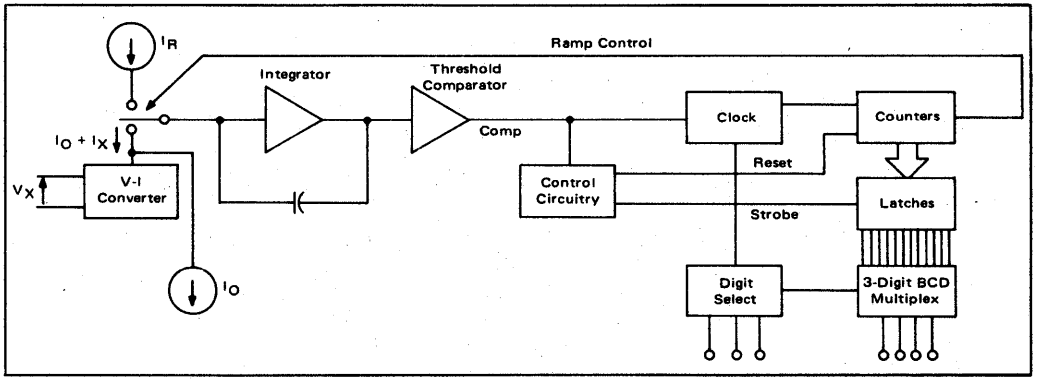


FIGURE 4 – DUAL SLOPE A/D CONVERTER SYSTEM TIMING DIAGRAM

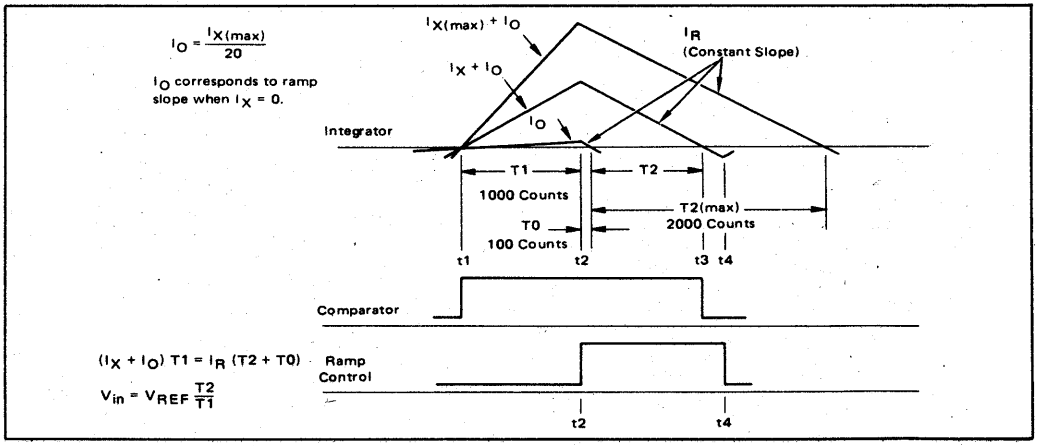
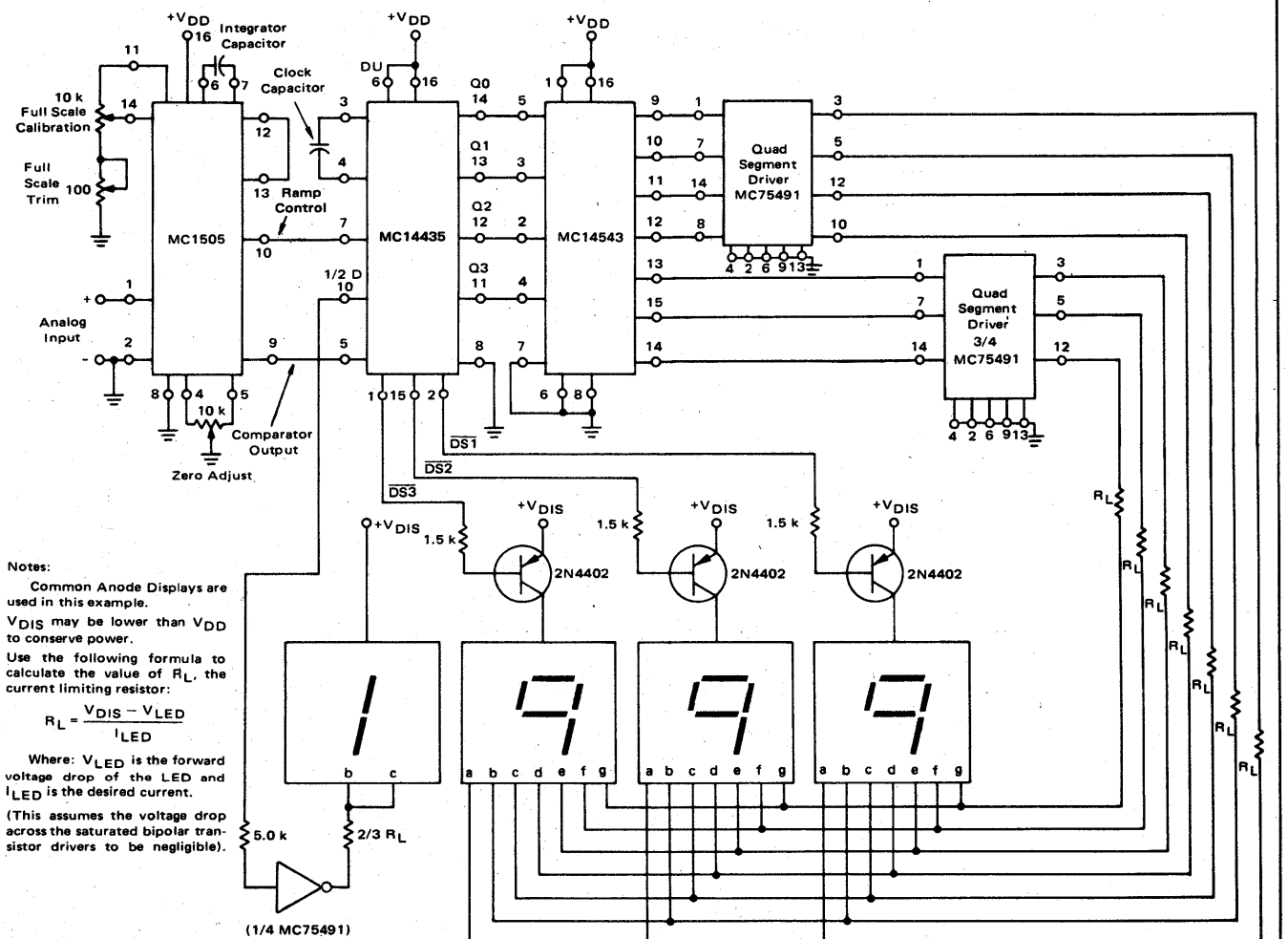


FIGURE 5 – TYPICAL A/D SYSTEM INCLUDING DRIVERS AND LED DISPLAYS



Notes:

Common Anode Displays are used in this example.

V_{DIS} may be lower than V_{DD} to conserve power.

Use the following formula to calculate the value of R_L, the current limiting resistor:

$$R_L = \frac{V_{DIS} - V_{LED}}{I_{LED}}$$

Where: V_{LED} is the forward voltage drop of the LED and I_{LED} is the desired current.

(This assumes the voltage drop across the saturated bipolar transistor drivers to be negligible).

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MC14440

L.C.D WATCH/CLOCK CIRCUIT

The MC14440 utilizes complementary MOS processing to give micropower performance for watch and clock applications. This circuit provides hours and minutes information during normal use. On demand, the seconds and date of the month are displayed sequentially. A 1/2-Hz flashing colon is provided to separate the hours and minutes.

All timekeeping registers in the MC14440 can be set at a 1-Hz rate by enabling the appropriate setting pin (hours, minutes, or days). The seconds register is set to zero when minutes are set; the start pin must be enabled to begin timekeeping.

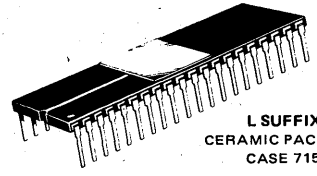
The MC14440 oscillator section is driven by a 32-kHz crystal, biasing capacitors and resistors, and a 1.58-V battery. Outputs are supplied to drive a diode-capacitor voltage converter that provides the drive for the high voltage (3.8 V typical) portion of the circuit and the liquid crystal display.

- Low Current Drain – 5.0 μA typical
- Single CMOS Chip
- On-Chip Oscillator (Uses 32.768-kHz Crystal)
- Diode Input Protection
- Operates from Single 1.58 Vdc Battery
- Frequency Outputs for DC-DC Up-Converter
- Directly Drives a Liquid Crystal Display (L.C.D)
- Hours, Minutes, Seconds, Date of Month Display Capability

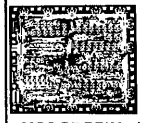
McMOS LSI

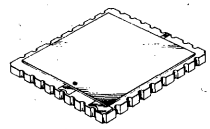
(LOW-POWER COMPLEMENTARY MOS)

L.C.D WATCH/CLOCK CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 715

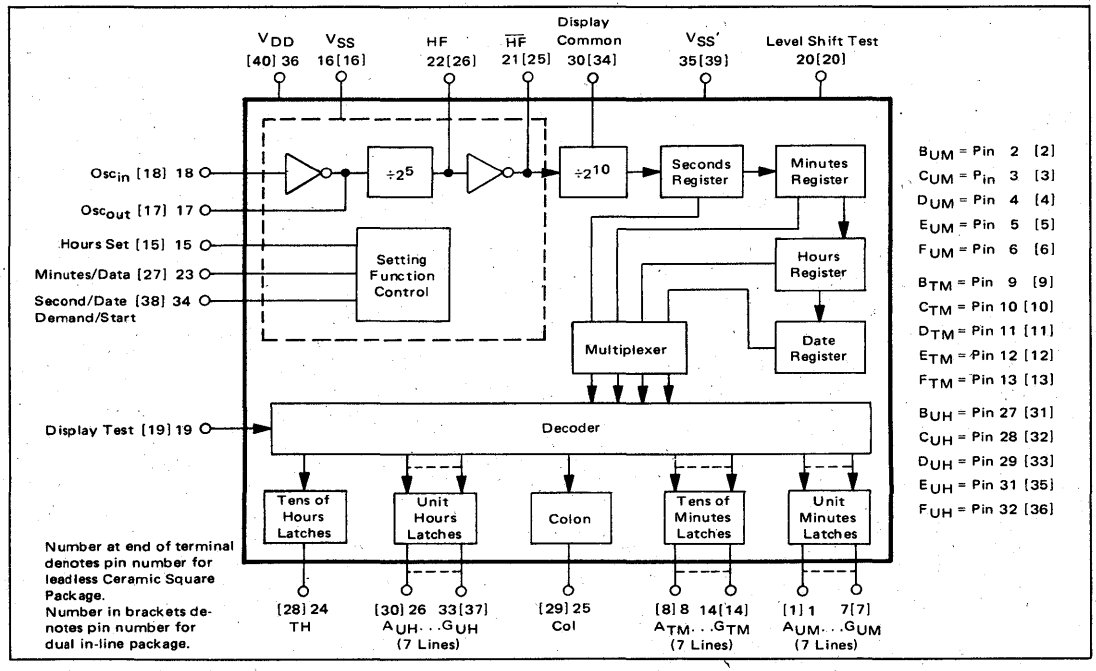




MCC PREFIX
CHIP

Z SUFFIX
LEADLESS CERAMIC PACKAGE
CASE 703

5



MAXIMUM RATINGS (Voltages referenced to V_{DD})

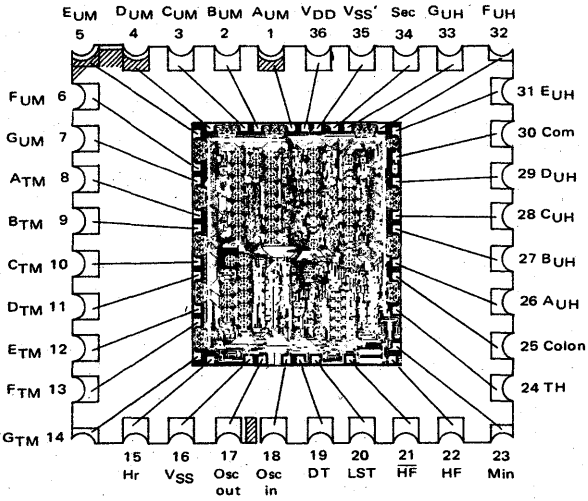
Rating		Symbol	Value	Unit
DC Supply Voltage		V_{SS} V_{SS}'	-1.65 to +0.5 -4.5 to +0.5	Vdc
Input Voltage	Display Test Input	V_{in}	V_{DD} + 0.5 to V_{SS}' -0.5	Vdc
	Other Inputs		V_{DD} + 0.5 to V_{SS} -0.5	
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range		T_A	-10 to +60	°C
Storage Temperature Range		T_{stg}	-30 to +85	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

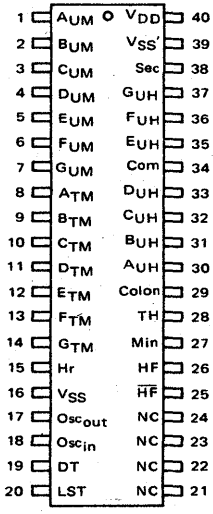
ELECTRICAL CHARACTERISTICS (V_{DD} = 0, V_{SS} = -1.40 Vdc, V_{SS}' = -4.5 Vdc, T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Power Supply Operating Range		V_{SS} V_{SS}'	-1.65 -4.5	-1.58 -3.8	-1.4 -3.0	Vdc
Output High Voltage		V_{OH}	-0.2	0.0	–	Vdc
Output Low Voltage	HF, $\overline{HF}$	V_{OL}	–	-1.4	-1.2	Vdc
	Segment Drivers, Display Common		–	-4.5	-4.3	
Output Drive Current (V_{DS} = 0.2 V)						µAdc
	HF, $\overline{HF}$	I_{OH}	70	100	–	
		I_{OL}	100	250	–	
	Segment Drivers	I_{OH}	2.0	10	–	
		I_{OL}	2.0	40	–	
	Display Common	I_{OH}	15	60	–	
		I_{OL}	15	60	–	
Quiescent Current		I_{QSS} I_{QSS}'	– –	0.1 0.2	1.0 3.0	µAdc
Input Current		I_{in}	–	0.00001	–	µAdc
Dynamic Device Current (f_{in} = 32.768 kHz, No Output Load, V_{SS} = -1.58 V)		I_{SS} I_{SS}'	– –	4.0 1.0	10 3.0	µAdc
Minimum Voltage Required for Oscillator Start (See Applications Information)		$V_{SS_{st}}$	–	1.4	1.5	Vdc



Die Size: 151 x 174 mils
Chip bonding pad assignment same as Case 703 pin assignment.
Chip geometry subject to change without notice as modifications are made.

Due to die cleavage angles, the actual size of the chip could be up to 7.0 mils (0.17 mm) larger than indicated in both dimensions.



OPERATING CHARACTERISTICS

NORMAL OPERATION

During normal operation the setting function inputs are tied to V_{SS} (-1.58 V) and the seven-segment outputs display tens of hours, unit hours, tens of minutes, and unit minutes information. The colon flashes at 1/2 Hz.

SECONDS/DATE DEMAND

When the seconds/date demand input is at V_{DD} (0.0 V) the seconds register information is displayed on the tens of minutes and unit minutes seven-segment outputs. The colon remains on and the tens and unit hours seven-segment outputs are blanked.

When the seconds/date demand input is returned to V_{SS} the date register information is displayed on the unit hours and tens of minutes seven-segment outputs for two to three seconds. Tens of hours, unit minutes, and the colon are blanked while the date is being displayed.

MINUTES SET

When the hours register is at "12", the minutes register may be set at a 1-Hz rate by applying V_{DD} to the minutes/date set input. To begin normal timekeeping, the start input must be enabled.

STARTING

During setting of the minutes register, the seconds register is reset to zero and the other timekeeping registers are prevented from advancing until V_{DD} is applied to the start input (second/date demand). This allows accurate time setting when referenced to a precision time standard.

HOURS SET

The hours register may be set at a 1-Hz rate when V_{DD} is applied to the hour set input. The other timekeeping registers are not altered or affected while hours are being set.

DATE SET

When the hours are not at "12" the date register may be set at a 1-Hz rate by applying V_{DD} to the minute/date set input. The other timekeeping registers are not affected while the date is being set.

DISPLAY TEST

When the display test input has V_{DD} applied, it may be used to generate a "1" on all seven-segment outputs relative to the voltage level of the display common output.

LEVEL SHIFT TEST

The level shift test input must be left open during normal operation. This input is used for rapid testing of the circuit. If it is tied to a fixed voltage, normal operation will be inhibited.

5

NORMAL DISPLAY TRUTH TABLE

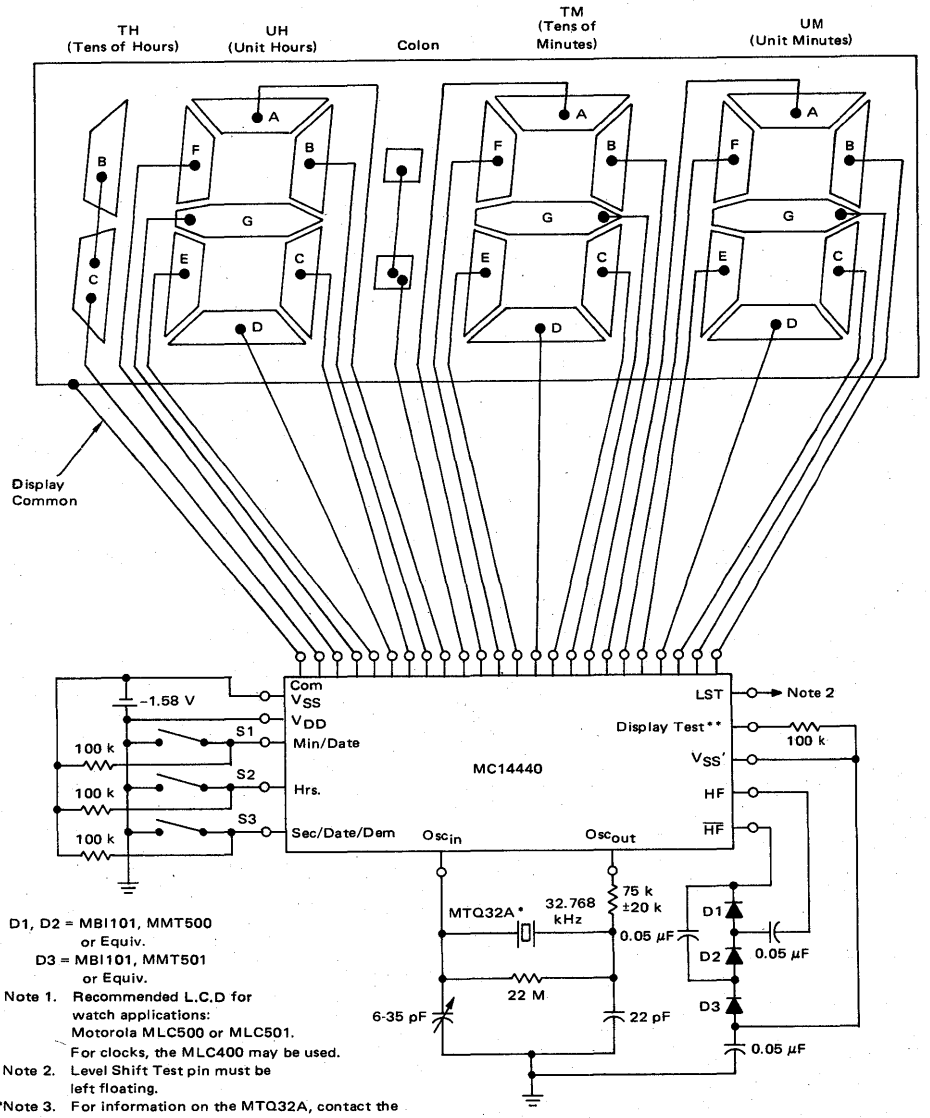
Function	Second/Date Demand/Start	Hours Set	Minutes/ Date Set	Comments
Hours, minutes display	0	0	0	Timepiece runs normally with hours and minutes displayed and the colon blinking.
Seconds display	1	0	0	Timepiece displays seconds and colon only.
Date display	0	0	0	For 2 to 3 seconds after coming to this input condition from the seconds display input condition, the date is displayed on the center two digits.

SETTING PROCEDURE

Step	Second/Date Demand/Start	Hours Set	Minutes/ Date Set	Comments
1. Set hours ≠ 12.	0	1	0	Hours advance at 1-Hz rate until released to the 0, 0, 0 input condition.
2. Set date.	0	0	1	With hours ≠ 12, date advances at a 1-Hz rate.
3. Set hours = 12.	0	1	0	Hours advance at 1-Hz rate until released to the 0, 0, 0 input condition.
4. Set minutes.	0	0	1	With hours = 12, minutes advance at 1-Hz rate and seconds are reset to zero.
5. Set hours.	0	1	0	Hours advance at 1-Hz rate until released to the 0, 0, 0 input condition.
6. Initiate timekeeping.	1	0	0	Timekeeping is started; date will be displayed for 2 to 3 seconds, then hours and minutes with colon blinking.

0 = V_{SS}, 1 = V_{DD}

APPLICATIONS INFORMATION



D1, D2 = MBI101, MMT500 or Equiv.
D3 = MBI101, MMT501 or Equiv.

Note 1. Recommended L.C.D for watch applications: Motorola MLC500 or MLC501. For clocks, the MLC400 may be used.

Note 2. Level Shift Test pin must be left floating.

*Note 3. For information on the MTQ32A, contact the Motorola Quartz Timepiece Crystal Group, (312) 451-1000.

**Note 4. When Display Test is connected to ground (V_{DD}), all segments are displayed.

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14450

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

OSCILLATOR/2^{16} DIVIDER/BUFFER

OSCILLATOR/2^{16} DIVIDER/BUFFER
with Integrated Feedback Capacitor

The MC14450 consists of an oscillator, 16-stage divider, and two buffers in a single monolithic structure. This circuit employs complementary MOS devices for low-voltage operation and extremely low power dissipation. It finds primary use in crystal controlled timing circuitry, and is particularly suited for wristwatch and low-voltage clock operation.

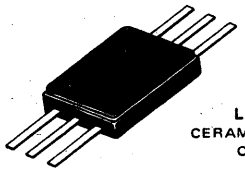
The oscillator section has an output capacitor integrated on the chip. The addition of a crystal, an input capacitor, and a feedback resistor is all that is necessary to complete the oscillator circuit.

The divider section consists of a 16-stage binary divider. Two outputs are provided, 180 degrees out of phase. The outputs of the last six stages of the divider are used to gate the output pulses, providing narrow output pulse widths. Both outputs are buffered to provide fast rise and fall times, and to maximize energy transfer to the load for the pulse duration.

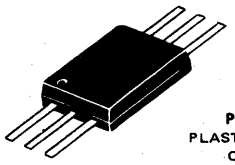
The MC14450 utilizes a 1.58 volt silver oxide battery, and provides peak output pulse voltages of more than 1.20 volts with a 5.2 kilohm load.

This device provides a divide-by-65,536 function and can be operated at frequencies to 1.0 MHz. When operated at 32.768 kHz, it provides 0.5 Hz, 1.563% duty cycle alternating output pulses.

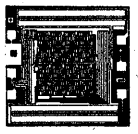
- Extremely Low Operating Current Consumption: 4.0 μA Typical
- Typical Power Supply = 1.58 V
- Inverting Amplifier with Integrated Feedback Capacitor
- Gated and Buffered Outputs
- Diode Protection on Input
- High Output Drive at Low Voltage



L SUFFIX
CERAMIC PACKAGE
CASE 688

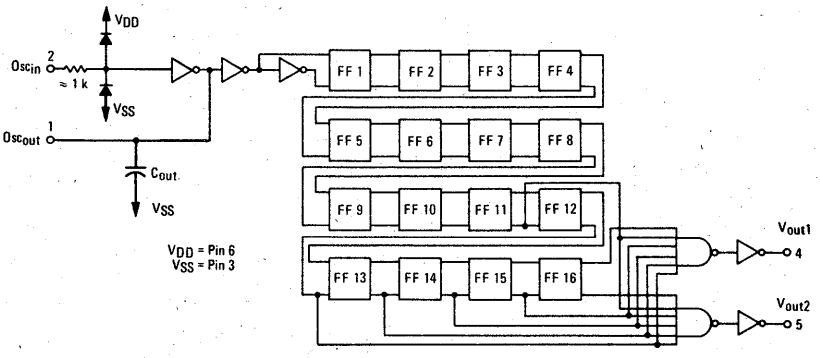


P SUFFIX
PLASTIC PACKAGE
CASE 704



MCC PREFIX
CHIP

BLOCK DIAGRAM



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MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 3.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+3.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	0 to +50	°C
Storage Temperature Range	T_{stg}	-30 to +85	°C

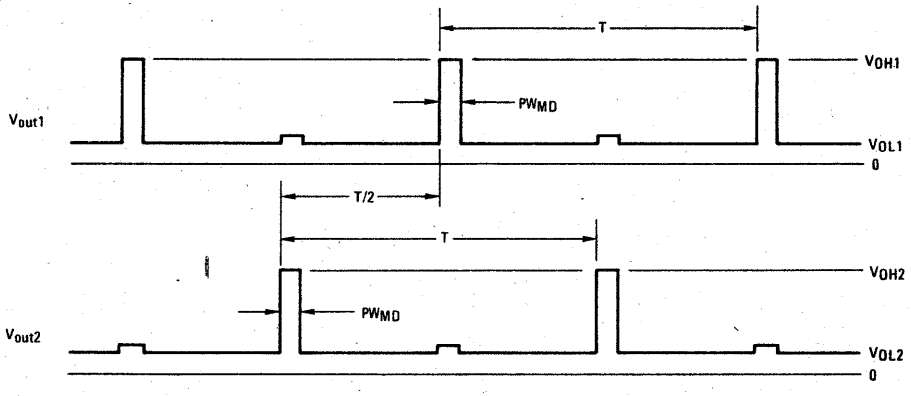
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (V_{DD} = 1.58 Vdc, V_{SS} = 0, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Operating Range	V_{DD}	1.3	1.5	3.0	Vdc
Output Voltage (No Load)	V_{OH}	1.4	1.5	–	Vdc
	V_{OL}	–	0.0	0.1	Vdc
Output Drive Current					
(V_{OH} = 1.3 Vdc)	I_{OH}	700	–	–	μAdc
(V_{OL} = 0.2 Vdc)	I_{OL}	1000	–	–	μAdc
Input Current	I_{in}	–	0.00001	–	μAdc
Quiescent Device Current	I_Q	–	–	1.0	μAdc
Dynamic Device Current	I_{DD}				μAdc
(f = 32.768 kHz, No Output Load) Square Wave, Pin 2		–	2.6	7.0	
MTQ32A Crystal		–	4.0	–	
Minimum Voltage Required for Oscillator Start	V_{DDS}	–	1.4	1.5	Vdc
Feedback Oscillator Capacitance	C_{out}	–	20	–	pF

FIGURE 1 – OUTPUT WAVEFORMS



PW_{MD}, MOTOR DRIVE PULSE WIDTH = $0.01563\ T$

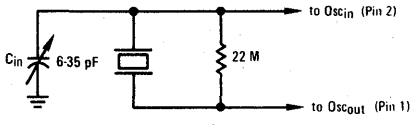
OUTPUT PERIOD, $T = \frac{65536}{\text{INPUT FREQUENCY}}$

$V_{on1} = V_{OH1} = V_{OL2}$

$V_{on2} = V_{OH2} = V_{OL1}$

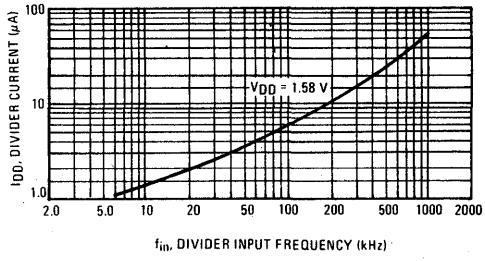
Note: Refer to Figure 4 for connection diagram.

FIGURE 2 – TYPICAL 32-kHz OSCILLATOR CIRCUIT



MOTOROLA MTQ32A CRYSTAL
$f_{A(C_L)}$ = 32.768 kHz
$R_S \leq 30\ k\Omega$
C_0 = 1.9 pF Typical
C_1 = 0.0056 pF Typical

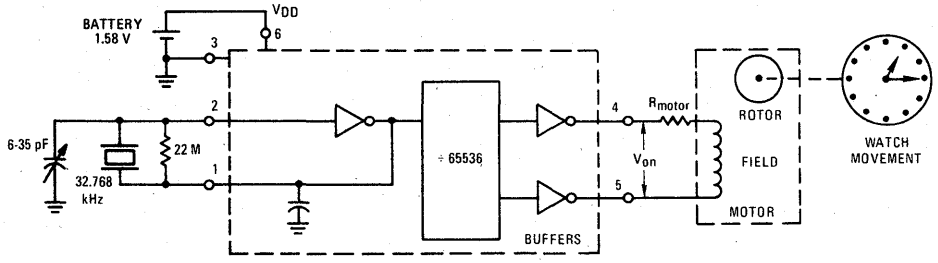
FIGURE 3 – TYPICAL CURRENT DRAIN versus FREQUENCY (No Output Load)



APPLICATIONS INFORMATION

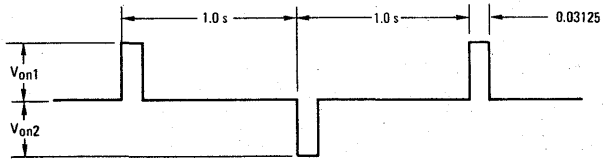
Figure 4 illustrates a typical wristwatch system. The MC14450 drives a rotary motor which rotates 180° with each input pulse.

FIGURE 4 – TYPICAL WRISTWATCH SYSTEM



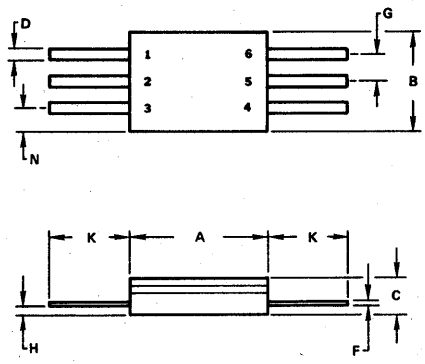
V_{on} = Voltage at pin 4 minus voltage at pin 5.
R_{motor} = 5.2 k Ω minimum

OUTPUT WAVEFORM ACROSS MOTOR



PACKAGE DIMENSIONS

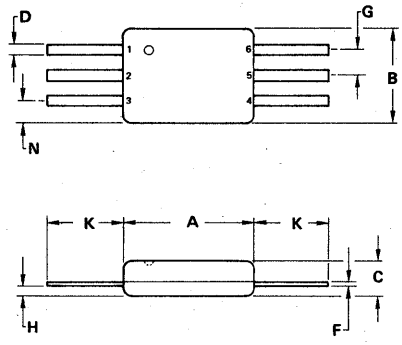
CASE 688-05



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	7.11	0.235	0.280
B	4.32	5.72	0.170	0.225
C	1.17	1.91	0.046	0.075
D	0.25	0.51	0.010	0.020
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.13	0.89	0.005	0.035
K	1.90	3.05	0.075	0.120
N	0.89	1.52	0.035	0.060

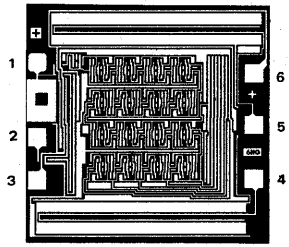
NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.13 mm (0.005) RADIUS TO DIM "A" & "B" AT MAXIMUM MATERIAL CONDITION.

CASE 704-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.69	6.35	0.224	0.250
B	4.06	5.08	0.160	0.200
C	1.17	1.90	0.046	0.075
D	0.38	0.51	0.015	0.020
F	0.20	0.30	0.008	0.012
G	1.22	1.32	0.048	0.052
H	0.13	0.89	0.005	0.035
K	2.34	2.84	0.092	0.112
N	0.89	1.14	0.035	0.045

MCC14450 BONDING PADS



Chip geometry subject to change without notice as modifications are made.

Due to die cleavage angles, the actual size of the chip could be up to 7.0 mils (0.17 mm) larger than indicated in both dimensions.

Die Size: 64 x 68 mils

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MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14451

OSCILLATOR/2^{11} to 2^{19} DIVIDER/BUFFERED DUTY CYCLE CONTROL

The MC14451 consists of three sections: an oscillator, an 18-stage divider, and a buffered flip-flop for pulse width control and current sink drive. These circuits employ metal-gate complementary MOS devices for low-voltage operation and extremely low power dissipation.

A wide variety of output pulse widths and frequencies can be obtained using the pulse-width-control flip-flop. The number of combinations can be further increased by the variety of crystal frequencies or R-C networks used with the oscillator section.

The buffered output of the duty-cycle-control flip-flop consists of an N-channel MOSFET for maximum current sinking capability and a P-channel active pullup device. Outputs from the 18-stage divider section provide a negative logic binary count.

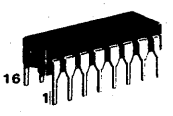
Applications of the MC14451 include power-off timers, low-power-consumption timers especially suited for battery applications, elapsed timers, wall clocks, auto-timers for feeding systems, fuse timers, incubator timers, weather measurement equipment, and many other battery or low-power applications.

- On-Chip Duty Cycle Control
- Buffered Duty Cycle Control Output
- On-Chip Oscillator
- Low Power Consumption —20 μW typical @ 1.5 Vdc and f = 262 kHz
- Operating Supply Voltage Range = 1.3 to 3.0 Vdc
- Diode Protection on Inputs

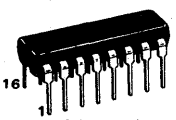
McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

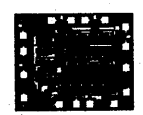
OSCILLATOR/2^{11} to 2^{19} DIVIDER/ BUFFERED DUTY CYCLE CONTROL



L SUFFIX
CERAMIC PACKAGE
CASE 620



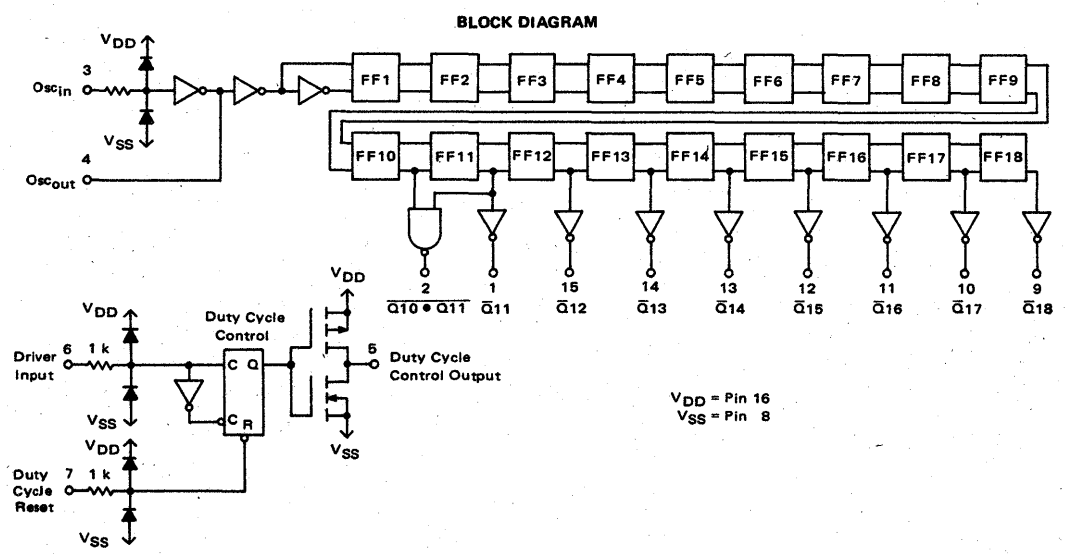
P SUFFIX
PLASTIC PACKAGE
CASE 648



MCC PREFIX
CHIP

5

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{DD}	+3.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-10 to +60	°C
Storage Temperature Range	T_{stg}	-30 to +85	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (V_{DD} = 1.58 Vdc, V_{SS} = 0, T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Power Supply Operating Range		V_{DD}	1.3	1.5	3.0	Vdc
Output Voltage		V_{OH}	1.38	1.5	–	Vdc
		V_{OL}	–	0.0	0.2	Vdc
Output Drive Current		I_{OH}				μAdc
(V_{OH} = 1.3 Vdc)	Divider Outputs		-8.0	-25	–	
	Duty Cycle Control Output		-8.0	-25	–	
(V_{OL} = 0.2 Vdc)	Divider Outputs	I_{OL}	15	50	–	μAdc
	Duty Cycle Control Output		400	1200	–	
Input Current		I_{in}	–	0.00001	–	μAdc
Quiescent Device Current		I_Q	–	1.0	15	μAdc
Dynamic Device Current (f = 262.144 kHz, no output load)		I_{DD}	–	20	200	μAdc
Minimum Voltage Required for Oscillator Start		V_{DDS}	–	1.2	1.5	Vdc

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TYPICAL OSCILLATOR CIRCUITS

FIGURE 1 – 262-kHz CIRCUIT

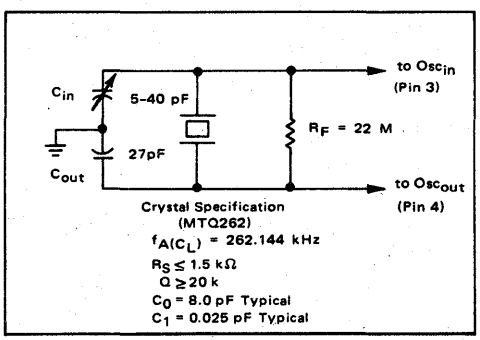


FIGURE 2 – 32.768 kHz CIRCUIT

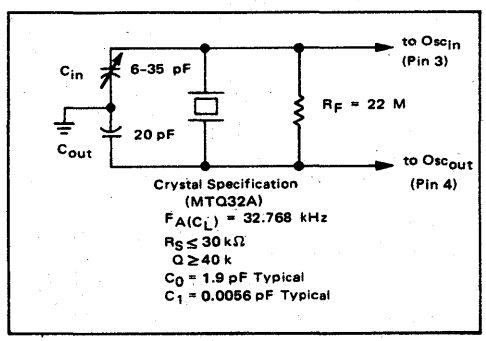
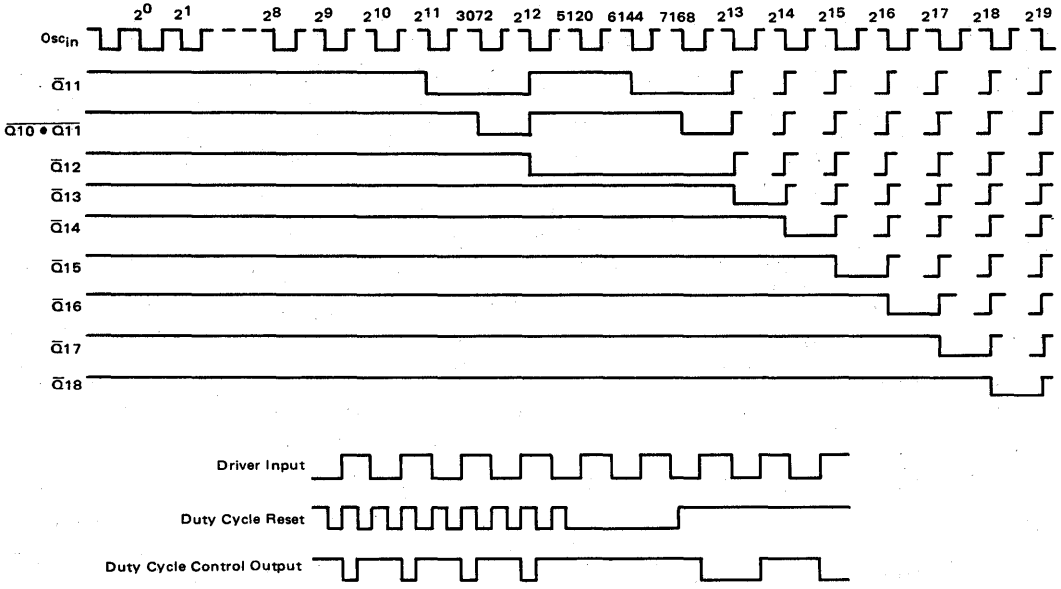


FIGURE 3 – TIMING DIAGRAM



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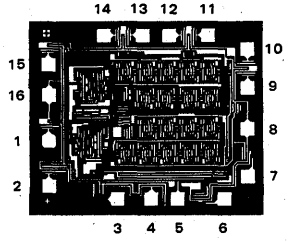
MCC14451 BONDING PADS



Die Size: 67 x 69 mils

Chip geometry subject to change without notice as modifications are made.

Due to die cleavage angles, the actual size of the chip could be up to 7.0 mils (0.17 mm) larger than indicated in both dimensions.

FIGURE 4 – FUNCTIONAL MATRIX

Crystal Frequency = 262.144 kHz

Pin 6 (Driver Input) Connected To:	Characteristic	Pin 7 (Duty Cycle Reset) Connected To:								
		Pin 1 $\overline{Q11}$	Pin 2 $\overline{Q10 \cdot Q11}$	Pin 15 $\overline{Q12}$	Pin 14 $\overline{Q13}$	Pin 13 $\overline{Q14}$	Pin 12 $\overline{Q15}$	Pin 11 $\overline{Q16}$	Pin 10 $\overline{Q17}$	Pin 9 $\overline{Q18}$
Pin 9 $\overline{Q18}$	Pulse Width	3.9 ms	5.85 ms	7.8 ms	15.62 ms	31.25 ms	62.5 ms	125 ms	250 ms	500 ms
	f_{out}	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz
Pin 10 $\overline{Q17}$	Pulse Width	3.9 ms	5.85 ms	7.8 ms	15.62 ms	31.25 ms	62.5 ms	125 ms	250 ms	
	f_{out}	2 Hz	2 Hz	2 Hz	2 Hz	2 Hz	2 Hz	2 Hz	2 Hz	
Pin 11 $\overline{Q16}$	Pulse Width	3.9 ms	5.85 ms	7.8 ms	15.62 ms	31.25 ms	62.5 ms	125 ms		
	f_{out}	4 Hz	4 Hz	4 Hz	4 Hz	4 Hz	4 Hz	4 Hz		
Pin 12 $\overline{Q15}$	Pulse Width	3.9 ms	5.85 ms	7.8 ms	15.62 ms	31.25 ms	62.5 ms			
	f_{out}	8 Hz	8 Hz	8 Hz	8 Hz	8 Hz	8 Hz			
Pin 13 $\overline{Q14}$	Pulse Width	3.9 ms	5.85 ms	7.8 ms	15.62 ms	31.25 ms				
	f_{out}	16 Hz	16 Hz	16 Hz	16 Hz	16 Hz				
Pin 14 $\overline{Q13}$	Pulse Width	3.9 ms	5.85 ms	7.8 ms	15.62 ms					
	f_{out}	32 Hz	32 Hz	32 Hz	32 Hz					
Pin 15 $\overline{Q12}$	Pulse Width	3.9 ms	5.85 ms	7.8 ms						
	f_{out}	64 Hz	64 Hz	64 Hz						
Pin 1 $\overline{Q11}$	Pulse Width	3.9 ms								
	f_{out}	128 Hz								

Crystal Frequency = 32.768 kHz

Pin 6 (Driver Input) Connected To:	Characteristic	Pin 7 (Duty Cycle Reset) Connected To:								
		Pin 1 $\overline{Q11}$	Pin 2 $\overline{Q10 \cdot Q11}$	Pin 15 $\overline{Q12}$	Pin 14 $\overline{Q13}$	Pin 13 $\overline{Q14}$	Pin 12 $\overline{Q15}$	Pin 11 $\overline{Q16}$	Pin 10 $\overline{Q17}$	Pin 9 $\overline{Q18}$
Pin 9 $\overline{Q18}$	Pulse Width	31.3 ms	46.8 ms	62.5 ms	125 ms	250 ms	500 ms	1000 ms	2000 ms	4000 ms
	f_{out}	0.125 Hz	0.125 Hz	0.125 Hz	0.125 Hz	0.125 Hz	0.125 Hz	0.125 Hz	0.125 Hz	0.125 Hz
Pin 10 $\overline{Q17}$	Pulse Width	31.3 ms	46.8 ms	62.5 ms	125 ms	250 ms	500 ms	1000 ms	2000 ms	
	f_{out}	0.25 Hz	0.25 Hz	0.25 Hz	0.25 Hz	0.25 Hz	0.25 Hz	0.25 Hz	0.25 Hz	
Pin 11 $\overline{Q16}$	Pulse Width	31.3 ms	46.8 ms	62.5 ms	125 ms	250 ms	500 ms	1000 ms		
	f_{out}	0.5 Hz	0.5 Hz	0.5 Hz	0.5 Hz	0.5 Hz	0.5 Hz	0.5 Hz		
Pin 12 $\overline{Q15}$	Pulse Width	31.3 ms	46.8 ms	62.5 ms	125 ms	250 ms	500 ms			
	f_{out}	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz			
Pin 13 $\overline{Q14}$	Pulse Width	31.3 ms	46.8 ms	62.5 ms	125 ms	250 ms				
	f_{out}	2 Hz	2 Hz	2 Hz	2 Hz	2 Hz				
Pin 14 $\overline{Q13}$	Pulse Width	31.3 ms	46.8 ms	62.5 ms	125 ms					
	f_{out}	4 Hz	4 Hz	4 Hz	4 Hz					
Pin 15 $\overline{Q12}$	Pulse Width	31.3 ms	46.8 ms	62.5 ms						
	f_{out}	8 Hz	8 Hz	8 Hz						
Pin 1 $\overline{Q11}$	Pulse Width	31.3 ns								
	f_{out}	16 Hz								

5

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MC14490

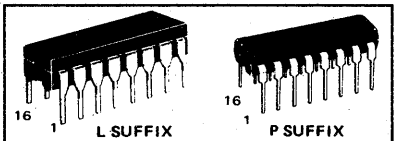
HEX CONTACT BOUNCE ELIMINATOR

The MC14490 is constructed with complementary MOS enhancement mode devices, and is used for the elimination of extraneous level changes that result when interfacing with mechanical contacts. The digital contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. The bounce eliminator circuit will remove bounce on both the "make" and the "break" of a contact closure. The clock for operation of the MC14490 is derived from an internal R-C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay). The clock may also be driven from an external clock source or the oscillator of another MC14490.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Six Debouncers per Package
- Internal Pullups on All Data Inputs
- Internal Oscillator (R-C), or External Clock Source
- TTL Compatible Data Inputs/Outputs
- Single Line Input, Debounces Both "Make" and "Break" Contacts
- Does Not Require "Form C" (Single Pole Double Throw) Input Signal
- Cascadable for Longer Time Delays
- Schmitt Trigger on Clock Input (Pin 7)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14490EFL/FL/FP)
  = 3.0 Vdc to 6.0 Vdc (MC14490EVL/VL/VP)

McMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

HEX CONTACT BOUNCE ELIMINATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

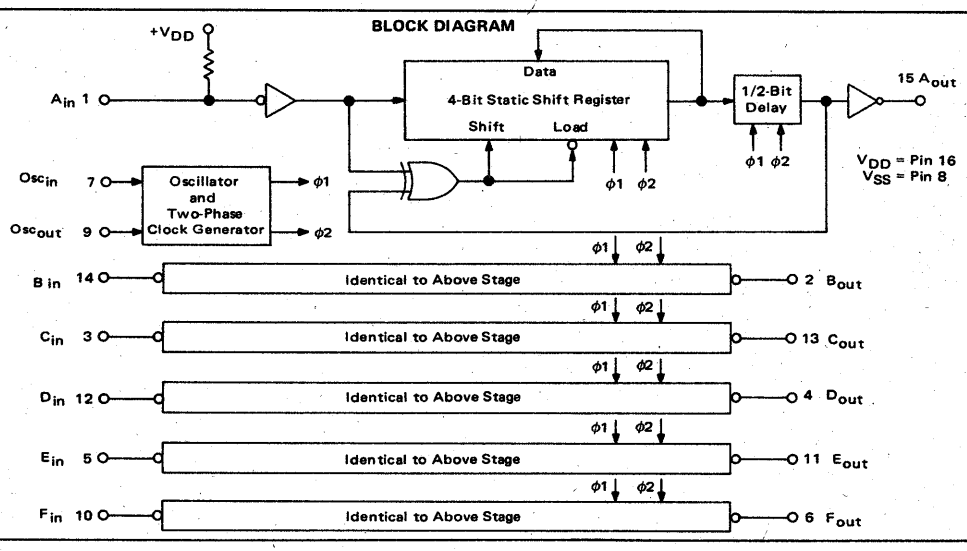
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14490	Suffix	Denotes
	L	Ceramic Package
	P	Plastic Package
	F	*Extended Operating Voltage Range
	V	*Limited Operating Voltage Range
	Blank	**Standard Operating Temperature Range
	E	**Extended Operating Temperature Range

*See Features (above, left)
**See Maximum Ratings

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage – MC14490EFL/FL/FP – MC14490EVL/VL/VP	V_{DD}	 +18 to -0.5 +6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range MC14490EFL/EVL MC14490FL/FP/VL/VP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}** Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.02	–	0	0.02	–	0.10	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current ***	I_{OH}									mAdc
Source										
Oscillator Output										
(V_{OH} = 2.5 Vdc)		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
Debounce Outputs										
(V_{OH} = 2.5 Vdc)		5.0	-0.60	–	-0.50	-2.6	–	-0.4	–	
(V_{OH} = 9.5 Vdc)		10	-0.60	–	-0.50	-1.4	–	-0.4	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-5.4	–	-1.2	–	
Sink	I_{OL}									mAdc
Oscillator Output										
(V_{OL} = 0.4 Vdc)		5.0	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.4	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Debounce Outputs										
(V_{OL} = 0.4 Vdc)		5.0	2.4	–	2.2	4.0	–	1.8	–	
(V_{OL} = 0.5 Vdc)		10	4.0	–	3.3	10	–	2.7	–	
(V_{OL} = 1.5 Vdc)		15	12	–	10	40	–	8.1	–	
Input Leakage Currents	I_{IH}									pAdc
Debounce Inputs ($V_{IH} = V_{DD}$)		–	–	–	–	10	–	–	–	
Pullup Resistor Source Current	I_{IL}									μAdc
Debounce Inputs		5.0	210	375	140	190	255	70	130	
($V_{IL} = V_{SS}$)		10	415	740	280	380	500	145	265	
		15	610	1100	415	570	750	215	400	
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Current	I_{DD}									μAdc
		5.0	–	150	–	40	120	–	100	
		10	–	280	–	75	225	–	180	
		15	–	840	–	225	675	–	550	

*T_{low} = -55°C for MC14490EFL, EVL; -40°C for MC14490FL, FP, VL, VP.
T_{high} = +125°C for MC14490EFL, EVL; +85°C for MC14490FL, FP, VL, VP.
**Only 5-volt specifications apply to MC14490EVL, VL, VP devices.
***Care must be taken not to exceed maximum current ratings (See Maximum Ratings Table and Figure 2).

ELECTRICAL CHARACTERISTICS (C_L = 15 pF)

Characteristic	Symbol	V_{DD}** Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Rise Time	t_r									ns
All Outputs		5.0	–	–	–	70	–	–	–	
		10	–	–	–	35	–	–	–	
		15	–	–	–	25	–	–	–	
Output Fall Time	t_f									ns
Oscillator Output		5.0	–	–	–	70	–	–	–	
		10	–	–	–	35	–	–	–	
		15	–	–	–	25	–	–	–	
Debounce Outputs		5.0	–	–	–	50	–	–	–	ns
		10	–	–	–	25	–	–	–	
		15	–	–	–	18	–	–	–	
Propagation Delay Time	t_{PHL}									ns
Oscillator Input to		5.0	–	–	–	625	–	–	–	
Debounce Outputs		10	–	–	–	250	–	–	–	
		15	–	–	–	200	–	–	–	
	t_{PLH}	5.0	–	–	–	700	–	–	–	ns
		10	–	–	–	275	–	–	–	
		15	–	–	–	200	–	–	–	
Maximum Clock Frequency	PRF									MHz
(50% Duty Cycle)		5.0	–	–	–	0.4	–	–	–	
		10	–	–	–	1.0	–	–	–	
		15	–	–	–	1.3	–	–	–	
Minimum Setup Time	t_{setup}	5.0	–	–	–	200	–	–	–	ns
(See Figure 1)		10	–	–	–	40	–	–	–	
		15	–	–	–	30	–	–	–	
Maximum External Clock Input	t_r,t_f									ns
Rise and Fall Time		5.0	–	–	–	∞	–	–	–	
Oscillator Input		10	–	–	–	∞	–	–	–	
		15	–	–	–	∞	–	–	–	
Typical Oscillator Frequency	f_{osc}	–	$f = \frac{0.375\ V_{DD}}{C_{ext}}$ (V_{DD} in Vdc, C_{ext} in pF)							MHz

*T_{low} = -55°C for MC14490 EFL, EVL; -40°C for MC14490FL, FP, VL, VP.
T_{high} = +125°C for MC14490 EFL, EVL; +85°C for MC14490FL, FP, VL, VP
**Only 5-volt specifications apply to MC14490 EVL, VL, VP devices.

FIGURE 1 – TYPICAL SWITCHING TIME WAVEFORMS

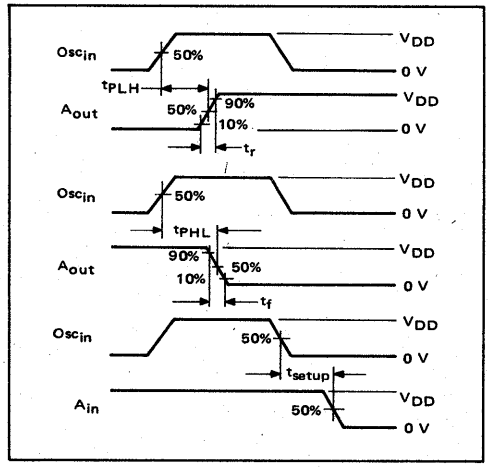
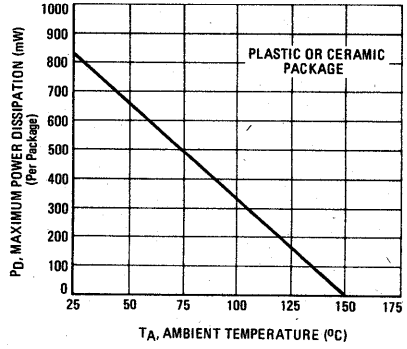


FIGURE 2 – AMBIENT TEMPERATURE POWER DERATING



THEORY OF OPERATION

The MC14490 Hex Contact Bounce Eliminator is basically a digital integrator. The circuit can integrate both up and down. This enables the circuit to eliminate bounce on both the leading and trailing edges of the signal, shown in the timing diagram of Figure 3.

Each of the six Bounce Eliminators is composed of a 4½-bit register (the integrator) and logic to compare the input with the contents of the shift register, as shown in Figure 4. The shift register requires a series of timing pulses in order to shift the input signal into each shift register location. These timing pulses (the clock signal) are represented in the upper waveform of Figure 3. Each of the six Bounce Eliminator circuits has an internal resistor as shown in Figure 4. A pullup resistor was incorporated rather than a pulldown resistor in order to implement switched ground input signals, such as those coming from relay contacts and push buttons. By switching ground, rather than a power supply lead, system faults (such as shorts to ground on the signal input leads) will not cause excessive currents in the wiring and contacts. Signal lead shorts to ground are much more probable than shorts to a power supply lead.

When the relay contact is open the shift register is loaded with a 1 (positive logic assumed) on each positive edge of the clock signal. To understand the operation, we assume all bits of the shift register are loaded with 1's and the output is at a 1 or high level.

At clock edge 1 (Figure 3) the input has gone low and a 0 (low level) has been loaded into the first bit or storage location of the shift register. Just after the positive edge of clock 1 the input signal has bounced back to a logic 1. This causes the shift register to be reset to all 1's in all four bits — thus starting the timing sequence over again.

During clock edges 3 to 6 the input signal has stayed low. Thus a logic 0 has been shifted into all four shift register bits and, as shown, the output goes to a 0 during the positive edge of clock pulse 6.

It should be noted that there is a 3½ to 4½ clock period delay between the clean input signal and output signal. In this example there is a delay of 3.8 clock periods from the beginning of the clean input signal.

After some time period of N clock periods, the contact is opened and at N+7 a 1 is loaded into the first bit. Just after N+7, when the input bounces low, all bits are reset to 0. At N+8 nothing happens because the input and output are low and all bits of the shift register are 0. At time N+9 and thereafter the input signal is a high (1) clean signal. At N+13 the output goes high (1) as a result of four 1's being shifted into the shift register.

Assuming the input signal is long enough to be clocked through the Bounce Eliminator, the output signal will be no longer or shorter than the clean input signal plus or minus one clock period.

The amount of time distortion between the input and output signals is a function of the difference in bounce characteristics on the edges of the input signal and the clock frequency. Since most relay contacts have more bounce when making as compared to breaking, the overall delay, counting bounce period, will be greater on the leading edge of the input signal than on the trailing edge. Thus, the output signal will be shorter than the input signal — if you include the leading edge bounce in the overall timing calculation.

The only requirement on the clock frequency in order to obtain a bounce free output signal is that four clock periods do not occur while the input signal is in a false state. Referring to Figure 3, a false state is seen to occur three times at the beginning of the input signal. The input signal goes low three times before it finally settles down to a valid low state. The first three low pulses are referred to as false states.

If the user has an available clock signal of the proper frequency, it may be used by connecting it to the oscillator input (pin 7). However, if an external clock is not available the user can place a small capacitor across the oscillator input and output pins in order to start up an internal clock source (as shown in Figure 4). The clock signal at the oscillator output pin may then be used to clock other MC14490 Bounce Eliminator packages. With the use of the MC14490, a large number of signals can be cleaned up, with the requirement of only one small capacitor external to the Hex Bounce Eliminator packages.

FIGURE 3 – TIMING DIAGRAM

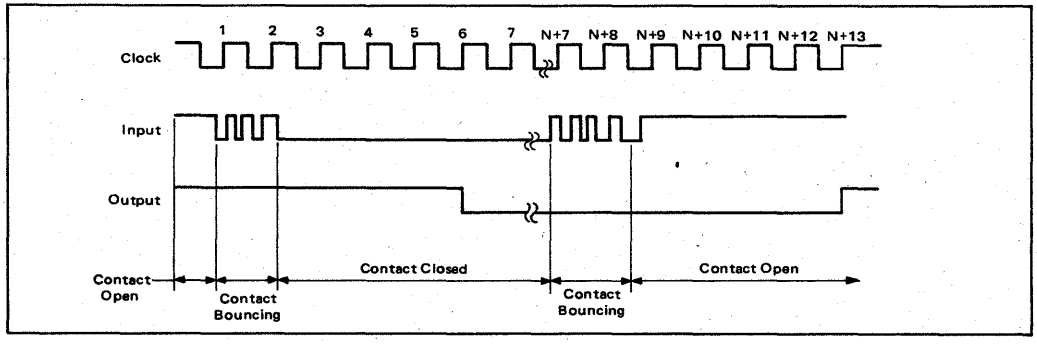
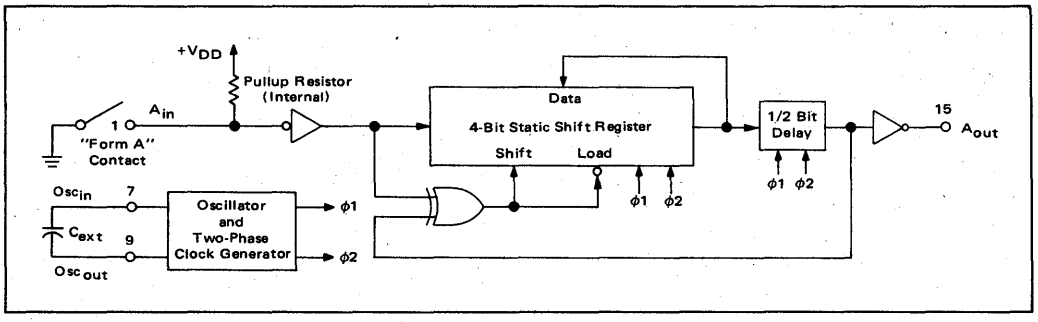


FIGURE 4 – TYPICAL "FORM A" CONTACT DEBOUNCE CIRCUIT
(Only One Debouncer Shown)



OPERATING CHARACTERISTICS

The single most important characteristic of the MC14490 is that it works with a single signal lead as an input, making it directly compatible with mechanical contacts (Form A and B).

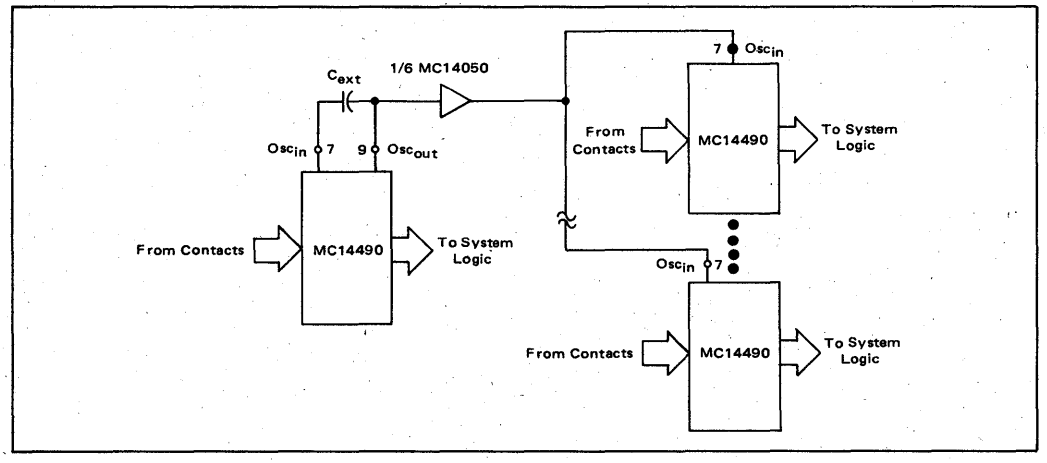
The circuit has a built in pullup resistor on each input. The worst case value of the pullup resistor (determined from the Electrical Characteristics table) is used to calculate the contact wetting current. If more contact current is required, an external resistor may be connected between V_{DD} and the input.

Because of the built in pullup resistors, the inputs cannot be driven with a single standard CMOS gate when V_{DD} is below 5 V. At this voltage, the input should be driven with paralleled standard gates or by the MC14049 or MC14050 buffers.

The clock input circuit (pin 7) has Schmitt trigger shaping such that proper clocking will occur even with very slow clock edges, eliminating any need for clock preshaping. In addition, other MC14490 oscillator inputs can be driven from a single oscillator output buffered by an MC14050 (see Figure 5).

The MC14490 is TTL compatible on both the inputs and the outputs. When V_{DD} is at 4.5 V, the buffered outputs can sink 1.6 mA at 0.4 V. The inputs can be driven with TTL as a result of the internal input pullup resistors.

FIGURE 5 – TYPICAL SINGLE OSCILLATOR
DEBOUNCE SYSTEM

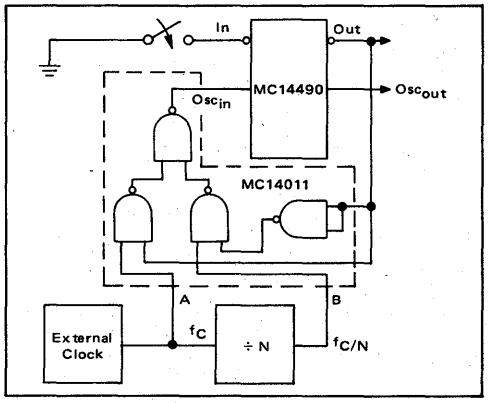


TYPICAL APPLICATIONS

ASYMMETRICAL TIMING

In applications where different leading and trailing edge delays are required (such as a fast attack/slow release timer.) Clocks of different frequencies can be gated into the MC14490 as shown in Figure 6. In order to produce a slow attack/fast release circuit leads A and B should be interchanged. The clock out lead can then be used to feed clock signals to the other MC14490 packages where the asymmetrical input/output timing is required.

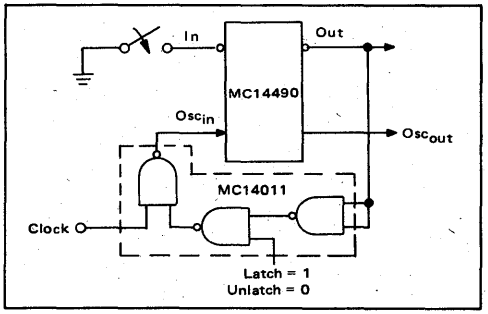
FIGURE 6 – FAST ATTACK/SLOW RELEASE CIRCUIT



LATCHED OUTPUT

The contents of the Bounce Eliminator can be latched by using several extra gates as shown in Figure 7. If the latch lead is high the clock will be stopped when the output goes low. This will hold the output low even though the input has returned to the high state. Any time the clock is stopped the outputs will be representative of the input signal four clock periods earlier.

FIGURE 7 – LATCHED OUTPUT CIRCUIT



MULTIPLE TIMING SIGNALS

As shown in Figure 8, the Bounce Eliminator circuits can be connected in series. In this configuration each output is delayed by four clock periods relative to its respective input. This configuration may be used to generate multiple timing signals such as a delay line, for programming other timing operations.

One application of the above is shown in Figure 9, where it is required to have a single pulse output for a single operation (make) of the push button or relay contact. This only requires the series connection of two Bounce Eliminator circuits, one inverter, and one NOR gate in order to generate the signal $A\overline{B}$ as shown in Figures 9 and 10. The signal $A\overline{B}$ is four clock periods in length. If the inputs to the NOR gate are interchanged the pulse $\overline{A}B$ will be generated upon release or break of the contact. With the use of a few additional parts many different pulses and waveshapes may be generated.

FIGURE 8 – MULTIPLE TIMING CIRCUIT CONNECTIONS

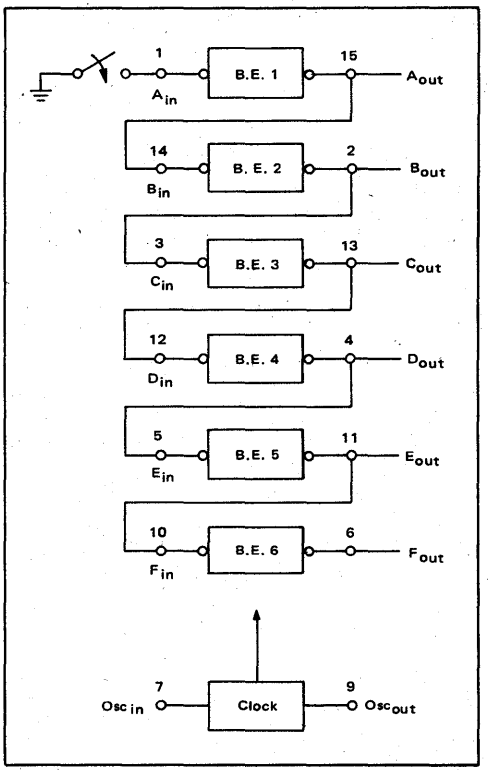
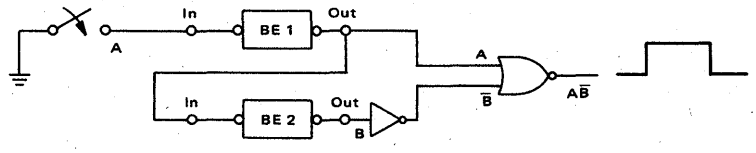
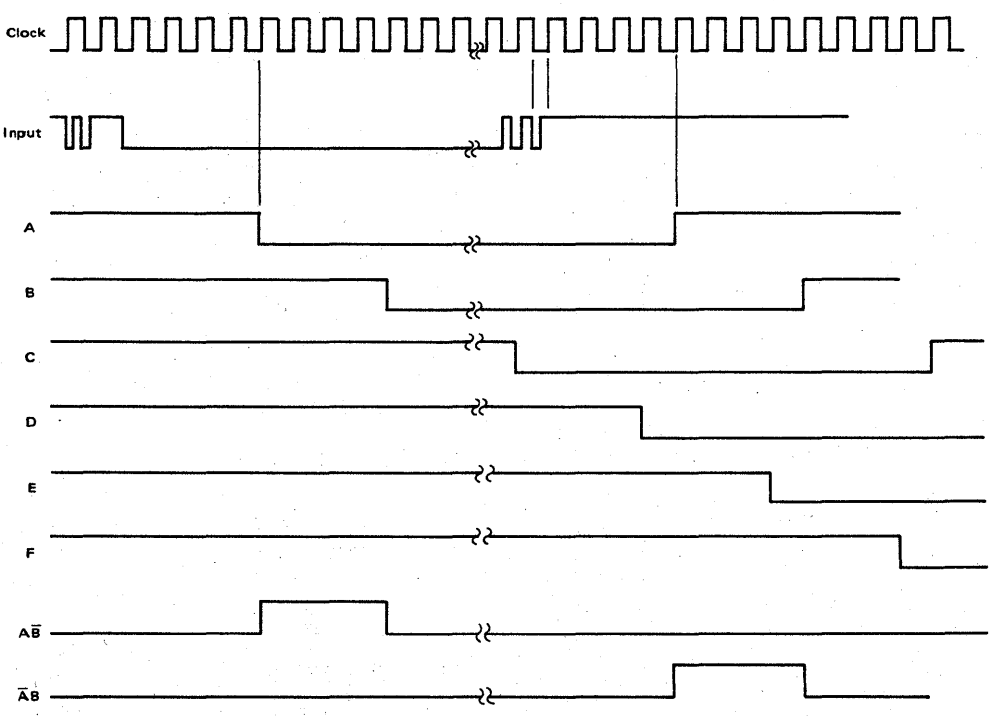


FIGURE 9 – SINGLE PULSE OUTPUT CIRCUIT



A ≡ Active Low
B ≡ Active Low

FIGURE 10 – MULTIPLE OUTPUT SIGNAL TIMING DIAGRAM



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14501

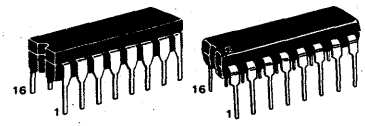
TRIPLE GATE
DUAL 4-INPUT "NAND" GATE
2-INPUT "NOR/OR" GATE
8-INPUT "AND/NAND" GATE

The MC14501 is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family Data Sheet.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

McMOS SSI
(LOW-POWER COMPLEMENTARY MOS)

TRIPLE GATE
DUAL 4-INPUT "NAND" GATE
2-INPUT "NOR/OR" GATE
8-INPUT "AND/NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

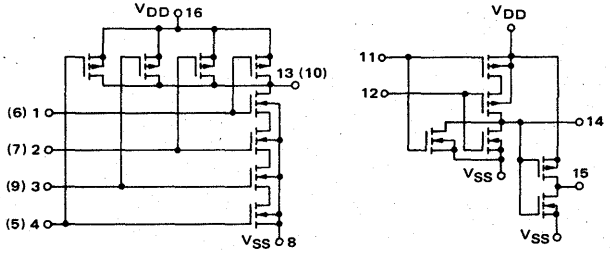
ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

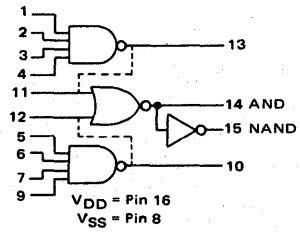
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



Numbers in parenthesis are for second 4-input gate.

LOGIC DIAGRAM
(POSITIVE LOGIC)



Use Dotted Connection Externally to Obtain 8-Input AND/NAND

Note: Pin 14 must not be used as an input to the inverter.

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.4	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	2.9	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.6	
(V_O = 1.4 or 3.6 Vdc) "1" Level	V_{IH}	5.0	3.6	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 2.8 or 7.2 Vdc)		10	7.1	–	7.0	5.50	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.4	–	11.25	8.25	–	11.0	–	
Output Drive Current	I_{OH}									mAdc
(AL Device)										
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc) NAND		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OH} = 2.5 Vdc) NOR		5.0	–2.1	–	–1.75	–3.0	–	–1.22	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	–0.42	–	–0.35	–0.63	–	–0.24	–	
(V_{OH} = 9.5 Vdc)		10	–1.06	–	–0.88	–1.58	–	–0.62	–	
(V_{OH} = 13.5 Vdc)		15	–3.1	–	–2.63	–6.12	–	–1.84	–	
(V_{OH} = 2.5 Vdc) NOR-		5.0	–3.6	–	–3.0	–5.1	–	–2.1	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	–0.72	–	–0.6	–1.08	–	–0.42	–	
(V_{OH} = 9.5 Vdc) Inverter		10	–1.8	–	–1.5	–2.7	–	–1.05	–	
(V_{OH} = 13.5 Vdc)		15	–5.4	–	–4.5	–10.5	–	–3.15	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc) NAND		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
(V_{OL} = 0.4 Vdc) NOR		5.0	0.92	–	0.77	1.32	–	0.54	–	mAdc
(V_{OL} = 0.5 Vdc)		10	2.34	–	1.95	3.37	–	1.36	–	
(V_{OL} = 1.5 Vdc)		15	6.12	–	5.1	13.2	–	3.57	–	
(V_{OL} = 0.4 Vdc) NOR-		5.0	1.54	–	1.28	2.2	–	0.90	–	mAdc
(V_{OL} = 0.5 Vdc) Inverter		10	3.90	–	3.25	5.63	–	2.27	–	
(V_{OL} = 1.5 Vdc)		15	10.2	–	8.5	22	–	5.95	–	
Output Drive Current	I_{OH}									mAdc
(CL/CP Device)										
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc) NAND		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OH} = 2.5 Vdc) NOR		5.0	–1.68	–	–1.4	–3.0	–	–1.05	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	–0.34	–	–0.28	–0.63	–	–0.21	–	
(V_{OH} = 9.5 Vdc)		10	–0.84	–	–0.7	–1.58	–	–0.52	–	
(V_{OH} = 13.5 Vdc)		15	–2.52	–	–2.1	–6.12	–	–1.57	–	
(V_{OH} = 2.5 Vdc) NOR-		5.0	–2.88	–	–2.4	–5.1	–	–1.8	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	–0.58	–	–0.48	–1.08	–	–0.36	–	
(V_{OH} = 9.5 Vdc) Inverter		10	–1.44	–	–1.2	–2.7	–	–0.9	–	
(V_{OH} = 13.5 Vdc)		15	–4.32	–	–3.6	–10.5	–	–2.7	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc) NAND		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
(V_{OL} = 0.4 Vdc) NOR		5.0	0.79	–	0.66	1.32	–	0.54	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.98	–	1.65	3.37	–	1.36	–	
(V_{OL} = 1.5 Vdc)		15	5.4	–	4.5	13.2	–	3.57	–	
(V_{OL} = 0.4 Vdc) NOR-		5.0	1.32	–	1.1	2.2	–	0.90	–	mAdc
(V_{OL} = 0.5 Vdc) Inverter		10	3.3	–	2.75	5.63	–	2.27	–	
(V_{OL} = 1.5 Vdc)		15	9.0	–	7.5	22.0	–	5.95	–	

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	–	0.10	–	0.0010	0.10	–	3.0	
		15	–	0.20	–	0.0015	0.20	–	6.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	0.5	–	0.0005	0.5	–	3.8	μAdc
		10	–	1.0	–	0.0010	1.0	–	7.5	
		15	–	2.0	–	0.0015	2.0	–	15	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.2\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (2.4\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (3.6\ \mu A/kHz)\ f + I_{DD}$							

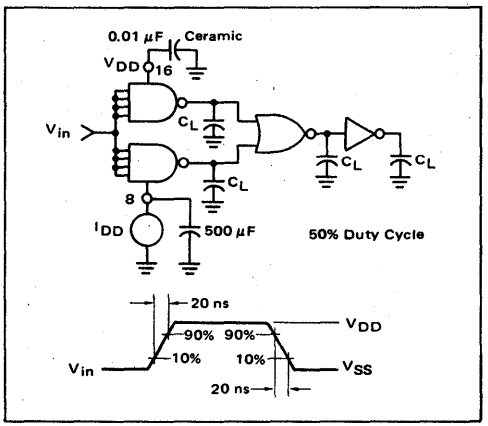
*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS** (C_L = 50 pF, T_A = 25°C)

Characteristic		Figure	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	NAND, NOR	2, 3	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns				5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns				10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns				15	65	110	160	
Output Fall Time	NAND, NOR	2, 3	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns				5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns				10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns				15	37	55	80	
Output Rise Time	NOR-Inverter	3	t_r					ns
t_r = (1.35 ns/pF) C_L + 32.5 ns				5.0	100	175	200	
t_r = (0.60 ns/pF) C_L + 20 ns				10	50	75	100	
t_r = (0.40 ns/pF) C_L + 17 ns				15	37	55	80	
Output Fall Time	NOR-Inverter	3	t_f					ns
t_f = (0.67 ns/pF) C_L + 26.5 ns				5.0	60	100	140	
t_f = (0.45 ns/pF) C_L + 17.5 ns				10	40	75	100	
t_f = (0.37 ns/pF) C_L + 11.5 ns				15	30	50	75	
Propagation Delay Time	NAND	2	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 45 ns				50	130	200	300	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 37 ns				10	70	110	175	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns				15	50	80	125	
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns	NOR	3	t_{PLH}, t_{PHL}	5.0	115	175	250	ns
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 32 ns				10	65	100	160	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 20 ns				15	45	75	100	
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 45 ns	NOR-Inverter	3	t_{PLH}, t_{PHL}	5.0	130	200	300	ns
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 37 ns				10	70	110	175	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns				15	50	80	125	

**The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 2 – 4-INPUT "NAND" GATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

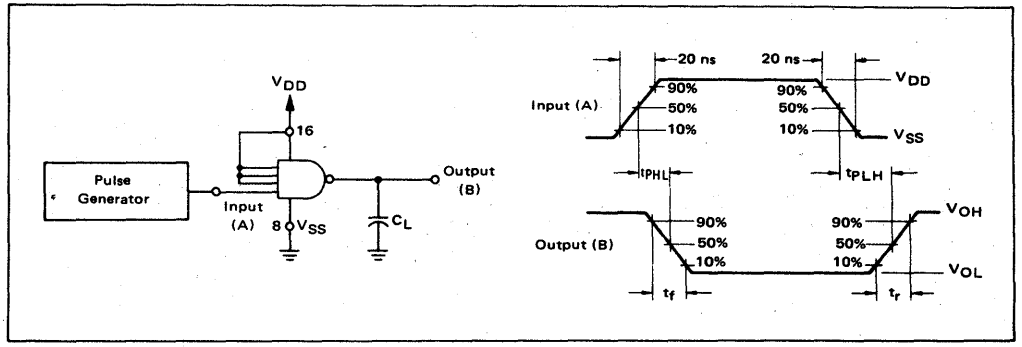
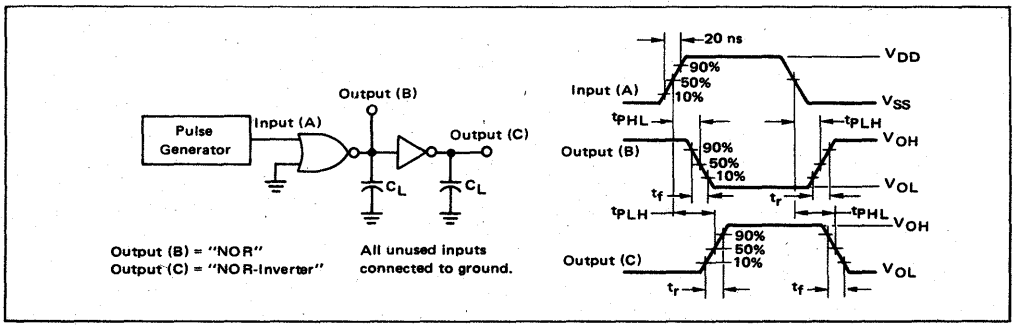


FIGURE 3 – "NOR" GATE and "NOR-INVERTER" SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14502B

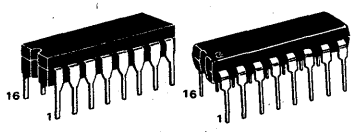
STROBED HEX INVERTER/BUFFER

The MC14502B is a strobed hex buffer/inverter with 3-state output, an inhibit control, and guaranteed TTL drive over the temperature range. The 3-state output simplifies design by allowing a common bus.

- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Separate Output Disable Control
- 3-State Output
- Output Impedance = 200 ohms @ 5.0 V Supply Guaranteed Over Full Temperature Range
- Input Impedance = 10^{12} ohms typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

McMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

STROBED HEX
INVERTER/BUFFER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

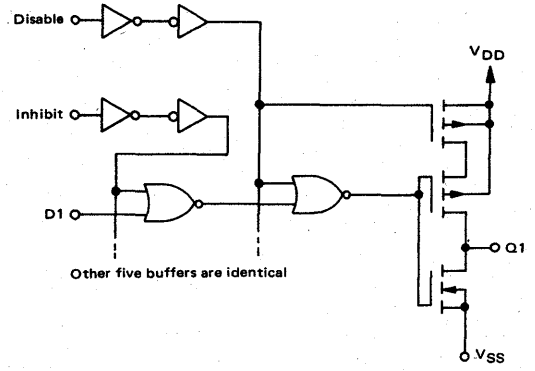
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

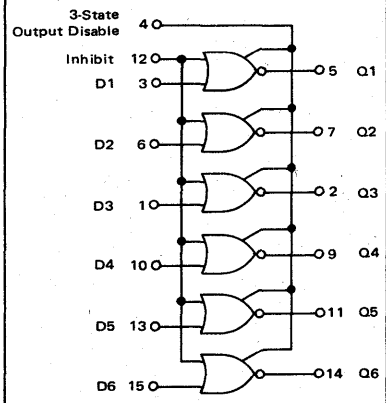
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	30	mAdc
Operating Temperature Range — AL Device	T_A	−55 to +125	°C
CL/CP Device		−40 to +85	
Storage Temperature Range	T_{stg}	−65 to +150	°C

CIRCUIT DIAGRAM



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

D_n	Inhibit	Disable	Q_n
0	0	0	1
1	0	0	0
X	1	0	0
X	X	1	High Impedance

X = Don't Care

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5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	3.5	–	2.8	6.6	–	2.0	–	mAdc
(V_{OL} = 0.5 Vdc)		10	7.8	–	6.3	17	–	4.4	–	
(V_{OL} = 1.5 Vdc)		15	29	–	24	66	–	16	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	2.3	–	1.9	6.6	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	5.0	–	4.2	17	–	3.4	–	
(V_{OL} = 1.5 Vdc)		15	19	–	16	66	–	13	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (2.7 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (5.3 μA/kHz) f + I_{DD}							
		15	I_T = (8.0 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types Min	All Types Typ	All Types Max	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_f					ns
t_f = (0.6 ns/pF) C_L + 10 ns		5.0	–	40	80	
t_f = (0.3 ns/pF) C_L + 5.0 ns		10	–	20	40	
t_f = (0.27 ns/pF) C_L + 1.5 ns		15	–	15	30	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.38 ns/pF) C_L + 116 ns		5.0	–	135	270	
t_{PHL} = (0.15 ns/pF) C_L + 47.5 ns		10	–	55	110	
t_{PHL} = (0.11 ns/pF) C_L + 34.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.4 ns/pF) C_L + 225 ns		5.0	–	295	590	
t_{PLH} = (0.7 ns/pF) C_L + 95 ns		10	–	130	260	
t_{PLH} = (0.3 ns/pF) C_L + 80 ns		15	–	95	190	
3-State Propagation Delay, Output "1" to High Impedance	$t_{"1"H}$					ns
$t_{"1"H}$ = (0.38 ns/pF) C_L + 46 ns		5.0	–	65	130	
$t_{"1"H}$ = (0.15 ns/pF) C_L + 22.5 ns		10	–	30	60	
$t_{"1"H}$ = (0.11 ns/pF) C_L + 19.5 ns		15	–	25	50	
3-State Propagation Delay, High Impedance to "1" Level	$t_{H"1"}$					ns
$t_{H"1"}$ = (0.38 ns/pF) C_L + 241 ns		5.0	–	260	520	
$t_{H"1"}$ = (0.15 ns/pF) C_L + 97.5 ns		10	–	105	210	
$t_{H"1"}$ = (0.11 ns/pF) C_L + 74.5 ns		15	–	80	160	
3-State Propagation Delay, Output "0" to High Impedance	$t_{"0"H}$					ns
$t_{"0"H}$ = (0.38 ns/pF) C_L + 131 ns		5.0	–	150	300	
$t_{"0"H}$ = (0.15 ns/pF) C_L + 62.5 ns		10	–	70	140	
$t_{"0"H}$ = (0.11 ns/pF) C_L + 49.5 ns		15	–	55	110	
3-State Propagation Delay, High Impedance to "0" Level	$t_{H"0"}$					ns
$t_{H"0"}$ = (0.38 ns/pF) C_L + 141 ns		5.0	–	160	320	
$t_{H"0"}$ = (0.15 ns/pF) C_L + 57.5 ns		10	–	65	130	
$t_{H"0"}$ = (0.11 ns/pF) C_L + 44.5 ns		15	–	50	100	

*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT TEST CIRCUIT (I_{OH})

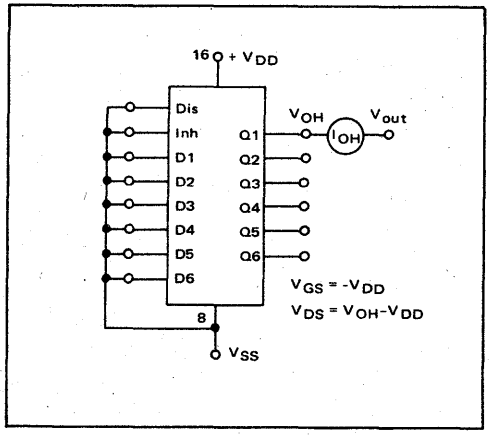


FIGURE 2 – TYPICAL OUTPUT SINK CURRENT TEST CIRCUIT (I_{OL})

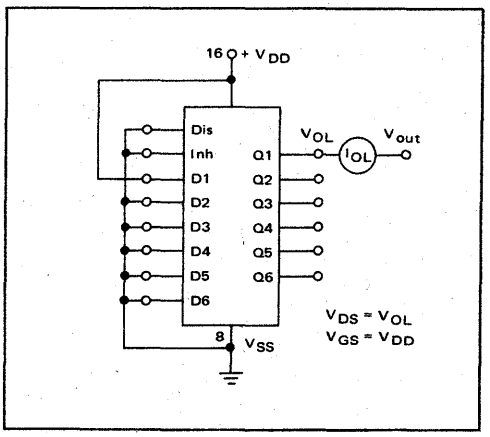


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

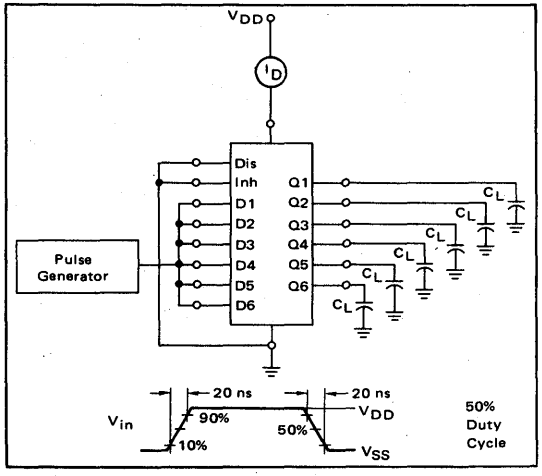


FIGURE 4 – AMBIENT TEMPERATURE POWER DERATING

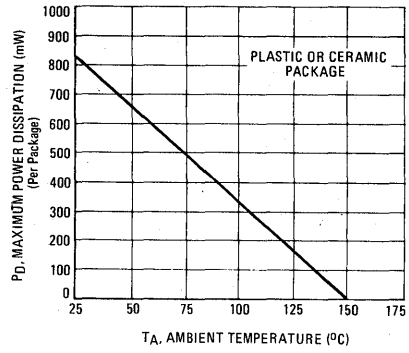


FIGURE 5 – AC TEST CIRCUIT AND WAVEFORMS
(t_r, t_f, t_{PHL}, and t_{PLH})

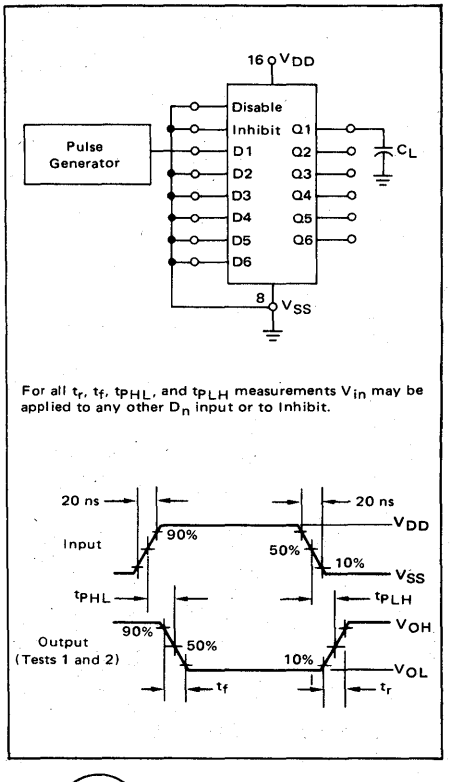
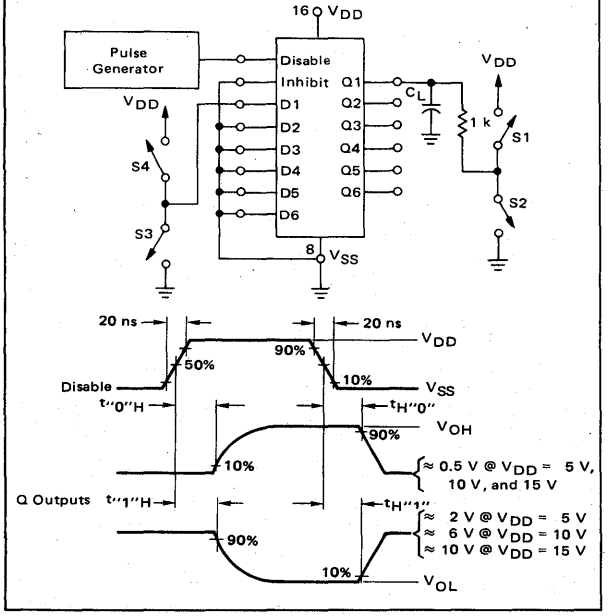


FIGURE 6 – 3-STATE AC TEST CIRCUIT AND WAVEFORMS
($t_{"1"H}$, $t_{H"1"}$, $t_{"0"H}$, $t_{H"0"}$)

Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
$t_{"1"H}$	Open	Closed	Closed	Open
$t_{"0"H}$	Closed	Open	Open	Closed
$t_{H"0"}$	Closed	Open	Open	Closed
$t_{H"1"}$	Open	Closed	Closed	Open



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14503B

HEX NON-INVERTING 3-STATE BUFFER

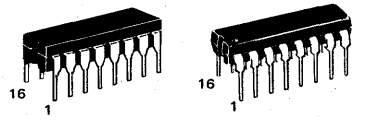
The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

- 3-State Outputs
- TTL Compatible — Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Symmetrical Turn-On and Turn-off Delays
- Symmetrical Output Rise and Fall Times
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX 3-STATE BUFFER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

Suffix	Denotes
L	Ceramic Package
P	Plastic Package
A	Extended Operating Temperature Range
C	Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

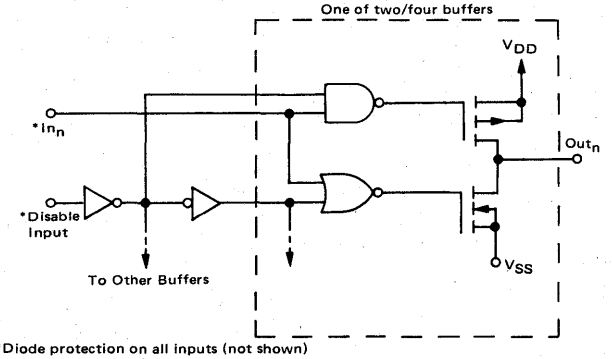
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	25	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

TRUTH TABLE

In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

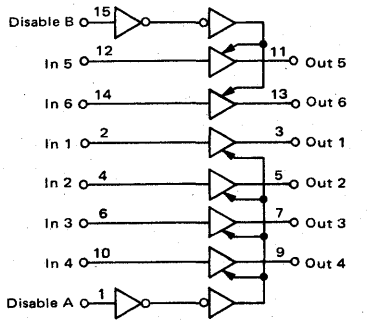
X = Don't Care

CIRCUIT DIAGRAM



*Diode protection on all inputs (not shown)

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Noise Immunity# "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.75	
"1" Level										
(V_O = 1.4 or 3.6 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 2.8 or 7.2 Vdc)		10	7.0	–	7.0	5.5	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.25	–	11.25	8.25	–	11.25	–	
Output Drive Current (AL Device)***	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		4.5	-4.55	–	-3.6	-6.35	–	-2.60	–	
(V_{OH} = 2.5 Vdc)		5.0	-6.00	–	-4.80	-8.40	–	-3.40	–	
(V_{OH} = 4.6 Vdc)		5.0	-1.28	–	-1.02	-1.76	–	-0.72	–	
(V_{OH} = 9.5 Vdc)		10	-3.20	–	-2.60	-4.50	–	-1.80	–	
(V_{OH} = 13.5 Vdc)		15	-8.20	–	-6.80	-17.60	–	-4.80	–	
Sink	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		4.5	2.80	–	2.30	2.55	–	1.60	–	
(V_{OL} = 0.4 Vdc)		5.0	3.00	–	2.40	2.75	–	1.75	–	
(V_{OL} = 0.5 Vdc)		10	7.85	–	6.35	7.00	–	4.45	–	
(V_{OL} = 1.5 Vdc)		15	19.95	–	16.10	25.00	–	11.30	–	
Output Drive Current (CL/CP Device)***	I_{OH}						–			mAdc
(V_{OH} = 2.5 Vdc) Source		4.75	-4.30	–	-3.60	-7.25	–	-2.60	–	
(V_{OH} = 2.5 Vdc)		5.0	-5.00	–	-4.20	-8.40	–	-3.40	–	
(V_{OH} = 4.6 Vdc)		5.0	-1.04	–	-0.88	-1.76	–	-0.72	–	
(V_{OH} = 9.5 Vdc)		10	-2.60	–	-2.20	-4.50	–	-1.80	–	
(V_{OH} = 13.5 Vdc)		15	-7.20	–	-6.00	-17.60	–	-4.80	–	
Sink	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		4.75	2.30	–	1.95	2.65	–	1.60	–	
(V_{OL} = 0.4 Vdc)		5.0	2.50	–	2.10	2.75	–	1.75	–	
(V_{OL} = 0.5 Vdc)		10	6.50	–	5.45	7.00	–	4.45	–	
(V_{OL} = 1.5 Vdc)		15	16.50	–	13.80	25.00	–	11.30	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±3.0	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_Q	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**†	I_{DD}	5.0	(I_T = 2.5 μA/kHz) f + I_{DD}							μAdc
(Dynamic plus Quiescent, Per Package)		10	(I_T = 6.0 μA/kHz) f + I_{DD}							
(C_L = 50 pF on all outputs)		15	(I_T = 10 μA/kHz) f + I_{DD}							
(All outputs switching, 50% Duty Cycle)										
3-State Output Leakage Current	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	μAdc
(AL Device)			–		–			–		
3-State Output Leakage Current	I_{TL}	15	–	±1.0	–	±0.0001	±1.0	–	±7.5	μAdc
(CL/CP Device)			–		–			–		

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$$

I_T is in μA (per package) C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C
***Care must be taken not to exceed maximum current ratings (see maximum ratings table and Figure 1).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V_{CC}	All Types Typ	All Types Max	Unit
Output Rise Time	t_r				ns
t_r = (0.5 ns/pF) C_L + 20 ns		5.0	45	60	
t_r = (0.3 ns/pF) C_L + 8.0 ns		10	23	30	
t_r = (0.2 ns/pF) C_L + 8.0 ns		15	18	25	
Output Fall Time	t_f				ns
t_f = (0.5 ns/pF) C_L + 20 ns		5.0	45	60	
t_f = (0.3 ns/pF) C_L + 8.0 ns		10	23	30	
t_f = (0.2 ns/pF) C_L + 8.0 ns		15	18	25	
Turn-Off Delay Time, all Outputs	t_{PLH}				ns
t_{PLH} = (0.3 ns/pF) C_L + 60 ns		5.0	75	100	
t_{PLH} = (0.15 ns/pF) C_L + 27 ns		10	35	40	
t_{PLH} = (0.1 ns/pF) C_L + 20 ns		15	25	30	
Turn-On Delay Time, all Outputs	t_{PHL}				ns
t_{PHL} = (0.3 ns/pF) C_L + 60 ns		5.0	75	100	
t_{PHL} = (0.15 ns/pF) C_L + 27 ns		10	35	40	
t_{PHL} = (0.1 ns/pF) C_L + 20 ns		15	25	30	
3-State Propagation Delay Time	$t_{"1"H}$				ns
Output "1" to High Impedance					
$t_{"1"H}$ = (0.12 ns/pF) C_L + 69 ns		5.0	75	110	
$t_{"1"H}$ = (0.12 ns/pF) C_L + 34 ns		10	40	60	
$t_{"1"H}$ = (0.12 ns/pF) C_L + 29 ns		15	35	45	
Output "0" to High Impedance	$t_{"0"H}$				ns
$t_{"0"H}$ = (0.12 ns/pF) C_L + 74 ns		5.0	80	120	
$t_{"0"H}$ = (0.12 ns/pF) C_L + 34 ns		10	40	60	
$t_{"0"H}$ = (0.12 ns/pF) C_L + 29 ns		15	35	50	
High Impedance to "1" Level	$t_{H"1"}$				ns
$t_{H"1"}$ = (0.09 ns/pF) C_L + 6 ns		5.0	65	100	
$t_{H"1"}$ = (0.06 ns/pF) C_L + 22 ns		10	25	40	
$t_{H"1"}$ = (0.03 ns/pF) C_L + 19 ns		15	20	30	
High Impedance to "0" Level	$t_{H"0"}$				ns
$t_{H"0"}$ = (0.09 ns/pF) C_L + 95 ns		5.0	100	150	
$t_{H"0"}$ = (0.06 ns/pF) C_L + 32 ns		10	35	50	
$t_{H"0"}$ = (0.03 ns/pF) C_L + 24 ns		15	25	40	

*The formulas given are for the typical characteristics only.

FIGURE 1 – AMBIENT TEMPERATURE POWER DERATING

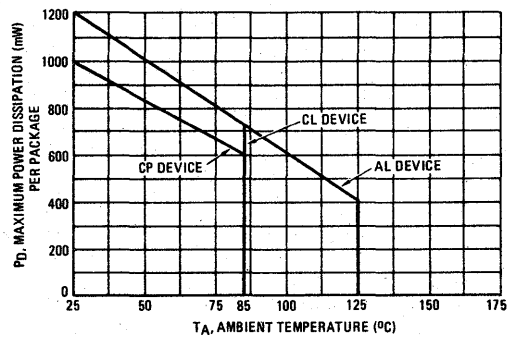


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(t_r, t_f, t_{PHL}, and t_{PLH})

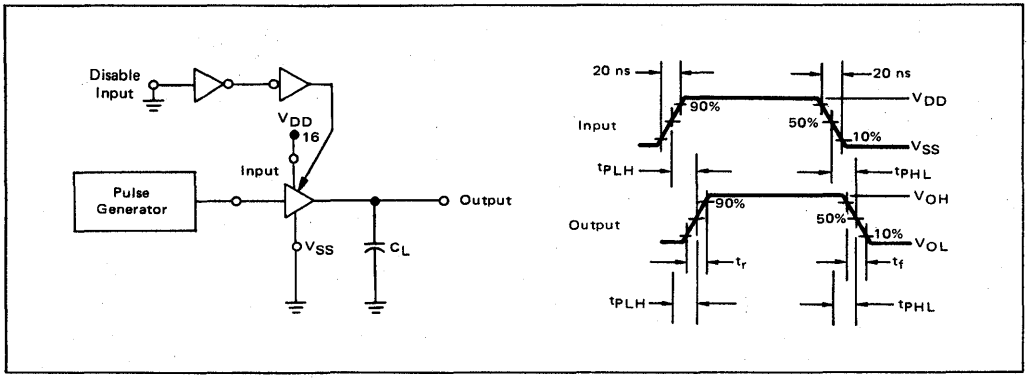
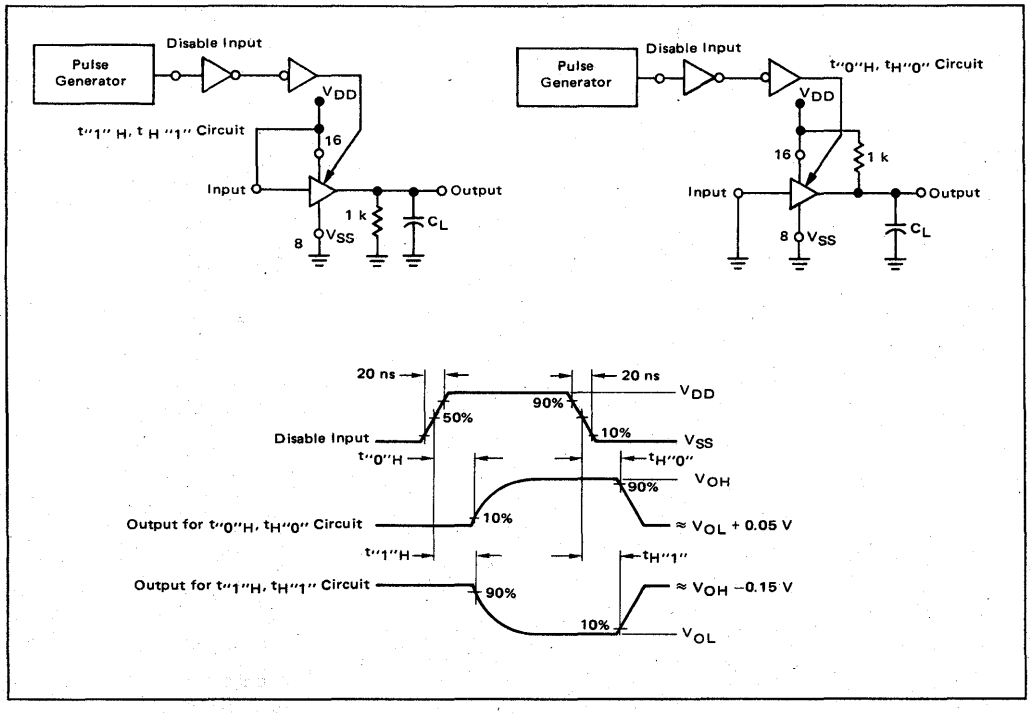


FIGURE 3 – 3 STATE AC TEST CIRCUITS AND WAVEFORMS
(t "1"H, t H "1", t "O " H, t H "O")



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MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MCM14505

McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

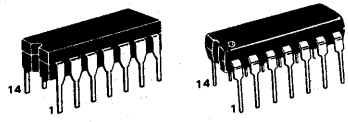
64-BIT (64 x 1) STATIC RANDOM ACCESS MEMORY

64-BIT STATIC RANDOM ACCESS MEMORY

The MCM14505 64-bit random access memory is fully decoded on the chip and organized as 64 one-bit words (64 X 1). Medium speed operation and micropower supply requirements make this device useful for scratch pad or buffer memory applications where power must be conserved or where battery operation is required.

When used with a battery backup, the MCM14505 can be utilized as an alterable read-only memory, allowing the battery to retain information in the memory when the system is powered down, and allowing the battery to charge when power is applied. The micropower requirements of this memory allow quiescent battery operation for great lengths of time without significant discharging.

- Quiescent Current = 5.0mA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Read/Write Control Line
- Wired-OR Output Capability (3-State Output) for Memory Expansion
- Access Time = 180 ns typical at V_{DD} = 10 Vdc
- Write Cycle Time = 275 ns typical at V_{DD} = 10 Vdc
- Fully Buffered Low Capacitance Inputs
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

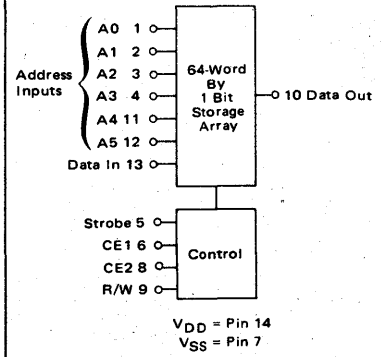
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Noise Immunity #	V_{NL}									Vdc
($\Delta V_{out} \leq$ 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq$ 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq$ 1.5 Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq$ 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq$ 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq$ 1.5 Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.3	–	0.25	0.35	–	0.18	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.9	–	0.75	1.2	–	0.50	–	
(V_{OL} = 1.5 Vdc)		15	2.2	–	1.7	4.5	–	1.2	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.2	–	0.15	0.35	–	1.0	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.6	–	0.5	1.2	–	4.0	–	
(V_{OL} = 1.5 Vdc)		15	3.9	–	0.75	4.5	–	6.0	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±1.0	–	±0.00001	±1.0	–	±14	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.050	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.100	10	–	300	
		15	–	20	–	0.150	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.050	50	–	375	μAdc
(Per Package)		10	–	100	–	0.100	100	–	750	
		15	–	200	–	0.150	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.28 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.56 μA/kHz) f + I_{DD}							
		15	I_T = (3.85 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ	Max		Unit
			All Types	AL Device	CL/CP Device	
Output Rise Time	t_r					ns
t_r = (2.43 ns/pF) C_L + 58.5 ns		5.0	180	360	360	
t_r = (1.08 ns/pF) C_L + 36 ns		10	90	180	180	
t_r = (0.72 ns/pF) C_L + 39 ns		15	75	150	150	
Output Fall Time	t_f					ns
t_f = (2.16 ns/pF) C_L + 52 ns		5.0	160	320	320	
t_f = (0.96 ns/pF) C_L + 32 ns		10	80	160	160	
t_f = (0.69 ns/pF) C_L + 33 ns		15	65	130	130	
Propagation Delay Time	$t_{acc(R)}$					ns
Read Access Time						
$t_{acc(R)}$ = (1.4 ns/pF) C_L + 385 ns		5.0	455	640	750	
$t_{acc(R)}$ = (10.7 ns/pF) C_L + 175 ns		10	210	215	400	
$t_{acc(R)}$ = (0.5 ns/pF) C_L + 105 ns		15	130	235	300	
Minimum Strobe Down Time	t_{STL}					ns
		5.0	100	400	500	
		10	50	100	125	
		15	75	80	95	
Address Setup Time	$t_{setup(A)}$					ns
		5.0	−100	200	300	
		10	−40	80	120	
		15	−25	60	90	
Data Setup Time	$t_{setup(D)}$					ns
		5.0	70	140	200	
		10	25	50	75	
		15	20	40	55	
Read Setup Time	$t_{setup(R)}$					ns
		5.0	90	180	270	
		10	20	40	60	
		15	15	30	45	
Write Setup Time	$t_{setup(W)}$					ns
		5.0	80	275	400	
		10	25	75	100	
		15	11	55	75	
Address Release Time	$t_{rel(R)}$					ns
		5.0	15	50	75	
		10	10	15	25	
		15	5.0	10	20	
Data Hold Time	$t_{hold(D)}$					ns
		5.0	0	35	50	
		10	0	10	15	
		15	0	7.5	10	
Read Release Time	$t_{rel(R)}$					ns
		5.0	−90	0	0	
		10	−25	0	0	
		15	−10	0	0	
Write Release Time	$t_{rel(W)}$					ns
		5.0	5.0	0	0	
		10	10	0	0	
		15	30	0	0	
Read Cycle Time	$t_{cyc(R)}$					ns
		5.0	500	650	750	
		10	200	300	400	
		15	150	225	300	
Write Cycle Time	$t_{cyc(W)}$					ns
		5.0	440	600	700	
		10	275	400	550	
		15	200	300	415	
Output Disable Delay	t_{dis}					ns
(10% Output Change into 1.0 kΩ Load)		5.0	200	400	600	
		10	80	160	200	
		15	60	120	150	

*The formula is for the typical characteristics only.

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FIGURE 1 – READ CYCLE TIMING DIAGRAM

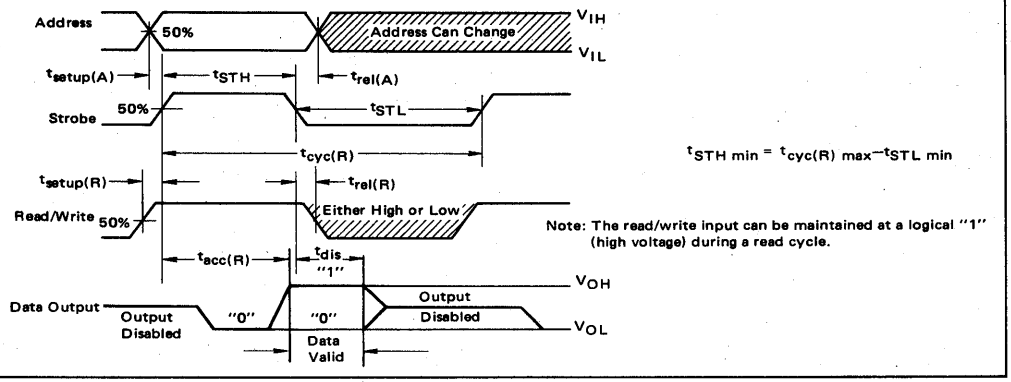

FIGURE 2 – WRITE CYCLE TIMING DIAGRAM

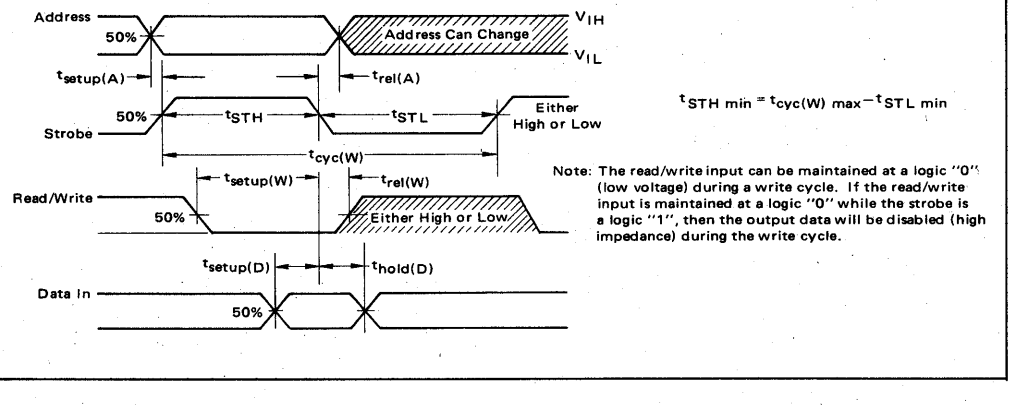

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FIGURE 3 – MAXIMUM STROBE PULSE WIDTH versus TEMPERATURE

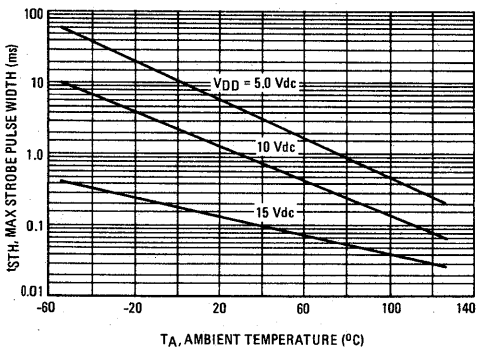


FIGURE 4 – TYPICAL READ ACCESS TIME versus LOAD CAPACITANCE

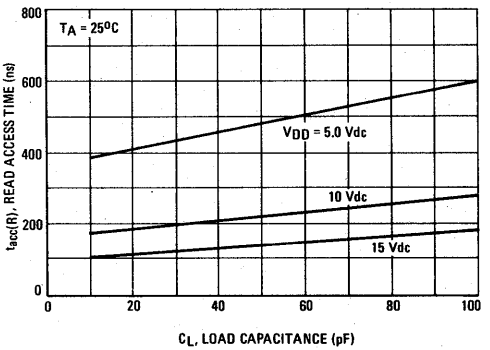
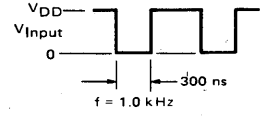
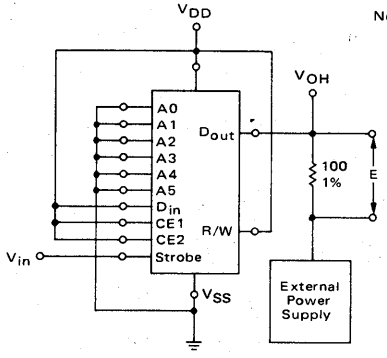


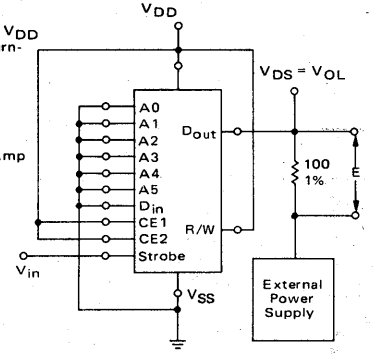
FIGURE 5 – TYPICAL OUTPUT SOURCE CAPABILITY versus TEMPERATURE

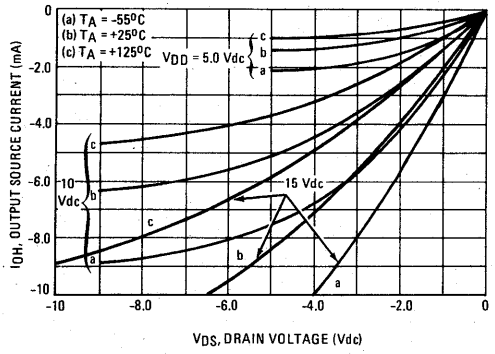
FIGURE 6 – TYPICAL OUTPUT SINK CAPABILITY versus TEMPERATURE





Notes:
1. Cycle R/W to ground and then to V_{DD} prior to measurement to insure turn-on of the device under test.
2. For the P-channel characteristics, $V_{DS} = V_{OH} - V_{DD}$.
3. For the N-channel characteristics, V_{DS} is measured directly.
4. For the drain current, $I_D = \frac{E}{100}$ Amp





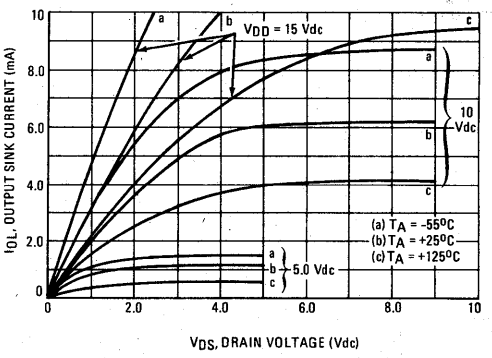


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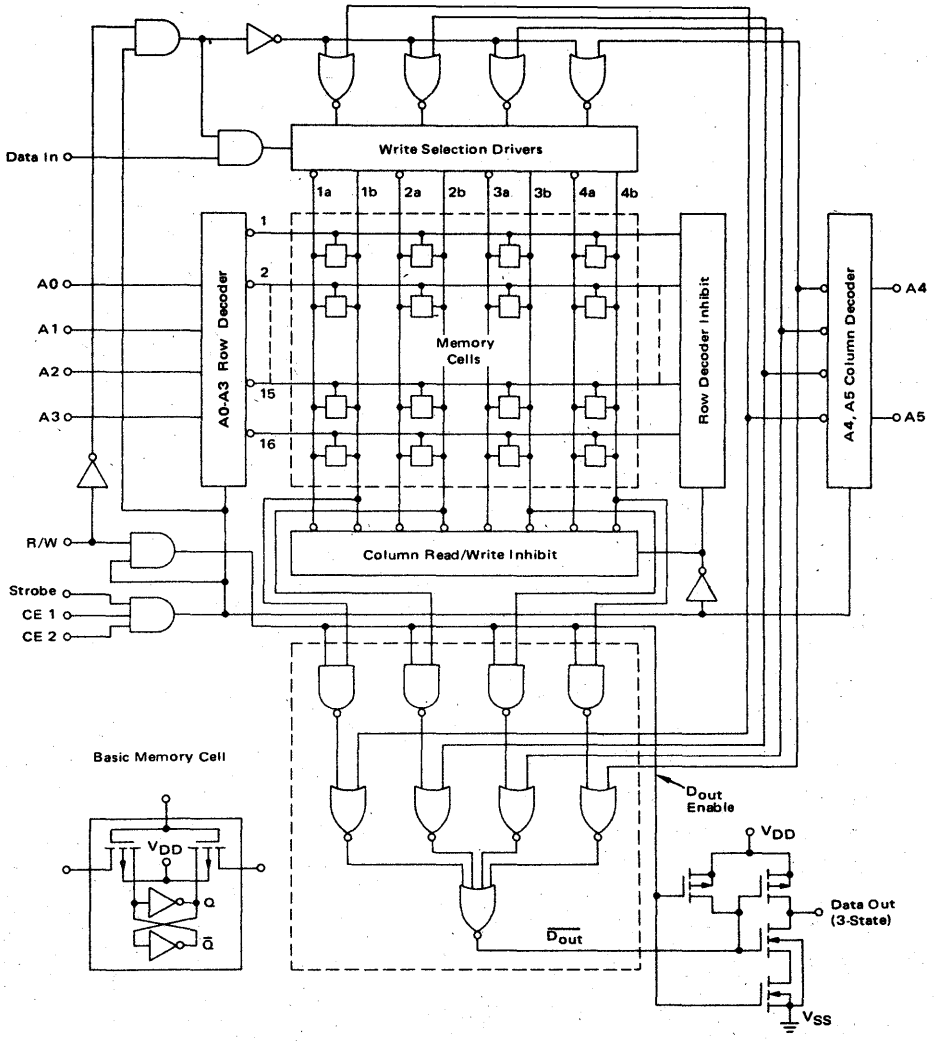
FIGURE 7 – FUNCTIONAL CIRCUIT DIAGRAM



OPERATING CHARACTERISTICS

In considering the operation of the MCM14505 CMOS memory, refer to the functional circuit diagram of Figure 7 and timing diagrams shown in Figures 1 and 2. The basic memory cell is a cross-coupled flip-flop consisting of two inverter gates and two P-channel devices for read/write control. The push-pull cell provides high speed as well as low power.

During a read cycle, when the strobe line is high the write selection drivers are disabled and the data from the selected row is available on columns 1b, 2b, 3b, and 4b. The A4 and A5 address bits are decoded to select output data from one of the four columns. The output data is available on the data output pin only when the strobe and read/write lines are high simultaneously and after the read access time, $t_{acc(R)}$, has occurred (see Figure 1). Note that the output is initially disabled and always goes to the logic "0" state (low voltage) before data is valid. The output is in the high-impedance state (disabled) when the strobe line or the R/W line is in the low state. The memory is strobed for reading or writing only when the strobe, CE1, and CE2 are high simultaneously. The R/W line can be a dc voltage during a read or write cycle and need not be pulsed, as shown in the timing diagrams. For this case the R/W line should be a logic "1" (high) for reading and a logic "0" for writing.

When the strobe line is high, the column read/write inhibit gates and the row decoder inhibit gates are disabled, the selected row is in the low state, and the unselected 15 rows retain their logic "1" level due to the row capacitance that exists when the row decoder inhibit gates are disabled. This capacitive storage mechanism requires a maximum strobe width (see Figure 3) equal to the junction reverse bias RC time constant. When the strobe is returned to a logic "0" the rows are forced to V_{DD} by the row decoder inhibit gates (pullup devices). Similarly the column read/write inhibit gates (pulldown devices) force the column lines to a logic "0" state.

Two column lines are associated with each memory cell in order to write into the cell. The write selection drivers are enabled when the R/W line is a logic "0" and the strobe line is a logic "1". The input data is written into the column selected by the column decoder. For instance, if a "1" is to be written in the memory cell associated with row 1 and column 1, then row 1 would be enabled (logic "0") while column 1b is forced high and column 1a is forced low by the write selection drivers. If a logic "0" is to be written into the cell, then column 1a is forced high and 1b is forced low. The data that is retained in the memory cell is the data that was present on the data input pin at the moment the strobe goes low when R/W is low, or when R/W goes high when the strobe is high.

APPLICATIONS INFORMATION

Figure 8 shows a 256-word by n-bit static RAM memory system The outputs of four MCM14505 devices are tied together to form 256 words by 1 bit. Additional bits are attained by paralleling the inputs in groups of four. Memories of larger words can be attained by decoding the most significant bits of the address and ANDing them with the strobe input.

Fan-in and fan-out of the memory is limited only by speed requirements. The extremely low input and output leakage current (100 nA maximum) keep the output voltage levels from changing significantly as more outputs are tied together. With the output levels independent of fan-out, most of the power supply range is available as logic swing, regardless of the number of units wired together. As a result, high noise immunity is maintained under all conditions.

Power dissipation is 0.1 μW per bit at a 1.0-kHz rate for a 5.0-volt power supply, while the static power dissipation is 2.0 nW per bit. This low power allows non-volatile information storage when the memory is powered by a small standby battery.

Figure 9 shows an optional standby power supply circuit for making a CMOS memory "non-volatile". When the usual power fails, a battery is used to sustain operation or maintain stored information. While normal power supply voltage is present, the battery is trickle-charged through a resistor which sets the charging rate. V_B is the sustaining voltage, and V^+ is the ordinary voltage from a power supply. V_{DD} connects to the power pin on the memory. Low-leakage diodes are recommended to conserve battery power.

The memory system shown in Figure 8 can be interfaced directly with the other devices in the McMOS family. No external components are required.

At the inputs to the CMOS memory, TTL devices can interface directly if an open-collector logic gate such as the MC7407 is used as shown in Figure 10. Driver circuits are not required since the input capacitance is low (4.0 to 6.0 pF). The address, data, and read/write inputs do not need to be fast since they can be changed for the duration when the strobe pulse is low, t_{STL} (see Figures 1 and 2). For high-speed operation, a push-pull driver should be used if more than five strobe inputs must be driven at one time. One circuit of the type shown in Figure 10 can be used for every ten strobe inputs.

Figures 11, 12, and 13 show methods of interfacing the memory output to TTL logic at various memory voltages. If a V_{DD} of 5.0 volts is used for slow-speed, low-power applications, one transistor and one resistor must be used (Figure 11). The MCM14505AL will drive one low-power TTL gate directly.

If a V_{DD} of 10 volts is used, the output of the memory device can fan out to two low-power TTL gates (Figure 12a) or to a discrete transistor (Figure 12b). The discrete transistor circuit provides higher speed and/or high fan-out. A pulldown resistor at the base of the transistor is not needed for fast turn-off because of the push-pull output of the memory. Turn-on time of the transistor is much faster in Figure 12b since the voltage rise is only 0.75 volt. The low output capacitance of the MCM14505 means that several outputs can be wire-ORed without significantly degrading performance. The read access time is increased by only 20 ns typically for 16 outputs tied together when Figure 12b is used.

Five low-power TTL gates can be driven from the memory output if a V_{DD} of 15 volts is used (Figure 13a). Figure 13b shows the interface if a discrete transistor is used. The 1.0 kilohm resistor in the base is required to insure that not more than 10 mA flows through the output as listed in the maximum ratings. If a 2.0 kilohm collector resistor is used (fan-out = 3), the turn-on time of the transistor is only slightly faster than in the circuit shown in Figure 12b due to the lower output impedance when V_{DD} = 15 volts. The voltage at the memory data output has to rise to only 1.3 volts to insure driving a fan-out of three TTL devices.

If a 510-ohm collector resistor is used, 20 TTL loads may be driven. The read access time is increased about 20 ns when four memory outputs are tied together since the output voltage must rise to 3.7 volts before the transistor can sink the full I_{OL} for a fan-out of 20 TTL devices. Almost any NPN transistor with a minimum beta of 15 can be used for the interface shown in Figures 11, 12 and 13.

The high source current from the push-pull output stage of the MCM14505 makes for a simpler interface circuit since a low source current memory requires a differential comparator to achieve high-speed operation.

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FIGURE 8 – CMOS 256-WORD BY n-BIT STATIC READ/WRITE MEMORY

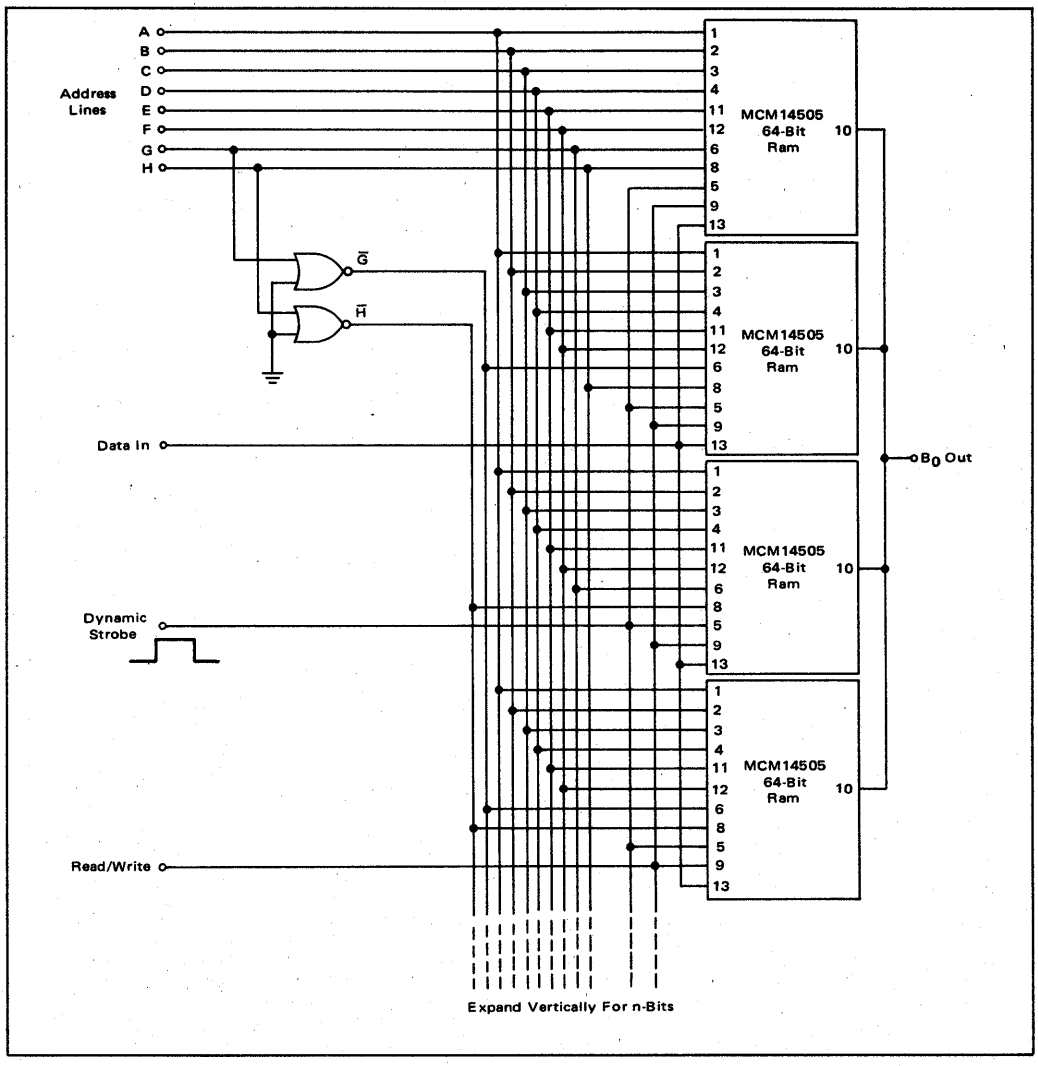


FIGURE 9 – STAND BY BATTERY CIRCUIT

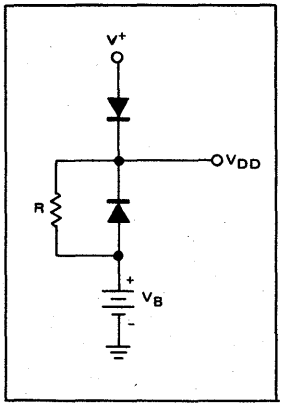


FIGURE 10 – TTL TO CMOS INTERFACE

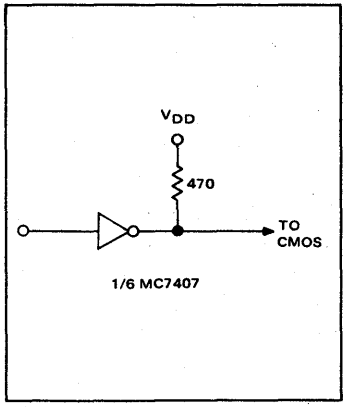
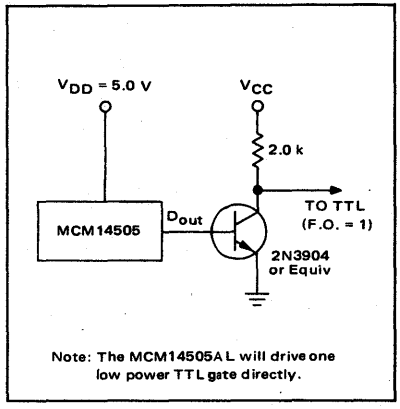


FIGURE 11 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 5.0 V



Note: The MCM14505AL will drive one low power TTL gate directly.

FIGURE 12 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 10 V

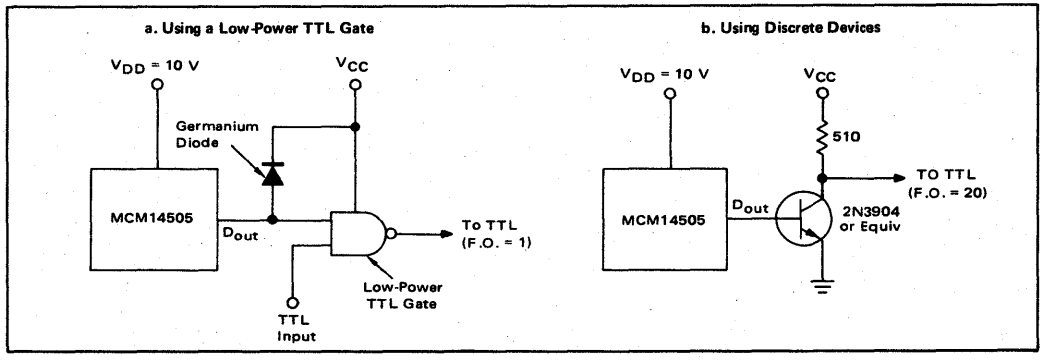
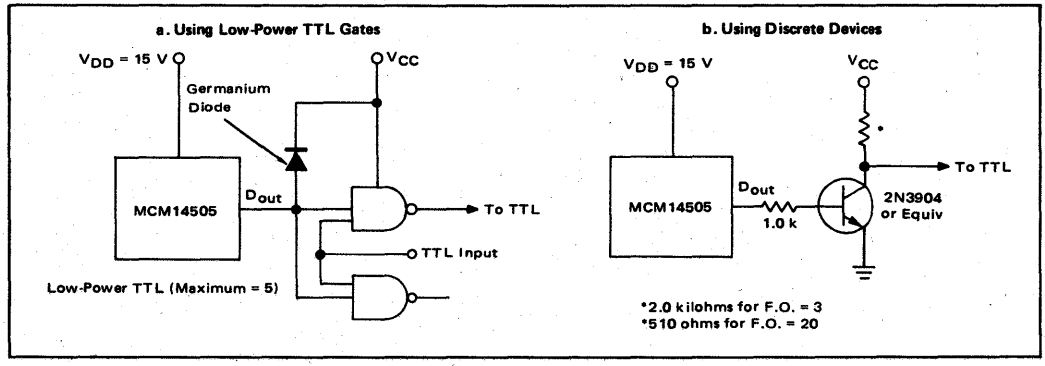


FIGURE 13 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 15 V



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MC14506B

McMOS SSI

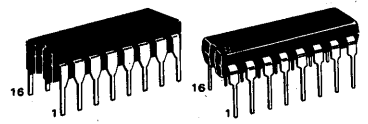
(LOW-POWER COMPLEMENTARY MOS)

DUAL EXPANDABLE AND-OR-INVERT GATE

DUAL 2-WIDE, 2-INPUT EXPANDABLE AND-OR-INVERT GATE

The MC14506B is an expandable AND-OR-INVERT gate with inhibit and 3-state output. The expand option allows cascading with any other gate, which may be carried as far as desired as long as the propagation delay added with each gate is considered. For example, the second AOI gate in this device may be used to expand the first gate, giving an expanded 4-wide, 2-input AOI gate. This device is useful in data control and digital multiplexing applications.

- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- 3-State Output
- Separate Inhibit Line
- Diode Protection on All Inputs
- Supply Voltage RAnge = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

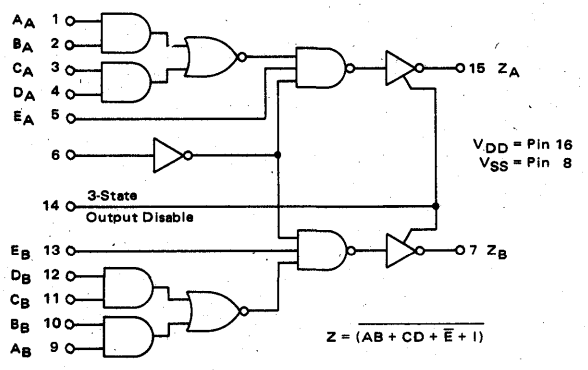
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

LOGIC DIAGRAM



TRUTH TABLE

A	B	C	D	E	INHIBIT	DISABLE	Z
0	0	0	0	1	0	0	1
0	X	0	X	1	0	0	1
0	X	X	0	1	0	0	1
X	0	0	X	1	0	0	1
X	0	X	0	1	0	0	1
1	1	X	X	X	X	0	0
X	X	1	1	X	X	0	0
X	X	X	X	0	X	0	0
X	X	X	X	X	1	0	0
X	X	X	X	X	X	1	High Impedance

X = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.6 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.1 μA/kHz) f + I_{DD}							
		15	I_T = (1.7 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

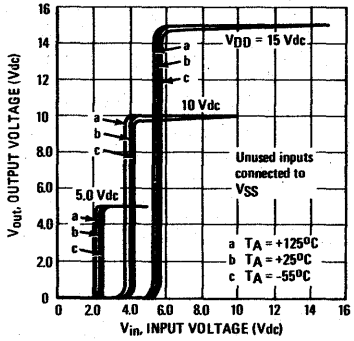
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Data Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pf) C_L + 210 ns		5.0	295	440	580	
t_{PLH} = (0.66 ns/pF) C_L + 77 ns		10	110	165	225	
t_{PLH} = (0.5 ns/pF) C_L + 50 ns		15	75	110	180	
t_{PHL} = (1.7 ns/pF) + C_L 185 ns	t_{PHL}	5.0	270	360	480	ns
t_{PHL} = (0.66 ns/pF C_L + 62 ns		10	95	135	175	
t_{PHL} = (0.5 ns/pF) C_L + 40 ns		15	65	110	140	
Expand Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 95 ns		5.0	180	270	430	
t_{PLH} = (0.66 ns/pF) C_L + 42 ns		10	75	110	160	
t_{PLH} = (0.5 ns/pF) C_L + 25 ns		15	50	75	125	
t_{PHL} = (1.7 ns/pF) C_L + 115 ns	t_{PHL}	5.0	200	270	330	ns
t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	80	90	110	
t_{PHL} = (0.5 ns/pF) C_L + 30 ns		15	55	60	90	
Inhibit Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 135 ns		5.0	220	360	500	
t_{PLH} = (0.66 ns/pF) C_L + 67 ns		10	100	150	225	
t_{PLH} = (0.5 ns/pF) C_L + 40 ns		15	65	100	160	
t_{PHL} = (1.7 ns/pF) C_L + 145 ns	t_{PHL}	5.0	230	360	400	ns
t_{PHL} = (0.66 ns/pF) C_L + 62 ns		10	95	140	175	
t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	60	100	150	
3-State Propagation Delay Time						
"1" to High Impedance	$t_{"1"H}$	5.0	60	125	150	ns
		10	45	75	110	
		15	35	60	90	
"0" to High Impedance	$t_{"0"H}$	5.0	90	135	225	ns
		10	55	80	140	
		15	40	60	100	
High Impedance to "1"	$t_{H"1"}$	5.0	110	250	300	ns
		10	50	100	125	
		15	40	60	100	
High Impedance to "0"	$t_{H"0"}$	5.0	170	255	425	ns
		10	70	105	175	
		15	50	75	125	

*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS

(a) EXPAND INPUTS



(b) DATA INPUTS

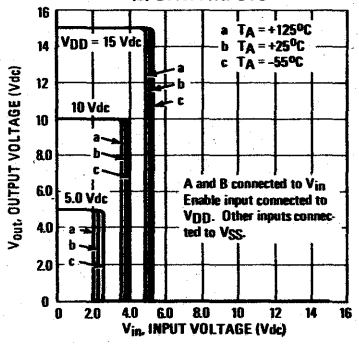


FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

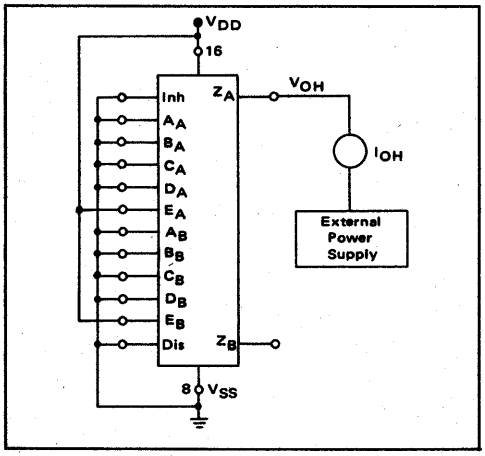


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

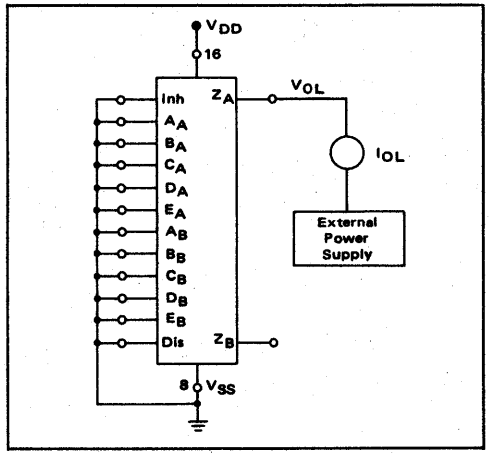


FIGURE 4 – 3-STATE LEAKAGE CURRENT TEST CIRCUIT

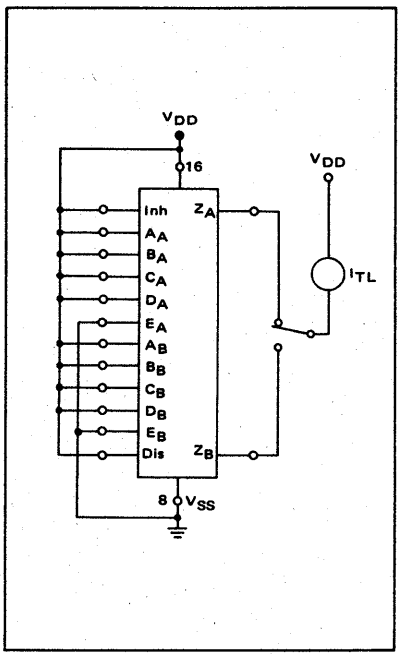


FIGURE 5 – TYPICAL POWER DISSIPATION TEST CIRCUIT

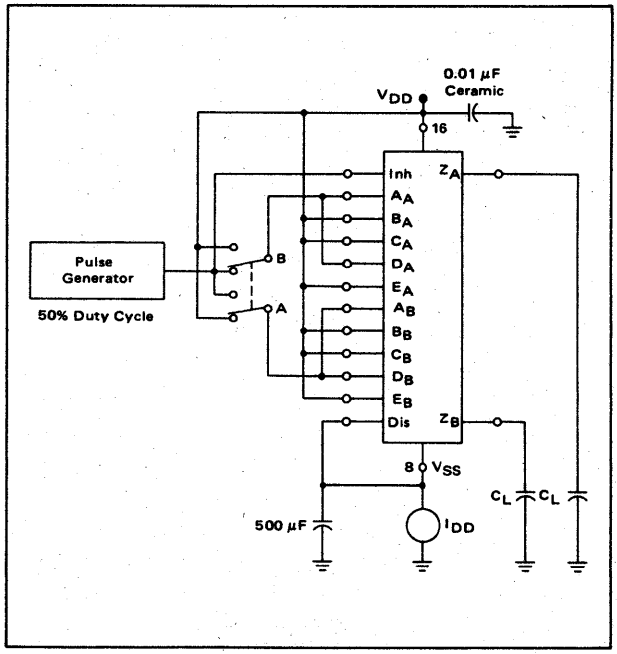


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FIGURE 6 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(Data Inputs)

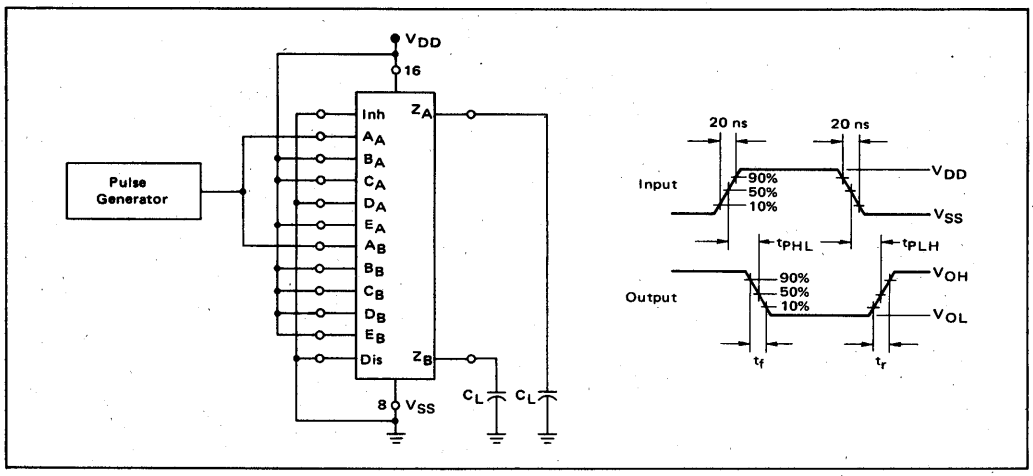
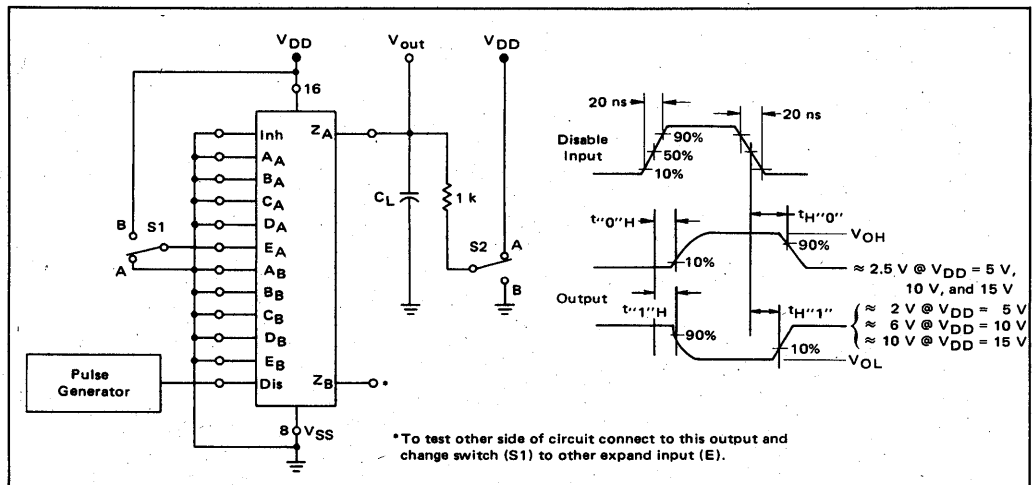


FIGURE 7 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(For 3-State Output)



*To test other side of circuit connect to this output and change switch (S1) to other expand input (E).

SWITCH POSITIONS

TEST	S1	S2
$t_{"0"H}$	A	A
$t_{"1"H}$	B	B
$t_{H"0"}$	A	A
$t_{H"1"}$	B	B

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MC14507

QUAD EXCLUSIVE "OR" GATE

The MC14507 quad exclusive OR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- High Fanout >50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

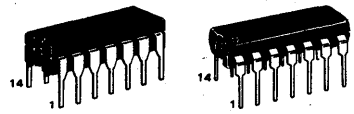
NOTE:

Not Recommended for New Designs. Use MC14070B as a Direct Replacement.

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD EXCLUSIVE "OR" GATE



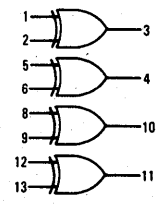
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

LOGIC DIAGRAM
POSITIVE LOGIC



3 = 1⊕2

V_{DD} = Pin 14
V_{SS} = Pin 7

5

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MC14508B

DUAL 4-BIT LATCH

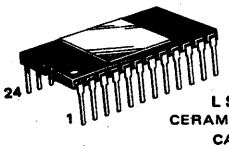
The MC14508B dual 4-bit latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The part consists of two identical, independent 4-bit latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high impedance state and allow the devices to be used in time sharing bus line applications.

These complementary MOS latches find primary use in buffer storage, holding register, or general digital logic functions where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family Data Sheet.

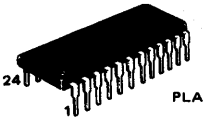
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- 3-State Output
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.

McMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-BIT LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 716



P SUFFIX
PLASTIC PACKAGE
CASE 709

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ORDERING INFORMATION

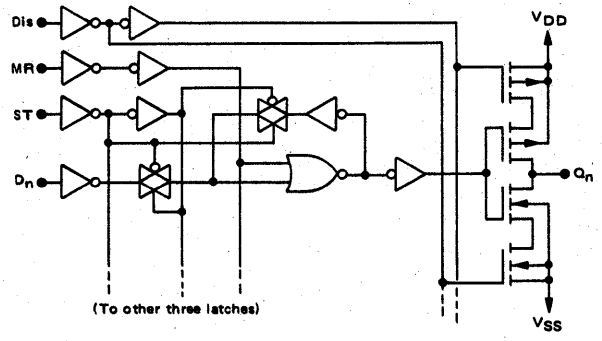
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

TRUTH TABLE

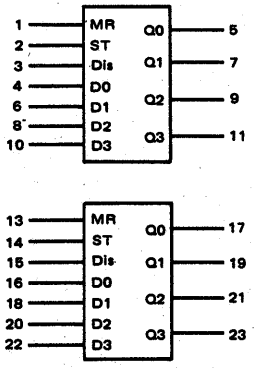
MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1	0	0	0
0	0	0	X	X	X	X	Latched			
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X	High Impedance			

X = Don't Care

CIRCUIT DIAGRAM



BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.46 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.91 μA/kHz) f + I_{DD}							
		15	I_T = (4.37 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 8 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Types	Max	
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns	t_{PHL}	5.0	–	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	120	
Minimum Master Reset Pulse Width	PW_{MR}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	35	70	
Minimum Strobe Pulse Width	PW_{ST}	5.0	–	70	140	ns
		10	–	35	70	
		15	–	20	40	
Minimum Setup Time	t_{setup}	5.0	–	25	50	ns
		10	–	10	20	
		15	–	5.0	10	
Hold Time	t_{hold}	5.0	–	0	0	ns
		10	–	0	0	
		15	–	0	0	
3-State Propagetion Delay Time	$t_{"1"H}$					ns
Output "1" to High Impedance						
$t_{"1"H}$ = (0.49 ns/pF) C_L + 60.5 ns		5.0	–	85	170	
$t_{"1"H}$ = (0.29 ns/pF) C_L + 35.5 ns		10	–	50	100	
$t_{"1"H}$ = (0.19 ns/pF) C_L + 25.5 ns		15	–	35	70	
Output "0" to High Impedance	$t_{"0"H}$					ns
$t_{"0"H}$ = 0.32 ns/pF) C_L + 49 ns		5.0	–	65	130	
$t_{"0"H}$ = (0.29 ns/pF) C_L + 25.5 ns		10	–	40	80	
$t_{"0"H}$ = (0.28 ns/pF) C_L + 16 ns		15	–	30	60	
High Impedance to "1" Level	$t_{H"1"}$					ns
$t_{H"1"}$ = (0.41 ns/pF) C_L + 64.5 ns		5.0	–	85	170	
$t_{H"1"}$ = (0.31 ns/pF) C_L + 34.5 ns		10	–	50	100	
$t_{H"1"}$ = (0.30 ns/pF) C_L + 20 ns		15	–	35	70	
High Impedance to "0" Level	$t_{H"0"}$					ns
$t_{H"0"}$ = (0.49 ns/pF) C_L + 60.5 ns		5.0	–	85	170	
$t_{H"0"}$ = (0.29 ns/pF) C_L + 35.5 ns		10	–	50	100	
$t_{H"0"}$ = (0.19 ns/pF) C_L + 25.5 ns		15	–	35	70	

*The formula given is for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – AC WAVEFORMS

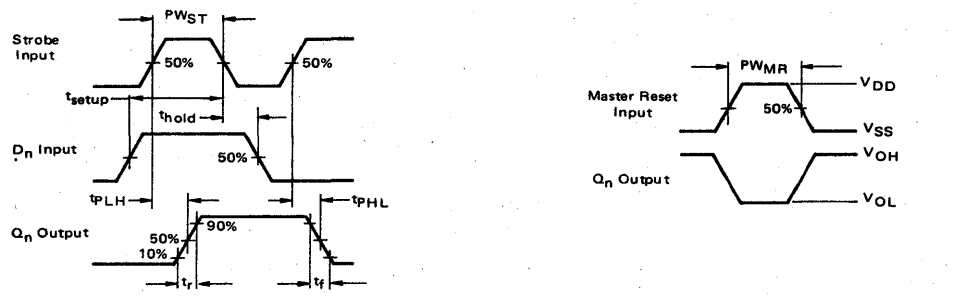
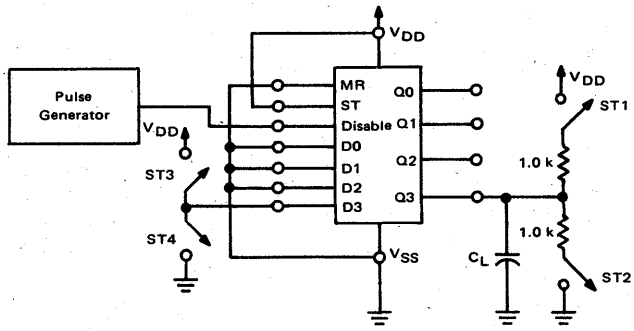
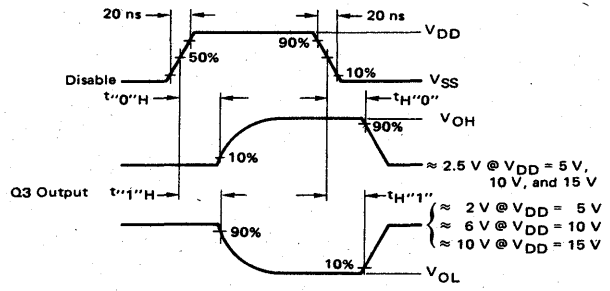


FIGURE 2 – 3-STATE AC TEST CIRCUIT AND WAVEFORMS



TEST	ST1	ST2	ST3	ST4
$t_{"1"H}$	OPEN	CLOSE	CLOSE	OPEN
$t_{"0"H}$	CLOSE	OPEN	OPEN	CLOSE
$t_{H"0"}$	CLOSE	OPEN	OPEN	CLOSE
$t_{H"1"}$	OPEN	CLOSE	CLOSE	OPEN

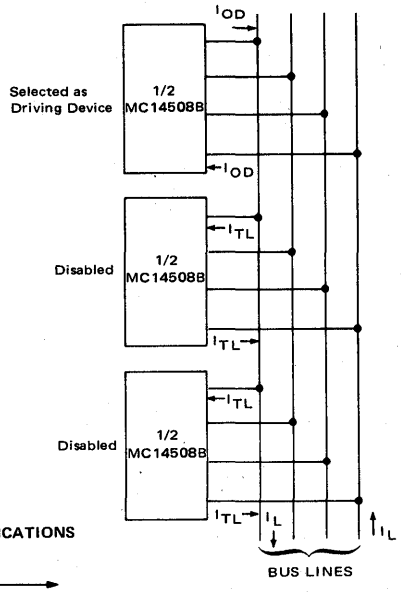


3-STATE MODE OF OPERATION

The MC14508B can be used in bussed systems as shown. The output terminals of N 4-bit latches can be directly wired to a bus line, and to one of the 4-bit latches selected. The selected latch controls the logic state of the bus line, and the remaining (N-1) 4-bit latches are disabled into a high impedance "off" state. The number of latches, N, which may be connected to a bus line is determined from the output drive current, I_{OD}, the 3-state or disabled output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs) and can be calculated by the following:

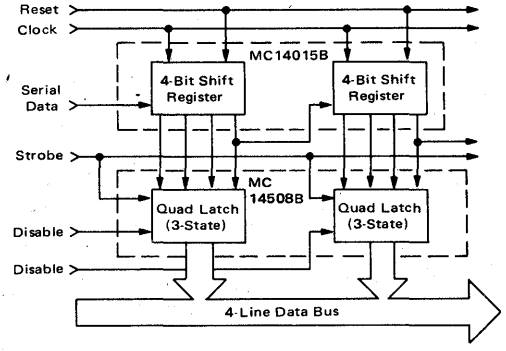
$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic states of the bus line.

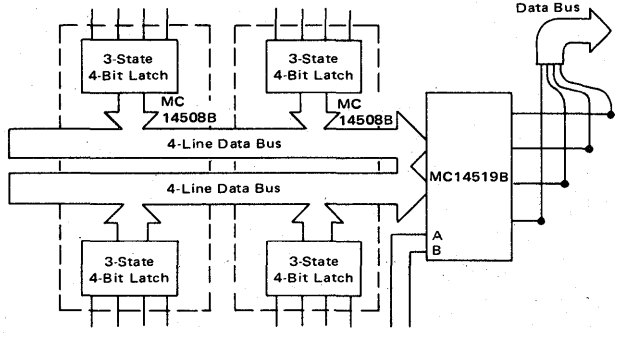


TYPICAL 3–STATE APPLICATIONS

EXAMPLE 1



EXAMPLE 2



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14510B

BCD UP/DOWN COUNTER

The MC14510B BCD up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide type T flip-flop capability. The counter can be cleared by applying a high level on the Reset line. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

- Quiescent Current = 5.0 nA/package typical @ 5.0 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance — 5.0 pF typical
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design — Count Occurs on Positive Going Edge of Clock
- 5.0-MHz Counting Rate
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

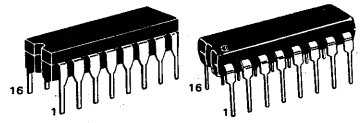
TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

McMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

BCD UP/DOWN COUNTER



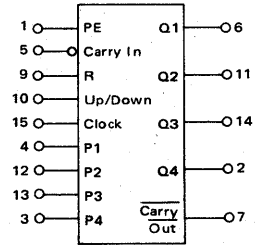
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.7 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types Min	All Types Typ	All Types Max	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_r = (1.5 ns/pF) C_L +15 ns		10	–	90	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Clock to $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 95 ns		5.0	–	180	360	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	–	80	160	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	120	
Preset or Reset to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Preset or Reset ot $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
Minimum Clock Pulse Width	PW_C	5.0	–	200	400	ns
		10	–	100	200	
		15	–	75	150	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	3.0	–	MHz
		10	3.0	6.0	–	
		15	4.0	8.0	–	
Preset or Reset Removal Time**	t_{rem}	5.0	–	325	650	ns
		10	–	115	230	
		15	–	90	180	
Maximum Clock Rise and Fall Time	t_r, t_f	5.0	15	–	–	µs
		10	15	–	–	
		15	15	–	–	
Carry In Setup Time	t_{setup}	5.0	–	130	260	ns
		10	–	60	120	
		15	–	50	100	
Up/Down Setup Time	t_{setup}	5.0	–	250	500	ns
		10	–	100	200	
		15	–	75	150	
Minimum Preset Enable Pulse Width	PW_{PE}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

*The formula given is for the typical characteristics only.

**The Preset or Reset Signal must be low prior to a positive-going transition of the clock.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

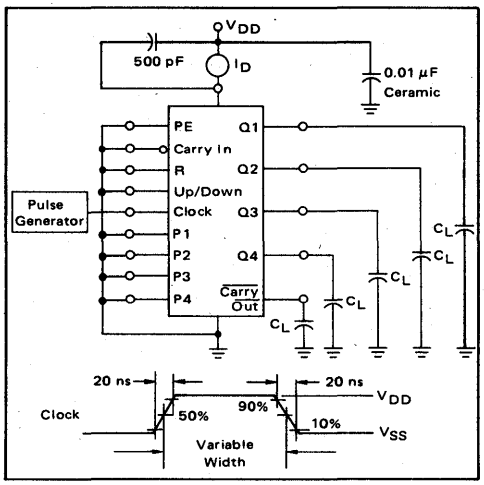
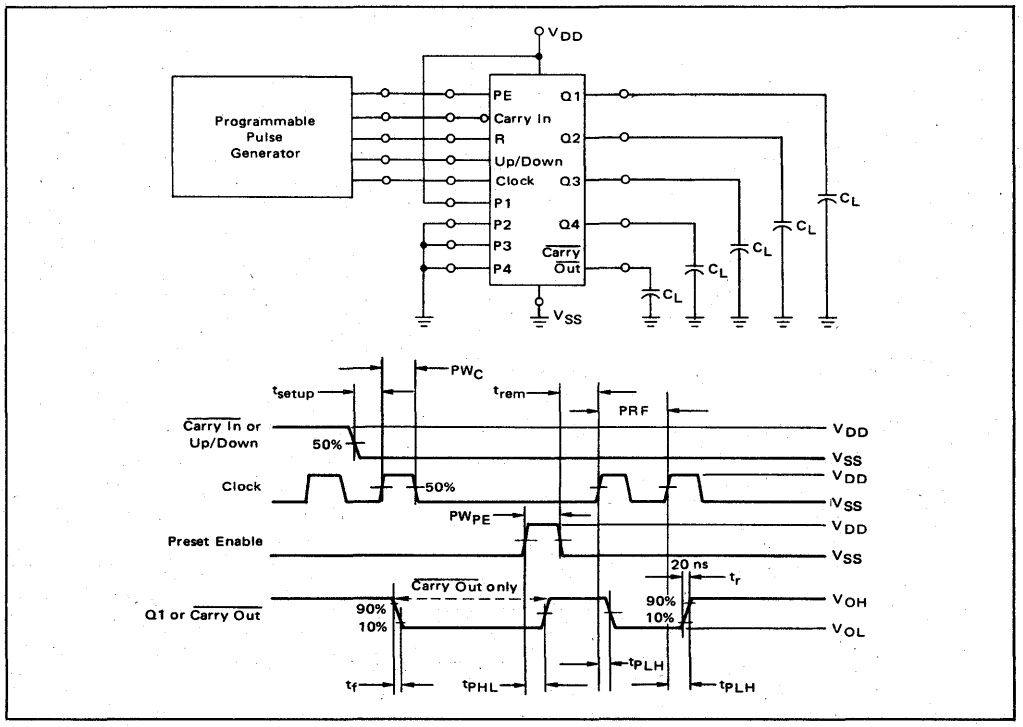
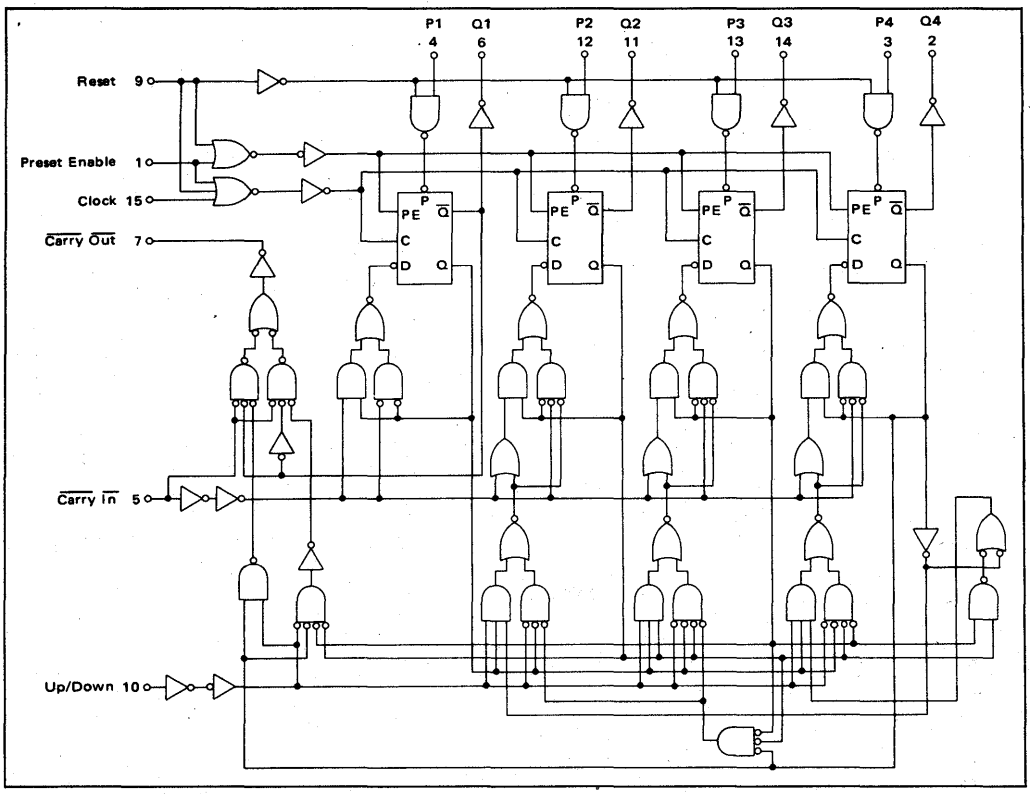


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



5

LOGIC DIAGRAM



TIMING DIAGRAM

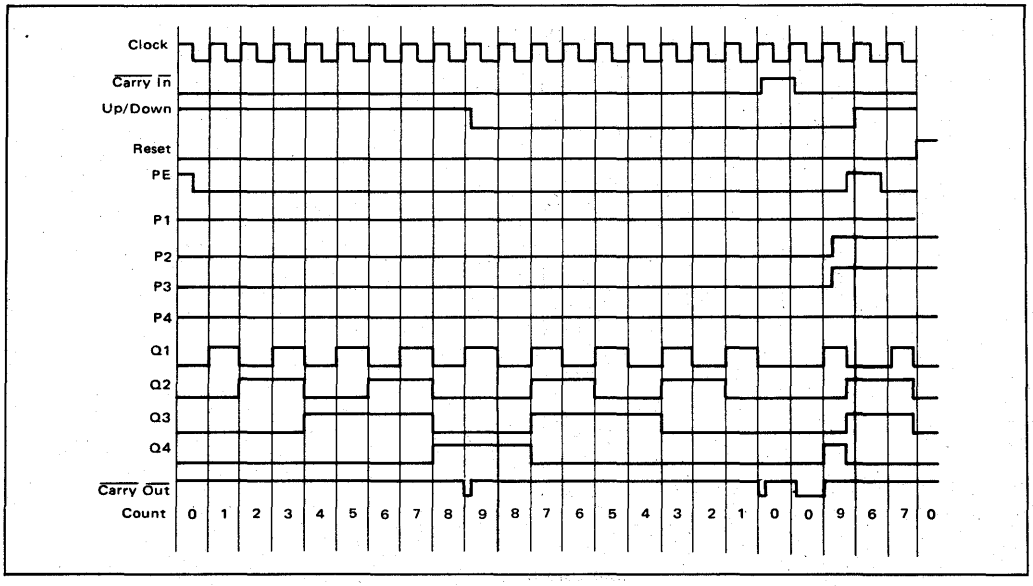


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FIGURE 3 – PRESETTABLE CASCADED UP/DOWN COUNTER

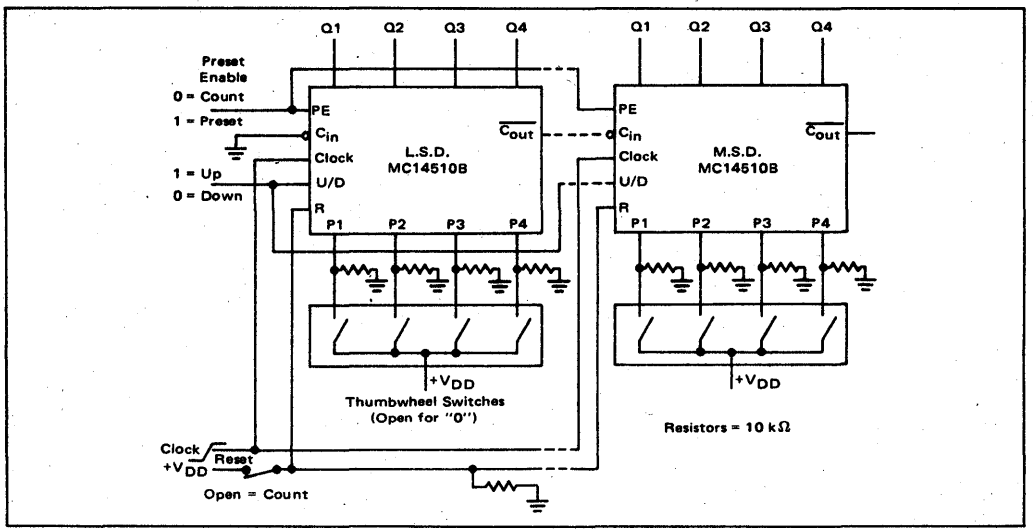
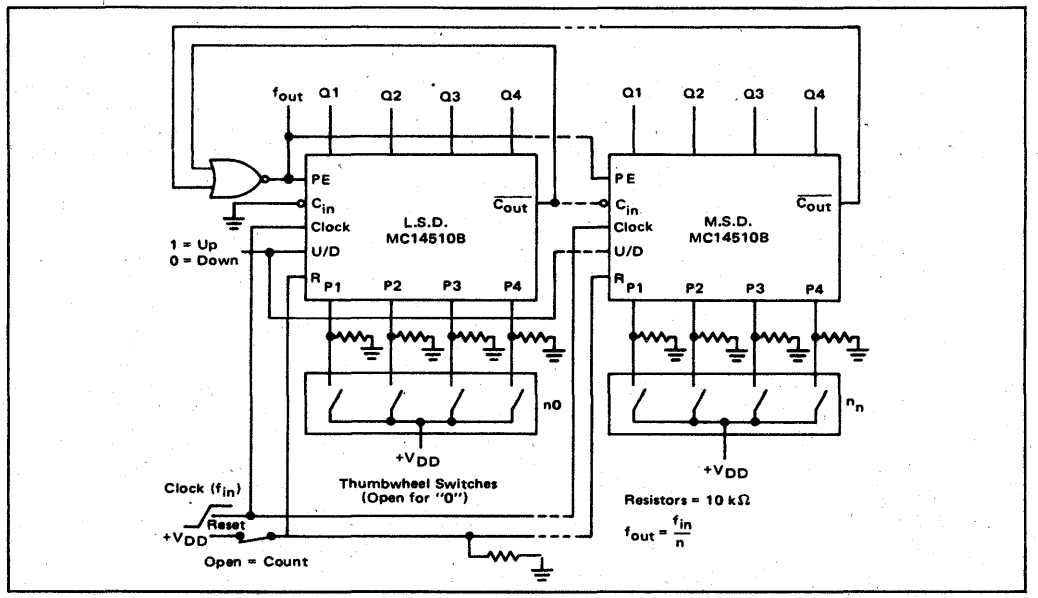


FIGURE 4 – PROGRAMMABLE CASCADED FREQUENCY DIVIDER



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14511B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14511B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

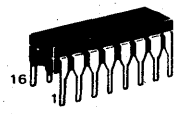
Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

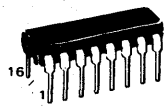
McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER



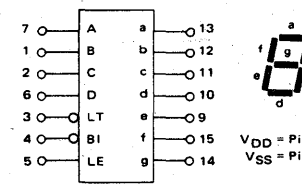
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range



MAXIMUM RATINGS (Voltages referenced to V_{SS}).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	
Maximum Continuous Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output ‡	P_{OHmax}	50	mW

‡ $P_{OHmax} = I_{OH}(V_{DD} - V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occure if V_{in} and V_{out} is not constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*							*

X = Don't Care
*Depends upon the BCD code previously applied when LE = 0

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.1	–	4.1	4.57	–	4.1	–	Vdc
V_{in} = 0 or V_{DD}		10	9.1	–	9.1	9.58	–	9.1	–	
		15	14.1	–	14.1	14.59	–	14.1	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.8 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 8.8 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.8 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
(V_O = 0.5 or 3.8 Vdc) "1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 8.8 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.8 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Voltage (AL Device)	V_{OH}									Vdc
(I_{OH} = 0 mAdc) Source		5.0	4.10	–	4.10	4.57	–	4.1	–	
(I_{OH} = 5.0 mAdc)			–	–	–	4.24	–	–	–	
(I_{OH} = 10 mAdc)			3.90	–	3.90	4.12	–	3.5	–	
(I_{OH} = 15 mAdc)			–	–	–	3.94	–	–	–	
(I_{OH} = 20 mAdc)			3.40	–	3.40	3.75	–	3.0	–	
(I_{OH} = 25 mAdc)			–	–	–	3.54	–	–	–	
(I_{OH} = 0 mAdc)		10	9.10	–	9.10	9.58	–	9.1	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	9.26	–	–	–	
(I_{OH} = 10 mAdc)			9.00	–	9.00	9.17	–	8.6	–	
(I_{OH} = 15 mAdc)			–	–	–	9.04	–	–	–	
(I_{OH} = 20 mAdc)			8.60	–	8.60	8.90	–	8.2	–	
(I_{OH} = 25 mAdc)			–	–	–	8.75	–	–	–	
(I_{OH} = 0 mAdc)		15	14.1	–	14.1	14.59	–	14.1	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	14.27	–	–	–	
(I_{OH} = 10 mAdc)			14.0	–	14.0	14.18	–	13.6	–	
(I_{OH} = 15 mAdc)			–	–	–	14.07	–	–	–	
(I_{OH} = 20 mAdc)			13.6	–	13.6	13.95	–	13.2	–	
(I_{OH} = 25 mAdc)			–	–	–	13.80	–	–	–	
Output Drive Voltage (CL/CP Device)	V_{OH}									Vdc
(I_{OH} = 0 mAdc) Source		5.0	4.10	–	4.10	4.57	–	4.1	–	
(I_{OH} = 5.0 mAdc)			–	–	–	4.24	–	–	–	
(I_{OH} = 10 mAdc)			3.60	–	3.60	4.12	–	3.3	–	
(I_{OH} = 15 mAdc)			–	–	–	3.94	–	–	–	
(I_{OH} = 20 mAdc)			2.80	–	2.80	3.75	–	2.5	–	
(I_{OH} = 25 mAdc)			–	–	–	3.54	–	–	–	
(I_{OH} = 0 mAdc)		10	9.10	–	9.10	9.58	–	9.1	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	9.26	–	–	–	
(I_{OH} = 10 mAdc)			8.75	–	8.75	9.17	–	8.45	–	
(I_{OH} = 15 mAdc)			–	–	–	9.04	–	–	–	
(I_{OH} = 20 mAdc)			8.10	–	8.10	8.90	–	7.8	–	
(I_{OH} = 25 mAdc)			–	–	–	8.75	–	–	–	
(I_{OH} = 0 mAdc)		15	14.1	–	14.1	14.59	–	14.1	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	14.27	–	–	–	
(I_{OH} = 10 mAdc)			13.75	–	13.75	14.18	–	13.45	–	
(I_{OH} = 15 mAdc)			–	–	–	14.07	–	–	–	
(I_{OH} = 20 mAdc)			13.1	–	13.1	13.95	–	12.8	–	
(I_{OH} = 25 mAdc)			–	–	–	13.80	–	–	–	
Output Drive Current (AL Device)	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc) Sink		5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc) Sink		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	

(Continued)

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.9 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.8 μA/kHz) f + I_{DD}							
		15	I_T = (5.7 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	All Types Typ	All Types Max	Unit
Output Rise Time	t_r	5.0	–	40	80	ns
		10	–	30	60	
		15	–	25	50	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 50 ns		5.0	–	125	250	
t_f = (0.75 ns/pF) C_L + 37.5 ns		10	–	75	150	
t_f = (0.55 ns/pF) C_L + 37.5 ns		15	–	65	130	
Data Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.40 ns/pF) C_L + 620 ns		5.0	–	640	1280	
t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns		10	–	250	500	
t_{PLH} = (0.20 ns/pF) C_L + 165 ns		15	–	175	350	
t_{PHL} = (1.3 ns/pF) C_L + 655 ns	t_{PHL}	5.0	–	720	1440	ns
t_{PHL} = (0.60 ns/pF) C_L + 260 ns		10	–	290	580	
t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns		15	–	200	400	
Blank Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.30 ns/pF) C_L + 305 ns		5.0	–	320	640	
t_{PLH} = (0.25 ns/pF) C_L + 117.5 ns		10	–	130	260	
t_{PLH} = (0.15 ns/pF) C_L + 92.5 ns		15	–	100	200	
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns	t_{PHL}	5.0	–	485	970	ns
t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns		10	–	200	400	
t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns		15	–	160	320	
Lamp Test Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.45 ns/pF) C_L + 290.5 ns		5.0	–	313	625	
t_{PLH} = (0.25 ns/pF) C_L + 112.5 ns		10	–	125	250	
t_{PLH} = (0.20 ns/pF) C_L + 80 ns		15	–	90	180	
t_{PHL} = (1.3 ns/pF) C_L + 248 ns	t_{PHL}	5.0	–	313	625	ns
t_{PHL} = (0.45 ns/pF) C_L + 102.5 ns		10	–	125	250	
t_{PHL} = (0.35 ns/pF) C_L + 72.5 ns		15	–	90	180	
Minimum Setup Time	t_{setup}	5.0	–	90	180	ns
		10	–	38	76	
		15	–	20	40	
Minimum Hold Time	t_{hold}	5.0	–	-90	0	ns
		10	–	-38	0	
		15	–	-20	0	
Minimum Latch Enable Pulse Width	PW_{LE}	5.0	–	260	520	ns
		10	–	110	220	
		15	–	65	130	

*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

Input LE low, and Inputs D, $\overline{BI}$ and $\overline{LT}$ high.
f in respect to a system clock.
All outputs connected to respective C_L loads.

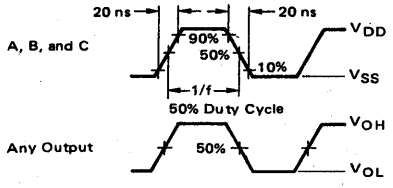
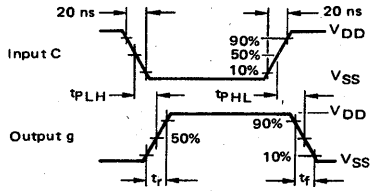
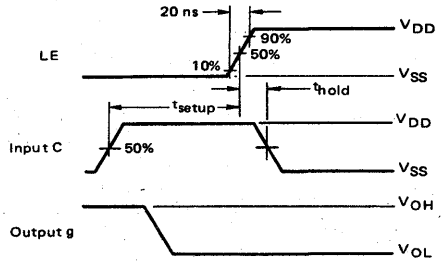


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS

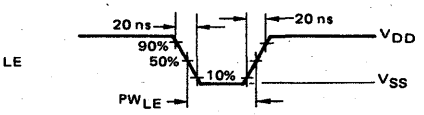
(a) Inputs D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



(b) Input D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



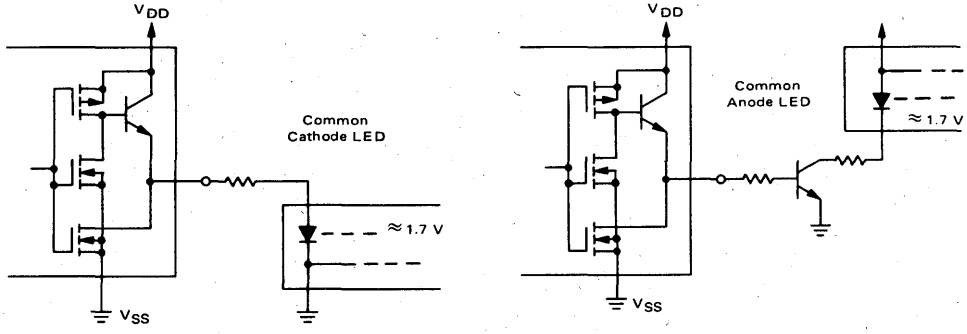
(c) Data DCBA strobed into latches.



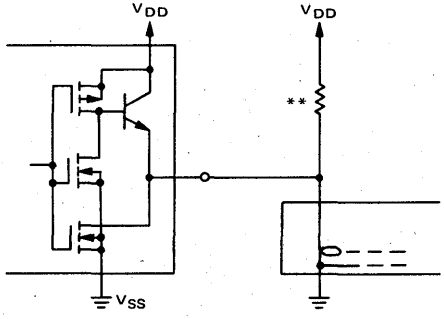
5

CONNECTIONS TO VARIOUS DISPLAY READOUTS

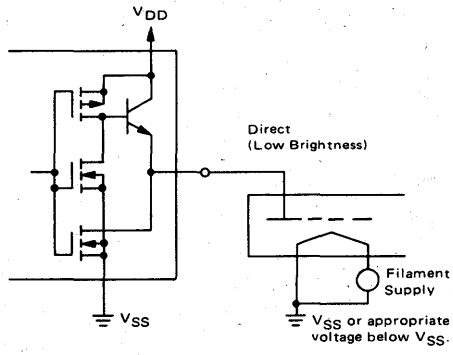
LIGHT EMITTING DIODE (LED) READOUT



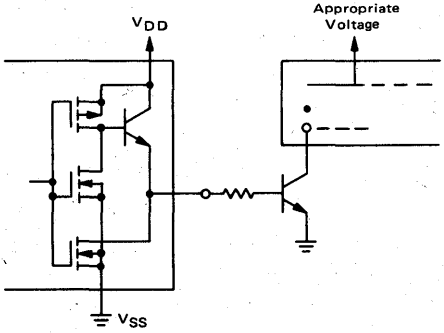
INCANDESCENT READOUT



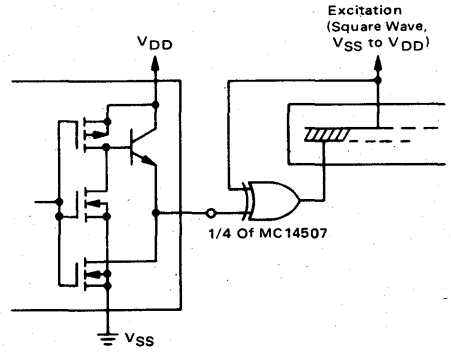
FLUORESCENT READOUT



GAS DISCHARGE READOUT



LIQUID CRYSTAL (LCD) READOUT

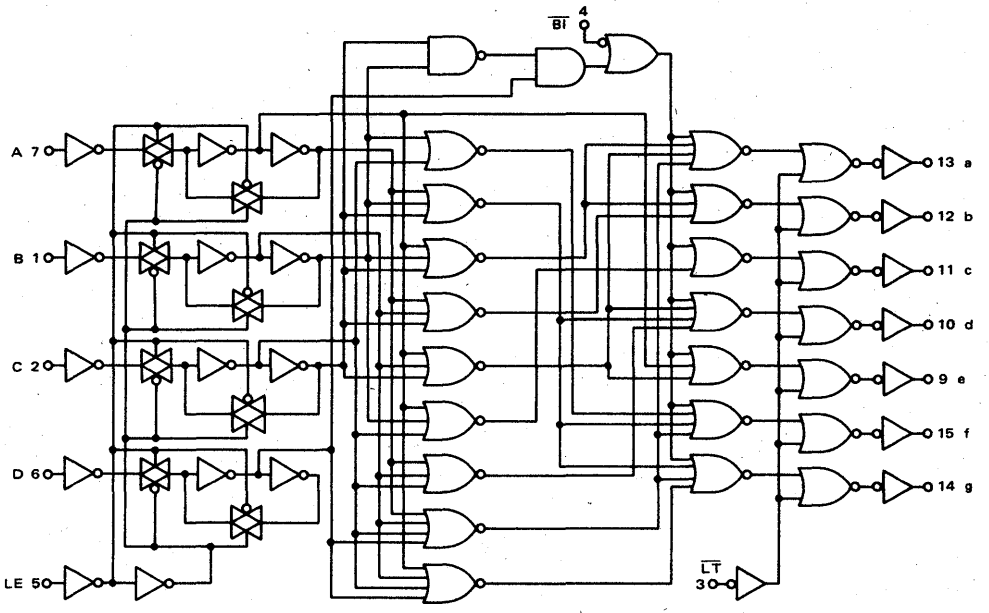


**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LCD's not recommended for life of LCD readouts.

5

LOGIC DIAGRAM



5

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14512

8-CHANNEL DATA SELECTOR

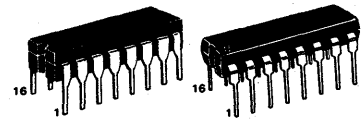
The MC14512 is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- High Fanout > 50
- Single Supply Operation – Positive or Negative
- 3-State Output (Logic "1", Logic "0", High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-CHANNEL DATA SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

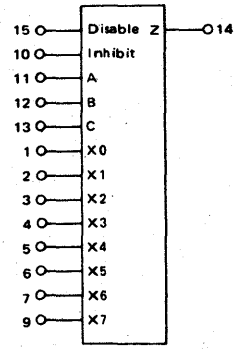
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

C	B	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
ϕ	ϕ	ϕ	1	0	0
ϕ	ϕ	ϕ	ϕ	1	High Impedance

ϕ = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−0.62	–	−0.50	−1.7	–	−0.35	–	
(V_{OH} = 9.5 Vdc)		10	−0.62	–	−0.50	−0.9	–	−0.35	–	
(V_{OH} = 13.5 Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−0.23	–	−0.20	−1.7	–	−0.16	–	
(V_{OH} = 9.5 Vdc)		10	−0.23	–	−0.20	−0.9	–	−0.16	–	
(V_{OH} = 13.5 Vdc)		15	−0.69	–	−0.60	−3.5	–	−0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.8 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.6 μA/kHz) f + I_{DD}							
		15	I_T = (2.4 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

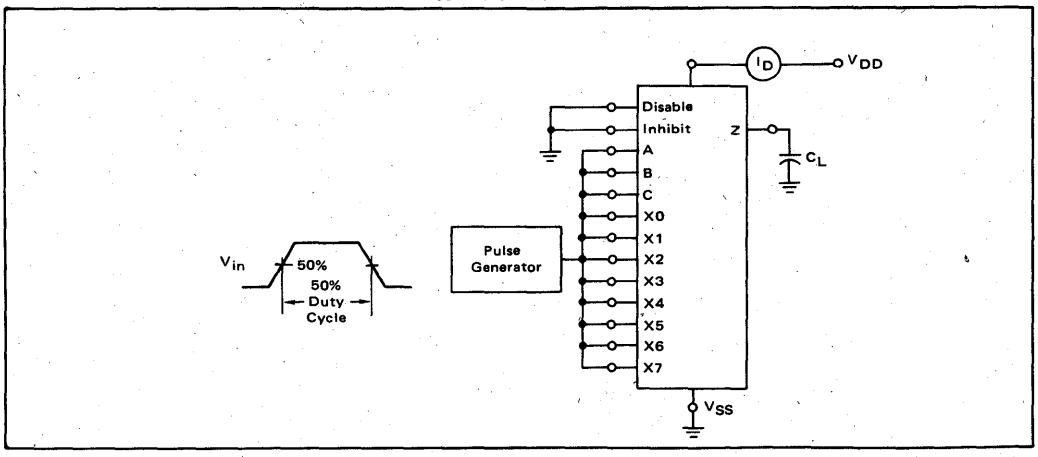
*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (0.9 ns/pF) C_L + 211 ns		5.0	225	500	750	
t_{PLH} = (0.3 ns/pF) C_L + 70 ns		10	75	175	200	
t_{PLH} = (0.23 ns/pF) C_L + 54 ns		15	57	130	150	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (2.7 ns/pF) C_L + 184 ns		5.0	225	500	750	
t_{PHL} = (0.9 ns/pF) C_L + 61 ns		10	75	175	200	
t_{PHL} = (0.68 ns/pF) C_L + 47 ns		15	57	130	150	
3-State Output Delay Times	$t_{"1"H}$, $t_{"0"H}$,	5.0	50	125	150	ns
"1" or "0" to High Z, and	$t_{"H"1}$, $t_{H"0"}$	10	25	75	100	
High Z to "1" or "0"		15	19	60	75	

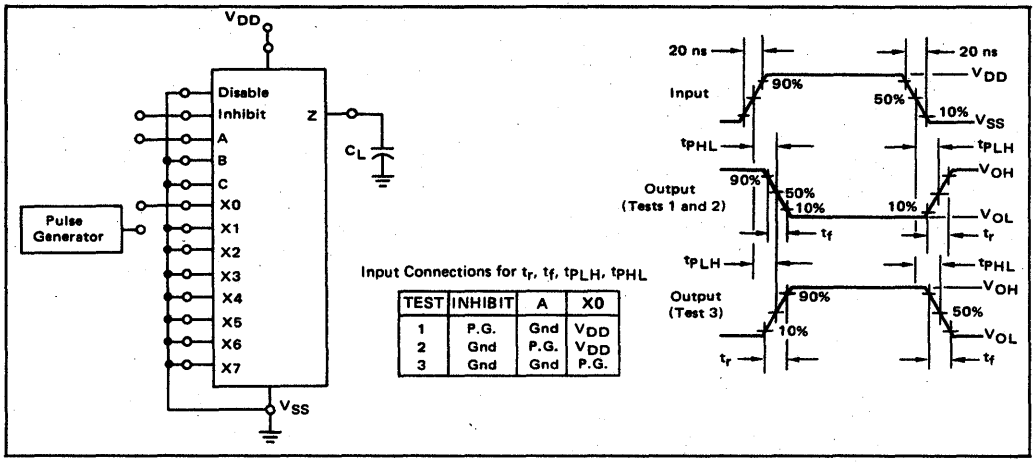
*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

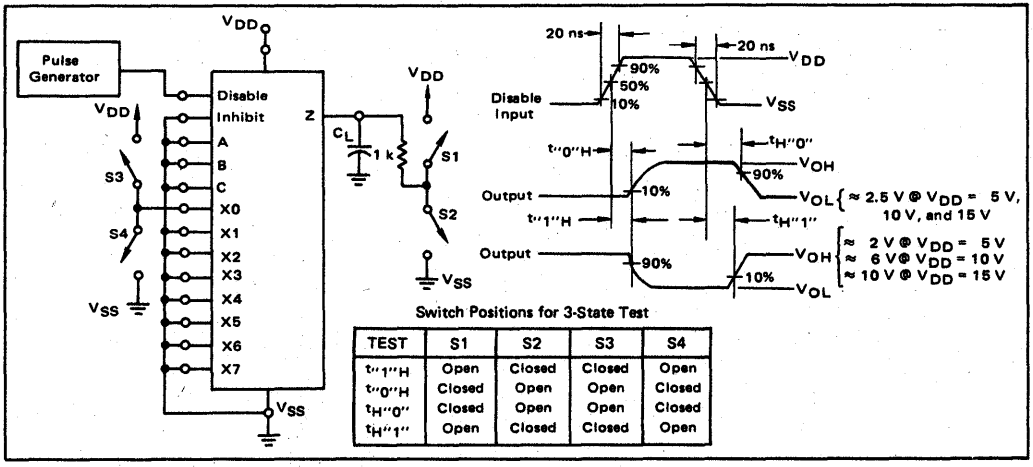
FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



Input Connections for t_r, t_f, t_{PLH}, t_{PHL}

TEST	INHIBIT	A	X0
1	P.G.	Gnd	V_{DD}
2	Gnd	P.G.	V_{DD}
3	Gnd	Gnd	P.G.

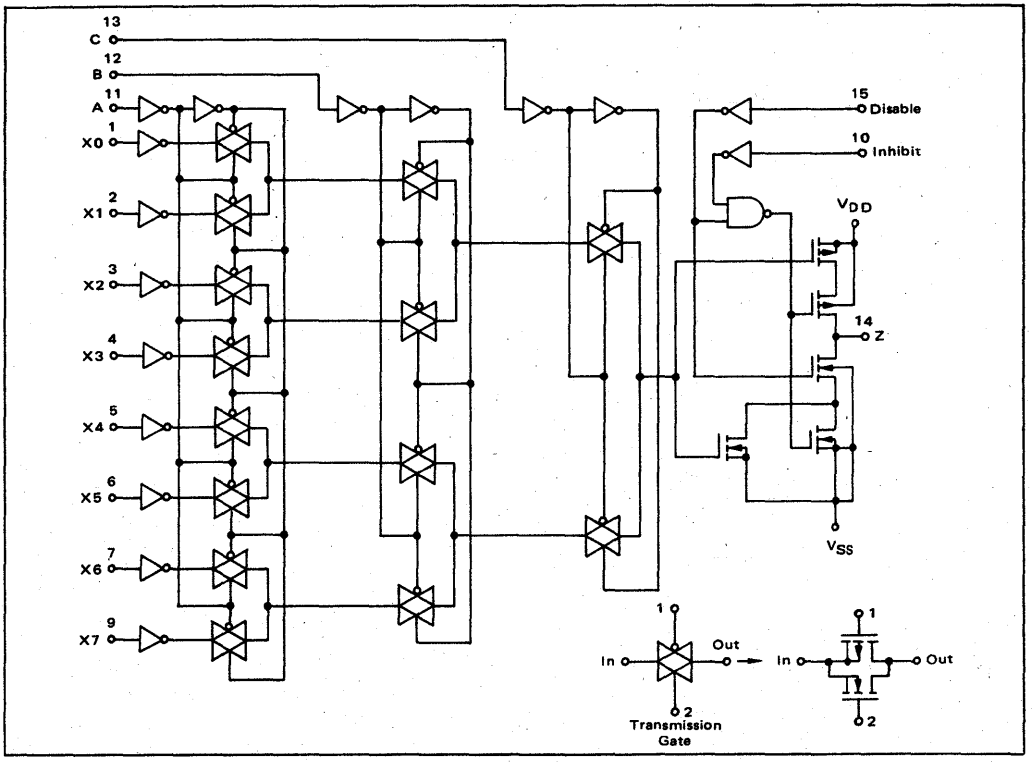
FIGURE 3 – 3-STATE AC TEST CIRCUIT AND WAVEFORM



Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
$t_{r}"1"H$	Open	Closed	Closed	Open
$t_{f}"0"H$	Closed	Open	Open	Closed
$t_H"0"$	Closed	Open	Open	Closed
$t_H"1"$	Open	Closed	Closed	Open

LOGIC DIAGRAM

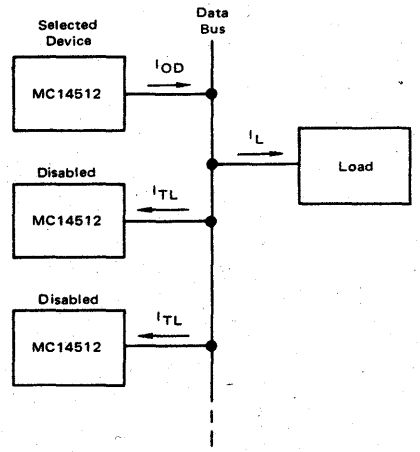


3-STATE MODE OF OPERATION

Output terminals of several MC14512 8-Bit Data Selectors can be connected to a single data bus as shown. One MC14512 is selected by the 3-state control, and the remaining devices are disabled into a high impedance "off" state. The number of 8-bit data selectors, N, that may be connected to a bus line is determined from the output drive current, I_{OD}, 3-state or disable output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs), and can be calculated by:

$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic states of the bus line.



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14514B
MC14515B

4-BIT LATCH/4-TO-16 LINE DECODER

The MC14514B and MC14515B are two output options of a 4 to 16 line decoder with latched inputs. The MC14514B (output active high option) presents a logical "1" at the selected output, whereas the MC14515B (output active low option) presents a logical "0" at the selected output. The latches are R-S type flip-flops which hold the last input data presented prior to the strobe transition from "1" to "0". These high and low options of a 4-bit latch/4 to 16 line decoder are constructed with N-channel and P-channel enhancement mode devices in a single monolithic structure. The latches are R-S type flip-flops and data is admitted upon a signal incident at the strobe input, decoded, and presented at the output.

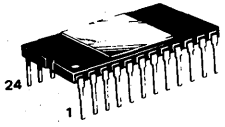
These complementary circuits find primary use in decoding applications where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 5.0 nA package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Single Supply Operation – Positive or Negative
- Input Impedance = 10^{12} ohms typical

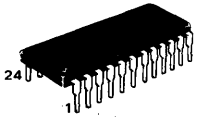
McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT LATCH/4-TO-16
LINE DECODER



L SUFFIX
CERAMIC PACKAGE
CASE 716



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

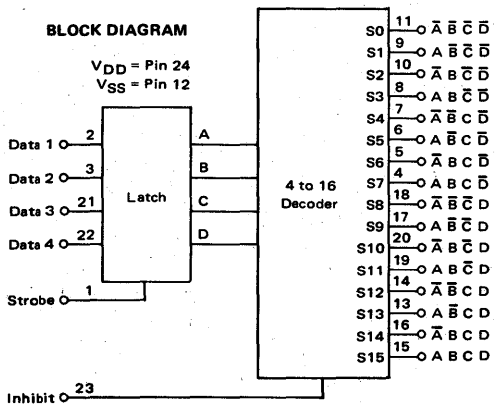
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

5

BLOCK DIAGRAM

V_{DD} = Pin 24
V_{SS} = Pin 12



DECODE TRUTH TABLE (Strobe = 1)

	DATA INPUTS				SELECTED OUTPUT
INHIBIT	D	C	B	A	MC14514 = Logic "1" MC14515 = Logic "0"
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, MC14514 All Outputs = 1, MC14515

X = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.35 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.70 µA/kHz) f + I_{DD}							
		15	I_T = (4.05 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns	t_{PHL}	5.0	–	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
Inhibit Propagation Delay Times	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns	t_{PHL}	5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	150	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Setup Time	t_{setup}					ns
		5.0	–	125	250	
		10	–	50	100	
		15	–	38	75	
Strobe Pulse Width	PW_{ST}					ns
		5.0	–	175	350	
		10	–	50	100	
		15	–	38	75	

*The formula given is for the typical characteristics only.

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FIGURE 1 – DRAIN CHARACTERISTICS TEST CIRCUIT

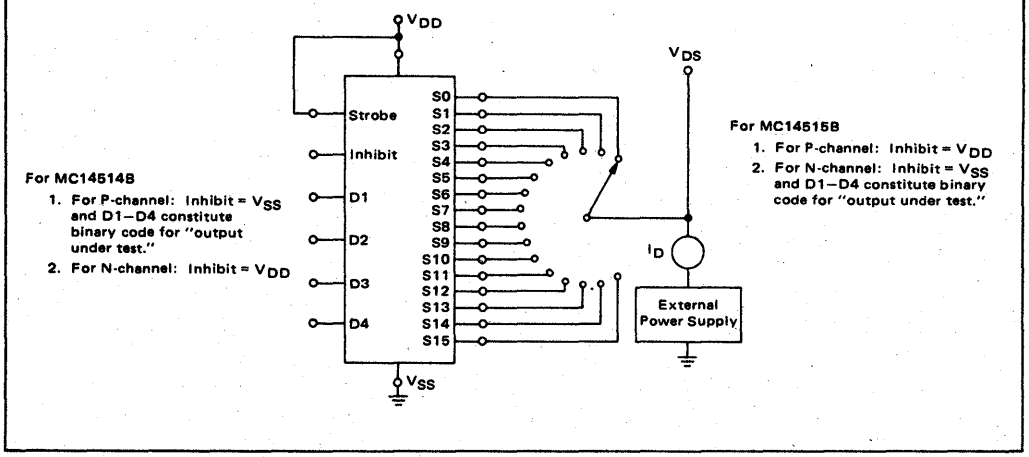


FIGURE 2 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

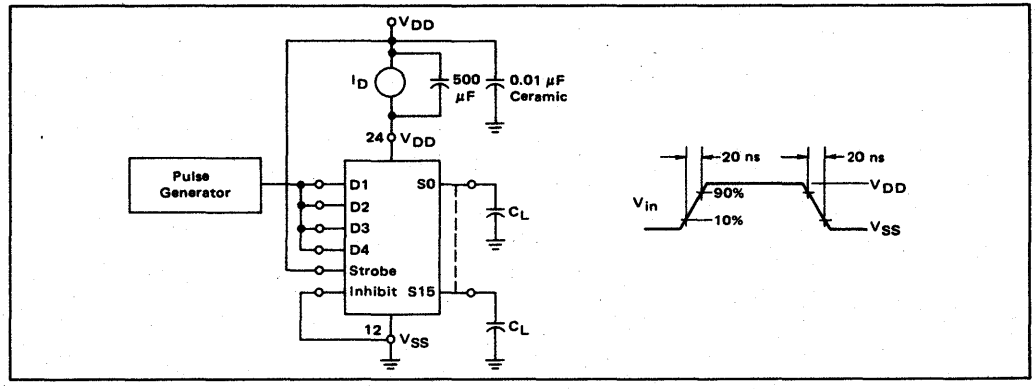
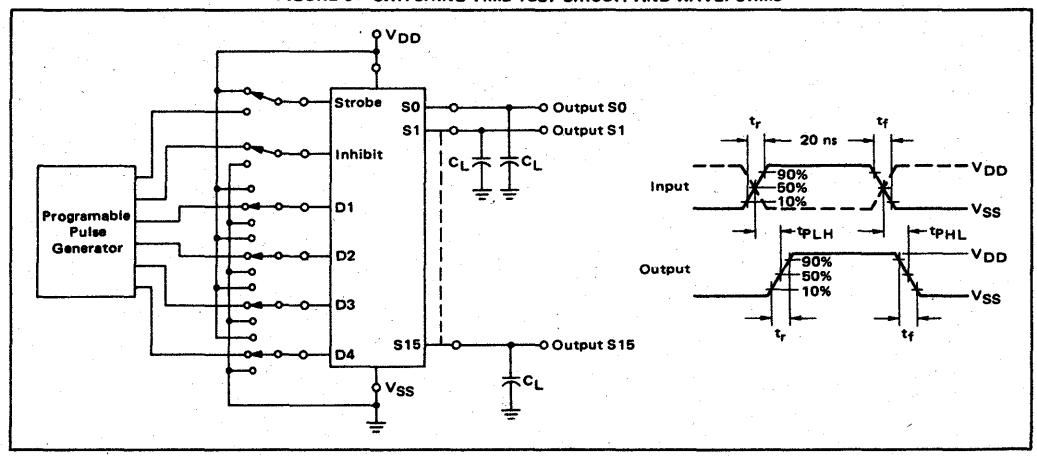


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



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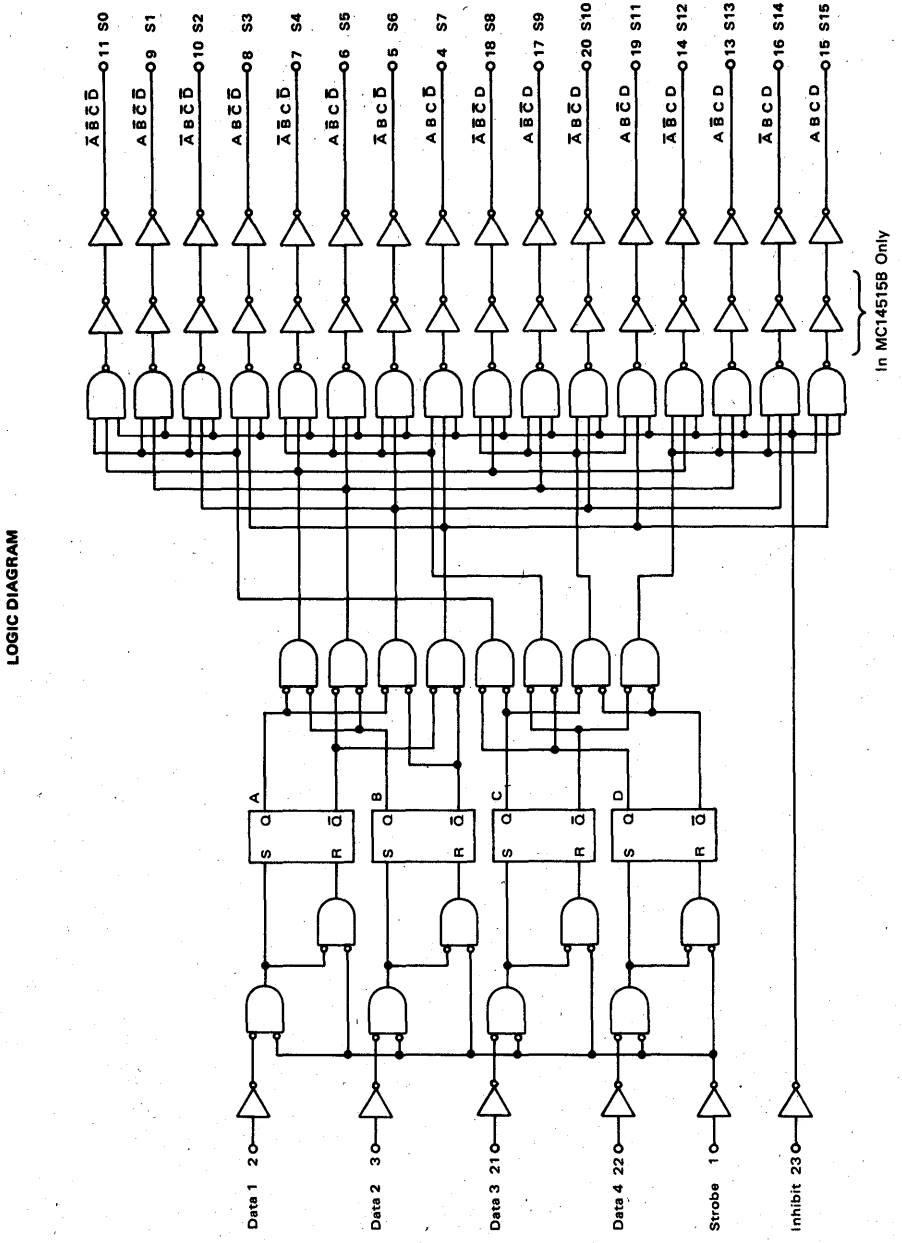
LOGIC DIAGRAM



COMPLEX DATA ROUTING

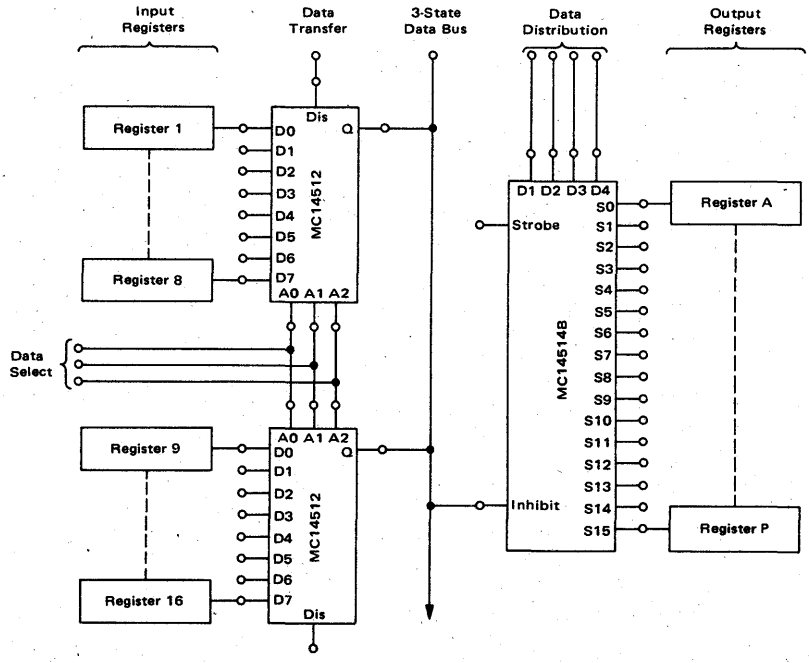
Two MC14512 eight-channel data selectors are used here with the MC14514B four-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3-state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on A0, A1, and A2 choose one of eight inputs for transfer out to the 3-state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3-state bus is redistributed by the MC14514B four-bit latch/decoder. Using the four-bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

DATA ROUTING SYSTEM



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14516B

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

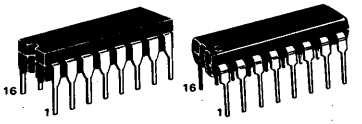
BINARY UP/DOWN COUNTER

BINARY UP/DOWN COUNTER

The MC14516B is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This complementary MOS circuit finds primary use where low power dissipation and/or high noise immunity is desired.

This binary presettable up/down counter may be used as a counting/frequency synthesizer, in A/D and D/A conversion, for up/down counting, for magnitude and sign generation, and for difference counting.

- Quiescent Current = 5.0nA/package typical @ 5.0 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance — 5.0 pF typical
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design — Count Occurs on Positive Going Edge of Clock
- 5.0-MHz Counting Rate
- Single Pin Reset
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



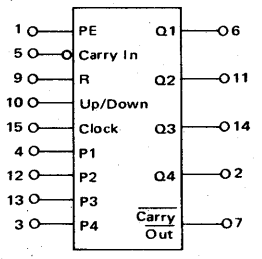
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.7 μA/kHz) f + I_{DD}							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

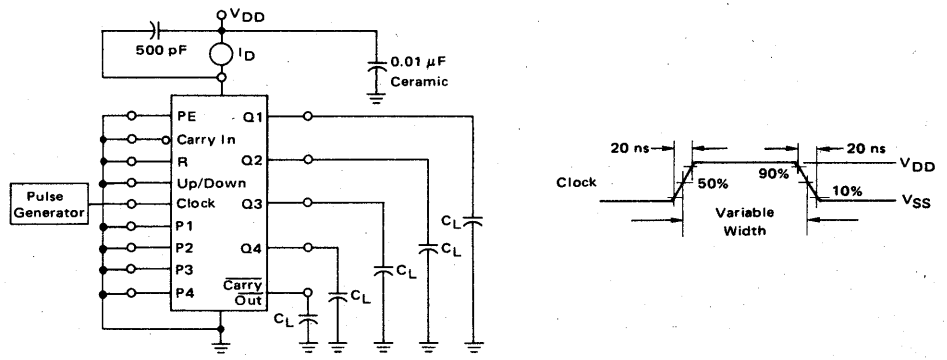
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Clock to Carry Out	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Carry In to Carry Out	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 95 ns		5.0	–	180	360	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 74 ns		10	–	80	160	
t_{PLH}, t_{PHL} = 0.5 ns/pF) C_L + 35 ns		15	–	60	120	
Preset or Reset to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	300	
Preset or Reset to Carry Out	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
Minimum Clock Pulse Width	PW_C	5.0	–	200	400	ns
		10	–	100	200	
		15	–	75	150	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	3.0	–	MHz
		10	3.0	6.0	–	
		15	4.0	8.0	–	
Preset or Reset Removal Time **	t_{rem}	5.0	–	325	650	ns
		10	–	115	230	
		15	–	90	180	
Maximum Clock Rise and Fall Time	t_r, t_f	5.0	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
Carry In Setup Time	t_{setup}	5.0	–	130	260	ns
		10	–	60	120	
		15	–	50	100	
Up/Down Setup Time	t_{setup}	5.0	–	250	500	ns
		10	–	100	200	
		15	–	75	150	
Minimum Preset Enable Pulse Width	PW_{PE}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

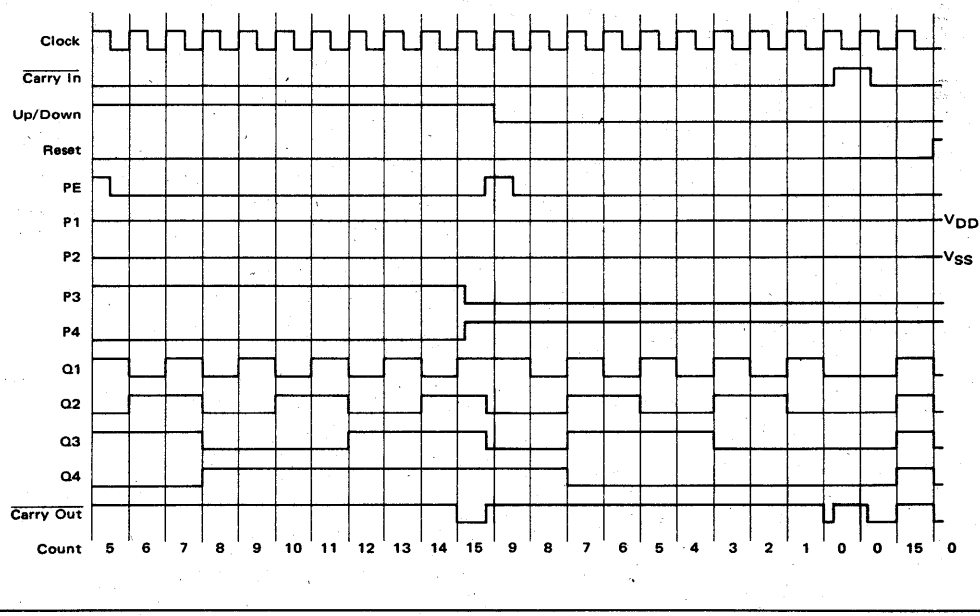
*The formula given is for the typical characteristics only.
**The Preset or Reset signal must be low prior to a positive-going transition of the clock.

5

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

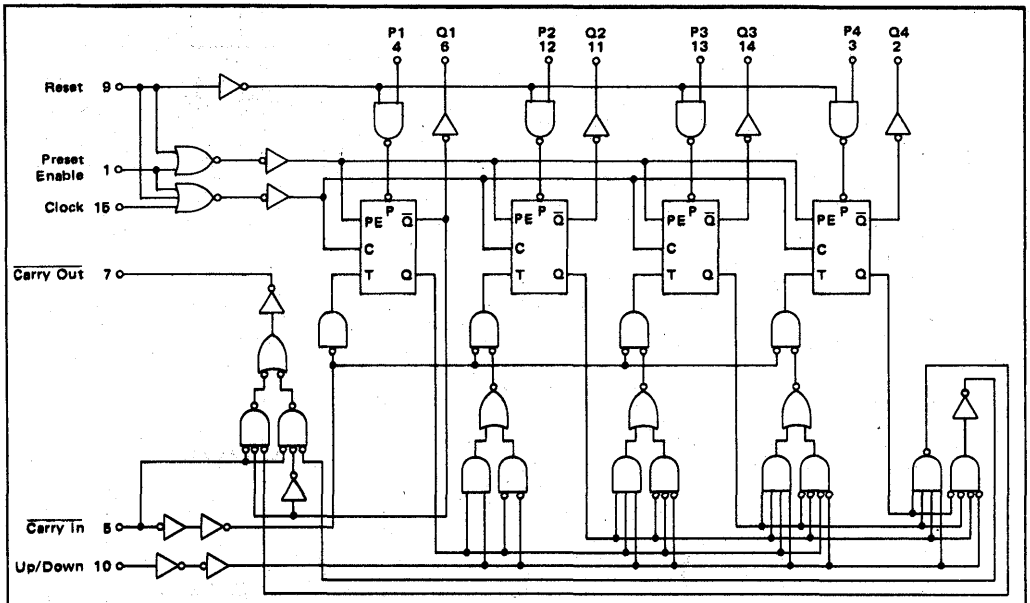


TIMING DIAGRAM

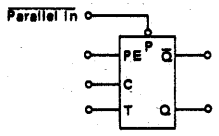


5

LOGIC DIAGRAM



TOGGLE FLIP-FLOP



FLIP-FLOP FUNCTIONAL TRUTH TABLE

PRESET ENABLE	CLOCK	TOGGLE ENABLE	Q_{n+1}
1	X	X	Parallel In
0	↑	0	Q_n
0	↑	1	$\overline{Q}_n$
0	↓	X	Q_n

X = Don't Care

FIGURE 2 – SWITCHING TIME WAVEFORMS

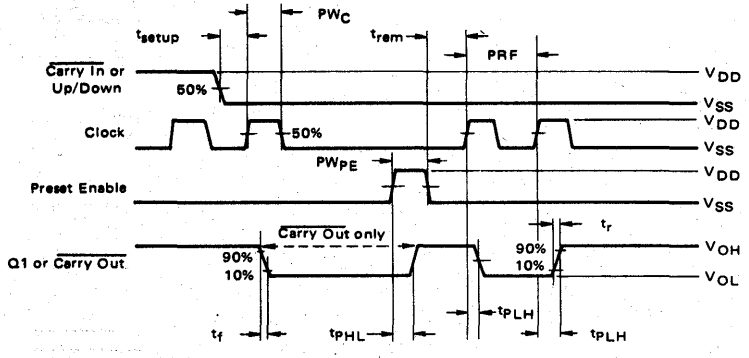


FIGURE 3 – PRESETTABLE CASCADED UP/DOWN COUNTER

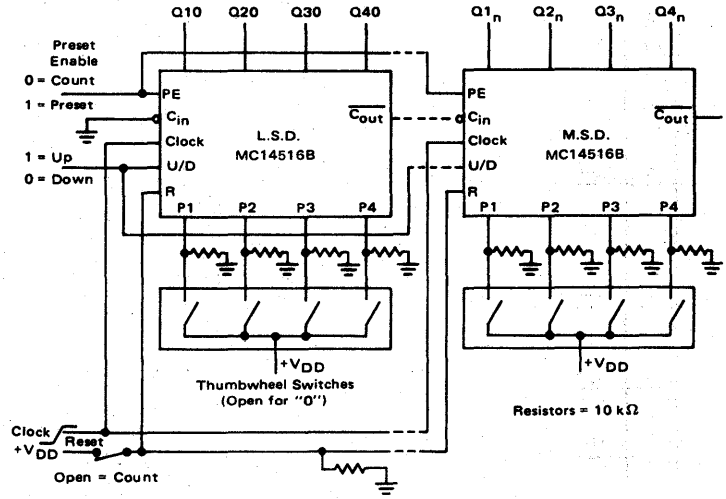
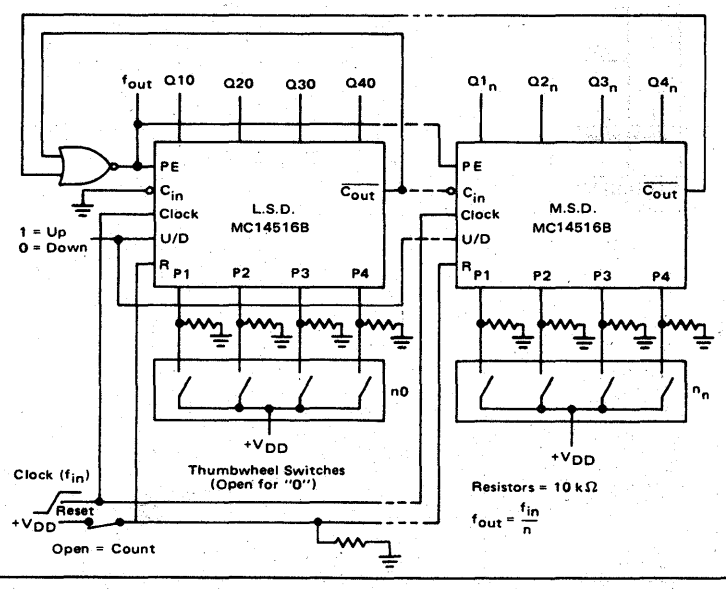


FIGURE 4 – PROGRAMMABLE CASCADED FREQUENCY DIVIDER



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MC14517B

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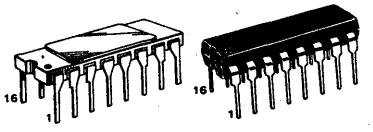
(LOW-POWER COMPLEMENTARY MOS)

DUAL 64-BIT STATIC SHIFT REGISTER

DUAL 64-BIT STATIC SHIFT REGISTER

The MC14517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

- Quiescent Current = 10 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- 6.7 MHz Operation @ V_{DD} = 10 Vdc
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3-State Output at 64th-Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



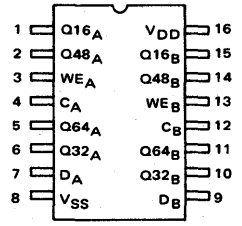
L SUFFIX
CERAMIC PACKAGE
CASE 690

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FUNCTIONAL TRUTH TABLE

CLOCK	WRITE ENABLE	DATA	16-BIT TAP	32-BIT TAP	48-BIT TAP	64-BIT TAP
0	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
⌐	0	Data entered into 1st Bit	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
⌐	1	Data entered into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 33-Bit	Data at tap entered into 49-Bit	High Impedance
¬	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
¬	1	X	High Impedance	High Impedance	High Impedance	High Impedance

X = Don't Care

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (4.2 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (8.8 µA/kHz) f + I_{DD}							
		15	I_T = (13.7 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 390 ns		5.0	–	–	475	590	770	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 177 ns		10	–	–	210	245	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 115 ns		15	–	–	140	175	215	
Minimum Clock Pulse Width	PW_C	5.0	–	–	170	250	330	ns
		10	–	–	75	100	125	
		15	–	–	60	75	100	
Maximum Clock Pulse Frequency	PRF	5.0	2.0	1.5	3.0	–	–	MHz
		10	5.0	4.0	6.7	–	–	
		15	6.7	5.3	8.3	–	–	
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0	–	–	–	No	No	–
		10	–	–	–	Limit	Limit	
		15	–	–	–	**	**	
Data to Clock Setup Time	t_{setup}	5.0	–	–	-40	-10	0	ns
		10	–	–	-15	0	10	
		15	–	–	0	5	15	
Data to Clock Hold Time	t_{hold}	5.0	–	–	75	120	150	ns
		10	–	–	25	50	75	
		15	–	–	10	25	35	
Write Enable to Clock Setup Time	t_{setup}	5.0	–	–	170	300	400	ns
		10	–	–	65	130	200	
		15	–	–	50	80	110	
Write Enable to Clock Release Time	t_{rel}	5.0	–	–	160	280	380	ns
		10	–	–	55	120	180	
		15	–	–	40	70	100	

*The formula given is for the typical characteristics only.

**When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage for the output capacitance load.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

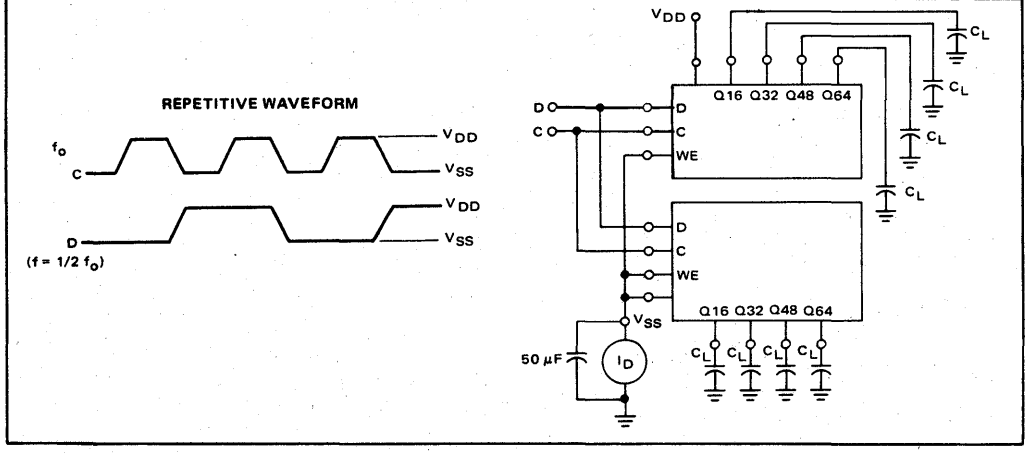
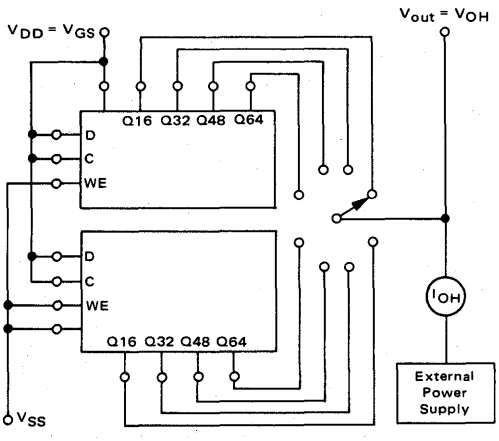
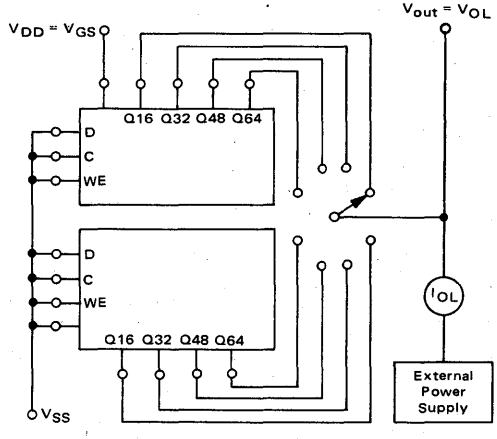


FIGURE 2 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT



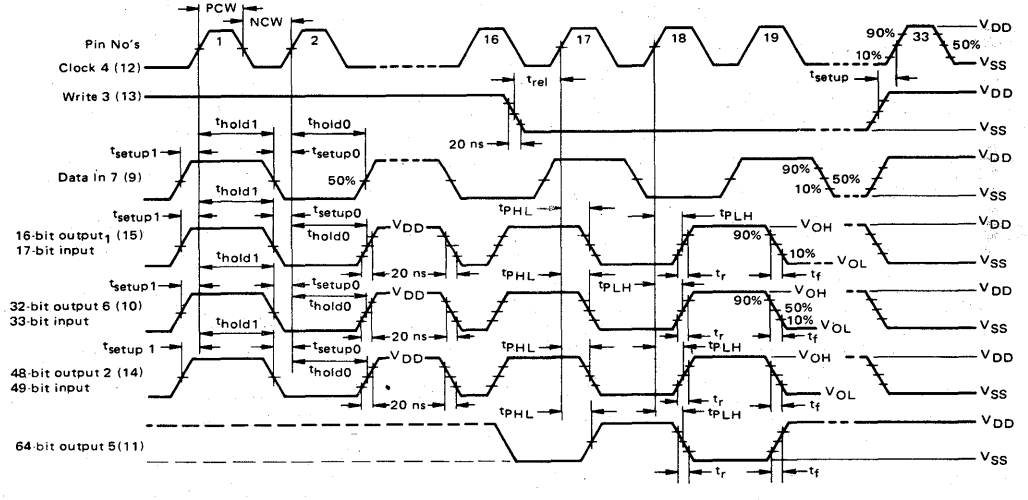
(Output being tested should be in the high-logic state).

FIGURE 3 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT

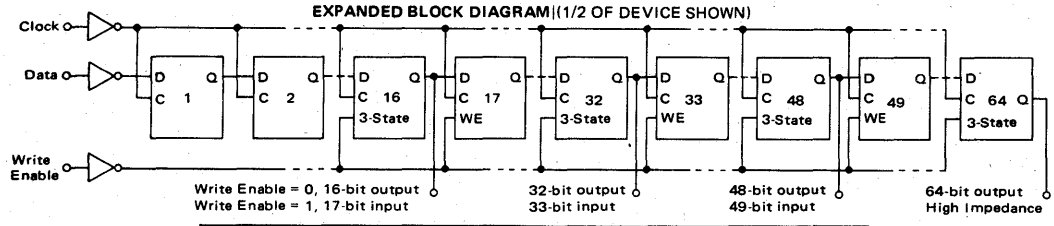


(Output being tested should be in the low-logic state).

FIGURE 4 – AC TEST WAVEFORMS



EXPANDED BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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BOX 20912 • PHOENIX, ARIZONA 85036

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McMOS MSI

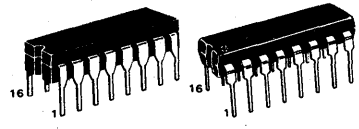
(LOW-POWER COMPLEMENTARY MOS)

DUAL BCD UP COUNTER
(MC14518B)
DUAL BINARY UP COUNTER
(MC14520B)

DUAL UP COUNTERS

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity. Additional characteristics can be found on the Family Data Sheet.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design — Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



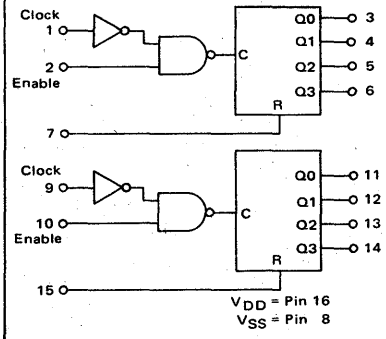
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–		5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.6 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.7 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	280	560	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	115	230	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	80	160	
Reset to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	330	660	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 95 ns		15	–	90	180	
Minimum Clock Pulse Width	PW_{CH}, PW_{CL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	35	70	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	2.5	–	MHz
		10	3.0	6.0	–	
		15	4.0	8.0	–	
Maximum Clock or Enable Rise and Fall Time	t_r, t_f	5.0	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
Minimum Enable Pulse Width	PW_E	5.0	–	220	440	ns
		10	–	100	200	
		15	–	70	140	
Minimum Reset Pulse Width	PW_R	5.0	–	125	250	ns
		10	–	55	110	
		15	–	40	80	

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

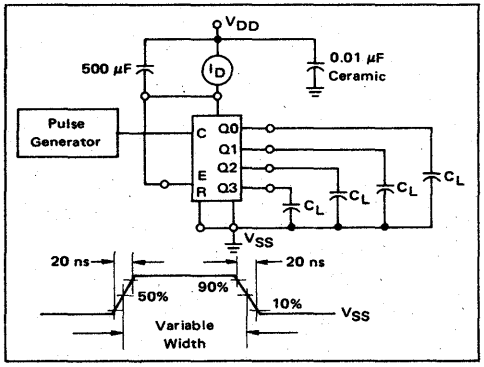


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

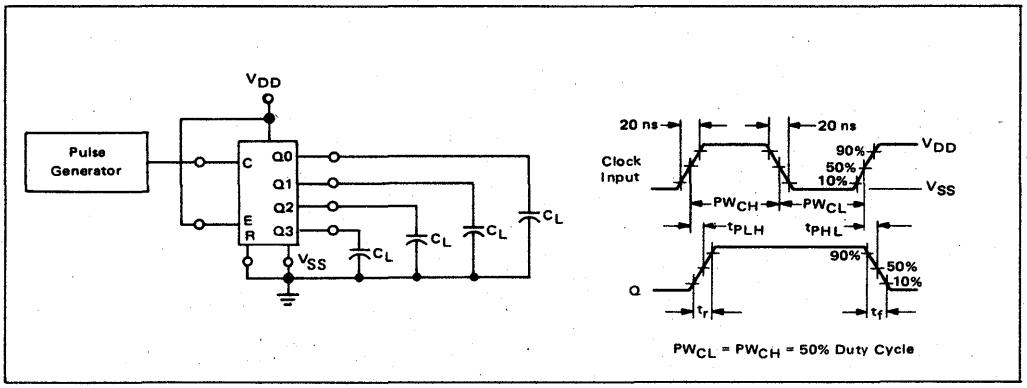


FIGURE 3 – TIMING DIAGRAM

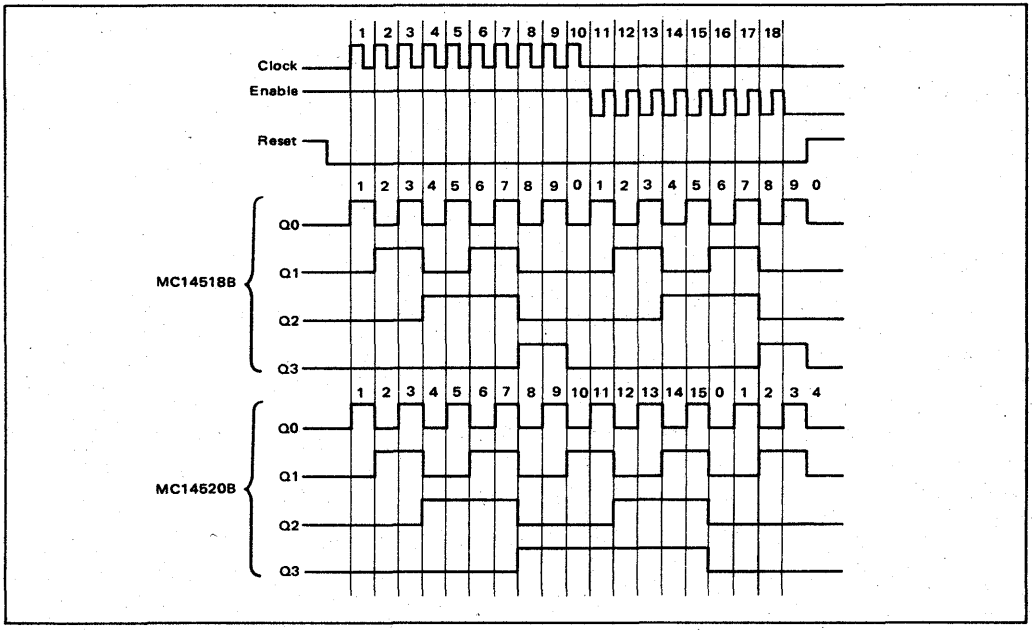


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FIGURE 4 – DECADE COUNTER (MC14518B) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)

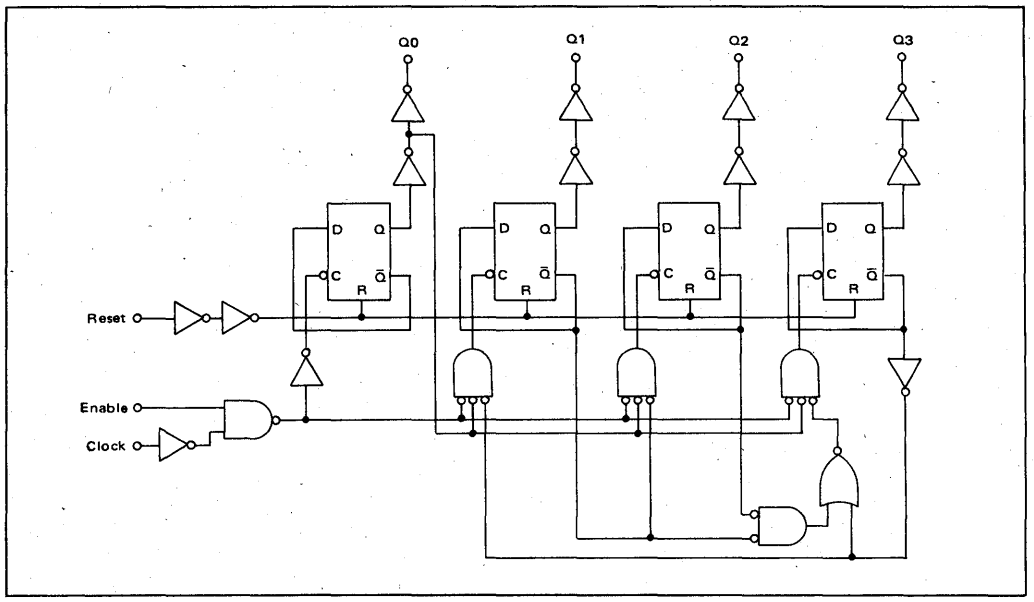
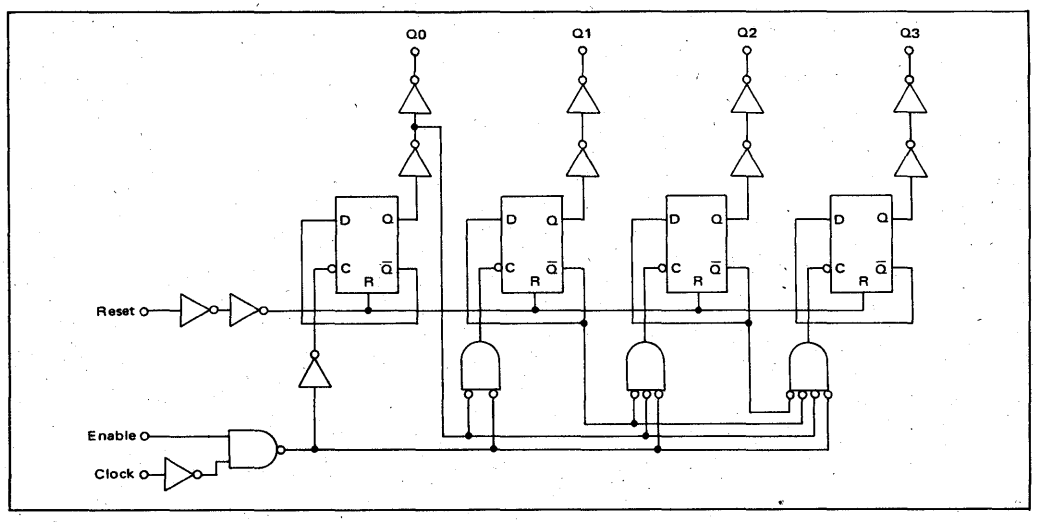


FIGURE 5 – BINARY COUNTER (MC14520B) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)



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MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14519B

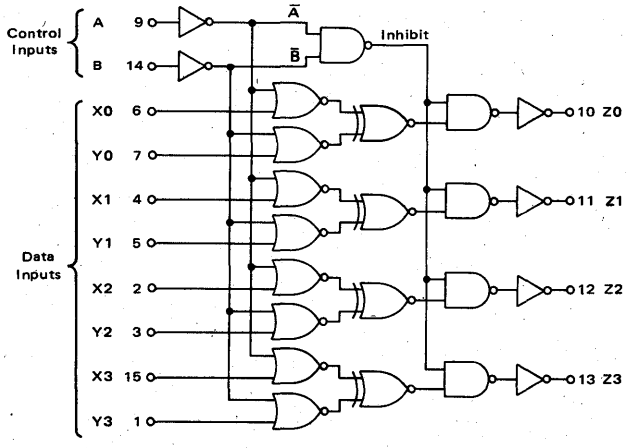
4-BIT AND/OR SELECTOR
or
QUAD 2-CHANNEL DATA SELECTOR
or
QUAD EXCLUSIVE "NOR" GATE

The MC14519B is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device exemplifies the design versatility of McMOS logic structure. This part provides three functions in one package; a 4-Bit AND/OR Selector, a Quad 2-Channel Data Selector, or a Quad Exclusive NOR Gate.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Plug-In Replacement for CD4019 in Most Applications

LOGIC DIAGRAM
(Positive Logic)

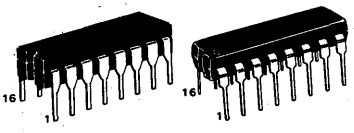


V_{DD} = Pin 16
V_{SS} = Pin 8

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT AND/OR SELECTOR



L SUFFIX	P SUFFIX
CERAMIC PACKAGE	PLASTIC PACKAGE
CASE 620	CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

TRUTH TABLE

CONTROL INPUTS		OUTPUT
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \circledcirc Y_n$

Note:
$X_n \circledcirc Y_n$ means X_n (Exclusive-NOR) Y_n

5

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range -- AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.2 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.4 μA/kHz) f + I_{DD}							
		15	I_T = (3.6 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 165 ns		5.0	250	375	500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 82 ns		10	115	170	225	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	90	135	165	

*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

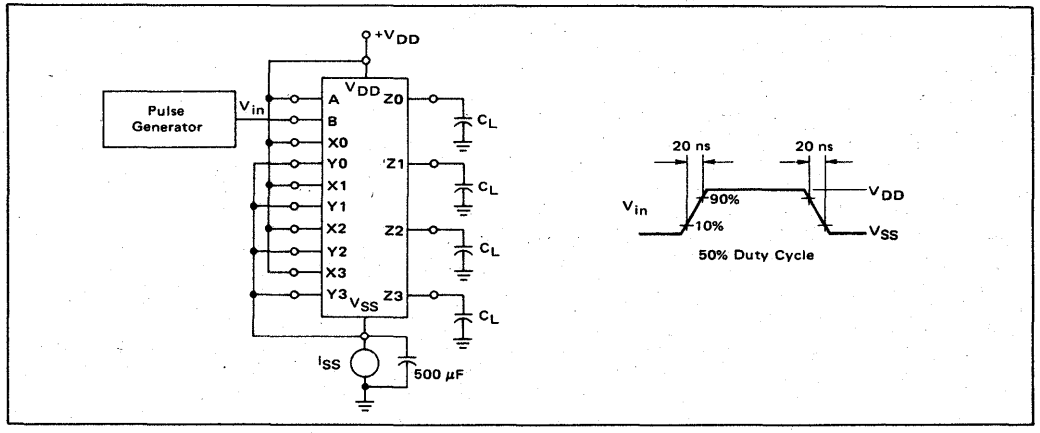
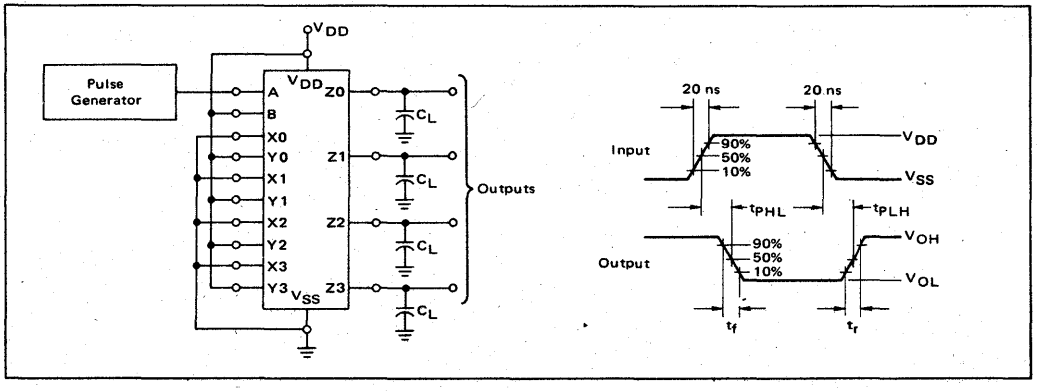


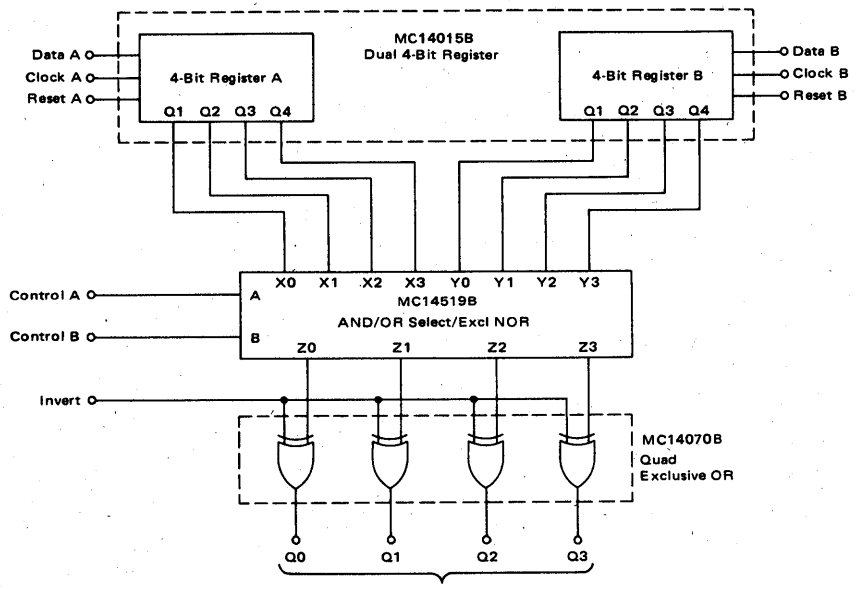
FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



5

TYPICAL CIRCUIT APPLICATIONS

DATA REGISTER SELECTION COMPARISON



CONVERSION TABLE

OPERATION CODE			OUTPUT				FUNCTION
A	B	INV	Q0	Q1	Q2	Q3	
0	0	0	0	0	0	0	Inhibit, all zeros
0	0	1	1	1	1	1	Inhibit, all ones
1	0	0	X0	X1	X2	X3	Control A
1	0	1	$\overline{X0}$	$\overline{X1}$	$\overline{X2}$	$\overline{X3}$	Control A and Invert
0	1	0	Y0	Y1	Y2	Y3	Control B
0	1	1	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	Control B and Invert
1	1	0	X0 ⊙ Y0	X1 ⊙ Y1	X2 ⊙ Y2	X3 ⊙ Y3	Exclusive NOR
1	1	1	X0 ⊕ Y0	X1 ⊕ Y1	X2 ⊕ Y2	X3 ⊕ Y3	Exclusive OR

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MC14520B

FOR COMPLETE DATA
SEE MC14518B

DUAL UP COUNTERS

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity. Additional characteristics can be found on the Family Data Sheet.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design — Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

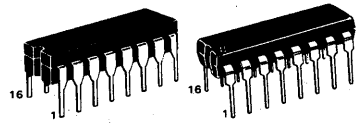
CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL BCD UP COUNTER
(MC14518B)
DUAL BINARY UP COUNTER
(MC14520B)



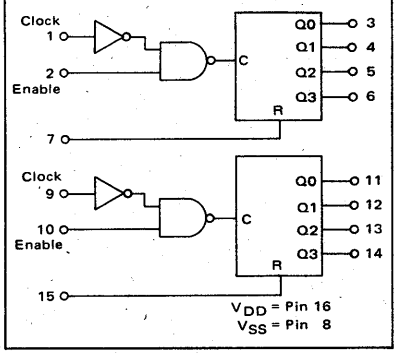
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MC14521B

24-STAGE FREQUENCY DIVIDER

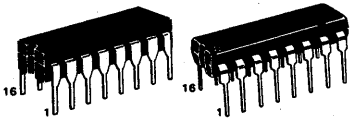
The MC14521B consists of a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip-flop divides the frequency of the previous flip-flop by two, consequently this part will count up to 2^{24} = 16,777,216. The count advances on the negative going edge of the clock. The outputs of the last seven-stages are available for added flexibility.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- $f_{(max)}$ = 9.0 MHz typical @ V_{DD} = 10V
- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- V_{DD}' and V_{SS}' Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low-Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

24-STAGE FREQUENCY DIVIDER



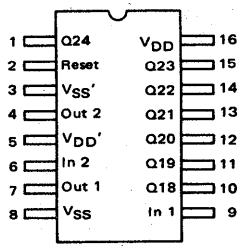
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

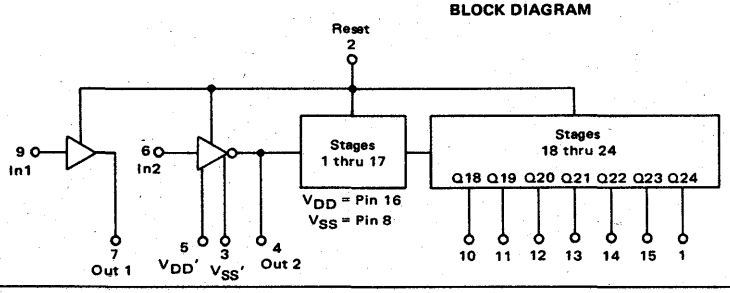
PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



OUTPUT	COUNT CAPACITY
Q18	2^{18} = 262,144
Q19	2^{19} = 524,288
Q20	2^{20} = 1,048,576
Q21	2^{21} = 2.097,152
Q22	2^{22} = 4,194,304
Q23	2^{23} = 8,388,608
Q24	2^{24} = 16,777,216

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.42 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.85 µA/kHz) f + I_{DD}							
		15	I_T = (1.4 µA/kHz) f + I_{DD}							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

5

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	110	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time Clock to Q18	t_{PLH}, t_{PHL}							µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 4415 ns		5.0	–	–	4.5	9.0	13.5	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 1667 ns		10	–	–	1.7	3.5	5.2	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 1175 ns		15	–	–	1.2	2.7	3.9	
Clock to Q24								µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5915 ns		5.0	–	–	6.0	12	18	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 2167 ns		10	–	–	2.2	4.5	6.5	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 1475 ns		15	–	–	1.5	3.5	5.0	
Propagation Delay Time Reset to Q_n	t_{PHL}							ns
t_{PHL} = (1.7 ns/pF) C_L + 1215 ns		5.0	–	–	1300	2600	4000	
t_{PHL} = (0.66 ns/pF) C_L + 467 ns		10	–	–	500	1000	1500	
t_{PHL} = (0.5 ns/pF) C_L + 325 ns		15	–	–	350	750	1200	
Minimum Clock Pulse Width	PW_C	5.0	–	–	140	250	385	ns
		10	–	–	55	100	150	
		15	–	–	40	75	120	
Maximum Clock Pulse Frequency	PRF	5.0	2.0	1.5	3.5	–	–	MHz
		10	5.0	3.5	9.0	–	–	
		15	6.5	4.5	12	–	–	
Maximum Clock Rise and Fall Time	t_r,t_f	5.0	15	15	–	–	–	µs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
Minimum Reset Pulse Width	PW_R	5.0	–	–	700	1400	1800	ns
		10	–	–	300	600	900	
		15	–	–	200	450	700	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

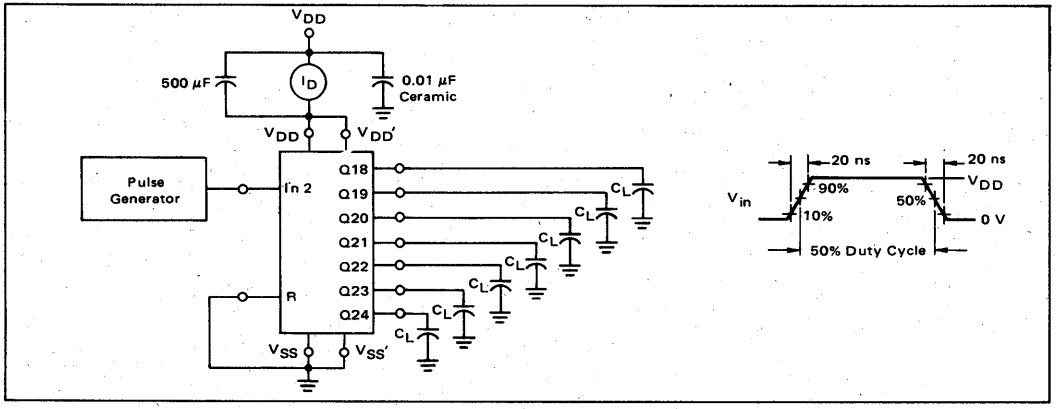


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

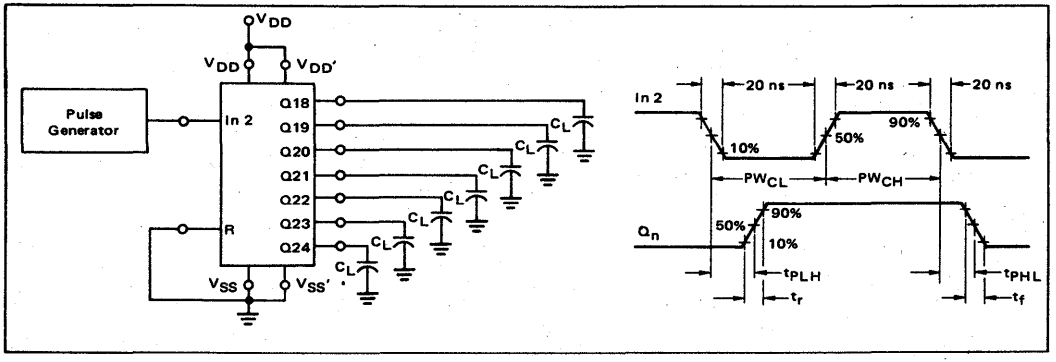
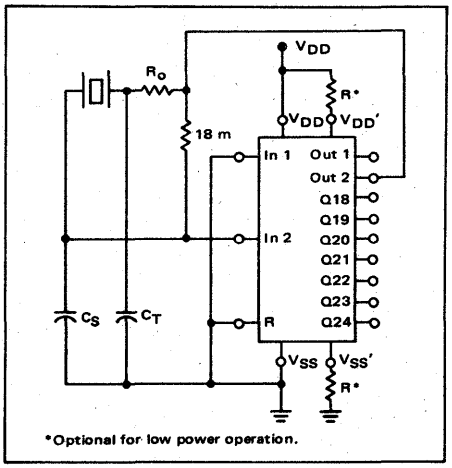


FIGURE 3 – CRYSTAL OSCILLATOR CIRCUIT



*Optional for low power operation.

FIGURE 4 – TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

CHARACTERISTIC	500 kHz CIRCUIT	50 kHz CIRCUIT	UNIT
Crystal Characteristics			
Resonant Frequency	500	50	kHz
Equivalent Resistance, R_S	1.0	6.2	kΩ
External Resistor/Capacitor Values			
R_o	47	750	kΩ
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Change as a Function of V_{DD} (T_A = 25°C)			
V_{DD} Change from 5.0 V to 10 V	+6.0	+2.0	ppm
V_{DD} Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature (V_{DD} = 10 V)			
T_A Change from -55°C to +25°C			
MC14521 only	-4.0	-2.0	ppm
Complete Oscillator*	+100	+120	ppm
T_A Change from +25°C to +125°C			
MC14521 only	-2.0	-2.0	ppm
Complete Oscillator*	-160	-560	ppm

*Complete oscillator includes crystal, capacitors, and resistors.

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FIGURE 5 – RC OSCILLATOR STABILITY

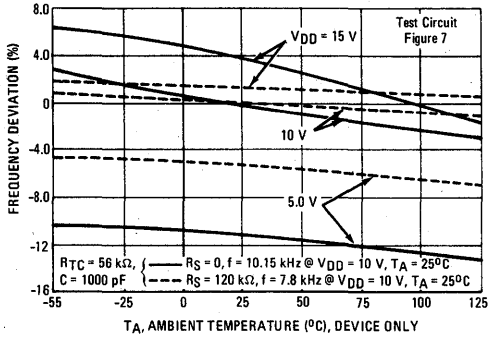


FIGURE 6 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C

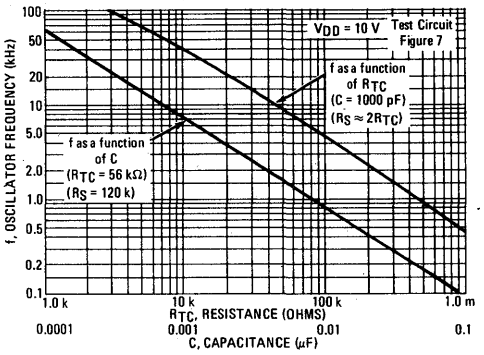


FIGURE 7 – RC OSCILLATOR CIRCUIT

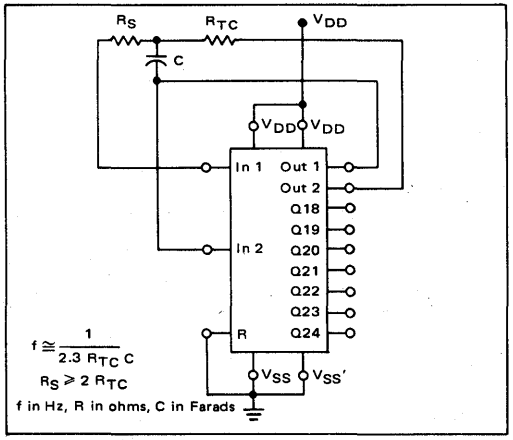
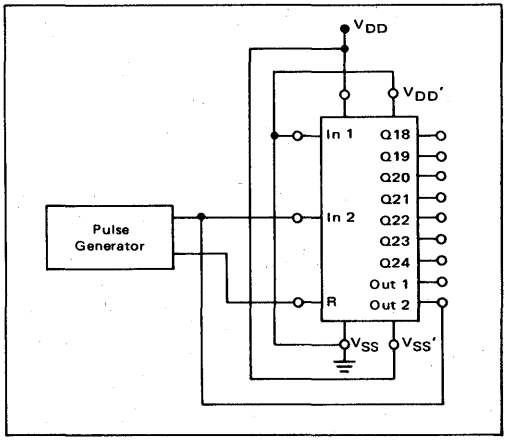


FIGURE 8 – FUNCTIONAL TEST CIRCUIT

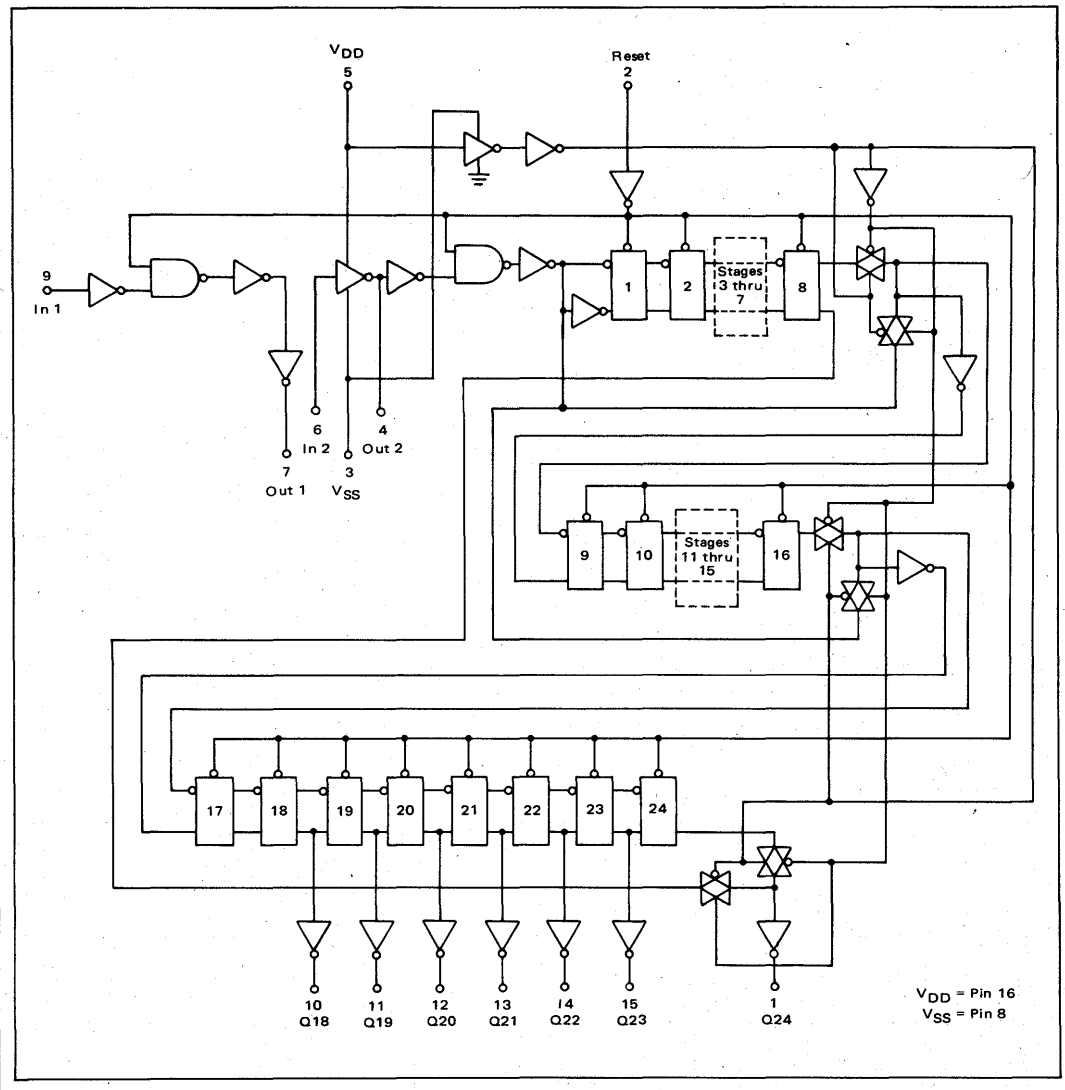


FUNCTIONAL TEST SEQUENCE

A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections, and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a logic "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all "1" state to an all "0" state.

INPUTS		OUTPUTS				COMMENTS
Reset	In 2	Out 2	V_{SS}'	V_{DD}'	Q18 thru Q24	
1	0	0	V_{DD}	Gnd	0	Counter is in three 8-stage sections in parallel mode Counter is reset. In 2 and Out 2 are connected together
0	1	1				First "0" to "1" transition on In 2, Out 2 node.
	0	0				255 "0" to "1" transitions are clocked into this In 2, Out 2 node.
	1	1				
	–	–				
	–	–				
	–	–				
	1	1			1	The 255th "0" to "1" transition.
	0	0			1	
	0	0	Gnd		1	
	1	0		V_{DD}	1	Counter converted back to 24-stages in series mode.
	1				1	Out 2 converts back to an output.
	0				0	Counter ripples from an all "1" state to an all "0" stage.

LOGIC DIAGRAM



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MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14522B
MC14526B

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

BCD – MC14522B
Binary – MC14526B

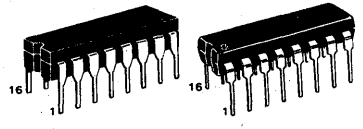
PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

The MC14522B BCD counter and the MC14526B binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure.

These devices are programmable, cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds.
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition of Clock Inhibit
- 5.0 MHz Counting Rate
- Asynchronous Preset Enable
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

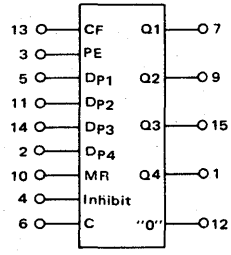
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

5

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLES

BOTH TYPES

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
↓	0	0	0	Count-1
X	1	0	0	No Count
1	↓	0	0	Count-1
X	X	1	0	Preset
X	X	X	1	Reset

MC14522B

Count	Output Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC14526B

Count	Output Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.7 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.4 µA/kHz) f + I_{DD}							
		15	I_T = (5.1 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min		Typ	Max		Unit
			AL Device	CL/CP Device	All Types	AL Device	CL/CP Device	
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}							ns
Q Outputs								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	–	550	825	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	–	230	234	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns		15	–	–	160	240	340	
"0" Output								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 155 ns		5.0	–	–	240	360	500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns		10	–	–	120	250	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	–	90	190	225	
Minimum Clock Pulse Width	PW_C	5.0	–	–	100	250	300	ns
		10	–	–	50	100	150	
		15	–	–	40	75	115	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	2.0	–	–	MHz
		10	3.0	2.5	5.0	–	–	
		15	4.0	3.0	6.6	–	–	
Maximum Clock or Inhibit Rise and Fall Time	t_r, t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
Hold Time	t_{hold}	5.0	–	–	75	125	150	ns
		10	–	–	25	50	75	
		15	–	–	20	40	60	
Minimum Preset Enable Pulse Width	PW_{PE}	5.0	–	–	100	250	300	ns
		10	–	–	50	100	150	
		15	–	–	40	75	115	
Minimum Master Reset Pulse Width	PW_{MR}	5.0	–	–	200	300	350	ns
		10	–	–	100	250	300	
		15	–	–	75	200	225	

*The formula given is for the typical characteristics only.

5

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

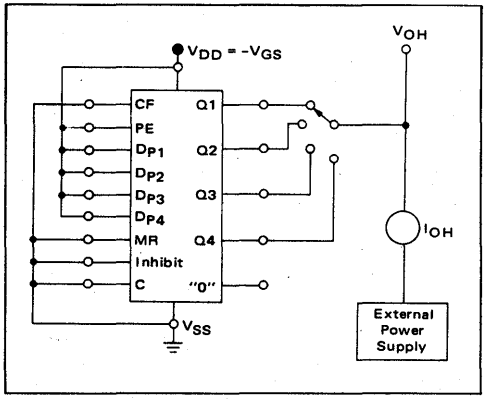


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

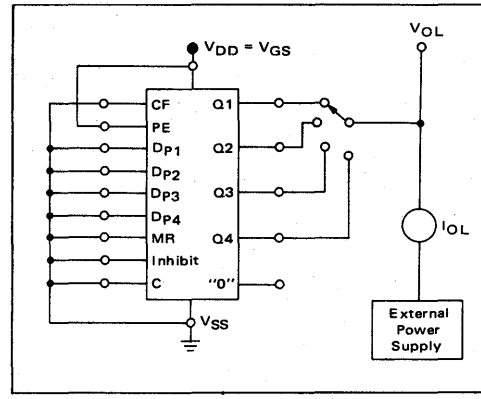


FIGURE 3 – POWER DISSIPATION

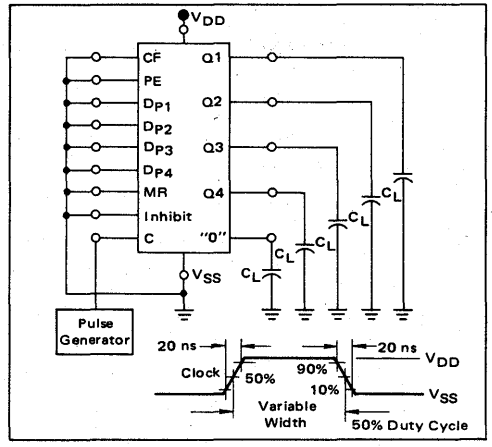


FIGURE 4 – AC TEST CIRCUITS

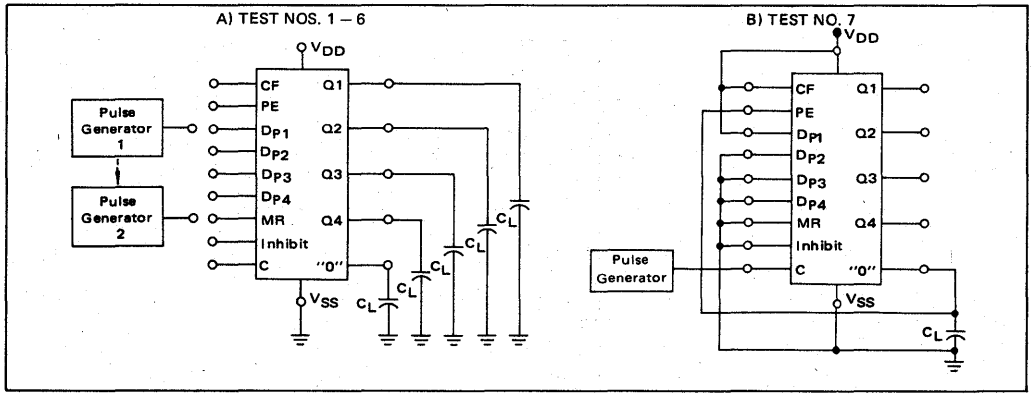
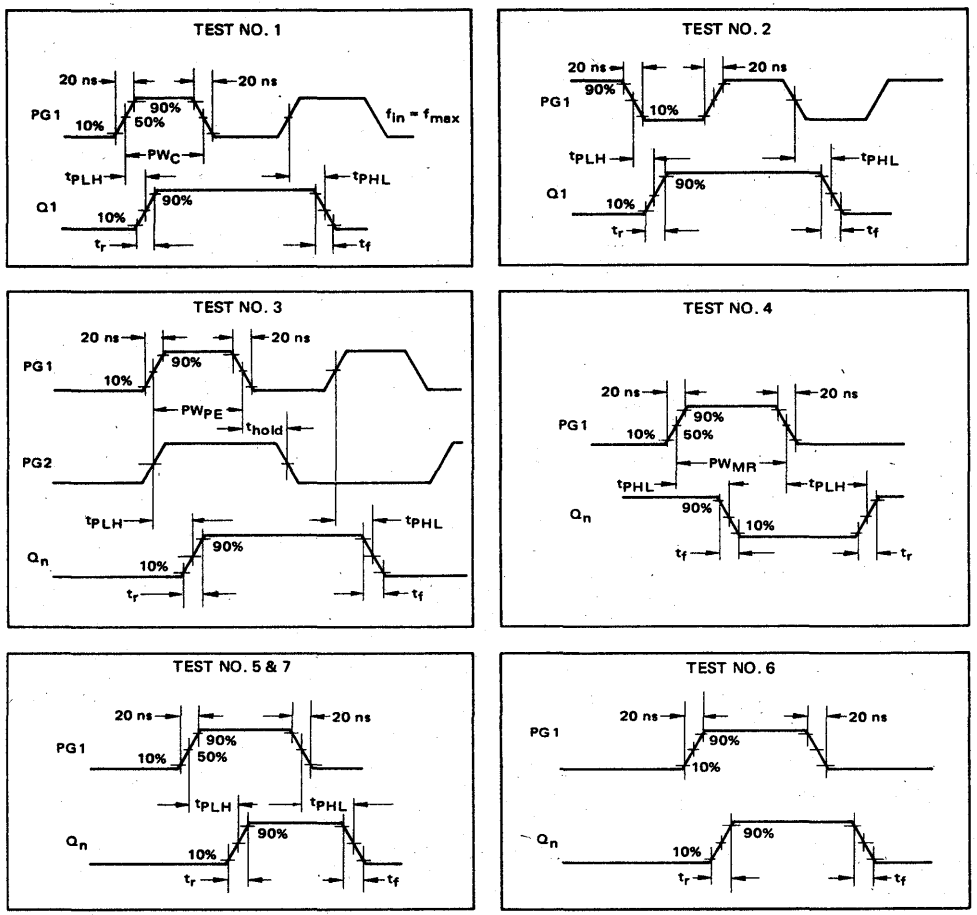


FIGURE 5 – AC TEST CONNECTIONS AND WAVEFORMS



CHARACTERISTIC	TEST NO.	CLOCK	INHIBIT	PE	MR	D_{Pn}	CF	OUTPUT
$t_r, t_f, t_{PLH}, t_{PHL}$	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	2	V_{DD}	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
	5	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	V_{SS}	Q_n
PW_{MR}	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
PW_{PE}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
PW_C	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
f_{Max}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
t_{hold}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
t_r, t_f	6	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	"0"
t_{PLH}, t_{PHL}	7	PG	V_{SS}	Fig 4B	V_{SS}	Fig 4B	V_{DD}	"0"

FIGURE 6 – MC14522B LOGIC DIAGRAM (BCD Divide-by-N Counter)

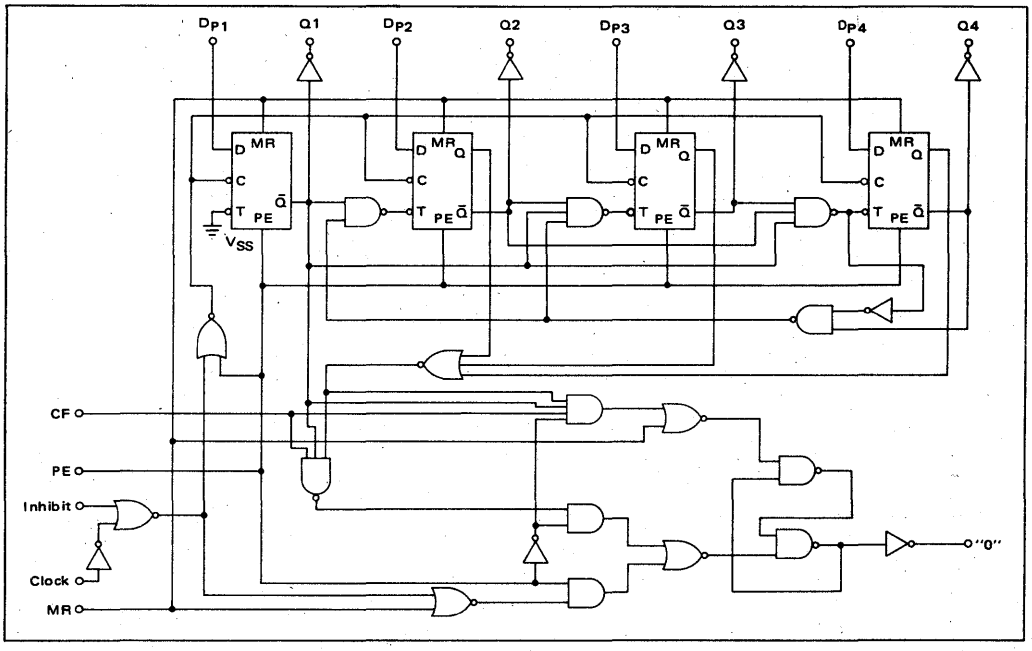


FIGURE 7 – MC14526B LOGIC DIAGRAM (Binary Divide-by-N Counter)

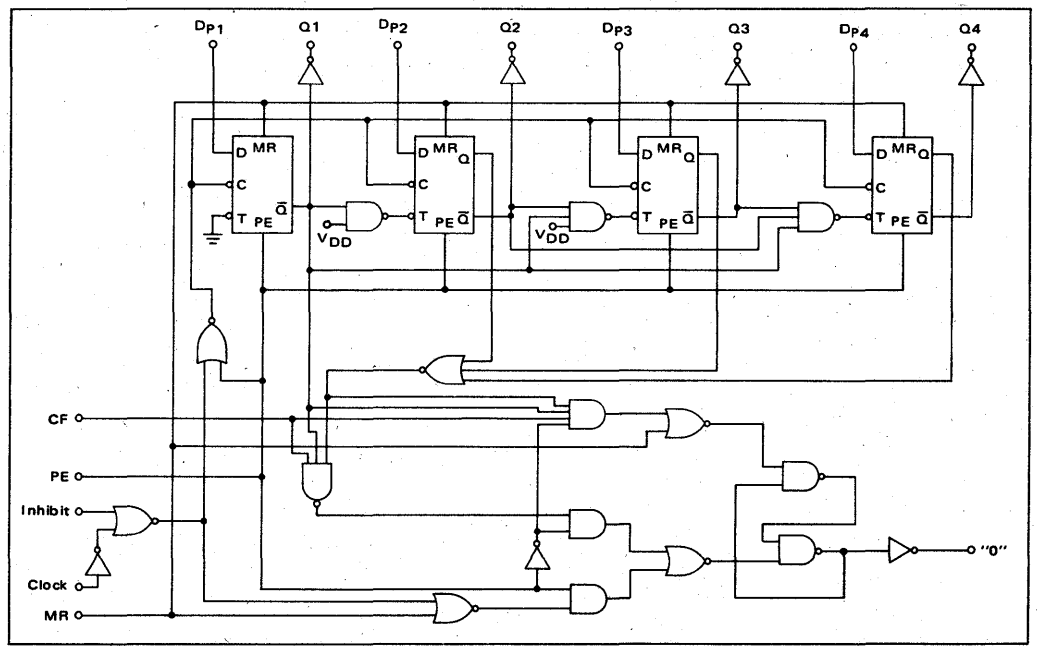


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FIGURE 8 – 2-STAGE PROGRAMMABLE DOWN COUNTER
(One Cycle)

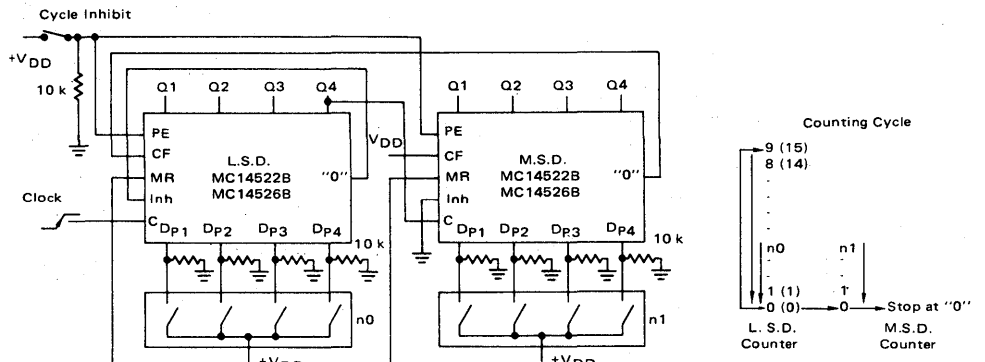
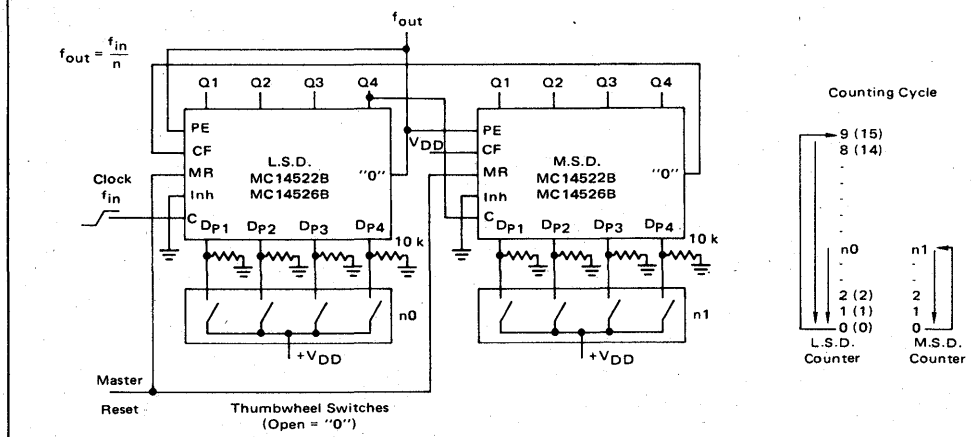


FIGURE 9 – 2-STAGE PROGRAMMABLE FREQUENCY DIVIDER



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MCM14524

McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

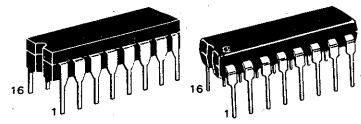
1024-BIT
(256 x 4)
READ ONLY MEMORY

1024-BIT READ ONLY MEMORY

The MCM14524 is a complementary MOS mask programmable Read Only Memory (ROM). This device is ordered as a factory special with its unique pattern specified by the user.

This ROM is organized in a 256 x 4-bit pattern. The contents of a specified address (< A0, A1, A2, A3, A4, A5, A6, A7 >) will appear at the four data outputs (B0, B1, B2, B3) following the negative going edge of the clock. When the clock goes high, the data present at the output will be latched. The memory Enable may be taken low asynchronously, forcing the data outputs low and resetting the output latches. This device finds application wherever low power or high noise immunity is a design consideration.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- Quiescent Current – 10 nA/package typical @ 5 Vdc
- Single Supply Operation – Either Positive or Negative
- Memory Enable Allows Expansion
- Output Latches Provide a Useful Storage Register
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

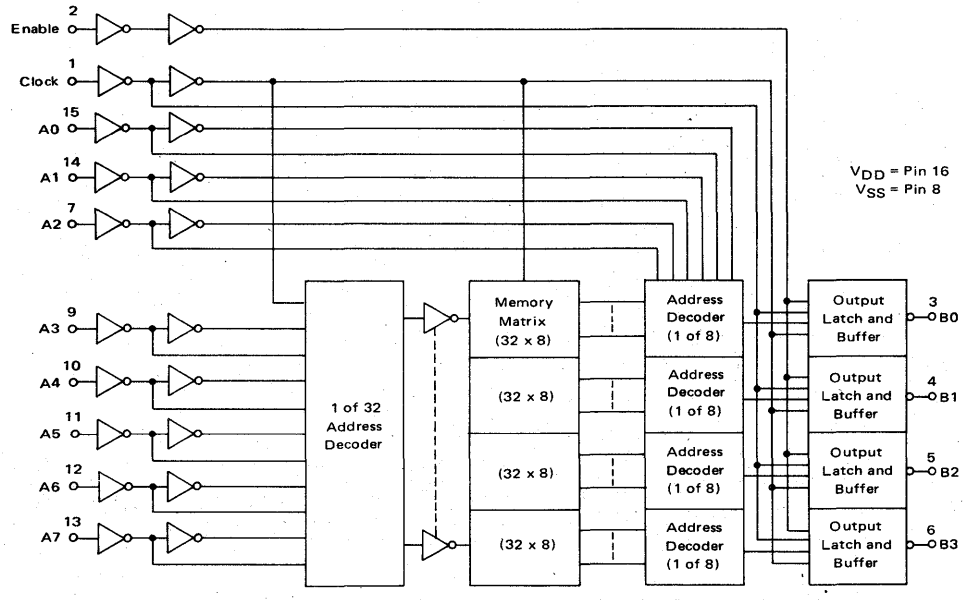
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

5

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.01	–	0	0.01	–	0.05	
"1" Level	V_{OH}	5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.99	–	14.99	15	–	14.95	–	
Noise Immunity #	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	3.75	–	3.75	6.75	–	3.75	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	3.65	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_Q	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_Q	5.0	–	50	–	0.010	50	–	375	µAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.6\ \mu A/kHz)\ f + I_Q$							µAdc
		10	$I_T = (3.2\ \mu A/kHz)\ f + I_Q$							
		15	$I_T = (4.8\ \mu A/kHz)\ f + I_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$$

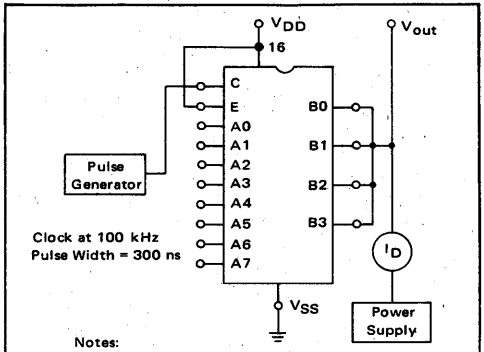
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Type	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r,t_f = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r,t_f = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r,t_f = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_r,t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_r,t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_r,t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Clock Read Access Delay Time	t_{accC}							ns
t_{accC} = (1.7 ns/pF) C_L + 1265 ns		5.0	–	–	1350	2650	4000	
t_{accC} = (0.66 ns/pF) C_L + 517 ns		10	–	–	550	1050	1600	
t_{accC} = (0.5 ns/pF) C_L + 325 ns		15	–	–	350	800	1200	
Enable Access Delay Time	t_{accEn}							ns
t_{accEn} = (1.7 ns/pF) C_L +160 ns		5.0	–	–	245	380	615	
t_{accEn} = (0.66 ns/pF) C_L + 77 ns		10	–	–	110	165	265	
t_{accEn} = (0.5 ns/pF) C_L + 50 ns		15	–	–	75	120	190	
Minimum Clock Pulse Width*	PW_{CH}	5.0	–	–	150	300	450	ns
		10	–	–	55	110	165	
		15	–	–	35	85	125	
	PW_{CL}	5.0	–	–	1200	2400	3600	ns
		10	–	–	475	950	1425	
		15	–	–	300	715	1070	
Maximum Low Clock Pulse Width#	PW_{CL}	5.0	5.0	2.0	10	–	–	ms
		10	1.5	0.9	3.0	–	–	
		15	0.15	0.1	0.3	–	–	
Address Setup Time	t_{setupA}	5.0	0	0	0	–	–	ns
		10	0	0	0	–	–	
		15	0	0	0	–	–	
Address Hold Time	t_{holdA}	5.0	0	0	0	–	–	ns
		10	0	0	0	–	–	
		15	0	0	0	–	–	
Minimum Clock to Enable Setup Time	t_{setupC}	5.0	–	–	1425	2850	4275	ns
		10	–	–	575	1150	1725	
		15	–	–	400	865	1295	
Minimum Clock to Enable Hold Time	t_{holdC}	5.0	–	–	0	100	150	ns
		10	–	–	0	50	75	
		15	–	–	0	40	55	

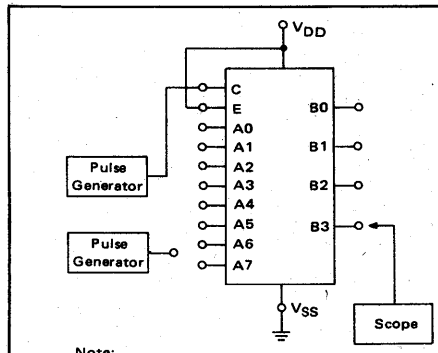
*The clock can remain high indefinitely with the data remaining latched.
#If clock stays low too long, the dynamically stored data will leak off and will have to be recalled.

FIGURE 1 – OUTPUT DRIVE CURRENT TEST CIRCUIT



Notes:
1. Source current, address ROM to obtain a "1" on all four outputs (B0 thru B3).
2. Sink current, address ROM to obtain a "0" on all four outputs (B0 thru B3).

FIGURE 2 – SWITCHING TIME TEST CIRCUIT (Refer to timing diagram)

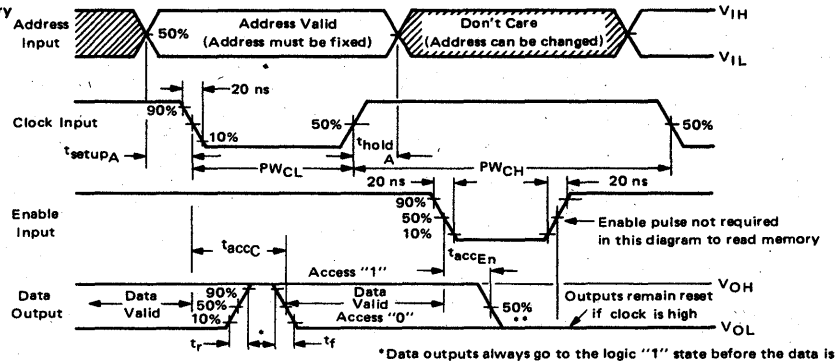


Note:
Address ROM to obtain level change when clocking any one address line.

5

MEMORY READ CYCLE TIMING DIAGRAMS

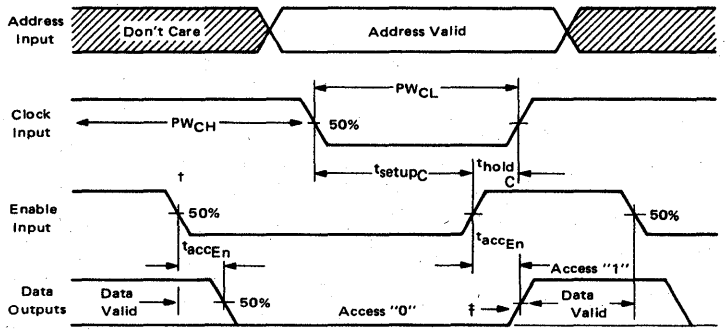
a) Using Clock to Read Memory



*Data outputs always go to the logic "1" state before the data is valid between accessing successive "0's"

**Outputs forced to "0" by Enable.

b) Using the Enable to Read Memory



† In this mode of operation, the negative going edge of Enable should occur on or before the clock negative edge.

‡The data outputs are valid without the logic "1" pulse occurring during the access cycle as shown in a) above.

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM14524, the customer may specify the content of the memory.

Address Inputs:

Words are numbered 0 through 255 and are addressed using sequential addressing of Address leads A0 through A7 with A0 as the least significant digit.

Logic "0" is defined as a "low" Address input (V_{IL}).
Logic "1" is defined as a "high" Address input (V_{IH}).

WORD \ ADDRESS	A7	A6	A5	A4	A3	A2	A1	A0
Word 0	0	0	0	0	0	0	0	0
Word 1	0	0	0	0	0	0	0	1
Word 2	0	0	0	0	0	0	1	0
Word 3	0	0	0	0	0	0	1	1
. .	.	.	.	.	.	.	.	.
. .	.	.	.	.	.	.	.	.
. .	.	.	.	.	.	.	.	.
Word 255	1	1	1	1	1	1	1	1

TRUTH TABLE

CLOCK	ENABLE	B0	B1	B2	B3
V_{DD} ⎍ V_{SS}	1	*⟨Address⟩	*⟨Address⟩	*⟨Address⟩	*⟨Address⟩
V_{SS} ⎍ V_{DD}	1	OUTPUT DATA LATCHES			
X	0	0	0	0	0

X = Don't Care

*Indicates contents of specified Address will appear at outputs as stated above.

BINARY TO HEXADECIMAL CONVERSION TABLE

BINARY WORD DESIRED	CARD CHARACTER
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	A
1 0 1 1	B
1 1 0 0	C
1 1 0 1	D
1 1 1 0	E
1 1 1 1	F

Two methods may be used to transmit the custom memory pattern to Motorola.

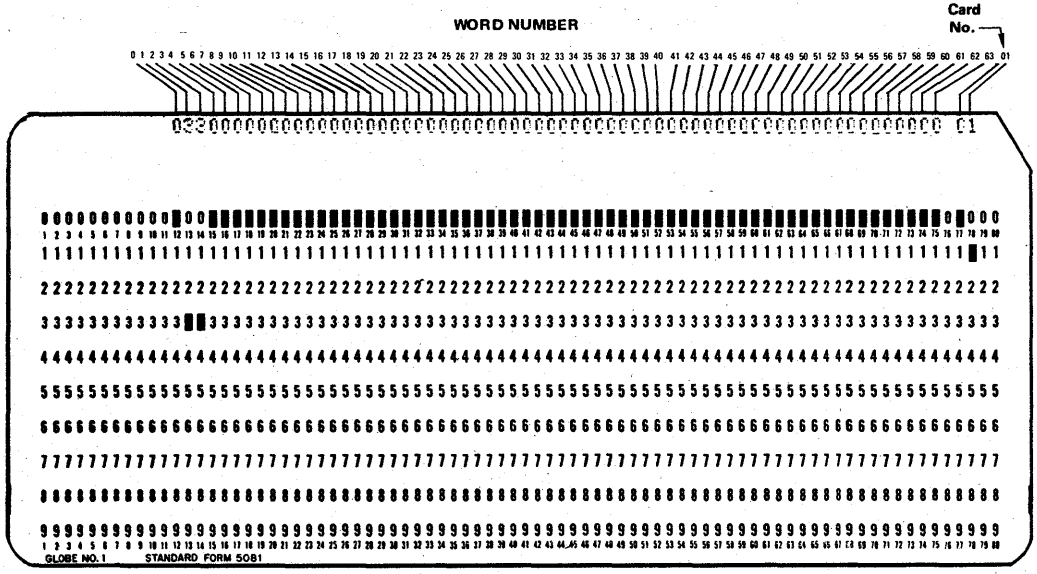
METHOD A: PUNCHED COMPUTER CARDS

A binary coded decimal equivalent of each desired output may be punched in standard computer cards (four cards are required for all 256 words) in numerical (word number) order. 64 words per card are punched in columns 12 thru 75 using the Binary to Hexadecimal conversion table. Columns 77 and 78 are used to number the cards, which must be in numerical order. Please use characters as shown in the table when punching computer cards.

ROM SAMPLE WORD PROGRAMMING FOR PUNCHED CARD

WORD NUMBER	ADDRESS INPUTS								SAMPLE WORD OUTPUTS				CARD CHARACTER
	A7	A6	A5	A4	A3	A2	A1	A0	B3	B2	B1	B0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	1	1	3
2	0	0	0	0	0	0	1	0	0	0	1	1	3
3	0	0	0	0	0	0	1	1	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
255	1	1	1	1	1	1	1	1	1	0	1	0	A

Shown in columns 12 – 15 on card below



METHOD B: TRUTH TABLE

For customers who do not have access to punch cards, Motorola will accept Truth Tables. When filling out the table, use the 0 to F hexidecimal character in column "C".

CUSTOM PROGRAM for the MCM14524 Read Only Memory

WORD	C
0	
1	
2	
3	
4	
5	
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7	
8	
9	
10	
11	
12	
13	
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15	
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36	
37	
38	
39	
40	
41	
42	
43	
44	
45	
46	
47	
48	
49	
50	

WORD	C
51	
52	
53	
54	
55	
56	
57	
58	
59	
60	
61	
62	
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64	
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WORD	C
102	
103	
104	
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WORD	C
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WORD	C
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MOTOROLA Semiconductors

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MC14526B

FOR COMPLETE DATA
SEE MC14522B

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

BCD – MC14522B
Binary – MC14526B

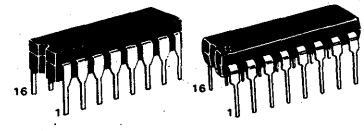
PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

The MC14522B BCD counter and the MC14526B binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure.

These devices are programmable, cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds.
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition of Clock Inhibit
- 5.0 MHz Counting Rate
- Asynchronous Preset Enable
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLES

BOTH TYPES

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
↓	0	0	0	Count-1
X	1	0	0	No Count
1	↓	0	0	Count-1
X	X	1	0	Preset
X	X	X	1	Reset

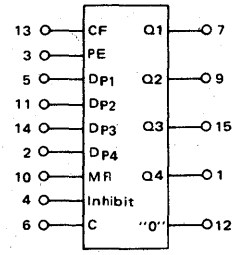
MC14522B

Count	Output Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC14526B

Count	Output Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

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MC14527B

BCD RATE MULTIPLIER

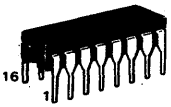
The MC14527B BCD rate multiplier (DRM) provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number, there will be six output pulses for every ten input pulses. This part may be used for arithmetic operations including multiplication and division. Typical applications include digital filters, motor speed control and frequency synthesizers.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance — 5.0 pF typical
- Internally Synchronous for High Speed
- Output Clocked on the Negative Going Edge of Clock
- Strobe for Inhibiting or Enabling Outputs
- Enable and Cascade Inputs for Cascade Operation of Two or More DRMs
- "9" Output for the Parallel Enable Configuration and DRMs in Cascade
- Complementary Outputs
- Clear and Set to Nine Inputs

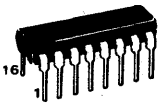
McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD RATE MULTIPLIER



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

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- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

5

MAXIMUM RATINGS (Voltages referenced to V_{SS})

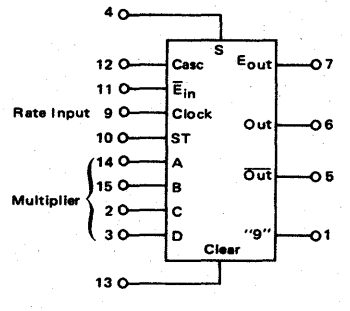
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS										OUTPUT LOGIC LEVEL NUMBER OF PULSES			
D	C	B	A	No. of Clock Pulses	$\overline{E}_{in}$	STROBE	CASCADE	CLEAR	SET	OUT	OUT	E_{out}	"9"
0	0	0	0	10	0	0	0	0	0	0	1	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	—	—	—	—
X	X	X	X	10	0	1	0	0	0	0	1	1	1
X	X	X	X	10	0	0	1	0	0	1	0	1	1
1	X	X	X	10	0	0	0	1	0	10	10	1	0
0	X	X	X	10	0	0	0	1	0	0	1	1	0
X	X	X	X	10	0	0	0	0	1	0	1	0	1

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.85\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (1.75\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (2.6\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1.2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L +30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time	t_{PHL}, t_{PHL}							ns
Clock to Out								
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 115 ns		5.0	–	–	200	300	500	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	–	100	150	250	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	–	70	120	175	
Clock to $\overline{Out}$	t_{PLH}, t_{PHL}							ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 40 ns		5.0	–	–	125	190	315	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 32 ns		10	–	–	65	100	150	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 20 ns		15	–	–	45	70	115	
Clock to E_{out}	t_{PLH}, t_{PHL}							ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 210 ns		5.0	–	–	295	500	900	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	–	130	200	325	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 60 ns		15	–	–	85	150	230	
Clock to "9"	t_{PLH}, t_{PHL}							ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	–	400	600	1000	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 122 ns		10	–	–	155	250	400	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	–	110	200	300	
Set or Clear to Out	t_{PHL}							ns
t_{PHL} = (1.7 ns/pF) C_L + 295 ns		5.0	–	–	380	700	1000	
t_{PHL} = (0.66 ns/pF) C_L + 132 ns		10	–	–	165	300	400	
t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	–	110	230	300	
Cascade to Out	t_{PLH}							ns
t_{PHL} = (1.7 ns/pF) C_L + 40 ns		5.0	–	–	125	190	315	
t_{PHL} = (0.66 ns/pF) C_L + 32 ns		10	–	–	65	100	150	
t_{PHL} = (0.5 ns/pF) C_L + 20 ns		15	–	–	45	70	115	
Strobe to Out	t_{PLH}							ns
t_{PHL} = (1.7 ns/pF) C_L + 145 ns		5.0	–	–	230	350	700	
t_{PHL} = (0.66 ns/pF) C_L + 72 ns		10	–	–	105	160	265	
t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	–	70	120	190	
Minimum Clock Pulse Width	PW_C	5.0	–	–	250	340	500	ns
		10	–	–	110	170	200	
		15	–	–	80	130	150	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	2.0	–	–	MHz
		10	3.0	2.5	4.5	–	–	
		15	4.0	3.3	6.0	–	–	
Maximum Clock Pulse Rise and Fall Time	t_r,t_f	5.0	15	15	–	–	–	µs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
Minimum Set or Clear Pulse Width	PW_S	5.0	–	–	80	180	240	ns
	PW_{clear}	10	–	–	35	70	100	
		15	–	–	30	55	75	
Set Removal Time	t_{rem}	5.0	–	–	-20	0	0	ns
		10	–	–	-10	0	0	
		15	–	–	-7.5	0	0	
Enable In Setup Time	t_{setup}	5.0	–	–	175	350	400	ns
		10	–	–	60	120	150	
		15	–	–	45	90	120	

*The formula given is for the typical characteristics only.

FIGURE 1 – TEST CIRCUIT AND TIMING DIAGRAM

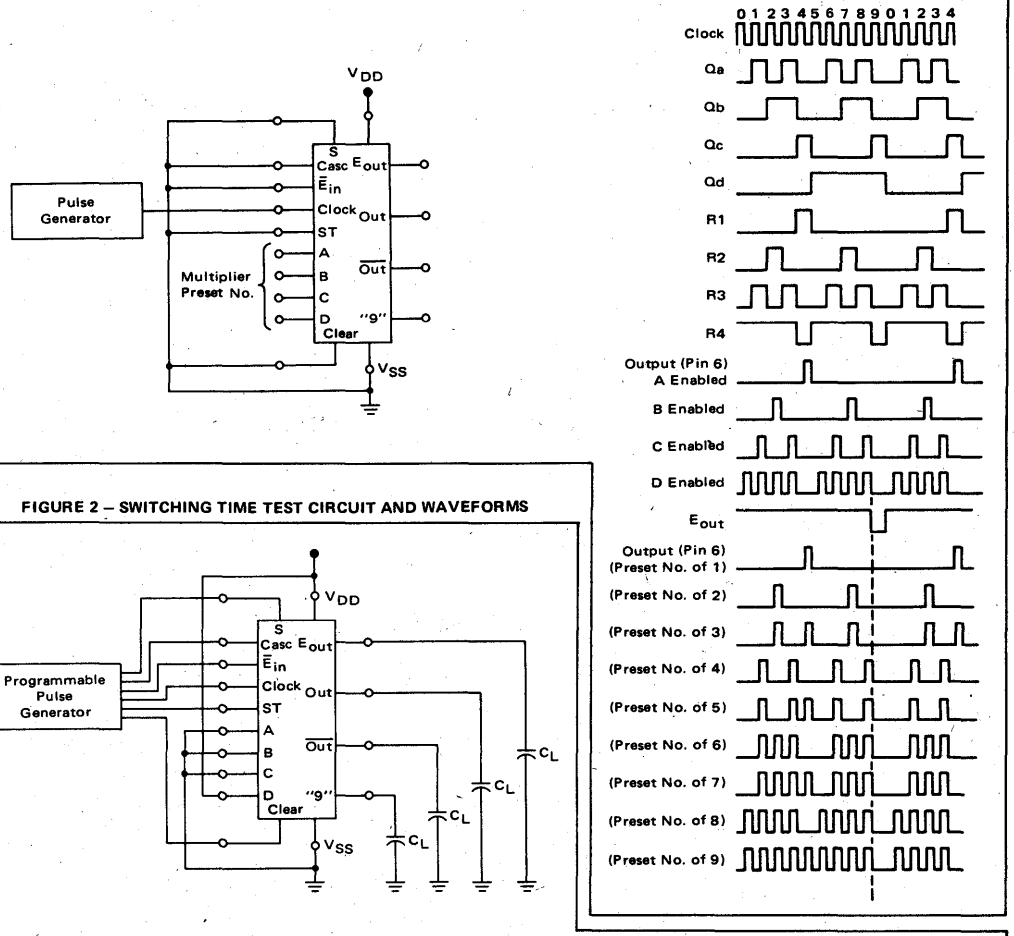


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

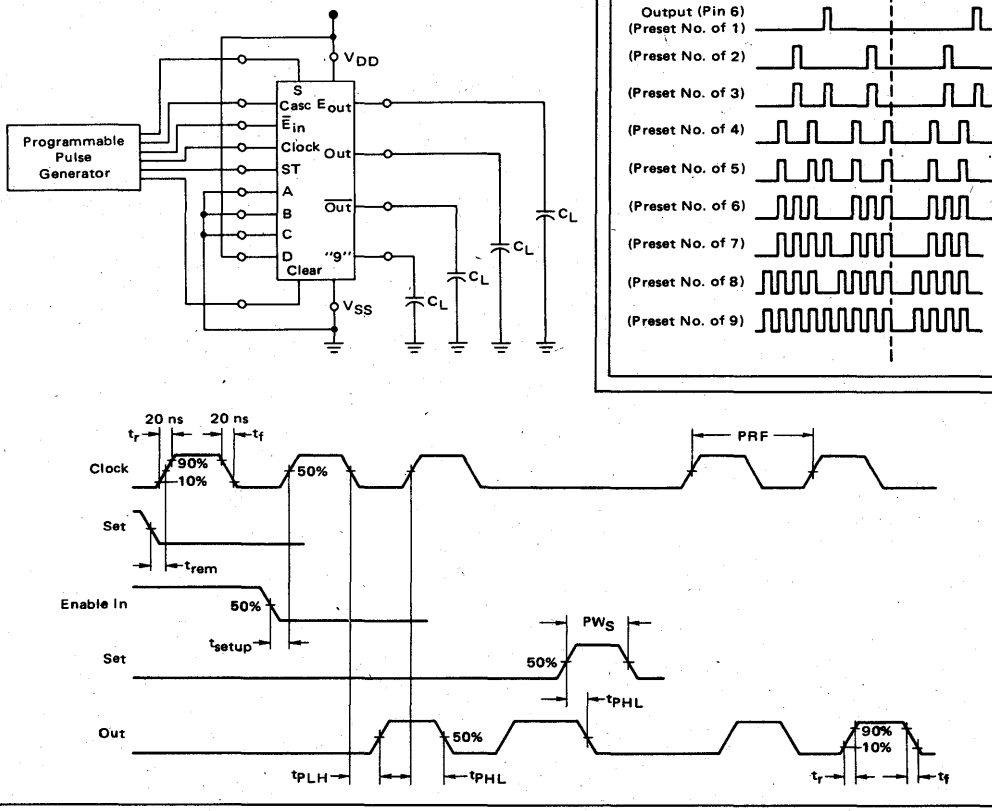


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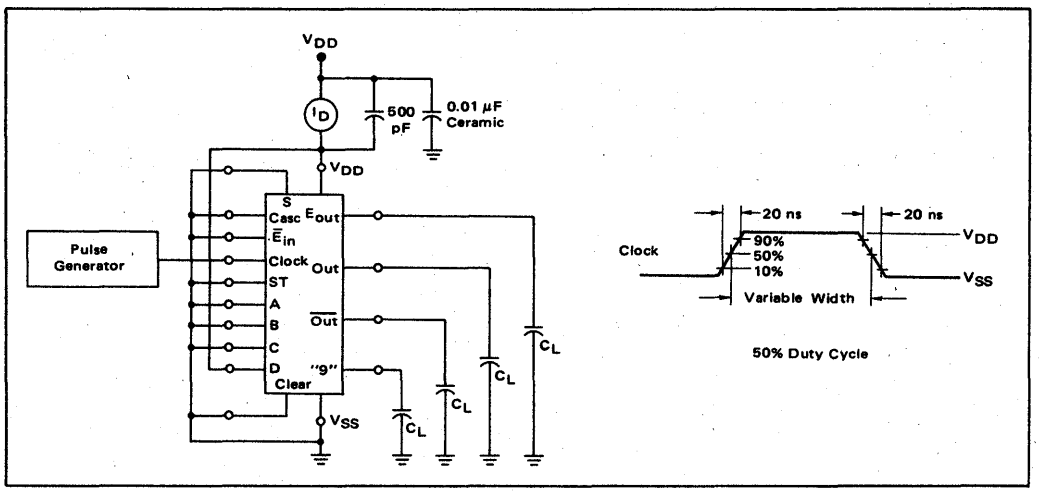
FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



LOGIC DIAGRAM

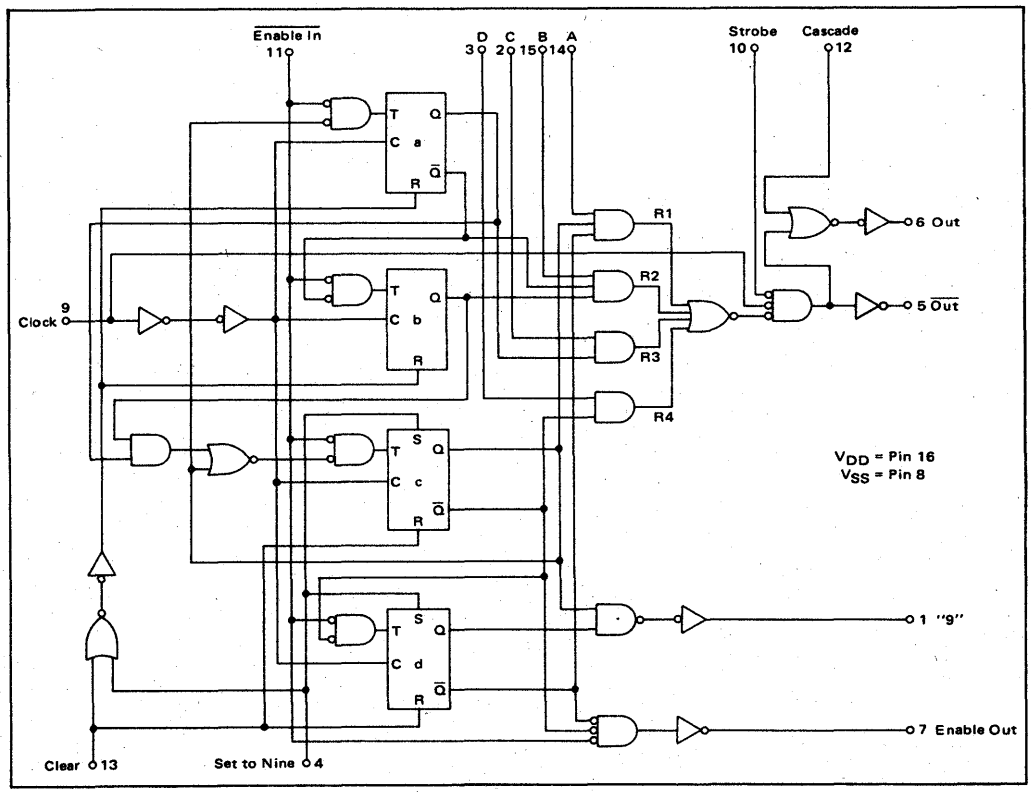
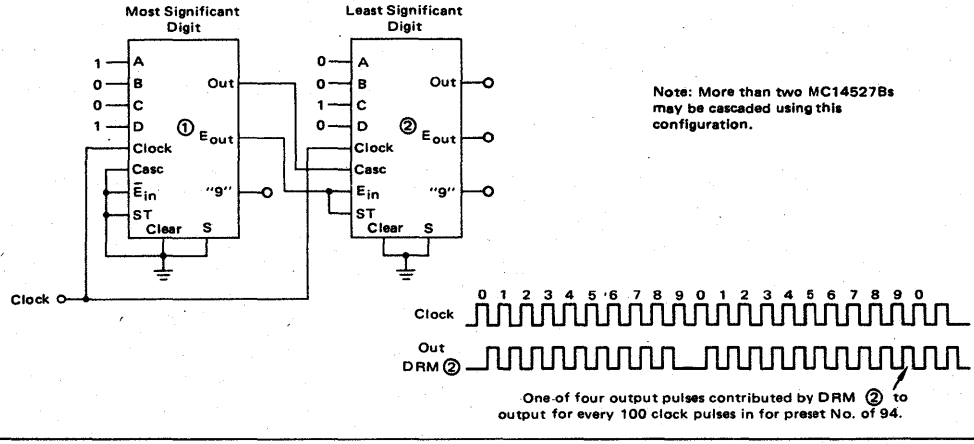


FIGURE 4 – TWO MC14527Bs IN CASCADE WITH PRESET NO. of 94



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MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14528B

McMOS MSI

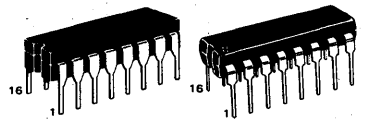
(LOW-POWER COMPLEMENTARY MOS)

DUAL RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

DUAL MONOSTABLE MULTIVIBRATOR

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

- Separate Reset Available
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

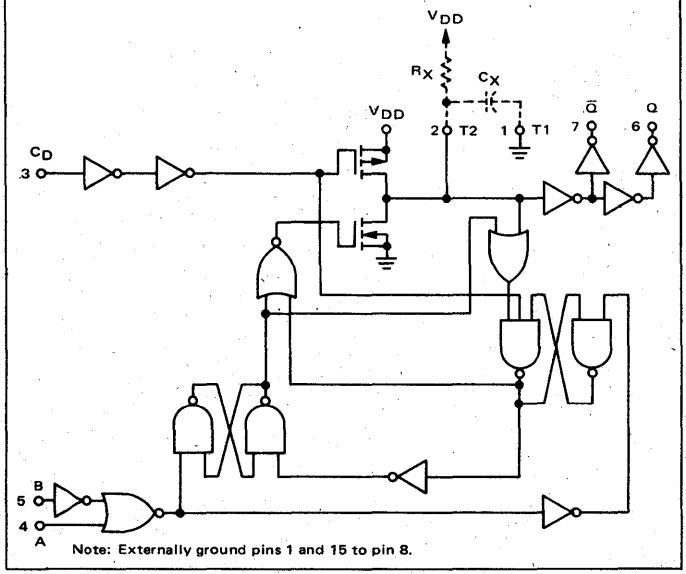
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

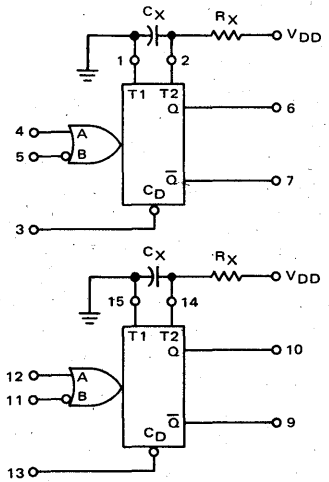
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM
(1/2 of Device Shown)



Note: Externally ground pins 1 and 15 to pin 8.

BLOCK DIAGRAM



R_X and C_X are external components.
V_{DD} = Pin 16
V_{SS} = Pin 8

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
**Total Supply Current at an external load Capacitance (C_L) and at external timing capacitance (C_X), use the formula –	I_T	–	$I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2\times10^{-8} R_X C_X (V_{DD}-2)^2 f] \times 10^{-3}$ where: I_T in µA (per circuit), C_L and C_X in pF, R_X in megohms, V_{DD} in Vdc, f in kHz is input frequency.							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS** (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	C_X pF	R_X kΩ	V_{DD} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r	–	–					ns
t_r = (3.0 ns/pF) C_L + 30 ns				5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns				10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns				15	65	110	160	
Output Fall Time	t_f	–	–					ns
t_f = (1.5 ns/pF) C_L + 25 ns				5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns				10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns				15	37	55	80	
Turn-Off, Turn-On Delay Time – A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L +240 ns				5.0	325	490	700	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns				10	120	180	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns				15	90	135	225	
Turn-Off, Turn-On Delay Time – A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	1000	10					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 620 ns				5.0	705	–	–	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L +257 ns				10	290	–	–	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 185 ns				15	210	–	–	
Minimum Input Pulse Width – A or B	PW_{in}	15	5.0	5.0	70	150	240	ns
				10	30	75	120	
				15	30	55	90	
		1000	10	5.0	70	–	–	ns
				10	30	–	–	
				15	30	–	–	
Output Pulse Width – Q or $\overline{Q}$	PW_{out}	15	5.0	5.0	550	–	–	ns
(For C_X < 0.01 μF use graph for appropriate V_{DD} level.)				10	350	–	–	
				15	300	–	–	
Output Pulse Width – Q or $\overline{Q}$	PW_{out}	10,000	10	5.0	30	±10	±15	μs
(For C_X > 0.01 μF use formula:				10	50	±25	±40	
PW_{out} = 0.2 R_X C_X Ln [V_{DD}–V_{SS}])†				15	55	±25	±40	
Pulse Width Match between Circuits in the same package	t1-t2	10,000	10	5.0	6.0	15	25	%
				10	8.0	20	35	
				15	8.0	20	35	
Reset Propagation Delay – C_D to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0	5.0	325	490	600	ns
				10	90	150	225	
				15	60	110	170	
		1000	10	5.0	1000	–	–	ns
				10	300	–	–	
				15	250	–	–	
Minimum Retrigger Time	t_{rr}	15	5.0	5.0	0	–	–	ns
				10	0	–	–	
				15	0	–	–	
		1000	10	5.0	0	–	–	ns
				10	0	–	–	
				15	0	–	–	
					Min			
External Timing	R_X	–	–	–	5.0	1000	1000	kΩ
External Timing Capacitance	C_X	–	–	–	No Limits			μF

**The formula given is for the typical characteristics only.

†R_X is in Ohms, C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.

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FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT

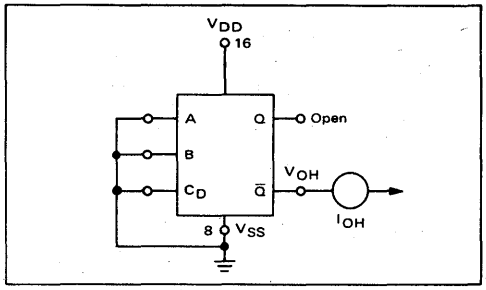


FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT

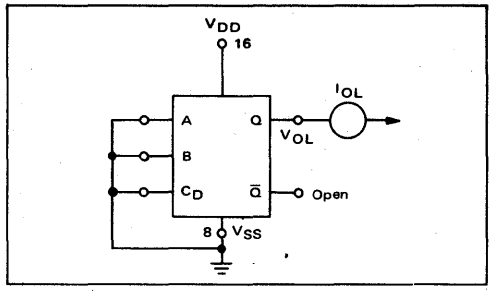


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

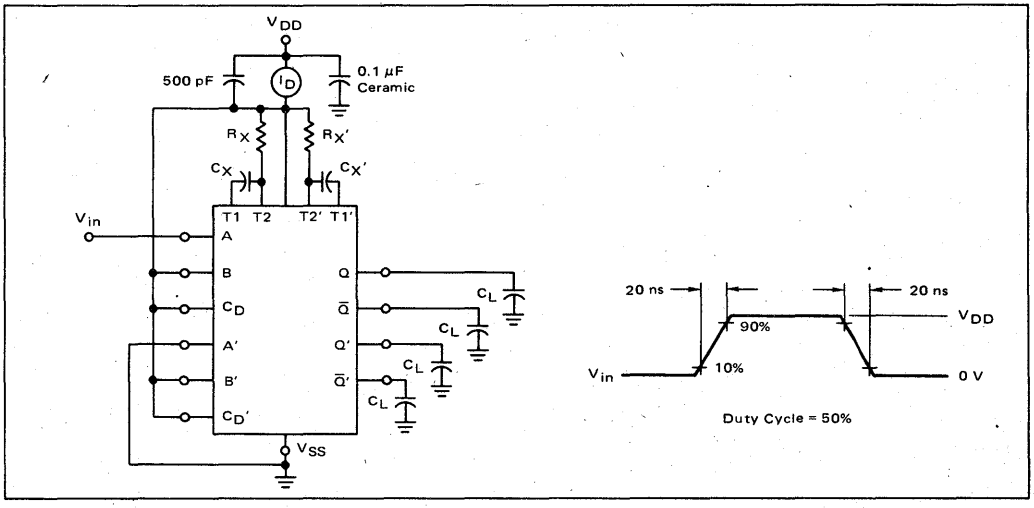
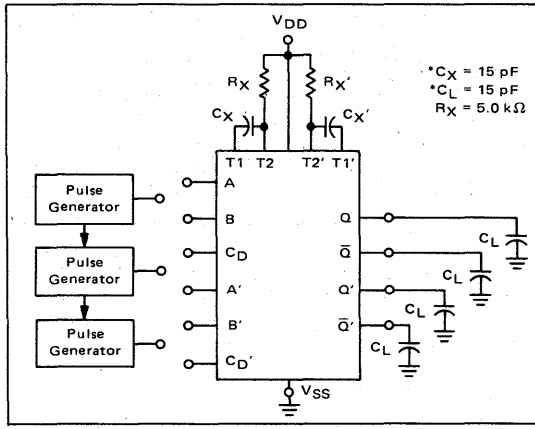


FIGURE 4 – AC TEST CIRCUIT



*CX = 15 pF
*CL = 15 pF
RX = 5.0 kΩ

INPUT CONNECTIONS

CHARACTERISTICS	CD	A	B
$t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}$	V_{DD}	PG1	V_{DD}
$t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}$	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}, t_{PHL(R)}, PW_{in}$	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE; AC test waveforms for PG1, PG2, and PG3 on next page.

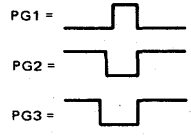


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FIGURE 5 – AC TEST WAVEFORMS

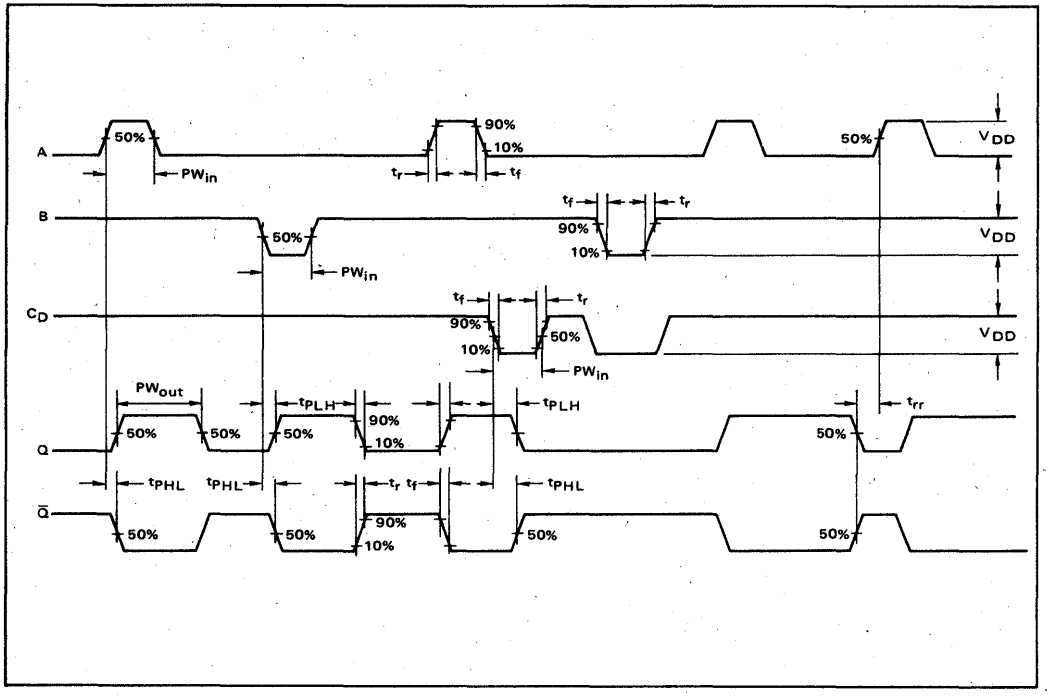

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FIGURE 6 – NORMALIZED PULSE WIDTH versus TEMPERATURE

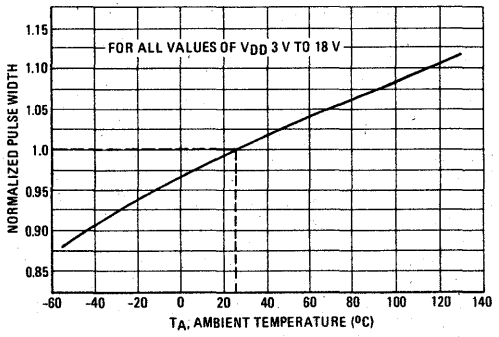
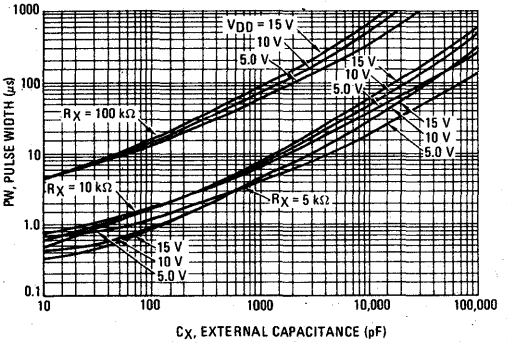


FIGURE 7 – PULSE WIDTH versus C_X



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14529B

DUAL 4-CHANNEL ANALOG DATA SELECTOR

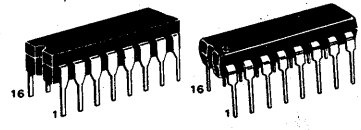
The MC14529 analog data selector is a dual 4-channel or single 8-channel device depending on the input coding. The device is suitable for digital as well as analog application, including various one-of-four and one-of-eight data selector functions. Since the device has bidirectional analog characteristics it can also be used as a dual binary to 1-of-4 or a binary to 1-of-8 decoder.

- Data Paths Are Bidirectional
- Quiescent Current = 1.0 nA/package typical @ 5.0 Vdc
- 10-MHz Operation (typical)
- 3-State Outputs
- Linear "On" Resistance
- "On" Resistance 120 Ohms typical @ 15 V
- Low Noise – 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-CHANNEL ANALOG DATA SELECTOR
OR
8-CHANNEL ANALOG DATA SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

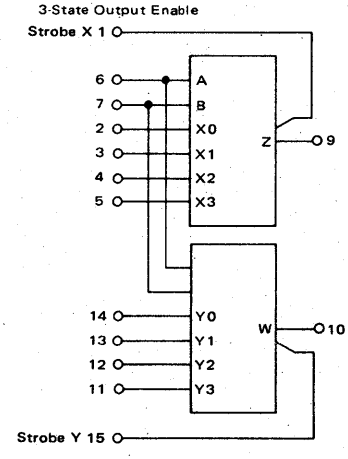
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

ST_X	ST_Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	ϕ	ϕ	High Impedance		

ϕ = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the control inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} or V_{out} is not constrained to the range $V_{SS} \leq V_{in}$ or $V_{out} \leq V_{DD}$.

5

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{SS} Vdc	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	1	V_{OL}	0.0	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0				10	–	0.05	–	[illegible]	0.05	–	0.05	
				15	–	0.05	–	0	0.05	–	0.05	
"1" Level		V_{OH}	0.0	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
				10	9.95	–	9.95	10	–	9.95	–	
V_{in} = 0 or V_{DD}				15	14.95	–	14.95	15	–	14.95	–	
Noise Immunity	2	V_{NL}	0.0									Vdc
($I_{out} \leq 10$ μAdc)				5.0	1.5	–	1.5	2.25	–	1.4	–	
				10	3.0	–	3.0	4.50	–	2.9	–	
				15	4.5	–	4.5	6.75	–	4.4	–	
($I_{out} \geq 10$ μAdc)		V_{NH}	0.0	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
				10	2.9	–	3.0	4.50	–	3.0	–	
				15	4.4	–	4.5	6.75	–	4.5	–	
Input Current (AL Device) Control		I_{in}	0.0	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device) Control		I_{in}	0.0	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	0.0									pF
Control				–	–	–	–	5.0	7.5	–	–	
Switch Input				–	–	–	–	8.0	–	–	–	
Switch Output				–	–	–	–	20	–	–	–	
Feed Through				–	–	–	–	0.3	–	–	–	
Quiescent Current (AL Device) (Per Package)	3	I_{DD}	–	5.0	–	1.0	–	0.001	1.0	–	60	μAdc
				10	–	1.0	–	0.002	1.0	–	60	
				15	–	2.0	–	0.003	2.0	–	120	
Quiescent Current (CL/CP Device) (Per Package)	3	I_{DD}	–	5.0	–	5.0	–	0.001	5.0	–	70	μAdc
				10	–	5.0	–	0.002	5.0	–	70	
				15	–	10	–	0.003	10	–	140	
"ON" Resistance (AL Device)	4,5, 6	R_{ON}										Ohms
(V_C = V_{DD}, R_L = 10 kΩ)												
(V_{in} = +5.0 Vdc)			-5.0	5.0	–	400	–	200	480	–	640	
(V_{in} = -5.0 Vdc)					–	400	–	200	480	–	640	
(V_{in} = ±0.25 Vdc)					–	400	–	190	480	–	640	
(V_{in} = +7.5 Vdc)			-7.5	7.5	–	240	–	160	270	–	400	
(V_{in} = -7.5 Vdc)					–	240	–	160	270	–	400	
(V_{in} = ±0.25 Vdc)					–	240	–	120	270	–	400	
(V_{in} = +10 Vdc)			0	10	–	400	–	180	480	–	640	
(V_{in} = +0.25 Vdc)					–	400	–	180	480	–	640	
(V_{in} = +5.6 Vdc)					–	400	–	220	480	–	640	
(V_{in} = +15 Vdc)			0	15	–	250	–	180	270	–	400	
(V_{in} = +0.25 Vdc)					–	250	–	180	270	–	400	
(V_{in} = +9.3 Vdc)					–	250	–	215	270	–	400	
"ON" Resistance (CL/CP Device)	4,5, 6	R_{ON}										Ohms
(V_C = V_{DD}, R_L = 10 kΩ)												
(V_{in} = +5.0 Vdc)			-5.0	5.0	–	410	–	200	480	–	560	
(V_{in} = -5.0 Vdc)					–	410	–	200	480	–	560	
(V_{in} = ±0.25 Vdc)					–	410	–	190	480	–	560	
(V_{in} = +7.5 Vdc)			-7.5	7.5	–	250	–	160	270	–	350	
(V_{in} = -7.5 Vdc)					–	250	–	160	270	–	350	
(V_{in} = ±0.25 Vdc)					–	250	–	120	270	–	350	
(V_{in} = +10 Vdc)			0	10	–	410	–	180	480	–	560	
(V_{in} = +0.25 Vdc)					–	410	–	180	480	–	560	
(V_{in} = +5.6 Vdc)					–	410	–	220	480	–	560	
(V_{in} = +15 Vdc)			0	15	–	250	–	180	270	–	350	
(V_{in} = +0.25 Vdc)					–	250	–	180	270	–	350	
(V_{in} = +9.3 Vdc)					–	250	–	215	270	–	350	
△"ON" Resistance Between any 2 circuits in a common package	–	$\triangle R_{ON}$										Ohms
(V_{in} = ±5.0 Vdc)			-5.0	5.0	–	–	–	15	–	–	–	
(V_{in} = ±7.5 Vdc)			-7.5	7.5	–	–	–	10	–	–	–	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device. T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

SWITCHING CHARACTERISTICS (T_A = 25°C)

Characteristic	Figure	Symbol	V_{SS}	V_{DD}	Typical All Types	Maximum AL Device	Maximum CL/CP Device	Unit
V_{in} to V_{out} Propagation Delay Time (C_L = 50 pF, R_L = 1.0 kΩ)	7	t_{PLH},t_{PHL}	0.0	5.0	20	40	60	ns
				10	10	20	30	
				15	8.0	15	25	
Propagation Delay Time, Control to Output, V_{in} = V_{DD} or V_{SS} (V_{in} ≤ 10 Vdc, C_L = 50 pF, R_L = 1.0 kΩ)	8	t_{PHL},t_{PLH}	0.0	5.0	200	400	600	ns
				10	80	160	240	
				15	50	120	180	
Crosstalk, Control to Output (C_L = 50 pF, R_L = 1.0 kΩ) R_{out} = 10 kΩ)	9	–	0.0	5.0	5.0	–	–	mV
				10	5.0	–	–	
				15	5.0	–	–	
Maximum Control Input Pulse Frequency (C_L = 50 pF, R_L = 1.0 kΩ)	10	–	0.0	5.0	5.0	–	–	MHz
				10	10	–	–	
				15	12	–	–	
Noise Voltage (f = 100 Hz)	11,12	–	0.0	5.0	24	–	–	nV/√Cycle
				10	25	–	–	
				15	30	–	–	
(f = 100 kHz)				5.0	12	–	–	
				10	12	–	–	
				15	15	–	–	
Sine Wave (Distortion) (V_{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	–	–	-5.0	5.0	0.36	–	–	%
Input/Output Leakage Current	–	–						nA
(V_{in} = +5.0 Vdc, V_{out} = -5.0 Vdc)			-5.0	5.0	±0.001	±125	±125	
(V_{in} = -5.0 Vdc, V_{out} = +5.0 Vdc)			-5.0	5.0	±0.001	±125	±125	
(V_{in} = +7.5 Vdc, V_{out} = -7.5 Vdc)			-7.5	7.5	±0.0015	±250	±250	
(V_{in} = -7.5 Vdc, V_{out} = +7.5 Vdc)			-7.5	7.5	±0.0015	±250	±250	
Insertion Loss (V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc, f = 1.0 MHz, $I_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$	–	–	-5.0	5.0				dB
(R_L = 1.0 kΩ)					2.0	–	–	
(R_L = 10 kΩ)					0.8	–	–	
(R_L = 100 kΩ)					0.25	–	–	
(R_L = 1.0 MΩ)					0.01	–	–	
Bandwidth (-3 dB) (V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc)	–	BW	-5.0	5.0				MHz
(R_L = 1.0 kΩ)					35	–	–	
(R_L = 10 kΩ)					28	–	–	
(R_L = 100 kΩ)					27	–	–	
(R_L = 1.0 MΩ)					26	–	–	
Feedthrough and Crosstalk ($20 \log_{10} \frac{V_{out}}{V_{in}}$ = -50 dB)	–	–	-5.0	5.0				kHz
(R_L = 1.0 kΩ)					850	–	–	
(R_L = 10 kΩ)					100	–	–	
(R_L = 100 kΩ)					12	–	–	
(R_L = 1.0 MΩ)					1.5	–	–	

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FIGURE 1 - OUTPUT VOLTAGE TEST CIRCUIT

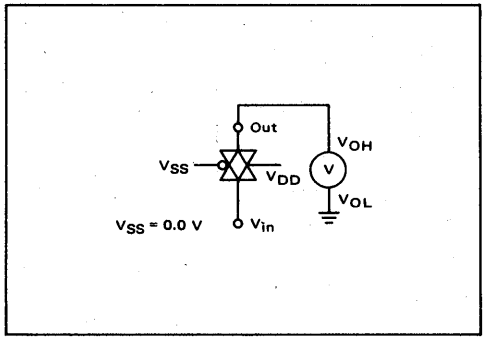


FIGURE 2 – NOISE IMMUNITY TEST CIRCUIT

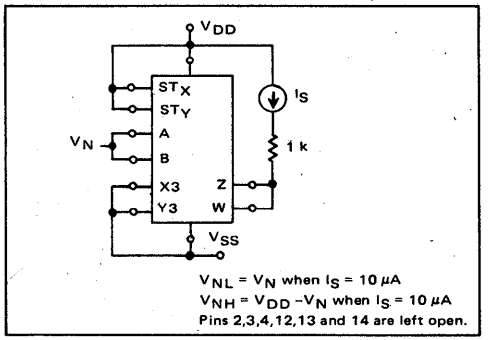


FIGURE 3 – QUIESCENT POWER DISSIPATION TEST CIRCUIT

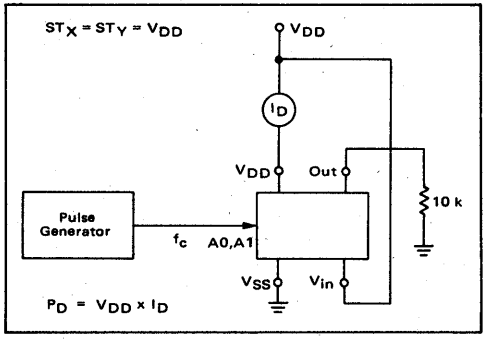
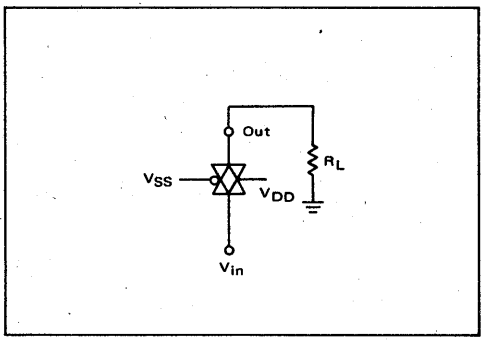


FIGURE 4 – R_{ON} CHARACTERISTICS TEST CIRCUIT



TYPICAL R_{ON} versus INPUT VOLTAGE

FIGURE 5

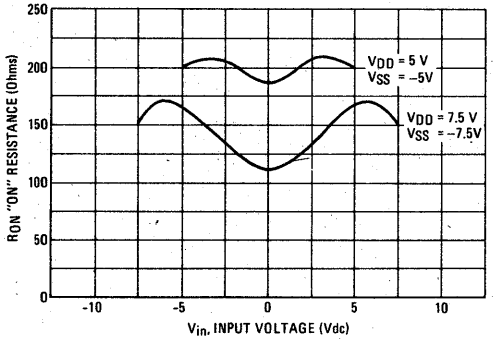


FIGURE 6

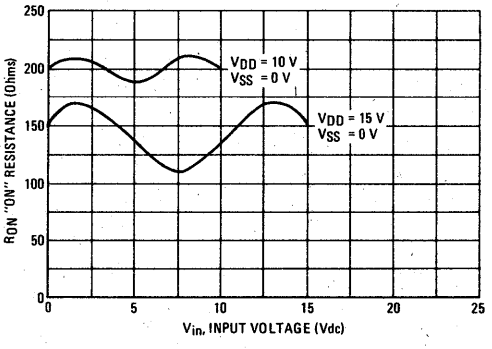


FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

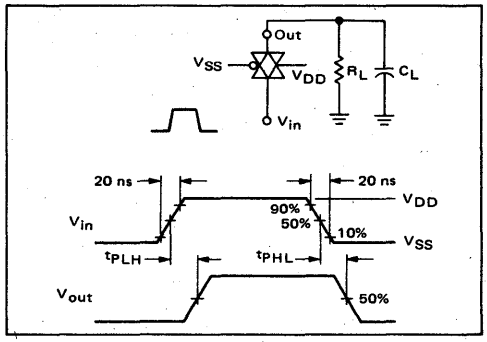


FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

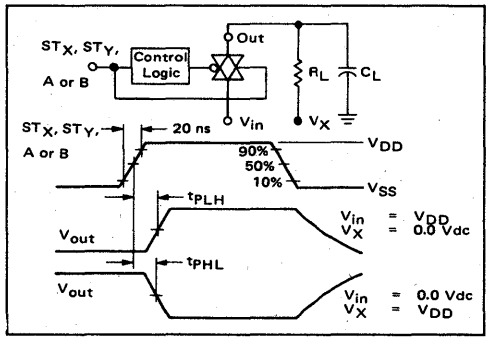


FIGURE 9 – CROSSTALK TEST CIRCUIT

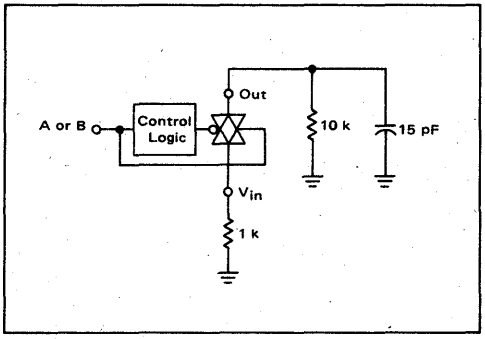


FIGURE 10 – FREQUENCY RESPONSE TEST CIRCUIT

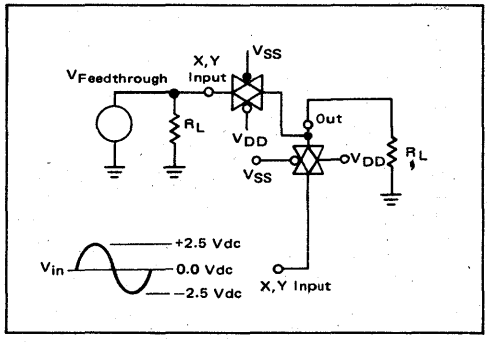


FIGURE 11 – NOISE VOLTAGE TEST CIRCUIT

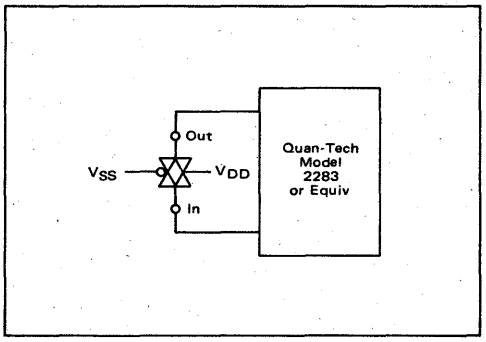


FIGURE 12 – TYPICAL NOISE CHARACTERISTICS

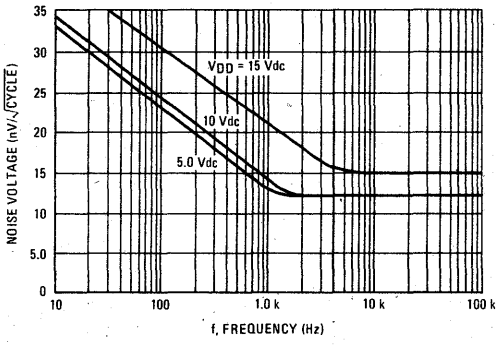


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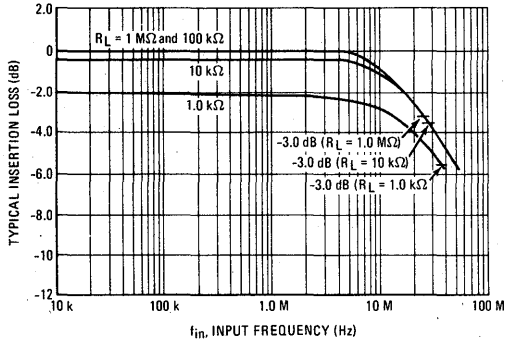
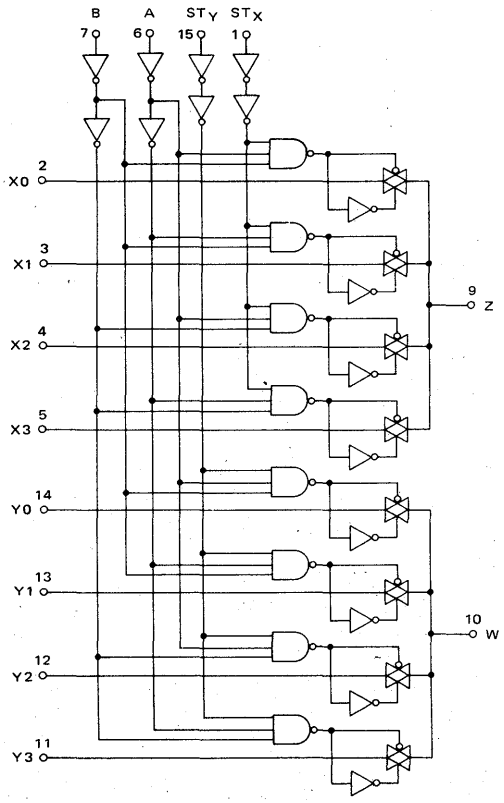
FIGURE 13 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14530B

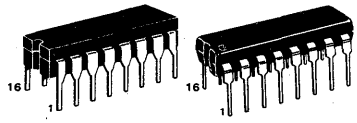
McMOS SSI
(LOW-POWER COMPLEMENTARY MOS)

DUAL 5-INPUT MAJORITY LOGIC GATE

DUAL 5-INPUT MAJORITY LOGIC GATE

The MC14530B dual five-input majority logic gate is constructed with P-channel and N-channel enhancement mode devices in a single monolithic structure. Combinational and sequential logic expressions are easily implemented with the majority logic gate, often resulting in fewer components than obtainable with the more basic gates. This device can also provide numerous logic functions by using the W and some of the logic (A thru E) inputs as control inputs.

- Single Supply Operation – Positive or Negative
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Input Impedance = 10^{12} ohms typical
- High Fanout > 50
- Diode Protection on Inputs
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

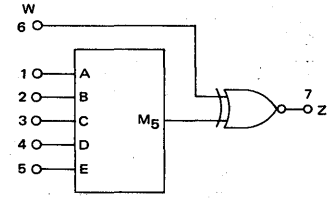
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

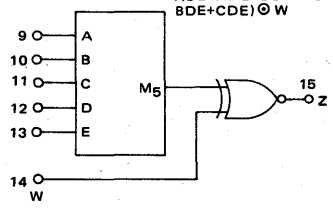
LOGIC TABLE

INPUTS A B C D E	W	Z
For all combinations of inputs where three or more inputs are logical "0".	0	1
	1	0
For all combinations of inputs where three or more inputs are logical "1".	0	0
	1	1

BLOCK DIAGRAM



* $Z = M_5 \odot W = (ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE) \odot W$



*M_5 is a logical "1" if any three or more inputs are logical "1".

$\odot$ ≡ Exclusive NOR ≡ $\overline{\text{Exclusive OR}}$

TRUTH TABLE

M_5	W	Z
0	0	1
0	1	0
1	0	0
1	1	1

V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must be tied to an appropriate logic level (e.g., V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.5 or 1.5 Vdc)		5.0	–	1.2	–	2.25	1.25	–	1.15	
(V_O = 7.0 or 3.0 Vdc)		10	–	2.5	–	4.50	2.5	–	2.4	
(V_O = 10.5 or 4.5 Vdc)		15	–	3.0	–	6.75	3.0	–	2.9	
"1" Level	V_{IH}									
(V_O = 1.5 or 3.5 Vdc)		5.0	3.85	–	3.75	2.75	–	3.75	–	Vdc
(V_O = 3.0 or 7.0 Vdc)		10	7.6	–	7.5	5.50	–	7.5	–	
(V_O = 4.5 or 10.5 Vdc)		15	12.1	–	12	8.25	–	12	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.50 µA/kHz) f + I_{DD}							
		15	I_T = (2.25 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination. Standard family noise margin specification is met for any one input tested at a time.
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

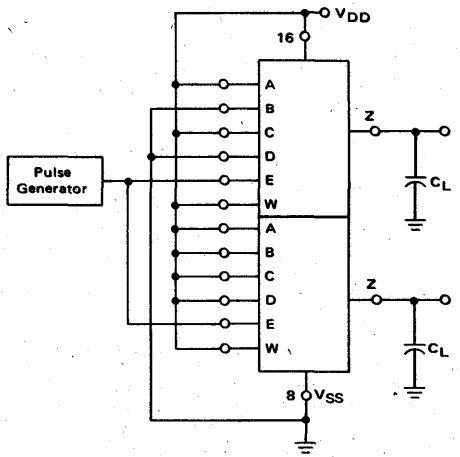
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

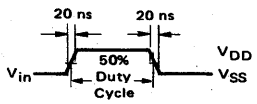
Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L +25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L +12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Propagation Delay Time	t_{PLH}					ns
A, C, W = V_{DD}; B, E = Gnd; D = Pulse Generator						
t_{PLH} = (1.7 ns/pF) C_L + 290 ns		5.0	375	640	960	
t_{PLH} = (0.66 ns/pF) C_L + 127 ns		10	160	260	400	
t_{PLH} = (0.5 ns/pF) C_L + 85 ns		15	110	200	300	
t_{PHL} = (1.7 ns/pF) C_L + 345 ns	t_{PHL}	5.0	430	800	1200	ns
t_{PHL} = (0.66 ns/pF) C_L + 162 ns		10	195	360	540	
t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	120	270	410	
A, B, C, D, E = Pulse Generator; W = V_{DD}	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 170 ns		5.0	255	400	640	
t_{PLH} = (0.66 ns/pF) C_L + 87 ns		10	120	180	300	
t_{PLH} = (0.5 ns/pF) C_L + 60 ns		15	85	140	210	
t_{PHL} = (1.7 ns/pF) C_L + 195 ns	t_{PHL}	5.0	280	500	750	ns
t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	125	220	330	
t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	100	170	250	
A, B, C, D, E = Gnd; W = Pulse Generator	t_{PLH}, t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 145 ns		5.0	230	350	575	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 72 ns		10	105	150	265	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 50 ns		15	75	120	190	

*The formula given is for the typical characteristics only.

5

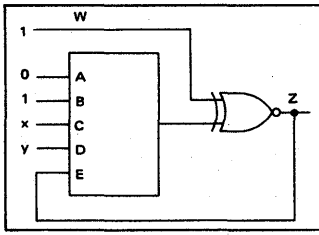
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM





SEQUENTIAL LOGIC APPLICATIONS

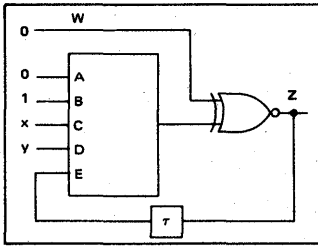
COINCIDENT FLIP-FLOP



x	y	Q_{n+1}
0	0	0
0	1	Q
1	0	Q
1	1	1

A flip-flop that will change only when both inputs agree.

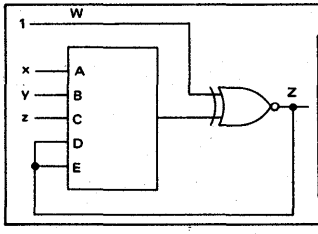
ASTABLE MULTIVIBRATOR



x	y	Q_{n+1}
0	0	1
0	1	2τ
1	0	2τ
1	1	0

A flip-flop with three output conditions, where the third state is in oscillation between "1" and "0". The period of oscillation is twice the delay of the gate and the feedback element.

COINCIDENT FLIP-FLOP

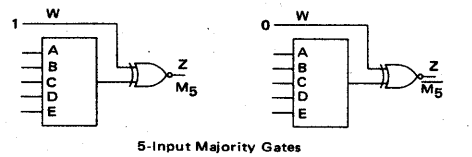


x	y	z	Q_{n+1}
0	0	0	0
0	0	1	Q_n
0	1	0	Q_n
0	1	1	Q_n
1	0	0	Q_n
1	0	1	Q_n
1	1	0	Q_n
1	1	1	1

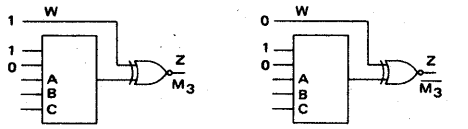
The flip-flop changes state only when all "1's" or all "0's" are entered. This configuration may be extended by cascading M_5 gates to cover n-inputs where all inputs must be "1's" or "0's" before the output will change. As an example, this configuration is useful for controlling an n-stage up/down counter that is to cycle from a minimum to maximum count and back again without flipping over (from all "1's" to all "0's".)

5

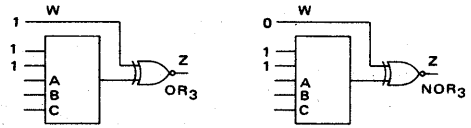
BASIC COMBINATIONAL FUNCTIONS



5-Input Majority Gates

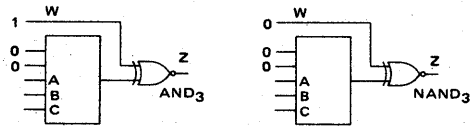


3-Input Majority Gates



3-Input OR Gate

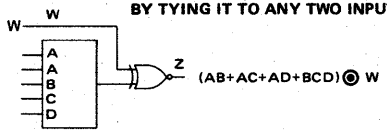
3-Input NOR Gate



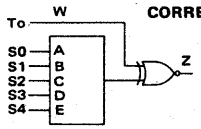
3-Input AND Gate

3-Input NAND Gate

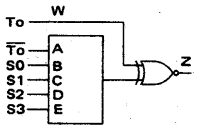
DOUBLING THE WEIGHT OF INPUT VARIABLE A BY TYING IT TO ANY TWO INPUTS

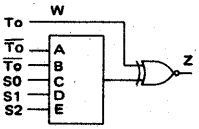


CORRELATION OF MULTIPLE SAMPLES WITH A TEST BIT



The gate will have a "1" output if the test bit To matches or correlates with 3, 4 or 5 of the sample bits S0-S4.



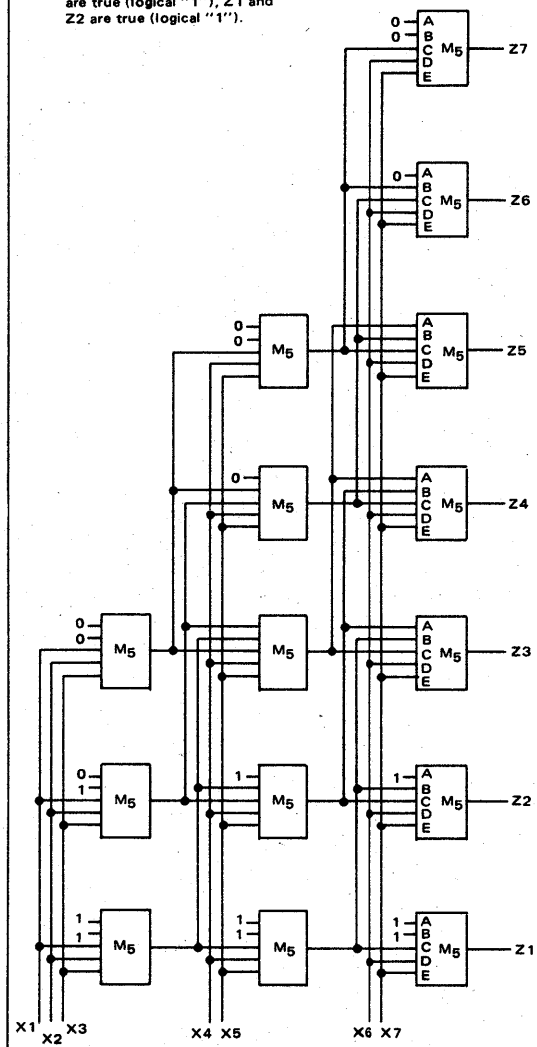


5-INPUT MAJORITY LOGIC GATE APPLICATIONS

Each package labeled M_5 is a single majority logic gate using five inputs, A thru E, and one output Z.

1. Majority Logic Gate Array yielding the symetric function of 1 thru 7 variables true, out of 7 input variables (X1 . . . X7)

(e.g., if any two-input variables are true (logical "1"), Z1 and Z2 are true (logical "1").



5

MOTOROLA Semiconductors

BOX 20912 • PHOENIX, ARIZONA 85036

MC14531B

12-BIT PARITY TREE

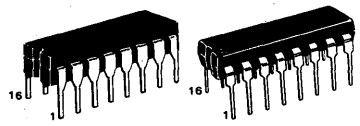
The MC14531B 12-bit parity tree is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of 12 data-bit inputs (D0 thru D11), and even or odd parity selection input (W) and an output (Q). The parity selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even or odd number of ones, respectively. Words of greater than 12-bits can be accommodated by cascading other MC14531B devices by using the W input. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple input summer without carries.

- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Quiescent Current – 5.0 nA/package typical @ 5 Vdc
- Variable Word Length
- Diode Protection on All Inputs

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

12-BIT PARITY TREE



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

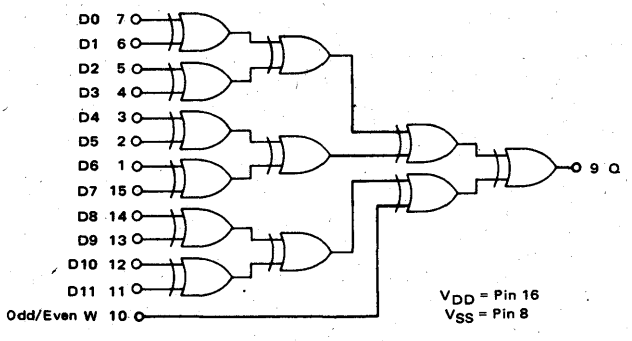
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

5

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



Q = D0 ⊕ D1 ⊕ D2 ⊕ . . . . ⊕ D11 ⊕ W

TRUTH TABLE

INPUTS								OUTPUT
W	D11	D10	· · ·	D2	D1	D0	DECIMAL (OCTAL) EQUIVALENT	Q*
0	0	0	· · ·	0	0	0	0 (0)	0
0	0	0	· · ·	0	0	1	1 (1)	1
0	0	0	· · ·	0	1	0	2 (2)	1
0	0	0	· · ·	0	1	1	3 (3)	0
0	0	0	· · ·	1	0	0	4 (4)	1
0	0	0	· · ·	1	0	1	5 (5)	0
0	0	0	· · ·	1	1	0	6 (6)	0
0	0	0	· · ·	1	1	1	7 (7)	1
:	:	:	:	:	:	:	:	:
1	1	1	· · ·	0	0	0	8184 (17770)	0
1	1	1	· · ·	0	0	1	8185 (17771)	1
1	1	1	· · ·	0	1	0	8186 (17772)	1
1	1	1	· · ·	0	1	1	8187 (17773)	0
1	1	1	· · ·	1	0	0	8188 (17774)	1
1	1	1	· · ·	1	0	1	8189 (17775)	0
1	1	1	· · ·	1	1	0	8190 (17776)	0
1	1	1	· · ·	1	1	1	8191 (17777)	1

*0 = Even Parity
1 = Odd Parity

Note: May redefine to suit application by manipulating W and/or other available D's.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.25 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.50 µA/kHz) f + I_{DD}							
		15	I_T = (0.75 µA/kHz) f + I_{DD}							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

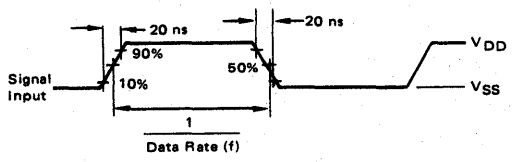
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Data to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 355 ns		5.0	440	880	1320	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 142 ns		10	175	350	525	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	120	240	360	
Odd/Even to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 165 ns		5.0	250	500	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	100	200	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	70	140	210	

*The formula given is for the typical characteristics only.

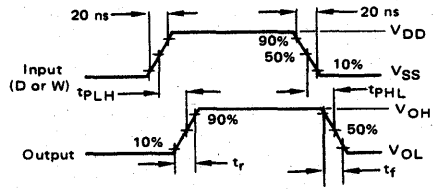
5

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORM



f in respect to system clock

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



MOTOROLA Semiconductors

BOX 20912 • PHOENIX, ARIZONA 85036

MC14532B

8-BIT PRIORITY ENCODER

The MC14532B is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (E_{in}) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (E_{out}).

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Low Input Capacitance — 5.0 pF typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUT									OUTPUT				
E_{in}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_{out}
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

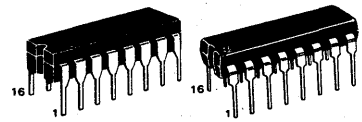
X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-BIT PRIORITY ENCODER



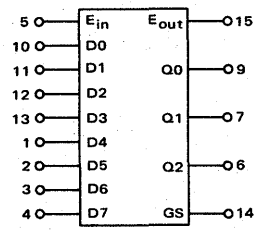
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.74 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.65 µA/kHz) f + I_{DD}							
		15	I_T = (5.73 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

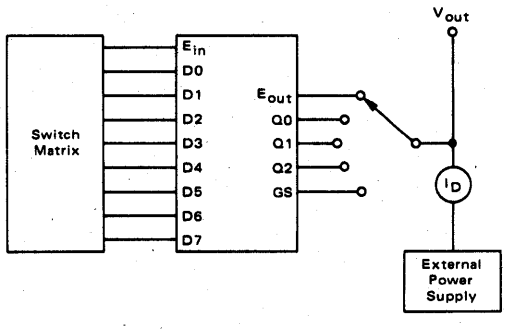
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 12.5 ns		15	37	55	80	
Propagation Delay Time — E_{in} to E_{out}	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 25 ns		5.0	205	315	475	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	110	165	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 20 ns		15	80	125	190	
Propagation Delay Time — E_{in} to GS	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 25 ns		5.0	175	270	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	90	135	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 20 ns		15	65	105	155	
Propagation Delay Time — E_{in} to Q_n	t_{PHL}, t_{PLH}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 85 ns		5.0	280	430	650	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 52 ns		10	140	210	325	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 40 ns		15	100	150	250	
Propagation Delay Time — D_n to Q_n	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns		5.0	300	465	720	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 77 ns		10	170	225	350	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 60 ns		15	110	170	265	
Propagation Delay Time — D_n to GS	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 85 ns		5.0	280	430	650	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 52 ns		10	140	210	325	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 40 ns		15	100	150	250	

*The formula given is for the typical characteristics only.

FIGURE 1 — TYPICAL SINK AND SOURCE CURRENT CHARACTERISTICS



Output Under Test	V_{GS} = V_{DD}, V_{DS} = V_{out} Sink Current		V_{GS} = -V_{DD}, V_{DS} = V_{out} -V_{DD} Source Current		
	D0 thru D7	E_{in}	D0 thru D6	D7	E_{in}
E_{out}	X	0	0	0	1
Q0	X	0	0	1	1
Q1	X	0	0	1	1
Q2	X	0	0	1	1
GS	X	0	0	1	1

FIGURE 2 — TYPICAL POWER DISSIPATION TEST CIRCUIT

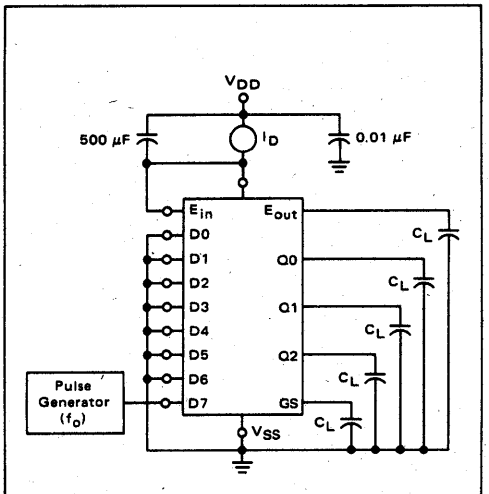
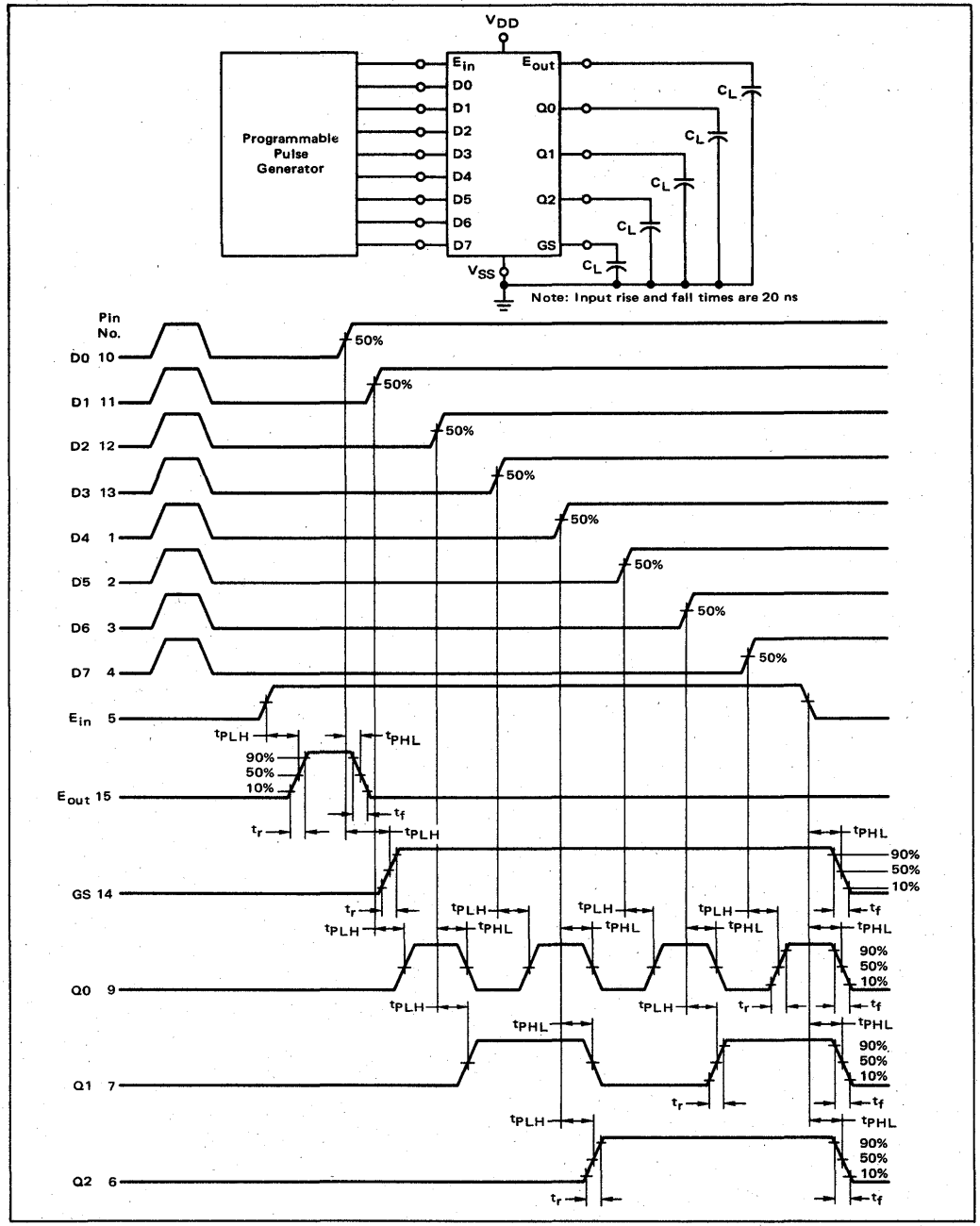


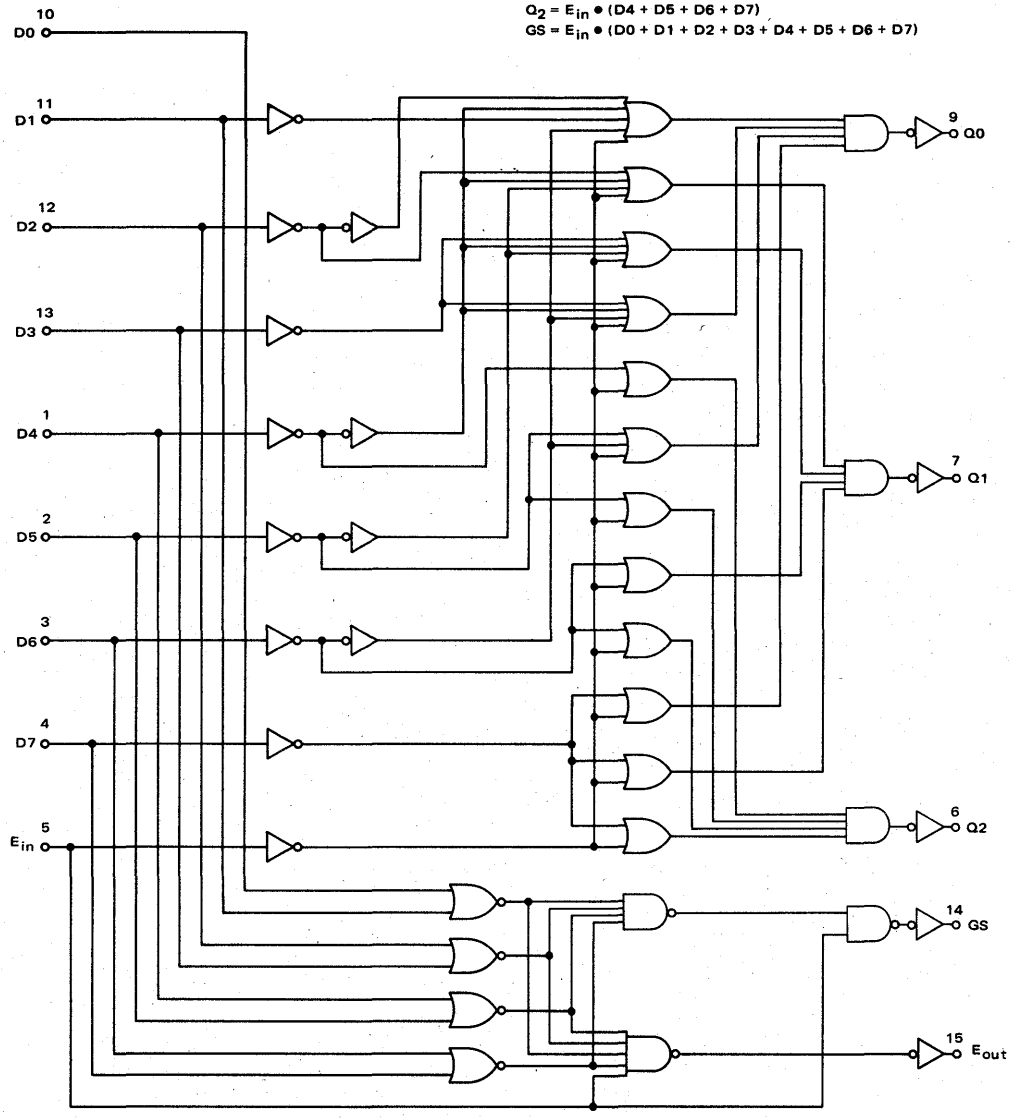
FIGURE 3 – AC TEST CIRCUIT AND WAVEFORMS



LOGIC DIAGRAM
(Positive Logic)

LOGIC EQUATIONS

$E_{out} = E_{in} \bullet \overline{D0} \bullet \overline{D1} \bullet \overline{D2} \bullet \overline{D3} \bullet \overline{D4} \bullet \overline{D5} \bullet \overline{D6} \bullet \overline{D7}$
$Q0 = E_{in} \bullet (D1 \bullet \overline{D2} \bullet \overline{D4} \bullet \overline{D6} + D3 \bullet \overline{D4} \bullet \overline{D6} + D5 \bullet \overline{D6} + D7)$
$Q1 = E_{in} \bullet (D2 \bullet \overline{D4} \bullet \overline{D5} + D3 \bullet \overline{D4} \bullet \overline{D5} + D6 + D7)$
$Q_2 = E_{in} \bullet (D4 + D5 + D6 + D7)$
$GS = E_{in} \bullet (D0 + D1 + D2 + D3 + D4 + D5 + D6 + D7)$



5

FIGURE 4 – TWO MC14532B's CASCADED FOR 4-BIT OUTPUT

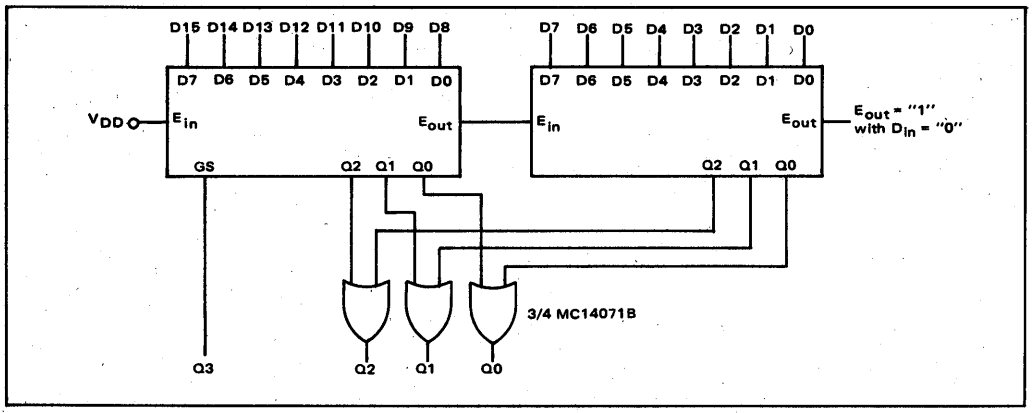
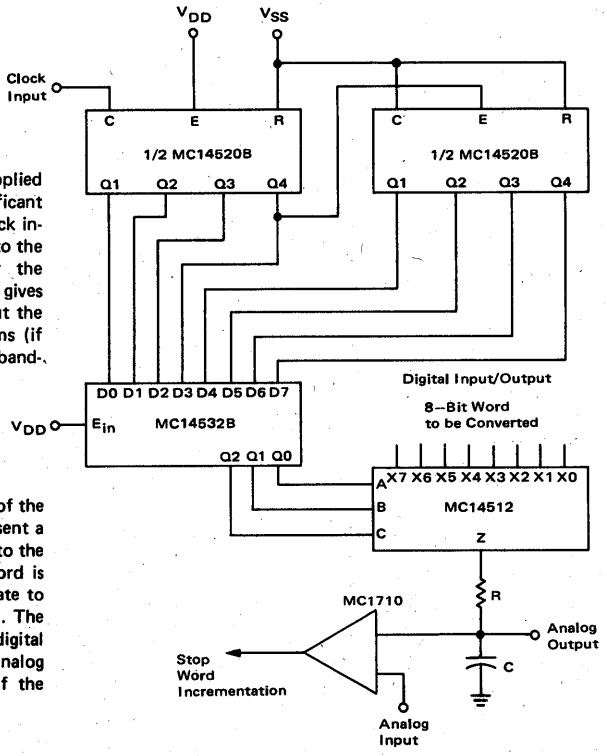


FIGURE 5 – DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTER



DIGITAL TO ANALOG CONVERSION

The digital eight-bit word to be converted is applied to the inputs of the MC14512 with the most significant bit at X7 and the least significant bit at X0. A clock input of up to 2.5 MHz (at V_{DD} = 10 V) is applied to the MC14520B. A compromise between I_{bias} for the MC1710 and ΔR between N and P-channel outputs gives a value of R of 33 k ohms. In order to filter out the switching frequencies, RC should be about 1.0 ms (if R = 33 k ohms, C ≈ 0.03 μF). The analog 3.0 dB bandwidth would then be dc to 1.0 kHz.

ANALOG TO DIGITAL CONVERSION

An analog signal is applied to the analog input of the MC1710. A digital eight-bit word known to represent a digitized level less than the analog input is applied to the MC14512 as in the D to A conversion. The word is incremented at rates sufficient to allow steady state to be reached between incrementations (i.e. 3.0 ms). The output of the MC1710 will change when the digital input represents the first digitized level above the analog input. This word is the digital representation of the analog word.

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14534B

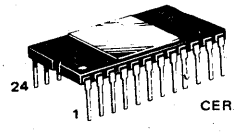
McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)
REAL TIME
5-DECADE COUNTER

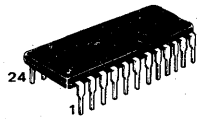
REAL TIME 5-DECADE COUNTER

The MC14534B is a complementary MOS circuit composed of five decade ripple counters that have their respective outputs time multiplexed using an internal scanner. Outputs of each counter are selected by the scanner and appear on four BCD pins. The selected decade is indicated by a logic high on the appropriate digit select pin. Both BCD and digit select outputs have three-state controls providing an "open-circuit" when these controls are high and allowing time multiplexing. Cascading may be accomplished by using the carry-out pin. The counters and scanner can be independently reset by applying a high to the counter master reset (MR) and the scanner reset (SR). The MC14534B was specifically designed for application in real time or event counters where continual updating and multiplexed displays are used.

- Four Operating Modes (See truth table)
- Input Error Detection Circuit
- Clock Conditioning Circuits for Slow Transition Inputs
- Counter Sequences on Positive Transition of Clock A
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 716



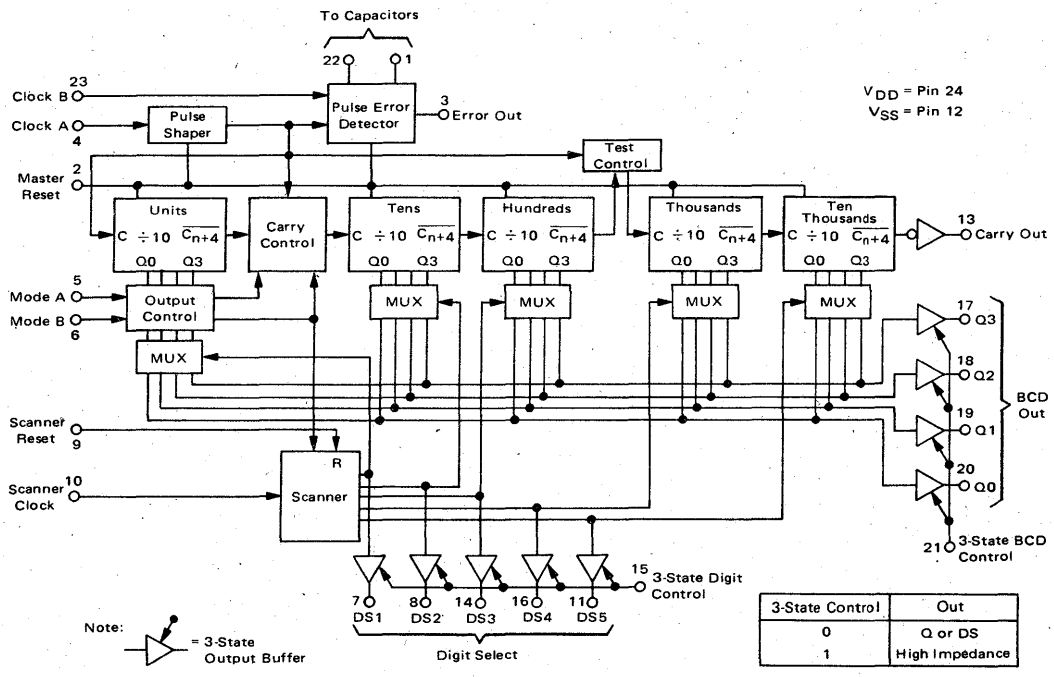
P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes

- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



3-State Control	Out
0	Q or DS
1	High Impedance

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	1.0	–	1.0	1.5	–	–	1.0	
(V_O = 9.0 or 1.0 Vdc)		10	2.0	–	2.0	3.0	–	–	2.0	
(V_O = 13.5 or 1.5 Vdc)		15	3.0	–	3.0	4.5	–	–	3.0	
(V_O = 0.5 or 4.5 Vdc) "1" Level	V_{IH}	5.0	4.0	–	4.0	3.5	–	4.0	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	8.0	–	8.0	7.0	–	8.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	12	–	12	11	–	12	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Output Drive Current — Pins 1 and 22 (AL Device)										mAdc
(V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.31	–	-0.25	-0.8	–	-0.17	–	
(V_{OH} = 9.5 Vdc)		10	-0.31	–	-0.25	-0.4	–	-0.17	–	
(V_{OH} = 13.5 Vdc)		15	-0.9	–	-0.75	-1.6	–	-0.51	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.024	–	0.02	0.03	–	0.014	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.06	–	0.05	0.09	–	0.035	–	
(V_{OL} = 1.5 Vdc)		15	1.3	–	0.25	1.63	–	0.175	–	
Output Drive Current — Pins 1 and 22 (CL/CP Device)										mAdc
(V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.11	–	-0.10	-0.8	–	-0.08	–	
(V_{OH} = 9.5 Vdc)		10	-0.11	–	-0.10	-0.4	–	-0.08	–	
(V_{OH} = 13.5 Vdc)		15	-0.33	–	-0.30	-1.6	–	-0.24	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.012	–	0.01	0.02	–	0.008	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.03	–	0.025	0.05	–	0.02	–	
(V_{OL} = 1.5 Vdc)		15	0.14	–	0.12	1.35	–	0.10	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	μAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.5\ \mu A/kHz)\ f + I_{DD}$ Scan Oscillator Frequency = 1 kHz							μAdc
		10	$I_T = (1.0\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (1.5\ \mu A/kHz)\ f + I_{DD}$							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

†To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3}\ (C_L - 50)\ V_{DD}f$ where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

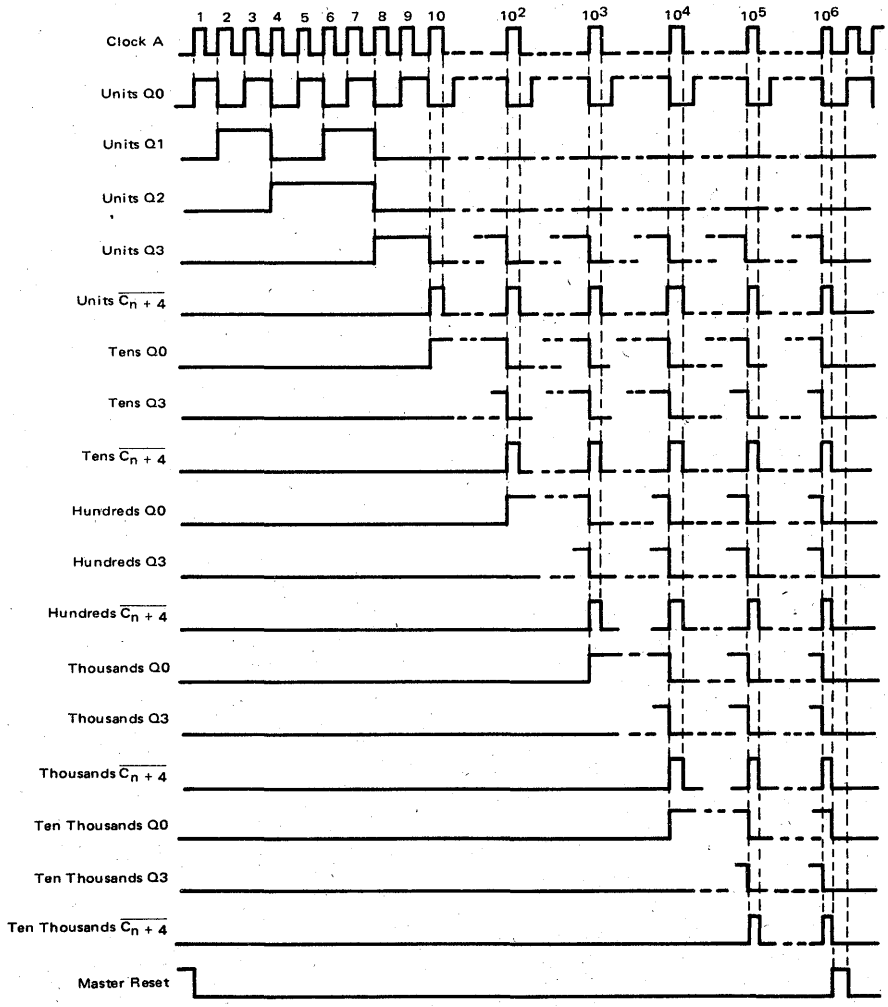
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
$t_r = (3.0\ ns/pF)\ C_L + 95\ ns$		5.0	–	–	180	350	400	
$t_r = (1.5\ ns/pF)\ C_L + 78\ ns$		10	–	–	90	150	200	
$t_r = (1.1\ ns/pF)\ C_L + 68\ ns$		15	–	–	65	110	160	
Output Fall Time	t_f							ns
$t_f = (1.5\ ns/pF)\ C_L + 117\ ns$		5.0	–	–	100	175	200	
$t_f = (0.75\ ns/pF)\ C_L + 89\ ns$		10	–	–	50	75	100	
$t_f = (0.55\ ns/pF)\ C_L + 67\ ns$		15	–	–	37	55	80	
Propagation Delay Time, Clock to Q	t_{PLH}, t_{PHL}							μs
$t_{PLH}, t_{PHL} = (1.8\ ns/pF)\ C_L + 4.0\ \mu s$		5.0	–	–	4.0	8.0	16	
$t_{PLH}, t_{PHL} = (0.8\ ns/pF)\ C_L + 1.5\ \mu s$		10	–	–	1.5	3.0	6.0	
$t_{PLH}, t_{PHL} = (0.6\ ns/pF)\ C_L + 1.0\ \mu s$		15	–	–	1.0	2.25	4.5	
Clock to Carry Out	t_{PLH}							μs
$t_{PLH} = (1.8\ ns/pF)\ C_L + 3.3\ \mu s$		5.0	–	–	3.3	6.6	13.2	
$t_{PLH} = (0.8\ ns/pF)\ C_L + 1.1\ \mu s$		10	–	–	1.1	2.2	4.4	
$t_{PLH} = (0.6\ ns/pF)\ C_L + 0.8\ \mu s$		15	–	–	0.8	1.7	3.9	
Master Reset to Q	t_{PHL}							μs
$t_{PHL} = (1.8\ ns/pF)\ C_L + 1.8\ \mu s$		5.0	–	–	1.8	3.6	7.2	
$t_{PHL} = (0.8\ ns/pF)\ C_L + 0.6\ \mu s$		10	–	–	0.6	1.2	2.4	
$t_{PHL} = (0.6\ ns/pF)\ C_L + 0.5\ \mu s$		15	–	–	0.5	0.9	1.8	
Master Reset to Error Out	t_{PHL}							μs
$t_{PHL} = (1.8\ ns/pF)\ C_L + 0.57\ \mu s$		5.0	–	–	0.6	1.5	3.0	
$t_{PHL} = (0.8\ ns/pF)\ C_L + 0.19\ \mu s$		10	–	–	0.2	0.5	1.0	
$t_{PHL} = (0.6\ ns/pF)\ C_L + 0.11\ \mu s$		15	–	–	0.12	0.38	0.75	
Scanner Clock to Q	t_{PLH}, t_{PHL}							μs
$t_{PLH}, t_{PHL} = (1.8\ ns/pF)\ C_L + 1.8\ \mu s$		5.0	–	–	1.8	3.6	7.2	
$t_{PLH}, t_{PHL} = (0.8\ ns/pF)\ C_L + 0.6\ \mu s$		10	–	–	0.6	1.2	2.4	
$t_{PLH}, t_{PHL} = (0.6\ ns/pF)\ C_L + 0.5\ \mu s$		15	–	–	0.5	0.9	1.8	
Scanner Clock to Digit Select	t_{PLH}, t_{PHL}							μs
$t_{PHL}, t_{PLH} = (1.8\ ns/pF)\ C_L + 1.5\ \mu s$		5.0	–	–	1.5	3.0	6.0	
$t_{PHL}, t_{PLH} = (0.8\ ns/pF)\ C_L + 0.5\ \mu s$		10	–	–	0.5	1.0	2.0	
$t_{PHL}, t_{PLH} = (0.6\ ns/pF)\ C_L + 0.4\ \mu s$		15	–	–	0.4	0.75	1.5	
Maximum Clock Pulse Frequency	PRF	5.0	0.5	0.25	1.0	–	–	MHz
		10	1.0	0.5	3.0	–	–	
		15	1.2	0.6	5.0	–	–	
Minimum Clock or Scanner Clock Pulse Width	PW_C	5.0	–	–	500	1000	2000	ns
		10	–	–	190	500	1000	
		15	–	–	125	375	750	
Master Reset Pulse Width	PW_{MR}	5.0	–	–	900	2000	4000	ns
		10	–	–	300	600	1500	
		15	–	–	250	450	1125	

*The formula given is for the typical characteristics only.

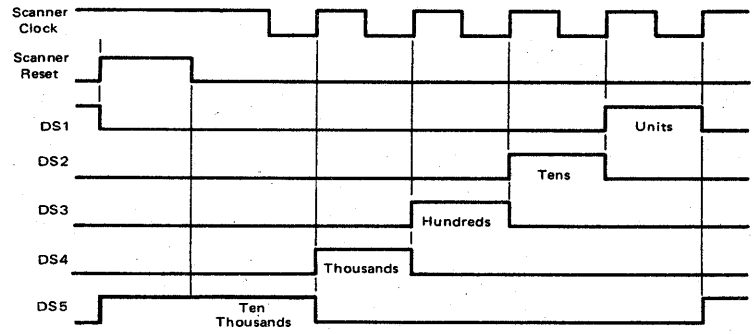
COUNTER TIMING DIAGRAM



MODE CONTROL TRUTH TABLE

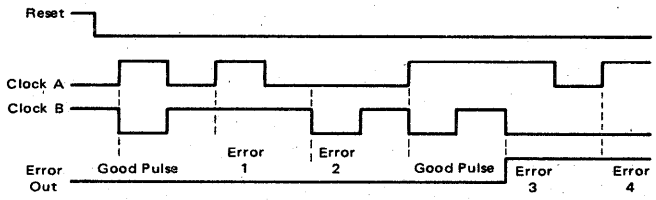
Mode A	Mode B	First Decade Output	Carry to Second Stage	Application
0	0	Normal Count and Display	At 9 to 0 transition of first decade	5-Decade Counter
0	1	Inhibited	Input Clock	Test Mode: Clock directly into stages 1, 2, and 4.
1	1	Inhibited	At 4 to 5 transition of first decade	4-decade counter with ÷ 10 and roundoff at front end.
1	0	Counts 3,4,5,6,7 = 5 Counts 8,9,0,1,2 = 0	At 7 to 8 transition of first decade	4-decade counter with 1/2 pence capability.

SCANNER TIMING DIAGRAM



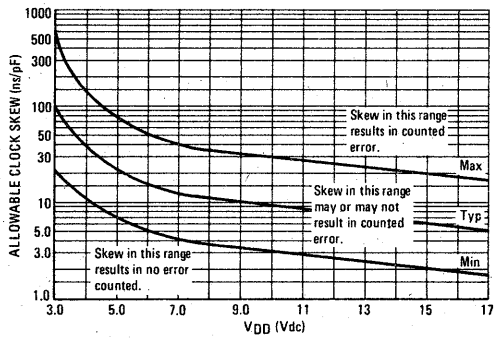
Note: If Mode B = 1, the first decade is inhibited and S1 will not go high, and the cycle will be shortened to four stages.
DS5 is selected automatically when Scanner Reset goes high.

ERROR DETECTION TIMING DIAGRAM



Note: Error detector looks for inverted pulse on Clock B. Whenever a positive edge at Clock A is not accompanied by a negative pulse at Clock B (or vice-versa) within a time period of the one-shots an error is counted. Three errors result in Error Out to go to a "1". If error detection is not needed, tie Clock B high or low and leave Pins 1 and 22 unconnected.

CLOCK SKEW RANGE

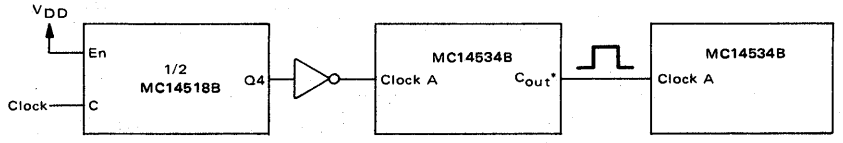


Notes:

1. The skew is the time difference between the low-to-high transition of C_A to the high-to-low transition of C_B or vice-versa. Capacitors C1 = C22 tied from pins 1 and 22 to V_{SS}.
2. This graph is accurate for C1 = C22 $\geqslant$ 100 pF.
3. When the error detection circuitry is not used, pins 1 and 22 are left open.

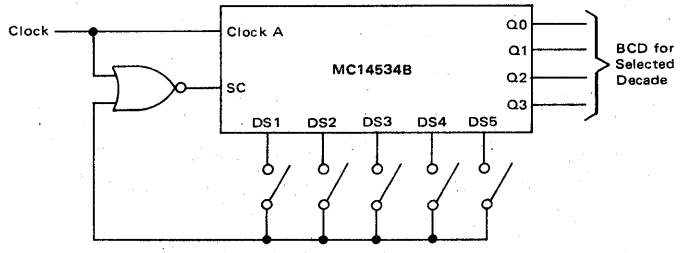
APPLICATIONS INFORMATION

FIGURE 1 – CASCADE OPERATION



*Carry Out is high for a single clock period when all five BCD decades go to zero. (Carry Out also goes high when MR is applied.)

FIGURE 2 – FORCING A DECADE TO THE Q OUTPUTS



When the Q outputs of a given decade are required, this configuration will lock up the selected decade within four clock cycles. The select line feedback may be hardwired or switched.

5

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14536B

PROGRAMMABLE TIMER

The MC14536B programmable timer is a flexible 24-stage ripple binary counter with 16 stages selectable by a binary code. Provisions for an on-chip RC oscillator, or an external clock are provided. An on-chip monostable circuit incorporating a pulse-type output has also been included. By selecting the appropriate output in conjunction with the correct input clock frequency, a variety of timing can be achieved.

- 24 Flip-Flop Stages – Will Count From 2^0 to 2^{24}
- Last 16 Stages Selectable By Four-Bit Select Code
- Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit Input
- On-Chip RC Oscillator Provisions
- On-Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation With Very Long Rise and Fall Times
- Clock Input f_{max} = 3.0 MHz typical @ V_{DD} = 10 Vdc
- Counter Advances On Negative Going Edge of Clock
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

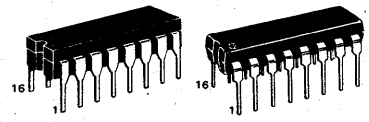
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE TIMER



L SUFFIX
CERAMIC PACKAGE
CASE 620

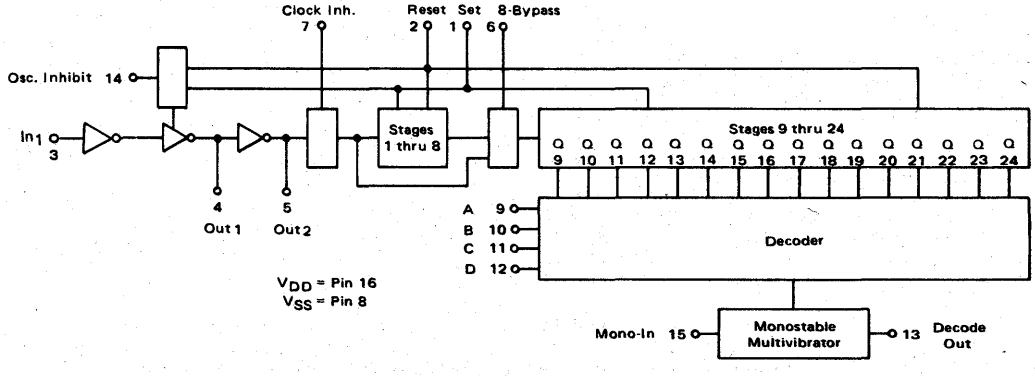
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

5

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.15 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.3 µA/kHz) f + I_{DD}							
		15	I_T = (3.55 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T$ (50 pF) + 3 x 10^{-3} (C_L -50) $V_{DD}f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time	t_{PLH},							ns
Clock to Q1, 8-Bypass (Pin 6) High	t_{PHL}							
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1715 ns		5.0	–	–	1800	3600	5400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 617 ns		10	–	–	650	1300	2000	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 425 ns		15	–	–	450	1000	1500	
Clock to Q1, 8-Bypass (Pin 6) Low	t_{PLH},							µs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3715 ns	t_{PHL}	5.0	–	–	3.8	7.6	12	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 1467 ns		10	–	–	1.5	3.0	4.5	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 1075 ns		15	–	–	1.1	2.3	3.5	
Clock to Q16	t_{PLH},							µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 6915 ns	t_{PHL}	5.0	–	–	7.0	14	21	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 2967 ns		10	–	–	3.0	6.0	9.0	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 2175 ns		15	–	–	2.2	4.5	7.0	
Reset to Q_n	t_{PHL}							ns
t_{PHL} = (1.7 ns/pF) C_L + 1415 ns		5.0	–	–	1500	3000	4500	
t_{PHL} = (0.66 ns/pF) C_L + 567 ns		10	–	–	600	1200	1800	
t_{PHL} = (0.5 ns/pF) C_L + 425 ns		15	–	–	450	900	1400	
Minimum Clock Pulse Width	PW_C	5.0	–	–	300	600	900	ns
		10	–	–	100	200	300	
		15	–	–	85	170	255	
Maximum Clock Pulse Frequency	PRF	5.0	0.6	0.4	1.2	–	–	MHz
(50% Duty Cycle)		10	2.0	1.5	3.0	–	–	
		15	2.5	2.0	5.0	–	–	
Maximum Clock Rise and Fall Time	t_r,t_f	5.0	No	No	–	–	–	–
		10	Limit	Limit	–	–	–	
		15			–	–	–	
Minimum Reset Pulse Width	PW_R	5.0	–	–	500	1000	1500	ns
		10	–	–	200	400	600	
		15	–	–	150	300	450	

*The formula given is for the typical characteristics only.

IN_1	Set	Reset	Clock Inh	Osc Inh	Out 2	Out 2	Decode Out
⌐	0	0	0	0	⌐	¬	No Change
¬	0	0	0	0	¬	⌐	Advance to next state
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0			No Change
0	0	0	0	X	0	1	No Change
1	0	0	0	⌐	¬	⌐	Advance to next state

X = Don't Care

TRUTH TABLE

D	C	B	A	Decode Out	8-Bypass
0	0	0	0	9	1
0	0	0	1	10	2
0	0	1	0	11	3
0	0	1	1	12	4
0	1	0	0	13	5
0	1	0	1	14	6
0	1	1	0	15	7
0	1	1	1	16	8
1	0	0	0	17	9
1	0	0	1	18	10
1	0	1	0	19	11
1	0	1	1	20	12
1	1	0	0	21	13
1	1	0	1	22	14
1	1	1	0	23	15
1	1	1	1	24	16

5

OPERATING CHARACTERISTICS

Set input initializes output to a "1". This is accomplished by setting an output conditioning latch to a 1 while at the same time resetting the 24 flip-flop stages. With the occurence of the first negative transition of the clock, the output will change to a "0". When the circuit is in the Set condition, the counter flip-flop stages will start counting on the second negative transition. The resulting behavior is the same as if each of the 24 flip-flop stages were set.

Reset inputs resets all stages to a logical "0". Reset or Set also disables the on-chip RC oscillator to allow very low power standby operation. In_1 input is used as the external Clock input or as the input to the on-chip RC oscillator.

Out 1, Out 2 outputs are used in the on-chip RC oscillator configuration.

8-Bypass input bypasses the first eight stages resulting in a 16-stage counter with all 16 stages selectable, one at a time. Clock Inhibit input disconnects the first counter stage from the input circuit, therefore inhibiting counting. This Clock Inhibit input is independent of the state of the Clock input. When the Clock Inhibit input is disabled, the counter will start counting only with the occurrence of the first negative edge of the Clock.

Binary Select inputs A, B, C, and D select the flip-flop stage to be connected to the output. Decode Out output can either be connected directly to a flip-flop output or to the monostable output. Osc Inhibit input can be used to disable the on-chip RC oscillator to allow very low power standby operation. Mono In input is used as the timing pin for the on-chip monostable oscillator. If the Mono In input is grounded through a resistor, the monostable circuit is disabled and the output is connected directly to the selected flip-flop. The monostable circuit is enabled if a resistor is connected between this pin and V_{DD} and a capacitor connected between this pin and ground. Any desired pulse width can be achieved depending upon the value of the R and C selected.

The test mode configuration divides the 24 flip-flop stages into three 8-stage sections to facilitate a fast test sequence. This test mode is enabled when 8-Bypass, Set and Reset are at a "1"

APPLICATIONS

FIGURE 1 – TIME INTERVAL CONFIGURATION USING EXTERNAL CLOCK; SET AND CLOCK INHIBIT FUNCTIONS

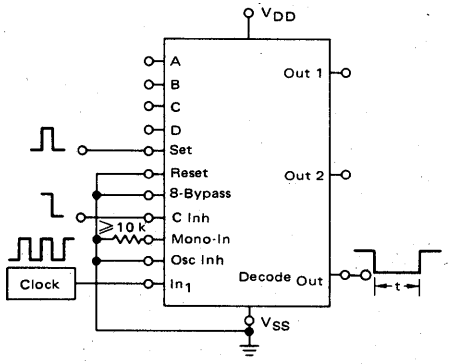


FIGURE 2 – TIME INTERVAL CONFIGURATION USING EXTERNAL CLOCK; RESET AND OUTPUT MONOSTABLE TO ACHIEVE A PULSE OUTPUT

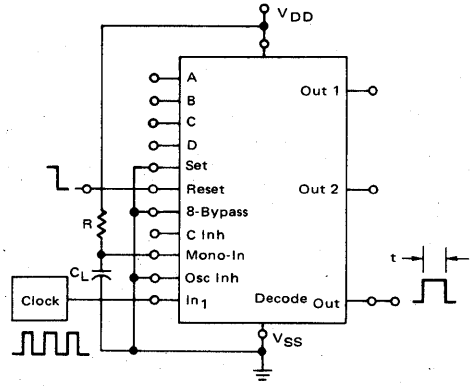
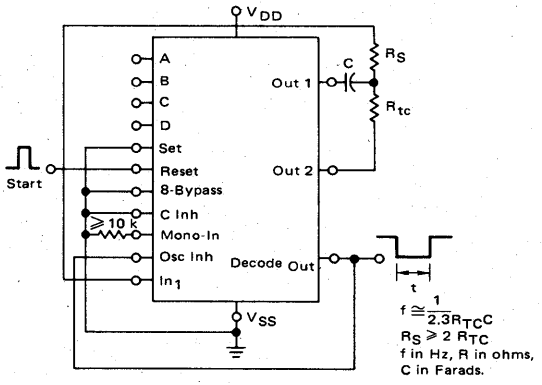
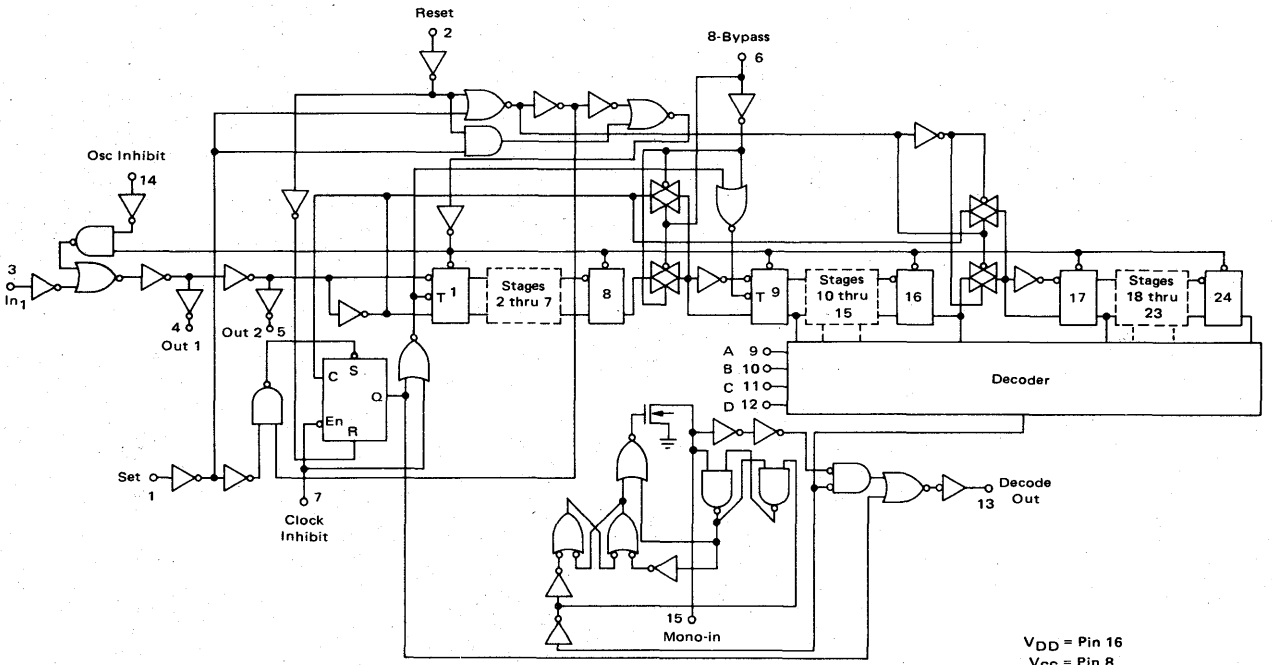


FIGURE 3 – TIME INTERVAL CONFIGURATION USING ON-CHIP RC OSCILLATOR AND RESET INPUT TO INITIATE TIME INTERVAL



LOGIC DIAGRAM



TYPICAL RC OSCILLATOR CHARACTERISTICS

(For Circuit Diagram See Figure 3 in Application)

FIGURE 4 – RC OSCILLATOR STABILITY

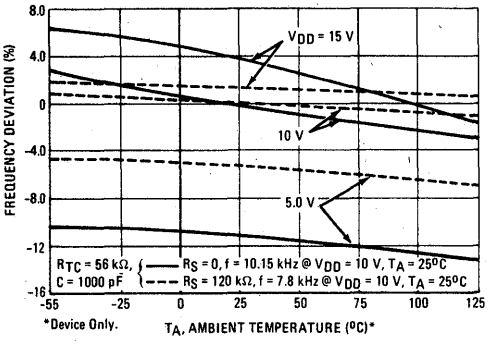
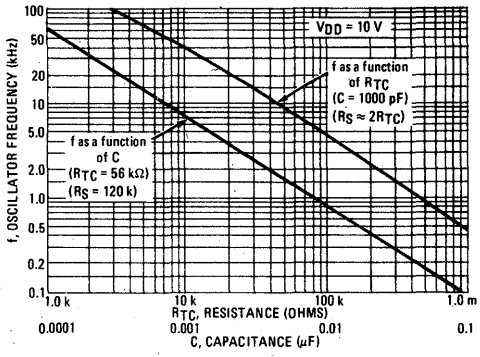


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C



MONOSTABLE CHARACTERISTICS

(For Circuit Diagram See Figure 2 in Application)

FIGURE 6 – TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 5.0 V

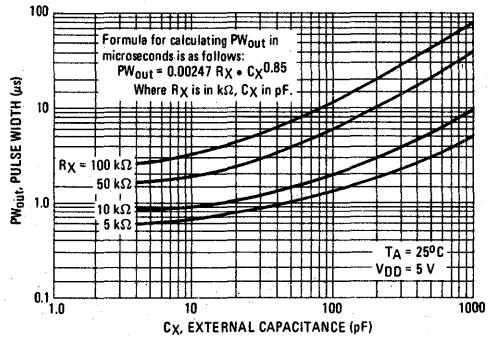


FIGURE 7 – TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 10 V

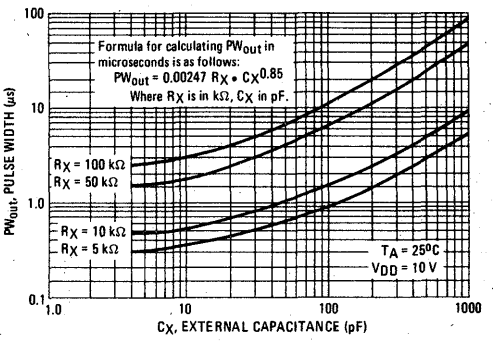
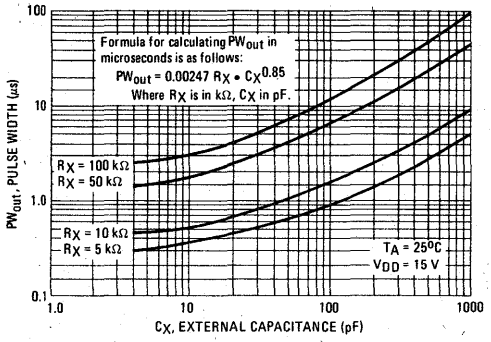


FIGURE 8 – TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 15 V



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 9 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

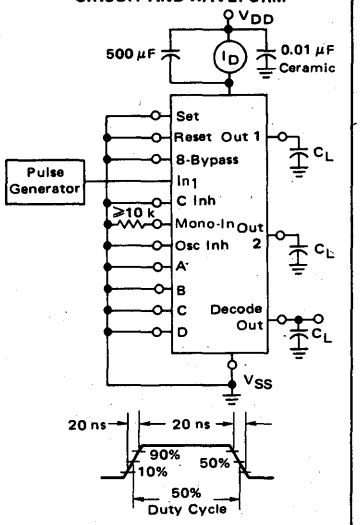
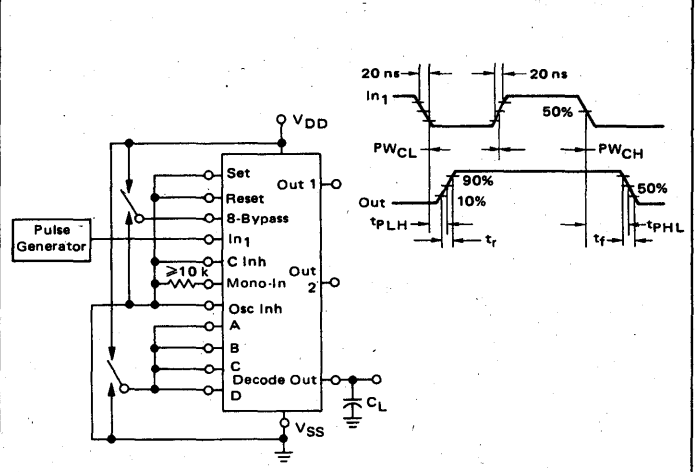


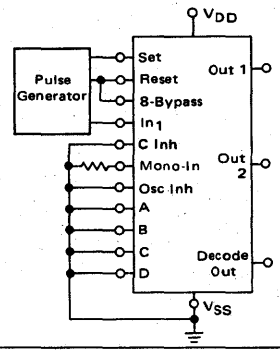
FIGURE 10 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



FUNCTIONAL TEST SEQUENCE

Test function (Figure 11) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into In_1 which will cause the counter to ripple from an all "1" state to an all "0" state.

FIGURE 11 – FUNCTIONAL TEST CIRCUIT



FUNCTIONAL TEST SEQUENCE

INPUTS				OUTPUTS	COMMENTS
In_1	Set	Reset	8-Bypass	Decade Out Q1 thru Q24	All 24 stages are in Reset mode.
1	0	1	1	0	
1	1	1	1	0	Counter is in three 8-stage sections in parallel mode.
0	1	1	1	0	First "1" to "0" transition of clock.
1 0 – – –	1	1	1		255 "1" to "0" transitions are clocked in the counter.
0	1	1	1	1	The 255 "1" to "0" transition.
0	0	0	0	1	Counter converted back to 24 stages in series mode. Set and Reset must be connected together and simultaneously go from "1" to "0".
1	0	0	0	1	In_1 Switches to a "1".
0	0	0	0	0	Counter Ripples from an all "1" state to an all "0" state.

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MCM14537

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14537 is a static random access memory (RAM) organized in a 256 x 1-bit pattern and constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of eight address inputs (A_n), one data input (D_{in}), one write enable input (WE), one strobe input (ST), two chip enable inputs (CE_n), and one data output (D_{out}).

Using both chip enable inputs as extensions of the address inputs, a 10-bit address scheme may be employed. Four MCM14537 devices may be used to comprise a 1024-bit memory without additional address decoding. The CE and ST inputs are dissimilary designed to enable usage of the memory in a variety of applications. An output latch is provided on the chip for storing the data read or written into memory, making a data-out storage register unnecessary. The CE inputs control the data output for third-state (high output impedance) or active operation which makes the memory very useful in a bus oriented system. When CE2 is high the chip is fully disabled. When CE1 is high the output is in the third state but data can be written into the output latch during a read cycle. This enables the use of the memory for fast reading by using the CE1 input to enable the latch. The memory is also designed so that dc signals can operate the memory with no maximum pulse width required on the CE and ST lines.

Medium speed operation and micropower operation make the device useful in scratch pad and buffer applications where micropower or battery operation and high noise immunity are required.

- Quiescent Current = 0.5 μA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- 3-state Output Capability for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

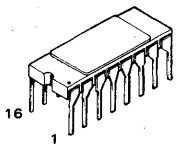
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (256 x 1) STATIC RANDOM ACCESS MEMORY

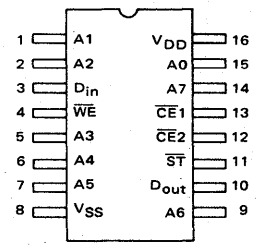


CERAMIC PACKAGE
CASE 690

ORDERING INFORMATION

MCM14XXX — Suffix Denotes
- L Ceramic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Noise Immunity #	V_{NL}									Vdc
($\Delta V_{out} \leq$ 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq$ 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq$ 1.5 Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq$ 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq$ 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq$ 1.5 Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±1.0	–	±0.00001	±1.0	–	±14	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	100	–	0.5	100	–	1800	µAdc
		10	–	200	–	1.0	200	–	3600	
		15	–	400	–	1.5	400	–	7200	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	100	–	0.5	100	–	1800	µAdc
		10	–	200	–	1.0	200	–	3600	
		15	–	400	–	1.5	400	–	7200	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.46 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.91 µA/kHz) f + I_{DD}							
		15	I_T = (4.37 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

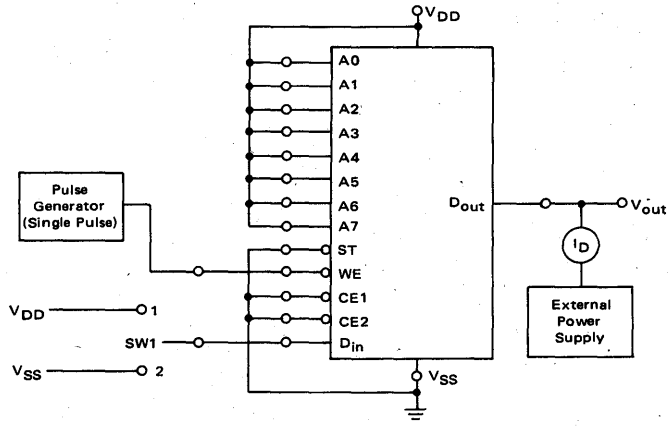
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	3	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns			5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns			10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns			15	–	–	65	110	160	
Output Fall Time	3	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns			5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns			10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns			15	–	–	37	55	80	
Read Access Time from $\overline{ST}$ or $\overline{CE2}$	4,5	$t_{acc(R)}$							ns
t_{acc} = (1.4 ns/pF) C_L + 2480 ns			5.0	450	400	2500	4000	6000	
t_{acc} = (0.7 nspF) C_L + 690 ns			10	200	150	700	1400	2000	
t_{acc} = (0.5 ns/pF) C_L + 393 ns			15	150	115	400	1050	1500	
Output Enable Delay from $\overline{CE1}$ or $\overline{CE2}$	5,6	$t_{acc(CE_n)}$	5.0	80	70	300	600	900	ns
			10	30	25	100	200	300	
			15	23	20	70	150	225	
Setup Time from A_n to $\overline{ST}$ or $\overline{CE2}$	4,5,6,7	$t_{setup(A)}$	5.0	–	–	600	1200	1800	ns
			10	–	–	200	400	600	
			15	–	–	140	300	450	
Hold Time from A_n to $\overline{ST}$ or $\overline{CE2}$	4,5,6,7	$t_{hold(A)}$	5.0	–	–	200	400	600	ns
			10	–	–	80	160	240	
			15	–	–	55	120	180	
Data Hold Time	7	$t_{hold(D)}$	5.0	–	–	480	960	1400	ns
			10	–	–	160	320	500	
			15	–	–	110	240	375	
Data Setup Time	7	$t_{setup(D)}$	5.0	–	–	1200	2400	3600	ns
			10	–	–	600	1200	1800	
			15	–	–	420	900	1350	
$\overline{\text{Write Enable}}$ Hold Time	7	$t_{hold(\overline{WE})}$	5.0	–	–	50	100	150	ns
			10	–	–	20	40	60	
			15	–	–	15	30	45	
$\overline{\text{Write Enable}}$ Setup Time	7	$t_{setup(\overline{WE})}$	5.0	–	–	240	480	720	ns
			10	–	–	80	160	240	
			15	–	–	55	120	180	
$\overline{\text{Write Enable}}$ to D_{out} Disable**	4	$t_{\overline{WE}}$	5.0	–	–	240	480	720	ns
			10	–	–	80	160	240	
			15	–	–	55	120	180	
$\overline{\text{Strobe}}$ or $\overline{CE2}$ Pulse Width When Reading	4,5,6	PW(R)	5.0	–	–	450	900	1350	ns
			10	–	–	150	300	450	
			15	–	–	100	225	340	
$\overline{\text{Strobe}}$, $\overline{CE1}$ or $\overline{CE2}$ Pulse Width When Writing	7	PW(W)	5.0	–	–	1200	1800	2400	ns
			10	–	–	600	840	1260	
			15	–	–	420	630	945	
Write Recovery Time	4	$t_{R(W)}$							ns
t_W = (1.4 ns/pF) C_L + 219 ns			5.0	80	70	240	480	720	
t_W = (0.7 ns/pF) C_L + 70 ns			10	30	25	80	160	240	
t_W = (0.5 ns/pF) C_L + 47.5 ns			15	25	20	55	120	180	
$\overline{CE1}$ or $\overline{CE2}$ to D_{out} Disable Delay**	6	$t_{\overline{CE}_n}$	5.0	80	70	300	600	900	ns
			10	30	25	100	200	300	
			15	25	20	70	150	225	
Read Setup Time	4,5	$t_{setup(R)}$	5.0	–	–	-100	-30	0	ns
			10	–	–	-40	-10	0	
			15	–	–	-30	-7.5	0	
Read Hold Time	4,5	$t_{hold(R)}$	5.0	–	–	180	360	540	ns
			10	–	–	60	180	240	
			15	–	–	45	135	180	
Read Cycle Time	4,5	$t_{cyc(R)}$	5.0	–	–	2500	4000	6000	ns
			10	–	–	700	1400	2100	
			15	–	–	500	1050	1575	
Write Cycle Time	7	$t_{cyc(W)}$	5.0	–	–	1400	3400	4800	ns
			10	–	–	700	1400	2100	
			15	–	–	500	1050	1575	

*The formula given is for the typical characteristics only.

**10% output change into a 1.0 kΩ load.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CURRENT CHARACTERISTICS TEST CIRCUIT



Input	Output Source Characteristics	Output Sink Characteristics
$\overline{WE}$	Pulse Once	Pulse Once
D_{in}	SW1 in Position 1	SW1 in Position 2
V_{GS}	$-V_{DD}$	V_{DD}
V_{DS}	$V_{out} - V_{DD}$	V_{out}

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

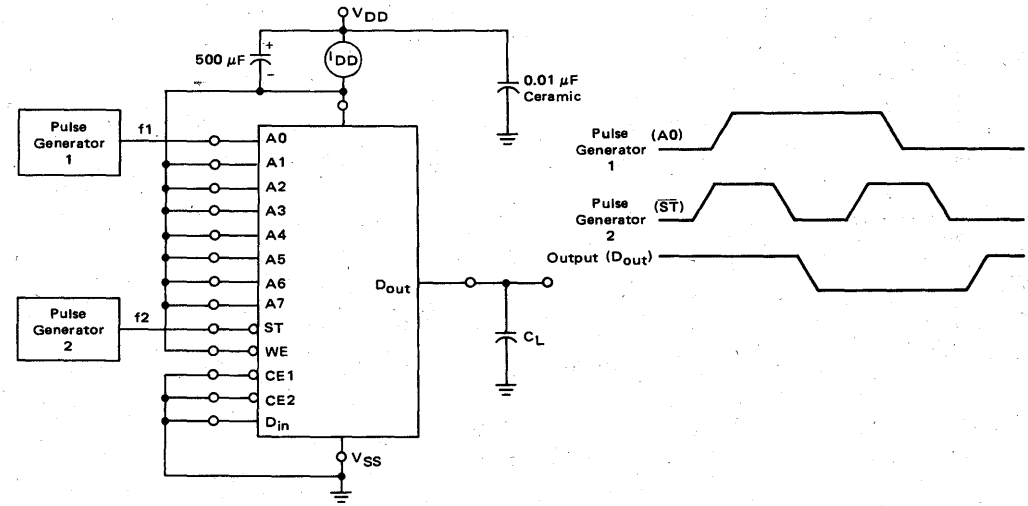


FIGURE 3 – AC TEST CIRCUIT

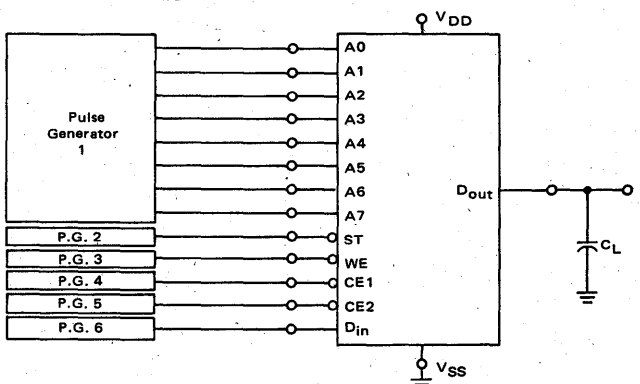
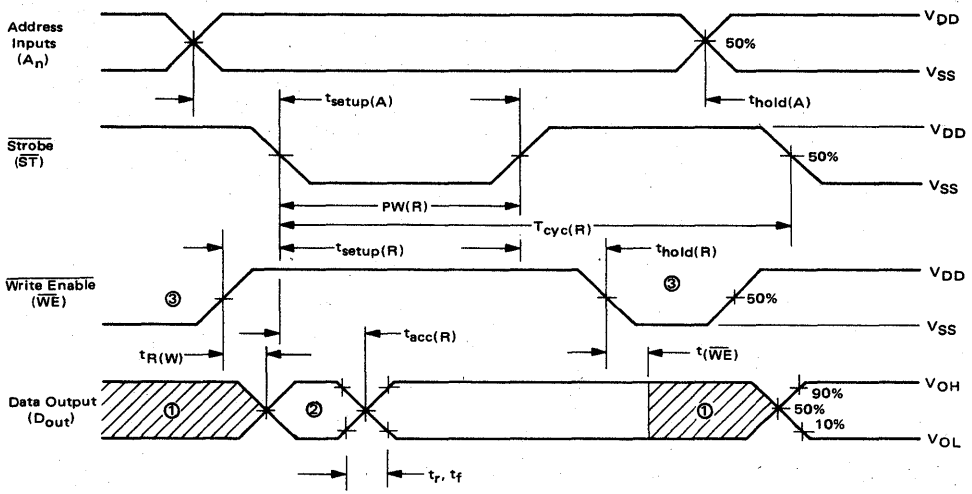
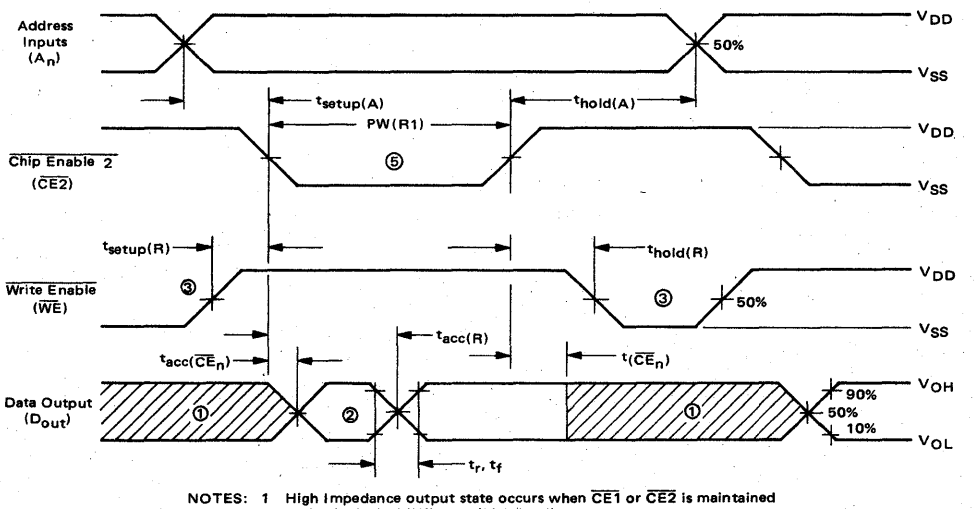


FIGURE 4 – READ CYCLE WAVEFORMS UTILIZING STROBE-TO-ACCESS MEMORY



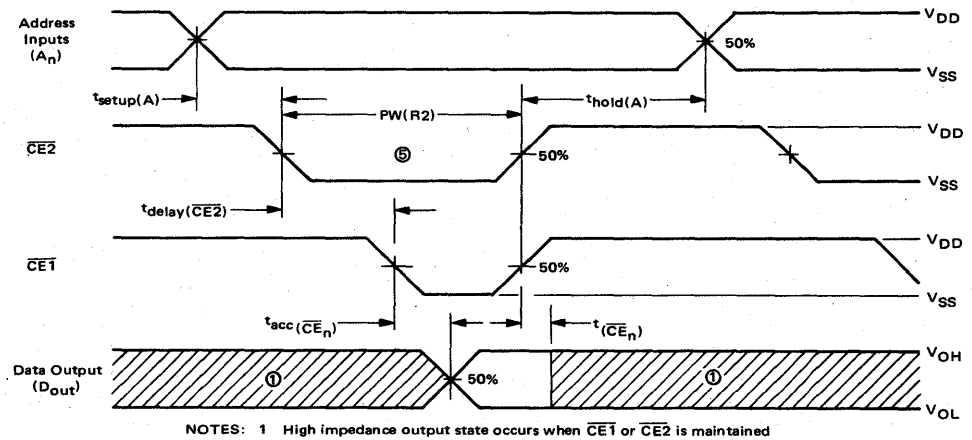
NOTES:
1. High impedance output state occurs when $\overline{WE}$ is maintained as a logical "0" (low level).
2. The output momentarily displays data from the previous state.
3. For read operation, $\overline{WE}$ may be maintained at a logical "1" (high level) during the complete cycle.
4. $\overline{CE1}$ and $\overline{CE2}$ are maintained at a logical "0" state (low level).
5. All input rise and fall times are 20 ns.

FIGURE 5 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE2}$ FOR ACCESS MEMORY



NOTES:
1. High impedance output state occurs when $\overline{CE1}$ or $\overline{CE2}$ is maintained in the logical "1" state (high level).
2. The output momentarily displays data from the previous state.
3. For read operation, $\overline{WE}$ may be maintained at a logical "1" (high level) during the complete cycle.
4. All input rise and fall times are 20 ns.
5. PW (R1) $\geqslant t_{acc}$ (R) max

FIGURE 6 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE1}$ AND $\overline{CE2}$ TO ACCESS MEMORY



NOTES: 1 High impedance output state occurs when $\overline{CE1}$ or $\overline{CE2}$ is maintained in the logical "1" state (high level).

2 $\overline{WE}$ is maintained at the logical "1" state for this example.

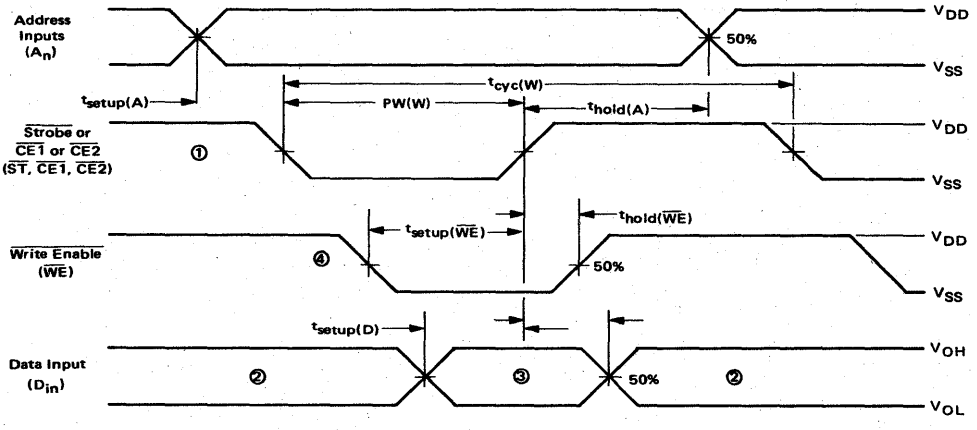
3 All input rise and fall times are 20 ns

4 $t_{delay(\overline{CE2})}$ minimum assuares that only data presently addressed will appear at the output.

$$t_{delay(\overline{CE2})}\ \text{min.} = t_{acc_R\ \text{max.}} - t_{acc(\overline{CE1})}\ \text{min.}$$

5 $PW(R2) \geqslant t_{delay}\ (\overline{CE2})\ \text{min} + t_{acc}\ (CE_n)\ \text{max}$

FIGURE 7 – WRITE CYCLE WAVEFORMS



NOTES: 1 The Strobe, $\overline{CE1}$ and $\overline{CE2}$ may be utilized to control a write cycle, however, during changes of address either Strobe or $\overline{CE2}$ must be in the logical "1" state (high level).

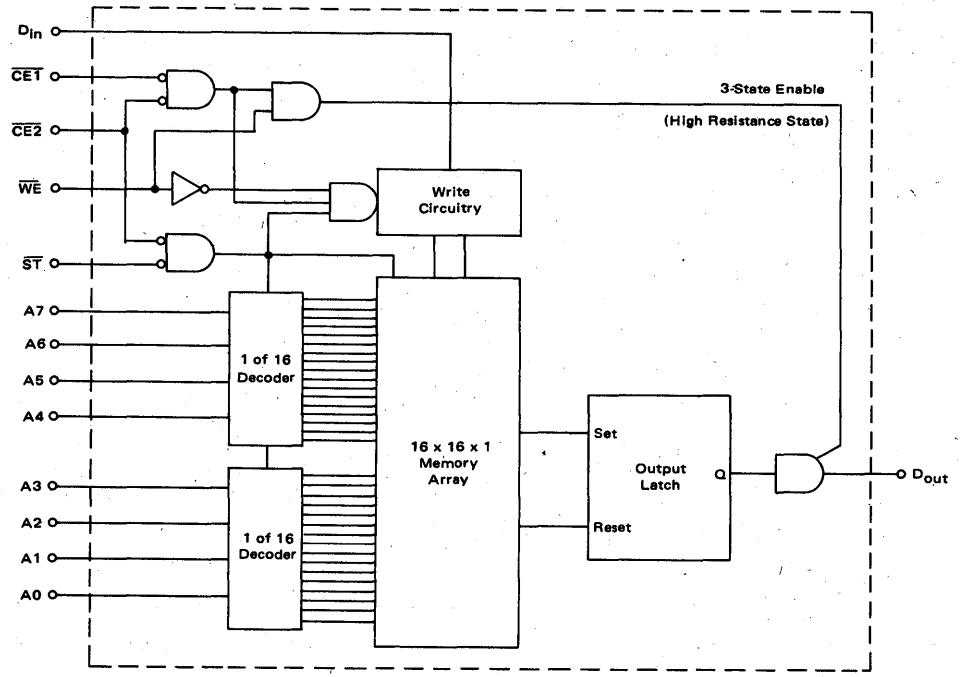
2 Data input logic level is don't care during the indicated intervals.

3 Data input logic level must remain fixed.

4 Write Enable may be maintained as a logical "0" during the write cycle.

5 All input rise and fall times are 20 ns.

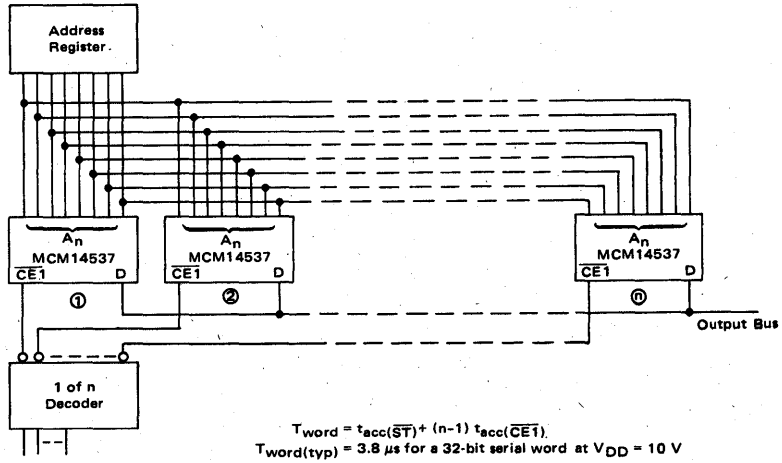
LOGIC/BLOCK DIAGRAM



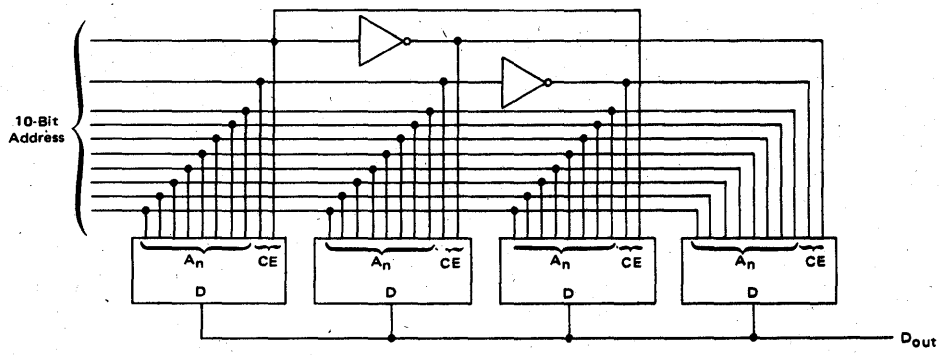
FUNCTION	$\overline{CE1}$	$\overline{CE2}$	$\overline{ST}$	$\overline{WE}$	D_{in}	D_{out}	COMMENTS
Address changing valid	X	X	1	X	X	R/A	D_{out} will be active if $\overline{CE1}$ and $\overline{CE2}$ = "0" and $\overline{WE}$ = "1".
	X	1	X	X	X	R	$\overline{CE2}$ = "1", fully disables internal logic and output.
Address changing not valid	X	0	0	X	X	R/A	Changing address in this mode may result in altered data.
D_{out} disabled in high resistance state	1	X	X	X	X	R	$\overline{CE1}$ = "1" disables write cycle and D_{out}.
	X	1	X	X	X	R	The chip is fully disabled.
	X	X	X	0	X	R	$\overline{WE}$ = "0" enables writing into memory if $\overline{CE1}$, $\overline{CE2}$, and $\overline{ST}$ = "0".
D_{out} enabled in active state	0	0	X	1	X	A	If $\overline{ST}$ = "1", the output stores and reads the previous data from or written into memory.
Read addressed memory location into output latch.	0	0	0	1	X	A	The output reads the present contents that are addressed.
	1	0	0	1	X	R	The addressed location is read into output latch with output in the "R" state.
Disable reading from memory	X	1	X	X	X	R	Address changing can take place in this condition.
	X	X	1	X	X	R/A	
Write into memory	0	0	0	0	A	R	D_{in} is written into memory and into the output latch
Write disabled	1	X	X	X	X	R	$\overline{WE}$ = "1" is a read enable.
	X	1	X	X	X	R	$\overline{WE}$ = "0" is a write enable.
	X	X	1	X	X	R/A	
	X	X	X	1	X	R/A	

R = High resistance state at D_{out}
A = An active level of either V_{SS} or V_{DD}
R/A = An R or A condition depending on the don't care condition
X = Don't care condition (must be in the "1" or "0" state)
1 = A high level at V_{DD}
0 = A low level at V_{SS}

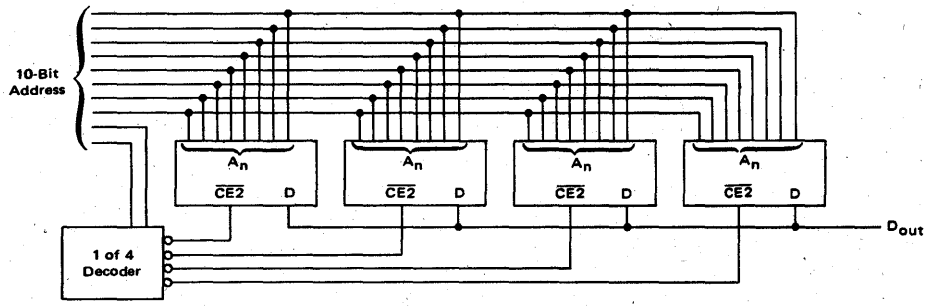
TYPICAL APPLICATION FOR SERIAL WORDS UTILIZING BUS TECHNIQUES



$T_{word} = t_{acc(\overline{ST})} + (n-1)\, t_{acc(\overline{CE1})}$
$T_{word(typ)} = 3.8\ \mu s$ for a 32-bit serial word at $V_{DD} = 10$ V



Typical 1024 x 1 RAM Utilizing Four MCM14537's.



Typical Low Power 1024 x 1 RAM Utilizing Four MCM14537's.

5

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14538B

Advance Information

McMOS MSI

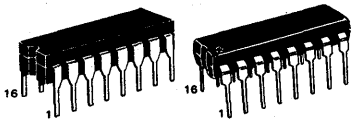
(LOW-POWER COMPLEMENTARY MOS)

DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

DUAL PRECISION MONOSTABLE MULTIVIBRATOR

The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X. Linear CMOS techniques allow more precise control of output pulse width.

- ±0.5% Typical Pulsewidth Variation from Part to Part
- ±0.5% Typical Pulsewidth Variation over Temperature Range
- New Formula: PW_{out} = RC (PW in seconds, R in ohms, C in farads)
- Pulse Width Range = 1.0 μs to ∞
- Symmetrical Output Sink and Source Capability
- Separate Latched Reset Inputs
- Quiescent Current (Standby) < 2 nA Typical
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive or Negative-Going Edge
- Pin-for-Pin Compatible with MC14528B and CD4098



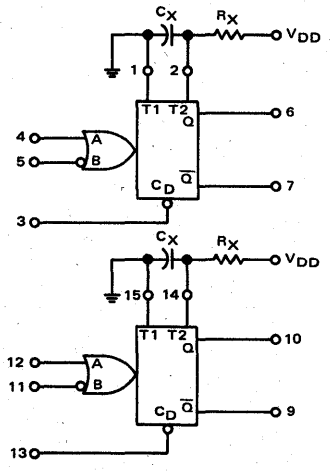
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



R_X and C_X are external components.
V_{DD} = Pin 16
V_{SS} = Pin 8

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This is advance information and specifications are subject to change without notice.

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–							µAdc
		10	–							
		15	–							
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–							µAdc
		10	–							
		15	–							
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0								µAdc
		10								
		15								

This table lists all of the characteristics to be specified for this device. Final specifications were not available at the time of printing. For the latest data, contact:

CMOS Marketing
Motorola Semiconductor Products Inc.
3501 Ed Bluestein Blvd.
Austin, Texas 78721
(512) 928-2600

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

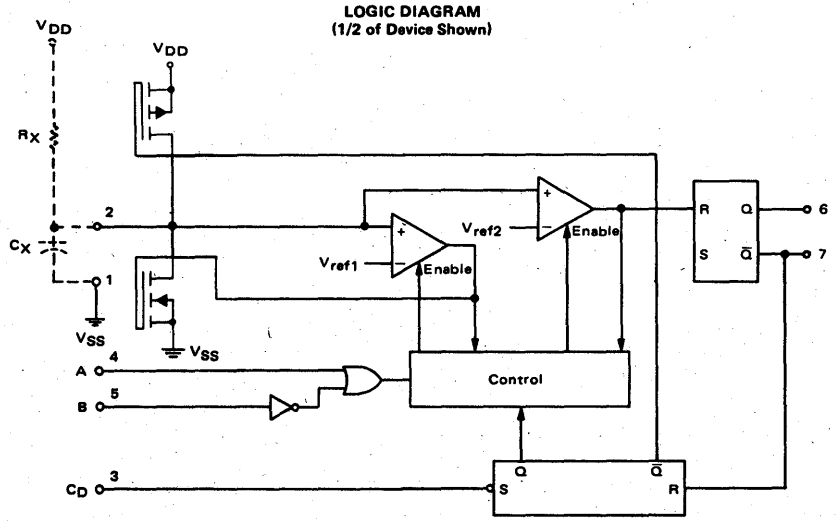
Characteristic	Symbol	C_X pF	R_X kΩ	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r	–	–	5.0 10 15	– – –	– – –				ns
Output Fall Time	t_f	–	–	5.0 10 15						ns
Propagation Delay Time A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}			5.0 10 15						ns
A or B to Q or $\overline{Q}$				5.0 10 15						ns
C_D to Q or $\overline{Q}$				5.0 10 15						ns
Minimum Input Pulse Width	PW_{in}			5.0 10 15	– – –	– – –				ns
Output Pulse Width – Q or $\overline{Q}$	PW_{out}			5.0 10 15	– – –	– – –				ns
Minimum Retrigger Time	t_{rr}			5.0 10 15	– – –	– – –				ns
External Timing Resistance	R_X	–	–	–				–	–	kΩ
External Timing Capacitance	C_X	–	–	–				–	–	μF

This table lists all of the characteristics to be specified for this device. Final specifications were not available at the time of printing. For the latest data, contact:

CMOS Marketing
Motorola Semiconductor Products Inc.
3501 Ed Bluestein Blvd.
Austin, Texas 78721
(512) 928-2600

5

LOGIC DIAGRAM
(1/2 of Device Shown)



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14539B

DUAL 4-CHANNEL DATA SELECTOR/MULTIPLEXER

The MC14539B data selector/multiplexer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of two sections of four inputs each. One input from each section is selected by the address inputs A and B. A "high" on the Strobe input will cause the output to remain "low".

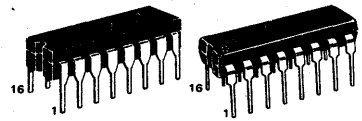
This device finds primary application in signal multiplexing functions. It permits multiplexing from N-lines to 1-line, and can also perform parallel-to-serial conversion. The Strobe input allows cascading of n-lines to n-lines.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- High Fanout >50
- Input Impedance = 10^{12} ohms typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-CHANNEL
DATA SELECTOR/MULTIPLEXER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

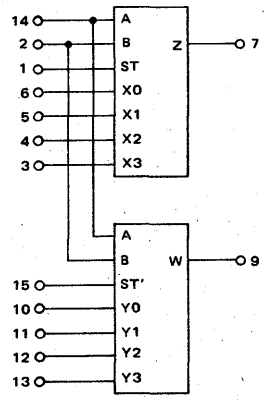
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS					
		X3	X2	X1	X0		OUTPUTS
B	A	Y3	Y2	Y1	Y0	ST,ST'	Z, W
X	X	X	X	X	X	1	0
0	0	X	X	X	0	0	0
0	0	X	X	X	1	0	1
0	1	X	X	0	X	0	0
0	1	X	X	1	X	0	1
1	0	X	0	X	X	0	0
1	0	X	1	X	X	0	1
1	1	0	X	X	X	0	0
1	1	1	X	X	X	0	1

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.85 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.7 µA/kHz) f + I_{DD}							
		15	I_T = (2.6 µA/kHz) f + I_{DD}							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

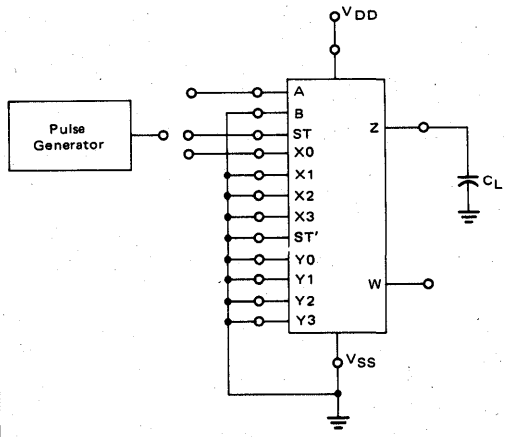
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

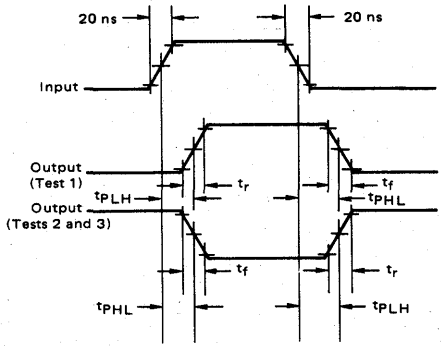
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ	Max		Unit
			All Types	AL Device	CL/CP Device	
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
X, Y Input to Output						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 125 ns		5.0	210	320	515	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	90	150	240	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	70	110	175	
A Input to Output	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 140 ns		5.0	225	340	565	
t_{PLH} = (0.66 ns/pF) C_L + 77 ns		10	110	165	275	
t_{PLH} = (0.5 ns/pF) C_L + 60 ns		15	85	130	215	
t_{PHL} = (1.7 ns/pF) C_L + 160 ns	t_{PHL}	5.0	245	430	645	ns
t_{PHL} = (0.66 ns/pF) C_L + 82 ns		10	115	190	285	
t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	90	150	220	
Strobe Input to Output	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 60 ns		5.0	145	220	365	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	75	115	185	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	60	90	140	

*The formula given is for the typical characteristics only.

FIGURE 1 – AC TEST CIRCUIT AND WAVEFORMS





Input Connections for t_r, t_f, t_{PLH}, T_{PHL}

TEST	STROBE	A	X0
1	Gnd	Gnd	P. G
2	P. G.	Gnd	V_{DD}
3	Gnd	P. G.	V_{DD}

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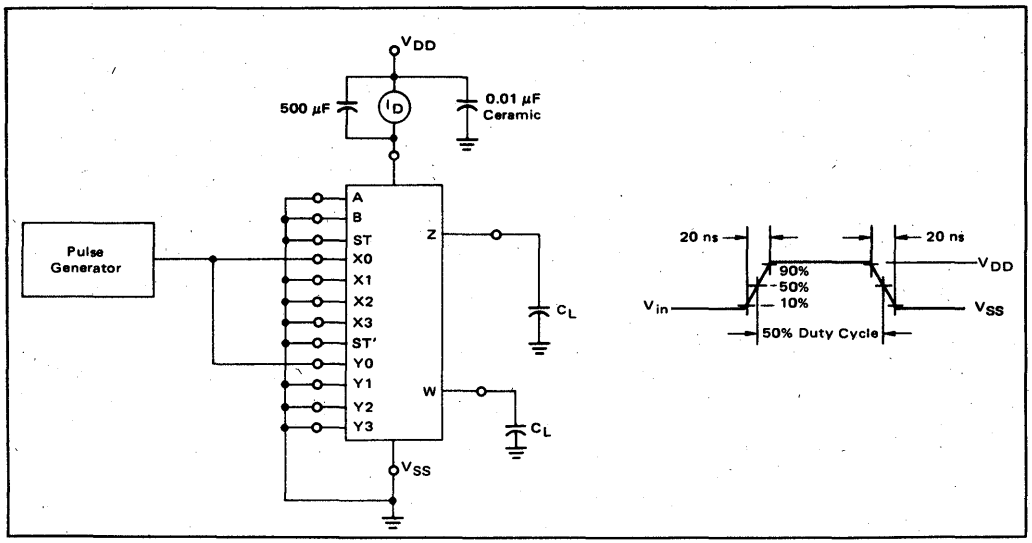
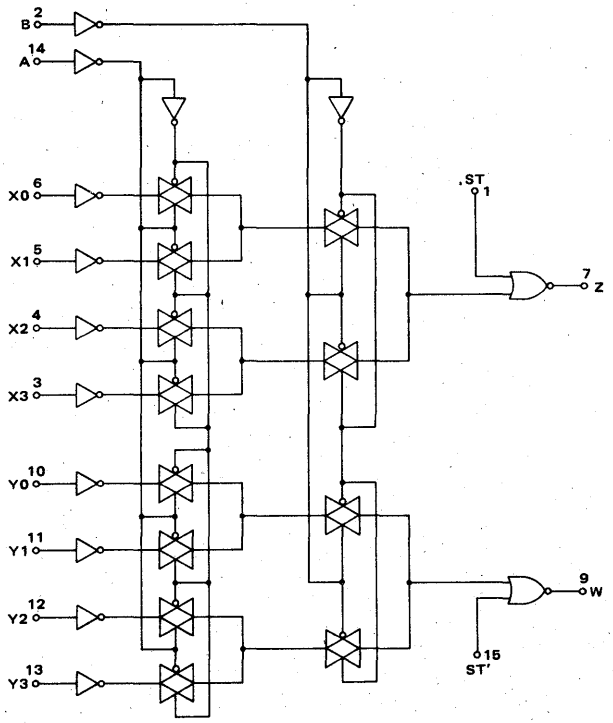
FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



LOGIC DIAGRAM



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MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14541B

PROGRAMMABLE TIMER

The MC14541B programmable timer consists of a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power-on reset circuit, and output control logic.

Timing is initialized by turning on power, whereupon the power-on reset is enabled and initializes the counter, within the specified V_{DD} range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16-stage counter divides the oscillator frequency (f_{osc}) with the n^{th} stage frequency being $f_{osc}/2^n$.

- Available Outputs 2^8, 2^{10}, 2^{13} or 2^{16}
- Increments on Positive Edge Clock Transitions
- Low Symmetrical Output Resistance (typically 100 Ω @ 15 Vdc)
- Built-in Low Power RC Oscillator (±2% accuracy over temperature range and ± 10% supply and ±3% over processing @ <10 kHz)
- Oscillator Frequency Range ≈ DC to 100 kHz
- Oscillator May Be Bypassed if External Clock Is Available (Apply external clock to Pin 3)
- Automatic Reset Initializes All Counters When Power Turns On (Limits – V_{DD} from 8.5 Vdc to 18 Vdc when enabled)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as 2^n Frequency Divider or Single Transition Timer
- Q/Q̄ Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow Clock Rise and Fall Times
- Supply Voltage Range = 3.0 Vdc to 18 Vdc

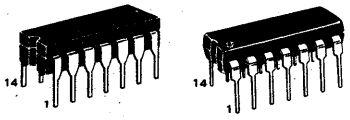
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

OSCILLATOR/TIMER



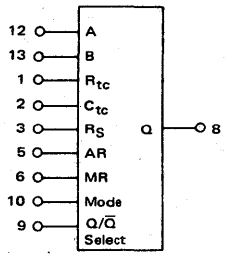
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	7.96	–	6.42	12.83	–	4.49	–	
(V_{OH} = 9.5 Vdc)		10	4.19	–	3.38	6.75	–	2.37	–	
(V_{OH} = 13.5 Vdc)		15	16.3	–	13.2	26.33	–	9.24	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.93	–	1.56	3.12	–	1.09	–	mAdc
(V_{OL} = 0.5 Vdc)		10	4.96	–	4.0	8.0	–	2.8	–	
(V_{OL} = 1.5 Vdc)		15	19.3	–	15.6	31.2	–	10.9	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	5.1	–	4.27	12.83	–	3.5	–	
(V_{OH} = 9.5 Vdc)		10	2.69	–	2.25	6.75	–	1.85	–	
(V_{OH} = 13.5 Vdc)		15	10.5	–	8.8	26.33	–	7.22	–	
(V_{OL} = 0.4 Vdc) Sink		5.0	1.24	–	1.04	3.12	–	0.85	–	
(V_{OL} = 0.5 Vdc)		10	3.18	–	2.66	8.0	–	2.18	–	
(V_{OL} = 15 Vdc)		15	12.4	–	10.4	31.2	–	8.50	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)										µAdc
		5.0	–	5.0	–	0.005	5.0	–	150	
(Pin 5 is High)	I_{DD}	10	–	10	–	0.010	10	–	300	
Auto Reset Disabled		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)										µAdc
		5.0	–	20	–	0.005	20	–	150	
(Pin 5 is High)	I_{DD}	10	–	40	–	0.010	40	–	300	
Auto Reset Disabled		15	–	80	–	0.015	80	–	600	
Auto Reset Quiescent Current										µAdc
		5.0	–	200	–	7	200	–	1200	
	I_{DDR}	10	–	250	–	30	250	–	1500	
(Pin 5 is low)		15	–	500	–	82	500	–	2000	
Supply Current**† (Dynamic plus Quiescent)	I_D	5.0	I_D = (0.4 µA/kHz) f + I_{DD}							µAdc
		10	I_D = (0.8 µA/kHz) f + I_{DD}							
		15	I_D = (1.2 µA/kHz) f + I_{DD}							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†When using the on chip oscillator the total supply current (in µAdc) becomes : $I_T = I_D + 2\ C_{tc}\ V_{DD}\ f \times 10^{-3}$ where I_D is in µA, C_{tc} is in pF, V_{DD} in Volts DC, and f in kHz. (see fig. 3)
Dissipation during power-on with automatic reset enabled is typically 50µA @ V_{DD} = 10Vdc.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	V_{DD} Symbol	Typical Vdc	All Types	Maximum AL Device	Maximum CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (p.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Turn-Off, Turn-On Clock to Q (2^8 Output)	t_{PLH}					µs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3415 ns	t_{PHL}	5.0	3.5	7.0	10.5	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 1217 ns		10	1.25	2.5	3.8	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 875 ns		15	0.9	1.9	2.9	
Turn-On, Turn-Off Clock to Q (2^{16} Output)	t_{PHL}					µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5915 ns	t_{PLH}	5.0	6.0	12	18	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 3467 ns		10	3.5	7.0	10	
t_{PHL}, t_{PLH} = (p.5 nsYpF) C_L + 2475 ns		15	2.5	5.25	7.5	
Minimum Clock Pulse Width	PW_C	5.0	300	600	900	ns
		10	100	200	300	
		15	85	150	225	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	–	–	MHz
		10	4.0	–	–	
		15	6.0	–	–	
Minimum MR Pulse Width	PW_{MR}	5.0	300	600	900	ns
		10	100	200	300	
		15	85	150	225	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

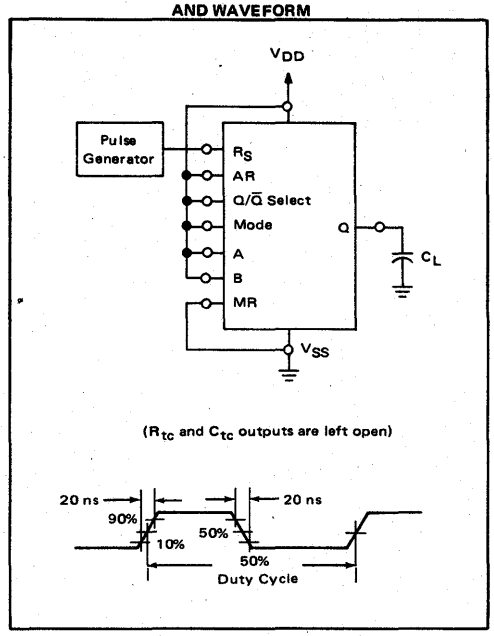

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

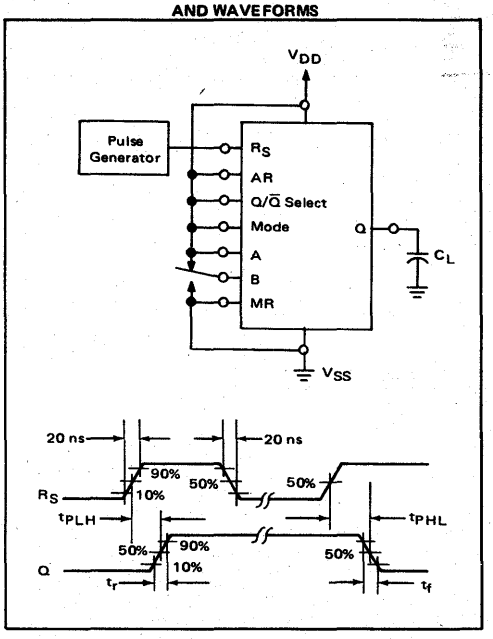

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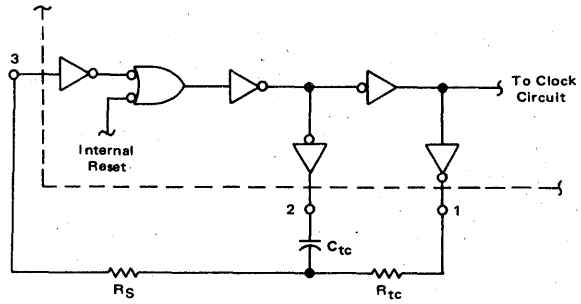
FIGURE 3 – OSCILLATOR CIRCUIT USING RC CONFIGURATION



TYPICAL RC OSCILLATOR CHARACTERISTICS

FIGURE 4 – RC OSCILLATOR STABILITY

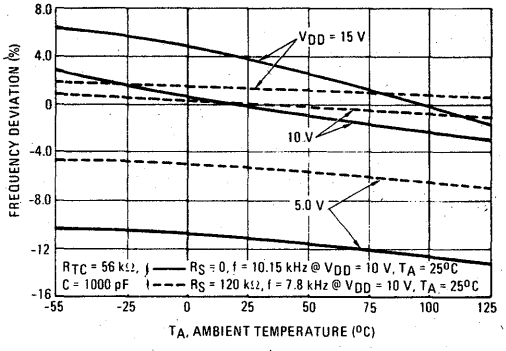
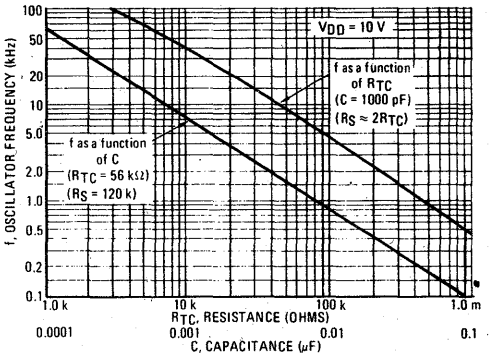
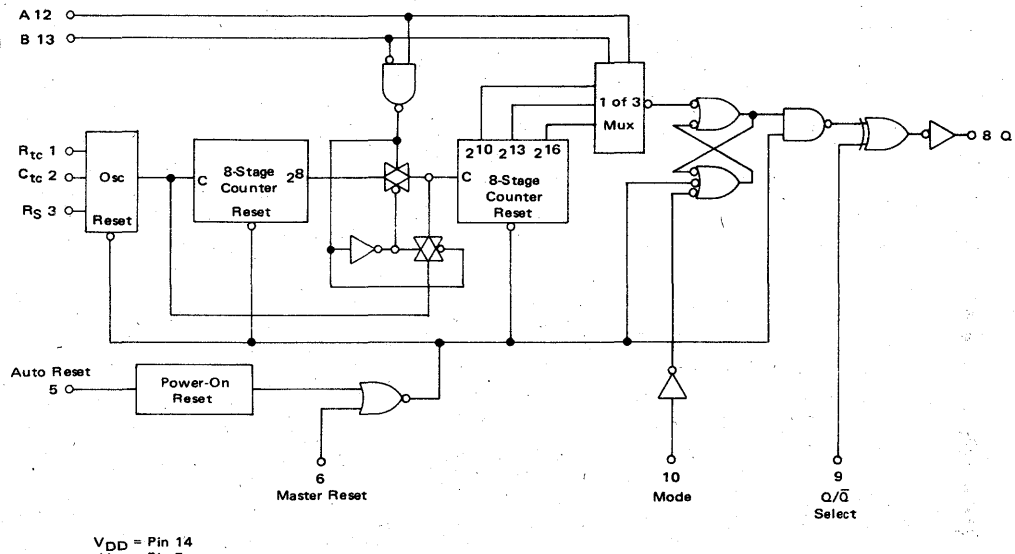


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C



EXPANDED BLOCK DIAGRAM



FREQUENCY SELECTION TABLE

A	B	Number of Counter Stages n	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

TRUTH TABLE

Pin	State	
	0	1
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset On
9	Output Initially Low After Reset	Output Initially High After Reset
10	Single Cycle Mode	Recycle Mode

OPERATING CHARACTERISTICS

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin when set to a "1" provides a low power operation.

The RC oscillator as shown in Figure 3 will oscillate with a frequency determined by the external RC network i.e.,

$$f = \frac{1}{2.3\,R_{tc}C_{tc}} \qquad \text{if } (1\text{ kHz} \leqslant f \leqslant 100\text{ kHz})$$

and $R_S \approx 2\,R_{tc}$ where $R_S \geqslant 10\text{ k}\Omega$

The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2^8, 2^{10}, 2^{13} and 2^{16}). The 2^n counts as shown in the Frequency Selection Table represents the Q output of the N^{th} stage of the counter. When A is "1", 2^{16} is selected for both states of B. However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputing 2^8).

The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/$\overline{Q}$ select pin is set to a "0" the Q output is a "0", correspondingly when Q/$\overline{Q}$ select pin is set to a "1" the Q output is a "1".

When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop (see Expanded Block Diagram) resets, counting commenced and after 2^{n-1} counts the RS flip-flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

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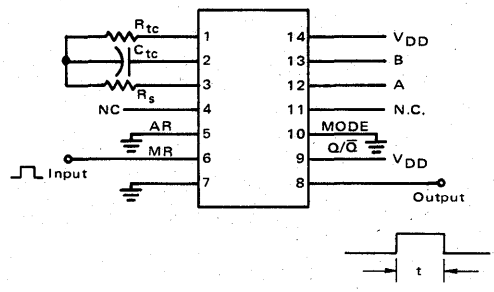


DIGITAL TIMER APPLICATION

When Master Reset (MR) receives a positive pulse, the internal counters and latch are reset. The Q output goes high and remains high until the selected (via A and B) number of clock pulses are counted, the Q output then goes low and remains low until another input pulse is received.

This "one shot" is fully retriggerable and as accurate as the input frequency. An external clock can be used (pin 3 is the clock input, pins 1 and 2 are outputs) if additional accuracy is needed.

Notice that a setup time equal to the desired pulse width output is required immediately following initial power up, during which time Q output will be high.

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14543B

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

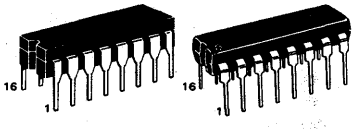
BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER for LIQUID CRYSTALS

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER for LIQUID CRYSTALS

The MC14543B BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (Bl), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. the outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockput display driver, and various clock, watch, and timer uses.

- Logic Circuit Quiescent Current = 5.0nA/package typical @ 5 Vdc
- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4056A (with Pin 7 Tied to V_{SS}).



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

5

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Rance	T_{stg}	−65 to +150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	I_{OHmax} I_{OLmax}	10	mAdc
Maximum Continuous Output Power* (Source or Sink) per Output	P_{OHmax} P_{OLmax}	70	mW

*$P_{OHmax} = I_{OH}(V_{OH} - V_{DD})$ and $P_{OLmax} = I_{OL}(V_{OL} - V_{SS})$

TRUTH TABLE

INPUTS							OUTPUTS							
LD	Bl	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	1	†				Inverse of Output Combinations Above							Display as above

X = Don't care
† = Above Combinations
* = For liquid crystal readouts, apply a square wave to Ph.
For common cathode LED readouts, select Ph = 0.
For common anode LED readouts, select Ph = 1.
** = Depends upon the BCD code previously applied when LD = 1.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 0.5 Vdc)		10	–	–	–	-8.7	–	–	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 9.5 Vdc)		10	–	–	–	10.1	–	–	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 0.5 Vdc)		10	–	–	–	-8.7	–	–	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 9.5 Vdc)		10	–	–	–	10.1	–	–	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.6 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.1 μA/kHz) f + I_{DD}							
		15	I_T = (4.7 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	100	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	110	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 520 ns		5.0	605	1100	1650	
t_{PLH} = (0.66 ns/pF) C_L + 217 ns		10	250	440	660	
t_{PLH} = (0.5 ns/pF) C_L + 160 ns		15	185	330	495	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 420 ns		5.0	505	1100	1650	
t_{PHL} = (0.66 ns/pF) C_L + 172 ns		10	205	440	660	
t_{PHL} = (0.5 ns/pF) C_L + 130 ns		15	155	330	495	
Minimum Setup Time	t_{setup}	5.0	-40	0	80	ns
		10	-15	0	30	
		15	-10	0	20	
Minimum Hold Time	t_{hold}	5.0	40	80	120	ns
		10	15	30	45	
		15	10	20	30	
Minimum Latch Disable Pulse Width (Strobing Data)	PW_{LD}	5.0	125	250	375	ns
		10	50	100	150	
		15	40	80	120	

*The formula given is for the typical characteristics only.

LOGIC DIAGRAM

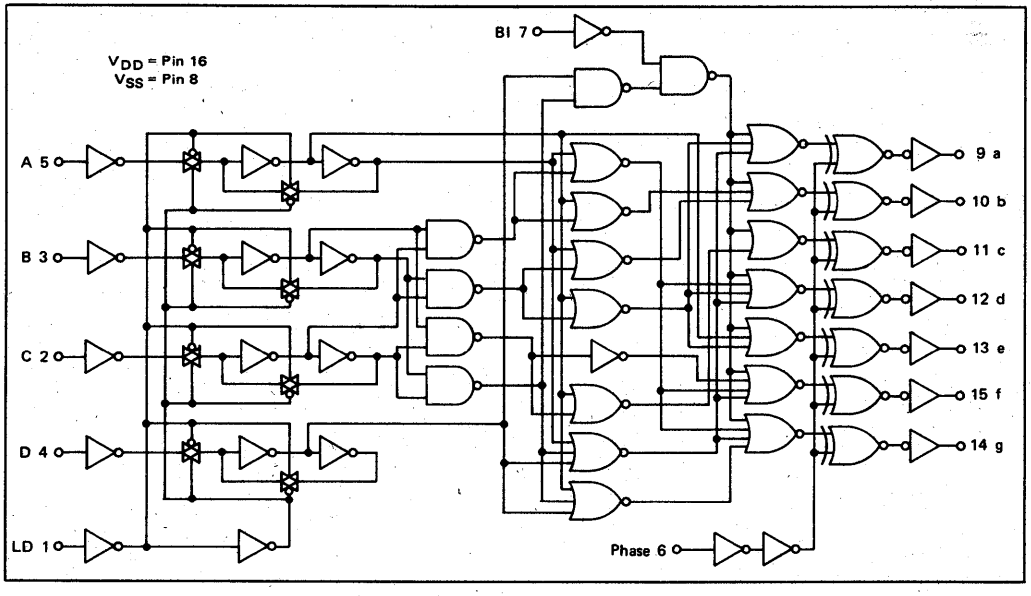


FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

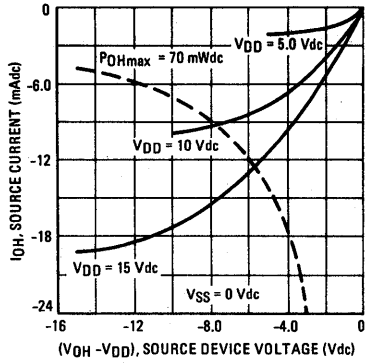


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS

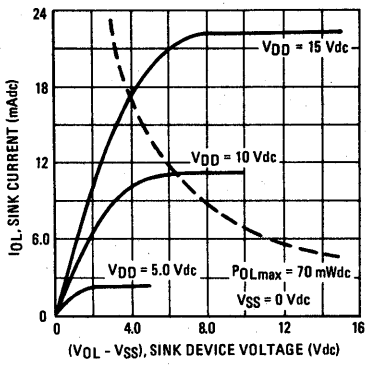


FIGURE 3 – DYNAMIC POWER DISIPATION SIGNAL WAVEFORMS

Inputs BI and Ph low, and Inputs D and LD high.
f in respect to a system clock.

All outputs connected to respective C_L loads.

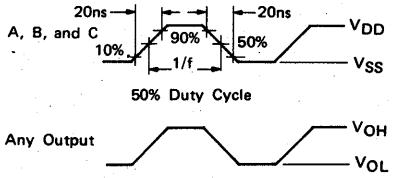
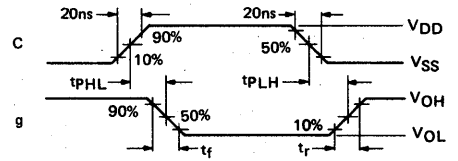
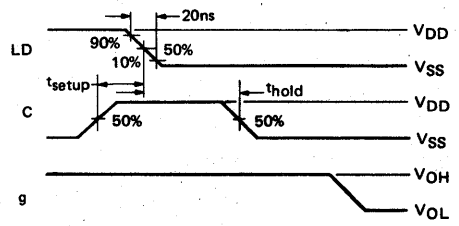


FIGURE 4 – DYNAMIC SIGNAL WAVEFORMS

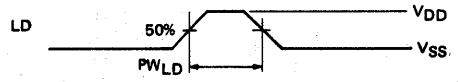
(a) Inputs D, Ph, and BI low, and Inputs A, B, and LD high.



(b) Inputs D, Ph, and BI low, and Inputs A and B high.



(c) Data DCBA strobed into latches



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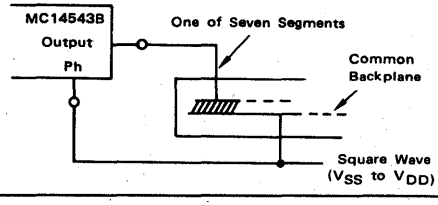
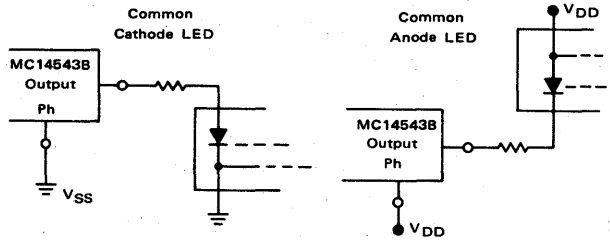
CONNECTIONS TO VARIOUS DISPLAY READOUTS

LIQUID CRYSTAL (LC) READOUT

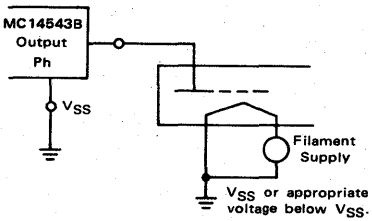


LIGHT EMITTING DIODE (LED) READOUT

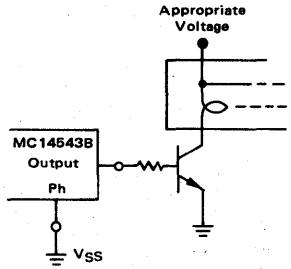


Note: Bipolar transistors may be added for gain (for $V_{DD} \leq 10V$ or $I_{out} \geq 10$ mA).

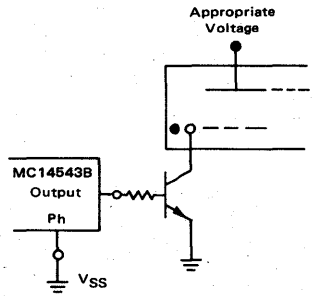
FLUORESCENT READOUT



INCANDESCENT READOUT

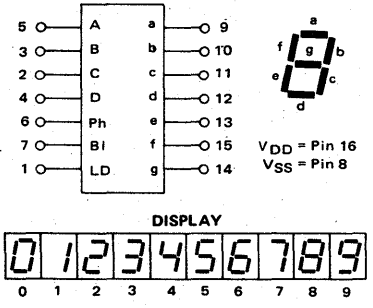


GAS DISCHARGE READOUT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).



MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14549B
MC14559B

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

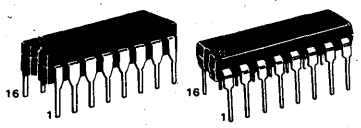
SUCCESSIVE APPROXIMATION REGISTERS

SUCCESSIVE APPROXIMATION REGISTERS

The MC14549B and MC14559B successive approximation registers are 8-bit registers providing all the digital control and storage necessary for successive approximation analog-to-digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the MC14549B is required in the cascaded mode when greater than 8 bits are desired. The Feed Forward (FF) of the MC14559B is used for register shortening where End-of-Conversion (EOC) is required after less than eight cycles.

Applications for the MC14549B and MC14559B include finding square roots, division, ring counters, serial-to-parallel conversion, and analog-to-digital conversion.

- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable
- Compatible with a Variety of Digital and Analog Systems such as the MC1408 8-Bit D/A Converter
- All Control Inputs Positive-Edge Triggered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



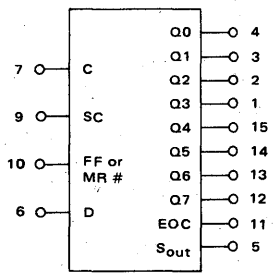
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

#For MC14549B Pin 10 is MR input
For MC14559B Pin 10 is FF input

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLES

MC14549B

SC	$SC_{(t-1)}$	MR	$MR_{(t-1)}$	Clock	Action
X	X	X	X	⎍	None
X	X	1	X	⎍	Reset
1	0	0	0	⎍	Start Conversion
1	X	0	1	⎍	Start Conversion
1	1	0	0	⎍	Continue Conversion
0	X	0	X	⎍	Continue Previous Operation

MC14559B

SC	$SC_{(t-1)}$	EOC	Clock	Action
X	X	X	⎍	None
1	0	0	⎍	Start Conversion
X	1	0	⎍	Continue Conversion
0	0	0	⎍	Continue Conversion
0	X	1	⎍	Retain Conversion Result
1	X	1	⎍	Start Conversion

X = Don't Care
t-1 = State at Previous Clock ⎍

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.28	–	1.02	1.76	–	0.72	–	mAdc
(V_{OL} = 0.5 Vdc) Q Outputs		10	3.2	–	2.6	4.5	–	1.8	–	
(V_{OL} = 1.5 Vdc)		15	8.4	–	6.8	17.6	–	4.8	–	
(V_{OL} = 0.4 Vdc) Sink		5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc) Pin 5, 11 only		5.0	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		10	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.04	–	0.88	1.76	–	0.72	–	mAdc
(V_{OL} = 0.5 Vdc) Q Outputs		10	2.6	–	2.2	4.5	–	1.8	–	
(V_{OL} = 1.5 Vdc)		15	7.2	–	6.0	17.6	–	4.8	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc) Pin 5, 11 only		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.8 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.6 μA/kHz) f + I_{DD}							
		15	I_T = (2.4 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L)$ $I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

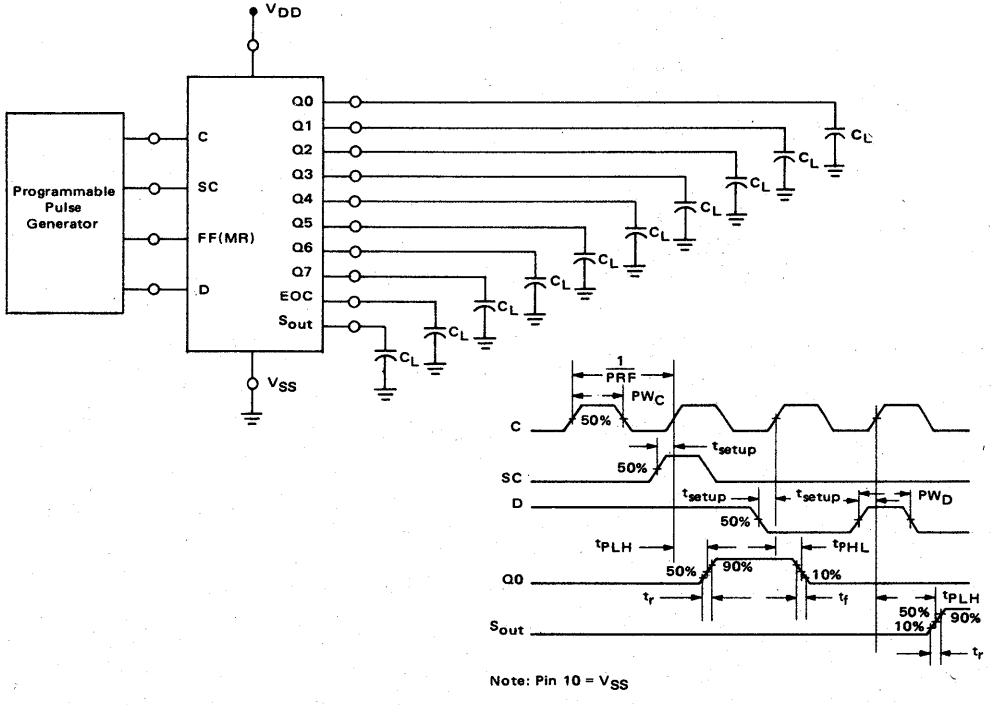
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time	t_{PLH},							ns
Clock to Q	t_{PHL}							
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	–	500	750	1200	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 177 ns		10	–	–	210	295	500	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 130 ns		15	–	–	155	225	380	
Clock to S_{out}								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns		5.0	–	–	750	1100	1800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 277 ns		10	–	–	310	450	750	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 195 ns		15	–	–	220	330	550	
Clock to EOC								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	–	300	440	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	–	130	195	325	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	–	100	150	250	
SC, D, FF or MR Setup Time	t_{setup}	5.0	–	–	125	175	300	ns
		10	–	–	50	75	150	
		15	–	–	40	55	115	
Minimum Clock Pulse Width	PW_C	5.0	–	–	350	500	600	ns
		10	–	–	135	200	300	
		15	–	–	100	150	225	
Minimum Pulse Width – D, SC, FF or MR	PW	5.0	–	–	250	375	750	ns
		10	–	–	100	150	300	
		15	–	–	80	115	225	
Maximum Clock Rise and Fall Time	t_r, t_f	5.0	15	15	–	–	–	μs
		10	5.0	5.0	–	–	–	
		15	4.0	4.0	–	–	–	
Maximum Clock Pulse Frequency	PRF	5.0	1.0	0.8	1.5	–	–	MHz
		10	2.0	1.5	3.0	–	–	
		15	2.5	2.0	4.0	–	–	

*The formula given is for the typical characteristics only.

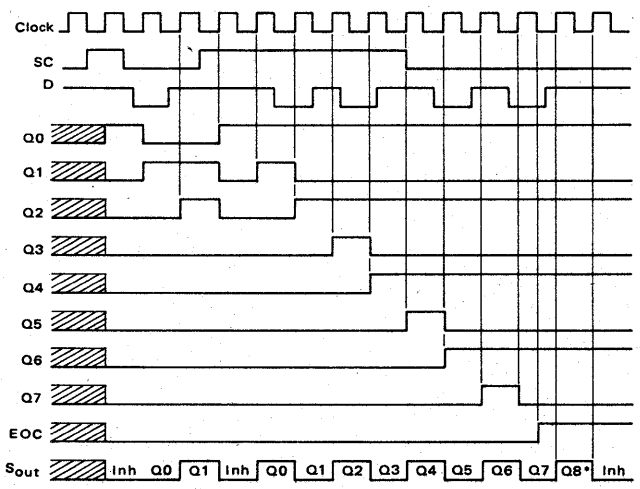
5

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



Note: Pin 10 = V_{SS}

TIMING DIAGRAM



– Don't care condition

Inh – Indicates Serial Out is inhibited low.

* – Q8 is ninth-bit of serial information available from 8-bit register.

Note: Pin 10 = V_{SS}

5

OPERATING CHARACTERISTICS

Both the MC14549B and MC14559B can be operated in either the "free run" or "strobed operation" mode for conversion schemes with any number of bits. Reliable cascading and/or recirculating operation can be achieved if the End of Convert (EOC) output is used as the controlling function, since with EOC = 0 (and with SC = 1 for MC14549B but either 1 or 0 for MC14559B) no stable state exists under continual clocked operation. The MC14559B will automatically recirculate after EOC = 1 during externally strobed operation, provided SC = 1.

All data and control inputs for these devices are triggered into the circuit on the positive edge of the clock pulse.

Operation of the various terminals is as follows:

C = Clock – A positive-going transition of the Clock is required for data on any input to be strobed into the circuit.

SC = Start Convert – A conversion sequence is initiated on the positive-going transition of the SC input on succeeding clock cycles.

D = Data In – Data on this input (usually from a comparator in A/D applications) is also entered into the circuit on a positive-going transition of the clock. This input is Schmitt triggered and synchronized to allow fast response and guaranteed quality of serial and parallel data.

MR = Master Reset (MC14549B only) – Resets all output to 0 on positive-going transitions of the clock. If removed while SC = 0, the circuit will remain reset until SC = 1. This allows easy cascading of circuits.

FF = Feed Forward (MC14559B only) – Provides register shortening by removing unwanted bits from a system.

For operation with less than 8 bits, tie the output *following* the least significant bit of the circuit to EOC. E.g., for a 6-bit conversion, tie Q6 to FF; the part will respond as shown in the timing diagram less two bit times. Note that Q6 and Q7 will still operate and must be disregarded.

For 8-bit operation, FF is tied to V_{SS}.

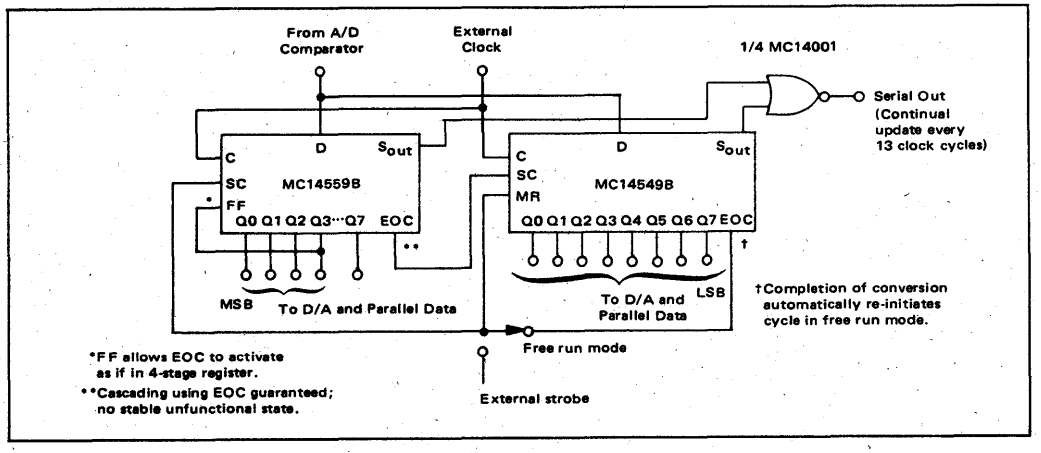
For applications with more than 8 but less than 16 bits, use the basic connections shown in Figure 1. The FF input of the MC14559B is used to shorten the setup. Tying FF directly to the least significant bit used in the MC14559B allows EOC to provide the cascading signal, and results in smooth transition of serial information from the MC14559B to the MC14549B. The Serial Out (S_{out}) inhibit structure of the MC14559B remains inactive one cycle after EOC goes high, while S_{out} of the MC14549B remains inhibited until the second clock cycle of its operation.

Q_n = Data Outputs – After a conversion is initiated the Q's on succeeding cycles go high and are then conditionally reset dependent upon the state of the D input. Once conditionally reset they remain in the proper state until the circuit is either reset or reinitiated.

EOC = End of Convert – This output goes high on the negative-going transition of the clock following FF = 1 (for the MC14559B) or the conditional reset of Q7. This allows settling of the digital circuitry prior to the End of Conversion indication. Therefore either level or edge triggering can indicate complete conversion.

S_{out} = Serial Out – Transmits conversion in serial fashion. Serial data occurs during the clock period when the corresponding parallel data bit is conditionally reset. Serial Out is inhibited on the initial period of a cycle, when the circuit is reset, and on the second cycle after EOC goes high. This provides efficient operation when cascaded.

FIGURE 1 – 12-BIT CONVERSION SCHEME



TYPICAL APPLICATIONS

Externally Controlled 6-Bit ADC (Figure 2)

Several features are shown in this application:

- Shortening of the register to six bits by feeding the seventh output bit into the FF input.
- Continuous conversion, if a continuous signal is applied to SC.
- Externally controlled updating (the start pulse must be shorter than the conversion cycle).
- The EOC output indicating that the parallel data are valid and that the serial output is complete.

Continuously Cycling 8-Bit ADC (Figure 3)

This ADC is running continuously because the EOC signal is fed back to the SC input, immediately initiating a new cycle on the next clock pulse.

Continuously Cycling 12-Bit ADC (Figure 4)

Because each successive approxiamtion register (SAR) has a capability of handling only an eight-bit word, two must be cascaded to make an ADC with more than eight bits.

When it is necessary to cascade two SAR's, the second SAR must have a stable resettable state to remain in while awaiting a subsequent start signal. However, the first stage must not have a stable resettable state while recycling, because during switch-on or due to outside influences, the first stage has entered a reset state, the entire ADC will remain in a stable non-functional condition.

This 12-bit ADC is continuously recycling. The serial as well as the parallel outputs are updated every thirteenth clock pulse. The EOC pulse indicates the completion of

FIGURE 2 – EXTERNALLY CONTROLLED 6-BIT ADC

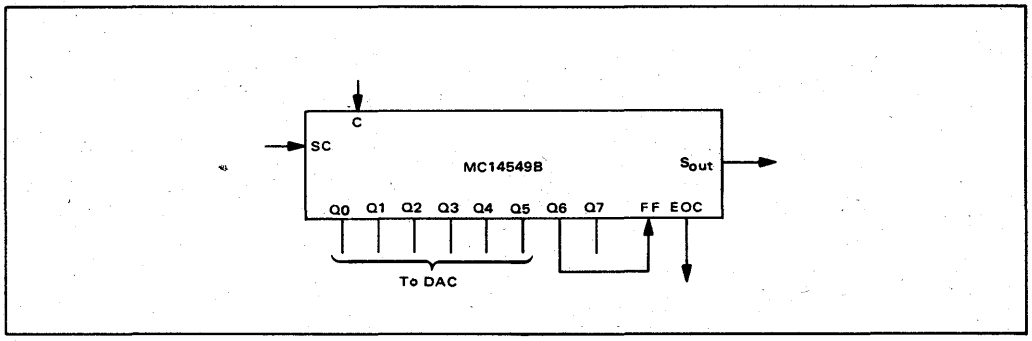


FIGURE 3 – CONTINUOUSLY CYCLING 8-BIT ADC

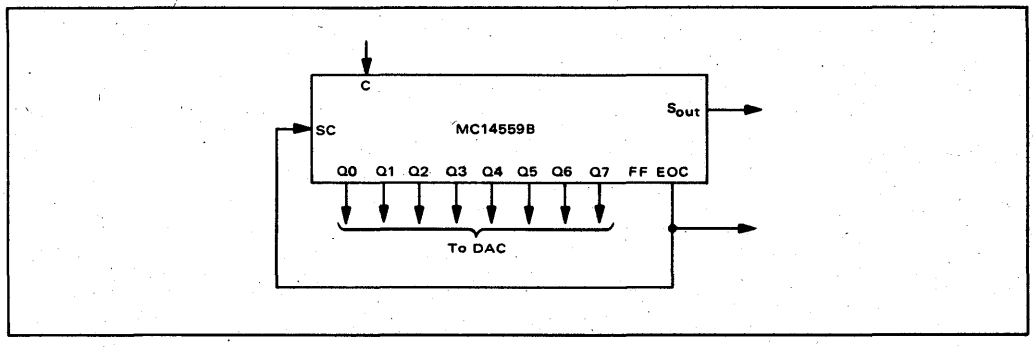
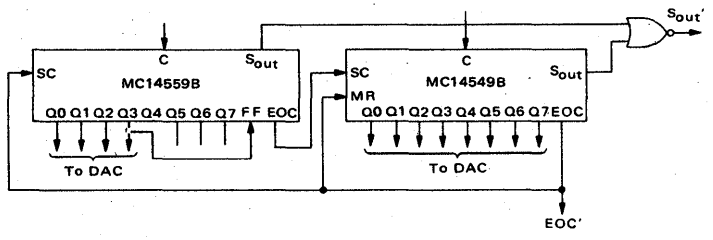


FIGURE 4 – CONTINUOUSLY CYCLING 12-BIT ADC



the 12-bit conversion cycle, the end of the serial output word, and the validity of the parallel data output.

Externally Controlled 12-Bit ADC (Figure 5)

In this circuit the external pulse starts the first SAR and simultaneously resets the cascaded second SAR. When Q4 of the first SAR goes high, the second SAR starts conversion, and the first one stops conversion. EOC indicates that the parallel data are valid and that the serial output is complete. Updating the output data is started with every external control pulse.

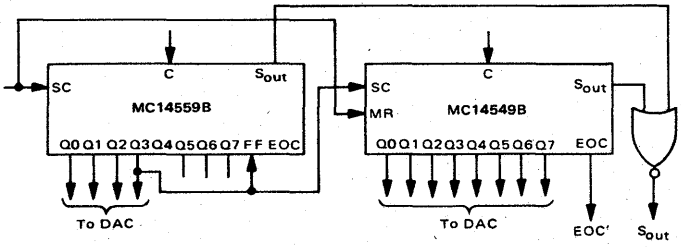
Additional Motorola Parts for Successive Approximation ADC

Monolithic digital-to-analog converters – The MC1408/1508 converter has eight-bit resolution and is available with 6, 7, and 8-bit accuracy. **The amplifier-comparator block** – The MC1407/1507 contains a high speed operational amplifier and a high speed comparator with adjustable window.

With these two linear parts it is possible to construct SA-ADCs with an accuracy of up to eight bits, using as the register one MC14549B or one MC14559B. An additional CMOS block will be necessary to generate the clock frequency.

Additional information on successive approximation ADC is found in Motorola Application Note AN-716.

FIGURE 5 – EXTERNALLY CONTROLLED 12-BIT ADC



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MCM14552

McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (64 x 4) STATIC RANDOM ACCESS MEMORY

256-BIT STATIC RANDOM ACCESS MEMORY

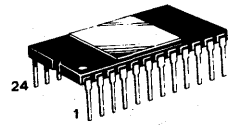
The MCM14552 is a static random access memory (RAM) organized in a 64 x 4 bit pattern. The three chip enable inputs can be used as extensions of the six address inputs, creating 9-bit address scheme. Eight MCM14552 devices may be used to comprise a 2048-bit memory (512 x 4) without additional address decoding.

The mode control (M) is used to change the control logic characteristic of the circuit. For example, with M high, the 3-state input (T) fully controls the 3-state characteristic of the output. With M low, the output 3-state characteristic is controlled by chip enable inputs (CE), write enable input (WE) and T. The latch enable (LE) input provides flexibility for holding output data unchanged during write operations as well as increasing the outputting of paired words.

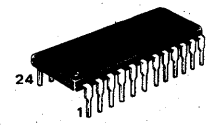
The memory is designed so that dc signals may operate the memory, with no maximum pulse width restrictions.

Medium speed, micropower operation, and control flexibility make the device useful in scratch pad or buffer applications where battery operation or high noise immunity are required.

- Quiescent Current = 50 μA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- 3-state Output Capability for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 716



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MCM14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

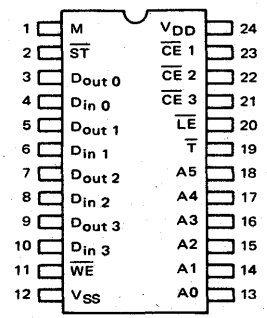
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN ASSIGNMENT



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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±1.0	–	±0.00001	±1.0	–	±14.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.050	5.0	–	150	µAdc
		10	–	10	–	0.100	10	–	300	
		15	–	20	–	0.150	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.050	50	–	375	µAdc
		10	–	100	–	0.100	100	–	750	
		15	–	200	–	0.150	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.98 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.96 µA/kHz) f + I_{DD}							
		15	I_T = (5.86 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	1	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns			5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns			10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns			15	65	110	160	
Output Fall Time	1	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns			5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns			10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns			15	37	55	80	
Read Cycle Time	1,2	$t_{cyc(R)}$	5.0	2000	3000	6000	ns
			10	750	1100	2200	
			15	500	825	1650	
Write Cycle Time	3,4	$t_{cyc(W)}$	5.0	1200	1800	3600	ns
			10	750	1100	2200	
			15	500	825	1650	
Address to $\overline{\text{Strobe}}$ Setup Time	1,3	$t_{setup(A\text{-}\overline{ST})}$	5.0	500	750	1500	ns
			10	150	225	450	
			15	120	170	350	
$\overline{\text{Strobe}}$ to Address Hold Time	1,3	$t_{hold(\overline{ST}\text{-}A)}$	5.0	50	75	150	ns
			10	0	35	100	
			15	0	25	75	
Address to $\overline{\text{Chip Enable}}$ Setup Time	2,4	$t_{setup(A\text{-}\overline{CE})}$	5.0	600	900	1800	ns
			10	200	300	600	
			15	150	225	450	
$\overline{\text{Chip Enable}}$ to Address Hold Time	2,4	$t_{hold(\overline{CE}\text{-}A)}$	5.0	150	225	450	ns
			10	100	150	300	
			15	75	120	225	
$\overline{\text{Strobe}}$ or $\overline{\text{Chip Enable}}$ Pulse Width When Reading	1,2	PW(R)	5.0	450	900	1800	ns
			10	150	225	450	
			15	100	170	350	
$\overline{\text{Strobe}}$ or $\overline{\text{Chip Enable}}$ Pulse Width When Writing	3,4	PW(W)	5.0	1200	1800	3600	ns
			10	600	900	1800	
			15	400	675	1350	
Read Setup Time	1	$t_{setup(R)}$	5.0	-100	30	0	ns
			10	-40	10	0	
			15	-30	7.5	0	
Read Hold Time	1	$t_{hold(R)}$	5.0	180	360	540	ns
			10	60	180	240	
			15	45	140	180	
Data Setup Time	3,4	$t_{setup(D)}$	5.0	600	900	1800	ns
			10	200	300	600	
			15	150	225	450	
Data Hold Time	3,4	$t_{hold(D)}$	5.0	200	300	600	ns
			10	50	75	150	
			15	30	60	120	

*The formula given is for the typical characteristics only.

(continued)

5

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C) (continued)

Characteristic	Figure	Symbol	V_{DD} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
$\overline{\text{Write Enable}}$ Setup Time	3,4	$t_{setup}(\overline{WE})$	5.0 10 15	240 80 55	480 160 120	720 240 180	ns
$\overline{\text{Write Enable}}$ Hold Time	3,4	$t_{hold}(\overline{WE})$	5.0 10 15	50 20 15	100 40 30	150 60 45	ns
Read Access Time from $\overline{\text{Strobe}}$	1,3	$t_{acc}(R\text{-}\overline{ST})$	5.0 10 15	2000 700 350	3000 1050 800	6000 2100 1600	ns
Read Access Time from $\overline{\text{Chip Enable}}$	2	$t_{acc}(R\text{-}\overline{CE})$	5.0 10 15	2100 750 400	3150 1100 825	6300 2250 1700	ns
Output Enable/Disable Delay from $\overline{\text{Chip Enable}}$ or $\overline{\text{Write Enable}}$	2,4	$t_{R(\overline{CE})}$, $t_{R(\overline{WE})}$	5.0 10 15	400 200 150	600 400 300	1200 600 450	ns
$\overline{\text{Three-State}}$ Enable/Disable Output Delay	2	$t(\overline{T})$	5.0 10 15	400 160 120	600 240 180	1200 480 360	ns
$\overline{\text{Latch}}$ to Output Propagation Delay	1	$t_{\overline{LE}}$	5.0 10 15	500 200 150	750 300 225	1500 600 450	ns

*The formula given is for the typical characteristics only.

5

LOGIC DIAGRAM

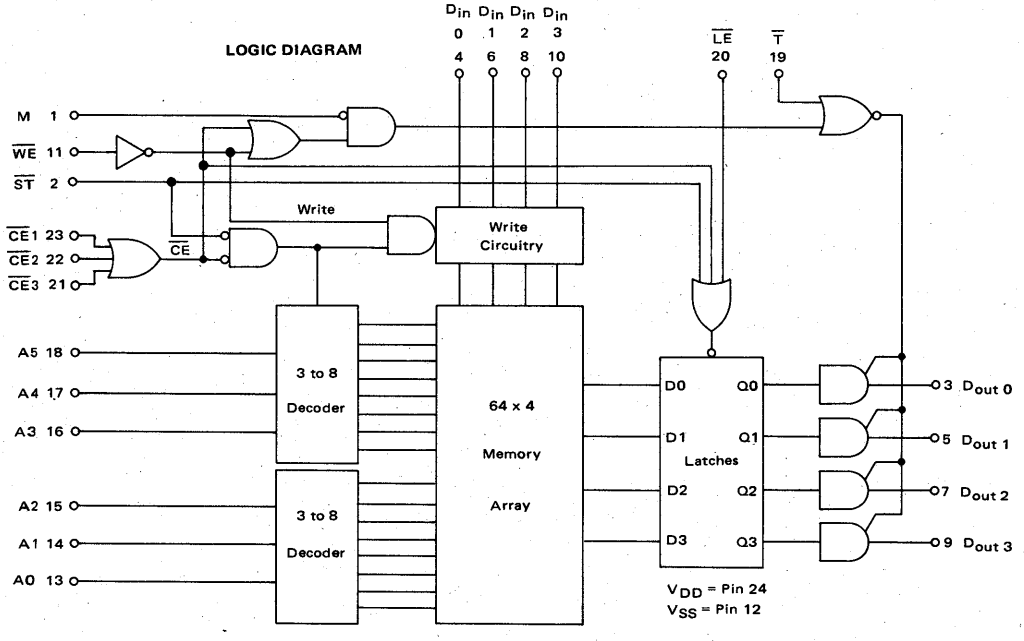
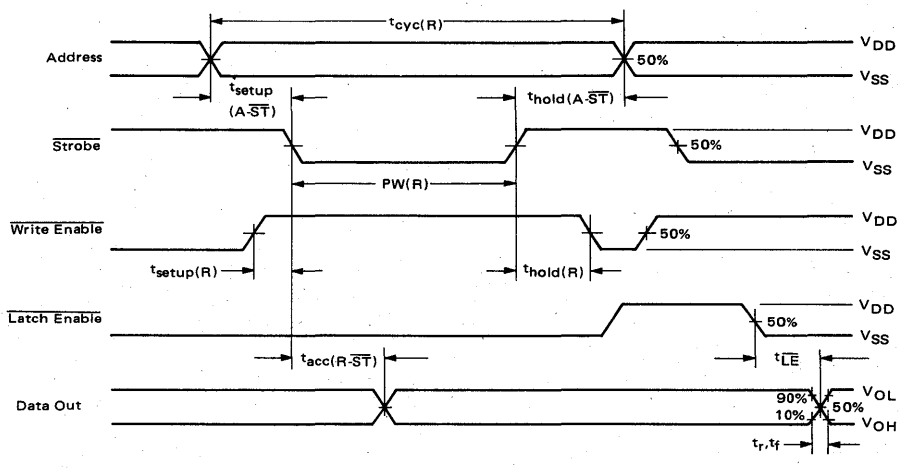


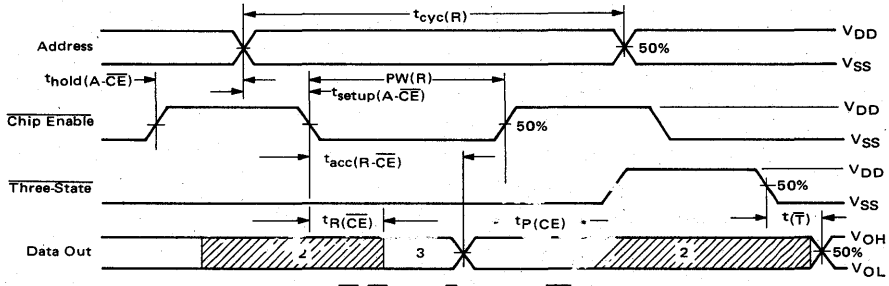
FIGURE 1 – READ CYCLE WAVEFORMS UTILIZING STROBE TO ACCESS MEMORY



Notes: 1 – $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and $\overline{T}$ are low, M is high.
2 – $\overline{WE}$ may be held high during the complete read cycle.

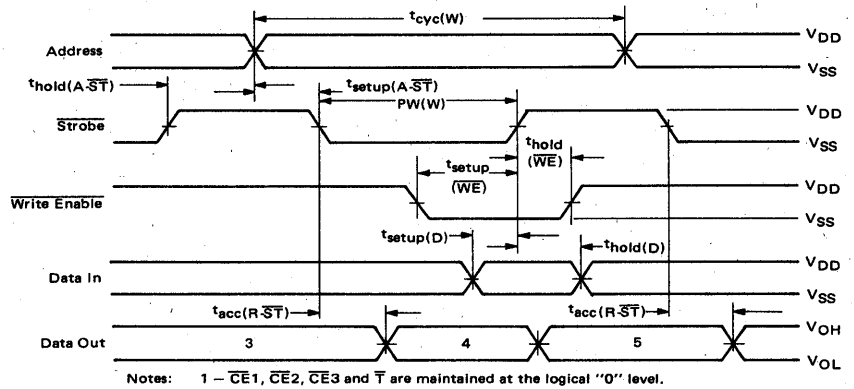
5

FIGURE 2 – READ CYCLE WAVEFORMS UTILIZING CHIP ENABLE TO ACCESS MEMORY



Notes: 1 – Unused $\overline{CE}$, $\overline{ST}$, M and $\overline{T}$ are low and $\overline{WE}$ is high.
2 – High impedance output state occurs when any $\overline{CE}$ is high and M is low, or when $\overline{T}$ is high.
3 – The output displays data from the previous state.
4 – PW(R) $\geq t_{acc(R\text{-}\overline{CE})max}$.

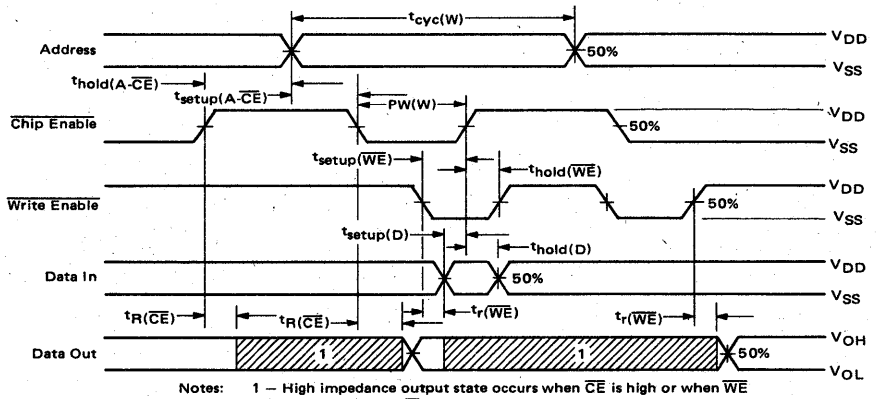
FIGURE 3 – WRITE CYCLE WAVEFORMS UTILIZING STROBE



Notes:
1 – $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and $\overline{T}$ are maintained at the logical "0" level.
2 – M is maintained at the logical "1" level.
3 – The output displays the contents of the previous state.
4 – The output displays the contents of the presently addressed location as in a read modify write cycle.
5 – The output displays the data that was written into addressed location.

5

FIGURE 4 – WRITE CYCLE WAVEFORM UTILIZING CHIP ENABLE



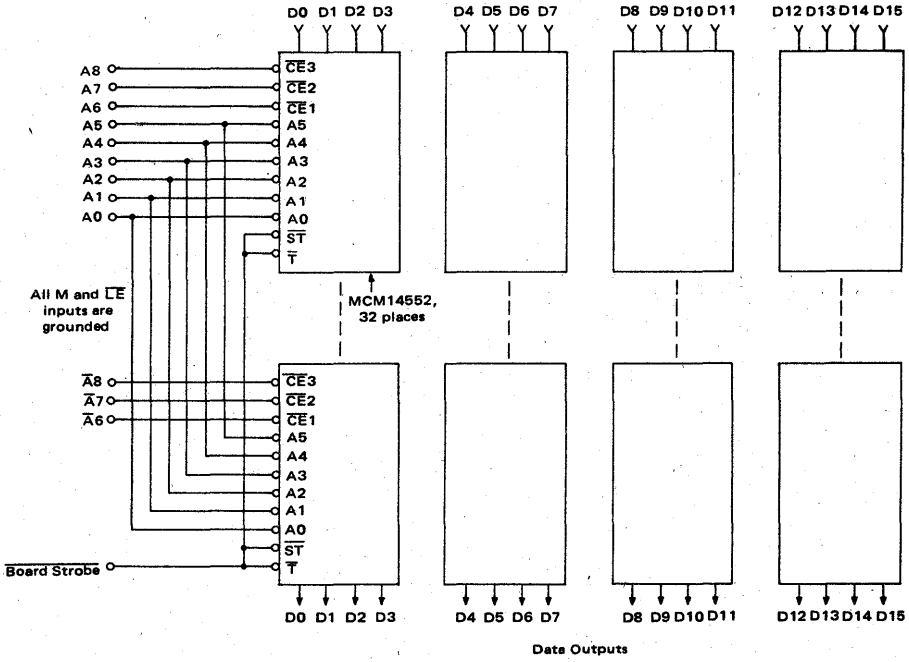
Notes:
1 – High impedance output state occurs when $\overline{CE}$ is high or when $\overline{WE}$ is low, for M and $\overline{T}$ maintained in the low state.
2 – Unused $\overline{CE}$'s, $\overline{ST}$, M and $\overline{T}$ are maintained at the logical "0" level.

TRUTH TABLE

Function	$\overline{CE}$ 1	$\overline{CE}$ 2	$\overline{CE}$ 3	$\overline{T}$	$\overline{LE}$	M	$\overline{ST}$	$\overline{WE}$	D_{in}	D_{out}	Comments
Address Changing Valid	X	X	X	X	X	X	1	X	X	R/A	D_{out} will be active if all $\overline{CE}$ = 0, $\overline{T}$ = 0 and $\overline{WE}$ = 1 or if M = 1 and $\overline{T}$ = 0
	X	1	X	X	X	X	X	X	X	R/A	
	X	X	1	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
Address Changing Not Valid	0	0	0	X	X	X	0	X	X	R/A	D_{out} will be active if $\overline{T}$ = 0 and $\overline{WE}$ = 1 or if M = 1 and $\overline{T}$ = 0
D_{out} Disabled (in high resistance state)	X	X	1	X	X	0	X	X	X	R	Disables write circuitry
	X	1	X	X	X	0	X	X	X	R	
	1	X	X	X	X	0	X	X	X	R	
	X	X	X	1	X	X	X	X	X	R	$\overline{T}$ = 1 always disables D_{out}
	X	X	X	X	X	0	X	0	X	R	M = 0 and write operation disables D_{out}
D_{out} Enabled (in active state)	0	0	0	0	X	X	X	1	X	A	Read operation, D_{out} active
	X	X	X	0	X	1	X	X	X	A	Read or write, D_{out} active
Read Addressed Memory Location Into Output Latch	0	0	0	X	0	X	0	X	X	R/A	If $\overline{WE}$ = 0, D_{in} = D_{out}
Disable Reading From Memory	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	
	X	X	X	X	X	X	X	0	X	R/A	
Write Into Memory	0	0	0	X	X	X	0	0	A	R/A	
Write Disabled	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	
	X	X	X	X	X	X	X	1	X	R/A	
Output Latch Enabled	0	0	0	X	0	X	0	X	X	R/A	
Output Latch Disabled	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	1	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	

R = High resistance state at D_{out}.
A = An active level of either V_{DD} or V_{SS}.
R/A = An R or A condition depending on the don't care condition.
X = Don't care condition (must be in the "1" or "0" state).
1 = A high level at V_{DD}.
0 = A low level at V_{SS}.

FIGURE 5 – 512 WORD x 16 BIT MEMORY BOARD



MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14553B

McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

THREE-DIGIT BCD COUNTER

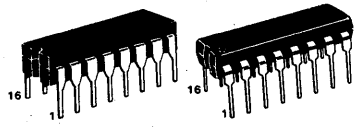
THREE-DIGIT BCD COUNTER

The MC14553B three-digit BCD counter consists of three negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on-chip oscillator provides the low-frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

- TTL Outputs
- On-Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

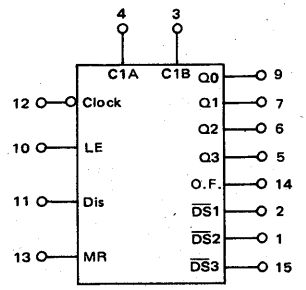
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
DC Current per Pin, All Outputs	I	20	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUTS				
MASTER RESET	CLOCK	DISABLE	LE	OUTPUTS
0	⎍	0	0	No Change
0	⎍	0	0	Advance
0	X	1	X	No Change
0	1	⎍	0	Advance
0	1	⎍	0	No Change
0	0	X	X	No Change
0	X	X	⎍	Latched
0	X	X	1	Latched
1	X	X	0	Q0 = Q1 = Q2 = Q3 = 0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 4.6 Vdc) Source		5.0	-0.25	–	-0.20	-0.36	–	-0.7	–	
(V_{OH} = 9.5 Vdc)		10	−0.62	–	−0.50	−0.9	–	−0.35	–	
(V_{OH} = 13.5 Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	
(V_{OL} = 0.4 Vdc) Sink-Pin 3	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
(V_{OL} = 0.4 Vdc) Sink-Other Outputs	I_{OL}	5.0	3.0	–	2.5	4.0	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	6.2	–	5.0	8.0	–	3.5	–	
(V_{OL} = 1.5 Vdc)		15	19	–	15	20	–	10	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 4.6 Vdc) Source		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink-Pin 3	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
(V_{OL} = 0.4 Vdc) Sink-Other Outputs	I_{OL}	5.0	2.4	–	2.0	4.0	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	3.8	–	3.0	8.0	–	2.5	–	
(V_{OL} = 1.5 Vdc)		15	10	–	8.4	20	–	7.0	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.35 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.85 µA/kHz) f + I_{DD}							
		15	I_T = (1.50 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	3a	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns			5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns			10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns			15	–	–	65	110	160	
Output Fall Time	3a	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns			5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns			10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns			15	–	–	37	55	80	
Clock to BCD Out	3a	t_{PLH}, t_{PHL}	5.0	–	–	900	1500	2000	ns
			10	–	–	500	800	1000	
			15	–	–	300	600	750	
Clock to Overflow	3a	t_{PHL}	5.0	–	–	600	1000	1300	ns
			10	–	–	400	600	800	
			15	–	–	200	450	600	
Reset to BCD Out	3b	t_{PHL}	5.0	–	–	900	1300	2000	ns
			10	–	–	500	700	1000	
			15	–	–	300	525	750	
Clock to Latch Enable Setup Time	3b	t_{setup}	5.0	–	–	300	700	900	ns
			10	–	–	200	350	500	
			15	–	–	100	265	375	
Minimum Clock Pulse Width	3a	PW_C	5.0	–	–	275	410	550	ns
			10	–	–	100	150	200	
			15	–	–	75	110	150	
Minimum Reset Pulse Width	3b	PW_R	5.0	–	–	200	400	600	ns
			10	–	–	125	200	300	
			15	–	–	75	150	225	
Input Clock Frequency	3a	f_C	5.0	0.9	0.7	1.5	–	–	MHz
			10	2.5	2.0	5.0	–	–	
			15	3.5	2.5	7.0	–	–	
Input Clock Rise Time	3b	t_r	5.0	–	–	–	No Limit	No Limit	ns
			10	–	–	–			
			15	–	–	–			
Scan Oscillator Frequency	2	f_{osc}	5.0	–	–	0.4/C1	–	–	Hz/μF
			10	–	–	1.2/C1	–	–	
			15	–	–	1.6/C1	–	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – AMBIENT TEMPERATURE POWER DERATING

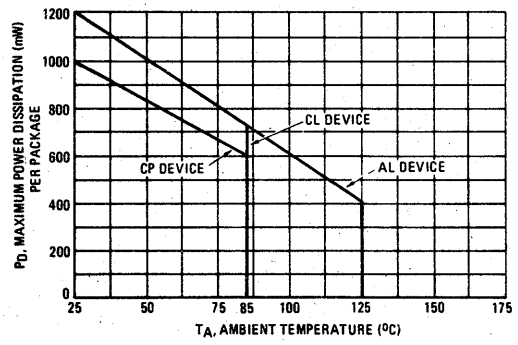


FIGURE 2 – 3-DIGIT COUNTER TIMING DIAGRAM (Reference Figure 4)

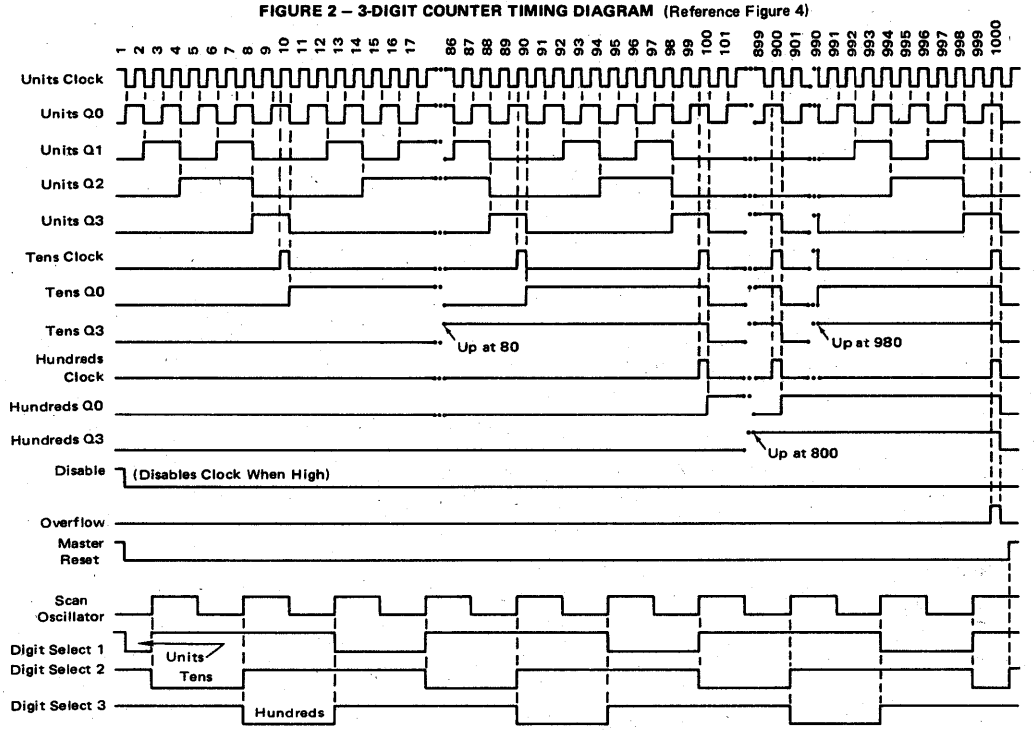
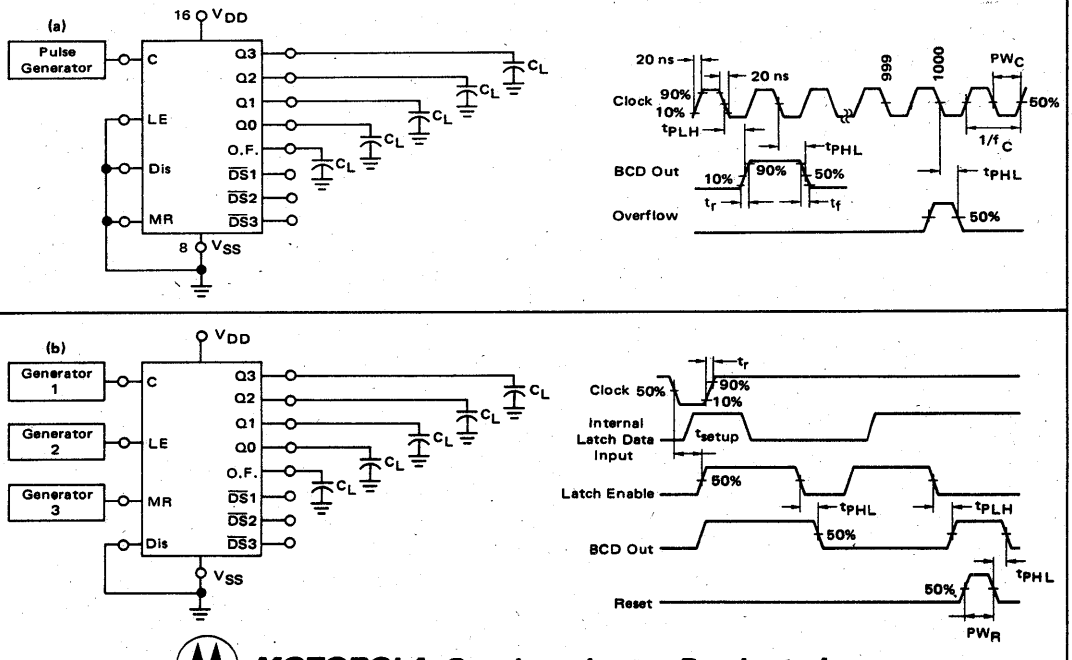


FIGURE 3 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



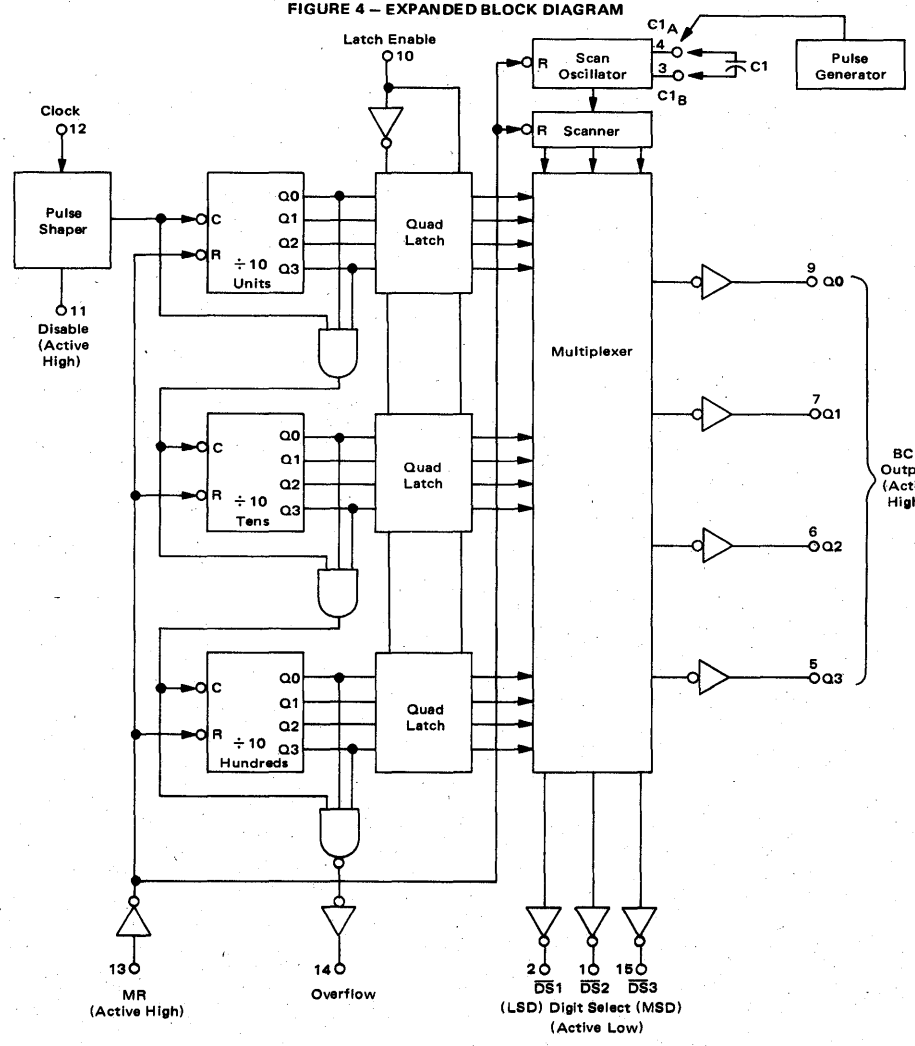
OPERATING CHARACTERISTICS

The MC14553B three-digit counter, shown in Figure 4, consists of three negative edge-triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active high), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active low) are provided for display control. All outputs are TTL compatible.

An on-chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. The frequency of the oscillator can be controlled externally by a capacitor between pins 3 and 4, or it can be overridden and driven with an external clock at pin 4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

The Master Reset input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit. While Master Reset is high the digit scanner is set to digit one; but all three digit select outputs are disabled to prolong display life, and the scan oscillator is inhibited. The Disable input, when high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times. Information present in the counters when the latch input goes high, will be stored in the latches and will be retained while the latch is high, independent of other inputs. Information can be recovered from the latches after the counters have been reset if Latch Enable remains high during the entire reset cycle.

FIGURE 4 – EXPANDED BLOCK DIAGRAM



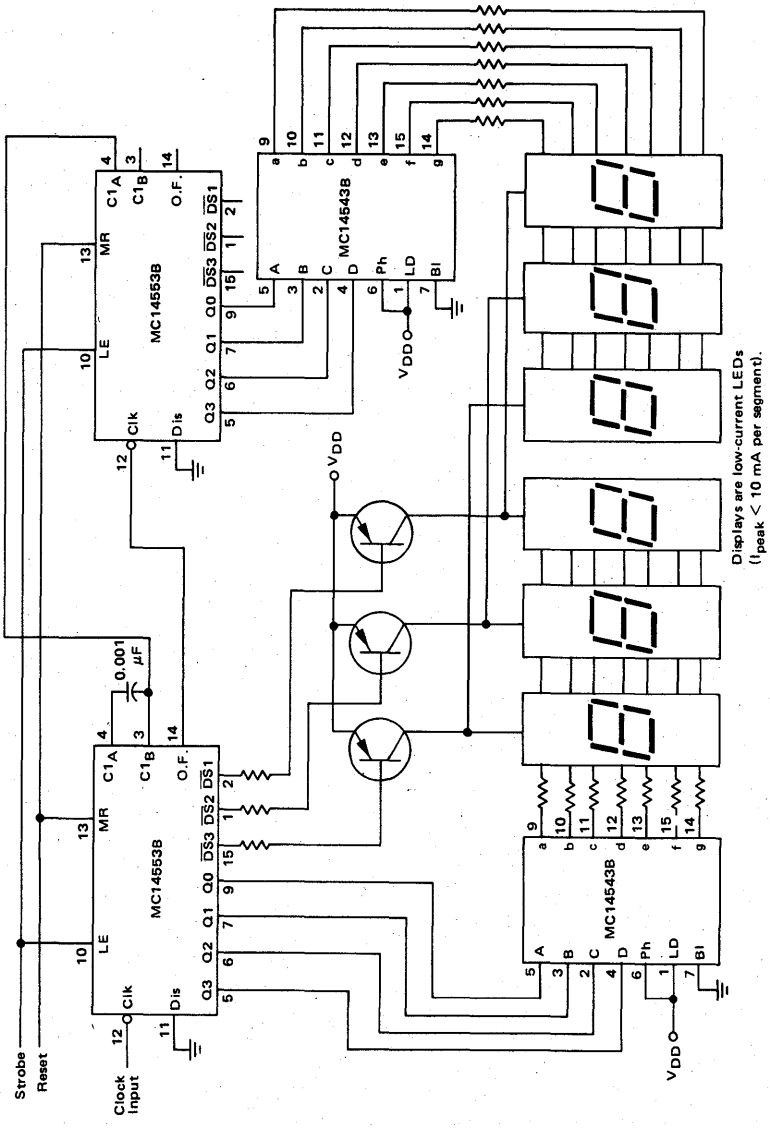


FIGURE 5 – SIX-DIGIT DISPLAY

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14554B

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

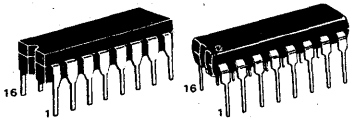
2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER

2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER

The MC14554B 2 x 2-bit parallel binary multiplier is constructed with complementary MOS (CMOS) enhancement mode devices. The multiplier can perform the multiplication of two binary numbers and simultaneously add two other binary numbers to the product. The MC14554B has two multiplicand inputs (X0 and X1), two multiplier inputs (Y0 and Y1), five cascading or adding inputs (K0, K1, M0, M1, and M2), and five sum and carry outputs (S0, S1, S2, C1 [S3], and C0). The basic multiplier can be expanded into a straightforward m-bit by n-bit parallel multiplier without additional logic elements.

Application areas include arithmetic processing (multiplying/adding, obtaining square roots, polynomial evaluation, obtaining reciprocals, and dividing), Fast Fourier Transform processing, digital filtering, communications (convoluation and correlation), and process and machine controls.

- Diode Protection on All Inputs
- All Outputs Buffered
- Quiescent Current = 5.0 nA typical @ 5 Vdc
- Straight-forward m-Bit By n-Bit Expansion
- No Additional Logic Elements Needed for Expansion
- Multiplies and Adds Simultaneously
- Positive Logic Design
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

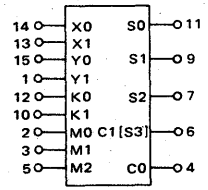
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

EQUATIONS

$S = (X \times Y) + K + M$

Where:
x Means Arithmetic Times.
+ Means Arithmetic Plus.
S = S3 S2 S1 S0, X = X1X0, Y = Y1Y0,
K = K1 K0, M = M1 M0 (Binary Numbers).

Example:

Given: X = 2(10), Y = 3(11)
K = 1(01), M = 2(10)

Then: S = (2 x 3) + 1 + 2 = 9
S = (10 x 11) + 01 + 10 = 1001

Note: C0 connected to M2 for this size multiplier.
See general expansion diagram for other size multipliers.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.0 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.0 µA/kHz) f + I_{DD}							
		15	I_T = (3.0 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
K0 to C0						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 185 ns		5.0	270	430	675	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 82 ns		10	115	170	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 60 ns		15	85	130	215	
M0 to S2						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 595 ns		5.0	680	1250	1700	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 247 ns		10	280	500	750	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 185 ns		15	210	380	570	

*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION WAVEFORMS

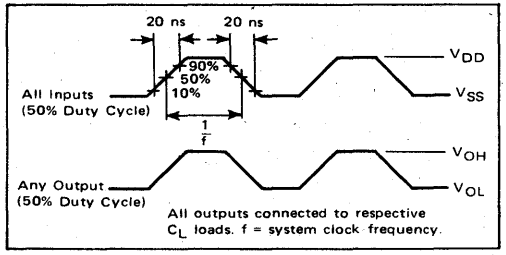
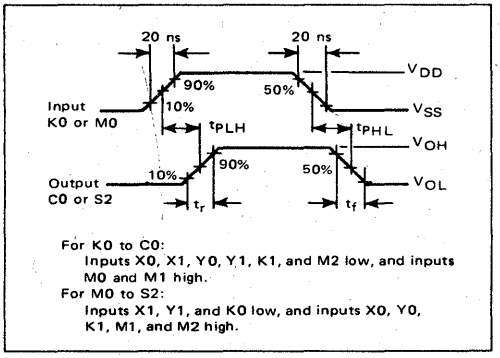
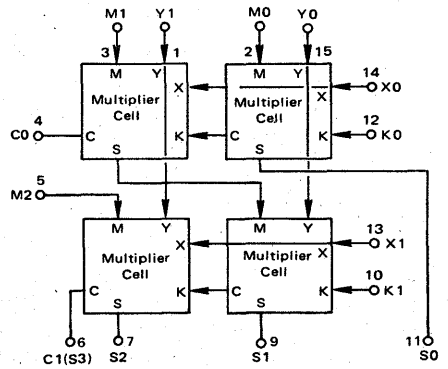


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS

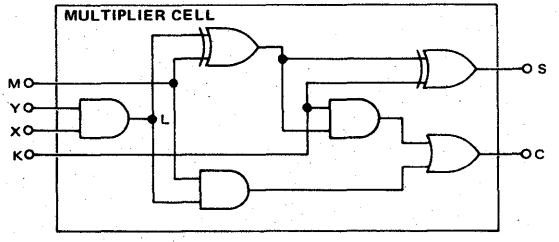


For K0 to C0:
Inputs X0, X1, Y0, Y1, K1, and M2 low, and inputs M0 and M1 high.
For M0 to S2:
Inputs X1, Y1, and K0 low, and inputs X0, Y0, K1, M1, and M2 high.

LOGIC DIAGRAM

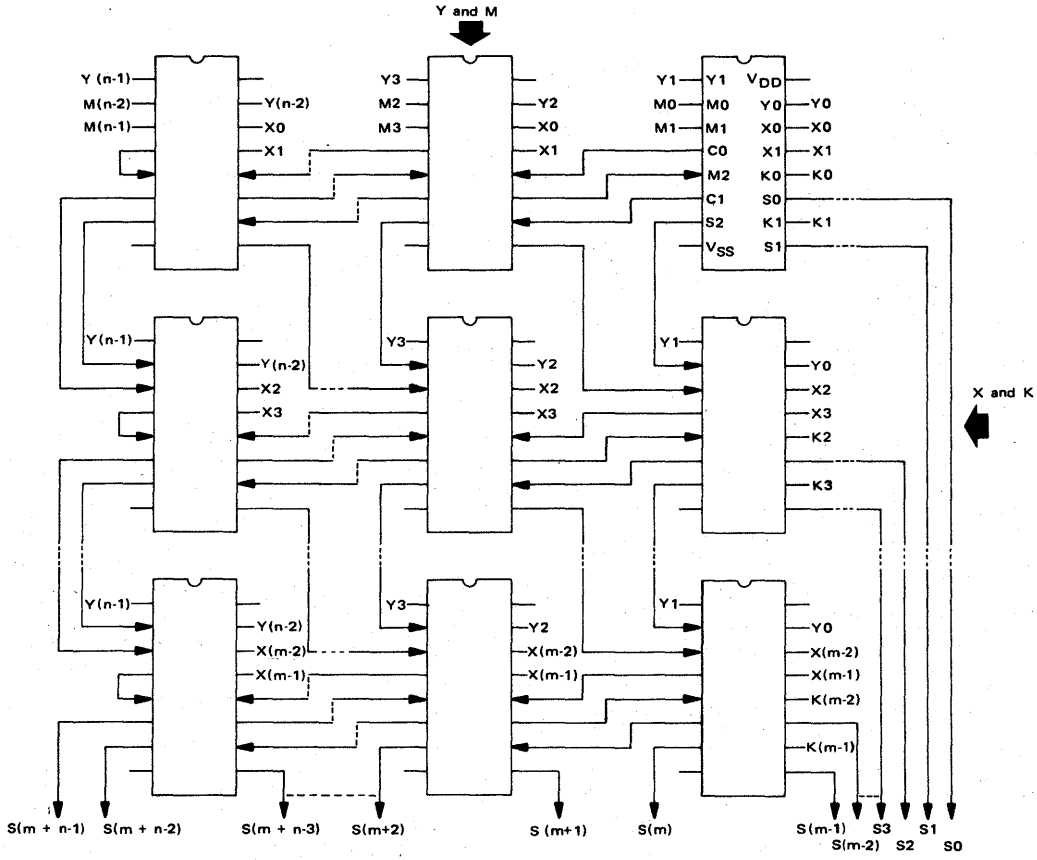


MULTIPLIER CELL



EXPANSION DIAGRAM

m-Bit by n-Bit Parallel Binary Multiplier (Top View)



S = (X x Y) + K + M Where: x means Arithmetic Times.
+ means Arithmetic Plus.

S = S(m + n-1) S(m + n-2) - - - S2 S1 S0
X = X(m-1) X (m-2) - - - X2 X1 X0, Y = Y(n-1) Y(n-2) - - - Y2 Y1 Y0
K = K(m-1) K(m-2) - - - K2 K1 K0 and M = M(n-1) M(n-2) - - - M2 M1 M0
(Binary Numbers).

Number of output binary digits = m + n
Number of packages = mxn/4 (For m or n or both odd select next highest even number.)

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14555B
MC14556B

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

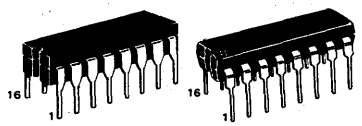
Active High Outputs – MC14555B
Active Low Outputs – MC14556B

DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the "high" state, and the MC14556B has the selected output go to the "low" state. Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other MC14555B or MC14556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Active High or Active Low Outputs
- Low Quiescent Current – 5.0 nA/package typical @ 5 Vdc
- Expandable
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

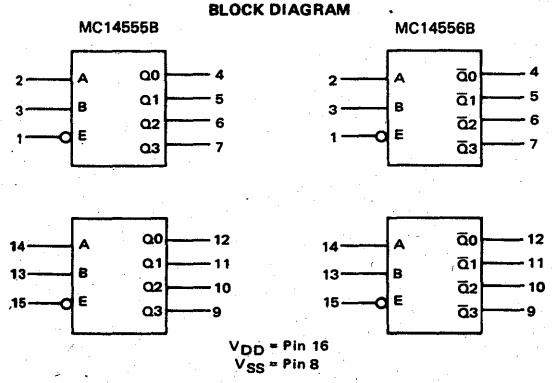
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS			OUTPUTS MC14555B				OUTPUTS MC14556B			
ENABLE	SELECT									
$\overline{E}$	B	A	Q3	Q2	Q1	Q0	$\overline{Q3}$	$\overline{Q2}$	$\overline{Q1}$	$\overline{Q0}$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.85 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.7 μA/kHz) f + I_{DD}							
		15	I_T = (2.6 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max All Types	Unit
Output Rise Time	t_r				ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	360	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	130	
Output Fall Time	t_f				ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	80	
Propagation Delay Time — A, B to Output	t_{PLH}, t_{PHL}				ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns		5.0	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 62 ns		10	95	190	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	70	140	
Propagation Delay Time — E to Output	t_{PLH}, t_{PHL}				ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 115 ns		5.0	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 52 ns		10	85	170	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 40 ns		15	65	130	

*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

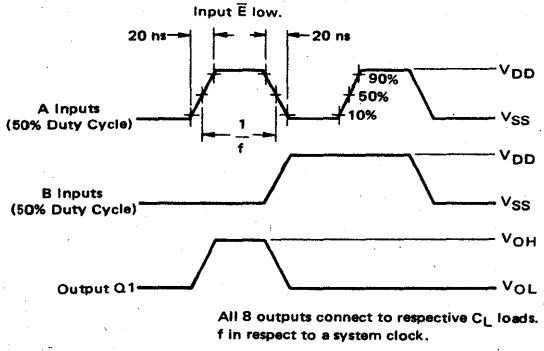
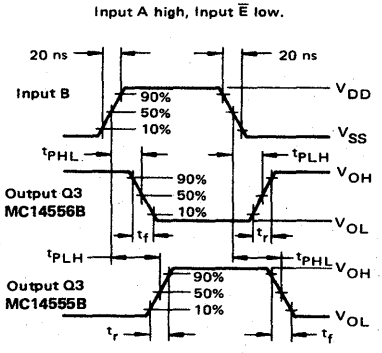
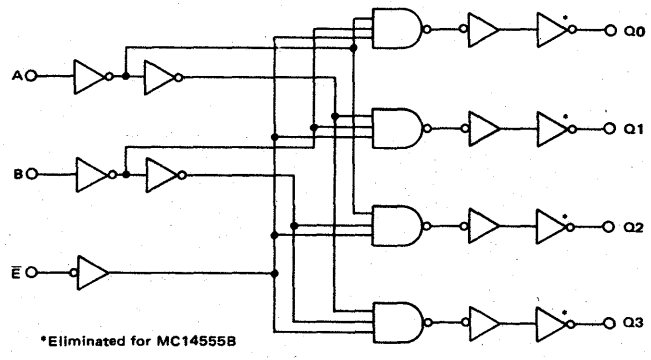


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



LOGIC DIAGRAM
(1/2 of Dual)



MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14557B

1-TO-64 BIT VARIABLE LENGTH SHIFT REGISTER

The MC14557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable (CE) input is provided to allow gating of the clock or negative edge clocking capability.

The device can be effectively used for variable digital delay lines or simply to implement odd length shift registers. characteristics can be found on the Family Data Sheet.

- Quiescent Current = 10 nA/package typical @ 5 Vdc
- 1-64 Bit Programmable Length
- Q and $\overline{Q}$ Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- 8 MHz Operation @ V_{DD} = 10 Vdc Typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LENGTH SELECT TRUTH TABLE

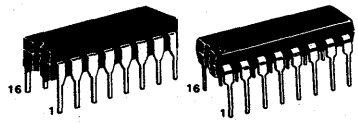
L32	L16	L8	L4	L2	L1	Register Length
0	0	0	0	0	0	1-Bit
0	0	0	0	0	1	2-Bits
0	0	0	0	1	0	3-Bits
0	0	0	0	1	1	4-Bits
0	0	0	1	0	0	5-Bits
0	0	0	1	0	1	6-Bits
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	0	0	0	0	0	33-Bits
1	0	0	0	0	1	34-Bits
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	0	0	61-Bits
1	1	1	1	0	1	62-Bits
1	1	1	1	1	0	63-Bits
1	1	1	1	1	1	64-Bits

Note: Length equals the sum of the binary length control subscripts plus one.

McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

1-TO-64 BIT
VARIABLE LENGTH
SHIFT REGISTER



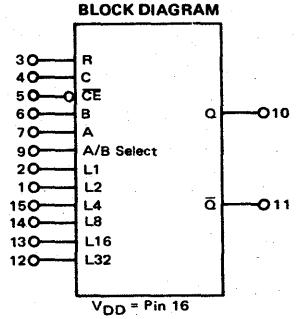
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

Inputs				Output
R	A/B	Clock	$\overline{CE}$	Q
0	0	↓	0	B
0	1	↓	0	A
0	0	1	↓	B
0	1	1	↓	A
1	X	X	X	0

Q is the output of the first selected shift register stage.
X = Don't Care.

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	μAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.75 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.5 μA/kHz) f + I_{DD}							
		15	I_T = (5.25 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Minimum No. of Bits Selected	Typical Setup Time B → $\overline{CE}$ ns	Length Select Lines = 1
1	180	None
2	120	L1
3	90	L2
5	60	L4
9	30	L8
17	0	L16
33	-30	L32

SETUP TIME CHART

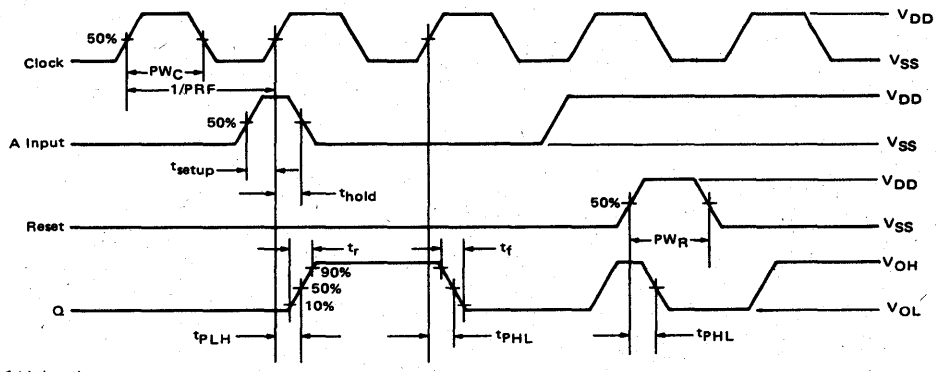
The nature of the length select logic causes the setup time to vary with the number of bits selected. The following table summarizes the typical variation at V_{DD} = 10 V, T_A = 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	100	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}							ns
(C or $\overline{CE}$ to Q or $\overline{Q}$)								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	–	500	750	1250	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 167 ns		10	–	–	200	300	500	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	–	150	225	375	
(R to Q or $\overline{Q}$)								ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 390 ns		5.0	–	–	475	715	1190	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 157 ns		10	–	–	190	285	475	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 115 ns		15	–	–	140	210	350	
Minimum Clock Pulse Width	PW_C	5.0	–	–	220	330	660	ns
		10	–	–	68	100	200	
		15	–	–	50	75	150	
Minimum Reset Pulse Width	PW_R	5.0	–	–	300	450	900	ns
		10	–	–	90	135	270	
		15	–	–	60	90	180	
Maximum Clock Pulse Frequency	PRF	5.0	1.7	0.83	2.5	–	–	MHz
		10	5.0	2.7	8.0	–	–	
		15	6.7	3.3	10.5	–	–	
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0	No Limit	No Limit	–	–	–	–
		10			–	–	–	
		15			–	–	–	
Data to Clock Setup Time (A or B to C or $\overline{CE}$) L1, L2, L4, L8, L16, L32 = 0	t_{setup}	5.0	–	–	450	675	1350	ns
		10	–	–	180	270	540	
		15	–	–	135	200	400	
Data to Clock Hold Time (A or B to C or $\overline{CE}$) L1, L2, L4, L8, L16, L32 = 0	t_{hold}	5.0	–	–	−450	−300	−150	ns
		10	–	–	−180	−120	−60	
		15	–	–	−135	−90	−45	

*The formula given is for the typical characteristics only.

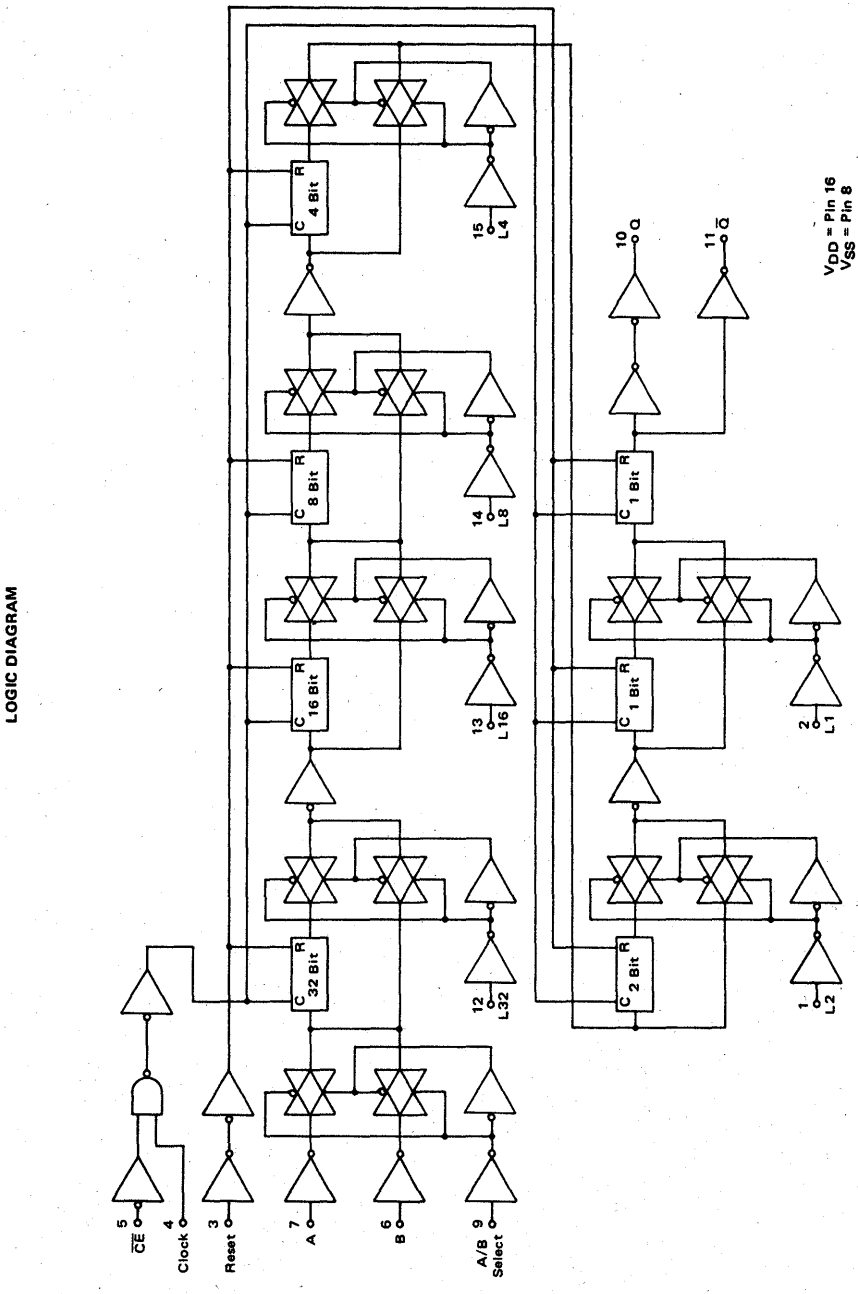
TIMING DIAGRAM



1-bit length:
$\overline{CE}$ = 0
A/B = 1
L1 = L2 = L4 = L8 = L16 = L32 = 0

5

LOGIC DIAGRAM



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MC14558B

BCD-TO-SEVEN SEGMENT DECODER

The MC14558B decodes 4-bit binary coded decimal data dependent on the state of auxiliary inputs, Enable and RBI, and provides an active high seven-segment output for a display driver.

An auxiliary input truth table is shown, in addition to the BCD to seven-segment truth table, to indicate the functions available with the two auxiliary inputs.

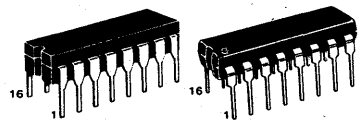
Leading Zero blanking is easily obtained with an external flip-flop in time division multiplexed systems displaying most significant decade first.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Segment Blanking for All Illegal Input Combinations
- Lamp Test Function
- Capability for Suppression of Non-Significant Zeros
- Lamp Intensity Function
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN
SEGMENT DECODER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

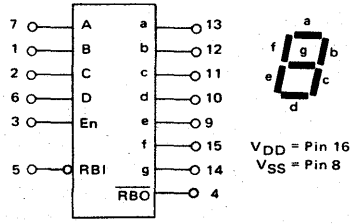
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

5

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM

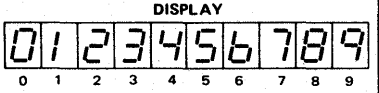


AUXILIARY INPUT TRUTH TABLE

Enable Pin 3	RBI Pin 5	BCD Input Code	RBO Pin 4	Function Performed
0	0	X	0	Lamp Test
0	1	X	1	Blank Segments
1	1	0	1	Display Zero
1	0	0	0	Blank Segments
1	X	1-9	1	1-9 Displayed

X = Don't Care
RBI = Ripple Blanking Input
RBO = Ripple Blanking Output

DISPLAY



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.2 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.4 μA/kHz) f + I_{DD}							
		15	I_T = (3.6 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C; see Figure 1)

Characteristic	Symbol	V_{DD}	Typ All Types	Maximum AL Device	Maximum CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 495 ns		5.0	580	1000	1500	
t_{PLH} = (0.66 ns/pF) C_L + 187 ns		10	220	400	600	
t_{PLH} = (0.5 ns/pF) C_L + 120 ns		15	145	300	450	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 695 ns		5.0	780	1500	2200	
t_{PHL} = (0.66 ns/pF) C_L + 242 ns		10	275	500	750	
t_{PHL} = (0.5 ns/pF) C_L + 160 ns		15	185	375	565	

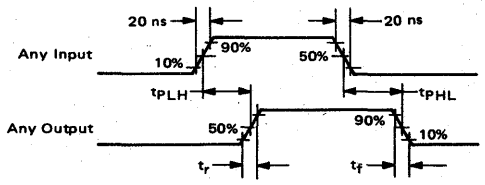
*The formula given is for the typical characteristics only.

TRUTH TABLE

INPUTS						OUTPUTS*								
En Pin 3	$\overline{RBI}$ Pin 5	D Pin 6	C Pin 2	B Pin 1	A Pin 7	a Pin 13	b Pin 12	c Pin 11	d Pin 10	e Pin 9	f Pin 15	g Pin 14	$\overline{RBO}$ Pin 4	DISPLAY
1	1	0	0	0	0	1	1	1	1	1	1	0	1	0
1	X	0	0	0	1	0	0	0	0	1	1	0	1	1
1	X	0	0	1	0	1	1	0	1	1	0	1	1	2
1	X	0	0	1	1	1	1	1	1	0	0	1	1	3
1	X	0	1	0	0	0	1	1	0	0	1	1	1	4
1	X	0	1	0	1	1	0	1	1	0	1	1	1	5
1	X	0	1	1	0	0	0	1	1	1	1	1	1	6
1	X	0	1	1	1	1	1	1	0	0	0	0	1	7
1	X	1	0	0	0	1	1	1	1	1	1	1	1	8
1	X	1	0	0	1	1	1	1	0	0	1	1	1	9
1	0	0	0	0	0	0	0	0	0	0	0	0	0	Blank
0	0	X	X	X	X	1	1	1	1	1	1	1	0	8
0	1	X	X	X	X	0	0	0	0	0	0	0	1	Blank

*All non-valid BCD input codes produce a blank display.
X = Don't Care

FIGURE 1 – SIGNAL WAVEFORMS



TYPICAL APPLICATIONS

FIGURE 2 – LEADING AND TRAILING ZERO SUPPRESSION WITH LAMP TEST

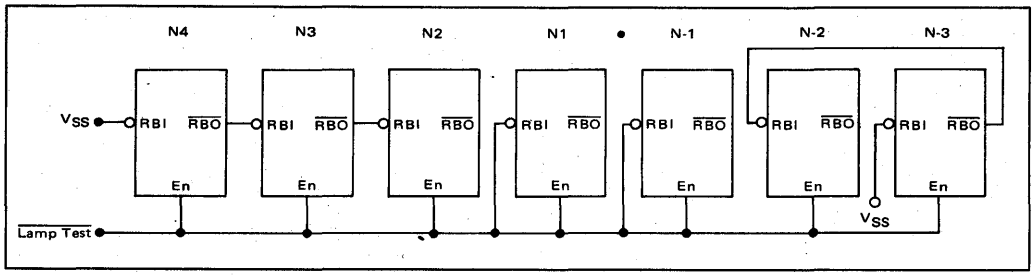


FIGURE 3 – LEADING AND TRAILING ZERO SUPPRESSION WITH PWM INTENSITY BLANKING AND NO LAMP TEST

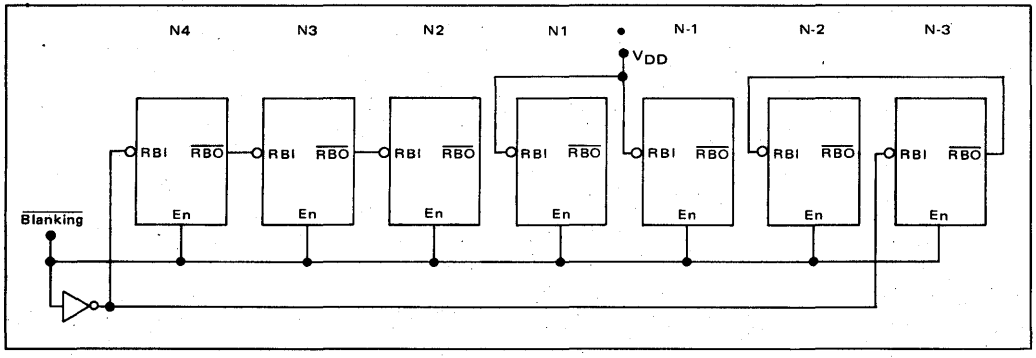
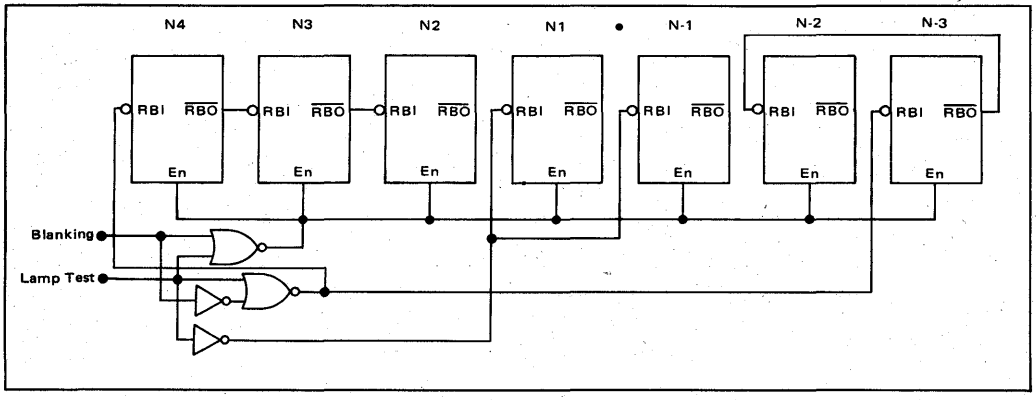
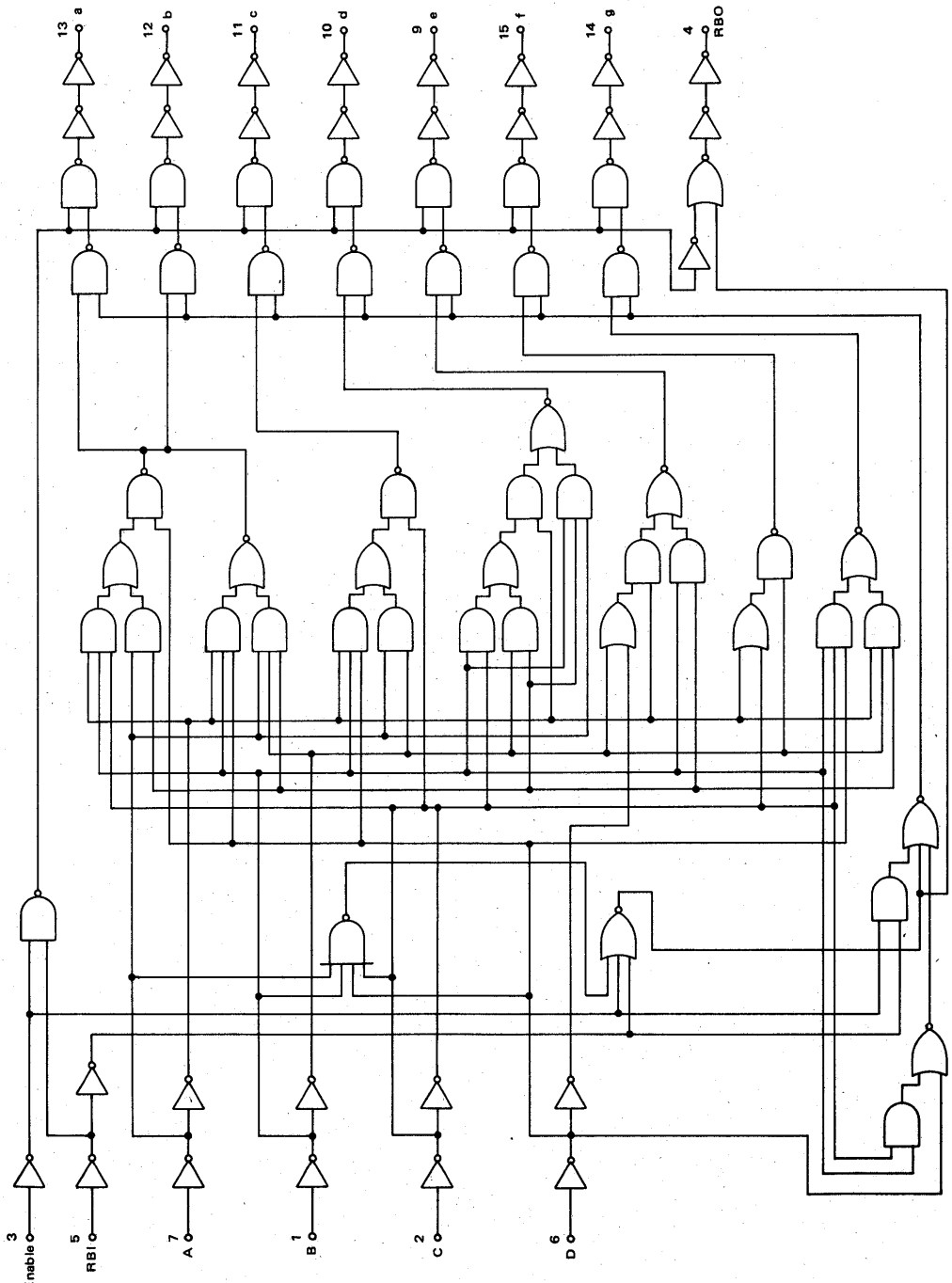


FIGURE 4 – ZERO SUPPRESSION WITH LAMP TEST AND INTENSITY BLANKING



5

LOGIC DIAGRAM



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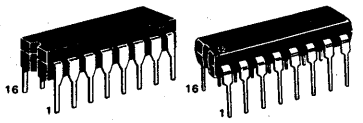
MC14559B

FOR COMPLETE DATA
SEE MC14549B

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

SUCCESSIVE APPROXIMATION REGISTERS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

SUCCESSIVE APPROXIMATION REGISTERS

The MC14549B and MC14559B successive approximation registers are 8-bit registers providing all the digital control and storage necessary for successive approximation analog-to-digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the MC14549B is required in the cascaded mode when greater than 8 bits are desired. The Feed Forward (FF) of the MC14559B is used for register shortening where End-of-Conversion (EOC) is required after less than eight cycles.

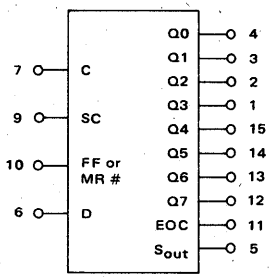
Applications for the MC14549B and MC14559B include finding square roots, division, ring counters, serial-to-parallel conversion, and analog-to-digital conversion.

- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable
- Compatible with a Variety of Digital and Analog Systems such as the MC1408 8-Bit D/A Converter
- All Control Inputs Positive-Edge Triggered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

#For MC14549B Pin 10 is MR input
For MC14559B Pin 10 is FF input

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLES

MC14549B

SC	$SC_{(t-1)}$	MR	$MR_{(t-1)}$	Clock	Action
X	X	X	X	⌐_	None
X	X	1	X	_⌐	Reset
1	0	0	0	_⌐	Start Conversion
1	X	0	1	_⌐	Start Conversion
1	1	0	0	_⌐	Continue Conversion
0	X	0	X	_⌐	Continue Previous Operation

MC14559B

SC	$SC_{(t-1)}$	EOC	Clock	Action
X	X	X	⌐_	None
1	0	0	_⌐	Start Conversion
X	1	0	_⌐	Continue Conversion
0	0	0	_⌐	Continue Conversion
0	X	1	_⌐	Retain Conversion Result
1	X	1	_⌐	Start Conversion

X = Don't Care
t-1 = State at Previous Clock _⌐

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

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MC14560B

NBCD ADDER

The MC14560B adds two 4-bit numbers in NBCD (natural binary coded decimal) format, resulting in sum and carry outputs in NBCD code.

This device can also subtract when one set of inputs is complemented with a 9's Complementer (MC14561B).

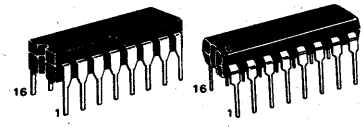
All inputs and outputs are active high. The carry input for the least significant digit is connected to V_{SS} for no carry in.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Single Supply Operation – Positive or Negative
- Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

NBCD ADDER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

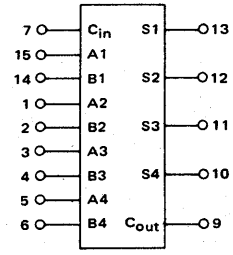
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE*

INPUT									OUTPUT				
A4	A3	A2	A1	B4	B3	B2	B1	C_{in}	C_{out}	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0	0	1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	1	0	1	0	0	1	1
0	1	1	0	1	0	0	0	0	1	0	1	0	0
1	0	0	1	1	0	0	1	1	1	1	0	0	1

*Partial truth table to show logic operation for representative input values.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.68 µA/kHz) f + I_Q I_{DD}							µAdc
		10	I_T = (3.35 µA/kHz) f + I_Q I_{DD}							
		15	I_T = (5.03 µA/kHz) f + I_Q I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$$

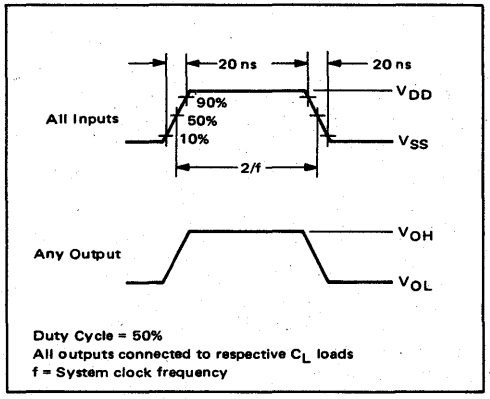
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
A or B to S						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns		5.0	750	1400	2100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 297 ns		10	330	600	900	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 195 ns		15	220	450	675	
A or B to C_{out}						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	650	1200	1800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	230	400	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	170	300	450	
C_{in} to C_{out}						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	550	1000	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 187 ns		10	220	400	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns		15	160	300	450	
Turn-Off Delay Time	t_{PLH}					ns
C_{in} to S						
t_{PLH} = (1.7 ns/pF) C_L + 715 ns		5.0	800	1500	2250	
t_{PLH} = (0.66 ns/pF) C_L + 317 ns		10	350	650	975	
t_{PLH} = (0.5 ns/pF) C_L + 215 ns		15	240	490	750	
Turn-On Delay Time	t_{PHL}					ns
C_{in} to S						
t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	650	1200	1800	
t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	230	400	600	
t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	170	300	450	

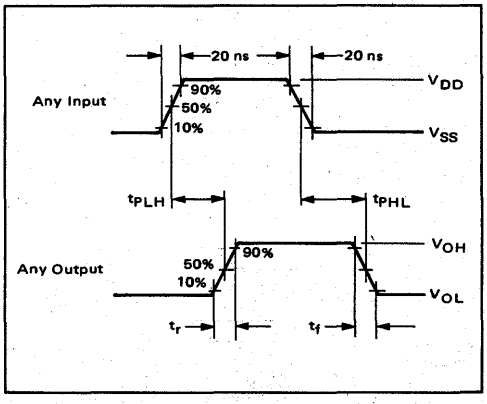
*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION WAVEFORMS



Duty Cycle = 50%
All outputs connected to respective C_L loads
f = System clock frequency

FIGURE 2 – SWITCHING TIME WAVEFORMS



5

FUNCTIONAL EQUIVALENT LOGIC DIAGRAM

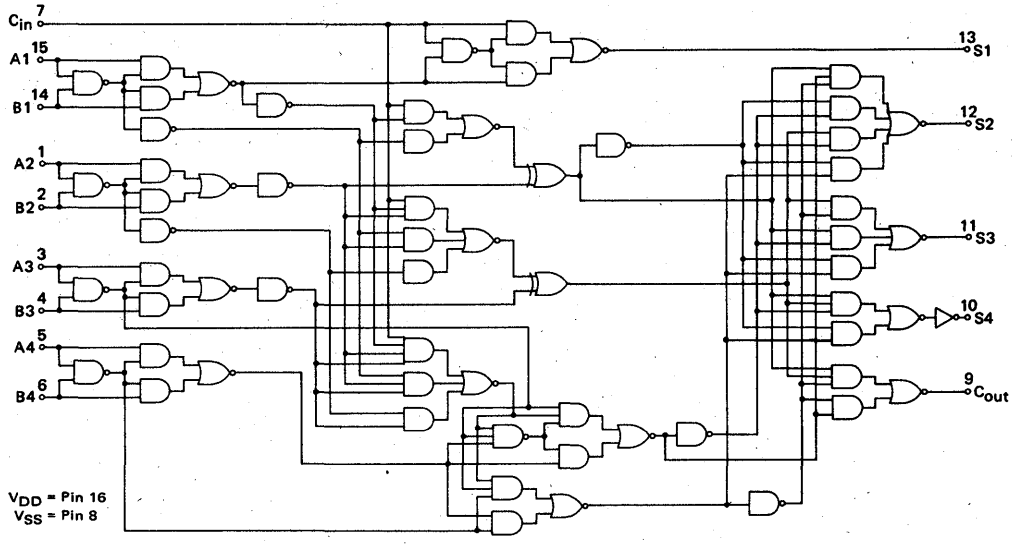
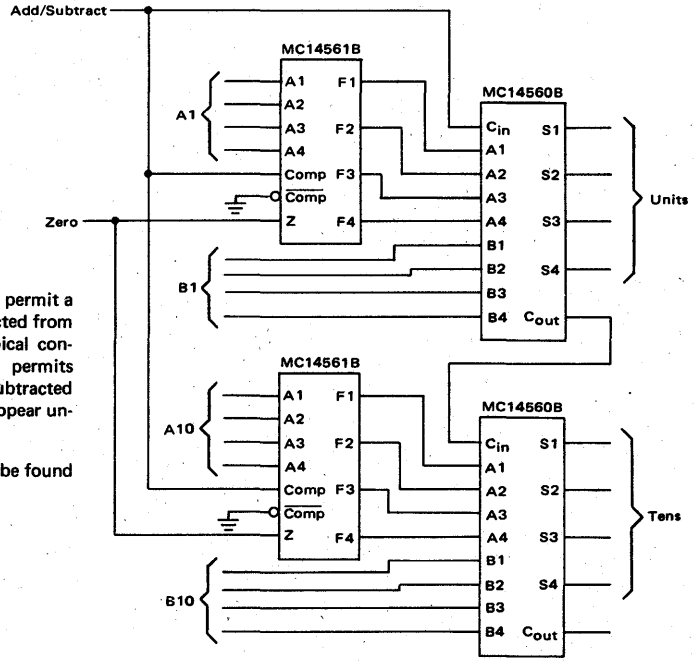


FIGURE 3 – PARALLEL ADD/SUBTRACT CIRCUIT



One MC14560B and MC14561B permit a BCD digit to be added to or subtracted from a second digit, such as in this typical configuration. A second MC14561B permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

Additional applications data may be found in Application Note AN-738.

TRUTH TABLE

Zero	Add/Subtract	Result
0	0	B plus A
0	1	B minus A
1	X	B

X = Don't Care

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Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14561B

9's COMPLEMENTER

The MC14561B 9's complementer is a companion to the MC14560B NBCD adder to allow BCD subtraction. A BCD number (8-4-2-1 code) is applied to the inputs ($A1 = 2^0$, $A2 = 2^1$, $A3 = 2^2$, $A4 = 2^3$). If the complement control (Comp) is low, the BCD number appears at the outputs unmodified. The complement disable (Comp) allows the complement control to be gated, or an inverted control signal to be used. If the complement input is high and the disable input low, the 9's complement of the number is displayed at the outputs. The zero control (Z), when high, forces the outputs low regardless of the state of the other inputs.

When the MC14561B is used to perform BCD subtraction in conjunction with the MC14560B NBCD adder, the complement control becomes an add/subtract control.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Propagation Delay = 160 ns typical at V_{DD} = 10 Vdc
- All Inputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

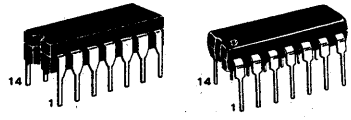
Z	Comp	$\overline{Comp}$	F1	F2	F3	F4	Mode
0	0	0	A1	A2	A3	A4	Straight-through
0	0	1					
0	1	1					
0	1	0	$\overline{A1}$	A2	$A2\overline{A3} + \overline{A2}A3$	$\overline{A2}\overline{A3}\overline{A4}$	Complement
1	X	X	0	0	0	0	Zero

X = Don't Care.

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

9's COMPLEMENTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

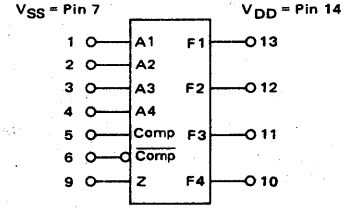
P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM

V_{SS} = Pin 7 V_{DD} = Pin 14



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.5 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.0 µA/kHz) f + I_{DD}							
		15	I_T = (4.5 µA/kHz) f + I_{DD}							

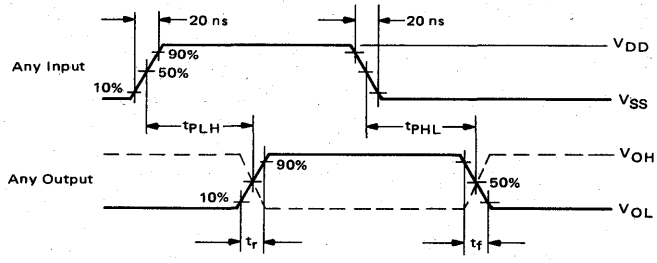
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Maximum AL Device	Maximum CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	400	600	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 127 ns		10	160	240	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	120	180	300	

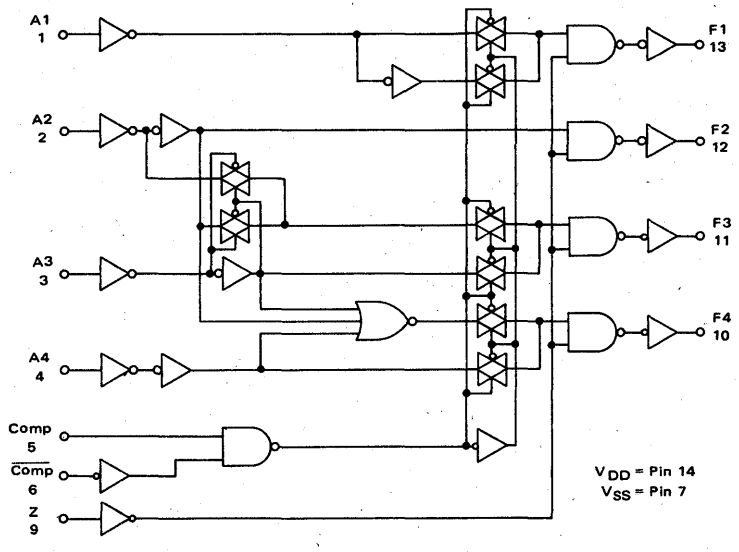
*The formula given is for the typical characteristics only.

FIGURE 1 – SWITCHING TIME WAVEFORMS



5

LOGIC DIAGRAM



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TRUTH TABLE – COMPLEMENT MODE

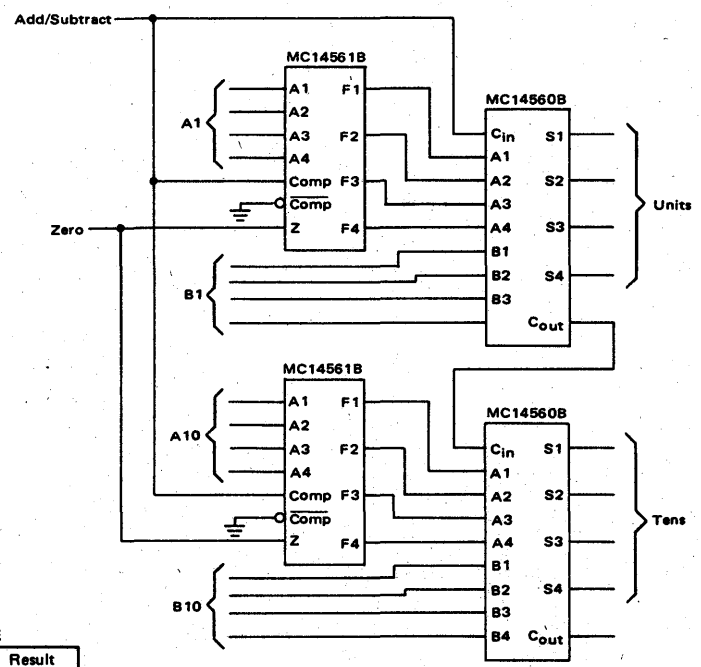
(Z = 0, Comp = 1, $\overline{\text{Comp}}$ = 0)

	Decimal Equivalent Input	Inputs				Decimal Equivalent Output	Outputs			
		A4	A3	A2	A1		F4	F3	F2	F1
	0	0	0	0	0	9	1	0	0	1
	1	0	0	0	1	8	1	0	0	0
	2	0	0	1	0	7	0	1	1	1
	3	0	0	1	1	6	0	1	1	0
	4	0	1	0	0	5	0	1	0	1
	5	0	1	0	1	4	0	1	0	0
	6	0	1	1	0	3	0	0	1	1
	7	0	1	1	1	2	0	0	1	0
	8	1	0	0	0	1	0	0	0	1
	9	1	0	0	1	0	0	0	0	0
Illegal BCD Input Codes	10	1	0	1	0	7	0	1	1	1
	11	1	0	1	1	6	0	1	1	0
	12	1	1	0	0	5	0	1	0	1
	13	1	1	0	1	4	0	1	0	0
	14	1	1	1	0	3	0	0	1	1
	15	1	1	1	1	2	0	0	1	0

TYPICAL APPLICATIONS

One MC14560B and one MC14561B permit a BCD digit to be added to or subtracted from a second digit, such as in the typical configurations in Figures 2 and 3. A second MC14561B permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

FIGURE 2 – PARALLEL ADD/SUBTRACT CIRCUIT (10's COMPLEMENT)

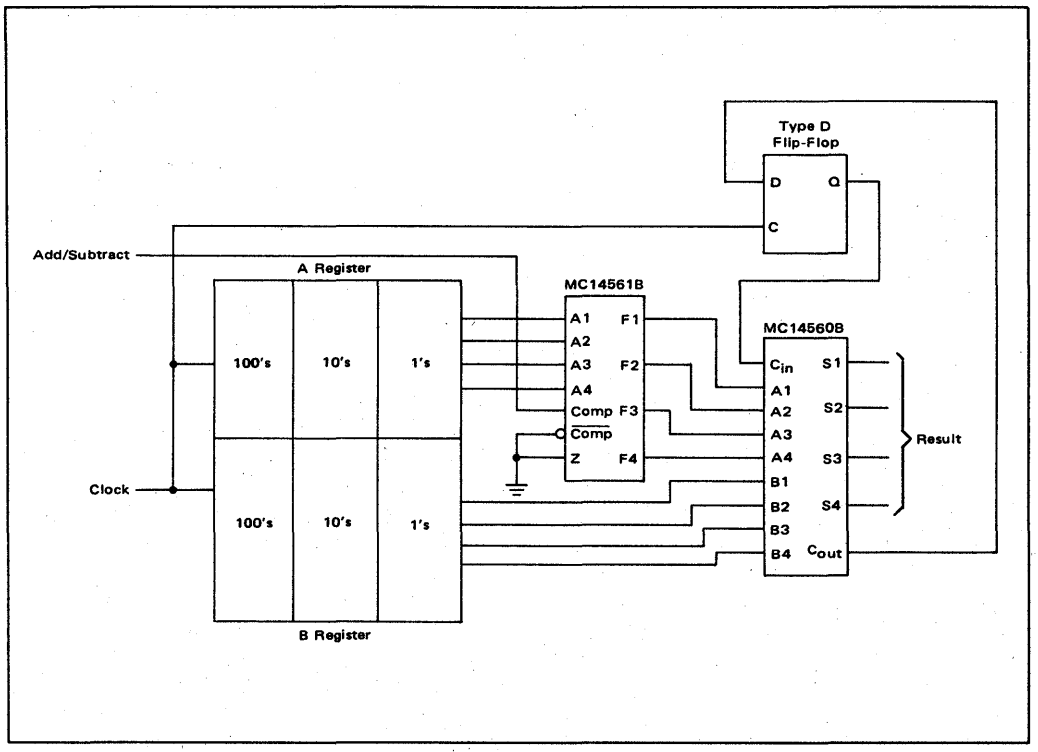


TRUTH TABLE

Zero	Add/Subtract	Result
0	0	B plus A
0	1	B minus A
1	X	B

X = Don't Care

FIGURE 3 – SERIAL ADD/SUBTRACT CIRCUIT



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MC14562B

128-BIT STATIC SHIFT REGISTER

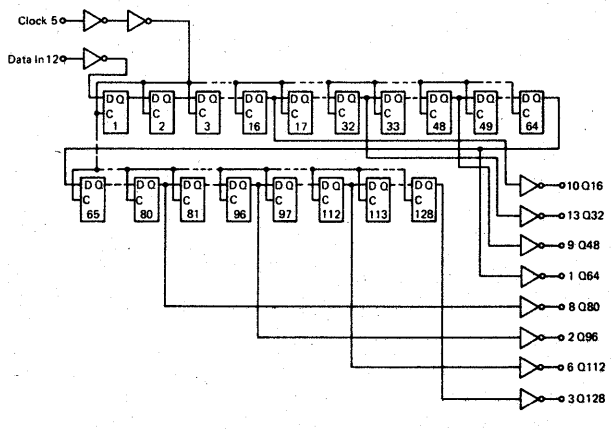
The MC14562B is a 128-bit static shift register constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data is clocked in and out of the shift register on the positive edge of the clock input. Data outputs are available every 16 bits, from 16 through bit 128. This complementary MOS shift register is primarily used where low power dissipation and/or high noise immunity is desired.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- Single Supply Operation – Positive or Negative
- Fully Static Operation
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 5.6 MHz Operation @ V_{DD} = 10 Vdc
- Cascadable to Provide Longer Shift Register Lengths – 1.5 MHz Operation @ V_{DD} = 10 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

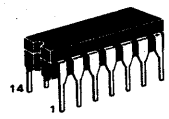
LOGIC DIAGRAM



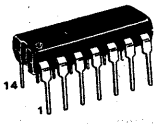
McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

128-BIT STATIC SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

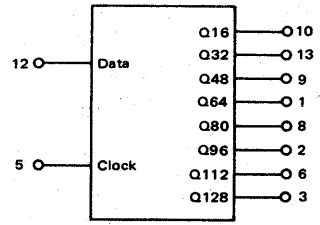


P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



Pins 4 and 11 not used.

V_{DD} = Pin 14
V_{SS} = Pin 7

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.94 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.81 µA/kHz) f + I_{DD}							
		15	I_T = (5.52 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

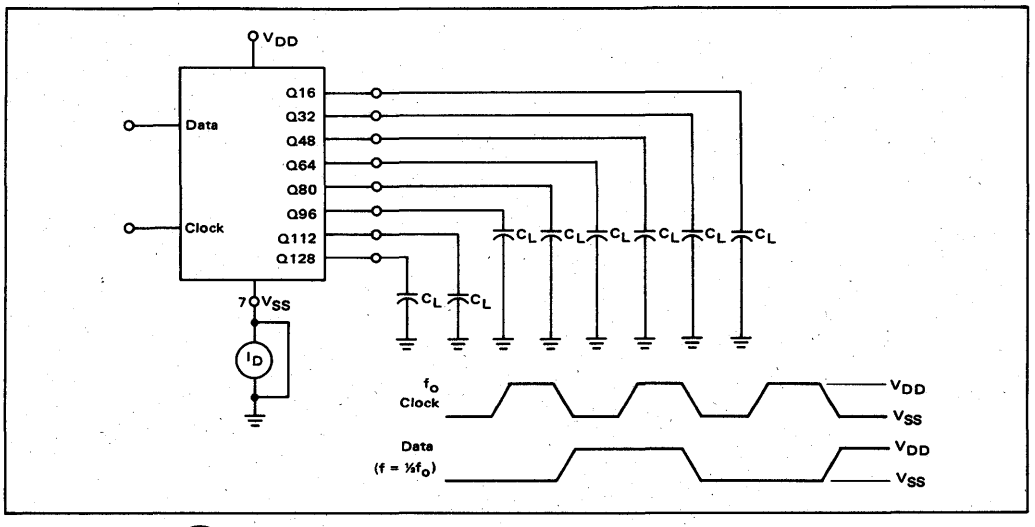
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

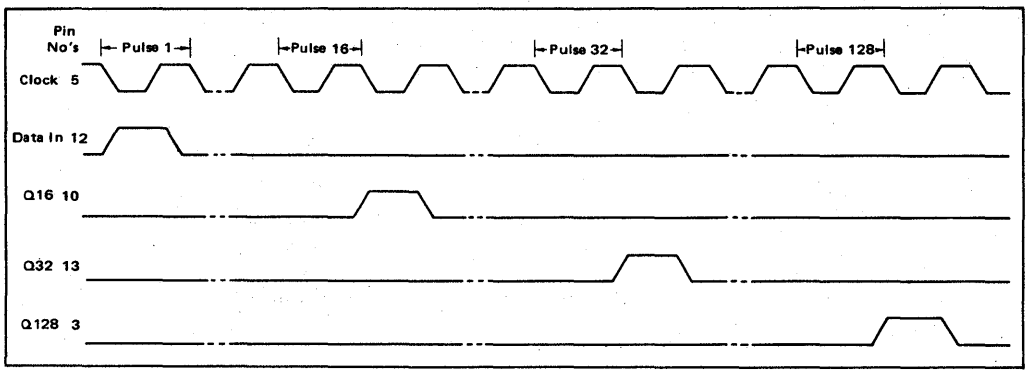
Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time Clock to Q	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 515 ns		5.0	–	–	600	900	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	–	–	250	375	660	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	–	170	255	500	
Minimum Clock Pulse Width (50% Duty Cycle)	PW_C	5.0	–	–	300	450	900	ns
		10	–	–	110	165	330	
		15	–	–	75	125	250	
Maximum Clock Pulse Frequency	PRF	5.0	1.1	0.6	1.9	–	–	MHz
		10	3.0	1.5	5.6	–	–	
		15	4.0	2.0	8.0	–	–	
Data to Clock Setup Time	t_{setup} "1"	5.0	–	–	–170	–40	–20	ns
		10	–	–	–64	–30	–10	
		15	–	–	–60	–15	0	
	t_{setup} "0"	5.0	–	–	–91	–40	–20	ns
		10	–	–	–58	–30	–10	
		15	–	–	–40	–15	0	
Data to Clock Hold Time	t_{hold} "1"	5.0	–	–	263	320	350	ns
		10	–	–	109	135	165	
		15	–	–	100	125	155	
	t_{hold} "0"	5.0	–	–	267	320	350	ns
		10	–	–	140	170	200	
		15	–	–	93	106	140	

*The formula given is for the typical characteristics only.

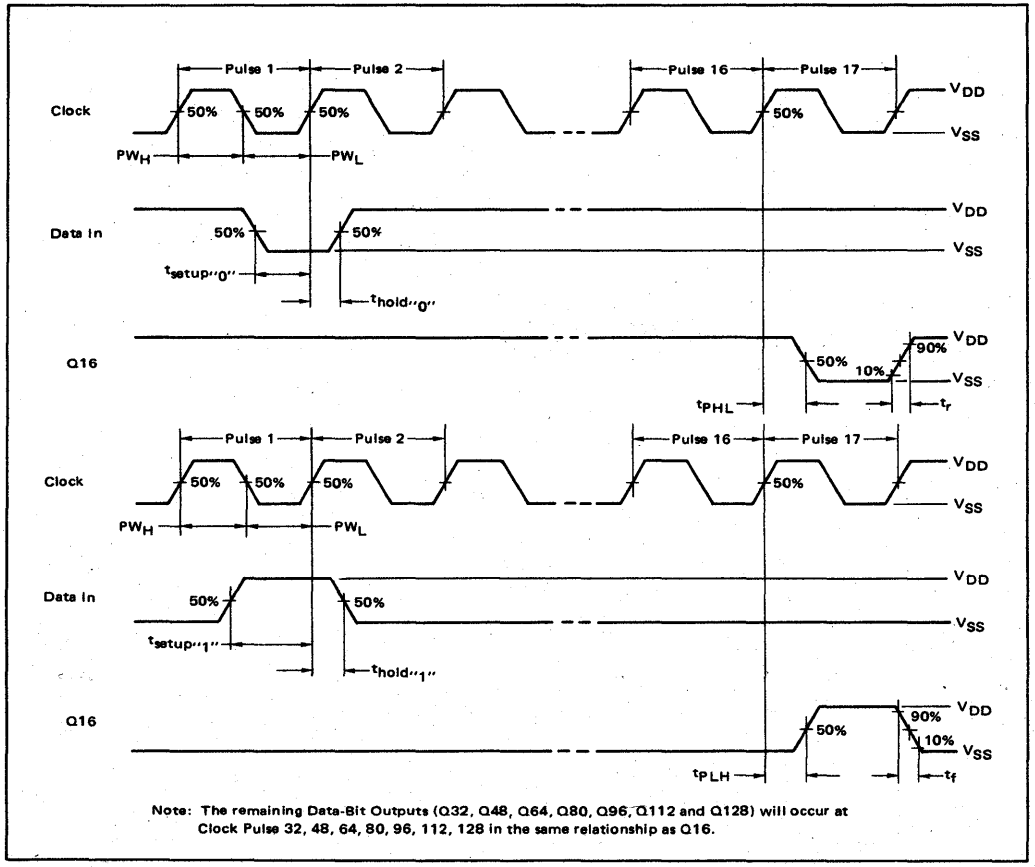
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



TIMING DIAGRAM



AC TEST WAVEFORMS



Note: The remaining Data-Bit Outputs (Q32, Q48, Q64, Q80, Q96, Q112 and Q128) will occur at Clock Pulse 32, 48, 64, 80, 96, 112, 128 in the same relationship as Q16.

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MC14566B

INDUSTRIAL TIME BASE GENERATOR

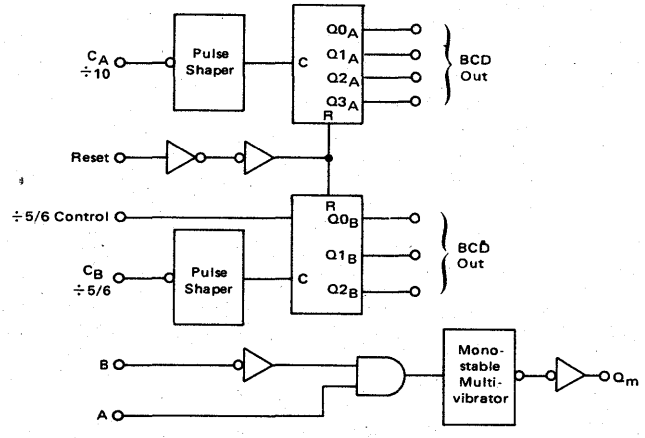
The MC14566B industrial time base generator is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of a divide-by-10 ripple counter and a divide-by-5 or divide-by-6 ripple counter to permit stable time generation from a 50 or 60 Hz line. By cascading this device as divide-by-60 counters, seconds and minutes can be counted and are available in BCD format at the circuit outputs. An internal monostable multivibrator is included whose output can be used as a reset or clock pulse providing additional frequency flexibility. Also a pin has been included to allow divide-by-5 counting for generating 1.0 Hz from European 50 Hz line.

- Negative Edge Triggered Counters for Ease of Cascading
- Pulse Shapers on Counter Inputs Accept Slow Input Rise Times
- Monostable Multivibrator Positive or Negative Edge Triggered
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

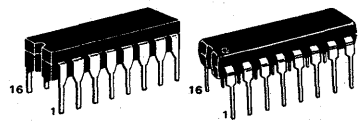
EXPANDED BLOCK DIAGRAM



McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

INDUSTRIAL TIME BASE GENERATOR



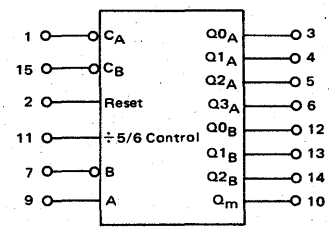
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.0 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.0 µA/kHz) f + I_{DD}							
		15	I_T = (3.0 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time, Clock to $Q3_A$	t_{PLH}, t_{PHL}							ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 1365 ns		5.0	–	–	1450	3000	4500	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 497 ns		10	–	–	530	1000	1500	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 295 ns		15	–	–	320	750	1000	
Propagation Delay Time, Reset to $Q3_A$	t_{PHL}							ns
t_{PHL} = (1.7 ns/pF) C_L + 845 ns		5.0	–	–	930	2000	3000	
t_{PHL} = (0.66 ns/pF) C_L + 282 ns		10	–	–	315	600	1000	
t_{PHL} = (0.5 ns/pF) C_L + 185 ns		15	–	–	210	450	750	
Minimum Clock Pulse Width	PW_C							ns
		5.0	–	–	400	750	1200	
		10	–	–	125	250	400	
		15	–	–	90	180	270	
Minimum Reset Pulse Width	PW_R							ns
		5.0	–	–	400	750	1200	
		10	–	–	125	250	400	
		15	–	–	90	180	270	
Maximum Clock Pulse Frequency	PRF							MHz
		5.0	0.5	0.3	1.0	–	–	
		10	1.5	1.0	2.5	–	–	
		15	2.0	1.5	4.2	–	–	
Maximum Clock Pulse Rise and Fall Time	t_r,t_f							–
		5.0	No	No	–	–	–	
		10	Limit	Limit	–	–	–	
		15			–	–	–	
Monostable Multivibrator Pulse Width	PW_{Q_m}							ns
		5.0	900	1200	2800	–	–	
		10	300	400	900	–	–	
		15	200	300	600	–	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

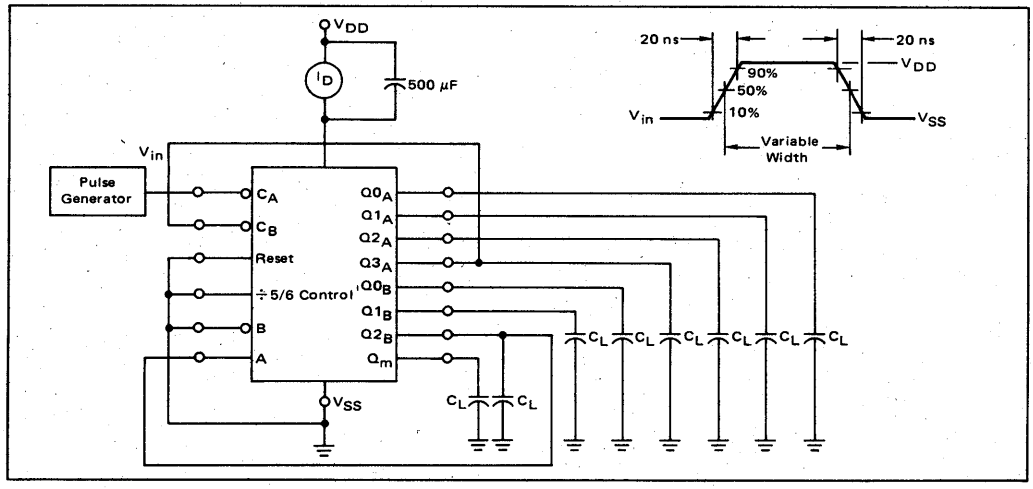
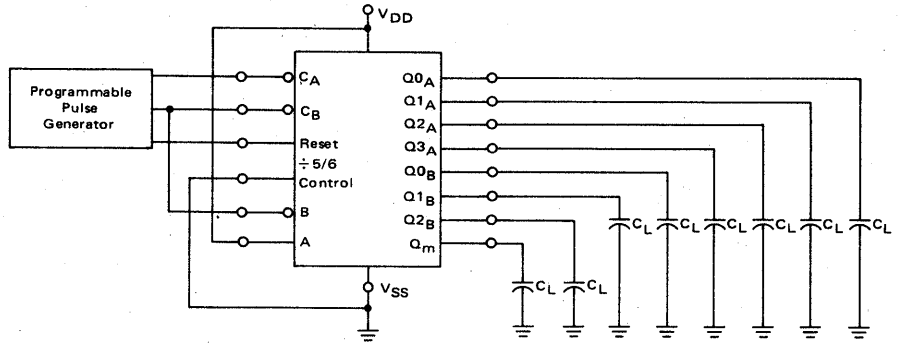
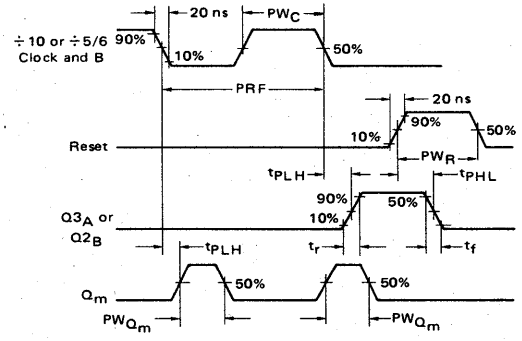


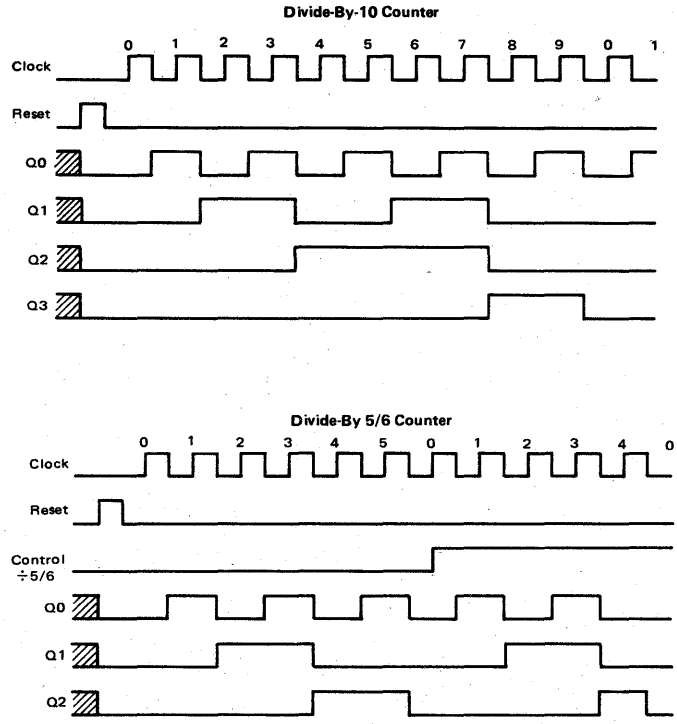
FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



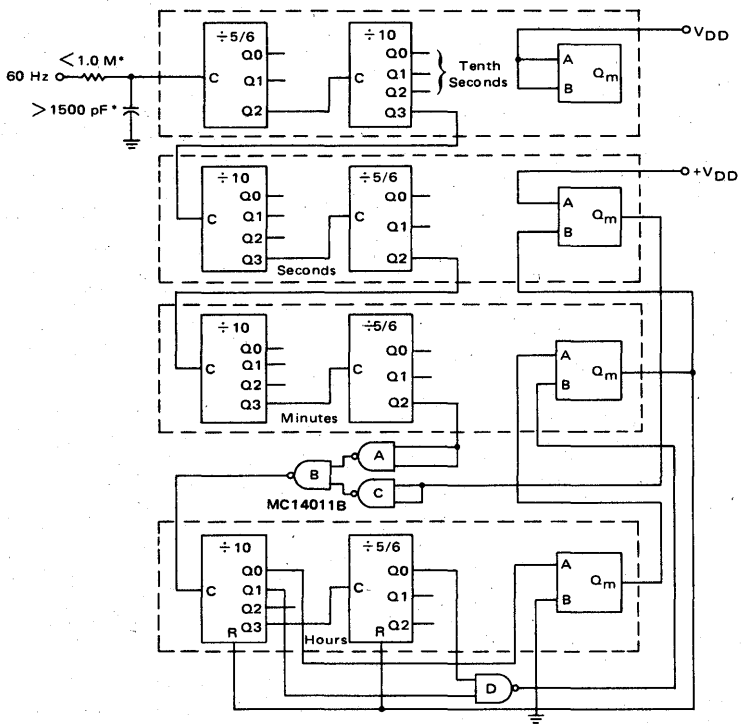
Note: Assume ÷10 Counter at "6" and ÷5/6 Counter at "2" at beginning of sequence.



TIMING DIAGRAM



APPLICATION – 12 HOUR CLOCK



÷ 5/6 Control not shown = V_{SS}

Reset pins not shown = V_{SS}

*Care must be taken in the indicated circuit to filter line transients which may cause "false" counting.

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14568B

Advance Information

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PHASE COMPARATOR AND PROGRAMMABLE COUNTERS

PHASE COMPARATOR AND PROGRAMMABLE COUNTERS

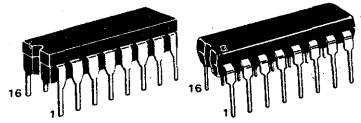
The MC14568B consists of a phase comparator, a divide-by-4, 16, 64 or 100 counter and a programmable divide-by-N 4-bit binary counter (all positive-edge triggered) constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a single monolithic structure.

This device can be used with:

- Both counters cascaded and the output of the second counter connected to the phase comparator (CTL high).
- Separate use of the programmable divide-by-N counter, for example cascaded with MC14569B (CTL low), MC14522B or MC14526B.

The MC14568B has been designed for use in conjunction with a programmable divide-by-N counter for frequency synthesizers and phase locked loop applications requiring low power dissipation and/or high noise immunity.

- Quiescent Current = 5.0 nA typ/pkg @ 5 Vdc



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

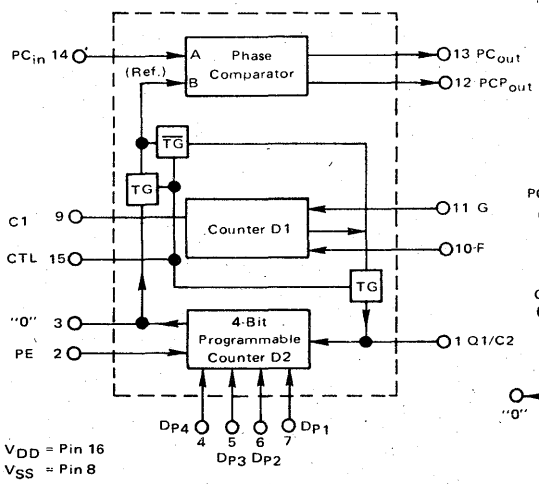
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

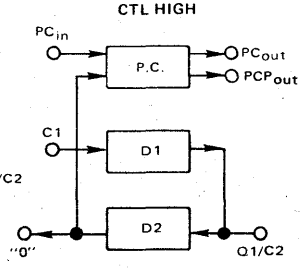
F Pin 10	G Pin 11	Division Ratio of Counter D1
0	0	4
0	1	16
1	0	64
1	1	100

The divide-by-zero state on the programmable divide-by-N 4-bit binary counter, D2, is illegal.

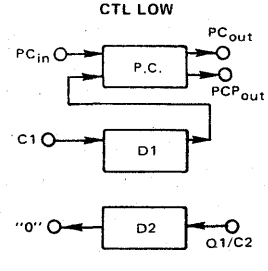
BLOCK DIAGRAM



CTL HIGH



CTL LOW



This is advance information and specifications are subject to change without notice.

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.2\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (0.4\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (0.9\ \mu A/kHz)\ f + I_{DD}$							
Three-State Leakage Current, Pins 1, 13 (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current, Pins 1, 13 (CL/CP Devices)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Minimum AL Device	Minimum CL/CP Device	Typical All Types	Maximum AL Device	Maximum CL/CP Device	Unit
Output Rise Time	t_r	5.0	–	–	180	350	400	ns
		10	–	–	90	150	200	
		15	–	–	65	110	160	
Output Fall Time	t_f	5.0	–	–	100	175	200	ns
		10	–	–	50	75	100	
		15	–	–	37	55	80	
Minimum Pulse Width, C1, Q1/C2, or PC_{in} Input	PW	5.0	–	–	125	250	300	ns
		10	–	–	60	120	150	
		15	–	–	45	90	115	
Maximum Clock Rise and Fall Time, C1, Q1/C2, or PC_{in} Input	t_r, t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
PHASE COMPARATOR								
Input Resistance	Rin	5.0 to 15	–	–	10^6	–	–	MΩ
Input Sensitivity, DC Coupled	–	5.0 to 15	See Input Voltage					
Turn-Off Delay Time, PC_{out} and PCP_{out} Outputs	t_{PHL}	5.0	–	–	550	825	1375	ns
		10	–	–	195	300	490	
		15	–	–	120	180	300	
Turn-On Delay Time, PC_{out} and PCP_{out} Outputs	t_{PLH}	5.0	–	–	675	1000	1690	ns
		10	–	–	300	450	750	
		15	–	–	190	285	475	
DIVIDE-BY-4, 16, 64 OR 100 COUNTER (D1)								
Maximum Clock Pulse Frequency	PRF							MHz
Division Ratio = 4, 64 or 100		5.0	3.0	2.0	6.0	–	–	
		10	8.0	6.0	16	–	–	
		15	10	9.0	22	–	–	
Division Ratio = 16		5.0	1.0	0.7	2.5	–	–	MHz
		10	3.0	2.5	6.3	–	–	
		15	5.0	4.0	9.7	–	–	
Propagation Delay Time, Q1/C2 Output	t_{PLH}, t_{PHL}							ns
Division Ratio = 4, 64 or 100		5.0	–	–	450	900	1200	
		10	–	–	190	300	400	
		15	–	–	130	250	300	
Division Ratio = 16		5.0	–	–	720	1400	1800	ns
		10	–	–	300	550	700	
		15	–	–	200	350	450	
PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (D2)								
Maximum Clock Pulse Frequency (Figure 3a)	PRF	5.0	1.5	1.0	1.8	–	–	MHz
		10	3.0	2.5	8.5	–	–	
		15	4.0	3.0	12	–	–	
Turn-On Delay Time, "0" Output (Figure 3a)	t_{PLH}	5.0	–	–	450	800	1100	ns
		10	–	–	190	300	400	
		15	–	–	130	210	300	
Turn-Off Delay Time, "0" Output (Figure 3a)	t_{PHL}	5.0	–	–	225	400	600	ns
		10	–	–	85	150	200	
		15	–	–	60	150	200	
Minimum Preset Enable Pulse Width (Figure 3b)	PW_{PE}	5.0	–	–	75	250	300	ns
		10	–	–	40	100	150	
		15	–	–	30	75	115	

5

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 1 – PHASE COMPARATOR

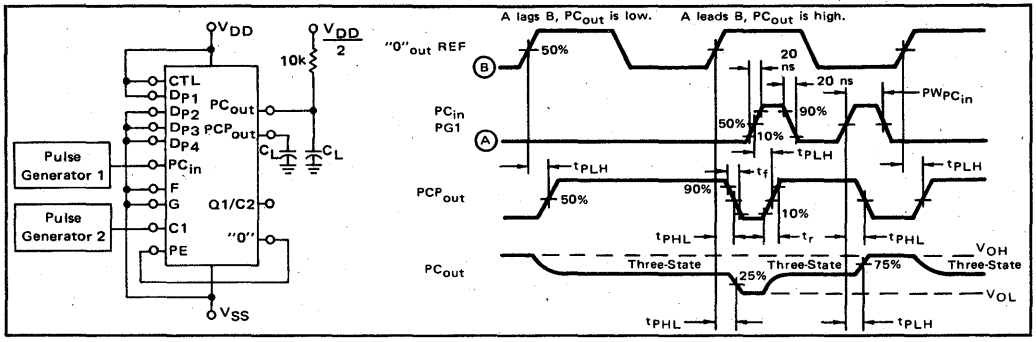


FIGURE 2 – COUNTER D1

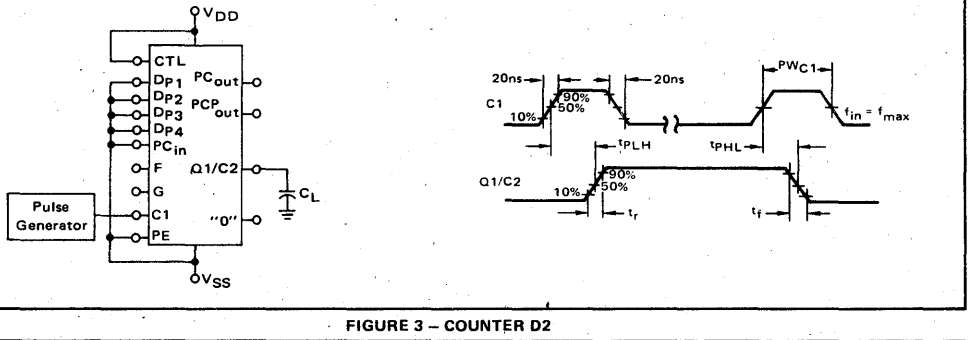
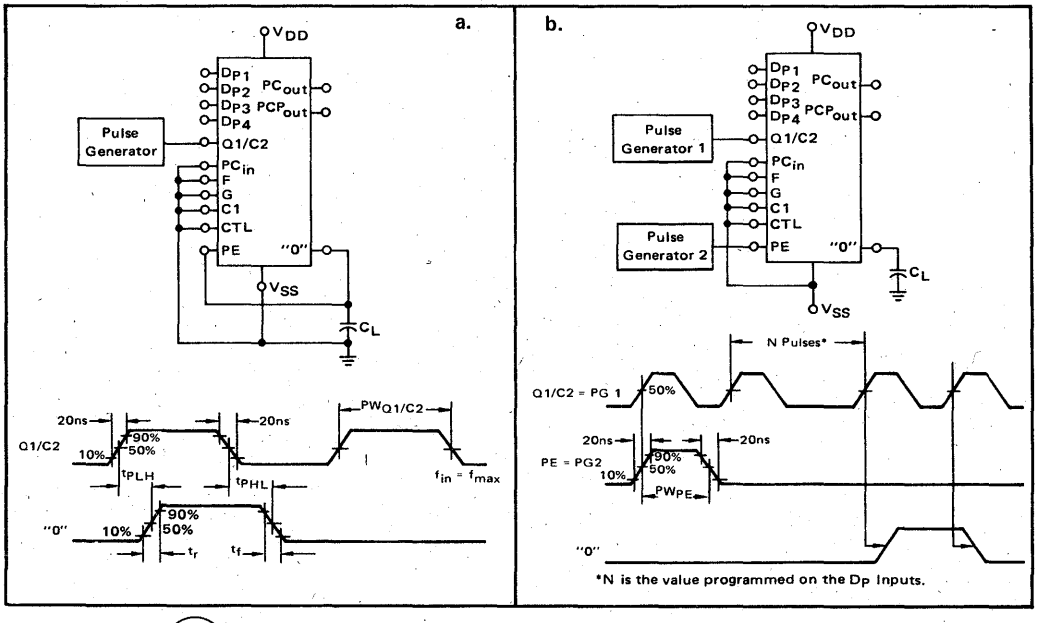
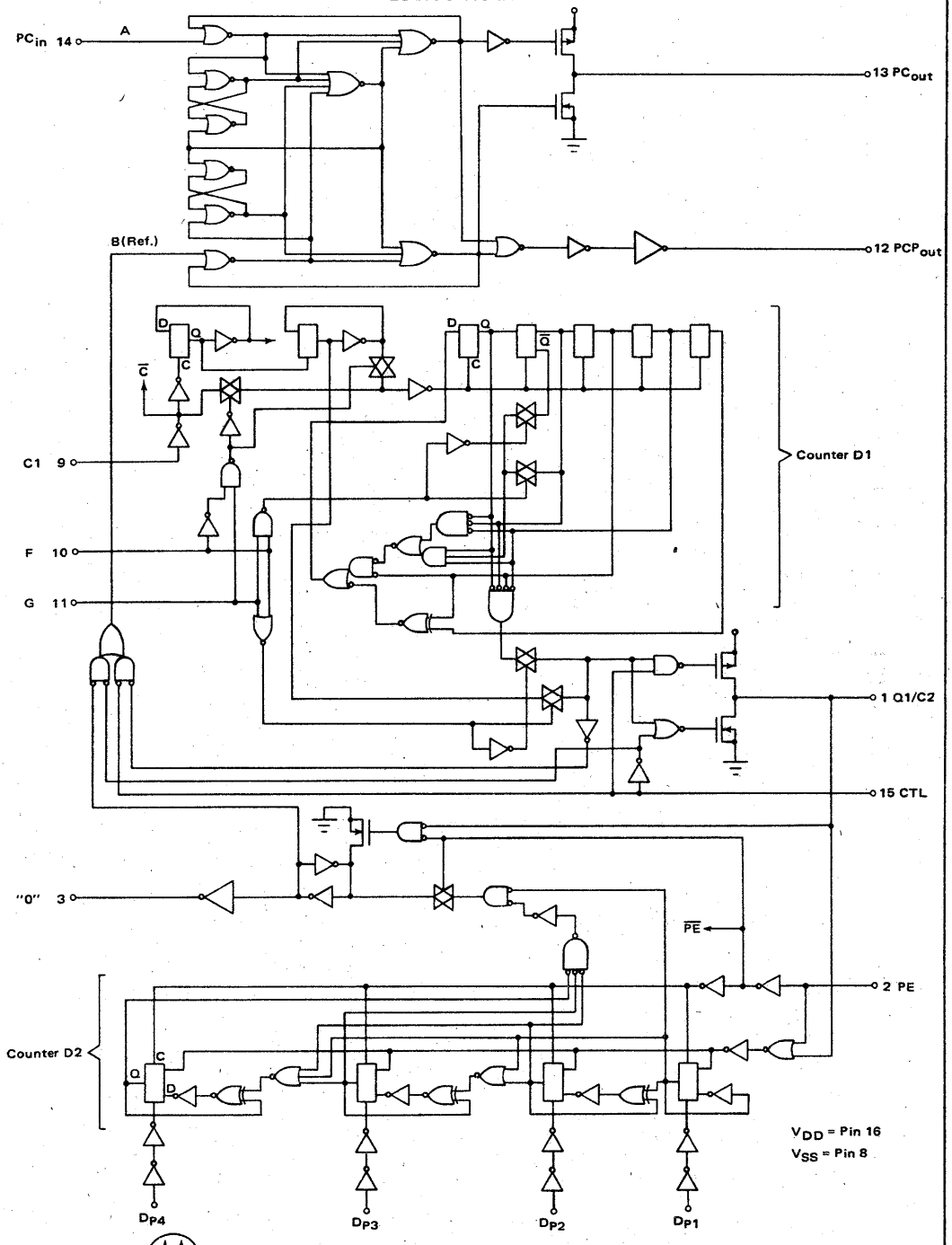


FIGURE 3 – COUNTER D2



LOGIC DIAGRAM



OPERATING CHARACTERISTICS

The MC14568B contains a phase comparator, a fixed divider (÷ 4, ÷ 16, ÷ 64, ÷ 100) and a programmable divide-by-N 4-bit counter.

PHASE COMPARATOR

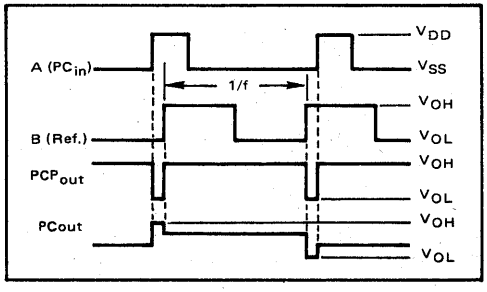
The phase comparator is a positive edge controlled logic circuit. It essentially consists of four flip-flops and an output pair of MOS transistors. Only one of its inputs (PC_{in}, pin 14) is accessible externally. The second is connected to the output of one of the two counters D1 or D2 (see block diagram).

Duty cycles of both input signals (at A and B) need not be taken into consideration since the comparator responds to leading edges only.

If both input signals have identical frequencies but different phases, with signal A (pin 14) leading signal B (Ref.), the comparator output will be high for the time equal to the phase difference.

If signal A lags signal B, the output will be low for the same time. In between, the output will be in a three-state condition and the voltage on the capacitor of an RC filter normally connected at this point will have some intermediate value (see Figure 4). When used in a phase locked loop, this value will adjust the Voltage Controlled Oscillator frequency by reducing the phase difference between the reference signal and the divided VCO frequency to zero.

FIGURE 4 – PHASE COMPARATOR WAVEFORMS



If the input signals have different frequencies, the output signal will be high when signal A has a lower frequency than signal B, and low otherwise.

Under the same conditions of frequency difference, the output will vary between V_{OH} (or V_{OL}) and some intermediate value until the frequencies of both signals are equal and their phase difference equal to zero, i.e. until locked condition is obtained.

Capture and lock range will be determined by the VCO frequency range. The comparator is provided with a lock indicator output, which will stay at logic 1 in locked conditions.

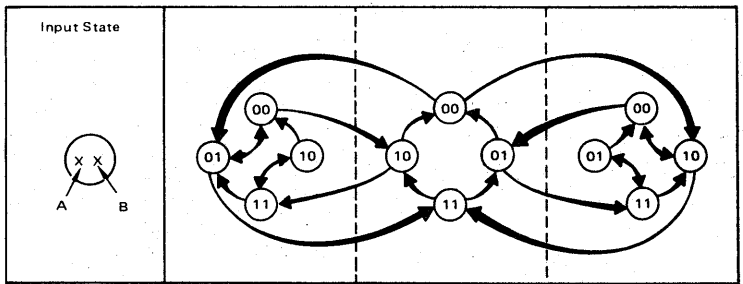
The state diagram (Figure 5) depicts the internal state transitions. It assumes that only one transition on either signal occurs at any time. It shows that a change of the output state is always associated with a positive transition of either signal. For a negative transition, the output does not change state. A positive transition may not cause the output to change; this happens when the signals have different frequencies.

DIVIDE BY 4, 16, 64 OR 100 COUNTER (D1)

This counter is able to work at an input frequency of 5 MHz for a V_{DD} value of 10 volts over the standard temperature range when dividing by 4, 64 and 100. Programming is accomplished by use of inputs F and G (pins 10 and 11) according to the truth table shown. Connecting the Control input (CTL, pin 15) to V_{DD} allows cascading this counter with the programmable divide-by-N counter provided in the same package. Independent operation is obtained when the Control input is connected to V_{SS}.

The different division ratios have been chosen to generate the reference frequences corresponding to the channel spacings normally required in frequency synthesizer applications. For example, with the division ratio 100 and a 5 MHz crystal stabilized source a reference frequency of 50 kHz is supplied to the comparator. The lower division ratios permit operation with low frequency crystals.

FIGURE 5 – PHASE COMPARATOR STATE DIAGRAM



PC_{out}	0	3-State Output Disconnected	1
PCP_{out} (Lock Indicator)	0	1	0

If used in cascade with the programmable divide-by-N counter, practically all usual reference frequencies, or channel spacings of 25, 20, 12.5, 10, 6.25 kHz, etc. are easily achievable.

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (D2)

This counter is programmable by using inputs D_{P1} . . . D_{P4} (pins 7 . . . 4). The Preset Enable input enables the parallel preset inputs D_{P1} . . . D_{P4}. The "0" output must be externally connected to the PE input for single stage applications. Since there is not a cascade feedback input, this counter, when cascaded, must be used as the most significant digit. Because of this, it can be cascaded with binary counters as well as with BCD counters (MC14569B, MC14522B, MC14526B).

TYPICAL APPLICATIONS

FIGURE 6 – CASCADING MC14568B AND MC14522B OR MC14526B WITH MC14569B

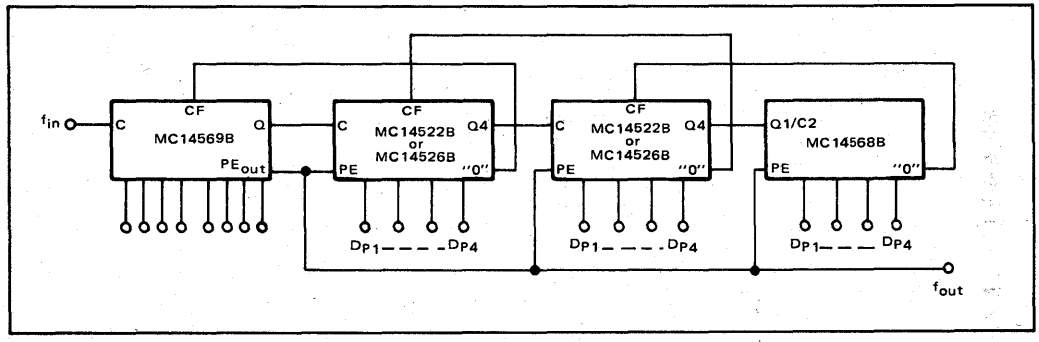


FIGURE 7 – FREQUENCY SYNTHESIZER WITH MC14568B and MC14569B USING A MIXER
(Channel Spacing 10 kHz)

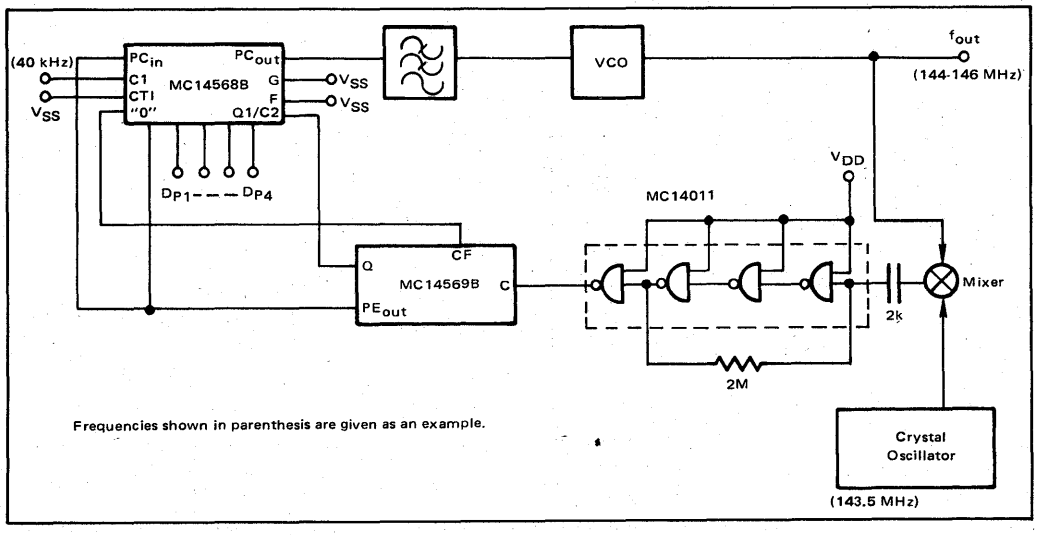
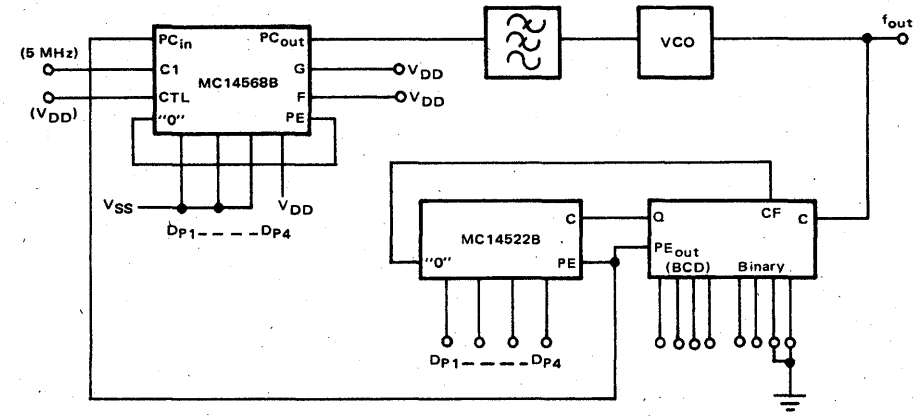


FIGURE 8 – FREQUENCY SYNTHESIZER USING MC14568B, MC14569B AND MC14522B
(Without Mixer)



N_1	N_2	N_3
(0–5)	(0–9)	(0, 4, 8, 12)
(625 kHz steps)	(62.5 kHz steps)	(6.25 kHz steps)

Divide ratio = $160N_1 + 16N_2 + N_3$

Example:
$f_{out} = N_1$ (MHz) + N_2 (x100 kHz) + N_3 (x25 kHz)
Frequency range = 5 MHz
Channel spacing = 25 kHz
Reference frequency = 6.25 kHz

Figures shown in parenthesis refer to example.

5

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MC14569B

Advance Information

McMOS MSI

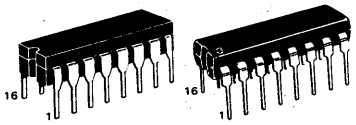
(LOW-POWER COMPLEMENTARY MOS)

HIGH SPEED PROGRAMMABLE DIVIDE-BY-N DUAL 4-BIT BCD/BINARY COUNTER

The MC14569B is a high speed programmable divide-by-N dual 4-bit BCD or binary down counter constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a single monolithic structure.

It has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- 8 MHz Counting Rate for Any Division Ratio Greater Than 1
- Speed-up Circuitry for Zero Detection and Preset Enable
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Quiescent Current = 5.0 nA typ/pkg @ 5 Vdc
- Can be Cascaded with MC14568B, MC14522B and MC14526B for Frequency Synthesizer Applications



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

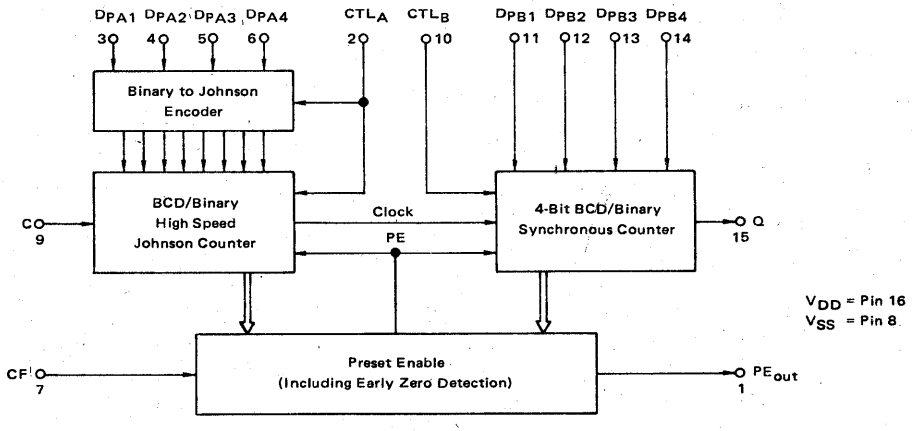
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM

CTL = "0" for Binary Count
CTL = "1" for BCD Count



This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-0.88	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.005	50	–	150	μAdc
(Per Package)		10	–	100	–	0.010	100	–	300	
		15	–	200	–	0.015	200	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15								μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Output Rise Time	t_r	5.0 10 15	–			ns
Output Fall Time	t_f	5.0 10 15	This table lists all of the characteristics to be specified for this device. Final specifications were not available at the time of printing. For the latest data, contact: CMOS Marketing Motorola Semiconductor Products Inc. 3501 Ed Bluestein Blvd. Austin, Texas 78721 (512) 928-2600			ns
Turn-On Delay Time PE_{out}	t_{PLH}	5.0 10 15				ns
Q Output		5.0 10 15				ns
Turn-Off Delay Time PE_{out}	t_{PHL}	5.0 10 15				ns
Q Output		5.0 10 15	– – –			ns
Minimum Clock Pulse Width	PW_C	5.0 10 15	– – –			ns
Maximum Clock Pulse Frequency #	PRF	5.0 10 15			– – –	MHz
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0 10 15	– – –			μs

#This inplies that zero detection and preset enable is done while the clock is running at the specified frequency.

5

SWITCHING WAVEFORMS

FIGURE 1

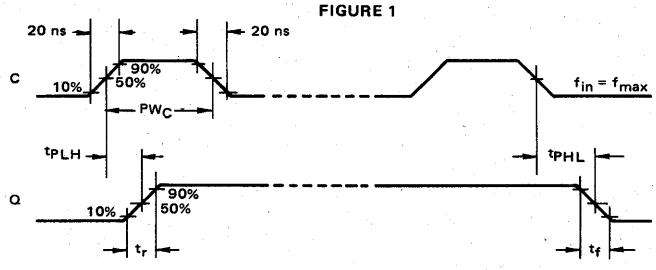
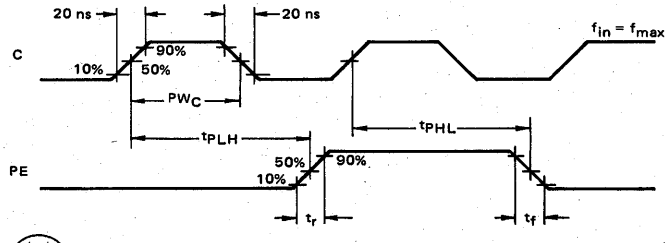
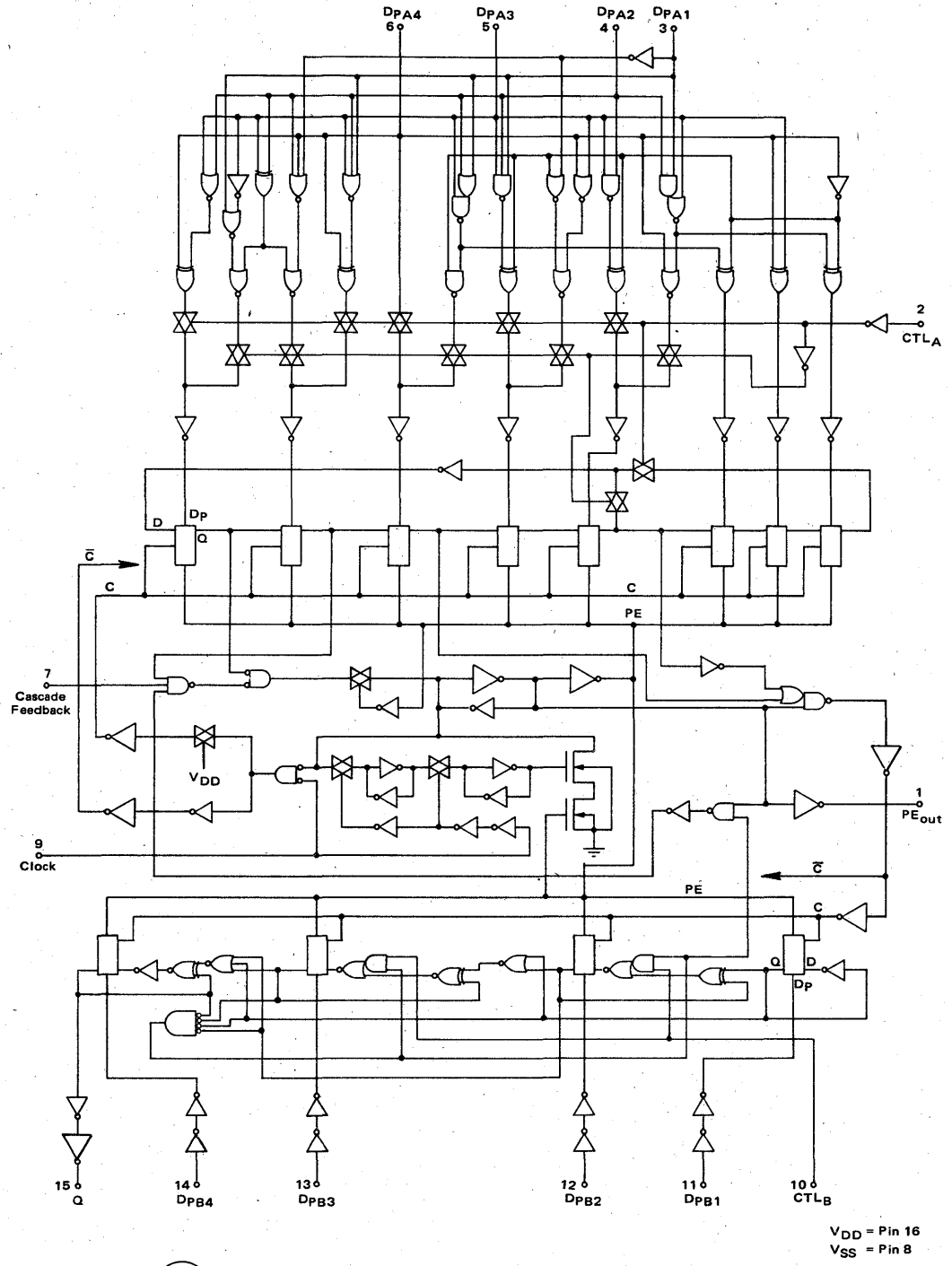


FIGURE 2



LOGIC DIAGRAM



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OPERATING CHARACTERISTICS

The MC14569B includes a high speed Johnson counter followed by a BCD/binary 4-bit synchronous counter (see block diagram). The use of an encoder allows the Johnson counter to be programmed (i.e. preset) in BCD or binary code through inputs D_{PA1}, D_{PA2}, D_{PA3}, and D_{PA4}.

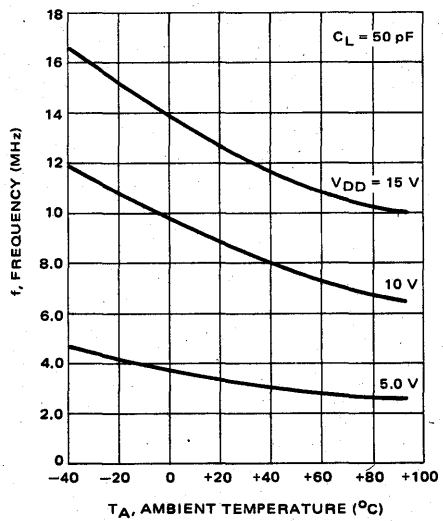
The BCD/binary counter can be programmed through inputs D_{PB1}, D_{PB2}, D_{PB3}, and D_{PB4}. For each counter a divide ratio of 10 (BCD count) or 16 (binary count) can be chosen independently by inputs CTL_A and CTL_B respectively. When one of those inputs is set high, the divide ratio of the corresponding counter is 10 (BCD); when it is set low, the division ratio is 16 (binary).

A Cascade Feedback input (pin 7), a Q output (pin 15) and a Preset Enable output (pin 1) made it possible to cascade the MC14568B, MC14522B and MC14526B with this device. CF, Q and PE_{out} of MC14569B must be respectively connected to "0", C and PE of the following counter.

When MC14569B is used alone, CF must be connected to V_{DD}. One pulse will appear on output PE_{out} every N clock periods (N being the value programmed on the Dp inputs). Both counters included in MC14569B, and eventually all the counters which are cascaded, should normally be preset at the programmed values during the clock period where they all reach the count zero. For best speed performance, preset is started as soon as count 1 is detected. As a consequence, it is not possible to program a frequency division ratio of one. However, it is possible to program a division ratio of 11 (i.e. $D_{PA1}, \ldots D_{PA4}$ = 1,0,0,0 and $D_{PB1}, \ldots D_{PB4}$ = 1,0,0,0), or a division ratio of 101 if another counter is cascaded with the MC14569B.

This high speed configuration makes it possible to guarantee a maximum clock pulse frequency of 5 MHz for a 10 V V_{DD} supply for any division ratio greater than one. Due to the presence of the early zero detection, the circuit must be used in the two least significant digit positions.

Because all the circuitry is static, there is no minimum frequency specification for the Clock input, C (pin 9).



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MC14572

HEX GATE

The MC14572 hex functional gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

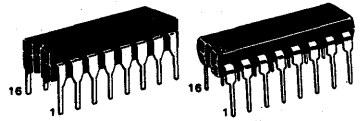
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Single Supply Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Input Impedance = 10^{12} ohms typical
- NOR Input Pin Adjacent to V_{SS} Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to V_{DD} Pin to Simplify Use As An Inverter
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND Application
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX GATE

4 INVERTERS PLUS
2-INPUT NOR GATE PLUS
2-INPUT NAND GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

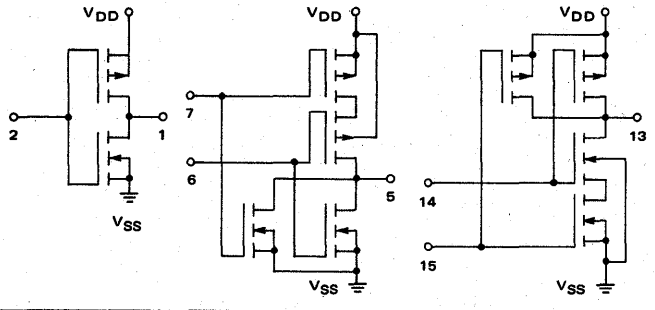
ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

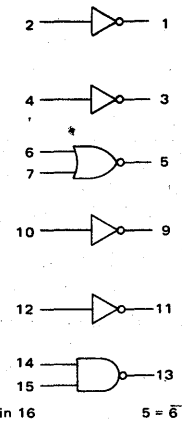
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

$5 = \overline{6 + 7}$
$13 = \overline{14 \cdot 15}$

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.4	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	2.9	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.6	
"1" Level	V_{IH}									
(V_O = 1.4 or 3.6 Vdc)		5.0	3.6	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 2.8 or 7.2 Vdc)		10	7.1	–	7.0	5.50	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.4	–	11.25	8.25	–	11.25	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.05	–	0.0005	0.05	–	1.5	µAdc
		10	–	0.10	–	0.0010	0.10	–	3.0	
		15	–	0.20	–	0.0015	0.20	–	6.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	0.5	–	0.0005	0.5	–	3.8	µAdc
		10	–	1.0	–	0.0010	1.0	–	7.5	
		15	–	2.0	–	0.0015	2.0	–	15	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.89 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.80 µA/kHz) f + I_{DD}							
		15	I_T = (5.68 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

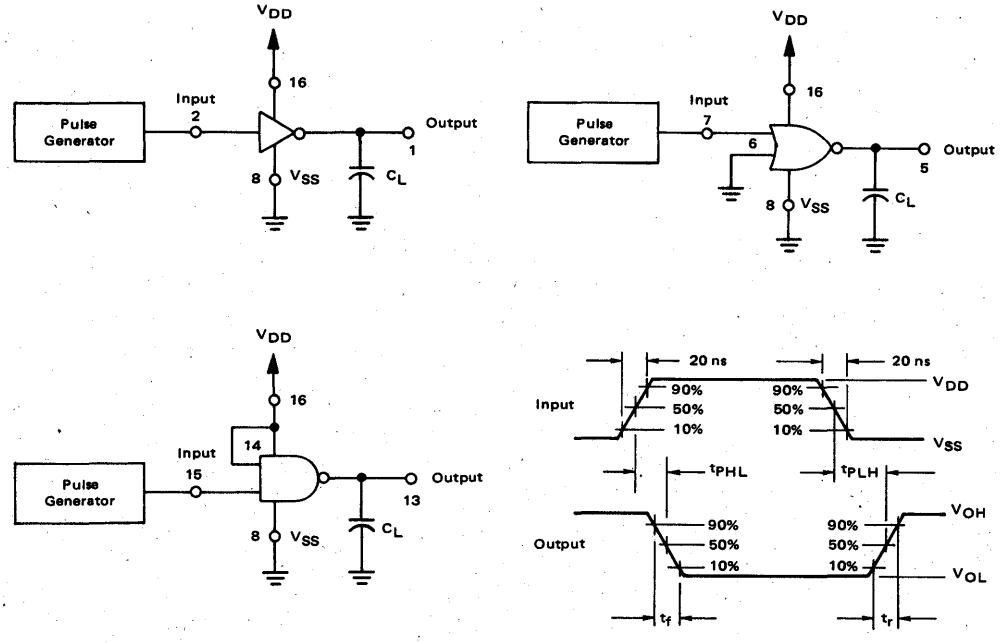
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns)		5.0	115	165	200	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns)		10	55	95	110	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 15 ns)		15	40	75	85	

*The formula given is for the typical characteristics only.

FIGURE 1 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



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MC14580B

4 x 4 MULTIPORT REGISTER

The MC14580B is a 4 by 4 multiport register useful in small scratch pad memories, arithmetic operations when coupled with an adder, and other data storage applications. It allows independent reading of any two words (or the same word at both outputs) while writing into any one of four words.

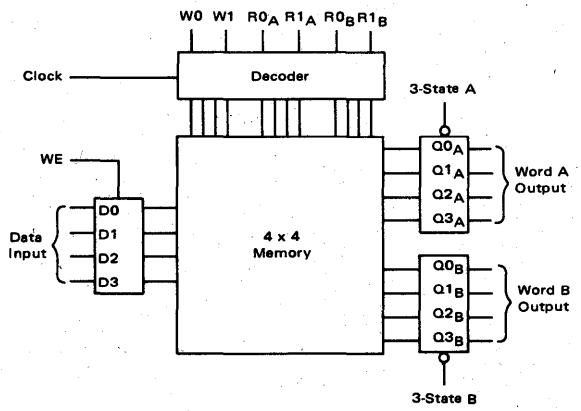
Address changing and data entry occur on the rising edge of the clock. When the write enable input is low, the contents of any word may be accessed but not altered.

- Logic Swing Independent of Fanout
- No Restrictions on Clock Input Rise or Fall Times
- 3-State Outputs
- Single Phase Clocking
- Quiescent Current = 10 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

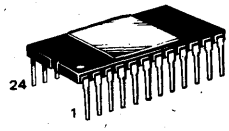
BLOCK DIAGRAM



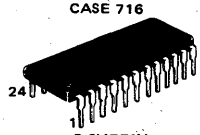
McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

4 x 4 MULTIPORT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 716

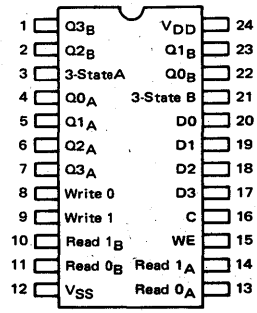


P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



V_{DD} = Pin 24
V_{SS} = Pin 12

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.18 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.91 µA/kHz) f + I_{DD}							
		15	I_T = (2.67 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

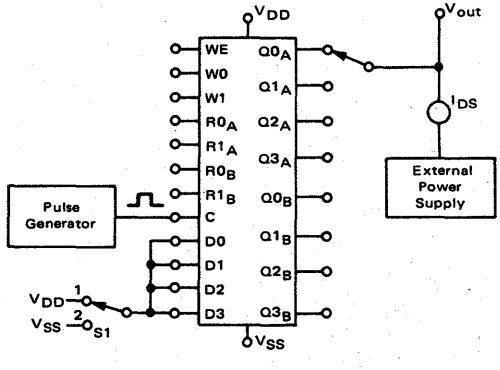
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Propagation Delay Time, Clock to Output	t_{PLH}, t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 1415 ns		5.0	1500	3000	4500	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 467 ns		10	500	1000	1500	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 325 ns		15	350	750	1125	
Write Enable Setup Time	$t_{setup(WE)}$	5.0	800	1600	2400	ns
		10	300	600	900	
		15	180	450	675	
Write Enable Setup Time	$t_{setup(\overline{WE})}$	5.0	-300	+100	+150	ns
		10	-100	+50	+75	
		15	-60	+40	+55	
Write Enable Hold Time	$t_{hold(\overline{WE})}$	5.0	-800	-1600	-2400	ns
		10	-300	-600	-900	
		15	-180	-450	-675	
Address and Data Setup Time	$t_{setup(D)}$, $t_{setup(W)}$	5.0	150	300	450	ns
		10	70	140	210	
		15	50	105	160	
Address and Data Hold Time	$t_{hold(D)}$, $t_{hold(W)}$	5.0	160	320	480	ns
		10	65	130	195	
		15	50	100	150	
3-State Enable/Disable Delay Time**	t_{dis}, t_{en}	5.0	355	600	900	ns
		10	140	220	350	
		15	85	165	250	
Positive Clock Pulse Width	PW_{CH}	5.0	1000	2000	3000	ns
		10	350	700	1050	
		15	200	525	800	
Negative Clock Pulse Width	PW_{CL}	5.0	400	800	1200	ns
		10	85	170	255	
		15	60	130	200	

*The formula given is for the typical characteristics only.

**Measured at the point of 10% change at output when the output load is 1.0 kΩ and 50 pF.

FIGURE 1 – OUTPUT DRIVE CURRENT TEST CIRCUIT



	Sink Current	Source Current
Position of S1	2	1
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS (3-State Inputs are High)

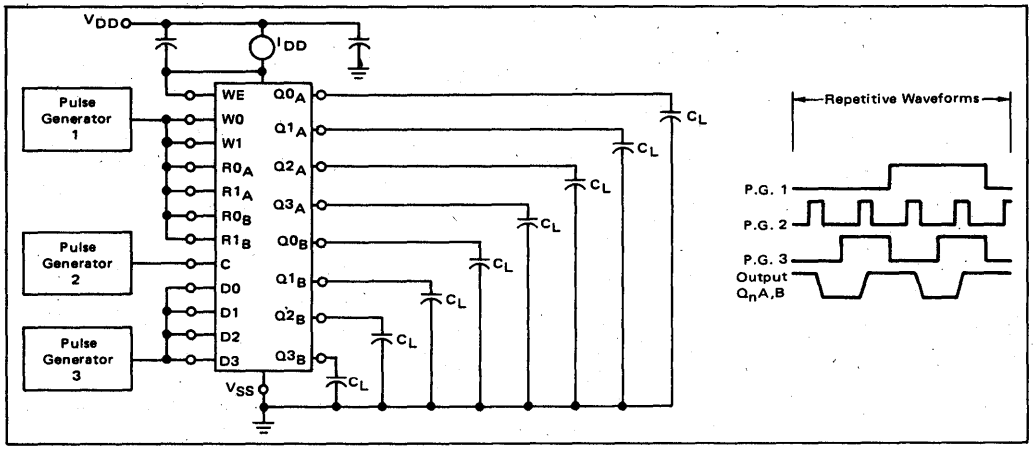


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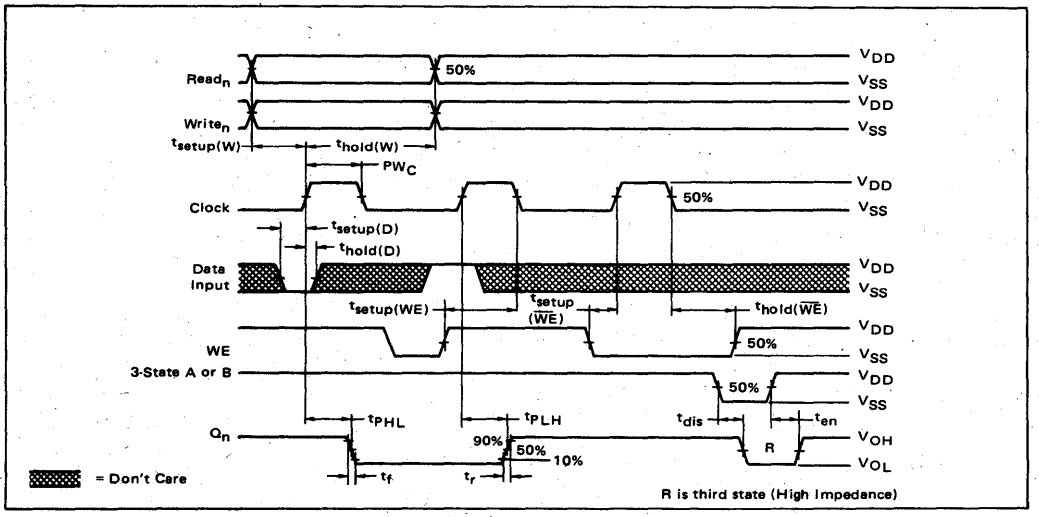
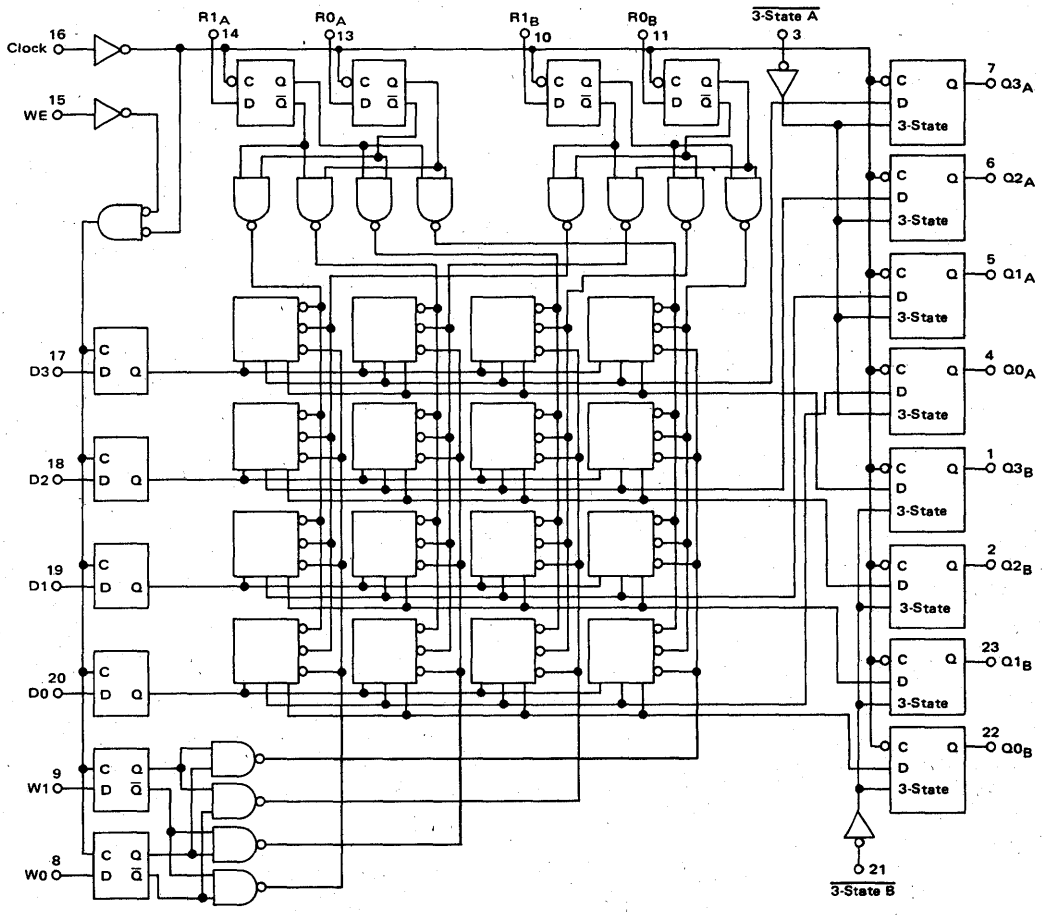
FIGURE 3 – AC WAVEFORMS AND DEFINITIONS



LOGIC DIAGRAM



TRUTH TABLE

Clock	WE	Write 1	Write 0	Read 1_A	Read 0_A	Read 1_B	Read 0_B	3-State A	3-State B	D_n	Q_nA	Q_nB
⎍	1	S1	S2	S1	S2	S1	S2	1	1	1	1	1
⎍	1	S1	S2	S1	S2	S1	S2	1	1	0	0	0
⎍	X	X	X	X	X	X	X	1	1	X	No Change	No Change
X	X	X	X	X	X	X	X	0	0	X	R	R
0	X	X	X	X	X	X	X	1	1	X	No Change	No Change
1	X	X	X	X	X	X	X	1	1	X	No Change	No Change
⎍	1	0	0	0	1	1	0	1	1	D_n to word 0	Contents of word 1 displayed	Contents of word 2 displayed
⎍	0	0	0	0	1	1	0	1	1	Word 0 not altered	Contents of word 1 displayed	Contents of word 2 displayed

S1 and S2 refer to input states of either "1" or "0"
R implies high resistance ~ 10^9 ohms.
X = Don't care

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14581B

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT ARITHMETIC LOGIC UNIT

4-BIT ARITHMETIC LOGIC UNIT

The MC14581B is a CMOS 4-bit ALU logic unit capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 4-bit words. The level of the mode control input determines whether the output funciton is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the select inputs (S0 thru S3) with the mode control input high, while the desired arithmetic operation is selected by applying a low voltage to the mode control input, the required level to carry in, and the appropriate word to the select inputs. The word inputs and function outputs can be operated with either active high or active low data.

Carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs are provided to allow a full look-ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the MC14582B as a second order look ahead block. An inverted ripple carry input (C_n) and a ripple carry output (C_{n+4}) are included for ripple through operation.

When the device is in the subtract mode (LHHL), comparison of two 4-bit words present at the $\overline{A}$ and $\overline{B}$ inputs is provided using the A = B output. It assumes a high-level state when indicating equality. Also, when the ALU is in the subtract mode the C_{n+4} output can be used to indicate relative magnitude as shown in this table:

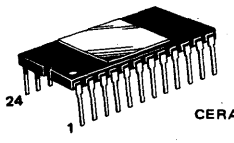
Data Level	C_n	C_{n+4}	Magnitude
Active High	H	H	$A \leq B$
	L	H	$A < B$
	H	L	$A > B$
	L	L	$A \geq B$
Active Low	L	L	$A \leq B$
	H	L	$A < B$
	L	H	$A > B$
	H	H	$A \geq B$

FEATURES:

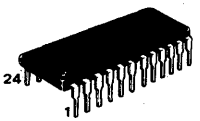
- Functional and Pinout Equivalent to 74181.
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- High Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Low Input Capacitance — 5.0 pF typical
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Load, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



L SUFFIX
CERAMIC PACKAGE
CASE 684

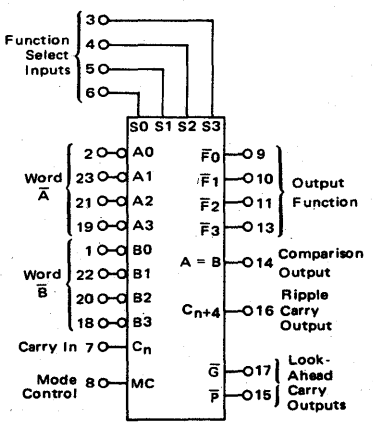


P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.8 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.7 μA/kHz) f + I_{DD}							
		15	I_T = (5.5 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 8 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Sum In to Sum Out						
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 620 ns		5.0	705	1050	2000	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	250	375	700	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	180	270	525	
Sum In to Sum Out (Logic Mode)	t_{PLH}, t_{PHL}					ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 520 ns		5.0	605	1000	1700	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 182 ns		10	215	350	600	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	180	270	525	
Sum In to A = B	t_{PLH}, t_{PHL}					ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 870 ns		5.0	955	1500	3000	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 297 ns		10	330	500	1000	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 220 ns		15	245	375	750	
Sum In to $\overline{P}$ or $\overline{G}$	t_{PLH}, t_{PHL}					ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 400 ns		5.0	485	730	1300	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	180	270	450	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	130	195	340	
Sum In to C_{n+4}	t_{PLH},					ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 530 ns		5.0	615	1000	1700	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 187 ns		10	220	350	600	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 135 ns		15	160	265	450	
Carry In to Sum Out	t_{PLH}, t_{PHL}					ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 295 ns		5.0	380	570	1000	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 112 ns		10	145	220	360	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 80 ns		15	105	160	265	
Carry In to C_{n+4}	t_{PLH}, t_{PHL}					ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 220 ns		5.0	305	460	760	
t_{PLH},t_{PHL} = (0.66 ns/pF) C_L + 87 ns		10	120	180	300	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 60 ns		15	85	130	210	

*The formula given is for the typical characteristics only.

5

AC TEST SETUP REFERENCE TABLE

TEST	AC PATHS INPUTS	AC PATHS OUTPUTS	DC DATA INPUTS TO V_{SS}	DC DATA INPUTS TO V_{DD}	MODE	FIG. 3 WAVEFORM
Sum_{in} to Sum_{out} Delay Time	$\overline{A}0$	Any $\overline{F}$	Remaining $\overline{A}$'s C_n	All $\overline{B}$'s	Add	#1
Sum_{in} to $\overline{P}$ Delay Time	$\overline{A}0$	$\overline{P}$	Remaining $\overline{A}$'s C_n	All $\overline{B}$'s	Add	#1
Sum_{in} to $\overline{G}$ Delay Time	$\overline{B}0$	C_{n+y}	All $\overline{A}$'s C_n	Remaining $\overline{B}$'s	Add	#1
Sum_{in} to C_{n+4} Delay Time	$\overline{B}0$	$\overline{G}$	All $\overline{A}$'s C_n	Remaining $\overline{B}$'s	Add	#2
C_n to Sum_{out} Delay Time	C_n	Any $\overline{F}$	All $\overline{A}$'s	All $\overline{B}$'s	Add	#1
C_n to C_{n+4} Delay Time	C_n	C_{n+4}	All $\overline{A}$'s	All $\overline{B}$'s	Add	#1
Sum_{in} to A = B Delay Time	$\overline{A}0$	A = B	All $\overline{B}$'s Remaining $\overline{A}$'s	C_n	Sub	#2
Sum_{in} to Sum_{out} Delay Time (Logic Mode)	All $\overline{B}$'s	Any $\overline{F}$	All A's	M	Exclusive OR	#2

FIGURE 1 – TYPICAL SOURCE CURRENT TEST CIRCUIT

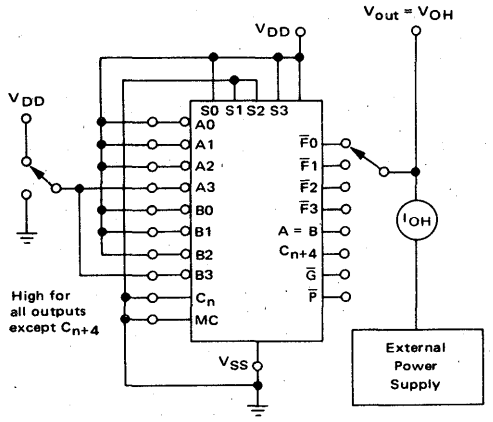


FIGURE 2 – TYPICAL SINK CURRENT TEST CIRCUIT

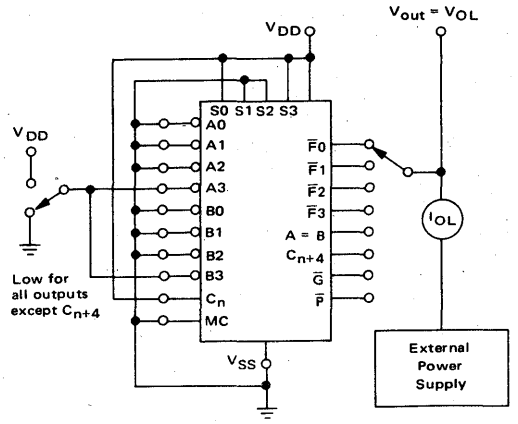


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

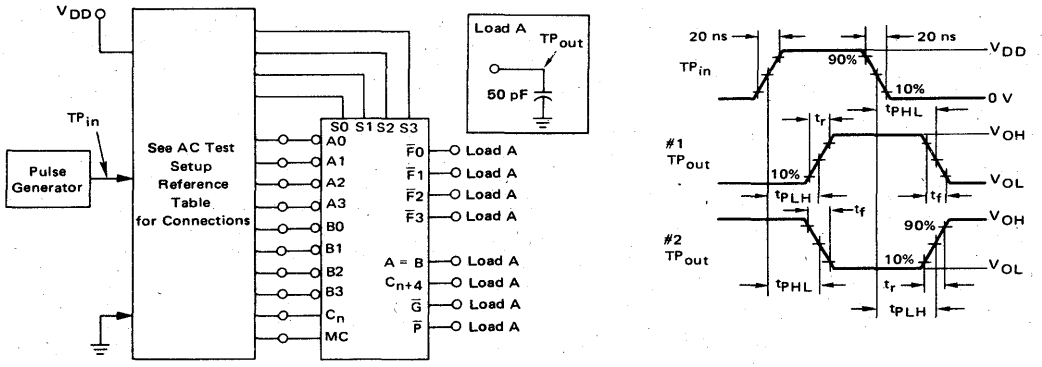
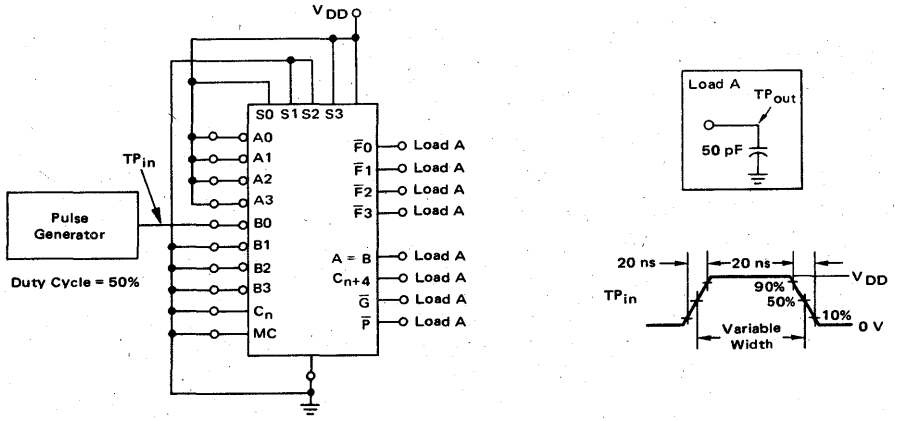
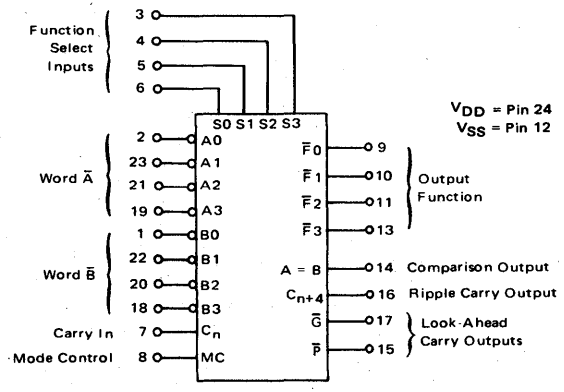


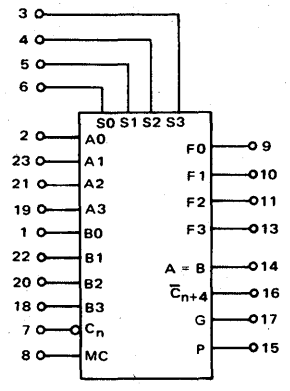
FIGURE 4 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



BLOCK DIAGRAM (ACTIVE LOW)



BLOCK DIAGRAM (ACTIVE HIGH)



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TRUTH TABLE

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE LOW		INPUTS/OUTPUTS ACTIVE HIGH	
				LOGIC FUNCTION	ARITHMETIC* FUNCTION	LOGIC FUNCTION	ARITHMETIC* FUNCTION
S3	S2	S1	S0	(MC = H)	(MC = L, C_n = L)	(MC = H)	(MC = L, $\overline{C}_n$ = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A+B
L	L	H	L	$\overline{A}+B$	$A\overline{B}$ minus 1	$\overline{A}B$	$A+\overline{B}$
L	L	H	H	Logic "1"	minus 1	Logic "0"	minus 1
L	H	L	L	$\overline{A+B}$	A plus $(A+\overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A+\overline{B})$	$\overline{B}$	$(A+B)$ plus $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{A}B$	A plus $(A+B)$	$\overline{A+B}$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus $(A+B)$	B	$(A+\overline{B})$ plus AB
H	L	H	H	A+B	A+B	AB	AB minus 1
H	H	L	L	Logic "0"	A plus A	Logic "1"	A plus A
H	H	L	H	$A\overline{B}$	AB plus A	$A+\overline{B}$	$(A+B)$ plus A
H	H	H	L	AB	$A\overline{B}$ plus A	A+B	$(A+\overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

* Expressed as two's complements. For arithmetic function with C_n in the opposite state, the resulting function is as shown plus 1.

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14582B

LOOK-AHEAD CARRY BLOCK

The MC14582B is a CMOS look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. The device is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table shown below.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- High Speed Operation — 140 ns typical @ V_{DD} = 10 Vdc (from Data-in to Carry-out)
- Expandable to any Number of Bits
- Noise Immunity = 45% of V_{DD} typical
- All Buffered Outputs
- Low Power Dissipation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC EQUATIONS

$C_{n+x} = \overline{G0} + (\overline{P0} \bullet C_n)$

$C_{n+y} = \overline{G1} + (\overline{P1} \bullet \overline{G0}) + (\overline{P1} \bullet \overline{P0} \bullet C_n)$

$C_{n+z} = \overline{G2} + (\overline{P2} \bullet \overline{G1}) + (\overline{P2} \bullet \overline{P1} \bullet \overline{G0}) + (\overline{P2} \bullet \overline{P1} \bullet \overline{P0} \bullet C_n)$

$\overline{G} = \overline{G3} + (\overline{P3} \bullet \overline{G2}) + (\overline{P3} \bullet \overline{P2} \bullet \overline{G1}) + (\overline{P1} \bullet \overline{P2} \bullet \overline{P3} \bullet \overline{G0})$

$\overline{P} = \overline{P3} \bullet \overline{P2} \bullet \overline{P1} \bullet \overline{P0}$

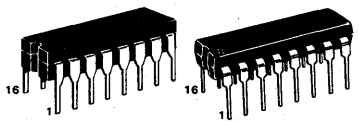
PIN DESIGNATIONS

DESIGNATION	PIN NO's	FUNCTION
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	3,1,14,5	Active-Low Carry-Generate Inputs
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	4,2,15,6	Active-Low Carry-Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y} C_{n+z}	12,11,9	Carry Outputs
$\overline{G}$	10	Active-Low Group Carry-Generate Output
$\overline{P}$	7	Active-Low Group Carry-Propagate Output

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

LOOK-AHEAD CARRY BLOCK



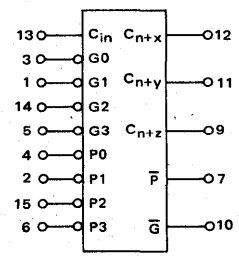
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.4 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.8 µA/kHz) f + I_{DD}							
		15	I_T = (4.3 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types		Unit
			Typical	Maximum	
Output Rise Time	t_r				ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	360	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	130	
Output Fall Time	t_f				ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}				ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 260 ns		5.0	345	690	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 107 ns		10	140	280	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	110	220	

*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

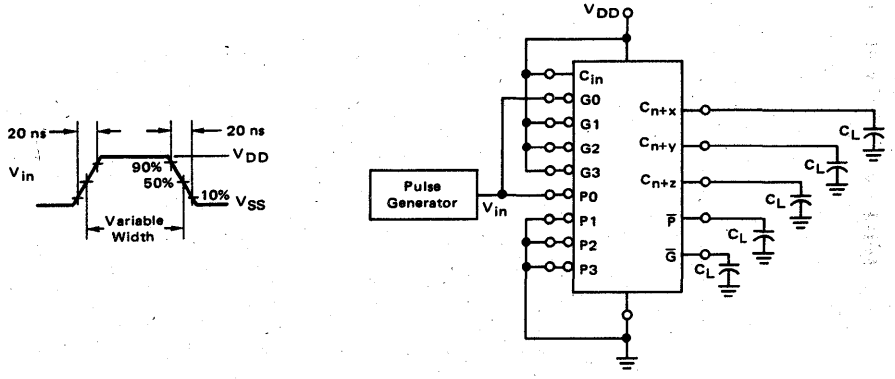


FIGURE 2 – SOURCE CURRENT TEST CIRCUIT

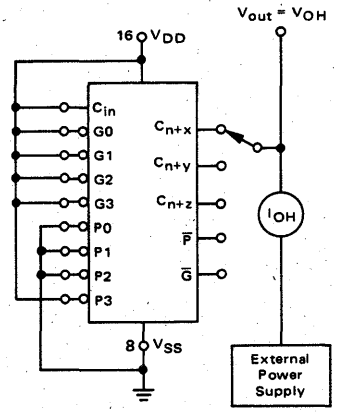


FIGURE 3 – SINK CURRENT TEST CIRCUIT

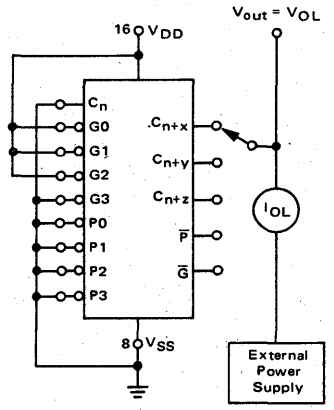
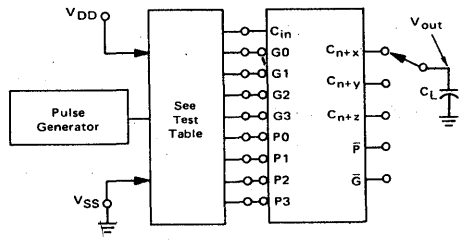
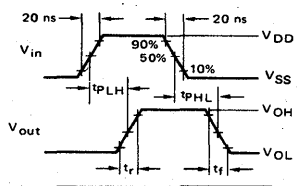


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

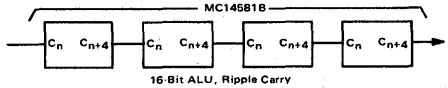


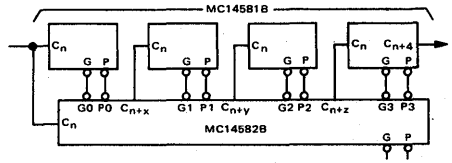
TEST TABLE

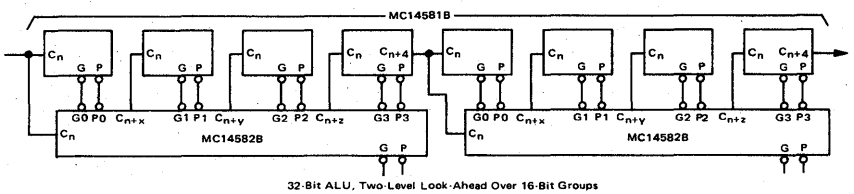
AC PATHS		DC DATA	
INPUT	OUTPUT	To V_{SS}	To V_{DD}
$\overline{P}0$	$\overline{P}$	Remaining $\overline{P}$'s, C_n	G's
$\overline{G}0$	$\overline{G}$	P's, C_n	Remaining $\overline{G}$'s
C_n	C_{n+x}, C_{n+y} C_{n+z}	$\overline{P}$'s	$\overline{G}$'s

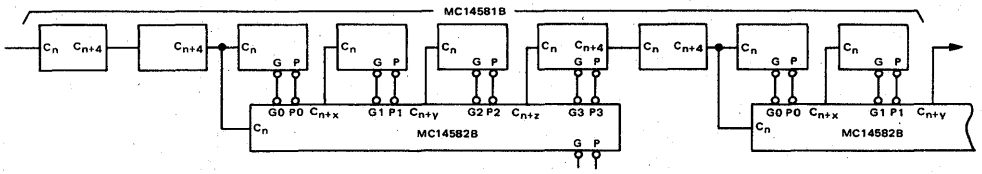


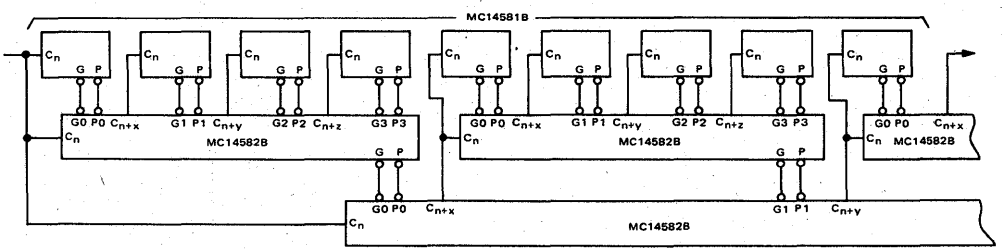
TYPICAL APPLICATIONS











A and B inputs and F outputs are not shown (MC14581B).

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14583B

DUAL SCHMITT TRIGGER

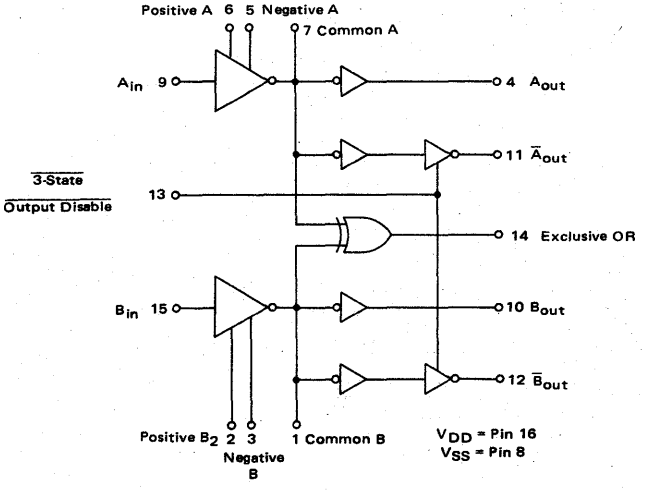
The MC14583B is a dual Schmitt trigger constructed with complementary P-channel and N-channel MOS devices on a monolithic silicon substrate. Each Schmitt trigger is functionally independent except for a common 3-state input and an internally-connected Exclusive OR output for use in line receiver applications. Trigger levels are adjustable through the positive, negative, and common terminals with the use of external resistors. Applications include the speed-up of a slow waveform edge in interface receivers, level detectors, etc.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Schmitt Trigger Input Noise Immunity = 60% of V_{DD} Typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Resistor Adjustable Trigger Levels

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

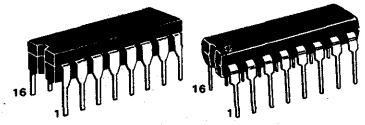
LOGIC DIAGRAM



McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL SCHMITT TRIGGER



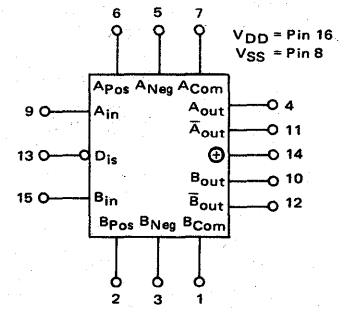
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS				
A	B	$\overline{Dis}$	A_{out}	$\overline{A}_{out}$	B_{out}	$\overline{B}_{out}$	⊕
0	0	0	0	R	0	R	0
0	0	1	0	1	0	1	0
0	1	0	0	R	1	R	1
0	1	1	0	1	1	0	1
1	0	0	1	R	0	R	1
1	0	1	1	0	0	1	1
1	1	0	1	R	1	R	0
1	1	1	1	0	1	0	0

R = High resistance at output

5

ELECTRICAL CHARACTERISTICS (R1 = R2 = ∞)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# A and B "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.05	–	0.0005	0.05	–	1.5	μAdc
(Per Package)		10	–	0.10	–	0.0010	0.10	–	3.0	
		15	–	0.20	–	0.0015	0.20	–	6.0	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	3.8	μAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	9.5	
		15	–	4.0	–	0.0015	4.0	–	15	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.33 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.65 μA/kHz) f + I_{DD}							
		15	I_T = (3.98 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

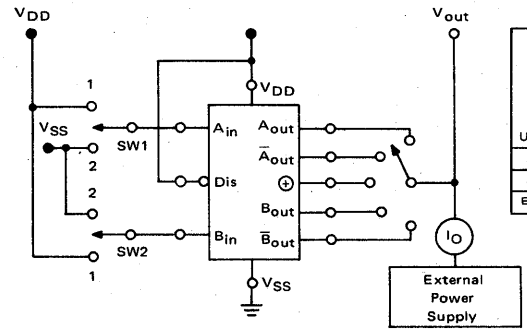
Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}							ns
A_{in},B_{in} to A_{out},B_{out}								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	–	–	650	990	1600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	–	230	345	550	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	–	150	260	365	
A_{in},B_{in} to $\overline{A}_{out}$,$\overline{B}_{out}$	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1015 ns		5.0	–	–	1100	1650	2700	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 347 ns		10	–	–	380	570	800	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 235 ns		15	–	–	260	400	610	
A_{in},B_{in} to Exclusive OR	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns		5.0	–	–	750	1125	1850	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 257 ns		10	–	–	280	420	675	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	–	170	300	470	
3-State Enable, Disable Delay Time	t_{on}, t_{off}							ns
t_{on}, t_{off} = (1.7 ns/pF) C_L + 140 ns		5.0	–	–	225	340	525	
t_{on}, t_{off} = (0.66 ns/pF) C_L + 57 ns		10	–	–	90	135	200	
t_{on}, t_{off} = (0.5 ns/pF) C_L + 30 ns		15	–	–	55	85	140	
Positive Threshold Voltage	V_P	5.0	–	–	3.30	–	–	Vdc
(R1, R2 = 5.0 kΩ)		10	–	–	5.70	–	–	
		15	–	–	8.20	–	–	
Negative Threshold Voltage	V_N	5.0	–	–	1.70	–	–	Vdc
(R1, R2 = 5.0 kΩ)		10	–	–	4.30	–	–	
		15	–	–	6.80	–	–	
Hysteresis Voltage	V_H	5.0	1.27	0.85	1.70	2.55	3.40	Vdc
(R1, R2 = 5.0 kΩ)		10	1.05	0.70	1.40	2.10	2.80	
		15	1.05	0.70	1.40	2.10	2.80	
Threshold Voltage Variation, A to B	ΔV_T	5.0	–	–	0.1	–	–	Vdc
(R1, R2 = 5.0 kΩ)		10	–	–	0.15	–	–	
		15	–	–	0.20	–	–	

*The formula given is for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

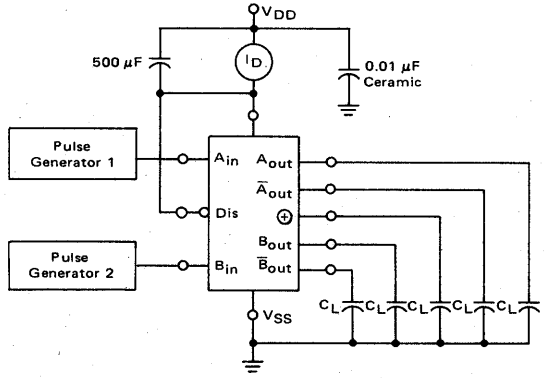
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CHARACTERISTICS TEST CIRCUIT



OUTPUT UNDER TEST	OUTPUT SOURCE CHARACTERISTICS		OUTPUT SINK CHARACTERISTICS	
	TEST VALUE $V_{GS} = -V_{DD}$, $V_{DS} = V_{out} - V_{DD}$		TEST VALUE $V_{GS} = V_{DD}$, $V_{DS} = V_{out}$	
	SWITCH POSITION		SWITCH POSITION	
	SW1	SW2	SW1	SW2
A_{out}, B_{out}	1	1	2	2
$\bar{A}_{out}$, $\bar{B}_{out}$	2	2	1	1
Exclusive OR	1	2	1	1

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



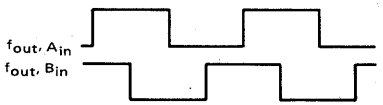
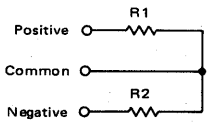
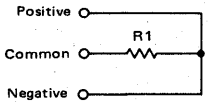


FIGURE 3 – TYPICAL THRESHOLD POINTS

A – Feedback scheme for independent threshold adjustment:



B – Feedback scheme for hysteresis adjustment:



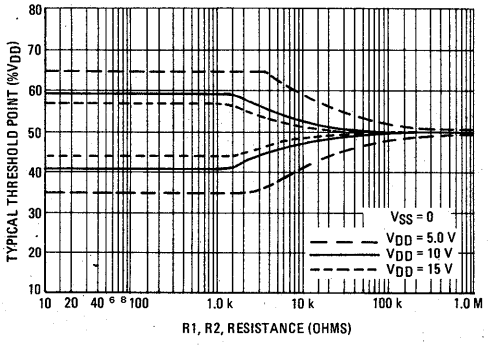
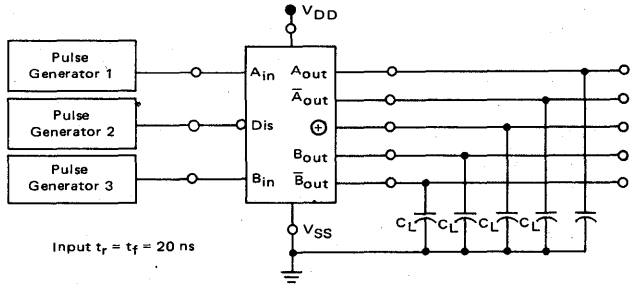
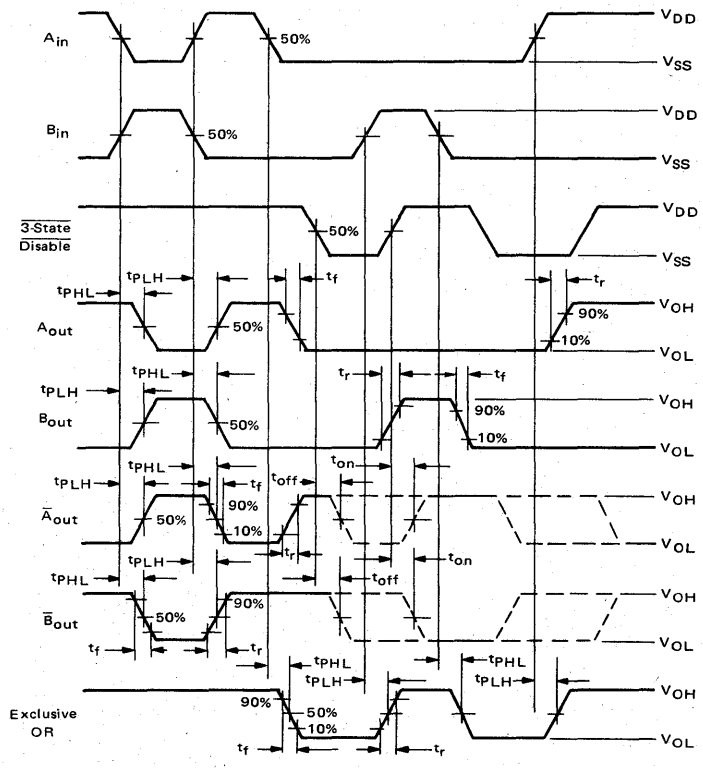


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

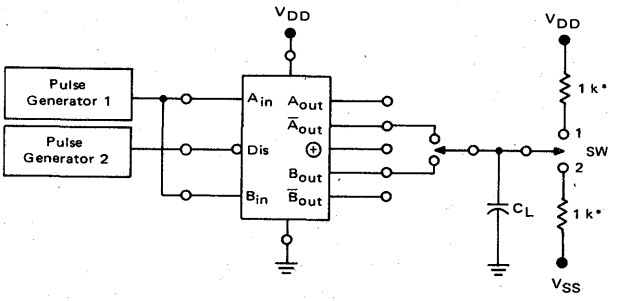




Note: Dashed lines indicate high output resistance.

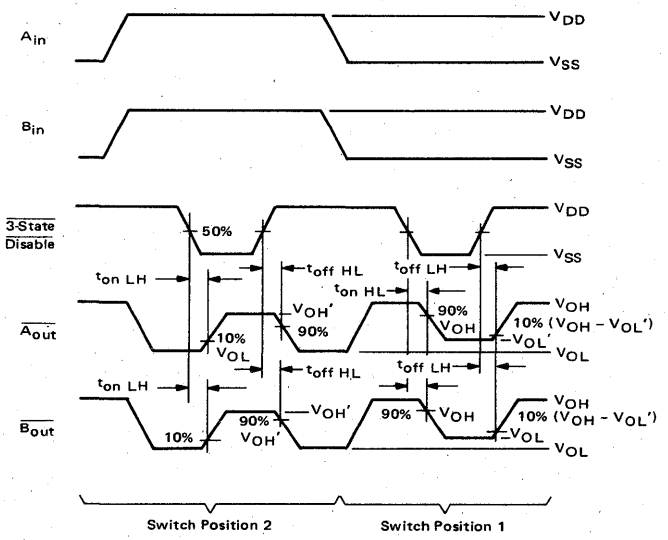
5

FIGURE 5 – 3-STATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	SWITCH POSITION
t_{on} HL	1
t_{on} LH	2
t_{off} HL	2
t_{off} LH	1

*Metal film, ± 1%, 1/4 W or greater
C_L = 15 pF, which includes test circuit capacitance.



V_{OL}' and V_{OH}' refer to the levels present as a result of the 1 k ohm load resistors.

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BOX 20912 • PHOENIX, ARIZONA 85036

MC14584B

Advance Information

McMOS SSI

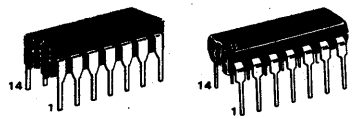
(LOW-POWER COMPLEMENTARY MOS)

HEX
SCHMITT TRIGGER

HEX SCHMITT TRIGGER

The MC14584B hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14584B may be used in place of the MC14069B hex inverter for enhanced noise immunity or to "square up" slowly changing waveforms.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD40106B and MM74C14
- Can Be Used to Replace MC14069B



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

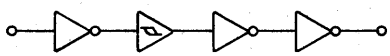
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

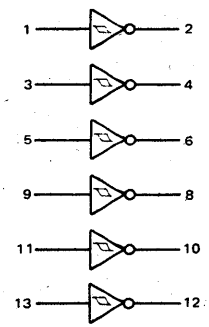
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

EQUIVALENT CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This is advance information and specification are subject to change without notice.

5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
(V_{OH} = 9.5 Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	
(V_{OH} = 13.5 Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–2.5	–	–2.1	–4.2	–	–1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.52	–	–0.44	–0.88	–	–0.36	–	
(V_{OH} = 9.5 Vdc)		10	–1.3	–	–1.1	–2.25	–	–0.9	–	
(V_{OH} = 13.5 Vdc)		15	–3.6	–	–3.0	–8.8	–	–2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	34	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.8 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.6 µA/kHz) f + I_{DD}							
		15	I_T = (5.4 µA/kHz) f + I_{DD}							
Hysteresis Voltage	V_H	5.0	–	–	–	0.4	–	–	–	Vdc
		10	–	–	–	0.45	–	–	–	
		15	–	–	–	0.9	–	–	–	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_r	5.0 10 15		100 50 40		ns
Output Fall Time	t_f	5.0 10 15		100 50 40		ns
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0 10 15		160 65 50		ns

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

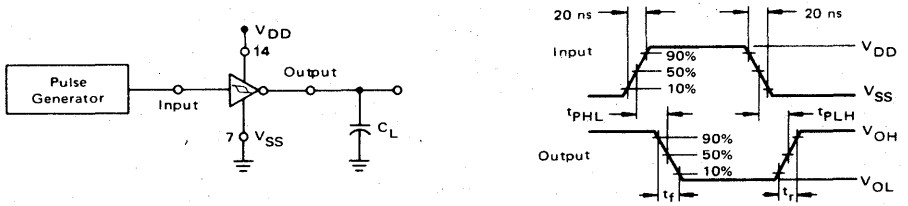
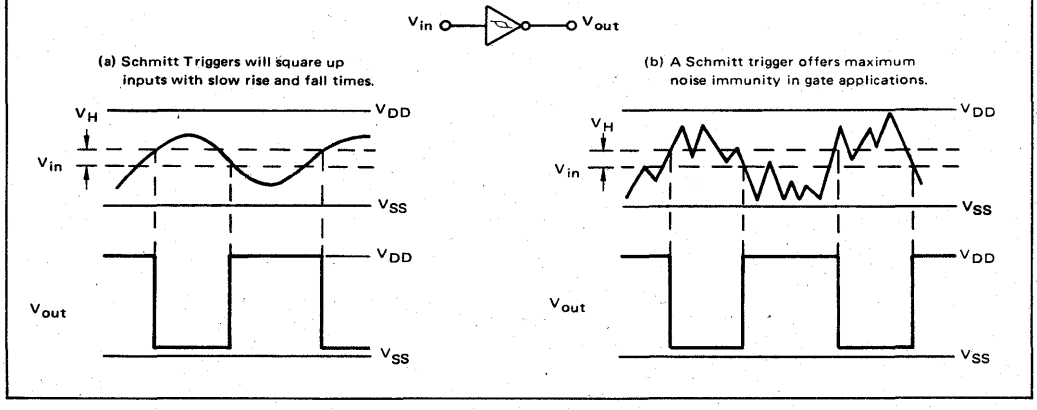


FIGURE 2 – TYPICAL SCHMITT TRIGGER APPLICATIONS



MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14585B

4-BIT MAGNITUDE COMPARATOR

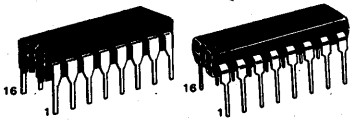
The MC14585B 4-Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs (A<B, A=B, and A>B), and three outputs (A<B, A=B, and A>B). This device compares two 4-bit words (A and B) and determines whether they are "less than", "equal to", or "greater than" by a high level on the appropriate output. For words greater than 4-bits, units can be cascaded by connecting outputs (A<B), and (A=B) to the corresponding inputs of the next significant comparator (input A>B is connected to a high). Inputs (A<B), (A=B), and (A>B) on the least significant (first) comparator are connected to a low, a high, and a high, respectively.

Applications include logic in CPU's, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- High Fanout > 50
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Expandable
- Applicable to Binary or 8421-BCD Code
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

McMOS MSI
(LOW POWER COMPLEMENTARY MOS)

4-BIT MAGNITUDE COMPARATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

5

MAXIMUM RATINGS (Voltages referenced to V_{SS})

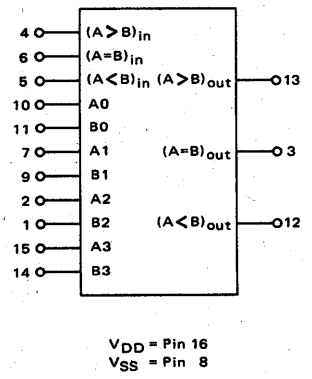
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	X	X	X	X	X	1	0	0	1
A3=B3	A2>B2	X	X	X	X	1	0	0	1
A3=B3	A2=B2	A1>B1	X	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	X	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	X	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	1	0	0

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.6 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.2 µA/kHz) f + I_{DD}							
		15	I_T = (1.8 µA/kHz) f + I_{DD}							

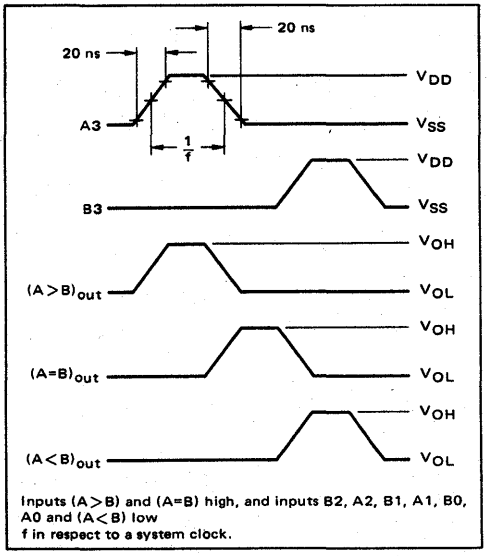
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	65	110	160	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	37	55	80	
Turn-Off Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 345 ns		5.0	430	750	1125	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	180	300	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	130	220	330	

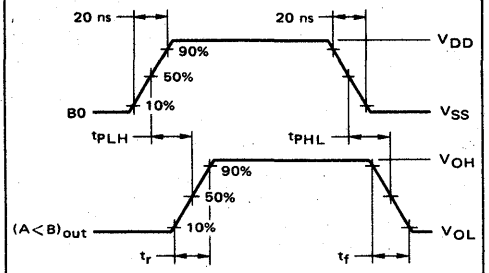
*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS



Inputs (A>B) and (A=B) high, and inputs B2, A2, B1, A1, B0, A0 and (A<B) low
f in respect to a system clock.

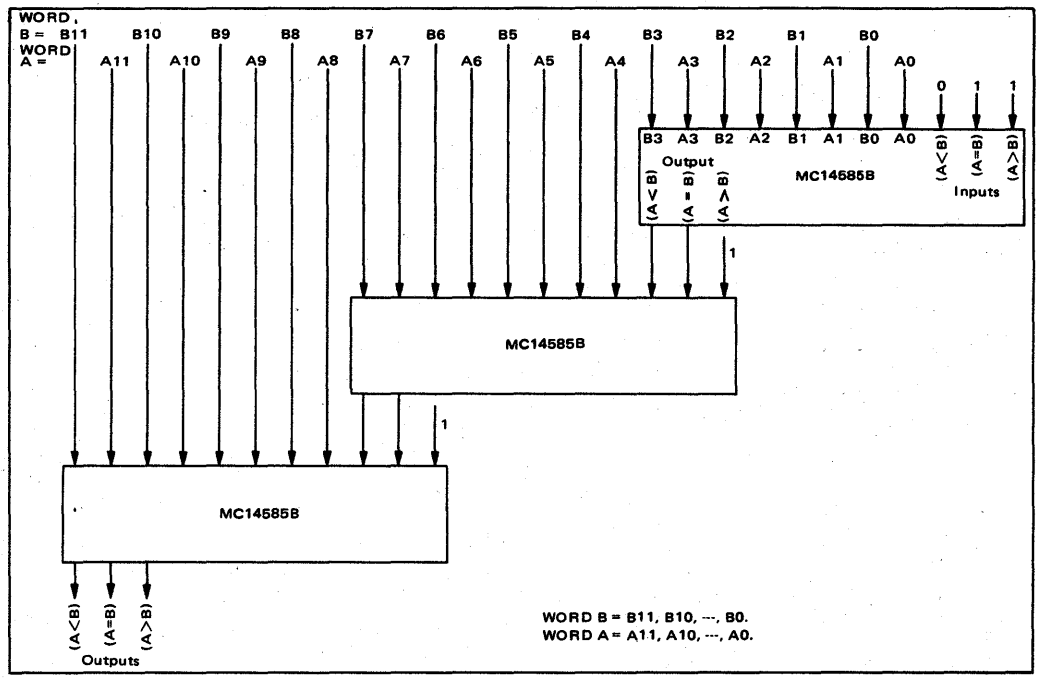
FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



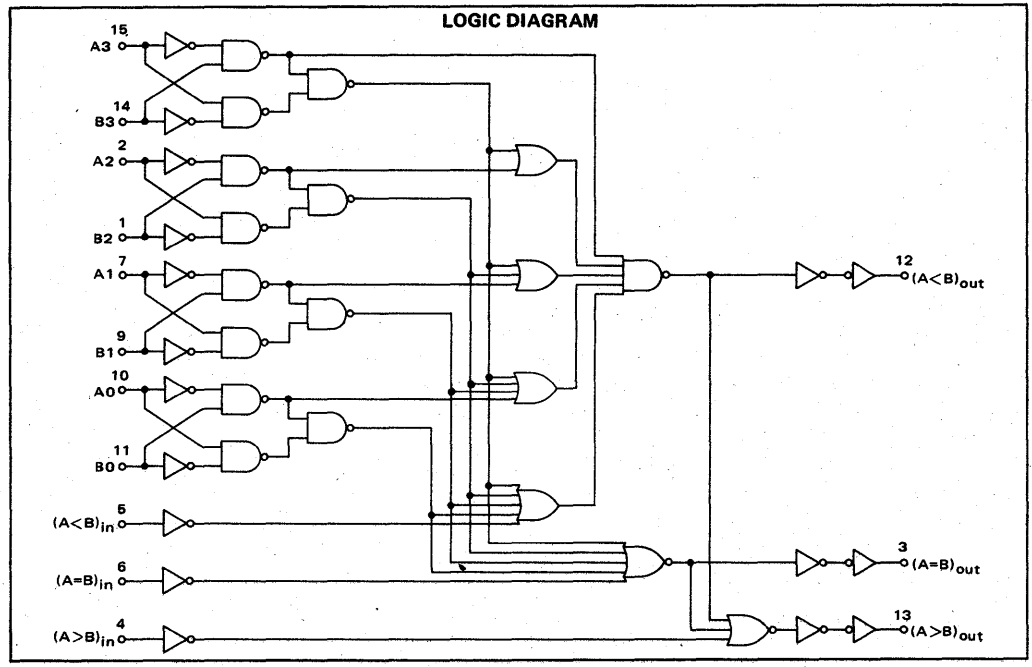
Inputs (A>B) and (A=B) high, and inputs B3, A3, B2, A2, B1, A1, A0, and (A< B) low.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 3 – CASCADING COMPARATORS



LOGIC DIAGRAM



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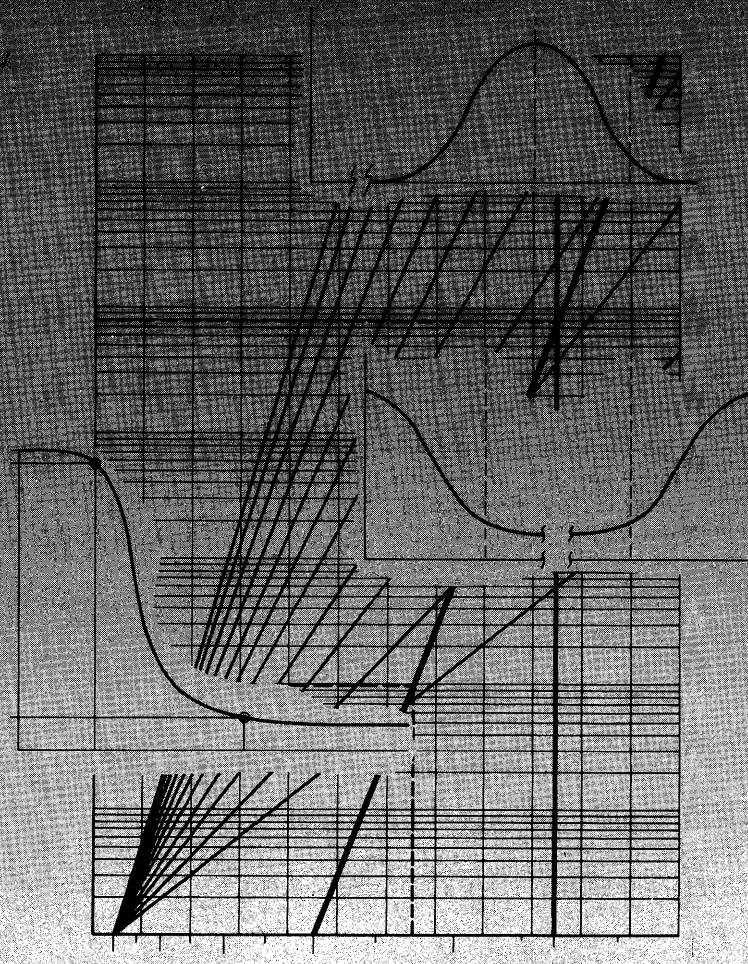

CMOS Reliability/Chapter 6

McMOS Reliability

Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of troublefree service it can offer. The reliability of a device is exactly that — an expression of how well it will serve the customer. The following discussion will attempt to present an overview of Motorola's MOS Reliability efforts.

BASIC CONCEPTS

It is essential to begin with an explanation of the various parameters of reliability. These are probably summarized best in the Bathtub Curve (Figure 1). The reliability performance of a device is characterized by three phases: infant mortality, random failure and wearout. When a device is produced there is often a small distribution of failure mechanisms which will exhibit themselves under relatively moderate stress levels and therefore appear early. This period of early failures, termed infant mortality, can often be reduced significantly through proper manufacturing controls and screening techniques. The most effective period is that in which only occasional random failure mechanisms appear. This typically spans a long period of time with a very low failure rate. The final period is that in which the devices literally wear out due to continuous phenomena which existed at the time of manufacture. Using reasonable design techniques and selectivity in applications, this period can easily be shifted beyond the lifetime required by the user.

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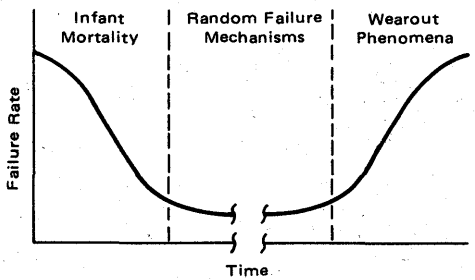
FIGURE 1 — THE BATHTUB CURVE



Random Failure

Both the infant mortality and random failure rate regions can be described through the same types of calculations. During this time the probability of having no failures to a specific point in time can be expressed by the equation

$$P_o = e^{-\lambda t}$$

where λ is the failure rate and t is time. Since λ is changing rapidly during infant mortality, the expression does not become useful until the random period, where λ is relatively constant. In this equation λ is failures per unit of time. It is usually expressed in percent failures per thousand hours. Other forms include FIT (Failures In Time = [%/10^3 hrs] x 10^{-4} = 10^{-9} failures per hour) and MTTF (Mean Time To Failure) or MTBF (Mean Time Between Failures), both being equal to $1/\lambda$ and having units of hours.

Since reliability evaluations usually involve only samples of an entire population of devices, the concepts of the Central Limit Theorem apply and λ is calculated using the χ^2 distribution through the equation:

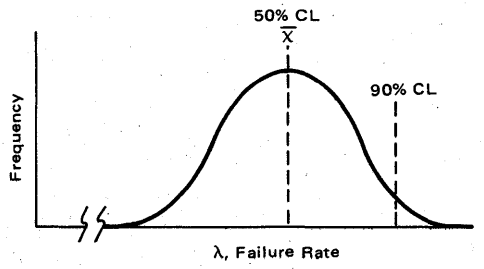
$$\lambda \leq \frac{\chi^2 (\alpha, 2r + 2)}{2nt}$$

where $\alpha = \frac{100-CL}{100}$

CL = Confidence Limit in percent
r = Number of rejects
n = Number of devices
t = Duration of test

The confidence limit is the degree of conservatism desired in the calculation. The Central Limit Theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher λ which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 2). The term (2r + 2) is called the degrees of freedom and is an expression of the number of rejects in a form suitable to χ^2 tables.

FIGURE 2 — CONFIDENCE LIMITS AND THE DISTRIBUTION OF SAMPLE FAILURE RATES



The number of rejects is a critical factor since the definition of rejects often differs between manufacturers. While Motorola uses data sheet limits to determine failures, sometimes rejects are counted only if they are catastrophic. Due to the increasing chance of a test not being representative of the entire population as sample size and test time are decreased, the χ^2 calculation produces surprisingly high values of λ for short test durations even though the true long term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long term failure rate. Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing has shown that temperature will accelerate failures and that this behavior fits the form of the Arrhenius equation:

$$R(t) = R_0(t)e^{-\theta/kT}$$

where $R(t)$ = Reaction rate as a function of time and temperature
R_0 = A constant
t = Time
θ = Activation energy in electon volts
k = Boltzman's constant
T = Temperature in degrees Kelvin

To provide time-temperature equivalents this equation is applied to failure rate calculations in the form

$$t = t_0\, e^{\theta/kT}$$

where
t = time
t_0 = A constant

The Arrhenius equation essentially states that reaction rate increases exponentially with temperature. This produces a straight line when plotted on log-linear paper with a slope expressed by θ. θ may be physically interpreted as the energy threshold of a particular reaction or failure mechanism. The activation energy exhibited by MOS integrated circuits varies from about 0.7 eV for serious contamination problems to about 1.3 eV. Although the relationships do not prohibit devices from having poor failure rates and high activation energies, good performance usually does imply a high θ. Studies by Bell Telephone Laboratories have indicated that an overall θ for semiconductors is 1.0 eV. This value has been accepted by the Rome Air Development Command for time-temperature acceleration in powered burn-in as specified in Method 1015.1 of MIL-STD-883A. Data taken by Motorola on MOS devices has verified this number and it is therefore applied as our standard time-temperature regression for extrapolation of high temperature failure rates to temperatures at which the devices will be used (Figure 3).

To accomplish this, the time in device hours (t1) and temperature (T1) of the test are plotted as point P1. A vertical line is drawn at the temperature of interest (T2) and a line with a 1.0 eV slope is drawn through point P1. Its intersection with the vertical line defines point P2, and determines the number of equivalent device hours (t2). This number may then be used with the χ^2 formula to determine the failure rate at the temperature of interest. Assuming T1 of 125°C at t1 of 10,000 hours, a t2 of 7.8 million hours results at a T2 of 50°C. If one reject results in the 10,000 device hours of testing at 125°C, the failure rate at that temperature will be 20%/1000 hours using a 60% confidence level. One reject at the equivalent 7.8 million device hours at 50°C will result in a 0.026%/1000 hour failure rate, as illustrated in Figure 4.

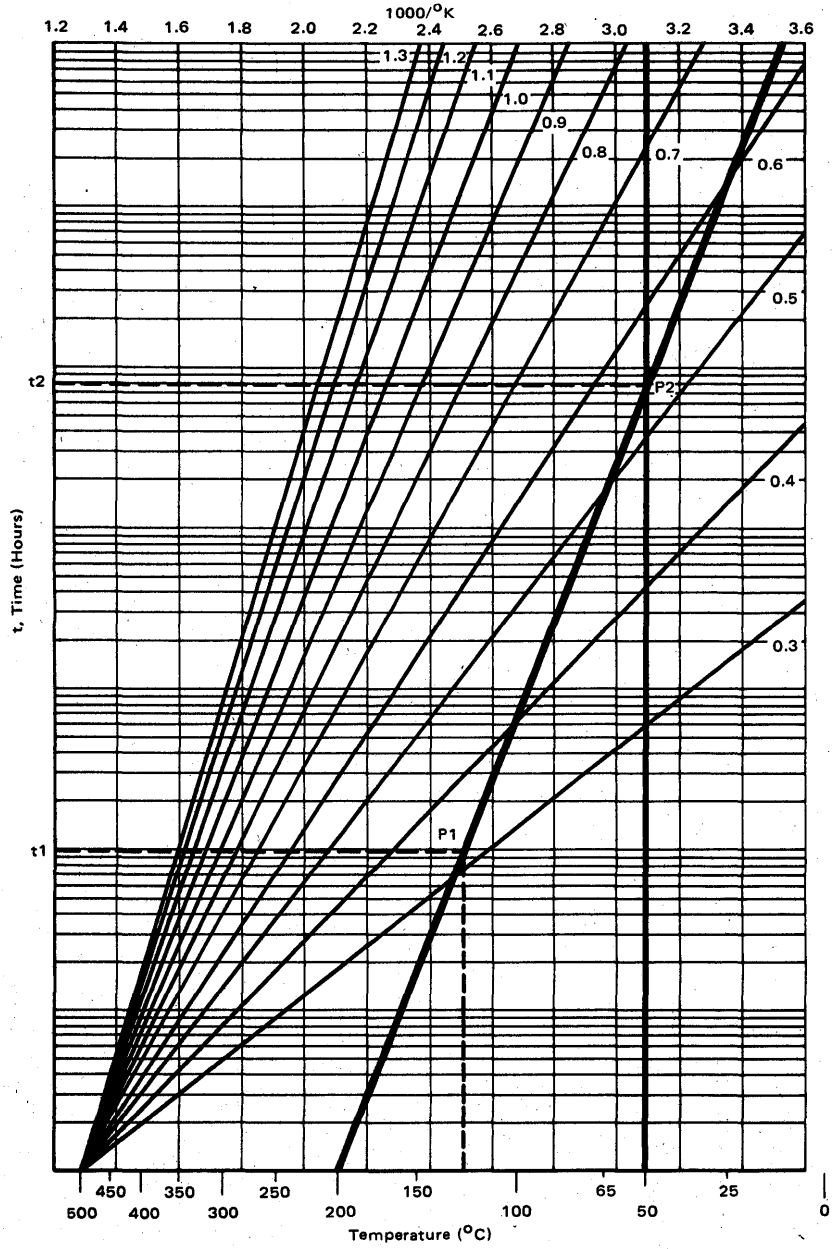
Three parameters determine the failure rate quoted by the manufacturer: the failure rate at the test temperature, the activation energy employed, and the difference between the test temperature and the temperature of the quoted λ. A term often used in this manipulation is the "acceleration factor" which is simply the equivalent device hours at the lower temperature divided by the actual test device hours.

Wearout

Every device will eventually fail, but with reasonable care in design and application the wearout phase can be extended far beyond the lifetime required. During wearout, as in infant mortality, the failure rate is changing rapidly and therefore loses its value. The parameter used to describe performance in this area is "Median Life" and is the point at which 50% of the devices have failed. There are currently only two significant wearout mechanisms: electromigration of circuit metallization and electrolytic corrosion in plastic devices.

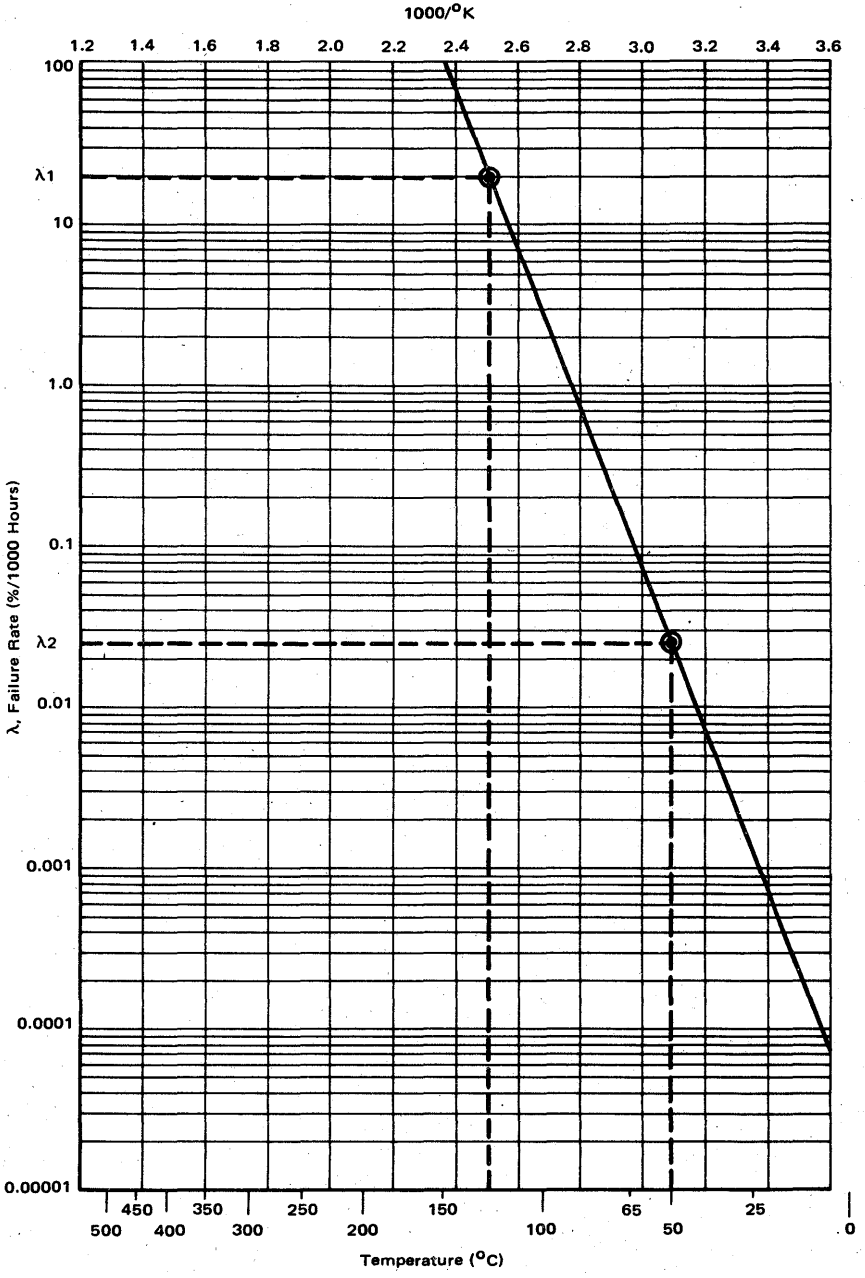
Electromigration is the current induced mass transport of metallization due to high temperature and current density. It is strongly affected by the type of metallization as well as the grain structure and surface sealing. It is therefore important that the designer predict the maximum junction temperature of the device, the current on all space limited lines and the process characteristics such as thickness variation, grain size, and step coverage. With these parameters fixed, a median life goal can be selected and the metal width chosen accordingly. Reasonable consideration in the design phase coupled with careful die inspection can therefore eliminate this phenomena as one of practical concern.

FIGURE 3 – NORMALIZED TIME-TEMPERATURE REGRESSIONS FOR VARIOUS ACTIVATION ENERGY VALUES



For increased flexibility in working with a broad range of device hours, the time-temperature regression lines have been normalized to 500°C and the time scale omitted, permitting the user to define the scale based on his own requirements.

FIGURE 4 – FAILURE RATE



A more pertinent mechanism is the electrolytic corrosion of die metallization by moisture and applied voltage. Although it can occur in hermetic packages which are not properly sealed, hermeticity testing can easily limit it to plastic packaging. In plastic devices there is never enough adhesion between the plastic and the other components to overcome the stresses developed due to differing coefficients of thermal expansion. As a result moisture can enter the device along the interface of the lead frame and the plastic, pass between the surface of the wire and the plastic and reach the surface of the die. If contaminants are present in the water or in the package an electrolyte is created which will corrode the metallization in the presence of an electric field. The median life is determined by many factors such as:

1. Matching of thermal expansion coefficients of the leadframe, wire, die and plastic
2. Purity of the encapsulant
3. Adhesion of the encapsulant
4. Length and width of the leadframe interface
5. Integrity of the final die passivation layer.

Plastic package corrosion is evaluated by exposing the device to extremes of temperature and humidity while under bias. Through consistent bias configurations and control of the environment, temperature-humidity-bias (THB) testing can be an invaluable indicator of performance. Typical test parameters are 85°C and 85% relative humidity. Pressure cooker test and operating tests under tropical conditions are also employed but are more difficult to repeat consistently. The problem with all the tests, however, is the difficulty in relating the results to the environment in which the customer will use the device. To accomplish this a model has been developed which substitutes vapor pressure for temperature in the Arrhenius equation. When available data points are used to adjust the constants, the plot in Figure 5 is the result. Based on several variations of THB conditions and extrapolated performance from burn-in tests, this model provides a good estimate of performance across the range of temperature and humidity environments possible in the customers application.

Sampling Procedures

There are primarily three methods of measuring how well a lot of product meets the quality and reliability requirements of the customer: 100% testing using a Percent Defective Allowable (PDA), sampling based on an Acceptance Quality Limit (AQL), and sampling based on a Lot Tolerance Percent Defective (LTPD). Since 100% testing is time consuming and expensive, sampling procedures are typically employed to assure acceptably low defect levels.

A PDA is simply a reject percentage above which the lot will be rejected. Depending on how the PDA was derived, it may or may not be statistically sound. The availability of theoretically accurate sampling plans in the various military specifications has led to wide use of AQL and LTPD plans. Depending on lot size and sample size, three different probability distributions may be used to derive the sampling plan: the Binomial, the Hypergeometric and the Poisson. The assumptions of a particular sample size (n) and acceptance number (c) and the use of these distributions will generate an Operating Characteristic (OC) Curve as in Figure 6. The AQL is defined at the 95% probability of lot acceptance level while the LTPD is defined at the 10% level. The AQL point describes the Producer's Risk of rejecting good lot (5%) while the LTPD point describes the Consumer's Risk of accepting bad lot (10%) given that the incoming product contains the percent defective p.

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FIGURE 5 – VAPOR PRESSURE MODEL

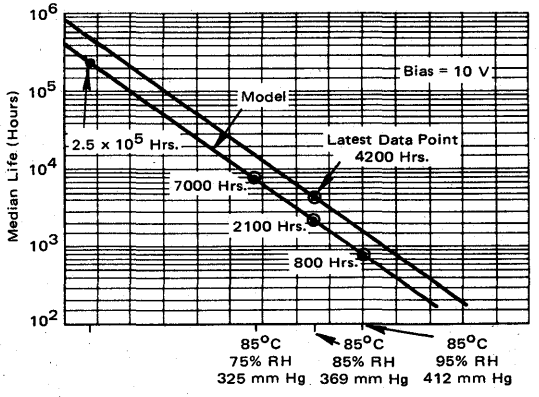
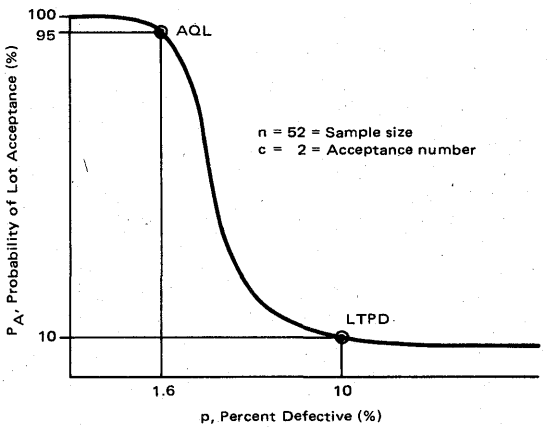


FIGURE 6 – OPERATING CHARACTERISTIC CURVE



It is important to remember that although the concepts of Producer's and Consumer's Risk are utilized to describe AQLs and LTPDs, both are merely indicators of the performance of the original population. Both plans are widely used by manufacturers and users alike. By definition, LTPDs employ fixed sample sizes while AQL plans adjust the sample size according to the lot size. As in the case of failure rate determination, the criteria established to determine rejects and their interpretation are key factors in determining the performance of lots during inspection.

THE SOURCE OF RELIABILITY

One of the most popular sayings about reliability is that it must be "built in", not "tested in". Every manufacturing process exhibits a distribution of quality and reliability. The intent of the saying is that this distribution must be controlled to assure a high mean value, a narrow range and a consistent shape. Through proper design and process control this can be accomplished, thereby reducing the task of screening programs which attempt to eliminate the lower tail of the distribution.

Design

A close interface must be maintained between reliability and design. For this reason a large part of the reliability staff is dedicated to a day by day interface with the device design and modeling groups. Through this mutual effort new techniques are evaluated and proven before they are committed to production. Special test vehicles are generated and experiments performed to verify that the performance of new approaches meets or exceeds the standards of the product line. This effort is not only a beneficial application of reliability but an absolute necessity to provide the rapid product development demanded by the dynamic integrated circuit marketplace.

Processing

In addition to the design interface, reliability engineers work closely with process engineers in both the wafer and assembly areas. As each new process is developed, it is also tested to assure that it presents no hazards to the reliability of the ultimate product. This testing is an extensive qualification program which is performed independently on processes, packages and designs.

New wafer processes are qualified using process control patterns and prototypes of production devices. Each new package is tested using methods based on MIL-STD-883A. Assembly process changes are qualified by employing them in the construction and testing of well characterized products. After these primary level qualifications, wafer processes are generically qualified in new packaging systems to assure process-package compatibility. While assembly oriented qualifications center around the thermal-mechanical sequences of MIL-STD-883A, wafer process qualifications emphasize dynamic high temperature stress testing. (see Figures 7 and 8.)

After testing has proven the performance of the process, it is specified and documented to provide a baseline for process control. Beyond the detailed process control efforts of the process engineering groups, an In-Process Quality Assurance (IPQA) group exists to assure that process control is meeting its objectives. IPQA accomplishes this through surveillance of both the wafer and assembly areas (see Figure 9). There are two major inspection points in the wafer processing areas: CV Plotting and Final Visual. Samples from each wafer lot are stringently tested for voltage shift and inspected for gold backing and visual defects. The major inspection points in the Assembly Area are Die Visuals, Die Bond, Wire Bond and Pre-Cap.

FIGURE 7 – PACKAGE EVALUATION

Test	MIL-STD-883 Test Method	Test Condition
Operating Life	1005	N/A
High Temperature Storage	1008	C
Temperature Cycle	1010	C
Thermal Shock	1011	C
Thermal Resistance	N/A	N/A
Mechanical Shock	2002	B
Constant Acceleration	2001	D
Vibration, Variable Frequency	2007	A
Wire Pull (Hermetic)	2011	D
Temperature-Humidity-Bias (Plastic)	N/A	85°C/85% RH/10V
Moisture Resistance	1004	1
Salt Atmosphere	1009	A
Solderability	2003	260°C
Lead Fatigue	2004	B2
Marking Permanency	2008	B
Physical Dimensions	2008	A

All of these inspection points are known as "Gate Inspections" and are performed on lots of material. Wafers are grouped into lots which generally consist of thirty to fifty wafers while individual devices are grouped into assembly orders consisting of 500 to 2000 devices. Each lot or assembly order is submitted to In-Process Quality Assurance Gate Inspection. If accepted, they are passed to the next operation, while failed material is returned to Production for 100% screening. Only the wafers or devices that meet all established standards are accepted for continued processing.

"Monitor" inspections are performed in the assembly area on each individual machine and operator. The monitors are designed to control the operation, and provide feedback of quality problems to the responsible production supervision. Periodic line audits are used to check for:

1. Documented procedures on each operation
2. Proper usage of specifications
3. Up-to-date calibration of equipment
4. Proper settings on equipment
5. Housekeeping
6. Safety precautions.

Comprehensive training programs are provided for all domestic and off-shore personnel, new plant start-ups, changes in specifications, or process changes. The primary objective is to evaluate the material in process and assure that MOS products meet the levels of reliability and quality which are consistent with the requirements of our customers.

FIGURE 8 – INITIAL EVALUATION OF NEW PRODUCT

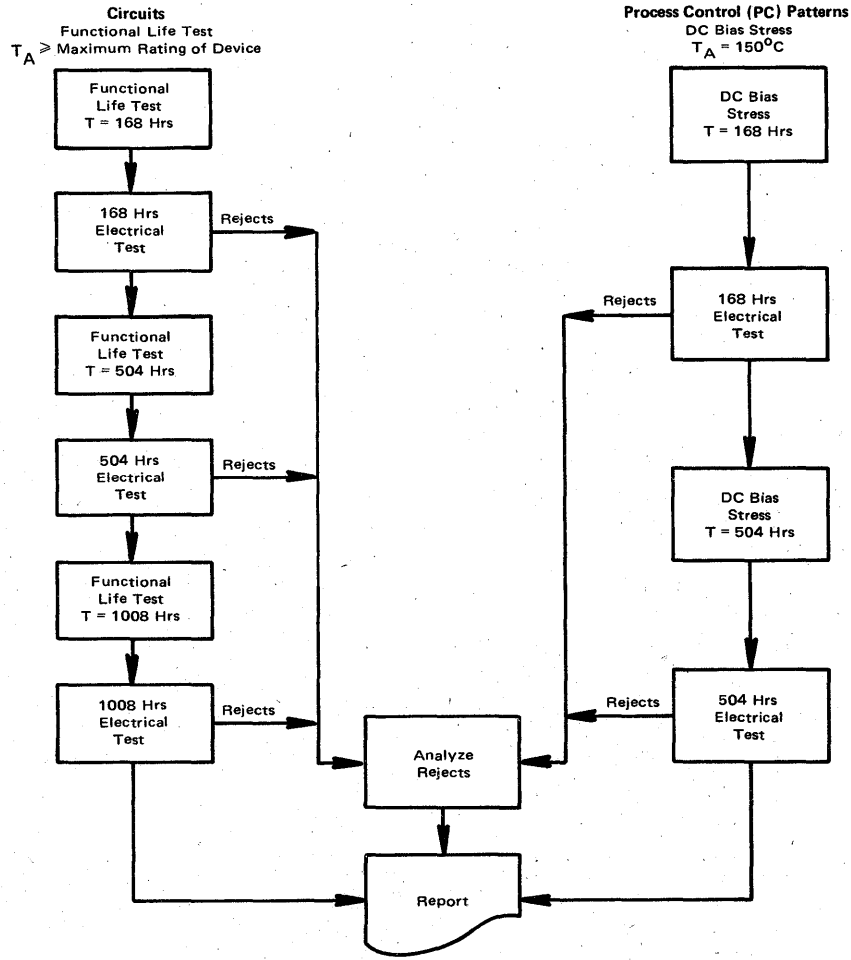
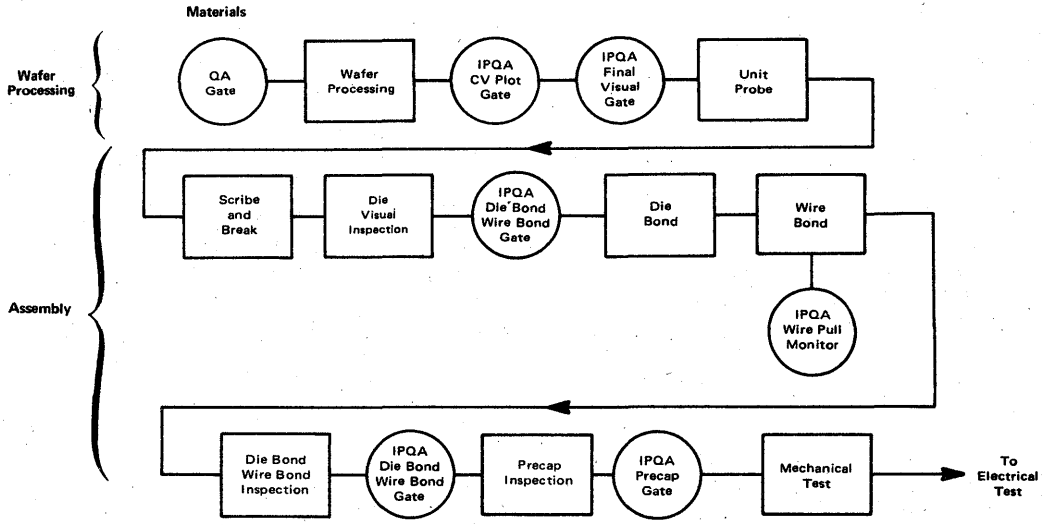


FIGURE 9 – IN-PROCESS QUALITY ASSURANCE FLOW CHART



SCREENING

During the past thirty years that semiconductor products have existed, a wide variety of screening techniques have evolved to eliminate the lower tail of the process distribution discussed previously. These techniques may be categorized in two ways, as illustrated by the two axes of the matrix in Figure 10. The performing agency varies depending on the type and purpose of the test. Most screens utilized by the industry today are based on MIL-STD-883A and are employed by Motorola in the various categories of Figure 10.

Several 100% visual screens are performed during assembly using both stereozoom and metallurgical microscopes. Subsequent sampling is performed by In-Process Quality Assurance as described above. Assembly mechanical tests for hermetic product consist of:

1. Gross leak sampling
2. Temperature cycling
3. Krypton-85 fine leak testing.

Other tests available as adders include stabilization bake and centrifuge. Stabilization bake originated with Mesa transistors which had exposed junctions. The high temperature bake had a significant effect on stabilizing the junction leakage and low current beta. Since integrated circuits have no exposed junctions, Motorola has found no benefit in stabilization bake. The intent of centrifuge is to exert a force on the wire bonds which would detect latent failures. Calculations have shown that even at 30,000 Gs, a higher than normal military requirement, the force on a wire is in the order of 100 mg. This is insignificant compared to a wire pull average of at least 7000 mg. Since each wire bonder is sampled continuously to provide constant control, centrifuge becomes a needless screen. Occasionally die bonds can fail in a centrifuge test, but Motorola controls this factor by employing stringent fillet and wetting criteria in a 100% visual screen enforced by In-Process QA.

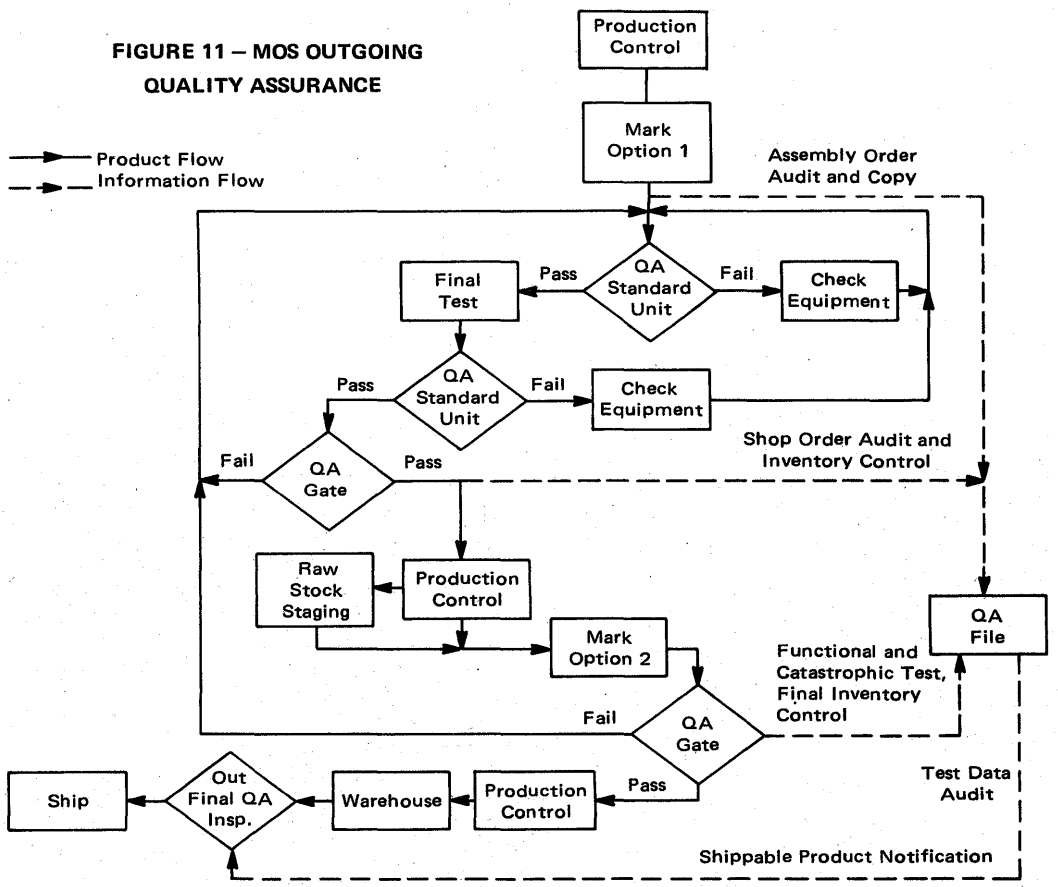
FIGURE 10 – TESTING CATEGORIES

Category	Visual Inspection	Mechanical Testing	Environmental Stress
100%	Assembly	Assembly	Production Burn-In
Sampling	In-Process QA	In-Process QA Outgoing QA	Outgoing QA
Qualification Testing	Reliability Engineering		

Many vendors offer extensive screening programs as an adder. Although some features definitely improve reliability, many are far from cost effective. As in the case of stabilization bake and centrifuge for hermetics, many unnecessary screens are applied to plastic product. Stabilization bake is often touted as a screening procedure for plastics, but this is usually the standard cure cycle through which every plastic device is processed. Temperature cycling and thermal shock are tests commonly employed to test for latent wire bond failures. This was a significant problem when the industry was using aluminum wire on various silicone compounds, and continues to be for those vendors who have not properly balanced the thermal expansion coefficients of the package components. Motorola, like many of the large suppliers, has spent years of research and testing in optimizing its epoxy Novolac plastic package to the extent that temperature intermittence has been virtually eliminated. In addition, recent work by Fitch* has shown that repeated temperature excursions over the military temperature range definitely degrade the THB life of plastic product.

At the end of the assembly process, production final test screens the product with a comprehensive series of dc, functional, and speed oriented electrical tests. These tests are normally more stringent than data sheet requirements and are sampled by Outgoing Quality Assurance. Outgoing QA establishes controls on the equipment, procedures and test programs. Through the use of such monitoring and standard correlation units, this In-Line Quality System (Figure 11) certifies that each unit has been screened to program limits such that all specifications are met or exceeded. Complementing the In-Line systems is a statistical sampling program based on MIL-STD-883A, Method 5005.2. This Group A inspection to Class B levels is detailed in Figure 12.

FIGURE 11 – MOS OUTGOING QUALITY ASSURANCE



*Fitch, William and Carpenter, Marvin: The Effect of Thermal Shock and High Temperature Storage on the Temperature Humidity Bias Life of Plastic Encapsulated TTL Gates, RLC #1239 Motorola Integrated Circuit Reliability Report.

FIGURE 12 – GROUP A ELECTRICAL TESTS[1]

Subgroups [2]	Class B LTPD	AQL
Subgroup 1 Static tests at 25°C	*5/1	0.46
Subgroup 2 Static tests at maximum rated operating temperature	7/2	1.1
Subgroup 3 Static tests at minimum rated operating temperature	7/2	1.1
Subgroup 4 Dynamic tests at 25°C	5/2	0.78
Subgroup 5 Dynamic tests at maximum rated operating temperature	7/2	1.1
Subgroup 6 Dynamic tests at minimum rated operating temperature	7/2	1.1
Subgroup 7 Functional tests at 25°C	*5/1	0.46
Subgroup 8 Functional tests at maximum and minimum rated operating temperatures	10/2	1.6
Subgroup 9 Switching tests at 25°C	7/2	1.1
Subgroup 10 Switching tests at maximum rated operating temperature	10/2	1.6
Subgroup 11 Switching tests at minimum rated operating temperature	10/2	1.6

1 The specific parameters to be included for tests in each subgroup shall be as specified in the applicable procurement document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test to satisfy Group A requirements.

2 A single sample may be used for all subgroup testing.

*Combined subgroups 1 and 7.

In addition to these two programs, all MOS product lines are monitored continuously via an MOS Ongoing Reliability Evaluation (MORE) Program for mechanical, environmental and operating life performance. This program evaluates the most recently manufactured product on a scheduled basis with methods derived from MIL-STD-883A (see Figure 13). MORE provides current generic data for process control feedback and, just as important, a "no charge" assurance of compliance to military quality standards for all MOS products.

When necessary, production burn-in is performed on particular device types. Burn-in procedures are always available at competitive adders. Qualification testing by Reliability Engineering has been described, and Motorola's reliability data is presented in the following section.

SYSTEM IMPLEMENTATION

Assessing System Requirements

The reliability needs of each system and application differ significantly, so the various aspects of component performance must be analyzed separately. The two parameters which should be addressed initially are infant mortality and long term random failure rate. Systems with large numbers of components require greater component reliability. Infant mortality should be estimated and used to calculate service costs. This data should be balanced against the cost of a functional burn-in and possibly a board or system burn-in. Long term reliability goals should be established for the system and used to calculate the necessary long term failure rate for the components. Long term failure rates cannot be effectively improved by short burn-ins unless they include infant mortality failures. (Infant mortality is included in Motorola's data.) Infant mortality can be effectively screened by short term accelerated stress testing such as a 24 to 48 hour high temperature functional burn-in. The concepts defined earlier can be used to relate the burn-in to equivalent system hours. Often, customers who are experiencing problems fail to distinquish between infant mortality, long term reliability and wearout. It is imperative that failure patterns be sufficiently investigated and recorded to accomplish this. Buying a Hi Rel device will not solve a problem caused by poor handling or an unforseen overstress in the application.

The system environment should be given careful consideration when choosing between plastic and hermetic packages. Sustained high temperature and humidity will accelerate the corrosion

wearout mechanism in plastic according to the model in Figure 5. Office environments, however, will rarely produce a detectable difference in plastic and hermetic packages. Since the die and wire bonding systems are totally encapsulated in plastic, these packages can often outperform hermetics for both thermal conductivity, and mechanical shock and vibration resistance. The potential for moisture condensation should be evaluated in light of the lead material and finish, whether the package is hermetic or plastic. Unusually moist or contaminated atmospheres can rapidly corrode ferrous metals under bias, regardless of the finish material.

Cost effectiveness is also influenced by the number of defective units received by the customer. For various reasons, a small percentage of product is defective as received. This may be due to handling, correlation, shipping damage or a host of minor difficulties. The percentage of these defects should be less than one percent and any significant levels should be discussed with the vendor immediately.

Comparing Competitors' Data

Every manufacturer has a slightly different method of generating his reliability data. It is therefore difficult for a user inexperienced in reliability calculations to make a valid comparison. Toward this end the concepts introduced earlier will be of great value. The following list should be verified before any conclusions of vendor superiority are drawn.

1. Confidence limit
2. Reject criteria (degradation, data sheet, functional, catastrophic, specific mechanisms)
3. Temperature of test
4. Activation energy
5. Distortion of failure rate due to a low number of device hours
6. Biasing configuration
7. Test monitoring (system failures can produce impressive results due to less stringent stress being applied to the device).

Only if all these factors are considered can a truly objective comparison be made.

FIGURE 13A – PRODUCTION LINE PROCESS EVALUATION
(Independent of package unless otherwise noted)

Test	Condition or Procedure
Subgroup A1 Electrical dc and Functional	All parameters per detail device specification at 25°C ± 5°C. (Go/No go)
Subgroup A2 Electrical dc and Functional	Critical parameters per detail device specification at minimum and maximum rated operating temperature. (Go/No go)
Subgroup A3 Electrical Switching	Critical switching parameters per detail device specification at 25°C ± 5°C. (Go/No go)
Subgroup A4 Electrical Continuity	Plastic package only; all pins at 125°C. (Go/No go)
Subgroup C1 Storage Life End Points: Electrical	1000 hours at maximum rated storage temperature. Functional and dc at 25°C ± 5°C; read and record at 168 hours, 500 hours, 1000 hours, and each 1000 hours until termination.
Subgroup C2 Operating Life or Steady State Bias End Points: Electrical	1000 hours minimum at maximum rated operating temperature. Conditions specified per device type in 12MRB06389A. Functional and dc at 25°C ± 5°C; read and record at 168 hours, 500 hours, 1000 hours, and each 1000 hours until termination.
Subgroup C3 Accelerated Steady State Life End Points: Electrical	48 hours minimum at 200°C static. Burn-in circuit per 12MRB06389A (CMOS ceramic only). Functional and dc parameters at 25°C ± 5°C. Read and record.

FIGURE 13B – HERMETIC PACKAGE EVALUATION

Test	Method	MIL-STD-883A Condition or Procedure
Subgroup B1		
Solderability	2003.1	Temperature = 260°C maximum. Omit Aging.
Subgroup B2		
Lead Fatigue	2004.1	Condition B2
Subgroup B3		
Seal	1014.1	
a. Fine		Condition B
b. Gross		Condition C2. Omit vacuum of Step 2.
Subgroup B4		
Physical Dimensions	2016	Per case outline drawing
Subgroup B5		
Marking Permanency	2015	Resistance to solvent
Subgroup B6		
Bond Strength	2011.1	Test Condition D
Subgroup C1		
Thermal Shock	1011.1	Condition B (15 cycles)
Temperature Cycle	1010.1	Condition C (30 cycles)
End Points:		
Seal	1014.1	
a. Fine		Condition B
b. Gross		Condition C2. Omit vacuum of Step 2.
Continuity	–	All pins at 25°C ± 5°C
Visual	–	Any crack at 10X magnification
Subgroup C2		
Mechanical Shock	2002.1	Condition B (Y1 axis only)
Vibration, Variable Frequency	2007	Condition A (Y axis only)
Constant Acceleration	2001.1	Condition E (Y1 axis only)
End Points:		
Seal	1014.1	
a. Fine		Condition B
b. Gross		Condition C2. Omit vacuum of Step 2.
Continuity	–	All pins at 25°C ± 5°C
Visual	–	Any crack at 10X magnification
Subgroup C3		
Salt Atmosphere	1009.1	Condition A

FIGURE 13C – PLASTIC PACKAGE EVALUATION

Test	Method	MIL-STD-883A Condition or Procedure
Subgroup B1		
Solderability	2003.1	Temperature = 260°C ± 10°C. Omit Aging.
Subgroup B2		
Lead Fatigue	2004.1	Condition B2
Subgroup B4		
Physical Dimensions	2016	Per case outline drawing
Subgroup B5		
Marking Permanency	2015	Resistance to solvent
Subgroup C1		
Thermal Shock	1011.1	Condition A (15 cycles)
Temperature Cycle	1010.1	Condition A (15 cycles)
End Points:		
Continuity	–	All pins at 125°C ± 5°C
Visual	–	Any crack at 10X magnification
Subgroup C2		
Mechanical Shock	2002.1	Condition B (Y1 axis only)
Vibration, Variable Frequency	2007	Condition A (Y axis only)
Constant Acceleration	2001.1	Condition E (Y1 axis only)
End Points:		
Continuity	–	All pins at 125°C ± 5°C
Visual	–	Any crack at 10X magnification
Subgroup C3		
Salt Atmosphere	1009.1	Condition A
Subgroup C4		
Temperature/Humidity/Bias	–	85°C/85% RH/10 V
End Points:		
DC and Functional	–	25°C Go/No go. Read and record rejects at 168 hours, 500 hours, 1000 hours, 1250 hours, 1500 hours.
Continuity	–	All pins at 125°C

Motorola Data

Motorola MOS failure rates are generated by dynamic high temperature stress testing at the maximum ratings of the device, or higher. A 60% confidence level is employed in the standard χ^2 calculation and the Arrhenius model, with a 1.0 eV activation energy, is used to extrapolate the data to typical operating temperatures. 1.0 eV was chosen based on the work done at Bell Telephone Laboratories, its acceptance by the Rome Air Development Command for MIL-STD-883B, and its consistency with our MOS data. Failure rates for CMOS are shown in Figures 14a, b, and c.

To assure data representative of the CMOS family, samples are randomly taken from standard production lots which have completed all standard processing and electrical testing. No special processing or electrical testing is conducted. The results presented are based on long-term life testing of the following device types within each logic category:

Gates	Arithmetic Functions	Memories	Decoders	Flip-Flops	Latches	Buffers/ Inverters	Special Functions	Shift Registers	Counters/ Timers	Multiplexers/ Data Selectors
MC14001	MC14008	MCM14505	MC14511	MC14013	MC14508	MC14049	MC14532	MC14006	MC14022	MC14016
MC14002	MC14585		MC14514	MC14027		MC14050	MC14583	MC14021	MC14040	MC14512
MC14007									MC14510	MC14519
MC14011									MC14518	MC14539
MC14012									MC14520	
MC14023										
MC14025										
MC14501										
MC14506										

All incremental electrical tests are performed to production final test limits (data sheet limits). Results include both catastrophic failures (non-functional) and degradation failures (functional devices which do not meet data sheet specifications).

Based on long-term life test data, the current failure rates indicated are:

6

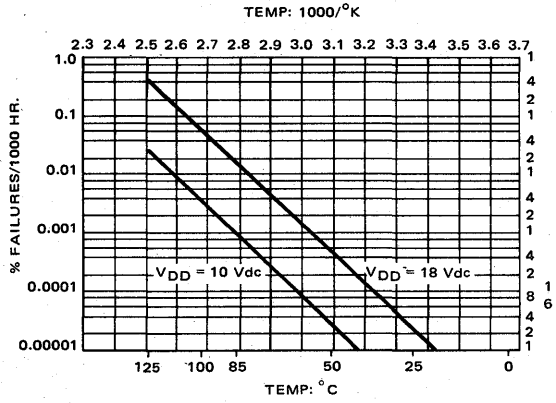
Device Series	Operating Voltage	85°C Failure Rate	125°C Failure Rate	See Figure
AL	18 volts	0.0150%/1000 hrs.	0.432%/1000 hrs.	14
	10 volts	0.00092%/1000 hrs.	0.028%/1000 hrs.	14a
CL	15 volts	0.06%/1000 hrs.	*	14b
	10 volts	0.0132%/1000 hrs.	*	14b
CP	15 volts	0.120%/1000 hrs.	*	14c
	10 volts	0.009%/1000 hrs.	*	14c

*Exceeds data sheet operating temperature limitations

The relationship of failure rate to operating temperature and operating voltage is presented in Graphs 1 (AL series), 2 (CL series), and 3 (CP series).

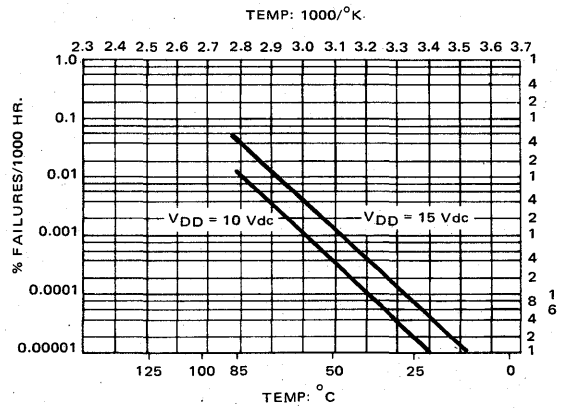
Parametric stability is indicated in the graphs of total device current and threshold drift.

FIGURE 14a – AL SERIES



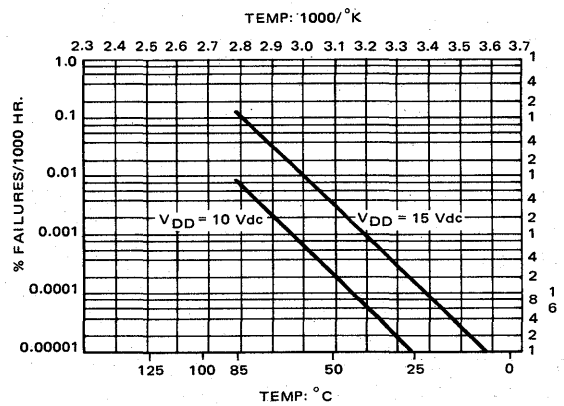
	V_{DD} = 10 Vdc	V_{DD} = 18 Vdc
Device Hours	3,225,190	1,200,000
Rejects	0	4
125°C Failure Rate*	0.028%/1000 hrs.	0.432%/1000 hrs.

FIGURE 14b – CL SERIES



	V_{DD} = 10 Vdc	V_{DD} = 15 Vdc
Device Hours	6,941,040	8,608,000
Rejects	0	4
85°C Failure Rate*	0.0132%/1000 hrs.	0.06%/1000 hrs.

FIGURE 14c – CP SERIES



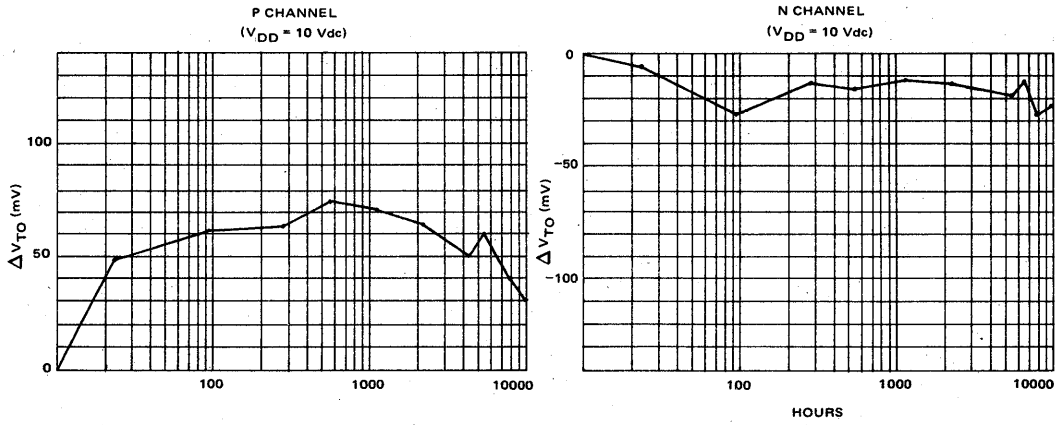
	V_{DD} = 10 Vdc	V_{DD} = 15 Vdc
Device Hours	34,763,042	31,260,454
Rejects	2	36
85°C Failure Rate*	0.009%/1000 hrs.	0.120%/1000 hrs.

*Failure rate at 60% confidence level. Rejects based on data sheet limits. Extrapolations based on an activation energy of 1.0 ev.

6

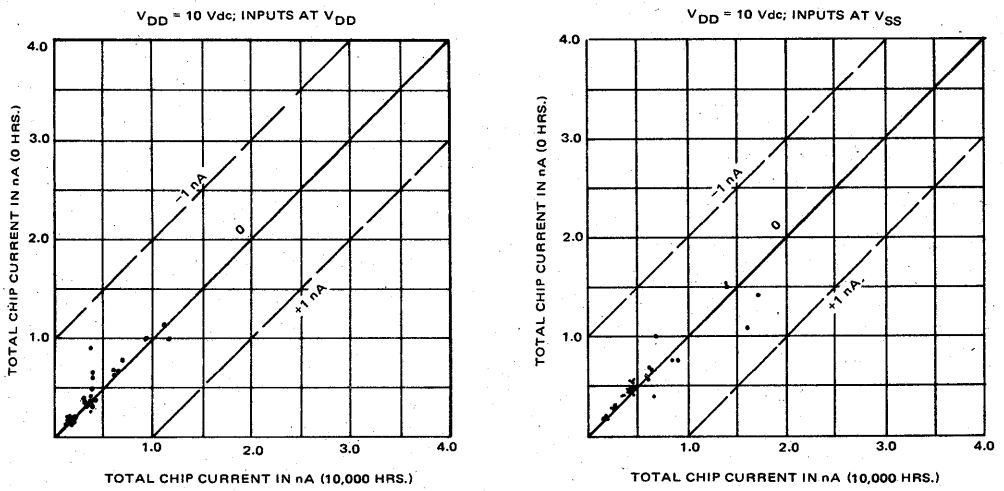
Wafer process variations are continuously monitored by classification probe and capacitance voltage testing in the wafer area, and by MORE sampling in Outgoing Quality Assurance. In addition to this, a system of periodic reliability tests is being implemented with Process Control patterns to establish the process distribution and track significant variations. Current tests with 10 V static bias at 150°C for 10,000 hours produced the plots of threshold stability shown in Figure 15a. Chip current changes after 10,000 hours of life test are shown in Figure 15b.

FIGURE 15a – THRESHOLD VOLTAGE CHANGE VERSUS LIFE TEST HOURS



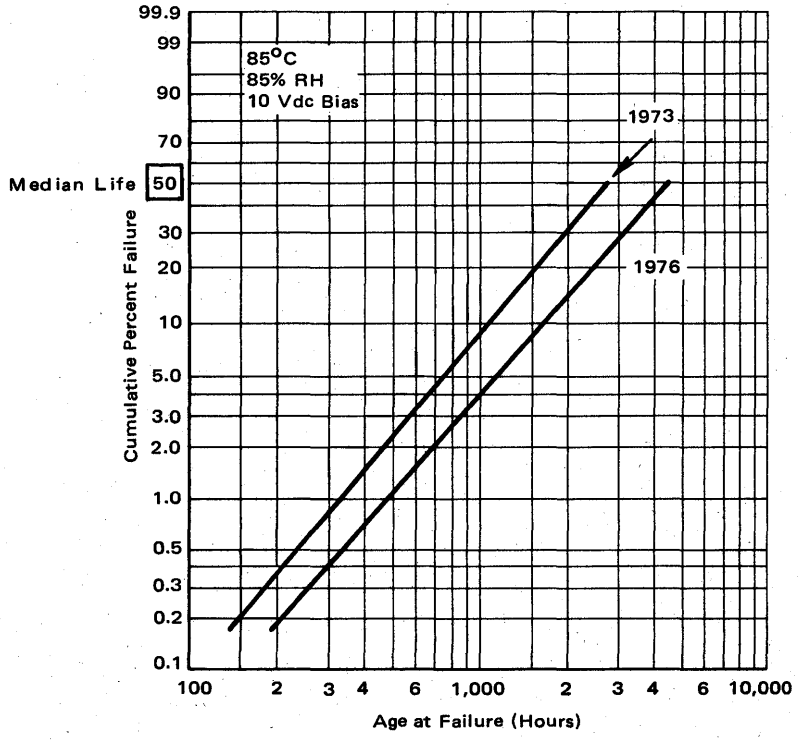
Notes: 1. Electrical Tests @ 25°C
2. Life Tests @ 150°C
3. Data Shown for Dual 4-Input NOR Gates

FIGURE 15b– CHIP CURRENT CHANGE after 10,000 HOUR LIFE TEST



Notes: 1. Electrical Tests @ 25°C
2. Life Tests @ 150°C
3. Data Shown for Dual 4-Input NOR Gates

FIGURE 16 – PERFORMANCE HISTORY
(TEMPERATURE HUMIDITY BIAS, WEIBULL PROBABILITY)



An ongoing improvement program has produced impressive results in plastic package temperature-humidity-bias performance. Based on CMOS testing, the Weibull plots of Figure 16 demonstrate this trend. There is a full two fold increase in median life since the data used to generate the vapor pressure model in Figure 5. Although it is not known if a parallel shift of this curve to the latest 85/85 results (ML = 4200 hours) is justified, the extrapolated performance to normal environments is impressive.

Periodically samples of competitors' product bought from distributors are tested with Motorola methods. To date no other vendor has performed as well as Motorola (see Figure 17). This data was gathered on CMOS product, and is an excellent indicator of the Motorola plastic packaging system.

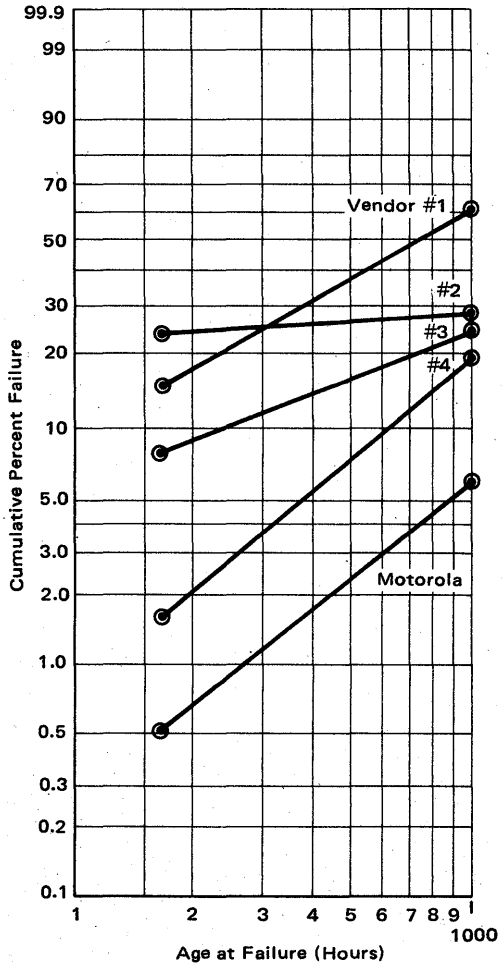
Proper evaluation of rejects and feedback to processing can occur only through intensive failure analysis. To support the processing areas, product groups and R & QA, a Product Analysis Laboratory exists. "State-of-the-art" analytical tools are at its disposal including mass spectrometry, Auger, electron microprobe, scanning electron microscopy (with voltage contrast strobe capability) and others too numerous to mention. This capability is complemented by computer tracking systems to evaluate failure patterns and distributions. A simplified example* is illustrated in the bar chart of Figure 18.

Detailed information on specific device types is available through individual reliability reports. This series also includes program plans, CMOS and N-Channel generic reports and a plastic packaging report.

*Based on test rejects and field failures.

FIGURE 17 – VENDOR COMPARISON

A – Temperature Humidity Bias



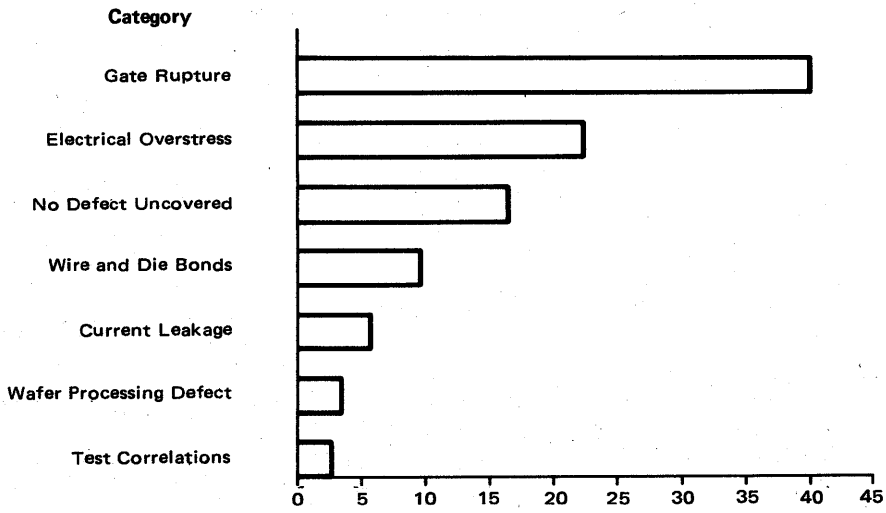
B – Other Testing

Vendor	1000 Hour Burn-In % Failure	Thermal Shock and Temperature Cycling
1	5.7	0
2	44.0	13.3
3	40.0	0
4	12.0	1.8
Motorola	2.3	0

Processing and Handling

No matter how good the reliability data, screening procedures, or incoming inspection, devices are still subject to degradation or destruction by processing and handling. All MOS vendors use input protection devices and most perform well, but there is no device which totally protects the circuit against all conditions. Most users are familiar with good static prevention procedures, but there are few, if any, who could not have prevented a small percentage of in-process failures by a careful review of their assembly lines. A discussion of handling procedures is found in Chapter 3. Every point at which a MOS device is handled apart from its conductive foam or rail should be evaluated. Conductive work surfaces and wrist straps (making contact with skin) should be tied to ground through a nominal one megohm resistor. Test equipment should be checked to assure grounded sockets during insertion and the absence of voltage spikes. Printed circuit board handling should be consistent with device handling using conductive bags or edge connectors. Conformal coating processes (which can extend the application range of plastic) or cleaning procedures should not be overlooked as possible sources of difficulty. Service personnel should be educated in handling procedures since even when service is completed successfully, valuable failure information can be masked by static damage. With reasonable effort very little static damage can be expected, but a review is always worthwhile.

FIGURE 18 – FAILURE CAUSE



Improper board cleaning procedures can often degrade plastic product performance. High purity flourocarbon systems are preferred to water based systems which can more easily introduce contaminants, particularly in the presence of wetting agents. Cooling the device during the clean or pressurized systems can also enhance the entrance of moisture and contaminants into the package along the lead-plastic interface. Even if contaminants are not present, a thorough bake should be performed to prevent premature introduction of an electrolyte.

CONCLUSION

This discussion has attempted to educate the user with the pertinent concepts of reliability, quality assurance, vendor selection and product use. Motorola's reputation for reliability and customer support has been established by the philosophy of its leadership and is being perpetuated through the efforts of MOS Reliability and Quality Assurance. Customer assistance is always available through sales offices, marketing or R & QA personnel directly.

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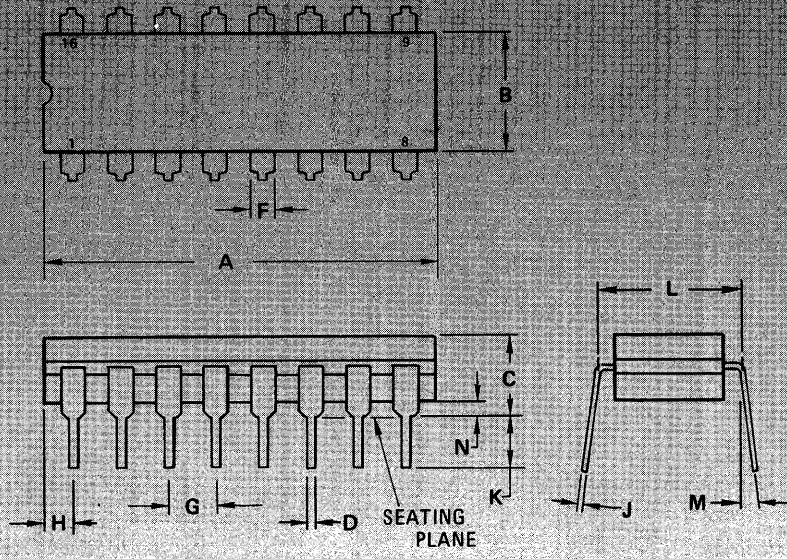
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	2.54	–	0.100	–
L	7.49	8.89	0.295	0.350
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

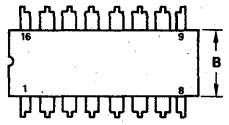


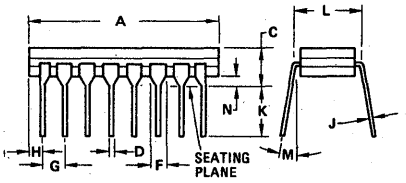
Mechanical Data/Chapter 7

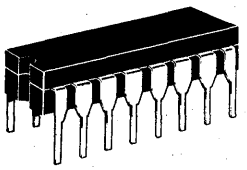
MECHANICAL DATA

The packaging availability for each device is indicated on the individual data sheets. Dimensions for the packages are given in this section. Pin assignment drawings are included in Chapter 8 for convenient reference.

L SUFFIX
CERAMIC PACKAGE
CASE 620





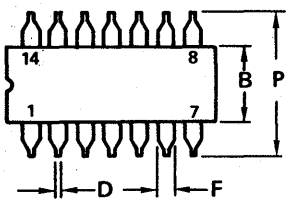


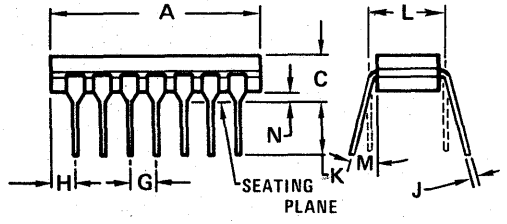
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	2.54	–	0.100	–
L	7.49	8.89	0.295	0.350
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

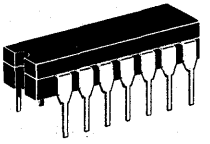
CASE 620-04

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
4. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY)

L SUFFIX
CERAMIC PACKAGE
CASE 632







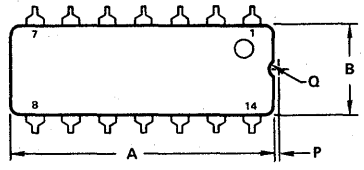
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	2.54	4.06	0.100	0.160
L	7.49	8.89	0.295	0.350
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
2. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY)

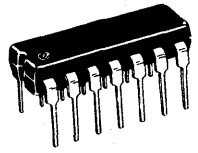
CASE 632-04

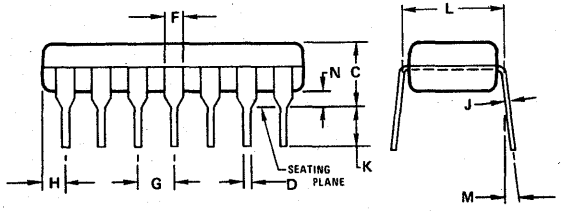
7

P SUFFIX
PLASTIC PACKAGE
CASE 646



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

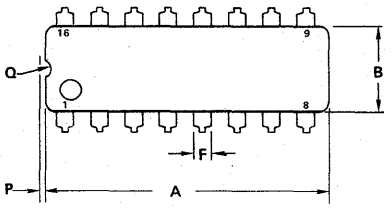




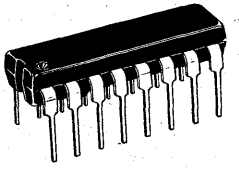
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

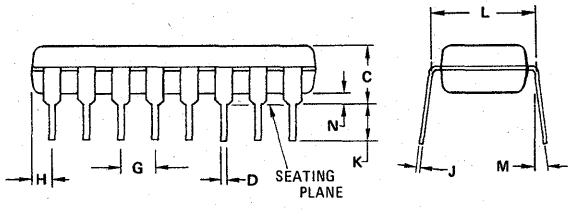
CASE 646-03

P SUFFIX
PLASTIC PACKAGE
CASE 648



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL



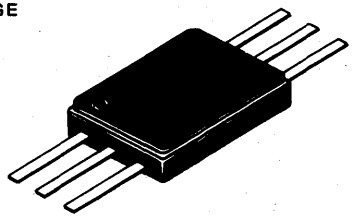


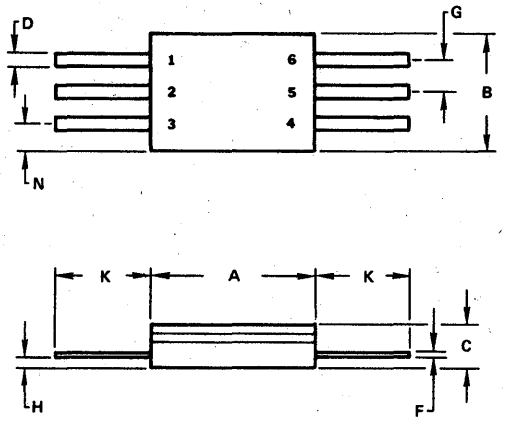
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

CASE 648-03

7

L SUFFIX
CERAMIC PACKAGE
CASE 688



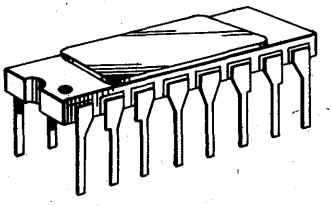


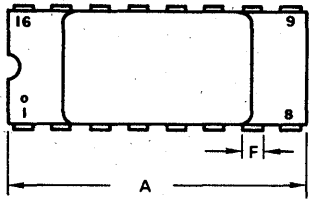
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	7.11	0.235	0.280
B	4.32	5.72	0.170	0.225
C	1.17	1.91	0.046	0.075
D	0.25	0.51	0.010	0.020
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.13	0.89	0.005	0.035
K	1.90	3.05	0.075	0.120
N	0.89	1.52	0.035	0.060

CASE 688-05

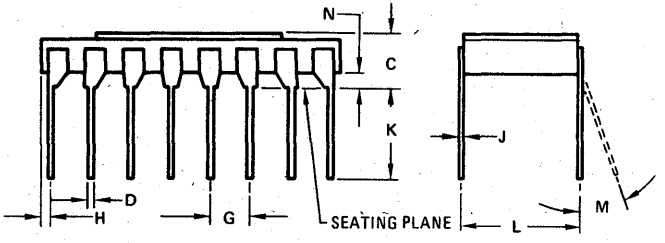
NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.13 mm (0.005) RADIUS TO DIM "A" & "B" AT MAXIMUM MATERIAL CONDITION.

L SUFFIX
CERAMIC PACKAGE
CASE 690





NOTE:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

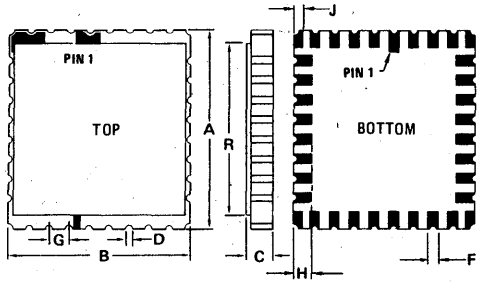


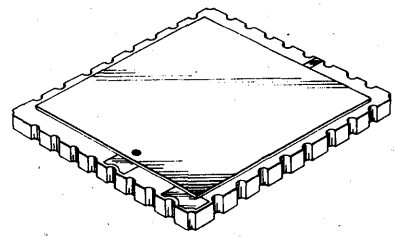
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.07	20.57	0.790	0.810
C	2.67	3.94	0.105	0.155
D	0.38	0.53	0.015	0.021
F	1.22	1.52	0.048	0.060
G	2.54 BSC		0.100 BSC	
H	1.14	1.40	0.045	0.055
J	0.20	0.31	0.008	0.012
K	3.05	4.83	0.120	0.190
L	7.62 BSC		0.300 BSC	
M	–	10^0	–	10^0
N	0.64	1.14	0.025	0.045

CASE 690-08

7

Z SUFFIX
LEADLESS CERAMIC PACKAGE
CASE 703



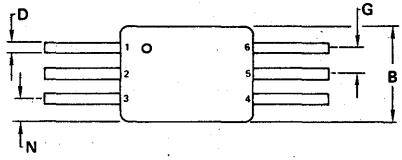


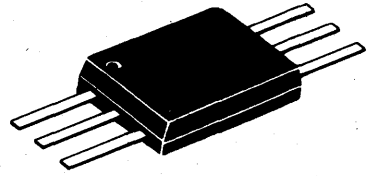
NOTE:
1. SLOTS, TRUE POSITIONED WITHIN 0.25 mm (0.010) TOTAL TO DIM. A and B AT MAXIMUM MATERIAL CONDITION.

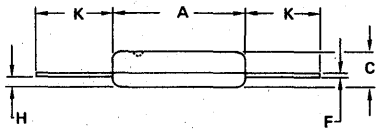
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.29	10.67	0.405	0.420
B	9.27	9.65	0.365	0.380
C	1.02	1.65	0.040	0.065
D	0.10	0.61	0.004	0.024
F	0.38	0.63	0.015	0.025
G	1.02 BSC		0.040 BSC	
H	0.76	1.14	0.030	0.045
J	0.25	0.51	0.010	0.020
R	8.76	9.02	0.345	0.355

CASE 703-01

P SUFFIX
PLASTIC PACKAGE
CASE 704



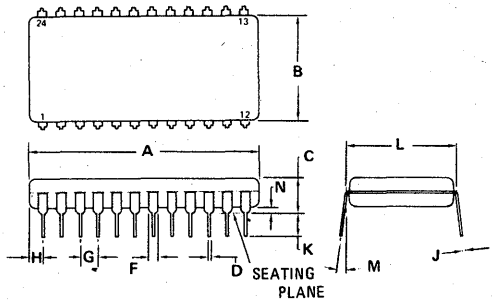


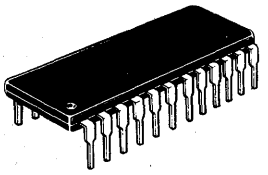


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.69	6.35	0.224	0.250
B	4.06	5.08	0.160	0.200
C	1.17	1.90	0.046	0.075
D	0.38	0.51	0.015	0.020
F	0.20	0.30	0.008	0.012
G	1.22	1.32	0.048	0.052
H	0.13	0.89	0.005	0.035
K	2.34	2.84	0.092	0.112
N	0.89	1.14	0.035	0.045

CASE 704-02

P SUFFIX
PLASTIC PACKAGE
CASE 709



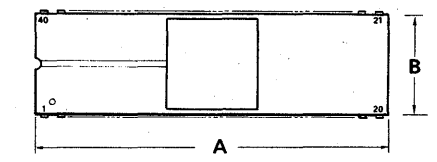


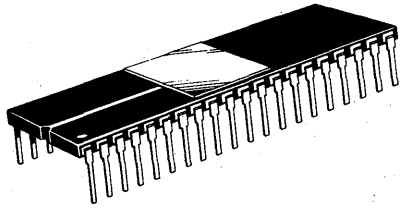
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.73	15.24	0.580	0.600
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

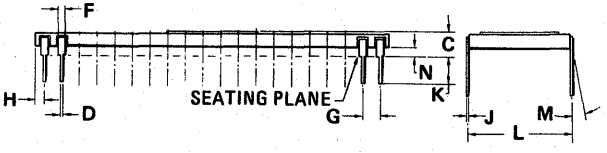
NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (DIM. "D")
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CASE 709-01

L SUFFIX
CERAMIC PACKAGE
CASE 715







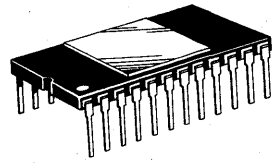
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060

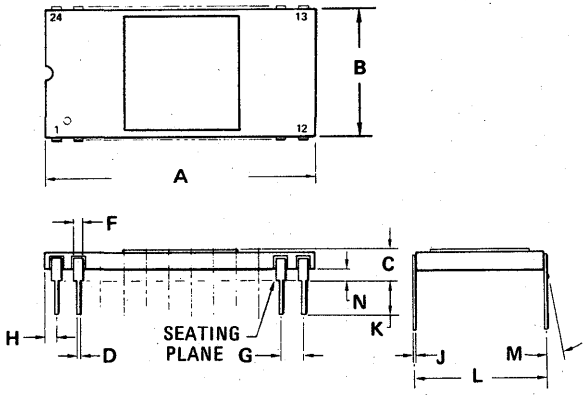
NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX. MAT'L CONDITION.

CASE 715-02

7

L SUFFIX
CERAMIC PACKAGE
CASE 716



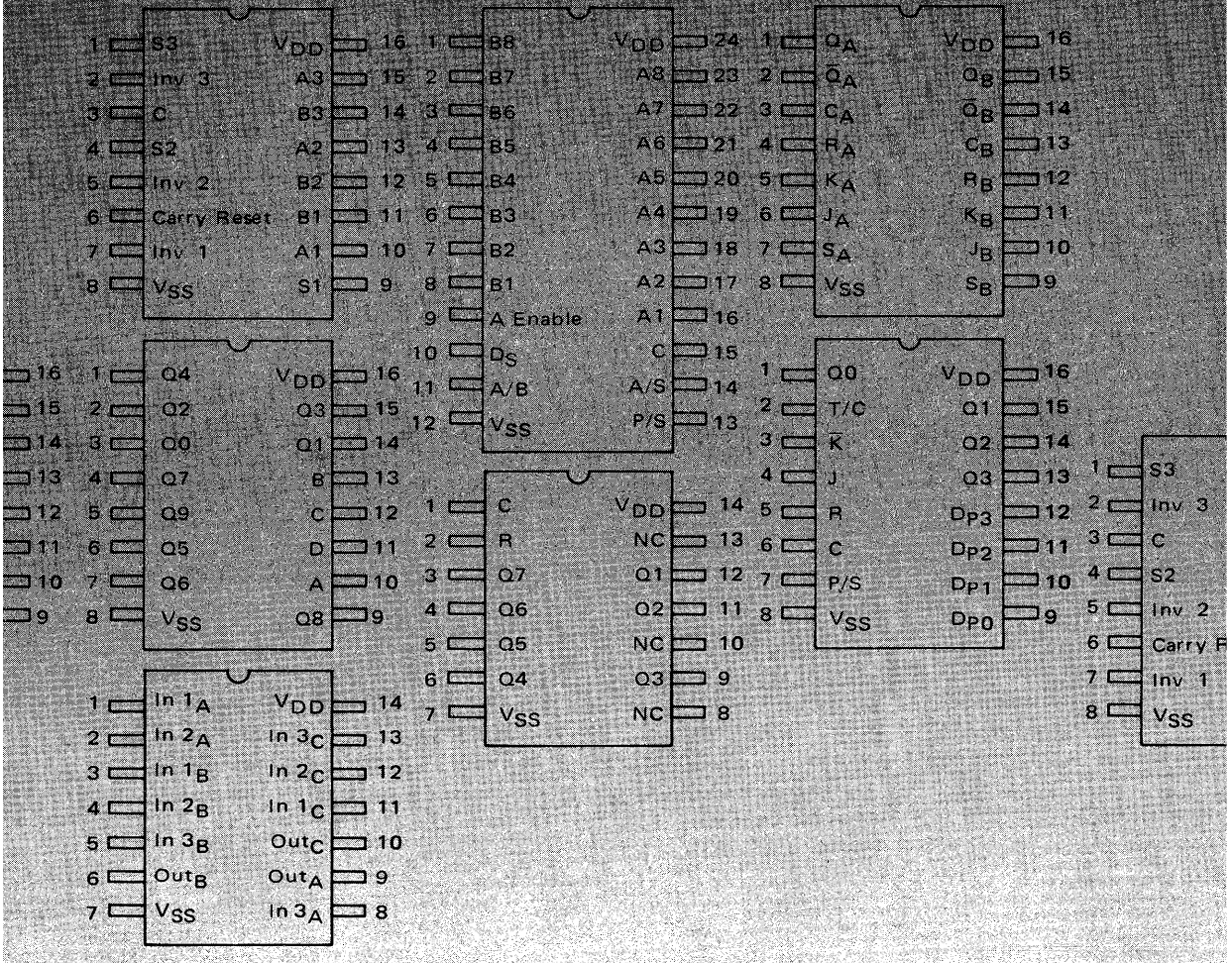


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	29.97	30.99	1.180	1.220
B	14.88	15.62	0.585	0.615
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.88	15.37	0.585	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060

CASE 716–02

NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.

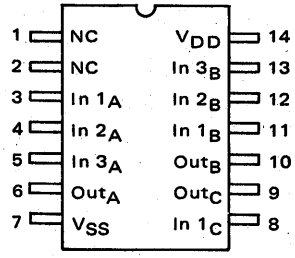
7



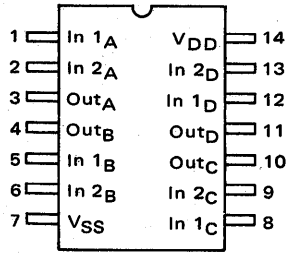
Pin Assignments/Chapter 8

PIN ASSIGNMENTS

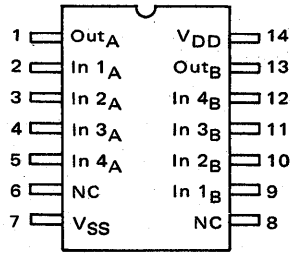
MC14000
Dual 3-Input NOR Gate Plus Inverter



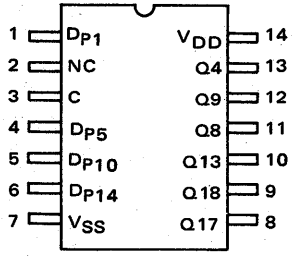
MC14001, MC14001B
Quad 2-Input NOR Gate



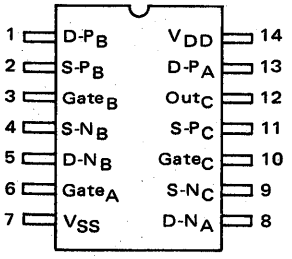
MC14002, MC14002B
Dual 4-Input NOR Gate



MC14006B
18-Bit Static Shift Register

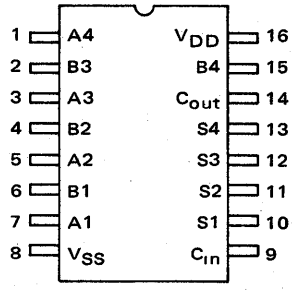


MC14007B
Dual Complementary Pair Plus Inverter

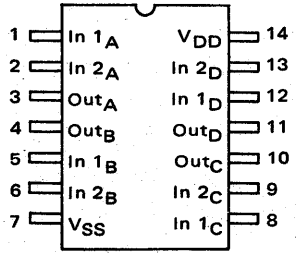


D = Drain
S = Source

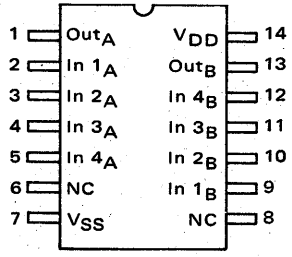
MC14008B
4-Bit Full Adder



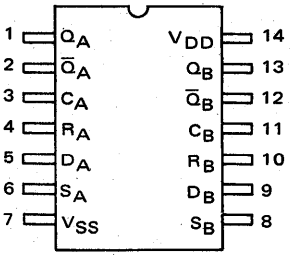
MC14011, MC14011B
Quad 2-Input NAND Gate



MC14012, MC14012B
Dual 4-Input NAND Gate



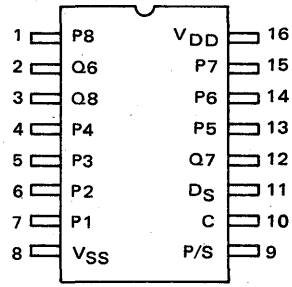
MC14013B
Dual Type D Flip-Flop



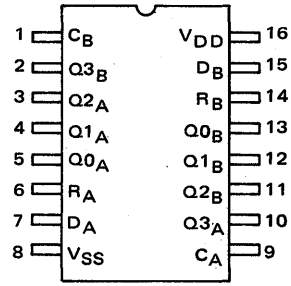
NC = No Connection

PIN ASSIGNMENTS (continued)

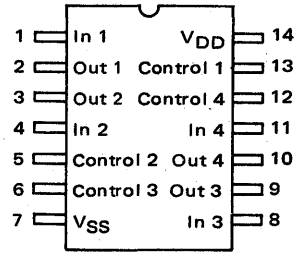
MC14014B
8-Bit Static Shift Register



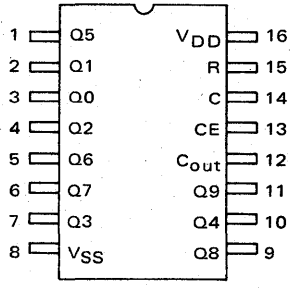
MC14015B
Dual 4-Bit Static Shift Register



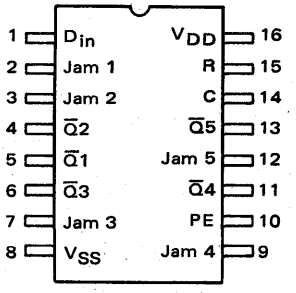
MC14016B
Quad Analog Switch/Quad Multiplexer



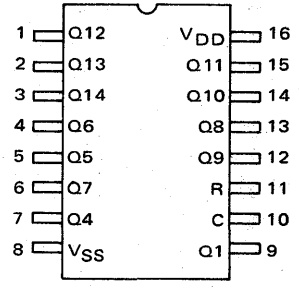
MC14017B
Decade Counter/Divider



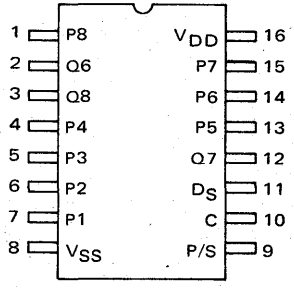
MC14018B
Presettable Divide-by-N Counter



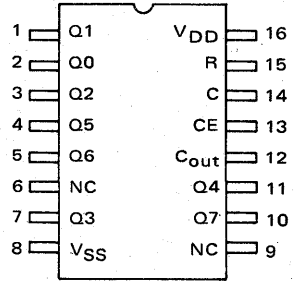
MC14020B
14-Bit Binary Counter



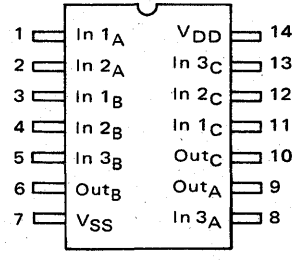
MC14021B
8-Bit Static Shift Register



MC14022B
Octal Counter/Divider



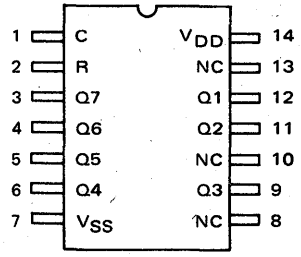
MC14023, MC14023B
Triple 3-Input NAND Gate



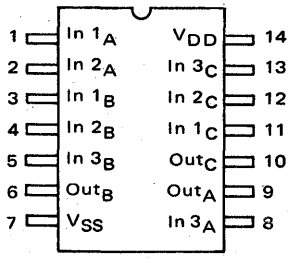
NC = No Connection

PIN ASSIGNMENTS (continued)

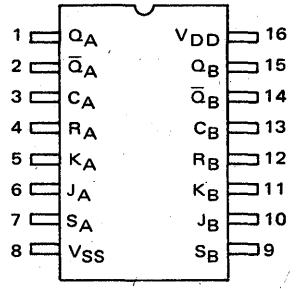
MC14024B
Seven-Stage Ripple Counter



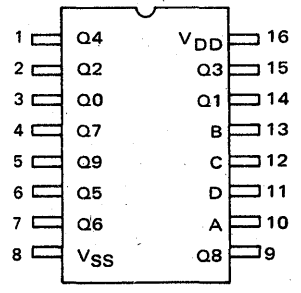
MC14025, MC14025B
Triple 3-Input NOR Gate



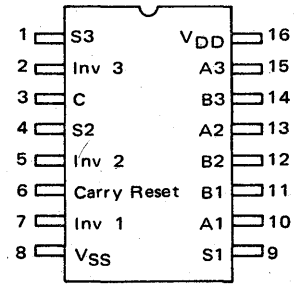
MC14027B
Dual J-K Flip-Flop



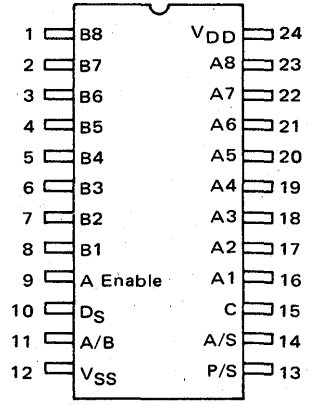
MC14028B
BCD-To-Decimal Decoder/
Binary-To-Octal Decoder



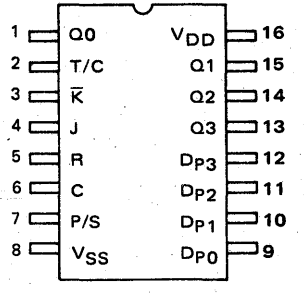
MC14032B
Triple Serial Adder
(Positive Logic)



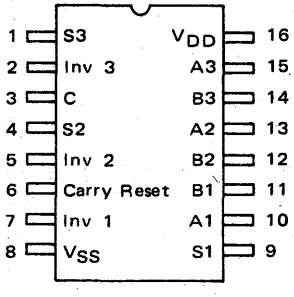
MC14034B
8-Bit Universal Bus Register



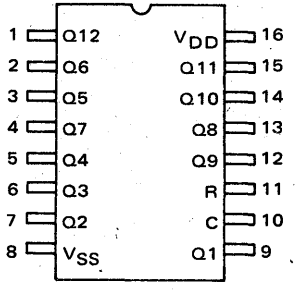
MC14035B
4-Bit Parallel-In/Parallel Out
Shift Register



MC14038B
Triple Serial Adder
(Negative Logic)



MC14040B
12-Bit Binary Counter

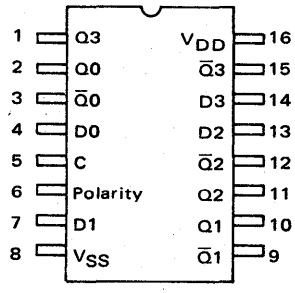


NC = No Connection

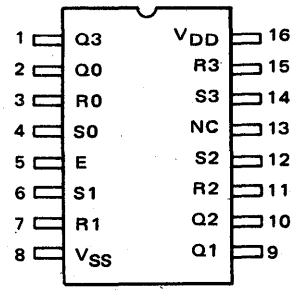
8

PIN ASSIGNMENTS (continued)

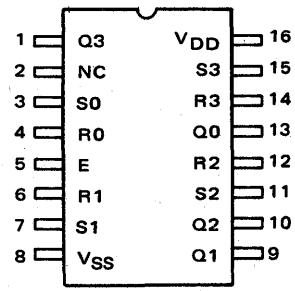
MC14042B
Quad Latch



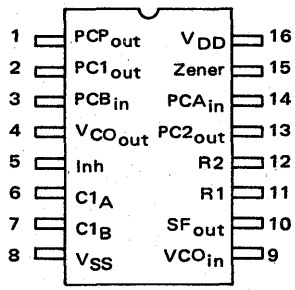
MC14043B
Quad NOR R-S Latch



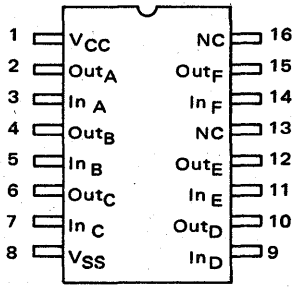
MC14044B
Quad NAND R-S Latch



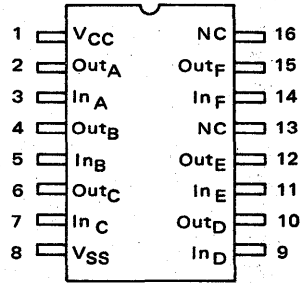
MC14046B
Phase-Locked Loop



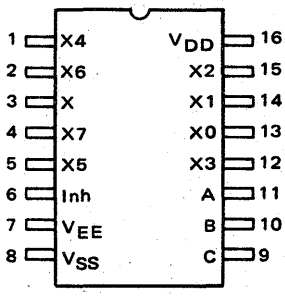
MC14049B
Hex Inverter/Buffer



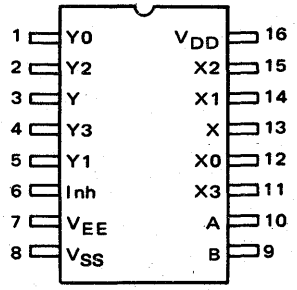
MC14050B
Hex Buffer



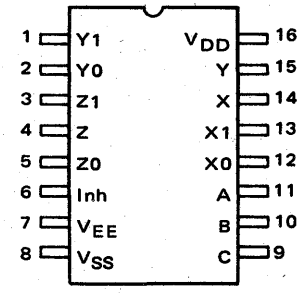
MC14051B
8-Channel Analog
Multiplexer/Demultiplexer



MC14052B
Dual 4-Channel Analog
Multiplexer/Demultiplexer



MC14053B
Triple 2-Channel Analog
Multiplexer/Demultiplexer

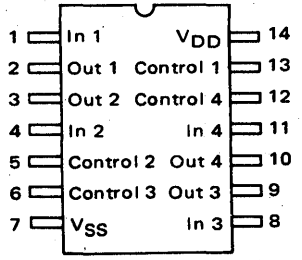


NC = No Connection

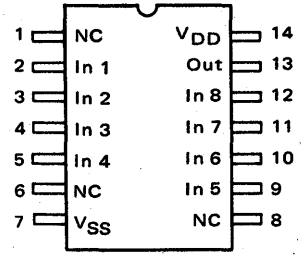
8

PIN ASSIGNMENTS (continued)

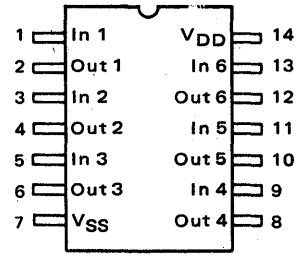
MC14066B
Quad Analog Switch
Quad Multiplexer



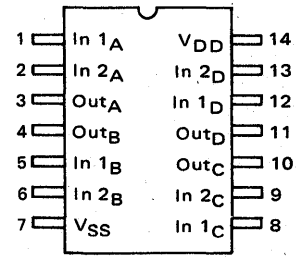
MC14068B
8-Input NAND Gate



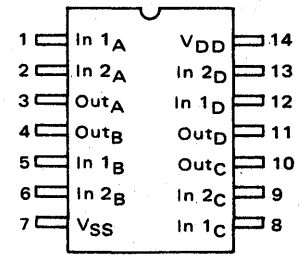
MC14069B
Hex Inverter



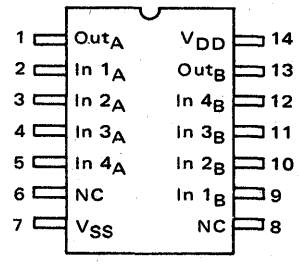
MC14070B
Quad Exclusive OR Gate



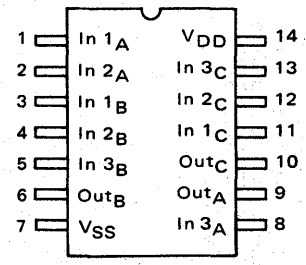
MC14071, MC14071B
Quad 2-Input OR Gate



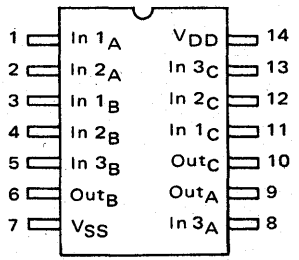
MC14072B
Dual 4-Input OR Gate



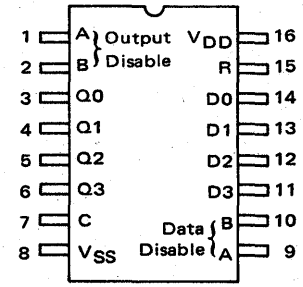
MC14073B
Triple 3-Input AND Gate



MC14075B
Triple 3-Input OR Gate



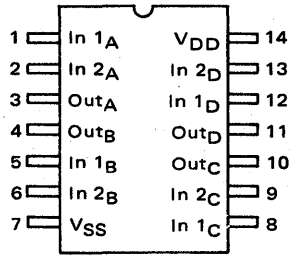
MC14076B
Quad D-Type Register



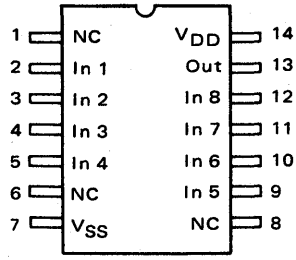
NC = No Connection

PIN ASSIGNMENTS (continued)

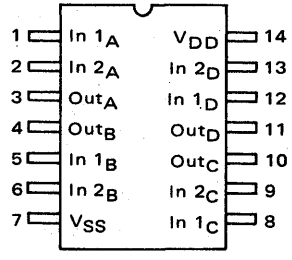
MC14077B
Quad Exclusive NOR Gate



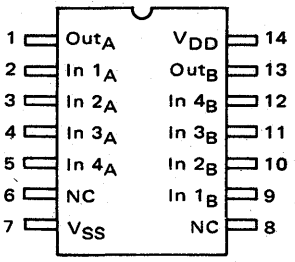
MC14078B
8-Input NOR Gate



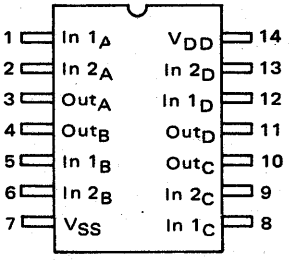
MC14081, MC14081B
Quad 2-Input AND Gate



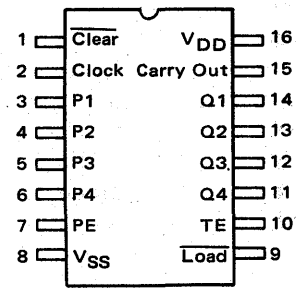
MC14082B
Dual 4-Input AND Gate



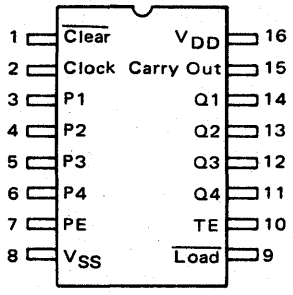
MC14093B
Quad 2-Input NAND
Schmitt Trigger



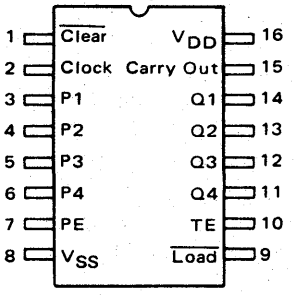
MC14160B
Decade Counter
with Asynchronous Clear



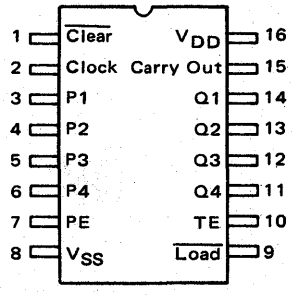
MC14161B
4-Bit Binary Counter
with Asynchronous Clear



MC14162B
Decade Counter
With Synchronous Clear



MC14163B
4-Bit Binary Counter
With Synchronous Clear

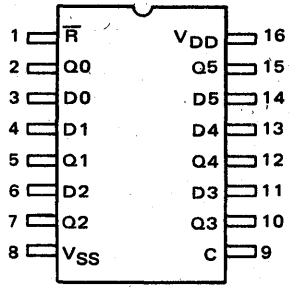


NC = No Connection

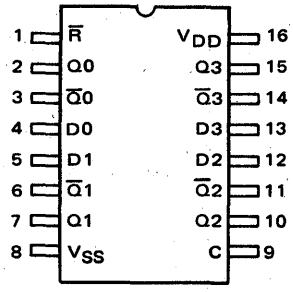
8

PIN ASSIGNMENTS (continued)

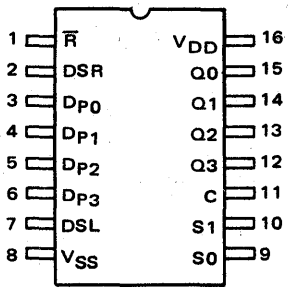
MC14174B
Hex Type D Flip-Flop



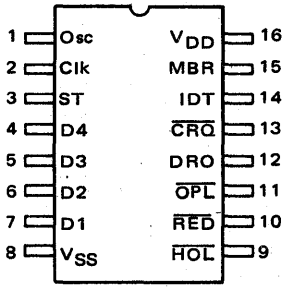
MC14175B
Quad Type D Flip-Flop



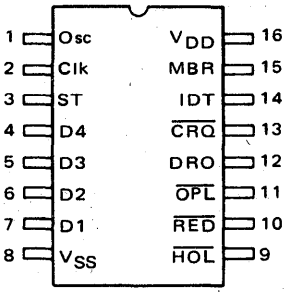
MC14194B
4-Bit Bidirectional
Universal Shift Register



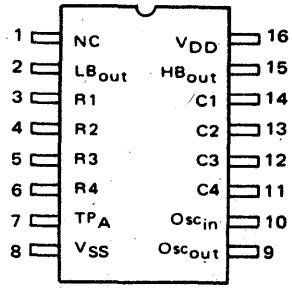
MC14408
Binary to Phone Pulse
Converter Subsystem



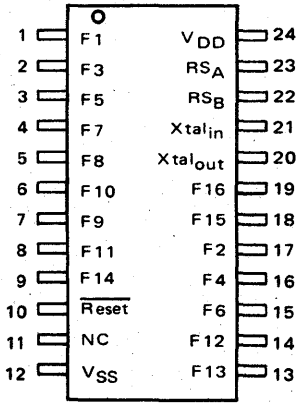
MC14409
Binary to Phone Pulse
Converter Subsystem



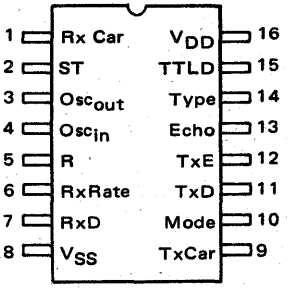
MC14410
2-of-8 Tone Encoder



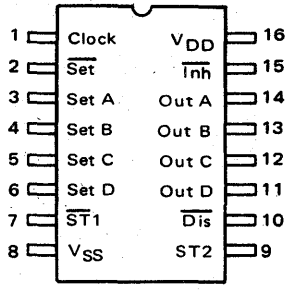
MC14411
Bit Rate Generator



MC14412
Universal
Low Speed Modem



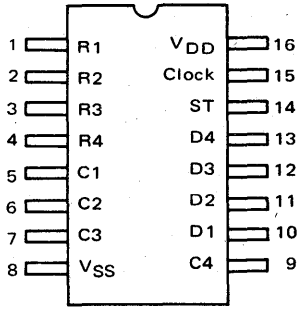
MC14415
Quad Precision Timer/Driver



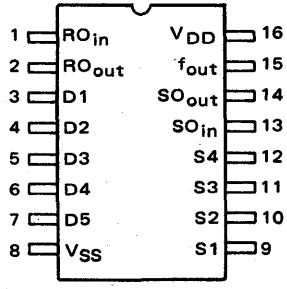
NC = No Connection

PIN ASSIGNMENTS (continued)

MC14419
2-of-8 Keypad-to-Binary Encoder

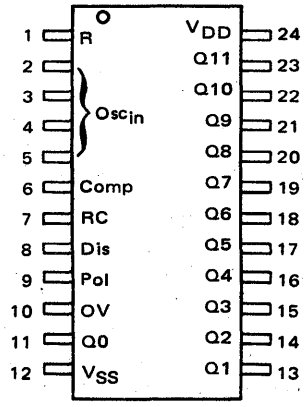


MC14422
Remote Control Transmitter



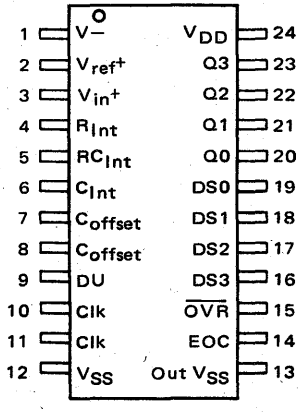
To be introduced

MC14431
12-Bit Binary A/D Converter Digital Subsystem



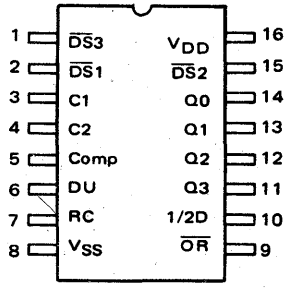
To be introduced

MC14433
3-½ Digit A/D Converter

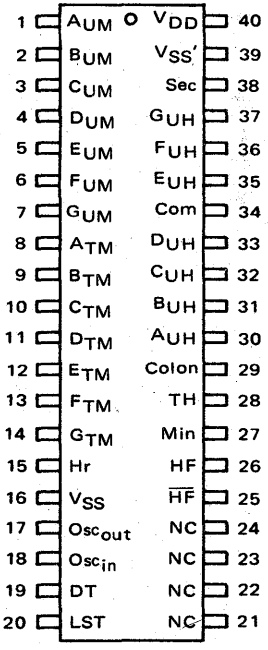


To be introduced

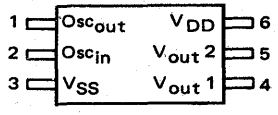
MC14435
3-½ Digit A/D Logic Subsystem



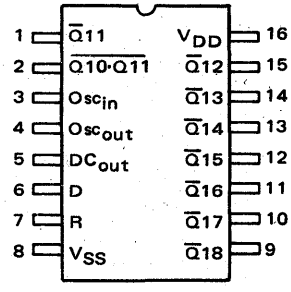
MC14440
LCD Watch/Clock Circuit



MC14450
Oscillator/2^{16} Divider/ Buffer



MC14451
Oscillator/2^{11} to 2^{19} Divider/ Buffered Duty Cycle Control

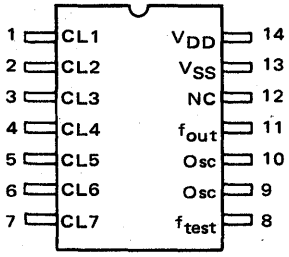


NC = No Connection

8

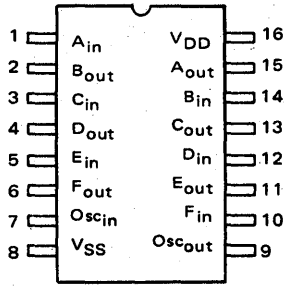
PIN ASSIGNMENTS (continued)

MC14452
Digitally Trimmed Frequency Divider

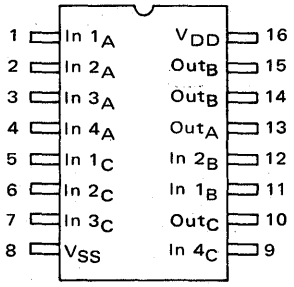


To be introduced

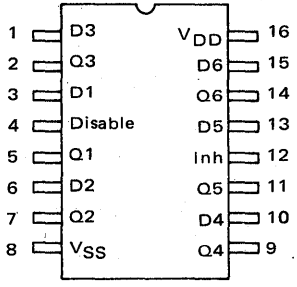
MC14490
Hex Contact Bounce Eliminator



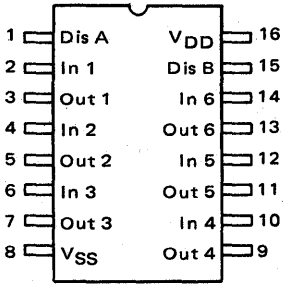
MC14501
Triple Gate



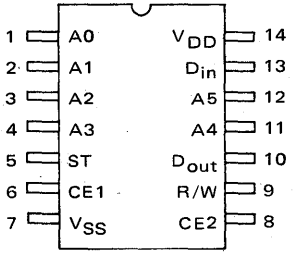
MC14502B
Strobed Hex Inverter/Buffer



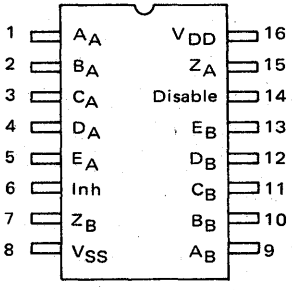
MC14503B
Hex 3-State Buffer



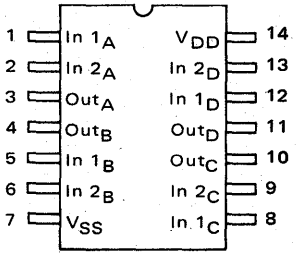
MCM14505
64-Bit Static Random Access Memory



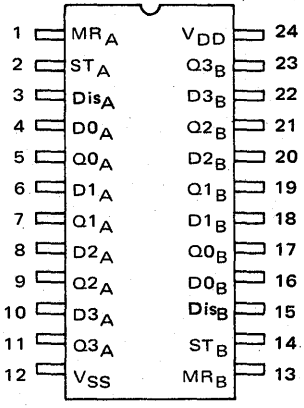
MC14506B
Dual Expandable AND-OR-INVERT Gate



MC14507
Quad Exclusive OR Gate

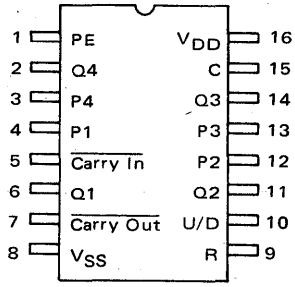


MC14508B
Dual 4-Bit Latch

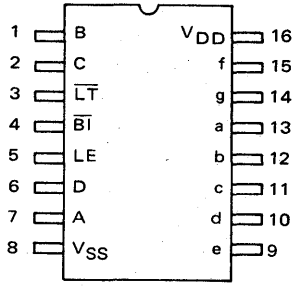


NC = No Connection

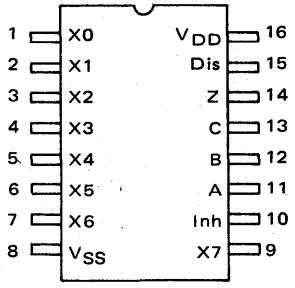
MC14510B
BCD Up/Down Counter



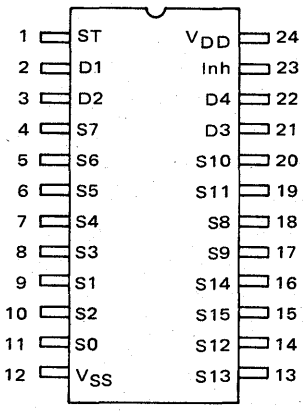
MC14511B
BCD-To-Seven Segment Latch/Decoder/Driver



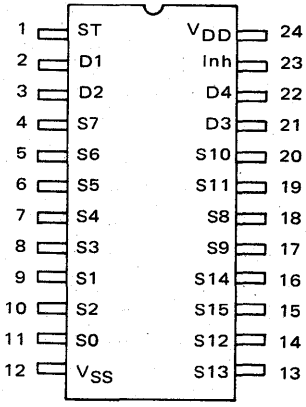
MC14512
8-Channel Data Selector



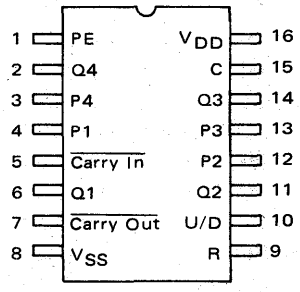
MC14514B
4-Bit Latch/4-To-16 Line Decoder



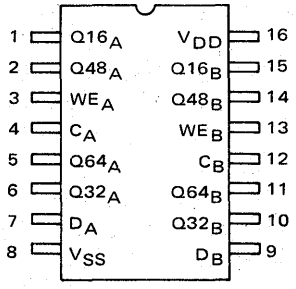
MC14515B
4-Bit Latch/4-To-16 Line Decoder



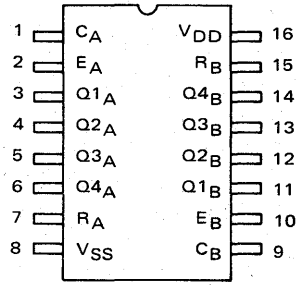
MC14516B
Binary Up/Down Counter



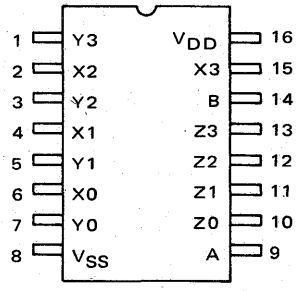
MC14517B
Dual 64-Bit Static Shift Register



MC14518B
Dual BCD Up Counter



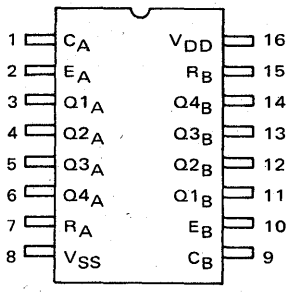
MC14519B
4-Bit AND/OR Selector



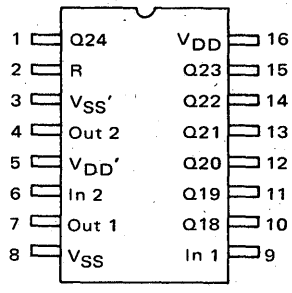
NC = No Connection

PIN ASSIGNMENTS (continued)

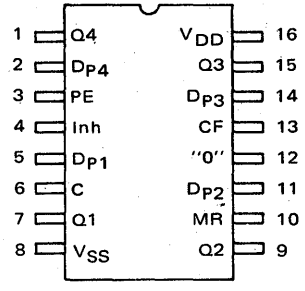
MC14520B
Dual Binary Up Counter



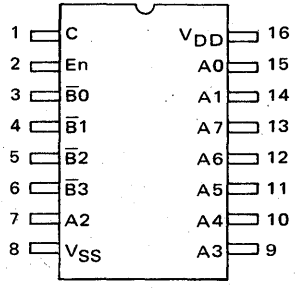
MC14521B
24-Stage Frequency Divider



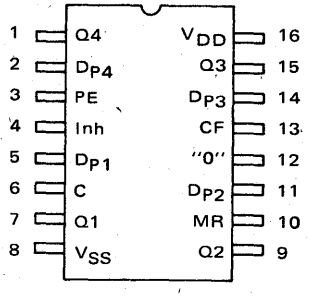
MC14522B
Programmable Divide-By-N-4-Bit BCD Counter



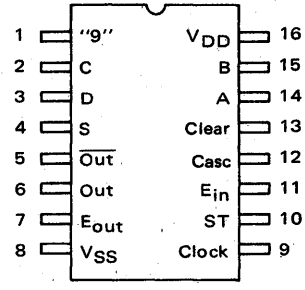
MCM14524
1024-Bit Read Only Memory



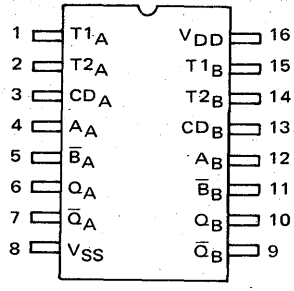
MC14526B
Programmable Divide-By-N-4-Bit Binary Counter



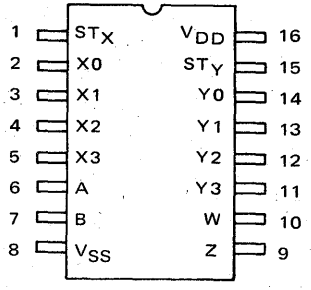
MC14527B
BCD Rate Multiplier



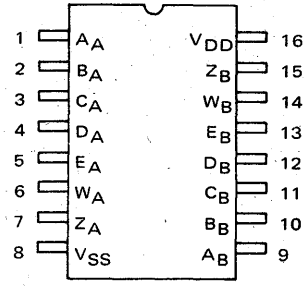
MC14528B
Dual Retriggerable/Resettable Monostable Multivibrator



MC14529B
Dual 4-Channel Analog Data Selector



MC14530B
Dual 5-Input Majority Logic Gate

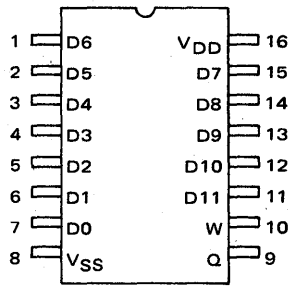


8

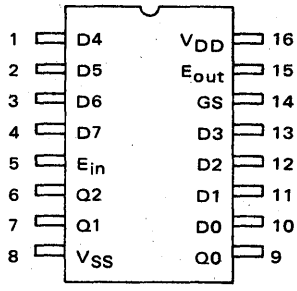
NC = No Connection

PIN ASSIGNMENTS (continued)

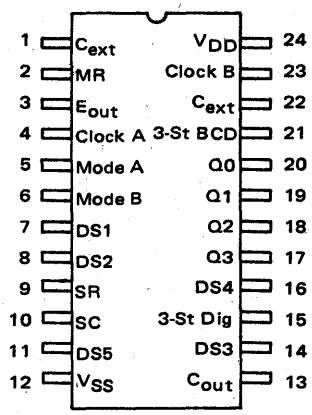
MC14531B
12-Bit Parity Tree



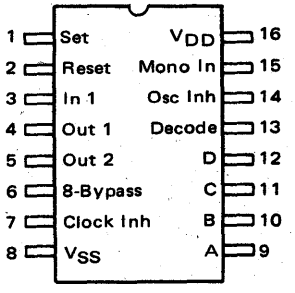
MC14532B
8-Bit Priority Encoder



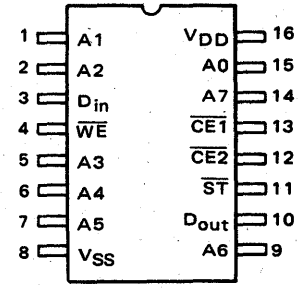
MC14534B
Real Time 5-Decade Counter



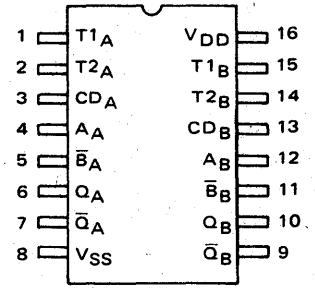
MC14536B
Programmable Timer



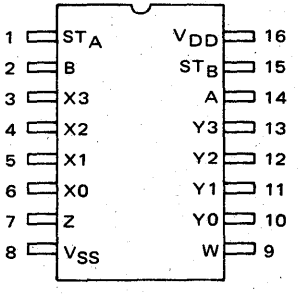
MC14537
256-Bit Static Random Access Memory



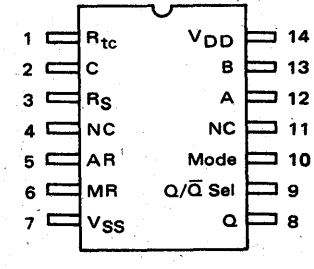
MC14538B
Dual Precision Retriggerable/Resettable Monostable Multivibrator



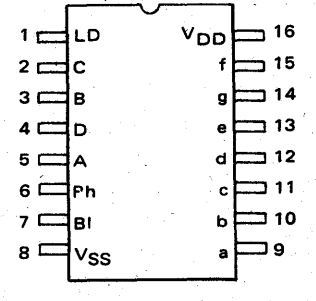
MC14539B
Dual 4-Channel Data Selector/Multiplexer



MC14541B
Programmable Oscillator/Timer

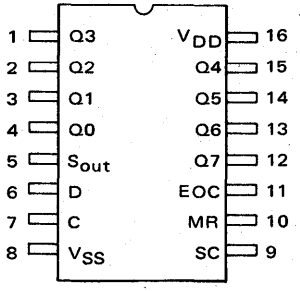


MC14543B
BCD-To-Seven Segment Latch/ Decoder/Driver

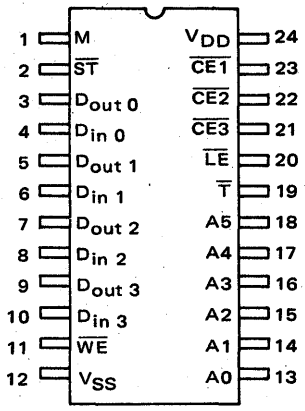


NC = No Connection

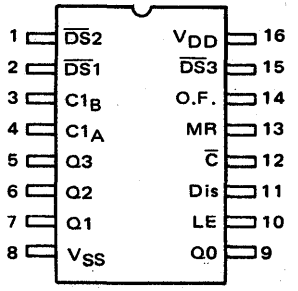
MC14549B
Successive Approximation Register



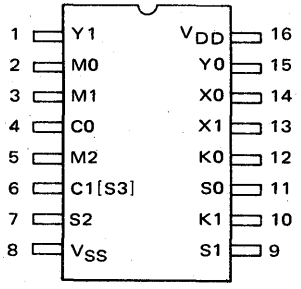
MCM14552
256-Bit Static Random Access Memory



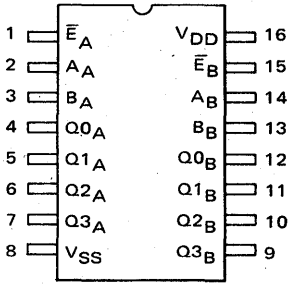
MC14553B
3-Digit BCD Counter



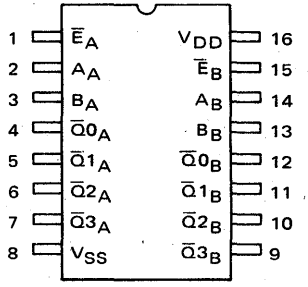
MC14554B
2 x 2-Bit Parallel Binary Multiplier



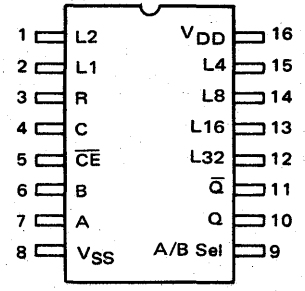
MC14555B
Dual Binary to 1-of-4 Decoder/ Demultiplexer



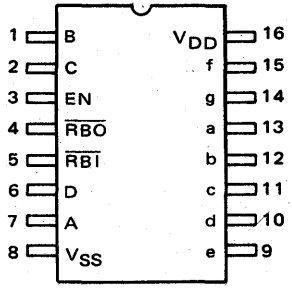
MC14556B
Dual Binary to 1-of-4 Decoder/ Demultiplexer



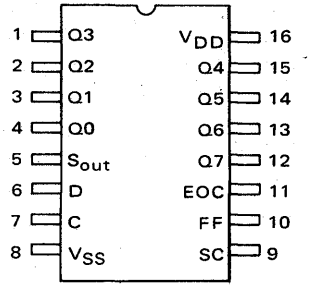
MC14557B
1 to 64-Bit Variable Length Shift Register



MC14558B
BCD-to-Seven Segment Decoder



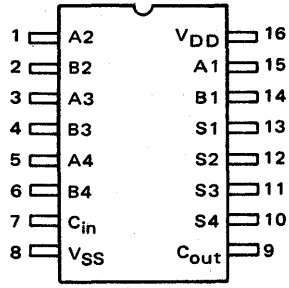
MC14559B
Successive Approximation Register



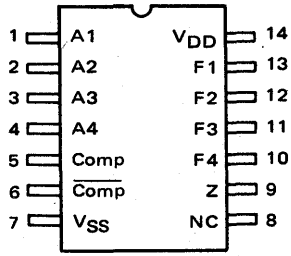
NC = No Connection

PIN ASSIGNMENTS (continued)

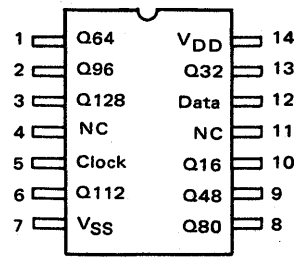
MC14560B
NBCD Adder



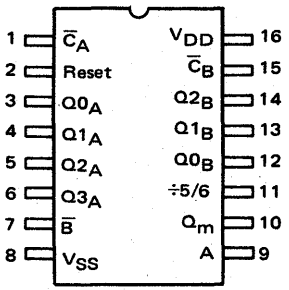
MC14561B
9's Complementer



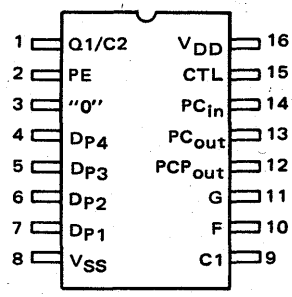
MC14562B
128-Bit Static Shift Register



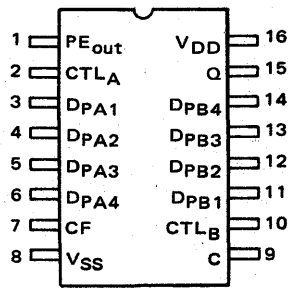
MC14566B
Industrial Time Base Generator



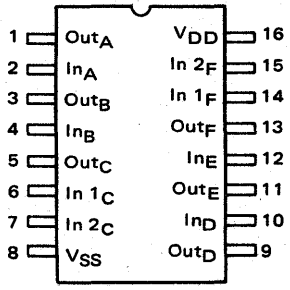
MC14568B
Phase Comparator and Programmable Counters



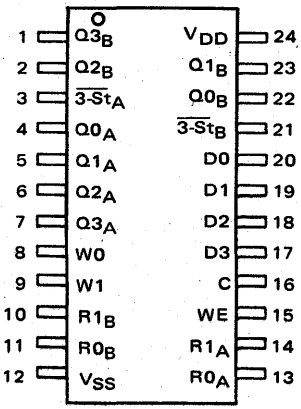
MC14569B
High Speed Programmable Divide-by-N Dual 4-Bit BCD/Binary Counter



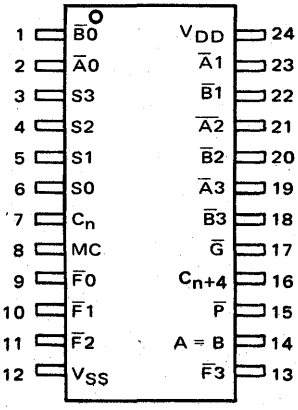
MC14572
Hex Gate



MC14580B
4 x 4 Multiport Register



MC14581B
4-Bit Arithmetic Logic Unit



NC = No Connection

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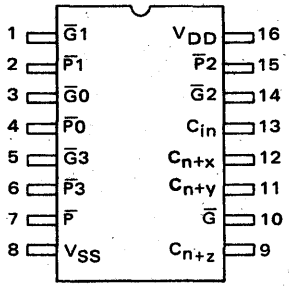
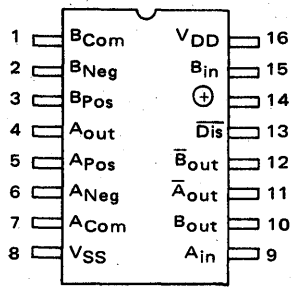
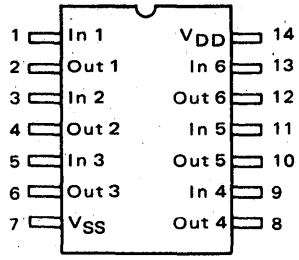
MC14582B
Look-Ahead Carry Block



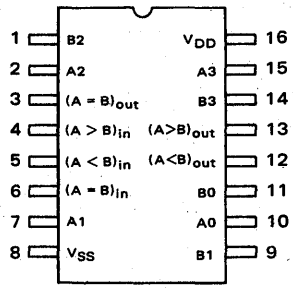
MC14583B
Dual Schmitt Trigger



MC14584B
Hex Schmitt Trigger



MC14585B
4-Bit Magnitude Comparator



NC = No Connection