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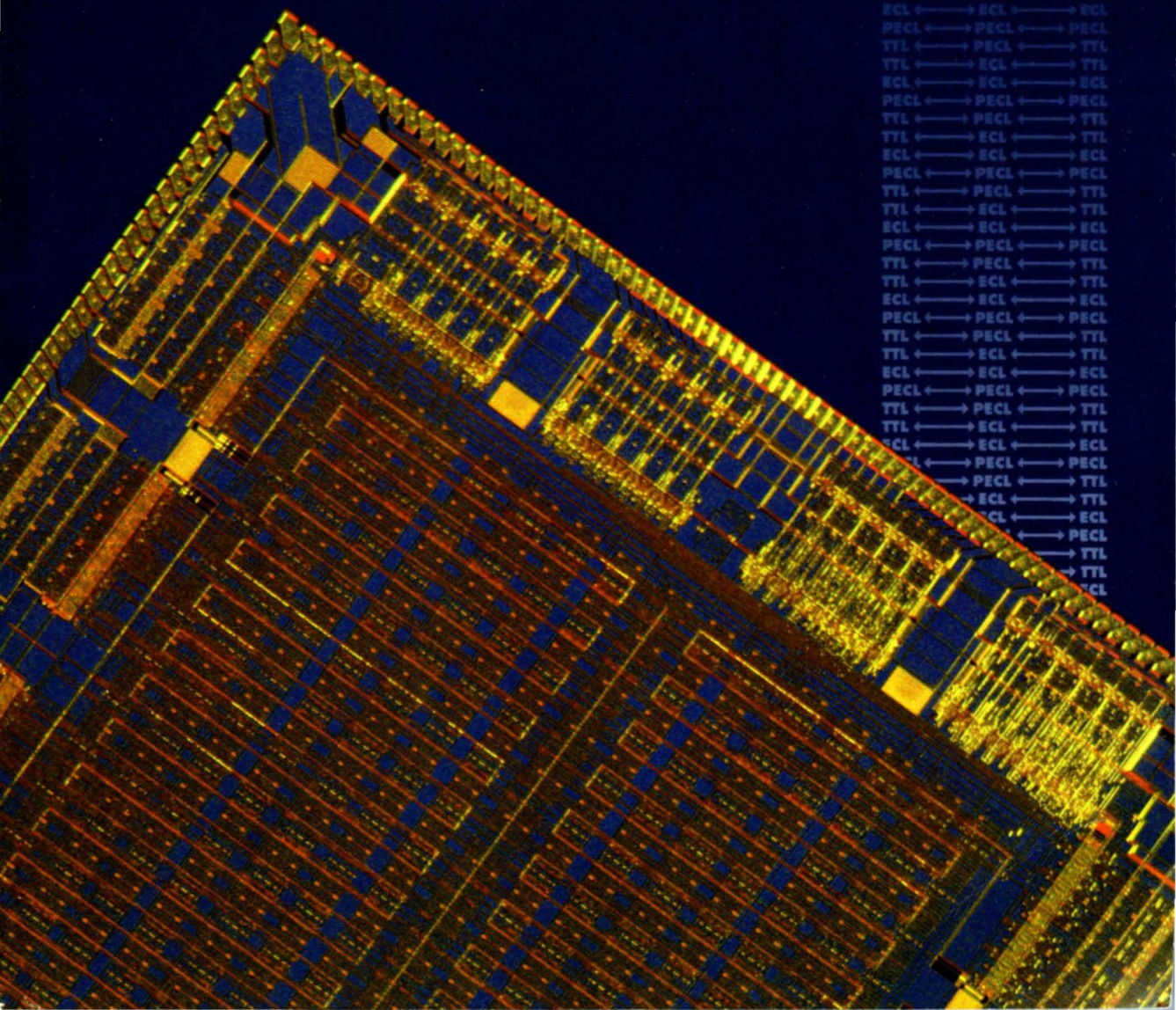
MCA3 ETL Series Design Manual



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MCA3 ETL SERIES

THIRD GENERATION BIPOLAR MACROCELL ARRAYS

Preliminary

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Summary of Change Information

The following list represents information which has been added or changed since **Version 1.41** of the Preliminary issue of the MCA3 ETL Series Design Manual.

1. Revised Section 2.4 and Figure 2-2 to include High Drive (L) Macros in description of speed/power programmability macro selection.

2. Included 160 QFP Pad to Pin Cross-Reference Table in Section 4.

3. Revised frequency specification and related information on pages 5-23 thru 5-25.

4. Included Notes in Pad to Pin Cross-Reference Tables (Section 4) and the 'Fix Placement of I/O Macros/Pins' paragraph (Section 6.3.4) clarifying prefacing actual pin numbers for both the 64 and 160 QFP packages for data entry into the **FIX** file.

5. Included 160 QFP Packaging Information in Section 7.

NOTE: This manual is preliminary and therefore subject to change without notice in order to provide the user with a more accurate specification of the functionality and performance of the product.

Acknowledgments:

The authors would like to acknowledge the **MCA3 ETL Array Design Group** for their effort and assistance in preparing this manual.

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MCA3 ETL Series Numerical Macro Listing

SIZE indicates the macrocell size in quarter cells for the internal macrocells and in U-cells for the input or Output macrocells.

SG indicates the levels of series gating used in the macrocell function. Note that a '3' in this column denotes a macro which uses three-level series gating and thus cannot be used with a supply voltage of −4.5 Vdc. All macrocells using three levels of series-gating are shaded.

INTERNAL MACROS (M−Cells)

Macro	Function	Size	SG
L/H200	5-INPUT OR/NOR	1/4 CELL	1
L/H201	4-INPUT OR/NOR	1/4 CELL	1
L/H202	2-INPUT OR/NOR	1/4 CELL	1
L/H203	8-INPUT OR/NOR	1/2 CELL	2
L204	12-INPUT OR/NOR	1/2 CELL	1
L/H207	6-INPUT OR/NOR	1/4 CELL	2
L/H211	2-2 OR/AND	1/4 CELL	2
L/H212	3-2-2-2 OR/AND	1/2 CELL	2
L213	4-3-3-3 OR/AND	1/2 CELL	1
L/H214	2-2-2-2-1-1-1-1 OR/AND	FULL CELL	2
L/H215	2-2-3-3-3 OR/AND	FULL CELL	2
L/H216	4-2-3-2-3 OR/AND	FULL CELL	2
L217	5-4-3-2 OR/AND	1/2 CELL	1
L/H218	5-4-3-2-1 OR/AND	FULL CELL	2
L/H219	3-3 OR/AND	1/4 CELL	2
L/H221	2-2 OR/EXOR	1/4 CELL	2
L/H222	DUAL 2-2 OR/AND/EXNOR	FULL CELL	2
L/H223	4-INPUT EXNOR	1/2 CELL	2
L/H224	4-INPUT EXOR	1/2 CELL	2
L/H225	2-1-1-2 OR/AND/EXOR	1/2 CELL	2
L/H226	2-1-1-2 OR/AND/EXNOR	1/2 CELL	2
L/H227	2-1 EXOR/AND/NAND	1/2 CELL	2
L/H228	2-1 AND/EXOR	1/4 CELL	2
L251	4-TO-1 MUX W/ENABLE (LOW)	1/2 CELL	2
L/H252	QUAD 2-TO-1 MUX	FULL CELL	2
L/H253	2-TO-1 MUX W/ENABLE (LOW)	1/4 CELL	2
L/H254	2-TO-1 MUX W/GATED INPUTS	1/4 CELL	2
L/H255	DUAL 2-TO-1 MUX W/COM. SELECT	1/2 CELL	2
L/H256	2-TO-1 MUX	1/4 CELL	2
L258	4-TO-1 MUX W/ENABLE (HIGH)	1/2 CELL	2
L/H259	4-TO-1 MUX	1/2 CELL	2
L/H261	1-OF-4 DECODER W/ENABLE (LOW)	1/2 CELL	2
L/H262	1-OF-4 DECODER W/ENABLE (HIGH)	1/2 CELL	2
L/H263	1-OF-4 DECODER (HIGH)	FULL CELL	2
L/H277	4-2-4-2-4-2 OR/AND	3/4 CELL	2
L/H278	3 DATA INPUT DATA LATCH	1/4 CELL	2
L/H279	4-2-4-2-4-2-4-2 OR/AND	FULL CELL	2
L/H280	4-2-4-2 OR/AND	1/2 CELL	2
L/H281	FULL ADDER	FULL CELL	2
L/H282	FULL ADDER W/GATED INPUTS	1/2 CELL	2
L/H283	2-BIT LOOK-AHEAD CARRY	FULL CELL	2
L/H284	HALF ADDER W/GATED INPUTS	1/4 CELL	2
L/H285	3-BIT ADDER (SUM)	1/2 CELL	2
L/H286	3-BIT ADDER (CARRY)	1/2 CELL	2
L/H290	D FLIP-FLOP WITH SET AND RESET	1/2 CELL	2
L/H291	D FLIP-FLOP WITH RESET	1/2 CELL	2
L/H292	D FLIP-FLOP WITH MUX	3/4 CELL	2
L/H293	D LATCH WITH RESET	1/4 CELL	2
L/H294	D LATCH WITH MUX	1/2 CELL	2
L/H295	GATED 2-WAY D LATCH	1/2 CELL	2
L/H296	EXNOR D LATCH	1/2 CELL	2
L/H297	GATED 4-WAY D LATCH	3/4 CELL	2
L/H298	DUAL D LATCH W/RESET	1/2 CELL	2
L302	INPUT OR/NOR (High Drive)	1/2 CELL	1
L/H310	4-4-4-4 OR/AND	FULL CELL	1

INTERNAL MACROS (M–Cells)

Macro	Function	Size	SG
L/H311	3-3-3-3 AND/OR	FULL CELL	2
L/H312	3-3-3 AND/OR	1/2 CELL	2
L/H313	2-2 OR/AND	1/4 CELL	2
L/H315	2-2-1-1 OR/AND	1/2 CELL	2
L/H318	3-3 AND/OR	1/2 CELL	1
L319	3-3-2-1 AND/OR	1/2 CELL	2
L/H320	2-3-4-4 AND/OR W/ENABLE (HIGH)	FULL CELL	2
L/H321	6-6-4-4-2-2 OR/AND	FULL CELL	2
L322	3-3-3 AND/OR	1/2 CELL	1
L/H323	3-2-2-2-2-3 AND/OR	FULL CELL	2
L/H324	5-5-5-5 AND/OR	FULL CELL	1
L328	2-1 AND/EXOR (High Drive)	1/2 CELL	2
L/H331	3-2-2 AND/OR	1/2 CELL	2
L/H332	GATED OR	1/2 CELL	2
L/H333	GATED OR	1/2 CELL	2
L/H370	DIFFERENTIAL LINE RECEIVER	1/4 CELL	2
L/H371	2-1 MUX WITH DIFFERENTIAL INPUTS	1/4 CELL	2
L/H372	D FLIP-FLOP W/DIFFERENTIAL CLOCK AND DATA	1/2 CELL	2
L/H373	2-1 MUX W/DIFF INPUTS AND DIFF MUX CTL	1/4 CELL	2
L/H374	DIFFERENTIAL LINE RECEIVER	1/4 CELL	1
L/H375	D FLIP-FLOP WITH DIFFERENTIAL CLOCK	1/2 CELL	2
L/H376	D FLIP-FLOP WITH DIFFERENTIAL CLOCK	1/2 CELL	2
L380	NOR LATCH	1/4 CELL	1
L/H381	D FLIP-FLOP WITH SET	1/2 CELL	2
L/H391	D FLIP-FLOP, NEGATIVE EDGE TRIGGERED	1/2 CELL	2
L/H392	D FLIP-FLOP WITH MUX, NEGATIVE EDGE TRIGGERED	3/4 CELL	2
L/H393	D LATCH WITH CLOCK ENABLE (HIGH)	1/4 CELL	2
L/H394	D FLIP-FLOP WITH MUX, NEGATIVE EDGE TRIGGERED	FULL CELL	2
L/H395	D FLIP-FLOP WITH ASYN SET AND DATA ENABLE	FULL CELL	2
L/H396	SCAN D FLIP FLOP	FULL CELL	2
L/H397	D LATCH WITH ASYN SET	1/4 CELL	2
L/H398	SCAN D LATCH W/ASYN SET	1/2 CELL	2
L/H400	12-INPUT OR	1/4 CELL	2
L/H401	12-INPUT NOR	1/4 CELL	2
L402	2-INPUT OR/NOR, 3-INPUT OR/NOR	1/4 CELL	1
L/H403	8-INPUT OR/NOR	1/4 CELL	1
L/H404	12-INPUT NOR	1/2 CELL	3
L/H411	2-2-2 OR/AND	1/4 CELL	3
L/H413	4-3-3-3 OR/AND	1/2 CELL	2
L414	3-3-3-3 OR/AND	1/2 CELL	2
L/H416	4-2-3-2-3 OR/AND	FULL CELL	3
L/H417	5-4-3-2 OR/AND	1/2 CELL	2
L/H418	5-4-3-2-1 OR/AND	3/4 CELL	2
L/H419	4-4 OR/AND	1/4 CELL	2
L421	DUAL EXOR	1/4 CELL	2
L/H422	DUAL 2-2 OR/AND/EXOR	1/2 CELL	3
L/H424	6-INPUT EXNOR	1/2 CELL	3
L/H425	6-INPUT EXOR	1/2 CELL	3
L/H427	2-1 EXOR/AND/NAND	1/4 CELL	3
L/H438	6-5-4-3-2-1 OR/AND	1/2 CELL	3
L/H451	4-1 MUX W/ENABLE(LOW)	1/2 CELL	3
L452	QUAD 2-TO-1 MUX	1/2 CELL	2
L/H453	2-TO-1 MUX W/ENABLE(LOW)	1/4 CELL	3
L/H454	2-TO-1 MUX W/ENABLE(HIGH)	1/4 CELL	3
L/H455	DUAL 2-TO-1 MUX W/ENABLE (HIGH)	1/2 CELL	3
L456	TRIPLE 2-TO-1 MUX(COMMON SELECT)	1/2 CELL	2
L457	TRIPLE 2-TO-1 MUX	1/2 CELL	2
L/H458	4-1 MUX W/ENABLE(HIGH)	1/2 CELL	3
L/H459	DUAL 4-1 MUX	1/2 CELL	3
L/H461	1-OF-4 DECODER WITH ENABLE(LOW)	1/2 CELL	3
L/H462	1-OF-4 DECODER WITH ENABLE(HIGH)	1/2 CELL	3
L464	8-3 ENCODER	FULL CELL	3
L/H465	1-OF-4 DECODER WITH ENABLE(LOW)	1/2 CELL	3
L/H466	1-OF-4 DECODER WITH ENABLE(HIGH)	1/2 CELL	3
L470	DUAL 2-TO-1 MUX(COMMON SELECT)	1/4 CELL	2

INTERNAL MACROS (M–Cells)

Macro	Function	Size	SG
L474	DIFFERENTIAL LINE RECEIVER (High Drive)	1/2 CELL	2
L482	TRIPLE FULL ADDER	FULL CELL	2
L/H485	3–BIT ADDER	1/2 CELL	3
L/H501	2–INPUT OR (Quad Buffer)	1/4 CELL	1
L/H502	2–INPUT NOR (Quad Buffer)	1/4 CELL	1
L503	5x2 INPUT OR	1/2 CELL	1
L/H510	4–4–4–4 OR/AND	1/2 CELL	2
L/H511	3–3–3–3 AND/OR	1/2 CELL	3
L/H512	3–3–3 AND/OR	1/2 CELL	3
L/H513	3–1–1–1 OR/AND	1/4 CELL	2
L/H518	3–3 AND/OR	1/4 CELL	2
L/H519	3–3–2–1 AND/OR	1/2 CELL	2
L/H520	2–3–4–4 AND/OR W/ENABLE(HIGH)	1/2 CELL	3
L/H523	3–2–2–2–3 AND/OR	FULL CELL	3
H553	2–TO–1 MUX W/ENABLE LOW	1/4 CELL	2
L/H571	8–OUTPUT BUFFER W/DIFf INPUT & ENABLE (Quad Buffer)	1/2 CELL	3
L585	D FLIP–FLOP W/2to 1 MUX DATA INPUT	1/2 CELL	2
L593	W BUFFER	1/4 CELL	1
L/H611	3–3–3 OR/AND	1/4 CELL	3
L/H616	4–2–3–3–2 OR/AND	1/2 CELL	3
L/H618	5–4–3–2–1 OR/AND	1/2 CELL	3
L/H658	4–1 MUX	1/2 CELL	3
L/H685	FULL ADDER W/GATED INPUTS	1/2 CELL	3
L/H691	D FLIP–FLOP W/RESET	1/2 CELL	2
L/H692	D FLIP–FLOP WITH MUX	3/4 CELL	2
L/H694	D FLIP–FLOP W/RESET (NEGATIVE HOLD TIME)	1/2 CELL	2
L700	DIFFERENTIAL LINE RECEIVER (High Drive)	1/2 CELL	2
L701	2–TO–1 MUX W/DIFF INPUTS AND MUX CONTROL (High Drive)	1/2 CELL	2
H710	D FLIP–FLOP WITH DIFFERENTIAL CLOCK AND DATA	1/2 CELL	2
H711	D FLIP–FLOP W/GATED DATA INPUT AND DIFF CLOCK	1/2 CELL	2
H712	D FLIP–FLOP W/EXNOR GATED DATA INPUT & DIFF CLOCK	FULL CELL	3
L713	D FLIP–FLOP W/DIFF CLOCK AND DATA (High Drive)	FULL CELL	2
L714	D FLIP–FLOP W/ GATED DATA & DIFF CLK (High Drive)	FULL CELL	2
L/H802	3–INPUT EXOR/EXNOR	1/4 CELL	3
L/H803	3–INPUT EXOR/EXNOR	1/4 CELL	3
L804	DUAL 2–INPUT AND	1/4 CELL	2
L805	DUAL 2–INPUT NAND	1/4 CELL	2
L806	DUAL 2–INPUT AND/NAND	1/4 CELL	2
L807	DUAL 2–INPUT AND/NAND	1/4 CELL	2
L/H809	8–1 MUX WITH ENABLE (HIGH)	FULL CELL	3
L/H810	8–1 MUX WITH ENABLE (HIGH)	FULL CELL	3
L811	DUAL 4–INPUT OR	1/4 CELL	1
L812	DUAL 4–INPUT OR/NOR	1/4 CELL	1
L813	DUAL 4–INPUT OR/NOR	1/4 CELL	1
L814	DUAL 4–INPUT NOR	1/4 CELL	1
L815	DUAL 2–INPUT OR	1/4 CELL	1
L816	DUAL 2–INPUT OR/NOR	1/4 CELL	1
L817	DUAL 2–INPUT OR/NOR	1/4 CELL	1
L818	DUAL 2–INPUT NOR	1/4 CELL	1
L/H819	3–2–1 OR/AND	1/4 CELL	3
L820	2–INPUT OR, 2–INPUT AND	1/4 CELL	2
L850	EXPANDABLE 2–1 MUX(CODER) AND 2x2–1 MUX	1/2 CELL	2
L851	EXPANDABLE 2–1 MUX	1/2 CELL	2
L852	EXPANDABLE 2–1 MUX	1/2 CELL	2
L853	EXPANDABLE 2–1 MUX	1/2 CELL	2
L860	EXPANDABLE 4–1 MUX(CODER) WITH ENABLE	1/2 CELL	3
L/H861	EXPANDABLE 4–1 MUX	1/2 CELL	3
L/H862	EXPANDABLE 4–1 MUX	1/2 CELL	3
L/H863	EXPANDABLE 4–1 MUX	1/2 CELL	3
L870	EXPANDABLE 8–1 MUX(CODER)	1/2 CELL	3
L/H871	EXPANDABLE 8–1 MUX	1/2 CELL	3
L/H872	EXPANDABLE 8–1 MUX	1/2 CELL	3
L/H873	EXPANDABLE 8–1 MUX	1/2 CELL	3
L881	DUAL D (INVERTING) FLIP–FLOP	1/2 CELL	2
L882	DUAL D FLIP–FLOP	1/2 CELL	2
L893	3xD LATCH WITH COMMON CLOCK	1/2 CELL	2
L/H894	D LATCH WITH MUX	1/4 CELL	3
L895	D FLIP–FLOP	1/4 CELL	2
L896	3xD LATCH WITH COMMON CLOCK AND RESET	1/2 CELL	2

ECL and PECL I/O Macros (U–Cells)

Macro	Function	Size	SG
INPUT INTERFACE (C) MACROS			
L/HC01	INPUT BUFFER (Non–Inverting) Quad Buffer	1–U CELL	1
L/HC02	INPUT BUFFER (Inverting) Quad Buffer	1–U CELL	1
L/HC03	INPUT BUFFER (Inverting, Non–Inverting)	1–U CELL	1
L/HC05	DUAL DIFFERENTIAL INPUT BUFFER	2–U CELLS	1
L/HC13	DIFFERENTIAL INPUT BUFFER	2–U CELLS	1
LC15	DIFFERENTIAL BYPASS	2–U CELLS	1
L/HC50	INPUT LATCH with ENABLE LOW	1–U CELL	1
LC70	DIFFERENTIAL INPUT BUFFER WITH OFF CHIP TERMINATION INPUTS (High Drive)	2–U CELLS	1
OUTPUT DRIVERS (E) MACROS, 60 & 50 ohm			
L/HE01	2–INPUT OR	1–U CELL	1
L/HE02	2–INPUT NOR	1–U CELL	1
L/HE03	4–INPUT OR	1–U CELL	1
L/HE04	4–INPUT NOR	1–U CELL	1
L/HE05	2 to 1 MUX	1–U CELL	2
L/HE06	2–2 OR/AND	1–U CELL	2
L/HE07	2–2 OR/EXOR	1–U CELL	2
HE08	2 to 1 MUX with ENABE LOW (Inverting))	1–U CELL	2
HE09	2 to 1 MUX with ENABLE LOW (Non–Inverting)	1–U CELL	2
L/HE10	2–2 OR/NAND	1–U CELL	2
L/HE11	2 to 1 MUX with ENABLE LOW	1–U CELL	2
L/HE12	DIFFERENTIAL OUTPUT BUFFER	2–U CELL	1
L/HE50	D LATCH with CLOCK ENABLE LOW	1–U CELL	2
HE70	DIFFERENTIAL OUTPUT BUFFER	2–U CELLS	1
HE71	OPEN COLLECTOR DIFFERENTIAL OUTPUT BUFFER	2–U CELLS	1
LE75	OFF–CHIP TERMINATION PAD	1–U CELL	1
CUTOFF OUTPUT (ZE) MACROS, 50 & 25 ohm			
ZE00	4–INPUT OR (50 ohm)	1–U CELL	1
ZE50	4–INPUT OR (25 ohm)	1–U CELL	2
STECL I/O (S) MACROS			
LS00	2–INPUT OR	1–U CELL	1
LS50	INPUT BUFFER	1–U CELL	1
BIDIRECTIONAL I/O (B) MACROS, 50 & 25 ohm			
HB26	2–2 OR/AND with INPUT BUFFER (50 ohm output)	1–U CELL	2
HB27	2–2 OR/NAND with INPUT BUFFER (50 ohm output)	1–U CELL	2
HB28	2 to 1 MUX LOW ENABLE with INPUT BUFFER (50 ohm output)	1–U CELL	2
HB29	4–INPUT OR with INPUT BUFFER (50 ohm output)	1–U CELL	1
HB30	4–INPUT NOR with INPUT BUFFER (50 ohm output)	1–U CELL	1
HB50	4–INPUT OR with INPUT BUFFER (25 ohm cutoff output)	1–U CELL	2
HB51	4–INPUT NOR with INPUT BUFFER (25 ohm cutoff output)	1–U CELL	2
HB76	4–INPUT OR with INPUT BUFFER (50 ohm cutoff output)	1–U CELL	1

TTL and PETL I/O Macros (U–Cells)

Macro	Function	Size	SG
INPUT TTL TO ECL (T: 00–29) MACROS			
L/HT00	TRANSLATOR with True and Complement	1-U CELL	1
OUTPUT ECL TO TTL (T: 30–59) MACROS			
L/HT30	NOR TRANSLATOR	1-U CELL	1
L/HT31	NOR TRANSLATOR with TTL Tri-State Enable	1-U CELL	1
L/HT33	OR TRANSLATOR	1-U CELL	1
L/HT36	OR TRANSLATOR with ECL Tri-State Enable	1-U CELL	2
L/HT37	NOR TRANSLATOR with ECL Tri-State Enable	1-U CELL	2
BIDIRECTIONAL I/O (T: 60–89) MACROS			
L/HT60	ECL 2-INPUT NOR TRANSLATOR and TTL to ECL INPUT BUFFER with TTL Tri-State Enable	1-U CELL	1
L/HT63	ECL 2-INPUT OR TRANSLATOR and TTL to ECL INPUT BUFFER with ECL Tri-State Enable	1-U CELL	1
L/HT64	ECL 2-INPUT NOR TRANSLATOR and TTL to ECL INPUT BUFFER with ECL Tri-State Enable	1-U CELL	1
ECL TO TRI–STATE CONTROL (T: 90) MACRO			
L/HT90	ECL to Tri-State Control NOR TRANSLATOR	1-U CELL	1
INPUT TTL TO PECL (P: 00–29) MACROS			
L/HP00	TRANSLATOR with True and Complement	1-U CELL	1
OUTPUT PECL TO TTL (P: 30–59) MACROS			
L/HP30	NOR TRANSLATOR	1-U CELL	1
L/HP33	OR TRANSLATOR	1-U CELL	1
L/HP36	OR TRANSLATOR with PECL Tri-State Enable	1-U CELL	1
L/HP37	NOR TRANSLATOR with PECL Tri-State Enable	1-U CELL	1
BIDIRECTIONAL I/O (P: 60–89) MACROS			
L/HP63	PECL 2-INPUT OR TRANSLATOR and TTL to PECL INPUT BUFFER with PECL Tri-State Enable	1-U CELL	1
L/HP64	PECL 2-INPUT NOR TRANSLATOR and TTL to PECL INPUT BUFFER with PECL Tri-State Enable	1-U CELL	1

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1. Introduction

1.1 Arrays Covered in This Manual

This manual contains information about the MCA3 ETL Series which currently consists of three arrays: MCA6200ETL, MCA3200ETL, and MCA750ETL. The three arrays are part of the Motorola "Third Generation" arrays and offer identical performance, with the only differences among the arrays being gate counts and package types. The MCA3 ETL array types and features are summarized in Table 1–1. Consult ASIC Applications for array availability.

1.2 About the Manual

This manual specifies the functionality and performance characteristics of the MCA3 ETL Arrays. The manual contains three major divisions. The first part, consisting of Sections 1 thru 8, describes the features of the MCA3 ETL Series (Sections 1 thru 3), specifies the guidelines for DC (functional) logic design (Section 4), and characterizes AC performance with respect to loading and metal line length (Section 5). The use of CAD tools is described in Section 6, packaging and thermal considerations in Section 7, along with testability considerations in Section 8.

The second part, consisting of Section 9, is composed of the Macrocell Library and Specification. The "library" specifies the functionality, power, and timing considerations associated with each marcocell.

The third part, Section 10 – identified as the Appendix, contains the Master Library list of macros for the MCA3 ECL and ETL Series. Also, the DC electrical characteristics for MCA3 ETL arrays, test circuitry, product reliability and ESD specifications are provided.

1.3 What is an ETL Macrocell Array?

An MCA3 ETL Macrocell Array is similar in design to existing MCA3 arrays such as the MCA10000 and MCA2200 ECL products. The extended feature in an ETL (ECL & TTL Levels) array is the additional processing capability of providing Schottky diodes in the I/O cells, thereby allowing for high performance ECL to TTL and TTL to ECL translation circuits. All MCA3 Series chips consist of an array of structures called "cells", each of which contains a number of unconnected transistors and resistors. Stored within Motorola's CAD system are the specifications for creating interconnecting patterns that can transform the unconnected transistors and resistors within each cell into SSI/MSI logic functions, called "macros". These macros take the form of standard MSI logic elements such as D flip-flops, full adders, latches, or 8-to-1 multiplexers. Presently, the Macrocell library for the MCA3 ETL Array Family contains more than 180 different logic functions (macros).

To generate an LSI design, the designer need only be concerned with developing the circuit (sometimes called an "option") by selecting the appropriate macros from the library, placing these in the desired cell locations and creating the necessary cell interconnection pattern. The macro interconnection information is transferred to the Motorola CAD system in the form of a network description (netlist). The computer itself generates the proper interconnecting metal pattern within each cell. Motorola carries an inventory of fully diffused wafers (wafers which have been processed up to the metalization steps). After the network description has been entered, the Motorola CAD system automatically generates the metal patterns necessary to implement the design. The metal layers are then added in the processing area where prototypes are fabricated and packaged for evaluation by the customer. The macrocell array concept offers the LSI designer a quicker turnaround time than full-custom or standard-cell approaches.

Compared with equivalent systems developed with discrete logic (separately packaged SSI/MSI logic functions), the high density of the MCA3 Series offers up to 400–1 reduction in system component count, with a power dissipation improvement (reduction) of as much as 20–1. This not only increases the MTBF for the circuit by reducing the part count, but also yields a substantial increase in system performance by reducing the need for interconnection between other chips on the same circuit board.

TABLE 1–1 MCA3 ETL Family Array Types and Features

Array	# of Equivalent Gates	# of Minimum Addressable Units (MAUs)	# Of Universal I/O Cells	Die Size (mils)	Packages
MCA750ETL	858	96	42	139 x 168	64 QFP
MCA3200ETL	3570	440	120	268 x 268	169 PGA/160 QFP
MCA6200ETL	6915	900	168	352 x 352	224 PGA/328 TAB*

*Contact factory for 328 TAB package information and availability.

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2. Features of the MCA3 ETL Macrocell Array Family

The MCA3 ETL Series contains three array densities offering the equivalent of 858 to 6915 gates (see Table 1-1). The arrays are fabricated from the MOSAIC III oxide-isolated, poly-electrode-transistor (PET) process. The MCA6200, 3200, and 750 ETL arrays, based on the MCA3 Low Power Array Version, deliver typical gate delays of 150 ps for a fanout of one with no metal interconnection between gates. MCA3 ETL arrays have complete internal library compatibility with all MCA3 ECL Macrocell Arrays, but with a new I/O macro logic library. All arrays include fully programmable I/O capable of MECL 100K, PECL (Pseudo-ECL), and TTL logic family interfaces (see Table 2-1 and Section 3.1). Additional features include three-level series-gated macrocells for increased density and performance, expandable macros, series-terminated ECL (STECL) outputs, and sufficient channels for automatic routing.

All ETL arrays are wirebonded and available in the package listed for each array in Table 1-1. Package data is given in Section 7.

TABLE 2-1 MCA3 ETL Array Features

1. Compatible with ECL 100K, 100E, PECL (ECL @ +5.0V), and TTL input/output logic levels
2. Fully programmable I/O cell (U-cell) capable of all compatibility options and translations
3. Macro power from: 1.2 - 2.4mW /2-input OR @ -4.5V
4. Inputs capable of operating at 2.6 GHz; Outputs operational at 1.6 GHz
5. Input cell delays: 200 ps (H macro); 275 ps (L macro) worst case
6. Internal cell delays: 200 ps (H macro); 250 ps (L macro) worst case (2-input OR, FO=1, metal=0)
7. Output cell delays: approx. 350 ps worst case (+ package delay: 100 - 400 ps)
8. TTL input translation delay: 700 ps (H macro); 850 ps (L macro) worst case
9. TTL output translation delay: 2475 ps worst case @ 15pF and 24mA output current
10. Standard and cutoff 50 and 25 ohm ECL output drivers. Optional low-power 60 ohm drivers
11. TTL push pull and tri-state outputs. 12mA and 24mA output current sinks
12. Bidirectional ECL and TTL I/O macros
13. Compatible with FAST™ TTL circuitry
14. Series-Terminated (STECL) outputs with on-chip series resistors and programmable current sinks
15. Expandable MUX/DECODE macro functions
16. Three-level series gated macros available for increased functional density and performance
17. Typical array power: 1-2 Watts for 750ETL; 4-7 Watts for 3200ETL; 7-12 Watts for 6200ETL

2.1 MOSAIC III Technology

The MCA3 ETL arrays are implemented using a high-performance process called MOSAIC III. This third-generation process (see Figure 2-1) is oxide-isolated in the same manner as was its predecessor, MOSAIC II. The key improvement over MOSAIC II is the use of the poly-electrode-transistor (PET) structure which utilizes p+ polysilicon for extrinsic base doping of the base electrode and n+ polysilicon for the emitter. The polysilicon base electrode greatly enhances switching speed by reducing the series base resistance and collector-base capacitance.

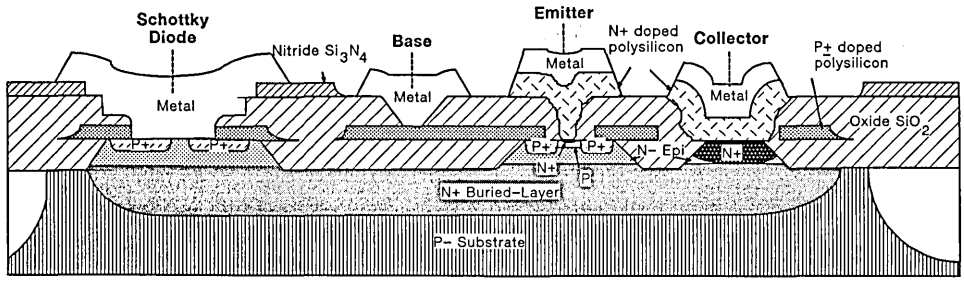

Figure 2-1 MOSAIC III Schottky-Transistor Cross-Section

An "edge-defined" technique gives the process the capability to produce submicron emitter widths without the use of submicron lithography. MOSAIC III allows for polysilicon resistors in order to reduce node capacitance where circuit speed is critical. A Schottky module is inserted into the standard MOSAIC III process for fabrication of guarded and non-guarded Schottky devices. With Schottky barrier fabrication, high performance TTL inputs and outputs are possible.

2.2 Internal Architecture

There are two types of cells: internal major (M) cells, and I/O universal (U) cells. The number of cells and I/O pads is given in Table 1-1. Each cell contains a fixed array of unconnected transistors and resistors; all macrocell array chips are built from a standard semiconductor diffusion mask set, and can be fabricated up to the metallization steps. The extensive MCA3 Macrocell Library of internal functions, beginning on page 9-4, contains descriptions of more than 180 logic functions which can be implemented in the (M) cells. A versatile I/O logic and translator macro selection is available for use in the (U) cells. Using this library, the designer can create schematics on the Apollo/HP™ Mentor™ Computer platforms.

Each internal major cell can be subdivided into quarter cells. Macros in the MCA3 internal library use from one to four quarter cells to implement a specific logic function. One internal major cell, for example, can contain a D flip-flop (291) and a full adder (282), each of which occupies two quarter cells.

The power, ground, and bias supply line interconnections are made automatically by the CAD system. Routing channels in the vertical direction (between macrocell columns) are for first layer metal routing tracks while the channels in the horizontal direction (over the macrocell rows) are for second layer metal routing. Second layer metal routing can be placed over the cell without interfering with the macro in that cell since all macros are interconnected on first layer metal. (Second layer metal is separated from the first layer of metal by a layer of dielectric isolation.) Connections between the first and second layers of metal are accomplished with "vias". A third layer of metal is used for power and ground distribution to minimize voltage drops. This third metal layer is transparent to the user.

2.3 I/O Structure

The placement of I/O macros within U-cells around the periphery of the array's internal logic permits the chip's interface pins to be programmed as inputs, outputs, or bidirectional I/O. The U-cells also provide the function of ECL, PECL, or TTL logic level translation. Each array contains one U-cell for each available I/O signal pad. The number of I/O signal pads for each array is listed in Table 1-1. Refer to Sections 3.1 and 4 for I/O types and configuration rules.

2.4 Speed/Power Programmability

The speed/power programmability feature of the MCA3 ETL arrays allows the designer to choose from three M-cell macro performance levels (see Figure 2-2). This is possible through specifying Low Power (L), High Power (H), or High Drive (L) macros in the design. Current-source switch currents are automatically adjusted according to the macro power level selected. Only specific macros (utilized when macro delay time or fanout are critical factors) are offered in the High Drive (L) version. Note that the (L) associated with High Drive is used for the purpose of macro classification and does not denote low power.

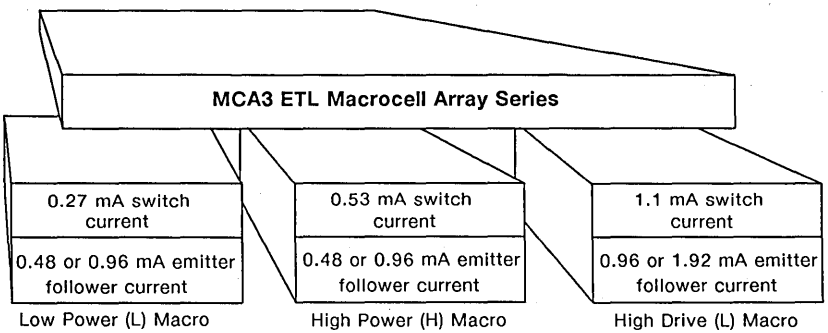

Figure 2-2 Speed/Power Programmability

3. Macrocell Array Description

3.1 Operational Modes and Allowed I/O

MCA3 ETL arrays can operate for several types of voltage level interfaces. The four primary modes of operation are shown in figure 3-1. A description of each mode and its use follows. Information on specific I/O connection rules can be found in Section 4. The available I/O macros to implement the following interfaces are listed in the macro library in Section 9.6. All ECL and PECL inputs onto the array, including bidirectional I/O, have a 75K ohm resistor pulldown to V_{EEE} as well as an ESD protection circuit. All TTL inputs onto the array have ESD protection and an input diode clamp.

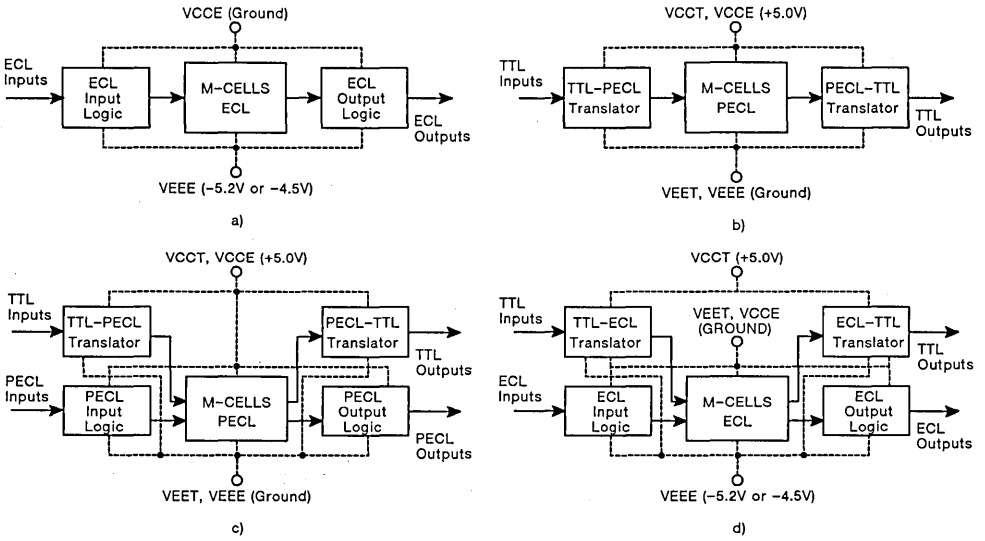

Figure 3-1 MCA3 ETL Array Signal Interface. a) ECL Signal b) TTL signal c) PECL/TTL Signal d) ECL/TTL Signal

3.1.1 Standard ECL I/O (a)

This mode is used to interface to 100K ECL signals only. Voltage requirements are -5.2 or -4.5 Vdc. Single-ended and differential ouput macros can be selected for driving external 68 and 50 ohm lines as well as cutoff driver outputs for 25 and 50 ohm bus interfaces. All specification in the manual for low power outputs assume a 68 ohm external load to -2.0 Vdc. The designer, however, may use an external load of 60 ohms with a slight loss in V_{OH} noise margin. Refer to Section 10.2 for V_{OH} and V_{OL} specifications.

3.1.2 TTL I/O (b)

MCA3 ETL arrays can be used with only +5.0 V and ground supplies. The internal portion of the array operates in Psuedo ECL (PECL, +5 & 0 volts), while the I/O are at TTL levels. The TTL outputs supported are push pull and tri-state outputs with 12 and 24 mA output current sinks.

3.1.3 PECL/TTL I/O (c)

This mode requires the same +5.0 Vdc supply as in (b), but allows for PECL levels in addition to the TTL signals to be brought off chip. PECL levels are given in the Electrical Characteristics section. Only temperature compensated signals (100K) are possible.

3.1.4 ECL/TTL I/O (d)

Mixed ECL and TTL I/O is allowed when both +5.0 Vdc and -5.2/-4.5 Vdc voltage levels are supplied. In this mode, ECL and TTL interfaces given in Sections 3.1.1 and 3.1.2 are valid.

3.1.5 Bidirectional I/O

Bidirectional I/O are available in ECL, PECL, and TTL levels. Therefore, bidirectional I/O macros can be used with any supply voltage configuration.

3.2 Series–Terminated ECL (STECL)

To facilitate multichip design, the array provides ECL outputs with programmable current-source pulldowns and selectable, on-chip series-terminating resistors. Figure 3-2 shows the STECL output circuit. The current source pulldown may be programmed to either 6 or 10 mA. The series resistor may be programmed to a value of 0, 27, or 40 ohms. The CAD system also allows the same type of current source used for a STECL output to be attached to an input pad. STECL I/O is ideal for applications where hybrid packaging constraints may make external line terminations difficult.

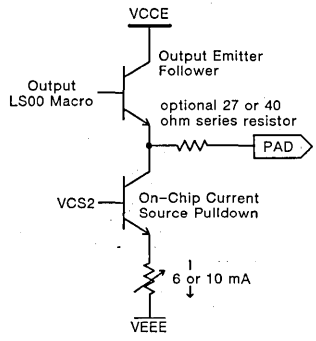

Figure 3–2 STECL Output

3.3 Series Gating

The value of ECL series-gating can be seen in the circuit schematic for the 6-input exclusive OR gate shown in Figure 3-4. To implement this function with gates would require thirty-two 6-input AND gates, one 32-input OR gate, and any additional gates required to form the true and complement of each input. If only 3-input gates were used, over one hundred of them would be needed to form the function.

A minimum of 224 connections would be required if single-level gates were used, compared to seven connections for the three-level series gated macro. Each output of the cell has a two-emitter transistor (a.k.a. "twin output") that allows twice the output emitter follower current to be selected for increased drive and performance. Connecting identical outputs together in this fashion (i.e. "twinning" the outputs) will allow an output emitter follower current of 0.96 mA. This also provides emitter-dotting (wired-OR) capability while retaining the non-dotted output function through the second emitter. All outputs of internal major cell macros are buffered and can be wire ORed with other macros. Refer to Section 4.2.6 for the rules on tying macro outputs together.

3.4 Internal Cell Architecture

The internal major (M) cells in the array comprise the internal area on the chip and are used for the majority of the logic capability. Each internal major cell contains 76 transistors and 76 resistors. Major cells are divided into four quadrants called "quarter cells". Figure 3-3 shows the uncommitted devices in a 1/4 cell. These components are connected together on first and second layer metal to form logic functions. Each macro in the internal major cell library specifies how much of the cell (either 1/4, 1/2, 3/4, or all) is needed to implement that particular function.

Figure 3-4 shows a 6-input exclusive OR macrocell function which is implemented in 1/2 of an internal major cell (i.e. in 2 quarter cells). The A and D inputs are connected to the top level of the series-gated tree. The B and E inputs are connected to an input follower which connects to the middle level of the series-gated current tree. The C and F inputs enter the lowest level of the current tree through an input follower and a diode drop. Refer to Section 9 for details on how middle and lower-level inputs are indicated in the Macrocell Library. Note that the output emitter followers utilize an active device current source referenced to V_{EEE}.

3.5 Using the Thermal Diode

A thermal diode can be selected for each of the MCA3 ETL arrays in order to monitor the junction temperature of the die. Two versions of the thermal diode are offered – a "one-pin" version and a "two-pin" version. The one-pin diode is selected in the FIX file (see Section 6.4.4) using the "$TDIODE" statement. The (+) terminal of the diode is connected to V_{CCE} and the (–) terminal is brought out to a die pad defined in Table 4-3. The two pin diode is selected using the "$TDIODE2" statement in the FIX file (see Section 6.4.4). Both the (+) and (–) terminals of the of this diode are connected to die pads defined in Table 4-3. For TDIODE placement restrictions see Section 4.3.

The maximum allowed current for the thermal diode is 10mA. The recommended current is 5mA. The breakdown voltage against the substrate (V_{EEE}) is typically 7 Vdc. The thermal diode tracks typically at –1.46 mV/°C for a current of 10mA.

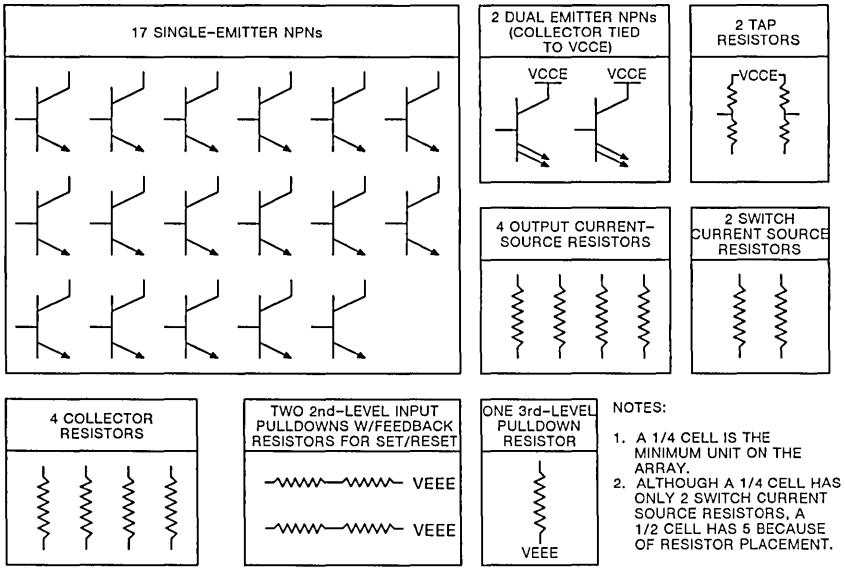

Figure 3–3 Internal Cell Architecture – 1/4 Cell

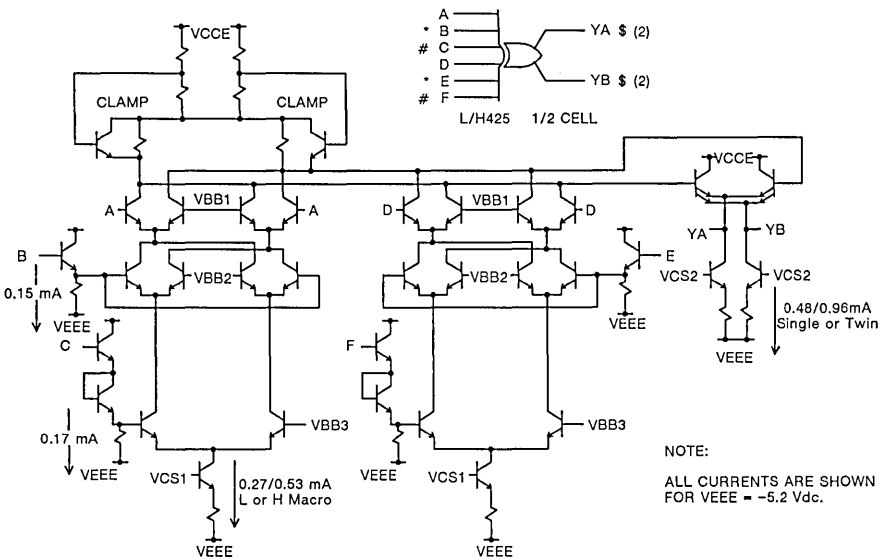

Figure 3–4 Internal (M) Cell Example: 6 Input Exclusive OR

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4. DC (Functional) Logic Design Considerations

This section contains logic design considerations which should be observed when developing a design as well as guidelines for calculating various DC parameters associated with the design. For detailed information on how to actually implement the design using the Open Architecture CAD System (OACS™) or the WACC CAD system (e.g. creating the FIX file, etc.), refer to Section 6. For workstation designs on Motorola's OACS™, complete information is available in the OACS Users Guide.

NOTATION:

In this manual, the following naming conventions are used:

Input and Output interface cells are referred to as 'U-cells' or Universal Cells. These cells are placed around the periphery of the chip. There is one cell for each I/O pad on the array. U-cells are capable of ECL/PECL buffer and logic inputs or outputs as well as TTL to ECL/PECL input and ECL/PECL to TTL output translations. A table listing available U-cell macro functions can be found in Section 9.

Internal major cells are referred to as 'M-cells' or Major Cells. Macrocells implemented in the internal portion of the array have either an 'H' or 'L' prefix, depending on the speed/power level selected, followed by the macro number (e.g. H202). See Section 2.4 and Figure 2-2 for a complete explanation of switch and output emitter follower (OEF) currents. A table listing available M-cell macro functions can be found in Section 9.6.

UPPER and LOWER Level Inputs

Inputs to the top level of a series-gated current switch are called 'UPPER' or 'UPPER LEVEL' inputs. If an input does not have an asterisk (*) or a pound sign (#) and does not appear in the AC loading table for that macro, then it is an UPPER LEVEL input. Inputs to the second level of a series-gated current switch are marked with an asterisk (*) and third level inputs are marked with a pound sign (#). Both second and third level inputs are referred to as 'LOWER' or 'LOWER LEVEL' inputs. Note that except for the case of input pads driving internal cells directly, UPPER and LOWER level inputs are not functionally different. The primary difference between the two is in speed, and in calculating AC and DC loading.

RESET and SET Input Considerations for Flip-flop and Latch Macros

The reset and/or set inputs of flip-flop and latch macros are marked with an '*' to signify that they **may not** be directly connected to external input pads. These inputs follow the I/O connection rules for second level inputs, since the input bias point on these inputs is referenced to a resistor divider rather than the bias driver. These reset and/or set '*' inputs must be driven by YA, YB, etc. outputs from interface or internal macros.

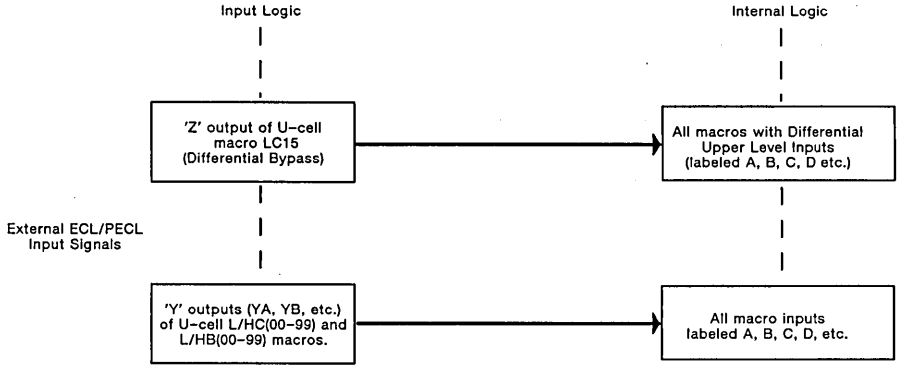


Figure 4-1 Allowed ECL/PECL Input Connections

4.1 I/O Connection Rules

4.1.1 I/O Pin Assignments

Pad to pin I/O configurations and array floorplan diagrams are given for each array beginning on page 4-10. Pin locations and other package related information can be found in Section 7, Packaging.

4.1.2 Input Configurations

The MCA3 ETL family uses input interface macros (U-cells) as input buffers and to translate the logic levels of external 100K or 100E (ECLinPS) levels to internal 10KH levels or external TTL levels to internal 10KH levels. The internal part of the array uses 10KH tracking for V_{BB}. The logic swing is reduced to approximately 550 mV in order to enhance the speed of the core circuitry and to allow for three-level series gating without encountering saturation problems.

Input Rules

Allowed ECL and PECL input connections are shown in Figure 4-1. Allowed TTL input connections are displayed in Figure 4-2. In addition, the following rule applies to inputs:

1. Two input pads may **not** be connected together on the array to form a wired-OR configuration.
2. All open TTL inputs represent a logic high.

Input pulldown resistors are present on all ECL input and bidirectional pins. The resistor has a 75K ohm value and is terminated to the V_{EEE} power rail, through two series diodes.

4.1.3 Current Source Inputs

Package pin inputs with active current source pulldowns can be selected for an ECL input line termination. These current sinks are the same ones used in implementing STECL outputs (LSxx Macros). The designer should note that a current source input behaves like an open line. The current source input does not provide a matched impedance termination. An unused current source input pin must be connected to a low impedance source with a V_{OL} or V_{OH} voltage in order to avoid current source regulation problems.

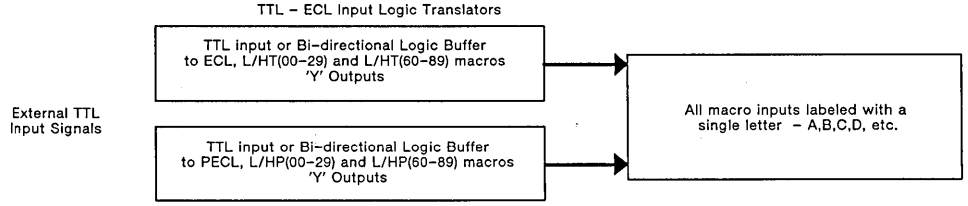


Figure 4-2 Allowed TTL Input Connections

4.1.4 Output Configurations

Outputs on the array can be configured to drive several levels and options. Available output signals are described in Section 3.1. The diagram in Figure 4–3 shows the ECL/PECL macro names and output types that are available on the arrays. Figure 4–4 shows the allowed TTL and PECL output options. ECL differential output macros require two cells and consequentially two output pads.

Using 25 and 50 Ohm Cutoff Drivers

Outputs on the low power array with 25 or 50 ohm cutoff drivers are useful in interfacing with bidirectional ECL/PECL busses since they operate in a very high impedance cutoff mode when the output is in the low state. Each 25 ohm output uses four output transistors. (A normal 50 ohm output uses two transistors.) The user should note that the V_{OH} specifications are different for 25 and 50 ohm cutoff outputs (see Section 10.2 for details).

The current supplied to the external load resistor for "standard" ECL/PECL outputs (non-STECL outputs) is given in Table 4–1. This table assumes a 50 ohm load is used for the 50 ohm outputs (both normal and cutoff), a 60 or 68 ohm load is used for the 68 ohm outputs, and a 25 ohm load is used for the 25 ohm cutoff drivers.

TABLE 4–1 Output Load Current for Standard ECL/PECL Outputs

OUTPUT TYPE	V_{OH}	V_{OL}
50 ohm	22 ma	5.0 ma
60 ohm	18.3 ma	4.2 ma
68 ohm	16.2 ma	3.7 ma
25 ohm cutoff	44 ma	0.0 ma
50 ohm cutoff	22 ma	0.0 ma

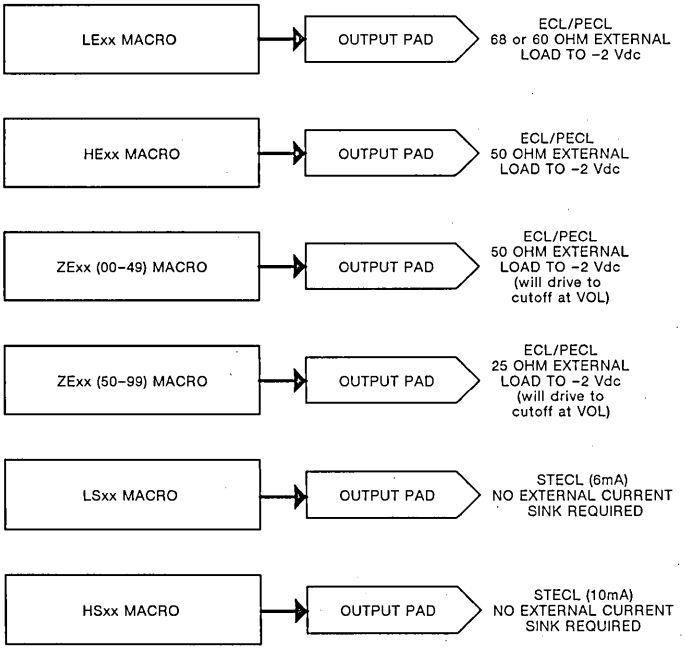


Figure 4–3 Allowed ECL/PECL Output Connections

STECL Outputs

STECL outputs provide either a 6 or 10 mA current sink on the array itself. In a strictly series-terminated application (assuming no external load resistors), the only current supplied by STECL outputs through the output pin will be the base currents of the inputs being driven.

Tri-State Outputs

There are two types of tri-state controlled TTL output macros. The first category consists of macros T31 and T60 which require TTL level inputs on their respective tri-state control lines (labeled 'CT'). These macros require the addition of an ECL to tri-state control translator macro (T90, with output labeled 'TA') to drive their tri-state control inputs ('CT'). The HT90 macro can only drive HT31 and HT60 macros. The LT90 macro can only drive LT31 and LT60 macros. The second category of tri-state controlled TTL output macros consists of T36, T37, T63, and T64 along with P36, P37, P63 and P64 which utilize normal ECL (or PECL if a Pxx macro) logic levels to control their respective tri-state control inputs (labeled '*C'). No other logic level translator macros are required for this group of TTL output macros. Tri-state enable to output delay versus output capacitance curves for TTL OR/NOR and tri-state output macros are shown in Section 5.1.9.

Output Rules

In addition to Figures 4-3 and 4-4, the following rules apply to outputs:

1. Any restrictions pertaining to the maximum number of outputs which can be simultaneously switched. See Section 5.1.6.
2. The Z outputs of U-cell E macros can only be connected to the inputs of U or M-cell macros if both outputs (ZA and ZB) are used to drive an upper level differential macro input.
3. The maximum current allowed on a STECL output device is 11 mA. This means that for a 6 mA STECL output, up to 5 mA of source current may flow through the output pin to the external load. For a 10 mA STECL output, 1 mA of additional load current may be sourced.

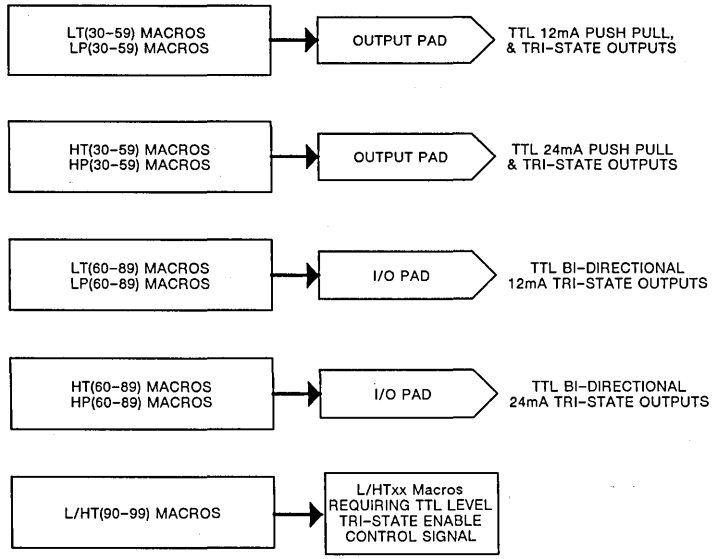


Figure 4-4 Allowed TTL Output Connections

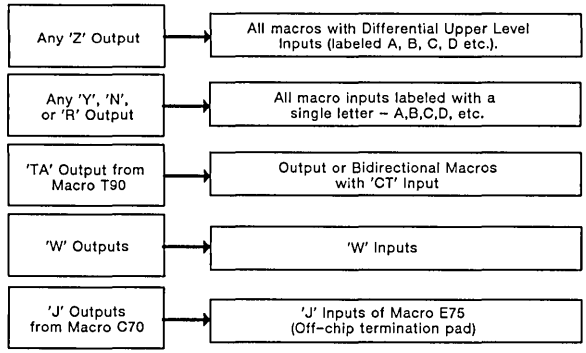


Figure 4–5 Allowed Internal Connections

4

4.2 Internal Connection Rules

Allowed internal cell connection rules are shown in Figure 4–5. Sections 4.2.1 through 4.2.9 contain additional rules and requirements for internal macro connections.

4.2.1 Restrictions on Using Three–Level Series Gated Macros

Macrocells which employ **three–level series gating** can **only** be used with a supply voltage of V_{EEE} = –5.2 Vdc for standard ECL, or with V_{CCE} = +5.0 Vdc and V_{EEE} = 0.0 Vdc for PECL. If a –4.5 volt V_{EEE} supply is used, then no three–level series gated macrocell functions may be included in the design. The Macro Quick Reference Guide in Section 9 of this manual indicates via shading which functions use three–level series gating. The levels of series gating for each macro are also included along with cell size below each macro number in the library (Section 9.6).

4.2.2 Rules for 'W' and 'J' Inputs and Outputs

Certain macrocells in the MCA3 library have inputs and/or outputs with specific interconnection restrictions. Both 'W' and 'J' inputs have input names with two letters, the first of which is the letter 'W' or 'J'. Similarly, the respective outputs begin with the letter 'W' or 'J'.

'W' outputs can **only** be connected to **'W' inputs.** The converse is also true. In addition, **'W' outputs cannot be connected together to form a wired–OR.** The DC fanout restrictions for 'W' outputs are the same as for an 'L' or 'H' macro with no external wired–OR. (See Table 4–2.)

The significant difference in 'W' outputs is that they switch at voltage levels equivalent to one diode drop below V_{BB1}. This voltage, V_{BB2}, is approximately –2.05 Vdc.

Likewise, **'J' outputs** can **only** be connected to **'J' inputs.** The 'J' input of macro C70 can only be connected to the 'J' output of macro E75, and this macro interface is used only for off–chip input termination.

4.2.3 Rules for 'R' or 'N' Outputs

Several of the macros in the library have outputs whose names begin with the letter 'R' or 'N' (commonly referred to as "R outputs" or "N outputs"). Macro 882, for instance, has two outputs, RA and RB. Macro 895 has one 'N' output, 'NA'. 'R' outputs utilize resistor pulldowns rather than the standard current source pulldowns used on 'Y' and 'Z' outputs. The value of resistance used is 4640 ohms. The connection rules for 'R' outputs are the same as 'Y' outputs with one important exception. **An 'R' or 'N' output may not be used in a wired–OR.** The designer should also note that the metal/fanout delay equations are different for 'R' outputs. Refer to Section 5 for the specific timing rules.

4.2.4 Unused Inputs and Outputs

The unused outputs of any cell can be left floating (unconnected). Unused ECL inputs in the array will automatically be forced to a 'low' voltage (Logic '0') by the CAD system (the input base is shorted to the emitter). There are no special provisions for creating a 'high' (Logic '1') on an unused input. A Logic '1' for internal cells can be generated using a spare gate on an internal or input macro.

4.2.5 Maximum Fanout of Macro Outputs

Refer to Table 4–2 and Section 9.2.2 for the DC fanout restrictions for the various types of macrocell outputs.

TABLE 4–2 Maximum DC Fanout

ETL ARRAYS Macro Type	MAX DC FANOUT (UNIT LOADS)**					
	Single Outputs Driven Separatley			Twin Outputs Connected Together		
	With no External Wired–OR	With External Wired–OR		With no External Wired–OR	With External Wired–OR	
		20mV	35mV		20mV	35mV
L Macro (M–Cell, U–Cell) (Except Z outputs of E Macros)	24	15	5	38	24	8
H Macro (M–Cell, U–Cell) (Except Z outputs of E Macros and QUAD BUFFERS*)	32	24	17	48	38	26
HI DRIVE MACROS	37	30	23	55	44	35
L QUAD BUFFERS (M–Cell, U–Cell)	6	–	–	10	–	–
H QUAD BUFFERS (M–Cell, U–Cell)	24	15	5	38	24	8
E Macros. Z Output (U–Cell)	48	38	26	–	–	–
P90 & T90, TA Output	10	–	–	–	–	–

NOTES:
1. *QUAD BUFFERS include all macros with four or more functionally equivalent outputs, such as macro L501.
2. **UNIT LOADS – Input loading values in the Macrocell Library must be multiplied by 2 for the UPPER LEVEL inputs of INTERNAL high power (H) macros. Loading for each internal macrocell input is one unless otherwise specified in parentheses in the Macrocell Library.
3. The 20mV and 35mV refer to the amount of VOH noise margin which the user wishes to allow for voltage drops between two outputs on a wired–OR. These voltage drops can be calculated on Motorola CAD system using the VDROP program.

4.2.6 Wired–OR Rules

The outputs of macrocells can be tied together to form a "wired–OR" function, subject to certain rules. The wired–OR rules contain both connection restrictions as well as maximum limits based on Nw and Ne. See Figure 4–6 for examples of wired–ORs.

Nw is the wired–OR total on a net. This is essentially the number of functionally unique outputs which are tied together to form the wired–OR. Twin outputs which are connected together only count as one in this total. This number must include internal wired ORs as indicated by a number in parentheses next to the output in the Macrocell Library.

Ne is the emitter total on a net. Ne is the total number of individual emitters which are tied together to form a wired–OR. Ne also includes internal wired ORs as indicated in the Macrocell Library.

Wired–OR Rules:

1. **Nw must be less than or equal to 4.**
2. **If any un–twinned outputs are part of the wired–OR, then only one emitter follower current (EFC) pulldown must be on the net.**
3. **If two EFC pulldowns are tied to the net, then all outputs on the net must be twinned.**
4. **If one EFC pulldown is tied to the wired–OR net, the Ne must be less than or equal to 4.**
5. **A 'Z' output can only be tied to other 'Z' outputs in order to create a wired–OR.**
6. **A 'Y' output can only be tied to another 'Y' output in order to create a wired–OR.**
7. **The outputs of HI DRIVE macro functions can only be wire ORed with the outputs of other HI DRIVE macrocells or twin outputs of normal macros.**
8. **'N' outputs may not be wire ORed.**
9. **'R' outputs may not be wire ORed.**
10. **'W' outputs may not be wire ORed.**
11. **'TA' outputs may not be wire ORed.**
12. **The metal length between outputs on a wired–OR net is limited due to voltage drops from an active output to the current sink. Refer to Section 6.5 for details. The VDROP program on the Motorola CAD system will check for voltage drop violations using a limit of either 20 or 35 mV. The designer can estimate the worst–case voltage drop by multiplying the estimated maximum metal lengths (L_{M1} and L_{M2}) between two outputs on the wired–OR net by the resistance per mil as given in Section 5.2.2 and in turn by the OEF current on the net.**

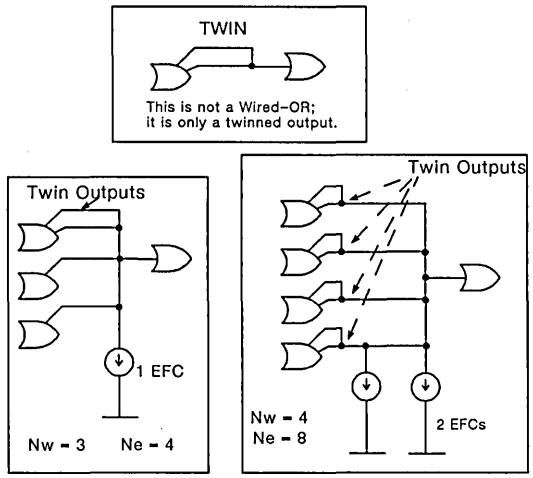


Figure 4–6 Wired–OR Examples

13. **Macros which have an internal wired–OR may not be used as part of a clock distribution tree.**

Note: By default, the Motorola CAD system will attach one EFC pulldown to each output of a macro which is used. Therefore, if a wired–OR is indicated in the SUPERNET file, then an entry must be made in the $MAMP section of the FIX file which turns off the extra current source(s). Otherwise, a new $MAMP property value is assigned to the net when using the workstation OACS kit.

4.2.7 Twin Outputs

For driving high fanouts, certain internal major cell outputs can be tied together for increased drive. These are known as "twin outputs" and always have identical logic functions. Twice the output follower current can be used when outputs are "twinned", which provides an OEF current of 0.96 mA. If high drive (HI DRIVE) macro outputs are twinned, the OEF current is 1.92 mA.

4.2.8 Designing Latches With Gates

When designing logic requiring latches, it is recommended that the designer use the latches and flip–flops in the library. The logic equivalent of a latch shows only the Q output being fed back. However, the actual circuit is implemented with Q and $\overline{Q}$ outputs fed back differentially to the input through separate emitter followers in most of the macros. This method eliminates race conditions caused by delay differences when switching the clock enable lines on the lower parts of the current tree (* and # inputs). This insures reliable operation and superior noise margins compared to single–ended feedback. All of the macros in the MCA3 library use differential feedback.

The logic designer is **not allowed** to make latches out of gates in the MCA Library using single–ended feedback as described below. As an example of a single–ended feedback latch, the 2–to–1 MUX (H254 or L254) can be made into a latch similar to the logic equivalent shown for H/L293. This could be accomplished by tying the YA output to the C input, using the A input as the data input, and using the E input as a clock enable. Designing this type of latch is not allowed.

The logic designer is allowed to make a latch or flip–flop out of gates only if differential feedback is a part of the design. However, the gates must use macros with upper level inputs only (no * or # inputs) and the output of the gates must not contain internal or external wired–OR connections. An example of an allowed design is when using two H/L202's to form a set–reset latch. Note that an indeterminate condition exists if the set and reset inputs are simultaneously switched from a high to low state. This is a normal condition for this type of flip–flop.

If a latch is needed with a number of data inputs, a latch in the library (such as L/H293) should be used with a gating function (such as L/H215) connected to the data input of the latch. If the designer needs a JK flip–flop, a JK flip–flop can be formed using L/H292 and labeling J to the A input, K to the B input, and connecting the YJ output to the D input.

4.2.9 Quad Buffer Rules

The following macrocell functions in the library have four logically equivalent outputs: Internal macro functions 501, 502, 571 (which is equivalent to two Quad Buffers), I01, I02, I04, I05, I07, and I08. These macros are referred to as "Quad Buffers". The outputs of these macros consist of two double-emitter transistors whose bases are connected together. The following rules apply to Quad Buffers:

1. Only twin emitters may be connected together on a Quad Buffer. This means that the 'YA' output may only be connected to the YB output, the 'YC' output may only be connected to the 'YD' output, the 'YD' to the 'YF', and so on.
2. The low power versions of the Quad Buffers can only be used in the low power arrays.

The fanout restrictions for Quad Buffers are given in Table 4-2. Motorola recommends the use of the high power versions of these macros in designing low-skew clock distribution trees and in other timing-critical applications.

4.2.10 Using High Drive Macros

The MCA3 library contains several macrocells such as L474 which allow the designer to use twice the normal switch and OEF currents. These are designated as 'HI DRIVE' macrocells in the library. Fanout restrictions for HI DRIVE functions are given in Table 4-2. HI DRIVE macros can only be wire ORed with other HI DRIVE macros or with twinned outputs of "normal" macros.

4.3 Macrocell Array Floorplans, Reference Tables, and Placement Restrictions

On the following pages are the floorplans and reference (pad to pin) tables for the MCA3 ETL Series arrays. Figure 4-7 thru 4-10 provide the cell grouping floorplans for MCA750ETL, MCA3200ETL, and MCA6200ETL arrays repectively. Tables 4-5 thru 4-8 provide pad to pin cross-reference data for each array. Macro placement restrictions for the arrays are categorized and described in the following paragraphs:

4.3.1 Thermal Diode Placement Restrictions

Each array has specified die pads with associated package pins that may be used for thermal diode connection. Table 4-3 defines the allowed die pads for thermal diode placement on each type of ETL array. Refer to Tables 4-5 thru 4-8 for die pad to package pin cross-reference data.

TABLE 4-3 Die Pads for TDIODE Placement

ETL Array	Allowed Die Pads	
	TDIODE	TDIODE2
MCA6200 & 3200	7(-)	7(-) & 8(+)
MCA750	63(-)	63(-) & 64(+)

4.3.2 Macro T90 Placement Restrictions

Selection of the T90 (ECL to TTL tri-state control) macro is configuration limited to one U-cell within a specific block of U-cells. Table 4-4 defines the blocks of tri-state groupings for each type of array that may include one T90 macro. Two or more T90 macros **may not** be selected within a specific block of U-cells. However, each T90 macro may provide tri-state control for all other U-cells within that specific block of U-cells. Each T90 macro requires the use of a complete U-cell, but does not use the pad. The associated pad (identical number to the U-cell site location number selected for macro T90 placement) cannot be used for external connection when the T90 macro is selected for that specific U-cell.

4.3.3 Edge or Level Sensitive Signal Placement Rules and Recommendations

The following recommendations and rules are to insure that the AC noise margin is sufficient to produce the highest possible reliability of operation for all combinations of possible I/O pin combinations.

Differential Drive Recommendation

Motorola recommends differential drive on all edge or level sensitive inputs such as CLOCK, RESET and SET signals. This is highly recommended for designs having 25 or 50 ohm cutoff bus outputs and TTL outputs that can be switched simultaneously. Differential drive provides superior noise margins and eliminates ground bounce problems at the input interface, since a reference voltage is not required on the differential input cell.

Rules for Single-ended Drive on Level Sensitive Inputs

For designs that require single-ended drive on edge or level sensitive inputs, the following rules apply:

1. All outputs that can be switched simultaneously, except STECL, must be separated from edge or level sensitive single-ended inputs such as CLOCK, RESET and SET signals as defined below in rules (1a) and (1b). Power and ground pads are allowed to be adjacent to sensitive input pads. There are **no restrictions on differential inputs** that are edge or level sensitive.

The following rule (1a) addresses the requirements for the wire bonded PGA packages, 169 PGA and 224 PGA:

1a The adjacent two pads on both sides of a sensitive input must **not** have outputs that are switching simultaneously in the same direction within a 2 ns window among themselves, or with any other bank of outputs (4 or more) on the array. If slowdown capacitors are used for all outputs that can be switched simultaneously, then the adjacent two pads on one side of the sensitive input can be part of a bank of outputs that are switching simultaneously as long as the adjacent two pads on the other side of the sensitive inputs are not switched simultaneously in the same direction within the 2 ns window.

For instance, an MCA3200ETL array in a 169 PGA can have a single-ended clock input on die pad 10 as long as die pads 8, 9, 11 and 12 do not have outputs that are switching simultaneously in a 2 ns window among themselves, or with any other bank of outputs. However, if all outputs that can be switched simultaneously use slowdown capacitors, then die pads 8 and 9 can be outputs that are switched simultaneously with a bank of outputs as long as die pads 11 and 12 are not switched simultaneously in the same direction within the 2 ns window.

The following rule (1b) addresses the requirements for the 64 and 160 QFP packages:

1b The adjacent pad on both sides of a sensitive input must not have outputs that are switching simultaneously in the same direction within a 2 ns window among themselves, or with any other bank of outputs (4 or more) on the array. If slowdown capacitors are used for all outputs that can be switched simultaneously, then the adjacent pad on one side of the sensitive input can be part of a bank of outputs that are switching simultaneously as long as the adjacent pad on the other side of the sensitive input is not switched simultaneously in the same direction within a 2 ns window.

For instance, if the MCA750ETL array is in a 64 QFP package, a single-ended clock input on die pad 6 is allowed as long as die pads 5 and 7 do not have outputs that are switching simultaneously in a 2 ns window among themselves, or with any other bank of outputs. However, if all outputs that can be switched simultaneoucly use slowdown capacitors, then die pad 5 can be an output that is switched simultaneously with a bank of outputs as long as die pad 7 is not switched simultaneously in the same direction within the 2 ns window.

2. **All single-ended edge or level sensitive inputs** and the adjacent pins, as specified in rule (1) above, **must be manually fixed** with entries under the $FIX keyword in the <option> FIX file (see Section 6.4.4).

This rule (2) is required to satisfy rule (1), since the program for automatic placement of pins is not able to verify the I/O signal conditions which necessitate this requirement.

4.3.4 I/O Macro Placement Restrictions for U-Cells

I/O macros are placed in U-cell site locations around the periphery of the die. The number of the U-cell site location (e.g. B007) after the letter 'B' directly corresponds to the connecting die pad number (e.g. 7). I/O macros that physically require only one U-cell may be placed in any U-cell site location. However, I/O macros requiring two U-cells (primarily for differential inputs and outputs) may only be located in specifically identified 'paired' U-cells. Certain U-cell site locations (indentified by **shading** of those U-cells in Figures 4-7 thru 4-10) **may not** be used for macros requiring **two** U-cells. For the MCA750 array, U-cell site locations B009 and B041 may not be used for I/O macros requiring two U-cells. For the MCA3200 array, U-cell site locations B024, B029, B076, B081, B128, B133, B180, and B185 are similarly restricted. For the MCA6200 array, U-cell site locations B007, B068, B080, B141, B153, B214, B226, and B287 are similarly restricted.

I/O macros requiring two cells must be placed in specifically identified 'paired' U-cells. The 'paired' cells start in the upper left corner using the first permitted U-cell site location; the U-cell 'pairs' then rotate clockwise around the periphery of the die avoiding those U-cell site locations that are not permitted for I/O macros requiring two U-cells (shaded sites). For the MCA750 array, the first 'pair' are U-cell site locations B063 and B064, followed by next pair B001 and B002, etc. For the MCA6200 array, the first **permitted** 'pair' are B008 and B009. Die pads connected to U-cell 'pairs' are not separated by a horizontal line between die pad numbers in Pad to Pin Cross- Reference Tables 4-5 thru 4-8. Both U-cells of a 'pair' must be 'open' before placement of a two U-cell I/O macro in a specific U-cell site location.

When differential input macro LC70 is configured for off-chip termination, an open U-cell for macro LE75 must be available adjacent to each LC70 input requiring off-chip termination.

TABLE 4–4 U–Cell Block Assignments for Tri–State Control Groupings

Array	Block Assignments for Placement of Macro T90
MCA750ETL	(B001–B009 & B063–B064)), (B011–B020), (B031–B041), (B043–B052)
MCA3200ETL	(B007–B016), (B020–B024 & B029–B033), (B037–B046), (B059–B068), (B072–B076 & B081–B085), (B089–B098), (B111–B120), (B124–B128 & B133–B137), (B141–B150), (B163–B172), (B176–B180 & B185–B189), (B193–B202)
MCA6200ETL	(B007–B017), (B024–B029 & B031–B034), (B041–B044 & B046–B051), (B058–B068), (B080–B090), (B097–B102 & B104–B107), (B114–B117 & B119–B124), (B131–B141), (B153–B163), (B170–B175 & B177–B180), (B187–B190 & B192–B197), (B204–B214), (B226–B236), (B243–B248 & B250–B253), (B260–B263 & B265–B270), (B277–B287)

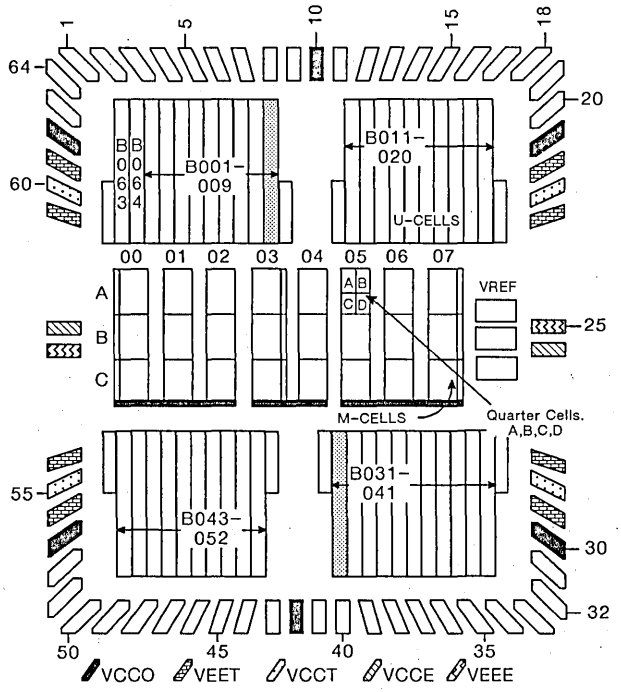


Figure 4–7 MCA750ETL Floorplan – 64 QFP (Wirebond)

NOTES:
1. U–cell site location numbers directly correspond to the associated die pad numbers which increase clockwise around the die.
2. I/O macros requiring two U–cells may not be placed in shaded U–cell site locations. (See Section 4.3.4 for I/O macro placement restrictions.)
3. Quarter cell location identifier letters A, C, or D append row and column numbers (e.g. A05D) for notating placement orientation of quarter cell macros.
4. Die pad numbering maps directly to package pins.
5. The bold black line at the bottom of the M–cells indicates the columns which are connected to the same slave bias drivers (electrically adjacent).

TABLE 4–5 MCA750ETL Array/64 QFP Pad to Pin Cross–Reference

DIE	PACKAGE	DIE	PACKAGE	DIE	PACKAGE	DIE	PACKAGE
DIE PAD	Bond Finger & PKG PIN	DIE PAD	Bond Finger & PKG PIN	DIE PAD	Bond Finger & PKG PIN	DIE PAD	Bond Finger & PKG PIN
1	1	17	17	33	33	49	49
2	2	18	18	34	34	50	50
3	3	19	19	35	35	51	51
4	4	20	20	36	36	52	52
5	5	21	VCCO (21)	37	37	53	VCCO (53)
6	6	22	VEET (22)	38	38	54	VEET (54)
7	7	23	VCCT (23)	39	39	55	VCCT (55)
8	8	24	VEET (24)	40	40	56	VEET (56)
9	9	25	VEEE (25)	41	41	57	VEEE (57)
10	VCCO (10)	26	VCCE (26)	42	VCCO (42)	58	VCCE (58)
11	11	27	VEET (27)	43	43	59	VEET (59)
12	12	28	VCCT (28)	44	44	60	VCCT (60)
13	13	29	VEET (29)	45	45	61	VEET (61)
14	14	30	VCCO (30)	46	46	62	VCCO (62)
15	15	31	31	47	47	63	63
16	16	32	32	48	48	64	64

NOTES:

1. Die pad numbers start at top left side and increment clockwise.
2. Bond finger numbers start at TOP left side of cavity and increment clockwise.
3. I/O (U–Cell) site location numbers directly correspond to the die pad numbers. (e.g. Die pad 9 is connected to U–Cell B009.)
4. Die pads connected to U–cell **'pairs'** are **not separated** by a horizontal line. Die pads that **may not** be used for I/O macros requiring two U–cells are **shaded.**
5. Ground planes VCCO and VCCE are electrically connected together on the die and in the package.
6. Pin assignments for power and ground are as follows:
   VCCO: 10,21,30,42,53,62
   VCCT: 23,28,55,60
   VCCE: 26,58
   VEET: 22,24,27,29,54,56,59,61
   VEEE: 25,57
7. For the 64 QFP package, **FIX** File package pin names must be four characters in length, starting with the letter P. Therefore, package pin No.1 above becomes P001 in the **FIX** File. (See Section 6.3.4, "Fixed Placement of I/O Macros/Pins".)
8. Refer to Table 4–3 for TDIODE placement.

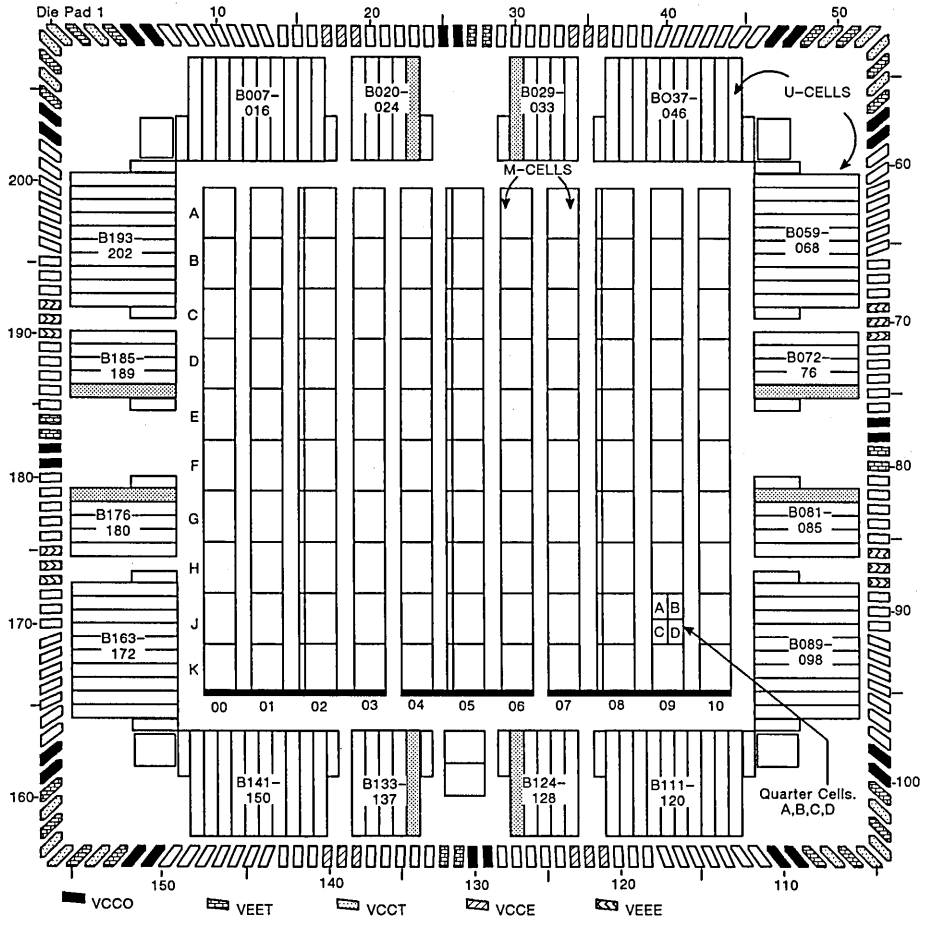


Figure 4–8 MCA3200ETL Floorplan – 160 QFP (Wirebond)

NOTES:
1. U-cell site location numbers directly correspond to the associated die pad numbers which increase clockwise around the die.
2. I/O macros requiring two U-cells may not be placed in shaded U-cell site locations. (See Section 4.3.4 for I/O macro placement restrictions.)
3. Quarter cell location identifier letters A, B, C, or D append row and column numbers (e.g. J09D) for notating placement orientation of quarter cell macros.
4. The bold black line at the bottom of the M-cells indicates the columns which are connected to the same slave bias drivers (electrically adjacent).

TABLE 4–6 MCA3200ETL Array/160 QFP Pad to Pin Cross–Reference

DIE	PACKAGE	DIE	PACKAGE	DIE	PACKAGE	DIE	PACKAGE
DIE PAD	Bond Finger & PKG PIN	DIE PAD	BOND FINGER & PDG PIN	DIE PAD	Bond Finger & PKG PIN	DIE PAD	Bond Finger & PKG PIN
1,3,206,208	VCCT (1,160)	54,56	VEET (42)	109,110	VCCO (83)	163	124
2,4	VEET (2)	57,58	VCCO (43)	111	84	164	125
5,6	VCCO (3)	59	44	112	85	165	126
7	4	60	45	113	86	166	127
8	5	61	46	114	87	167	128
9	6	62	47	115	88	168	129
10	7	63	48	116	89	169	130
11	8	64	49	117	90	170	131
12	9	65	50	118	91	171	132
13	10	66	51	119	92	172	133
14	11	67	52	120	93	173,174,175	VEEE (134)
15	12	68	53	121,122,123	VCCE (94)	176	135
16	13	69,70,71	VEEE (54)	124	95	177	136
17,18,19	VCCE (14)	72	55	125	96	178	137
20	15	73	56	126	97	179	138
21	16	74	57	127	98	180	139
22	17	75	58	128	99	181,182	VCCO (140)
23	18	76	59	129,130	VCC0 (100)	183,184	VEET (141)
24	19	77,78	VCCO (60)	131,132	VEET (101)	185	142
25,26	VCCO (20)	79,80	VEET (61)	133	102	186	143
27,28	VEET (21)	81	62	134	103	187	144
29	22	82	63	135	104	188	145
30	23	83	64	136	105	189	146
31	24	84	65	137	106	190,191,192	VEEE (147)
32	25	85	66	138,139,140	VCCE (107)	193	148
33	26	86,87,88	VEEE (67)	141	108	194	149
34,35,36	VCCE (27)	89	68	142	109	195	150
37	28	90	69	143	110	196	151
38	29	91	70	144	111	197	152
39	30	92	71	145	112	198	153
40	31	93	72	146	113	199	154
41	32	94	73	147	114	200	155
42	33	95	74	148	115	201	156
43	34	96	75	149	116	202	157
44	35	97	76	150	117	203,204	VCC0 (158)
45	36	98	77	151,152	VCCO (118)	205,207	VEET (159)
46	37	99,100	VCCO (78)	153,155	VEET (119)	D/A	VEEE
47,48	VCCO (38)	101,103	VEET (79)	154,156,157,159	VCCT (120, 121)		
49,51	VEET (39)	102,104,105,107	VCCT (80,81)	158,160	VEET (122)		
50,52,53,55	VCCT (40,41)	106,108	VEET (82)	161,162	VCCO (123)		

NOTES:

1. Die pad numbers start at top left side and increment clockwise.
2. Bond finger numbers start at TOP left side of cavity and increment clockwise.
3. I/O (U–Cell) site location numbers directly correspond to the die pad numbers. (e.g. Die pad 7 is connected to U–Cell B007.)
4. Die pads connected to U–cell **'pairs'** are **not separated** by a horizontal line. Die pads that **may not** be used for I/O macros requiring two U–cells are **shaded.**
5. Ground planes VCCO and VCCE are electrically connected together on the die and in the package.
6. Pin assignments for power and ground are as follows:
   VCCO: 3,20,38,43,60,78,83,100,118,123,140,158
   VCCT: 1,40,41,80,81,120,121,160
   VCCE: 14,27,94,107
   VEET: 2,21,39,42,61,79,82,101,119,122,141,159
   VEEE: 54,67,134,147
7. For the 160 QFP package, **FIX** File package pin names must be four characters in length, starting with the letter P. Therefore, package pin No. 1 above becomes P001 in the **FIX** File. (See Section 6.3.4, "Fixed Placement of I/O Macros/Pins".
8. 'D/A' indicates die attach.
9. Refer to Table 4–3 for TDIODE placement.

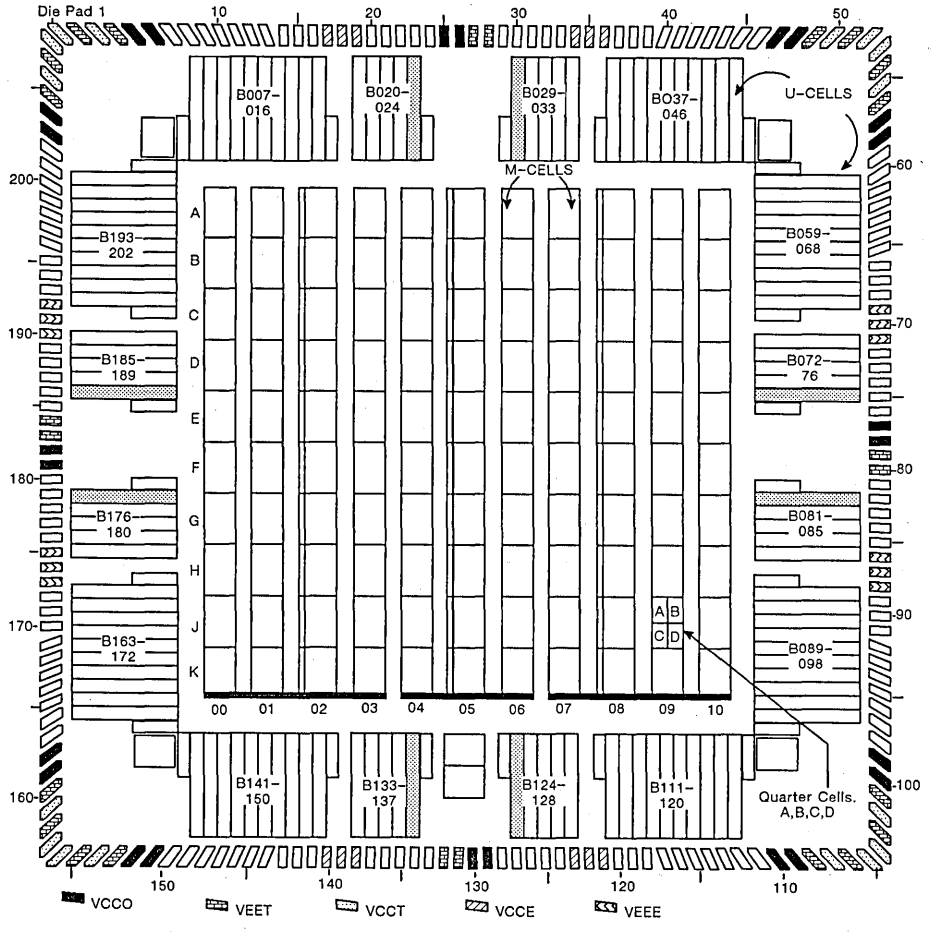


Figure 4–9 MCA3200ETL Floorplan – 169 PGA (Wirebond)

NOTES:
1. U-cell site location numbers directly correspond to the associated die pad numbers which increase clockwise around the die.
2. I/O macros requiring two U-cells may not be placed in shaded U-cell site locations. (See Section 4.3.4 for I/O macro placement restrictions.)
3. Quarter cell location identifier letters A, B, C, or D append row and column numbers (e.g. J09D) for notating placement orientation of quarter cell macros.
4. The bold black line at the bottom of the M-cells indicates the columns which are connected to the same slave bias drivers (electrically adjacent).

TABLE 4–7 MCA3200ETL Array/169 PGA Pad to Pin Cross–Reference

DIE	PACKAGE		DIE	PACKAGE		DIE	PACKAGE		DIE	PACKAGE	
DIE PAD	Bond Finger	PKG PIN	DIE PAD	Bond Finger	PKG PIN	DIE PAD	Bond Finger	PKG PIN	DIE PAD	Bond Finger	PKG PIN
1,3	1	VCCT	54,56	42	VEET	109,110	83	VCCO	163	124	A16
2,4	2	VEET	57,58	43	VCCO	111	84	T17	164	125	B16
5,6	3	VCCO	59	44	U2	112	85	T16	165	126	A15
7	4	B1	60	45	T2	113	86	R17	166	127	B15
8	5	B2	61	46	U3	114	87	R16	167	128	A14
9	6	C1	62	47	T3	115	88	P17	168	129	B14
10	7	C2	63	48	U4	116	89	P16	169	130	A13
11	8	D1	64	49	T4	117	90	N17	170	131	B13
12	9	D2	65	50	U5	118	91	N16	171	132	A12
13	10	E1	66	51	T5	119	92	M17	172	133	B12
14	11	E2	67	52	U6	120	93	M16	173,174,175	134	VEEE
15	12	F1	68	53	T6	121,122,123	94	VCCE	176	135	B11
16	13	F2	69,70,71	54	VEEE	124	95	L16	177	136	A11
17,18,19	14	VCCE	72	55	T7	125	96	L17	178	137	B10
20	15	G2	73	56	U7	126	97	K16	179	138	A10
21	16	G1	74	57	T8	127	98	K17	180	139	B9
22	17	H2	75	58	U8	128	99	J16	181,182	140	VCCO
23	18	H1	76	59	T9	129,130	100	VCCO	183,184	141	VEET
24	19	J2	77,78	60	VCCO	131,132	101	VEET	185	142	A9
25,26	20	VCCO	79,80	61	VEET	133	102	J17	186	143	A8
27,28	21	VEET	81	62	U9	134	103	H17	187	144	B8
29	22	J1	82	63	U10	135	104	H16	188	145	A7
30	23	K1	83	64	T10	136	105	G17	189	146	B7
31	24	K2	84	65	U11	137	106	G16	190,191,192	147	VEEE
32	25	L1	85	66	T11	138,139,140	107	VCCE	193	148	B6
33	26	L2	86,87,88	67	VEEE	141	108	F16	194	149	A6
34,35,36	27	VCCE	89	68	T12	142	109	F17	195	150	B5
37	28	M2	90	69	U12	143	110	E16	196	151	A5
38	29	M1	91	70	T13	144	111	E17	197	152	B4
39	30	N2	92	71	U13	145	112	D16	198	153	A4
40	31	N1	93	72	T14	146	113	D17	199	154	B3
41	32	P2	94	73	U14	147	114	C16	200	155	A3
42	33	P1	95	74	T15	148	115	C17	201	156	A1
43	34	R2	96	75	U15	149	116	A17	202	157	A2
44	35	R1	97	76	U17	150	117	B17	203,204	158	VCCO
45	36	U1	98	77	U16	151,152	118	VCCO	205,207	159	VEET
46	37	T1	99,100	78	VCCO	153,155	119	VEET	206,208	160	VCCT
47,48	38	VCCO	101,103	79	VEET	154,156	120	VCCT		S/R	VCCE
49,51	39	VEET	102,104	80	VCCT	157,159	121	VCCT		D/A	VEEE
50,52	40	VCCT	105,107	81	VCCT	158,160	122	VEET			
53,55	41	VCCT	106,108	82	VEET	161,162	123	VCCO			

NOTES:
1. Die pad numbers start at top left side and increment clockwise.
2. Bond finger numbers start at TOP left side of cavity and increment clockwise.
3. I/O (U–Cell) site location numbers directly correspond to the die pad numbers. (e.g. Die pad 7 is connected to U–Cell B007.)
4. Die pads connected to U–cell **'pairs'** are **not separated** by a horizontal line. Die pads that **may not** be used for I/O macros requiring two U–cells are **shaded.**
5. Ground planes VCCO and VCCE are electrically connected together on the die.
6. Pin assignments for power and ground are as follows:
   VCCO: C6,C10,C12,F3,F15,H3,K15,M3,M15,R6,R8,R12
   VCCT: C5,C13,E3,E15,N3,N15,R5,R13
   VCCE: G3,G15,L3,L15
   VEET: C3,C4,C8,C9,C14,C15,D3,D4,D15,H15,J3,J15,K3,P3,P15,R3,R4,R9,R10,R14,R15
   VEEE: C7,C11,R7,R11
7. 'S/R' indicates seal ring.
8. 'D/A' indicates die attach.
9. Refer to Table 4–3 for TDIODE placement.

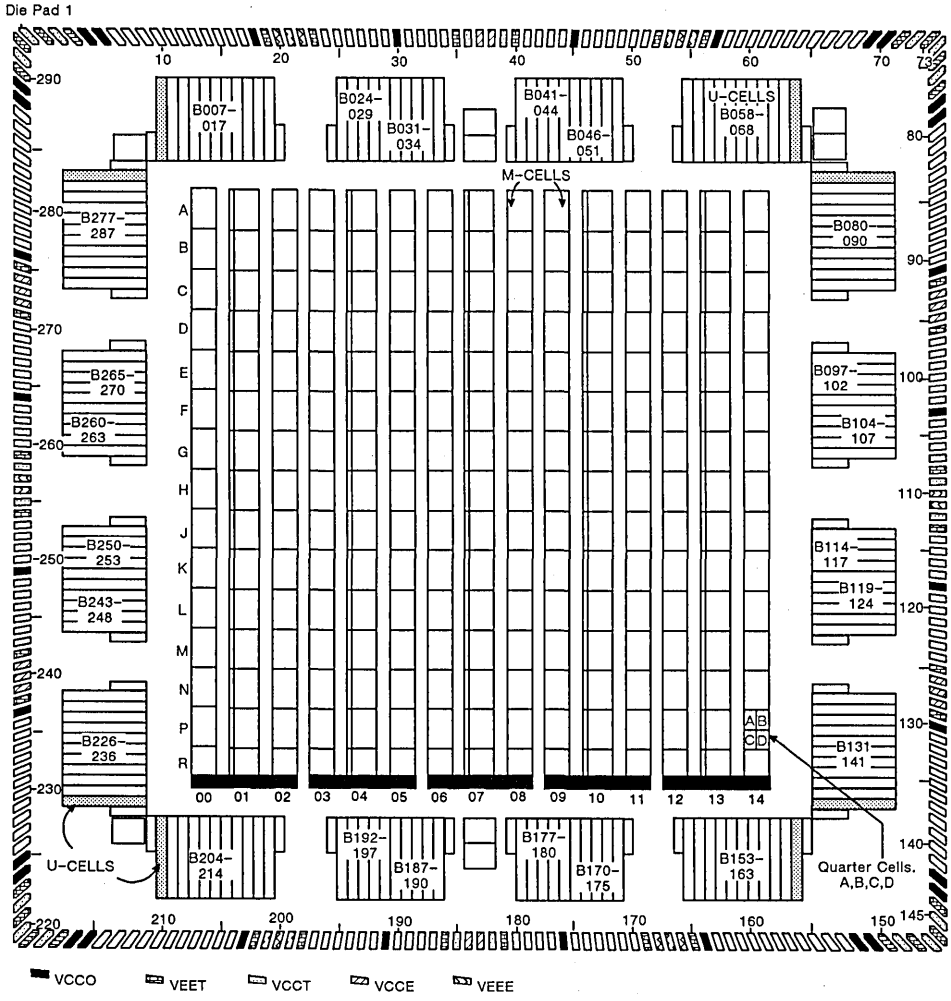


Figure 4–10 MCA6200ETL Floorplan – 224 PGA (Wirebond)

NOTES:
1. U-cell site location numbers directly correspond to the associated die pad numbers which increase clockwise around the die.
2. I/O macros requiring two U-cells may not be placed in shaded U-cell site locations. (See Section 4.3.4 for I/O macro placement restrictions.)
3. Quarter cell location identifier letters A, B, C, or D append row and column numbers (e.g. P14D) for notating placement orientation of quarter cell macros.
4. The bold black line at the bottom of the M-cells indicates the columns which are connected to the same slave bias drivers (electrically adjacent).

TABLE 4–8 MCA6200ETL Array/224 PGA Pad to Pin Cross–Reference

DIE PAD	PACKAGE Bond Finger	PACKAGE PKG PIN	DIE PAD	PACKAGE Bond Finger	PACKAGE PKG PIN	DIE PAD	PACKAGE Bond Finger	PACKAGE PKG PIN	DIE PAD	PACKAGE Bond Finger	PACKAGE PKG PIN
291,1,3	1	VCCT	72,74,76	60	VCCT	151,152	119	VCCO	226	178	D15
290,292,2,4	2	VEET	78,79	61	VCCO	153	120	R15	227	179	C15
5,6	3	VCCO	80	62	R4	154	121	R16	228	180	B17
7	4	D4	81	63	T4	155	122	U17	229	181	C14
8	5	D3	82	64	U2	156	123	P16	230	182	D14
9	6	B2	83	65	T5	157	124	P15	231	183	B14
10	7	E3	84	66	R5	158	125	P17	232	184	B16
11	8	E4	85	67	U5	159	126	T17	233	185	C13
12	9	E2	86	68	U3	160	127	N16	234	186	B15
13	10	C2	87	69	T6	161	128	R17	235	187	B13
14	11	F3	88	70	U4	162	129	N17	236	188	D13
15	12	D2	89	71	U6	163	130	N15	237	189	VCCO
16	13	F2	90	72	R6	164	131	VCCO	238,242	190	VEET
17	14	F4	91	73	VCCO	165,169	132	VEET	239,240,241	191	VCCE
18	15	VCCO	92,96	74	VEET	166,167,168	133	VEEE	243	192	C12
19,23	16	VEET	93,94,95	75	VCCE	170	134	M16	244	193	A13
20,21,22	17	VEEE	97	76	T7	171	135	N18	245	194	B12
24	18	G3	98	77	V6	172	136	M17	246	195	A12
25	19	F1	99	78	U7	173	137	M18	247	196	C11
26	20	G2	100	79	V7	174	138	L16	248	197	D11
27	21	G1	101	80	T8	175	139	L15	249	198	VCCO
28	22	H3	102	81	R8	176	140	VCCO	250	199	A11
29	23	H4	103	82	VCCO	177	141	L18	251	200	B11
30	24	VCCO	104	83	V8	178	142	L17	252	201	C10
31	25	H1	105	84	U8	179	143	K16	253	202	B10
32	26	H2	106	85	T9	180	144	K17	254,259	203	VEET
33	27	J3	107	86	U9	181,186	145	VEET	255	204	VCCT
34	28	J2	108,113	87	VEET	182	146	VCCT	256,257	205	VEEE
35,40	29	VEET	109	88	VCCT	183,184	147	VCCE	258	206	VCCT
36	30	VCCT	110,111	89	VEEE	185	148	VCCT	260	207	B9
37,38	31	VCCE	112	90	VCCT	187	149	J17	261	208	D9
39	32	VCCT	114	91	U10	188	150	J15	262	209	B8
41	33	K2	115	92	R10	189	151	H17	263	210	C9
42	34	K4	116	93	U11	190	152	J16	264	211	VCCO
43	35	L2	117	94	T10	191	153	VCCO	265	212	A8
44	36	K3	118	95	VCCO	192	154	H18	266	213	C8
45	37	VCCO	119	96	V11	193	155	H16	267	214	D8
46	38	L1	120	97	T11	194	156	H15	268	215	B7
47	39	L3	121	98	R11	195	157	G17	269	216	A7
48	40	L4	122	99	U12	196	158	G18	270	217	C7
49	41	M2	123	100	V12	197	159	G16	271,275	218	VEET
50	42	M1	124	101	T12	198,202	160	VEET	272,273,274	219	VCCE
51	43	M3	125,129	102	VEET	199,200,201	161	VEEE	276	220	VCCO
52,56	44	VEET	126,127,128	103	VCCE	203	162	VCCO	277	221	A6
53,54,55	45	VEEE	130	104	VCCO	204	163	F18	278	222	B6
57	46	VCCO	131	105	V13	205	164	F17	279	223	D6
58	47	N1	132	106	U13	206	165	F15	280	224	C6
59	48	N2	133	107	R13	207	166	F16	281	225	B4
60	49	N4	134	108	T13	208	167	D17	282	226	B5
61	50	N3	135	109	U15	209	168	E17	283	227	B3
62	51	R2	136	110	U14	210	169	C17	284	228	C5
63	52	P2	137	111	U16	211	170	E16	285	229	D5
64	53	T2	138	112	T14	212	171	E15	286	230	C4
65	54	P3	139	113	R14	213	172	D16	287	231	C3
66	55	P4	140	114	T15	214	173	C16	288,289	232	VCCO
67	56	R3	141	115	T16	215,216	174	VCCO		S/R	VCCE
68	57	T3	142,143	116	VCCO	217,219,221,223	175	VEET		D/A	VEEE
69,70	58	VCCO	144,146,148,150	117	VEET	218,220,222	176	VCCT			
71,73,75,77	59	VEET	145,147,149	118	VCCT	224,225	177	VCCO			

NOTES:

1. Die pad numbers start at top left side and increment clockwise.
2. Bond finger numbers start at TOP left side of cavity and increment clockwise.
3. I/O (U-Cell) site location numbers directly correspond to the die pad numbers. (e.g. Die Pad 9 is connected to U-Cell B009.)
4. Die pads connected to U-cell **'pairs'** are **not separated** by a horizontal line. Die pads that **may not** be used for I/O macros requiring two U-cells are **shaded.**
5. Ground planes VCCO and VCCE are electrically connected together on the die.
6. Pin assignments for power and ground are as follows:
   VCCO : A4,A5,A14,A15,D1,D18,E1,E18,P1,P18,R1,R18,V4,V5,V14,V15
   VCCE: D10,G4,G15,M4,M15,R9,S/R
   VEET: A2,A3,A9,A10,A16,A17,B1,B18,U1,U18,J1,J18,K1,K18,V2,V3,V9,V10,V16,V17
   VEEE: D7,D12,J4,K15,R7,R12,D/A
   VCCT: A1,A18,C1,C18,T1,T18,V1,V18
7. 'S/R' indicates seal ring.
8. 'D/A' indicates die attach.
9. Refer to Table 4-3 for TDIODE placement.

4.4 Calculation of Minimum and Maximum Power Dissipation

The worst-case power dissipation of the die due to process and temperature variations at a given V_{EEE} for a given design can be calculated using the following procedure.

P_{MAX} =

$1.25(P_{MACRO}+P_{INT\_OEF}+P_{STECL}+P_{BIAS})+P_{EXT\_OEF}$

The minimum power dissipation is given by:

P_{MIN} =

$0.75(P_{MACRO}+P_{INT\_OEF}+P_{STECL}+P_{BIAS})+P_{EXT\_OEF}$

where:

P_{MACRO} = P_{INT_MACRO} (sum of internal M-cell macro powers) + P_{I/O_MACRO} (sum of I/O U-cell macro powers). Typical macro power values are listed in the library (Section 9.6 not including the OEF power). Macro power is listed for V_{EEE} = -5.2 Vdc and V_{CCT} = 5.0 Vdc. If V_{EEE} = -4.5 Vdc, the typical macro power for ECL macrocells is calculated by multiplying by the factor 0.865. When operating in PECL mode, where V_{CC} = 5.0 Vdc, the typical power for internal and output ECL/PECL macrocells is calculated by multiplying by the factor 0.962. The power is given for both high and low power macros. For TTL macros, the sum of the components of both V_{CCT} and V_{EEE} are used for calculating macro power.

P_{INT_OEF} = sum of internal emitter follower current multiplied by $|V_{EEE}|$.

P_{STECL} = power dissipation due to the output current source (STECL) currents. The power for each STECL output is:

$I_{CS}|V_{EEE}|$ where I_{CS} is 6 or 10 mA.

P_{BIAS} = ($I_{EEEB}V_{EEE}$)

where bias currents I_{EEEB} for each array are:

- 6200ETL - I_{EEEB} = 327 mA (nominal I_{EEE} bias)
- 3200ETL - I_{EEEB} = 157 mA (nominal I_{EEE} bias)
- 750ETL - I_{EEEB} = 57 mA (nominal I_{EEE} bias)

P_{EXT_OEF} = the power dissipated on-chip in the output emitter followers at the output pads. The powers shown below are for 50, 60 and 68 ohm outputs, and 25 and 50 ohm cutoff outputs. They are calculated by taking the average of the power in the high state (VOH=-0.95 Vdc) and the low state (VOH=-1.75 Vdc for 50 and 68 ohm non-cutoff outputs). Either a 50, 68, or 25 ohm resistor to -2 Vdc is assumed as the load. Note that the power in the low state is equal to zero for the cutoff outputs. No external OEF power is used for TTL outputs.

Average Power for Outputs with External Loading

68 Ohm = 10.9 mW (68 ohm termination)
68 Ohm = 12.0 mW (60 ohm termination)
50 Ohm = 15.0 mW
25 Ohm Cutoff = 20.0 mW
50 Ohm Cutoff = 10.0 mW

Power Calculation Example:

The following is an example of the power calculation for an MCA3 ETL array assuming V_{EEE} = -5.2 Vdc. The example will use a typical design for a fully utilized MCA3 6200ETL array.

The internal macro power is first calculated by adding up the power values listed in the power table for each macrocell used. Note that the power values listed in the Macrocell Library represent the typical switch current power, but do not include the output emitter follower power. (See the Macrocell Library.) Assuming that 225 M-cells are used, the power could range from 5.6 mW (4 L202s/M-cell) to 21.6 mW (2 H291/M-cell) for one M-cell. Therefore, P_{INT_MACRO} could range from 225 x 5.6 = 1.26 W to 225 x 21.6 = 4.86 W.

Assuming an average mix of M-cell macros:

P_{INT_MACRO} = 3.06 W (225 M-cells)

Power for I/O U-cells is calculated in a similar manner. For this example, we will assume 80 inputs and 72 outputs. Power calculations are as follows:

{28-TTL inputs}x(8.3mW) = 0.23 W
{52-ECL inputs}x(2.8mW) = 0.15 W
(16-24mA TTL outputs)x(34.0mW) = 0.54 W
{12-12mA TTL outputs}x(18.4mW) = 0.22 W
{36-50 ohm ECL outputs}x(17.7mW) = 0.64 W
{8-6mA STECL outputs}x(17.7mW) = 0.14 W

P_{I/O_MACRO} = 1.92 W (152 I/O U-cells)
P_{MACRO} = 3.06 + 1.92 = 4.98 W

Next, the internal output emitter follower currents (either 0.48 or 0.96 mA for Major Cell outputs) should be summed and multiplied by the magnitude of V_{EEE}. Once again, a large variation in power will occur for different designs. For example, assuming a maximum number of outputs possible, the internal OEF current could reach 1.7 A [4 gates/M-cell x 2 outputs x 0.96mA each (twinned outputs) x 225 M-cells]. A realistic minimum of 0.216 A is obtained from 2 outputs for each M-cell x 0.48 mA for each output. An average ECL design

would yield about 4 used outputs per M-cell, 2 twinned (0.96mA) and 2 single (0.48mA), thus:

$I_{OEF\_INT\_SUM}$ = 648 mA $|V_{EEE}|$ = 5.2 V
therefore:
P_{INT_OEF} = (648 mA)(5.2 V) = 3.37 W

The total external power can be calculated by adding up the number of each type of outputs used (ECL/PECL, TTL, and STECL) and then multiplying by the average power per output for that type as shown above. From the I/O macros assumed on the P_{EXT_MACRO} calculations the design uses 8 - 6mA STECL outputs, 36 - 50 ohm outputs, and 28 TTL outputs.

P_{STECL} =
(8-STECLs)(6 mA)(5.2 Vdc) = 0.25 W

$P_{EXT\_OEF\_ECL}$ =
(36-50 ohm outputs)(15 mW) = 0.54 W

Dissipation in I/O U-Cells due to sink current:
P_{TTL_SINK} =
($V_{OL/OH}$ max typ)(Sink Current[12 or 24 mA]) x (number of outputs).

Dissipation of the output transistor driven by a TTL I/O U-Cell macro is 6mW or 12mW for 12mA or 24mA macros respectively, when in the low state. When in the high state, the power dissipation will be 10.2mW.

P_{TTL_SINK} =
(12 - 12 mA TTL)(10.2 mW) + (16 - 24 mA TTL) x (12 mW) = 0.31 W

P_{EXT_OEF} = $P_{EXT\_OEF\_ECL}$ + P_{TTL_SINK} = 0.85 W

The bias power I_{EEEB} for a 6200ETL array is calculated as follows:

P_{BIAS} = (327 mA)(5.2 V) = 1.70 W

The total worst-case power for this design, therefore, is:

1.25(4.98+3.37+0.25+1.70) + 0.85 = 13.7 W

$P_{MAX\_WORST\_CASE}$ = 13.7 W

For absolute worst-case, the worst-case supply voltage values should be used. The worst-case I_{EEEB} current for a given design is calculated automatically via the CAD system using the IEE program. Refer to the on-line help system or Motorola CAD documentation for details.

Note: I_{EEEB} and I_{CCT} values are calculated by the IEE program on the Motorola CAD system for worst-case (i.e. they already are multiplied by the 1.25 factor for processing and temperature variations). Also note that the current passing through the emitter followers at the output pads and the P_{TTL_SINK} current are not counted in the IEE program since these currents do not sink to V_{EEE} on the chip.

4.5 Differential Receivers

Several macros in the MCA3 ETL library can be driven differentially. The use of differential drive is strongly recommended for high-frequency applications.

Differential receivers must be driven by a single macro (macro L/H202, for example) having a true and a complement output. If an unused differential input pair is connected to package pins, at least one input of the pair must be forced to V_{OH} or V_{OL} during test to avoid current source regulation problems. These problems arise when both devices in the ECL switch are off and the current source attempts to draw its desired current from the V_{CS} bias circuitry.

The metal and fanout delay for a differential net is calculated to the crossing point of the differential signal pair by the Motorola CAD system. A differential net is a pair of signals that are driven differentially by a single macro and connected only to differential receivers. If a single-ended input is connected to a net, the net cannot be treated as a differential net since the Motorola simulator cannot attach a single-ended and a differential delay to the same net at the same time. For this reason, the designer should avoid driving a single-ended input off a potential differential net.

4.6 Noise Margin Considerations

The DC Electrical Specifications (see Section 10.2) for MCA3 are specified using junction instead of ambient temperature. Precise measurement correlation (including DC and AC specifications) between the customer and the vendor dictated the use of junction temperature. Two versions of a thermal diode (see Section 3.5) can be selected on an MCA3 array which can be used to accurately measure the junction temperature under operating conditions. It is highly recommended that the designer use a thermal diode on each MCA3 option. The junction temperature is the primary parameter that affects the DC levels as well as the AC delays. Simply specifying the ambient temperature presents correlation problems since assumptions must be made about the variation in the package thermal impedance, the direction and velocity of the air flow, and the ambient temperature change as the air circulates through the system. The power dissipation for an MCA3 ETL array will vary depending on the design, utilization, output types and whether low or high power macros are used. Also, the die size, package type, and cooling method affect the junction temperature.

For an array using the 100K option, the worst-case noise margin for the standard 50 ohm output is 140mV in the high state (NMhigh = VOHmin- VIHmin) and 145mV in the low state (NMlow = VILmax – VOLmax) over all combinations of temperature and voltage. This is an improvement over standard logic 100K which over temperature specifies 120mV for both the high and low state for V_{EEE} = 4.2V and V_{EEE} = -4.8V, and 130mV and 135mV respectively for V_{EEE} = -4.5V (noise margin is reduced to 100mV for all combinations of temperature and voltage). The improvement is due to the better regulation of the bias regulator and the fact that input signals must connect to an input cell.

5. AC Performance Guidelines

The guidelines presented in this section allow the designer to predict the internal AC performance of the array. These guidelines are not, however, specification limits. All times are worst-case over process, voltage, and temperature unless otherwise indicated.

5.1 Input/Output Delay Calculations

This section outlines the delay characteristics associated with the package type and the various I/O configurations.

5.1.1 I/O Capacitance

The total I/O capacitance (C_{IP}) is composed of capacitances contributed by the package pin and signal lead, bond metal, metal routing from the pad to the input cells, and the input cells themselves. For the ETL array packages, the I/O capacitance is calculated as follows:

$$C_{IP} = C_{PKG} + C_{PAD\_CELL} + \Sigma N_i C_i$$

where:

$\Sigma N_i C_i$ is the sum of the input capacitances on the net. Refer to Table 5-7.
C_{PKG} = 11 pF for the 224 PGA
C_{PKG} = 11 pF for the 169 PGA
C_{PKG} = 6 pF for the 160 QFP
C_{PKG} = 4 pF for the 64 QFP
C_{PAD_CELL} = 2 pF for the 224 and 169 PGA,
= 1 pF for the 160 and 64 QFP.
(Includes pad and routing to U-cell I/O macro.)

5.1.2 External Degradation Due to Input Capacitance

ECL Inputs

When an external signal drives an input macro on the chip with transmission lines using parallel termination, the signal will be degraded due to the input pin capacitance. The equations for the maximum propagation delay and rise/fall time degradation at the input pin are:

$\Delta t_{r/f} = 0.35\ Z_O C_{IP}$ for $C_{IP} \leq 10$ pF
$\Delta t_{r/f} = 0.6\ Z_O C_{IP}$ for $10 \leq C_{IP} < 50$ pF

If picofarads are used for the capacitance, then the result will be in picoseconds.

TTL Inputs

An external TTL signal driving an input translator macro on the chip can be considered as a series terminated line. Therefore, the signal will be degraded due to the input capacitance by the following equation:

$\Delta t_{r/f} = 0.7\ Z_O C_{IP}$ (for transmission line external to the package)

NOTE: The Motorola CAD system assumes an external transmission line delay of 0 ps for AC delay calculations.

5.1.3 Propagation Delay Degradation of the Input Due to Rise/Fall Time and Voltage Skew at the I/O Pin

ECL Inputs

When external ECL signals drive an input pin to the array, the rise and fall times should be 0.5 ns (20 to 80%) in order to meet the propagation delay specified in the Macrocell Library. Although the driving source may provide a signal with 0.5 ns rise and fall times, the capacitance at the end of the transmission line (see Section 5.1.2) will degrade the signal. For each 1.0 ns increase above 0.5 ns in the rise and fall time at the input pin of the array, 50 ps should be added to the input macro propagation delay time. This assumes that the 50% point of the input signal is not skewed by more than ± 20 mV from nominal V_{BB}. V_{BB} remains essentially unchanged through the temperature range for these 100K compatible arrays. The propagation delay degradation (in ps) due to the rise or fall time of the input signal being larger than 0.5 ns is:

$$\Delta t_{pd[RISE/FALL]}\ \text{ps} = 50\ \text{ps/ns}\ (t_{r/f[TOTAL]} - 0.5)\ \text{ns}$$

where:
$t_{r/f[TOTAL]} = t_{r/f[TESTER]} + \Delta t_{r/f}$
$t_{r/f[TESTER]}$ = 1.0 ns (rise/fall time for ECL signals on the Trillium tester)

If the 50% point of the input signal is skewed by more than ± 20 mV from the switching point (V_{BB}) of the output macro, inaccurate propagation delay measurements can result when the measuring equipment uses the 50% point of the input and output signals as the reference point. When the input signal is skewed negative, the propagation delay will appear larger on the rising edge and shorter on the falling edge. The measurement error delay change (in picoseconds) due to the input signal being skewed can be calculated using the following equation:

$$\Delta t_{pd[VOLTAGE\ SKEW]}\ \text{ps} = \pm 2.1 (V_{SKEW})(t_{r/f[TOTAL]})$$

where $t_{r/f[TOTAL]}$ is the 20 to 80% rise/fall time of the input at the I/O pin in nanoseconds and V_{SKEW} is the amount of voltage difference in millivolts between the 50% point of the input signal and the actual V_{BB} voltage.

5

TTL Inputs

When external TTL signals drive an input pin to the array, the rise and fall times should be 2.0 ns (10 to 90%) in order to meet the propagation delay specified in the Macrocell Library. Although the driving source may provide a signal with 2.0 ns rise and fall times, the capacitance at the end of the transmission line (see Section 5.1.2) will degrade the signal. For each 1 ns increase above 2.0 ns in the rise and fall time at the input pin of the array, 70 ps should be added to, or subtracted from, the input macro propagation delay time. This assumes that the input signal is skewed due to temperature less than 80mV from the 1.5V switching point threshold. If the switching point threshold of the input signal is skewed by more than ± 80 mV from the switching point (1.5V) of the output macro, inaccurate propagation delay measurements can result when the measuring equipment uses the threshold point of the input and output signals as the reference point. For ambient temperatures other than 25°C, the threshold will vary over temperature typically by 0.72mV/°C. The measurement error delay change (in nanoseconds) due to the rise or fall time of the input signal being larger than 2.0 ns, combined with the result of the ambient temperature being higher than 25°C, is:

$$\Delta t_{pd[RISE]}\ ns = [(0.07)(t_{r[TOTAL]} - 2.0)]\ ns - [(0.00072)(t_{r[TOTAL]} - 3)(T - 25°C)]\ ns$$

$$\Delta t_{pd[FALL]}\ ns = [(0.07)(t_{f[TOTAL]} - 2.0)]\ ns + [(0.00072)(t_{f[TOTAL]} - 3)(T - 25°C)]\ ns$$

for $t_{r[TOTAL]}, t_{f[TOTAL]} > 2.0$ ns

where:

$$t_{r[TOTAL]} = t_{r[TESTER]} + \Delta t_{r/f}$$
$$t_{f[TOTAL]} = t_{f[TESTER]} + \Delta t_{r/f}$$

and

$t_{r/f[TESTER]}$ = 2.0 ns (rise/fall time for TTL signals on the Trillium tester).

Note: The Motorola CAD system assumes the above rise/fall time tester skew degradation in AC delay calculations. However, the voltage skew delay ($\Delta t_{pd[VOLTAGE\ SKEW]}$) is not accounted for in the CAD system.

5.1.4 Delay From an Input Pad to a Macrocell

When an input signal is brought on chip through an input buffer bypass macro (LC15), metal runs from the I/O pad to the input and/or internal macros can cause degradation of the propagation delay due to the capacitance and resistance of the metal, and the capacitance due to fanin. The following equation should be used for calculating the degradation due to metal routing from the input pad to the macros and the capacitive loading of the macro inputs:

Input Pad Metal/Fanout Delay (ps) Worst Case

$$T_{pd\_INPUT\_MFO} = 1.25(C_{TOT})(R_{TOT})$$

where:
$C_{TOT} = \Sigma N_i C_i + L_{M1}C_{M1} + L_{M2}C_{M2}$
$R_{TOT} = Z_0 + 0.7L_{M1}R_{M1} + 0.7L_{M2}R_{M2}$
$\Sigma N_i C_i$ is the sum of the input capacitances on the net.
L_{M1} = Length of metal1 (mils)
L_{M2} = Length of metal2 (mils) + 40 mils
C_{M1} = 0.00385 pF/mil
C_{M2} = 0.00415 pF/mil
R_{M1} = 0.46 Ω/mil
R_{M2} = 0.19 Ω/mil
Z_0 = 50 Ω (characteristic impedance of transmission line on the Trillium tester board)

Note: The L_{M2} term accounts for the 40 mils of interconnect from the pad through the I/O U-cell.

5.1.5 Delay Due to the Package and Bonding

The I/O pin delay depends largely on the package selection as well as the position of the package pin. Worst-case minimum and maximum package pin delays for the 224 PGA, 169 PGA, 160QFP, and 64QFP packages are listed below:

$T_{pd\_PKG\_PIN\_224}$ = 350 ps max (224 PGA)
$T_{pd\_PKG\_PIN\_224}$ = 150 ps min (224 PGA)
$T_{pd\_PKG\_PIN\_169}$ = 350 ps max (169 PGA)
$T_{pd\_PKG\_PIN\_169}$ = 200 ps min (169 PGA)
$T_{pd\_PKG\_PIN\_160}$ = 200 ps max (160 QFP)
$T_{pd\_PKG\_PIN\_160}$ = 175 ps min (160 QFP)
$T_{pd\_PKG\_PIN\_64}$ = 175 ps max (64 QFP)*
$T_{pd\_PKG\_PIN\_64}$ = 150 ps min (64 QFP)

The designer can select pins which best match the delay constraints for any given signal.

*Note: The WACC CAD system inserts the maximum package pin delay for each type of package. However, the minimum value which the CAD system can assign is 200 ps.

5.1.6 Simultaneous Switching Limit

Simultaneous switching is defined as switching two or more outputs in the same direction within a 2.0 ns window. When TTL and single-ended ECL outputs are switched simultaneously, a noise spike is introduced on unswitched outputs by the instantaneous change in current on the V_{EET} or V_{CCE} bus respectively. This spike could exceed system noise margins, thus producing system reliabil-

ity problems or spurious switching. The total number of simultaneously switched single-ended outputs, therefore, must be limited as dictated by the following relation:

$$\Sigma N_o \Delta I_o / t_{r/f} \leq V_{NOISE} / L_{EFF}$$

where:

N_o = number of a given type of output (50 ohm, 68 ohm, 50 ohm cutoff, 25 ohm cutoff, 12mA or 24mA current sink) simultaneously switched
ΔI_o = the delta current induced by switching the given type of output (see table 5-2)
$t_{r/f}$ = the rise/fall time for the given output
L_{EFF} = (See Table 5-1)
V_{NOISE} = 0.2 Volts for ECL and mixed ECL/TTL

TABLE 5-1 Effective Inductance Values

PACKAGE TYPE	L_{EFF} (nH) OUTPUT TYPE	
	ECL	TTL
224 PGA	0.112	0.10
160 QFP & 169 PGA	0.151	0.11
64 QFP	0.200	0.17

If the design in the 224 PGA calls for twenty 50 ohm outputs and sixteen 25 ohm cutoff drivers to be switched simultaneously with no slowdown capacitors (and none of these outputs are differential pairs), then the relation would become:

$$(20)(18\text{ mA})/(0.6\text{ ns}) + (16)(44\text{ mA})/(0.6\text{ ns}) \leq (0.2\text{ Volts})/(0.112\text{ nH})$$

$$1.77\text{ A/ns} \leq 1.79\text{ V/nH} \quad \text{(pass)}$$

Table 5-3 shows the number of a given type of output which can be switched simultaneously if **only** that type of output is used.

TABLE 5-2 Simultaneous Switching Constants

ECL OUTPUT TYPE	ΔI_o		$t_{r/f}$ with no slowdown	$t_{r/f}$ with slowdown
50 ohm (H)	18 mA		0.6 ns	1.0 ns
68 ohm (L)	15 mA		0.7 ns	1.2 ns
50 ohm cutoff	22 mA		0.75 ns	1.2 ns
25 ohm cutoff	44 mA		0.6 ns	1.0 ns
TTL OUTPUT TYPE	ΔI_o (with load)		$t_{r/f}$ (50pF)	$t_{r/f}$ (100pF)
	50 pF	100 pF		
12 mA	40 mA	60 mA	2.0 ns	2.0 ns
24 mA	60 mA	80 mA	1.5 ns	1.5 ns

Note: ΔI_o is the maximum change in current for switching that output type. Rise/fall times are typical values, except for TTL which are minimum.

Even though STECL outputs have a constant current source, they will contribute to simultaneous switching noise in systems when loaded with board interconnect. If the slowdown option is used for STECL outputs, there is no simultaneous switching limit. If the slowdown option is not used on a STECL output, then the limit is the same as the 50 or 68 ohm output type with the slowdown option (see Table 5-3).

TABLE 5-3 Simultaneous Switching Limits Using Only One Output Type

ECL OUTPUT TYPE	WITH NO SLOWDOWN			WITH SLOWDOWN		
	--	160 QFP	64 QFP	--	160 QFP	64 QFP
	224 PGA	169 PGA	--	224 PGA	169 PGA	--
50 ohm (H macro)	60	44	33	99	74	42
68 ohm (L macro)	84	62	42	120	106	42
50 ohm cutoff	61	45	34	97	72	42
25 ohm cutoff	24	18	14	40	30	23
TTL OUTPUT TYPE	@ 50 pF load			@ 100 pF load		
12 mA	100	91	42	67	61	39
24 mA	50	45	29	38	34	22

Note: Please consult ASIC Bipolar Applications for latest information.

Differential outputs (outputs driven by the true and complement output of a single U-cell) also do not contribute appreciably to simultaneous switching noise and do not figure into the maximum switching total.

These simultaneous switching limits represent guidelines recommended by Motorola for using the array in a system. The particular noise margin requirements and the effects of simultaneously switched outputs will vary with each design. The designer, for instance, may not care if noise is coupled to data signals during a non-critical part of the clock cycle. Motorola, therefore, recommends that the designer analyze the electrical environment in which the part will be operating (e.g. loading conditions, bypassing, noise margin requirements, etc.) when designing a part which will switch large numbers of outputs.

5.1.7 Simultaneous Switching Delay

When non-differential outputs are switched simultaneously a delay penalty is incurred for those outputs switched. This penalty is due to the fact that the inductance of the ground pins of the package and socket limit the response time of the bypass capacitor(s) in supplying the increased switching current.

Simultaneously switched outputs refer to any group of outputs switched in a 2 ns window. The Motorola CAD system does not in-

clude simultaneous switching effects in delay calculations.

In order to calculate the delay experienced by any output which is switched simultaneously within a group, one must sum the contributions of each output switched in the group according to Table 5-4.

TABLE 5-4 Simultaneous Switching Delay Contribution for Various Output Types

ECL OUTPUT TYPE	WITH NO SLOWDOWN			WITH SLOWDOWN		
	--	160 QFP	64 QFP	--	160 QFP	64 QFP
	224 PGA	169 PGA	--	224 PGA	169 PGA	--
50 ohm (H)	17 ps	23 ps	24 ps	10 ps	14 ps	14 ps
68 ohm (L)	13 ps	16 ps	17 ps	7 ps	9 ps	10 ps
50 ohm cutoff	16 ps	22 ps	24 ps	10 ps	14 ps	15 ps
25 ohm cutoff	41 ps	55 ps	57 ps	25 ps	33 ps	34 ps
TTL OUTPUT TYPE	@ 50 pF load			@ 100 pF load		
12 mA	15 ps	16 ps	20 ps	22 ps	25 ps	31 ps
24 mA	30 ps	33 ps	41 ps	39 ps	44 ps	55 ps

Note: Please consult ASIC Bipolar Applications for latest information.

Differentially driven output pin pairs cause less of an effect on the V_{CCE} bus because they essentially represent a constant current drain even when switching. If an output is part of a differential pair, then its contribution should be multiplied by a factor of 0.15. Simultaneously switched STECL outputs do contribute to the delay with the contribution being half the value shown for the 50 ohm or 68 ohm output type. Simultaneously switched TTL outputs will have negligible delay effects.

5.1.8 Simultaneous Switching Noise

When simultaneously switching single-ended outputs, a noise pulse is coupled to the non-switched outputs due to cross-talk and lead inductance. The maximum noise amplitude is typically less than 200 mV for ECL and 400 mV for TTL if the simultaneous switching limits are observed. The width of the noise pulse will vary with the rise times of the outputs being switched, but is typically between 1 and 2 nanoseconds.

5.1.9 Output Delays

Output macro specifications include metal routing to the die pad, the die pad, package capacitive loading effects, and stray capacitance. The capacitance due to the routing is given in Section 5.1.1.

All TTL output macro delay tables in the library contain a load factor for calculation of external (outside the package) loading. In general, this linear approximation will result in an accurate delay for a loaded output. TTL OR/NOR, and tri-state output delays versus capacitance curves are shown in Figures 5-1 to 5-3.

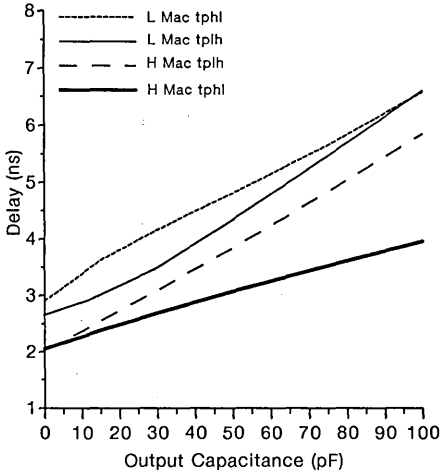


Figure 5-1 TTL OR/NOR Output Delay versus Output Capacitance

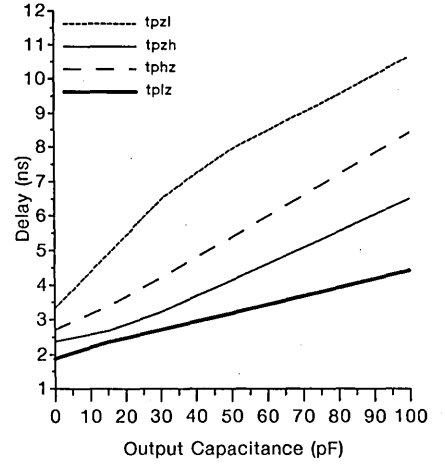


Figure 5-2 Tri-State Enable to Output Delay versus Output Capacitance (L Macro)

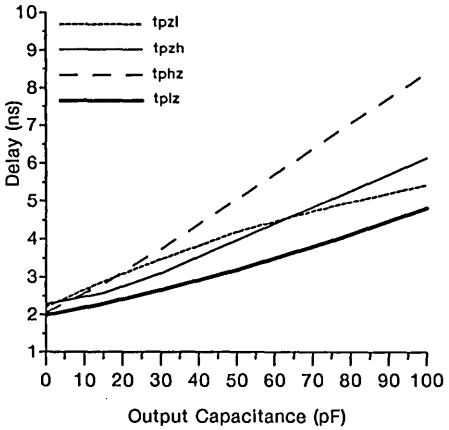


Figure 5–3 Tri–State Enable to Output Delay versus Output Capacitance (H Macro)

5.1.10 Output Edge Rates

Output rise/fall times for various output configurations on MCA3 ETL arrays are summarized in Table 5–5. These rise/fall times are specified for a stray capacitance of ≤5pF (see Figure 10–1) and an appropriate load resistor (50, 68, or 25 ohms) connected to –2.0 Vdc.

TABLE 5–5 MCA3 ETL Rise/Fall Time Specification

ECL OUTPUT TYPE	NO SLOWDOWN		W/SLOWDOWN	
	MIN	MAX	MIN	MAX
50 ohm (H Macro)	0.4 ns	1.2 ns	0.6 ns	2.2 ns
68 ohm (L Macro)	0.4 ns	1.4 ns	0.6 ns	2.5 ns
25 ohm cutoff	0.3 ns	1.9 ns	0.5 ns	2.9 ns
50 ohm cutoff	0.4 ns	2.0 ns	0.6 ns	3.0 ns
STECL – 6 mA	0.4 ns	1.6 ns	0.6 ns	2.7 ns
STECL – 10 mA	0.4 ns	1.4 ns	0.6 ns	2.5 ns
HE70 Macro	0.1 ns	0.4 ns	N/A	N/A
HE71 Macro	0.1 ns	0.4 ns	N/A	N/A
TTL OUTPUT TYPE	@ 15 pF Load		@ 50 pF Load	
	MIN	MAX	MIN	MAX
12 mA	1.8 ns	6.5 ns	2.0 ns	8.0 ns
24 mA	1.5 ns	4.5 ns	1.5 ns	7.0 ns

Note: ECL rise/fall times are for 20–80%.
TTL rise/fall times are for 10–90%.
Rise and fall times based on full swing output.

5.1.11 SLOWDOWN Capacitor Delay

An option can be used [SLOW property] to select a slowdown capacitor in order to decrease the slew rate of a given set of ECL outputs. For more information on how to use this property in a design, see Section 6.4. If a slowdown capacitor is used on an output, the following delay occurs due to the edge rate degradation:

$T_{pd\_SLOWDOWN}$ = 0.5 ns.

5.2 Between Internal Macros

This section specifies the various delay degradations associated with connections in the internal portion of the macrocell array. The macrocell delays themselves are shown in the Macrocell Library and represent the maximum worst–case delays across temperature, process, and voltage, for 0 metal while driving one upper level input equivalent to the driving macro.

5.2.1 Metal and Fanout Degradation

The delay due to interconnections between internal major cells is basically a capacitive loading effect rather than a transmission line phenomena. The loading can be accurately modeled as a distributed capacitance along the metal run itself, a lumped capacitance at the base of the input transistor(s) of the receiving cells, a series metal resistance, and a lumped capacitance at the emitter follower transistor(s) of the driving cell(s) in the case of a wired–OR. The input capacitance of a macrocell is basically a function of its input current. The effective input capacitance seen by a rising edge is also different than that seen by a falling edge. The equations include worst–case process, temperature, and voltage variations.

5.2.2 Metal/Fanout Delay Equations

The following equations specify the delay degradation of a signal due to metal length and fanout. All delay values are in picoseconds and all metal lengths are in mils. A delay calculation example is given on page 5–9. Refer to Section 5.2.3 for information on estimating metal lengths before placement and routing.

Rising Edge Metal/Fanout Delay – General Equation (ps) – **Worst Case** (T_J = 115 °C)

$$T_{pd+} = 1.25(K_r)(\Sigma N_i C_i - C_{DR} + L_{M1}C_{M1} + L_{M2}C_{M2})(R_{sr} + 0.7L_{M1}R_{M1} + 0.7L_{M2}R_{M2}) + T_{ECS} + T_{WOR+}$$

where:

$K_r = K_R[1-K_{TR}(115-T_j)]$ for $L_{M1} + L_{M2} \leq 150$ mils
$K_r = K_R[1-K_{TR}(115-T_j)][0.715 + 0.285e^{-((L_{M1}+L_{M2}-150)/250)}]$ for $L_{M1} + L_{M2} > 150$ mils
$R_{sr} = R_{SR}[1-K_{TSR}(115-T_j)]$

Falling Edge Metal/Fanout Delay – General Equation (ps) – **Worst Case** (T_J = 25 °C)

$T_{pd-} = 0.88(\Sigma N_i C_i - C_{DR} + L_{M1}C_{M1} + L_{M2}C_{M2})(R_{sf} + R_{mf}) + T_{WOR-}$ (for Y,Z,N outputs)
$T_{pd-} = 0.19K_f(\Sigma N_i C_i - C_{DR} + L_{M1}C_{M1} + L_{M2}C_{M2})(R_{sfr} + 0.7L_{M1}R_{M1} + 0.7L_{M2}R_{M2})$ (for R outputs)

TTL Output Macro Loading Delay Calculation (ps) – **Worst Case**

$$T_{pd+/-TTL\_OUT} = TTL_{+/-\_LF}(C_{PKG} + C_{PAD\_CELL} + C_{EXTERNAL\_LOAD} - 15\ pF)$$

where:

$R_{mf} = 0$ when $R_{sf} \geq 0.7L_{M1}R_{M1} + 0.7L_{M2}R_{M2} + R_{sr}$
$R_{mf} = R_{sr} - R_{sf} + 0.322L_{M1} + 0.133L_{M2}$ when $R_{sf} < 0.7L_{M1}R_{M1} + 0.7L_{M2}R_{M2} + R_{sr}$
$R_{sf} = R_{SF}[1-K_{TSF}(T_j-25)]$
$R_{sfr} = R_{SFR}[1-0.0011(T_j - 25)]$
$K_f = 0.53[1-0.0013(T_j - 25)][1 - 1.5((V_{EEE}/V_{EEEnom}) - 1)]$
$TTL_{+/-\_LF}$ = + or – edge loading factor from TTL macro delay tables.

Definition of Parameters and Typical Values

C_{DR} = Upper level input capacitance of the driving macro, except Z outputs, where C_{DR}=0.09 pF (However, for L/HT00 use C_{DR} = 0, due to the 1 pF input capacitance of L/HT00)
T_{ECS} = 25 ps for High Drive or H macro twinned output with 2 EFC's (emitter follower currents)
T_{ECS} = 50 ps for an L macro twinned output with 2 EFC's (emitter follower currents)
T_{ECS} = 0 ps for all other cases. ('ECS' stands for 'Extra Current Source')
L_{M1} = Length of metal1 (in mils)
L_{M2} = Length of metal2 (in mils)
C_{M1} = Capacitance per mil of metal1 0.00385 pF/mil (typ)
C_{M2} = Capacitance per mil of metal2 0.00415 pF/mil (typ)
R_{M1} = Resistance per mil of metal1 0.46 ohms/mil (typ)
R_{M2} = Resistance per mil of metal2 0.19 ohms/mil (typ)
R_{SR} = Source resistance rising (from Table 5-6), T_j = 115°C
R_{SF} = Source resistance falling (from Table 5-6), T_j = 25°C
$T_{WOR}+$ = Rising-edge wired-OR delay (from Table 5-8).
$T_{WOR}-$ = Falling-edge wired-OR delay (from equation in Section 5.2.8).
R_{mf} = Weighted metal resistance (falling).
K_R = Rising-edge metal/fanout delay coefficient (from Table 5-6), T_j = 115°C
K_{TR} = Temperature coefficient for K_R 0.00085/°C (typ)
K_{TSR} = Temperature coefficient for R_{SR} 0.0011/°C (typ)
K_{TSF} = Temperature coefficient for R_{SF} 0.0014/°C (typ)
R_{sfr} = source resistance for R outputs (from Table 5-6, T_j = 25 °C)
K_f = falling edge metal fanout delay coefficient

$\Sigma N_i C_i$ is the sum of the input capacitances on the net. To calculate this number, multiply the input capacitance (C_i) for each type of input on the net (from Table 5-7) by the number (N_i) of those input types and sum the individual results. If a macrocell input is connected to more than one input type internal to the macro, the AC loading factors are given in a separate AC loading table. In the **internal cell library**, if only a DC loading factor is present in parentheses, then that number also represents the AC load (i.e. if a lower level input has a (2) by it, then the Ci value should be multiplied by two). In the **output cell library**, if the **AC load** is more than **one**, then it will be indicated in a separate AC loading table. **Do not multiply** the Ci value for an input by the **DC loading number in ( )** for the **output cell macros.**

The AC loading tables in the Macrocell Library are included to provide a more accurate estimate of AC load capacitance. These numbers can be used in the **Rising and Falling Edge Metal/Fanout Delay Equations** provided above. However, the metal/fanout delay calculations on the Motorola WACC CAD system modify the values in the AC loading tables for certain cases. For instance, the WACC system truncates the number of AC loads to an integer value. For macros with both upper and lower level AC load values, the AC capacitance differs slightly from that calculated by WACC. All AC propagation delays calculated by the WACC CAD system are the worst case specified delays and are guaranteed by AC testing.

TABLE 5–6 Source Resistances –Rsr, Rsf and Rising Edge Delay Coefficient – Kr

Internal (M) Cells and Input (Cxx, Bxx, & T/P00) macros

All R Values in Ohms		# of EFC's	LOW POWER ARRAY			
			L MACRO		H MACRO	
			Twinned	Single	Twinned	Single
R_{SR}	Except Quad Buffers	1 or 2	400	530	200	265
	Quad Buffers	1 or 2	520	660	260	330
R_{SF}	All Except Quad Buffers and R Outputs	2	475	–	508	–
		1	1100	1012	1140	1052
	Quad Buffers	2	425	–	476	–
		1	1050	960	1106	1012
R_{SFR}	R Outputs 881,882	resistor	4640	–	–	–
K_R	All Except Quad Buffers	2	1.25	–	1.05	–
		1	1.10	1.16	0.95	1.0
	Quad Buffers	2	1.40	–	1.25	–
		1	1.15	1.25	1.10	1.16

See Notes applicable to Table 5–6 at top of next page.

Z Outputs (Exx macros)

All R Values in Ohms		LOW POWER ARRAY	
		L MACRO	H MACRO
R_{SR}	Z Output	50	35
R_{SF}	Z Output	1052	1052
K_R	Z Output	1.1	

HI DRIVE Macros

	# of EFC's	Twinned	Single
R_{SR}	1 or 2	100	135
R_{SF}	2	250	–
	1	585	520
K_R	2	1.05	–
	1	0.95	1.0

TABLE 5–7 Input Capacitance, Ci (typical)

FANOUT CAPACITANCE Ci (in pF)		LOW POWER ARRAY	
CELL TYPE	INPUT TYPE	L MACRO	H MACRO
INTERNAL (M CELL)	UPPER	0.07	0.09
	LOWER	0.05	0.05
OUTPUT (E,B,ZE,S,T,P macros)	UPPER	0.18	0.23
	LOWER	0.07	0.07
ECL INPUT (C macros)	UPPER	0.07	0.09
	LOWER	0.05	0.05
TTL INPUT (T00&P00 macros)	UPPER	1.0	1.0
HI DRIVE	UPPER	0.12	--
	LOWER	0.05	--

Note: "LOWER" inputs are marked with a '*' or a '#' in the Macrocell Library. Inputs which appear in an AC LOADING TABLE in the Macrocell Library represent some combination of UPPER and LOWER inputs.

NOTES FOR TABLE 5–6:

1. Values shown for R_{SR} and K_R are typical values at T_j = 115°C.

2. Values shown for R_{SF} and R_{SFR} are typical values at T_j = 25°C

3. # of EFC's refers to the number of emitter follower current sources connected to the output:

   1 EFC = 0.48 mA in the Low Power Array, 0.96 mA for HI DRIVE macros.

   2 EFCs = 0.96 mA in the Low Power Array, 1.92mA for HI DRIVE macros.

   R output (resistor) = 0.88 mA (881 & 882)

   (R outputs are twinned internally and have a resistor pulldown instead of a current source.)

AC Delay Variations Versus Voltage and Temperature

The array exhibits the following metal/fanout delay factors due to changes in the junction temperature (T_J) and the supply voltages (V_{EEE}):

K_r decreases 0.91% with a 10°C decrease
R_{sr} increases 1.22% with a 10°C increase
R_{sf} decreases 1.4% with a 10°C increase
R_{sf} increases 1.4% with a 5% increase in $|V_{EEE}|$
R_{sfr} decreases 1.1 % for 10°C rise
K_f decreases 1.4 % for 10°C rise

The macro delays themselves are specified at T_j = 115°C, and V_{EEE} = −5.2 ± 8% or −4.5 ± 0.3 Vdc. The macro delay variation due to voltage supply and temperature change is negligible over the specified operating range of V_{EEE} and T_J = 25°C to 115°C.

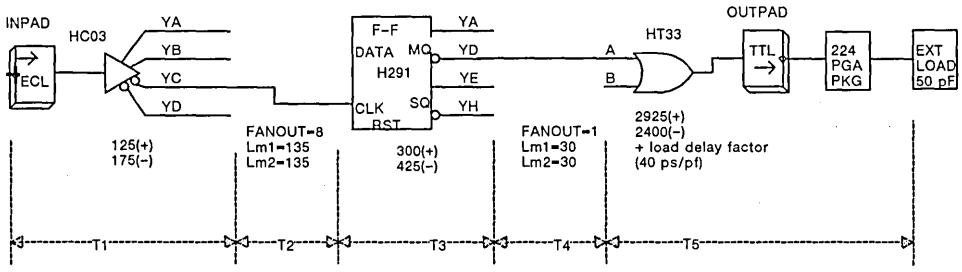


Figure 5–4 Path Delay Example

Path Delay Example Calculation

Figure 5-4 shows an example of a delay path from an input pad, through some internal logic, and finally to an output pad on an MCA3 ETL array. For this example, a 224PGA package will be used for package delay values. Assume that a high to low transition occurs at the input pad, the H291 YD output is currently low, and the data input to the H291 is setup low. The total input to output delay can be broken down into five components, T1–T5. The calculation of each component is done in the following manner:

$T1 = T_{pd\_PKG\_PIN\_224} + T_{pd[RISE/FALL]} + T_{pd\_macro}$

The input pad and macro HC03 are specified in the library for the delay from the pad to the macro output.

$T_{pd\_PKG\_PIN\_224}$ = 350 ps

The increased delay due to the rise time variation from input capacitance can be calculated as described in Sections 5.1.1, and 5.1.2 as shown below:

C_{IP} = 13 + 0.09 = 13.09 pF

$\Delta t_{r/f} = 0.6 Z_O C_{IP} = 0.6(50)(13.09) = 393$ ps

$t_{r/f[TOTAL]} = t_{r/f[TESTER]} + \Delta t_{r/f} = 1 + 0.393$
$= 1.393$ ns

so
$t_{pd[RISE/FALL]} = (50)(1.393 - 0.5) = 45$ ps

T_{pd_macro} = 125 ps

T1 = (45 + 350 + 125) ps => 525 ps
(rounded to nearest 25 ps)

T2 = rising edge metal/fanout delay of HC03

Using the rising edge metal/fanout delay equation for internal macrocells for the fanout and metal length shown on the HC03 output, the following number is calculated for T2:

$T2 = 1.25(K_r)[(8)(0.05)-0.09+(135)(0.00385)+$
$(135)(0.00415)][(265+0.7(135)(0.46)+$
$0.7(135)(0.19)] + 0 + 0$
where
$K_r = 0.715 + .285e^{-((135+135-150)/250)} = 0.891$
which gives
T2 = 505 which rounds to 500 ps

T3 = clock to MQ delay for output rising
= 300 ps

T4 = rising edge metal/fanout delay of H291

Using the same formula as in the T2 calculation:

$T4 = 1.25(1.0)[(1)(0.23)-0.09+(30)(0.00385)+$
$(30)(0.00415)][(265+0.7(30)(0.46)+$
$0.7(30)(0.19)] + 0 + 0$
= 132.4 ps => 125 ps
(rounded to nearest 25 ps)

$T5 = T_{pd+HT33} + T_{pd+/-\_TTL\_OUT} + T_{pd\_PKG\_PIN\_224}$

Using the load factor for a rising edge output on macro HT33, the delay due to loading is calculated as follows:

$T_{pd+/-\_TTL\_OUT} = TTL_{+/-\_LF}(C_{PKG} + C_{PAD\_CELL} + C_{EXTERNAL\_LOAD} - 15\text{ pF})$

$= 40\text{ps/pF}[(11+2+50-15)\text{ pF}] = 1920$ ps

T5 = 2925 + 1920 + 350 = 5195 ps

The total delay from the input package pin to the output package pin is:

$T_{pd\_TOT} = T1 + T2 + T3 + T4 + T5$
$= (525 + 500 + 300 + 125 + 5195)$ ps
$= 6645$ ps

Note that MCASIM and ACMCASIM simulators will round off all delays to the nearest 25 ps increment.

In order to simplify the general metal/fanout delay equations, the designer may wish to make certain assumptions based on a particular design. The following set of assumptions, for example, results in the reduced forms of the equations listed.

List of Typical Assumptions:

1. A low power macro is driving upper level inputs of low power macros on a low power array.
2. The output is not twinned (i.e. only one emitter follower current, or EFC, is used)
3. $L_{M1} + L_{M2} \leq 150$ mils
4. $L_{M1} = L_{M2}$
5. 30 mils of metal are used per connection
6. The output is not part of a wired OR
7. All delays are at worst-case temperature, nominal V_{EEE}, and worst-case process.

Reduced Forms of the Worst Case Rising and Falling Edge Metal/Fanout Delay Equations

$T_{pd}+ = (2N^2 + 150N + 40)$ ps where $N \leq 4$

$T_{pd}- = (170N + 45)$ ps where $N \leq 4$

where N is the number of inputs being driven by the output in question.

Remember that any reduced forms of the metal/fanout delay equations are valid **only** for the conditions used in making the assumptions.

5.2.3 Estimating Metal Lengths Before Place and Route

The average metal length per fanout on a gate array will vary with factors such as array size, cell architecture, circuit topology, amount of fixed placement and routing, and the proficiency of the placement and routing software. For the MCA6200ETL and MCA3200ETL, the following equations are used by the Motorola CAD system to estimate metal length on a net as a function of the fanout:

$L_{M1} = (15N + 15)$ mils
$L_{M2} = (15N + 15)$ mils

For the MCA750ETL, the estimated net length per fanout is 20mils and described below:

$L_{M1} = (10N + 10)$ mils
$L_{M2} = (10N + 10)$ mils

total metal length on net = $L_{M1} + L_{M2}$

where N is the fanout on the net. Note that a macro input on the net with an internal fanin number greater than one (as indicated by a number in parentheses next to the input) still only counts as a fanout of one for estimating metal length.

The designer should note that the above equations do not produce a worst-case number for metal length. The formulas do yield a valid typical number based on statistical data of placed and routed MCA3 ETL options. If the net in question is weighted higher than other nets, the following equations can be used to estimate metal length per fanout:

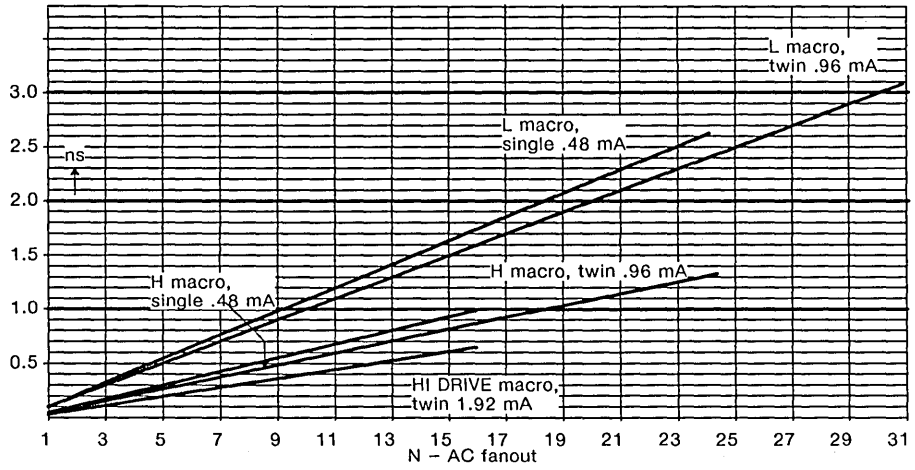
$L_{M1} = (10N + 10)$ mils
$L_{M2} = (10N + 10)$ mils

The Motorola placement program, AUTOP, produces a pre-route estimate of the metal length for each net. This estimate is based on the Manhattan distance multiplied by a factor of 1.2. The Manhattan distance is the shortest length of metal required to connect all ports on a net using only 90 degree angles.

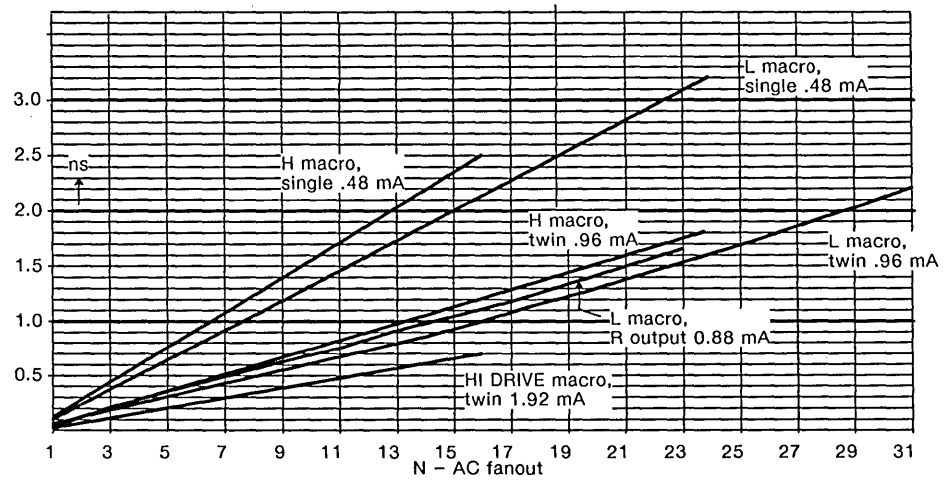
5.2.4 Metal/Fanout Delay Curves

The following set of curves show the metal/fanout delay which must be added to the delay of a macro as a function of the AC fanout being driven by the macro output. AC fanout refers to the number of upper level inputs of the same macro type being driven. An AC fanout of 10 for an H macro refers to an H macro output driving 10 upper level H macro inputs. The curves also reflect the effects of a given length of metal per connection (20 or 30 mils).

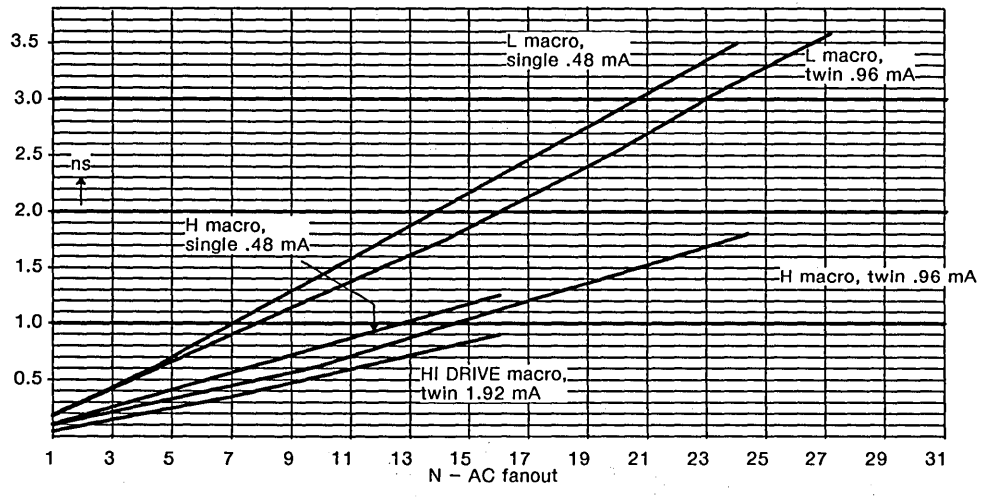
Internal Macro Rising Edge Delay, $t_{pd}+$ (LPA, 20 mils/connection, Worst Case T_J = 115 °C)



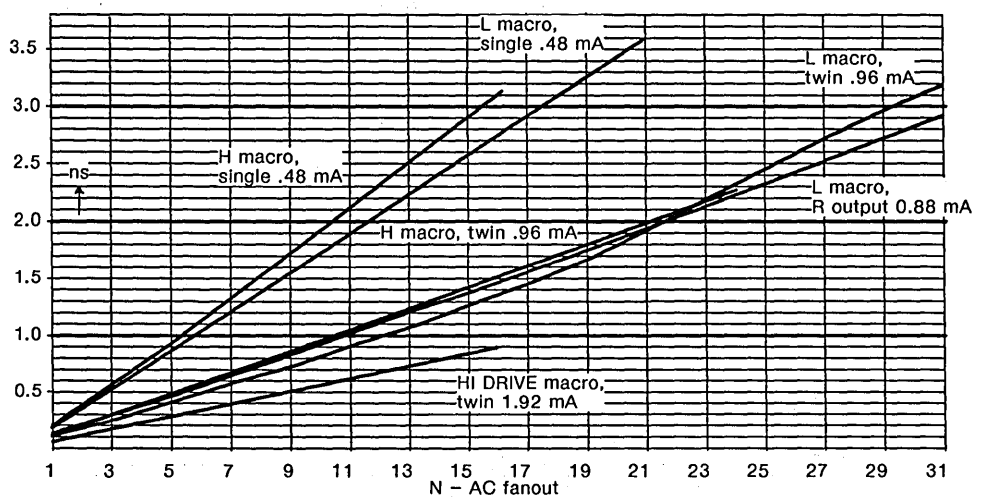
Internal Macro Falling Edge Delay, $t_{pd}-$ (LPA, 20 mils/connection, Worst Case T_J = 25 °C)



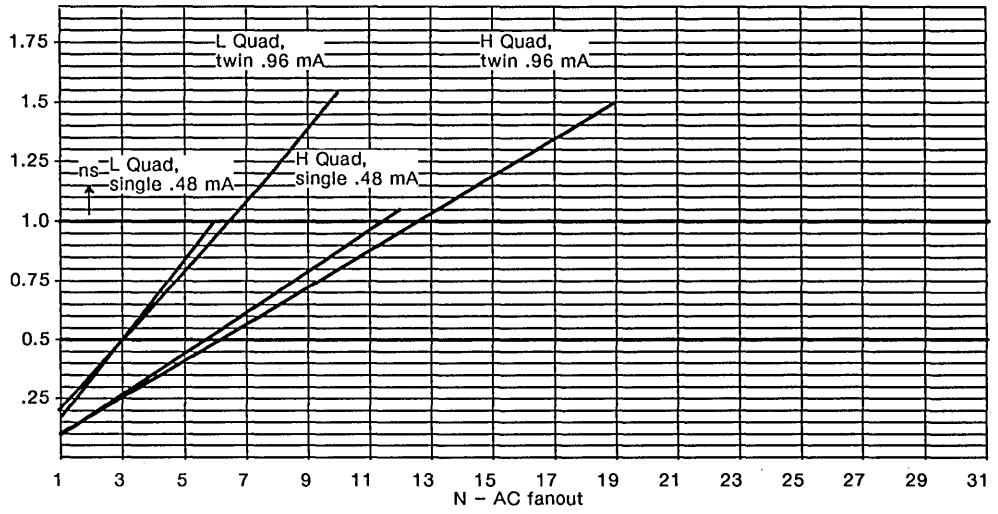
Internal Macro Rising Edge Delay, $t_{pd}+$ (LPA, 30 mils/connection, Worst Case T_J = 115 °C)



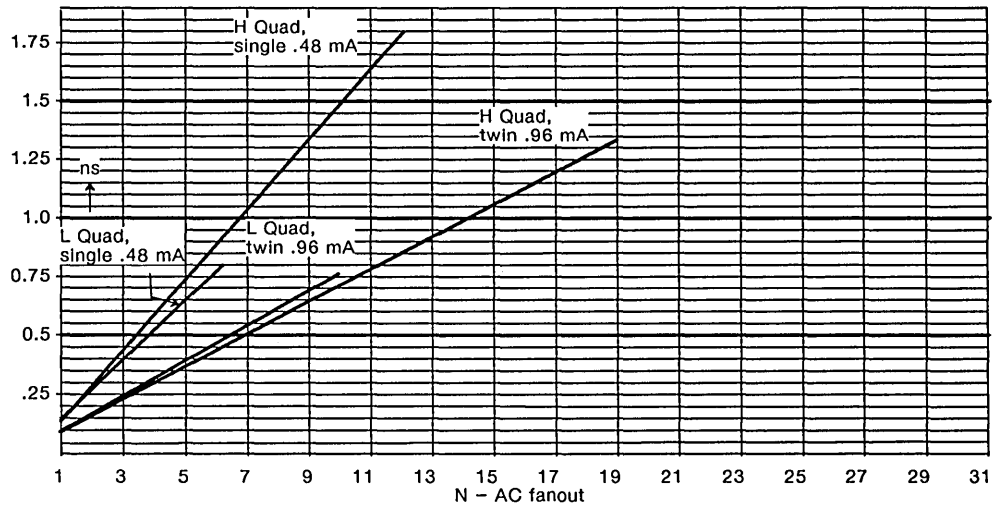
Internal Macro Falling Edge Delay, $t_{pd}-$ (LPA, 30 mils/connection, Worst Case T_J = 25 °C)



Quad Buffer Rising Edge Delay, $t_{pd}+$ (LPA, 20 mils/conn, Worst Case T_J = 115 °C)



Quad Buffer Falling Edge Delay, $t_{pd}-$ (LPA, 20 mils/conn, Worst Case T_J = 25 °C)



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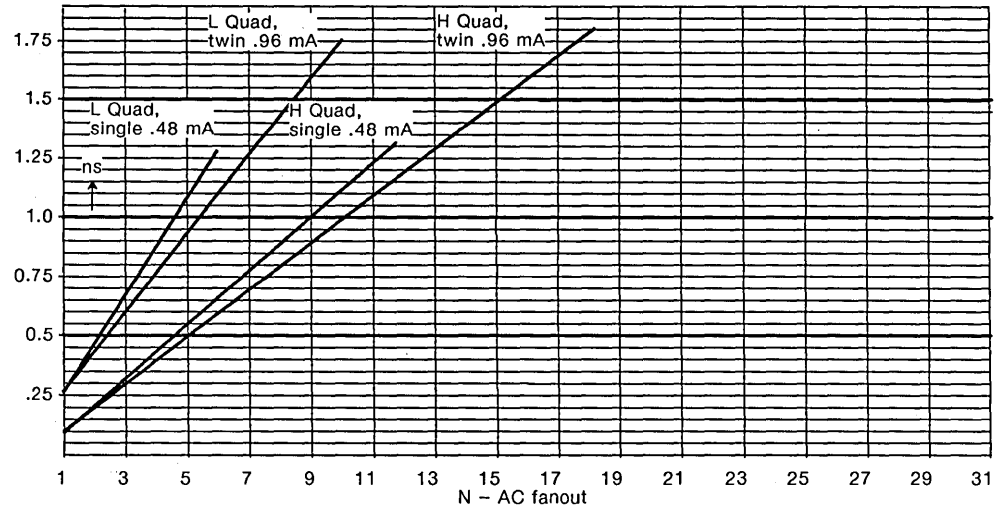
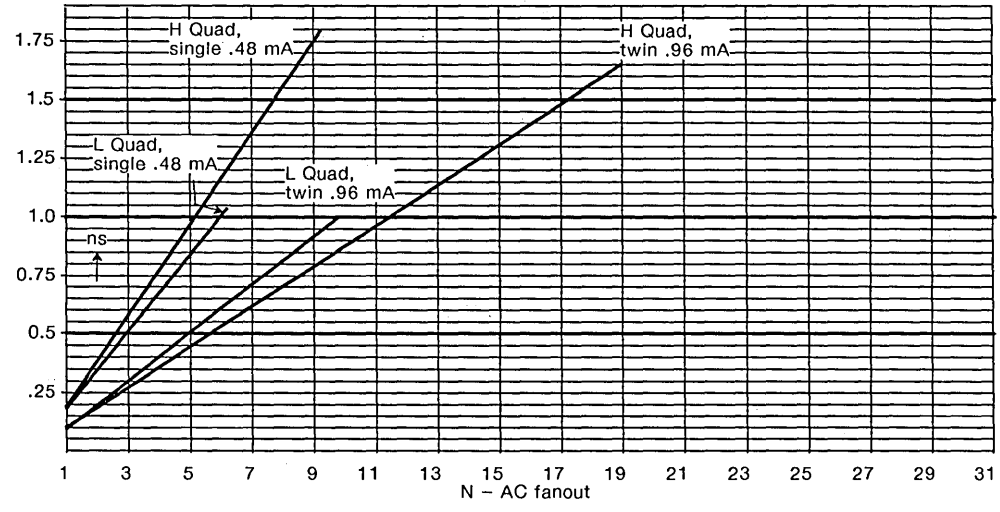
Quad Buffer Rising Edge Delay, $t_{pd}+$ (LPA, 30 mils/conn, Worst Case T_J = 115 °C)



Quad Buffer Falling Edge Delay, $t_{pd}-$ (LPA, 30 mils/conn, Worst Case T_J = 25 °C)



5.2.5 Twin Outputs Driving a Single Net

It is important to note that the falling edge metal and fanout delays can be approximately cut in half by using twin outputs tied together ("twinned") with two current source pulldowns. Many of the macrocells in the library have one or more double emitter output transistors which share a common base. Output emitters on the same transistor are known as "twin outputs" and can be tied together for increased drive. Each pair of these outputs has two current source pulldowns available to it, used for controlling the internal macros' drive capability. The number of current source pulldowns on an output net is selected via the MAMP property value during schematic capture, or by selecting the MAMP value in the FIX file (see Section 6.) Speeding up the falling edge delays can bring them into line with the usually faster rising edge metal/fanout delays. Matching the rising and falling edge output delays in this manner can help reduce pulse width shrinkage and other skew problems in metal paths. The AC effects of using a twinned output are included in the metal/fanout delay equations and the metal/fanout delay curves.

5.2.6 Twin Outputs Driving Separate Nets

When twin outputs are not tied together, but are used to drive separate loads, part of the **rising edge** delay from each output is reflected back to the other. Both outputs will experience the same metal and fanout delay degradation. To calculate this delay, first calculate the metal and fanout rising edge delay for both outputs, $T_{pd+(Y1)}$ and $T_{pd+(Y2)}$, individually using the rising edge delay equation in Section 5.2.2. The metal and fanout rising edge delay for **both** outputs will then be the largest of the following two equations:

1. $(T_{pd+} = T_{pd+(Y1)} + 0.333T_{pd+(Y2)} + T_{ECS})$ ps
2. $(T_{pd+} = T_{pd+(Y2)} + 0.333T_{pd+(Y1)} + T_{ECS})$ ps

where T_{ECS} is 25 ps for an H macro and 50 ps for an L macro.

5.2.7 Quad Buffer Outputs Driving Separate Nets

The following macrocells in the library have four functionally equivalent outputs: 501, 502, 571 (which has eight equivalent outputs), C01 and C02. These are referred to as "Quad Buffers". The outputs of these macrocells consist of two twin emitter transistors (a.k.a. "twins") connected to the same base - twin outputs YA and YB on one transistor and twin outputs YC and YD on the other. The **rising edge** delay for all four outputs, therefore, is the same and is based on the total loading on all four outputs. **Thus, the rising edge delays calculated for the outputs of a Quad Buffer must be modified if more than one output is being used.** These delays should be modified in the following manner:

1. First calculate the rising delay for pairs YA/YB, $T_{pd+(YA/YB)}$. If the twin pair is tied together, use the appropriate rising edge metal/fanout delay equation in Section 5.2.2. If YA and YB are driving separate loads, use the procedure in Section 5.2.6.
2. Repeat step 1 for outputs YC and YD to get $T_{pd+(YC/YD)}$.
3. The rising delay for **all outputs** on the macro is the largest delay of the following two equations:

$$T_{pd+} = T_{pd(YA/YB)} + 0.25T_{pd(YC/YD)}$$
$$T_{pd+} = T_{pd(YC/YD)} + 0.25T_{pd(YA/YB)}.$$

5.2.8 Wired-OR Delays

Wired-OR configurations of internal macro outputs will cause some delay degradation which must be added to the metal fanout delays calculated in Section 5.2.1. The maximum wired-OR delay for the falling edge is given below.

Falling Edge Wired-OR Delay (T_{WOR-})

$$T_{WOR-} = [40N_E(0.4mA/I_{EF})] \text{ ps}$$

where N_E is the total number of emitters tied together to form the wired-OR (twinned outputs count as two emitters in this number), and I_{EF} is the output emitter follower current. This degradation is small because the capacitance of the additional output devices on the line is very small. The propagation delay for the output rising edge, T_{WOR+}, as shown in Table 5-8, however, is usually much greater. When two macro outputs are tied together in a wired-OR configuration and both are in the logic low state (V_{OL}), one output could be supplying more current to the current source pulldowns than the other (called current hogging). When the output that is supplying the smallest amount of current switches to the logic high state (V_{OH}), it must now supply all of the current resulting in the additional rising edge delays shown in the table.

NOTE: The wired-OR delays in the following table should only be added to macro outputs which have an **external** wired-OR connection. The delay should **not** be added to the delay path for a macro output which has only internal macro wired-ORs - these delays are included in the internal macro delays.

TABLE 5–8 Rising Edge Wired–OR Delay (Twor+)

MACRO TYPE L or H		# of EFC's	WIRED–OR TOTAL (Nw)		
			2	3	4
HI DRIVE	L	2	100	125	150
		1	75	100	125
LPA	H	2	125	155	185
		1	75	105	135
	L	2	200	235	270
		1	125	160	195

EFC – Emitter Follower Current Sources.

N_W is the number of wired ORs. Note that twinned outputs only count as one in this number as opposed to N_E where the twin outputs count as two emitters. The designer should note that two EFC's on a net can only be used on a wired–OR net if all outputs on the net are twinned. Refer to Section 4.2.6 for functional rules concerning wired ORs.

5

5.3 Delay Skew Considerations

The Motorola CAD system does not account for skew considerations as discussed below. A skew calculation is performed during the execution of MCASIM with the IRACE option. See Section 3.4.4 of the Motorola CAD Reference for ASIC Design and Release Manual for information on IRACE.

5.3.1 Minimum Propagation Delays Due to Process Variation

The maximum delays specified in the metal and fanout delay equations are worst–case over process (the temperature and voltage variations are called out explicitly). The macrocell delays specified in the library are worst–case maximums over process, voltage, and temperature. The **minimum** delays in the various elements on the array due to process variations are specified below as K factors which should be multiplied by the appropriate maximum delays.

Minimum Delays

For macrocell outputs without collector dots:

$K_{MACRO\_MIN} = 0.4$

For macrocell outputs with collector dots:

$K_{MACRO\_MIN} = 0.3$

For all internal 700 series macros and 70 series I/O macros:

$K_{MACRO\_MIN} = 0.55$

For metal/fanout delay:

$K_{METAL\_MIN} = 0.4$

5.3.2 Electrical Adjacency

Certain macrocells are said to be "electrically adjacent" to others. This means that these macrocells are connected to the same slave bias drivers. Electrically adjacent cells share a common row and reside together generally in groups of three or four adjacent columns. (i.e. columns 0,1, and 2; 3,4, and 5, etc. Where column 0 begins on the left side of the array.) The floorplans for each array shown in Section 4.3 identify the electrically adjacent M–cells by a solid black line at the bottom of the M–cell columns.

5.3.3 On–Chip Propagation Delay Skew

The on–chip propagation delay skew is defined as the largest delay difference which can exist between similar signal path elements (i.e. macros or metal) located in different places on the die. This delay skew depends on the types and relative positions of elements making up the delay path.

In order to guarantee that the worst–case skew conditions are analyzed, the designer should calculate the skew between the two paths in question for four cases:

1. assuming that the chip has slow macros and slow metal; therefore, all delays are running at the specified maximums.

2. assuming that the chip has fast macros and fast metal: therefore, all delays are running at the minimum values as discussed in Section 5.3.1.

3. assuming that the chip has fast macros and slow metal.

4. assuming that the chip has slow macros has fast metal.

The skews are given as K factors. In order to analyze skew for the "slow chip" case, the maximum delay is multiplied by the K factor listed to provide the skewed delay. For the "fast chip" case, the minimum delay is multiplied by 1/K.

Internal Major Cell Delay Skews

For macro outputs **without** collector dots (a '$' next to an output in the Macrocell Library denotes a collector dot) or a macro having true and complement outputs:

$K_{MACRO\_SKEW} = 0.8$

For differential receivers being driven differentially:

$K_{MACRO\_SKEW} = 0.9$

For macro outputs **with** collector dots:

$K_{MACRO\_SKEW} = 0.4$

For electrically adjacent identical internal Major cell macros with no collector dotting:

$K_{MACRO\_SKEW} = 0.92$

I/O (U) Cell Delay Skews

For physically adjacent, U-cell input macros:

$K_{MACRO\_SKEW} = 0.85$

For any two non-adjacent U-cell input macros:

$K_{MACRO\_SKEW} = 0.8$

For physically adjacent identical U-cell output macros:

$K_{MACRO\_SKEW} = 0.85$

For non-adjacent U-cell output macros:

$K_{MACRO\_SKEW} = 0.7$

Note: The U-cell output macro skews above do not take into account the effects of simultaneous switching, which must also be added in.

Metal, Wired-OR, and Fan-Out Delay Skews

For signals switching in the **same** direction propagating along separate metal paths:

$K_{METAL\_SKEW} = 0.7$

For differential signals switching in the same direction

$K_{METAL\_SKEW} = 0.8$

For signals switching in **opposite** directions propagating along separate metal paths:

$K_{METAL\_SKEW} = 0.6$

For example, assume two L202 macrocells, (Cell 1) and (Cell 2), are placed on opposite sides of a low power chip. Furthermore, assume that the propagation delay time of a rising edge from input A to output YA for macro (1) is the specified maximum, 250 ps. The fastest that the same path (A to YA) can be on macro (2), therefore is:

$$250(0.8) = 200$$

Similarly, the greatest delay difference which can exist between signals switching in the same direction traveling along two equivalent metal paths (equal in length and fanout) is given by:

$$td2 = td1(0.7)$$

where td1 is the larger of the two delays in question and td2 is the smallest value that the other delay can have.

5.3.4 Setup and Hold Time Calculations

Setup and hold times for flip-flops and latches are defined by the following equations:

Setup Time – General Equation

(1) $T_S = T_{MS} + T_{DMAX} - T_{CMIN}$

Hold Time – General Equation

(2) $T_H = T_{MH} + T_{CMAX} - T_{DMIN}$

where:

T_S = setup time at the input
T_H = hold time at the input
T_{CMAX} = maximum clock path time
T_{CMIN} = minimum clock path time
T_{DMAX} = maximum data path time

T_{DMIN} = minimum data path time
T_{MS} = specified macro setup time
T_{MH} = specified macro hold time

NOTE: The setup times, T_{MS}, for each latch and flip-flop are specified in the timing tables in the Macrocell Library. The hold time, T_{MH}, is always zero (0) unless otherwise specified.

The minimum setup time is the amount of time the data must be present at the data input pin before the latching edge of the clock at the clock input pin in order to insure that the data is latched properly. The minimum hold time is the amount of time the data must remain unchanged at the data input pin after the latching edge of the clock at the clock input pin in order to ensure the data will remain valid. A negative hold time means that the data may be changed before the clocking edge and still be successfully latched.

Setup and hold times for flip-flops and latches as seen from the input pins will vary from the times given in the Macrocell Library due to differences in the delay paths leading to the macrocells of interest. The actual setup and hold times as seen from the input pins are found by de-rating the times listed in the Macrocell Library by the difference between the minimum and maximum delay in the clock and data paths leading to the latch or flip-flop. To calculate the effective setup and hold times at the inputs to the delay paths leading to the data and clock/enable, the designer must look at the four possible combinations of slow and/or fast skew effects.

The four combinations are:

1. Slow Chip **(SS)** – slow macros and slow metal.
2. Fast Chip **(FF)** – fast macros and fast metal.
3. Slow macro and fast metal **(SF)**.
4. Fast macro and slow metal **(FS)**.

The factors determining which combination to use depend on the following values and their relationships with each other.

T_{CMAX}, T_{CMIN}, T_{DMAX}, T_{DMIN} = previously defined
T_{CMAC_MAX} = maximum delay due to the macros in the clock path
T_{DMAC_MAX} = maximum delay due to the macros in the data path
T_{CMFO_MAX} = maximum delay due to the metal and fanout in the clock path
T_{DMFO_MAX} = maximum delay due to the metal and fanout in the data path

In order to determine the minimum setup and hold times, taking into account the minimum propagation delay (Section 5.3.1) and the on-chip propagation delay skew (Section 5.3.3), one should use the following set of equations to first determine the case which yields the correct equation for the minimum setup (T_{SMIN}) and minimum hold (T_{HMIN}) times.

Equations to Determine Minimum Setup Time

1A For the **(SS)** case, if the following conditions exist $\Rightarrow$
$T_{CMFO\_MAX} \leq (1/K_{METAL\_SKEW})\ (T_{DMFO\_MAX})$ and $T_{CMAC\_MAX} \leq (1/K_{MACRO\_SKEW})\ (T_{DMAC\_MAX})$, then:

$$T_{SMIN} = T_{MS} + T_{DMAX} - K_{METAL\_SKEW}\ (T_{CMFO\_MAX}) - K_{MACRO\_SKEW}\ (T_{CMAC\_MAX})$$

2A For the **(FF)** case, if the following conditions exist $\Rightarrow$
$T_{CMFO\_MAX} > (1/K_{METAL\_SKEW})\ (T_{DMFO\_MAX})$ and $T_{CMAC\_MAX} > (1/K_{MACRO\_SKEW})\ (T_{DMAC\_MAX})$, then:

$$T_{SMIN} = T_{MS} + (K_{METAL\_MIN}/K_{METAL\_SKEW})\ (T_{DMFO\_MAX}) + (K_{MACRO\_MIN}/K_{MACRO\_SKEW})\ (T_{DMAC\_MAX}) - K_{METAL\_MIN}\ (T_{CMFO\_MAX}) - K_{MACRO\_MIN}\ (T_{CMAC\_MAX})$$

3A For the **(SF)** case, if the following conditions exist $\Rightarrow$
$T_{CMFO\_MAX} > (1/K_{METAL\_SKEW})\ (T_{DMFO\_MAX})$ and $T_{CMAC\_MAX} \leq (1/K_{MACRO\_SKEW})\ (T_{DMAC\_MAX})$, then:

$$T_{SMIN} = T_{MS} + (K_{METAL\_MIN}/K_{METAL\_SKEW})\ (T_{DMFO\_MAX}) - K_{METAL\_MIN}\ (T_{CMFO\_MAX}) + T_{DMAC\_MAX} - K_{MACRO\_SKEW}\ (T_{CMAC\_MAX})$$

4A For the **(FS)** case, if the following conditions exist $\Rightarrow$
$T_{CMFO\_MAX} \leq (1/K_{METAL\_SKEW})\ (T_{DMFO\_MAX})$ and $T_{CMAC\_MAX} > (1/K_{MACRO\_SKEW})\ (T_{DMAC\_MAX})$, then:

$$T_{SMIN} = T_{MS} + T_{DMFO\_MAX} - K_{METAL\_SKEW}\ (T_{CMFO\_MAX}) + (K_{MACRO\_MIN}/K_{MACRO\_SKEW})\ (T_{DMAC\_MAX}) - K_{MACRO\_MIN}\ (T_{CMAC\_MAX})$$

Equations to Determine Minimum Hold Time

1B For the **(SS)** case, if the following conditions exist $\Rightarrow$
$T_{DMFO\_MAX} < (1/K_{METAL\_SKEW})\ (T_{CMFO\_MAX})$ and $T_{DMAC\_MAX} < (1/K_{MACRO\_SKEW})\ (T_{CMAC\_MAX})$, then:

$$T_{HMIN} = T_{MH} + T_{CMAX} - K_{METAL\_SKEW}\ (T_{DMFO\_MAX}) - K_{MACRO\_SKEW}\ (T_{DMAC\_MAX})$$

2B For the **(FF)** case, if the following conditions exist $\Rightarrow$
$T_{DMFO\_MAX} \geq (1/K_{METAL\_SKEW})\ (T_{CMFO\_MAX})$ and $T_{DMAC\_MAX} \geq (1/K_{MACRO\_SKEW})\ (T_{CMAC\_MAX})$, then:

$$T_{HMIN} = T_{MH} + (K_{METAL\_MIN}/K_{METAL\_SKEW})\ (T_{CMFO\_MAX}) + (K_{MACRO\_MIN}/K_{MACRO\_SKEW})\ (T_{CMAC\_MAX}) - K_{METAL\_MIN}\ (T_{DMFO\_MAX}) - K_{MACRO\_MIN}\ (T_{DMAC\_MAX})$$

3B For the **(SF)** case, if the following conditions exist $\Rightarrow$
$T_{DMFO\_MAX} \geq (1/K_{METAL\_SKEW})\ (T_{CMFO\_MAX})$ and $T_{DMAC\_MAX} < (1/K_{MACRO\_SKEW})\ (T_{CMAC\_MAX})$, then:

$$T_{HMIN} = T_{MH} + (K_{METAL\_MIN}/K_{METAL\_SKEW})\ (T_{CMFO\_MAX}) - K_{METAL\_MIN}\ (T_{DMFO\_MAX}) + T_{CMAC\_MAX} - K_{MACRO\_SKEW}\ (T_{DMAC\_MAX})$$

4B For the **(FS)** case, if the following conditions exist $\Rightarrow$
$T_{DMFO\_MAX} < (1/K_{METAL\_SKEW})\ (T_{CMFO\_MAX})$ and $T_{DMAC\_MAX} \geq (1/K_{MACRO\_SKEW})\ (T_{CMAC\_MAX})$, then:

$$T_{HMIN} = T_{MH} + T_{CMFO\_MAX} - K_{METAL\_SKEW}\ (T_{DMFO\_MAX}) + (K_{MACRO\_MIN}/K_{MACRO\_SKEW})\ (T_{CMAC\_MAX}) - K_{MACRO\_MIN}\ (T_{DMAC\_MAX})$$

Example of Setup and Hold Time Calculation Using Delay Skew

The following example shows the calculation of the worst-case hold time at the DATA and CLK inputs to the network. For simplicity, all worst-case gate delays are assumed to be 1 ns. Metal delays are assumed to be 1ns for the data path, and 4ns in the clock path.

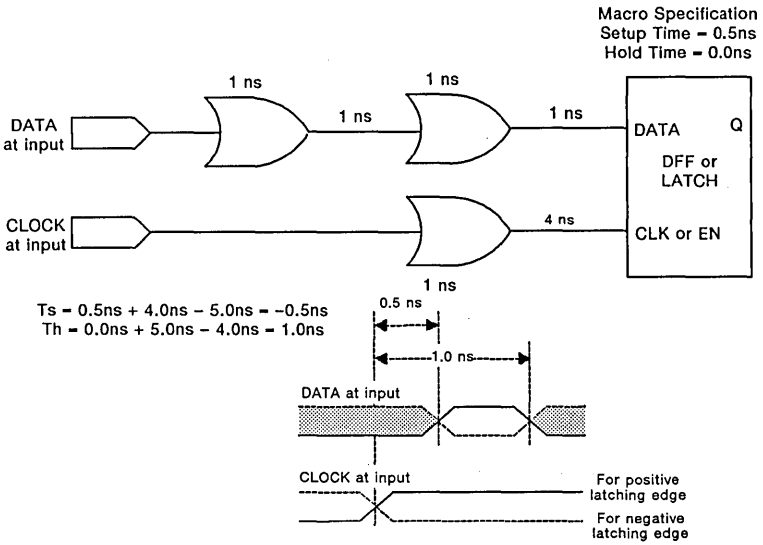


Figure 5-5 Setup and Hold Time Example – No Skew

Figure 5-5 shows the setup and hold time calculation without taking into account the on-chip skew for this example. The setup time at the DFF/LATCH inputs is specified at 0.5 ns. If all max delays are used, the setup time at the DATA and CLK inputs is -0.5 ns. The hold time at the DFF/LATCH inputs is specified at 0.0 ns. If all max delays are used, the setup time at the DATA and CLK inputs is 1.0 ns.

The minimum setup and hold time will now be calculated using the skewed values for the macro and metal delays. First, the case **(SS, FF, SF, FS)** must be found for the setup and hold time.

Case Determination for Setup Time

For this example, the following values can be calculated:

T_{CMAC_MAX} = 1.0ns
T_{DMAC_MAX} = 2.0ns
T_{CMFO_MAX} = 4.0ns
T_{DMFO_MAX} = 2.0ns

Using the equations to determine the case for the minimum setup time would result in case **3A (SF)**, slow macros and fast metal since;

T_{CMFO_MAX} (4.0ns) > $(1/K_{METAL\_SKEW})$ (T_{DMFO_MAX})
= 1.67 (2.0ns) = 3.34ns

and

T_{CMAC_MAX} (1.0ns) ≤ $(1/K_{MACRO\_SKEW})$ (T_{DMAC_MAX})
= 1.25 (2.0ns) = 2.5ns

Case Determination for Hold Time

Using the equations to determine the case for minimum hold time would result in case **4B (FS)**, fast macros and slow metal since;

T_{DMFO_MAX} (2.0ns) < $(1/K_{METAL\_SKEW})$ (T_{CMFO_MAX})
= 1.67 (4.0ns) = 6.68ns

and

T_{DMAC_MAX} (2.0ns) ≥ $(1/K_{MACRO\_SKEW})$ (T_{CMAC_MAX})
= 1.25 (1.0ns) = 1.25ns

Figure 5–6 contains the example circuit showing the setup and hold time calculations with skew. Values in square brackets [ ] are the values used in the setup time calculation, while values in parentheses ( ) are values used to determine the new hold time. The equations are listed below:

The minimum setup time (T_{SMIN}) is calculated by using Equation **3A.**

$$T_{SMIN} = T_{MS} + (K_{METAL\_MIN}/K_{METAL\_SKEW})\,(T_{DMFO\_MAX}) - K_{METAL\_MIN}\,(T_{CMFO\_MAX}) + T_{DMAC\_MAX} - K_{MACRO\_SKEW}\,(T_{CMAC\_MAX})$$

$$= 0.5ns + (0.4/0.6)(2.0ns) - (0.4)(4.0ns) + 2.0ns - (0.8)(1.0ns) = 1.43ns$$

The minimum hold time (T_{HMIN}) is calculated by using Equation **4B.**

$$T_{HMIN} = T_{MH} + T_{CMFO\_MAX} - K_{METAL\_SKEW}\,(T_{DMFO\_MAX}) + (K_{MACRO\_MIN}/K_{MACRO\_SKEW})\,(T_{CMAC\_MAX}) - K_{MACRO\_MIN}\,(T_{DMAC\_MAX})$$

$$= 0.0ns + 4.0ns - (0.6)(2.0ns) + (0.4/0.8)(1.0ns) - (0.4)(2.0ns) = 2.50ns$$

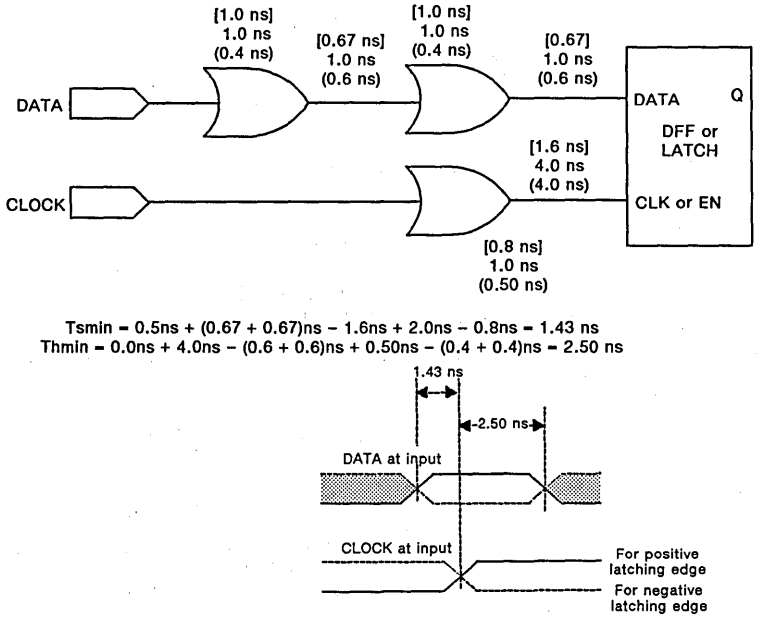


Figure 5–6 Setup and Hold Time Example – With Skew

5.3.5 Propagation Delay Skew Between Two Chips

The minimum delays for given logic elements on an array are specified in Section 5.3.1. If two MCA arrays interface in the same system, ($\Delta T_J \leq 20°C$, voltage ± 5%) the actual skew between two identical paths is less than the difference between the absolute minimum and maximum delays. This is because part of the spread between absolute minimums and maximums is due to guardbanding for delay specification inaccuracies. Such inaccuracies include the rounding of delays up to the nearest 25 ps and simulation and characterization inaccuracy. The following K factors can be used to determine skew between paths on two different chips. The K factor should be multiplied by the maximum delay number to determine the minimum number for an identical element on another MCA chip.

Macro Delay Skew Between Chips

Macros with no collector-dotted '$' outputs:

$$K_{MACRO\_SKEW} = 0.5$$

For the same differential receiver macro driving other differential receivers on two different devices:

$$K_{MACRO\_SKEW} = 0.65$$

Macros with collector-dotted '$' outputs:

$$K_{MACRO\_SKEW} = 0.4$$

Metal/Fanout Delay Skew Between Chips

For two metal paths having the same metal length, fan-out and output follower current with signals switching in the same direction on two different array devices:

$$K_{METAL\_SKEW} = 0.5$$

If the signals above are switching in opposite directions:

$$K_{METAL\_SKEW} = 0.4$$

For a differential metal path between a differential driver and receiver identically occurring on two different array devices having the same metal length, fan-out and output follower current:

$$K_{METAL\_SKEW} = 0.65$$

5.3.6 Clock Distribution and Clock Pulse Generation

Clock Distribution

In implementing a synchronous design, care must be taken in the distribution of clock signals on-chip to ensure both that the minimum pulse width specifications are met for the latches and flip-flops being clocked and that no possible race conditions exist because of clock skew. The use of differential clock distribution can help minimize skew problems. One possible configuration is the use of a differential input buffer (ECL/PECL input macros C13 & 14) to drive a number of 571 differential receivers which in turn drive the single-ended clock inputs of a number of latches or flip-flops. This configuration is shown in figure 5-7. Skew can be further minimized if the clock distribution is completely differential using differential receiver/drivers such as the H374.

NOTE: Macros which have an internal wired-OR **must not be used** as a part of a clock distribution tree. Such outputs can produce a negative pulse while in the high state under certain switching conditions. The width of such a pulse may be wide enough to cause a flip-flop or latch to erroneously switch.

Clock Pulse Generation

Clock pulses can be generated on-chip by using a delay network built from several gates in series with the final gate in the delay chain inverting the signal. The original clock input signal and the output of the delay chain can be connected to OR gate inputs for clock distribution. A high-to-low transition fed into the network will produce a negative clock pulse whose width is dependent on the propagation delay of the delay network.

To calculate the delay required for the clock pulse generator, the pulse-width shrinkage for the clock distribution network must be calculated as defined in Section 5.5 The minimum pulse width required by the latch or flip-flop is specified for a slow chip in the Macrocell Library for each macro speed/power level.

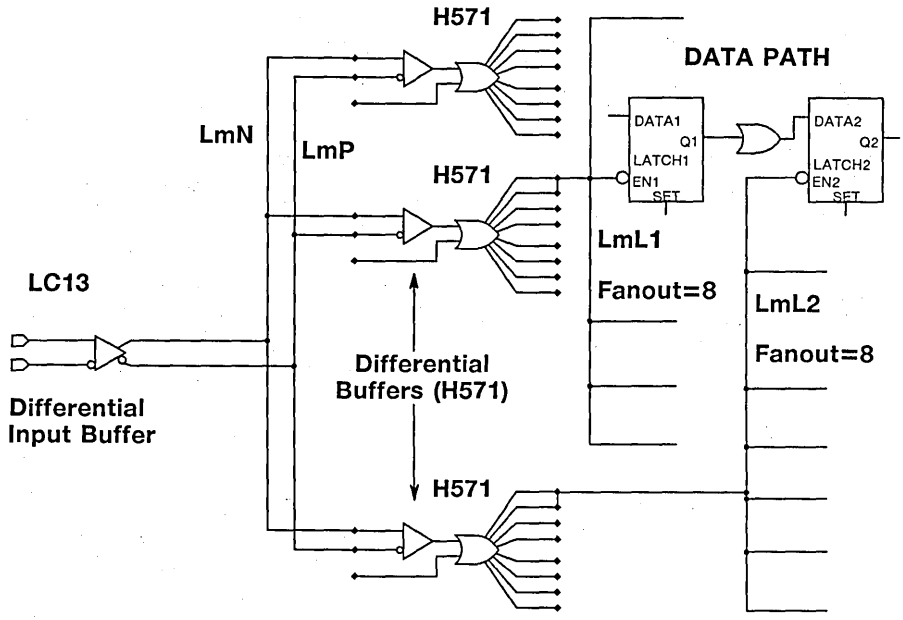


Figure 5–7 Clock Distribution Example

The delay network will automatically compensate for a fast or slow chip. The delay network must be designed to guarantee that a negative pulse width greater than the minimum pulse width specified in the Macrocell Library (e.g.. 1000 ps for L291 in the low power array) appears at the macro clock input. If the chip happens to be faster due to process variations, temperature, etc., then the delay of the delay network will be smaller, but the minimum pulse width required at the latch or flip-flop inputs will also be smaller. If the clock pulse was generated off-chip, the delay network of the external source would have to be designed using the minimum delays for that chip in order to meet the minimum pulse width specifications for the latches and flip-flops on the MCA3 ETL arrays. (The minimum propagation delay rules for MCA3 ETL arrays are specified in Section 5.3.1). It is recommended that clock pulses be generated on-chip. If the clock pulse was generated off-chip, the delay network would have to be designed using minimum delays (Section 5.3.1).

5.3.7 Pulse Width Shrinkage Due to Rise/Fall Delay Skew

In order to ensure that latches and flip-flops in the Macrocell Library operate correctly, the minimum clock pulse width specifications for these macros must be met. Pulses propagating through paths in the array, however, tend to shrink due to the delay differences in the rising edge delays versus the falling edge delays both for the macro delays and the metal and fanout delays. Even if the worst-case rising and falling edge delays are specified the same, pulse width shrinkage can still occur. The following equations give the total pulse width shrinkage due to the driving macro, and the metal and fanout for both negative and positive pulses:

Negative Pulse Width Shrinkage:

$$(1)\ PWS(-) = t_{PD\ MACRO(-)} - 0.8t_{PD\ MACRO(+)} + t_{PD\ METAL/FO(-)} - 0.6t_{PD\ METAL/FO(+)}$$

Positive Pulse Width Shrinkage:

$$(2)\ PWS(+) = t_{PD\ MACRO(+)} - 0.8t_{PD\ MACRO(-)} + t_{PD\ METAL/FO(+)} - 0.6t_{PD\ METAL/FO(-)}$$

where:
$t_{PD\ MACRO(+)}$ = Macro rising delay (from library)
$t_{PD\ MACRO(-)}$ = Macro falling delay (from library)
$t_{PD\ METAL/FO(+)}$ = Metal/Fanout Delay, rising
$t_{PD\ METAL/FO(-)}$ = Metal/Fanout Delay, falling

If an external clock driver is driving the clock input pin, the rise and fall times of the clock driver must be such that the minimum required pulse widths specified in equations (1) and (2) are met. The minimum pulse width that the external clock driver can generate as a function of the rise/fall time and the input fan-in is:

External Clock Driver:

(3) $PW_{min}(DRIVER) = 1.7t_r + 0.1(FI - 1)$

where:
t_r is the 20% to 80% rise or fall time (in ns) at the input and FI is the input fan-in.

Pulse width shrinkage (and stretching) due to skew can be minimized by using pairs of physically adjacent inverting gates with approximately the same fanout and metal lengths.

5.3.8 Pulse Width Shrinkage Due to Narrow Pulses

A short pulse with a small duty cycle (<20%) will tend to shrink as it propagates through an ECL gate because the response time of the circuit may keep the signal from fully reaching the opposite logic state voltage (V_{OH} or V_{OL}). This shrinkage will occur at each gate through which the narrow pulse passes. The designer should note that using a series of inverting gates will not alleviate this type of shrinkage.

The following guideline should be used to estimate additional pulse width shrinkage due to narrow pulse effects:

$K_{NP}=0.0281(W_P/t_{PD\_MAX})+0.694$

for $W_P/t_{PD\_MAX} < 10$

where:
W_p = width of the pulse
t_{PD_MAX} = the maximum delay (either rising or falling edge) of the gate through which the pulse is passing. This number does not include metal/fanout delay since it is accounted for in Section 5.3.7.

$(1 - K_{NP})$ is multiplied by the maximum gate delay, T_{PD_MAX}, to yield the pulse shrinkage. Note that this formula only applies if the width of the pulse is less than 10 times the maximum delay of the gate.

5.3.9 Minimum Pulse Width Specifications

The widths of all internal pulses should satisfy the following criterion after pulse width shrinkage has been taken into account:

$$PW_{MIN} > 2(t_{pd\_max})$$

Internal pulse widths at the clock inputs of all latches and flip-flops should always be kept above the minimum values specified in the Macrocell Library, taking into account pulse width shrinkage (See Sections 5.3.7 and 5.3.8). If the pulse is going to an output pin from an output macro, the pulse at the pin(s), after the pulse width shrinkage is calculated, must be at least 1.6 times the worst-case rise time of the output for single-ended outputs. For differential outputs driving differential receivers, the output pulse width must be greater than 0.8 times the output rise time.

5.4 High Frequency Specifications

This section provides information concerning limitations, macro usage, signal characteristics, guidelines, and application information regarding high frequency signals going on and off MCA3 ETL arrays.

With the introduction of internal and I/O macros capable of operating at frequencies up to 2.6 GHz, the following specifications are provided. To obtain test results which correlate with Motorola, the designer must adhere to specific testing techniques. See the Appendix, Section 10.3, for an MCA3 ETL test setup. The designer should contact **Motorola Bipolar Design Center and Applications Group** for all option designs operating at over 800 MHz to assure system design performance objectives can be met.

5.4.1 MCA3 ETL Maximum Recommended Operating Frequencies

In general, recommended maximum operating frequencies for the arrays are shown in Table 5-9.

TABLE 5-9 Maximum Array Operating Frequencies (Preliminary)

Signal Type		Max. Freq. (MHz) (50% Duty Cycle) Single-ended	Max. Freq. (MHz) (50% Duty Cycle) Differential
ECL/PECL	Input	2600 (1)	2600
	Output	1600	1600
TTL	Input	250	
	Output	100 (@ 15pF)	

Notes:
1. Input Frequencies up to 2.6 GHz can be obtained with a sinusoidal AC coupled single-ended input.

5.4.2 High Frequency Input Macros

For operating at frequencies up to 650 MHz, or 1.0 Gb/s, standard 'C' input macros [C01, C02, and C03] or differential input macros [C05, C13 and C70 (high frequency input buffer)] may be used provided the following guidelines are observed:

1. Differential input signal swing must be at least 250 mV.
2. Single-ended input signal swing for macros C01, C02, and C03 should be at least 550 mV centered around V_{BB} (-1.32 V dc).

At frequencies above 650 MHz, package capacitance, characteristic impedance and die pad capacitance effects cause reduced signal amplitudes at outputs and necessitate increased signal amplitude requirements for inputs.

These effects are a function of the specific I/O macro used, die size, package type, and location of I/O package pin. Figures 5-8 and 5-9 below indicate the required signal amplitude at a given frequency for single-stage and two-stage buffer inputs for the four package types currently offered. A single-stage input refers to the use of an input macro driving an internal macro clock input. A two-stage input refers to the use of an input macro immediately driving a buffer (i.e. L700, L302) or non-select input of a multiplexer (L701) macro.

Single-ended input signals should be biased to V_{BB} (see Figure 10-5) and have amplitudes of twice the differential amplitude plus 40 mV. Non-biased single-ended input signals should swing around V_{BB} (-1.32 V dc) and have amplitudes of twice the differential amplitude plus 120 mV. The graphs in Figures 5-8 and 5-9 are based on the following guidelines:

1. All high frequency inputs should use macro C70 in conjunction with off-chip termination macro E75 (see Figure 10-3). For connection of macro E75, each respective off-chip termination pad, 'VA' of macro E75, must be connected through a 50 ohm off-chip termination resistor to -2.0 V dc. See Appendix, Section 10.4, for further information regarding off-chip termination.
2. The designer carefully selects the pin location of all high frequency inputs such that the shortest length signal lead inside the package is utilized.
   a. PGA - Pins should be selected that are closest to the center of the package and approximately in the middle of the die.
   b. QFP - Pins should be selected that are in the approximate middle of a side on the perimeter of the package.

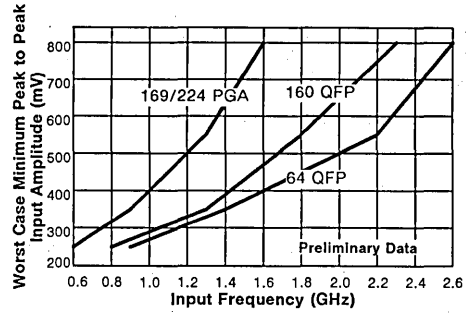


Figure 5-8 Recommended Minimum Differential Input Signal Amplitude for Single-Stage Input Buffer (Macro LC70)

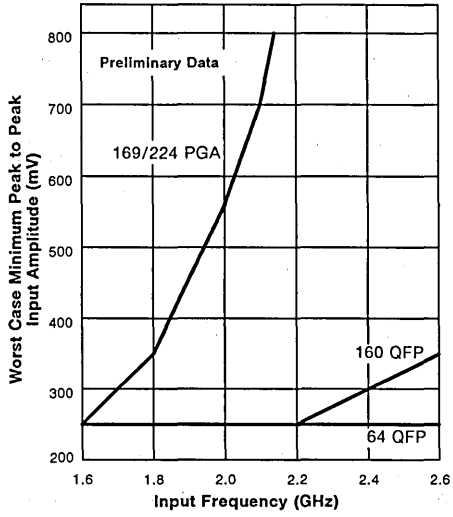


Figure 5-9 Recommended Minimum Differential Input Signal Amplitude for Two-Stage Input Buffer

5.4.3 High Frequency Outputs

The worst-case output signal amplitude versus frequency for the HE70 macro is shown in Figure 5-10. The majority of attenuation is due to the output macro itself rather than the package. Other suggestions for high frequency outputs are:

1. The physical line length of the driven transmission line can be adjusted to allow reflections to increase the output amplitude.
2. Use CML macro HE71 in a 50 ohm transmission line environment. To determine worst-case peak-to-peak output amplitude for HE71 macro, multiply the HE70 macro amplitude for the specific frequency and package as shown in Figure 5-10 by a factor of 0.88. (Computation based on minimum CML specified current of 10.5 ma through 50 ohm termination.) See Appendix, Section 10.4, for an example of using macro E71 at high frequencies.
3. Consult bipolar applications for the latest output macro selections.

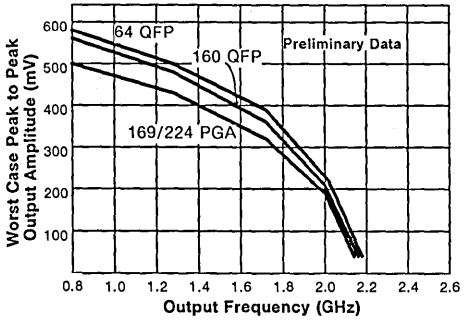


Figure 5-10 Worst-case Output Amplitude for Macro HE70

5.4.4 Bit Rate Versus Frequency

The operating frequency specified above can be related to a bit rate by multiplying the frequency by a factor of 1.6. Therefore, if the frequency specification is 1.6 GHz, this can be translated to 2.56 Gb/s (1.6 X 1.6 GHz).

The reason a direct 2 to 1 translation between frequency and bit rate can not be made is that the frequency specifications are for a 45 to 55% duty cycle. Bit rates will not exhibit this duty cycle and can produce minimum V_{OL} or V_{OH} levels on internal and I/O macros. At high frequencies, a 45 to 55% duty cycle signal may never reach minimum V_{OL} or maximum V_{OH}; therefore, a smaller swing is required to reach the switch point. In general, the 1.6 multiplication factor to determine the bit rate will ensure macro switching for levels at minimum V_{OL} or maximum V_{OH}.

5.4.5 On-chip Operation Above 650 MHz

Signals above 650 MHz may require special macros and differential nets to ensure all requirements are met. Differential flip-flop macros with minimum pulse width of 450 ps (1.11 GHz) are available in several configurations (H372, H375, H376). Macros in the L/H700 series have been designed to operate at high frequencies. Three flip-flops are specified for a minimum pulse width of 300 ps (1.66 GHz). In addition, two high drive flip-flops (L713 and L714) have been designed to operate with a minimum pulse width of 200 ps (2.5 GHz). High drive macros L302, L328, L474, L700, and L701 (combinational logic functions) are also recommended for operating at frequencies over 800 MHz. For additional information and macro availability, have your Motorola sales representative contact the ASIC Bipolar Products and Design Center group.

5.4.6 High Frequency Design Considerations

The following guidelines should be used for high frequency signals:

1. Length of the package leads should be a minimum distance to the die pad.
2. Only package pins which are physically closest to the die pad should be used.
3. Differential I/O macros should be used.
4. The pins connected to the pads adjacent to high frequency inputs and outputs should be connected to ground.
5. Metal lengths on the high-frequency path should be minimized using weighting and/or fixed placement in automatic place and route.
6. The input capacitance due to input metal and fanout should be kept below 0.5 pF.
7. The bandwidth of the macro being driven must satisfy the minimum pulse width requirements at the macro input(s).
8. The setup and hold times for flip-flops and latches should be analyzed, taking into account slow and/or fast skew effects as outlined in Section 5.3.4.

In addition, all internal signals above 400 MHz should preferably be driven **differentially**, from either high drive macros (OEF current = 0.96 mA) or from standard H macros with twinned outputs. The fanout should be limited to half of the maximum DC fanout limits specified in Table 4-2 in order to meet the high frequency rise and fall times. High drive macros can also be twinned (OEF current = 1.92 mA) to provide additional drive capability to satisfy large fanout requirements.

5.5 Differential Calculations

5.5.1 Differential Macro Delay

For pulse width shrinkage and delay skew calculations, the delay due to a differential macro should be calculated as follows:

1. $T_{pd-(YA/YC)} = \frac{2[T_{pd-(YA)}]\,[T_{pd+(YC)}]}{T_{pd-(YA)} + T_{pd+(YC)}}$

2. $T_{pd+(YA/YC)} = \frac{2[T_{pd+(YA)}]\,[T_{pd-(YC)}]}{T_{pd+(YA)} + T_{pd-(YC)}}$

where $T_{pd-(YA/YC)}$ is the macro delay for the signal YA going negative or signal YC going positive. For this example YA = YC. The term $T_{pd-(YA)}$ is the macro delay for output YA going negative.

NOTE: The WACC and OACS based timing simulators do not use the above equations for determining differential macro delays. These simulators use the largest macro delay for either rising or falling edges. The largest macro delay for a rising edge is the larger of YA going positive or YC (the macro compliment output) going negative. Conversely, for the falling edge, the largest macro delay is the larger of YA going negative or YC going positive.

5.5.2 Differential Net Delay

A differential net is a pair of signals that are driven differentially by a single macro and connected only to differential receivers. The switching point for a single-ended signal is the crossing point referenced to V_{BB}, while the switching point for a differential net is at the point where the signals cross. The Motorola CAD system calculates the metal and fanout delay for a differential net using the following equations:

1. $T_{pd-(Y1/Y2)} = \frac{2[T_{pd-(Y1)}]\,[T_{pd+(Y2)}]}{T_{pd-(Y1)} + T_{pd+(Y2)}}$

2. $T_{pd+(Y1/Y2)} = \frac{2[T_{pd+(Y1)}]\,[T_{pd-(Y2)}]}{T_{pd+(Y1)} + T_{pd-(Y2)}}$

where $T_{pd-(Y1/Y2)}$ is the differential metal and fanout delay for signal Y1 going negative or signal Y2 going positive for the differential net composed of signals Y1 and Y2 with the '–' sign denoting the switching direction of the Y1 signal. The term $T_{pd-(Y1)}$ is the single-ended metal and fanout delay for the signal Y1 going negative. The other terms follow similarly.

5.5.3 Differential Pulse Shrinkage Calculations

Pulse width shrinkage is minimized when using differential signal pairs compared with single-ended signals. the following rule applies to a differential net concerning pulse shrinkage:

For a differential net, composed of signals Y1 and Y2, the K factor for matched lines is 0.9 and for the unmatched portion the K factor is 0.8.

The following equations give the total differential pulse width shrinkage for the metal and fanout for unmatched line lengths for the differential pair, Y1 and Y2, where the line length, L1, of signal Y1 is greater than or equal to the line length, L2, of signal Y2.

Negative Differential Pulse Width Shrinkage of Y1 for L1 ≥L2:

1. $PWS\_(Y1/Y2) = T_{pd-(Y1/Y2)} - .8T_{pd+(Y1/Y2)} - \frac{.2[T_{pd-(Y2)}]\,[T_{pd+(Y2)}]}{T_{pd-(Y2)} + T_{pd+(Y2)}}$

Positive Differential Pulse Width Shrinkage of Y1 for L1 ≥L2:

2. $PWS_+(Y1/Y2) = T_{pd+(Y1/Y2)} - .8T_{pd-(Y1/Y2)} - \frac{.2[T_{pd-(Y2)}]\,[T_{pd+(Y2)}]}{T_{pd-(Y2)} + T_{pd+(Y2)}}$

PWS_(Y1/Y2) refers to pulse width shrinkage of the differential pulse from the time Y1 goes negative until the time when Y1 goes positive.

6. Using CAD Tools for Design Development

This section describes the Motorola CAD tools available for designing MCA3 arrays, and it outlines the format of the various files which are required to develop a design option on the Motorola CAD system. Refer to the Motorola CAD Reference For ASIC Design and Release Manual and the OACS Users Guide version 1.2 (and later) for comprehensive information on using the Motorola CAD system.

6.1 Motorola CAD System Overview

Motorola's Open Architecture CAD System (OACS™) supports front end design along with pre- and post-layout timing simulation on Mentor Graphics® engineering workstations. Physical layout (place and route) and timing analysis design tools are supported on Motorola's mainframe CAD system (WACC).

In a typical design flow using the MCA3 OACS tool set (see Figure 6-1), the customer executes the first design phase by developing the schematic (using NetEd™) and performing functional and pre-layout simulations (using QuickSim™) on the workstation. Pre-layout simulations use worst-case macro propagation delays with typical metal lengths per fanout and include worst-case net delays. Motorola then uses the resulting design files to perform physical layout of the circuit on WACC. The post-layout timing files, based on actual wire routing lengths, that originated on WACC are back-annotated to the customer to support QuickSim for final system timing simulations. Design and/or layout iterations are made if necessary. Following a successful post-layout design verification and sign off by the customer, Motorola implements manufacturing the customer's specific ASIC design.

Logic Simulation

The WACC (**LOGCAP™**) logic simulation provides the guaranteed circuit performance for an option. It should be noted that inherent differences exist between the logic simulators on the Mentor workstation (**QUICKSIM™**) and the WACC (**LOGCAP**) systems. For all MCA3 macros, functional models agree between systems for all logic states **that are defined** in truth tables, or equations, in the Macrocell Library and Specification. However, logic states not defined in the truth tables, or equations, for a macro are considered undefined and may not agree between systems. Known inconsistencies may occur on multiplexor, flip-flop, and latch macros.

Therefore, it is recommended that the entire circuit be set to a known state and that the test vector patterns be initiated after all 'X' states have been cleared.

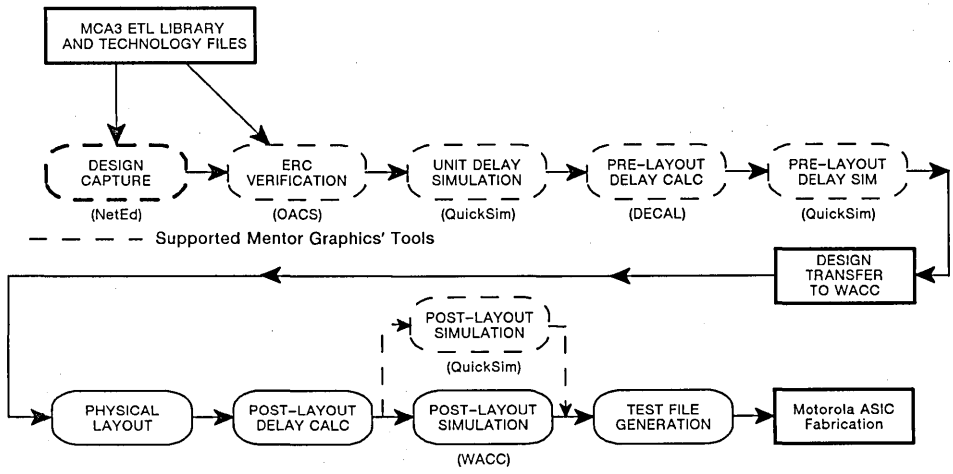


Figure 6-1 Typical MCA3 ETL OACS Originated Design Flow

6.2 MCA3 Option Development Procedure

This section contains step-by-step instructions for developing an MCA3 design option on the Motorola OACS/WACC CAD system outlined above. These instructions describe the various commands and the order in which they are to be executed, and highlight the key decision points along the design development process. For a complete explanation of each command in the Motorola CAD system, the designer should refer to the Motorola CAD Reference For ASIC Design and Release Manual. Refer to the appropriate OACS user's documentation for specific information on schematic capture, simulation, and netlisting.

In the following set of instructions, (OACS) after an instruction indicates that this step is to be executed on an Mentor Graphics workstation using the OACS CAD software. (WACC) indicates that this step is to be performed on the Motorola CAD WACC system. If both (OACS) and (WACC) appear, then this step can be executed on either system. Statements listed in bold and within parentheses indicate the command required to run the OACS or WACC software tool.

1. Create the design directory structure (**CREATE_BLOCK**) and design information file (**DESIGN_INFO**) to simplify the development of a complete design database. (OACS)
2. Enter schematic (**CAPTURE**) with Mentor Graphics design tools NetEd™ and symbol editor SymEd™ using the macrocell library. (OACS)
3. Generate a Mentor Graphics Design Database (**FLATTEN**) through using Mentor tool EXPAND™ (translator) program. (OACS)
4. Produce an EDIF netlist file (**NETLIST**). (OACS)
5. [OPTIONAL] Run an Electrical Rules Check (**ERC**) on the EDIF netlist. The ERC not only performs electrical rule checking, but calculates the cell count and power for the design. (OACS)
6. [OPTIONAL] Perform unit delay simulation (**QSIM**) using the Mentor tool QuickSim™ to prove the design functionality and assist in test vector generation. If there is an error in the design, then repeat steps 2 thru 5. (OACS)
7. [OPTIONAL] Run the program **SIMCAP** to generate unit delay WACC simulator command, test pattern, and simulation response files. These files are respectively named:

   /<option>/layout/scom
   /<option>/vectors/stimulus/spat.unit
   /<option>/vectors/test/tlog.unit

   The above will be produced with the existing data from the design and QUICKSIM files. (OACS)
8. [OPTIONAL] Run **MCA3_DELAY** to calculate the estimated pre-layout metal and fanout delays. This program is the MCA3 version of DECAL. See Section 6.3 for a description of known limitations and incorrect calculations of MCA3_DELAYS. (OACS)
9. [OPTIONAL] Execute **INSERT_DELAYS** to effectively back-annotate the MCA3_DELAY generated timing data into the QuickSim simulator database. (OACS)
10. [OPTIONAL] Perform estimated pre-layout delay simulation (**QSIM**) using the Mentor tool QuickSim. (OACS)
11. [OPTIONAL] Run the program **SIMCAP** to generate pre-layout WACC simulator files. (See step No. 7.) (OACS)
12. Create a SUPERNET netlist and a placement/design parameter FIX file from the EDIF netlist (**EDIF2X**). Make any necessary changes to the FIX file. (OACS)
13. Use the naming convention below and upload the following files to WACC:

WACC	MENTOR
<option> SUPERNET	-- super.net
<option> SPATTERN	-- spat.unit
<option> SCOMMAND	-- scom
<option> TLOG	-- tlog.unit
<option> FIX	-- edif_fix
<option> ACCOMM (optional)	-- N/A
<option> ACPATT (optional)	-- N/A

   ACCOMM and ACPATT are AC simulator command and pattern files respectively. They are required only when functional simulation is completed. These files are not generated from the OACS software. However, ACCOMM and ACPATT files may be generated from SIMCAP by performing a second simulation (with AC test patterns) on QuickSim.
14. Create an SNETWORK file by expanding the SUPERNET file using **SUPERMAC.** (WACC)

15. Run design and simulation check programs **LOGCHK** and **NETCHK.** If errors were encountered during any of the checking programs, the source of the error should be identified. If an error exists in another file, this can be corrected using the XEDIT editor in WACC. (WACC)

16. Prepare your account disk for simulation by running **LOGINIT x,** where x is the number of cylinders of space requested. As a rule of thumb, request at least 10 cylinders for each 2000 vectors.

17. Run **MCASIM** (software simulator) or **SIM** (hardware simulator) both with the AC OPTION to perform a functional simulation with the AC library. Use **SIM** for simulation sequences greater than 5000 vectors. Compare the response file from the WACC simulation to the OACS QuickSim simulation. (WACC)

18. [OPTIONAL] Prepare for AC simulation by running **ACLOGCHK.** (WACC)

19. [OPTIONAL] Run **ACMCASIM** to perform an AC simulation using predicted metal path delays. (WACC)

20. Is the functionality and timing of the design satisfactory? If not, then the design or pattern files should be modified as necessary.

21. Run **AUTOP** to perform automatic placement, which also runs a **VDROP** check. (WACC)

22. [OPTIONAL] If desired, a post-placement, pre-routed net delay file can be back annotated to perform QuickSim delay simulation. See steps 39 thru 42 for directions.

23. Run **AUTOR** to perform automatic routing.

24. Are manual routing modifications either desired or necessary? If not, proceed to step 29. The designer should note that manual routing is rarely required to complete an option.

25. Utilize **MROUTE** with **(IROUTE** option to manually route any "unroutes". (WACC)

26. Depending on the manual routing option selected, execution of the MROUTE program may be required to clean up the routed design file. (WACC)

27. Run net check program **CKNETS.** (WACC)

28. Are there any design violations? If so, go to step 25.

29. Run **IEE** and **VDROP.** (WACC)

30. Were errors encountered while running **VDROP or IEE?** If so, proceed to the next step. If not, skip to step 35.

31. The FIX file may need to be modified if fixed placements or net route weighting have caused the VDROP or IEE errors. After correcting the FIX file (if necessary), return to step 17.

32. [IF REQUIRED] Run **AUXTRACT** to perform physical design changes. (See Motorola CAD Reference Manual for ASIC Design and Release.) If **AUXTRACT** is not executed, skip to step 35. (WACC)

33. Run **AUX2DSF.** (WACC)

34. Run **MROUTE.** (WACC)

35. Run the **METAL** program to extract actual metal lengths from the routed design file. (WACC)

36. Run a post-layout simulation (MCASIM or SIM) to generate the ACDELAY file and perform a delay simulation on the test pattern.

37. [OPTIONAL] Run **ACMCASIM** to perform an AC simulation. (WACC)

38. If modifications to the design are necessary, then edit the design in NETED; produce an EDIF file **(NETLIST)** of the modified design; upload the new SUPERNET file to the Motorola CAD system and go back to step 14.

39. [OPTIONAL] Prepare for QuickSim post-layout actual delay simulation. Use the naming convention below and upload the following files from WACC to the Mentor design database. (OACS)

WACC	MENTOR
▫ ACDELAY	/design/layout/acdelay
▫ SNETWORK	/design/netlist/snetwork

40. [OPTIONAL] Run **MCA3_DELAY** with the Post Layout option to generate QuickSim delay and timing files. (OACS)

41. [OPTIONAL] Execute **INSERT_DELAYS** to generate binary QuickSim delay and timing files. (OACS)

42. [OPTIONAL] Perform final post-layout delay simulation (**QSIM**). (OACS)

43. [OPTIONAL] Run the program SIMCAP to generate post-layout WACC Simulator files. (See step No. 7.) (OACS)

44. [OPTIONAL] Upload the new spat.unit, scom and tlog.xxx files to the WACC.

45. [OPTIONAL] Run a post-layout simulation on WACC and verify the results with the Mentor Graphics QuickSim.

46. Run **TESTCHK**. This program will execute the following programs:

    - RELSE
    - CKNETS
    - CALPREP
    - NETCHK
    - VDROP
    - IEE
    - MCASIM TEST (SYS AC
    - MCASIM (SYS IRACE 10
    - ACMCASIM TEST (SYS
    - ACMCASIM (SYS IRACE 10
    - SENTRY

    Note: **TESTSIM/POSTSIM** may be run instead of **TESTCHK**.

47. If **TESTCHK** was completed successfully, the option is ready for **DSGNCHK**. This utility will check to ensure that all files with the physical definition of the option are in place and will prepare them for release to Motorola.

48. Run **RELTAPE**. This utility will transfer the files to the manufacturing input organization at Motorola.

6.3 MCA3_DELAY (DECAL) Delay Calculation Limitations and Errors

As outlined in Section 6.2, MCA3 Option Development Procedure, estimated pre-layout delays can be calculated on both the Mentor Graphics platform (MCA3_DELAY) as well as the WACC system (MCASIM). These programs both calculate net delays based on the assumption of 30 mils of metal per connection for all arrays except the MCA750ETL where 20 mils per connection is assumed. (Note: In either case, Metal 1 length = Metal 2 length.)

Due to output type recognition and equation limitations, the OACS MCA3_DELAY program may calculate different net delays than the actual pre-layout net delays as calculated on WACC.

In most instances, the net delays calculated by MCA3_DELAY are expected to give the designer an approximate prediction of each net's worst-case delay. Since a homogeneous length of metal per connection is assumed during pre-layout delay calculations, significant differences from the post-layout actual net delays can result due to incorrect metal estimations. The metal added per connection during pre-layout delay calculation has been chosen to over-approximate 70% of the actual post-layout metal lengths.

In general, the following summarizes the percentage differences for net delays calculated with MCA3_DELAY.

1. For nets driven by single outputs:

   a. Rising edge net delays: Error increases from 0 to 10% as net reaches maximum fanout.

   b. Falling edge net delays: Error increases from 0 to a negative 25% as net reaches maximum fanout.

2. For nets driven by twin outputs*:

   a. Rising edge net delays: Error increases from 0 to 25% as net reaches maximum fanout.

   b. Falling edge net delays: Error decreases from 135% to 20% as net reaches maximum fanout. *(Note: Twin outputs are not recognized by MCA3_DELAY and therefore net delays are calculated equivalent to single output driven net delays.)

Other factors that may contribute to differences in net delays are:

1. Twin and Quad buffer outputs driving separate nets: The net delay adjustments as described in Sections 5.2.6 and 5.2.7 are not used for net delay calculations.

2. Differential macro and net delays: The WACC and MCA_3 DELAY simulation programs estimate pre-layout differential net delays based upon slightly variant methods of calculation. The WACC program utilizes the net delay equations described in Section 5.5.2 for estimating differential net delays. The WACC calculated differential net delay is assigned to both complimentary outputs for the nets being driven from the differential macro outputs. MCA3_DELAY calculates the net delays for each complimentary output but does not calculate a differential net delay.

   Both QuickSim and WACC logic simulators calculate the macro delay referenced from the time the last input (either A or B) changes its relative input state to the YA and YC (compliment) output. [i.e. If B switches low to high after A switches from high to low, then calculate macro delay based upon when B switches state. Use macro delay times from the macrocell library propagation delay table for that

macro based from the B input to YA or YC outputs.]

3. Wired-OR configurations: Nets containing wired-ORs are not adjusted for delay degradation as described in Section 5.2.8. In actuality, when several macros are connected in a wired-OR configuration, each macro output may have a different net delay even though all outputs are driving the same net.

4. The delay due to the package and bonding is not included. See Section 5.1.5 to calculate this delay.

5. External degradation due to input capacitance is ignored. See Section 5.1.2 in order to determine this delay.

6. The I/O pin delay due to package and bonding is not added to the output delay. See Section 5.1.5 to determine this delay.

Back-Annotated Net Delay

The post-placement and/or post-layout net delay, as generated on WACC, can be back-annotated into the Mentor Graphics platform for subsequent simulations as described in Section 6.2 steps 38 thru 41. The QuickSim post-layout simulation with the back-annotated net delay information allows the designer to perform an actual delay simulation with the following exception:

1. The largest calculated net delay will be used for a wired-OR net. This limitation exists since each net can only have one delay and a wired-OR is composed of one net. However, each macro driving the wired-OR net may have a different net delay. If all L or all H macros with all single or all twin outputs are used in the wired-or net, this limitation does not exist.

6.4 Description of Files Required by the WACC Simulator

In the previous section, the various files required and how they are produced starting from the OACS framework were discussed. This section will now discuss in detail the following files required by the WACC system:

file name	file type	file mode
<option>	SUPERNET	A
<option>	SPATTERN	A
<option>	SCOMMAND	A
<option>	FIX	A
<option>	ACCOMM	A
<option>	ACPATT	A

<option> is usually the customer chosen 'option' name for his design. Use only columns 1-72 when building these files.

6.4.1 SUPERNET File

The <option> SUPERNET file is a network description in psuedo-LOGCAP format. An example of a partial SUPERNET file created from the OACS EDIF2X tool (Step 8) is shown in Figure 6-2. The top portion of the file contains a list of the inputs and outputs going on and off the chip and statements indicating the wired-ORs in the design. The body of the file lists each macrocell instance in the design and the associated connectivity.

Note that unused input pins on a macro can be represented with an asterisk. Unused outputs are automatically assigned a value DNGLxx representing a dangling output. It is recommended that the designer attaches names to the first output if it is unused, so that they may be easily identified. The Electrical Rules Checking program will issue a warning for all unused outputs. Signal names in the SUPERNET file must conform to LOGCAP format which specifies that the name must be eight or less alphanumeric characters and must start with a letter. No underscores are allowed.

$NETWORK 'option_name' - Identifies this as the network description file and has an optional design name comment field.

$INP 'input_list' and $OUT 'output_list' - All outputs and inputs must be specified in this section. The Motorola CAD system breaks up bi-directional signals into an input and an output, each with a unique name. These two signals, therefore, must appear in the $INP and $OUT statements, respectively.

If more than one line is needed for the signal list, the '&' character is used as a continuation character at the end of each line.

$OR 'out_name' - Identifies a wired-or logic function with zero propagation delay. (See example of correct syntax in Figure 6-2, Example SUPERNET File.

$SUBU 'macro_type' - This statement signifies the start of a connectivity list for a particular macrocell component. See the next section for syntax.

Pin Ordering in the SUPERNET File

The pins for every macro function in the library are in **alphabetical order.** Thus, the signal connected to the 'YA' output of a macro (if it has one) should appear first in the netlist in the line following the $SUBU card, the signal connected to the 'YB' output (if there is one) should appear second, etc. The format of the output/input list for the $SUBU statement is as follows:

$SUBU <macro_name>
<out1> <out2> ... / <in1> <in2>...

where <out1>,<out2>,<in1>,<in2>, etc. are the signal names connected to the macro. These must be in alphabetical order by the pin name on the macro.

Figure 6–2 Example SUPERNET File

```
$$ *** EDIF2X Version 1.02p ***
$$ %DESIGN MC62ETL
$NETWORK
$INP CLK1 IN1 IN2
$OUT QOUT1 OUT2 OUT3
$OR 0 0
WOR1 2 N4 N2
$SUBU HC01
  N1 N2 DNGL0 DNGL1 / CLK1
$SUBU LC03
  N3 N4 N6 = / IN1
$SUBU H291
  FFOUT DNGL3 DNGL4 DNGL5 / N3 * N1 *
        "                   "

$$
$$ END OF SUPERNET FILE
```


Twin Outputs

The output emitter follower current on most internal macro outputs can be set to one of three values – 0.0, 0.48 or 0.96mA (see Figure 2–2). If a single emitter is driving the net, then the output emitter follower current will default to the lower value (0.48 mA). To double the current, one can tie emitters of "twin outputs" together and select twice the default output follower current (0.96 mA in the low power array). Twin outputs are outputs which are logically equivalent. In order to tie two twin outputs together, the same signal must be connected to both outputs in the SUPERNET file. When using twinned outputs, special entries must be made in the $MAMP section of the FIX file to designate the desired current value if two output follower currents are to be connected. No entry in the $MAMP section results in the default value of one output follower current.

In the example SUPERNET file, the two complement outputs, YC and YD, of the LC03 macro instance (11th line of the SUPERNET file) are "twinned" by placing the N6 signal name in the third (YC) position and an equal (=) sign in the fourth (YD) position. The same results can be accomplished by placing the N6 signal name in both the third and fourth positions. If the appropriate entry is made in the $MAMP section of the $FIX file [$MAMP n6 200], then the output emitter current for N6 will be 0.96 mA instead of the default value of 0.48 mA. Otherwise, the CAD system will still attach just one current source pulldown to the net by default thus giving the net an OEF current of 0.48 mA. Each macro entry in the Macrocell Library of Section 9.6 indicates which macros are speed/power programmable. If a given macro has only an 'L' version listed, then only the 'L' prefix can be used on that macrocell.

6.4.2 SPATTERN File

<option> SPATTERN is the file that contains the simulation vectors in a format ready for simulation on the WACC simulator. This pattern can be used for functional (unity delay models) or for AC simulation, before and after place and route. If AC testing is required by the customer, a separate ACPATT pattern file must be generated also. The difference being the ACPATT file is usually much smaller (500 to 1000 test vectors) and requires special statements as to which pins are to be tested and at what test vector it is to be tested.

EXAMPLE: <option> SPATTERN

```
$CYCLE = 10NS
CLK1  ONE 1 3 5 7 9 11 13 15 17 19
IN1   ONE 1 3-7 13-20
IN2   ONE 1-10
```

The following is a brief description of the statements required in the SPATTERN file. For further information, see the Motorola CAD Reference For ASIC Design and Release Document for further information.

$CYCLE = '<cycle time> NS'

This must be the first non-comment line in the pattern file. The CYCLE time must be longer than the longest path in the customer's design.

The following example explains the syntax of the body of the SPATTERN file:

CLK1 ZERO 1 4-6 RPT(110:8-16) 20-END

In this example, the CLK1 input will be low at vectors 1, 4–6, 10, 13, 16, and 20–end of the simulation run. This input will be high the rest of the time. (The RPT construct indicates that the 110 pattern is to be repeated during cycles 8–16.)

Bi-directional signals require a separate line for future test program generation. The format for this line is:

$$* <output_signal_name> <enable_sense> <enable_signal_name>

where:

<output_signal_name> is the net connected to the output port of the Bidirectional macro.

<enable_sense> is the state in which the enable line will enable the output.

<enable_signal_name> is the net connected to the input port of the bidirectional macro.

6.4.3 SCOMMAND File

<option> SCOMMAND is a file containing information as to how many vectors are to be run in a simulation and how the information is to be formatted in the printout. This file has the following format:

```
SIM <option_name>
SWEEP TO <n>
PRINT <node_list>
GO
PRINT <node_list>
GO
EXIT
```

where:

SIM <option_name> - compiles the network file and prepares it for simulation.

SWEEP TO <n> - starts the simulation run at 1 and continues to vector 'n'.

PRINT <node_list> and GO - formats the output of input and output results from simulation. Each PRINT/GO combination will produce a separate output of the simulation results.

The <node_list> is made up of any signal name in the SNETWORK file, including input, output, and internal signals. Blank columns are inserted into the printout by using one or more '/'s and the '&' is used to continue the node_list to the next line. GO signifies the end of the PRINT statement and that it is ready to be printed.

Example SCOMMAND file:

```
SIM
SWEEP TO  50
PRINT CLK1 IN1 IN2 QOUT OUT2
GO
EXIT
```

<option> SLOGLIST is the output of a DO MCASIM simulation and contains the output formatted by the SCOMMAND file and simulated with the vectors supplied in the SPATTERN file. If an engineering workstation is used for functional simulation, this file can be compared to the SIMCAP file tlog.unit generated after running a quicksim simulation.

6.4.4 FIX File

<option> FIX is a file that contains specific information needed to complete the design and simulation. For example, a compatibility statement ($COMPATI) is used to denote that type of logic compatibility (i.e. ECL, ETL, or PECL and TTL). For an OACS based design, a partial FIX file will be generated by EDIF2X. The appropriate properties must be added in the schematic via menus in NETED. These properties are automatically extracted from the expanded design and placed in the EDIF netlist. The EDIF properties are, in turn, used by EDIF2X to produce that part of the FIX file which deals with these design properties. Information such as Package Info, Array Type, etc. is not part of the schematic, but is entered in the design_info program. In Figure 6-3 a sample FIX file is shown. This section includes:

INFORMATION	KEYWORD
Package info (R)	$PKG
Array type (R)	$ARRAYTYPE
Logic Compatibility(R)	$COMPATI
Motorola part number (R)	$OPTIONCODE
Fix macro/pin placement	$FIX
Macro CS Pulldowns	$MAMP
Select Output Slowdown	$SLOW
Place a test diode	$TDIODE
Initial macro placement	$INIT
Net weighting for AUTOR	$WEIGHTS
STECL CS value	$STECL
Pulse and Delay data:	$PULS0
	$PULS1
	$DELAY
	$ACDELAY
	$ACPULS0
	$ACPULS1

(R) = Required

$PKG – This designates to the CAD system which package is to be used for this design. Package codes for the MCA3 ETL arrays are:

224PGA – MCA6200ETL
169PGA – MCA3200ETL
160QFP – MCA3200ETL
64QFP – MCA750ET

$ARRAYTYPE – Designates the particular array to be used. The choices are:

M62LWETL – MCA6200ETL
M32LWETL – MCA3200ETL
M07LWETL – MCA750ETL

Currently, all available arrays are wire bond and based on the low power version of the MCA3 diffusion set.

$COMPATI – This entry indicates the desired logic compatibility for the I/O on the array. One of the entries shown below must be made immediately following the $COMPATI statement:

100K4.5 – ECL 100K/–4.5 V supply
100K5.2 – ECL 100K/–5.2 V supply
100K4.5T – ECL 100K/–4.5 & TTL +5 V Supply
100K5.2T – ECL 100K/–5.2 & TTL +5 V Supply
P100K5T – PECL & TTL +5 V Supply

Consult factory for compatibility availability.

$OPTIONCODE – This is the Motorola supplied part number. You must have this number in the <option> FIX file to complete the design process past uploading the files to WACC. If you do not have a part number, call your Option Development engineer or salesman. The format for this section is:

$OPTIONCODE
MOT <part_number>

$FIX – This section contains the specifications for fixed placement of signal pins and macrocells. The format for fixing macrocells and pins is:

To fix macrocell placement:

<signal_name> <array_cell_location>

where <signal_name> is the name of the signal connected to the "first" output (or "last" input) of the macrocell and <array_cell_location> is the location of the desired cell defined by 3 characters followed by a single letter A, B, C, or D (for orientation of output and major cells).

Macrocell Orientation

Macros which occupy only one quarter cell may be placed in any one of four quadrants (A, B, C, or D) of a cell location. Refer to the floorplans of the arrays in Section 4.3 for the location of each cell and quadrant site for the purpose of fixed placement. The macro orientation identifier is the letter to the right of the cell placement row and column (letter and number, respectively) identifiers. For quarter cell macros, such as H202, the orientation letter indicates the quadrant used. The letter 'A' in cell placement F03A indicates that the marco is physically located in quadrant A.

It should be noted that if one position of a cell location is fixed, then the other unused quadrants of the cell must be fixed. Otherwise, they will be unused by the Auto Placement Program.

Assume the designer wants to fix the location of an H202. To fix this macrocell at a particular location, the <signal_name> will be the signal connected to the YA output pin. The following statement fixes the macro with a YA signal of YA1OUT in row F, column 03 and in the A position (upper left quadrant):

YA1OUT F03A

Note that all column numbers must have two digits (i.e. column 3 is 03).

The following table shows the orientation letter identifier and corresponding quadrant used for single quarter cell macros for a specified fixed placement:

1/4 Cell Macro Orientation Identifier Used	Quadrant
A	A
B	B
C	C
D	D

Macros which use two quarter cells (1/2 cell) can only be placed into the combined A and B quadrants or the C and D quadrant locations. However, the orientation of the circuit layout within the half cell may be positioned via mirror images to accomodate specific I/O routing requirements. The macro orientation identifier 'A' indicates normal 'AB' macro placement; macro orientation identifier 'B' indicates the mirror image or 'BA' placement.

The following table shows the orientation letter identifier and the corresponding quandrant/order (mirror image) used for half cells for a specified fixed placement:

1/2 Cell Macro Orientation Identifier Used	Quadrants/Order
A	AB
B	BA
C	CD
D	DC

Macros which use three quarter cells (3/4 cell) are placed in the A, B, and C quadrants for normal 'A' macro orientation, or in the following quadrants and corresponding order for various mirror images of the circuit layout of the normal placement.

3/4 Cell Macro Orientation Identifier Used	Quadrants/Order
A	ABC
B	BAD
C	CDA
D	DCB

Macros which use a full cell are placed in all four quadrants, and for normal 'A' macro orientation appear in the A, B, C, and D order. The various mirror images of the circuit layout of the normal 'A' placement are indicated via the full cell macro orientation identifier in the table below:

Full Cell Macro Orientation Identifier Used	Quadrants/Order
A	ABCD
B	BADC
C	CDAB
D	DCBA

Fixed Placement of I/O Macros/Pins

Specify the macro signal name and the package pin number cooresponding to the die pad (which is also the U-cell number) where the I/O macro is to be located. The die pad to package pin cross-reference tables in Section 4.3 can be used to determine this information. Placement of the I/O macro in a specific U-cell defines the I/O package pin used. I/O Macros that require two U-cells must be placed in the specifically identified **'paired'** U-cell site locations noted in Tables 4-5 thru 4-8.

Example:

<macro_signal_name> <package pin_#>

clock1 A3

Notes:
(1) Macro signal names for **input** and **output** U-cells are identified by the signal name associated with the **alphabetically last input pad label** for input U-Cells and the **alphabetically first output pad label** for output U-cells. This signal is for identification only. For dual cell input macros, the alphabetically last input will be placed in the site assigned by the user. See the Notes below macro LC70 in the macrocell library for an example.

(2) For the 64 and 160 QFP packages only, package pin numbers from the package pin cross-reference table in Section 4.3 are prefaced with the letter P and number 0, or 00, such that the entry into the **FIX** file is four characters in length. Therfore, package pin No. 1 becomes P001, or package pin No. 26 becomes P026, when entered into the **FIX** file.

$MAMP - The MAMP section is used to place current source pulldowns on the outputs of internal macrocells. By default, every output used internally will have one current source attached, except in the case of "twinned" outputs. If like outputs on the same macro are connected together in the SUPERNET file, only one current source pulldown will be attached to the pair by default. If the designer wishes to double the output pulldown current by using two emitter follower currents, the following entry must be made in the FIX file:

$MAMP
<output_signal_name> 200

If a value of '0' were used in place of the 200, then no current source would be attached to that output. A MAMP value of '0' is used in the case of wired-OR nets to "turn off" the current on some of the outputs because the total current which the net can handle is limited. A $MAMP value of 100 is the default.

$TDIODE – The $TDIODE statement will cause the (–) side of a thermal diode to be attached to the correct die pad for the array used. The (+) side is connected to VCCO.

*$TDIODE2 – The $TDIODE2 statement will cause the CAD system to attach the (–) end of the thermal diode to a die pad. The (+) side of the diode gets automatically connected to the correct die pad. *

* Table 4–3 contains the correct die pads for the TDIODE on each array.

$SLOW – The $SLOW option allows the designer to have a slowdown capacitor attached to an output. Refer to Section 5.1.10 for the timing considerations of using the slowdown capacitor. The format of the $SLOW option is a "$SLOW" statement followed by one or more lines containing output signal names:

$SLOW
<output_signal_name>

$WEIGHTS – This allows the designer to bias the placement of macros connected to certain nets as well as specifying that these nets are to be routed first during automatic routing. This is especially useful for the automatic layout of critical paths. The default weighting for a net is 100%, so a weighting greater than this should be used if it is to be routed first. If nets have the same weighting value, then they are routed in alphabetic order of net names. If no $WEIGHTS are applied to nets, for instance, then all nets will be routed alphabetically by net name. The format is:

$WEIGHTS
<net_name> <weighting_percent>

$STECL – This entry is used to designate the current in the current source pulldowns for STECL outputs. This entry **is also** used to designate the use of current source pulldowns (a.k.a. "STECL Inputs") on input pins. One must observe the rules for placing current source pulldowns on inputs as outlined in Section 4.1. Either 6 or 10 mA current source must be specified for inputs and outputs. For STECL outputs only, the value of the series resistor (0, 27, or 40 ohms) must also be specified. The following syntax is used for specifying STECL inputs and outputs in the FIX file.

$STECL
<input name> [6 or 10]
<output name> [6 or 10] [0, 27, or 40]

$ACPULS0,1 and $ACDELAY cannot be used in final test, and should be used only for debugging or for simulation that will more closely emulate the customers system.

The following is a sample FIX file. (Comments can be added by using '$$' at the beginning of the comment line.) Contact a Motorola Option Development Engineer for specific package codes, array types, and option codes. Note that all data must start in column No. 1 and be entered in upper case.

Figure 6–3 Sample FIX File

```
$PKG
224PGA
$ARRAYTYPE
M62LWETL
$COMPATI
100K4.5T
$OPTIONCODE
MOT 53999HA03
$TDIODE
$$
$$ – DOUBLE THE OEF CURRENT ON N6 –
$$
$MAMP
N6 200
$$
$$ ----- FIX THE PIN PLACEMENTS -----
$$
$FIX
CLK1    B9
IN1     A8
IN2     D9
QOUT    A7
OUT2    B7
OUT3    D8
$$
$$ ----- FIX MACRO PLACEMENTS ------
$$
N1      P14D
N2      P14B
FFOUT   F03A
$$
$WEIGHT
$$
$$  GIVE NET3 A WEIGHTING OF 300%
$$  SO IT WILL BE GIVEN A PREFERRED
$$ PLACEMENT AND WILL BE ROUTED FIRST.
$$  (100% IS THE NOMINAL VALUE)
$$
NET3    300
```

6.5 CAD Layout Considerations

If manual modifications need to be made to the metal routing manually using a graphics interface to the Motorola CAD system, the designer should be aware that certain restrictions exist on the length of metal runs and the placement of VIA's (connections between first and second metal).

6.5.1 Wired–OR Macro Outputs

When outputs are tied together, current will flow from the output that is "high" to the load resistor located at other outputs. This current causes a small IR drop, which decreases the V_{OH} noise margin. Note that the maximum DC fanout restrictions are specified with two values of IR drops: 20 mV or 35 mV. The maximum metal length between any two wired–OR outputs so as not to exceed a 35 mV IR drop for a given OEF current is as follows:

Output Current	Maximum Metal Length
0.48 mA	224 mils
0.96 mA	112 mils

If the maximum allowed IR drop is 20 mV, the following maximum metal lengths apply:

Output Current	Maximum Metal Length
0.48 mA	128 mils
0.96 mA	64 mils

The Motorola CAD system will automatically calculate the voltage drops between two outputs on a wired–OR using a program called VDROP.

6.5.2 Via Placement

The designer should be aware that certain restrictions exist on the placement of VIAs. Adjacent horizontal VIAs are not allowed in the routing channels (i.e. a VIA cannot be placed either directly to the left or to the right of another VIA). This restriction has very little impact on the layout of a circuit. Adjacent diagonal and vertical VIAs are allowed.

6.6 MACH 1000 Hardware Accelerator

Functional and AC simulation may be run on a MACH 1000 hardware accelerator which is tied into the Motorola CAD system. The MACH 1000 is accessed via the use of certain alternate simulation commands. The SIM command may be used in place of MCASIM for functional simulation and the TESTSIM/POSTSIM command serves the same function as TESTCHK. Simulations run on the MACH 1000 generally use much less CPU time than equivalent simulations run on WACC, if over 5,000 vectors are involved.

NOTE: Designs containing **tri–state outputs** currently **can not** be used on the MACH 1000 hardware accelerator. Contact Bipolar Applications for current hardware accelerator capabilities.

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7. Packaging

Primary features of the two Quad Flat Pack (QFP) and two Pin Grid Array (PGA) packages are summarized below. Both the 64 and 160 QFP packages have been designed for optimum high frequency operation by incorporating a strip line characteristic impedance of 50 ohms for the I/O interface. Consult the factory for information concerning the 328 TAB (Tape Automated Bond) version for the MCA6200ETL array. Drawings for each package described below are shown in Figures 7-9, 7-10, 7-11, and 7-12.

64 Pin QFP (MCA750ETL):
- 42 I/O
- 22 power/ground
- Plastic (non-hermetic)
- Die attach heat slug
- Optional heat sink
- JEDEC registration M0094

160 Pin QFP (MCA3200ETL):
- 120 I/O
- 40 power/ground
- Plastic (non-hermetic)
- Die attach heat slug
- Optional heat sink
- JEDEC registration M0108

169 Pin Grid Array (MCA3200ETL):
- 0.100" pin spacing
- 120 I/O
- 49 power/ground
- Multi-layer ceramic (hermetic)
- CuW die attach heat slug
- Wire-bond interconnect
- Ag filled epoxy die attach
- Optional heat sink

224 Pin Grid Array (MCA6200ETL):
- 0.100" pin spacing
- 168 I/O
- 56 power/ground
- Multi-layer ceramic (hermetic)
- CuW die attach heat slug
- Wire-Bond Interconnect
- Ag filled epoxy die attach
- Optional heat sink

7.1 Thermal Characteristics Using Heat Sinks

Θ_{JC}, junction to case thermal coefficient, is typically between 1.8 to 2.2°C/W for the 224 and 169 PGA package. Almost all the heat generated by the device is removed via the CuW heat slug to which the die is attached. Therefore, a heat sink or cold plate should be attached directly to the CuW heat slug in order to effectively remove heat from the package and die.

Given that $\Theta_{JA} = \Theta_{JC} + \Theta_{CA}$, the array must operate in a thermal environment such that Θ_{CA} (the thermal resistance between the package case and ambient air) and T_A (the ambient temperature) are controlled in order to meet the T_J specification for AC performance of 115°C.

The heat sinks currently being offered by Motorola for all ETL packages are composed of black anodized aluminum. For the 224 and 169 PGA packages the heat sink is of the pin-fin type (see Figure 7-4) and for the 64 and 160 QFP is of the circular fin type with a square base (see Figures 7-5 and 7-6). Figure 7-1 shows how the heat sink is mounted directly to the heat slug on the package. The chip is also attached directly to the heat slug using a silver filled epoxy compound in order to provide a low thermal resistance. A 'thermal compound' is used between the heat slug and the heat sink to provide good thermal contact. The aluminum heat sinks were chosen because of their overall thermal performance and low cost.

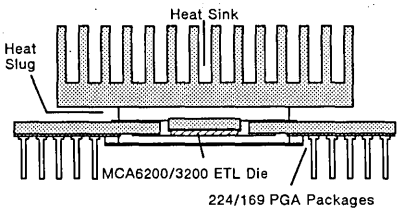

Figure 7-1 Heat Sink Mounted on the 224/169 PGA Packages

Forced Convection Impingement

Forced convection impingement involves forcing ambient air through an opening directly down on the heat sink (see Figure 7-2). The air flow through the pin fins is generally non-laminar. The thermal resistance from the device to the ambient air (Θ_{JA}) depends heavily on the flow rate of the impinged air.

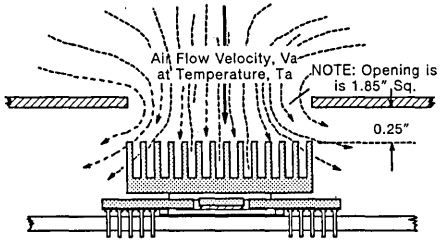

Figure 7-2 Forced Convection Impingement

Forced Convection Horizontal ("Conventional Flow")

Horizontal air flow, or forced convection horizontal is a conventional air flow configuration used in many TTL and lower power ECL environments (see Figure 7-3). Ambient air is blown horizontally (parallel to the plane of the package) over the package and heat sink.

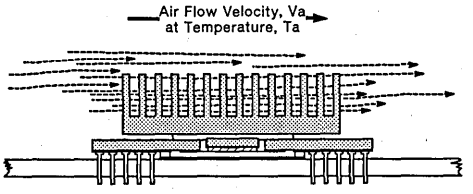

Figure 7-3 Forced Convection Horizontal

7.2 Heat Sinks and Cooling Considerations

The worst case propagation delays in the MCA3 series macro library are specified for a maximum junction temperature of 115°C. The ECL DC I/O logic levels are specified over a junction temperature range of 25 to 115°C for the 100K interface. The TTL DC I/O logic levels are also specified for junction temperatures over a range of 25 to 115°C.

Figure 7-7 shows typical package thermal characteristics as a function of air flow. The curves are based on the 224 and 169 PGA packages with an Aluminum pin-fin heat sink attached (see Figure 7-4). The heat sink was attached using a Hi-thermal conduction adhesive applied approximately 0.004 inch thick on the heat sink. Pressure was applied to remove bubbles and insure proper mating. The adhesive was cured at 150°C for 30 minutes. Figure 7-8 shows the same type of package thermal characteristic curves for the 64 and 160 QFP packages.

The thermal requirements for an MCA3 ETL design will vary according to array size, percent utilization of the array, desired reliability levels, and the mixture of high and low power macrocells within the array. The MCA6200ETL array (7-12 Watts-typical) and the MCA3200ETL array (4-7 Watts-typical) power dissipation for a fully utilized chip requires a heat sink with air flow to meet the maximum junction temperature limit of 115°C for AC specifications. For the MCA750ETL (1-2 Watts-typical), a heat sink may be required depending on ambient temperature and power dissipation.

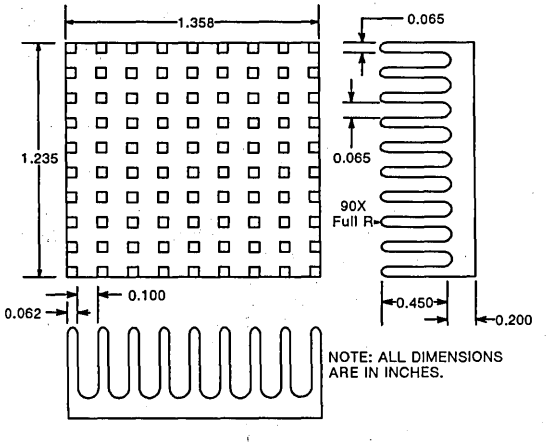

Figure 7-4 Aluminum Pin-Fin Heat Sink for 224/169 PGA Packages (Thermalloy Part No. 2329B)

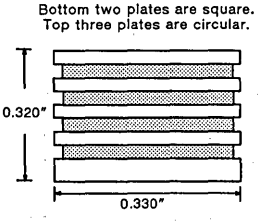

Figure 7-5 Aluminum Circular Fin Heat Sink for 64 QFP Package (Motorola H00809A001)

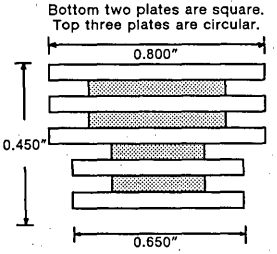

Figure 7-6 Aluminum Circular Fin Heat Sink for 160 QFP Package (Preliminary Drawing)

7.3 Thermal Characteristics

Thermal Resistance

The total thermal resistance of the packaging configuration depends on many variables including parallel heat flow paths other than from the die to the heat sink (e.g. heat may flow from the board itself to the heat sink.) The thermal resistance from the die to the heat sink is composed of thermal resistances for the silicon, epoxy die attach, and the heat sink.

Thermal Calculations

The modest power requirements for the ETL arrays combined with good package thermal characteristics should minimize any thermal problems. Junction temperature can be calculated with the equation:

$$T_J = T_A + P_D \Theta_{JA}$$

where

T_J = Junction temperature
Θ_{JA} = Thermal coefficient (from Figure 7-7)
P_D = Array power dissipation
T_A = Ambient temperature

For example, based on the following list of assumptions, the junction temperature can be calculated as follows:

Assumptions:
224 PGA with heat sink
T_A = 50°C (ambient)
P_D = 11 Watts (die power)
air flow = 500 lfpm

From Figure 7-7, Θ_{JA} = 3.1°C/W
The junction temperature of the device is given by:

$T_J = T_A + P_D\Theta_{JA}$ =
50 + (11)(3.1) = 84.1°C

This number is well below the 115°C specified maximum junction temperature for the array.

64 QFP Thermal Considerations

Based on similar calculations as for the 224 PGA, a 64 QFP dissipating 1.5 watts with no heat sink can be used in ambient temperatures up to 68.5°C before reaching the maximum junction temperature of 115°C. While still dissipating 1.5 watts but with a heat sink and 200 lfpm of air flow, the 64 QFP can be used in ambient temperatures up to 91°C. Dissipating 2.0 watts with a heat sink and 500 lfpm of air flow, the 64 QFP can be used in ambient temperatures up to 94°C.

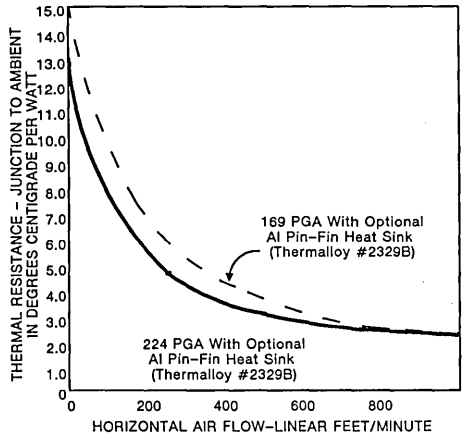

Figure 7-7 Thermal Resistance 169 and 224 PGAs (Typical)

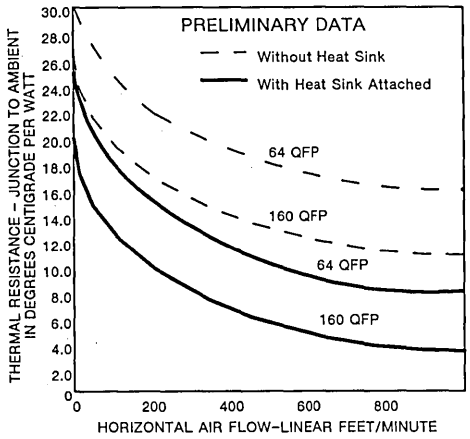

Figure 7-8 Thermal Resistance 64 and 160 QFPs (Typical)

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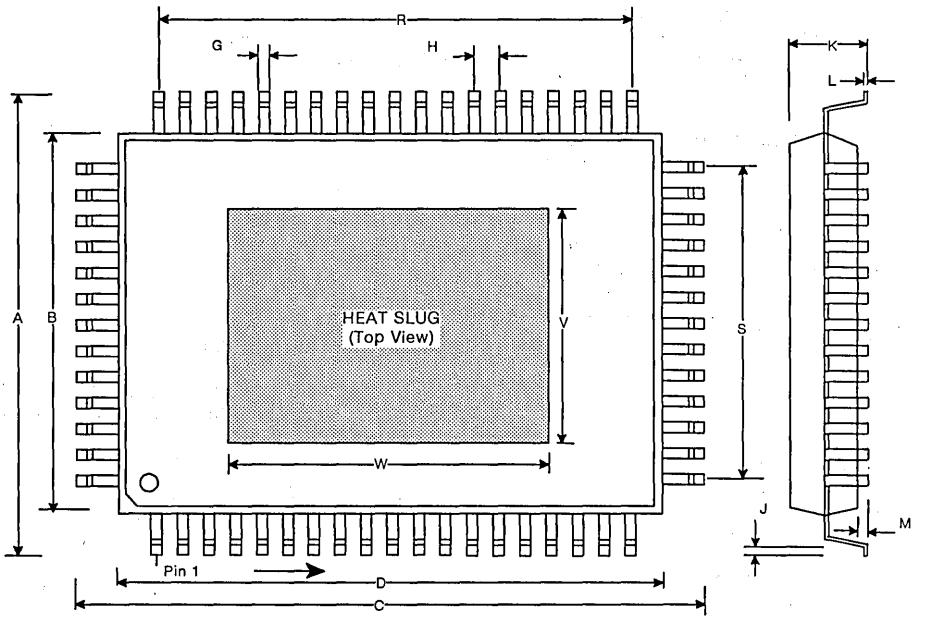

Figure 7–9 MCA750ETL 64 QFP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.10	17.37	0.673	0.684
B	13.90	14.10	0.547	0.555
C	23.10	23.37	0.909	0.921
D	19.90	20.10	0.783	0.791
G	0.381	0.559	0.015	0.022
H	1.000 TYP.		0.039 TYP.	
J	0.75	0.92	0.030	0.036
K	2.85	3.15	0.112	0.124
L	0.10	0.18	0.004	0.007
M	0.25	0.35	0.010	0.012
R	18.0 Ref.		0.709 Ref.	
S	12.0 Ref.		0.472 Ref.	
V	8.8 TYP.		0.346 TYP.	
W	11.5 TYP.		0.453 TYP.	

TABLE 7–1 64 Quad Flat Pack Power Pin Assignments

2	V_{EEE} pins	25	57						
8	V_{CCE}/V_{CCO} pins	26	58						
		10	21	30	42	53	62		
4	V_{CCT} pins	23	28	55	60				
8	V_{EET} pins	22	24	27	29	54	56	59	61

V_{CCO} and V_{CCE} ground planes are electrically connected together in the package and on the die.

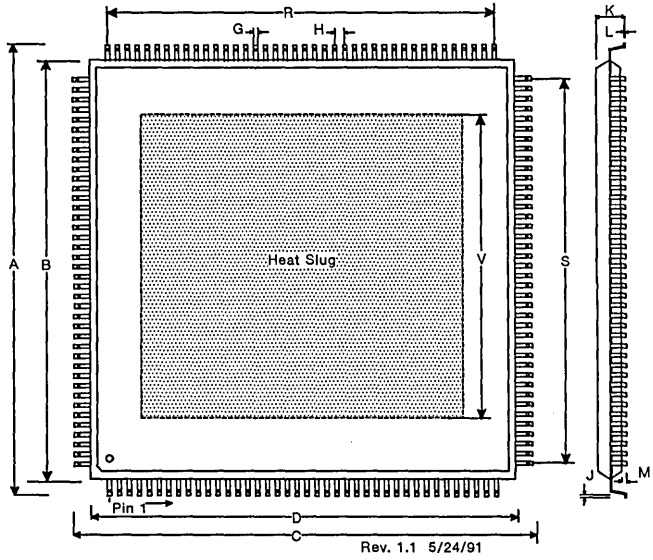

Figure 7–10 MCA3200ETL 160 QFP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.10	31.37	1.224	1.235
B	27.90	28.10	1.098	1.106
C	31.10	31.37	1.224	1.235
D	27.90	28.10	1.098	1.106
G	0.220	0.380	0.009	0.015
H	.650 BSC		0.0256 BSC	
J	0.75	0.92	0.030	0.036
K	3.45	3.85	0.136	0.152
L	0.13	0.18	0.005	0.007
M	0.25	0.35	0.010	0.012
R	25.35 Ref.		0.998 Ref.	
S	25.35 Ref.		0.998 Ref.	
V	16.8 Sq		0.661	

TABLE 7–2 160 Quad Flat Pack Power Pin Assignments

4	V_{EEE} pins	54	67	134	147		
16	V_{CCE}/V_{CCO} pins	14	27	94	107		
		3	20	38	43	60	78
		83	100	118	123	140	158
8	V_{CCT} pins	1	40	41	80	81	120
		121	160				
12	V_{EET} pins	2	21	39	42	61	79
		82	101	119	122	141	159

V_{CCO} and V_{CCE} ground planes are electrically connected together in the package and on the die.

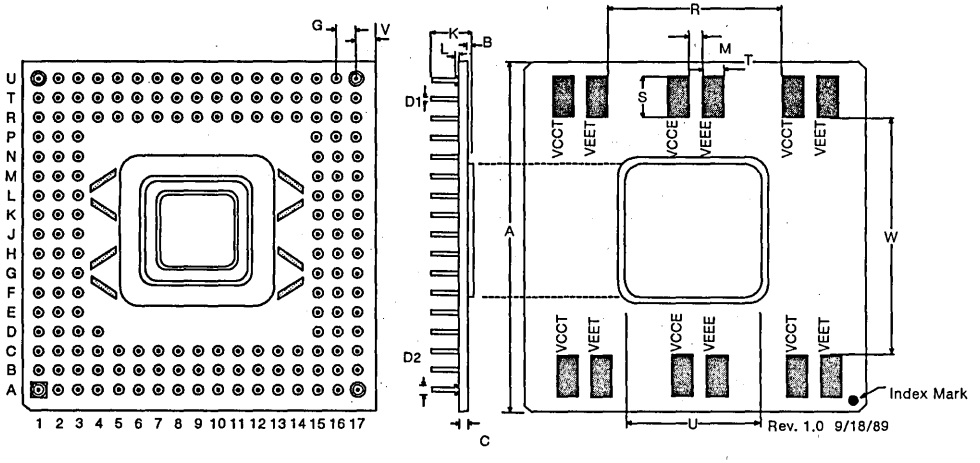

Figure 7–11 MCA3200ETL 169 PGA

DIM	INCHES	TOLERANCE
A	1.760 Sq	±.018
B	0.035	±.005
C	0.110	±.011
D1	0.018 (169X)	±.001
D2	0.050 (4X)	±.005
G	0.100	±.005
K	0.325	±.005
L	0.050	±.005
M	0.040	±.005
R	1.130	±.012
S	0.120	±.005
T	0.060	±.005
V	0.080	±.005
U	0.700	±.009
W	1.420	±.014

7

TABLE 7–3 169–Pin Grid Array (100 mil spacing) Power Pin Assignments

4	V_{EEE} pins	C7	C11	R7	R11	D/A	
4	V_{CCE} pins	G3	G15	L3	L15	S/R	
12	V_{CCO} pins	C6	C10	C12	F3	F15	H3
		K15	M3	M15	R6	R8	R12
8	V_{CCT} pins	C5	C13	E3	E15		
		N3	N15	R5	R13		
21	V_{EET} pins	C3	C4	C8	C9	C14	C15
		D3	D4	D15	H15	J3	J15
		K3	P3	P15	R3	R4	R9
		R10	R14	R15			

V_{CCO} and V_{CCE} are separate planes in the package, but electrically connected together on the die.

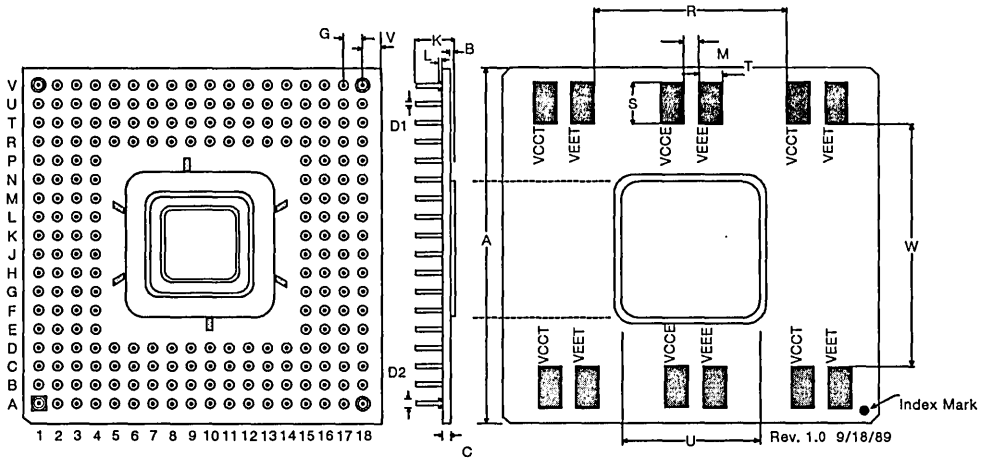

Figure 7–12 MCA6200ETL 224 PGA

DIM	INCHES	TOLERANCE
A	1.860 Sq	±.019
B	0.035	±.005
C	0.110	±.010
D1	0.018 (224X)	±.001
D2	0.050 (4X)	±.005
G	0.100	±.005
K	0.325	±.005
L	0.050	±.005
M	0.040	±.005
R	1.200	±.012
S	0.120	±.005
T	0.060	±.005
V	0.080	±.005
U	0.750	±.008
W	1.520	±.015

TABLE 7–4 224–Pin Grid Array (100 mil spacing) Power Pin Assignments

7	V_{EEE} pins	D7	D12	J4	K15	R7	R12	D/A		
7	V_{CCE} pins	D10	G4	G15	M4	M15	R9	S/R		
16	V_{CCO} pins	A4	A5	A14	A15	D1	D18	E1	V14	V15
		E18	P1	P18	R1	R18	V4	V5		
8	V_{CCT} pins	A1	A18	C1	C18	T1	T18	V1	V18	
20	V_{EET} pins	A2	A3	A9	A10	A16	A17	B1	B18	U1
		U18	J1	J18	K1	K18	V2	V3	V9	V10
		V16	V17							

V_{CCO} and V_{CCE} are separate planes in the package, but electrically connected together on the die.

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8. Design for Testability

As the complexity of IC circuits increases, the problem of testing gets increasingly difficult. The required number of test patterns to do exhaustive testing for a purely combinational circuit with n inputs, is equal to 2^n. For a sequential circuit with n inputs and m state variables (latches), the required number of test vectors is equal to $2^{(n+m)}$. A circuit with 32 inputs and 42 latches would require 2^{74} or 1.9 X 10^{22} patterns for exhaustive testing. At one microsecond per test pattern applied at the tester, it would take more than **one billion years** to test one IC.

There are two major facets of testing problems: test generation and test verification. Test generation is the process of creating stimuli for a circuit to demonstrate its correct functionality. The usual CAD tools that are provided toward this end are usually logic simulators, timing analysis tools and automatic test pattern generators. On the other hand, test verification is the process of proving the effectiveness of a set of test vectors toward correct operation. Fault simulation is a tool that produces a quantitative measure of test effectiveness. Computer execution time for test generation and fault simulation is proportional to the number of logic gates to the power of three. Based on this test approach the costs of testing grow exponentially with increasing complexity. For circuits that incorporate a design for testability (DFT) scheme, the test costs have almost linear characteristics with respect to circuit complexity. These costs and the inability to generate a sufficient test, have led to the implementation of DFT schemes.

If circuits are to be testable, test requirements must influence the design procedure. Testability should be added to the traditional aspects of design: performance, functionality, speed, power consumption and reliability.

8.1 Definition of Testability

Two major concepts pervade all DFT schemes: these are controllability and observability. Controllability is the ability to establish the circuit into a controlled initial state, from which all future states can be predicted. Observability is the ability to observe, through the primary outputs, the internal states and internal signals of a circuit. Several CAD programs have been written which give analytical measures of controllability and observability for all nodes in a circuit. The logic designer can use these measures to determine whether some of the DFT techniques can be applied to the circuit to ease the testing problem.

The ability to generate and to apply test vectors depends on the ease of controlling and observing the values of the internal nodes of the circuits. A node is controllable if the tester is able to control through primary inputs the value of the node to all logic levels (0,1,or high impedance). Certain types of nets should be controllable for maximum testability:

- Clock signals
- Control signals such as PRESET/CLEAR, Tri-State control and ENABLE/HOLD
- Select signals: Data select, Address bus and Data bus

A node is observable if the tester is able to observe through primary outputs the value of the node to all logic levels (0,1,or high impedance). The following types of nets should be made observable if possible:

- Any embedded control signals
- Data lines of storage devices such as flip-flops, counters, shift registers, RAM and ROM
- Global feedback paths.
- Data outputs of combinational logic devices such as encoders, multiplexers, and parity generators

8.2 Design For Testability Approaches

Design For Testability (DFT) techniques involve increasing the controllability and observability of the constituents of a design. All DFT techniques can be categorized to contain one or more of following methods:

8.2.1 Test Points

Test points are defined as poorly controllable and/or poorly observable nodes. Identification of these test points can be achieved either by checklist, as listed in the previous section, and/or by using a software program that computes testability measures. The testability analysis programs attempt to quantify a testability measure of an arbitrary design that is designed with no consideration for testability.

Once test points are identified, the next step is to modify the basic design by providing a logical access to these test points through primary inputs and primary outputs. With the limitations in the number of primary inputs or outputs, addition of control logic such as decoders, multiplexers and shift registers can be used to provide additional test points. The above mentioned control nodes and observation nodes are good candidates as test points.

An example is shown in Figures 8-1 and 8-2. The inputs of the embedded block B are difficult to control and the outputs of block B are difficult to observe. The multiplexers at the inputs provide direct control to the embedded block B. The decoders at the outputs provide observability of the embedded block B.

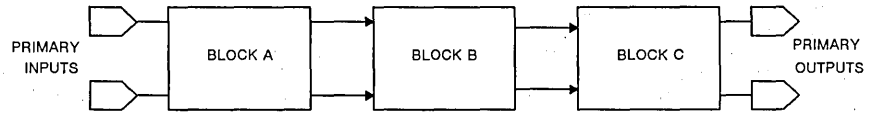

Figure 8-1 Network Partitioned Into Three Subnetworks

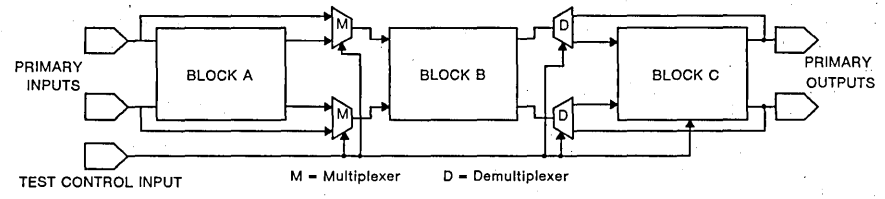

Figure 8-2 Direct Access For Testability Improvement

8.2.2 Partitioning

An increase in circuit complexity of VLSI chips and higher level of integration results in an increase of testing difficulty. Since the testing time of a circuit is related to the cube of its complexity, it is intuitive to divide and conquer by testing complex circuit parts as a whole. For example, testing one half of a circuit takes one-eighth of the time required to test the whole circuit. Partitioning increases the observability or controllability of the constituents of a design by decomposing the overall design into more manageable elements for test purposes. Some of the partitioning techniques proposed are:

1) "Natural Partitioning" found by analysis of system blocks in VLSI designs and availability of design methodologies such as standard cells and silicon generators that include supercells such as RAM, ROM and microprocessor core.

An advantage of system block partitioning is the ability to reuse test programs developed for common block types. Use of multiplexers and demultiplexers on pins, as shown in Figures 8-1 and 8-2, creates direct access to block B. As a result, the test program that was developed for block B can be applied directly.

2) "Partitioning created by adding DFT structures". DFT techniques such as scan path and LSSD structures partition the circuit into one or more shift registers and a collection of purely combinational logic that is easier to test.

3) "Partitioning by bus architecture". Bus architecture provides visibility to and from circuit elements that are tied to the bus. To take advantage of this approach, the bus must be accessible to the primary inputs and outputs. An internal ROM connected to the bus can be verified by reading its contents onto the bus and externally comparing the value to a correct copy of the ROM.

8.2.3 Scan Design

Scan design techniques connect the state storing elements (does not include RAM and ROM) into one or more shift registers that provide the ability to scan data into and out of the circuit. This capability provides access, that has total observability and controllability, to the state of the circuit. Access to the data can be accomplished in two ways. The first access method uses serial scan through the shift register.

Random access scan is the second method which uses an addressing technique that allows each storage element to be individually and randomly selected. The design and manufacturing costs associated with serial scan are primarily influenced by a 5% to 25% cost increase in silicon area overhead. There is a resultant performance impact using a serial scan technique. There are several different versions of scan design techniques that are

being used in the industry. Some of those techniques are:

1) Level Sensitive Scan Design (LSSD)

LSSD is a serial scan DFT approach that uses latches for memory elements. To ensure race-free system operation and testing, the LSSD technique is based on the following concepts:

- Logic design is implemented in accordance to a set of rules that are outlined in reference (4). As a result, correct operations of the circuit is insensitive to AC characteristics such as rise time, fall time, and minimum delays of an individual gate.
- The basic memory element must be a level sensitive latch that is hazard-free and race-free. This latch has additional gates that are used to chain such latches into a shift register. An example of a shift register latch (SRL) is shown if Figure 8-3. An SRL is composed of two latches L1 and L2. L1 is generally used to store normal data, while L2 is used for shift register linkage as shown in Figure 8-4. Non-overlapping clocks are used for shifting clock signals A and B. The L2 latch can be used by the designer for other circuit functions and thus minimize silicon area overhead.

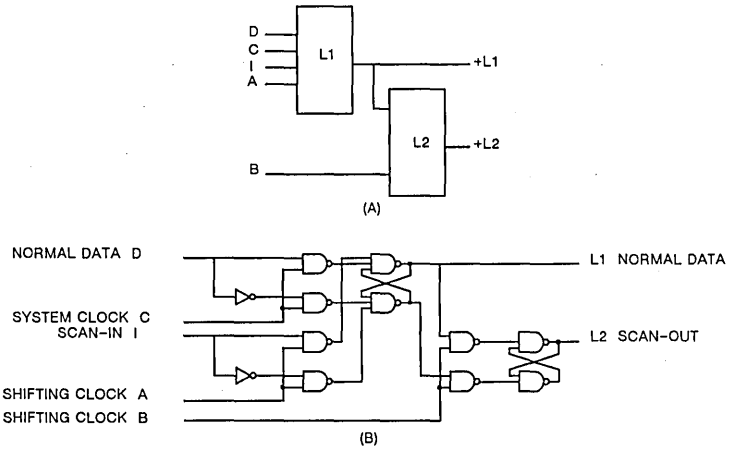

Figure 8-3 Shift Register Latch, (A) Symbolic Representation, (B) NAND Gate Implementation

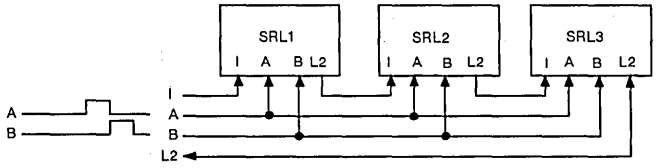

Figure 8-4 Linking Several SRL's

2) Scan Path

Scan path design technique uses the same design methodology as LSSD but does not use level-sensitive memory elements. Scan path uses only one system clock and the technique could be exposed to race conditions. This exposure can be easily minimized by using careful design rules regarding synchronous operations.

As shown in Figure 8-5, a two-to-one multiplexer can be added at each data input of a memory element (e.g.. edge-triggered D flip-flop, and master-slave D flip flop). The result is an equivalent of an SRL with one clock. Similar methods can be applied to other types of memory elements, such as the J-K flip flop.

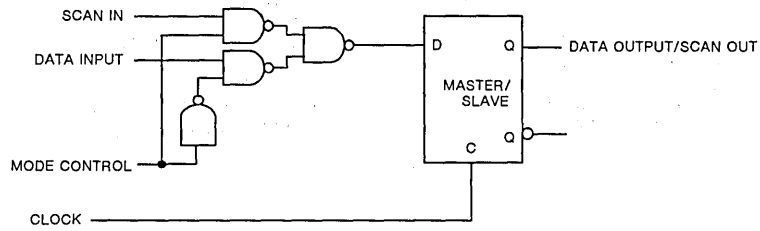

Figure 8-5 D-Type Master-Slave Flipflop With Scan Capability

To implement the scan path technique, each memory element in a circuit should be modified by replacing each regular memory element with a data-multiplexed storage element. Scan path design rule checking should be applied to the modified circuit to ensure correct scan design techniques and race-free operation. An example is shown in Figures 8-6 & 8-7.

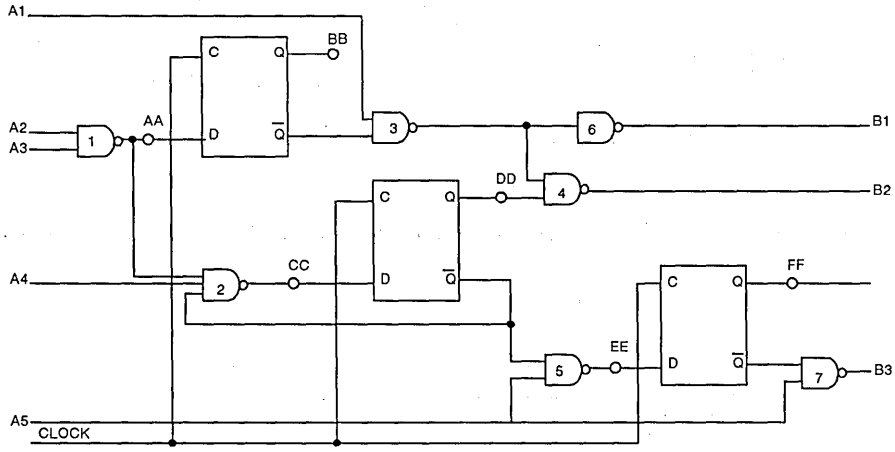

Figure 8-6 Sequential Network With a Sequential Depth

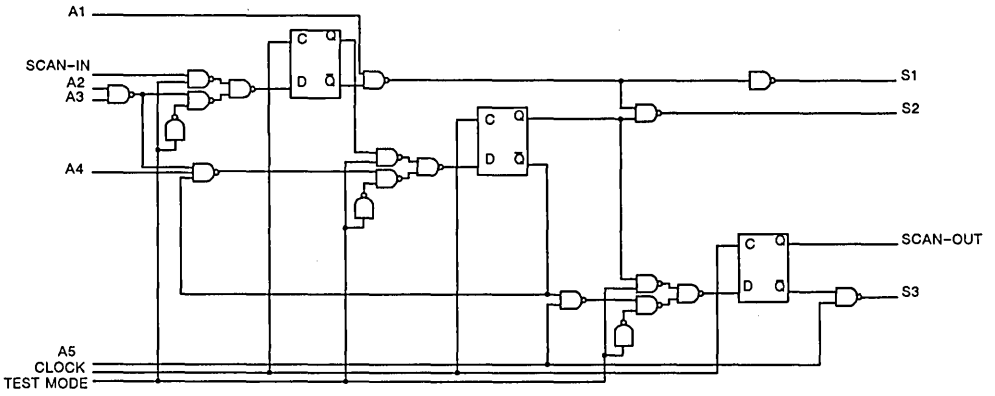

Figure 8–7 Sequential Network With Complete Scan Path

8.2.4 Self Test

Built in self-test (BIST) uses tools and techniques in the design and the implementation process to give a chip the ability to test itself. Figure 8–8 shows a general approach to BIST. There are four general resources that can be included on the chip. The two basic resources are:

1) Test Pattern Generators (TPG).

TPG's are used to provide stimuli to the circuit under the control of the TPG Supervisor. For a large circuit, partitioning will provide smaller silicon overhead for TPG implementation. The following are examples of TPG's:

- Counters: Provide somewhat deterministic stimuli
- ROM: Can store a limited number of deterministic stimuli
- Linear Feedback Shift Register (LFSR): Generates a psuedo-random sequence of stimulus vectors. It allows a large number of stimuli to be generated and applied to a circuit without requiring a large silicon area to store them. A large number of randomly generated patterns are required to achieve a given fault coverage.

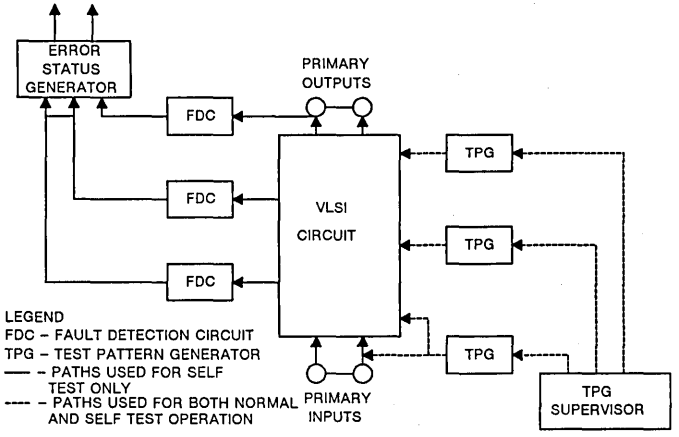

Figure 8–8 General Self Test Approach

2) Fault Detection Circuit (FDC)

FDC detects faults in the circuit and feeds them into the error status generator for analysis. Examples of FDC are:

- ROM can be used to store test results and with a comparator, fault detection can be accomplished.
- LFSR is used as a data compressor that develops a compressed syndrome of test results. This syndrome (or signature) can then be compared by the error status generator to a stored value. A multiple input implementation of LFSR, called multiple input signature register (MISR), is shown in Figure 8-9.

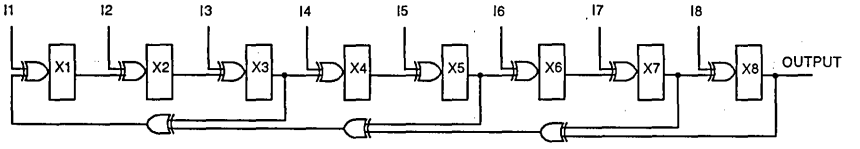

Figure 8-9 Multiple Input Signature Register

By adding a few gates to an LFSR a multifunctional register is obtained. One implementation is shown in Figure 8-10.

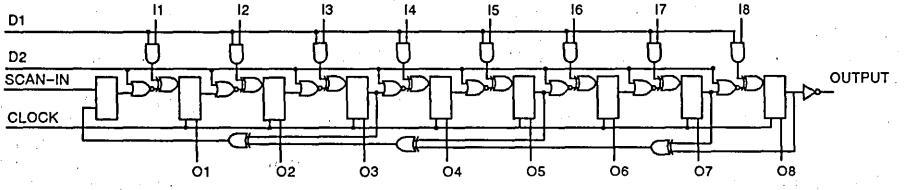

Figure 8-10 A Multifunctional Register

8.3 General Guidelines For Testability

Observability:

Design using dedicated test pins to monitor critical nodes of the circuit. If no dedicated test pins can be made available, it may be possible to replace some output buffers with bi-directional buffers and use the newly created inputs as test inputs. The same method may be used with input buffers to create test outputs. Also, output pins may be multiplexed between normal circuit functioning and test-circuit functioning.

As a last resort, when the above methods can not be used, it may be possible to use the normal circuit inputs for testing. This is done by using input logic combinations that will not occur under normal circuit operation and internally decoding them as test modes.

Use test pins to exercise the I/O buffers independently of the internal logic where possible. Design using dedicated test logic to provide and control such functions as reset, tri-state output enable, preset, data-bus enable, or other means of initializing and controlling the states of the logic. Do not design flip-flops, registers, latches, and counters to which there is no access for initialization. Partition large circuits into smaller, more manageable circuits that will allow the use of control and test logic.

Design using synchronous logic. Asynchronous designs can exhibit race conditions that vary as IC processing varies and may not appear on CAD simulations. Do not allow any unclocked feedback paths, such as those found in ring oscillators.

Use care when designing a circuit that depends upon internal propagation delays for timing. Always take internal skews into account to avoid race-conditions.

Avoid race conditions to cells (such as between data and clock, set and clock, reset and clock, preset and clock, or preset data and preset enable).

During functional and ac simulation, observe several internal nodes, to insure that the circuit is functioning as desired.

To avoid long counting sequences during simulation and testing, design counters so that

they are broken up, with each section separately presettable. This allows simulation and test steps (vectors) to be used for simulation and testing, not for counting.

One important simulation function is to insure that the device can be tested by both wafer-probe and final-test equipment. Race conditions may exist not only because of design flaws, but also because of IC tester limitations. Ideally, a test system would simultaneously apply all input test vectors and later compare circuit outputs with simulation results. IC testers for cell arrays can have skew between needle points (bonding pads) at wafer probe. For this reason, a circuit that simulates properly and is designed for proper flip-flop setup and hold times can fail at wafer probe or final test. Designers should be aware of the possibility of tester race conditions and should define test vectors accordingly.

When specifying timing relations, try to allow enough margin to take into account the possible skew of the tester. When using more than one clock, design for worst-case skewing between clocks. To avoid skewing problems, do not change any input signal to a clocked cell on the active clock edge. If a positive hold time is present on the latch or flop, then the data must be held for the appropriate length of time after the clock edge.

Simulation (and test) vectors may be different from the input sequence of the actual system application. Initialize all storage elements at the beginning of the simulation (and test) sequences. Do not clock a cell and change the data on the same vector. Do not clock cells or change data on the same vector that a reset is applied or an enable signal is removed. There may not have been sufficient recovery time, and the new data may not get clocked in. Unpredictable simulation results may occur.

Within simulators, it is possible to initialize any or all storage elements in the design by using initialization commands. IC testers do not have this automatic initialization capability. In actual operation, when powered up, the storage elements can be in either a set or a reset state, and this power-up state can change from circuit to circuit. A simulation test pattern that depends upon storage elements being initialized upon power-up will almost certainly fail actual test at wafer probe or final test. Initialization should be accomplished by signals on the set or reset inputs, or by clocking in known data.

Do not design using flip-flops models that self-initialize. Otherwise, have the circuit provide the logic necessary to put the output into a desired state. Problems arise because the tester is not able to do the same initialization procedure as encountered during normal circuit operation.

REFERENCES

1. Goldstein, L.H., "Controllability/ Observability Analysis of Digital Circuits". IEEE Trans. Circuits and Systems, Vol. CAS-26, No. 9, September 1979, pp 685-693.
2. Kojivanic, P.G., "Testability Analysis", IEEE Test Conference, 1979, pp 310-316.
3. Dussalt, J.A., "A Testability Measure", IEEE Test Conference, 1978, pp 113-116.
4. Eichelberger, E.B and Williams, T.W. "A Logic Design Structure For LSI Testability", Journal of Design Automation and Fault Tolerant computing, Vol. 2 No. 2, May 1978, pp. 165-178.
5. Bennetts, R. G., Design of Testable Logic Structures, Addison-Wesley, 1984.
6. Williams, T. W., et al, "Design for Testability - A Survey," IEEE Transactions on Computers, January 1983, Vol C31, No.1.

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9. The Macrocell Library and Specification

9.1 Macrocell Array Logic Type Classifications

ETL macrocells are listed in numerical order in a table in the front of this manual, and listed by function prior to the Macrocell Library in this section. The macro identification number is prefaced by an 'L' or 'H' to indicate low or high power version availability. A preface of 'L/H' indicates both power versions are available. The Macrocell Library consists of the following groups of macrocell functions:

1. **Internal Macrocells** (L/Hxxx)
   Internal macrocells (identified by a three digit number after L or H) can be placed anywhere in the internal portion of the array. These macro functions are sometimes referred to as M-cells. Each internal quarter cell (1/4 of an M-cell) contains 19 resistors and 19 transistors. A quarter cell is the minimum addressable unit (MAU) of the internal array. These components are connected together on first layer metal to form logic functions. The internal macrocells can use 1/4, 1/2, 3/4, or 1 entire M-cell to implant a specific logic function.

2. **ECL/PECL Input Macrocells** (L/HCxx)
   Input macro functions (identified by a C after L or H, then followed by two digits) can be placed in any of the U-cell locations on the periphery of the array. These macrocells are used for interfacing with ECL 100K external levels and PECL (+5.0 V ECL), driving lower level inputs from off-chip, and for input buffering. Differential input buffers, as well as, direct pad to internal cell connections can be implemented.

3. **ETL/PETL Translator Macrocells** (L/HTxx and L/HPxx macros)
   These macros (identified by a T or P after L or H) consist of input and output translators which can be placed in U-cell locations on the periphery of the array. 'T' macrocells are for translating TTL to ECL levels for on-chip use or ECL to TTL signals when going off-chip. Macro T90 is a tri-state control macro which is used to translate ECL on chip signals to levels required by the control line 'CT' inputs of TTL output tri-state control macros (T31 and T60). Macro T90 requires one U-cell and therefore the corresponding I/O pad can not be used. 'P' macrocells are similar in function but convert signals to/from PECL (+5 V ECL) operation.

4. **ECL/PECL Output Driver Macrocells** (L/HExx and ZExx macros)
   Output driver macrocells (identified by E or ZE after L or H) are used as an interface from the internal macrocells to the bonding pads. Signal levels may be ECL 100K and PECL (+5.0 V ECL). An output macrocell occupying a single U-cell has the logic capability similar to that of an internal macro in a quarter cell.

5. **ECL, TTL and PECL Bidirectional I/O Macrocells** (L/HBxx, L/HTxx, L/HPxx)
   Bidirectional macrocells (identified by B, T, or P after L or H) are available for placement in U-cells. These macros can be used for supplying ECL, TTL, or PECL levels to output pads while using the same pad for ECL, TTL, or PECL inputs respectively. A variety of logic functions are symbolically represented in the Macrocell Library.

9.2 How to Read the Macro Symbols

Figure 9-1 shows an example of a macrocell symbol in the library indicating the various symbol properties (e.g. DC input loading, input levels, etc.) which are shown in the Macrocell Library. The following macrocell attributes are defined on each symbol:

9.2.1 Input and Output Signal Names

1. Single letter (A,B,C,etc.) = ECL inputs.
2. EI = ECL/PECL input from package pin.
3. FI = ECL/PECL input from package pin (used on differential inputs only).
4. TI = TTL input from package pin.
5. CT = signal from tri-state control macro output (TA) only.
6. Internal macros (M-cell) with inputs or outputs beginning with a 'W' are one diode drop below the standard internal level. *
7. Outputs beginning with a 'Y' are standard internal level ECL signals.
8. Outputs beginning with an 'R' have resistive output follower pulldowns. **
9. Outputs beginning with an 'N' are internally twinned. **
10. CO = ECL/PECL output to package pin.
11. DO = ECL/PECL output to package pin (used on differential outputs only).
12. WA = TTL output to package pin.
13. CB = ECL/PECL bidirectional signal to package pin.
14. TB = TTL bidirectional signal to package pin.

* See Section 4.2 Internal Connection Rules.
** No wired-OR configurations are allowed.

9.2.2 DC Input Loading – Internal and I/O Macrocells

For all macros, i.e. internal M-cells and I/O U-cells, numbers in parentheses ( ) in front of the input name [e.g. (2,3) *D] indicate the DC loading factors (low and high power) for that specific input. If a number is **not present in parentheses** ( ) in front of the input, the loading factor for that input is the **default value** which **equals** (1). The sum of the number of DC loads indicated for specific inputs on a net is used in conjunction with Table 4-2 to verify that the total maximum DC fanout for the **macro driving the net** is not exceeded.

For internal M-cells only, **upper level** inputs (indicated by the absence of either an * or a # sign in front of the input name) must have their indicated DC loading factor **doubled if the high power version** (H) of the macro is being used. If no number appears in front of an **upper level** input, the default value of 1 is doubled to 2 for the H macro.

For output macrocells only, the numbers in parentheses indicate the **actual** number of DC loads, and these values **should not** be doubled for H macros. If only one number is shown in parentheses, that number indicates the number of DC loads for that input for either the L or H macro version shown in the Macrocell Library.

If two numbers appear in parentheses ( ), the first number is the loading factor for the low power macro [e.g. (2) for input *D per example above] and the second number [e.g. (3) for input *D per example above] is the loading factor for the high power macro.

Throughout the Macrocell Library, an '*' in front of an input name (e.g. *D) indicates that it is a second level input. A '#' sign in front of an input name indicates that the input is a third level input. Both second level and third level inputs are considered **lower level** inputs for calculation of input capacitance (see Table 5-7).

MACRO: 424 6-INPUT EXNOR

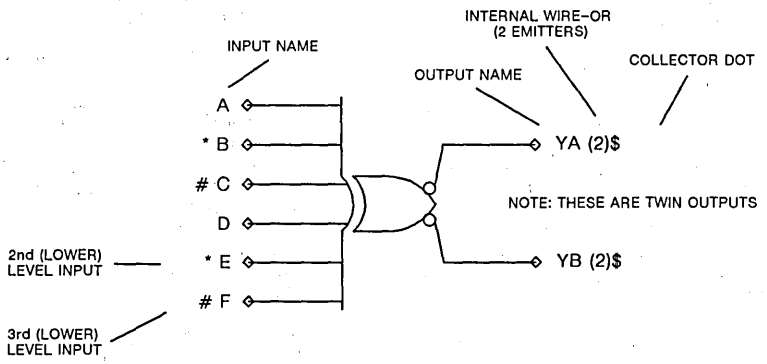

Figure 9-1 Macro Symbol Example

SYMBOL NOTES: If an input does not have an '*' or a '#', then it is considered an **upper level** input. DC loading (fan-in) on inputs is shown in parentheses, if it differs from the default value of 1. For internal M-cells only, the DC loading values for **upper level** inputs must be doubled if the high power (H) version of the macro is used. Note that the default fan-in value for an **upper level** input of an H macro is 2.

9.2.3 AC Input Loading – Internal and Input Macrocells

The AC capacitive loading of an input is a function of both the level (**upper/lower**) and the number of **low power** (L macro) DC loads. The L macro DC loading factor (first number in parentheses) in front of an input also represents the number of AC loads, unless a separate AC load table is provided for the specific macro/input combination. Separate AC load tables are provided when an input is internally connected to more than one input level, or it is connected to inputs on complementary sides of the same current switch such as in XOR

macrocells. The AC loads for each input on a net are in turn multiplied by the capacitance per unit load given in Table 5-7. The resulting values are inserted in the rising and falling edge metal/fanout delay equations in Section 5.2.2. Table 9-1 below summarizes the DC and AC load information provided in this and the preceding paragraph for internal macro 286. Refer to macro 286 on page 9-25 in the Macrocell Library in conjunction with Table 5-7 to verify the information provided in Table 9-1.

NOTE: It should be noted that the AC loading tables are not used by the WACC CAD simulation software. For macros with both upper and lower level AC load values, the AC capacitance differs slightly from that calculated by WACC. All AC propagation delays calculated by the WACC CAD system are the worst case specified delays and are guaranteed by AC testing.

9.2.4 AC Input Loading – Ouput Macrocells

The rules for deriving the AC input loading for output macrocell inputs are different than those for calculating the AC loading for internal macrocells.

Although the DC loading numbers in the internal cell library also represent AC loads in most cases, the DC loading factors in the output macrocell sections are based on the number of unit base current loads which the input draws. These numbers do not reflect the number of devices to which the input is connected internally. If the input represents **more than one AC unit load**, then a separate AC loading table will be shown with the macro. The unit capacitances for output macrocell inputs are listed in Table 5-7.

9.2.5 Upper and Lower Level Inputs

Inputs to the top level of a series-gated current switch are called **upper level** inputs. If an input name does not have an asterisk '*' or a pound sign '#' beside it, and does not appear in the AC loading table for that macro, then it is an upper level input. Inputs to the second level of a series-gated current switch are marked with an asterisk '*' and third level inputs are marked with a pound sign '#'. Both second and third level inputs are referred to as **lower level** inputs. Note that except for the case of input pads driving internal cells directly, upper and lower level inputs are not functionally different. The primary difference between the two levels is in operating speed, and in calculating AC and DC capacitive loading (see Table 5-7).

9.2.6 RESET and SET Input Considerations for Flip-flop and Latch Macros

The reset and/or set inputs of flip-flop and latch macros that are marked with an '*' should be treated as **upper level** inputs for **AC and DC fan-in considerations only.** The numbers in parentheses ( ) in front of these '*' designated inputs further clarify the DC input loading factors as explained in Section 9.2.2. These reset and set inputs are designated with an '*' to signify that they **may not** be directly connected to external input pads. These inputs follow the I/O connection rules for second level inputs. These reset and/or set '*' inputs must be driven by YA, YB, etc. outputs from interface or internal macros.

TABLE 9-1 MACRO: 286 – DC Load and AC Input Capacitance Summary

INPUT NAME	NUMBER OF DC LOADS				NUMBER OF AC LOADS		NiCi (pF)	
	L Macro		H Macro		L or H Macro		L Macro	H Macro
Level	Upper	Lower	Upper	Lower	Upper	Lower		
(2,3) *A		2		3	1	1	.12	.14
(2,3) *B		2		3	1	1	.12	.14
(2) C	2		4		2		.14	.18
(2) D	2		4		2		.14	.18
*E		1		1		1	.05	.05
*F		1		1		1	.05	.05

NOTES: Values of Ci for calculating the NiCi for a specific input are obtained from Table 5- 7. For Upper Level inputs, Ci = 0.07 pF for L macros and Ci = 0.09 pF for H macros. For Lower Level inputs Ci = 0.05pF for both L and H macros. The number of Upper or Lower level inputs for input names *A and *B are obtained from the AC load table below macro 286 on page 9-25.

9.3 Propagation Delay and Power Dissipation

Macro propagation delays given in the library are for worst-case as specified for V_{EEE} =-5.2 V ± 8% or V_{EEE} = -4.5 ± 0.3 V (dependingon option compatibility), V_{cct} = 4.75 to 5.25 V, and a maximum junction temperature of T_J max = 115°C. See Section 5 for details in calculating worst-case, input pin to output pin delays. In general, a lower junction temperature can result in slightly faster intrinsic propagation delays. Macrocell power dissipation is specified at V_{EEE} = -5.2 V. For V_{EEE} = -4.5 V, the typical macro power is calculated by multiplying P_D by the factor 0.865. When operating in PECL mode, the ECL/PECL macro powers are calculated by multiplying P_D by the factor 0.962. See Section 4.4 for calculation of minimum and maximum power.

9.4 Minimum Pulse Width, Setup and Hold Times

The worst-case minimum pulse width (t_{PW}) is specified for the clock inputs of flip-flops and latches to insure proper operation. The setup times for the latches and flip-flops are specified in the Macrocell Library for each version of each macro. The hold time for all latches and flip-flops is zero (0) unless otherwise specified.

9.5 Min RESET, SET Pulse Width and Recovery Time

Many of the flip-flops in the library (such as macros 291, 292, 381, 391, 392, 691, 692, and 694) require the clock line to be in a certain state in order to reset or set the flip-flop. The reason is that the RESET or SET line only goes to the master portion of the flip-flop. The AC specifications in the Design Manual are specified assuming that all inputs are at a DC level except the input that is specified. For instance, the specification for the MIN RESET PULSE WIDTH for macro 291 requires that the CLOCK line (C or D) be HIGH when the flip-flop is reset. This time assures that the master portion of the flip-flop will be reset. Since the slave is enabled, it will also be reset after the master is reset.

An asynchronous reset (or set) can be formed by tying the RESET (or SET) input to one of the clock inputs together on certain flip-flops. Since the RESET (or SET) pulse must ripple through the master and then the slave, the MIN RESET (or SET) PULSE WIDTH must be greater than the specified value and can be calculated from the library specifications using the following formulas:

MIN RESET PULSE WIDTH =
MIN CLOCK POSITIVE PULSE WIDTH +
T_{pd+} (RESET to QB) – T_{pd+} (CLOCK to QB)

MIN SET PULSE WIDTH =
MIN CLOCK POSITIVE PULSE WIDTH +
T_{pd+} (SET to Q) – T_{pd+} (CLOCK to Q)

This is also the time that the clock must remain HIGH after RESET (or SET) goes HIGH. If the clock goes low before satisfying this time, the slave can go into a metastable condition if the Q output of the flip-flop is in the opposite state prior to reset (or set).

For negative edge triggered flip-flops (such as macro 391 and 392), an asynchonous reset cannot be formed by tying the RESET and CLOCK lines together since the CLOCK line must be LOW in order to reset the flip-flop. To calculate how long the CLOCK line must remain LOW from the start of the RESET line going HIGH, the following equation is used:

MIN CLOCK LOW =
MIN CLOCK NEGATIVE PULSE WIDTH +
T_{pd+} (RESET to QB) – T_{pd+} (CLOCK to QB)

The minimum RESET (or SET) recovery time is defined as the amount of time from the falling edge of RESET (or SET) until the active edge of the CLOCK. Unless specified otherwise, the recovery time is equal to the MIN CLOCK NEGATIVE PULSE WIDTH for positive edge triggered flip-flops. For negative edge triggered flip-flops, the recovery time is equal to the MIN CLOCK POSITIVE PULSE WIDTH.

9.6 Macrocell Library

The macro Quick Reference Guide containing the MCA3 ETL array macros listed by function begins on the next page with the macro specifications following. A numerical listing of the macros can be found beginning on page ix. A complete listing of all MCA3 Series macros is located in the Appendix, beginning on page 10-1. The array electrical and switching characteristics are in Sections 10.2 and 10.3 respectively.

MACRO QUICK REFERENCE GUIDE

SIZE indicates the macrocell size in quarter cells for the internal macrocells and in I or O cells for the Input Interface or Output macrocells, respectively.

SG indicates the levels of series gating used in the macrocell function. Note that a '3' in this column denotes a macro which uses three-level series gating and thus cannot be used with a supply voltage of -4.5 Vdc. **All three-level series gated functions are indicated by shading.**

INTERNAL (M-CELL) MACROS

ADDERS

Macro	Function	Size	SG	Page
L/H281	FULL ADDER	FULL CELL	2	9-23
L/H282	FULL ADDER W/GATED INPUTS	1/2 CELL	2	9-23
L/H284	HALF ADDER W/GATED INPUTS	1/4 CELL	2	9-24
L/H285	3-BIT ADDER (SUM)	1/2 CELL	2	9-25
L/H286	3-BIT ADDER (CARRY)	1/2 CELL	2	9-25
L482	TRIPLE FULL ADDER	FULL CELL	2	9-58
L/H485	3-BIT ADDER	1/2 CELL	3	9-59
L/H685	FULL ADDER W/GATED INPUTS	1/2 CELL	3	9-66

AND'S and NAND'S

L804	DUAL 2-INPUT AND	1/4 CELL	2	9-74
L805	DUAL 2-INPUT NAND	1/4 CELL	2	9-75
L820	2-INPUT OR, 2-INPUT AND	1/4 CELL	2	9-79

AND/OR'S

L/H311	3-3-3-3 AND/OR	FULL CELL	2	9-32
L/H312	3-3-3 AND/OR	1/2 CELL	2	9-32
L/H318	3-3 AND/OR	1/2 CELL	1	9-33
L319	3-3-2-1 AND/OR	1/2 CELL	2	9-33
L/H320	2-3-4-4 AND/OR W/ENABLE (HIGH)	FULL CELL	2	9-34
L322	3-3-3 AND/OR	1/2 CELL	1	9-35
L/H323	3-2-2-2-2-3 AND/OR	FULL CELL	2	9-35
L/H324	5-5-5-5 AND/OR	FULL CELL	1	9-36
L/H331	3-2-2 AND/OR	1/2 CELL	2	9-37
L/H511	3-3-3-3 AND/OR	1/2 CELL	3	9-60
L/H512	3-3-3 AND/OR	1/2 CELL	3	9-61
L/H518	3-3 AND/OR	1/4 CELL	2	9-61
L/H519	3-3-2-1 AND/OR	1/2 CELL	2	9-62
L/H520	2-3-4-4 AND/OR W/ENABLE(HIGH)	1/2 CELL	3	9-62
L/H523	3-2-2-2-2-3 AND/OR	FULL CELL	3	9-62

DECODERS and ENCODERS

L/H261	1-TO-4 DECODER W/ENABLE (LOW)	1/2 CELL	2	9-20
L/H262	1-TO-4 DECODER W/ENABLE (HIGH)	1/2 CELL	2	9-20
L/H263	1-TO-4 DECODER (HIGH)	FULL CELL	2	9-20
L/H461	1-OF-4 DECODER W/ENABLE (LOW)	1/2 CELL	3	9-55
L/H462	1-OF-4 DECODER W/ENABLE (HIGH)	1/2 CELL	3	9-56
L464	8-3 ENCODER	FULL CELL	3	9-56
L/H465	1-OF-4 DECODER W/ENABLE (LOW)	1/2 CELL	3	9-57
L/H466	1-OF-4 DECODER W/ENABLE (HIGH)	1/2 CELL	3	9-57

EXOR and EXNOR'S

L/H223	4-INPUT EXNOR	1/2 CELL	2	9-15
L/H224	4-INPUT EXOR	1/2 CELL	2	9-16
L/H424	6-INPUT EXNOR	1/2 CELL	3	9-50
L/H425	6-INPUT EXOR	1/2 CELL	3	9-51

Macro	Function	Size	SG	Page
FLIP-FLOPS				
L/H290	D FLIP-FLOP WITH SET AND RESET	1/2 CELL	2	9-26
L/H291	D FLIP-FLOP WITH RESET	1/2 CELL	2	9-27
L/H292	D FLIP-FLOP WITH MUX	3/4 CELL	2	9-27
L/H372	D FLIP-FLOP W/DIFFERENTIAL CLOCK AND DATA	1/2 CELL	2	9-38
L/H375	D FLIP-FLOP W/DIFFERENTIAL CLOCK	1/2 CELL	2	9-40
L/H376	D FLIP-FLOP W/DIFFERENTIAL CLOCK	1/2 CELL	2	9-40
L/H381	D FLIP-FLOP WITH SET	1/2 CELL	2	9-41
L/H391	D FLIP-FLOP, NEGATIVE EDGE TRIGGERED	1/2 CELL	2	9-42
L/H392	D FLIP-FLOP W/MUX, NEGATIVE EDGE TRIGGERED	3/4 CELL	2	9-42
L/H394	D FLIP-FLOP W/MUX, NEGATIVE EDGE TRIGGERED	FULL CELL	2	9-43
L/H395	D FLIP-FLOP WITH ASYN SET AND DATA ENABLE	FULL CELL	2	9-44
L/H396	SCAN D FLIP-FLOP	FULL CELL	2	9-44
L/H585	SCAN D FLIP-FLOP WITH 2-TO-1 MUX /OR	1/2 CELL	2	9-64
L/H691	D FLIP-FLOP WITH RESET	1/2 CELL	2	9-66
L/H692	D FLIP-FLOP WITH MUX	3/4 CELL	2	9-67
L/H694	D FLIP-FLOP W/RESET (NEGATIVE HOLD TIME)	3/4 CELL	2	9-67
L881	DUAL D (INVERTING) FLIP-FLOP (R OUTPUTS)	1/2 CELL	2	9-85
L882	DUAL D FLIP-FLOP (R OUTPUTS)	1/2 CELL	2	9-86
L895	D FLIP-FLOP	1/4 CELL	2	9-87
LATCHES				
L/H278	3 DATA INPUT DATA LATCH	1/4 CELL	2	9-21
L/H293	D LATCH WITH RESET	1/4 CELL	2	9-28
L/H294	D LATCH WITH MUX	1/2 CELL	2	9-28
L/H295	GATED 2-WAY D LATCH	1/2 CELL	2	9-29
L/H296	EXNOR D LATCH	1/2 CELL	2	9-29
L/H297	GATED 4-WAY D LATCH	3/4 CELL	2	9-30
L/H298	DUAL D LATCH WITH RESET	1/2 CELL	2	9-30
L380	NOR LATCH	1/4 CELL	1	9-41
L/H393	D LATCH WITH CLOCK ENABLE (HIGH)	1/4 CELL	2	9-43
L/H397	D LATCH WITH ASYN SET	1/4 CELL	2	9-45
L/H398	SCAN D LATCH WITH ASYN SET	1/2 CELL	2	9-45
L893	3XD LATCH WITH COMMON CLOCK	1/2 CELL	2	9-86
L/H894	D LATCH WITH MUX	1/4 CELL	3	9-87
L/H896	3XD LATCH WITH COMMON CLOCK	1/2 CELL	2	9-88
EXPANDABLE MUX'S				
L850	EXPANDABLE 2-1 MUX(CODER) AND 2x2-1 MUX	1/2 CELL	2	9-80
L851	EXPANDABLE 2-1 MUX	1/2 CELL	2	9-80
L852	EXPANDABLE 2-1 MUX	1/2 CELL	2	9-81
L853	EXPANDABLE 2-1 MUX	1/2 CELL	2	9-81
L860	EXPANDABLE 4-1 MUX(CODER) WITH ENABLE	1/2 CELL	3	9-81
L/H861	EXPANDABLE 4-1 MUX	1/2 CELL	3	9-82
L/H862	EXPANDABLE 4-1 MUX	1/2 CELL	3	9-82
L/H863	EXPANDABLE 4-1 MUX	1/2 CELL	3	9-83
L870	EXPANDABLE 8-1 MUX(CODER)	1/2 CELL	3	9-83
L/H871	EXPANDABLE 8-1 MUX	1/2 CELL	3	9-84
L/H872	EXPANDABLE 8-1 MUX	1/2 CELL	3	9-84
L/H873	EXPANDABLE 8-1 MUX	1/2 CELL	3	9-85
MUX'S				
L251	4-TO-1 MUX W/ENABLE (LOW)	1/2 CELL	2	9-17
L/H252	QUAD 2-TO-1 MUX	FULL CELL	2	9-17
L/H253	2-TO-1 MUX W/ENABLE (LOW)	1/4 CELL	2	9-18
L/H254	2-TO-1 MUX W/GATED INPUTS	1/4 CELL	2	9-18
L/H255	DUAL 2-TO-1 MUX W/COM. SELECT	1/2 CELL	2	9-18
L/H256	2-TO-1 MUX	1/4 CELL	2	9-19
L258	4-TO-1 MUX W/ENABLE (HIGH)	1/2 CELL	2	9-19
L/H259	4-TO-1 MUX	1/2 CELL	2	9-19
L/H371	2-1 MUX WITH DIFFERENTIAL INPUTS	1/4 CELL	2	9-38

Macro	Function	Size	SG	Page
MUX'S				
L/H373	2-1 MUX W/DIFF INPUTS AND DIFF MUX CTL	1/4 CELL	2	9-39
L/H451	4-1 MUX W/ENABLE(LOW)	1/2 CELL	3	9-52
L452	QUAD 2-TO-1 MUX	1/2 CELL	2	9-52
L/H453	2-TO-1 MUX W/ENABLE(LOW)	1/4 CELL	3	9-52
L/H454	2-TO-1 MUX W/ENABLE(HIGH)	1/4 CELL	3	9-53
L/H455	DUAL 2-TO-1 MUX W/ENABLE (HIGH)	1/2 CELL	3	9-53
L456	TRIPLE 2-TO-1 MUX (COMMON SELECT)	1/2 CELL	2	9-54
L457	TRIPLE 2-TO-1 MUX	1/2 CELL	2	9-54
L/H458	4-1 MUX W/ENABLE (HIGH)	1/2 CELL	3	9-54
L/H459	DUAL 4-1 MUX	1/2 CELL	3	9-55
L470	DUAL 2-TO-1 MUX (COMMON SELECT)	1/4 CELL	2	9-57
H553	2 TO 1 MUX W/ENABLE LOW	1/4 CELL	2	9-63
L/H658	4-1 MUX	1/2 CELL	3	9-65
L/H809	8-1 MUX WITH ENABLE (HIGH)	FULL CELL	3	9-76
L/H810	8-1 MUX WITH ENABLE (HIGH)	FULL CELL	3	9-76
NOR'S				
L/H401	12-INPUT NOR	1/4 CELL	2	9-46
L/H404	12-INPUT NOR	1/2 CELL	3	9-47
L/H502	2-INPUT NOR (Quad Buffer)	1/4 CELL	1	9-59
L814	DUAL 4-INPUT NOR	1/4 CELL	1	9-78
L818	DUAL 2-INPUT NOR	1/4 CELL	1	9-78
OR'S				
L/H332	GATED OR	1/2 CELL	2	9-37
L/H333	GATED OR	1/2 CELL	2	9-37
L/H400	12-INPUT OR	1/4 CELL	2	9-46
L/H501	2-INPUT OR (Quad Buffer)	1/4 CELL	1	9-59
L503	5x2 INPUT OR	1/2 CELL	1	9-59
L811	DUAL 4-INPUT OR	1/4 CELL	1	9-77
L815	DUAL 2-INPUT OR	1/4 CELL	1	9-78
L820	2-INPUT OR, 2-INPUT AND	1/4 CELL	2	9-79
OR/AND/EXOR'S and OR/AND/EXNOR'S				
L/H222	DUAL 2-2 OR/AND/EXNOR	FULL CELL	2	9-15
L/H225	2-1-1-2 OR/AND/EXOR	1/2 CELL	2	9-16
L/H226	2-1-1-2 OR/AND/EXNOR	1/2 CELL	2	9-16
L421	DUAL EXOR	1/4 CELL	2	9-50
L/H422	DUAL 2-2 OR/AND/EXOR	1/2 CELL	3	9-50
OR/AND'S				
L/H211	2-2 OR/AND	1/4 CELL	2	9-12
L/H212	3-2-2-2 OR/AND	1/2 CELL	2	9-12
L213	4-3-3-3 OR/AND	1/2 CELL	1	9-13
L/H214	2-2-2-2-1-1-1-1 OR/AND	FULL CELL	2	9-13
L/H215	2-2-3-3-3 OR/AND	FULL CELL	2	9-13
L/H216	4-2-3-2-3 OR/AND	FULL CELL	2	9-14
L217	5-4-3-2 OR/AND	1/2 CELL	1	9-14
L/H218	5-4-3-2-1 OR/AND	FULL CELL	2	9-14
L/H219	3-3 OR/AND	1/4 CELL	2	9-15
L/H277	4-2-4-2-4-2 OR/AND	3/4 CELL	2	9-21
L/H279	4-2-4-2-4-2-4-2 OR/AND	FULL CELL	2	9-22
L/H280	4-2-4-2 OR/AND	1/2 CELL	2	9-22
L/H310	4-4-4-4 OR/AND	FULL CELL	1	9-31
L/H313	2-2 OR/AND	1/4 CELL	2	9-32
L/H315	2-2-1-1 OR/AND	1/2 CELL	2	9-33
L/H321	6-6-4-4-2-2 OR/AND	FULL CELL	2	9-34
L/H411	2-2-2 OR/AND	1/4 CELL	3	9-47

Macro	Function	Size	SG	Page
OR/AND'S				
L/H413	4-3-3-3 OR/AND	1/2 CELL	2	9-48
L414	3-3-3-3 OR/AND	1/2 CELL	2	9-48
L/H416	4-2-3-2-3 OR/AND	FULL CELL	3	9-48
L417	5-4-3-2 OR/AND	1/2 CELL	2	9-49
L/H418	5-4-3-2-1 OR/AND	3/4 CELL	2	9-49
L/H419	4-4 OR/AND	1/4 CELL	2	9-49
L/H438	6-5-4-3-2-1 OR/AND	1/2 CELL	3	9-51
L/H510	4-4-4-4 OR/AND	1/2 CELL	2	9-60
L/H513	3-1-1-1 OR/AND	1/4 CELL	2	9-61
L/H611	3-3-3 OR/AND	1/4 CELL	3	9-64
L/H616	4-2-3-3-2 OR/AND	1/2 CELL	3	9-65
L/H618	5-4-3-2-1 OR/AND	1/2 CELL	3	9-65
L/H819	3-2-1 OR/AND	1/4 CELL	3	9-79
OR/NOR'S				
L/H200	5-INPUT OR/NOR	1/4 CELL	1	9-11
L/H201	4-INPUT OR/NOR	1/4 CELL	1	9-11
L/H202	2-INPUT OR/NOR	1/4 CELL	1	9-11
L/H203	8-INPUT OR/NOR	1/2 CELL	2	9-11
L204	12-INPUT OR/NOR	1/2 CELL	1	9-12
L/H207	6-INPUT OR/NOR	1/4 CELL	2	9-12
L402	2-INPUT OR/NOR, 3-INPUT OR/NOR	1/4 CELL	1	9-46
L/H403	8-INPUT OR/NOR	1/4 CELL	1	9-47
L812	DUAL 4-INPUT OR/NOR	1/4 CELL	1	9-77
L813	DUAL 4-INPUT OR/NOR	1/4 CELL	1	9-77
L816	DUAL 2-INPUT OR/NOR	1/4 CELL	1	9-78
L817	DUAL 2-INPUT OR/NOR	1/4 CELL	1	9-78
MISC				
L/H221	2-2 OR/EXOR	1/4 CELL	2	9-15
L/H227	2-1 EXOR./AND/NAND	1/2 CELL	2	9-16
L/H228	2-1 AND/EXOR	1/4 CELL	2	9-17
L/H283	2-BIT LOOK-AHEAD CARRY	FULL CELL	2	9-24
L/H370	DIFFERENTIAL LINE RECEIVER	1/4 CELL	2	9-37
L/H374	DIFFERENTIAL LINE RECEIVER	1/4 CELL	1	9-39
L/H427	2-1 EXOR/AND/NAND	1/4 CELL	3	9-51
L/H571	8-OUTPUT BUFFER W/DIFF INPUT & ENABLE (Quad Buffer)	1/2 CELL	3	9-63
L/H593	W BUFFER	1/4 CELL	1	9-64
L/H802	3-INPUT EXOR/EXNOR	1/4 CELL	3	9-74
L/H803	3-INPUT EXOR/EXNOR	1/4 CELL	3	9-74
L/H806	DUAL 2-INPUT AND/NAND	1/4 CELL	2	9-75
L/H807	DUAL 2-INPUT AND/NAND	1/4 CELL	2	9-75

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HIGH FREQUENCY MACROS				
L302	INPUT OR/NOR (High Drive)	1/2 CELL	1	9-31
L328	2-1 AND/EXOR (high Drive)	1/2 CELL	2	9-36
L474	DIFFERENTIAL LINE RECEIVER (High Drive)	1/2 CELL	2	9-58
L700	DIFFERENTIAL LINE RECEIVER (High Drive)	1/2 CELL	1	9-68
L701	2-TO-1 MUX W/DIFFERENTIAL INPUTS AND DIFFERENTIAL MUX CONTROL (High Drive)	1/2 CELL	2	9-68
H710	D FLIP-FLOP WITH DIFFERENTIAL CLOCK AND DATA	1/2 CELL	2	9-69
H711	D FLIP-FLOP W/GATED DATA INPUT AND DIFF CLOCK	1/2 CELL	2	9-70
H712	D FLIP-FLOP W/EXNOR GATED DATA INPUT AND DIFFERENTIAL CLOCK	FULL CELL	3	9-71
L713	D FLIP-FLOP W/DIFF CLOCK AND DATA (High Drive)	FULL CELL	2	9-72
L714	D FLIP-FLOP W/GATED DATA INPUT AND DIFFERENTIAL CLOCK (High Drive)	FULL CELL	2	9-73

I/O (U-CELL) MACROS

ECL INPUT (C) MACROS

L/HC01	INPUT BUFFER (Non-Inverting) Quad Buffer	1-U CELL	1	9-89
L/HC02	INPUT BUFFER (Inverting) Quad Buffer	1-U CELL	1	9-89
L/HC03	INPUT BUFFER (Inverting, Non-Inverting)	1-U CELL	1	9-89
L/HC05	DUAL DIFFERENTIAL INPUT BUFFER	2-U CELL	1	9-90
L/HC13	DIFFERENTIAL INPUT BUFFER	2-U CELL	1	9-90
LC15	DIFFERENTIAL BYPASS	2-U CELL	1	9-90
L/HC50	INPUT LATCH with ENABLE LOW	1-U CELL	1	9-91
LC70	DIFFERENTIAL INPUT BUFFER WITH OFF CHIP TERMINATION INPUTS (High Drive)	2-U CELLS	1	9-91

ECL OUTPUT (E) MACROS

L/HE01	2-INPUT OR	1-U CELL	1	9-92
L/HE02	2-INPUT NOR	1-U CELL	1	9-92
L/HE03	4-INPUT OR	1-U CELL	1	9-92
L/HE04	4-INPUT NOR	1-U CELL	1	9-93
L/HE05	2-TO-1 MUX	1-U CELL	2	9-93
L/HE06	2-2 OR/AND	1-U CELL	2	9-93
L/HE07	2-2 OR/EXOR	1-U CELL	2	9-94
HE08	2-TO-1 MUX with ENABE LOW (Inverting)	1-U CELL	2	9-94
HE09	2-TO-1 MUX with ENABLE LOW (Non-Inverting)	1-U CELL	2	9-95
L/HE10	2-2 OR/NAND	1-U CELL	2	9-95
L/HE11	2-TO-1 MUX with ENABLE LOW	1-U CELL	2	9-96
L/HE12	DIFFERENTIAL OUTPUT BUFFER	2-U CELLS	1	9-96
L/HE50	D LATCH with CLOCK ENABLE LOW	1-U CELL	2	9-97
HE70	DIFFERENTIAL OUTPUT BUFFER	2-U CELLS	1	9-98
HE71	OPEN COLLECTOR DIFFERENTIAL OUTPUT BUFFER	2-U CELLS	1	9-98
LE75	OFF-CHIP TERMINATION PAD	1-U CELL	1	9-98

ECL CUTOFF OUTPUT (ZE) MACROS

ZE00	4-INPUT OR (50 ohm)	1-U CELL	1	9-99
ZE50	4-INPUT OR (25 ohm)	1-U CELL	2	9-99

ECL STECL I/O (S) MACROS

LS00	2-INPUT OR	1-U CELL	1	9-100
LS50	INPUT BUFFER	1-U CELL	1	9-100

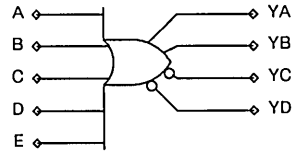
ECL BIDIRECTIONAL (B) MACROS

HB26	2-2 OR/AND with INPUT BUFFER (50 ohm output)	1-U CELL	2	9-101
HB27	2-2 OR/NAND with INPUT BUFFER (50 ohm output)	1-U CELL	2	9-101
HB28	2-TO-1 MUX LOW ENB with INPUT BUFF (50 ohm output)	1-U CELL	2	9-102
HB29	4-INPUT OR with INPUT BUFFER (50 ohm output)	1-U CELL	1	9-102
HB30	4-INPUT NOR with INPUT BUFFER (50 ohm output)	1-U CELL	1	9-103
HB50	4-INPUT OR with INPUT BUFFER (25 ohm cutoff output)	1-U CELL	2	9-103
HB51	4-INPUT NOR with INPUT BUFFER (25 ohm cutoff output)	1-U CELL	2	9-104
HB76	4-INPUT OR with INPUT BUFFER (50 ohm cutoff output)	1-U CELL	1	9-104

Macro	Function	Size	SG	PAGE
TTL TO ECL INPUT (T:00–29) MACROS				
L/HT00	TRANSLATOR with True and Complement	1–U CELL	1	9–105
ECL TO TTL OUTPUT (T:30–59) MACROS				
L/HT30	NOR TRANSLATOR	1–U CELL	1	9–106
L/HT31	NOR TRANSLATOR with TTL Tri–State Enable	1–U CELL	1	9–106
L/HT33	OR TRANSLATOR	1–U CELL	1	9–107
L/HT36	OR TRANSLATOR with ECL Tri–State Enable	1–U CELL	1	9–107
L/HT37	NOR TRANSLATOR with ECL Tri–State Enable	1–U CELL	1	9–108
TTL BIDIRECTIONAL (T:60–89) MACROS				
L/HT60	ECL 2–INPUT NOR TRANSLATOR and TTL to ECL INPUT BUFFER with TTL Tri–State Enable	1–U CELL	1	9–109
L/HT63	ECL 2–INPUT OR TRANSLATOR and TTL to ECL INPUT BUFFER with ECL Tri–State Enable	1–U CELL	1	9–110
L/HT64	ECL 2–INPUT NOR TRANSLATOR and TTL to ECL INPUT BUFFER with ECL Tri–State Enable	1–U CELL	1	9–111
ECL TO TRI–STATE CONTROL (T:90) MACROS				
L/HT90	ECL to Tri–State Control NOR TRANSLATOR	1–U CELL	1	9–112
TTL TO PECL INPUT (P:00–29) MACROS				
L/HP00	TRANSLATOR with True and Complement	1–U CELL	1	9–113
PECL TO TTL OUTPUT (P:30–59) MACROS				
L/HP30	NOR TRANSLATOR	1–U CELL	1	9–114
L/HP33	OR TRANSLATOR	1–U CELL	1	9–114
L/HP36	OR TRANSLATOR with PECL Tri–State Enable	1–U CELL	1	9–115
L/HP37	NOR TRANSLATOR with PECL Tri–State Enable	1–U CELL	1	9–116
TTL BIDIRECTIONAL (P:60–89) MACROS				
L/HP63	PECL 2–INPUT OR TRANSLATOR and TTL to PECL INPUT BUFFER with PECL Tri–State Enable	1–U CELL	1	9–117
L/HP64	PECL 2–INPUT NOR TRANSLATOR and TTL to PECL INPUT BUFFER with PECL Tri–State Enable	1–U CELL	1	9–118

INTERNAL (M) MACROCELLS

MACRO: 200 5-Input OR/NOR
1/4 CELL
1 LEVEL SERIES GATING

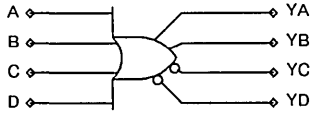


POWER: (mW)
LP Array
L Macro 1.4
H Macro 2.8

YA=YB=$\overline{YC}$=$\overline{YD}$=A+B+C+D+E

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D,E	YA,YB	250	250	200	200
A,B,C,D,E	YC,YD	500	475	350	325

MACRO: 201 4-Input OR/NOR
1/4 CELL
1 LEVEL SERIES GATING

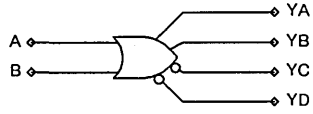


POWER: (mW)
LP Array
L Macro 1.4
H Macro 2.8

YA=YB=$\overline{YC}$=$\overline{YD}$=A+B+C+D

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D	YA,YB	250	275	200	200
A,B,C,D	YC,YD	400	400	300	300

MACRO: 202 2-Input OR/NOR
1/4 CELL
1 LEVEL SERIES GATING

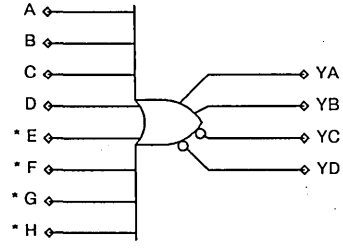


POWER: (mW)
LP Array
L Macro 1.4
H Macro 2.8

YA=YB=$\overline{YC}$=$\overline{YD}$=A+B

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB	250	250	200	200
A,B	YC,YD	250	300	200	225

MACRO: 203 8 INPUT OR/NOR
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6

YA=YB= A+B+C+D+E+F+G+H
YA=YB=$\overline{YC}$=$\overline{YD}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D	YA,YB	250	250	200	200
A,B,C,D	YC,YD	500	475	350	325
E,F,G,H	YA,YB	275	625	225	450
E,F,G,H	YC,YD	525	425	400	325

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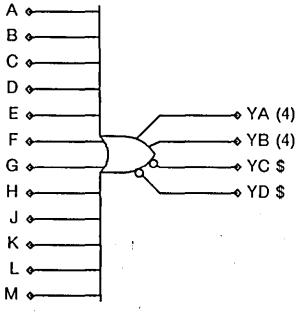
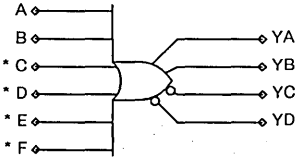
MACRO: 204 12 INPUT OR/NOR
1/2 CELL
1 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 5.7
$YA=YB=\overline{YC}=\overline{YD}=A+B+C+D+E+F+G+H+J+K+L+M$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO			
IN	OUT	(+)	(-)		
A..M	YA,YB	325	250		
A..M	YC,YD	1000	1000		

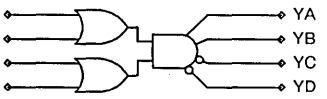
MACRO: 207 6 INPUT OR/NOR
1/4 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6
$YA=YB=\overline{YC}=\overline{YD}=A+B+C+D+E+F$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB	225	250	175	175
A,B	YC,YD	350	200	225	175
C,D,E,F	YA,YB	275	400	200	300
C,D,E,F	YC,YD	350	200	250	200

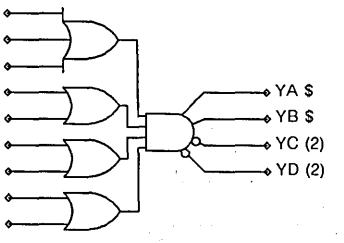
MACRO: 211 2–2 OR/AND
1/4 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6
$YA=YB=\overline{YC}=\overline{YD}=(A+B) \bullet (C+D)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB	325	325	250	250
A,B	YC,YD	250	300	200	225
C,D	YA,YB	275	375	200	300
C,D	YC,YD	350	350	300	250

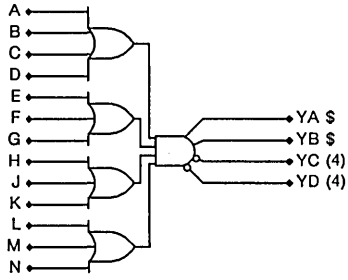
MACRO: 212 3–2–2–2 OR/AND
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1
$YA=(A+B+C) \bullet (D+E) \bullet (F+G) \bullet (H+J)$
$YA=YB=\overline{YC}=\overline{YD}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,F,G	YA,YB	525	500	350	325
A,B,C,F,G	YC,YD	375	300	275	250
D,E,H,J	YA,YB	475	550	300	400
D,E,H,J	YC,YD	475	375	375	275

MACRO: 213 4-3-3-3 OR/AND
1/2 CELL
1 LEVEL SERIES GATING

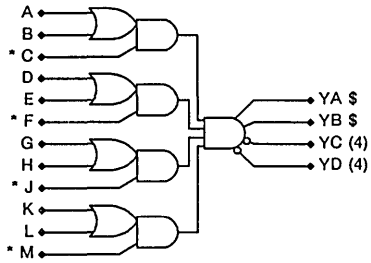


POWER: (mW)
LP Array
L Macro 5.7

YA= (A+B+C+D) • (E+F+G) • (H+J+K) • (L+M+N)
YA=YB=$\overline{YC}$=$\overline{YD}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO			
IN	OUT	(+)	(-)		
A..N	YA,YB	525	500		
A..N	YC,YD	500	350		

MACRO: 214 2-2-2-2-1-1-1-1 OR/AND
FULL CELL
2 LEVEL SERIES GATING

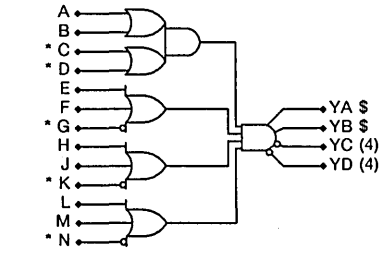


POWER: (mW)
LP Array
L Macro 8.9
H Macro 14.2

YA=((A+B) • C) • ((D+E) • F) • ((G+H) • J) • ((K+L) • M)
YA=YB=$\overline{YC}$=$\overline{YD}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,D,E...	YA,YB	875	775	550	500
A,B,D,E...	YC,YD	350	275	275	200
C,F,J,M	YA,YB	825	800	500	550
C,F,J,M	YC,YD	450	350	350	250

MACRO: 215 2-2-3-3-3 OR/AND
FULL CELL
2 LEVEL SERIES GATING

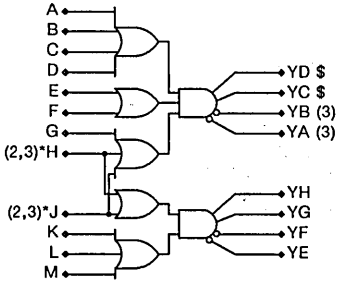


POWER: (mW)
LP Array
L Macro 8.9
H Macro 14.2

YA=YB= ((A+B) • (C+D)) • (E+F+$\overline{G}$) • (H+J+$\overline{K}$) • (L+M+$\overline{N}$)
YA=YB=$\overline{YC}$=$\overline{YD}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,E,F,H,J,L,M	YA,YB	650	600	450	375
A,B,E,F,H,J,L,M	YC,YD	350	300	275	225
C,D,G,K,N	YA,YB	600	650	375	450
C,D,G,K,N	YC,YD	475	350	375	250

MACRO: 216 4–2–3–2–3 OR/AND
FULL CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
H	1	1	
J	1	1	

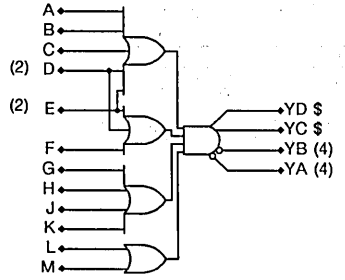
POWER: (mW)
LP Array
L Macro 6.5
H Macro 11.8

$YC = YD = \overline{YA} \cdot \overline{YB} = (A+B+C+D) \cdot (E+F) \cdot (G+H+J)$

$YG = YH = \overline{YE} \cdot \overline{YF} = (H+J) \cdot (K+L+M)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A..G	YA,YB	500	350	350	275
A..G	YC,YD	475	425	350	300
K,L,M	YE,YF	325	350	250	250
K,L,M	YG,YH	325	325	250	250
H,J	YA,YB	400	325	300	250
H,J	YC,YD	450	425	325	300
H,J	YE,YF	450	400	350	300
H,J	YG,YH	275	375	300	300

MACRO: 217 5–3–4–2 OR/AND
1/2 CELL
1 LEVEL SERIES GATING



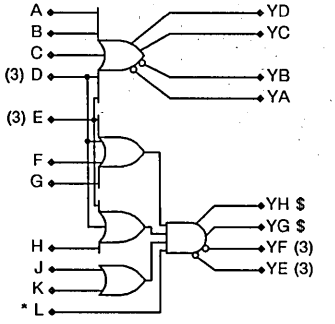
POWER: (mW)
LP Array
L Macro 5.7

$YC = YD = (A+B+C+D+E) \cdot (E+D+F) \cdot (G+H+J+K) \cdot (L+M)$

$YC = YD = \overline{YA} \cdot \overline{YB}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO			
IN	OUT	(+)	(–)		
A..M	YA,YB	500	425		
A..M	YC,YD	525	500		

MACRO: 218 5–4–3–2–1 OR/AND
FULL CELL
2 LEVEL SERIES GATING



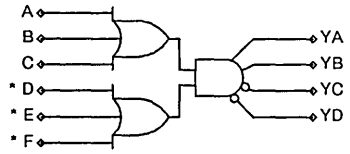
POWER: (mW)
LP Array
L Macro 6.5
H Macro 11.8

$YC = YD = \overline{YA} \cdot \overline{YB} = (A+B+C+D+E)$

$YG = YH = \overline{YE} \cdot \overline{YF} = (D+E+F+G) \cdot (E+D+H) \cdot (J+K) \cdot L$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A..E	YA,YB	575	475	375	325
A..E	YC,YD	250	275	200	225
D..K	YE,YF	375	350	300	250
D..K	YG,YH	550	350	375	250
L	YE,YF	525	375	475	275
L	YG,YH	550	500	375	450

MACRO: 219 3-3 OR/AND
1/4 CELL
2 LEVEL SERIES GATING

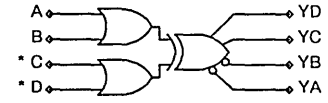


POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6

$YA=YB=\overline{YC}=\overline{YD}=(A+B+C) \cdot (D+E+F)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C	YA,YB	325	325	250	250
A,B,C	YC,YD	325	350	250	250
D,E,F	YA,YB	275	375	200	300
D,E,F	YC,YD	450	400	350	300

MACRO: 221 2-2 OR/EXOR
1/4 CELL
2 LEVEL SERIES GATING



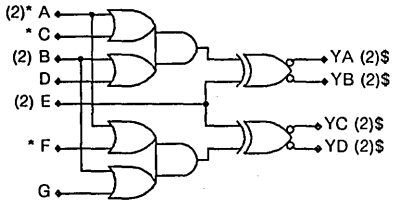
	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		
B	1.5		

POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6

$YC=YD=\overline{YA}=\overline{YB}=(A+B)\oplus(C+D)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YC,YD	325	350	250	250
A,B	YA,YB	375	350	275	275
C,D	YC,YD	400	600	275	450
C,D	YA,YB	425	400	325	300

MACRO: 222 DUAL 2-2 OR/AND/EXNOR
FULL CELL
2 LEVEL SERIES GATING



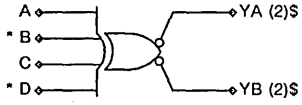
POWER: (mW)
LP Array
L Macro 7.3
H Macro 12.6

$YA=YB=\overline{((A+C) \cdot (B+D))\oplus E}$

$YC=YD=\overline{((A+F) \cdot (B+G))\oplus E}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
B,D,E,G	YA..YD	500	425	325	300
A,C,F	YA..YD	450	550	300	400

MACRO: 223 4-INPUT EXNOR
1/2 CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		
C	1.5		

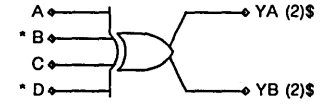
POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1

$YA=YB=\overline{A\oplus B\oplus C\oplus D}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,C	YA,YB	725	800	450	350
B,D	YA,YB	875	950	550	600

9

MACRO: 224 4-INPUT EXOR
1/2 CELL
2 LEVEL SERIES GATING



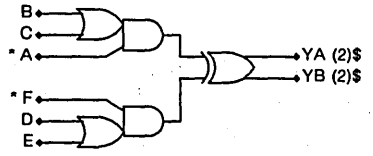
	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		
C	1.5		

POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1

YA=YB=A⊕B⊕C⊕D

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,C	YA,YB	725	600	425	550
B,D	YA,YB	850	900	550	600

MACRO: 225 2-1-1-2 OR/AND/EXOR
1/2 CELL
2 LEVEL SERIES GATING

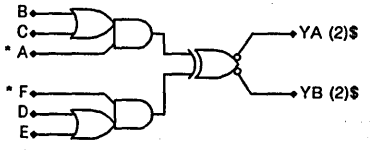


POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1

YA=YB=((B+C) • A)⊕((D+E) • F)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
B,C,D,E	YA,YB	575	475	350	300
A,F	YA,YB	650	525	400	350

MACRO: 226 2-1-1-2 OR/AND/EXNOR
1/2 CELL
2 LEVEL SERIES GATING

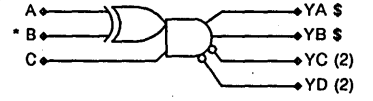


POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1

YA=YB=((B+C) • A)⊕((D+E) • F)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
B,C,D,E	YA,YB	575	450	350	300
A,F	YA,YB	625	500	400	350

MACRO: 227 2-1 EXOR/AND/NAND
1/2 CELL
2 LEVEL SERIES GATING



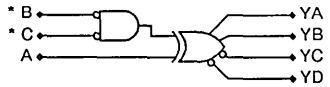
	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		

POWER: (mW)
LP Array
L Macro 3.7
H Macro 6.3

YA=YB=$\overline{YC}$=$\overline{YD}$=(A⊕B) • C

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A	YA,YB	425	375	275	250
A	YC,YD	325	275	225	200
C	YA,YB	475	425	300	275
C	YC,YD	200	200	175	150
B	YA,YB	500	650	300	425
B	YC,YD	400	425	250	325

MACRO: 228 2–1 AND/EXOR
1/4 CELL
2 LEVEL SERIES GATING



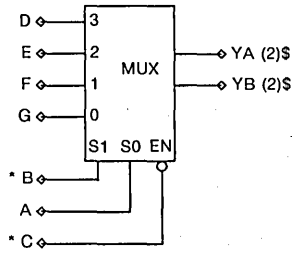
	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		

POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6

$YA = YB = \overline{YC} = \overline{YD} = (\overline{B} \cdot \overline{C}) \oplus A$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A	YA,YB	275	275	200	200
A	YC,YD	275	275	200	200
B,C	YA,YB	325	475	250	350
B,C	YC,YD	325	450	250	350

MACRO: 251 4–TO–1 MUX W/ENABLE (LOW)
1/2 CELL
2 LEVEL SERIES GATING



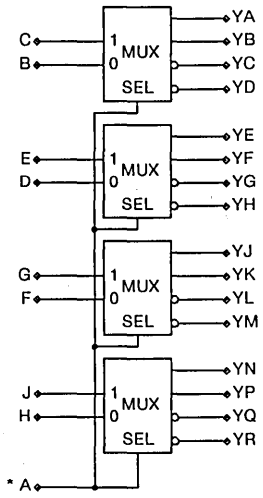
POWER: (mW)
LP Array
L Macro 7.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO			
IN	OUT	(+)	(–)		
A,D,E,F,G	YA,YB	550	500		
B,C	YA,YB	600	750		

TRUTH TABLE

C	B	A	YA	YB
H	X	X	L	L
L	L	L	G	G
L	L	H	F	F
L	H	L	E	E
L	H	H	D	D

MACRO: 252 QUAD 2–TO–1 MUX
FULL CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 6.5
H Macro 11.8

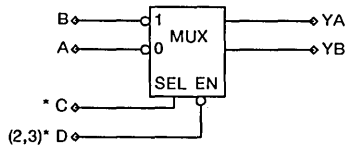
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
B..H	YA,YB	300	300	225	225
B..H	YC,YD	225	275	175	200
A	YA,YB	350	575	250	425
A	YC,YD	350	375	275	250

TRUTH TABLE

A	YA,YB	YC,YD	YE,YF	YG,YH	YJ,YK	YL,YM	YN,YP	YQ,YR
H	C	$\overline{C}$	E	$\overline{E}$	G	$\overline{G}$	J	$\overline{J}$
L	B	$\overline{B}$	D	$\overline{D}$	F	$\overline{F}$	H	$\overline{H}$

9

MACRO: 253 2–TO–1 MUX W/ENABLE (LOW)
1/4 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6

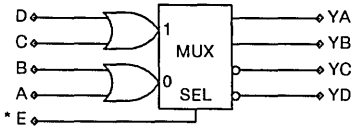
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB	425	400	300	275
C,D	YA,YB	525	625	350	425

	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
D	1	1	

TRUTH TABLE

D	C	YA,YB
H	X	L
L	L	$\overline{A}$
L	H	$\overline{B}$

MACRO: 254 2–TO–1 MUX W/GATED INPUTS
1/4 CELL
2 LEVEL SERIES GATING



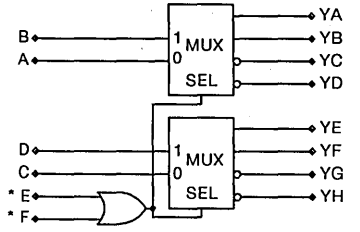
POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	YA,YB	300	300	225	250
A,B,C,D	YC,YD	400	400	300	300
E	YA,YB	350	550	225	400
E	YC,YD	500	450	375	300

TRUTH TABLE

E	YA,YB	YC,YD
L	A+B	$\overline{(A+B)}$
H	C+D	$\overline{(C+D)}$

MACRO: 255 DUAL 2–TO–1 MUX W/COM. SELECT
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 3.7
H Macro 6.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB	300	300	225	225
A,B	YC,YD	250	275	175	200
C,D	YE,YF	300	300	225	225
C,D	YG,YH	250	275	175	200
E,F	YA,YB,YE,YF	350	475	250	350
E,F	YC,YD,YG,YH	475	350	350	250

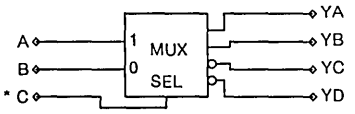
TRUTH TABLE

SEL	YA,YB	YC,YD
L	A	$\overline{A}$
H	B	$\overline{B}$

SEL	YE,YF	YG,YH
L	C	$\overline{C}$
H	D	$\overline{D}$

SEL=E+F

MACRO: 256 2-TO-1 MUX
1/4 CELL
2 LEVEL SERIES GATING



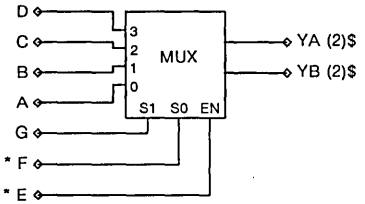
TRUTH TABLE

C	YA,YB	YC,YD
L	B	$\overline{B}$
H	A	$\overline{A}$

POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB	300	300	225	225
A,B	YC,YD	250	275	175	200
C	YA,YB	325	450	250	350
C	YC,YD	450	325	350	250

MACRO: 258 4-TO-1 MUX W/ENABLE (HIGH)
1/2 CELL
2 LEVEL SERIES GATING



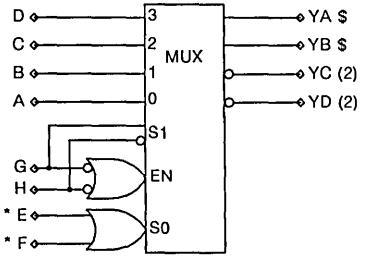
POWER: (mW)
LP Array
L Macro 7.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO			
IN	OUT	(+)	(-)		
A,B,C,D,G	YA,YB	550	475		
E,F	YA,YB	525	550		

TRUTH TABLE

E	G	F	YA,YB
L	X	X	L
H	L	L	A
H	L	H	B
H	H	L	C
H	H	H	D

MACRO: 259 4-TO-1 MUX
1/2 CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
G	1.5		
H	1.5		

POWER: (mW)
LP Array
L Macro 3.7
H Macro 6.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D,G,H	YA,YB	525	450	325	300
A,B,C,D,G,H	YC,YD	450	350	300	250
E,F	YA,YB	575	675	350	450
E,F	YC,YD	550	475	400	300

TRUTH TABLE

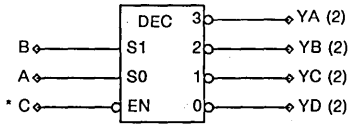
G	H	E+F	YA,YB	YC,YD	
L	H	L	A	$\overline{A}$	4 to 1 MUX SELECTED
L	H	H	B	$\overline{B}$	
H	L	L	C	$\overline{C}$	
H	L	H	D	$\overline{D}$	
H	H	X	H	L	MUX DISABLED
L	L	L	A•C	$\overline{A}\bullet\overline{C}$	2 to 1 MUX SELECTED
L	L	H	B•D	$\overline{B}\bullet\overline{D}$	

$YC\text{-}YD\text{-}(\overline{A} \bullet \overline{G} \bullet (\overline{E+F})+\overline{B} \bullet \overline{G} \bullet (E+F)+\overline{C} \bullet \overline{H} \bullet (\overline{E+F})+\overline{D} \bullet \overline{H} \bullet (E+F)) \bullet (\overline{G}+\overline{H})$

$YA\text{-}YB\text{-}\overline{YC}\text{-}\overline{YD}$

9

MACRO: 261 1–OF–4 DECODER W/ENABLE (LOW)
1/2 CELL
2 LEVEL SERIES GATING



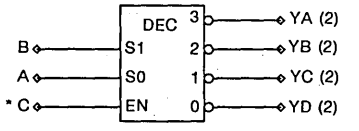
POWER: (mW)
LP Array
L Macro 3.7
H Macro 6.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB,YC,YD	225	250	175	175
C	YA,YB,YC,YD	475	525	300	375

TRUTH TABLE

C	B	A	YA	YB	YC	YD
H	X	X	H	H	H	H
L	L	L	H	H	H	L
L	L	H	H	H	L	H
L	H	L	H	L	H	H
L	H	H	L	H	H	H

MACRO: 262 1–OF–4 DECODER W/ENABLE (HIGH)
1/2 CELL
2 LEVEL SERIES GATING



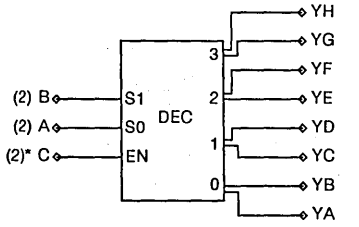
POWER: (mW)
LP Array
L Macro 3.7
H Macro 6.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB,YC,YD	300	275	225	200
C	YA,YB,YC,YD	400	250	300	175

TRUTH TABLE

C	B	A	YA	YB	YC	YD
L	X	X	H	H	H	H
H	L	L	H	H	H	L
H	L	H	H	H	L	H
H	H	L	H	L	H	H
H	H	H	L	H	H	H

MACRO: 263 1–OF–4 DECODE (HIGH)
FULL CELL
2 LEVEL SERIES GATING



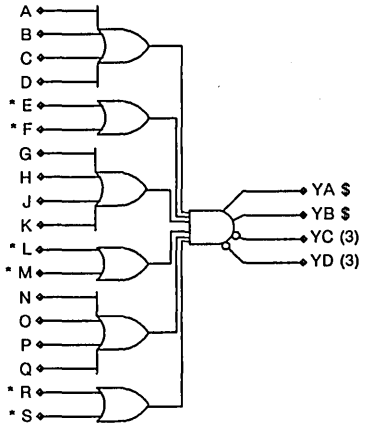
POWER: (mW)
LP Array
L Macro 7.3
H Macro 12.6

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YC,YD,YG,YH	425	375	275	250
A,B	YA,YB,YE,YF	350	350	225	250
C	ALL OUTPUTS	475	600	300	425

TRUTH TABLE

C	B	A	YA,YB	YC,YD	YE,YF	YG,YH
L	X	X	L	L	L	L
H	L	L	H	L	L	L
H	L	H	L	H	L	L
H	H	L	L	L	H	L
H	H	H	L	L	L	H

MACRO: 277 4-2-4-2-4-2 OR/AND
3/4 CELL
2 LEVEL SERIES GATING

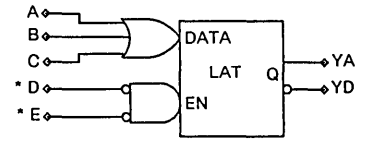


POWER: (mW)
LP Array
L Macro 6.7
H Macro 10.7

$YA=YB=\overline{YC}=\overline{YD}=(A+B+C+D) \bullet (E+F) \bullet (G+H+J+K) \bullet (L+M) \bullet (N+O+P+Q) \bullet (R+S)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
ABCDGHJKNOPQ	YA,YB	425	325	300	250
ABCDGHJKNOPQ	YC,YD	550	525	350	350
E,F,L,M,R,S	YA,YB	425	375	300	275
E,F,L,M,R,S	YC,YD	550	525	350	350

MACRO: 278 3 DATA INPUT D LATCH
1/4 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 4.7
H Macro 6.0

DATA=A+B+C
YA=$\underline{Q}$
YD=$\underline{YA}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C	YA,YD	400	400	250	250
D,E	YA,YD	450	525	300	350
SET UP TIME		600		450	
MIN ENABLE PULSE WIDTH		1000		750	

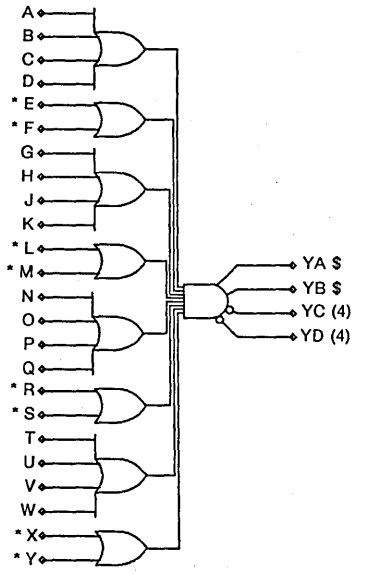
TRUTH TABLE

DATA	D	E	YA
X	H	X	--
X	X	H	--
L	L	L	L
H	L	L	H

NOTE: -- = NO CHANGE

9

MACRO: 279 4-2-4-2-4-2-4-2 OR/AND
FULL CELL
2 LEVEL SERIES GATING



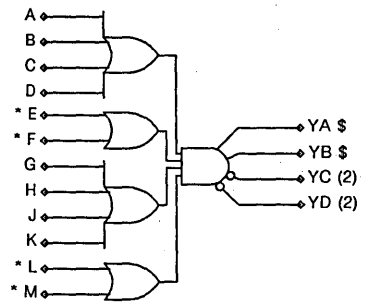
POWER: (mW)
LP Array
L Macro 8.9
H Macro 14.2

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
ABCDGHJKNOPQ TUVWW	YA,YB	675	650	400	375
ABCDGHJKNOPQ TUVWW	YC,YD	575	375	350	250
E,F,L,M,R,S,X,Y	YA,YB	775	850	475	500
E,F,L,M,R,S,X,Y	YC,YD	625	375	400	250

YA=YB=(A+B+C+D) • (E+F) • (G+H+J+K) • (L+M) • (N+O+P+Q) • (R+S) • (T+U+V+W) • (X+Y)

$YA=YB=\overline{YC}=\overline{YD}$

MACRO: 280 4-2-4-2 OR/AND
1/2 CELL
2 LEVEL SERIES GATING

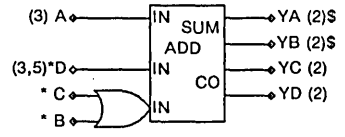


POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1

$YA=YB=\overline{YC}=\overline{YD}$=(A+B+C+D) • (E+F) • (G+H+J+K) • (L+M)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D,G,H,J,K	YA,YB	525	500	350	325
A,B,C,D,G,H,J,K	YC,YD	375	300	270	250
E,F,L,M	YA,YB	475	550	300	400
E,F,L,M	YC,YD	475	375	375	275

MACRO: 281 FULL ADDER
FULL CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	3.5		
D	2	1	

YA-YB YC-YD

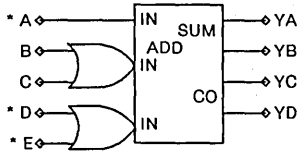
POWER: (mW)
LP Array
L Macro 7.3
H Macro 12.6

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A	YA,YB	400	350	275	225
A	YC,YD	450	350	300	250
B,C,D	YA,YB	525	425	375	275
B,C,D	YC,YD	500	550	325	400

TRUTH TABLE

D	C	B	A	YA,YB	YC,YD
L	L	L	L	L	L
L	L	L	H	H	L
L	H	X	L	H	L
L	X	H	L	H	L
L	H	X	H	L	H
L	X	H	H	L	H
H	L	L	L	H	L
H	L	L	H	L	H
H	H	X	L	L	H
H	X	H	L	L	H
H	H	X	H	H	H
H	X	H	H	H	H

MACRO: 282 FULL ADDER W/GATED INPUTS
1/2 CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
B	1.5		
C	1.5		

YA-YB YC-YD

POWER: (mW)
LP Array
L Macro 5.5
H Macro 8.1

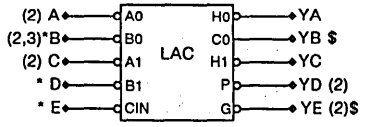
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A	YA,YB	350	350	250	250
A	YC,YD	350	525	225	375
B,C	YA,YB	600	700	475	500
B,C	YC,YD	675	775	425	550
D,E	YA,YB	800	900	600	600
D,E	YC,YD	750	975	450	700

TRUTH TABLE

A	B+C	D+E	YA,YB	YC,YD
L	L	L	L	L
H	L	L	H	L
L	H	L	H	L
H	H	L	L	H
L	L	H	H	L
H	L	H	L	H
L	H	H	L	H
H	H	H	H	H

9

MACRO: 283 2-BIT LOOK-AHEAD CARRY
FULL CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	2.5		
B	1	1	
C	2.5		

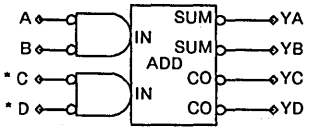
POWER: (mW)

	LP Array
L Macro	8.1
H Macro	13.4

TRUTH TABLE

D	C	B	A	YE	YD	YA	YC
L	L	L	L	L	H	H	H
L	L	L	H	L	H	L	H
L	L	H	L	L	H	L	H
L	L	H	H	L	H	H	H
L	H	L	L	L	H	H	L
L	H	L	H	H	L	L	L
L	H	H	L	H	L	L	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	H	L
H	L	L	H	H	L	L	L
H	L	H	L	H	L	L	L
H	L	H	H	H	H	H	L
H	H	L	L	H	H	H	H
H	H	L	H	H	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	H	H	H	H

MACRO: 284 HALF ADDER W/GATED INPUTS
1/4 CELL
2 LEVEL SERIES GATING



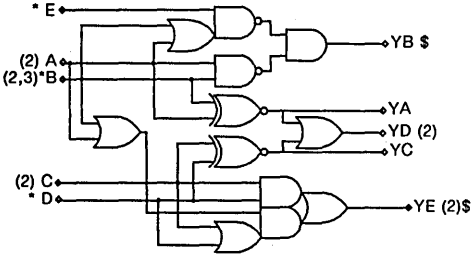
POWER: (mW)

	LP Array
L Macro	2.2
H Macro	3.6

	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		
B	1.5		

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A	YA	250	275	200	200
A	YB	350	350	225	225
A	YD	275	275	200	200
A	YE	375	300	250	225
B,D,E	YA,YC	350	400	275	275
B,D,E	YB	300	325	200	225
B,D,E	YD	375	400	300	275
B,D,E	YE	400	450	275	325
C	YD,YC	325	325	225	225
C	YE	425	325	275	225

LOGIC EQUIVALENT



TRUTH TABLE

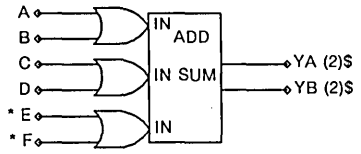
A	B	E	YB
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	L

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB	325	350	225	225
A,B	YC,YD	225	225	175	175
C,D	YA,YB	425	500	300	325
C,D	YC,YD	250	400	175	300

TRUTH TABLE

A	B	C	D	YA,YB	YC,YD
L	L	L	L	H	L
L	L	H	X	L	H
L	L	X	H	L	H
H	X	L	L	L	H
X	H	L	L	L	H
X	H	X	H	H	H
X	H	H	X	H	H
H	X	X	H	H	H
H	X	H	X	H	H

MACRO: 285 3–BIT ADDER (SUM)
1/2 CELL
2 LEVEL SERIES GATING

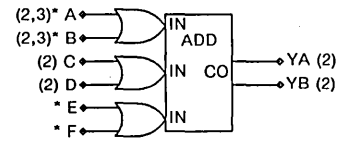


	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
C	1.5		
D	1.5		

POWER: (mW)
LP Array
L Macro 3.7
H Macro 6.3
YA–YB=(A+B)⊕(C+D)⊕(E+F)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB	600	475	350	300
C,D	YA,YB	650	500	375	325
E,F	YA,YB	725	725	450	450

MACRO: 286 3–BIT ADDER (CARRY)
1/2 CELL
2 LEVEL SERIES GATING

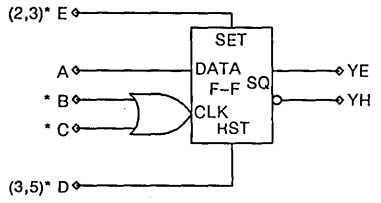


	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1	1	
B	1	1	

POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1
YA–YB=(A+B) • (C+D)+(A+B) • (E+F)+(C+D) • (E+F)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB	300	350	225	275
C,D	YA,YB	350	325	250	225
E,F	YA,YB	300	325	200	250

MACRO: 290 D FLIP–FLOP WITH SET AND RESET
1/2 CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
D	2	1	
E	1	1	

TRUTH TABLE

RESET	SET	DATA	CLOCK	SLAVE Q	
D	E	A	B+C	YE	
L	L	X	H	--	
L	L	X	L	--	
L	L	L	L→H	L	
L	L	H	L→H	H	
L→H	X	X	X	L	1,3
H	X	X	L→H	L	1,3
L	L→H	L	L	⊻	2
L	L→H	X	H	H	
L	L→H	H	X	H	
L	H	X	L→H	H	
H→L	H→L	X	X	ND	3
H	L→H	X	X	L	3
H	H→L	X	X	L	3,4
H→L	H	X	X	H	3,5

NOTE: -- = NO CHANGE
ND = NOT DEFINED

POWER: (mW)

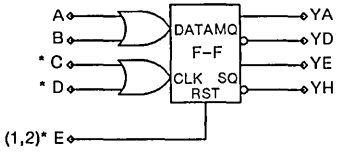
	LP Array
L Macro	8.1
H Macro	10.8

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
B,C	YE	450	425	325	300
B,C	YH	325	550	250	350
D	YE	--	450	--	300
D	YH	350	--	250	--
E	YE	900	--	625	--
E	YH	--	900	--	600
SET UP		600		450	
MIN CLOCK PERIOD		2000		1500	
MIN CLOCK PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	
MIN SET PULSE WIDTH IF CLK IS 'L'		1500		1100	
MIN SET PULSE WIDTH IF CLK IS 'H'		1075		825	
MIN SET/RESET RECOVERY TIME		1000		750	

TRUTH TABLE NOTES:

1. No output glitch occurs due to the RESET input.
2. A negative glitch occurs due to the SET input.
3. The SQ will be low and the SQ-invert will be high while both SET and RESET are high, but output states are unpredictable if both go low simultaneously.
4. The RESET input is not allowed to switch to a "L" for at least 1100 ps (LPA) or 900 ps (HPA) after SET switches from "H" to "L".
5. The output goes to an unknown state for 480 ps (LPA) or 350 ps (HPA) ps max before switching to a "H". The SET input is not allowed to switch to a "L" for 1500 (LPA) ps or 1100 ps (HPA) after RESET switches from "H" to "L" [1100 ps (LPA) or 900 ps (LPA) if clock = "H"].

MACRO: 291 D FLIP–FLOP W/RESET
1/2 CELL
2 LEVEL SERIES GATING



TRUTH TABLE

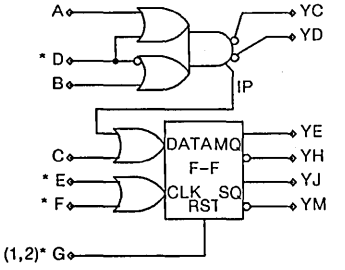
RESET	DATA	CLOCK	MASTER Q	SLAVE Q
E	A+B	C+D	YA	YE
L	X	H	--	--
L	L	L	L	--
L	L	L→H	L	L
L	H	L	H	--
L	H	L→H	H	H
H	X	H	L	L
H	L	L	L	--
H	L	L→H	L	L
H	H	L	H	--
H	H	L→H	L	⊓

NOTE: -- = NO CHANGE

POWER: (mW)
LP Array
L Macro 8.1
H Macro 10.8

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YD	400	400	275	300
C,D	YA,YD	400	625	300	425
C,D	YE,YH	350	425	250	275
E	YA,YD	525		375	
E	YE,YH	950		700	
SET UP		600		450	
MIN CLOCK PERIOD		2000		1500	
MIN CLOCK PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	

MACRO: 292 D FLIP–FLOP WITH MUX
3/4 CELL
2 LEVEL SERIES GATING



TRUTH TABLE

RESET	DATA	CLOCK	MASTER Q	SLAVE Q
L	X	H	--	--
L	L	L	L	--
L	L	L→H	L	L
L	H	L	H	--
L	H	L→H	H	H
H	X	H	L	L
H	L	L	L	--
H	L	L→H	L	L
H	H	L	H	--
H	H	L→H	L	⊓

NOTE: -- = NO CHANGE

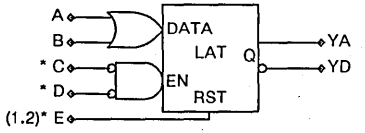
POWER: (mW)
LP Array
L Macro 11.4
H Macro 15.3
RESET=G MASTER Q =YE
DATA= (A+D) • (B+$\overline{D}$)+C CLOCK=E+F
SLAVE Q=YJ

YC=YD= $\overline{(A+D) \bullet (B+\overline{D})}$ YH=$\overline{YE}$ YM=$\overline{YJ}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YC,YD	250	275	175	200
A,B	YE,YH	700	700	500	525
A,B	IP	300	300	225	225
D	IP	325	450	250	350
D	YC,YD	350	475	250	350
D	YE,YH	725	850	525	650
C,IP	YE,YH	400	400	275	300
E,F	YE,YH	400	625	300	425
E,F	YJ,YM	350	425	250	275
G	YE,YH	525		375	
G	YJ,YM	950		700	
C, IP TO CLOCK SET UP		600		450	
MIN CLOCK PERIOD		2000		1500	
MIN CLOCK PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	

NOTES:
1. If A,B or D inputs are used the AB, IP, or D →IP Delay must be added to the setup and hold time.
2. C,IP to clock hold = 0ps
3. 292 can be used as a JK Flip–Flop by labeling the B input as 'J', the A input as 'K', and connecting output YM to input D.

MACRO: 293 D LATCH WITH RESET
1/4 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 4.7
H Macro 6.0
RESET=E YA=Q

DATA=A+B YD= $\overline{YA}$
EN=$\overline{C}$ • $\overline{D}$

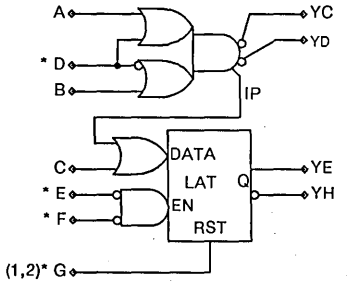
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YD	400	400	250	250
C,D	YA,YD	450	525	300	350
E	YA	--	525	--	375
E	YD	525	--	375	--
SET UP TIME		600		450	
MIN ENABLE PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	

TRUTH TABLE

RESET	DATA	C	D	Q
L	X	H	X	-
L	X	X	H	-
H	X	H	X	L
H	X	X	H	L
X	L	L	L	L
X	H	L	L	H

NOTE: -- = NO CHANGE

MACRO: 294 D LATCH WITH MUX
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 7.9
H Macro 10.6
RESET=G YE=Q

DATA=(A+D) • (B+D)+C YH= $\overline{YE}$

$\overline{YC-YD}$=(A+D) • ($\overline{B+D}$)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YC,YD	250	275	175	200
A,B	YE,YH	700	700	475	475
A,B	IP	300	300	225	225
D	IP	325	450	250	350
D	YC,YD	325	425	250	275
C	YE,YH	400	400	250	250
E,F	YE,YH	450	525	300	350
G	YE,YH	525	525	375	375
D	YE,YH	725	850	500	600
C, IP TO EN SETUP TIME		600		450	
MIN ENABLE PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	

TRUTH TABLE

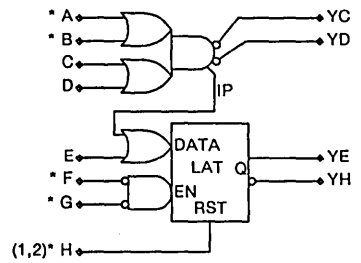
RESET	DATA	E	F	Q
L	X	H	X	-
L	X	X	H	-
H	X	H	X	L
H	X	X	H	L
X	L	L	L	L
X	H	L	L	H

NOTE: -- = NO CHANGE

NOTES
1 If A,B or D inputs are used the delay to IP must be added to the setup and hold time.
2. Hold time on input C is 0 ps.

9

MACRO: 295 GATED 2-WAY D LATCH
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 7.9
H Macro 10.6
RESET=H YE=Q
DATA=(A+B) • (C+D)+E YH=$\overline{YE}$

YC=YD=(A+B) • (C+D)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YC,YD	325	425	250	275
A,B	YE,YH	725	850	500	600
A,B	IP	325	450	250	350
C,D	IP	300	300	225	225
C,D	YC,YD	225	275	175	200
C,D	YE,YH	700	700	475	475
F,G	YE,YH	450	525	300	350
H	YE,YH	525	525	375	375
E	YE,YH	400	400	250	250
E, IP TO EN SETUP TIME		600		450	
MIN ENABLE PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	

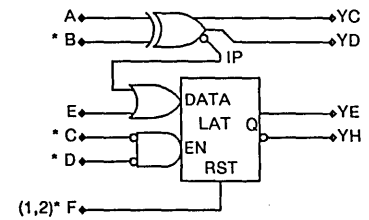
TRUTH TABLE

RESET	DATA	F	G	Q
L	X	H	X	--
L	X	X	H	--
H	X	H	X	L
H	X	X	H	L
X	L	L	L	L
X	H	L	L	H

NOTE: -- = NO CHANGE

NOTES
1. If A-D are used, the delay to IP must be added to setup/hold time.
2. Hold time on input E is 0ps.

MACRO: 296 EXNOR D LATCH
1/2 CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		

POWER: (mW)
LP Array
L Macro 7.9
H Macro 10.6

RESET=F YE=Q

DATA=$\overline{(A \oplus B)}$+E YH=$\overline{YE}$
YC=YD=A⊕B

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A	YC,YD	300	300	200	200
A	YE,YH	775	750	525	525
A	IP	375	350	275	275
B	IP	425	400	325	300
B	YC,YD	350	450	250	325
B	YE,YH	825	800	575	550
E	YE,YH	400	400	250	250
C,D	YE,YH	450	525	300	350
F	YE,YH	525	525	375	375
E, IP TO EN SETUP TIME		600		450	
MIN ENABLE PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	

TRUTH TABLE

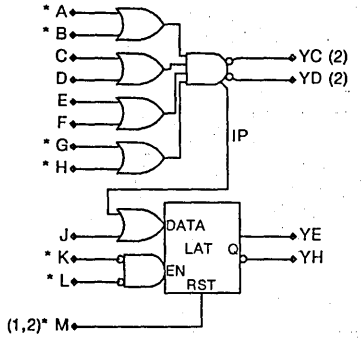
RESET	DATA	C	D	Q
L	X	H	X	-
L	X	X	H	-
H	X	H	X	L
H	X	X	H	L
X	L	L	L	L
X	H	L	L	H

NOTE: -- = NO CHANGE

NOTES
1. If A or B is used, the delay to IP must be added to setup/hold time.
2. Hold time on input E is 0 ps.

9

MACRO: 297 GATED 4-WAY D-LATCH
3/4 CELL
2 LEVEL SERIES GATING



POWER: (mW)

	LP Array
L Macro	10.1
H Macro	14.1

RESET=M
DATA=(A+B) • (C+D) • (E+F) • (G+H)+J

YC=YD=(A+B) • (C+D) • (E+F) • (G+H)
YE=Q
YH= $\overline{YE}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,G,H	YC,YD	325	425	250	275
A,B,G,H	YE,YH	875	950	550	650
A,B,G,H	IP	475	550	300	400
C,D,E,F	YC,YD	250	275	175	200
C,D,E,F	IP	525	500	350	325
C,D,E,F	YE,YH	925	900	600	575
J	YE,YH	400	400	250	250
K,L	YE,YH	450	525	300	350
M	YE,YH	525	525	375	375
J, IP TO EN SETUP TIME		600		450	
MIN ENABLE PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	

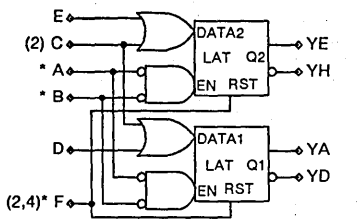
TRUTH TABLE

RESET	DATA	K	L	Q
L	X	H	X	--
L	X	X	H	--
H	X	H	X	L
H	X	X	H	L
X	L	L	L	L
X	H	L	L	H

NOTE: -- = NO CHANGE

NOTES
1. If A-H inputs are used the delay to IP must be added to the setup and hold time.
2. Hold time on input J is 0ps.

MACRO: 298 DUAL D-LATCH W/RESET
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)

	LP Array
L Macro	8.1
H Macro	10.8

RESET=F YA=Q1 YE=Q2
DATA 1=D+C YH= $\overline{YE}$
DATA 2=C+E YD= $\overline{YA}$

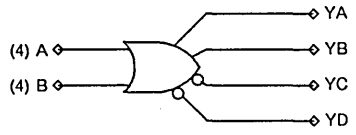
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YD,YE,YH	450	525	300	350
C,D,E	YA,YD,YE,YH	400	400	250	250
F	YA,YD,YE,YH	525	525	375	375
SET UP TIME		600		450	
MIN ENABLE PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	

TRUTH TABLE

RESET	DATA (i)	A	B	Q (i)
L	X	H	X	--
L	X	X	H	--
H	X	H	X	L
H	X	X	H	L
X	L	L	L	L
X	H	L	L	H

NOTE: -- = NO CHANGE

MACRO: 302 INPUT OR/NOR
HI DRIVE MACRO
1/2 CELL
1 LEVEL SERIES GATING



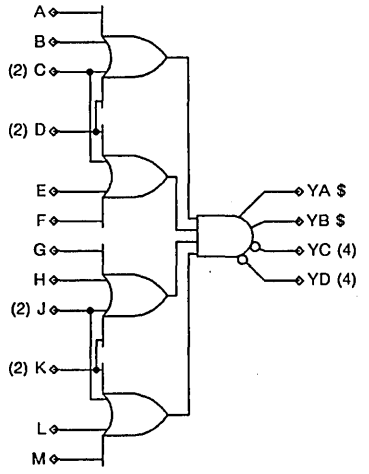
	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1		
B	1		

POWER: (mW)
LP Array
L Macro 5.7
$YA=YB=YC=\overline{YD}=A+B$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB	175	175		
A,B	YC,YD	200	200		

Notes:
1. The default output follower current for each output is 0.96 ma. If the outputs are twinned, the user can select 1.92 ma.
2. The user should note that different R_{Sr}, R_{Sf} and K values apply for Hi-Drive Macros.

MACRO: 310 4-4-4-4 OR/AND
FULL CELL
1 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 5.7
H Macro 11.0

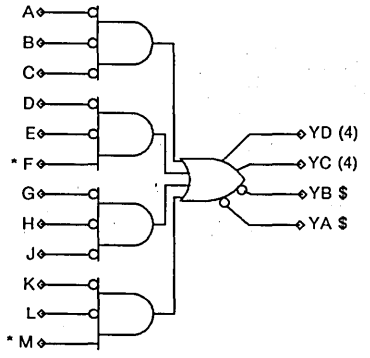
$YA=YB=\overline{YC}=\overline{YD}$

$YA=YB=(A+B+C+D) \bullet (C+D+E+F) \bullet (G+H+J+K) \bullet (J+K+L+M)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A..M	YA,YB	550	500	350	300
A..M	YC,YD	500	400	325	250

9

MACRO: 311 3-3-3-3 AND/OR
FULL CELL
2 LEVEL SERIES GATING

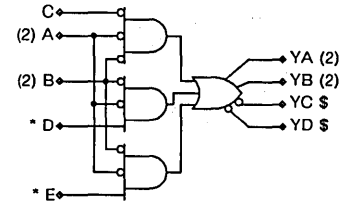


POWER: (mW)
LP Array
L Macro 7.3
H Macro 12.6
YA=YB=$\overline{YC}$=$\overline{YD}$

YA=YB=(A+B+C) • (D+E+$\overline{F}$) • (G+H+J) • (+K+L+$\overline{M}$)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C	YA,YB	525	500	325	300
A,B,C	YC,YD	400	300	275	200
D,E	YA,YB	550	300	350	225
D,E	YC,YD	350	300	225	225
G,H,J	YA,YB	525	250	350	175
G,H,J	YC,YD	300	325	200	225
K,L	YA,YB	500	200	350	150
K,L	YC,YD	300	350	200	225
F	YA,YB	625	525	400	325
F	YC,YD	450	375	300	275
M	YA,YB	675	400	450	250
M	YC,YD	375	400	250	300

MACRO: 312 3-3-3 AND/OR
1/2 CELL
2 LEVEL SERIES GATING

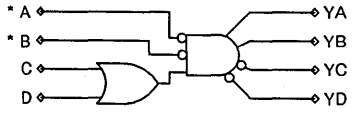


POWER: (mW)
LP Array
L Macro 3.7
H Macro 6.3

YC=YD=$\overline{YA}$= $\overline{YB}$=(C+A+B) • (B+A+$\overline{D}$) • (A+B+$\overline{E}$)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB	300	325	200	325
A,B	YC,YD	375	250	275	200
C	YA,YB	350	300	225	200
C	YC,YD	350	350	250	250
D,E	YA,YB	400	400	300	300
D,E	YC,YD	425	450	300	300

MACRO: 313 2-2 OR/AND
1/4 CELL
2 LEVEL SERIES GATING

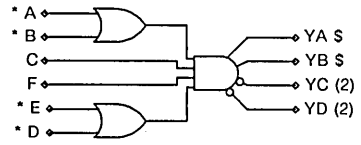


POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6

YA=YB=$\overline{YC}$= $\overline{YD}$=$\overline{A}$ • $\overline{B}$ • (C+D)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB	300	350	250	225
A,B	YC,YD	325	450	250	350
C,D	YA,YB	300	300	225	225
C,D	YC,YD	225	275	175	200

MACRO: 315 2-2-1-1 OR/AND
1/2 CELL
2 LEVEL SERIES GATING

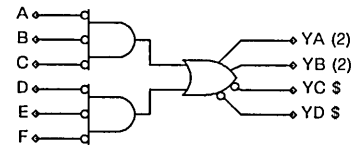


POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1

YA=YB=$\overline{YC}$= $\overline{YD}$=(A+B) • C • F • (E+D)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,D,E	YA,YB	625	725	375	450
A,B,D,E	YC,YD	300	275	250	200
C,F	YA,YB	650	475	400	350
C,F	YC,YD	225	300	200	200

MACRO: 318 3-3 AND/OR
1/2 CELL
1 LEVEL SERIES GATING

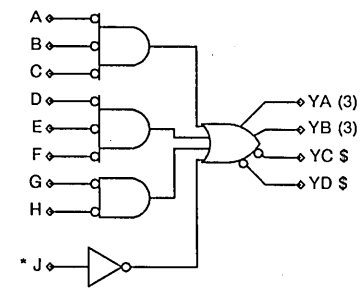


POWER: (mW)
LP Array
L Macro 2.9
H Macro 5.5

YC=YD=$\overline{YA}$= $\overline{YB}$=(A+B+C) • (D+E+F)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C	YA,YB	375	300	250	225
A,B,C	YC,YD	350	350	250	250
D,E,F	YA,YB	300	350	200	225
D,E,F	YC,YD	375	250	250	200

MACRO: 319 3-3-2-1 AND/OR
1/2 CELL
2 LEVEL SERIES GATING

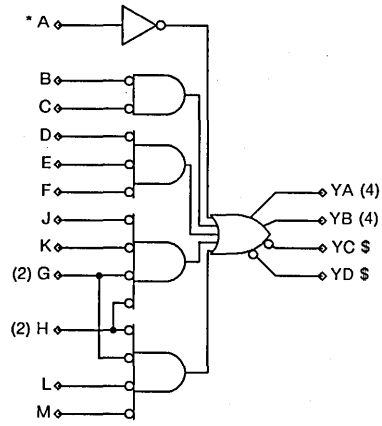


POWER: (mW)
LP Array
L Macro 5.1

YC=YD=$\overline{YA}$= $\overline{YB}$=(A+B+C) • (D+E+F) • (G+H) • J

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C	YA,YB	400	300		
A,B,C	YC,YD	525	500		
D,E,F	YA,YB	325	325		
D,E,F	YC,YD	550	325		
G,H	YA,YB	250	325		
G,H	YC,YD	525	250		
J	YA,YB	400	350		
J	YC,YD	525	500		

MACRO: 320 2-3-4-4 AND/OR W/ENABLE (HIGH)
FULL CELL
2 LEVEL SERIES GATING



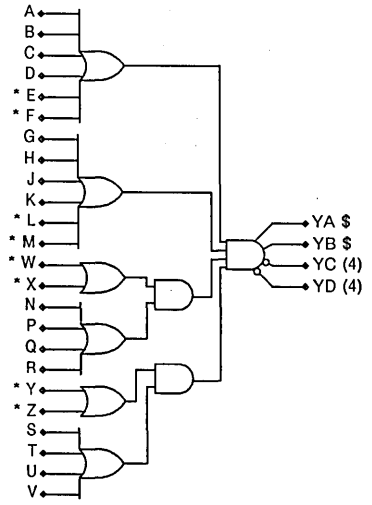
POWER: (mW)
LP Array
L Macro 6.5
H Macro 11.8

$YC = YD = \overline{YA} \cdot \overline{YB}$

$YC = YD = A \cdot (B+C) \cdot (D+E+F) \cdot (J+K+G+H) \cdot (G+H+L+M)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A	YA,YB	400	400	300	250
A	YC,YD	600	575	350	350
B..M	YA,YB	425	350	275	250
B..M	YC,YD	625	350	375	250

MACRO: 321 6-6-2-4-2-4 OR/AND
FULL CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 8.9
H Macro 14.2

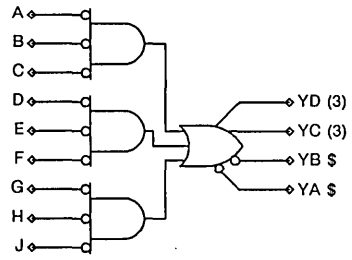
$YA = YB = \overline{YC} \cdot \overline{YD} \cdot$

$(A+B+C+D+E+F) \cdot (G+H+J+K+L+M) \cdot (N+P+Q+R) \cdot$

$(S+T+U+V) \cdot (W+X) \cdot (Y+Z)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D,G,H,J,K, N,P,Q,R,S,T,U,V	YA,YB	675	650	400	375
A,B,C,D,G,H,J,K, N,P,Q,R,S,T,U,V	YC,YD	575	375	350	250
E,F,L,M,W,X,Y,Z	YA,YB	775	850	450	500
E,F,L,M,W,X,Y,Z	YC,YD	625	350	400	250

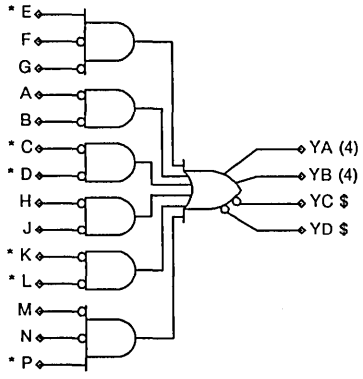
MACRO: 322 3-3-3 AND/OR
1/2 CELL
1 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 4.3
YA=YB=
$\overline{YC}$= $\overline{YD}$=(A+B+C) • (D+E+F) • (G+H+J)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
ALL	YA,YB	400	450		
ALL	YC,YD	325	400		

MACRO: 323 3-2-2-2-2-3 AND/OR
FULL CELL
2 LEVEL SERIES GATING



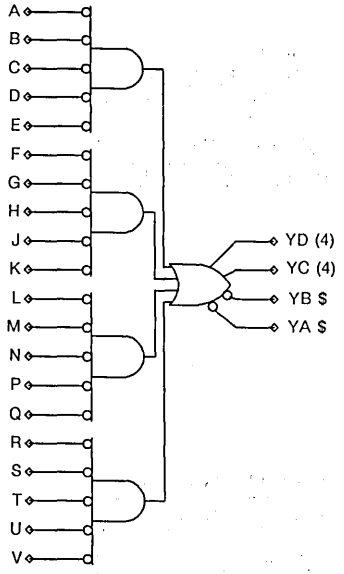
POWER: (mW)
LP Array
L Macro 8.9
H Macro 14.2

YC=YD=$\overline{YA}$= $\overline{YB}$

YC=YD=($\overline{E}$+F+G) • (A+B) • (C+D) • (H+J) • (K+L) • (M+N+$\overline{P}$)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,F,G,H,J,M,N	YA,YB	325	300	225	225
A,B,F,G,H,J,M,N	YC,YD	725	650	425	375
C,D,E,K,L,P	YA,YB	450	400	325	250
C,D,E,K,L,P	YC,YD	825	700	525	425

MACRO: 324 5-5-5-5 AND/OR
FULL CELL
1 LEVEL SERIES GATING

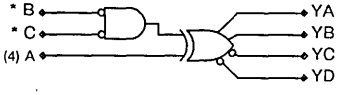


POWER: (mW)
LP Array
L Macro 8.9
H Macro 14.2

$YA=YB=\overline{YC}=\overline{YD}=(A+B+C+D+E) \bullet (F+G+H+J+K) \bullet (L+M+N+P+Q) \bullet (R+S+T+U+V)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A..V	YA,YB	525	500	350	300
A..V	YC,YD	600	450	350	275

MACRO: 328 2-1 AND/EXOR
HIGH DRIVE MACRO
1/2 CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		

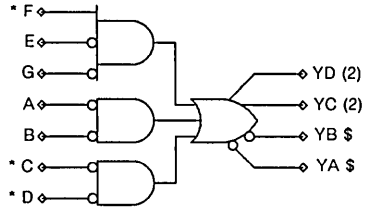
POWER: (mW)
LP Array
L Macro 6.5

$YA=YB=\overline{YC}=\overline{YD}=(\overline{B} \bullet \overline{C})\oplus A$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A	YA,YB	170	170		
A	YC,YD	170	170		
B,C	YA,YB	210	250		
B,C	YC,YD	190	260		

Notes:
1. The default output follower current for each output is 0.96 ma. If the outputs are twinned, the user can select 1.92 ma.
2. The user should note that different R_{Sr}, R_{Sf} and K values apply for Hi-Drive Macros.

MACRO: 331 3-2-2 AND/OR
1/2 CELL
2 LEVEL SERIES GATING

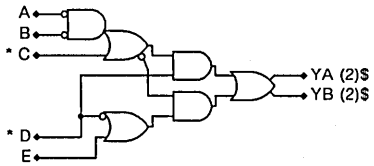


POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1

$YC=YD=\overline{YA}=\ \overline{YB}=(F \cdot \overline{E} \cdot \overline{G})+(\overline{A} \cdot \overline{B})+(\overline{C} \cdot \overline{D})$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
E,G	YA,YB	450	400	275	275
E,G	YC,YD	350	300	250	200
A,B	YA,YB	450	275	300	200
A,B	YC,YD	250	300	175	200
C,D	YA,YB	500	600	300	400
C,D	YC,YD	375	325	300	250
F	YA,YB	500	450	350	300
F	YC,YD	475	500	300	350

MACRO: 332 GATED OR
1/2 CELL
2 LEVEL SERIES GATING

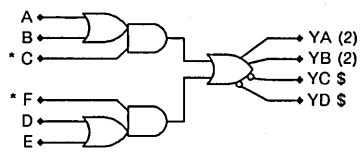


POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1

$YA=YB=(((\overline{A} \cdot \overline{B})+C) \cdot D)+\overline{(((\overline{A} \cdot \overline{B})+C) \cdot (\overline{D}+E))}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB	400	350	275	225
C	YA,YB	525	550	350	375
E	YA,YB	625	575	400	400
D	YA,YB	525	425	375	275

MACRO: 333 GATED OR
1/2 CELL
2 LEVEL SERIES GATING

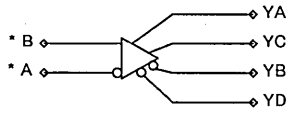


POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1

$YA=YB=\overline{YC}=\ \overline{YD}=((A+B) \cdot C)+(D+E) \cdot F)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB	350	275	250	200
A,B	YC,YD	450	425	275	275
D,E	YA,YB	300	300	200	225
D,E	YC,YD	450	275	300	200
C	YA,YB	375	400	250	300
C	YC,YD	575	500	375	300
F	YA,YB	300	450	200	325
F	YC,YD	600	350	425	250

MACRO: 370 DIFFERENTIAL LINE RECEIVER
1/4 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 3.0
H Macro 4.4

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB,YC,YD	125	200	100	200

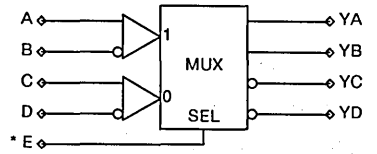
TRUTH TABLE

A	B	YA,YC	YB,YD
L	L	ND	ND
L	H	H	L
H	L	L	H
H	H	ND	ND

NOTE: ND = NOT DEFINED

9

MACRO: 371 2–1 MUX WITH DIFFERENTIAL INPUTS
1/4 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6

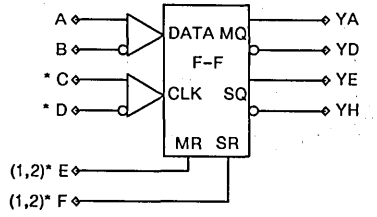
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	YA,YB	200	250	175	200
A,B,C,D	YC,YD	175	250	150	200
E	YA,YB	350	525	250	375
E	YC,YD	300	350	250	250

TRUTH TABLE

C	D	A	B	E	YA,YB	YC,YD
L	L	X	X	L	ND	ND
L	H	X	X	L	L	H
H	L	X	X	L	H	L
H	H	X	X	L	ND	ND
X	X	L	L	H	ND	ND
X	X	L	H	H	L	H
X	X	H	L	H	H	L
X	X	H	H	H	ND	ND

NOTE: ND = NOT DEFINED

MACRO: 372 D FLIP–FLOP WITH DIFFERENTIAL CLOCK AND DATA
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 9.3
H Macro 12.0

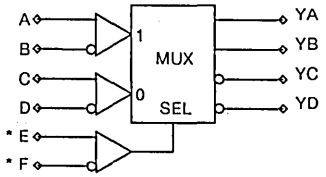
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA	300	300	200	250
A,B	YD	200	250	175	200
C,D	YA	350	450	275	350
C,D	YD	275	400	250	300
C,D	YE	350	500	275	375
C,D	YH	275	400	250	300
E	YA	--	550	--	400
E	YD	450	--	350	--
E	YH	850	--	650	--
E	YE	--	1050	--	750
F	YE	--	550	--	400
F	YH	450	--	350	--
SET UP		475		375	
MIN CLOCK PERIOD		1250		900	
MIN CLOCK PULSE WIDTH		625		450	
MIN RESET PULSE WIDTH		975		900	

TRUTH TABLE

MASTER RESET	SLAVE RESET	DATA		CLOCK		MASTER Q	SLAVE Q
E	F	A	B	C	D	YA	YE
L	L	X	X	H	L	--	--
L	L	L/H	H/L	L	H	L/H	--
L	L	L	H	L→H	H→L	L	L
L	L	H	L	L→H	H→L	H	H
H	X	X	X	H	L	L	L
H	L	L/H	H/L	L	H	L/H	--
X	H	L/H	H/L	L	H	L/H	L/L
L	H	X	X	H	L	--	--
H	H	H	L	L→H	H→L	⌥	⌤
X	X	L	H	L→H	H→L	L	L
H	L	H	L	L→H	H→L	⌥	⌤
L	H	H	L	L→H	H→L	H	⌟

NOTE: -- = NO CHANGE

MACRO: 373 2–TO–1 MUX WITH DIFF INPUTS AND DIFF MUX CONTROL
1/4 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 3.0
H Macro 4.4

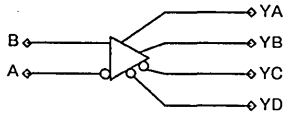
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	YA,YB,YC,YD	175	225	150	175
E,F	YA,YB,YC,YD	200	250	175	225

TRUTH TABLE

C	D	A	B	E	F	YA,YB	YC,YD
L	L	X	X	L	H	ND	ND
L	H	X	X	L	H	L	H
H	L	X	X	L	H	H	L
H	H	X	X	L	H	ND	ND
X	X	L	L	H	L	ND	ND
X	X	L	H	H	L	L	H
X	X	H	L	H	L	H	L
X	X	H	H	H	L	ND	ND
X	X	X	X	L	L	ND	ND
X	X	X	X	H	H	ND	ND

NOTE: ND = NOT DEFINED

MACRO: 374 DIFFERENTIAL LINE RECEIVER
1/4 CELL
1 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 1.4
H Macro 2.8

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB,YC,YD	150	200	150	175

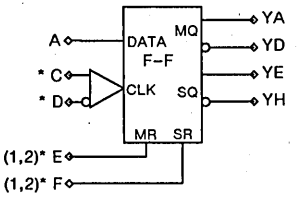
TRUTH TABLE

A	B	YA,YB	YC,YD
L	L	ND	ND
L	H	H	L
H	L	L	H
H	H	ND	ND

NOTE: ND = NOT DEFINED

9

MACRO: 375 D FLIP–FLOP WITH DIFFERENTIAL CLOCK
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 9.3
H Macro 12.0

MASTER Q=YA YH=$\overline{YE}$
SLAVE Q=YE YD=$\overline{YA}$

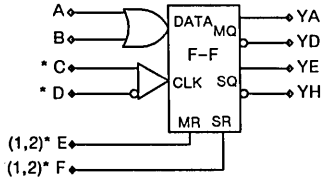
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A	YA	300	300	200	250
A	YD	200	250	175	200
C,D	YA	350	450	275	350
C,D	YD	275	400	250	300
C,D	YE	350	500	275	375
C,D	YH	275	400	250	300
E	YA	--	550	--	400
E	YD	450	--	350	--
E	YE	--	1050	--	750
E	YH	850	--	650	--
F	YE	--	550	--	400
F	YH	450	--	350	--
SET UP		475		375	
MIN CLOCK PERIOD		1250		900	
MIN CLK PSE WIDTH		625		450	
MIN RST PSE WIDTH		975		900	

TRUTH TABLE

MASTER RESET	SLAVE RESET	DATA	CLOCK		MASTER Q	SLAVE Q
E	F	A	C	D	YA	YE
L	L	X	H	L	--	--
L	L	L/H	L	H	L/H	--
L	L	L	L→H	H→L	L	L
L	L	H	L→H	H→L	H	H
H	X	X	H	L	L	L
H	L	L/H	L	H	L/H	--
X	H	L/H	L	H	L/H	L/L
L	H	X	H	L	--	--
H	H	H	L→H	H→L	⌥	⎍
X	X	L	L→H	H→L	L	L
H	L	H	L→H	H→L	⌥	⎍
L	H	H	L→H	H→L	H	⌿

NOTE: -- = NO CHANGE

MACRO: 376 D FLIP–FLOP WITH DIFFERENTIAL CLOCK
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 9.3
H Macro 12.0

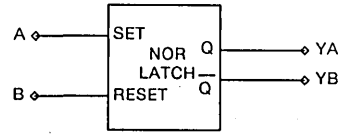
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA	300	300	200	250
A,B	YD	200	250	175	200
C,D	YA	350	450	275	350
C,D	YD	275	400	250	300
C,D	YE	350	500	275	375
C,D	YH	275	400	250	300
E	YA	--	550	--	400
E	YD	450	--	350	--
E	YE	--	1050	--	750
E	YH	850	--	650	--
F	YE	--	550	--	400
F	YH	450	--	350	--
SET UP		475		375	
MIN CLOCK PERIOD		1250		900	
MIN CLK PSE WIDTH		625		450	
MIN RST PSE WIDTH		975		900	
MIN RST RECRY TIME		625		450	

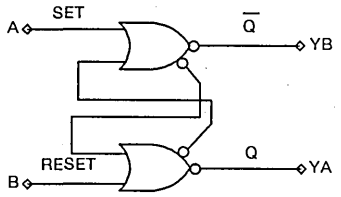
TRUTH TABLE

MASTER RESET	SLAVE RESET	DATA	CLOCK		MASTER Q	SLAVE Q
E	F	A+B	C	D	YA	YE
L	L	X	H	L	--	--
L	L	L/H	L	H	L/H	--
L	L	L	L→H	H→L	L	L
L	L	H	L→H	H→L	H	H
H	X	X	H	L	L	L
H	L	L/H	L	H	L/H	--
X	H	L/H	L	H	L/H	L/L
L	H	X	H	L	--	--
H	H	H	L→H	H→L	⌥	⎍
X	X	L	L→H	H→L	L	L
H	L	H	L→H	H→L	⌥	⎍
L	H	H	L→H	H→L	H	⌿

NOTE: -- = NO CHANGE

MACRO: 380 NOR LATCH
1/4 CELL
1 LEVEL SERIES GATING





LOGIC EQUIVALENT

POWER: (mW)
LP Array
L Macro 4.9

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A/B	YB/YA	525	--		
A/B	YA/YB	--	300		
MIN SET PULSE WIDTH		1075			
MIN RESET PULSE WIDTH		1075			

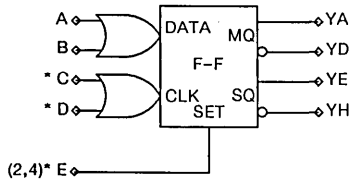
TRUTH TABLE

A	B	YA	YB
L	L	--	--
H	L	H	L
L	H	L	H
H	H	L	L

NOTE: -- = NO CHANGE

If A and B are simultaneously high, one input must not fall within 2.0ns (LPA) or 1.0ns (HPA) of the other.

MACRO: 381 D FLIP-FLOP WITH SET
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 8.1
H Macro 10.8

SET=E SLAVE Q=YE
DATA=(A+B) MASTER Q=YA
CLOCK= C+D YH=YE

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YD	400	400	275	300
C,D	YA,YD	400	625	300	425
C,D	YE,YH	350	425	250	275
E	YA,YD	525		375	
E	YE,YH	950		700	
SET UP		600		450	
MIN CLOCK PERIOD		2000		1500	
MIN CLOCK PULSE WIDTH		1000		750	
MIN SET PULSE WIDTH		1075		825	
MIN SET RECOVERY TIME		1000		750	

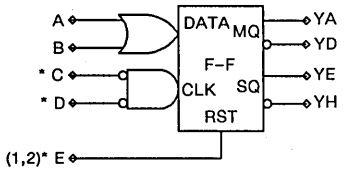
TRUTH TABLE

SET	DATA	CLOCK	MASTER Q	SLAVE Q
E	A+B	C+D	YA	YE
L	X	H	--	--
L	L	L	L	--
L	L	L→H	L	L
L	H	L	H	--
L	H	L→H	H	H
H	X	H	H	H
H	L	L	L	H
H	L	L→H	L→H	⅄
H	H	L	H	H
H	H	L→H	H	H

NOTE: -- = NO CHANGE

9

MACRO: 391 D FLIP–FLOP, NEGATIVE EDGE TRIGGERED
1/2 CELL
2 LEVEL SERIES GATING



TRUTH TABLE

RESET	DATA	~CLOCK	MASTER Q	SLAVE Q
E	A+B	C+D	YA	YE
L	X	L	--	--
L	L	H	L	--
L	L	H→L	L	L
L	H	H	H	--
L	H	H→L	H	H
H	X	L	L	L
H	L	H	L	--
H	L	H→L	L	L
H	H	H	H	--
H	H	H→L	L	⊓

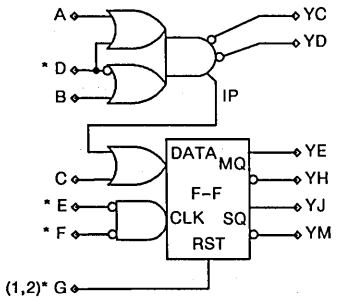
NOTE: -- = NO CHANGE

POWER: (mW)
LP Array
L Macro 8.1
H Macro 10.8

$YD=\overline{YA}$ $YH=\overline{YE}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YD	400	400	250	250
C,D	YA,YD	425	525	300	350
C,D	YE,YH	300	500	225	375
E	YA	--	525	--	375
E	YD	525	--	375	--
E	YH	925	--	700	--
E	YE	--	925	--	700
SET UP		600		450	
MIN CLOCK PERIOD		2000		1500	
MIN CLOCK PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	

MACRO: 392 D FLIP–FLOP WITH MUX, NEGATIVE EDGE TRIGGERED
3/4 CELL
2 LEVEL SERIES GATING



TRUTH TABLE

RESET	DATA	E+F	MASTER Q	SLAVE Q
L	X	L	--	--
L	L	H	L	--
L	L	H→L	L	L
L	H	H	H	--
L	H	H→L	H	H
H	X	L	L	L
H	L	H	L	--
H	L	H→L	L	L
H	H	H	H	--
H	H	H→L	L	⊓

NOTE: -- = NO CHANGE

POWER: (mW)
LP Array
L Macro 11.4
H Macro 15.3

RESET=G SLAVE Q=YJ

DATA=(A+D) • (C+$\overline{D}$)+C YH= $\overline{YE}$

YC=YD=$\overline{((A+D) \bullet (B+\overline{D}))}$ YM= $\overline{YJ}$

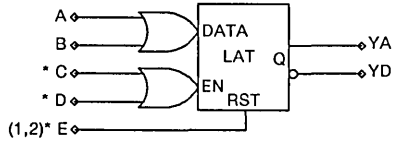
CLK = $\overline{E} \bullet \overline{F}$ MASTER Q=YE

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YC,YD	250	275	175	200
C,IP	YE,YH	400	400	250	250
G	YE	--	525	--	375
G	YH	525	--	375	--
G	YJ	--	925	--	700
G	YM	925	--	700	--
E,F	YE,YH	425	525	300	350
E,F	YJ,YM	300	500	225	375
D	YC,YD	350	475	250	350
A,B	IP	275	250	200	175
D	IP	475	350	350	250
C, IP TO CLOCK SET UP TIME		600		450	
MIN CLOCK PERIOD		2000		1500	
MIN CLOCK PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	

NOTE: Delay from A,B to IP and D to IP must be added to the SETUP time in the delay table and subtracted from the HOLD time of 0 ps.

9

MACRO: 393 D LATCH WITH CLOCK ENABLE (HIGH)
1/4 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 4.7
H Macro 6.0

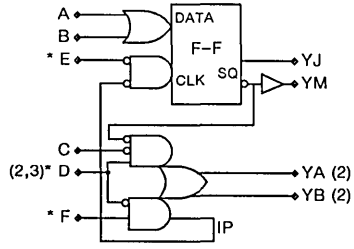
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YD	400	400	250	250
C,D	YA,YD	425	525	300	350
E	YA	--	525	--	375
E	YD	525	--	375	--
SET UP TIME		600		450	
MIN CLK PSE WIDTH		1000		750	
MIN RST PSE WIDTH		1075		825	

TRUTH TABLE

RESET	DATA	ENABLE		Q
E	A+B	C	D	YA
L	X	L	L	-
H	X	L	L	L
X	L	H	X	L
X	H	X	H	H

NOTE: -- = NO CHANGE

MACRO: 394 D FLIP-FLOP WITH MUX,NEGATIVE EDGE TRIGGERED
FULL CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 13.6
H Macro 18.9

$YA = YB = (\overline{D} \cdot F) + (D \cdot \overline{C} \cdot YJ)$

$YM = \overline{YJ}$

	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
D	1	1	

TRUTH TABLE

DATA	$\overline{\text{CLOCK}}$	SLAVE Q
A+B	$(\overline{D} \cdot F)+E$	YJ
X	L	--
L	H	--
L	H→L	L
H	H	--
H	H→L	H

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
C	YA,YB	425	350	275	250
D	YA,YB	325	300	250	225
D	YJ	625	875	500	650
D	YM	625	775	500	575
D	IP	325	300	250	225
F	IP	350	350	250	250
F	YA,YB	350	350	250	250
F	YJ	650	925	500	675
F	YM	650	825	500	600
E	YA,YB	925	625	675	425
E	YJ	300	575	250	425
E	YM	300	475	250	350
A,B TO CLK E, IP SET UP TIME		600		450	
MIN CLOCK PERIOD		2000		1500	
MIN CLOCK PULSE WIDTH		1000		750	

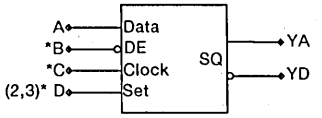
TRUTH TABLE

C	D	F	YA,YB
L	L	L	L
L	L	H	H
L	H	L	YJ
L	H	H	YJ
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	L

9

MACRO: 395 D FLIP-FLOP WITH ASYN SET AND DATA ENABLE

FULL CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
D	1	1	

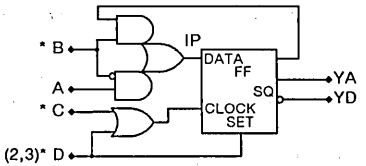
TRUTH TABLE

A	B	D	C	SQ (n+1)
L	L	L→H	L	*
X	X	L→H	H	H
H	X	L→H	X	H
X	X	H	X	H
X	X	L	L	--
X	X	L	H	--
X	H	L	L→H	--
L	L	L	L→H	L
H	L	L	L→H	H

*NOTE: A negative glitch occurs due to set input -- = NO CHANGE

POWER: (mW)
LP Array
L Macro 11.4
H Macro 15.3

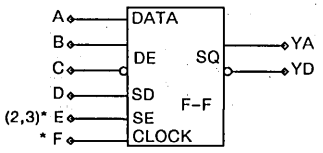
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
C	YA	350	450	225	300
D	YA	775	--	525	--
D	YD	--	775	--	525
C	YD	450	350	300	225
A	IP	300	300	200	225
B	IP	450	450	300	325
IP TO C SET UP		600		450	
MIN CLOCK PERIOD		2000		1500	
MIN CLOCK PULSE WIDTH		1000		750	
MIN SET PULSE WIDTH		1075		825	
MIN SET RECOVERY TIME		1000		750	



LOGIC EQUIVALENT

MACRO: 396 SCAN D FLIP-FLOP

FULL CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
E	1	1	

TRUTH TABLE

E	C	B	F	Q (n+1)
L	L	L	L→H	Q (n)·A
L	L	H	L→H	A
L	H	L	L→H	--
L	H	H	L→H	H
H	L	L	L→H	D
H	L	H	L→H	D
H	H	L	L→H	D
H	H	H	L→H	D

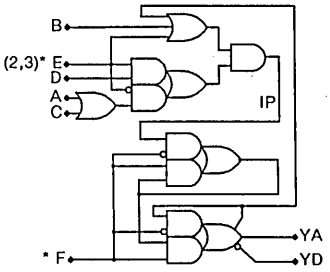
NOTE: -- = NO CHANGE

NOTE: If B and C are complement of each other, then: IP = $(AB + SQ \cdot \overline{B}) \cdot \overline{E} + D \cdot E$

IP = $(Data \cdot DE + SQ \cdot \overline{DE})\overline{SE} + SD \cdot SE$

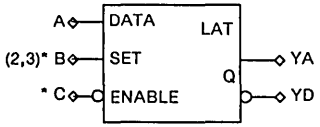
POWER: (mW)
LP Array
L Macro 12.8
H Macro 18.1

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
F	YA	350	525	225	300
F	YD	450	350	225	250
C,A,D	IP	400	375	275	250
E	IP	450	550	300	375
B	IP	425	400	275	250
IP TO F SET UP		600		450	
MIN CLOCK PERIOD		2000		1500	
MIN CLOCK PULSE WIDTH		1000		750	



LOGIC EQUIVALENT

MACRO: 397 D LATCH WITH ASYN SET
1/4 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 4.7
H Macro 6.0

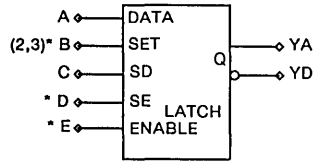
	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
B	1	1	

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(−)	(+)	(−)
A	YA	300	300	225	325
A	YD	350	350	225	225
B	YA	400	500	300	350
B	YD	425	525	325	325
C	YA	350	500	250	350
C	YD	425	575	300	400
A TO C SET UP TIME		600		450	
MIN ENABLE PULSE WIDTH		1000		750	
MIN SET PULSE WIDTH		1075		825	

TRUTH TABLE

B	C	A	Q (n+1)
H	X	X	H
L	H	X	Q (n)
L	L	A	DATA(A)

MACRO: 398 SCAN D LATCH WITH ASYN SET
1/2 CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
B	1	1	

TRUTH TABLE

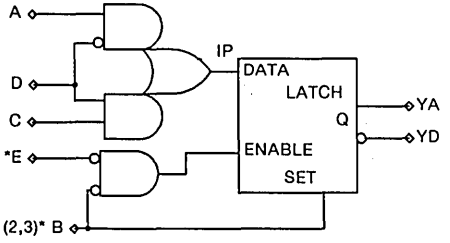
B	D	E	A	C	Q (n+1)
H	X	X	X	X	H
L	X	H	X	X	Q (n)
L	L	L	L	X	L
L	H	L	X	L	L
L	L	L	H	X	H
L	H	L	X	H	H

POWER: (mW)
LP Array
L Macro 7.9
H Macro 10.6

IP= A • $\overline{D}$+C • D

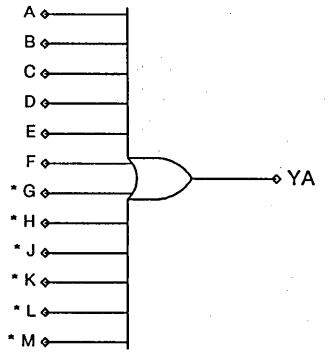
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(−)	(+)	(−)
B	YA,YD	400	500	300	325
E	YA,YD	525	525	325	325
A,C	YA,YD	600	600	400	400
A,C	IP	300	300	200	200
D	YA,YD	750	750	475	475
D	IP	450	450	275	275
SET UP (IP TO E)		600		450	
MIN CLOCK PERIOD		2000		1500	
MIN CLOCK PULSE WIDTH		1000		750	

NOTE:
A and C inputs are MUXED into the data input of the latch with D as the select. Setup time listed is from the MUX output (IP) to E.



LOGIC EQUIVALENT

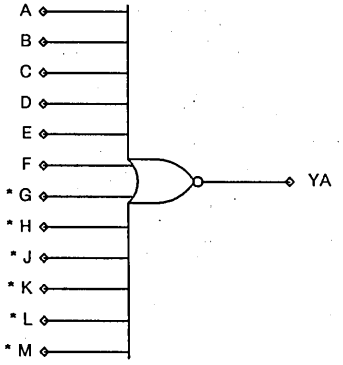
MACRO: 400 12–INPUT OR
1/4 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6
YA=A+B+C+D+E+F+G+H+J+K+L+M

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D,E,F	YA	225	250	175	175
G,H,J,K,L,M	YA	300	400	225	300

MACRO: 401 12–INPUT NOR
1/4 CELL
2 LEVEL SERIES GATING

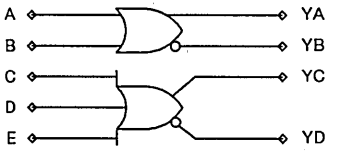


POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6

$YA=\overline{A+B+C+D+E+F+G+H+J+K+L+M}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D,E,F	YA	750	650	425	375
G,H,J,K,L,M	YA	750	650	450	375

MACRO: 402 2–INPUT OR/NOR 3–INPUT OR/NOR
1/4 CELL
1 LEVEL SERIES GATING

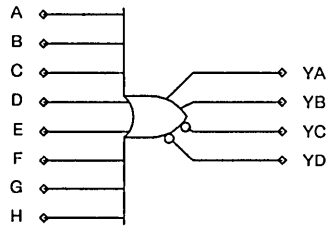


POWER: (mW)
LP Array
L Macro 2.9

$YA=\overline{YB}=A+B$ $YC=\overline{YD}=C+D+E$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA	200	225		
A,B	YB	250	225		
C,D,E	YC	200	225		
C,D,E	YD	325	300		

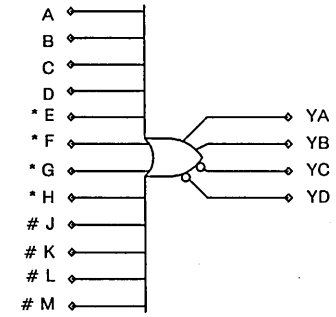
MACRO: 403 8–INPUT OR/NOR
1/4 CELL
1 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 1.4
H Macro 2.8
$YA=\overline{YB}=\overline{YC}=\overline{YD}=A+B+C+D+E+F+G+H$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D,E,F,G,H	YA,YB	225	250	175	200
A,B,C,D,E,F,G,H	YC,YD	800	725	475	400

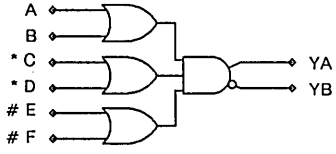
MACRO: 404 12–INPUT NOR
1/2 CELL
3 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4
$YA=\overline{YB}=\overline{YC}=\overline{YD}=A+B+C+D+E+F+G+H+J+K+L+M$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	YA,YB	225	250	150	175
A,B,C,D	YC,YD	650	575	375	350
E,F,G,H	YA,YB	250	400	200	300
E,F,G,H	YC,YD	750	700	450	375
J,K,L,M	YA,YB	300	575	200	425
J,K,L,M	YC,YD	800	775	525	400

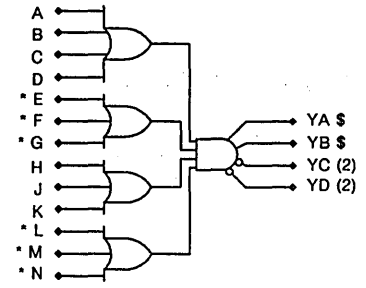
MACRO: 411 2–2–2 OR/AND
1/4 CELL
3 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4
$YA=\overline{YB}=(A+B)\bullet(C+D)\bullet(E+F)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA	375	350	250	250
A,B	YB	200	250	150	175
C,D	YA	325	400	225	300
C,D	YB	300	325	250	225
E,F	YA	300	450	200	350
E,F	YB	400	400	325	275

MACRO: 413 4-3-3-3 OR/AND
1/2 CELL
2 LEVEL SERIES GATING

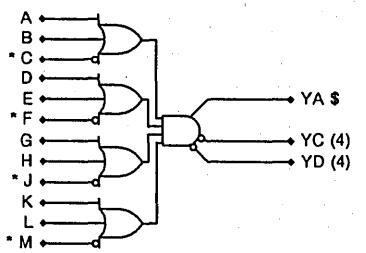


POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1
$YA=\overline{YB}=\overline{YC}=\overline{YD}=$

$(A+B+C+D) \cdot (E+F+G) \cdot (H+J+K) \cdot (L+M+N)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D,H,J,K	YA,YB	525	500	325	300
A,B,C,D,H,L,K	YC,YD	425	350	275	225
E,F,G,L,M,N	YA,YB	575	675	350	450
E,F,G,L,M,N	YC,YD	525	400	350	275

MACRO: 414 3-3-3-3 OR/AND
1/2 CELL
2 LEVEL SERIES GATING

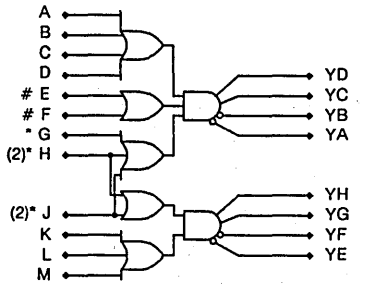


POWER: (mW)
LP Array
L Macro 8.9

$YA=\overline{YC}=\overline{YD}=(A+B+\overline{C}) \cdot (D+E+\overline{F}) \cdot (G+H+\overline{J}) \cdot (K+L+\overline{M})$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,D,E,G,H,K,L	YA	675	650		
A,B,D,E,G,H,K,L	YC,YD	550	425		
C,F,J,M	YA	550	750		
C,F,J,M	YC,YD	600	500		

MACRO: 416 4-2-3-2-3 OR/AND
FULL CELL
3 LEVEL SERIES GATING



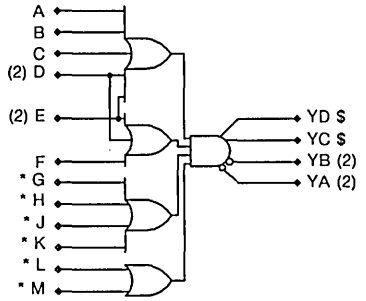
POWER: (mW)
LP Array
L Macro 5.3
H Macro 8.0

$\overline{YA}=\overline{YB}=YC=YD=(A+B+C+D) \cdot (E+F) \cdot (G+H+J)$

$\overline{YE}=\overline{YF}=YG=YH=(H+J) \cdot (K+L+M)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D	YA,YB	400	375	250	250
A,B,C,D	YC,YD	375	375	250	250
G,H,J	YA,YB	475	450	325	300
G,H,J	YC,YD	325	400	225	275
E,F	YA,YB	600	525	425	350
E,F	YC,YD	325	450	200	350
H,J	YE,YF	400	400	300	275
H,J	YG,YH	250	325	200	250
K,L,M	YE,YF	300	300	200	225
K,L,M	YG,YH	300	325	200	225

MACRO: 417 5-3-4-2 OR/AND
1/2 CELL
2 LEVEL SERIES GATING

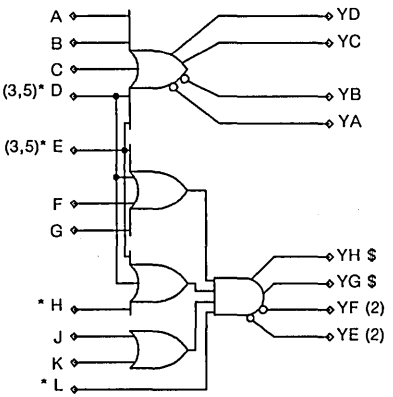


POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1

$YC=YD=\overline{YA}=\overline{YB}=(A+B+C+D+E) \bullet (G+H+J+K) \bullet (D+E+F) \bullet (L+M)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D,E,F	YA,YB	500	400	325	250
A,B,C,D,E,F	YC,YD	525	500	325	300
L,M,G,H,J,K	YA,YB	600	475	400	300
L,M,G,H,J,K	YC,YD	575	675	350	425

MACRO: 418 5-4-3-2-1 OR/AND
3/4 CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
D	2	1	
E	2	1	

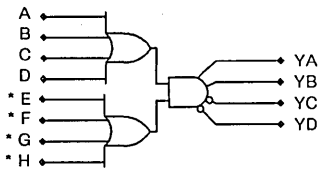
POWER: (mW)
LP Array
L Macro 5.9
H Macro 9.9

$YC=YD=\overline{YA}=\overline{YB}=(A+B+C+D+E)$

$YG=YH=\overline{YE}=\overline{YF}=(D+E+F+G) \bullet (D+E+H) \bullet (J+K) \bullet L$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D,E	YA,YB	525	475	325	300
A,B,C,D,E	YC,YD	225	250	175	200
J,K	YG,YH	550	500	325	300
J,K	YE,YF	275	250	200	175
L	YG,YH	575	700	350	450
L	YE,YF	375	325	275	225
D,E,F,G,H	YG,YH	575	575	350	350
D,E,F,G,H	YE,YF	350	400	225	250

MACRO: 419 4-4 OR/AND
1/4 CELL
2 LEVEL SERIES GATING



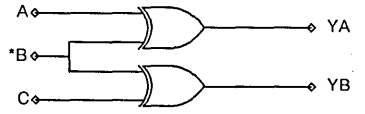
POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6

$YA=YB=\overline{YC}=\overline{YD}=(A+B+C+D) \bullet (E+F+G+H)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D	YA,YB	425	450	300	300
A,B,C,D	YC,YD	550	525	350	350
E,F,G,H	YA,YB	400	500	275	375
E,F,G,H	YC,YD	675	650	450	425

9

MACRO: 421 DUAL EXOR
1/4 CELL
2 LEVEL SERIES GATING



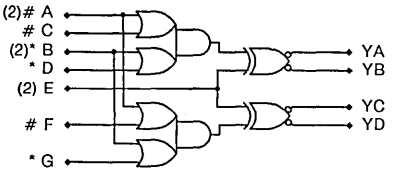
	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		
C	1.5		

POWER: (mW)
LP Array
L Macro 3.7

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,C	YA,YB	325	350		
B	YA,YB	400	600		

YA=A⊕B
YB=B⊕C

MACRO: 422 DUAL 2–2 OR/AND/EXNOR
1/2 CELL
3 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
E	3		

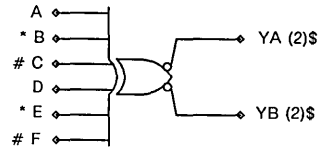
POWER: (mW)
LP Array
L Macro 6.2
H Macro 8.9

$YA=YB=\overline{((A+C) \cdot (B+D))} \oplus E$

$YC=YD=\overline{((A+F) \cdot (B+G))} \oplus E$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
E	YA,YB,YC,YD	425	375	275	275
B,D,G	YA,YB,YC,YD	525	600	325	400
A,C,F	YA,YB,YC,YD	450	775	300	500

MACRO: 424 6–INPUT EXNOR
1/2 CELL
3 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		
D	1.5		

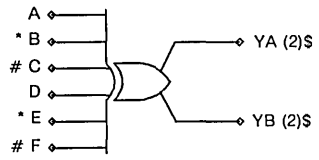
POWER: (mW)
LP Array
L Macro 6.2
H Macro 8.9

$YA=YB=\overline{A \oplus B \oplus C \oplus D \oplus E \oplus F}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,D	YA,YB	575	450	350	300
B,E	YA,YB	650	725	400	475
C,F	YA,YB	725	925	425	600

9

MACRO: 425 6-INPUT EXOR
1/2 CELL
3 LEVEL SERIES GATING

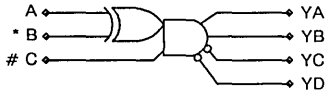


	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		
D	1.5		

POWER: (mW)
LP Array
L Macro 6.2
H Macro 8.9
YA=YB=A⊕B⊕C⊕D⊕E⊕F

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,D	YA,YB	575	450	350	300
B,E	YA,YB	650	725	400	475
C,F	YA,YB	725	925	425	600

MACRO: 427 2-1 EXOR/AND/NAND
1/4 CELL
3 LEVEL SERIES GATING

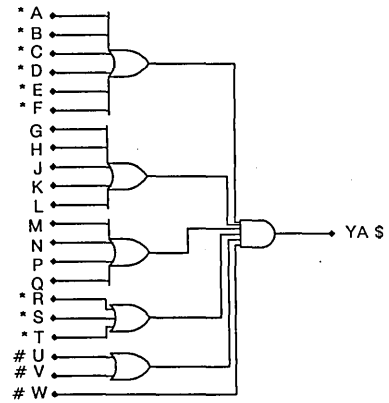


	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		

POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4
YA=YB=$\overline{YC}$=$\overline{YD}$=(A⊕B) • C

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A	YA,YB	350	350	250	250
A	YC,YD	225	275	175	200
B	YA,YB	425	525	300	375
B	YC,YD	300	400	250	275
C	YA,YB	450	650	300	450
C	YC,YD	400	400	300	275

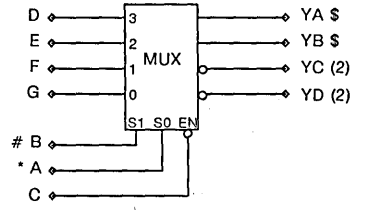
MACRO: 438 6-5-4-3-2-1 OR/AND
1/2 CELL
3 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 6.2
H Macro 8.9
YA=(A+B+C+D+E+F) • (G+H+J+K+L) •
(M+N+P+Q) • (R+S+T) • (U+V) • W

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
G,H,J,K,L,M,N,P,Q	YA	850	850	500	500
A,B,C,D,E,R,S,T	YA	825	850	500	550
U,V,W	YA	800	900	475	575

MACRO: 451 4–1 MUX W/ENABLE(LOW)
1/2 CELL
3 LEVEL SERIES GATING



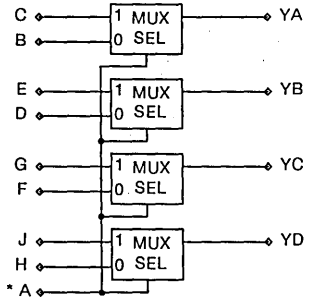
POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.2

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
D,E,F,G	YA,YB	650	575	375	350
D,E,F,G	YC,YD	450	375	300	250
C	YA,YB	700	625	400	375
C	YC,YD	225	225	175	150
A	YA,YB	700	800	450	500
A	YC,YD	575	575	400	400
B	YA,YB	775	900	500	575
B	YC,YD	650	700	450	500

TRUTH TABLE

C	B	A	YA,YB	YC,YD
H	X	X	L	H
L	L	L	G	$\overline{G}$
L	L	H	F	$\overline{F}$
L	H	L	E	$\overline{E}$
L	H	H	D	$\overline{D}$

MACRO: 452 QUAD 2–TO–1 MUX
1/2 CELL
2 LEVEL SERIES GATING
LOW POWER MACRO ONLY



POWER: (mW)
LP Array
L Macro 6.5

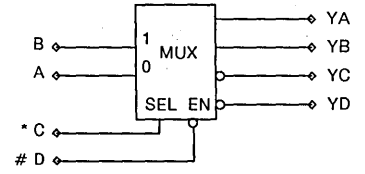
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
B,C	YA	300	300		
A	YA	350	550		

TRUTH TABLE

A	YA	YB	YC	YD
L	B	D	F	H
H	C	E	G	J

NOTE: YA delays also apply to the other three MUXes

MACRO: 453 2–TO–1 MUX W/ENABLE(LOW)
1/4 CELL
3 LEVEL SERIES GATING



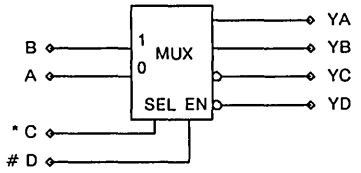
POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB	375	350	250	250
A,B	YC,YD	225	275	175	200
C	YA,YB	400	450	300	275
C	YC,YD	325	450	225	325
D	YA,YB	350	250	275	175
D	YC,YD	425	625	275	450

TRUTH TABLE

D	C	YA,YB	YC,YD
H	X	L	H
L	L	A	$\overline{A}$
L	H	B	$\overline{B}$

MACRO: 454 2–TO–1 MUX W/ENABLE(HIGH)
1/4 CELL
3 LEVEL SERIES GATING



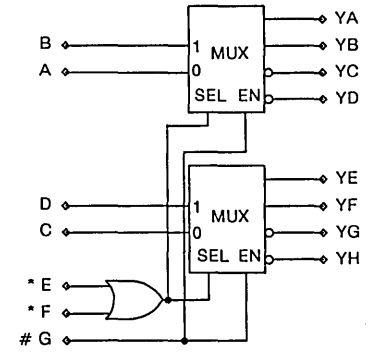
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB	375	350	250	250
A,B	YC,YD	225	275	175	200
C	YA,YB	400	450	300	275
C	YC,YD	325	450	225	325
D	YA,YB	325	450	200	350
D	YC,YD	425	425	325	300

TRUTH TABLE

D	C	YA,YB	YC,YD
L	X	L	H
H	L	A	$\overline{A}$
H	H	B	$\overline{B}$

POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4

MACRO: 455 DUAL 2–TO–1 MUX W/ENABLE (HIGH)
1/2 CELL
3 LEVEL SERIES GATING



MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB	375	350	250	250
A,B	YC,YD	250	225	200	175
G	YA,YB	450	525	300	375
G	YC,YD	475	325	350	250
E,F	YA,YB	325	475	225	375
E,F	YC,YD	500	450	300	350

TRUTH TABLE

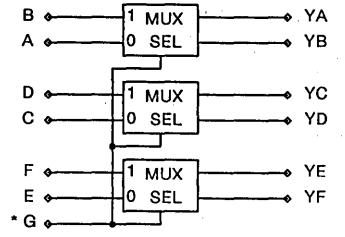
E+F	G	YA,YB	YC,YD	YE,YF	YG,YH
X	L	L	H	L	H
L	H	A	$\overline{A}$	C	$\overline{C}$
H	H	B	$\overline{B}$	D	$\overline{D}$

NOTE: Delays for YE,YF,YG, and YH are the same as those listed for YA,YB,YC, and YD.

POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.2

9

MACRO: 456 TRIPLE 2–TO–1 MUX(COMMON SELECT)
1/2 CELL
2 LEVEL SERIES GATING



MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB	300	300		
G	ALL	350	500		

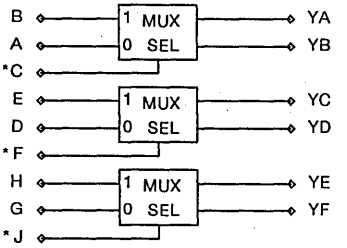
NOTE: Delays for D,C to YC, YD and E,F to YE,YF are the same as those listed for A,B to YA,YB.

TRUTH TABLE

G	YA,YB	YC,YD	YE,YF
L	A	C	E
H	B	D	F

POWER: (mW)
LP Array
L Macro 5.1

MACRO: 457 TRIPLE 2–TO–1 MUX
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 6.7

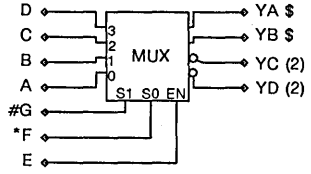
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB	300	300		
C	YA,YB	350	450		

NOTE: Delays for the other two MUX's are the same as those listed above.

TRUTH TABLE

C,F,J	YA,YB	YC,YD	YE,YF
L	A	D	G
H	B	E	H

MACRO: 458 4–1 MUX W/ENABLE(HIGH)
1/2 CELL
3 LEVEL SERIES GATING



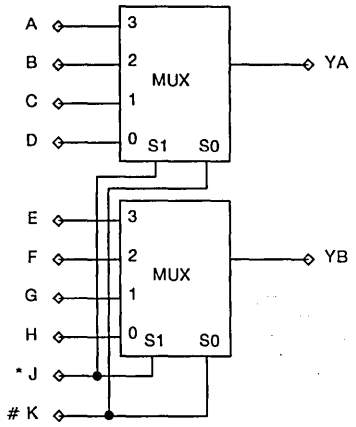
POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.2

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	YA,YB	650	575	375	350
A,B,C,D	YC,YD	450	375	300	250
E	YA,YB	650	575	375	325
E	YC,YD	275	225	200	175
F	YA,YB	700	800	450	500
F	YC,YD	575	575	400	400
G	YA,YB	775	900	500	575
G	YC,YD	650	700	450	500

TRUTH TABLE

E	G	F	YA,YB	YC,YD
L	X	X	L	H
H	L	L	A	$\overline{A}$
H	L	H	B	$\overline{B}$
H	H	L	C	$\overline{C}$
H	H	H	D	$\overline{D}$

MACRO: 459 DUAL 4–1 MUX
1/2 CELL
3 LEVEL SERIES GATING



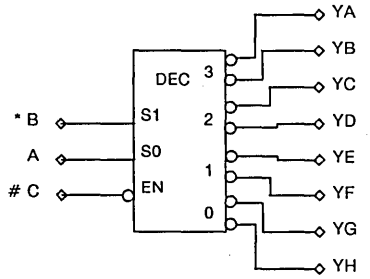
POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.2

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	YA	575	500	350	300
E,F,G,H	YB	575	500	350	300
J	YA,YB	650	800	425	525
K	YA,YB	725	1100	450	650

TRUTH TABLE

J	K	YA	YB
L	L	D	H
L	H	C	G
H	L	B	F
H	H	A	E

MACRO: 461 1–OF–4 DECODER WITH ENABLE(LOW)
1/2 CELL
3 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		

POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4

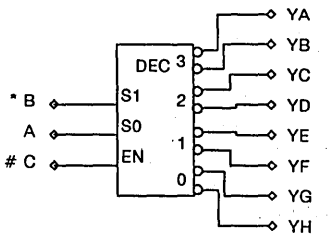
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A	ALL	225	225	175	175
B	ALL	225	275	200	200
C	ALL	300	550	250	425

TRUTH TABLE

C	B	A	YA,YB	YC,YD	YE,YF	YG,YH
H	X	X	H	H	H	H
L	L	L	H	H	H	L
L	L	H	H	H	L	H
L	H	L	H	L	H	H
L	H	H	L	H	H	H

9

MACRO: 462 1-OF-4 DECODER WITH ENABLE(HIGH)
1/2 CELL
3 LEVEL SERIES GATING



POWER: (mW)

	LP Array
L Macro	3.1
H Macro	4.4

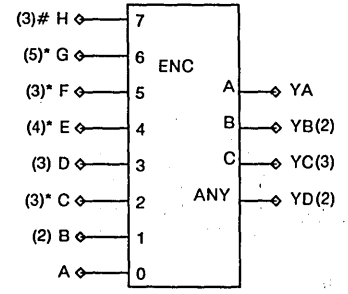
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A	ALL	225	225	175	175
B	ALL	200	275	200	200
C	ALL	350	450	300	375

TRUTH TABLE

C	B	A	YA,YB	YC,YD	YE,YF	YG,YH
L	X	X	H	H	H	H
H	L	L	H	H	H	L
H	L	H	H	H	L	H
H	H	L	H	L	H	H
H	H	H	L	H	H	H

	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		

MACRO: 464 8-3 ENCODER
FULL CELL
3 LEVEL SERIES GATING
LOW POWER ONLY



POWER: (mW)

	LP Array
L Macro	12.6

YA=E+F+G+H

$YC=\overline{(C+E+G)} \cdot B+\overline{(E+G)} \cdot D+\overline{G} \cdot F+H$

$YB=((C+D) \cdot \overline{(E+F)})+(G+H)$

YD=A+B+C+D+E+F+G+H

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
ALL	YD	250	275		
E,F,G,H	YA	275	350		
E,F	YB	275	225		
C,D	YB	325	300		
G,H	YB	250	250		
B,D	YC	375	300		
E,C	YC	325	225		
F	YC	350	275		
H	YC	425	500		
G	YC	275	225		

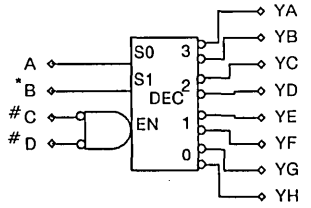
TRUTH TABLE

A	B	C	D	E	F	G	H	YA	YB	YC	YD
X	X	X	X	X	X	X	H	H	H	H	H
X	X	X	X	X	X	H	L	H	H	L	H
X	X	X	X	X	H	L	L	H	L	H	H
X	X	X	X	H	L	L	L	H	L	L	H
X	X	X	H	L	L	L	L	L	H	H	H
X	X	H	L	L	L	L	L	L	H	L	H
X	H	L	L	L	L	L	L	L	L	H	H
H	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L

	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
C	2	1	
E	1	3	
F	2	1	
G	2	3	
H	2		1

MACRO: 465 1-OF-4 DECODER WITH ENABLE(LOW)
1/2 CELL
3 LEVEL SERIES GATING

POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4



MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A	ALL	200	225	175	175
B	ALL	225	375	175	300
C,D	ALL	400	575	300	425

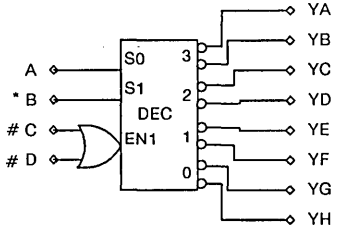
TRUTH TABLE

D	C	B	A	YA,YB	YC,YD	YE,YF	YG,YH
X	H	X	X	H	H	H	H
H	X	X	X	H	H	H	H
L	L	L	L	H	H	H	L
L	L	L	H	H	H	L	H
L	L	H	L	H	L	H	H
L	L	H	H	L	H	H	H

	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		

MACRO: 466 1-OF-4 DECODER WITH ENABLE(HIGH)
1/2 CELL
3 LEVEL SERIES GATING

POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4



MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A	ALL	200	225	175	175
B	ALL	200	275	200	200
C,D	ALL	350	450	300	375

TRUTH TABLE

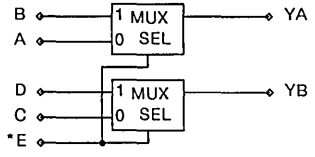
EN1	B	A	YA,YB	YC,YD	YE,YF	YG,YH
L	X	X	H	H	H	H
H	L	L	H	H	H	L
H	L	H	H	H	L	H
H	H	L	H	L	H	H
H	H	H	L	H	H	H

EN1=C + D

	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		

MACRO: 470 DUAL 2-TO-1 MUX (COMMON SELECT)
1/4 CELL
2 LEVEL SERIES GATING

POWER: (mW)
LP Array
L Macro 3.7

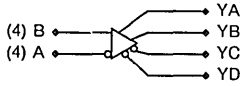


MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D	YA,YB	300	300		
E	YA,YB	325	475		

TRUTH TABLE

E	YA	YB
L	A	C
H	B	D

MACRO: 474 DIFFERENTIAL LINE RECEIVER
HI DRIVE MACRO
1/2 CELL
1 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1		
B	1		

POWER: (mW)
LP Array
L Macro 5.7

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB,YC,YD	100	150		

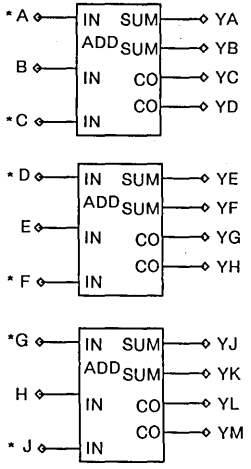
Notes:
1. The default output follower current for each output is 0.96 ma. If the outputs are twinned, the user can select 1.92 ma.
2. The user should note that different R_{Sr}, R_{Sf} and K values apply for Hi-Drive Macros.

TRUTH TABLE

A	B	YA,YB	YC,YD
L	L	ND	ND
L	H	H	L
H	L	L	H
H	H	ND	ND

NOTE: ND = NOT DEFINED

MACRO: 482 TRIPLE FULL ADDER
FULL CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
B	1.5		
E	1.5		
H	1.5		

POWER: (mW)
LP Array
L Macro 16.4

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A	YA,YB	350	350		
A	YC,YD	350	525		
B	YA,YB	600	700		
B	YC,YD	675	775		
C	YA,YB	800	900		
C	YC,YD	750	975		

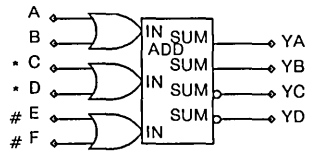
TRUTH TABLE

A	B	C	SUM	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

NOTE: Truth Table is the same for all three adders

9

MACRO: 485 3-BIT ADDER
1/2 CELL
3 LEVEL SERIES GATING



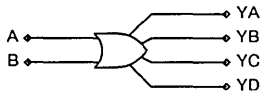
	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		
B	1.5		

POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4

$YA=YB=\overline{YC}=\overline{YD}=(A+B)\oplus(C+D)\oplus(E+F)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB,YC,YD	400	425	275	275
C,D	YA,YB,YC,YD	550	475	400	325
E,F	YA,YB,YC,YD	750	525	525	400

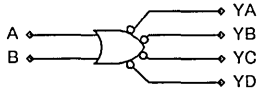
MACRO: 501 2 INPUT OR QUAD BUFFER
1/4 CELL
1 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 1.4
H Macro 2.8
YA=YB=YC=YD=A+B

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB,YC,YD	275	300	200	225

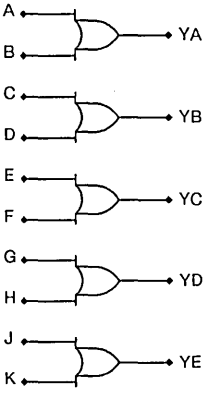
MACRO: 502 2 INPUT NOR QUAD BUFFER
1/4 CELL
1 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 1.4
H Macro 2.8
$YA=YB=YC=YD=\overline{A+B}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB,YC,YD	325	300	225	200

MACRO: 503 5x2 INPUT OR
1/2 CELL
1 LEVEL SERIES GATING



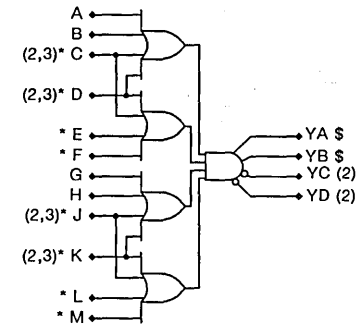
POWER: (mW)
LP Array
L Macro 7.1

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA	250	250		

YA = A + B
YB = C + D
YC = E + F
YD = G + H
YE = J + K

9

MACRO: 510 4-4-4-4 OR/AND
1/2 CELL
2 LEVEL SERIES GATING



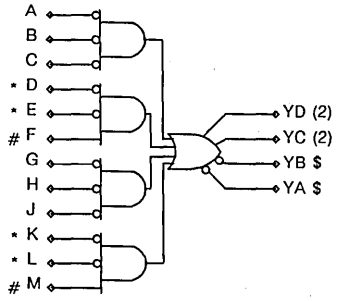
POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1

$YA=YB=\overline{YC}=\overline{YD}=(A+B+C+D) \bullet (C+D+E+F) \bullet (G+H+J+K) \bullet (J+K+L+M)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D,G,H,J,K	YA,YB	525	500	325	300
A,B,C,D,G,H,J,K	YC,YD	400	325	250	225
E,F,L,M	YA,YB	550	675	350	450
E,F,L,M	YC,YD	550	450	400	300

	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
C	1	1	
D	1	1	
J	1	1	
K	1	1	

MACRO: 511 3-3-3-3 AND/OR
1/2 CELL
3 LEVEL SERIES GATING



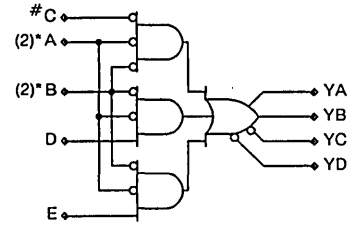
POWER: (mW)
LP Array
L Macro 6.2
H Macro 8.9

$YA=YB=\overline{YC}=\overline{YD}=(A+B+C) \bullet (D+E+\overline{F}) \bullet (G+H+J) \bullet (K+L+\overline{M})$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,G,H,J	YA,YB	375	400	250	275
A,B,C,G,H,J	YC,YD	275	300	175	200
D,E,L,K	YA,YB	350	550	250	375
D,E,L,K	YC,YD	425	450	300	300
F,M	YA,YB	400	425	300	300
F,M	YC,YD	500	675	325	475

9

MACRO: 512 3-3-3 AND/OR
1/2 CELL
3 LEVEL SERIES GATING



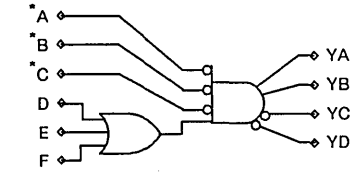
	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	0	1	1
B	0	1	1

POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4

$YC\text{-}YD\text{-}\overline{YA}\text{-}\overline{YB}\text{-}(C+A+B) \bullet (B+A+\overline{D}) \bullet (A+B+\overline{E})$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB	300	350	250	225
A,B	YC,YD	450	650	300	425
C	YA,YB	475	500	375	300
C	YC,YD	350	500	250	375
D,E	YA,YB	300	300	225	225
D,E	YC,YD	325	350	225	225

MACRO: 513 3-1-1-1 OR/AND
1/4 CELL
2 LEVEL SERIES GATING

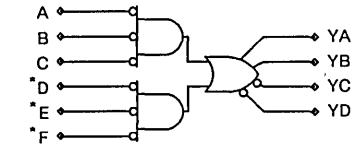


POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6

$YA\text{-}YB\text{-}\overline{YC}\text{-}\overline{YD}\text{-}\overline{A} \bullet \overline{B} \bullet \overline{C} \bullet (D+E+F)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C	YA,YB	350	375	250	250
A,B,C	YC,YD	350	475	250	350
D,E,F	YA,YB	325	350	250	250
D,E,F	YC,YD	250	300	200	200

MACRO: 518 3-3 AND/OR
1/4 CELL
2 LEVEL SERIES GATING

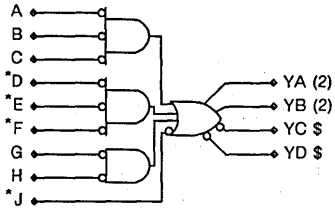


POWER: (mW)
LP Array
L Macro 2.2
H Macro 3.6

$YC\text{-}YD\text{-}\overline{YA}\text{-}\overline{YB}\text{-}(A+B+C) \bullet (D+E+F)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C	YA,YB	300	300	225	200
A,B,C	YC,YD	325	300	225	200
D,E,F	YA,YB	475	325	350	225
D,E,F	YC,YD	400	375	250	275

MACRO: 519 3-3-2-1 AND/OR
1/2 CELL
2 LEVEL SERIES GATING

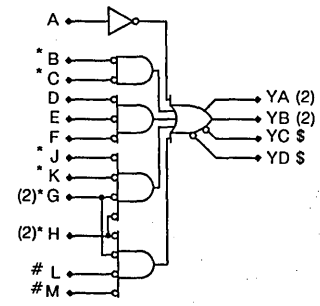


POWER: (mW)
LP Array
L Macro 4.5
H Macro 7.1

$YC = YD = \overline{YA} = \overline{YB} = (A+B+C) \cdot (D+E+F) \cdot (G+H) \cdot J$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,G,H	YA,YB	375	300	250	200
A,B,C,G,H	YC,YD	575	500	350	325
D,E,F,J	YA,YB	450	375	325	250
D,E,F,J	YC,YD	625	725	375	450

MACRO: 520 2-3-4-4 AND/OR W/ENABLE(HIGH)
1/2 CELL
3 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 5.3
H Macro 8.0

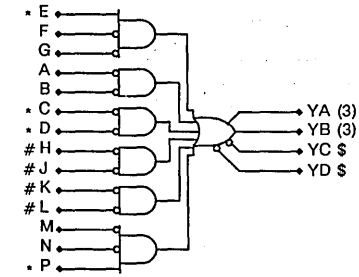
$YC = YD = \overline{YA} = \overline{YB}$

$YC = YD = A \cdot (B+C) \cdot (D+E+F) \cdot (J+K+G+H) \cdot (G+H+L+M)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,D,E,F	YA,YB	375	300	250	225
A,D,E,F	YC,YD	700	600	400	350
B,C,J,K	YA,YB	300	300	250	200
B,C,J,K	YC,YD	750	825	425	500
G,H,L,M	YA,YB	375	425	250	300
G,H,L,M	YC,YD	700	1000	400	550

	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
G	0	1	1
H	0	1	1

MACRO: 523 3-2-2-2-2-3 AND/OR
FULL CELL
3 LEVEL SERIES GATING

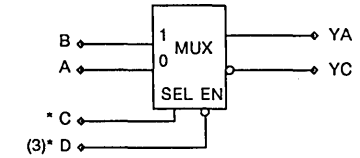


POWER: (mW)
LP Array
L Macro 8.4
H Macro 12.4

$YA = YB = \overline{YC} = \overline{YD} = (E \cdot \overline{F} \cdot \overline{G}) + (\overline{A} \cdot \overline{B}) + (\overline{C} \cdot \overline{D}) + (\overline{J} \cdot \overline{H}) + (\overline{K} \cdot \overline{L}) + (\overline{M} \cdot \overline{N} \cdot P)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,M,N,F,G	YA,YB	450	375	300	250
A,B,M,N,F,G	YC,YD	950	850	550	500
C,D,E,P	YA,YB	550	450	400	325
C,D,E,P	YC,YD	1000	1100	600	650
H,J,K,L	YA,YB	675	525	500	375
H,J,K,L	YC,YD	1125	2325	625	1375

MACRO: 553 2 to 1 MUX W/ENABLE(LOW)
1/4 CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
D	1	1	

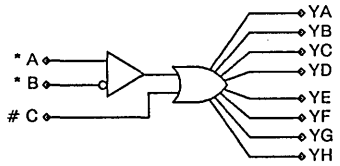
POWER: (mW)
LP Array
H Macro 3.6

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YC			300	275
C,D	YA,YC			350	425

TRUTH TABLE

D	C	YA	YC
H	X	L	H
L	L	A	$\overline{A}$
L	H	B	$\overline{B}$

Macro: 571 8 OUTPUT BUFFER W/DIFF INPUT AND ENABLE
QUAD BUFFER
1/2 CELL
3 LEVEL SERIES GATING



NOTE: The structure of this macro is essentially a dual QUAD buffer and, hence, all QUAD buffer output characteristics apply.

POWER: (mW)
LP Array
L Macro 5.3
H Macro 8.0
YA-YB-YC-YD-YE-YF-YG-YH

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA-YH	275	300	200	225
C	YA-YH	575	775	350	525

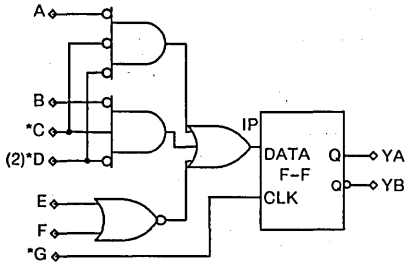
TRUTH TABLE

A	B	C	YA
L	L	L	ND
L	H	L	L
H	L	L	H
H	H	L	ND
X	X	H	H

NOTE: ND = NOT DEFINED

9

MACRO: 585 SCAN D FLIP–FLOP W/2 to 1 MUX/OR
1/2 CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
D	1	1	

POWER: (mW)
LP Array
L Macro 13.6

IP = DATA
IP = $(\overline{A} \cdot \overline{C} \cdot \overline{D})+(\overline{B} \cdot C \cdot \overline{D})+(\overline{E} \cdot \overline{F})$

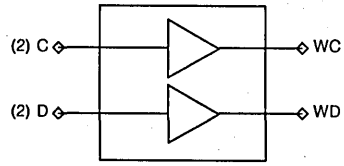
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	IP	425	400		
C,D	IP	525	625		
E,F	IP	250	225		
G	YA,YB	350	425		
IP TO CLK SET UP		600			
MIN CLOCK PERIOD		2000			
MIN CLOCK PULSE WIDTH		1000			

TRUTH TABLE

DATA	CLK	YA	YB
X	L	––	––
X	H	––	––
L	L→H	L	H
H	L→H	H	L
X	H→L	––	––

NOTE: –– = NO CHANGE

Macro: 593 W BUFFER
1/4 CELL
1 LEVEL SERIES GATING



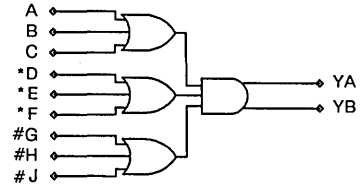
V_{EEE} POWER: (mW)
LP Array
L Macro 8.3

V_{EEE} CURRENT: (mA/output)
LP Array
0 .96

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
C,D	WC,WD	0	0		

Note: The 593 contains two emitter followers with 0.96mA pulldowns to V_{EEE}. The output follower current is always on. The R_{Sr} and R_{Sf} are for H macro with twin outputs. The DC fanout limits are for an L macro wiith single output. This macro is used to interface to the clock inputs of 895 macro or the select and enable inputs of 851,852,853.

MACRO: 611 3–3–3 OR/AND
1/4 CELL
3 LEVEL SERIES GATING

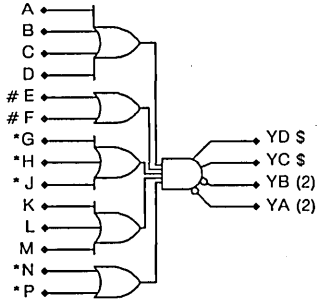


POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4

YA=YB=(A+B+C) • (D+E+F) • (G+H+J)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C	YA,YB	525	550	350	325
D,E,F	YA,YB	475	550	325	400
G,H,J	YA,YB	450	625	300	450

MACRO: 616 4-2-3-3-2 OR/AND
1/2 CELL
3 LEVEL SERIES GATING

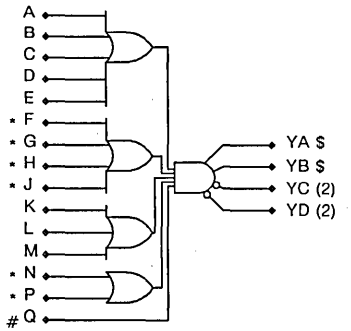


POWER: (mW)
LP Array
L Macro 5.3
H Macro 8.0

$YC=YD=\overline{YA}=\overline{YB}=(A+B+C+D) \cdot (E+F) \cdot (G+H+J) \cdot (K+L+M) \cdot (N+P)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D,K,L,M	YA,YB	650	600	375	350
A,B,C,D,K,L,M	YC,YD	450	350	275	250
G,H,J,N,P	YA,YB	600	625	350	400
G,H,J,N,P	YC,YD	550	425	375	275
E,F	YA,YB	600	675	350	450
E,F	YC,YD	575	450	400	300

MACRO: 618 5-4-3-2-1 OR/AND
1/2 CELL
3 LEVEL SERIES GATING

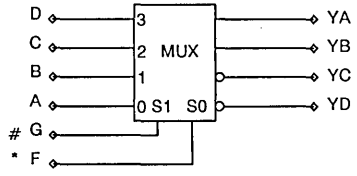


POWER: (mW)
LP Array
L Macro 5.3
H Macro 8.0

$YA=YB=\overline{YC}=\overline{YD}=(A+B+C+D+E) \cdot (F+G+H+J) \cdot (K+L+M) \cdot (N+P) \cdot Q$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D,E,K,L,M	YA,YB	625	600	375	350
A,B,C,D,E,K,L,M	YC,YD	550	400	325	250
F,G,H,J,N,P	YA,YB	600	600	350	400
F,G,H,J,N,P	YC,YD	650	500	400	300
Q	YA,YB	600	650	350	425
Q	YC,YD	575	450	400	300

MACRO: 658 4-1 MUX
1/2 CELL
3 LEVEL SERIES GATING



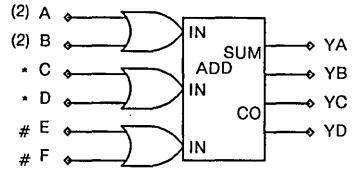
POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D	YA,YB	475	450	300	275
A,B,C,D	YC,YD	425	400	250	250
F	YA,YB	525	600	325	400
F	YC,YD	525	550	350	325
G	YA,YB	575	775	350	525
G	YC,YD	600	700	400	400

TRUTH TABLE

G	F	YA,YB	YC,YD
L	L	A	$\overline{A}$
L	H	B	$\overline{B}$
H	L	C	$\overline{C}$
H	H	D	$\overline{D}$

MACRO: 685 FULL ADDER W/GATED INPUTS
1/2 CELL
3 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	2.5		
B	2.5		

POWER: (mW)
LP Array
L Macro 6.2
H Macro 8.9

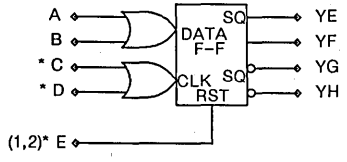
YA=YB=(A+B)⊕(C+D)⊕(E+F)
YC=YD=(A+B)(C+D)+(A+B)(E+F)+(C+D)(E+F)

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB	500	525	350	350
C,D	YA,YB	575	800	400	600
E,F	YA,YB	700	1000	475	700
A-F	YC,YD	350	775	250	550

TRUTH TABLE

A+B	C+D	E+F	YA,YB	YC,YD
L	L	L	L	L
H	L	L	H	L
L	H	L	H	L
H	H	L	L	H
L	L	H	H	L
H	L	H	L	H
L	H	H	L	H
H	H	H	H	H

MACRO: 691 D FLIP-FLOP W/RESET
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 8.1
H Macro 10.8

SLAVE Q= YE=YF=$\overline{YG}$=$\overline{YH}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
C,D	YE,YF,YG,YH	350	425	250	275
E	YE,YF,YG,YH	950		700	
SET UP		600		450	
MIN CLOCK PERIOD		2000		1500	
MIN CLOCK PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	

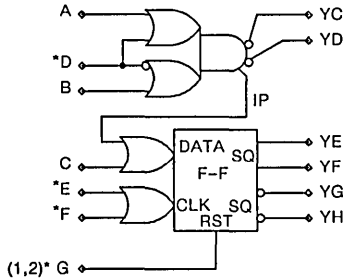
TRUTH TABLE

RESET	DATA	CLOCK	SLAVE Q
E	A+B	C+D	YE,YF
L	X	L	--
L	X	H	--
L	L	L→H	L
L	H	L→H	H
H	X	H	L
H	X	L	--
H	L	L→H	L
H	H	L→H	⊓

NOTE: -- = NO CHANGE

9

MACRO: 692 D FLIP–FLOP WITH MUX
3/4 CELL
2 LEVEL SERIES GATING



TRUTH TABLE

RESET	DATA	CLOCK	SLAVE Q
G	C+IP	E+F	YE,YF
L	X	L	--
L	X	H	--
L	L	L→H	L
L	H	L→H	H
H	X	H	L
H	X	L	--
H	L	L→H	L
H	H	L→H	⎍

NOTE: -- = NO CHANGE

POWER: (mW)

	LP Array
L Macro	11.4
H Macro	15.3

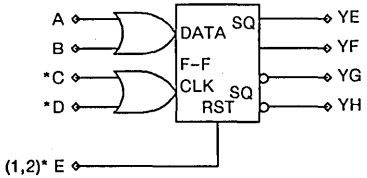
RESET=G

DATA= (A+D) • (B+$\overline{D}$)+C
CLOCK=E+F
SLAVE Q =YE=YF=$\overline{YG}$=$\overline{YH}$

YC=YD= $\overline{(A+D) \cdot (B+\overline{D})}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YC,YD	250	275	175	200
D	YC,YD	350	475	250	350
E,F	YE,YF,YG,YH	350	425	250	275
G	YE,YF,YG,YH	950		700	
A,B	IP	300	300	225	225
D	IP	325	450	250	350
C, IP TO CLOCK SET UP TIME		600		450	
MIN CLOCK PERIOD		2000		1500	
MIN CLOCK PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	

MACRO: 694 D FLIP–FLOP W/RESET (NEGATIVE HOLD TIME)
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)

	LP Array
L Macro	8.1
H Macro	10.8

SLAVE Q = YE=YF=$\overline{YG}$=$\overline{YH}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
C,D	YE,YF,YG,YH	350	425	250	275
E	YE,YF,YG,YH	950		700	
SET UP		700		500	
MIN CLOCK PERIOD		2000		1500	
MIN CLOCK PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	
HOLD		-100		-50	

TRUTH TABLE

RESET	DATA	CLOCK	SLAVE Q
E	A+B	C+D	YE,YF
L	X	L	--
L	X	H	--
L	L	L→H	L
L	H	L→H	H
H	X	H	L
H	X	L	--
H	L	L→H	L
H	H	L→H	⎍

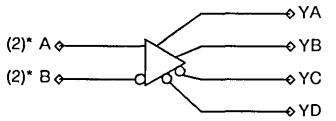
NOTE: -- = NO CHANGE

NOTE: This macro is essentially a 691 with delay inserted in the data path.

9

HI SPEED DIFFERENTIAL INPUT MACROS (L700 – L799)

MACRO: 700 DIFFERENTIAL LINE RECEIVER
HI DRIVE MACRO
1/2 CELL
1 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	Actual Capacitance
A	1		0.09 pF
B	1		0.09 pF

POWER: (mW)
LP Array
L Macro 10.6

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB	125	125		
A,B	YC,YD	100	150		

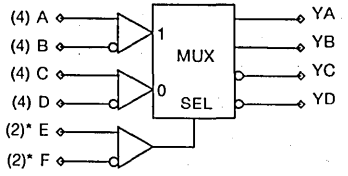
Notes:
1. The default output follower current for each output is 0.96 ma. If the outputs are twinned, the user can select 1.92 ma.
2. The user should note that different R_{sr}, R_{sf} and K values apply for Hi-Drive Macros.

TRUTH TABLE

A	B	YA,YB	YC,YD
L	L	ND	ND
L	H	L	H
H	L	H	L
H	H	ND	ND

NOTE: ND = NOT DEFINED

MACRO: 701 2–TO–1 MUX WITH DIFF INPUTS AND DIFF MUX CONTROL
HI DRIVE MACRO
1/2 CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	Actual Capacitance
A	1		0.12 pF
B	1		0.12 pF
C	1		0.12 pF
D	1		0.12 pF
E		1	0.07 pF
F		1	0.07 pF

POWER: (mW)
LP Array
L Macro 10.6

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	YA,YB,YC,YD	100	125		
E,F	YA,YB,YC,YD	150	200		

Notes:
1. The default output follower current for each output is 0.96 ma. If the outputs are twinned, the user can select 1.92 ma.
2. The user should note that different R_{sr}, R_{sf} and K values apply for Hi-Drive Macros.

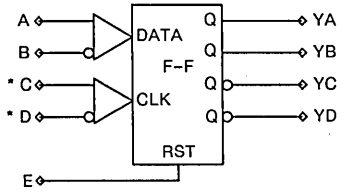
TRUTH TABLE

C	D	A	B	E	F	YA,YB	YC,YD
L	L	X	X	L	H	ND	ND
L	H	X	X	L	H	L	H
H	L	X	X	L	H	H	L
H	H	X	X	L	H	ND	ND
X	X	L	L	H	L	ND	ND
X	X	L	H	H	L	L	H
X	X	H	L	H	L	H	L
X	X	H	H	H	L	ND	ND
X	X	X	X	L	L	ND	ND
X	X	X	X	H	H	ND	ND

NOTE: ND = NOT DEFINED

MACRO: 710 D FLIP–FLOP WITH DIFFERENTIAL CLOCK AND DATA
1/2 CELL
2 LEVEL SERIES GATING

POWER: (mW)
LP Array
H Macro 16.0



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	Actual Capacitance
A	1		0.09 pF
B	1		0.09 pF
C		1	0.07 pF
D		1	0.07 pF
E	1		0.09 pF

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
C,D	YA,YB,YC,YD			300	300
E	YA,YB			--	575
E	YC,YD			575	--
MIN CLOCK PULSE WIDTH				300	
MIN RESET PULSE WIDTH				550	
DATA SET UP				200	
DATA HOLD				100	
MIN RESET HOLD				100	
MIN RESET RECOVERY				200	

Notes:
1. The default output follower current for each output is 0.48 ma. If the outputs are twinned, the user can select 0.96 ma.
2. Minimum reset hold time is the minimum amount of time that RESET must be be held 'high' after the CLOCK switches from a 'low' to a 'high' in order for the flip-flop to remain in the reset state.
3. It should be noted that the Master portion of the flip-flop is asynchronously reset when the RESET line is 'high'. This reset scheme eliminates the possibility of an output glitch for the condition:
RESET = 'H', DATA = 'H', and the CLOCK transitions from 'L'→'H'.

TRUTH TABLE

RESET	DATA		CLOCK		Q
E	A	B	C	D	YA
L	X	X	H	L	--
L	X	X	L	H	--
L	L	H	L→H	H→L	L
L	H	L	L→H	H→L	H
H	X	X	H	L	L
H	X	X	L	H	--
H	H	L	L→H	H→L	L

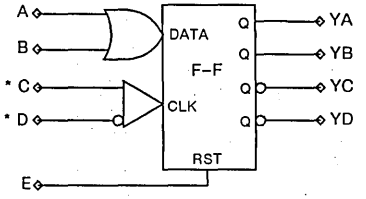
NOTE: -- = NO CHANGE

9

MACRO: 711 D FLIP–FLOP WITH GATED DATA INPUT AND DIFFERENTIAL CLOCK

1/2 CELL
2 LEVEL SERIES GATING

POWER: (mW)
LP Array
H Macro 16.0



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	Actual Capacitance
A	1		0.09 pF
B	1		0.09 pF
C		1	0.07 pF
D		1	0.07 pF
E	1		0.09 pF

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
C,D	YA,YB			300	350
C,D	YC,YD			300	325
E	YA,YB			--	575
E	YC,YD			575	
MIN CLOCK PULSE WIDTH				300	
MIN RESET PULSE WIDTH				550	
DATA SET UP				200	
DATA HOLD				100	
MIN RESET HOLD				100	
MIN RESET RECOVERY				200	

Notes:
1. The default output follower current for each output is 0.48 ma. If the outputs are twinned, the user can select 0.96 ma.
2. Minimum reset hold time is the minimum amount of time that RESET must be be held 'high' after the CLOCK switches from a 'low' to a 'high' in order for the flip–flop to remain in the reset state.
3. It should be noted that the Master portion of the flip–flop is asynchronously reset when the RESET line is 'high'. This reset scheme eliminates the possibility of an output glitch for the condition:
RESET = 'H', DATA = 'H', and the CLOCK transitions from 'L'→'H'.

TRUTH TABLE

RESET	DATA	CLOCK		Q
E	A+B	C	D	YA
L	X	H	L	--
L	X	L	H	--
L	L	L→H	H→L	L
L	H	L→H	H→L	H
H	X	H	L	L
H	X	L	H	--
H	H	L→H	H→L	L

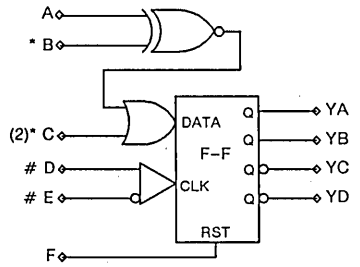
NOTE: -- = NO CHANGE

9

MACRO: 712 D FLIP–FLOP WITH EXNOR GATED DATA INPUT AND DIFFERENTIAL CLOCK

1 FULL CELL
3 LEVEL SERIES GATING

POWER: (mW)
LP Array
H Macro 20.36



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd or 3rd LEVEL	Actual Capacitance
A	1.5		0.12 pF
B		1	0.07 pF
C	1	1	0.19 pF
D		1	0.07 pF
E		1	0.07 pF
F	1		0.09 pF

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
D,E	YA,YB,YC,YD			300	325
F	YA,YB			--	425
F	YC,YD			425	--
MIN CLOCK PULSE WIDTH				300	
MIN RESET PULSE WIDTH				550	
DATA SET UP				200	
DATA HOLD				100	
MIN RESET HOLD				100	
MIN RESET RECOVERY				200	

Notes:
1. The default output follower current for each output is 0.48 ma. If the outputs are twinned, the user can select 0.96 ma.
2. Minimum reset hold time is the minimum amount of time that RESET must be be held 'high' after the CLOCK switches from a 'low' to a 'high' in order for the flip-flop to remain in the reset state.
3. It should be noted that the Master portion of the flip-flop is asynchronously reset when the RESET line is 'high'. This reset scheme eliminates the possibility of an output glitch for the condition:
RESET = 'H', DATA = 'H', and the CLOCK transitions from 'L'→'H'.

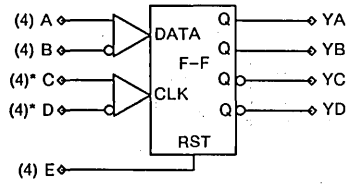
TRUTH TABLE

RESET	DATA	CLOCK		Q
F	$C+\overline{(A \oplus B)}$	D	E	YA
L	X	H	L	--
L	X	L	H	--
L	L	L→H	H→L	L
L	H	L→H	H→L	H
H	X	H	L	L
H	X	L	H	--
H	H	L→H	H→L	L

NOTE: -- = NO CHANGE

9

MACRO: 713 D FLIP–FLOP WITH DIFFERENTIAL CLOCK AND DATA
HI DRIVE MACRO
FULL CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	Actual Capacitance
A	1		0.12 pF
B	1		0.12 pF
C		2	0.10 pF
D		2	0.10 pF
E	1		0.12 pF

POWER: (mW)

	LP Array
L Macro	32.0

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
C,D	YA,YB,YC,YD	200	200		
E	YA,YB	--	375		
E	YC,YD	375	--		
MIN CLOCK PULSE WIDTH		200			
MIN RESET PULSE WIDTH		350			
DATA SET UP		100			
DATA HOLD		75			
MIN RESET HOLD		75			
MIN RESET RECOVERY		100			

Notes:
1. The default output follower current for each output is 0.96 ma. If the outputs are twinned, the user can select 1.92 ma.
2. The user should note that different R_{sr}, R_{sf} and K values apply for Hi-Drive Macros.
3. Minimum reset hold time is the minimum amount of time that RESET must be be held 'high' after the CLOCK switches from a 'low' to a 'high' in order for the flip-flop to remain in the reset state.
4. It should be noted that the Master portion of the flip-flop is asynchronously reset when the RESET line is 'high'. This reset scheme eliminates the possibility of an output glitch for the condition:
RESET = 'H', DATA = 'H', and the CLOCK transitions from 'L'→'H'.

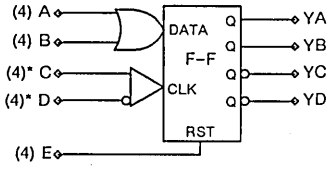
TRUTH TABLE

RESET	DATA		CLOCK		Q
E	A	B	C	D	YA
L	X	X	H	L	--
L	X	X	L	H	--
L	L	H	L→H	H→L	L
L	H	L	L→H	H→L	H
H	X	X	H	L	L
H	X	X	L	H	--
H	H	L	L→H	H→L	L

NOTE: -- = NO CHANGE

9

MACRO: 714 D FLIP–FLOP WITH GATED DATA INPUT AND DIFFERENTIAL CLOCK
HI DRIVE MACRO
FULL CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	Actual Capacitance
A	1		0.12 pF
B	1		0.12 pF
C		2	0.10 pF
D		2	0.10 pF
E	1		0.12 pF

POWER: (mW)

	LP Array
L Macro	32.0

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
C,D	YA,YB,YC,YD	200	200		
E	YA,YB	--	375		
E	YC,YD	375	--		
MIN CLOCK PULSE WIDTH		200			
MIN RESET PULSE WIDTH		350			
DATA SET UP		125			
DATA HOLD		75			
MIN RESET HOLD		75			
MIN RESET RECOVERY		125			

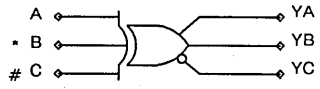
Notes:
1. The default output follower current for each output is 0.96 ma. If the outputs are twinned, the user can select 1.92 ma.
2. The user should note that different R_{sr}, R_{sf} and K values apply for Hi-Drive Macros.
3. Minimum reset hold time is the minimum amount of time that RESET must be be held 'high' after the CLOCK switches from a 'low' to a 'high' in order for the flip-flop to remain in the reset state.
4. It should be noted that the Master portion of the flip-flop is asynchronously reset when the RESET line is 'high'. This reset scheme eliminates the possibility of an output glitch for the condition:
RESET = 'H', DATA = 'H', and the CLOCK transitions from 'L'→'H'.

TRUTH TABLE

RESET	DATA	CLOCK		Q
E	A+B	C	D	YA
L	X	H	L	--
L	X	L	H	--
L	L	L→H	H→L	L
L	H	L→H	H→L	H
H	X	H	L	L
H	X	L	H	--
H	H	L→H	H→L	L

NOTE: -- = NO CHANGE

MACRO: 802 3–INPUT EXOR/EXNOR
1/4 CELL
3 LEVEL SERIES GATING



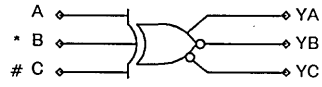
	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		

POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4

$YA=YB=\overline{YC}=A\oplus B\oplus C$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A	YA,YB	300	325	225	225
A	YC	150	250	125	175
B	YA,YB	350	575	250	400
B	YC	300	350	250	250
C	YA,YB	400	750	250	525
C	YC	375	400	300	275

MACRO: 803 3–INPUT EXOR/EXNOR
1/4 CELL
3 LEVEL SERIES GATING



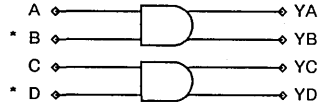
	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		

POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4

$YA=\overline{YB}=\overline{YC}=A\oplus B\oplus C$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A	YA	300	300	200	225
A	YB,YC	175	250	150	200
B	YA	325	550	225	400
B	YB,YC	350	350	250	250
C	YA	375	750	250	525
C	YB,YC	400	450	325	300

MACRO: 804 DUAL 2 INPUT AND
1/4 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 4.5

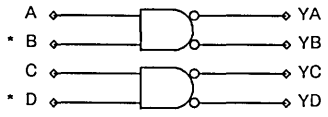
$YA=YB=A \cdot B$

$YC=YD=C \cdot D$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A	YA,YB	350	325		
B	YA,YB	300	375		
C	YC,YD	350	325		
D	YC,YD	300	375		

9

MACRO: 805 DUAL 2–INPUT NAND
1/4 CELL
2 LEVEL SERIES GATING



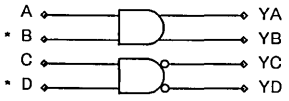
POWER: (mW)
LP Array
L Macro 4.5

$\overline{YA-YB}$-A • B

$\overline{YC-YD}$-C • D

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A	YA,YB	150	225		
B	YA,YB	250	300		
C	YC,YD	150	225		
D	YC,YD	250	300		

MACRO: 806 DUAL 2–INPUT AND/NAND
1/4 CELL
2 LEVEL SERIES GATING



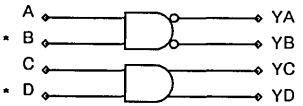
POWER: (mW)
LP Array
L Macro 4.5

YA-YB-A • B

$\overline{YC-YD}$-C • D

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A	YA,YB	350	325		
B	YA,YB	300	375		
C	YC,YD	150	225		
D	YC,YD	250	300		

MACRO: 807 DUAL 2–INPUT AND/NAND
1/4 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 4.5

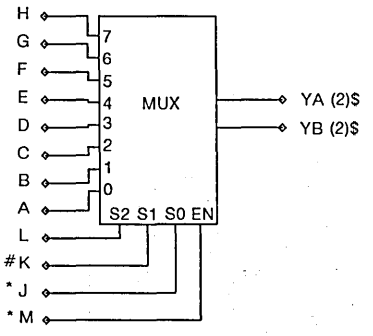
YC-YD-C • D

$\overline{YA-YB}$-A • B

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A	YA,YB	150	225		
B	YA,YB	250	300		
C	YC,YD	350	325		
D	YC,YD	300	375		

9

MACRO: 809 8–1 MUX WITH ENABLE (HIGH)
FULL CELL
3 LEVEL SERIES GATING



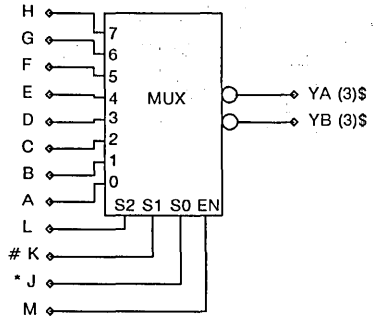
POWER: (mW)
LP Array
L Macro 8.2
H Macro 13.5

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
ABCDEFGHL	YA,YB	850	800	525	475
J,M	YA,YB	975	1050	600	700
K	YA,YB	1025	1225	650	800

TRUTH TABLE

M	L	K	J	YA,YB
L	X	X	X	L
H	L	L	L	A
H	L	L	H	B
H	L	H	L	C
H	L	H	H	D
H	H	L	L	E
H	H	L	H	F
H	H	H	L	G
H	H	H	H	H

MACRO: 810 8–1 MUX WITH ENABLE (HIGH)
FULL CELL
3 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 8.2
H Macro 13.5

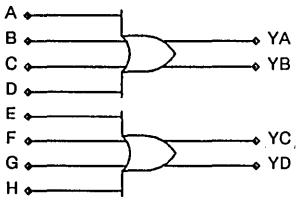
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
ABCDEFGHL	YA,YB	850	800	525	475
J	YA,YB	975	1050	600	700
K	YA,YB	1025	1225	650	800
M	YA,YB	500	475	350	325

TRUTH TABLE

M	L	K	J	YA,YB
L	X	X	X	Logic (H)
H	L	L	L	$\overline{A}$
H	L	L	H	$\overline{B}$
H	L	H	L	$\overline{C}$
H	L	H	H	$\overline{D}$
H	H	L	L	$\overline{E}$
H	H	L	H	$\overline{F}$
H	H	H	L	$\overline{G}$
H	H	H	H	$\overline{H}$

9

MACRO: 811 DUAL 4 INPUT OR
1/4 CELL
1 LEVEL SERIES GATING

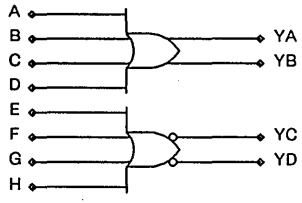


POWER: (mW)
LP Array
L Macro 2.9
YA=YB=A+B+C+D
YC=YD=E+F+G+H

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D	YA,YB	225	250		

NOTE: Delays are the same as above for E,F,G,H to YC, YD

MACRO: 812 DUAL 4 INPUT OR/NOR
1/4 CELL
1 LEVEL SERIES GATING

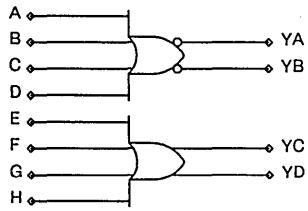


POWER: (mW)
LP Array
L Macro 2.9

YA=YB=$\overline{A+B+C+D}$
YC=YD=E+F+G+H

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D	YA,YB	225	250		
E,F,G,H	YC,YD	475	425		

MACRO: 813 DUAL 4 INPUT OR/NOR
1/4 CELL
1 LEVEL SERIES GATING



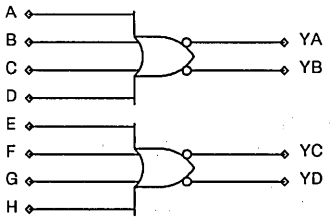
POWER: (mW)
LP Array
L Macro 2.9

YC=YD=$\overline{E+F+G+H}$
YA=YB=A+B+C+D

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D	YA,YB	475	425		
E,F,G,H	YC,YD	225	250		

9

MACRO: 814 DUAL 4–INPUT NOR
1/4 CELL
1 LEVEL SERIES GATING



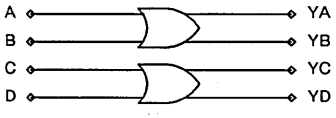
POWER: (mW)
LP Array
L Macro 2.9

$YA=YB=\overline{A+B+C+D}$
$YC=YD=\overline{E+F+G+H}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	YA,YB	475	425		

NOTE: Delays are the same as above for E,F,G,H to YC, YD

MACRO: 815 DUAL 2–INPUT OR
1/4 CELL
1 LEVEL SERIES GATING

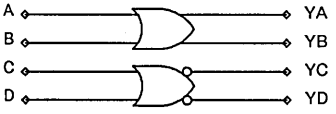


POWER: (mW)
LP Array
L Macro 2.9
YA=YB=A+B
YC=YD=C+D

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB	250	250		

NOTE: Delays are the same as above for C,D to YC, YD

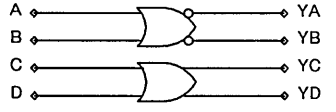
MACRO: 816 DUAL 2–INPUT OR/NOR
1/4 CELL
1 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 2.9
$YA=YB=\overline{A+B}$
YC=YD=C+D

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB	250	250		
C,D	YC,YD	250	300		

MACRO: 817 DUAL 2–INPUT OR/NOR
1/4 CELL
1 LEVEL SERIES GATING



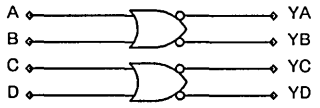
POWER: (mW)
LP Array
L Macro 2.9

$YA=YB=\overline{A+B}$
YC=YD=C+D

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	YA,YB	250	300		
C,D	YC,YD	250	250		

9

MACRO: 818 DUAL 2-INPUT NOR
1/4 CELL
1 LEVEL SERIES GATING



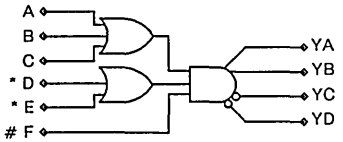
POWER: (mW)
LP Array
L Macro 2.9

$YA=YB=\overline{A+B}$
$YC=YD=\overline{C+D}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA,YB	250	300		

NOTE: Delays are the same as above for C,D to YC, YD

MACRO: 819 3-2-1 OR/AND
1/4 CELL
3 LEVEL SERIES GATING

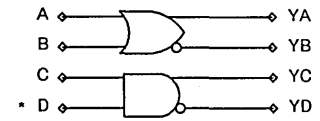


POWER: (mW)
LP Array
L Macro 3.1
H Macro 4.4

$YA=YB=\overline{YC}=\overline{YD}= (A+B+C) \bullet (D+E) \bullet F$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C	YA,YB	500	525	325	350
A,B,C	YC,YD	425	450	275	300
D,E	YA,YB	400	550	300	375
D,E	YC,YD	525	550	375	350
F	YA,YB	450	600	300	450
F	YC,YD	650	600	450	400

MACRO: 820 2-INPUT OR, 2-INPUT AND
1/4 CELL
2 LEVEL SERIES GATING



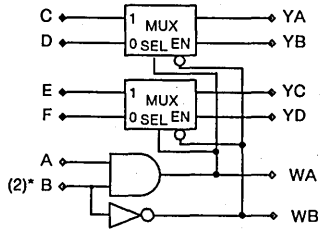
$YA=\overline{YB}=A+B$
$YC=\overline{YD}=CD$

POWER: (mW)
LP Array
L Macro 3.7

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YA	250	250		
A,B	YB	250	300		
C	YC	350	325		
C	YD	150	225		
D	YC	300	375		
D	YD	250	300		

9

MACRO: 850 EXPANDABLE 2–1 MUX(CODER) AND 2x2–1 MUX
1/2 CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
B	1	1	

POWER: (mW)
LP Array
L Macro 12.2

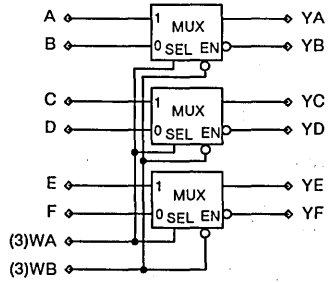
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A	YA,YB,YC,YD	850	900		
B	YA,YB,YC,YD	475	600		
C,D,E,F	YA,YB,YC,YD	425	375		

NOTE: MUX's are enabled when B is high. Macro delays for 850 coder circuitry are included in the delay tables for 851, 852, and 853. Metal and fanout delays must still be added for the 850 'W' outputs using the calculations for a single, low-power internal macrocell output. Metal and fanout delays for the WA, WB outputs and the YA,YB,YC,YD outputs must also be added to the delay numbers listed in the table above (i.e. two sets of metal/fanout delays must be added.) The output follower current for the WA and WB outputs are connected to V_{EEE} and are included in the specified power.

TRUTH TABLE

A	B	YA,YB	YC,YD	WA	WB
X	L	L	L	L	H
L	H	D	F	L	L
H	H	C	E	H	L

MACRO: 851 EXPANDABLE 2–1 MUX
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 4.3

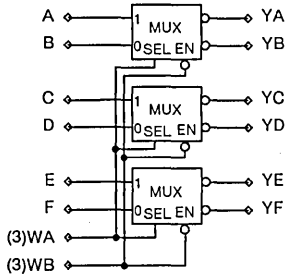
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
WA	YA,YC,YE	800	875		
WA	YB,YD,YF	550	725		
WB	YA,YC,YE	450	575		
WB	YB,YD,YF	525	650		
A–F	YA,YC,YE	375	350		
A–F	YB,YD,YF	225	275		

NOTE: 'A' and 'B' in the following table represent the A and B inputs to the 850 coder macro.

TRUTH TABLE

A	B	YA	YB	YC	YD	YE	YF
X	L	L	H	L	H	L	H
L	H	B	$\overline{B}$	D	$\overline{D}$	F	$\overline{F}$
H	H	A	$\overline{A}$	C	$\overline{C}$	E	$\overline{E}$

MACRO: 852 EXPANDABLE 2–1 MUX
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 4.3

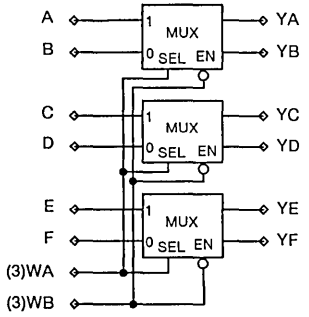
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
WA	ALL	575	750		
WB	ALL	550	675		
A–F	ALL	250	300		

NOTE: 'A' and 'B' in the following table represent the A and B inputs to the 850 coder macro.

TRUTH TABLE

A	B	YA	YB	YC	YD	YE	YF
X	L	H	H	H	H	H	H
L	H	$\overline{B}$	$\overline{B}$	$\overline{D}$	$\overline{D}$	$\overline{F}$	$\overline{F}$
H	H	$\overline{A}$	$\overline{A}$	$\overline{C}$	$\overline{C}$	$\overline{E}$	$\overline{E}$

MACRO: 853 EXPANDABLE 2–1 MUX
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 4.3

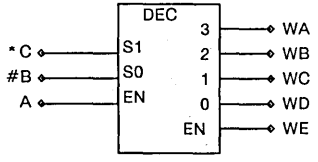
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
WA	ALL	850	900		
WB	ALL	475	600		
A–F	ALL	425	375		

NOTE: 'A' and 'B' in the following table represent the A and B inputs to the 850 coder macro.

TRUTH TABLE

A	B	YA	YB	YC	YD	YE	YF
X	L	L	L	L	L	L	L
L	H	B	B	D	D	F	F
H	H	A	A	C	C	E	E

MACRO: 860 EXPANDABLE 4–1 MUX(CODER) WITH ENABLE
1/2 CELL
3 LEVEL SERIES GATING



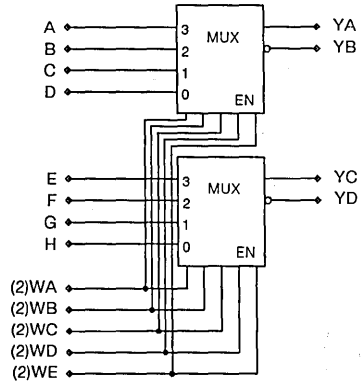
POWER: (mW)
LP Array
L Macro 21.6

NOTE: MUX's are enabled when A is high. Macro delays for 860 are included in the delay tables for 861, 862, and 863. Metal and fanout delays must still be added for the 860 outputs using the calculations for a single, low-power internal macrocell output. The output follower current for the W outputs are connected to V_{EEE} and are included in the specified power.

TRUTH TABLE

B	C	WA	WB	WC	WD	WE
L	L	L	L	L	H	A
H	L	L	L	H	L	A
L	H	L	H	L	L	A
H	H	H	L	L	L	A

MACRO: 861 EXPANDABLE 4–1 MUX
1/2 CELL
3 LEVEL SERIES GATING



POWER: (mW)

	LP Array
L Macro	2.9
H Macro	5.5

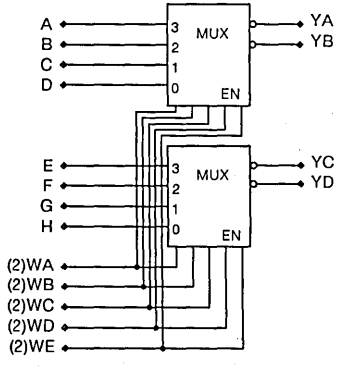
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A–H	YA,YC	550	475	325	300
	YB,YD	400	375	250	250
WA,WB,WC,WD	YA,YC	700	875	450	575
WA,WB,WC,WD	YB,YD	725	750	500	500
WE	YA,YC	575	500	350	400
WE	YB,YD	550	625	350	475

NOTE: A,B,C in the left columns of the truth table represent the SELECTS and ENABLE from the 860 macro.

TRUTH TABLE

A	B	C	WA	WB	WC	WD	WE	YA	YB	YC	YD
L	X	X	X	X	X	X	L	L	H	L	H
H	L	L	L	L	L	H	H	D	$\overline{D}$	H	$\overline{H}$
H	H	L	L	L	H	L	H	C	$\overline{C}$	G	$\overline{G}$
H	L	H	L	H	L	L	H	B	$\overline{B}$	F	$\overline{F}$
H	H	H	H	L	L	L	H	A	$\overline{A}$	E	$\overline{E}$

MACRO: 862 EXPANDABLE 4–1 MUX
1/2 CELL
3 LEVEL SERIES GATING



POWER: (mW)

	LP Array
L Macro	2.9
H Macro	5.5

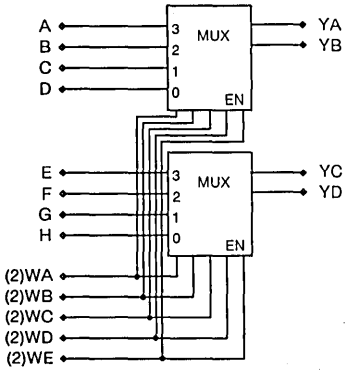
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A–H	YA,YB,YC,YD	400	400	250	250
WA,WB, WC,WD	YA,YB,YC,YD	750	800	525	500
WE	YA,YB,YC,YD	725	650	400	500

NOTE: A,B,C in the left columns of the truth table represent the SELECTS and ENABLE from the 860 macro.

TRUTH TABLE

A	B	C	WA	WB	WC	WD	WE	YA	YB	YC	YD
L	X	X	X	X	X	X	L	H	H	H	H
H	L	L	L	L	L	H	H	$\overline{D}$	$\overline{D}$	$\overline{H}$	$\overline{H}$
H	H	L	L	L	H	L	H	$\overline{C}$	$\overline{C}$	$\overline{G}$	$\overline{G}$
H	L	H	L	H	L	L	H	$\overline{B}$	$\overline{B}$	$\overline{F}$	$\overline{F}$
H	H	H	H	L	L	L	H	$\overline{A}$	$\overline{A}$	$\overline{E}$	$\overline{E}$

MACRO: 863 EXPANDABLE 4–1 MUX
1/2 CELL
3 LEVEL SERIES GATING



POWER: (mW)

	LP Array
L Macro	2.9
H Macro	5.5

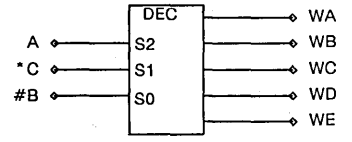
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A–H	YA,YB,YC,YD	575	500	350	325
WA,WB, WC,WD	YA,YB,YC,YD	725	900	475	600
WE	YA,YB,YC,YD	525	450	325	375

NOTE: A,B,C in the left columns of the truth table represent the SELECTS and ENABLE from the 860 macro.

TRUTH TABLE

A	B	C	WA	WB	WC	WD	WE	YA	YB	YC	YD
L	X	X	X	X	X	X	L	L	L	L	L
H	L	L	L	L	L	H	H	D	D	H	H
H	H	L	L	L	H	L	H	C	C	G	G
H	L	H	L	H	L	L	H	B	B	F	F
H	H	H	H	L	L	L	H	A	A	E	E

MACRO: 870 EXPANDABLE 8–1 MUX(CODER)
1/2 CELL
3 LEVEL SERIES GATING



POWER: (mW)

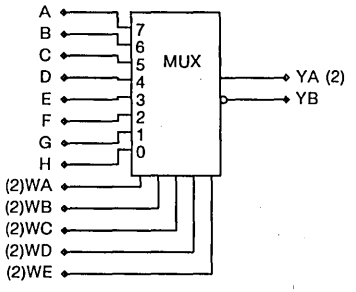
	LP Array
L Macro	21.9

NOTE: Macro delays for 870 are included in the delay tables for 871, 872, and 873. Metal and fanout delays must still be added for the 870 outputs using the calculations for a single, low-power internal macrocell output. The output follower current for the W outputs are connected to V_{EEE} and are included in the specified power.

TRUTH TABLE

B	C	WA	WB	WC	WD	WE
L	L	L	L	L	H	A
H	L	L	L	H	L	A
L	H	L	H	L	L	A
H	H	H	L	L	L	A

MACRO: 871 EXPANDABLE 8–1 MUX
1/2 CELL
3 LEVEL SERIES GATING



POWER: (mW)

	LP Array
L Macro	2.9
H Macro	5.5

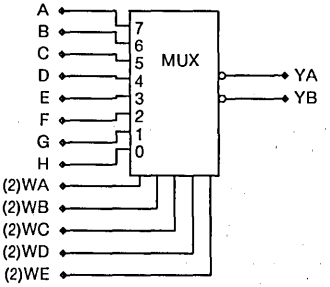
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A–H	YA	550	475	325	300
A–H	YB	400	375	250	250
WA,WB,WC,WD	YA	700	875	450	575
WA,WB,WC,WD	YB	725	750	500	500
WE	YA	575	500	350	400
WE	YB	550	625	350	475

NOTE: A, B, and C in the left columns of the truth table represent the selects from the 870 coder macro.

TRUTH TABLE

A	B	C	WA	WB	WC	WD	WE	YA	YB
L	L	L	L	L	L	H	L	H	$\overline{H}$
L	H	L	L	L	H	L	L	G	$\overline{G}$
L	L	H	L	H	L	L	L	F	$\overline{F}$
L	H	H	H	L	L	L	L	E	$\overline{E}$
H	L	L	L	L	L	H	H	D	$\overline{D}$
H	H	L	L	L	H	L	H	C	$\overline{C}$
H	L	H	L	H	L	L	H	B	$\overline{B}$
H	H	H	H	L	L	L	H	A	$\overline{A}$

MACRO: 872 EXPANDABLE 8–1 MUX
1/2 CELL
3 LEVEL SERIES GATING



POWER: (mW)

	LP Array
L Macro	2.9
H Macro	5.5

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A–H	YA,YB	400	375	250	250
WA,WB,WC,WD	YA,YB	725	750	500	500
WE	YA,YB	550	625	350	475

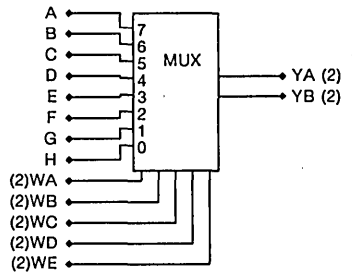
NOTE: A, B, and C in the left columns of the truth table represent the selects from the 870 coder macro.

TRUTH TABLE

A	B	C	WA	WB	WC	WD	WE	YA	YB
L	L	L	L	L	L	H	L	$\overline{H}$	$\overline{H}$
L	H	L	L	L	H	L	L	$\overline{G}$	$\overline{G}$
L	L	H	L	H	L	L	L	$\overline{F}$	$\overline{F}$
L	H	H	H	L	L	L	L	$\overline{E}$	$\overline{E}$
H	L	L	L	L	L	H	H	$\overline{D}$	$\overline{D}$
H	H	L	L	L	H	L	H	$\overline{C}$	$\overline{C}$
H	L	H	L	H	L	L	H	$\overline{B}$	$\overline{B}$
H	H	H	H	L	L	L	H	$\overline{A}$	$\overline{A}$

9

MACRO: 873 EXPANDABLE 8–1 MUX
1/2 CELL
3 LEVEL SERIES GATING



POWER: (mW)

	LP Array
L Macro	2.9
H Macro	5.5

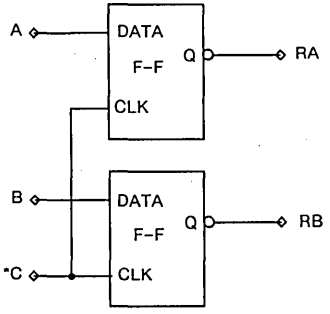
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A–H	YA,YB	550	475	325	300
WA,WB,WC,WD	YA,YB	700	875	450	575
WE	YA,YB	575	500	350	400

NOTE: A, B, and C in the left columns of the truth table represent the selects from the 870 coder macro.

TRUTH TABLE

A	B	C	WA	WB	WC	WD	WE	YA	YB
L	L	L	L	L	L	H	L	H	H
L	H	L	L	L	H	L	L	G	G
L	L	H	L	H	L	L	L	F	F
L	H	H	H	L	L	L	L	E	E
H	L	L	L	L	L	H	H	D	D
H	H	L	L	L	H	L	H	C	C
H	L	H	L	H	L	L	H	B	B
H	H	H	H	L	L	L	H	A	A

MACRO: 881 D FLIP–FLOP
1/2 CELL
2 LEVEL SERIES GATING
LOW POWER MACRO ONLY



POWER: (mW)

	LP Array
L Macro	14.2

OEF V_{EEE} CURRENT: (mA/output)

	LP Array
	0.88

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
C	RA,RB	450	525		
SET UP		600			
MIN POS CLK PULSE WIDTH		1500			
MIN NEG CLK PULSE WIDTH		1000			

TRUTH TABLE

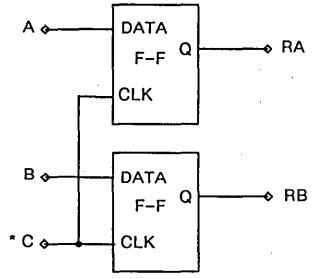
DATA	CLOCK	SLAVE $\overline{Q}$
A/B	C	RA/RB
X	H	--
L	L	--
L	L→H	H
H	L	--
H	L→H	L

NOTE: -- = NO CHANGE

NOTES:
1. The 881 has passive (resistive) output pulldowns.
2. Outputs RA and RB may not be used in a wired OR.
3. For the LPA, the average follower power due to the V_{EEE} current for each output is 4.58 mW for V_{EEE} = –5.2 V.
4. The resistive follower is only connected if the output is used.
5. Max F.O. = 24 (LPA).
6. R_{SR} values are for a twinned output.

9

MACRO: 882 D FLIP–FLOP
1/2 CELL
2 LEVEL SERIES GATING
LOW POWER MACRO ONLY



MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
C	RA,RB	450	525		
SET UP		600			
MIN POS CLK PULSE WIDTH		1500			
MIN NEG CLK PULSE WIDTH		1000			

TRUTH TABLE

DATA	CLOCK	SLAVE Q
A/B	C	RA/RB
X	H	--
L	L	--
L	L→H	L
H	L	--
H	L→H	H

NOTE: -- = NO CHANGE

POWER: (mW)

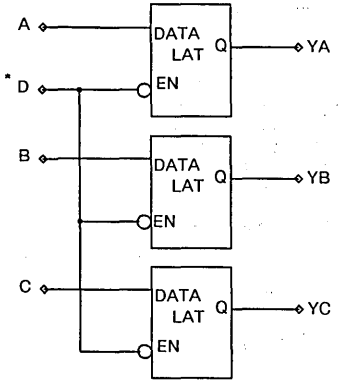
	LP Array
L Macro	14.2

OEF V_{EEE} CURRENT: (mA/output)

L Macro	0.88

NOTES:
1. The 882 has passive (resistive) output pulldowns.
2. Outputs RA and RB may not be used in a wired OR.
3. For the LPA, the average follower power due to the V_{EEE} current for each output is 4.58 mW for V_{EEE} = –5.2 V.
4. The resistive follower is only connected if the output is used.
5. Max F.O. = 24 (LPA).
6. R_{SR} values are for a twinned output.

MACRO: 893 3xD LATCH WITH COMMON CLOCK
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)

	LP Array
L Macro	12.8

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C	YA,YB,YC	350	400		
D	YA,YB,YC	475	525		
SET UP TIME		600			
MIN ENABLE PULSE WIDTH		1000			

TRUTH TABLE

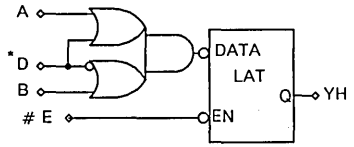
DATA	$\overline{EN}$	Q
A/B/C	D	YA/YB/YC
X	H	--
L	L	L
H	L	H

NOTE: -- = NO CHANGE

NOTE:
Latches are enabled when input D is low.

MACRO: 894 D LATCH WITH MUX

1/4 CELL
3 LEVEL SERIES GATING



$DATA = \overline{(A+D) \cdot (B+\overline{D})}$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	YH	450	475	300	300
D	YH	575	800	400	450
E	YH	525	875	375	600
SET UP TIME		600		450	
MIN ENABLE PULSE WIDTH		1000		750	

POWER: (mW)

	LP Array
L Macro	6.1
H Macro	8.7

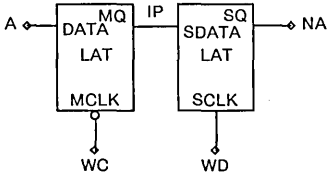
TRUTH TABLE

DATA	$\overline{EN}$	Q
$\overline{(A+D) \cdot (B+\overline{D})}$	E	YH
X	H	--
L	L	L
H	L	H

NOTE: -- = NO CHANGE

NOTE: Latch is enabled low.

Macro: 895 D FLIP-FLOP
1/4 CELL
2 LEVEL SERIES GATING



TRUTH TABLE

SDATA	SCLK	SQ
IP	WD	NA
X	L	--
H	H	H
L	H	L

NOTE: -- = NO CHANGE

POWER: (mW)

	LP Array
L Macro	6.9

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A	IP	400	400		
WC	IP	450	525		
A	NA	800	800		
WC	NA	850	925		
WD	NA	450	525		
WD MIN PULSE WIDTH		1750	1000		
WC MIN PULSE WIDTH		1000			
A to WC SET UP		600			
IP to WD SET UP		1350			

TRUTH TABLE

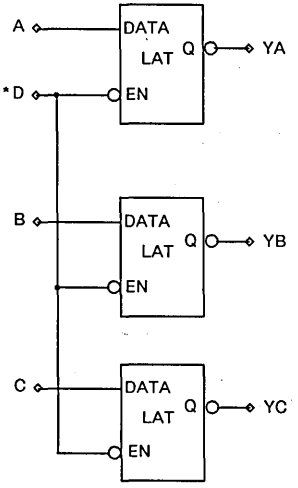
DATA	$\overline{MCLK}$	MQ
A	WC	IP
X	H	--
L	L	L
H	L	H

NOTE: -- = NO CHANGE

NOTE: If the user switches WC and WD clocks at the same time, then the setup time should be referenced off of the first clock edge and WC and WD inputs must be tied together and driven from 593 W Buffer.
NA is a twinned output. Wired-OR connections are not permitted.

MACRO: 896 3xD LATCH WITH COMMON CLOCK
1/2 CELL
2 LEVEL SERIES GATING
LOW POWER MACRO ONLY

POWER: (mW)
LP Array
L Macro 12.8



MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C	YA,YB,YC	350	400		
D	YA,YB,YC	475	625		
SET UP TIME		600			
MIN ENABLE PULSE WIDTH		1000			

TRUTH TABLE

DATA	$\overline{EN}$	$\overline{Q}$
A/B/C	D	YA/YB/YC
X	H	--
L	L	H
H	L	L

NOTE: -- = NO CHANGE

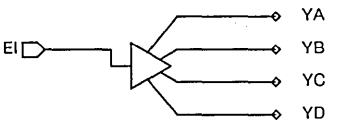
NOTE: Data inputs are separate, enable inputs are common. Function is the same for all three latches. Latches are enabled when input D is low.

9

INPUT/OUTPUT (U) MACROCELLS

ECL INPUT INTERFACE [(C) MACROS (U–CELLS)]

MACRO: C01 INPUT BUFFER (Non–Inverting)
Quad Buffer
1 U-CELL
1 LEVEL SERIES GATING

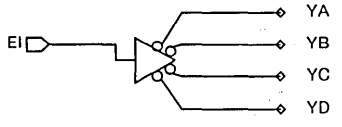


POWER: (mW)
LP Array
L Macro 1.4
H Macro 2.8

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
EI	YA,YB,YC,YD	300	300	225	225

EI = YA = YB = YC = YD

MACRO: C02 INPUT BUFFER (Inverting)
Quad Buffer
1 U-CELL
1 LEVEL SERIES GATING



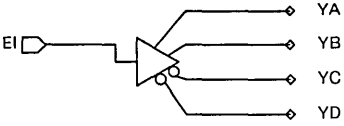
POWER: (mW)
LP Array
L Macro 1.4
H Macro 2.8

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
EI	YA,YB,YC,YD	200	275	150	200

EI = $\overline{YA}$ = $\overline{YB}$ = $\overline{YC}$ = $\overline{YD}$

MACRO: C03 INPUT BUFFER (Inverting, Non–Inverting)

1 U-CELL
1 LEVEL SERIES GATING



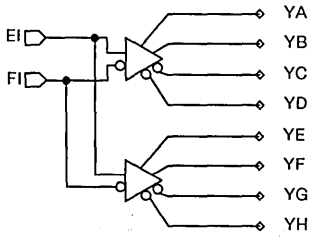
POWER: (mW)
LP Array
L Macro 1.4
H Macro 2.8

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
EI	YA,YB	225	250	175	200
EI	YC,YD	150	225	125	175

EI = YA = YB = $\overline{YC}$ = $\overline{YD}$

9

MACRO: C05 DUAL DIFFERENTIAL INPUT BUFFER
2 U-CELLS
1 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 2.8
H Macro 5.5

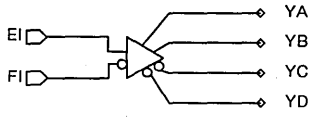
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
EI,FI	YA -YH	175	225	175	200

TRUTH TABLE

EI	FI	YA,YB,YE,YF	YC,YD,YG,YH
L	L	ND	ND
L	H	L	H
H	L	H	L
H	H	ND	ND

NOTE: ND = NOT DEFINED

MACRO: C13 DIFFERENTIAL INPUT BUFFER
2 U-CELLS
1 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 1.4
H Macro 2.8

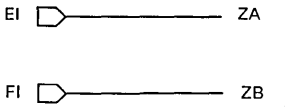
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
EI,FI	YA,YB,YC,YD	175	225	175	200

TRUTH TABLE

EI	FI	YA,YB	YC,YD
L	L	ND	ND
L	H	L	H
H	L	H	L
H	H	ND	ND

NOTE: ND = NOT DEFINED

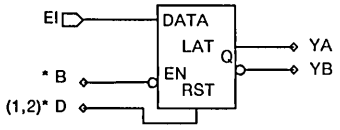
MACRO: C15 DIFFERENTIAL BYPASS
2 U-CELLS
1 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 0.0

$EI = \overline{FI} = ZA = \overline{ZB}$

MACRO: C50 INPUT LATCH with ENABLE LOW
1 U-CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 8.6
H Macro 9.9

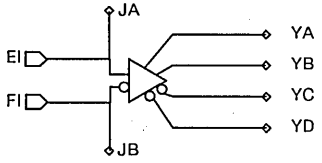
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
EI	YA,YB	400	400	250	250
B	YA,YB	425	525	300	350
D	YA	--	525	--	375
D	YB	525	--	375	--
SET UP		600		450	
MIN CLOCK PULSE WIDTH		1000		750	
MIN RESET PULSE WIDTH		1075		825	

TRUTH TABLE

RST	DATA	ENABLE	Q
D	EI	B	YA
H	X	H	L
L	X	H	--
X	L	L	L
X	H	L	H

NOTE: -- = NO CHANGE

MACRO: C70 DIFFERENTIAL INPUT BUFFER WITH OFF CHIP TERMINATION INPUTS
HI DRIVE MACRO
2 U-CELLS
1 LEVEL SERIES GATING



NOTES:
1.Outputs JA and JB can be used as off-chip input termination ports when connected via Macro E75. If outputs JA and JB are left open, Macro C70 may be used as a standard differential input buffer.
2. The FIX file uses output JA as the first output to fix the FI signal of the macro.
3. Output JA is the alphabetically first output of the macro.
4. Macro C70 can be used for input frequencies up to 2.6 GHz. Refer to Section 5.4 for requirements and limitations.

POWER: (mW)
LP Array
L Macro 7.8

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
EI,FI	YA,YB,YC,YD	75	100		

TRUTH TABLE

EI	FI	YA,YB	YC,YD
L	L	ND	ND
L	H	L	H
H	L	H	L
H	H	ND	ND

NOTE: ND = NOT DEFINED

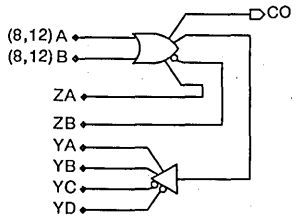
9

ECL OUTPUT DRIVERS [(E) MACROS (U-CELLS)]

NOTE: DC input loading (fanin) is shown in parentheses (). For example, if (8,12) is shown in parentheses, that input represents a DC load of 8 for a low power macro and 12 for a high power macro in the low power array. The number of AC loads is shown in a separate table if it is other than one.

L Macro – 60 ohm outputs
H Macro – 50 ohm outputs

MACRO: E01 2-INPUT OR
1 U-CELL
1 LEVEL SERIES GATING

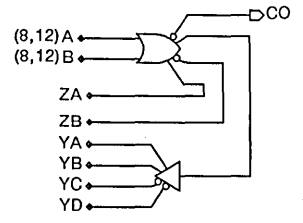


POWER: (mW)
LP Array
L Macro 17.7
H Macro 23.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	CO	500	300	350	275
A,B	ZA	425	425	325	350
A,B	ZB	425	450	350	350
A,B	YA,YB	600	650	475	525
A,B	YC,YD	650	700	525	550

$CO = ZA = YA = YB = \overline{ZB} = \overline{YC} = \overline{YD} = A+B$

MACRO: E02 2-INPUT NOR
1 U-CELL
1 LEVEL SERIES GATING



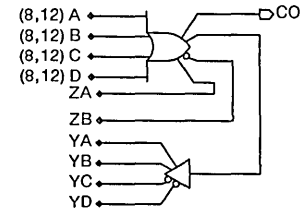
POWER: (mW)
LP Array
L Macro 17.7
H Macro 23.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	CO	525	350	375	275
A,B	ZA	425	425	325	350
A,B	ZB	425	450	350	350
A,B	YA,YB	650	675	500	550
A,B	YC,YD	575	650	475	500

$\overline{CO} = \overline{ZB} = \overline{YC} = \overline{YD} = ZA = YA = YB = A+B$

MACRO: E03 4-INPUT OR

1 U-CELL
1 LEVEL SERIES GATING



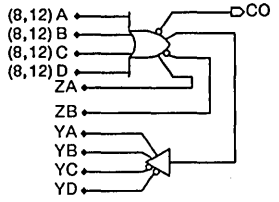
POWER: (mW)
LP Array
L Macro 17.7
H Macro 23.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	CO	500	300	350	275
A,B,C,D	ZA	425	450	325	350
A,B,C,D	ZB	500	500	375	375
A,B,C,D	YA,YB	650	700	500	550
A,B,C,D	YC,YD	600	650	475	500

$CO = ZA = YA = YB = \overline{ZB} = \overline{YC} = \overline{YD} = A+B+C+D$

MACRO: E04 4-INPUT NOR

1 U-CELL
1 LEVEL SERIES GATING



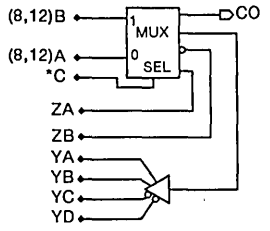
POWER: (mW)
LP Array
L Macro 17.7
H Macro 23.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B,C,D	CO	600	375	425	300
A,B,C,D	ZA	425	450	325	350
A,B,C,D	ZB	500	500	375	375
A,B,C,D	YA,YB	650	700	500	550
A,B,C,D	YC,YD	600	650	475	500

$\overline{CO} = \overline{ZB} = \overline{YC} = \overline{YD} = ZA = YA = YB = A+B+C+D$

MACRO: E05 2-TO-1 MUX

1 U-CELL
2 LEVEL SERIES GATING



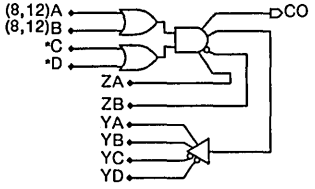
POWER: (mW)
LP Array
L Macro 17.7
H Macro 23.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	CO	550	325	375	300
A,B	ZA	450	450	350	350
A,B	ZB	425	475	350	350
A,B	YA,YB	675	700	525	550
A,B	YC,YD	600	675	475	525
C	CO	600	400	425	350
C	ZA	525	525	400	425
C	ZB	500	550	425	400
C	YA,YB	750	775	575	625
C	YC,YD	675	750	550	575

$CO = YA = YB = ZA = \overline{ZB} = \overline{YC} = \overline{YD} = [(B \bullet C)+(A \bullet \overline{C})+(A \bullet B)]$

MACRO: E06 2-2 OR/AND

1 U-CELL
2 LEVEL SERIES GATING



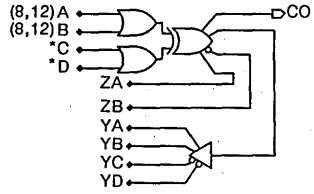
POWER: (mW)
LP Array
L Macro 17.7
H Macro 23.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	CO	550	325	375	300
A,B	ZA	450	450	350	350
A,B	ZB	425	450	350	350
A,B	YA,YB	600	650	475	525
A,B	YC,YD	650	700	525	550
C,D	CO	600	400	425	350
C,D	ZA	500	550	400	450
C,D	ZB	500	500	425	400
C,D	YA,YB	650	725	525	600
C,D	YC,YD	725	750	600	600

$CO = ZA = YA = YB = \overline{ZB} = \overline{YC} = \overline{YD} = (A+B) \bullet (C+D)$

MACRO: E07 2–2 OR/EXOR

1 U-CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A	1.5		
B	1.5		

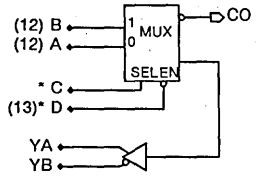
POWER: (mW)
LP Array
L Macro 17.7
H Macro 23.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	CO	550	350	400	300
A,B	ZA	450	500	350	350
A,B	ZB	475	475	350	375
A,B	YA,YB	625	700	500	525
A,B	YC,YD	700	725	525	575
C,D	CO	650	400	475	325
C,D	ZA	550	550	450	400
C,D	ZB	550	550	425	450
C,D	YA,YB	700	775	575	600
C,D	YC,YD	775	800	600	650

$CO = ZA = YA = YB = \overline{ZB} = \overline{YC} = \overline{YD} = (A+B) \oplus (C+D)$

MACRO: E08 2–TO–1 MUX with ENABLE LOW (Inverting)

1 U-CELL
2 LEVEL SERIES GATING



	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
D	1	1	

$CO = \overline{YA} = YB = \overline{D} \cdot [(\overline{C} \cdot \overline{A}) + (C \cdot \overline{B}) + (\overline{B} \cdot \overline{A}) + D]$

POWER: (mW)
LP Array
H Macro 23.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	CO			400	300
A,B	YA			575	575
A,B	YB			500	575
C	CO			500	350
C	YA			650	625
C	YB			550	650
D	CO			500	375
D	YA			650	650
D	YB			575	650

TRUTH TABLE

A	B	C	D	CO	YA	YB
X	X	X	H	L	H	L
L	X	L	L	H	L	H
H	X	L	L	L	H	L
X	L	H	L	H	L	H
X	H	H	L	L	H	L
L	L	X	L	H	L	H
H	H	X	L	L	H	L

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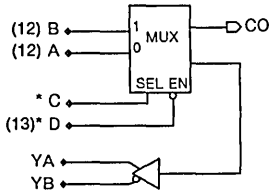
MACRO: E09 2–TO–1 MUX with ENABLE LOW (Non–Inverting)

1 U-CELL
2 LEVEL SERIES GATING



MACRO E09 SYMBOL

	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
D	1	1	

$\overline{CO} = \overline{YA} = YB = \overline{D} \bullet [(\overline{C} \bullet \overline{A}) + (C \bullet \overline{B}) + (\overline{B} \bullet \overline{A}) + D]$

POWER: (mW)
LP Array
H Macro 23.3

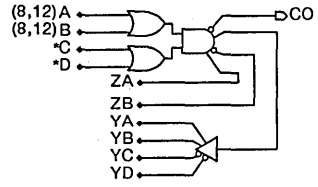
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	CO			400	300
A,B	YA			575	575
A,B	YB			500	575
C	CO			500	350
C	YA			650	625
C	YB			550	650
D	CO			500	375
D	YA			650	650
D	YB			575	650

TRUTH TABLE

A	B	C	D	CO	YA	YB
X	X	X	H	H	H	L
L	X	L	L	L	L	H
H	X	L	L	H	H	L
X	L	H	L	L	L	H
X	H	H	L	H	H	L
L	L	X	L	L	L	H
H	H	X	L	H	H	L

MACRO: E10 2–2 OR/NAND

1 U-CELL
2 LEVEL SERIES GATING



MACRO E10 SYMBOL

POWER: (mW)
LP Array
L Macro 17.7
H Macro 23.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	CO	500	350	375	275
A,B	ZA	450	450	350	350
A,B	ZB	425	450	350	350
A,B	YA,YB	600	650	475	525
A,B	YC,YD	650	700	525	550
C,D	CO	600	400	450	325
C,D	ZA	500	550	400	450
C,D	ZB	500	500	425	400
C,D	YA,YB	650	725	525	600
C,D	YC,YD	725	750	600	600

$\overline{CO} = \overline{ZB} = \overline{YC} = \overline{YD} = ZA = YA = YB = (A+B) \bullet (C+D)$

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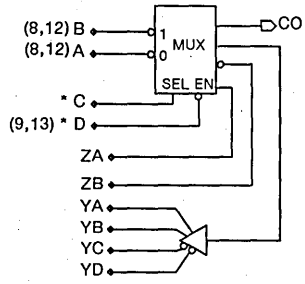
MACRO: E11 2–TO–1 MUX with ENABLE LOW

1 U-CELL
2 LEVEL SERIES GATING



$CO = ZA + \overline{ZB} + \overline{D} \cdot [(\overline{B} \cdot \overline{A}) + (C \cdot \overline{B}) + (\overline{C} \cdot \overline{A}) + D]$

POWER: (mW)
LP Array
L Macro 17.7
H Macro 23.3

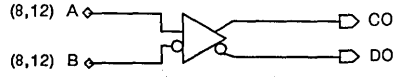
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	CO	550	400	400	300
A,B	ZA,ZB	500	500	400	375
A,B	YA,YB	650	725	500	575
A,B	YC,YD	725	750	575	575
C	CO	650	450	500	350
C	ZA,ZB	575	575	475	425
C	YA,YB	725	800	550	650
C	YC,YD	800	825	650	625
D	CO	675	475	500	375
D	ZA,ZB	600	600	475	450
D	YA,YB	750	825	575	650
D	YC,YD	825	850	650	650

TRUTH TABLE

C	D	CO	ZA,YA,YB	ZB,YC,YD
X	H	L	L	H
L	L	$\overline{A}$	$\overline{A}$	A
H	L	$\overline{B}$	$\overline{B}$	B

MACRO: E12 DIFFERENTIAL OUTPUT BUFFER

2 U-CELLS
1 LEVEL SERIES GATING



$CO = \overline{DO} = A = \overline{B}$

POWER: (mW)
LP Array
L Macro 12.3
H Macro 17.9

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	CO	425	275	325	200
A,B	DO	475	225	300	225

TRUTH TABLE

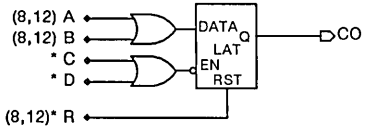
A	B	DO	CO
L	L	ND	ND
L	H	H	L
H	L	L	H
H	H	ND	ND

NOTE: ND = NOT DEFINED

9

MACRO: E50 D LATCH with CLOCK ENABLE LOW

1 U-CELL
2 LEVEL SERIES GATING



POWER: (mW)

	LP Array
L Macro	17.2
H Macro	22.8

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	CO	600	350	400	300
C,D	CO	650	475	500	400
R	CO	---	425	---	375
SET UP TIME		800		600	
MIN CLOCK PULSE WIDTH		1200		900	
MIN RESET PULSE WIDTH		1400		1050	

TRUTH TABLE

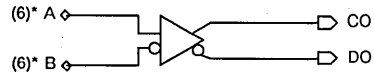
RESET	DATA	C	D	Q
L	X	H	X	--
L	X	X	H	--
H	X	H	X	L
H	X	X	H	L
X	L	L	L	L
X	H	L	L	H

NOTE: -- = NO CHANGE

9

HI SPEED DIFFERENTIAL OUTPUT BUFFER MACROS (E70 – E79)

MACRO: E70 DIFFERENTIAL OUTPUT BUFFER
2 U-CELLS
1 LEVEL SERIES GATING



$CO = \overline{DO} = A = \overline{B}$

NOTES:
1. Inputs A and B should be treated as upper level inputs for AC and DC fan-in considerations only. These inputs follow the I/O connection rules for second level inputs.

2. See Section 5.4.3 for Worst-Case Output Voltage versus Frequency.

POWER: (mW)
LP Array
H Macro 57.2

MACRO DELAYS (ps)		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	CO,DO			150	225

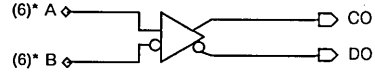
TRUTH TABLE

A	B	DO	CO
L	L	ND	ND
L	H	H	L
H	L	L	H
H	H	ND	ND

NOTE: ND = NOT DEFINED

	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A,B		2	

MACRO: E71 OPEN COLLECTOR DIFFERENTIAL (CML) OUTPUT BUFFER
2 U-CELLS
1 LEVEL SERIES GATING



$CO = \overline{DO} = A = \overline{B}$

NOTES:
1. Inputs A and B should be treated as upper level inputs for AC and DC fan-in considerations only. These inputs follow the I/O connection rules for second level inputs.

2. Open collector outputs CO and DO require a specific resistor termination configuration to exhibit a differential output level of 0.0 mv to -650 mv (typical) with 50 ohm load to ground. The output sink current is 13.0 ± 2.5 ma. Output levels and swings can be tailored to satisfy other output requirements. Refer to Section 5.4 for a description of output termination considerations.

POWER: (mW)
LP Array
H Macro 78.0

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	CO,DO			200	225

NOTE: Propagation delays indicated above are for outputs CO and DO terminated with 50 ohms to VCCE (ground).

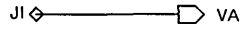
TRUTH TABLE

A	B	DO	CO
L	L	ND	ND
L	H	H	L
H	L	L	H
H	H	ND	ND

NOTES: ND = NOT DEFINED
In the truth table **'L'** in the output represents the **ON** state with the output sinking 12 mA. **'H'** represents the **OFF** state.

	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
A,B		2	

MACRO: E75 OFF-CHIP TERMINATION PAD
1 U-CELLS
1 LEVEL SERIES GATING



JI = VA

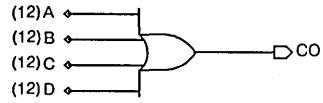
POWER: (mW)
LP Array
L Macro 0.0

NOTE: Macro E75 is only used in conjunction with Macro C70 for off-chip termination of inputs EI and FI. The JI input of this macro connects to JA or JB outputs of Macro C70 by abutment. Therefore, macro E75 must be placed adjacent to the U-cell containing the input to which the E75 macro is going to be connected.

ECL CUTOFF OUTPUT [(ZE) MACROS (U–CELLS)]

MACRO: ZE00 4–INPUT OR
(50 ohm)

1 U–CELL
1 LEVEL SERIES GATING



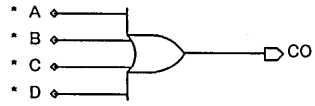
POWER: (mW)
LP Array
L Macro 17.9

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	CO	550	550		

CO = A+B+C+D

MACRO: ZE50 4–INPUT OR
(25 ohm)

1 U–CELL
2 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 30.8

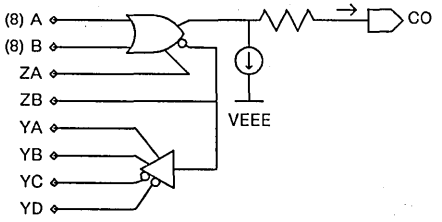
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	CO	575	300		

CO = A+B+C+D

STECL I/O [(S) MACROS (U-CELLS)]

NOTE: STECL outputs consist of single output transistors with an optional series resistor and a current source pulldown attached. These ouputs are generally used for applications where line lengths are short and external parallel terminations are not desirable or possible (e.g. multi-chip hybrid packages).

MACRO: S00 2-INPUT OR
1 U-CELL
1 LEVEL SERIES GATING



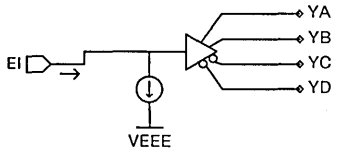
POWER: (mW)
LP Array
L Macro 17.7

STECL OUTPUT POWER:
6mA 31.2 mW
10mA 52.0 mW

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
A,B	CO	500	300		
A,B	ZA	425	425		
A,B	ZB	425	450		
A,B	YA,YB	650	700		
A,B	YC,YD	600	650		

$CO = ZA = \overline{ZB} = \overline{YA} = \overline{YB} = YC = YD = A+B$

MACRO: S50 INPUT BUFFER
1 U-CELL
1 LEVEL SERIES GATING



POWER: (mW)
LP Array
L Macro 1.4

STECL INPUT POWER:
6mA 31.2 mW
10mA 52.0 mW

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
EI	YA,YB	225	250		
EI	YC,YD	150	225		

$EI = YA = YB = \overline{YC} = \overline{YD}$

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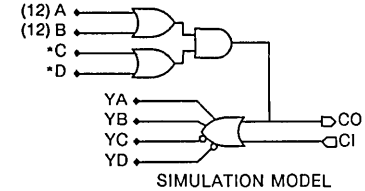
BIDIRECTIONAL I/O [(B) MACROS (U–CELLS), 50 & 25 ohm]

MACRO: B26 2–2 OR/AND
with Input Buffer (50 ohm output)
1 U-CELL
2 LEVEL SERIES GATING

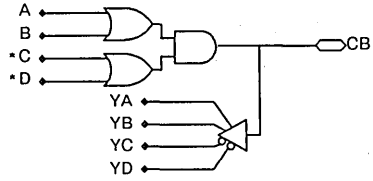


SIMULATION MODEL

POWER: (mW)
LP Array
H Macro 20.6

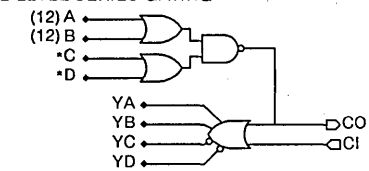
$CB = YA = YB = \overline{YC} = \overline{YD} = (A+B) \bullet (C+D)$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	CB			375	300
A,B	YA,YB			550	500
A,B	YC,YD			425	550
C,D	CB			425	350
C,D	YA,YB			600	550
C,D	YC,YD			475	600
CB	YA,YB			175	200
CB	YC,YD			125	175



ACTUAL CIRCUIT

MACRO: B27 2–2 OR/NAND
with Input Buffer (50 ohm output)
1 U-CELL
2 LEVEL SERIES GATING

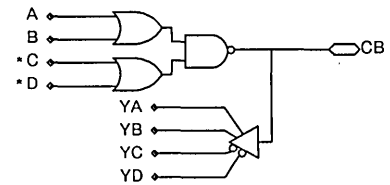


SIMULATION MODEL

POWER: (mW)
LP Array
H Macro 20.6

$\overline{CB} = \overline{YA} = \overline{YB} = YC = YD = (A+B) \bullet (C+D)$

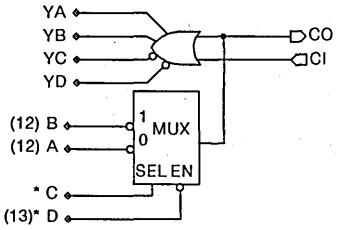
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	CB			375	275
A,B	YA,YB			550	475
A,B	YC,YD			400	550
C,D	CB			450	325
C,D	YA,YB			625	525
C,D	YC,YD			450	625
CB	YA,YB			175	200
CB	YC,YD			125	175



ACTUAL CIRCUIT

9

MACRO: B28 2–1 MUX LOW ENABLE
with Input Buffer (50 ohm output)
1 U-CELL
2 LEVEL SERIES GATING



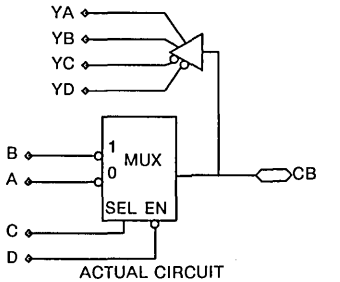
SIMULATION MODEL

	NUMBER OF AC LOADS		
INPUT	1st LEVEL	2nd LEVEL	3rd LEVEL
D	1	1	

POWER: (mW)
LP Array
H Macro 20.6

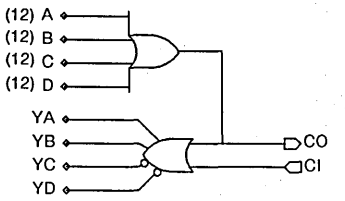
$CB = \overline{D} \bullet [(\overline{A} \bullet \overline{C}) + (\overline{B} \bullet C) + (\overline{A} \bullet \overline{B}) + D]$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	CB			400	300
A,B	YA,YB			575	500
A,B	YC,YD			425	575
C	CB			500	350
C	YA,YB			675	550
C	YC,YD			475	675
D	CB			500	375
D	YA,YB			675	575
D	YC,YD			500	675
CB	YA,YB			175	200
CB	YC,YD			125	175



ACTUAL CIRCUIT

MACRO: B29 4–INPUT OR
with Input Buffer (50 ohm output)
1 U-CELL
1 LEVEL SERIES GATING

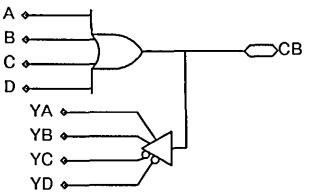


SIMULATION MODEL

POWER: (mW)
LP Array
H Macro 20.6

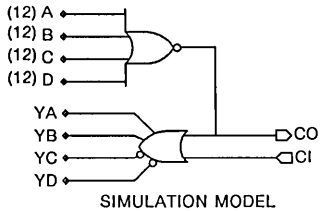
$CB = YA + YB + \overline{YC} + \overline{YD} = A+B+C+D$

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	CB			350	275
A,B,C,D	YA,YB			525	475
A,B,C,D	YC,YD			400	525
CB	YA,YB			175	200
CB	YC,YD			125	175



ACTUAL CIRCUIT

MACRO: B30 4–INPUT NOR
with Input Buffer (50 ohm output)
1 U–CELL
1 LEVEL SERIES GATING

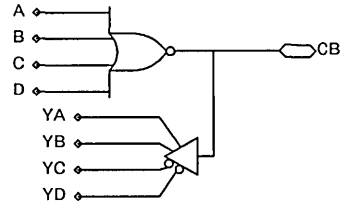


SIMULATION MODEL

POWER: (mW)
LP Array
H Macro 20.6

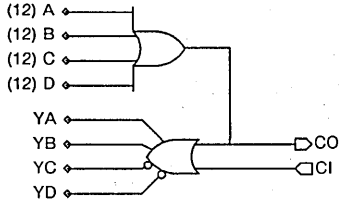
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	CB			425	300
A,B,C,D	YA,YB			600	500
A,B,C,D	YC,YD			425	600
CB	YA,YB			175	200
CB	YC,YD			125	175

$CB = \overline{YC} = \overline{YD} = YA = YB = \overline{A+B+C+D}$



ACTUAL CIRCUIT

MACRO: B50 4–INPUT OR
with Input Buffer (25 ohm cutoff output)
1 U–CELL
1 LEVEL SERIES GATING

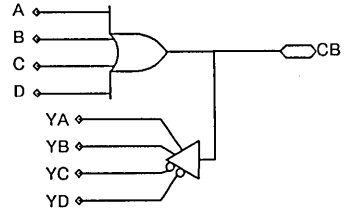


SIMULATION MODEL

POWER: (mW)
LP Array
H Macro 31.7

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	CB			575	300
A,B,C,D	YA,YB			750	500
A,B,C,D	YC,YD			425	750
CB	YA,YB			175	200
CB	YC,YD			125	175

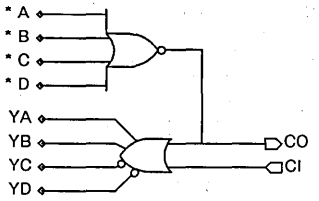
$CB = YA = YB = \overline{YC} = \overline{YD} = A+B+C+D$



ACTUAL CIRCUIT

9

MACRO: B51 4–INPUT NOR
with Input Buffer (25 ohm cutoff output)
1 U-CELL
2 LEVEL SERIES GATING

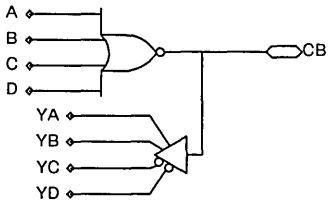


SIMULATION MODEL

POWER: (mW)
LP Array
H Macro 31.7

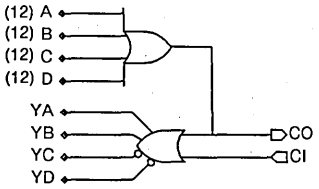
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	CB			625	200
A,B,C,D	YA,YB			800	400
A,B,C,D	YC,YD			325	800
CB	YA,YB			175	200
CB	YC,YD			125	175

$CB = YA = YB = \overline{YC} = \overline{YD} = \overline{A+B+C+D}$



ACTUAL CIRCUIT

MACRO: B76 4–INPUT OR
with Input Buffer (50 ohm cutoff output)
1 U-CELL
1 LEVEL SERIES GATING

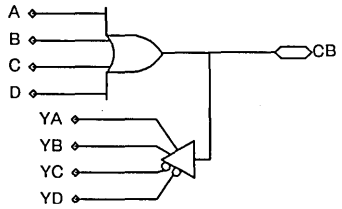


SIMULATION MODEL

POWER: (mW)
LP Array
H Macro 19.3

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B,C,D	CB			550	550
A,B,C,D	YA,YB			725	750
A,B,C,D	YC,YD			675	725
CB	YA,YB			175	200
CB	YC,YD			125	175

$CB = YA = YB = \overline{YC} = \overline{YD} = A+B+C+D$

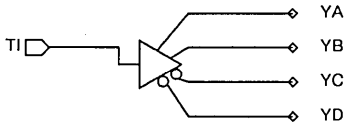


ACTUAL CIRCUIT

9

TTL to ECL INPUT TRANSLATOR [(T:00–29) MACROS (U–CELLS)]

MACRO: T00 TRANSLATOR
with True and Complement
1 U–CELL
1 LEVEL SERIES GATING



Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (Input High)	2.6	2.6
VCCT (Input Low)	1.8	1.8
VEEE	4.4	5.7

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
TI	YA,YB	625	850	575	700
TI	YC,YD	750	700	600	675

$TI = YA = YB = \overline{YC} = \overline{YD}$

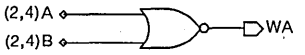
9

ECL to TTL OUTPUT [(T:30–59) MACROS (U–CELLS)]

NOTE: For all TTL outputs ('WA'), the delays in CAD logic simulation reflect testing loads of 50.0 pF.

MACRO: T30 NOR TRANSLATOR

1 U-CELL
1 LEVEL SERIES GATING



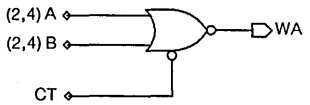
Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (Output Low)	14.8	27.0
VCCT (Output High)	5.8	8.9
VEEE	3.6	7.0

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	WA	2875	3450	2475	2275
Load Factor (ps/pF)		35	44	19	39

Macro delays are for 15pF. Use Load Factor to determine the delay for other loads.

$\overline{WA} = A+B$

MACRO: T31 NOR TRANSLATOR
with TTL Tri–State Enable
1 U-CELL
1 LEVEL SERIES GATING



Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (Output Low)	14.8	27.0
VCCT (Output High)	5.8	8.9
VCCT (Output Z)	13.2	24.0
VEEE	2.8	5.4

TRUTH TABLE

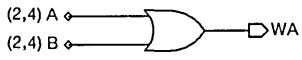
A	B	CT	WA
X	X	H	Z
L	L	L	H
L	H	L	L
H	L	L	L
H	H	L	L

MACRO DELAYS (ps)		LOW POWER ARRAY							
		L MACRO				H MACRO			
IN	OUT	(+)		(–)		(+)		(–)	
A,B	WA	3525		4200		2775		2775	
Load Factor (ps/pF)		41		41		40		20	
		ZH	ZL	HZ	LZ	ZH	ZL	HZ	LZ
CT	WA	5100	8275	3200	3850	3675	4850	2900	3225
Load Factor (ps/pF)		35	62	61	28	49	26	62	27

Tri–state delays listed above include the delay time of the tri–state control gate delay T90.
Macro delays are for 15pF. Use loading factor to determine the delay for other loads.

MACRO: T33 OR TRANSLATOR

1 U-CELL
1 LEVEL SERIES GATING



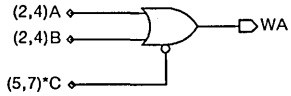
Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (Output Low)	14.8	27.0
VCCT (Output High)	5.8	8.9
VEEE	3.6	7.0

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(−)	(+)	(−)
A,B	WA	3550	3825	2925	2400
Load Factor (ps/pF)		42	44	40	22

Macro delays are for 15 pF. Use Loading Factor to determine the delay for other loads.

WA = A+B

MACRO: T36 OR TRANSLATOR with ECL Tri-State Enable
1 U-CELL
2 LEVEL SERIES GATING



TRUTH TABLE

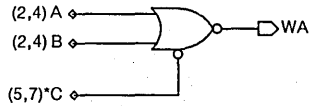
A	B	C	WA
X	X	H	Z
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	H

Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (Output Low)	27.7	41.4
VCCT (Output High)	19.7	24.8
VCCT (Output Z)	29.3	44.5
VEEE (Output High)	12.9	16.8
VEEE (Output Low)	12.9	16.8
VEEE (Output Z)	13.3	17.5
TOTAL (Output Low)	40.6	58.2
TOTAL (Output High)	32.6	41.7
TOTAL (Output Z)	42.6	61.9

MACRO DELAYS (ps)		LOW POWER ARRAY							
		L MACRO				H MACRO			
IN	OUT	(+)		(−)		(+)		(−)	
A,B	WA	3325		3200		2975		1950	
Load Factor (ps/pF)		43		36		39		19	
		ZH	ZL	HZ	LZ	ZH	ZL	HZ	LZ
C	WA	2650	5100	3400	2400	2525	2950	2825	2350
Load Factor (ps/pF)		46	66	59	25	43	30	65	30

Macro delays are for 15 pF. Use Loading Factor to determine the delay for other loads.

MACRO: T37 NOR TRANSLATOR
with ECL Tri-State Enable
1 U-CELL
2 LEVEL SERIES GATING



Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (Output Low)	27.7	41.4
VCCT (Output High)	19.7	24.8
VCCT (Output Z)	29.3	44.5
VEEE (Output High)	12.9	16.8
VEEE (Output Low)	12.9	16.8
VEEE (Output Z)	13.3	17.5
TOTAL (Output Low)	40.6	58.2
TOTAL (Output High)	32.6	41.7
TOTAL (Output Z)	42.6	61.9

TRUTH TABLE

A	B	C	WA
X	X	H	Z
L	L	L	H
L	H	L	L
H	L	L	L
H	H	L	L

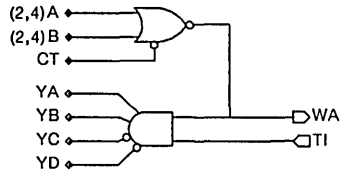
MACRO DELAYS (ps)		LOW POWER ARRAY							
		L MACRO				H MACRO			
IN	OUT	(+)		(-)		(+)		(-)	
A,B	WA	2950		3625		2575		2400	
Load Factor (ps/pF)		43		35		39		18	
		ZH	ZL	HZ	LZ	ZH	ZL	HZ	LZ
C	WA	2650	4500	3400	2375	2550	2900	2825	2300
Load Factor (ps/pF)		46	72	59	24	43	30	65	30

Macro delays are for 15 pF. Use Loading Factor to determine the delay for other loads.

BIDIRECTIONAL I/O [(T: 60–89) MACROS (U–CELLS)]

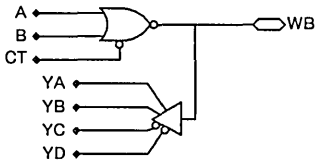
MACRO: T60 ECL 2–INPUT NOR TRANSLATOR and TTL to ECL INPUT BUFFER with TTL Tri–State Enable

1 U-CELL
1 LEVEL SERIES GATING



SIMULATION MODEL

Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (Output Low)	16.6	28.8
VCCT (Output High)	8.4	11.5
VCCT (Output Z) WB +	15.8	26.5
VCCT (Output Z) WB –	15.0	25.7
VEEE	7.2	11.1



ACTUAL CIRCUIT

TRUTH TABLE

A	B	CT	WB	YA,YB	YC,YD
X	X	H	Z	X	X
L	L	L	H	H	L
L	H	L	L	L	H
H	L	L	L	L	H
H	H	L	L	L	H
X	X	H	L	L	H
X	X	H	H	H	L

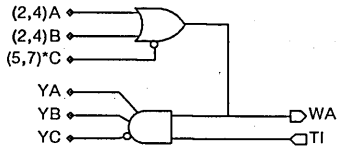
MACRO DELAYS (ps)		LOW POWER ARRAY							
		L MACRO				H MACRO			
IN	OUT	(+)		(–)		(+)		(–)	
A,B	WB	3525		4200		2775		2775	
A,B	YA,YB	4150		5050		3350		3475	
A,B	YC,YD	4950		4225		3375		3450	
Load Factor (ps/pF)		41		41		40		20	
		ZH	ZL	HZ	LZ	ZH	ZL	HZ	LZ
CT	WB	5100	8275	3200	3850	3675	4850	2900	3225
Load Factor (ps/pF)		35	62	61	28	49	26	62	27
WB	YA,YB	625		850		575		700	
WB	YC,YD	750		700		600		675	

Tri-state delays listed above include the delay time of tri-state control gate delay T90. Macro delays are for 15pF.
Use Load Factor to determine the delay for other loads.

9

MACRO: T63 ECL 2–INPUT OR TRANSLATOR and TTL to ECL INPUT BUFFER with ECL Tri–State Enable

1 U-CELL
2 LEVEL SERIES GATING

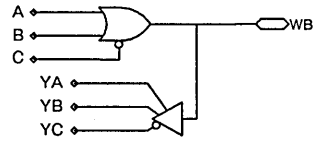


SIMULATION MODEL

Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (WB Low)	29.5	43.1
VCCT (WB High)	22.3	27.4
VCCT (WB ZH)	31.9	47.1
VCCT (WB ZL)	31.1	46.2
VEEE (WB Low)	17.2	22.5
VEEE (WB High)	17.2	22.5
VEEE (WB Z)	17.7	23.2
TOTAL (WB Low)	46.7	65.7
TOTAL (WB High)	39.5	50.0
TOTAL (WB ZH)	49.6	70.2
TOTAL (WB ZL)	48.8	69.4

TRUTH TABLE

A	B	C	WB	YA,YB	YC
X	X	H	Z	X	X
L	L	L	L	L	H
H	X	L	H	H	L
X	H	L	H	H	L
X	X	H	L	L	H
X	X	H	H	H	L



ACTUAL CIRCUIT

MACRO DELAYS (ps)		LOW POWER ARRAY							
		L MACRO				H MACRO			
IN	OUT	(+)		(–)		(+)		(–)	
A,B	WB	3325		3200		2975		1950	
A,B	YA,YB	3950		4050		3550		2650	
A,B	YC	3950		4025		2550		3650	
Load Factor (ps/pF)		43		36		39		19	
		ZH	ZL	HZ	LZ	ZH	ZL	HZ	LZ
C	WB	2650	5100	3400	2400	2525	2950	2825	2350
Load Factor (ps/pF)		46	66	59	25	43	30	65	30
WB	YA,YB	625		850		575		700	
WB	YC	750		700		600		675	

Macro delays are for 15pF. Use Load Factor to determine the delay for other loads.

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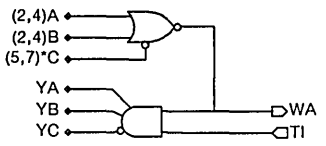
MACRO: T64 ECL 2–INPUT NOR TRANSLATOR and TTL to ECL INPUT BUFFER with ECL Tri–State Enable

1 U-CELL
2 LEVEL SERIES GATING

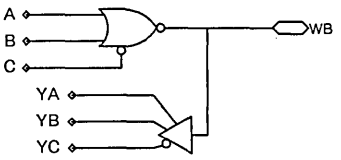


SIMULATION MODEL

Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (WB Low)	29.5	43.1
VCCT (WB High)	22.3	27.4
VCCT (WB ZH)	31.9	47.1
VCCT (WB ZL)	31.1	46.2
VEEE (WB Low)	17.2	22.5
VEEE (WB High)	17.2	22.5
VEEE (WB Z)	17.7	23.2
TOTAL (WB Low)	46.7	65.7
TOTAL (WB High)	39.5	50.0
TOTAL (WB ZH)	49.6	70.2
TOTAL (WB ZL)	48.8	69.4

TRUTH TABLE

A	B	C	WB	YA,YB	YC
X	X	H	Z	X	X
L	L	L	H	H	L
H	X	L	L	L	H
X	H	L	L	L	H
X	X	H	L	L	H
X	X	H	H	H	L



ACTUAL CIRCUIT

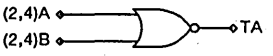
MACRO DELAYS (ps)		LOW POWER ARRAY							
		L MACRO				H MACRO			
IN	OUT	(+)		(–)		(+)		(–)	
A,B	WB	2950		3625		2575		2400	
A,B	YA,YB	3575		4475		3150		3100	
A,B	YC	4375		3650		3000		3250	
Load Factor (ps/pF)		43		36		39		19	
		ZH	ZL	HZ	LZ	ZH	ZL	HZ	LZ
C	WB	2650	4500	3400	2375	2550	2900	2825	2300
Load Factor (ps/pF)		46	66	59	25	43	30	65	30
WB	YA,YB	625		850		575		700	
WB	YC	750		700		600		675	

Macro delays are for 15pF. Use Load Factor to determine the delay for other loads.

ECL to TRI–STATE CONTROL [(T:90) MACROS (U–CELLS)]

MACRO: T90 ECL TO Tri–State Control NOR TRANSLATOR

1 U-CELL
1 LEVEL SERIES GATING



Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (Output Low)	11.6	21.2
VCCT (Output High)	8.6	14.7
VEEE	2.8	5.4

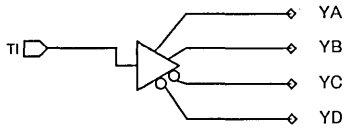
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	TA	2275	2400	1475	1675

Delays for this gate are accounted for in gates with TRI-STATE ENABLES.

$\overline{TA} = A+B$

TTL INPUT to PECL [(P:00–29) MACROS (U–CELLS)]

MACRO: P00 TRANSLATOR
with True and Complement
1 U-CELL
1 LEVEL SERIES GATING



MACRO P00 SYMBOL

Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCE (Output Low)	3.5	4.5
VCCE (Output High)	3.0	4.0

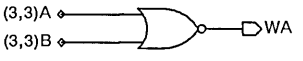
MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(-)	(+)	(-)
TI	YA,YB	250	400	300	325
TI	YC,YD	275	450	200	375

PECL to TTL OUTPUT [(P:30–59) MACROS (U–CELLS)]

NOTE: For all TTL outputs ('WA'), the delays in CAD logic simulation reflect testing loads of 50.0 pF.

MACRO: P30 NOR TRANSLATOR

1 U-CELL
1 LEVEL SERIES GATING



$\overline{WA} = A+B$

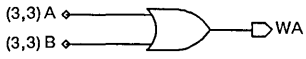
Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (Output Low)	16.4	20.1
VCCT (Output High)	11.4	12.7
VCCE (Output Low)	1.7	1.7
VCCE (Output High)	1.4	1.4
TOTAL (Output Low)	18.1	21.8
TOTAL (Output High)	12.8	14.1

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	WA	4850	5350	3850	4175
Load Factor		28	37	31	26

Macro delays are for 15pF. Use Load Factor to determine the delay for other loads.

MACRO: P33 OR TRANSLATOR

1 U-CELL
1 LEVEL SERIES GATING



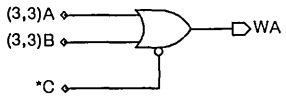
WA = A+B

Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (Output Low)	15.8	19.8
VCCT (Output High)	11.4	13.2
VCCE (Output Low)	1.4	1.4
VCCE (Output High)	1.7	1.7
TOTAL (Output Low)	17.2	21.2
TOTAL (Output High)	13.1	14.9

MACRO DELAYS (ps)		LOW POWER ARRAY			
		L MACRO		H MACRO	
IN	OUT	(+)	(–)	(+)	(–)
A,B	WA	5200	6175	4525	4575
Load Factor (ps/pF)		28	46	31	28

Macro delays are for 15 pF. Use Loading Factor to determine the delay for other loads.

MACRO: P36 OR TRANSLATOR
with PECL Tri-State Enable
1 U-CELL
1 LEVEL SERIES GATING



TRUTH TABLE

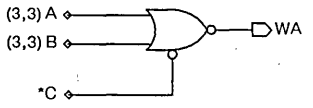
A	B	C	WA
X	X	H	Z
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	H

Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (Output Low)	15.8	19.8
VCCT (Output High)	11.4	13.2
VCCT (Output Z)	16.3	20.0
VCCE (Output Low)	16.8	16.6
VCCE (Output High)	17.1	17.0
VCCE (Output Z)	16.5	16.2
TOTAL (Output Low)	32.6	36.4
TOTAL (Output High)	28.5	30.1
TOTAL (Output Z)	32.8	36.2

MACRO DELAYS (ps)		LOW POWER ARRAY							
		L MACRO				H MACRO			
IN	OUT	(+)		(-)		(+)		(-)	
A,B	WA	6275		6325		5625		4750	
Load Factor (ps/pF)		24		47		30		28	
		ZH	ZL	HZ	LZ	ZH	ZL	HZ	LZ
C	WA	6025	8100	1925	2500	5100	6050	2375	2575
Load Factor (ps/pF)		28	27	57	22	33	32	57	22

Macro delays are for 15 pF. Use Loading Factor to determine the delay for other loads.

MACRO: P37 NOR TRANSLATOR
with PECL Tri-State Enable
1 U-CELL
1 LEVEL SERIES GATING



Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (Output Low)	11.9	19.5
VCCT (Output High)	17.4	12.6
VCCT (Output Z)	17.0	19.5
VCCE (Output Low)	17.9	16.9
VCCE (Output High)	18.2	16.7
VCCE (Output Z)	18.0	16.6
TOTAL (Output Low)	29.8	36.4
TOTAL (Output High)	35.6	29.3
TOTAL (Output Z)	35.0	36.1

TRUTH TABLE

A	B	C	WA
X	X	H	Z
L	L	L	H
L	H	L	L
H	L	L	L
H	H	L	L

MACRO DELAYS (ps)		LOW POWER ARRAY							
		L MACRO				H MACRO			
IN	OUT	(+)		(-)		(+)		(-)	
A,B	WA	5525		5600		5000		4450	
Load Factor (ps/pF)		29		37		24		37	
		ZH	ZL	HZ	LZ	ZH	ZL	HZ	LZ
C	WA	5975	7675	2400	2325	4650	5775	2400	2500
Load Factor (ps/pF)		27	25	57	22	33	32	56	22

Macro delays are for 15 pF. Use Loading Factor to determine the delay for other loads.

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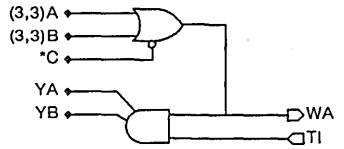
BIDIRECTIONAL I/O [(P:60–89) MACROS (U–CELLS)]

MACRO: P63 PECL 2–INPUT OR TRANSLATOR and TTL to PECL INPUT BUFFER with PECL Tri–State Enable

1 U-CELL
1 LEVEL SERIES GATING

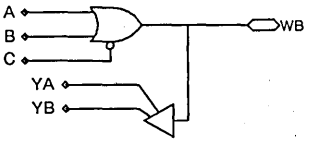


SIMULATION MODEL

Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (WB Low)	15.8	19.8
VCCT (WB High)	11.4	13.2
VCCT (WB Z)	16.3	20.0
VCCE (WB Low)	20.3	21.2
VCCE (WB High)	20.1	21.0
VCCE (WB Z)	20.0	20.8
TOTAL (WB Low)	36.1	41.0
TOTAL (WB High)	31.5	34.2
TOTAL (WB Z)	36.3	40.7

TRUTH TABLE

A	B	C	WB	YA,YB
X	X	H	Z	X
L	L	L	L	L
H	X	L	H	H
X	H	L	H	H
X	X	H	L	L
X	X	H	H	H



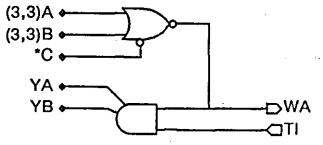
ACTUAL CIRCUIT

MACRO DELAYS (ps)		LOW POWER ARRAY							
		L MACRO				H MACRO			
IN	OUT	(+)		(–)		(+)		(–)	
A,B	WB	6275		6325		5650		4750	
A,B	YA,YB	6525		6725		5925		5050	
Load Factor (ps/pF)		24		47		30		28	
		ZH	ZL	HZ	LZ	ZH	ZL	HZ	LZ
C	WB	6025	8100	1925	2500	5100	6050	2375	2575
Load Factor (ps/pF)		28	27	57	22	33	32	57	22
WB	YA,YB	250		400		300		325	

Macro delays are for 15pF. Use Load Factor to determine the delay for other loads.

MACRO: P64 PECL 2–INPUT NOR TRANSLATOR and TTL to PECL INPUT BUFFER with PECL Tri–State Enable

1 U-CELL
1 LEVEL SERIES GATING

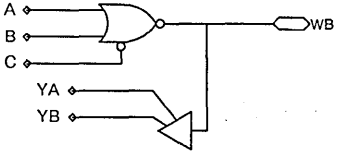


SIMULATION MODEL

Power (mW)	LOW POWER ARRAY	
	L MACRO	H MACRO
VCCT (WB Low)	11.9	19.6
VCCT (WB High)	17.4	12.6
VCCT (WB Z)	17.0	19.5
VCCE (WB Low)	21.4	21.5
VCCE (WB High)	21.2	20.7
VCCE (WB Z)	21.5	21.1
TOTAL (WB Low)	33.3	41.0
TOTAL (WB High)	38.6	33.3
TOTAL (WB Z)	38.5	40.7

TRUTH TABLE

A	B	C	WB	YA,YB
X	X	H	Z	X
L	L	L	H	H
H	X	L	L	L
X	H	L	L	L
X	X	H	L	L
X	X	H	H	H



ACTUAL CIRCUIT

MACRO DELAYS (ps)		LOW POWER ARRAY							
		L MACRO				H MACRO			
IN	OUT	(+)		(–)		(+)		(–)	
A,B	WB	5525		5600		5000		4450	
A,B	YA,YB	5775		6000		5275		4750	
Load Factor (ps/pF)		29		37		24		37	
		ZH	ZL	HZ	LZ	ZH	ZL	HZ	LZ
C	WB	5975	7675	2400	2350	4650	5775	2400	2500
Load Factor (ps/pF)		27	25	57	22	33	32	56	22
WB	YA,YB	250		400		300		325	

Macro delays are for 15pF. Use Load Factor to determine the delay for other loads.

9

10. Appendices

10.1 MCA3 Series Reference Guide

Tables 10–1 through 10–3 contain the available MCA3 Series arrays and features, internal macrocells, and I/O cells respectively. It is included here for reference only. The ECL arrays are described in the MCA3 ECL Series Design Manual.

TABLE 10–1 MCA3 Series Arrays and Features

Array			# of M–Cells	# of I–Cells	# of O–Cells	# of U–Cells	Die Pads	Package Type	# of I/O
ECL	MCA2200ECL	HPA	68	96	96	–	132	135 PGA	108
ECL	MCA10000ECL	LPA/ HPA	414	224	200	–	252	235 PGA	180
							360	289 PGA	256
							360	360 TAB	256
ETL	MCA750ETL	LPA	24	–	–	42	64	64 QFP	42
ETL	MCA3200ETL	LPA	110	–	–	120	208	169 PGA	120
ETL	MCA6200ETL	LPA	225	–	–	168	292	224 PGA	168

TABLE 10–2 MCA3 Series Internal (M) Macrocells

INTERNAL (M) MACROS

MACRO	FUNCTION	SIZE (M–Cells)	S G	10K ECL LPA	10K ECL HPA	2200 ECL HPA	ETL LPA
L/H200	5–INPUT OR/NOR	1/4 CELL	1	L/H	L/H	L/H	L/H
L/H201	4–INPUT OR/NOR	1/4 CELL	1	L/H	L/H	L/H	L/H
L/H202	2–INPUT OR/NOR	1/4 CELL	1	L/H	L/H	L/H	L/H
L/H203	8–INPUT OR/NOR	1/2 CELL	2	L/H	L/H	L/H	L/H
L204	12–INPUT OR/NOR	1/2 CELL	1	L	L	L	L
L/H207	6–INPUT OR/NOR	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H211	2–2 OR/AND	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H212	3–2–2–2 OR/AND	1/2 CELL	2	L/H	L/H	L/H	L/H
L213	4–3–3–3 OR/AND	1/2 CELL	1	L	L	L	L
L/H214	2–2–2–2–1–1–1–1 OR/AND	FULL CELL	2	L/H	L/H	L/H	L/H
L/H215	2–2–3–3–3 OR/AND	FULL CELL	2	L/H	L/H	L/H	L/H
L/H216	4–2–3–2–3 OR/AND	FULL CELL	2	L/H	L/H	L/H	L/H
L217	5–4–3–2 OR/AND	1/2 CELL	1	L	L	L	L
L/H218	5–4–3–2–1 OR/AND	FULL CELL	2	L/H	L/H	L/H	L/H
L/H219	3–3 OR/AND	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H221	2–2 OR/EXOR	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H222	DUAL 2–2 OR/AND/EXNOR	FULL CELL	2	L/H	L/H	L/H	L/H
L/H223	4–INPUT EXNOR	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H224	4–INPUT EXOR	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H225	2–1–1–2 OR/AND/EXOR	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H226	2–1–1–2 OR/AND/EXNOR	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H227	2–1 EXOR/AND/NAND	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H228	2–1 AND/EXOR	1/4 CELL	2	L/H	L/H	L/H	L/H
L251	4–TO–1 MUX W/ENABLE (LOW)	1/2 CELL	2	L	L	L	L
L/H252	QUAD 2–TO–1 MUX	FULL CELL	2	L/H	L/H	L/H	L/H
L/H253	2–TO–1 MUX W/ENABLE (LOW)	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H254	2–TO–1 MUX W/GATED INPUTS	1/4 CELL	2	L/H	L/H	L/H	L/H

TABLE 10–2 MCA3 Series Internal (M) Macrocells [continued]

INTERNAL (M) MACROS

MACRO	FUNCTION	SIZE (M–Cells)	S G	10K ECL LPA	10K ECL HPA	2200 ECL HPA	ETL LPA
L/H255	DUAL 2–TO–1 MUX W/COM. SELECT	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H256	2–TO–1 MUX	1/4 CELL	2	L/H	L/H	L/H	L/H
L258	4–TO–1 MUX W/ENABLE (HIGH)	1/2 CELL	2	L	L	L	L
L/H259	4–TO–1 MUX	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H261	1–OF–4 DECODER W/ENABLE (LOW)	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H262	1–OF–4 DECODER W/ENABLE (HIGH)	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H263	1–OF–4 DECODER (HIGH)	FULL CELL	2	L/H	L/H	L/H	L/H
L/H277	4–2–4–2–4–2 OR/AND	3/4 CELL	2	L/H	L/H	L/H	L/H
L/H278	3 DATA INPUT DATA LATCH	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H279	4–2–4–2–4–2–4–2 OR/AND	FULL CELL	2	L/H	L/H	L/H	L/H
L/H280	4–2–4–2 OR/AND	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H281	FULL ADDER	FULL CELL	2	L/H	L/H	L/H	L/H
L/H282	FULL ADDER W/GATED INPUTS	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H283	2–BIT LOOK–AHEAD CARRY	FULL CELL	2	L/H	L/H	L/H	L/H
L/H284	HALF ADDER W/GATED INPUTS	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H285	3–BIT ADDER (SUM)	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H286	3–BIT ADDER (CARRY)	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H290	D FLIP–FLOP WITH SET AND RESET	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H291	D FLIP–FLOP WITH RESET	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H292	D FLIP–FLOP WITH MUX	3/4 CELL	2	L/H	L/H	L/H	L/H
L/H293	D LATCH WITH RESET	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H294	D LATCH WITH MUX	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H295	GATED 2–WAY D LATCH	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H296	EXNOR D LATCH	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H297	GATED 4–WAY D LATCH	3/4 CELL	2	L/H	L/H	L/H	L/H
L/H298	DUAL D LATCH W/RESET	1/2 CELL	2	L/H	L/H	L/H	L/H
L302	INPUT OR/NOR (High Drive)	1/2 CELL	1	L			L
L/H310	4–4–4–4 OR/AND	FULL CELL	1	L/H	L/H	L/H	L/H
L/H311	3–3–3–3 AND/OR	FULL CELL	2	L/H	L/H	L/H	L/H
L/H312	3–3–3 AND/OR	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H313	2–2 OR/AND	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H315	2–2–1–1 OR/AND	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H318	3–3 AND/OR	1/2 CELL	1	L/H	L/H	L/H	L/H
L319	3–3–2–1 AND/OR	1/2 CELL	2	L	L	L	L
L/H320	2–3–4–4 AND/OR W/ENABLE (HIGH)	FULL CELL	2	L/H	L/H	L/H	L/H
L/H321	6–6–4–4–2–2 OR/AND	FULL CELL	2	L/H	L/H	L/H	L/H
L322	3–3–3 AND/OR	1/2 CELL	1	L	L	L	L
L/H323	3–2–2–2–2–3 AND/OR	FULL CELL	2	L/H	L/H	L/H	L/H
L/H324	5–5–5–5 AND/OR	FULL CELL	1	L/H	L/H	L/H	L/H
L328	2–1 AND/EXOR (High Drive)	1/2 CELL	2	L			L
L/H331	3–2–2 AND/OR	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H332	GATED OR	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H333	GATED OR	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H370	DIFFERENTIAL LINE RECEIVER	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H371	2–1 MUX WITH DIFFERENTIAL INPUTS	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H372	D FLIP–FLOP W/DIFFERENTIAL CLOCK AND DATA	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H373	2–1 MUX W/DIFF INPUTS AND DIFF MUX CTL	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H374	DIFFERENTIAL LINE RECEIVER	1/4 CELL	1	L/H	L/H	L/H	L/H
L/H375	D FLIP–FLOP WITH DIFFERENTIAL CLOCK	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H376	D FLIP–FLOP WITH DIFFERENTIAL CLOCK	1/2 CELL	2	L/H	L/H	L/H	L/H
L380	NOR LATCH	1/4 CELL	1	L	L	L	L
L/H381	D FLIP–FLOP WITH SET	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H391	D FLIP–FLOP, NEGATIVE EDGE TRIGGERED	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H392	D FLIP–FLOP WITH MUX, NEG. EDGE TRIGGERED	3/4 CELL	2	L/H	L/H	L/H	L/H

TABLE 10–2 MCA3 Series Internal (M) Macrocells [continued]

INTERNAL (M) MACROS

MACRO	FUNCTION	SIZE (M–Cells)	S G	10K ECL LPA	10K ECL HPA	2200 ECL HPA	ETL LPA
L/H393	D LATCH WITH CLOCK ENABLE (HIGH)	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H394	D FLIP–FLOP WITH MUX, NEG. EDGE TRIGGERED	FULL CELL	2	L/H	L/H	L/H	L/H
L/H395	D FLIP–FLOP WITH ASYN SET AND DATA ENABLE	FULL CELL	2	L/H	L/H	L/H	L/H
L/H396	SCAN D FLIP FLOP	FULL CELL	2	L/H	L/H	L/H	L/H
L/H397	D LATCH WITH ASYN SET	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H398	SCAN D LATCH W/ASYN SET	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H400	12–INPUT OR	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H401	12–INPUT NOR	1/4 CELL	2	L/H	L/H	L/H	L/H
L402	2–INPUT OR/NOR, 3–INPUT OR/NOR	1/4 CELL	1	L	L	L	L
L/H403	8–INPUT OR/NOR	1/4 CELL	1	L/H	L/H	L/H	L/H
L/H404	12–INPUT NOR	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H411	2–2–2 OR/AND	1/4 CELL	3	L/H	L/H	L/H	L/H
L/H413	4–3–3–3 OR/AND	1/2 CELL	2	L/H	L/H	L/H	L/H
L414	3–3–3–3 OR/AND	1/2 CELL	2	L	L	L	L
L/H416	4–2–3–2–3 OR/AND	FULL CELL	3	L/H	L/H	L/H	L/H
L/H417	5–4–3–2 OR/AND	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H418	5–4–3–2–1 OR/AND	3/4 CELL	2	L/H	L/H	L/H	L/H
L/H419	4–4 OR/AND	1/4 CELL	2	L/H	L/H	L/H	L/H
L421	DUAL EXOR	1/4 CELL	2	L			L
L/H422	DUAL 2–2 OR/AND/EXOR	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H424	6–INPUT EXNOR	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H425	6–INPUT EXOR	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H427	2–1 EXOR/AND/NAND	1/4 CELL	3	L/H	L/H	L/H	L/H
L/H438	6–5–4–3–2–1 OR/AND	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H451	4–1 MUX W/ENABLE(LOW)	1/2 CELL	3	L/H	L/H	L/H	L/H
L452	QUAD 2–TO–1 MUX	1/2 CELL	2	L	L	L	L
L/H453	2–TO–1 MUX W/ENABLE(LOW)	1/4 CELL	3	L/H	L/H	L/H	L/H
L/H454	2–TO–1 MUX W/ENABLE(HIGH)	1/4 CELL	3	L/H	L/H	L/H	L/H
L/H455	DUAL 2–TO–1 MUX W/ENABLE (HIGH)	1/2 CELL	3	L/H	L/H	L/H	L/H
L456	TRIPLE 2–TO–1 MUX(COMMON SELECT)	1/2 CELL	2	L	L	L	L
L457	TRIPLE 2–TO–1 MUX	1/2 CELL	2	L	L	L	L
L/H458	4–1 MUX W/ENABLE(HIGH)	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H459	DUAL 4–1 MUX	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H461	1–OF–4 DECODER WITH ENABLE(LOW)	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H462	1–OF–4 DECODER WITH ENABLE(HIGH)	1/2 CELL	3	L/H	L/H	L/H	L/H
L464	8–3 ENCODER	FULL CELL	3	L	L	L	L
L/H465	1–OF–4 DECODER WITH ENABLE(LOW)	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H466	1–OF–4 DECODER WITH ENABLE(HIGH)	1/2 CELL	3	L/H	L/H	L/H	L/H
L470	DUAL 2–TO–1 MUX(COMMON SELECT)	1/4 CELL	2	L	L	L	L
L474	DIFFERENTIAL LINE RECEIVER (High Drive)	1/2 CELL	2	L			L
L482	TRIPLE FULL ADDER	FULL CELL	2	L	L	L	L
L/H485	3–BIT ADDER	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H501	2–INPUT OR (Quad Buffer)	1/4 CELL	1	L/H	H	H	L/H
L/H502	2–INPUT NOR (Quad Buffer)	1/4 CELL	1	L/H	H	H	L/H
L503	5x2 INPUT OR	1/2 CELL	1	L	L	L	L
L/H510	4–4–4–4 OR/AND	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H511	3–3–3–3 AND/OR	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H512	3–3–3 AND/OR	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H513	3–1–1–1 OR/AND	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H518	3–3 AND/OR	1/4 CELL	2	L/H	L/H	L/H	L/H
L/H519	3–3–2–1 AND/OR	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H520	2–3–4–4 AND/OR W/ENABLE(HIGH)	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H523	3–2–2–2–2–3 AND/OR	FULL CELL	3	L/H	L/H	L/H	L/H

TABLE 10–2 MCA3 Series Internal (M) Macrocells [continued]

INTERNAL (M) MACROS

MACRO	FUNCTION	SIZE (M–Cells)	S G	10K ECL LPA	10K ECL HPA	2200 ECL HPA	ETL LPA
H553	2–TO–1 MUX W/ENABLE LOW	1/4 CELL	2	H	H	H	H
L/H571	8–OUTPUT BUFFER W/DIFF IN AND ENABLE (Quad Buffer)	1/2 CELL	3	L/H	H	H	L/H
L585	SCAN D FLIP–FLOP W/2to 1 MUX /OR	1/2 CELL	2	L	L	L	L
L593	W BUFFER	1/4 CELL	1	L	L	L	L
L/H611	3–3–3 OR/AND	1/4 CELL	3	L/H	L/H	L/H	L/H
L/H616	4–2–3–3–2 OR/AND	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H618	5–4–3–2–1 OR/AND	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H658	4–1 MUX	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H685	FULL ADDER W/GATED INPUTS	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H691	D FLIP–FLOP W/RESET	1/2 CELL	2	L/H	L/H	L/H	L/H
L/H692	D FLIP–FLOP WITH MUX	3/4 CELL	2	L/H	L/H	L/H	L/H
L/H694	D FLIP–FLOP W/RESET (NEGATIVE HOLD TIME)	1/2 CELL	2	L/H	L/H	L/H	L/H
L700	DIFFERENTIAL LINE RECEIVER (High Drive)	1/2 CELL	1				L
L701	2–TO–1 MUX W/DIFFERENTIAL INPUTS AND DIFFERENTIAL MUX CONTROL (Hight Drive)	1/2 CELL	2				L
H710	D FLIP–FLOP WITH DIFF CLOCK AND DATA	1/2 CELL	2				H
H711	D FLIP–FLOP W/GATED DATA INPUT & DIFF CLK	1/2 CELL	2				H
H712	D FLIP–FLOP W/EXNOR GATED DATA INPUT AND DIFFERENTIAL CLOCK	FULL CELL	3				H
L713	D FLIP–FLOP W/DIFF CLK AND DATA (HI Drive)	FULL CELL	2				L
L714	D FLIP–FLOP W/GATED DATA INPUT AND DIFFERENTIAL CLOCK (High Drive)	FULL CELL	2				L
L/H802	3–INPUT EXOR/EXNOR	1/4 CELL	3	L/H	L/H	L/H	L/H
L/H803	3–INPUT EXOR/EXNOR	1/4 CELL	3	L/H	L/H	L/H	L/H
L804	DUAL 2–INPUT AND	1/4 CELL	2	L	L	L	L
L805	DUAL 2–INPUT NAND	1/4 CELL	2	L	L	L	L
L806	DUAL 2–INPUT AND/NAND	1/4 CELL	2	L	L	L	L
L807	DUAL 2–INPUT AND/NAND	1/4 CELL	2	L	L	L	L
L/H809	8–1 MUX WITH ENABLE (HIGH)	FULL CELL	3	L/H	L/H	L/H	L/H
L/H810	8–1 MUX WITH ENABLE (HIGH)	FULL CELL	3	L/H	L/H	L/H	L/H
L811	DUAL 4–INPUT OR	1/4 CELL	1	L	L	L	L
L812	DUAL 4–INPUT OR/NOR	1/4 CELL	1	L	L	L	L
L813	DUAL 4–INPUT OR/NOR	1/4 CELL	1	L	L	L	L
L814	DUAL 4–INPUT NOR	1/4 CELL	1	L	L	L	L
L815	DUAL 2–INPUT OR	1/4 CELL	1	L	L	L	L
L816	DUAL 2–INPUT OR/NOR	1/4 CELL	1	L	L	L	L
L817	DUAL 2–INPUT OR/NOR	1/4 CELL	1	L	L	L	L
L818	DUAL 2–INPUT NOR	1/4 CELL	1	L	L	L	L
L/H819	3–2–1 OR/AND	1/4 CELL	3	L/H	L/H	L/H	L/H
L820	2–INPUT OR, 2–INPUT AND	1/4 CELL	2	L	L	L	L
L850	EXPANDABLE 2–1 MUX(CODER) AND 2x2–1 MUX	1/2 CELL	2	L	L	L	L
L851	EXPANDABLE 2–1 MUX	1/2 CELL	2	L	L	L	L
L852	EXPANDABLE 2–1 MUX	1/2 CELL	2	L	L	L	L
L853	EXPANDABLE 2–1 MUX	1/2 CELL	2	L	L	L	L
L860	EXPANDABLE 4–1 MUX(CODER) WITH ENABLE	1/2 CELL	3	L	L	L	L
L/H861	EXPANDABLE 4–1 MUX	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H862	EXPANDABLE 4–1 MUX	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H863	EXPANDABLE 4–1 MUX	1/2 CELL	3	L/H	L/H	L/H	L/H
L870	EXPANDABLE 8–1 MUX(CODER)	1/2 CELL	3	L	L	L	L
L/H871	EXPANDABLE 8–1 MUX	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H872	EXPANDABLE 8–1 MUX	1/2 CELL	3	L/H	L/H	L/H	L/H
L/H873	EXPANDABLE 8–1 MUX	1/2 CELL	3	L/H	L/H	L/H	L/H
L881	DUAL D (INVERTING) FLIP–FLOP	1/2 CELL	2			L	L

TABLE 10–2 MCA3 Series Internal (M) Macrocells [continued]

INTERNAL (M) MACROS

MACRO	FUNCTION	SIZE (M–Cells)	S G	10K ECL LPA	10K ECL HPA	2200 ECL HPA	ETL LPA
L882	DUAL D FLIP–FLOP	1/2 CELL	2			L	L
L891	DUAL D (INVERTING) FLIP–FLOP	1/2 CELL	2	L	L		
L892	DUAL D FLIP–FLOP	1/2 CELL	2	L	L		
L893	3xD LATCH WITH COMMON CLOCK	1/2 CELL	2	L	L	L	L
L/H894	D LATCH WITH MUX	1/4 CELL	3	L/H	L/H	L/H	L/H
L895	D FLIP–FLOP	1/4 CELL	2	L	L	L	L
L896	3xD LATCH W/ COMMON CLK & RESET	1/2 CELL	2	L	L	L	L
L897	DUAL LATCH W/ COMMON ENABLE	1/4 CELL	2	L			

TABLE 10–3 MCA3 Series I/O, and Misc. Cells

MACRO	FUNCTION	SIZE/ TYPE	S G	10K ECL LPA	10K ECL HPA	2200 ECL HPA	ETL LPA
INPUT INTERFACE (I) MACROCELLS							
L/HI00	2–INPUT OR/NOR	1 I–CELL	1	L/H	L/H	L/H	
L/HI01	2–INPUT OR (H MACRO, HPA ONLY)	1 I–CELL	1	L/H	H	H	
L/HI02	2–INPUT NOR (H MACRO, HPA ONLY)	1 I–CELL	1	L/H	H	H	
L/HI03	DIFFERENTIAL BUFFER	1 I–CELL	1	L/H	L/H	L/H	
L/HI04	DIFFERENTIAL BUFFER (L MACRO, LPA ONLY)	1 I–CELL	2	L/H	H	H	
L/HI05	DIFFERENTIAL BUFFER (L MACRO, LPA ONLY)	1 I–CELL	1	L/H	H	H	
L/HI06	INPUT BUFFER	1 I–CELL	1	L/H	L/H	L/H	
L/HI07	INPUT BUFFER (L MACRO, LPA ONLY)	1 I–CELL	1	L/H	H	H	
L/HI08	INPUT BUFFER (L MACRO, LPA ONLY)	1 I–CELL	1	L/H	H	H	
X MACROS (O–CELLS)							
L/HX01	2–INPUT OR/NOR	1 O–CELL	1	L/H	L/H	L/H	
L/HX02	4–INPUT OR/NOR	1 O–CELL	1	L/H	L/H	L/H	
L/HX03	2–2 OR GATES	1 O–CELL	2	L/H	L/H	L/H	
L/HX04	2–2 OR GATES	1 O–CELL	2	L/H	L/H	L/H	
L/HX05	5–INPUT OR/NOR	1 O–CELL	1	L/H	L/H	L/H	
L/HX06	8–INPUT OR/NOR	2 O–CELLS	2	L/H	L/H	L/H	
L/HX07	DUAL AND/OR	2 O–CELLS	2	L/H	L/H	L/H	
L/HX08	DUAL AND/OR	2 O–CELLS	2	L/H	L/H	L/H	
L/HX11	2–2 OR/AND	1 O–CELL	2	L/H	L/H	L/H	
L/HX21	2–2 OR/EXOR	1 O–CELL	2	L/H	L/H	L/H	
L/HX51	2–TO–1 MUX	1 O–CELL	2	L/H	L/H	L/H	
L/HX52	DUAL 2–TO–1 MUX	2 O–CELLS	2	L/H	L/H	L/H	
L/HX53	2–TO–1 MUX WITH ENABLE(LOW)	1 O–CELL	2	L/H	L/H	L/H	
L/HX58	4–TO–1 MUX	2 O–CELLS	3	L/H	L/H	L/H	
LX59	4–TO–1 MUX (Y OUTPUTS)	2 O–CELLS	3	L	L	L	
L/HX71	DIFFERENTIAL BUFFER	1 O–CELL	2	L/H	L/H	L/H	
L/HX91	D FLIP–FLOP W/RESET	2 O–CELLS	2	L/H	L/H	L/H	
L/HX92	D LATCH WITH RESET	1 O–CELL	2	L/H	L/H	L/H	
L/HX93	DUAL D LATCH WITH RESET	2 O–CELLS	2	L/H	L/H	L/H	
L/HX94	D FLIP–FLOP W/RESET	2 O–CELLS	2	L/H	L/H	L/H	
ZX MACROS (O–CELLS)							
ZX01	2–INPUT OR (50 OHM CUTOFF DRIVER)	1 O–CELL	1	L	L	L	
ZX02	4–INPUT OR (50 OHM CUTOFF DRIVER)	1 O–CELL	1	L	L	L	
ZX03	2–2 OR (50 OHM CUTOFF DRIVER)	1 O–CELL	2	L	L	L	
ZX04	2–2 OR (50 OHM CUTOFF DRIVER)	1 O–CELL	2	L	L	L	
ZX05	5–INPUT OR (50 OHM CUTOFF DRIVER)	1 O–CELL	1	L	L	L	
ZX06	8–INPUT OR (50 OHM CUTOFF DRIVER)	2 O–CELL	2	L	L	L	

TABLE 10–3 MCA3 Series I/O, and Misc. Cells [continued]

MACRO	FUNCTION	SIZE/ TYPE	S G	10K ECL LPA	10K ECL HPA	2200 ECL HPA	ETL LPA
ZX07	DUAL AND/OR (50 OHM CUTOFF DRIVER)	2 O–CELL	2	L	L	L	
ZX11	2–2 OR/AND (CUTOFF)	1 O–CELL	2	L	L	L	
ZX51	2–TO–1 MUX (CUTOFF)	1 O–CELL	2	L	L	L	
ZX52	DUAL 2–TO–1 MUX (CUTOFF)	2 O–CELL	2	L	L	L	
ZX58	4–TO–1 MUX (CUTOFF)	2 O–CELL	3	L	L	L	
ZX71	DIFFERENTIAL BUFFER (CUTOFF)	1 O–CELL	2	L	L	L	
ZX81	25 OHM OR/NOR DRIVER (CUTOFF)	1 O–CELL	2	L			
ZX82	4–INPUT OR GATE (25 OHM CUTOFF DRIVER)	1 O–CELL	2	L			
ZX83	2–2 OR GATES (25 OHM CUTOFF DRIVER)	2 O–CELL	3	L			
ZX84	2–2 OR GATES (25 OHM CUTOFF DRIVER)	2 O–CELL	3	L			
ZX85	8–INPUT OR GATE (25 OHM CUTOFF DRIVER)	2 O–CELL	2	L			
ZX86	2–2 OR/AND (25 OHM CUTOFF DRIVER)	2 O–CELL	3	L			
ZX87	2–TO–1 MUX (25 OHM CUTOFF DRIVER)	2 O–CELL	3	L			
CLOCK BUFFER MACROS							
CLK5	DIFFERENTIAL CLOCK GENERATOR (5 GATES)	CLK CELL	2	L	L		
CLK6	DIFFERENTIAL CLOCK GENERATOR (6 GATES)	CLK CELL	2	L	L		
CLK7	DIFFERENTIAL CLOCK GENERATOR (6 GATES + EXT. GATES)	CLK CELL	2	L	L		
STANDARD ECL OUTPUTS							
VO25	25 OHM PAD CELL	PAD CELL		YES			
VO50	50/68 OHM PAD CELL	PAD CELL		YES	YES	YES	
BIDIRECTIONAL I/O CELLS							
VB25	25 OHM BIDIRECTIONAL PAD CELL	PAD CELL		YES			
VB50	50 OHM BIDIRECTIONAL PAD CELL	PAD CELL		YES	YES	YES	
VBS0	BIDIRECTIONAL STECL BUFFER	PAD CELL		YES	YES		
SERIES–TERMINATED (STECL) OUTPUTS							
VS00	STECL PAD CELL – 0 OHMS SERIES	PAD CELL		YES	YES		
VS27	STECL PAD CELL – 27 OHMS SERIES	PAD CELL		YES	YES		
VS40	STECL PAD CELL – 40 OHMS SERIES	PAD CELL		YES	YES		

ETL INPUT/OUTPUT INTERFACE MACROS

MACRO	FUNCTION	Size/Type	S G	10K ECL LPA	10K ECL HPA	2200 ECL HPA	ETL LPA
ECL INPUT INTERFACE (C) MACROS							
L/HC01	INPUT BUFFER (Non-Inverting) Quad Buffer	1-U CELL	1				L/H
L/HC02	INPUT BUFFER (Inverting) Quad Buffer	1-U CELL	1				L/H
L/HC03	INPUT BUFFER (Inverting, Non-Inverting)	1-U CELL	1				L/H
L/HC05	DUAL DIFFERENTIAL INPUT BUFFER	2-U CELL	1				L/H
L/HC13	DIFFERENTIAL INPUT BUFFER	2-U CELL	1				L/H
LC15	DIFFERENTIAL BYPASS	2-U CELL	1				L
L/HC50	INPUT LATCH with ENABLE LOW	1-U CELL	1				L/H
LC70	DIFFERENTIAL INPUT BUFFER WITH OFF CHIP TERMINATION INPUTS (High Drive)	2-U CELLS	1				L
ECL OUTPUT DRIVERS (E) MACROS, 60 & 50 ohm							
L/HE01	2-INPUT OR	1-U CELL	1				L/H
L/HE02	2-INPUT NOR	1-U CELL	1				L/H
L/HE03	4-INPUT OR	1-U CELL	1				L/H
L/HE04	4-INPUT NOR	1-U CELL	1				L/H
L/HE05	2-TO-1 MUX	1-U CELL	2				L/H
L/HE06	2-2 OR/AND	1-U CELL	2				L/H
L/HE07	2-2 OR/EXOR	1-U CELL	2				L/H
HE08	2-TO-1 MUX with ENABE LOW (Inverting)	1-U CELL	2				H
HE09	2-TO-1 MUX with ENABE LOW (Non-Inverting)	1-U CELL	2				H
L/HE10	2-2 OR/NAND	1-U CELL	2				L/H
L/HE11	2-TO-1 MUX with ENABLE LOW	1-U CELL	2				L/H
L/HE12	DIFFERENTIAL OUTPUT BUFFER	2-U CELL	1				L/H
L/HE50	D LATCH with CLOCK ENABLE LOW	1-U CELL	2				L/H
HE70	DIFFERENTIAL OUTPUT BUFFER	2-U CELLS	1				H
HE71	OPEN COLLECTOR DIFF OUTPUT BUFFER	2-U CELLS	1				H
LE75	OFF-CHIP TERMINATION PAD	1-U CELL	1				L
ECL CUTOFF OUTPUT (ZE) MACROS, 50 & 25 ohm							
ZE00	4-INPUT OR (50 ohm)	1-U CELL	1				L
ZE50	4-INPUT OR (25 ohm)	1-U CELL	2				L
ECL STECL I/O (S) MACROS							
LS00	2-INPUT OR	1-U CELL	1				L
LS50	INPUT BUFFER	1-U CELL	1				L
ECL BIDIRECTIONAL I/O (B) MACROS, 50 & 25 ohm							
HB26	2-2 OR/AND with INPUT BUFFER (50 ohm output)	1-U CELL	2				H
HB27	2-2 OR/NAND with INPUT BUFFER (50 ohm output)	1-U CELL	2				H
HB28	2-TO-1 MUX LOW ENABLE with INPUT BUFFER (50 ohm output)	1-U CELL	2				H
HB29	4-INPUT OR with INPUT BUFFER (50 ohm output)	1-U CELL	1				H
HB30	4-INPUT NOR with INPUT BUFFER (50 ohm output)	1-U CELL	1				H
HB50	4-INPUT OR with INPUT BUFFER (25 ohm cutoff output)	1-U CELL	2				H
HB51	4-INPUT NOR with INPUT BUFFER (25 ohm cutoff output)	1-U CELL	2				H
HB76	4-INPUT NOR with INPUT BUFFER (50 ohm cutoff output)	1-U CELL	1				H
TTL TO ECL INPUT (T: 00-29) MACROS							
L/HT00	TRANSLATOR with True and Complement	1-U CELL	1				L/H

ETL INPUT/OUTPUT INTERFACE MACROS

MACRO	FUNCTION	Size/Type	S G	10K ECL LPA	10K ECL HPA	2200 ECL HPA	ETL LPA
ECL TO TTL OUTPUT (T: 30–59) MACROS							
L/HT30	NOR TRANSLATOR	1–U CELL	1				L/H
L/HT31	NOR TRANSLATOR with TTL Tri–State Enable	1–U CELL	1				L/H
L/HT33	OR TRANSLATOR	1–U CELL	1				L/H
L/HT36	OR TRANSLATOR with ECL Tri–State Enable	1–U CELL	1				L/H
L/HT37	NOR TRANSLATOR with ECL Tri–State Enable	1–U CELL	1				L/H
TTL BIDIRECTIONAL I/O (T: 60–89) MACROS							
L/HT60	ECL 2–INPUT NOR TRANSLATOR and TTL to ECL INPUT BUFFER with TTL Tri–State Enable	1–U CELL	1				L/H
L/HT63	ECL 2–INPUT OR TRANSLATOR and TTL to ECL INPUT BUFFER with ECL Tri–State Enable	1–U CELL	1				L/H
L/HT64	ECL 2–INPUT NOR TRANSLATOR and TTL to ECL INPUT BUFFER with ECL Tri–State Enable	1–U CELL	1				L/H
ECL TO TRI–STATE CONTROL (T: 90) MACROS							
L/HT90	ECL to Tri–State Control NOR TRANSLATOR	1–U CELL	1				L/H
TTL TO PECL INPUT (P: 00–29) MACROS							
L/HP00	TRANSLATOR with True and Complement	1–U CELL	1				L/H
PECL TO TTL OUTPUT (P: 30–59) MACROS							
L/HP30	NOR TRANSLATOR	1–U CELL	1				L/H
L/HP33	OR TRANSLATOR	1–U CELL	1				L/H
L/HP36	OR TRANSLATOR with PECL Tri–State Enable	1–U CELL	1				L/H
L/HP37	NOR TRANSLATOR with PECL Tri–State Enable	1–U CELL	1				L/H
TTL BIDIRECTIONAL I/O (P: 60–89) MACROS							
L/HP63	PECL 2–INPUT OR TRANSLATOR and TTL to PECL INPUT BUFFER with PECL Tri–State Enable	1–U CELL	1				L/H
L/HP64	PECL 2–INPUT NOR TRANSLATOR and TTL to PECL INPUT BUFFER with PECL Tri–State Enable	1–U CELL	1				L/H

10.2 DC Electrical Characteristics

MCA3 ETL arrays are available in the following options:

100K operating at −4.5 Vdc (ECL) with 5.0 Vdc (TTL)
100K operating at −5.2 Vdc (ECL) with 5.0 Vdc (TTL)
PETL Operating at 5.0 Vdc (PECL and TTL)

10.2.1 ECL and TTL Characteristics

The power supply voltage limits for the following tables are:

V_{CCE} = V_{CCO} = 0 volts
V_{EEE} = −4.2 to −4.8 volts *or*
V_{EEE} = −4.784 to −5.616 volts

V_{CCT} = 4.75 to 5.25 volts
V_{EET} = 0 volts

100K COMPATIBLE OPTIONS – ECL OUTPUTS

Symbol	Characteristic	Specification Limits T_J = 25 to 115 °C Min	Typ	Max	Unit
V_{OH}[1]	Output HIGH Voltage	−1025	−955	−880	mV
V_{OH}[2]	Output HIGH Voltage (low power)	−1045	−975	−880	mV
V_{OH}[3]	Output HIGH Voltage (cutoff)	−1050	−910	−735	mV
V_{OL}	Output LOW Voltage	−1810	−1705	−1620	mV
V_{OL}[3]	Output LOW Voltage (cutoff)	−2020	−1985	−1950	mV
I_{OH}[4]	Output HIGH Current (CML output)	--	0	1.0	mA
I_{OL}[4]	Output LOW Current (CML output)	15.5	13.0	10.5	mA
V_{LR}	Load Return Voltage (CML output – Max[5])	--	--	5.5	Volts
V_{OLS}	Output Voltage Low (CML output – Min[6])	−1.8	--	--	Volts
V_{IH}	Input HIGH Voltage	−1165		−850	mV
V_{IL}	Input LOW Voltage	−2020		−1475	mV

1. Standard (HE and HB macro) 50 ohm outputs terminated with a 50 ohm resistor to −2.0 volts or low power (LE macro) outputs terminated with a 68 ohm resistor to −2.0 volts.
2. Low power outputs with a 60 ohm external load to −2.0 volts.
3. Cutoff outputs are not compensated for temperature.
4. With CML output connected to V_{CCE}.
5. The 5.5 V dc value is a maximum rating, do not exceed.
6. Limitations of load resistor and load return voltage combinations.

100K COMPATIBLE OPTIONS – STECL OUTPUTS (6mA AND 10mA CURRENT SOURCE)

Symbol	Characteristic	Specification Limits T_J = 25 to 115 °C Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	−1025	−945	−850	mV
V_{OL}	Output LOW Voltage	−1900	−1785	−1620	mV
V_{IH}	Input HIGH Voltage	−1165		−850	mV
V_{IL}	Input LOW Voltage	−2020		−1475	mV

1. STECL output levels are specified with no external load.
2. This table specifies levels for all STECL outputs.

DC CURRENT LIMITS – 100K COMPATIBLE OPTIONS

Symbol	Input Forcing Voltages	Specification Limits T_J = 25 to 115 °C	Unit
I_{INH} Max	V_{IH} Max	$I_{pulldown} + (N_L)(I_{input})$	mA
$I_{pulldown}$	where:	0.067 for standard input (75K pulldown)	mA
$I_{pulldown}$		12.5 for 10 mA current source input	mA
$I_{pulldown}$		7.5 for 6 mA current source input	mA
N_L		Number of DC unit loads connected to input	UL's
I_{input}		0.005	mA
I_{INL} Min	V_{IL} Min	0.5	µA
I_{EEE}	--	CAD LIMIT	--

DC CURRENT AND RESISTOR LIMITS – STECL OUTPUTS AND INPUT CS

Symbol	Characteristic	Specification Limits T_J = 25 °C to T_J = 115 °C			Unit
		MIN	TYP	MAX	
Iout 10	STECL and Input CS	8.0	10	12.5	mA
Iout 6	STECL and Input CS	4.5	6	7.5	mA
Rout 27	STECL Series Resistor	20	27	42	ohms
Rout 40	STECL Series Resistor	30	40	56	ohms

1. Iout 10 and Iout 6 refer to a 10 mA or 6 mA, respectively, internal current source for a STECL output or an input current source.
2. Rout 27 and Rout 40 refer to a 27 ohm or 40 ohm, respectively, internal series resistor at the output of a STECL driver.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE – TTL

Symbol	Characteristic	Specification Limits T_J = 25 to 115 °C Min	Typ	Max	Unit	Test Conditions	
V_{OH}	Output HIGH Voltage	2.7	3.4	--	V	I_{OH}= -3.0mA	V_{CCT}=Min
V_{OL}	Output LOW Voltage	--	0.35	0.50	V	I_{OL}=12/24mA	V_{CCT}=Min
V_{IH}	Input HIGH Voltage	2.0	--	--	V	threshold over V_{CCT} and temp. range	
V_{IL}	Input LOW Voltage	--	--	0.80	V	threshold over V_{CCT} and temp. range	
V_{IK}	Input Clamp Diode Voltage			-1.2	V	V_{CCT}=Min, I_{IN}= -18 mA	
I_{IH}[1]	Input HIGH Current	--	--	20	µA	V_{CCT}=Max, V_{in}=2.7 V	
I_{IL}[1]	Input LOW Current	--	--	-400	µA	V_{CCT}=Max, V_{in}=0.5 V	
I_{OZH}	Ouput Off Current HIGH	--	--	50	µA	V_{CCT}=Max, V_{in}=2.7 V	
I_{OZL}	Output Off Current LOW	--	--	-50	µA	V_{CCT}=Max, V_{in}=0.5 V	
I_{OS}[2]	Output Short Circuit Current	-25	--	-150	mA	12 mA Driver	V_{CCT}=Max, V_{out}=0

1. Current per input.
2. Output should not be shorted for more than one second and no more than one output should be shorted at a time.

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10.2.2 PECL Characteristics

The power supply voltage limits for the following tables are:

V_{EEE} = 0 volts
V_{CCT} = 4.75 to 5.25 volts
V_{CCE} = V_{CCO} = 4.75 to 5.25 volts
V_{EET} = 0 volts

PECL OUTPUTS

Symbol	Characteristic	Specification Limits T_J = 25 to 115 °C Min	Typ	Max	Unit
V_{OH}[1]	Output HIGH Voltage	V_{CCE} – 1025	V_{CCE} – 955	V_{CCE} – 880	mV
V_{OH}[2]	Output HIGH Voltage (low power)	V_{CCE} – 1045	V_{CCE} – 975	V_{CCE} – 880	mV
V_{OH}[3]	Output HIGH Voltage (cutoff)	V_{CCE} – 1050	V_{CCE} – 910	V_{CCE} – 735	mV
I_{OH}[4]	Output HIGH Current (CML output)	--	0	1.0	mA
I_{OH}[4]	Output LOW Current (CML output)	15.5	13.0	10.5	mA
V_{LR}	Load Return Voltage (CML output – Max[5])	--	--	5.5	Volts
V_{OLS}	Output Voltage Low (CML output – Min[6])	–1.8	--	--	Volts
V_{OL}	Output LOW Voltage	V_{CCE} – 1810	V_{CCE} – 1705	V_{CCE} – 1620	mV
V_{OL}[3]	Output LOW Voltage (cutoff)	V_{CCE} – 2020	V_{CCE} – 1985	V_{CCE} – 1950	mV
V_{IH}	Input HIGH Voltage	V_{CCE} – 1165		V_{CCE} – 850	mV
V_{IL}	Input LOW Voltage	V_{CCE} – 2020		V_{CCE} – 1475	mV

1. Standard (HE and HB macro) 50 ohm outputs terminated with a 50 ohm resistor to [V_{CCE} –2.0] volts, or low power (LE macro) outputs terminated with a 68 ohm resistor to [V_{CCE} –2.0] volts.
2. Low power outputs with a 60 ohm external load to [V_{CCE} –2.0] volts.
3. Cutoff outputs are not compensated for temperature.
4. 50 ohm load termination to V_{CCE} for CML outputs.
4. With CML output connected to V_{CCE}.
5. The 5.5 V dc value is a maximum rating, do not exceed.
6. Limitations of load resistor and load return voltage combinations.

10.2.3 Operation Conditions and Limits

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristic	Value	Unit
V_{EEE}	Supply Voltages (V_{CCE} = V_{CCO} = 0) for –4.5 V Options	–4.5 ± 0.3	Vdc
V_{EEE}	Supply Voltages (V_{CCE} = V_{CCO} = 0) for –5.2 V Options	–5.2 ± 8%	Vdc
V_{CCE}	Supply Voltages (V_{EEE} = 0) for 5.0 V Options	5.0 ± 5%	Vdc
V_{CCT}	TTL Supply Voltages for all Options	5.0 ± 5%	Vdc
T_J	Operating Temperature (Functional)	10 to 130	°C
T_J	Junction Temperature (AC and DC Specs)	25 to 115	°C
t_r,t_f	Max Clock Input Rise/Fall Times (20 to 80%) ECL	5	ns
t_r,t_f	Max Clock Input Rise/Fall Times (10 to 90%) TTL	15	ns

LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

Symbol	Characteristic	Value	Unit
V_{EEE}	ECL Supply Voltage (V_{CCE}=V_{CCO}=0)	−7.0 to +0.5	Vdc
V_{in}	ECL Input Voltage (V_{CCE}=V_{CCO}=0)	+0.5 to V_{EEE}	Vdc
V_{in}	ECL Input Voltage on Bidirectional (Cutoff) (V_{CCE}=V_{CCO}=0)[1]	+0.5 to −2.0	Vdc
V_{CCE}	PECL Supply Voltage (V_{EEE}=0)	−0.5 to +7.0	Vdc
V_{in}	PECL Input Voltage (V_{EEE}=0)	V_{EEE} to +5.5	Vdc
V_{in}	PECL Input Voltage on Bidirectional (Cutoff) (V_{EEE}=0)[1]	+3.0 to +5.5	Vdc
V_{CCT}	TTL Supply Voltage (V_{EET}=0)	−0.5 to +7.0	Vdc
V_{in}	TTL Input Voltage (V_{EEE}=0)	−0.5 to +7.0	Vdc
V_{out}	TTL Output Voltage	−0.5 to +5.5	Vdc
V_{CO}	CML Output Voltage (V_{EEE}= −5.2 Vdc,V_{CCE}=V_{CCO}=0)	+7.0 to −2.3	Vdc
I_{out}	ECL/PECL Output Source Current Continuous (50/60 ohm)	30	mA
I_{out}	ECL/PECL Output Source Current Surge (50/60 ohm)[2]	100	mA
I_{out}	ECL/PECL Output Source Current Continuous (25 ohm)	60	mA
I_{out}	ECL/PECL Output Source Current Surge (25 ohm)[2]	200	mA
I_{out}	ECL/PECL Output Source Current Continuous (STECL, 10 mA)	5	mA
I_{out}	ECL/PECL Output Source Current Surge (STECL, 10 mA)	40	mA
I_{out}	ECL/PECL Output Source Current Continuous (STECL, 6 mA)	9	mA
I_{out}	ECL/PECL Output Source Current Surge (STECL, 6 mA)	44	mA
I_{IN}	TTL Input Current	−30 to +5.0	mA
I_{OL}	TTL Output Current	Twice Rated I_{OL}	mA
T_{stg}	Storage Temperature	−55 to +150	°C
T_J	Junction Temperature (no time limit)	165	°C
T_J	Junction Temperature (<240 hours)	250	°C

1. If a cutoff output is in the low (disabled) state and is being forced by an external driver, the forcing voltage must fall between V_{CCE} and −2.0 volts for ECL and V_{CCE} and +3.0V for PECL operation.

2. Surge current is defined as an output current between 30 mA and 100 mA for a 50/60 ohm output, 60 mA and 200 mA for a 25 ohm output, 5mA and 40 mA for a STECL (10mA), and 9 mA and 44 mA for a STECL (6mA). The surge current must last for less than 10µs and must have a duty cycle equal to or less than 1%.

10.3 Switching Circuit and Waveforms

Figure 10-1 illustrates a typical test circuit used for measuring switching characteristics. For ECL signals a 50 ohm termination to ground is provided for each scope channel input. All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. Figure 10-2 illustrates a typical test circuit used for measuring TTL output AC characteristics. Specific AC waveforms and associated terminology are described in Section 10.5.

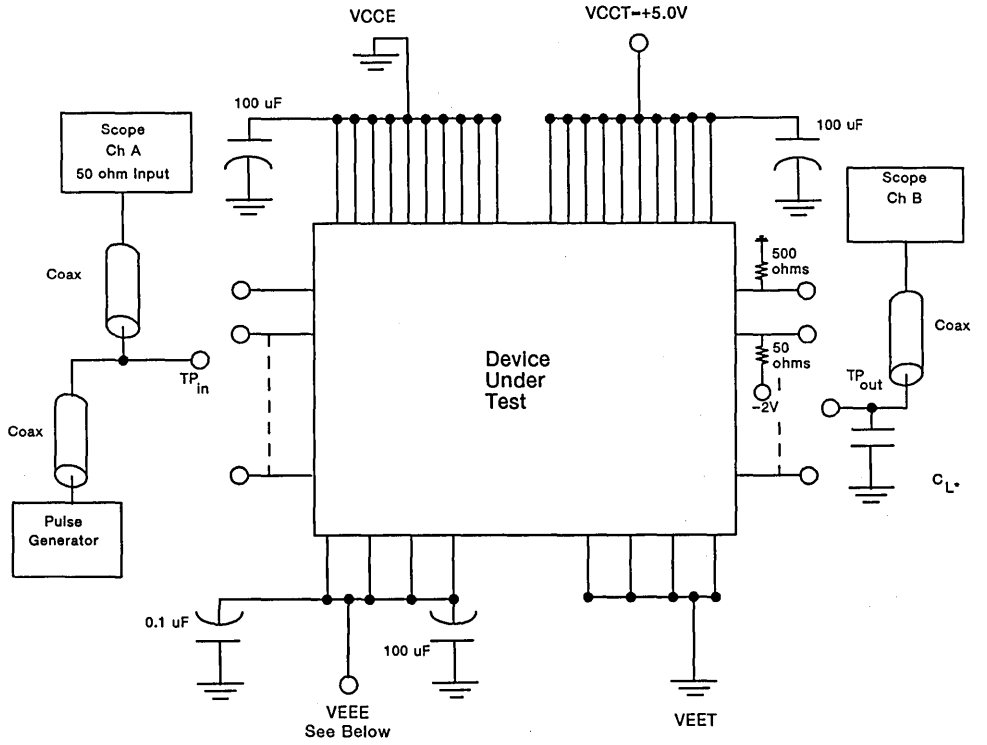

Figure 10-1 Switching Test Circuit

INPUT PULSE
$t_r = t_f = 0.5$ ns (20 to 80%) ECL
$t_r = t_f = 1.9$ ns (10 to 90%) TTL

VEEE = -5.2 or -4.5 V_{dc}

*$C_L \leq 5$pF stray capacitance (for connector and 1/4 inch of wire)

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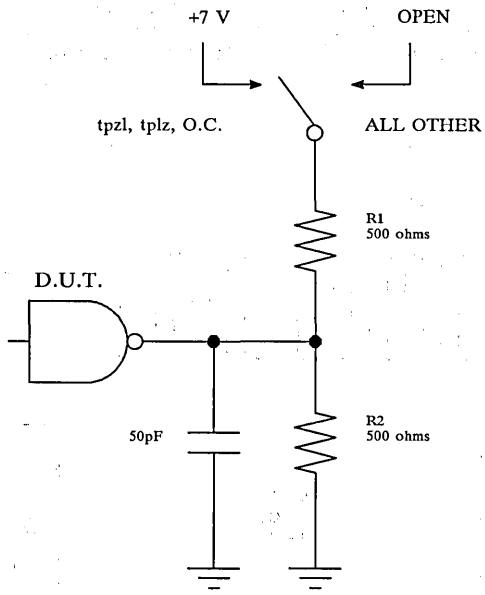

Figure 10–2 TTL Output AC Test Circuit

10.4 Examples for Bringing High Frequency Signals On Chip

The following three figures illustrate some methods for bringing high frequency signals on chip.

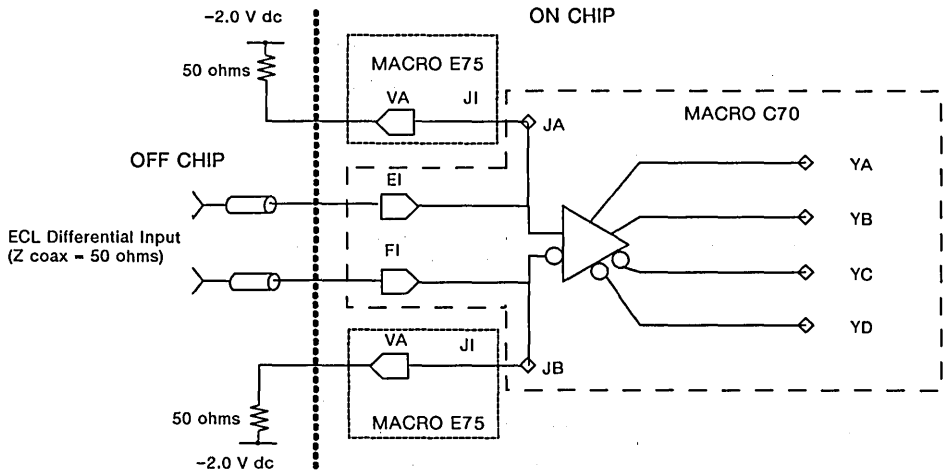

Figure 10–3 Schematic for 2.6 GHz Differential ECL Input with Off–Chip Termination

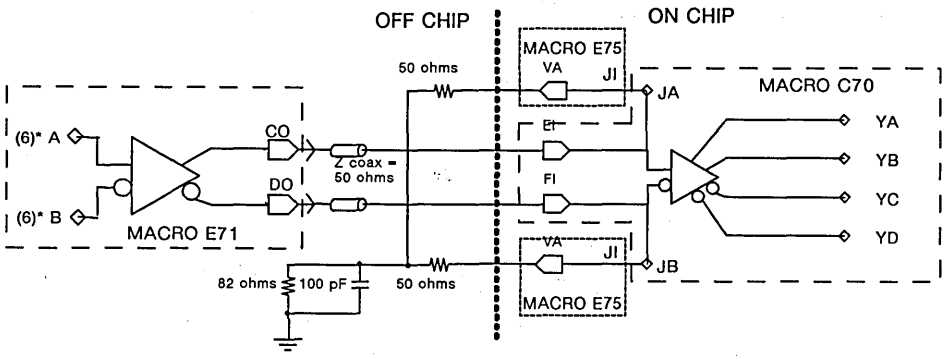

Figure 10–4 Differential 1.6 GHz (50% duty cycle) CML Output Macro E71 Interface to Input Buffer Macro C70

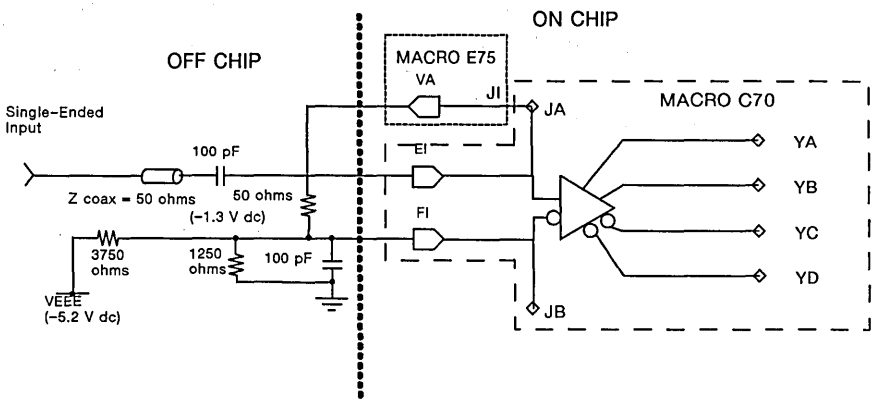

Figure 10–5 Schematic for 2.6 GHz Single–ended Input with Off–Chip Termination

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10.5 AC Switching Parameters and Waveforms

ECL Measurements

The propagation delays specified are measured from the 50% point of the input rising or falling edge to the V_{TH} point of the output rising or falling edge. V_{TH} is the V_{BB} threshold voltage which is equal to -1.3 volts (for V_{CCE}= 0 volts) or + 3.7 volts (for V_{CCE} = + 5.0 V) at 65 °C junction temperature.

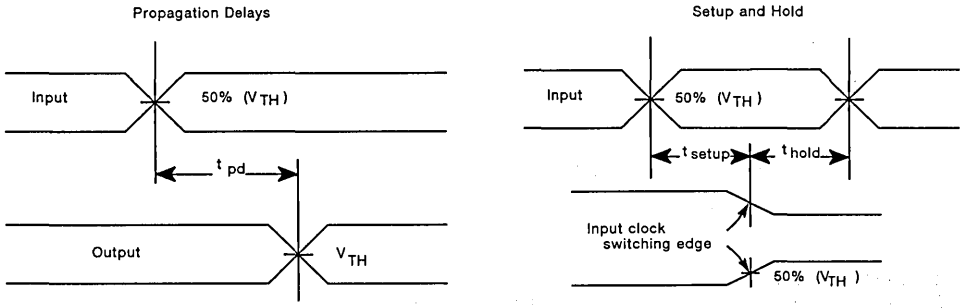


Figure 10–6 ECL Switching Waveforms

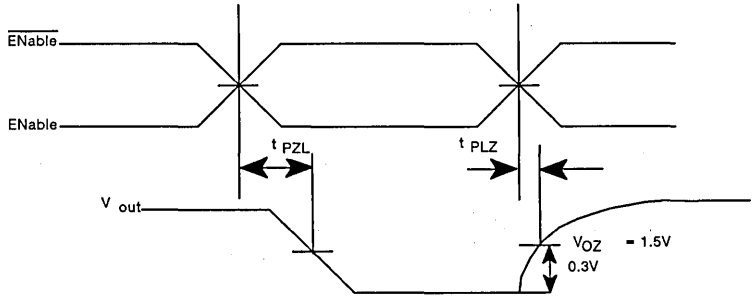
TTL Measurements

t_{PLZ} Output disable time: LOW to Z

The time delay between the specified amplitude point on the enable input and when the output falls 0.3V from the steady-state LOW level.

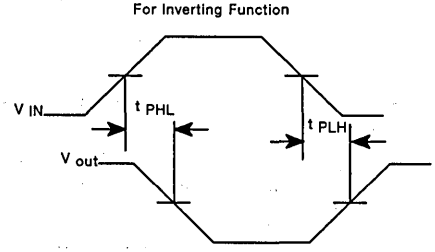
t_{PZL} Output enable time: Z to LOW

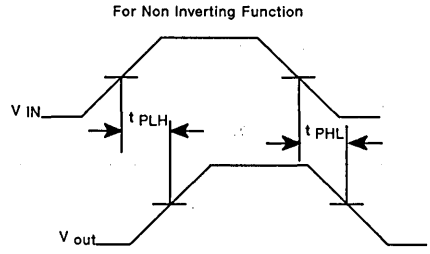
The time delay between the specified amplitude points on the enable input and the output, when the output is going from a disabled state to a logic LOW state.



t_{PLH} Propagation delay LOW-TO-HIGH
The time delay when the input is 1.5V to when the output reaches 1.5V while the output changes to a logic HIGH.

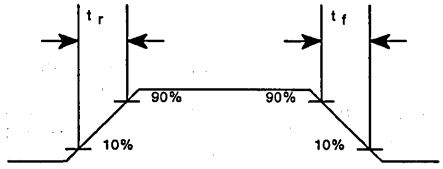
t_{PHL} Propagation delay HIGH-TO-LOW
The time delay when the input is 1.5V to when the output reaches 1.5V while the output changes to a logic LOW.





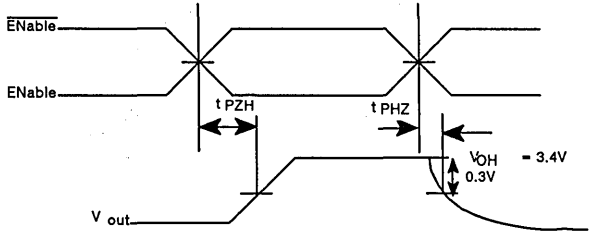
t_r Waveform Rise Time
LOW to HIGH logic transition time, measured from the 10% to 90% points of the waveform.

t_f Waveform Fall Time
HIGH to LOW logic transition time, measured from the 90% to 10% points of the waveform.



t_{PHZ} Output disable time: LOW to Z
The time delay between the specified amplitude point on the enable input and when the output falls 0.3V from the steady-state HIGH level.

t_{PZH} Output enable time: Z to LOW
The time delay between the specified amplitude points on the enable input and the output, when the output is going from a disabled state to a logic HIGH state.



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10.6 Product Reliability

The highest possible level of quality in concrete, measurable terms is Motorola's goal for its products and services. Each process and product is extensively characterized and qualified. Reliability assurance engineers work closely with macrocell array designers and computer aided design software engineers to identify and eliminate problem causes. Statistical process control techniques are used in each step of manufacturing to assure first pass design success for all customers.

In addition to initial qualification the Reliability Engineering Department performs ongoing reliability testing to maintain a high level of confidence in fabrication and assembly operations. Failure rates as a function of junction temperature are plotted for the MCA3 ETL arrays in Figure 10–7. At a junction temperature of 115°C the failure rate is estimated to be: 250 FIT for the 6200ETL; 145 FIT for the 3200ETL; and 50 FIT for the 750ETL array. An activation energy of 0.70 EV was used to calculate acceleration factors for other temperatures.

1 FIT = One device failure per 10^9 device hours or
One part per million failure rate per 10^3 hours

The reliability estimate is based on modeling of various failure mechanisms where the MCA3 ETL arrays features have been compared to other MCA3 arrays as well as previous generation arrays. Comparison of actual reliability data to previous estimates derived in an identical manner have closely predicted actual results.

As a result of exceedingly high quality and reliability standards, Motorola has achieved one of the lowest part reject records in the industry.

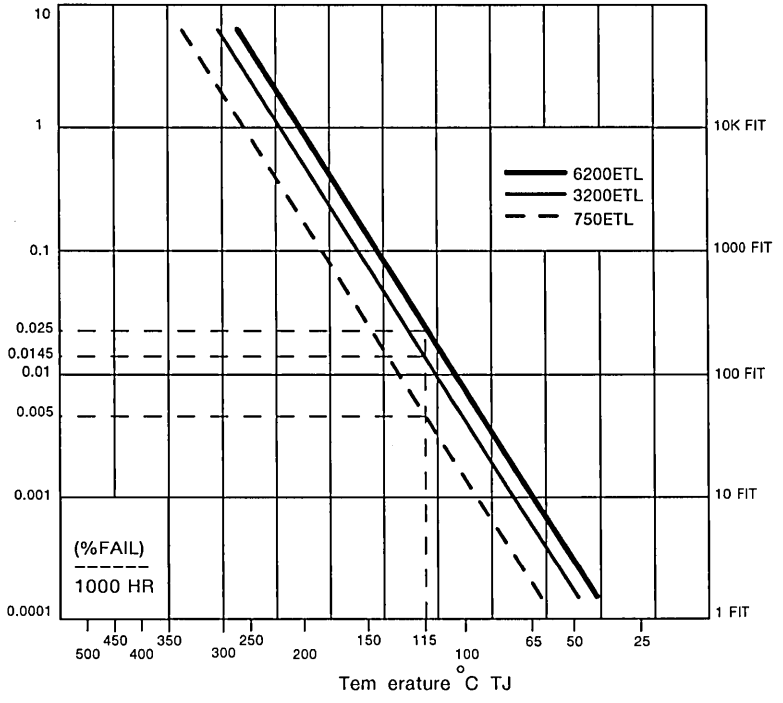

Figure 10–7 Failure Rate vs Reciprocal Temperature for MCA3 ETL Arrays
Estimated static operation average failure-rate as a function of junction temperature (Slope of line based on Arrhenius equation with 0.70 EV activation energy)

10.7 Electrostatic Discharge (ESD)

All inputs to the array, including bidirectional pins, have an ESD protection circuit in order to provide some protection to the narrow base junction of the transistor. The failure mode due to ESD is a damaged base junction which causes increased leakage current, or even worse, an open or shorted pin. Although the ESD protection network provides a great deal of protection against static voltage when handling the device, the inputs to the array are not immune to damage. For example, a static voltage of approximately 5000 volts has been measured when a person is walking on a waxed floor.

The standard input protection network consist of two reversed biased diodes connected between the input pin, and V_{CCE} and V_{EEE}. For TTL, reversed biased diodes are connected between the input pin and V_{CCT} and V_{EET}. The diodes use the large output transistors that are used for driving the output pins. These input pins have at least 1000 volts of protection as defined by MIL STD 883C, Method 3015.6.

ESD testing was performed on several options using the Human Body Model (HBM) according to MIL STD 883C, Method 3015.6 using an IMCS Model 5000 Automated ESD Test System. The failure criteria was defined as a + or – 10% variation in input leakage. Each pin was given 5 zaps of both + and – polarity with respect to the selected power rail (V_{EEE}, V_{EET}, or V_{CCE}, V_{CCO}, V_{CCT}). For standard inputs, the protection measured between 2200 and 3500 volts.

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