MOTOROLA

BR1339/D
REV 2

LCX DATA
Low-Voltage CMOS Logic

DATA SHEET CLASSIFICATIONS

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This heading on a data sheet indicates that the device is in the formative stages or in design (under development). The disclaimer at the bottom of the first page reads: "This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice."

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LCX Data

Low–Voltage CMOS Logic

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Functional Selection Guide

Motorola currently supplies three major product lines that interface with 3V buses. Besides the LCX family that is highlighted in this data book, the LVQ and High–Speed CMOS (HC) families are guaranteed to be functional as low as 2V V_{CC}. A broad selection of LVQ and HC products are also included in this selection guide to assist you in finding a wide selection of products that fit your design needs.

The LCX family provides industry leading CMOS technology. LCX products are specially designed for 3V applications and have special features enabling LCX to interface directly with 5V buses. This emerging logic family is available now with alternate sources already in place.

The LVQ product line also has DC and AC specifications for V_{CC} = 3V. LVQ can be a less expensive solution when 5V tolerance is not required.

The High–Speed CMOS HC product line is specified at 2V, 4.5V and 6V supplies. There are a few HC products that have been specified at 3V (contact your Motorola sales representative for information). Generally for designs not requiring fast propagation delays, users may estimate the 3V propagation delays using the 2V and 4.5V numbers. Please see Motorola's High–Speed CMOS data book (DL129/D) for more information.

Motorola welcomes customer input for LCX family portfolio expansion.

Abbreviations

S = Synchronous
A = Asynchronous
B = Both Synchronous and Asynchronous
2S = 2-State Output
3S = 3-State Output
N = Available Now
P = Planned (See Logic New Product Calendar, BR1332/D, for the latest availability and new product status)
– = No Current Plans or Not Applicable

Inverters

Description	Type of Output	No.	LCX	LVQ	HC
Hex	2S	04	N	N	N
Hex, w/Open Drain Outputs	2S	05	–	–	–

AND Gates

Description	Type of Output	No.	LCX	LVQ	HC
Quad 2-Input	2S	08	P	P	N
Triple 3-Input	2S	11	–	–	N

NAND Gates

Description	Type of Output	No.	LCX	LVQ	HC
Dual 4-Input	2S	20	–	–	N
Quad 2-Input	2S	00	P	N	N
Triple 3-Input	2S	10	–	–	N

OR Gates

Description	Type of Output	No.	LCX	LVQ	HC
Quad 2-Input	2S	32	P	P	N

NOR Gates

Description	Type of Output	No.	LCX	LVQ	HC
Quad 2-Input	2S	02	P	P	N

Exclusive OR/NOR Gates

Description	Type of Output	No.	LCX	LVQ	HC
Quad 2-Input XOR	2S	86	P	P	N
Quad 2-Input XNOR	2S	7266	–	–	N

Schmitt Triggers

Description	Type of Output	No.	LCX	LVQ	HC
Hex, Inverting	2S	14	–	–	N
Quad 2-Input, NAND	2S	132	–	–	N

Flip-Flops

Description	Clock Edge	No.	LCX	LVQ	HC
Dual D w/Set & Clear	Pos	74	P	P	N
Dual J$\overline{K}$	Pos	109	–	–	N

Multiplexers

Description	Type of Output	No.	LCX	LVQ	HC
8-to-1	2S	151	–	–	N
	3S	251	–	–	N
Dual 4-to-1, Non-Inverting	2S	153	–	–	N
	3S	253	–	–	N
Quad 2-to-1, Inverting	2S	158	–	–	N
Quad 2-to-1, Non-Inverting	2S	157	P	P	N
	3S	257	P	P	N

Functional Selection Guide

Shift Registers

Description	No. of Bits	Type of Output	Mode* SR	SL	Hold	Reset	No.	LCX	LVQ	HC
Parallel In-Parallel Out, Bidirectional	4	2S	X	X	X	A	194	–	–	N
	8	3S	X	X	X	A	299	–	–	N
8–Bit Serial In–Parallel/Serial Out With 3–State	8	3S	–	X	X	A	595	–	–	N

*SR = Shift Right
SL = Shift Left

Buffers/Line Drivers

Description	Type of Output	No.	LCX	LVQ	HC
Quad	3S	125	P	P	N
	3S	126	–	–	N
Octal, Non-Inverting	3S	241	–	–	N
	3S	244	N	N	N
Flow Through Pinout	3S	541	N	P	N
16–Bit, Non–Inverting	3S	16244	P	–	–
Octal, Inverting	3S	240	N	N	N
Flow Through Pinout	3S	540	N	P	N
16–Bit, Inverting	3S	16240	P	–	–

Transceivers

Description	Type of Output	No.	LCX	LVQ	HC
Octal, Non-Inverting	3S	245	N	N	N
	3S	640	–	–	N
16–Bit, Non–Inverting	3S	16245	P	–	–
Octal, Non-Invert w/Reg	3S	646	P	P	N
	3S	652	P	P	–
16–Bit, Non-Invert w/Reg	3S	16646	P	–	–
	3S	16652	P	–	–
Octal, Reg'd Transceiver w/ Clock Enable	3S	2952	P	–	–
18–Bit, Univ Bus Trnscvr	3S	16500	P	–	–

Cascadable Synchronous Counters — Positive Edge-Triggered

Description	Type of Output	Load	Reset	No.	LCX	LVQ	HC
Decade	2S	S	A	160	–	–	N
	2S	S	S	162	–	–	N
4-Bit Binary	2S	S	A	161	–	–	N
	2S	S	S	163	–	–	N

Decoders/Demultiplexers

Description	Type of Output	No.	LCX	LVQ	HC
Dual 1-of-4	2S	139	–	–	N
1-of-8	2S	138	P	P	N

Latches

Description	Type of Output	No.	LCX	LVQ	HC
Addressable	2S	259	–	–	N
Transparent, Inverting	3S	533	–	–	N
	3S	563	–	–	N
Octal, Non-Inverting	3S	573	N	P	N
Transparent	3S	373	N	P	N
16–Bit, Non–Inverting	3S	16373	P	–	–
Octal, Bidirectional	3S	543	P	P	–
16–Bit, Bidirectional	3S	16543	P	–	–

Flip-Flops/Registers

Description	No. of Bits	Type of Output	Set or Reset	No.	LCX	LVQ	HC
D-Type, Non-Inverting	6	2S	A	174	–	–	N
	8	2S	A	273	–	–	N
	8	3S	–	374	N	P	N
Flow Through Pinout	8	3S	–	574	N	P	N
16–Bit, D-Type, Non-Inverting	16	3S	–	16374	P	–	–
D-Type, Inverting	8	3S	–	564	–	–	N

Introducing LCX

Motorola's Low-Voltage CMOS Logic Family

Motorola's 3V LCX family features 5V–tolerant inputs and outputs that enable easy transition from 5V to mixed 3V/5V systems or to 3V systems. Low power, low switching noise and fast switching speeds make this family perfect for low power portable applications as well as high–end, advanced workstation applications.

The unique feature of this family is its ability to interface to pure 3V or both 3V and 5V buses in the same design without sacrificing performance. The LCX family improves system performance by drastically reducing static and dynamic power consumption which extends battery life for portable and handheld applications. Customers also realize simplified system design in mixed voltage environments, as well as expedited development of their low voltage systems. The 3V/5V interface using LCX, requires no other special components that would be necessary to protect other low voltage logic families that cannot tolerate signals beyond the V_{CC} supply level.

The Motorola LCX family is available in industry standard JEDEC SOIC, EIAJ SOIC, SSOP type 2, and TSSOP packages. LCX family specifications range from –40°C to +85°C. The LCX family was developed in accordance with an alliance including Motorola and two other major semiconductor suppliers, so there are alternate sources available now.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion/Withdrawal (3–State Devices)
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V (3–State Devices)
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

LCX Family Specifications

To assist the designer in evaluating the performance of Motorola's LCX family, data specifications and actual performance information are included here.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$ [1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1 I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage — (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	2.7V ≤ V_{CC} ≤ 3.6V	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	2.7V ≤ V_{CC} ≤ 3.6V		0.8	V
V_{OH}	HIGH Level Output Voltage	2.7V ≤ V_{CC} ≤ 3.6V; I_{OH} = –100µA	V_{CC} – 0.2		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	2.7V ≤ V_{CC} ≤ 3.6V; I_{OL} = 100µA		0.2	V
		V_{CC} = 2.7V; I_{OL}= 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	
I_I	Input Leakage Current	2.7V ≤ V_{CC} ≤ 3.6V; 0V ≤ V_I ≤ 5.5V		±5.0	µA
I_{OZ}	3–State Output Current	2.7 ≤ V_{CC} ≤ 3.6V; 0V ≤ V_O ≤ 5.5V; V_I = V_{IH} or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current (Note 2)	V_{CC} = 0V; V_I or V_O = 5.5V		10	µA
I_{CC}	Quiescent Supply Current	2.7 ≤ V_{CC} ≤ 3.6V; V_I = GND or V_{CC}		10	µA
		2.7 ≤ V_{CC} ≤ 3.6V; 3.6 ≤ V_I or V_O ≤ 5.5V		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	2.7 ≤ V_{CC} ≤ 3.6V; V_{IH} = V_{CC} – 0.6V		500	µA

NOTE 1: These values of V_I are used to test DC electrical characteristics only. Functional test should use V_{IH} ≥ 2.4V, V_{IL} ≤ 0.5V.
NOTE 2: I_{OFF} is applicable only to devices with 3–state outputs.

DYNAMIC SWITCHING CHARACTERISTICS

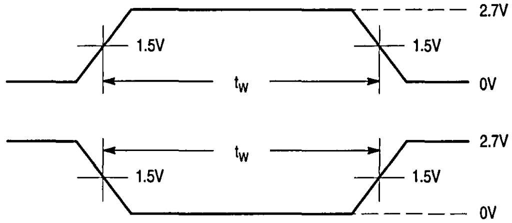
Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V

1 Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

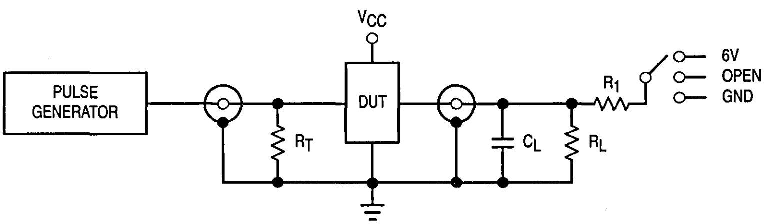
Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	NOTE 1	pF
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
$C_{I/O}$	Input/Output Capacitance[2]	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF

1 Function dependent, see individual datasheets.
2 Bidirectional devices only.



PULSE WIDTH
$t_R = t_F$ = 2.5ns (or fast as required) from 10% to 90%;
Output requirements: $V_{OL} \leq 0.8V$, $V_{OH} \geq 2.0V$

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

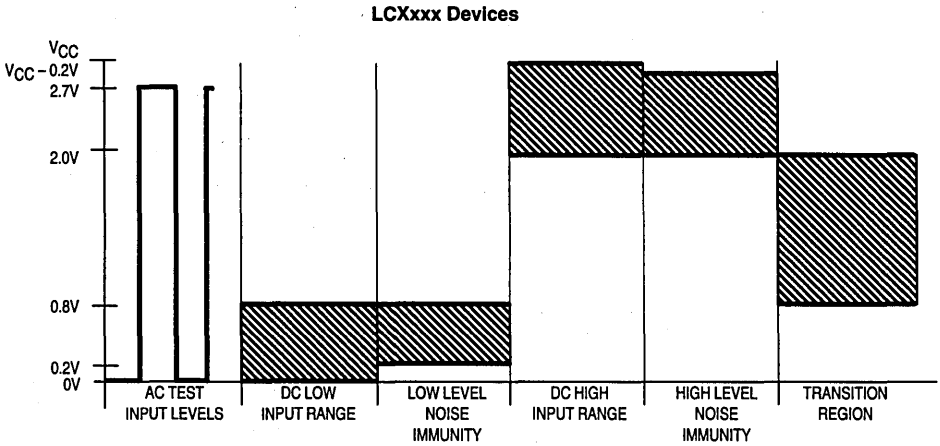


Figure 3. Test Input Signal Levels

Test Conditions

Figure 3 describes the input signal voltage levels to be used when testing LCX circuits. The AC test conditions follow industry convention requiring V_{IN} to range from 0 V for a logic LOW to 2.7V for a logic HIGH. The DC parameters are normally tested with V_I at guaranteed input levels, that is V_{IH} to V_{IL} (see datasheets for details). Care must be taken to adequately decouple these high performance parts and to protect the test signals from electrical noise. In an electrically noisy environment, (e.g., a tester and handler not specifically designed for high speed work), DC input levels may need adjustment to increase the noise margin allowance for the tester. This noise will not likely be seen in a system environment.

Noise immunity testing is performed by raising V_I to the nominal supply voltage of 3.3V then dropping to a level corresponding to V_{IH} characteristics, and then raising it again to the 3.3V level. Noise tests are performed on the V_{IL} characteristics by raising V_I from 0 V to V_{IL}, then returning to 0 V. Both V_{IH} and V_{IL} noise immunity tests should not induce a switch condition on the appropriate outputs of the LCX device.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output wave form transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths.

Rise and Fall Times

Input signals should have rise and fall times of 2.5ns and signal swing of 0V to 2.7V. Rise and fall times less than or equal to 1ns should be used for testing f_{max} or pulse widths.

CMOS devices tend to oscillate when the input rise and fall times become lengthy. As a direct result of its increased performance, LCX devices can be more sensitive to slow input rise and fall times than other lower performance technologies. Recommended edge rate is ≤10ns/V.

It is important to understand why this oscillation occurs. Consider the outputs, where the problem is initiated. Usually, CMOS outputs drive capacitive loads with low DC leakage. When the output changes from a HIGH level to a LOW level, or from a LOW level to a HIGH level, this capacitance is charged or discharged. With the present high performance technologies, charging or discharging takes place in a very short time, typically 2–3ns. The requirement to charge or discharge the capacitive loads quickly creates a condition where the instantaneous current change through the output structure is quite high. A voltage is generated across the V_{CC} or ground leads inside the package due to the lead inductance. The internal ground of the chip will change in reference to the outside world because of this induced voltage.

Next, consider the inputs. If the internal ground changes, the input voltage level appears to change to the DUT. If the input rise time is slow enough, its level might still be in the threshold region, or very close to it, when the output switches. If the internally-induced voltage is large enough, it is possible to shift the threshold enough so that it re-crosses the input level. If the gain of the device is sufficient and the input rise or fall time is slow enough, then the device may go into oscillation. As device propagation delays become shorter, the inputs will have less time to rise or fall through the threshold region. As device gains increase, the outputs will swing more, creating more induced voltage. Instantaneous current change will be greater as outputs become quicker, generating more induced voltage.

Package-related causes of output oscillation are not entirely to blame for problems with input rise and fall time measurements. All testers have V_{CC} and ground leads with some finite inductance. This inductance must be added to the inductance of the package to determine the overall voltage which will be induced when the outputs change. As the reference for the input signals moves further away from the pin under test, the test will be more susceptible to problems caused by the inductance of the leads and stray noise. Any noise on the input signal will also cause problems.

Enable and Disable Times

Figure 7 and Figure 8 show that the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from the voltage rail level (i.e., ground for t_{PLZ} or V_{CC} for t_{PHZ}). This change enhances the repeatability of measurements, reduces test times, and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the high–impedance state rising or falling waveform is RC-controlled, the first 0.3V of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 0.3V is adequate to ensure that a device output has turned OFF. Measuring to a larger change in voltage merely exaggerates the apparent Disable time artificially penalizing system performance (since the designer must use the Enable and Disable times to figure worst case timing.)

Propagation Delay, f_{max}, Set, Hold, and Recovery Times

A 1 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{max}. A 50% duty cycle should always be used when testing f_{max}. Two pulse generators are usually required for testing such parameters as setup time (t_s), hold time (t_h), recovery time (t_{REC}) shown in Figure 6.

Electrostatic Discharge

Precautions should be taken to prevent damage to devices by electrostatic discharge. Static charge tends to accumulate on insulated surfaces such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to LCX devices, it is recommended that individuals wear a grounded wrist strap when handling devices. More often, handling equipment, which is not properly grounded, causes damage to parts. Ensure that all plastic parts of the tester, which are near the device, are conductive and connected to ground.

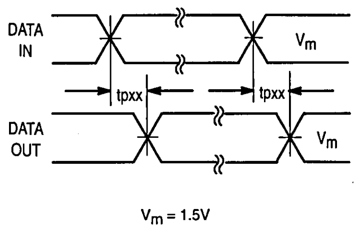


Figure 4. Waveform for Inverting and Non-Inverting Functions

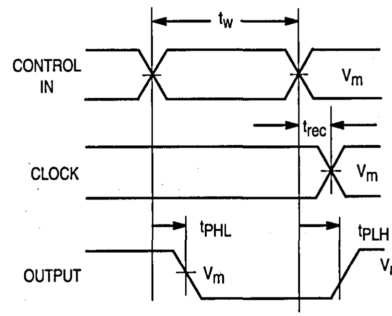


Figure 5. Propagational Delay, Pulse Width and t_{rec} Waveforms

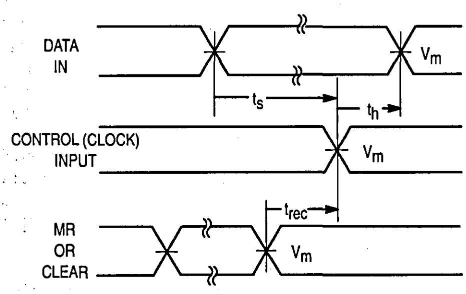


Figure 6. Setup Time, Hold Time and Recovery Time

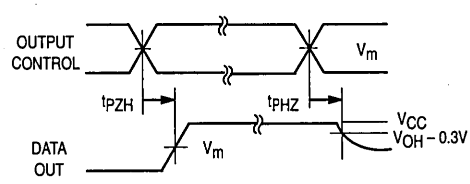
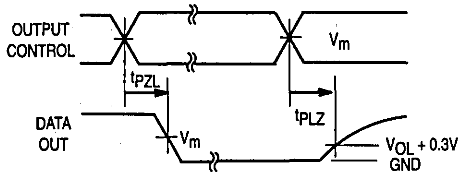


Figure 7. 3–State Output High Enable and Disable Times



$V_m = 1.5V$

Figure 8. 3–State Output Low Enable and Disable Times

Definitions of Symbols

DC Characteristics

Currents	Positive current is defined as conventional current flow into a device. Negative current is defined as current flow out of a device.
Voltages	All voltages are referenced to the ground pin.
I_{CC}	The current flowing into the V_{CC} supply terminal when the device is at a quiescent state.
I_{CCH}	The current flowing into the V_{CC} supply terminal when the outputs are in the HIGH state.
I_{CCL}	The current flowing into the V_{CC} supply terminal when the outputs are in the LOW state.
I_{CCZ}	The current flowing into the V_{CC} supply terminal when the outputs are disabled (high impedance).
ΔI_{CC}	Additional I_{CC} due to TTL HIGH levels forced on CMOS inputs.
I_I	Input Current. The current flowing into or out of an input when a specified LOW or HIGH voltage is applied to that input.
I_{OH}	Output HIGH Current. The current flowing out of an output which is in the HIGH state.
I_{OL}	Output LOW Current. The current flowing into an output which is in the LOW state.
I_{OS}	Output Short Circuit Current. The current flowing out of an output in the HIGH state when that output is shorted to ground (or other specified potential).
I_{OZ}	Output high impedance current. The current flowing into or out of a disabled output when specified LOW or HIGH voltage is applied to that output.
I_{OFF}	Input/Output power–off leakage current. The maximum leakage current into or out of the input/output transistors when forcing the input/output from 0V to 5.5V with V_{CC} = 0V.
V_{CC}	Supply Voltage. The range of power supply voltages over which the device is guaranteed to operate.
V_{IH}	Input HIGH Voltage. The minimum input voltage that is recognized as a DC HIGH level.
V_{IL}	Input LOW Voltage. The maximum input voltage that is recognized as a DC LOW level.
V_{OH}	Output HIGH Voltage. The voltage at an output conditioned HIGH with a specified output load and V_{CC} supply voltage.
V_{OL}	Output LOW Voltage. The voltage at an output conditioned LOW with a specified output load and V_{CC} supply voltage.
V_{OLP}	Maximum (peak) voltage induced on a static LOW output during switching of other outputs.
V_{OLV}	Minimum (valley) voltage induced on a static LOW output during switching of other outputs.

AC Characteristics

f_{max} **Toggle Frequency/Operating Frequency** – The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function properly.

t_{PLH} **Propagation Delay Time** – The time between the specified reference points, on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} **Propagation Delay Time** – The time between the specified reference points, on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_W **Pulse Width** – The time between specified amplitude points of the leading and trailing edges of a pulse.

t_h **Hold Time** – The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

t_s **Setup Time** – The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition.

t_{PHZ} **Output Disable Time (of a 3–state Output) from HIGH Level** – The time between specified levels on the input and a voltage 0.3V below the steady state output HIGH level with the 3–state output changing from the defined HIGH level to a high impedance (OFF) state.

t_{PLZ} **Output Disable Time (of a 3–state Output) from LOW Level** – The time between specified levels on the input and a voltage 0.3V above the steady state output LOW level with the 3–state output changing from the defined LOW level to a high impedance (OFF) state.

t_{PZH} **Output Enable Time (of a 3–state Output) to a HIGH Level** – The time between the specified levels of the input and output voltage waveforms with the 3–state output changing from a high impedance (OFF) state to a HIGH level.

t_{PZL} **Output Enable Time (of a 3–state Output) to a LOW Level** – The time between the specified levels of the input and output voltage waveforms with the 3–state output changing from a high impedance (OFF) state to a LOW level.

t_{rec} **Recovery Time** – The time between the specified level on the trailing edge of an asynchronous input control pulse and the same level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

LCX Family Characteristics

LCX and LVT Products

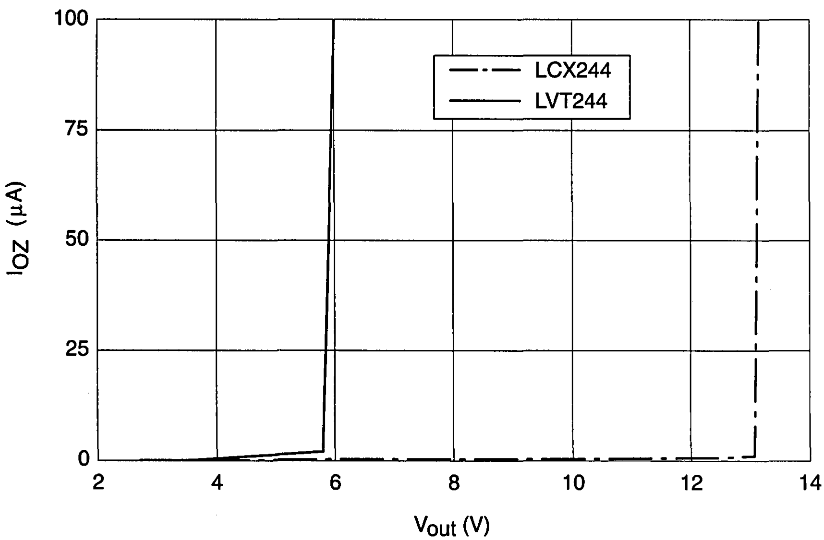
Product Family	74LCX	74LVT
Technology	**CMOS**	BiCMOS
I_{CCL} (mA)	**0.01**	12.0
I_{CC} vs Frequency (50MHz)	**130mA**	275mA
Speed ('244 Max)	**6.5ns**	4.1ns
Drive (2.0V/0.55V) JEDEC (2.4V/0.4V)	**>–24mA/24mA** **–18mA/16mA**	–32mA/64mA –8mA/16mA
5V Tolerant Inputs Outputs	**YES** **YES**	YES YES*
Power–Down High–Z	**YES**	YES
Data Retention	**YES**	NO

* LVT claims 5V–Tolerant outputs, but it is not specified.

The following graph compares the 5V–tolerance capability of LCX and LVT. When LCX is not driving the bus (outputs are disabled), the levels on that bus can exceed the LCX V_{CC} with no adverse effect on the device or any loading on the bus. In fact, test data shows that a disabled LCX output can "tolerate" signals over 13V on the outputs.

5V Output Tolerance

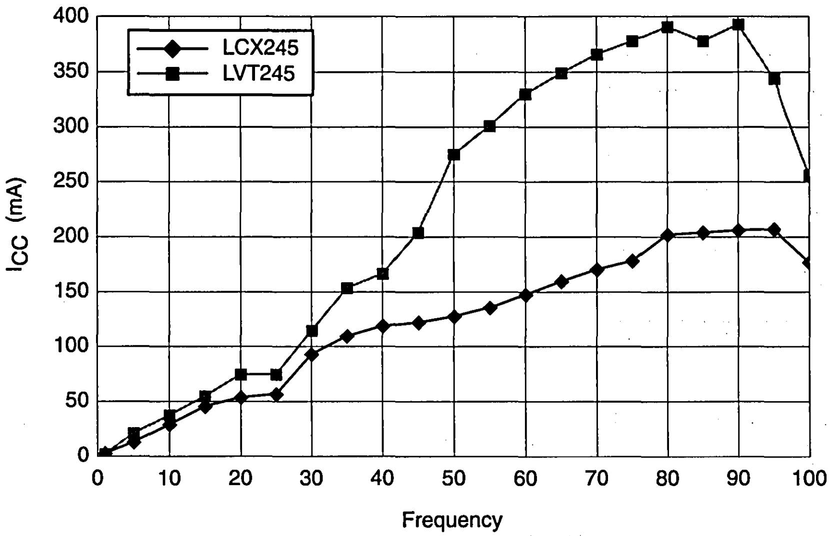
(I_{OZ} vs V_{out}, V_{CC} = 2.7V, +25°C)



Another advantage of the LCX family is the low dynamic current. Low dynamic current means low power consumption. Low power consumption means smaller power supplies, longer battery life and physically smaller systems. The following graph shows the Motorola 74LCX245's I_{CC} vs. Frequency performance with 8 outputs switching. To give an idea of power improvement that can be had with low voltage logic, a 74LCX245 consumes about the same power running at 35MHz that a 74F245 does statically. At 100MHz the LCX device only consumes about 200mA.

I_{CC} versus Frequency

(25°C, 3.3V)



LCX — Low–Voltage CMOS Logic (With 5V–Tolerant Inputs and Outputs)

The LCX family represents Motorola's Low–Voltage CMOS family. These devices offer mixed 3V–5V capability and are recommended for applications where 3.3V and 5V subsystems interface with one another and where low power consumption is a necessity. The input and output (Note 1) structures of the LCX family of products will tolerate input and output node exposure to signals or DC levels that exceed the V_{CC} level (Note 2). Refer to Figure 9 for schematic description of a typical LCX circuit. Note that the output PMOS device P1 has its bulk potential supplied by the output of the comparator X1 rather than by V_{CC} as in conventional CMOS. The circuitry contained within the comparator is designed such that the output is always the greater of V_{CC} or V_O. This technique circumvents the P+/N– bulk–source forward junction that usually appears between the PMOS drain at the output and the bulk connection of the output PMOS which is usually tied to V_{CC}. Eliminating this junction is fundamental to the powered–down high Z and overvoltage tolerance features that distinguish Motorola's LCX family from other Low–Voltage CMOS products.

NOTE 1: U.S. patent pending.
NOTE 2: Output overvoltage is permitted unconditionally for 3–stated outputs. For active outputs, see datasheet.

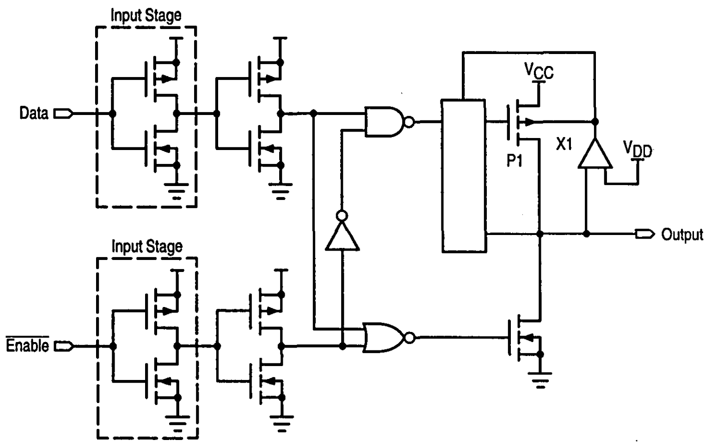


Figure 9. Simplified LCX Schematic Diagram

LCX Applications Information

Introduction

Many system designers concerned about reducing power in mobile computing, portable systems and communications may be unnecessarily avoiding the use of 3.3V products because of either cost or the *dreaded* 3V/5V interface. Cost may be a concern, but nearly every new 3.3V device has better performance - either increased speed or reduced power - when compared to a 5V "counterpart". In the long run it could easily cost the equipment maker more to continue with older technology rather than make the move to 3.3V or mixed 3.3V/5V systems.

There are three major reasons that chip manufacturers are accelerating the introduction of low voltage devices. First-DRAM manufacturers are worried about damage to products with fine geometries. As memory becomes more dense, feature geometries by necessity shrink. Voltages as high as 5V would damage these compactly designed RAMs. Second-as processor manufacturers have increased the performance of their chips, they have found that packages could not handle the increased power dissipation need. The enabling factor is the move to 3.3V supplies. Power dissipation varies by the ratio of the squares of the V_{CC}s, ($P_D \cong (V_{CC}^2)$(capacitance)(frequency)), so the ratio of reduction in power is $3.3^2/5^2$ (11/25) when moving from 5V to 3.3V. Third-Battery–powered system manufactures are continually working for extended battery life. Obviously a 56+% reduction in power would considerably extend battery life. There are other benefits as well. Smaller packaging can be used to house the low voltage chips-saving board space and making the end product smaller and lighter. Smaller or fewer power supplies are required, and costly, space– hogging heat dissipating equipment can be eliminated.

Most 3.3V logic families can directly interface only with other 3.3V products. LVC, LVX, VHC, LVQ, FCT3, and HC product families are lines that may work well for pure 3.3V system interface. Of these families only LVX guarantees 5V–tolerant inputs. The other families can tolerate maximum input and output levels of only V_{CC}+0.5V. If a 5V TTL bus voltage swings to levels that exceed these specifications then the non 5V–tolerant products may be damaged, destroyed, load the bus, or current may be sourced into its 3.3V supply. Not only is it important to be 5V–tolerant on the inputs but to be 5V–tolerant on the outputs as well.

The LCX family provides the necessary circuitry to bridge the technology gap between the 5V and 3.3V worlds. The inputs of this low voltage family can be safely driven to 5.5V, guaranteed, easily handling a 5V TTL or 5V CMOS interface on the input bus. When the LCX device outputs, or I/Os, have finished their tasks and are in the high–impedance state, the voltage levels on the bus to which they are tied may rise well above the 3.3V V_{CC}, up to 5.5V without loading the bus or causing damage to the device or power supply, guaranteed. This capability has been properly termed *5V tolerant*, rather than 3.3V/5V translation which is a misnomer. (Products that are powered by 3.3V supplies do not drive 5V rail–to–rail output swings. Dual 3.3V/5V supply devices are needed to drive 5V CMOS level outputs.)

There is no longer reason to fear mixed voltage designs. The LCX family is available now to help you bridge the 3.3V–5V interface.

Interfacing Dual Systems

To properly interface between integrated circuits, it is imperative that input and output specifications be reviewed and voltage and current levels satisfied. Output specifications (V_{OH} and V_{OL}) of the driving device must meet or exceed the input requirements (V_{IH} and V_{IL}) of the receiving device for the interface to function properly. Meeting these requirements protects against malfunction when operating in environments which may induce noise to the interface.

The 5V power supply has been the standard for many years in the IC world. Several product families have been introduced with varying speeds, drive capabilities, and power requirements. Because of this many I/O standards have evolved complicating the interface between 5V devices. The move to 3.3V power supplies actually simplifies the interface problem. Pure Bipolar products do not function well at 3.3V, so the core technology is either BiCMOS or pure CMOS. In a pure 3.3V MOS environment the interface can be made directly — inputs and outputs. However, it will be several years before all system components operate from 3.3V supplies. This is especially true for peripheral devices such as printers, displays, and faxes.

Interfacing 5V–TTL to Pure 3.3V Logic

(No 5V–Tolerance)

When the desired interface is 5V–TTL to pure 3.3V CMOS (such as LVQ), the solution may become a little messy. The designer must make sure that the 5V–TTL outputs do not exceed the 3.3V CMOS input specifications. There are a few options available to protect the 3.3V device from excessive input current. The 3.3V and 5V power supplies should be regulated together. It would also be a benefit to run the 5V supply on the low side reducing the V_{CC}–V_{OH} difference. If, however, the power supplies are not regulated together and the supplies end up at 5V+10% and 3.3V–10% then the 3.3V CMOS input specifications would likely be violated. To keep within the 3.3V CMOS input specification the 5V–TTL output cannot exceed 0.5V + V_{CC} of the CMOS device. The simplest way to ensure that V_{OH} remains within the input specification is to use a parallel termination resistor tied to ground. There are also CMOS switches that can be placed between the 5V and 3.3V devices to reduce the V_{OH}, but this solution can be very expensive.

Interfacing 5V–CMOS to Pure 3.3V Logic

(No 5V–Tolerance)

When the interface is a 5V CMOS device and a 3.3V CMOS device without 5V–tolerance, the problem is much like the 5V–TTL interface — but worse. The output of the 5V device must be reduced or large currents will flow into the

3.3V device. This type of interface is simply not recommended.

Interfacing Pure 3.3V Logic to 5V Inputs

(No 5V Output Tolerance)

Interfacing 3.3V CMOS to 5V–TTL inputs can be done directly. LVCMOS/LVTTL output specifications and 5V–TTL input specifications are compatible. Be aware of 5V buses that have pull–up resistors on the inputs. If pull–up resistors are used then pull–down resistors should be used to compensate and reduce a high voltage level to within the output specification range of the 3.3V device. Interfacing a 3.3V CMOS output to a 5V CMOS output should NEVER be done. The output swing of the 3.3V device is insufficient to drive the 5V CMOS device. If a pull–up resistor to 5V V_{CC} was used to raise the input level high enough to drive the 5V CMOS input then massive current would flow into the 3.3V device output.

Interfacing to 5V–Tolerant LCX Devices

Many of the problems and concerns associated with pure 3.3V interface can be resolved simply by using 5V–tolerant LCX devices. LCX tolerates 5V–TTL or 5V CMOS levels on its inputs. There is no inherent leakage path that would damage the device or in any way adversely affect these interfaces.

The 5V–tolerant output feature protects the 3.3V bus from high signal excursions on the 5V bus when the 3.3V bus is inactive (3–State). Only LCX devices with 3–State capability have 5V–tolerant outputs. Gates and MSI products without 3–State capability have 5V–tolerant inputs but not 5V–tolerant outputs. When an LCX device is enabled the 5V output tolerance is not active and will not protect the LCX device in cases of bus contention. Care must be taken to ensure that the LCX device is 3–Stated when there are 5V signals present on the bus.

5V signals can also be caused by the use of pull–ups on the 5V bus. Similarly certain 5V devices with internal pull–ups could cause leakage current into the LCX enabled outputs. Pay close attention to the 5V device data sheets to be sure that 5V pull–ups do not exist on the 5V bus. Do not interface an LCX output to a 5V CMOS input. The V_{OH} level of LCX devices is not high enough to reliably drive a 5V CMOS input.

Summary

LCX is recommended for interfacing 3V and 5V buses. LCX is CMOS based, so it is very stingy when it comes to power consumption — perfect for battery powered applications. Built on Motorola's .8 micron CMOS process, LCX has high drive and high speed making it perfect for many high end applications, and 5V–tolerant inputs and outputs makes LCX ideal for use in mixed voltage environments.

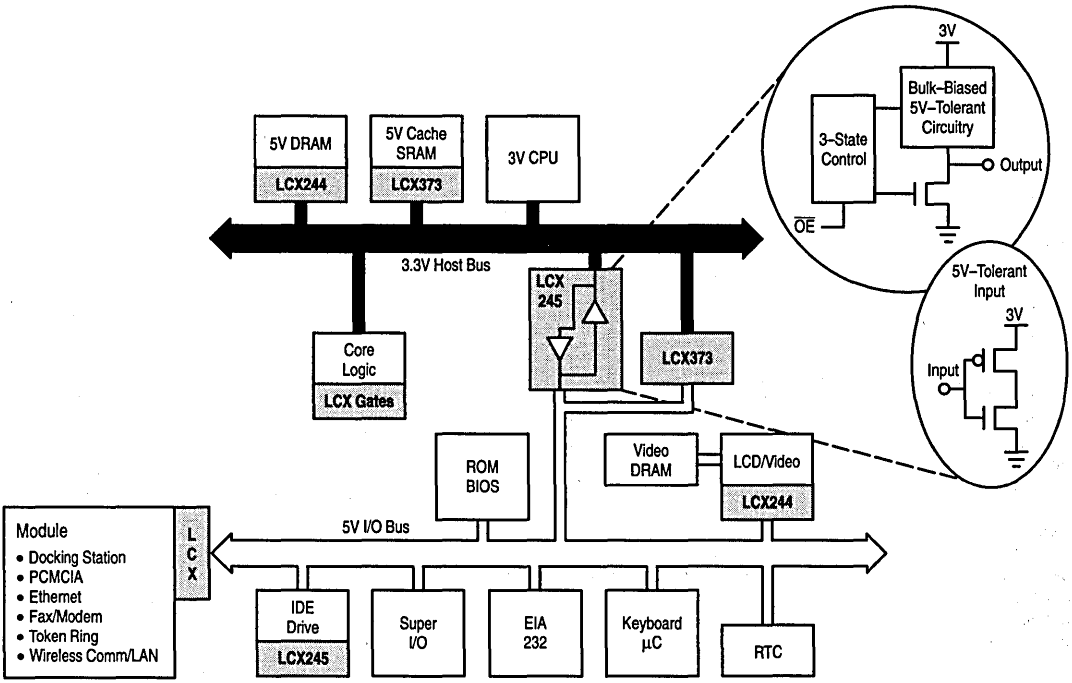


Figure 10. LCX System Block Diagram

Design Considerations

The LCX family was designed to alleviate many of the drawbacks that are common to current low–voltage logic circuits. LCX combines the low static power consumption and the high noise margins of CMOS with a high fan-out, low input loading and a 50Ω transmission line drive capability.

Performance features such as 5ns speeds at CMOS power levels, ±24mA drive, excellent noise, ESD and latch-up immunity are characteristics that designers of state-of-the-art systems require. LCX provides this level of performance. To fully utilize the advantages provided by LCX, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common design concerns relative to the performance and requirements of LCX.

There are six items of interest which need to be evaluated when implementing LCX devices in new designs:

- Thermal Management — circuit performance and long-term circuit reliability are affected by die temperature.
- Interfacing — interboard and technology interfaces, battery backup and power down or live insert/extract systems require some special thought.
- Transmission Line Driving — LCX has excellent line driving capabilities.
- Noise effects — As edge rates increase, the probability of crosstalk and ground bounce problems increases. The enhanced noise immunity and high threshold levels improve LCX's resistance to crosstalk problems.
- Board Layout — Prudent board layout will ensure that most noise effects are minimized.
- Power Supplies and Decoupling — Maximize ground and V_{CC} traces to keep V_{CC}/ground impedance as low as possible; full ground/V_{CC} planes are best. Decouple any device driving a transmission line; otherwise add one capacitor for every package

Thermal Management

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point. See the Thermal Management Considerations Section on page 187 for LCX power calculations.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit — from the junction region to the ambient environment. The basic formula for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\bar{\theta}_{JC} + \bar{\theta}_{CA}) \qquad (1)$$

or

$$T_J = T_A + P_D(\bar{\theta}_{JA}) \qquad (2)$$

where

T_J = maximum junction temperature
T_A = maximum ambient temperature
P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III).
$\bar{\theta}_{JC}$ = average thermal resistance, junction to case
$\bar{\theta}_{CA}$ = average thermal resistance, case to ambient
$\bar{\theta}_{JA}$ = average thermal resistance, junction to ambient

This Motorola recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL-M-38510 (JAN) devices.

Only two terms on the right side of equation (1) can be varied by the user — the ambient temperature, and the device case-to-ambient thermal resistance, $\bar{\theta}_{CA}$. (To some extent the device power dissipation can also be controlled, but under recommended use the V_{CC} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\bar{\theta}_{CA}$ thermal resistance term. $\bar{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature-controlled heat sink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D(\bar{\theta}_{JC}) \qquad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

Air Flow

The effect of air flow over the packages on $\bar{\theta}_{JA}$ (due to a decrease in $\bar{\theta}_{CA}$) reduces the temperature rise of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over the devices, or differences in ambient temperature between two devices.

The majority of users employ some form of air-flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations.

Optimizing The Long Term Reliability of Plastic Packages

Todays plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However when the ultimate in system reliability is required, thermal management must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperatures are consistent with system reliability goals.

Predicting Bond Failure Time

Based on the results of almost ten (10) years of +125°C operating life testing, a special arrhenius equation has been developed to show the relationship between junction temperature and reliability.

$$(1)\ T = (6.376 \times 10^{-9})e\left[\frac{11554.267}{273.15 + T_J}\right]$$

Where: T = Time in hours to 0.1% bond failure (1 failure per 1,000 bonds).

T_J = Device junction temperature, °C.

And:

$$(2)\ T_J = T_A + P_D\theta_{JA} = T_A + \Delta T_J$$

Where: T_J = Device junction temperature, °C.

T_A = Ambient temperature, °C.

P_D = Device power dissipation in watts.

θ_{JA} = Device thermal resistance, junction to air, °C/Watt.

ΔT_J = Increase in junction temperature due to on-chip power dissipation.

Table 1 shows the relationship between junction temperature, and continuous operating time to 0.1% bond failure, (1 failure per 1,000 bonds).

TABLE 1 — DEVICE JUNCTION TEMPERATURE versus TIME TO 0.1% BOND FAILURES.

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Table 1 is graphically illustrated in Figure 11 which shows that the reliability for plastic and ceramic devices is the same until elevated junction temperatures induce intermetallic failures in plastic devices. Early and mid-life failure rates of plastic devices are not effected by this intermetallic mechanism.

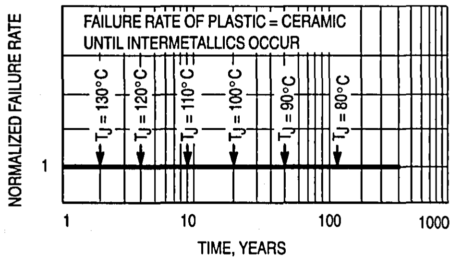


Figure 11. Failure Rate versus Time Junction Temperature

Procedure

After the desired system failure rate has been established for failure mechanisms other than intermetallics, each device in the system should be evaluated for maximum junction temperature. Knowing the maximum junction temperature, refer to Table 1 or Equation 1 to determine the continuous operating time required to 0.1% bond failures due to intermetallic formation. At this time, system reliability departs from the desired value as indicated in Figure 11.

Air flow is one method of thermal management which should be considered for system longevity. Other commonly used methods include heat sinks for higher powered devices, refrigerated air flow and lower density board stuffing. Since $\overline{\theta}_{CA}$ is entirely dependent on the application, it is the responsibility of the designer to determine its value. This can be achieved by various techniques including simulation, modeling, actual measurement, etc.

The material presented here emphasizes the need to consider thermal management as an integral part of system design and also the tools to determine if the management methods being considered are adequate to produce the desired system reliability.

Line Driving

With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects.

Although all circuit conductors have transmission line properties, these characteristics become significant when the edge rates of the drivers are equal to or less than three times the propagation delay of the line. Significant transmission line properties may be exhibited in an example where devices have edge rates of 3ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

Of the many properties of transmission lines, two are of major interest to the system designer: Z_{oe}, the effective equivalent impedance of the line, and t_{pde}, the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_o and t_{pd}, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z_{oe} and t_{pde} can be calculated with:

$$Z_{oe} = \frac{Z_o}{\sqrt{1 + C_t/C_l}}$$

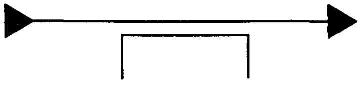
$$t_{pde} = t_{pd}\sqrt{1 + C_t/C_l}$$

where C_l = intrinsic line capacitance and C_t = additional capacitance due to gate loading.

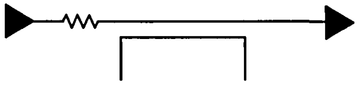
The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.

There are several termination schemes which may be used. Included are series, parallel, AC parallel and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.

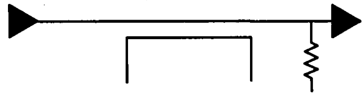
Termination Schemes



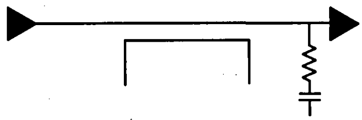
a: No Termination



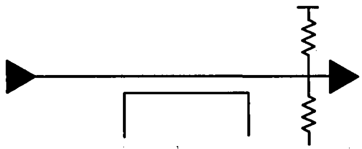
b: Series Termination



c: Parallel Termination



d: AC Parallel Termination



e: Thevenin Termination

Figure 12. Termination Schemes

Series Terminations

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line. Loads that are between the driver and the end of the line will receive a two-step waveform. The first wave will be the incident wave. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor and the impedance of the line according to the formula

$$V_W = V_{CC} \bullet Z_{oe}/(Z_{oe} + R_S + Z_S)$$

The amplitude will be one-half the voltage swing if R_S (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance. The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

Parallel Termination

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{CC} or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

AC Parallel Termination

AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable. The effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

Thevenin Termination

Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination will generally not be a function of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that lines with Thevenin terminations should not be left floating since this will cause the input levels to float between V_{CC} or ground, increasing power consumption.

LCX circuits have been designed to drive 50Ω transmission lines over the full temperature range.

LCX devices also feature balanced totem pole output structures to allow equal source and sink current capability. This provides balanced edge rates and equal rise and fall times. Balanced drive capability and transition times eliminates the need to calculate two different delay times for each signal path and the requirement to correct signal polarity for the shortest delay time.

Noise Effects

LCX offers excellent noise immunity. However, even the most advanced technology alone cannot eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the superior performance of LCX circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per chip. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Crosstalk is the capacitive coupling of signals from one line to another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent.

Crosstalk has two basic causes. Forward crosstalk, Figure 13, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air ($\epsilon_r = 1$) and epoxy glass ($\epsilon_r = 4.7$). As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. This delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

Reverse crosstalk, Figure 14, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. LCX's industry-leading noise margins makes it easier to design systems immune to crosstalk-related problems.

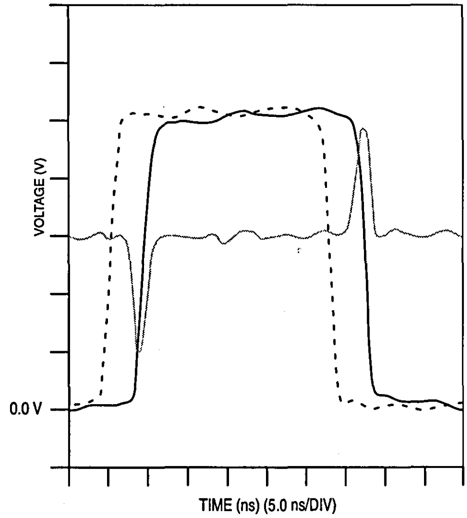


Figure 13. Forward Crosstalk on PCB Traces

Key	Vertical Scale	Horizontal Scale
- - - - - Active Driver	1.0 V/Div	50 ns/Div
——— Forward Crosstalk	0.2 V/Div	5.0 ns/Div
——— Active Receiver	1.0 V/Div	5.0 ns/Div

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

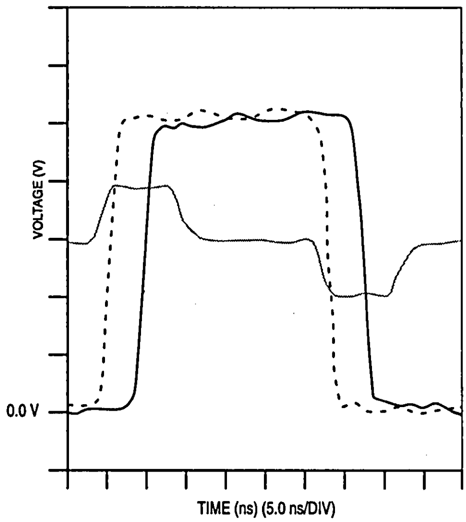


Figure 14. Reverse Crosstalk on PCB Traces

Key	Vertical Scale	Horizontal Scale
- - - - - Active Driver	1.0 V/Div	50 ns/Div
——— Forward Crosstalk	0.2 V/Div	5.0 ns/Div
——— Active Receiver	1.0 V/Div	5.0 ns/Div

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

Ground Bounce

Ground bounce occurs as a result of the intrinsic characteristics of the leadframes and bondwires of the packages used to house CMOS devices. As edge rates and drive capability increase in advanced logic families, the effects of these intrinsic electrical characteristics become more pronounced.

Figure 15 shows a simple circuit model for a device in a leadframe driving a standard test load. The inductor L1 represents the parasitic inductance in the ground lead of the package; inductor L2 represents the parasitic inductance in the power lead of the package; inductor L3 represents the parasitic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor C_L and R_L represent the standard test load on the output of the device.

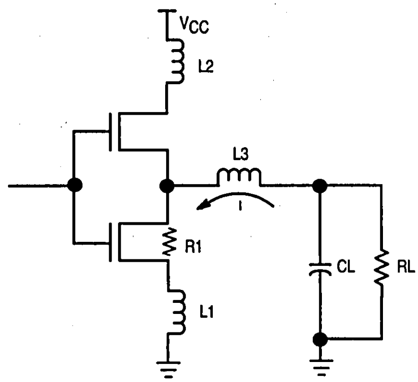


Figure 15. Output Model

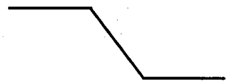


Figure 16. Output Voltage

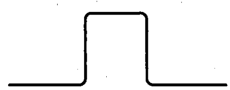


Figure 17. Output Current

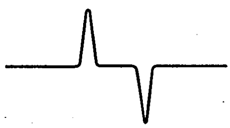


Figure 18. Inductor Voltage

The three waveforms shown in Figure 16 through Figure 18 depict how ground bounce is generated. The first waveform shows the voltage (V) across the load as it is switched from a logic HIGH to a logic LOW. The output slew rate is dependent upon the characteristics of the output transistor, the inductors L1 and L3, and C_L, the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [$I = C_L \bullet dV/dt$]. The third waveform shows the voltage that is induced across the inductance in the ground lead due to the changing currents [$V_{gb} = -L \bullet (dI/dt)$].

There are many factors which affect the amplitude of the ground bounce. Included are:

- Number of outputs switching simultaneously: more outputs result in more ground bounce.
- Type of output load: capacitive loads generate two to three times more ground bounce than typical system traces. Increasing the capacitive load to approximately 60–70 pF increases ground bounce. Beyond 70 pF, ground bounce drops off due to the filtering effect of the load. Moving the load away from the output reduces the ground bounce.
- Location of the output pin: outputs closer to the ground pin exhibit less ground bounce than those further away.
- Voltage: lowering V_{CC} reduces ground bounce.
- Test fixtures: standard test fixtures generate 30 to 50% more ground bounce than a typical system since they use capacitive loads which both increase the AC load and form LCR tank circuits that oscillate.

Ground bounce produces several symptoms:

- Altered device states. LCX does not exhibit this symptom.
- Propagation delay degradation. LCX devices are characterized not to degrade more than 200ps per additional output switching.
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.
- Quiet output noise. The LCX worst case quiet output has been characterized to be typically 800mV. It will be much less in well designed systems.

Observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce:

First, use caution when driving asynchronous TTL-level inputs from CMOS octal outputs, or

Second, use caution when running control lines (set, reset, load, clock, chip select) which are glitch-sensitive through the same devices that drive data or address lines.

When it is not possible to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:

- Locate these outputs as close to the ground pin as possible.
- Use the lowest V_{CC} possible or separate the power supplies.
- Use board design practices which reduce any additive noise sources, such as crosstalk, reflections, etc.

Design Rules

The set of design rules listed below are recommended to ensure reliable system operation by providing the optimum power supply connection to the devices. Most designers will recognize these guidelines as those they have employed with advanced bipolar logic families.

- Use multi-layer boards with V_{CC} and ground planes, with the device power pins soldered directly to the planes to ensure the lowest power line impedances possible.
- Use decoupling capacitors for every device, usually 0. 1 µF should be adequate. These capacitors should be located as close to the ground pin as possible.
- Do not use sockets or wirewrap boards whenever possible.
- Do not connect capacitors from the outputs directly to ground.

Decoupling Requirements

Motorola's LCX family, as with other high-performance, high-drive logic families, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with LCX products.

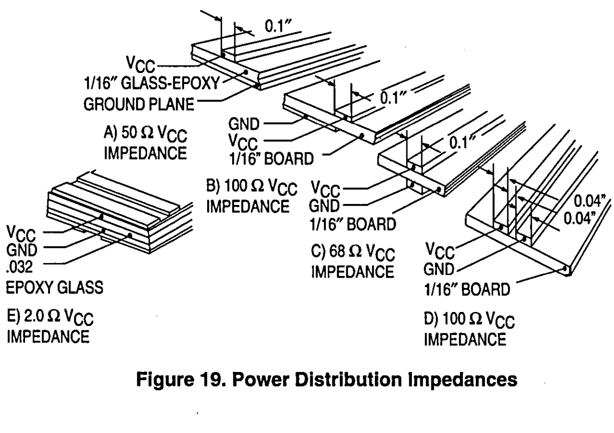


Figure 19. Power Distribution Impedances

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to a HIGH value. This power is necessary to charge the load capacitance or drive a line impedance. Figure 19 displays various V_{CC} and ground layout schemes along with associated impedances.

For most power distribution networks, the typical impedance is between 100 and 150Ω. This impedance appears in series with the load impedance and will cause a droop in the V_{CC} at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in Figure 20 to calculate the amount of decoupling necessary. This circuit utilizes an LCX240 driving a 150Ω bus from a point somewhere in the middle.

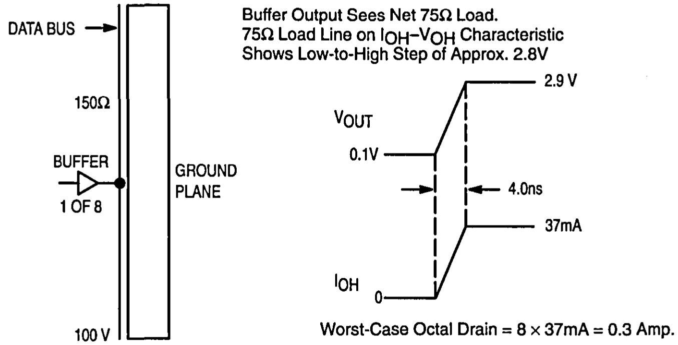


Figure 20. Octal Buffer Driving a 150Ω Bus

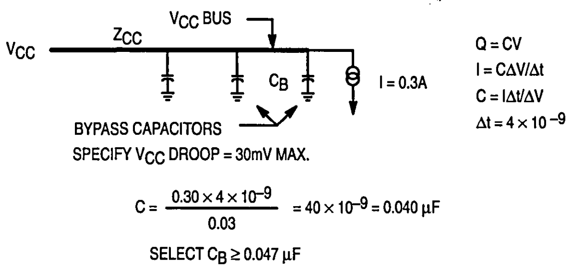
Being in the middle of the bus, the driver will see two 150Ω loads in parallel, or an effective impedance of 75Ω. To switch the line from rail to rail, a drive of 37mA is needed; about 300mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage across the impedance of the power lines, causing the actual V_{CC} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in Figure 21.

In this example, if the V_{CC} droop is to be kept below 30mV and the edge rate equals 4 ns, a 0.04µF capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package.

Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.



$Q = CV$

$I = C\Delta V/\Delta t$

$C = I\Delta t/\Delta V$

$\Delta t = 4 \times 10^{-9}$

$$C = \frac{0.30 \times 4 \times 10^{-9}}{0.03} = 40 \times 10^{-9} = 0.040\ \mu F$$

SELECT $C_B \geq 0.047\ \mu F$

Place one decoupling capacitor adjacent to each package driving any transmission line and distribute others evenly throughout the logic.

Figure 21. Formula for Calculating Decoupling Capacitors

Device Datasheets

Product Preview

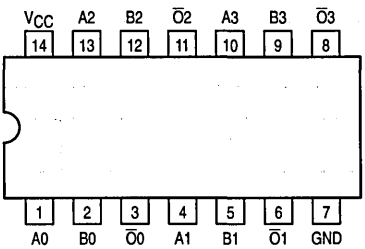
Low-Voltage CMOS Quad 2-Input NAND Gate
With 5V-Tolerant Inputs

The MC74LCX00 is a high performance, quad 2–input NAND gate operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX00 inputs to be safely driven from 5V devices.

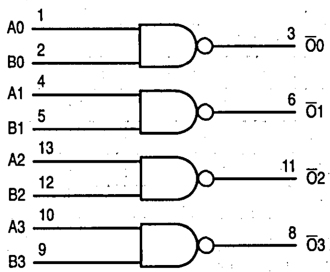
Current drive capability is 24mA at the outputs.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant Inputs — Interface Capability With 5V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

Pinout: 14–Lead (Top View)



LOGIC DIAGRAM



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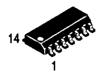
MC74LCX00

LCX

LOW–VOLTAGE CMOS QUAD 2–INPUT NAND GATE



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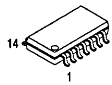

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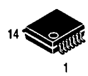

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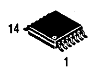


DT SUFFIX
PLASTIC TSSOP
CASE 948G–01

PIN NAMES

Pins	Function
An, Bn	Data Inputs
$\overline{O}n$	Outputs

FUNCTION TABLE

Inputs		Outputs
An	Bn	$\overline{O}n$
L	L	H
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
V_O	DC Output Voltage	$-0.5 \leq V_O \leq V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State)	0		V_{CC}	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \leq V_{CC} \leq 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \leq V_{CC} \leq 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \leq V_{CC} \leq 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \leq V_{CC} \leq 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \geq 2.4V$, $V_{IL} \leq 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	μA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	μA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I \le 5.5V$		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	μA

AC CHARACTERISTICS[1] ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits T_A = –40°C to +85°C V_{CC} = 3.0V to 3.6V Min	V_{CC} = 3.0V to 3.6V Max	V_{CC} = 2.7V Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	5.2 5.2	6.0 6.0	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0		ns

1. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

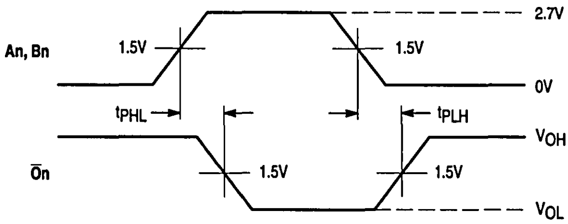
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C Min	Typ	Max	Unit
V_{OLP}	Dynamic LOW Peak Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V

1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

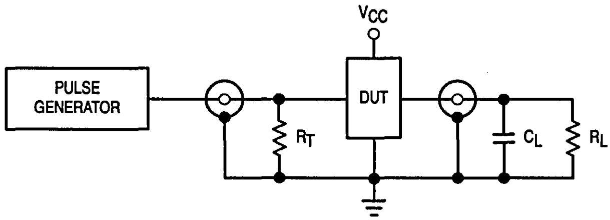
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF



PROPAGATION DELAYS
$t_R = t_F = 2.5$ns, 10% to 90%; f = 1MHz; $t_W = 500$ns

Figure 1. AC Waveforms



C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Product Preview

Low-Voltage CMOS Quad 2-Input NOR Gate

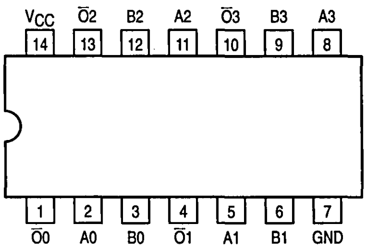
With 5V-Tolerant Inputs

The MC74LCX02 is a high performance, quad 2–input NOR gate operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX02 inputs to be safely driven from 5V devices.

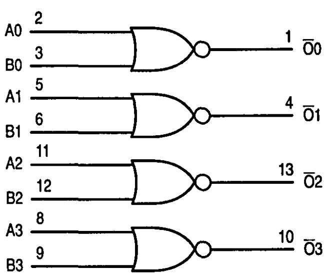
Current drive capability is 24mA at the outputs.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant Inputs — Interface Capability With 5V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

Pinout: 14–Lead (Top View)



LOGIC DIAGRAM



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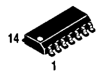
MC74LCX02

LCX

LOW–VOLTAGE CMOS QUAD 2–INPUT NOR GATE



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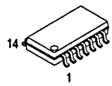

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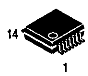
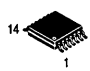


SD SUFFIX
PLASTIC SSOP
CASE 940A–03



DT SUFFIX
PLASTIC TSSOP
CASE 948G–01

PIN NAMES

Pins	Function
An, Bn $\overline{On}$	Data Inputs Outputs

FUNCTION TABLE

INPUTS		OUTPUTS
An	Bn	$\overline{On}$
L	L	H
L	H	L
H	L	L
H	H	L

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
V_O	DC Output Voltage	$-0.5 \leq V_O \leq V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State)	0		V_{CC}	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \leq V_{CC} \leq 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \leq V_{CC} \leq 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \leq V_{CC} \leq 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \leq V_{CC} \leq 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \geq 2.4V$, $V_{IL} \leq 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I \le 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS[1] ($t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Waveform	Limits			Unit
			T_A = –40°C to +85°C			
			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V	
			Min	Max	Max	
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	5.2 5.2	6.0 6.0	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0		ns

1. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

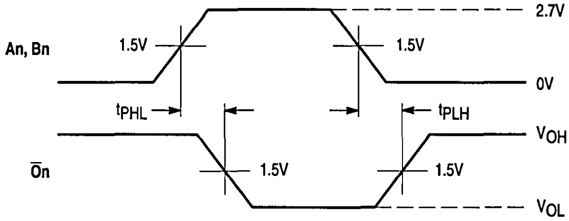
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V

1. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

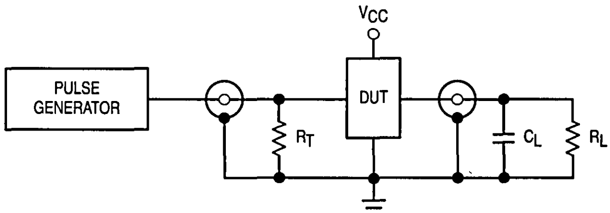
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF



PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 1. AC Waveforms



C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

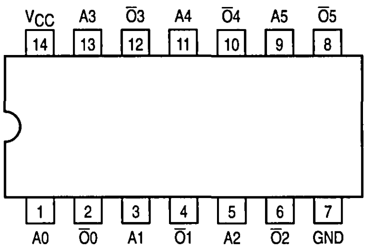
Low-Voltage CMOS Hex Inverter
With 5V-Tolerant Inputs

The MC74LCX04 is a high performance hex inverter operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX04 inputs to be safely driven from 5V devices.

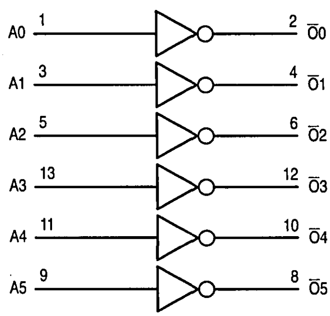
Current drive capability is 24mA at the outputs.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant Inputs — Interface Capability With 5V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

Pinout: 14–Lead (Top View)



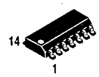
LOGIC DIAGRAM



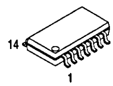
MC74LCX04

LCX

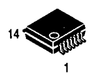
LOW–VOLTAGE CMOS HEX INVERTER



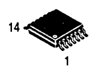
D SUFFIX
PLASTIC SOIC
CASE 751A–03



M SUFFIX
PLASTIC SOIC EIAJ
CASE 965–01



SD SUFFIX
PLASTIC SSOP
CASE 940A–03



DT SUFFIX
PLASTIC TSSOP
CASE 948G–01

PIN NAMES

Pins	Function
An $\overline{On}$	Data Inputs Outputs

FUNCTION TABLE

An	$\overline{On}$
L	H
H	L

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State)	0		V_{CC}	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	$T_A = -40°C$ to $+85°C$ Min	Max	Unit
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I \le 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits, $T_A = -40°C$ to $+85°C$, V_{CC} = 3.0V to 3.6V, Min	V_{CC} = 3.0V to 3.6V, Max	V_{CC} = 2.7V, Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	5.2 5.2	6.0 6.0	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1)			1.0 1.0		ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

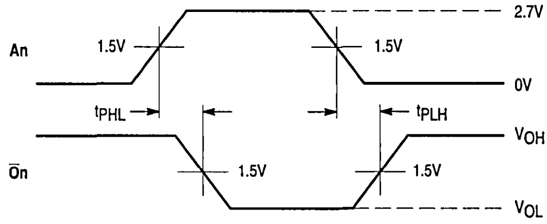
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25°C$ Min	Typ	Max	Unit
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

1. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

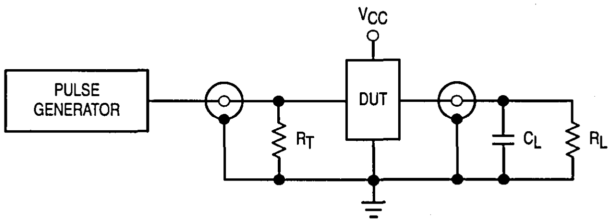
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, V_I = 0V or V_{CC}	8	pF



PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 1. AC Waveforms



C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Product Preview

Low-Voltage CMOS Quad 2-Input AND Gate

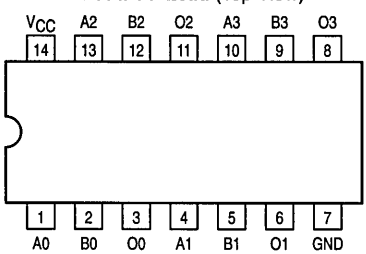
With 5V-Tolerant Inputs

The MC74LCX08 is a high performance, quad 2–input AND gate operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX08 inputs to be safely driven from 5V devices.

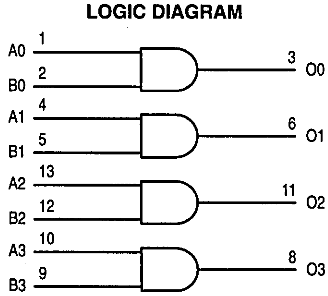
Current drive capability is 24mA at the outputs.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant Inputs — Interface Capability With 5V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

Pinout: 14–Lead (Top View)



LOGIC DIAGRAM

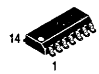


This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

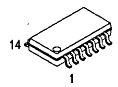
MC74LCX08

LCX

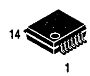
LOW–VOLTAGE CMOS QUAD 2–INPUT AND GATE



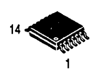
D SUFFIX
PLASTIC SOIC
CASE 751A–03



M SUFFIX
PLASTIC SOIC EIAJ
CASE 965–01



SD SUFFIX
PLASTIC SSOP
CASE 940A–03



DT SUFFIX
PLASTIC TSSOP
CASE 948G–01

PIN NAMES

Pins	Function
An, Bn On	Data Inputs Outputs

FUNCTION TABLE

INPUTS		OUTPUTS
An	**Bn**	**On**
L	L	L
L	H	L
H	L	L
H	H	H

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State)	0		V_{CC}	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OH} = –100µA	V_{CC} – 0.2		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OL} = 100µA		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I \le 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS[1] ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits			Unit
			T_A = –40°C to +85°C			
			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V	
			Min	Max	Max	
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	5.5 5.5	6.2 6.2	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0		ns

1. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

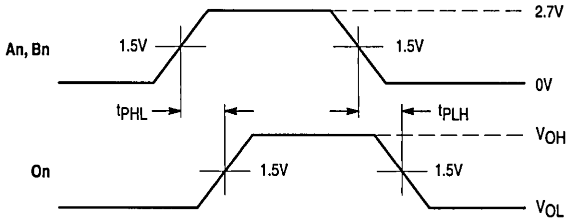
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

1. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

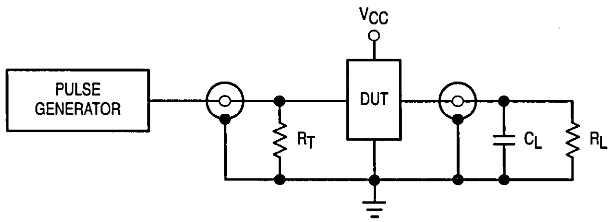
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, V_I = 0V or V_{CC}	8	pF



PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 1. AC Waveforms



C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Product Preview

Low-Voltage CMOS Quad 2-Input OR Gate

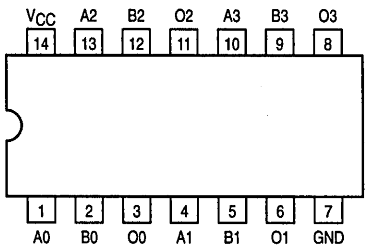
With 5V-Tolerant Inputs

The MC74LCX32 is a high performance, quad 2–input OR gate operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX32 inputs to be safely driven from 5V devices.

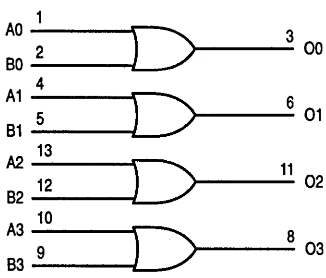
Current drive capability is 24mA at the outputs.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant Inputs — Interface Capability With 5V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

Pinout: 14–Lead (Top View)



LOGIC DIAGRAM



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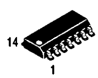
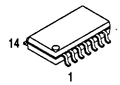
MC74LCX32

LCX

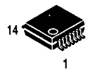
LOW–VOLTAGE CMOS QUAD 2–INPUT OR GATE



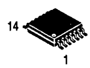
D SUFFIX
PLASTIC SOIC
CASE 751A–03



M SUFFIX
PLASTIC SOIC EIAJ
CASE 965–01



SD SUFFIX
PLASTIC SSOP
CASE 940A–03



DT SUFFIX
PLASTIC TSSOP
CASE 948G–01

PIN NAMES

Pins	Function
An, Bn	Data Inputs
On	Outputs

FUNCTION TABLE

INPUTS		OUTPUTS
An	Bn	On
L	L	L
L	H	H
H	L	H
H	H	H

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	–50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State)	0		V_{CC}	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V				–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V				24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V				–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V				12	mA
T_A	Operating Free–Air Temperature		–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V		0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	$T_A = -40°C$ to $+85°C$		Unit
			Min	Max	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I \le 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS[1] ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits			Unit
			$T_A = -40°C$ to $+85°C$			
			$V_{CC} = 3.0V$ to $3.6V$		$V_{CC} = 2.7V$	
			Min	Max	Max	
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	5.5 5.5	6.2 6.2	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0		ns

1. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

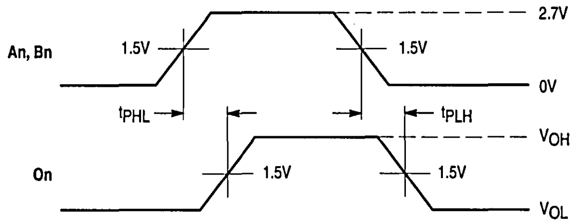
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25°C$			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

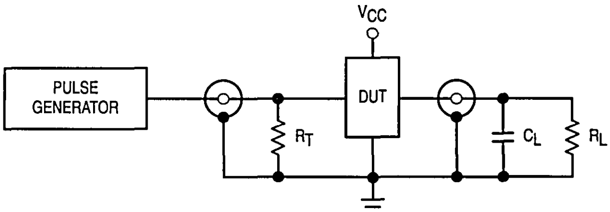
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, V_I = 0V or V_{CC}	8	pF



PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 1. AC Waveforms



C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

MC74LCX74

LCX

LOW–VOLTAGE CMOS
DUAL D–TYPE FLIP–FLOP

Product Preview

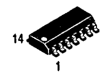
Low-Voltage CMOS Dual D-Type Flip-Flop

With 5V-Tolerant Inputs

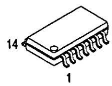
The MC74LCX74 is a high performance, dual D–type flip–flop with asynchronous clear and set inputs and complementary (O, $\overline{O}$) outputs. It operates from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX74 inputs to be safely driven from 5V devices.

The MC74LCX74 consists of 2 edge–triggered flip–flops with individual D–type inputs. The flip–flop will store the state of individual D inputs, that meet the setup and hold time requirements, on the LOW–to–HIGH Clock (CP) transition.

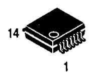
- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant Inputs — Interface Capability With 5V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



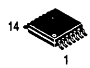
D SUFFIX
PLASTIC SOIC
CASE 751A–03



M SUFFIX
PLASTIC SOIC EIAJ
CASE 965–01

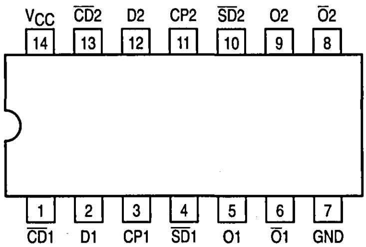


SD SUFFIX
PLASTIC SSOP
CASE 940A–03



DT SUFFIX
PLASTIC TSSOP
CASE 948G–01

Pinout: 14–Lead (Top View)



PIN NAMES

Pins	Function
CP1, CP2	Clock Pulse Inputs
D1, D2	Data Inputs
$\overline{CD}1$, $\overline{CD}2$	Direct Clear Inputs
$\overline{SD}1$, $\overline{SD}2$	Direct Set Inputs
On, $\overline{O}$n	Outputs

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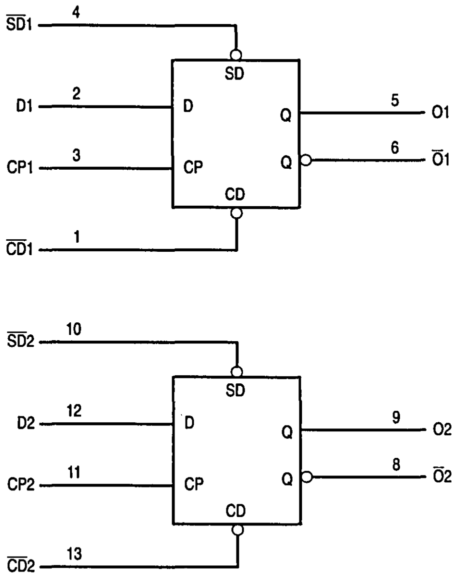
LOGIC DIAGRAM



INPUTS				OUTPUTS		OPERATING MODE
$\overline{SDn}$	$\overline{CDn}$	CPn	Dn	On	$\overline{On}$	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Clear
L	L	X	X	H	H	Undetermined
H	H	↑	h	H	L	Load and Read Register
H	H	↑	l	L	H	
H	H	‡	X	NC	NC	Hold

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; NC = No Change; X = High or Low Voltage Level or Transitions are Acceptable; ↑ = Low–to–High Transition; ‡ = Not a Low–to–High Transition; For I_{CC} Reasons DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State)	0		V_{CC}	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OH} = –100μA	V_{CC} – 0.2		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OL} = 100μA		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I \le 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS[1] ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits, T_A = –40°C to +85°C, V_{CC} = 3.0V to 3.6V Min	V_{CC} = 3.0V to 3.6V Max	V_{CC} = 2.7V Min	V_{CC} = 2.7V Max	Unit
f_{max}	Clock Pulse Frequency	1	150				MHz
t_{PLH} t_{PHL}	Propagation Delay CPn to On or $\overline{On}$	1	1.5 1.5	7.0 7.0		8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{SDn}$ or $\overline{CDn}$ to On or $\overline{On}$	2	1.5 1.5	7.0 7.0		8.0 8.0	ns
t_s	Setup Time, HIGH or LOW Dn to CPn	1	2.5		2.5		ns
t_h	Hold Time, HIGH or LOW Dn to CPn	1	1.5		1.5		ns
t_w	CPn Pulse Width, HIGH or LOW	1	3.3		3.3		ns
	$\overline{SDn}$ or $\overline{CDn}$ Pulse Width, LOW	3	3.3		3.3		ns
t_{rec}	Recovery Time $\overline{SDn}$ or $\overline{CDn}$ to CPn	1	2.0		2.5		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0			ns

1. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

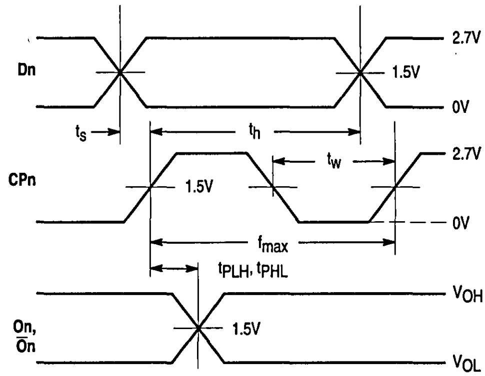
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C Min	Typ	Max	Unit
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

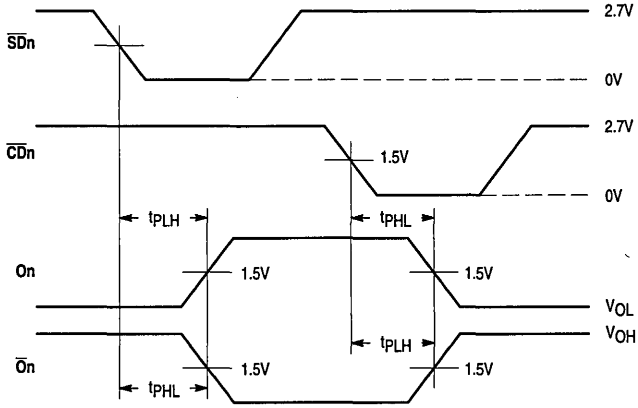
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

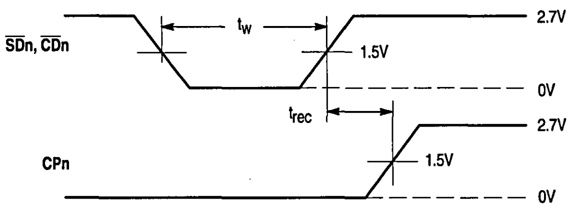
Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, V_I = 0V or V_{CC}	8	pF



WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

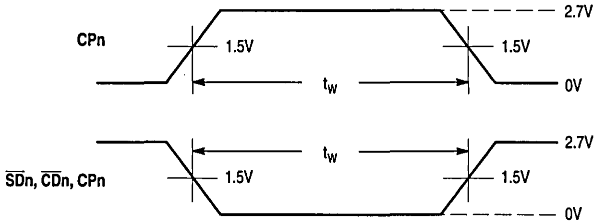


WAVEFORM 2 – PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



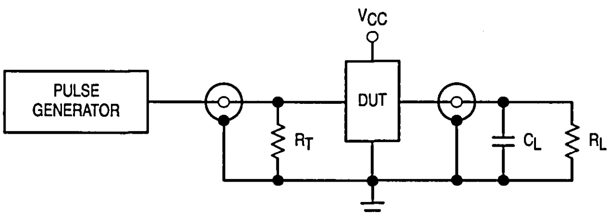
WAVEFORM 3 – RECOVERY TIME
$t_R = t_F = 2.5ns$ from 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 1. AC Waveforms



WAVEFORM 4 – PULSE WIDTH
$t_R = t_F$ = 2.5ns (or fast as required) from 10% to 90%;
Output requirements: $V_{OL} \leq 0.8V$, $V_{OH} \geq 2.0V$

Figure 1. AC Waveforms (continued)



C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Product Preview

Low-Voltage CMOS Quad 2-Input XOR Gate

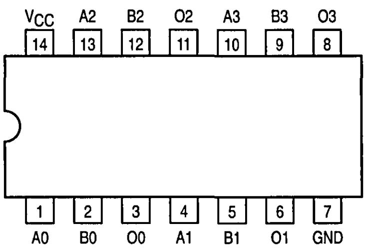
With 5V-Tolerant Inputs

The MC74LCX86 is a high performance, quad 2–input XOR gate operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX86 inputs to be safely driven from 5V devices.

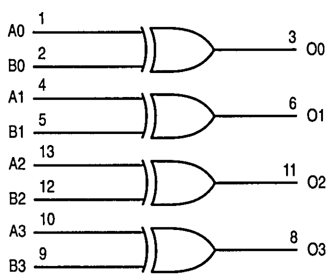
Current drive capability is 24mA at the outputs.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant Inputs — Interface Capability With 5V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

Pinout: 14–Lead (Top View)



LOGIC DIAGRAM

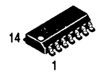


This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

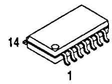
MC74LCX86

LCX

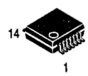
LOW–VOLTAGE CMOS QUAD 2–INPUT XOR GATE



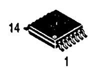
D SUFFIX
PLASTIC SOIC
CASE 751A–03



M SUFFIX
PLASTIC SOIC EIAJ
CASE 965–01



SD SUFFIX
PLASTIC SSOP
CASE 940A–03



DT SUFFIX
PLASTIC TSSOP
CASE 948G–01

PIN NAMES

Pins	Function
An, Bn $\overline{On}$	Data Inputs Outputs

FUNCTION TABLE

Inputs		Outputs
An	Bn	$\overline{On}$
L	L	L
L	H	H
H	L	H
H	H	L

REV 0

Product Preview

Low-Voltage CMOS Quad Buffer

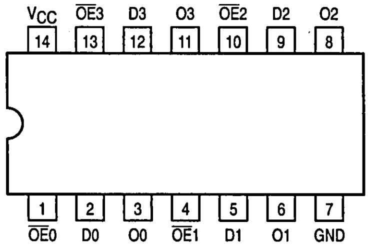
With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX125 is a high performance, non–inverting quad buffer operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX125 inputs to be safely driven from 5V devices. The MC74LCX125 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

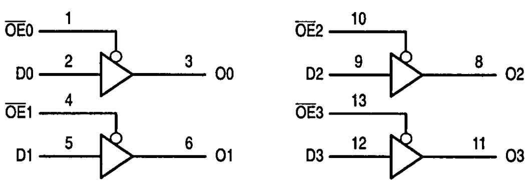
Current drive capability is 24mA at the outputs. The Output Enable ($\overline{OE}$n) inputs, when HIGH, disable the outputs by placing them in a HIGH Z condition.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

Pinout: 14–Lead (Top View)



LOGIC DIAGRAM



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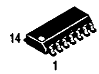
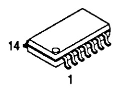
MC74LCX125

LCX

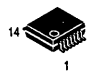
LOW–VOLTAGE CMOS QUAD BUFFER



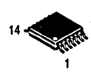
D SUFFIX
PLASTIC SOIC
CASE 751A–03



M SUFFIX
PLASTIC SOIC EIAJ
CASE 965–01



SD SUFFIX
PLASTIC SSOP
CASE 940A–03



DT SUFFIX
PLASTIC TSSOP
CASE 948G–01

PIN NAMES

Pins	Function
$\overline{OE}$n	Output Enable Inputs
Dn	Data Inputs
On	3–State Outputs

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$n	Dn	On
L	L	L
L	H	H
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	–50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage — (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

			T_A = –40°C to +85°C		
Symbol	Characteristic	Condition	Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS[1] ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits T_A = –40°C to +85°C V_{CC} = 3.0V to 3.6V Min	V_{CC} = 3.0V to 3.6V Max	V_{CC} = 2.7V Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	6.0 6.0	6.5 6.5	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	7.0 7.0	8.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	6.0 6.0	7.0 7.0	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0		ns

1. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

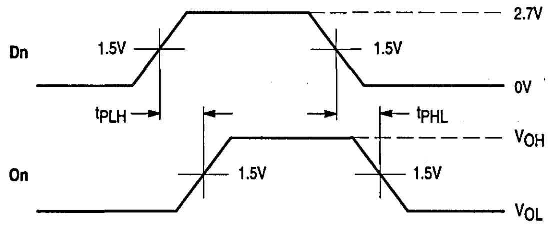
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C Min	Typ	Max	Unit
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

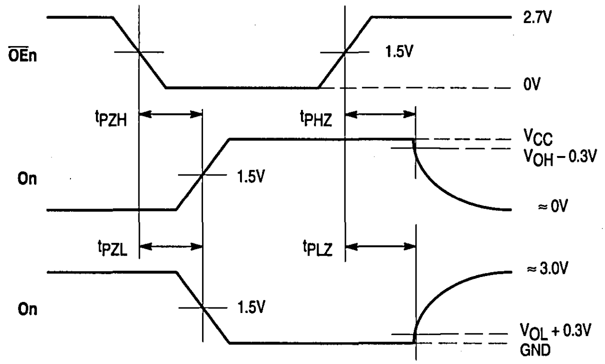
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	25	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF

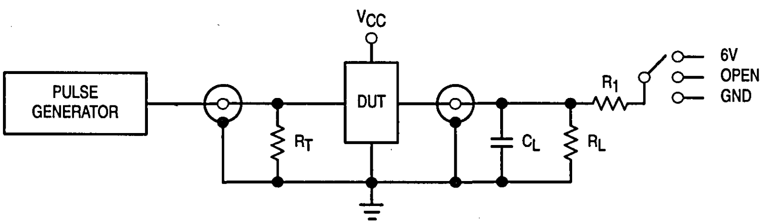


WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Product Preview

Low-Voltage CMOS 1-of-8 Decoder/Demultiplexer

With 5V-Tolerant Inputs

The MC74LCX138 is a high performance, 1–of–8 decoder/demultiplexer operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX138 inputs to be safely driven from 5V devices. The MC74LCX138 is suitable for memory address decoding and other TTL level bus oriented applications.

The MC74LCX138 high-speed 1–of–8 decoder/demultiplexer accepts three binary weighted inputs (A0, A1, A2) and, when enabled, provides eight mutually exclusive active–LOW outputs ($\overline{O0}$–$\overline{O7}$). The LCX138 features three Enable inputs, two active–LOW ($\overline{E1}$, $\overline{E2}$) and one active–HIGH (E3). All outputs will be HIGH unless $\overline{E1}$ and $\overline{E2}$ are LOW, and E3 is HIGH. This multiple enabled function allows easy parallel expansion of the device to a 1–of–32 (5 lines to 32 lines) decoder with just four LCX138 devices and one inverter (See Figure 1). The LCX138 can be used as an 8–output demultiplexer by using one of the active–LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active–HIGH or active–LOW state.

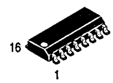
Current drive capability is 24mA at the outputs.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant Inputs — Interface Capability With 5V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

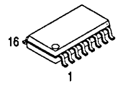
MC74LCX138

LCX

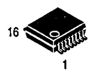
LOW–VOLTAGE CMOS DECODER/DEMULTIPLEXER



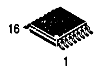
D SUFFIX
PLASTIC SOIC
CASE 751B–05



M SUFFIX
PLASTIC SOIC EIAJ
CASE 966–01

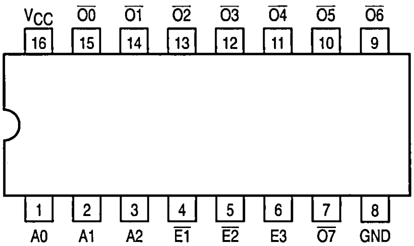


SD SUFFIX
PLASTIC SSOP
CASE 940B–03



DT SUFFIX
PLASTIC TSSOP
CASE 948F–01

Pinout: 16–Lead Plastic Package (Top View)



PIN NAMES

Pins	Function
A0–A2	Address Inputs
$\overline{E1}$–$\overline{E2}$	Enable Inputs
E3	Enable Input
$\overline{O0}$–$\overline{O7}$	Outputs

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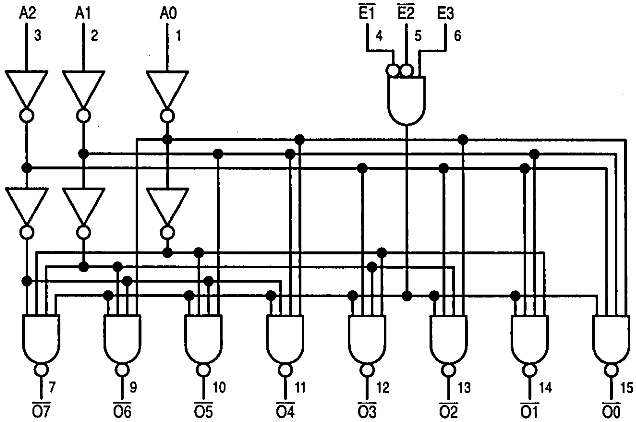
LOGIC DIAGRAM



INPUTS						OUTPUTS							
$\overline{E1}$	$\overline{E2}$	E3	A0	A1	A2	$\overline{O0}$	$\overline{O1}$	$\overline{O2}$	$\overline{O3}$	$\overline{O4}$	$\overline{O5}$	$\overline{O6}$	$\overline{O7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Voltage Level; L = Low Voltage Level; X = High or Low Voltage Level and Transitions Are Acceptable; For I_{CC} reasons, DO NOT FLOAT Inputs

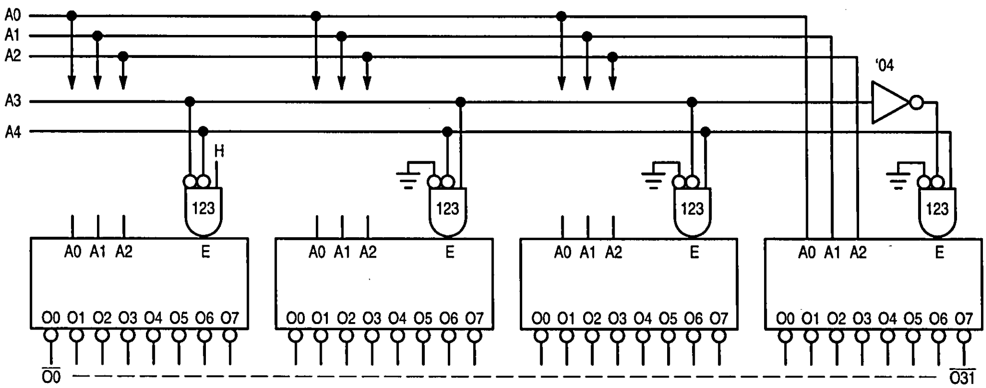


Figure 1. Expansion to 1–of–32 Decoding

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State)	0		V_{CC}	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	2.7V ≤ V_{CC} ≤ 3.6V	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	2.7V ≤ V_{CC} ≤ 3.6V		0.8	V
V_{OH}	HIGH Level Output Voltage	2.7V ≤ V_{CC} ≤ 3.6V; I_{OH} = –100µA	V_{CC} – 0.2		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	2.7V ≤ V_{CC} ≤ 3.6V; I_{OL} = 100µA		0.2	V
		V_{CC} = 2.7V; I_{OL}= 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	
I_I	Input Leakage Current	2.7V ≤ V_{CC} ≤ 3.6V; 0V ≤ V_I ≤ 5.5V		±5.0	µA
I_{CC}	Quiescent Supply Current	2.7 ≤ V_{CC} ≤ 3.6V; V_I = GND or V_{CC}		10	µA
		2.7 ≤ V_{CC} ≤ 3.6V; 3.6 ≤ V_I ≤ 5.5V		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	2.7 ≤ V_{CC} ≤ 3.6V; V_{IH} = V_{CC} – 0.6V		500	µA

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use V_{IH} ≥ 2.4V, V_{IL} ≤ 0.5V.

AC CHARACTERISTICS[1] (t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Waveform	Limits, T_A = –40°C to +85°C, V_{CC} = 3.0V to 3.6V Min	V_{CC} = 3.0V to 3.6V Max	V_{CC} = 2.7V Max	Unit
t_{PLH} t_{PHL}	Propagation Delay An to $\overline{On}$	1, 2	1.5 1.5	6.0 6.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E1}$, $\overline{E2}$ to $\overline{On}$	2	1.5 1.5	6.0 6.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay E3 to $\overline{On}$	1	1.5 1.5	7.0 7.0	8.0 8.0	ns

1. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF

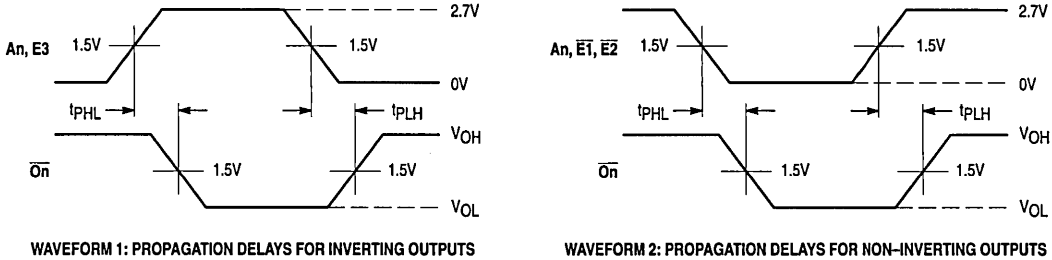
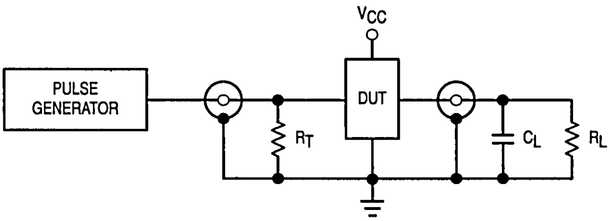


Figure 2. AC Waveforms



C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 3. Test Circuit

Product Preview

Low-Voltage CMOS Quad 2-Input Multiplexer

With 5V-Tolerant Inputs

MC74LCX157

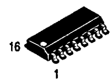
LCX

LOW–VOLTAGE CMOS QUAD 2–INPUT MULTIPLEXER

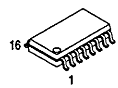
The MC74LCX157 is a high performance, quad 2–input multiplexer operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX157 inputs to be safely driven from 5V devices.

Four bits of data from two sources can be selected using the Select and Enable inputs. The four outputs present the selected data in the true (non–inverted) form. The MC74LCX157 can also be used as a function generator. Current drive capability is 24mA at the outputs.

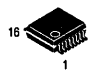
- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant Inputs — Interface Capability With 5V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



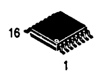
D SUFFIX
PLASTIC SOIC
CASE 751B–05



M SUFFIX
PLASTIC SOIC EIAJ
CASE 966–01

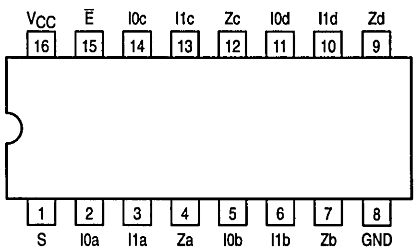


SD SUFFIX
PLASTIC SSOP
CASE 940B–03



DT SUFFIX
PLASTIC TSSOP
CASE 948F–01

Pinout: 16–Lead Plastic Package (Top View)



TRUTH TABLE

Inputs				Outputs
E̅	S	I0n	I1n	Zn
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

PIN NAMES

Pins	Function
I0n	Source 0 Data Inputs
I1n	Source 1 Data Inputs
E̅	Enable Input
S	Select Input
Zn	Outputs

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Low-Voltage CMOS Octal Buffer
With 5V-Tolerant Inputs and Outputs (3-State, Inverting)

MC74LCX240

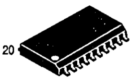
LCX

LOW–VOLTAGE CMOS OCTAL BUFFER

The MC74LCX240 is a high performance, inverting octal buffer operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX240 inputs to be safely driven from 5V devices. The MC74LCX240 is suitable for memory address driving and all TTL level bus oriented buffer applications.

Current drive capability is 24mA at the outputs. The Output Enable ($\overline{OE}$) input, when HIGH, disables the outputs by placing them in a HIGH Z condition.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V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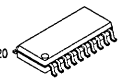
DW SUFFIX
PLASTIC SOIC
CASE 751D–04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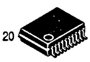
M SUFFIX
PLASTIC SOIC EIAJ
CASE 967–01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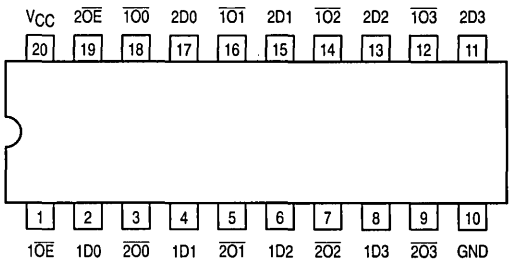
SD SUFFIX
PLASTIC SSOP
CASE 940C–03


20
1

DT SUFFIX
PLASTIC TSSOP
CASE 948E–02

Pinout: 20–Lead (Top View)



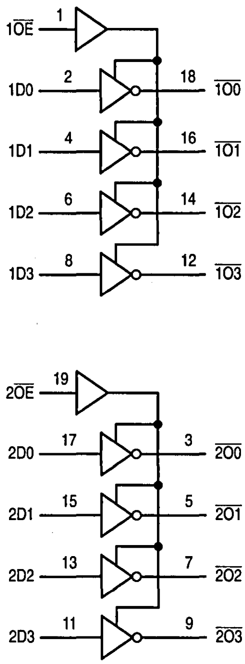
PIN NAMES

Pins	Function
n$\overline{OE}$	Output Enable Inputs
1Dn, 2Dn	Data Inputs
$\overline{1On}$, $\overline{2On}$	3–State Outputs

REV 3

MOTOROLA

LOGIC DIAGRAM



INPUTS		OUTPUTS
$\overline{1OE}$ $\overline{2OE}$	1Dn 2Dn	$\overline{1On}$, $\overline{2On}$
L	L	H
L	H	L
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.
1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V				–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V				24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V				–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V				12	mA
T_A	Operating Free–Air Temperature		–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V		0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

			T_A = –40°C to +85°C		
Symbol	Characteristic	Condition	Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits T_A = –40°C to +85°C V_{CC} = 3.0V to 3.6V Min	V_{CC} = 3.0V to 3.6V Max	V_{CC} = 2.7V Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	6.5 6.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	8.0 8.0	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	7.0 7.0	8.0 8.0	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1)			1.0 1.0		ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

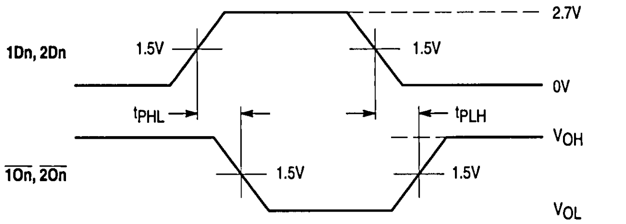
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C Min	Typ	Max	Unit
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

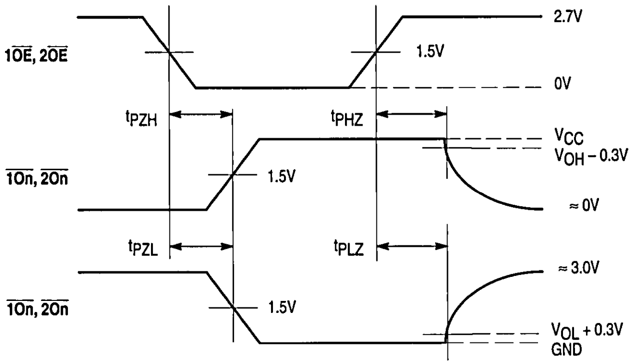
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	25	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF

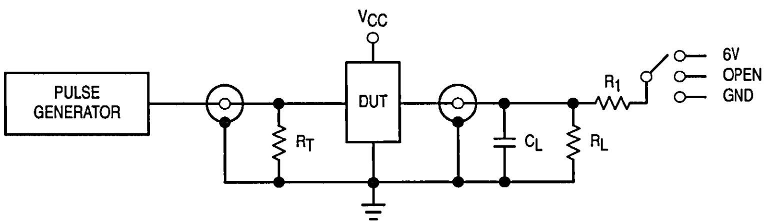


WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Low-Voltage CMOS Octal Buffer

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX244

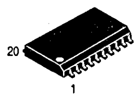
LCX

LOW–VOLTAGE CMOS OCTAL BUFFER

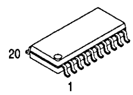
The MC74LCX244 is a high performance, non–inverting octal buffer operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX244 inputs to be safely driven from 5V devices. The MC74LCX244 is suitable for memory address driving and all TTL level bus oriented buffer applications.

Current drive capability is 24mA at the outputs. The Output Enable ($\overline{OE}$) input, when HIGH, disables the output by placing them in a HIGH Z condition.

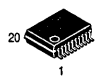
- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



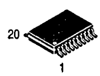
DW SUFFIX
PLASTIC SOIC
CASE 751D–04



M SUFFIX
PLASTIC SOIC EIAJ
CASE 967–01

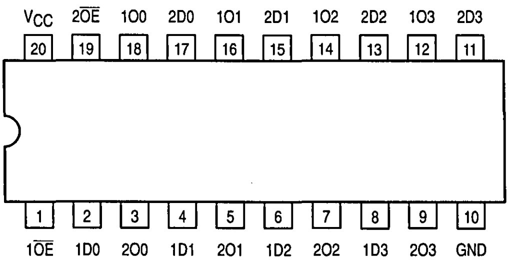


SD SUFFIX
PLASTIC SSOP
CASE 940C–03



DT SUFFIX
PLASTIC TSSOP
CASE 948E–02

Pinout: 20–Lead (Top View)

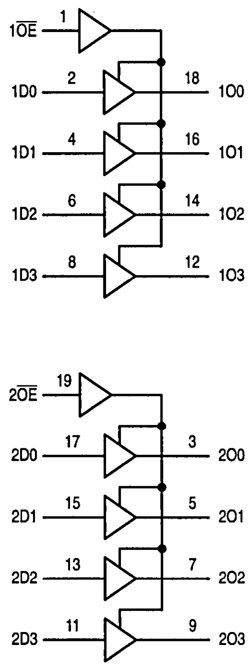


PIN NAMES

Pins	Function
n$\overline{OE}$	Output Enable Inputs
1Dn, 2Dn	Data Inputs
1On, 2On	3-State Outputs

MOTOROLA

LOGIC DIAGRAM



INPUTS		OUTPUTS
$1\overline{OE}$ $2\overline{OE}$	1Dn 2Dn	1On, 2On
L	L	L
L	H	H
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage — (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits			Unit
			T_A = –40°C to +85°C			
			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V	
			Min	Max	Max	
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	6.5 6.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	8.0 8.0	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	7.0 7.0	8.0 8.0	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1)			1.0 1.0		ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

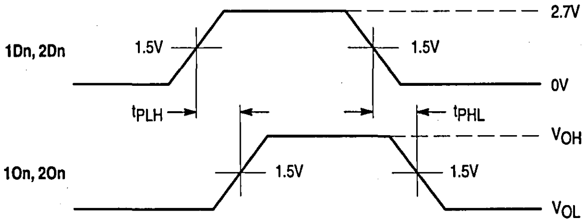
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

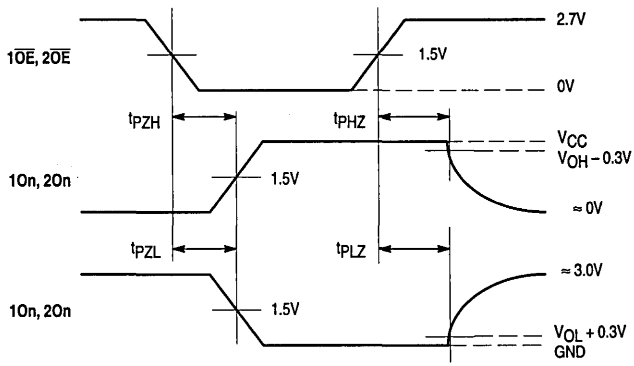
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, V_I = 0V or V_{CC}	8	pF

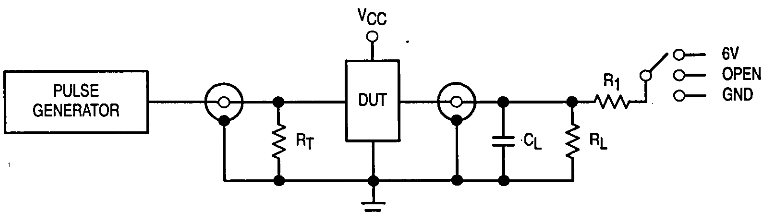


WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Low-Voltage CMOS Octal Transceiver

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX245 is a high performance, non–inverting octal transceiver operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX245 inputs to be safely driven from 5V devices. The MC74LCX245 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

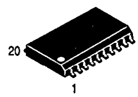
Current drive capability is 24mA at both A and B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bi–directional transceiver. Transmit (active–HIGH) enables data from A ports to B ports; Receive (active–LOW) enables data from B to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

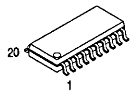
MC74LCX245

LCX

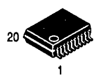
LOW–VOLTAGE CMOS OCTAL TRANSCEIVER



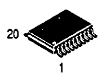
DW SUFFIX
PLASTIC SOIC
CASE 751D–04



M SUFFIX
PLASTIC SOIC EIAJ
CASE 967–01

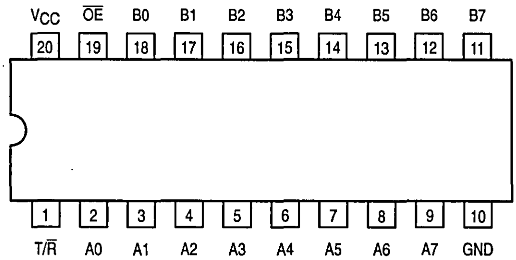


SD SUFFIX
PLASTIC SSOP
CASE 940C–03



DT SUFFIX
PLASTIC TSSOP
CASE 948E–02

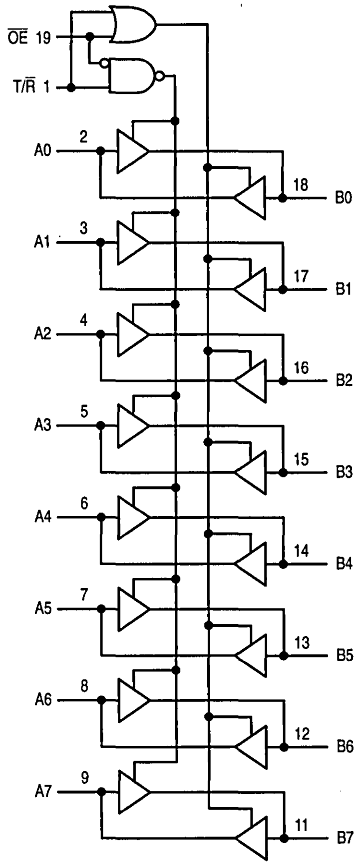
Pinout: 20–Lead (Top View)



PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A0–A7	Side A 3–State Inputs or 3–State Outputs
B0–B7	Side B 3–State Inputs or 3–State Outputs

LOGIC DIAGRAM



INPUTS		OPERATING MODE Non–Inverting
$\overline{OE}$	T/$\overline{R}$	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable; For I_{CC} reasons, Do Not Float Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

			T_A = –40°C to +85°C		
Symbol	Characteristic	Condition	Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
I_I	Input Leakage Current	2.7V ≤ V_{CC} ≤ 3.6V; 0V ≤ V_I ≤ 5.5V		±5.0	μA
I_{OZ}	3–State Output Current	2.7 ≤ V_{CC} ≤ 3.6V; 0V ≤ V_O ≤ 5.5V; V_I = V_{IH} or V_{IL}		±5.0	μA
I_{OFF}	Power–Off Leakage Current	V_{CC} = 0V; V_I or V_O = 5.5V		10	μA
I_{CC}	Quiescent Supply Current	2.7 ≤ V_{CC} ≤ 3.6V; V_I = GND or V_{CC}		10	μA
		2.7 ≤ V_{CC} ≤ 3.6V; 3.6 ≤ V_I or V_O ≤ 5.5V		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	2.7 ≤ V_{CC} ≤ 3.6V; V_{IH} = V_{CC} – 0.6V		500	μA

AC CHARACTERISTICS (t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Waveform	Limits, T_A = –40°C to +85°C, V_{CC} = 3.0V to 3.6V Min	V_{CC} = 3.0V to 3.6V Max	V_{CC} = 2.7V Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	7.0 7.0	8.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	8.5 8.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	7.5 7.5	8.5 8.5	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1)			1.0 1.0		ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

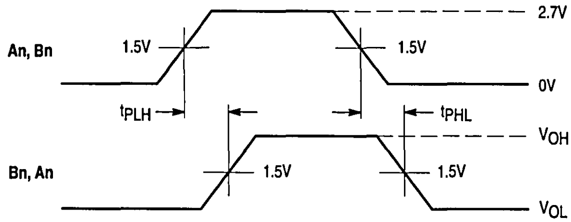
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C Min	Typ	Max	Unit
V_{OLP}	Dynamic LOW Peak Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V

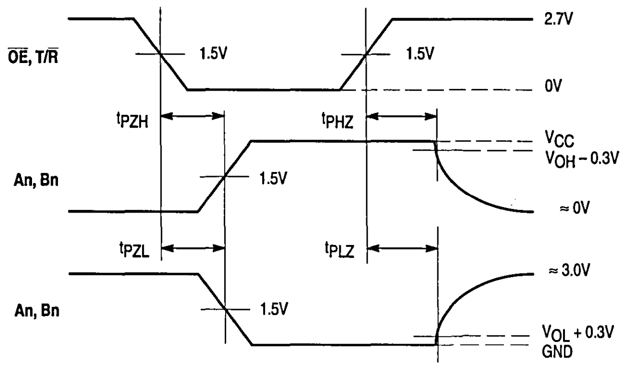
1. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF

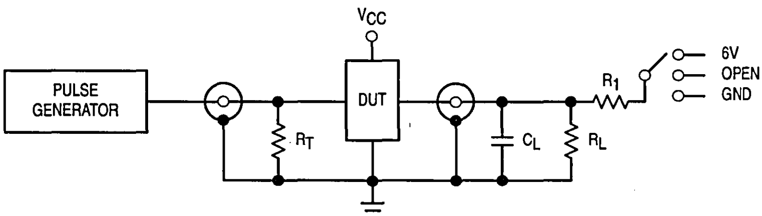


WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Product Preview

Low-Voltage CMOS Quad 2-Input Multiplexer

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX257

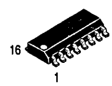
LCX

LOW–VOLTAGE CMOS QUAD 2–INPUT MULTIPLEXER

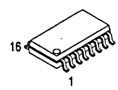
The MC74LCX257 is a high performance, quad 2–input multiplexer with 3–state outputs operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX257 inputs to be safely driven from 5V devices.

Four bits of data from two sources can be selected using the Select input. The four outputs present the selected data in the true (non–inverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the Output Enable ($\overline{OE}$) input. Current drive capability is 24mA at the outputs.

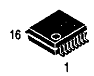
- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



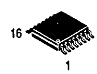
D SUFFIX
PLASTIC SOIC
CASE 751B–05



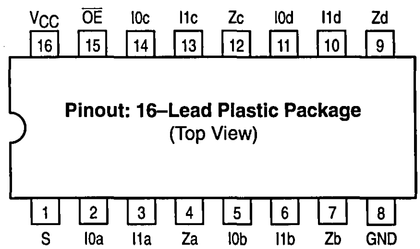
M SUFFIX
PLASTIC SOIC EIAJ
CASE 966–01



SD SUFFIX
PLASTIC SSOP
CASE 940B–03



DT SUFFIX
PLASTIC TSSOP
CASE 948F–01



PIN NAMES

Pins	Function
I0n	Source 0 Data Inputs
I1n	Source 1 Data Inputs
$\overline{OE}$	Output Enable Input
S	Select Input
Zn	Outputs

TRUTH TABLE

Inputs				Outputs
$\overline{OE}$	S	I0n	I1n	Zn
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Low-Voltage CMOS Octal Transparent Latch
With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX373

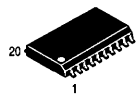
LCX

LOW–VOLTAGE CMOS OCTAL TRANSPARENT LATCH

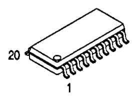
The MC74LCX373 is a high performance, non–inverting octal transparent latch operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX373 inputs to be safely driven from 5V devices.

The MC74LCX373 contains 8 D–type latches with 3–state outputs. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH–to–LOW transition of LE. The 3–state standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are enabled. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches.

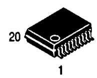
- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



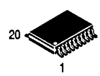
DW SUFFIX
PLASTIC SOIC
CASE 751D–04



M SUFFIX
PLASTIC SOIC EIAJ
CASE 967–01

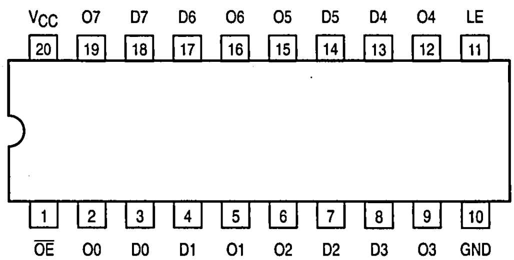


SD SUFFIX
PLASTIC SSOP
CASE 940C–03



DT SUFFIX
PLASTIC TSSOP
CASE 948E–02

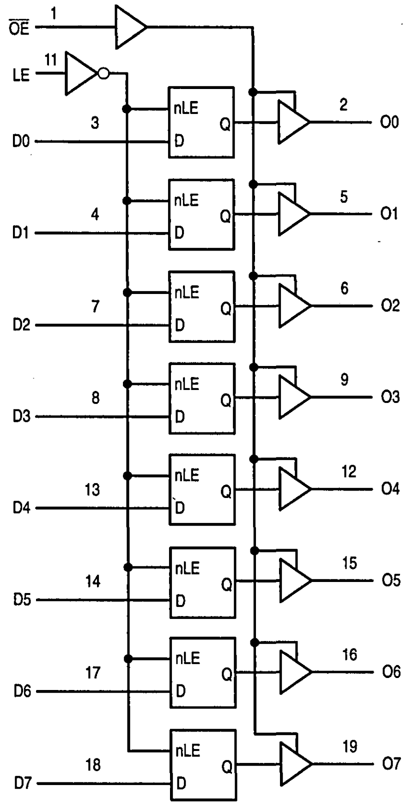
Pinout: 20–Lead (Top View)



PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
LE	Latch Enable Input
D0–D7	Data Inputs
O0–O7	3–State Latch Outputs

LOGIC DIAGRAM



INPUTS			INTERNAL LATCHES	OUTPUTS	OPERATING MODE
$\overline{OE}$	LE	Dn	Q	On	
L L	H H	H L	H L	H L	Transparent (Latch Disabled); Read Latch
L L	↓ ↓	h l	H L	H L	Latched (Latch Enabled) Read Latch
L	L	X	NC	NC	Hold; Read Latch
H	L	X	NC	Z	Hold; Disabled Outputs
H H	H H	H L	H L	Z Z	Transparent (Latch Disabled); Disabled Outputs
H H	↓ ↓	h l	H L	Z Z	Latched (Latch Enabled); Disabled Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable High–to–Low Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable High–to–Low Transition; NC = No Change; X = High or Low Voltage Level or Transitions are Acceptable; Z = High Impedance State; ↓ = High–to–Low Transition; For I_{CC} Reasons DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.
1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage — (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	V_{CC} – 0.2		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	μA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	μA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	μA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	μA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	μA

AC CHARACTERISTICS ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits				Unit
			T_A = –40°C to +85°C				
			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Dn to On	1	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to On	3	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH and LOW Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time from HIGH and LOW Level	2	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_s	Setup Time, HIGH or LOW Dn to LE	3	2.5		2.5		ns
t_h	Hold Time, HIGH or LOW Dn to LE	3	1.5		1.5		ns
t_w	LE Pulse Width, HIGH	3	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1)			1.0 1.0			ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

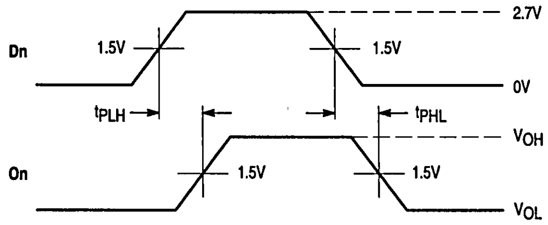
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

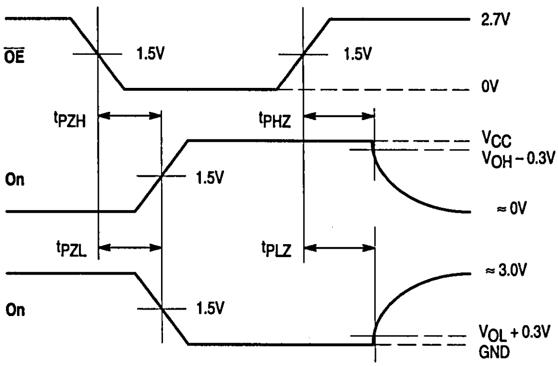
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

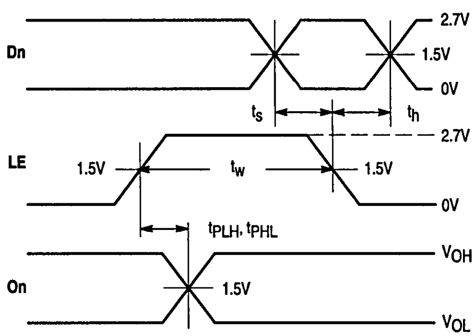
Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, V_I = 0V or V_{CC}	8	pF



WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

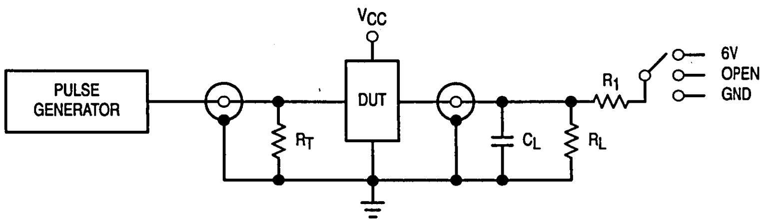


WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns



WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns except when noted

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

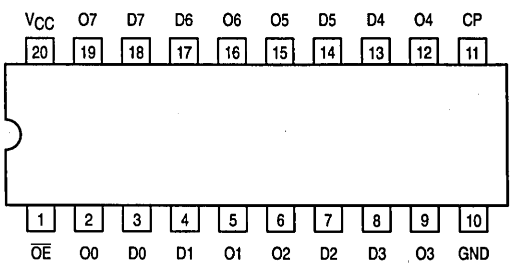
Low-Voltage CMOS Octal D-Type Flip-Flop
With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX374 is a high performance, non–inverting octal D–type flip–flop operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX374 inputs to be safely driven from 5V devices.

The MC74LCX374 consists of 8 edge–triggered flip–flops with individual D–type inputs and 3–state true outputs. The buffered clock and buffered Output Enable ($\overline{OE}$) are common to all flip–flops. The eight flip–flops will store the state of individual D inputs that meet the setup and hold time requirements on the LOW–to–HIGH Clock (CP) transition. With the $\overline{OE}$ LOW, the contents of the eight flip–flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. The $\overline{OE}$ input level does not affect the operation of the flip–flops.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

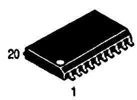
Pinout: 20–Lead (Top View)



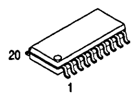
MC74LCX374

LCX

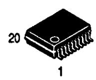
LOW–VOLTAGE CMOS
OCTAL D–TYPE FLIP–FLOP



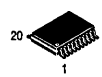
DW SUFFIX
PLASTIC SOIC
CASE 751D–04



M SUFFIX
PLASTIC SOIC EIAJ
CASE 967–01



SD SUFFIX
PLASTIC SSOP
CASE 940C–03

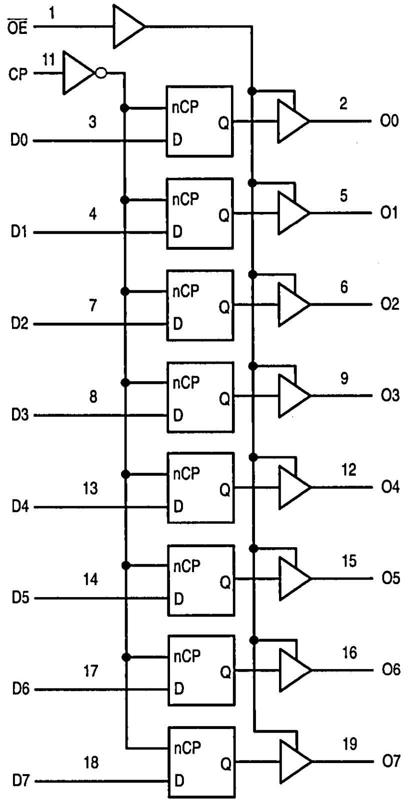


DT SUFFIX
PLASTIC TSSOP
CASE 948E–02

PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
CP	Clock Pulse Input
D0–D7	Data Inputs
O0–O7	3–State Outputs

LOGIC DIAGRAM



INPUTS			INTERNAL LATCHES	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	Q	On	
L L	↑ ↑	l h	L H	L H	Load and Read Register
L	‡	X	NC	NC	Hold and Read Register
H	‡	X	NC	Z	Hold and Disable Outputs
H H	↑ ↑	l h	L H	Z Z	Load Internal Register and Disable Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; NC = No Change; X = High or Low Voltage Level and Transitions are Acceptable; Z = High Impedance State; ↑ = Low–to–High Transition; ‡ = Not a Low–to–High Transition; For I_{CC} Reasons DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V				–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V				24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V				–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V				12	mA
T_A	Operating Free–Air Temperature		–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V		0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	$T_A = -40°C$ to $+85°C$		Unit
			Min	Max	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits				Unit
			$T_A = -40°C$ to $+85°C$				
			$V_{CC} = 3.0V$ to $3.6V$		$V_{CC} = 2.7V$		
			Min	Max	Min	Max	
f_{max}	Clock Pulse Frequency	1	150				MHz
t_{PLH} t_{PHL}	Propagation Delay CP to On	1	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH and LOW Levels	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time from HIGH and LOW Levels	2	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_s	Setup Time, HIGH or LOW Dn to CP	1	2.5		2.5		ns
t_h	Hold Time, HIGH or LOW Dn to CP	1	1.5		1.5		ns
t_w	CP Pulse Width, HIGH or LOW	3	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1)			1.0 1.0			ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

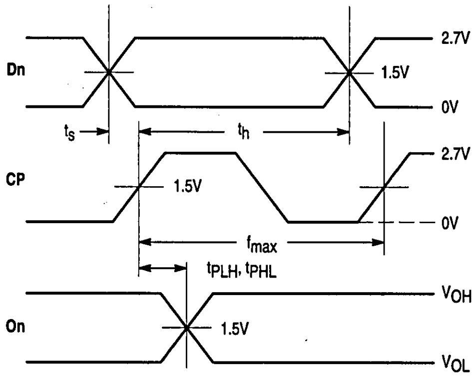
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25°C$			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

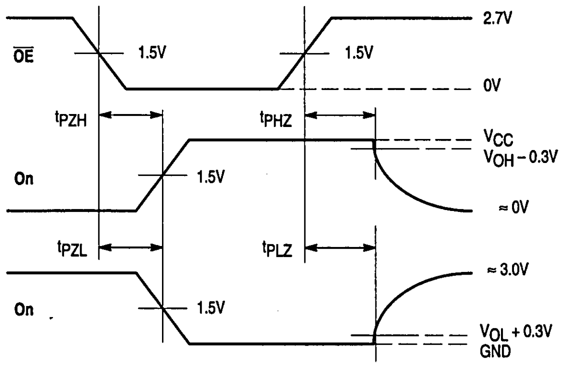
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

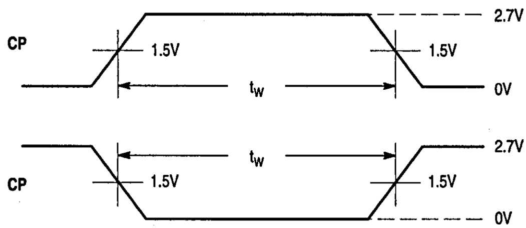
Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	25	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF



WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

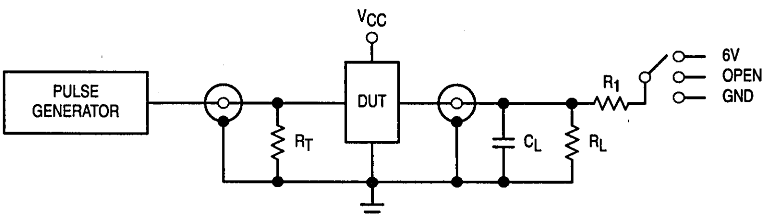


WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns



WAVEFORM 3 – PULSE WIDTH
$t_R = t_F$ = 2.5ns (or fast as required) from 10% to 90%;
Output requirements: $V_{OL} \le 0.8V$, $V_{OH} \ge 2.0V$

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Low-Voltage CMOS Octal Buffer Flow Through Pinout

With 5V-Tolerant Inputs and Outputs (3-State, Inverting)

MC74LCX540

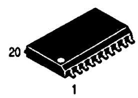
LCX

LOW–VOLTAGE CMOS OCTAL BUFFER

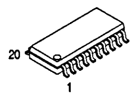
The MC74LCX540 is a high performance, inverting octal buffer operating from a 2.7 to 3.6V supply. This device is similar in function to the MC74LCX240, while providing flow through architecture. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX540 inputs to be safely driven from 5V devices. The MC74LCX540 is suitable for memory address driving and all TTL level bus oriented buffer applications.

Current drive capability is 24mA at the outputs. The Output Enable ($\overline{OE1}$, $\overline{OE2}$) inputs, when HIGH, disables the outputs by placing them in a HIGH Z condition.

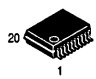
- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



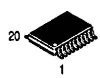
DW SUFFIX
PLASTIC SOIC
CASE 751D–04



M SUFFIX
PLASTIC SOIC EIAJ
CASE 967–01

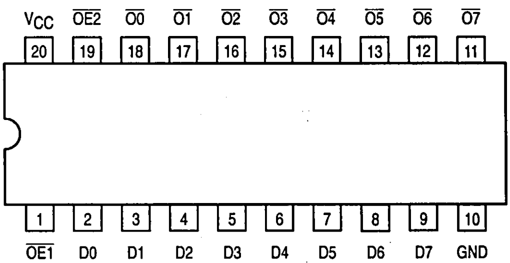


SD SUFFIX
PLASTIC SSOP
CASE 940C–03



DT SUFFIX
PLASTIC TSSOP
CASE 948E–02

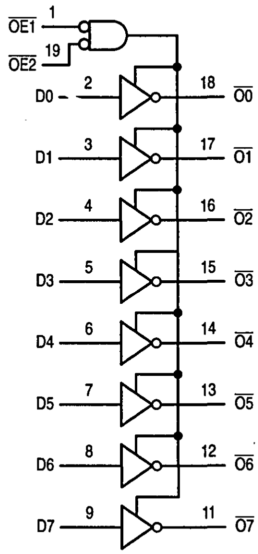
Pinout: 20–Lead (Top View)



PIN NAMES

Pins	Function
$\overline{OEn}$	Output Enable Inputs
Dn	Data Inputs
$\overline{On}$	3–State Outputs

LOGIC DIAGRAM



INPUTS			OUTPUTS
$\overline{OE1}$	$\overline{OE2}$	Dn	$\overline{On}$
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V				–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V				24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V				–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V				12	mA
T_A	Operating Free–Air Temperature		–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V		0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
I_I	Input Leakage Current	2.7V ≤ V_{CC} ≤ 3.6V; 0V ≤ V_I ≤ 5.5V		±5.0	μA
I_{OZ}	3–State Output Current	2.7 ≤ V_{CC} ≤ 3.6V; 0V ≤ V_O ≤ 5.5V; V_I = V_{IH} or V_{IL}		±5.0	μA
I_{OFF}	Power–Off Leakage Current	V_{CC} = 0V; V_I or V_O = 5.5V		10	μA
I_{CC}	Quiescent Supply Current	2.7 ≤ V_{CC} ≤ 3.6V; V_I = GND or V_{CC}		10	μA
		2.7 ≤ V_{CC} ≤ 3.6V; 3.6 ≤ V_I or V_O ≤ 5.5V		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	2.7 ≤ V_{CC} ≤ 3.6V; V_{IH} = V_{CC} – 0.6V		500	μA

AC CHARACTERISTICS (t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Waveform	Limits			Unit
			T_A = –40°C to +85°C			
			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V	
			Min	Max	Max	
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	6.5 6.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	8.5 8.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	7.5 7.5	8.5 8.5	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1)			1.0 1.0		ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

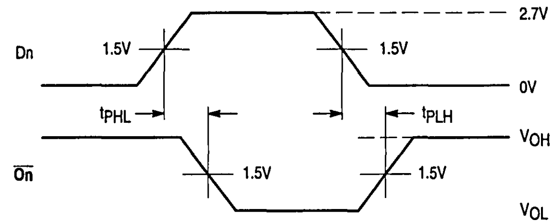
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V

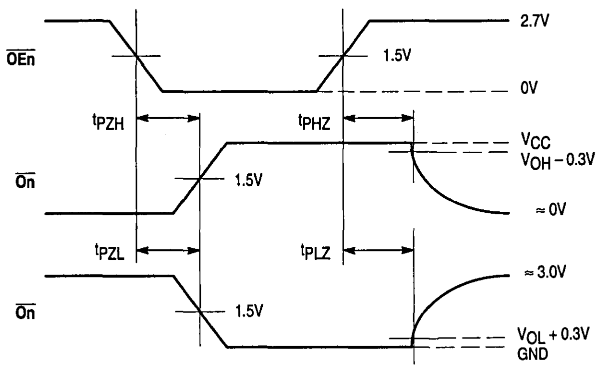
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF

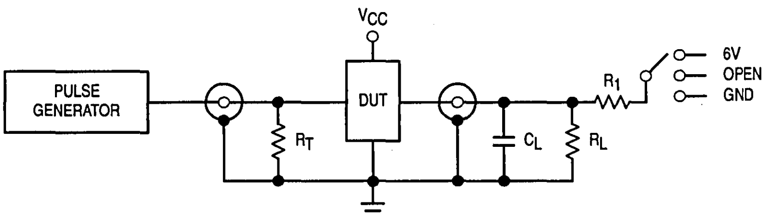


WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Low-Voltage CMOS Octal Buffer Flow Through Pinout
With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX541

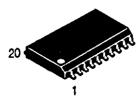
LCX

LOW–VOLTAGE CMOS OCTAL BUFFER

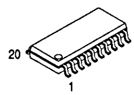
The MC74LCX541 is a high performance, non–inverting octal buffer operating from a 2.7 to 3.6V supply. This device is similar in function to the MC74LCX244, while providing flow through architecture. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX541 inputs to be safely driven from 5V devices. The MC74LCX541 is suitable for memory address driving and all TTL level bus oriented buffer applications.

Current drive capability is 24mA at the outputs. The Output Enable ($\overline{OE1}$. $\overline{OE2}$) inputs, when HIGH, disables the output by placing them in a HIGH Z condition.

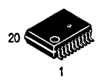
- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



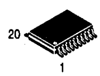
DW SUFFIX
PLASTIC SOIC
CASE 751D–04



M SUFFIX
PLASTIC SOIC EIAJ
CASE 967–01

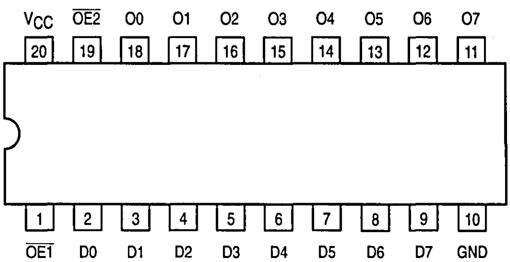


SD SUFFIX
PLASTIC SSOP
CASE 940C–03



DT SUFFIX
PLASTIC TSSOP
CASE 948E–02

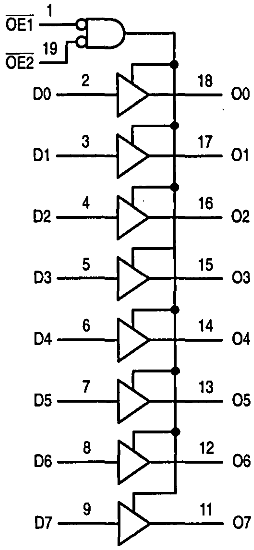
Pinout: 20–Lead (Top View)



PIN NAMES

Pins	Function
$\overline{OEn}$	Output Enable Inputs
Dn	Data Inputs
On	3–State Outputs

LOGIC DIAGRAM



INPUTS			OUTPUTS
$\overline{OE1}$	$\overline{OE2}$	Dn	On
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage — (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	V_{CC} = 0V; V_I or V_O = 5.5V		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS ($t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω)

			Limits			
			T_A = –40°C to +85°C			
			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V	
Symbol	Parameter	Waveform	Min	Max	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	6.5 6.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	8.5 8.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	7.5 7.5	8.5 8.5	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1)			1.0 1.0		ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

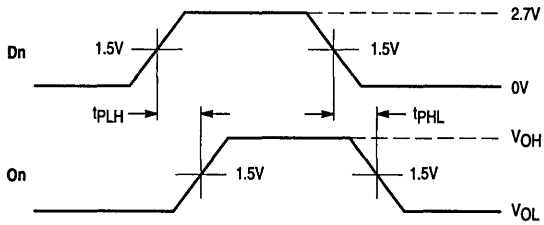
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C Min	Typ	Max	Unit
V_{OLP}	Dynamic LOW Peak Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V

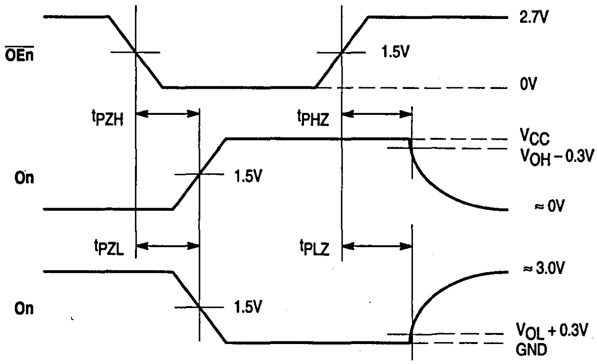
1. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF

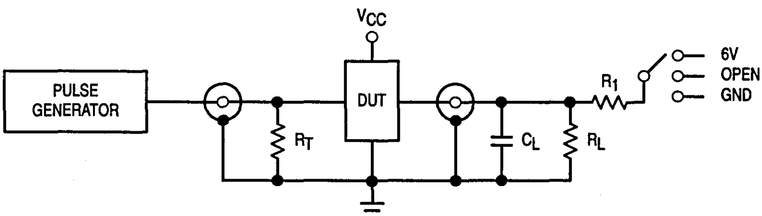


WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Product Preview

Low-Voltage CMOS Octal Latching Transceiver

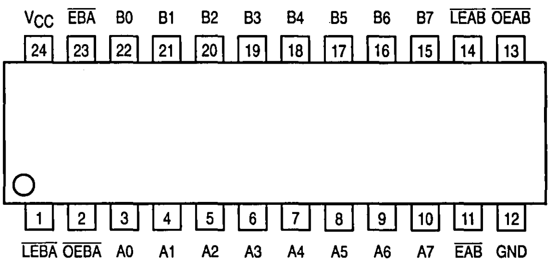
With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX543 is a high performance, non–inverting octal latching transceiver operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX543 inputs to be safely driven from 5V devices. The MC74LCX543 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

For data flow from A to B with the $\overline{EAB}$ LOW, the A–to–B Output Enable ($\overline{OEAB}$) must be LOW in order to enable data to the B bus, as indicated in the Function Table. With $\overline{EAB}$ LOW, a LOW signal on the A–to–B Latch Enable ($\overline{LEAB}$) input makes the A–to–B latches transparent; a subsequent LOW–to–HIGH transition of the $\overline{LEAB}$ signal will latch the A latches, and the outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both LOW, the 3–State B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is symetric to that above, but uses the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

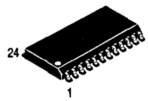
Pinout: 24–Lead Package (Top View)



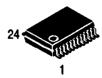
MC74LCX543

LCX

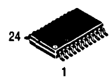
LOW–VOLTAGE CMOS OCTAL LATCHING TRANSCEIVER



DW SUFFIX
PLASTIC SOIC
CASE 751E–04



SD SUFFIX
PLASTIC SSOP
CASE 940D–03



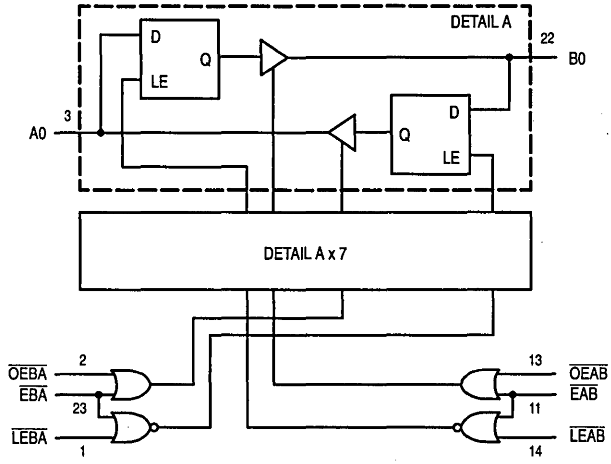
DT SUFFIX
PLASTIC TSSOP
CASE 948H–01

PIN NAMES

Pins	Function
$\overline{OExx}$	Output Enable Inputs
$\overline{Exx}$	Enable Inputs
$\overline{LExx}$	Latch Enable Inputs
A0–A7	3–State Inputs/Outputs
B0–B7	3–State Inputs/Outputs

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

LOGIC DIAGRAM



FUNCTION TABLE

Inputs								Internal Latch		Outputs		
An	$\overline{OEAB}$	$\overline{EAB}$	$\overline{LEAB}$	Bn	$\overline{OEBA}$	$\overline{EBA}$	$\overline{LEBA}$	QABn	QBAn	A0–A7	B0–B7	Operating Mode
h	L	L	↑	U	H	X	X	H	X	NA	H	Latch & Display B Outputs
l	L	L	↑	U	H	X	X	L	X	NA	L	
X	L	L	H	U	H	X	X	NC	X	NA	NC	Hold, Read B Outputs
h	L	↑	L	X	H	X	X	H	H	NA	Z	Latch and B Outputs Disabled
l	L	↑	L	X	H	X	X	L	L	NA	Z	
h	H	L	↑	X	H	X	X	H	X	NA	Z	
l	H	L	↑	X	H	X	X	L	X	NA	Z	
H	L	L	L	U	H	X	X	H	X	NA	H	Transparent A to B
L	L	L	L	U	H	X	X	L	X	NA	L	
X	H	X	X	X	H	X	X	X	X	NA	Z	Disable B Outputs
X	X	H	X	X	H	X	X	NC	X	NA	Z	
U	H	X	X	h	L	L	↑	X	H	H	NA	Latch & Display A Outputs
U	H	X	X	l	L	L	↑	X	L	L	NA	
U	H	X	X	X	L	L	H	X	NC	NC	NA	Hold, Read A Outputs
X	H	X	X	h	L	↑	L	H	H	Z	NA	Latch and A Outputs Disabled
X	H	X	X	l	L	↑	L	L	L	Z	NA	
X	H	X	X	h	H	L	↑	X	H	Z	NA	
X	H	X	X	l	H	L	↑	X	L	Z	NA	
U	H	X	X	X	L	L	L	X	H	H	NA	Transparent B to A
U	H	X	X	L	L	L	L	X	L	L	NA	
X	H	X	X	X	H	X	X	X	X	Z	NA	Enable A Outputs
X	H	X	X	X	X	H	X	X	NC	Z	NA	

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable or Enable Low–to–High Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable or Enable Low–to–High Transition; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable; NC = No Change; ↑ = Low–to–High Transition; U = Undriven

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
V_O	DC Output Voltage	$-0.5 \leq V_O \leq +7.0$	Output in 3–State	V
		$-0.5 \leq V_O \leq V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage — (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \leq V_{CC} \leq 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \leq V_{CC} \leq 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \leq V_{CC} \leq 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \leq V_{CC} \leq 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \geq 2.4V$, $V_{IL} \leq 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS[1] ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits				Unit
			T_A = –40°C to +85°C				
			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay An to Bn or Bn to An	1	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to An or $\overline{LEAB}$ to Bn	4	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn	2	1.5 1.5	9.0 9.0	1.5 1.5	10.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn	2	1.5 1.5	7.0 7.0	1.5 1.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{EBA}$ to An or $\overline{EAB}$ to Bn	2	1.5 1.5	9.0 9.0	1.5 1.5	10.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{EBA}$ to An or $\overline{EAB}$ to Bn	2	1.5 1.5	7.0 7.0	1.5 1.5	7.5 7.5	ns
t_s	Setup Time, HIGH to LOW Data to $\overline{LExx}$	4	2.5		2.5		ns
t_h	Hold Time, HIGH to LOW Data to $\overline{LExx}$	4	1.5		1.5		ns
t_s	Setup Time, HIGH to LOW Data to $\overline{Exx}$	4	2.5		2.5		ns
t_h	Hold Time, HIGH to LOW Data to $\overline{Exx}$	4	1.5		1.5		ns
t_w	Latch Enable or Enable Pulse Width, LOW	4	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0			ns

1. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

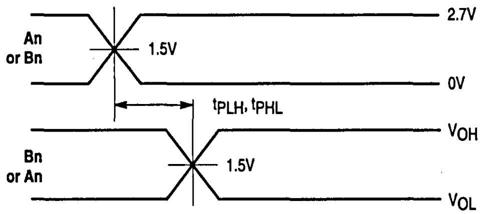
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

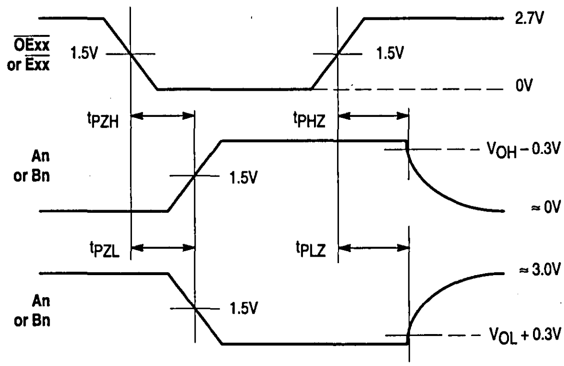
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF

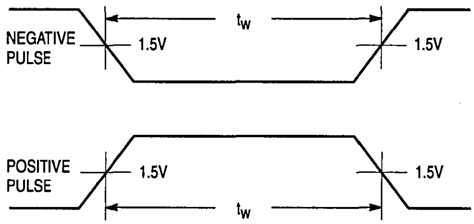


WAVEFORM 1 – A/B to B/A PROPAGATION DELAYS
t_R = t_F = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

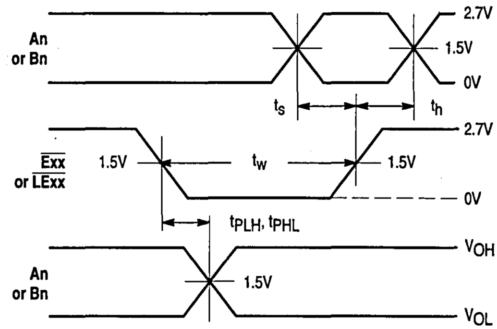


WAVEFORM 2 – $\overline{OExx}$/$\overline{Exx}$ to A or B OUTPUT ENABLE AND DISABLE TIMES
t_R = t_F = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

Figure 1. AC Waveforms

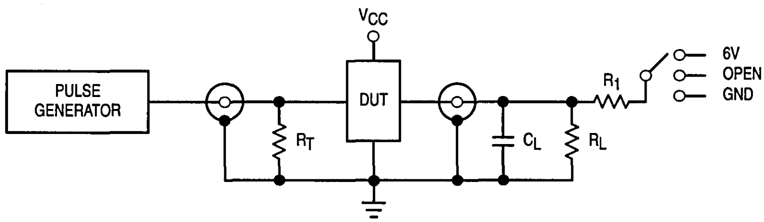


WAVEFORM 3 – INPUT PULSE DEFINITION
$t_R = t_F = 2.5ns$, 10% to 90% of 0V to 2.7V



WAVEFORM 4 – Enable to A or B PROPAGATION DELAYS, Enable MINIMUM PULSE WIDTH, A or B to Enable SETUP AND HOLD TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; t_W = 500ns except when noted

Figure 2. AC Waveforms (continued)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 3. Test Circuit

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Low-Voltage CMOS Octal Transparent Latch Flow Through Pinout
With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX573

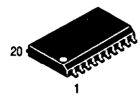
LCX

LOW–VOLTAGE CMOS OCTAL TRANSPARENT LATCH

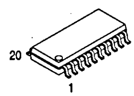
The MC74LCX573 is a high performance, non–inverting octal transparent latch operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX573 inputs to be safely driven from 5V devices.

The MC74LCX573 contains 8 D–type latches with 3–state standard outputs. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH–to–LOW transition of LE. The 3–state standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are enabled. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches. The LCX573 flow through design facilitates easy PC board layout.

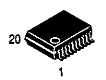
- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



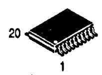
DW SUFFIX
PLASTIC SOIC
CASE 751D–04



M SUFFIX
PLASTIC SOIC EIAJ
CASE 967–01

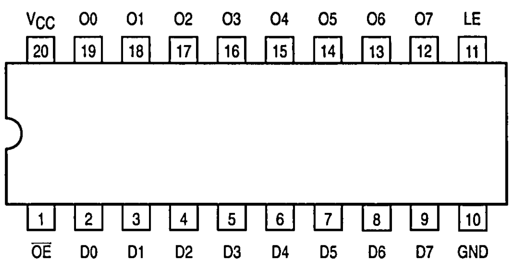


SD SUFFIX
PLASTIC SSOP
CASE 940C–03



DT SUFFIX
PLASTIC TSSOP
CASE 948E–02

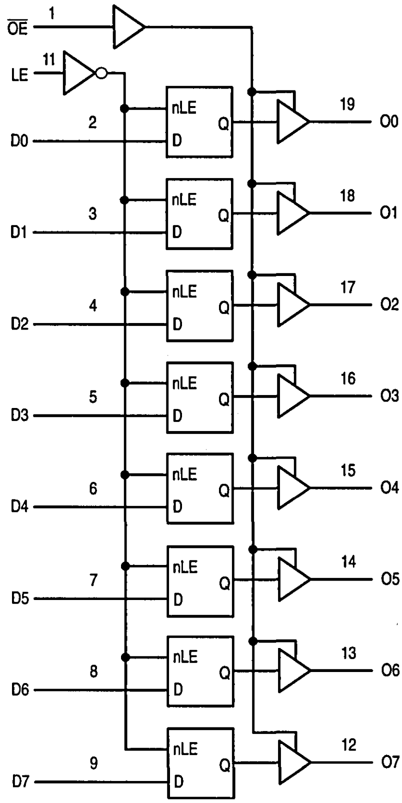
Pinout: 20–Lead (Top View)



PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
LE	Latch Enable Input
D0–D7	Data Inputs
O0–O7	3–State Latch Outputs

LOGIC DIAGRAM



INPUTS			INTERNAL LATCHES	OUTPUTS	OPERATING MODE
$\overline{OE}$	LE	Dn	Q	On	
L L	H H	H L	H L	H L	Transparent (Latch Disabled); Read Latch
L L	↓ ↓	h l	H L	H L	Latched (Latch Enabled) Read Latch
L	L	X	NC	NC	Hold; Read Latch
H	L	X	NC	Z	Hold; Disabled Outputs
H H	H H	H L	H L	Z Z	Transparent (Latch Disabled); Disabled Outputs
H H	↓ ↓	h l	H L	Z Z	Latched (Latch Enabled); Disabled Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable High–to–Low Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable High–to–Low Transition; NC = No Change; X = High or Low Voltage Level and Transitions are Acceptable; Z = High Impedance State; ↓ = High–to–Low Transition; For I_{CC} Reasons DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	$V_I <$ GND	mA
I_{OK}	DC Output Diode Current	–50	$V_O <$ GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage — (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

			T_A = –40°C to +85°C		
Symbol	Characteristic	Condition	Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	$T_A = -40°C$ to $+85°C$ Min	Max	Unit
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; $V_I = GND$ or V_{CC}		10	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits, $T_A = -40°C$ to $+85°C$, $V_{CC} = 3.0V$ to $3.6V$ Min	Max	$V_{CC} = 2.7V$ Min	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Dn to On	1	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to On	3	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH and LOW Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time from HIGH and LOW Level	2	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t_s	Setup Time, HIGH or LOW Dn to LE	3	2.5		2.5		ns
t_h	Hold Time, HIGH or LOW Dn to LE	3	1.5		1.5		ns
t_w	LE Pulse Width, HIGH	3	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1)			1.0 1.0			ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

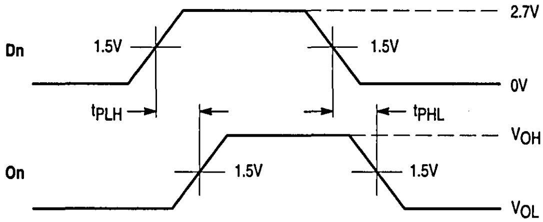
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25°C$ Min	Typ	Max	Unit
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

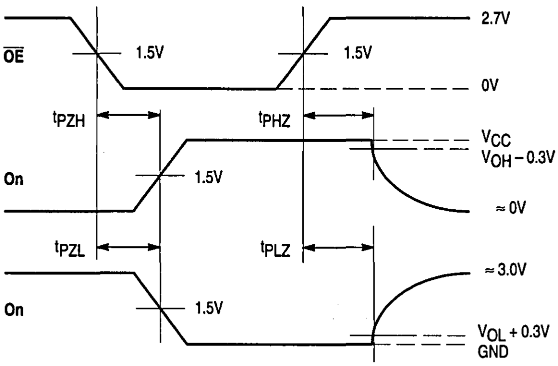
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

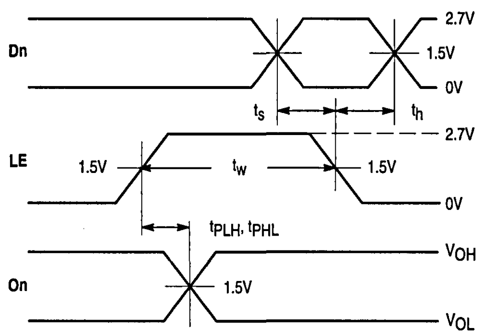
Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	25	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF



WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

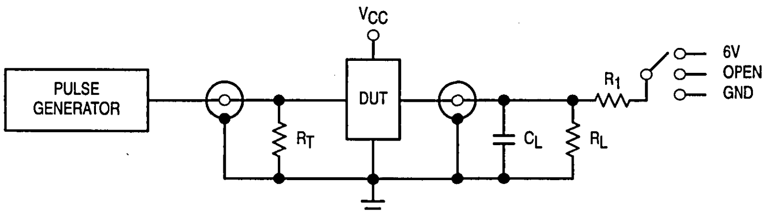


WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$ except when noted

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Low-Voltage CMOS Octal D-Type Flip-Flop Flow Through Pinout

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX574

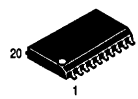
LCX

LOW–VOLTAGE CMOS OCTAL D–TYPE FLIP–FLOP

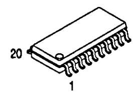
The MC74LCX574 is a high performance, non–inverting octal D–type flip–flop operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX574 inputs to be safely driven from 5V devices.

The MC74LCX574 consists of 8 edge–triggered flip–flops with individual D–type inputs and 3–state true outputs. The buffered clock and buffered Output Enable ($\overline{OE}$) are common to all flip–flops. The eight flip–flops will store the state of individual D inputs that meet the setup and hold time requirements on the LOW–to–HIGH Clock (CP) transition. With the $\overline{OE}$ LOW, the contents of the eight flip–flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. The $\overline{OE}$ input level does not affect the operation of the flip–flops. The LCX574 flow through design facilitates easy PC board layout.

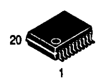
- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



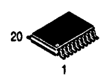
DW SUFFIX
PLASTIC SOIC
CASE 751D–04



M SUFFIX
PLASTIC SOIC EIAJ
CASE 967–01

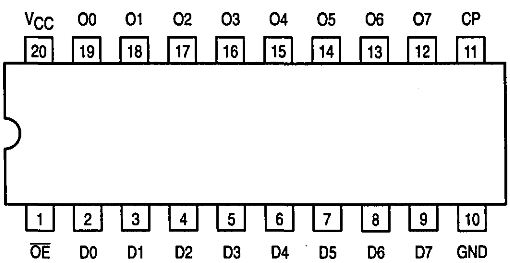


SD SUFFIX
PLASTIC SSOP
CASE 940C–03



DT SUFFIX
PLASTIC TSSOP
CASE 948E–02

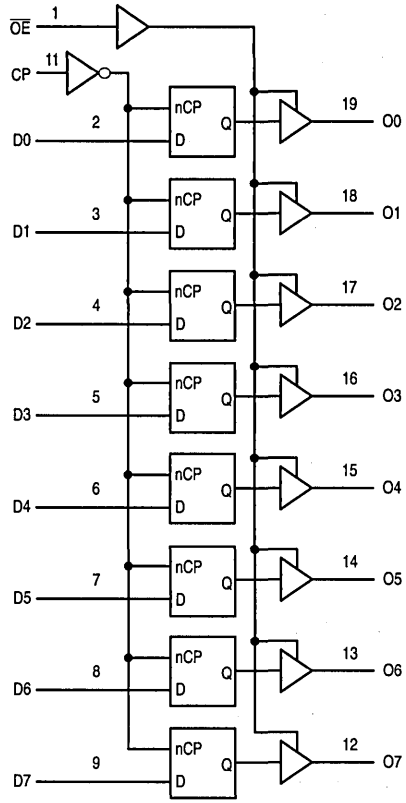
Pinout: 20–Lead (Top View)



PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
CP	Clock Pulse Input
D0–D7	Data Inputs
O0–O7	3–State Outputs

LOGIC DIAGRAM



INPUTS			INTERNAL LATCHES	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	Q	On	
L L	↑ ↑	l h	L H	L H	Load and Read Register
L	‡	X	NC	NC	Hold and Read Register
H	‡	X	NC	Z	Hold and Disable Outputs
H H	↑ ↑	l h	L H	Z Z	Load Internal Register and Disable Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; NC = No Change; X = High or Low Voltage Level and Transitions are Acceptable; Z = High Impedance State; ↑ = Low–to–High Transition; ‡ = Not a Low–to–High Transition; For I_{CC} Reasons DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V				–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V				24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V				–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V				12	mA
T_A	Operating Free–Air Temperature		–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V		0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL}= 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
I_I	Input Leakage Current	2.7V ≤ V_{CC} ≤ 3.6V; 0V ≤ V_I ≤ 5.5V		±5.0	µA
I_{OZ}	3–State Output Current	2.7 ≤ V_{CC} ≤ 3.6V; 0V ≤ V_O ≤ 5.5V; V_I = V_{IH} or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	V_{CC} = 0V; V_I or V_O = 5.5V		10	µA
I_{CC}	Quiescent Supply Current	2.7 ≤ V_{CC} ≤ 3.6V; V_I = GND or V_{CC}		10	µA
		2.7 ≤ V_{CC} ≤ 3.6V; 3.6 ≤ V_I or V_O ≤ 5.5V		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	2.7 ≤ V_{CC} ≤ 3.6V; V_{IH} = V_{CC} – 0.6V		500	µA

AC CHARACTERISTICS (t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Waveform	Limits				Unit
			T_A = –40°C to +85°C				
			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V		
			Min	Max	Min	Max	
f_{max}	Clock Pulse Frequency	1	150				MHz
t_{PLH} t_{PHL}	Propagation Delay CP to On	1	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH and LOW Levels	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time from HIGH and LOW Levels	2	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t_s	Setup Time, HIGH or LOW Dn to CP	1	2.5		2.5		ns
t_h	Hold Time, HIGH or LOW Dn to CP	1	1.5		1.5		ns
t_w	CP Pulse Width, HIGH or LOW	3	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1)			1.0 1.0			ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

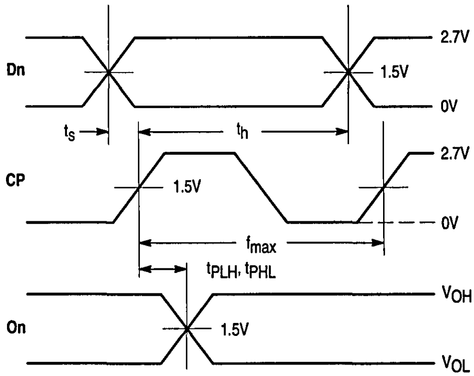
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V

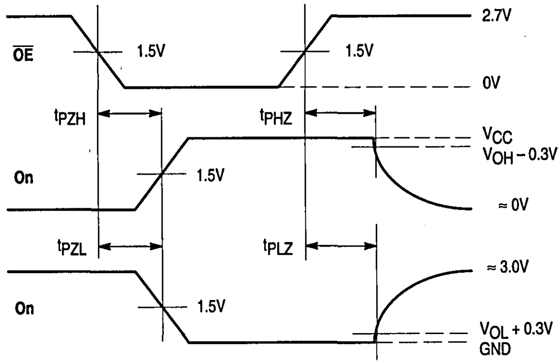
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

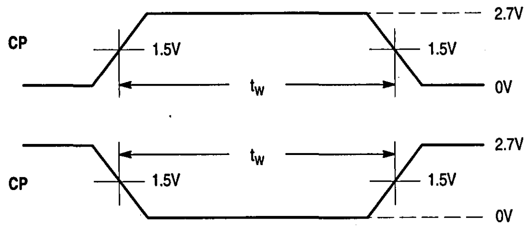
Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF



WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

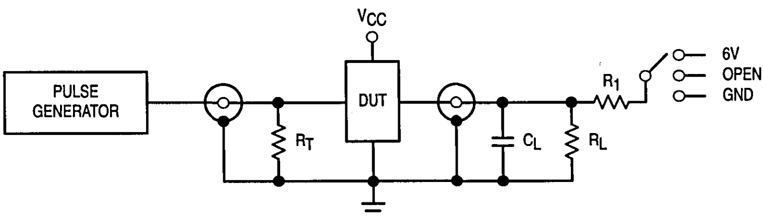


WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



WAVEFORM 3 – PULSE WIDTH
$t_R = t_F = 2.5ns$ (or fast as required) from 10% to 90%;
Output requirements: $V_{OL} \leq 0.8V$, $V_{OH} \geq 2.0V$

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Product Preview

Low-Voltage CMOS Octal Transceiver/Registered Transceiver

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

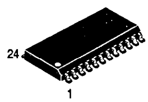
MC74LCX646

LCX

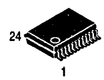
LOW–VOLTAGE CMOS OCTAL TRANSCEIVER/ REGISTERED TRANSCEIVER

The MC74LCX646 is a high performance, non–inverting octal transceiver/registered transceiver operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX646 inputs to be safely driven from 5V devices. The MC74LCX646 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

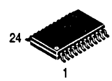
Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes from a LOW–to–HIGH logic level. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver outputs. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls (SBA, SAB) can multiplex stored and real–time (transparent mode) data. The direction control (DIR) determines which bus will receive data when the enable $\overline{OE}$ is active LOW. In the isolation mode ($\overline{OE}$ HIGH), A data may be stored in the B register or B data may be stored in the A register. Only one of the two buses, A or B, may be driven at one time.



DW SUFFIX
PLASTIC SOIC
CASE 751E–04



SD SUFFIX
PLASTIC SSOP
CASE 940D–03

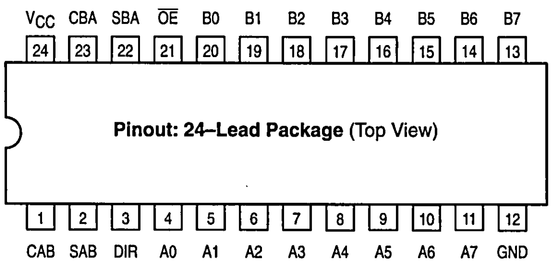


DT SUFFIX
PLASTIC TSSOP
CASE 948H–01

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

PIN NAMES

Pins	Function
A0–A7	Side A Inputs/Outputs
B0–B7	Side B Inputs/Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Select Control Inputs
DIR, $\overline{OE}$	Output Enable Inputs



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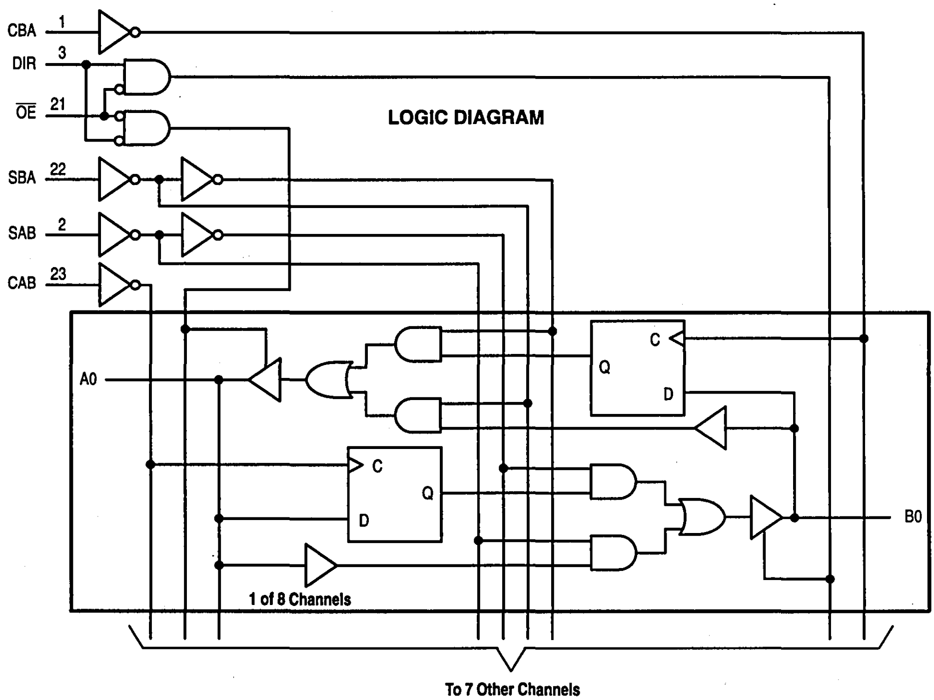
LOGIC DIAGRAM



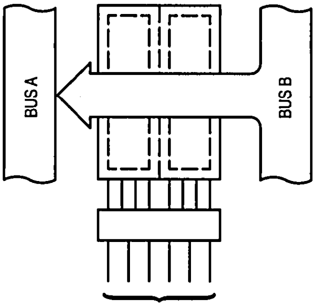
FUNCTION TABLE

Inputs						Storage Registers		Data Ports		Operating Mode
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	Q_A	Q_B	A_n	B_n	Operating Mode
H	X							Input	Input	
		‡	‡	X	X	NC	NC	X	X	Isolation, Hold Storage
		↑	↑	X	X	L H X X	X X L H	L H X X	X X L H	Store A and/or B Data
L	H							Input	Output	
		‡	X*	L	X	NC NC	NC NC	L H	L H	Real Time A Data to B Bus
				H	X	NC	NC	X	Q_A	Stored A Data to B Bus
		↑	X*	L	X	L H	NC NC	L H	L H	Real Time A Data to B Bus; Store A Data
				H	X	L H	NC NC	L H	Q_A Q_A	Stored A Data to B Bus; Store A Data
L	L							Output	Input	
		X*	‡	X	L	NC NC	NC NC	L H	L H	Real Time B Data to A Bus
				X	H	NC	NC	Q_B	X	Stored B Data to A Bus
		X*	↑	X	L	NC NC	L H	L H	L H	Real Time B Data to A Bus; Store B Data
				X	H	NC NC	L H	Q_B Q_B	L H	Stored B Data to A Bus; Store B Data

H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = Low–to–High Clock Transition; ‡ = NOT Low–to–High Clock Transition; NC = No Change; * = The clocks are not internally gated with either the Output Enables or the Source Inputs. Therefore, data at the A or B ports may be clocked into the storage registers, at any time. For I_{CC} reasons, Do Not Float Inputs.

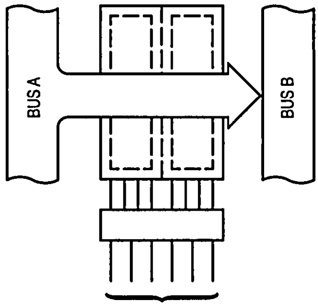
BUS APPLICATIONS

Real Time Transfer – Bus B to Bus A



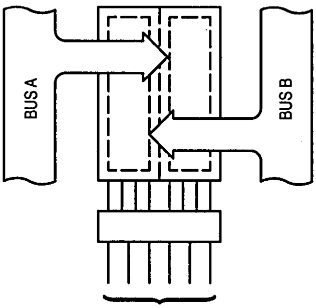
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

Real Time Transfer – Bus A to Bus B



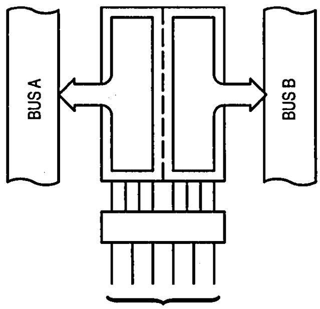
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

Store Data from Bus A, Bus B or Busses A and B



$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Transfer Storage Data to Bus A or Bus B



$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	$T_A = -40°C$ to $+85°C$		Unit
			Min	Max	
I_I	Input Leakage Current	$2.7V \leq V_{CC} \leq 3.6V$; $0V \leq V_I \leq 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \leq V_{CC} \leq 3.6V$; $0V \leq V_O \leq 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \leq V_{CC} \leq 3.6V$; V_I = GND or V_{CC}		10	µA
		$2.7 \leq V_{CC} \leq 3.6V$; $3.6 \leq V_I$ or $V_O \leq 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \leq V_{CC} \leq 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS[1] ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits $T_A = -40°C$ to $+85°C$				Unit
			$V_{CC} = 3.0V$ to $3.6V$		$V_{CC} = 2.7V$		
			Min	Max	Min	Max	
f_{max}	Clock Pulse Frequency	3	150				MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	3	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay Select to Output	1	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_s	Setup Time, HIGH or LOW Data to Clock	3	2.5		2.5		ns
t_h	Hold Time, HIGH or LOW Data to Clock	3	1.5		1.5		ns
t_w	Clock Pulse Width, HIGH or LOW	3	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0			ns

1. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

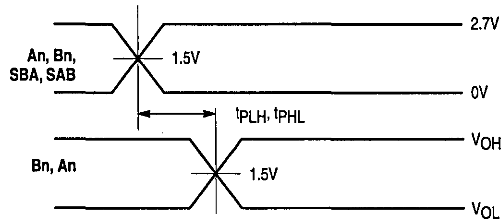
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25°C$			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

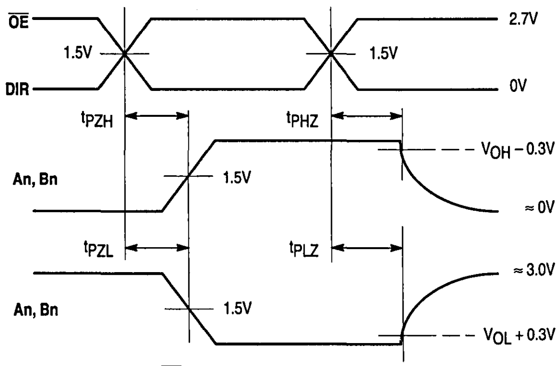
1. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF

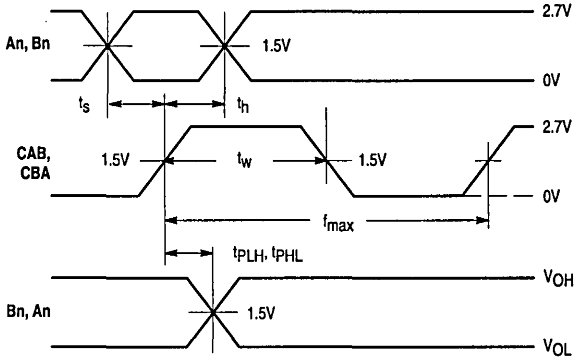


WAVEFORM 1 – SAB to B and SBA to A, An to Bn PROPAGATION DELAYS
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

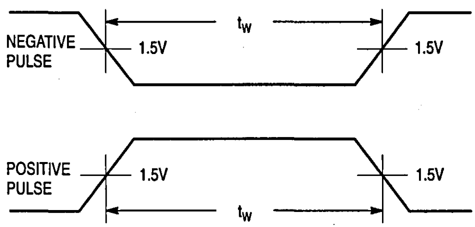


WAVEFORM 2 – $\overline{\text{OE}}$/DIR to An/Bn OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

Figure 1. AC Waveforms

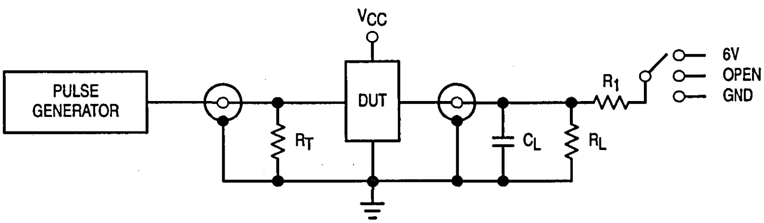


WAVEFORM 3 – CLOCK to Bn/An PROPAGATION DELAYS, CLOCK MINIMUM PULSE WIDTH, An/Bn to CLOCK SETUP AND HOLD TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$ except when noted



WAVEFORM 4 – INPUT PULSE DEFINITION
$t_R = t_F = 2.5ns$, 10% to 90% of 0V to 2.7V

Figure 2. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 3. Test Circuit

Product Preview

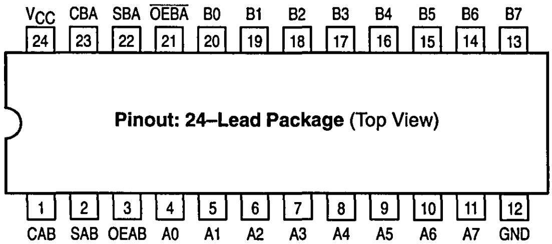
Low-Voltage CMOS Octal Transceiver/Registered Transceiver With Dual Enable

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX652 is a high performance, non–inverting octal transceiver/registered transceiver operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX652 inputs to be safely driven from 5V devices. The MC74LCX652 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes from a LOW–to–HIGH logic level. Two Output Enable pins ($\overline{OEBA}$, OEAB) are provided to control the transceiver outputs. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls (SBA, SAB) can multiplex stored and real–time (transparent mode) data. In the isolation mode (both outputs disabled), A data may be stored in the B register or B data may be stored in the A register. When in the real–time mode, it is possible to store data without using the internal registers by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input (data retention is not guaranteed in this mode).

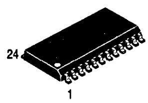
- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



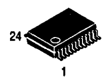
MC74LCX652

LCX

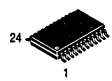
LOW–VOLTAGE CMOS OCTAL TRANSCEIVER/ REGISTERED TRANSCEIVER WITH DUAL ENABLE



DW SUFFIX
PLASTIC SOIC
CASE 751E–04



SD SUFFIX
PLASTIC SSOP
CASE 940D–03



DT SUFFIX
PLASTIC TSSOP
CASE 948H–01

PIN NAMES

Pins	Function
A0–A7	Side A Inputs/Outputs
B0–B7	Side B Inputs/Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Select Control Inputs
$\overline{OEBA}$, OEAB	Output Enable Inputs

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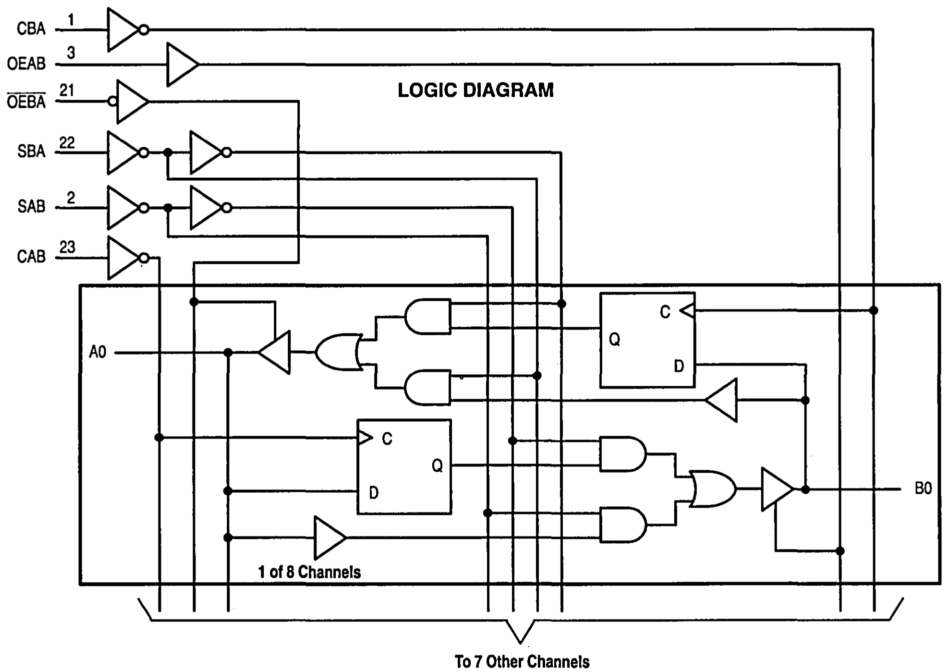
LOGIC DIAGRAM



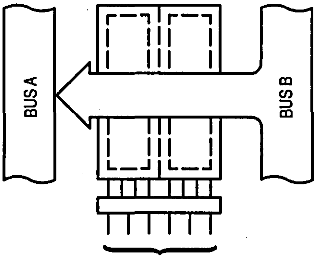
FUNCTION TABLE

Inputs						Storage Registers		Data Ports		Operating Mode
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA	Q_A	Q_B	A_n	B_n	
L	H							Input	Input	
		↕	↕	X	X	NC	NC	X	X	Isolation, Hold Storage
		↑	↑	X	X	L H X X	X X L H	L H X X	X X L H	Store A and/or B Data
H	H							Input	Output	
		↕	X*	L	X	NC NC	NC NC	L H	L H	Real Time A Data to B Bus
				H	X	NC	NC	X	Q_A	Stored A Data to B Bus
		↑	X*	L	X	L H	NC NC	L H	L H	Real Time A Data to B Bus; Store A Data
				H	X	L H	NC NC	L H	Q_A Q_A	Stored A Data to B Bus; Store A Data
L	L							Output	Input	
		X*	↕	X	L	NC NC	NC NC	L H	L H	Real Time B Data to A Bus
				X	H	NC	NC	Q_B	X	Stored B Data to A Bus
		X*	↑	X	L	NC NC	L H	L H	L H	Real Time B Data to A Bus; Store B Data
				X	H	NC NC	L H	Q_B Q_B	L H	Stored B Data to A Bus; Store B Data
H	L							Output	Output	
		↕	↕	H	H	NC	NC	Q_B	Q_A	Stored A Data to B Bus, Stored B Data to A Bus

H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = Low–to–High Clock Transition; ↕ = NOT Low–to–High Clock Transition; NC = No Change; * = The clocks are not internally gated with either the Output Enables or the Source Inputs. Therefore, data at the A or B ports may be clocked into the storage registers, at any time. For I_{CC} reasons, Do Not Float Inputs.

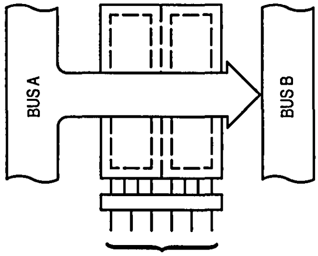
BUS APPLICATIONS

Real Time Transfer – Bus B to Bus A



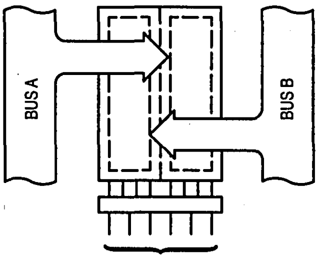
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA
L	L	X	X	X	L

Real Time Transfer – Bus A to Bus B



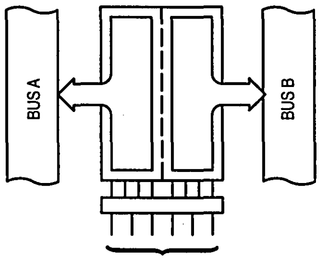
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA
H	H	X	X	L	X

Store Data from Bus A, Bus B or Bus A and Bus B



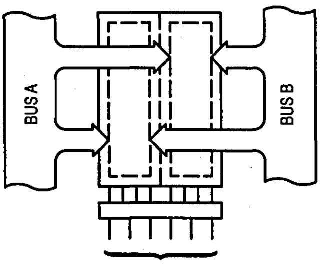
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Transfer A Stored Data to Bus B or Stored Data Bus B to Bus A or Both at the Same Time



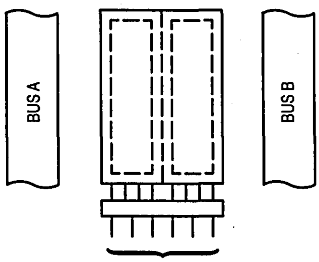
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H

Store Bus A in Both Registers or Store Bus B in Both Registers



OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA
H	H	↑	↑	L	X
L	L	↑	↑	X	L

Isolation



OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA
L	H	H or L	H or L	X	X

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.
1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage — (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS[1] ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits				Unit
			T_A = –40°C to +85°C				
			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V		
			Min	Max	Min	Max	
f_{max}	Clock Pulse Frequency	3	150				MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	3	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay Select to Output	1	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_s	Setup Time, HIGH or LOW Data to Clock	3	2.5		2.5		ns
t_h	Hold Time, HIGH or LOW Data to Clock	3	1.5		1.5		ns
t_w	Clock Pulse Width, HIGH or LOW	3	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0			ns

1. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

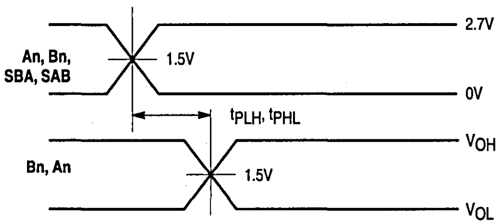
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

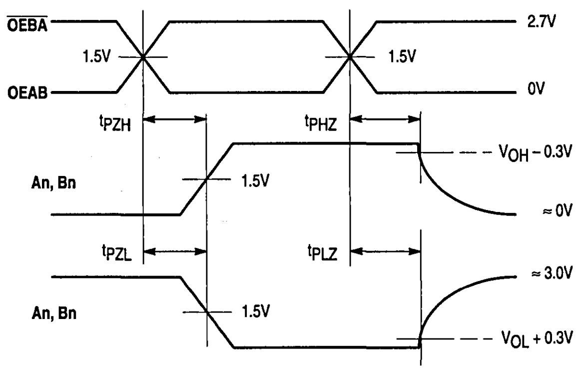
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state. The LCX652 is characterized with 7 outputs switching with 1 output held LOW.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF

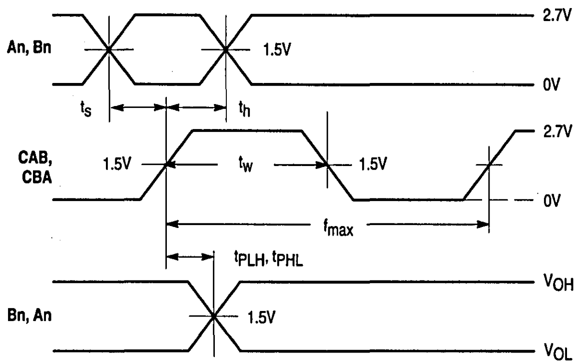


WAVEFORM 1 – SAB to B and SBA to A, An to Bn PROPAGATION DELAYS
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns



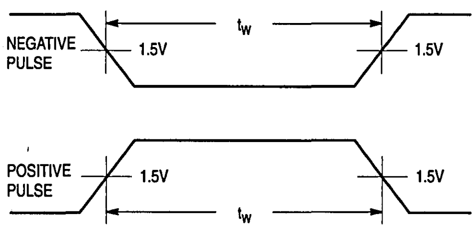
WAVEFORM 2 – $\overline{OEBA}$/OEAB to An/Bn OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

Figure 1. AC Waveforms



WAVEFORM 3 – CLOCK to Bn/An PROPAGATION DELAYS, CLOCK MINIMUM PULSE WIDTH, An/Bn to CLOCK SETUP AND HOLD TIMES

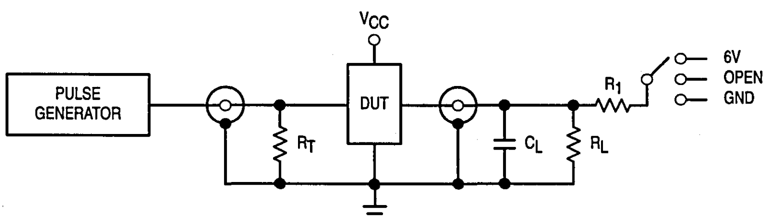
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$ except when noted



WAVEFORM 4 – INPUT PULSE DEFINITION

$t_R = t_F = 2.5ns$, 10% to 90% of 0V to 2.7V

Figure 2. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 3. Test Circuit

Product Preview

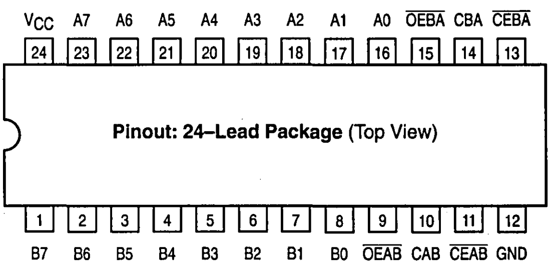
Low-Voltage CMOS Octal Registered Transceiver With Dual Output and Clock Enables

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX2952 is a high performance, non–inverting octal registered transceiver operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX2952 inputs to be safely driven from 5V devices. The MC74LCX2952 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Two 8–bit back to back registers store data from either of two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CAB, CBA) provided that the Clock Enable ($\overline{\text{CEAB}}$, $\overline{\text{CEBA}}$) is Low. The data is then presented at the 3–state output buffers, but is only accessible when the Output Enable ($\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$) is Low. The operation of the MC74LCX2952 is symmetrical — A inputs to B outputs occurs in the same manner as B inputs to A outputs.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

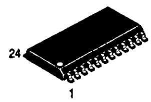


This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

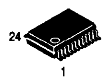
MC74LCX2952

LCX

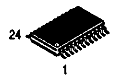
LOW–VOLTAGE CMOS OCTAL REGISTERED TRANSCEIVER



DW SUFFIX
PLASTIC SOIC
CASE 751E–04



SD SUFFIX
PLASTIC SSOP
CASE 940D–03

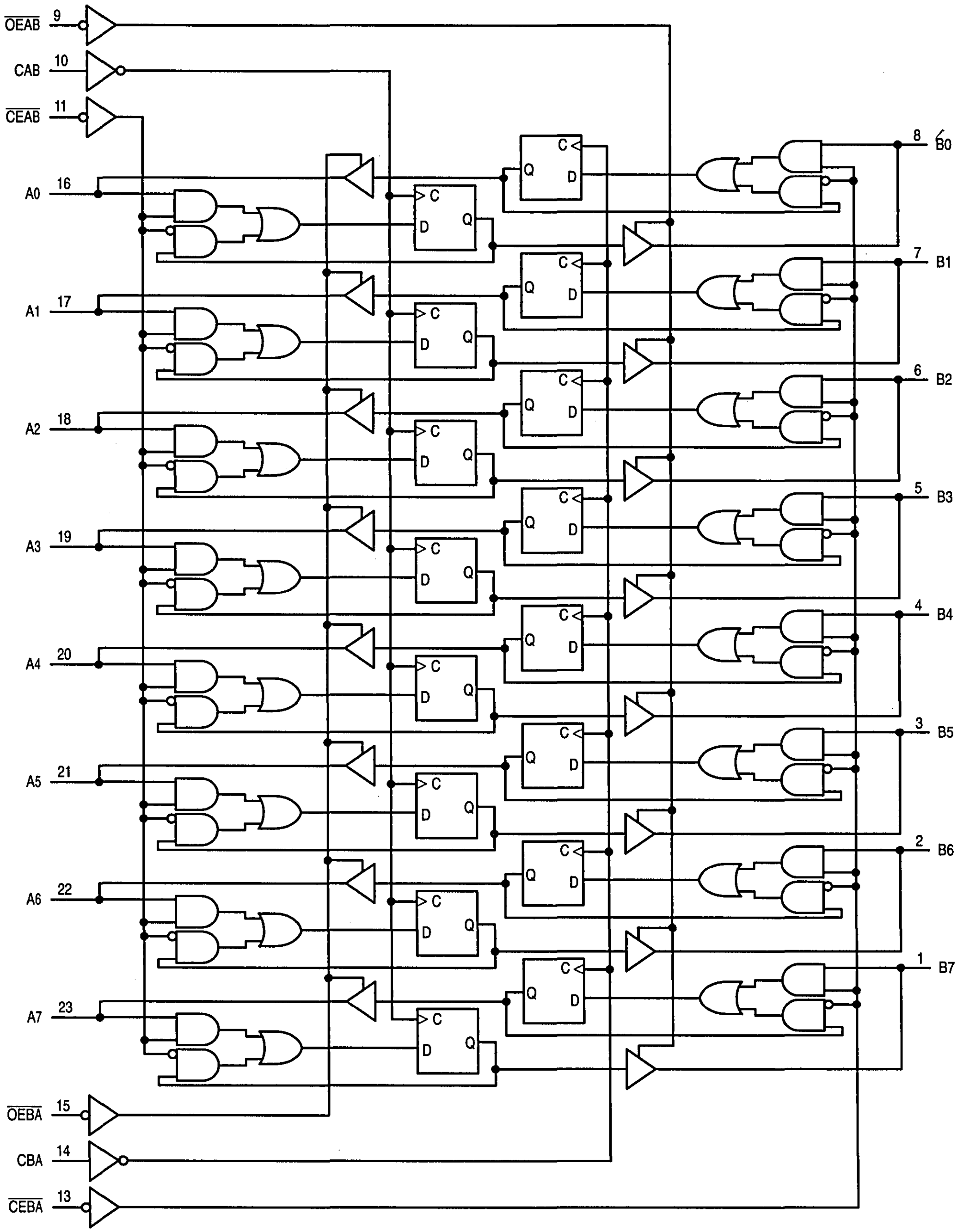


DT SUFFIX
PLASTIC TSSOP
CASE 948H–01

PIN NAMES

Pins	Function
A0–A7	Side A Inputs/Outputs
B0–B7	Side B Inputs/Outputs
CAB, CBA	Clock Pulse Inputs
$\overline{\text{CEAB}}$, $\overline{\text{CEBA}}$	Clock Enable Inputs
$\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$	Output Enable Inputs

LOGIC DIAGRAM



FUNCTION TABLE

Inputs								Internal Register		Outputs		
An	$\overline{OEAB}$	$\overline{CEAB}$	CAB	Bn	$\overline{OEBA}$	$\overline{CEBA}$	CBA	QABn	QBAn	An	Bn	Operating Mode
h	L	l	↑	U	H	X	X	H	X	NA	H	Load A to B Register;
l	L	l	↑	U	H	X	X	L	X	NA	L	Read B Output
X	L	h	X	U	H	X	X	NC	X	NA	NC	Hold; Read B Output
h	H	l	↑	X	H	X	X	H	X	NA	Z	Load A to B Register;
l	H	l	↑	X	H	X	X	L	X	NA	Z	Disable B Outputs
X	H	h	X	X	H	X	X	NC	X	NA	Z	Hold; Disable B Outputs
U	H	X	X	h	L	l	↑	X	H	H	NA	Load B to A Register;
U	H	X	X	l	L	l	↑	X	L	L	NA	Read A Output
U	H	X	X	X	L	h	X	X	NC	NC	NA	Hold; Read A Output
X	H	X	X	h	H	l	↑	X	H	Z	NA	Load B to A Register;
X	H	X	X	l	H	l	↑	X	L	Z	NA	Disable A Outputs
X	H	X	X	X	H	h	X	X	NC	Z	NA	Hold; Disable A Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to Clock Low–to–High Transition; L = Low Voltage Level; l =Low Voltage Level One Setup Time Prior to Clock Low–to–High Transition; NA = Not Applicable; U = Undriven; Z = High Impedance State; X = Don't Care; NC = No Change; ↑ = Low–to–High Transition

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	–50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V				–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V				24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V				–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V				12	mA
T_A	Operating Free–Air Temperature		–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V		0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OH} = –100µA	V_{CC} – 0.2		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OL} = 100µA		0.2	V
		V_{CC} = 2.7V; I_{OL}= 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	V_{CC} = 0V; V_I or V_O = 5.5V		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		10	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

AC CHARACTERISTICS ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits: $T_A = -40°C$ to $+85°C$, $V_{CC} = 3.0V$ to $3.6V$ Min	Max	$V_{CC} = 2.7V$ Min	Max	Unit
f_{max}	Clock Pulse Frequency	3	150				MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	1	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_s	Setup Time, HIGH to LOW Data to Clock	3	2.5		2.5		ns
t_h	Hold Time, HIGH to LOW Data to Clock	3	1.5		1.5		ns
t_s	Setup Time, HIGH to LOW $\overline{CExx}$ to Clock	3	2.5		2.5		ns
t_h	Hold Time, HIGH to LOW $\overline{CExx}$ to Clock	3	1.5		1.5		ns
t_w	Clock Pulse Width, HIGH or LOW	3	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0			ns

1. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

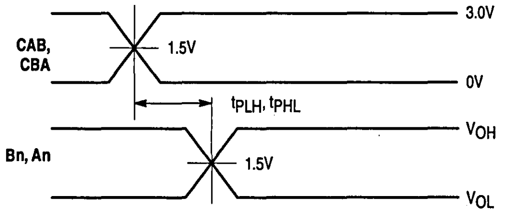
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25°C$ Min	Typ	Max	Unit
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

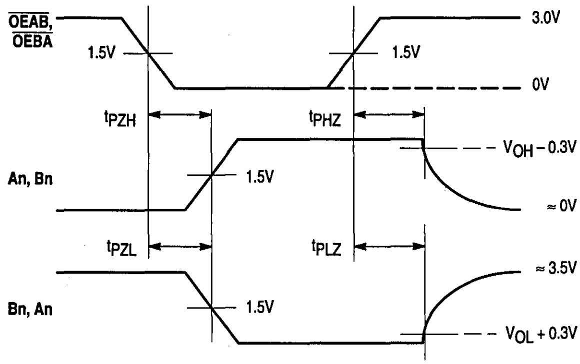
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

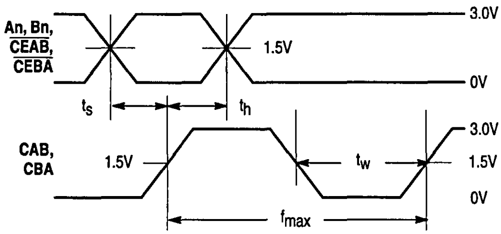
Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	25	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF



WAVEFORM 1 – Cxx to An/Bn PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

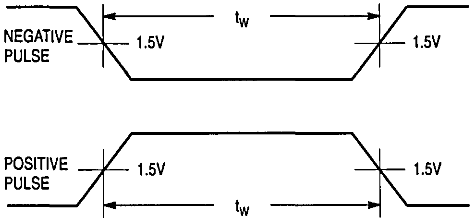


WAVEFORM 2 – $\overline{OExx}$ to An/Bn OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



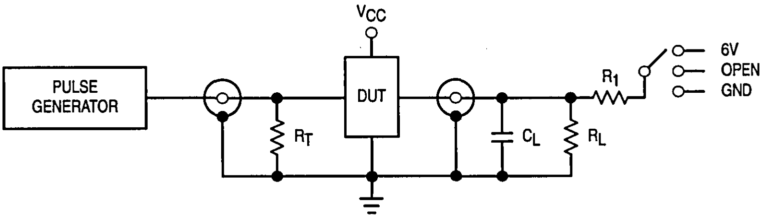
WAVEFORM 3 – Cxx MINIMUM PULSE WIDTH, An/Bn/$\overline{CExx}$ to Cxx SETUP AND HOLD TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$ except when noted

Figure 1. AC Waveforms



WAVEFORM 4 – INPUT PULSE DEFINITION
$t_R = t_F = 2.5ns$, 10% to 90% of 0V to 2.7V

Figure 2. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 3. Test Circuit

16-Bit Devices

Product Preview

Low-Voltage CMOS 16-Bit Buffer

With 5V-Tolerant Inputs and Outputs (3-State, Inverting)

The MC74LCX16240 is a high performance, inverting 16–bit buffer operating from a 2.7 to 3.6V supply. The device is nibble controlled. Each nibble has separate Output Enable inputs which can be tied together for full 16–bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16240 inputs to be safely driven from 5V devices. The LCX16240 is suitable for memory address driving and all TTL level bus oriented buffer applications.

Current drive capability is 24mA at the outputs. The Output Enable ($\overline{\text{OEn}}$) inputs, when HIGH, disable the outputs by placing them in a HIGH Z condition.

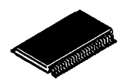
- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

The MC74LCX16240 contains sixteen inverting buffers with 3–state 5V–tolerant outputs. The device is nibble controlled with each nibble functioning identically, but independently. The control pins may be tied together to obtain full 16–bit operation. The 3–state outputs are controlled by an Output Enable ($\overline{\text{OEn}}$) input for each nibble. When $\overline{\text{OEn}}$ is LOW, the outputs are on. When $\overline{\text{OEn}}$ is HIGH, the outputs are in the high impedance state.

MC74LCX16240

LCX

LOW–VOLTAGE CMOS 16–BIT BUFFER

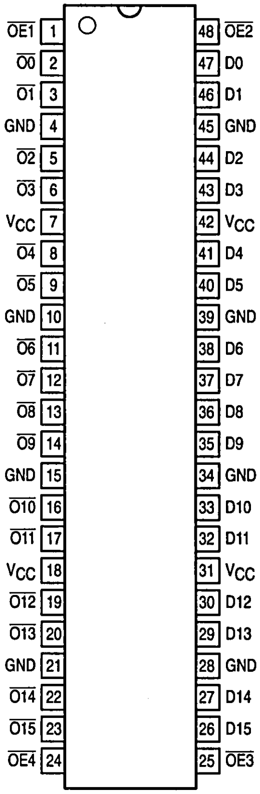


DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1201–01

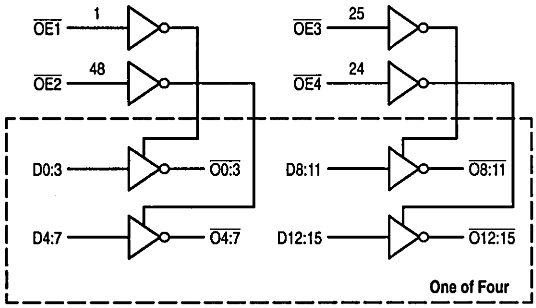
PIN NAMES

Pins	Function
$\overline{\text{OEn}}$	Output Enable Inputs
D0–D15	Inputs
$\overline{\text{O0}}$–$\overline{\text{O15}}$	Outputs

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.



LOGIC DIAGRAM



$\overline{OE1}$	D0:3	$\overline{O0:3}$	$\overline{OE2}$	D4:7	$\overline{O4:7}$	$\overline{OE3}$	D8:11	$\overline{O8:11}$	$\overline{OE4}$	D12:15	$\overline{O12:15}$
L	L	H	L	L	H	L	L	H	L	L	H
L	H	L	L	H	L	L	H	L	L	H	L
H	X	Z	H	X	Z	H	X	Z	H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	–50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.
1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	$T_A = -40°C$ to $+85°C$		Unit
			Min	Max	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	μA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	μA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	μA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		20	μA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	μA

AC CHARACTERISTICS[1] ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits			Unit
			$T_A = -40°C$ to $+85°C$			
			$V_{CC} = 3.0V$ to $3.6V$		$V_{CC} = 2.7V$	
			Min	Max	Max	
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	4.5 4.5	5.3 5.3	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	5.4 5.4	6.0 6.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	5.3 5.3	5.4 5.4	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0		ns

1. These AC parameters are preliminary and may be modified prior to release.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

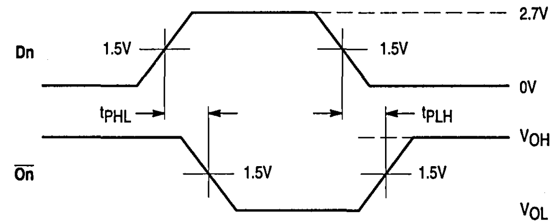
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25°C$			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

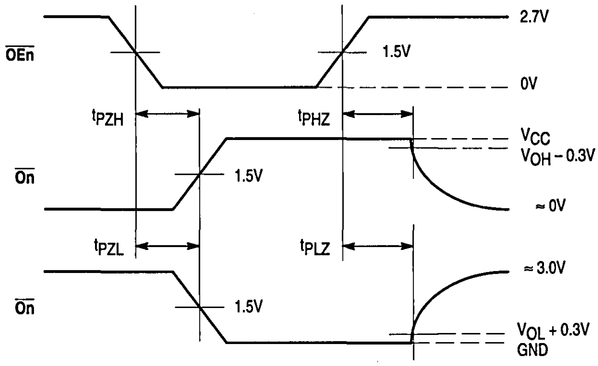
1. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	20	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF

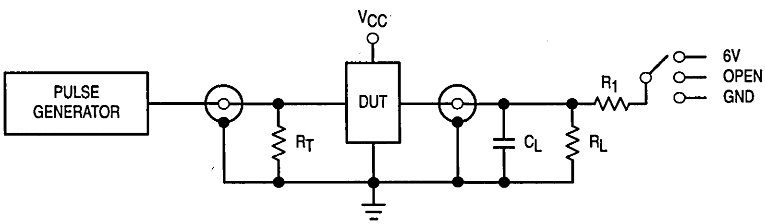


WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Product Preview

Low-Voltage CMOS 16-Bit Buffer

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX16244

LCX

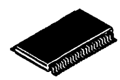
LOW–VOLTAGE CMOS 16–BIT BUFFER

The MC74LCX16244 is a high performance, non–inverting 16–bit buffer operating from a 2.7 to 3.6V supply. The device is nibble controlled. Each nibble has separate Output Enable inputs which can be tied together for full 16–bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16244 inputs to be safely driven from 5V devices. The MC74LCX16244 is suitable for memory address driving and all TTL level bus oriented buffer applications.

Current drive capability is 24mA at the outputs. The Output Enable ($\overline{\text{OEn}}$) inputs, when HIGH, disable the outputs by placing them in a HIGH Z condition.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

The MC74LCX16244 contains sixteen non–inverting buffers with 3–state 5V–tolerant outputs. The device is nibble controlled with each nibble functioning identically, but independently. The control pins may be tied together to obtain full 16–bit operation. The 3–state outputs are controlled by an Output Enable ($\overline{\text{OEn}}$) input for each nibble. When $\overline{\text{OEn}}$ is LOW, the outputs are on. When $\overline{\text{OEn}}$ is HIGH, the outputs are in the high impedance state.

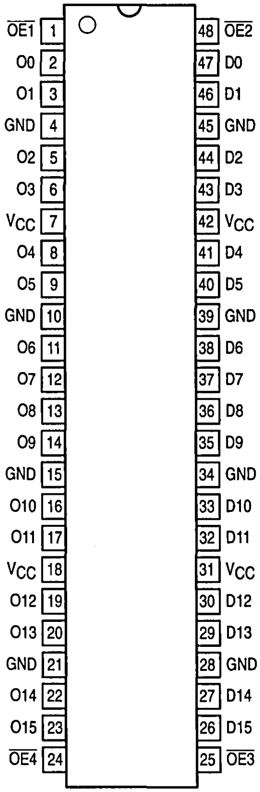


DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1201–01

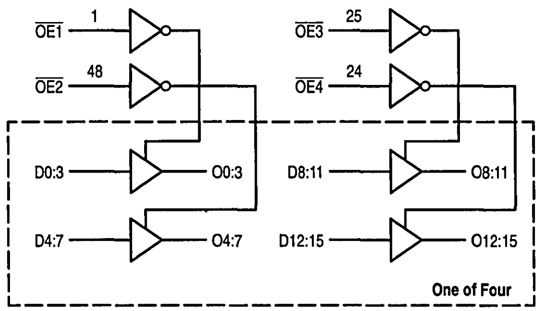
PIN NAMES

Pins	Function
$\overline{\text{OEn}}$	Output Enable Inputs
D0–D15	Inputs
O0–O15	Outputs

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.



LOGIC DIAGRAM



$\overline{OE1}$	D0:3	O0:3	$\overline{OE2}$	D4:7	O4:7	$\overline{OE3}$	D8:11	O8:11	$\overline{OE4}$	D12:15	O12:15
L	L	H	L	L	H	L	L	H	L	L	H
L	H	L	L	H	L	L	H	L	L	H	L
H	X	Z	H	X	Z	H	X	Z	H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V				–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V				24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V				–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V				12	mA
T_A	Operating Free–Air Temperature		–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V		0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
I_I	Input Leakage Current	2.7V ≤ V_{CC} ≤ 3.6V; 0V ≤ V_I ≤ 5.5V		±5.0	µA
I_{OZ}	3–State Output Current	2.7 ≤ V_{CC} ≤ 3.6V; 0V ≤ V_O ≤ 5.5V; V_I = V_{IH} or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	V_{CC} = 0V; V_I or V_O = 5.5V		10	µA
I_{CC}	Quiescent Supply Current	2.7 ≤ V_{CC} ≤ 3.6V; V_I = GND or V_{CC}		20	µA
		2.7 ≤ V_{CC} ≤ 3.6V; 3.6 ≤ V_I or V_O ≤ 5.5V		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input	2.7 ≤ V_{CC} ≤ 3.6V; V_{IH} = V_{CC} – 0.6V		500	µA

AC CHARACTERISTICS[1] (t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Waveform	Limits			Unit
			T_A = –40°C to +85°C			
			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V	
			Min	Max	Max	
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	4.5 4.5	5.2 5.2	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	5.5 5.5	6.3 6.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	5.4 5.4	5.7 5.7	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0		ns

1. These AC parameters are preliminary and may be modified prior to release.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

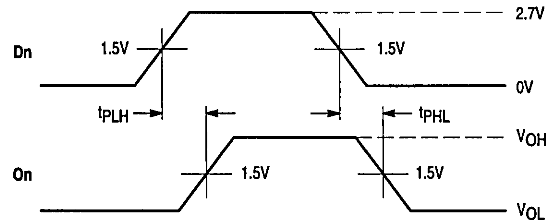
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V

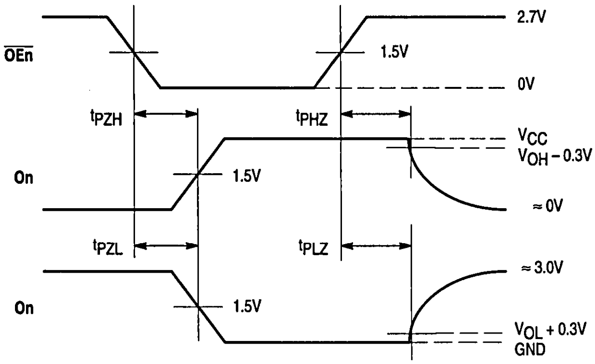
1. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	20	pF
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF

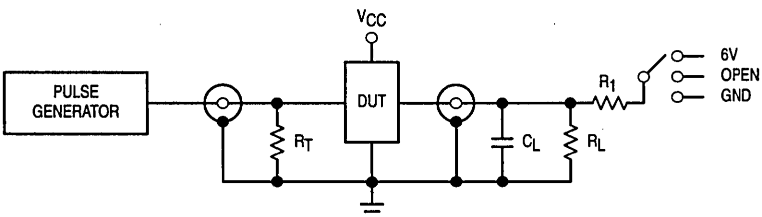


WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Product Preview

Low-Voltage CMOS 16-Bit Transceiver

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX16245

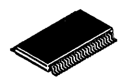
LCX

LOW–VOLTAGE CMOS 16–BIT TRANSCEIVER

The MC74LCX16245 is a high performance, non–inverting 16–bit transceiver operating from a 2.7 to 3.6V supply. The device is byte controlled. Each byte has separate Output Enable inputs which can be tied together for full 16–bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16245 inputs to be safely driven from 5V devices. The MC74LCX16245 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Current drive capability is 24mA at both A and B ports. The Transmit/Receive (T/$\overline{R}$n) inputs determine the direction of data flow through the bi–directional transceiver. Transmit (active–HIGH) enables data from A ports to B ports; Receive (active–LOW) enables data from B to A ports. The Output Enable inputs ($\overline{OEn}$), when HIGH, disable both A and B ports by placing them in a HIGH Z condition.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1201–01

PIN NAMES

Pins	Function
$\overline{OEn}$	Output Enable Inputs
T/$\overline{R}$n	Transmit/Receive Inputs
A0–A15	Side A Inputs or 3–State Outputs
B0–B15	Side B Inputs or 3–State Outputs

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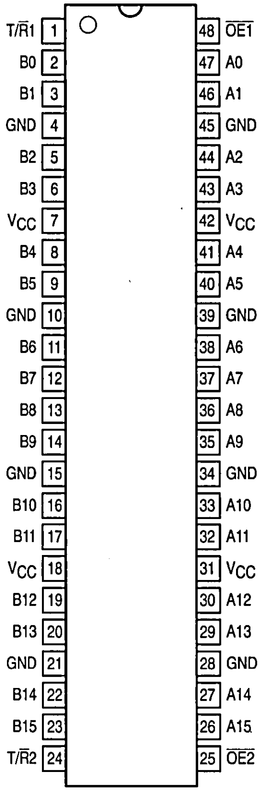
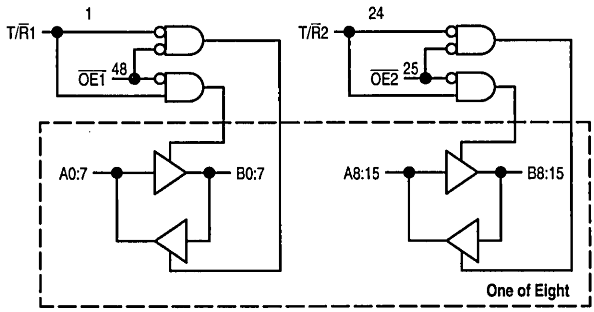


LOGIC DIAGRAM



Inputs		Outputs	Inputs		Outputs
$\overline{OE1}$	T/$\overline{R}$1		$\overline{OE2}$	T/$\overline{R}$2	
L	L	Bus B0:7 Data to Bus A0:7	L	L	Bus B8:15 Data to Bus A8:15
L	H	Bus A0:7 Data to Bus B0:7	L	H	Bus A8:15 Data to Bus B8:15
H	X	High Z State on A0:7, B0:7	H	X	High Z State on A8:15, B8:15

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage — (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	$T_A = -40°C$ to $+85°C$ Min	Max	Unit
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		20	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS[1] ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits $T_A = -40°C$ to $+85°C$ $V_{CC} = 3.0V$ to $3.6V$ Min	Max	$V_{CC} = 2.7V$ Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	4.5 4.5	5.2 5.2	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	6.5 6.5	7.2 7.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	6.4 6.4	6.9 6.9	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0		ns

1. These AC parameters are preliminary and may be modified prior to release.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

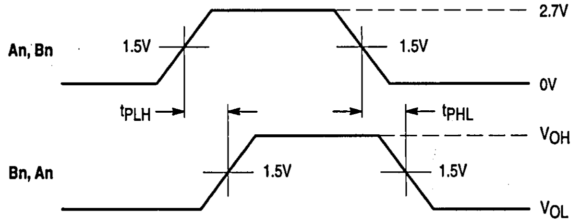
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25°C$ Min	Typ	Max	Unit
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

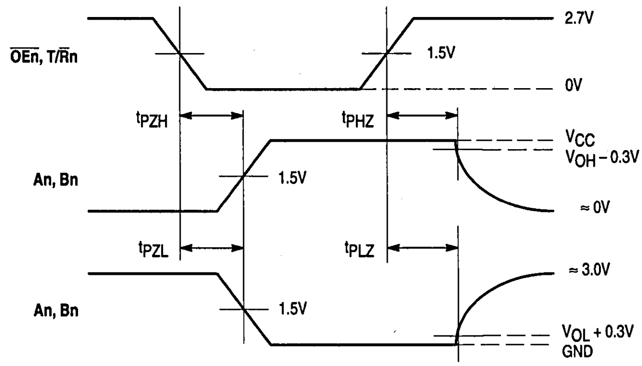
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	20	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF

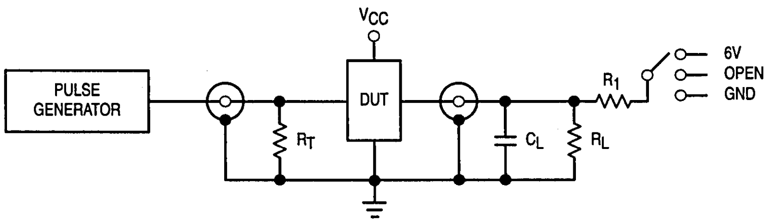


WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; $f = 1MHz$; $t_W = 500ns$



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; $f = 1MHz$; $t_W = 500ns$

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Product Preview

Low-Voltage CMOS 16-Bit Transparent Latch

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX16373 is a high performance, non–inverting 16–bit transparent latch operating from a 2.7 to 3.6V supply. The device is byte controlled. Each byte has separate Output Enable and Latch Enable inputs. These control pins can be tied together for full 16–bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16373 inputs to be safely driven from 5V devices.

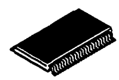
The MC74LCX16373 contains 16 D–type latches with 3–state 5V–tolerant outputs. When the Latch Enable (LEn) inputs are HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH–to–LOW transition of LE. The 3–state outputs are controlled by the Output Enable ($\overline{OEn}$) inputs. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

MC74LCX16373

LCX

**LOW–VOLTAGE
CMOS 16–BIT
TRANSPARENT LATCH**

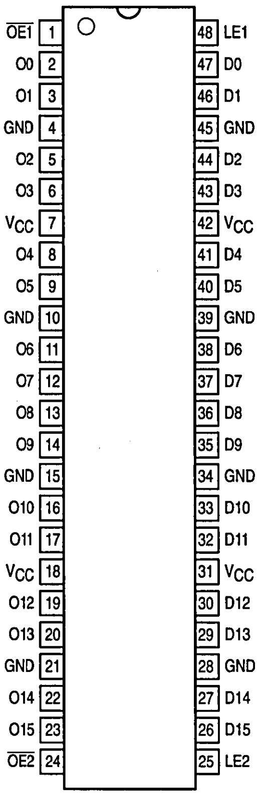


DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1201–01

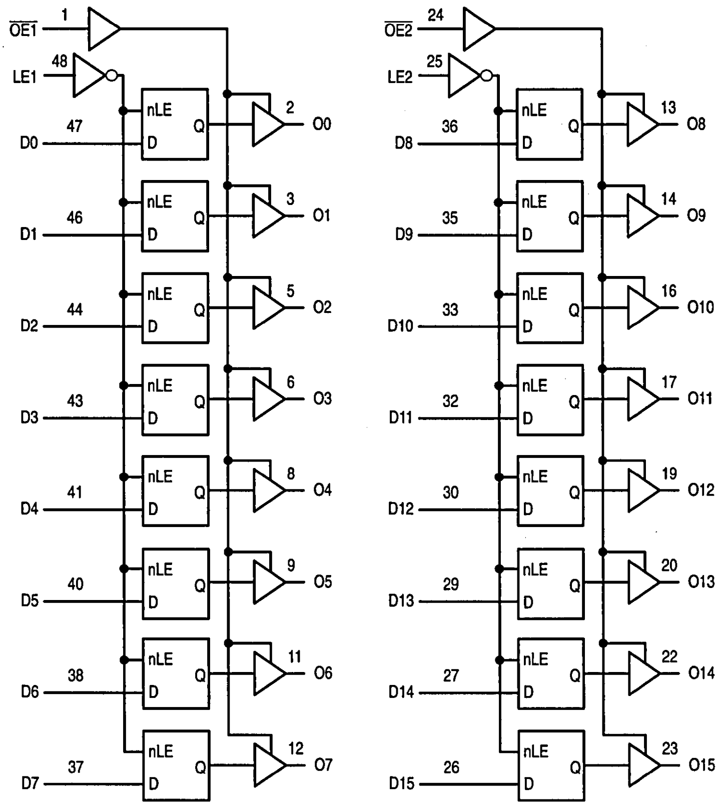
PIN NAMES

Pins	Function
$\overline{OEn}$	Output Enable Inputs
LEn	Latch Enable Inputs
D0–D15	Inputs
O0–O15	Outputs

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.



LOGIC DIAGRAM



Inputs			Outputs	Inputs			Outputs
LE1	$\overline{OE1}$	D0:7	O0:7	LE2	$\overline{OE2}$	D8:15	O8:15
X	H	X	Z	X	H	X	Z
H	L	L	L	H	L	L	L
H	L	H	H	H	L	H	H
L	L	X	O0	L	L	X	O0

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	$T_A = -40°C$ to $+85°C$		Unit
			Min	Max	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		20	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS[1] ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits				Unit
			$T_A = -40°C$ to $+85°C$				
			$V_{CC} = 3.0V$ to $3.6V$		$V_{CC} = 2.7V$		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Dn to On	1	1.5 1.5	5.4 5.4	1.5 1.5	5.9 5.9	ns
t_{PLH} t_{PHL}	Propagation Delay LE to On	3	1.5 1.5	5.5 5.5	1.5 1.5	6.4 6.4	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH and LOW Level	2	1.5 1.5	6.1 6.1	1.5 1.5	6.5 6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time from HIGH and LOW Level	2	1.5 1.5	6.0 6.0	1.5 1.5	6.3 6.3	ns
t_s	Setup Time, HIGH or LOW Dn to LE	3	2.5		2.5		ns
t_h	Hold Time, HIGH or LOW Dn to LE	3	1.5		1.5		ns
t_w	LE Pulse Width, HIGH	3	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0			ns

1. These AC parameters are preliminary and may be modified prior to release.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

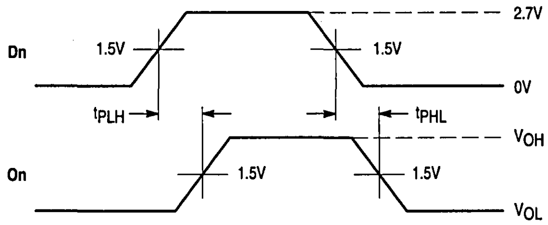
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25°C$			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

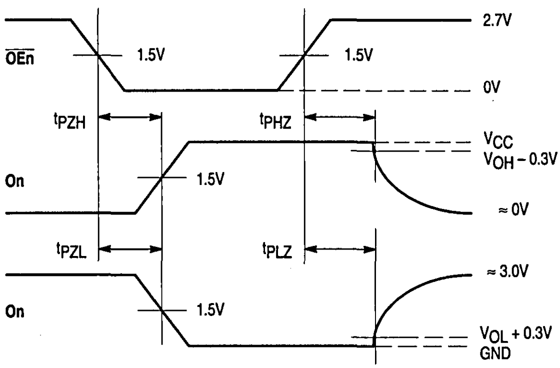
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

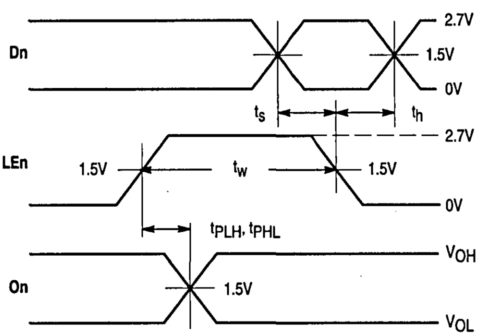
Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	20	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF



WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

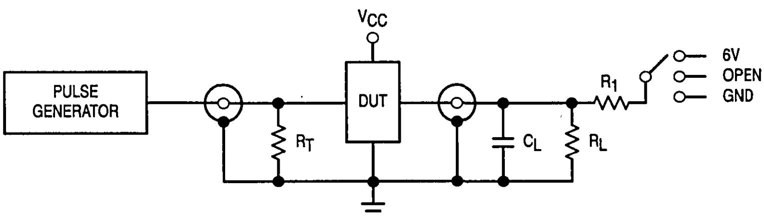


WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$ except when noted

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Product Preview

Low-Voltage CMOS 16-Bit D-Type Flip-Flop

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX16374 is a high performance, non–inverting 16–bit D–type flip–flop operating from a 2.7 to 3.6V supply. The device is byte controlled. Each byte has separate Output Enable and Clock Pulse inputs. These control pins can be tied together for full 16–bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16374 inputs to be safely driven from 5V devices.

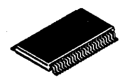
The MC74LCX16374 consists of 16 edge–triggered flip–flops with individual D–type inputs and 5V–tolerant 3–state true outputs. The buffered clocks (CPn) and buffered Output Enables ($\overline{\text{OEn}}$) are common to all flip–flops within the respective byte. The flip–flops will store the state of individual D inputs that meet the setup and hold time requirements on the LOW–to–HIGH Clock (CP) transition. With the $\overline{\text{OE}}$ LOW, the contents of the flip–flops are available at the outputs. When the $\overline{\text{OE}}$ is HIGH, the outputs go to the high impedance state. The $\overline{\text{OE}}$ input level does not affect the operation of the flip–flops.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

MC74LCX16374

LCX

LOW–VOLTAGE CMOS 16–BIT D–TYPE FLIP–FLOP

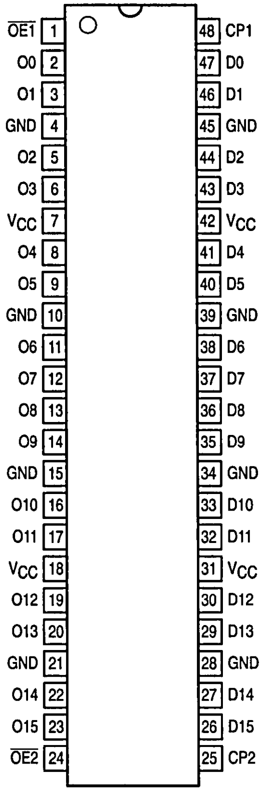


DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1201–01

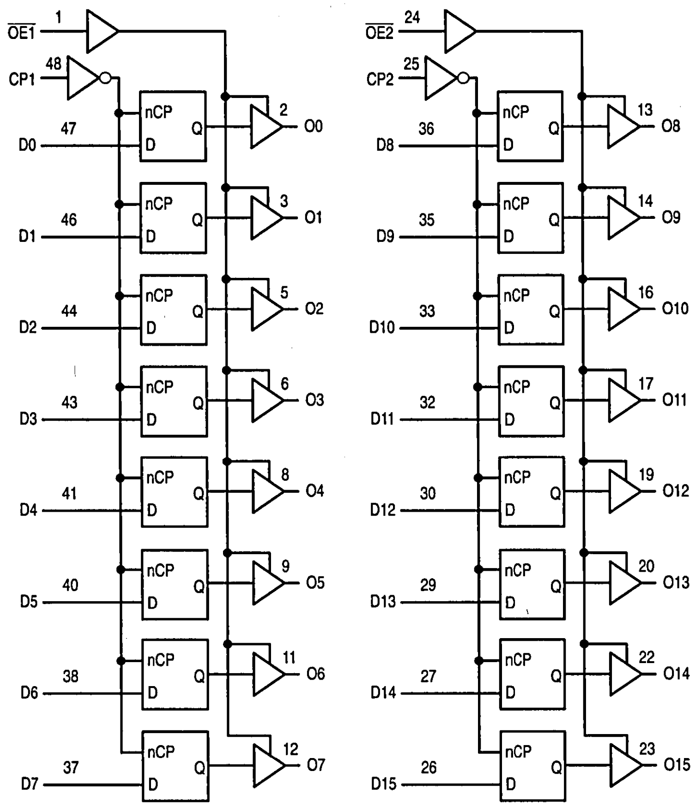
PIN NAMES

Pins	Function
$\overline{\text{OEn}}$	Output Enable Inputs
CPn	Clock Pulse Inputs
D0–D15	Inputs
O0–O15	Outputs

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.



LOGIC DIAGRAM



Inputs			Outputs	Inputs			Outputs
CP1	$\overline{OE1}$	D0:7	O0:7	CP2	$\overline{OE2}$	D8:15	O8:15
↑	L	H	H	↑	L	H	H
↑	L	L	L	↑	L	L	L
L	L	X	O0	L	L	X	O0
X	H	X	Z	X	H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; ↑ = Low–to–High Transition; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage — (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		V_{CC} = 2.7V; I_{OL} = 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		20	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

AC CHARACTERISTICS[1] ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits, T_A = –40°C to +85°C, V_{CC} = 3.0V to 3.6V Min	Max	V_{CC} = 2.7V Min	Max	Unit
f_{max}	Clock Pulse Frequency	1	170				MHz
t_{PLH} t_{PHL}	Propagation Delay CP to On	1	1.5 1.5	6.2 6.2	1.5 1.5	6.5 6.5	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH and LOW Levels	2	1.5 1.5	6.1 6.1	1.5 1.5	6.3 6.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time from HIGH and LOW Levels	2	1.5 1.5	6.0 6.0	1.5 1.5	6.2 6.2	ns
t_s	Setup Time, HIGH or LOW Dn to CP	1	2.5		2.5		ns
t_h	Hold Time, HIGH or LOW Dn to CP	1	1.5		1.5		ns
t_w	CP Pulse Width, HIGH or LOW	3	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0			ns

1. These AC parameters are preliminary and may be modified prior to release.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

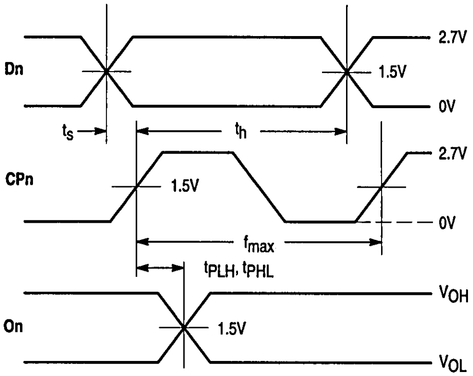
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C Min	Typ	Max	Unit
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

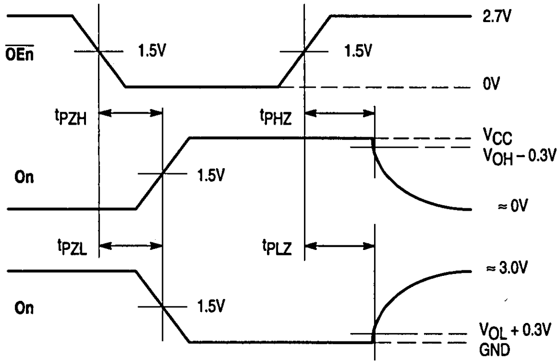
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

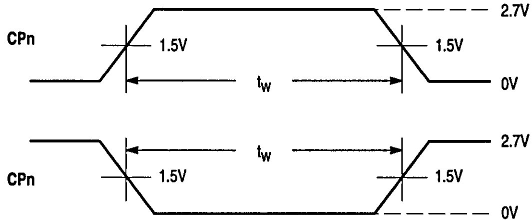
Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	20	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF



WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

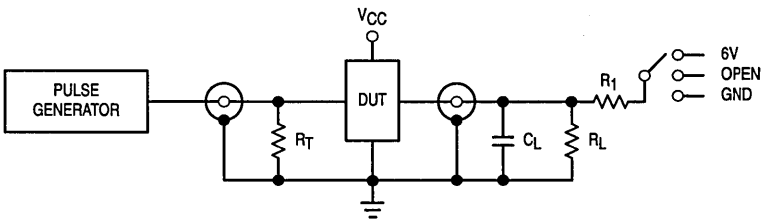


WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



WAVEFORM 3 – PULSE WIDTH
$t_R = t_F = 2.5ns$ (or fast as required) from 10% to 90%;
Output requirements: $V_{OL} \leq 0.8V$, $V_{OH} \geq 2.0V$

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Product Preview

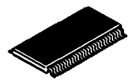
Low-Voltage CMOS 18-Bit Universal Bus Transceiver

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX16500

LCX

LOW–VOLTAGE CMOS 18–BIT UNIVSERAL BUS TRANSCEIVER

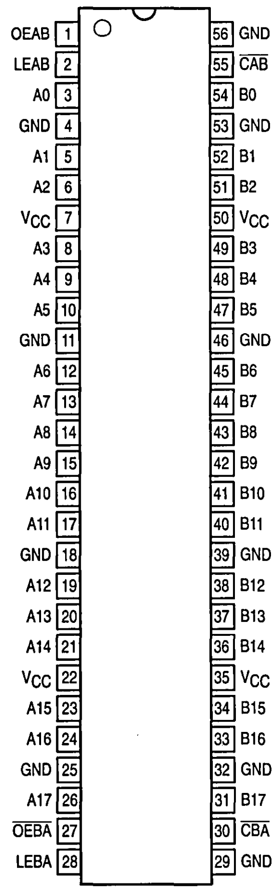


DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202–01

The MC74LCX16500 is a high performance, non–inverting 18–bit universal bus transceiver operating from a 2.7 to 3.6V supply. The device is "byte+1" controlled. Each "byte+1" has separate control inputs which can be tied together for full 18–bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16500 inputs to be safely driven from 5V devices. The MC74LCX16500 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Data flow in each direction is controlled by Output Enable (OEAB, $\overline{\text{OEBA}}$), Latch Enable (LEAB, LEBA) and Clock inputs ($\overline{\text{CAB}}$, $\overline{\text{CBA}}$). When LEAB is HIGH, the A–to–B dataflow is transparent. When LEAB is LOW, and $\overline{\text{CAB}}$ is held at LOW or HIGH, the data A is latched; on the HIGH–to–LOW transition of $\overline{\text{CAB}}$ the A–data is stored in the latch/flip–flop. The outputs are active when OEAB is HIGH. When OEAB is LOW the B–outputs are in 3–state. Similarly, the LEBA, $\overline{\text{OEBA}}$ and $\overline{\text{CBA}}$ control the B–to–A dataflow. Please note that the output enables are complementary; OEAB is active HIGH, $\overline{\text{OEBA}}$ is active LOW.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Product Preview

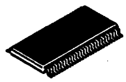
Low-Voltage CMOS 16-Bit Latching Transceiver

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX16543

LCX

LOW–VOLTAGE CMOS 16–BIT LATCHING TRANSCEIVER

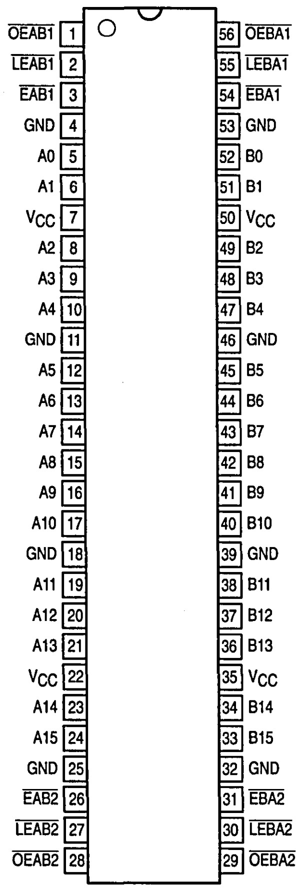


DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202–01

The MC74LCX16543 is a high performance, non–inverting 16–bit latching transceiver operating from a 2.7 to 3.6V supply. The device is byte controlled. Each byte has separate control inputs which can be tied together for full 16–bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16543 inputs to be safely driven from 5V devices. The MC74LCX16543 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

For data flow from A to B with the $\overline{\text{EAB}}$ LOW, the A–to–B Output Enable ($\overline{\text{OEAB}}$) must be LOW in order to enable data to the B bus, as indicated in the Function Table. With $\overline{\text{EAB}}$ LOW, a LOW signal on the A–to–B Latch Enable ($\overline{\text{LEAB}}$) input makes the A–to–B latches transparent; a subsequent LOW–to–HIGH transition of the $\overline{\text{LEAB}}$ signal will latch the A latches, and the outputs no longer change with the A inputs. With $\overline{\text{EAB}}$ and $\overline{\text{OEAB}}$ both LOW, the 3–State B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is symetric to that above, but uses the $\overline{\text{EBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Product Preview

Low-Voltage CMOS 16-Bit Transceiver/Registered Transceiver

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX16646

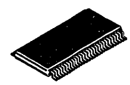
LCX

LOW–VOLTAGE CMOS 16–BIT TRANSCEIVER/ REGISTERED TRANSCEIVER

The MC74LCX16646 is a high performance, non–inverting 16–bit transceiver/registered transceiver operating from a 2.7 to 3.6V supply. The device is byte controlled. Each byte has separate control inputs which can be tied together for full 16–bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16646 inputs to be safely driven from 5V devices. The MC74LCX16646 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes from a LOW–to–HIGH logic level. Output Enable ($\overline{OEn}$) and Direction Control (DIRn) pins are provided to control the transceiver outputs. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls (SBAn, SABn) can multiplex stored and real–time (transparent mode) data. The DIR determines which bus will receive data when $\overline{OE}$ is active LOW. In the isolation mode ($\overline{OE}$ HIGH), A data may be stored in the B register or B data may be stored in the A register. Only one of the two buses, A or B, may be driven at one time.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202–01

PIN NAMES

Pins	Function
A0–A15	Side A Inputs/Outputs
B0–B15	Side B Inputs/Outputs
CABn, CBAn	Clock Pulse Inputs
SABn, SBAn	Select Control Inputs
DIRn, $\overline{OEn}$	Output Enable Inputs

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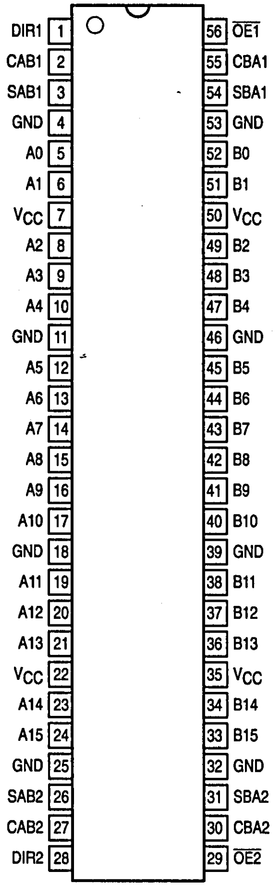
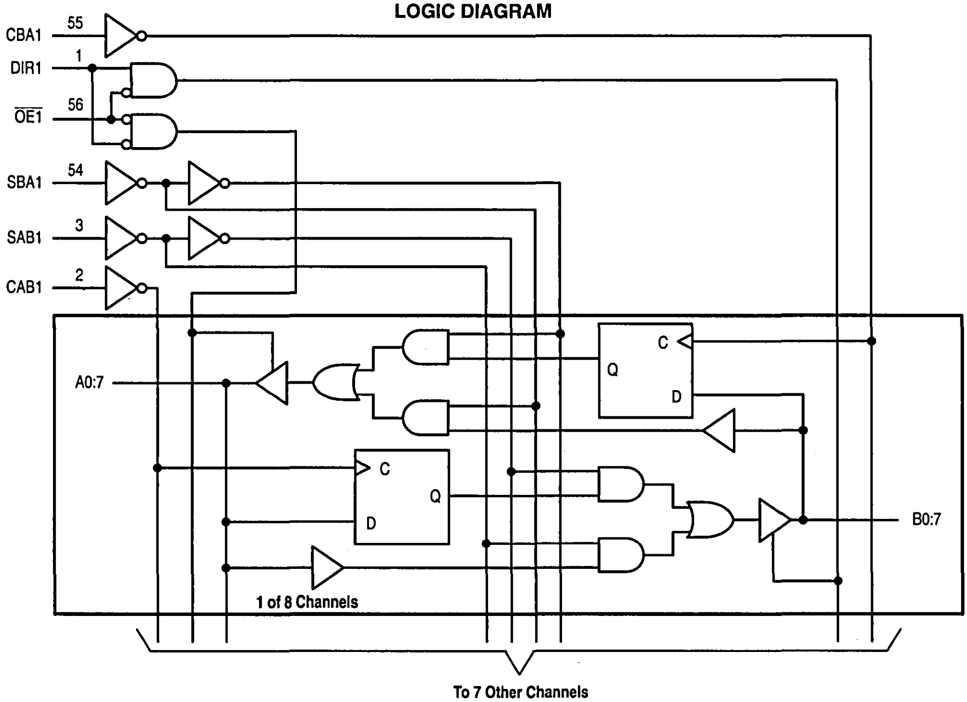
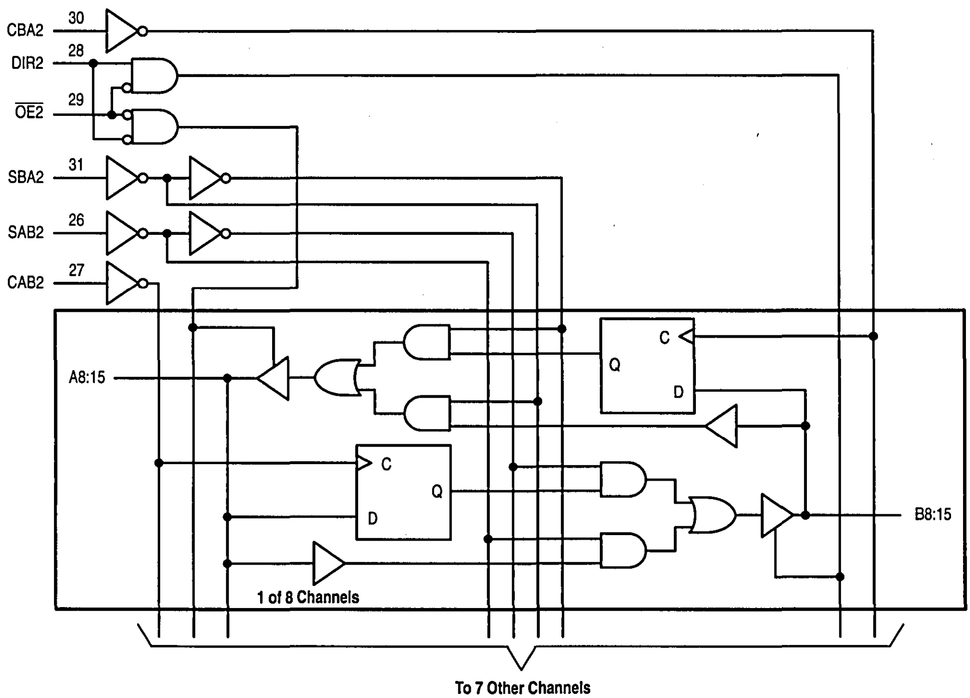

DIR1 1
CAB1 2
SAB1 3
GND 4
A0 5
A1 6
V_{CC} 7
A2 8
A3 9
A4 10
GND 11
A5 12
A6 13
A7 14
A8 15
A9 16
A10 17
GND 18
A11 19
A12 20
A13 21
V_{CC} 22
A14 23
A15 24
GND 25
SAB2 26
CAB2 27
DIR2 28
56 $\overline{OE1}$
55 CBA1
54 SBA1
53 GND
52 B0
51 B1
50 V_{CC}
49 B2
48 B3
47 B4
46 GND
45 B5
44 B6
43 B7
42 B8
41 B9
40 B10
39 GND
38 B11
37 B12
36 B13
35 V_{CC}
34 B14
33 B15
32 GND
31 SBA2
30 CBA2
29 $\overline{OE2}$

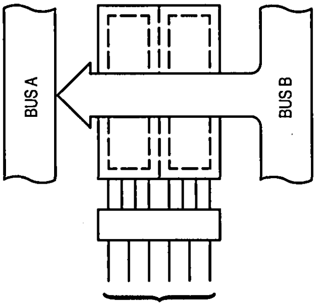
LOGIC DIAGRAM





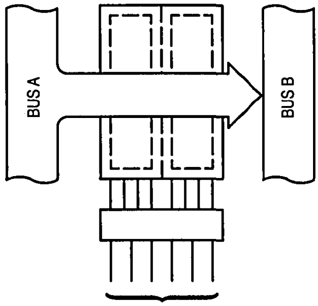
BUS APPLICATIONS

Real Time Transfer – Bus B to Bus A



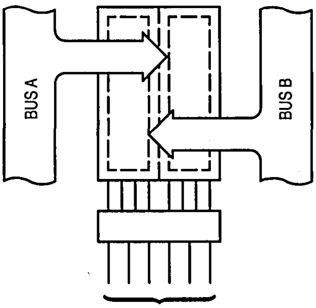
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

Real Time Transfer – Bus A to Bus B



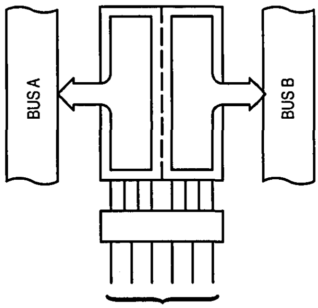
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

Store Data from Bus A, Bus B or Busses A and B



$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Transfer Storage Data to Bus A or Bus B



$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

FUNCTION TABLE

Inputs						Storage Registers		Data Ports		Operating Mode
$\overline{OEn}$	DIRn	CABn	CBAn	SABn	SBAn	Q_A	Q_B	A_n	B_n	Operating Mode
H	X							Input	Input	
		‡	‡	X	X	NC	NC	X	X	Isolation, Hold Storage
		↑	↑	X	X	L H X X	X X L H	L H X X	X X L H	Store A and/or B Data
L	H							Input	Output	
		‡	X*	L	X	NC NC	NC NC	L H	L H	Real Time A Data to B Bus
				H	X	NC	NC	X	Q_A	Stored A Data to B Bus
		↑	X*	L	X	L H	NC NC	L H	L H	Real Time A Data to B Bus; Store A Data
				H	X	L H	NC NC	L H	Q_A Q_A	Stored A Data to B Bus; Store A Data
L	L							Output	Input	
		X*	‡	X	L	NC NC	NC NC	L H	L H	Real Time B Data to A Bus
				X	H	NC	NC	Q_B	X	Stored B Data to A Bus
		X*	↑	X	L	NC NC	L H	L H	L H	Real Time B Data to A Bus; Store B Data
				X	H	NC NC	L H	Q_B Q_B	L H	Stored B Data to A Bus; Store B Data

H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = Low–to–High Clock Transition; ‡ = NOT Low–to–High Clock Transition; NC = No Change; * = The clocks are not internally gated with either the Output Enables or the Source Inputs. Therefore, data at the A or B ports may be clocked into the storage registers, at any time. For I_{CC} reasons, Do Not Float Inputs.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	–50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.
1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V				–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V				24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V				–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V				12	mA
T_A	Operating Free–Air Temperature		–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V		0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

			T_A = –40°C to +85°C		
Symbol	Characteristic	Condition	Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	2.7V ≤ V_{CC} ≤ 3.6V	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	2.7V ≤ V_{CC} ≤ 3.6V		0.8	V
V_{OH}	HIGH Level Output Voltage	2.7V ≤ V_{CC} ≤ 3.6V; I_{OH} = –100µA	V_{CC} – 0.2		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	2.7V ≤ V_{CC} ≤ 3.6V; I_{OL} = 100µA		0.2	V
		V_{CC} = 2.7V; I_{OL}= 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	
I_I	Input Leakage Current	2.7V ≤ V_{CC} ≤ 3.6V; 0V ≤ V_I ≤ 5.5V		±5.0	µA
I_{OZ}	3–State Output Current	2.7 ≤ V_{CC} ≤ 3.6V; 0V ≤ V_O ≤ 5.5V; V_I = V_{IH} or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	V_{CC} = 0V; V_I or V_O = 5.5V		10	µA
I_{CC}	Quiescent Supply Current	2.7 ≤ V_{CC} ≤ 3.6V; V_I = GND or V_{CC}		20	µA
		2.7 ≤ V_{CC} ≤ 3.6V; 3.6 ≤ V_I or V_O ≤ 5.5V		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input	2.7 ≤ V_{CC} ≤ 3.6V; V_{IH} = V_{CC} – 0.6V		500	µA

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use V_{IH} ≥ 2.4V, V_{IL} ≤ 0.5V.

AC CHARACTERISTICS[1] ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits $T_A = -40°C$ to $+85°C$ $V_{CC} = 3.0V$ to $3.6V$ Min	Max	$V_{CC} = 2.7V$ Min	Max	Unit
f_{max}	Clock Pulse Frequency	3	170				MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	3	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	5.0 5.0	1.5 1.5	6.0 6.0	ns
t_{PLH} t_{PHL}	Propagation Delay Select to Output	1	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_s	Setup Time, HIGH or LOW Data to Clock	3	2.5		2.5		ns
t_h	Hold Time, HIGH or LOW Data to Clock	3	1.5		1.5		ns
t_w	Clock Pulse Width, HIGH or LOW	3	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0			ns

1. These AC parameters are preliminary and may be modified prior to release.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

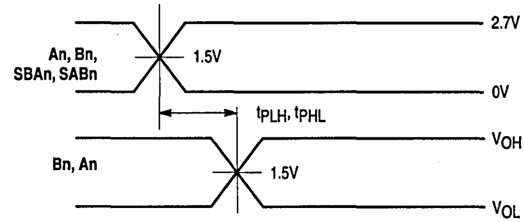
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25°C$ Min	Typ	Max	Unit
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

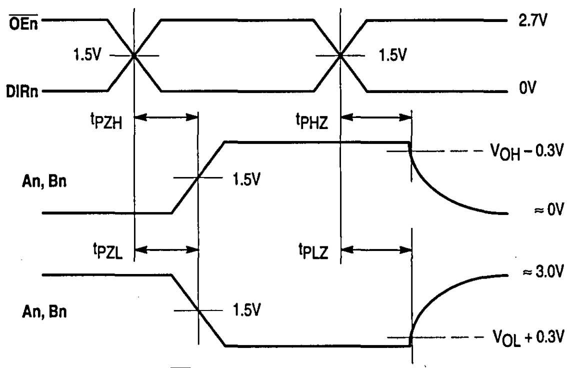
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	20	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF

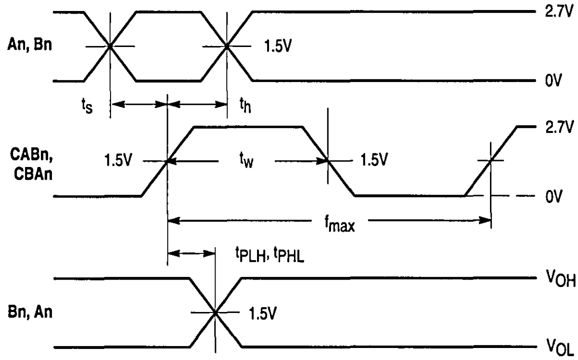


WAVEFORM 1 – SAB to B and SBA to A, An to Bn PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



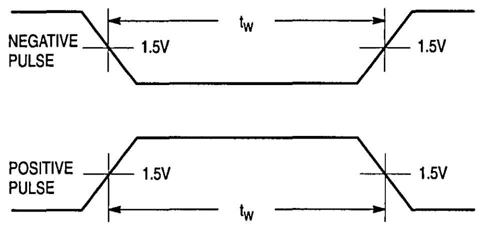
WAVEFORM 2 – $\overline{OE}$/DIR to An/Bn OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 1. AC Waveforms



WAVEFORM 3 – CLOCK to Bn/An PROPAGATION DELAYS, CLOCK MINIMUM PULSE WIDTH, An/Bn to CLOCK SETUP AND HOLD TIMES

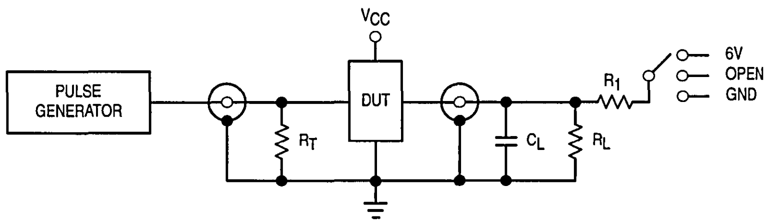
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$ except when noted



WAVEFORM 4 – INPUT PULSE DEFINITION

$t_R = t_F = 2.5ns$, 10% to 90% of 0V to 2.7V

Figure 1. AC Waveforms (continued)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Product Preview

Low-Voltage CMOS 16-Bit Transceiver/Registered Transceiver With Dual Enable

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

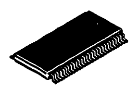
MC74LCX16652

LCX

LOW–VOLTAGE CMOS 16–BIT TRANSCEIVER/ REGISTERED TRANSCEIVER WITH DUAL ENABLE

The MC74LCX16652 is a high performance, non–inverting 16–bit transceiver/registered transceiver operating from a 2.7 to 3.6V supply. The device is byte controlled. Each byte has separate control inputs which can be tied together for full 16–bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16652 inputs to be safely driven from 5V devices. The MC74LCX16652 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes from a LOW–to–HIGH logic level. Output Enable pins ($\overline{\text{OEBAn}}$, OEABn) are provided to control the transceiver outputs. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls (SBAn, SABn) can multiplex stored and real–time (transparent mode) data. In the isolation mode (both outputs disabled), A data may be stored in the B register or B data may be stored in the A register. When in the real–time mode, it is possible to store data without using the internal registers by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input (data retention is not guaranteed in this mode).



DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202–01

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

PIN NAMES

Pins	Function
A0–A15	Side A Inputs/Outputs
B0–B15	Side B Inputs/Outputs
CABn, CBAn	Clock Pulse Inputs
SABn, SBAn	Select Control Inputs
$\overline{\text{OEBAn}}$, OEABn	Output Enable Inputs

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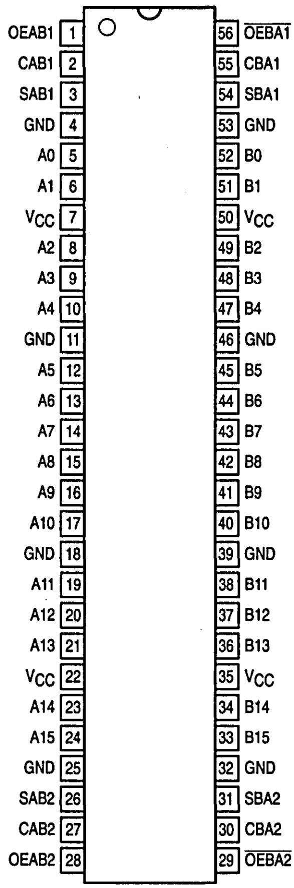
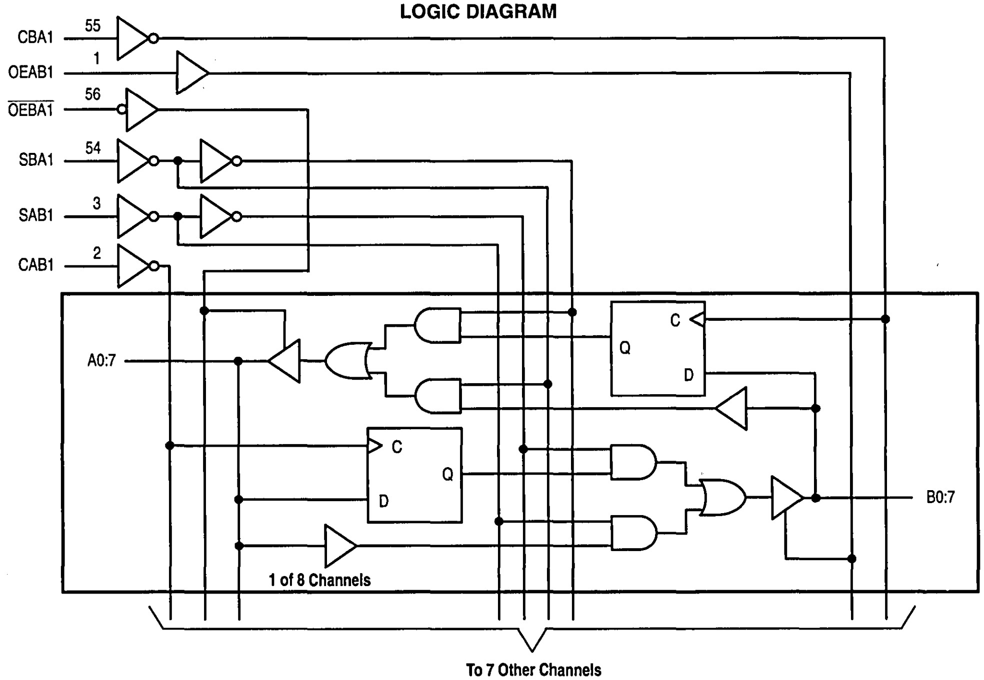
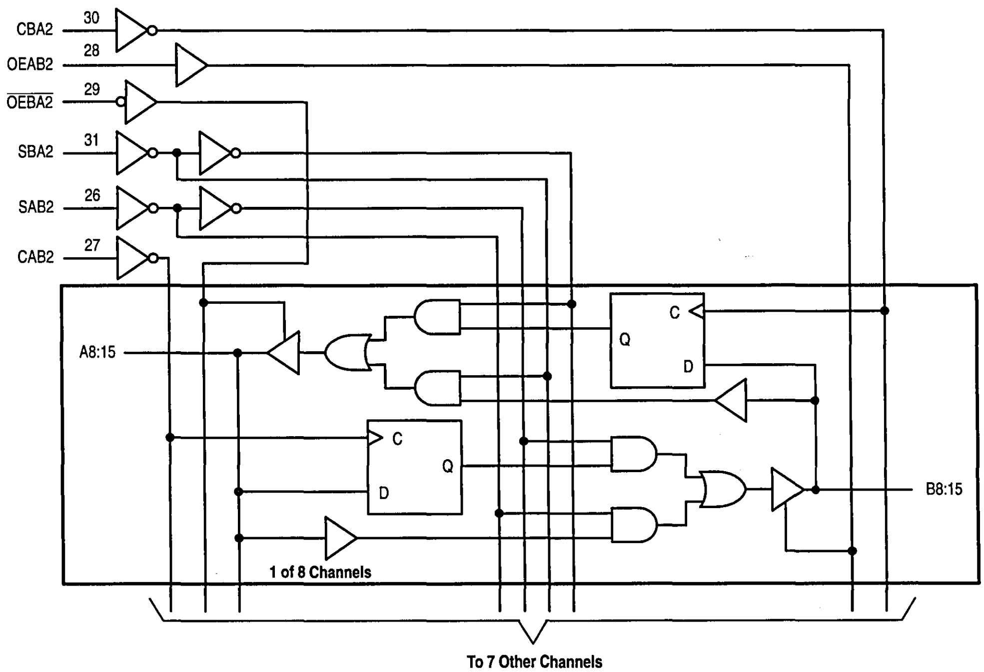

OEAB1 1
CAB1 2
SAB1 3
GND 4
A0 5
A1 6
VCC 7
A2 8
A3 9
A4 10
GND 11
A5 12
A6 13
A7 14
A8 15
A9 16
A10 17
GND 18
A11 19
A12 20
A13 21
VCC 22
A14 23
A15 24
GND 25
SAB2 26
CAB2 27
OEAB2 28
56 OEBA1
55 CBA1
54 SBA1
53 GND
52 B0
51 B1
50 VCC
49 B2
48 B3
47 B4
46 GND
45 B5
44 B6
43 B7
42 B8
41 B9
40 B10
39 GND
38 B11
37 B12
36 B13
35 VCC
34 B14
33 B15
32 GND
31 SBA2
30 CBA2
29 OEBA2

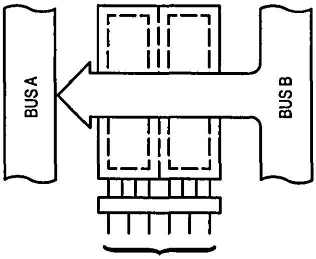
LOGIC DIAGRAM





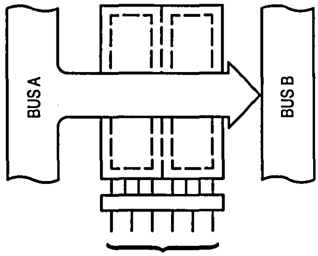
BUS APPLICATIONS

Real Time Transfer – Bus B to Bus A



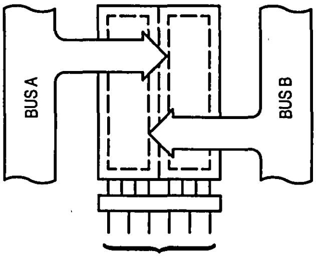
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA
L	L	X	X	X	L

Real Time Transfer – Bus A to Bus B



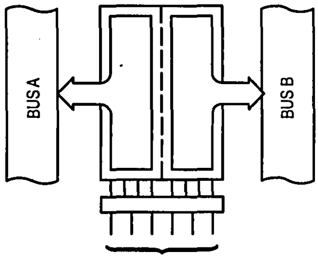
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA
H	H	X	X	L	X

Store Data from Bus A, Bus B or Bus A and Bus B



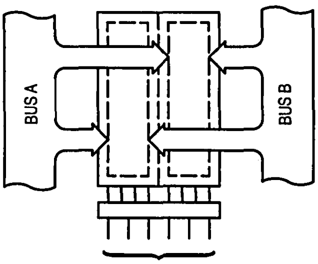
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Transfer A Stored Data to Bus B or Stored Data Bus B to Bus A or Both at the Same Time



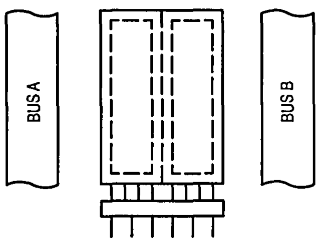
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H

Store Bus A in Both Registers or Store Bus B in Both Registers



OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA
H	H	↑	↑	L	X
L	L	↑	↑	X	L

Isolation



OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA
L	H	H or L	H or L	X	X

FUNCTION TABLE

Inputs						Storage Registers		Data Ports		Operating Mode
$\overline{OEBAn}$	OEABn	CABn	CBAn	SABn	SBAn	Q_A	Q_B	A_n	B_n	
H	L							Input	Input	
		‡	‡	X	X	NC	NC	X	X	Isolation, Hold Storage
		↑	↑	X	X	L H X X	X X L H	L H X X	X X L H	Store A and/or B Data
H	H							Input	Output	
		‡	X*	L	X	NC NC	NC NC	L H	L H	Real Time A Data to B Bus
				H	X	NC	NC	X	Q_A	Stored A Data to B Bus
		↑	X*	L	X	L H	NC NC	L H	L H	Real Time A Data to B Bus; Store A Data
				H	X	L H	NC NC	L H	Q_A Q_A	Stored A Data to B Bus; Store A Data
L	L							Output	Input	
		X*	‡	X	L	NC NC	NC NC	L H	L H	Real Time B Data to A Bus
				X	H	NC	NC	Q_B	X	Stored B Data to A Bus
		X*	↑	X	L	NC NC	L H	L H	L H	Real Time B Data to A Bus; Store B Data
				X	H	NC NC	L H	Q_B Q_B	L H	Stored B Data to A Bus; Store B Data
L	H							Output	Output	
		‡	‡	H	H	NC	NC	Q_B	Q_A	Stored A Data to B Bus, Stored B Data to A Bus

H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = Low–to–High Clock Transition; ‡ = NOT Low–to–High Clock Transition; NC = No Change; * = The clocks are not internally gated with either the Output Enables or the Source Inputs. Therefore, data at the A or B ports may be clocked into the storage registers, at any time. For I_{CC} reasons, Do Not Float Inputs.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$[1]	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage — (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			12	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		$V_{CC} = 2.7V$; $I_{OH} = -12mA$	2.2		
		$V_{CC} = 3.0V$; $I_{OH} = -18mA$	2.4		
		$V_{CC} = 3.0V$; $I_{OH} = -24mA$	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		$V_{CC} = 2.7V$; $I_{OL} = 12mA$		0.4	
		$V_{CC} = 3.0V$; $I_{OL} = 16mA$		0.4	
		$V_{CC} = 3.0V$; $I_{OL} = 24mA$		0.55	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		20	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	µA

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.

AC CHARACTERISTICS[1] ($t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits $T_A = -40°C$ to $+85°C$ $V_{CC} = 3.0V$ to $3.6V$ Min	Max	$V_{CC} = 2.7V$ Min	Max	Unit
f_{max}	Clock Pulse Frequency	3	170				MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	3	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	5.0 5.0	1.5 1.5	6.0 6.0	ns
t_{PLH} t_{PHL}	Propagation Delay Select to Output	1	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_s	Setup Time, HIGH or LOW Data to Clock	3	2.5		2.5		ns
t_h	Hold Time, HIGH or LOW Data to Clock	3	1.5		1.5		ns
t_w	Clock Pulse Width, HIGH or LOW	3	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)			1.0 1.0			ns

1. These AC parameters are preliminary and may be modified prior to release.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

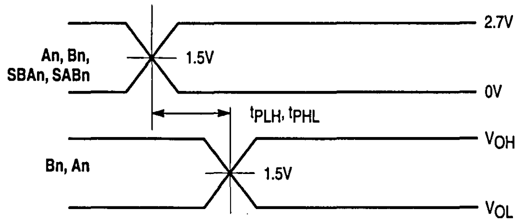
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25°C$ Min	Typ	Max	Unit
V_{OLP}	Dynamic LOW Peak Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage[1]	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

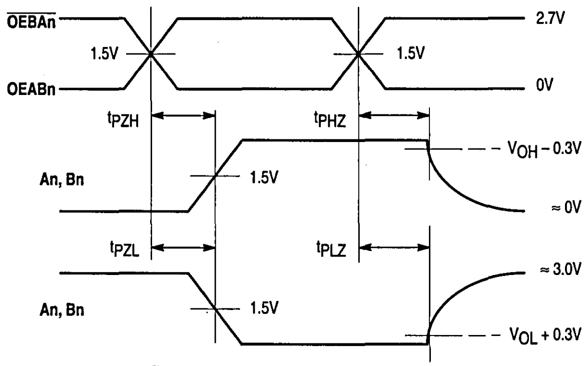
1. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state. The LCX16652 is characterized with 15 outputs switching with 1 output held LOW.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	20	pF
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF

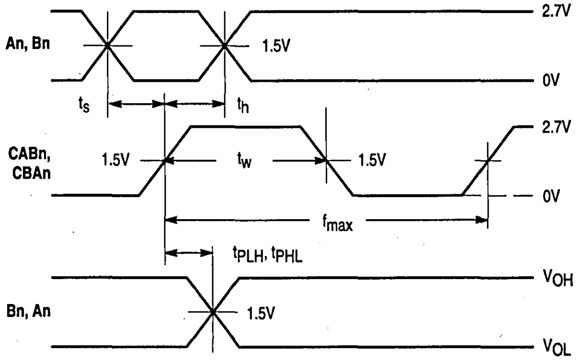


WAVEFORM 1 – SAB to B and SBA to A, An to Bn PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



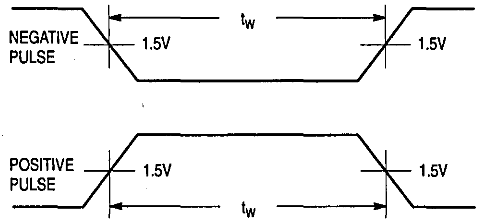
WAVEFORM 2 – $\overline{OEBA}$/OEAB to An/Bn OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 1. AC Waveforms



WAVEFORM 3 – CLOCK to Bn/An PROPAGATION DELAYS, CLOCK MINIMUM PULSE WIDTH, An/Bn to CLOCK SETUP AND HOLD TIMES

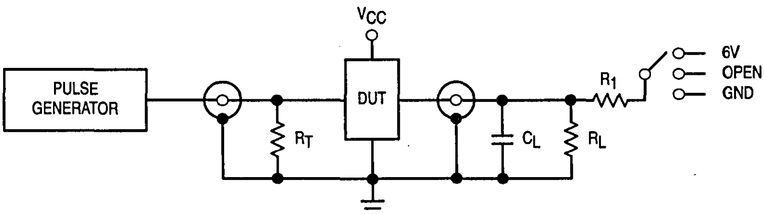
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$ except when noted



WAVEFORM 4 – INPUT PULSE DEFINITION

$t_R = t_F = 2.5ns$, 10% to 90% of 0V to 2.7V

Figure 1. AC Waveforms (continued)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

Reliability Information

Motorola Reliability and Quality Assurance

Motorola has a long standing reputation for manufacturing products of excellent Quality and Reliability since the introduction of the first car radio in 1928. This has helped Motorola to become one of the largest corporations exclusively devoted to electronics.

In today's semiconductor marketplace, two important elements for the success of a company are its quality and reliability systems. They are interrelated, reliability being quality extended over the expected life of a product. For any manufacturer to remain in business, its products must meet or exceed basic quality and reliability standards and customer needs.

At Motorola, the most stringent and demanding definitions of quality and reliability are used.

Quality

- Reduction of variability around a target so that conformance to customer requirements and expectations can be achieved in a cost–effective way
- The probability that a device (equipment, parts) will have performance characteristics within specified limits
- Fitness for use

Reliability

- Quality in time and environment
- The probability that our semiconductor devices, which initially have satisfactory performance, will continue to perform their intended function for a given time in usage environments

At Motorola, our Reliability and Quality Assurance Program is designed to generate ongoing data for both reliability and quality for the various product families. Both reliability and quality monitors are performed on the different major categories of semiconductor products. These monitors are designed to test the product's design and material as well as to identify and eliminate potential failure mechanisms to ensure reliable device performance in a "real world" application. Thus, the primary purpose of the program is to identify trends from generated data, so if need be, corrective action(s) can be taken toward improving performance. In addition, this reliability and quality data can be utilized by our customers for failure rate predictions.

It is the explicit purpose of this communication to inform the customer of our LCX qualification results. In addition, we have provided a general definition of our reliability and quality assurance program.

LCX Device Description

Motorola's LCX family, the first Low–Voltage CMOS family with 5V tolerant inputs and outputs, is manufactured on the H4C "plus" 75% CMOS (double layer metal) process at MOS 6. The LCX family emphasizes low power, low switching noise, and fast switching speeds. LCX devices will be assembled in SOIC, SSOP and TSSOP packages. The H4C "plus" 75% CMOS process in MOS 6 was qualified using the LCX family's E76S maskset.

LCX Processing Information

PROCESSING SUMMARY — H4C "plus," 75% CMOS (Double Layer Metal)

General	
Process Type	CMOS on EPI
Effective Channel Length	Min. target=0.65μm
Process Complexity	Single Poly, Double Metal
Gate Processing	
Gate Oxide Thickness	150Å
Gate Terminal	Phosphorous Doped Polysilicon (POCL)
N+ Source Drain Dopant	Phosphorous & Arsenic
P+ Source Drain Dopant	Boron (BF2)
Metallization Processing	
Metal Composition	AlSiCu w/TiN Barrier (M1) AlSiCu (M2)
Passivation Processing	
Passivation Type	Double Layer, Nitride over PSG Oxide
Electrical Characteristics	
Field Threshold Voltage	>12V
Punchthrough Voltage	>12V
Gate Oxide Breakdown	>14V

LCX Qualification Introduction

LCX Qualification consisted of intrinsic and extrinsic reliability testing. Intrinsic reliability concerns device degradation issues and is assessed via electromigration, hot carrier injection and dielectric breakdown measures. Extrinsic reliability addresses both processing and packaging related issues and utilizes several tests: high temperature bias, temperature cycling, pressure temperature humidity, thermal shock, temperature humidity bias, surface mount preconditioning, physical dimensions, solderability and marking permanency. (Included below are definitions of the aforementioned terms.)

INTRINSIC RELIABILITY

Electromigration

Electromigration is the movement of metal in the direction of electron flow. This is accelerated by high current densities and temperatures which result in metal void and/or collection (hillock) formations, and ultimately shorts. Design rules specify minimum metal widths and maximum current densities to circumvent electromigration issues.

Hot Carrier Injection (HCI)

Hot carrier injection is the result of electron scattering and subsequent trapping in the gate oxide of MOS devices. Scattering is a function of electron velocity and thus electric fields and temperature. Ultimately, carrier mobility and transconductance are reduced causing threshold voltage shifts. Processing conditions are set to minimize hot carrier generation rates and gate trapping efficiencies.

Dielectric Breakdown

Dielectric breakdown results in the formation of a conductive path connecting once–isolated conducting layers. High voltage induced charge injection and trapping accelerates this breakdown. Dielectric integrity is maximized via uniform depositional thickness, and dielectric quality is achieved through minimizing impurity, charge, and defect levels.

EXTRINSIC RELIABILITY

High Temperature Bias (HTB)

High temperature bias (HTB) testing is performed to accelerate failure mechanisms which are activated through the application of elevated temperatures and the use of biased operating conditions. The temperature and voltage conditions used in the stress are dependent on the product under stress. However, the typical ambient temperature is 145°C with the static bias applied equal to or greater than the data sheet nominal value.

Temperature Cycling (MIL–STD–833D–1010C)

Temperature cycle testing accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed per MIL–STD–883D Method 1010C with the minimum and maximum temperatures being –65°C and +150°C, respectively. During temperature cycle testing, devices are inserted into a cycling system and held at the cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minute minimum time period. The system employs a circulating air environment to assure rapid stabilization at the specified temperature. The dwell at each extreme, plus the two transition times of five minutes each (one up to the hot dwell temperature, another down to the cold dwell temperature), constitute one cycle.

Thermal Shock (MIL–STD–833D–1010C)

The objective of thermal shock testing is the same as that for temperature cycle testing, that is, to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides additional stress, in that the device is exposed to a sudden change in temperature due to a maximum transfer time of ten seconds, as well as the increased thermal conductivity of a liquid ambient. This test is typically performed per MIL–STD–883D Method 1011C with minimum and maximum temperatures being –65 °C to +150 °C, respectively. Devices are placed in a bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes minimum, the devices are transferred to an adjacent chamber at the maximum specified temperature for an equivalent time. Two five minute dwells plus two ten second transitions constitute one cycle.

Temperature Humidity Bias (THB Motorola Std)

This stress is performed to accelerate the effects of moisture penetration, with the dominant effect being corrosion. Conditions employed during this test are a temperature of 85°C, humidity of 85% RH, and a nominal bias level.

Pressure Temperature Humidity (PTH Motorola Std)

This stress is performed to accelerate the effects of moisture penetration, with the dominant effect being corrosion. This test detects similar failure mechanisms as THB but at a greatly accelerated rate. Conditions employed during this test are a temperature of 121°C, pressure of 15psig or greater, humidity of 100% RH, unbiased.

Surface Mount Preconditioning (Motorola Std)

Preconditioning tests are performed to simulate the customer board mount process where surface mount parts are subjected to a high temperature for a short duration. These tests detect mold compound delamination from the die and leadframe which can result in reliability failures. The dominant failure mechanism is corrosion, but other stress–related problems could also occur like fractured wirebonds, passivation cracks, smeared metal on die, etc.

The conditions typically used are 245°C for IR reflow and 260°C for solder immersion. For small pitch packages, a 260°C oil immersion is substituted for the 260°C solder to avoid solder bridging of the leads.

Physical Dimensions (MIL–STD–883D–2016)

The purpose of this test is to verify the external dimensions of the device are in accordance with the case outline specification. This test is typically performed per MIL–STD–883D Method 2016.

Solderability (MIL–STD–883D–2003)

The purpose of this test is to determine the solderability of all terminations which are normally joined by a soldering operation. This test is typically performed per MIL–STD–883D Method 2003. The test verifies the ability of these terminations to be wetted or coated by solder, and to predict suitable fillet when dip soldered. An accelerated aging test is included in this method which simulates a minimum of six months natural aging under a combination of various storage conditions that have a deleterious effect on the solderability.

Marking Permanency (Motorola Std)

The purpose of this test is to verify the device markings will not become illegible when subjected to solvents, and the solvents will not cause any mechanical, electrical, damage or deterioration, of the materials or finishes. This test is typically performed per Motorola standard.

Process Qualification Information

PROCESS QUALIFICATION SUMMARY

The H4C "plus" 75% CMOS (double layer metal) process qualification consisted of intrinsic reliability testing (Electromigration, Hot Carrier Injection, and Dielectric Breakdown) and extrinsic reliability testing (High Temperature Bias, Temperature Cycling, and Pressure Temperature Humidity).

The intrinsic reliability measures indicate no significant degradation over the lifetime of the device. Extrinsic reliability for the process resulted in zero failures.

INTRINSIC RELIABILITY RESULTS

DEVICE QUALIFICATION

Electromigration

Electromigration evaluation of MOS 6 metals used in the H4C "plus" 75% CMOS (double layer metal) process revealed an acceptable metallization process for a minimum lifetime of 10 years at 100°C with $\leq$ .01% cumulative failures.

Hot Carrier Injection

HCI test (low temperature electrical stress) results indicate less than 10% change in transconductance over the lifetime of the transistor.

Dielectric Breakdown

The current conduction and QBD (charge breakdown) data taken in MOS 6 was used to calculate an intrinsic gate oxide lifetime of 1364 years. This estimated lifetime greatly exceeds the expected lifetime of the device.

EXTRINSIC RELIABILITY RESULTS/DATA

PROCESS QUALIFICATION

The reliability testing consisted of High Temperature Bias (145°C, 3.6V bias), Temperature Cycling (–65°C to 150°C), and PTH (121°C, 15PSIG, & 100% RH). Samples from three wafer lots were tested.

One wafer lot was a metal/dielectric split lot. The metal and dielectric layers were run at the maximum and minimum thickness specifications in order to account for step coverage extremes.

The second wafer lot was a Vt/Leff split lot. The Vt and Leff were run at minimum and maximum specifications in order to account for extremes in leakage, speed, and translation window.

The remaining lot was a nominal lot. Zero process related rejects occurred after 504 hours of op–life, 600 temp cycles, and 240 hours of PTH. (The device failure in time (FIT) was calculated based on HTB results at 14.4; stress temp = 145°C; activation energy = 0.7eV).

The H4C "plus" 75% CMOS (double layer metal) process in MOS 6 was qualified and approved in light of the results of the above intrinsic and extrinsic reliability results.

Package Qualification

MC74LCX family is being offered in SOIC, SSOP and TSSOP packaging. As the TSSOP package is a newer technology, a qualification summary has been included in this report. All reliability tests have passed successfully, including preconditioning tests used to simulate customer board mount processes (see below). Furthermore, based on reliability results, drypack is not required for this package type.

Package Qualification Summary

TSSOP leads	Op Life	Temperature Cycle	Thermal Shock	THB	Surface Mount Preconditioning	Solderability	Marking Permanency	Physical Dimension
14	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
16	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
20	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

Summary Package Information

• Package Material	Hitachi CEL 9200N
• Leadframe Material	Copper
• Plating	80/20 tin/lead solder plate
• Die Attach Epoxy	Sumitomo CRM 1033B
• Wire Bond Material	1.0 mil gold
• Wire Bond Method	Thermosonic Ball
• Theta JA (20 ld TSSOP)	140 Deg C/W
• 14–/16–Lead Flag Size	83 x 93 mils
• 20–Lead Flag Size	83 x 120 and 110 x 120 mils

Reliability Audit Program Summary

The Motorola Logic Reliability Audit Program (RAP) is designed to monitor the ability of Logic products to exceed minimum acceptable reliability standards. Mesa Reliability Engineering has overall responsibility for RAP, including updating requirements, interpreting results, offshore administration, and monthly reporting.

Testing

RAP is a system of mechanical, environmental, and electrical tests performed periodically on randomly selected samples of standard products. Each sample receives minimum standard tests covering all wafer fab sites, assembly sites, and packages. Within each family, devices are chosen to represent the range of die sizes and functional complexity.

In addition to standard tests, each package type also receives special pre–conditioning tests, the frequency of which is intended to sample every package type and assembly site once per month.

Reliability tests are run at three sites: Mesa, Arizona (LICD); Manila, Philippines (MPI); and Taipei, Taiwan (METL). Following mechanical and electrical testing, devices receive standard static and functional electrical tests using conditions and limits per applicable device specifications.

Failures

All failed devices require recorded data. Failure data and failure verification information accompany all rejects to a product analysis lab where root cause failure analysis is performed on all occurrences observed at that site. All information regarding failed units is logged into a tracking database.

A review is called if any sample has a failure. The findings are analyzed relative to past performance to determine if customers are at risk for abnormally high failure rates. Customer notification may then be required and, if needed, is prepared and distributed. Following the completion of testing and data review, the local reliability engineering group enters all data into the Reliability Audit Program Database.

Thermal Considerations

Prepared by: Lance K. Packer
LCX Application Engineering

Reliability of Plastic Packages

Although today's plastic packages are as reliable as ceramic packages under most environmental conditions, as the junction temperature increases a failure mode unique to plastic packages becomes a significant factor in the long term reliability of the device.

Modern plastic package assembly utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. As the temperature of the silicon (junction temperature) increases, an intermetallic compound forms between the gold and aluminum interface. This intermetallic formation results in a significant increase in the impedance of the wire bond and can lead to performance failure of the affected pin. With this relationship between intermetallic formation and junction temperature established, it is incumbent on the designer to ensure that the junction temperature for which a device will operate is consistent with the long term reliability goals of the system.

Reliability studies were performed at elevated ambient temperatures (125°C) from which an Arrhenius Equation (Eq 1), relating junction temperature to bond failure, was established. The application of this equation yields the values in Table 1. This table relates the junction temperature of a device in a plastic package to the continuous operating time before 0.1% bond failure (1 failure per 1000 bonds).

$$T = 6.376 \times 10^{-9}\, e\left[\frac{11554.267}{273.15 + T_J}\right] \qquad \text{(Eq 1)}$$

Where:
T = Time to 0.1% bond failure

Table 1. Tj vs Time to 0.1% Bond Failure

Junction Temp. (°C)	Time (hours)	Time (yrs.)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.1
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Thermal Management

As in any system, proper thermal management is essential to establish the appropriate trade–off between performance, density, reliability and cost. In particular, the designer should be aware of the reliability implication of continuously operating semiconductor devices at high junction temperatures.

The increasing popularity of surface mount devices (SMD) is putting a greater emphasis on the need for better thermal management of a system. This is due to the fact that SMD packages generally require less board space than their through hole counterparts so that designs incorporating SMD technologies have a higher thermal density. To optimize the thermal management of a system it is imperative that the user understand all of the variables which contribute to the junction temperature of the device.

The variables involved in determining the junction temperature of a device are both supplier and user defined. The supplier, through lead frame design, mold compounds, die size and die attach, can positively impact the thermal resistance and the junction temperature of a device. Motorola continually experiments with new package designs and assembly techniques in an attempt to further enhance the thermal performance of its products.

It can be argued that the user has the greatest control of the variables which commonly impact the thermal performance of a device. Depending on the environment in which an IC is placed, the user could control over 75% of the current that flows through the device. Ambient temperature, air flow and related cooling techniques are the obvious user controlled variables, however, PCB substrate material, layout density, size of the air–gap between the board and the package, amount of exposed copper interconnect, use of thermally–conductive epoxies and number of boards in a box and output loading can all have significant impacts on the thermal performance of a system.

PCB substrates all have different thermal characteristics, these characteristics should be considered when exploring the PCB alternatives. The user should also account for the different power dissipations of the different devices in his system and space them on the PCB accordingly. In this way, the heat load is spread across a larger area and "hot spots" do not appear in the layout. Copper interconnect traces act as heat radiators, therefore, significant thermal dissipation can be achieved through the addition of interconnect traces on the top layer of the board. Finally, the use of thermally conductive epoxies can accelerate the transfer of heat from the device to the PCB where it can more easily be passed to the ambient.

The advent of SMD packaging and the industry push towards smaller, denser designs makes it incumbent on the designer to provide for the removal of thermal energy from the system. Users should be aware that they control many of the variables which impact the junction temperatures and, thus, to some extent, the long term reliability of their designs.

Calculating Junction Temperature

The following equation can be used to estimate the junction temperature of a device in a given environment:

$$T_J = T_A + P_D \Theta_{JA}$$

where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
Θ_{JA} = Avg Pkg Thermal Resistance (Junction Ambient)

$$P_D = V_{CC}\left[\overset{1}{C_P V_{CC}\sum_{i=1}^{s} F_{OUT_i}}\right] + \overset{2}{V_{CC}\,[\Delta I_{CC} n]}$$

$$+ (V_{CC} - V_{OH})\left[\overset{3}{(V_{OH} - V_{OL})\sum_{i=1}^{s} C_{L_i} F_{OUT_i}} + \overset{4}{\sum_{i=1}^{h}\frac{V_{OH}}{R_{D_i}}}\right]$$

$$+ (V_{OL})\left[\overset{5}{(V_{OH} - V_{OL})\sum_{i=1}^{s} C_{L_i} F_{OUT_i}} + \overset{6}{\sum_{i=1}^{l}\frac{(V_{CC} - V_{OL})}{R_{U_i}}}\right]$$

Power Dissipation Equation

The power dissipation equation is made up of five major factors controlled by the user which contribute to increased power dissipation:

1 Frequency of operation (output switching frequency)
2 Input voltage levels
3 Output loading (capacitive and resistive)
4 V_{CC} level
5 Duty cycle

Each of these five factors are addressed in the estimating equation except duty cycle. Duty cycle can be addressed by "weighting" the power dissipation equation terms appropriately.

The first current term is I_{CCD}, with the device unloaded. It is caused by the internal switching of the device. Static I_{CC} is so small for LCX, that when estimating power dissipation, it is ignored.

$$C_P V_{CC} \sum_{i=1}^{s} F_{out_i}$$

This term represents the I_{CC} current with absolutely no load. This measurement is taken without the output pins connected to the board. The C_P for a device is calculated by:

$$C_P = \frac{I_{CC}(@50MHz) - I_{CC}(@1MHz)}{V_{CC}(49MHz)s}$$

"s" is the number of outputs switching. C_P may vary slightly from part to part within a product family.

The next term is from current due to holding the CMOS inputs at V_{CC}–0.6V rather than at the rail voltages. This term becomes insignificant as load and frequency increase.

$$\Delta I_{CC} n$$

ΔI_{CC} is the through current when holding the input High of a device to V_{CC}–0.6V. This value is typically 300μA or less. "n" is the number of inputs held at this level.

The third term is current through the upper structure of the device. It is caused by the external capacitive load and the output frequency. If a capacitive load exists then this term can become very significant.

$$(V_{OH} - V_{OL}) \sum_{i=1}^{s} C_{L_i} F_{OUT_i}$$

V_{OH}–V_{OL} is the voltage swing of the output. C_L is the output load (this could vary from output to output). F_{OUT} is the output frequency which can also vary from output to output.

The fourth term stems from current through the upper structure due to an external resistive load to ground.

As the output frequency increases, the measured current approaches that of static High outputs.

$$\sum_{i=1}^{h} \frac{V_{OH}}{R_{D_i}}$$

R_D is an external pull–down resistor. A different value load could be applied to each output.

The fifth current term is determined by the output capacitive load and the output frequency on the lower structure of the device. If this load exists than this term is also significant.

$$(V_{OH} - V_{OL}) \sum_{i=1}^{s} C_{L_i} F_{OUT_i}$$

All variables are the same as with the third term with the exception that this is current flowing through the lower structure of the IC. This current is not I_{CC}, but rather current that is "sinked" from an external source.

The final term is due to an external load connected to V_{CC}. This term includes both switching and static Low outputs.

$$\sum_{i=1}^{l} \frac{(V_{CC} - V_{OL})}{R_{U_i}}$$

As with term five, this is current that flows through the lower structure of the IC. This current too is not I_{CC}.

Example of Thermal Calculations

Junction temperature can be estimated using the following equation:

$$T_J = (\Theta_{JA} \times P_D) + T_A$$

where:

T_J = Junction Temperature (°C)
Θ_{JA} = Thermal Resistance (Junction–to–Ambient)
P_D = Power Dissipation at a T_J
T_A = Ambient Temperature (°C)

Example of LCX T_J Calculation

1. Calculate Current Consumption:

For example, the LCX244's C_P is 25pF. Let V_{CC} = 3V; operating temperature = 85°C; F_{OUT} = 50MHz; for 4 outputs switching; hold 2 inputs LOW and 2 inputs HIGH (at V_{CC} – 0.6V); C_L = 100pF; 500Ω pull–down; no pull–up.

$$\overset{1}{\left[25\text{pF} \times 3\text{V} \sum_{i=1}^{4} 50\text{MHz} \right]} + \overset{2}{0.3\text{mA}(2)}$$

=15mA + 0.6mA = 15.6mA

These unloaded terms contribute only 10% of the total I_{CC} current.

$$\overset{3}{(2.8\text{V} - 0.2\text{V}) \sum_{i=1}^{4} 100\text{pF}(50\text{MHz})} + \overset{4}{\sum_{i=1}^{6} \frac{2.8\text{V}}{500\Omega}}$$

= 52mA + 33.6mA = 85.6mA

In this example, terms three and four contribute over 55% of the total I_{CC} current. This part of I_{CC} is entirely due to external loading.

$$\overset{5}{(2.8\text{V} - 0.2\text{V}) \sum_{i=1}^{4} 100\text{pF}(50\text{MHz})} + \overset{6}{\sum_{i=1}^{6} \frac{3\text{V} - 0.2\text{V}}{\infty}}$$

= 52mA + 0 = 52mA

These terms are not I_{CC} currents, but rather currents "sinked" by the lower structure of the device. The total current from all terms is 153.2mA.

2. Finding PD (V x I)

When calculating the total power dissipation of the device, the first two terms are multiplied by V_{CC}, which in this example is

3V(15.6mA) = 46.8mW

The third and fourth terms are multiplied by the voltage drop across the upper structure of the device, V_{CC}–V_{OH}. This is approximately 0.2V.

0.2V(85.6mA) = 17.1mW

The fifth and sixth terms are multiplied by the voltage drop across the lower structure of the device, V_{OL}.

0.2V(52mA) = 10.4mW

The total estimated power dissipation of an LCX 244 with 4 outputs switching, at 85°C, with V_{CC}=3V, with 2 outputs held static Low, and 2 inputs at 2.4V with 100pF capacitive loads, 500Ω pull–downs, and 50MHz switching frequency is:

74.3 mW

3. Θ_{JA} Value

The θ_{JA} for a 20–pin TSSOP is approximately 140°C/W.

4. Final Calculations for T_J for the LCX244

$T_J = (P_D \times \Theta_{JA}) + T_A$ = (0.0743W × 140°C/W) + 85°C = 95.4°C. LCX runs cool — well below the point for reliability worries. Using the Arrhenius Equation (Eq 1 on page 187), the time to 0.1% bond failures is approximately 30 years.

System Considerations

The manner in which an IC package is mounted and positioned in its surrounding environment will have significant effects on operating junction temperatures. These conditions are under the control of the system designer and are worthy of serious consideration in PC board layout and system ventilation and airflow.

Forced–air cooling will significantly reduce Θ_{JA}. Air flow parallel to the long dimension of the package is generally a few percent more effective than air flow perpendicular to the long dimension of the package. In actual board layouts, other components can provide air flow blocking and flow turbulence, which may reflect the net reduction of Θ_{JA} of a specific component.

External heat sinks applied to an IC package can improve thermal resistance by increasing heat flow to the ambient environment. Heat sink performance will vary by size, material, design, and system air flow. Heat sinks can provide a substantial improvement.

Package mounting can affect thermal resistance. Surface mount packages dissipate significant amounts of heat through the leads. Improving heat flow from package leads to ambient will decrease thermal resistance.

- *Metal (copper) traces* on PC boards conduct heat away from the package and dissipate it to the ambient; thus the larger the trace area the lower the thermal resistance.
- *Package stand–off* has a small effect on Θ_{JA}. Boards with higher thermal conductivity (ceramic) may show the most pronounced benefit.
- The use of *thermally conductive adhesive* under SO packages can lower thermal resistance by providing a direct heat flow path from the package to board. Naturally high thermal conductivity board material and/or cool board temperatures amplify this effect.
- *High thermal conductive board material* will decrease thermal resistance. A change in board material from epoxy laminate to ceramic will help reduce thermal resistance.

Conclusion

Thermal management remains a major concern of producers and users of IC's. An increase in Θ_{JA} is the major trade–off one must accept for package miniaturization. When the user considers all of the variables that affect the IC junction temperature, he is then prepared to take maximum advantage of the tools, materials and data that are available.

References

1. "High Performance ECL Data – ECLinPS and ECLinPS Lite," Motorola, pp. 4–32.
2. "Thermal Considerations for Advanced Logic Families; AN241," Philips Semiconductors

Ordering Information

Device Nomenclature

MC 74 LCX YYYY ZZ

Motorola Circuit Identifier — MC

Temperature Range — 74
- 74 = –40 to +85°C

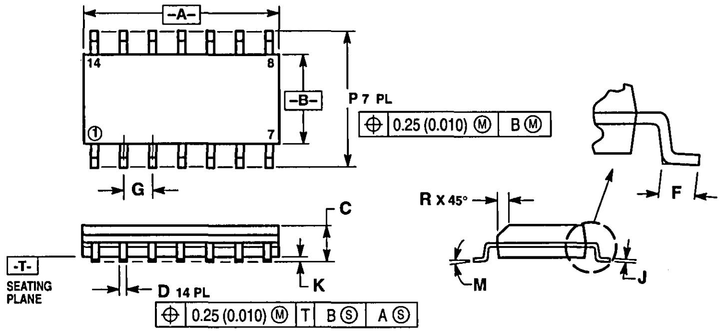
Family Identifier — LCX
- LCX = 5V–Tolerant Low–Voltage CMOS

Function Type — YYYY

Package Type — ZZ
- D = Plastic Narrow JECDEC SOIC
- DW = Plastic Wide JEDEC SOIC
- M = Plastic EIAJ SOIC
- SD = Plastic SSOP
- DT = Plastic TSSOP

Case Outlines

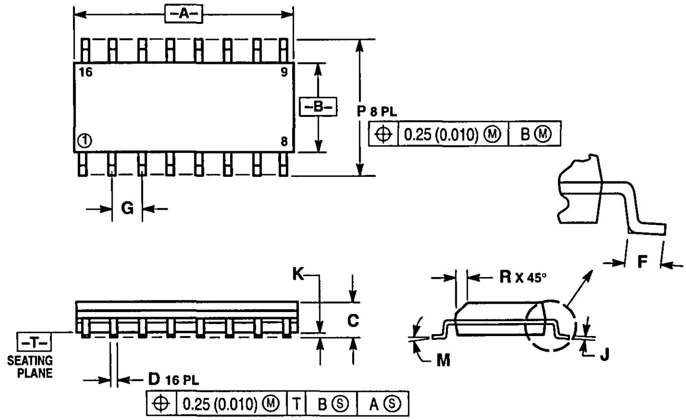
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

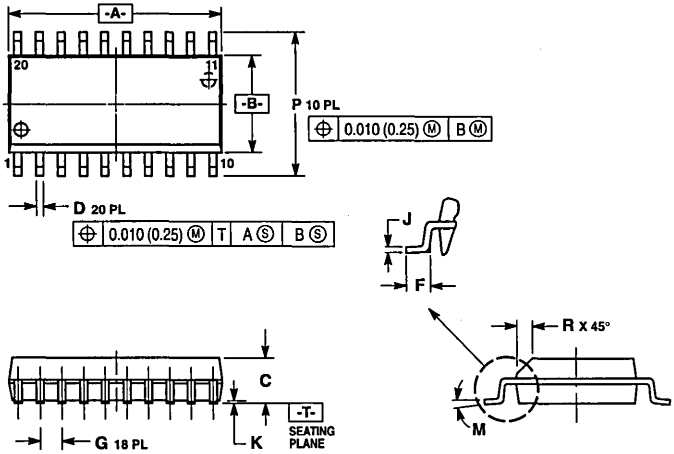
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

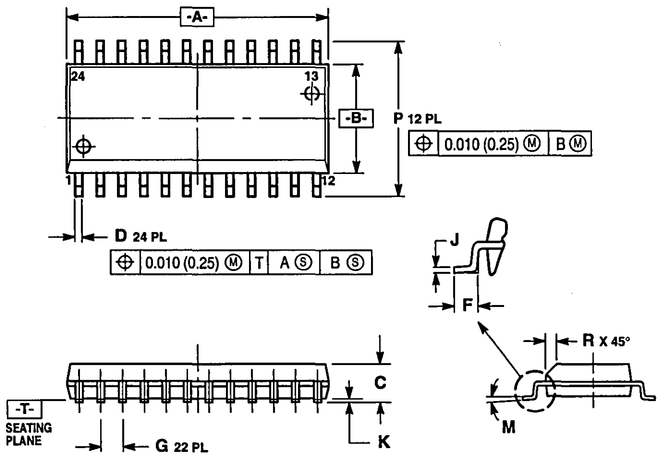
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

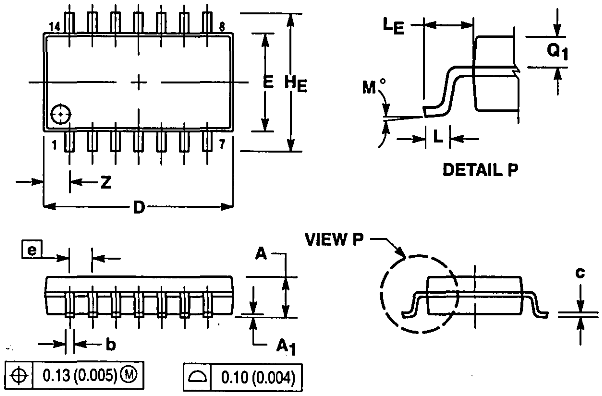
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

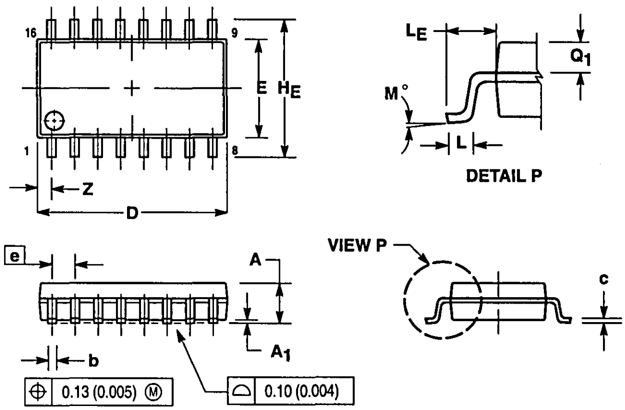
M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 965–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 966–01
ISSUE O



NOTES:
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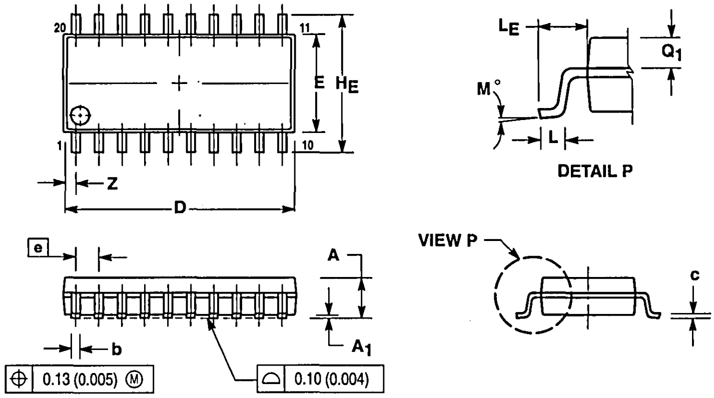
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

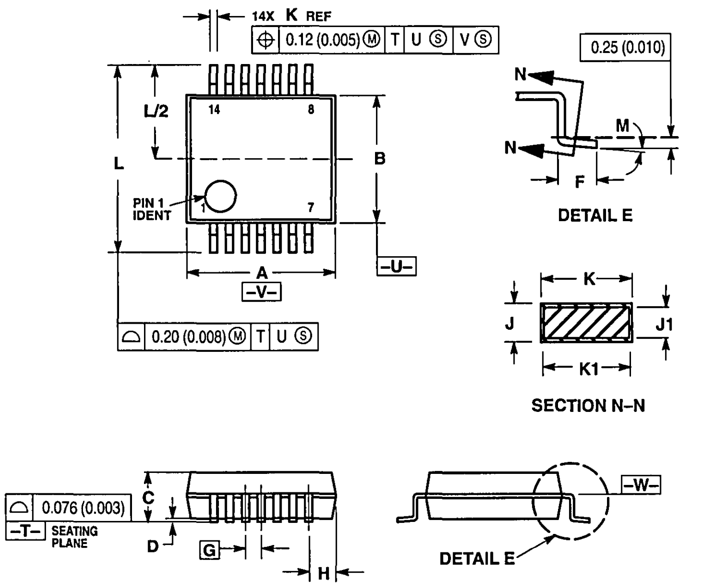
M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 967–01
ISSUE O



NOTES:
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5 THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

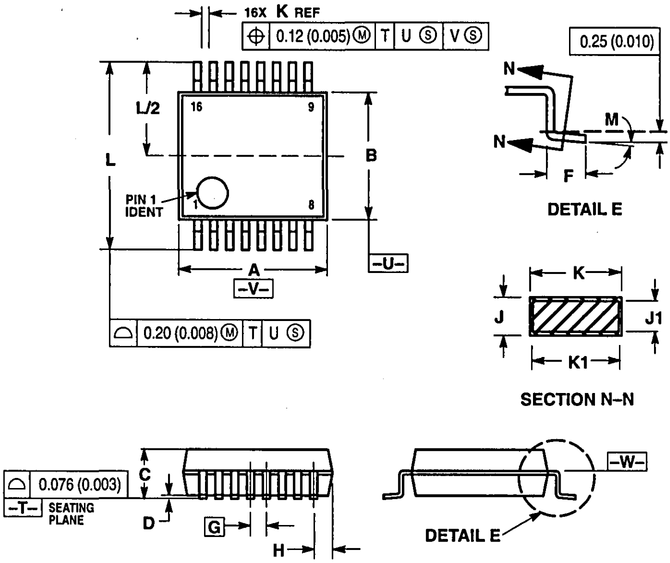
SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940A–03
ISSUE B



NOTES:
6 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
7 CONTROLLING DIMENSION: MILLIMETER.
8 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
9 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
10 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
11 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
12 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.07	6.33	0.238	0.249
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	1.08	1.22	0.042	0.048
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

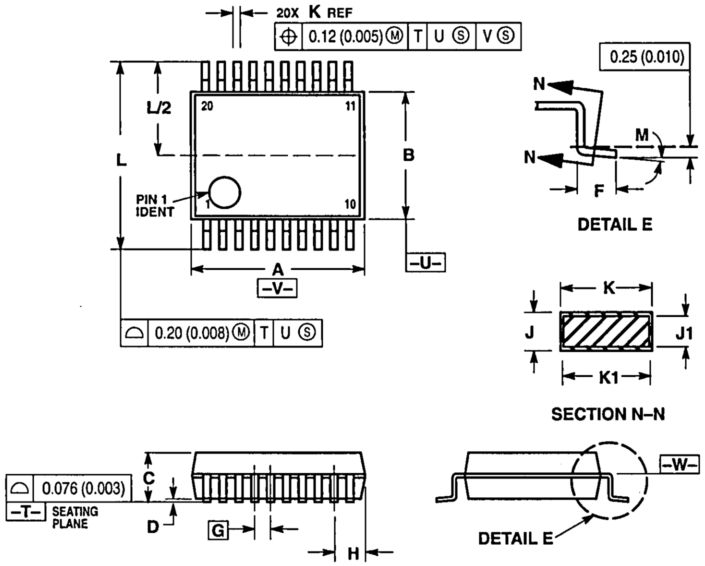
SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940B–03
ISSUE B



NOTES:
13 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
14 CONTROLLING DIMENSION: MILLIMETER.
15 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
16 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
17 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
18 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
19 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.07	6.33	0.238	0.249
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.73	0.90	0.028	0.035
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

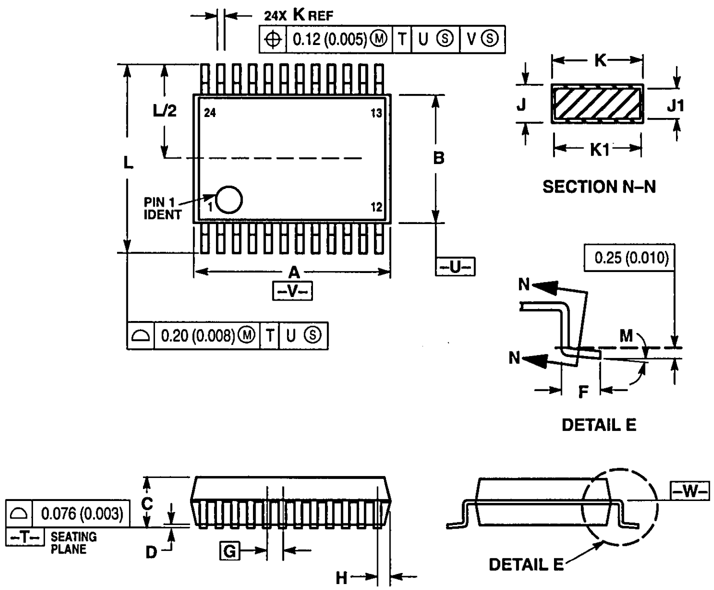
SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940C–03
ISSUE B



NOTES:
20 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
21 CONTROLLING DIMENSION: MILLIMETER.
22 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
23 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
24 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
25 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
26 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.07	7.33	0.278	0.288
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.59	0.75	0.023	0.030
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

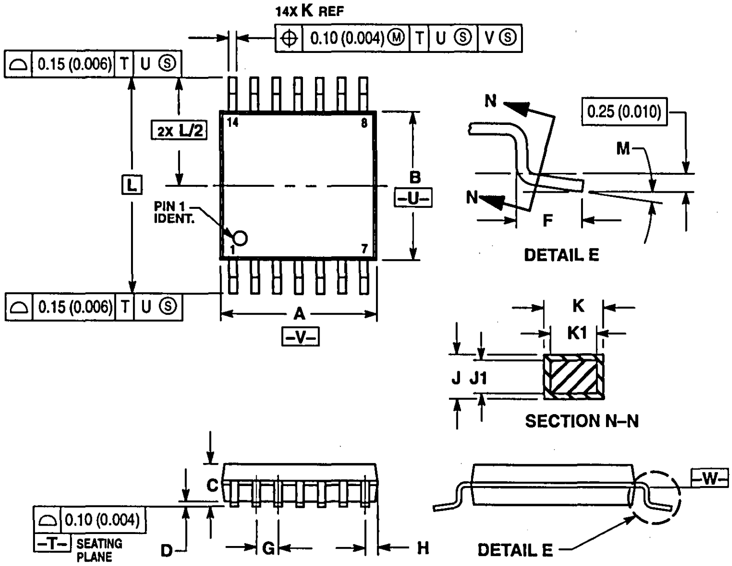
SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940D–03
ISSUE B



NOTES:
27 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
28 CONTROLLING DIMENSION: MILLIMETER.
29 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
30 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
31 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
32 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
33 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.07	8.33	0.317	0.328
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.44	0.60	0.017	0.024
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

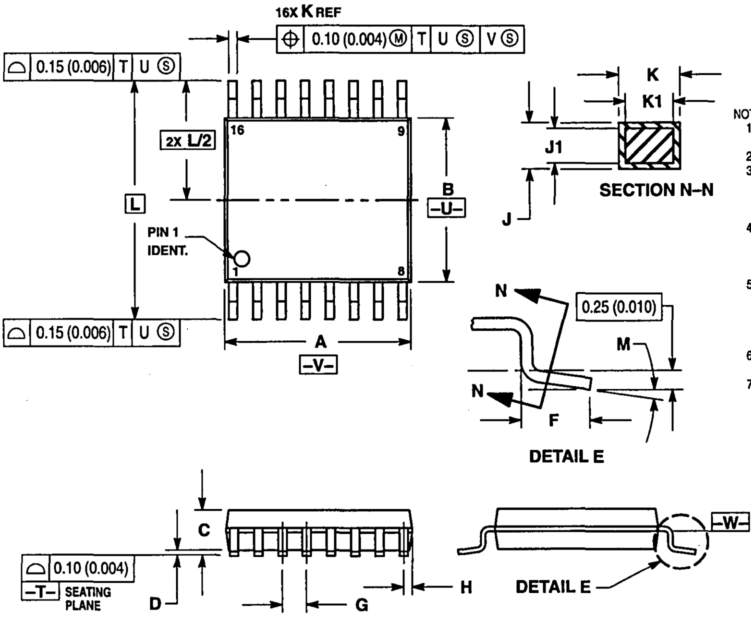
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948G–01
ISSUE O



NOTES:
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

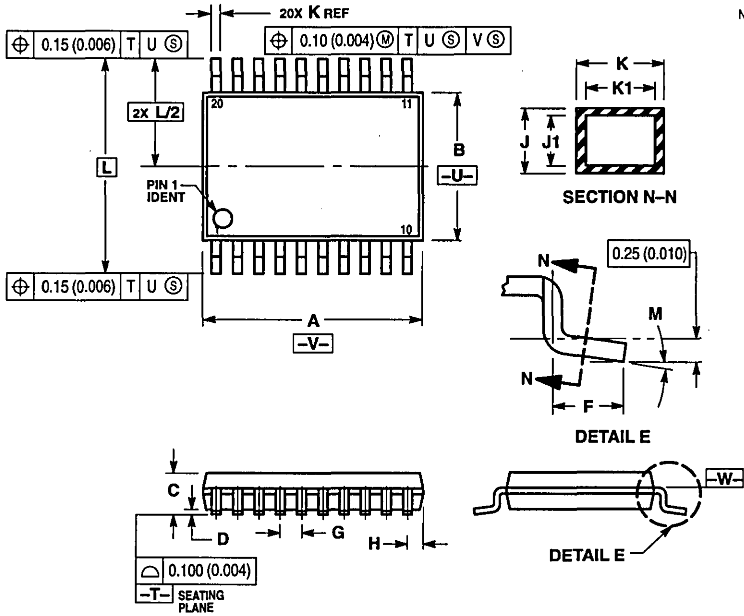
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

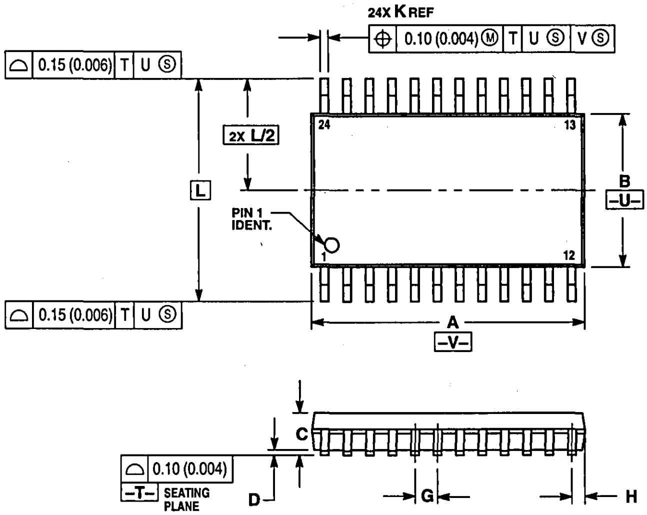
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A

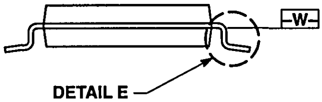


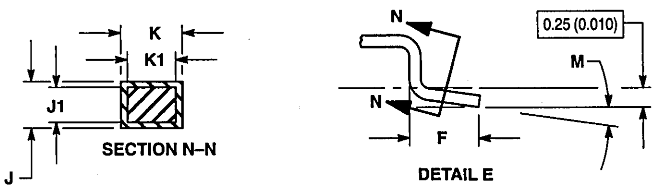
NOTES:
8. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
9. CONTROLLING DIMENSION: MILLIMETER.
10. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
11. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
12. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
13. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
14. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948H–01
ISSUE O



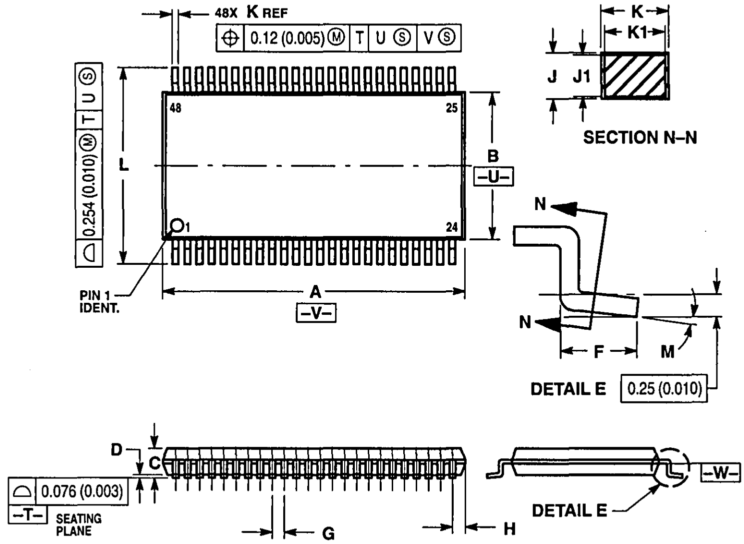




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

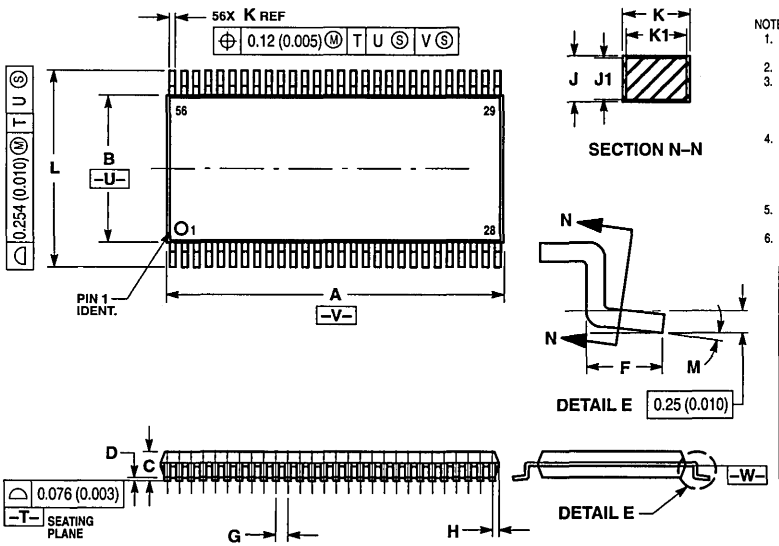
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1201–01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	—	1.10	—	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	—	0.015	—
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202–01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	13.90	14.10	0.547	0.555
B	6.00	6.20	0.236	0.244
C	—	1.10	—	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.12	—	0.005	—
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

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