DP83916EB-AT: High Performance AT Compatible Bus Master Ethernet® Adapter Card

National Semiconductor
Application Note 855
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INTRODUCTION

The DP83916EB-AT board is a high performance 16-bit Ethernet adapter card designed for IBM® PC-AT®/compatible computer systems. It employs a unique bus master architecture which transfers packet data at rates up to 10 Megabytes/second to and from the PC-AT's system memory during Ethernet reception and transmission. Featuring the National Semiconductor DP83916 Systems-Oriented Network Interface Controller (SONIC™-16) and the PLX AT9010, the board functions as a bus master adapter card for implementing Ethernet nodes. Its design includes an interface which enables PC-AT managed-hub applications. Furthermore, it supports three types of media for functionality in IEEE 802.3 networks.

By using the DP83916 SONIC-16, the DP83916EB-AT board maximizes bus master performance over existing adapter cards. First, the SONIC-16's highly integrated design eliminates the need for I/O mapped or dual port adapter RAM designs. Second, the SONIC-16's bus master architecture facilitates writing and reading network data directly to and from main system memory. This architecture is supported by the SONIC-16's bus latency tolerance, its link-list buffer management scheme and its 24-bit memory addressing capability.

The PLX AT9010/AT9010B provides a compact, inexpensive and high performance AT bus interface for the DP83916EB-AT adapter card. It integrates much of the AT/SONIC-16 signal decoding and control logic. Because most options are selected by software drivers, the use of jumpers is reduced.

The DP83916EB-AT offers management interface logic to implement a managed hub when the board is coupled with the DP83950EB-AT RICKIT. This interface allows the SONIC-16 to emulate a RIC™ on the Inter-RIC™/Management bus; hence, the SONIC-16 can receive packets containing network data and collision information and also transmit packets over this bus. By using hub management, the DP83916EB-AT makes network statistics available to a manager located anywhere on the network.

Finally, the adapter card offers multiple IEEE 802.3 cable media options: the DP8392 Coaxial Transceiver Interface for Thin Ethernet and an AUI connector for Thick Ethernet or Twisted-Pair.

Use of the DP83916EB-AT adapter card provides a low cost 15-chip bus master Ethernet node that supports three media options for IEEE 802.3 networks. SONIC-16 hub management is included by the addition of only five chips and the DP83950EB-AT RICKIT.

FEATURES

- Efficient NSC DP83916 Systems-Oriented Network Interface Controller (SONIC-16)
- Highly integrated PLX AT9010/B for PC-AT bus master interface
- Inter-RIC/Management bus interface for optional connection to DP83950EB-AT RICKIT
- Selectable media interfaces: Thin Ethernet or AUI for Twisted-Pair and Thick Ethernet
- Optional EPROM for remote system boot
- Four programmable master data transfer speeds including 5, 6.7, 8, and 10 Megabytes/second
- Selectable interrupt lines, bus request channels, adapter card I/O addresses and EPROM memory addresses

HARDWARE OVERVIEW

A block diagram for the DP83916EB-AT board is shown in *Figure 1*. The design can be broken into four sections: slave logic, master logic, hub management and media interface.

The slave logic facilitates the AT's CPU in accessing the SONIC-16's registers, the AT9010's registers, the Ethernet Address ID PROM and the network Boot EPROM (socket). Much of the slave circuitry decode (chip selects) and control logic is implemented in the AT9010. The slave devices are accessed in I/O and memory space.

The bus master logic assists the SONIC-16 in transferring data directly to and from the AT's system memory. It includes all signal translation and control logic required to access the bus, a large portion of which is integrated in the AT9010. The SONIC-16 uses the DMA controller to arbitrate between bus requestors for control of the bus and additional buffers for address and data buses.

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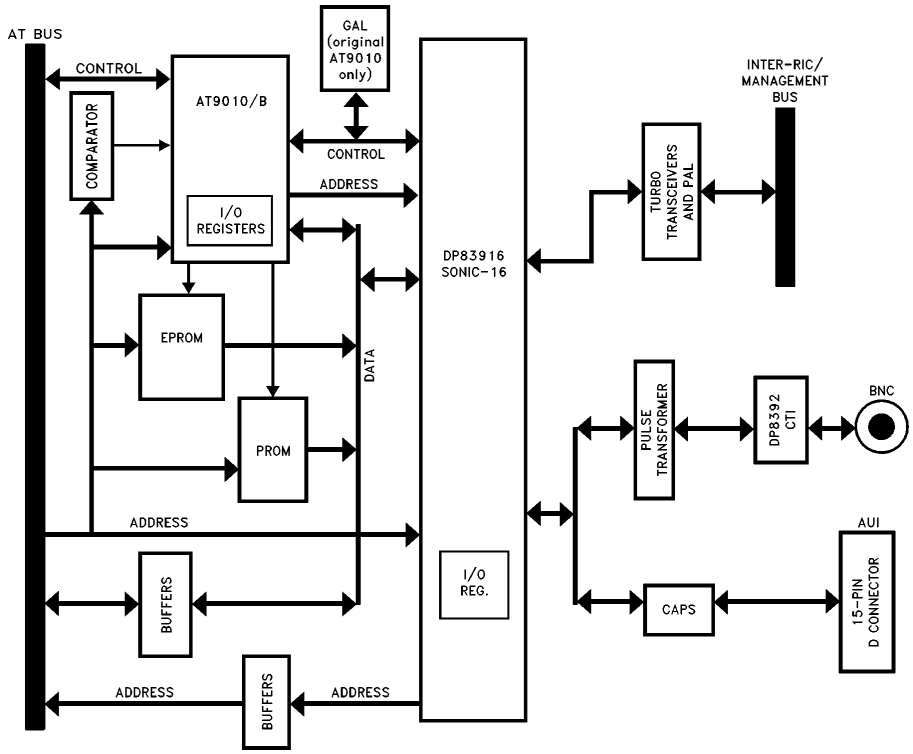

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FIGURE 1. DP83916EB-AT Board Block Diagram

The hub management logic interfaces the Inter-RIC/Management (IR/M) bus and the SONIC-16. The IR/M bus enables the SONIC™ to gather network statistics for packets transmitted from a DP83950EB-AT RIC evaluation board, to receive control packets from remote nodes (managers) and to transmit packets to the network. The logic includes turbo transceivers (BTLs) for driving signals, a PAL® for IR/M bus arbitration signals and a flip-flop which provides the IR/M transmit clock.

The media interface connects the adapter card to one of three network media choices: Coax for 10BASE2 (Thin Ethernet) and AUI for 10BASE5 (Thick Ethernet) and 10BASE-T (Twisted-Pair).

Connection requirements for each choice will be described later.

The DP83916EB-AT supports two versions of the PLX interface chip for the SONIC-16 and the PC-AT platform: the original AT9010 and the AT9010B. If the board is populated with the AT9010, a GAL (U11) is required to fix bugs in the AT9010 chip. The bugs are corrected in the AT9010B and adapter cards containing this version of the chip **should not** have a GAL placed in the socket for U11. (Note, all subsequent references in this application note to ''AT9010'' apply to both versions of the chip unless specified otherwise.)

Since the GAL is not populated when the AT9010B is populated, signals driven from the AT9010B into the GAL will have no effect.

The appendices at the end of this application note provide the following information: Appendix I—PAL and GAL equations, Appendix II—Bill of Materials (BOM), Appendix III—AT9010/AT9010B Register Descriptions, Appendix IV—Signal Descriptions, Appendix V— DP83916EB-AT Card Layout, Appendix VI—Test Pin Layout, Appendix VII—Design Change Recommendation and Appendix VIII—Compatibility Testing. In addition, a detailed schematic for the DP83916EB-AT adapter card is also located at the end of this application note.

SLAVE LOGIC SECTION

During slave cycles, the AT's CPU accesses one of the four slave devices on the card: the SONIC-16's 64 internal registers, the Ethernet address PROM, the AT9010's five internal registers or the boot EPROM. Slave mode also includes card initialization.

The AT9010 provides chip select/control and signal conversion logic. Its configuration registers specify I/O address mapping and SONIC-16 register select information, EPROM memory address decoding and interrupt line specification.

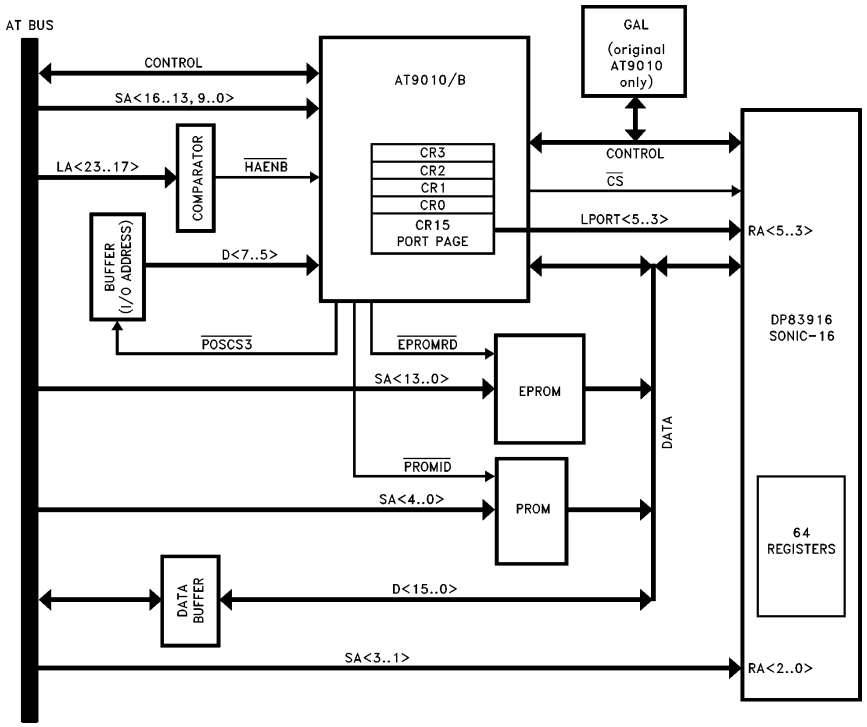

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FIGURE 2. Slave Logic Block Diagram

I/O MAPPING

The SONIC-16 registers, AT9010 registers and Ethernet address PROM reside in the PC-AT's I/O space. The AT9010 offers a choice of seven 32-byte I/O blocks (shown in Table I) to place the card within I/O space. The user can map the board into any one of these blocks by selecting an unused portion of I/O space and positioning jumpers JP1–JP3 accordingly. A shorted jumper corresponds to a 0 and an open jumper corresponds to a 1. The values of these jumpers are enabled onto the data bus during power up and subsequently initialize the AT9010's Configuration Register 1, bits 7, 6, and 5.

TABLE I. I/O Space Mapping

JP1	JP2	JP3	CR1 Bits<7..5>	I/O Address (Hex)
0	0	0	000	100–11F
0	0	1	001	120–13F
0	1	0	010	140–15F
0	1	1	011	160–17F
1*	**0***	**0***	**100**	**300–31F***
1	0	1	101	320–33F
1	1	0	110	340–35F
1	1	1	111	340–35F

* DP83916EB-AT default setting

0 = short (jumper on), 1 = open (jumper off)

The actual mapping of the SONIC-16 registers, AT9010 registers, PROM and SONIC-16 paging register into one of the 32-byte blocks of I/O space is shown in *Figure 3*. Bytes 2–5 are the AT9010's Configuration Registers 0–3, bytes 8–13 are the Ethernet address PROM, byte 15 is AT9010's Configuration Register 15, and bytes 16–32 are the SONIC-16's registers. All other bytes are reserved.

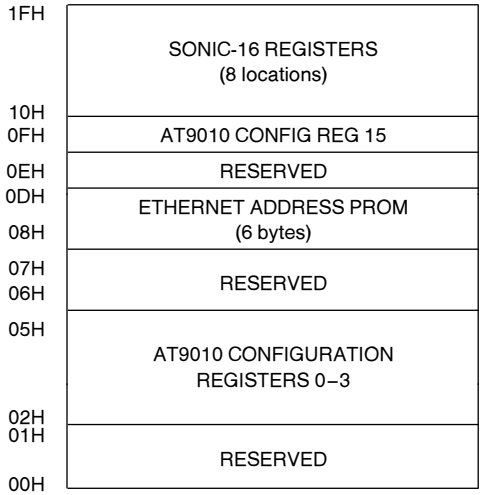

FIGURE 3. Card 32-Byte I/O Space Map

SONIC-16 AND AT9010 REGISTER ACCESS

Due to limited PC-AT I/O space, only eight of the SONIC-16's 64 registers are accessible at any one time. The DP83916EB-AT accommodates this by partitioning the SONIC-16's registers into eight pages of eight registers (16-bit locations).

To access the registers, the CPU must drive a 6-bit register address. First, the CPU sets up the page number (0 to 7) by executing an 8-bit I/O write cycle of D<5. .3> to the AT9010's Configuration Register 15, bits<5. .3>. These data bits drive the three most significant SONIC-16 register address bits RA<5. .3>. Then, the CPU executes a 16-bit I/O read or write cycle using the PC-AT's lower address lines SA<3. .1 > to drive the SONIC-16's address bits RA<2. .0> which select the appropriate register. This completes the SONIC-16 register access. Note, most SONIC-16 register accesses actually require only one I/O cycle because the SONIC-16 registers which are accessed most often are located on Page 0.

The AT9010 configuration registers are 8 bits wide and are read or written through standard 8-bit I/O cycles.

PROM AND EPROM MEMORY MAPPING

The PROM is a 32-byte register which holds a unique 6-byte Ethernet ID Address in offset locations 08H–0DH. It is read by 8-bit I/O read cycles.

The optional boot EPROM (socket), which resides in the PC's BIOS memory space, is also an 8-bit device. If used, the EPROM can be programmed with instructions that are scanned on power-up and enable a diskless workstation to boot up remotely from a network, then access a server.

The boot EPROM can be memory mapped above 640k within the first megabyte of memory. Specifically, the AT9010 places the EPROM in a section of memory within the 0C0000H to 0DFFFFH address range. As shown in *Figure 4*, the upper address decode bits for LA<23. .17> are predetermined by the AT9010. To complete the base address, the decode bits for SA<16. .13> must be programmed by the user in Configuration Register 2. The AT9010 can be configured for an 8k, 16k or 32k EPROM.

During EPROM memory accesses, address lines LA<23. .17> are decoded to notify the AT9010 of EPROM activity. This decode is accomplished by the comparator shown in *Figure 2*.

The DP83916EB-AT design supports an 8k or 16k EPROM (socket); hence, the memory base address options are 8k or 16k sections of memory. Table II shows the decode for a 16k EPROM. Note, SA13 is driven directly into the EPROM; therefore, bit 2 of Configuration Register 2 is a don't care bit.

If the EPROM is used, Configuration Register 2, bits 7 and 6 must be set to 1 and 0 to enable an 8k EPROM or 0 and 1 to select a 16k EPROM. If the EPROM is not used, these bits must be set to 1s to disable the EPROM.

TABLE II. EPROM Memory Base Address

CR2 Bits<5. .2>				Base Address 16k EPROM
bit5	bit4	bit3	bit2	(Hex)
0	0	0	X	0C0000
0	0	1	X	0C4000
0	1	0	X	0C8000
0	1	1	X	0CC000
1	0	0	X	0D0000
1	0	1	X	0D4000
1	1	0	X	0D8000
1	1	1	X	0DC000

INTERRUPT LINE SELECTION

As the SONIC-16 transmits and receives packets from the network, it generates interrupts (via an IRQx line from the AT9010) to the CPU. This results in several slave cycles which read the SONIC-16's Interrupt Status Register and service the interrupt. When the original AT9010 chip asserts an interrupt, it sets a non-latched interrupt indicator in bit 2 of Configuration Register 15 that is cleared when IRQx is cleared. (In the AT9010B, the interrupt indicator is latched; hence, it is maintained even if IRQx deasserts and is cleared by writing a 1 to CR15, bit 2.)

The DP83916EB-AT user can select one of four interrupt lines by programming the AT9010's Configuration Register 0. Table III presents the IRQx choices (lines 3, 4, 5 or 9) and indicates the necessary bits to select the appropriate line. In addition to choosing an IRQx line, the user must also program Configuration Register 0, bit 3 to mask (0) or unmask (1) the chosen interrupt upon assertion of INT from the SONIC-16.

TABLE III. Interrupt Line Selection

CR 0, Bits<2,1>	PLX Reference	IRQx Signal
00	0	3
01	1	4
10	2	5
11	3	9

Comparator Decode							Configuration Register 2			
LA23	LA22	LA21	LA20	LA19	LA18	LA17	SA16	SA15	SA14	SA13
0	0	0	0	1	1	0	bit5	bit4	bit3	bit2

FIGURE 4. EPROM Address Bit Specification

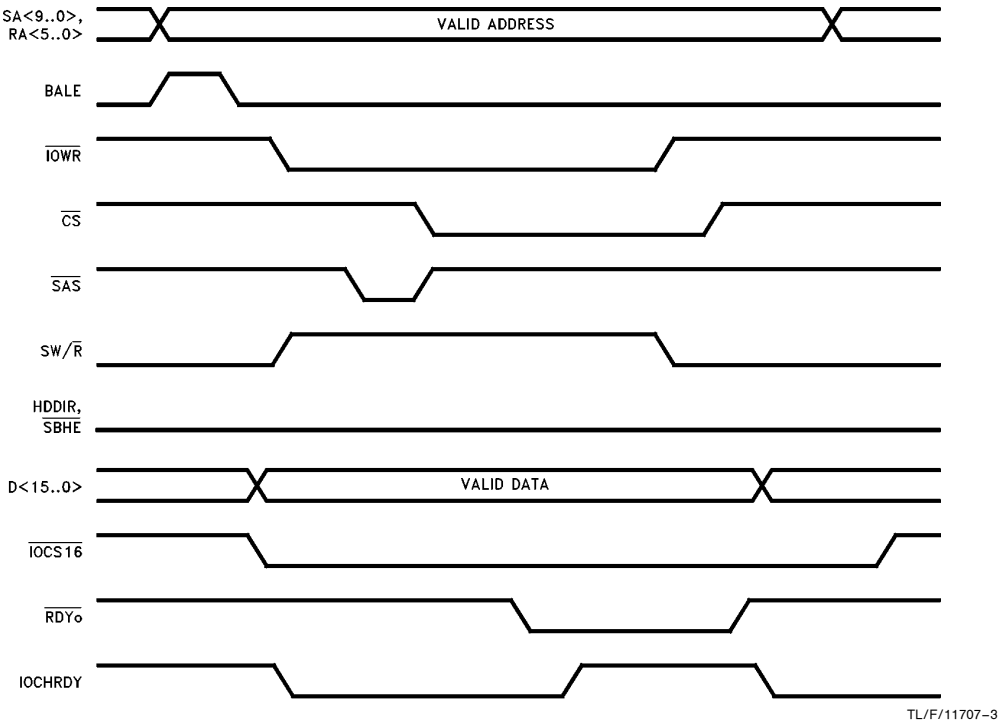

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FIGURE 5. I/O Write Cycle to SONIC-16 Registers

SLAVE CYCLES

The following section presents a basic description and timing diagrams for the signals generated by the AT bus, AT9010 and SONIC-16 when the DP83916EB-AT is in slave mode. A detailed description of the relevant signals associated with AT I/O cycles to the adapter card and AT memory accesses to the EPROM is located in Appendix IV at the end of this application note.

The DP83916EB-AT adapter card is designed so that on power-up, the POSCS3 pin will enable the I/O address of the adapter card onto the data bus. This address is latched into bits<7. .5> of Configuration Register 1 and locates the card in I/O space. Software drivers must subsequently program all registers with the correct data for operation.

The AT bus initiates an I/O cycle by driving the address onto the bus, asserting BALE high and generating -IORD or -IOWR. The AT9010 then generates a chip select to the appropriate slave device.

The SONIC-16 registers, which are located in I/O space, can be written or read. Because they are 16 bits wide, a special signal IOCSI6 is driven to the AT bus for the duration of the SONIC-16 I/O access. The AT9010 drives IOCHRDY low (not ready) after the address and IORD/IOWR signals are asserted (and MEMR/MEMW are not active). (Note, in this document, IOCHRDY will not be broken down into IOCHRDYBUS and IOCHRDYAT in order to give a clear explanation of the signal IOCHRDY's purpose. For an explanation of these signals, refer to the signal descriptions and GAL equations in the appendices and the schematic at the end of this application note.) When the SONIC-16 has latched write data or driven valid read data, it generates RDYo to terminate the cycle. At this time, the AT9010 asserts IOCHRDY high to the AT bus. An example of the signal timing for an I/O write cycle to SONIC-16 registers is shown in *Figure 5*.

Most I/O devices (like the DP83916EB-AT during slave mode) drive IOCHRDY low after the address and I/O command signal are asserted. However, some AT compatible machines use chip sets (from Chips and Technologies or VLSI Technologies) with modified timing characteristics whereby during 16-bit I/O cycles, the PC's bus controller samples IOCHRDY before IORD or IOWR is driven. This problem is detailed in the NSC document "PC-AT Design Considerations for the DP83902EB-AT".

To accommodate this early sampling problem, the AT9010B can be programmed to drive IOCHRDY low immediately upon SONIC-16 register address decode. The AT9010B then uses a gating signal to maintain IOCHRDY if the cycle is an I/O cycle or to stop asserting IOCHRDY if the cycle is a memory cycle. Specifically, if the AT9010B Configuration Register 3, bit 3 is set to 1, IOCHRDY will be driven low early, based on I/O address decode of a SONIC-16 register, then qualified with a gating signal. If CR3, bit 3 is set to 0, IOCHRDY will follow the AT standard: address decode of a SONIC-16 register and IORD/IOWR and inactive MEM-R/MEMW. The early IOCHRDY feature should not be used if the PC I/O cycles are functioning properly. Furthermore, it is not supported by the original AT9010 chip.

The AT9010's registers can be written or read. The 32-byte PROM, however, can only be read. For either device, the I/O read cycles are finished once the data has been enabled onto the bus and read by the CPU. An I/O write cycle to an AT9010 register is completed once the data has been latched to the AT9010. IOCHRDY is not driven low during the 8-bit cycles to either of these devices.

The AT bus initiates a boot EPROM cycle by driving the address onto the bus, asserting BALE high and generating $\overline{\text{MEMR}}$. Once the AT9010 has chip selected the EPROM, data is enabled onto the data bus and the memory cycle is complete. An EPROM read cycle is illustrated in *Figure 6*. IOCHRDY is not driven during EPROM cycles.

DP83916EB-AT REGISTER INITIALIZATION

Upon power-up, the DP83916EB-AT card pulses the card's I/O address into Configuration Register 1. Subsequently, software initializes Configuration Registers 0–3 and 15 for operation.

The original AT9010 is enabled by setting bit 0 of Configuration Register 0 to a 1. If this bit is a 0, the original AT9010 will not respond to any host bus access except hard reset. In the AT9010B, the card is enabled regardless of the state of this bit.

The AT9010B supports software reset. If Configuration Register 15, bit 7 is set to a 1, the AT9010B will reset all the chip's functions to the default condition except Configuration Registers 0–3 and bits 3–5 and 7 of Configuration Register 15. The software must subsequently write a 0 to CR 15, bit 7 to clear this bit. Bit 7 of CR 15 is a reserved bit in the original AT9010. If it is set to 1, the card is lost in I/O space and can only be recovered by hard reset.

Note: The AT9010B corrects bugs in the AT9010 and offers additional features. The DP83916EB-AT card and demonstration software support both versions of the interface chip. Appendix III provides details regarding specific programming of all Configuration Registers.

MASTER LOGIC SECTION

During master mode, the AT's CPU allows the SONIC-16 to take over the system bus and access main memory directly. The SONIC-16 uses the DMA controller to assist in the bus arbitration process. In addition, it utilizes the AT9010's bus interface logic for requesting the bus and generating AT compatible read/write signals. A block diagram showing the master logic is presented in *Figure 7*.

DMA CONTROLLER CHANNEL SELECTION

For data transfer, PC-ATs utilize two 8237A DMA controllers with four channels each. Controller 1 contains channels 0–3 which support byte transfers and are typically reserved for diskette, SDLC, etc. It is cascaded with Controller 2 which contains channels 4–7 to support word transfers. While channel 4 is used to cascade Controller 2, channels 5–7 are usually spare.

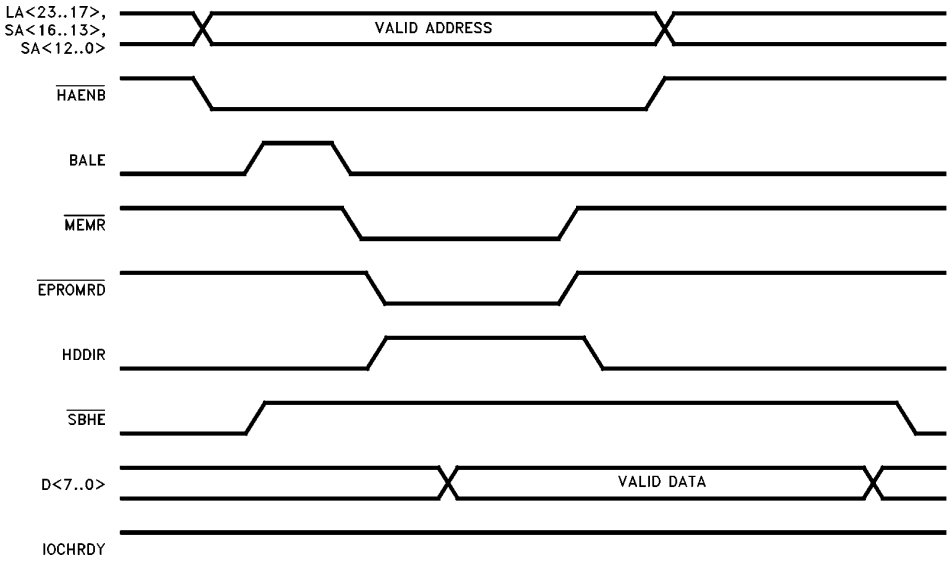

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FIGURE 6. Memory Read Cycle to Boot EPROM

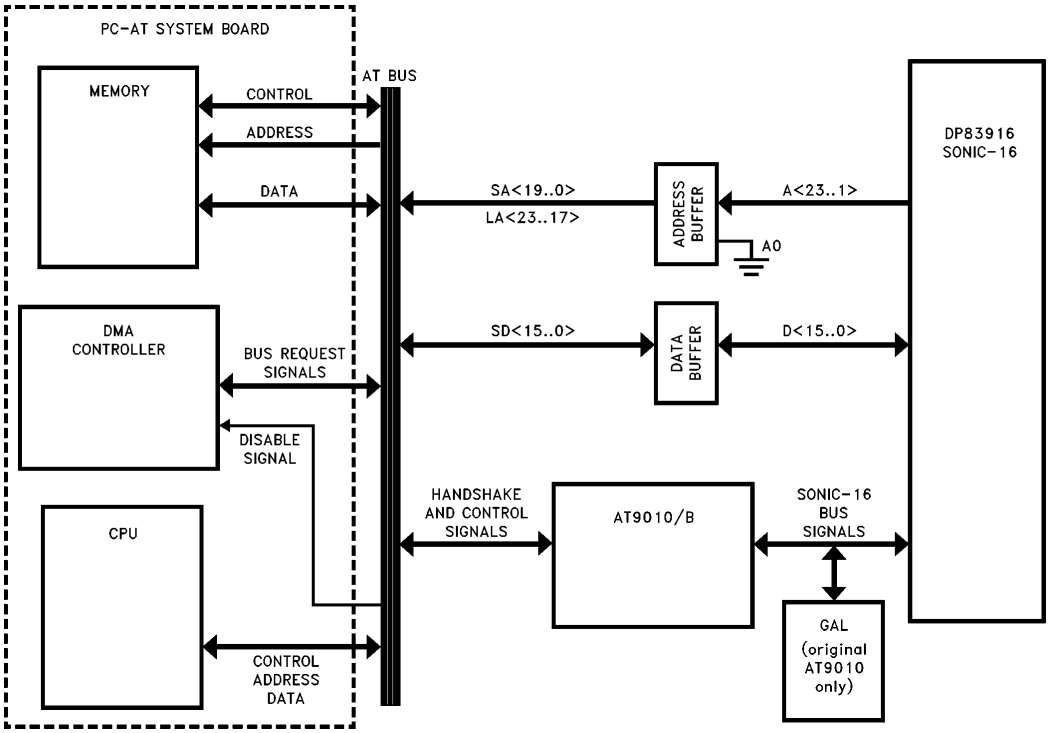

FIGURE 7. Master Logic Block Diagram

The user must select one of the spare DMA channels. By programming the AT9010's bits 0 and 1 of Configuration Register 3, the user can select DMA request line 3, 5, 6, or 7 as shown in Table IV. This will route the DMA request (DRQx) and acknowledge (-DACKx) signals to and from the appropriate DMA controller channel.

TABLE IV. DMA Channel Selection

CR 3, Bits<1,0>	PLX Reference	DMA Channel
00	0	3
01	1	5
10	2	6
11	3	7

An example PC and adapter card configuration is shown in *Figure 8*. Controller 1 is cascaded with Controller 2. Hence, channel 4 of Controller 2 must be programmed for cascade mode so that whenever Controller 1 requests the bus, Controller 2 will arbitrate for it without executing DMA memory or I/O cycles. The software driver must also program the DMA channel used by the SONIC-16 for cascade mode. This is done by writing the commands shown in Table V to the registers of the appropriate DMA Controller. These commands define the sense of the DROx/$\overline{\text{DACK}}$x lines, set the arbitration priority algorithm (fixed or rotating), enable and cascade a particular channel and unmask the channel.

TABLE V. DMA Controller Programming

DMA Register	I/O Addr	Data	Channel
COMMAND			
	08H	10H	3
$\overline{\text{DRQ}}$x Active High	D0H	10H	5
$\overline{\text{DACK}}$x Active Low	D0H	10H	6
Rotating Priority	D0H	10H	7
Enable Channel			
MODE	0BH	D3H	3
	D6H	D1H	5
Cascade Channel	D6H	D2H	6
	D6H	D3H	7
Write Single	0AH	03H	3
Mask Bit	D4H	01H	5
	D4H	02H	6
Unmask Channel	D4H	03H	7

MASTER CYCLES

The following section presents a basic description of the AT bus, AT9010 and SONIC-16 signals generated when the DP83916EB-AT becomes a bus master. It illustrates a timing diagram and presents a basic description of relevant

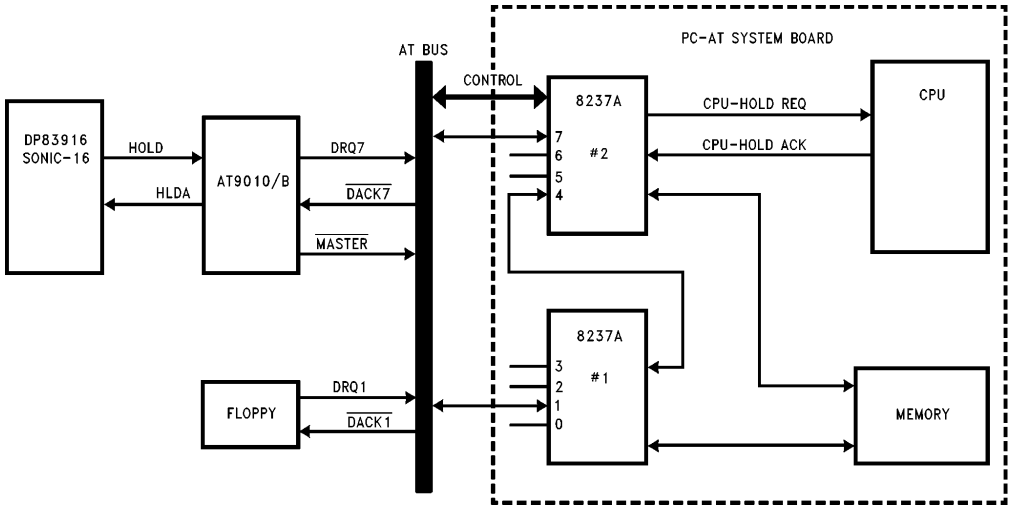

FIGURE 8. Example DMA Controller Configuration

signals associated with the SONIC-16's read and write cycles to system memory. A more detailed description of the signals associated with master cycles is located in Appendix IV at the end of this application note.

As the DP83916EB-AT transmits and receives packets, it accesses system memory to read and write packet data or descriptor information. The SONIC-16 requires the bus for these operations; hence, it drives HOLD to the AT9010 which translates this request for the bus into an active DRQx line. Once the AT bus is available, the DMA controller responds to the AT9010 via the chosen $\overline{\text{DACKx}}$ line. Subsequently, the AT9010 asserts $\overline{\text{MASTER}}$ to the AT bus and relays the $\overline{\text{DACKx}}$ to the SONIC-16 by asserting HLDA. This handshake is shown in *Figure 8*.

Once the SONIC-16 has gained ownership of the AT bus, it generates multiple read or write cycles to the AT's system memory. To begin the cycle, the SONIC-16 drives MW-R to the AT9010. Then, the AT9010 drives $\overline{\text{HAOE}}$ to enable the address buffers, $\overline{\text{HDOE0}}$/$\overline{\text{HDOE1}}$ to enable the data buffers and HDDIR high (memory write) or low (memory read) to establish direction for the flow of data through the data buffers.

At the beginning of each transfer in the cycle, the SONIC-16 drives an address into the address buffers, asserts address strobe, $\overline{\text{ADS}}$, to the AT9010 and latches the address onto the bus. The rest of the transfer depends on whether the SONIC-16 is writing data or reading data from system memory.

If the SONIC-16 is writing data, the AT9010 will strobe $\overline{\text{MEMW}}$ low to the bus for each transfer. The SONIC-16 will source data which is valid after the falling edge of the first BSCK of each cycle. Once the system asserts IOCHRDY high, the AT9010 will drive $\overline{\text{RDYi}}$ to the SONIC-16 to complete the write cycle. A timing diagram for a master write cycle is shown in *Figure 9*.

If the SONIC-16 is reading data, the AT9010 will pulse $\overline{\text{MEMR}}$ to the bus for each read transfer. The system memory will source the data which is latched to the SONIC-16 on the rising edge of the first BSCK after $\overline{\text{RDYi}}$ is asserted. Again, when the CPU asserts IOCHRDY high, the AT9010 will drive $\overline{\text{RDYi}}$ to the SONIC-16 to complete the read cycle.

DP83916EB-AT BUS CYCLE CONFIGURATION

There are two timers which govern the SONIC-16's activity on the bus during master mode. The first is a bus hold timer which is activated to ensure the SONIC-16 cannot hog the bus. It begins when the AT9010 receives $\overline{\text{DACKx}}$ from the bus and expires after 6 (or 12) μs depending on whether AT9010 Configuration Register 0, bit 5 is 0 (or 1).

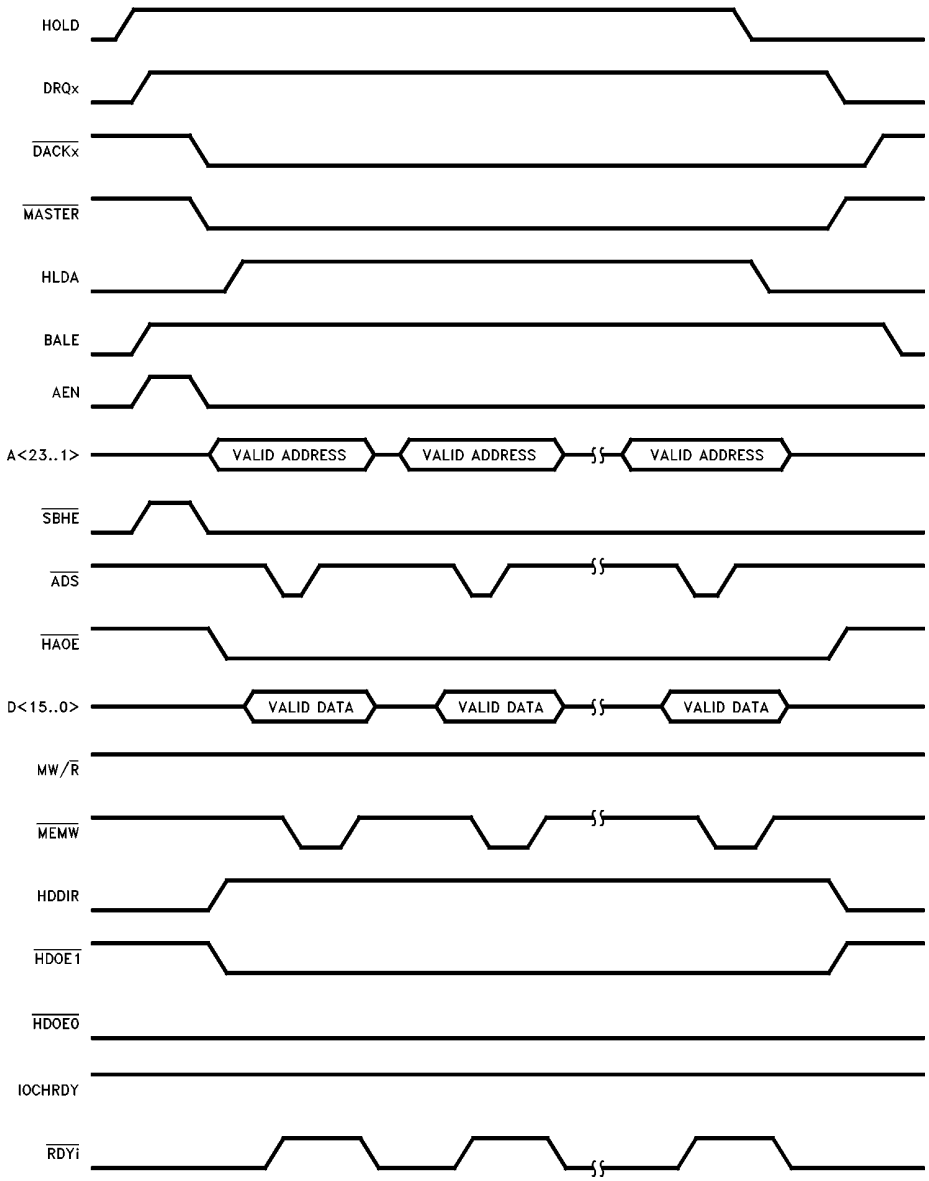

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FIGURE 9. Master Write Cycle

At this point, the AT9010 pre-empts the SONIC off the bus by deasserting HLDA. The original AT9010 chip does not follow proper timing requirements for pre-empting the SONIC-16 and this has been corrected in both the GAL (U11) and the AT9010B. Now, in certain PCs with slow memory cycles, pre-emption causes FIFO underruns or overruns during loopback diagnostics due to the SONIC-16's heavy use of the bus during this mode. Because of these compatibility issues, pre-emption can be disabled. To enable (or disable) the AT9010, set Configuration Register 1, bit 1 to 1 (or 0). This drives a signal PRE-EMPT high (or low) to the GAL (U11). To enable (or disable) pre-emption in the AT9010B, program CR 1, bit 4 to 0 (or 1).

The second timer is an 800 ns timer. Its purpose is to shorten the SONIC-16's bus acquisition time when the SONIC-16 has control of the bus then deasserts HOLD and re-asserts HOLD before 800 ns has expired. In the original AT9010, if these conditions are satisfied **and** the 6 (or 12) μs timer has not expired, the original AT9010 will maintain DRQx to the bus. However, if the conditions are satisfied and the 6 (or 12) μs timer has expired, the SONIC will lose the bus once it

deasserts HOLD. This is true regardless of the state of the signal PRE-EMPT. In the AT9010B, the 800 ns timer is independent of the 6 (or 12) μs timer if the 6 (or 12) μs timer is disabled. The AT9010B's 800 ns timer can be enabled (or disabled) by setting CR0, bit 4 to 1 (or 0). For both versions of the AT9010, if the 6/12 μs timer is active and has not expired **and** the 800 ns timer is active, then if the SONIC-16 deasserts HOLD then re-asserts HOLD before 800 ns has expired, HLDA follows HOLD but DRQx is maintained high to the bus.

The AT9010 offers an option of different master transfer cycle speeds. These speeds define the widths of the $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ pulses for each cycle. They are selected in Configuration Register 3 and are outlined in Table VI.

TABLE VI. Master Transfer Cycle Speeds

CR,3 Bits <5,4>	Megabytes/sec
00	5
01	6.7
10	8
11	10

HUB MANAGEMENT

The DP83916EB-AT incorporates an interface to the Inter-RIC/Management (IR/M) bus of the DP83950EB-AT. This interface implements a managed hub by connecting the DP83916EB-AT to one or several DP83950EB-ATs. In this configuration, the SONIC-16 gathers and buffers network statistics for packets sent from the RICs on the DP83950EB-ATs. The SONIC-16 also transmits over the IR/M bus, allowing management statistics to be accessed by any node on the network. A block diagram of the adapter card portion of the managed hub is shown in *Figure 10*. A comprehensive list of the hub management signals is presented in Appendix IV at the end of this note.

IR/M RECEIVED PACKET FORMAT

Packets are sent by RICs on DP83950EB-ATs to the SONIC-16 over the Management portion of the IR/M bus. The format of these packets differs from the format of standard Ethernet packets. First, the preamble and start of frame delimiter of the packets is a 5-bit sequence 01011 rather than the standard eight bytes of 10101....1011.

Second, the packets have Non Return to Zero (NRZ) format because they are sent over the IR/M bus, rather than through the physical layer.

Third, seven bytes of status information are appended by the RICs after the cyclical redundancy check (CRC) sequence of the packet. This information contains statistics regarding the packet's transmission over the network. Because the status field is appended to the end of the packet, the SONIC-16 interprets the last four bytes of status as CRC and flags a CRC error even though there is no legitimate CRC error. For this reason, the SONIC-16's Receive Control Register (RCR) must be programmed to accept packets with errors.

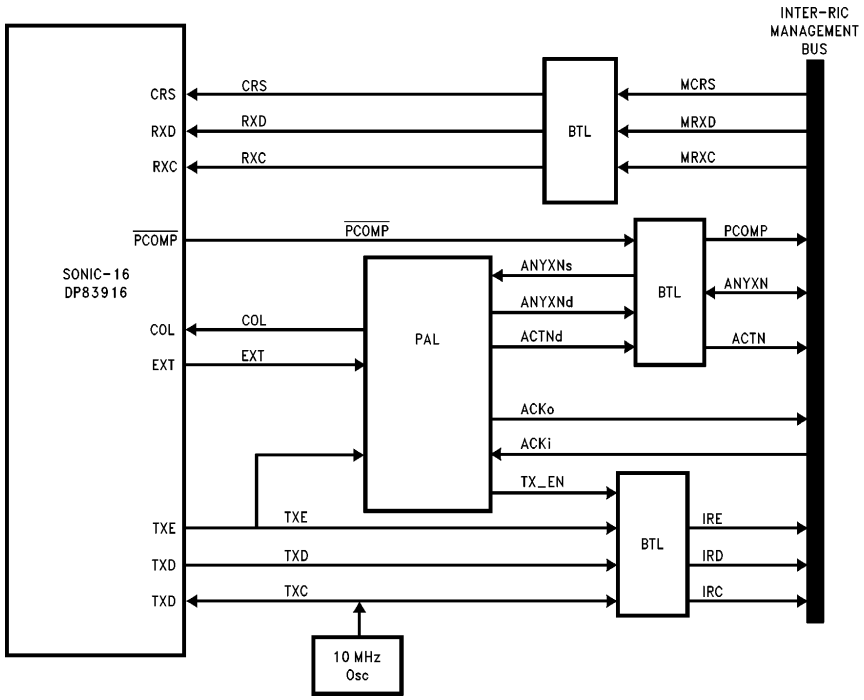

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FIGURE 10. Hub Management Interface

Finally, the packet's destination may specify the SONIC-16 node if the packet contains management commands intended for the SONIC-16 or another node if the packet is sent to the SONIC-16 for the purpose of saving the status information. Hence, the SONIC-16's RCR must be configured to accept all packets including runt packets and all address type packets (in addition to accepting errored packets as described above).

A packet that is sent over the management bus has the format shown in *Figure 11.* A detailed description of the information contained in the seven bytes of management statistics is located in the DP83950 Repeater Interface Controller (RIC) Data Sheet.

PACKET RECEPTION SIGNALS

The signals MCRS, MRXD and MRXC sent over the management bus, are the management carrier sense, management data, and management clock which specify the packets sent to the SONIC-16. They are buffered through inverting turbo transceivers (BTLs). The BTLs drive the IR/M bus signals with the same characteristics as the signals on the DP83950EB-AT card. BTL features include high density backplane capabilities, minimum delay and fast voltage switching characteristics; however, BTLs are not required for all applications.

As described above, the packets are in NRZ format; hence, the buffered signals, CRS, RXD and RXC driven to the SONIC-16 are NRZ signals. These signals are connected directly to the CRS, RXD and RXC of the SONIC-16. The SONIC-16 is programmed (USER__PIN3 of AT9010 Configuration Register 1 is set to 1) for external ENDEC mode.

With the above configuration, the SONIC-16 will buffer every packet received from the IR/M bus. It can, however, be programmed to save memory space by ''compressing'' packets whose data is not intended for reception by the SONIC-16. With this feature, the SONIC-16 can buffer status information, a portion of data and status or the entire packet. This is accomplished via a SONIC-16 control signal called $\overline{\text{PCOMP}}$. If $\overline{\text{PCOMP}}$ is asserted to the management bus, the receive clock signal, MRXC, will be inhibited during transmission of packet data and enabled during transmission of the packet's seven bytes of status information. This causes the packet to be ''compressed''; i.e., only destination address and status data are buffered to memory.

In order to use packet compression, the SONIC-16's DCR2 register must be programmed to assert $\overline{\text{PCOMP}}$ upon CAM (Content Addressable Memory) register match or mismatch. For a managed hub, the DCR2 must be programmed to assert $\overline{\text{PCOMP}}$ upon CAM mismatch. Then, if the SONIC-16's CAM is programmed with its own Ethernet address, all packets with destination addresses equal to the SONIC-16's address will be buffered. All other packets will be compressed. For a managed bridge, the DCR2 register must be programmed to assert $\overline{\text{PCOMP}}$ upon CAM register match. In this case, the SONIC-16's CAM is programmed with the addresses of all RICs on the LAN from which the packet is being transmitted. Then, only packets intended for the SONIC-16 or for nodes on the other side of the bridge link will be buffered. All packets which are merely repeated to the RIC connected to the SONIC-16 then forwarded to the SONIC-16 over the Management bus, will be compressed to save status information only.

In addition to programming the SONIC-16's DCR2 the Packet Compress Decode (PCD) Register of the RIC must be initialized with the number of bytes after SFD, not including seven bytes of status information, to be transferred if the SONIC-16 asserts $\overline{\text{PCOMP}}$. According to the DP83950 RIC Data Sheet, the value of this register must be less than or equal to 255 bytes. The actual value, however, must be between 7–255 bytes because the SONIC-16 requires six bytes of destination address and five bits of address compare time in order to determine whether or not to assert $\overline{\text{PCOMP}}$. If the user enters a PCD value less than seven bytes, the driver software should change the value to seven so that $\overline{\text{PCOMP}}$ will operate properly. In this scenario, six bytes of destination address and one byte of source address will be buffered along with the seven bytes of status information.

An example of $\overline{\text{PCOMP}}$ and the effect on MRXC is shown in *Figure 11*. For this example, the RIC's PCD is 0EH. As it transmits the packet, the RIC counts 14 bytes from the beginning of the destination address. Because the SONIC-16 asserts $\overline{\text{PCOMP}}$, the RIC inhibits the MRXC 14 bytes after the beginning of the packet. It enables the MRXC for the last seven bytes of status data.

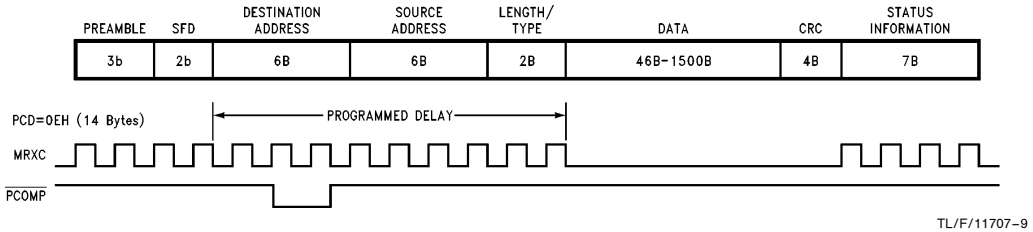

FIGURE 11. Packet Reception Over Management Bus

IR/M PACKET RECEPTION

When the SONIC-16 begins receiving a packet, it compares the destination address of the packet with all addresses in its content addressable memory (CAM) register. If the SONIC-16 is configured as a managed hub and there is a CAM match, the entire packet, along with the seven bytes of status information, is buffered to memory where it waits to be processed by upper-level management software. If there is no CAM match, the SONIC-16 asserts $\overline{\text{PCOMP}}$ to the Management bus. Depending on the value of the PCD, the RIC sending the packet will inhibit the receive clock signal, MRXC during a portion of the packet data and enable it during the seven bytes of status. Hence, only destination address, a portion of source address/data and status information is buffered to memory where it waits to be processed by upper-level management software.

IR/M TRANSMITTED PACKET FORMAT

Packets are sent by the SONIC-16 to the RICs on DP83950EB-ATs over the Inter-RIC portion of the IR/M bus. These packets have the format of standard Ethernet packets.

PACKET TRANSMISSION SIGNALS

The SONIC-16 transmits over the Inter-RIC bus using the transmit enable (TXE), transmit data (TXD) and transmit clock (TXC) to specify the packets. TXC is driven by a 10 MHz signal from a flip-flop which divides an external 20 MHz oscillator clock by two. The transmit signals are connected to the SONIC-16's transmit pins, TXE, TXD and TXC and have NRZ format. They are driven through an inverting turbo transceiver (BTL) and become the Inter-RIC enable (IRE), Inter-RIC data (IRD) and Inter-RIC clock (IRC), which connect directly to the Inter-RIC bus.

Because of the SONIC-16's interface to the Inter-RIC/Management bus, it appears to be another RIC to the rest of the RIC network. Hence, the SONIC-16 participates in the RICs' serial arbitration scheme for transmission and uses the same handshake signals. This arbitration scheme is contained in a PAL and is described in the following paragraphs. The actual PAL equations are located at the end of this application note.

The RICs and SONIC-16 are connected in the serial arbitration scheme by two signals, ACKi and ACKo. ACKo of a RIC above the SONIC-16 connects to ACKi of the SONIC-16; ACKo of the SONIC-16 connects to ACKi of a RIC below it. The SONIC-16 and RICs pass permission to transmit down the chain by driving ACKo high to the ACKi of the next chip in the chain.

Regardless of whether or not the SONIC-16 has permission to transmit, it does so whenever the management bus is quiet and there is data to send. Hence, when the SONIC-16 wants to transmit, it drives TXE high. If the SONIC-16 has permission to transmit (i.e., ACKi is high), the PAL activates ACTNd high to notify the RICs of the SONIC-16's transmit activity on the Inter-RIC bus. If the SONIC-16 does not have permission to transmit (i.e., ACKi is low), the PAL activates ANYXNd high which notifies the RICs of a SONIC-16 transmit collision.

The SONIC-16's collision pin (COL) is driven by the PAL when the SONIC-16 is transmitting and either a transmit collision occurs on the network/Inter-RIC bus or a receive collision occurs on a RIC's AUI port. If the SONIC-16 is transmitting and a collision occurs, the SONIC-16 sends jam pattern, then backs off the Inter-RIC bus. At the same time, the RICs send jam pattern and then become idle. After some time, the SONIC-16 attempts to retransmit. If the SONIC-16 is not transmitting and a collision occurs on the network, the RICs send jam to their ports. A Management Interface Configuration (MIFCON) bit in the RIC's Interrupt and Management Configuration Register determines the outcome of this collision event. If MIFCON is 0 and the collision occurs before the packet's start of frame delimiter, the RIC whose packet has collided, will send 01011 followed by seven bytes of status (which reflect the collision) to the SONIC-16. If MIFCON is 1 and the collision occurs before the SFD, neither packet nor status data is transmitted over the Management bus to the SONIC-16. Finally, if MIFCON is 0 (or 1) and the collision occurs after the packet's SFD, the RIC appends the status information and sends the packet to the SONIC-16.

The PAL drives a BTL transmit enable (TX__EN) signal to the transmit BTL which enables the BTL only when the SONIC-16 is configured for an external ENDEC, has permission to transmit and wants to transmit. This prevents the BTL from driving IRE, IRD and IRC unless the SONIC-16's transmission is valid.

DP83916EB-AT CONFIGURATION FOR HUB MANAGEMENT

The adapter card must be configured differently to use the hub-management option. First, the card cannot be connected to Inter-RIC/Management bus and a physical layer interface at the same time. Jumper 4 must be disconnected. Second, the AT9010's USER__PIN3 (bit 3) in Configuration Register 1 must be set to a 1 to configure the SONIC-16 for external ENDEC mode. Third, the AT9010's USERPIN2 (bit 2) in Configuration Register 1 must be set to a 0 to enable the receiving BTL.

MEDIA INTERFACE

The network interface of the DP83916EB-AT card offers three media interface options (in addition to the Inter-RIC/Management interface): Thin Ethernet, Thick Ethernet and Twisted-Pair. **Only one of the three interfaces may be used at a given time and cabling requirements are specified in the following section.** A physical layer block diagram is given in *Figure 12*.

The Coaxial Interface features the DP8392C Coaxial Transceiver Interface (CTI) as a coaxial cable line driver/receiver connected between the SONIC-16 and the BNC connector for Thin Ethernet coaxial cable. For transmission, it converts AUI signals to single-ended 10BASE2 signals. On reception, it converts single-ended 10BASE2 signals to AUI signals. The isolation between the CTI and the SONIC-16, required by the IEEE 802.3, is satisfied on the signal lines by a transformer. Power isolation for the CTI is performed by a DC to DC converter which supplies the CTI with a −9V power supply for operation. To use the adapter card in a Thin Ethernet environment, it is necessary to short JP4 which supplies the CTI with −9V.

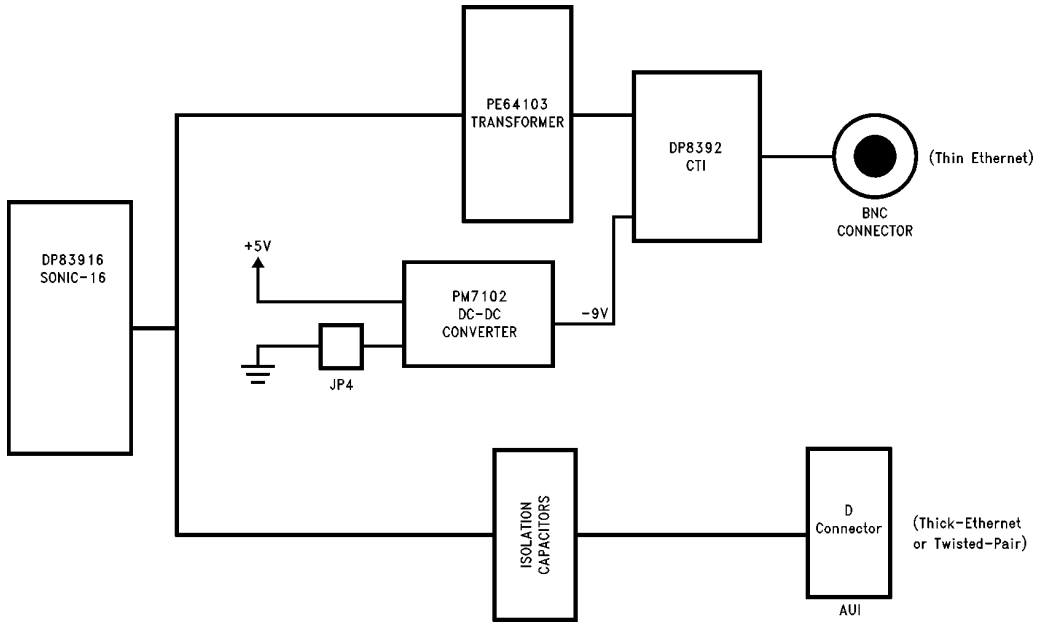

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FIGURE 12. Media Interface Block Diagram

The AUI Interface option allows the use of the DP83916EB-AT with one of several alternative cable media. Possible choices include Thick Ethernet cable for 10BASE2 networks and Twisted-Pair cable for 10BASE-T networks. No on-board transformers are required for isolation because the connector to the AUI is a medium attachment unit (MAU) which houses its own transformer and DC to DC converter. However, capacitors are used for DC isolation and 16V fault tolerance. To use the AUI interface, open JP4 to disable power to the CTI.

The interface options and jumper settings are summarized in Table VII. It is imperative to note that **only one network interface option and cable can be used at a time. Multiple cables will result in network errors.**

TABLE VII. Jumper Selection for Media Interface or Hub Management

JP4	Network Interface/HM
Short*	**Thin Ethernet***
Open	Thick Ethernet, Twisted-Pair via AUI
Open	HUB-Management

* DP83916EB-AT default setting

DP83916EB-AT CONFIGURATION

In order to maximize the utility and options of the DP83916EB-AT adapter card, it is imperative that the board is configured correctly. The following section highlights the **hardware and software configuration issues which must be considered prior to installation of the card for the first time.**

HARDWARE CONFIGURATION

There are two versions of the PLX bus interface chip: the AT9010 and the AT9010B. The DP83916EB-AT design supports both chips with the following component placement considerations. If the original AT9010 is used, a GAL (U11) containing AT9010 fixes must be populated. In addition, resistors R46, R47 and R48 must not be populated. If the AT9010B is used, the GAL (U11) must be left open and resistors R46, R47 and R48 must be populated. The above considerations are determined at the time of board assembly. Hence, they should not be of concern to the card user.

The user must determine the I/O address of the card and set jumpers JP1–JP3. If the optional boot EPROM is to be used, it must be inserted on the adapter card.

To use the DP83916EB-AT's media interface, the user must select one of the interface options including Thin Coax (10BASE2) or AUI (with 10 BASE5 or 10BASE-T) and configure JP4 according to the Media Interface Section. Or, to use hub management, the user must install a DP83950E-B-AT RICKIT, disconnect any DP83916EB-AT media interface connections and open JP4.

The above hardware settings must be considered prior to inserting the board into an AT bus slot.

SOFTWARE CONFIGURATION

The DP83916EB-AT features many user options which can be selected by programming the configuration registers of the AT9010. The following summarizes the software options available; references to AT9010 are given as (Configuration Register Number, Applicable Bits). For a complete listing of AT9010 Configuration Registers and demonstration software defaults, refer to Appendix III.

Card enable (CR0, Bit0): enables (1) or disables (0) the original AT9010. Once disabled, the original AT9010 can only be re-enabled with hard reset. The AT9010B is always enabled regardless of the state of this bit.

Selectable interrupt lines (CR0, Bits<2,1>): one of four must be chosen: 00 = IRQ3, 01 = IRQ4, 10 = IRQ5, 11 = IRQ9.

Interrupt unmask (CR0, Bit 3): unmasks (1) or masks (0) the IRQx signal when INT is driven by the SONIC-16.

800 ns timer (CR0, Bit 4): enables (1) or disables (0) the 800 ns timer in AT9010B. This timer is always enabled in the original AT9010.

Maximum bus hold time after detection of $\overline{\text{DACKx}}$ (CR0, Bit 5): 0 = 6 μs, 1 = 12 μs. In the original AT9010, this timer can be enabled (or disabled) by setting CR1, bit 1 to 1 (or 0). In the AT9010B, it can be enabled (or disabled) by setting bit 4 of CR1 to 0 (or 1).

USER__PIN1/PRE-EMPT (CR1, Bit 1): enables (1) or disables (0) SONIC-16 pre-emption in the original AT9010.

USER__PIN2/-RE__EN (CR1, Bit2): drives a 0 for a BTL receive enable in the hub management interface. This bit must be a 1 when not using hub management.

USER__PIN3/EXT (CRI, Bit3): drives a 0 for an internal SONIC-16 ENDEC when using the physical interface or a 1 for an external ENDEC when using the hub management interface.

I/O address of the card (CR1, Bits <7. .5>): one of seven choices must be made; these are outlined in the Slave Logic Section. Note, the address programmed in the AT9010's CR1 must match the address selected by JP1–JP3.

EPROM memory size or disable (CR2, Bits <7,6>): selects a 16k EPROM, 8k EPROM or EPROM disable: 01 = 16k, 10 = 8k, 11 = disable.

EPROM memory address (CR2, Bits <5..2>): this address must be specified if using the EPROM. Details are given in the Slave Logic Section.

Selectable DMA lines (CR3, Bits <1,0>): one of four must be chosen: 00 = DMA 3, 01 = DMA 5, 10 = DMA 6 11 = DMA7.

$\overline{\text{MEMW}}$ cycle extension (CR3, Bit 2): when set to 0, this option will extend the -MEMW cycle by 50 ns to allow additional address set-up time.

IOCHRDY assert (CR3, Bit 3): selects IOCHRDY normal assert (0) or early assert (1) in AT9010B only. See Slave Logic Section for details.

Master data transfer cycle (CR3, Bits <5,4>): one of four speeds must be chosen: 00 = 5, 01 = 6.7, 10 = 8, 11 = 10 MB/sec.

Channel check enable: (CR3, Bit 6) is not used by the DP83916EB-AT. This bit should be set to 1 to disable the AT9010 check output.

Software reset (CR15, Bit 7): is supported in the AT9010B. When this bit is set to 1, the AT9010B resets all of the chip's functions to their default conditions except CR0–3 and CR15, bits 3–5. This bit is cleared by writing a 0 to CR15, bit 7 to clear the bit. In the original AT9010, setting this bit to 1 causes the card to be lost in I/O space; it can only be recovered by hard reset.

ADDITIONAL INFORMATION

Additional information for the AT9010 Bus Master Interface Chip is available through PLX Technology, Inc., 625 Clyde Avenue, Mountain View, CA 94043, (415) 960-0448, FAX (415) 960-0479.

APPENDIX I: PAL (U16) AND GAL (U11) EQUATIONS

This appendix provides the equations for the PAL (U16) and the GAL (U11). The PAL contains arbitration equations for hub management. The GAL contains fixes for the bugs in the original AT9010 chip.

DP83916EB-AT Inter-RIC/Management Interface PAL (U16)

```
module intf2

title 'SONIC/RIC Management Interface for DP83916EB-AT (r2)'

"history: finalized by Bill Bunch on 9/19/91

"device declaration
      U16_PAL2  device 'p16l8';

"inputs

      anyxn_s    pin  2;
      ack        pin  3;
      ext        pin  4;
      txe        pin  9;
      coln       pin  17;

"outputs

      col        pin  12;
      tx_en      pin  13;
      acko       pin  14;
      actn_d     pin  18;
      anyxn_d    pin  19;

equations

     acko = !txe & acki;

     actn_d = txe & acki;

     anyxn_d = txe & !acki;

     col = txe & (anyxn_s # coln);

     tx_en = txe & acki & ext;

     col.oe = ext;

     actn_d.oe = ext;

     anyxn_d.oe = ext;

end intf2;
```

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DP83916EB-AT Original AT9010 GAL Fixes (U11)

```
module splxr2

flag '-r1','-t4';

title 'GAL fixes for original PLX AT9010 bugs and DP83916EB-AT - p/n U11'

"history: Finalized by Denise Troutman on 6/1/92

"This GAL fixes the following problems in the original AT9010 chip:
"    1.  Asserting IOCHRDYAT inappropriately when certain PCs drive the SONIC-16's I/O address
"        during boot-up
"    2.  Not maintaining HLDA long enough to satisfy the SONIC-16's pre-emption specification
"        in the following case: the SONIC-16 requests the bus (drives HOLD high) within 800 ns of
"        giving up the bus (driving HOLD low) and the 6/12 µs timer has just expired
"    3.  LRESET with inverted polarity
"    4.  Inability to disable SONIC-16 pre-emption off the bus - this causes problems in certain PCs
"        with slow memory whereby the memory transfers are so long that FIFO underruns during
"        transmission or FIFO overruns during reception may occur; the problem is aggravated during
"        loopback because of the SONIC-16's heavy use of the bus for this mode.

"device declaration
      U11_GAL2 device 'P20V8R';

@page

"pin assignments

      "INPUTS
      aen               pin 8;
      !iord             pin 2;
      !iowr             pin 3;
      !hostown          pin 4;
      lclk              pin 5;
      hold              pin 6;
      hlda              pin 7;
      preempt           pin 9;
      lreset            pin 10;

"outputs
      hldadlym          pin 16;
      hldadly           pin 17;
      hldaout           pin 22;
      !iochrdyoe        pin 19;
      !iochrdyat        pin 20;
      !iochrdybus       pin 21;
      hldasonic         pin 18;
      reset             pin 15;

      iochrdyoe         istype 'com,neg';
      iochrdyat         istype 'com,neg';
      iochrdybus        istype 'com,neg';
      hldadlym          istype 'com,neg';
      hldadly           istype 'com,neg';
      hldaout           istype 'com,neg';
      hldasonic         istype 'com,neg';
      reset             istype 'com,neg';
```

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```
"constant declarations
      L    = 0;
      H    = 1;
      OFF  = 0;
      ON   = 1;
      X    = .X.;
      Z    = .Z.;
      CK   = .C.;

@page
equations

"Qualify IOCHRDYAT with IORD and IOWR
     iochrdyoe = !hostown & !aen & iochrdyat & (iord # iowr);

     iochrdybus.OE = iochrdyoe;
     iochrdybus = ON;

     iochrdyat.OE = hostown;
     iochrdyat = iochrdybus;

"Delay HLDA from AT9010 up to one clock
     hldadlym = (!lclk & hlda) # (lclk & hldadlym) # (hlda & hldadlym);

     hldadly = (lclk & hldadlym) # (!lclk & hldadly) # (hldadlym & hldadly);

     hldaout = hlda # (hold & hldadly);

"Enable or disable pre-emption based on state of PREEMPT
     hldasonic = (preempt & hldaout) #
          (!preempt & (hlda # hldadly # (hold & hldasonic)));

"Invert RESET to SONIC-16
     reset = !lreset;

end splxr2;
```

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APPENDIX II: BILL OF MATERIALS (BOM) for DP83916EB-AT

This appendix provides a list of all components placed on the DP83916EB-AT. If the original AT9010 is populated, a GAL (U11) must also be populated and resistors R46, R47 and R48 should be left open. If the AT9010B is populated, the GAL (U11) should be left open and R46, R47 and R48 should be populated.

Capacitors (58)

C3..C6	0.1 μF/50V	10% Monolithic
C7	0.01 μF/25V	20% Monolithic
C8	0.01 μF/1 kV	10% Ceramic Disk
C9	0.75 pF/1 kV	Spark Gap
C10, 11	0.01 μF/50V	10% Monolithic
C12	47 μF/50V	20% Tantalum
C13. .C25, C28. .C39	0.1 μF/50V	20% Monolithic
C26, C27, C40. .C48	4.7 μF/16V	20% Tantalum
C49	4.7 μF/25V	20% Tantalum
C50. .C54	0.1μF/50V	20% Tantalum
C55 .C60	1 μF/50V	10% Monolithic

Resistors (46) (5%, 1/4W unless otherwise specified)

R1. .R4, R9, R12		
R16, R17, R30. .R45	4.7k	
R5. .R8	10k	
R10	1k	
R18, R20. .R23	1k	1%, 1/4W
R14, R15	270	
R19	150	1%, 1/4W
R24	10k	1%, 1/4W
R25	IM	5%, 1/2W
R26. .R29	39.2	1%, 1/4W
R46. .R48	0	(do not populate for original AT9010; populate for AT9010B)

Integrated Circuits (17)

U1, U2	DM74AS245	
U3	DM74S288	
U4	NMC27CP128	(not supplied on board)
U5	DM74ALS244A	
U6. .U8	DM74ALS541	
U9	DM74ALS521	
U10	PLXAT9010/B	
U11	GAL20V8A-15	(populate for original AT9010; do not populate for AT9010B)
U12	DP83916B	
U14	74F74	
U15, U17, U18	DS3893A BTL	
U16	PAL16L8A	
U19	DP8392V	

Connectors (2)

J4	BNC Connector, socket	(AMP #227161-2)
J5	15-Pin D Connector, socket	(AMP 9020A # 747845-4)

Magnetics (2)

T1	PE64103 (Pulse Engineering) or LT6003 (Valor)
U20	PM7102 (Valor) DC-DC Converter

Jumpers (4)

JPl. .JP4	Single Jumpers 1 x 2 Shunt Block with 0.1″ spacing

Test Pins (35)

TP1. .TP35	Single post pins

Sockets (5)

S1	24-pin, Dual in-line socket for GAL (U11)	
S2	20-pin, Dual in-line socket for PAL (U16)	
S3	16-pin, Dual in-line socket for the PROM (U3)	
S4	28-pin, Dual in-line socket for EPROM (U4)	
S5	132-pin AMP Socket for SONIC-16 (U12)	
	Housing Sub-Assembly Cover	(AMP #821949-5)
	Cover	(AMP #821942-1)

Others (6)

U13	20 MHz Oscillator 40%–60% Duty, 0.001% Tolerance	
D1	MMBD1203 Diode	
Bracket	Face plate	
Slide Latch Kit	For 15-pin D-Connector (J5)	(AMP # 745583-5)

Note: U4 (EPROM) is marked ‘‘not supplied on board’’; the component socket is left open.

APPENDIX III: AT9010 and AT9010B CONFIGURATION REGISTERS

This appendix describes the features and programming for the original AT9010 and AT9010B Configuration Registers. It can be assumed that the bits have the same function in both chips unless otherwise noted. The demonstration software ''sonicpla.exe'' defaults are also provided.

CONFIGURATION REGISTER 0: default = 71 H

Bit	7	6	5	4	3	2	1	0
Short Name	RES	RES	BHT	RES/ET	UI	IS	IS	CE/RES
Default	0	1	1	1	0	0	0	1

RES = reserved
BHT = bus hold time (0 = 6 μs/1 = 12 μs)
RES/ET = AT9010: reserved
AT9010B: enable 800 ns timer (1 = enable/0 = disable)
UI = unmask interrupt (1 = unmask/0 = mask)
IS = interrupt select (O0 = IRQ3, 01 = IRQ4, 10 = IRQ5, 11 = IRQ9)
CE/RES = AT9010: card enable
AT9010B: reserved

CONFIGURATION REGISTER 1: default = 94 H

Bit	7	6	5	4	3	2	1	0
Short Name	IOA	IOA	IOA	RES/DT	EXT	$\overline{\text{RE}}$__EN	PE	U0
Default	1	0	0	1	0	1	0	0

IOA = I/O base address (000 = 100 H, 001 = 120 H, 010 = 140 H, 011 = 160 H,
100 = 300 H, 101 = 320 H, 110 = 340 H, 111 = 340 H)
RES/DT = AT9010: reserved
AT9010B: disable 6/12 μs bus hold timer (1 = disable/0 = enable)
EXT = external ENDEC for Inter-RIC/Management (0 = internal/1 = external)
$\overline{\text{RE}}$__EN = enable receive for Inter-RIC/Management (0 = enable 1 = disable)
PE = pre-empt enable (1 = enable/0 = disable SONIC pre-emption; AT9010)
U0 = User bit 0 (not used)

CONFIGURATION REGISTER 2: default = C0 H

Bit	7	6	5	4	3	2	1	0
Short Name	PS	PS	PBA	PBA	PBA	PBA	RES	RES
Default	1	1	0	0	0	0	0	0

PS = PROM select - size or disable (00 = 32k, 01 = 16k, 10 = 8k, 11 = disable)
PBA = PROM base address (for 16k EPROM: 000X = C0000 H, 001X = C4000 H,
010X = C8000H, 011X = CC000 H, 100X = D0000 H, 101X = D4000H,
110X = D8000 H, 111X = DC000 H)
RES = reserved

CONFIGURATION REGISTER 3: default = C2 H

Bit	7	6	5	4	3	2	1	0
Short Name	CCA	MCC	MDT	MDT	RES/IS	ETO	DMA	DMA
Default	1	1	0	0	0	0	1	0

CCA = channel check (output) assert (not used)
MCC = mask channel check (not used)
MDT = master data transfer cycle speed (00 = 5, 01 = 6.7, 10 = 8, 11 = 10 MB/sec)
RES/ISA = AT9010: reserved
AT9010B: IOCHRDY signal assert (0 = normal/1 = early IOCHRDY signal)
ETO = extra time off (0 = extended/1 = normal -MEMW cycle)
DMA = DMA channel select (00 = DMA3, 01 = DMA 5, 10 = DMA 6 11 = DMA 7)

CONFIGURATION REGISTER 15: default = 00 H

Bit	7	6	5	4	3	2	1	0
Short Name	RES/SR	CSI	P5	P4	P3	II	RES	RES
Default	0	0	0	0	0	0	0	0

RES/SR = AT9010: reserved
AT9010B: software reset (1 = soft reset/0 = non-soft reset mode)
CSI = channel check (input) indicator (not used)
P5, P4, P3 = SONIC register page select - bit 5, bit 4, bit 3
II = interrupt indicator
RES = reserved

APPENDIX IV: DP83916EB-AT SIGNALS

This appendix presents a detailed description of the adapter card control signals specific to timing, slave cycles and initialization, master cycles and hub management. They are presented in the form SIGNAL (ORIGIN, DESTINATION) or SIGNAL (ORIGIN to DESTINATION/ORIGIN to DESTINATION).

CLOCK SIGNALS

The clock signals are provided for the synchronous operations of the AT9010, the SONIC-16 and the optional IR/M interface. They are described in detail below:

20 MHz (20 MHz Osc, AT9010 and SONIC-16 and Flip-flop) is an oscillator signal which drives all synchronous operations in the AT9010 and provides a clock for the SONIC-16's ENDEC. It also provides a 20 MHz signal to the flip-flop divide by two circuit which drives 10 MHz to the transmit BTL.

BSCK (AT9010, AT bus and GAL) provides timing for the SONIC-16 DMA logic.

TXC (Flip-flop, SONIC-16 and Tx BTL) provides the timing for the transmission of packets when using the hub-management interface.

SLAVE CYCLE SIGNALS

The following control signals provide interrupt, reset and status functions:

INT (SONIC-16, AT9010) is active when the SONIC-16 is asserts an interrupt request.

IRQx (AT9010, AT bus) is asserted by the AT9010 when the SONIC-16 asserts its interrupt request line, INT. One of four lines IRQ9, IRQ5, IRQ4 or IRQ3 is selected as the interrupt by programming bits <2,1> of the AT9010's Configuration Register 0.

RES__DRV (AT bus, AT9010) provides a hard reset to the AT9010. This signal initializes logic internal to the AT9010.

LRESET/-RESET (AT9010 to GAL to SONIC-16) provides a hardware reset to the SONIC-16. It is asserted and deasserted synchronous to BSCK. For the AT9010B, this signal is inverted inside the chip and is driven directly to the SONIC-16.

S<2..0> (SONIC-16, AT9010) are SONIC-16 status lines which indicate the current SONIC-16 bus operation.

USER__PIN3/EXT (AT9010, SONIC-16 and PAL) drives the EXT pin input of the SONIC-16 low to enable the SONIC-16's internal ENDEC (when using a media interface) and high to disable the ENDEC (for managed-hub applications). The level of this signal is set in the AT9010's Configuration Register 1.

USER__PIN2/-RE__EN (AT9010, BTL) drives the receive enable signal $\overline{\text{RE}}$__EN, to one of the turbo-transceivers (BTL) when using the SONIC-16/RIC hub-management interface.

$\overline{\text{POSCS3}}$ (AT9010, A-buffer) enables an address buffer to load the address of the adapter card into AT9010 Configuration Register 1, bits <7..5> after hard reset. All other $\overline{\text{POSCS}}$ pins are not connected because the registers are loaded by software rather than by hardware.

The following signals are utilized during slave mode for both I/O cycles and EPROM cycles:

BALE (AT bus, AT9010) is driven high for all slave cycles on the DP83916EB-AT.

HDDIR (AT9010, D-Buffers) is an input to the data buffers which identifies the direction of a data transfer. It drives high for data transfers to the AT bus during an I/O or EPROM read cycle. It drives low for data transfers to the adapter card during an I/O write cycle.

IOCHRDYAT/IOCHRDYBUS (AT9010 to GAL to AT bus) are input and output signals for both the AT bus and the AT9010. For the original AT9010, the GAL translates the AT9010's IOCHRDYAT into IOCHRDYBUS and drives this signal to the AT bus to complete a 16-bit I/O cycle to the SONIC-16's registers. For the AT9010B, IOCHRDY is driven from the AT9010B directly to the AT bus. An early IOCHRDY signal can be driven by the AT9010B. This is detailed in the Slave Logic Section.

During I/O cycles, the following signals are generated:

AEN (AT bus, AT9010 and GAL) is a signal asserted high to all ports during DMA cycles to prevent I/O resources that do not have an active $\overline{\text{DACKx}}$ from responding to DMA controller I/O cycles. The AT9010 uses the low level of AEN to qualify CPU accesses to the registers in I/O space.

$\overline{\text{IORD}}$ (AT bus, AT9010 and GAL) indicates that the system is reading data from an I/O register.

$\overline{\text{IOWR}}$ (AT bus, AT9010 and GAL) indicates that the system is writing data to an I/O register.

$\overline{\text{CS}}$ (AT9010, SONIC-16) is the chip select to the SONIC-16.

$\overline{\text{IOCS16}}$ (AT9010, AT bus) is driven to the AT bus when SONIC-16 registers are to be accessed; it indicates a 16-bit slave device.

PROMID (AT9010, PROM) is the chip enable for the PROM.

$\overline{\text{SAS}}$ (AT9010, SONIC-16) is asserted by the AT9010 to the SONIC-16. During a register write cycle, this signal indicates a valid address on the bus. During a register read cycle, it indicates the SONIC-16 can begin sourcing data.

SW-R (AT9010, SONIC-16) is driven to the SONIC-16 to identify whether the current register access is a read or write cycle.

$\overline{\text{RDYo}}$ (SONIC-16, AT9010) is driven after the system has accessed the SONIC-16's registers and the SONIC-16 has completed the I/O cycle. The SONIC-16 may use this signal to insert wait states in the cycle.

The following signals are driven during AT memory cycles to the boot EPROM:

$\overline{\text{EPROMRD}}$ (AT9010, EPROM) is the chip enable for the boot EPROM.

$\overline{\text{HAENB}}$ (Comp, AT9010) is a signal which indicates when the BIOS EPROM is being accessed. It is the output of a comparator which uses the base address of the EPROM (in CR2, bits<5..2>) and LA<23..17> as inputs for an address decode.

$\overline{\text{MEMR}}$ (AT bus, AT9010) is input to the AT9010 to indicate a memory read cycle during EPROM memory access.

MASTER CYCLE SIGNALS

A description of master signals generated while requesting the bus during memory read and write cycles is given below. Again, the format followed is SIGNAL (ORIGIN, DESTINATION).

HOLD (SONIC-16, AT9010 and GAL) is the SONIC-16's DMA request signal that notifies the AT9010 that the SONIC-16 is requesting the bus.

DRQx (AT9010, AT bus) is the conversion of HOLD. It is driven by the AT9010 through the AT bus to the DMA controller.

$\overline{\text{DACKx}}$ (AT bus, AT9010) is the DMA acknowledgment signal which grants the DMA controller ownership of the AT bus.

$\overline{\text{MASTER}}$ (AT9010, AT bus) is asserted to the AT bus when $\overline{\text{DACK}}$x is received. It disables the DMA buffers off the AT bus.

HLDAAT/HLDASONIC (AT9010 to GAL to SONIC-16) is generated by the AT9010 when it has been granted ownership of the bus. Due to bugs in the original AT9010, HLDAAT is extended by the GAL up to one clock before being driven to the SONIC-16 as HLDASONIC. For the AT9010B, the problem is corrected and HLDA is driven directly to the SONIC-16.

USER__PIN1/PRE-EMPT (AT9010, GAL) drives a 1 (or 0) to the GAL to enable (or disable) SONIC pre-emption. This is for the original AT9010 only.

The following signals are driven during the memory read or write cycles of master mode operation:

$\overline{\text{BALE}}$ (AT bus, AT9010) is high for the duration of master mode.

$\overline{\text{ADS}}$ (SONIC-16, AT9010) is an address strobe driven by the SONIC-16 which notifies the AT9010 of a valid address on the bus.

$\overline{\text{HAOE}}$ (AT9010, A-buffers) is an enable to the address buffers which gate the address from the adapter card to the AT bus.

MW-R (SONIC-16, AT9010) is input to the AT9010 by the SONIC-16 to indicate a read operation (signal low) or a write operation (signal high).

$\overline{\text{MEMR}}$ (AT9010, AT bus) is an AT9010 conversion of the signal MW/-R and indicates a SONIC-16 read cycle of system memory.

MEMW (AT9010, AT bus) is an AT9010 conversion of the signal MW-R and indicates a SONIC-16 write cycle to system memory.

$\overline{\text{SBHE}}$ (AT9010, AT bus) and (AT bus, AT 9010) denotes data on the most significant byte D<15..8> of the data bus. It notifies the system bus during a SONIC-16 memory write and notifies the AT9010 during a SONIC-16 memory read.

HDDIR (AT9010, D-Buffers) is an input to the data buffers which identifies the direction of a data transfer. It drives high for data transfers to the AT bus during a memory write cycle. It drives low for data transfers to the adapter card during a memory read cycle.

$\overline{\text{HDOE1}}$ (AT9010, D-buffer) enables the data buffer for the upper byte of data D<15..8>.

$\overline{\text{HDOE0}}$ (AT9010, D-buffer) enables the data buffer for the lower byte of data D<7..0>.

IOCHRDYBUS/IOCHRDYAT (AT bus to GAL to AT9010) are input and output signals for both the AT bus and the AT9010. For the original AT9010, the GAL translates the AT bus's IOCHRDYBUS into IOCHRDYAT and drives this signal to the AT9010 to insert wait states and complete a memory access. For the AT9010B, the AT bus drives IOCHRDY directly to the AT9010B.

$\overline{\text{RDYi}}$ (AT9010, SONIC-16) indicates to the SONIC-16 that a memory cycle has completed. The SONIC-16 will wait for this signal before re-asserting $\overline{\text{ADS}}$ to begin another cycle.

HUB MANAGEMENT SIGNALS

The following signals are generated during use of the in the hub management interface. The signals are presented in the format of SIGNAL (ORIGIN, DESTINATION) or SIGNAL (ORIGIN to DESTINATION /ORIGIN to DESTINATION).

MCRS/CRS (IR/M bus to BTL to SONIC-16) is the management carrier sense which indicates data on the SONIC-16's receive lines.

MRXD/RXD (IR/M bus to BTL to SONIC-16) is the management receive data.

MRXC/RXC (IR/M bus to BTL to SONIC-16) is the management receive clock.

$\overline{\text{PCOMP}}$ (SONIC-16 to BTL to M bus) is the SONIC-16's packet compression output pin which causes the transmitting RIC to inhibit the MRXC clock upon mismatch of the packet's destination address with the SONIC-16's CAM when the SONIC-16 is in managed-hub mode.

TXE/IRE (SONIC-16 to BTL to IR bus) is the SONIC-16's transmit enable signal.

TXD/IRD (SONIC-16 to BTL to IR bus) is the SONIC-16's transmit data.

TXC/IRD (Flip-flop to BTL and SONIC-16 to IR bus) is a 10 MHz transmit clock signal.

ACKI (IR bus, PAL) passes permission (ACKI = 1) or denial (ACKI=0) to the SONIC-16 from the RIC above it in the arbitration chain. (This is for transmission arbitration.)

ACKO (PAL, IR bus) passes permission (ACKO = 1) to transmit over the Inter-RIC bus to the RIC below the SONIC-16 if the SONIC-16 has permission to transmit and does not want to transmit. ACKO passes denial (ACKO = 0) if the SONIC-16 does not have permission (ACKI = 0) or the SONIC-16 wants to transmit (ACKI = 1).

TX__EN (PAL, BTL) is the transmit drive enable of the BTL. It is asserted when the SONIC-16 transmits (TXE = 1), has permission to transmit (ACKI = 1) and is configured for an external ENDEC (EXT = 1).

ACTNd (PAL, BTL) notifies the RICs that the SONIC-16 wants to transmit. It is asserted when the SONIC-16 transmits (TXE = 1) and it has permission to transmit (ACKI = 1).

ANYXNd (PAL, BTL) is asserted when the SONIC-16 transmits (TXE = 1) and it does not have permission to transmit (ACKI = 0). ANYXNd indicates a collision on the Inter-RIC bus.

ANYXNs (BTL, PAL) senses transmit collisions on the Inter-RIC bus and the network.

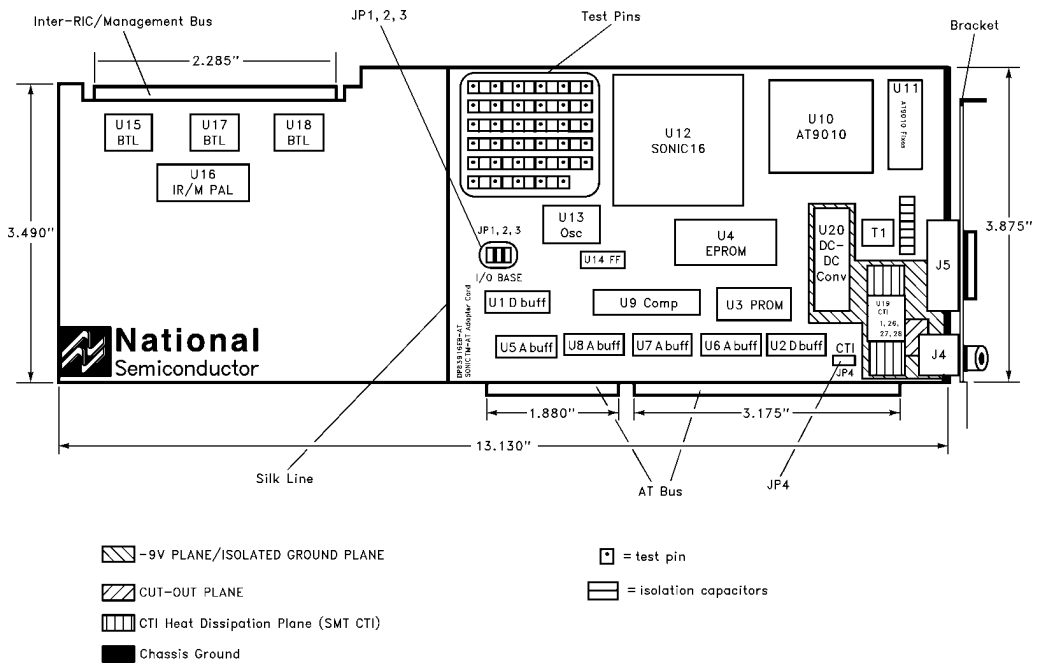
COL (PAL, SONIC-16) is driven by the PAL when there is a transmit collision on the Inter-RIC bus (ANYXN = 1) or there is a receive collision on the network (COLN = 1) and during either event the SONIC-16 is transmitting (TXE = 1).

$\overline{\text{COLN}}$ (IR bus to BTL to PAL) indicates receive collisions on the network.

APPENDIX V: DP83916EB-AT CARD AND COMPONENT PLACEMENT

This appendix illustrates the placement of the DP83916EB-AT components. Special layout considerations for the DP8392 (Coaxial Transceiver Interface) are identified. (Details regarding these considerations can be found in the data sheet for the DP8392.) The silk line illustrates a place on the board in which power and ground planes and Inter-RIC/Management signals are non-overlapping; hence, the full card can be cut into a half card along this line. JP1–JP3 and JP4 are located on the adapter card as shown. A bed of test pins is provided on the card. The test pin signals are defined in Appendix VI.

DP83916EB-AT Layout



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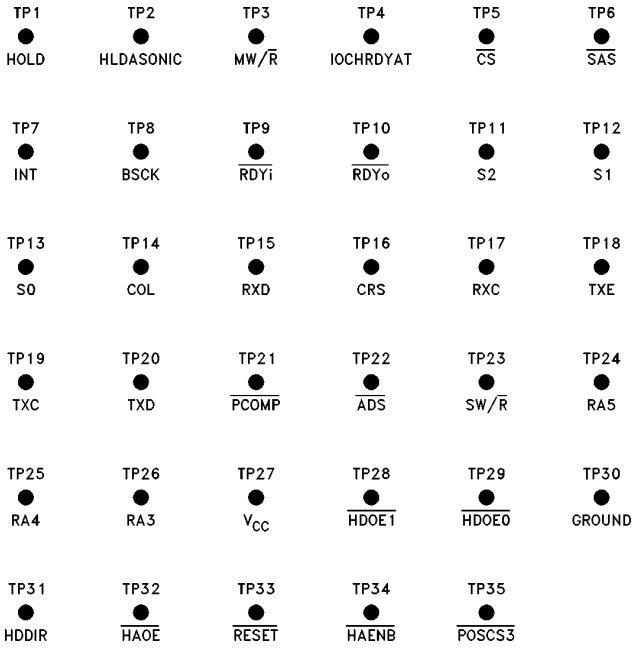
APPENDIX VI: TEST PIN LAYOUT

The test pins and their associated signals are presented below. Most other signals can be probed off the bus via an AT extender card.



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APPENDIX VII: DP83916EB-AT DESIGN CHANGE RECOMMENDATION

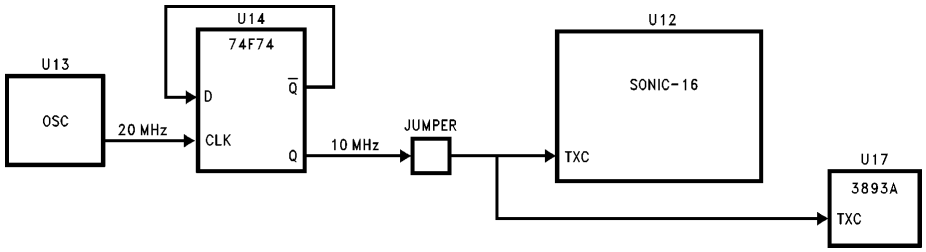
This appendix outlines a design change recommendation for future designs which implement both hub management and alternative media on the same card. There is a signal TXC which is driven from the flip−flop (U14) to the TXC pin (pin 12) of the SONIC-16 (U12) and the Inter-RIC/Management transmit BTL (U17). This signal is intended to provide a 10 MHz transmit clock to the SONIC-16's MAC when the SONIC is configured for hub management and hence, external ENDEC mode.

The current design of the DP83916EB-AT, however, provides TXC whether the SONIC-16 is in internal ENDEC mode (as a stand-alone node) or external ENDEC mode (as a hub manager). When the SONIC-16 is in internal ENDEC mode, it drives a 10 MHz signal (from the ENDEC) out of the chip. Because the flip−flop is also driving this node, a problem could arise if the clocks become out of phase.

Although no problems have arisen in lab testing, it is recommended that one of the following changes be made on future designs implementing the same functionality as the DP83916EB-AT. One of these changes will be implemented on the next version of this adapter card.

1. Place a jumper between the flip-flop output and the SONIC-16's TXC pin. Populate the jumper during hub management mode only.

Jumper Solution



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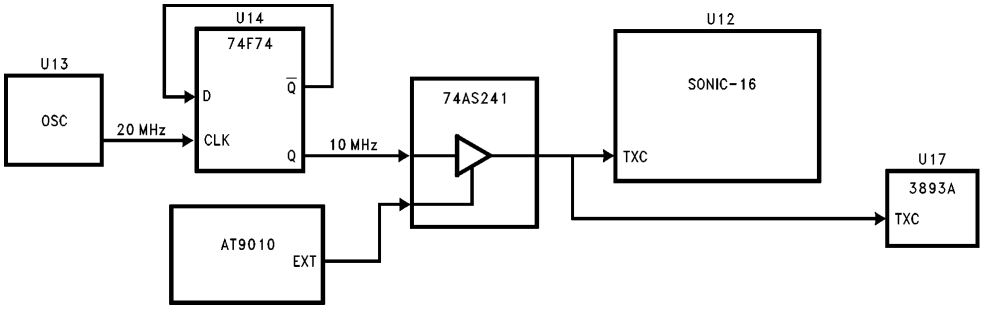
2. Place a TRI-STATE® buffer (74AS241A) between the flip-flop and the SONIC-16's TXC pin. Use the USER__PIN3 EXT from the AT9010 as the buffer enable. When EXT is 0 for internal ENDEC, the buffer will be disabled. When EXT is 1 for external ENDEC, the buffer will be enabled and the 10 MHz signal will drive into the SONIC-16's TXC pin and the transmit BTL.

TRI-STATE Buffer Solution



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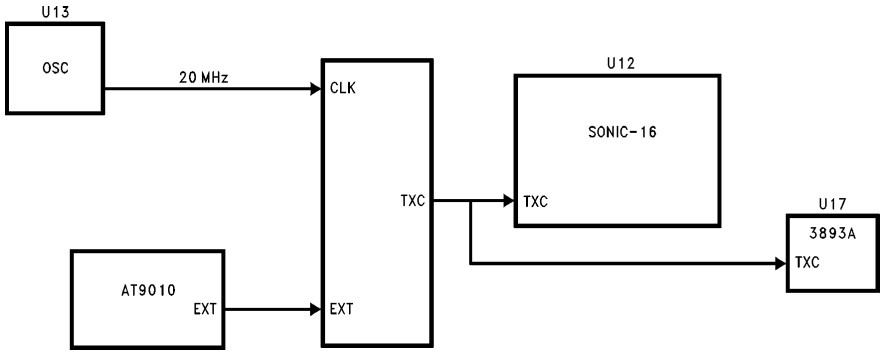
3. Delete the flip-flop (U14) and replace the PAL (U11) with a registered GAL (GAL16V8). Input the 20 MHz clock into the GAL's clock pin (pin 1). Define TXC in the pin assignment as TXC (pin 15). Change the device declaration to ''P16V8R''. Include in the GAL equations the following two equations: TXC := !TXC and TXC.OE = EXT. The signal TXC will only drive out when EXT is 1 for external ENDEC mode. When EXT is 0, TXC will be TRI-STATE.

Note: The ':=' defines that the equation for TXC is clocked on the rising edge of the 20 MHz signal. Since all equations in the GAL are asynchronous except for the TXC equation, there should only be a colon before the equal sign for the TXC equation.

This solution reduces the overall chip count by one and places all hub management signals in one IR/M GAL. However, because the 20 MHz and 10 MHz signals are traversing half the length of the card, radiation of noise is increased.

Inter-RIC/Management GAL Solution



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Additional Equations in GAL:

TXC : = !TXC
TXC.OE = EXT

APPENDIX VIII: COMPATIBILITY TESTING

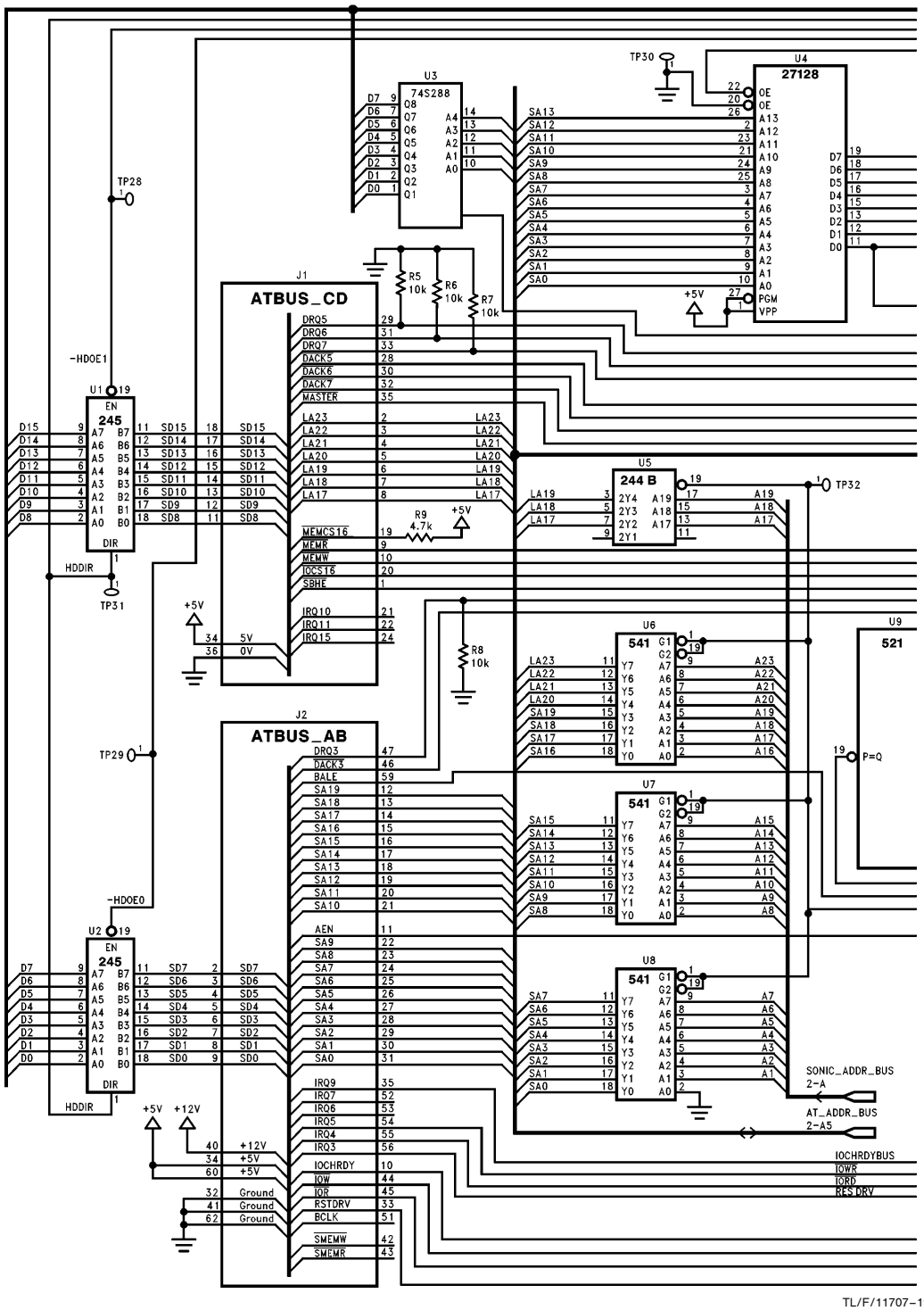
This appendix describes basic compatibility testing results for the DP83916EB-AT.

The DP83916EB-AT has been tested in various PC-AT/Compatible and EISA machines. The original AT9010 chip was used, SONIC-16 pre-emption was disabled and the master data transfer rate was 5 MB/s. The following basic tests were used:

1. Initialization and loopback
2. CAM load and Ethernet address PROM read
3. 16k EPROM enable/read
4. Simultaneous transmission/reception in two-node network
5. Continuous manual CTI loopback (set RCR to FE00h, set CTDA link field and CTDA register to current TDA address, set CR to 2h)

The DP83916EB-AT passed the basic tests in the following PC-AT/Compatible and EISA machines:

	Machine	Fastest Master Transfer Speed
AT:	ALR 386DX/33 MHz	8 MB/s
	AST 386/33 MHz	8 MB/s
	Clone 386	8 MB/s
	Clone 386SX/16 MHz	6.7 MB/s
	Clone 386/25 MHz	10 MB/s
	Clone 386/33 MHz	10 MB/s
	Compaq 286	8 MB/s
	Compaq 486DX/50 MHz	6.7 MB/s
	Dell 386/25 MHz	6.7 MB/s
	Dell 486SX/20 MHz	6.7 MB/s
	Dell 486DX/50 MHz	8 MB/s
	Everex 386SX/16 MHz	10 MB/s
	Everex 386/33 MHz	10 MB/s
	Zeos 486/33M Hz	10 MB/s
EISA:	ALR EISA 386DX/33 MHz	8 MB/s
	AST EISA 486/33 MHz	8 MB/s
	Compaq EISA 386/33 MHz	6.7 MB/s
	Compaq EISA 486SX/25 MHz	6.7 MB/s
	Compaq EISA 486DX/50 MHz	10 MB/s
	Dell EISA 486/25 MHz	8 MB/s
	Dell EISA 486DX/33 MHz	8 MB/s
	HP EISA 486/33 MHz	8 MB/s
	NEC EISA 386/33 MHz	8 MB/s



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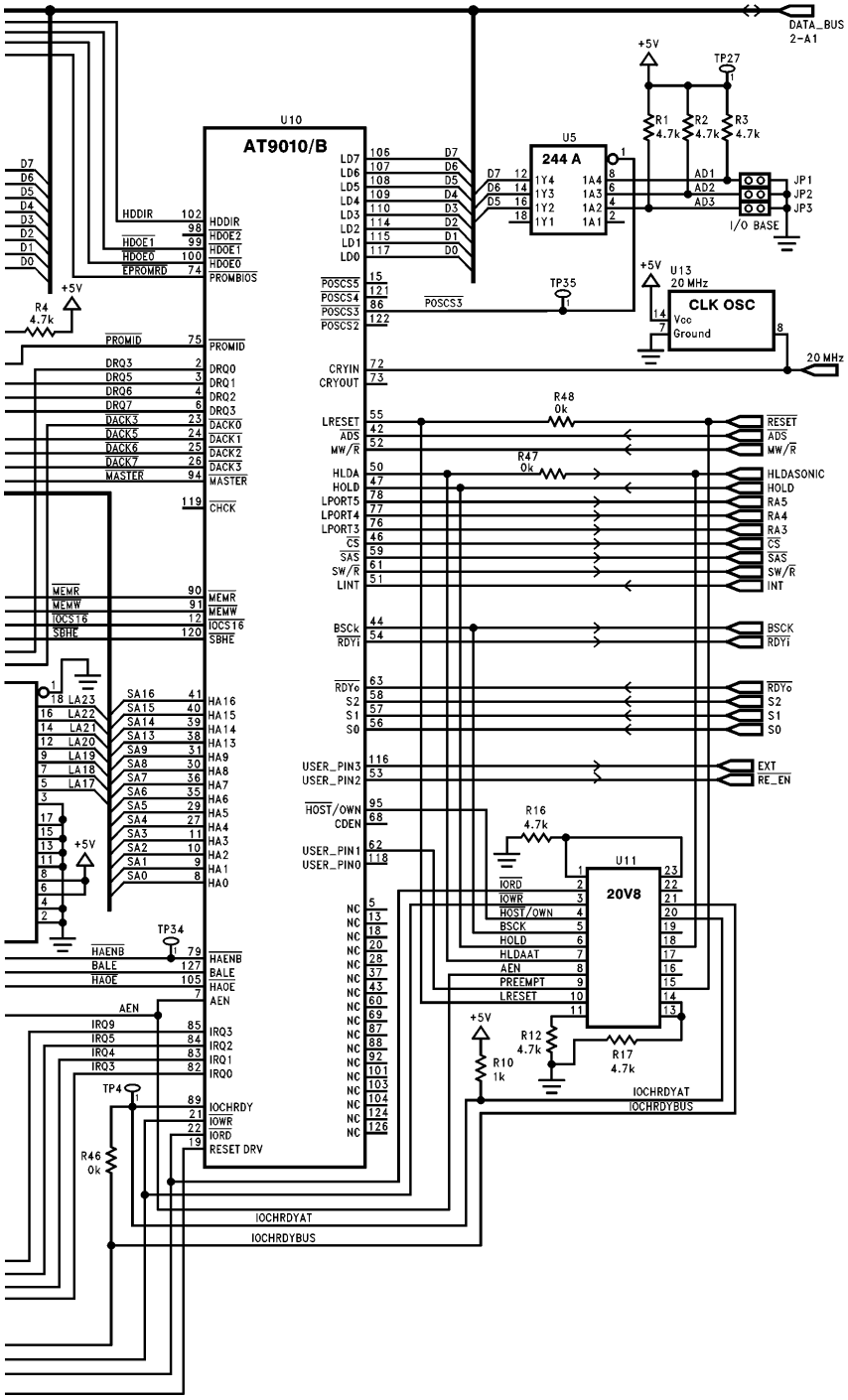
AT Bus Interface



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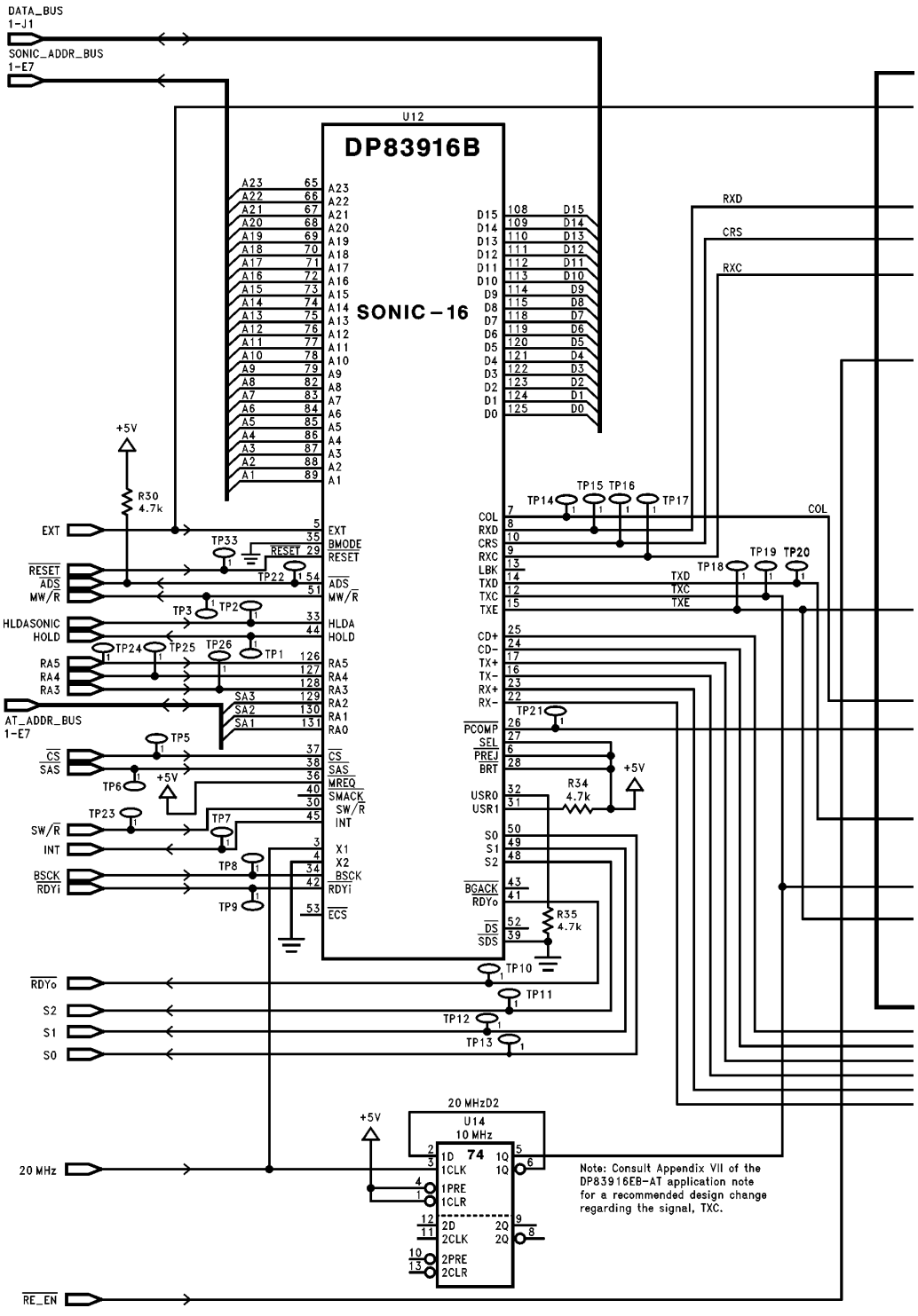
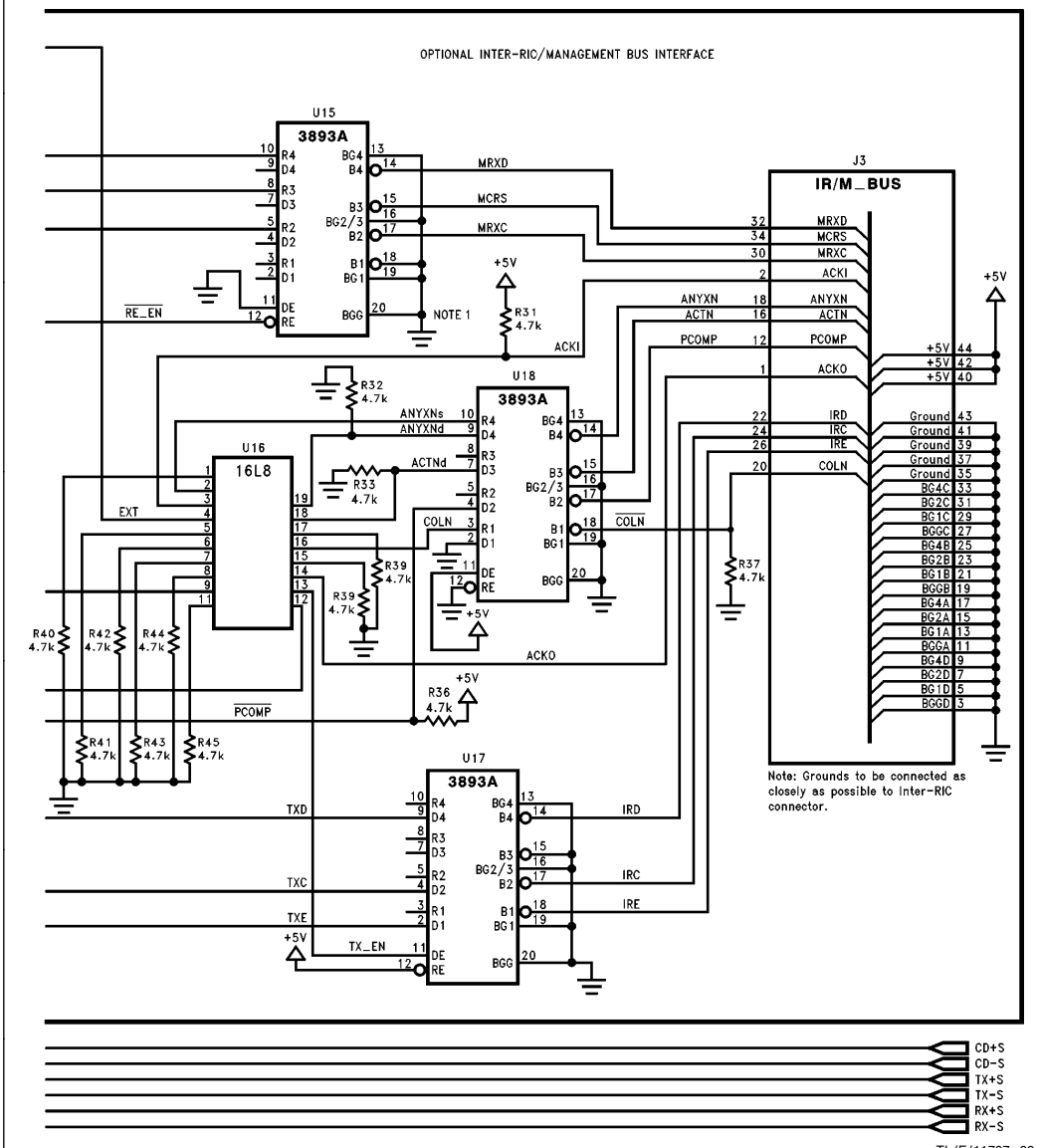
Note: For original AT9010, install U11 and leave R46, R47 and R48 open. For AT9010B install R46, R47 and R48 and leave U11 open.

AT Bus Interface (Continued)



SONIC and Inter-RIC/Management Interface



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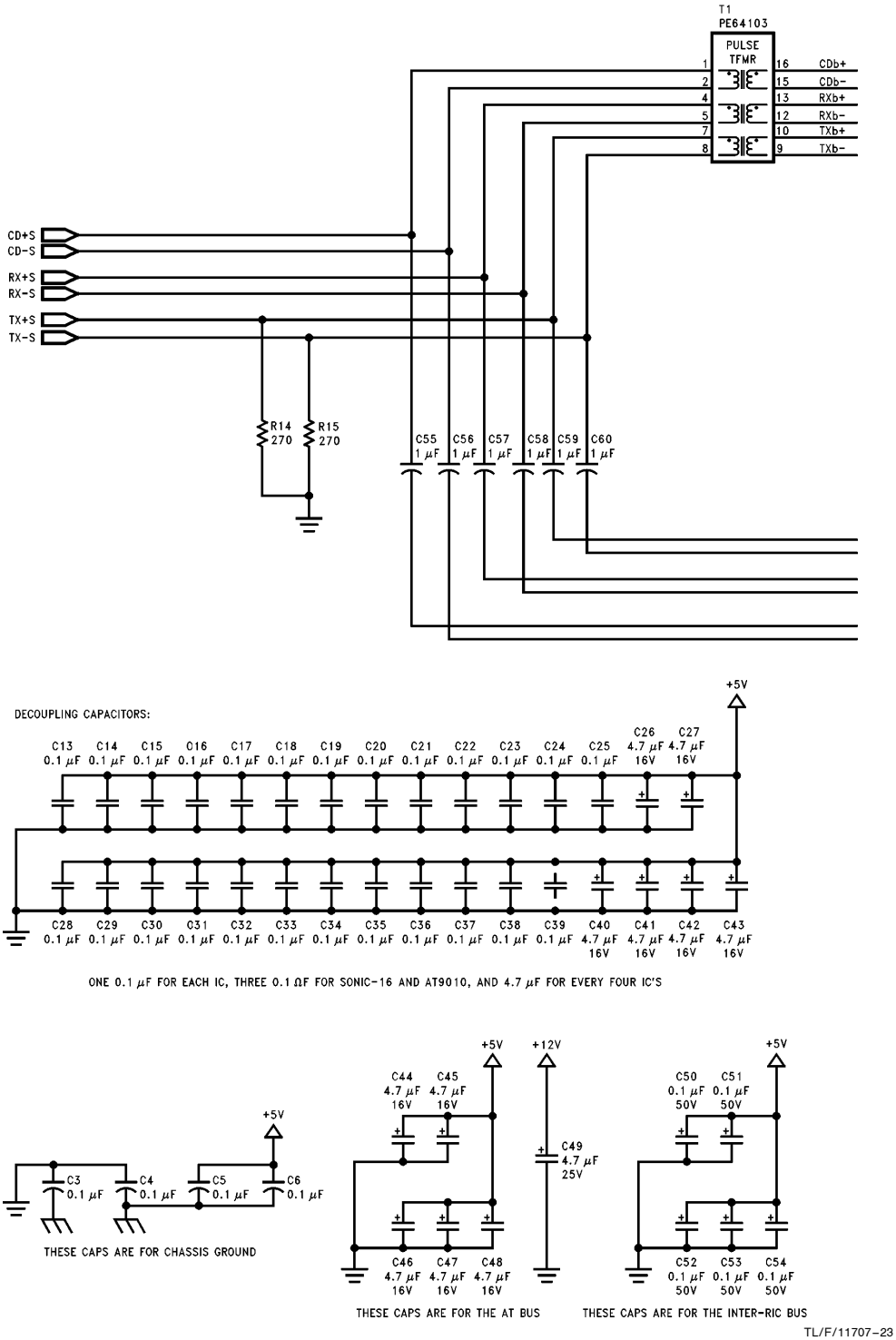
SONIC and Inter-RIC/Management Interface (Continued)



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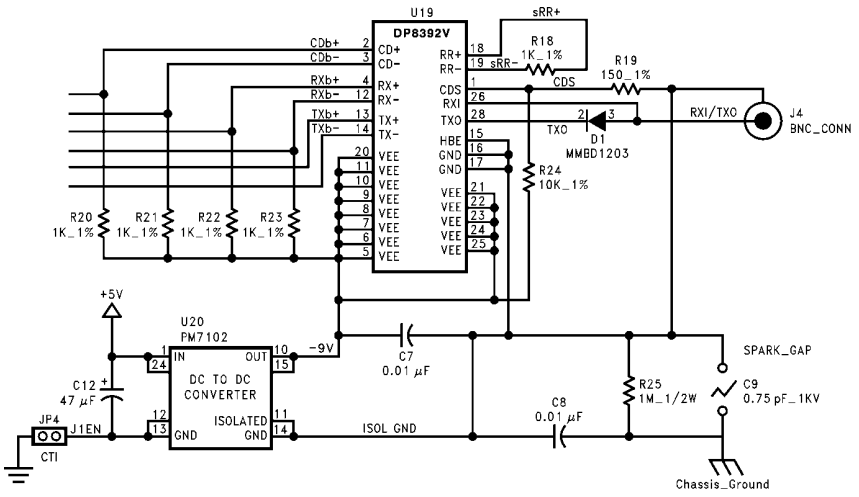
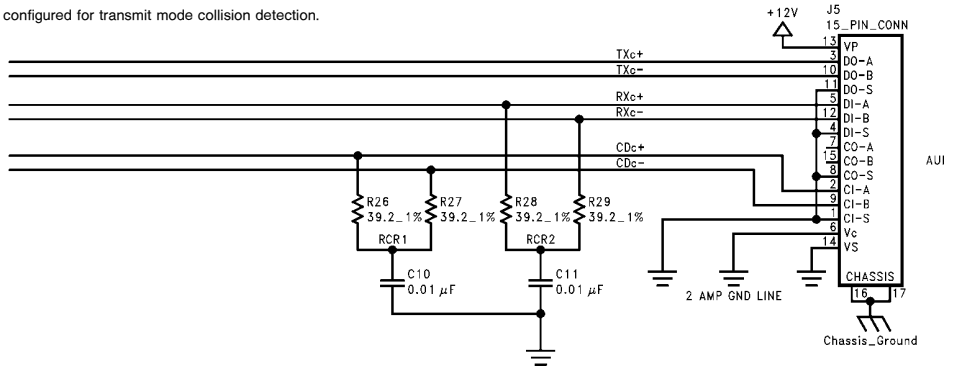
Media Interface



Note: CTI configured for transmit mode collision detection.



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Note: Unless otherwise specified, resistors are 5%, 1/4W.

Media Interface (Continued)

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